N00014-22-1-2385

ONR Pulsed Tactical Effector for Regulated Attack (PTERA): Annual Review 2023

07/01/2022−08/31/2023

November 15, 2023

Prepared by:
Michelle Paquette
paquettem@umkc.edu

Program Point of Contact:
Travis Fields
Missouri Institute for Defense and Energy
University of Missouri-Kansas City
816-235-1291
fieldstd@umkc.edu

REPORT DOCUMENTATION PAGE

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED	
		START DATE	END DATE
20231115	Annual Review	20220701	20230831

4. TITLE AND SUBTITLE

ONR Pulsed Tactical Effector for Regulated Attack (PTERA): Annual Review 2023

5a. CONTRACT NUMBER	5b. GRANT NUMBER	5c. PROGRAM ELEMENT NUMBER
	N00014-22-1-2385	
5d. PROJECT NUMBER	**5e. TASK NUMBER**	**5f. WORK UNIT NUMBER**

6. AUTHOR(S)

Allen, R.; Berber Halmen, F.; Bhattarai, G.; Caruso, A.; Dhungana, S.; Durbhakula, K.; Eifler, J.; Fields, T.; Hamdalla, M.; Hassan, A.; May, J.; Paquette, M.; Rahman, M.; Rao, P.; Rinck, D.; Sisk, S.; Sobhansarbandi, S.; Young, S.; Usenko, A.; West, R.

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Missouri Institute for Defense and Energy
University of Missouri-Kansas City
5110 Rockhill Rd
Kansas City, MO 64110

8. PERFORMING ORGANIZATION REPORT NUMBER

PTERA_Grant_Annual_Review_OCT2023

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)	11. SPONSOR/MONITOR'S REPORT NUMBER(S)
Office of Naval Research One Liberty Center, 875 N Randolph Arlington, VA 22203	ONR	

12. DISTRIBUTION/AVAILABILITY STATEMENT

Distribution Statement A: Approved for public release; distribution is unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

The Pulsed Tactical Effector for Regulated Attack (PTERA) Grant program aims to push the state-of-the-art in reconfigurable antennas, compact sources, edge-based signals analysis hardware/software, and UAS combat survivability that collectively enable leapfrog technology for aerial directed energy systems. This report compiles presentations from the PTERA Grant Annual Technical Review, which was held at the University of Missouri-Kansas City (UMKC) on October 10 2023, and covers technical program updates for the PTERA-G subprograms for the year 1 period of performance (07/01/2022–08/31/2023) as well as plans for the year 2 period of performance.

15. SUBJECT TERMS

high power microwaves; pulsed power sources; unmanned aerial systems, reconfigurable antennas; machine learning; gallium nitride power amplifiers; drift-step-recovery diodes; silicon avalanche shapers; thermal management; RF shielding; electromagnetic interference; MXenes; cyber operations; field programmable gate arrays; edge devices; low-k dielectrics; electromagnetic pathogen inactivation

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES
a. REPORT	b. ABSTRACT	C. THIS PAGE		
U	U	U	UU	148

19a. NAME OF RESPONSIBLE PERSON	19b. PHONE NUMBER *(Include area code)*
Travis Fields	816-235-1291

Page of

PREVIOUS EDITION IS OBSOLETE.

STANDARD FORM 298 (REV. 5/2020)
Prescribed by ANSI Std. Z39.18

Executive Summary

The Pulsed Tactical Effector for Regulated Attack (PTERA) Grant program aims to push the state-of-the-art in reconfigurable antennas, compact sources, edge-based signals analysis hardware/software, and UAS combat survivability that collectively enable leapfrog technology for aerial directed energy systems. The program is operated as a series of sub-efforts within each of these areas.

The PTERA Grant Annual Review was held at the University of Missouri-Kansas City (UMKC) on October 10 2023 as part of the larger UMKC ONR Annual Review, with program performers as well as academic, industry, and government stakeholders in attendance. The review covered technical program updates for the PTERA-G subprograms for the year 1 period of performance (07/01/2022−08/31/2023) as well as plans for the year 2 period of performance (see agenda below). The presentations are compiled herein.

October 10	**PTERA Grant (All Sessions UNCLASSIFIED/DISTRO A)**
Time	**Title**
1300-1315	Welcome, Agenda, and PTERA-G Overview
1315-1400	Multifaceted Reconfigurable Antennas for UAS Applications
1400-1435	Innovations in Design and Fabrication of DSRD/SAS Sources
1435-1450	Break
1450-1515	Pushing Beyond GaN Limits through Cooling
1515-1545	Enabling Cyber Capabilities
1545-1615	Sprayable Coatings for Broadband EMI Shielding
1615-1700	Year 2 Research Directions Overview

UMKC/MIDE ONR Annual Review

10OCT2023

Roy Allen
roy.allen@umkc.edu

Uriah Tobey

Uriah.tobey@umkc.edu

Travis Fields
fieldstd@umkc.edu

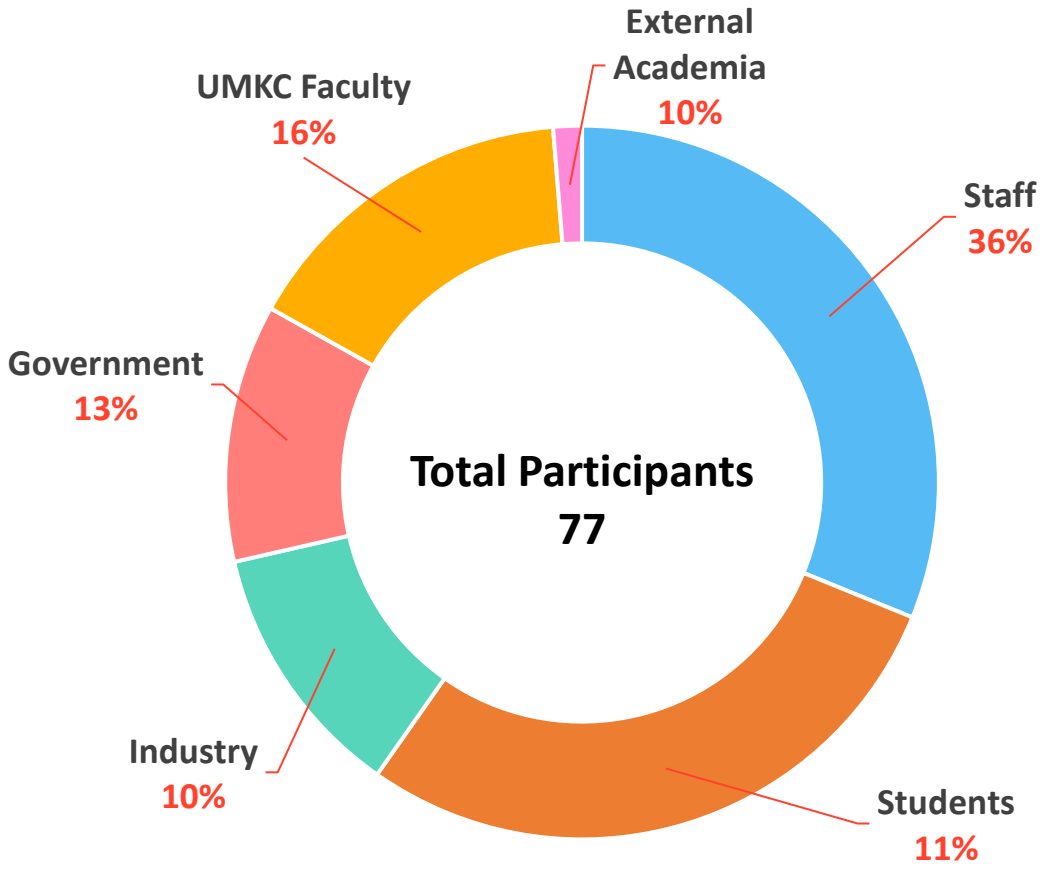
Annual Review Purpose and Structure

Review Objectives:

1. Provide current **missions** and **concepts of employment** for **UAS** & ground and air-based **DEW** and **Cyber** technologies

2. Disseminate latest **technical** foci and progress/results

3. Solicit **feedback** (through discussion) from technical experts, collaborators, and stakeholders to **align** PTERA and CUCKOO efforts with **operationally-needed missions**



Review Overview

Tuesday
1300-1700

Grant Year 1 Review

High risk, high reward technology review for air-emplaced offensive and defensive missions

UMKC Administration Building

Unclassified // Distribution A

Wednesday
0800-1700

Program Closeout

CsUAS program history, results, recommendations, and impact of HPM technologies, wargaming, lethality modeling, and RF coupling

1300 Summit St, Kansas City, MO

Classified // Distribution D

1730-1930

Dinner at Char Bar

Thursday
0730-1630

Contract Year 2 Review

Review of A) compact HPM source technologies, B) UAS design, survivability, and testing, and C) signals collection and cyber ops

1300 Summit St, Kansas City, MO

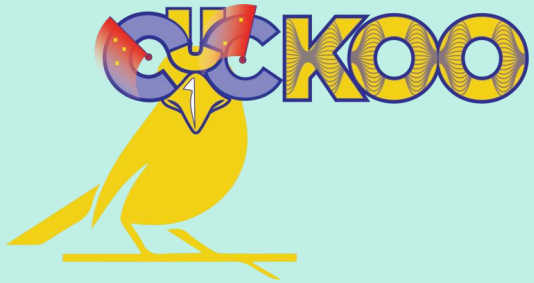
Classified // Distribution D

1800-2100

Chiefs vs. Broncos

*Game tickets not included in registration fee

Friday
0900-1430



Program Kickoff

Overview of program organization, mission, KPPs, and initial technology initiatives for HPM, UAS, and Cyber

1300 Summit St, Kansas City, MO

Classified // Distribution D

MIDE Overview

MIDE MISSION

Improve the quality of life by bridging academia with industry to address *wicked* problems.

MIDE VISION

Lead in the development of technologies that *directly* and positively impact society, and to grow the leaders of tomorrow in a *team-focused* culture

MIDE Personnel

- ***100+ actively paid MIDE personnel***
- ***25% Faculty, 25% Staff, 50% Students***
- Chemistry, Physics, History, Engineering, and Computer Science

Current Portfolio

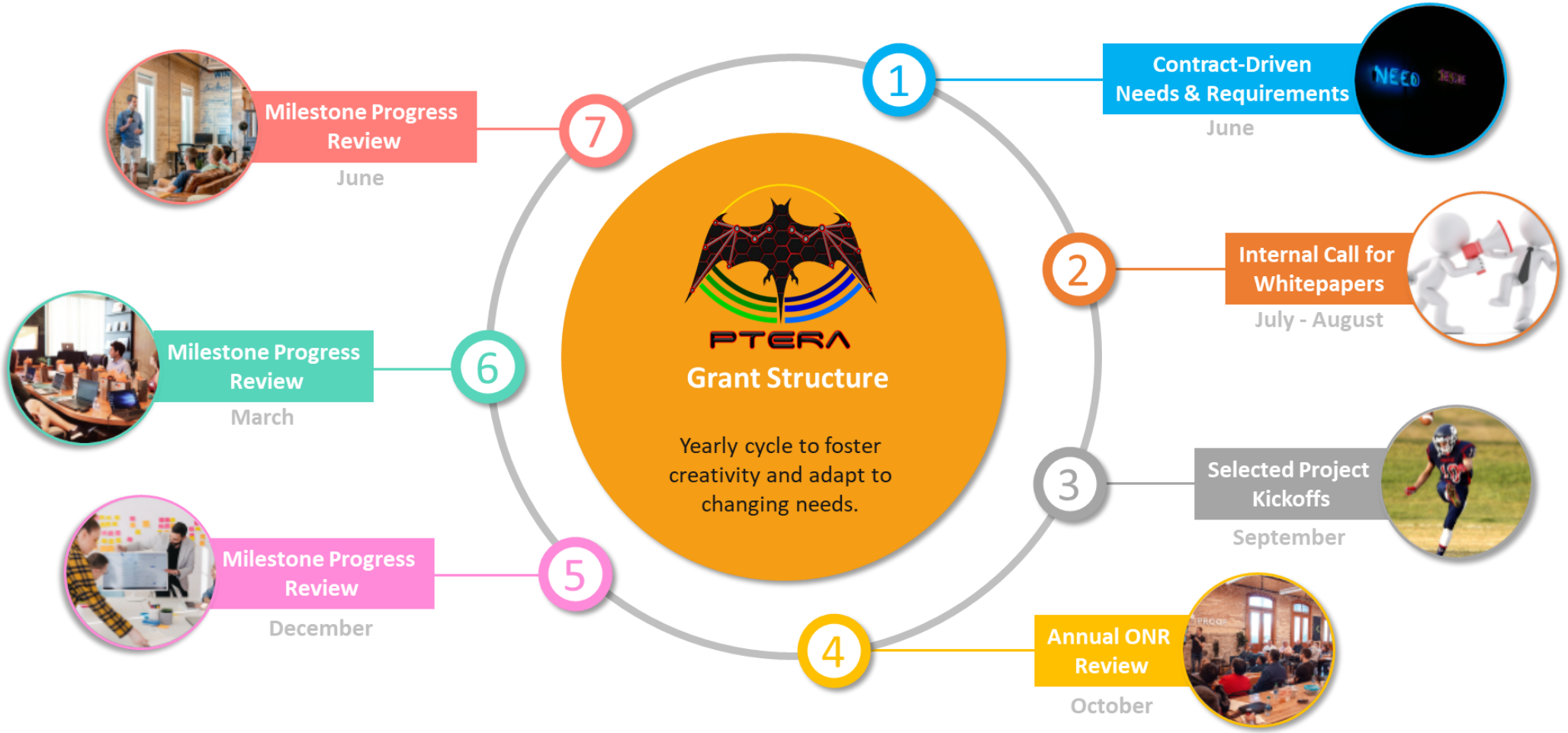
Directed Energy: *Solid-state pulser design and fabrication, ultracompact sources, high power antenna design, lethality testing, simulations (all aspects), and biological safety/interactions.*

Unmanned Aircraft Systems: *Fixed-wing, multirotor, and VTOL-Retrofit, payload integration, flight testing, customization, guidance and control, low observability (RCS & acoustics)*

Cyber Operations: *automated collection, vulnerability analysis, and exploit delivery. Primary focus is on forward-deployed (air-emplaced) delivery.*

PTERA Grant Overview

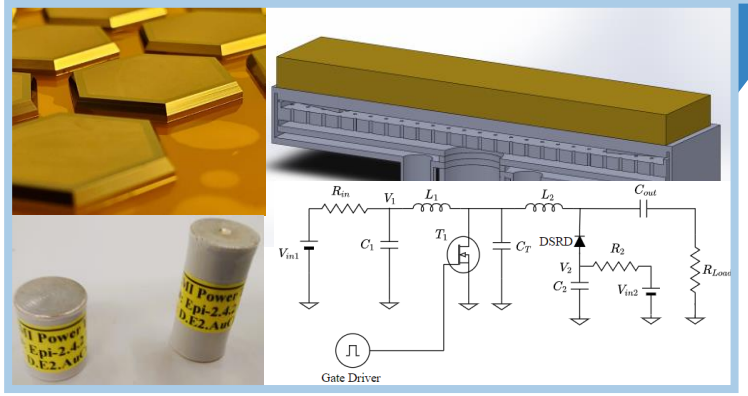
The PTERA Grant is a holistic research effort to **identify**, **develop**, and **evaluate** technologies that provide leap-ahead multi-mission capabilities. Three primary thrusts: (1) **HPM** pulsers, diodes, and antennas, (2) survivable **UAS** technologies, and (3) information operations **(IO/Cyber)** hardware/software.



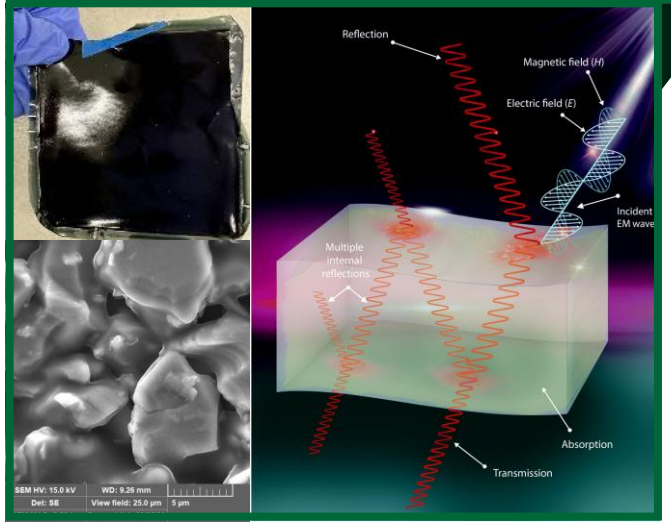
Funding provided by ONR under grant N00014-22-1-2385

2022-2023 PTERA Grant Research Teams

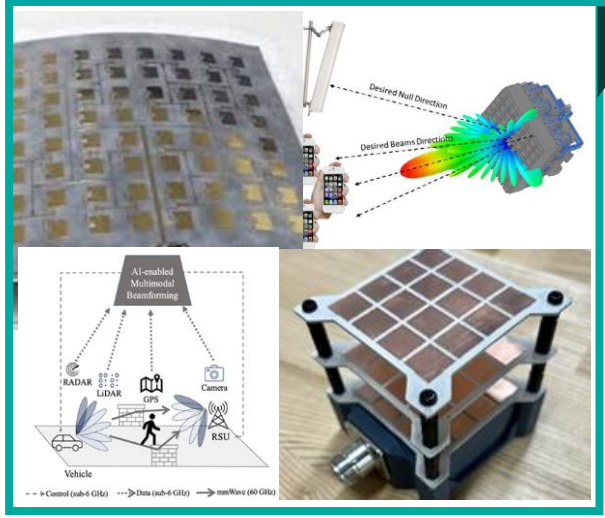
HPM Pulsers



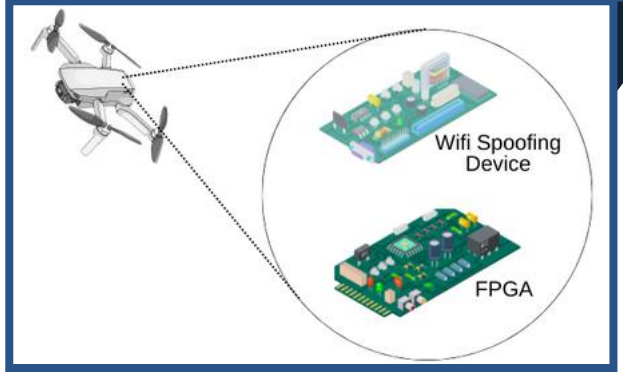
RF Shielding



High Power Antennas



Information Operations



Funding provided by ONR under grant N00014-22-1-2385

Multifaceted Reconfigurable Antennas for UAS Applications

PTERA Grant Annual Review

October 10, 2023

Funding provided by ONR under grant N00014-22-1-2385

Kalyan Durbhakula kalyandurbhakula@umkc.edu
Mohamed Hamdalla mhamdalla@umkc.edu

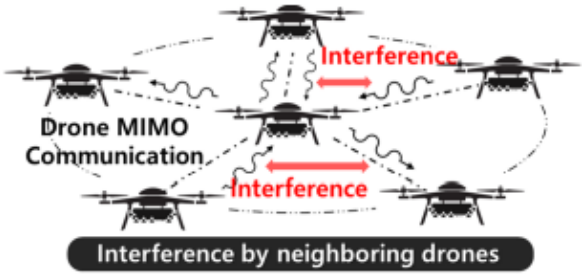
Motivation: Why Reconfigurable Antennas are the future?

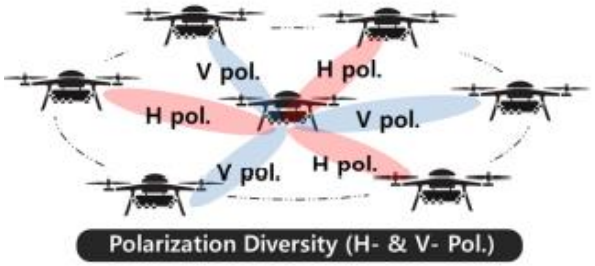
Applied Motivation: High input power, Frequency reconfigurability, Compact, Lightweight, Low DC power, and Beam Steering.

Fundamental Motivation: Determine performance tradeoffs from employing different technologies assisting improvement in critical antenna metrics (bandwidth (BW), gain, steerability).

Relevancy to PTERA Mission: An antenna demonstrating real-time frequency reconfigurability within the targeted frequency spectrum (GSM, GPS, Sub-1 GHz IoT, Wi-Fi, X-, and Ku-bands), high boresight gain, and rapid beamforming or beam steering.

Air to Air communication





Air to Ground communication

Antenna Requirements :

- Wideband
- High gain
- Operation at different frequencies
- Beam steerability
- Narrow beam radiation

Solution: Reconfigurable Antennas

Motivation: Why Reconfigurable Antennas are the future?

State-of-the-Art (SOTA):

- A microstrip patch antenna with radiofrequency (RF) switch(es)
- Small form factor, low DC power consumption, low profile, and the ability to enable reconfigurability efficiently.

***Deficiency in the SOTA*:**

- Narrow frequency reconfigurability range (20% BW and 25% f_{center} reconfigurability).
- Low realized gain

Primary Objective: A lightweight, high-power antenna array that can achieve > 15 dBi peak gain at the f_{center} while demonstrating BW (from 3% to 150%), f_{center} (from 1 to 5.8 GHz) reconfigurability, and beam steering, or beamforming using RF switches.

Target metrics

Metric name	Threshold	Objective	Ideal
Frequency Reconfigurability (%)	25	35	50
Bandwidth Reconfigurability (%)	20	50	150
Operating Range [GHz]	L-band to S-band	L-band to C-band	L-band to Ku-band
Antenna Peak Gain (dBi)	3	5	7
Antenna + Metamaterial Peak Gain (dBi)	7	10	15
Beam Steering (°)	20	45	65
Form factor (mm^3)	150 x 150 x 50	100 x 100 x 45	50 x 50 x 25
Weight (lbs.)	< 10	< 3	< 1
Power Handling (kW)	> 1	> 100	> 1000

Agenda

Topics:

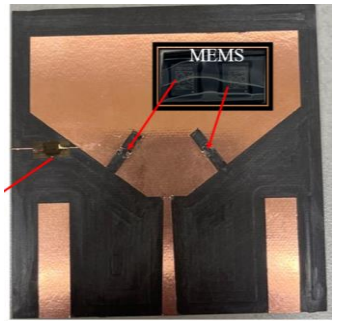
I. MEMS-based Superwideband Reconfigurable Antenna Design

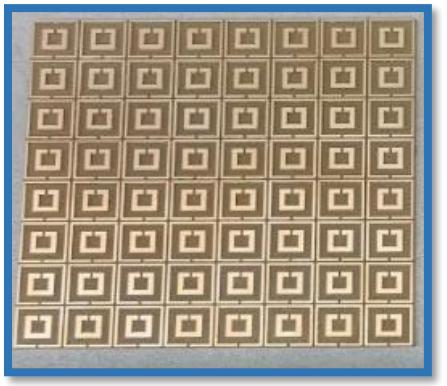
II. UWB Gain Enhancement Using Modified Split Ring Resonators

III. Artificial Intelligence-based Modular Beamforming using software-defined radios (SDRs)

IV. Reconfigurable Nonlinear Antenna

V. Reconfigurable High Power Metasurface Lens Antenna



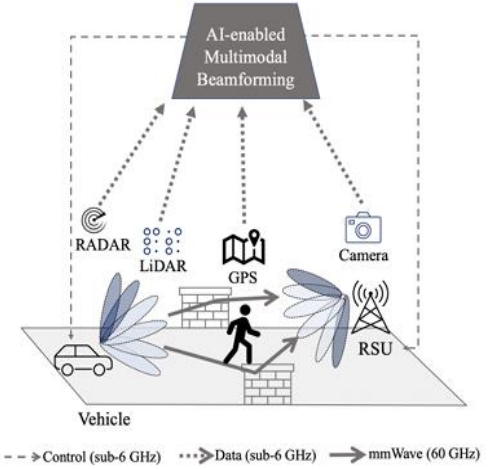


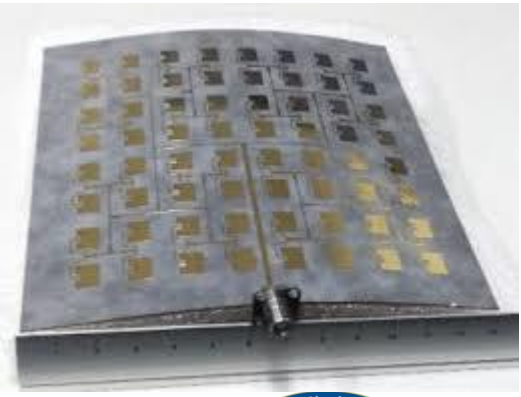
Ongoing Efforts:

I. Genetic Algorithm-based Beam Steering

II. Flexible substrate-based Conformal Antennas

III. Non-Dispersive Waves



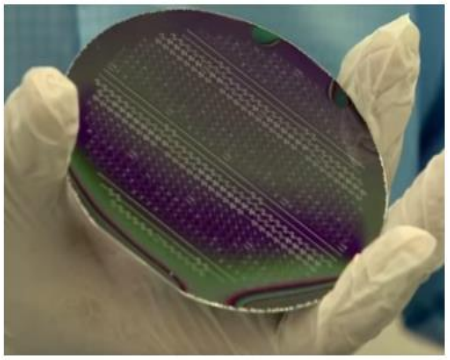


1. D. Roy et al., “Going Beyond RF: How AI-enabled Multimodal Beamforming will Shape the NextG Standard”.
2. T. Bai et al. "Design of cylindrical conformal array antenna based on microstrip patch unit." *The Applied Computational Electromagnetics Society Journal (ACES)*, pp. 1008-1014, 2021.

Mini-Gantt Chart

Milestone	AUG	SEP	OCT-NOV	DEC – FEB	MAR – MAY	JUN – AUG
Literature Review						
Modeling & Simulation						
Materials & Components Procurement						
Fabrication & Assembly						
Testing & Validation						

Why Should You are?



5G MEMS antenna startup raises £2.3m

Business news | August 12, 2020

By Nick Flaherty

MATERIALS & PROCESSES

RF TRANSMISSION

Why MEMS?

Why Metamaterials?

Why Nonlinear Circuits?

Nokia to produce broadband network electronics products in the United States

NOKIA

PUBLISHED: AUG 05, 2023, 4:47 AM

so far: 1) broadband matching of electrically small and highly reactive antennas (short dipoles and small loops) [2]–[18]; 2) broadband nearly non-dispersive metamaterials and metasurfaces [19]–[31]; 3) broadband distributed amplifiers and broadband power amplifiers based on compensation of parasitic capacitances [32]–[34]; 4) highly efficient power amplifiers based on the "inverse" inter-stage matching [35]; 5) broadband phase shifters based on an ordinary phase-lag network followed by a non-Foster phase-lead network [36]–[39]; 6) broadband hybrid junctions and the Wilkinson power dividers [40]; 7) broadly tunable voltage-controlled oscillators based on the extension and linearization of varactor characteristic by addition of negative capacitors [41], [42]; 8) broadly tunable self-oscillating antennas [43]–[46]; and 9) broadly tunable substrate integrated waveguide

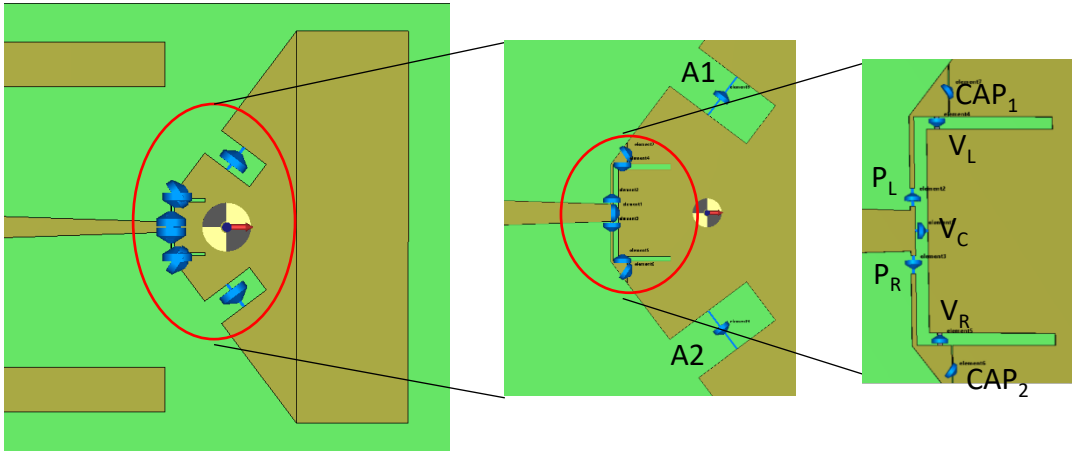
Why SDRs?

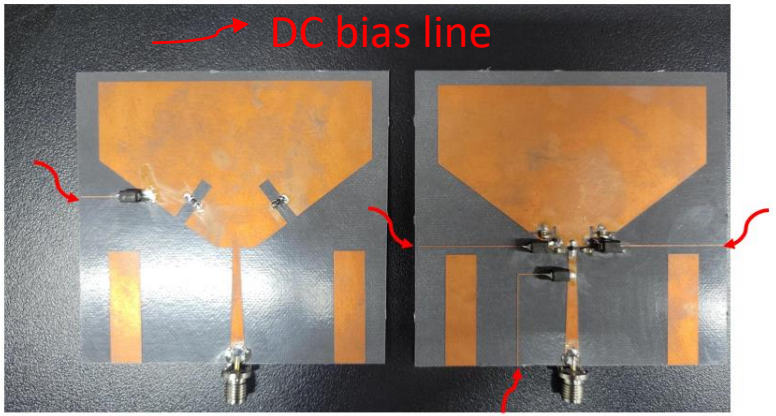
FPGAs in SDRs for Radar, EW and MilCom Applications

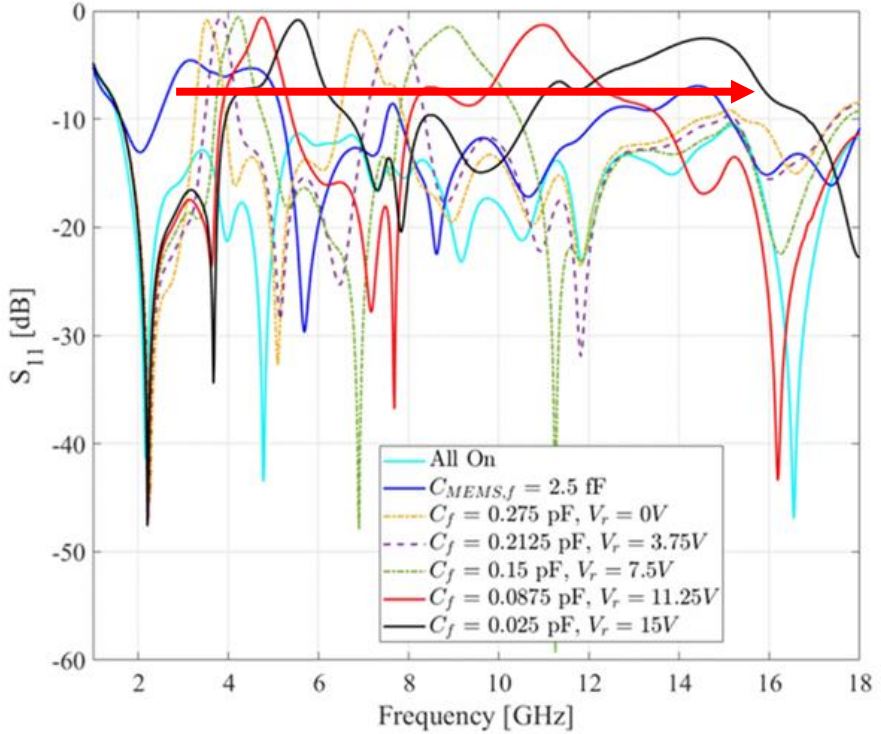
Brandon Malatest

Software-defined radios (SDRs) are becoming increasingly popular across various applications, including electronic warfare (EW), radar and military communications (MilCom). The flexibility and versatility of SDRs enable them to adapt to changing requirements and challenges, making them an ideal choice for these applications. For instance, in EW applications, SDRs can detect and identify signals from various sources and jam them to disrupt communication, providing a significant tactical advantage on the battlefield. In the same way, SDRs can be used for radar applications to detect and track targets in real-time, making them an ideal choice for military applications. In MilCom, SDRs offer interoperability between different types of radios, allowing different forces to communicate seamlessly, regardless of the radio system used all while being able to adapt to changing requirements, making them ideal for dynamic battle- field conditions. This flexibility enables troops to communicate effectively, make critical decisions in real-time and improve overall battlefield situational awareness. All these features and applications are enabled by SDRs and the underlying use of field-programmable gate arrays (FPGAs).

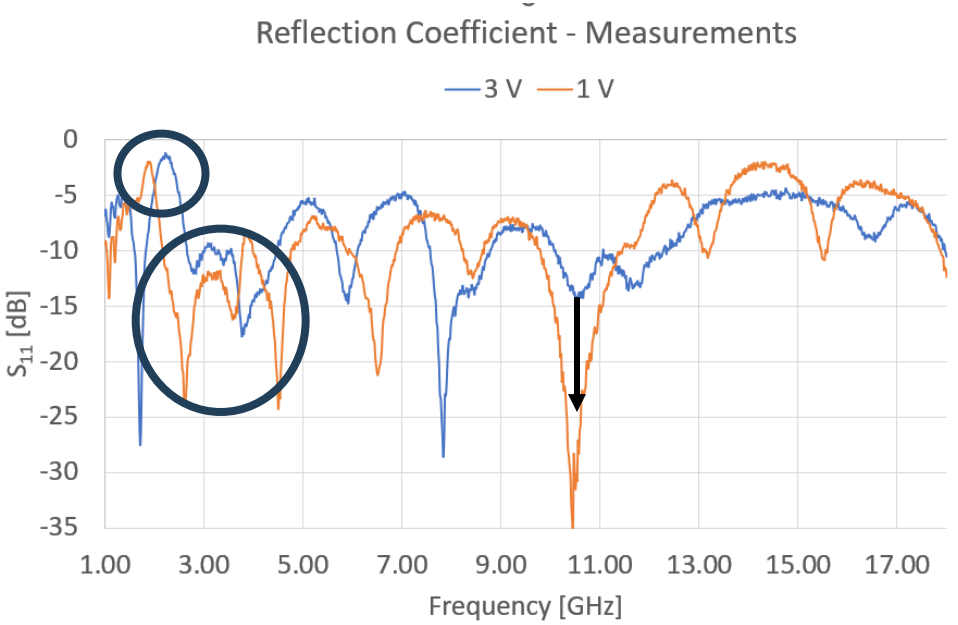
Bandwidth & Center Frequency Reconfigurability using RF Switches



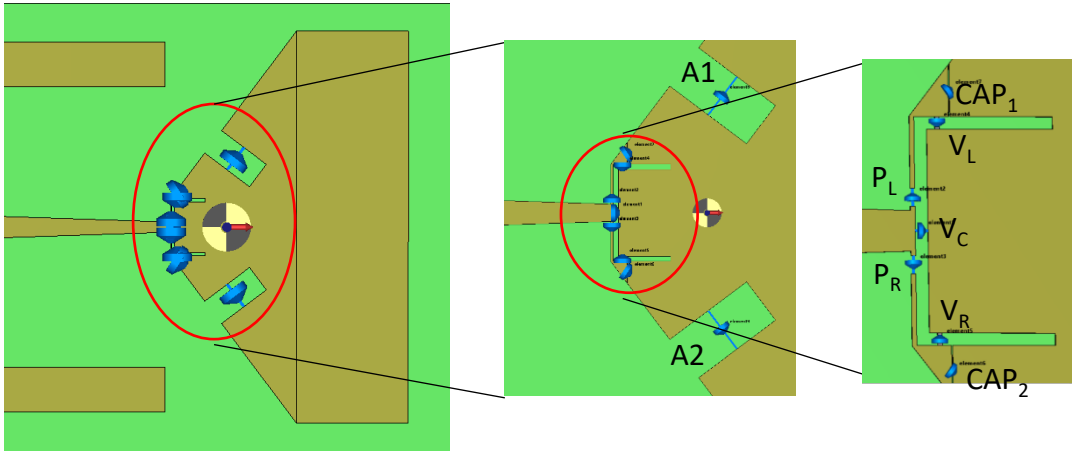


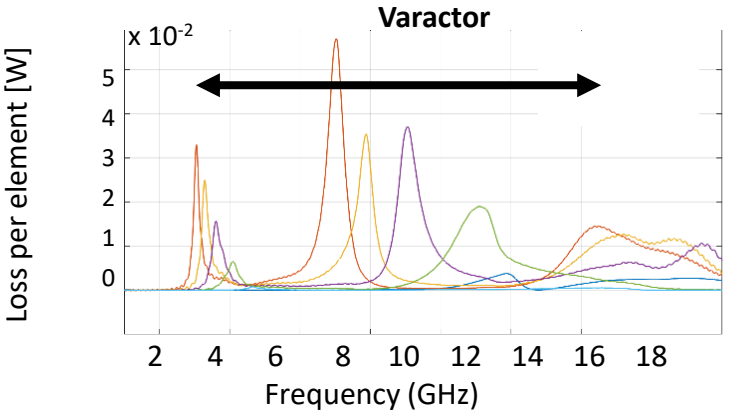


- Used bigger size varactors with a smaller capacitance ratio due to fabrication challenges

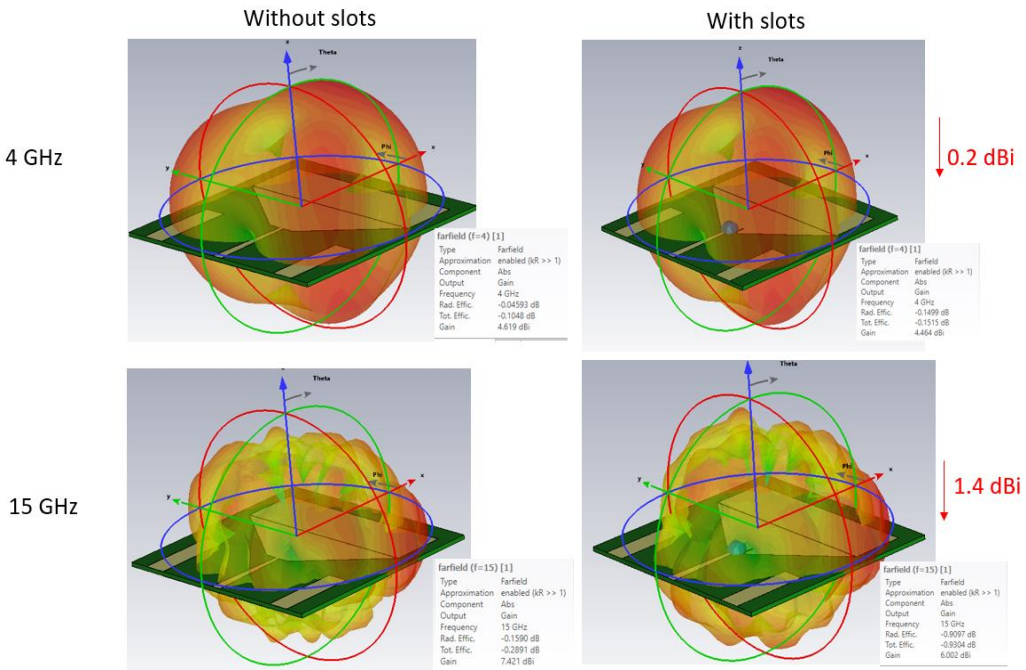


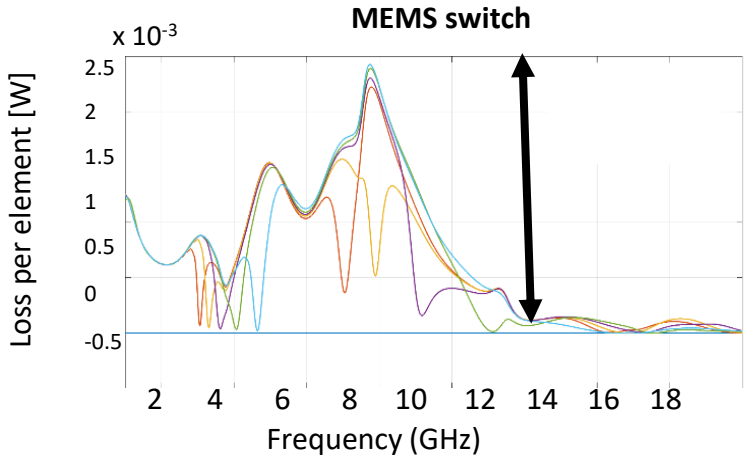
Bandwidth & Center Frequency Reconfigurability using RF Switches





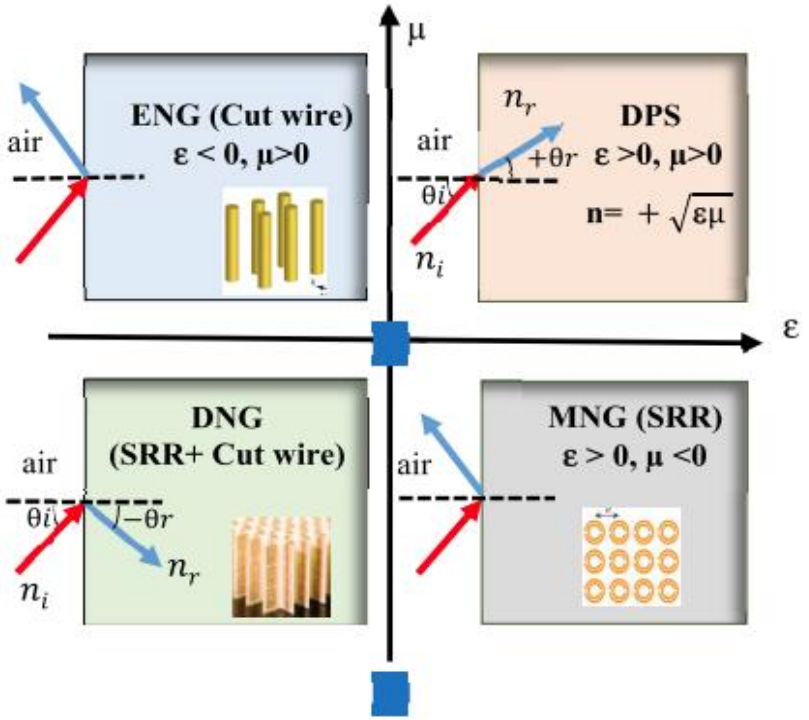
Radiation Pattern



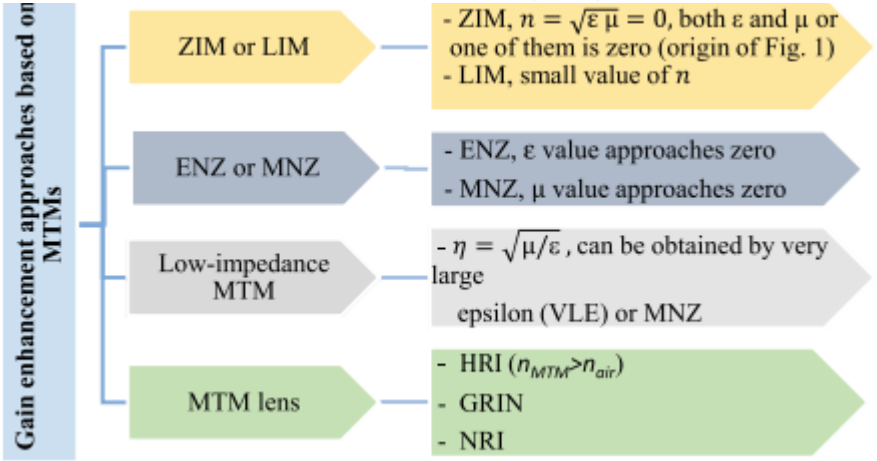


- Power loss is 10x higher in varactors than MEMS switches
- Minimum to no effect on the radiation pattern
- Reconfigurability from:
  - Simulations - MEMS switches - 2.4 to 6 GHz F_{center},
  - Simulations - Varactors - 3.8 to 17 GHz F_{center},
  - Experiments – 2.93 to 3.8 GHz F_{center}, 1.6 to 1 GHz BW

Introduction to Metamaterials



Zero-index material (ZIM)



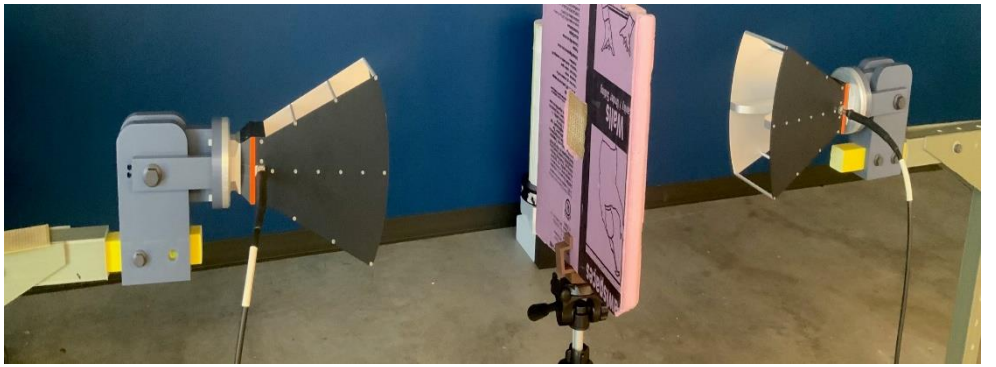
- Antennas with small form factor and high gain are desired, however, antenna gain is directly proportional to the antenna aperture area.
- Modified split ring resonators (MSRRs) generate positive +ve permeability as opposed to -ve permeability by traditional SRRs.
- The existing MSRRs in literature are limited to narrowband (< 500 MHz) applications.
- A MSRR that works over a broad frequency range (1 - 18 GHz) is desirable to cover a wide range of applications with high realized gain.

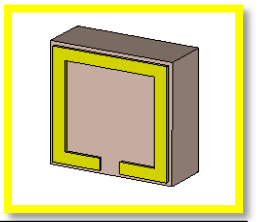
B. A. F. Esmail, S. Koziel and S. Szczepanski, "Overview of Planar Antenna Loading Metamaterials for Gain Performance Enhancement: The Two Decades of Progress," in IEEE Access, vol. 10, pp. 27381-27403, 2022, doi: 10.1109/ACCESS.2022.3157634.

UWB Gain Enhancement using MSRRs

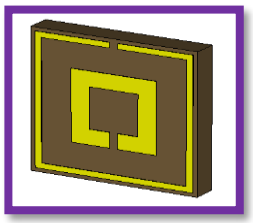
Experimental Verification of MSRR Reflection Coefficient

- The size of the MSRR is the same as the antenna with 21 mm spacing.
- Proposed wideband (WB) MSRR achieved 2x improvement in bandwidth.
- The narrowband (NB) and WB MSRRs exhibited a peak realized gain of 10 and 12 dBi, respectively.

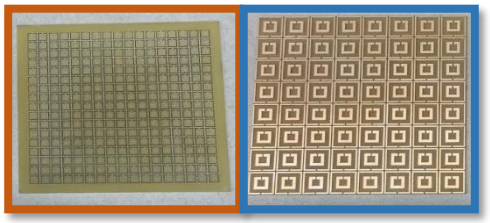




NB Unit Cell Simulation

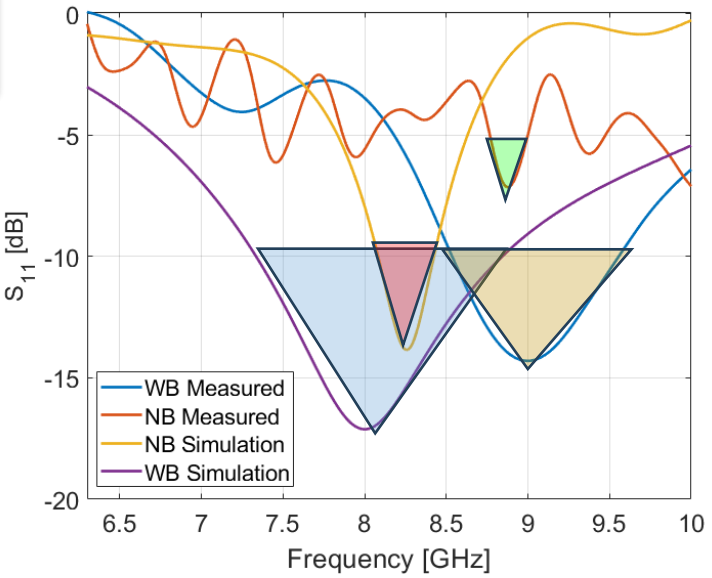


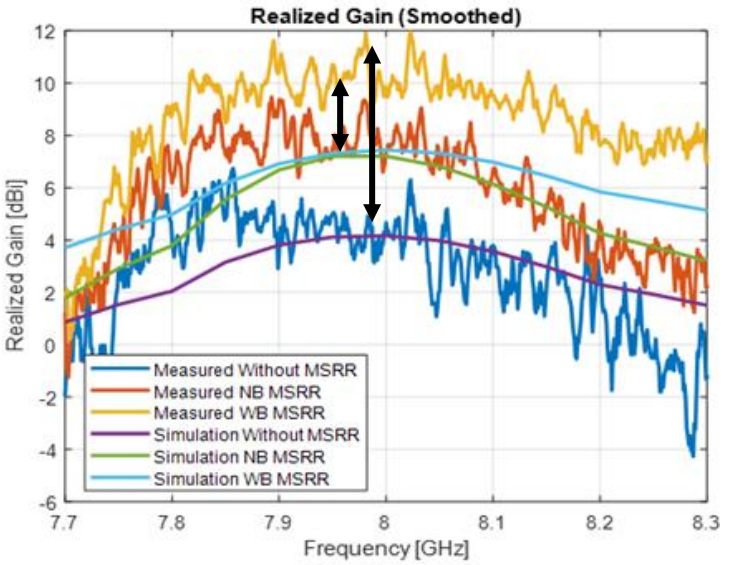
WB Unit Cell Simulation



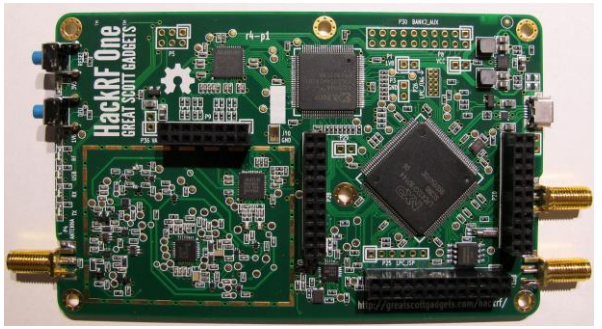
NB Measured

WB Measured

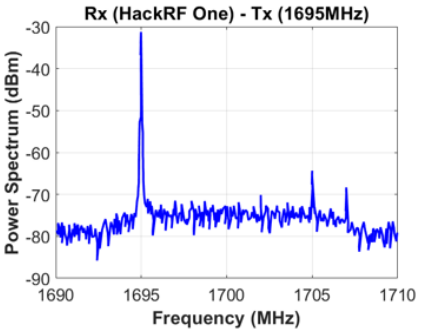


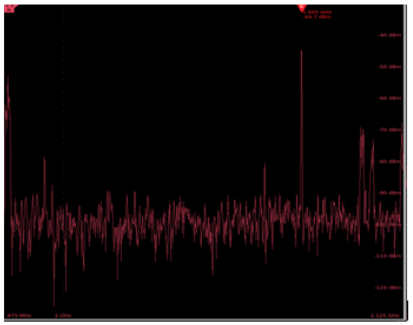


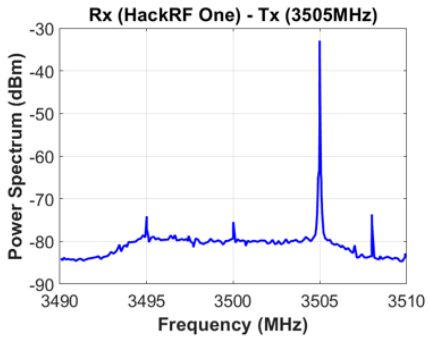
Machine Learning-based Fast Inference Beamforming

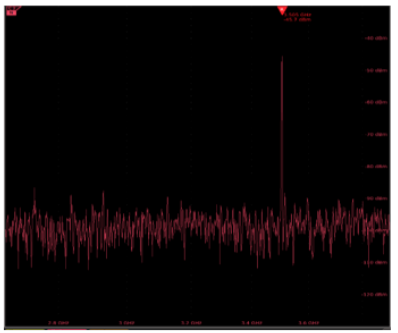


- A low-profile and low-cost software-defined radio (HackRF One) is utilized for signal reception, processing, digitization, and transmission.
- Wide frequency range (1 to 6000 MHz) with a sample rate of up to 20 million samples per second.
- The incoming signal is processed and digitized using HackRF One and GNU Companion, an open-source software toolkit.
- HackRF One operates in half-duplex mode.



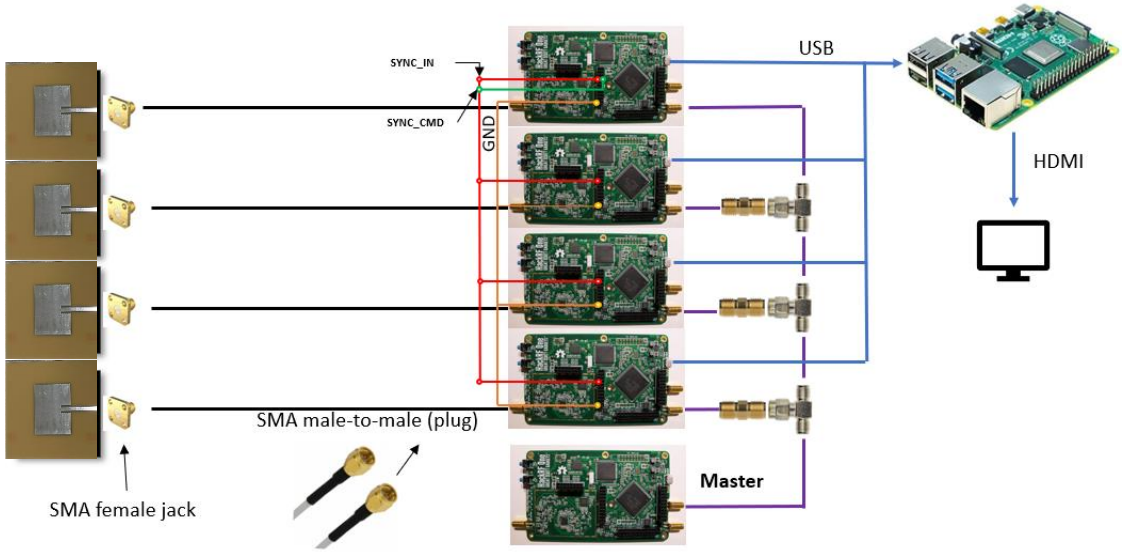






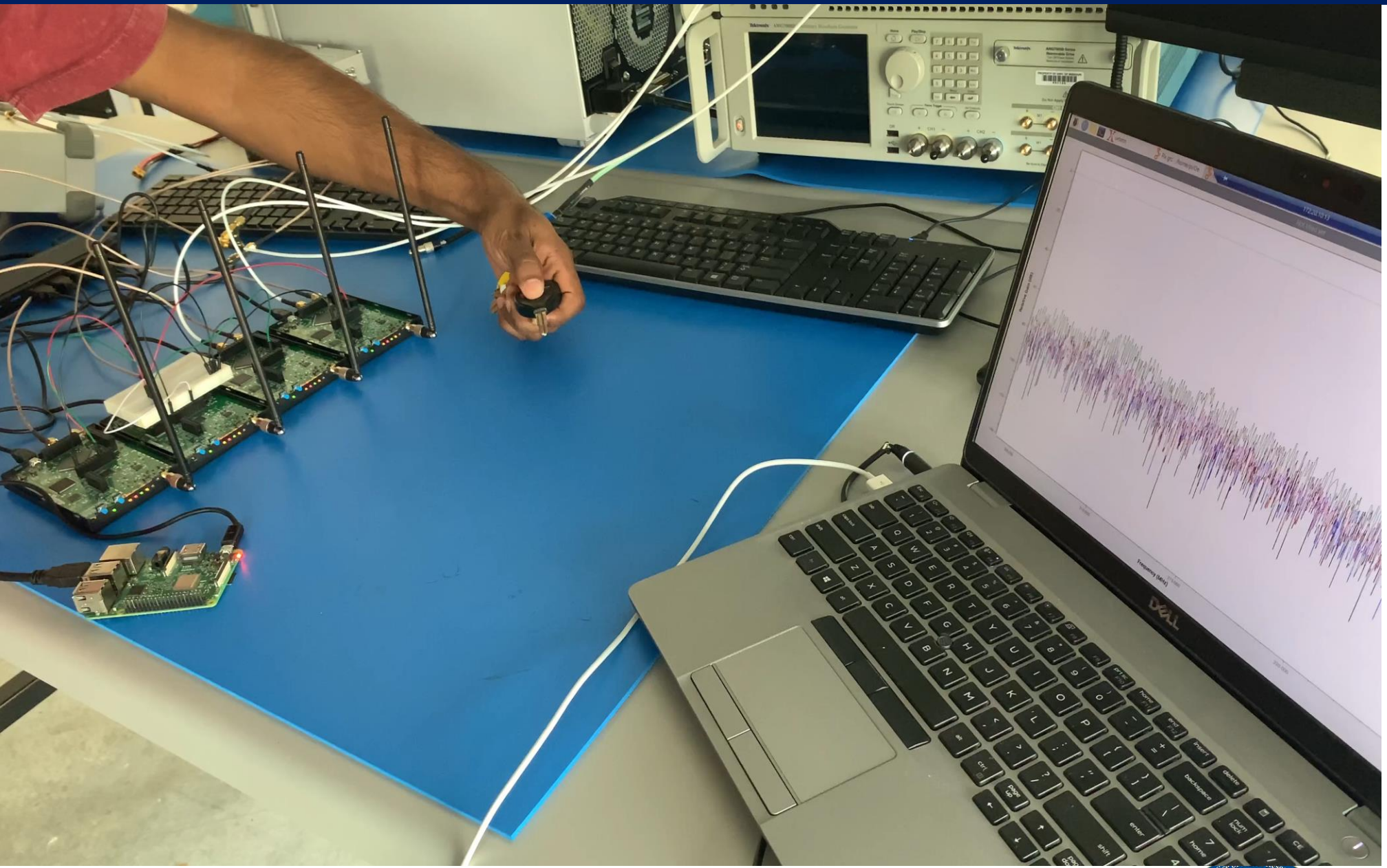
Frequency (MHz)	Power levels (dBm)	
	HackRF One	Oscilloscope
255	-20	-6.8
1695	-32	-44.7
3505	-36	-45.7

Machine Learning-based Fast Inference Beamforming



- The top left figure shows an illustration of the full array experimental setup
- The time and frequency synchronization between the SDRs is required to ensure that the incoming signals are received, processed, and transmitted simultaneously.

Machine Learning-based Fast Inference Beamforming



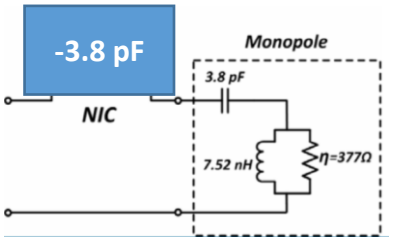
Reconfigurable Lens and Nonlinear Antenna

Technical Background and Approach

The proposed approach

Design a high gain , wideband, and beam steerable single antenna element

Introduce frequency reconfigurability using external circuit (Non-Foster circuit)



- The design supports closely spaced modes result in broadband performance.
- The Design is suitable for wideband applications
- The design will have a gain ≥ 10 dB.
- The design will be modified to handle high power

- A Non-Foster Circuit (NFC) provides negative capacitance.

W. Liu, Z. N. Chen and X. Qing, "Metamaterial-Based Low-Profile Broadband Aperture-Coupled Grid-Slotted Patch Antenna," in IEEE Transactions on Antennas and Propagation, vol. 63, no. 7, pp. 3325-3329, July 2015, doi: 10.1109/TAP.2015.2429741.

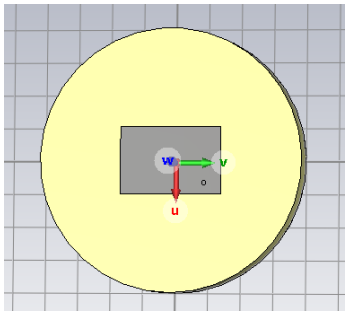
G. Linvill, "Transistor Negative-Impedance Converters," in Proceedings of the IRE, vol. 41, no. 6, pp. 725-729, June 1953, doi: 10.1109/JRPROC.1953.274251.

Frequency Reconfigurability Using NFC – Design, Simulations

Motivation : upgrade the NFC concept to GHz band

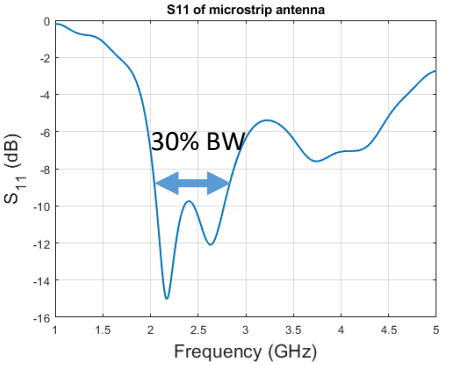
Procedure

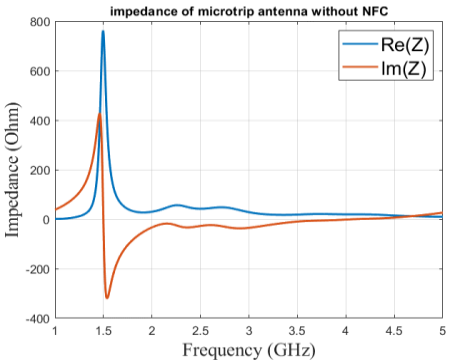
- Design the antenna
- Measure the input impedance of the antenna at the required new resonance
- Design a Non-Foster Circuit that provides a negative impedance at the new resonance
- Integrate the two designs to generate electrically small antenna



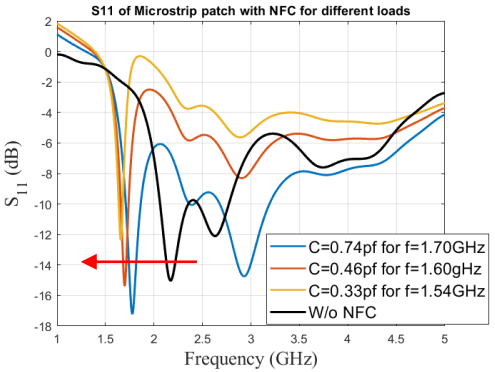
Design parameters:

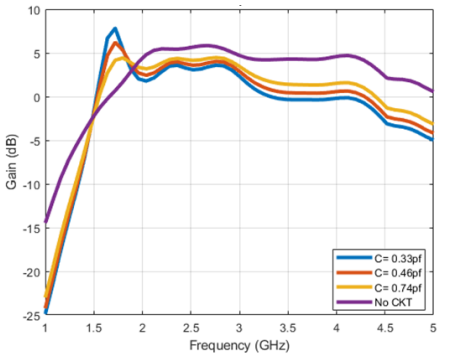
- Fr4
- h=10 mm
- L=20.47 mm
- W=30.7 mm



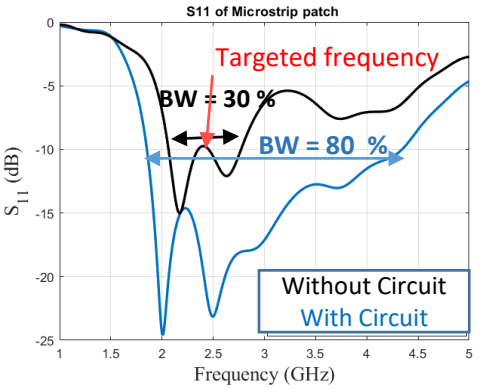


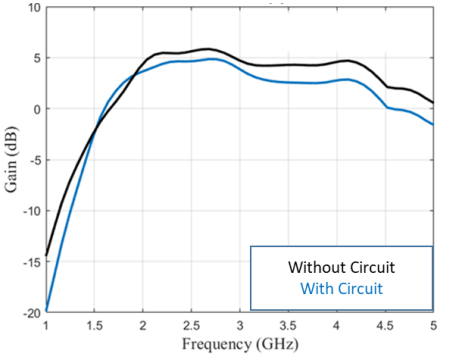
Frequency Reconfigurability



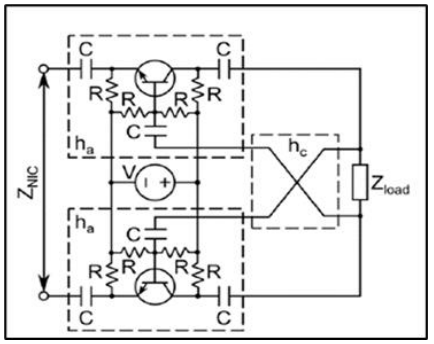


Bandwidth Reconfigurability

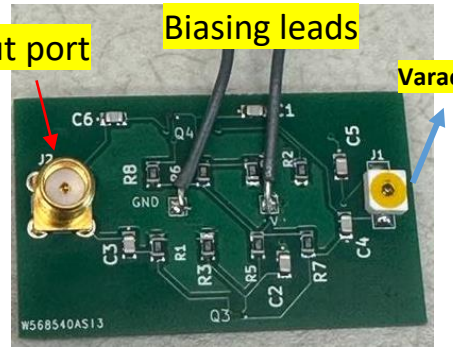


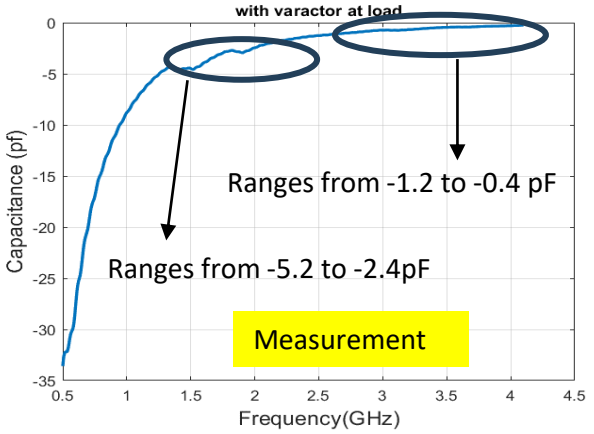


Frequency Reconfigurability Using NFC - Measurements

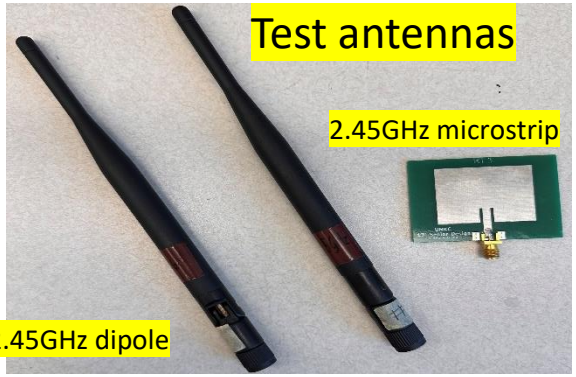


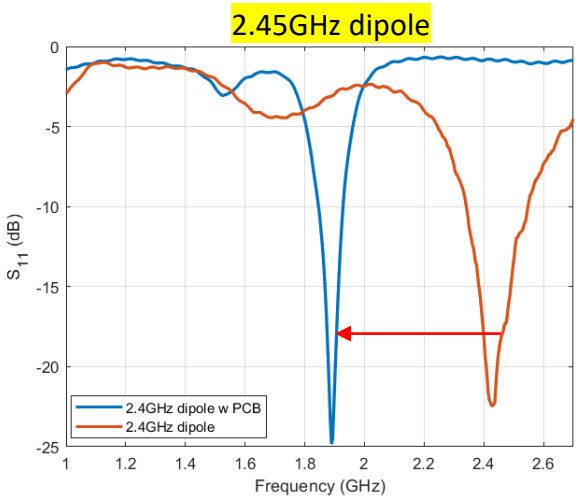
Component	Values
R	750 Ω
C	1.1 nF
V_{bias}	9 V
Transistor	BFR843EL3
Frequency of operation	0.5 – 4 GHz



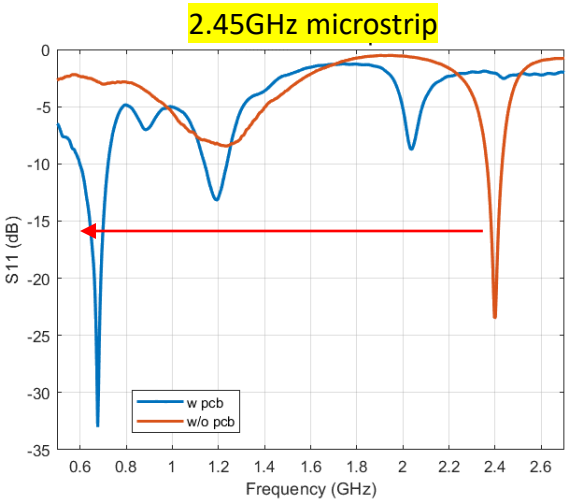


- The circuit provides -0.4 to -5.2 pf.





25 % reconfigurability

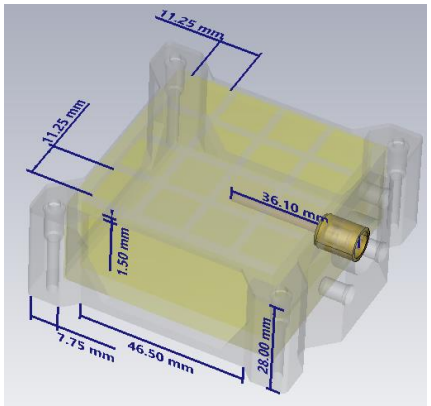


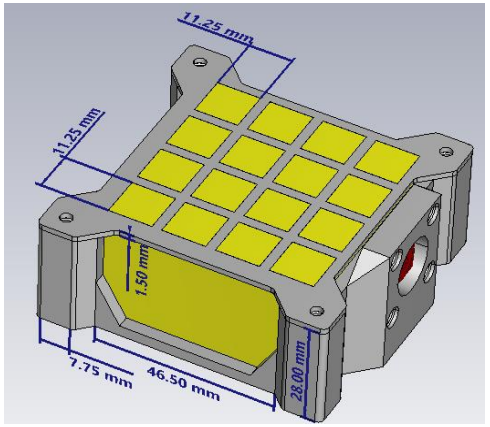
120 % frequency reconfigurability.

High Power Antenna Design

Design

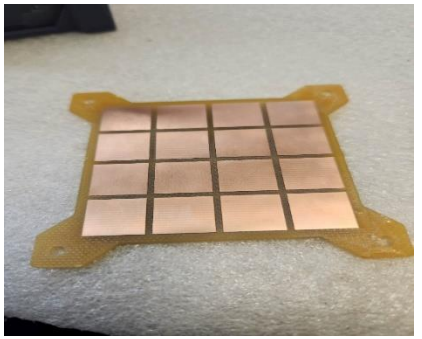
- The cavity of the new design is fed by an N-type connector Hence, it's power handling capability is limited by the power handling capability of its N-type connector.
- The maximum dimension is 0.48 λ at 2.5 GHz.
- The upper metasurface layer consists of 4×4 patches designed above a 1.6 mm Rogers 3003 substrate with ε_r=3 and FR-4 substrate with ε_r=4.4



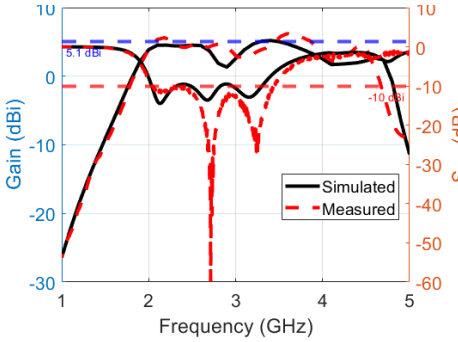


Fabrication and Experimental Measurements

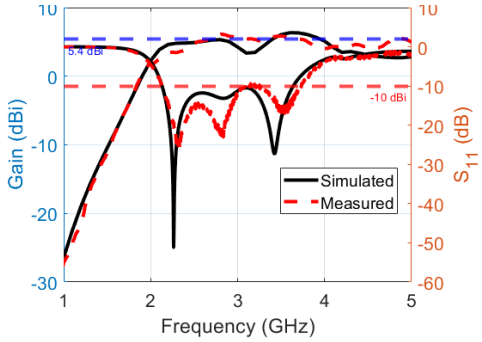
- The cavity was 3D printed and covered internally by a thin sheet of copper.



FR-4



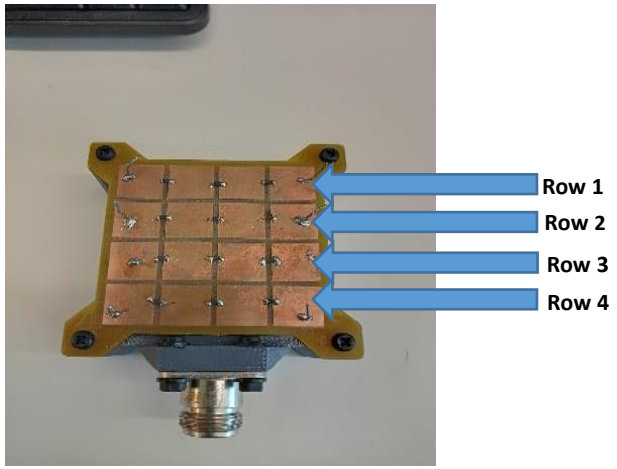
Rogers



	FR-4	Rogers
BW (%)	52	55
Gain (dBi)	5.1	5.4

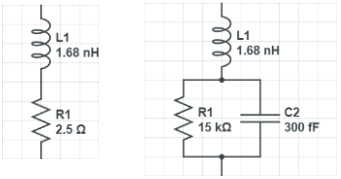
Antenna Reconfigurability

Diodes were added to connect all the patches

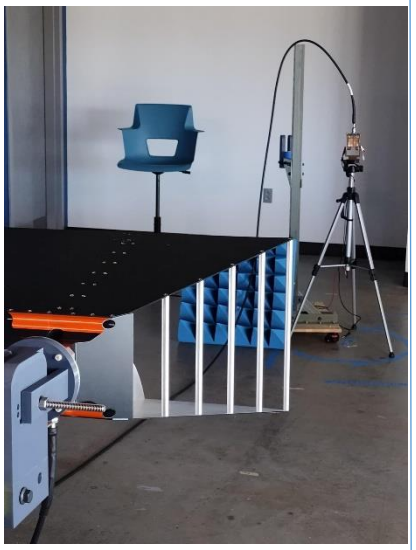


When Row 1 is biased

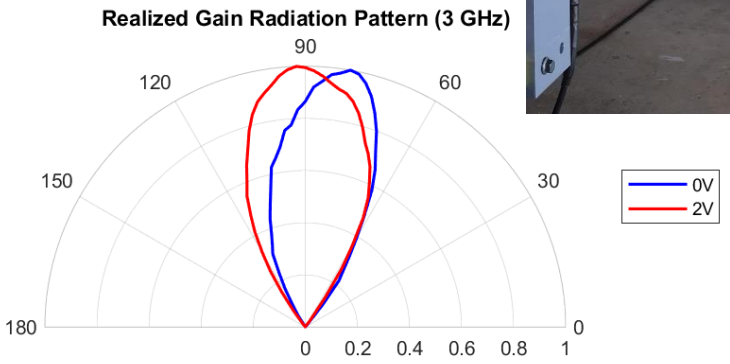
NXP BAP64-03 DIODE



On State ***Off State***



Beam Steerability (Measurements)

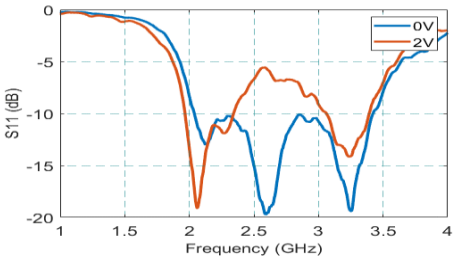


- ~ 15° beam steerability. Simulations show 33°

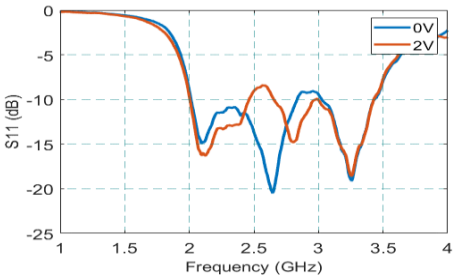
Frequency Reconfigurability (Experimental Measurements)

- Maximum bandwidth decreased by 40% and maximum bandwidth increased by 24%.
- Maximum frequency blue shift is 15% and 20% red shift .

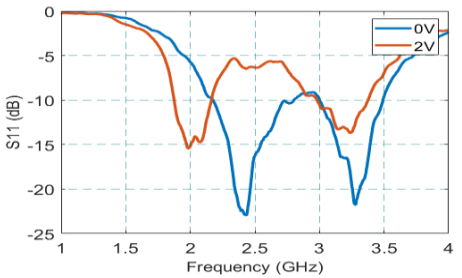
When Row 2 is biased



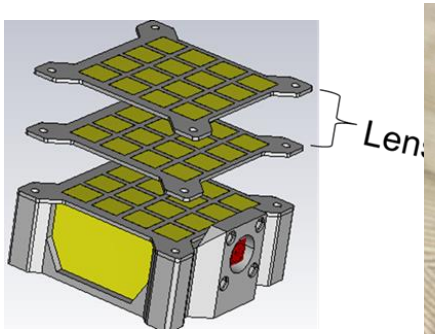
When Row 3 is biased

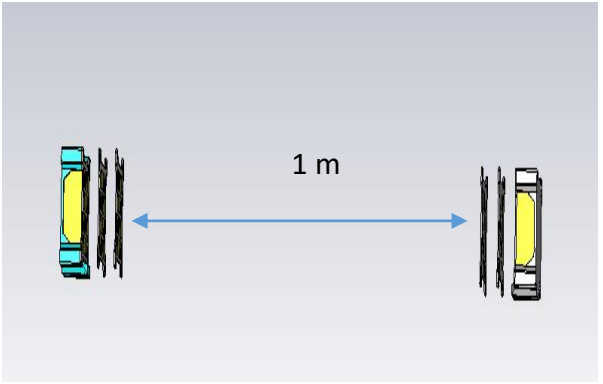


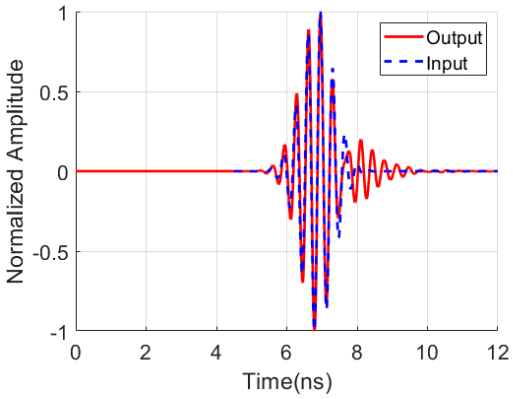
When Row 2&3 is biased

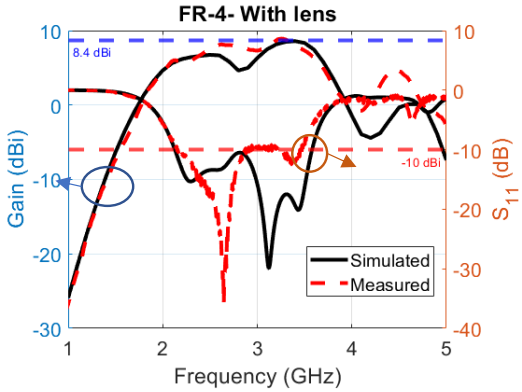


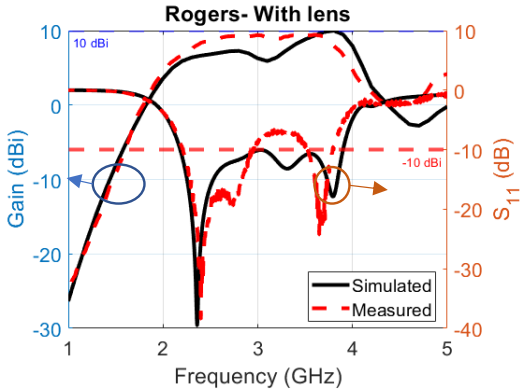
Gain and Bandwidth Improvement - Measurements











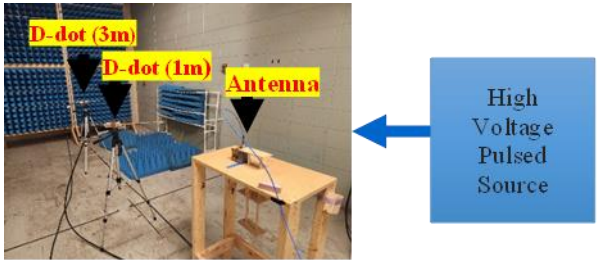
Rogers	Bandwidth(%)	Gain(dBi)
Without Lens	52	5.1
With lens	56	10

- The maximum dimension is ~ 0.5λ at 2.5 GHz.

- The fidelity factor indicates how good the antenna radiate without distorting the input signal.
- The FF is 0.970.

High power test

7 kV picosecond pulsed source



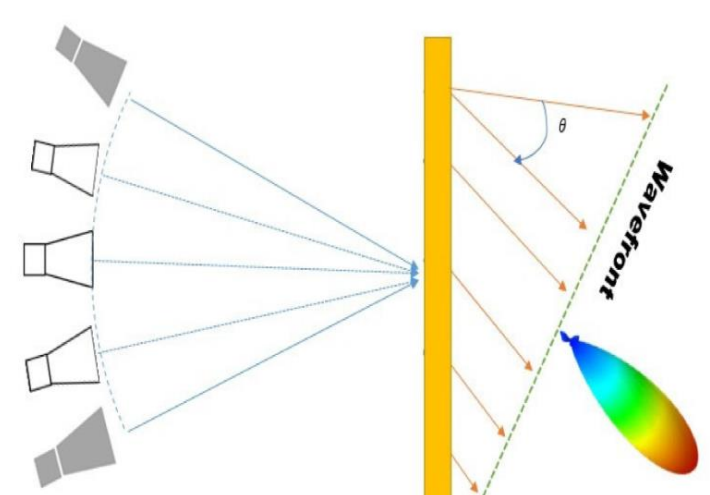
	Power density at 1 m (W/m²)	Power density at 3 m (W/m²)
FR4-With lens	1.1543e+05	2.1008e+04
Roger-With lens	1.2255e+05	2.3025e+04

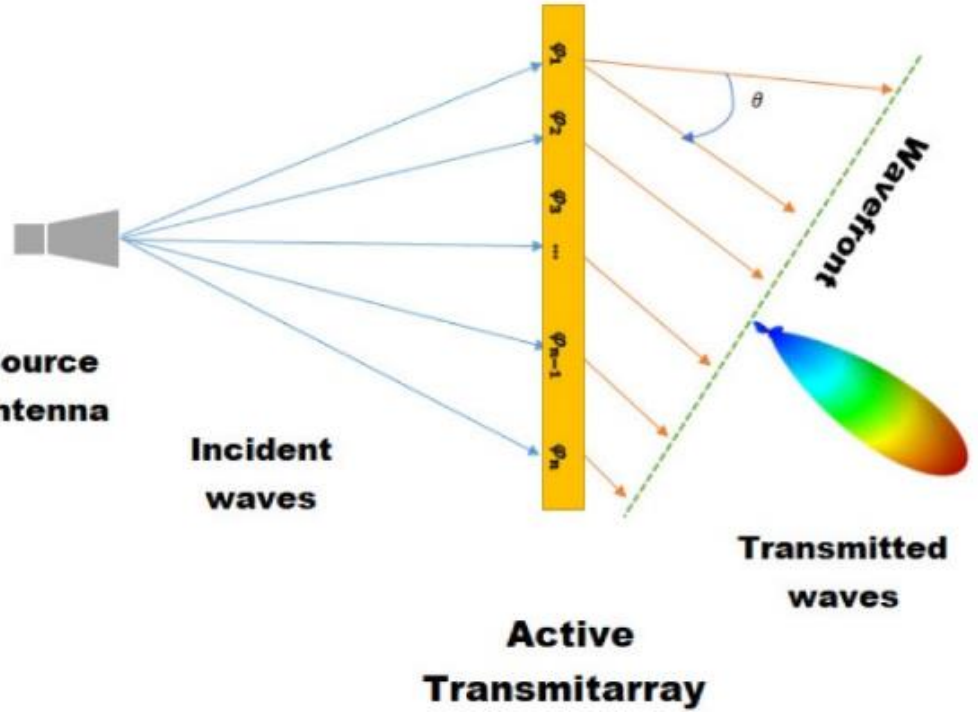
- No sparks nor breakdown

Metrics Comparison & Summary

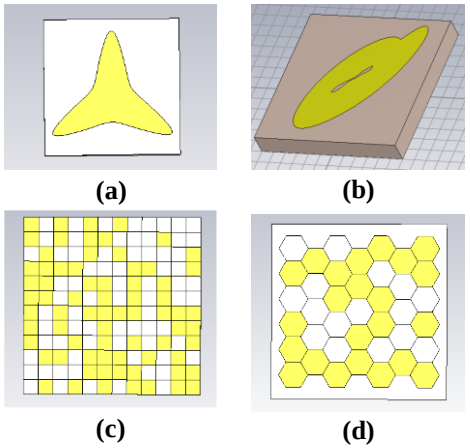
Metric name	Threshold	Objective	Ideal	Reconfigurable Superwideband & MSRR-loaded Antennae	Reconfigurable Lens and Nonlinear Antennae
Frequency Reconfigurability (%)	25	35	50	47 (Sim.), 31 (Meas.)	27% using diodes (Meas.) 120% using NFC (Meas.)
Bandwidth Reconfigurability (%)	20	50	150	137 (Sim.), 60% (Meas.)	24 (Meas.)
Operating Range [GHz]	L-band to S-band	L-band to C-band	L-band to Ku-band	L-band to Ku-band (Meas.)	S-band to C-band (Meas.)
Antenna Peak Gain (dBi)	3	5	7	6 (Meas.)	5 (Meas.)
Antenna + Metamaterial Peak Gain (dBi)	7	10	15	12 (Meas.)	10 (Meas.)
Beam Steering (°)	20	45	65	46 (Sim.)	33 (Sim.)
Form factor (mm^3)	150 x 150 x 50	100 x 100 x 45	50 x 50 x 25	80 x 80 x 21	60 x 60 x 25
Weight (lbs.)	<10	< 3	< 1	0.1	0.1
Power Handling (kW)	> 1	> 100	> 1000	Did not test	> 1000

Recommendations and Future Work

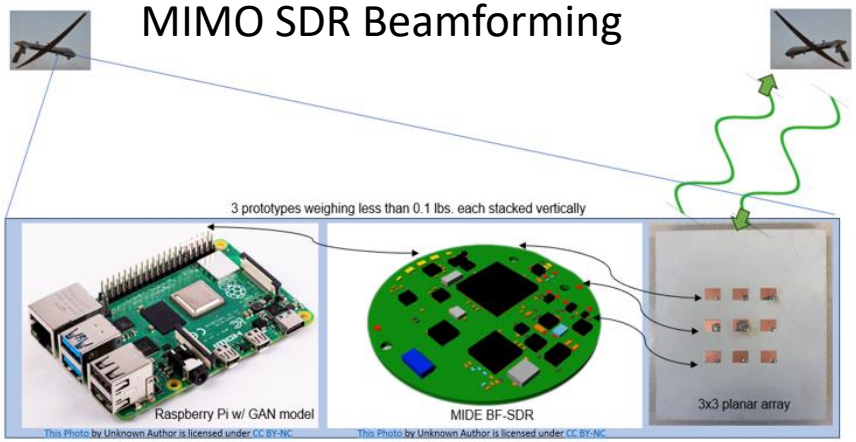




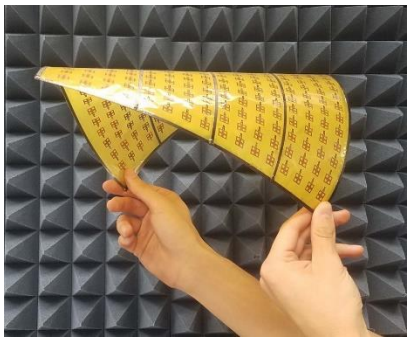
GA Inspired Metamaterial



MIMO SDR Beamforming



Flexible Antenna



Q. Ali *et al.*, "Recent Developments and Challenges on Beam Steering Characteristics of Reconfigurable Transmitarray Antennas," *Electronics*, vol. 11, no. 4, Art. no. 4, Jan. 2022, doi: 10.3390/electronics11040587
A. Fikes, O. S. Mizrahi and A. Hajimiri, "A Framework for Array Shape Reconstruction Through Mutual Coupling," in IEEE Transactions on Microwave Theory and Techniques, vol. 69, no. 10, pp. 4422-4436, Oct. 2021, doi: 10.1109/TMTT.2021.3097729..

Journal Publications

In Preparation

- Mohamed Z. M. Hamdalla, Mashrur Zawad, Somen Baidya, Roy Allen, Peter J. Bland, and Ahmed M. Hassan, “Design of a Low-Profile Wide Band Cavity Backed Metasurface Antenna for High Power Applications,” *IEEE Antennas and Wireless Propagation Letters*. [under preparation] .
- S. S. Indharapu, A. N. Caruso, K. C. Durbhakula, “Machine Learning Assisted Antenna Design Optimization of UWB Fractal Antenna,” *IEEE Access*, In Preparation.

Submitted / Under Revision

- A.-M. Al-Hinaai, A. N. Caruso, R. C. Allen, and K. C. Durbhakula, “Design of a Hollow Dielectric Lens for Wideband Gain Enhancement of a Horn Antenna,” *Progress in Electromagnetics Research*, Accepted, Sep. 2023.

Conference Publications/Presentations

- M. Z. M. Hamdalla, R. Allen, P. J. Bland and A. M. Hassan, "Cavity Backed Metasurface Antenna for High Power Applications," *2023 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (USNC-URSI)*, Portland, OR, USA, 2023, pp. 1085-1086.
- S. S. Indharapu, A. N. Caruso and K. C. Durbhakula, "Next Generation Antenna Design Synthesis Framework Using k-Nearest Neighbors Algorithm," *2023 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (USNC-URSI)*, Portland, OR, USA, 2023, pp. 611-612.
- S. S. Indharapu, A. N. Caruso and K. C. Durbhakula, "Fast Inference Beamforming Prediction using Machine Learning," *2023 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (USNC-URSI)*, Portland, OR, USA, 2023, pp. 925-926.

Submitted / Under Revision

- Mashrur Zawad, M. Z. M. Hamdalla and A. M. Hassan, "Different Geometrical Representations of Partially Reflected Surfaces for Fabry-Perot Antenna Optimization,” *2024 National Radio Science Meeting*, Boulder, CO.

Theses

In preparation

- A.-M. Al-Hinaai, “Advancements in Antenna Gain Enhancement Techniques,” Master of Science in Physics, UMKC, Dec. 2023.

Sai Indharapu
Ph.D. Student

Gabriella Ramirez
B.S. Physics (Grad.)

Mashrur Zawad
Ph.D. Student

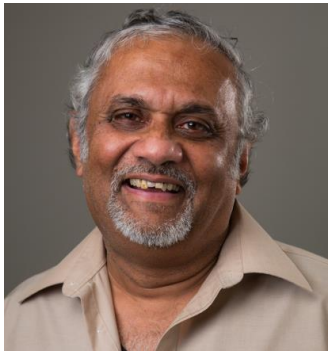
Al-Moatasem Al-Hinaai
M.S. Student

Niharika Kaja
M.S. Student

Kalyan Durbhakula
Assistant Research Professor

Mohamed Hamdalla
Assistant Research Professor

Ahmed Hassan
Associate Professor



Deb Chatterjee
Associate Professor

THANK YOU!!!

Questions?

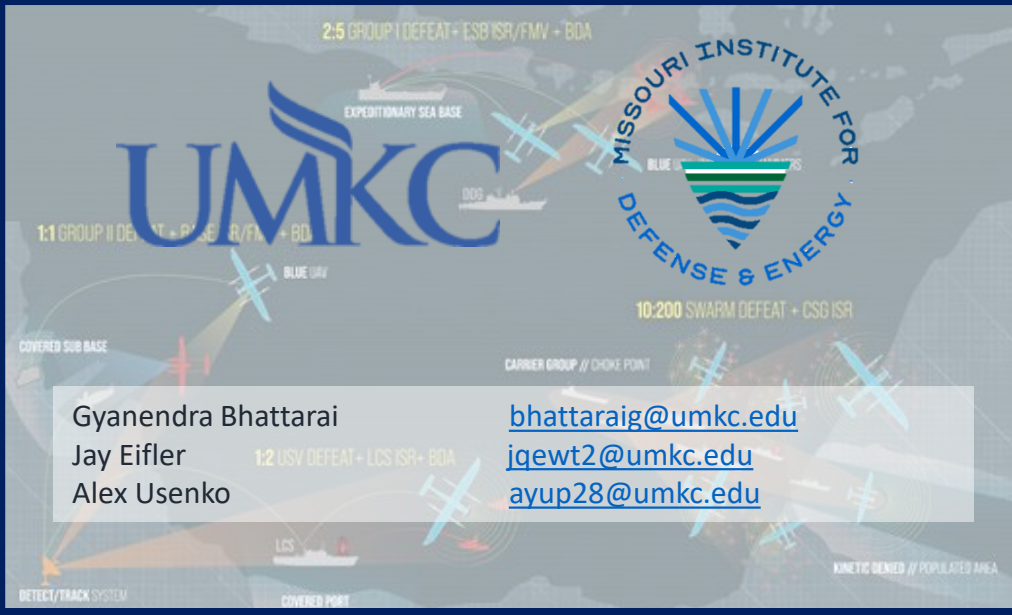
Pulse Tactical Effector for Regulated Attack

Innovations in Design and Fabrication of DSRD/SAS Sources

PTERA Grant Annual Review

October 10, 2023

Funding provided by ONR under grant N00014-22-1-2385



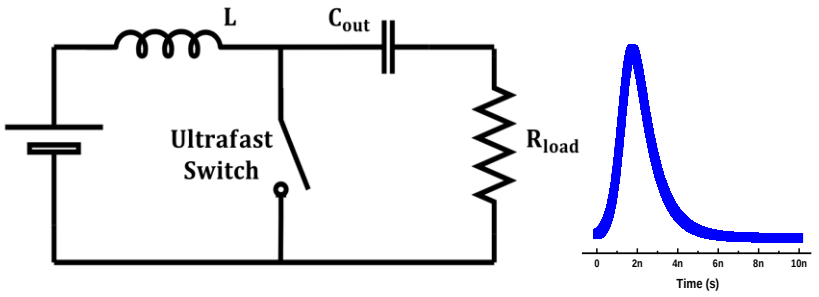
Gyanendra Bhattarai bhattaraig@umkc.edu
Jay Eifler jqewt2@umkc.edu
Alex Usenko ayup28@umkc.edu

Motivation

Ultra short pulse Source

- All-Solid-State
- Nano/Sub-Nanosecond
- Ultra Portable
- High-Voltage
- Non-Optical

High-Power Electronic Effectors on UAV



Yes! Inductive Energy Storage and Release

Old: Exploding wires

New: Semiconductor

Theory and Optimization

- Many circuit topologies exist but not optimized
- No standard circuit working principle/theory
- Very crude optimization scheme (energy, efficiency, PRF)

Switch Fabrication

- No COTS fast semiconductor opening switches (SOS) and silicon avalanche sharpener (SAS) available in the US.
- Available diodes are made with old (60 years) technology.

Objective

Pulser Metrics

- **Peak voltage ≥50 kV**
- **Risetime ≤ 1 ns**
- **PRF ≥ 100 kHz PRF**
- **Volume ≤ 1 liter**

- 16.4 kV
- 3 ns
- **100 kHz**
- 2 liter

Achieved

DSRD Pulser Circuit

- **Develop pulser circuit theory to increase diode current**
- **Minimize prime source voltage**
- **Minimize switch voltage/Stack multiple switches**

Increase diode current to >2 kA

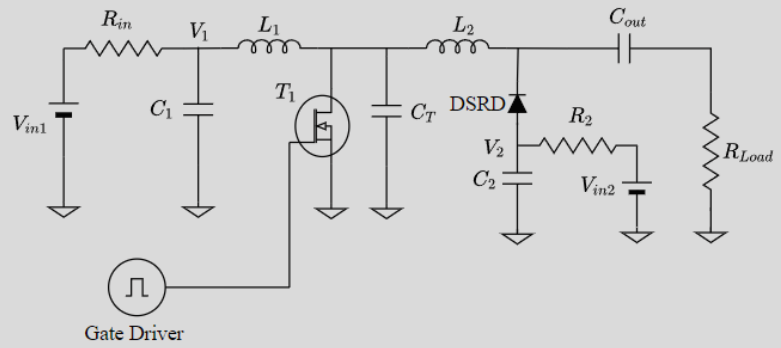
DSRD/SAS Modeling

- **Optimize DSRD geometry and doping profile to decrease switching time**
- **Develop DSRD models for SPICE/TCAD simulations**
- **Optimize SAS geometry and doping profile**
- **Match pulser simulation with experiments**

DSRD/SAS Fabrication

- **Develop DSRD and SAS process Flow**
- **Manufacture stacked DSRD (60 –70 dies) to enable >50 kV pulser**
- **Manufacture matched SAS pairs to DSRD**

Pulser Circuit Theory and Optimization

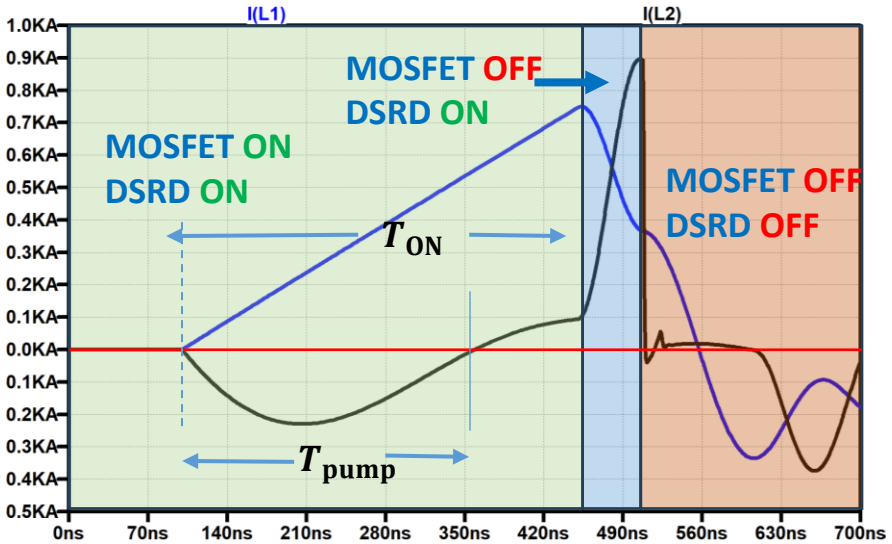


DSRD-based pulser circuit

Last Year

- Developed a simple theory
- Optimization based on forward injected charge
- Role of C_T was not clear

$$\mathbf{I_{L2}(peak) \leq I_{L1}\ (peak)}$$

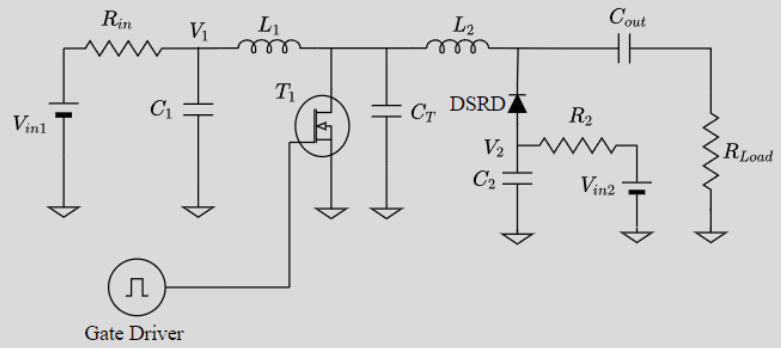


This year

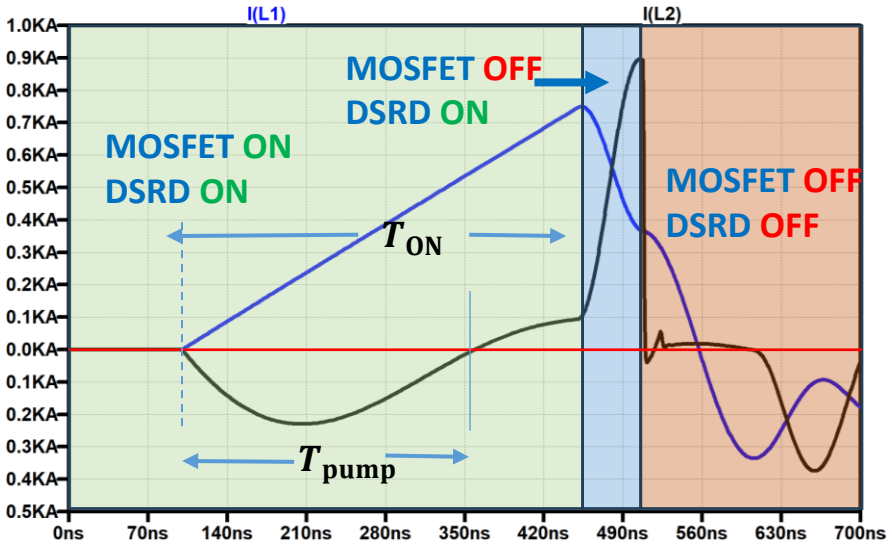
- Optimization based on energy required
- Role of C_T Explained
- $I_{L2} > I_{L1}$ possible
- Role of C_1, V_{in1}, and R_{in} for PRF explained
- Measured and verified I_{L2}

Allowed systematic optimization of circuit elements → Predict what you get!!

Circuit Optimization: Input Energy



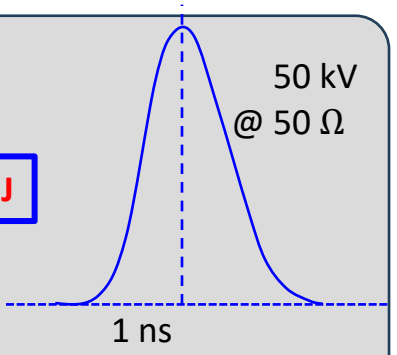
DSRD-based pulser circuit



Output Energy

$$E_{out} = \frac{V_{Load}^2}{R_{load}} t_{rise}$$

=50 mJ



Input Energy

$$E_{in} = \frac{1}{2} \frac{V_{in1}^2 T_{ON}^2}{L_1}$$

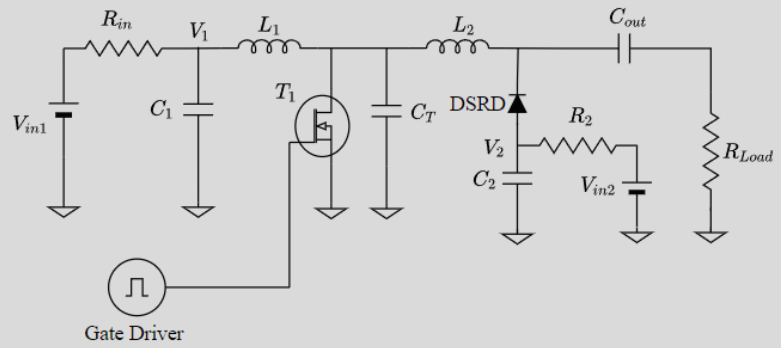
Fixes V_{in1}, T_{ON}, and L_1

Peak L_1 Current

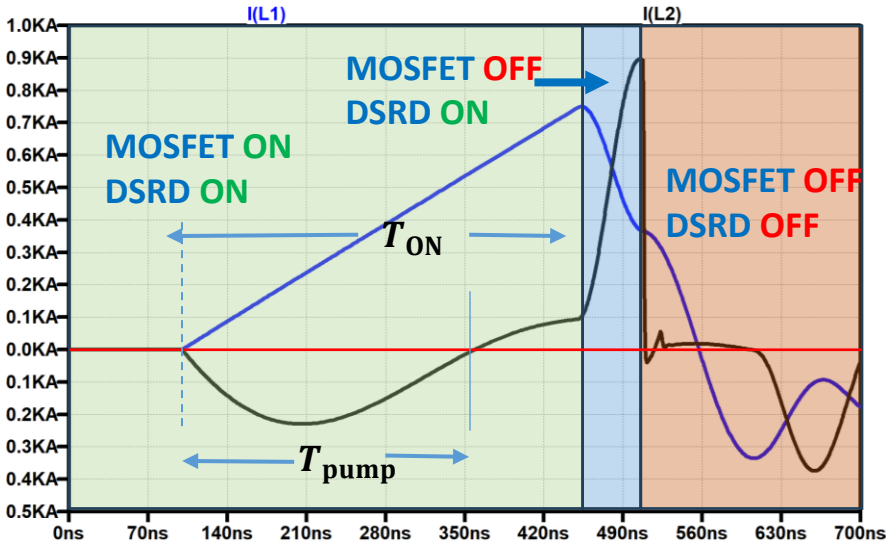
$$I_0 = \frac{V_{in1}}{L_1} T_{ON}$$

Add more MOSFETs in Parallel to increase current

Circuit Optimization: Diode Reverse Current



DSRD-based pulser circuit



L_2 Energy

$$E_{L2} = \frac{1}{2} L_2 I_{L2}^2 \leq E_{in}$$

$I_{L2} > I_{L1}$

Only if $L_2 < L_1$

Role of C_T

- Intermediate energy transfer
- Determines reverse pump time

$$\omega \approx \frac{1}{\sqrt{L_2 C_{2T}}} \sqrt{1 - \frac{R_d^2 C_{2T}}{4 L_2}}$$

- Determines MOSFET voltage

$$V_{MOSFET} \approx I_0 \sqrt{\frac{L_2}{C_T}}$$

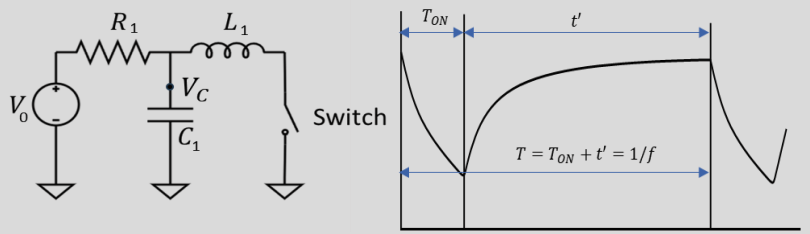
Stack MOSFETs in series

Role of C_2

- Determines diode forward pumping time
- Determines DSRD snap-OFF time

Optimize C_2

Circuit Optimization: Pulse Repetition Frequency



C_1 discharging and recharging

$$\frac{V_{Cn}}{V_0} = |q|^n + p\sum_{0}^{n-1}|q|^n$$

$$p = 1 - a + abc$$
$$q = abd$$

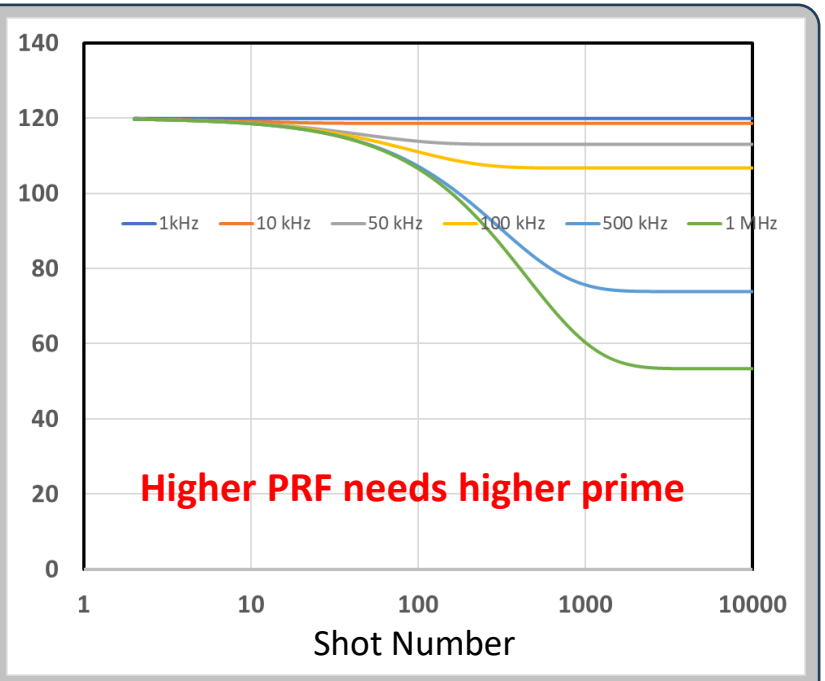
$$a = \exp\left(\frac{T_{ON} - T}{\tau}\right)$$

$$b = \frac{\tau_0}{2\tau}\exp\left(-\frac{T_{ON}}{2\tau}\right)$$

$$c = 2\sin\frac{T_{ON}}{\tau_0}$$

$$d = \left(\sin\frac{T_{ON}}{\tau_0} - \frac{2\tau}{\tau_0}\cos\frac{T_{ON}}{\tau_0}\right)$$

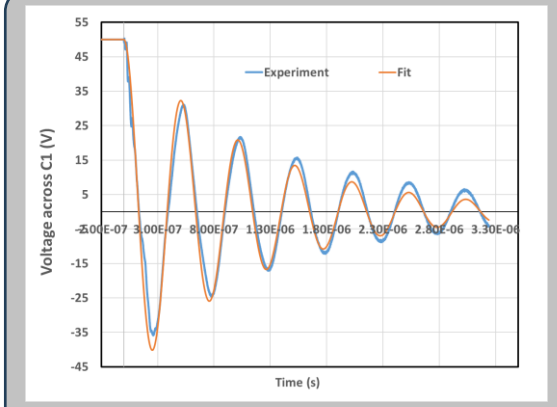
$\frac{1}{T} = PRF$,
$\tau = R_1C_1$, and
$\tau_0 = \sqrt{L_1C_1}$



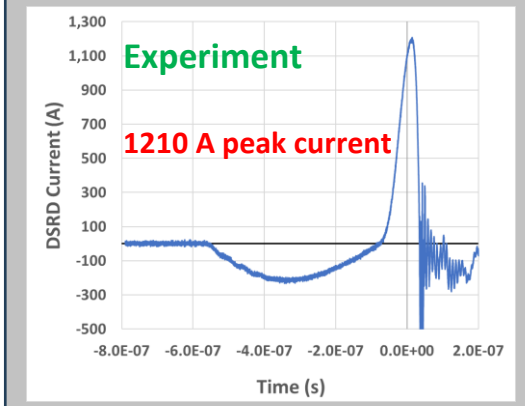
Example for a 30 kV Pulser

$$\boldsymbol{V_{in1} = 120\ V,}$$
$$\boldsymbol{L_1 = 100\ nH,}$$
$$\boldsymbol{C_1 = 1\ mF,}$$
$$\boldsymbol{T_{ON} = 500\ ns,}$$
$$\boldsymbol{R_1 = 1\ \Omega.}$$

Circuit Optimization: Verifications

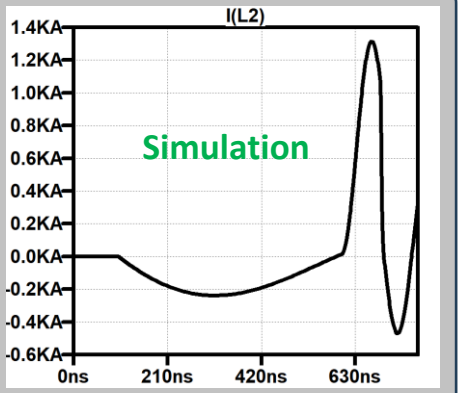


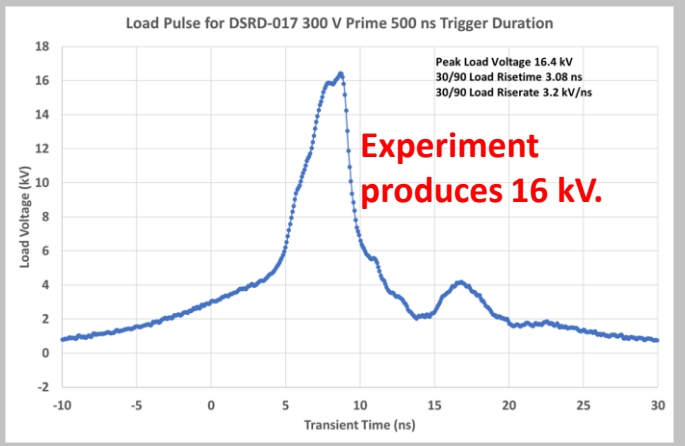
$C_1 = 124\ nF$
$L_1 = 52\ nH$
$R_M = 0.9\ \Omega$



$L_1 = 52\ \text{nH}$
$L_2 = 138\ \text{nH}$
$T_{ON} = 500\ \text{ns}$
$V_{in1} = 300\ \text{V}$

Peak Diode Current = 1314 A

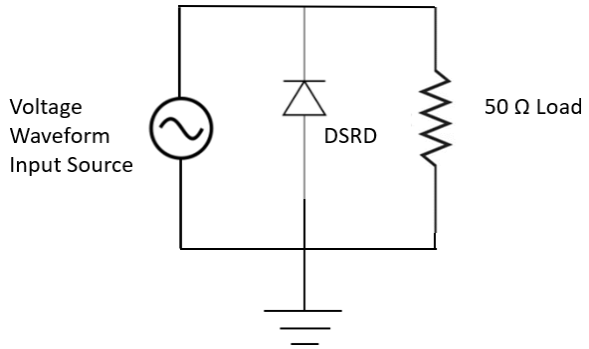




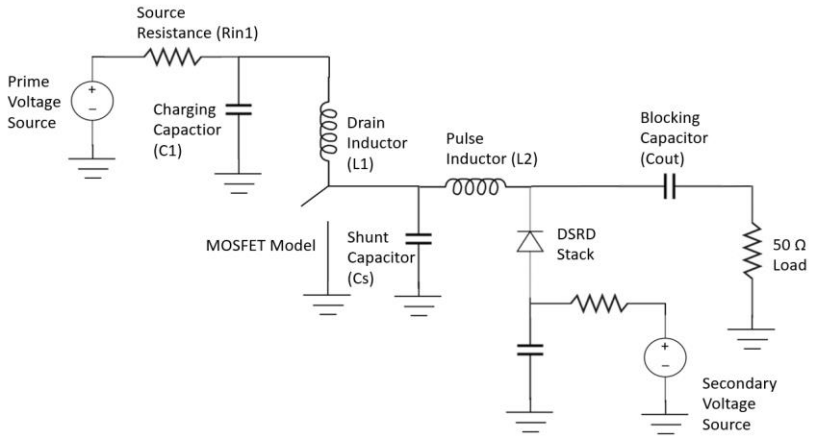
- **CIRCUIT works as expected.**
- **LT-Spice simulation predicts ~ 44 kV**

- **Diode does not snap as fast as we expect**
- **LT-Spice DSRD model is not accurate**

DSRD: TCAD Modeling and Simulation



Simple DSRD Circuit



Realistic DSRD Pulser Circuit

DSRD simulated in both realistic pulser circuit and simple circuit

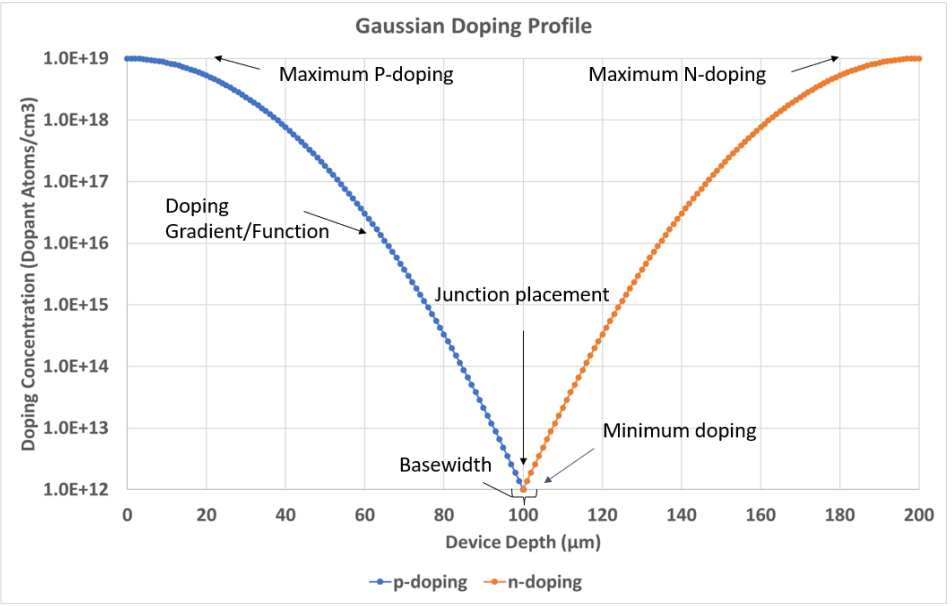
- Circuit component optimization performed originally in LTspice, so original DSRD models were LTspice models
- SmartSpice CMC Verilog-A diode model also used for developing DSRD model for pulser simulation
- TCAD has capability to design doping profile, originally used for DSRD doping profile design and modeling
- TCAD has performed best for fitting simulation and experiment

DSRD: TCAD Modeling and Simulation

DSRD Doping Profile Design

- TCAD only simulation method available to optimize doping profile
- (At right) is shown a prototypical Gaussian doping profile (other functions can be used)
- With Epi-style DSRD any doping profile can be made within the epi-manufacturers limits (total range of doping difference, doping depth)
- DSRD thickness is also a doping profile parameter

SPT DSRD 1-stack

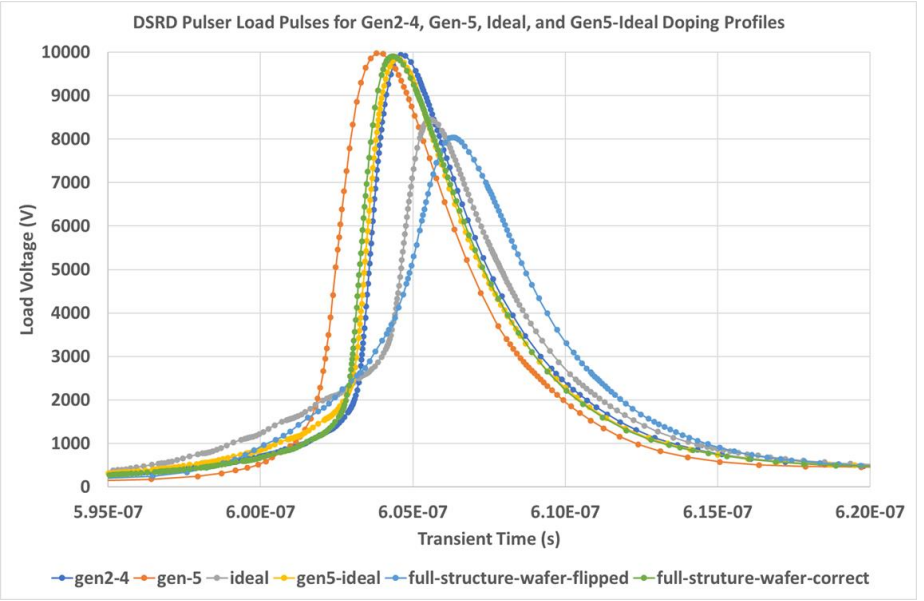


Gaussian Doping Profile with Doping Parameters Labeled

- Doping parameters: maximum doping, minimum doping, basewidth, junction placement, doping gradient/function, and junction placement are doping parameters (shown above)
- Our doping profile has followed the DSRD profiles developed from diffusion (gaussian, error function type doping gradients)
- Larger number of doping profiles to be studied in context of realistic DSRD pulser simulations for best performing DSRD doping profiles

DSRD Doping Profile TCAD Performance Evaluation

- Spreading resistance profiles have been taken of SPT Epi-DSRD and simulated within TCAD for DSRD performance
- Doping profiles not shown
- Differences in the slope of the doping profile likely cause differences in the DSRD performance
- (At right) are shown TCAD simulated load output pulses
- Table (below) shows collected data for load pulses and doping profiles
- Calculating the depletion width using TCAD can determine if depletion width extends too far to the right of the junction then performance drops (based on doping gradient)

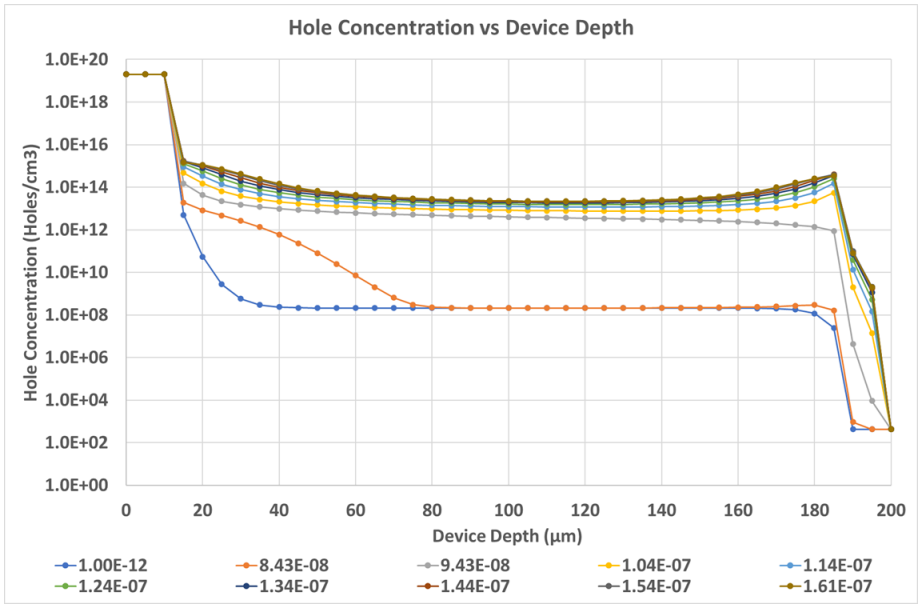


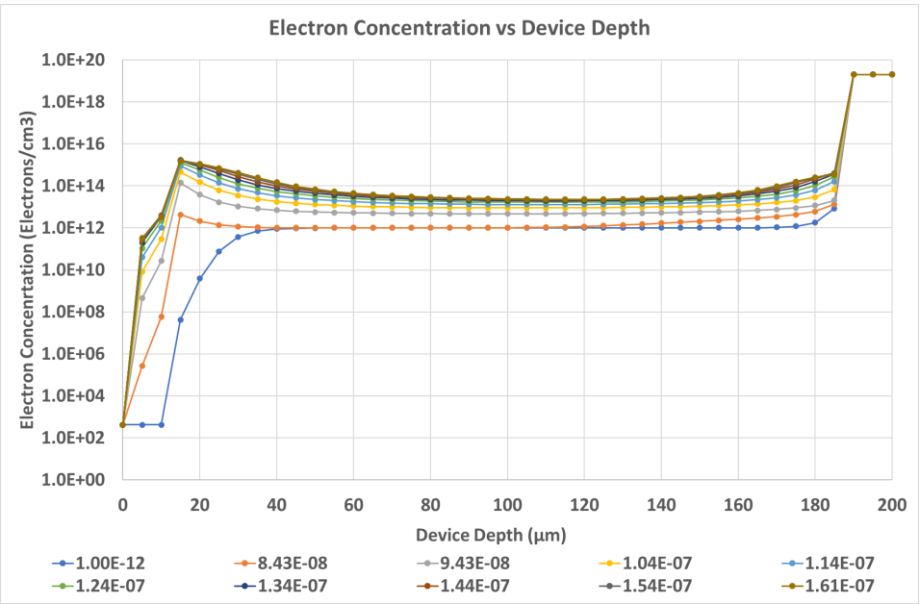
DSRD Load Pulses for Various Doping Profiles

Doping Profile	Peak Load Voltage (V)	30/90 Load Risetime (ns)	30/90 Load Riserate (V/s)	Thickness (µm)	Depletion Width (µm)	Peak Load voltage/Thickness (V/um)	Riserate/Thickness (V/(s*um))	Peak Load Voltage/Depletion Width (V/um)	Riserate/Depletion Width (V/(s*um))	Junction Placement (µm)	Junction Placement/Thickness
Gen2-4	9940	0.79	7.57E+12	235	75	42.29787234	3.22E+10	132.5333333	1.01E+11	116	0.493617021
Gen-5	9974	1.06	5.62E+12	220	55	45.33636364	2.55E+10	181.3454545	1.02E+11	106	0.481818182
Ideal	8451	1.79	2.84E+12	205	90	41.22439024	1.39E+10	93.9	3.16E+10	109	0.531707317
Gen5-Ideal	9848	0.81	7.32E+12	220	75	44.76363636	3.33E+10	131.3066667	9.76E+10	106	0.481818182
Full-structure-wafer-flipped	8040	2.75	1.75E+12	225	70	35.73333333	7.78E+09	114.8571429	2.50E+10	107	0.475555556
Full-structure-wafer-correct	9900	0.79	7.48E+12	225	70	44	3.32E+10	141.4285714	1.06857E+11	115	0.511111111

DSRD Non-Equilibrium Carrier Distribution

- Using simple DSRD TCAD simulations for carrier concentration (hole and electron concentrations at bottom)
- Idea was to confirm the non-equilibrium carrier distribution of the DSRD due to the manner of the forward pump
- Hole concentration is higher at the P+-p- junction (~20 um depth) than in the middle of device, also see some increased hole concentration at the n-N+ junction (~180 um depth)
- Further studies comparing the degree of steepness of the non-equilibrium carrier concentration as part of pumping studies can determine if it is possible to speed the DSRD snapoff (usually from manipulating the junction injection efficiencies)

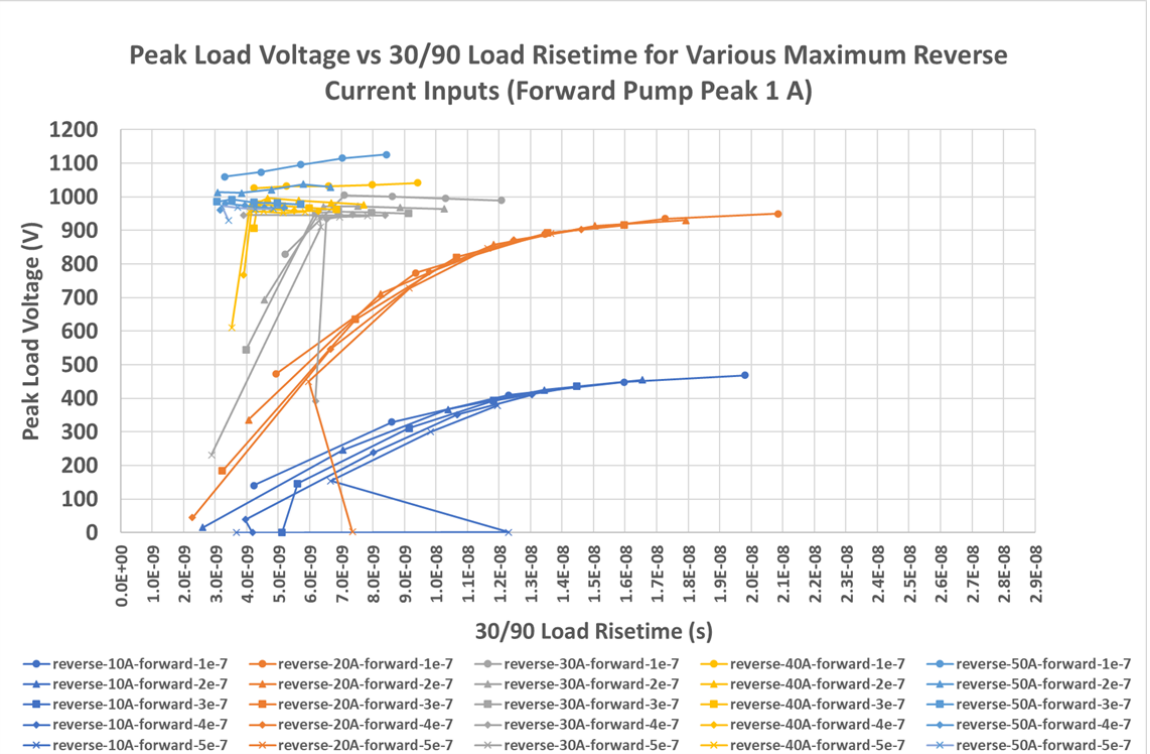




DSRD Carrier Distribution Profiles

DSRD Pumping and Performance from TCAD

- With simple DSRD TCAD simulations have studied the pumping
- Pumping consists of the forward-biasing and reverse-biasing of the DSRD within the DSRD pulser circuits
- (At right) is shown a detailed graphing of the DSRD peak load voltage/risetime performance with symbols denoting duration of forward pump and colors denoting magnitude of reverse
- Increased magnitude of reverse pump current produces increased peak load voltage up to the point of breakdown (flattening of the graphed lines above 930 V)
- We can see that different forward pump times do not separate in performance until we are at lower reverse pumping times (not shown)



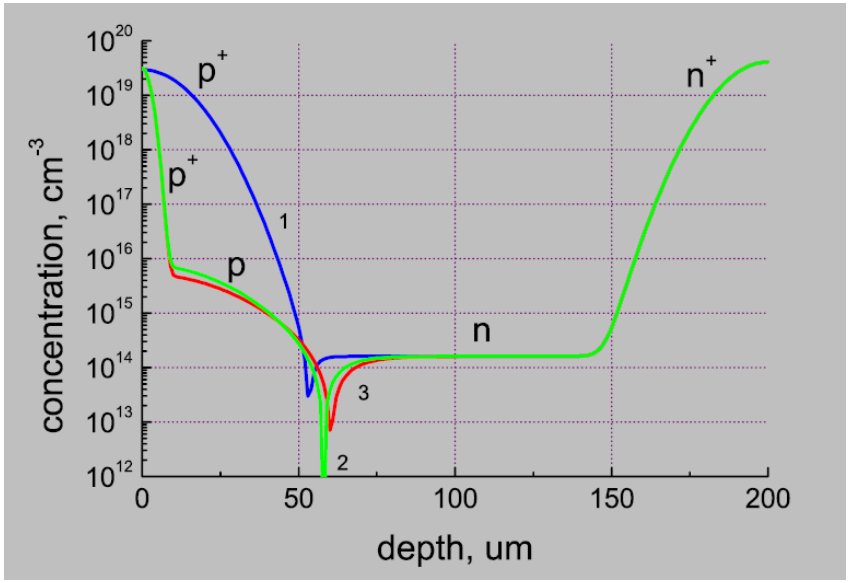
DSRD Pumping Performance Analysis

- Datapoints between 800 V – 930 V with low as risetime as possible are the best performers
- Note by altering reverse pump time can move datapoints out of breakdown into best performing region
- Larger set of forward and reverse pumps under study

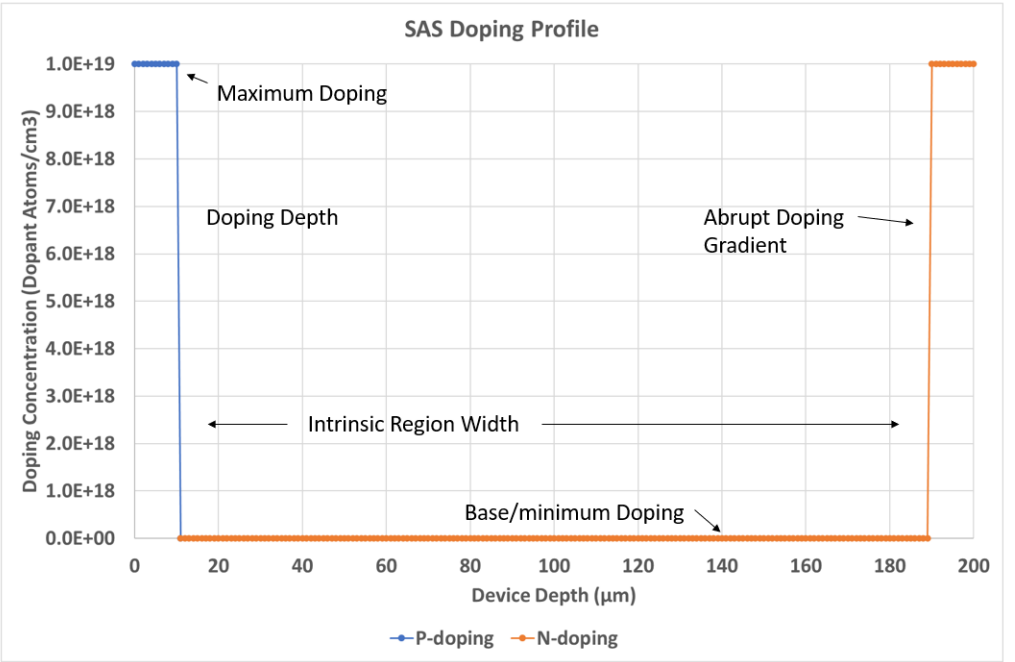
SAS: TCAD Modeling and Simulation

SAS Doping Profile and Simulation Method

- Not possible to model/simulate SAS in SPICE without major development effort
- TCAD is best choice for SAS modeling/simulation even if no accurate/quantitative SAS model exists
- Use both simple circuit and realistic pulser circuit to simulate SAS within
- SAS can include reverse-bias to SAS (have not used peaking capacitor)



Traditional SAS Doping Profiles*



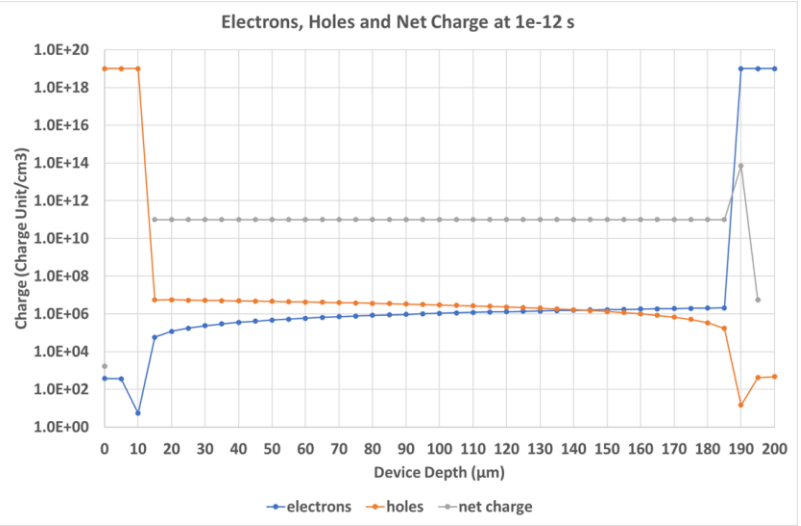
SAS Simulation Doping Profile

- SAS profile used in TCAD studies
- Used epi-style SAS doping profile
- Doping depth of 10 µm at contacts for P+ and N+ doping
- Wide, low-doped n- intrinsic region
- Defects not shown (when included)

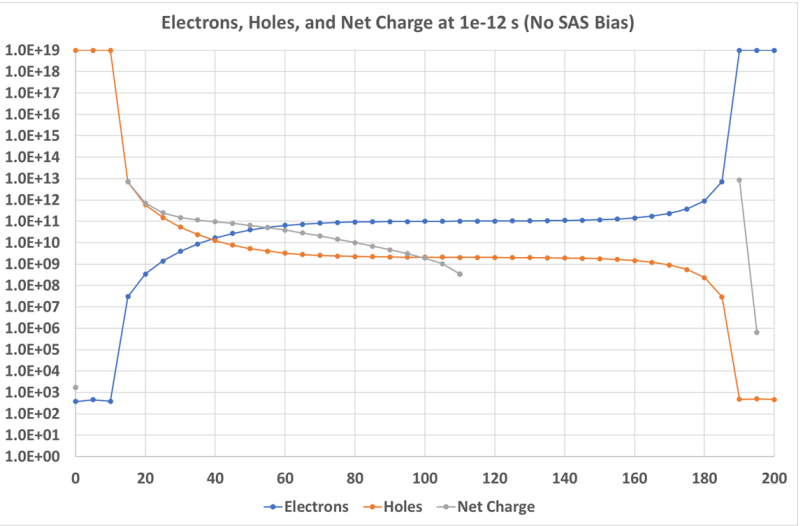
*Brylevskiy, Viktor, Irina Smirnova, Andrej Gutkin, Pavel Brunkov, Pavel Rodin, and Igor Grekhov. "Delayed avalanche breakdown of high-voltage silicon diodes: Various structures exhibit different picosecond-range switching behavior." *Journal of applied physics* 122, no. 18 (2017).

Carrier Profile for Unbiased and Biased SAS

- SAS often reverse-biased to improve performance
- Have used SAS biasing with our COTs SAS diodes and shown improvement (SAS biasing not necessary on higher perfoming PCB boards)
- (At right) are shown electron and hole concentrations initially in SAS from TCAD simulation along with net or space charge (grey)
- (Top) For SAS biasing shows the low levels of initial carrier concentration (space charge is at 1e11/cm3 indicative of intrinsic n- doping of 1e11/cm3)
- (Bottom) For the case of no SAS biasing shows the higher levels of initial carriers and space charge (falls off)
- Originally led to believe SAS biasing lowered capacitance of SAS for improved performance
- SAS biasing helps to raise starting voltage on SAS before ramped voltage and improve depletion (removal of carriers) in the space charge region
- When SAS pulsing is repeated, SAS does not have time to recover fully but SAS can still operate (typically with higher riserate DSRD input)



Initial Biased SAS Carrier Profile

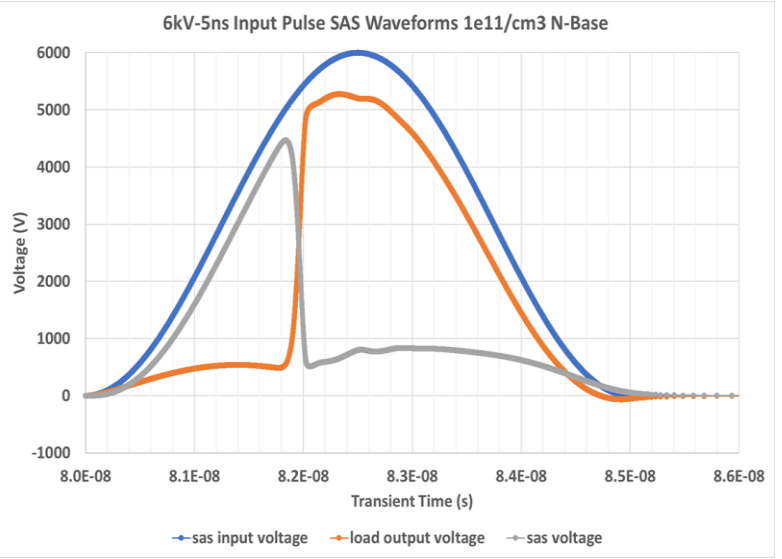


Initial Unbiased SAS Carrier Profile

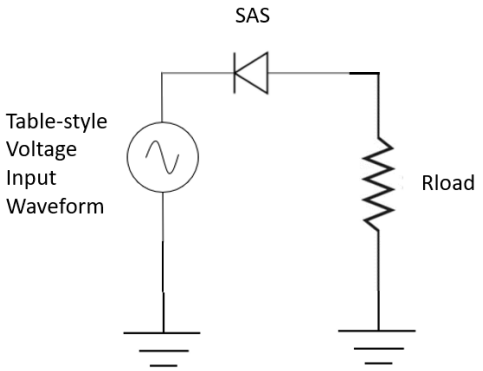
SAS: TCAD Modeling and Simulation

SAS Circuits and Characteristic Waveforms

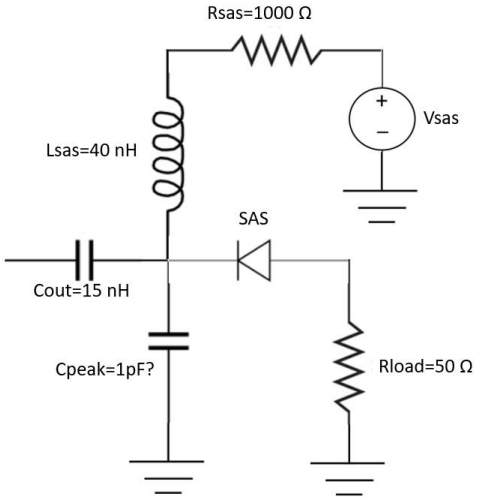
- Simple circuit used for SAS simulation as in literature (bottom left)
- SAS biasing accomplished with circuit (at bottom right), note this circuit is attached at Cout of the DSRD pulser (SAS biasing and peaking capacitor not always present)
- Simple circuit is faster to simulate and easier to analyze
- Realistic pulser circuit more comparable to experiment



SAS Simulation Waveforms



Simple SAS Simulation Circuit



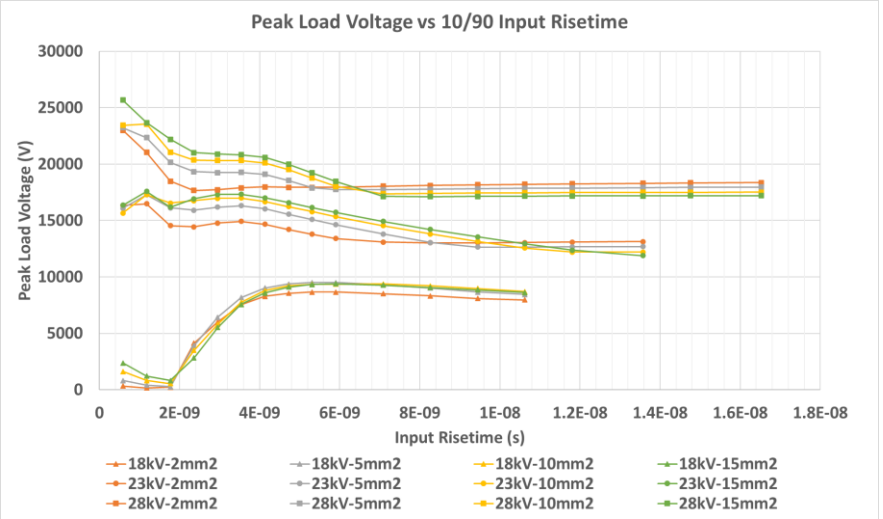
SAS Biasing Circuitry

- Typical SAS simulation waveforms (shown above)
- (Blue) Input voltage waveform
- (Orange) load output waveform-sharpened
- (Grey) SAS voltage showing voltage collapse of SAS
- Note how closely the SAS voltage follows the input voltage due to SAS capacitance

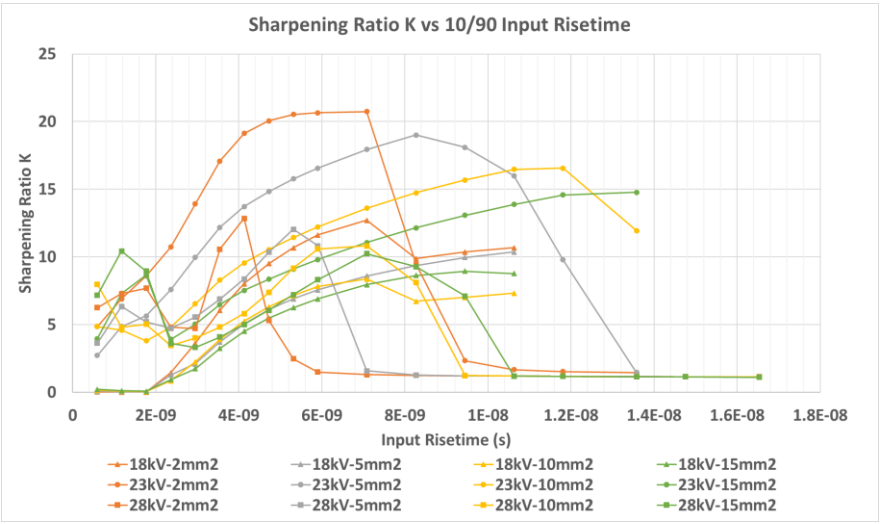
SAS: TCAD Modeling and Simulation

Summary of Simple SAS Simultion

- Want to either tailor SAS to DSRD output pulse or DSRD output pulse to SAS (can depend on circumstances)
- SAS are generally stacked for higher voltage
- SAS of certain thickness needed for DSRD input pulse of certain peak, as well, area affects this operation (for example 1cm^2 area SAS require stacking to sharpen effectively)
- With increases in input peak or area, peak load voltage increases generally
- Load risetime shorter with lower input peak and smaller area
- Opposite trends of peak load voltage and risetime requirements give an optimum SAS geometry for performance
- Vout/Vin not highest for optimal peak load voltage/ristime performance
- SAS Sharpening Ratio tends higher for lower area
- Stacked SAS have higher sharpening ratio
- Highest sharpening ratio does not coincide with optimal peak load voltage/risetime performance
- 200um-thick SAS 5-stacked with 5mm2 area performed best overall



SAS Peak Load Voltage vs Input Risetime

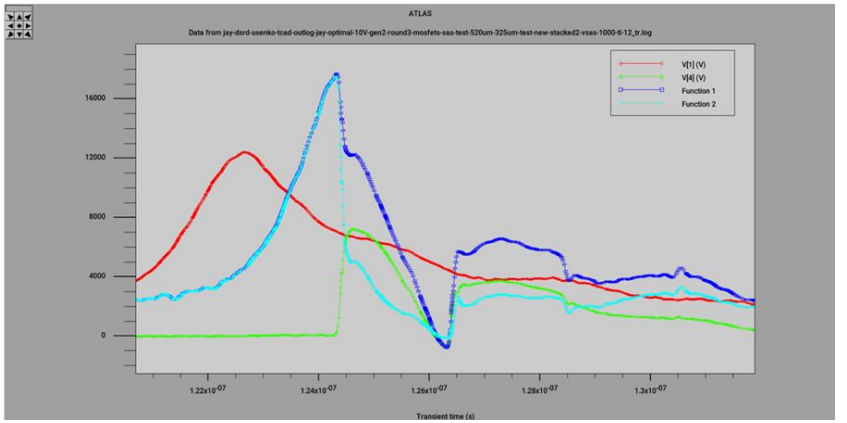


SAS Sharpening Ratio vs Input Risetime

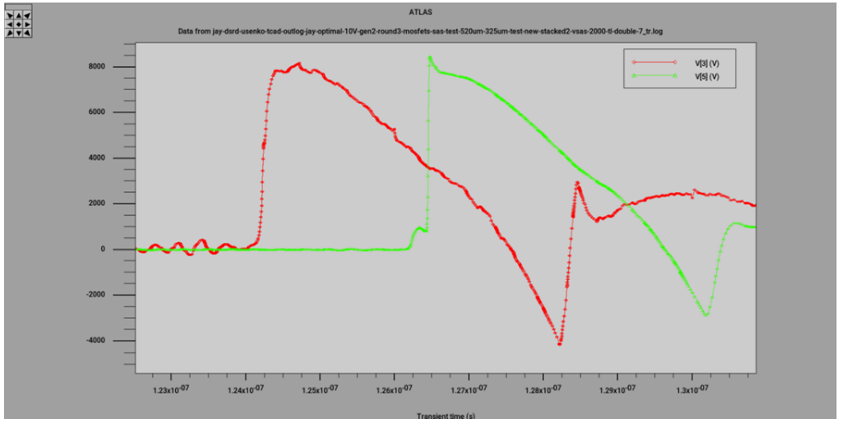
SAS: TCAD Modeling and Simulation

SAS Within Transmission Lines and Multiple Sharpening Sections

- SAS often are reported as being included into the gap of the center conductor of a transmission Line (TL)
- Recent work by Kesar*, shows the necessity of including TLs in SAS simulations for simulation accuracy
- (Top Right) are shown the input voltage waveform (V[1]-red), load voltage (v[4]-green), SAS cathode voltage (Function 1-dark blue), and SAS voltage (Function 2-light blue) demonstrating that the SAS cathode voltage can rise to nearly twice the input waveform (here about 1.4 x)
- (Bottom left) is shown the output waveforms at the load for including two separate, sufficiently spaced SAS within a TL producing a second subsequent sharpening
- Efforts are being made to include SAS into high performance TLs
- Efforts are being made to produce two SAS sharpening sections to lower load risetime



SAS Simulated Within Transmission Line



Two SAS Separated SAS Sharpening Sections

*Ivanov, Mikhail, Viktor Brylevskiy, Irina Smirnova, and Pavel Rodin. "Picosecond-range switching of high-voltage Si diode due to the delayed impact-ionization breakdown: Experiments vs simulations." *Journal of Applied Physics* 131, no. 1 (2022).

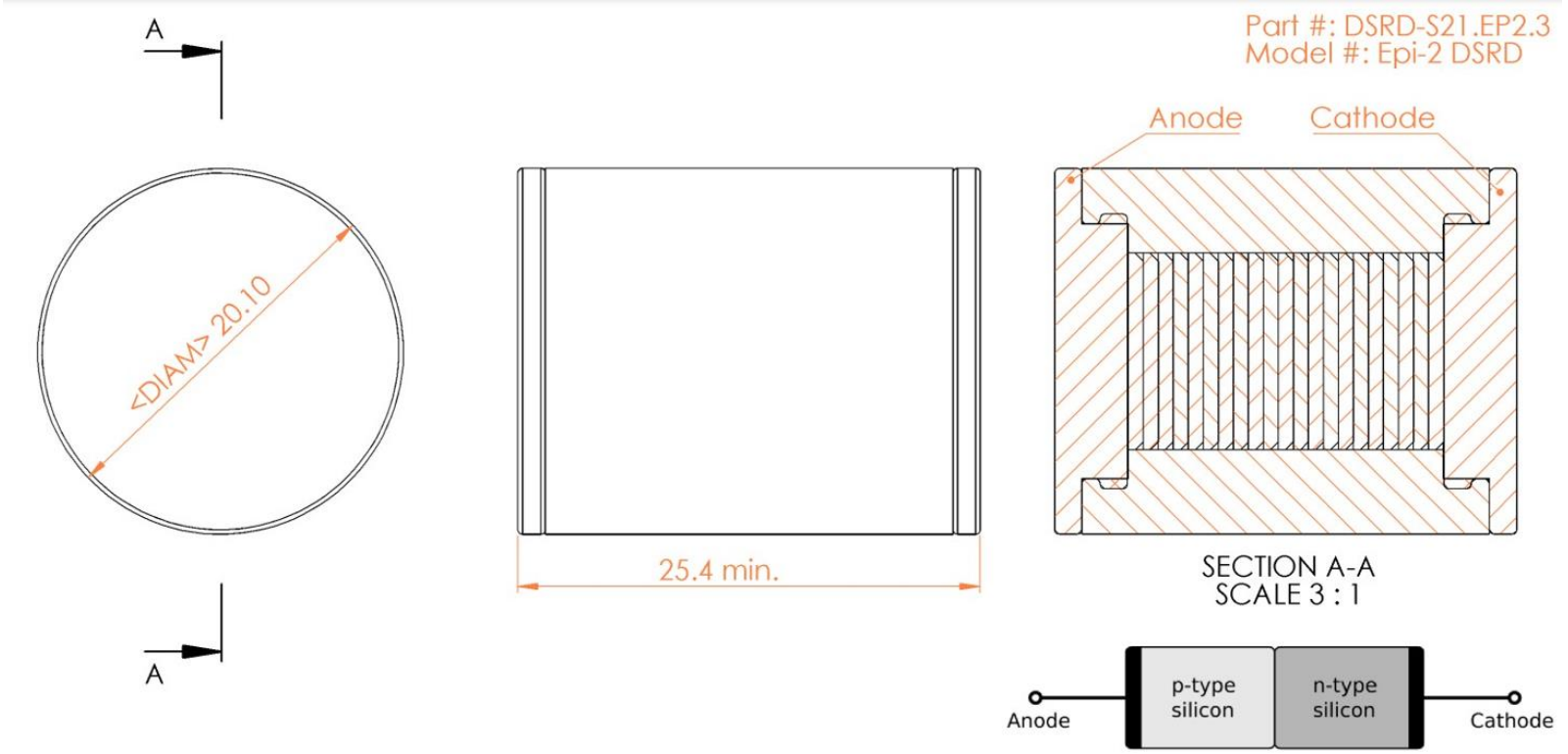
DSRD Fabrication: Gen2 Process Flow

Simplified Gen2 process flow for stacked, passivated, and encapsulated DSRD

- A • Starting material: highly As-doped epi-ready Si wafer
- B • Graded n-type epitaxy in first reactor
- C • Graded p-type epitaxy in second reactor
- D • Wafer metallization via physical vapor deposition
- E • Partial cut bevel-edge groove of wafer with dicing saw
- F • Full singulation straight-cut of residual Si with dicing saw
- G • Edge surface clean and surface passivation
- H • DSRD chip-stack compressed assembly with Cu-contacts
- I • Chip-stack encapsulated with thermally conductive epoxy

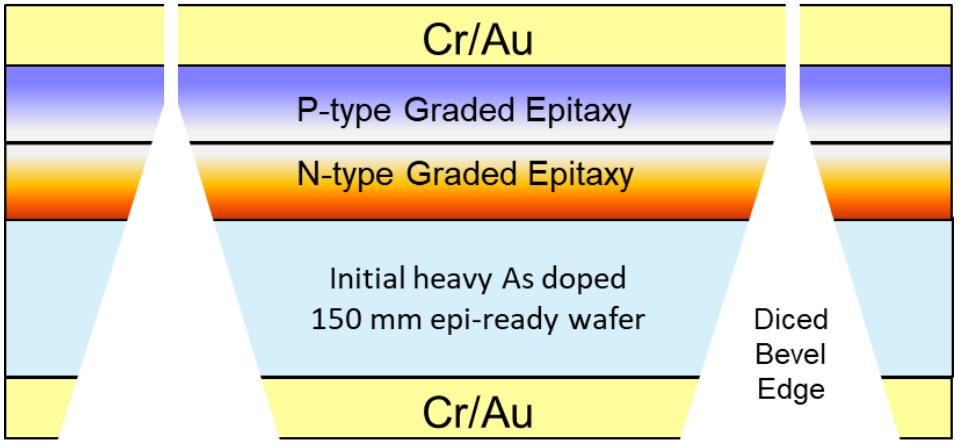
Gen2 lots use graded epitaxy. Other new process steps will be implemented for Gen3 during Year-2

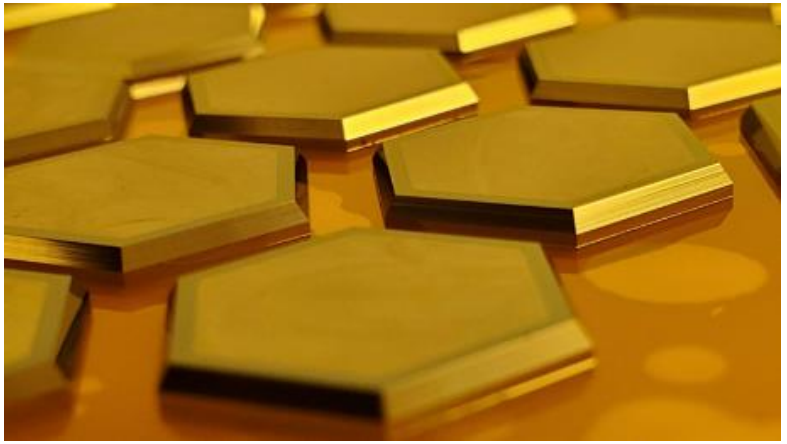
DSRD Fabrication: Encapsulation Design



Encapsulation design used in Gen2 lots. During project 2nd year improvements will be toward better thermal sink from the device

DSRD Fabrication: Bevel Cut by Dicing Saw





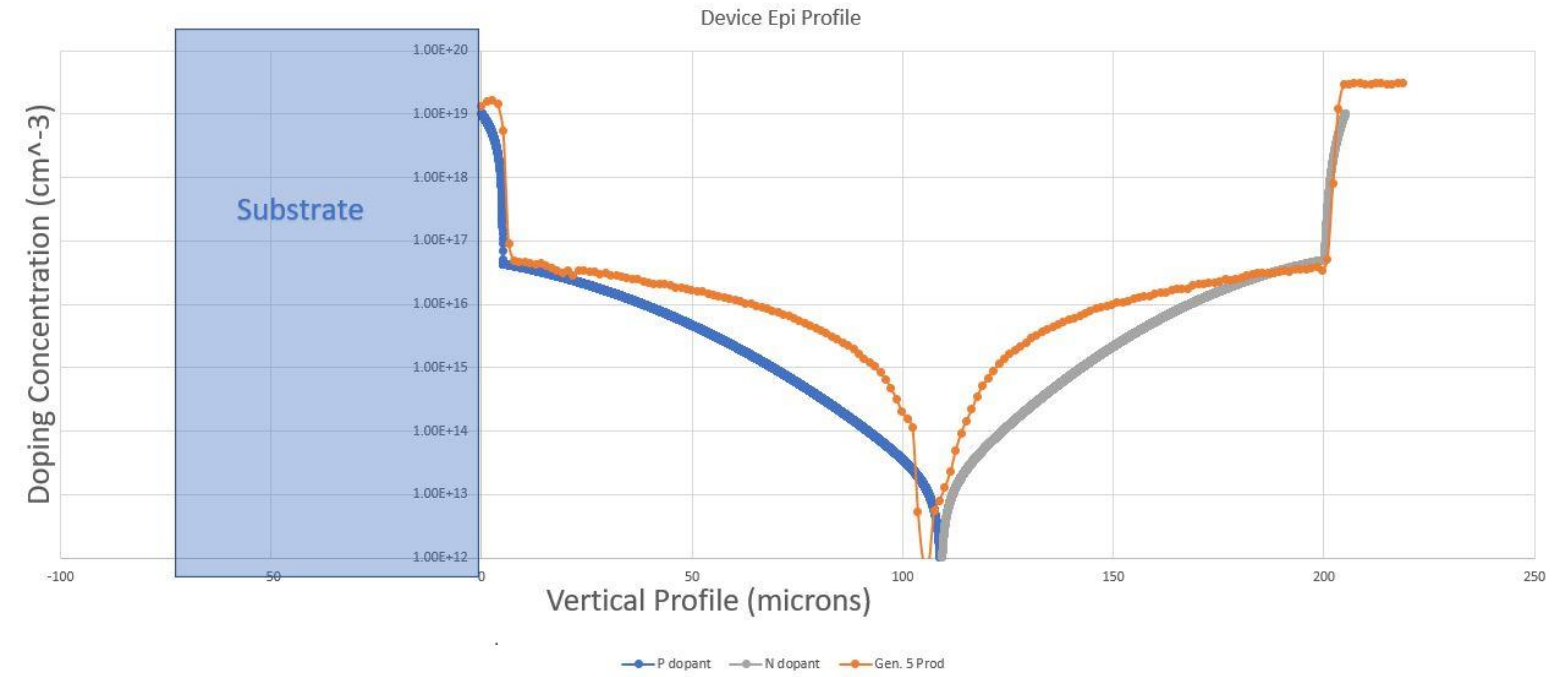
Single DSRD dies ready for stacking

DSRD beveled and hexagonal-cut chips with 1-cm^2 area, 825um total-thickness, and Cr-Au metal contacts

DSRD Fabrication: Final Product

Gen2-4 21- and 42-diode stack

DSRD Fabrication: Gen2-5 Doping Profile



- **Gen 2-5 is the Ideal DSRD doping Profile predicted.**
- **5th epitaxy run was less successful in copying of an ideal doping profile into silicon**

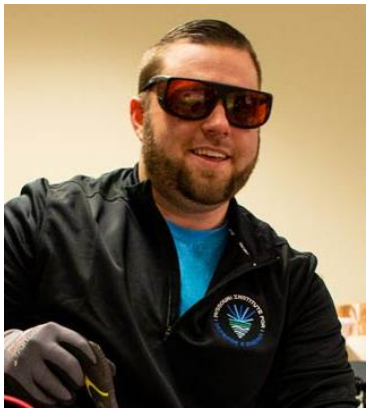
Summary

- **A working theory for driving DSRD-based pulser has been developed**
  - Can optimize/increase DSRD reverse current with minimum prime supply voltage
  - Can predict maximum PRF based on Prime source and Capacitance
  - Simulation closely agrees with experiment and theory.
- **Experimental load output of 16 kV achieved**
  - Output does not match with LT-Spice Simulation (44 kV)
  - LT-Spice DSRD model is not accurate
  - DSRD does not snap as fast as expected
- **TCAD models (most accurate/quantitative models) are used to design DSRD and SAS doping profile**
  - By altering design of DSRD doping profile, we have achieved the best DSRD yet!!
  - Simulations have shown shorter risetimes achievable by matching of SAS doping profile and geometry to DSRD input waveform
  - Successive sharpening with multiple SAS sections can significantly lowers pulse risetime.
- **Our novel approach for DSRD manufacturing have been experimentally proven**
  - 5 lots of Gen2 DSRD diodes have been manufactured, supplied to pulser team and tested
  - The pulse performance tests shown significantly better performance as compared to competitors
  - Both – UMKC tests, and independent lab tests (Ron Focia) confirmed that our in-house made DSRDs give higher pulse magnitude, shorter rise time and higher rise rate as compared to all available competitor DSRDs

Recommendations and Future Work

- **Alternative methods to increase DSRD reverse current**
  - Increasing prime supply voltage
  - Increasing MOSFET open-circuit voltage (Stacking MOSFETs/Thyristors)
  - Using NLTL to amplify DSRD current
- **How to make DSRD step recovery fast**
  - Does recovery depend on reverse current? (yes, simple circuit DSRD simulations show both the reverse current maximum and reverse current fallrate influence snap-off time)
  - Manipulating injection efficiencies may allow for best improvement in DSRD snap-off time along with careful study of doping profile parameter variation and internal carrier distributions
- **Better circuit simulations with SmartSpice**
  - SmartSpice CMC Verilog-A DSRD model can be fit more closely to match experimental result
  - SmartSpice allows use of manufacturer models for primary switches (gate drivers/MOSFETs/Thyristors)
- **Optimization and implementation of SAS**
  - SAS doping profile and geometry variations to match DSRD output for sharpening
  - SAS studies within TLs for improved performance
  - SAS studies with multiple SAS sections (sufficiently spaced) for improved sharpening capabilities
- **Finish upgrading of DSRD manufacturing process**
  - Replacement of deep diffusion by graded epitaxy finished and gave us the best DSRD already
  - Now concentrate on implementing all other new process steps we suggest - diode side termination and passivation, stacking and packaging

Personnel



Roy Allen
Director of Research

Alex Usenko
Research Professor

Gyanendra Bhattarai
Asst. Res. Professor

Jay Eifler
Post Doc. Associate

Shailesh Dhungana
Post Doc. Associate

Sapeth Will
Graduate Student

Outputs

- G. Bhattarai, J. Eifler, R. Allen, and T. Fields, “DSRD-based pulse generator: Theory and Experiments,” 2023, Journal article in preparation. Journal Publications In Preparation
- S. Bellinger, A. Caruso, A. Usenko, “Bond-and-Thin Process for Making Heterogeneous Substrate with a Thin Ga2O3 Layer oN Polycrystalline SiC Substrate”, presented at 6th U.S. Workshop on Gallium Oxide (GOX 2023) University at Buffalo Campus, Buffalo, New York, August 13-16, 2023.
- S. Bellinger, A. Caruso, R. Focia, A. Usenko, “Optimal doping profile and new mesa passivation design for drift step recovery diode” Abstract - 24th IEEE Pulsed Power Conference, San Antonio, TX, June 25-29, 2023.
- S. Bellinger, A. Caruso, A. Usenko, “Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme”, Oral Presentation, Conference Digest GOMACTech 2023, San Diego, CA, March 20 – 23, 2023.
- A. Usenko, S. Dhungana, A. N. Caruso and S. L. Bellinger, “Electroless Nickel Plating for Ohmic Contacts to Silicon Power Devices,” Oral Presentation, Abstracts of 242nd Electrochemical Society Meeting, Atlanta, GA, October 9-13, 2022.
- S. Bellinger, A. Caruso, A. Usenko, “Stacked Diode with Side Passivation and Method of Making the Same,” US Patent Application 17/946022 filed 09/15/2022.
- A. Usenko, A. Caruso, S. Bellinger, S. Dhungana, R. Allen, “Adopting Processes from Mainstream Silicon Technology to Discrete Power Devices Technology,” 2nd Annual Workshop on Solid State Devices and Applications for Directed Energy at GE Research in Niskayuna, NY, October 26-28, 2022.
- A. Caruso, A. Usenko, “ENGINEERED SUBSTRATE FOR RADIATION HARD CHIPS AND METHOD OF MAKING THE SAME”, Invention Disclosure filed Oct.5. 2023.

Thank You

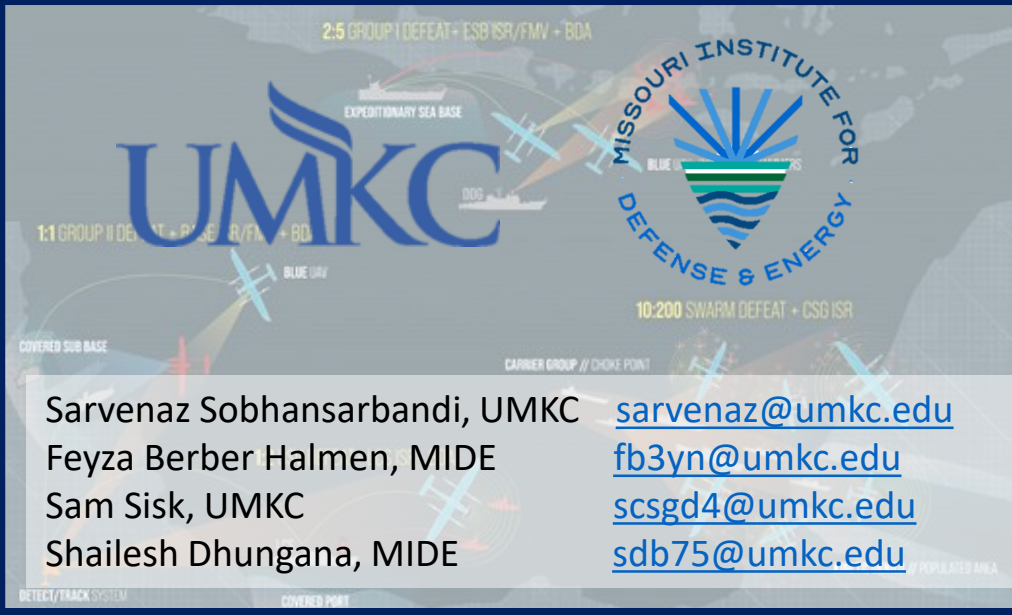
Pulse Tactical Effector for Regulated Attack

Pushing Beyond GaN Limits through Cooling

PTERA Grant Annual Review

October 10, 2023

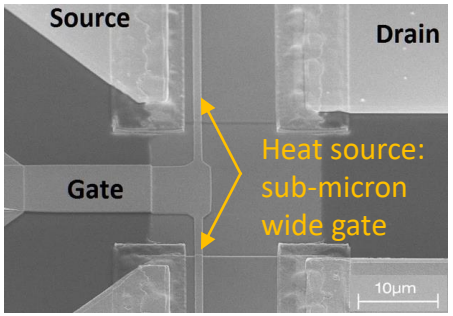
Funding provided by ONR under grant N00014-22-1-2385

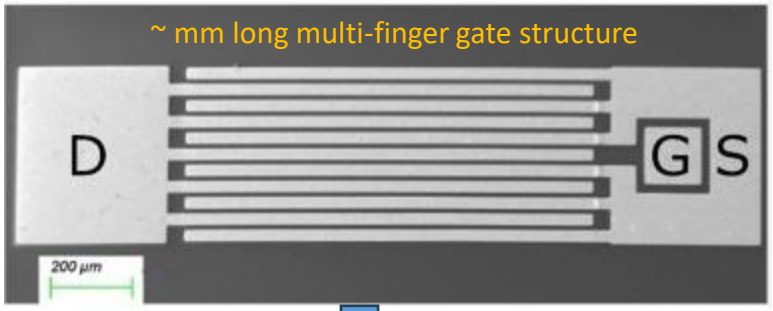


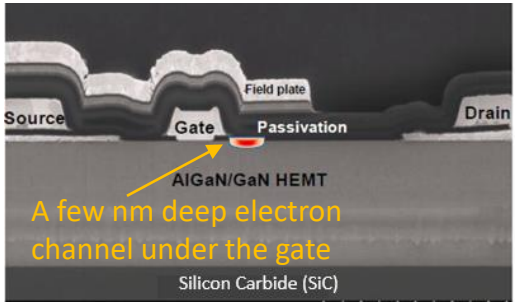
Sarvenaz Sobhansarbandi, UMKC sarvenaz@umkc.edu
Feyza Berber Halmen, MIDE fb3yn@umkc.edu
Sam Sisk, UMKC scsgd4@umkc.edu
Shailesh Dhungana, MIDE sdb75@umkc.edu

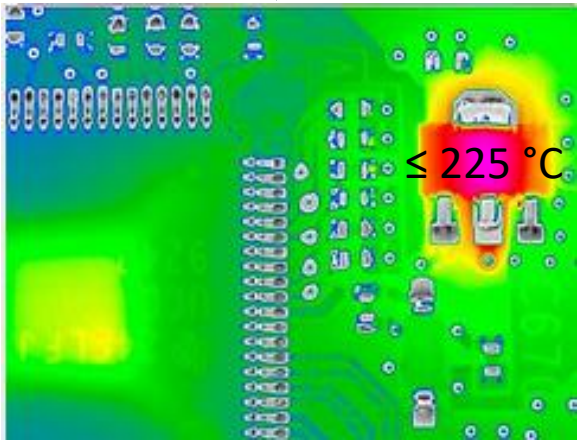
Motivation

- Effects-driven, high peak power RF source is needed to meet the PTERA offensive & defensive electronic mission requirements within SWAP-C^2 specifications.
- Solid-state power amplifiers (SSPA) utilizing gallium-nitride (GaN) semiconductors offer the best commercially available solution.
- High power density (W/mm) of GaN PAs result in excessive heating.





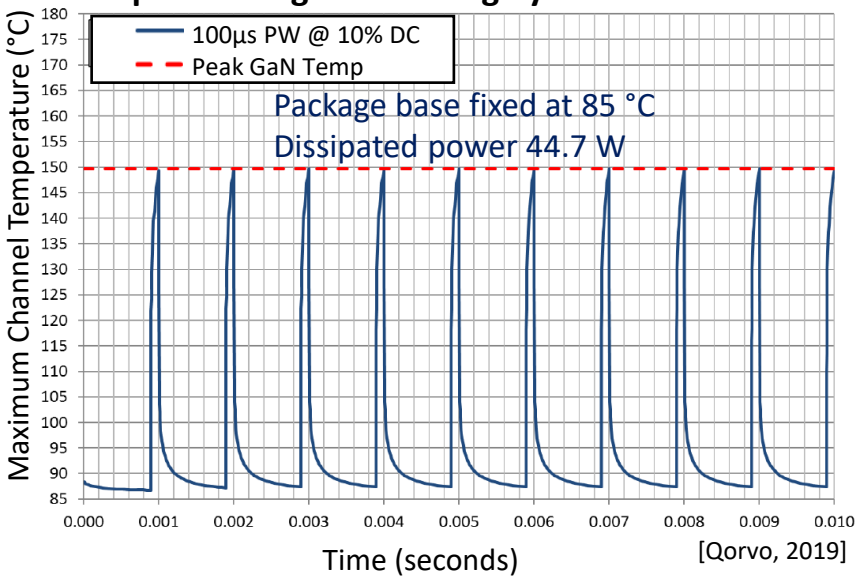




Motivation

- High power GaN PAs are operated in pulsed mode to avoid performance and reliability degradation due to heating, effectively reducing the average output power.

Example Heating and Cooling Cycle in Pulsed Mode



[Qorvo, 2019]

GaN PAs of interest

Output power = 1.8 - 7 kW + Efficiency ≤ 65 %

Dissipated power = 1 – 3.8 kW

+ Hot spot area 10s of sub-micron by mm gate fingers

+ Max Channel Temperature ≤ 225 °C

+ No active cooling

Pulse width ≤ 200 µs & Duty cycle ≤ 1%

Objective

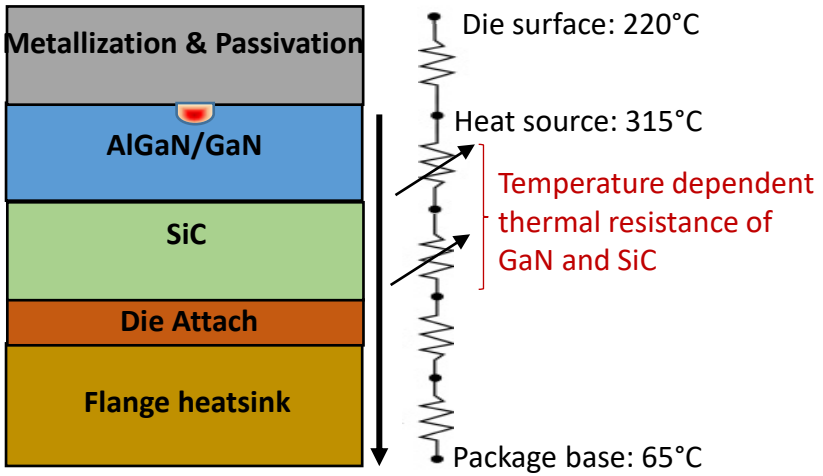
- Thermal management is required to increase the duty cycle or pulse width of GaN PAs, to increase the average output power achievable with such a PTERA source.
- This effort focused on
  - Modeling the thermal response of the GaN PAs to assess the cooling requirements for different operating conditions, and
  - Design and fabrication of an **Ultra Jet Impingement Thermal Management System (UJI-TMS)**, with a cooling density of **2 kW/cm²**, double the SOTA.

Tasks & Milestones	15 Months														
	M1-M3			M4-M6			M7-M9			M10-M12			M13-M15		
GaN device modeling & verification															
Electro-thermal GaN PA simulations															
Fin integrated jet impingement modeling															
Milestone 1: GaN modeling & baseline design completed															
UJI-TMS design modifications															
Experimental design setup															
Milestone 2: UJI-TMS Design finalized															
UJI-TMS Fabrication															
Experimental validation															
	Deliverables														
Technical reports															
Journal, Conference Publications and Presentations															

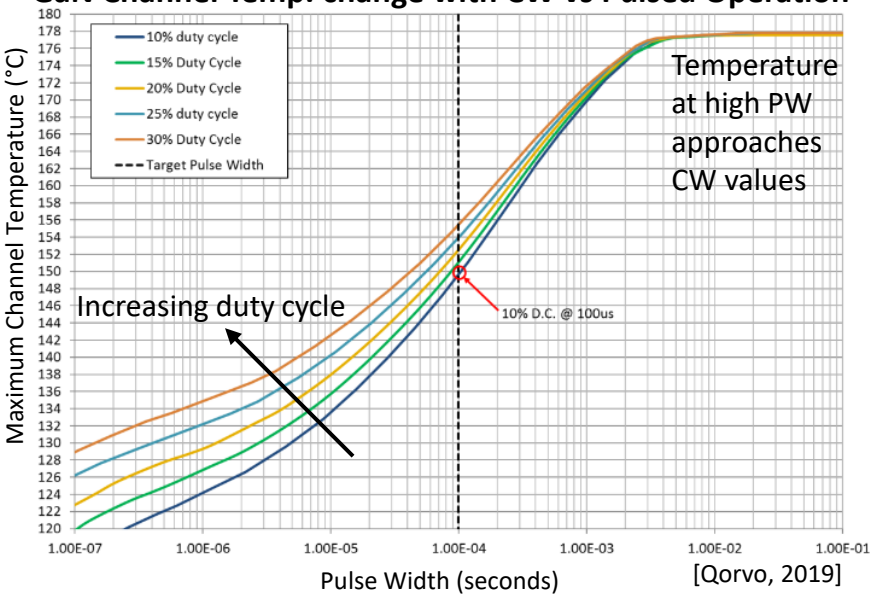
GaN Device Modeling

- To determine cooling requirements for different GaN operating conditions (pulse width & duty cycle), temperature dependent thermal resistance of GaN PA is needed.

Thermal path between hot spot & TMS



GaN Channel Temp. change with CW vs Pulsed Operation



[Qorvo, 2019]

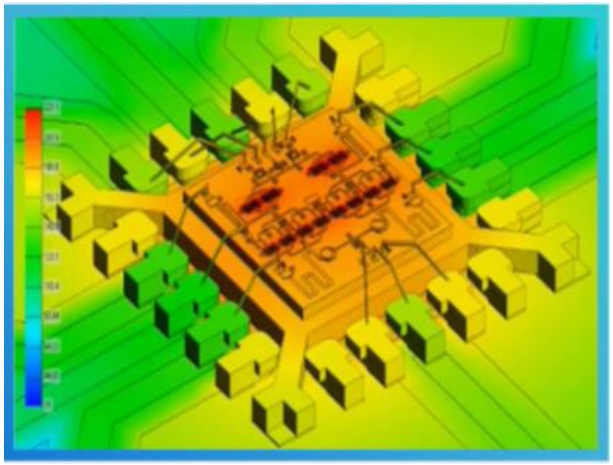
- Challenge: GaN device layers and properties are foundry-dependent and proprietary.
- GaN thermal modeling involved data collection from open literature in Fall 2022.
- 2.6 kW Macom GaN PA data was shared by Macom in Spring 2023 after collaboration agreement and NDA.

MACOM®
Partners from RF to Light

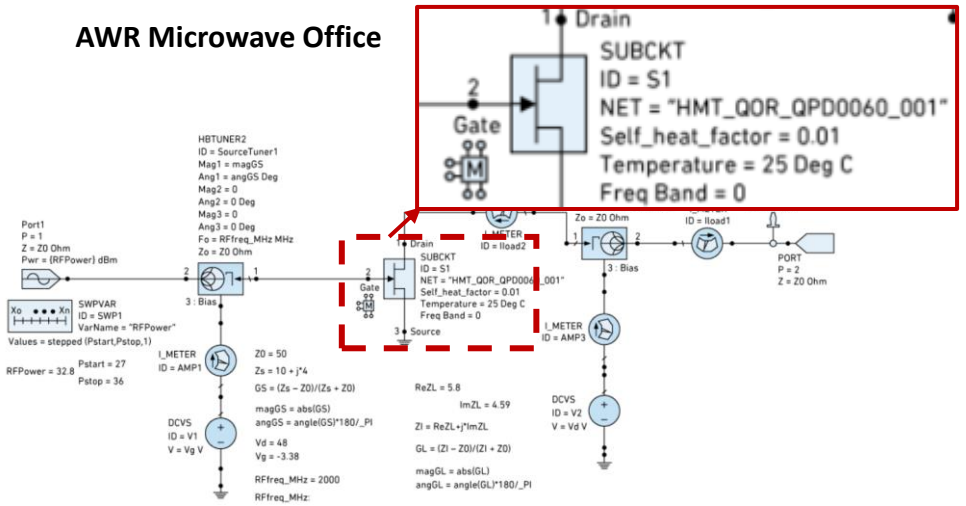
Electro-thermal GaN PA Simulations

- Another method considered for determining cooling requirements was GaN device simulations.

Celsius Thermal Solver



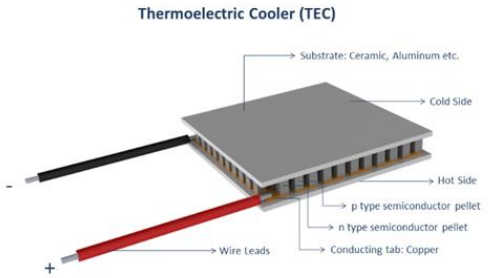
AWR Microwave Office

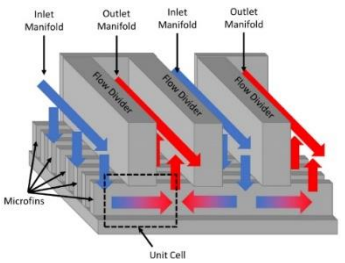


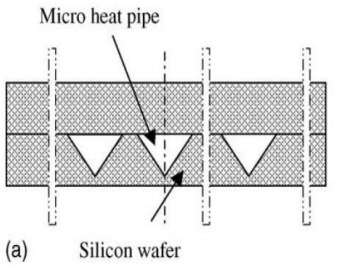
- This effort was abandoned due to lack of necessary models for Qorvo 1.8 kW and Macom 2.6 kW GaN PAs:
  - No models are available with these high power GaN PAs for Celsius Thermal solver,
  - Cadence AWR models available for these GaN PAs do not have a “Temperature” node,
  - “Self heating factor” available in Cadence AWR models are valid for several duty cycles and only for the pulse width of 100 µs.
- Upside of this failed attempt: Cadence AWR / Celsius Thermal Solver software and Modelithics models are acquired and available to MIDE and UMKC for future use.

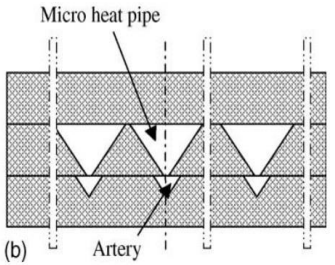
Thermal Solution Space

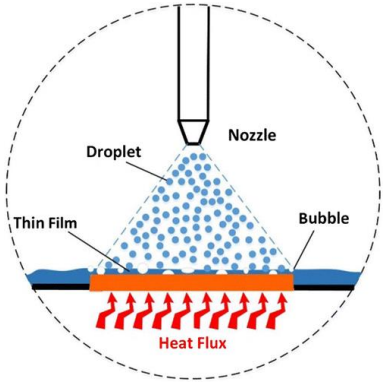
Summary and remarks of the macro-scale cooling technologies for semiconductor devices



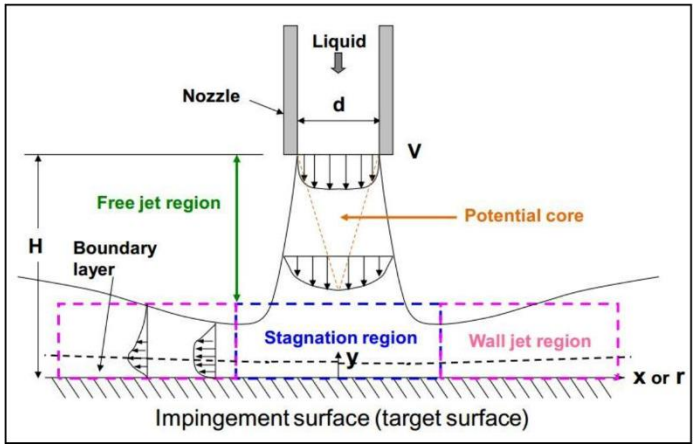








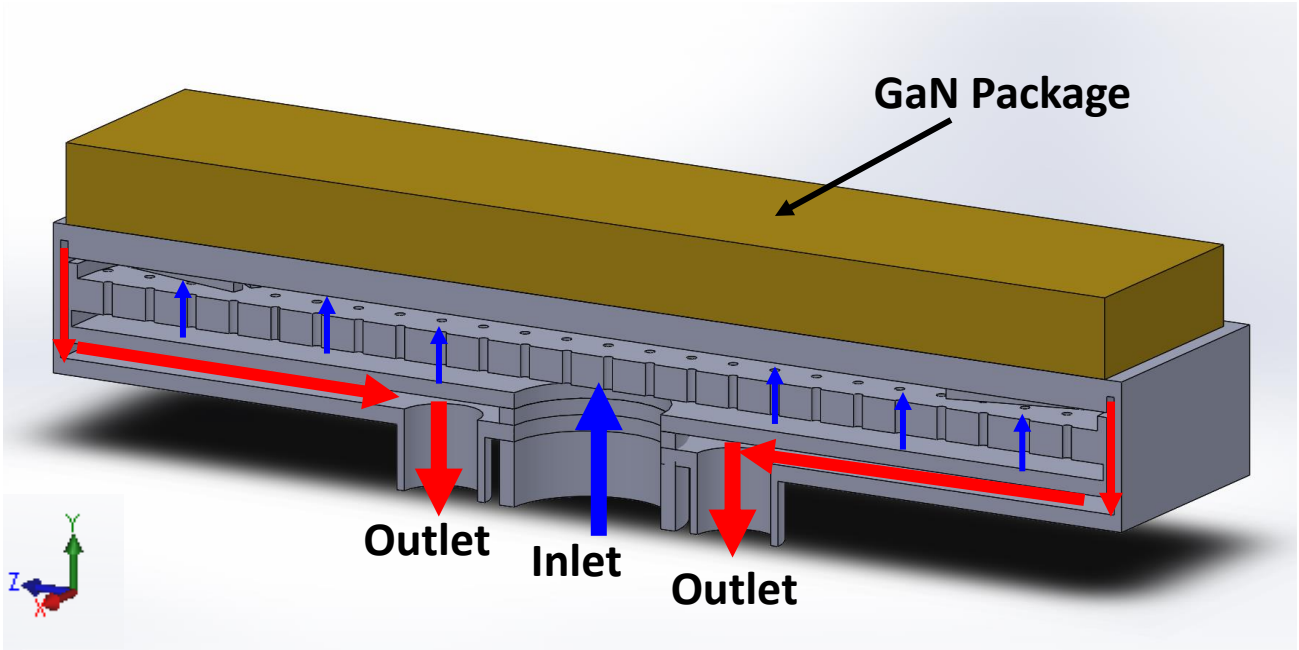
Selected TMS



Pros:

- high heat flux removal;
- Potential to easy re-design/optimization.

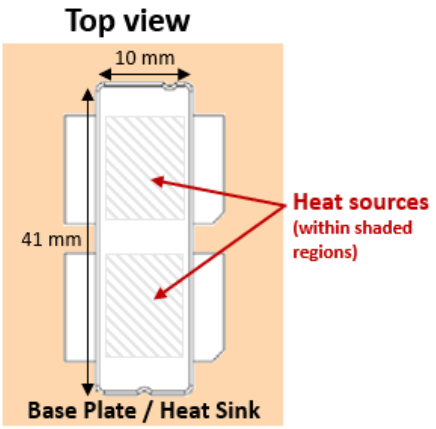
Proposed UJI-TMS Solution



Cross-sectional view of the GaN package and UJI-TMS

- ✓Ultra Jet Impingement based system to deliver a cooling density of **2 kW/cm^2**, <u>double the SOTA</u>, is proposed for GaN PA cooling.
- ✓UJI-TMS integrated with micro fins design proposed herein has active surface heat flux area of **3.28 cm^2**, with around **300 nozzles**, **2 outlets** with equivalent surface area to total nozzle's cross-sectional area.
- ✓The selected type of heat transfer fluid (HTF) for the preliminary analysis is **DI water**.

Technical Approach



GaN Package

Applied Pulsed Power
Thermophysical Properties
Resistances

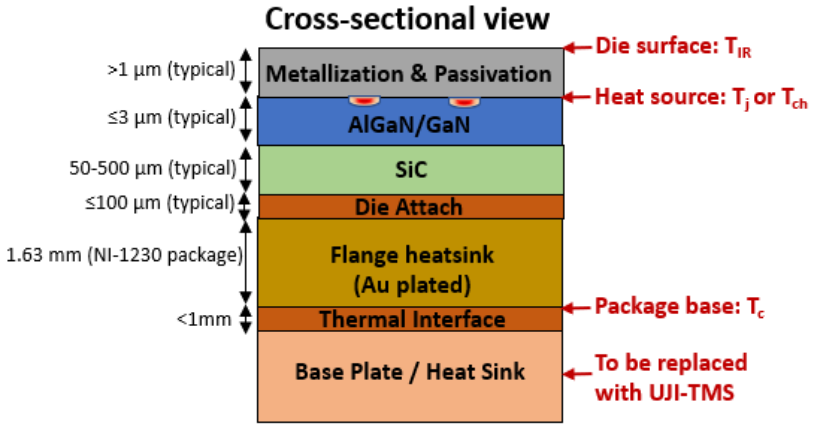
CFD Modeling

Ansys

Experimental
Analysis

Mission

Optimal TMS Design



✓ Manufacturing ability has a tolerance of nearly 10 µm, the optimal jet diameter will be initially tested at 100 µm (0.1 mm).

Technical Approach (CFD Modeling)

❑ Benefit of CFD:

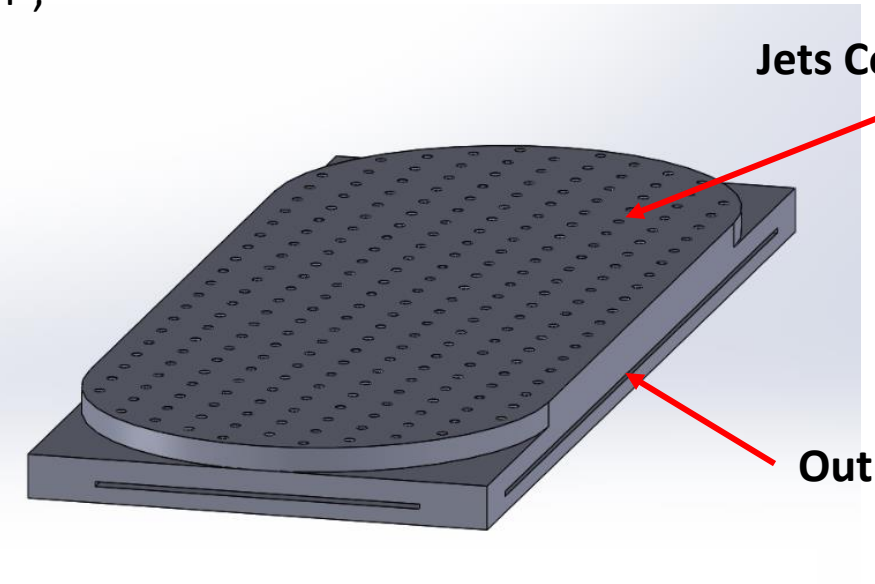
✓Detailed insight of thermal behavior.

Ansys FLUENT

❑ Geometry:

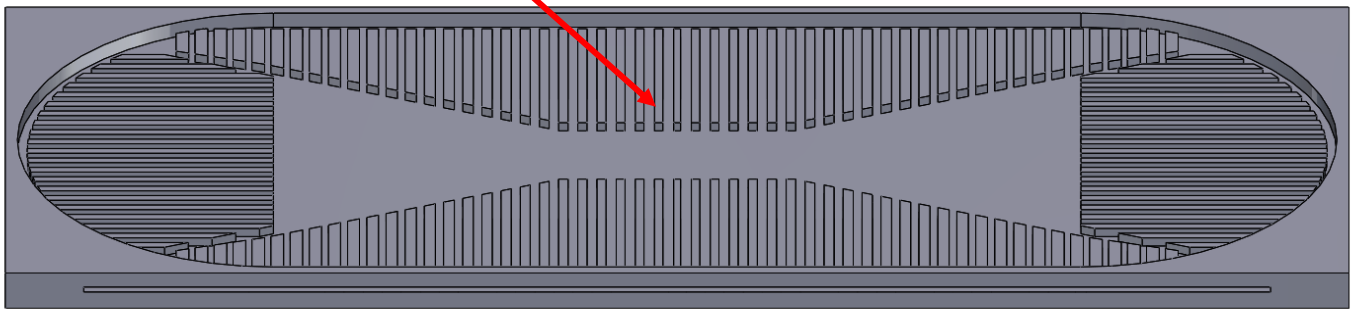
- The geometry is developed by performing **parametric study** on the flow behavior;
- Active surface heat flux area of 3.28 cm^2;
- Around 300 nozzles, 4 outlets.

Jets Configuration



Outlet 4x

Preliminary Fin Array Configuration

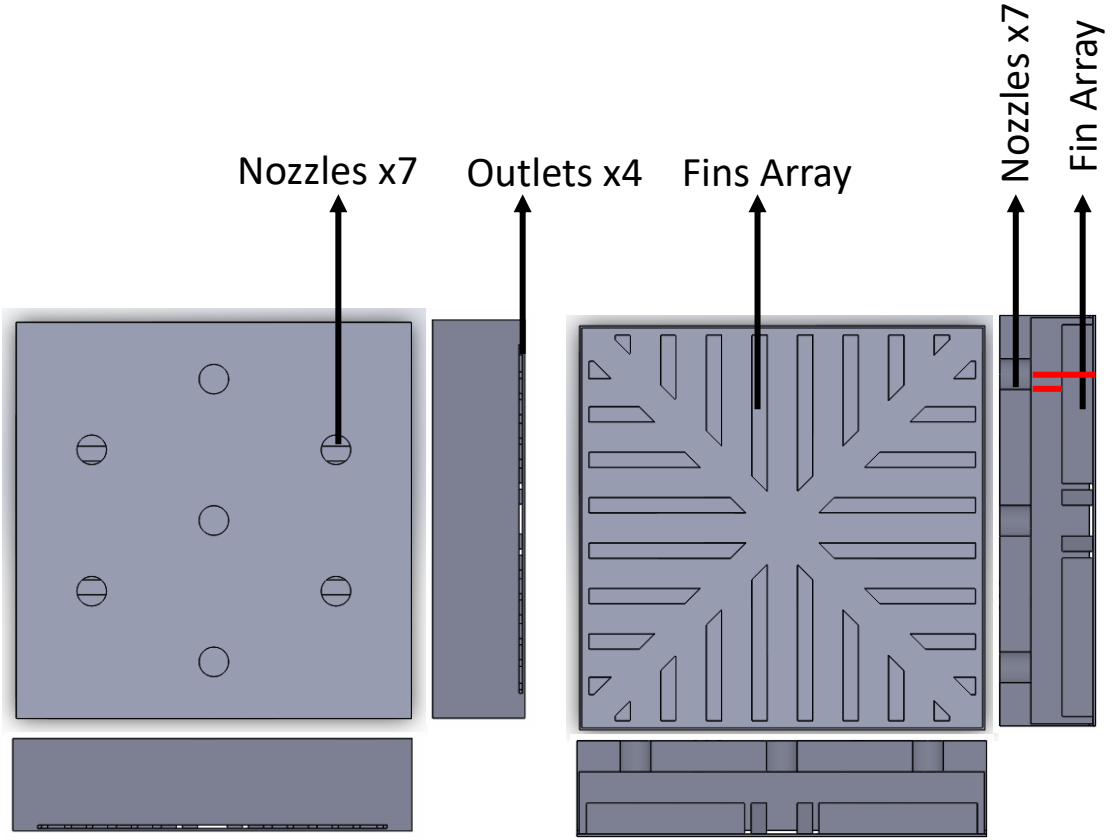


Proof of Concept: Single Array of Nozzles

❑ Motivation:

How the integration of single array of nozzles with fins affect the temperature drop?

- **Nozzles:**
  - Diameter = 0.3 mm (can be smaller)
- **Fins:**
  - Height = D
  - Width = D/2
  - Length = Varies
  - Spacing = D/2
- **Outlets:**
  - Cross Sectional Area x4 = Total Nozzle CS area
- **Internals:**
  - (Impinging length) H/D Ratio = 2 (red line)



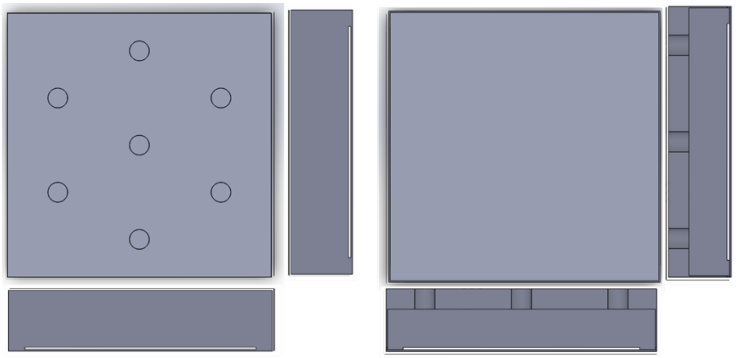
Array of Nozzles

Array of Nozzles w/ Sectional view showing fins

Proof of Concept: Array of Nozzles

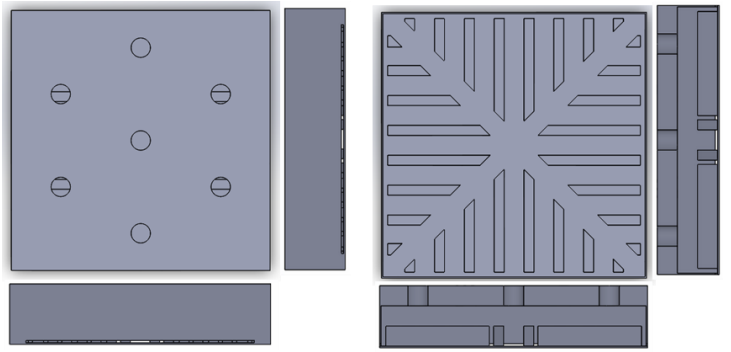
❑ Geometry:

- To develop a UJI-TMS a preliminary analysis of geometrical features was done to minimize simulation time for new geometric modifications:



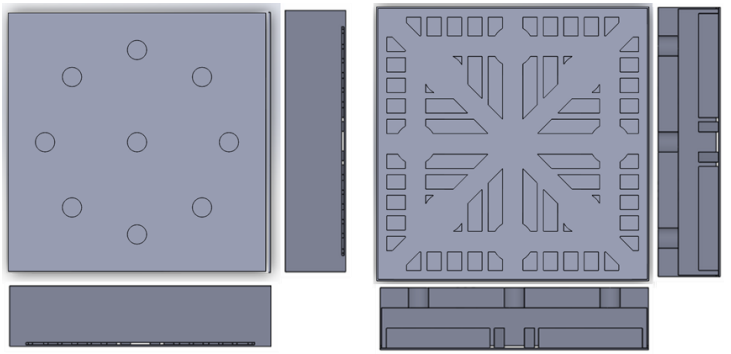
(a)

- (a) A basic JI model was created as a datum for the addition of fins;



(b)

- (b) A simple fin model was created from the basic JI model with fins directing fluid to the four outlets



(c)

- (c) An optimized fin model was created to work in tandem with the jets to allow for open fluid flow

Meshing Method and Boundary Conditions

❑ Mesh:

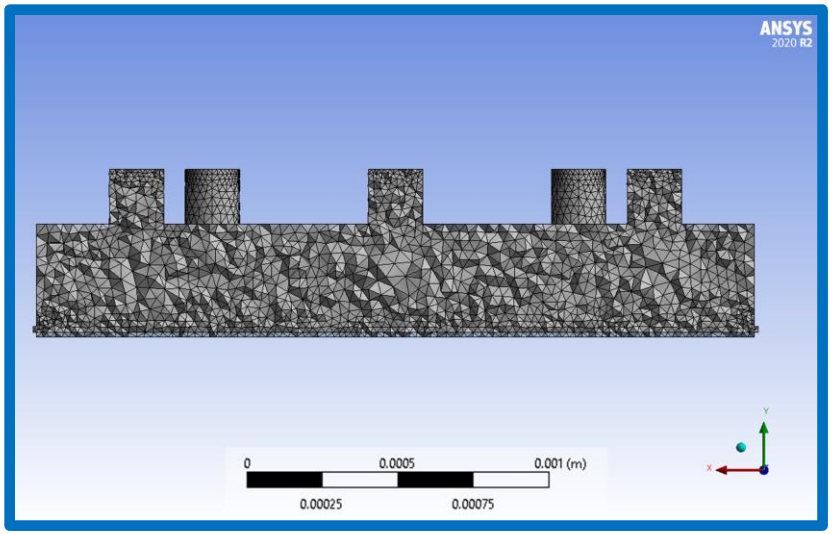
- Tetrahedron mesh elements;
- Maximum skewness < 0.9;
- Orthogonal quality > 0.1;
- Mesh sizes from 500K - 2.2M Elements and 82K-400K nodes;

❑ Mesh Independency:

- Each mesh nodes and elements will be increased until the results from previous simulation mesh and current mesh difference is less than one percent.
- This is done to increase mesh quality to ensure credible simulation results.

❑ Simulation Set-Up:

- Standard k-epsilon physics model for focus on turbulency;
- Heat Flux of 2 $\frac{kW}{cm^2}$ on Heated Plate;
- Fluid outlet cross sectional area is equivalent to the sum of nozzles surface area;
- Incoming fluid is set to 40 m/s at a flow rate of 3.1 GPM;
- Simulation method has been validated with similar experimental results available in the literature.



Boundary Conditions

Simulation Set-Up:

- Standard k-epsilon physics model for focus on turbulency;
- Heat Flux of 2 $\frac{kW}{cm^2}$ on Heated Plate;
- Fluid outlet cross sectional area is equivalent to the sum of nozzles surface area;
- Incoming fluid is set to 38 m/s at a flow rate of 3.1 GPM;
- Simulation method has been validated with similar experimental results available in the literature.

Parameter	Value
Inlet velocity	38 m/s
TMS material	Aluminum
TMS Coolant	Di Water
Number of nozzles	7-9
Nozzle outlet to diameter ratio	2
Nozzle spacing	0.3 mm
Re number	0.952 mm
Fin height	10000 – 11400
Number of outlets	4x
Outlet area	Sum of the nozzles cross sectional area

Energy Model

$$\frac{\partial(\rho E)}{\partial t}+\frac{\partial(\rho u_i E)}{\partial x_i}=\frac{\partial}{\partial x_j}\left[(\mu+\mu_t)\frac{\partial T}{\partial x_j}\right]+\frac{\mu_t}{Pr}\frac{\partial u_i}{\partial x_j}\frac{\partial u_i}{\partial x_j}+Y$$

Transport Equation for k

$$\frac{\partial(\rho k)}{\partial t}+\frac{\partial(\rho u_i k)}{\partial x_i}=\frac{\partial}{\partial x_j}\left[(\mu+\mu_t)\frac{\partial k}{\partial x_j}\right]+G-\rho\varepsilon$$

Transport Equation for epsilon

$$\frac{\partial(\rho \varepsilon)}{\partial t}+\frac{\partial(\rho u_i \varepsilon)}{\partial x_i}=\frac{\partial}{\partial x_j}\left[(\mu+\mu_t)\frac{\partial \varepsilon}{\partial x_j}\right]+C_{\varepsilon 1}\frac{\varepsilon}{k}G-C_{\varepsilon 2}\rho\frac{\varepsilon^2}{k}$$

CFD Validation: Modeling Methodology

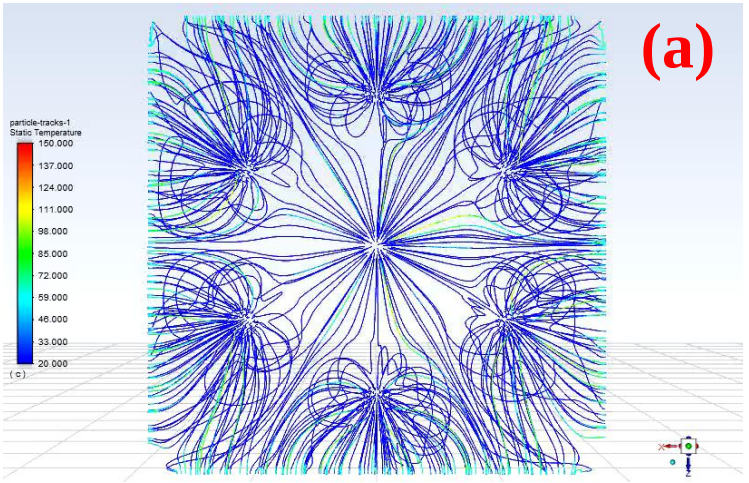
- To validate the selected CFD modeling approach, a specified JI model proposed by Wu et al. [1] is developed:
  - Impinging jet geometry with 22 nozzles of 300 micrometer diameter;
  - For the purpose of validation, all geometrical and initial conditions were used exactly as stated in their work;
  - The recreated geometry was then meshed with tetrahedral meshing method and simulated under k-epsilon viscous flow model.
  - The comparison of the results showed an average difference of 4.96% between the developed simulation model and experimental work proposed by Wu et al. [1] for the surface temperature.

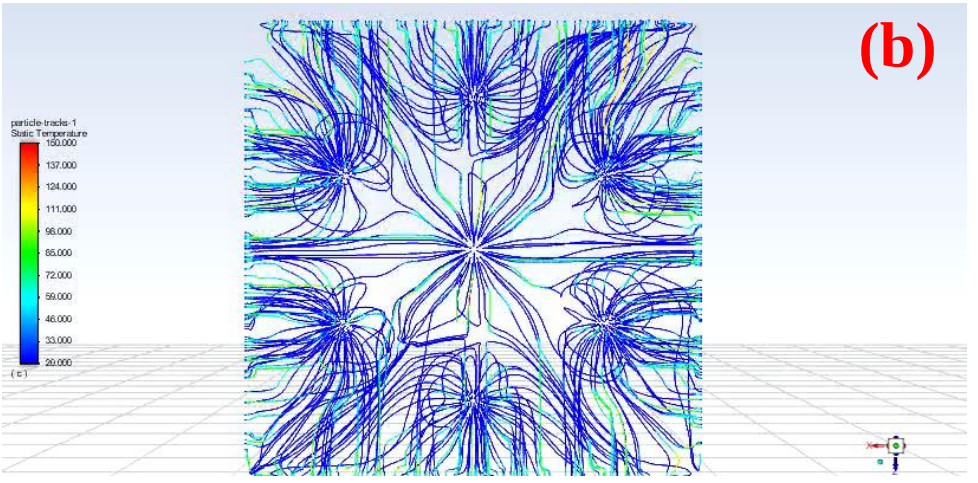
TABLE 1. Methodology validation results

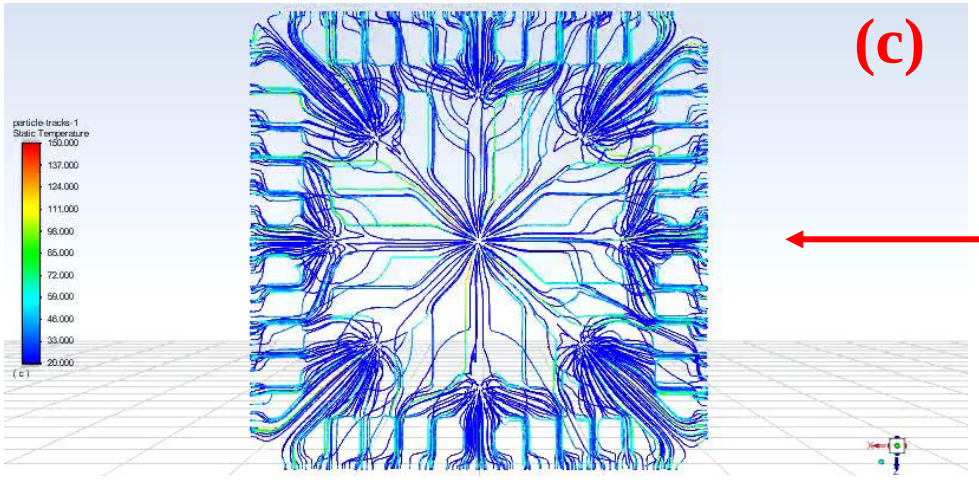
Power (W)	Exp. T (°C) [29]	Sim. T (°C)	Percent Diff.
100	4.94	5.51	11.59
150	7.75	7.59	2.106
200	9.98	9.16	2.81
250	12.4	13.05	5.31
300	15.06	15.51	3.02

[1] Wu, R., Hong, T., Cheng, Q., Zou, H., Fan, Y., and Luo, X., 2019. "Thermal modeling and comparative analysis of jet impingement liquid cooling for high power electronics". International Journal of Heat and Mass Transfer, 137, pp. 42–51.

CFD Results





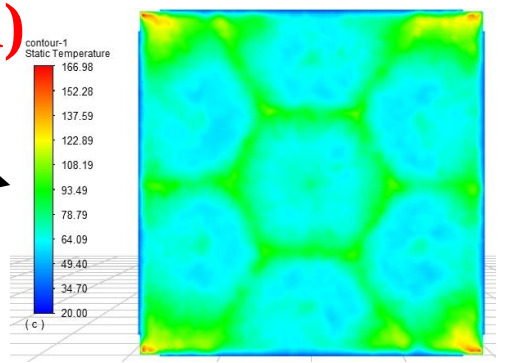


More Uniform temperature distribution was noted in optimized fin geometry.

CFD Results and Mesh Independency

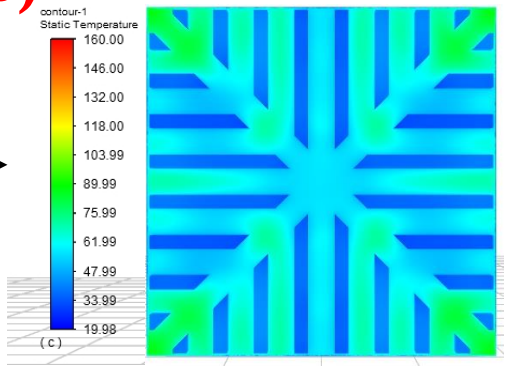
Grid Sets	1	2	3
Elements	442,798	1,030,314	1,807,942
Nodes	82,315	180,530	349,501
Orth Quality	0.77604	0.76804	0.76026
Avg Static temp ($°C$)	78.20356	73.20950	73.08878

(a)



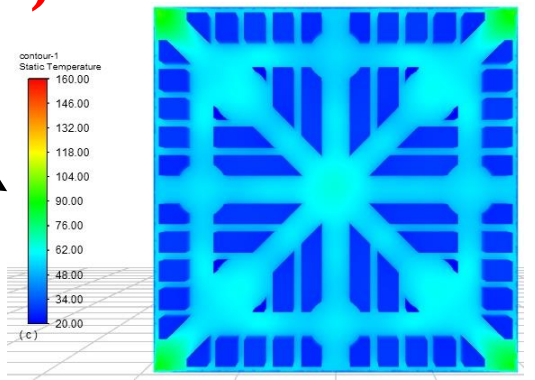
Grid Sets	1	2	3
Elements	514,909	1,114,470	2,185,532
Nodes	93,605	212,858	393,715
Orth Quality	0.74623	0.75356	0.75622
Avg Static temp ($°C$)	56.3876	51.93421	51.50636

(b)



Grid Sets	1	2	3
Elements	522,418	1,095,078	2,171,661
Nodes	95,444	197,943	403,200
Orth Quality	0.738	0.74583	.75007
Avg Static temp ($°C$)	40.56199	38.22699	38.1179

(c)



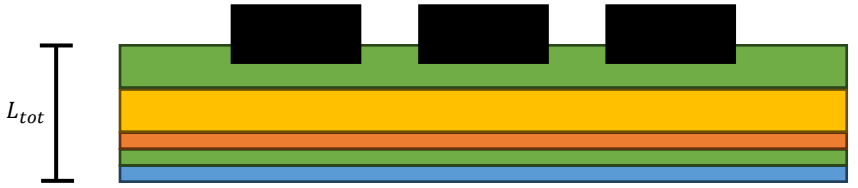
- **Conclusion:**
  - The open Fin array proved to have the most optimized arrangement for heat removal.

GaN Device Modeling and Validation

❑ Modeling GaN Device:

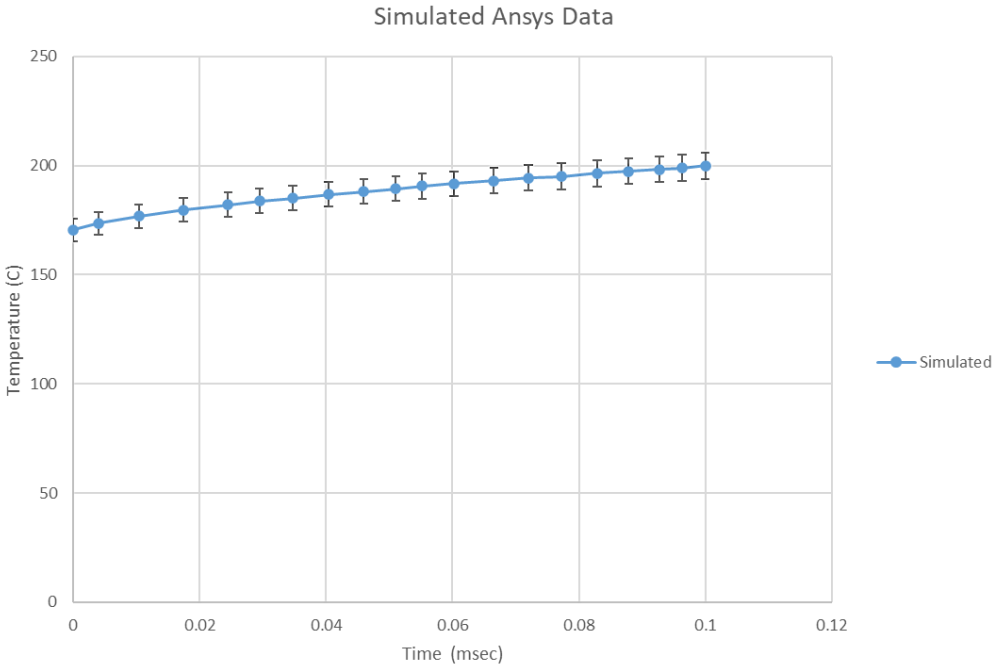
$$C_{p\,mix} = \frac{m_1}{m_{mix}} C_{p1} + \frac{m_2}{m_{mix}} C_{p2} + \frac{m_n}{m_{mix}} C_{pn} \quad \text{(eq 1)}$$

$$k_{eff} = \frac{k_1 k_2 k_n L_{tot}}{L_1 k_2 k_n + L_2 k_1 k_n + L_n k_1 k_2} \quad \text{(eq 2)}$$

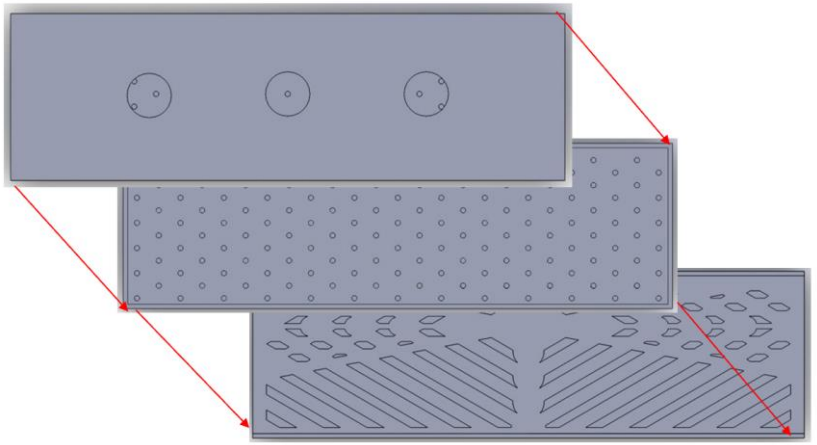


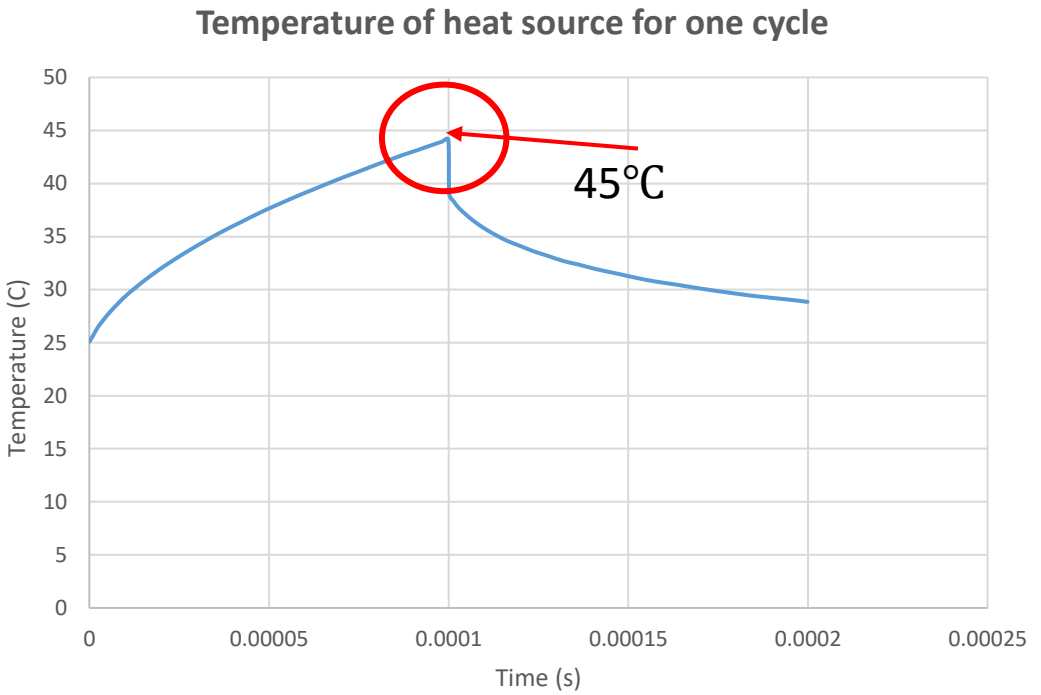
Schematic of Physical System

- The only boundary conditions were **initial temperature of the system of 100 °C** and the **heat flux** which is proprietary information.
- The resulting data was validated using the data provided from MACOM, which has a maximum of 3% deviation with the data provided by MACOM (not shown on graph as it is proprietary information).



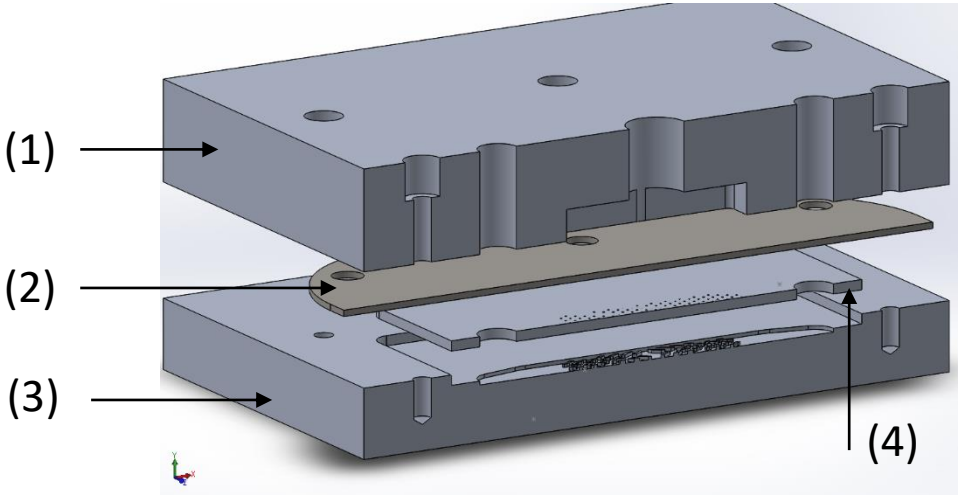
Modified UJI-TMS Design based on Parametric Study



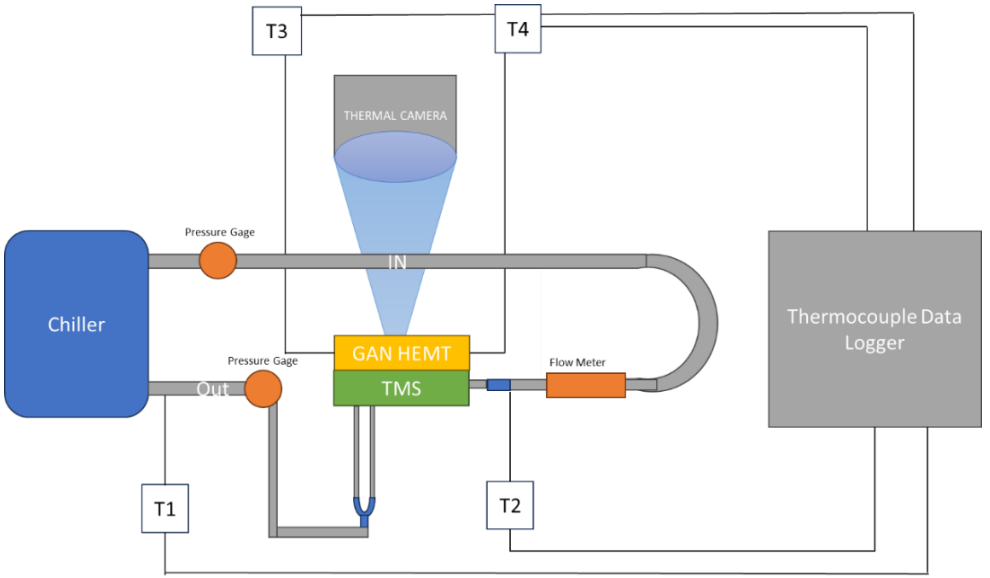


Achieved Results	
Heat rejection rate from the fins	15,725 W/m^2-K
Heat transfer coefficient	10,251 W/K-m^2
Heat source surface overall temperature rise during one cycle	4°C

Experimental Validation



- **Cross-Sectional view of the current UJI-TMS geometry:**
  - (1) The top plate with outlet and inlet to the chiller;
  - (2) The Silicone sheet to stop fluid from leaking;
  - (3) The enhanced heat sink with fins;
  - (4) The nozzle plate that sits into the heatsink.

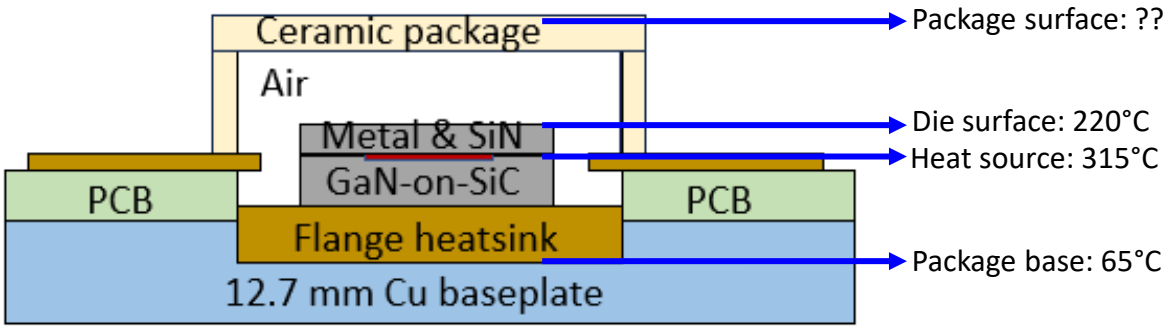


Experimental Configuration

Experimental Setup: Challenges

Device Under Test

- Macom MAPC-A1500 GaN PA with an L-band evaluation board (EVB) is the DUT for the final product.
- Board modifications considered for more efficient thermal testing and evaluation:
  - Lid removal from ceramic package: to minimize thermal resistance during imaging.
  - Heatsink removal from EVB: to remove extra thermal resistance in heat removal path, which will reduce UJI-TMS efficiency.



Options available for purchase

Cu under GaN	Lid	Cost	Lead Time
0.5”	yes	$2,250	4-6 Weeks
0.5”	no	$3,600	4-6 Weeks
0.25”	no	$14,500	8-10 Weeks
0.1”	no	$22,000	9-11 Weeks

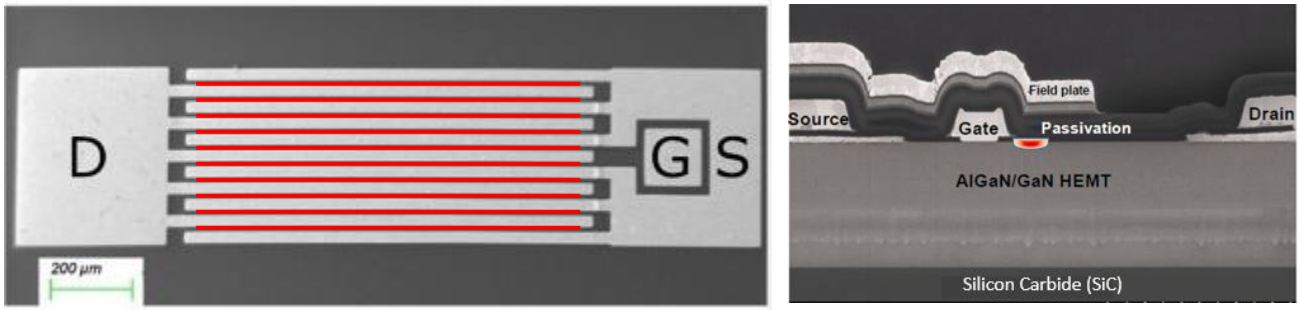
- Ordered DUTs: Standard GaN EVB with and without package lid removed.
  - Thermal measurements to establish temperature difference with package lid for future test plans.
- Lab setup for MAPC-A1500 testing ongoing:
  - 3-phase 15 kW power supply purchased for bias
  - High current electrical wiring for the lab pending

Experimental Setup: Challenges

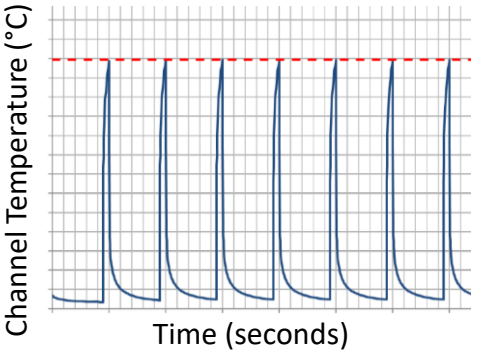
Thermal Imaging

- Transient thermal measurement is a challenge with pulsed GaN due to high spatial and temporal resolution required.

Submicron wide, nanometer deep, millimeter long hot spots

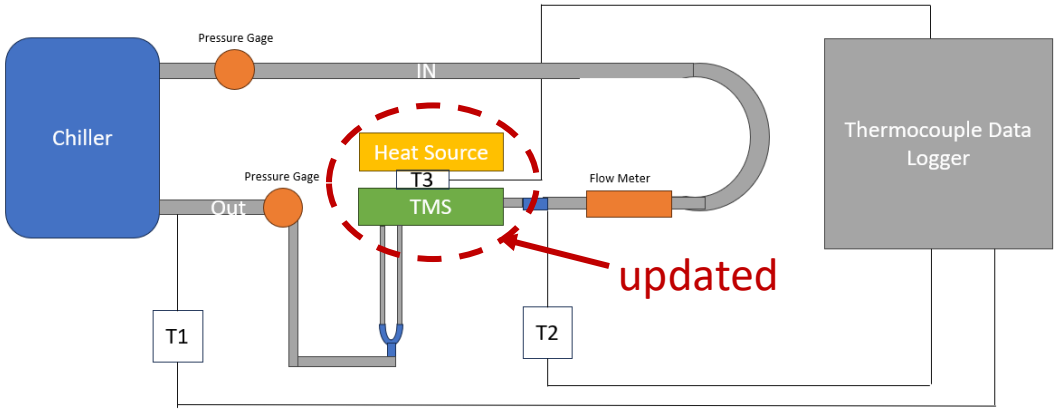


Thermal transients within 100 µs

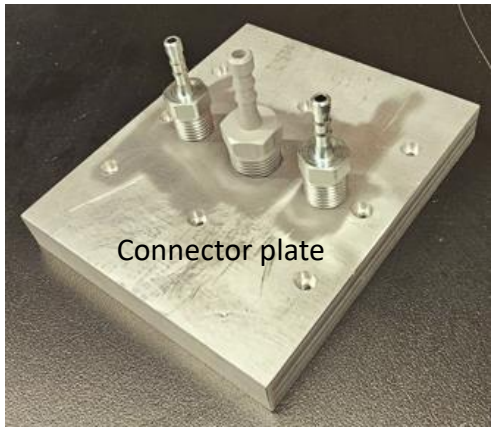


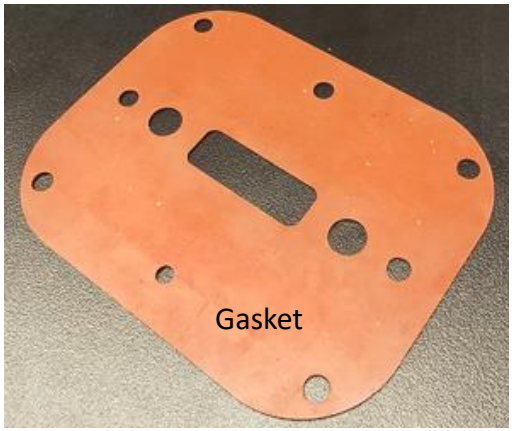
- Two thermal imaging options considered:
  - micro-Raman thermography: 0.5 µm lateral resolution but averaging in vertical direction; modifications required for nanosecond temporal resolution.
  - Infrared (IR) spectroscopy: 3 -5 µm spatial resolution; sub-100 µm temporal range possible.
- Both options cost > $150k; no funding available currently
- Demo unit for a down selected IR camera will be available in 2 months and can be used in initial thermal measurements.

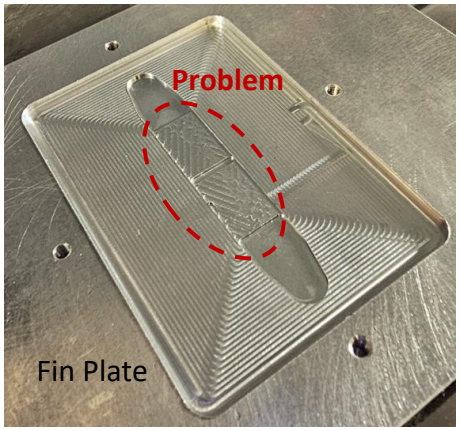
Revised Experimental Plan



- A **constant heat source** will be used in initial proof-of-concept experiments.
- Thermal imaging will be done with a thermocouple between heat source and TMS.
- Initial proof-of-concept testing is pending prototype fabrication and will provide heat rejection rate of UJI TMS and the temperature of the target surface, from which the **GaN duty cycle** can be approximated.







- GaN PA testing for increased PW/DC with TMS on-hold until an IR camera is available.

Journal Publications

In Preparation

- Sisk, S., Berber Halmen, F. and Sobhansarbandi, S., Design/Development of an Ultra-Compact Jet Impingement Thermal Management System Integrated With Micro-Fins for High Power Applications: A CFD Modeling and Experimental Cross-Validation. In ASME Power Applied R&D 2023. American Society of Mechanical Engineers Digital Collection for International Journal of Thermal Sciences, In preparation, 2023.

Conference Publications

- Sisk, S., Berber Halmen, F. and Sobhansarbandi, S., Design/Development of an Ultra-Compact Jet Impingement Thermal Management System Integrated With Micro-Fins for High Power Applications: A CFD Modeling. In ASME Power Applied R&D 2023. American Society of Mechanical Engineers Digital Collection [doi].

Conference Presentations

- Sisk, S., Dhungana, S., Berber Halmen, F. and Sobhansarbandi, S., Performance Enhancement of GaN Power Amplifier through Integration of an Ultra-Compact Thermal Management System Integrated with Micro-Fins: A CFD Modeling and Experimental Study. In Directed Energy Professional Society (DEPS). November 13-16, 2023, Monterey, CA.

- Sisk, S., Berber Halmen, F. and Sobhansarbandi, S., Design/Development of an Ultra-Compact Jet Impingement Thermal Management System Integrated With Micro-Fins for High Power Applications: A CFD Modeling. In ASME Power Applied R&D 2023. American Society of Mechanical Engineers Digital Collection [doi] (**2nd best paper award**).

- Sisk, S., Berber Halmen, F. and Sobhansarbandi, S., Performance Enhancement of GaN Power Amplifiers by an Ultra-Compact Integrated Thermal Management System. In Directed Energy Professional Society (DEPS). April 3-6, 2023, San Antonio, TX.

Personnel

PI: Sarvenaz Sobhansarbandi, Ph.D.

Co-PI: Feyza Berber Halmen, Ph.D.

Graduate Research Assistant: Samual C. Sisk responsible for design and development of multi pronged UJI-TMS in alignment with SWAP-C2 constrained PTERA platform

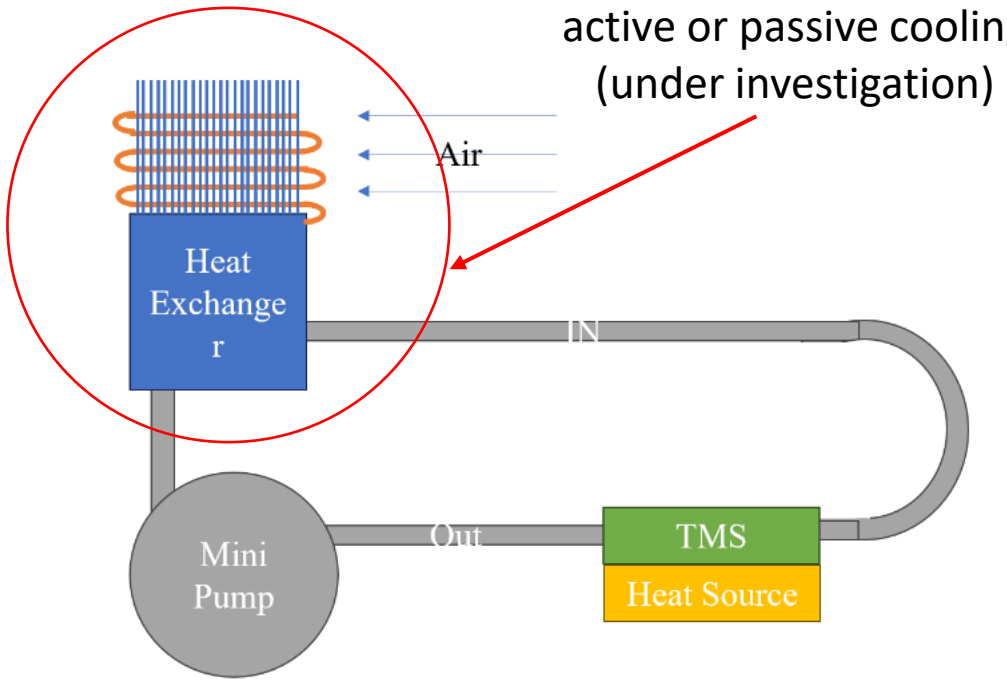
Post Doctoral Assistant: Shailesh Dhungana, Ph.D. provides support in terms of applicability of proposed ideas to PTERA mission and system testing

Summary

- The preliminary proof of concept for the integration of fin and one nozzle array is performed with ANSYS fluent, and the results show that such an integration improves **cooling capability by 30℃**.
- The GaN device modeling was **validated** within 3% of MACOM propriety data.
- Further design optimization of the nozzles and fin array resulted in a **heat transfer coefficient of 10 kW/K-m^2**.
- The **full-scale design** with optimized metrics of the nozzles/fins arrangements is being prototyped and will be tested experimentally under the said boundary conditions.
- The results from experimental analysis will provide heat rejection rate of UJI-TMS and the temperature of the target surface, from which the **GaN duty cycle** can be approximated.

The UJI TMS is being **re-designed** to meet the **PTERA SWAP** requirements under PTERA II.

Proposed Design 1 (Sep. – Dec. 2023)



Schematic of UJI-TMS

- Phase II involves miniaturization of UJI-TMS auxiliary components to achieve a cooling system within PTERA size and weight requirements.
- A **mini pump** (weight: <500g / size: 11 x 9.8 x 9 cm) that can provide the required heat removal capability is already identified.
- Various options for **miniaturized heat exchanger** is being investigated.

Thank you for your attention!

For any questions, please contact:

sarvenaz@umkc.edu

feyza.berberhalmen@umkc.edu

MACOM

Partners from RF to Light

Pulse Tactical Effector for Regulated Attack

Enabling Cyber Capabilities

PTERA Grant Annual Review

October 10, 2023

Funding provided by ONR under grant N00014-22-1-2385

Mostafizur Rahman rahmanmo@umkc.edu

Objectives

Mission Objectives:

Intelligent electronic warfare/offensive cyber operations on the edge using Field Programmable Gate Array (FPGA) devices

- Brain for cyber offensive; automated intelligent decision making without internet/back-end support
- Mitigate data transfer bottleneck from the field to command center
- Remote erasure/destruction of hardware codes

Technical Objectives:

- IP Cores to be used for Neural Network implementation in FPGAs
- FPGA interface with drone host controller
- Integration of military dataset with open-source glow compiler for task partitioning and machine level code generation
- Remote programming & erase of the FPGA from back-end server

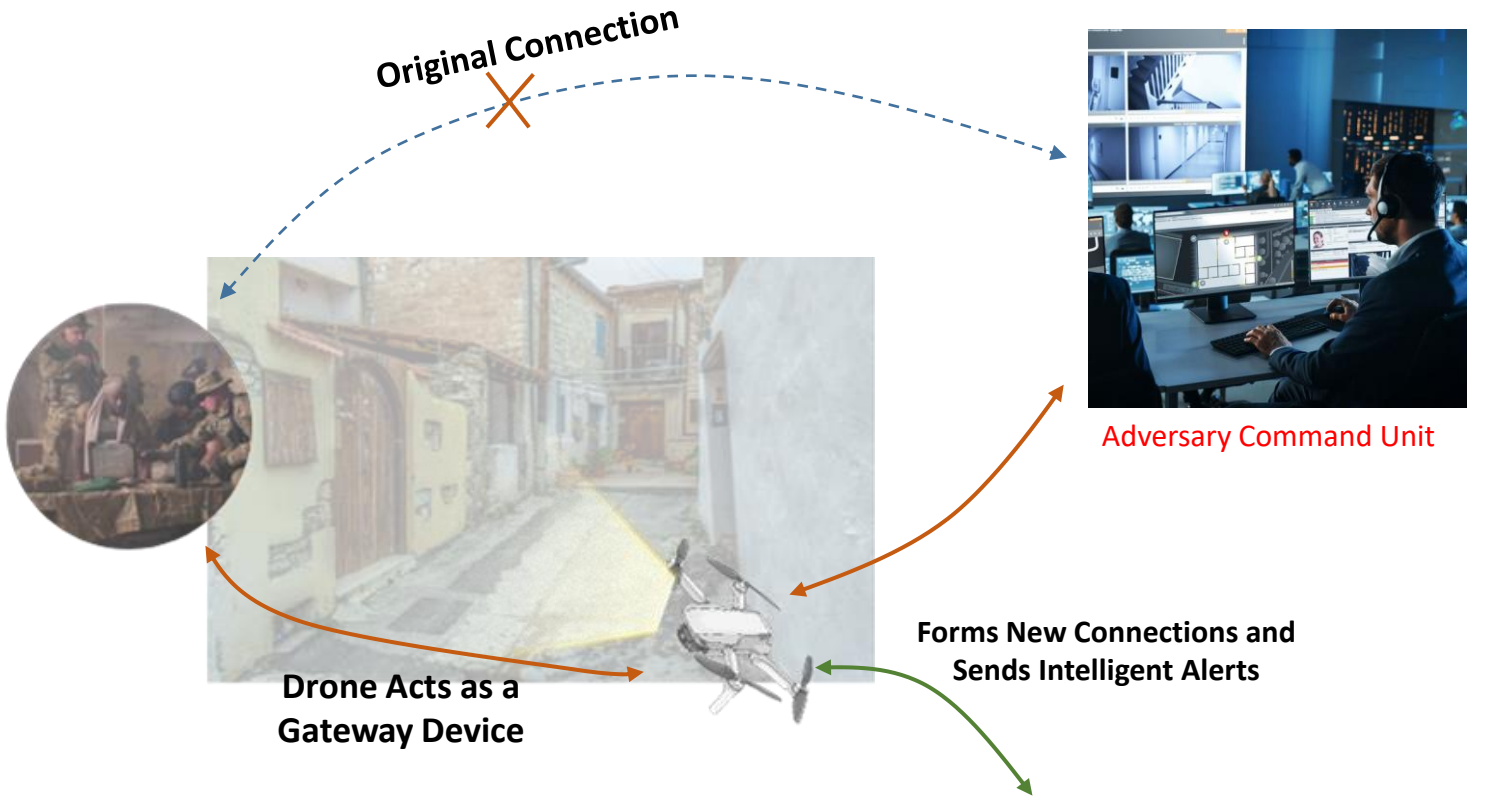
Vision

Behind the wall EM signal detection & identification

- Detect all active wireless devices that are connected through wifi
- Determine identifying information (device type, IP, signal strength, activity, etc.)
- Hack into the network and eavesdrop on all the packets
- Analyze packets and find suspicious behavior

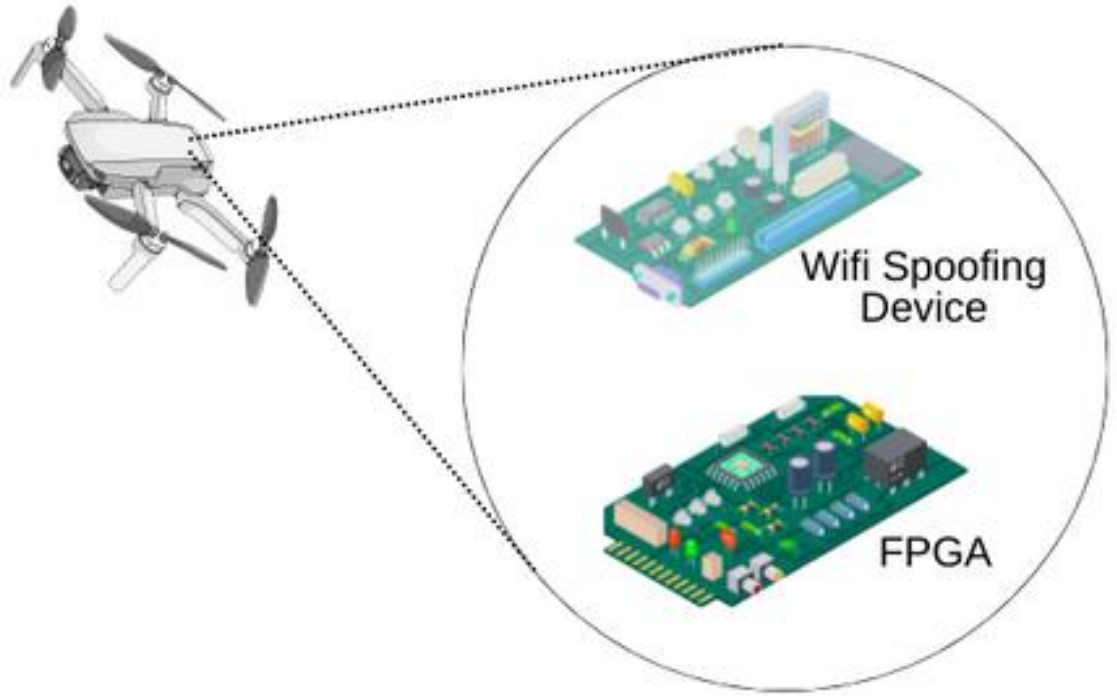
Wifi Spoofing and Detection

Man in the Middle Attack



- PTERA drone to act as a gateway device (middleman) between victim and receiver
- Eavesdrop on all the packets and identify suspicious activities

System Overview

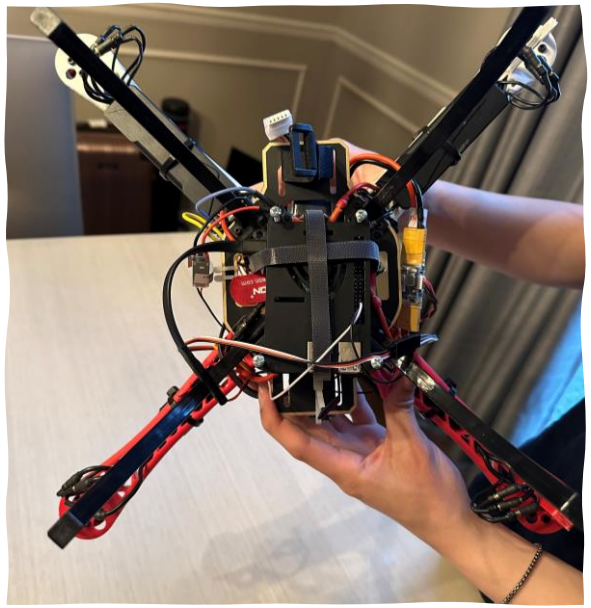


<u>Inside the hood</u>

2 devices: Wifi Spoofing hardware and FPGA board

- The spoofing board will be used to hack into the wifi and retrieve packets
- The FPGA board will analyze the packets through machine learning approaches
  - FPGAs (programmable chips) for machine learning

Wifi Spoofing on a Simulated Environment (2022-23 UG Senior Design Project with Dr. Abdesselam)

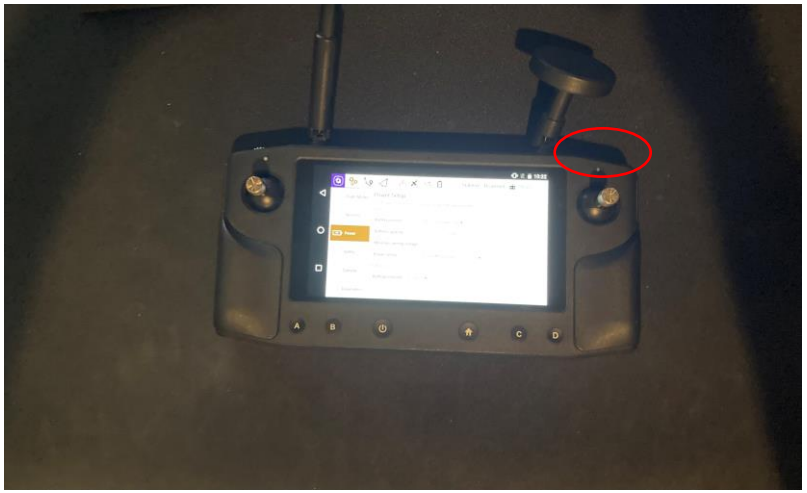


Bottom view
(Raspberry Pi attached to bottom)

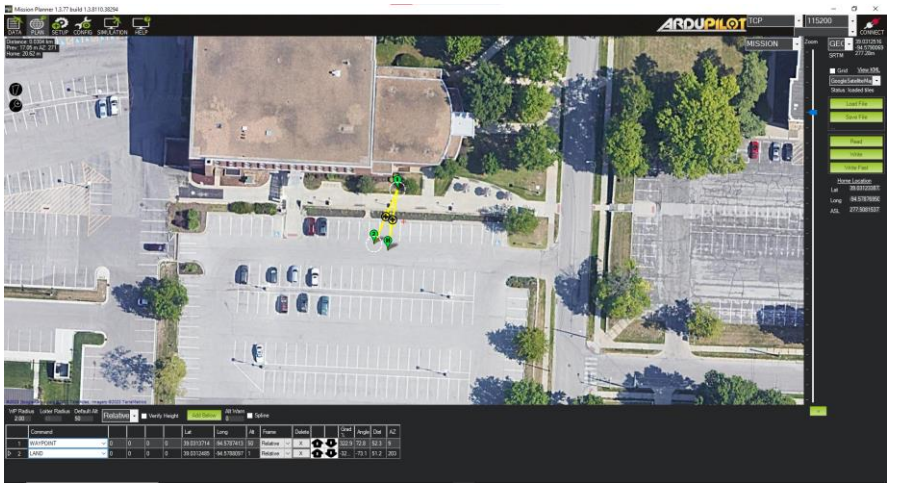
Top View
(Arduino Nano circled in red)

Side View

Wifi Spoofing on a Simulated Environment (2022-23 UG Senior Design Project with Dr. Abdesselam)



Remote Control
(Button to Trigger Wifi-spoof in red circle.)



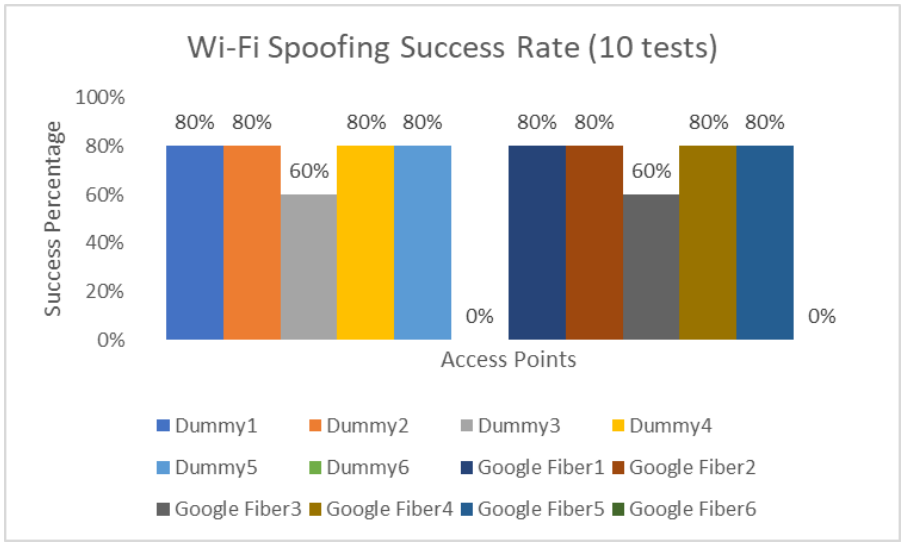
Flight plan to that remote control has.
(education building)

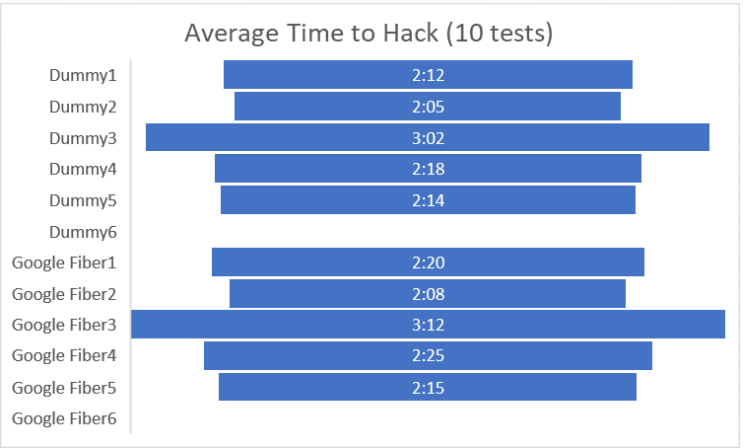
Wifi Spoofing on a Simulated Environment (2022-23 UG Senior Design Project with Dr. Abdesselam)

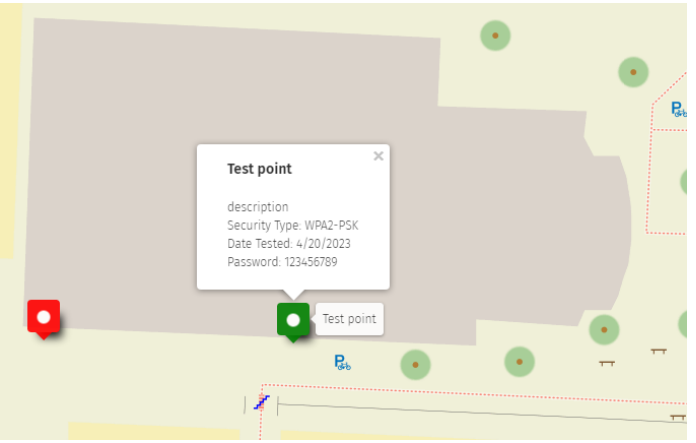
Intelligent electronic warfare/offensive operations on the edge using programmable devices

- Mitigate data transfer bottleneck from the field to command center
- On demand intelligent decisions at the edge

Wifi Spoofing on a Simulated Environment (2022-23 UG Senior Design Project with Dr. Abdesselam)

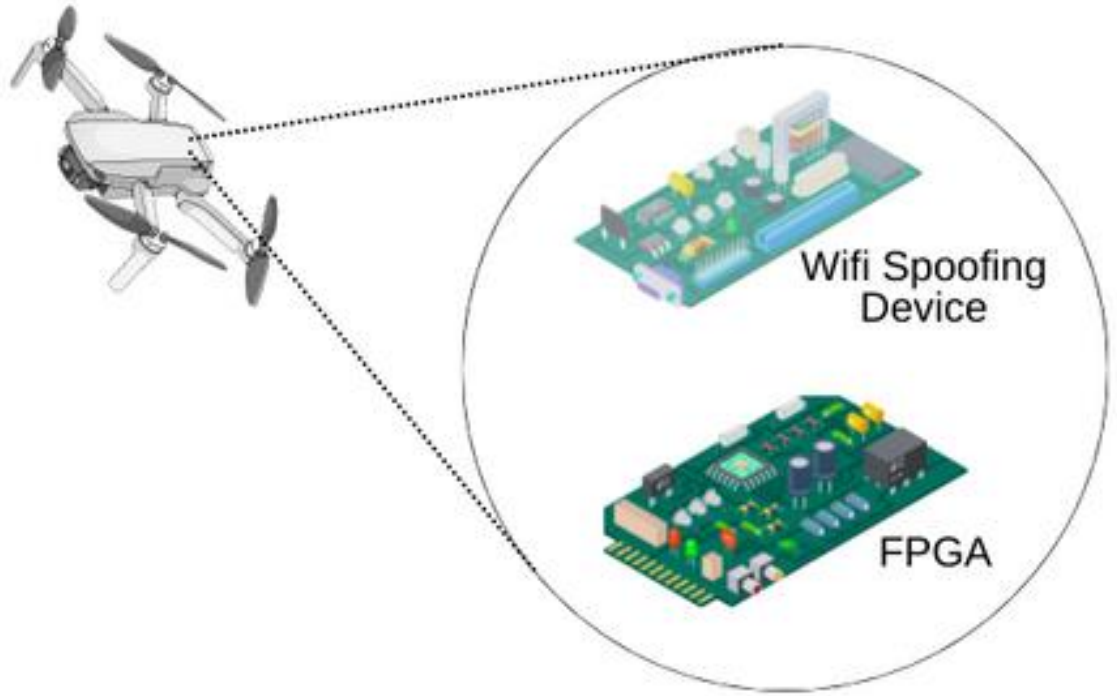






UMAP overlay for test point description.

Revisiting the System

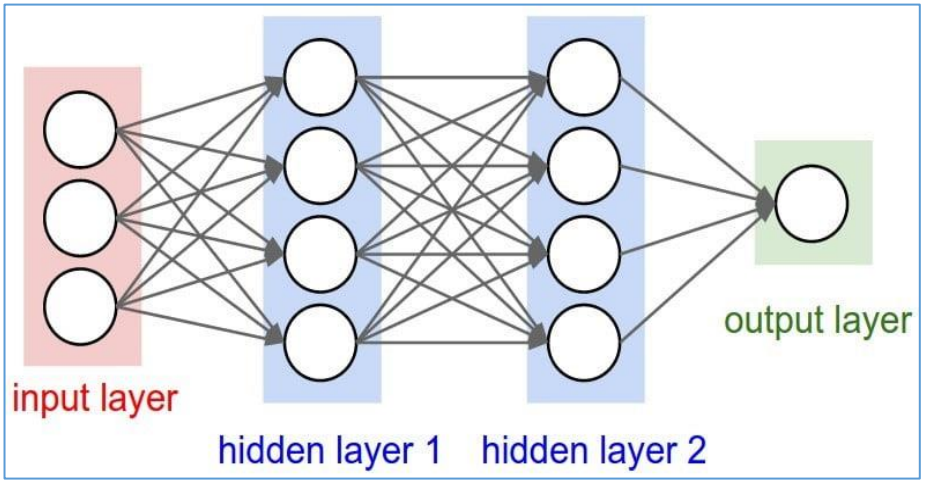


Inside the hood

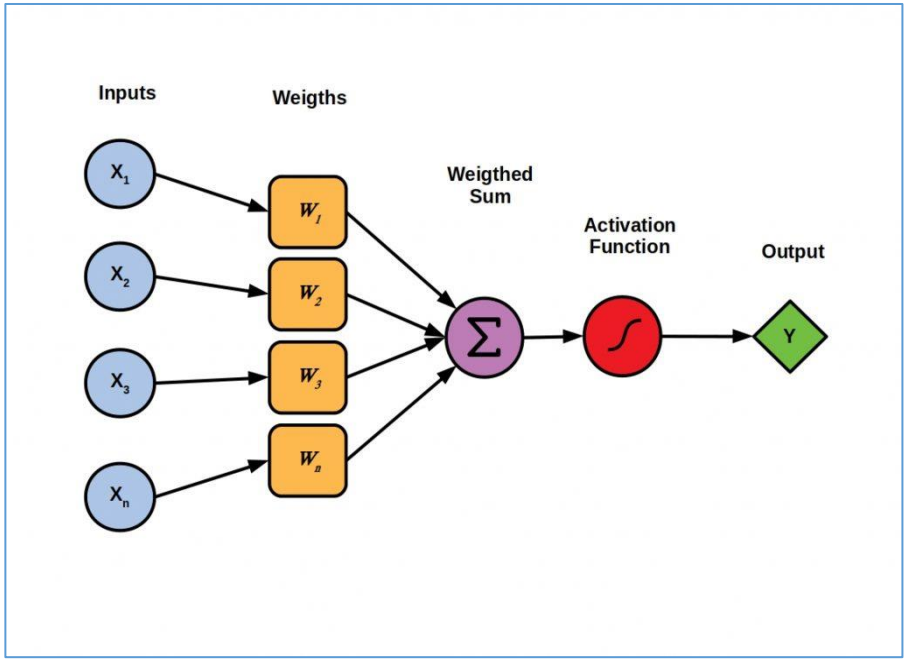
2 devices: Wifi Spoofing hardware and FPGA board

- The spoofing board will be used to hack into the wifi and retrieve packets
- The FPGA board will analyze the packets through machine learning approaches
  - FPGAs (programmable chips) for machine learning

Our Focus



Neural Network (Abstract)

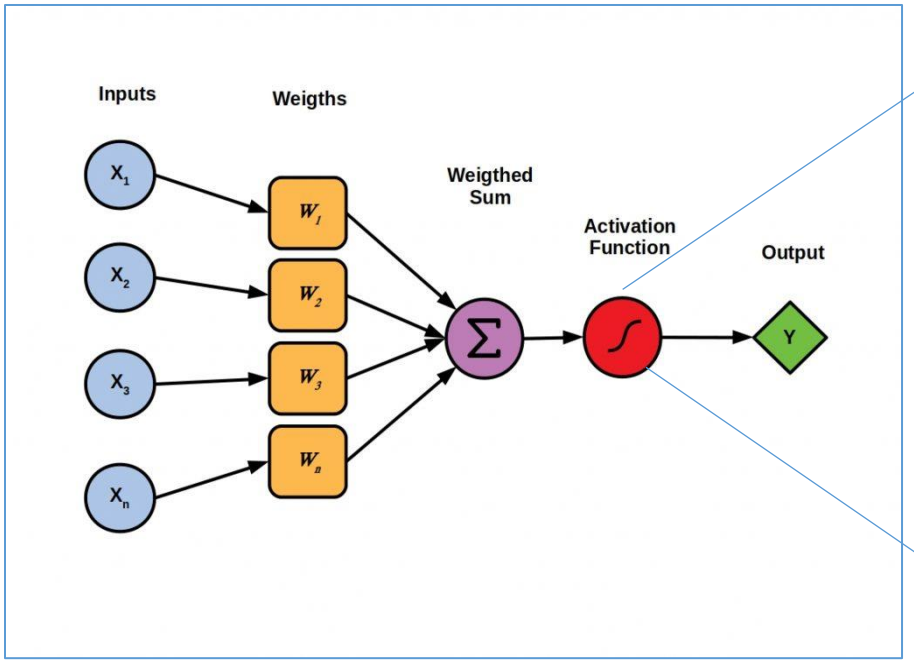


Neural Network (Operations)

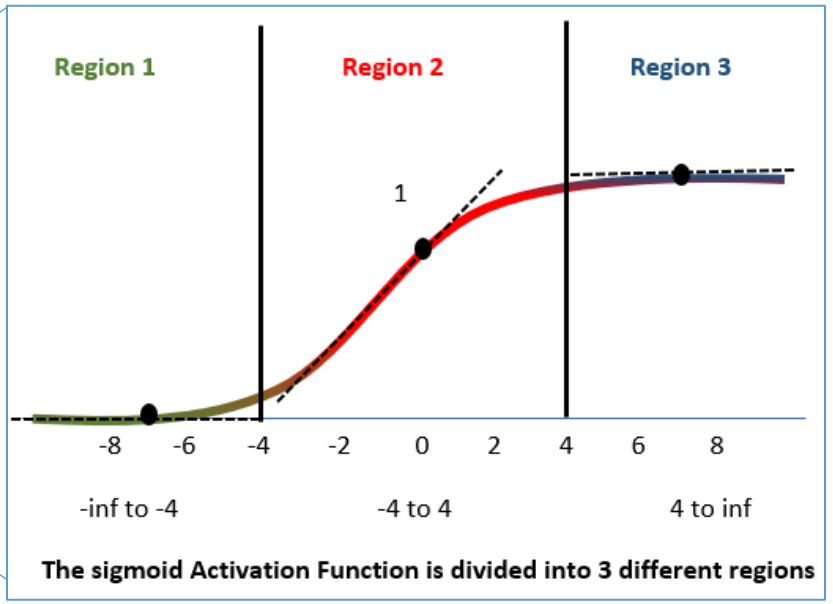
Questions we are seeking to answer

- How to implement core computing blocks?
- How to interface with the software?
- How to map select neural network on to the FPGA chip?

Implementation of Core Blocks



Neural Network (Operations)



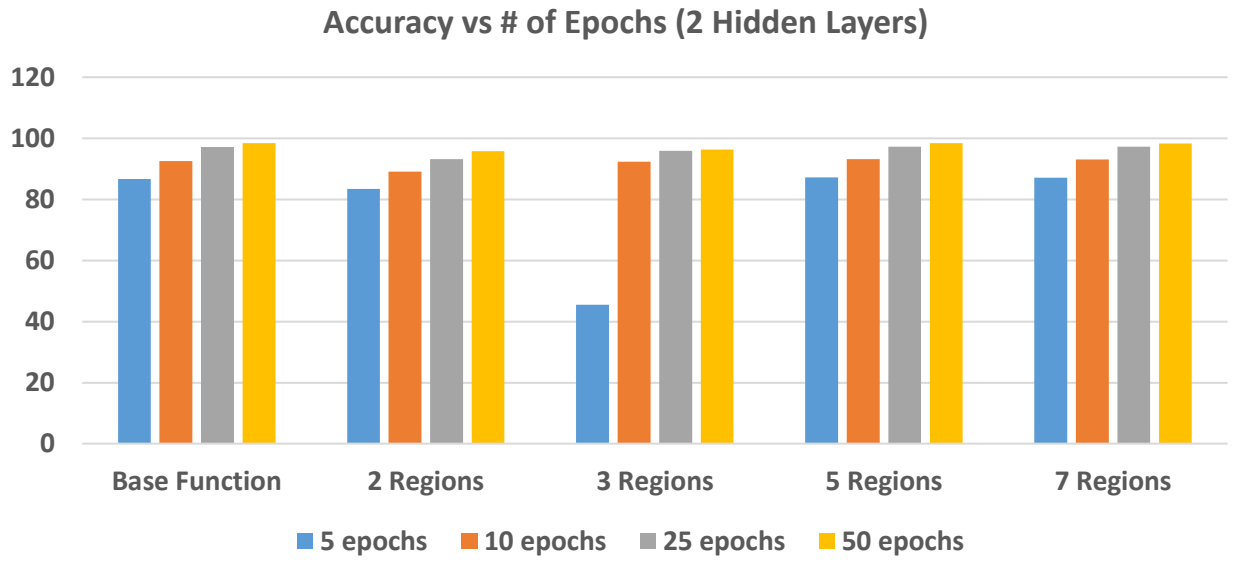
Sigmoid Activation Function

Typical operations in a neural network that the accelerator hardware should perform are: multiplication, addition, and activation

-Activation is a non-linear function $$S(x) = \frac{1}{1+e^{-x}} = \frac{e^x}{e^x+1} = 1 - S(-x).$$

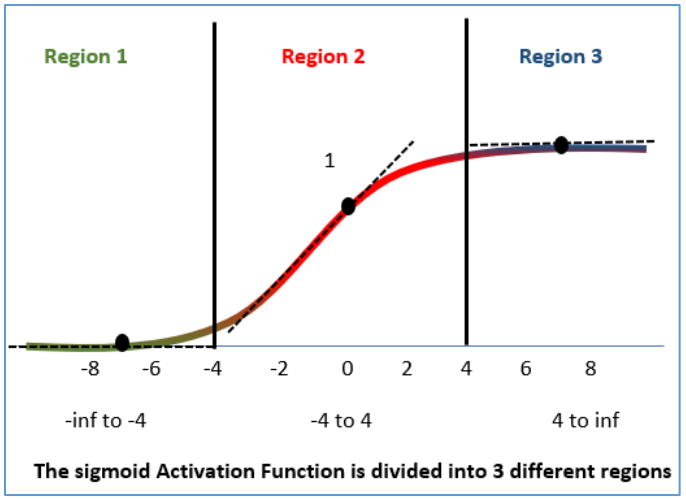
Our approach: *linear approximation*

Accuracy vs. Epochs (2 Hidden Layers)

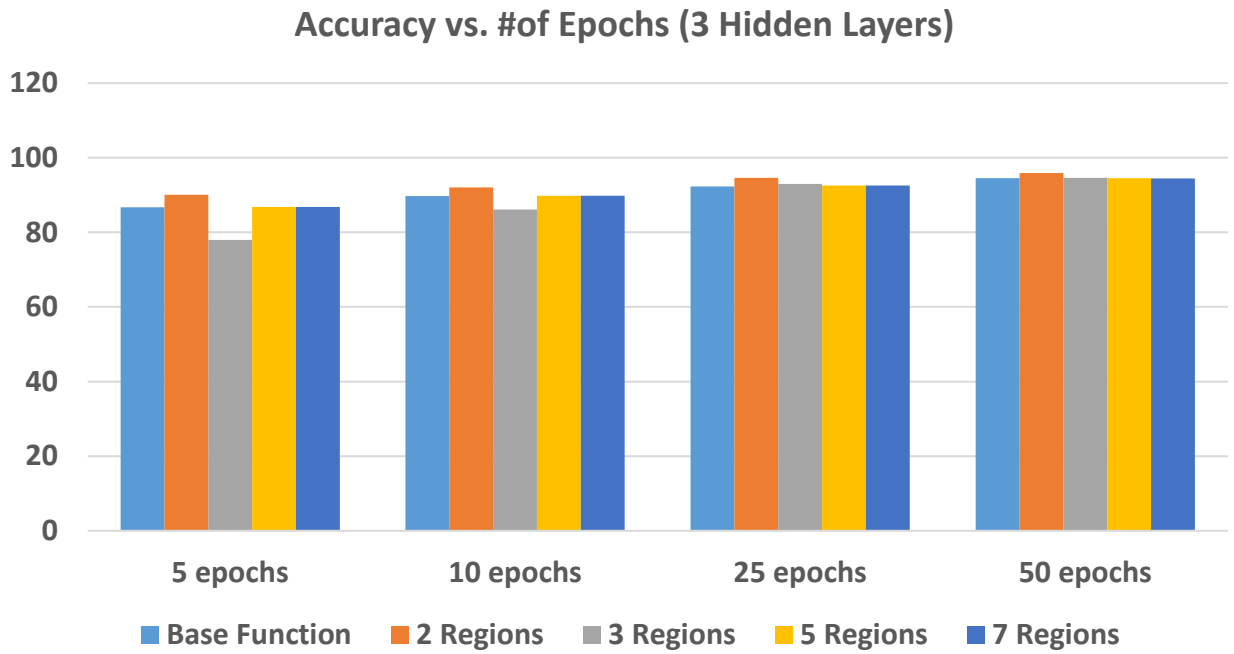


The linear approximation was emulated in software to determine effectiveness prior to burning on the FPGA chip

- With more epochs and higher number of regions the results are within 0.05% accuracy of the base function

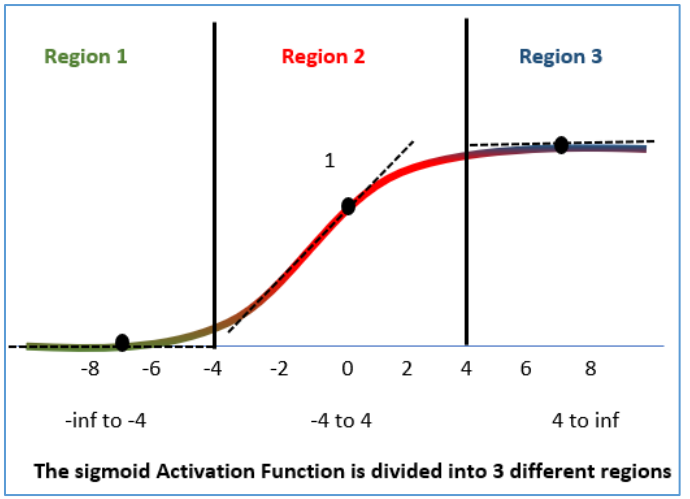


Accuracy vs. Epochs (3 Hidden Layers)



For larger networks, the trend seems to continue

- Linear approximation is in good agreement with the original Sigmoid function



Edge Machine Learning Framework

FPGA/RPI4 as Custom Accelerator

SN74LS157N MUX

AT45D321E External Memory

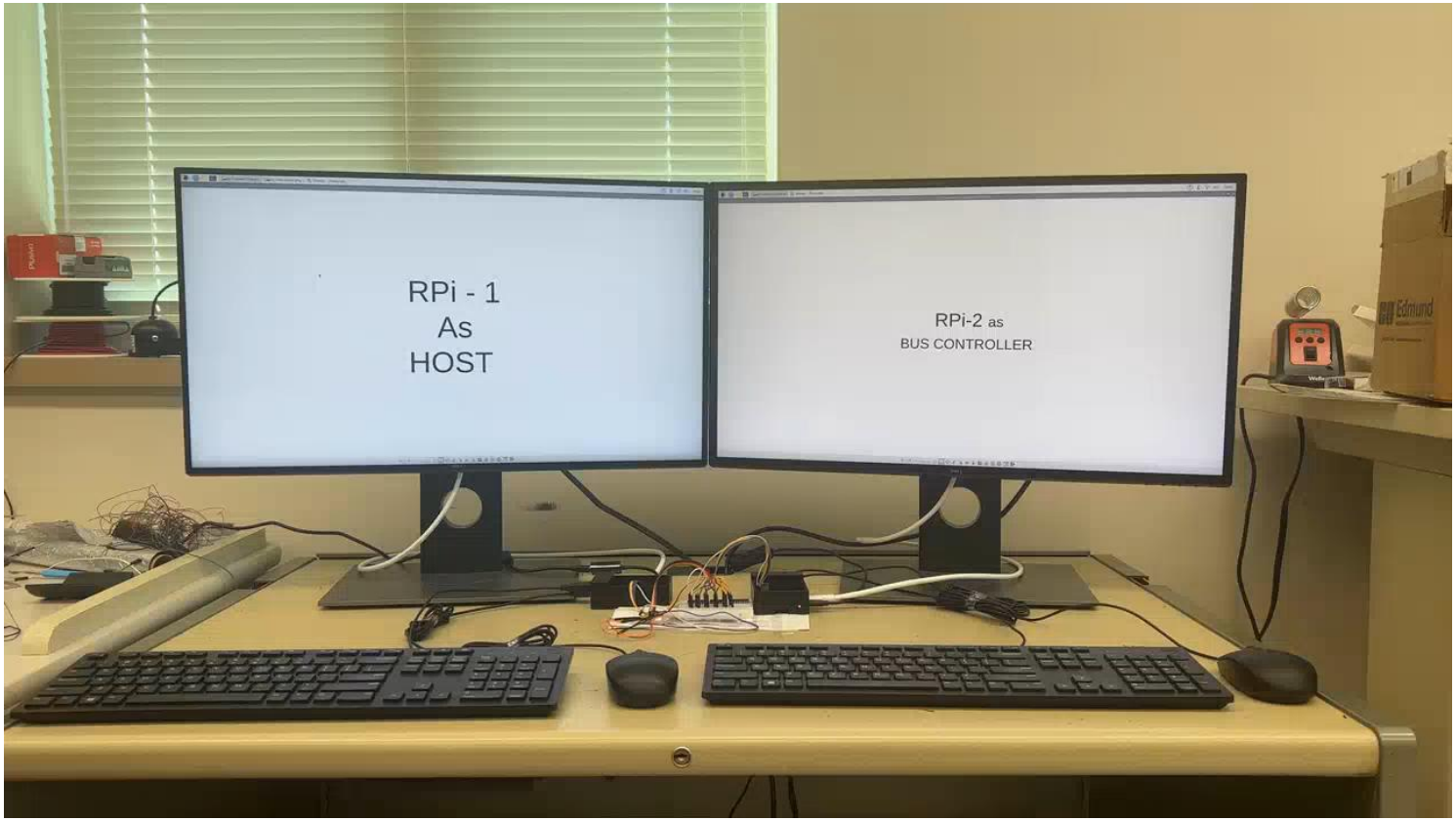
RPI4 as Bus Controller

Multi-Protocol Interface

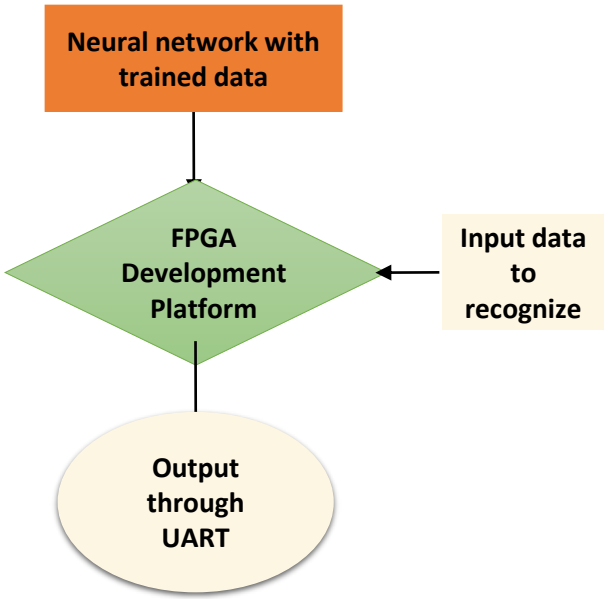
Our Driver

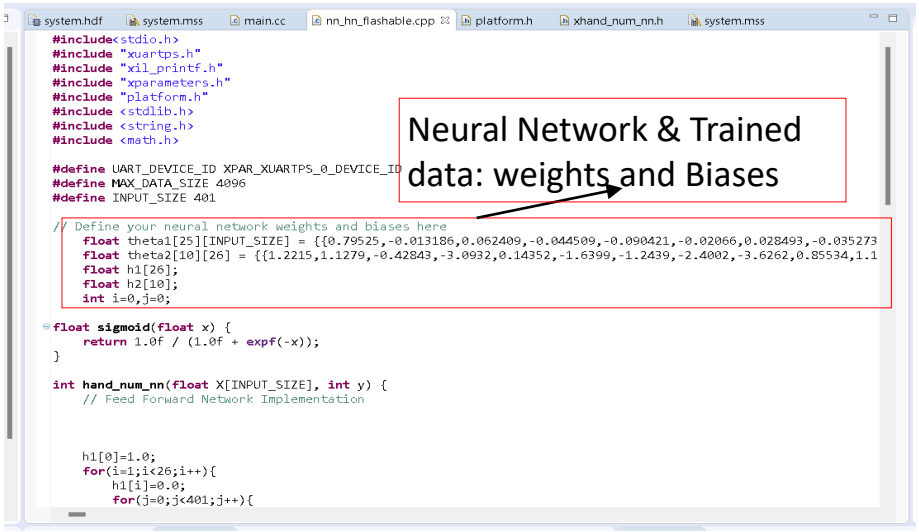
HOST Device

Demo of Linux/Win Driver + Protocol Control



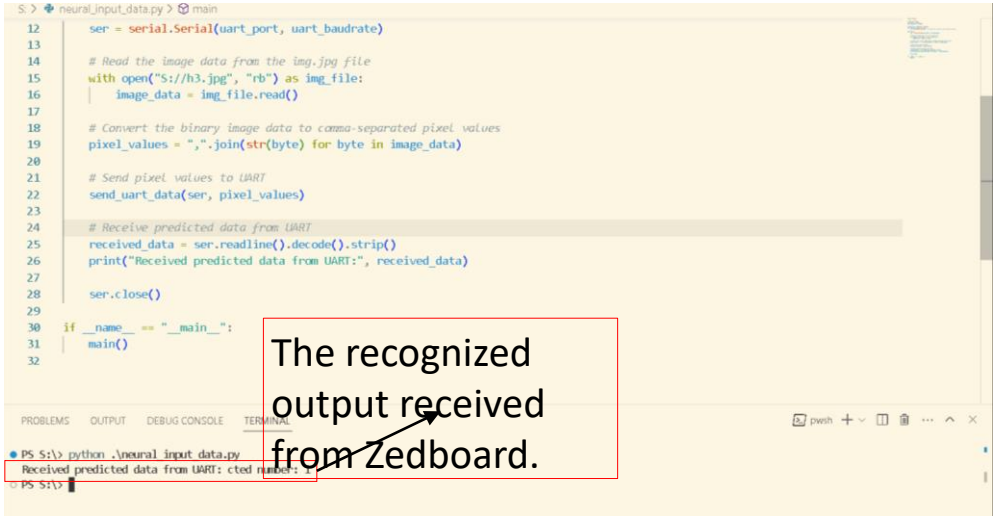
Neural Network Demo on FPGA





The steps involved for running a neural network is shown below-

1. The neural network with trained data will be flashed into the ZedBoard.
2. Input data will be sent to the ZedBoard through UART to recognize the images.
3. The input will be given through python code which is enabled for UART serial communication; the driver will convert the data to Binary data
4. The binary data will be sent through UART to the ZedBoard and recognizes the data.
5. Once it recognized, the ZedBoard will send the output through UART.

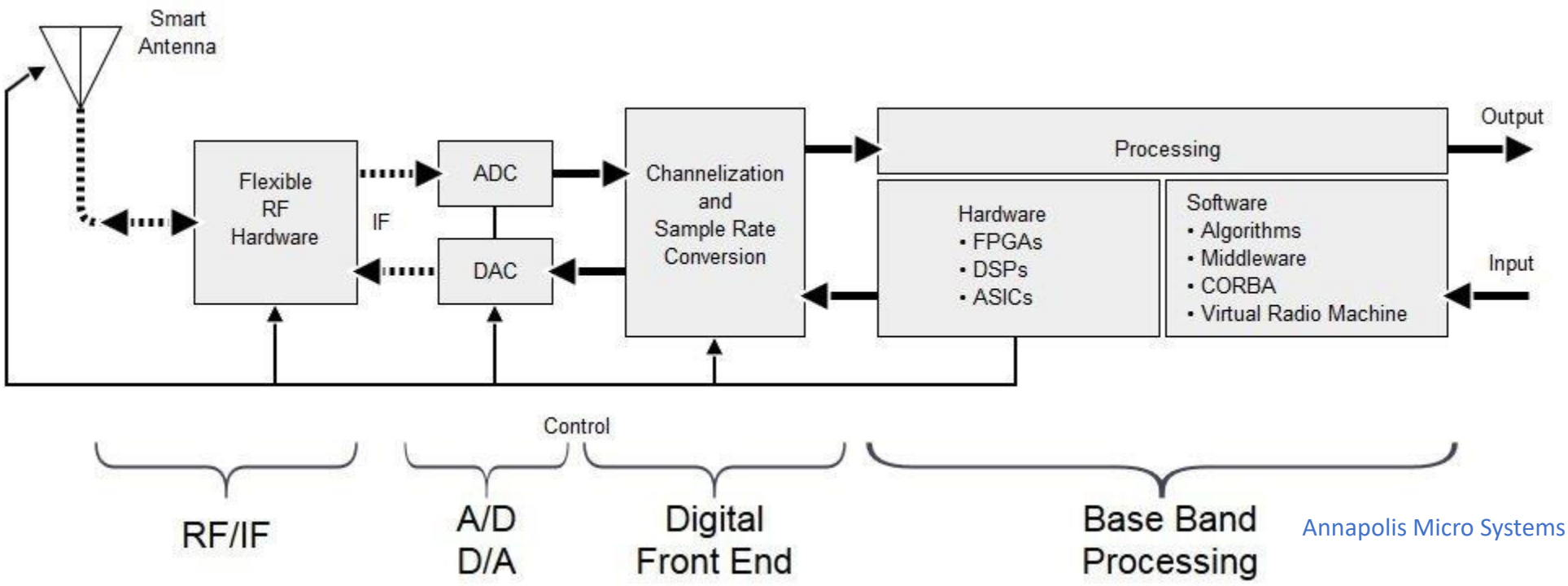


Future Work

Detect signal of interest in real time

- Edge hardware is generic and can perform any ML tasks as long as the data is ready
- Accelerator performance is heavily dependent on input data bandwidth
- RF signal of interest can have a wide range
- Dealing with many different RF signal for classification can be challenging
  - De-noising interesting data
  - Preparing it for machine learning

A Combined SDR and Accelerator

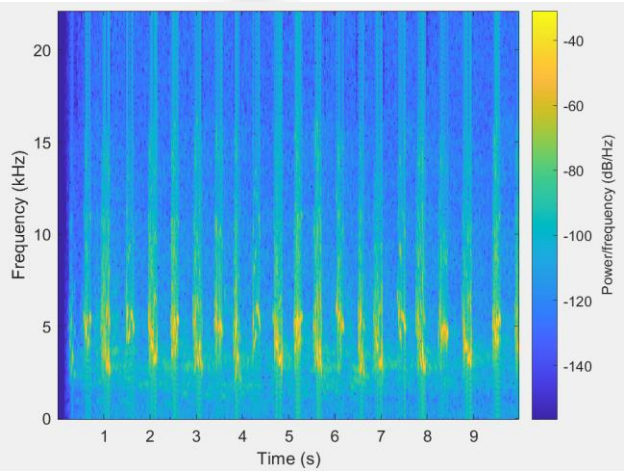


Annapolis Micro Systems

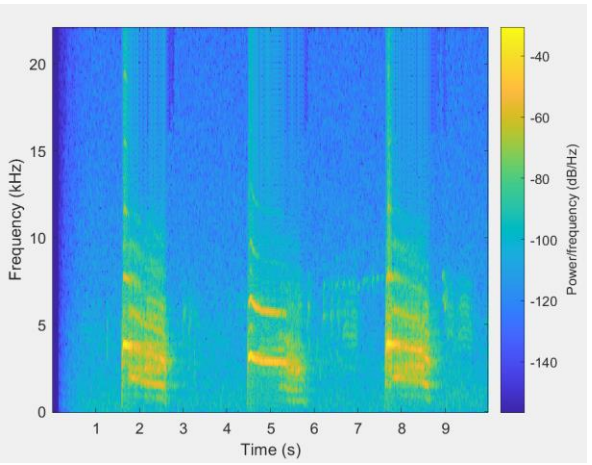
- A SDR stores data as a grid in memory after digitization
- A custom hardware/FPGA processing unit performs inference on the data

Bird Sounds as Examples

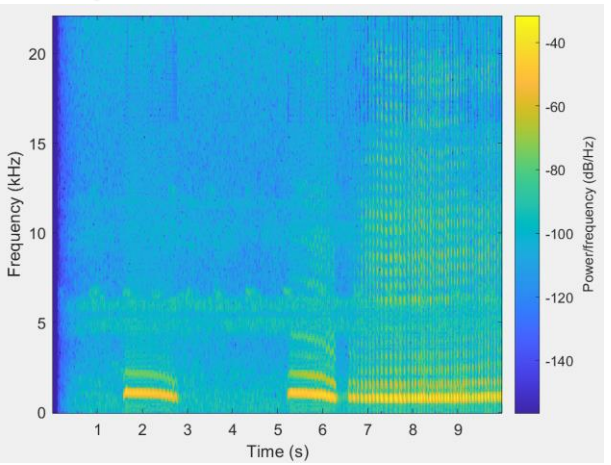
Sparrow



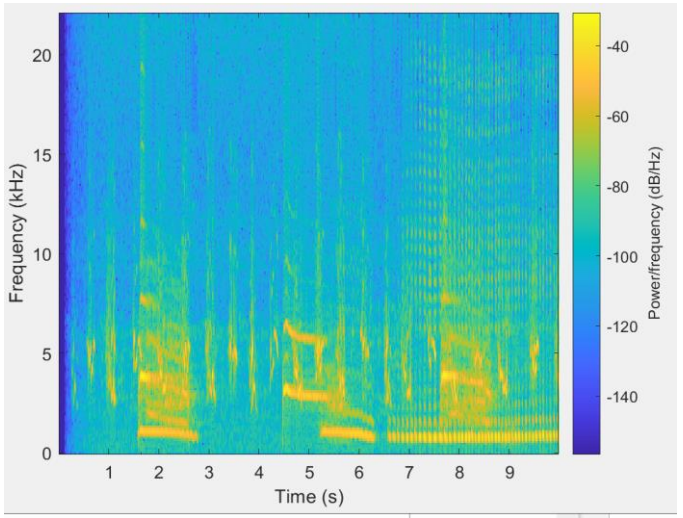
Red Tail Hawk



Eastern Screech Owl



Mix of Signals



Applying Convolution Filters on Spectrogram Images

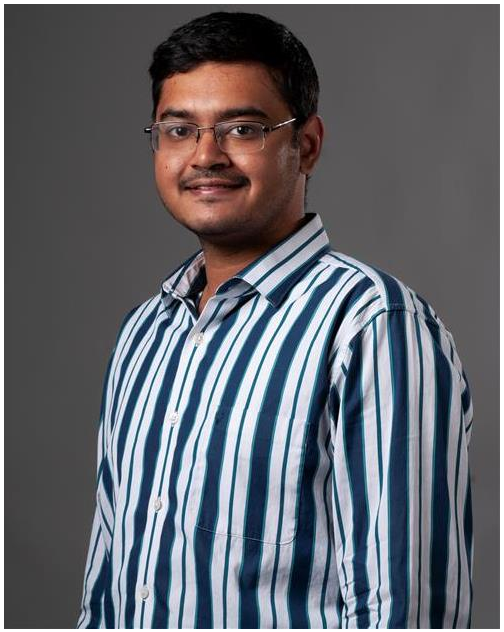
Y gradient filtering to separate Screech Owl Sound

- Convolution layers can be applied to separate out/classify signals of interest
- Signal logger to keep track of signal origins
- Combined SDR, Accelerator architecture can bridge data bottleneck gaps and pave way for real time mass signal classification

Personnel

Dr. Mostafizur Rahman

Satya Sai S. R. K. Akula



Srinivas Rahul

Abhiram Cholleti

Sprayable Coatings for Broadband EMI Shielding

PTERA Grant Annual Review

October 10, 2023

Funding provided by ONR under grant N00014-22-1-2385

Dr. Stephan Young Stephanyoung@umkc.edu
smy899@mide.umkc.edu (CUI)
Dr. Pratish Rao prrhcf@umkc.edu

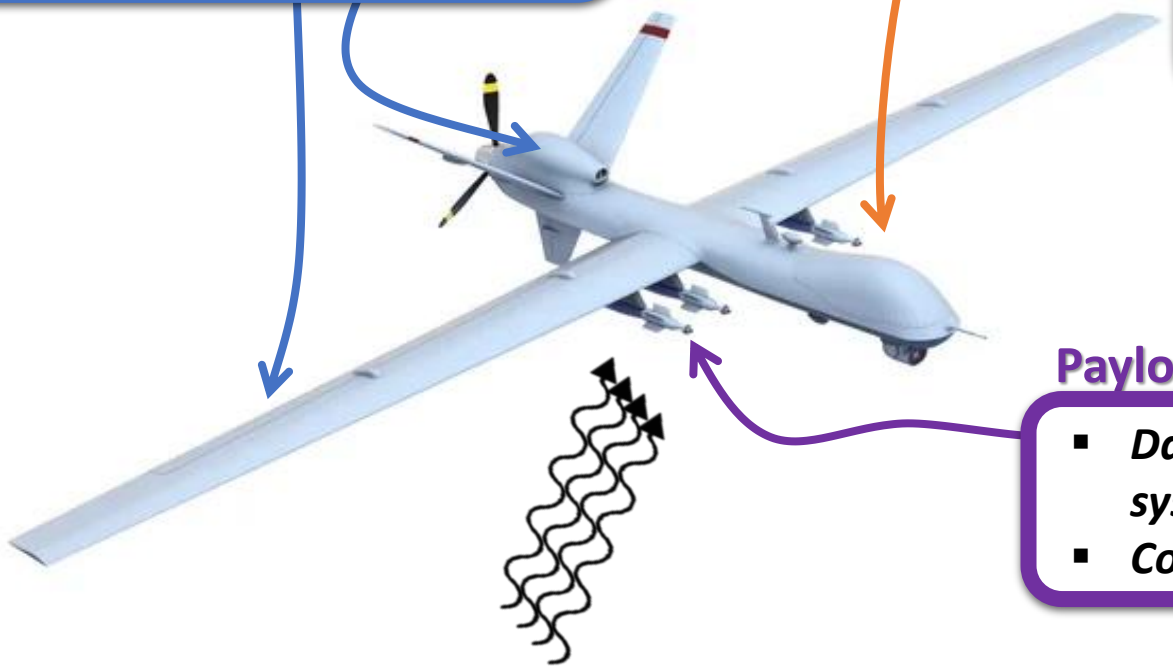
Motivation: EMI → UAS?

Flight Control Systems

- *Disrupt/destroy flight controller, sensor systems, speed controllers, propulsion systems, etc.*

Communication Systems

- *Can disrupt/destroy communication hardware*
- *Loss/delay in reception of instructions/directions*
- *Disrupt navigation*
- *Interrupt in-flight tracking*

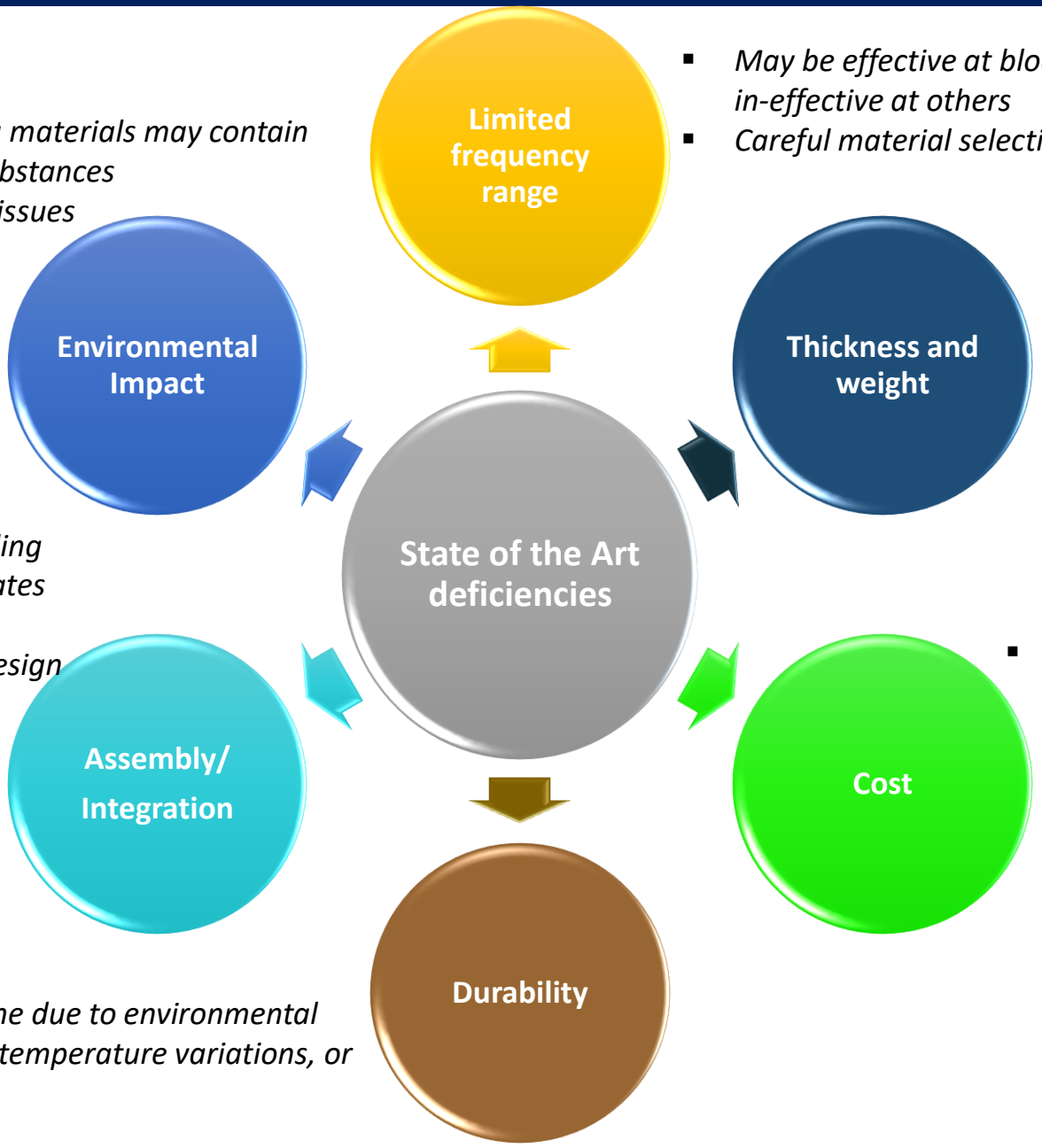


Payload

- *Damage/disrupt mission-critical systems and/or capabilities*
- *Corrupt collected data*

→ EMI can impact the success of a UAS mission

Critical Deficiencies



- *May be effective at blocking certain frequencies, in-effective at others*
- *Careful material selection needed*

- *Often requires thicker and denser materials making them heavy and bulky*

- *Engineering high-quality EMI shielding materials can be expensive, to provide shielding across a broad range of frequencies.*

- *May degrade over time due to environmental factors like moisture, temperature variations, or UV exposure*

- *Integrating EMI shielding materials onto substrates can be complex*
- *May require careful design and manufacturing processes*

- *EMI shielding materials may contain hazardous substances*
- *Recyclability issues*

Objective

→ Mitigate effects of EMI on UAS platforms of interest
→ Develop cost-effective, lightweight, broadband sprayable coatings with sufficient shielding effectiveness

Requirements:

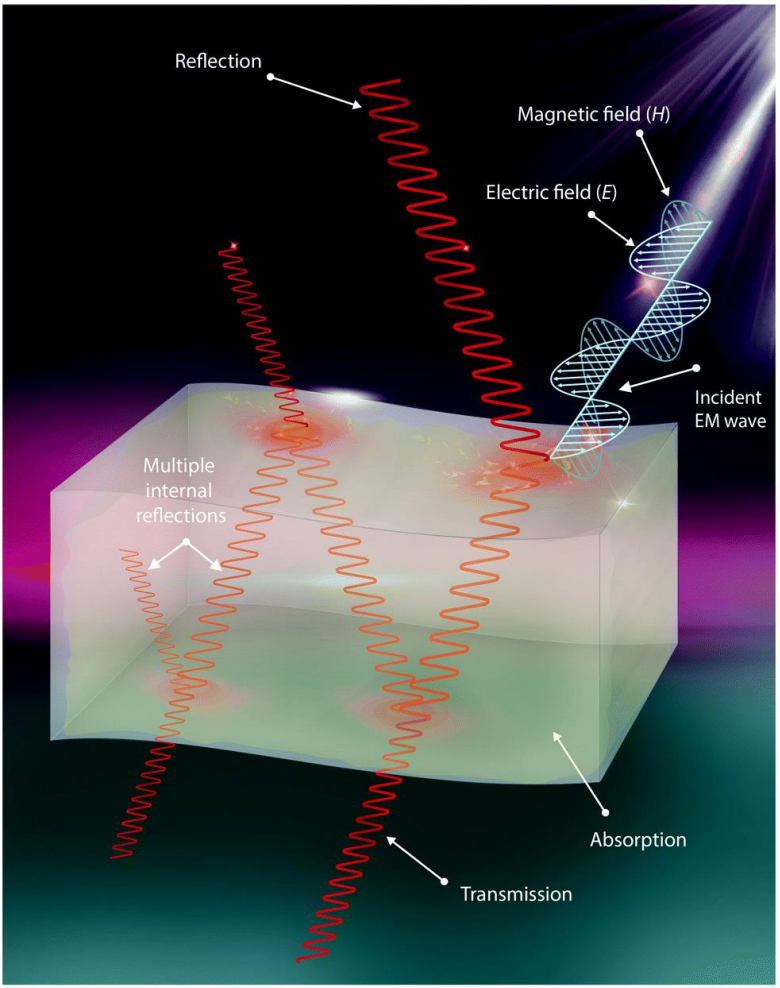
- Cost-effective
- Lightweight
- Sprayable
- Broadband
- > 100 dB shielding effectiveness

Stable dispersions with optimized composition

Sprayable coating

Test EMC

Technical Background



$$T(\omega, \boldsymbol{E}, \boldsymbol{H}) = (1 - R)\exp\{-\alpha l\}$$

reflection coefficient; absorption coefficient; thickness

$$R = \left|\frac{\sqrt{\tilde{\mu}/\tilde{\varepsilon}} - 1}{\sqrt{\tilde{\mu}/\tilde{\varepsilon}} + 1}\right|^2 \; ; \; \alpha = \omega\sqrt{2}\left[(\mu'\varepsilon' - \mu''\varepsilon'')\left(\sqrt{1 + \left(\frac{\mu'\varepsilon'' + \mu''\varepsilon'}{\mu'\varepsilon' - \mu''\varepsilon''}\right)^2} - 1\right)\right]^{1/2}$$

real permeability; real permittivity; imaginary permeability; imaginary permittivity

Reflection

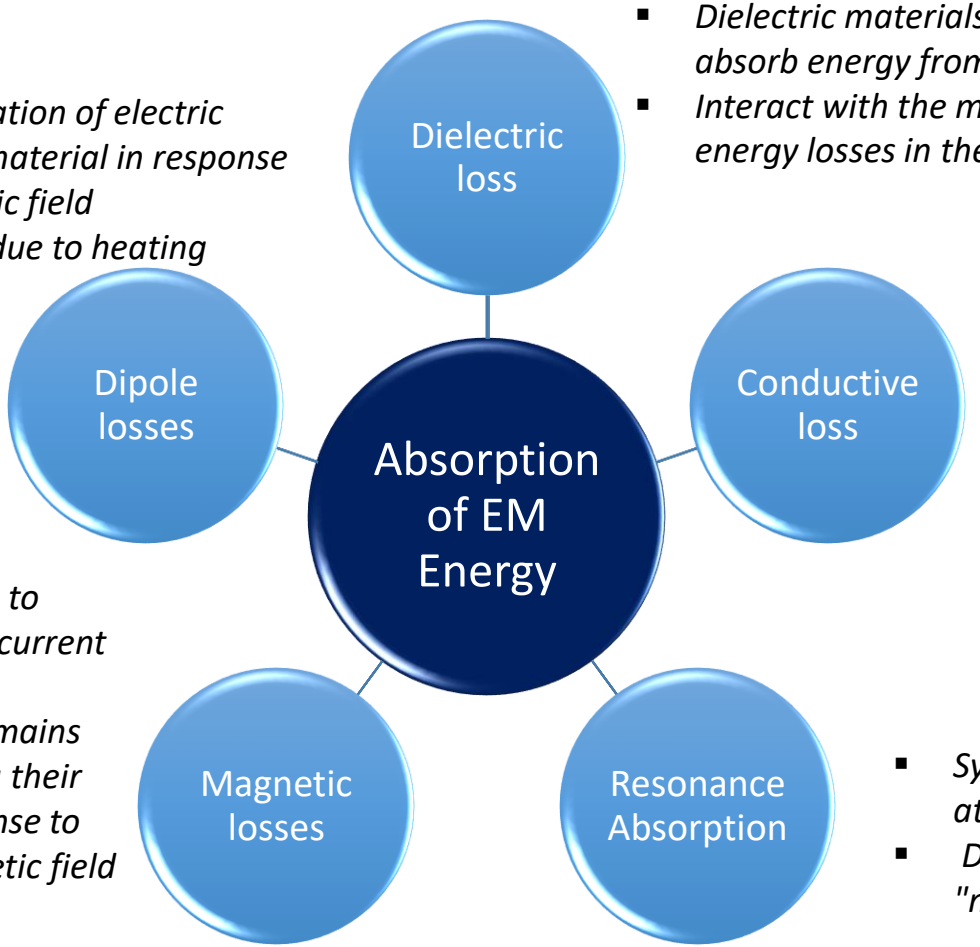
- Impedance mismatch
- Strong dependence on surface properties

Absorption

- Depends on electric permittivity (ε) and magnetic permeability (μ)
- Strong dependence on thickness
- Heating, electronic excitations, chemical reactions

→ **Minimize Reflection and Transmission**
→ **Maximize absorption by tuning chemical constituents and microstructure**

Absorption Dominated Mechanisms in EMI Shielding



- *Dielectric materials, like plastics and ceramics, can absorb energy from EM waves.*
- *Interact with the material's electric dipoles and cause energy losses in the form of heat*

- *Due to the reorientation of electric dipoles within the material in response to an applied electric field*
- *Energy dissipation due to heating*

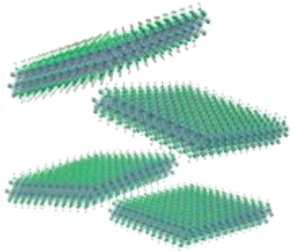
- *The electric field component of the wave induces currents in the material.*
- *These induced currents carry the electromagnetic interference through the material.*

- *Magnetic losses due to hysteresis and eddy current losses.*
- *Due to magnetic domains constantly switching their orientation in response to the changing magnetic field*

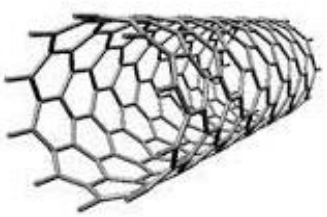
- *System absorbs energy most efficiently at a specific resonant frequency*
- *Dependent on physical properties or "natural" frequency of the system.*

Absorption mechanisms arise from chemical groups, constituents and structure and how these interact with the EM radiation

Performance of Current Classes of Material

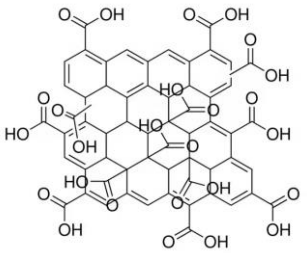


MXenes
(~1.5 gcm^{-3})

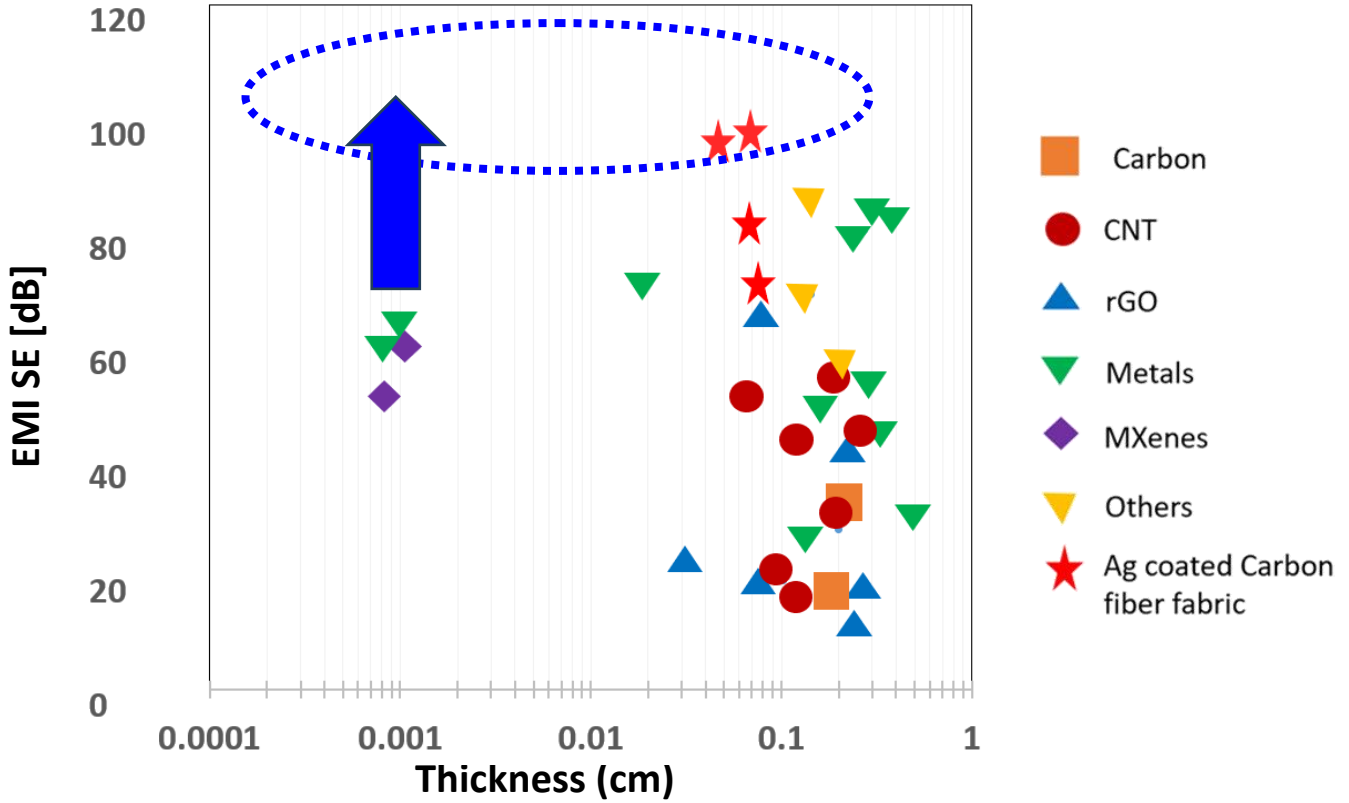


SWCNT
(~ 1.7 -1.9 gcm^{-3})

MWCNT
(~ 1.7 - 2.1 gcm^{-3})



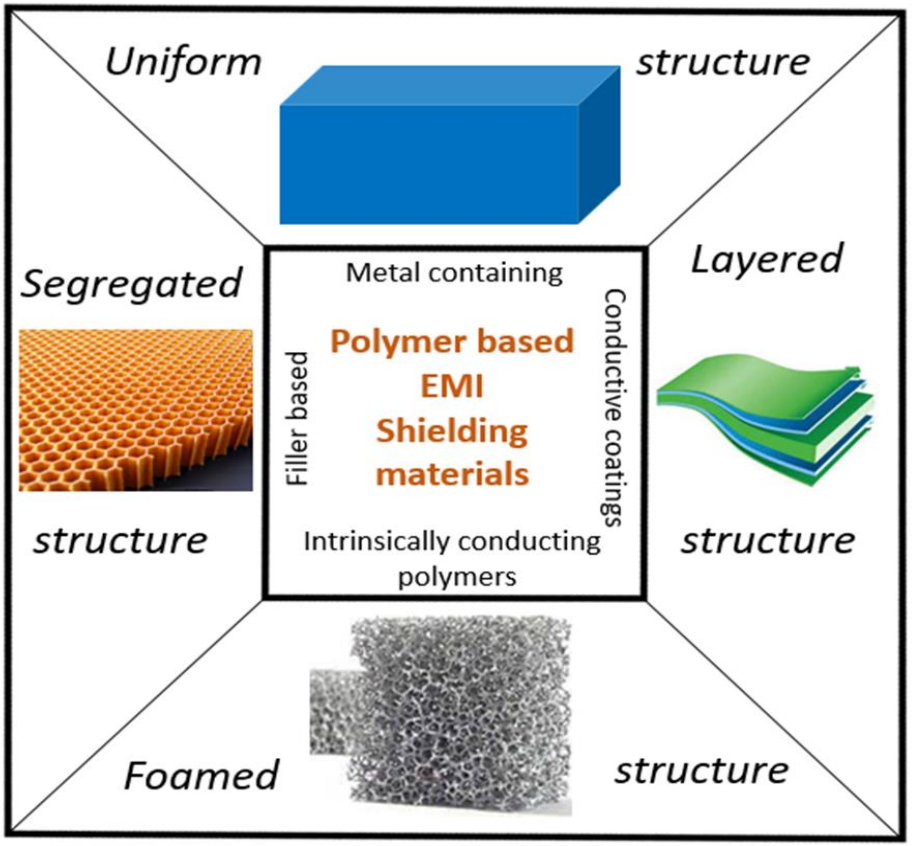
rGO
(~ 2.0 - 2.2 gcm^{-3})



→ Investigate/optimize candidate materials for sprayable coating

Polymer based EMI Shielding Materials

- *Thin coatings are effective even at higher frequencies*
- *Corrosion and compatibility maybe an issue*
- *Weight issues*

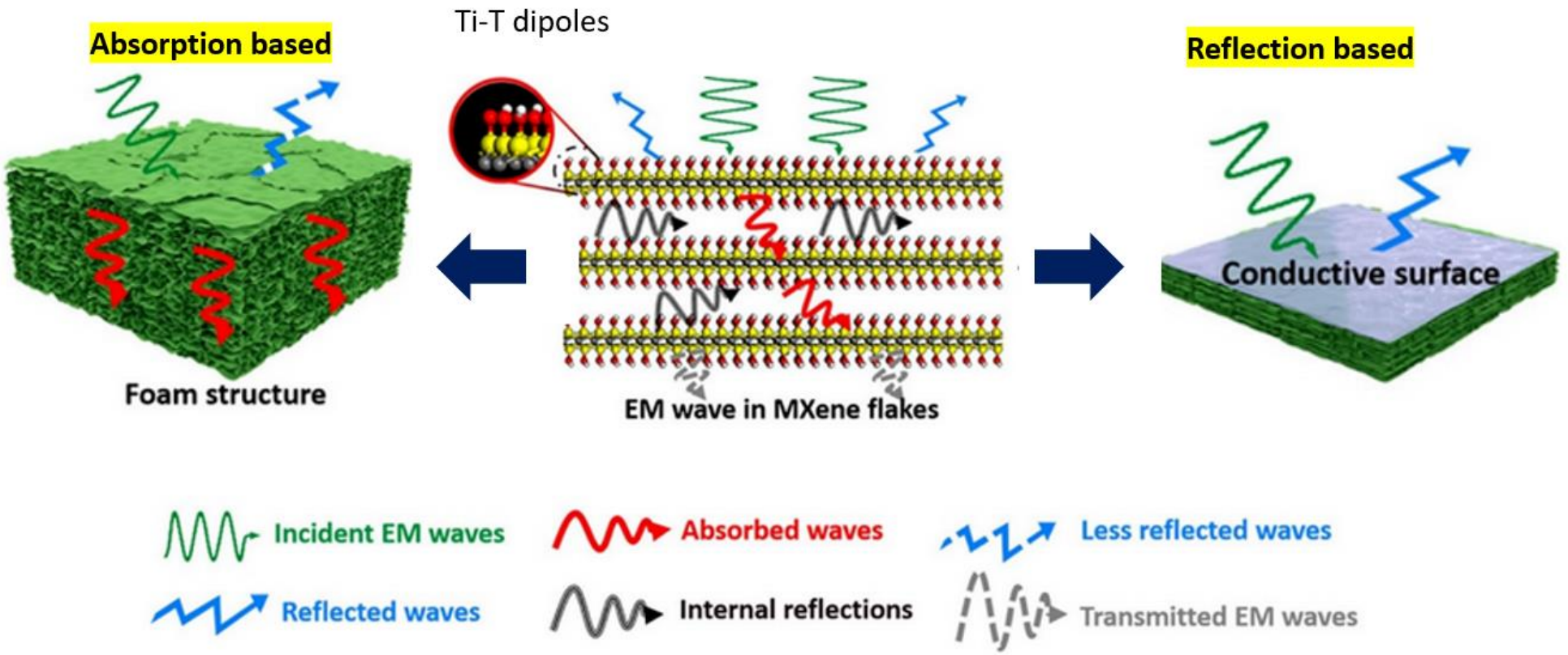


- *Tuned microstructures possible*
- *Synergistics effects of fillers and matrix useful*
- *Compatibility needs careful consideration*

- *Multiple materials can be integrated*
- *Tailored conductivity can be obtained*
- *Delamination to be considered*

- Light weight, tuned microstructures possible
- Tuned conductivities
- Thicker structure for shielding effectiveness
- Mechanical stability

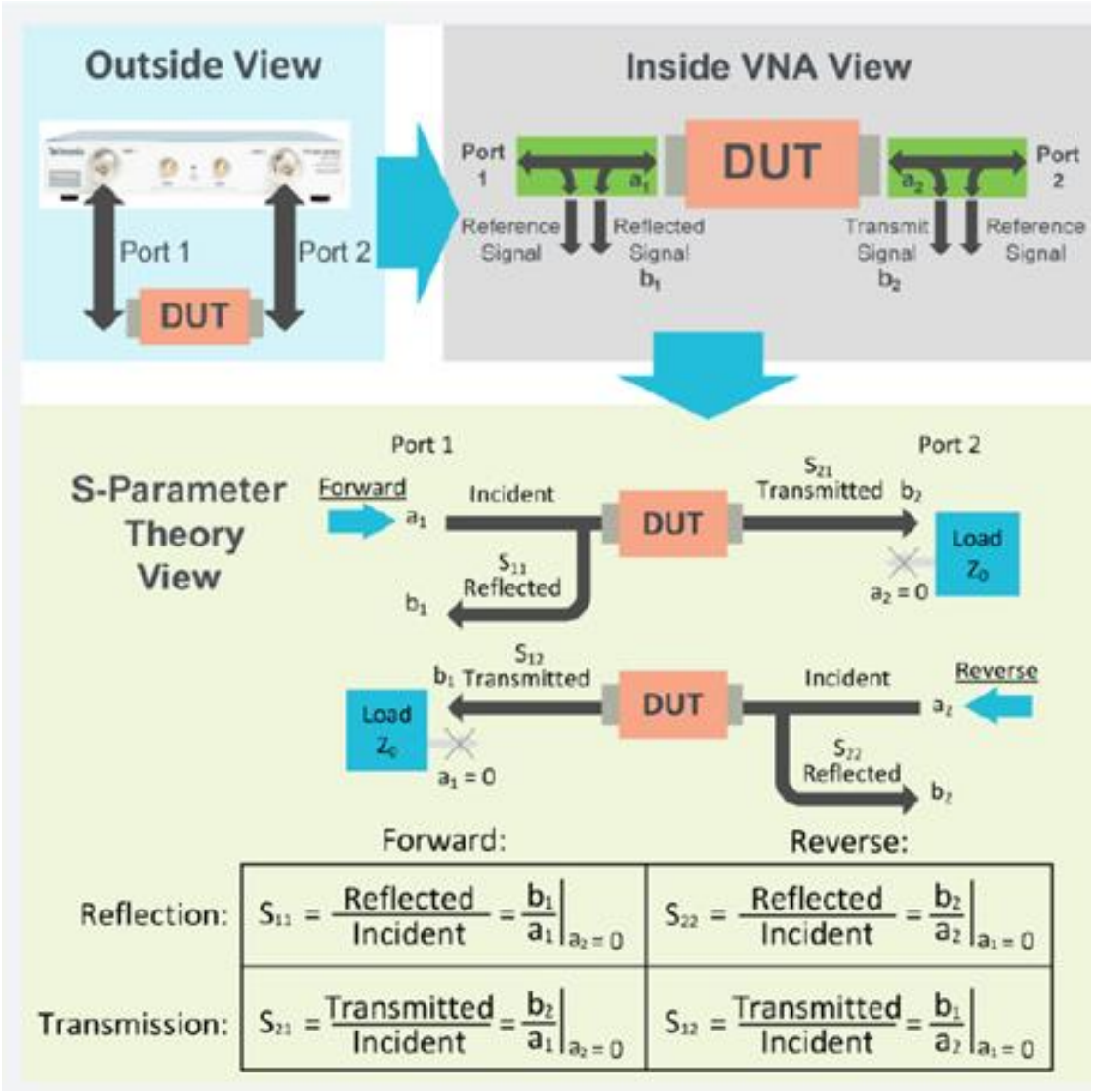
2D MXenes as Promising Fillers

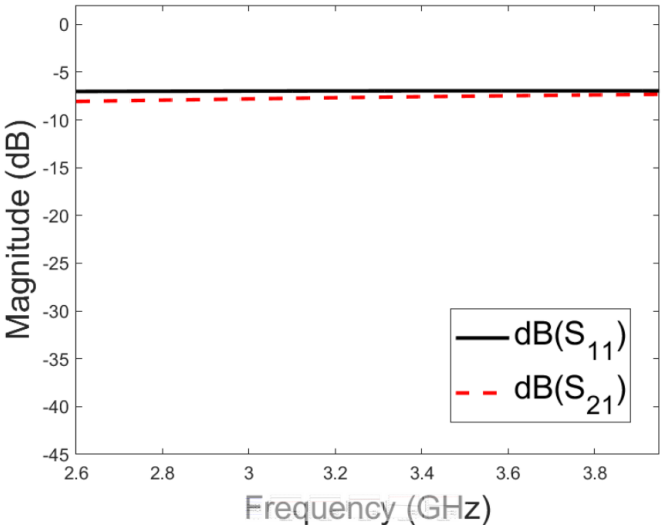


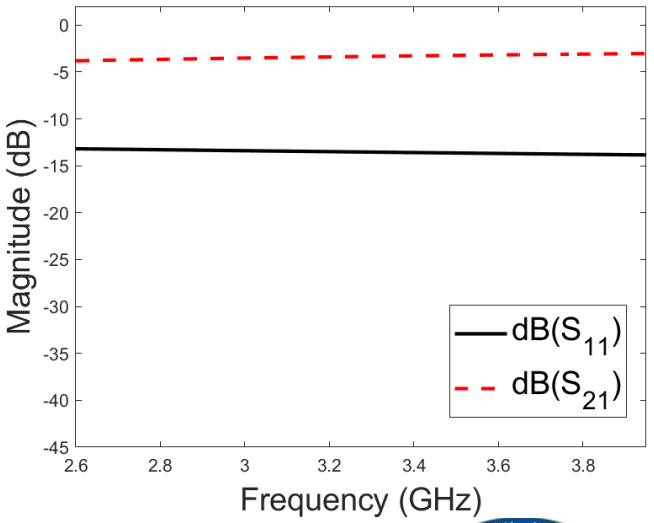
MXenes have ability to maximize EM absorption due to multiple internal reflections (MIR)

Electrical Characterization of Films

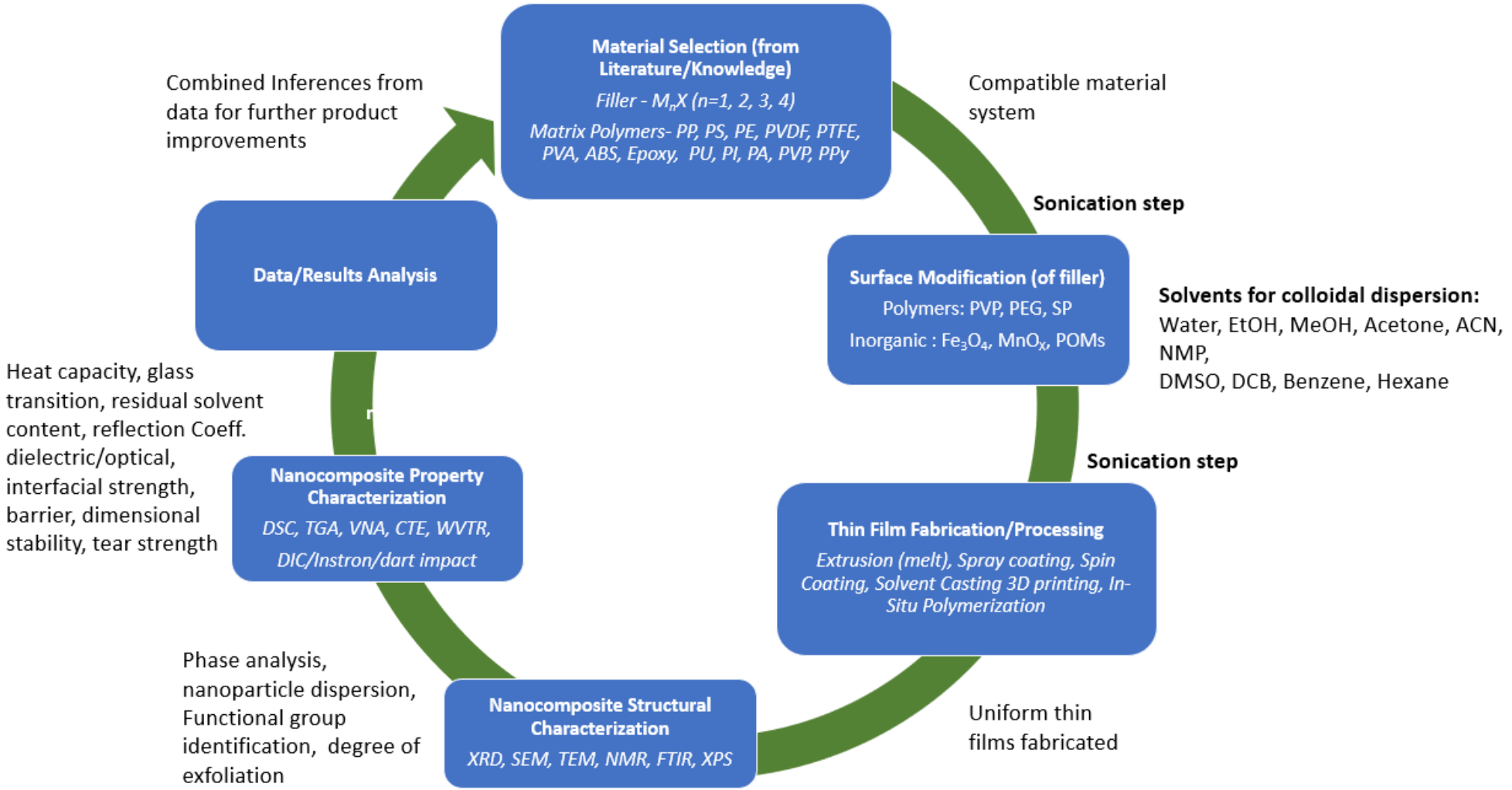
VNA setup for extraction of Transmission (S21) and Reflection (S11) coefficients





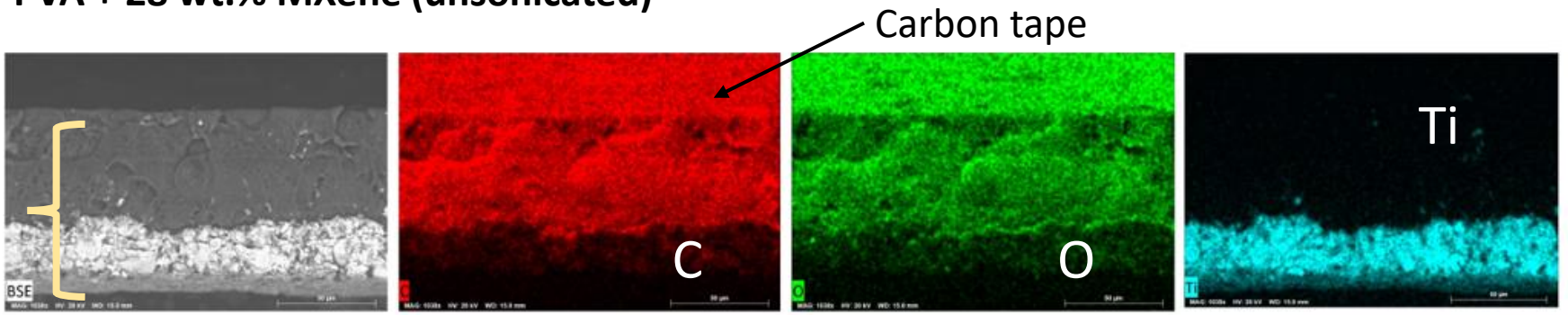


Approach: From Cradle to Grave

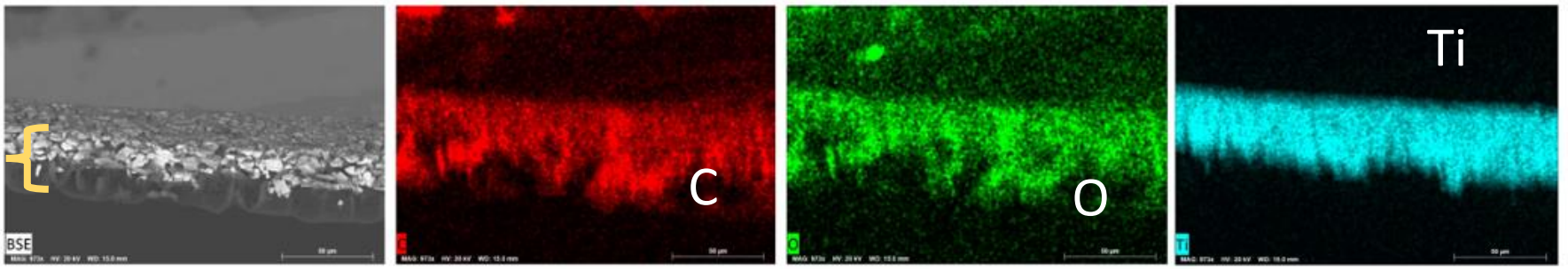


Effect of Sonication on Polymer Infiltration

PVA + 28 wt.% MXene (unsonicated)



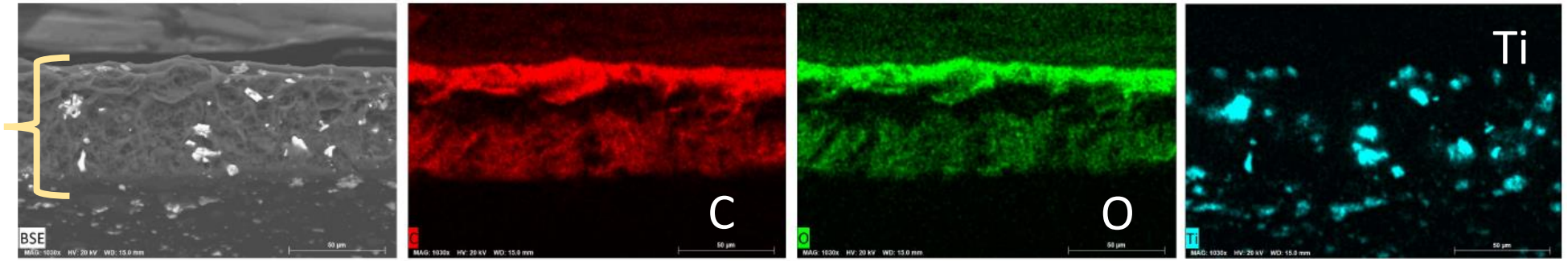
PVA + 28 wt.% MXene (sonicated)



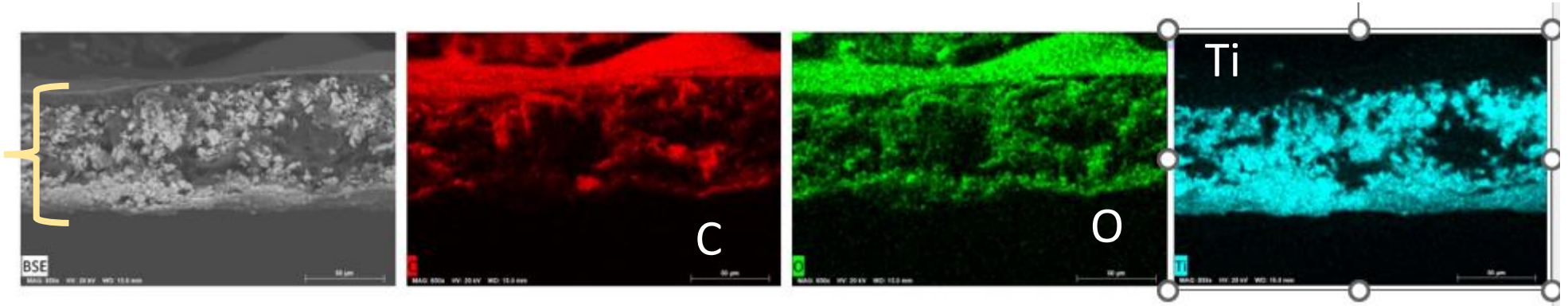
Sonication leads to PVA infiltration in between the MXene sheets
Sonication energy can be tuned to form multilayered structure in a single step

Effect of CNTs: SWCNT vs MWCNT

PVA + 7 wt.% MXene + 7 wt.% SWCNT



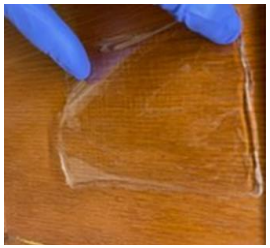
PVA + 7 wt.% MXene + 7 wt.% MWCNT



MWCNT addition leads to agglomerated MXene, dispersion difficult, viscosity issues

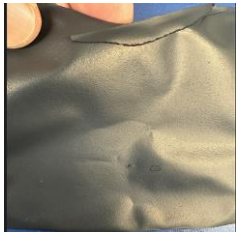
Total Shielding Effectiveness (SE) vs Frequency
Polyvinyl Alcohol (PVA)

PVA Control

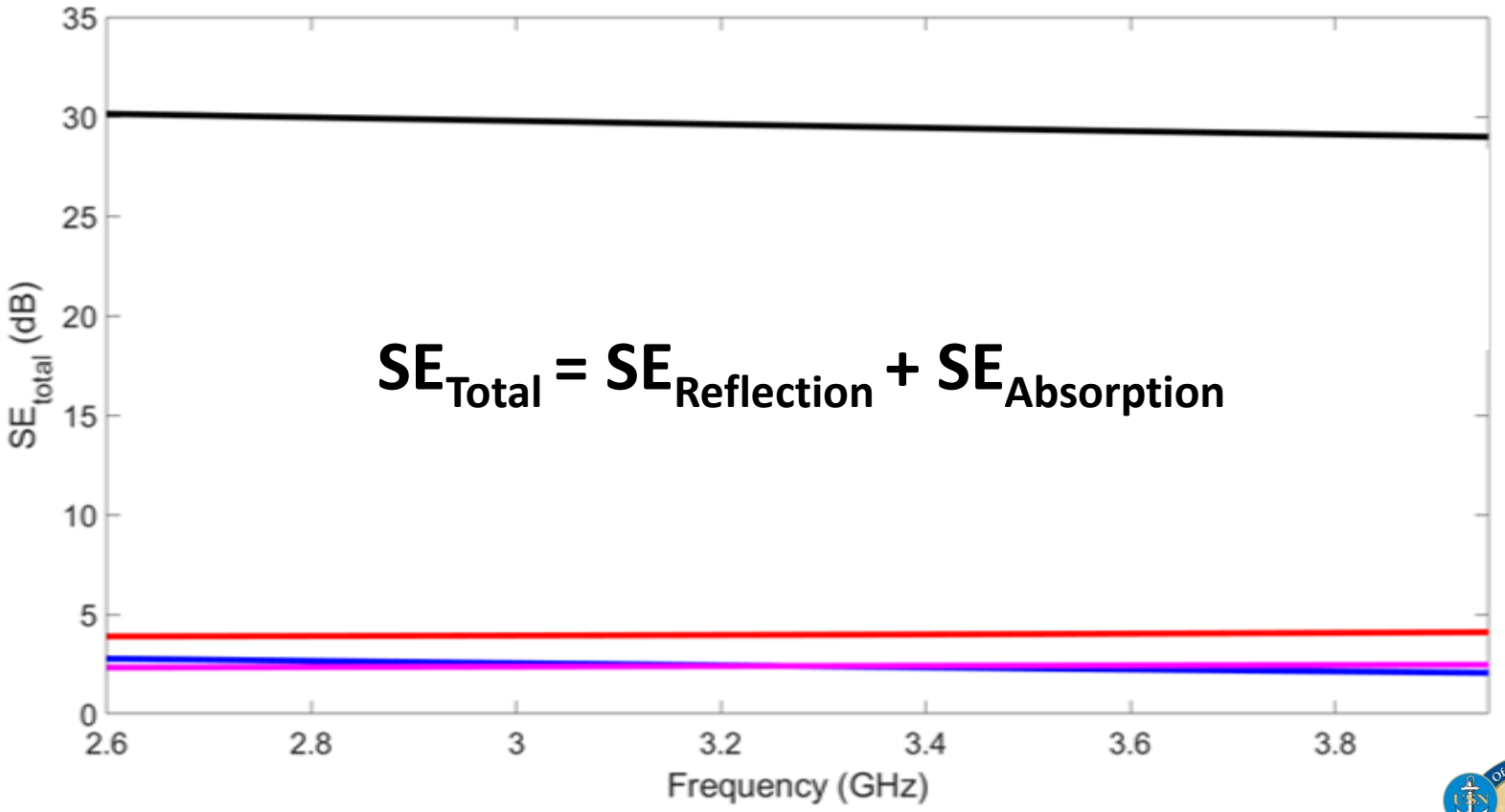


28% wt. MXene

7% wt. MXene
7% wt. MWCNT



7% wt. Mxene
7% wt. SWCNT

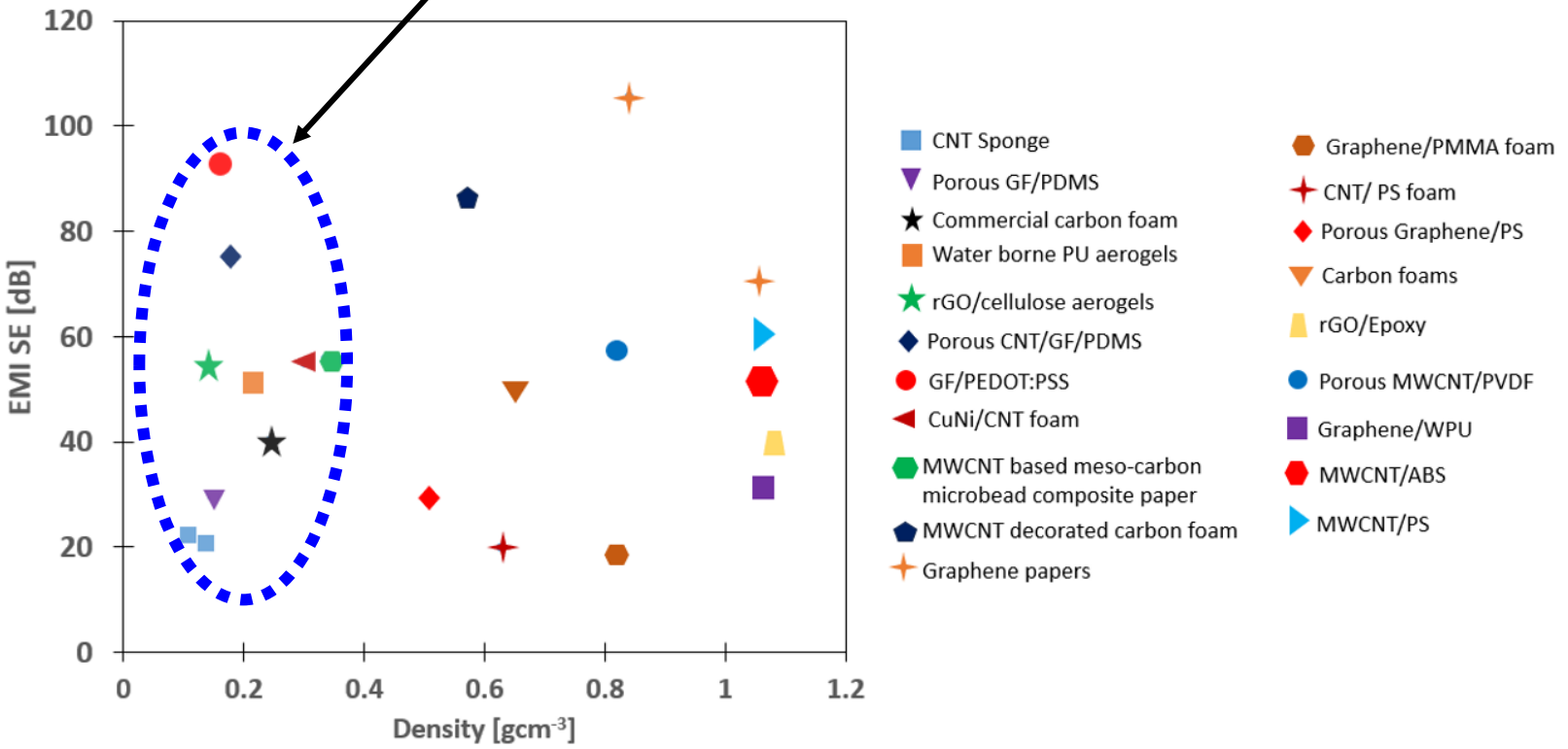


$$SE_{Total} = SE_{Reflection} + SE_{Absorption}$$

Performance of Carbon-based Materials

Ideal shielding material attributes

→ High EMI SE value at relatively low densities



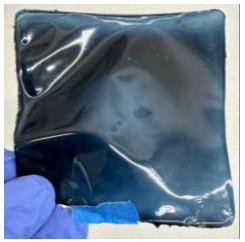
→ Can we use poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) into a binder such as PVA, and still have a stable water based sprayable coating?

Total Shielding Effectiveness (SE) vs Frequency

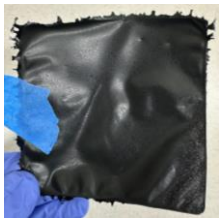
PVA + PEDOT:PSS

PVA Control

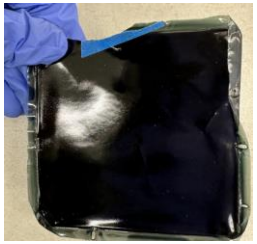
16% wt. PEDOT:PSS

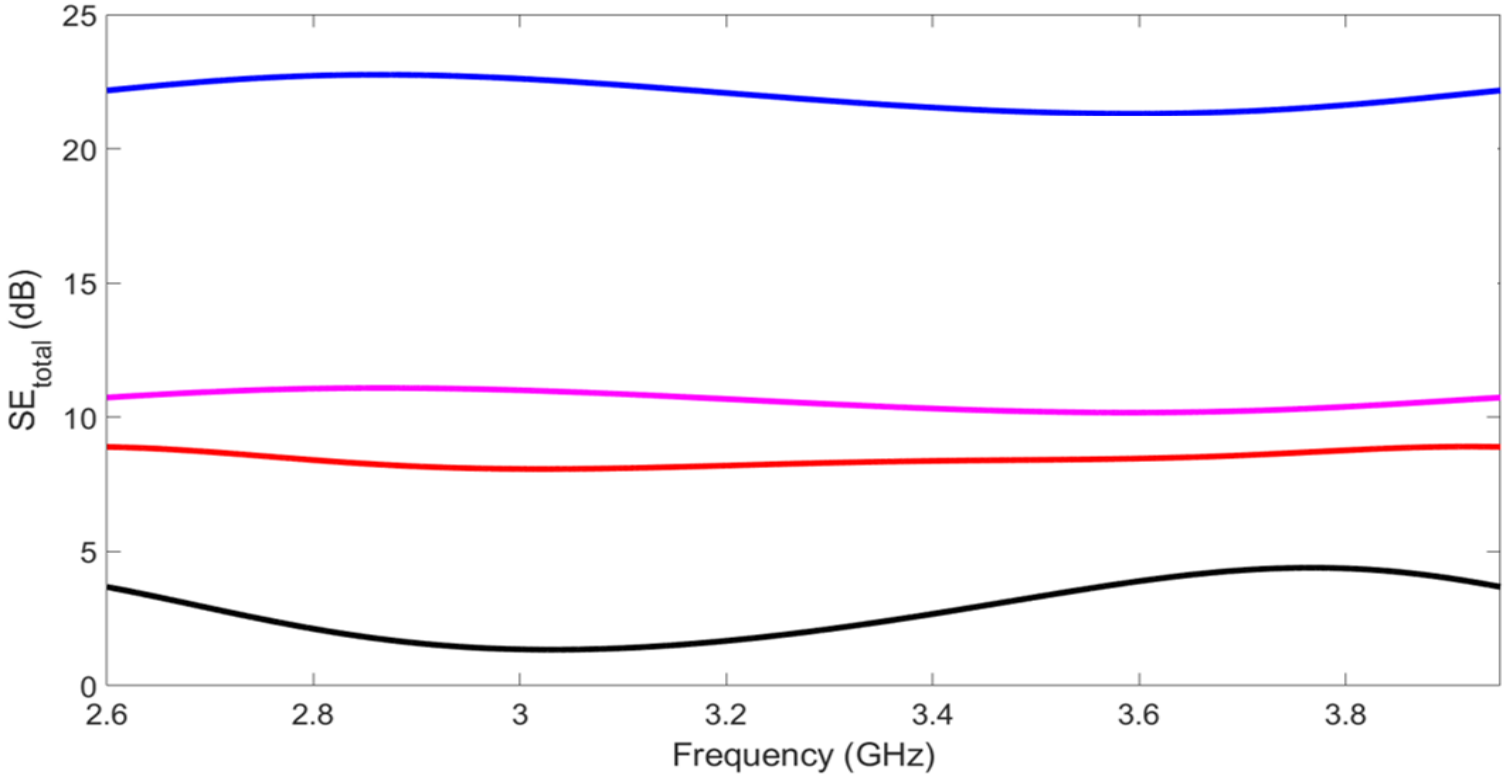


21% wt. PEDOT:PSS
10% wt. MWCNT



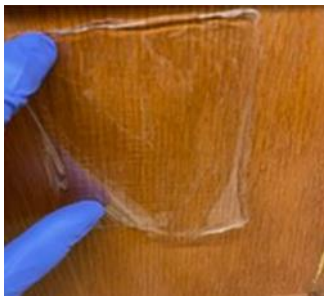
10% wt. PEDOT:PSS
35% wt. MXene



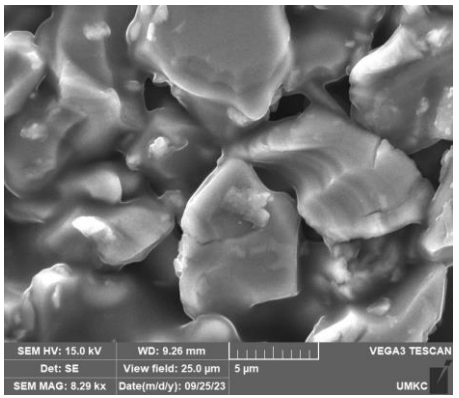


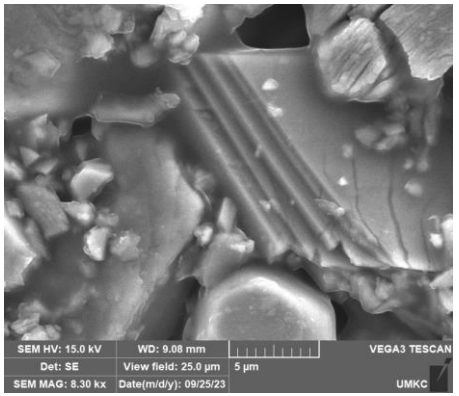
Summary

Facile synthesis of bubble-free, freely standing films by solution casting (*Current-Dec 2023*)

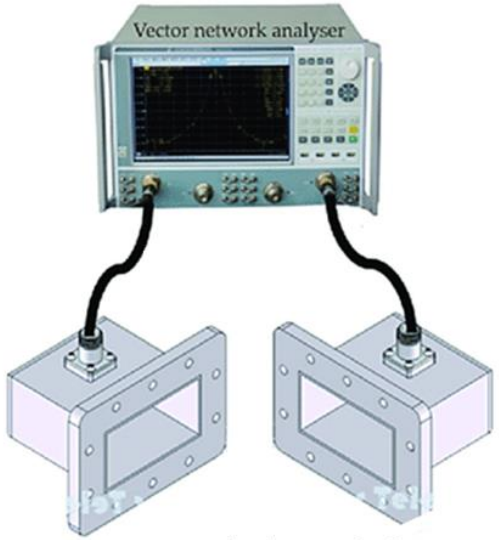


Structural characterization (*Current-Dec 2023*)





VNA for S-parameter measurement (*Current-Dec 2023*)



Scalable spraying technique onto UAV components *(Jan 2023-Mar 2023)*

Recommendations and Future Work

Literature Review

- Identify current systems for EMI shielding
- Limitations in the State-of-the-Art

Material Selection/Fabrication

- Material selection based on desired objectives
- Optimize composition
- Utilize matrices and fillers with varying aspect ratios, loading

Testing (Pilot scale)

- Structural characterization
- VNA testing for SE at a range of frequencies (1-30 GHz)

Application

Implement coating techniques for forming barriers to EMI

MIDE/UMKC Personnel

- Dr. Stephan Young (PI) Assistant Research Professor
- Dr. Travis Fields (co-PI) Associate Professor
- Dr. Pratish Rao (co-PI) Lead Research Specialist
- Alec Chance (Staff)
- Adam Solimani (UG)
- Deborah Para Cervantes (MS)

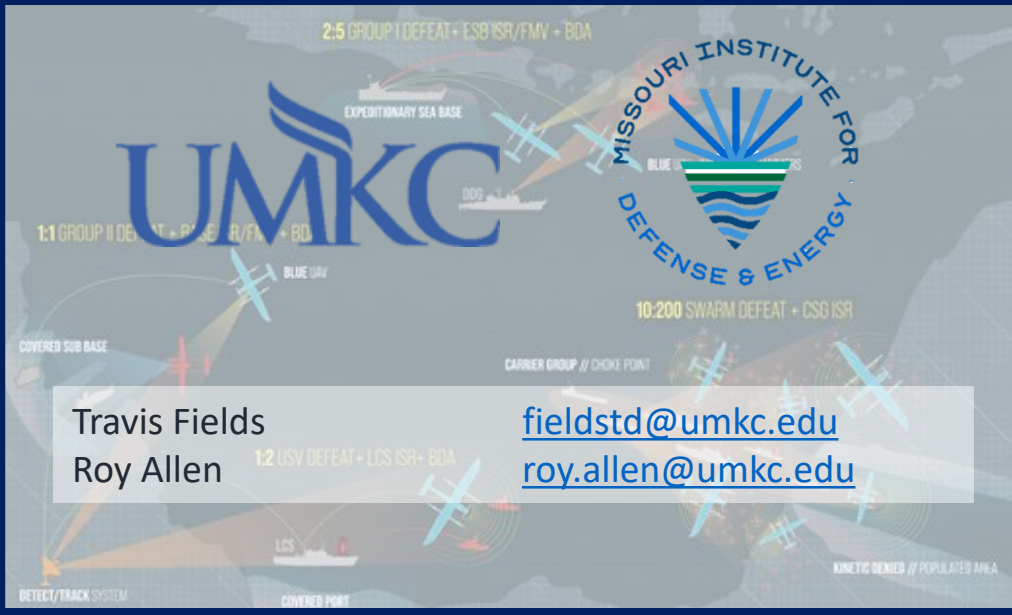
Pulse Tactical Effector for Regulated Attack

Year 2 Research Directions Overview

PTERA Grant Annual Review

October 10, 2023

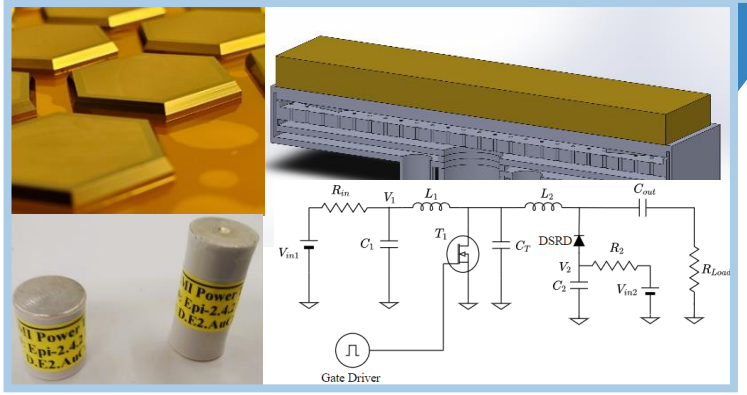
Funding provided by ONR under grant N00014-22-1-2385



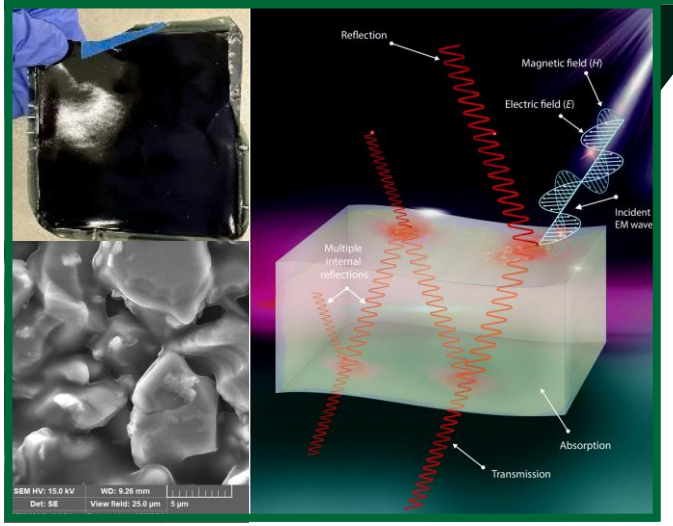
Travis Fields fieldstd@umkc.edu
Roy Allen roy.allen@umkc.edu

Year 2 (2023-2024) Research Thrusts

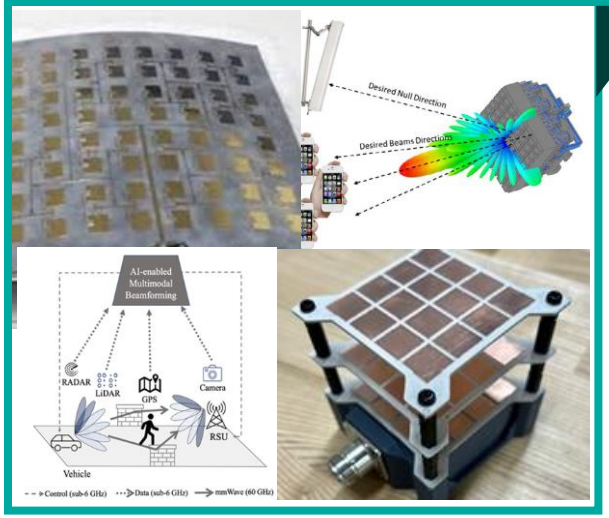
HPM Pulsers



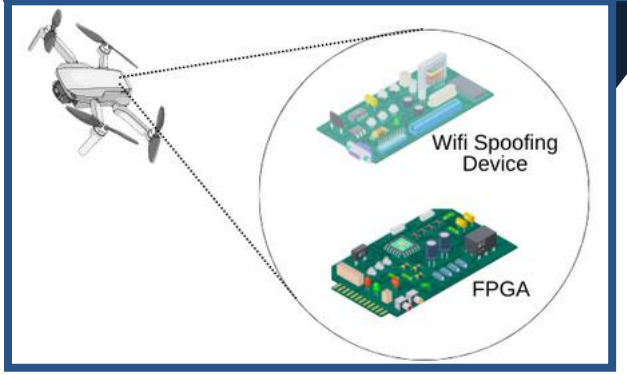
RF Shielding



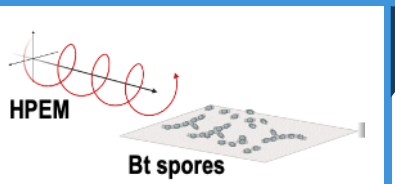
High Power Antennas



Information Operations

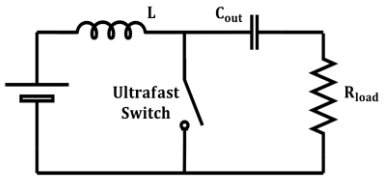


Bio EM



Semiconductor-based Pulsed Power Source Development

Motivation



Inductive Energy Storage and Release

Something very small that fits in a UAV but produces sub-nanosecond >50 kV pulses for defense applications.

● Volume <1 liter ● Weight <5 lb. ● Peak voltage >50 kV ● Risetime <500 ps

State of the Art and Problems

Semiconductor solutions exist but with limitations.

- **Limited output voltage (<7 kV)**
- **Limited pulse repetition frequency (10 kHz)**
- **Large operating voltage**
- **60-year old switch (DSRD/SAS) fabrication technology**
- **No COTS devices (DSRD and SAS) in the U.S.**

Objectives

- **Improve our advanced DSRD/SAS fabrication process and device quality**
- **Further optimize DSRD and SAS geometry and doping profile**
- **Increase pulser circuit voltage gain and energy efficiency**
- **Demonstrate >50 kV pulser**

Team Members

Gyanendra Bhattarai, PI
Pulser Optimization

Alex Usenko, co-PI
DSRD/SAS Fabrication

Jay Eifler, Post Doc.
DSRD/SAS Optimization

Shailesh Dhungana, Post Doc.
DSRD/SAS Structural Characterization

TBD
Graduate Student
Pulser module design and testing

TBD
Undergrad Student
Diode characterizations

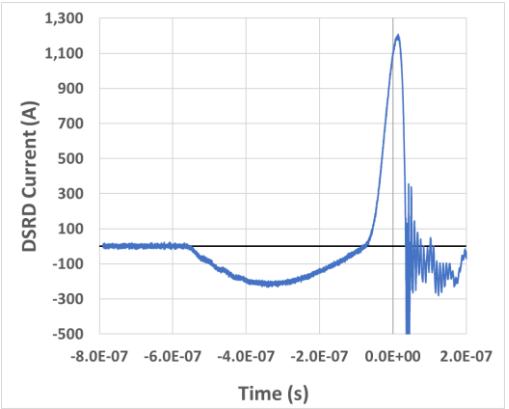
Semiconductor-based Pulsed Power Source Development

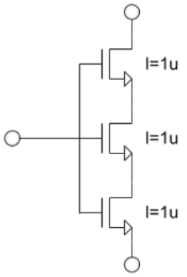
Approach

- **Increase the DSRD reverse current: Stack multiple MOSFETs in series and parallel**
- **Optimize circuit elements: Use our theory to develop efficient optimization scheme.**
- **Optimize DSRD/SAS geometry and doping profile based on pulser working principle to shorten switching time.**
- **Study SAS within high-quality TL and within sufficiently spaced multiple SAS sections**
- **Incorporate novel process flow for DSRD Fabrication**

Process Steps	Traditional Process Flow	Our Novel Process Flow
Wafer Preparation	Thinning	None (no need to thin)
Doping	Diffusion	Graded Epitaxy
Metallization	Blanket Deposition	Selective Plating
Patterning	Mechanical Sawing	Photolithography
Die Side Termination	Mechanical Sawing	Anisotropic Etch
Saw damage removal	Etch in HNA	None (no defects, thus no need)
Die Side Passivation	Polymer Coating	Stain Etch
Stacking	Soldering or Eutectic	Intermetallic bonding

Comparison of traditional and novel DSRD process integration schemes





Milestones

Tasks	Timeline
2 kA diode current, series stacking of at least two MOSFETs, Gen-3 diode model, singulation step (DSRD flow), 20 kV pulser	**Q1**
Stack 3-4 MOSFETs (>10 kV), SAS simulations for risetime <100 ps, V-Groove Glass frit filling, 30 kV pulser	**Q2**
Finish Gen3 DSRD fabrication, Provide DSRD-SAS pairs for experiments, Gen4 DSRD doping profile, Multiple SAS sharpening sections (<50 ps), 50 kV pulser	**Q3-Q4**

Multi-Pronged TMS for GaN Power Amplifiers

PI: Sarvenaz Sobhansarbandi, Ph.D.

Co-PI: Feyza Berber Halmen, Ph.D.

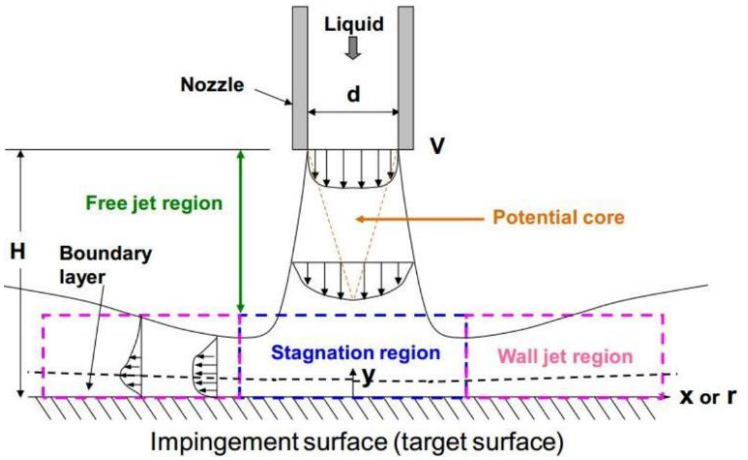
Post Doctoral Assistant: Shailesh Dhungana, Ph.D. provides support in terms of applicability of proposed ideas to PTERA mission and system testing

Graduate Research Assistant: Samual C. Sisk responsible for design and development of multi pronged UJI-TMS in alignment with SWAP-C2 constrained PTERA platform

Multi-Pronged Thermal Management Solutions for GaN Power Amplifiers

Motivation

A compact thermal management system (TMS) is required to enable the development of a high average power GaN PAs for the PTERA platform. The current SOTA integrated cooling technologies can achieve the cooling density of 1.5 kW /cm^2 through surface-to-surface contact points. However, this relies on cohesive connections, increases the amount of material, thus limiting the heat removal rate.



Objective

- To design and experimentally characterize several compact thermal solutions that can be fitted to the SWAP-C2 constrained PTERA platform as part of a GaN source.
- The proposed active cooling solutions will provide a constant temperature ≤ 85 °C to the bottom of the GaN package flange, in order to ensure more than **10x increase of the current 1% duty cycle**.

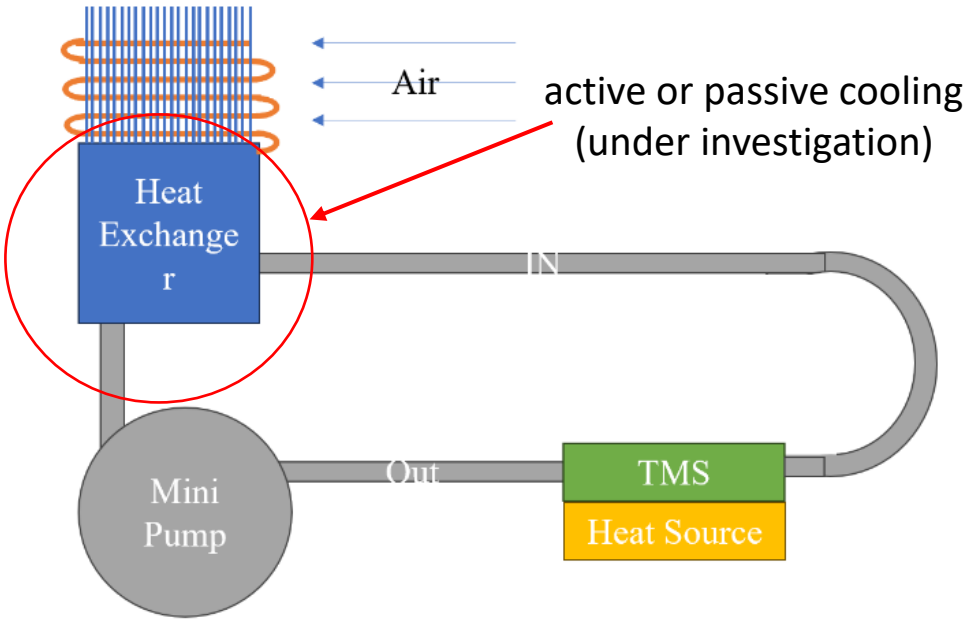
Multi-Pronged TMS for GaN Power Amplifiers

Milestones

- Phase II involves miniaturization of UJI-TMS auxiliary components to achieve a cooling system within PTERA size and weight requirements (less than 1000 cm^3 volume and 5 lbs. weight).
- The feasibility of the TMS will be tested under various power levels (2.6 kW - 5 kW GaN system).
- Experimental analysis of the system will be performed with a single mini pump to confirm the viability of the solution proposed, and/or whether further modifications is needed or move to the next solution space.

Approach

- Experimental analysis will be performed to provide heat rejection rate of Ultra Compact Jet Impingement TMS (UJI-TMS) and the temperature of the target surface, from which the **GaN duty cycle** can be approximated.
- A **mini pump** (weight: <500g / size: 11 x 9.8 x 9 cm) that can provide the required heat removal capability with the flow rate of 3gpm is already identified.
- Various options for **miniaturized heat exchanger** is being investigated.



Proposed Design 1 (Sep. – Dec. 2023)

BCN as a Thermally Conductive Low-*k* Dielectric

Prof. Michelle Paquette
PI

Dr. Feyza Berber Halmen
Co-PI

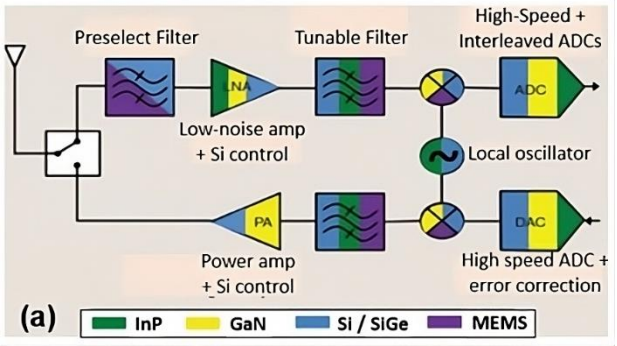
Dr. Shailesh Dhungana
Co-PI

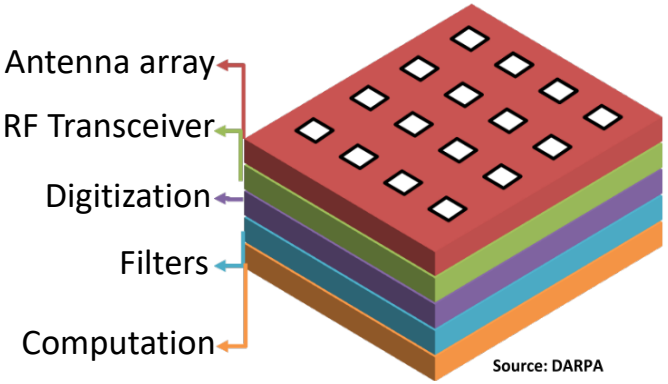
Objective

To investigate the potential of BCN films as a low-dielectric-constant (low-*k*) high-thermal-conductivity (κ) interlayer dielectric (ILD) for thermal management in Si CMOS and 3D integration. Our goal is to map process–property relationships and optimize films to achieve properties superior to SiO_2 ($k < 4$ and $\kappa > 1$ W/m·K, with comparable electrical and mechanical properties).

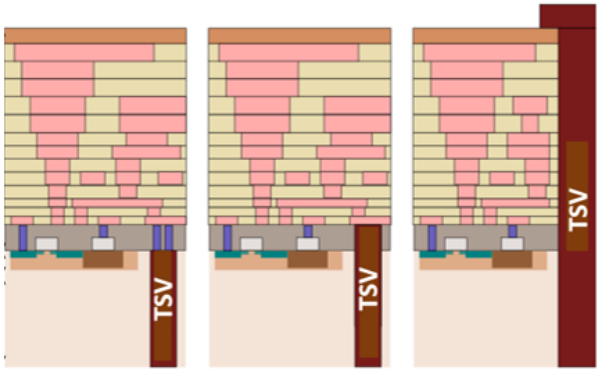
Motivation

- Heat generation by millions of transistors in a small area, as in modern CMOS, and high-power-density devices, such as gallium nitride power amplifiers, is a substantial issues for stand-alone integrated circuits (ICs), exacerbated by stacking or 3D integration.
- Due to the low thermal conductivity of interlayer dielectrics, traditional thermal management solutions involve substrate engineering and the use of through-silicon vias (TSVs).
- The development of thermally conductive ILDs offers a promising thermal management strategy.





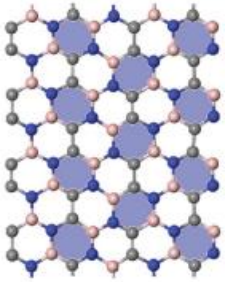
A transceiver system including CMOS control circuitry and its 3D-integration as envisioned by DARPA.



Through-silicon vias (TSVs) within an integrated circuit.

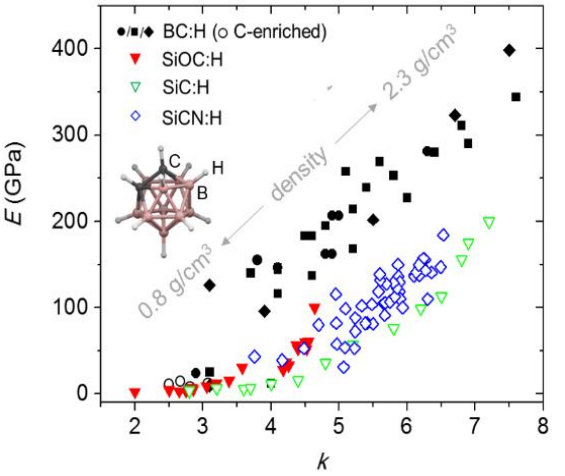
BCN as a Thermally Conductive Low-*k* Dielectric

Nordell et al., *Front. Mater.*, **2019**, 6, 264 [doi]; Paquette et al US Patent no. 10,301,719 B1, May 28 **2019;** Nordell et al., *Adv. Electron. Mater.*, **2017**, 3, 1700116 [doi]; Nordell et al., *Adv. Electron. Mater.*, **2016**, 2, 1600073 [doi]; Nordell et al., *Mater. Chem. Phys.*, **2016**, 173, 268 [doi]; Nordell et al., *J. Appl. Phys.*, **2015**, 118, 035703 [doi]



Approach

- Boron carbon nitride (BCN) has a combination of low dielectric constant, robust mechanical and chemical properties, and high electrical insulation.
- It can be synthesized by a variety of techniques, with tunable properties.
- BCN is predicted to have high thermal conductivity (e.g., 175 W/m·K; Muthaiah 2021), but experimental work is nearly non-existent.



DOE 2^k factorial growths of BCN thin films

Film characterization

- **Electrical and Electronic** (Band gap, dielectric constant, refractive index, leakage current, dielectric breakdown field)
- **Thermal and Mechanical** (Thermal conductivity, Young's modulus)
- **Fundamental** (Thickness, growth rate, density, chemical composition, bonding)

New fabrication conditions based on the results

Months 1–3	Preliminary growth and characterization of BCN thin films using plasma-enhanced chemical vapor deposition (PECVD) and physical vapor deposition (PVD).
Months 4–6	First round of design of experiment (DOE) 2^k factorial growths: process–property results.
Months 7–9	Second round of DOE 2^k factorial growths targeting $k < 4$ and $\kappa > 1$ W/m·K: process–property results.
Months 10–12	Final round of DOE 2^k factorial growths targeting $k < 3$ and $\kappa > 5$ W/m·K: process–property results with assessment of potential as an ILD for thermal management.

Milestones/Deliverables

Conformal Antenna Array for HPM UAS Applications

Faculty

Kalyan Durbhakula
Assistant Research Professor, Missouri Institute for Defense & Energy

Mohamed Hamdalla
Assistant Research Professor, Missouri Institute for Defense & Energy

Ashiqur Rahman
Instructor, Division of EMS, UMKC

Ahmed M. Hassan
Associate Professor, Division of EMS, UMKC

Dec Chatterjee,
Associate Professor, Division of EMS, UMKC

Students

Sai Indharapu
Ph.D. Student

Mashrur Zawad
Ph.D. Student

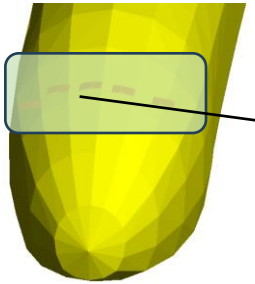
Al-Moatasem Al-Hinaai
Ph.D. Applicant

Chandana Kolluru
M.S. Student

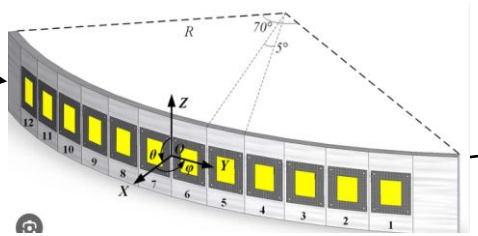
Semire Olatunde-Salawu
Undergraduate Junior

Conformal Antenna Array for HPM UAS Applications

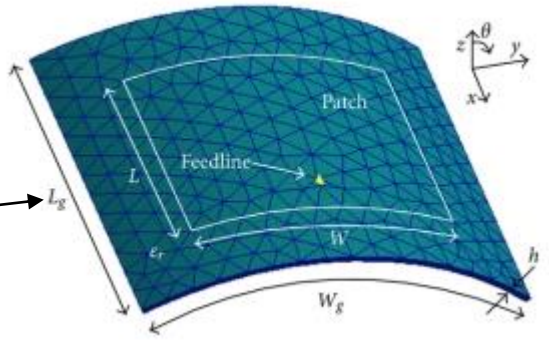
Mugin-4 Pro VTOL UAV Platform



FEKO model of an array positioned on the fuselage



Cylindrical Conformal Antenna Array



Conformal Antennas Design

Motivation:

- UAS applications require antennas (or arrays) to be small, flexible, easily integrable, and lightweight while ensuring the antenna's frequency and time-domain performances are retained.
- Conformal antennas are a promising avenue to explore and enable reconfigurability.

Current SOTA Limitations:

- Ability to tune the operating frequency
- Array size doubles or quadruples
- Use of expensive and bulky phase shifters, and RF front-end modules
- Larger footprint and costly to produce and maintain such array systems

Objective:

- To demonstrate:
  - A reconfigurable conformal antenna array built on a flexible substrate
  - 50% frequency tunability utilizing RF switches
  - GA-inspired metasurface lens to amplify the nominal gain (10 dBi) and peak gain (15 dBi)
  - Reduced electromagnetic wave dispersion rate in the far-field leading to improved power density
  - Beam steering or formation in the range of +/- 60° from the boresight with an angular tolerance of ≤2°

Conformal Antenna Array for HPM UAS Applications

Sep 23 – Nov 23

- Optimize, and compare the INITIAL PERFORMANCE values from different sub-efforts and verify to meet the threshold/objective.

Dec 23 – Feb 24

- Produce the first round of CAD files for fabrication followed by TESTING, comparison, analysis, and design improvements for the next version.

Mar 24 – May 24

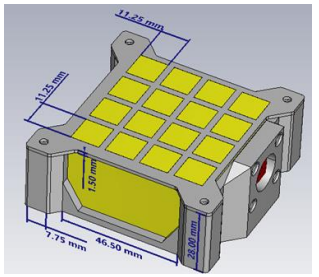
- Integrate the STANDALONE designs to a single conformal antenna array of size Nx1 and demonstrate their coexistence on a flexible substrate.

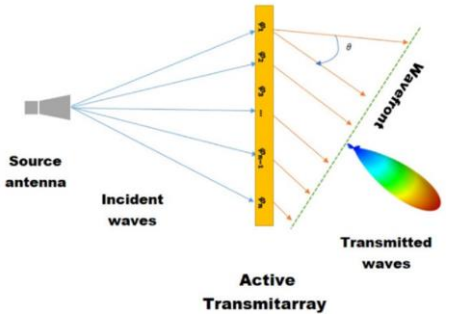
Jun 24 – Aug 24

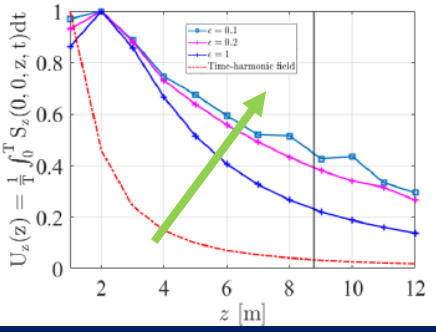
- Showcase the optimized conformal antenna ARRAY PROTOTYPE identifying major performance improvements. Perform UAV-integrated tests if feasible.

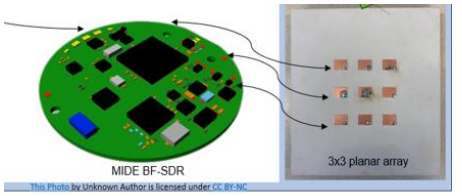
Approach:

1. Optimize single-element high-power antenna prototype by incorporating a phase gradient metasurface design to provide beam steerability. The design will be tested inside the fuselage of a UAV.
2. COTS RF switches will be used to enable frequency and bandwidth reconfigurability of an ultrawideband patch antenna element built on a low-cost flexible substrate and later scaled to an appropriate linear array.
3. The shape of the UWB patch antenna element and of the array will be studied and optimized using aperture analysis techniques to achieve minimum power density roll-of in the far-field.
4. Generative adversarial networks and reinforcement learning algorithms will be used and tested to improve real-time beamforming efforts with low angular tolerance.









Nanosecond HPEM Waveforms for Pathogen Inactivation

- Personnel

PI: Ahmed M. Hassan, Ph.D.
Associate Professor, University of Missouri-Kansas City, Division of Energy, Matter and Systems

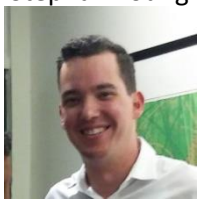
Co-PI: Jared P. May, Ph.D.
Assistant Professor, University of Missouri-Kansas City, Division of Biological and Biomedical Systems

Co-PI: Stephan Young, Ph.D.
Research Assistant Professor, MIDE

Ahmed Hassan

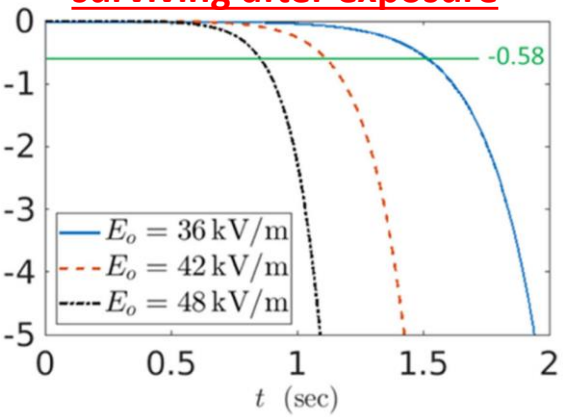
Jared May

Stephan Young



- Motivation
  - Current SOTA for eliminating biological threats is chemical decontamination
    - Often incomplete, e.g., bleach is only 90% effective against anthrax spores after 10 minutes.
  - UVC-based UAVs requires >5-minute treatment time
    - Technologies developed in this proposal will operate on <1-minute timescales for disinfection.
  - HPEM techniques require fields in the order of 40-2350 kV/m
  - Current UAV-based methods primarily focus on detection, not neutralization.

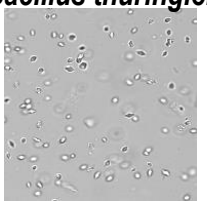
Log scale fraction of virus surviving after exposure



- Objective

Optimize nanosecond High Power Electromagnetic (HPEM) waveforms to inactivate bacterial and viral pathogens at lower peak power.

Bacillus thuringiensis



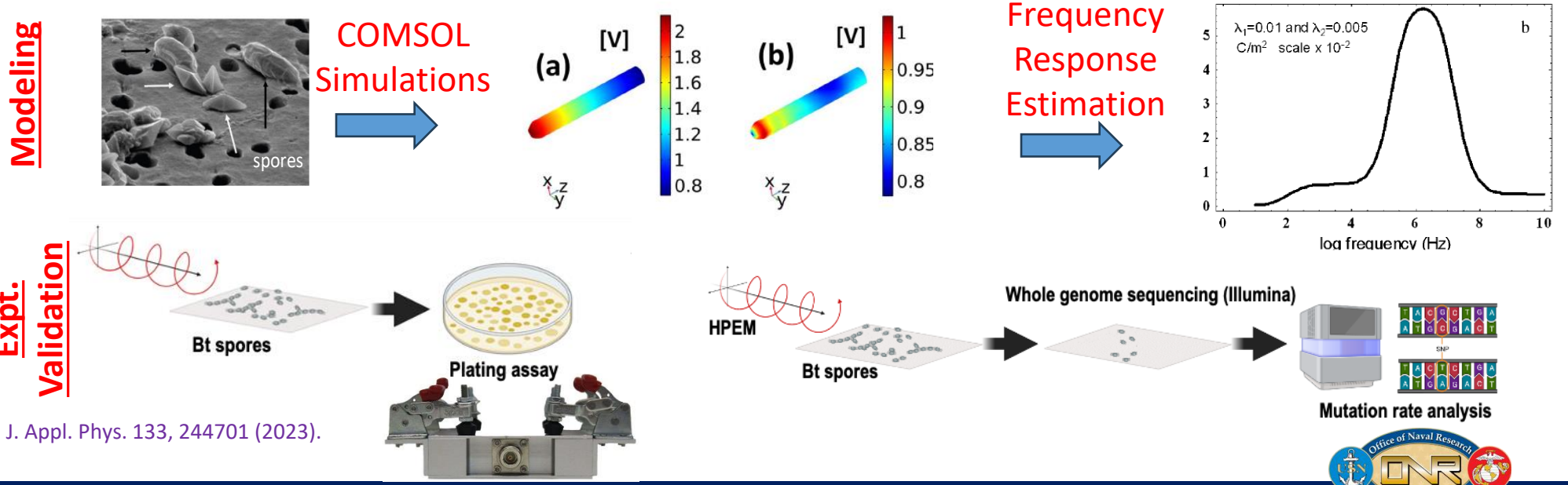
Mock

+TMV

- Bacterial – Anthrax surrogate – *Bacillus thuringiensis and* Viral – Tobacco mosaic virus

Nanosecond HPEM Waveforms for Pathogen Inactivation

- Milestones/deliverables
  - 1. Optimized HPEM waveform parameters (computationally modeled) for Bt spores and TMV.
    - 2 months
  - 2. Development of Bt spore and TMV viability assays for HPEM testing
    - 2 months
  - 3. Experimentally validated optimized nanosecond HPEM waveform parameters for reducing Bt spore viability and TMV virulence
    - 6 months
  - 4. Mutagenesis capacity of optimized HPEM waveforms and potential resistance mutations
    - Months 6-11
- Approach
  - Optimize HPEM waveforms for eliminating bacterial spores and viruses using COMSOL Finite-Element simulations and TEM cell measurements
  - Evaluate optimized waveforms for inducing genetic instability in bacterial genomes.



J. Appl. Phys. 133, 244701 (2023).

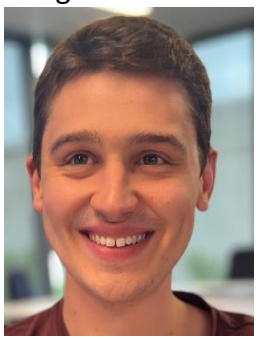
Innovations in Ultralightweight EMI/RFI Shielding

Dr. Stephan Young
PI

Prof. Travis Fields
PI

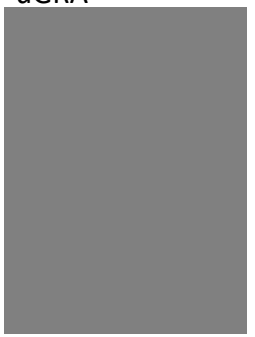
Dr. Pratish Rao
Co-PI/Technical Lead

Alec Chance
Engineer

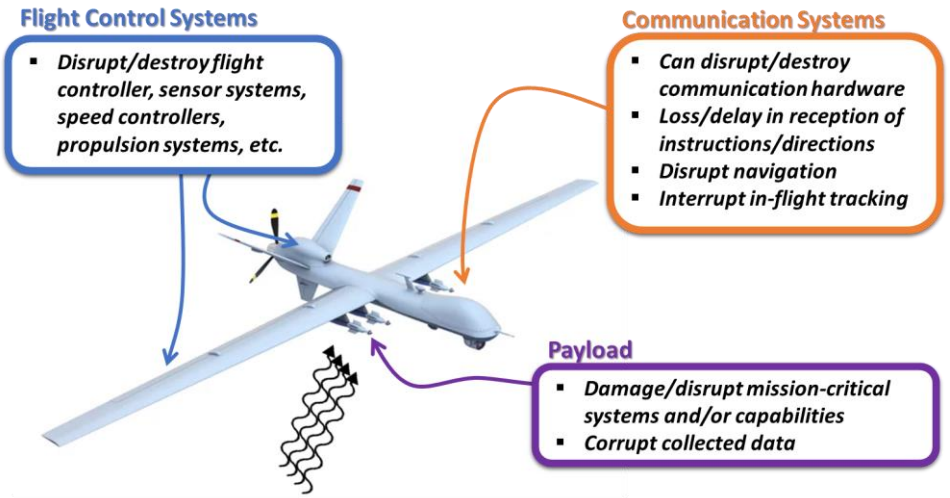


Debbie ParraCervantes
GRA

Adam Solimani
uGRA



Motivation



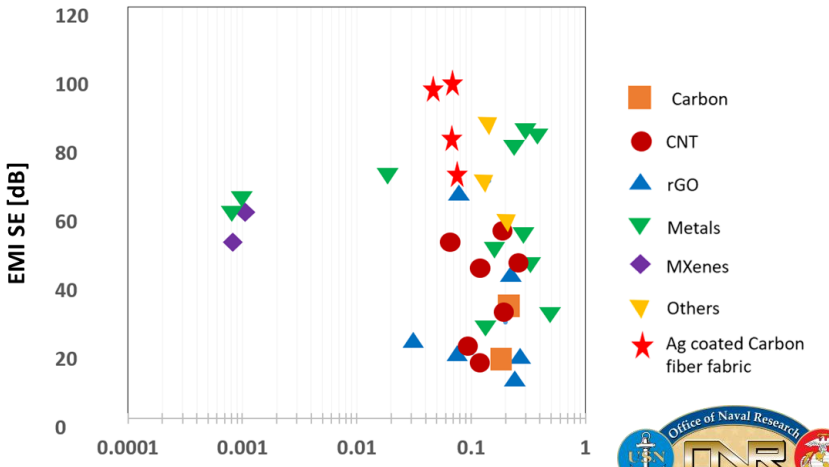
→ EMI can impact the success of a UAS mission

→ There is a need for robust, lightweight, and inexpensive coatings to shield UAS platforms from the effects of EMI

Objective

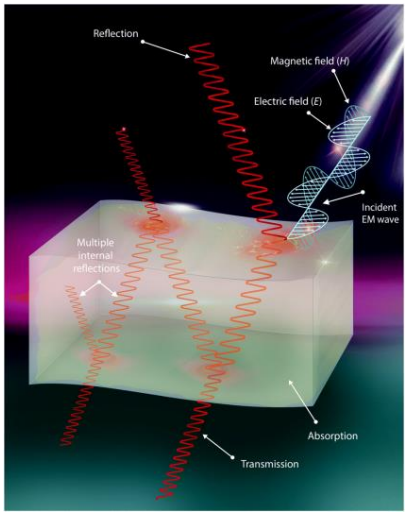
→ Develop shielding coating with:
- > 50 dB SE from 1-30 GHz
- Thickness < 100 µm

→ Investigate synergistic effects between constituent materials (i.e. polymer matrix, nanoparticles filler, and dispersing agent)



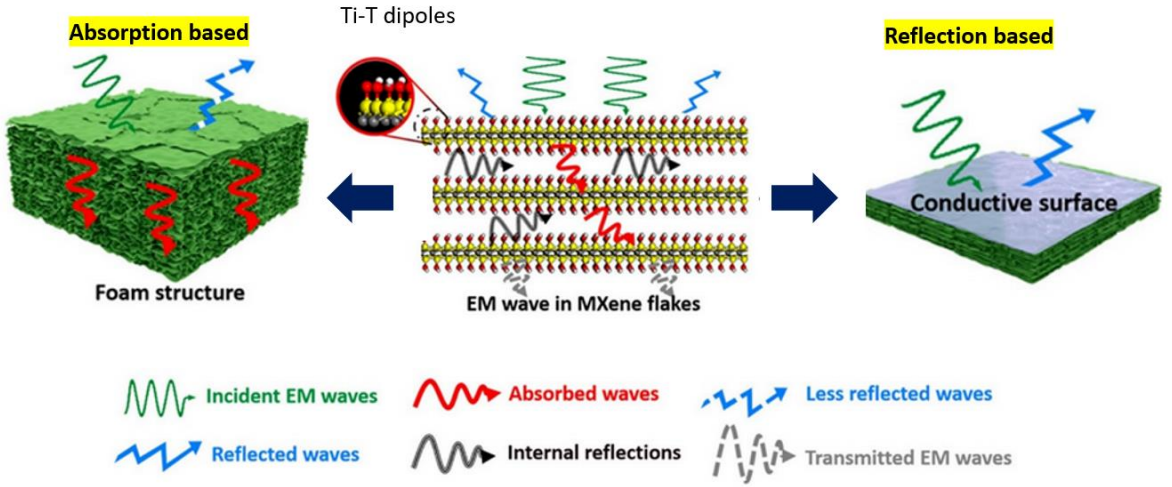
Innovations in Ultralightweight EMI/RFI Shielding

Approach



→ Maximize Absorption

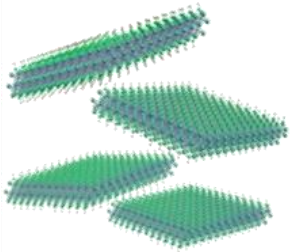
Sprayable MXene-based nanocomposite coatings



Task No	Task Description	Personnel	Resources	Timeframe
1	Literature review/Materials selection	Pratish Rao	Web	Sept 2023 to Oct 2023
2	Fabrication of freely standing nanocomposite films	Pratish Rao	Wet chemistry lab	Sept 2023 to Dec 2023
3	Optimization of dispersion	Pratish Rao	Wet chemistry lab	Oct 2023 to Dec 2023
4	Characterization of dispersion/films	Pratish Rao/MIDE/UMKC facility	Zetasizer/Rheometer/ SEM/XRD/EDS	Oct 2023 to Dec 2023
5	Electrical characterization/conductivity measurements/S-parameters	Deborah Cervantes	VNA	Oct 2023 to Dec 2023
6	Translate lab-based dispersion into an ultrasonically sprayable coating	Pratish Rao	Ultrasonic spray coating nozzle with handheld setup	Jan 2024 to Feb 2024
7	Spray coating evaluation on UAV components	Alec Chance/Pratish Rao	Controlled environment chambers/exposure conditions	Feb 2024 to May 2024
8	Review of coating performance	Entire team	Data/performance evaluation	July 2024 to Aug 2024

Deliverables

1) 10 samples/week
2) Weekly status update
3) Monthly and quarterly status report



Next Gen Battle Space ISR For Edge Devices

Next Gen Battle Space ISR For Edge Devices –
aka "KisMORE"

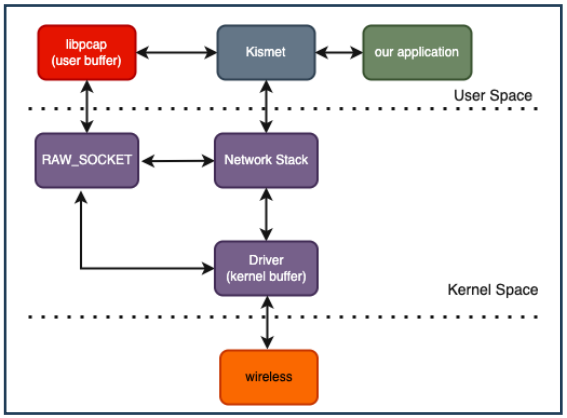
Ryan Andrew West
Associate Director of Research –
Cyber Defense & Cyber Security
Missouri Institute for Defense & Energy

David I. Rinck
LEAD SOFTWARE ARCHITECT
Missouri Institute for Defense & Energy

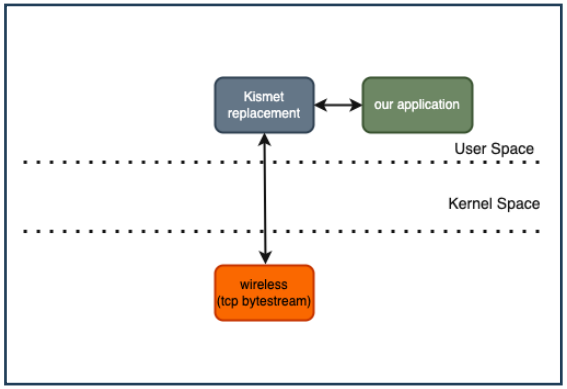
Motivation – SOTA RF survey tools such as Kismet work relatively well when used in specific frequency bands to detect very specific data types but fall short when detecting multiple data types from large numbers of devices on many frequencies.

Proposed Solution - To redevelop the Kismet stack reducing the operating system's exposure to data traffic generated during EM surveying by offloading packet inspection tasks to Field Programable Gate Arrays built into commercial SDR boards.

Current data flow using Kismet for RF survey



Data flow of proposed "KisMORE"



Next Gen Battle Space ISR For Edge Devices

Our design process is pretty standard.

Q1
- Acquire hardware and recruit FPGA Dev
- Begin code development

Q2
- Test cycle one code
- Debug and continue code development

Q3
- Test cycle two code
- Debug and continue code development

Q4
- Test cycle three code
- Debug and integrate

Research possible solutions and hardware necessary to development.

Develop code using Agile like cycles.

Test software.

Integrate into standardized GUI.

KPP	Threshold	Ideal
No. of devices sensed/sec	100/sec	1000/sec
Frequency range	315MHz-5.8GHz	315MHz-5.8GHz
Instantaneous bandwidth	>100MHz	>500MHz

Bottom line… We are developing this software stack to sense higher quantities, of more devices, on more frequencies, with less latency compared to what is available in the current state of the art.