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TECHNICAL REPORT

Pulsed-Laser Single-Event Effects (PL SEE) Testing – A Practical Desk Reference

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This Pulsed-Laser Single-Event Effects (PL SEE) Desk Reference is intended to provide practical guidance to assist in planning for PL SEE test campaigns. This guideline document will provide the reader with guidance in both test development and execution, resulting in enhanced efficiency and use of facility time, while providing insights into avoiding common mistakes and pitfalls.

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15. SUBJECT TERMS

PL SEE Pulsed-Laser Single-Event Effects
SEU Single-event upset
SEL Single-event latch-up
ASET Analog single-event transient
DSET Digital single-event transient
RHBD radiation hardening by design
RHBP radiation hardening by process
SPA single-photon absorption
NLO nonlinear-optical
TPA two-photon absorption
LTVs library test vehicles

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1 PURPOSE AND SCOPE

This Pulsed-Laser Single-Event Effects (PL SEE) Desk Reference is intended to provide practical guidance to assist in planning for PL SEE test campaigns. This guidelines document will provide the reader with guidance in both test development and execution, resulting in enhanced efficiency and use of facility time, while providing insights into avoiding common mistakes and pitfalls.

This document is intended for scientists and engineers planning for, or considering, future PL SEE test campaigns. The target audience includes both novice and experienced radiation scientists, radiation engineers, test engineers, program managers, and students. It is particularly well suited for those with some particle beam SEE testing experience because the differences between heavy-ion and PL test approaches are noted frequently.

This desk reference is focused on test methodologies, that is, how to test, rather than SEE mechanisms. The document discusses both the capabilities and limitations of the PL SEE approach, including suggestions as to when, or if, PL SEE testing is appropriate. The important components of a PL SEE test setup are described, with guidelines on the appropriate choice of laser parameters for testing specific types of devices. Detailed discussions on device preparation and board design are provided.

These guidelines are intended for PL SEE users, rather than operators, or those wishing to design or build a PL SEE system; such details are beyond the scope of this document. A similar comment applies to such topics as PL SEE modeling, dosimetry, data analysis, and laser-ion correlation. However, this document will provide the reader with an extensive list of references for these more in-depth subjects, as well as the specific topics covered herein.

2 CAPABILITIES & LIMITATIONS OF PL SEE

For SEE studies, at the most fundamental level, the pulsed laser is a tool for injecting charge into semiconductor microelectronic and nano-electronic structures. A primary advantage of focused laser-based approaches over broad-beam heavy-ion testing lies in their spatial selectivity: the ability to pinpoint and characterize sensitive nodes of circuits, often leading to insights not readily extracted from other approaches [1]. Furthermore, these studies can be conducted without the concomitant damage associated with accelerator-based particle radiation sources. This chapter discusses the capabilities, benefits, and challenges associated with PL SEE testing and highlights the particular applications that can be targeted.

2.1 CAPABILITIES

PL irradiation produces:

- a well-characterized quantity of charge
- at a well-defined, highly-localized spatial position
- with a known charge deposition profile
- at a well-defined time.

Laser-based SEE testing approaches have exploited these unique characteristics to interrogate an ever-expanding range of phenomena in addressing challenges facing the radiation-effects community. A partial list of applications that have been addressed using PL SEE testing is given below.

- Sensitive node identification/mitigation
- Single-event upset (SEU) mapping of sensitive areas
- Logical-to-physical bit map generation
- Single-event latch-up (SEL) screening and mitigation
- Analog single-event transient (ASET) screening
- Digital single-event transient (DSET) characterization and mitigation
- Hardened circuit verification: radiation hardening by design (RHBD), radiation hardening by process (RHBP)
- Dynamic SEE testing
- Experimental test setup verification
- Software verification
- Complex circuit evaluation/error signature identification
- Basic mechanisms studies
- Model validation and calibration
- Fault injection studies

Both linear- and nonlinear-optical approaches are used for charge generation in semiconductor materials. Linear approaches are based on above-bandgap, single-photon absorption (SPA), with the absorption governed by the Beer-Lambert Law; nonlinear-optical (NLO) approaches are based on sub-bandgap, two-photon absorption (TPA). Schematic diagrams illustrating the SPA and TPA processes are shown in **Figure 2.1** [2].
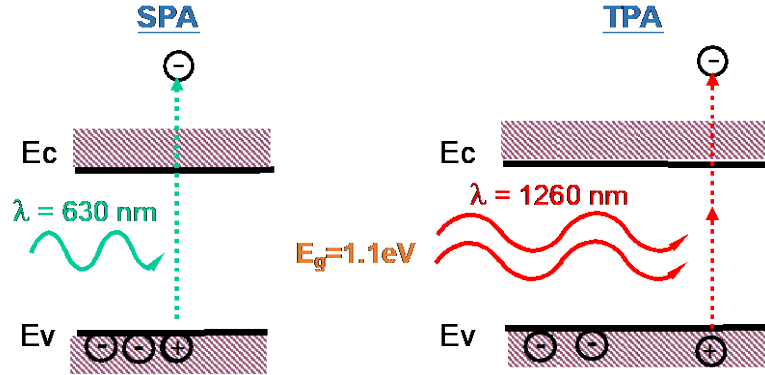
Figure 2.1. *Schematic representation of single-photon absorption (SPA) and two-photon absorption (TPA) processes in silicon. Ec and Ev indicate the conduction band and valence band, respectively.*

For SPA, a single photon with a photon energy above the material bandgap is absorbed, creating a single electron-hole pair. For TPA to be the dominant process, experiments are performed at wavelengths (typically denoted by λ) with photon energies below the energy bandgap of the material, such that SPA is negligible [2]. In TPA, two sub-bandgap photons are absorbed simultaneously, creating a single electron-hole pair. Details regarding the dependencies of the carrier generation process for SPA and TPA are discussed in **Section 4.2**.

In PL SEE, the sensitive region of a DUT can be accessed using either top-side or back-side, through-wafer irradiation, as is illustrated in **Figure 2.2**. Back-side probing can utilize either SPA, at wavelengths near the material band edge [3], or TPA, using sub-bandgap photons [4]. 1064 nm is a common wavelength used for back-side SPA excitation in silicon [3, 5, 6], whereas wavelengths in the range of 1250 nm to 1550 nm typically are used for TPA in silicon [7]. Other material systems often require different optical wavelengths. The factors that determine that proper choice of laser wavelength for the semiconductor under test are covered in **Section 4.2.1**.
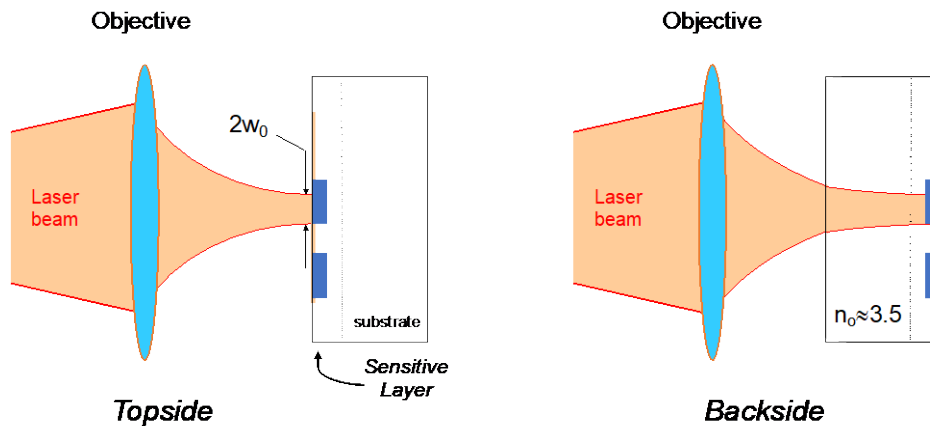
Figure 2.2. *Schematic diagram illustrating top-side and back-side, through-wafer irradiation. After [3].*

The choice of using either SPA or TPA for testing is determined by a range of factors, with primary considerations being laser availability and whether or not top-side access is impeded by excessive metallization. ASET screening in older-generation silicon bipolar technologies, for example, utilizes almost exclusively top-side SPA irradiation, but TPA could work as well. In contrast, recent-generation, highly-scaled technologies with flip-chip packaging necessarily require back-side, through-wafer irradiation. In general, a range of factors will determine the appropriate laser choice, wavelength, and test configuration, and whether TPA or SPA is the correct choice. These issues are discussed in the following chapters.

Today, PL SEE systems fall into two classes: custom-built and commercial. Custom-built systems typically are tabletop laboratory instruments with free-space optics. In recent years, commercial PL SEE systems have become available for both SPA and TPA excitation. Some of the commercial systems utilize fiber-optic delivery (both SPA and TPA), and generally have more compact footprints than tabletop systems. Open free-space systems typically offer greater experimental flexibility, but require qualified operators to maintain and operate, whereas commercial systems typically are more user friendly, turn-key systems requiring less user intervention.

Unlike particle-beam accelerator facilities, which tend to be geared toward external user access, PL SEE facilities generally are located in academic, industrial, or Government labs. The list of such facilities has grown rapidly in recent years. Many of the PL SEE laboratories are open to collaboration, and some provide external user access in different capacities, the details of which vary on a case-by-case basis.

In the following sections, the specific strengths and weaknesses of the PL SEE approach are discussed. Detailed discussions are presented in the following chapters.

2.2 BENEFITS

Spatial Selectivity. A unique characteristic that differentiates PL SEE from broad-beam accelerator sources is the intrinsic spatial selectivity of the focused laser pulse: the ability to deposit charge directly into sensitive nodes of a circuit with sub-micrometer spatial resolution. While micro-beam sources can be used for similar localized interrogation, their availability and particle energy ranges are severely limited. This spatial selectivity enables most of the applications listed in **Section 2.1**, and is used to identify, interrogate, and characterize sensitive nodes in circuits, and to generate 2-dimensional (2-D) SEE maps that reveal the spatial sensitivity of critical circuit elements. Visible (VIS) and near-infrared (NIR) laser pulses can be focused to less than a 1-μm full-width-at-half-maximum (FWHM) spot size, and ultraviolet (UV) laser pulses have been focused to 0.3 μm (details about focused beam sizes are given in **Section 4.4**). The position of the focused beam is controlled by a translation stage (see **Section 4.6**) with a spatial (X and Y) resolution typically of <0.1 μm. **Figure 2.3** shows one example where this spatial selectivity was exploited: propagation-induced pulse broadening was first demonstrated experimentally using focused top-side SPA irradiation in a partially-depleted (PD) silicon-on-insulation (SOI) inverter chain [8, 9]. In this example, spatial selectivity permits charge generation in any inverter along the chain, revealing unequivocally the effects of SET pulse propagation in a chain of inverters. This particular example is discussed in greater detail in **Section 6.5**.
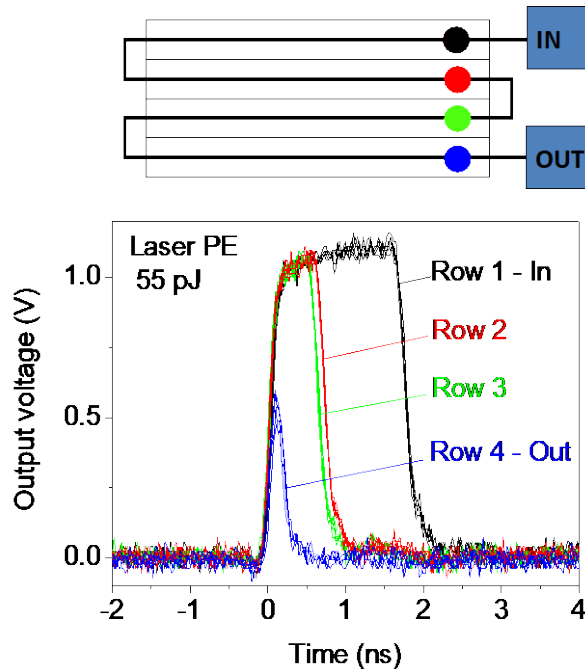
Figure 2.3. Schematic diagram of an inverter chain illustrating the snake-shape layout with the four laser strike positions indicated (color coded). Also shown are the voltage transients measured at the chain output of a 130 nm PD SOI device as a function of the laser strike position, illustrating the utility of PL SEE spatial selectivity. After [9].

Lack of Radiation Damage. A significant advantage of optical techniques is their inherent lack of radiation damage. This characteristic permits repeated testing of parts without total-ionizing dose (TID) degradation or displacement damage, and can be especially useful in mechanisms studies, for example, which often require repeated probing of a single part, or even a single transistor. To be clear, however, intense focused laser pulses can damage semiconductor devices through other mechanisms [10] but these damage thresholds can mostly be avoided by limiting the intensity of the focused laser.

Laboratory Instrument. In contrast to the large facilities that house particle-beam accelerators, the vast majority of PL SEE setups are table-top instruments located in smaller laboratories. This provides easy access for owners and collaborators, resulting in ease of test planning and flexibility not offered by accelerator facilities. With PL SEE testing the experimental dynamic is change from one of 'collecting as much data as possible while beamtime is available', to one in which series of experiments can be planned, adjusted, and repeated as needed.

Complementary to Broad-Beam Heavy-Ion Testing. PL SEE experiments provide information that is complementary to that obtained by broad-beam heavy-ion data alone. This is due, in a large part, to the spatial selectivity noted above. Laser SEE probing specifically takes advantage of this spatial selectivity to interrogate details of, and better understand, circuit responses to localized ionizing radiation. When used in conjunction with heavy-ion and/or proton testing, PL SEE leads to information and insights that are difficult to extract from broad-beam data alone. The list of PL SEE applications in **Section 2.1** is a direct consequence of the complementary nature of PL SEE.

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Laser Pulse Energy / Laser-Equivalent LET Adjustment. The LET spectrum available at particle accelerators is discrete, whereas the laser pulse energy and, by extension, the laser-equivalent LET (LET_L), can be adjusted continuously with high resolution. This continuous adjustment obviates the need for angle-tuning of the DUT, a method used to fine-tune the incident ion LET. In most PL SEE systems, the LET_L can be made significantly larger than the LETs that are available from either terrestrial accelerators or from the natural space environment. This feature provides extra margins for PL SEE part screening or part qualification and is one of the advantages that PL SEE testing has over energetic particle testing. The differences between heavy-ion and PL testing in terms of adjusting the LET are discussed in **Section 3.1.2**.

Part Screening. PL SEE testing is an effective and established tool for screening parts for space missions and can often be used to reduce heavy-ion testing, and sometimes to eliminate heavy-ion testing entirely. Screening for acceptance or rejection of a part involves evaluating its SEE response at a particular LET. In PL testing, the laser can be tuned to a specific LET_L and, if this value is set to a target LET metric for a program, part qualification decisions can be informed by the screening results. PL SEE part screening applications are discussed in more detail in the sections below.

2.3   LIMITATIONS AND CHALLENGES

Optical Access. PL SEE testing differs from the broad-beam heavy-ion testing in significant ways. In terms of DUT preparation, a primary consideration is optical access to the silicon, since laser light cannot pass through metal and other opaque materials. Optical access can be blocked by back-end-of-the-line (BEOL) metallization, packaging, board design, or opaque coatings (usually on the back surface). This means that appropriate preparation of the device under test (DUT) is essential for a successful PL SEE test. For top-side illumination the package generally needs to be de-lidded. For back-side illumination the substrate must be polished to a "mirror finish". For through-wafer illumination, thinning generally is not necessary unless the part is fabricated on a highly-doped substrate; in that case thinning to <100 μm typically is required (depending on the doping level). If parts are expected to undergo both back-side laser and back-side heavy-ion testing, thinning generally will be necessary for the heavy-ion testing and, with an additional polish (not required for heavy-ion testing), those parts also can be used for back-side laser testing. DUT preparation for PL SEE is discussed in greater detail in **Chapter 3** and **Chapter 5**.

Laser-Ion Correlation. The charge deposition profile for PL irradiation is different from that of heavy ions (or protons), and this can make correlating or matching the SEE responses between the different radiation sources (*i.e.*, laser-ion correlation) challenging. Nonetheless, an empirical correlation approach has proven valuable for such studies involving a variety of SEE phenomena [11-16]. This approach uses existing heavy-ion data to provide a correlation factor that converts a laser parameter (*e.g.*, pulse energy) to LET. With this correlation factor, heavy-ion response can be predicted in the same DUT under different operating conditions or in related DUTs. The main drawbacks for this approach are that the conditions used for determining the correlation factor must be replicated when doing subsequent testing (for examples, see **Section 6.2.6** and **Section 6.4.6**) and that existing heavy-ion data are required. Another approach involves tuning the LET_L to the prescribed heavy-ion LET and reproducing the heavy-ion SEE response without the need for existing heavy-ion data [17-19]. While the predictive aspect of this approach is attractive, the intrinsic differences in charge generation profiles between lasers and ions imply that only certain PL testing configurations are appropriate, and details about the testing geometry and DUT are required for accurate estimation of LET_L (see **Section 4.2** and **Section 4.3**). With these various challenges, laser-ion correlation continues to be an active area of research.

Dosimetry. For quantitative measurements, including laser-ion correlation studies, accurate dosimetry is essential. PL SEE dosimetry is not trivial, and procedures for reliable, reproducible PL SEE dosimetry for TPA have been developed only recently [20], and implementation is not widespread. PL SEE dosimetry can be challenging, but necessary for quantitative, reproducible measurements (see **Section 4.1** for details).

Cross-section Determination. Cross-section determination is a subset of laser-ion correlation, so all the challenges noted above are applicable here. The process of measuring a laser cross-section curve (*e.g.*, area vs. laser pulse energy) is straight-forward, in principle, but tedious and time consuming in practice, especially for larger devices, with various practical challenges that complicate the process [6, 21]. Once a laser cross-section is obtained, converting that to an equivalent heavy-ion cross-section can be challenging without input from heavy-ion measurements. Since cross-section vs. LET curves are needed for error rate calculations, it is generally accepted that, in most cases, heavy ion and proton test data are required for error-rate prediction.

Angle of Incidence. Due to a variety of reasons (see **Section 3.1.2** for details), PL SEE measurements are almost exclusively performed at zero-degree incidence (*i.e.*, with the laser beam normal to the die surface). Limited angular tuning to vary the effective LET is possible, but rarely implemented since the LET_L is easily adjusted using optical manipulation (see **Section 4.3**). This becomes a limitation, however, for investigations of RHBD circuits employing redundancy such that dual-node strikes are required for upset [22]. For such circuits, grazing-angle (near 90-degree incidence) ion strikes are required to fully evaluate the device sensitivity; such grazing-angle irradiation is not possible with optical techniques.

Highly-Scaled Devices/Advanced Packaging. Recent-generation, highly-scaled devices can represent challenges for radiation testing, with each new technology presenting unique challenges for both laser and particle-beam test approaches. For PL SEE, these typically are addressed on a case-by-case basis and depend both on the particular technology node, the packaging constraints, and the end goals of each investigation. In many cases, concerns about laser-based probing of highly-scaled devices are unfounded, such as when back-side access is available: optical injection through the substrate into the active regions of the device is possible, permitting interrogation of the most highly-scaled devices. One example is the back-side irradiation of a 90 nm SOI SRAM: the charge deposition can be described by a simple overlap integral, and quantitative agreement between laser and ion is obtained [23]. Another approach involves using specially designed test structures, measuring charge-collection transients in single transistors has been demonstrated for highly-scaled (50 nm) silicon on insulator (SOI) transistors [24, 25]. For many highly-scaled bulk devices, such as recent generation bulk FinFET technologies, SEE is driven by charge deposited in the substrate; in such cases, charge injection by a laser pulse can reproduce the effects of heavy-ion irradiation quite well. For emerging technologies, such as the gate-all-around transistor, the potential applicability of PL SEE is to-be-determined. For testing highly integrated structures, such as 2.5/3D designs, the utility of PL SEE approaches is expected to be limited. The approach for addressing 2.5/3D structures is expected to be similar to that presently used for advanced ASICs, utilizing library test vehicles (LTVs) for evaluation of the various radiation-hardened library elements, rather than attempting to test the final manufactured product. For future 2.5/3D designs, to the extent that LTV design and evaluation remains part of the flow, PL SEE testing should remain relevant.

2.4 Target Applications for PL SEE

The PL SEE approach is complementary to heavy-ion testing and is often used in conjunction with a heavy-ion test campaign, although in other cases it is used in a stand-alone fashion. Various examples of when PL SEE is appropriate are given below. Each of these is discussed in more detail in the following sections and specific case studies are provided in **Chapter 6**.

Basic Mechanisms in Transistors and Simple Devices.   Because of its inherent spatial selectivity and lack of radiation damage, PL SEE is a valuable tool for investigating the basic mechanisms of charge deposition and collection. SEE mechanisms often are complicated, and typically details are not revealed in the first pass. Having access to a PL SEE system opens up the possibility of repeatedly revisiting an experiment, adjusting parameters, and exploring different parts of the parameter space, to zero in on details that might otherwise be missed.

SEU/SET Mechanisms in Circuits.   Similar to investigations on single transistors, the spatial selectivity of PL SEE is key to investigating the consequences of ionizing events in integrated circuits (ICs). Whether investigating SET propagation in digital circuits, the SET response of linear circuits, or the complex error signatures of a recent-generation system on a chip (SOC), the spatial selectivity of PL SEE provides insights not possible with broad-beam particle irradiation sources.

RHBD/RHBP Evaluation/Validation. For the same reasons as above, PL SEE is commonly used to validate the performance of RHBD and RHBP circuitry. Side-by-side A/B comparisons under identical experimental conditions generally provide a direct measure of the relative hardness of the two circuits, without the need for heavy-ion testing.

ASET Screening. PL SEE can be very effective for SET screening, particularly in older-generation linear devices [26, 27]. The laser pulse energy can be adjusted to arbitrarily high charge injection levels, corresponding to effective LETs exceeding those induced by the natural space environment. This capability permits the quick and efficient determination of worst-case transients the part will see, information that can be used to inform the board designer for part acceptance, part rejection, or the implementation of mitigation. Beyond screening, the spatial selectivity permits accurate determination of the origin (location) of the worst-case transients, information that can be used to inform future designs, if appropriate.

SEL Screening. Rejection of a part whose LET threshold (LET_{th}) for SEL is below a program's target LET can save significant time and money in terms of both accelerator and TID testing. PL SEE screening of parts for SEL based on this type of accept/reject criterion has been used since the early days of the technique. During PL SEL screening, a part's susceptibility to SEL depends on its threshold relative to the laser's operating point: $LET_{th} < LET_L \rightarrow$ SEL, $LET_{th} > LET_L \rightarrow$ no SEL. Since the LET_L can be adjusted via the laser pulse energy (see **Section 3.1.2**), the LET_L value could be tuned to a target LET metric for a program (or above it for a more conservative approach) thereby informing part qualification decisions. Some programs accept parts based on laser-based SEL screening; others do not. Example case studies of PL SEL screening are given in **Section 6.1**.

Pre-Accelerator Test Setup Verification and Optimization. It is not uncommon for significant time (and money) to be lost at particle accelerators in evaluating and modifying the test hardware/software before the actual testing begins. Much of this effort can be performed at a PL SEE facility, permitting more beamtime to be dedicated to the actual test. This includes correcting and improving flaws in the test plan.

In addition, when testing a new part, surprises are not uncommon, and these are often revealed in a PL SEE test. Detecting surprises in advance of the particle accelerator test provides time to modify the test plan as necessary to accommodate for such surprises.

Post-Accelerator Testing. PL SEE interrogation is commonly used to better understand the unexplained results of heavy-ion tests. This is a common use of PL SEE in terms of supporting radiation hardness assurance efforts, and generally arises due to heavy-ion results that are inconsistent with expectations. The intrinsic spatial selectivity of PL SEE is used to locate, identify, and characterize the sensitive nodes responsible for the anomalous results.

Complex Circuit Evaluation. Accelerator-based testing of complex circuits, such as FPGAs, SOCs, ASICs, and microprocessors, often reveals unanticipated error signatures; there are almost always surprises [28]. The spatial selectivity of PL SEE permits separation and independent evaluation of different error signatures arising from different functional blocks. Observing these first in the laser lab provides test engineers with the opportunity to modify the test approach, as necessary, without wasting precious beam time trying to sort out what's going on. PL SEE is suitable for both pre- and post-test evaluation.

2.5 SHOULD YOU USE PL SEE?

The question often arises as to when the use of PL SEE should be considered. While there clearly are pros and cons associated with laser testing, PL SEE testing can provide value in many circumstances, and this guideline document will help understand what PL SEE testing can and cannot accomplish**.** Most generally, PL SEE is a tool for understanding the error modes of the device under test, whether those error modes arise from SEU, ASET, DSET, SEL, SEFI, or SEB. However, it is not (yet) an acceptable method for measuring quantitative SEE cross-section curves, which are used for predicting error rates in space. An important function of PL SEE is to reveal spatial and temporal information about SEE sensitivity.

Below are a guiding set of questions that should be addressed prior to considering the use of PL SEE testing. Answering these questions with a 'yes' suggests that PL SEE testing could prove valuable.

- Does your experiment require spatial sensitivity? Do you have a need for generating a spatial map showing the locations of SEU or SET?

- Does the laser beam have access to the active regions of the device, either from the top side, or through the wafer from the back side? If not, can the board/DUT be modified such that optical access is possible?

- Do you want/need to trouble-shoot your experimental setup prior to ion testing?

- Do you have a complex device that is expected to exhibit an array of error modes, such that it would be useful to better understand them prior to heavy-ion beamtime?

- Do you have a complex device that, in previous heavy-ion testing, exhibited a complicated array of error signatures, and it would be useful map out the physical origin of the various different error modes?

- Do you require information complementary to that obtained in heavy-ion tests?

- Do you have questions regarding prior test results that need to be clarified with additional experiments?

- Are you in need of a timely, cost-effective approach for SEL or ASET screening?

- Do you require a physical correlation of fault injection locations with device output?

- Do you require temporal information on SEE propagation in your device?

- Are you okay with not being able to extract cross-section measurements for event rate prediction?

3 EXPERIMENTAL DESIGN

This chapter presents a comprehensive list of issues that must be considered when contemplating a PL SEE test campaign. The beginning is geared towards engineers familiar with HI SEE testing by pointing out the similarities and differences between HI- and PL SEE Testing. This is followed by a detailed discussion of issues associated with performing PL SEE testing for the novice so that pitfalls can be avoided.

3.1 DIFFERENCES BETWEEN HEAVY-ION AND PL SEE TESTING

PL testing has some things in common with heavy-ion testing, but there are also significant differences. The user must be aware of these differences when planning a PL SEE test. This section describes some of the differences and similarities between PL SEE and accelerator testing. Typical PL SEE and accelerator testing facilities are shown in **Figure 3.1**.
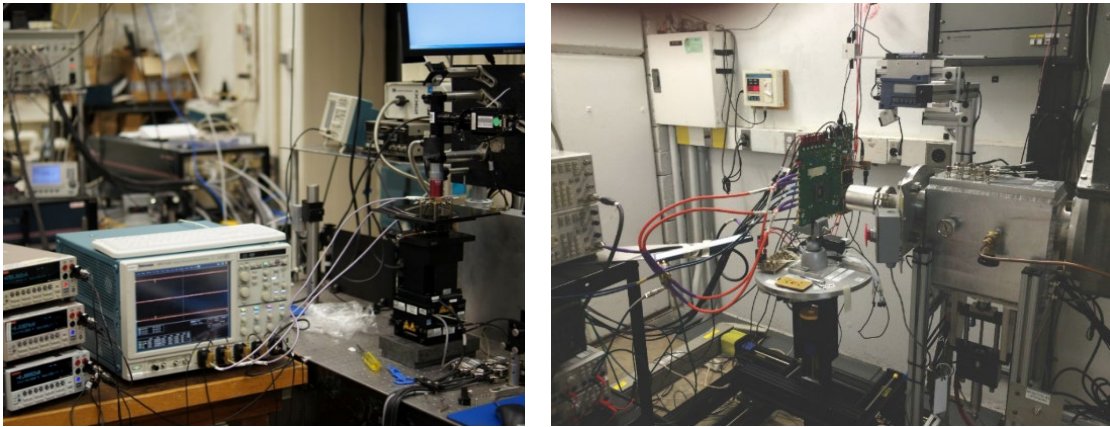
Figure 3.1. Photograph of a typical PL SEE setup (left; U.S. Naval Research Laboratory) and a broad beam heavy-ion facility (right; Texas A&M Cyclotron). Note that due to the lack of radiation exposure concerns, the operator/user is typically stationed adjacent to the DUT for the PL SEE testing.

3.1.1 Facility

Exposure. Precautions against radiation exposure are different for accelerator testing and PL testing. Accelerator testing with both protons and heavy ions often is performed in air, and it is necessary to avoid exposing personnel and equipment to the beam, and also to the secondary particles, especially neutrons, that are emitted when the beam activates materials in the test chamber. In fact, there are very strict government regulations requiring all personnel to be outside the chamber during testing. Thick concrete blocks and heavy metal doors shield the test personnel from the radiation. Accordingly, the distance between the location of the DUT at the end of the beam-line and the location of the test personnel and test equipment can be 100 feet or more. It is, therefore, necessary to use sufficiently long cables, which must be shipped to the accelerator test facility. Because of the radiation danger associated with accelerator testing, special training, sometimes quite extensive, is required at many facilities to qualify as a radiation worker.

Radiation exposure is not an issue for PL testing. Since the exposure of personnel and equipment to radiation are of no concern, the operator and user are typically stationed adjacent to the DUT (see **Figure 3.1**). The primary danger at a PL facility is from the beam itself as high-intensity optical pulses are capable of damaging eyes and burning skin. However, these dangers are easily mitigated by optical shielding, such as adding baffles, enclosing the beam in light pipes, and requiring personnel to wear the appropriate eye protection and clothing. Eye-protection goggles must be rated to reject the light with the specific wavelength being used. The laser facility should keep the beam at waist level to minimize the danger due to scattered light.

Travel. Travel is a reality for heavy-ion testing, and cross-country or international travel often is required. One potential advantage of PL SEE testing is that no travel is required for in-house facilities, which are becoming more and more common. Any organization involved in a significant amount of SEE testing should consider purchasing a PL SEE system for easy access, rapid turnaround, and useful information not available from ion testing. Being able to avoid the logistics associated with travel, as well as the ability to dry-run and optimize your experimental setup prior to ion testing, are attractive features afforded by an in-house facility.

3.1.2   Irradiation

Varying the LET. The LET deposited by heavy ions is proportional to the square of the charge on the ion and inversely proportional to its kinetic energy. Therefore, in an ion experiment, the LET can be changed by changing either the ion species or the kinetic energy of the ions. The kinetic energy can be adjusted either by tuning the accelerator, or by placing degraders in the beam. The accelerator operators usually take care of tuning the beam energy (in some cases, this takes a considerable amount of time – several hours – to tune the beam). Ion beam energies are usually measured with ionization chambers by the experimenters, with the help of the accelerator personnel, if needed. Another way to change LET is by changing the angle of the incident ion relative to the surface of the DUT. When an ion enters a device at an incidence angle Θ (relative to the normal), the LET is increased by $1/\cos(\Theta)$, and the cross-section is reduced by $\cos(\Theta)$.

In PL SEE, the laser-equivalent LET (LET_L) is proportional to the laser pulse energy for SPA (see **Section 4.2.2**) or the square of the laser pulse energy for TPA (see **Section 4.2.3**). Consequently, varying the pulse energy is equivalent to changing the ion LET and, since adjustment of the pulse energy is straightforward, this provides advantages in terms of continuous tunability, greater flexibility, and speed. Further, PL testing can produce LET_L values exceeding those produced at terrestrial heavy-ion test facilities. The method for adjusting the LET_L and the typical ranges encountered are discussed, in detail, in **Section 4.3**.

Beam Delivery & Uniformity. There are significant differences between heavy-ion and PL testing regarding the delivery of the beam and the concept of beam uniformity. For broad-beam ion testing, the DUT is irradiated by a large area beam (typically several inches in diameter) and the working distance between the beam exit window and the DUT can be several inches. Beam diameter and uniformity are of paramount importance for heavy-ion SEE testing because non-uniformities can affect the determination of SEE cross-section, complicating the analysis and distorting the results. Beam uniformity is achieved by proper alignment, and by inserting into the beam a thin foil that scatters the particles and broadens the beam to produce one with a smooth Gaussian shape. The center of the Gaussian beam is relatively flat over a distance of a few centimeters, sufficient to encompass the DUT. The uniformity of the beam is

measured by placing a radio-chromic film at the location of the DUT or to position four secondary electron emission monitors around the perimeter of the beam for continuous monitoring.

For PL testing, a focused laser spot with a nominal diameter of ≤1 μm (FWHM) is achieved by sending a laser beam into a microscope objective that focuses the beam onto the DUT (see **Section 4.1** for details about the optical layout). The working distance between where the beam exits the objective and focuses on the DUT is typically 10-20 mm. This limited working distance, shown in **Figure 3.2**, is a necessary tradeoff to achieve a small spot size. Ion-beam uniformity does not have a direct analog when considering PL testing because the laser beam is focused on a single location. While there are certain requirements for the input beam to the objective (see **Section 4.4**), these only serve to focus the beam effectively. Only in the case of a laser beam being scanned across the surface of a DUT is there a tenuous connection to beam uniformity, *i.e.*, the charge deposition profile generated by the laser beam should remain constant as it scans the surface. This can be achieved by ensuring that the various laser parameters that determine the charge profile do not change significantly during scanning. The methods for monitoring these various parameters are discussed in **Section 4.1**.
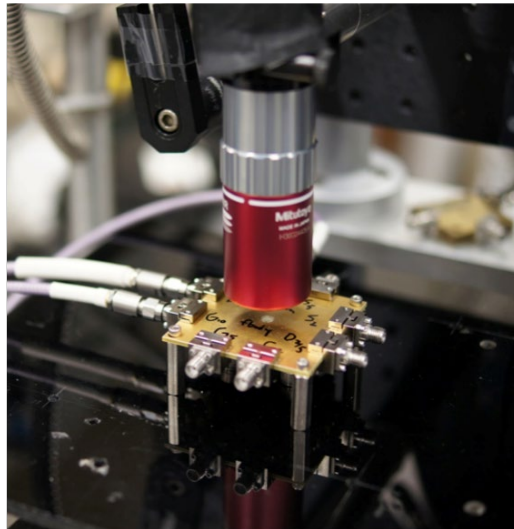
Figure 3.2. *Photograph of a long working distance 100x objective used to focus the laser beam onto the DUT.*

Carrier Distribution. The charge deposition profile, or carrier distribution (CD), generated by a heavy ion is different from that generated by a laser pulse, as depicted in **Figure 3.3**. A typical heavy-ion CD possesses an axial size (or depth) that can range between 50 μm and 200 μm, depending on the ion and its kinetic energy. The lateral size of the CD is typically 0.1 μm, which yields an aspect ratio (the ratio of axial to lateral size) around 1000:1. When focused with a high-magnification 100x objective, the laser-generated CD typically possesses a lateral size of ~1 μm and an aspect ratio closer to 10:1 (see **Figure 3.3**). These characteristics depend uniquely on a variety of parameters that are tied to the particular optical setup being used. The dependencies of the laser-generated CD on these parameters (*e.g.*, laser wavelength, microscope objective, input beam size, semiconductor under investigation) are discussed in **Chapter 4**. While the differences in the CDs for the two sources can make correlating results between

laser- and heavy-ion-testing difficult, this has not prohibited successful application of PL SEE testing (see **Section 2.4**).
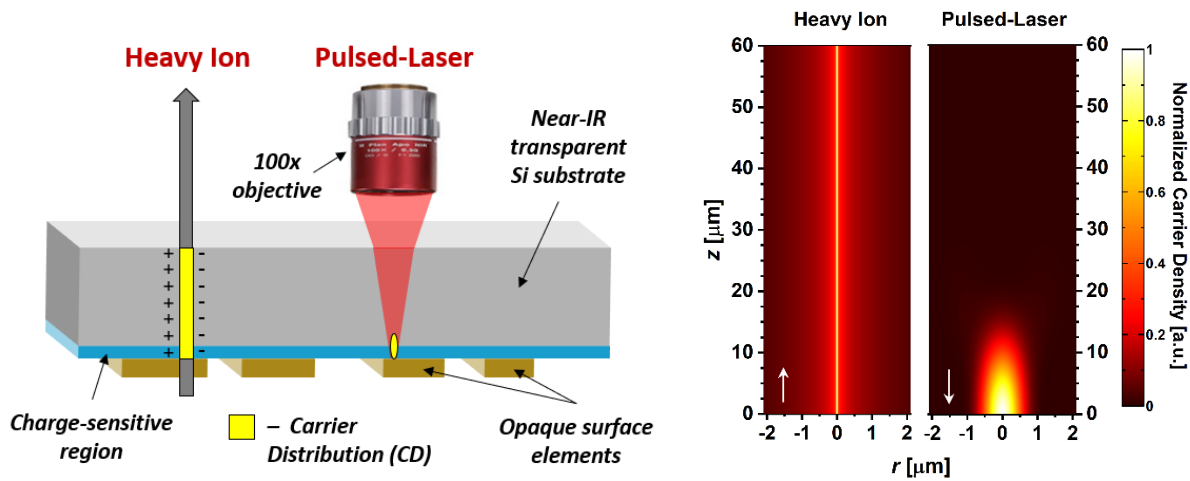
Figure 3.3. *Depiction of the carrier generation processes in a DUT via heavy-ion irradiation and back-side TPA-based PL excitation using a 100x objective (left). Calculated CDs produced by each irradiation source are given on the right, with the axial (z) and lateral (r) dimensions shown. The CDs are normalized to their respective peak carrier densities and the heavy-ion CD is plotted on a log scale. The arrows denote the direction of the irradiation. After [29].*

Non-Normal Incidence. In addition to varying an energetic particle's angle of incidence to tune the effective LET, there are other reasons for utilizing non-normal incidence in energetic particle experiments. These include probing the basic physics of ion-induced charge collection in different technologies and probing RHBD circuits that utilize spatial redundancy. As an example of the latter, for an upset to occur in a DICE cell, an ion has to pass through, or very close to, two physically separated nodes [30]. The probability of an upset can be determined through grazing angle experiments at heavy-ion facilities.

For PL SEE, varying the angle of incidence of the laser beam is not practical. The limited working distance of the microscope objectives prevents any substantive board rotation. Furthermore, refraction at the semiconductor interface places limits on the possible rotation angle. As noted above, these limitations have no impact on the ability to fine-tune the LET_L but grazing angle experiments to investigate RHBD circuits employing redundancy are not possible. However, if the two nodes comprising the redundancy are not too far apart, it is possible to deposit charge at the two redundant nodes in a DICE cell and cause an upset with a single laser pulse. This can be achieved either by increasing the size of the beam with the help of lower magnification lenses, or by focusing between the cells with a tightly focused beam and relying on diffusion in bulk technologies.

Flux. In heavy-ion testing, one deals with particle flux, which is the number of particles crossing a unit area in a unit time. The higher the flux, the more rapidly single events are registered. Ion beam fluxes are established by the ionization method used for the source. The flux can be measured with an ionization chamber prior to the start of SEE testing. The measured value is used as a reference for the secondary electron emission foils used to measure flux and flux uniformity during an actual run.

The equivalent metric for flux encountered in PL testing is the laser pulse repetition rate – each pulse is the equivalent of a single ion incident on a known location. The repetition rate of a laser itself generally is

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fixed (for thermal reasons), but there are various methods that can be used to step down the pulse repetition rate at the DUT. The key point is that the rate must be sufficiently slow to permit the DUT to return to equilibrium between laser pulses, but not so slow as to impact data acquisition and the time allotted for the test. Details regarding the role of repetition rate in PL SEE testing are given in **Section 4.5**.

Fluence. In heavy-ion testing, fluence is the number of particles per unit area (*i.e.*, the time-integrated flux). Single-event cross-sections can be calculated by dividing the number of measured events by the fluence delivered to the DUT. Ion experiments typically are conducted until sufficient events are measured or a target fluence is reached. The target fluence can be set such that the resulting limiting event cross-section is below the required specification for a given application.

In PL testing, pulses are delivered to a well-defined spatial position by focusing the laser beam (rather than over a particular area). Therefore, these is no exact analog to heavy-ion fluence for laser testing. To determine the event cross-section with a focused laser pulse, the beam must be scanned across the DUT while noting the regions that experience an SEE response. The cross-section would be obtained based on the physical areas in the DUT for which events were observed.

Ambient Light. Exposure of the DUT to ambient light during both heavy-ion and PL-light testing generally should be avoided. This is because the ambient light sometimes generates additional carriers that can affect SEEs. This can lead to a distortion of SETs in certain devices, for example. It is always a good idea to verify whether ambient light is affecting SEE measurements. During accelerator testing, the room lights are usually darkened. During PL testing, all sources of light, *especially* the illuminator used for imaging the chip, should be turned off. If it is not possible, or desirable, to turn all the room lights off, baffles should be positioned around the DUT to block any ambient light.

3.1.3   Devices

Semiconductor Bandgap & Doping. The electronic energy bandgap of a semiconductor is not a parameter that needs to be considered for heavy-ion testing. The ions generate electron-hole pairs with energies that far exceed the electronic energy bandgap (E_g) of the material, even for wide bandgap semiconductors, like GaN and SiC, as well as for insulators like SiO_2. It takes, on average, an energy of $3 \cdot E_g$ to create one electron-hole pair using heavy ions. In contrast, E_g is an important parameter for PL SEE testing, determining the laser wavelengths required for testing a given material, or, conversely, whether or not a certain test can be performed with a given laser system. Discussions on wavelength selection for different bandgap semiconductor materials are given in **Section 4.2.1** and **Section 5.1**.

Highly doped semiconductors, such as n+ doped regions in devices, have no impact on heavy-ion testing; the interaction between the incident ions and the valence electrons is not affected by the presence of free electrons and holes. In contrast, doping can play a role in PL SEE testing, because the free electrons in the conduction band can both modify the E_g of the material and lead to a kind of absorption termed "free carrier absorption." While this additional absorption mechanism does not produce any SEEs, there can be ramifications on PL SEE testing and these are discussed in **Section 5.1**.

Sample Preparation – Thinning and Polishing. Sample preparation goals are not necessarily the same for heavy-ion and PL SEE testing. When testing with high-energy ions, little sample preparation is required, while the use of low-energy ions may require deprocessing of the package (top-side access) or thinning (back-side access). By contrast, sample preparation is one of the more significant aspects of PL SEE testing. Unless one is starting with a bare chip, it is always necessary to remove some of the packaging material,

since the light cannot penetrate metal, plastic, or ceramic. The need for thinning is determined on a case-by-case basis, depending both on the nature of the substrate and the experimental details. Additional details associated with part preparation, with emphasis on the various challenges associated with different part types, are discussed in **Chapter 5**.

3.1.4   Testing

General Alignment. Broadbeam heavy-ion testing provides a large area beam and so lateral alignment typically consists of grossly aligning the DUT with some sort of visible guide, such as a laser beam. The axial position of the DUT is chosen mainly based on ease of accessibility, but the approximate position must be noted to accurately estimate the LET profile.

By contrast, laser testing involves interrogating SEE-sensitive regions with sub-micron spatial resolution and so lateral alignment (X, Y) is critically important. This alignment is typically accomplished by using a microscope to visualize the focused laser beam on the DUT and using a computer-controlled translation stage to co-locate the beam and the region-of-interest (see **Section 4.1**). To this end, it is very useful to have a large-sized hardcopy layout of the chip available (in addition to a GDS-II file) and to be familiar with the orientation and the various regions. This helps facilitate locating the regions-of-interest and identifying the areas over which spatial scans (*i.e.*, acquiring SEE response data at specific spatial positions) will be performed. Fiducial points on the chip can help with navigation and can be used as starting points for PL SEE spatial scans. An example of this is given in **Figure 3.4**.
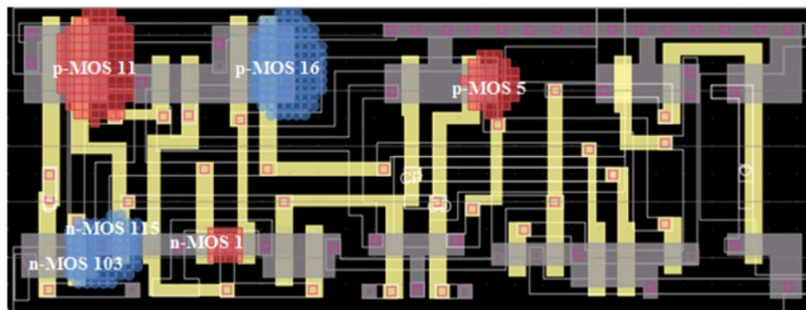
Figure 3.4. GDS file showing the layout for a D-Latch. The experimentally-obtained SEU-sensitive regions are superimposed on the layout. After [31].

Axial alignment (Z) is also important for laser testing because the magnitude of the charge profile depends on its position relative to the sensitive region (see **Section 4.2**). Axial positioning is usually done with respect to where the beam is focused on the surface, or silicon/ SiO_2 interface, of the DUT; this is often referred to as the Z = 0 position. This position is determined by properly focusing the beam (*i.e.*, moving the Z position of the translation stage) such that the minimum spot size is observed. This procedure should be done away from metal lines and other structures such that a clear, round, laser spot is evident. This Z = 0 position will not be the same at different X-Y locations unless the part is perfectly perpendicular to the focused beam. When performing large area spatial scans, if the axial position of the focused beam changes with lateral position, the magnitude of the SEE response could also change with position thereby making data interpretation difficult. This issue can be partly mitigated by correcting the angle of the device

by mechanically adjusting its tip/tilt (to make it perpendicular to the beam), but this is often an approximate adjustment. Ideally, this correction is done in software where the Z = 0 position is recorded for three X-Y coordinates (*e.g.*, the corners of the proposed spatial scan area) and interpolation is used to calculate the Z = 0 position for all other X-Y values.

Test Approach. Generally, the primary goal of heavy-ion SEE testing is to measure the event cross-section as a function of LET. For non-destructive SEEs, heavy ions having the highest LETs should be used first. The SEE cross-section should then be measured at several smaller LETs, until the threshold is determined. For destructive SEEs, to minimize the number of devices used, it is best to begin at low LETs, so that the LET threshold can be determined without significantly diminishing the DUT parts supply.

Locating SEE sensitive regions in a DUT involves scanning the device with respect to the focused laser beam. Such scans can be either manual or automated. The approach chosen depends on the particular details of any given DUT, as well as the goals of the test. For instance, manual scans may be the most time efficient if the operator has insight into which regions are expected to be sensitive. If these are unknown and a wide area must be surveyed, an automated scan is best. When performing testing on parts for the first time, lower magnification objectives (*e.g.*, 10x or 20x) should be used since they possess a larger field of view and produce larger focused spot sizes; this minimizes the time it takes to locate and identify SEE-sensitive regions.

After the SEE-sensitive regions have been identified, a higher magnification objective that produces a smaller spot size (*e.g.*, 100x) could be used to obtain detailed spatial information in the regions-of-interest. Once the desired spatial location has been determined, a testing approach can be taken that is similar to heavy-ion SEE testing: start testing at a high pulse energy / LET_L for non-destructive SEEs and at a low pulse energy / LET_L for destructive SEEs. Care should be taken to not operate at too-high pulse energies that may deposit too much charge into the sensitive region of the DUT.

Generally, there are four main knobs for adjustment that are utilized during PL SEE testing: pulse energy (or LET_L) and the three spatial dimensions, X, Y, and Z. Any combination of these parameters can be adjusted during an experimental scan and each combination can provide unique information about the SEE response of the DUT. Three of the most common types of scans that are performed during PL SEE testing are as follows: (1) an *E*-scan allows the energy (or LET_L) to be varied at a fixed position (X, Y, Z); (2) a *Z*-scan uses a fixed energy and lateral position (X, Y) but scans the axial position (Z); (3) a raster scan uses a fixed energy and axial position (Z) but varies the lateral positions (X, Y).

Stage Considerations. X-Y-Z translation stages are sometimes used for DUT positioning in heavy-ion testing. Once positioned, there is no need to move the DUT, and, therefore, no need for high-precision automated motion control. If the angle of the DUT relative to the beam needs to be changed to increase or decrease LET, the stages can accomplish the change in a matter of a few seconds between test runs.

A primary goal of PL SEE is to identify sensitive areas in a DUT, hence the requirement for precision, automated motion control. This generally takes the form of a precision X-Y-Z translation stage and details regarding stage specifications are given in **Section 4.6**. For 2-D or 3-D spatial scans, the required spatial resolution (or step size) is determined by a number of factors including the size of the area to be scanned, the estimated dimensions of the sensitive regions, the amount of time available for that particular experiment, the focused laser beam spot size, and the specific goals of that experiment. Large area, high

resolution scans are time consuming. While such scans certainly are possible, the longer the scan duration, the more important are parameters such as mechanical stability (see **Section 3.2.1**), laser stability (see **Section 4.3**), and thermal stability (see **Section 3.2.3**) in the laboratory. Such issues should be discussed as part of the test planning process.

Software. For accelerator testing, the software is designed based on the part type and the specific tests being performed. For testing an SRAM, for example, data is first written into the memory, and, after the SRAM is exposed to the beam at a predetermined fluence, the beam is stopped, the memory is read, and the number of errors counted. Handshaking can be implemented to handle destructive events, such as latch up. In all cases, the number of SEEs detected is stored for later analysis.

The highly localized nature of PL SEE irradiation requires different test protocols than for heavy ions. Like for heavy-ion testing, the details depend on the part type and the specific tests being performed. Handshaking between the data acquisition hardware (oscilloscope, computer, etc.) and the experimental equipment (translation stage, shutter, etc.) is required for many types of PL SEE experiments. Computer control over the laser pulse energy (or LET_L) is possible and should be included in the experimental test software (see **Section 4.3**). Communication with the facility operators typically is necessary to implement various computer controls into the test software. Infinite variations are possible here; such details need to be coordinated in advance with the facility test team (additional details are given in **Section 4.7**). Finally, the data acquisition software should generate a log file that includes all relevant information, including the X-Y-Z coordinates of the stage for each data point, calibration signals from various beam monitors, the bias conditions of the DUT, the run number, the device type and manufacturer, and the outcome of each interrogation (SEE, yes/no, etc.).

Data Logs. For heavy-ion testing, the data log usually contains columns for the following: date, facility, run number, time, device ID, device manufacturer, device type, ion species, angle of incidence, LET (or energy for protons), flux, fluence, DUT conditions such as bias and temperature, file identification, the number of events, and finally any relevant comments. For PL SEE testing the data log may look as follows: date, facility, run number, time, device ID, device manufacturer, device type, laser wavelength, SPA or TPA, laser pulse energy, laser pulse width, focused laser spot size, microscope objective used, scanning information like step size, speed, and area covered, DUT conditions such as bias and temperature, effects observed, and any relevant notes. Additional optical data that vary with each experimental setup, are generally required as well. These might include any filters used to modify the pulse energy or details of the focusing arrangement beyond the objective used (beam input diameter and beam divergence, for example).

## 3.2   CONSIDERATIONS FOR PL SEE TESTING

This section discusses numerous aspects of PL SEE testing involving mounting the DUT to a stage, handling cables, and reducing vibrations, all of which could negatively impact the test if not done properly. Those familiar with HI SEE testing should take special note because of the differences between PL SEE testing and HI SEE testing.

3.2.1 Mechanical Stability and Mounting

Mechanical stability is critical to success in PL SEE measurements. While most details in this regard are handled by the different facilities, it is important for users to understand various issues when designing their test and test board.

Mechanical Stability. For PL SEE, to optimize mechanical stability, boards typically are mounted horizontally, although vertical mounting has been used. With the optical beam approaching the DUT vertically, either from below the DUT or from above the DUT, the gantry supporting the optics, which includes the focusing lens, illumination lamp, and camera, must be designed for maximum mechanical stability, and firmly secured to the optical table (see **Section 4.1** for details about the system layout). The precision X-Y-Z translation stage used to position the DUT must be securely mounted to the optical table. The bolts securing the stage to the optical table should be very tight to avoid unwanted movement. The optical table itself should be isolated from vibrations in the building by vibration isolation legs. Such details regarding the mechanical stability of the beam delivery system and translation stage are handled by the facility.

Securely mounting the DUT, or the board containing the DUT, to the stage is essential for eliminating vibrations. This is done through sturdy board design and mechanically sound mounting. Boards should be mounted at four points for stability. Avoid the "diving board" effect involving boards mounted only on one edge, or through a single connector on a mother board. An example of a "diving board" configuration for a daughter board is shown in **Figure 3.5**. Such designs can be problematic, especially for the highest resolution measurements. In this particular example, for measurements on a large-area power device, this configuration was sufficiently stable.
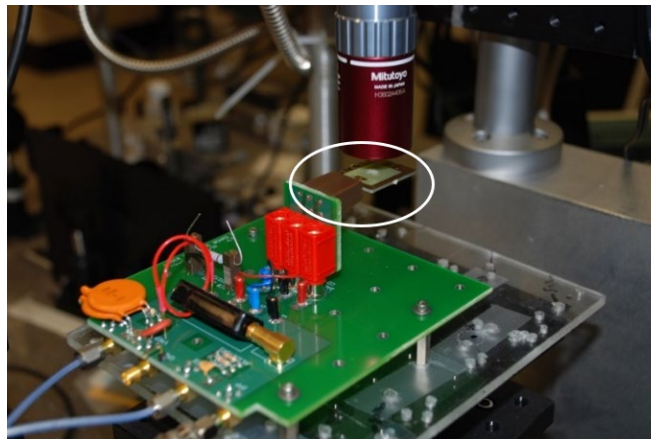
Figure 3.5. *Example of a board setup for TPA PL SEE test of a power MOSFET test illustrating a "diving board" design. The diving board is highlighted by the white oval.*

The size of the board can be an important parameter for laser testing. This is, in part, because the mass of larger boards can overwhelm some precision X-Y-Z stages, limiting their ability to function properly. In addition, larger boards can present mounting and stability problems. If the board is much larger than the stage, the edges of the board may be unsupported, leading to instabilities. Such issues can be addressed through creative mounting schemes but are better avoided from the outset. None of these factors are

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issues for smaller boards. Consequently, the size and weight of test boards should be minimized so that they can be accommodated by the stage, optical gantry, and focusing objective.

Mounting the Test Board. As mentioned above, boards are typically mounted horizontally and secured to the top of the translation stage. The top of the stage normally has an array of screw holes, with distances between the holes being 1" in both X- and Y-directions. In most cases, it is not practical to place the board containing the DUT directly on the surface of the stage because of other components and wires attached to the board. A way to solve this problem is to use standoffs, which attach the board to the holes on the stage. **Figure 3.5** shows how these standoffs provide sufficient room under the board to accommodate attached wires. If these standoffs directly connect the board and the stage, the holes on the board need to be consistent with the 1" spacing grid of holes on the stage. This might pose difficulties because metal traces are placed within the board that could interfere with drilling holes in certain positions on the board for attaching to the standoffs. Adapter boards, such as the plexiglass adapter board shown in **Figure 3.5**, can be used to accommodate test boards with irregular hole patterns. Holes should be incorporated into the board at the design stage with the understanding that each facility will have different requirements for mounting boards.

Additionally, the position of the DUT on the board can matter as well, depending on the size of the board and the specifics of a given facility. For larger boards, this means that the DUT often must be offset from the center of the board and mounted closer to one or more edges. This restriction is due to the physical size limitations associated with the stage and optical setups. Different facilities have different requirements for acceptable board sizes and for the distance of the DUT from the edge of the board. A photograph of a large test board mounted in the PL SEE system at the U.S. Naval Research Laboratory is shown in **Figure 3.6**. Note that the DUT is offset from the center of this rather large board which accommodates the maximum DUT-to-board-edge distance of 5.5".
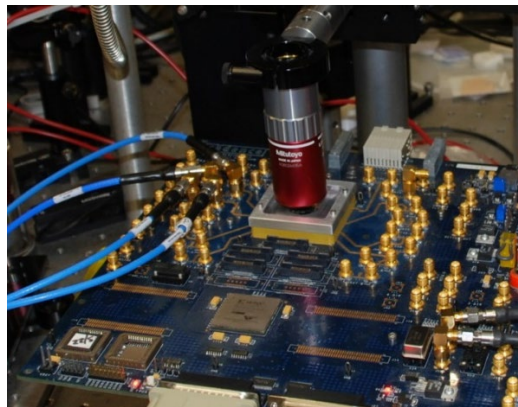
Figure 3.6. *Photograph of a representative TPA PL SEE test setup and focusing configuration.*

It is critical to ensure that there are no impediments to the microscope objective getting close to the DUT, such as large capacitors that could physically impede the objective. The facility will supply the objective dimensions and the associated working distances. A general rule of thumb is that the working distance of common high-magnification, long working distance objectives is in the vicinity of 12 mm. Further, there should be no obstructions between the objective and the sensitive area on the DUT since any such objects

could interfere with the focusing laser beam. **Figure 3.5** and **Figure 3.6** provide good examples of boards that offer unobstructed access to PL SEE testing.

3.2.2   Cabling

Cables conducting the electrical signals from the DUT to the test equipment and power supplies are issues at both accelerator and laser testing facilities, but the issues are quite different.

Cable Length.   At accelerator facilities, the DUT is usually remote from the test equipment to eliminate radiation exposure to personnel. Since much of the test equipment is placed outside the test chamber, long cable runs and/or specialized setups are required to gather the data. PL SEE testing, being free of harmful radiation, does not have these problems and test equipment can be situated close to the test setup. While minimizing cable lengths is desirable, placing test equipment directly on the optical table where DUT testing occurs should be avoided. Test equipment frequently contain fans or keyboards that will cause vibrations that can affect the stability of the DUT. By placing the equipment on a separate table, the worst of the vibrations can be avoided. It is important when travelling to a remote site for laser testing to know how long the cables must be if the test equipment is placed on a separate table. A good estimate is about 3 to 6 ft.

Another issue for heavy-ion testing is that there should be sufficient slack in the cables to allow the DUT to be rotated to different angles. Although the board containing the DUT is usually affixed securely to the stage so that it does not move when the stage is rotated, extreme stability is not important because the DUT is irradiated with a broad beam. In PL SEE testing, the board is not rotated, and so significant cable slack is not required. However, the cables should have sufficient slack, so they don't limit translational movement of the DUT during scanning leading to potential misalignment. This slack also serves to limit the transmission of any potential vibrations from the test equipment to the DUT.

Cable Stability.   Cabling can present a couple of issues involving mechanical stability that require attention for PL SEE testing. The first involves stability of the DUT against vibrations. When a micron-sized beam is overlapped with a small sensitive area, even the slightest vibration can cause problems with measurements due to misalignment. Cables that are not firmly supported will move when exposed to air currents from heating or cooling systems. The cables can also transmit vibrations from the cooling fans on measuring instruments and power supplies or even from personnel typing on keyboards. Any of these movements can cause misalignment of the DUT.

An option that can help minimize vibrations through the cables is to use a structure securely attached to the optical table and placed at a convenient location on the table. The cables are secured to the structure with clamps, but with sufficient slack is allowed for the DUT to move without being restricted by the length of the cables. This "structure" can be as simple as a standard optical post.

3.2.3   Thermal Considerations

Much like for heavy-ion testing, temperature control often is required in PL SEE testing and careful consideration must be given to mitigate any potentially negative impacts.

Cooling.   The operating temperatures of some parts can be well above room temperature requiring of cooling. There are various methods used for cooling parts in PL SEE experiments. The most common involves thermo-electric coolers attached to the back side of the part. Others utilize a cooled liquid that

is pumped through narrow pipes designed into the board. Such pumps can contribute significant vibrations to the DUT, which can make laser testing quite difficult. Another approach involves flowing lower-temperature gas over the chip. The gas (usually nitrogen) typically is cooled by flowing it through an ice bath, a dry-ice bath, or even a liquid nitrogen bath, to achieve the desired temperature. Since this is done in open air, condensation can be significant for temperatures below the dew point. In addition to electrical issues associated with condensation, focusing of the laser beam can also be adversely affected by condensation. Fans can also be used to blow cool air over a hot chip. A fan attached to the board containing the DUT is not desirable for PL SEE tests because it will add significant vibration. Instead, a fan should be placed nearby to blow the air gently across the surface of the chip. One should monitor the impact of vibrations and adjust the position and flow rate accordingly.

Heating. Elevated temperature testing is often needed such as parts being tested for SEL that may require part qualification at a case temperature of 125° C (a common level used in the industry). Implementing this requirement is done by attaching a heater to the rear of the DUT and including a thermocouple to monitor and control the temperature. This is usually not a problem because the system does not contain moving parts that could cause vibrations, aside from additional wires that could cause problems when scanning. However, tight temperature control should be implemented during testing since fluctuations in temperature can affect both the position and focus of the laser beam on the DUT, as discussed below.

Impact on Beam Alignment. Changes in temperature can lead to expansion or contraction of the DUT. These mechanical changes can affect the position and focus of the laser-generated CD on the sensitive region which could lead to changes in the SEE response (see **Section 4.2**). Temperature changes can arise from the deliberate heating or cooling of the DUT, but also can arise from anything that changes the thermal load on the device, such as changes in bias or operating mode. Achieving valid data when performing lengthy experiments with varied operational parameters is challenging, and sometimes requires re-optimization of the beam focus for each change in parameters.

3.3 EXPERIMENTAL DESIGN CHECKLIST
The checklist below is provided as a convenient guide on what to do prior to undertaking PL SEE testing at a remote facility.

- Prior to testing, have you communicated the goals of the test with the facility operators?
- Prior to testing, have you shared a test plan with the facility operators and verified that the experiments are realistic and executable within the allotted time?
- Prior to testing, have you verified that the test equipment is operating properly, the software is free of bugs, and can capture the signatures desired?
- If shipping equipment, have you arranged so that it arrives in advance of the test date and can you arrive a day early to familiarize yourself with the test setup and operational procedures?
- If the facility is going to provide equipment, such as a power supply, make sure that it is in proper working order and can perform the necessary function before visiting the facility for the first time.
- Have you communicated with the facility operators in advance to develop handshaking for any communication between the facility equipment (stage, oscilloscope, etc.) and the test setup required to automate the test?

- Have you estimated the sizes of the areas to be scanned and the scanning resolution and is this consistent with the specifical goals of the experiment? Have you budgeted sufficient time for these particular experiments?

- Do you have a large-sized hardcopy layout of the chip available to help with navigation?

- Has your board been designed so that it be properly mounted on the stage at the facility, and have you ensured that the focused beam from the objective can access the DUT, free of obstructions?

- Has the stability of the board and its attached wires been considered?

- Have you discussed with the facility an estimated pulse energy / LET_L range to try and ensure proper data acquisition while avoiding potential damage due to excessive charge generation?
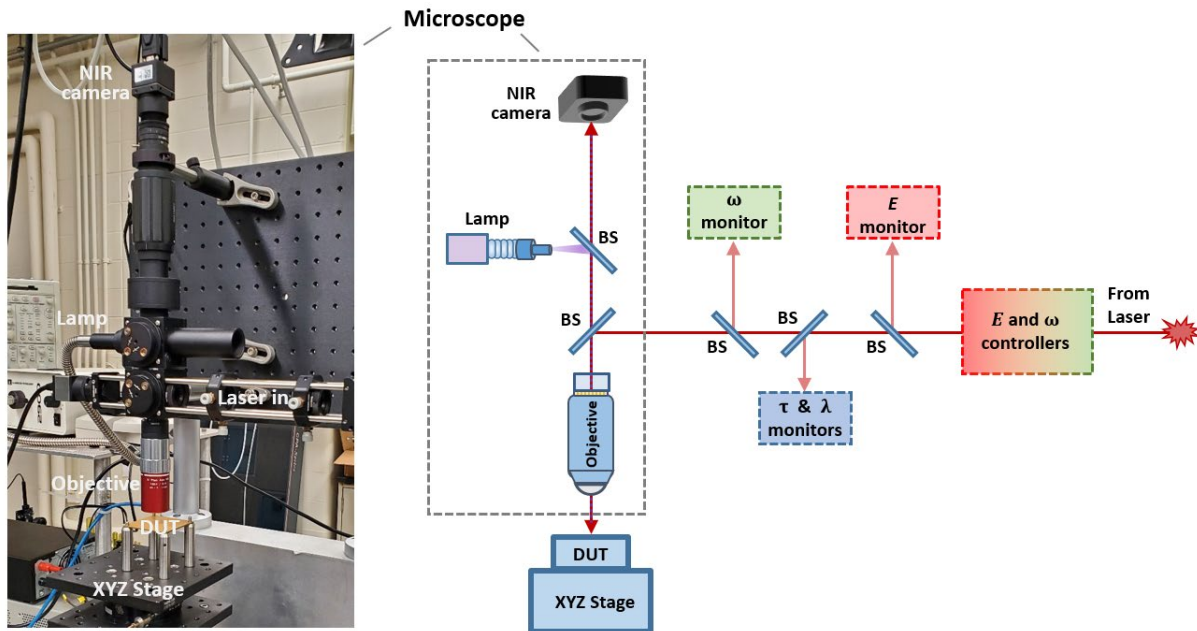
4 PL SEE SYSTEM AND PARAMETERS

The interaction between the CD, generated by any excitation mechanism, and the charge-sensitive region of the device or circuit ultimately determines its SEE response. Consequently, understanding the details of the CD and being able to accurately deliver it to the DUT are critical for PL SEE testing. This chapter details the system for pulse delivery and the parameters that govern the magnitude and shape of the CD.

4.1 SYSTEM LAYOUT

The laser beam must be routed from its source to the microscope where it will be delivered to the DUT. The path the beam takes depends on the specific laser being used, with certain lasers passing through a number of optical components before reaching the microscope while others can be located close to the microscope with few, if any, intervening components. Regardless of the laser system used, there should be a means of adjusting and characterizing the laser parameters that determine the generated CD. The key laser parameters are the center wavelength (λ), the pulse energy (E), the focused beam size (ω_0), the pulse width (τ), and the repetition rate (RR). These parameters are described in detail in subsequent sections, but it is useful to see how their adjustment and characterization are integrated into a typical PL SEE system. A schematic diagram of the U.S. Naval Research Laboratory's PL SEE system is shown in **Figure 4.1**. The laser, optical components, and microscope are all attached to a large optical table. Such a table allows for the various components to be moved or replaced when needed but then tightly secured (through screw holes located at regularly spaced locations) once properly positioned. The laser beam is routed, using highly reflective mirrors, through components that allow for controlling two key parameters: pulse energy and laser beam size/shape. The pulse energy (see **Section 4.3**) is the primary means of controlling the magnitude of the CD while the input beam size (ω) and shape dictates the focused beam size (see **Section 4.4**) and therefore the size of the CD. While the remaining laser parameters (wavelength, pulse width, repetition rate) can also be controlled, they typically remain fixed for a testing system.

Prior to being delivered to the microscope, the various laser parameters are characterized. The methods and instruments used for characterizing each specific parameter are discussed in their respective sections below. As illustrated in **Figure 4.1**, a small portion of the laser beam is sampled (via a partially reflective mirror known as a beamsplitter) for each characterization step. This allows the characterization to be performed in a standoff manner, thereby allowing real-time monitoring of the parameters without interfering with the laser delivery to the DUT. The combined effect of these monitors is that the factors that determine the CD are well-characterized. Since the CD (and its overlap with the sensitive region of the DUT) determines the SEE response, these efforts are important for performing repeatable and traceable experiments in a routine manner. Furthermore, accurate characterization of the CD is important for efforts aimed at facilitating device modeling and correlations between laser and heavy-ion excitation. References detailing the impact of various laser parameters on the generated CD and the associated characterization efforts can be found in [1, 2, 19, 20, 32].

Figure 4.1. *Photograph of a typical PL SEE microscope setup (left) and schematic detailing the laser beam delivery, parameter controllers and monitors, and microscope (right). BS – beamsplitter.*

Common to every PL SEE system is a microscope designed for reflective imaging. Imaging is critical for locating and identifying the target region of interest on a DUT for testing. The key components of the microscope are shown in the schematic in **Figure 4.1**. These components can be housed in a commercial microscope body or in a home-built assembly. A photograph of the home-built system at the U.S. Naval Research Laboratory is shown in **Figure 4.1**, with the various components labeled. Imaging is accomplished by sending lamp light through a high-quality microscope objective, which then reflects off the sensitive region of the DUT and/or the metal overlayers and is subsequently imaged onto a CCD or CMOS camera. The choice of laser wavelength for testing (see **Section 4.2**) typically determines the lamp light, objective, and camera used. The lamp light, which is broadband (or possesses a wide range of wavelengths), overlaps with the laser wavelength, while the objective is designed for certain wavelength ranges. The camera is either Si-based (for $\lambda < 1100$ nm) or InGaAs-based (for $\lambda > 1100$ nm). The objective typically has a large numerical aperture or NA (> 0.4), since a larger NA allows for improved spatial resolution. Further, an objective provides a certain magnification of the area being imaged, with magnification factors ranging from 5x to 100x. In practice, a lower magnification objective is used to initially locate the region of interest before moving to a higher magnification objective for improved resolution and testing. Photographs of a DUT imaged under different magnifications are shown in **Figure 4.2**.

The laser beam is introduced into the microscope such that it follows the same path into the objective as the lamp light used for imaging. In **Figure 4.1**, this is accomplished by injecting the laser from the side (via a beamsplitter) and into the objective. The objective then focuses the laser beam to produce a small focal spot size (for details, see **Section 4.4**). Like the lamp light, a portion of this focused beam is reflected and imaged onto the camera, which therefore provides the location of the focused beam on the DUT, as shown

in **Figure 4.2**. In order to co-locate the focused beam with the region of interest for testing, the DUT is positioned using a 3D translation stage (see **Section 4.6**) relative to the fixed laser beam (which is typically more difficult to move).
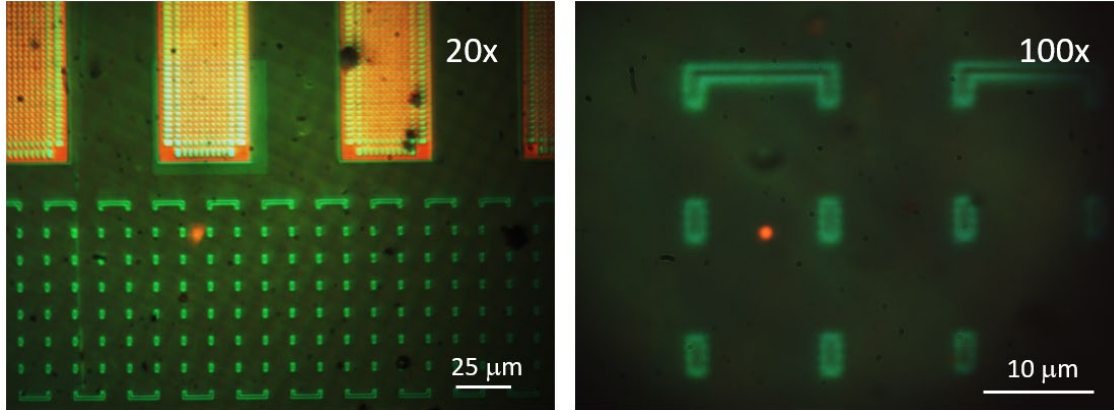
Figure 4.2. *Micro-photographs of a 28-nm SOI SRAM taken by a microscope (top-side SPA excitation, λ = 690 nm) using different objectives. The focused laser beams are shown as red dots and have spot sizes (ω_0, HW1/e^2) of 2.1 μm and 0.76 μm, for the 20x (NA = 0.42) and 100x (NA = 0.55) objective, respectively.*

Descriptions of other PL SEE systems can be found in [33-36]. Finally, a useful reference describing the functionality and purpose of many of the optical components described in **Chapter 4** can be found in the introductory chapter of the following online reference [37].

4.2   WAVELENGTH AND CARRIER GENERATION

PL SEE testing is performed over a wide range of wavelengths, with regions typically designated as ultraviolet (UV, λ < 400 nm), visible (VIS, 400 nm > λ > 750 nm), and near-infrared (NIR, λ > 750 nm). The laser wavelength is characterized and/or monitored by a spectrometer. The choice of wavelength dictates the type of laser as well as the optical components that are employed. Consequently, a PL SEE system is typically designed for a single wavelength, although tunable systems can also be used for wavelength-dependent studies [38-40]. Importantly, the combination of the laser wavelength and the semiconductor under test determines the type of carrier generation process that will occur (*i.e.*, SPA or TPA), which significantly impacts the laser-generated CD. This section discusses the proper choice of wavelength for studying the DUT and the impacts on the resulting CD.

4.2.1   Wavelength Selection for Semiconductors

The bandgap of the semiconductor material under test (E_g) is an important parameter for PL SEE testing. Since SPA involves inter-band excitation of an electron through absorption of a single photon, the photon energy (E_{ph}) must be greater than E_g for SPA to occur (see **Figure 2.1**). Given the inverse relationship between photon energy and wavelength, this restriction imposes an upper limit on the specific wavelength that can be used for SPA. Knowing that E_{ph} > E_g, one can use the following relationship to determine the upper wavelength limit for SPA: λ (nm) = 1240 / E_{ph} (eV). Using Si (E_g = 1.14 eV) as an example, a NIR wavelength marks the limit of SPA testing: λ < 1090 nm. By contrast, for a wide-bandgap semiconductor such as GaN (E_g = 3.4 eV), UV wavelengths are required for SPA testing: λ < 365 nm. For

TPA, where the carrier generation process requires the absorption of two photons, the photon energy must satisfy the relationship $E_g > E_{ph} > E_g/2$ (see **Figure 2.1**). Essentially, for wavelengths above the SPA limit, TPA is the dominant carrier generation process. The wavelength regions used for SPA- and TPA-based PL SEE testing for three common semiconductors are shown in **Figure 4.3**. It should be noted that the relationships described above are for pristine, low-doped semiconductors. The presence of dopants and/or impurities can affect this relationship (see **Section 5.1**).

Below the cutoff wavelength for SPA, the strength of the absorption is characterized by the SPA coefficient, α. As shown in **Figure 4.3**, α exhibits a strong wavelength dependence for most semiconductors. An important value for laser testing is the optical penetration depth, which is the reciprocal of the SPA coefficient, $L_{PD} = 1/\alpha$. After the incident laser light has propagated a distance L_{PD}, it is reduced to $1/e$ of its initial value. In this sense, L_{PD} is analogous to the penetration depth of a heavy-ion and should be chosen with the sensitive depth of the DUT in mind. Like α, the optical penetration depth strongly depends on the wavelength. For instance, **Figure 4.3** indicates that L_{PD} in Si can vary from several 100's of microns in the NIR to only a few microns in the VIS.
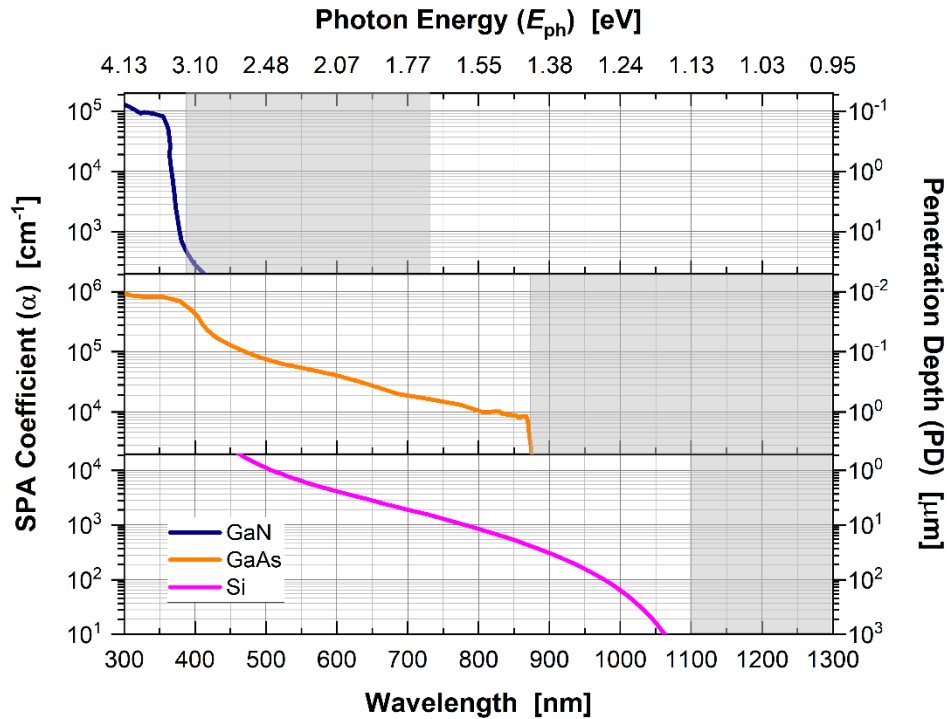
Figure 4.3. Plot of SPA coefficient/penetration depth versus wavelength/photon energy for three different semiconductors: GaN, GaAs, and Si. The greyed-out region below the bandgap indicates the wavelength range where TPA is the dominant excitation mechanism.

The practical consequences of laser wavelength selection can be understood in terms of accessing the sensitive region of a DUT. When access to sensitive nodes is possible from the top side of the DUT (*i.e.*, unhindered by the presence of metal interconnects or packaging, see **Figure 2.2**), SPA testing can be readily implemented with the consideration that L_{PD} is sufficient to probe the sensitive depth of the device. For devices with shallow sensitive depths, UV or VIS wavelengths are often chosen since they afford the

smallest focused spot size (see **Section 4.4**). Oftentimes, access to the sensitive region via top-side excitation is blocked by packaging or metal overlayers (see **Figure 2.2**) and the laser light should be directed through the back side of the wafer. If the wafer is not thinned, the SPA wavelength must be chosen such that L_{PD} can reach the sensitive volume. For Si, a wavelength of 1064 nm (a common laser wavelength for SPA testing) provides a sufficiently long penetration depth for most back-side testing. **Figure 4.4** shows a comparison between top-side and back-side SPA testing for an LM139 comparator, revealing the deleterious impact of metal overlayers for the former. For TPA testing, back-side testing is straightforward to implement since the optical penetration depth is not a concern, *i.e.*, the light propagates through the semiconductor un-attenuated until charge generation occurs near the focal point.
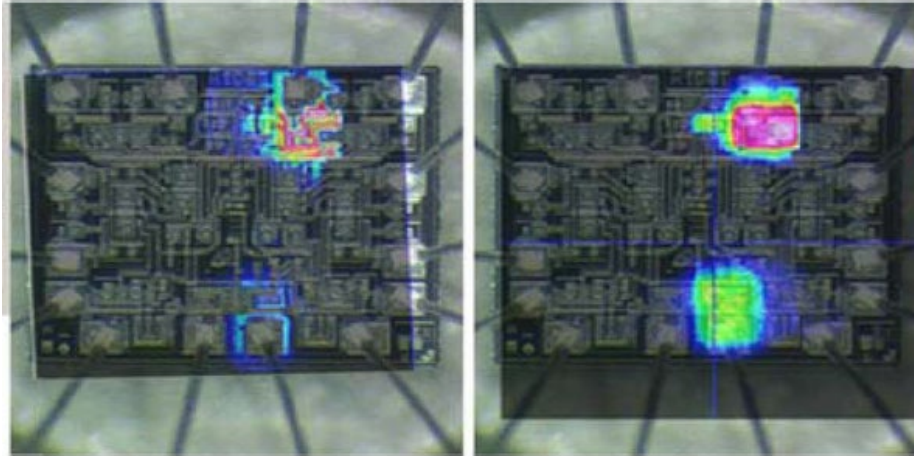
Figure 4.4. *A comparison between top-side (left) and back-side (right) laser excitation for SPA testing (λ = 1064 nm) of an LM139 comparator. The color scale corresponds to the laser energy threshold for SPA needed to trigger SETs whose amplitudes are greater than a reference value (magenta is the lowest energy or most sensitive region while blue is the highest energy or least sensitive region). Clearly, some sensitive regions are blocked via metallization for top-side testing. After [1].*

4.2.2 SPA-Induced Carrier Generation

The laser-generated CD is determined by both the dominant optical absorption process and the focusing of the light. The laser wavelength plays a role in both of these contributing factors, with the wavelength-dependence of the absorption process discussed in **Section 4.2.1** and the impact of wavelength on the focused beam size discussed in **Section 4.4**. It is instructive to look at the role the SPA coefficient and the laser parameters play in the SPA-generated CD. Various references describe how to accurately calculate the laser-induced CD [19, 32, 41]. For the purposes of qualitatively understanding the major factors that impact the carrier generation, a simplified approach is taken here. The SPA-induced CD is given by:

$$CD_{SPA} \propto \left(\frac{\alpha E}{\omega_0^2}\right) \cdot e^{-\alpha z} \cdot S(r,z), \tag{1}$$

where $S(r,z)$ represents the spatial distribution (in the lateral and axial dimensions) created by the focused laser. This is distribution typically takes the shape of an ellipsoid, limited by the focused spot size in the lateral dimension and with a larger size in the axial dimension [42]. Essentially, the pre-factor in Eq. (1) controls the magnitude of the CD, with peak values increasing with stronger SPA or a more focused beam. Most importantly, the peak CD can be easily controlled through the laser pulse energy, and this is

the primary way in which the SEE response is characterized (see **Section 4.3**). The shape of the CD is controlled by $S(r,z)$ and $e^{-\alpha z}$, highlighting the importance of focusing and absorption, respectively.

Simulated CDs are shown in **Figure 4.5** that are representative of those generated during SPA testing in Si using different laser excitation wavelengths. All CDs show strong localization in the lateral dimension (≤ 1 μm FWHM) reflecting the spatial confinement that is key to PL SEE testing. Despite the fact that the pulse energy is nearly 400x larger for 1064 nm compared to 590 nm, the peak CD is greater for the latter; this underscores the impact of the larger α value for the shorter wavelength (see **Figure 4.3**). The axial distributions are mainly controlled by the L_{PD} values for the two shorter wavelengths. For 1064 nm, the L_{PD} value is 900 μm and yet the CD is still confined to within 10 μm of the surface. This reflects the role of both beam focusing and absorption in the generation of the CD, with the former having a significantly greater impact at this wavelength.
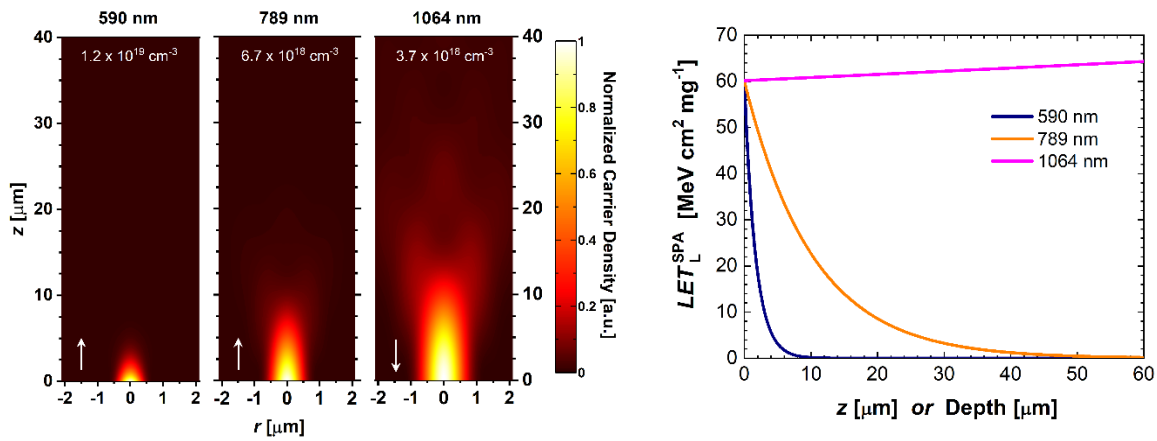
Figure 4.5. *Simulated SPA-generated CDs (left) and LET_L^{SPA} profiles (right) for different excitation wavelengths in Si using a 100x objective (NA = 0.55). The CDs are normalized to their respective peak carrier densities (listed as insets) and the arrows denote the direction of the excitation (note: 1064 nm is from the back-side). The relevant laser parameters for the different wavelengths are: (1) λ = 590 nm, E = 3.4 pJ, ω_0 = 0.45 μm (HW1/e^2), α = 5882 cm^{-1}, L_{PD} = 1.7 μm; (2) λ = 789 nm, E = 14.8 pJ, ω_0 = 0.6 μm (HW1/e^2), α = 971 cm^{-1}, L_{PD} = 10.3 μm; (3) λ = 1064 nm, E = 1300 pJ, ω_0 = 0.81 μm (HW1/e^2), α = 11 cm^{-1}, L_{PD} = 900 μm. Simulations were performed using the approach described in [7].*

Interestingly, if the CD given by Eq. (1) is integrated over the entire lateral dimension, only an axial charge-deposition profile remains [19]. Analogous to a heavy ion, this is referred to as the laser-equivalent LET (LET_L)[1] and can be written as follows:

$$LET_L^{SPA} \propto (\alpha E) \cdot e^{-\alpha z}. \tag{2}$$

The lateral integration of the CD leaves a simple and intuitive expression for the laser-induced charge deposition. The peak LET is controlled by just two parameters, the SPA coefficient and the pulse energy (further discussion of the LET_L as a function of pulse energy is included in **Section 4.3**). Further, the axial dependence is dictated entirely by α, or equivalently L_{PD} (in contrast to the CD which also depends on how

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[1] The units for the LET_L are given in pC/μm but can be converted to the more common units of MeV· cm^2/mg by multiplying it by $E_{ehp}/(q \times \rho)$, where E_{ehp} is the average energy to create an electron-hole pair (*e.g.*, 3.6 eV in Si), q is the elementary charge, and ρ is the density of the semiconductor (*e.g.*, 2330 mg/cm^3 in Si).

strongly the beam is focused). The LET_L^{SPA} profiles for the SPA-generated CDs discussed above are also shown in **Figure 4.5**. One key point is that the LET_L^{SPA} profile for 1064 nm shows essentially a constant value over the depth shown, consistent with the large value of L_{PD}. This similarity to the LET profile of a deeply penetrating heavy ion is a primary reason why PL SEE testing at 1064 nm on Si devices is utilized often.

4.2.3   TPA-Induced Carrier Generation

Taking a similar approach to the one used above for SPA, a simplified approximation of the comprehensive description of the TPA-generated CD [7, 19, 43] is employed to understand the impact of various parameters on the carrier generation. The TPA-induced CD is given by:

$$CD_{TPA} \propto \left(\frac{\beta_2 E^2}{\omega_0^4 \tau}\right) \cdot S\left(r, z, z_{foc}\right)^2, \tag{3}$$

where β_2 is the TPA coefficient, and z_{foc} is the distance from the surface to the focal point of the laser. The distribution has a number of similarities to the SPA-induced CD, including a peak CD that has dependencies on the absorption coefficient, the focused spot size, and the pulse energy (for TPA, the pulse width is also a contributing factor). The dependencies are stronger for TPA because it depends on the square of the laser intensity [2, 19, 44]. This accounts for the quadratic dependencies of *E* and $S\left(r, z, z_{foc}\right)$, the latter leading to a CD that is strongly localized around the focal point of the laser. This localization is evident in **Figure 4.6**, which shows simulated CDs representative of those generated during TPA testing. In addition to a lateral localization similar to that of SPA, the TPA-generated CDs are also localized in the axial dimension. This additional degree of confinement allows the CD to be moved axially; the two CDs shown in **Figure 4.6** are positioned at different z_{foc} locations.
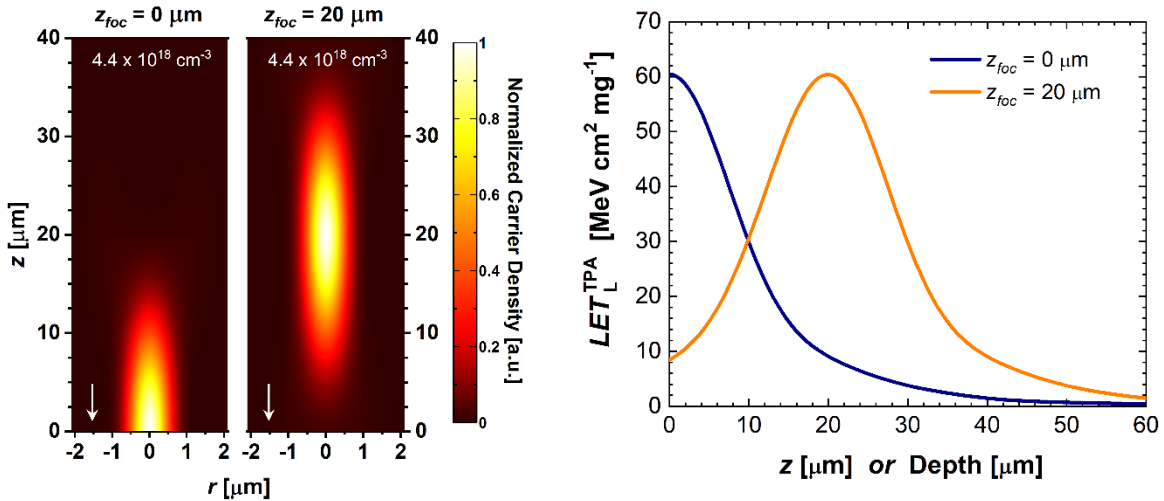
Figure 4.6. Simulated TPA-generated CDs (left) and LET_L^{TPA} profiles (right) for excitation at different axial focal positions in Si using a 100x objective (NA = 0.50). The CDs are normalized to their respective peak carrier densities (listed as insets) and the arrows denote the direction of the excitation. The relevant laser parameters for the different focal positions (z_{foc} = 0 μm, z_{foc} = 20 μm) are: λ = 1260 nm, E = 472 pJ, ω_0 = 1.04 μm (HW1/e²), τ = 100 fs (HW1/e), β = 1.1×10⁻¹¹ m/W. Simulations were performed using the approach described in [7].

Similar to before, integrating Eq. (3) over the entire lateral dimension leads to an axial charge-deposition profile and an expression for the LET_L [44]:

$$LET_L^{TPA} \propto \left(\frac{\beta_2 E^2}{\omega_0^2 \tau}\right) \cdot S\left(z, z_{foc}\right). \tag{4}$$

The peak LET exhibits strong dependencies on the laser parameters (see **Section 4.3** for the dependence on pulse energy). Unlike SPA, where the LET_L^{SPA} profiles are determined by the optical penetration depth, the LET_L^{TPA} profiles are determined by the focusing of the laser. This leads to charge deposition profiles with narrow axial widths whose positions can be controlled based on the focal point of the laser, or z_{foc}.
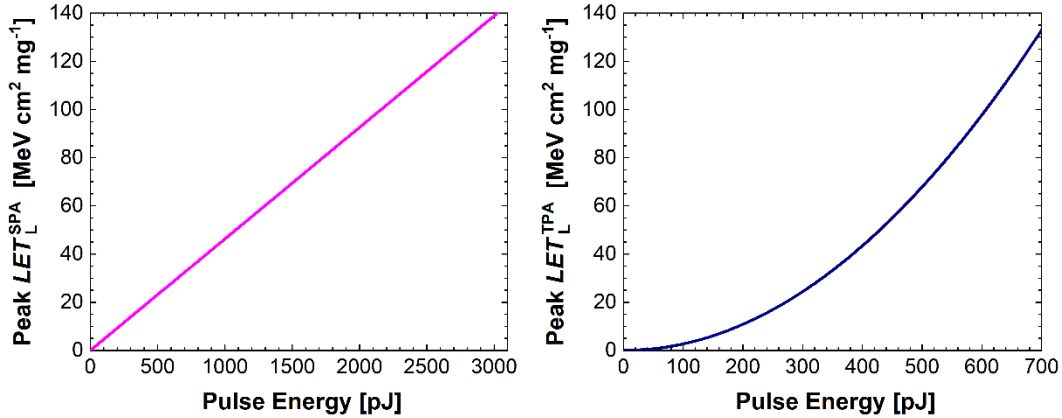
4.3 PULSE ENERGY

As shown in the previous two sections, the laser pulse energy (*E*) is a key parameter in determining the magnitude of the laser-generated CD and the LET_L. Therefore, pulse energy control in PL SEE testing allows one to control the operating point of the laser in an analogous way that LET is controlled in heavy-ion testing. Furthermore, varying *E* (and therefore LET_L) in a PL SEE system is straightforward and therefore the primary knob for characterizing the SEE response of a DUT. While there are different ways to vary *E*, a common method is by using an intensity modulator, which consists of a half-wave plate and a polarizer. When the laser passes through these components and the half-wave plate is rotated, the transmitted energy can be controlled. The rotation can be computer-controlled with fine adjustments such that continuous control of the pulse energy is possible. The pulse energy can also be modified by placing filters within the beam path that only transmit a portion of the laser energy (so-called neutral density filters). Since these filters typically modify the pulse energy in discrete amounts, they are often used in conjunction with the continuous control provided by the intensity modulator.

E should be measured at the DUT position for the conditions under which testing will occur. This can involve placing a calibrated energy meter at the DUT position near the position of the focused laser (using the objective for testing). A second energy meter (as shown in **Figure 4.1**) records values at the same time as the meter at the DUT position, and the two recorded values can be used to generate a calibration curve. Once the meter at the DUT position is removed to begin testing, the second meter serves as a proxy for the first and allows for real-time monitoring of pulse energy. This enables accurate estimates of *E* and monitors its stability over time. Pulse energy stability is critical for achieving good-quality PL SEE test data.

Figure 4.7 shows peak LET_L values for pulse energy ranges commonly used during SPA testing (at 1064 nm) and TPA testing. The LET values show a linear and quadratic dependence on pulse energy, as expected for SPA and TPA, respectively. What is also clear is that PL testing can produce LET_L values that easily exceed those produced at terrestrial heavy-ion test facilities. There are important caveats regarding the LET_L values shown in **Figure 4.7** (or any estimation of LET_L for that matter). The calculated LET_L values are valid for the experimental conditions specified, and so any modifications to these conditions will necessarily change the LET_L values. Accurate characterization of these parameters is critical for accurate estimates of LET_L.

Figure 4.7. *LET_L versus pulse energy for SPA (left) and TPA (right) excitation. The values were determined using the same simulations shown in* **Figure 4.5** *(for λ = 1064 nm) and* **Figure 4.6** *(for z_{foc} = 0 μm). Any modifications to the laser testing geometry could change these values.*

Finally, the LET_L values (as determined by Eq. (2) and Eq. (4)) are derived by integrating over the entire CD and so are appropriate for devices with sensitive areas larger than the CD. For devices with sensitive areas smaller than the CD, the LET_L would have to be reduced according to the overlap area between the two, which can introduce challenges when the sensitive area of the DUT is not well-known [42, 44, 45]. Therefore, the values given in **Figure 4.7** represent the largest achievable LET with the lower bound scaled according to the DUT. This is a direct consequence of the larger lateral size of the CD generated by PL testing compared to heavy-ion testing (see **Figure 3.3**). Interestingly, this concept of a spatially-restricted LET has also been utilized in the context of heavy-ion testing on highly-scaled SOI devices [25, 46].

4.4 FOCUSED BEAM SIZE

The focused beam size (ω_0) plays a key role in determining both the magnitude and size of the laser-generated CD (see Eq. (1) and Eq. (3)). In discussing ω_0, it is important to specify whether it is the radius measured at an intensity $1/e^2$ of the maximum (HW1/e^2, and the value used in this work) or the full-width-at-half-maximum (FWHM). It is often desirable to achieve the smallest value of ω_0 since this gives the smaller CD and therefore the highest spatial resolution (CDs typically have lateral dimensions of $\leq 1\ \mu$m FWHM). The focal spot size is inversely proportional to the NA of the objective used. The impact of this can be seen in **Figure 4.2**, where the larger magnification objective (with the larger NA) produces the smaller focused spot size. Additionally, ω_0 scales with the laser excitation wavelength. This is evident in **Figure 4.5** where the CD (and, by extension, the spot size) decreases as the SPA excitation wavelength gets shorter.

Being able to generate a range of focused beam sizes can be beneficial for laser SEE investigations [12, 21]. Thus, it is best to have several objectives with different magnifications (and NAs). For instance, when testing a new device, it is more efficient to use a lower magnification objective to grossly locate SEE sensitive regions before using a higher magnification objective to precisely probe the SEE sensitive area (see **Figure 4.2**, for example). For an objective with a given NA, ensuring that the input laser beam (ω) is larger than the back aperture of the objective guarantees the smallest value of ω_0. However, by reducing the size of ω, the effective NA of the objective can be reduced resulting in larger value of ω_0 [20, 47]. The

ability to vary the focused beam size by changing objectives and input beam sizes is summarized in **Figure 4.8**.
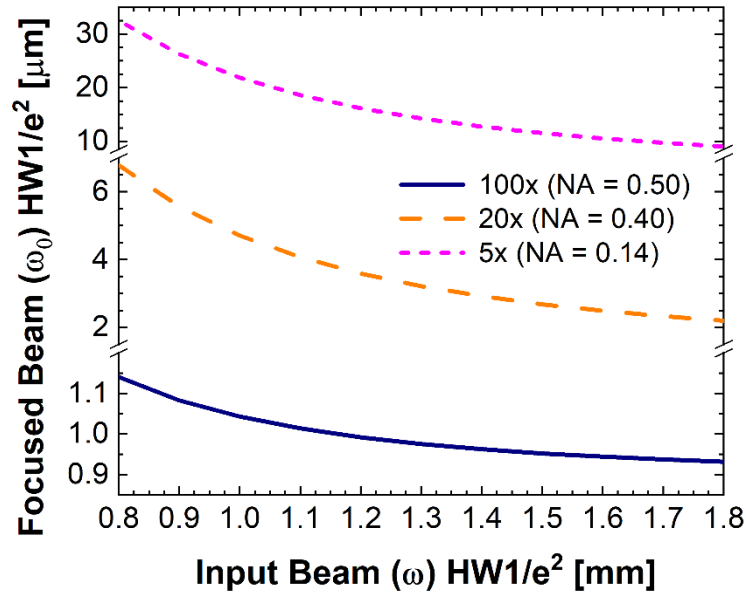
Figure 4.8. *The variation in focused beam size (ω_0) at the DUT for a TPA PL SEE system operating at λ = 1260 nm. These are obtained by using different focusing objectives and different input beam sizes (ω). These calculations were performed according to the method outlined in [47].*

In addition to the size of the input beam, the quality of its spatial profile plays an important role in achieving a good, focused beam. Ideally, the input beam has a Gaussian shape. However, some laser beams are less than ideal and require spatial filtering (a type of low pass filter to remove spatial noise) to improve their shapes. The input beam size and shape can be monitored using a CCD or CMOS camera. Furthermore, since ω essentially dictates the size of ω_0 (for a given objective), the camera can be used as a real-time monitor, as shown in **Figure 4.1**.

4.5   PULSE WIDTH AND REPETITION RATE

The interaction between an ion and a sensitive node of an IC occurs for less than a picosecond [48, 49]. In order to emulate this interaction, the laser pulse width (τ) should be comparable to or shorter than a picosecond. In fact, for charge collection and circuit responses that take much longer than a picosecond, τ must only be significantly shorter than this response time. In any event, provided the pulse duration satisfies this criterion, the actual pulse width does not matter in SPA-based PL SEE testing. For TPA-based testing, pulse widths on the order of 100 – 200 fs are needed for efficient carrier generation (and sub-200-fs pulse widths are certainly faster than the response times of measured devices and ICs). Given the dependence of the peak CD and LET_L on τ for TPA excitation (see Eq. (3) and Eq. (4), respectively), it is important to characterize the laser's pulse width. This is typically done with a device known as an autocorrelator, which is shown as one of the real-time monitors in **Figure 4.1**.

The repetition rate (RR) of the laser refers to the number of pulses generated per second. While some systems have the flexibility to adjust the RR, most systems operate at a single RR in the kHz to MHz range. Two factors must be considered with regard to the RR for a given experiment: the response time of the DUT and acquisition speed. For a system with a higher RR, if the SEE response of a device does not fully relax to its equilibrium state prior to the arrival of the next laser pulse, cumulative effects may arise leading to erroneous data. For a lower RR system, acquisition speed may suffer if the SEE response from many pulses must be recorded for averaging purposes or if a sufficient number of pulses must be present at each position when spatial scanning is done (see **Section 4.6**).

4.6   STAGE SPECIFICATIONS

In order to proceed with testing, the laser-generated CD must be co-located with the SEE-sensitive region of interest. Typically, this is accomplished by positioning the DUT using a 3D translation stage, while the focused beam remains fixed (while less common, movement of the focused laser beam is possible [34]). The stage consists of two lateral dimensions (X and Y) and one axial dimension (Z). A typical travel range for each of these dimensions is 50 mm, which provides sufficient lateral movement to accommodate most devices. Given the very small sizes of the sensitive nodes in current ICs, a stage with a minimum resolution or step size of 0.1 μm, that is also stable and repeatable, should be used. Ideally, the stage should be computer-controlled so that scanning can be done manually with a joystick or automatically through a computer program. The program should direct the stage to move to a position, remain at that position for as long as is required for data to be acquired (known as the dwell time), store the data and the stage position, and then move to the next position.

Step size, scanning speed and dwell time are important factors to consider when performing laser testing. Performing a high-resolution scan over a large area is time consuming, and tradeoffs between the scan area (raster size) and scan resolution (step size) will determine the total data acquisition time. For instance, attempting to scan a large chip with a sensitive area of one centimeter on a side, using a small step size such as 5 μm, could take 100's of hours and so it is generally not practical. On the other hand, small step sizes should be used when scanning the focused beam axially past the surface of the DUT as significant changes in device response can occur. Scanning speed and dwell time must also be considered when testing as they impact the overall acquisition time.

4.7   PREPARATION FOR FACILITY TESTING

Much like in preparation for heavy-ion testing, it is important to be aware of the laser parameters and general capabilities of a laser test facility before committing to a visit to ensure that the desired experiments are feasible. Unlike most heavy-ion test facilities, the pertinent information is not typically publicly available and so it is necessary to reach out to the facility manager/director for details. To this end, some guiding questions are listed below that should facilitate these communications. Certain facilities may provide a document detailing the key capabilities and parameters of the testing system and so it is worth inquiring about this prior to a visit.

- Is the PL SEE system designed for SPA or TPA testing?
- What are the operational laser wavelengths and are these appropriate for the candidate DUT?
- Can testing be conducted via top-side or back-side excitation?

- Which objectives are typically used and what focused spot sizes do they provide?

- What is the pulse width and repetition rate of the laser? Are these parameters adjustable?

- What are the typical pulse energies or LET_L values used for testing?

- What are the stage specifications in terms of travel range and step size?

- How are the laser parameters characterized and monitored?

5 DUT CONSIDERATIONS

A primary consideration for PL SEE testing is ensuring optical access to the active regions of a DUT. While penetration depth of charge particles is routinely considered before executing an SEE experiment at a particle accelerator, additional factors must be considered when using pulsed lasers to inject charge. Some of these factors include the semiconductor material itself, the structure of the DUT, the surface quality of the die, the package used, and the specific design of the board.

This chapter includes an overview of some of the challenges to PL SEE testing that must be addressed prior to a successful test campaign. Considerations about material systems are included. In addition, this chapter presents several packaging challenges that could be encountered when preparing DUTs for PL SEE testing, as well as some approaches for addressing those challenges.

5.1 SEMICONDUCTOR MATERIALS CONSIDERATIONS

In contrast to traditional accelerator testing, some parameters of the semiconductor material should be considered for PL SEE testing. For example, the material system used to fabricate the DUT will determine the appropriate wavelength for a given experiment. In addition, highly doped substrates can inhibit or modify the propagation of laser pulses. These factors, which are specific challenges to PL testing, are discussed in detail below.

5.1.1 Semiconductor Materials

Typically, the electronic bandgap (E_g) of the semiconductor being tested is not a parameter that needs to be considered when doing heavy-ion testing. The ions generate electron-hole pairs with energies that far exceed the E_g of the material, even for wide-bandgap semiconductors like GaN and SiC, or insulators like SiO$_2$. In contrast, the bandgap of the material is a critical parameter for PL SEE testing.

As discussed in greater detail in **Section 4.2.1**, wavelength selection will determine whether charge is deposited via SPA or TPA in a given material. This can present challenges and unique experimental opportunities for DUTs that have multiple material systems (*e.g.*, material stacks and heterojunctions). One of these challenges is the difference in charge generated in each layer of a material stack, which is a result of the different bandgaps and absorption coefficients for each layer. When testing material stacks, these differences in absorption coefficients could prevent charge from being deposited in the layers of interest. For example, if the laser pulse first encounters a material with $E_{ph} > E_g$, it will lead to SPA. Depending on the absorption coefficient and thickness, this layer potentially can deplete the beam, blocking carrier generation in the other layers.

Yet another concern lies in attempting charge deposition by TPA ($E_g > E_{ph} > E_g/2$), when there exist layers that absorb by SPA ($E_{ph} > E_g$). Because the laser pulse energies required for TPA can be larger than those for a typical SPA experiment, absorption in the SPA layer can be significant (depending on the thickness and absorption coefficient). Carriers generated in that layer will likely dominate the experimental observables and the potential for catastrophic damage can be significant.

However, this difference in charge deposition can be utilized to enable unique experimental opportunities. One example is shown in **Figure 5.1** for an InAlAs/InGaAs HEMT. In this case, charge can be

generated selectively in the InGaAs channel (via SPA) by tuning the laser wavelength to just above the InGaAs band edge ($E_{ph} > E_g$), but below the InP and InAlAs band edges. This localized charge deposition is useful in basic mechanisms studies and is a unique scenario that is impossible to reproduce with particle radiation.
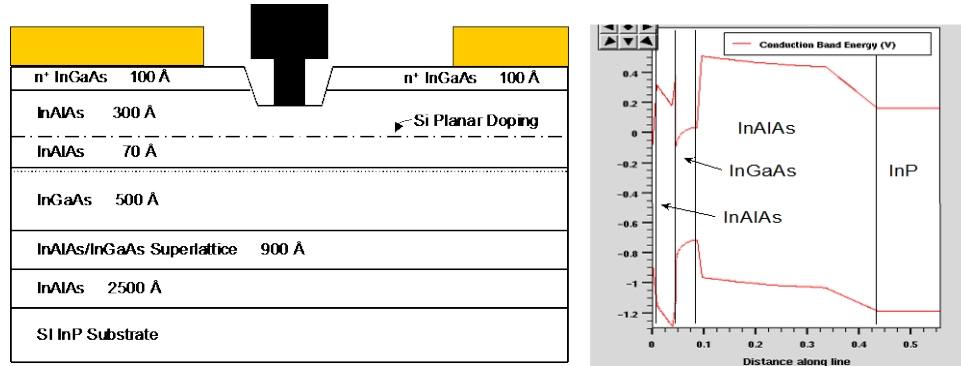

Figure 5.1. InGaAs/InAlAs HEMT structure and band diagram. After [50].

5.1.2 Doping Consequences and Processing Modifications

Highly doped semiconductors, such as n+ silicon substrates, pose no challenges for ion testing because the interaction between the incident ions and the valence electrons is not affected by the presence of free electrons and holes. In contrast, doping can play a significant role in PL testing because doping serves to (1) shift the bandgap in ways that modifies the absorption coefficient at certain wavelengths, and (2) populates the conduction band with additional carriers, leading to a phenomenon known as free-carrier absorption.

When the doping level is increased, the effective bandgap is reduced, an effect known as "bandgap narrowing". This reduction of E_g leads to changes in the absorption coefficient that become more significant as the doping level is increased. For heavily doped p-type GaAs, for example, the absorption coefficient increases significantly for photon energies below the band edge (E_g = 1.42 eV), as is shown in **Figure 5.2**. This increase will contribute to beam depletion as it traverses the heavily doped material. **Figure 5.2** illustrates that bandgap narrowing also is significant in silicon at the doping levels typically used in implants and for highly doped substrates (>5 x 10^{18}). This increase in absorption coefficient in highly doped substrates will affect the optical penetration depth and can limit optical access to the sensitive regions of the DUT for backside focusing, depending on the substrate thickness.

Another relevant phenomenon is "free carrier absorption", in which the absorption cross-section of free electrons in highly doped regions becomes non-negligible, as is illustrated in **Figure 5.2**. Free-carrier absorption depletes (reduces) the intensity of the propagating laser pulse, but no new carriers are generated, and no SEEs are produced. When performing SEE testing using SPA from the top side, the highly doped source and drain regions are so thin that they have little effect on the intensity of the propagating light. However, for device structures that consist of a low-doped, thin epitaxial layer sitting on top of a highly doped substrate (commonly called an "epi wafer"), the free carriers can affect the propagation of optical pulses when using through-wafer (*i.e.*, back-side) irradiation. For standard epi wafer thicknesses and standard doping levels, the optical pulse will be fully depleted prior to reaching the active layer. In such cases, the substrate must be thinned, by polishing or milling, typically to less than

100 μm. Although the exact thickness required depends on the doping level, a good rule of thumb is that if you cannot image the active regions through the silicon substrate with a near-IR camera, then the laser pulse will not reach the active regions. One added complication is that quantitative assessment becomes difficult when there is significant free-carrier absorption. That is, in either SPA or TPA, free-carrier absorption renders the quantitative determination of charge deposited in the sensitive regions of a device difficult.
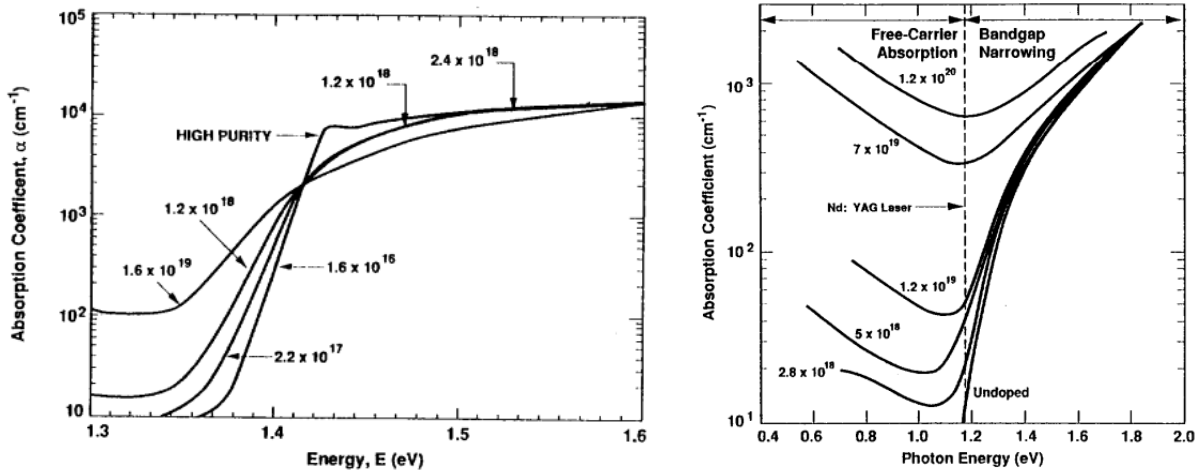

Figure 5.2. *Changes in absorption coefficient due to semiconductor doping: (Left) Bandgap narrowing in p-type GaAs due to high doping levels, (Right) bandgap narrowing and free-carrier absorption in silicon. After [51].*

Since PL facilities often have access to a limited number of wavelengths, it is important to clarify all such details prior to committing to a particular laser test facility.

5.2 OPTICAL ACCESS

Often, the most significant challenge for PL SEE test planning and execution is the preparation of DUTs, which can range from individual bare die to packaged commercial parts. Unlike the high-energy particles of the natural space environment and some terrestrial test facilities, laser light cannot penetrate device packages, which are typically made from metal, plastic, ceramic, or some combination of these. Consequently, DUTs must be specially prepared for PL SEE testing. In general, the process for gaining access to sensitive volumes in a DUT is similar for both low- to medium-energy heavy-ion testing, and PL SEE. In most cases, the DUT is either chemically or mechanically processed to expose the die such that there is optical access to the sensitive volumes of interest. There are a few key differences between DUT preparation for ion and laser experiments, which will be outlined in this section.

5.2.1 Considerations for Top-side or Back-side Testing

Typically, one of the most important considerations when deciding to test a particular component is whether charge will be deposited via excitation from the "top side" or "back side". For top-side excitation, the DUT is oriented such that the beam will first encounter back-end-of-line (BEOL) metal and passivation layers before depositing charge in the sensitive volume. In contrast, for back-side or "through-wafer" excitation the beam first encounters the substrate before depositing charge in the sensitive volume. Both

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types of testing can be performed using heavy ions and pulsed lasers, and there are advantages and disadvantages to each approach. In addition, there are different packaging considerations for each type of testing, a summary of which is included in **Table 5.1**.

Table 5.1. *List of Considerations when de-processing devices for broad beam heavy-ion testing versus PL SEE testing.*

	Broad Beam Heavy-Ion Testing	PL SEE Testing
Top-side	Unclean, or "muddy" die surface is acceptable	Extremely clean die surface required (this can impact yield)
	BEOL oxides might need to be removed if using ultra-low energy ions	BEOL oxides are transparent to laser light and do not need to be removed
Back-side	Unpolished surface acceptable	Optical quality surface required (*i.e.*, "mirror finish")
	Extremely uniform thickness desired for LET uniformity across the die	Uneven thickness is acceptable for TPA due to 3-D focusing but can make the experiment more difficult; extremely uniform thickness is desired for back-side SPA
	Final substrate thickness depends on ion beam penetration	Final substrate thickness depends on doping levels and wavelength

Factors to Consider for Top-side Testing. When using heavy ions, top-side testing is perhaps the most common approach. Typical ions available during accelerator tests have enough energy to traverse metals and passivation layers. In addition, as will be discussed in **Section 5.3**, most de-processing techniques tend to facilitate top-side access for wire-bonded components. For PL SEE testing, however, top-side testing can be challenging as any metallization can prohibit optical access to portions of the sensitive volumes. Oftentimes, testing cannot be performed on devices that have more than two metal layers, which is an increasingly common occurrence for modern semiconductor fabrication processes.

Top-side testing can be performed via SPA or TPA, and the requirements for sample preparation are similar. In particular, a smooth, flat surface that is clear of debris is required. However, the process for ensuring a high-quality surface can impact DUT yield, as the de-processing steps can affect device performance. In addition, dense metallization above the sensitive volume will obscure laser light. Gaps in the metal layers that allow light to pass through could enable qualitative measurements, but quantitative estimates of charge deposited become difficult, if not impossible.

Ultimately, the key constraints for top-side testing, via either SPA and TPA, are surface quality and metal coverage. The decision on whether to perform top-side PL SEE testing will depend on the particular DUT. If metal coverage is too dense, back-side testing is a good alternative.

Factors to Consider for Back-side Testing.   When top-side excitation is not possible, either due to packaging constraints or metal coverage, back-side or through-wafer testing can be an alternative. Back-side excitation can be performed using both ions and pulsed lasers and is often necessary for flip-chip devices. For through-wafer testing using heavy ions, back-side thinning is often required, depending on the range of the ions used. The substrate thickness for most devices ranges from 100 to 750 μm, which is enough to stop some ions at beam facilities from reaching the sensitive volumes. However, an optically smooth surface is not necessary for ion testing.

For through-wafer SPA the main concern becomes beam depletion as it traverses the silicon substrate (discussed in **Section 5.1.2**). Therefore, the die should be thinned such that the beam can deposit charge in the sensitive volume, which will depend on the substrate doping level and laser wavelength. Publicly available absorption curves (see **Figure 4.3**, for example) should be consulted to determine the appropriate die thickness. While die thickness is less critical for through-wafer TPA, die thicknesses greater than 400 μm can lead to distortions of the charge deposition profile. Therefore, it is recommended that the die are thinned below this thickness. In this case, the general rule of thumb still applies: if the sensitive volume can be imaged with a NIR camera, the die is sufficiently thin.

When thinning a device, it sometimes happens that the wafer, which is under stress, buckles, making the thickness of the wafer vary across the surface. Uneven thickness can be problematic for SPA since the LET_L depends on the thickness (see **Section 4.2.2**). For TPA, uneven thickness is acceptable since it can be corrected for by adjusting the focal position. While this can make the experiment more difficult, these positional corrections can be determined beforehand and compensated during the experiment.

A highly polished surface is essential for both TPA and SPA but is especially critical for TPA since a poor surface quality can significantly affect the beam quality, which has a direct impact on the charge generation process. To ensure that the back surface of the silicon chip is sufficiently smooth for TPA testing, this surface should have a "mirror" finish. Surface roughness values are specified relative to the wavelength and normally range between $\lambda/5$ to $\lambda/20$, where λ is the wavelength used and $\lambda/20$ is the highest quality surface. As a rule of thumb, a sufficiently smooth back surface exists if the metallization on the top side of the chip can be seen through the substrate using a NIR camera.

Package Considerations. The type of package and available de-processing techniques could limit whether top-side or back-side excitation are possible. Top-side irradiation is almost always required for wire-bonded parts. While not impossible, the preparation of wire-bonded parts for back-side irradiation can be extremely labor intensive, if not impractical. The most straightforward approach is to completely remove the die and attempt to re-package in a way that exposes the substrate. Similarly, flip-chip devices tend to be better suited for through-wafer excitation. Although not an exhaustive treatment on the topic, the following section outlines several packaging scenarios and available de-processing techniques, which will inform the feasibility and practicality of performing top-side or back-side excitation for a given DUT.

5.3   PACKAGING SCENARIOS AND DE-PROCESSING TECHNIQUES

Generally, most packaged parts can be divided into two types: wire-bonded and flip-chip. Wire-bonded parts utilize thin wires, typically made of gold, to connect the metal pads on the top of a die to the pins of a package. Flip-chip parts, on the other hand, utilize small metal bumps to connect the metal pads on top of a die to pads on the package that are electrically connected to the pins. This method results in a die with an orientation that is "flipped" (*i.e.*, the top side is facing down) compared to the traditional wire-bonded parts.

Although the requirements for top- and back-side testing were discussed in the previous section, the type of package will impose practical restrictions on the type of testing that can be performed. Many recent-generation ASICs and standard parts are packaged in a flip-chip configuration, which often can be quite convenient for through-wafer PL SEE interrogation using either SPA or TPA. In contrast, many older-generation packaged parts tend to be wire-bonded. Once decapsulated, these are most easily accessible via top-side irradiation using either SPA or TPA, depending on the specific technology.

Regardless of the package type or de-processing technique used, it is imperative that the device be both functional and parametrically equivalent to the encapsulated device prior to de-processing. Otherwise, the results obtained during an SEE test campaign may not be representative of an encapsulated part that will operate in a radiation environment. A discussion of various considerations for de-processing for these types of packages follows.

5.3.1 Wire-Bonded Parts

Wire-bonded parts can be divided into two main types: hermetic packages and plastic encapsulated microcircuits. Hermetic packages can typically withstand higher temperatures than equivalent plastic packages, while plastic packages are typically lower cost. However, both types of packages are broadly used and routinely tested for SEEs, and each package type requires specific de-processing techniques.

Hermetic Packages. Hermetic packages come in several configurations, including multilayer ceramic packages, pressed ceramic packages, and metal can packages [52] (see **Figure 5.3**). There are two general approaches to preparing ceramic packages for PL SEE testing such that optical access to the die can be achieved.


Figure 5.3. Example of a 20-pin ceramic dual inline package (left), flat metal lid (center), and TO (can) package (right).

The first approach to de-capsulate ceramic or metal-lid packages consists of scoring the glass seal-to-lid interface. Devices are then clamped into a knife-edged vice, or other pressure-inducing device. The applied pressure is increased until the lid separates. Alternatively, a small ballpein hammer can be used to induce vibrations until separation occurs. While this is probably the most common approach, it is also the riskiest, and the results can be very unpredictable. This approach is far more successful with a flat metal lid package where a small cut is made in the solder fillet at a perimeter corner in order to guide the blade between the lid and the seal ring. A knife blade can then be carefully tapped into the seal, or again a knife-edge vice, avoiding contact with wirebond loops or the die surface. The lid will almost always break free from a thick film seal ring layer on a ceramic package. On a metal seal frame, there may be a tendency to gouge the seal frame, and extra care is needed to keep the blade from cutting into the solder seal. With this method, metal debris will very likely be deposited into the package cavity, which must be carefully removed to avoid electrical shorting or other unwanted effects.

The second approach is the use of a lapping wheel with a diamond grit to grind the surface of the package. The device should be ground down until the cavity becomes apparent, as shown in **Figure 5.4**. The use of water is recommended to keep the device cool; however, water should not be introduced into the cavity

if possible. Care should be taken not to over etch the package, as doing so can cause the lid to shatter. The shards of the lid can be violently thrust into the cavity of the device, destroying bond wires and potentially the IC itself. An Isopropyl rinse and bake should take place after grinding. At this point, the remainder of the ceramic material should be fractured and removed using double sided tape (such as carbon tape) on a solid surface. A clean break should yield a cavity that looks like the one shown in **Figure 5.5**.
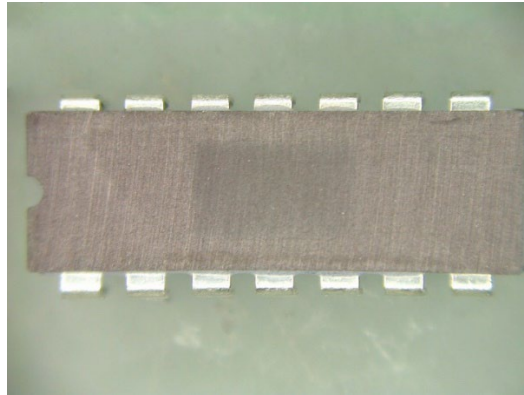
Figure 5.4. Mostly ground ceramic package after pre-cavitation process. Device is ready for de-lidding.
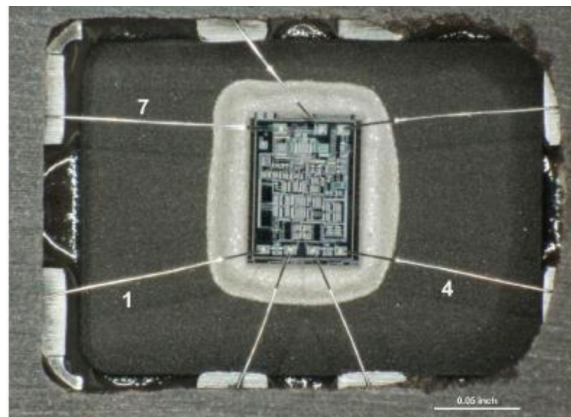
Figure 5.5. Fully de-lidded ceramic cavity showing the exposed die and wirebonds.

The easiest package to open is perhaps the TO-style can. While there are several approaches, the simplest is to acquire a "can-opener" intended for this style of package. The can is turned (either automatically or by hand) with a set of wheels that apply pressure to a circular blade, slowly carving into the can. During this process, the bond wires should not be disturbed. The finished de-lidded can should look like **Figure 5.6**.
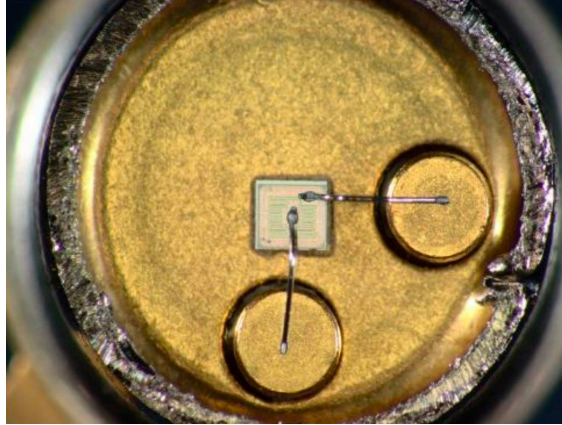
Figure 5.6. *De-lidded TO-style metal can package.*

When using these mechanical techniques for device preparation all debris must be removed from the package. Conductive debris can cause intermittent or permanent device failure. Debris of any sort can block the laser from reaching any sensitive volumes located under the debris.

Plastic Encapsulated Microcircuits. Unlike hermetic packages, plastic encapsulated microcircuits (PEMs) require a different process to ensure optical access to the sensitive volumes during PL SEE testing. Furthermore, there are differences in the specific process utilized depending on the purpose of this decapsulation (*e.g.*, construction analysis, destructive physical analysis, or failure analysis). This section applies to all plastics encapsulated devices, but the various techniques depend on both the encapsulant and the IC construction material. However, the general approach is the same and the process is outlined in **Figure 5.7**. A description of each step follows.
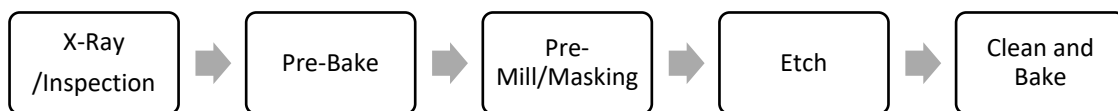

Figure 5.7. *General approach for decapsulation of PEMs.*

1. **X-Ray or Destructive Inspection.** X-ray analysis should be performed prior to decapsulation to determine the size, location, and bond wire placement. This information will allow for a higher initial decapsulation yield. If an X-ray machine is unavailable, and there are several, inexpensive samples, one may destructively determine construction by submerging the entire device in fuming nitric acid and inspecting the remains. This is a brute-force approach, and X-ray inspection is always recommended. Regardless of the approach, documentation, including pre-inspection photographs and X-ray imaging is recommended, as exemplified in **Figure 5.8**. If using X-rays, the imaged device should either be discarded, or the dose delivered to the device should be known. Real time X-ray machines and CT inspection can easily deliver several krads(Si) of total dose to a device, which can either change the parametric characteristics of a device, cause functional failure, and/or induce undesired synergistic SEE/TID effects [53].
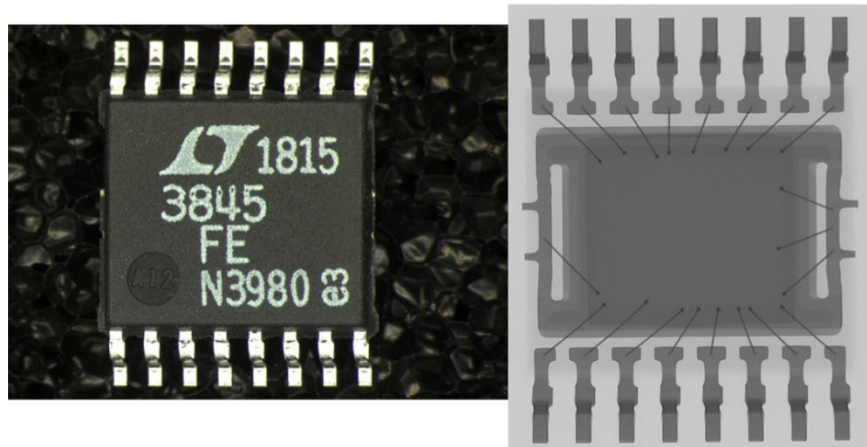
Figure 5.8. *Photograph of encapsulated IC and X-ray photograph of the same IC.*

2. **Preliminary Bake Out.** While not required, it is recommended that PEMs be subjected to a 12-24 hour bake at 125 °C to eliminate any moisture in the epoxy. This step will reduce the likelihood of corrosion in the copper lead frames and bond wires during a wet etch.

3. **Pre-cavitation and Masks.** Pre-cavitation uses mechanical methods to begin carving a cavity in the package. While not required, pre-cavitation is recommended prior to a wet etch and a plasma etch. This step reduces the length of the etching process and, in the case of the wet etch, provides an initial cavity for the acid, which prevents spills and reduces the likelihood of damage to the edges of the package and leads. Any appropriate milling machine can be used, providing the bit is small enough to work within the package dimensions, and the dimensional controls are fine enough not to over-mill the device (an example of this process is shown in **Figure 5.9**). Detailed procedures are provided in [54]. Alternatively, laser ablation can be used to pre-cavitate the package. While a thorough discussion of different types of masks is outside the scope of this document, masks are applied to isolate the portion of the package that will be etched in the following step.
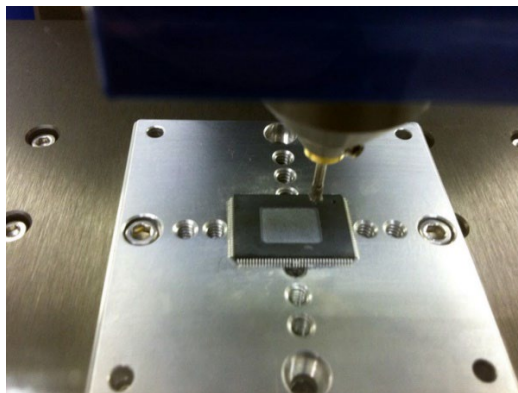

Figure 5.9. *Mechanical pre-cavitation of PEMS from (UltraTec USA, 2019).*

4. ***Etching.*** There are five general etching approaches for decapsulation of PEMs: manual wet etch, automated wet etch, laser ablation, plasma etching, and an immersing wet etch (along with varying combinations of the aforementioned techniques). The appropriate etching approach will depend on the construction of the DUT, as well as the availability of chemicals and equipment.

5. ***Clean and Bake.*** After decapsulation, the DUT should be cleaned and baked. The appropriate cleaning step will depend on the decapsulation method used. After the appropriate cleaning, another bake session at 100 °C for 12 hours is suggested to remove all residual moisture from the package.

5.3.2 Flip-Chip Components

With flip-chip devices, it is not uncommon for a die to be directly attached onto a printed circuit board (PCB). Thus, decapsulation or de-processing is typically not required. For flip-chip devices through-wafer SEE testing for both heavy ions and pulsed laser will be necessary because any de-processing of the part to access the top side would sever the electrical connection to the package. Therefore, the only required pre-processing step is back-side thinning and polish.

However, with larger die sizes and PCB-based packaging, curved and warped die have become increasingly common. Center-to-edge warpage of 20 µm is quite common, and values of hundreds of microns have also been observed [55]. The issue occurs when there are thermal expansion mismatches between different materials in the package. Back-side thinning of a warped die can lead to a sudden relaxation of pressure and cause die cracking. To solve this problem, several companies have developed tools such as thermal stages, which relax the die, and three-dimensional software that uniformly thins the substrate.

Typically, devices are thinned down to around 60 µm to 80 µm of remaining silicon for heavy ion testing. Before beginning the actual thinning process, one must know starting die thickness. Some manufacturers will provide nominal thickness values, but these often have a tolerance of up to 2%. If die thickness information is not available from the manufacturer, additional techniques could be used such as taking a device cross-section on a sacrificial device or using interferometric or other light-based measurement techniques [55].

When thinning a warped die, both die thickness and uniformity must be considered. While substrate uniformity could be as significant problem for heavy-ion testing, it can also add challenges to PL SEE testing. When using through-wafer SPA, variations in thickness will lead to differences in beam attenuation, resulting in different deposited charge across the die. These differences can be subtle or significant, depending on the substrate doping level. For through-wafer TPA, focus is extremely important, and thickness uniformities could add unnecessary complexities to the experimental procedure. Therefore, while additional thickness variations can be accommodated and even compensated by PL SEE testing, a uniform thickness would significantly simplify experiments.

Finally, if an evaluation board is necessary for testing, thinning the part while mounted on the board is recommended because this approach reduces time and cost, and increases reliability.

5.3.3 Bare Die

Sometimes, a simpler alternative to de-processing is to procure a bare die from a manufacturer, if available. In this case, no additional processing on the die is needed for top-side access, as long as wirebonds do not obstruct the laser.

One potential advantage of obtaining bare die is that through-wafer access can be more easily facilitated by designing a custom board. In this case, it is possible to drill a hole in the printed circuit board and to attach the die over the hole. An example of this approach is shown in **Figure 5.10**. This is often achieved using epoxy and can be challenging depending on the size of the chip, the size of the chip relative to the hole, and the location of the circuits of interest on the chip. Care must be taken to optimize the mechanical stability of the epoxied chip, while not smearing epoxy over the areas of the chip that are of interest. In such configurations, the microscope objective should have a long working distance, and the hole in the board should be sufficiently large so that the beam is not obstructed. Note that the general considerations provided in **Section 5.2.1** to ensure a polished surface still apply and some minor processing (*i.e.,* die thinning and polishing) might be required prior to attaching the die on the board.
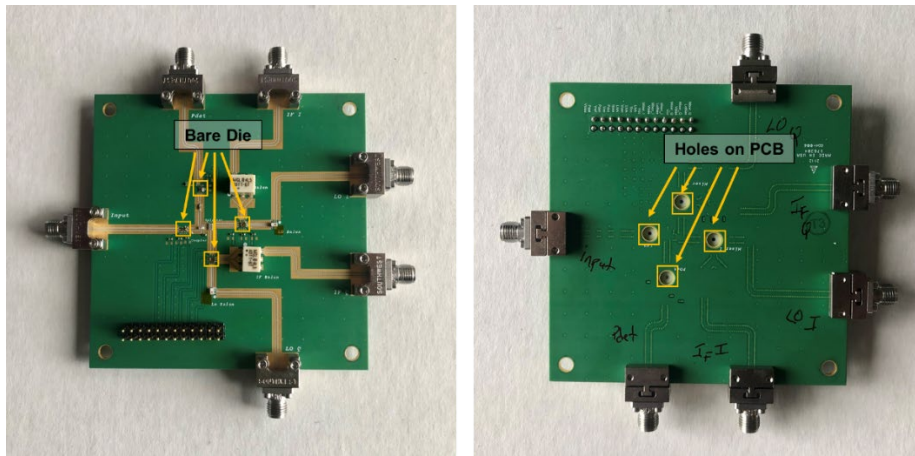
Figure 5.10. *Top view (left) and back view (right) of an example board design with bare, wire-bonded die mounted on a PCB that provides back-side access via drilled holes.*

5.3.4 General Comments

Semiconductor de-processing is a practice driven by the field of failure analysis. Most of the techniques that have been discussed here evolved with the goal of destructive physical analysis, part construction analysis, and failure analysis. The International Symposium for Testing and Failure Analysis (ISTFA) is an excellent resource to learn more about de-processing techniques [56]. Fortuitously, for most failure analysis applications, the die must be polished without scratches, similar to the mirror-finish requirements for PL SEE testing. As a result, most companies that work in the field of failure analysis should be proficient in providing a polished surface. The topics covered in this chapter should help radiation engineers communicate surface quality requirements to companies that specialize in de-processing.

Not every component can be de-processed. The trends toward 3-D integration in electronic packaging effectively eliminates historically standard radiation hardness assurance techniques, of which PL SEE can now be considered, and necessitates alternative approaches. The failure analysis community is currently addressing de-processing approaches for 3-D integrated components, yet the techniques will ultimately be partially destructive [57].

Because of the unique challenges that arise from PL SEE testing compared to heavy ion testing, planning ahead is key. The most successful strategy in this regard is to always assume PL SEE testing will be required, from the earliest stages in the design and planning process. Key decisions made early regarding DUT package and board design can either enable or prevent a successful PL SEE test, if deemed necessary at a later time.

5.4 RELEVANT CONSIDERATIONS FOR DUT PREPARATION

The following list of questions summarizes the many considerations discussed in this chapter regarding DUT preparation. These questions should be evaluated when deciding to test a given component at a pulsed laser facility.

- What is the material system (*e.g.*, Si, GaAs, GaN, SiC) and/or fabrication process used for the DUT?

- What wavelength do you intend to use? Can the laser facility provide it?

- Or, similarly, can you use one of the wavelengths provided by the facility?

- What type of metal coverage is expected for this device type (*e.g.*, most likely dense for highly scaled digital chips, less dense for legacy analog chips) and how does this affect the feasibility of pursuing PL SEE testing?

- After considering the metal coverage, DUT type, package, and material system, should you aim for top-side or back-side excitation?

- Is it possible to perform the required de-processing in-house, or should a vendor be contacted?

- Are there bare die available, and would packaging be simpler than de-processing?

6 PRACTICAL GUIDANCE – EXAMPLE CASE STUDIES

This chapter discusses practical guidance that is valuable when using PL testing to investigate specific SEE mechanisms. Each section of this chapter is devoted to a specific mechanism: single-event latchup (SEL), single-event upsets (SEU), single-event functional interrupts (SEFI), analog and digital single-event transients (ASET, DSET), transient charge-collection for basic mechanisms studies, and single-event burnout (SEB). Every section includes a general definition for the SEE mechanism, typical goals specific to PL testing, general experimental procedures, data acquisition and equipment considerations, and measurement challenges that may be encountered. Finally, each section will conclude with example case studies along with published references that include more detailed descriptions.

6.1 SINGLE-EVENT LATCHUP (SEL)

6.1.1 General Definition

Single-Event Latchup (SEL) occurs in CMOS integrated circuits (ICs) when the charge deposited by an ion causes disruption by turning on the two parasitic bipolar transistors between a CMOS well and substrate inducing a high-current latch-up condition [58, 59]. This sudden, large current surge may physically damage the IC. While SEL is generally non-destructive, it can be debilitating since its occurrence can necessitate a full chip power-down to remove the condition. For very sensitive chips, these resets might occur often enough to interfere with the general mission of a spacecraft or electronic system. In some cases, if enough current is drawn, latent or catastrophic damage can become so severe that the IC stops operating. In any case, engineers are wise to avoid using SEL-sensitive ICs for space applications. In terms of commercial off-the-shelf (COTS) parts, the PL approach often is used as a pre-screening for SEL sensitivity prior to heavy-ion measurements: laser sensitivity can quickly and efficiently flag susceptible parts, eliminating them from further consideration. Implementation of laser interrogation as the initial step in the screening process can result in significant cost savings in terms of both personnel time and accelerator costs. Both SPA and TPA approaches can be utilized for screening and characterization, as appropriate.

6.1.2 Specific Goals of PL SEE Testing

- To determine if the part is SEL sensitive – a binary screening procedure (SEL/no SEL)
- To determine the physical cross-section of the sensitive area/region
- To determine a part's LET threshold (LET_{th}) for SEL
- Locate and identify the SEL sensitive regions of the chip (allows for implementation of mitigation techniques that are efficient in terms of development time and chip area)
- Determine whether the latchup events are damaging or not
- Determine whether repeatedly triggering latchup in the same location could eventually cause observable damage that could later lead to diminished lifetime
- Evaluation of SEL mitigation approaches

6.1.3 General Experimental Procedure

For SEL screening and to locate SEL sensitive regions:

- A part's susceptibility to SEL depends on its threshold relative to the laser's operating point: $LET_{th} < LET_L \rightarrow$ SEL, $LET_{th} > LET_L \rightarrow$ no SEL.

- Adjust the pulse energy to the desired LET_L operating point and monitor supply currents.

- Focus the beam into the active region and begin scanning the laser over the desired area.

- If an SEL is detected, record X, Y, Z position (a micrograph with the overlay of the laser spot and device is useful here).

- SEL detection is sufficient for screening, but scanning can continue to identify other sensitive regions.

- Reset power supplies and continue scan.

- Repeat as necessary, adjusting LET_L, if desired, to locate additional sensitive regions.

To determine a part's SEL threshold (LET_{th}):

- SEL threshold measurement is a tedious process; automation is suggested.

- Position the laser spot in an SEL sensitive location (identified as above) and perform fine X, Y, Z adjustments to find the most sensitive location.

- Lower the laser pulse energy (or LET_L) until SEL disappears, then re-optimize X, Y, Z.

- Repeat until SEL is no longer triggered; the lowest LET_L that triggers SEL is the LET_{th}.

- Repeat procedure as necessary to validate result; repeat at various SEL sensitive regions.

- To obtain the most accurate LET_{th} value sometimes requires manual iteration of X, Y, Z and the LET_L.

6.1.4 Data Acquisition and Equipment Considerations

- Typical PL SEE systems have a mechanism for scanning the beam relative to the surface of the part (*e.g.*, a programmable, motorized stage moving the sample or beam rastering).

- Software will need to monitor power supplies for SEL and have some sort of handshaking procedure to stop the scan, reset power supplies and restart the scan.

6.1.5 Measurement Challenges

- Accurate estimation of SEL location from top-side measurements is limited by BEOL metal coverage.

- SEL measurements using back-side measurements are susceptible to changes in focus. If a die is tilted, the shifting focus could result in missed SEL regions for large scan areas.

6.1.6 Example Case Studies

SEL Screening in COTS Parts

- Source: [60, 61].

- One early example of PL SEL screening for COTS parts is shown in **Figure 6.1**. This part, a Data Device Corporation (DDC) RDC19220 resolver-to-digital converter, was under consideration for a NASA space mission. Top-side scanning of the part using SPA at 590 nm reveals significant SEL-sensitive areas in the CMOS circuitry.
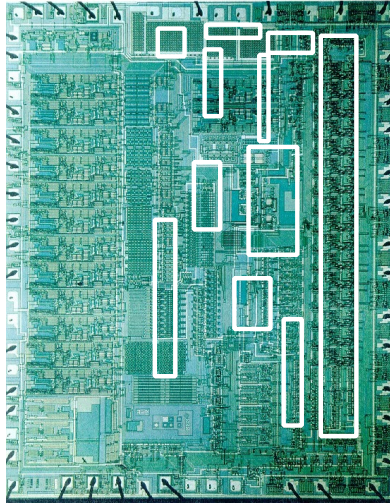
Figure 6.1. *Photomicrograph of a DDC RDC19220 resolver-to-digital converter for PL SEL testing. Significant SEL-sensitive areas in the CMOS circuitry are outlined in white boxes. After [60].*

- For this example, the laser-induced SEL threshold for 590 nm top-side PL excitation was measured to be 2.8 pJ, corresponding to 1.4 pC of deposited charge. Using the empirically-determined correlation factor of 1 pJ = 3 MeV·cm^2/mg demonstrated for bulk CMOS [13] (see **Section 6.2.6**), 2.8 pJ corresponds to a heavy-ion SEL threshold of 8.4 MeV·cm^2/mg.

- Based solely on this PL SEE result, with no additional heavy-ion testing performed, the DDC RDC19220 was eliminated from current and future NASA missions. This is one example of PL SEE screening being used to eliminate parts without any accelerator testing being required.

- It is worth highlighting that subsequent and independent heavy-ion measurements on the RDC19220 were performed at Brookhaven National Laboratory that established an SEL LET threshold between 5 and 15 MeV·cm^2/mg, in excellent agreement with the pulsed-laser prediction of 8.4 MeV·cm^2/mg.

SEL Identification and Mitigation in ASICs

- Source: [58, 61].

- The National Semiconductor (NS) DS90C031 low voltage differential signaling (LVDS) quad differential line driver, is a QML-V space-qualified CMOS part that was designed into the GPS-II global positioning system upgrade program. As the launch date was approaching, heavy-ion testing by NASA revealed (surprisingly) an unexpected SEL susceptibility, failing the mission requirements. The potential impact on cost and schedule was significant: scrubbing the launch due to this single part was a possibility.

- Top-side SPA excitation at 590 nm revealed that latchup was limited to a single, localized region in the circuit, labeled "B" in **Figure 6.2**. Charge injection in the region between the large drive transistor (D) and ground could trigger a parasitic PNPN silicon-controlled rectifier (SCR) with a latchup path involving the PMOS source at VDD, its associated N-well, the P-substrate, and the grounded end of the N+ resistor diffusion (C).
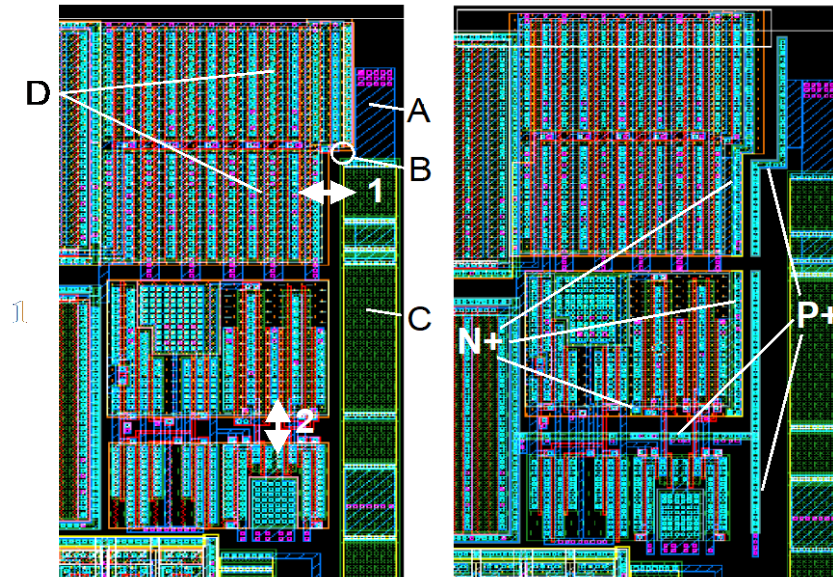
Figure 6.2. *Photomicrograph of a NS DS90C031 LVDS quad differential line driver for PL SEL testing. Denoted regions are described in the text. After [58].*

- Having identified the origin of the susceptibility, the designers at Boeing implemented layout changes: the PMOS drive transistor and the N+ resistor diffusion were moved further apart (1 and 2, above left), and P+ and N+ guard stripes that extended along the entire length of the resistor were inserted between the two (**Figure 6.2**, right). The part was re-fabricated by NS, retested at Texas A&M University by NASA, and found to be SEL-free. The GPS-II mission launched on schedule.

6.2 SINGLE-EVENT UPSET (SEU)

6.2.1 General Definition

When an energetic particle strikes a sensitive location in a memory cell, the resulting charge disturbance can be significant enough to reverse or flip the data state [59, 62, 63]. This phenomenon, known as a Single-Event Upset (SEU), is considered a soft error as no permanent damage is caused by the radiation event and the device will function properly if new data is written to the bit. The criterion for SEU is whether the collected charge (Q_{col}) exceeds a minimum amount of charge called the critical charge (Q_{crit}). While Q_{col} depends on a complex combination of factors (*e.g.*, sensitive volume, collection efficiency, bias, etc.), it is proportional to the deposited charge (Q_{dep}), which is more readily estimated. Consequently, the SEU criterion is often given as $Q_{dep} > Q_{crit}$. The ability of the laser to deposit a well-defined amount of charge in a well-defined area enables PL SEE testing to provide good discrimination for SEU thresholds and for mapping the sensitive regions.

6.2.2 Specific Goals of PL SEE Testing

- To determine the SEU laser threshold (the minimum amount of pulse energy needed to produce an upset) and/or LET_L threshold for the part

- Locate and identify the SEU sensitive regions of the chip

- To determine the physical cross-section of this sensitive area/region

- Unraveling a memory's bit-map (the translation from logical to physical address)

6.2.3 General Experimental Procedure

To map SEU sensitive regions:

- Set pulse energy (or LET_L) at a low to moderate level.

- Focus the beam into the active region and begin scanning the laser over the desired area.

- When an SEU is detected, record X, Y, Z position (a micrograph with the overlay of the laser spot and device is useful here).

- For each position, the DUT must be read, recorded, and reset; the read/write process should be completed before the next laser pulse is delivered.

- When testing a single cell for an SRAM (not unusual), it is advantageous to write/read only to that, and a few surrounding, cells; interrogating the entire memory is quite slow and unnecessary.

To determine a part's SEU threshold (LET_{th}):

- Automation is suggested in initial search to determine the SEU laser threshold measurement.

- Position the laser spot in an SEU sensitive location (identified as above) and perform fine X, Y, Z adjustments to find the most sensitive location.

- Lower the laser pulse energy (or LET_L) until SEU disappears, then re-optimize X, Y, Z.

- Repeat until SEU is no longer triggered; the lowest LET_L that triggers SEU is the LET_{th}.

- Repeat procedure as necessary to validate result; repeat at various SEU sensitive regions.

- To obtain the most accurate LET_{th} value sometimes requires manual iteration of X, Y, Z and the LET_L.

6.2.4 Data Acquisition and Equipment Considerations

- Typical PL SEE systems have a mechanism for scanning the beam relative to the surface of the part (*e.g.*, a programmable, motorized stage moving the sample or beam rastering).

- Software will need to read the target cell or cells for SEU and have some sort of handshaking procedure to stop the scan, record the event, and write to the cell/cells before restarting the scan.

6.2.5 Measurement Challenges

- Accurate estimation of SEU location from top-side measurements is limited by BEOL metal coverage.

- SEU measurements using back-side measurements are susceptible to changes in focus. If a die is tilted, the shifting focus could result in missed SEU regions for large scan areas.

- Subsequent pulses hitting different transistors within the same SEU-sensitive cell can re-flip a flipped bit.

- Modern devices have sensitive regions that are smaller than the focused laser spot size which could lead to multiple cells being upset.

6.2.6 Example Case Studies

SEU Sensitivity Mapping in an SRAM

- Source: [61, 64].

- An example of SEU sensitivity mapping using SPA excitation is illustrated in **Figure 6.3** for a custom SRAM test chip. Analogous types of maps can be generated for many types of SEE sensitivities.
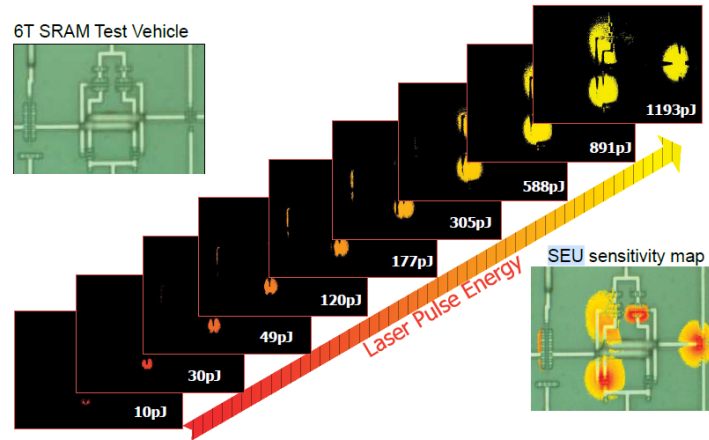
Figure 6.3. *SEU sensitivity maps generated for a specially designed SRAM test structure. The data (diagonally arranged) show the individual two-dimensional scans measured as a function of the laser pulse energy. The bottom right figure shows the SEU sensitivity map generated from the individual scans. After [64].*

- For a given laser pulse energy, a two-dimensional scan of the SEU sensitivity is performed. The data illustrate that the SEU-sensitive area increases as laser pulse energy increases in much the same way as cross-section increases with increasing heavy-ion LET. Combining these laser data sets and overlaying them on the device layout produces the SEU sensitivity map shown in the lower right-hand corner of **Figure 6.3**.

Empirical Correlation to Predict SEU Thresholds

- Source: [13, 14, 61, 65].

- Significant effort has been devoted to correlating PL SEE measurements with heavy-ion thresholds and cross-section measurements. In particular, early work focused primarily on empirically correlating laser pulse energy thresholds and thresholds derived from heavy-ion measurements. The first published report is an investigation of SEL in specially designed bulk CMOS test structures [14]. This investigation showed the SEL threshold as a function of well spacing and illustrated that SPA-based PL SEL threshold measurements correlate well with heavy-ion induced SEL measurements.

- This SEL effort was followed by [13], which collected laser and heavy-ion SEU data for several different bulk device types, mostly CMOS, down to the 0.25 μm node. The results of that study are reproduced in **Figure 6.4**, including the SEL results of [14]. These results established a laser/ion correlation factor of 1 pJ = 3 MeV·cm^2/mg for SPA excitation at 590-600 nm for a wide range of technologies and device types. This empirical correlation could then be used to predict heavy-ion thresholds on previously untested parts. Another example of the success of using empirical correlations for prediction is described in the case study in **Section 6.1.6**.
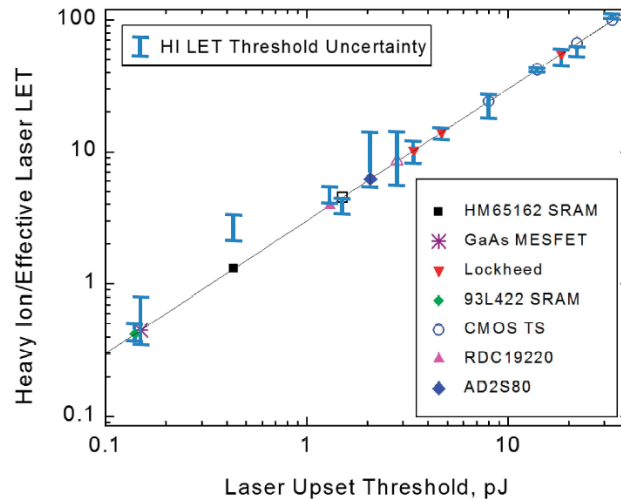
Figure 6.4. *Part LET threshold (LET$_{th}$) as predicted by laser upset measurements (symbols and line), compared with the heavy-ion threshold measurements (uncertainly bars) in units of MeV·cm^2/mg. The uncertainly bars are not error bars in the conventional sense, but rather represent the range between the lowest ion LET for which an error was detected, and the highest ion LET for which no error was detected. After [13].*

- As discussed in **Section 2.3**, empirical correlation approaches are quite useful laboratory tools when appropriate, but their utility is limited to the specific experimental conditions of the reference measurements. In particular, the correlation factor for the data of **Figure 6.4** has been validated for top-side SPA excitation at nominally 600 nm. Longer wavelength optical pulses, say 850 nm or 1064 nm, will possess smaller absorption coefficients and therefore require significantly larger laser pulse energies to produce a similar *LET*$_L$ (see **Section 4.2.2**). A tabulation of relevant SPA data, illustrating this point and the general trends, has been compiled and is given in [65]. Furthermore, for technologies with spatially-restricted sensitive volumes, the overlap of the charge profile with the sensitive volume must be explicitly considered (see **Section 4.3**).

Determining the Bit-Map of an SRAM

- Source: [1].

- Understanding the spatial distribution of SEUs can be important when calculating error rates based on measured heavy-ion induced SEU cross-sections. The error rate should reflect the total number of events but, since each event may consist of multiple bit upsets (frequently the case for high-density memories), the extracted rate could be inaccurate.

- If the logical-to-physical bit-map is known, interpretation of the SEU data is possible. However, manufacturers often consider this information proprietary and will not provide it. Fortunately, PL testing is well-equipped for determining a memory's bit-map. This is accomplished by generating an SEU in the cell of interest and recording its address. By repeating this process on physically adjacent cells until a pattern emerges, the bit-map can be constructed.

- **Figure 6.5** shows a physical bit-map of a simple SRAM (the 93L422, a 1-Kbit bipolar memory) reconstructed using PL testing. The bit-map was key in understanding the nature of the SEUs that were detected in that memory while in space. It was known that if two errors were produced in the same word, the error correction code would not be able to correct the errors. The

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reconstructed bit-map shows that, in some cases, bits of the same word are physically adjacent. Therefore, an ion intersecting the two adjacent bits could cause an upset in both and defeat the error correction code, something that was observed in on-orbit data. The SEUs generated from a glancing-angle, high-energy cosmic ray that caused this anomaly are illustrated in **Figure 6.5**.

107	105	121	119	103	101	117	115	99	97	113	126
43	41	57	55	39	37	53	51	35	33	49	62
11	9	25	23	7	5	21	19	3	1	17	30
206	201	217	215	199	197	213	211	195	193	209	222
235	233	249	247	231	229	245	243	227	225	241	254
171	169	185	183	167	165	181	179	163	161	177	190
139	137	153	151	135	133	149	147	131	129	145	158
139	137	153	151	135	133	149	147	131	129	145	158
171	169	185	183	167	165	181	179	163	161	177	190
235	233	249	247	231	229	245	243	227	225	241	254
206	201	217	215	199	197	213	211	195	193	209	222
11	9	25	23	7	5	21	19	3	1	17	30
43	41	57	55	39	37	53	51	35	33	49	62
107	105	121	119	103	101	117	115	99	97	113	126
75	73	89	87	71	69	85	83	67	65	81	94

Figure 6.5. *A portion of the physical bit-map of a simple SRAM reconstructed using PL testing. The cells in grey have two bits in the same word physically adjacent to each other. The outlined cells are those that experienced upsets as a result of a single high-energy cosmic ray strike while the device was in orbit. After [1].*

6.3   SINGLE EVENT FUNCTIONAL INTERRUPT (SEFI)

6.3.1   General Definition
Another type of soft error, known as a Single-Event Functional Interrupt (SEFI), results from an SEU in a system control register, such as those found in FPGAs or memory control circuitry [1, 59, 61, 63]. This error can lead to functional failure in a variety of forms, including a halt in operation or lock-up (no response to commands). Typically, this error cannot be reset with a simple write to the register and must be corrected by resetting the entire state of the device, either through a software restart, hard reboot, or power cycle. Experimentally, SEFIs in complex circuits can be difficult to detect and characterize. Even if a device does not exhibit SEFI during broad-beam particle-based testing, the test conditions and data need to be carefully scrutinized to ensure that the device is SEFI-free, and that the observations are not a result of inadequate test conditions. Conversely, a low SEFI threshold can interfere with SEU, SET, or SEL threshold determination in broad-beam ion tests. Due to its spatial selectivity, PL SEE can be utilized to separate SEFI from other effects. PL SEE methods can be very useful for identifying and characterizing the various types of SEFIs since charge can be injected directly into the offending register, permitting detailed evaluation of its characteristics and behavior, such that mitigation approaches can be developed.

6.3.2   Specific Goals of PL SEE Testing
- To determine the SEFI laser threshold (the minimum amount of pulse energy needed to produce an upset) and/or LET_L threshold for the part
- Locate and identify the regions (or specific registers) on the chip sensitive to SEFI

- To determine the physical cross-section of this sensitive area/region

- To explore the wide range of test conditions that could lead to SEFI, either before heavy-ion testing to map out the origin of various error modes or for post-testing rationalization of a complicated array of error signatures

6.3.3 General Experimental Procedure

To find SEFI sensitive regions (or specific registers):

- Set pulse energy (or LET_L) at a low to moderate level.

- Focus the beam into the active region and begin scanning the laser over the desired area.

- When a SEFI is detected, record X, Y, Z position (a micrograph with the overlay of the laser spot and device is useful here).

- For each position, depending on the nature of the SEFI, the DUT must be reset (*e.g.*, a power cycle, software restart, or rewrite to the particular register that is upset); this reset process should be completed before the next laser pulse is delivered.

To determine a part's SEFI threshold (LET_{th}):

- Automation is suggested to determine the SEFI laser threshold measurement.

- Position the laser spot in a SEFI sensitive location (identified as above) and perform fine X, Y, Z adjustments to find the most sensitive location.

- Lower the laser pulse energy (or LET_L) until SEFI disappears, then re-optimize X, Y, Z.

- Repeat until SEFI is no longer triggered; the lowest LET_L that triggers SEFI is the LET_{th}.

- Repeat procedure as necessary to validate result; repeat at various SEFI sensitive regions.

6.3.4 Data Acquisition and Equipment Considerations

- Typical PL SEE systems have a mechanism for scanning the beam relative to the surface of the part (*e.g.*, a programmable, motorized stage moving the sample or beam rastering).

- Software will need to read the register for SEFI and have some sort of handshaking procedure to stop the scan, record the event, and reset the DUT before restarting the scan.

6.3.5 Measurement Challenges

- Accurate estimation of SEFI location from top-side measurements is limited by BEOL metal coverage.

- SEFI measurements using back-side measurements are susceptible to changes in focus. If a die is tilted, the shifting focus could result in missed SEU regions for large scan areas.

6.3.6 Example Case Studies

SEFI Mapping in an FPGA

- Source: [1, 66].

- The PL SEE testing enables injection of faults (SEUs in registers and memories) at known physical locations. This aids in assessing the impact of a given injected fault on the application running at the time of the fault injection.

- As an example of this capability, long-wavelength SPA excitation (1064 nm) was used to inject errors over a large area of a 180-nm FPGA [66]. **Figure 6.6** shows a map of the regions in the configuration memory that were sensitive to SEUs. The FPGA was configured to execute a specific application using a specific design, and the laser was used to probe the configuration memory. At each strike location the output of the FPGA was monitored to determine when an error triggered in the configuration memory caused a failure in the operation of the component.

- **Figure 6.6** shows the same area scanned when the FPGA was loaded with a specific application. The figure shows the locations of SEUs in the configuration memory and the color codes indicate the different types of resources affected when operating at the application level. Comparing the two maps shows that only 14% of the injected errors in this part of the configuration memory actually cause SEFIs when running an application. This exercise illustrates the capability of the pulsed laser to act as a fault injection tool for complex digital components.
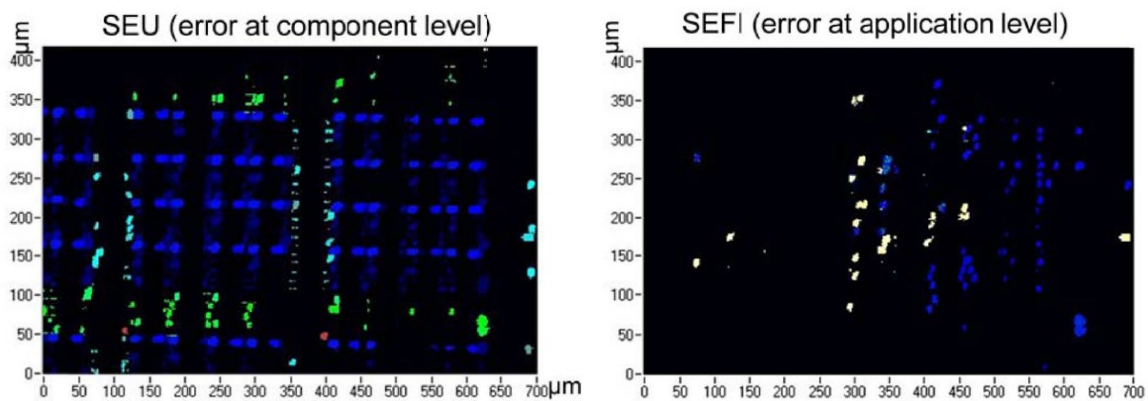
Figure 6.6. *Laser-generated map of the areas in the configuration memory of an FPGA sensitive to SEUs (left) and sensitive to SEFIs at the application level (right). Comparison of the two maps reveals that only 14% of the SEUs triggered by the laser actually induce SEFIs. After [66].*

6.4 ANALOG SINGLE EVENT TRANSIENT (ASET)

6.4.1 General Definition

Analog Single Event Transients (ASETs) occur in analog or mixed-signal devices when the charge deposited by an ion passing through a sensitive node is collected by an electric field, inducing a current or voltage transient on the device contacts. Radiation-induced ASETs are a concern for microcircuit designs in the space environment where downstream circuitry depends on their functionality.

6.4.2 Specific Goals of PL SEE Testing

- Identify the ASET sensitive regions of the chip

- Identify worst-case operating conditions for ASETs

- Determine the effectiveness of externally applied mitigations strategies (e.g., filters)

- Evaluation of RHBD techniques to mitigate ASETs (e.g., changes to circuit topology and physical layout)

6.4.3 General Experimental Procedure

To find ASET sensitive regions:

- Set pulse energy (or LET_L) at a low to moderate level.

- Focus the beam into the active region and begin scanning the laser over the desired area.

- Record ASET and position at which event is observed.

- Once scan is finished, repeat scan at larger pulse energy until LET_L is high enough to generate worst-case ASETs and record event.

To determine a part's ASET threshold (LET_{th}):

- Position the laser spot in an ASET sensitive location (identified as above) and perform fine X, Y, Z adjustments to find the most sensitive location.

- Lower the laser pulse energy (or LET_L) until ASET disappears, then re-optimize X, Y, Z.

- Repeat until ASET is no longer triggered; the lowest LET_L that triggers ASET is the LET_{th}.

- Repeat procedure as necessary to validate result; repeat at various ASET sensitive regions.

6.4.4 Data Acquisition and Equipment Considerations

- Typical PL SEE systems have a mechanism for scanning the beam relative to the surface of the part (*e.g.*, a programmable, motorized stage moving the sample or beam rastering).

- Software will need to monitor device contacts for ASET and have some sort of handshaking procedure to record the location of the ASETs during the scan.

- Recording pertinent information about worst-case ASETs (*e.g.*, amplitude, duration) are important for board-level filter design.

- It is critical to test in the same configuration as the intended application because each configuration leads to different transient shapes.

6.4.5 Measurement Challenges

- Accurate estimation of ASET location from top-side measurements is limited by BEOL metal coverage.

- ASET measurements using back-side measurements will be very susceptible to changes in focus. If a die is tilted, the shifting focus could result in missed ASET regions for large scan areas.

- If the ASET duration is longer than the laser pulse repetition rate, the part will not be allowed to return to equilibrium condition, which could distort the measured ASET in significant ways.

- ASETs are highly dependent on the charge distribution (CD) profiles. If the appropriate CD is not used, it might be difficult to evaluate the efficacy of external mitigation approaches.

6.4.6 Example Case Studies

Identifying ASET Sensitive Regions: LM124 Operational Amplifier

- Source: [11, 15].

- Significant effort has been expended investigating ASETs in the LM124 operational amplifier. **Figure 6.7** shows a comparison of the selected LM124 SETs measured from irradiating the LM124

with high-energy ions and optical pulses with a 590 nm wavelength [11]. The various pulse shapes are indicative of ion/laser strikes on different transistors.

- Because the part was exposed to a broad beam of ions, it was impossible to relate SET shapes to any specific transistor response using ion data only. For the data shown in **Figure 6.7** the largest amplitude SETs representative of each pulse shape were selected from the heavy-ion data (to represent the worst-case), and these were matched up to corresponding SET shapes generated for pulsed laser irradiation. This procedure allows the different transistors responsible for the different pulse shapes measured with the broad-beam heavy-ion irradiation to be identified. The final knob used to obtain the laser-ion agreement shown in **Figure 6.7** involves adjusting the laser pulse energies to match the amplitude of the heavy-ion SETs.
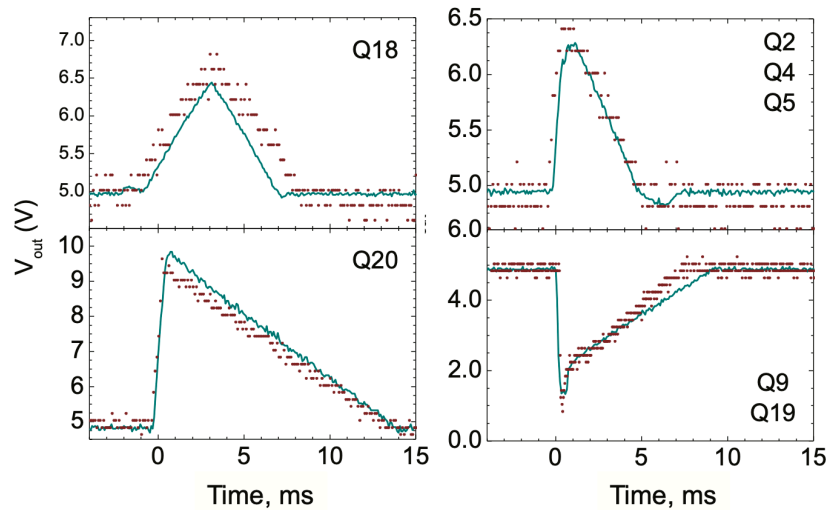

Figure 6.7. *SET waveforms measured for selected LM124 transistors via broad-beam heavy-ion excitation and SPA-based excitation at 590 nm. Laser pulse energy optimized to match amplitude of worst-case SET measured for each pulse shape. Xe ion, LET = 53.9 MeV·cm²/mg; device configured as a voltage follower with input 1V and supply of +/- 15 V. After [11].*

- It is important to reiterate that the conditions that enabled this laser-ion agreement are specific to this particular PL testing configuration (see **Section 2.3** that discusses empirical correlation approaches). In particular, significant differences in the ASET response of the LM124 operational amplifier have been found when employing different wavelengths for SPA testing and different focusing geometries for TPA testing [16, 17, 67].

ASET Screening: LM124 Operational Amplifier

- Source: [26].

- A primary goal of ASET screening typically is to determine the worst-case transients for a given device for the configurations of interest. These worst-case transients can then be used to evaluate their effect on the follow-on circuitry. Depending on the results, it is determined by the circuit/box designers whether (i) the part is acceptable as is, (ii) the part is acceptable with additional mitigation required, or (iii) the part is unacceptable for the given application.

- A convenient methodology for characterizing ASET pulses was developed for heavy-ion irradiation, and then adapted to PL irradiation [26, 27, 68]. This approach is referred to as the V-

Δt methodology. In this approach, data, such as those shown in **Figure 6.7**, are re-plotted such that the SET pulse amplitude (V) is plotted as a function of the SET pulse width (Δt). An example for the LM124 is shown in **Figure 6.8**, showing both ion and laser data for the same configuration and bias as for **Figure 6.7**.
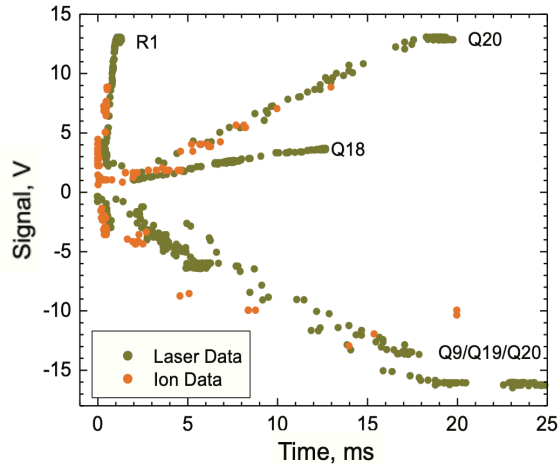

Figure 6.8. V-Δt representation of SET data collected for an LM124 operational amplifier SPA-based excitation at 590 nm and 1.3 GeV, 53.9 MeV·cm²/mg LET Xe ions. Device configured as a voltage follower with V_{dd} = +/-15 V and V_{in} = 5 V. After [26].

- For broad-beam heavy-ion measurements, all transients are collected, stored, and post-processed to extract the pulse amplitude and pulse width for each. A similar approach is used for the PL SEE measurements, except that, because of its intrinsic spatial selectivity, the device is scanned, and transients are recorded as a function of x-y position and laser pulse energy (there are various approaches to this). This process can be automated, or, depending on the complexity of the part, can be performed manually. Each data point in **Figure 6.8** corresponds to a measured transient originating from a single ionizing particle for the heavy ion data, or a single optical pulse for the laser data.

- For SET screening, it's critical to perform the laser and/or ion tests in the same configuration as the intended application, because each configuration leads to different transient shapes, and different V-Δt plots.

*RHBD Evaluation of a Voltage Regulator*

- Source: [69].

- PL SEE testing was performed on multiple Aeroflex voltage regulators to examine effects of circuit conditions on ASETs. This test campaign took advantage of the various strengths of the PL SEE technique.

- The laser was used to verify the experimental setup. Specifically, the use of an electronic load for SET measurements was validated by comparing the resulting ASETs with those generated when using a physical resistor. The ASETs for both conditions, shown in **Figure 6.9**, are strikingly similar, suggesting that electronic loads are adequate for this particular measurement.

- Due to the spatial selectivity of the pulsed laser, the dependence of the output ASET on the input voltage when charge is deposited at a fixed location on the chip could be evaluated. The measured ASETs are shown in **Figure 6.9**. These are examples of how heavy-ion beam time can be saved by performing validations using a pulsed laser.
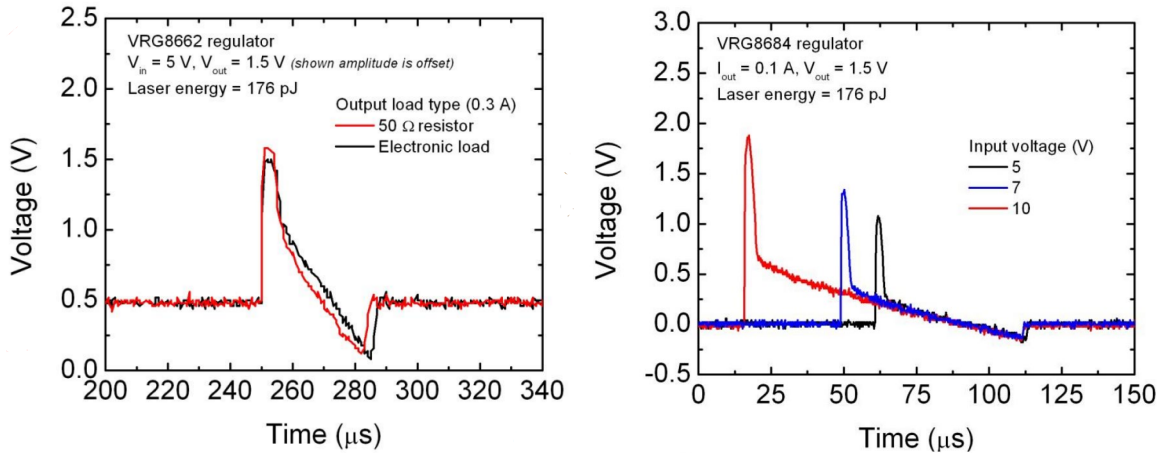
Figure 6.9. *Comparison of ASETs generated in a voltage regulator with an electronic load and a physical resistor (left). The similarity between both traces validates the use of an electronic load in place of a physical resistor for this experimental setup. Comparison of ASETs generated in a voltage regulator for different input voltages when the laser is focused at a fixed position (right). The positive part of the ASET and total duration are a strong function of input voltage, but the negative part remains unchanged. After [69].*

- Finally, ASETs with and without filtering were compared to see the efficacy of a filter on the output voltage as a mitigation approach (see **Figure 6.10**). Filtered ASETs had a shorter duration and a smaller amplitude than non-filtered ASETs. This measurement is an example of how the pulsed laser can be used to verify system-level RHBD approaches.

- Other conditions that were tested include comparisons of heavy-ion- and PL-induced ASETs, effects of load on ASET response, effects of input voltage on ASET response, and a comparison of ASET response by Aeroflex part number.
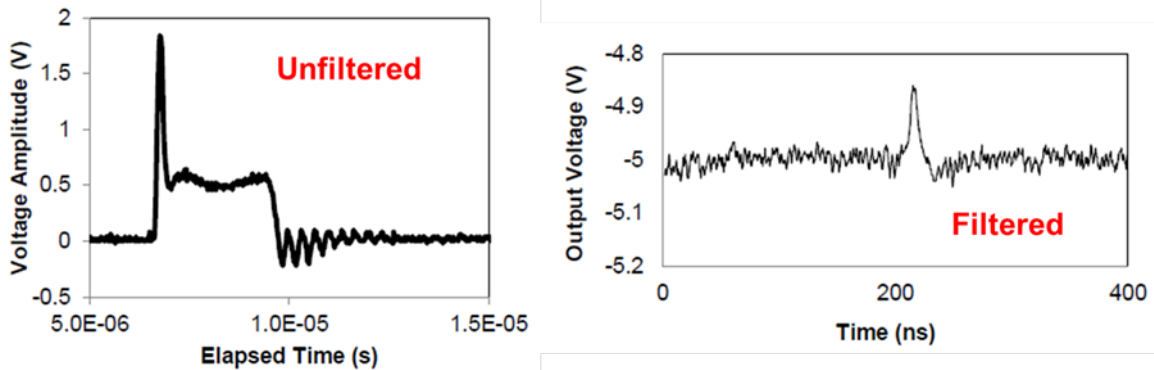

Figure 6.10. *ASETs with and without filtering were compared to see the effect of filtering on the output voltage. After [69].*

Analog-to-Digital Converter ASET

- Source: [70].

- PL SEE and heavy-ion SEE testing was performed on an Aeroflex ADC in an effort to characterize distortions in ASET amplitude as LET increases.

- The strike location at which an ASET occurs affects the observed response. The pulsed laser was used to identify the locations corresponding to specific ASET characteristics, including the frequency-response of the different ASETs (see **Figure 6.11**).

- Laser-induced SETs were used to inform the results of heavy-ion testing, and several effects were explained due to the unique capabilities of the pulsed laser. For example, a single clock error (**Figure 6.11** – middle, right) resulted in five data errors (**Figure 6.11** – middle, left). Due to spatial and temporal localization offered by the pulsed laser, this observation was attributed to the pipeline architecture of this ADC.
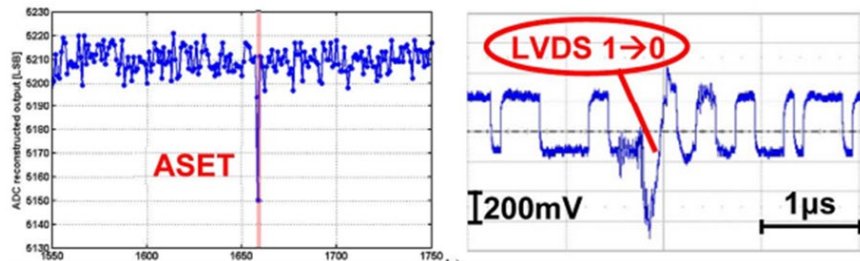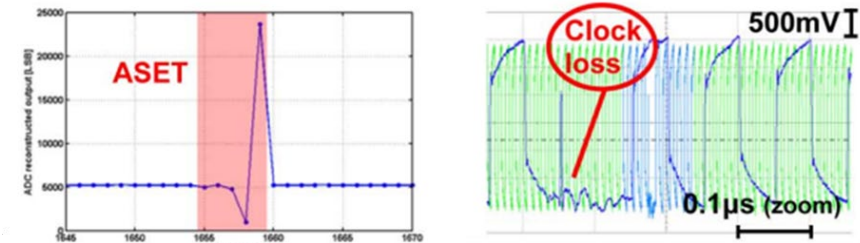
Figure 6.11. *Results from a laser strike on the LVDS output (top). Result from a laser strike on the clock driver (middle). Result from a laser strike on the internal voltage reference (bottom). The left plots show the ADC output, while the right plots show the oscilloscope snapshots for the same transient event. After [70].*

6.5 DIGITAL SINGLE EVENT TRANSIENT (DSET)

6.5.1 General Definition

DSETs refer to ionization-induced transients generated in combinational logic. DSETs themselves are generally not problematic; it is the possibility that they can be latched into follow-on circuitry that poses the problem. PL measurements typically are used to characterize the properties of DSETs in combinational logic to help evaluate their potential impact on ICs operating in radiation environments. Understanding how these properties change for a given technology node as a function of various design parameters permits intelligent design choices for IC design.

6.5.2 Specific Goals of PL SEE Testing

- Locate and identify the regions on the chip sensitive to DSETs

- Characterize DSET parameters including intrinsic SET width, SET propagation characteristics (broadening, compression), sensitivity to the location of the charge generation, the relative sensitivity of PMOS vs. NMOS transistors, etc.

- Evaluate schematic-level design parameter space (*e.g.*, drive strength, transistor dimensions, etc.) and layout-level (*e.g.*, node spacings, guard ring placement, common centroid vs. alternative layout approaches, etc.)

- Evaluate masking probabilities (*e.g.*, logical or temporal masking) of a DSET that originates at a specific location of a circuit

6.5.3 General Experimental Procedure

Approaches for DSET detection:

- There are two primary approaches to DSET measurement and characterization: direct measurement using a high-bandwidth, high-impedance output buffer [25], and indirect measurement using an on-chip pulse-width detection circuit [71, 72].

- These two approaches are suitable for both PL and particle accelerator testing. Particle accelerators result in a random distribution of particle strikes on the DUT, generally giving rise to a broad distribution of pulse widths being detected, whereas the primary advantage of PL SEE DSET measurement is its spatial selectivity, permitting detailed interrogation of the consequences of strike location on SET generation and measurement.

To find DSET sensitive regions:

- Set pulse energy (or LET_L) at a low to moderate level.

- Focus the beam into the active region and begin scanning the laser over the desired area.

- Record DSET and position at which event is observed.

6.5.4 Data Acquisition and Equipment Considerations

- Typical PL SEE systems have a mechanism for scanning the beam relative to the surface of the part (*e.g.*, a programmable, motorized stage moving the sample or beam rastering).

- Direct measurement requires (i) appropriate circuit design (on a high-speed package) including a high-bandwidth output buffer suitable for driving a high-impedance scope probe, (ii) a single-shot,

high-speed oscilloscope (bandwidth ≥ 16 GHz), and (iii) a high-impedance, high-bandwidth scope probe.

- Indirect measurement requires (i) circuit design with pulse-capture circuit suitable detecting and binning the generated DSETs, and (ii) the appropriate measurement electronics for reading the digital output of the capture circuit.

6.5.5 Measurement Challenges

- The primary challenge to PL DSET measurements arises from the difficulty of reproducibly injecting charge into specific transistors in recent-generation, highly-scaled technologies. To address this, special test structures sometimes are designed with increased separation between the n-MOS and p-MOS transistors.

- Mechanical and optical stability are especially important for PL DSET measurements, as is precision, reproducible X, Y, Z position control.

- For the direct measurement approach a primary challenge lies in design of the high-bandwidth, high-drive output buffer. Secondary challenges are associated more generally with chip and board design.

- For the indirect measurement approach a primary challenge lies in design of the self-triggered, on-chip measurement circuit. Since the original demonstration [72], on-chip measurement circuits have been improved and optimized to eliminate artifacts [71].

6.5.6 Example Case Studies

Evaluate Dependence of SEUs on Clock Rate

- Source: [73].

- Early PL SEE measurements of error rate as a function of clock frequency demonstrated the important role of clock frequency in the SEE response of combinational logic [73, 74].

- **Figure 6.12** illustrates (i) the linear dependence of error rate on frequency for inverter test structures, and (ii) for a given frequency, the error rate increases with increasing laser pulse energy. Similar dependencies have been reported for heavy-ion irradiation as a function of ion LET. The linear dependence arises because the number of clock edges increases linearly with frequency. The LET dependence is manifested in **Figure 6.12a** as an increase in the slope of the error rate vs. frequency curves with increasing laser pulse energy.

- That same study also verified that for sequential logic elements (in this case, a flip-flop), the error rate is independent of frequency. Combining the results for combinational and sequential logic in **Figure 6.12b** illustrates that, at low frequencies, the circuit is invariant with frequency because it is dominated by contributions from sequential logic; at higher frequencies the frequency-dependent effects of the combinational logic become significant and can dominate the SEE response. This frequency-dependent effect has made DSETs a dominant source of errors as technology scaling has driven clock rates higher.

- This study was uniquely enabled by the spatial selectivity of the pulsed laser. In addition, the repeating pulses that can be delivered at the same location allowed extraction of a "window of vulnerability," or the time period prior to a clock edge during which DSETs can be converted into upsets [74].
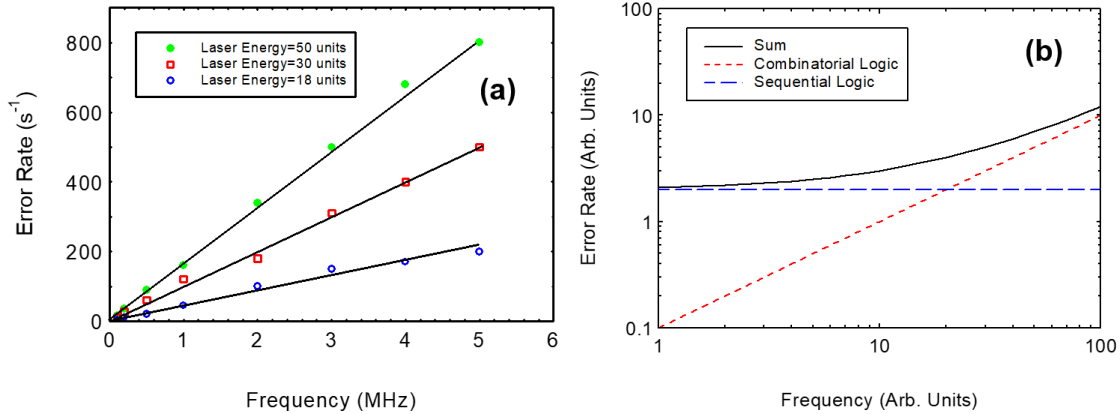
Figure 6.12. *PL SEE measurements of error rate as a function of frequency for three different laser pulse energies (a). The straight lines are best fits to the data. Error rate trends as a function of frequency for combinational and sequential logic elements (b), illustrating the dominance of combinational contributions at higher frequencies (note log scale). After [73].*

Propagation-Induced Pulse Broadening

- Source: [8, 9].

- The consequences of propagation-induced pulse broadening (PIPB) were first revealed by PL SEE measurements [8].

- That study utilized 800-inverter chains fabricated in 130-nm, partially-depleted silicon-on-insulator (PD SOI) CMOS. Measurements were performed using the direct measurement approach.

- Taking advantage of the spatial selectivity of the PL SEE approach, focused laser pulses were used to inject charge into four different locations along the chains: near the output, two in the middle of the chain, and near the input. The key experimental results are shown in **Figure 6.13**.

- These data reveal that SET broadening occurs as the transients propagate along the chain, with very short transients (approximately 200 ps) detected for charge injection near the chain output, and the longest transients (1.8 ns) detected for charge injection near the chain input.

- The average broadening per inverter for this test structure was determined to be 2 ps/inverter.

- This particular study using PL SEE testing revealed that the digital test structures that consist of long chains of inverters could artificially skew the distribution of measured DSETs in a heavy-ion environment.
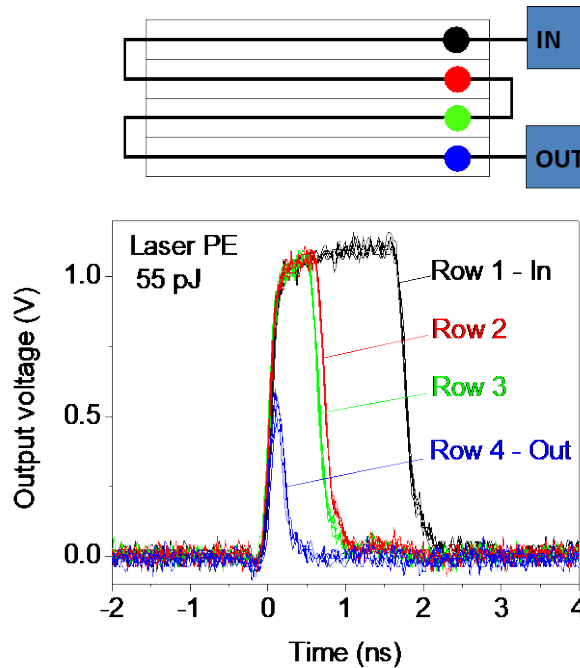
Figure 6.13. *Schematic diagram of an SOI inverter chain illustrating the snake-shape layout with the four laser strike positions indicated (color coded). Also shown are the voltage transients measured at the chain output as a function of the laser strike position. After [8].*

6.6 TRANSIENT CHARGE COLLECTION FOR BASIC MECHANISMS STUDIES

6.6.1 General Definition

Time-integrated charge-collection measurements traditionally have been the approach for investigating the basic mechanisms of charge transport, recombination, and collection at the single transistor level. Such measurements provide insight into the physics that occur when ionizing radiation interacts with semiconductor devices. This understanding is then used to improve the SEU performance of complex ICs through changes in device and/or circuit design. Such time-integrated charge-collection measurements are performed using nuclear counting approaches that involve charge-sensitive pre-amplifiers fed into multi-channel analyzers [75], and measure the total, time-integrated charge produced on a given node for each ionizing event.

The introduction of PL approaches for charge generation facilitated the development of transient charge-collection methodologies. The high-bandwidth sampling oscilloscopes (up to 70 GHz) used in early experiments were ideally suited for the periodic excitation provided by mode-locked laser sources [24, 25, 39, 76-80], but generally were not suitable for broad-beam heavy-ion measurements [76]. This is because the extensive signal averaging required by sampling techniques results in accumulated radiation damage that rapidly degrades the device characteristics [76] and also, averaging transients from different ion strike locations results in smeared-out averages that are not representative of any unique ion strike location.

More recent advances in oscilloscope technology have led to the development of single-shot oscilloscopes with sufficient bandwidth for transient charge-collection measurements [81-87]. The most recent generation of single-shot oscilloscopes exhibit bandwidths up to 70 GHz, although the practical minimum bandwidth for most high-frequency transient measurements is about 12 GHz. With these technological advances the transient charge-collection techniques that were initially developed for sampling approaches in the laser lab (high-frequency packaging, cabling, connectors, etc.), now have become the norm for transient capture across the radiation spectrum: pulsed laser, pulsed focused x-ray, broad-beam heavy-ion, heavy-ion microbeam, and proton broad-beam irradiation sources [83, 86-88].

6.6.2 Specific Goals of PL SEE Testing

- Utilize the unique characteristics of focused-laser charge injection (spatial selectivity, continuous control of the injected charge, and lack of radiation damage) to probe the basic mechanisms of charge transport and collection in single-transistor test structures

- Evaluate how device configuration (*e.g.*, device type, sizing, layout, bias) affects basic charge transport and collection mechanisms

- Map the charge-collection efficiency (*i.e.*, the sensitive volume) of test structures in X, Y, Z

- Compare the sensitivity of various semiconductor platforms to charge deposition events

6.6.3 General Experimental Procedure

- Most single-transistor experiments currently utilize high-bandwidth approaches since those yield the highest information content. The more traditional low-bandwidth, time-integrated approaches (typically involving DIP packaging and charge-sensitive pre-amplifiers) can provide useful information as well. Sometimes the two are used in combination. We focus here on high-bandwidth measurements.

- DUT is mounted on a precision X, Y, Z stage and connected to a high-bandwidth oscilloscope via high-frequency (typically >20 GHz) cables.

- Because of the lack of radiation damage, extensive experiments can be performed as a function of device bias conditions, injected charge density, and X, Y, Z position.

- Generated transients are stored and available for analysis post-processing.

6.6.4 Data Acquisition and Equipment Considerations

- High-bandwidth charge-collection measurements typically are performed using high-speed oscilloscopes, either sampling or single-shot (in contrast, single-shot scopes typically are required for particle accelerator measurements). The required bandwidth of the oscilloscope will depend on the particular response of the sample. A practical bandwidth of 12 GHz will cover many applications.

- The transistor is mounted in a high-bandwidth package, either using custom-designed printed circuit boards or other high-frequency, microwave package types, such as brass blocks with microstrip lines added.

- The device is wire-bonded to high-frequency transmission lines (microstrip or co-planar) with wire bonds kept as short as possible to minimize inductance.

- The signals from the transmission lines are launched into high frequency connectors (18 GHz SMA connectors represent the practical minimum bandwidth for most measurements). To minimize dispersion, high-bandwidth cables between the DUT and oscilloscope should be kept short, typically 3 feet or less.

- Triggering can be either external, triggered by the laser, or internal, depending on the specific goals of the experiment.

- As with all PL SEE measurements, mechanical stability is essential; this can be a challenge with stiff, high-bandwidth cables, especially when scanning in X, Y, Z.

6.6.5 Measurement Challenges

- High-bandwidth measurements have unique challenges associated with the transmission and measurement of picosecond-timescale pulses.

- The ringing associated with long bond wire inductances can easily swamp fast signals.

6.6.6 Example Case Studies

High-Bandwidth Measurement of Charge-Collection Transients

- Source: [24, 25].

- A schematic diagram of a representative transient charge-collection experimental setup is shown in **Figure 6.14a**, together with a charge-collection transient measured for a 50-nm fully-depleted SOI single transistor [24, 25].
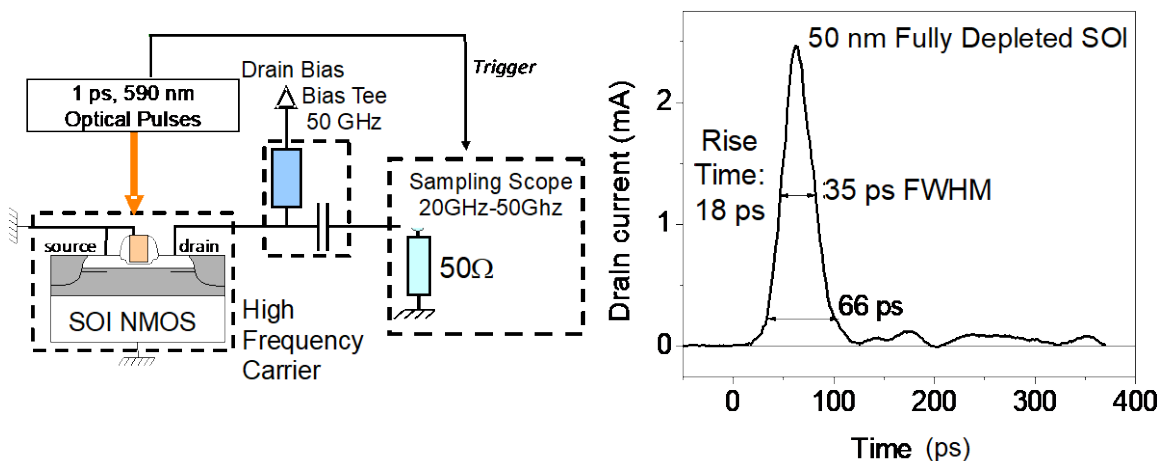
Figure 6.14. *Schematic diagram of the experimental setup with corresponding drain current transient for an off-biased 50-nm floating-body fully depleted SOI transistor measured into 50 Ω. After [24].*

- For these measurements, the DUT is mounted in a high-frequency (50 GHz) microwave package with the gate and drain wire-bonded to microstrip transmission lines, with the source grounded. The transient signals are passed through a 50 GHz bias tee and measured into 50 Ω in a using a high-bandwidth sampling oscilloscope with a 50 GHz sampling head.

- The measurements were collected at a 12 kHz laser pulse repetition rate. The small amplitude and fast recovery are consistent with expectations for a highly-scaled SOI device. The charge-

collection transient shown in **Figure 6.14b** represents the first such measurement on such a highly-scaled technology node.

- At the time of these measurements, analogous measurements for heavy-ion irradiation were not yet possible due to the lack of single-shot oscilloscopes of sufficient bandwidth, and also were complicated by the small cross-section associated with a single transistor in this highly-scaled technology.

Charge-Collection Mechanisms of III-V FETs

- Source: [79, 89].

- Technologies based on III-V FETs have a demonstrated sensitivity to SEEs. Early charge-collection measurements on III-V FETs revealed that the charge collected at the drain of the transistor could exceed the total charge generated by the ion or laser pulse [76, 79, 87, 89-92]. In fact, charge enhancement is the norm, rather than the exception in III-V FETs. For example, charge enhancement factors (CEF) of up to 60 have been reported for α-particle irradiation of GaAs HFETs [93]; the CEF is defined as the ratio of the collected charge divided by the charge generated by the ion or laser pulse.
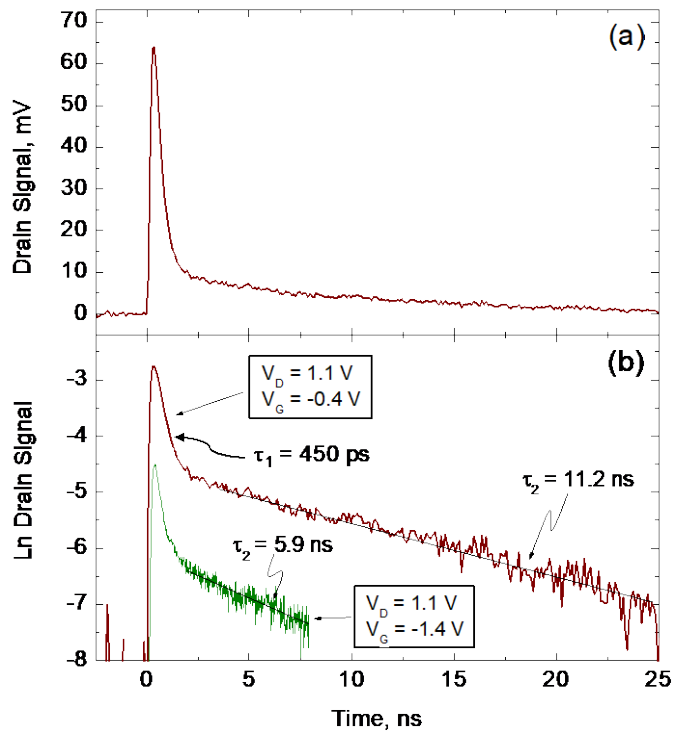
Figure 6.15. *Typical drain charge-collection transients measured for a 0.35 μm gate length, depletion-mode InP HEMT plotted in linear and logarithmic formats for the bias conditions indicated and 100 fC of deposited charge. After [89].*

- Analysis of transient charge-collection measurements in III-V n-channel FETs revealed that charge-enhancement is, to a large extent, a consequence of hole accumulation in, and below the active region of the device. One example illustrating the role of charge-enhancement process in an InAlAs/InGaAs HEMT device is illustrated in **Figure 6.15**, which shows representative laser-

induced charge-collection transients for SPA excitation at 590 nm [89]. The transients measured for these devices exhibit characteristics similar to those of other III-V devices, including: (i) a two- (or more) component relaxation, (ii) relaxation times and signal amplitudes that decrease as gate bias is made more negative, (iii) clear evidence for charge enhancement, in this case with CEFs of up to 33. These characteristics provide insight into the charge-collection mechanisms of these devices.

Charge-Collection Mechanisms of PD SOI MOSFETs

- Source: [94].

- PL SEE was used to investigate the quantitative differences in the charge-collection response between T-body and notched-body 45-nm PD SOI nFETs. **Figure 6.16** illustrates the use of PL SEE for probing charge collection mechanisms in highly-scaled devices.
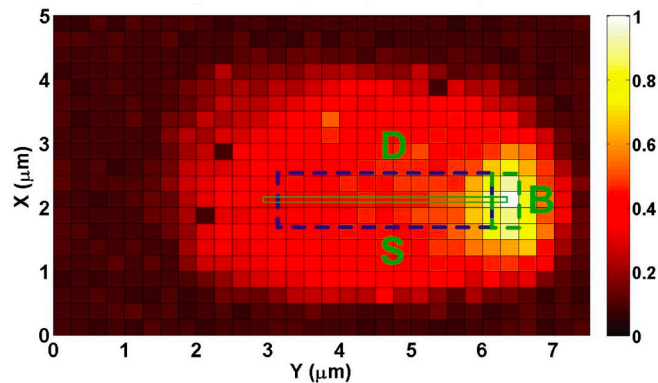

Figure 6.16. *Normalized peak currents for laser-induced transients as a function of laser position for a 45 nm T-body-contacted partially-depleted SOI nFET showing efficient charge collection adjacent to the body contact. After [94].*

- **Figure 6.16** shows a charge-collection map for a T-body nFET. This plot shows (normalized) peak body currents plotted as a function of the incident laser position. This plot illustrates that the location of maximum charge collection is associated with direct strikes into the body contact.

- Such measurements provide insight into the effectiveness of body contacts for suppressing charge collection.

Comparing the Sensitivity of Various Semiconductor Platforms

- Source: [95].

- PL SEE was used to investigate the quantitative differences in charge collection between silicon-germanium heterojunction bipolar transistors (SiGe HBTs) fabricated on bulk and SOI substrates, following a heavy-ion experiment. Ion data showed very different SET rates, despite the devices having identical design. PL SEE data confirmed that the sensitive region where SETs occur is different for both devices, as shown by **Figure 6.17**. This difference was attributed to the elimination of a collector-substrate junction.
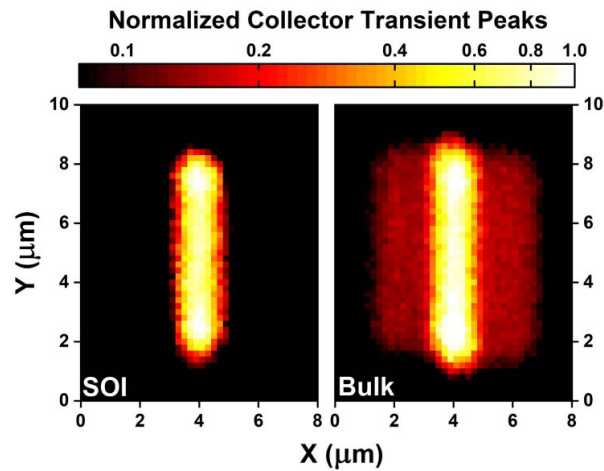
Figure 6.17. *Measured transient amplitudes as a function of laser focus position for SiGe HBTs fabricated on SOI (left) and bulk (right) substrates. The SiGe HBT fabricated on SOI has a smaller sensitive area compared to the one on bulk. After [95].*

- The fundamental finding was that, despite the removal of this additional junction, the worst-case peak amplitudes were identical, and PL SEE confirmed that the worst-case transient occurred in the same location for both devices. TCAD simulations revealed the reason for this amplitude was due to the high-doping level of the sub-collector region.

- This study highlights, yet again, how spatial selectivity can be used to compare the sensitivity of different platforms to charge deposition events.

6.7 SINGLE-EVENT BURNOUT (SEB)

6.7.1 General Definition

Single-event burnout (SEB) typically occurs in power devices (e.g., MOSFETs and diodes) when the charge produced by an energetic particle is separated by large electric fields and produces high currents that can lead to localized and destructive breakdown of the device. In power MOSFETs, SEB is attributed to the turn-on of a parasitic bipolar transistor in the device structure, while in power diodes it is attributed to avalanche multiplication. Due to its catastrophic nature, SEB is a significant concern for power devices operating in the space environment.

6.7.2 Specific Goals of PL SEE Testing
- Identify sensitive regions for SEB
- Determine safe-operating-area (SOA) of a device

6.7.3 General Experimental Procedure

Although SEB testing can be destructive, test circuits that allow for non-destructive characterization of SEB can be used in some cases. The procedures described below assume that these circuits are being utilized to minimize the number of samples required. An example of one of these circuits is shown in the case studies below.

To find SEB sensitive regions with experimental setup that allows for non-destructive SEB testing:

- Set pulse energy (or LET_L) at a low to moderate level and the device reverse biased at moderate to high level.

- Focus the beam into the active region and begin scanning the laser over the desired area.

- Record transient event corresponding to SEB and the position at which event was observed.

- Once scan is finished, repeat scan at larger pulse energy until LET_L is high enough for the given application.

To find SEB SOA:

- Set pulse energy (or LET_L) at a low level and the device reverse biased at high level.

- Position the laser spot in an SEB sensitive location (identified as above).

- Increase the pulse energy (or LET_L) until SEB is triggered and record the pulse energy (or LET_L) and device bias.

- Repeat for lower device bias until SEB is no longer triggered. The lowest bias that triggers SEB is the voltage SOA.

- Repeat procedure as necessary to validate result; repeat at various SEB sensitive regions.

- Note: If a test circuit that results in destructive SEB is used, a new device will be required for each bias step.

6.7.4   Data Acquisition and Equipment Considerations

- Typical PL SEE systems have a mechanism for scanning the beam relative to the surface of the part (*e.g.*, a programmable, motorized stage moving the sample or beam rastering).

- Software will need to monitor the devices and test circuits and have some sort of handshaking procedure to record the location of the SEB events during the scan.

6.7.5   Measurement Challenges

- Many power devices have metallization on both the top- and back-side of the die, which makes optical access more difficult (*i.e.*, would require additional processing).

- SEB can be destructive, which can result in a tedious experimental procedure when finding the appropriate X, Y, Z, laser pulse energy, and bias to trigger SEB. A non-destructive experimental setup is possible in some cases [96] and should be considered to enable testing of multiple conditions while minimizing the number of samples required.

6.7.6   Example Case Studies

Identifying SEB Sensitive Regions

- Source: [97, 98].

- By leveraging the localized nature of PL SEE Testing, the sensitive regions for SEB in a device can be determined. Due to the number of laser pulses incident on the device during this type of test, it is imperative that a test circuit that allows for non-destructive SEB characterization be used, similar to the one shown in **Figure 6.18**. With this test circuit, the transient voltage drop across

resistor R1 is measured and SEB triggering is identified once this voltage exceeds a certain threshold amplitude.
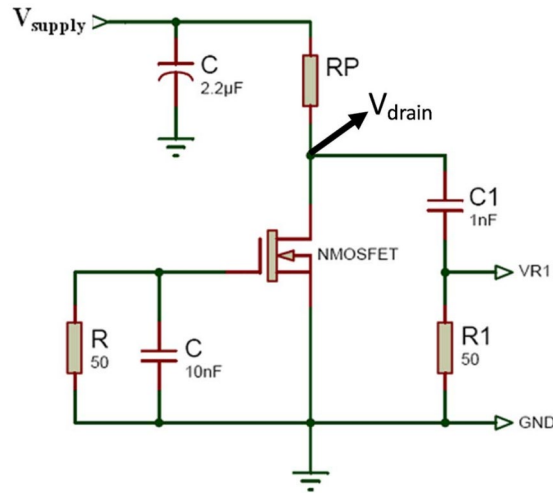

Figure 6.18. *Test circuit for non-destructive SEB measurements. After [98].*

- When using this circuit, the laser can then be scanned across the device to create sensitivity maps like the one shown in **Figure 6.19**. In this case, SEB is identified when the transient voltage across R1 exceeds approximately -3 V, as shown in the right panel.
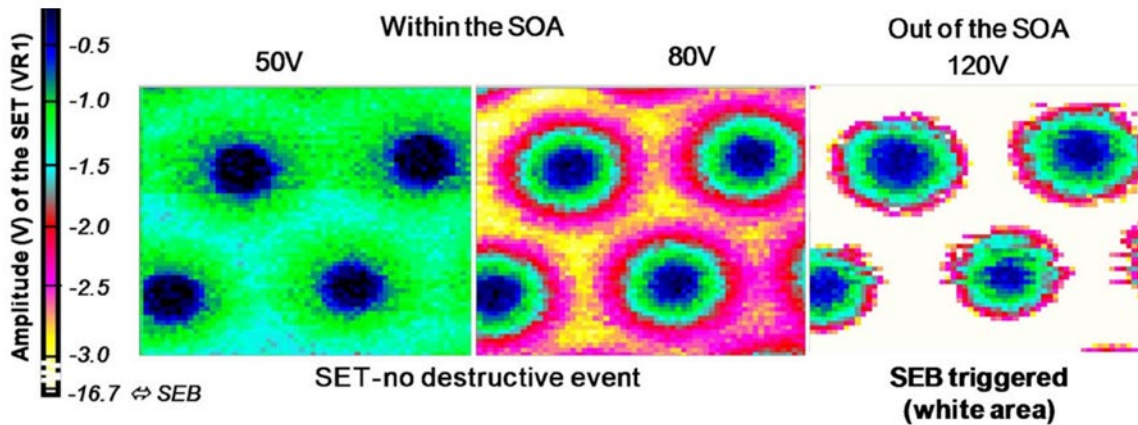
Figure 6.19. *Data resulting from scanning the laser across the device. Transient amplitudes at resistor R1 when the device is biased at (left) 50 V, (center) 80 V, and (right) 120 V. SEB is identified when these amplitudes exceed a certain threshold value. In this case, that threshold value is around -3 V, and those areas are shown in white in the right panel. After [98].*

- This approach can be extended to three dimensions when using TPA, due to the axial discrimination afforded by this technique. An example of a three-dimensional sensitivity map is shown in **Figure 6.20**.

Figure 6.20. *3-D sensitivity map of SEB in a power MOSFET (a). Cut plane of this volume for y = 10 μm (b). After [97].*

Determining SOA of Commercial Power MOSFETs

- Source: [99].

- As a rule of thumb, power devices are typically de-rated by 50% to avoid SEB. That is, they are operated at 50% of the maximum blocking voltage specified in the data sheet. A more accurate specification for SEB is given by the SOA, which is the range of bias voltages and LETs for which SEB cannot be triggered.
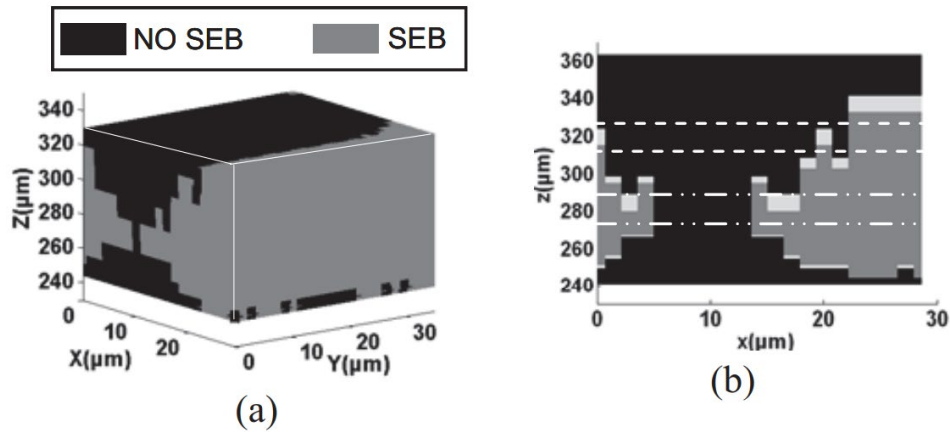
- Through-wafer PL SEE testing at a center wavelength of 1060 nm was used to determine the SOA of the IRFU420, a commercially available 500-V, N-channel MOSFET. The back contact was locally removed by mechanical etching to allow for optical access. A similar test circuit for non-destructive SEB measurements to that shown in **Figure 6.18** was utilized.
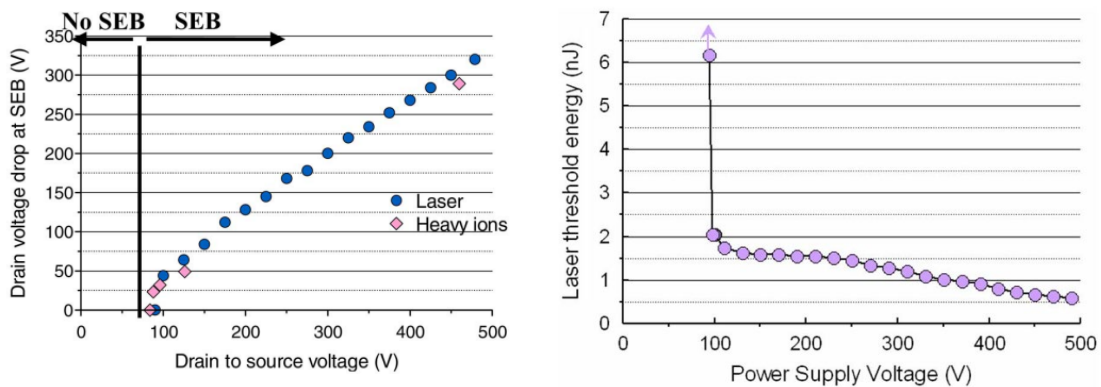
Figure 6.21. *Voltage amplitude at R1 in test circuit as a function of drain-to-source voltage (left). The SOA boundary is identified as the drain-to-source voltage when the voltage at R1 tends to zero, when testing with high laser pulse energies. Laser pulse energy required to trigger SEB as a function of drain-to-source voltage (labeled as "Power Supply Voltage") (right). The SOA boundary is identified as the drain-to-source voltage when the required pulse energy shows a drastic increase with asymptotic behavior. Both approaches show the same result. After [99].*

- In this study, the SOA is mainly characterized by the voltage drop across resistor R1 (see in **Figure 6.18**). When SEB is triggered, this voltage will be large. The SOA can then be determined by finding the minimum drain-to-source voltage that triggers SEB, as shown in **Figure 6.21** (left). Alternatively, the threshold laser energy to trigger SEB as a function of drain-to-source voltage can be examined, and the SOA will show as an asymptotic behavior, as shown in **Figure 6.21** (right). Both methods show the same voltage rating for SOA.

- PL SEE testing results, which were confirmed with heavy ion data, show that the SOA for this device is between 90 and 100 V, with an uncertainty of ±10 V. This result suggests that a more conservative de-rating of 80% is required to avoid SEB.

- This SOA measurement can be made at multiple locations in the device (following procedures similar to the ones previously discussed), resulting in a spatially defined SOA as shown in **Figure 6.22**. Note that, although visually similar, this measurement is fundamentally different than that shown in **Figure 6.20**. This type of measurement could yield useful insights to re-design devices and improve their SOA.
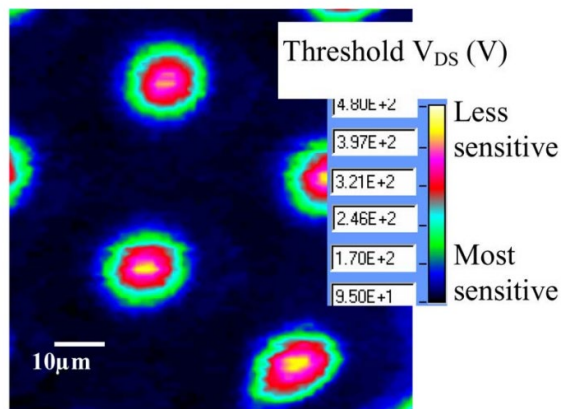
Figure 6.22. *Voltage SOA as a function of laser focus position. The areas with the lowest voltage (shown in black) represent the most sensitive regions of the device. After [99].*

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