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HIGH PERFORMANCE APPLICATION SPECIFIC INTEGRATED CIRCUITS (ASICS) BASED ON ADVANCED SiGe BiCMOS

Prof. Gabriel M. Rebeiz, Prof. Ian Galton, and Prof. Tzu-Chien Hsueh
University of California San Diego

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14. ABSTRACT
The goal of the UCSD T-MUSIC program was to develop state-of-the-art linear and mixed-signal circuits using advanced SiGe BiCMOS technologies developed at TowerJazz Semiconductor. Mixed-signal circuits designed as a result of this effort include a 30 GHz VCO/PLL, a 110-140 GHz divider and a high-dynamic range ADC. UCSD also designed *additional* circuits which are critical to DoD and can result in a jump-start to the defense industry. The circuits are 6-100 GHz LNAs and PAs (drivers) with low-noise and high linearity.

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SiGe BiCMOS, VCO, PLL, Frequency divider, Wideband, LNA, PA

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1 PROJECT SUMMARY

The goal of this program is to develop state-of-the-art linear and mixed-signal circuits using advanced SiGe BiCMOS technologies developed at TowerJazz. The proposed work is based on deep and fundamental circuit topologies coupled with accurate technology characterization, and can be broken into 3 parts:

1) UCSD will work with TowerJazz to characterize their processes using detailed measurements of test devices (transistors, ring oscillators, etc.) and passive circuits (transmission-lines, inductors, capacitors, deep well isolation structures, etc). Equivalent models will be derived for the advanced technologies and fed back to the foundries.

2) UCSD will design mixed-signal circuits as required by this program (VCO/PLL, divider and ADCs) and with a goal of meeting and exceeding the program metrics.

3) UCSD will design *additional* circuits which are critical to DoD and can result in a jump-start to the defense industry. The circuits are 6-100 GHz LNAs and PAs (drivers) with low-noise and high linearity, and 14-bit DACs at 12 GSps with 10x better in signal-to-noise-and- distortion-ratio (SNDR) than the current state-of-the-art.

2 SUMMARY OF THE WORK (PHASE 1)

A summary of the work in Phase 1 is shown below:

1) The 10-100 GHz LNA worked great with state-of-the-art performance, low noise figure and high gain. This was done in SiGe SBCS5. See Section 3 for details.

2) The 10-110 GHz PA great with state-of-the-art performance, low noise figure, and high gain and 12 dBm peak power achieved at40-60 GHz. This was done in SiGe SBCS5. See Section 4 for details.

3) The 110-140 GHz divider worked great and achieved a clean division ratio up to 145 GHz. This was done in SiGe SBCS5. It achieved nearly Phase II specs. See Section 5 for details.

4) The 30 GHz VCO worked great with -110 dBc/Hz at 1 MHz and achieved nearly Phase II specs. See Section 6 for details.

5) We did not have time to complete the PLL in Phase 1. However, it was completed later in 2022 and achieved all the specs of Phase 1 with < -100 dBc at 1 MHz and 99fs integrated noise. See Section 6 for details.

6) The T-Semi transistors worked great with measured ft/fmax of ~500GHz/350GHz. This was without the thick oxide and IDL excellent results.

7) The T-Semi tapeout with thick oxide <u>did not work</u> and we had continuity issues. We could not measure transistors, inductors, capacitors and cavities in this process.

8) The ADC design was completed, and the ADC's total power consumption was predicted to be 90 Watts (had we not solved the jitter issue, it would have been higher by a factor of at least 5). This required that the ADC be split into 20 chips connected at the circuit board level and sorting out the details of this took more time than expected. We finished laying out most of the blocks but were not able to finish the complete layout and digital place- and-route by the end of the quarter. See Section 7 for details.

Students:

1) Oguz Kazan graduated in June 2022. He subsequently joined Qualcomm.
2) Zhaoxin Hu is still at UCSD and will graduate in Jan 2023.
3) Mohammed Badr left UCSD with an MS and joined Illinois Urbana Champaign.
4) Nick Ma graduated with an MS and joined Astranis.

Publications:

1) O. Kazan and G. M. Rebeiz, "A 10–110 GHz LNA with 19-25.5 dB Gain and 4.8-5.3 dB NF for Ultra-Wideband Applications in 90nm SiGe HBT Technology," *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Atlanta, GA, USA, 2021, pp. 39-42, doi: 10.1109/RFIC51843.2021.9490504.

2) O. Kazan and G. M. Rebeiz, "A 10-130 GHz Distributed Power Amplifier Achieving 2.6 THz GBW with Peak 13.1 dBm Output P1dB for Ultra-Wideband Applications in 90nm SiGe HBT Technology," *2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, Monterey, CA, USA, 2021, pp. 1-4, doi: 10.1109/BCICTS50416.2021.9682475.

3) Zhaoxin Hu, Tzu-Chien Hsueh and G. M. Rebeiz, " A Low-Power 130-GHz Tuned Frequency Divider in 90-nm SiGe BiCMOS," *to appear in IEEE MICROWAVE AND WIRELESS COMPONENT LETTERS*.

4) Zhaoxin Hu, Eric Wagner, Tzu-Chien Hsueh and G. M. Rebeiz, " A 28-GHz Low Phase Noise Class-C Transformer VCO with 187-dBc/Hz FoM in 90-nm SiGe BiCMOS," to appear in *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES*.

3 ULTRA-WIDEBAND LNA

3.1 A 10-110 GHz LNA with 19-25.5 dB Gain and 4.8-5.3 dB NF for Ultra-Wideband Applications in 90nm SiGe HBT Technology

Oguz Kazan and Gabriel M. Rebeiz
University of California, San Diego, La Jolla, CA, USA okazan@ucsd.edu, grebeiz@ucsd.edu

Abstract—**This paper presents a broadband differential low noise amplifier (LNA) at 10-110 GHz. The four-stage LNA is realized using 90 nm SiGe BiCMOS process having a 300 GHz f_T HBT. Resistive feedback is used for operation at 10-50 GHz, and a wideband collector load with a linear impedance increase versus frequency compensates for the transistor output capacitance and guarantees a monotonic increase in the gain from 60 to 100 GHz. The LNA has a measured small-signal gain of 19-25.5 dB and the measured noise figure (NF) is 4.8-5.3 dB at 10-50 GHz. The LNA also achieves an output-referred 1dB compression point (OP1dB) of -3.3 dBm at 66 GHz. The differential LNA consumes 96 mW (48 mW half circuit) with an active circuit area of 1.3x0.6 mm². Application areas are in wideband receivers and in wideband microwave and millimeter-wave instrumentation systems.**

Keywords— **broadband amplifiers, low-noise amplifiers, microwave integrated circuits, noise figure, wideband.**

3.1.1 Introduction

Due to the ever-increasing 5G frequencies, starting from 24 GHz extending to 52 GHz, and with possible extensions down to the 10 GHz range and up to 94 GHz range, it is important to develop wideband receivers and instrumentation capable of developing covering the entire 10-110 GHz range. Previously, distributed amplifiers (DA) have been shown to cover such a range (DC-105 GHz, etc.) but were designed mostly for wireline applications and with relatively high-power consumption [1-5]. Also, distributed amplifiers normally occupy a large area which is not suitable for wideband phased arrays.

In this paper, an ultra-wideband LNA at 10-110 GHz is demonstrated. The circuit is composed of 4 differential common-emitter amplifier stages, and the wide bandwidth is achieved using a multi-stage wideband load and resistive shunt feedback. The amplifier area is very small and results in state-of-the-art performance.

3.1.2 Technology

The wideband LNA is implemented in the Tower Semiconductor 90 nm SiGe BiCMOS platform with aluminum backend and a 7-metal stack. For most of the inductors, the top layer is used, and a ground plane is placed at M1/M2 to increase the inductor Q. All the inductors and metal capacitors are modelled using Integrand Software, EMX.

Fig. 3.2 presents a transistor layout and simulations in the Tower Semiconductor SBC18S5 technology for the common-emitter and cascode configurations with 4 μm emitter length. The common-emitter transistor has an NFmin of 2.1 dB at 0.21 mA/μm (60 GHz). However, if the transistors are connected in a cascode configuration, the achievable NFmin becomes 2.7 dB at 0.56 mA/μm (60 GHz). However, in this design, the first stage is biased at 1.5 mA/μm with an NFmin penalty of 0.3 dB to increase the first-stage gain by 2

dB and to lower the noise contribution of the subsequent stages. The second, third and fourth stages are biased at 0.56 mA/ μm for lowest NF and to conserve DC power.
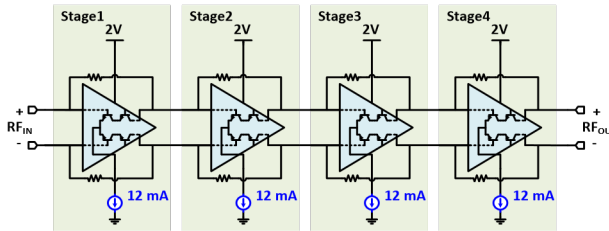
Fig. 3.1. Schematic of the 4-stage Wideband LNA

(a)   (b)
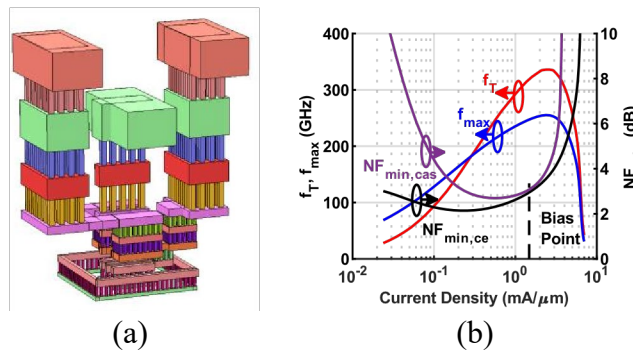
Fig. 3.2. (a) Physical Layout of a Transistor, (b) 4µm Transistor Performance
Black, red, and blue curves show single transistor performance. Purple curve shows two cascode connector transistors performance. NFmin results are for 60 GHz operation.

3.1.3   DESIGN

The proposed wideband LNA is shown in Fig 1. It is composed of 4 cascode differential stages to achieve the desired gain and noise figure (NF) at 10-110 GHz and to match well with a wideband differential antenna. For the tail current sources, HBT devices are used due to their lower parasitics compared to the 0.18um CMOS devices available in this technology, to improve the common-mode rejection. The current-source device size is chosen as a compromise between the transistor parasitics and the voltage headroom. The common mode rejection is further improved by tying the bases of the cascode devices.

(a)   (b)
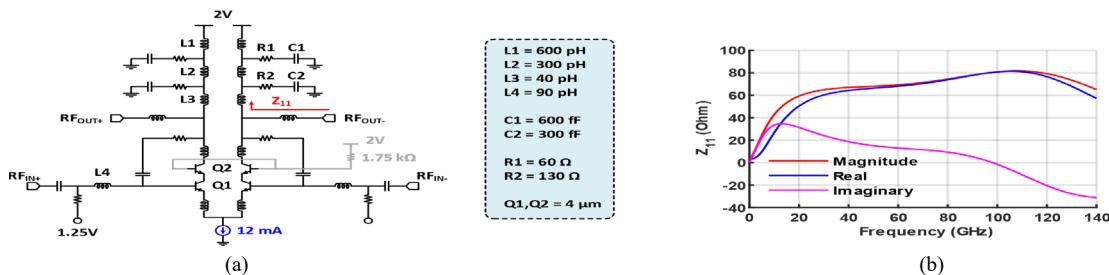
Fig. 3.3. (a) First Stage of the Wideband LNA (other stages are similar but with different L and C values), (b) Simulated Impedance of the FIRST Stage Load

A large amplifier bandwidth is generally achieved using light resistive feedback and inductive loads with wideband impedance characteristics. One of the essential problems in wideband amplifier design is that

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the load inductor which is chosen to operate well at the lower frequency range, will resonate at the higher band resulting in a severe drop in amplifier gain. If the inductor is chosen for operation at high frequencies, then the amplifier gain is low at the lower frequency band. One solution is high resistive feedback, but this greatly lowers the gain per stage and increases the total amplifier power. Another solution is using a resistor in series with a high value inductor, (commonly called a low-Q load), but this results in low voltage headroom, and does not compensate for the transistor capacitance as the frequency increasing resulting again in a gradual gain drop as the frequency increases. The final solution is of course, the distributed amplifier design technique which is excellent but consumes a lot of power.

This work introduces an innovative multi-stage load composed of L1/L2/L3 and C1R1/C2R2 with the specific purpose of generating an increasing load impedance versus frequency without going into resonance (Fig. 3.3a). At the lower frequency range, C1 and C2 are nearly open circuited and the load is composed of L1+L2+L3. At mid-frequencies, the load is composed of L3+L2, and the resonance in L1 is dampened by R1. At the highest frequencies, the load is composed mostly of L3 and the resonance in L2 is dampened by R2. The multistage load occupies a small area and has an effective impedance which increases from 40 Ω at 10 GHz to 80 Ω at 100-110 GHz while still being inductive over the entire frequency range. The load also has a near-zero impedance at DC to reduce the power consumption. The load network is simulated with EMX.

Fig. 3.4 presents the simulated gain and NF of every stage in the 4-stage LNA. The values are in power gain assuming a load of 100 Ω, but the final gain is higher than the added block gain (in dB) due to the inductive match at each base. At the midband frequency of 50 GHz, the first stage has a gain of 6.5 dB and a NF of 5.1 dB, with all other stages having a gain of 4-4.8 dB. The gain is nearly equally distributed for near-optimal P1dB performance, and to result in wideband performance for all four stages, and thus for the entire LNA.
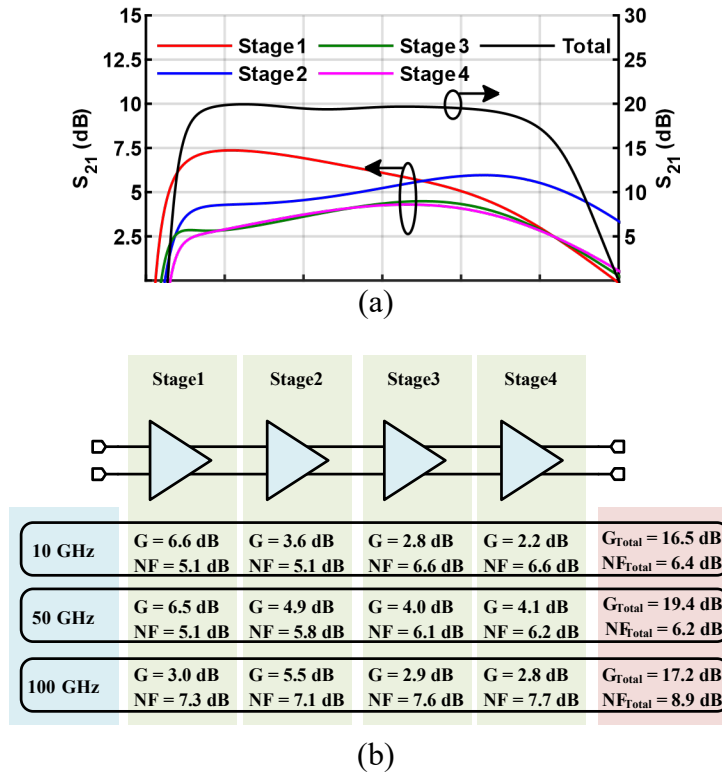
Fig. 3.4. (a) Gain Response of Individual Stages, (b) Simulated Gain and Noise Figure at 10, 50 and 100 GHz

3.1.4   Measurements

The LNA die photo is shown in Fig. 3.5, with chip dimensions of 1.5x1.0 mm^2, including the pads, and 1.3x0.6 mm^2, excluding the pads. To our knowledge, this is the smallest 10-110 GHz LNA reported and is much smaller than distributed amplifier designs. The amplifier employs a GSSG input and output pads and all measurements are calibrated to these ports.

For gain measurements, a GSSG probe was used up to 40 GHz. Also, LNAs with Marchand baluns at their input and output ports were also placed on the tape-out and covering the frequencies of 10-30 GHz, 20-50 GHz, 45-100 GHz, and these circuits are for measurement purposes. The Marchand baluns result in an LNA with GSG ports and allow for NF measurements to be possible up to 100 GHz. One of the LNAs with Marchand baluns is depicted in Fig. 3.5(b). Back-to-back baluns are also placed on the tape-out for de-embedding.

Small-signal S-parameters and linearity performances are evaluated up to 70 GHz, and NF is evaluated up to 50 GHz using a Keysight N5247A PNA-X Network Analyzer. This setup is used for both single-ended 2-port measurements and differential 4-port measurements. Small-signal S-parameters between 70-110 GHz are obtained using a setup containing a Keysight E8364B PNA Network Analyzer, a Keysight N5260A Millimeter Head Controller, and Virginia Diodes WR-10 75-110 GHz extenders.

Fig. 3.6(a) presents the small-signal performance. S_{21} is 18-19 dB at 20-30 GHz and increases to 25.5 dB at ~97 GHz, which is desirable for our purposes as the blocks connected at the output of the LNA have

higher loss and need a bit of additional gain (mixers, phase shifters, etc.). The gain is higher than simulated at 70-100 GHz and is most probably due to the wideband network having an even higher impedance. The LNA has a reverse isolation (S_{12}) < -40 dB at 70-110 GHz.

The measured noise figure is shown in Fig. 3.6(b). The NF is obtained by de-embedding the input and output balun losses, and is 4.8-5.5 dB up to 50 GHz, with a mean of 5.3 dB. NF measurements at higher frequencies are not performed due to the unavailability of the noise source for 60-90 GHz. It is seen that the measured NF is close/lower than simulations and this is due to the use of early models in this technology (seen on different circuits). The measured OP1dB performance is -9 dBm to -4 dBm at 10-60 GHz and agrees well with simulations (Fig. 3.6c). The measured OIP3 is ~9 dB higher than the OP1dB and agrees with simulations (Fig. 3.6d).
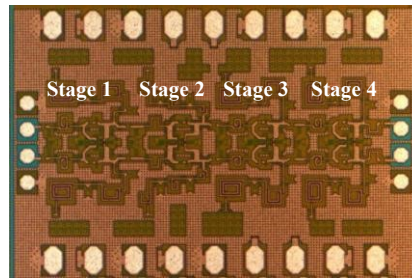
(a)
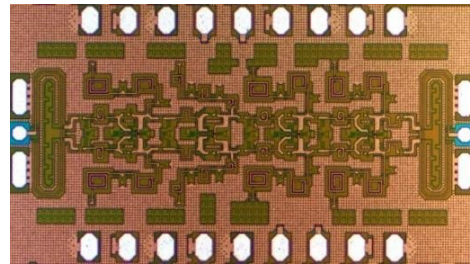
(b)

Fig. 3.5. (a) Die Photo of the Wideband Differential LNA, the Size is 1.5x1.0 mm^2 Including the Pads, and 1.3x0.6 mm^2 Excluding the Pads, (b) Die Photo of the LNA with Input and Output March and Baluns for Operation at 45-100 GHz

The wideband LNA is compared to the state-of-the-art in Table 1, and the figure-of-merit (FoM) is given by [9]:

$$FoM = 20log_{10}\left(\frac{Gain[lin\,]\times BW[GHz]}{P_{DC}[mW]\times(NF[lin]-1)}\right) \tag{1}$$

State-of-the-art-gain, bandwidth, power consumption and NF has been achieved, resulting in a large FoM.
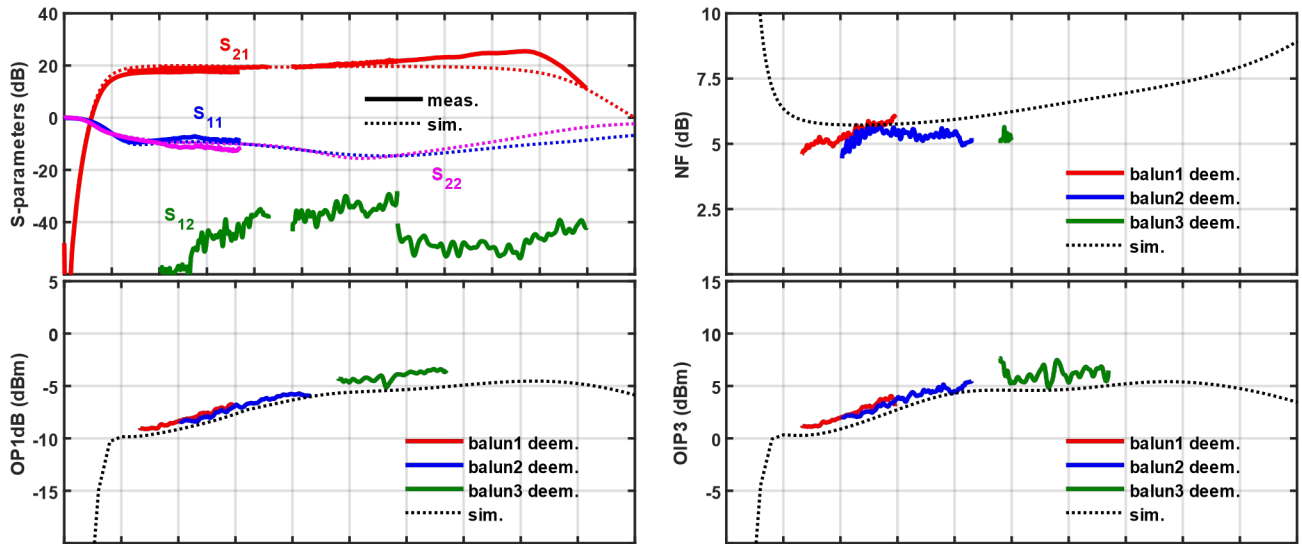
Fig. 3.6. Measured and Simulated: (a) S-parameters; (b) Noise Figure; (c) OP1dB, and (d) OIP3

Table 3.1. Comparison with State-of-the-Art Wideband Amplifiers

Reference	Technology	Topology	Frequency (GHz)	Gain (dB)	NF (dB)	P_{DC} (mW)	Area (mm²)	FoM
[5] ISIC 2016	130-nm SiGe BiCMOS	DA with Stacked HBTs	10-170	19	N.R.	560	0.91	-
[6] TMTT 2015	28-nm CMOS	2 Stage Cascode	54.5-72.5	13.8	4	24	0.38	7.7
[7] JSSC 2017	65-nm CMOS	3 Stage Cascode	62.5-92.5	18.5	5.5	27	0.24	11.3
[8] MWCL 2016	65-nm CMOS	5 Stage Cascode	88.5-110	16.7	7.2	48.6	0.29	-2.9
[9] APMC 2015	65-nm CMOS	6 Stage Cascode	73.5-93.5	22	6.8	21	0.45	10
[10] TMTT 2020	22-nm CMOS FD-SOI	3 Stage Cascode	70-100	18.2	5.8	16	0.43	15
This work	90-nm SiGe BiCMOS	4 Differential Stage Cascode	10-110	19-25.5	4.8-5.3	48*	0.78&	22.7

N.R. = Not Reported   *Single-ended half-circuit   &Differential circuit area

3.1.5   Conclusion

A 10-110 GHz LNA is presented in this paper. The circuit employs a wideband multi-stage L/C/R load and resistive shunt feedback to achieve an ultra-large bandwidth. The measurements indicate that the LNA exhibits high performance and is unconditionally stable. The proposed LNA is a very good candidate for ultra-wideband applications.

3.1.6   ACKNOWLEDGEMENT

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3.1.7 REFERENCES

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4 ULTRA-WIDEBAND DISTRIBUTED POWER AMPLIFIER

4.1 A 10-130 GHz Distributed Power Amplifier Achieving 2.6 THz GBW with Peak 12.2 dBm Output P1dB for Ultra-Wideband Applications in 90nm SiGe HBT Technology

Oguz Kazan and Gabriel M. Rebeiz

University of California, San Diego, La Jolla, CA, USA okazan@ucsd.edu, grebeiz@ucsd.edu

Abstract—This paper presents a 10-130 GHz ultra-wideband distributed power amplifier (DPA) with 2.6 THz gain-bandwidth product (GBW). The DPA is composed of 3 stages each with multiple cascode amplifier sections. The circuit is realized using 90 nm SiGe BiCMOS process having a 255 GHz f_T HBT. The amplifier achieves small-signal gain of 18-23 dB at 10-30 GHz and monotonically increasing to the peak of 33 dB at 98 GHz. The return losses are better than 10 dB covering more than 140 GHz. The circuit has a peak OP1dB of 12.2 dBm at 26 GHz. To the best of authors' knowledge, the proposed amplifier achieves the largest GBW in SiGe DPAs while providing relatively high power.

Keywords— 5G, broadband amplifiers, distributed amplifiers, microwave integrated circuits, power amplifiers, SiGe BiCMOS, wideband.

4.1.1 Introduction

Broadband distributed power amplifiers (DPAs) can process ultra-narrow pulses, which makes them attractive for wireline communication links, high-frequency instrumentation, and high-resolution imaging. In literature, there several DPAs implemented in SiGe BiCMOS, CMOS SOI and InP HBT. The DPAs reported in SiGe technologies either have low gain and high output power [1][2] or are wideband and with low output power [3]. Also, state-of-the-art SiGe DPAs have a gain bandwidth product (GBW) of ~ 1.6 THz [1-7].

In this work, an ultrawideband 10-130 GHz DPA in 90nm SiGe HBT technology is demonstrated. The circuit is composed of three cascaded distributed amplifier stages, each having 5, 6 and 16 gain sections. The amplifier has ultra-wideband characteristics while providing high power. To the best of authors' knowledge, the proposed DPA has the largest GBW of 2.6 THz among other SiGe distributed amplifiers.

4.1.2 Technology

The wideband DPA is implemented using Tower Semiconductor 90 nm SiGe BiCMOS platform (SBC18S5L). The process has HBTs having a peak f_T of 255 GHz. The backend is composed of an all-aluminum seven metal layer stack with metal-insulator-metal (MiM) capacitors and TiN resistors. Inductors employ the top M7 layer, and for the ground, merged M1/M2 layers are used to increase the inductor Q. All the inductors, capacitors and HBT interconnects are modelled using Integrand Software, EMX.
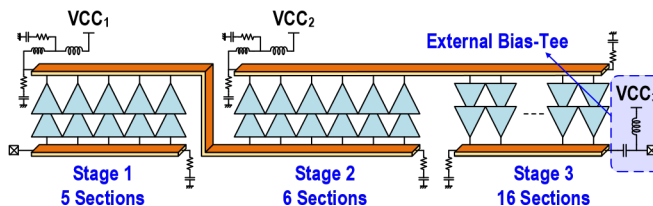
Fig. 4.1. A 3-stage Wideband Distributed Power Amplifier using 90nm SiGe

4.1.3 Design

In conventional power amplifiers, high output power is obtained by using large transistors and high supply voltages to create large voltage and current swings governed by the transistor maximum I-V relationship. In distributed power amplifiers, however, the transistors are distributed between the input and output ports, and the number sections are chosen according to the input transmission line losses. As the wave travels through the input transmission line, it will be reduced due to the transmission-line loss, and the section gain will not be sufficient to contribute to the output power. This sets the upper limit on the number of sections which are used.

To provide high power, a 16-section DPA stage is used at the output, considering the input transmission line loss of that stage (Fig. 4.1), and the supply voltage of 2.8 V is fed from the RF output port using an external bias-tee.

The first and second stages are used as a driver amplifier to increase the small-signal gain while consuming a low amount of DC power. Each stage can deliver sufficient power to drive its succeeding stage so that the ultimate overall OP1dB is not deteriorated. Since the output power which is delivered from the first and the second stage are much lower than the output stage, a lower supply voltage of 1.8 V and 2.0 V are used, respectively, to reduce the overall power consumption. These supply voltages are delivered using a two-section DC feed as shown in Fig. 4.2. The DC feed structures provide a very low DC resistance to conserve power consumption. They also provide a wideband impedance of ~35 Ω up to 90 GHz.
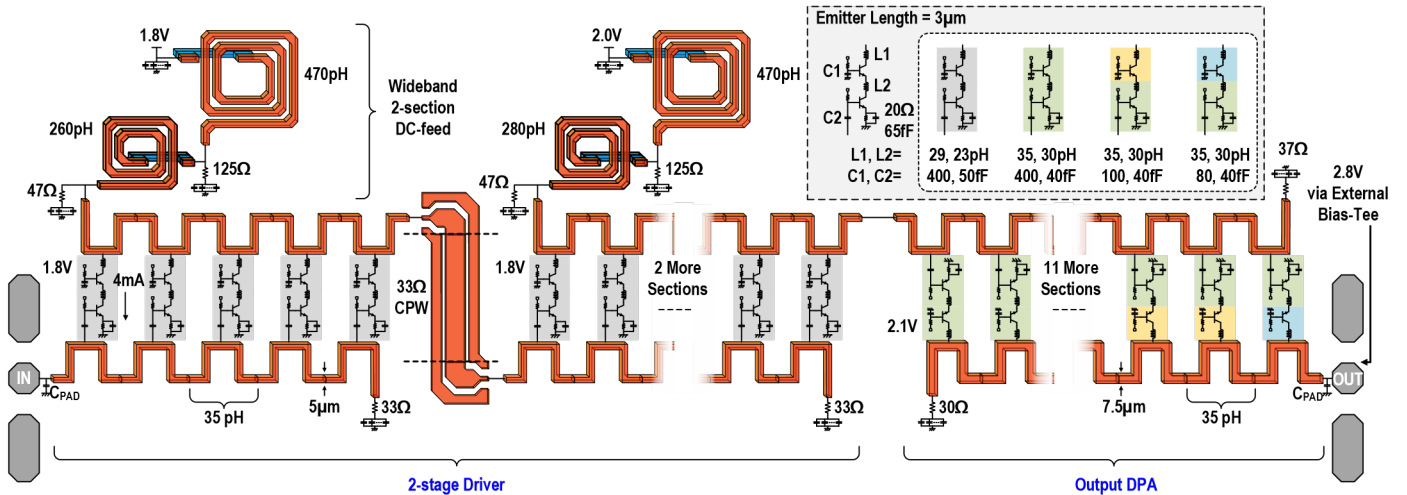
Fig. 4.2. Schematic of the Wideband 3-stage DPA

In distributed amplifiers, the maximum achievable bandwidth is dictated by the cutoff frequency of the artificial transmission lines (ATLs) which is expressed as:

$$f_c = \frac{1}{\pi\sqrt{L\cdot(C+C_{par})}}$$

(1)

where L and C are the inductance and capacitance of the ATL and C_{par} is parasitic capacitance induced by the transistor sections. To increase the cut-off frequency, the capacitive load introduced by the ATL inductors themselves must also be minimized. In the design, most of the ATL employ narrow 5 μm width inductors having sufficient margin for electro migration rules and providing low additional capacitance.

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However, for the output ATL for stage 3, 7.5 µm-width inductors are used due to the higher current. Also, to reduce the HBT capacitive loading, small 3µm emitter length devices are used throughout the design for wide bandwidths.

The ATL characteristic impedance is chosen considering the power delivered by the sections and the input and output return losses. The characteristic impedance is determined by:

$$Z_O = \sqrt{\frac{L}{C+C_{par}}} \tag{2}$$

With L=35pH and $C+C_{par}$=25fF, a Z_0 and f_c of ~37 Ω and 340 GHz are obtained.

Since the single HBT devices have a finite C_{bc} capacitance, the stage sections employ cascode topology to improve the isolation between the input and the output ATLs. The ATL loss are compensated by adding inductors, L1/L2, at the collectors of the cascode HBTs [8]. To reduce the loading effect of the base-emitter capacitances, 40-50 fF series capacitors (C2) are also added between the HBT bases and the ATL. Also, RC (20 Ω and 65 fF) emitter degeneration networks are used to reduce the resistive and capacitive loading, and they also work as a peaking network to further enhance the bandwidth.

Fig. 4.3 presents the DPA with chip dimensions of 2.4x1.0 mm^2 including the pads. The active circuit size is 2.11x0.59 mm^2. The amplifier employs a GSG input and output pads, and all measurements are calibrated to the probe tips.
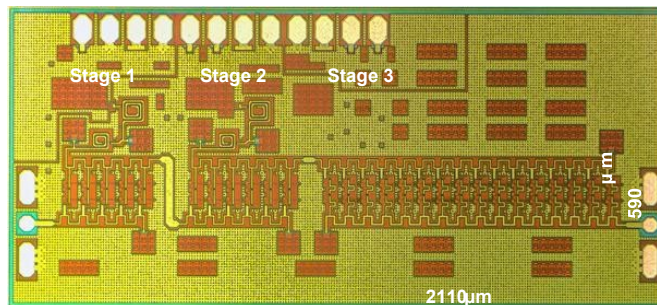
Fig. 4.3. Die Photo of the Wideband DPA

4.1.4 Measurements

Small-signal and power measurements are performed using a Keysight N5247A PNA-X Network Analyzer. With this setup, the DPA performance up to 70 GHz is evaluated. Small-signal performance for 70-110 GHz is evaluated using a setup containing a Keysight E8364B PNA Network Analyzer, a Keysight N5260A Millimeter Head Controller, and Virginia Diodes WR-10 75-110 GHz extenders. For frequencies higher than 110 GHz, OML WR-6 frequency extenders are used.

The measured S_{21} is 18-23 dB at 10-30 GHz and monotonically increases to a peak of 33 dB at 93 GHz. The circuit has average gain of ~27 dB between 10-130 GHz. Considering the average gain, the circuit has the largest GBW (2.6 THz) compared to the other state-of-the-art SiGe DPAs. The return losses are better than ~10 dB up to frequencies higher than 140 GHz. Also, the reverse isolation is greater than the gain of the amplifier, ensuring the unconditionally stable operation. Measurements of k (>1) and mu (not shown) confirm unconditional stability at all frequencies, even at 90-110 GHz in the region of peak gain.
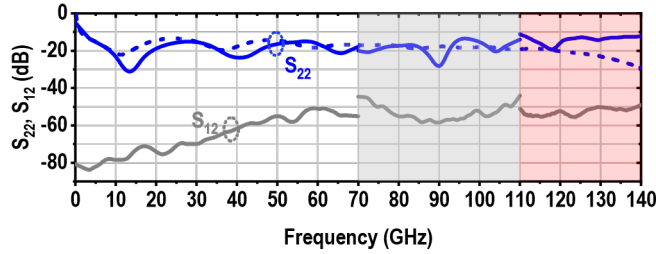
Fig. 4.4. S-parameter Performance of the DPA

There is a discrepancy between the simulated and measured results at frequencies higher than 60 GHz. This is due to the improper modelling of the inductors inside the gain section, causing peaking at high frequencies. The peaking might also be caused by the RC network used for the emitter degeneration. We are currently investigating this with additional electromagnetic analysis to take into accounts multiple sections and multiple couplings between inductors.

The large-signal performance is shown in Fig. 4.5. The circuit achieves a an OP1dB of 11.5-12.2 dBm at 17-67 GHz. As a sanity check for the measured OP1dB, the OIP3 is also measured, and it is around 10 dB higher. Both agree well with simulations.

The performance of the DPA is compared to the other state-of-the-art SiGe DPAs in Table 4.1. There are still some measurements remaining which should be performed to fully characterize the proposed DPA such as high frequency OP1dB (>70 GHz), saturated output power, power added efficiency and error-vector magnitude. We are planning to complete these in the near future.

4.1.5 Conclusion

A 10-130 GHz DPA is presented. To enhance the bandwidth, peaking inductors and parallel RC degeneration are used on every stage. Measurements indicate that the DPA exhibits the largest GBW product compared to the state-of-the-art SiGe DPAs, while delivering a relatively high power.
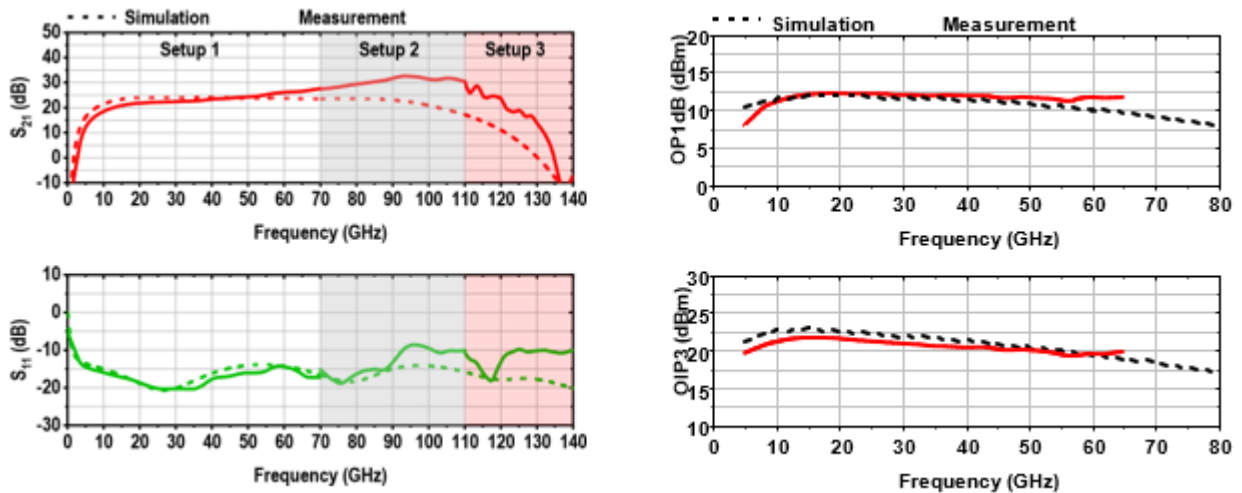
Fig. 4.5. Large Signal Performance of the DPA

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Table 4.1. Comparison with State-of-the-art SiGe BiCMOS DPAs

Ref.	Process	Gain (dB)	BW (GHz)	GBW (GHz)	Peak OP1dB (dBm)
[1]	90nm SiGe	12	91	362	14.9
[2]	130nm SiGe	10	110	348	16.7
[3]	130nm SiGe	10	170	537	8.2*
[4]	130nm SiGe	24	95	1500	N.R.
[5]	130nm SiGe	19	160	1515	N.R.
[6]	130nm SiGe	13	170	759	N.R.
[7]	130nm SiGe	18.7	180	1550	N.R.
This work	**90nm SiGe**	**27**	**120**	**2577**	**12.2**

* Estimated from plots   N.R. Not reported

4.1.6   Acknowledgment

4.1.7   References

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5 FREQUENCY DIVIDER

5.1 A Low-Power 130-GHz Tuned Frequency Divider in 90-nm SiGe BiCMOS

Zhaoxin Hu, *Graduate Student Member, IEEE,* Tzu-Chien Hsueh, *Senior Member, IEEE,* and Gabriel M. Rebeiz, *Fellow, IEEE*

Abstract—This letter presents a flip-flop-based tuned frequency divider in a 90-nm SiGe BiCMOS process. The operating bandwidth is 120–140 GHz with a self-oscillation frequency of 130 GHz. The input sensitivity at 130 GHz is -25 dBm and remains less than -4 dBm at 120–134 GHz. The chip consumes 45.1 mW from a 2 V supply, with a core power consumption of 36 mW. Potential applications include frequency synthesis in the 120–140 GHz band.

Index Terms—Frequency divider, heterojunction bipolar transistor (HBT), phase noise, SiGe BiCMOS.

5.1.1 INTRODUCTION

Frequency dividers play a key role in synthesizers and in I/Q LO generation for direct-conversion and single-sideband transceivers. To push the operating frequency above 100 GHz, static dividers can employ two emitter-follower (EF) stages and a maximum operating frequency of 128.7 GHz is achieved [1]. However, power consumption is doubled if the transistors in the EF stages have identical bias currents as the tracking and latching differential pairs. Another solution uses current-mode logic dividers with asymmetric latches, resulting in a maximum operating frequency of 113 GHz [2]. However, additional tuning circuitry is required to steer the bias current away from the tracking pair, a disadvantage in terms of design complexity.

In this letter, a tuned frequency divider with inductive peaking is presented for high-frequency, low-power, and low design complexity. Open-loop and closed-loop analyses are performed considering the similarities between the divider and two-stage ring oscillators. The required silicon area for a peaking inductor is only 40×50 μm^2 at 130 GHz and does not increase the chip area significantly. The divider is designed in a 90-nm SiGe BiCMOS process. A state-of-the-art performance is demonstrated with a proper choice of biasing, sizing, and careful layout considerations.

5.1.2 TECHNOLOGY

The divider is designed in TowerSemi's 5th generation SiGe BiCMOS process which features 90-nm wide heterojunction bipolar transistors (HBTs) and 7 metal layers. The reported peak f_t is 285 GHz and peak f_{max} is 310 GHz [3]. The inductors on the top two thick metal layers have Q-factors of 18 at 130 GHz, which makes this technology ideal for >100 GHz systems.
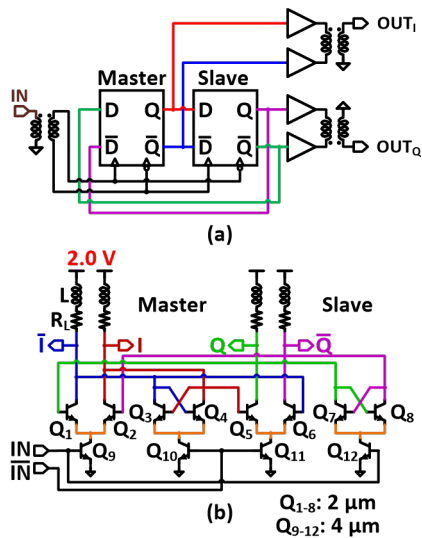
Fig. 5.1. Divider (a) Block Diagram and (b) Schematic
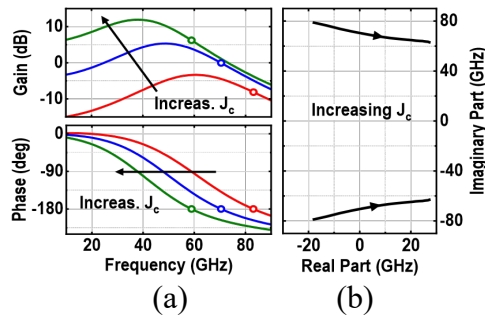
Fig. 5.2. (a) Simulated Open-loop Gain and Phase Responses and (b) Root Locus of the Closed-loop Poles for J_c = 0.4–2 mA/µm

5.1.3 Design

The divider block diagram and schematic are shown in Fig. 5.1(a) and Fig. 5.1(b) and is the same topology as a conventional static divider. A tuned divider can oscillate by itself without any input power, similar to a two-stage ring oscillator. For oscillation to start up, the small-signal equivalent circuit must have (i) open-loop gain exceeding unity, and (ii) a total of 180° phase delay provided by the two stages, at the frequency of oscillation ($0.5f_{osc}$ when referred to the input). Alternatively, the closed-loop system must have poles on the right half-plane (RHP).
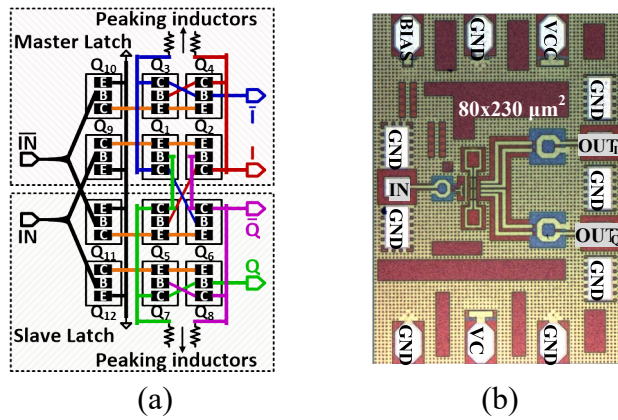
Fig. 5.3. (a) Layout of the D-FF (80×70 μm²) without Peaking Inductors, (b) Chip Micrograph with Input and Output Baluns

The chip size is 690×970 μm²

The simulated open-loop gain and phase responses are plotted in Fig. 5.2(a) for three increasing current densities (J_c[1]). When J_c increases, the gain response curve shifts up as g_m increases. C_{be} also increases and introduces more phase delay, shifting the phase response curve leftward. The -180° crossing points and the corresponding gains are marked with circles. Note that oscillation cannot start for small J_c (~0.4 mA/μm), since the gain is smaller than unity. Oscillation is sustained as the gain becomes larger than unity (at $J_c \approx$ 0.8 mA/um), but f_{osc} decreases for larger J_c.

A similar trend is observed in the closed-loop system. The root locus plot of the complex pole pair is shown in Fig. 5.2(b). As J_c increases beyond ~0.8 mA/μm, the poles move to the right half-plane and self-oscillation starts. The imaginary part of the poles becomes smaller in magnitude as J_c further increases, indicating a smaller f_{osc}. These observations explain the downward trend of f_{osc} versus J_c. The HBTs in this design are biased near J_c = 1.1 mA/μm, small enough for a relatively large f_{osc}.

In static dividers, the load resistor and the bias current must be large enough for a large swing and complete current steering. For tuned dividers, a small load resistor (R_L) and a properly-sized peaking inductor (L) are preferred to increase f_{osc}, though the divider may lose static operation [4]. For $f_{osc} \approx$ 130 GHz, R_L and L are chosen to be 12 Ω and 35 pH, respectively. The transistor sizes are also small to reduce capacitive loading, with tracking ($Q_{1,2}$ and $Q_{5,6}$) and latching ($Q_{3,4}$ and $Q_{7,8}$) pair sizes of 2 μm × 90 nm, and tail-current HBT (Q_{9-12}) sizes of 4 μm × 90 nm.

Each of the four nodes (I, ¯I, Q, and Q) is connected to two ¯base and collector terminals in the D flip-flop (D-FF) and an output buffer. To minimize the routing capacitance, the metal connections should be as short as possible with few crossovers between them. These requirements lead to the layout shown in Fig. 5.3(a). The master latch is placed at the top side and the slave is at the bottom side. The input signal is fed from the left side and the buffers are placed on the right for minimal connection lengths. The tracking and latching pairs with their respective tail-current HBTs are placed in the same row to reduce parasitic resistance and inductance in the tail node. In the right two columns, the HBTs with collectors on the same output node are placed in a column. These layout choices lead to a simple routing with short interconnect lengths and low parasitics.

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[1] $J_c = I_c/L_e$, where J_c is the current density, I_c is the collector current, and L_e is the emitter length

The chip micrograph is shown in Fig. 5.3(b). Q_{9-12} are biased by current mirrors which is controlled externally through the bias pad (top left). The 40 × 50 μm² single-turn peaking inductors have a self-resonant frequency of 386 GHz and a Q-factor of 17.5 at 130 GHz. On-chip baluns with ~2 dB insertion loss are included to facilitate single-ended probe measurements, and the return loss is ~10 dB near 130 GHz and 65 GHz. The core size is 80 × 230 μm² including the peaking inductors. The chip operates under a 2 V supply. The simulated power consumption of the divider core, the output buffer, and the entire chip including bias are 36.0, 8.7, and 49.2 mW, respectively. The chip power consumption increases to 51.7 mW when the input power is -5 dBm.

5.1.4   Measurements

The input sensitivity is measured using WR-6 100-μm GSG RF probes at the input (120–144 GHz) and 1.85-mm 150-μm GSG RF probes at one of the I/Q outputs (60–72 GHz) while the other output is floating (Fig. 5.4). The chip, including bias and output buffers, consumes 45.1 mW from a 2 V supply.

The measured and simulated input sensitivity curves are shown in Fig. 5.5. The simulated f_{osc} is 132 GHz while the measured f_{osc} is 125–130 GHz, with an input sensitivity of -25 dBm. The divider operates at 120–140 GHz (limited by the on-chip baluns and measurement setup) with < -4 dBm input power at 120–134 GHz. Without the baluns, the divider operates at 105–154 GHz in simulations. In the future design, more resistance could be switched into the load for static operation as in [5].

The output power is measured using an Agilent V8486A power sensor with de-embedded probe and cable loss. The results agree well with simulations, and the imbalance between the outputs is < 2 dB (Fig. 5.6). A higher output power could be achieved by cascading an amplifier stage after the buffer.

Divider phase noise contribution is evaluated by comparing the phase noise measurement results between two setups. In the first setup, the AMC 333 is configured as a ×6 multiplier by removing the last doubler. The output phase noise is measured with the Agilent E5052B signal source analyzer after down conversion. The second setup is the same as Fig. 5.4, where the AMC 333 is configured as a ×12 multiplier. The phase noise profiles of the two setups are virtually identical, which demonstrate that the divider contributes negligible phase noise at 100 Hz – 10 MHz offset (Fig. 5.7).
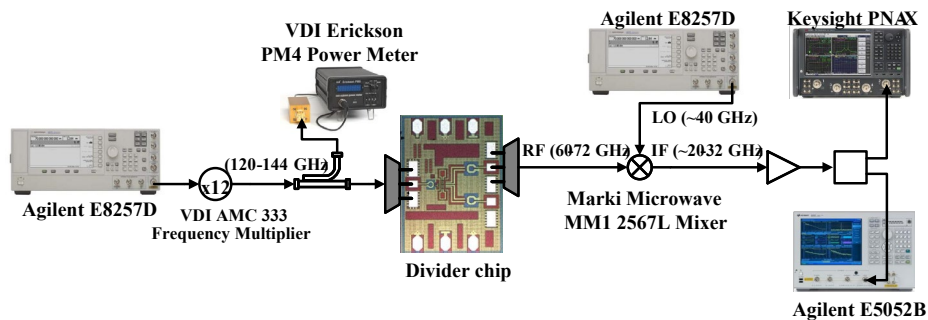
Fig. 5.4. Measurement Setup for Input Sensitivity and Phase Noise
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Table I compares the performance of this work with the state-of-the-art SiGe frequency dividers. The divider in this letter demonstrates a very competitive power consumption.

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Table 5.1. High-Frequency SiGe Divider Comparison

Design	This Work	[6] TMTT'12	[7] EuMIC'15	[2] RFIC'09	[8] BCTM'09	[1] GeMiC'15	[9] EDL'15	[10] BCTM'10	[11] CSIC'05
Static Divider?	No	No	No	No	No	Yes	Yes	Yes	Yes
Technology	90-nm SiGe	0.12-um SiGe	0.13-um SiGe	0.18-um SiGe	0.2-um SiGe	0.13-um SiGe	0.13-um SiGe	0.13-um SiGe	0.14-um SiGe
Transistor f_t/f_{max} (GHz)	285 / 310	280 / 400	300 / 500	200 / -	215 / -	300 / 500	300 / 500	230 / 350	225 / -
Supply Voltage (V)	2.0	1.5	4.9	3.3	4.0	4.9	3.6	5.8	5.2
Core Power (mW) Total Power (mW)	36 45.1	32.0 -	392 -	- 115.5	105 320	392 -	- 154.4	210 -	340 -
f_{osc} (GHz)	130	-	149	104	-	111.6	-	98	-
Max. Division Freq. (GHz)	142	148	166	113	168	>128.7	161	133	>110
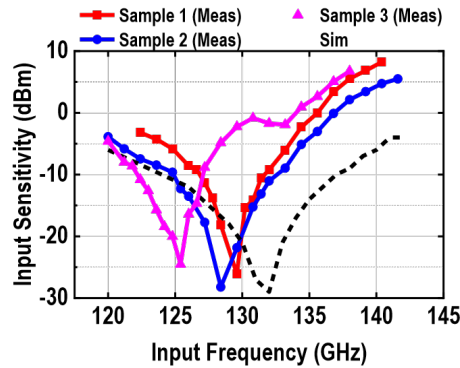
Fig. 5.5. Measured and Simulated Input Sensitivity Curves
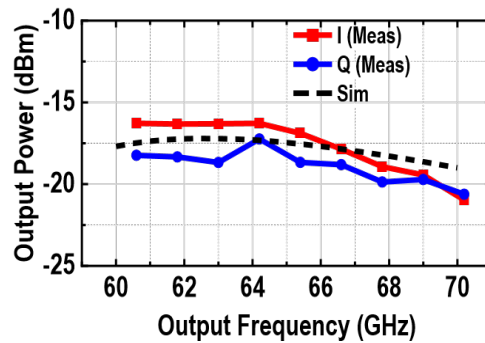
Fig. 5.6.   Measured Output Power Curves
The probe and cable loss are deembedded.

5.1.5   Conclusion

In this letter, a tuned frequency divider in a 90-nm SiGe BiCMOS process is presented. Design considerations for sizing, current density, and layout are discussed. The divider achieves an f_{osc} of 130 GHz in a silicon-based process with the lowest power consumption and can operate up to 140 GHz with < 4 dBm of input power. As the divider contributes negligible phase noise, potential applications include frequency synthesis in the 120–140 GHz band.
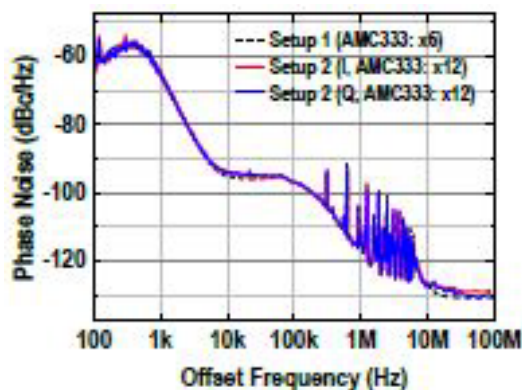
Fig. 5.7. Comparison of the measured phase-noise profiles between setups 1 and 2 at 64.2 GHz. Spurs at 0.3–8 MHz are due to the AMC 333 power supply.

5.1.6   References

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6   LOW PHASE NOISE VCO

6.1   A 28-GHz Low Phase Noise Class-C Transformer VCO with 187-dBc/Hz FoM in 90-nm SiGe BiCMOS

Zhaoxin Hu, *Graduate Student Member, IEEE,* Eric Wagner, *Member, IEEE,* Tzu-Chien Hsueh, *Senior Member, IEEE,* and Gabriel M. Rebeiz, *Fellow, IEEE*

Abstract—This paper presents a 27.9–28.8 GHz voltage-controlled oscillator (VCO) in a 90-nm SiGe BiCMOS process. The VCO consists of class-C active devices and a transformer tank. A transformer tank model which captures all parasitic capacitance is formulated. Several transformer design examples are studied, and a transformer tank is also compared with an LC tank in terms of quality factor and tuning range. The VCO achieves a state-of-the-art phase noise of -111.5 dBc/Hz at 1-MHz offset. The figure-of-merit (FoM) is 187 dBc/Hz and the flicker corner is 100 kHz with a power consumption of 24.7 mW. Potential applications include phase-locked loops (PLLs) for wireless systems at 28, 60, and 90 GHz.

Index Terms—Class-C, phase noise, phase-locked loop (PLL), SiGe BiCMOS, transformer, voltage-controlled oscillator (VCO).

6.1.1   Introduction

Wireless communication systems at 24–29, 57–71, and 92–95 GHz offer multi-Gb/s data rate using wide bandwidth and high-order quadrature amplitude modulation (QAM) [1]–[3]. Stringent requirements on the error-vector magnitude (EVM) of the transmitter (TX) and receiver (RX), particularly the contribution of the local oscillator (LO), must be met to deliver the desired modulation quality. In 5G New Radio, the maximum allowed TX EVM for 64-QAM is 8% [4], [5]. In IEEE 802.11ad (60-GHz band), to support 64-QAM with orthogonal frequency-division multiplexing (OFDM), a TX EVM of -26 dB (5%) is required for the modulation and coding scheme index of 12.3 [6]. Apart from the LO, the EVM contribution is mostly from the power amplifier. Assuming equal contributions, both should be < 3.6% if an overall 5% TX EVM is desired. The LO contribution is typically < 2% to provide enough margin for power amplifiers.

The LO contribution to the EVM can be expressed as [7]

$$EVM_{LO(\%)} = \sqrt{2 \int \mathcal{L}(f)df} \times 100\% \tag{1}$$

where $\mathcal{L}(f)$ (in dBc/Hz) is the spot phase noise at the offset frequency f. The square root term is the definition of the double-sideband (DSB) phase error (in radians), and the corresponding root-mean-square (RMS) jitter (in seconds) is obtained by dividing it by $2\pi f_{osc}$ (oscillation frequency in rad/s). To keep the LO EVM contribution at < 3.6%, the required DSB phase error is 0.036 rad (2.06°), and the RMS jitters are 205/95/64 fs at 28/60/90 GHz. The RMS jitters should be < 114/53/35 fs at 28/60/90 GHz if the LO EVM contribution is < 2%.
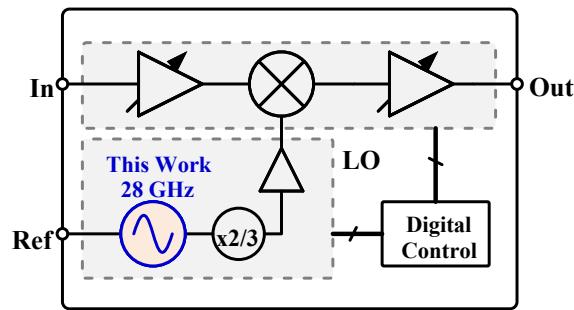
Fig. 6.1. Block Diagram of a 28-/60-/90-GHz TX/RX

The LO consists of a frequency synthesizer near 28 GHz and a frequency multiplier for 60-/90-GHz systems.

While an LO near 28 GHz can be implemented with a synthesizer at 28 GHz, a practical approach to achieve a 60/90 GHz LO is to employ a frequency multiplier (Fig. 6.1). Consider a 60-GHz TX example, the required DSB phase error of the 28-GHz synthesizer should be halved while the RMS jitter is the same. It is reasonable to assume that in-band phase noise is flat, and out-of-band phase noise rolls off at 20 dB/dec. To meet a 2% or 3.6% LO EVM requirement over 1 kHz–10 MHz integration bounds, if the in-band noise is -95 dBc/Hz, the loop bandwidth should be 80 kHz or 250 kHz. The resulting out-of-band phase noise at 1-MHz offset is therefore -117 dBc/Hz or -107 dBc/Hz, respectively. This sets a constraint for VCO phase noise which dominates the out-of-band noise.

This paper presents a class-C transformer VCO that achieves a very low phase noise. The class-C topology is especially suitable for heterojunction bipolar transistors (HBTs) in SiGe process technologies [8]–[10]. Transformer tanks were studied in previous work (e.g. [11]–[13]), and the relation between the resonant frequency (ω_{res}), tank impedance (Z_{tank}), quality factor (Q), and some key design parameters (see Section II-A) were analyzed. However, all previous models neglected the coupling capacitance between the primary and secondary coils, and transformers employing wide coils for low ohmic loss have significant parasitic coupling capacitance between them (e.g. [7], [10]). In addition, the analysis assumed that the key design parameters can be independently tuned to improve Q. In practice, several parameters could be changed simultaneously, e.g., by varying the geometry, which might have opposing effects on Q. As an example, the Q-factors of the individual coils might degrade when their separation is reduced for a stronger coupling coefficient (k).
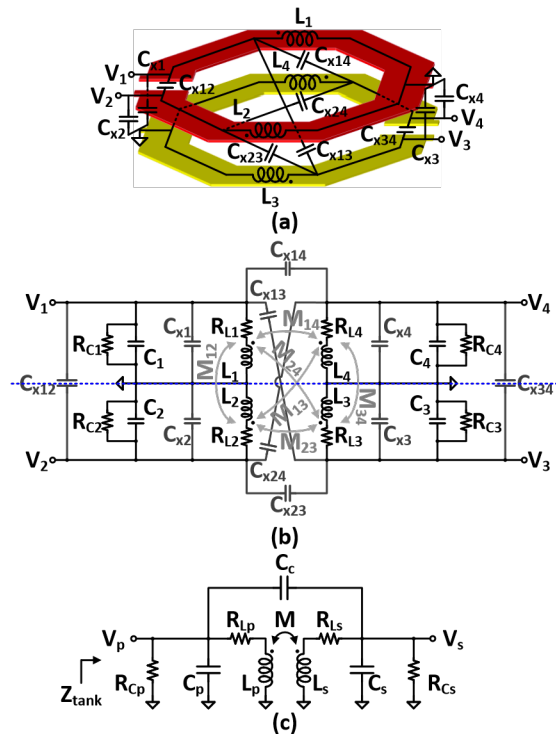
Fig. 6.2. Single-turn Stacked Transformer
(a) layout (series resistors and mutual inductors are not annotated for brevity), (b) 4-port model, and (c) 2-port half circuit in CM and DM

This paper aims to address these issues by developing a transformer tank model considering the coupling capacitors between the coils. New expressions for ω_{res}, Z_{tank}, and Q are provided. Design examples are presented to study the effect of coil separation on Q. Transformer tanks are also compared with LC counterparts.

The paper is organized as follows. Section 6.1.2 presents the transformer tank model, studies the design examples, and compares the transformer and LC tanks. Section 6.1.3 describes the implementation of the class-C transformer VCO. The measurement results are provided in Section 6.1.4 and conclusions are drawn in Section 6.1.5.

6.1.2 Transformer Tank Analysis

A. Transformer Tank Model

Consider the single-turn stacked transformer used in resonant tanks of mm-wave VCOs with all parasitic components annotated (Fig. 6.2(a)). The full 4-port model in Fig. 6.2(b) captures all parasitic capacitance ($C_{x13,14,23,24}$) between the primary and secondary coils. C_{1-4} are the fixed capacitors and varactors added to the tank. If the tank is symmetrical along the dashed blue line, the equivalent 2-port common-mode/differential-mode (CM/DM) half circuits are shown in Fig. 6.2(c), and the relations between the components in the 4-port model and 2-port half circuits are listed in Table 6.1.

Table 6.1. Components in the 2-Port Half Circuits

Component	CM	DM
L_p	$\frac{1}{2}(L_1 + M_{12})$	$2(L_1 - M_{12})$
L_s	$\frac{1}{2}(L_3 + M_{34})$	$2(L_3 - M_{34})$
M	$\frac{1}{2}(M_{13} + M_{14})$	$2(M_{13} - M_{14})$
C_p	$2(C_1 + C_{x1})$	$\frac{1}{2}(C_1 + C_{x1}) + C_{x12} + C_{x14}$
C_s	$2(C_3 + C_{x3})$	$\frac{1}{2}(C_3 + C_{x3}) + C_{x34} + C_{x14}$
C_c	$2(C_{x13} + C_{x14})$	$\frac{1}{2}(C_{x13} - C_{x14})$
R_{Lp}	$\frac{1}{2}R_{L1}$	$2R_{L1}$
R_{Ls}	$\frac{1}{2}R_{L3}$	$2R_{L3}$
R_{Cp}	$\frac{1}{2}R_{C1}$	$2R_{C1}$
R_{Cs}	$\frac{1}{2}R_{C3}$	$2R_{C3}$

In the DM half circuit, C_c is usually negative as $C_{x14} > C_{x13}$. Both CM and DM half circuits have two parallel resonances and CM resonance is often employed in CMOS oscillators for flicker-noise suppression [7], [14]–[16]. Nevertheless, flicker noise is rarely an issue in SiGe HBTs and the discussion will focus on the 2-port DM half circuit.

In the subsequent analysis, the primary side is connected to the active devices. The tank impedance (Z_{tank}) looking into the primary side in Fig. 6.2(c) has two parallel resonant frequencies ($\omega_{res,1} < \omega_{res,2}$). The tank is usually designed such that oscillation occurs near $\omega_{res,1}$, unless for wideband operation where both $\omega_{res,1}$ and $\omega_{res,2}$ can be used [17]–[19].

It is convenient to define the following variables to compute Z_{tank}, Q, and $\omega_{res,1}$ ($\omega_{res,2}$). Denote $C'_p = C_p + C_c$ and $C'_s = C_s + C_c$. The resonant frequencies of the primary and secondary sides can be defined as $\omega_p = 1/\sqrt{L_p C'_p}$ and $\omega_s = 1/\sqrt{L_s C'_s}$, and $\sigma_c = 1/\sqrt{L_p L_s C_c}$ can be regarded as the "resonant frequency" associated with C_c.

The key design parameters are (i) the "normalized" resonant frequencies, defined as $u_p = \omega_p^2/\omega_{res,1}^2$, and $u_s = \omega_s^2/\omega_{res,1}^2$, and $u_c = \sigma_c/\omega_{res,1}^2$ (usually negative), and (ii) the Q-factors of the inductors and capacitors at $\omega_{res,1}$, defined as $Q_{Lp} = \omega_{res,1}L_p/R_{Lp}$, $Q_{Ls} = \omega_{res,1}L_s/R_{Ls}$, $Q_{Cp} = \omega_{res,1}C_pR_{Cp}$, and $Q_{Cs} = \omega_{res,1}C_sR_{Cs}$. If the Q-factors are high, Z_{tank} can be expressed as

$$Z_{tank} = \frac{b}{a} \approx \frac{b_0 + b_1 s + b_2 s^2 + b_3 s^3}{1 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4}\omega_{res,1}L_p$$

(2)

where

$$b_0 = \frac{1}{Q_{Lp}}$$

(3a)

$$b_1 = \frac{1}{\omega_{res,1}}$$

(3b)

$$b_2 = \frac{1}{\omega_{res,1}^2} \frac{1}{u_s} \left(\frac{1}{Q_{Lp}} + \frac{1}{Q_{Ls}} + \frac{(1-k^2)}{Q_{Cs}} \right)$$

(3c)

$$b_3 = \frac{1}{\omega_{res,1}^3} \frac{1}{u_s} (1-k^2)$$

(3d)

$$a_1 = \frac{1}{\omega_{res,1}} \left(\frac{1}{u_p Q_{Lp}} + \frac{1}{u_s Q_{Ls}} + \frac{1}{u_p Q_{Cp}} + \frac{1}{u_s Q_{Cs}} \right)$$

(3e)

$$a_2 = \frac{1}{\omega_{res,1}^2} \left(\frac{1}{u_p} + \frac{1}{u_s} - \frac{2k}{u_c} \right)$$

(3f)

$$a_3 = \frac{1}{\omega_{res,1}^3} \left[\left(\frac{1}{u_p u_s} - \frac{1}{u_c^2} \right) \left(\frac{1}{Q_{Lp}} + \frac{1}{Q_{Ls}} \right) \right.$$
$$\left. + (1-k^2) \frac{1}{u_p u_s} \left(\frac{1}{Q_{Cp}} + \frac{1}{Q_{Cs}} \right) \right]$$

(3g)

$$a_4 = \frac{1}{\omega_{res,1}^4} \left(\frac{1}{u_p u_s} - \frac{1}{u_c^2} \right) (1-k^2)$$

(3h)

At the resonant frequencies, $|Z_{tank}|$ can be calculated based on the following observation. If the tank were lossless, a would be real (= 0 at resonance), and b would be imaginary. For finite but high Q_{Lp}, Q_{Ls}, Q_{Cp} and Q_{Cs}, the imaginary parts of a and b dominate since the tank impedance is real at resonance. $|Z_{tank}| \approx$ Im$\{b\}$/Im$\{a\}$ and is shown in (4). $Q = |\frac{1}{2}\omega \frac{d}{d\omega} \angle Z_{tank}|$ evaluated at $\omega_{res,1}$ [20]. $\frac{d}{d\omega} \angle Z_{tank} = \frac{d\angle b}{d\omega} - \frac{d\angle a}{d\omega}$, and it can be shown that $\frac{d\angle a}{d\omega}$ dominates at $\omega_{res,1}$ and $\frac{d\angle a}{d\omega} \approx \frac{d}{d\omega} (\text{Re}\{a\}) / \text{Im}\{a\}$ after further simplifications. Q therefore can be approximated as (5).

(4)

$$|Z_{tank}| \approx \frac{u_p \left[u_s - (1-k^2) \right] Q_{Lp} Q_{Ls}}{Q_{Lp} \left(u_p - 1 + \frac{u_p u_s}{u_c^2} \right) + Q_{Ls} \left(u_s - 1 + \frac{u_p u_s}{u_c^2} \right) + Q_{Lp} Q_{Ls} \left[\frac{u_p}{Q_{Cs}} + \frac{u_s}{Q_{Cp}} - (1-k^2) \left(\frac{1}{Q_{Cp}} + \frac{1}{Q_{Cs}} \right) \right]} \omega_{res} L_p$$

$$Q \approx \frac{2u_p u_s - u_p - u_s + \frac{2k u_p u_s}{u_c}}{Q_{Lp} \left(u_p - 1 + \frac{u_p u_s}{u_c^2} \right) + Q_{Ls} \left(u_s - 1 + \frac{u_p u_s}{u_c^2} \right) + Q_{Lp} Q_{Ls} \left[\frac{u_p}{Q_{Cs}} + \frac{u_s}{Q_{Cp}} - (1-k^2) \left(\frac{1}{Q_{Cp}} + \frac{1}{Q_{Cs}} \right) \right]} Q_{Lp} Q_{Ls}$$

(5)

The expressions for $|Z_{tank}|$ and Q are similar to the ones in [11] and [12], but the analysis presented here is simpler and also considers the effect of u_c which arises from C_c.

$\omega_{res,1}$ (and $\omega_{res,2}$) can be calculated based on observation that $\text{Re}\{a\} = 0$ at resonance.

$$(1 - k^2)\left(\frac{1}{\omega_p^2 \omega_s^2} - \frac{1}{\sigma_c^2}\right)\omega_{res}^4 - \left(\frac{1}{\omega_p^2} + \frac{1}{\omega_s^2} - \frac{2k}{\sigma_c}\right)\omega_{res}^2 \tag{6a}$$
$$+1 = 0$$

There are many possible combinations of ω_p and ω_s to achieve the same $\omega_{res,1}$ (or $\omega_{res,2}$) if k and σ_c are given. Alternatively,

$$(1 - k^2)\left(\frac{1}{u_p u_s} - \frac{1}{u_c^2}\right) - \left(\frac{1}{u_p} + \frac{1}{u_s} - \frac{2k}{u_c}\right) + 1 = 0 \tag{6b}$$

which serves as the constraint for u_p and u_s if k and u_c are given. Fig. 6.3 shows plots of u_s versus u_p for some k and u_c. Three regions stand out: (i) $u_p \ll u_s$ ($\omega_p \ll \omega_s$), (ii) $u_p \approx u_s$ ($\omega_p \approx \omega_s$), and (iii) $u_p \gg u_s$ ($\omega_p \gg \omega_s$).

(a)   (b)
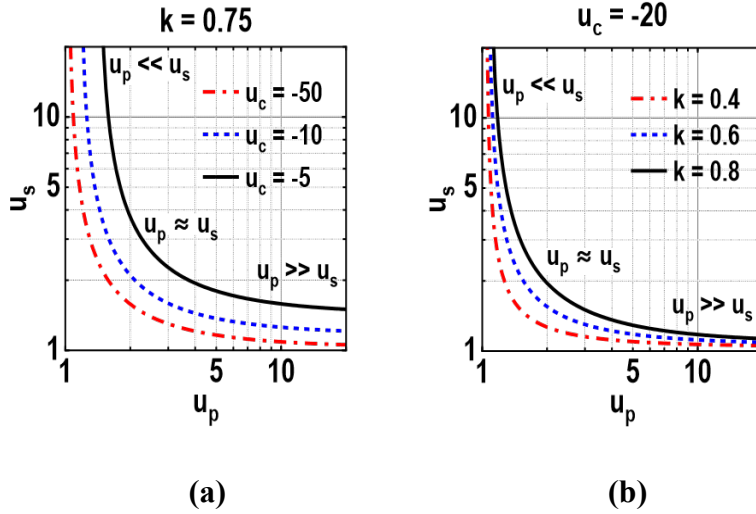
Fig. 6.3. u_s versus u_p when (a) $k = 0.75$ and u_c is varying, and (b) $u_c = -20$ and k is varying

B. Transformer Tank Design for Maximum Q

Since the same $\omega_{res,1}$ can be achieved with different combinations of u_p and u_s, it is worth investigating the condition for maximum Q. Once the transformer geometry is selected, $u_p(\omega_p)$ and $u_s(\omega_s)$ are mainly determined by how the tank capacitance is allocated between the primary and secondary sides.

Three design examples are shown in Fig. 6.4. The transformers are laid out on the top two metal layers. The extracted component values are given in Table II. Here, the same L_p and L_s are obtained with different widths and diameters. Capacitors with negligible loss are added to ensure $\omega_{res,1} = 2\pi(30 \times 10^9)$ rad/s. The simulated $|Z_{tank}|$ and Q versus u_p/u_s in Spectre are compared with the ones predicted by (4) and (5). Q is maximized when $u_p/u_s \approx 1$, or equivalently when the primary and secondary sides have the same resonant frequency. For single-turn stacked transformers with $L_p = L_s$, this corresponds to equally splitting the tank capacitance between the primary and secondary sides. As u_p/u_s becomes small or large, the tank Q approaches Q_{Lp} or Q_{Ls}. Consider the special case where $C_c = 0$ and hence $u_c = \infty$, if $Q_{Lp} = Q_{Ls}$ and
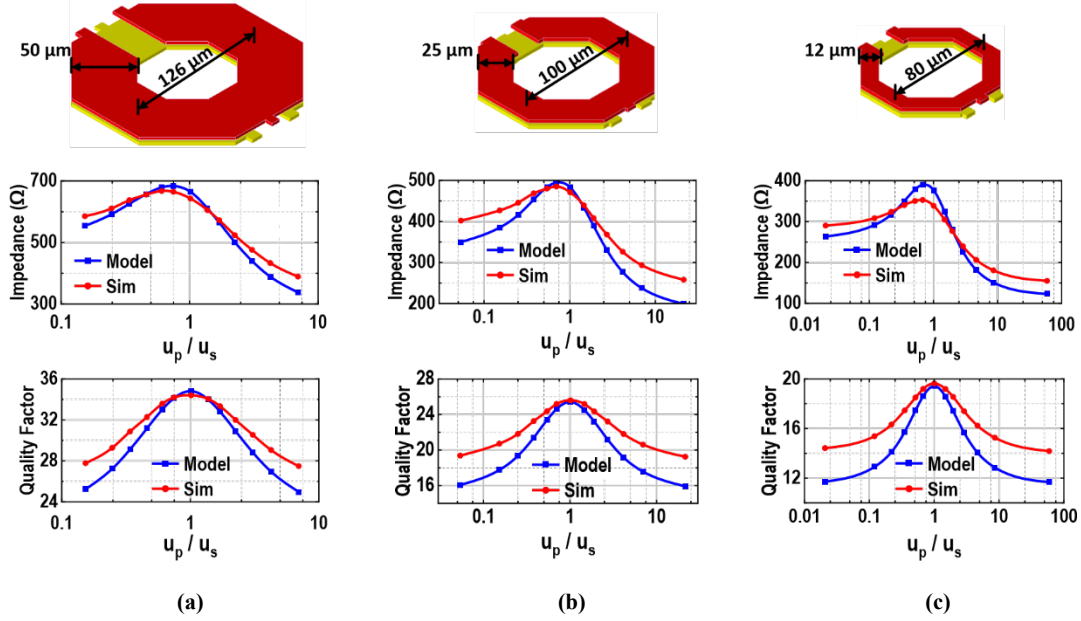
Fig. 6.4. Layout of the Transformer Examples with Dimensions |Z_{tank}| and Q based on simulations are compared with (4) and (5) for (a) width of 50 μm and diameter of 126 μm, (b) width of 25 μm and diameter of 100 μm, and (c) width of 12 μm and diameter of 80 μm.

$u_p/u_s = 1$, $|Z_{tank}| \approx \frac{1}{2}(1+k)^2 Q_{Lp}\omega_{res}L_p$ and $Q \approx (1+k)Q_{Lp}$, as noted in [11]. It is tempting to conclude that for closer primary and secondary coils, k will be larger, and hence the transformer tank will have a larger Q. However, the effect of separation on Q_{Lp} and Q_{Ls} must also be considered. The example in Fig. 6.4(b), shown again in Fig. 6.5(a), will be used to study the relation between Q and separation. It is assumed that the capacitors are lossless, $u_p/u_s = 1$, and $\omega_{res,1} = 2\pi(30\times10^9)$ rad/s in all cases. As the horizontal separation (S) increases, k is reduced while Q_{Lp} and Q_{Ls} becomes larger (Fig. 6.5(b)). This is reasonable as both the self-resonant frequency and the peak Q-factors of the coils increase. The tank Q in this example is maximized at a separation where k is slightly smaller than the maximum achievable value (Fig. 6.5(c)). However, when k is further reduced, $\omega_{res,2}$ becomes closer to $\omega_{res,1}$ and its resonant peak becomes larger in magnitude (Fig. 6.5(d)), increasing the likelihood of oscillation at the undesired peak.

The cases where Q_{Cp} or Q_{Cs} is finite, representing varactor loss, are studied next. It is reasonable to assume only one of Q_{Cp} or Q_{Cs} is finite and the other is still infinite, since the fixed capacitors on the other side, if added, can be implemented with custom metal-oxide-metal (MOM) capacitors with Q-factors above 100. Capacitors with three different combinations of Q_{Cp} and Q_{Cs} are added to the transformer in Fig. 6.4(b) for $\omega_{res,1} = 2\pi(30\times10^9)$ rad/s, and the simulated |Z_{tank}| and Q versus u_p/u_s are plotted in Fig. 6.6. Q is near the maxima when $u_p/u_s \approx 1$ for finite Q_{Cp} or Q_{Cs} just as the case where the capacitors are lossless.

Table 6.2. Transformer DM Half Circuit Component Values (without additional capacitors)

Transformer	(a)	(b)	(c)
L_p	123.2 pH	122.4 pH	120.8 pH
L_s	123.4 pH	122.8 pH	120.6 pH
M	87.4 pH	89.2 pH	80.8 pH
k	0.71	0.73	0.67
C_p	45.1 fF	19.2 fF	7.8 fF
C_s	46.8 fF	20.8 fF	8.7 fF
C_c	-14.8 fF	-8.0 fF	-3.9 fF
R_{Lp}	1.1 Ω	1.5 Ω	2.0 Ω
R_{Ls}	1.1 Ω	1.5 Ω	2.0 Ω
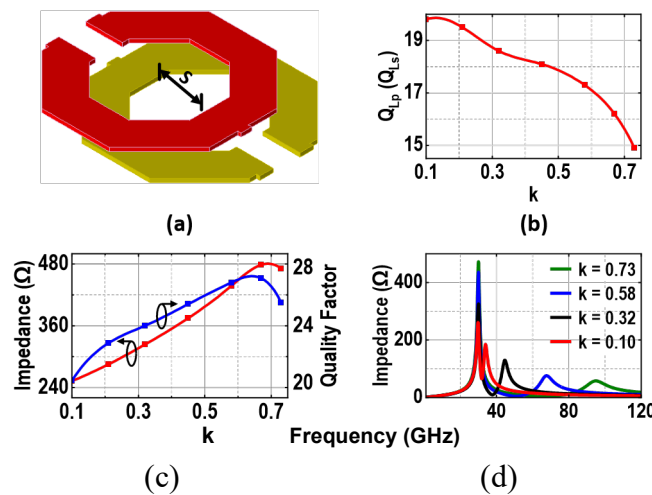
Fig. 6.5. (a) Layout of the transformer in Fig. 6.4(b) with coil separation S = 0–60 µm. **(b)** Simulated Q-factors of individual coils versus k. **(c)** |Z$_{tank}$| and Q versus k. **(d)** |Z$_{tank}$| versus frequency for different k

C. Comparison with LC Tanks

Transformer tanks do not provide any fundamental advantage in terms of Q compared to LC tanks [11], [21]. To validate the claim, consider first the transformer tank in Fig. 6.7(a) (same as Fig. 6.4(b)). When C_p = C_s = 125.5 fF with Q_{Cp} = Q_{Cs} = ∞ are added, Q = 25.6 and |Z_{tank}| = 471.4 Ω. An inductor (L = 96.5 pH) can be designed as in Fig. 6.7(b) such that Q = 25.6 and |Z_{tank}| = 472.9 Ω when 291.1 fF of capacitance with negligible loss is added.

Next, the 4 possible configurations to include varactors (Fig. 6.7(c)) are compared. The varactors have close to minimum lengths for the maximum Q-factors (11.5–23) and the corresponding $(C_{max} - C_{min})/C_{avg}$ = 60%. The fixed capacitors and varactors are sized such that a 10% tuning range in $\omega_{res,1}$ is achieved at the extremes of the control voltage.
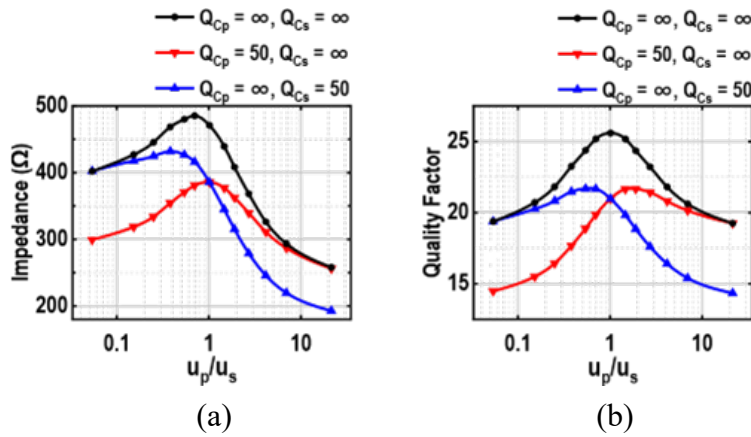
Fig. 6.6. Simulated (a) $|Z_{tank}|$ and (b) Q versus u_p/u_s for the example in Fig. 6.4(b).
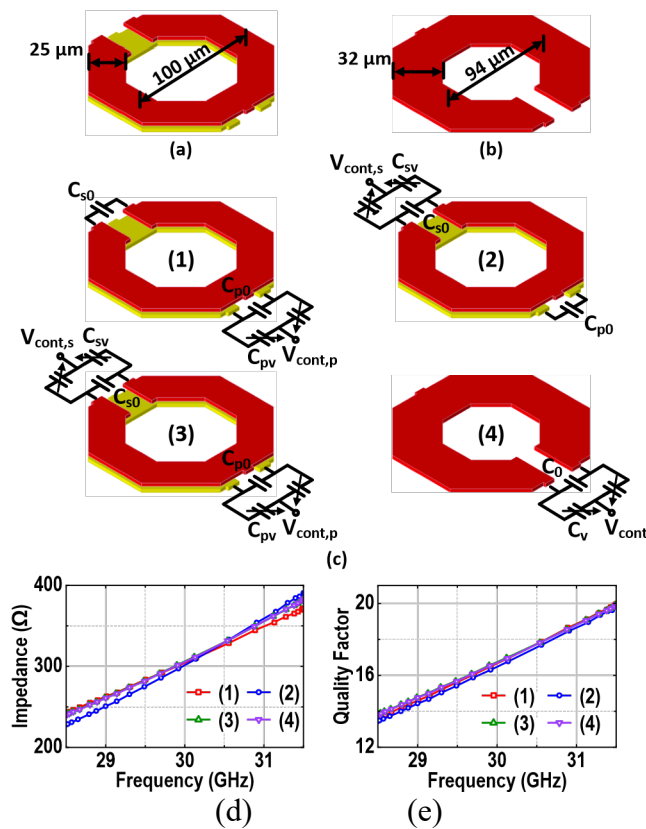
Fig. 6.7. (a) Layout of the transformer in Fig. 6.4(b). (b) An inductor with the same Q and $|Z_{tank}|$ as the transformer tank can be achieved, (c) 4 possible tank configurations with lossy varactor. (1)–(3) are based on the transformer, and (4) is based on the inductor. Simulated (d) $|Z_{tank}|$ and (e) Q of the tanks

The required varactor sizes are nearly identical in all cases (70–130 fF), except for configuration (3) where varactors are added to both sides and only 35–65 fF is required. As shown in Fig. 6.7(d) and (e), the simulated $|Z_{tank}|$ and Q are almost the same for all 4 tanks.

31

A class-C VCO example is shown in Fig. 6.8(a) incorporating these 4 tanks. The fixed capacitance in configuration (4) and on the primary side of configurations (1)–(3) is reduced by ~50 fF to account for the capacitive loading of the active devices. The bias current is also adjusted for the same oscillation amplitude, shown in Fig. 6.8(b). The simulated phase noise at 1-MHz offset (Fig. 6.8(c)) is similar in these 4 cases. The phase noise of configurations (2) and (3) is slightly lower than (4), which in turn has a minor advantage compared to (1).
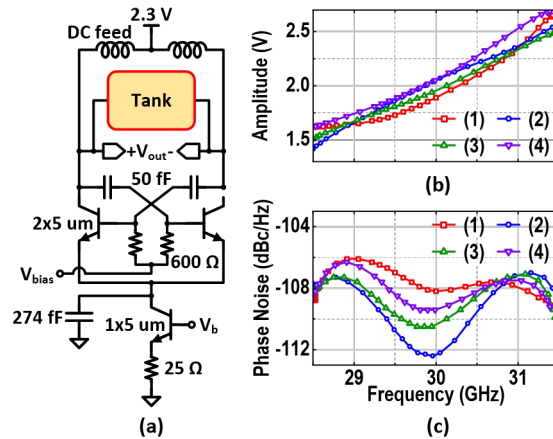
Fig. 6.8. (a) Schematic of the Class-C VCO example, the 4 Design Examples in Fig. 6.7(c) are used as the Tanks, Simulated (b) Oscillation Amplitude and (c) Phase Noise at 1-MHz Offset Versus Oscillation Frequency
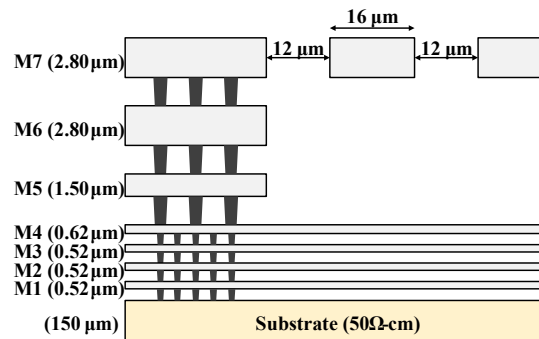
Fig. 6.9. Tower Semiconductor's 90-nm SiGe BiCMOS process stackup

As shown in the previous examples, it is possible to find an LC tank with almost the same Q and $|Z_{tank}|$ as a transformer tank, even in the case where varactors are included. The resulting VCO phase noise is also similar, with the transformer tank in configuration (2) having a small advantage. However, in LC tanks, the varactor gates are always biased at the supply voltage, a disadvantage if only one supply domain is allowed, and the control voltage cannot exceed the supply. The same is true for (1) and (3) in Fig. 6.7(c). The transformer tank in (2) offers the advantage of biasing the varactors at a different voltage through the center tap of the secondary coil. The control voltage hence need not exceed the supply, and the tuning range is not compromised compared to the LC tank or other transformer tank configurations.

6.1.3   VCO AND PLL DESIGN AND IMPLEMENTATION

A. VCO

The VCO is designed in Tower Semiconductor's 90-nm SiGe BiCMOS process. The process offers high-performance NPN HBTs (f_t/f_{max} at 285/310 GHz [22]) and thick top metal layers (Fig. 6.9). The VCO schematic is shown in Fig. 6.10(a).
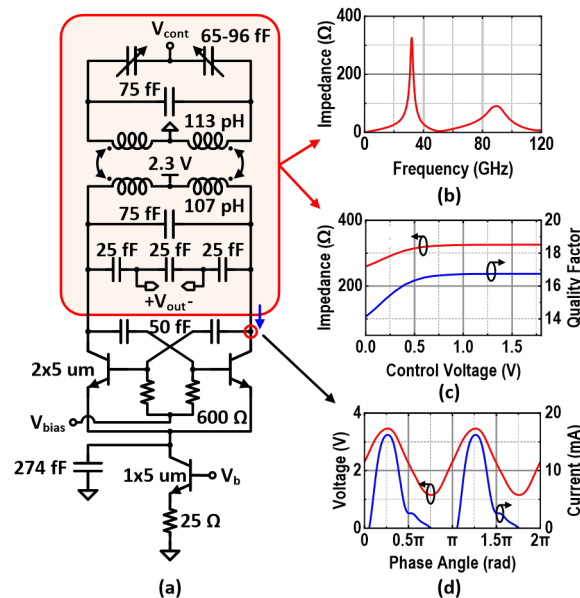
Fig. 6.10. (a) VCO schematic. Other Components of the 4-port Tank Model are not Shown for Brevity (b) Simulated Tank Impedance versus Frequency (Vcont = 1 V). (c) Simulated |Ztank| and Q Versus Control Voltage (d) Simulated single-ended Tank Voltage and Current Waveforms (Vcont = 1 V)

The VCO transformer, shown in Fig. 6.11(a), has a width of 23 μm and a diameter of 100 μm. It has a similar geometry to Fig. 6.4(b) for a relatively high tank Q, compact area, and ease of routing. The primary coil is laid out by stacking M3–M5 with via connections. The secondary coil, which is connected to the varactors, is built on the top two metal layers (M6 and M7 stacked and connected with vias). In the transformer DM half circuit, $L_p \approx L_s \approx 120$ pH, $k \approx 0.7$, and the peak Q-factors are 15 and 17 for the primary and secondary coils, respectively (Fig. 6.11(b)). All capacitors, except for the varactors and the tail capacitor, are implemented with custom interdigitated MOM capacitors. They are laid out on M1–M3 with a capacitance density of ~0.54 fF/μm². Two fixed differential capacitors of 75 fF are added to the primary and secondary sides, and the simulated Q-factors are > 130 near 28 GHz (Fig. 6.11(c)). The MOS varactors have a tuning range of 65–96 fF and a Q-factor of 14–23 near 28 GHz.

The varactors are placed on the secondary side as in configuration (2) of Fig. 6.7(c). Placing the varactors on the secondary side ensures that $u_p/u_s \approx 1$ since the active devices and buffers connected to the primary side introduce ~100 fF of single-ended capacitive loading. In addition, the control voltage (V_{cont}) need not exceed the supply, and the tuning range is not compromised.

The tank without varactors has a Q of around 20 at 28 GHz, and the complete tank including the varactors and buffer loading has a $|Z_{tank}|$ of 260–320 Ω and a Q of 14–17 depending on V_{cont} (Fig. 6.10(c)). The tuning sensitivity of the VCO (K_{vco}) is around 400 MHz/V near 28 GHz.

Switched capacitor banks were not included in this design to achieve the highest possible Q and hence the lowest possible phase noise at the expense of tuning range. A VCO design with switched capacitor banks and a wider tuning range is provided in the appendix to show Q and phase noise degradation due to switch loss.

Fig. 6.11. (a) Transformer and MOM Capacitor Layout, (b) Simulated DM inductance and Q-factors of the Transformer Primary and Secondary Coils, (c) Simulated Capacitance and Q-factors of the 75-fF MOM Capacitors

Fig. 6.12. VCO Chip Micrograph

An 8 mA bias provided by an HBT tail current source is chosen for a large swing without driving the VCO deeply into the voltage-limited regi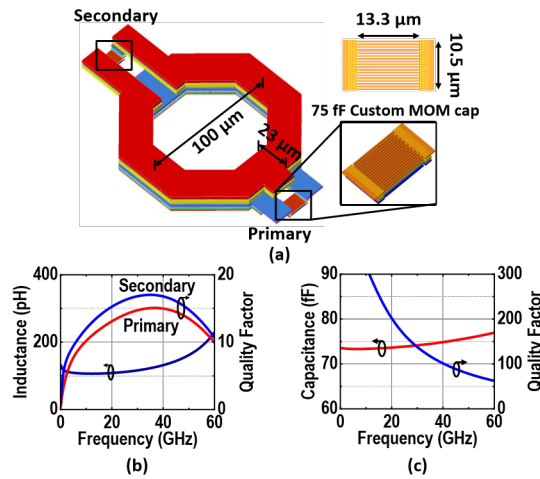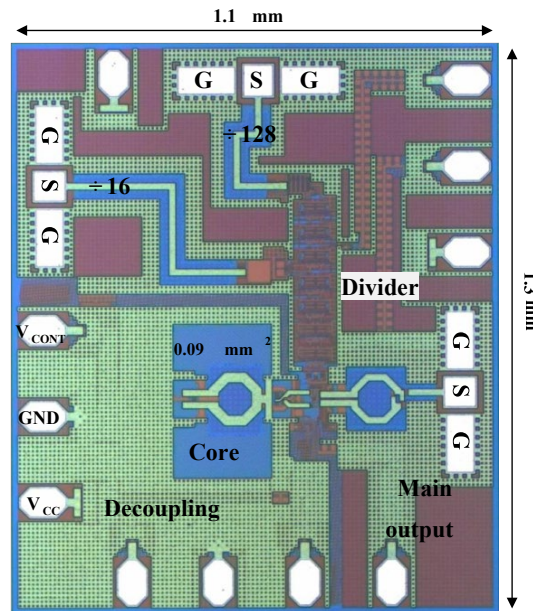me. The cross-coupled HBT pair is then sized to operate at a high f_t/f_{max}. The base terminals are connected to a 1.3-V bias voltage through resistors, which are chosen to be 600 Ω to minimize noise contribution. AC coupling capacitors C_{bias} = 50 fF with a capacitive feedback ratio $C_{bias}/(C_{bias} + C_{be})$ of ~0.4 ensure VCO start-up and prevent phase noise degradation due to B-C junctions turning on. A 274-fF tail capacitor enables class-C operation and filters the noise of the tail current source without introducing amplitude instability. The single-ended voltage and current waveforms of the tank are shown in Fig. 6.10(d). The maximum V_{ce} of the cross-coupled HBTs is 2.8 V which is higher than BV_{ceo}. However, BV_{ceo} is not a fundamental limit for the allowed voltage swing [23], [24] as the base terminals are not seeing an open circuit. Practical HBT circuits can be designed to allow V_{ce} to be 1.5–2× higher than BV_{ceo} [25], [26].

The chip incorporates two common-emitter buffers at the output of the VCO core. To minimize their loading effect, a divider consisting of 3 capacitors in series is used and the buffers are connected to the middle 25-fF capacitor. One buffer is connected to an on-chip balun to facilitate single-ended measurements, and the simulated power at the balun output is -3.3 dBm at 28 GHz. The other buffer is connected to a chain of fixed divide-by-2 dividers. The static current-mode logic (CML) dividers are implemented with HBTs for high-speed operation. The chip has two additional outputs after the 4th and 7th dividers, with overall division ratios of 16 and 128, respectively. The 4th divider (at ~1.75 GHz) is connected to the output pads through a buffer and a differential to single-ended converter. CML-to-CMOS logic converters and CMOS output drivers are connected between the 7th divider (at ~220 MHz) and output pads. These low-frequency outputs can be connected to external PLL synthesizers for frequency synthesis.
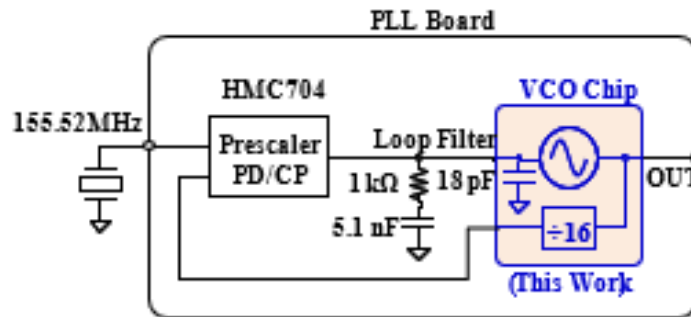
Fig. 6.13. Block Diagram of the Integer-N type-II Charge-pump PLL.

The VCO core operates from separate 2.3-V supply and ground domains from the rest of the chip. This reduces noise coupling from the other blocks. Separation of the ground domains does not pose any issue as the VCO core and buffers are differential and AC-coupled. In simulation, the VCO core consumes 24.9 mW including bias. The buffers and the divider chain are in another 2.3-V supply domain and consume 17.7 and 33.0 mW, respectively. The chip micrograph is shown in Fig. 6.12. The size of the VCO core is 0.09 mm^2, and the entire chip has a size of 1.1 × 1.3 mm^2.

B. PLL

An integer-*N* type-II charge-pump PLL working near 28-GHz is designed with the VCO (Fig. 6.13). Usually, the VCO contribution to the LO RMS jitter (or EVM) should be slightly less than half to account for the contribution from other blocks. In a 28-GHz system, to limit the EVM contribution of the VCO to

35

1.2%, or equivalently an RMS jitter of 67 fs, the loop bandwidth is calculated to be around 420 kHz given the VCO phase noise (see Fig. 6.16(c)).

As for the prescaler, a large division ratio N can be selected if a smaller channel spacing is desired, which would require a proportionately large reference division ratio. However, the noise contribution from the phase detector (PD) and charge pump (CP) can be excessive as they are multiplied by N^2. For this reason, the division ratio is chosen to be below 400. The resulting PD frequency is around 70 MHz.

Given the loop bandwidth, N, and K_{vco}, the choice of loop filter component values can be determined if the phase margin and CP current (I_{cp}) are specified. The phase margin is chosen to be greater than 60° and I_{cp} = 2.5 mA. The required resistor (1 kΩ) and zero capacitor (5.1 nF) are implemented with surface-mount devices on the PCB and the pole capacitor (18 pF) is absorbed into the on-chip decoupling capacitor. N and K_{vco} can vary as the PLL output frequency changes. The CP current is programmable to keep the loop transfer function roughly unchanged and maintain a low RMS jitter.
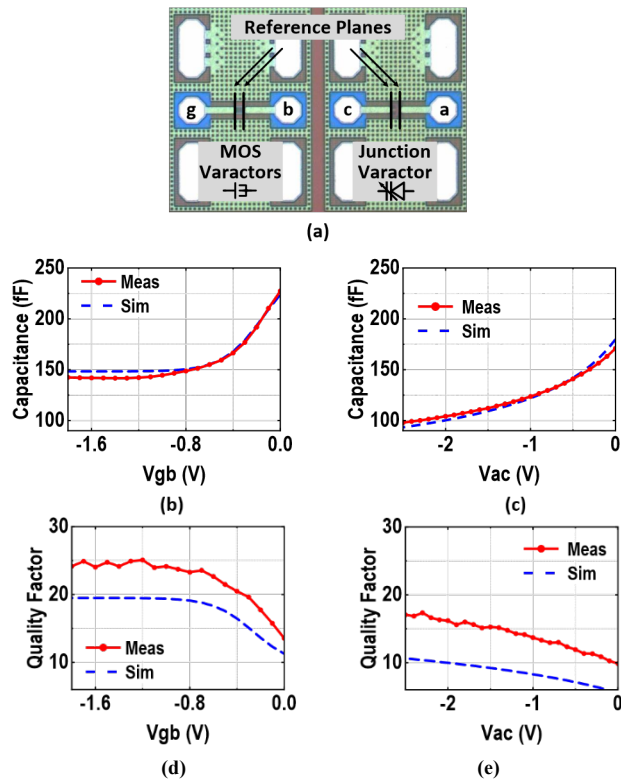
Fig. 6.14. Micrograph of the MOS and Junction Varactor Test Structures (a), Capacitance of the (b) MOS Varactors and (c) Junction Varactor, Q-factors of the (d) MOS Varactors and (e) Junction Varactor at 30 GHz

The prescaler, PD, and CP are all included in the Analog Devices' HMC704 synthesizer. An Abracon ABLNO-155.52MHz crystal oscillator with -160 dBc/Hz phase noise at 1-MHz offset is used as the reference and is divided by 2 in the HMC704 such that f_{PD} = 77.76 MHz. The VCO chip is bonded onto the PLL board, and the ÷16 output is routed to the HMC704 with a 50-Ω transmission line. All supply and bias voltages (including V_{bias} in Fig. 6.10(a)) are provided by ADM7151 low-noise low-dropout regulators from Analog Devices.

6.1.4 MEASUREMENTS

A. Varactors

The process offers PN-junction varactors in addition to MOS varactors. To evaluate their performance, test structures of the MOS varactors used in the VCO and a junction varactor of similar tuning capacitance are fabricated (Fig. 6.14(a)). The MOS varactor sizes are 4×2.5 µm/0.2 µm (close to minimum length) with 5 vertical fingers, and two varactors are connected in parallel. The junction varactor anode area is 3×20 µm×0.9 µm. The measurement results include the routing resistance and capacitance up to the top metal. Pad capacitance and routing inductance on the top metal are de-embedded.
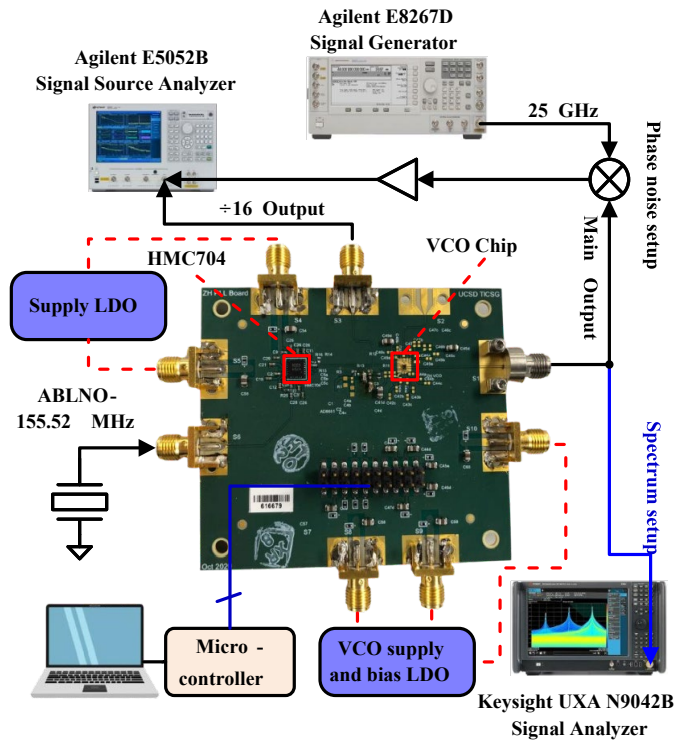
Fig. 6.15. Measurement setup for the VCO and PLL
The phase noise of the main output is measured after downconversion.
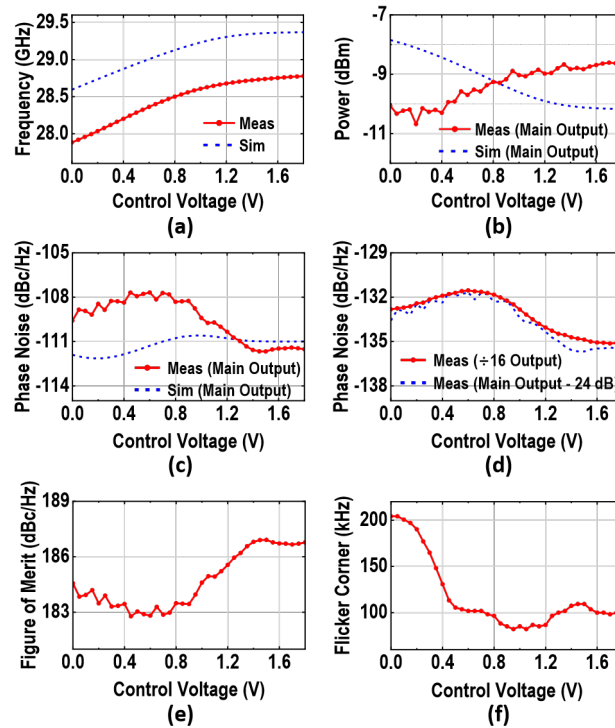
Fig. 6.16. (a) Measured and Simulated f_{osc} versus Control Voltage (b) Measured and Simulated VCO Main Output Power, including Bondwire, PCB Trace, and Connector Loss (c) Measured and Simulated VCO Main Output Phase Noise at 1-MHz Offset versus Control Voltage (d) Measured VCO Phase Noise of the Main and ÷16 Outputs (e) Measured VCO FoM at 1-MHz Offset (f) Measured VCO Flicker Corner

As shown in Fig. 6.14(b), the MOS varactors can be tuned from 140 fF to 220 fF with a gate-body voltage (V_{gb}) between -1.8 V and 0 V. The measured Q-factor is 12–25 at 30 GHz and agrees well with simulations (Fig. 6.14(d)). The junction varactor can be tuned from 100 fF to 170 fF with an anode-cathode voltage (V_{ac}) between -2.5 V and 0 V (Fig. 14(c)). Its Q-factor (10–18) at 30 GHz is lower (Fig. 6.14(e)).

B. VCO

Fig. 6.15 presents the measurement setup of the PLL board. The VCO core including bias consumes 24.7 mW from a 2.3-V supply, and the buffers and dividers consume 67.5 mW from another 2.3-V supply. The logic converters and output drivers consume 15.5 mW from a 1.8-V supply. To measure the unlocked VCO, the charge pump in the HMC704 is disabled, and V_{cont} of the VCO is connected to the control voltage output of the Agilent E5052B signal source analyzer. The main output is down-converted to around 3 GHz and measured with the E5052B. The Agilent E8257D signal generator (25-GHz LO) and Marki Microwave MM1-2567L mixer contribute negligible phase noise to the measurement. The ÷16 output is measured with the E5052B without any frequency conversion. As shown in Fig. 6.16(a), the measured VCO oscillation frequency (f_{osc}) is 27.9–28.8 GHz when the control voltage is varied from 0 to 1.8 V. The output power measured at the connector varies between -11 and -8 dBm and compares well with simulation (Fig. 6.16(b)). The measured and simulated phase noise of the main output at 1-MHz offset is compared in Fig. 6.16(c). The measured phase noise is below -107.5 dBc/Hz with a minimum of -111.5 dBc/Hz over the tuning range. The phase noise variation at low V_{cont} is likely due to the noise

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contribution from the bias circuitry of the tail HBT. In hindsight, an RC filter with an off-chip capacitor (1 nF) could be included to lower the bias noise. The measured phase noise of the ÷16 output is compared with the main output with excellent agreement (Fig. 6.16(d)). This shows that the divider has little impact on phase noise, which is important in a PLL. The FoM at 1-MHz offset is above 183 dBc/Hz with a maximum of 187 dBc/Hz (Fig. 6.16(e)). The flicker corner is plotted in Fig. 6.16(f) with a minimum of 82 kHz. Finally, the phase noise and FoM versus offset frequency at f_{osc} = 28.62 GHz are plotted in Fig. 6.17(a) and 6.17(b), respectively.
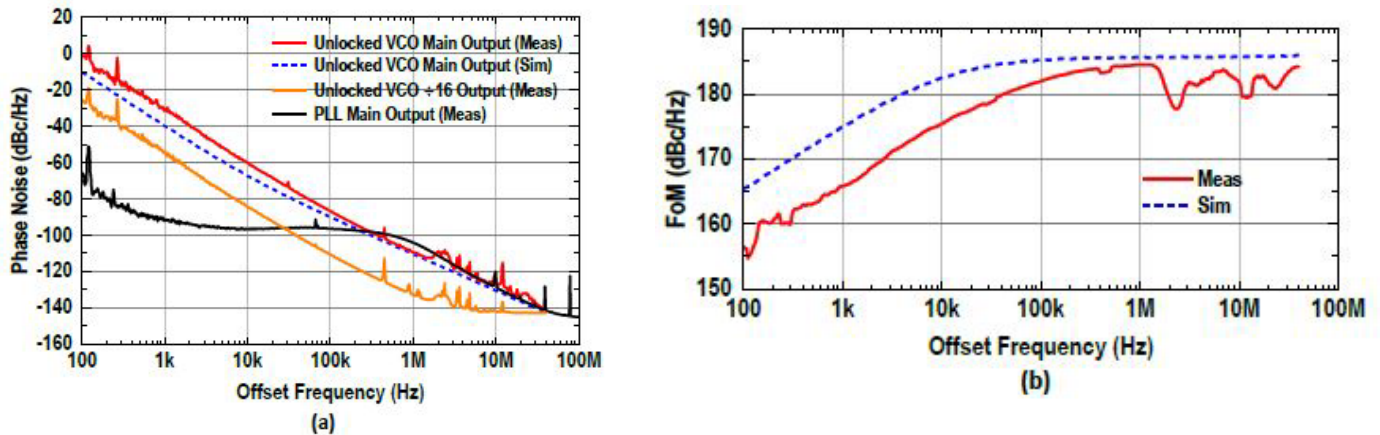
Fig. 6.17. Simulated and Measured (a) VCO and PLL Phase Noise and (b) VCO FoM Versus Offset Frequency when f_{osc} = 28.62 GHz

Class-C VCOs often employ dynamic bias to the base terminals of the active devices for robust start-up. In this design, an off-chip feedback loop can be built consisting of buffers, a peak detector, and a comparator/error amplifier with a configuration similar to [27]. However, no start-up issue is observed in simulation or measurement when a constant 1.3-V V_{bias} is applied.

C. PLL

The charge pump in the HMC704 is now enabled for PLL measurements. The main output phase noise as measured on the E5052B is shown in Fig. 6.18 when the PLL is locked at 28.62 GHz, and the same plot is overlaid with that of the unlocked VCO in Fig. 6.17(a). At 1-MHz offset, the spot phase noise is -104 dBc/Hz due to noise contribution from the other blocks. The RMS jitter integrated from 1 kHz to 10 MHz is 99 fs. The resulting contribution to the system EVM is 1.8% if used in a 28-GHz system without frequency multiplication, and 3.6%/5.4% if followed by a frequency multiplier in 60-/90-GHz systems. A drawback of this design is that the VCO tuning range cannot be fully covered as part of the tuning voltage is not supported by the CP output. The problem is alleviated when the PFD and CP are integrated on the same chip in future work.
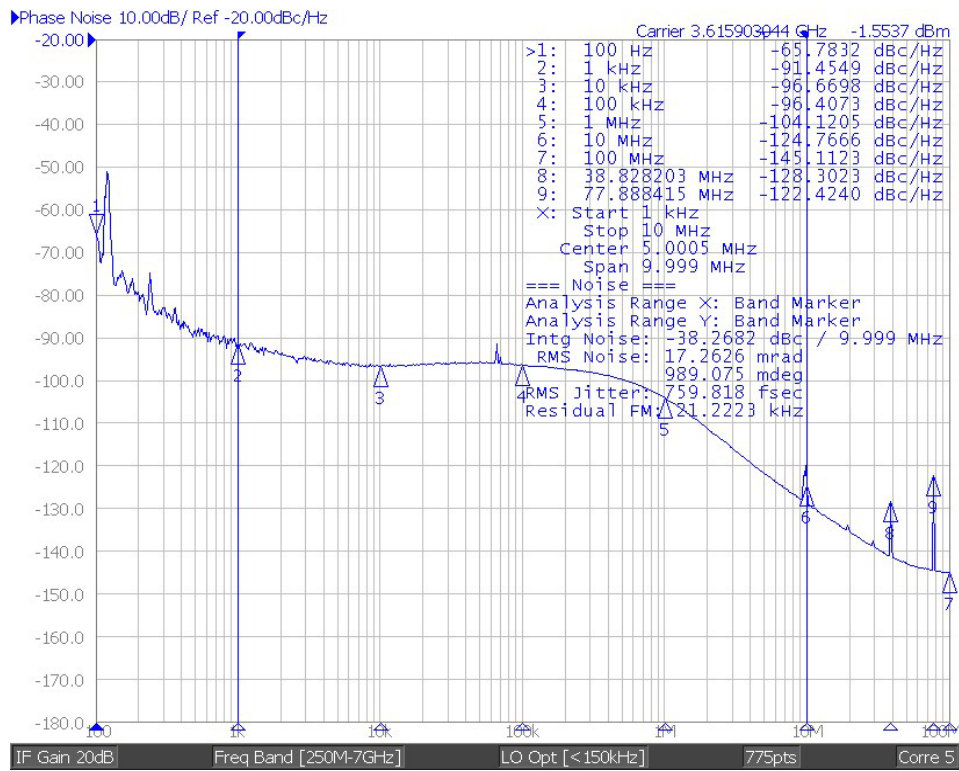
Fig. 6.18. E5052B screenshot of measured PLL main output phase noise versus offset frequency when the PLL is locked at 28.62 GHz

The main output is connected to the Keysight N9040B UXA signal analyzer to measure the close-in and full-span spectra (Fig. 6.19). The measured PD spur and its 1/8 subharmonic at 77.76 and 9.72 MHz are below -61 dBc. The leakage from the ÷16 output is -28.4 dBc due to coupling on the PCB.

(a)   (b)
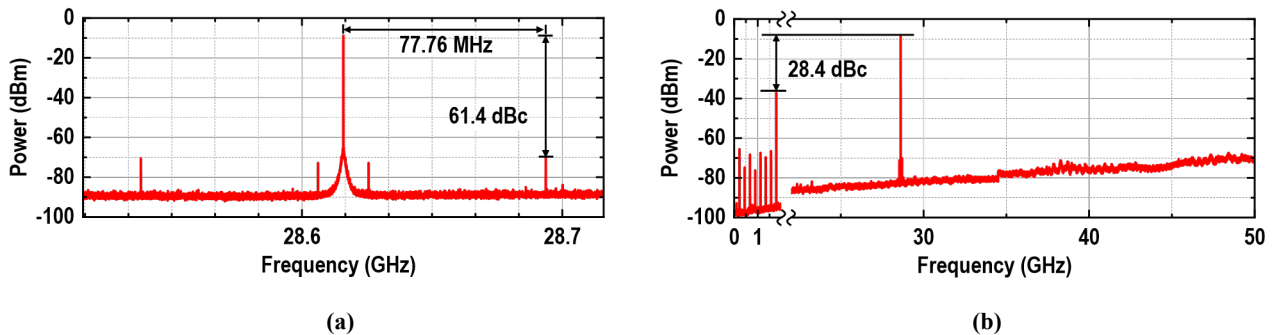
Fig. 6.19. Measured (a) Close-in and (b) Full-span Spectra of the PLL
The -28.4 dBc spur near 2 GHz is due to coupling from the strong ÷16 output on the PCB

TABLE III
COMPARISON WITH PREVIOUSLY PUBLISHED VCO

Reference	Technology	Freq. (GHz)	TR (%)	Supply Voltage (V)	DC Power (mW)	PN @ 1-MHz (dBc/Hz)	FoM[1] (dBc/Hz)	FoM$_T$[2] (dBc/Hz)	Area (mm^2)
This Work	**90-nm SiGe BiCMOS**	**27.9–28.8**	**3**	**2.3**	**24.7**	**-111.5**	**187.0**	**176.5**	**0.09**
[10]	90-nm SiGe BiCMOS	27.0–30.5	10	1.8	25.2*	-105.1	-	-	0.16
[28]	0.13-µm SiGe BiCMOS	31.8–39.6	22	2.3	30.0	-103.9	180.1	187.0	0.06
[29]	0.13-µm SiGe BiCMOS	28.0–37.8	30	1.5	10.5	-103.6	184.0	193.5	0.03
[30]	0.17-µm SiGe BiCMOS	29.6–35.5	18	-	20.0	-107.4	183.8	189.0	0.10
[31]	65-nm CMOS	25.4–29.9	16	0.5	4.0	-109.2	191.6	195.7	0.08
[32]	40-nm CMOS	23.0–29.9	26	1.0	16.1	-110.0	187.0	195.3	0.10
[16]	28-nm CMOS	27.3–31.2	14	1.0	12.0	-106.0	184	186.9	0.15
[33]	28-nm CMOS	20.7–31.8	42	0.9	5.5	-103.6	183.3	195.8	0.07

[1] $FoM = -\mathcal{L}(\Delta f) + 10\log\left(\left(\frac{f_{osc}}{\Delta f}\right)^2 \frac{1mW}{P_{DC}}\right)$ [2] $FoM_T = FoM + 20\log\left(\frac{TR}{10\%}\right)$ * Including buffer

D. Comparison

Table III compares the demonstrated VCO performance with the state-of-the-art VCOs operating at similar frequencies. The VCO presented in this paper achieves the best phase noise and an excellent FoM at 1-MHz offset, and has a very low flicker corner. The PLL is also very competitive in terms of jitter and EVM performance.

6.1.5   CONCLUSION

In this paper, a low phase noise class-C transformer VCO and an integer-N type-II charge-pump PLL are presented. A transformer tank model with all parasitic capacitance is provided and design examples are studied and compared with LC tanks. The VCO fabricated in 90-nm SiGe BiCMOS achieves a phase noise of -111.5 dBc/Hz at 1-MHz and an FoM of 187 dBc/Hz. The PLL achieves an RMS jitter of 99 fs integrated from 1 kHz to 10 MHz and is suitable for 28-/60-/90-GHz applications.

6.1.6   APPENDIX

Fig. 6.20(a) presents a VCO with a wider tuning range. The design is the same as Fig. 6.10(a) except that the 75-fF fixed capacitors on the primary and secondary sides are replaced by switched capacitor banks consisting of custom MOM capacitors. As shown in Fig. 6.20(b), the unit capacitance of the 4-bit banks is 15 fF such that there are no gaps between different capacitor bank control codes. The NMOS switches have an $R_{on}C_{off}$ of 260 fs and resistance of a 100 µm/0.16 µm (W/L) NMOS switch is 6 Ω. The source and drain terminals of the switches are biased at 1.8 V in the off state to prevent unintended turn-on. The capacitance (60–110 fF) and Q-factor (19–40) of each switched capacitor bank are shown in Fig. 6.20(c), and the entire tank has a Q of 10.5–14 (Fig. 6.20(d)).
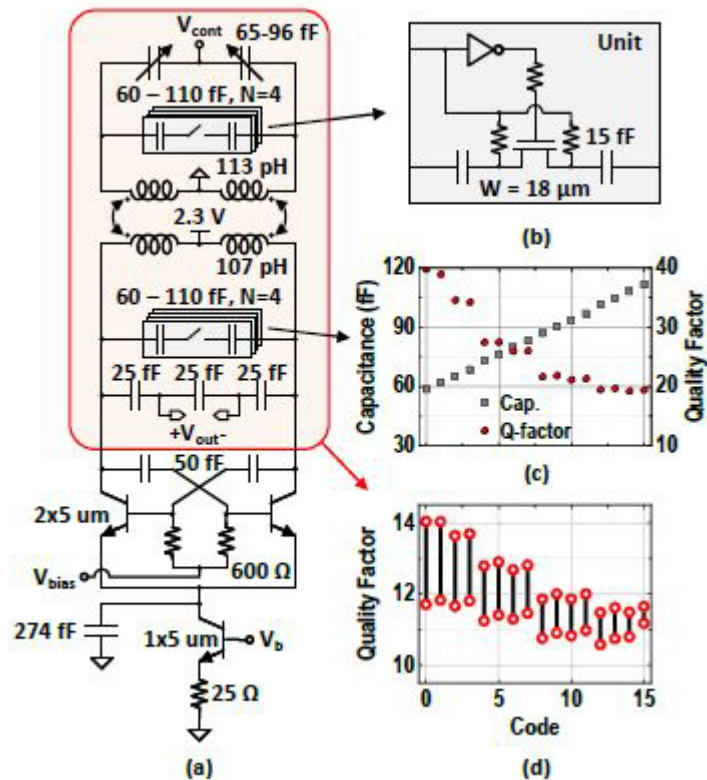
Fig. 6.20. (a) VCO schematic with switched capacitor banks. (b) Switched capacitor unit schematic. (c) Simulated capacitance and Q-factor of each bank versus code. (d) Simulated tank Q versus code.

With the capacitor banks, the tuning range is extended to 25.8–30.8 GHz (17.7%) for the entire 16 codes (Fig. 6.21(a)). f_{osc} is also shown in Fig. 6.21(b) versus control code. The phase noise at 1-MHz offset, which was lower than -110 dBc/Hz, is now between -109.3 and -106.7 dBc/Hz (Fig. 6.21(c)). The phase noise degradation at high code values is larger due to the lower Q-factor of the capacitor banks and tank Q. The corresponding FoM is 181.3–185.2 dBc/Hz (Fig. 6.21(d)), and FoM$_T$ is 186.3–190.2 dBc/Hz.
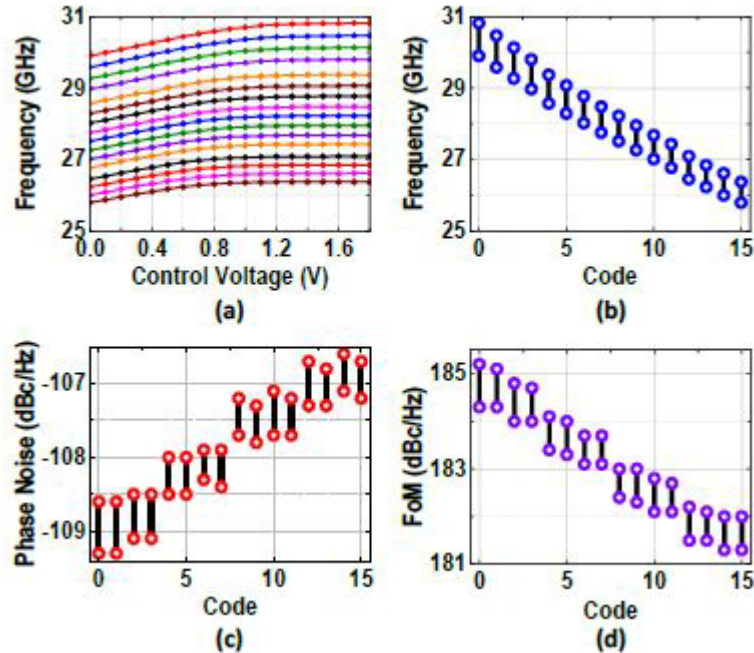
Fig. 6.21. (a) Simulated f_{osc} versus Control Voltage (b) Simulated f_{osc} versus Code (c) Simulated VCO Main Output Phase Noise at 1-MHz Offset Versus Code (d) Simulated VCO FoM at 1-MHz offset Versus Code

6.1.7 Acknowledgment

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7 ANALOG-TO-DIGITAL CONVERTER

7.1 T-MUSIC Anolog-to-Digital Converter (ADC)

Nick Mah and Ian Galton

7.1.1 Introduction

The goal of the project is to design a 100 MHz signal bandwidth (BW), 16-b ENOB ADC with a sample rate over 1 GSPS using the Global Foundries 9HP BiCMOS process. Power consumption and chip area are unconstrained. These requirements lead to jitter requirements that restricted the use of conventional delta sigma ($\Delta\Sigma$) architecture. The chosen architecture for this project is a combination of parallel delta sigma ($\Pi\Delta\Sigma$) modulation and VCO-based ADCs to attempt to relax jitter requirements while still meeting the Signal to Noise and Distortion Ratio (SNDR) target. The project was able to determine the viability of such an architecture and whether or not the solution proves to be an effective method to relax the jitter requirements in high SNDR, high bandwidth applications. The project was able to progress to schematic level simulations and did not progress to layout or tapeout. Test plans on how to implement a test board if the project were to be continued to tapeout are discussed.

Section 7.1.2 covers the jitter limitation in conventional $\Delta\Sigma$ ADCs, Section 7.1.3 shows how VCO-based ADCs are able to overcome the jitter problem while still providing quantization noise shaping, Section 7.1.4 shows how $\Pi\Delta\Sigma$ modulation is able to help meet the ENOB requirement, and Section 7.1.5 covers the overall architecture. Section 7.1.6 covers how the VCO-Based ADC concept is combined with the $\Pi\Delta\Sigma$ concept. Section 7.1.7 covers design considerations and circuit implementations of the ADC. Sections 7.1.8, 7.1.9, and 7.1.10 cover how the ADC was simulated to predict performance of the schematic model. Sections 7.1.11 and 7.1.12 cover the performance predicted from schematic and behavioral simulations and proposed floorplan and testing strategy if the project were to be continued to layout and tapeout. Finally, Section 7.1.13 summarizes the work and final results of the project.

The main concepts and solutions derived in this project are adapted from [1] and [2].

7.1.2 Challenges of Jitter in high bandwidth, high SNDR designs

A SNDR of over 98dB is required to achieve 16-b ENOB. Conventional ADCs are limited by clock jitter in high bandwidth, high SNDR systems. It can be verified that the SNR in a jitter-limited conventional non-noise shaping ADC is

$$SNR_{jitter} = -20\log_{10}(2\pi f \sigma_j) + 10\log_{10}(OSR) \tag{1}$$

where f is frequency of an input test sinusoid at the maximum analog bandwidth, σ_j is the standard deviation of the clock jitter, and OSR is the oversampling ratio. Assuming an OSR of 12 and a SNR of 99dB before accounting for clock jitter, the jitter cannot be greater than 30 fs.
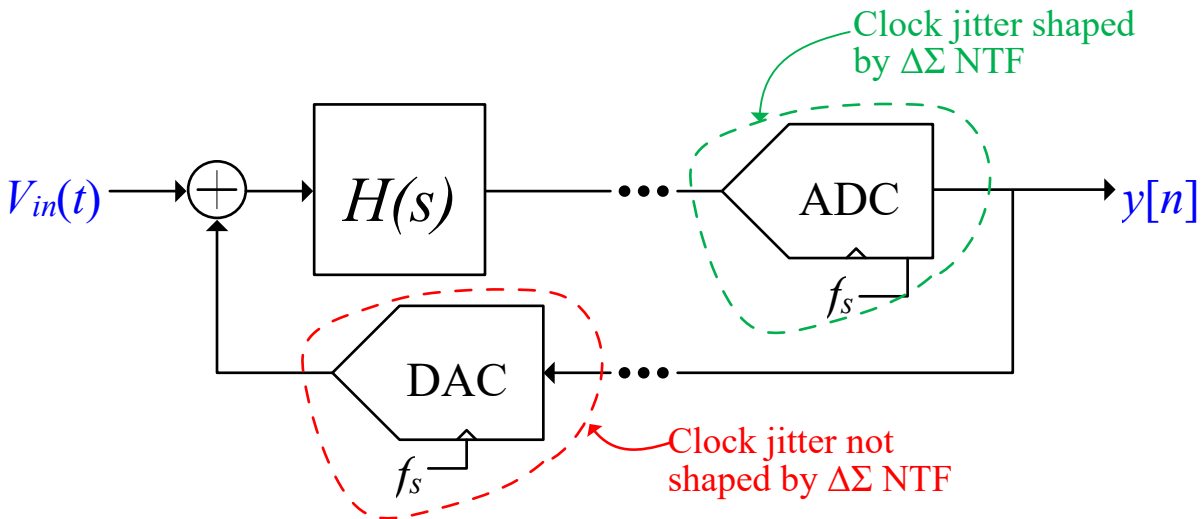

Fig. 7.1. Conventional Delta Sigma ADC Block Diagram

When considering a continuous time delta sigma modulator (CTDSM), we can see that the clock jitter on the ADC is suppressed by the loop filter, relaxing the clock jitter requirements. However, jitter induced in the feedback path is only affected by the signal transfer function (STF) and remains largely unaffected by the loop filter, limiting the acceptable DAC jitter to 30 fs.

A delta sigma ADC structure that does not require feedback DACs is an attractive solution to reduce sensitivity to clock jitter. Section 3 will provide an overview of the operation of VCO-Based ADCs and prove that this architecture is more tolerant of jitter than conventional ΔΣ ADCs.

7.1.3 VCO-Based ADCs

a) Ideal Operation

A VCO-Based ADC uses the input signal to frequency modulate a Voltage Controlled Oscillator (VCO). The VCO frequency is then quantized into a phase value and converted back to frequency

through a digital differentiation. It will be shown below how these operations are implemented and how this is equivalent to a 1st order ΔΣ modulator. A more detailed explanation of VCO-based ADCs can be found in [2].
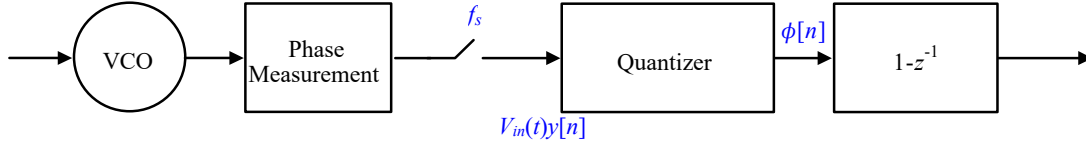

Fig. 7.2. VCO-Based ADC Block Diagram

Fig. 7.2 represents the overall block diagram of a VCO-Based ADC. The input signal, $V_{in}(t)$, modulates the frequency of a VCO such that the VCO frequency, $f_{vco}(t)$, is

$$f_{VCO}(t) = f_o + \frac{K_{VCO}}{2} V_{in}(t) \tag{2}$$

The VCO phase is then sampled to convert $f_{vco}(t)$ to the phase value, $\phi[n]$, where

$$\varphi[n] = \int_0^{nT_s} K_{VCO} V_{in}(t) dt \tag{3}$$

Provided that $0.5f_o < f_{VCO}(t) < 1.5f_o$, $\phi[n]$ is then unwrapped and differentiated to produce a sampled quantized output signal, $y[n]$, $\phi[n]$ can be represented as

$$\varphi[n] = \sum_0^{N-1} \omega[n] \tag{4}$$

where

$$\omega[n] = \int_{(n-1)T_s}^{nT_s} K_{VCO} V_{in}(\tau) d\tau \tag{5}$$

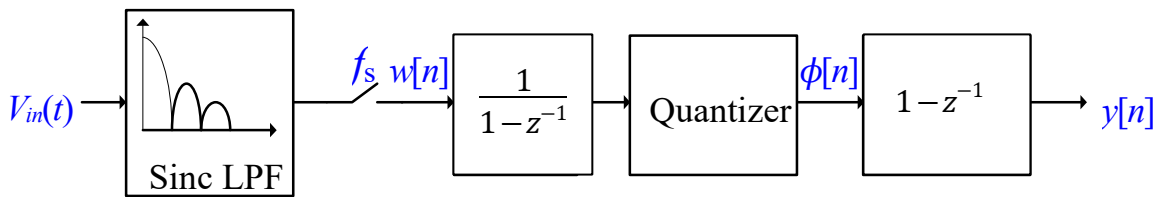It can be verified that Fig. 7.2 may be redrawn as Fig. 7.3.

Fig. 7.3. VCO-Based ADC Equivalent Block Diagram

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where the frequency response of the Sinc LPF, H(f) is

$$H(f) = K_{VCO}e^{-j\pi T_s f}\frac{\sin(\pi T_s f)}{\pi f} \tag{6}$$

As explained in [3], the transfer function of Fig. 7.3 is equivalent to that of a 1st order CTDSM because quantization noise is introduced by the quantizer to $\phi[n]$ by the differentiator and the signal path is only filtered by H(f). However, a VCO-Based ADC does not require feedback DACs to produce the 1st order noise shaping. Therefore, the architecture is only subject to clock jitter error from the phase sampler.
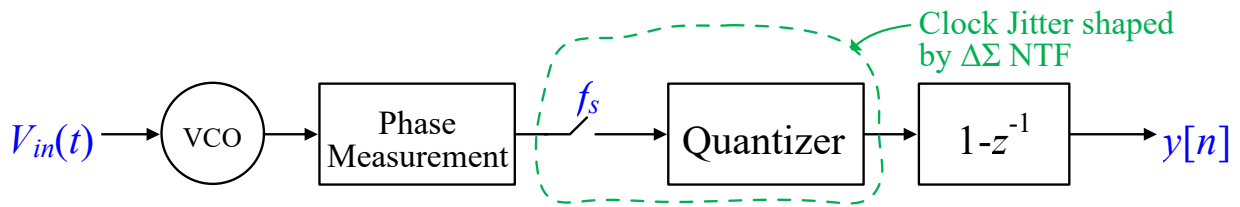

Fig. 7.4. VCO-Based ADC Block Diagram

Fig. 7.4 shows the jitter noise sources in a VCO-Based ADC. It can be shown that the SNR due to jitter is

$$SNR_{jitter} = -10 * \log_{10}\frac{4\pi^4 f^2 \sigma_j^2}{3OSR^3} \tag{7}$$

Assuming a 99dB SNDR before jitter and an OSR of 12, a VCO-Based ADC requires 205 fs of jitter or less to achieve a 98dB SNDR.

b) Ring VCO Implementation

A current-controlled ring oscillator (ICRO) that is sampled by flip flops implements the VCO and phase measurement. In a ring oscillator, only one inverter either in positive or negative transition. During this time, the input and output of one inverter will either both be high, or low. During one VCO period, each inverter will go through one positive and one negative transition. This property is used to interpret the flip flop states as a VCO phase.

The flip flops sample the state of each ring oscillator inverter output. Because each inverter can either be in positive or negative transition, there are a total of 2*Q unique states for the ring oscillator. A phase decoder maps the ring oscillator outputs to a phase number, $\phi[n]$ over the range of {0, 1, …, 2Q-1}, where Q is the number of inverters in the ring oscillator. Therefore, a ring oscillator will provide 2*Q quantization levels.
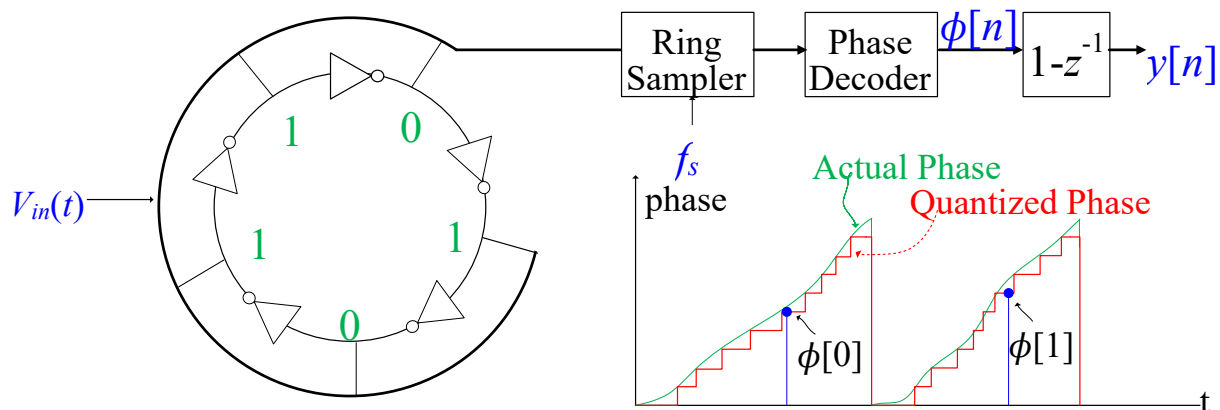
Fig. 7.5. Ring VCO and Phase-to-Digital Converter

Fig. 7.5 depicts a single-ended implementation of a 5-element VCO. The ring sampler block represents the flip flops which sample the output of each inverter, and the phase decoder block represents the digital logic which converts the ring sampler output to a phase number, ϕ[n]. As explained in [3], a pseudodifferential implementation of Fig. 7.5 is required to eliminate quantization errors related to mismatched rise/fall times.

c) Nonlinearity

In an ideal ICRO, the current controls the *delay* of each inverter element, not the frequency. The inverse relationship between delay and frequency means that even an ideal ICRO has a nonlinear transfer function. Circuit simulations of the ICRO model indicate that third order harmonic products can be as high as 46.5dBc, limiting the SNDR of the ADC well below the project specifications. As such, a nonlinearity correction implementation is required to handle such nonlinearity issues.

Nonlinearity is corrected by implementing the VCO-based ADC as a 4-path, pseudo-differential architecture with digital foreground calibration. These topics will be discussed in the following sections.

d) Calibration

A look up table (LUT) implements a nonlinearity correction block to improve SNDR. The LUT maps y[n] to a linearized output value, y_corrected[n].

The values of the LUT are determined by first measuring the nonlinear transfer function of y[n] as a function of ω[n],

$$y[n] = \alpha_o + \alpha_1 \omega[n] + \alpha_2 \omega[n]^2 + \alpha_3 \omega[n]^3 + \alpha_4 \omega[n]^4 + \alpha_5 \omega[n]^5 \qquad (8)$$

where α_n is the nth order Taylor series coefficient. Then, the inverse of (8) is solved to generate coefficients to populate the LUT. A similar method is used in [1], but only coefficients up to the 3rd order are solved. Simulations indicated that calibrating up to the 5th order is required to keep distortion products below 98dBc.
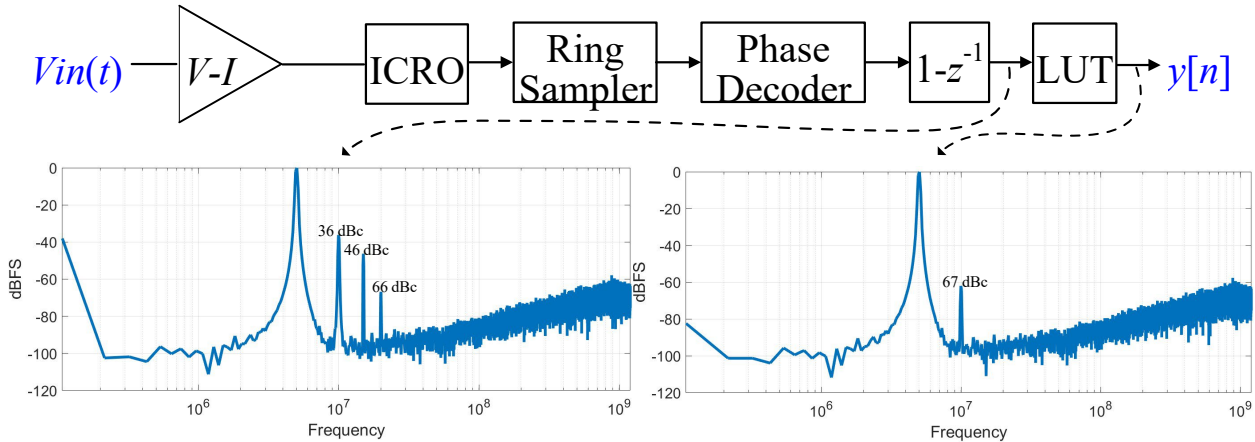

Fig. 7.6. VCO-Based ADC with LUT Calibration

The LUT is a memory-less nonlinearity correction implementation; it depends only on the current value of y[n] and cannot correct for memory distortion or nonlinear phase shifts. Solutions to overcome memory effects are presented in future sections.

e) Differential Topology

Circuit level simulation indicates that the LUT is only able to reduce the nominal second-order distortion from 44.5dBc to 68.5dBc. Even-order distortion products are addressed by combining two VCO-Based ADC paths to create a pseudo-differential signal path. This change is accommodated by using a differential V-I converter to drive the inputs of two separate ICROs. Circuit simulations indicate that second order distortion products can be corrected to over 98dBc when connected pseudo-differentially.
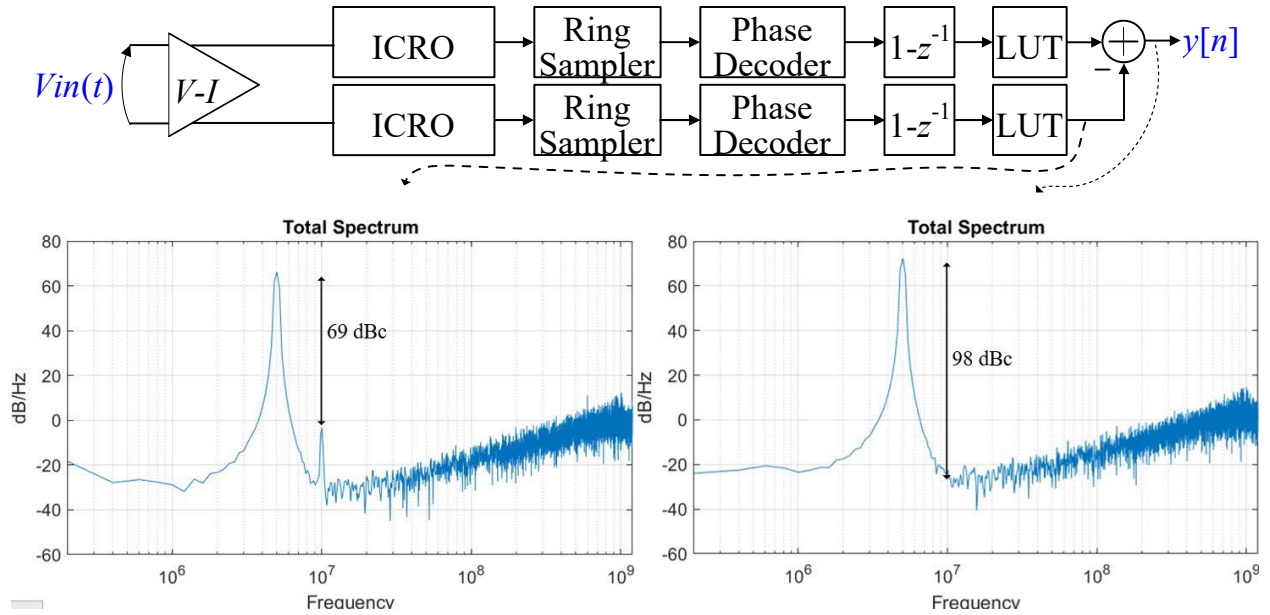
Fig. 7.7. Pseudo-Differential VCO-Based ADC

f) Self-Cancelling Dither

As identified in [3], a dither signal is required in order to keep quantization noise well behaved. However, dither signals cannot be injected after the integration in Fig. 7.3. Therefore, the same self-cancelling dither technique from [3] is used. A pseudo-differential signal path is replicated to create a 4-path VCO-Based ADC. Both pseudo-differential signal paths receive the same input signal, but oppositely signed dithers. When the paths are summed, the dither signal is suppressed. A 300 MHz dither signal that reduces the input dynamic range by 1dB is needed to keep the quantization noise well behaved.

g) Overall 4-Path Architecture

As in [3], the SQNR of the 4-path VCO-Based ADC is can be shown to be

$$SQNR = 20\log_{10}(2Q) + 30\log_{10}\frac{f_o}{2B} + 1.59 \tag{9}$$

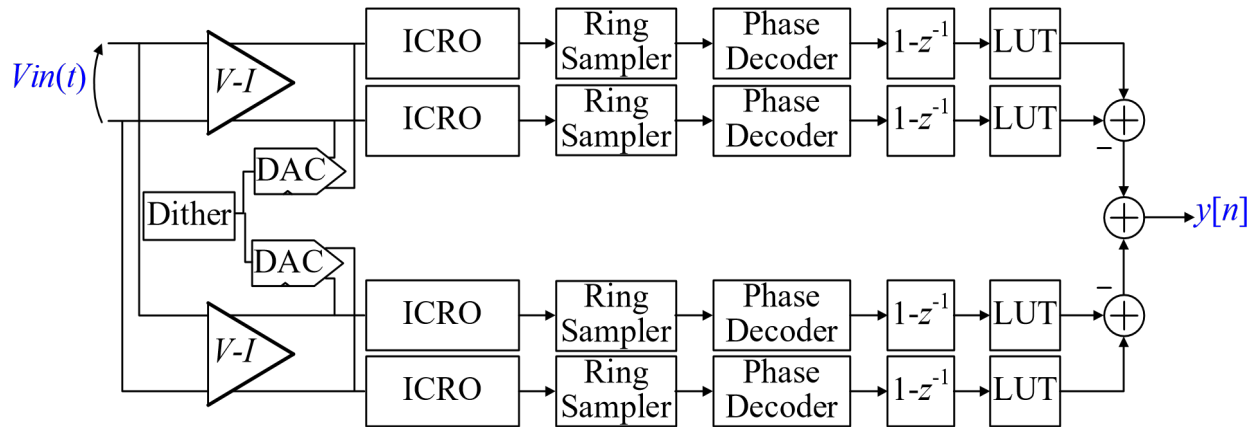where f_o is the sampling frequency.

Fig. 7.8. 4-Path VCO based ADC with Calibration

h) Details of Foreground Calibration with a 4-path VCO-Based ADC

During calibration, a full-scale input test sinusoid is applied to the VCO-Based ADC input with the look up table bypassed. Then, α_n coefficients are measured using the technique in [4] and then used to generate LUT coefficients as described in the above section.

i) 45-degree Coupled, Differential ICRO

In a VCO-Based ADC, the maximum sampling frequency and the number of quantization levels are dependent on each other. In order to increase the number of quantization levels, the number of inverters in the ICRO must be increased. However, this decreases the center frequency of the ICRO. For a given ICRO configuration, the maximum sampling frequency will be limited by the minimum inverter delay, τ.

An injection locked ring oscillator can be used to decrease τ. By locking a pair of ring oscillators in 90degree coupling, the overall f_0 of the composite ring oscillator can be doubled without reducing the number of quantization levels. This is equivalent to halving τ and is utilized in [3]. This concept is further extended to 45-degree coupling to reduced τ by 1/4 compared to a non-injection locked ICRO.

In a 45-degree ICRO, 4 ring oscillators are locked through resistors, and the outputs of all inverters are sampled at f_0. A single inverter in each of the four ring oscillators will be in transition. The phase decoder then converts the outputs of all inverters to $\phi[n]$.
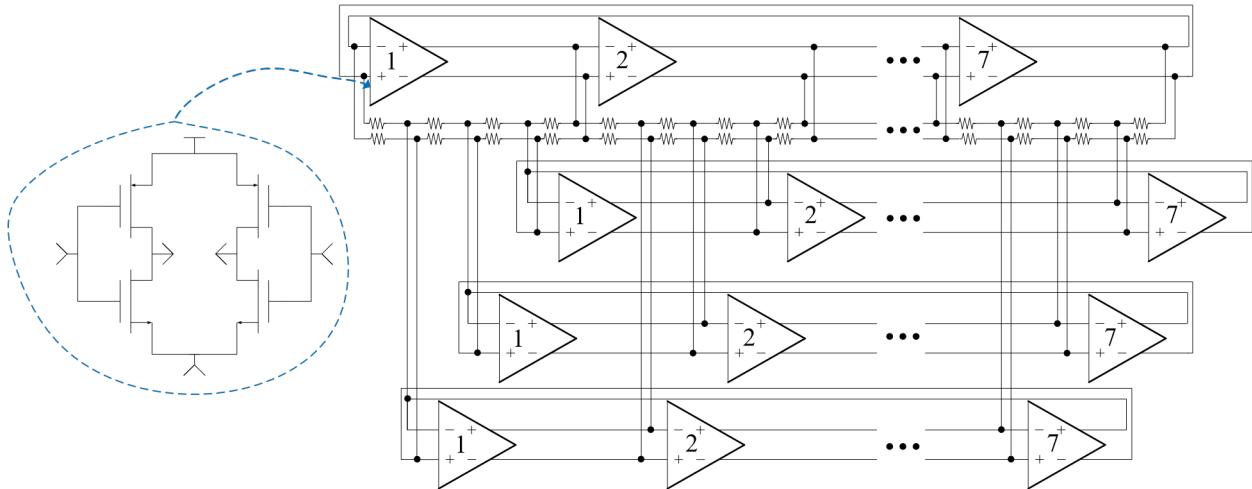
Fig. 7.9. 45-Degree Coupled, Differential ICRO

7.1.4   ΠΔΣ Modulation

The VCO-Based ADC architecture can only implement 1st order high-pass noise shaping, limiting the maximum SQNR for a given bandwidth and process. A simple solution to increase the SQNR without impacting jitter is to use a parallel combination of ADCs. Parallel ADCs do not degrade the Schreier Figure of Merit (FOM) because the SNDR and power consumption both increase by 3dB for each doubling of parallel ADCs. Therefore, the ratio of power to SNDR is maintained.

Circuit simulations indicate that a VCO-Based ADC in the 9HP process can achieve 68.9dB SQNR. Over 1000 parallel ADCs would be required to increase the SQNR to the 103dB target. The complexity and extra digital power required for this design makes such a solution impractical.

One solution to efficiently increase the SQNR is to use a parallel ΔΣ (ΠΔΣ) architecture. In a ΠΔΣ, M-parallel ADCs are employed. However, each ADC is first multiplied by unique ±1 sequences from a Hadamard matrix. The ADC outputs are then lowpass filtered and down-sampled. Finally, the ADC outputs are demodulated by a delayed version of the Hadamard sequence and summed together. The Hadamard demodulation removes the lowpass filtering of the input signal while leaving the quantization noise unaffected [5].
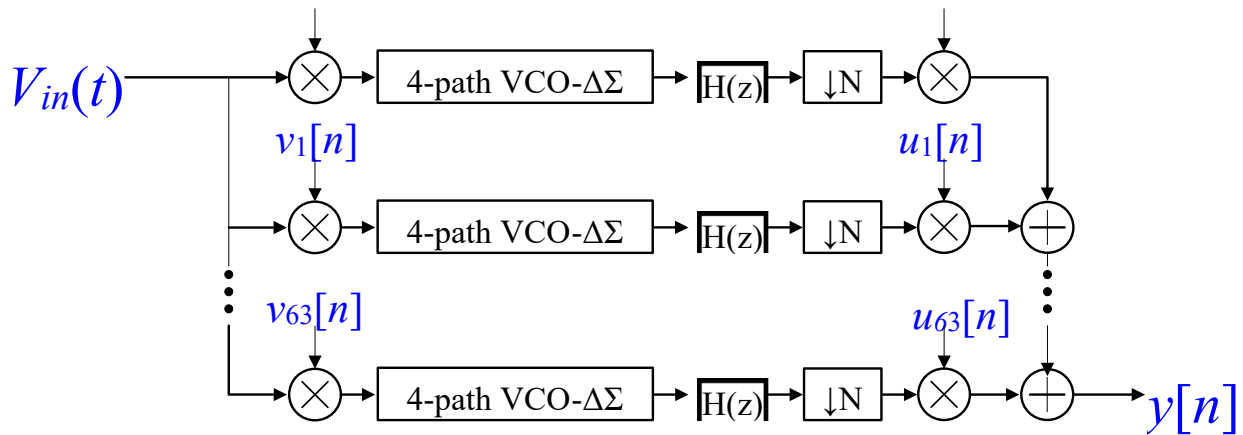
Fig. 7.10. ΠΔΣ ADC Block Diagram

ΠΔΣ modulation is equivalent to increasing the SQNR by 6dB when using 4-path VCO-Based ADCs. Using ΠΔΣ modulation, only 64 ADC channels are needed to meet the same SQNR target.

a) Principle of Operation

The following explanation can be found in complete detail in [5]. Consider a conventional ΔΣ ADC where the delta sigma modulator can be approximated as having delay-only STF, and a high pass shaped noise transfer function (NTF). Each of the ΔΣ ADC inputs are modulated by a Hadamard sequence from a unique row of a Hadamard matrix. Hadamard matrices exist for M = 1, 2, and every multiple of 4 up to 428 [5]. Hadamard sequences also exist for higher values of M. The Hadamard modulated sequences are then quantized, filtered, down-sampled, and then demodulated and recombined.

As seen in Fig. 7.10 and explained in [5], input signals that are Hadamard modulated have the filtering removed after they are demodulated. However, uncorrelated noise sources do **not** have the filtering removed. This allows the low pass filter to attenuate quantization noise within the signal band without affecting the STF. It is shown in [1] that oversampling does not impact the operation of ΠΔΣ modulation, provided the Hadamard modulation occurs at the down-sampling frequency.
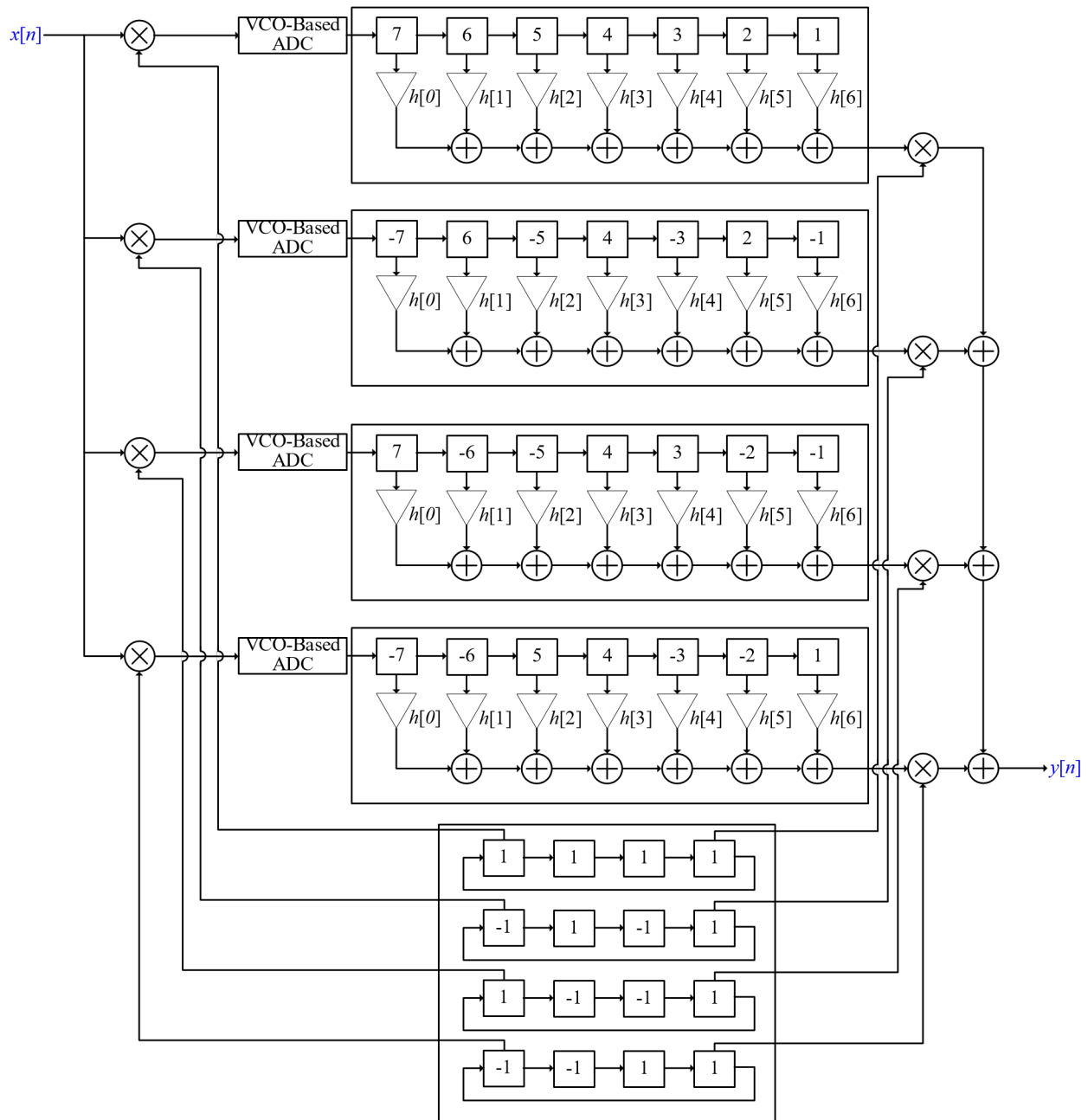
Fig. 7.11. Example of a 4-Channel ΠΔΣ [5]

Fig. 7.11 depicts a 4-channel ΠΔΣ ADC. The output of each VCO-Based ADC feeds into a 7-element FIR filter. It can be verified that only the sample at the 4th filter tap is present at y[n].

Ideally, the ΠΔΣ architecture allows each of the M parallel channels to operate at 1/M of the signal bandwidth, effectively increasing the OSR by M and increasing the total noise power by M. Signal power is unaffected by M. For high-pass shaped noise, there is a P increase in bits for each doubling of channels, where P is the order of the noise shaping. In a conventional ADC, doubling the OSR would result in a P+0.5 bit increase in resolution. The discrepancy between the

ΠΔΣ and conventional delta sigma structure can be explained by the M increase in uncorrelated quantization noise generated by each Hadamard channel. In the case of white noise, the increase in OSR is counteracted by the M increase in ADC channels.

   b)   Thermal Noise Performance

Thermal noise it is not attenuated by the ΠΔΣ structure because it is white. Therefore, the integrated thermal noise power of each ΠΔΣ channel must be 99dB below the full-scale signal power.

A simple solution is to increase the size of the VCO-Based ADC analog circuitry to reduce thermal noise power. However, the solution would require over 200 W of power. A more power efficient method would be to remove ΠΔΣ modulation and only use parallel ADCs, however, this is undesirable as explained earlier. The chosen solution is to include both parallel and ΠΔΣ channels to optimize for power consumption.

The reason why using only ΠΔΣ channels is power inefficient can be understood by considering the Schreier FOM

$$FOM = SNDR + 10 * \log_{10}\left(\frac{BW}{P_{cons}}\right) \qquad (10)$$

Where P_{cons} is total power consumed, and BW is the analog bandwidth. Since SNDR and BW are fixed targets by the project, the design configuration that achieves the highest FOM will have the lowest power consumption.

When parallel combining ADCs, total power consumption of each VCO-Based ADC will double. However, the SNDR will also improve by 3dB, causing the FOM to remain constant. When adding ΠΔΣ channels, only the SQNR increases by 6dB and the power consumption doubles. In thermal noise limited designs, the FOM will decrease by 3dB.

Changing the size of the analog section only affects the analog power consumption. When analog power consumption is below or comparable to digital power consumption, increasing the size of analog transistors will increase the FOM. Therefore, there exists an analog power consumption value that maximizes the FOM. This implies that the optimal configuration to reach the target SNDR is a combination of both parallel and ΠΔΣ channels. Fig. 7.12 plots the FOM and power consumption of a ΠΔΣ ADC as the number of Hadamard channels is varied for the final expected performance. Parallel ADCs and VCO-Based ADC size are chosen to maintain a constant target SNDR for all Hadamard channel sizes.
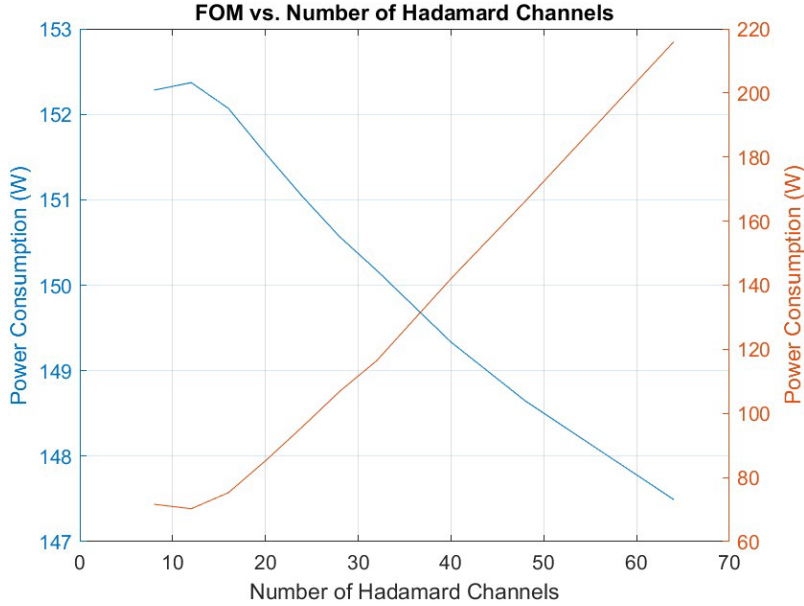
FOM vs. Number of Hadamard Channels

Fig. 7.12. Schreier FOM vs. Parallel and Hadamard ADC Combinations

7.1.5 Overall Architecture

The design strategy is to create a high FOM VCO-Based ADC, then combine parallel and Hadamard modulated channels until acceptable performance is achieved. The overall SNR and SQNR scaling are as follows

$$SQNR = 20\log_{10}(2Q) + 30\log_{10}\left(\frac{f_o}{2B}\right) + 20\log_{10}(M) + 10\log_{10}(P) + 1.59$$

$$SNR = SNR_{4-pathVCOADC} + \log_{10}P \tag{11}$$

where P is the number of parallel channels, M is the number of $\Pi\Delta\Sigma$ channels, SNR is the SNR due to thermal noise alone, and SNR_4-path VCO ADC is the SNR of a 4-path VCO-Based ADC. The overall structure will be referred to as the VCO-Based $\Pi\Delta\Sigma$ ADC.
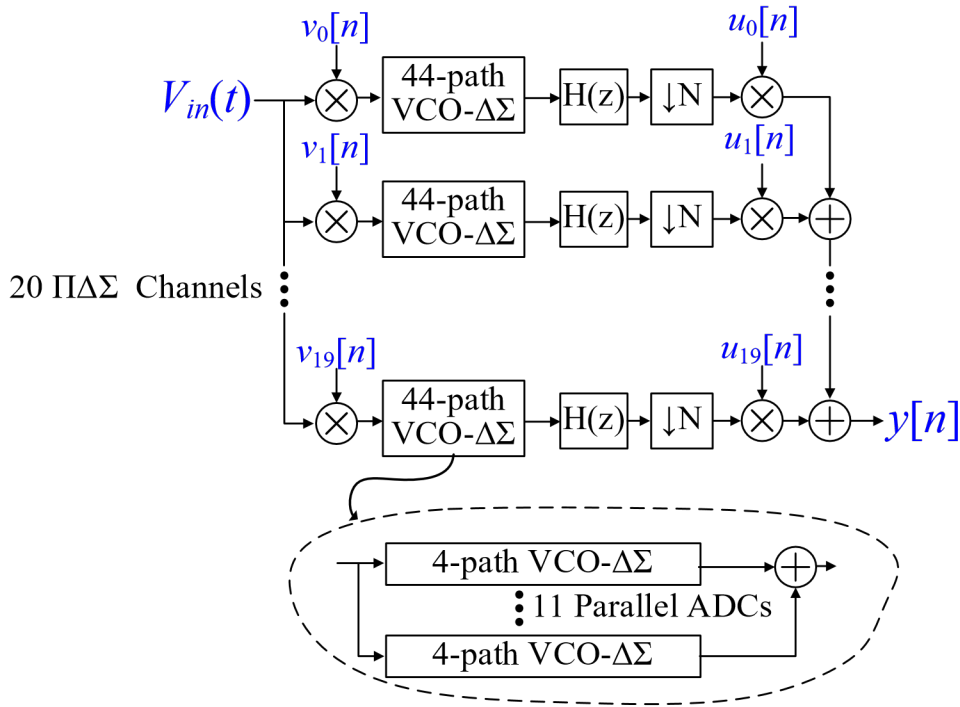
Fig. 7.13. Overall System Block Diagram

7.1.6 Integration of Parallel VCO-Based ADCs and Hadamard Modulation

Swapper cells swap the differential signal input to produce the ± multiplication required for ΠΔΣ modulation. However, swapping in the voltage domain is difficult at high bandwidths. Implementing the swapper cells after the V-I converter to swap current signals resolves the difficulty by operating in the current domain. Circuit simulations indicate that calibration is not significantly impacted by swapping after the V-I converter.

The parallel ICROs are combined before the LUT to reduce chip area. Additionally foreground calibration is applied to the sum of parallel inputs to simplify the calibration process.

Dither DACs between parallel ADCs require separate current steering DACs but can receive the same dither sequence. Circuit simulations indicate that the thermal noise is sufficient to keep the quantization noise between dither DACs uncorrelated and well-behaved.
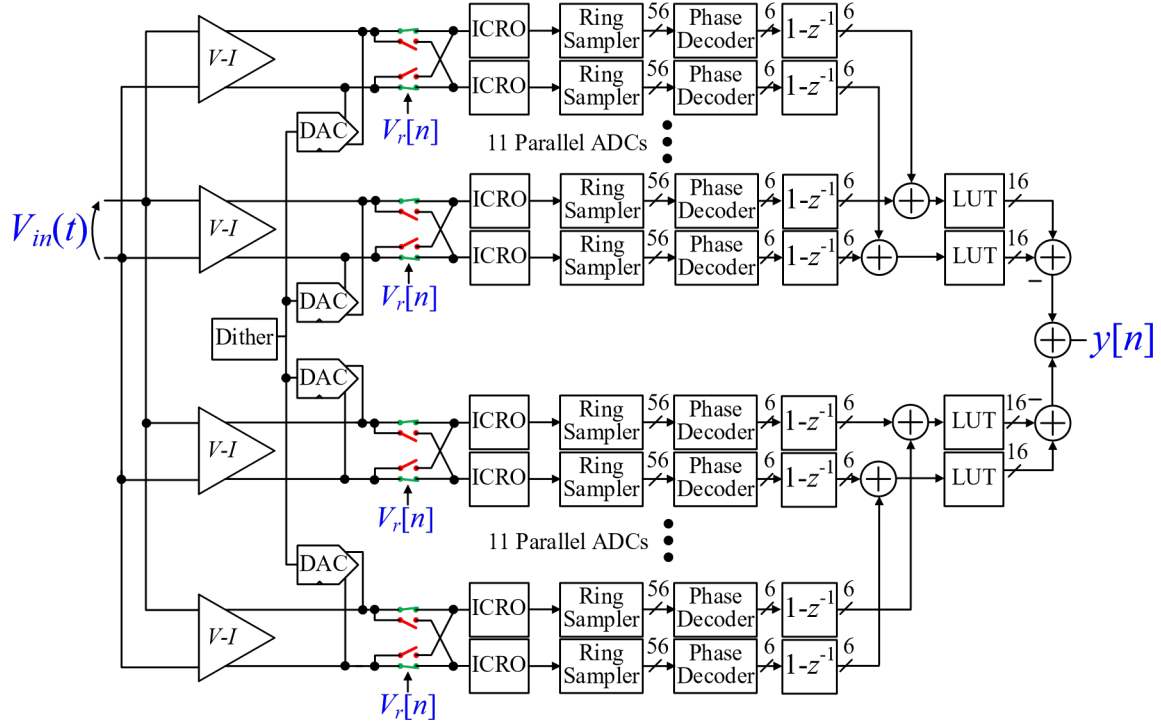
Fig. 7.14. Parallel VCO-Based ADC Block Diagram

a) Jitter

There are two effects of jitter to consider in a VCO ΠΔΣ ADC: clock jitter effects in the channel ADC, and clock jitter effects due to analog Hadamard modulation. We will assume that jitter at any clock instance n, δ[n], is the same for every ΠΔΣ channel.

i) Channel Sampling Jitter

For a sinusoidal input signal and assuming that the jitter only affects the sampling instant of the ADC, we can model the jitter before the quantizer as

$$e_{jitter}^i[n] \approx \delta_j[n] * \left(\int_0^{nT_s} v^i(t)x(t)dt - \int_0^{(n-1)T_s} v^i(t)x(t)dt \right) = \delta_j[n]v^i[n]\omega[n] \qquad (12)$$

where e_{jitter}^i is the additive jitter error of the ith ΠΔΣ channel, δ_j is the time jitter at sample n, and v^i is the analog Hadamard swapping sequence of the ith ΠΔΣ channel. The total jitter error is attenuated by the STF of the Hadamard structure and not the NTF. This is because the jitter is correlated and each jitter error sequence is swapped by the analog swapping sequence.

ii) Analog Hadamard Modulation Jitter

Another effect of Hadamard modulation must be captured: clock jitter induces an amount of error in the variation in analog Hadamard modulation durations that is captured by the sinc low pass filter.

Unfortunately, the Hadamard modulation jitter error is not subject to the NTF of the Hadamard modulation scheme, nor the VCO-Based ADC. This limits the maximum jitter tolerance to 16fs. Intuitively, one can treat the jitter in switching as occurring before the integrator. Therefore, the jitter is subject to the STF instead of the NTF. The jitter tolerance is lower than a conventional delta sigma ADC because the swapping sequence modulates the input signal at Fs/OSR, which is twice the analog signal bandwidth. Additionally, Hadamard modulation jitter error is independent of input signal because it is dependent on the swapping frequency, which is always Fs/OSR.

7.1.7   Circuit Design of VCO-Based ADC

a)   V-I Converter

The purpose of the V-I converter is to translate the input voltage signal to the current domain to facilitate current swapping for Hadamard modulation and dither signals through current steering DACs. An emitter degenerated architecture was chosen as the V-I converter. An alternative option involving op amps is possible, but the simpler emitter degenerated architecture was chosen to reduce input referred noise [2].

Both pseudo-differential and fully differential pair configurations were considered. Both designs use resistive degeneration to increase the input signal swing and relax the calibration requirements for the LUT. The pseudo-differential pair has more available headroom. However, the 2nd order distortion in a pseudo-differential architecture was too high after calibration to meet the SNDR target. Due to this, a fully differential architecture is used in this design.
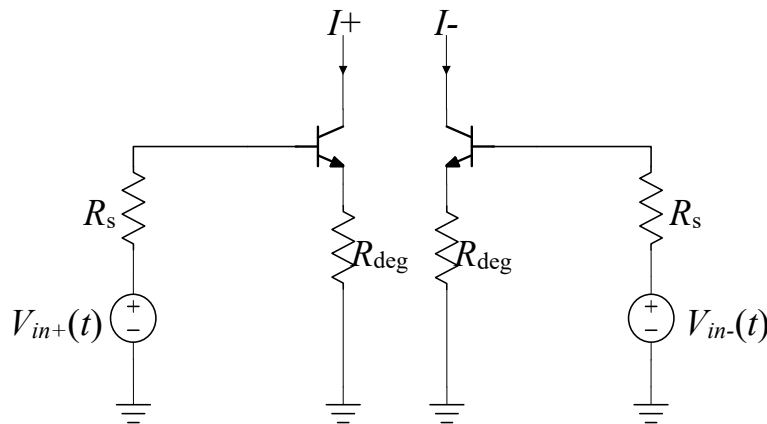

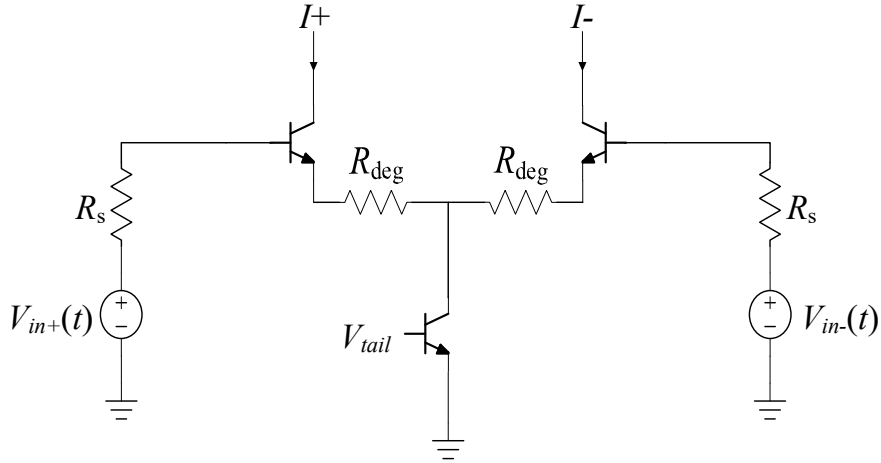**Fig. 7.15. Pseudo-Differential V-I Converter**

Fig. 7.16. Fully-Differential V-I Converter

b) Swapper Cell

BJT swapper cells implement the ±1 multiplication required for Hadamard modulation by swapping the V-I converter output current between two ICROs. The swapper cells are implemented as current steering cascode transistors. BJT transistors were chosen to take advantage of the faster switching speed compared to an equivalent CMOS structure. A swapper cell driver was developed to drive the bases of the swapper cell, but the design could not meet the required swing of 200mV peak to peak. If the swing at the swapper cell base is too low, then swapping will not occur properly. If the swing at the swapper cell bases is too high, then the linearity will degrade.
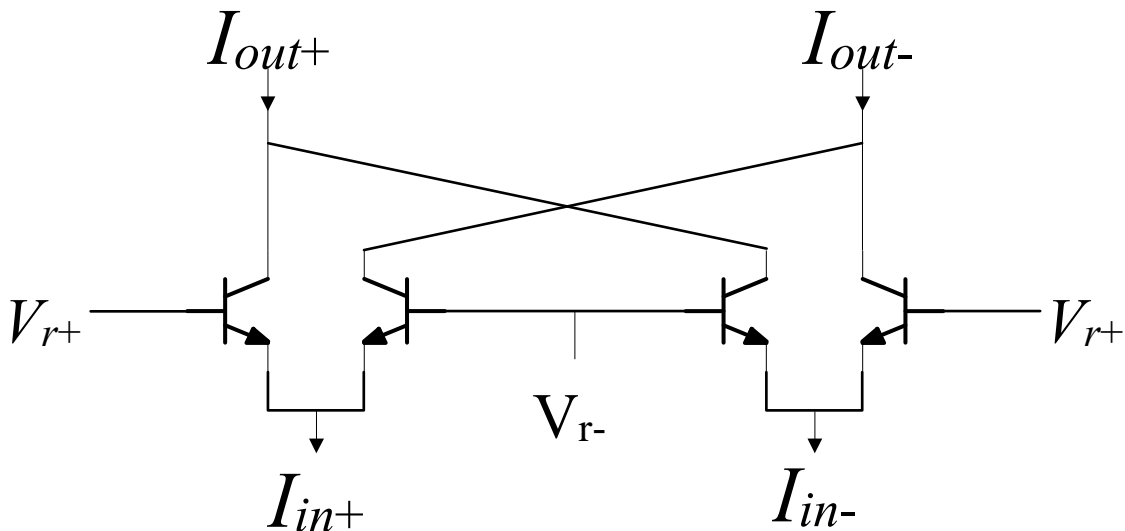

Fig. 7.17. Swapper Cell

c) ICRO

Two main types of ring oscillator designs were considered during the design: a BJT-based oscillator, and a CMOS-based oscillator. Both designs use the pseudo-differential implementation but implement different inverter designs.

i) BJT Ring Oscillator

In the BJT ring oscillator, each inverter is composed of a NPN transistor and a resistor forming a CML inverter. Circuit simulations indicated that a CML oscillator was not able to simultaneously meet the
$0.5fs<f<1.5fs$ frequency swing and phase noise requirements at a reasonable power consumption limit.
The ring oscillator was then modified to include a Schottky diode to increase the frequency swing range. The Schottky diode limits the maximum voltage swing of each inverter to the forward voltage. By limiting the maximum swing, the ring oscillator is allowed to increase the current swing before the BJT enters saturation and leaves CML operation. However, the phase noise was not able to meet design requirements.
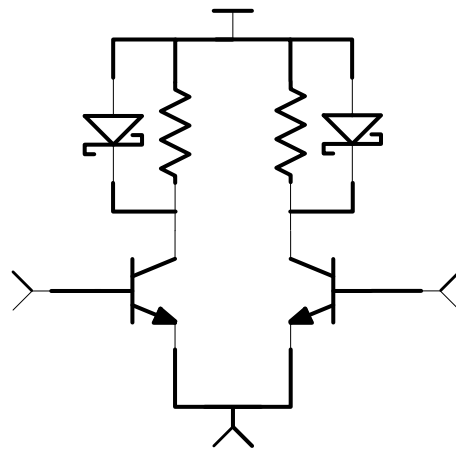

Fig. 7.18. Inverter for Diode-Limited BJT Ring Oscillator

A third design involving diode-only loads was considered. However, a suitable design was not found that produced acceptable phase noise specifications. Moreover, it was found that higher oscillator speeds may be limited by the sampling rate of flip flops in the process, limiting the viability of higher frequency oscillator topologies.

ii) CMOS Ring Oscillator

The CMOS ring oscillator is able to meet the phase noise requirements at acceptable power consumption levels, but is limited to a 2.4 GHz center frequency, while the BJT ring oscillator is able to operate at a 4 GHz center frequency. However, simulation of the phase sampler indicates that surpassing a 2.4 GHz sampling frequency is difficult in the process.
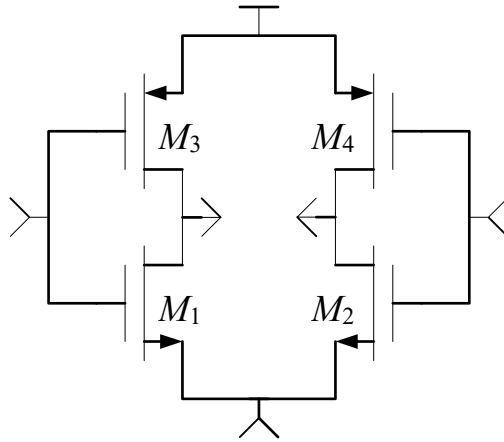
Fig. 7.19. CMOS Ring Oscillator

d) I-V Converter

In [3] and [2], the ring oscillators were implemented as current controlled ring oscillators and driven by a current source. Full circuit simulation of the ICRO indicates that capacitance at the source-coupled node presented enough memory distortion to limit the bandwidth of the VCO-Based ADC to 5 MHz by introducing nonlinear phase shift. One solution is to implement a memory calibration system, where the LUT depends on both current and previous samples. However, such solutions require significant chip area, power consumption, and development time. Instead, using a I-V converter to present a low impedance source to the ICRO in order to reduce the effects of capacitance was chosen. The I-V converter is comprised of a load resistor, common collector buffer, and a bias transistor.
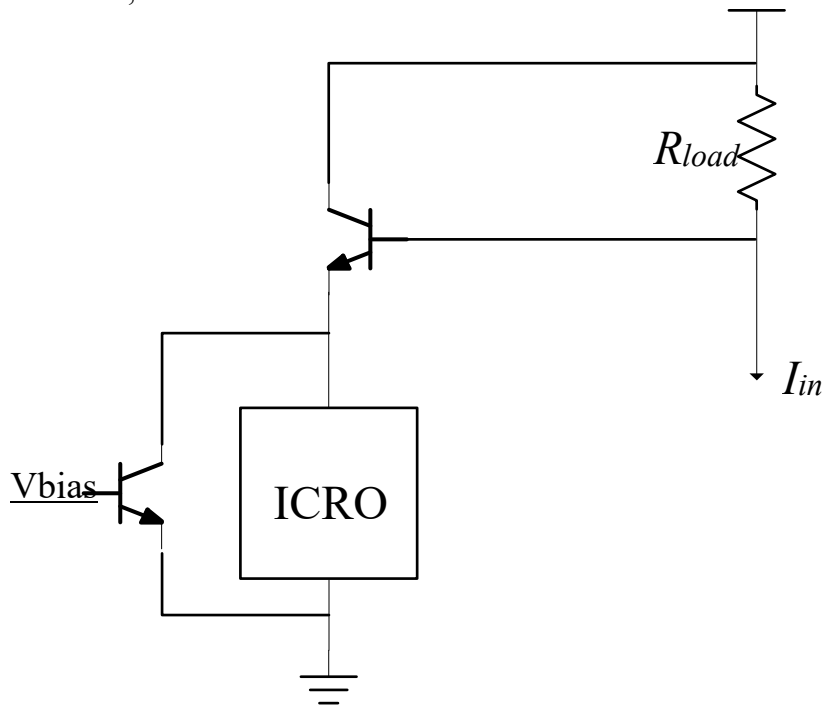

Fig. 7.20. I-V Converter Implementation

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7.1.8 Overall Analog VCO-Based ADC Architecture

Fig. 7.21 depicts 2 paths of the VCO-Based ADC analog section with the I-V bias transistors removed. The main differences compared to [2] is the fully differential V-I converter, swapper cells for Hadamard modulation, and inclusion of I-V converters. A full circuit model of the 4-path VCO-Based ADC would include another copy of the 2 paths, but with opposite dither connections.
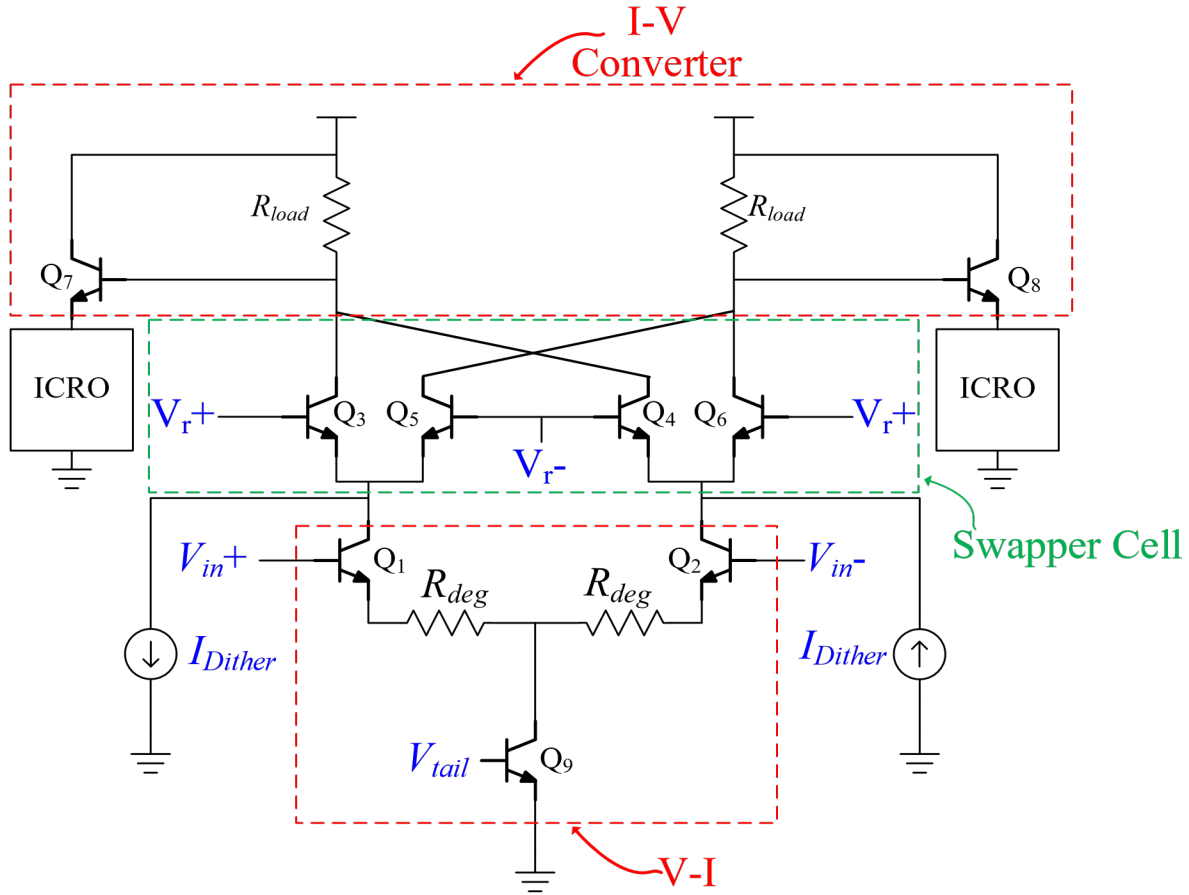

Fig. 7.21. VCO-ADC Block Diagram (2-Path)

b) Phase Sampler

The phase sampler reads the differential output of the ring oscillator to determine the phase.

i) Standard Cell Flip Flop

The standard cell flip flop was originally chosen to sample the phase. However, it was found that the standard cell flip flop setup and hold times were too long to accurately sample the ring oscillator phase at the 2.4 GHz operating frequency.

ii) StrongARM Latch Sense Amplifier

Instead, a StrongARM latch, combined with a SR latch, is used as a flip flop for faster sampling of the ring oscillator phase.
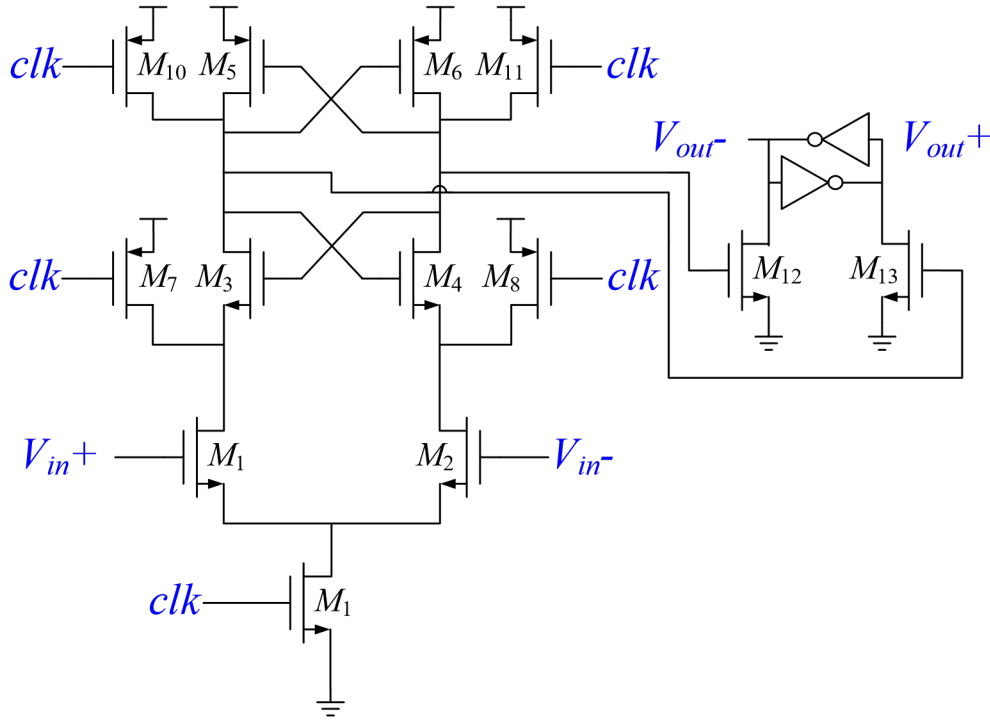

Fig. 7.22. StrongARM Latch

c) Digital Blocks

After sampling the ring oscillator outputs, the phase of each 45-degree locked ring oscillator is decoded into a single-phase value in a one-hot form. Next, the one-hot phase value is converted to binary and the $1-z^{-1}$ is applied. Because the design samples at the center frequency, phase must be unwrapped during the derivative to prevent the strong nonlinearity associated with phase wrapping. The phase unwrapping is the same logic as in [3].

$$y[n] = \begin{cases} \emptyset[n] - \emptyset[n-1] \; if -28 \le \emptyset[n] - \emptyset[n-1] \le 27 \\ \emptyset[n] - \emptyset[n-1] \; if \; \emptyset[n] - \emptyset[n-1] \ge 28 \\ \emptyset[n] - \emptyset[n-1] \; else \end{cases} \qquad (13)$$

The values from each of the parallel ADCs are added together and fed to a lookup table to linearize the final VCO-ADC output. The current LUT implementation does not account for swapping inputs. As a result, mismatches before the ring oscillators could impact the calibration performance below the requirements.
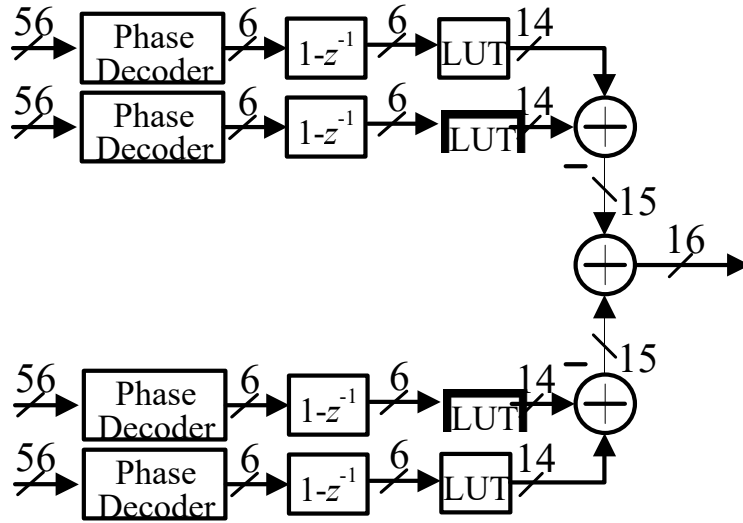
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Fig. 7.23. VCO-Based ADC Digital Logic Post Phase Sampler
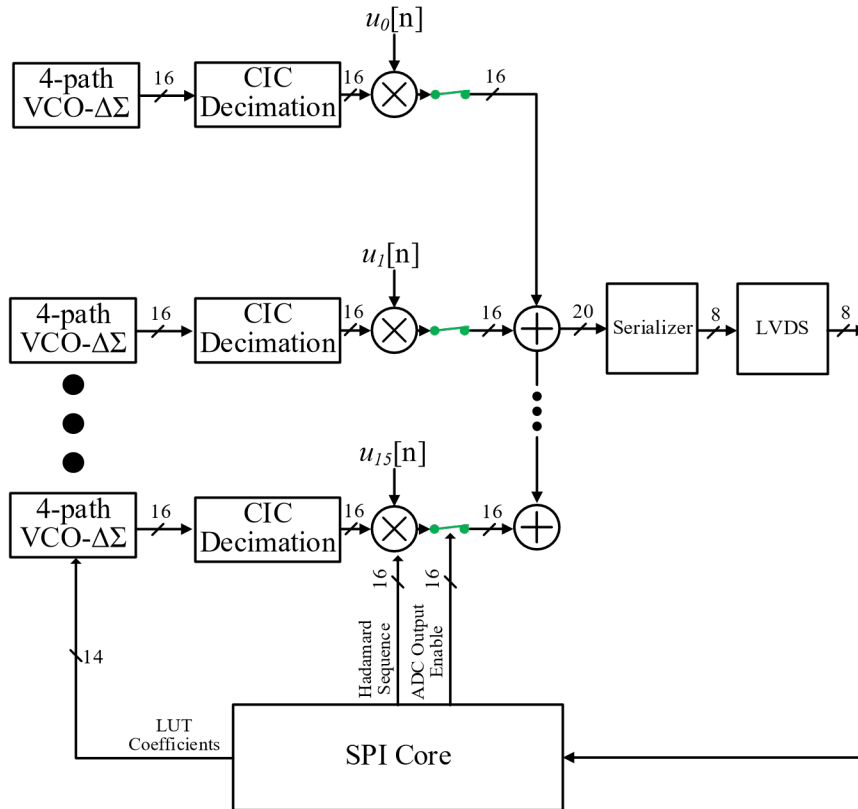
Fig. 7.24. Digital Logic Post-VCO-Based ADC

The phase decoder, $1\text{-}z^{-1}$, LUT, and CIC decimator were implemented in Verilog and tested with standard cells. Remaining blocks are left for future work. The performance of the digital blocks in the slow corner is currently unable to meet timing requirements. It is recommended that the existing logic written should be implemented as a custom circuit to meet timing requirements.

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d)   Dither DACs

The dither DAC architecture in [2] is used in this project. The self-cancelling dither technique relies on the matching accuracy of the differential signal paths. In order to improve the matching accuracy of the dither outputs, the outputs of the dither DACs are swapped at twice the dither DAC rate. This swapping provides first order high-pass shaping to the dither mismatch error.

Additionally, a dual return-to-zero architecture is implemented in the current steering DACs to avoid nonlinear inter-symbol interference that is associated with non-return-to-zero current steering DACs. This architecture employs two RZ DACs that are offset by half of the dither period to have an overall effect equivalent to a NRZ DAC.
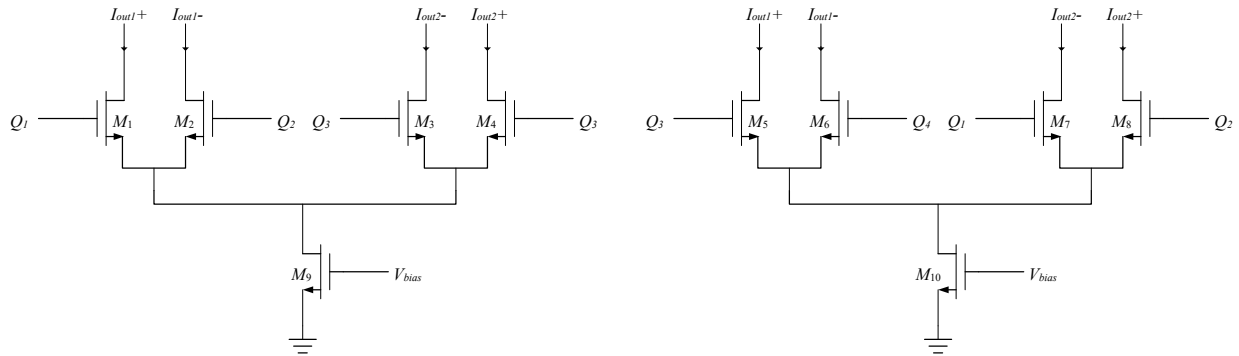

Fig. 7.25. Current Steering DAC

e)   Clock Divider

A clock divider is required to create the down-sampled control signals for Hadamard modulation and CIC decimation. The clock divider module was simulated at a block level, but not integrated into 4-path VCO-Based ADC simulations due to time constraints.
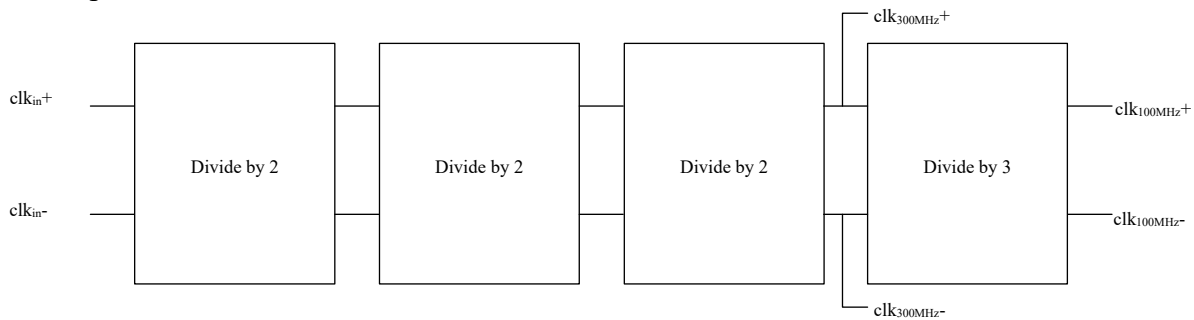
Fig. 7.26. Clock Divider Block Diagram

7.1.9   Linearity Analysis

Time domain and periodic steady state (PSS) analysis is used to characterize the linearity of a VCOBased ADC. Behavioral simulation of the full system architecture indicates that Hadamard modulation does not impact the SFDR of the ADC. Therefore, we are able to measure the SFDR of a single 4-path VCO-Based ADC to determine the impact of linearity of the overall system.

In time domain analysis, a transient simulation is run with a full-scale input sinusoid applied to a circuit model of a 4-path VCO-Based ADC without the phase decoder and remaining digital circuitry. The ICRO output data is captured and processed in a MATLAB script that implements digital logic. A periodogram of the output data is captured and the SFDR is analyzed.

In the PSS analysis, a sinusoidal input is applied to 2-path VCO-Based ADC model consisting of the V-I, swapper cell and I-V converter. The I-V converter then connects to a behavioral model of the ICRO. PSS analysis is used to measure the phase and magnitude response of the VCO-Based ADC model. The linearity and calibration performance are then estimated through the phase and magnitude response. A behavioral model of the ICRO is required because PSS is unable to resolve simulation of a free-running oscillator with a sinusoidal input and Hadamard modulation. A 4-path VCO-Based ADC is not required as dither is not required for the simulation.

PSS analysis is used primarily to reduce required simulation time. A transient simulation of one 4-path VCO-Based ADC can take upwards of 12 hours while a PSS simulation requires up to 10 minutes of simulation time.

7.1.10 Noise Analysis

Thermal noise analysis presents a unique problem because the thermal noise requirement of a single VCO-Based ADC is stricter than the quantization noise requirement. Therefore, the noise floor of a single VCO-Based ADC will only show quantization noise. Additionally, full circuit simulation of the VCO-Based $\Pi\Delta\Sigma$ ADC would require excessively high simulation resources and time. Thermal noise analysis was performed through use of PSS analysis and time domain analysis with quantization noise interpolation.

   a) PSS Analysis

The PSS analysis is split into two sections: ICRO phase noise, and the remaining analog circuitry. Noise from the phase sampler is subject to the NTF and is not included in this analysis.

To analyze the phase noise of the ICRO, a circuit model of the ICRO is simulated with PSS/Pnoise analysis as a free running oscillator at the center frequency. It can be shown that the phase noise of a ICRO can be input referred with the model and equation below:
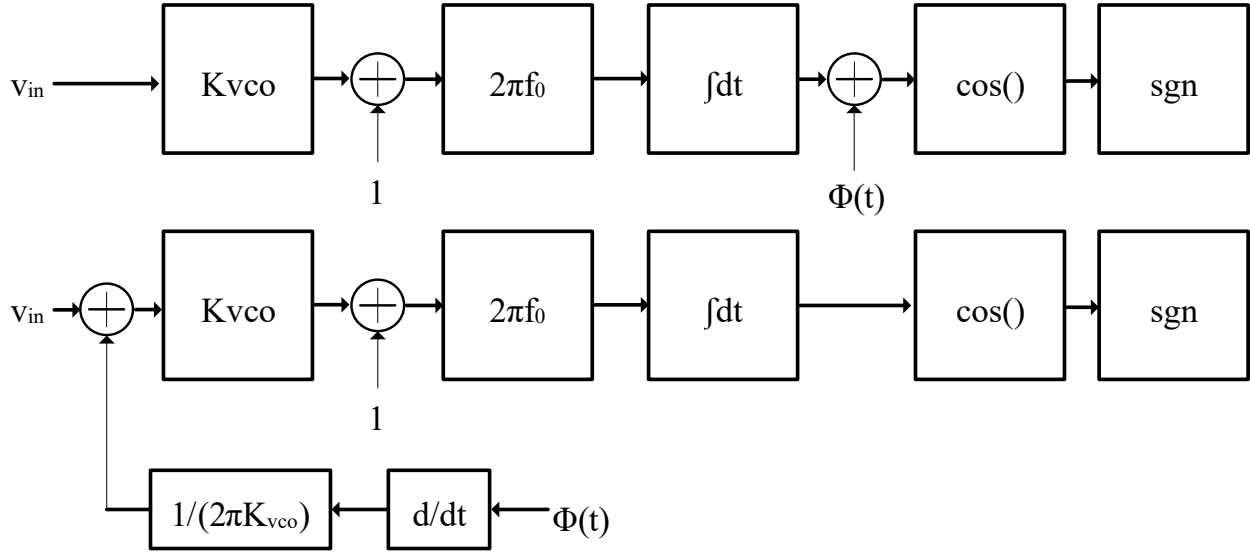
Fig. 7.27. VCO Phase Noise Model

$$S_{IRPN}(\Delta f) = \frac{2*L(\Delta f)(2\Delta f^2)}{k_{VCO}^2 f_o^2} \tag{14}$$

Where $L(\Delta f)$ is the measured phase noise, Δf is the phase noise offset frequency, k_{VCO} is the voltage to frequency gain, and f_0 is the ICRO center frequency [6].

To analyze the thermal noise of the rest of the circuit, we perform PSS/Pnoise analysis of the same circuit used in the PSS analysis for linearity measurements. With this model, we get the differential input referred noise of a two-path VCO-Based ADC. 3dB is subtracted from the noise to account for the differential gain, and the input referred phase noise is added to get the total input referred noise for a single path of the VCO-Based ADC.

$$SNR_{4-pathVCOADC} = \frac{P_{signal}}{\frac{S_{IRPN}}{G^2} + P_{noise}} + 6dB \tag{15}$$

Where G is the gain of the V-I and I-V converter, and P_{noise} is the single-ended input noise of the analog circuitry not including the ICRO.

b) Transient Analysis

The same circuit model in the transient linearity analysis is used, but without a no-input sinusoid. After running the same Matlab script, the total output noise will be reflective of the SQNR. To reduce the quantization error, we measure the time domain output of the ICROs and interpolate the phase values. Because the time of each ICRO transition is known precisely from a transient

simulation, the phase quantization can be interpolated to generate additional quantization levels, decreasing the SQNR.
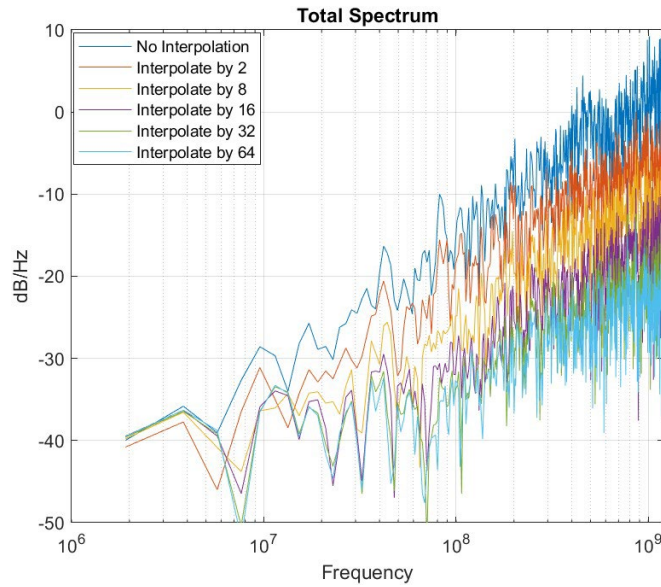

Fig. 7.28. Quantization Noise Spectrum with Different Interpolation Factors

7.1.11 Behavioral Modeling

In addition to Cadence circuit schematic simulations, a C code behavioral model was adapted to provide expected performance of the VCO-Based ΠΔΣ ADC. A behavioral simulation model from [1] was adapted to model the effects of a VCO-Based ADC, nonlinearity, clock jitter, and parallel ADCs. A behavioral model is required because a circuit simulation of a full VCO-Based ΠΔΣ ADC would be impractical.

7.1.12 Expected Performance

Circuit design indicates that a VCO-ADC is able to achieve a $SNR_{thermal}$ of 81.5dB, SQNR of 69dB FOM_{th} of 164.6dB, FOM_q of 153dB, P_{analog} of 395mW. A $P_{digital}$ of 88.6mW is estimated by scaling the power dissipation of a previous VCO-ADC design to match this project's process and system configuration. Using these values, the predicted minimum power dissipation of the VCO-Based ΠΔΣ ADC is 85W, corresponding to a FOM_{total} of 152.6dB.

This configuration uses 20 Hadamard modulated channels with 11 parallel ADCs.

Table 7.1. Overall Configuration

Parameter	Value
Number of Inverters (total)	28
f_0: Center/Sampling Frequency	2.4 GHz
OSR: Oversampling Rate	12
M: ΠΔΣ Channels	20
P: Parallel ADCs	11
Total Number of VCO-Based ADCs	220
Dither DAC Frequency	300 MHz

The power consumption of the analog blocks is dominated by the ICRO, then sampling unit. ICRO power consumption is high due to the large sizes needed to meet the noise targets.
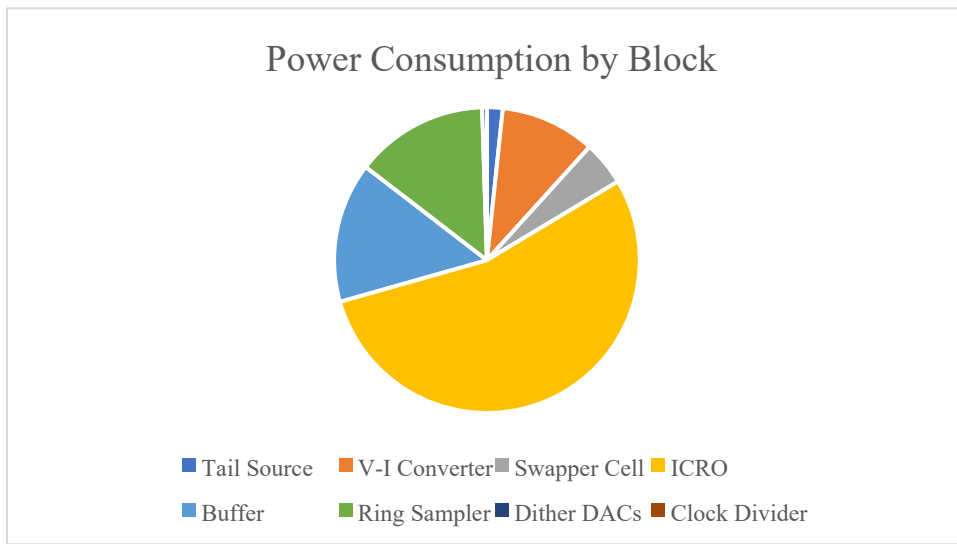

Fig. 7.29. Power Consumption Chart

a) Noise Performance

The estimated SNR due to thermal noise of the VCO-Based ΠΔΣ ADC is 91dB. The noise is limited by the linearity of the ICRO. It was found that increasing the ICRO power consumption such that the 99dB SNR target was met lead to a non-linear phase shift and memory that could not be corrected by the LUT. Therefore, a smaller ICRO is used.
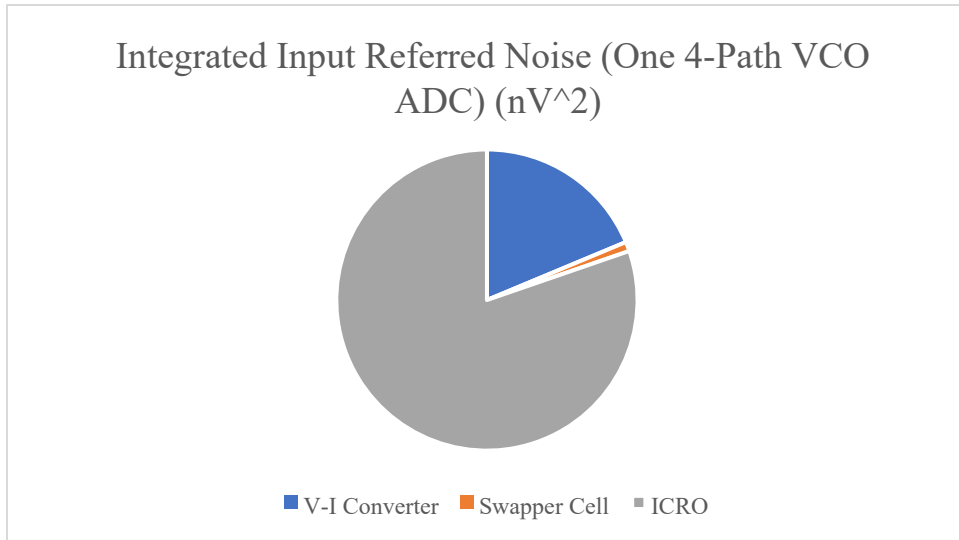
Fig. 7.30. Noise Breakdown Chart

b) Linearity Performance

Figures below depict the final schematic simulation results of the design. These simulations also demonstrate the linearity problem. Here, two tone and single tone simulations are performed to demonstrate the difference in calibration of harmonic distortion and IMD3. In both single and two-tone tests, the HD3/IMR3 can be improved to over 90dBc. However, different calibration coefficients are required in the single-tone vs. two-tone case. In a memory-less system, both two-tone and single-tone simulations would require the same calibration coefficients. If calibration coefficients are determined through no-swap calibration, then a 30 MHz input signal will create an 82dBc third order harmonic.
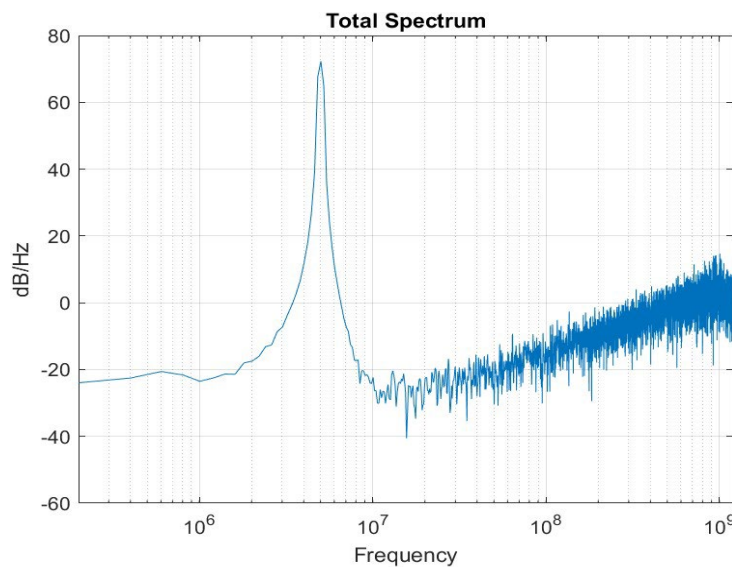

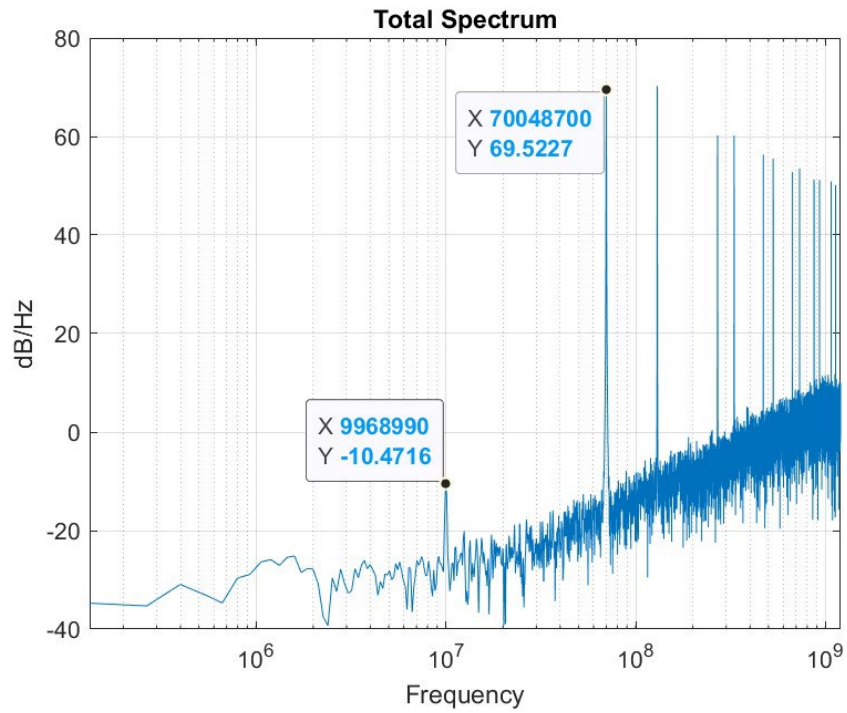**Fig. 7.31. Calibrated Single-Tone Output without Swapping**

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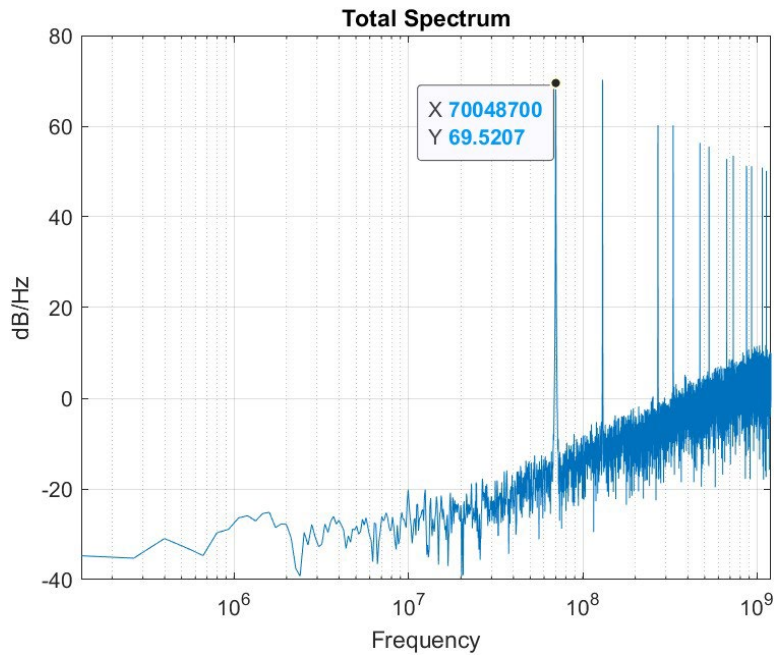**Fig. 7.32. Calibrated Single Tone Output with Swapping**

Fig. 7.33. Calibrated Single Tone Output with Swapping and Modified LUT Coefficients
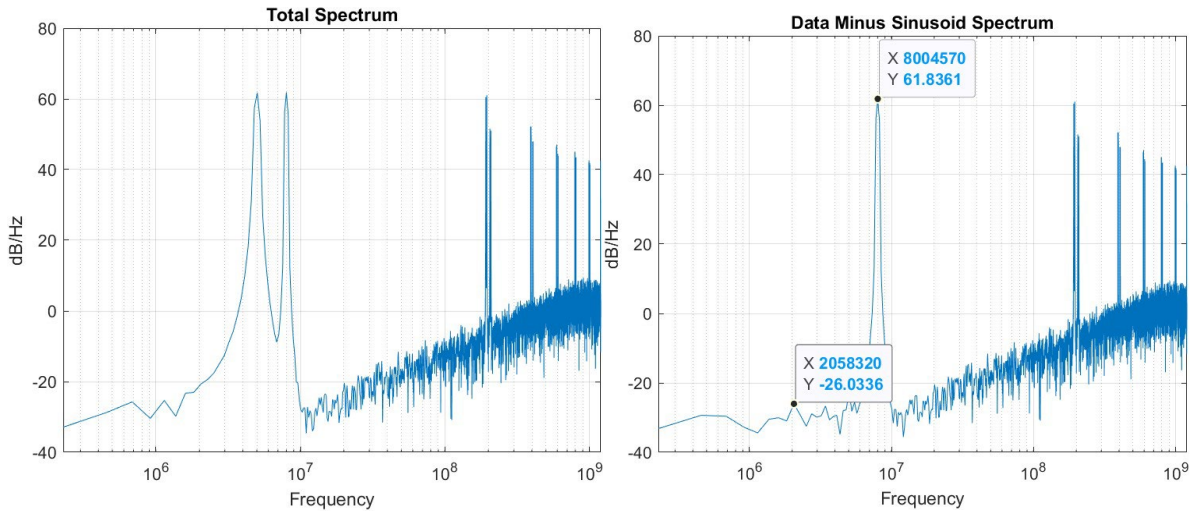
Fig. 7.34. Calibrated Two Tone Simulation with 3 MHz Spaced Tones

c) Comparison with State of the Art

The performance of this project compared to other state-of-the-art ADC is shown in Table 2 [7].

Table 7.2. Comparison to State-of-the-Art

ADC	SNDR (dB)	BW (MHz)	FOM (dB)
This Project	91	100	152.6
[8]	79.8	50	168.7
[9]	72.6	100	170.5
[10]	74 (75.8)	150 (100)	158.4

7.1.13 Floorplan and Testing Plans

Floorplan block diagrams and testing plans were developed during the project as well.

The proposed floorplan uses a 5x5mm, 36 pin quad-flat no-leads (QFN) package. 16 pins are dedicated LVDS to provide ADC output codes, 4 pins are dedicated to SPI to load calibration coefficients, and the remaining pins are dedicated to power supply. A reference pin is provided to assist with generation of bias currents. Chip area is dominated by the ICROs and digital logic. Due to high power and area consumption, the total ADC system is composed of 20 chips, each for a separate Hadamard channel. Each chip contains 11 parallel ADCs to meet the thermal and quantization noise targets. The total area is estimated to be 4.4 mm^2 per chip.

Table 1 and Fig. 7.35 depict the proposed pinout and floorplan. Fig. 7.36 shows the distribution of are to each major block for one of the 20 proposed chips. Area of the signal converter was estimated based off of results of [2].

Table 7.3. Proposed Pinout

| Pin Number	Pin Function	Pin Number	Pin Function
1,33,34,35,36	ICRO_Supply	17	LVDS[3]-
2	1.2V Analog Supply	18	LVDS[4]+
3	1.2V Digital Supply	19	LVDS[4]-
4	Swapper_Cell_Supply P	20	LVDS[5]+
5	Swapper_Cell_Supply N	21	LVDS[5]-
6	Clk	22	LVDS[6]+
7	Vin+	23	LVDS[6]-
8	Vin-	24	LVDS[7]+
9	Iref	25	LVDS[7]-
10	LVDS[0]+	26	LVDS_clk+
11	LVDS[0]-	27	LVDS_clk-
12	LVDS[1]+	28	1.8V IO
13	LVDS[1]-	29	SPI_CLK
14	LVDS[2]+	30	SPI_MOSI
15	LVDS[2]-	31	SPI_MISO
16	LVDS[3]+	32	SPI_CS
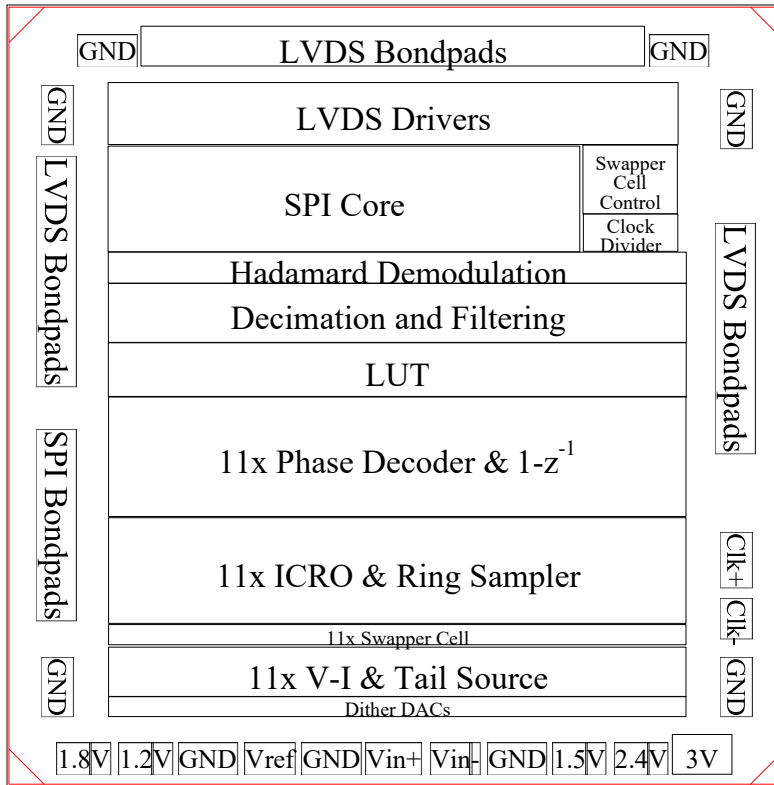
Fig. 7.35. General Floorplan

The largest analog block is the ICRO, which is estimated to be 0.46 mm^2 per VCO-Based ADC, followed by the phase sampler, 0.25 mm^2, then the V-I converter, 0.21mm^2.
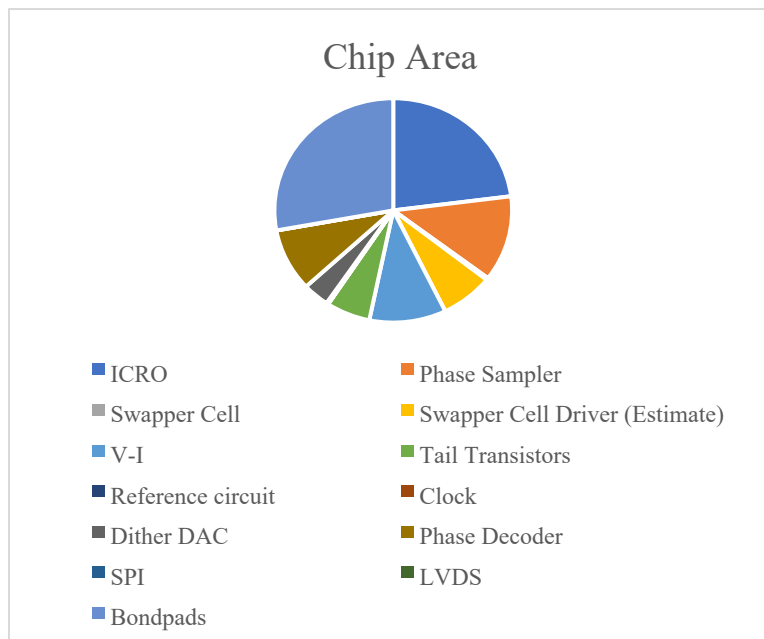

Fig. 7.36. Chip Area Breakdown by Block

A test board containing FPGAs will connect to the 20 chips and process the data to allow for off-chip calibration coefficient measurement and combining of digital data. All chips will be enabled and an input test sinusoid will be injected at the input of the ADCs. The quantized values from the phase sampler will be sampled by the FPGA and nonlinearity coefficients will be generated by the method described in Section 3.
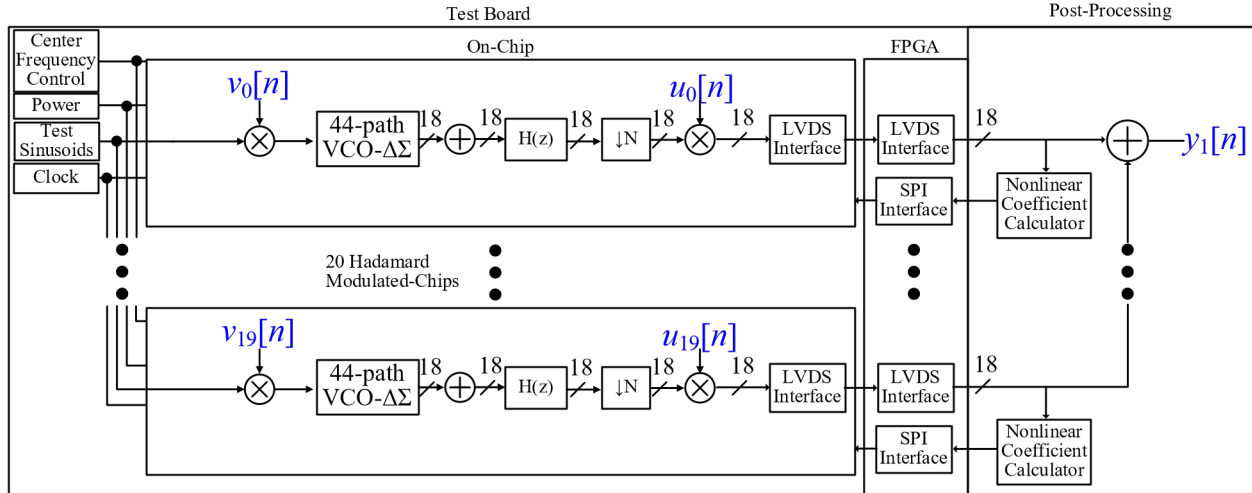

Fig. 7.37. Proposed Test Setup

7.1.14 Conclusion

In this project, we were able to complete the schematic design of the main analog blocks for the proposed VCO-based $\Pi\Delta\Sigma$ ADC as well as develop behavioral simulation and circuit analysis methods to characterize the architecture. Behavioral and circuit analysis indicates that the VCO-based $\Pi\Delta\Sigma$ ADC is not an efficient method to create high BW, high SNDR ADCs. In systems with lower BW and SNDR targets, the I-V converter is an acceptable solution as a memory calibration system requires significant power consumption. To resolve linearity issues in future works, a memory calibration system should be considered. While the I-V converter is able to solve some memory associated with the source-coupled capacitance to extend the bandwidth, it is not able to effectively shunt enough capacitance to achieve the desired 98 dB SNDR.

a) Summary of Remaining Work

If the project is to continue to tapeout, the following work is recommended: The clock divider should be included in future simulations. Additionally, development of a swapper cell driver is required. A previous design using CMOS inverters was developed but cannot be used because the swapper cell requires 200mV swing, smaller than the driver architecture can supply. Layout and layout parasitic simulations will be required. Work into debugging layout and parasitic extraction was performed, but full layout will be required. To complete digital design, the high-speed digital circuits may be adapted from Verilog models to hand-placed transistors. An LVDS driver and controller is required to interface with the FPGA on the test board. Additionally, logic for a Hadamard modulation and dither sequence shift register must be made. Finally, an SPI core in

Verilog used by the research group has been adapted for the project but must be completed once it is confirmed that all digital inputs and outputs are complete.

b) Recommendations

If the project is to be restarted, the author recommends the following:

It is recommended that future VCO-Based ADCs be developed in more highly scaled CMOS processes as opposed to advanced BiCMOS processes. One of the key difficulties in the design is maintaining high performance in the ring oscillators and high sample rates. Simulations have shown that power consumption, noise and bandwidth are limited by the ICRO. The loss in noise and swapping performance from changing the NPN transistors in the V-I, swapper cell, and I-V to CMOS transistors will be compensated for by the faster available sample rate and lower parasitics of a more scaled process.

7.1.15 References

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[10] Shibata et al., "A DC-to-1GHz tunable RF ΔΣ ADC achieving DR = 74dB and BW = 150MHz at f0 = 450MHz using 550mW," *IEEE International Solid-State Circuits Conference,* no. doi: 10.1109/ISSCC.2012.6176954, pp. 150-152, 2012.