AFRL-AFOSR-VA-TR-2023-0232

Fundamental studies of InAlN/GaN HEMTs on Si substrate

Zeng, Yuping
UNIVERSITY OF DELAWARE
220 HULLIHEN HALL
NEWARK, DE, 19716
USA

12/21/2022
Final Technical Report

Air Force Research Laboratory
Air Force Office of Scientific Research
Arlington, Virginia 22203
Air Force Materiel Command

REPORT DOCUMENTATION PAGE

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1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED	
20221221	Final	START DATE 20211231	END DATE 20221230

4. TITLE AND SUBTITLE
Fundamental studies of InAlN/GaN HEMTs on Si substrate

5a. CONTRACT NUMBER	5b. GRANT NUMBER	5c. PROGRAM ELEMENT NUMBER
FA9550-21-1-0076		61102F
5d. PROJECT NUMBER	**5e. TASK NUMBER**	**5f. WORK UNIT NUMBER**

6. AUTHOR(S)
Yuping Zeng

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
UNIVERSITY OF DELAWARE
220 HULLIHEN HALL
NEWARK, DE 19716
USA

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)	11. SPONSOR/MONITOR'S REPORT NUMBER(S)
Air Force Office of Scientific Research 875 N. Randolph St. Room 3112 Arlington, VA 22203	AFRL/AFOSR RTA1	AFRL-AFOSR-VA-TR-2023-0232

12. DISTRIBUTION/AVAILABILITY STATEMENT
A Distribution Unlimited: PB Public Release

13. SUPPLEMENTARY NOTES

14. ABSTRACT
The next-generation of communication systems, including 5G and beyond, vehicles and internet of things needs components operating at mm-Wave bands with low cost and high-efficiency. For such communication system, high efficiency and high bandwidth power amplifiers are the key elements. However, the current commercially available power amplifiers using Si and GaAs technologies can not meet such requirements due to their lack of high power and high frequency capabilities. Instead, GaN high electron mobility transistor (HEMT) technology is one of the potential candidates, resulting from the high electron mobility and wide bandgap features. Two dominant GaN technologies are GaN-on-Si HEMTs and GaN-on-SiC HEMTs. Compared to their GaN-on-SiC counterpart, GaN-on-Si HEMTs feature advantages of low cost, large-scale capability and are thus compatible with large wafer diameter CMOS foundries. However, to-date, GaN-on-silicon HEMTs DC and RF performances still need to be drastically improved.

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES
a. REPORT U	b. ABSTRACT U	c. THIS PAGE U	UU	72

19a. NAME OF RESPONSIBLE PERSON	19b. PHONE NUMBER *(Include area code)*
KENNETH GORETTA	426-7349

Fundamental studies of InAlN/GaN HEMTs on Si substrate

PI: Yuping Zeng, yzeng@udel.edu, University of Delaware,
Award No. FA9550-21-1-0076
(Funding period: Dec 31, 2020-Dec 31,2023, Defunded Jan 1,2022)
Collaborator Partner: Ashwani Sharma, ashwani.sharma@us.af.mil, Air Force Research Laboratory
June 24, 2022

Abstract

The next-generation of communication systems, including 5G and beyond, vehicles and internet of things needs components operating at mm-Wave bands with low cost and high-efficiency. For such communication system, high efficiency and high bandwidth power amplifiers are the key elements. However, the current commercially available power amplifiers using Si and GaAs technologies can not meet such requirements due to their lack of high power and high frequency capabilities. Instead, GaN high electron mobility transistor (HEMT) technology is one of the potential candidates, resulting from the high electron mobility and wide bandgap features. Two dominant GaN technologies are GaN-on-Si HEMTs and GaN-on-SiC HEMTs. Compared to their GaN-on-SiC counterpart, GaN-on-Si HEMTs feature advantages of low cost, large-scale capability and are thus compatible with large wafer diameter CMOS foundries. However, to-date, GaN-on-silicon HEMTs DC and RF performances still need to be drastically improved.

In particular, when downscaling is adopted to improve the RF performances, device nonlinearity behavior and thermal instability problems are severely observed. The behind reasons are still not clear and innovations in materials, fabrication process and device design techniques to prevent these problems are needed.

Within this year, Prof. Zeng's group has developed InAlN/GaN-on-Si technology for both high electron mobility transistors (HEMTs) and metal-insulator-semiconductor high electron mobility transistors (MISHEMTs) with high performance. For HEMTs, with a series of innovation techniques, we have demonstrated GaN-on-Si HEMTs with current gain cutoff frequency (f_T of 215GHz, record high f_TxL_g of 16GHz·μm), f_{MAX} of 270GHz), which is highlighted by more than

10 news media (including "Semiconductor Today", etc.). For MISHEMTs, we used HfZrO, TiO_2 and TiAlO as the gate dielectric and demonstrated GaN-on-Si MISHEMTs with excellent performance, enabling its high speed power applications.

Accomplishments

- **Research Objectives:**

We proposed to develop high performance InAlN GaN-on-Si HEMTs with nanowire as the channel by using innovative material, process and device design techniques and evaluate the device linearity and temperature stability.

Our specific objectives are to: (1) optimize the epitaxial layer design for GaN HEMTs; (2) develop the fabrication process for GaN HEMTs; (3) evaluate the device DC and RF characteristics, linearity as well as stability and identify the behind performance degradation mechanisms. Aim (1) and (2) work will be led by Dr. Zeng, and Aim (3) work will be led by Dr. Sharma.

- **Details of accomplishments during this reporting period.**

(1) High speed GaN-on-Si HEMTs with record high $f_T \times L_g$ performance have been achieved [1], the carrier transport mechanisms of which are now under investigation through Dr. Ashwani Sharma's group in Air Force Research Lab (AFRL).
(2) GaN-on-Si HEMTs with high f_{MAX} of 270GHz has been achieved [2].
(3) Subthreshold slope of lower than 60mV/dec GaN-on-Si HEMTs have been demonstrated [3].
(4) High performance MISHEMTs using ZrO_2 [4] as the gate dielectric have been demonstrated [4].
(5) The performance of downscaled device with Lg=20nm has been projected [5] with an f_T/f_{MAX} of 320/535Ghz.
(6) High performance MISHEMTs using HZO as the gate dielectrics have been demonstrated (Under review, work with Neil Moser, Chabak Kelson, AFRL) and their power performance has been characterized.
(7) GaN MISHEMTs with TiO_2 and TiAlxO gate dielectrics have been demonstrated.
(8) TCAD simulation model has been developed and used to predict the device power performance.

- **How were the results disseminated to communities of interest?**
  Our results are published in the following 16 papers and 1 patent [6]:

1. Peng Cui, **Yuping Zeng**, "Effect of Device Scaling on Electron Mobility in Nanoscale GaN HEMTs with Polarization Charge Modulation", Nanomaterials, Vol. 12, pp. 1718, 2022.

2. H Zhao, G Lin, P Cui, J Zhang, **Y Zeng**, "Multilayer MoS_2 Back-Gate Transistors with ZrO_2 Dielectric Layer Optimization for Low-Power Electronics," physica status solidi (a), Vol. 219, pp. 2100760, 2022

3. Q Cheng, S Khandelwal, **Y Zeng**, "A Physics-Based Model of Vertical TFET--Part I: Modeling of Electric Potential", IEEE Transaction on Electron Device, pp.3966-3973, 2022.

4. Qi Cheng, S Khandelwal, **Y Zeng**, "A Physically-Based Model of Vertical TFET--Part II: Drain Current Model", IEEE Transaction on Electron Device, pp.3974-3982, 2022.

5. Guangyang Lin, Kun Qian,Hongjie Cai, Haochen Zhao, Jianfang Xua, Songyan Chen, Cheng Li, Ryan Hickey, James Kolodzey, **Yuping Zeng**, "Enhanced photoluminescence of GeSn by strain relaxation and spontaneous carrier confinement through rapid thermal annealing," Journal of Alloys and Compounds, Volume 915, 165453, 15 September 2022.

6. Jie Zhang, Meng Jia, Maria Gabriela Sales, Yong Zhao, Guangyang Lin, Peng Cui, Chaiwarut Santiwipharat, Chaoying Ni, Stephen McDonnell, **Yuping Zeng**, "Impact of ZrO_2 dielectrics thickness on electrical performance of TiO_2 thin film transistors with sub-2 V operation," ACS Applied electronic materials, Vol. 3. pp. 5483-5495, 2021.

7. G Lin, P Cui, T Wang, R Hickey, J Zhang, H Zhao, J Kolodzey, **Y Zeng**, "Fabrication of germanium tin microstructures through inductively coupled plasma dry etching," IEEE Transactions on Nanotechnology, vol. 20, pp.846-851, September 30, 2021.

8. Peng Cui, **Yuping Zeng**, "Technology of sub-100 nm InAlN/GaN HEMTs on silicon with suppressed leakage current," Solid State Electronics, Volume 185, 108137, 2021.

9. Peng Cui, Tzu-Yi Yang, Jie Zhang, Yu-Lun Chueh and **Yuping Zeng**, "Improved On/off current ratio and linearity of InAlN/GaN HEMTs with N_2O surface treatment for radio frequency application," ECS Journal of solid state science and technology, No.10, 065013, 2021.

10. Peng Cui, **Yuping Zeng**, "Electrical properties of 90-nm InAlN/GaN HEMT on silicon substrate," Physica E: Low-dimensional systems and nanostructures, Vol. 134, 114821, 2021.

11. Jie Zhang, Graduate Student Member, Yuying Zhang, Peng Cui, Guangyang Lin, Chaoying Ni, and **Yuping Zeng**, "One-Volt TiO_2 Thin Film Transistors With Low-Temperature Process," IEEE Electron Device Letters, Vol. 42, No.4, pp.521-524, 2021.

12. Peng Cui, Meng Jia, Hang Chen, Guangyang Lin, Jie Zhang, Lars Gundlach, John Q Xiao, **Yuping Zeng**, "InAlN/GaN HEMT on Si With fmax= 270 GHz," IEEE Transaction on Electron Devices, Vol. 68, No. 3, pp. 994-999, 2021.

13. Peng Cui, **Yuping Zeng**, "Electrical properties of 90-nm InAlN/GaN HEMT on silicon substrate," Physica E: Low-dimensional systems and nanostructures, Vol. 134, 114821, 2021.

Conference papers

1. Tuofu Zhama, Peng Cui, Jie Zhang, Haochen Zhao, Ashwani Sharma and **Yuping Zeng**, "Improved On/Off Current Ratio of TiO_2/AlGaN/GaN/ MIS-HEMTs with N_2O Surface Treatment on TiO_2 Layer", Device Research Conference, 2022 (Top 15%).

2. Jie Zhang, Yuping Zeng, "High performance TiO_2 thin film transistors using TiO_2 as both channel and dielectric," Device Research Conference, 2022

3. Peng Cui, Yuping Zeng, "HZO/InAlN/GaN MIS-HEMT on Silicon with SS of 60 mV/dec and f_T/fmax of 115/200 GHz", Device Research Conference, June, 2021.

Patent

1. P. Cui and **Y. Zeng**, "A Two-Step Annealing on InAIN/GaN Source/Drain Contacts," Filed patent, 2022.

We have developed the high speed GaN-on-Si HEMTs technology with InAlN/GaN barrier layer. Based on these developed technologies, we are in the progress of further developing GaN HEMTs/MISHEMTs with planar and nanowire channel for Dr. Ashwani Sharma's group to further study on carrier transport next year. We have also successfully developed TiO_2 materials for the gate dielectric since its rutile phase features high permittivity up to ~120. We have achieved GaN MISHEMTs with enhanced performance using ZrO_2, HfZrO, TiO_2, TiAlO due to its high bandgap and high permittivity.

Impacts

We have developed device technology for high performance InAlN/GaN-on-Si HEMTs in RF applications. Our developed GaN-on-Si HEMTs have been highlighted by more than 10 news media (Semiconductor Today, Udaily, Science Daily, SciTech Daily, Smart 2.0, Nanotech-now, MSM supplies, Everything RF, Associated Environmental Systems, Interesting Engineering, etc). Because of these achievements, we built up another collaboration work with Chabak Kelson, AFRL for power measurements of our GaN-on-Si HEMTs and MISHEMTs and achieved high power performance at Ka band. Due to the GaN radiation robustness, we have also set up collaboration work with NASA international space station for radiation tests of our fabricated devices. Our technology has attracted NASA interests from GSFC for cloud-radar application and helps to secure funding from NASA EPSCOR program.

Our research results have secured interests from industry like Wolfspeed, AirLiquide companies. We have already been working with AirLiquide and the work is to be continued. We also expect to work with Wolfspeed in the coming year.

Through working with Ashwani Sharma, we expect to demonstrate the first temperature stability study of InAlN/GaN HEMTs on silicon with nanowire as the channel, enabling high efficiency and high linearity RF power amplifier on silicon substrates. The developed devices will lead to high performance systems with a reduced cost, size and weight, compatible with CMOS mainstream technology, indicating the great potential of using this technology for RF applications.

Technical Updates

Here is the outline of our technical updates:
(1) High speed GaN-on-Si HEMTs with record high $f_T \times L_g$ performance have been achieved [1],
(2) GaN-on-Si HEMTs with high f_{MAX} of 270GHz has been achieved [2].
(3) Subthreshold slope of lower than 60mV/dec GaN-on-Si HEMTs have been demonstrated [3].
(4) High performance MISHEMTs using ZrO_2 [4] as the gate dielectric have been demonstrated.
(5) Transistor with downscaling L_g=20nm was predicted to exhibit 320/535GHz [5].
(6) High performance MISHEMTs using HZO as the gate dielectrics have been demonstrated (Under review, work with AFRL) [7]. It presents a high performance with I_{ON}/I_{OFF} of 9.3×10^7, SS of 130 mV/dec, DIBL of 45 mV/V, f_T/f_{max} of 155/250 GHz, $(f_T \times f_{max})^{1/2}$ of 197 GHz, and JFOM of 5.4 THz·V. Power performance at 30 GHz exhibit a saturation P_{out} of 1.36 W/mm, a maximum G_P of 12.3 dB, and a peak PEA of 21%,
(7) TiO_2 and $TiAl_xO$ gate dielectrics have been achieved by atomic layer deposition method and successfully applied to demonstrate GaN MISHEMTs for RF and power applications.
(8) TCAD simulation model has been successfully developed and used to predict GaN transistor power performance.

We will describe them (1-8) in more details in the "Technical Updates" section. Based on these developed technologies, we plan to further develop GaN-on-Si HEMTs/MISHEMTs with planar and nanowire channels for Dr. Ashwani Sharma's group further study on carrier transport. We will also analyze carrier scattering mechanisms and apply various passivation techniques using our developed TiO_2-related materials to address the device reliability issue.

1. Record high $f_T \times L_g$ with a rectangular gate

1.1 Introduction

We report an 80-nm-gate-length $In_{0.17}Al_{0.83}N$/GaN high-electron mobility transistor (HEMT) on silicon substrate with a record low gate leakage current of 7.12×10^{-7} A/mm, a record high on/off current ratio of 1.58×10^6, and a steep subthreshold swing of 65 mV/dec, which are excellent features among the reported InAlN/GaN HEMTs on Si. Due to the excellent DC performance, a current gain cutoff frequency f_T of 200 GHz is achieved, resulting in $f_T \times L_g = 16$ GHz · μm for GaN HEMTs on Si which to the best of our knowledge is a new record.

1.2 Background

Due to the attractive material properties of GaN such as a wide bandgap (~ 3.4 eV), high breakdown field (~ 3.3 MV/cm) and high saturation electron drift velocity (~ 2.5×10^7 cm/s), GaN high electron mobility transistors (HEMTs) have been demonstrated as promising candidates for high-power and high-frequency applications.[8-12] During the last several decades, GaN HEMTs on SiC substrate have shown impressive radio frequency (RF) performance.[13-17] Y. Yue *et al*. reported a 30-nm-gate-length InAlN/AlN/GaN/SiC HEMTs with a current gain cutoff frequency (f_T) of 370 GHz by using a dielectric-free passivation and regrown ohmic contacts.[13] Y. Tang *et al*. reported that a record-high f_T of 454 GHz with a simultaneous maximum oscillation frequency (f_{max}) of 444 GHz was achieved on a 20-nm-gate-length AlN/GaN/AlGaN double heterostructure HEMT on SiC, representing the state-of-the-art performance of GaN HEMTs to-date.[14]

Although GaN HEMTs on SiC have shown excellent performance, the high cost of SiC substrate will limit their large-scale application. Considering the low-cost and the scaling capability of silicon substrates up to 200 mm, GaN HEMTs on Si substrate have attracted significant attention. In addition, owing to the developments in epitaxial growth and device fabrication, remarkable advancements in the performance of GaN-on-Si have been realized.[18-23] W. Jatal *et al.* reported that a f_T of 176 GHz was achieved on an 80-nm-gate-length AlGaN/GaN on Si with Au-free ohmic contact technology.[24] Y. Murase *et al.* demonstrated an 0.16-μm AlGaN/GaN HEMT on Si with a three-terminal breakdown voltage (BV_3) of 98 V and a f_{max} of 226 GHz.[25] F. Medjdoub *et al.* reported that a sub-1-dB minimum noise figure at 36 GHz was achieved on an 80-nm AlN/GaN-on-Si HEMTs with the f_T/f_{max} = 105/145 GHz.[18] D. Marti *et al*. reported that an InAlN/GaN HEMT on Si with a gate length (L_g) of 50 nm exhibited a peak transconductance of 650 mS/mm and f_T/f_{max} = 141/232 GHz.[19] W. Xing *et al*. reported a drain current of 2.66 A/mm and a record high f_T = 250 GHz on a 40-nm-gate-length InAlN/GaN HEMTs on Si.[20] S. Dai *et al*. reported AlGa(In)N/GaN HEMTs on Si with a record low gate leakage below 10^{-5} A/mm, a high on/off current (I_{on}/I_{off}) ratio of 1.78×10^5, and a record high value of $(f_T \cdot f_{max})^{1/2}$ = 178 GHz (f_T/f_{max} = 145/220 GHz) among the reported GaN-on-Si devices.[21] However, compared with the GaN HEMTs on SiC, there is still much room for the performance improvement of GaN HEMTs on Si. In this work, an 80-nm-gate-length InAlN/GaN HEMT on Si with a record low gate leakage current of 7.12×10^{-7} A/mm, a record low off current of 7.97×10^{-7} A/mm, a record high I_{on}/I_{off} ratio of 1.58×10^6, and a record high $f_T \times L_g$ = 16 GHz·μm was demonstrated.

1.3 Experimental Details, Results and Discussions

The InAlN/GaN heterostructure consists of 2-nm GaN cap layer, an 8-nm lattice-matched $In_{0.17}Al_{0.83}N$ barrier layer, a 1-nm AlN interlayer, a 15-nm GaN channel layer, a 4-nm $In_{0.12}Ga_{0.88}N$ back barrier layer, and a 2-μm undoped GaN buffer layer on a Si substrate. This structure is grown by metalorganic chemical vapor deposition (MOCVD). The sheet electron concentration and electron mobility measured by Hall measurements were 2.28×10^{13} cm^{-2} and 1205 $cm^2/V \cdot s$, respectively.

The device fabrication started with mesa isolation using Cl_2- based plasma reactive ion etching, followed by alloyed ohmic contacts with a Ti/Al/Ni/Au stack annealed at 850˚C for 40s in N_2. The source-drain spacing (L_{ds}) is 2 μm. Transmission line measurement shows that the ohmic contact resistance is 0.6 Ω·mm. Prior to gate lithography, an oxygen plasma treatment was applied on the chip using the Allwin21 O_2 Plasma Asher with the RF power of 800W for 1 min. The resulted oxide layer on the surface can effectively reduce the gate leakage current and improve RF performance.[26-29] Then an 80-nm gate was defined in the center of the source and drain contacts by electron beam lithography followed by Ni/Au gate metal stack deposition with electron beam evaporation.

The DC current-voltage (*I–V*) measurements were carried out by using an Agilent B1500A semiconductor parameter analyzer. Figure 1(a) shows the *I-V* output characteristic of the 80-nm InAlN/GaN HEMT. The gate-to-channel distance t_{bar} (including 2-nm GaN, 8-nm InAlN, and 1-nm AlN) is 11nm. Since L_g is 80 nm, the device has a high aspect ratio (L_g/ t_{bar}) of 7.3, leading to the suppressed short-channel effects (SCEs)[27, 30, 31] and the excellent pinch-off *I-V* output characteristics. The semi-log-scale transfer curves and the gate leakage currents as a function of gate-source voltage (V_{gs}) at drain-source voltage V_{ds} = 10 V with and without O_2 plasma treatment are shown in Fig. 1(b). After O_2 plasma treatment, both the off-state current (I_{off}) and the gate leakage current (I_g) reduce two orders of magnitude, the I_{on}/I_{off} ratio increases two folds, and the subthreshold swing (SS) improves from 76 mV/dec to 65 mV/dec. Therefore, using the O_2 plasma treatment, the I_{off} of 7.97×10^{-7} A/mm, I_g of 7.12×10^{-7} A/mm, I_{on}/I_{off} ratio of 1.58×10^6, and SS of 65 mV/mm are simultaneously achieved on an 80-nm-gate-length InAlN/GaN HEMT on Si. To the best of our knowledge, these DC measurement results all show record values among those reported InAlN/GaN HEMTs on Si to-date (I_g of 7×10^{-6} A/mm,[21] I_{off} of 7×10^{-6} A/mm,[21] I_{on}/I_{off} ratio of 1.78×10^5,[21] and SS of 82 mV/dec[32] are the best values that have been reported in InAlN/GaN HEMTs). Due to the thin InAlN barrier (~ 8 nm), both the I_g and I_{off} are higher than

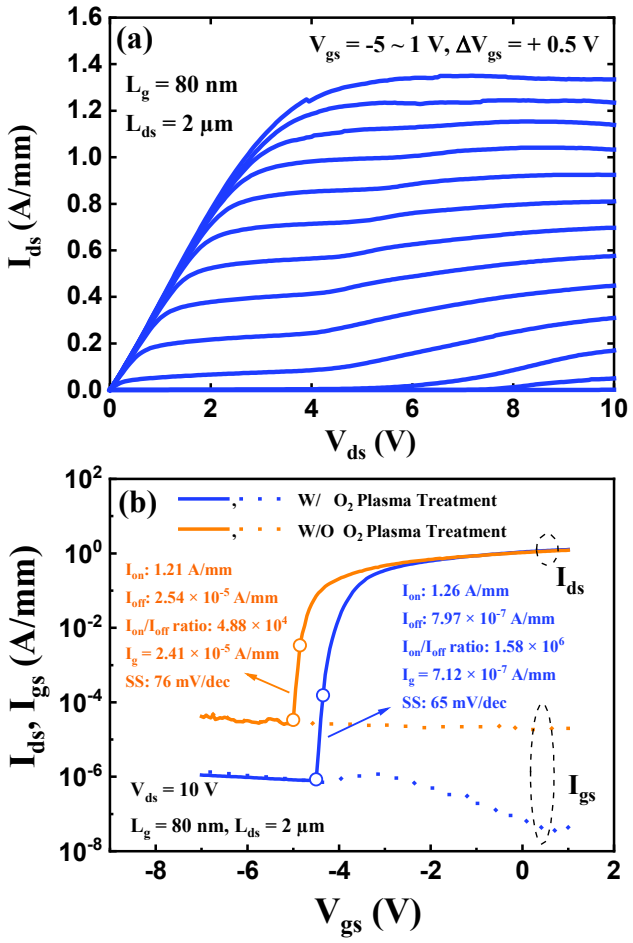

Fig. 1. (a) *I-V* output characteristic, (b) the semi-log-scale transfer curves and the gate leakage current as a function of V_{gs} at V_{ds} = 10 V of InAlN/GaN HEMT (L_g = 80 nm) with and without O_2 plasma treatment.

those have been reported in AlGaN/GaN HMETs on Si with a 20-nm AlGaN barrier layer (I_g of 10^{-12} A/mm, I_{off} of 10^{-12} A/mm, and I_{on}/I_{off} ratio of 2.5×10^{11} are the record values among the GaN HEMT on Si).[33] Three reasons are accounted to explain these achievements: 1) the high L_g/t_{bar} effectively suppresses the SCEs and thus leads to an excellent gate control capability;[27, 30, 31] 2) the oxygen plasma treatment reduces the gate leakage from the thin InAlN barrier layer;[26-29] 3) the InGaN back-barrier layer improves the carrier confinement, decreases the buffer leakage current, and reduces the SCEs.[16, 34, 35] Due to the three factors, the decrease of the leakage current (gate/drain-source current) and thus the suppression of the SCEs result in the improved I_{on}/I_{off} and the steep SS.

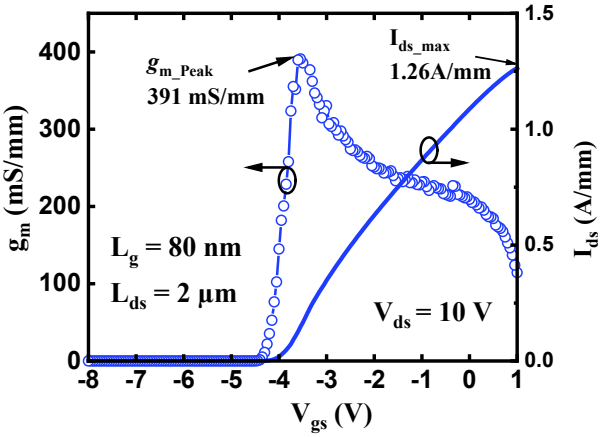

Fig. 2. Measured extrinsic transconductance g_m with a peak transconductance g_{m_peak} = 442 mS/mm and transfer curve at V_{ds} = 10 V of InAlN/GaN HEMT (L_g = 80 nm).

Figure 2 shows the extrinsic transconductance g_m and the transfer curves at V_{ds} = 10 V. Due to the thin InAlN barrier, the g_m peak (g_{m_peak}) reaches at 391 mS/mm, which is higher than that was reported in AlGaN/GaN HEMTs (L_g = 75nm, t_{bar} = 11.5 nm, g_{m_peak} = 374 mS/mm) on Si with almost the same L_g.[36] However, the device g_{m_peak} is lower than that in AlN/GaN HEMTs on Silicon (L_g = 80 nm, t_{bar} = 6 nm, g_{m_peak} = 580 mS/mm) due to the thinner AlN barrier in Ref [18]. The maximal drain current (I_{ds_max}) (at V_{ds} = 10 V, V_{gs} = 1 V) is 1.26 A/mm, lower than the record values of 2.66 A/mm with L_{ds} = 300 nm in Ref [20]. The low I_{ds_max} in this work should result from the larger extrinsic resistance arising from the large L_{ds} which is 2 µm.

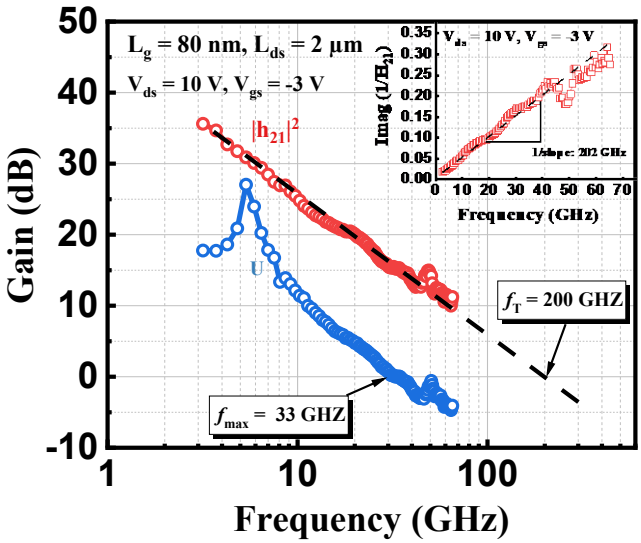

Fig. 3. RF performance of the 80-nm-gate-length InAlN/GaN HEMTs with f_T/f_{max} =200/33 GHz. The inset shows the Gummel's method with f_T = 202 GHz.

The device RF performance was measured by an Agilent E8361C vector network analyzer. The measured frequency range was from 1 to 65 GHz. Before device measurement, the network analyzer was calibrated using a two port short/open/load/through method. The on-wafer open and

short structures were used to eliminate the effects of parasitic elements. After de-embedding, the current gain $|h_{21}|^2$ and unilateral gain U as a function of frequency when the device is operated at V_{DS} = 10 V, V_{GS} = −3 V were shown in Fig. 3. A current gain cutoff frequency f_T of 200 GHz was obtained by extrapolation of $|h_{21}|^2$ with a -20 dB/dec slope. As shown in the inset of Fig. 3, the Gummel's method is also applied to extract f_T [37], and a similar f_T value of 202 GHz was also obtained. Due to the high resistance of the rectangular gate, a low f_{max} value of 33 GHz is expected.

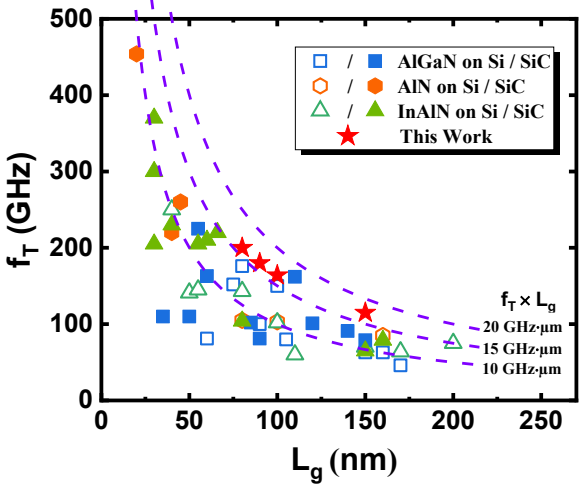

Fig. 4. Comparison of the f_T of the InAlN/GaN HEMTs on Si in this work with other reported GaN HEMTs (AlGaN on Si [24, 38-45]/SiC [27, 46-52], AlN on Si [18, 53, 54]/SiC [55-57], and InAlN on Si [19-21, 25, 58, 59]/SiC [10, 13, 16, 29, 60-65] with $L_g \leq 200$ nm).

The InAlN/GaN HEMTs with L_g = 80 nm shows a high $f_T \times L_g$ of 16 GHz·μm. As shown in Fig. 4, the reported highest $f_T \times L_g$ value among the GaN HEMTs with $L_g \leq 200$ nm is 17.8 GHz·μm in 162-GHz AlGaN/GaN HEMT on SiC with L_g = 110 nm.[27] To the best of our knowledge, the $f_T \times L_g$ in our study achieves the highest value among all reported GaN HEMTs on silicon, and set a new record among GaN HEMTs on SiC/Si with $L_g \leq 100$ nm.

The relationship between f_T and L_g can be written as[31]

$$f_T = \frac{\frac{v_{e-eff}}{2\pi}}{L_g + a \cdot t_{bar}}, \quad (1)$$

where v_{e-eff} is the effective electron velocity and a is a fitting parameters. a is uncorrelated with L_g. In Figure 4, the f_T values of the InAlN/GaN HEMTs are 115 GHz (L_g = 150 nm), 164 GHz (L_g = 100 nm), 180 GHz (L_g = 90 nm), 200 GHz (L_g = 80 nm), respectively. By fitting the experiment results using (1), v_{e-eff} = 1.18 × 10^7 cm/s and a = 1.31 are obtained. The v_{e-eff} is slightly smaller than that in reported AlGaN/GaN HEMTs on SiC (v_{e-eff} = 1.24 × 10^7 cm/s), which may be due to the usually better material quality grown on SiC. a is much smaller than that reported in AlGaN/GaN HEMTs (where a = 5.1), an indication of the suppressed SCEs. Using (1), f_T and $f_T \times L_g$ can be plotted shown in Fig. 5. The f_T increases from 200 GHz (L_g = 80 nm) to 346 GHz (L_g = 40 nm) and 546 GHz (L_g = 20 nm). Due to the increased SCEs and the parasitic component effect with the decreased L_g, $f_T \times L_g$ decreases from 16 GHz · μm (L_g = 80 nm) to 13.8 GHz · μm (L_g = 40 nm)

and 10.9 GHz · μm (L_g = 20 nm). These results present the great potential of the device technology for further improving the device RF performances if the device is further scaled down.

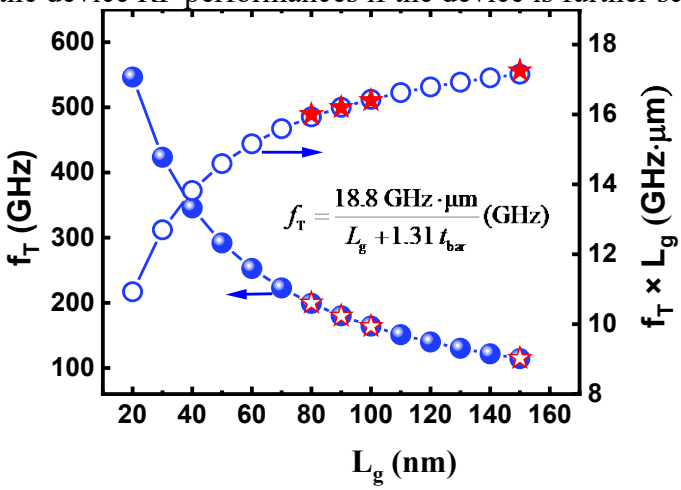

Fig. 5. The predicted f_T (left) and $f_T \times L_g$ (right) as a function of L_g (The stars represent the experimental results).

1.4 Summary

The presented device technology reveals a record low gate leakage current of 7.12 × 10^{-7} A/mm, a record low off current of 7.97 × 10^{-7} A/mm, a record high I_{on}/I_{off} ratio of 1.58 × 10^6, and a steep SS of 65 mV/dec as well as a record high $f_T \times L_g$ of 16 GHz · μm which can be simultaneously achieved from InAlN/GaN HEMT on Si with L_g = 80 nm. The high $f_T \times L_g$ shows that the great potential of the InAlN GaN HEMT device technology to be applied in high speed applications on silicon platform when further downscaling the device feature size.

2. High f_{MAX} of 270GHz HEMTs with a T-shaped gate achieved by a two-step annealing

2.1 Introduction

Device surface properties are critical for its performance such as channel electron density, leakage current, subthreshold swing, and noise in gallium nitride high-electron-mobility transistors (HEMTs). In this paper, the improved surface property of InAlN/GaN HEMTs with forming gas (FG, 5% H_2 and 95% N_2) annealing is demonstrated. X-ray photoelectron spectra (XPS) shows that the number of Ga-O bonds decreases while that of the Ga-N bonds increases, an indication of the surface native oxide removal after FG annealing. Compared with N_2 annealing, an increase of two-dimensional electron gas (2DEG) electron density with FG annealing is determined by both energy band simulation and capacitance-voltage measurement. Transmission line measurement (TLM) shows that N_2 annealing offers a lower ohmic contact resistance (R_C) while FG annealing features a lower sheet resistance (R_{sheet}). Herein, a FG/N_2 two-step ohmic contact annealing is developed to achieve a subthreshold swing (SS) of 110 mV/dec, a transconductance (g_m) peak of 415 mS/mm, a record low drain-induced barrier lowing (DIBL) of 65 mV/V, and a record high power gain cutoff frequency (f_{max}) of 270 GHz on a 50-nm InAlN/GaN HEMT on Si.

2.2 Background

InAlN/GaN high-electron mobility transistor (HEMTs) on Si substrate have attracted extensive attentions [66-70]. Although Si substrate features a low cost and scaling capability than SiC substrate, the larger lattice mismatch between Si and GaN hinders the epitaxial material quality and device RF performance improvement. A high current gain cutoff frequency f_T of 400 GHz was achieved on a 30-nm InAlN/GaN HEMTs on SiC [71]. A balanced current/power gain cutoff frequency f_T/f_{max} of 348/340 GHz (for E-mode device) and f_T/f_{max} of 302/301 GHz (for D-mode device) were demonstrated on 37-nm InAlN/GaN HEMTs on SiC [15]. To date, f_T/f_{max} of 250/204 GHz [72] and f_T of 310 GHz [67] were demonstrated on InAlN/GaN HEMTs on Si, respectively. This indicates that GaN-on-Si HEMTs technology needs to be drastically improved as compared to the GaN-on-SiC counterpart.

To improve device performance of InAlN/GaN HEMTs on Si, technologies of fabrication process and material growth are the two keys. The low quality surface native oxide (GaO_x) presents a significant influence on the material electron mobility and device performance [73, 74]. An in-situ remote plasma pretreatment (RPP) carried out in an atomic layer deposition (ALD) system has demonstrated the capability of removing the surface native oxide [75], but the surface damage due to the plasma treatment is presented. H_2/N_2 forming gas (FG) annealing can be used for the post-metallization annealing (PMA) to avoid unintentional oxidation, decrease leakage current, and reduce the traps due to the hydrogen passivation [76, 77]. Thus, FG annealing becomes one of the possible effective ways to remove surface native oxide prior to gate metal deposition.

Considering that, in this paper, N_2 and FG are used during ohmic contact annealing in InAlN/GaN HEMTs on Si. Compared with N_2 annealing, the native oxide is removed by FG annealing and the two-dimensional electron gas (2DEG) electron density increases as determined by X-ray photoelectron spectra (XPS), energy band simulation and capacitance-voltage measurement. Transmission line measurement (TLM) shows that N_2 annealing offers a lower ohmic contact resistance (R_C) while FG annealing features a lower sheet resistance (R_{sheet}). Afterwards, a process using FG/N_2 two-step annealing is developed, and a subthreshold swing (SS) of 110 mV/dec, a transconductance (g_m) peak of 415 mS/mm, a record low drain-induced barrier lowing (DIBL) of 65 mV/V, and a record high power gain cutoff frequency (f_{max}) of 270 GHz are achieved on a 50-nm InAlN/GaN HEMT.

2.3 Experimental Details, Results and Discussions

The epitaxial layer used in this paper is grown by metal organic chemical vapor deposition (MOCVD) on 4-inch Si substrate. It consists of a 2-nm GaN cap layer, an 8-nm lattice-matched $In_{0.17}Al_{0.83}N$ barrier layer, a 1-nm AlN interlayer, a 15-nm GaN channel layer, a 4-nm $In_{0.12}Ga_{0.88}N$ back barrier layer, and a 2-μm undoped GaN buffer layer.

Device fabrication starts with mesa isolation using Cl_2-based inductively coupled plasma etching process. Ti/Al/Ni/Au stack is deposited and annealed to form alloyed ohmic contacts. Here a

N_2/FG two-step annealing is used for the InAlN/GaN HEMTs. Devices are annealed at 850˚C first in FG for 20s and then in N_2 for 20s. The ohmic contact rapid thermal annealing (RTA) process is carried out using Solaris 150 Rapid Thermal Processing System with a ramping rate of 50˚C/s. The system temperature accuracy and stability are both ± 2.5˚C and the temperature variation across the entire chamber is ± 2.5˚C. Following oxygen plasma treatment, a Ni/Au T-shaped gate with a gate width (W_g) of 2 × 20 μm is fabricated by electron beam lithography. The devices present a source-drain spacing (L_{sd}) of 1 μm, a gate-source spacing (L_{gs}) of 475 nm, and a gate footprint (L_g) of 50 nm, respectively. No passivation process is applied on the reported devices. The current-voltage (I–V) and capacitance-voltage (C-V) measurements are taken by using an Agilent B1500A semiconductor parameter analyzer.

To study the effect of forming gas and N_2 annealing on the material surface properties, two annealing conditions are adopted: (a) 850˚C for 40s in N_2; (b) 850˚C for 40s in forming gas (FG: 5% H_2 and 95% N_2). **Fig. 6** shows the X-ray photoelectron spectra (XPS) of Ga 3d core-level, N 1s core-level, and O 1s core-level taken from InAlN/GaN heterostructure with 2-nm GaN cap layer after N_2 and FG annealing, respectively. Relative percentage of fitting components is calculated from the ratio of the area under individual peak and total peak area of all components, as shown in **Table I**. In **Fig. 6(a)**, the Ga 3d spectra is resolved into three peaks. The fitting peaks at 19.96 ± 0.15, 18.19 ± 0.27, and 16.21± 0.20 eV binding energies are corresponding to Ga-O, Ga-N, and Ga-Ga bonds, respectively [73, 78, 79]. With N_2 annealing, the relative percentage of Ga-O and Ga-N bonds are 76% and 18%, which results in the ratio between Ga-O and Ga-N of 4.2. With FG annealing, the relative percentage of Ga-O and Ga-N bonds are 63% and 29%, resulting in the ratio between Ga-O and Ga-N of 2.2. The decrease of the Ga-O to Ga-N ratio shows that the native oxide is reduced after FG annealing. **Fig 6(b)** shows the N 1s core level spectra with three fitted peaks. The fitting peaks at 397.24 ± 0.02, 396.29 ± 0.07, and 392.69 ± 0.07 eV for Ga-N bond and two components for Ga LMM Auger features (Ga-LMM1 and GaN-LMM2, respectively) [80, 81]. The relative percentage of Ga-N for samples with N_2 annealing and FG annealing is 25% and 35%, respectively. Because the number of Ga atoms is fixed, the Ga-N bonds increasing means the Ga-O bonds decreasing. This also indicates that native oxide is reduced with FG annealing. **Fig. 6(c)** shows that the O 1s spectra have been fitted using two components (Ga-O bonds with fitting peak at 531.14 ± 0.23 eV and OH bonds with fitting peak at 532.14 ± 0.23 eV) [82, 83]. The relative percentages of Ga-O bonds are 55% (N_2 annealing) and 37% (FG annealing), a direct indication of the decreased Ga-O bonds with FG annealing. Therefore, the removal of native oxide using FG annealing is confirmed from these XPS measurement results and the schematic of FG annealing effect is shown in **Fig. 7**. Because material is exposed to the air, a native oxide layer (GaO_x) is formed on the surface of GaN cap layer [73, 74], as shown in **Fig. 7(a)**. The only difference between N_2 annealing and FG annealing is the existence of H_2 in the ambient. During the high temperature (850℃) annealing process, the H atoms in H_2 can combine with the O atom in the native oxide. The O atoms are extracted by the H atoms and thus the O vacancies are formed on the surface. N_2 in the FG can offer nitrogen atoms to fill the O vacancies. After removing native oxide, a new nitridation layer is formed on the surface. Hence, with FG annealing, the number of Ga-O bonds decreases while that of Ga-N bonds increases.

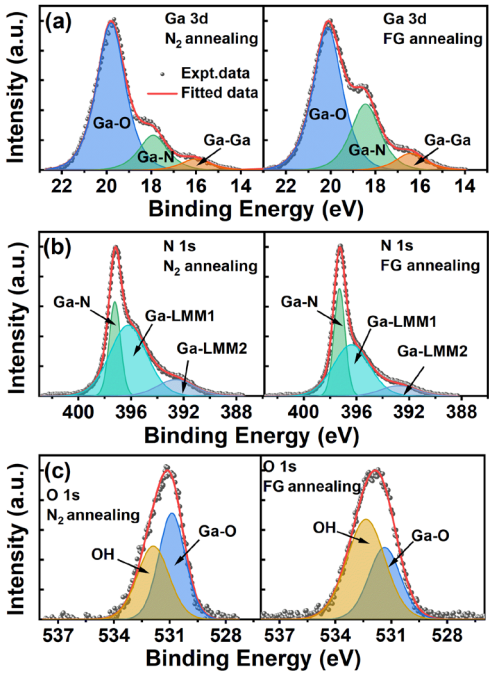

Fig. 6. XPS spectra of **(a)** Ga 3d core-level **(b)** N 1s core-level, and **(c)** O 1s core-level taken from InAlN/GaN heterostructure with 2-nm GaN cap layer after N_2 and FG annealing, respectively.

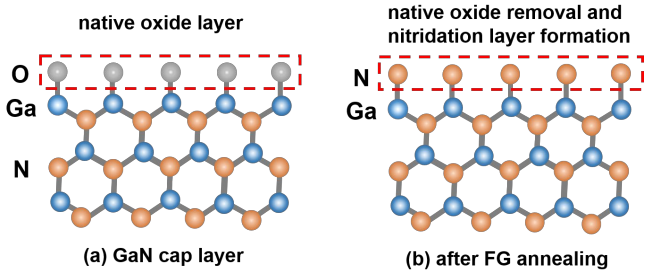

Fig. 7. Schematic of the GaN cap layer **(a)** before annealing and **(b)** after FG annealing.

Table I. Summary of fitting parameters for the Ga 3d core-level spectra, N 1s core level spectra, and O 1s (in **Fig. 1**) for samples after N_2 and FG annealing, respectively. Relative percentage of fitting components is calculated from the ratio of the area under individual peak and total peak area of all components.

Parameter		N2 annealing		FG annealing	
		Relative (%)	Peak (eV)	Relative (%)	Peak (eV)
Ga 3d	Ga-O	76	19.81	63	20.11
	Ga-N	18	17.91	29	18.46
	Ga-Ga	6	16.01	8	16.41
N 1s	Ga-N	25	397.21	35	397.26
	Ga-LMM1	61	396.21	53	396.36
	Ga-LMM2	14	392.61	12	392.76
O 1s	OH	45	531.91	63	532.36
	Ga-O	55	530.91	37	531.36

A. Electron density simulation

Fig. 8(a) and **(b)** show the valence band edge spectra taken from samples after N_2 and FG annealing, respectively. The position of valence band maximum (VBM) is determined from the extrapolation of the red solid lines [80, 81]. It turns out that VBM energy (E_v) lies at 2.11 (N_2 annealing) and 2.50 eV (FG annealing) below surface Fermi energy level (E_f). That means that the values of ($E_f - E_v$) are 2.11 (N_2 annealing) and 2.50 eV (FG annealing). Hence, the VBM positions can be obtained, confirming that E_f at the material surface is lifted up with FG annealing. The lifted E_f of GaN surface should come from the removal of native oxide and the new nitridation layer formation [84]. In GaN/InAlN/GaN heterostructure, the surface donor state is treated as the source of the two-dimensional electron gas (2DEG) electrons [85-87]. The lifted E_f on the surface means more surface electrons, which can be transferred to the 2DEG channel via the barrier electrical field, leading to the increased 2DEG electron density [86, 88]. The increased 2DEG electron density is beneficial for the improvement of the drain current and power density in GaN HEMTs. To obtain the detailed 2DEG electron density, the energy band structure can be simulated using the self-consistent Poisson-Schrodinger equations [85, 89, 90]. ENREF 2 **Fig. 8(c)** and **(d)** show the simulated energy band structure and electron concentration distribution as a function of distance (z) from the material surface for both samples. The ($E_f - E_v$) of 2.11 and 2.50 eV (obtained from valence band edge spectra) are used for the energy band simulation. Considering the GaN band gap of 3.4 eV [85, 91], ENREF 26 $E_c - E_f$ (E_c is the conductance energy minimum) of 1.29 and 0.9 eV are obtained. Hence, the surface barrier height (φ_b, here $\varphi_b = E_c - E_f$) can be determined to be 1.29 (N_2 annealing) and 0.9 eV (FG annealing), respectively. The reduction in surface barrier height can result in the increase of 2DEG density [92, 93]. As shown in **Fig. 8(c)** and **(d)**, the higher peak of the electron concentration (n) presents the increased 2DEG electron density. Here the 2DEG electron density (n_{2D}) can be extracted from the energy band simulation. n_{2D} of sample with FG annealing is 1.91×10^{13} cm^{-2}, which corresponds to 10% percent increase as compared to that of the sample with N_2 annealing (1.75×10^{13} cm^{-2}). Therefore, FG annealing can effectively decrease the surface barrier height and increase 2DEG electrons in InAlN/GaN heterostructure.

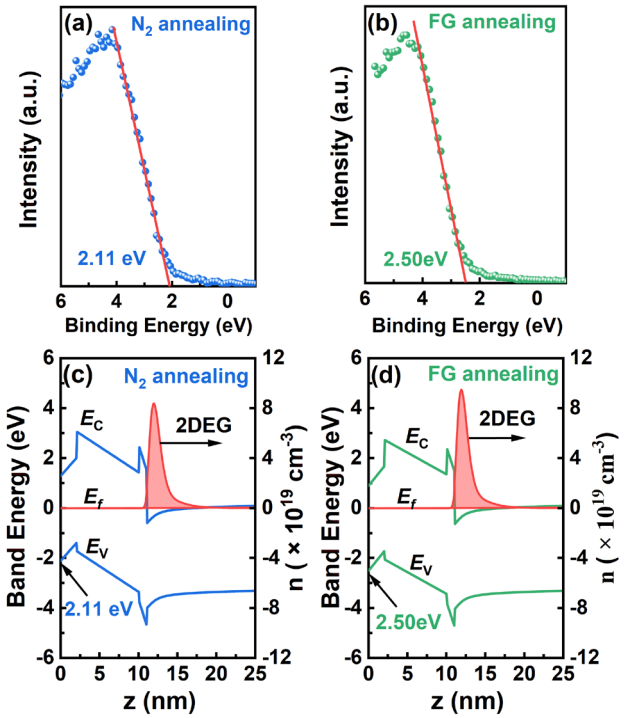

Fig. 8. Valence band edge spectra taken from samples after **(a)** N_2 and **(b)** FG annealing, respectively. Simulated energy bands and electron concentration distribution as a function of distance (z) from the material surface for samples after **(c)** N_2 and **(d)** FG annealing, respectively.

B. C-V measurement

To study the influence of trap electrons, the capacitance-voltage measurement with a frequency of 1MHz is performed as shown in **Fig. 9(a)**. The circular Schottky diodes are fabricated for the capacitance-voltage measurement and the device schematic is shown in the insert of **Fig. 9 (b)**. During the ohmic contact annealing, N_2 and FG annealing are applied on the two samples, respectively. The measured capacitance (C) under voltage of 0 V increases from 0.879 (C_{N2}, with N_2 annealing) to 0.976 μF/cm^2 (C_{FG}, with FG annealing). For the sample with N_2 annealing, the native oxide can introduce an oxide capacitance. The oxide capacitance (C_{ox}) is in series with the barrier capacitance (C_b), resulting in $1/C_{N2} = 1/C_{ox} + 1/C_b$ [94]. The removed native oxide with FG annealing leads to C_{FG}, with the value equal to C_b. Hence, the introduced C_{ox} can decrease the total capacitance. The 2DEG electron density can be calculated using the integration of capacitance-voltage curves and is shown below

$$n_{2d} = \frac{1}{eA}\int_{V_T}^{V} CdV\,, \qquad (1)$$

where e is the electron charge, and A is the schottky contact area. **Fig. 9(a)** shows the calculated n_{2d} as a function of voltage. At the voltage of 0 V, the 2DEG electron density are 1.82×10^{13} (N_2) and 2.15×10^{13} cm^{-2} (FG), respectively. The increased n_{2D} with FG annealing is consistent with the results from energy band simulations. Here both of the n_{2D} calculated with capacitance-voltage curves are higher than those determined from the simulated energy bands. Although the high frequency of 1MHz has been used during capacitance measurement, the influence of trap electrons

cannot be neglected. The trap electrons will contribute to the 2DEG electrons in the capacitance integration calculation method, leading to the increased calculated n_{2D}.

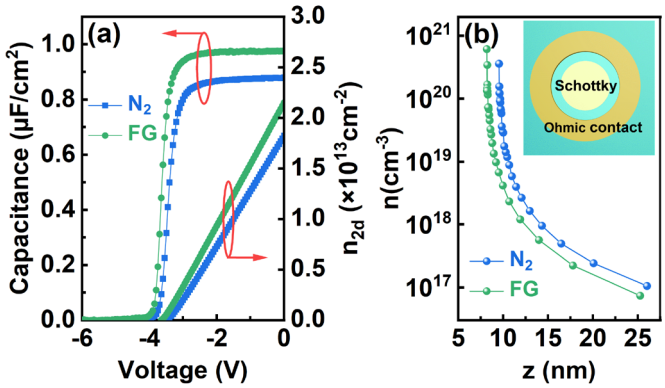

Fig. 9. (a) The capacitance measured at frequency of 1MHz (left), two-dimensional electron gas (2DEG) electron density n_{2D} (right) as a function of applied voltage, and **(b)** the electron concentration n as a function of the distance (z) from the surface for the samples with N_2 and FG annealing, respectively. Insert: the circular Schottky diode pattern for the capacitance measurement.

The electron concentration distribution versus the distance (z) from the material surface can also be calculated using the measured capacitance-voltage curves as follows [95]

$$n = -\frac{2}{e\varepsilon A^2}\cdot\frac{1}{d(1/C^2)/dV}, \qquad (2)$$

where ε is the dielectric constant of the barrier layer. As shown in **Fig. 9(b)**, the sample with FG annealing shows a rapid decrease with z. This decrease means that most of the 2DEG electrons are confined in the potential well and a thinner channel layer is formed with FG annealing. A thinner channel is easier to be modulated by the gate voltage. Hence a stronger electron confinement can effectively improve the gate control capacity, which is beneficial for decreasing the leakage current, improving on/off current ratio, reducing subthreshold swing, and suppressing the short-channel effect in GaN HEMTs.

In addition, to confirm the variation of 2DEG the electron system, Hall measurement (not shown) is carried out on the InAlN/GaN heterostructure with N_2 and FG annealing, respectively. The results show that n_{2d} increases from 1.60×10^{13} cm^{-2} (N_2 annealing) to 1.94×10^{13} cm^{-2} (FG annealing). Due to the improved surface properties, the 2DEG electron mobility (μ_{2d}) is also enhanced from 1242 cm^2/V·s (N_2 annealing) to 1358 cm^2/V·s (FG annealing), presenting a significant influence of annealing ambient on the InAlN/GaN HEMTs characteristics.

C. Ohmic contact resistance

Fig. 10(a) and **(b)** show the Ohmic contact resistance (R_C) and sheet resistance (R_{sheet}) for three types annealing conditions obtained using six sets of TLM patterns. The average values of R_C are 0.43 Ω·mm (N_2 annealing), 0.92 Ω·mm (FG annealing), and 0.49 Ω·mm (FG/N_2 annealing), respectively. The average values of R_{sheet} are 361 Ω/□ (N_2 annealing), 269 Ω/□ (FG annealing), and 288 Ω/□ (FG/N_2 annealing), respectively. N_2 annealing shows the lowest R_C and highest R_{sheet}, and FG annealing presents the opposite behavior. As discussed above, FG annealing can

effectively remove the native oxide and increase the 2DEG electron density, leading to the decrease of R_{sheet}. However, the increased R_C from FG annealing degrades the device performance. In order to benefit from the good material property due to FG annealing and the low R_C due to N_2 annealing, a FG/N_2 two-step annealing is applied and a compromised device performance is obtained.

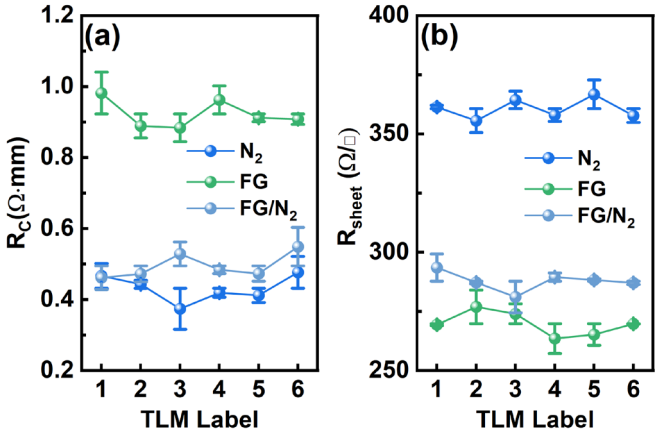

Fig. 10. (a) Ohmic contact resistance (R_C) and **(b)** sheet resistance (R_{sheet}) under N_2 annealing, FG annealing, and FG/N_2 two-step annealing with six sets of TLM patterns ("I" represents the error bar).

D. Device performance

Fig. 11(a) shows the output characteristic of the 50-nm InAlN/GaN HEMT with FG/N_2 annealing. **Fig. 11(b)** shows the transfer and gate current characteristics in semi-log scale at V_{ds} of 10 V and 3 V, respectively. At V_{ds} = 10 V, I_{on}/I_{off} ratio of ~10^6 and an SS of 110 mV/dec are observed. The DIBL of 65 mV/V is extracted at I_d = 10 mA/mm between V_{ds} = 10 V and V_{ds} = 3V. To the best of our knowledge, this is the lowest value among all GaN HEMTs on Si. The breakdown voltage (BV) is 20 V as determined at I_d = 1 mA/mm when V_{gs} is fixed at -8 V. **Fig. 11(c)** shows the extracted extrinsic transconductance (g_m) at V_{ds} of 10 V and a g_m peak ($g_{m,peak}$) of 415 mS/mm.

The RF measurement is taken with Anritsu MS4647B vector network analyzer configured to operate from 1 to 65 GHz. The network analyzer is calibrated using Line Reflect Match (LRM) calibration. On-wafer open and short structures are used to eliminate the effects of parasitic elements. After de-embedding, the current gain ($|h_{21}|^2$) and unilateral gain (U) as a function of frequency at V_{ds} = 10 V, V_{gs} = −3 V are plotted in **Fig. 11(d)**. f_T/f_{max} of 125/270 GHz is extracted using extrapolation of $|h_{21}|^2$ and U with a -20 dB/dec slope, resulting in $f_T \cdot L_g$ of 6.25 GHz·μm. **Fig. 12** shows the comparison of f_T/f_{max} of the InAlN/GaN HEMTs in this work with those from reported GaN HEMTs on Si. To the best of our knowledge, these devices with FG annealing present the highest f_{max} among the reported GaN HEMTs on Si.

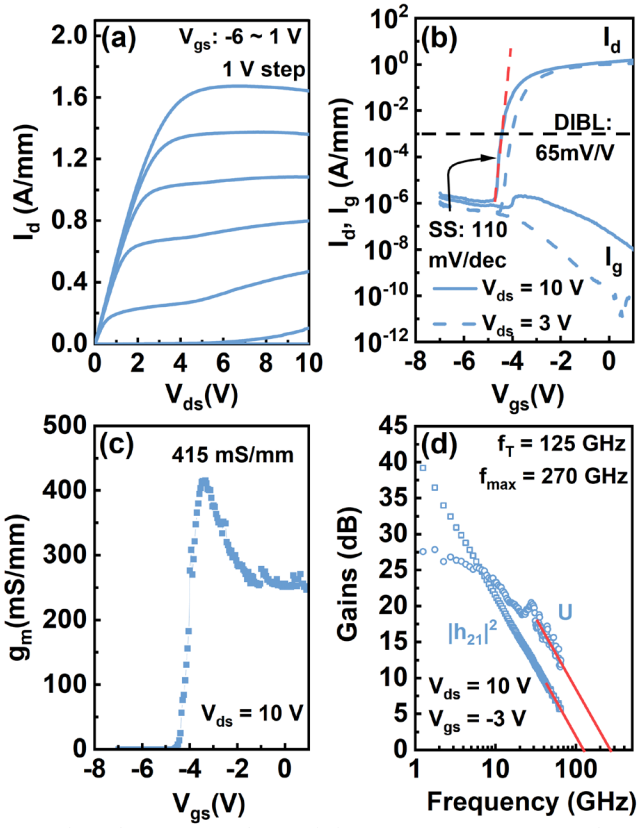

Fig. 11. (a) Output characteristic, **(b)** transfer and gate current characteristics at V_{ds} = 10 V, **(c)** transconductance, and **(d)** RF performance of 50-nm InAlN/GaN HEMT with FG/N_2 annealing.

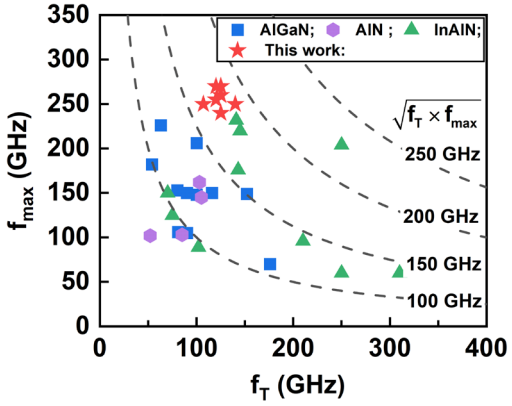

Fig. 12. Comparison of f_T/f_{max} of the InAlN/GaN HEMTs in this work with other reported GaN HEMTs on Si (AlGaN [24, 36, 39, 40, 42-44, 96-99], AlN [18, 54, 100], and InAlN [19, 20, 58, 59, 67, 69, 101, 102]).

2.4 Summary

In summary, the improved surface characteristic and 2DEG electron density with FG annealing are demonstrated. With the developed FG/N_2 ohmic contact annealing technology, the 50-nm InAlN/GaN HEMT on Si exhibits an average SS of 110 mV/dec, a record low DIBL of 65 mV/V, a $g_{m,peak}$ of 415 mS/mm, and a record high f_{max} of 270 GHz. This fabrication technology for GaN

HEMTs on Si yields excellent RF characteristics, which indicates the great application potential of GaN-on-Si for millimeter wave power amplifiers.

3. Sub-60mV/dec Switching achieved via rectangular gate

3.1 Introduction

A subthreshold swing (SS) of sub-60 mV/dec is for the first time observed in InAlN/GaN high electron mobility transistors (HMETs). With a 40-nm gate length (L_g), an average SS of 30 mV/dec over three orders of magnitude in drain current (I_d) and a minimum point-by-point SS of 15 mV/dec are achieved. The transistor body factor (m) of 4.99/6.98 (in forward/reverse sweep) determined from temperature-variation measurements indicates that the sub-60 mV/dec SS characteristic is not attributed to the negative capacitance effect. The negative differential resistance (NDR) of gate current (I_g) is observed and the hot electron transfer from channel to gate is believed to account for the sub-60 mV/dec SS characteristic. It is further confirmed by the fact that, SS decreases as drain-source voltage (V_{ds}) increases and L_g decreases. Due to the increased V_{ds} and decreased L_g, the channel lateral electric field is strengthened, leading to the hot electron formation and thus the enhanced effect of hot electron transfer on the SS. This sub-60 mV/dec SS characteristic in the nanoscale devices shows the great potential of the InAlN/GaN HEMTs to be applied in future logic switches.

3.2 Background

Boltzmann distribution dictates that, to affect an order of magnitude increase in the drain current, the gate voltage needs to change by at least 60 mV at 300 K [103-105]. This means that the subthreshold swing (SS) in conventional field effect transistors (FETs) cannot fall below 60 mV/dec at room temperature, which will hinder the devices for further low voltage/low power applications. Novel devices such as tunneling FETs [106, 107] and ferroelectric FETs [108, 109] have been demonstrated to break this SS limit with sub-60 mV/decade switching.

Due to the high electron velocity and large bandgap, gallium nitride high-electron-mobility transistors (HEMTs) have been demonstrated for the high-frequency and high-power applications in the last two decades [110-112]. InAlN/GaN metal-insulator-semiconductor HEMTs (MIS-HEMTs) with SS below 60 mV/dec have been reported by several groups [113-116]. There are several similar characteristics reported in these devices: 1) gate dielectrics are employed; 2) gate length (L_g) is 1~3 μm; 3) SS of sub-60 mV/dec is observed in forward sweep (from low to high) of gate-source voltage (V_{gs}).

In this work, we report for the first time that sub-60 mV/dec SS can be observed in GaN HEMTs without depositing gate dielectric. Different from current InAlN/GaN MIS-HEMTs, the SS of sub-60 mV/dec is observed in reverse sweep (from high to low) of V_{gs}. Because of the decreased SS as drain-source voltage (V_{ds}) increases and L_g decreases, the effect of the hot electron transfer from channel to gate on the sub-60 mV/dec SS characteristic is confirmed.

3.3 Experimental Details, Results and Discussions

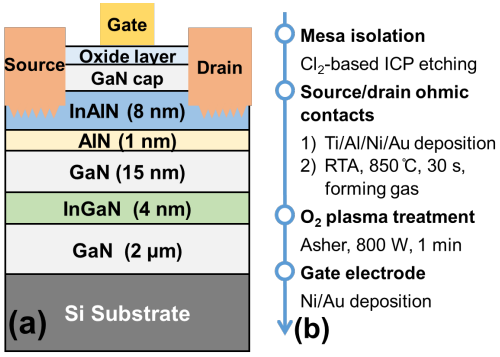

Fig. 13. **(a)** Schematic cross-section, and **(b)** process flow for the InAlN/GaN HEMT.

Fig. 13(a) shows the schematic cross-section of the fabricated InAlN/GaN HEMT on Si substrate. The epitaxial layer consists of a 2-µm undoped GaN buffer layer, a 4-nm $In_{0.12}Ga_{0.88}N$ back barrier layer, a 15-nm GaN channel layer, a 1-nm AlN interlayer, an 8-nm lattice-matched $In_{0.17}Al_{0.83}N$ barrier layer, and a 2-nm GaN cap layer. **Fig. 13(b)** displays the process flow for the InAlN/GaN HEMT. The device fabrication started with mesa isolation by Cl_2-based inductively coupled plasma (ICP) etching. Ti/Al/Ni/Au metal stack was then deposited and annealed at 850˚C for 30 s in forming gas (5% H_2, balanced with N_2) to form the alloyed ohmic contact. Subsequently, sample surface was blanket treated with oxygen plasma treatment to form an oxide layer on the whole material surface [70, 117]. Finally, gate electrodes with gate width (W_g) of 50 × 2 µm were defined using electron beam lithography followed by Ni/Au metal stack deposition. The devices with source-drain distances (L_{sd}) of 2 µm (L_g = 40, 70, 100, 150, and 300 nm) and 6 µm (L_g = 1, 2, 3 µm) are fabricated, respectively. The DC current-voltage (I–V) measurements were carried out by using an Agilent B1500A semiconductor parameter analyzer.

Fig. 14(a) exhibits the measured output characteristics of the InAlN/GaN HEMT with L_g = 40 nm under forward/reverse sweep of V_{ds}. **Fig. 14(b)** shows the measured transfer and gate current (I_g) characteristics in semi-log scales of the InAlN/GaN HEMT with L_g = 40 nm at V_{ds} = 10 V under forward/reverse sweep of V_{gs}. To determine point-by-point SS, the sweep step of V_{gs} is set at 5 mV. The on current (I_{on}), off current (I_{off}), on/off current (I_{on}/I_{off}) ratio, and I_g (at V_{gs} = -7 V) under forward/reverse sweep are 1.52/1.52 A/mm, $8.95\times10^{-7}/4.17\times10^{-7}$ A/mm, $1.69\times10^{6}/3.64\times10^{6}$, and $1.49\times10^{-6}/1.16\times10^{-6}$ A/mm, respectively. The extracted average SS value over three/four orders of magnitude in I_d is 118/30 mV/dec under forward/reverse sweep. The SS in reverse sweep is far below the thermal limit of 60 mV/dec, leading to an abrupt change in I_d. **Fig. 14(c)** presents the dependence of point-by-point SS as a function of I_d extracted from **Fig. 14(b)**. In the subthreshold region, the SS values under forward sweep are all above 60 mV/dec, while those under reverse sweep all fall below the thermal limit for over 3 decades of I_d. Under reverse sweep, a minimum point-by-point SS of 15 mV/dec is achieved.

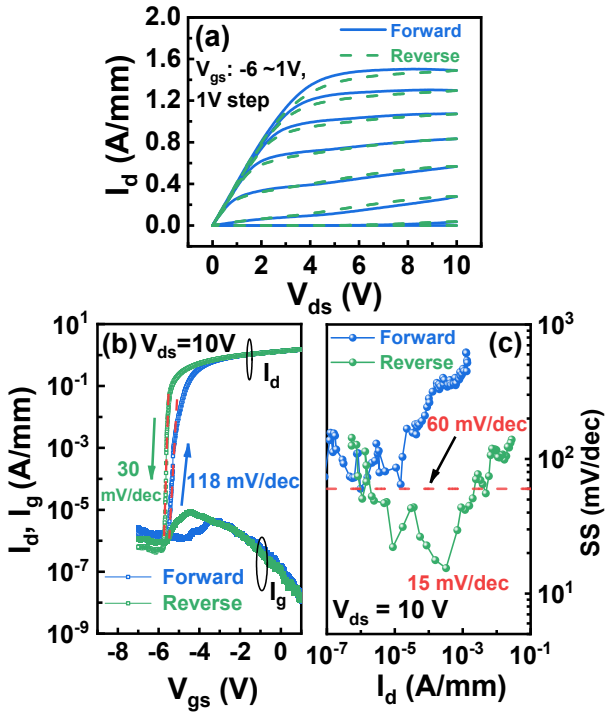

Fig. 14(a) Output characteristics of InAlN/GaN HEMT with L_g = 40 nm under forward/reverse sweep of V_{ds}; **(b)** Transfer and gate current characteristics of InAlN/GaN HEMT with L_g = 40 nm at V_{ds} = 10 V under forward/reverse sweep of V_{gs}; **(c)** Point-by-point SS as a function of I_d at V_{ds} = 10 V under forward/reverse sweep of V_{gs}.

The SS can be expressed as [104, 105, 113]

$$SS = \frac{\partial V_{gs}}{\partial(\log_{10} I_d)} = \frac{\partial V_{gs}}{\partial \psi_s} \cdot \frac{\partial \psi_s}{\partial(\log_{10} I_d)} = mkT/q \times \ln(10), \qquad (1)$$

where ψ_s is the channel potential, k is the Boltzmann's constant, T is the temperature, q is the electron charge. $m = \partial V_{gs}/\partial \psi_s = 1 + C_s/C_{ins}$ is the body factor [104, 105, 113], where C_s and C_{ins} are the GaN channel capacitance and the insulator capacitance, respectively. Here C_{ins} in GaN HEMT is the capacitance between gate electrode and GaN channel. As shown in Fig. 1(a), C_{int} is derived from the stack of AlN interlayer, InAlN barrier layer, GaN cap layer, and the oxide layer. In conventional FETs, m generally exceeds one, thus SS features a lower limit of 60 mV/dec at m = 1 [104, 105, 113]. When m < 1, device would present a negative capacitance (NC) effect [104, 105, 113]. To obtain the value of m, the transfer and gate current characteristics of InAlN/GaN HEMT with L_g = 40 nm under different temperatures (T) are taken at V_{ds} = 10 V under forward and reverse sweeps of V_{gs}, as shown in **Fig. 15(a)** and **(b)**. **Fig. 15(c)** shows the dependence of extracted average SS on T under forward/reverse sweep. As T elevates, the average SS increases and under reverse sweep, the average SS rises above 60 mV/dec at T > 333 K. **Fig. 15(d)** shows the measured and fitted $SS/(k/q \times \ln(10))$ results extracted from **Fig. 15(c)**. Based on (1), m value of 4.99/6.98 is obtained under forward/reverse sweep. This indicates the sub-60 mV/dec SS characteristic under reverse sweep is not due to the NC effect.

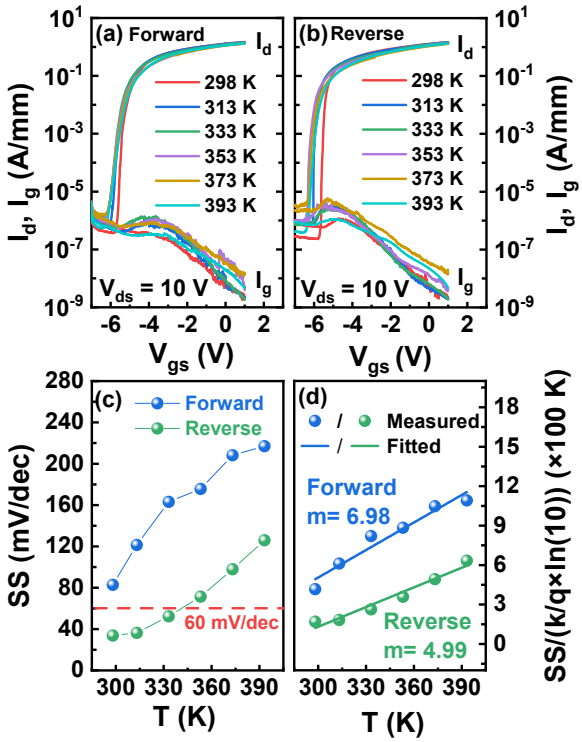

Fig. 15 Transfer and gate current characteristics in semi-log scales at V_{ds} = 10 V of InAlN/GaN HEMT with L_g = 40 nm under different temperatures **(a)** under forward sweep, and **(b)** under reverse sweep of V_{gs}, respectively. **(c)** The SS as a function of temperature (T) under forward/reverse sweep of V_{gs}. **(d)** The measured and fitted SS/(k/q×ln(10)) results as a function of temperature (T) under forward/reverse sweep of V_{gs}.

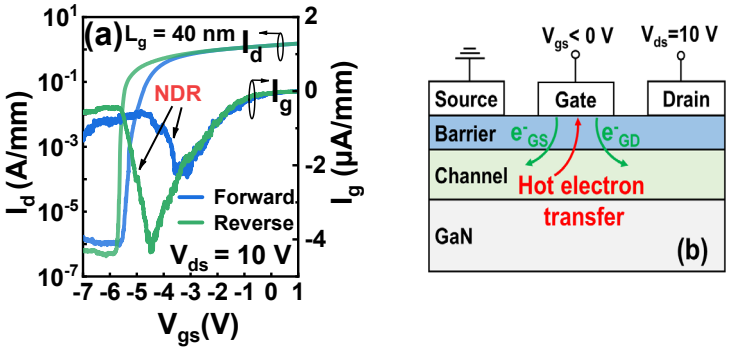

Fig. 16 (a) The transfer characteristics in semi-log scales and the gate current characteristics in linear scales at V_{ds} = 10 V under forward/reverse sweep of V_{gs}. **(b)** Schematic of the hot electron transfer at V_{gs} < 0 V and V_{ds} = 10 V. Arrows are the electron flow direction.

Another possible reason for the acquisition of sub-60 mV/dec SS is the hot electron transfer from channel to gate [118, 119]. **Fig. 16(a)** shows the transfer characteristics in semi-log scales and the gate current characteristics in linear scales of InAlN/GaN HEMT with L_g = 40 nm. Herein, the I_g-V_{gs} curves present a negative differential resistance (NDR) at $I_d \geq$ 10 mA/mm (device turns on) but before its transition to saturation. **Fig. 16(b)** shows the schematic of the hot electron transfer in InAlN/GaN HEMTs at V_{gs} < 0 V and V_{ds} = 10 V. Under negative V_{gs}, the electrons flow from gate to source (e^-_{GS}) and drain (e^-_{GD}), which contributes to I_g. Hence, I_g is negative and should increase with V_{gs}. However, due to the short gate length (L_g = 40 nm), the lateral electric field under the gate region is very high. The channel electrons under the gate region can obtain high energy from

the strong lateral electric field and possibly transfer through the InAlN barrier to gate. The electron transfer from channel to gate is in opposite direction to the electron flow of both e^-_{GS} and e^-_{GD}, leading to the decrease of I_g with increased V_{gs} and observation of NDR.

Under forward sweep (**Fig. 16(a)**), as V_{gs} increases from -7 V to -5 V ($I_d \leq 10$ mA/mm), the channel does not turn on and few electrons are accumulated under the gate channel. Hence the possibility of electron transfer to gate is low and I_g increases with V_{gs}. When channel turns on at $V_{gs} \geq$ -5 V ($I_d \geq 10$ mA/mm), the electron density in the channel increases with V_{gs}. The channel electrons under the gate region can obtain high energy from the strong lateral electric field and the hot electrons can transfer through the InAlN barrier to gate. Then I_g-V_{gs} presents an NDR. Since the channel has been turned on, the hot electron transfer does not affect the subthreshold characteristic. Therefore, SS is not affected. When V_{gs} further increases to the saturation region ($V_{gs} \geq$ -3 V and $I_d \geq 0.5$ A/mm), more channel electrons are accumulated under the gate region, which will decrease the resistance of the gate channel and the lateral electric field. The electrons cannot obtain enough energy. Hence no electrons can be transferred to gate and I_g increases with V_{gs}.

The electron transfer under reverse sweep is almost the same with that under forward sweep. In saturation region (when V_{gs} decreases from 1 V to -4.5 V with $I_d \geq 0.5$ A/mm), the electron density under the gate region is high and the lateral electric field under the gate region is not high enough. Hence no electron can be transferred to gate. When V_{gs} decreases below -4.5 V ($I_d < 0.5$ A/mm), due to the decrease of electron density, the lateral electric field under the gate region increases giving rise to the formation of hot electrons and transfer of hot electrons. Then NDR is observed when V_{gs} is in the range of -4.5 to -5.5 V (at V_{gs} = -5.5 V the channel begins to turn off). Under reverse sweep, the electron transfer starts before device turns off and can play a significant influence on the subthreshold characteristic. The transferred hot electrons not only can result in the decreased number of channel electrons (namely, decrease I_d), but also can add negative gate potential to deplete the channel electrons. Hence, a smaller gate voltage is needed to turn off the channel. Based on SS = $\partial V_{gs}/\partial(\log_{10}(I_d))$, a smaller V_{gs} causes a deep SS.

To verify this explanation, the transfer and gate current characteristics of the InAlN/GaN HEMT with L_g = 40 nm at different V_{ds} (V_{ds} increases from 1 V to 10 V with 1 V step) were measured, as shown in **Fig. 17(a)** and **(b)**. It is observed that the SS decreases with increased V_{gs} in both sweep directions. The NDR is observed when V_{ds} is larger than 5 V, and is more pronounced with increased V_{ds}, which presents a good consistency with the decreased SS with increased V_{ds}. **Fig. 17(c)** shows the extracted average SS as a function of V_{ds}. It is shown that SS decreases with increased V_{ds} in both sweep directions. Under forward sweep, SS decreases from 164 mV/dec (at V_{ds} = 1V) to 118 mV/dec (at V_{ds} = 10 V). Under reverse sweep, SS decreased from 161 mV/dec (at V_{ds} = 1 V) to 30 mV/dec (at V_{ds} = 10 V). The increased V_{ds} can enhance the channel lateral electric field. The higher electric field can promote to the hot electron transfer and results in a more significant NDR. Therefore, the SS decreases with increase in V_{ds}.

Fig. 17(d) shows the measured transfer and gate current characteristics of the InAlN/GaN HEMTs with different L_g at V_{ds} = 10 V under reverse sweep of V_{gs}. The NDR of I_g-V_{gs} curve is only observed when L_g < 100 nm. **Fig. 17(e)** shows the extracted average SS as a function of L_g. When L_g decreases from 3 μm to 40 nm, SS significantly decreases and falls below 60 mV/dec when L_g < 100 nm. As L_g scales down, the lateral electric field under the gate region increases and

hot electrons are more likely to be created, leading to the hot electrons transfer and the decreased SS. **Fig. 5(f)** shows the statistical distribution of SS for the fabricated 16 individual devices with SS below 60 mV/dec. The gate lengths of these devices are all below 100 nm, corroborating the effect of the hot electron transfer behavior on SS in the down-scaled devices.

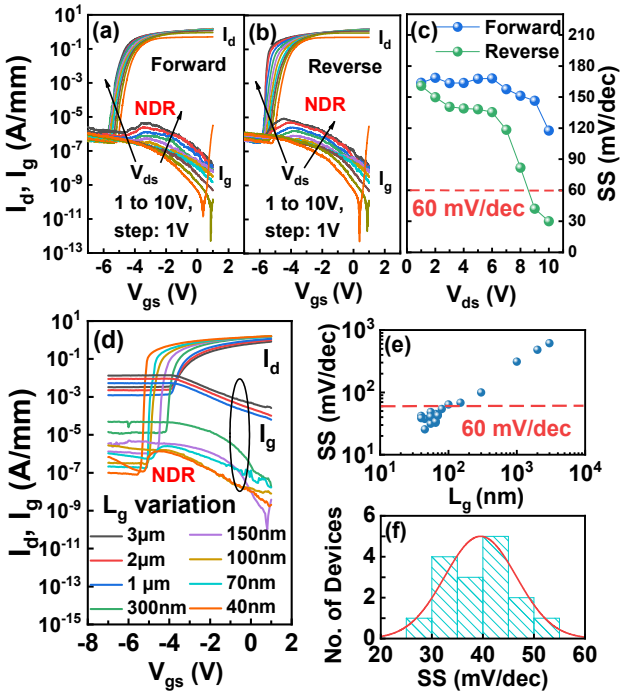

Fig. 17 (a)The transfer and gate current characteristics in semi-log scales of InAlN/GaN HEMT with L_g = 40 nm at different V_{ds} (here V_{ds} increases from 1 V to 10 V with 1 V step and arrows are the V_{ds} increase directions.) under forward sweep, and **(b)** under reverse sweep of V_{gs}. **(c)** The average SS as a function of V_{ds} under forward/reverse sweep of V_{gs}. **(d)** The transfer and gate current characteristics in semi-log scales of the InAlN/GaN HEMTs with different L_g at V_{ds} = 10 V under reverse sweep of V_{gs}. **(e)** The average SS as a function of L_g. When L_g < 100 nm, the SS falls below 60 mV/dec. **(f)** The statistical distribution of SS for the fabricated 16 individual devices with SS below 60 mV/dec.

3.4 Summary

In summary, an average SS of 30 mV/dec over three orders of magnitude in I_d and a minimum point-by-point SS of 15 mV/dec were achieved on the InAlN/GaN HEMT with a gate length of 40 nm. It is found that SS decreases as V_{ds} increases and L_g decreases. The decrease of SS as the device dimension scales down is attributed to the hot electron transfer from channel to gate. This study shows the great potential of the InAlN/GaN HEMTs to be applied in future logic switches.

4. High performance GaN MISHEMTs using high quality ZrO_2

4.1 Introduction

We present the electrical properties of the InAlN/GaN metal-insulator-semiconductor high-electron-mobility transistor (MISHEMT) with plasma enhanced atomic layer-deposited ZrO_2 as the gate dielectric. The InAlN/GaN MISHEMT with an on/off current (I_{on}/I_{off}) ratio of 1.46×10^9 as well as a subthreshold swing (SS) of 85 mV/dec was achieved. The interface trap density (D_{it}) decreased from 1.16×10^{12} $eV^{-1}cm^{-2}$ (at E_C-E_T = 0.26 eV) to 4.68×10^{11} $eV^{-1}cm^{-2}$ (at E_C-E_T = 0.40

eV), indicating a good interface property. This study suggests a feasible way for the application of ZrO_2/InAlN/GaN MISHEMTs.

4.2 Background

InAlN/GaN high electron mobility transistor (HEMT) has been demonstrated to be promising candidates for its high-power and high-frequency applications.[20, 70, 120-122] Due to the strong spontaneous polarization and ultra-thin barrier layer, InAlN/GaN HEMT has great potential to achieve further improved device performances compared with AlGaN/GaN HEMT. However, the ultra-thin InAlN barrier layer of InAlN/GaN HEMT often leads to non-negligible gate leakage current (I_g), which is detrimental to the device performances, such as on/off current ratio (I_{on}/I_{off}) and subthreshold swing (SS). Employing metal-insulator-semiconductor high-electron-mobility transistor (MISHEMT) can effectively reduce gate leakage and improve the device DC performances.[77, 123] Several kinds of dielectrics have been used as the gate insulator materials for InAlN/GaN MISHEMT, such as Al_2O_3,[124, 125] SiO_2,[121, 126, 127] MgCaO,[123] Y_2O_3, [128, 129] $GdScO_3$,[130] $HfZrO_2$,[131] La_2O_3,[132] and SiN,[133] etc. G. Dutta *et al* observed a positive threshold voltage shift in the InAlN/GaN MISHEMT with reactive-ion-sputtered Al_2O_3 as a gate dielectric, indicating the presence of net negative charge at oxide-semiconductor interface.[125] H.-S. Lee *et al* reported that the gate leakage current in the InAlN/GaN MISHEMT is ~10^{-10} A/mm owing to the use of a SiO_2 gate dielectric.[121] H. Zhou *et al* demonstrated high-performance InAlN/GaN MISHEMT using atomic-layer-epitaxy crystalline $Mg_{0.25}Ga_{0.75}O$ gate dielectric. An off-state leakage current of 3×10^{-13} A/mm, I_{on}/I_{off} ratio of 4×10^{12}, SS of 62 mV/dec were realized.[123] Among these gate dielectrics, the high-k gate dielectrics are desired to achieve an excellent gate control over the channel. Most of the conventional dielectric materials (e.g., Al_2O_3, SiO_2, and SiN) are with relatively low dielectric contact and not ideal. In contrast, ZrO_2, with a large band gap (Eg ~ 7.8 eV) and a high dielectric constant (ε ~16-23), emerges as an attractive gate dielectric.[134, 135] It has been demonstrated that using the ZrO_2 gate dielectric can achieve ultra-low gate leakage and excellent gate control over the channel in AlGaN/GaN MISHEMT.[136-139] In InAlN/GaN MISHEMT, a few works on the ZrO_2 gate dielectric deposited by metal-organic chemical vapor deposition (MOCVD) or atomic layer deposition (ALD) have also been investigated.[130, 135, 140-144] However, to the best of our knowledge, few reports on the InAlN/GaN MISHEMT using ZrO_2 gate dielectric show significantly enhanced electrical performances. Therefore, further improving device performances of InAlN/GaN MISHEMT using ZrO_2 as the gate dielectric is still desired.

Here, the electrical properties of the InAlN/GaN MISHEMT with the ZrO_2 gate dielectric were studied. With ZrO_2 as the gate dielectric prepared by plasma enhanced atomic layer deposition (PEALD) method, InAlN/GaN MISHEMT exhibits excellent device performances with an I_{on}/I_{off} ratio of ~10^9, a SS of 85 mV/dec, and a low interface state density ranging from 4.68×10^{11} $eV^{-1}cm^{-2}$ to 1.16×10^{12} $eV^{-1}cm^{-2}$.

4.3 Experimental Details, Results and Discussions

The InAlN/GaN heterostructure epitaxial layer structure was grown on a Si substrate by metalorganic chemical vapor deposition (MOCVD). The epitaxial structure, as shown in Fig.

18(a), consists of a 2 nm GaN cap layer, an 8 nm $In_{0.17}Al_{0.83}N$ barrier layer, a 1 nm AlN interlayer, a 15 nm GaN channel layer, a 4 nm $In_{0.12}Ga_{0.88}N$ back barrier layer, and a 2 µm undoped GaN buffer layer. The device process started with mesa isolation by inductively coupled plasma reactive ion etching (ICP-RIE). Then the source and drain ohmic contacts were formed by depositing Ti/Al/Ni/Au multilayer and annealing at 850˚C for 40s in N_2. The transmission-line measurements revealed an ohmic contact resistance of 0.48 Ω·mm. Finally, Ni/Au metal stack was used as the gate contact. For InAlN/GaN HEMT, gate was immediately fabricated after S/D contact lift-off. For the InAlN/GaN MISHEMT, prior to the gate metal deposition, an 8 nm ZrO_2 was deposited as gate dielectric by plasma enhanced atomic layer deposition (PEALD). Bis (methyl-η5−cyclopentadienyl) methoxymethylzirconium (ZRCMMM) and O_2 were used as Zr source and oxygen source, respectively. The oxygen reactant gas was introduced in plasma state at a flow rate of 60 sccm. The Zr precursor was introduced into the reaction chamber using argon (Ar) carrier gas at a flow rate of 100 sccm. The ICP power of 400 W was used. ZrO_2 film was deposited at 130˚C and the deposition rate was 0.5Å/cycle. As shown in **Fig. 18(a)**, for both samples, the gate-drain distance L_{GD}, gate-source distance L_{GS}, gate length L_G, and the gate width W_G was respectively 5 µm, 5 µm, 2 µm, and 50 µm. The current-voltage (I–V) measurements were carried out at room temperature using an Agilent B1500A semiconductor parameter analyzer. The capacitance-voltage (C-V) measurements were carried out at room temperature using an Agilent B1520 A semiconductor parameter analyzer at 1MHz.

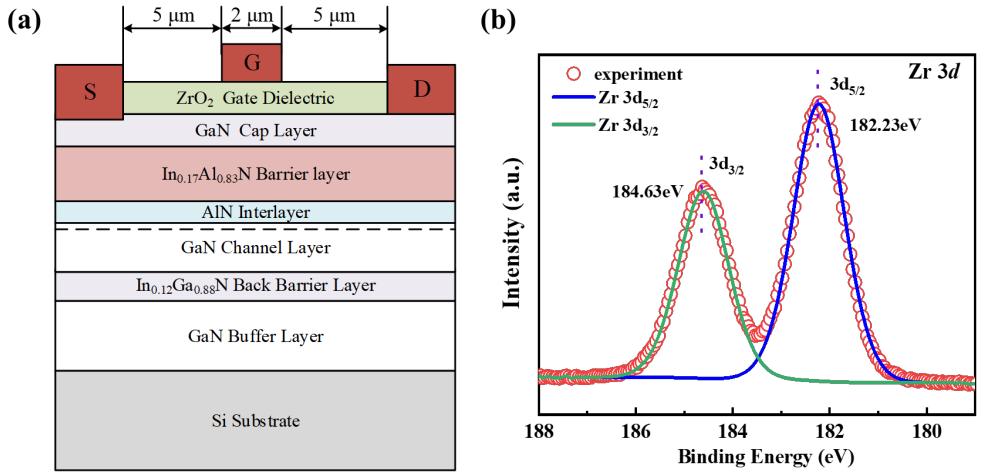

Fig. 18 (a) Schematic of the InAlN/GaN MISHEMT with 8-nm ZrO_2 as the gate dielectric; (b) the XPS spectrum of Zr 3d core level of the 2-nm ZrO_2 on InAlN/GaN MISHEMT.

Fig. 18 (b) shows the measured X-ray photoelectron spectroscopy (XPS) spectrum of Zr 3d core level of the 2-nm ZrO_2 on InAlN/GaN MISHEMT. Zr $3d_{5/2}$ and Zr $3d_{3/2}$ spin orbit split components are observed for Zr 3d spectrum.[27] Doublet peaks with the centered binding energy of 182.23 eV (Zr $3d_{5/2}$) and 184.63 eV (Zr $3d_{3/2}$) are extracted, respectively. The Zr $3d_{5/2}$ originates from the oxidation state Zr^{+4} and its binding energy is close to the reported value,[145, 146] which confirms that the gate dielectric is ZrO_2.

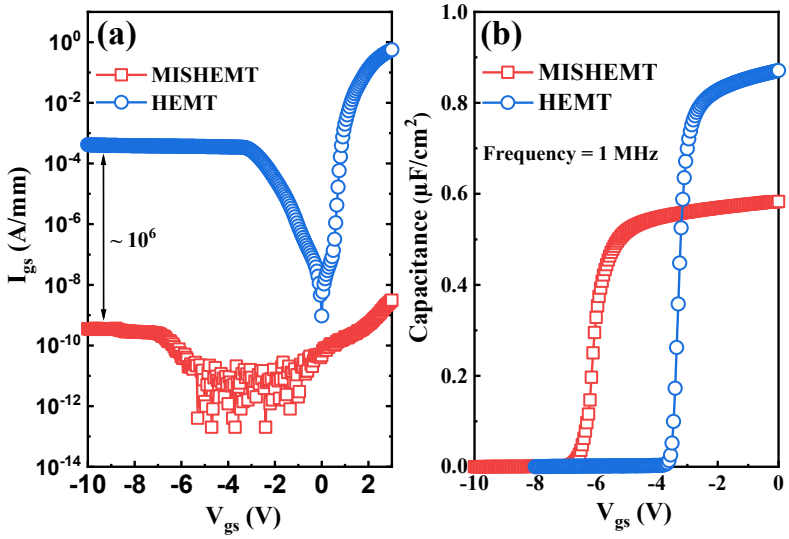

Fig. 19 (a) the gate-source current I_{gs} and (b) the gate diode capacitance as a function of the gate-source voltage V_{gs} for both samples.

The gate diode I_{gs}-V_{gs} curves of both samples were measured in **Fig. 19 (a)**. With the ZrO_2 gate dielectric, the reverse gate leakage current at V_{gs} = -10 V decreases from 4.17×10^{-4}A/mm (HEMT) to 3.57×10^{-10}A/mm (MISHEMT) (more than six orders of magnitude difference). The gate diode C-V measurement is shown in **Fig. 19 (b)**. It's known that $1/C_{MISHEMT} = 1/C_{HEMT} + 1/C_{ZrO2} = 1/C_{HEMT} + d_{ZrO2}/\varepsilon_0\varepsilon_{ZrO2}$,[94] where $C_{MISHEMT}$, C_{HEMT}, and C_{ZrO2} represent the capacitances of the MISHEMT gate diode, HEMT gate diode, and the ZrO_2 gate dielectric, respectively. d_{ZrO2} is the ZrO_2 thickness, ε_0 is the vacuum dielectric permittivity, ε_{ZrO2} is the ZrO_2 dielectric constant. d_{ZrO2} was measured by Ellipsometer and confirmed to be 8 nm on a Si test sample which is placed near the InAlN/GaN sample during the ALD ZrO_2 deposition. With the measured capacitance at V_{GS} = 0 V, ε_{ZrO2} of 16 were determined.

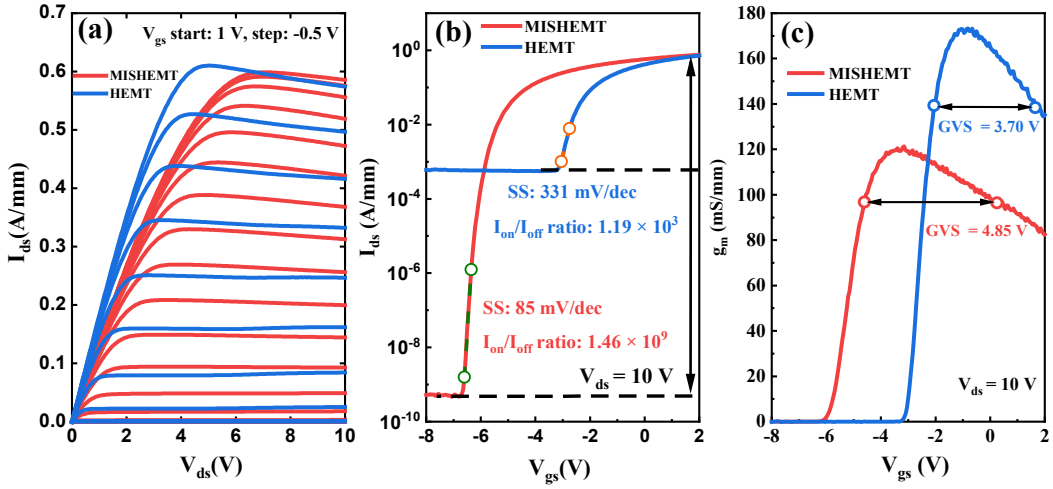

Fig. 20. Measured (a) *I-V* characteristics, (b) transfer curves, and (c) extrinsic transconductance curves of the both samples.

The I_{ds}-V_{ds} characteristics and transfer curves at the drain-source voltage V_{ds} = 10 V are shown in **Fig. 20 (a) and (b)**. The low maximum drain current is due to the material degradation during the device process. The device on-resistance (R_{on}) extracted at V_{gs} = 0 V and V_{ds} between 0 V and 0.5 V increased from 5.63 Ω·mm (HEMT) to 7.25 Ω·mm (MISHEMT). Because the V_{ds} is small and V_{gs} is 0 V, the influence of the drain voltage on the gate channel can be ignored, and the gate channel part is treated as the same with the parasitic access part. By subtracting the influence of the ohmic contact resistance (R_C = 0.48 Ω·mm), the sheet resistance R_{sh} can be extracted using $R_{sh} = R_{on}/L_{sd}$, where L_{sd} is the drain-source distance. It is shown that the ZrO_2 deposition increased the sheet resistance form 389 Ω/□ (HEMT) and 524 Ω/□ (MISHEMT). By the integration of the *C*-*V* curves, the two-dimensional electron gas (2DEG) electron density (n_0) at V_{gs} = 0 V can be obtained. n_0 in MISHEMT was 2.08 × 10^{13} cm^{-2}, which was 23% higher than that value of 1.69 × 10^{13} cm^{-2} in HEMT. The increased electron density was also observed in SiO_2/AlGaN/GaN MISHEMT by M. Marso *et al* [147]. The increase of the sheet carrier concentration by the ZrO_2 deposition is attributed to the reduction of the surface states that can trap electrons or to the trapping of a positive charge at the ZrO_2/GaN interface that neutralizes the fixed polarization charge [147]. The electron mobility (at V_{gs} = 0 V and V_{ds} = 0.5 V) can be calculated using $R_{sh} = 1/(n_0 q \mu)$. which was 950 $cm^2/(V \cdot s)$ in HMET and 573 $cm^2/(V \cdot s)$ in MISHEMT, respectively. It is confirmed that the ZrO_2 layer decreased the electron mobility, which caused the increase of the sheet resistance and R_{on} in MISHEMT. Due to the thin InAlN barrier layer, in ZrO_2/InAlN/GaN MISHEMT, the interfacial charge between the ZrO_2 and GaN cap layer can introduce the remote interfacial charge scattering [148-150], which decreased the two-dimensional electron gas (2DEG) electron mobility and increased the device on-resistance. The transfer curves reveal that the I_{on}/I_{off} ratio increases from 1.19 × 10^3 (HEMT) to 1.46 × 10^9 (MISHEMT), and the SS reduces from 331 mV/dec (HEMT) to 81 mV/dec (MISHEMT), indicating the excellent gate control capability and switching characteristics of InAlN/GaN MISHEMT. **Figure 20 (c)** shows the extrinsic transconductance g_m as a function of V_{GS} at V_{DS} = 10 V. The g_m curves of both transistors show a decline after reaching a maximum as the gate voltage increases. This decline represents the degradation of the device linearity. The InAlN/GaN MISHEMT shows a gradual decline, an indication of better linearity. To quantitatively compare the linearity performance between the MISHEMT and the conventional HEMT, the gate-voltage swing (GVS) can be obtained (the GVS is defined as the range of the gate voltage where the g_m remains within 20% drop of its maximum value[151, 152]). The GVS for the MISHEMT and the HEMT are determined to be 4.80 V and 3.75 V, respectively. This remarkable improvement in GVS (28% increase) implies device linearity enhancement of the MISHEMT.

The gate diode capacitance of the InAlN/GaN MISHEMT under difference frequencies (1kHz to 1 MHz) were measured shown in **Fig. 21(a)**. The small frequency dispersion of capacitance indicates a good interface quality with lower interface trap density. The interface trap state density D_{it} were extracted from the measured equivalent parallel conductance G_P of as a function of bias voltage and frequency (shown in **Fig. 21(b)**). The conductance, which represents the loss mechanism due to interface trap capture and emission of carriers, is used to extract D_{it} according to[138, 153-155]

$$\frac{G_P}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2}, \qquad (1)$$

where $\omega = 2\pi f$, f is the measurement frequency, q is the electron charge, τ_{it} is the interface trap time constant. The measured conductance as a function frequency is plotted as

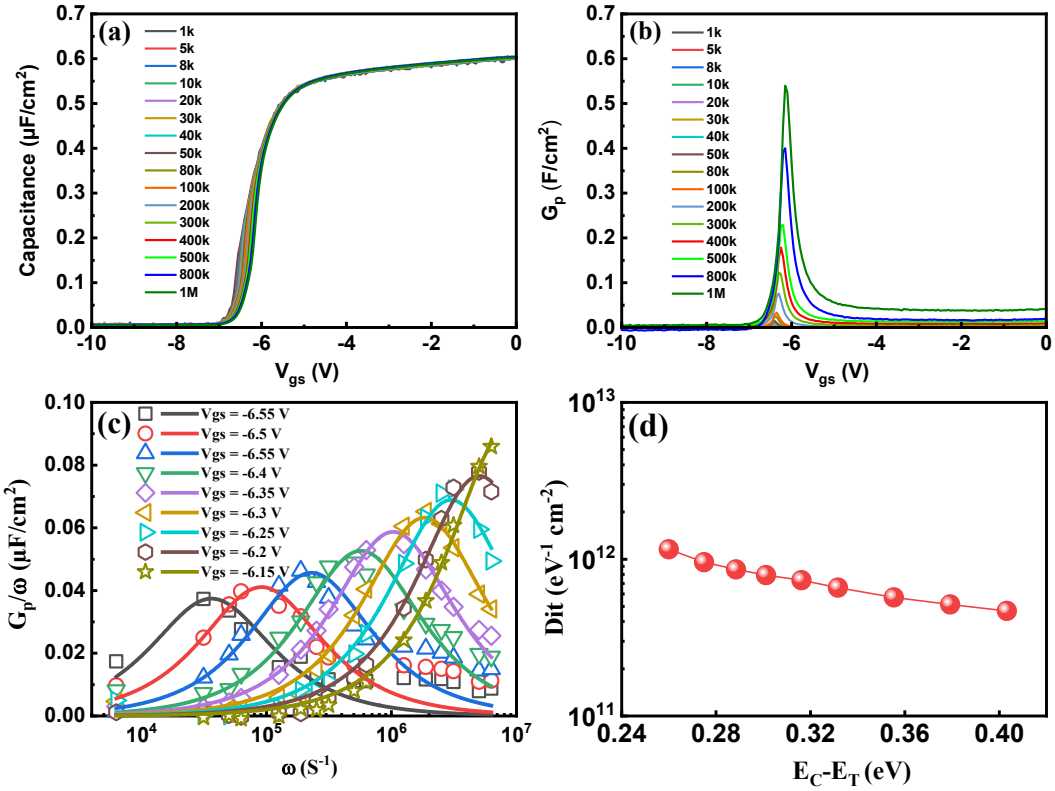

Fig. 21. The measured gate diode (a) capacitance and (b) the conductance G_P as a function of V_{GS} with different frequency (from 1 kHz to 1 MHz); (c) the measured G_P/ω versus ω with the fitting curves under different V_{gs}; (d) the interface trap density (D_{it}) as a function of the trap energy level below the GaN conductance band (E_C-E_T).

G_P/ω versus ω, shown in Fig. **21(c)**. G_P/ω has a maximum at $\omega = 1/\tau_{it}$ and at that maximum $D_{it} = 2\,G_P/q\omega$. Using (1) and the fitting curves in Fig. 4(c), the D_{it} and τ_{it} are extracted. The trap energy level below the GaN conductance band, E_C-E_T, was calculated by E_C-$E_T = k_B T \ln(\nu_{th}\sigma_n N_c \tau_{it})$.[154] Here the Boltzmann constant k_B of 1.38×10^{-23} J/K, electron temperature T of 300K, electron average thermal velocity ν_{th} of 2.6×10^7 cm/s, the capture cross section of the trap states σ_n of 3.4×10^{-15} cm^2, the density of states in the conduction band N_c of $4.3 \times 10^{14} \times T^{3/2}$ cm^{-3} were used.[153] The extracted Dit as a function of (E_C-E_T) were shown in Fig. 21(d). The Dit decreases from 1.16×10^{12} eV^{-1}cm^{-2} at E_C-E_T = 0.26 eV to 4.68×10^{11} eV^{-1}cm^{-2} at E_C-E_T = 0.40 eV. The low D_{it} showed a good interface quality, which is beneficial for the SS of the MISHEMT.

Table II shows the comparison of the key parameters of the reported GaN-based MISHEMTs with ZrO_2 gate dielectric. The application of ZrO_2 in AlGaN/GaN MISHEMTs have achieved a series of excellent results ($I_{on}/I_{off} \sim 10^{10}$, SS~66mV/dec, Dit $\sim 2 \times 10^{11}$ eV^{-1}cm^{-2}). But in InAlN/GaN MISHEMTs, there is still much room to improve. This work demonstrates the application of ZrO_2 in InAlN/GaN MISHEMT results in six orders of magnitude of reduction in I_{gs}, an I_{on}/I_{off} of 10^9 and SS of ~85 mV/dec, as well as a low D_{it} ranging from 4.68×10^{11} to 1.16×10^{12} cm^{-2} eV^{-1}.

Table II. Comparison of the key parameters in GaN-based MISHEMTs with ZrO_2 gate dielectric

Ref	Material	ZrO_2 Deposition (Method, Temperature, thickness)	ε_{ZrO2}	L_g/L_{sd} (μm)	Magnitude of reduction for I_{gs}	g_m (mS/mm)	I_{on}/I_{off}	SS	Dit (cm^{-2} eV^{-1})
[146]	AlGaN on Si	ALD, 200℃, 28nm	29	2/20	4 order, at V_{gs} = -6V	127	5×10^{10}	66	1.2×10^{12}
[156]	AlGaN on Si	ALD, 250℃, 10nm	17~19	1.9/–	4 order, at V_{gs} = -10V	138	~10^6	–	2×10^{11}
[157]	AlGaN on Si	ALD, 200℃, 23nm	–	1.5/7.5	–	135	~10^9	95	3×10^{12}
[158]	AlGaN on Si	ALD, 200℃, 21nm	25	–	4 order, at V_{gs} = -5 V	92.5	–	93	7×10^{12}
[159]	AlGaN on Sapphire	ALD, 250℃, 4nm	–	2/9	–	93	~10^9	–	–
[160]	InAlN on Sapphire	MOCVD, 450℃, 10nm	20~22	2/8	4 order, at V_{gs} = -10V	110	–	–	–
[141]	InAlN on Sapphire	ALD, 150℃, 10.5~11nm	–	2/8	4 order, at V_{gs} = -10V	–	–	–	–
[142]	InAlN on Sapphire	MOCVD, 450℃, 12~14nm	7.5~8	2/–	4 order, at V_{gs} = -10V	–	–	–	–
This Work	**InAlN on Si**	**ALD, 130℃, 8nm**	**16**	**2/12**	**6 order, at V_{gs} = -10V**	**121.3**	**1.46×10^9**	**85**	**$(4.68\sim11.6)\times10^{11}$**

4.4 Summary

In summary, using the ZrO_2 gate dielectric, the InAlN/GaN MISHEMT exhibited a I_{gs} of 3.57×10^{-10}A/mm, I_{on}/I_{off} of 1.46×10^9, and a SS of 85 mV/dec. The interface trap density D_{it} decreases from 1.16×10^{12} $eV^{-1}cm^{-2}$ (at E_C-E_T = 0.26 eV) to 4.68×10^{11} $eV^{-1}cm^{-2}$ (at E_C-E_T = 0.40 eV), indicating a good interface quality. This suggests a feasible way to utilize ZrO_2 as the gate dielectric in the InAlN/GaN MISHEMTs.

5. Downscaling behavior of our transistors down to Lg=20nm

5.1 Introduction

Due to the low cost and the scaling capability of Si substrate, InAlN/GaN high-electron-mobility transistors (HEMTs) on silicon substrate have attracted more and more attentions. Here, a high-performance 50-nm-gate-length InAlN/GaN HEMT on Si with a high on/off current (I_{on}/I_{off}) ratio of 7.28×10^6, an average subthreshold swing (SS) of 72 mV/dec, a low drain-induced barrier lowing (DIBL) of 88 mV, an off-state three-terminal breakdown voltage (BV_{ds}) of 36 V, a current/power gain cutoff frequency (f_T/f_{max}) of 140/215 GHz, and a Johnson's figure-of-merit (JFOM) of 5.04 THz·V is simultaneously demonstrated. The device extrinsic and intrinsic parameters are extracted using equivalent circuit model, which is verified by the good agreement between simulated and measured *S*-parameter values. Then the scaling behavior of InAlN/GaN HEMTs on Si is predicted using the extracted extrinsic and intrinsic parameters of devices with different gate lengths (L_g). It presents that a f_T/f_{max} of 230/327 GHz can be achieved when L_g scales down to 20 nm with the technology developed in the study, and an improved f_T/f_{max} of 320/535 GHz can be achieved on a 20-nm-gate-length InAlN/GaN HEMT with regrown ohmic contact technology and 30% decreased parasitic capacitance. This study confirms the feasibility of further improvement of InAlN/GaN HEMTs on Si for RF applications.

5.2 Background

InAlN/GaN high-electron-mobility transistors (HEMTs) on silicon substrate have attracted more and more attentions due to the low cost and the scaling capability of Si substrate[161-164]. L. Li *et al.* demonstrated a InAlN/GaN HEMT on Si with a gate length (L_g) of 55 nm and a source-drain spacing (L_{sd}) of 175 nm [72]using n^{++}-GaN regrowth source/drain contacts. The device presents a maximum drain current ($I_{d,\,max}$) of 2.8 A/mm, a peak extrinsic transconductance (g_m) of 0.66 S/mm, and a current/power gain cutoff frequency (f_T/f_{max}) of 250/204 GHz. H. Xie *et al.* reported that a record f_T of 310 GHz was achieved on a InAlN/GaN HEMT on Si with a 40-nm gate length [67]. P. Cui *et al.* demonstrated an 80-nm-gate-length InAlN/GaN HEMT on Si with a record high on/off current (I_{on}/I_{off}) ratio of 1.58×10^6, a steep subthreshold swing (SS) of 65 mV/dec, and a f_T of 200 GHz, resulting in a record high $f_T \times L_g$ = 16 GHz·μm [70]. N. Chowdhury *et al.* demonstrated a complementary logic circuit (an inverter) on a GaN-on-Si platform with a record maximum voltage gain of 27 V/V at an input voltage of 0.59 V with V_{DD} = 5 V [165]. H. Xie *et al.* reported an InAlN/GaN HEMT on Si with a f_T of 210 GHz and a three-terminal off-state breakdown voltage (BV_{ds}) of 46 V, leading to a record high Johnson's figure-of-merit (JFOM = $f_T \times BV_{ds}$) of 8.8 THz·V [69]. H. W. Then *et al* reported the high f_T/f_{max} of 190/300 GHz was achieved on the e-mode high-k InAlN/GaN transistor on 300 mm Si substrate [166].

However, to the best of our knowledge, the highest f_T/f_{max} of 454/444 GHz and 348/340 GHz were achieved on 20-nm-gate-length AlN/GaN HEMT [14] and 27-nm-gate-length InAlN/GaN HEMTs on SiC [15], respectively. Although excellent performances have been demonstrated, InAlN/GaN HEMTs on Si still presents much room to be improved compared with GaN HEMTs on SiC substrate. The InAlN barrier can be grown lattice-matched to GaN when the In component is 17%, which makes it easier grow than AlN on GaN [167]. The InAlN/GaN heterostructure also exhibits higher quantum well polarization-induced charge than AlGaN/GaN heterostructure, resulting in higher channel electron density and drain current [91, 168]. In addition, compared with AlGaN/GaN, a thinner InAlN barrier in InAlN/GaN HEMTs not only can offer higher frequency performance with an improved device transconductance, but also can suppress the short-channel effect with the reduced gate-to-channel distance [13, 31]. Hence, exploring the possible limiting factors of InAlN/GaN HEMTs on Si is significant to further improve the device performance. In this paper, high-performance InAlN/GaN HEMTs on Si are demonstrated. The extrinsic and intrinsic parameters of devices with different gate lengths are extracted and the scale behavior of InAlN/GaN HEMTs on Si is predicted. It presents that a f_T/f_{max} of 230/327 GHz can be achieved when L_g scales down to 20 nm with the technology developed in the study, and an improved f_T/f_{max} of 320/535 GHz can be achieved on a 20-nm-gate-length InAlN/GaN HEMTs with regrowth ohmic contact technology and 30% decreased parasitic capacitance. This confirms the feasibility of further improvement of InAlN/GaN HEMTs on Si for RF applications.

5.3 Experimental Details, Results and Discussions

Experiment

Figure 22(a) shows the used lattice-matched $In_{0.17}Al_{0.83}N$/GaN heterostructure, which is grown on a Si substrate by metalorganic chemical vapor deposition (MOCVD). The epitaxial layer structure consists of a 2-nm GaN cap layer, an 8-nm $In_{0.17}Al_{0.83}N$ barrier layer, a 1-nm AlN interlayer, a 15-nm GaN channel layer, a 4-nm $In_{0.12}Ga_{0.88}N$ back-barrier layer, and a 2-μm undoped GaN buffer layer [169]. The electron sheet concentration and electron mobility measured by Hall measurements were 2.28×10^{13} cm^{-2} and 1205 $cm^2/V{\cdot}s$, respectively.

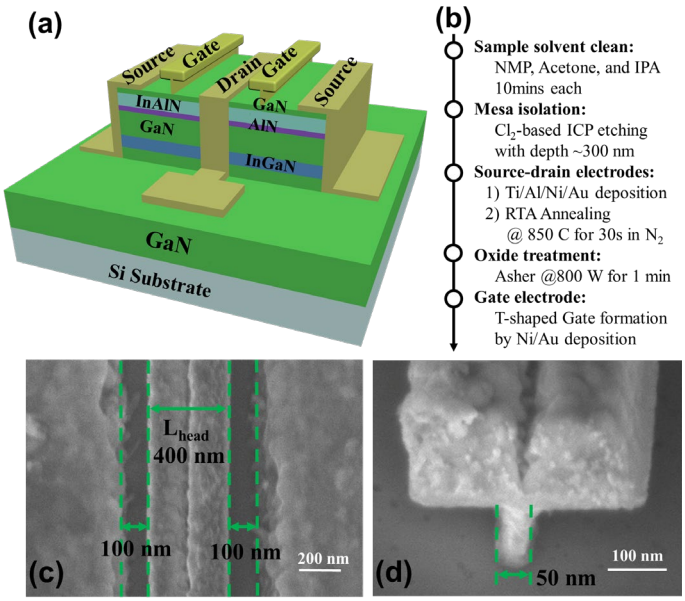

Figure 22. (a) Schematic of fabricated InAlN/GaN HEMT; **(b)** Detailed device fabrication steps; **(c)** a plan-view scanning electron microscopy (SEM) image of the InAlN/GaN HEMT with a gate head length (L_{head}) of 400 nm and a source-drain spacing (L_{sd}) of 600 nm; **(d)** A SEM image of T-shaped gate structure depicting a gate footprint of 50 nm.

Figure 22(b) shows the detailed device fabrication steps. The device fabrication started with mesa isolation using $Cl_2/CH_4/He/Ar$ inductively coupled plasma etching. Then Ti/Al/Ni/Au stack was deposited and annealed at 850˚C for 40s in N_2 to form the alloyed ohmic contacts. The ohmic contact resistance is 0.3 Ω·mm. An oxygen plasma treatment was then applied to form the oxide layer on top of the InAlN layer, which can effectively reduce the gate leakage current and improve RF erformance [26-29]. Finally, a Ni/Au T-shaped gate with a gate width (W_g) of 2 × 20 μm was fabricated by electron beam lithography. **Figure 22(c)** shows a plan-view scanning electron microscopy (SEM) image of the InAlN/GaN HEMT with a gate head length (L_{head}) of 400 nm and a source-drain spacing (L_{sd}) of 600 nm. **Figure 22(d)** shows a SEM image of T-shaped gate structure depicting a gate footprint of 50 nm.

Results and discussion

A. DC performance

The DC current-voltage (*I–V*) measurements are carried out by using an Agilent B1500A semiconductor parameter analyzer. **Figure 22(a)** shows the output characteristic of the InAlN/GaN

HEMT with a 50-nm gate length. The device on-resistance (R_{on}) extracted at gate-source (V_{gs}) of 0 V and drain-source voltage (V_{ds}) between 0 and 0.5 V is 1.33 Ω·mm. The gate-to-channel distance t_{bar} (including a 2-nm GaN, an 8-nm InAlN, and a 1-nm AlN) is 11 nm. Since L_g is 50 nm, the device presents an aspect ratio (L_g/t_{bar}) of 4.5. Due to the low L_g/t_{bar}, the short-channel effects (SCEs) start to appear when V_{ds} is larger than 5 V and V_{gs} is between -4 to -1 V. At V_{gs} = 1 V, drain current (I_d) in saturation region presents a decrease with increased V_{ds}, an indication of the thermal effect.

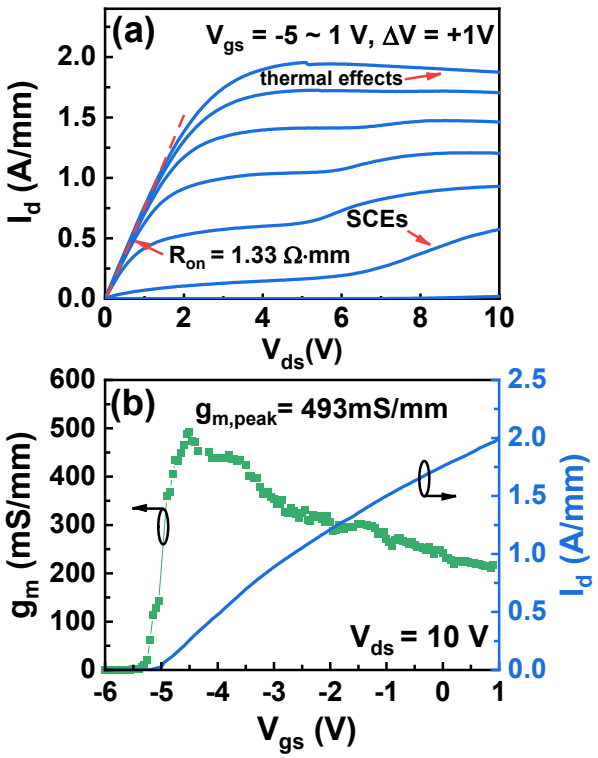

Figure 22. (a) Output characteristic, **(b)** the extrinsic transconductance g_m, and the transfer characteristic at V_{ds} = 10 V of the InAlN/GaN HEMT with a 50-nm gate length.

Figure 22(b) shows the transfer characteristic with the extracted extrinsic transconductance (g_m) of the InAlN/GaN HEMT with a 50-nm gate length at V_{ds} = 10 V. The maximum saturation drain current ($I_{d,\,max}$) is 2.01 A/mm at V_{gs} = 1 V and V_{ds} = 10 V. The g_m perk ($g_{m,\,peak}$) is 493 mS/mm. To the best of our knowledge, the record high $I_{d,\,max}$ of 2.8 A/mm and $g_{m,peak}$ of 660 mS/mm were achieved on a 55-nm-gate-length InAlN/GaN HEMT on Si with regrowth technology and L_{sd} of 175 nm [72]. The lower I_d and $g_{m,peak}$ in this study result from the regrowth-free technology and the larger source-drain spacing (L_{sd} = 600 nm).

Figure 23(a) shows the transfer and gate current (I_g) characteristics in semi-log scale of the InAlN/GaN HEMT with a 50-nm gate length at V_{ds} = 5 V and 10 V, respectively. At V_{ds} = 10 V,

the device off-current (I_{off}) is 2.76 × 10^{-7} A/mm and the I_{on}/I_{off} ratio is 7.28 × 10^{6}, which are higher than the record reported values (I_{off} of 7.12 × 10^{-7} A/mm and I_{on}/I_{off} ratio of 1.58 × 10^{6}) achieved from the InAlN/GaN HEMT on Si [70]. An average subthreshold swing (SS) of 72 mV/dec over more than two orders of I_d is extracted from the transfer curve. The drain-induced barrier lowering (DIBL) of 88 mV/V is extracted at I_d = 10 mA/mm between V_{ds} = 10 V and V_{ds} = 5 V, which is the lowest value among the reported GaN HEMTs on Si. The lowest DIBL value suggests a suppressed SCEs for the sub-100nm gate-length device. **Figure 23(b)** shows the off-state three-terminal breakdown characteristic of the 50-nm InAlN/GaN HEMT measured at V_{gs} = -8 V. The device features a BV_{ds} of 36 V at a drain leakage current of 1 mA/mm.

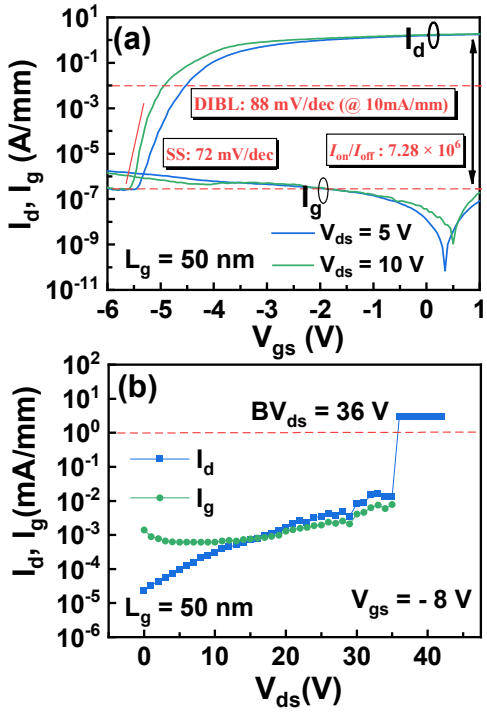

Figure 23. (a) The transfer and gate current characteristics in semi-log scale at V_{ds} = 10 V and 5 V, **(b)** the I_d and I_g as a function of V_{ds} at V_{gs} = -8 V of the InAlN/GaN HEMT with a 50-nm gate length. A BV_{ds} of 36 V was determined.

B. RF performance

The device RF performance is measured with a frequency range from 1 to 65 GHz. The network analyzer is calibrated using a two-port short/open/load/through method. On-wafer open and short structures is used to eliminate the effects of parasitic elements. **Figure 24(a)** shows the ~~the~~ current gain ($|h_{21}|^2$), unilateral gain (U), and the maximum stable gain (MSG) as a function of frequency at V_{ds} = 10 V, V_{gs} = −3 V after de-embedding. f_T/f_{max} of 140/215 GHz for the InAlN/GaN HEMT with a 50-nm gate length is obtained by extrapolation of $|h_{21}|^2$ with a -20 dB/dec slope. An $(f_T \times f_{max})^{1/2}$ of 173 GHz is obtained, which is the highest record values among the reported

InAlN/GaN HEMTs on Si with regrowth-free ohmic contact technology. To the best of our knowledge, a high $(f_T \times f_{max})^{1/2}$ of 226 GHz (f_T/f_{max} = 250/204 GHz) was achieved on a 55-nm InAlN/GaN HEMT on Si [72], and a high $(f_T \times f_{max})^{1/2}$ of 239 GHz (f_T/f_{max} = 190/300 GHz) was demonstrated on the e-mode high-k InAlN/GaN MISHEMTs with L_g of 50 nm [166]. The ohmic contact regrowth technology was used in both reported devices. Here for our device, the alloyed ohmic resistance (R_C: 0.3 Ω·mm) is higher than the reported regrowth ohmic contact resistance (R_C: 0.05 Ω·mm) [72]. This presents a high potential for the RF performance improvement by further decreasing the ohmic contact resistance. Due to f_T/f_{max} of 140/215 GHz, products of $f_T \times L_g$ and $f_{max} \times L_g$ of 7.0 and 10.75 GHz·μm are achieved, respectively. Although neither passivation nor field plate technology is used, the 140-GHz InAlN/GaN HEMT with an BV_{ds} of 36 V presents a Johnson's figure-of-merit (JFOM = $f_T \times BV_{ds}$) of 5.04 THz·V. **Figure 24(b)** shows the measured f_T and f_{max} of the 50-nm InAlN/GaN HEMT as a function of V_{gs}. Both f_T and f_{max} show a gradual decrease compared with their peak values, presenting a good device linearity.

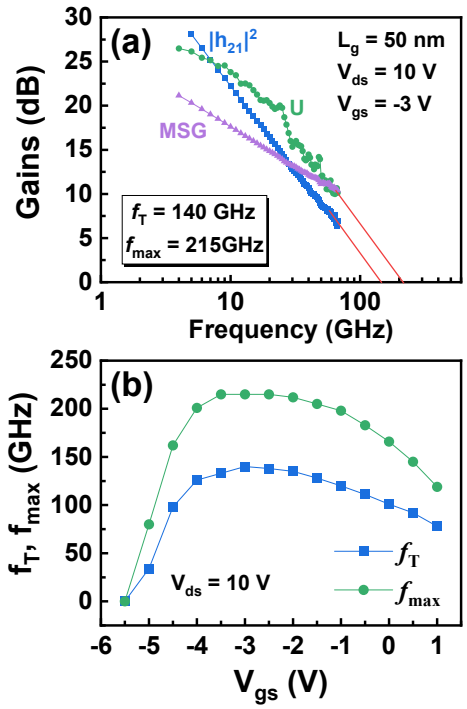

Figure 24. (a) RF performance of the InAlN/GaN HEMT with a 50-nm gate length at V_{gs} = -3 V and V_{ds} = 10 V with f_T/f_{max} = 140/215 GHz. **(b)** The f_T and f_{max} as a function of V_{gs}.

C. Equivalent circuit model

The classical 16-element equivalent-circuit model is used for the InAlN/GaN HEMT, as shown in **Figure 25 (a)** [96, 170]. Based on this model, the device extrinsic and intrinsic parameters are extracted in Table I [96, 170, 171]. The slight discrepancy between the simulated and measured *S*-parameter values is observed in **Figure 25 (b),** verifying the accuracy of the extracted extrinsic and intrinsic parameters. The f_T and f_{max} can be calculated using [96, 172]

$$f_T = \frac{G_m / G_0}{2\pi((C_{gs}+C_{gd})(1/G_0+(R_s+R_d))+(C_{gd}\cdot G_m/g_0)(R_s+R_d))},$$
$$f_{\max} = \frac{f_T}{2\sqrt{(R_s+R_g+R_i)\cdot G_0 + 2\pi f_T R_g C_{gd}}}. \quad (1)$$

where G_m and G_0 are the intrinsic transconductance and drain-source conductance, respectively; C_{gs} and C_{gd} are the gate-source and gate-drain parasitic capacitance, respectively; R_s, R_d, R_g, and R_i are the parasitic source access resistance, drain access resistance, gate electrode resistance, and input resistance, respectively.

The calculated f_T/f_{max} = 145/218 GHz is very close to the value (f_T/f_{max} = 140/215 GHz) extracted by the extrapolation of $|h_{21}|^2$ with a -20 dB/dec slope, which confirms the excellent device RF performance. The high intrinsic transconductance/drain-source conductance (G_m/G_0) ratio of 10.6 contributes to the high f_{max}.

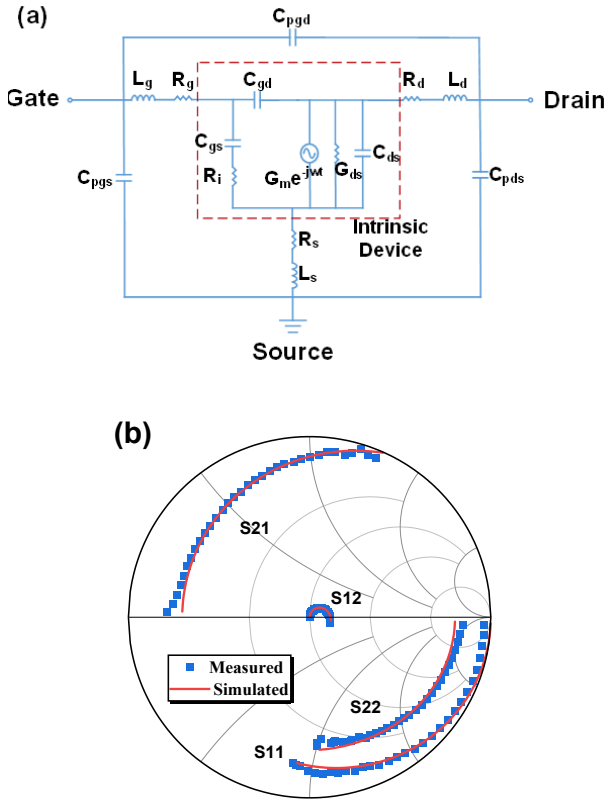

Figure 25. (a) Equivalent-circuit model for InAlN/GaN HEMT. The intrinsic elements are shown in the red dashed box. **(b)** Comparison of the simulated and measured S-parameters for the InAlN/GaN HEMT with a 50-nm gate length at V_{ds} =10 V and V_{gs} = −3 V.

Table I

THE EXTRACTED EXTRINSIC AND INTRINSIC PARAMETERS FOR THE 50-NM INALN/GAN HEMTS

Extrinsic parameters	Intrinsic parameters
C_{pgd} = 1.16 fF	C_{gs} = 444 fF/mm
C_{pgs} = 26.35 fF	C_{gd} =104 fF/mm
C_{pds} = 26.21 fF	C_{ds} = 318 fF/mm
L_s = 3.17 pH	R_i = 0.90 Ω·mm
L_g = 44.03 pH	G_m = 573 mS/mm
L_d = 41.30 pH	G_0 = 54 mS/mm
R_s = 0.43 Ω·mm	G_m/G_0 = 10.6
R_g = 0.26 Ω·mm	τ = 1.09 ps
R_d = 0.45 Ω·mm	$f_{T,\ model}$ =145 GHz
	$f_{max,\ model}$ =218 GHz

D. Scaling behavior

The InAlN/GaN HEMTs with L_g between 50 nm and 350 nm are fabricated. **Figure 26(a)** shows the measured f_T/f_{max} of the InAlN/GaN HEMTs with different L_g at V_{gs} = -3 V and V_{ds} = 10 V. The devices with L_g of 50, 70, 100, 150, 250, and 350 nm present f_T/f_{max} of 140/215, 135/205, 120/170, 90/160, 60/136, 36/128 GHz, respectively. $f_T \times L_g$ and $f_{max} \times L_g$ are obtained in **Figure 26(b)**. A $f_T \times L_g$ peak of 15 GHz·μm is achieved on the 250-nm-gate-length InAlN/GaN HEMT with a f_T of 135 GHz. $f_{max} \times L_g$ presents a decrease from 44.8 GHz·μm (L_g = 350 nm) to 10.75 GHz·μm (L_g = 50 nm). The decrease of both $f_T \times L_g$ and $f_{max} \times L_g$ as L_g scales down means that the effect of parasitic parameters is more pronounced, thus hindering the improvement of f_T and f_{max}. Due to the large head length of T-shaped gate (L_{head} = 400 nm), the transistors features higher f_{max} and $f_{max} \times L_g$.

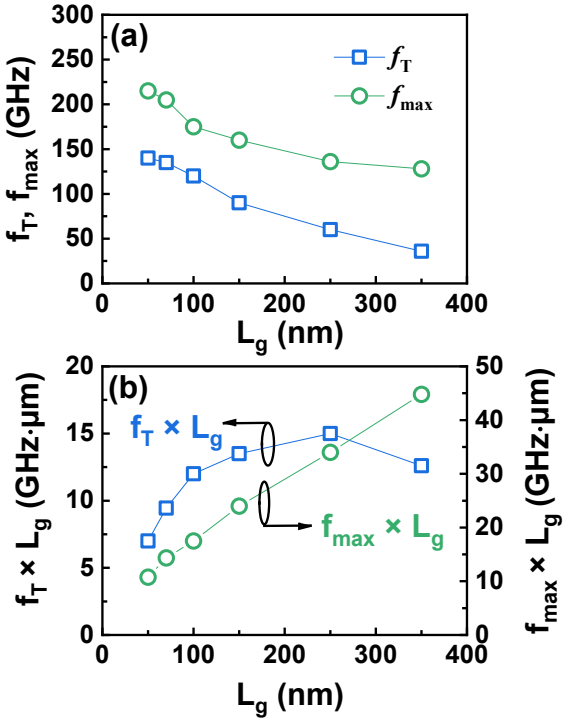

Figure 26. (a) Measured f_T and f_{max} as a function of L_g at V_{gs} = -3 V and V_{ds} =10V. **(b)** $f_T \times L_g$ and $f_{max} \times L_g$ as a function of L_g.

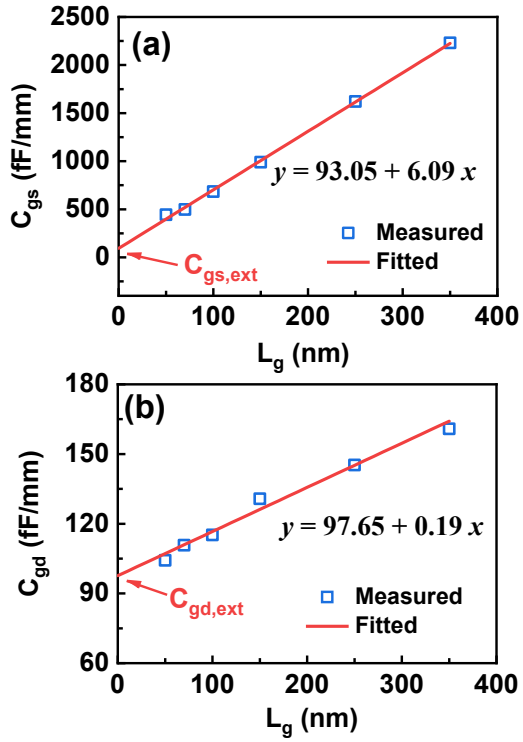

Figure 27. Measured and linear fitted **(a)** gate-source parasitic capacitance C_{gs} and **(b)** gate-drain parasitic capacitance C_{gd} as a function of L_g at V_{gs} = -3 V and V_{ds} =10V.

To shed more light on the scaling behavior, the extrinsic and intrinsic parameters of these devices are further extracted using the equivalent circuit model discussed above. C_{gs} can be separated to two parts: gate-source intrinsic capacitance ($C_{gs,int}$) and gate-source extrinsic capacitance ($C_{gs,\,ext}$). It means $C_{gs} = C_{gs,int} + C_{gs,ext}$ [173]. C_{gd} can also be written as $C_{gd} = C_{gd,int} + C_{gd,ext}$. **Figure 27** shows the extracted C_{gs} and C_{gd} as a function of L_g. Both C_{gs} and C_{gd} present a linear dependence upon L_g. By linear fitting, the $C_{gs,ext}$ and $C_{gd,\,ext}$ are obtained from C_{gs} and C_{gd} at $L_g = 0$ nm [173], as shown in **Figure 27**. Here $C_{gs,ext}$ of 93.05 fF/mm and $C_{gd,ext}$ of 97.65 fF/mm are determined, respectively.

The total delay (τ) of transistors can be written as [173] [16]

$$\tau = \frac{1}{2\pi f_T} = \tau_t + \tau_{ext} + \tau_{par} \qquad (2)$$

Here τ is partitioned into three components: transit time (τ_t), parasitic charging delay (τ_{ext}), and parasitic resistance delay (τ_{par}).

τ_t is the transit time under the gate region. It is related to the gate length as well as the electron velocity (v_e) under the gate region, and can be calculated by [16, 173]

$$\tau_t = \frac{Cgsi + Cgdi}{G_m} = \frac{L_g}{v_e}. \qquad (3)$$

τ_{ext} is parasitic charging delay through $C_{gs,ext}$ as well as $C_{gd,ext}$, and can be written as [173] [16]

$$\tau_{ext} = \frac{Cgs,ext + Cgd,ext}{G_m}. \qquad (4)$$

τ_{par} is parasitic resistance delay mainly associated with R_s as well as R_d, and can be written as [173] [16]

$$\tau_{par} = C_{gd}(R_s + R_d)[1 + (1 + \frac{C_{gs}}{C_{gd}})\frac{G_0}{G_m}]. \qquad (5)$$

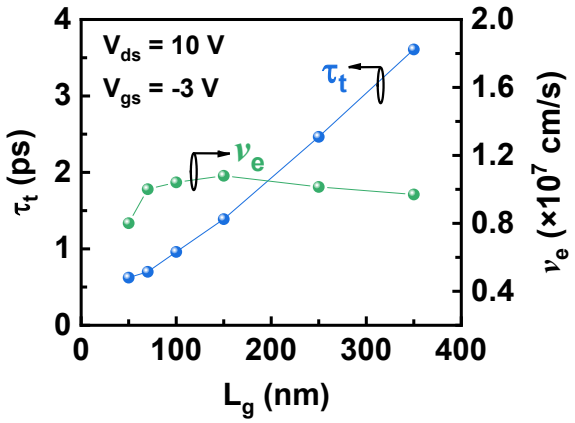

Figure 28. Extracted transit time (τ_t) and electron velocity (v_e) as a function of L_g at V_{gs} = -3 V and V_{ds} =10V.

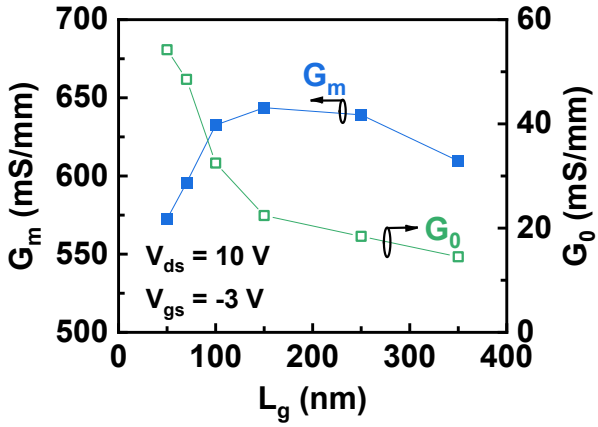

Figure 29. Extracted intrinsic transconductance (G_m) and intrinsic conductance (G_0) as a function of L_g at V_{gs} = -3 V and V_{ds} =10V.

Figure 28 plots τ_t and v_e as a function of L_g calculated from (3). As L_g decreases, τ shows a monotonous drop, which corresponds to the increased f_T. With decreased L_g, v_e increases to a maximum value of 1.08×10^7 cm/s (at L_g = 150 nm) and then drop to 0.80×10^7 cm/s (at L_g = 50 nm). **Figure 29** shows the extracted G_m and G_0 from the equivalent-circuit model as a function of L_g. G_0 shows an increase with decreased L_g. The dependence of G_m and v_e on L_g present the same trend. Based on (3), because C_{gsi} and C_{gdi} linearly depends on L_g, we conclude that the change of G_m is attributed to v_e difference. The same trend of G_m and v_e on L_g is also observed in InAs HEMTs and result from the short channel effect [174-176].

Figure 30 exhibits the calculated τ_t, τ_{ext}, and τ_{par} using (3) to (5). τ_{ext} and τ_{par} is almost unchanged. Conversely, τ_t decreases with decreased L_g and dominates the total delay in all devices. This makes it possible to decrease delay and improve f_T through downscaling of device gate length. However, for the device with L_g below 100 nm, the effect of τ_{ext} and τ_{par} become non-negligible. The ratios of $(\tau_{ext} + \tau_{par})/\tau_t$ are 39% and 40% for the InAlN/GaN HEMTs with L_g of 70 and 50 nm, respectively. This means the parasitic capacitance and resistance significantly hampers further L_g scaling benefits in RF performance of sub-100 nm InAlN/GaN HEMTs.

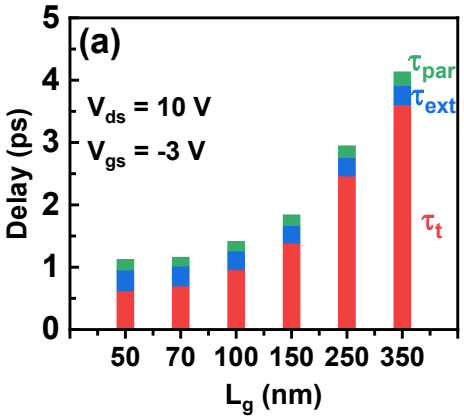

Figure 30. Extracted delay components as a function of L_g. The delay (τ) is partitioned into three components: transit time (τ_t), parasitic charging delay (τ_{ext}), and parasitic resistance delay (τ_{par}).

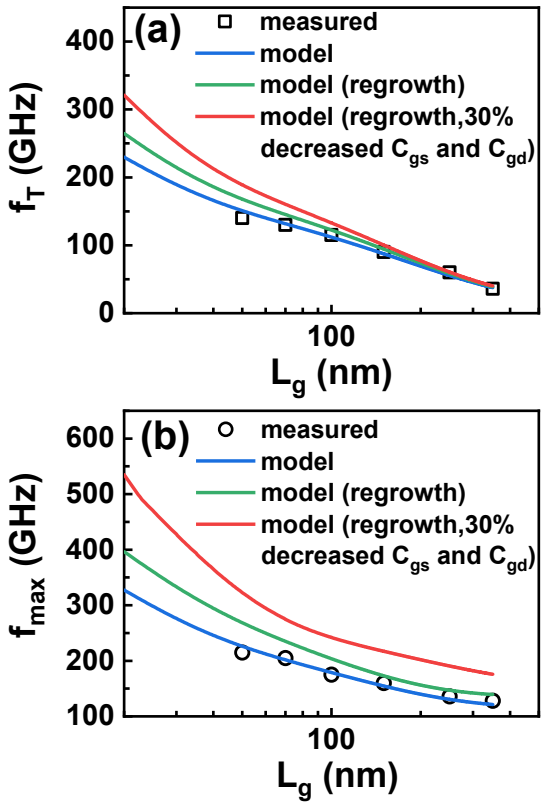

Figure 31. f_T and f_{max} under measured results (Scatters), obtained from model with extracted parameters (Blue-line), model with regrowth ohmic contact(Green-line), and model with regrowth and 30% decreased C_{gs} and C_{gd} (Red-line).

Therefore, downscaling and decreasing parasitic resistances as well as capacitances are very important for further improving device performance of InAlN/GaN HEMTs on Si. **Figure 31** plots the calculated f_T and f_{max} based on the model and the extracted parameters (Blue-line in **Figure 31**), which shows a good agreement with the measured results. In terms of the electron velocity saturation, the electron velocity of the InAlN/GaN HEMTs with $L_g < 50$ nm is assumed to be the same as that with $L_g = 50$ nm. With the obtained v_e, τ_t can be obtained using (3), τ_{ext} is parasitic charging delay through $C_{gs,ext}$ and $C_{gd,ext}$, and both are the constant as shown in **Figure 27**. τ_{par} is mainly associated with R_s and R_d, which are independent on L_g. As shown in **Figure 30**, τ_{ext} and τ_{par} present slight change with L_g. So here τ_{par} of the device with $L_g = 50$ nm is used during the model calculation. Then f_T can be calculated with the obtained τ_t, τ_{ext} and τ_{par} by using (2). When L_g decrases from the 50 nm to 20 nm, the T-shaped gate head length of 400 nm is unchanged, so the effect of the small gate length variation on R_g and R_i is miminal. Hence R_g and R_i of device with L_g of 50 nm are used. C_{gd} is extracted from the linear fitting in Figure 7 (b) and then f_{max} is obtained using (1). The model results present that f_T/f_{max} of 230/327 GHz can be achieved when L_g scales down to 20 nm with the technology developed in the study. To decrease the parasitic

resistance, the regrowth ohmic contact can be used. Here R_s (0.30 Ω·mm), R_d (0.32 Ω·mm), and G_m (573 mS/mm) are changed to 0.10 Ω·mm, 0.08 Ω·mm, and 620 mS/mm [72]. Then new model results with regrowth technology are plotted (Green-line in **Figure 31**) and a f_T/f_{max} of 265/397 GHz is achieved on the device with a 20-nm gate length. Optimizing the detailed structure of T-shaped gate can decrease C_{gs} and C_{gd}. Hence when 30% decreasing of C_{gs} and C_{gd} is added into the model, new results (Red-line in **Figure 31**) are plotted and an improved f_T/f_{max} of 320/535 GHz on 20-nm-gate-length InAlN/GaN HEMT is demonstrated. These values are comparable to the 27-nm InAlN/GaN HEMTs on SiC with f_T/f_{max} of 348/340 GHz, suggesting the possibility of further improvement of InAlN/GaN HEMTs on Si.

5.4 Conclusions

In summary, high-performance 50-nm InAlN/GaN HEMT on Si with an I_{on}/I_{off} ratio of 7.28×10^6, a SS of 72 mV/dec, a DIBL of 88 mV/V, a BV_{ds} of 36, a f_T/f_{max} of 140/215 GHz, and a JFOM of 5.04 THz·V are demonstrated. The extrinsic and intrinsic parameters of transistors with different L_g are extracted and the scaling behavior of InAlN/GaN HEMTs on Si is demonstrated. Based on extracted model, a f_T/f_{max} of 320/535 GHz can be achieved on a 20-nm-gate-length InAlN/GaN HEMT with regrowth ohmic contact technology and 30% decreased parasitic capacitance. This study confirms the feasibility of further improvement of InAlN/GaN HEMTs on Si for RF applications.

6. High-Performance HZO/InAlN/GaN MISHEMT for Ka-Band Application

6.1 Introduction

We report on the demonstration of microwave power performance at 30 GHz on InAlN/GaN metal-insulator-semiconductor high electron mobility transistor (MISHEMT) on silicon substrate by using the $Hf_{0.5}Zr_{0.5}O_2$ (HZO) as a gate dielectric. Compared with HEMT, the MISHEMT with a gate length (L_G) of 50 nm presents a significantly enhanced performance with an ON/OFF current ratio (I_{ON}/I_{OFF}) of 9.3×10^7, a subthreshold swing (SS) of 130 mV/dec, a low drain-induced barrier lowing (DIBL) of 45 mV/V, and a breakdown voltage of 35 V. RF characterizations reveal a current gain cutoff frequency (f_T) of 155 GHz and a maximum oscillation frequency (f_{max}) of 250 GHz, resulting in both record high $(f_T \times f_{max})^{1/2}$ of 197 GHz and Johnson's figure-of-merit (JFOM = $f_T \times$BV) of 5.4 THz·V among the reported GaN MISHEMTs on Si. The power performance at 30 GHz exhibits a maximum output power of 1.36 W/mm, a maximum power gain of 12.3 dB, and a peak power-added efficiency of 21%, demonstrating the great potential of HZO/InAlN/GaN MISHEMTs for the Ka-band application.

6.2 Background

GaN-based high-electron-mobility transistors (HEMTs) indicate great potential for RF and millimeter-wave power applications [9, 57, 177-179]. To date, excellent current gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) have been demonstrated on GaN HEMTs

with device downscaling [14, 27, 72, 180]. However, device downscaling usually causes high gate leakage current and deteriorates breakdown voltage (BV), thus limiting the maximum drain current and output power density. These bottlenecks can be circumvented by inserting a dielectric material under the gate of HEMTs. Therefore, the introduction of gate dielectric on GaN metal-insulator-semiconductor HEMTs (MISHEMTs) could lead to further improvement of the device performance for high-speed and high-power applications.

For high-speed device application, different dielectric materials (Al_2O_3 [181-190], HfO_2 [191-193], SiN [194-198], SiO_2 [199], TiO_2 [200], MgCaO [201], ZnO [202], *et al*.) have been investigated as the gate dielectric in GaN MISHEMTs. The relevant device performance, such as maximum drain current ($I_{d,max}$) of 2.4 A/mm [203], on/off current ratio (I_{ON}/I_{OFF}) of 5×10^8 [201], transconductance (g_m) of 653 mS/mm [182], f_T/f_{max} of 190/300 GHz [191], and Johnson's figure-of-merit (JFOM) of 10.8 THz·V [194] has been demonstrated.

In this study, we report the first demonstration of the $Hf_{0.5}Zr_{0.5}O_2$ (HZO) as the gate dielectric for GaN-based high-speed MISHEMTs. Key device performance parameters, including low leakage current, high I_{ON}/I_{OFF}, low drain-induced barrier lowing (DIBL), high f_T/f_{max}, JFOM, and power performance are simultaneously achieved on the HZO/InAlN/GaN MISHEMT, suggesting its great potential for high-speed applications.

6.3 Experimental Details, Results and Discussions

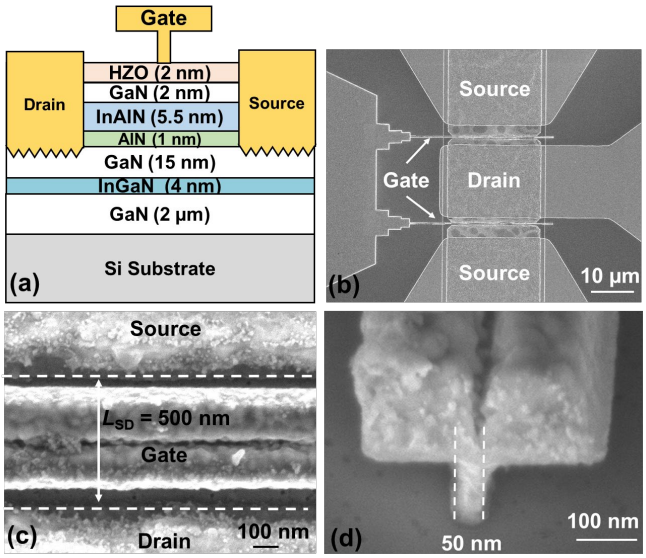

Fig. 32 (a) Schematic of the fabricated HZO/InAlN/GaN MISHEMT. Scanning electron microscope (SEM) images of **(b)** an overview of a fabricated device with source, drain and gate, **(c)** a zoom-in view of a fabricated device with a source-drain spacing (L_{SD}) of 500 nm, and **(d)** a T-shaped gate with a gate length (L_G) of 50 nm.

Fig. 32(a) shows the schematic of the fabricated HZO/InAlN/GaN MISHEMT. The growth of epitaxial structure is performed with metalorganic chemical vapor deposition (MOCVD) on a 4-inch high-resistance Si (111) substrate. The epitaxial layer consists of a 2-μm undoped GaN buffer layer, a 4-nm $In_{0.12}Ga_{0.88}N$ back-barrier layer, a 15-nm GaN channel layer, a 1-nm AlN interlayer,

a 5-nm lattice-matched $In_{0.17}Al_{0.83}N$ barrier layer, and a 2-nm GaN cap layer. Device mesa isolation was carried out with Cl_2-based inductively coupled plasma (ICP) etching with an etch depth of ~300 nm. Ohmic contact was formed with Ti/Al/Ni/Au deposition and annealing at 850˚C for 40 s. Then HZO was deposited as the gate dielectric and passivation layer by using plasma-enhanced atomic layer deposition (PEALD) at 150°C. Tetrakis(dimethylamino)hafnium (TDMAH), Bis(methyl-η5−cyclopentadienyl)methoxymethylzirconium (ZRCMMM), and oxygen are used as Hf, Zr, and O source, respectively. The film was grown with a Hf: Zr ratio of 1:1 by alternating cycles of TDMAH, O_2, ZRCMMM, O_2. The alternating cycles were repeated 30 times for 2-nm HZO growth. These steps were followed by T-shaped gate fabrication with electron beam lithography and Ni/Au metal stack deposition. Finally, HZO on the pad was removed by dipping the samples in HF solution (HF: H_2O = 1: 9) for 30s. In addition, the InAlN/GaN HEMTs without HZO deposition are also fabricated as a reference. **Fig. 32(b)~(c)** show the scanning electron microscope (SEM) images of a typical fabricated device. The source-drain spacing (L_{SD}), gate-source spacing (L_{GS}), gate-drain spacing (L_{GD}) are 500, 200, and 250 nm, respectively. The T-shaped gate exhibits a gate footprint of 50 nm, a gate head of 400 nm, and a gate width (W_G) of 2 × 20 μm.

Fig. 33(a) and **(b)** show the typical transfer and gate leakage current characteristics of the InAlN/GaN HEMT and MISHEMT (L_G = 50 nm, and L_{SD} = 500 nm), respectively. The HEMT exhibits an OFF-current (I_{OFF}) of 5.03 × 10^{-5} A/mm, a ON-OFF current ratio (I_{ON}/I_{OFF}) of 3.7 × 10^4, a subthreshold swing (SS) of 225 mV/dec, and a drain-induced barrier lowing (DIBL, extracted at I_D of 1×10^{-3} A/mm with V_{DS} of 10 V and 1 V) of 65 mV/V. Compared with HEMT, the MISHEMT shows a significantly enhanced performance with a I_{OFF} of 2.33 × 10^{-8} A/mm, a I_{ON}/I_{OFF} of 7.9 × 10^7, a SS of 130 mV/dec, and a DIBL of 45 mV/V. It's well known that the gate dielectric can suppress the gate leakage, resulting in the low I_{OFF} and high I_{ON}/I_{OFF}. However, the enhanced SS and DIBL characteristics are beyond expectation. The aspect ratio (L_G/T_B, T_B is the gate-to-channel distance) of HEMT and MISHEMT is 6.25 and 5, respectively. In general, the short channel effects (SCEs) can be mitigated when the aspect ratio L_G/T_B is larger than 15 [31, 57]. Although the insert of 2-nm HZO gate dielectric decreases the L_G/T_B, the low SS and DIBL mean the improved gate control capacity, which indicates the potential applications of HZO/InAlN/GaN MISHEMTs on power loss reduction, noise performance, and high-frequency switch.

Fig. 33(c) shows the output characteristics of both devices. The on-resistance (R_{ON}) of 1.54 Ω·mm (HEMT) and 1.41 Ω·mm (MISHEMT) are extracted at V_{DS} of 0.5 V and V_{GS} of 0 V. The reduced R_{ON} is confirmed with Hall measurements. Before HZO deposition, the electron density (n_{2D}) of 1.71 × 10^{13} cm^{-2} and electron mobility (μ_{2D}) of 1663 $cm^2/V{\cdot}s$ are obtained as shown from Hall measurement. After HZO deposition, n_{2D} of 2.24 × 10^{13} cm^{-2} and μ_{2D} of 1613 $cm^2/V{\cdot}s$ are determined. The increased n_{2D} presents a good passivation effect on the material surface [204, 205], and the negligible change in μ_{2D} means that the electron mobility does not degrade with the dielectric deposition.

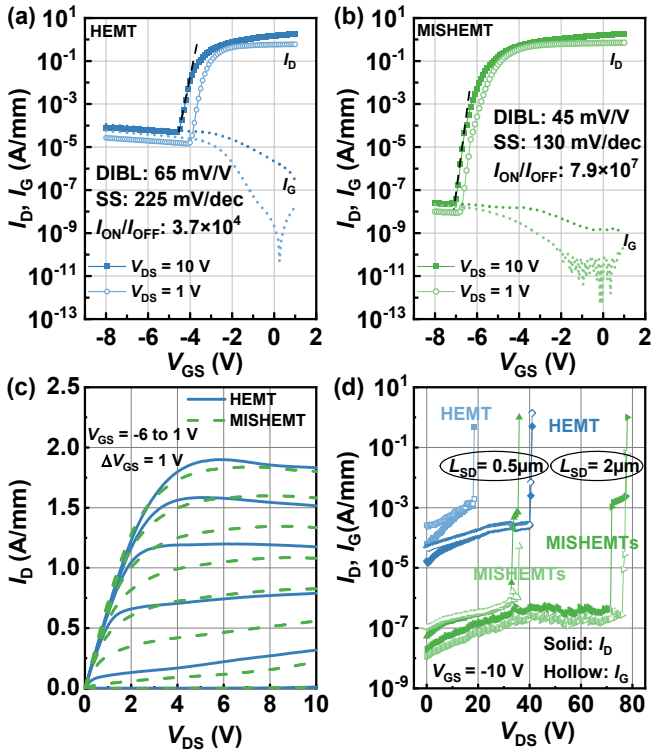

Fig. 33 Transfer and gate leakage current characteristics in semi-log scale at V_{DS} of 10 V and 1 V of the L_G = 50 nm **(a)** HEMT and **(b)** MISHEMT, respectively. **(c)** Output characteristic of both devices. **(d)** Off-state three-terminal breakdown characteristics for the L_G = 50 nm HEMTs and MISHEMTs with L_{SD} of 2 μm and 500 nm as labeled.

Fig. 33(d) shows the off-state three-terminal breakdown characteristics of HEMTs and MISHEMTs with a L_G of 50 nm. The breakdown voltage (BV) of 15 V (HEMT) and 35 V (MISHEMT) are obtained on the devices with L_{SD} of 500 nm. With the increased L_{SD} of 2 μm, BV values increase to 40 V (HEMT) to 72 V(MISHEMT), respectively.

The microwave characteristics of the HZO/InAlN/GaN MISHEMT are characterized from 1 to 65 GHz using an Anritsu MS4647B vector network analyzer. By using the de-embedded S-parameters, the high-frequency gains of the devices are extracted. **Fig. 34(a)** plots the measured short-circuit current gain ($|h_{21}|^2$), Mason's unilateral gain (U), maximum-stable-gain (MSG), and stability-factor (k) of the MISHEMT with L_G of 50 nm and L_{SD} of 500 nm at V_{DS} = 10 V and V_{GS} = -3.8 V. f_T/f_{max} of 155/250 GHz is obtained by extrapolation of $|h_{21}|^2$ and U with a -20 dB/dec slope, resulting in $f_T \times L_G$ of 7.75 GHz·μm and $(f_T \times f_{max})^{1/2}$ of 197 GHz. f_T/f_{max} versus I_D is also measured and plotted in **Fig. 34(b)**. f_T for the L_G = 50 nm devices with L_{SD} of 500 nm and 2 μm is 155 and 110 GHz (BV of 35 V and 72 V), resulting in the high Johnson's figure-of-merit (JFOM = $f_T \times$ BV) of 5.4 and 7.9 THz·V, respectively. **Fig. 35(a)** and **(b)** show the f_{max} and BV versus f_T benchmark for the presented devices against state-of-the-art GaN-based MISHEMTs on SiC, Sapphire, Si, and GaN substrates [181-203]. The HZO/InAlN/GaN MISHEMTs on Si in this work exhibit both record high $(f_T \times f_{max})^{1/2}$ and JFOM among the reported GaN MISHEMTs on Si substrate, indicating the outstanding potential for high-speed and high power applications.

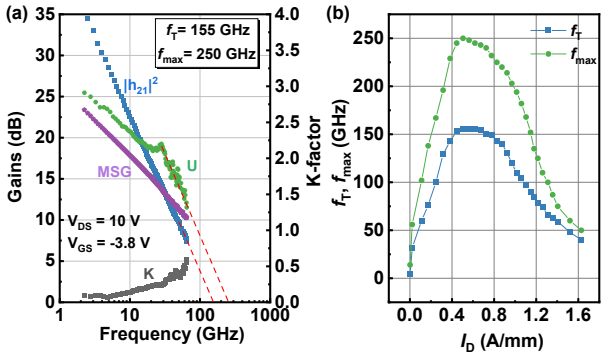

Fig. 34 (a) High-frequency gains ($|h_{21}|^2$, U and MSG), stability factor (k), **(b)** f_T/f_{max} versus I_D of HZO/InAlN/GaN MISHEMT with L_G of 50 nm.

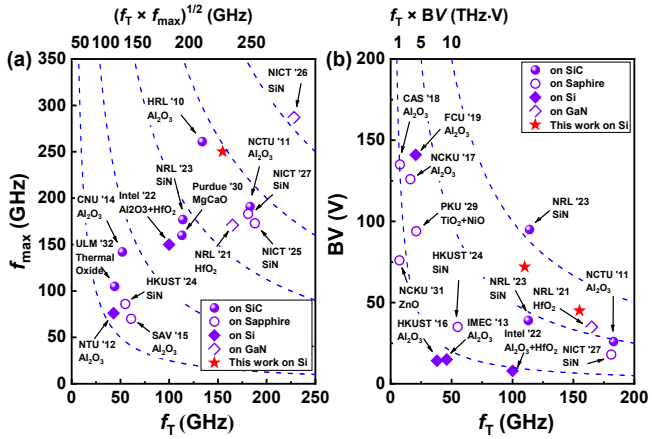

Fig. 35 (a) f_{max} and **(b)** BV versus f_T benchmark for the presented devices (HZO/InAlN/GaN MISHEMTs on Si) against state-of-the-art GaN MISHEMTs on SiC, Sapphire, Si, and GaN substrates.

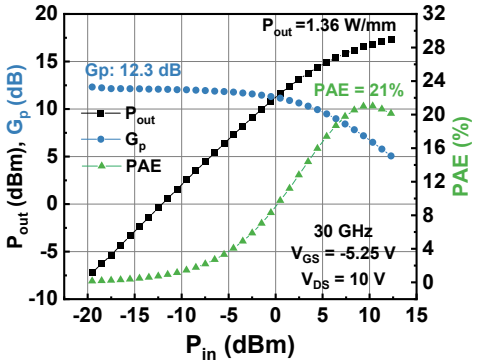

Fig. 36 Power sweep of the HZO/InAlN/GaN MISHEMT with L_G of 50 nm at 30 GHz at the bias condition of V_{GS} at -5.25V and V_{DS} at 10 V. The device is showing a maximum output power (P_{out}) of 1.36 W/mm, a maximum gain (G_p) of 12.3 dB, and a peak power added efficiency (PAE) of 21 %.

To shed light on the power performance of the HZO/InAlN/GaN MISHEMT, load-pull measurements were carried out. **Fig. 36** shows a power sweep of the HZO/InAlN/GaN MISHEMT with a L_G of 50 nm, a L_{SD} of 500 nm, and a W_G of 2 × 20 µm at the bias condition of V_{GS} at -5.25 V and V_{DS} at 10 V. At 30 GHz, the device shows a saturated output power (P_{out}) of 17.36 dB (amounts to 1.36 W/mm) and a maximum power gain (G_P) of 12.3 dB. At the peak power-added

efficiency (PEA) of 21%, the device offers a P_{out} of 1.20 W/mm, with an associated power gain of 6.5 dB. To the best of our knowledge, this is the first demonstrate of GaN MISHEMT on Si substrate for the Ka-band application.

6.4 Summary

In summary, by using HZO as the gate dielectric, the L_G = 50 nm InAlN/GaN MISHEMT presents a high performance with I_{ON}/I_{OFF} of 9.3 × 10^7, SS of 130 mV/dec, DIBL of 45 mV/V, f_T/f_{max} of 155/250 GHz, $(f_T \times f_{max})^{1/2}$ of 197 GHz, and JFOM of 5.4 THz·V. Power performance at 30 GHz exhibit a saturation P_{out} of 1.36 W/mm, a maximum G_P of 12.3 dB, and a peak PEA of 21%, demonstrating the great potential of the HZO/InAlN/GaN MISHEMTs for Ka-band applications.

7. High Performance AlGaN/GaN and InAlN/GaN MISHEMTs using N_2O treated TiO_2 as the Gate dielectric

7.1 Introduction

In this work, TiO_2 thin films deposited by atomic layer deposition (ALD) method, were treated with a special N_2O plasma surface treatment and used as the gate dielectric for AlGaN/GaN and InAlN/GaN metal-insulator-semiconductor high-electron-mobility-transistors (MISHEMTs). These TiO_2 films exhibit a dielectric constant of 33.1 and a two-terminal current of 1.96×10^{-10} A/mm. When applied as the gate dielectric, the AlGaN/GaN MISHEMT with a 2-μm-gate-length shows a high on/off ratio of 1.44×10^8 and a low *SS* of 85 mV/dec while the InAlN/GaN MISHEMT with 2-μm-gate-length depicts a high on/off ratio of 2.9×10^7 and a record low *SS* of 82 mV/dec among all GaN MISHEMTs using TiO_2 as the gate dielectric. This work provides a feasible way to significantly improve the TiO_2 film electrical property for gate dielectrics and it suggests that the developed TiO_2 dielectric is a promising high-κ gate oxide and a potential passivation layer for GaN-based MISHEMTs, which can be further extended to other transistors.

7.2 Background

GaN-based high electron mobility transistors, due to its superior material properties[1-3], have been extensively studied for high frequency and high-power applications. Nevertheless, due to the Schottky gate contact nature, the conventional GaN HEMTs feature a high gate leakage current which limits the device performance. To address this problem, gate dielectric can be used. Conventional materials such as SiN, SiO_2[4-6], Al_2O_3[7] have been employed as the gate dielectric but it comes at a cost of device transconductance degradation and undesirable threshold voltage shifts. A number of high-k dielectrics such as ZrO_2, HfO_2, MgCaO, Ta_2O_5[7-12], etc., have been investigated. However, problems remain unsolved with the threshold voltage instability being the most serious one[13]. TiO_2 has been shown to be a promising candidate for high-κ gate dielectric due to its high dielectric constant[14] (i.e., 80-120 of its rutile phase). Nonetheless, TiO_2 features a low energy bandgap of 3.4 eV which could cause high gate leakage current and degrade the device performance. In this work, we demonstrate a promising N_2O plasma surface treatment method that can be applied on TiO_2 dielectric to eliminate the high leakage problem. With such a TiO_2 gate dielectric, our AlGaN/GaN and InAlN/GaN MISHEMTs show a slight threshold voltage

shift and a negligible hysteresis, demonstrating superior electrical performances (including high on/off ratio and record low SS) compared with other reported GaN-based MISHEMTs using TiO_2 as the gate dielectric.

7.3 EXPERIMENTAL DETAILS, RESULTS AND DISCUSSIONS

We desire to maintain an amorphous TiO_2 state with the N_2O treatment to minimize the gate leakage current. Thus, two-terminal electrical characterization and X-ray diffraction measurement are performed to respectively evaluate TiO_2 electrical property and crystalline feature before and after treatment. The experimental results are shown as the following. A 15 nm TiO_2 was deposited by atom layer deposition method at 150℃ on SiO_2/Si substrate to measure the two-terminal current. After the deposition, the samples received a 2-12 mins N_2O surface treatment in a plasma enhanced chemical vapor deposition (PECVD) chamber. **Fig. 37(a)** shows the XRD measurement results. No diffraction peaks were observed for the as-deposited film. For the 0.5 min treated TiO_2 sample, it shows a broadened diffraction peak between 15° and 35°, indicating a standard amorphous structure. For the 2 min treated TiO_2 sample, it begins to crystallize and changes from amorphous to anatase phase. With the treatment time increases, the (1 0 1) anatase diffraction peak of TiO_2 becomes more prominent.

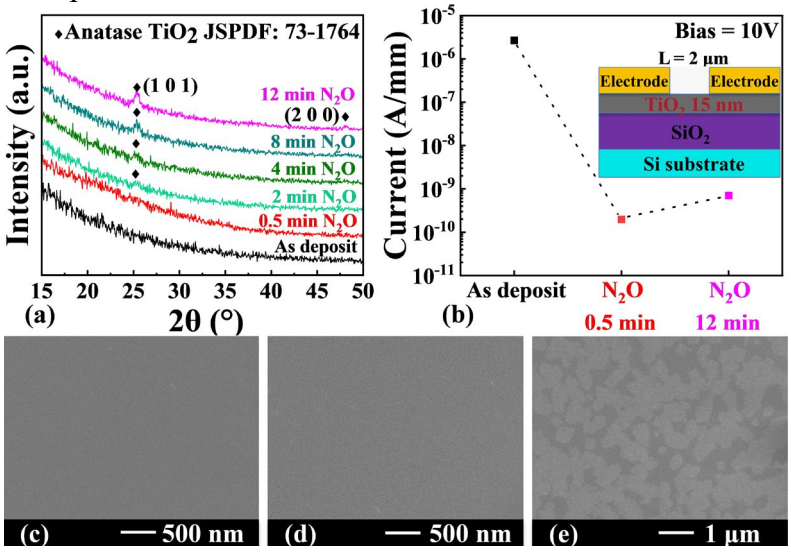

Fig. 37. (a) X-ray diffraction patterns of the as-deposit film and 0.5 min, 2 min, 4 min, 8 min, 12 min treated film, respectively; (b) Two terminal current of different TiO_2 film with 2 μm contact separation; Surface morphology for the as-deposit (c) film, 0.5 min treated (d) and 12 min treated (e) film, respectively.

Fig. 37(c) and **Fig. 37(d)** are the SEM pictures showing the surface morphology of the as-deposit film and the 0.5 min treated TiO_2 film, respectively. The films are smooth and flat, and no crystallization was observed. **Fig. 37(e)** depicts the surface of 12 min treated TiO_2 film, exhibiting a mixture of light and dark area, which is attributed to the island growth mode of anatase TiO_2[206]. **Fig. 37(b)** shows the representative two terminal current of some N_2O treated TiO_2 films, with the contact separation of 2 μm at the bias of 10V. The 0.5 min treated sample exhibited a current of 1.96×10^{-10} A/mm, indicating that the N_2O plasma surface treatment can improve the

TiO_2 insulation property significantly. The oxygen vacancies in the treated TiO_2 film are reduced with the N_2O plasma treatment, which effectively recover the defects in low temperature thermal ALD deposited TiO_2 film[207, 208]. In addition, a long treatment time will promote the crystallization of TiO_2, which leads to a degraded insulation property [209].

DEVICE FABRICATION

In order to check whether our N_2O treated TiO_2 film is suitable for the gate dielectric, we applied it on both InAlN and AlGaN MISHEMTs. The AlGaN/GaN (with 20nm thick barrier) and InAlN/GaN (with 8nm thick barrier) heterostructures were grown by metalorganic chemical vapor deposition (MOCVD) on SiC substrate as shown in **Fig. 38(a)** and **Fig. 38(b)**, respectively.

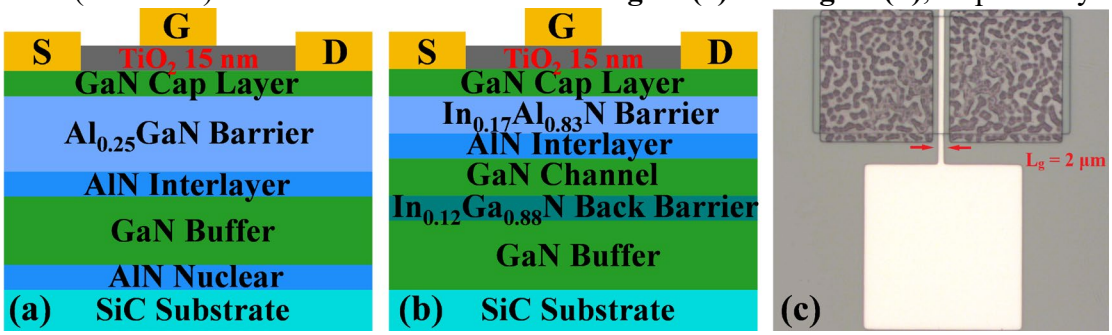

Fig. 38. Schematic of TiO_2/AlGaN/GaN (a) and TiO_2/InAlN/GaN (b) MISHEMT cross-section; (c) Microscope image of a fabricated device top-view with the gate length of 2 µm;

TABLE I
DETAILS OF THE FABRICATION CONDITIONS FOR SAMPLE A-F

Name	Type	12 min N_2O treatment before TiO_2 deposition	30s N_2O treatment on TiO_2 layer
Sample A	AlGaN HEMT	No	-
Sample B	AlGaN MISHEMT	No	Yes
Sample C	AlGaN HEMT	Yes	-
Sample D	AlGaN MISHEMT	Yes	Yes
Sample E	InAlN HEMT	No	-
Sample F	InAlN MISHEMT	Yes	Yes

Device fabrication process started with mesa isolation by Cl_2-based inductively coupled plasma (ICP) etching. Alloyed ohmic contact of Ti/Al/Ni/Au metal stack was then deposited and annealed at 800ºC for 30s in N_2 and 850ºC for 30s in forming gas (H_2/N_2)[2], respectively. Based on transmission line measurement results, the ohmic contact resistance (R_c) for AlGaN/GaN HEMT and MISHEMT were extracted to be 0.36±0.05 Ω·mm and 0.39±0.04 Ω·mm, while that of InAlN/GaN were 0.43±0.05 Ω·mm and 0.49±0.05 Ω·mm. To further improve the device performance, we carried out an extra step of 12 min N_2O surface treatment before the TiO_2 deposition according to our previous work[210]. For MISHEMTs, the 15 nm TiO_2 gate dielectric was deposited followed by the 0.5 min N_2O plasma surface treatment. Finally, the Ni/Au stack was deposited as gate electrode for all devices, completing the device fabrication. All devices

feature a gate length (L_g) of 2 μm and a gate-source and gate-drain distance of 3 μm. **Fig. 38(c)** shows the microscope image of a representative fabricated device. Table 1 shows the detailed fabrication conditions of each sample.

RESULTS AND DISCUSSION

Fig. 39(a) presents the transfer curves of the fabricated AlGaN/GaN HEMTs and MISHEMTs at V_{DS} = 10 V. Comparing sample A and B, it is shown that the MISHEMT with N_2O plasma treated TiO_2 dielectric exhibits a low gate leakage current of 1.03×10^{-7} A/mm and an on/off ratio of 1.19×10^{7} which is 2 order higher than HEMT. Comparing sample C and A, the leakage current decreased by 2 orders. The N_2O pre-treatment can increase the 2DEG electron mobility due to the weakened polar optical phonon, interface roughness and polarization Coulomb field scatterings[210], leading to better device performance. Comparing sample D and C, it is shown that the two-step N_2O treated MISHEMT exhibits a low gate leakage current of 4.72×10^{-9} A/mm and on/off ratio of 1.44×10^{8}, which is almost 2 order magnitude higher than that of treated HEMT. This indicates that the TiO_2 film still plays a very important role even when the pre-treated HEMT leakage current is already very low. The *SS* of TiO_2 MISHEMT is calculated to be 85 mV/dec, standing in contrast to 150 mV/dec obtained from HEMT.

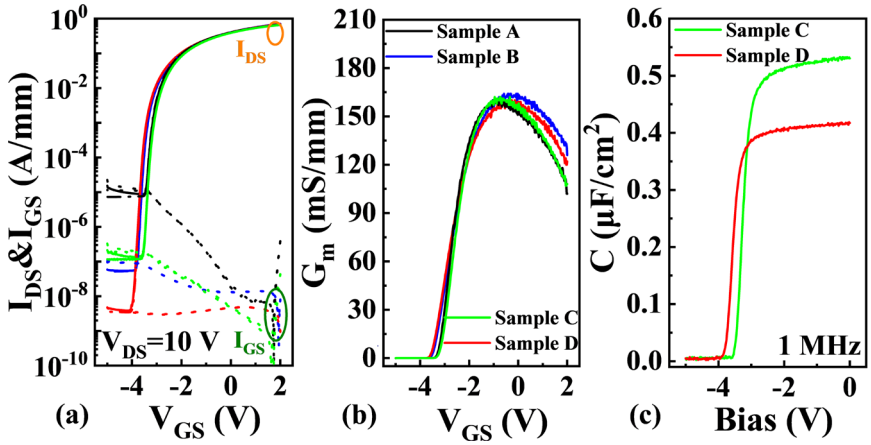

Fig. 39. (a) Double sweep transfer curves in log scale at V_{DS} = 10 V for AlGaN HEMTs and MISHEMTs; (b) Transconductance at V_{DS} = 10 V. (c) The gate-diode capacitance of sample C and D.

Fig. 39(b) shows the corresponding transconductance as a function of gate voltage at V_{DS} = 10 V. Theoretically, the insertion of TiO_2 oxide should result in a reduced transconductance due to the reduced capacitance arising from the increased gate-to-channel distance separation. However, surprisingly, the peak transconductance for TiO_2 MISHEMT (sample B) is 160 mS/mm, which is even higher than that of the HEMT (sample A). This could be due to its large dielectric constant and the surface passivation effect (it exists in the device extension region), an indication of the great promise of using it as the gate dielectric and the surface passivation layer.

To find the dielectric constant, the capacitance voltage (C-V) characteristic of the gate diodes with a 1 MHz signal is measured as shown in **Fig. 39(c)**. The ε_{TiO_2} is calculated to be 33.1 from *C-V* curves[4], higher than the reported 28.5 of amorphous TiO_2 gate dielectric[211]. The interface

traps C_{it} is calculated to be 0.319 μF/cm^2 from *SS*[209].

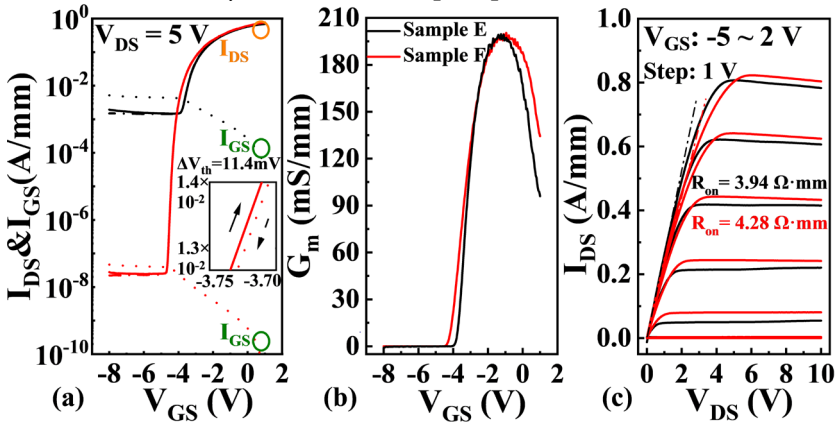

Fig. 40 (a) Transfer curves in log scale at V_{DS} = 5 V for InAlN HEMT and MISHEMT; (b) Extracted corresponding transconductance at V_{DS} = 5 V; (c) I_{DS}-V_{DS} characteristics of InAlN HEMT and MISHEMT.

Fig. 40(a) depicts the transfer curves of the fabricated InAlN/GaN HEMT and MISHEMT at V_{DS} = 5 V (Sample E and F). The transfer curves show that MISHEMT with TiO_2 dielectric exhibit an on/off ratio of 2.9×10^7 which is much higher than that of the HEMT. The *SS* of TiO_2/InAlN/GaN MISHEMT was calculated to be 82 mV/dec, standing in great contrast to 508 mV/dec obtained from HEMT. The reduced *SS* indicates the great improvement of the gate control capability and excellent gate switching characteristics. It also indicates a low interface trap density, manifesting a high interface quality of the TiO_2 gate dielectric. **Fig. 40(b)** shows the corresponding transconductance as a function of gate voltage at V_{DS} = 5 V. The peak transconductance for MISHEMT is 200 mS/mm similar to that obtained from the HEMT. Fig. 4(c) shows the output characteristics of both devices at room temperature. The maximum output current at V_{GS} = 1 V for the HEMT and MISHEMT were 783 mA/mm and 804 mA/mm, respectively. At V_{GS} of 0 V and V_{DS} between 0~0.5 V, the HEMT on-resistance was calculated to be 3.94 Ω·mm, while the MISHEMT on-resistance was 4.28 Ω·mm. It should be noted that the insertion of high-κ dielectric layer increases the gate-to-channel separation, which only leads to a slight shift of threshold voltage when comparing HEMT and MISHEMT for both InAlN/GaN and AlGaN/GaN epi-structures. This may be due to the TiO_2 high dielectric constant nature.

Fig. 41(a) summarizes the on/off ratio and gate leakage current of AlGaN/GaN, InAlN/GaN HEMT and MISHEMT. After applying the TiO_2 gate dielectric, the on/off ratio of AlGaN/GaN device improves ~3 orders, and that of InAlN/GaN device improves ~5 orders. The gate leakage current of both kinds of devices decreases ~5 orders. **Fig. 41(b)** compares the on/off ratio and *SS* of this work with previous published GaN-based MISHEMT with TiO_2 dielectric[209, 211-215]. It is shown that our MISHEMTs feature the highest on/off ratio among all reported TiO_2 based GaN MISHEMTs. Besides, the TiO_2/InAlN/GaN MISHEMT exhibits the record low *SS* and a record high transconductance compared with previous reported TiO_2 gate dielectric MISHEMTs. Such excellent performance shows that the N_2O plasma treated TiO_2 has great potential to be used as a high-κ gate dielectric for all other transistors.

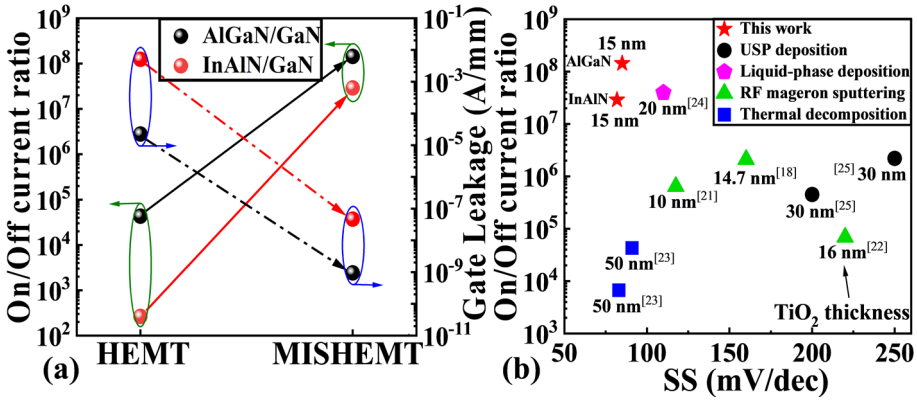

Fig. 41. (a)The on/off ratio and gate leakage current of AlGaN/GaN, InAlN/GaN HEMT and HEMTs; (b) Comparison of on/off ratio and *SS* for MISHEMTs with TiO_2 dielectric.

7.4 Summary

In this work, TiO_2 films with N_2O plasma surface treatment were optimized and used as the gate dielectric in AlGaN/GaN and InAlN/GaN MISHEMTs. The TiO_2 film shows a dielectric constant of 33.1 and a two-terminal current of 1.96×10^{-10} A/mm. The AlGaN/GaN MISHEMT shows an on/off ratio of 1.44×10^{8} and a low *SS* of 85 mV/dec while the InAlN/GaN MISHEMT shows a high on/off ratio of 2.9×10^{7} and a record low *SS* of 82 mV/dec. The superior TiO_2 MISHEMTs performance indicates that N_2O plasma treated TiO_2 has the great potential to be used as a high-κ gate dielectric.

8. TCAD simulation (unpublished)

We have built an initial TCAD model and predicted GaN HEMT DC and RF performance.

For simplicity, initially, we did not consider traps and thermal effects. We took into account the physical mechanisms which include piezoelectric polarization effect of the GaN, AlN, InAlN, InGaN semiconductors, fermi distribution of the carriers, the electron's high-electric-field-saturation effect (when calculating its mobility), electron barrier tunneling at the Schottky gate contact. We then manually turned off the piezoelectric polarization effect at the interface between GaN buffer and insulator substrate. We optimized the mesh grid of the device structure to reduce the simulation time consumption while maintaining a sufficient accuracy.

While fitting the experimental data, we reasonably adjusted some parameters. For example, by assuming: (1)90% strain activation of the entire piezoelectric polarization effect; (2)electron mobility of GaN semiconductor μ_e of 1205 $cm^2/(V.s)$; (3)contact resistance of both the drain and source: R_C = 250 Ω; (4)electron barrier tunneling effective mass for the Schottky gate electrode: $m_{t,e} = 0.1m_0$, we were able to fit one of our experimental results as shown in **Fig.42**. Incorporating these parameters and models, we also expect to be able to predict the device RF performance.

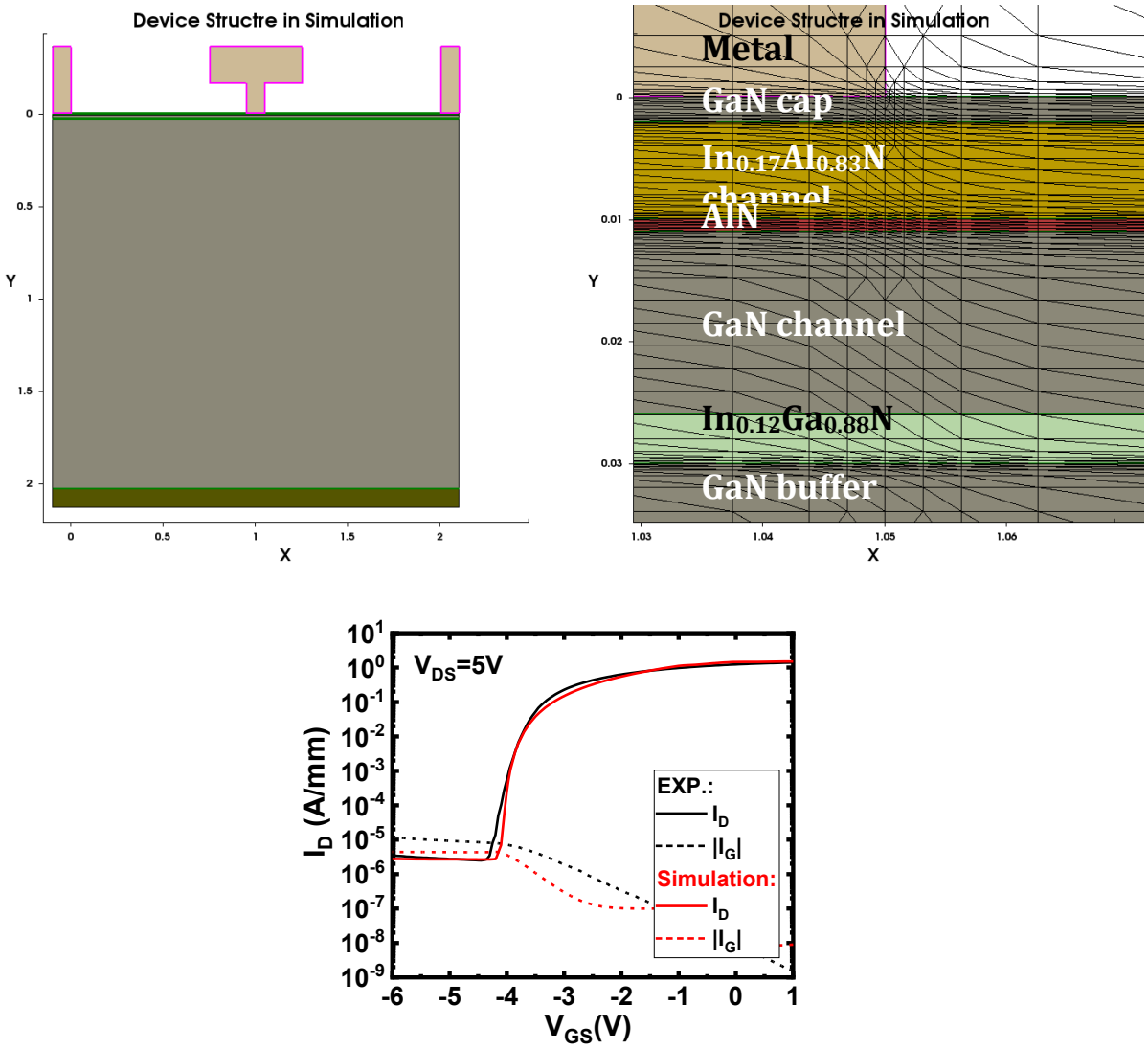

Fig.42 Simulated and experimental transfer curves and gate leakage characteristics of a transistor with 100nm T-shaped gate length at VDS of 5V.

Based on this models, the device RF and power performance for devices with different architecture can be predicted. Here, an example is shown in **Fig.43**. A gate field plate was employed to enhance the device power performance. Our preliminary simulation results indicate that, device structure with the conventional rectangular field plate shows enhanced power performance. The device with the field plate shows a higher breakdown voltage (2626V vs 2290V) than that without field plate. A further downscaled transistor with 20nm long gate reveals the breakdown voltage of 1550V with on-resistance of 0.298 $m\Omega.cm^2$ (close to its theoretical limit). Further optimizations on the field plate geometry can be performed to further improve device performance.

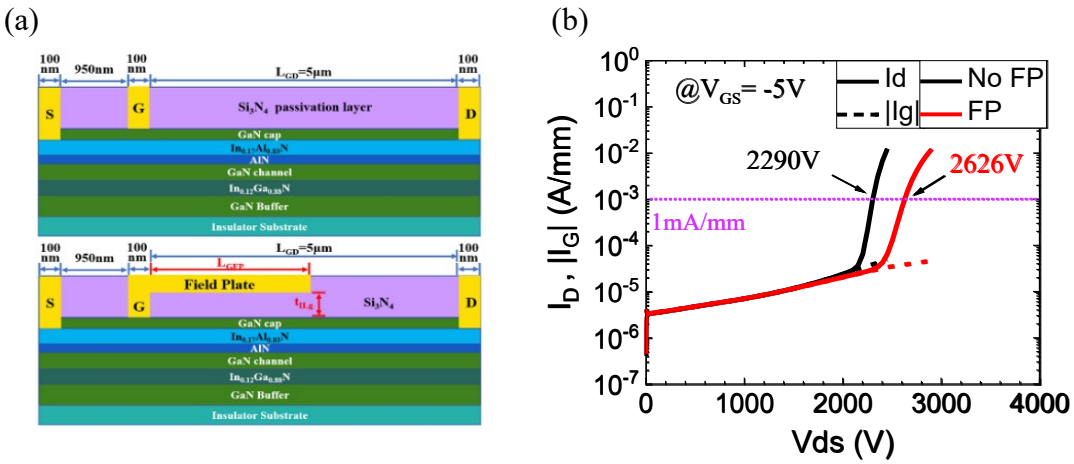

Fig. 43 TCAD simulation results on breakdown voltage with/without field plate.

9. Conclusion

We have demonstrated high performance GaN-on-Si HEMTs and MISHEMTs including DC and RF performance by innovative techniques in material design and device fabrication processes. These techniques include dielectric free plasma treatment, surface treatments (superacid treatment and N_2O treatment), high quality ZrO_2 dielectric, two-step annealing contact annealing process, T-shaped gate, high-k dielectric, etc.

(1) We have achieved GaN-on-Si HEMTs with high cutoff frequencies of 214GHz/270GHz, highlighted by more than 10 news media including "Semiconductor-Today", etc.

(2) We have demonstrated sub-60mV/dec InAlN/GaN HEMTs for the first time. Various material characterizations and electrical characterizations reveal that our techniques are essential for enhancing the device performance.

(3) With HfZrO, we demonstrated MISHEMTs with I_{ON}/I_{OFF} of 9.3 × 10^7, SS of 130 mV/dec, DIBL of 45 mV/V, f_T/f_{max} of 155/250 GHz, $(f_T \times f_{max})^{1/2}$ of 197 GHz, and JFOM of 5.4 THz·V. Power performance at 30 GHz exhibit a saturation P_{out} of 1.36 W/mm, a maximum G_P of 12.3 dB, and a peak PEA of 21%, demonstrating the great potential of the HZO/InAlN/GaN MISHEMTs for Ka-band applications.

(4) We have developed a reliable GaN HEMT device model in TCAD, which can be used for other GaN-related device performance prediction. Excellent power performance has been predicted using our technology platform.

(5) Our technology with downscaled gate length of 20nm will exhibit f_T/f_{MAX} of 320/535GHz.

(6) Our recently developed N_2O treated TiO_2, high quality ZrO_2, TiAlO dielectrics have been used for further enhancing GaN-on-Si MISHEMTs performance for high power RF applications. The developed TiO_2 dielectrics can be extended to enable other transistor performance. Rutile TiO_2 with a dielectric constant of 80-120, has a great potential to be used for enhancing high RF and high power performance, not only as the dielectric, but also as the passivation layer.

The carrier transport mechanisms of all the fabricated RF and power devices are now under investigation of Prof. Ashwani Sharma. Once understanding the device carrier transport, power performance and temperature stability, we will apply more innovations in fabrication techniques including high temperature contact schemes, surface passivation techniques to enhance the transistors stability, expecting to bridge the technology gap between GaN-on-SiC and GaN-on-Si.

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