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RAPID MODELING AND ANALYSIS FRAMEWORK FOR FULL-CHIP/PACKAGE/BOARD LAYOUT AUTOMATION

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14. ABSTRACT

Rapid and accurate layout modeling and analysis at a scale as large as full-chip, complete package and whole board is one of the key enablers to the success of machine generated physical layout in fast CPU run time. Existing layout tools lack such a capability, which has resulted in frequent layout failure and time intensive manual correction of the layout. In this work, PI Jiao has developed algorithms and software for rapid and first-principle-accurate full-chip/package/board layout modeling and analysis, and used such a capability to guide layout synthesis in a fast turnaround time.

15. SUBJECT TERMS

parasitic extraction, layout simulation, first-principles accuracy, large-scale modeling and analysis

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Table of Contents

Section **Page**

List of Figures

Figure **Page**

1 INTRODUCTION

1.1 Problem Statement

One of the key deficiencies in existing layout automation tools is the lack of accurate and large-scale layout models, because existing models, be they C- (capacitor), RC- (resistor-capacitor), RLC- (resistor-inductor-capacitor), or full wave S-parameter based, do not represent the correct physics of the global electrical interactions occurring on the chip, in the package, and on the board. A physical design tool built upon inaccurate or erroneous layout models, no matter how superior it is in machine learning and optimization algorithms, will fail to generate a working layout within feasible run time. Even though there exist a few layout automation tools in the market for analogue design, large discrepancies have been frequently reported between schematic-level simulations and post-layout simulations, as well as real measurements of the fabricated product in analog, mixed-signal SoC, and package/board design. This has forced designers to go through multiple time intensive design iterations. In many circumstances, designers have to rely on layout engineers' years of experiences to manually fix the layout, the process of which is labor intensive, time consuming, and often results in a compromised circuit performance. The key enabler for the success of machine generated physical layout with "no human in the loop" is a correct layout model, which has first-principles physics-based accuracy, and meanwhile can be generated in a fast turnaround time, for scales as large as full-chip, package and board. Such a model generated directly in time domain at the desired locations in the layout will also alleviate the simulation burden at the SPICE level because no netlist is required to represent the layout. In this project, PI Jiao has developed fast algorithms and software for full-chip, complete-package, and whole-board layout modeling and analysis, which can be used to guide every step of a physical design, from schematic level design to floor planning, placement, clock-tree synthesis, routing, and layout.

1.2 State-of-the-Art Layout Modeling and Simulation

In existing layout automation tools, the physical layout of an IC, package, or board is modeled either as C-, RC-, RLC-, transmission line, impedance- or S (scattering) parameters-based full wave models. In C-based models, given an electric potential source, the charges on the conductors are solved from a partial differential equation (PDE)- or an IE-based solver of Laplace's equation in inhomogeneous materials; to generate an RC-model, the R is separately extracted, and then stitched with C elements to build an equivalent RC model; in RL-based models, a magneto-quasistatic problem is formulated in the physical layout, from which the R and L are extracted. One can argue that at relatively low working frequencies, the RC- and RLC-based models obtained from decoupled Maxwell's equations are sufficiently accurate. However, even at these frequencies, there exist distributed effects as well as 3-D effects, which have not been well captured by existing layout models. As another example, the substrate is one of the main sources for interference and crosstalk. However, the global effect of the substrate is not well captured in existing layout models. As far as full wave modeling is concerned, although it is accurate at high frequencies, existing methods have a limited capability. They are not capable of performing extraction and simulation at the full-chip scale in fast CPU run time. Many of these tools require a 3D mesher. The meshing of a full package alone would take more than one day, not mention it may not be feasible. In addition, the direct field-based representation of the layout and the resulting field solution remain too abstract to be put into practical use by circuit designers as they are more grounded in circuit theory.

The extracted layout models are typically simulated in SPICE-type circuit simulators to evaluate the performance of an analog or mixed-signal IC. SPICE is highly capable of simulating active devices; however, it can no longer cope with the increasingly complex modeling of the layout. In the early years, the interconnects are modeled simply as lumped capacitors, and the physical layout is a very small component of an IC. The exponentially increased complexity of ICs, however, has made circuit simulation increasingly challenging. Even though the simulation of a circuit is the end goal, the state-of-the-art circuit simulation flow involves first the construction of an RLC-based, T (transmission)-line-based, or S-parameters-based model of the layout; this step is called parasitic extraction. The extracted model of the layout is then stitched with the nonlinear devices for the simulation of the entire circuit. The sheer dominance of the layout over the nonlinear network in analogue, mixed-signal ICs, SiPs, and PCBs poses challenges to the prevailing simulation paradigm in both extraction and simulation.

1.3 Contributions of This Work

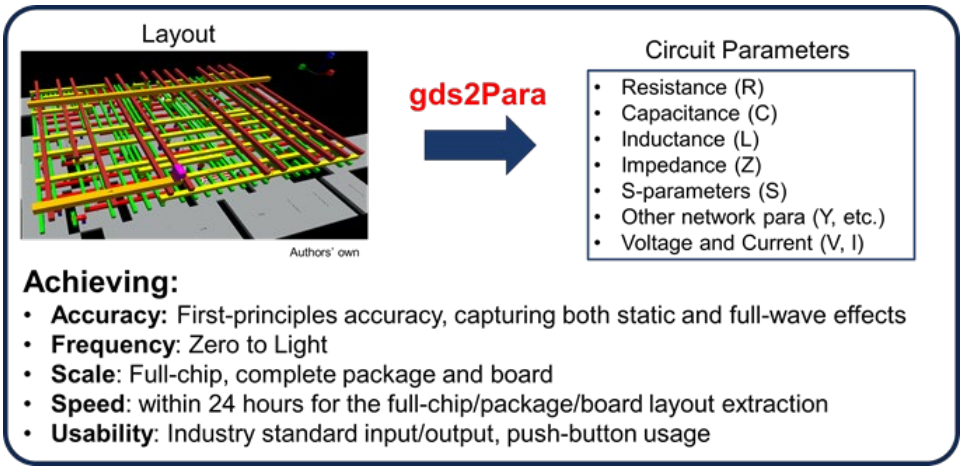

Figure 1: Capabilities Achieved in this Work

In this project, we have accomplished a breakthrough in layout modeling and simulation algorithms for full-chip, complete-package, and entire-board layout generation, which offers not only unprecedented first-principles accuracy but also unparalleled efficiency. Such a capability is then used to guide every step of a physical design tool to automate the layout generation. Starting from full wave Maxwell's equations where **E** and **H** are coupled, we derive an RLC representation of the layout with neither numerical computation nor approximation. We then decompose the solution of full wave Maxwell's equations rigorously into two components: RC-component and RL-/full wave components, again with neither numerical computation nor approximation. Such a decomposition is drastically different from existing practices, where a quasi-static or static version of Maxwell's equations is first solved, and then the solutions of decoupled **E** and **H** are combined in a manner of stitching extracted RC, and L elements. Here, we start from a full wave coupled Maxwell's equation, and then show its solution has two components, each of which can be found individually, and then superposed together to obtain the total solution in a physical layout. In this way, not only many accuracy issues related to existing layout modeling can be well addressed, but also, we speed up full wave simulations because if the RC-effects of a layout are dominant, we can avoid computing the other component that captures RL- and full wave effect. In contrast, in existing full wave simulations, even though what is being analyzed is an RC layout, the whole full wave solution still has to be

computed. The proposed decomposition will provide circuit designers with many new insights to enhance his/her understanding of the physical layout. After decomposing the full wave solution into RC- and RL-/full wave components, we develop fast and large-scale solution algorithms to find each component in optimal (linear) complexity. In devising these algorithms, many steps are also made analytical, thus bypassing numerical computations. Furthermore, the proposed modeling and simulation algorithms permit an embarrassingly parallel implementation, and thereby achieving linear speedup by exploiting the parallelism provided by the many cores on a chip or a cluster of nodes. We also propose algorithms to address process variations, layout variations, and design-parameter variations.

The proposed fundamental breakthroughs in layout modeling and simulation algorithms can be applied to perform large-scale parasitic extraction, timing analysis, power and signal integrity analysis, and guide every step of a physical design where the layout effects need to be assessed or incorporated. Moreover, if the simulation is the end goal, the proposed work can also be used as a "from layout directly to simulation" layout simulator, thus completely removing the step of layout parasitic extraction.

In this work, PI Jiao has developed the aforementioned fast algorithms and software for rapid and first principle-accurate full-chip/package/board layout modeling and analysis and used it to guide fast and accurate layout synthesis and automation. The major accomplishments are illustrated in Figure 1. Comparisons with state of the art are given in Figure 2.

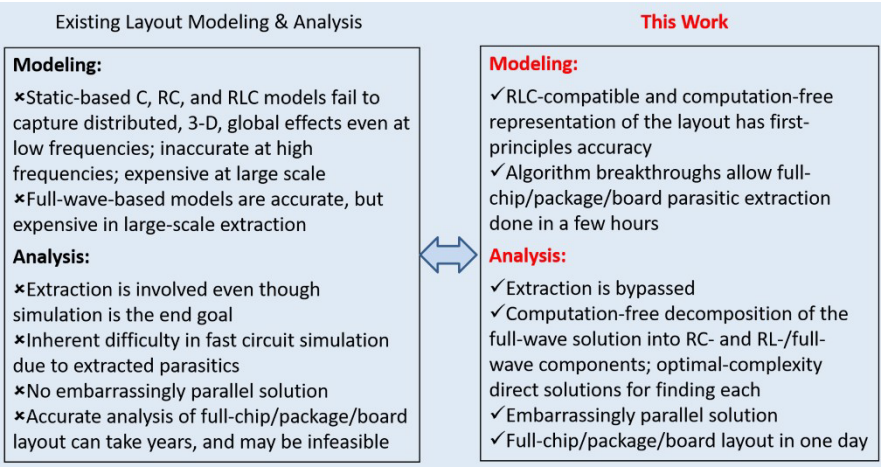

Figure 2: Comparisons with State of the Art

2 PROPOSED METHODS

2.1 Rapid Modeling and Simulation of Integrated Circuit Layout in Both Frequency and Time Domain from the Perspective of Inverse

Starting from full wave PDE based Maxwell's equations where **E** and **H** are coupled, we derive a closed-form model of the inverse of the Maxwell's system of equations in the physical layout of an integrated circuit, package, and board. In this model, we decompose the inverse rigorously into R-, C, L- and full wave components, with neither numerical computation nor approximation, and for an arbitrary physical layout. As a result, each component can be found independently, and then superposed to obtain the total response of a layout to any circuit stimuli. The time marching and point-by-point frequency sweeping are also avoided for the RC-component as this component's time and frequency dependence is analytically revealed in the proposed model. Moreover, the full wave component is efficiently represented by a small number of high frequency modes.

Using the proposed model, not only many accuracy issues related to existing layout modeling can be addressed, but also, we drastically speed up layout modeling and simulation, and provide circuit designers with an effective model for layout automation. In addition, we develop fast and large-scale algorithms to find each component of the inverse rapidly, where many steps are made analytical, thus further saving CPU run time. The proposed work has been applied to largescale layout extraction and analysis. Superior performance has been demonstrated in accuracy, efficiency, and capacity.

More details can be found in the following paper:
L. Xue and D. Jiao, "Rapid Modeling and Simulation of Integrated Circuit Layout in Both Frequency and Time Domain from the Perspective of Inverse," *IEEE Trans. Microw. Theory Tech.*, vol. 68, no. 4, pp. 1270-1283, April 2020.

2.2 Fast Method for Accelerating Convergence of Iterative Partial Differential Equation Solvers by Changing System Matrix to Laplacian Counterpart

We find that the matrix representing the curl-curl operator in a partial differential equation solver of Maxwell's equations can be analytically decomposed into a gradient divergence operator and a Laplacian, both of which can be constructed from the mesh information without any need for computation. The curl-curl operator can hence be replaced by the Laplacian to find the divergence-free component of the field solution. The Laplacian is positive definite and well-conditioned. As a result, the convergence of an iterative solution of Maxwell's equations can be guaranteed, and also significantly accelerated.

Based on the finding, we represent the divergence-free component of the unknown field solution by deducting its curl-free component. The curl-free component resides in the nullspace of the curl-curl operator, which is also analytically known from the mesh information no matter it is a regular grid or an unstructured mesh. After the divergence-free component is rapidly solved from a Laplacian counterpart of the original system matrix, the curl-free component can also be solved from a Laplacian matrix, and hence having fast and guaranteed convergence. The total computational cost of the proposed method is simply a small number of sparse matrix-vector multiplications. The proposed

method has been successfully applied to solve ill-conditioned, on-chip, packaging, and antenna radiation problems at both low and high frequencies, involving both inhomogeneous dielectrics and lossy conductors. Numerical experiments have demonstrated its fast and guaranteed convergence, as well as trivial computational cost independent of problem size.

More details can be found in the following paper:
L. Xue and D. Jiao, "Fast Method for Accelerating Convergence of Iterative Partial Differential Equation Solvers by Changing System Matrix to Laplacian Counterpart," *IEEE Trans. Antennas Propagat*., accepted, 2020.

2.3 Application to Layout Automation

Given the complete layout of a full-chip SoC, SiP, or PCB, the proposed simulator can finish the layout simulation within one day. The outputs include current, voltage, and fields anywhere inside the physical layout, in both time and frequency domain.

The proposed advanced algorithms not only can be used to establish a new physical design flow completely bypassing layout extraction, but also can be employed to significantly accelerate the computation in existing physical design flow, where parasitic extraction is required. We use the proposed fast solution algorithms to simulate the layout and obtain the desired layout model. First, we obtain the RC component of the full wave solution for a given excitation; then we obtain the RL-/full wave component if it is important. Adding the two together makes the total solution. From the solution at the desired ports, we can extract any network parameters of interest such as the impedance (Z)-, Scattering (S)-parameters etc. The parasitic extraction results can be provided in both frequency and time domain.

A parasitic extraction tool that can finish layout extraction of a function block in a few hours. The input of the parasitic extraction tool is a GDS file that specifies the geometrical and material information of the layout. The physical locations of the pins/ports for layout model generation should also be provided. The output of our tool is the impedance (Z)-, scattering (S)-, or any other network parameters at the ports of interest. Both frequency-domain and time-domain models can be generated from this tool. Furthermore, given a power delivery network of a chip, package, and board, we can provide static IR drop as well as transient voltage map for any given stimuli, and thus performing power integrity analysis.

3 RESULTS AND DISCUSSION

3.1 gds2Para Software

OpenSource at GitHub: https://github.com/purdue-onchip/gds2Para/

This project involves a significant amount of work in software development, where multiple graduate students have worked on for three years. Figure 3 shows the flowchart of the entire gds2Para tool, where a gds file is loaded, and the layout specified in the gds file is analyzed to produce electrical parameters.

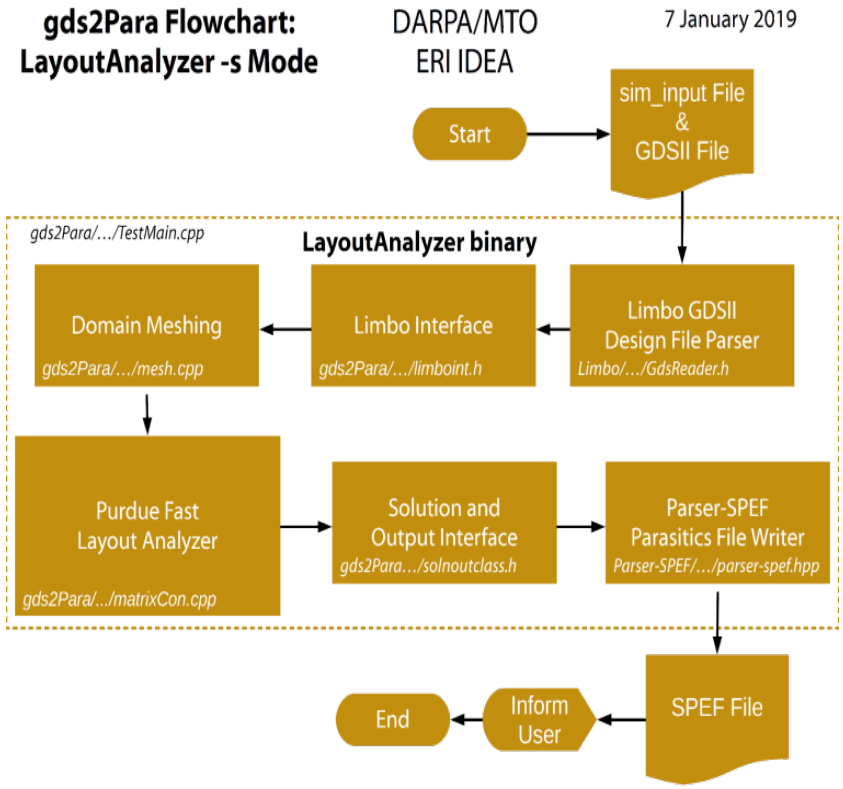

Figure 3: Flowchart of the gds2Para Tool

3.2 Full-Chip Layout Modeling and Simulation

The application of gds2Para ranges from on-chip extraction to package and board modeling and analysis.

As an example, here is an ASAP 7nm design involving 9 metal layers and 16724 nets provided by OpenRoad team, as illustrated in Figure 4. Our tool gds2Para successfully simulated the entire layout for a given current stimulus. The voltage distribution across the entire chip can be seen from Figure 5. The run time is only 1164 s with the layout discretized into over 86 million unknowns on a single core running at 3 GHz. In addition to direct layout simulation, we also support the traditional analysis mode, where each net is extracted as a netlist and output into a .spef file. Different from traditional

RC extractors, the R and C are coupled to extract in gds2Para, which is important for accuracy when the layout is a complicated 3-D structure.

- On-Chip Parasitic Extraction and Circuit Simulation

ASAP7 design: M1-M9, 16724 nets (source: UCSD OpenRoad)

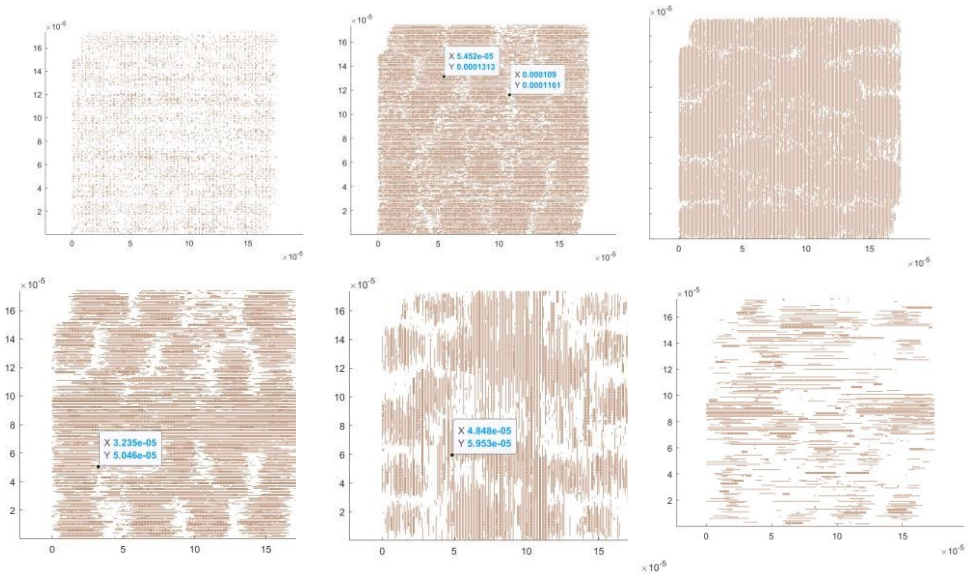

Figure 4: Layout of an ASAP 7 nm Design
Voltage distribution across the chip

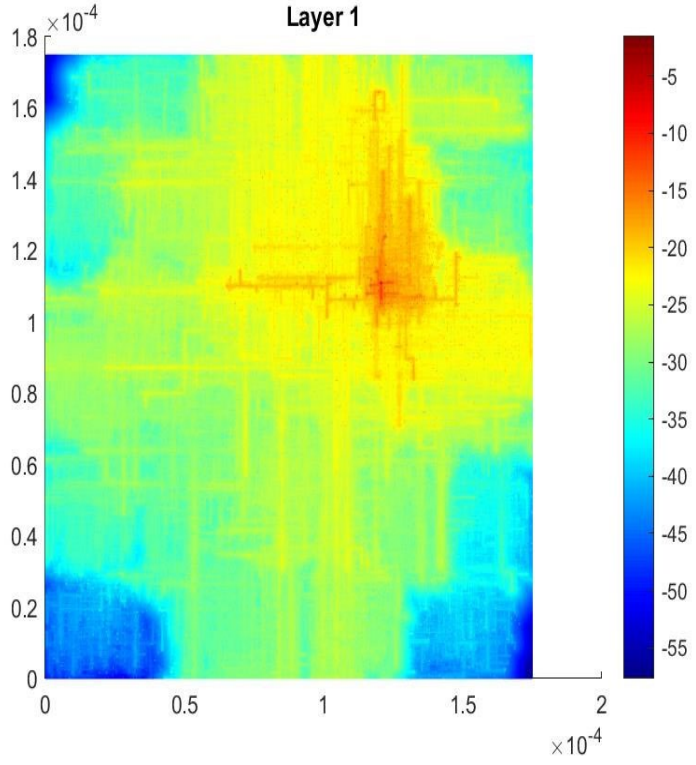

Figure 5: Voltage Distribution across the Chip of an ASAP 7 nm Design

3.3 Complete Package Extraction

Here is an example provided by IBM. It is a full package involving a whole stack of package substrate. The gds2Para was used to extract S-parameters at ports of interest, and shown to agree very well with reference data which was validated by measurements.

- IBM Plasma Package Extraction

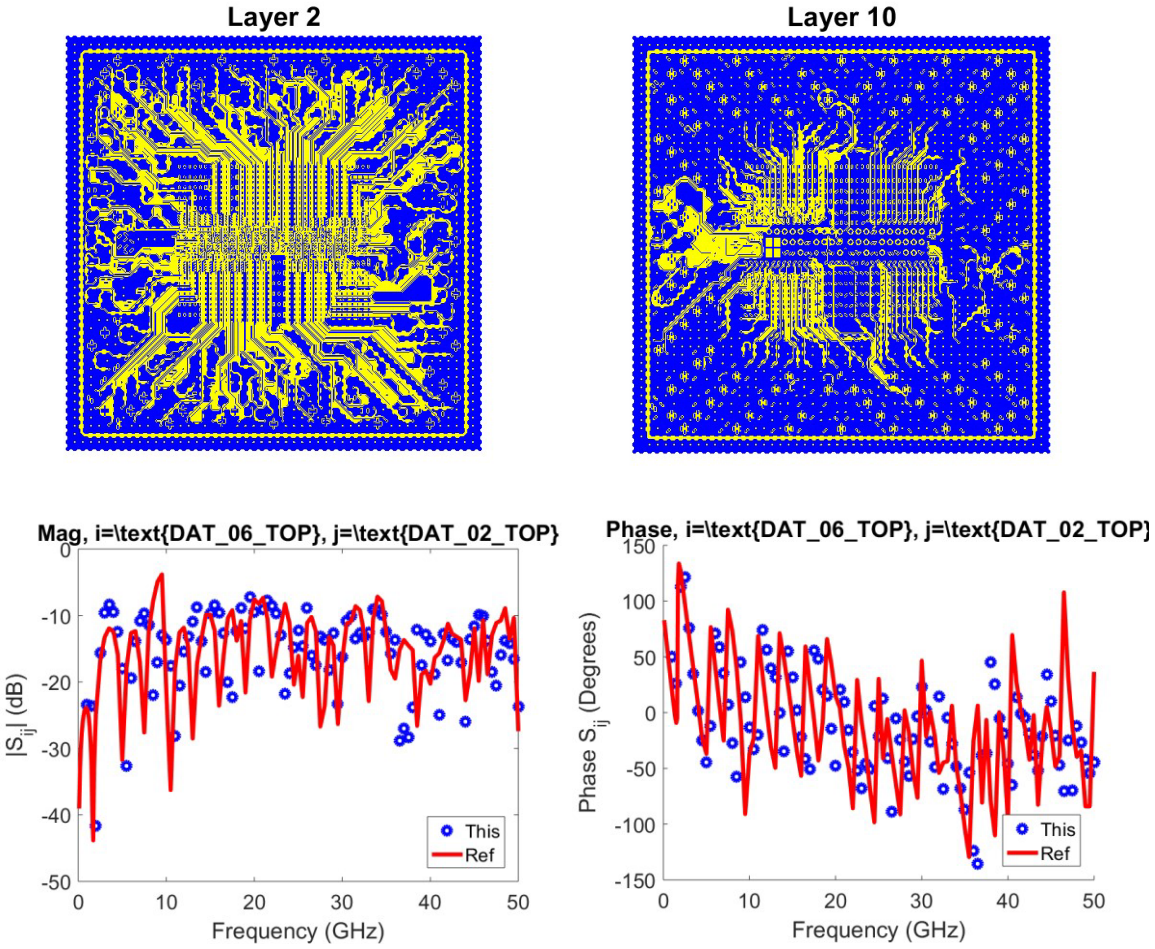

Figure 6: S-parameters Extracted from an IBM Package

4 CONCLUSIONS

This project addresses TA-1: Machine Generated Physical Layout. It offers not only unparalleled efficiency but also unprecedented first principles-based accuracy in layout modeling and analysis, for scales as large as full-chip/package/board. The research outcome can be used to guide every step of a physical design to automate the layout generation with guaranteed success. Defense companies and research labs are potential technology transition partners in DoD such as NGC, Boeing, AFSOR, Navy, Army Research Lab, etc.

5 PUBLICATIONS OF THIS PROJECT

This project has resulted in 28 publications as follows.

[1] M. Ma and D. Jiao, "Direct Solution of General ${\mathcal H}^2$-Matrices with Controlled Accuracy and Concurrent Change of Cluster Bases for Electromagnetic Analysis," IEEE Trans. Microw. Theory Tech., vol. 67, no. 6, pp. 2114-2127, June 2019.

[2] S. Sun and D. Jiao, "First-Principles Based Multiphysics Modeling and Simulation of On-Chip Cu-Graphene Hybrid Nano-Interconnects in Comparison with Simplified Model Based Analysis," IEEE Journal on Multiscale and Multiphysics Computational Techniques, vol. 4, pp. 374-382, 2019.

[3] L. Xue and D. Jiao, "Method for Analytically Finding the Nullspace of Stiffness Matrix for Both Zeroth- and Higher-Order Curl-Conforming Vector Bases in Unstructured Meshes," IEEE Trans. Microw. Theory Tech., vol. 68, no. 2, pp. 456468, Dec. 2020.

[4] S. Sun and D. Jiao, "Multiphysics Modeling and Simulation of 3-D Cu-Graphene Hybrid Nano-Interconnects," IEEE Trans. Microw. Theory Tech., vol. 68, no. 2, pp. 490-500, Feb. 2020.

[5] L. Xue and D. Jiao, "Rapid Modeling and Simulation of Integrated Circuit Layout in Both Frequency and Time Domain from the Perspective of Inverse," IEEE Trans. Microw. Theory Tech., vol. 68, no. 4, pp. 1270-1283, April 2020.

[6] M. Ma and D. Jiao, "Accuracy Controlled Structure-Preserving ${\cal H}^2$-Matrix Matrix Product in Linear Complexity with Change of Cluster Bases," IEEE Trans. Microw. Theory Tech., vol. 68, no. 2, pp. 441-455, Feb. 2020.

[7] L. Xue and D. Jiao, "Fast Method for Accelerating Convergence of Iterative Partial Differential Equation Solvers by Changing System Matrix to Laplacian Counterpart," IEEE Trans. Antennas Propagat., accepted, 2020.

[8] L. Xue and D. Jiao, "Fast Time-Domain Method for Computing the Full wave Solution of Integrated Circuit Layouts by Changing the Curl-Curl Operator to Laplacian," IEEE Trans. MTT, accepted

[9] M. Ma and D. Jiao, "Accuracy Controlled Direct Integral Equation Solver of Linear Complexity with Change of Basis for Large-Scale Interconnect Extraction," IEEE International Microwave Symposium (IMS), June 2018.

[10] M. Ma and D. Jiao, "Accuracy Controlled H2-Matrix-Matrix Product in Linear Complexity and Its Applications," IEEE International Symposium on Antennas and Propagation, July 2018. (**HONORABLE MENTION AWARD**, $1500 STIPEND)

[11] L. Xue and D. Jiao, "Fast FDTD Method for Large-Scale Layout Extraction and Analysis of Integrated Circuits," IEEE International Symposium on Antennas and Propagation, July 2018.

[12] L. Xue and D. Jiao, "Broadband and Sparse Finite-Element Formulation Free of Low-Frequency Breakdown," IEEE International Symposium on Antennas and Propagation, July 2018.

[13] S. Sun and D. Jiao, "Transient Multiphysics Simulation of High-Speed GrapheneBased Interconnects," PIERS 2018, Aug. 2018. (**INVITED**)

[14] M. Ma and D. Jiao, "Accuracy Controlled ${\cal H}^2$ Matrix-Matrix Product in Linear Complexity," PIERS 2018, Aug. 2018. (**INVITED**)

[15] M. Ma and D. Jiao, "Direct Solution of General H2-Matrix with Controlled Accuracy and Change of Cluster Bases for Large-Scale Electromagnetic Analysis," IEEE International Conference on Numerical Electromagnetic Modeling and Optimization (NEMO), Aug. 2018. (**INVITED**)
[16] M. Ma and D. Jiao, "Accuracy-Controlled and Structure-Preserved H2-MatrixMatrix Product in Linear Complexity," 2018 International Conference on Electromagnetics in Advanced Applications (ICEAA), Sept. 2018. (**INVITED**)
[17] M. Ma, D. Jiao, J. Yan, and J. Zhu, "Method for Accurate and Efficient Signaling Analysis of Nonlinear Circuits," SRC TECHCON, Sept. 2018.
[18] M. Ma and D. Jiao, "Non-Leaf-Level Algorithms in Structure Preserving HSS Matrix Inversion in Exact Arithmetic," IEEE International Conference on Computational Electromagnetics (ICCEM), Mar. 2019 (**Ulrich L. Rohde Paper Award Finalist**)
[19] M. Ma and D. Jiao, "Direct Factorization of General ${\mathcal H}^2$-Matrices with Controlled Accuracy and Concurrent Change of Cluster Bases for Large-Scale Circuit Extraction," IEEE International Conference on Computational Electromagnetics (ICCEM), Mar. 2019 (**Best Student Paper Award Finalist**)
[20] L. Xue and D. Jiao, "Method for Analytically Finding the Null Space of Stiffness Matrix for Both Zeroth- and Higher-Order Curl-Conforming Vector Bases," IEEE MTT-S International Conference on Numerical Electromagnetic Modeling and Optimization (NEMO), May 2019.
[21] M. Ma and D. Jiao, "Accuracy-Controlled and Rank-Minimized H2 Matrix-Matrix Product with Change of Cluster Bases in Linear Complexity," IEEE MTT-S International Conference on Numerical Electromagnetic Modeling and Optimization (NEMO), May 2019.
[22] S. Sun and D. Jiao, "Multiphysics Modeling and Simulation of 3-D Cu-Graphene Hybrid Nano-Interconnects," IEEE MTT-S International Conference on Numerical Electromagnetic Modeling and Optimization (NEMO), May 2019
[23] L. Xue and D. Jiao, "Rapid Inverse Modeling of Integrated Circuit Layout in Both Frequency and Time Domain," IEEE International Microwave Symposium (IMS), June 2019 (**Best Student Paper Award Finalist**)
[24] L. Xue and D. Jiao, "Fast Finite Difference Method for First-Principles Based Parasitic Extraction of Integrated Circuits," IEEE International Symposium on Antennas and Propagation, July 2019.
[25] M. Ma and D. Jiao, "Linear-Complexity H2-Based Direct Sparse Solver for Electromagnetic and Multiphysics Analysis," IEEE International Symposium on Antennas and Propagation (AP-S), July 2019.
[26] S. Sun and D. Jiao, "Multiphysics Modeling of Crosstalk Effect in Graphene-Encapsulated Cu Nano-Interconnects," IEEE International Symposium on Antennas and Propagation (AP-S), July 2019. (**Best Student Paper Award Finalist**)
[27] Li Xue and D. Jiao, "Fast Method for Accelerating Convergence in Iterative Solution of Frequency-Domain Partial Differential Equation Methods," IEEE International Symposium on Antennas and Propagation (AP-S), July 2020. (**Best Student Paper Award Finalist**, $1600 Stipend)
[28] S. Sun and D. Jiao, "Split-Field Domain Decomposition Algorithm with Fast Convergence for Electromagnetic Analysis," IEEE International Symposium on Antennas and Propagation (AP-S), Dec. 2021. (**Best Student Paper Award Finalist**, $1600 Stipend), 2020.

LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS

ACRONYM	DESCRIPTION
C	Capacitor
RC	Resistor Capacitor
RLC	Resistor-Inductor-Capacitor
IC	Integrated Circuit
CPU	Central Processing Unit
PDE	Partial Differential Equation
SPICE	Simulation Program with Integrated Circuit Emphasis
IR	Current-Resistance
IBM	Name of a company