

# Homoepitaxy of III-Nitride Semiconductors

JENNIFER HITE  
MICHAEL MASTRO  
JAIME FREITAS  
EVAN GLASER  
JAMES GALLAGHER  
TRAVIS ANDERSON

*Power and Advanced Materials Branch  
Electronics Science and Technology Division*

DAVID STORM  
MATTHEW HARDY

*Electromagnetic Technology Branch  
Electronics Science and Technology Division*

JOHN LYONS

*Center for Materials Physics and Technology  
Materials Science and Technology Division*

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# HOMOEPITAXY OF III-NITRIDE SEMICONDUCTORS

## 1. INTRODUCTION

### 1.1 Objective

This program focused on understanding the fundamental issues involved in homoepitaxial growth of III-nitride semiconductors with the goal of enabling applications in the fields of high power and rf electronics as well as other novel areas.

### 1.2 Motivation

As a materials system spanning both wide (GaN) and ultra-wide (AlN) bandgaps, the nitride-based semiconductors are attractive for next-generation power devices, including RF amplifiers based on high electron mobility transistor (HEMT) structures, high voltage vertical diodes and power switches, resonant tunneling diodes, and optoelectronic devices. Such devices have a wide range of immediate naval applications, such as high-power satellite communications and radar, unmanned underwater and aerial vehicles, ship drive components, and hybrid vehicle inverters. Despite significant device breakthroughs involving III-nitride semiconductors, such as high efficiency blue LEDs and HEMT-based MMICs, there are still significant materials challenges that must be overcome to realize their full potential and enable widespread adoption and technology insertion.

Until recently, most nitride-based devices were limited to lateral devices, due to the lack of a native substrate which would permit vertical conduction through the substrate. Additionally, the use of a non-native substrate led to high defect densities, especially dislocations, which impacted device performance and application. The recent introduction, commercial availability, and improving quality of native III-nitride substrates will enable next-generation devices to be vertical in nature. A schematic of the difference between these devices is illustrated in Fig. 1. Although these substrates enable new vertical structures, in order for the homoepitaxial material to reach its full potential, there are several fundamental materials issues that must be addressed, from the substrate surface preparation to impurity and alloy incorporation in the active layers.

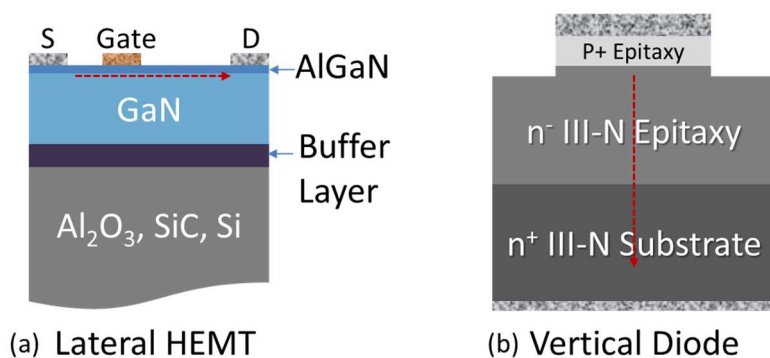


Figure 1. Shows the difference in geometry and current path (red dotted line) on (a) a standard lateral device, in this case and AlGaN/GaN HEMT grown heteroepitaxially on a non-native substrate and (b) a vertical p-i-n diode. In the lateral HEMT, the current path is at the surface of the wafer between the source and the drain. In the vertical, the path is from top to bottom, through both the epitaxy and the substrate.

### 1.3 Background

Currently, there are several vying techniques used to grow III-nitride substrates. For GaN, the two most prominent techniques are ammonothermal growth and hydride vapor phase epitaxy (HVPE). For AlN substrates, the primary growth technique is physical vapor transport (PVT). Dislocation densities in commercial products are approximately  $10^6 \text{ cm}^{-2}$  for HVPE,  $10^4 \text{ cm}^{-2}$  for ammonothermal, and  $10^3 \text{ cm}^{-2}$  for PVT. These levels are still higher than those in commercial SiC substrates ( $10^2$ - $10^4 \text{ cm}^{-2}$ ), but are much reduced in comparison to heteroepitaxial nitride growth on non-native substrates ( $10^{10} \text{ cm}^{-2}$  on sapphire). Additionally, some of the growth methods also result in large lattice bowing within the substrates [1]. The process of slicing wafers from such a boule with distorted crystal planes inherently leads to varying step density across the wafer.

Although the quality of the substrates has improved, there are several remaining issues to be overcome in the initial stages of growth on these substrates. SIMS analysis of homoepitaxial GaN films grown by molecular beam epitaxy (MBE) on both N- and Ga-polar GaN have shown a spike in impurities at the substrate interface, which can act as a leakage path in the buffer and requires additional intentional compensating impurities in order to mitigate this issue [2-4]. As the native oxide on AlN surfaces is bound even more strongly than that for GaN, this is due to be a bigger problem in the ultra-wide bandgap materials. Empirically, we have observed that incoming substrates from different vendors have vastly different surface polish quality. Additionally, the different step densities produced by lattice bow may affect the growth nucleation, surface morphology, and impurity incorporation. In order to grow epitaxially, surface preparation techniques must be developed to remove surface damage and adsorbates prior to growth and to provide a similar starting surface regardless of vendor.

In addition to challenges at the initial nucleation, there are additional challenges to be overcome in order to enable vertical devices. These include reducing impurity incorporations in order to controllably dope the films. For power switches, a drift layer is needed with electron carrier concentrations on the order of  $10^{15} \text{ cm}^{-2}$ . In order to reliably achieve these levels, intrinsic defects, compensating impurities, and unintentional dopants must all be understood and controlled at a level an order of magnitude less than this. Compensating impurities are also a problem in achieving p-type doping. These impurities must not only be controlled through growth parameters, but substrate effects must also be taken into consideration. Just as different crystallographic planes incorporate impurities at different rates, the different step densities may also influence impurity incorporation. This perspective explains the observed Si-concentration variation in high Al-containing AlGaIn films [5].

Additionally, the lower dislocation density in the III-nitride substrates enables a new examination into the role of dislocations as well as poses new challenges. NRL has shown that the dislocation density of the substrate can be propagated through the homoepitaxially grown films without the introduction of additional threading dislocations by both metal organic chemical vapor deposition (MOCVD) and MBE [6,7]. However, in heteroepitaxial growth, threading screw dislocations act as growth nucleation sites. The impact of lowered dislocation densities on growth mechanics needs to be understood. With the use of native substrates instead of heteroepitaxial growth, additional defects may arise from the substrate, such as basal plane dislocations. Additionally, many nitride defects deleteriously impact optical emission of the material. Understanding of the extended and point defects arising from the substrate as well as methods of reduction must be achieved. In GaN-based resonant tunneling diodes, repeatable negative differential resistance has been difficult to observe, ostensibly due in part to dislocations which can act as leakage paths [8]. This has been observed even when grown homoepitaxially on HVPE substrates, showing that further reduction of dislocation density is still necessary to fulfill the full potential of these types of devices. The limited supply of low-defects native substrates has prevented an understanding of the behavior of electronic and optical processes at low dislocation densities. Thus, the question in III-nitrides has now become how low in defectivity can we achieve and how low is actually necessary.

## 2. APPROACH

A cross section of a very simple vertical device structure, a Schottky diode, is shown in Figure 2. Our approach to form a fundamental understanding of homoepitaxial growth was to focus on several areas of interest. These include understanding the incoming substrate characteristics, the effects of the substrate on epitaxial growth and properties, the homoepitaxial interface characteristics, impurity incorporation within the epitaxial layers, and then how those issues affect device performance and processing. The samples in this work were grown either by metal organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE), with MOCVD being the dominant technique reviewed in Sections 3.1 – 3.5.3.

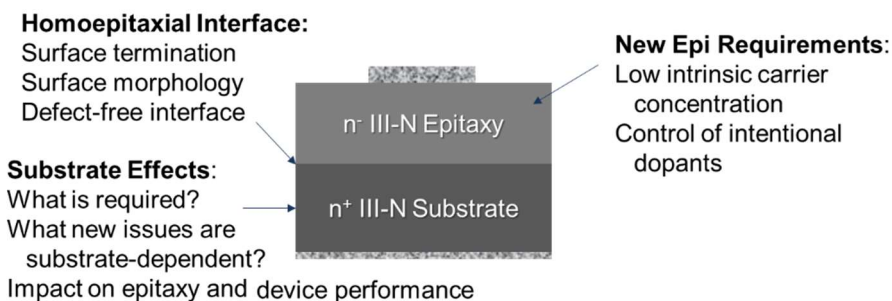


Figure 2. Cross-section of a simple Schottky diode where the layers consist of a highly doped native n-type substrate and a homoepitaxially grown n<sup>-</sup> drift layer, with metal contacts on both sides. The points of interest for the program are indicated.

## 3. RESULTS AND DISCUSSION

### 3.1 Understanding the Incoming Native GaN Substrates

The foundational step in moving GaN technology to a vertical geometry lies in the introduction of native, commercial substrates. With the introduction of these substrates, the first step is to fully understand the characteristics of the incoming material. At the beginning of this work, the technology was in its infancy, and substrate sizes were small (10 x10 mm<sup>2</sup> in some cases). By evaluating multiple wafers from several vendors using Raman spectroscopy, photoluminescence, white light optical profilometry, and Nomarski imaging, it was found that the quality and characteristics of the incoming substrates varied considerably. Various defects were seen in different wafers, including grain boundaries, large wafer bow, impurity incorporation, point defects, v-shaped cone defects, polishing defects, crystal stress damage, and varying insulating and conductive regions, all of which are concerning for a device technology. However, others were more uniform. All incoming wafers showed smooth surface morphology on a small scale, with sub-nm rms roughness, but often saw variations on a larger scale. The details of these results can be found in [9]. Throughout the maturing of the substrate technology, which also resulted in an increase in average wafer size to 2" diameter, incoming substrates were characterized using the long-range techniques previously mentioned. Over time, the substrates could be categorized into two types by their uniformity with respect to defects and carrier concentration: Type I which were highly uniform and Type II which were not. Type II were further divided into those with a regular, patterned non-uniformity (Type IIa) and those with a more random non-uniformity (Type IIb). This first group (Type IIa), although not as desirable as Type I substrates from a yield perspective, still allowed for further understanding of the non-uniformities on the epitaxial layers and on electrical performance. Further details of this work can be found in [10, 11]. As the substrate technology has progressed and these results were published, most manufacturers are now producing Type I substrates and wafers with up to 4" diameters have become available.

### 3.2 Substrate-Epitaxy Effects

#### 3.2.1 Roughness



The surface morphology of the substrate is replicated and exaggerated with increasing thickness in the epilayers. Samples with more surface morphology or polishing damage did not evidence step flow-growth. Details on the growth and results were published in [12].

### 3.2.2 *Inhomogeneity*

As mentioned earlier, Type II substrates showed inhomogeneity in carrier concentration through characterization using Raman spectroscopy mapping. Surprisingly, that inhomogeneity carried into the epitaxial layers. This was shown both in Raman spectroscopy mapping and photoluminescence measurements. Photoluminescence is extremely surface sensitive, and broadening of the near band edge emission from the GaN epitaxial layers grown on Type II substrates shows that this inhomogeneity in carrier concentration is present at the sample surface. Thus, changes in carrier concentration, if present in the substrate, continue to impact the epitaxial growth. Details of this work are found in [10, 12].

## 3.3 **Homoepitaxial Interface**

In general, a clean interface is highly desired at any regrowth interface – either substrate-epi or epi-epi, as impurities in the III-nitrides can lead to changes in carrier concentration, induce defects and dislocations, and inhibit thermal conductivity.

### 3.3.1 *Composition*

It had previously been published that the homoepitaxial interface of GaN grown by MBE shows a large concentration of oxygen, carbon, and silicon at the interface [3]. It was assumed that growing the homoepitaxial layers by MOCVD would reduce all of these contaminants, due to the use of hydrogen as a carrier gas at high temperatures during the ramp to growth temperatures. That was found to be true for C and O. However, regardless of the substrate vendor or substrate composition, a large, sharp peak in Si was observed in secondary ion mass spectroscopy data at the substrate-epi interface. This was found to only occur after the original GaN substrate surface was exposed to atmosphere, meaning the source of the silicon is not from within the reactor chamber. Additionally, in a controlled experiment varying the Si dopant level of the GaN substrate, it was established that the Si at the interface increased with increasing Si levels in the substrate. Theoretical calculations show Si to have the lowest energy barrier to incorporation of all group IV elements into GaN, meaning it will readily incorporate if on the surface of GaN, even at low temperatures. When ramping up to growth temperatures, the atmosphere in the MOCVD will clean the surface of hydrocarbons. Additionally, there is some decomposition of the surface. However, the MOCVD atmosphere does not remove the Si. Substrates with a larger Si composition would have more Si at the surface to be incorporated. Further details of this work can be found in [12-14].

### 3.3.2 *Thermal Conductivity*

With large amounts of Si at the interface, the effects on thermal conductivity needed to be understood. From time domain thermoreflectance and steady state thermoreflectance measurements of equivalent thicknesses of heteroepitaxial and homoepitaxial GaN films, it was determined that the homoepitaxial GaN films possessed much higher thermal conductivities than the heteroepitaxial material. The homoepitaxial films, even with layers as thin as 0.25  $\mu\text{m}$ , agree with or are slightly higher than the first principles lattice dynamics predictions. The mean thermal conductivities of the homoepitaxial films higher than the predictions may indicate scattering at the homoepitaxial interface in these calculations may not be as diffusive as assumed in the calculations. In general, this means that at room temperature, the high concentration of Si at the GaN/GaN homoepitaxial interface is not impacting the thermal conductivity of the material. However, it was observed that below 200 K scattering at the interface and defects begins to reduce the thermal conductivity. More details of this work and the techniques used can be found in [15,16].

### 3.4 Impurity Incorporation

There are many impurities incorporated into the III-nitride semiconductors during growth. In GaN, these include unintentional impurities (O, Si, C) and those intentionally added to add holes or electrons to certain epitaxial layers (Mg, Si), those added to compensate donors to produce semi-insulating layers (C, Fe, Mn, Be), and those used to alloy the materials to control the bandgap (In, Al, B). To support a thorough understanding of impurity incorporation, a tutorial was published [17]. In it, the basic concepts were explained defining the behavior of dopants, unintentional impurities, and point defects in GaN. It also described how to interpret experimental results in the context of theoretical calculations, and how defect properties vary in III-nitride alloys.

#### 3.4.1 Carbon in GaN

Carbon incorporation in GaN is extremely complex, as it can form states such as interstitials, self-compensating donors, deep acceptors, acceptor pairs, and other complexes [18]. In MOCVD-grown films, it is unintentionally incorporated from the metal-organic precursors used as a Group III source, such as trimethylgallium, trimethylaluminum, and trimethylindium. The level of carbon unintentionally incorporated can be somewhat controlled with growth conditions. In this program, it was also found that the unintentional incorporation of C changes with the substrate offcut, increasing with increasing offcut angle [12]. Theoretical efforts supported this finding, as calculations showed the lowest energy barrier for C incorporation is at a step edge. The higher offcut angle wafers have more steps so should incorporate more carbon into the homoepitaxial layers. Part of these calculations can be found in [19].

However, C can also be intentionally incorporated at high concentrations to produce semi-insulating GaN layers. The optical and electrical properties of heavily C doped GaN were studied using photoluminescence spectroscopy and hybrid density functional theory (DFT). Previous work had established that carbon acceptors ( $C_N$ ) give rise to a yellow luminescence band near 2.2 eV [20]. Photoluminescence measurements showed this optical transition shifting as a function of carbon concentration, suggesting a change in the behavior of carbon dopants. Hybrid DFT was used to calculate the electrical and optical behavior of carbon species containing multiple carbon impurities and compared the behavior of these complexes to the isolated centers. From this, the  $C_{Ga}-C_N$  complex is a good candidate to explain the shift in the YL peak. Furthermore, the local vibrational modes of carbon impurity centers were determined, and compared these results to recent experiments. Further details can be found in [21].

#### 3.4.2 Carbon in Ultra-Wide Bandgap III-Nitrides

With increasing bandgap, the ability to dope semiconductors becomes increasing difficult, with the proclivity to doping type depending on the band structure and defects [22]. For example, p-type doping in GaN is difficult, with Mg having an ionization energy  $>140$  meV and hydrogen (a carrier gas in MOCVD) forming a neutral complex with Mg that must be broken to achieve p-type conductivity. The situation is even more complicated in AlN and BN, both with bandgaps greater than 6.0 eV.

In AlN, theoretical investigations in hole behavior show that there is a small energy difference between delocalized and trapped holes in AlN, so small permutations in the lattice structure can result in hole trapping – forming transition levels. We see that most alloying elements (B, In, Sc) will trap holes, and the transition levels formed may explain deep optical signals in some of these alloys. Acceptor impurities also strongly trap holes – doing so by stabilizing 2 holes and forming 2 localized states, except for Be. The stability of the trapped holes increases with increasing size mismatch. Also, the ionization energy of all other acceptors investigated are higher than Mg. So, theoretically, none should be easier to use as a dopant than Mg. Details of this work are found in [23].

For cubic boron nitride (c-BN), another ultra-wide bandgap III-nitride semiconductor, hybrid DFT was used to address potential n-type dopants and compensating centers. This work investigated Si, Ge, S, Se, C, O, F, and Li as dopants. Many of these candidates' usefulness were impacted by self-compensation

or high formation energies. However, potential candidate donors were found in  $\text{Si}_B$  and  $\text{O}_N$ . For all of these dopants, compensation by boron vacancies remains a concern. Further details are in [24].

### 3.5 Effects on Processing and Device Performance

#### 3.5.1 Surface Roughness

To understand the effects of roughness on device performance, Schottky diodes were fabricated on a single 2" diameter wafer at the beginning of the program. Across this single wafer, large differences in leakage current and breakdown voltage were observed. Investigating the morphology around individual diodes showed an immediate correlation between large-scale surface roughness and device performance, where rougher areas showed increased leakage current and reduced breakdown voltage. Further details of the experimental details and results can be found in [25]. These findings helped establish the utility of using large-scale characterization techniques on both incoming substrates and epitaxy and were further supported by efforts in training neural networks to predict device performance from morphological data. These machine learning efforts have been able to predict device metrics with high accuracy using wafer morphology as the incoming data. This is the basis of one recently granted US patent, another patent application, and a manuscript currently under review [26, 27].

#### 3.5.2 Inhomogeneity

Comparing *p-i-n* diodes fabricated on Type I vs. Type IIa substrates revealed some issues due to inhomogeneity in carrier concentration as well as defectivity in the Type IIa wafers. The inhomogeneity was shown earlier to carry into the homoepitaxial films. Due to the regular, patterned nature of the inhomogeneity in the Type IIa substrates, devices could be aligned with respect to the inhomogeneous pattern. In comparison, device yield and performance on *p-i-n* diodes on Type I substrates are more consistent with higher yield and lower leakage current. However, devices with Type IIa substrates show the impact of locating devices over substrate defects – in this case, at stress centers (identified by Raman spectroscopy mapping of the E2 peak). In this case, the effects of the stress center seem to have the largest influence on devices, impacting the rectification ratio and increasing leakage current on devices directly over these defects. Further details can be found in [28].

#### 3.5.3 Metal-Assisted Chemical Etching (MAC)

In addition to understanding the influence of epitaxy and substrate on devices, novel processing will be necessary for several types of vertical devices, including a need for etching of deep trenches without incurring sidewall damage. One of the potential ways to do this is by using metal-assisted chemical etching (MAC), which is a metal-catalyzed and local (open-circuit) electrochemical etching method capable of producing semiconductor structures defined by a patterned metal film in a forward (etching below the metal) or inverse (etching outside the metal) process. By etching pillars through GaN epitaxial layers into the native substrate, it was found that increasing the Si-doping levels to produce n-type conductivity in the MOCVD epitaxial layers increases the etch rate and produces smoother etch surfaces. However, the substrates showed a different etch morphology and accelerated etch rate. This is partially thought to be due to the high Si concentration at the GaN/GaN regrowth interface. Etching in this manner achieved etch rates similar to RIE etching, but without non-radiative sidewall damage. More details on this work are published in [29].

#### 3.5.4 Resonant Tunnel Diodes

In addition to the Schottky and *p-i-n* diodes investigated with MOCVD, to assess the homoepitaxial growth of structures grown via MBE, resonant tunneling diodes (RTDs) have been grown homoepitaxially on native substrates for comparison to those grown heteroepitaxially on sapphire substrates. The electrical

properties of these RTDs are sensitive to the abruptness of the interfaces between the barrier layers and the quantum well, as well as the uniformity of the layer thicknesses, and hence are useful indicators of material quality. These efforts have been successful, resulting in the first demonstration in the III-nitride material system of repeatable, stable, hysteresis-free negative differential resistance (NDR) at room temperature, as well as possessing extremely high current density and near-UV cross-gap light emission. While repeatable, room-temperature NDR was first observed in III-N RTDs grown homoepitaxially on low dislocation-density native GaN substrates, the results from this program show homoepitaxial and heteroepitaxial RTDs to possess NDR, but the homoepitaxial structures have a better peak-to-valley current ratio. Experiments with growth temperature showed similar trends for both homoepitaxial and heteroepitaxial structures, where higher growth temperatures had higher peak current density, but lower temperature growth had better yield and smoother surfaces. A two-step growth process was investigated along with in-situ surface preparation to increase the current density, which resulted in a record high peak current density of 1 MA/cm<sup>2</sup> and a peak-to-valley current ratio greater than 2. Additionally, 90% of the devices using this process exhibited stable NDR at room temperature. Further details of this work can be found in [30-33].

#### 4. SUMMARY

This program focused on understanding the fundamental issues involved in homoepitaxial growth of III-nitride semiconductors with the goal of enabling applications in the fields of high power and rf electronics. The program showed the importance of incoming characteristics of the GaN wafers – with roughness, structural defects, degree of offcut, and inhomogeneity impacting homoepitaxial growth and electrical performance in *p-i-n* and Schottky diodes. Additionally, the utility of long-range characterization of incoming substrates and epitaxy was highlighted and used to first set metrics and then predict electrical performance. The regrowth interface was shown to be compositionally clean in MOCVD growth, except for high levels of Si at the interface. However, this Si did not impact thermal conductivity of the boundary or epitaxial layers at room temperature. Impurities in the nitrides were described in a tutorial on GaN and the optical changes in highly C-doped GaN were explained. Further theoretical work on ultra-wide bandgap nitrides found that holes in AlN will be easily localized reducing the potential for p-type conductivity. Investigations in c-BN found two potential n-type dopants. MAC etching showed a dependence of etch rate on the conductivity and type of material (substrate vs. epitaxial layers), but still shows potential in producing deep etching without causing non-radiative defects, which are observed with more conventional plasma-based processes. Finally, in examining MBE-grown RTDs, high performing devices were produced on homoepitaxial structures using optimized surface cleaning and a 2-step growth process. In general, the work in this program set a foundational base for forming vertical device technologies in our current GaN efforts as well as exploring aspects for ultra-wide bandgap nitride semiconductors.

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## 5.3 Patents

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