AFRL-RY-WP-TR-2022-0157

HIGHLY EFFICIENT WIDE-BAND POWER AMPLIFIERS DESIGN FOR MILLIMETER-WAVE DIGITAL ARRAYS (MIDAS)

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SEPTEMBER 2022
Final Report

AIR FORCE RESEARCH LABORATORY
SENSORS DIRECTORATE
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AIR FORCE MATERIEL COMMAND
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REPORT DOCUMENTATION PAGE

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1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED	
		START DATE	END DATE
September 2022	Final	1 November 2018	1 February 2022

4. TITLE AND SUBTITLE

HIGHLY EFFICIENT WIDE-BAND POWER AMPLIFIERS DESIGN FOR MILLIMETER-WAVE DIGITAL ARRAYS (MIDAS)

5a. CONTRACT NUMBER	5b. GRANT NUMBER	5c. PROGRAM ELEMENT NUMBER
FA8650-19-1-7902	N/A	62716E
5d. PROJECT NUMBER	**5e. TASK NUMBER**	**5f. WORK UNIT NUMBER**
N/A	N/A	Y1WV

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8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)		10. SPONSOR/MONITOR'S ACRONYM(S)	11. SPONSOR/MONITOR'SREPORT NUMBER(S)
Air Force Research Laboratory, Sensors Directorate Wright-Patterson Air Force Base, OH 45433-7320 Air Force Materiel Command, United States Air Forces	Defense Advanced Research Projects Agency (DARPA/MTO) 675 North Randolph Street Arlington, VA 22203	AFRL/RYDI	AFRL-RY-WP-TR-2022-0157

12. DISTRIBUTION/AVAILABILITY STATEMENT

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14. ABSTRACT

This is the final report of the Phase II of the DARPA MIDAS program from Prof. Donald Lie's team at Texas Tech University (TTU). Monolithic high-efficiency wideband millimeter-wave power amplifiers (mm-Wave PAs) can be critically important for realizing ultra-low-power, miniaturized mm-Wave digital arrays (MIDAS) systems, since these PAs can often consume about half of the overall system power budget. This work, therefore, performs fundamental research on the design of broadband 18 – 50 GHz mm-Wave PAs in several state-of-the-art semiconductor technologies for potential commercial and DoD (Department of Defense) applications. Specifically, we take advantages of the HRL's (Hughes Research Labs) 40 nm GaN T3 technology on SiC, GF's (GlobalFoundries) 90 nm SiGe BiCMOS (9HP) and GF's 22nm CMOS-FD (fully-depleted) SOI processes (22FDX), together with novel IC design techniques, to realize highly-efficient broadband mm-Wave PAs. We will investigate the design of broadband mm-Wave PAs in the medium output power range of ~ < 20 dBm, with very broad BW of ~ 20-30 GHz, excellent broadband peak PAE > ~20 - 45 %, and also good linearity. This comprehensive final report on broadband highly-efficient and linear mm-Wave PA design consists of six chapters, 131 figures, and over two hundred pages.

15. SUBJECT TERMS

millimeter-wave power amplifiers, miniaturized mm-wave digital arrays

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES
a. REPORT	b. ABSTRACT	C. THIS PAGE		
Unclassified	Unclassified	Unclassified	SAR	178

19a. NAME OF RESPONSIBLE PERSON	19b. PHONE NUMBER *(Include area code)*
Aji Mattamana	(937) 713-8893

PREVIOUS EDITION IS OBSOLETE.

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1 SUMMARY

This is the final report of the Phase II of the DARPA MIDAS program from Prof. Donald Lie's team at Texas Tech University (TTU). Monolithic high-efficiency wideband millimeter-wave power amplifiers (mm-Wave PAs) can be critically important for realizing ultra-low-power, miniaturized mm-Wave digital arrays (MIDAS) systems, since these PAs can often consume about half of the overall system power budget. This work, therefore, performs fundamental research on the design of broadband 18 – 50 GHz mm-Wave PAs in several state-of-the-art semiconductor technologies for potential commercial and DoD (Department of Defense) applications. Specifically, this workthis work takes advantages of the HRL's (Hughes Research Labs) 40 nm GaN T3 technology on SiC, GF's (GlobalFoundries) 90 nm SiGe BiCMOS (9HP) and GF's 22nm CMOS-FD (fully-depleted) SOI processes (22FDX), together with novel IC design techniques, to realize highly-efficient broadband mm-Wave PAs. This workThis work will investigate the design of broadband mm-Wave PAs in the medium output power range of ~ < 20 dBm, with very broad BW of ~ 20-30 GHz, excellent broadband peak PAE > ~20 - 45 %, and also good linearity. This comprehensive final report on broadband highly-efficient and linear mm-Wave PA design consists of five chapters, 131 figures, and over two hundred pages.

2 INTRODUCTION

2.1 Overview and Motivation

Monolithic high-efficiency wideband millimeter-wave power amplifiers (mm-Wave PAs) are critically important for realizing 5G and ultra-low-power, miniaturized mm-Wave digital arrays (MIDAS) systems, as these PAs can often consume about half of the overall system power budget [1,2]. Designing narrow-band 50 GHz mm-Wave PAs with peak power-added-efficiency (PAE) targeting above 35% is already challenging, but it becomes very difficult to design mm-Wave PAs with 35%-45% PAE across the entire 18-50 GHz operation range, not to mention to further maintain excellent PAE at power back off to support high peak-to-average-power-ratio (PAPR) signals. Therefore, wideband high-efficiency mm-Wave PA design is a mission critical area to enable miniaturized and efficient MIDAS systems, where fundamental research on innovative circuits and devices design must be conducted to create breakthroughs. This workThe TTU team thus proposes to take advantage of several most advanced device technologies, specifically the HRL's (Hughes Research Labs) 40 nm GaN on SiC, GF's (GlobalFoundries) 90 nm SiGe BiCMOS (9HP) and GF's 22nm CMOS-FD (fully-depleted) SOI processes (22FDX), together with novel IC design techniques, to realize highly-efficient MIDAS PAs. For applications where POUT needs to be above ~ 3 to 10 Watts at 15 GHz and above, Ref. [2] indicates that state-of-the-art silicon PAs still have difficulties competing with their III-V counterparts. Note most reported GaN PAs were for high-power defense or aerospace applications, but this week will specifically examine broadband GaN PAs for MIDAS applications at low POUT < 1W here (i.e., POUT >16.5 dBm) for the MIDAS work.

5G (5th Generation) eMBB (enhanced Mobile Broadband) applications achieve 10+ Gb/s download speed and x100 more wireless connected devices compared to 4G with sub-1 mS latency time for UR/LL (ultra-reliable, low-latency) for mMTC (massive machine type communication). As shown in the timeline given by 3GPP (Figure 2.1), the initial release of these specifications for the new radio specifications for 5G was in 2017, and the next two years focused on trying to achieve these specifications for the release of the Phase 1 5G system in 2019. The first step was to bridge from 4G LTE (Long Term Evolution) to 5G, which was enabled by integrating 5G into previous LTE networks, (i.e., Non-Stand-Alone 5G radio) as a steppingstone before a standalone version was released. Towards the completion of Release 15, researchers began to look towards Release 16 or 5G Phase 2, which included radio enhancements such as NR (new radio) access to an unlicensed band, Industrial Internet-of-things (IoT), Vehicle-to-Everything (V2X) applications, eURLLC (enhanced UR/LL communication), 5G satellite access, network slicing, Integrated Access and Backhaul (IAB), power-saving features and time sensitive networking (TSN) [1]. While finalizing Release 16, Release 17 has been worked upon, which focuses on NR MIMO (multiple input multiple output), systems moving up to the 52.6 GHz - 71 GHz BW, enhancing previous works such as Industrial IoT and eURLLC, NR positioning and coverage [1]. Thus, there has been strong efforts focus on moving up the operating frequency from the sub-6 GHz FR1 band to the millimeter-wave (mm-Wave) 5G FR2 band and beyond. The FR2 band of 24.25 GHz to 52.6 GHz is ~ 4 – 75x higher in frequency compared to the FR1 band and thus the power-added efficiency (PAE) of a power amplifier (PA) will be considerably lower due to higher effect of passive parasitics as well as

lower fMAX and/or switching speeds of devices. The PA is known to be the most power-hungry component in front-end modules (FEM), which makes the mm-Wave PA a critical barrier to overcome for achieving low-power portable mm-Wave 5G electronics [2]. Figure 2.2 (a) shows a simplified block diagram for a 4G/LTE transceiver, which shows that there are two paths, one for receiving (RX) and transmitting (TX) and one antenna as RX and TX are done with duplexing. Note this Figure 2.2(a) only shows a sub-6G full-duplex 4G LTE transceiver IC without the integration of the RF FEM, which contains the PAs, switches, filters, control logics, etc., and thus the FEM cannot be integrated into a single-chip with the silicon transceiver [3]. Some recent works have tried to integrate the 4G LTE transceiver IC with sub-6 GHz 5G functions to create a simpler, one chip solution for the sub-6 GHz transceiver only, such as in Figure 2.2(b) [4]. However, when migrating to the mm-Wave 5G NR standard, the frequencies and path loss is considerably higher so it would be necessary to use more complicated mm-Wave phased array systems with multiple input multiple output (MIMO) to achieve 3-D beamsteering, and thus the RF FEM for mm-Wave 5G becomes considerably more complex (Figure 2.2 (b), (c)), as suggested in 3GPP 5G Release 16 and Release 17 focused efforts. This mm-Wave 5G FEM requires many circuits and components in a small area, which means inefficient PAs with low PAE will create heat and reliability issues. In addition, ongoing works on broadband electronics attempt to simplify system complexity and reducing cost by having the circuits/filters covering a larger frequency range within the entire FR2 band (from 24.25 GHz – 52.6 GHz). Designing broadband mm-Wave FEM that can cover a major portion of these frequencies could be an attractive solution to reduce the number of components and thus reducing size and cost. For instance, the iPhone 12, Samsung Galaxy Note 20 and Google Pixel 5 only cover the n260 (37 – 40 GHz) and n261 (27.5 – 28.25 GHz) bands within the mm-Wave 5G FR2 band. The iPhone 12 uses one state-of-the-art FEM module for this and thus if the additional bands n257 (26.5 – 29.5 GHz), n258 (24.25– 27.5 GHz) and n259 (39.5 – 43.5 GHz) need to be accessed, additional components would most likely need to be added. Note even though this justifies and underscores the importance on the research for very broadband high-efficiency mm-Wave PA design, there are other strict limitations and products specifications in commercial applications that would prevent these very broadband mm-Wave electronics incorporated into real 5G handsets, such as the bandwidth, size and performance limitations of the available wideband antennas in handsets, and the noise/inference considerations. However, these very broadband high-efficient mm-Wave PAs might be instrumental for certain DoD applications, such as on EW (electronic warfare) and future wideband phased array systems.

Although this report work focuses on PA design in the current mm-Wave FR2 band, the similar design approach can be extended and is applicable for higher frequencies. In 5G user equipment (UE) and femto/picocells, since MIMO phased array is used, each of the PA's RF output power POUT will only need to be in the sub-Watt range. Thus, in this report, my work will focus on medium-power mm-Wave PAs design with POUT under the Watt-level, and the emphasis will be on very broadband performance with high PAE and good linearity.

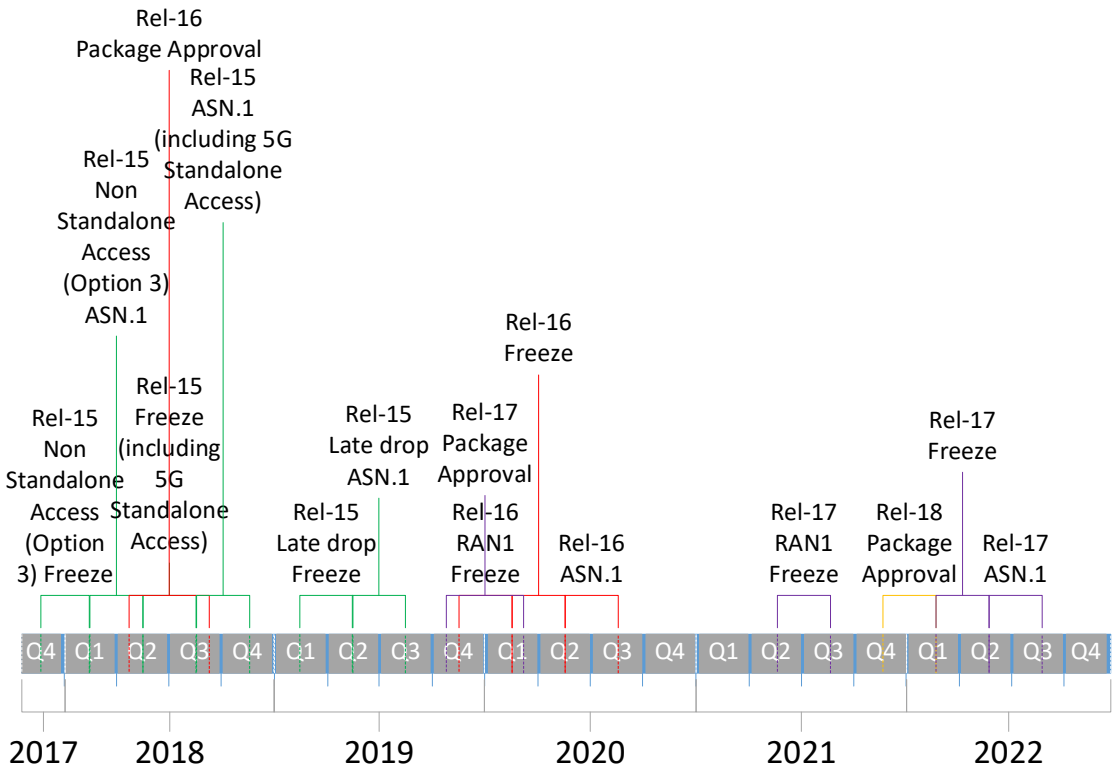


Figure 2.1: Estimated release schedules of various versions of 5G NR standards from 3GPP [1]

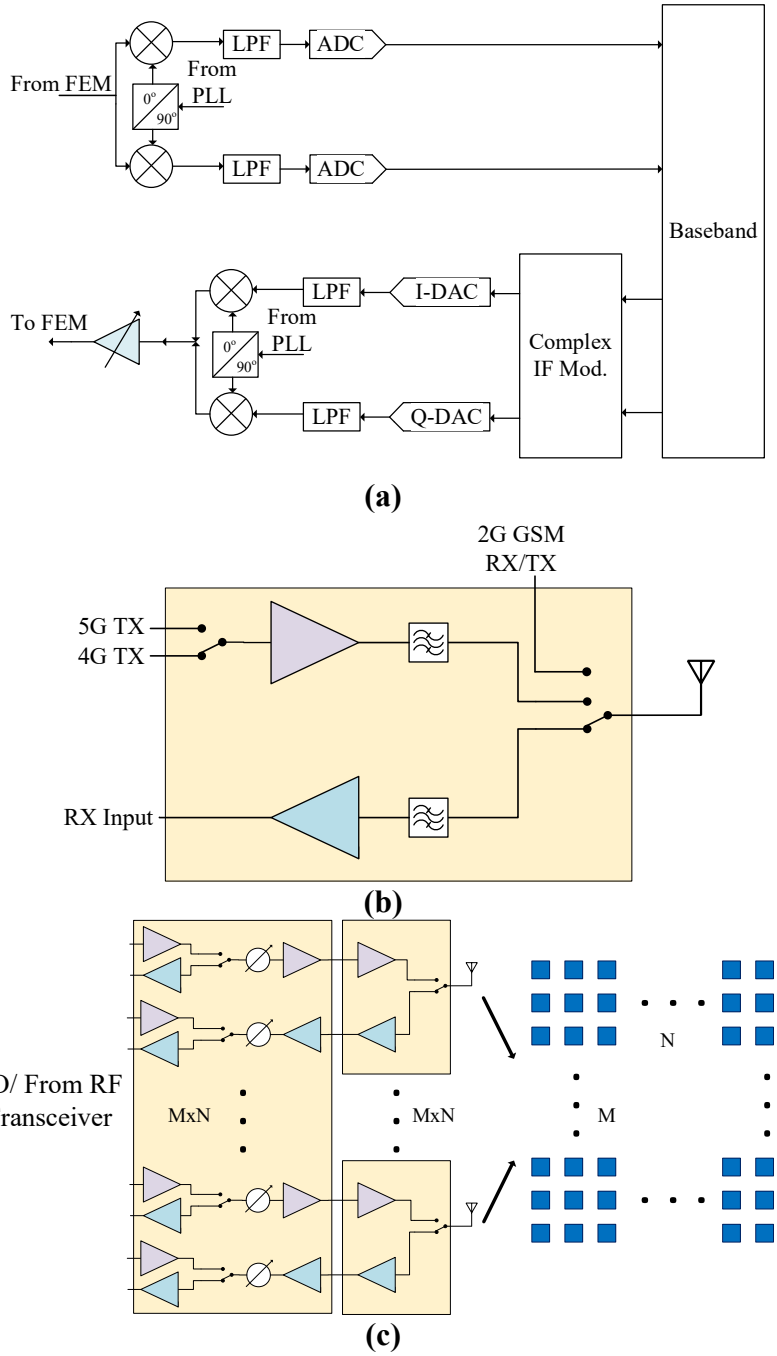


Figure 2.2: Simplified Block Diagrams of Examples

A 4G LTE RF transceiver IC [3] (a), (b) a highly simplified "ideal" version of a RF FEM that supports both 4G and sub-6 GHz 5G for a common frequency band [4] and (c) a FEM for mm-Wave 5G that uses MIMO phased arrays to achieve 3-D beamforming [5].

Output power, frequency performance, size, reliability/robustness and cost are important design metrics for monolithic RF PAs, and they may be inherently determined and/or limited by the semiconductor device technology used. For instance, even though a smaller technology node

may have a higher fT, it usually has a lower allowable output power POUT due to lower breakdown voltage and/or robustness. Thus, silicon designers especially must devise ways to work around these problems to provide power efficient and robust RF PA designs for high POUT. Silicon-based technologies, especially CMOS-SOI technologies, offer potentially higher integrability allowing for switches, LNA and PA to coexist on the same die, providing the possibility for a one-chip FEM IC solution for mm-Wave 5G and reducing the need for SiP (system-in-package), even though high-performance filters still cannot be integrated on-chip. On the other hand, III-V devices such as GaN and GaAs technologies have superior breakdown robustness with larger bandgaps and provide better fMAX > 200 - 400 GHz for higher PAE operations. Additionally, III-V technologies provide better high-Q on-chip passives due to the thicker process metals and semi-insulating substrates, which are crucial to achieving great power efficiencies and on chip EM structures (e.g., baluns). This work will look at several different state-of-the-art mm-Wave semiconductor technologies such as FD-SOI (fully-depleted silicon on insulator) CMOS, GaN. and SiGe processes to compare these advantages and disadvantages around broadband PAE, output power range and linearity for designing broadband mm-Wave medium-power PAs.

2.1.1 Device Basics

Figure 2.3 shows a highly simplified illustration of the energy band diagram for an isolated semiconductor with an external electric field (ε) is applied, which consists of a valence band, a conduction band and a bandgap energy (E_g), which is the amount of energy it takes for an electron to move from the valence band to the conduction band. To provide more physical insights, the bandgap energy E_g is the minimum energy required to break a covalent bond and thus generate an electron-hole pair in the semiconductor. This bandgap energy can play a big role in many aspects of semiconductor devices characteristics such as breakdown, f_T /f_{MAXx}, power handling capabilities and power efficiency. This work aims to investigate several different types of silicon-based single-crystal and also III-V based compound semiconductor technologies with different bandgap values and carrier mobilities with different transistor types for potential very broadband mm-Wave 5G medium-power PAs applications.

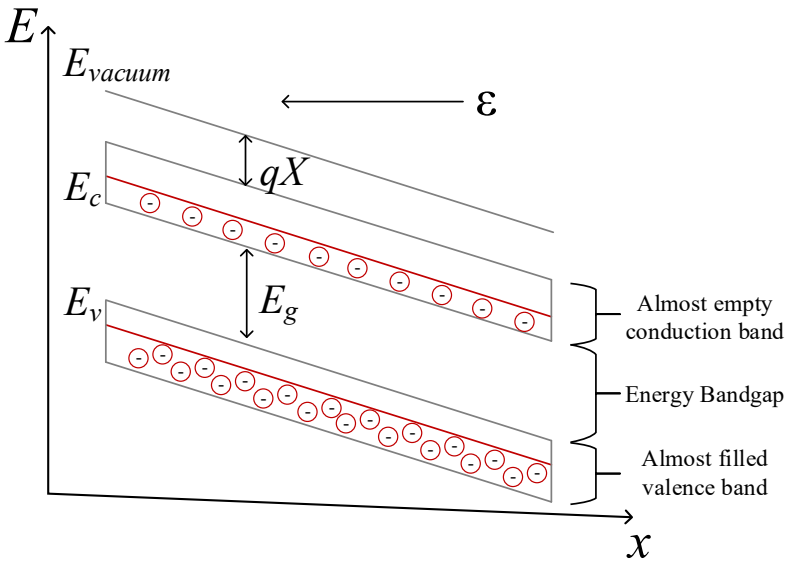


Figure 2.3: Basic and Highly-simplified Illustration of an Energy Band Diagram of a Semiconductor

As it is well-known, *p*-type and *n*-type regions are formed by doping semiconductors using acceptors or donors, respectively. This adds more carriers into the semiconductors, allowing for the material to conduct under active biasing. However, since the mobility of the free carriers is a function of dopant concentrations due to impurity scattering, the channel doping profiles for a MOSFET (metal-oxide-semiconductor field-effect transistor) or a HEMT (high electron mobility transistor) need to be engineered carefully to optimize the device performance, especially for short-channel transistors [6-7].

As mentioned before the energy bandgap of a semiconductor can play a big role in device breakdown characteristics, and in PA design where higher P_{OUT} is desired, this generally makes higher bandgap semiconductors more attractive. One way that a device can breakdown is by impact ionization which can then cause avalanche breakdown. This occurs in a reverse biased PN junction, such as the base-collector junction in a BJT (bipolar junction transistor). When a large reverse-bias voltage is applied in a P-N junction, which induces a high electric field $\mathcal{E}$, it can give carriers enough kinetic energy to break the covalent bonds and accelerate them to knock off more electrons and set off a chain reaction to create more and more electron-hole pairs like an avalanche (see Figure 2.4), causing current to rise and to be uncontrolled. When the bandgap of a semiconductor material is higher, it requires more energy from the electrons to be able to break the covalent bonds and generate the electron–hole pairs, and thus can sustain a larger signal voltage before going into avalanche breakdown [8]. However, since for our targeted mm-Wave applications, the broadband medium power PA P_{OUT} requirement is below Watt-level, it is unclear how much advantages these high-speed devices made in compound semiconductors (intrinsically of higher E_g) will have over those designed in advanced silicon technologies. Compound semiconductor devices would usually provide higher carrier mobilities and better low-loss on-chip passives than their silicon counterparts but are generally

considerably more expensive and difficult to integrate monolithically with the digital logics, memory and analog circuits that are typically designed in silicon. Therefore, this work will study and design these very broadband medium-power mm-Wave PA in various semiconductor technologies to shed some insights on these interesting technological considerations.

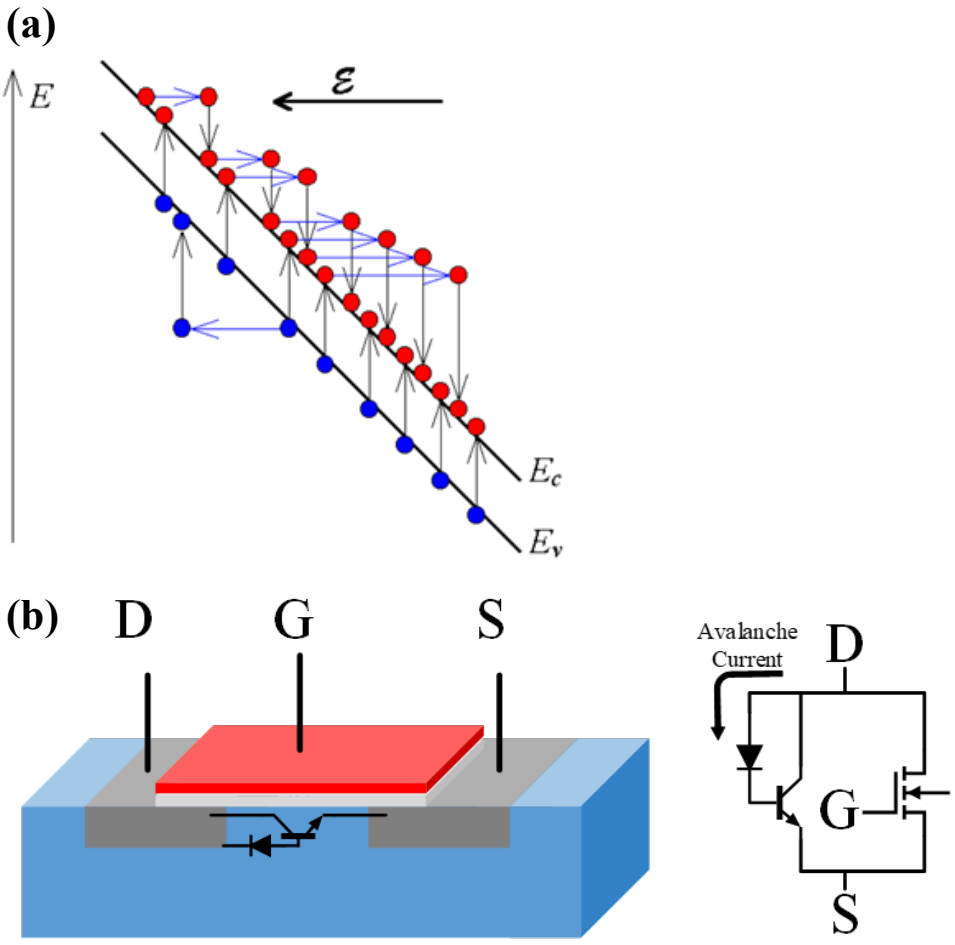


Figure 2.4: Basic Energy Band Diagram of a Semiconductor to Illustrate the Chain Reaction of Electron-hole Pairs Generation Under a High External Electric Field ℰ that is causing an Avalanche Breakdown (a); and (b) a Simplified Diagram of the Avalanche Breakdown in a n-MOSFET, where the Avalanche Current Flows through the Base-Collector Junction of the Parasitics npn BJT [8]

2.1.2 Advanced Millimeter-Wave Semiconductor Devices Used in this Work

Throughout this report several different advanced mm-Wave semiconductor technologies in both silicon and compound semiconductors will be discussed and compared. In addition to the different materials used, different types of transistors will be used in this work as well, such as CMOS FD-SOI MOSFET, SiGe HBT (heterojunction bipolar transistor) and GaN HEMT

devices, etc. The next sections will talk about the specific technologies/devices used in this work.

2.1.2.1 22 nm FD-SOI Process

Figure 2.5 illustrates a highly-simplified cross section of two bulk N-MOSFETs (metal-oxide-semiconductor field-effect transistor) and two N-MOSFETs on SOI stacked in series. In an n-type MOSFET, it is typically formed on a p-substrate/p-well, where the source and the drain junctions are heavily doped in n-type and then silicided for contacts to provide S/D terminals for biasing. An insulator of excellent quality is formed as the gate dielectric (mostly in SiO2 or oxynitride), where traditionally a polysilicon layer is deposited and etched and silicided above the gate oxide to form the small active region and thus the gate region. Figure 2.5 illustrates the S/D to body junction and its associated capacitance exists in a typical MOSFET, but it is reduced in the SOI devices with the oxide formation, especially if the body node is made floating (i.e., open). This work this workwill be using GlobalFoundries' (GF) state-of-the-art 22FDX technology, which is a 22 nm CMOS FD-SOI technology. The simplified cross section of the mm-Wave FD-SOI FET device, which is given in GF's technology brief [9], is shown in Figure 2.6. A salient feature of this high-speed device is that an ultra-thin buried oxide insulator is placed on top of the epi-silicon, rendering a fully depleted channel which reduces leakage from the channel into the body. This technology also allows access to body biasing through a back bias ring (see Figure 2.6) that can change the FET's threshold voltage (VT). It has been established that this technology has the distinguished advantage for low-power and highly integrated digital IC design where one can use software controlled transistor body-biasing to dynamically tune VT for both power and performance [10]. This can be done on digital circuits where high VT devices reduces the leakage current Ioff to reduce power consumption, and low VT devices to enhance the speed performance. This technology also provides high fT and fMAX transistors with the miminized junction capacitance to enable mm-Wave applications, and boasts lower device mismatches than other mm-Wave bulk CMOS technologies with comparable fT and fMAX performance as they mostly require smaller channel length (e.g., 16 nm FinFET) [10], and thus 22 nm FD-SOI may help to achieve better broadband CMOS differential PA performance as will be discussed in subsequent chapters.

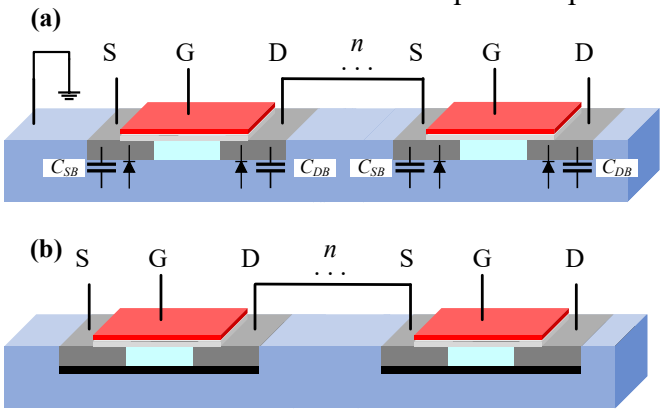


Figure 2.5: Highly Simplified Cross Section of 2 MOSFETs Connected in Series
Bulk N-MOS devices (a) and (b) thin-film N-MOS SOI devices.

For high frequency applications, junction parasitic capacitances, such as source to body (C_{SB}) and drain to body (C_{DB}) capacitances, can degrade the f_T /f_{MAX} of a device, and it can be reduced by adding an insulating layer below the epi-silicon to form an SOI device. This work uses the GF 22 nm FD-SOI device where the channel is fully-depleted to reduce junction leakage and with reasonable kink currents compared to partially-depleted devices [11]. In addition, having a CMOS SOI device with its body node floating can have an important advantage for RF/mm-Wave or analog amplifier design, as this allows stacking/cascode MOSFETs without increasing the body voltages that could otherwise limit the output signal swing due to the body effect. To illustrate this body effect a little more, let's go back to Figure 2.5 where for the case of n = 2, it shows the cross section of stacked bulk CMOS devices, with the intrinsic body diodes connected to the sources and drains. In a stacked amplifier as connection shown in Figure 2.5 (n = 2), the drain to bulk voltage of the top device becomes *x2* times of that of the bottom device since the body is connected to ground, and thus this can become a limiting factor in stacked designs that use bulk CMOS. However, CMOS SOI devices get rid of this intrinsic diode and thus does not experience this limiting factor by the body diode, and the maximum output swing instead would likely be higher than the case of stacked FETs in bulk CMOS, but still limited by the oxide breakdown/reliability voltage [12]. Stacked devices in 22FDX have floating body nodes electrically isolated so thus they do not experience leakage into the substrate and will not experience substrate breakdown [13]. Some research works have also reported that SOI MOSFETs with floating bodies achieve slightly better output power and efficiency on top of better reliability than grounding the body nodes, [14] and this is expected as the large signal output will not turn on the parasitic drain to body diode in transients for floating body SOI devices vs. the bulk CMOS devices.

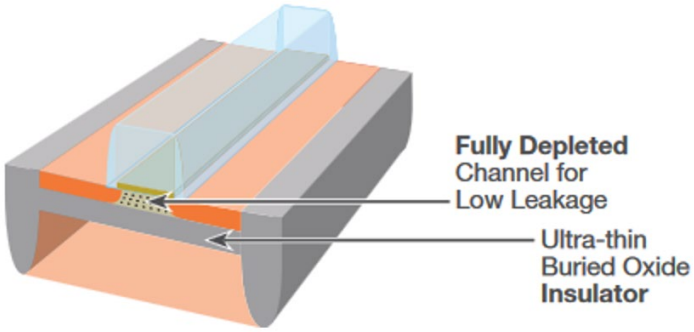


Figure 2.6: Cross Section of Fully Depleted Silicon-on-Oxide Device from GF's Technical Brief [9]

2.1.2.2 90 nm SiGe BiCMOS Process

For MOSFET devices in their saturation regions, electrons and holes conduct mainly by drift currents. However, in BJTs (bipolar junction transistor), the diffusion currents dominate. In this simplified case illustrating a npn device, two P-N junctions are formed with an *n*-type emitter added with a *p*-type base and then a *n*-type collector. The dynamic or ac response of a BJT device can be improved by using different semiconductor materials in the base such as in a SiGe HBT (Figure 2.7). The difference of the bandgaps between the semiconductors (in this case of

SiGe HBT, between Ge with an E_g = 0.66V and Si with an E_g = 2.12V) allows for the current gain to increase exponentially by using a SiGe base with the reduced E_g [15-17]. Additionally, by ramping the Ge profile in the thin base, one can also increase the carrier mobility with this additional E-field in the base to accelerate the carriers, reducing the base transit time and also allow us to dope the base region more to reduce the parasitic base resistance [18].Thus, the SiGe HBTs can have the advantages of having higher f_T and f_{MAX} at a given breakdown voltage than a regular BJT, effectively raising the Johnson's limit of the $BV_{CEO} \cdot f_T$ product [15-17]. This work will use GF's 9HP process, which is a 90 nm SiGe BiCMOS process and these devices achieve f_T of 310 GHz and f_{MAX} of 370 GHz and boasts 50% more integration density compared to GF's larger HBT technology nodes, as well as providing many integrated RF passives, and with optional thick metal thick layers. As SiGe HBTs have much better breakdown perfromance than the short-channel CMOS which suffers from oxide reliability and hot-carrier effects, this work will investigate our broadband mm-Wave PA designs in 90 nm SiGe HBT as well.

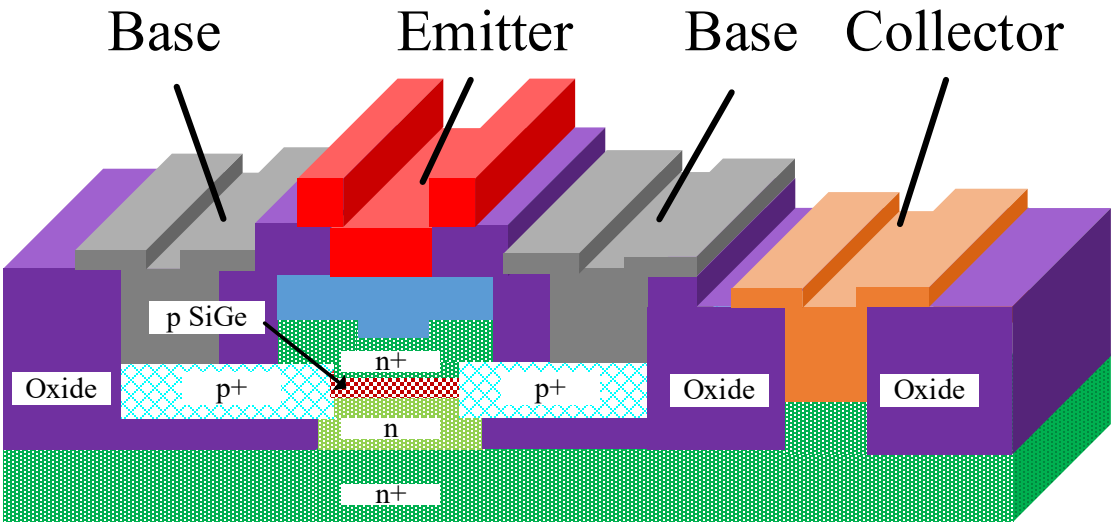


Figure 2.7: A simplified diagram of a SiGe HBT as shown in [18]

Ideally, when two dissimilar semiconductor materials are used to form a heterogeneous junction, their lattice constants would need to be matched perfectly to reduce crystal defects at and near the interface. Strained epilayer, or pseudomorphic growth of epitaxial layer on a lattice mismatch system such as SiGe on Si can be explored to make the epi-SiGe layer to have the matched lattice constant at the SiGe/Si interface, thus making the epi-SiGe elastically strained and elongated along the direction normal to the wafer to improve its carrier mobility and also keep the layer defect free (and hence the name "pseudomorphic" growth) [16-17]. Research has indicated that electron mobility can improve significantly by using these strained-layer pseudomorhic epi-SiGe layer on silicon [16-17]. Thus, pseudomorphic HEMTs (pHEMT) were also designed to take advantage of this strained-layer lattices, where the lattice mismatch is reconciled by making one of the materials very thin to be thermal dynamically stable so that the lattice of the epilayer stretches instead of forming defects, while the strained epilayer also can

improve the carrier mobility [15-17]. The SiGe HBT uses the pseudomorphic growth of the SiGe epilayer in the base, and also the ramping of the Ge content in the SiGe base.

2.1.2.3 40 nm T-Gate HEMT GaN Process

Figure 2.8 shows a simplified cross section of a GaN HEMT device. GaN is typically grown on a SiC substrate with a buffer layer, and this junction between GaN and AlGaN forms a 2DEG, or 2-dimensional electron gas due to the different energy levels of each material. Figure 2.8 also shows the simplified energy band diagram of a heterogenous junction, illustrating the triangular area where electrons are confined between the two materials, forming the 2DEG, where E_F is the Fermi energy level, or the hypothetical energy level where the highest electron orbital occupies (at 0° K). The Fermi level determines the probability of electron occupancy at different energy levels [19]. These 2DEG formed heterogeneous junctions have the benefits of high carrier mobility without additional doping and thus with reduced carrier scattering to enhance mobility. Usually, GaN layer is added below the AlGaN as a buffer due to lattice mismatches between the AlGaN and substrate [20]. All these layers are usually grown on top of either Si, SiC or sapphire to add thermal stability. Electrons flow very easily here, and the on-resistance R_{ON}, or the resistance of the channel when the device is on, is quite low for these devices. These devices are "normally on" devices due to the high mobility of the 2DEG and require a negative voltage to turn off the device. Adding a positive voltage to the drain before the gate is fully turned off can break the device (depending on the specific device technology), thus there have been efforts to make these "normally-on", also known as the depletion-mode (D-mode) devices into "normally-off", or enhancement-mode (E-mode) devices, similar to the vast majority of the CMOS devices today. It would also be advantageous to create E-mode devices for realizing digital logic circuitry [21].

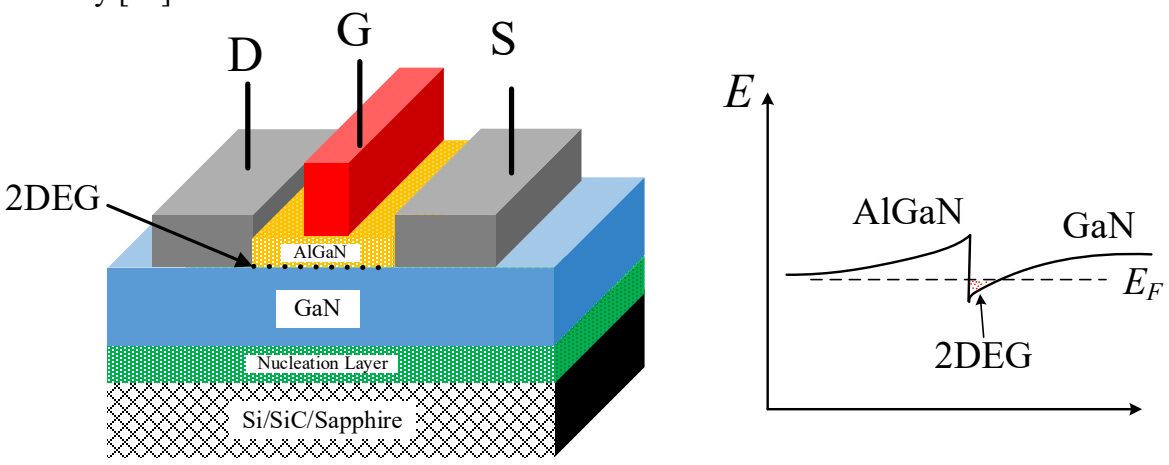


Figure 2.8: A simplified Cross Section of Typical GaN HEMT Device (a) and (b) Energy Diagram of Heterogenous Junction Showing 2DEG [22]

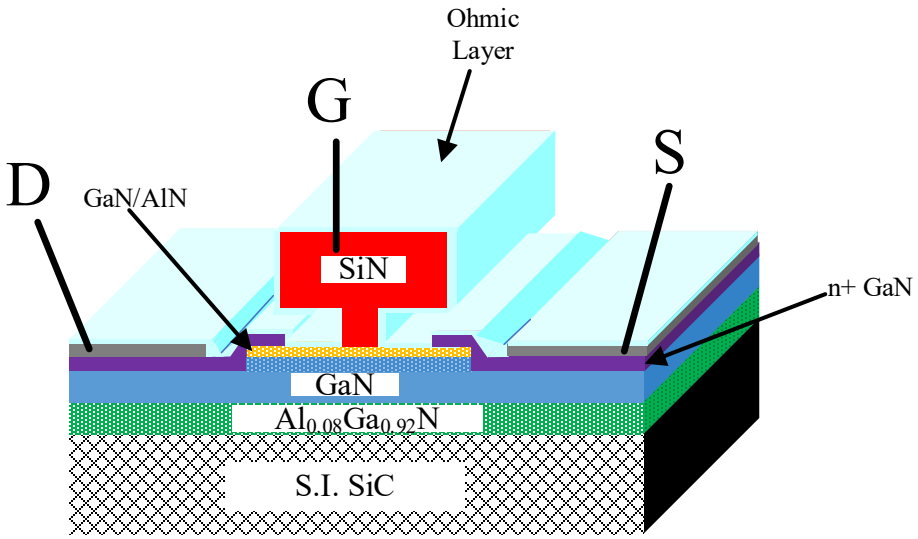


Figure 2.9: A Cross-section of a Fully-passivated 40 nm-gate AlN/GaN/AlGaN DH-HEMT by HRL, which is Rather Similar to the GaN Transistors used in this Work [23]

This work will utilize HRL Laboratories' advanced T3 40 nm GaN HEMT technology, similar to what is illustrated in Figure 2.9. This figure details a GaN technology that is slightly different than the T3 technology used in this work, as it is showing a DH-HEMT (dual heterogenous HEMT), and thus has two heterogenous junctions with the channel GaN epilayer sandwiched by the top GaN/AlN layer and the underlying $Al_{0.08}GaN_{0.92}$ layer. This DH-HEMT managed to maintain a high 2DEG density of 1.3×10^{13} cm^2 and a high mobility of 1200 $cm^2/V\cdot s$, as measured after surface passivation by SiN, and with a low gate leakage current. The $Al_{0.08}Ga_{0.92}N$ back barrier was used to increase carrier confinement and suppressing the short channel effect [23]. Similar to what is shown in Figure 2.9, the T3 40 nm GaN/SiC process used in this work is a process that uses a T-gate structure, which has the benefits of improving contact resistance by increasing the gate area contact while maintaining small gate length and thus improves on-resistance while minimizing degradation of f_T and f_{MAX}. This technology achieves a knee voltage of ~2 V, I_{DMAX} of 1.6 A/mm, V_{BR} of 50 V, f_T of 220 GHz and f_{MAX} of 400 GHz [24]. This technology supports drain operation up to 12 V and can operate at smaller supply voltages where PAE can be optimized at the sacrifice of lower RF P_{OUT} for mm-Wave PA applications where P_{OUT} per PA greater than Watt-level will not be needed due to phased array spatial power combining (e.g., small cells and handsets).

2.2 RF Amplifiers and 5G Communication Protocols

I will discuss some fundamental design aspects for RF/mm-Wave amplifier design next, and also cover some of the basics of the 5G communication standards next that has affected the broadband highly-efficient and linear mm-Wave PA design.

2.2.1 Basic Amplifier Classes

A well-known design trade-off in RF power amplifier design is on its linearity vs. power efficiency, and this work will see this theme repeated throughout this work. In this section, basic amplifier operation modes (classes) will be briefly discussed. A simplified schematic of a single stage, common source PA is shown in Figure 2.10. This schematic does not include a real matching network, just a DC block and a DC feed to bias the device. The conduction angle of a PA is typically used to classify the type of biasing for a particular PA [25-26]. Figure 2.11 shows a typical I-V curve of gate voltage versus drain current. When the bias goes below the threshold voltage V_T, the device "turns off" and does not conduct significant current as a PA (i.e., in the sub-V_T region). However, when the gate voltage is biased right at the V_T threshold voltage level, one can expect that the large-signal RF input driving into the gate can swing up and down the voltage at the gate, making the amplifier conduct according to the duty cycle of the input signal, and thus produces an output waveform with the same conduction duty cycle (or the "conduction angle" as the input). Therefore, depending on the gate DC bias voltage, this work have several classes of amplifiers that will have different conduction angles. For example, in a Class A PA, the gate bias is significantly above V_T, and thus the PA conducts all the time (i.e., 360^o conduction angle, always on) and its input-output characteristics can be rather linear before the output hits compression. However, its quiescent/DC bias current is inevitably higher, and thus the Class A PA is less power efficient. In an ideal Class B operation, the gate is biased exactly at V_T, and thus the PA conducts only during the positive cycle of the RF input signal and has a conduction angle of 180^o (for a sinusoidal input), and is consuming about half of the DC power vs. a Class A PA; however, because the PA is off half of the time, it is considerably less linear than the Class A. PA designers will often bias the commercial RF PA products in between these two classes (called Class AB), for a trade-off on linearity vs. power efficiency. Another class of PA operation is the Class C design, and this is when the PA is biased below V_T and thus conducts less than 180^o and therefore is even more efficient than Class B, but it is inevitably not linear. In 5G mm-Wave commercial systems, complicated modulation schemes and wideband waveforms with high peak-to-average-power-ratio (PAPR) may be used to achieve the high data rates 5G promises, which demands very good linearity to achieve low EVM (error-vector magnitude) for communications. A big challenge is that in 5G small cells, numerous PAs can be in phased array systems where many FEMs are contained in a small area, making low heat dissipation (and thus high PA power efficiency) very important. Thus, this choice of biasing and efficiency/linearity enhancement on a RF/mm-Wave PA design is definitely not trivial, and they have been a very hot research area for both commercial and DoD applications.

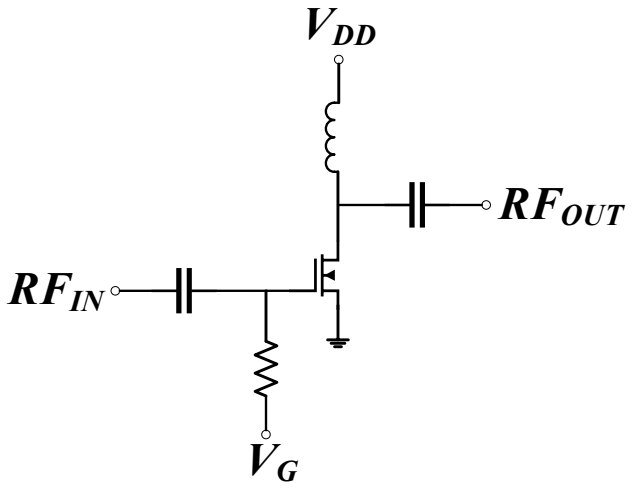


Figure 2.10: A Simplified Schematic of a Single Stage, Common Source PA

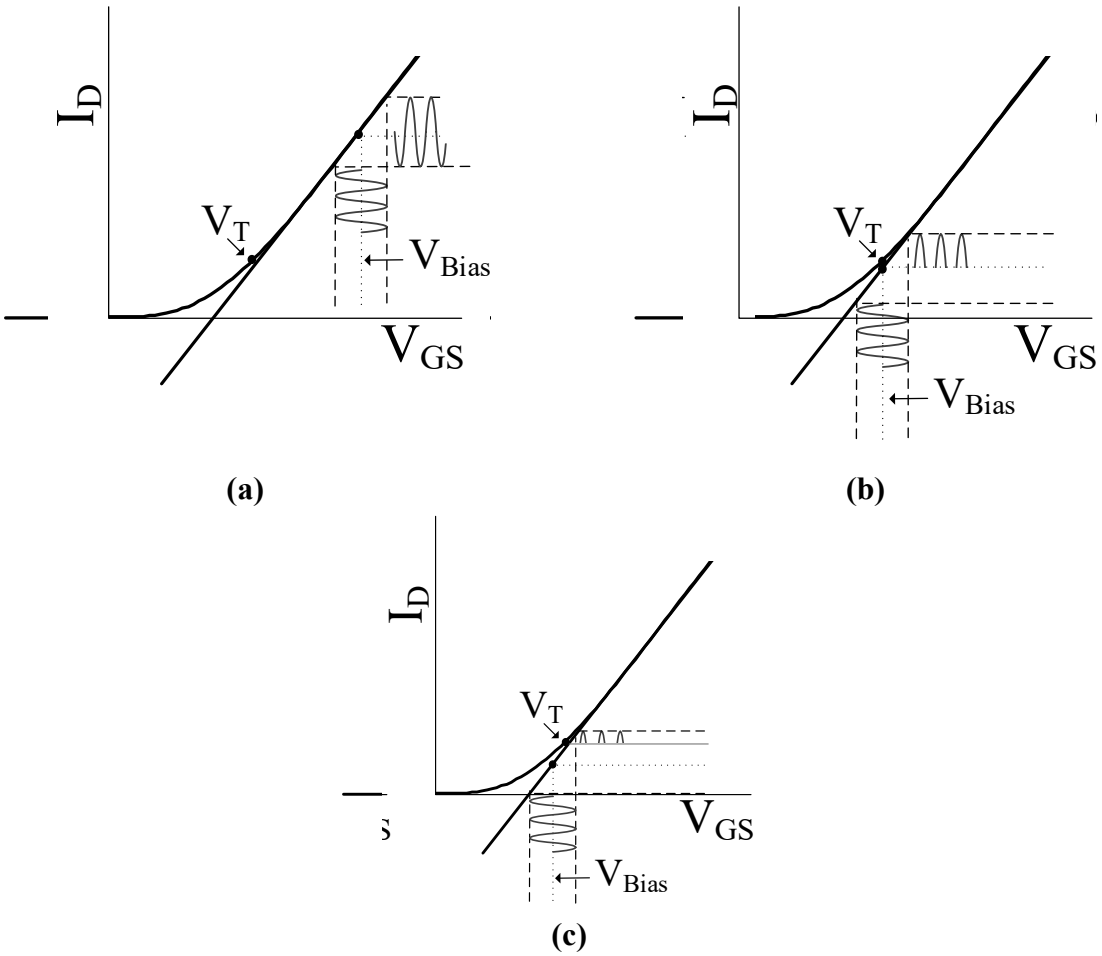


Figure 2.11: I-V Curve of the Ideal PA shown in Figure 2.10 with (a) Class A, (b) Class B and (c) Class C Biasing

2.2.2 Modulation Schemes

In the previous section, the basic bias choice and the trade-off of linearity vs. power efficiency for a RF PA design was briefly discussed, and the consequences of those choices becomes more apparent when inserting these PAs into mm-Wave systems that are being driven by complicated wideband signals with high PAPR that demand very high linearity. This work will thus briefly talk about some these modulation schemes next. Two of the simplest modulation types are frequency modulation (FM) and phase modulations (PM), where the frequency/phase is changed according to data/symbol that carries the information, and thus the modulated signal waveforms do *not* have any amplitude variation, relaxing the linearity requirement of the amplifying PAs. One can also use amplitude modulation (AM) to encode the data/symbol, which results in signal waveforms that contain significant amplitude variations, thus requiring high linearity amplifiers for signal amplification. Additionally, a signal can be modulated with a combination of two-phase modulation (or amplitude modulation) in the I/Q (in-phase/quadrature) domains. The signal is split into I (in-phase) and Q (quadrature) paths that are phase shifted by 90 degrees toward each other. This technique can be used in modulation schemes such as Gaussian minimum shift keying (GMSK, similar to FM with a Gaussian filter), quadrature phase shift keying (QPSK; PM, used in most satellite communications), and quadrature amplitude modulation (QAM), which is commonly used in 4G/5G signals to increase the data/symbol rates. The spectral efficiency of these modulation can be measured by the symbol rate, which is the ratio of the bit rate to number of bits in a symbol, or pulse in the data baseband. The simplest of these types of modulation schemes is BPSK (binary phase shift keying) which changes the phase of the carrier abruptly to two different phases corresponding to a 1 or 0. QPSK works by combining two orthogonal BPSK channels together. Combining two BPSKs allows the channel to carry two bits of data per symbol rather than just one like in BPSK. I and Q can carry an either a 1 or a 0 in BPSK and when combined to form QPSK, carry a 00, 01, 10 or 11. A constellation plot like in Figure 2.12 shows the data being portrayed at each symbol. Note for the QPSK modulation scheme, the subsequent amplifier would have to deal with transient non-linearity issues as data will be passing through the origin (00) point. To alleviate this problem, offset quadrature phase shift keying was created by having the odd-bit stream can be delayed by a half bit [27]. This produces a constellation diagram also shown in Figure 2.12 (b) as O-QPSK. Another form of O-QPSK is minimum-shift keying (MSK) modulation uses half period sinusoids to carry data rather than square waves. 1 and -1 are described in this method using higher and lower frequencies, respectively. To get even more spectral efficiency and a lower symbol rate, one can store more bits in the I and Q constellation diagram. For example, in 16 QAM, four values are held on each I and Q axes, giving 16 possible states and four bits per symbol, as shown in Figure 2.12 (c). This type of higher-order QAM modulation can be expanded to other 2^x forms such as 64, 128, 256, 512, 1024 QAM, etc., and many of these are allowed modulation as legitimate 5G waveforms (e.g., 256 QAM Downlink (DL) for 5G) [28]. As the modulation scheme becomes more complicated, the linearity becomes more important as this will lead to more signal leakage into adjacent channels (often characterized by the adjacent channel leakage ratio or ACLR) from the transmitter (TX) output, which has an allowable amount prescribed in the specific communication protocol. Many of these complex modulated signals used in commercial 3G/4G/5G communications have high PAPR of 7-14 dB, and thus PA needs to have high PAE at ***both*** peak output power, where efficiency is important, so this

work do not waste lots of power at peak output, and also at power back-off (say 10 dB back-off for 3G WCDMA) to achieve the best ***average*** PAE for handsets. Some techniques to address these PA design challenges will be discussed later, such as with Doherty PAs that usually do not work for broadband applications, etc.

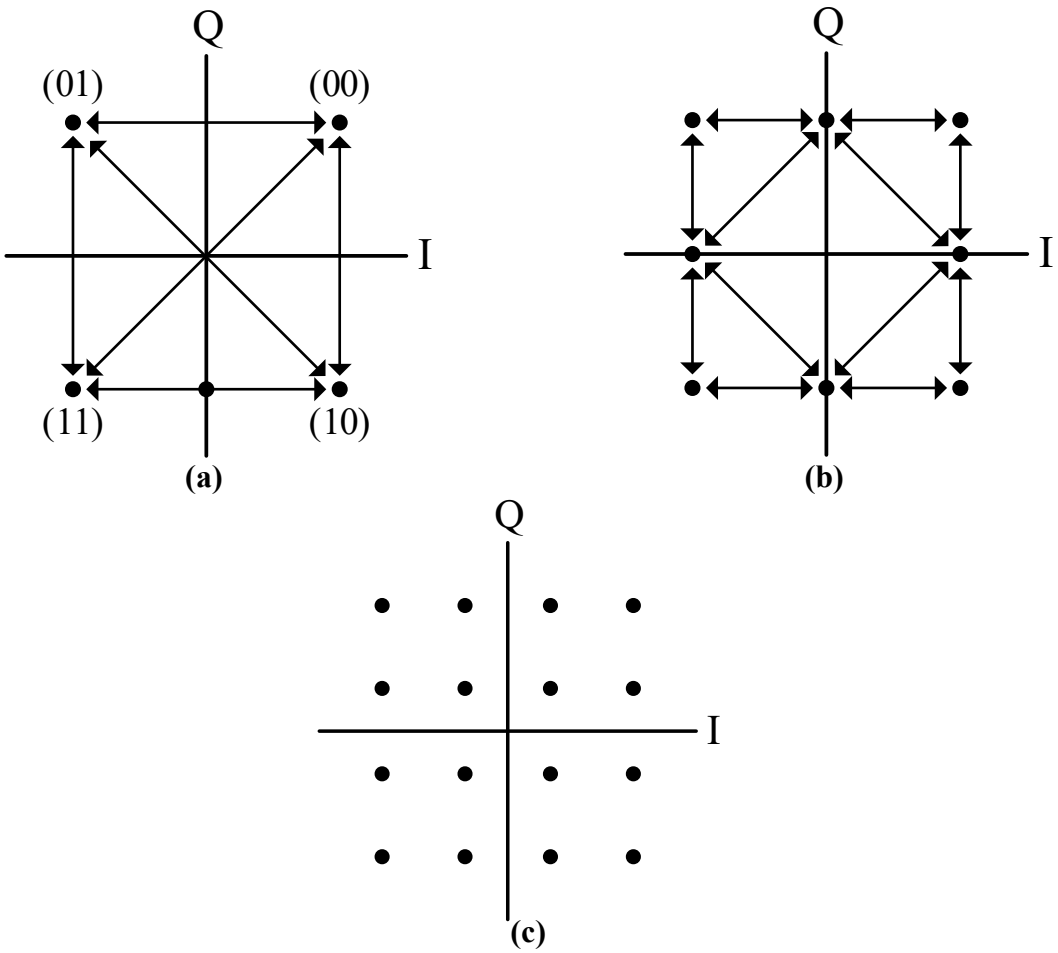


Figure 2.12: Constellation Diagram of (a) QPSK, (b)OPSK and (c)16-QAM [29]

Another example to make the modulated waveform more spatially efficient is to use the Orthogonal Frequency Division Multiplexing (OFDM), which is an efficient modulation format used in modern wireless communication systems including 5G. This technique uses bandlimited orthogonal subcarrier signals and combined them with ***significant overlap*** in the frequency domain while avoiding interchannel interference [30]. Note these subcarriers must be orthogonal functions (i.e., the integral of the subcarriers' products over the designated time interval should be zero). The wireless LAN (local area network) standard, IEEE 802.11a, was one of the first standards to employ OFDM. That standard uses 64 subcarriers each of 20 MHz bandwidth and spaced by 312 kHz, which can be modulated with several different QAM variations: BPSK, QPSK, 16QAM or 64QAM.

However, this success of OFDM should *not* be confused with what is shown in Figure 2.13, where multiple channels are added together without overlap to form a large BW single channel. In this case willthis work just connecting 9 different adjacent 100 MHz channels to form a 900 MHz signal, which is the broadest TX channel bandwidth above what is currently allowed in the 5G NR standard (for transmit signal, the 5G NR widest BW is currently at 400 MHz, which is expected to increase in the future). What is shown in Figure 2.13 is called carrier aggregation (CA), which can increase the signal BW considerably and thus causing difficult PA linearity challenges [31-32]. For 5G NR, the CA method to increase signal BW is also called as a component carriers (CC) scenario. For example, [31] shows a wideband 28 GHz PA supporting 8 × 100 MHz carrier aggregation for 5G NR in 40 nm CMOS. To test with 5G data-rates, 1-, 4-, and 8-component-carrier (CC) aggregation scenarios are measured, for 90 MHz-wide CCs and 10 MHz guard bands. A 5G-NR 28 GHz linear and efficient CMOS PA in 28 nm CMOS supporting wideband 64-QAM OFDM signals with non-contiguous 2CC x100 MHz scenarios is demonstrated in [32]. This work will use this most aggressive signal BW in Figure 2.13 to evaluate the linearity of some of our broadband mm-Wave PAs in the subsequent chapters.

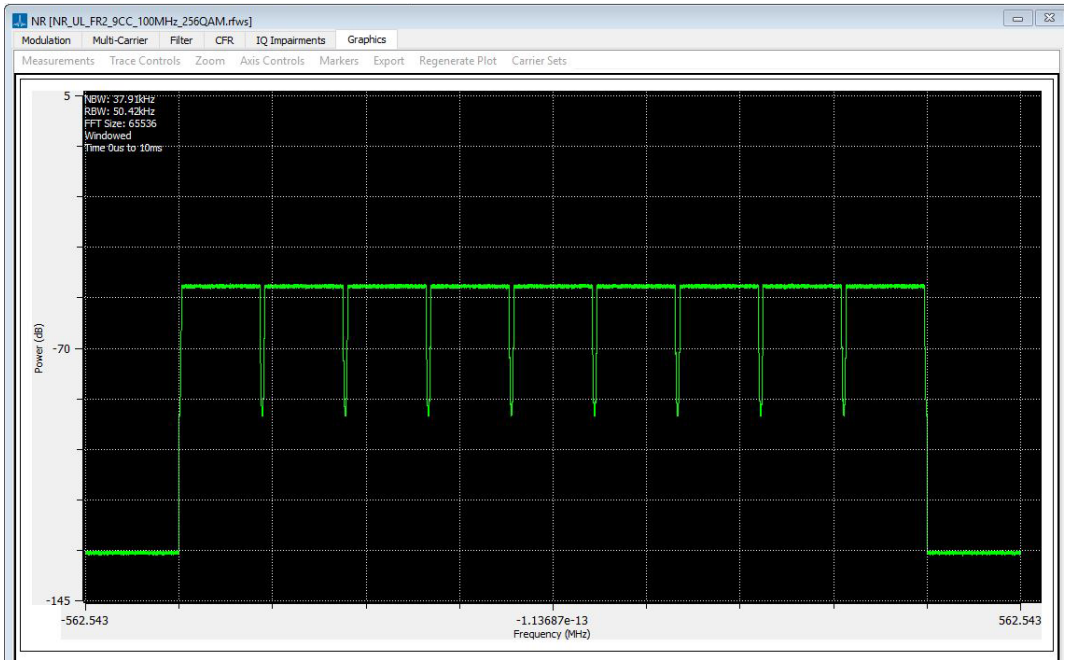


Figure 2.13: Baseband Signal of a 9 x 100 MHz Channel by Carrier Aggregation
i.e., 900 MHz signal BW

3 METHODS, ASSUMPTIONS AND PROCEDURES

3.1 METHODS

I will discuss some of the mm-Wave PA design techniques used in this work in the following sections and will describe some basic design principles to serve as introduction to the specific broadband mm-Wave medium-power PA designs to be presented in the following chapters.

3.2 NEUTRALIZATION CAPACITORS FOR GAIN ENHANCEMENT

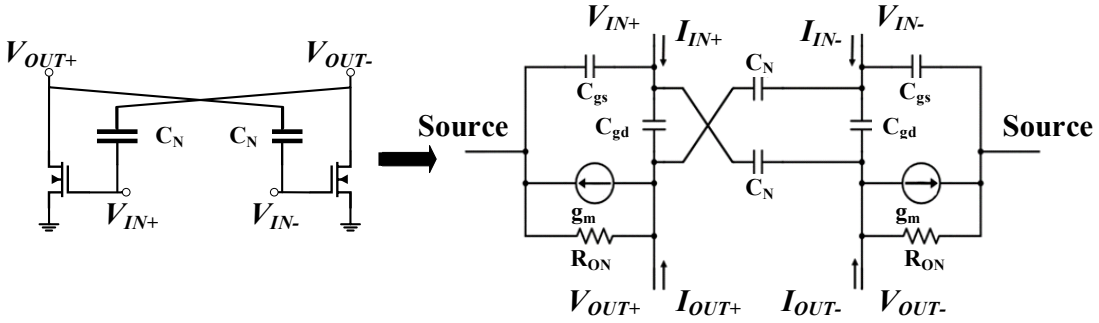


Figure 3.1: A Simplified Small-signal Equivalent Circuit Model of MOSFET Differential Cell with Neutralization Capacitors [35]

Due to the low power gain (f_{MAX}) for transistors' at mm-wave frequencies, gain enhancement may need to be utilized in order to achieve good performance for mm-Wave PA design. Differential operation has the benefit of less source degeneration from the parasitics to ground due to the symmetry at the virtual ground point connected to the common-source of the FETs in Figure 3.1 [33]. Thus, this technique can effectively reduce parasitics to ground that would otherwise considerably degrade the amplifier's gain at mm-Wave, especially if one is designing in process technologies that do not offer thru-wafer-vias (TWV) directly to ground from the chip ground [34], Neutralization capacitors can be added to a differential design to further improve the power gain and the PA's high frequency performance [35]. Figure 3.1 shows a simplified small-signal equivalent model of a MOSFET differential pair with neutralization capacitors, which are labeled with a value of "C_N" With this schematic, the Y-parameters from the differential 2 port (admittance parameters) can then be derived and are shown in (3.1) and (3.2) [35].

$$Y_{12} = \frac{I_{in\pm}}{V_{out\pm}}\Big|_{V_{in\pm}=0} = -j\omega(C_{gd} - C_N) \qquad (3.1)$$

$$Y_{21} = \frac{I_{out\pm}}{V_{in\pm}}\Big|_{V_{out\pm}=0} = g_m - j\omega(C_{gd} - C_N) \qquad (3.2)$$

Note Y_{21} is the differential pair circuit transconductance gain G_m, and Eq. (3.2) suggest G_m can be maximized to g_m by choosing C_{gd} equals to C_N. This work can now proceed to show the derived maximum stable gain G_A of the circuit [35]. Here Y_{21} and Y_{12} are inserted in the

maximum available power gain equation (3.3), and k is the stability factor [36]. When k is at least 1, and this work assume the other stability factor B is also greater than zero as it normally is, then the design is unconditionally stable, thus this work can set k to equal 1 to get the maximum stable power gain G_S here as shown in Eq. (3.4).

$$G_A = \frac{|Y_{21}|}{|Y_{12}|}\left(k - \sqrt{k^2 - 1}\right) \quad (3.3)$$

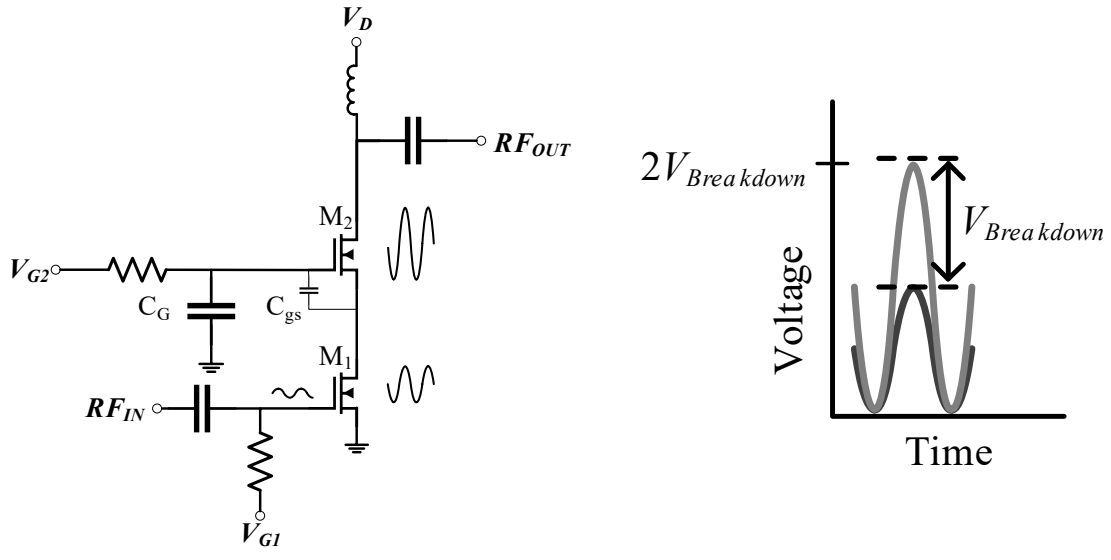
$$G_S = \frac{|Y_{21}|}{|Y_{12}|} = \sqrt{\frac{{g_m}^2}{\omega^2(C_{gd} - C_x)^2} + 1} \quad (3.4)$$

One can see in the denominator of Eq. (3.4), the Miller capacitance term C_{gd} is subtracted with the neutralization capacitance term C_N. Thus, the amount the maximum stable power gain degradation from the Miller capacitance C_{gd} can be reduced by the judicious choice of C_N. For mm-Wave frequencies, care must be taken when adding the interconnects from each transistor to the other transistor for connecting this shared neutralization capacitor since at these frequencies, as the added parasitic inductance from the interconnect will resonate some of the neutralization capacitance out. In addition, the interconnects could add additional coupling from the output of the device to the input, which can cause stability issues. Instead of using interconnects and lumped components, [35] designed a differential cell where the parasitic capacitance from the transistor signal lines is used for cross coupling. Although that particular layout technique is not used in our work due to our decision not to change the transistor's layouts from the PCells provided by the original foundry design kit, the basic design considerations from that work were adopted.

3.2.1 Stacked PAs for Power Enhancement

One drawback to silicon technologies is that the breakdown voltage is much lower than those of their GaAs and GaN counterparts. Moreover, to achieve satisfactory performance at higher frequencies, wthe technology nodes should decrease with reduced minimum channel length especially for higher f_{MAX}. As the technology node decreases, the operating voltage also decreases and more importantly the breakdown voltage will reduce further, degrading the maximum allowed output signal power level (i.e., Johnson's Limit [37]). Thus, there is a significant degradation of the available output power at mm-Wave frequencies. There are several ways to increase the output power such as using what this work has shown in the previous section with a differential pair with neuralization caps. Other methods include using parallel devices or larger devices to hopefully increase current for more power; performing power combining of parallel PAs; and/or using cascode topology to increase maximum output voltage for more power. However, larger devices have the drawbacks of lower f_T and f_{MAX} due to increased parasitic capacitance, and power combining relies on passive components that can be quite lossy in silicon technologies at mm-Wave frequencies that will degrade PAE. A cascode design can be further improved upon carefully calculated changes to achieve a stacked amplifier design to improve its performance [38-40]. Figure 3.1(a) shows a basic two stack amplifier configuration but with the ideal waveforms. Note that this stacked topology can be scaled up to

any number of devices in theory. Different from a cascode design, which consists of a common source device and a common gate device, a two-stacked topology ideally adds multiple transistors in series to improve its breakdown characteristics to deliver higher output power, gain and PAE. A capacitor C_G is carefully chosen and added to the gate of the stacked device so that a voltage divider is formed by the gate-to-source capacitance of the stacked FET $C_{gs,2}$ and C_G so its gate voltage becomes $V_{DS,1} \, x \, (C_G / (C_{gs,2} + C_G))$, and can be identical to the input voltage fed to the bottom CS gate voltage. Therefore, this gate voltage on the stacked FET can now swing along with its drain voltage $V_{D,2}$. This enables the gate to source voltage of the stacked device to operate in a safe region, which tends to be the breakdown limiting factor for cascode designs as the gate of the cascode device is at RF ground. The drain to source voltage V_{DS} of the stack device is thus made to be identical to the maximum V_{DS} allowed by the breakdown limit on the CS device, successfully doubling the maximum allowable output voltage at the output node to $2 \, x \, V_{DS,1}$. This can be shown in Figure 3.2(b), which illustrates an ideal two-stack waveform. The total swing at the output is 2 *x* that of a single device while the individual V_{DS} of each device remains within the breakdown voltage. Note that this stacked topology works best for narrowband PA design, as the voltage divider at the gate of the stacked FET works best for narrowband operation where $C_{gs,2}$ remains constant within that frequency range. However, since the optimal output impedance is effectively doubled vs. a CS FET, it can help to get the output matching closer to 50 Ω and become more suitable for broadband operation. Also, there is an optimum number of stacked devices as there is an increase in resistance R_{ON} on each device, and this work cannot ignore both the parasitic capacitance on the drain (drain to bulk cap C_{db} is problematic for bulk CMOS) and the Miller capacitance C_{gd} going through the stack for each device and this problem is exasperated at higher frequencies. The detailed analysis is out of the scope of this report as only two-stacks will be shown here, but please refer to reference [38-40] for more details.



(a) **(b)**

Figure 3.2: A Basic Two Stack FET Amplifier Design (a) and (b) Ideal Drain-to-source $V_{DS,1}$ and $V_{DS,2}$ Waveforms of Stacked Design

Another drawback of using silicon devices for mm-Wave PA design is that they tend to have low optimum impedances due to higher parasitics compared with III-V devices, which requires a larger impedance transformation ratio and thus PAE will be hurt using lossy on-chip passive components. Stacked power amplifier designs have the benefit of increasing the optimum load to $N\,x\,R$, where N is the number of stacked devices and R is the optimum load of a single device. This is due to the fact that the current I_D is the same in a single device or in a stacked design, but $V_{DS,N}$ increases by N times. Since the voltage is increased by N, then the R is also increased by that same amount. If this output impedance is close to 50 Ω, this work can achieve excellent output broadband performance at least in theory. However, as discussed briefly above, at higher frequencies this output impedance will be degraded due to the parasitics at the drain node, and the on resistance may be higher as well due to the choice of smaller devices to achieve high frequency operation.

To calculate the value of the capacitor on the gate of the nth stacked device ($C_{G,n}$) that includes the effect of the Miller capacitance, [39] derives the Equation (3.5) from the g_m of the nth device ($g_{m,n}$), the gate to source capacitance of the nth device ($C_{gs,n}$), the gate to drain capacitance of the nth device ($C_{gd,n}$) and R_{OPT}, where the optimum load impedance (Z_{OPT}) is assumed to be mostly real and is equal to $N\,x\,R_{OPT}$.

$$C_{G,n} = \frac{C_{gs,n} + C_{gd,n}(1 + g_{m,n}R_{OPT})}{(\mathrm{n}-1)g_{m,n}R_{OPT} - 1} \quad n = 2, 3 \ldots N \quad (3.5)$$

3.2.2 Class J PA for Efficiency Enhancement

The basic PA Classes description presented in Section 2.3.1 did not take into account any sort of parasitics from the device. The parasitic drain capacitances, such as the drain to source capacitance, C_{ds}, can change the waveform at the load considerably. Several other types of classes of PAs were designed to relieve performance degradation from classical results due to C_{ds} such as Class E, Class F and Class J. Class J operation is investigated in this work and the simplified schematic is shown in Figure 3.3 and is discussed in depth in [25, 41]. A Class J amplifier operates with a Class B or deep Class A/B biasing so that the current waveform is a half-wave rectified sine-wave with a phase shift, so that the current and voltage slightly overlap as such in Figure 3.4. Class J also requires wave shape forming, where the load is chosen such the fundamental and harmonics follow equations (3.6), (3.7) and (3.8). This deviates from the classical approach of harmonic shorts and instead at the 2nd harmonic adds a reactive termination. Since this work's goal is for more broadband operations, a Class J is chosen as it may have the benefit over Class E/Class F of being able to operate within its class for a larger range of frequencies.

$$Z_{f_0} = R_L + j * R_L \quad (3.6)$$

$$Z_{2f_0} = 0 - j * \frac{3}{8} * R_L \quad (3.7)$$

$$Z_{>2f_0} = 0 \quad (3.8)$$

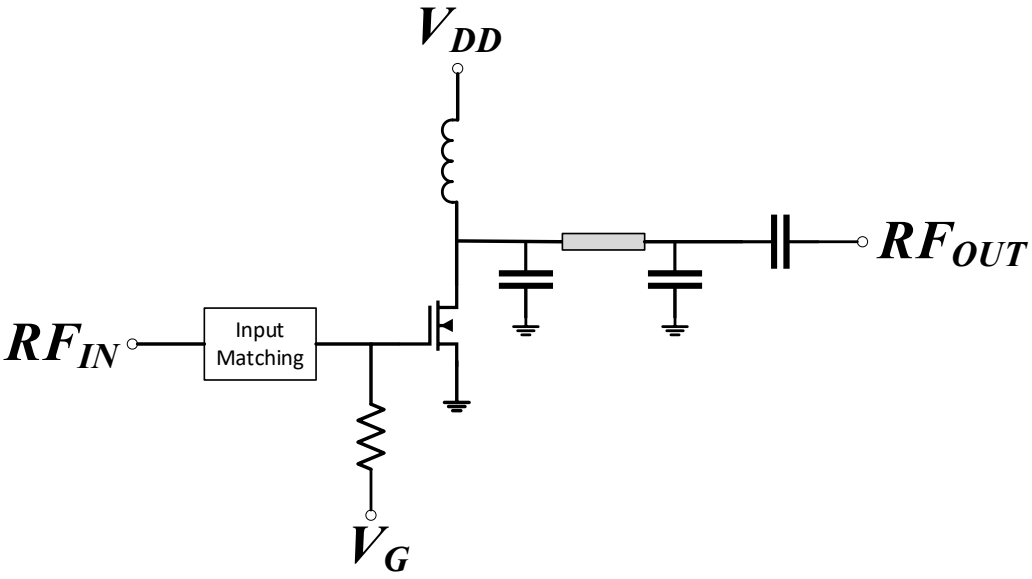


Figure 3.3: Simplified schematic of Class J PA

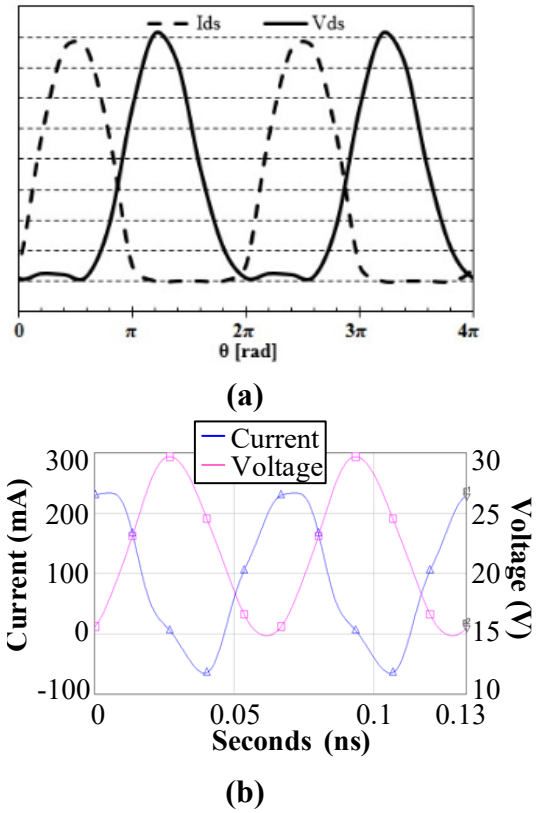


Figure 3.4: Ideal Waveform of Class J PA from [41] (a) and (b) Waveform from AFRL GaN Technology Class J PA Waveform

3.2.3 Some Methods For Broadband Amplifiers

As discussed so far, since the 5G FR2 band spans such a large frequency range from 24.25 to 52.6 GHz, and broadband PA design is an important fundamental research area that has its applications in various DoD and biomedical applications as well. It is advantageous to investigate designing highly efficient broadband PA to reduce the number of components in the RF FEM or to improve PA functionalities to cover this whole range instead of several parallel narrowband designs that are switched between. There are many methods to increase the BW such as adding feedback, increasing the order of the matching networks, using distributed amplifiers design [42-43] and also by asymmetrical power combining [44-45]. Some broadband PA design methods such as distributed amplifiers design were not studied in this work due to its larger die size and the lack of low-loss passives on silicon that would hurt its PAE, but the reader is encouraged to read about the details as it is a relatively mature research area [42-43]. It is well known that distributed amplifiers are fairly large due to the use of many inductors as well as lower output powers and thus may diminish the benefits of using a single broadband PA over more narrowband PAs.

3.2.3.1 Broadband Design Choice of Transistors and by Feedbacks

In any PA design, the choice for the power transistor is very important, and thus how the devices were chosen for broadband operation in this work will be discussed next in general. In this work, load pull simulations at the fundamental frequencies are done to find optimum loads for max. PAE and/or gain across frequencies, which ideally will be near 50 Ω to minimize the loss of on-chip impedance transformation. It would also be advantageous to have the optimum load to have low reactance/susceptance, as in those cases these matching components will have an undesired larger frequency dependence.

Another method to increase the BW of an amplifier is to use higher order matching networks. This creates more zeros and poles that will increase the BW. This is good to use for input matching, however, when used at the load, the lossy components can hurt the PAE and P_{OUT} a bit more. This problem is exasperated at higher frequencies due to the lower Q of the components. This work will use several different semiconductor technologies to compare the effective of using large input matching networks, in tandem with simpler output matching networks to achieve good broadband PA performance at mm-Wave.

It is well-known that negative feedback can also increase the BW of the amplifier design [46]. Although this work uses a broadband negative feedback where gain is sacrificed to extend the BW using a generic negative RC feedback, a derivation is shown next where the BW is extended due to a pole being added to the transfer function to highlight the sacrifice of gain for BW. Consider the classical negative feedback system in Figure 3.5. Suppose this system has a pole at s/ω_0 such as in (3.9). Substituting the new V_{IN} value of $V_{IN} - \beta V_{OUT}$, the close loop gain is derived as (3.10). This reveals that a new pole is formed at $(1 + \beta G_0)\omega_0$, extending the BW as shown in Figure 3.5(a).

$$G(s) = \frac{G_0}{1 + \frac{s}{\omega_0}} \qquad (3.9)$$

$$G_{CL} = \frac{\frac{G_0}{1 + \frac{s}{\omega_0}}}{1 + \frac{s}{(1 + \beta G_0)\omega_0}} \qquad (3.10)$$

However, this negative feedback method can degrade the overall performance of the PA as power gain is being degraded through the feedback. This method does have the benefit of added stability, which may be important when the use of high gain devices necessary for high frequency designs.

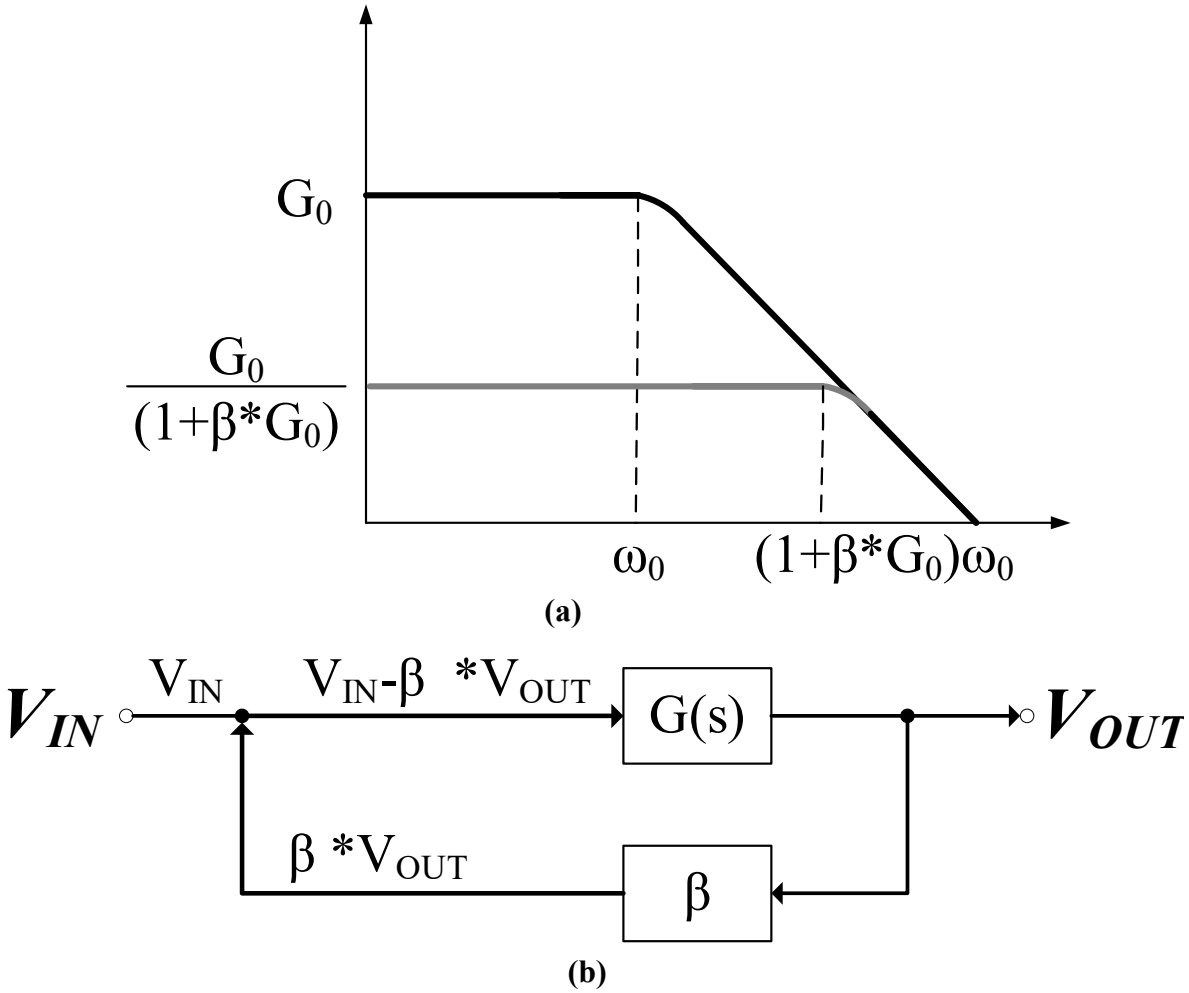


Figure 3.5: Frequency Response of a Negative Feedback Circuit (a), where G_0 is the gain before the Feedback and β is the Feedback factor; (b) simplified Block Diagram of a Negative Feedback System [46]

3.2.4 Additive Amplifiers or Combined Amplifiers Design for Load Modulations

In this section, I will discuss additive amplifiers, or combined amplifiers design, where two (or more) PAs in parallel whose individual outputs change with different driving conditions, and thus the load of the other parallel PA's changes. In this work, these PAs will not be symmetrical, and thus the loads do not just scale with the addition of parallel PAs but instead interact with each other. The interaction of these parallel PAs can be used as another degree of freedom to change the load each device sees.

3.2.4.1 The Doherty PA

The Doherty PA is a classic load modulated PA that has been heavily researched [47-50]. The benefit of the Doherty PA is for its high PAE at power back off. Shown in Figure 3.6(a), this Doherty PA consists of two parallel PAs, a main PA and an auxiliary PA. The signal is first split into two with high isolation between the two ends, such as with a Wilkinson Divider. The main PA is biased in Class A or Class A/B operation, and the auxiliary PA, which often uses a larger device size, can be biased in a Class C mode. With low input powers, the auxiliary PA is turned off due to the Class C biasing; and as the PA is driven more, the auxiliary PA begins to turn on and contributes to the overall output power. Since the auxiliary PA is not on during lower powers, its impact to the PAE of the Doherty PA is low at smaller P_{IN}; however, it can contribute to increase the output power when the main PA begins to compress [25].

Figure 3.6 (b) shows the basic concept of how load modulation works. The devices of the two separate PAs can be approximated as two current generators, a generator for the auxiliary PA and a generator for the main PA.

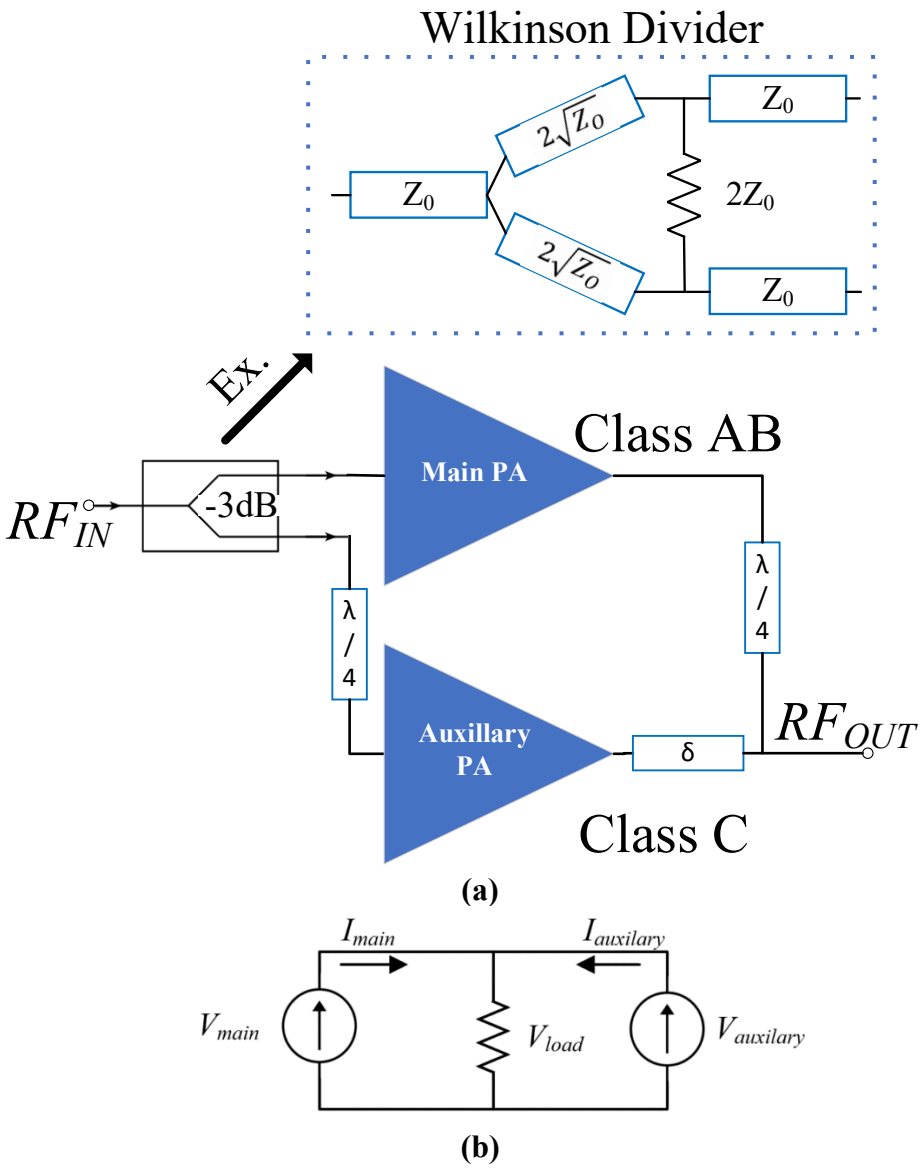


Figure 3.6: Basic Doherty PA Block Diagram (a), (b) Simplified Diagram of Load Modulation in a Doherty PA [25]

The voltage at the load of where the two PAs (here approximated as current generators) combine can easily be found as (3.11) from this approximation with respect to the currents coming from the two generators into the load impedance. With this, the load that the "main" generator sees can be derived as Eq. (3.12). Eq. (3.12) clearly shows the effect that the current of the "auxiliary" generator ($I_{auxilary}$) has on the impedance of the main generator (R_{main}) [25]. However, as the PA is driven more, the current of the "auxiliary" generator will increase and thus the impedance the "main" generator sees will also increase, but this is not this workdesirable in a Doherty PA. Thus, at the output of the main power amplifier is a λ/4 transmission line. This is to complete an impedance transformation so that the impedance that the main PA sees decreases as the current of the auxiliary PA increases so that the voltage at the

output of the main PA remains constant. A λ/4 transformer is put at the input of the auxiliary PA as well so that the two PAs add in phase [25].

$$V_{load} = R_{load}(I_{main} + I_{auxilary}) \qquad (3.11)$$

$$R_{main} = R_{load}\left(\frac{I_{main} + I_{auxilary}}{I_{main}}\right) \qquad (3.12)$$

As this work has shown, the λ/4 transformers are necessary to ensure that maximum voltage is able to be maintained on the main PA output while the auxiliary PA turns on. However, this makes the Doherty PA's BW very narrowband due to the strong frequency dependence on the λ/4 transmission line. There have been some improvements to get BWs higher in references [47-50]. Reference [47] expanded the BW by using lumped elements to do the impedance transformation. This was done in [48] by taking extra care in choice of output capacitance due to the frequency dependence of the impedance transformation when turning on the auxiliary PA. A Lange Coupler is used in [49] to achieve the 90-degree phase shift which improves from the frequency dependance of the λ/4 transmission line. Another issue is that these transmission lines can be quite long, and especially at lower frequencies this can drive the cost up. Some methods to improve upon this includes using a Lange coupler or lumped components such as in references [47-49].

An example of simulated P_{OUT} vs. PAE and gain is shown in Figure 3.7 from a GaAs PA this work designed to show how the effects of this operation are seen. From this graph, it is seen that the main PA is on and starts to compress around 16 dBm, as seen in the dip in the gain and in the PAE, but then the auxiliary PA turns on and the gain and the PAE begins to increase. There are several works that address this dip to be carefully designed out as done in reference [50]. For maximum efficiency, the theoretical analysis of a Doherty PA assumes a zero knee for perfect load modulation. However, when the knee voltage is taken into effect, the efficiency at power back-off is degraded due to the main amplifier not being in saturation when the auxiliary amplifier turns on.

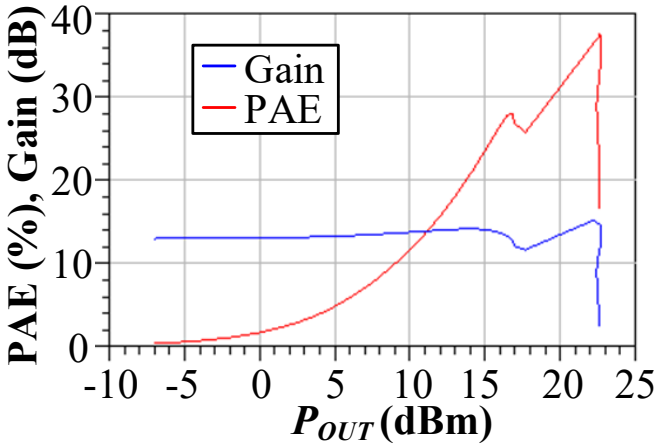


Figure 3.7: Simulated P_{OUT} vs. PAE and gain of a GaAs Doherty PA

3.2.4.2 Asymmetrically Combined PAs

As discussed earlier, one method to get more PA output power is by power combining. This is typically done symmetrically, where the outputs of the parallel PAs are added in phase and the powers are added together. As there is a large dependance in the phase that these signals add, there will be trade-off of output power, BW and efficiency since the phase of the combiner will have a frequency dependence [42]. However, when these PAs are not symmetric and the isolation between these two PAs is removed, this work may improve the BW as shown in Figure 3.8. Even though this practical design technique has been used in the industry for a long time, the theoretical analysis has been discussed carefully by Kaushik Sengupta's group recently in [42-43] but will be briefly summarized in this section. Although the initial work in [43] uses an FPGA to tune the biasing of each half to change the impedance seen by the other half, the work showed that even without changing the biasing, the BW of the asymmetrically combined PA is increased. It is argued that the BW is increased because this technique can create a pseudo-higher-order matching network without lossy series components that can hurt the PAE. Note with a traditional symmetrical power combined system, the impedance is scaled with each added parallel PA; however, with asymmetrically combined PAs, they are assumed and expected to interact with each other.

For a PA that is symmetrically combined, the maximum achievable BW can be given by the Bode-Fano bound in (3.13), where $|r(f)|$is the fraction of the reflected power and $n(f)$is the transfer efficiency. This is compared to (3.14) which shows the same bound by for an asymmetrically combined PA, where $n_{max}$is the maximum efficiency of the network. Thus, the bandwidth is increased by *x N*, where *N* is the number of combined PAs. Figure 3.8 shows a simplified illustration on how an asymmetrically combined PA may improve its bandwidth according to network reciprocity. Interested readers are recommended to check [44-45] for details. However, please note in reality, even with ideal on-chip passive without any loss, it is still not possible to greatly increase the BW of the PA by a very large *x N,* and this may be due to the finite device parasitics capacitances and also the non-negligible resistive loss in the transistors themselves.

$$\int_0^\infty ln\left(\frac{1}{|r(f)|}\right)df = \int_0^\infty ln\left(\frac{1}{\sqrt{1-n(f)}}\right)df \leq \frac{1}{2RC} \quad (3.13)$$

$$\int_0^\infty ln\left(\frac{1}{|r(f)|}\right)df = \int_0^\infty ln\left(\frac{1}{\sqrt{1-n_{max}}}\right)df \leq \frac{N}{2RC} \quad (3.14)$$

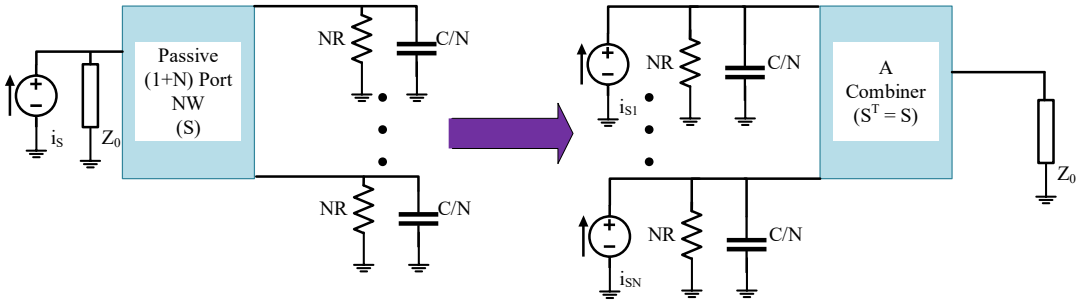


Figure 3.8: An Asymmetrically Combined PA According to [43] with Increased BW for Broadband Operation

3.3 PROCEDURE

For small signal measurements, the data was either taken with Agilent's 38363B or Anritsu's 37397D Network Analyzers. The large signal measurement data was taken with feeding the RF with Agilent's Signal Generator, E8267D and reading the signal with Agilent's Spectrum Analyzer E4448A. All modulated data is taken with National Instruments' PXIE mm-Wave 5G testing bench [51]. For 5 - 22 GHz, the PXIE can generate the RF signals directly. For 22-44.5 GHz, the PXIE creates an IF signal from digital baseband & upconverts the signal in radio heads. These radio heads can be swapped out to cover higher frequency of 71-76 GHz. Ports of the radio heads are assigned to SA (spectrum analyzer) and SG (signal generator) in software GUI for measurement. Many different telecommunication standards can be generated and measured including 5G NR which can be generated greater than a 1 GHz BW signal. This system can define modulation type, BW, number of carriers and subcarrier spacing. Filters can be added to improve and signals can be clipped to achieve a target PAPR. The adjacent channel leakage ratio measurements easily allow for ACLR to be measured with the carrier and subcarrier powers. Digital predistortion can easily be added to improve measurements in the GUI and using the PXIe embedded controller, this system can support wideband envelope tracking to the device under test to improve PAE. All RF is probed using GSG or GSSG probes. In this work, we fed the DC, by gold-wire bonding the DC pads to a custom PCB where additional bypass capacitors are soldered onto the DC lines for stability.

3.4 CONCLUSION

5G has a relatively long and aggressive roadmap that includes going higher in frequency with more operating bands. MIMO phased array systems require a lot of FEMs, and with all these operating bands, broadband mm-Wave highly-efficient PAs would be very attractive to help reduce the number of hardware components needed for both commercial and DoD mm-Wave systems. This work will utilize several state-of-the-art semiconductor technologies, including a 22 nm CMOS FD-SOI process, a 90 nm SiGe BiCMOS process, and a 40 nm GaN HEMT technology.

As what was a constant theme in this section, there is always a design trade-off of PA's PAE, linearity, BW, cost and output power, especially at mm-wave frequencies. This work discussed some techniques that can be used to optimize the max. PAE and BW considering these trade-

offs that this are used in this work with different technologies, and these details and design examples will be discussed next. The design goals are to target for the max. PAE to be hopefully above 35% to 45% and cover as much of the 18 – 50 GHz bandwidth as possible, with RF output power P_{OUT} above 16 dBm per PA.

4 RESULTS AND DISCUSSIONS

4.1 GaN Results and Discussions

This section utilizes HRL Laboratories' advanced T3 40 nm GaN HEMT (High Electron Mobility Transistor) technology on SiC. This is a T-gate technology, which benefits over field plate technologies by having higher f_T/f_{MAX} and low contact resistance while having the ability to operate at a lower supply voltage [23]. This particular technology achieves a knee voltage of ~2 V, I_{DMAX} of 1.6 A/mm, V_{BR} of 50 V, f_T of 220 GHz and f_{MAX} of 400 GHz [24]. It also boasts low on-resistance of < 0.9 Ω·mm. This process offers backvias, which can be used to reduce the source parasitics to ground. Typically, GaN is used for higher power applications; however, this work is able to take advantage of lower optimum supply voltages to design medium-power mm-Wave PAs and this, to the best of our knowledge, are the first medium-power, broadband GaN PAs that covers the vast majority of the 5G FR2 band. Using GaN has other benefits such as better thermal conductivity and robust breakdown, especially if advanced GaN on Si substrate can be mass produced in the near future to reduce its cost drastically [51].

4.2 Broadband mm-Wave GaN PA Using A Higher Order Input Matching Network

First, broadband PAs are designed using a higher-order input matching network. This will then be compared to broadening the BW of PAs using an RC feedback in the next section. All PAs use the same initial steps of conducting load-pull simulations on several device sizes with measurement-based models, and a 4 *x* 37.5 µm device is chosen for good trade-off of high PAE and gain and this device will be used in all of these single-stage PAs. In addition, all these monolithic PA designs include the input and output matching networks, RF choke and a 1 pF bypass capacitor on all the DC pads on-chip.

As what had been described in Chapter 3, in order to achieve broadband high PAE performance, it would be advantageous that the device's optimum load for max. PAE be near 50 Ω across the design frequencies to reduce the number of lossy components for realizing low-loss impedance transformation. In addition, having small reactance for the device output in broadband designs is preferred to minimize frequency dependence in the impedance transformation. Fundamental load-pull simulations for max. PAE circles are done on the 4 *x* 37.5 µm device using Cadence AWR as shown in Figure 4.1 for V_{DD} = 4/6/12 V at 18/28/44 GHz. With a 12 V supply, not only is the PAE lower than with a 4/6 V supply, but the optimum load has higher reactance. For instance, at 28 GHz, the optimum load for max. PAE for 12 V is 51.5 + 113.5*j, and for 6 V it is 50 + 82*j.

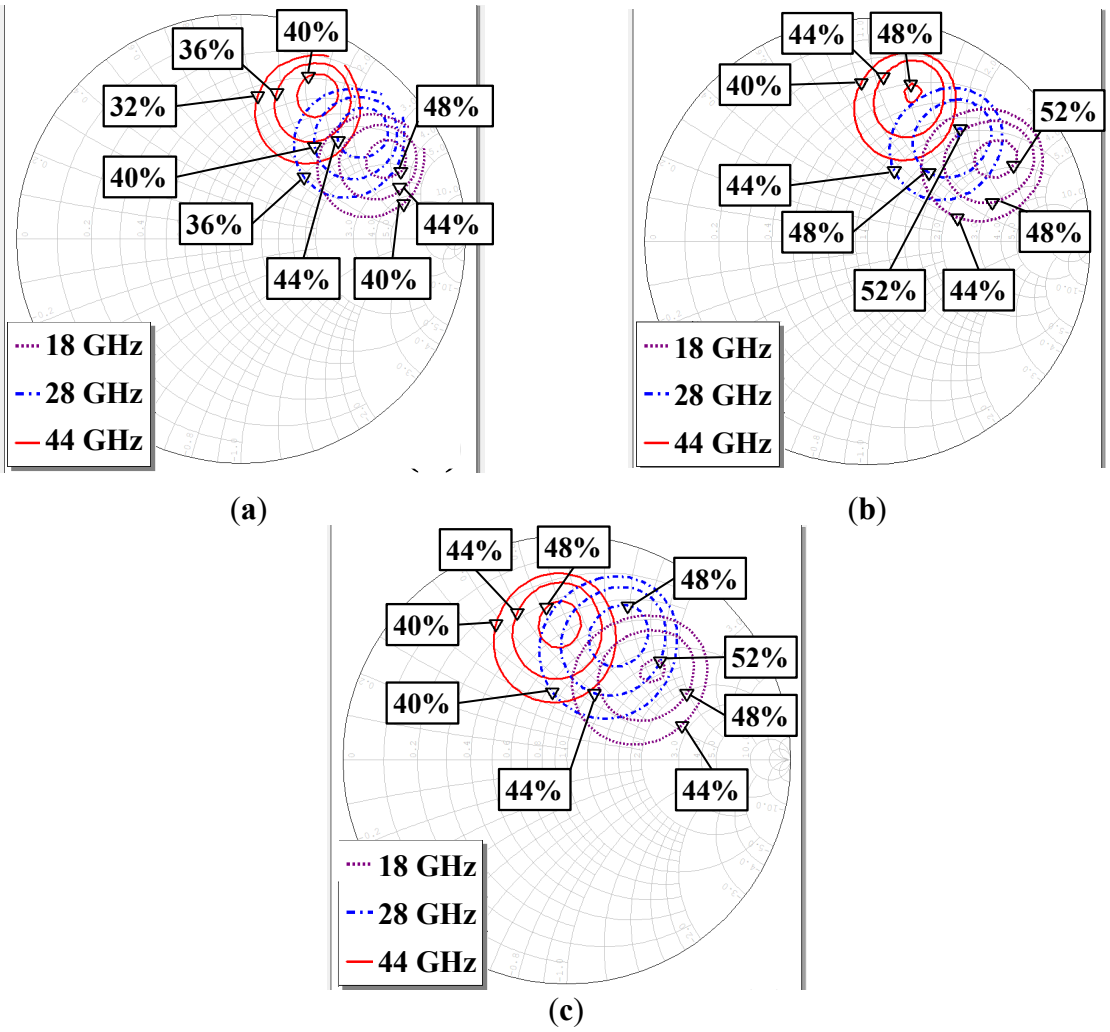


Figure 4.1: Fundamental PAE Load-pull Simulations on a GaN 4 *x* 37.5 µm Device with V_{DD} = (a) 12 V, (b) 6 V, and (c) 4 V.

Using the load-pull simulations, the output matching is designed using only 3 matching components (including the RF choke) to minimize loss. A 3rd-order input matching network is utilized to broaden the input match and increase the usable gain bandwidth. The schematic for this design is shown in Figure 4.2. The PA is biased at a class A/B mode for good trade-off of linearity and PAE.

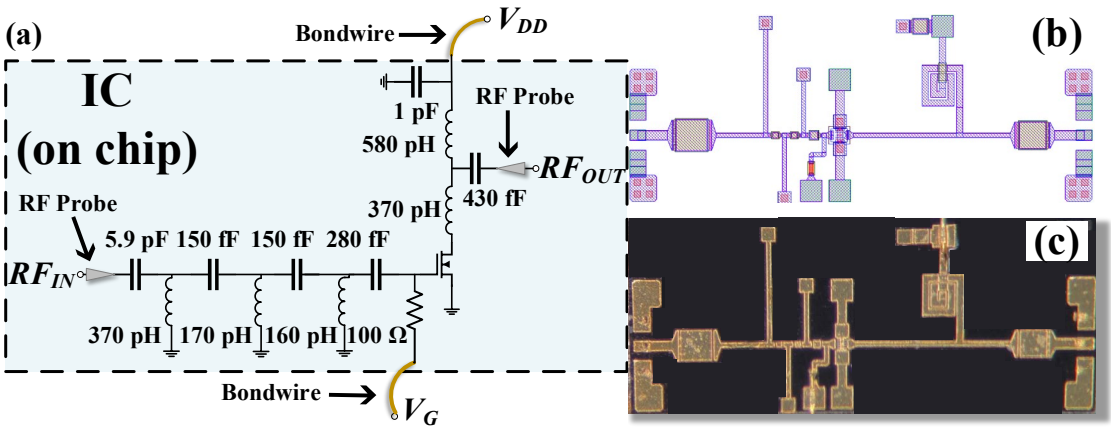


Figure 4.2: Schematic (a); (b) Layout; and (c) Micrograph of the 2.1 *x* 0.88 mm^2 Broadband mm-Wave GaN PA Designed in this Work

Post-layout EM load-pull simulations with the full GaN PA are performed for V_{DD} = 4 – 12 V and the max. PAE circles are plotted in Figure 4.3 for 18/28/44 GHz. For V_{DD} = 12 V the PA does not have the best broadband performance similarly to the results in Figure 4.1. However, for V_{DD} = 4 V, the design is almost perfectly matched to the optimum PAE load near 50 Ω at 28 GHz. In a full PA design load pull, it is ideal for the optimum loads to be near the system's characteristic impedance so that the optimum performance is achieved; here V_{DD} = 4 V provides an optimum supply bias for good PAE across 18 – 44 GHz with near 50 Ω match.

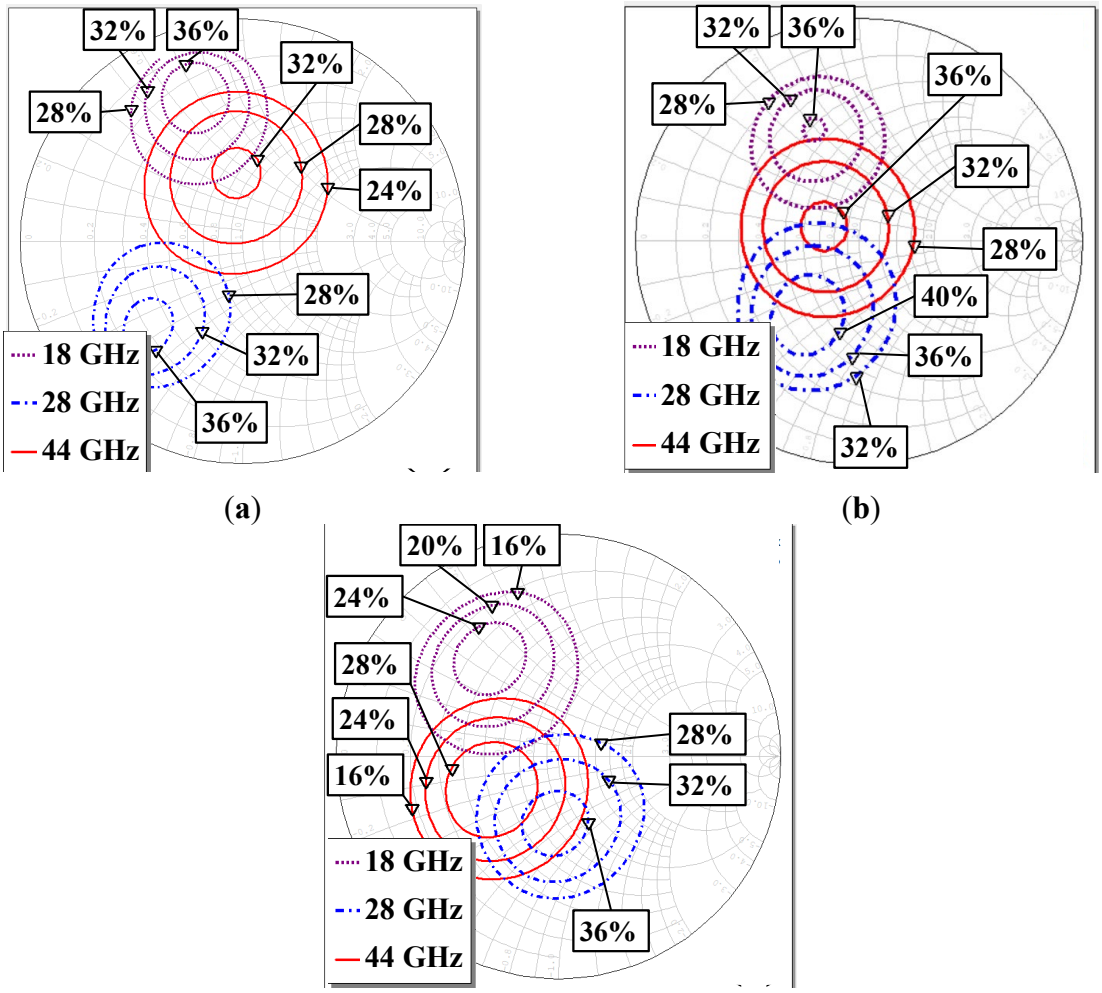


Figure 4.3: Post-layout Fundamental PAE load-pull EM Simulations Done on Full 1-stage GaN PA with V_{DD} = (a) 12 V, (b) 6 V, and (c) 4 V.

Figure 4.4 shows the S-parameter measurements vs. post-layout EM simulations of the broadband GaN PA. This PA achieves max. S21 of 12.5 dB and small-signal 3-dB BW of 18 – 38.7 GHz at VDD = 6 V, max. S21 =10.3 dB with BW = 18 – 40.3 GHz at VDD = 4 V, and max. S21 =13.0 dB with BW = 18.3 – 32.7 GHz at VDD = 12 V. This work see that the S21 modeling at VDD = 4 V is not as accurate vs. at VDD = 6/12 V, which may be due to fact that the 4 V model is constructed from extrapolation, whereas the 6/12 V models are constructed from direct measurements.

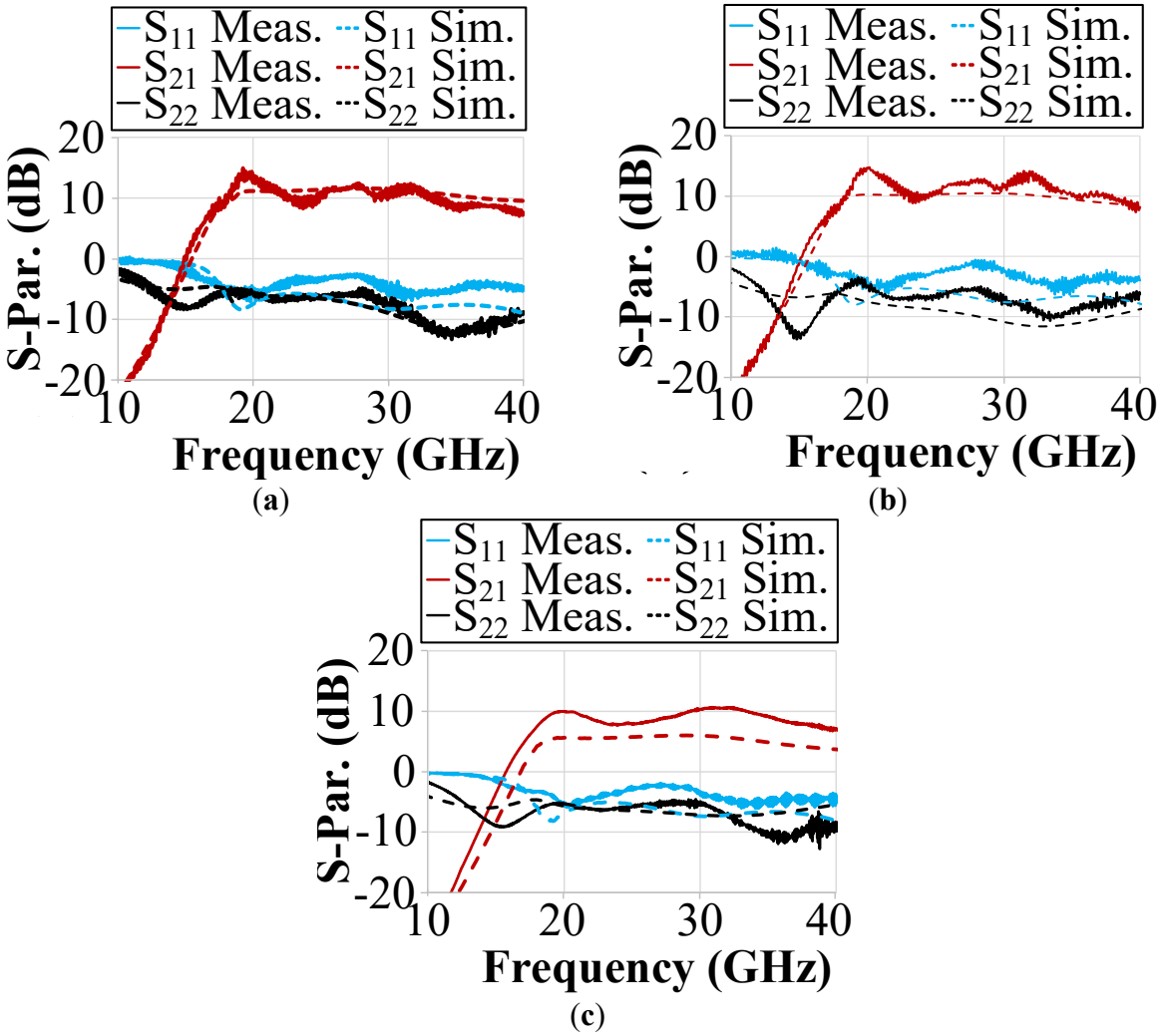


Figure 4.4: S-parameter Measurements of the Broadband GaN PA with V_{DD} = (a) 12 V, (b) 6 V, and (c) 4 V.

The large signal measurement vs. post-layout EM simulation is shown in Figure 4.5 for 28 GHz at VDD = 4/6/12 V. Here, this PA achieves max. PAE/POUT,SAT of 34.6%/ 20.3 dBm at VDD = 6 V, and 23.3%/ 22.8 dBm at VDD = 12 V and at VDD = 4 V, it achieves max. PAE/ POUT,SAT of 42.1%/ 18.6 dBm. This measurement data is summarized in Table 4.1. Note Figure 4.6 shows that lowering VDD from 12 V to 4/6 V not only achieves higher PAE, but it also makes the PA more broadband, as suggested from Figures. 4.1 and 4.3. The modeled large-signal PA data at VDD = 4 V is again not as accurate vs. the measured data at VDD = 6/12 V as shown in Figure 4.7. Nonetheless, measurement results demonstrated a superior performance at VDD= 4 V, allowing its usage in medium power broadband mm-Wave applications.

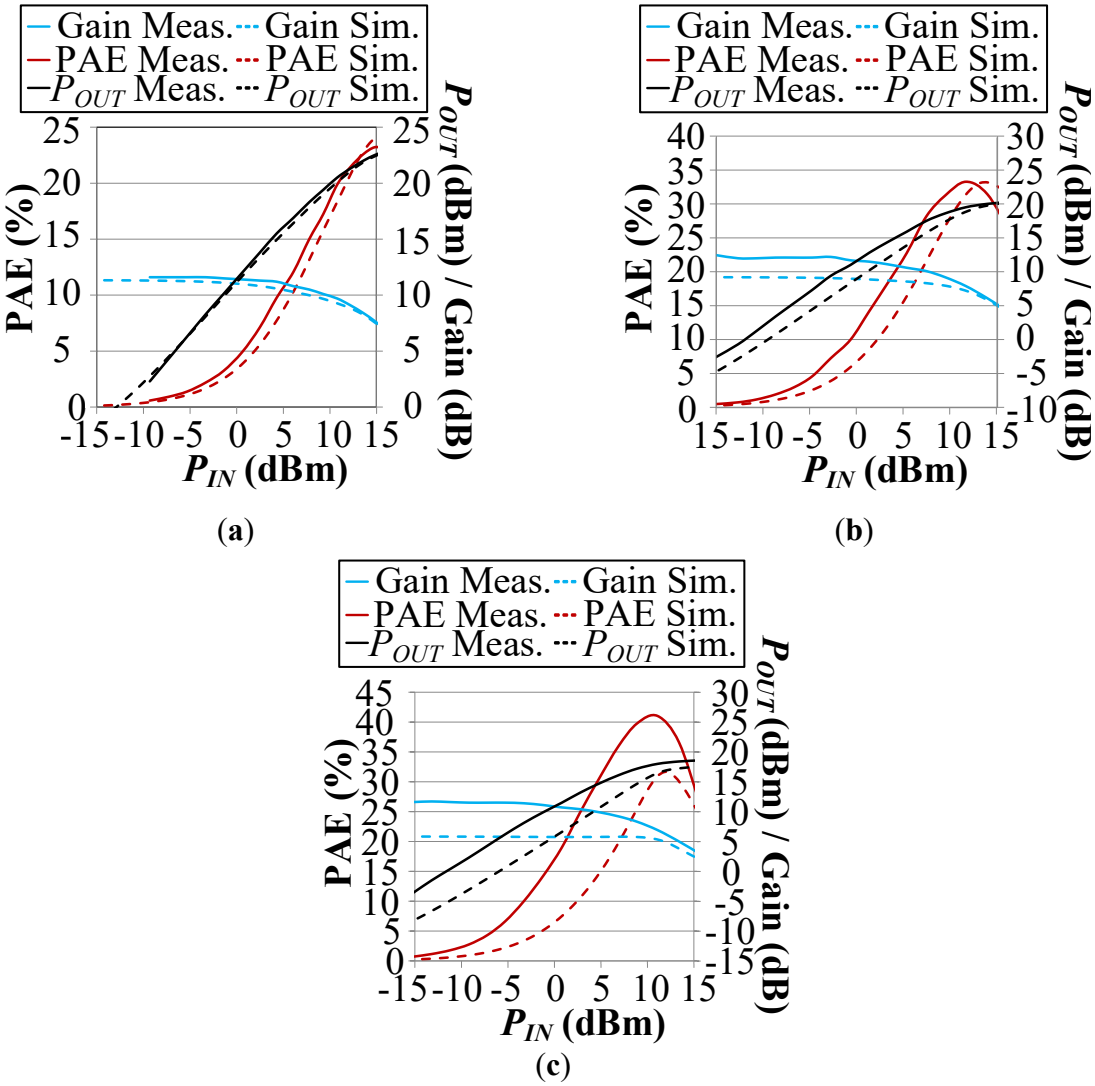
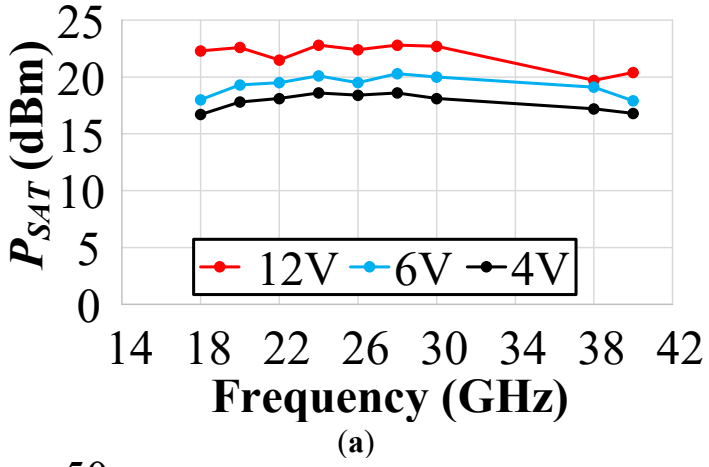
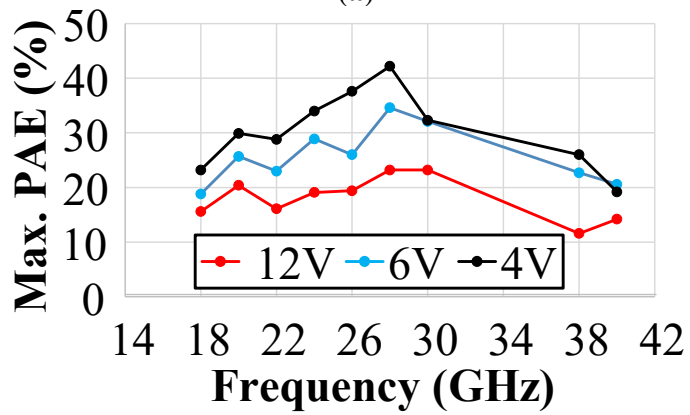


Figure 4.5: P_{IN} vs PAE, P_{OUT} and Gain Measurements of the Broadband GaN PA with V_{DD} = (a) 12 V, (b) 6 V, and (c) 4 V at 28 GHz



(a)



(b)

Figure 4.6: Measured (a) $P_{OUT,SAT}$ vs. Frequency and (b) max. PAE vs. Frequency of the Broadband GaN PA

Table 4.1. Summary of the Large Signal Single-ended GaN with 3rd-Order Input Matching PA Measurements

V_{DD} (V)	Freq. (GHz)	Max. PAE (%)	$P_{OUT,SAT}$ (dBm)	OP_{1dB} (dBm)
4	18	23.2	16.7	11.2
	28	42.1	18.6	11.5
	38	26.0	17.2	13.4
6	18	22.7	20.3	13.6
	28	34.6	20.3	14.4
	38	22.7	19.1	14.6
12	18	15.6	22.3	15.6
	28	23.2	22.8	18.3
	38	11.6	19.7	13.7

Linearity is tested with a 9x100 MHz 256-QAM modulated 5G NR input at PAPR (peak-to-average-power ratio) = 8 dB as shown in Figure 4.7. They are measured with the state-of-the-art

mm-Wave PXIE system by National Instruments (NI), which can produce modulated 5G NR signals of up to 1 GHz BW up to 44 GHz [52]. At 28 GHz, this PA achieves ACLR = -26.8 dBc / -27.0 dBc with P_{OUT} = 14.2 dBm/ 11.3 dBm and PAE_{AVE} of 14.0% /13.9% at V_{DD} = 6V/4V. At 38 GHz it achieves ACLR of -28.0 dBc / -27.9 dBc at P_{OUT} = 12.4 dBm/ 10.8 dBm and PAE_{AVE} of 10.5% /12.6%. Table 4.2 shows a comparison to state-of-the-art broadband medium power mm-Wave 5G PAs. Our PA achieves the best small signal 3-dB BW in literature, with excellent peak PAE and good broadband linearity. To the best of our knowledge, this is the first reported medium power broadband GaN PA for mm-Wave 5G. Adjusting V_{DD} from 12 V to 4 V can achieve an optimal trade-off on PAE and P_{OUT}, which is not feasible for silicon-based stacked broadband mm-Wave PAs.

Table 4.2. Comparison of the Single-Ended Broadband PA with 3rd-Order Input Matching Network to other Medium Power State of the Art PAs

Ref.	Tech.	Design	Supply Volt. (V)	3-dB BW (GHz)	Freq. (GHz)	$P_{OUT,SAT}$ (dBm)	Max. PAE (%)	Gain (dB)	Signal Type	ACLR (dBc) @P_{OUT} (dBm)
[53]	65-nm CMOS	Multi-port load-pulling	1.1	26-42	28	19	21	15	1 GHz 64-QAM OFDM	–@7.5 PAE=5.1%
					37	19.6	21.9	16	2 GHz 64-QAM OFDM	-25@9.8 PAE=10.2%
[54]	0.15 µm GaAs	Trans-former -Coupled	4	21.6-32.5	28	26.5	31	12.6	64QAM 6Gb/s	-30@ 21.6 PAE=13.5%
									64QAM 9Gb/s	-30@19.9 PAE=9.5%
[55]	130-nm SiGe	2-stage Doherty	1.5	23.3-39.7	28	16.8	20.3	18.2	64-QAM 500 MSym/s	-28.4@9.2 Coll. Eff. =18.5%
					37	17.1	22.6	17.1		-28.2@9.5 Coll. Eff. =19.2%
					39	17	21.4	16.6		-29.8@9.3 Coll. Eff. =17.2%
[56]	45nm SOI CMOS	Continuous Hybrid Class F/F^{-1}	2	23-40.5	28	18.9	43.2	18.7	64-QAM 500 MSym/s	-28@10.3 PAE=13.1%
					37	18.9	37	18		-30.5@11.7 PAE=11.9%
					39	18.9	36	15.6		-28@11 PAE=10.2%
[57]	0.2 µm GaN on SiC	3-stage Harmonic Tuning	28	29-34	33	39.5	36	25	-	-
This work	40-nm GaN	3rd-order input match 1-stage	4	18-40.3	24	18.6	34	7.8	9x100 MHz 256-QAM 5G NR	-27.7@9.7 PAE=8.1%
					28	18.6	42.1	9.2		-27@11.3 PAE=13.9%
					38	17.2	26	7.9		-27.9@10.8 PAE=12.6%
This work	40-nm GaN	3rd-order input match 1-stage	6	18-38.7	24	20.1	28.9	9.6		-27@11.9 PAE=10.2%
					28	20.3	34.6	11.9		-26.8@14.2 PAE=14.0%
					38	19.1	22.7	10.2		-28@12.4 PAE=10.5%

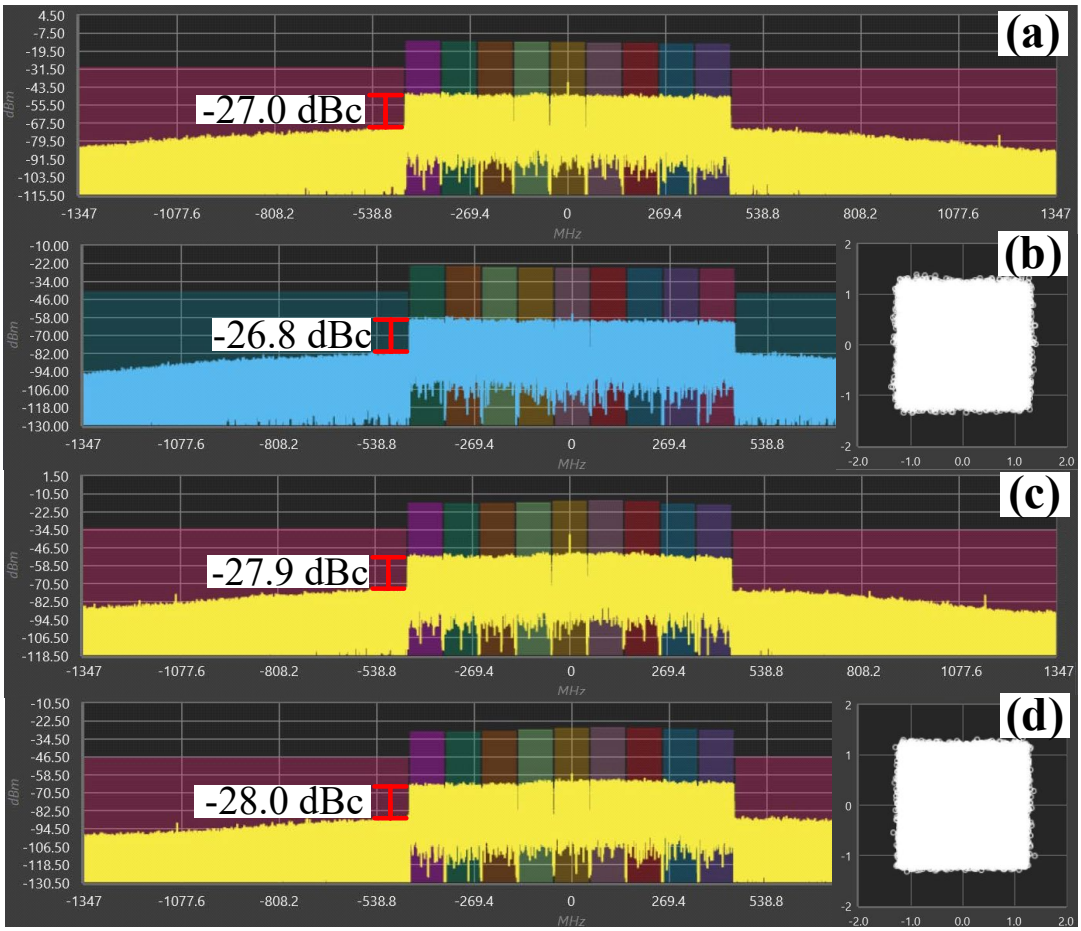


Figure 4.7: ACLR Measurements of the Broadband GaN PA

A 9x100 MHz 256-QAM NR at 28 GHz for V_{DD} = (a) 4 V and (b) 6 V and (c) at 38 GHz for V_{DD} = 4 V (d) and 6 V. Constellation diagrams are shown in (b) & (d) too.

After the design and characterization of the previous single-ended broadband GaN PA, a differential broadband mm-Wave 5G PA as shown in Figure 4.8 is designed by expanding upon that common-source (CS) design by adding neutralization capacitors for improved MSG (maximum stable gain). In addition, RC traps were added at the gates of these GaN transistors to further stabilize the PA [58]. Although this is a differential design, its layout is only slightly larger than the 1.85 mm^2 area of the single ended design, with an area of 1.94 mm^2 (with pads). PEX EM simulations in Axiem indicate that this differential GaN PA achieves 3-dB BW from 20.1 – 44.3 GHz (or an absolute BW of 75.2%) and max. S_{21} of 13.4 dB, at V_{DD}= 6 V. This has a BW that is comparable to the single-ended GaN design presented earlier in this section, but with higher gain and P_{OUT}.

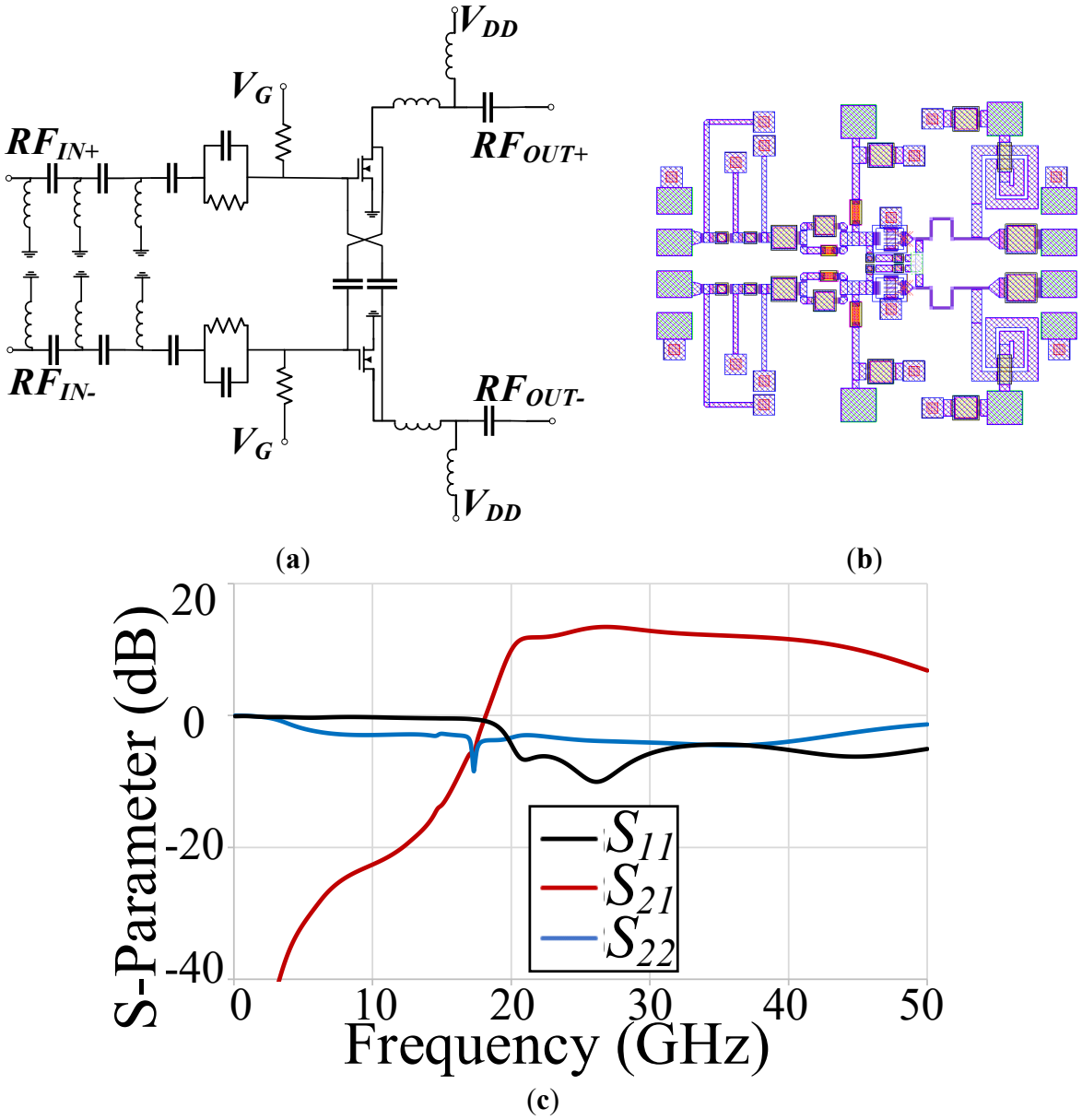


Figure 4.8: Simplified Schematics (a) and (b) the Layout of the Broadband Differential GaN PA using a 3rd-order Input Matching Network (2.0 *x* 0.97 mm² with pads); and (c) its S-parameter EM PEX Simulation Results

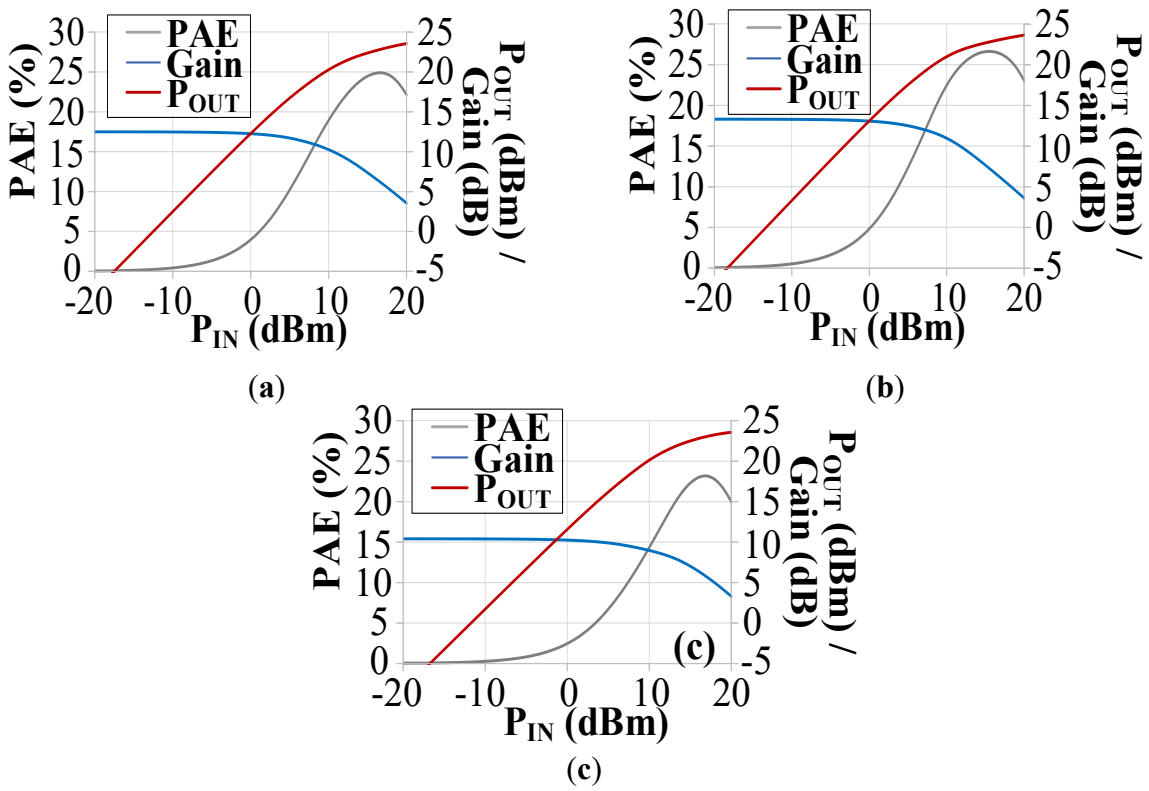


Figure 4.9: Large-signal EM PEX Simulations of the Broadband Differential GaN PA using a 3rd-order Input Matching Network for CW Inputs at (a) 24, (b) 28 and (c) 44 GHz

The large signal EM simulations results for this differential GaN PA with neutralization capacitors and a 3rd-order input matching network are shown in Figure 4.9, which indicates that this PA can achieve max. PAE of 24.9%/ 26.6%/ 23.3% and $P_{OUT,SAT}$ of 23.5/ 23.6/ 23.3 dBm at 24/ 28/ 44 GHz with V_{DD}= 6 V (Table 4.3). Figure 4.10 shows the broadband nature of this PA, as it is able to achieve > 20% max. PAE across the 20 – 44 GHz band, and has a very high simulated 1-dB $P_{OUT,SAT}$ BW and also $P_{OUT,SAT}$ larger than ~23 dBm in the 5G FR2 band of interest. Compared to the measured single-ended version of the GaN PA, it achieves similar max. PAE, while having ~ 3 dB greater $P_{OUT,SAT}$ than the single-ended design.

Table 4.3. Summary of EM PEX Simulation the Broadband Differential GaN PA Using a 3rd-Order Input Matching Network

Freq. (GHz)	S_{11} (dB)	S_{21} (dB)	Max. PAE (%)	OP_{1dB} (dBm)	$P_{OUT,SAT}$ (dBm)
24	-7.4	12.5	24.9	17.5	23.5
28	-8.0	13.3	26.6	18.3	23.6
44	-6.2	10.4	23.3	17.4	23.3

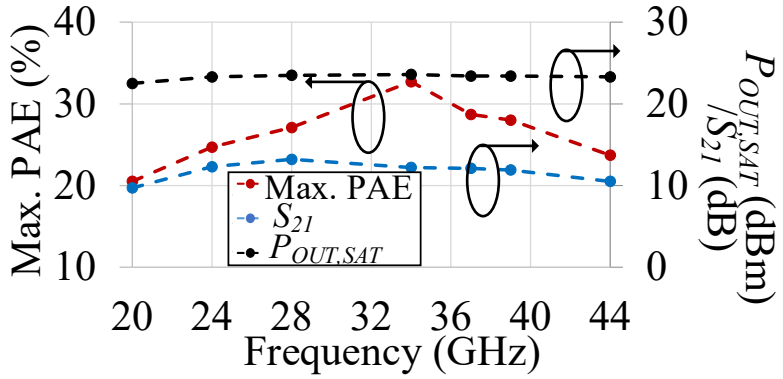


Figure 4.10: EM PEX Simulated Max. PAE, S_{21} and $P_{OUT,SAT}$ vs Frequency of the Broadband Differential GaN PA using a 3rd-order Input Matching Network

4.2.1 Broadband mm-Wave GaN PA Using RC Feedback

Next, to achieve broadband results in this technology, the RC feedback technique is utilized, using the same 4 *x* 37.5 µm device used in the 3rd-order input matching network design (Figure 4.11). The simulation vs. measurement S-parameters are shown in Figure 4.11 and this design in simulation achieves 3-dB BW of 17.2 – 50.4 GHz with max. S_{21} of 10.3 dB with V_{DD}= 6 V. Thus, in simulation, this PA did achieve better 3-dB BW compared to the version using a higher order input matching network. In addition, with an area of 1.08 mm^2, it also reduces the area compared to the design using a 3rd-order input matching due to the ability to use a simpler and smaller input matching circuit. However, gain is much less, which is to be expected since there is a sacrifice to gain when using an RC feedback, as discussed in Chapter 3. As Figure 4.11 shows, there is a discrepancy between the simulation and measurement results, specifically with the gain, which is due to processing issues that resulted in a degradation in the g_m for this MPW (multi-project wafer) run. This will be discussed in Chapter 5 in the future plans.

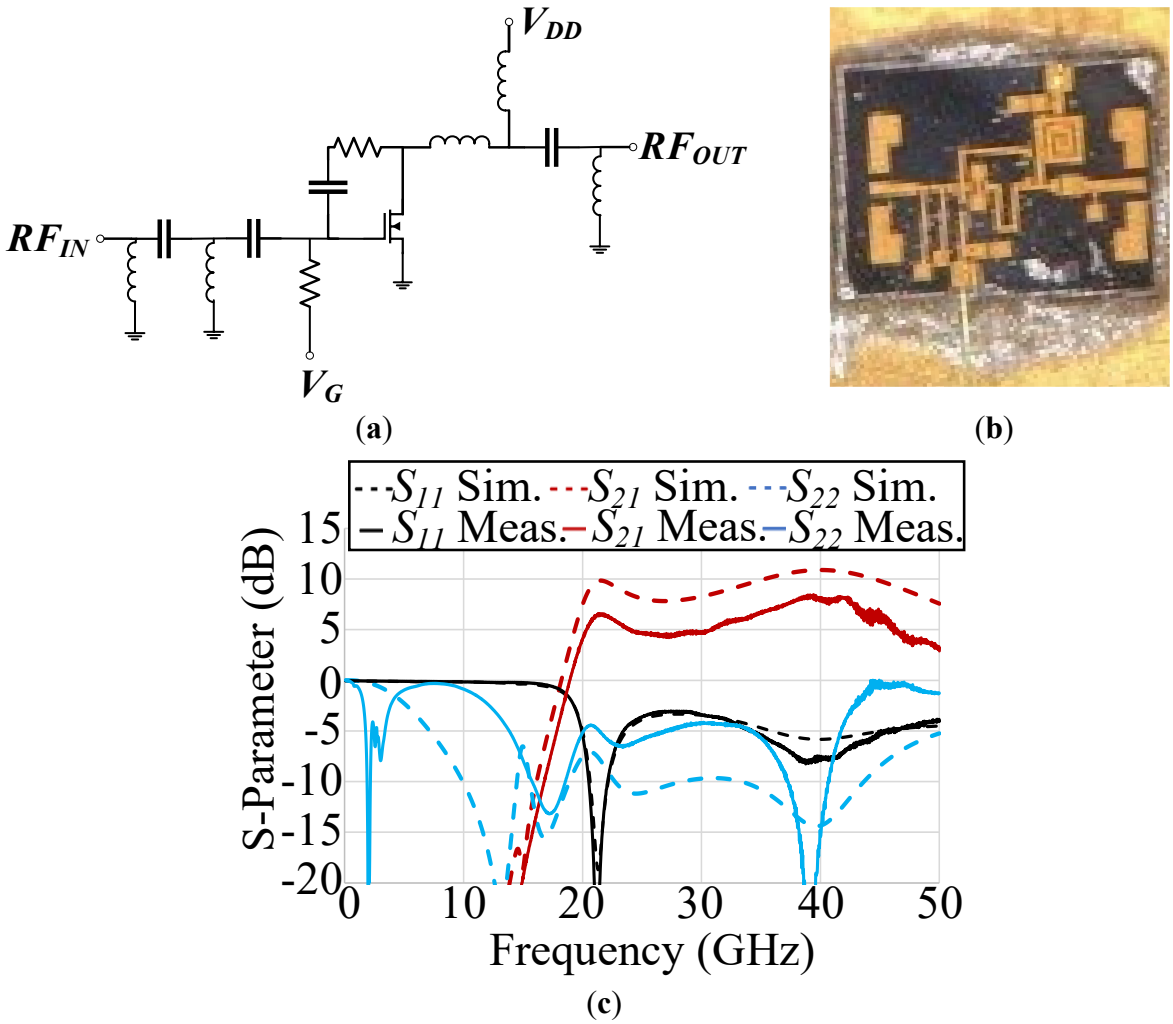


Figure 4.11: Simplified Schematics (a) and (b) the Layout of the Broadband Single-ended GaN PA with RC Feedback (1.2 *x* 0.9 mm^2 with pads); and (c) its S-parameter EM PEX Simulation vs. Measurement Results

Due to the large degradation of gain, the large signal results will only be discussed in EM simulation and the large signal simulated results are shown in Figure 4.12 for V_{DD} = 6 V. The results for this PA are also summarized in Table 4.4. The broadband nature of this design is shown in Figure 4.13, which plots max. PAE, $P_{OUT,SAT}$ and S_{21} vs. frequency. Although the BW of this design is higher, the max. PAE and $P_{OUT,SAT}$ with the RC feedback is comparable to that of the design with a 3rd-order input matching network. Thus, with a sacrifice to gain, the BW can be improved without much of a degradation in max. PAE and $P_{OUT,SAT}$, but measurements (on the dies being fabricated that this work have not received yet) must be taken on this to confirm these findings.

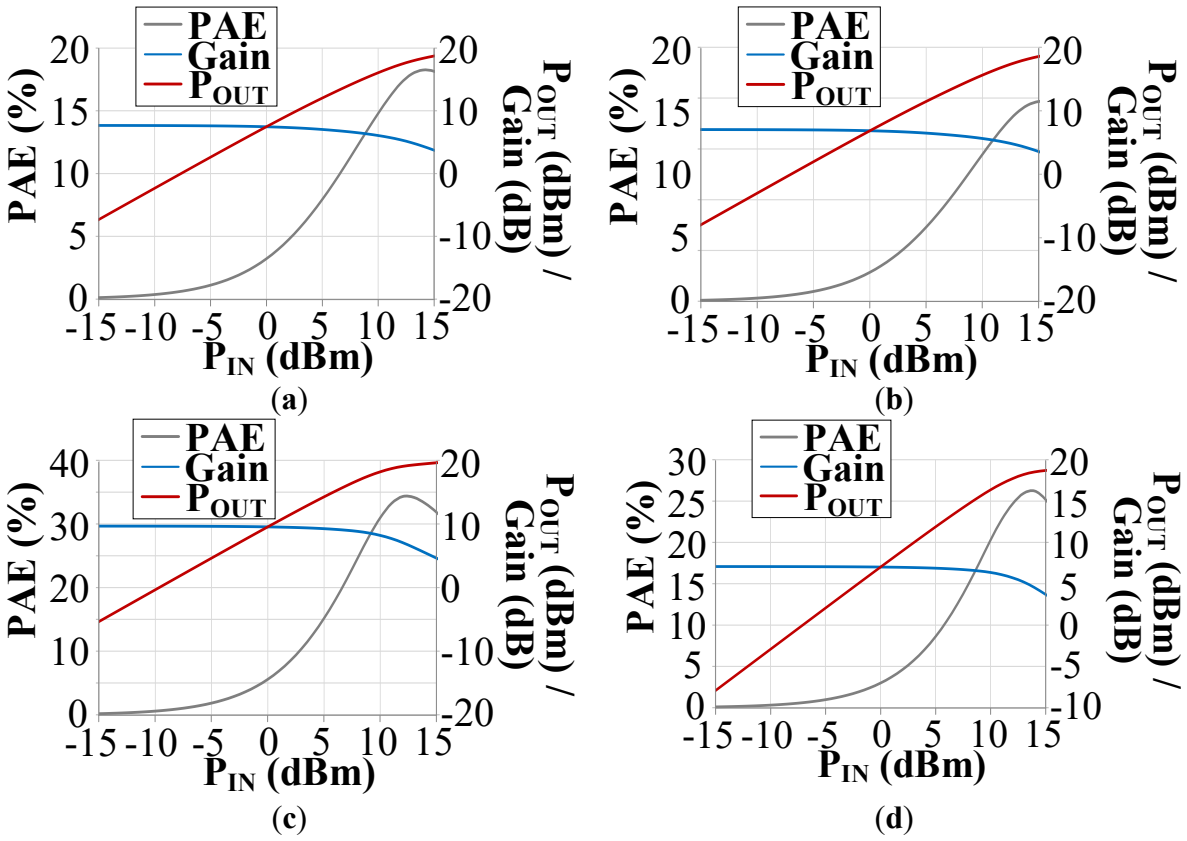


Figure 4.12: Large-signal of the Broadband Single-ended GaN PA using RC Feedback with V_{DD} = 6 V at (a) 24, (b) 28, (c) 44 (d), and 50 GHz

Table 4.4. Summary of EM PEX Simulation Broadband Single-ended GaN PA using RC Feedback

Freq. (GHz)	S_{11} (dB)	S_{21} (dB)	Max. PAE (%)	OP_{1dB} (dBm)	$P_{OUT,SAT}$ (dBm)
24	-4.7	8.5	18.2	14.5	20.2
28	-3.3	7.9	19.7	14.0	20.2
44	-5.2	10.2	34.2	17.6	20.4
50	-4.5	7.6	26.2	17.1	19.4

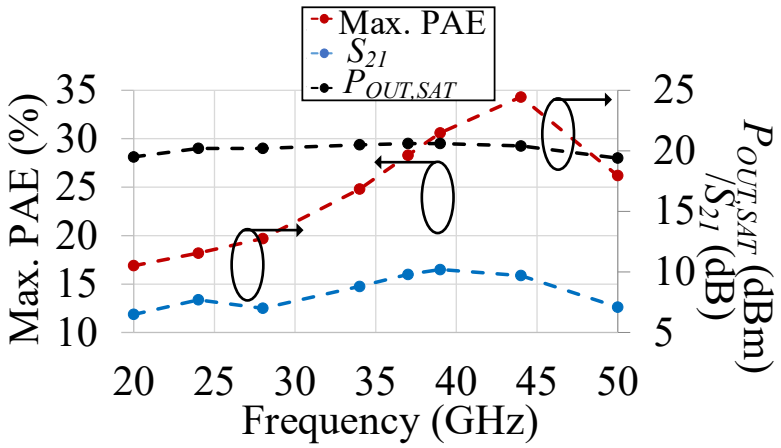


Figure 4.13: EM PEX Simulated max. PAE, S_{21} and $P_{OUT,SAT}$ vs. Frequency of the Broadband Single-ended GaN PA using rc Feedback

Like what had been done on the 3rd-order input matching network design, the design with RC feedback is made differential and neutralization capacitors are added (Figure 4.14). With an area of 1.94 mm^2, this design is ~x2 of the 1.08 mm^2 single-ended version of this design.

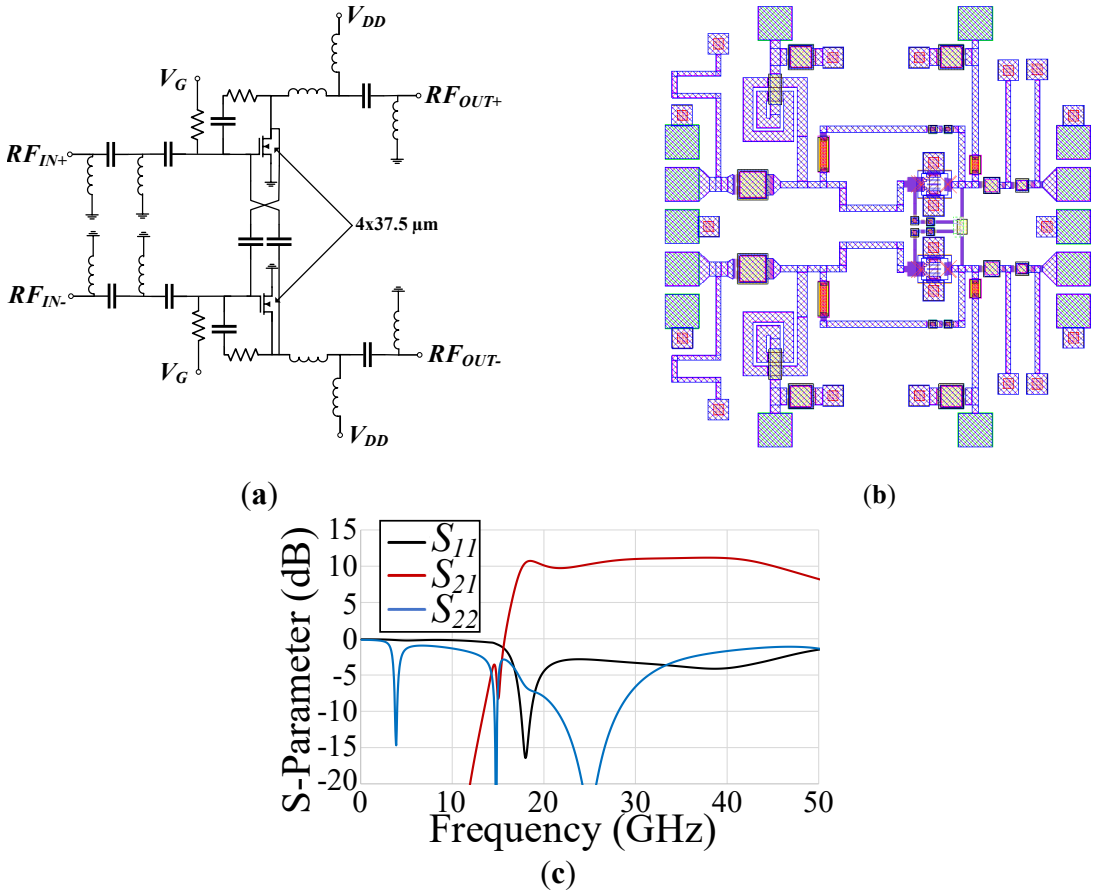


Figure 4.14: Simplified Schematics (a) and (b) the Layout of the Broadband Differential GaN PA using RC Feedback and Neutralization Capacitors (2.0 *x* 0.97 mm^2 with pads); and (c) its S-parameter EM PEX Simulation Results

The S-parameter EM PEX simulations are shown in Figure 4.14, and this PA achieves 3-dB BW of 17.2 – 50 GHz with max. S_{21} of 11.2 dB with V_{DD} = 6 V. Thus, making the single-ended design with RC feedback into a differential topology so that neutralization capacitors could be utilized, increased the gain by ~1 dB. However, due to the RC feedback, the gain is reduced when compared to when a higher order input matching network is used to achieve broadband results as this design achieves max. S_{21} of 11.2 dB while the differential design using the 3rd-order input matching network achieves 13.4 dB of gain. Just as with the single-ended versions, using RC feedback increased the BW when compared to using a higher-order input matching network version. The large signal results are shown in Figure 4.15 and summarized in Table 4.5 with V_{DD} = 6 V, and this does achieve ~3 dB more output power when compared to the single-ended version. Additionally, power is also reduced in this design compared to the 3rd-order input matching design, reducing from ~23 dBm $P_{OUT,SAT}$ to ~22 dBm $P_{OUT,SAT}$ which is to be expected due to the power reduced through the feedback. However, the Figure4.16 plots max. PAE, $P_{OUT,SAT}$ and S_{21}, which shows that this PA is also quite broadband.

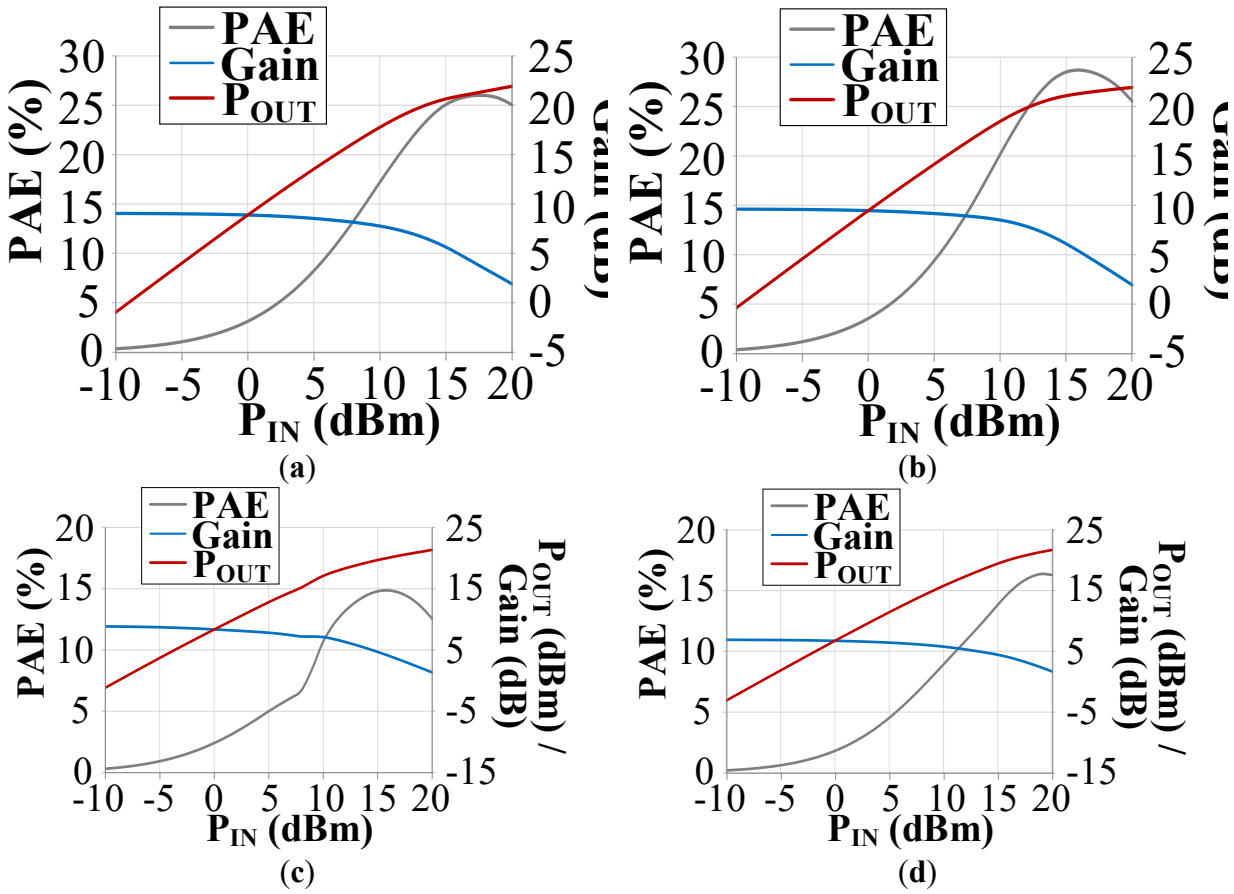


Figure 4.15: Large-signal EM PEX Simulation of the the Broadband Differential GaN PA using RC Feedback and Neutralization Capacitors with V_{DD}= 6 V at (a) 24, (b) 28, (c) 44, and (d) 50 GHz

Table 4.5. Summary of EM PEX Simulation the Broadband Differential GaN PA using RC Feedback and Neutralization Capacitors

Freq. (GHz)	S_{11} (dB)	S_{21} (dB)	Max. PAE (%)	OP_{1dB} (dBm)	$P_{OUT,SAT}$ (dBm)
24	-2.8	10.0	26.0	16.1	21.9
28	-3.1	10.8	28.7	17.7	21.9
44	-3.2	10.3	14.7	11.0	21.3
50	-1.5	8.2	16.4	15.8	21.7

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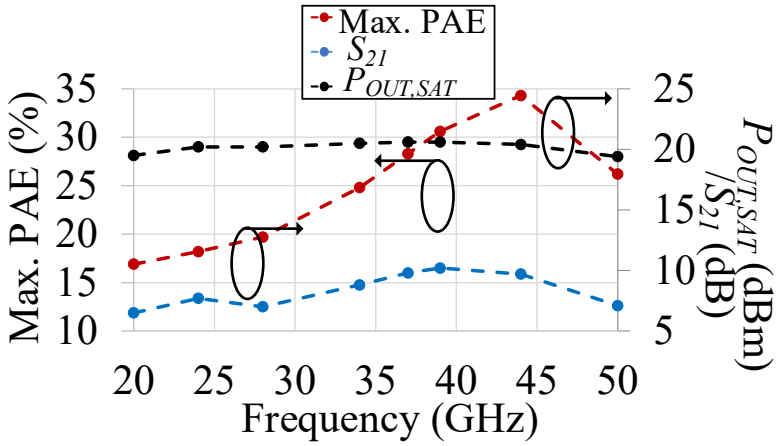


Figure 4.16: EM PEX Simulated max. PAE, S_{21} and $P_{OUT,SAT}$ vs. Frequency of the Broadband Differential GaN PA using RC Feedback

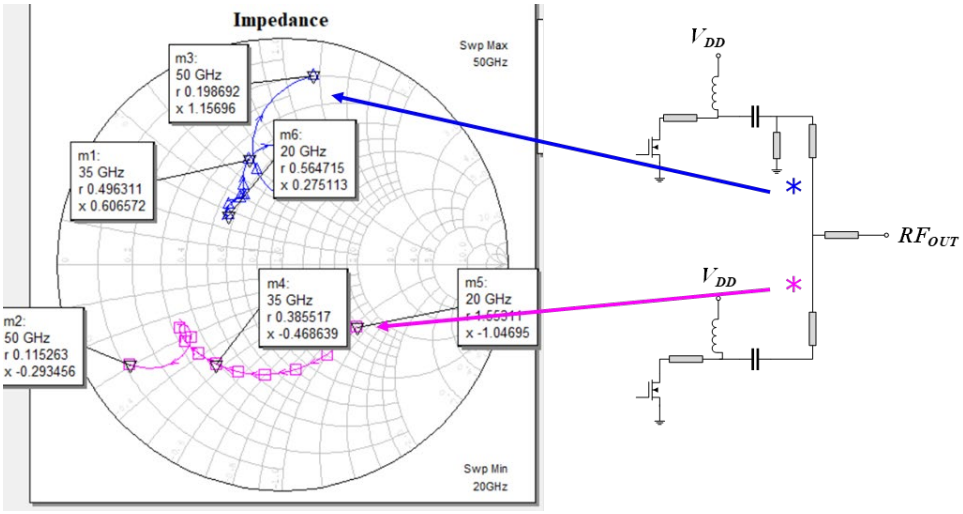


Figure 4.17: Impedance of the Asymmetric Combiner for the GaN PA

4.1.2. ASYMMETRICALLY COMBINED GAN PAS

The BW of a PA can also be expanded using a novel asymmetrically combined PA architecture using this GaN technology, such as what had been discussed in Chapter 3 [44-45]. Figure 4.17 shows the asymmetrical combiner of this PA which shows that this combiner is close to fulfilling the requirement that the impedances looking into the combiner should be close to $\Gamma_1 = \Gamma_2^*$ across the design frequencies of 20 - 50 GHz. The schematic of the two-stage asymmetrically combined PA is shown in Figure 4.18. The asymmetrically combined PA improves the BW and optimum PAE, so in order to improve the S_{11} this work use a high order input matching network. For this design, this work were targeting for Watt-level output powers.

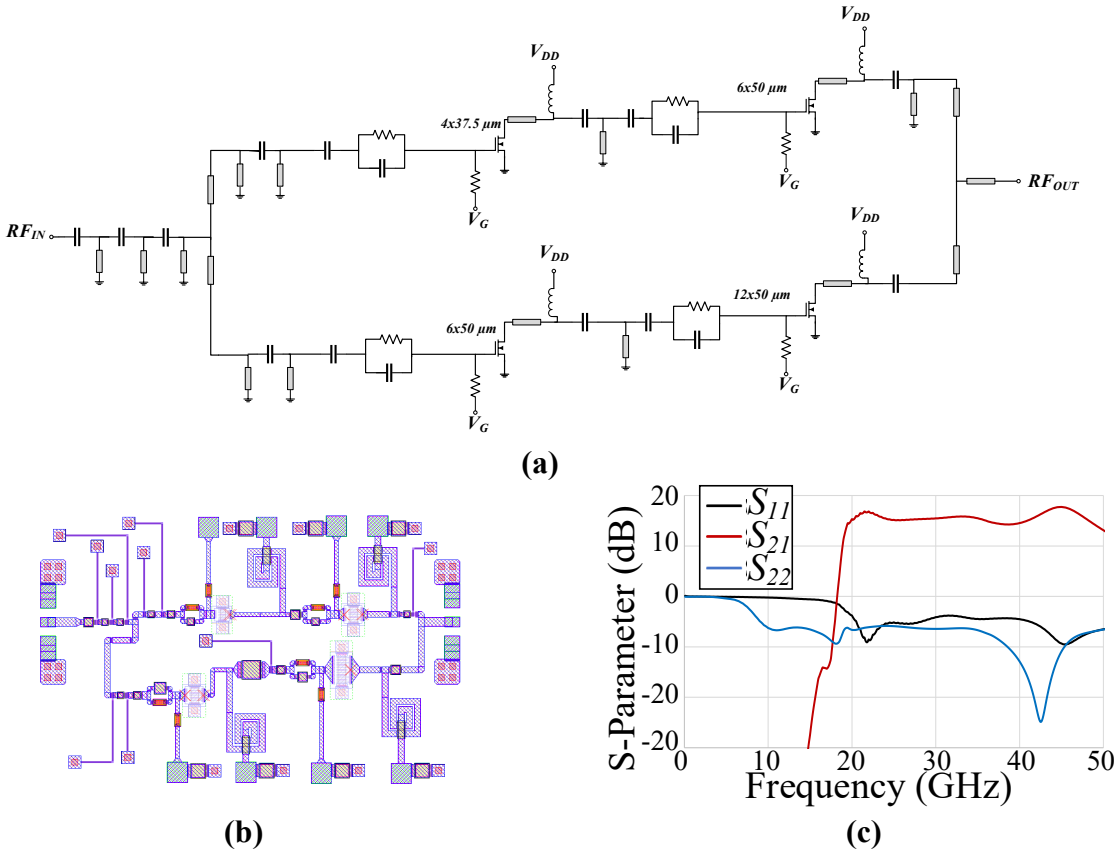


Figure 4.18: Simplified Schematics (a) and (b) the Layout of the Two-stage Asymmetrically Combined GaN PA (2.0 *x* 1.3 mm^2 with pads); and (c) its S-parameter EM PEX Simulation Results

EM simulations are run using AWR's AXIEM and the post-layout EM S-parameters are shown in Figure 4.18. The S-parameters simulations indicate that this PA achieves a 3-dB BW of 20 – 50 GHz with max. S_{21} of 17.2 dB with V_{DD} = 12 V.

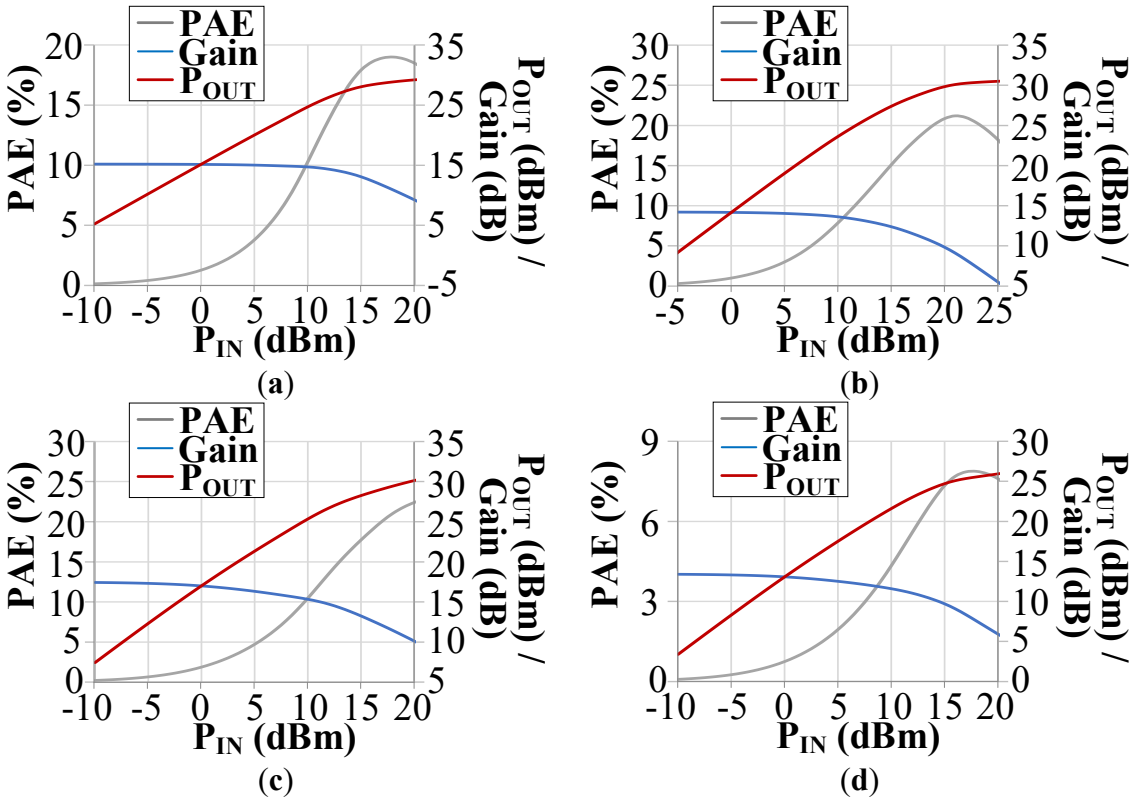


Figure 4.19: Post-layout EM P_{IN} vs PAE, P_{OUT}, Gain Simulations at (a) 20, (b) 38, (c) 44, and (d) 50 GHz of the Two-stage Asymmetrically Combined GaN PA

Using a 12 V supply, this PA achieves ~1 W of output power across the band and max. PAE of 24.2% at 38 GHz. Comparing to the one stage GaN PA designs from Section 4.1.1, the EM simulations of this PA achieves better gain and output power while also achieving comparable max. PAE using a 12 V supply. The large signal results are shown in Figure 4.19 and the BW performance is summarized in Table 4.6.

Table 4.6. Summary of EM PEX Simulations of the Two Stage Asymmetrically Combined PA

Freq. (GHz)	S_{11} (dB)	S_{21} (dB)	Max. PAE (%)	OP_{1dB} (dBm)	$P_{OUT,SAT}$ (dBm)
20	-8.8	15.1	19.0	17.0	29.5
38	-3.0	14.4	24.2	25.3	30.6
44	-3.8	15.2	23.0	20.5	31.0
50	-9.6	13.4	7.9	18.4	27.3

This work also designed a one-stage asymmetrically combined PA as shown in Fig. 4.20. This PA does not a require a higher-order input matching network as in the two-stage design. The post-layout PEX S-parameter simulations are shown in Fig. 4.20. This PA's 3-dB BW is ~18-50 GHz with maximum gain of 11.6 dB.

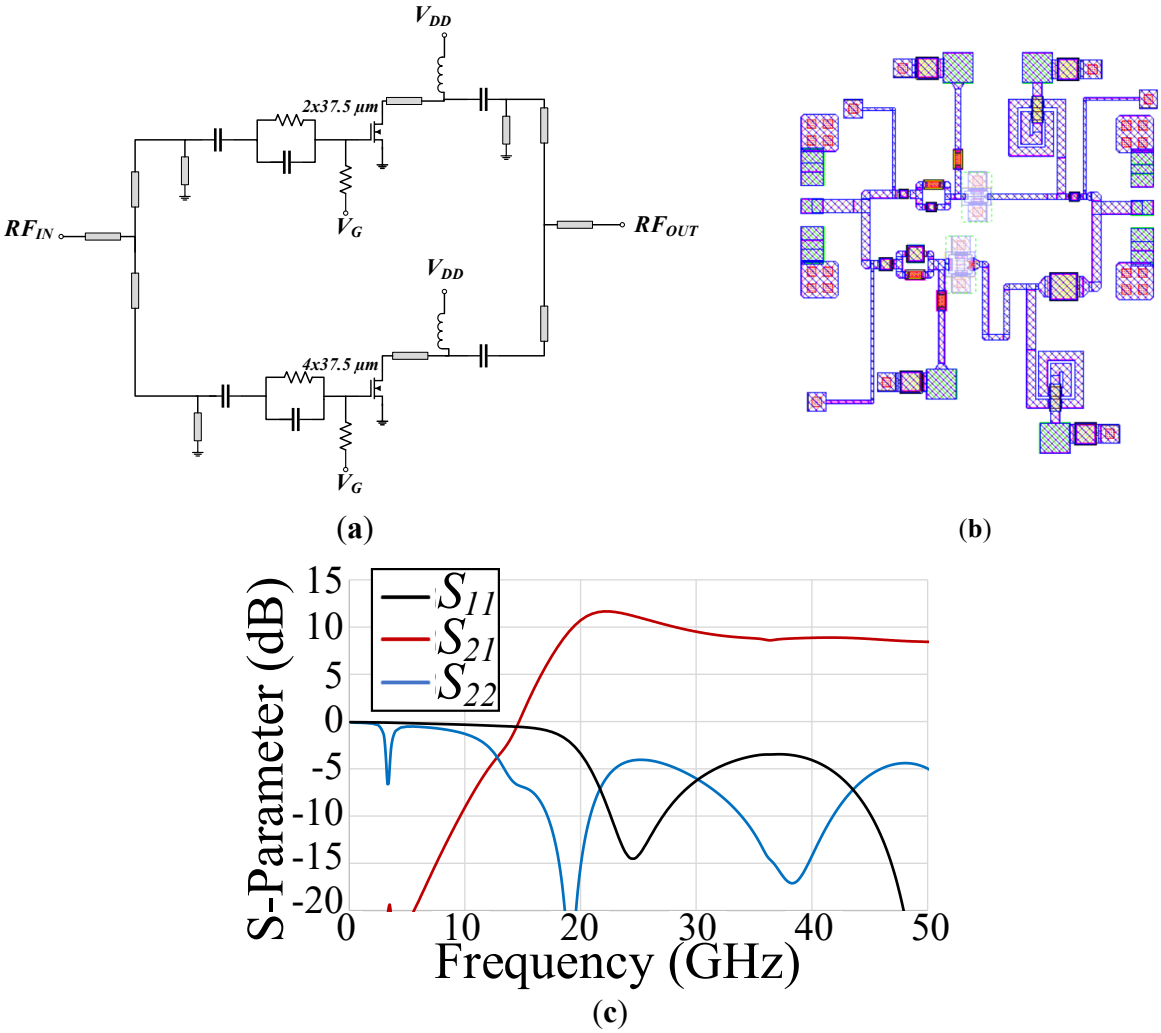


Figure 4.20: Simplified Schematics (a) and (b) the Layout of the One-stage Asymmetrically Combined GaN PA (1.1 *x* 1.3 mm^2 with pads); and (c) its S-parameter EM PEX Simulation Results

This PA achieves max. PAE of 27.6% at 20 GHz as shown in in Figure 4.21 with V_{DD} = 12 V. The broadband performance is summarized in Table 4.7. When comparing to the other one-stages presented in this chapter, this PA's gain is reduced, even with a large drain voltage; however, with the maximum $P_{OUT,SAT}$ is higher than the differential broadband versions that use RC feedback and a higher-order input matching network.

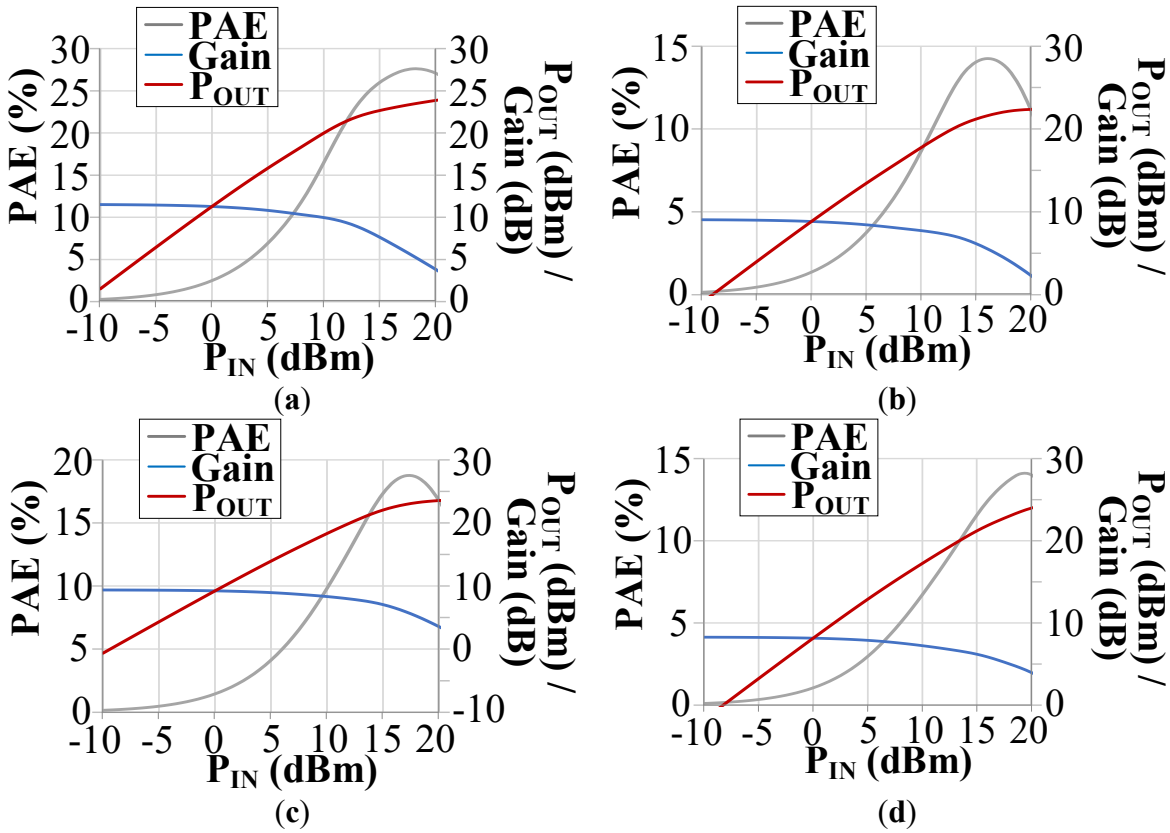


Figure 4.21: Post-layout EM P_{IN} vs PAE, P_{OUT}, Gain Simulations at 20, 38, 44, and 50 GHz of the One-stage Asymmetrically Combined GaN PA

Table 4.7. Summary of EM PEX Simulations of the One-stage Asymmetrically Combined PA

Freq. (GHz)	S_{11} (dB)	S_{21} (dB)	Max. PAE (%)	OP_{1dB} (dBm)	$P_{OUT,SAT}$ (dBm)
20	-3.5	11.6	27.6	17.5	24.5
38	-3.7	9.1	14.2	16.0	22.4
44	-7.3	9.4	18.7	18.3	23.7
50	-20.0	8.6	14.1	17.3	24.8

4.2.2 Broadband Two-Stage GaN Class J Pa

In Chapter 3, Class J operation was discussed, and a Class J PA is designed in this HRL technology. First, using device load-pull data on a 6 *x* 50 µm device, and the optimum load at 34 GHz was found to be 30 + j*35. Using the equations from Chapter 3 (Eq. (4.1) – (4.3)), the load impedances to achieve Class J operation were calculated to be 30 + j*30 at the fundamental frequency of 34 GHz, 0 – 35.3*j at second harmonic with value of 68 GHz and ~ 0 at the higher harmonics.

$$Z_{f_0} = R_L + j * R_L \qquad (4.1)$$

$$Z_{2f_0} = 0 - j * \frac{3}{8} * R_L \quad (4.2)$$

$$Z_{>2f_0} \quad (4.3)$$

Class J PAs operation does not have a large frequency dependence compared to other waveform shaping operations such as Class E, and therefore is able to be maintained broadband within a larger range of loads [41]. Figure 4.22 shows load achieved in the Class J GaN PA (schematic and layout shown in Figure 4.23), and it does achieve approximately the conditions calculated by Eq. (1) – (3) at f_o of 34 GHz (esp. Eq. 1, if R_L is 30 Ω).

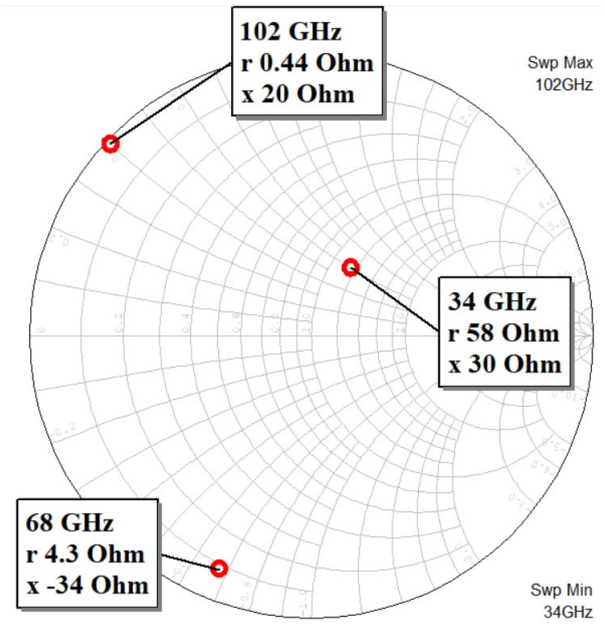


Figure 4.22: Load of the Second Stage Device of the Broadband Two-stage Class J GaN PA where f_o = 34 GHz, $2f_o$= 68 GHz, and $3f_o$= 102 GHz.

The S-parameter measurement vs. simulations is shown in Figure 4.23 and ignoring the spike at ~20 GHz due to mismatch, this design achieves 3-dB BW 19.6 – 35.6 GHz with max. S_{21} of 21.9 dB with V_{DD}= 6 V and 3-dB BW 19.6 – 36.0 GHz with max. S_{21} 22.6 dB of with V_{DD} = 12 V in measurement. With a lower supply voltage, the mismatch at ~20 GHz is much worse as the max. S_{22} with V_{DD} = 12 V is +4.6 dB and with V_{DD} = 6 V it is +8.8 dB. The S_{11} also becomes positive at ~30 – 35 GHz which is also exasperated with lowering the supply voltage, and this could damage to whatever is driving the PA, such a signal generator, a pre-amplifier, or a driver. Thus, care must be taken when taking measurements on this design, especially for large signal testing.

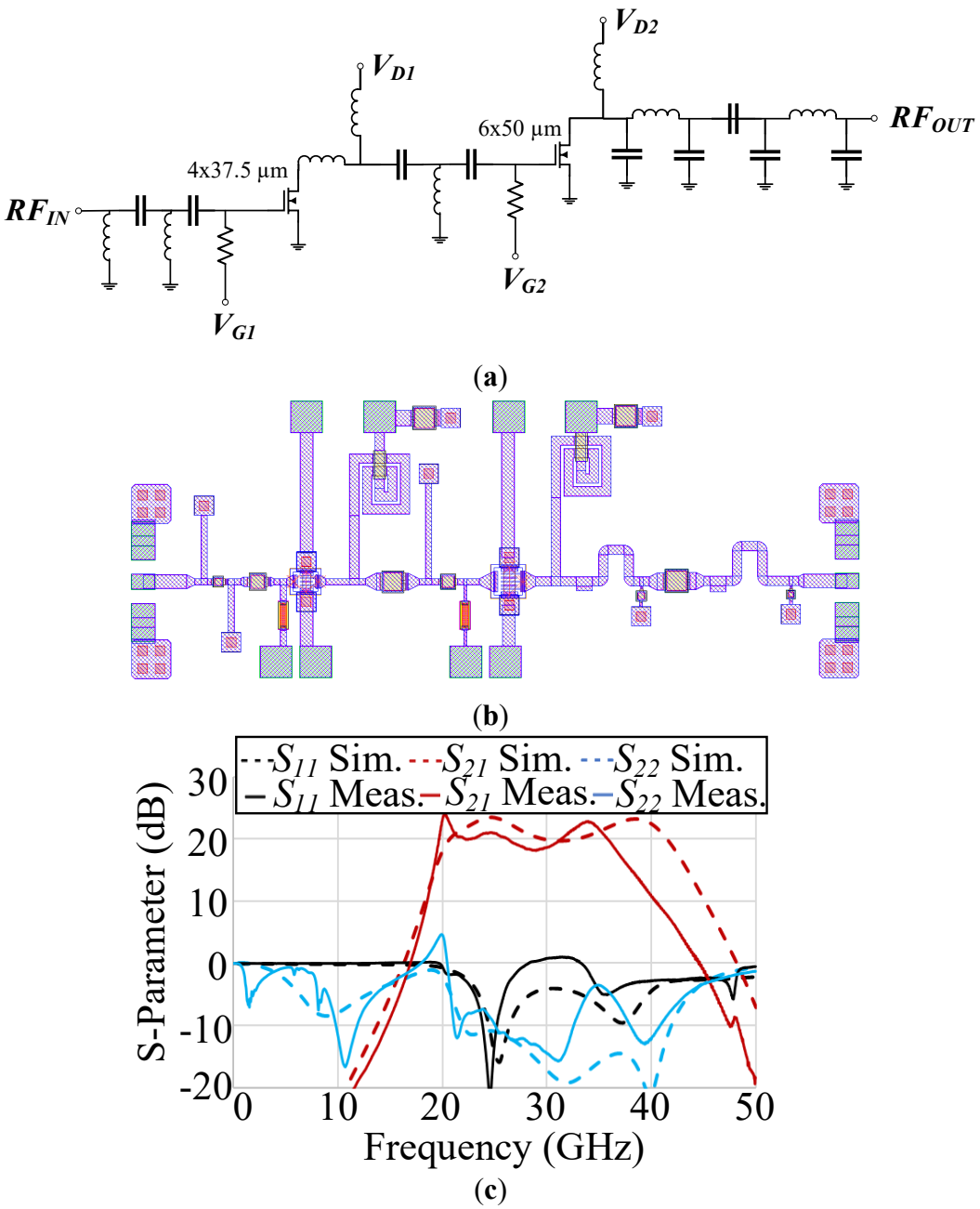


Figure 4.23: Simplified Schematics (a) and (b) the Layout of the Broadband Two-stage Class J GaN PA (2.3 *x* 0.9 mm^2 with pads); and its S-parameter EM PEX Simulation vs. Measurement Results for V_{DD}= (c) 4 V and (d) 6 V

Large signal measurements vs. simulations are shown in Figure 4.24 and Figure 4.25 at 22, 26 and 30 GHz. Although there are some issues with mismatch, this design is able to achieve max. PAE of 21.2%/ 21.8%/14.6%, $P_{OUT,\,SAT}$ of 22.2/ 22.4/ 19.6 dBm at 22/ 26 / 30 GHz with V_{DD}= 6 V and max. PAE of 14.2%/ 15.2%/8.5%, $P_{OUT,\,SAT}$ of 24.6/ 24.5/ 20.9 dBm with V_{DD}= 12 V. However, at a frequency of 30 GHz, this design was not driven far enough and thus probably

has higher PAE and output power than data presented here. Regardless, 30 GHz data is shown here to demonstrate the broadband nature of this design.

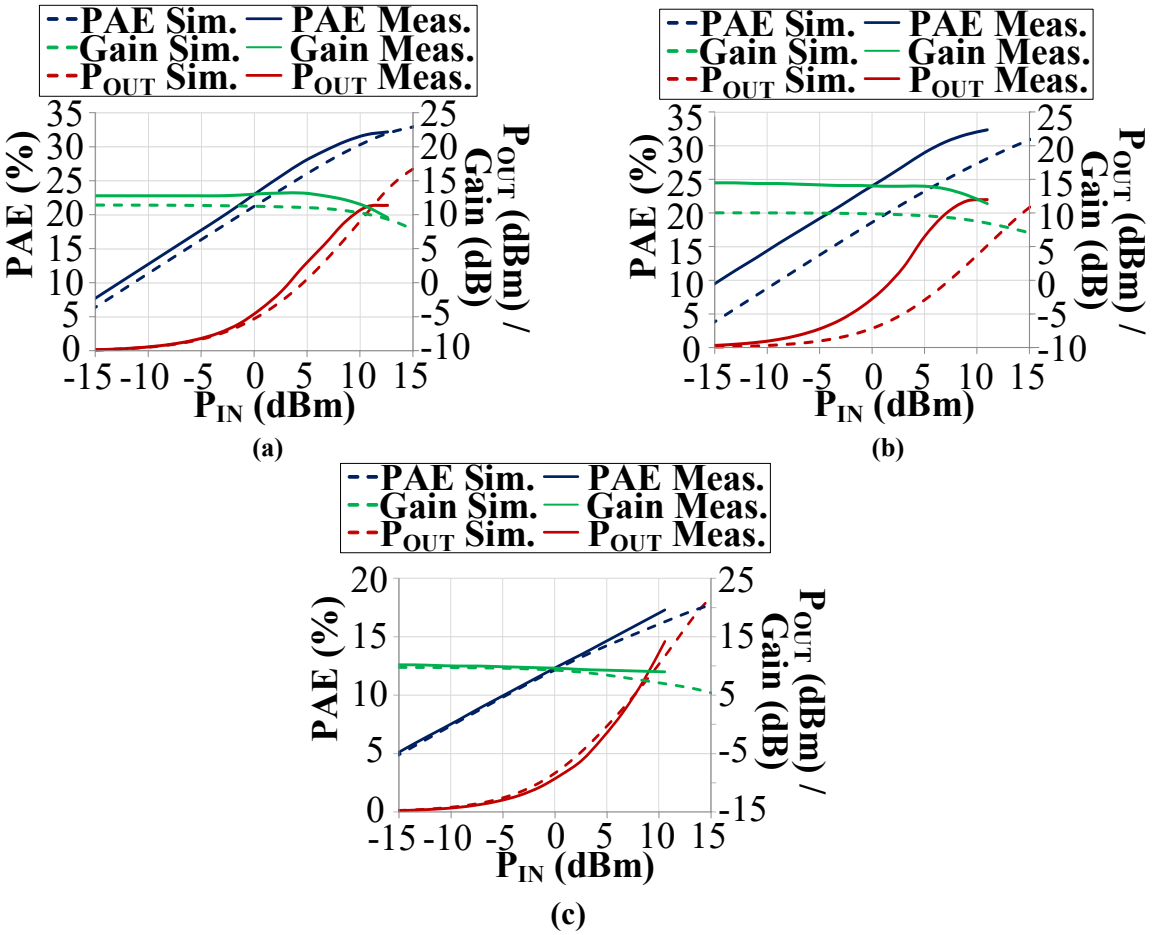


Figure 4.24: P_{IN} vs PAE, P_{OUT}, Gain Measurements vs. EM PEX Simulations of the Broadband Two-stage Class J GaN PA at (a) 22, (b) 26, and (c) 30 GHz with V_{DD} = 6 V

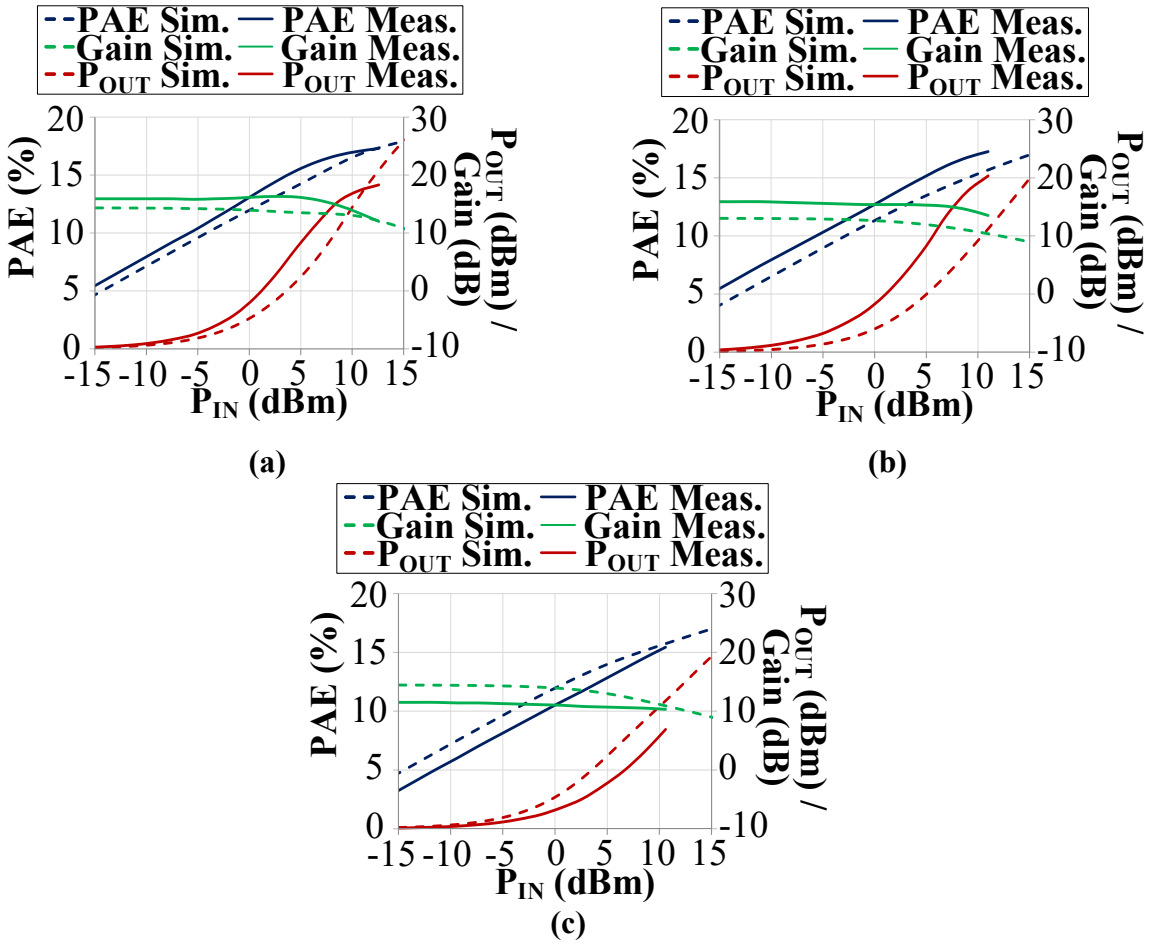
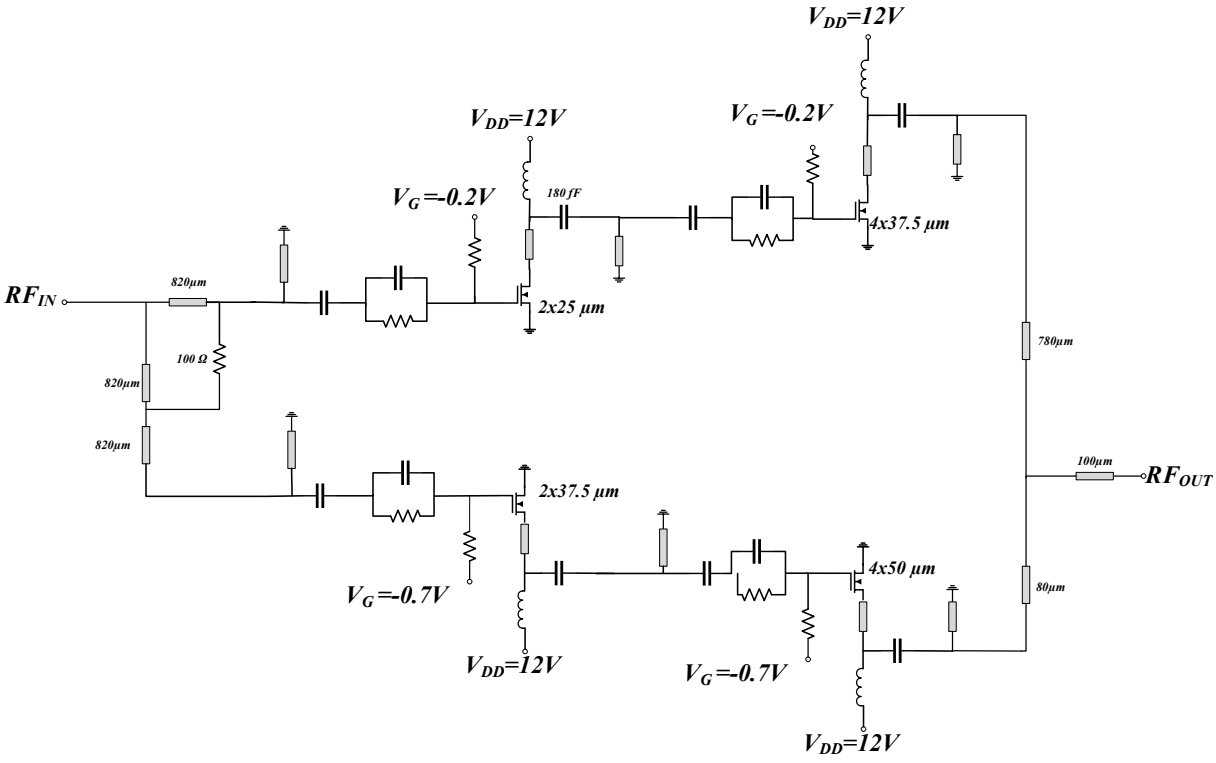


Figure 4.25: P_{IN} vs PAE, P_{OUT}, Gain Measurements vs. EM PEX Simulations of the Broadband Two-stage Class J GaN PA at (a) 22, (b) 26, and (c) 30 GHz with V_{DD} = 12 V

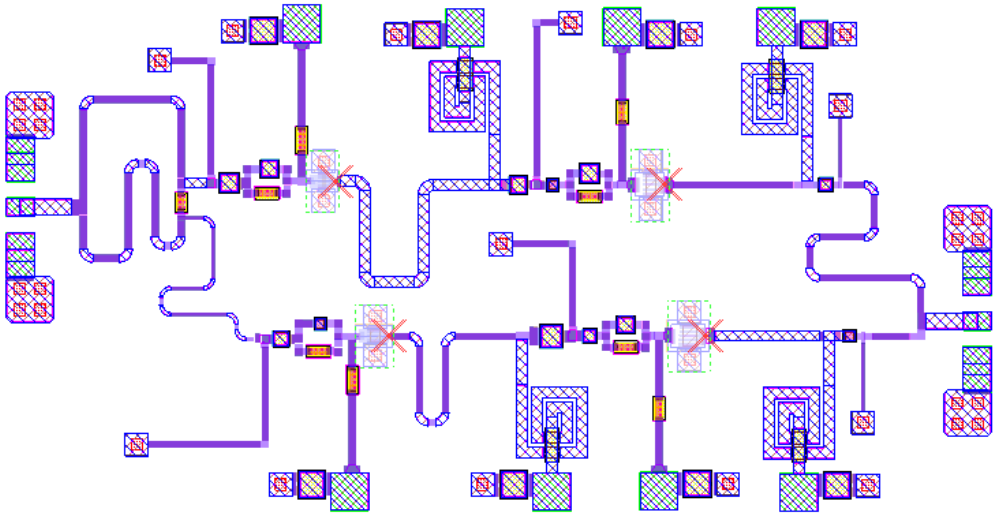
Although this PA has input/output mismatch issues, the measurement vs. simulation data agrees reasonably and shows promising results, so this design will be discussed in the Future Plans chapter later. This I/O mismatch issue has been investigated in simulation, and another Class J PA design has been retaped out and this work are currently waiting for the dies to come back to verify our updated design.

4.2.3 Narrowband Gan PA

Chapter 3 discussed the Doherty PA operation briefly and Figure 4.26 shows the schematic and layout of a narrowband 39 GHz two-stage Doherty GaN PA. This design uses the same classic Doherty architecture with a Wilkinson power divider at the input, and a λ/4 transmission line at the input of the of the auxiliary PA and at the output of the main PA [25]. Post layout EM simulations are done using Cadence's Axiem for this PA are shown in Figure 4.27 which indicate that this PA achieves S_{21} of 25.7 dB and S_{11} of -17.0 dB. The large signal EM PEX simulations (Figure 4.27) indicate that this PA achieves max. PAE of 28.1% with output power of 25.6 dBm and 18.4% PAE at 6-dB back-off.



(a)



(b)

Figure 4.26: Schematic (a) and (b) layout of the two-stage 39 GHz Doherty PA

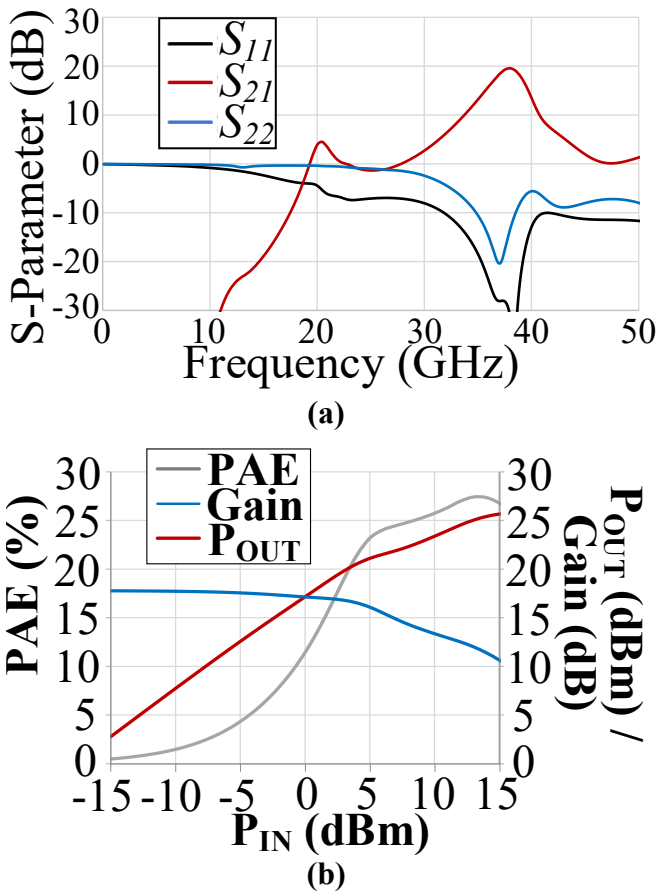


Figure 4.27: Post-Layout EM (a) S-parameter and (b) P_{IN} vs P_{OUT}, PAE and Gain Simulations of the Two-stage GaN 39 GHz Doherty PA

4.2.4 GaN Conclusion

Using HRL's advanced 40 nm GaN technology, several different BW enhancement techniques were investigated and compared. First, measurement data was successfully taken from a 3rd-order input matching network which achieved very broadband results with a 3-dB BW of 18 – 38.7 GHz with V_{DD} = 6 V as well as good measured max. PAE of ~40% at 28 GHz when V_{DD} = 4 V. Expanding upon these results, a differential version was designed and has just taped out. This version was able to attain higher gain, going from 12.5 dB to 13.3 dB with V_{DD} = 6 V in EM PEX simulations. With a $P_{OUT,SAT}$ of ~13.6 dBm, the differential version achieves ~3 dB higher $P_{OUT,SAT}$ and with similar PAE and BW results in EM PEX simulations. Another BW enhancement that was investigated was an RC feedback configuration. This technique in the single-ended version showed to have higher BW, with 3-dB of 17.2 – 50.4 GHz but with lower gain of 10.3 dB in EM PEX simulations. Adding the RC feedback also lowered the output power to a $P_{OUT,SAT}$ of ~20 dBm when compared to using a 3rd-order input matching network. A differential version of this PA was also designed with neutralization capacitors and it achieved similar BW in simulation. These designs also followed that the gain was able to be improved by making the design differential and adding neutralization capacitors as well as increasing the

$P_{OUT,SAT}$ by ~3-dB. All of these designs were designed to be in the medium-power range with $P_{OUT,SAT}$ less than a Watt, which typically is not done using mm-Wave GaN PA. For instance, the published work of the single-ended design using a 3rd-order input matching network was, to the best of our knowledge, the first published broadband GaN PA for mm-Wave 5G as shown in Figure 4.28. This shows the single-ended PA using a 3rd-order input matching work compared to other state-of-the-art GaN PAs and it shows that our power is much less than most GaN PAs while also maintaining competitive PAE across the band. Asymmetrically combined PAs were also investigated where Watt level $P_{OUT,SAT}$ was achieved in simulation. In addition, a narrowband design Doherty PA was designed to enhance PAE at power back-off. There is still work that can be done to improve on these PAs, and this will be discussed in Chapter 5.

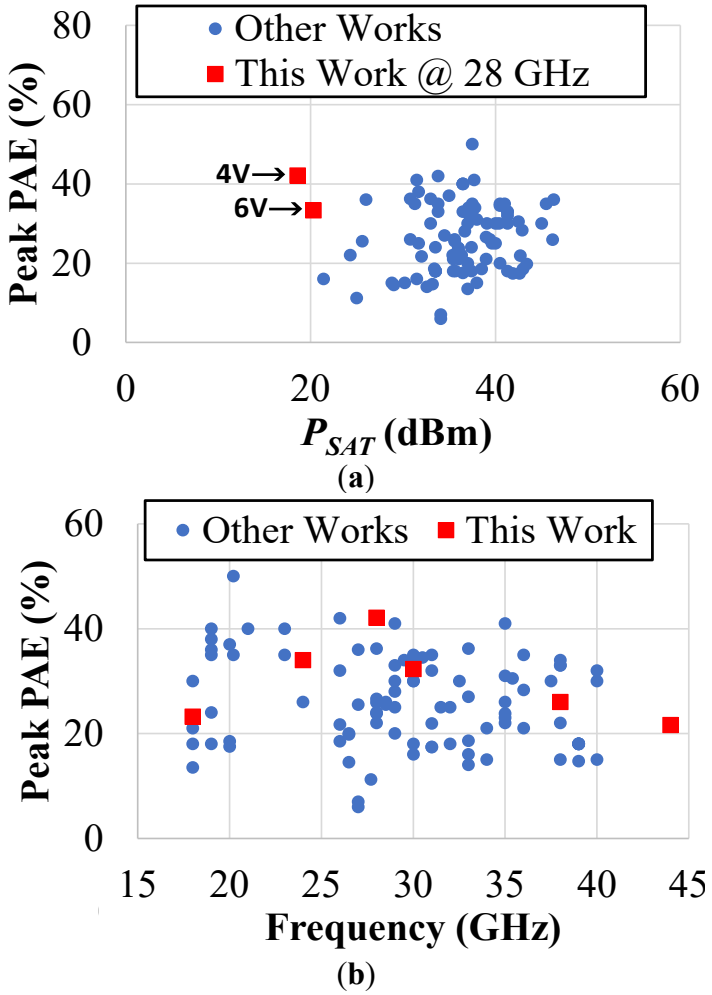


Figure 4.28: Comparison of Peak PAE vs $P_{OUT,SAT}$ with the Single-ended GaN PA using a 3rd-Order Input Matching Network Measured at 28 GHz (a) and (b) Peak PAE vs. Frequency with this Work Measured at V_{DD} = 4 V to Other State of the Art 18 – 44 GHz GaN PAs [59]

4.3 22FDX Results and Discussions

As what had been introduced in Chapter 2, the mm-Wave PA designs to be presented in this chapter use the GlobalFoundries' (GF) 22FDX technology, which is a 22 nm fully depleted silicon on insulator (FD-SOI) process. The designs throughout this chapter use SLVTNFETs (super low threshold voltage NFET), whose smallest device achieves a peak f_T / f_{MAX} ~350 GHz/~400 GHz. Using different body bias (V_B) applied to a 22 nm FD-SOI device, the current density versus f_T is plotted and this shows that body bias does not change the f_T at a given current density (Figure 4.39 (a)). Figure 4.39 (b) shows V_G vs. f_T curves, which indicates that for a fixed V_G, its f_T does increase with positive body bias V_B, which could be due to the fact that as V_B increases by 1 V, V_T reduces by ~80 mV, making the device turned on earlier. However, the peak f_T values do not change much for different V_B. Note that the V_G vs. f_T curves are flattened by a small amount, and this interesting effect could improve its linearity near the peak of the f_T where the curve is flattened more vs. V_G at larger V_B, as suggested by [18].

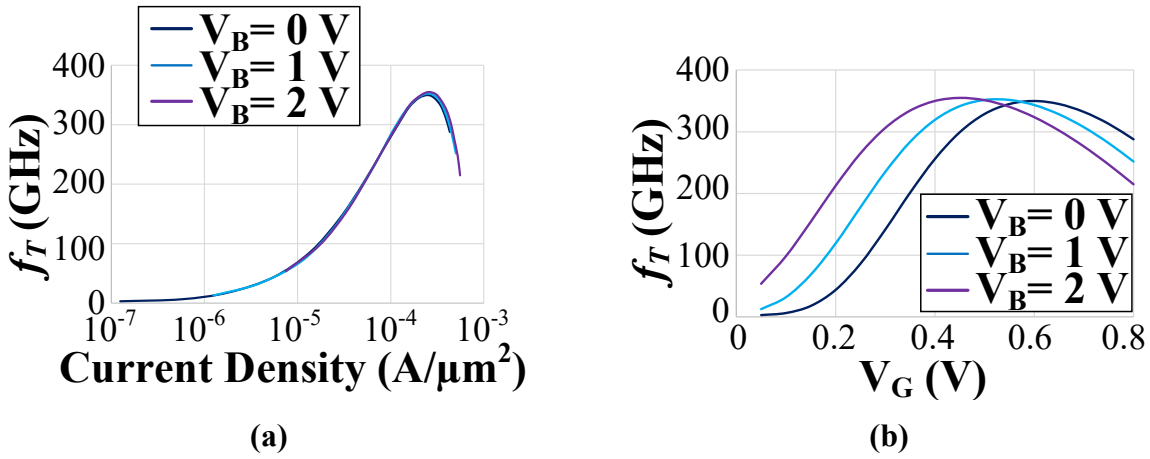


Figure 4.29: Current Density vs. f_T for a 16 x 0.5 µm *x* 0.02 µm 22 nm SOI SLVTNFET Device (a); (b) Gate Overdrive Voltage V_G vs. f_T at Several V_B.

4.3.1 28 GHz Narrowband 22FDX PA

In this section, this work will show a narrowband 28 GHz two-stage differential PA (Figure 4.40) that uses neutralization capacitors to improve max. stable gain and reverse isolation. Also, this design makes use of on-chip baluns for input/output (I/O) and interstage matching that the PDK nicely provides. Simulations are run on the two types of baluns, interleaved and stacked baluns, that are offered from this PDK and an interleaved balun is chosen. Two external capacitors are added to the output of the balun to improve amplitude imbalance, achieving a loss of -4.7/-5.9 dB at 28 GHz. The first stage is a common source (CS) PA, and the second stage is in a two-stacked configuration. All SPICE simulation data presented in this chapter has been obtained with post-layout extraction (P4.EX) using the Calibre xACT extraction tool, using R+C+CC extraction rather than with EM (electromagnetic) simulations as these are much more time-consuming [59]. However, this work have compared the measurement data vs. PEX simulation data using both Caibre xACT and EM simulations in ADS Momentum, and the

Calibre xACT PEX simulated data turns out to be closer to measurement (data not shown) for the fixed bias PAs in this chapter. The layout of this PA is 750 µm *x* 360 µm, with the core area of only 500 µm *x* 150 µm (without pads). The device size is 150 µm with a C_{gd} of 46.7 fF and C_{gs} of 81.3 fF at 28 GHz. Using the Eq. 1.4 from Chapter 3, the neutralization capacitors would theoretically be 81.3 fF to completely neutralize this parasitic capacitance at 28 GHz; however, the Eq. 1.4 is an oversimplified model by ignoring other device parasitics in the small-signal equivalent circuit model. Eventually a smaller value of 40 fF is chosen to be the optimum value of neutralization capacitor used in this design according to PEX simulations.

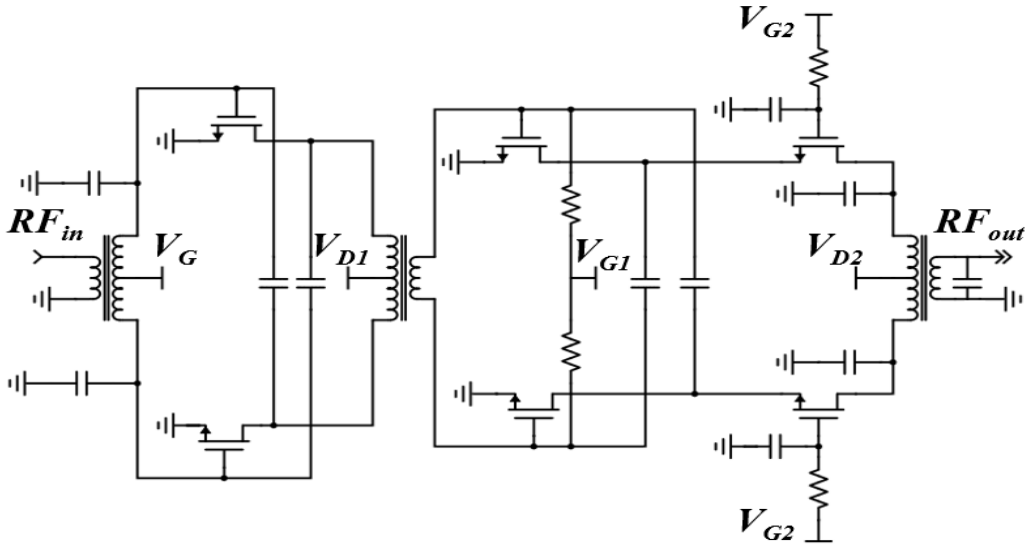


Figure 4.30: Schematic of the Two-stage Narrowband 28 GHz CMOS SOI PA Design

Similarly, this work can find the stacked gate capacitor value of 50.9 fF from the equation in Chapter 3 (Eq. 3.5) using C_{gs} and the optimum load value of ~ 90 Ω derived from load-pull simulations. However, after looking at transient waveforms, a value of 160 fF capacitor is used for the stacked transistor. As what was discussed in Chapter 3, the stacked design should split the V_{DD} equally across the devices, and the waveforms are supposed to be in phase. Figure 4.21 shows the drain voltage waveforms with respect to ground for each device for the stacked second stage of this PA, where V_{D2} is the drain voltage of the stacked top device and V_{D1} is the voltage at the drain of the bottom CS device. This shows that the voltage is well split across the two devices with the maximum voltage on the top drain equal to 3.4 V, while the voltage at the bottom device's drain is equal to 1.7 V and they are close in phase. Thus, the maximum V_{DS2} (i.e., the drain to source voltage of the top stacked device) is equal to 1.7 V, and the maximum output voltage swing is equally spread across both devices, enabling higher output V_{DD} and P_{OUT}, with mitigated breakdown constraints.

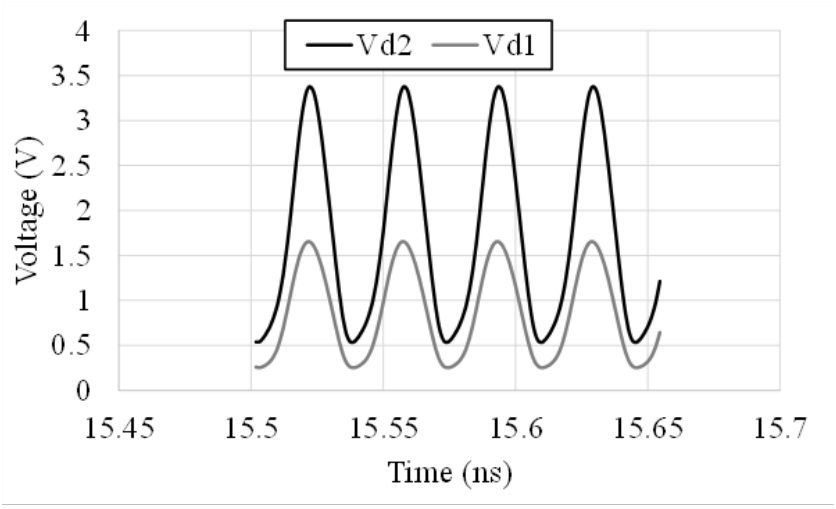


Figure 4.31: Simulated Drain Voltage Waveforms of the First and Second Drain of the Stacked FETs in the Second Stage of the Narrowband Two-stage 28 GHz Stacked PA

Figure 4.32 shows the S-parameters and the large-signal simulation at 28 GHz data of this design. The PA achieves high maximum small signal gain of 27.4 dB at ~26 GHz with good stability in PEX simulation. The body nodes of the CS devices of the second stage are tied together and biased at V_B = 0 V and 1 V when V_G (i.e., the voltage at the gate of the device of the CS first stage) = 0.4 V, V_{G1} (i.e., the voltage at the gate of the CS device of the second stage) = 0.4 V and V_{G2} (i.e., the voltage at the gate of the stacked device of the second stage) = 1.4 V. PEX simulations indicate that the gain rises by ~1.5 dB with increased V_B to 1 V, and OP_{1dB} from 13.0 dBm to 14.5 dBm; however, PAE is not affected much as V_B increases. This is to be expected since increasing V_B reduces V_T by ~ 80 mV as shown in Figure 4.19, increasing the gain and P_{OUT}. This narrowband PA may serve as a good starting point for us to add additional complexity and reconfigurability to achieve broadband operation as discussed in subsequent designs.

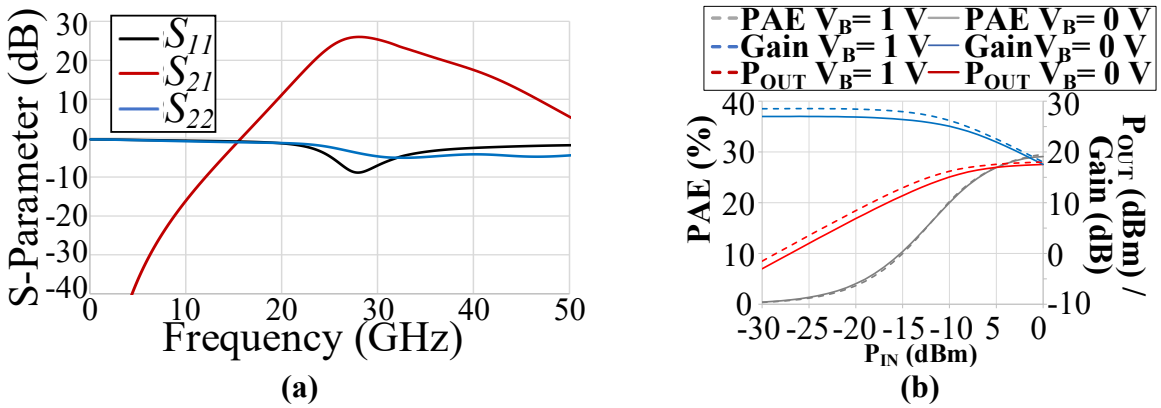


Figure 4.32: Post-layout PEX simulated data of the two-stage narrowband CMOS SOI 28 GHz PA for (a) S-parameters; and (b) large signal performance with V_G = 0.4 V (first stage); and V_{G1} = 0.4 V (CS of the second stage), $V_{G2} = V_{G1}$ + 1 V (stacked device of the second stage), V_B = 0 or 1 V for the CS devices of the second stage.

4.3.1.1 Reconfigurable 28 GHz Narrowband 22 FDX PA

Next, reconfigurability is investigated by including digitally controlled switches for fine tuning of the neutralization capacitors, I/O and interstage matching as shown in the schematics of the reconfigurable two-stage 22 nm CMOS SOI PA (Figure 4.33). The amount of feedback in the PA can be optimized for a certain frequency with the digitally controlled neutralization capacitors, where each stage of the PA includes two pairs of these switches. Each switch is tied to a complementary switch to ensure that there is equal neutralization from one side to the other. To turn off a neutralization path, the series switches are turned off, which is facilitated by adding resistors that are shunted to ground through a third switch to establish ~0 V on each side of the capacitor. When activating a neutralization path, series switches are turned on and the third switch is open. The reconfigurability has 8 different states since the two different switches for each neutralization capacitor are considered to be equal. The body nodes of the bottom device of the second stage are tied together as one bias node, and the body nodes of the first stage devices are also tied together as another bias node, and thus there are two different body bias nodes and four different states.

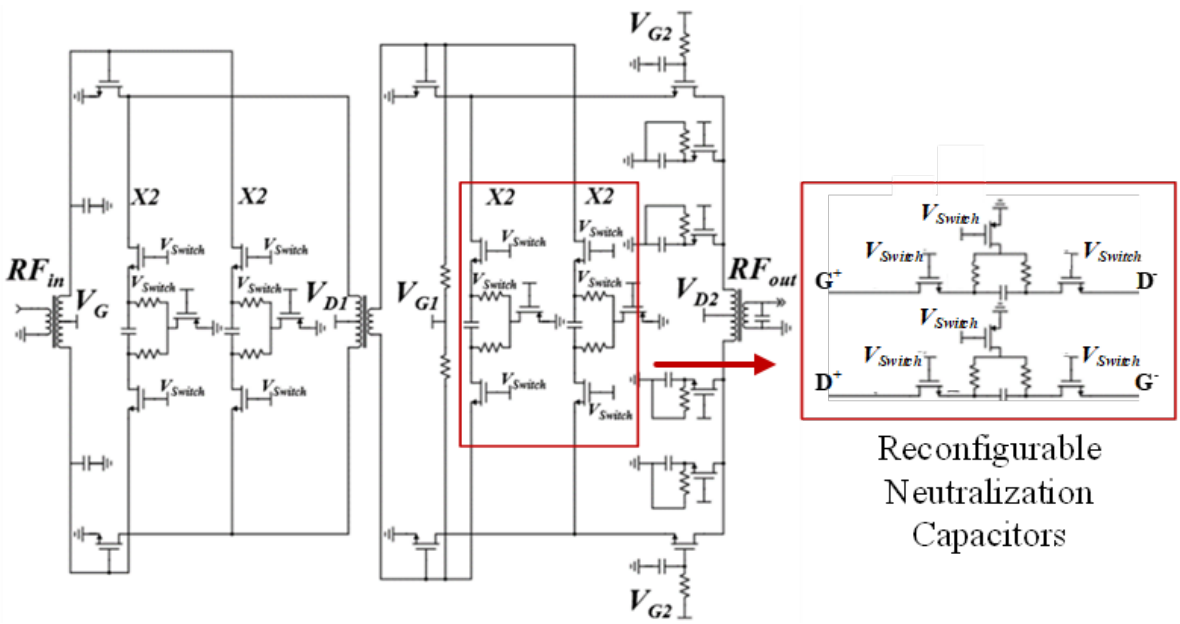
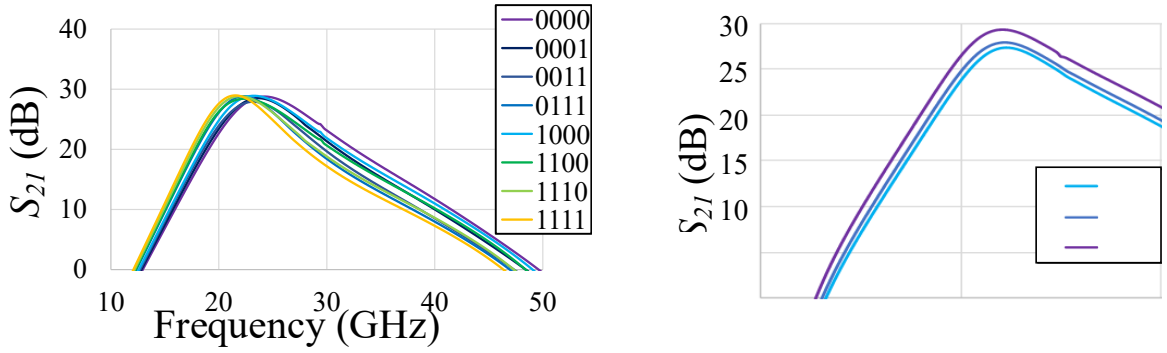


Figure 4.33: Schematic of the Two-stage Reconfigurable CMOS SOI PA with the Reconfigurable Neutralization Capacitors Highlighted

For the digitally controlled neutralization capacitors, there are 8 different states, where the first two bits are the ON/OFF states for neutralization capacitors on the first stage, and the last two bits are for neutralization capacitors for the second stage. Here a state of "01" is the same as "10" since the neutralization capacitor pairs are considered to be equal. Figure 4.34 shows the PEX simulations of the reconfigurable PA, which indicate that the max. S_{21} can now be controlled from ~24 GHz (case 0000; all switches *OFF*) to ~21 GHz (case 1111; all switches *ON*) by digitally controlling the neutralization capacitors. Also, this work can adjust S_{21} by 6 dB at 28 GHz by using these different states (see Figure 4.24 (a)), when the body bias of both stages is kept at 0 V. With all the digitally controlled neutralization capacitors in the OFF state, the body bias can enable ~4 dB S_{21} tuning, as shown in Figure 4.34 (b) where stage 1/2, V_B = 0/0 V, 0/1 V, and 1/1 V (the first digit is the voltage to the body nodes of the first stage, and the second digit is the voltage to the body nodes of the CS devices of the second stage).



(a) **(b)**

Figure 4.34: Post-layout PEX Simulations of the Reconfigurable PA on: (a) S_{21} under different ON/OFF Conditions of the Neutralization Capacitors; and (b) S_{21} vs. body bias V_B of the CS Devices on the First and Second Stage of the two-stage Reconfigurable CMOS SOI PA

PAE@P_{1dB}, max. PAE, gain, OP_{1dB} and $P_{OUT,\,SAT}$ as a function of V_{G1} of the bottom CS device on the second stage of the PA are plotted in Figure 4.35 (a) (note the gate bias of the stacked FET, or V_{G2}, is equal to V_{G1} + 1 V). Here the effect of the gate biasing of the second stage PA is shown, where the value of the max. PAE and PAE@P_{1dB} are close in value at V_{G1} = ~0.3 V, suggesting a linear and efficient class-AB biasing point. Thus, V_{G1} = 0.3 V can be chosen to be the biasing point at power back-off for high average PAE vs. Class-A bias for large PAPR (peak-to-average-power-ratio) input signals, if linearity is acceptable.

Next, Figure 4.35 (b) shows the effect of the body bias at lower V_{G1} = 0.3 V (V_{G2} = 1.3 V), which is close to the SLVTNFET's threshold voltage V_T. PEX simulated cascaded max. PAE, PAE@P_{1dB}, large signal gain, OP_{1dB} and $P_{OUT,\,SAT}$ as a function of body bias V_B of the second stage CS FET is plotted, showing the gain to increases by 2 dB when V_B is increased from 0 V to 1 V, most likely due to the lowering of V_T by ~ 80 mV. When V_{G1} = 0.5 V (and V_{G2} = 1.5 V), the devices are biased closer to Class A operation as shown in Figure 4.35 (c), and thus V_B increasing by 1 V has little effect on gain.

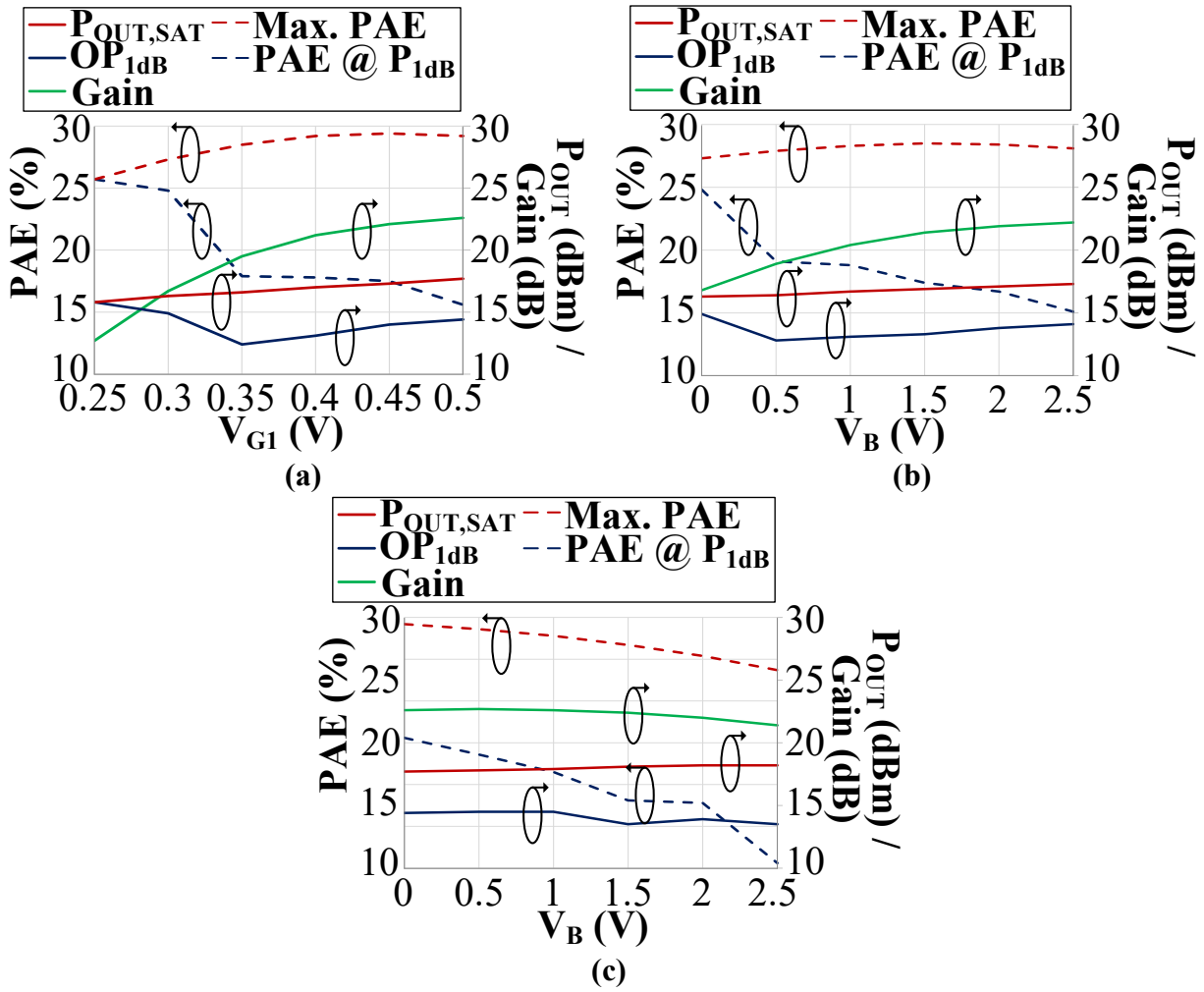


Figure 4.35: Post-layout PEX Simulations of the Two-stage CMOS PA where PAE@ P_{1dB}, max. PAE, gain, OP_{1dB} and $P_{OUT,SAT}$ as a Function of (a) V_{G1} of the bottom CS Device on the Second Stage of the PA (with V_B = 0 V); (b) body bias V_B of the Second Stage with V_{G1} = 0.3V; and (c) body bias V_B of the Second Stage with V_{G1}=0.5V

Figure 4.36 shows the effect of the gate bias V_{G1}, (with V_B of the second stage = 0 V), on the cascaded two-stage PA's linearity, namely on its AM-AM (amplitude to amplitude modulation) and AM-PM (amplitude to phase modulation). As expected, when V_{G1} decreases from 0.5 V to 0.25 V (i.e., going from Class-A towards Class-B operation), linearity degrades, and this can be seen by the AM-PM phase change $\Delta\Phi@P_{1dB}$ increasing by ~15°. It is interesting that $\Delta\Phi@P_{1dB}$ can be close to 0° at V_{G1} = 0.35V, suggesting good AM-PM linearity at this bias point.

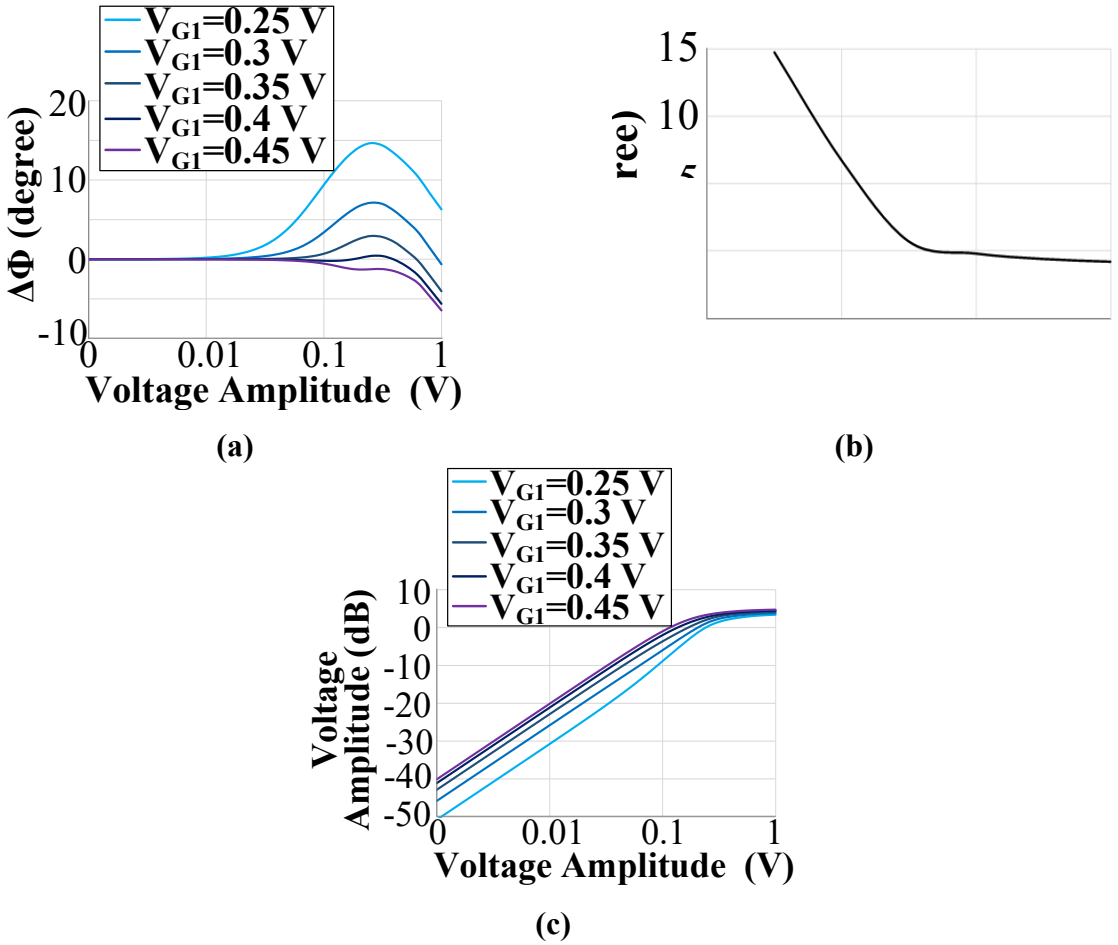


Figure 4.36: Post-layout PEX Simulations of the Two-stage PA on its (a) AM-PM, (b) the Phase Change ΔΦ@P_{1dB} vs. V_{G1} and (c) AM-AM, with V_B of the Second Stage = 0 V

Next, the effect of the body bias on linearity is investigated in Figure 4.37, which shows the effects of V_B tuning of the second stage CS FETs on its AM-PM distortion when V_{G1} = 0.3 V. It is interesting that the AM-PM nonlinearity can be reduced from ~6.6° to 0.1° when increasing V_B from 0 V to 1 V, and thus the body bias V_B tuning can be rather attractive for PA linearity enhancement. In addition, there is a slight improvement of the AM distortion at higher V_B in AM-AM simulations, due to the PA going closer into Class A operation. Large signal simulations indicates when V_B = 1 V and V_{G1} =0.3 V, this PA achieves OP_{1dB} of 13.1 dBm, PAE@P_{1dB} of 18.8%, max. PAE of 28.3% and 20.4 dB gain.

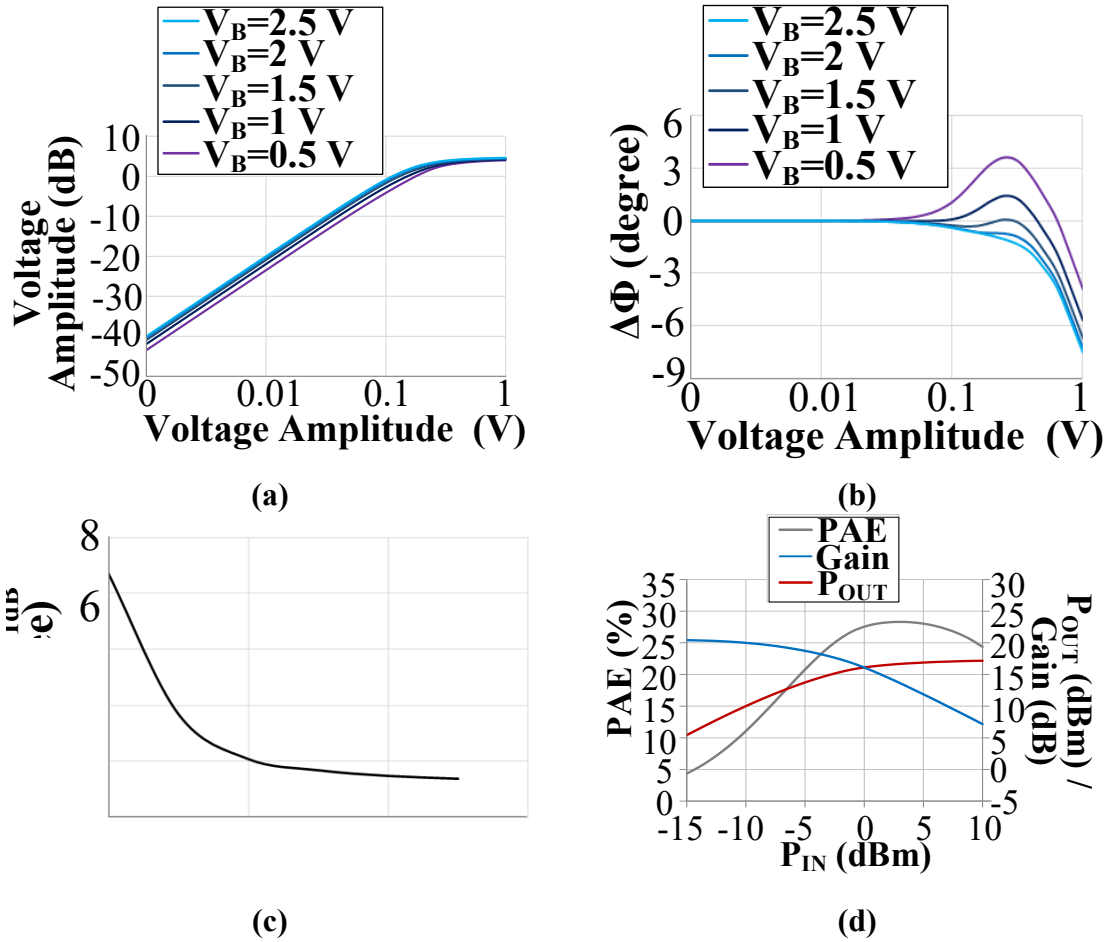


Figure 4.37: Post-layout PEX Simulations with V_{G1} = 0.3V for (a) AM-AM; (b) AM-PM both at Different V_B of the CS device of the Second Stage; (c) ΔΦ@P_{1dB} vs. V_B; and (d) P_{IN} vs. PAE, Gain and P_{OUT} at V_B =1 V.

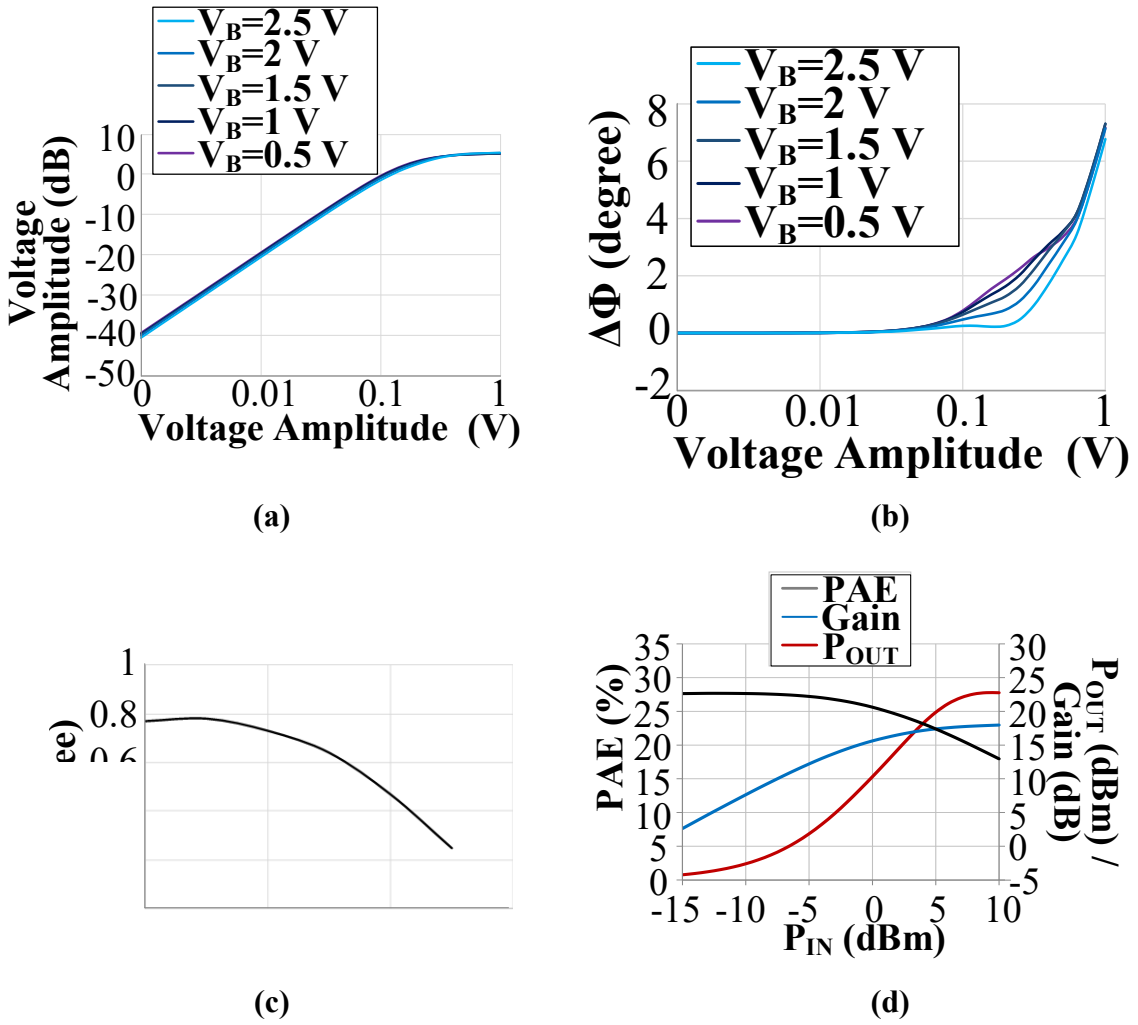


Figure 4.38: Post-layout PEX Simulations with V_{G1} = 0.5 V of (a) AM-AM; (b) AM-PM Both at Different V_B of the CS Device of the Second Stage; (c) ΔΦ@P_{1dB} vs. V_B; and (d) P_{IN} vs. PAE, Gain and P_{OUT} at V_B =0 V

With higher gate bias voltages (e.g., V_{G1} = 0.5 V and V_{G2} = 1.5 V), the body bias does not have much of an effect on the second stage of the PA's linearity as indicated in Figure 4.38. Here there is only a maximum phase change ΔΦ@P_{1dB} of ~ 0.8°, which is due to the PA is already being linear with its Class-A biasing. As V_B increases from 0 to 2.5 V, there is thus just ~0.6° of reduction of AM-PM nonlinearities, and there is not much change in the AM-AM distortion from this V_B tuning. The large signal PEX simulation for when this PA is biased in Class A mode at V_B = 0 V achieves a gain of 22.6 dB, OP_{1dB} of 14.4 dBm, max. PAE of 29.2% and PAE@P_{1dB} of 15.5%.

In this section, the effects of the gate bias and body bias of the second stage FETs on the PA's overall linearity and PAE were investigated. Based on post-layout simulations, the data indicates that V_B can improve PA linearity by tuning the AM-PM distortion to be close to 0° at P_{1dB} when

biasing at a Class-AB mode to improve the average PAE. In addition, being able to effectively tune the gain with V_B is attractive for improving the yield for nm-CMOS by alleviating V_T variation due to poly CD and short-channel effects.

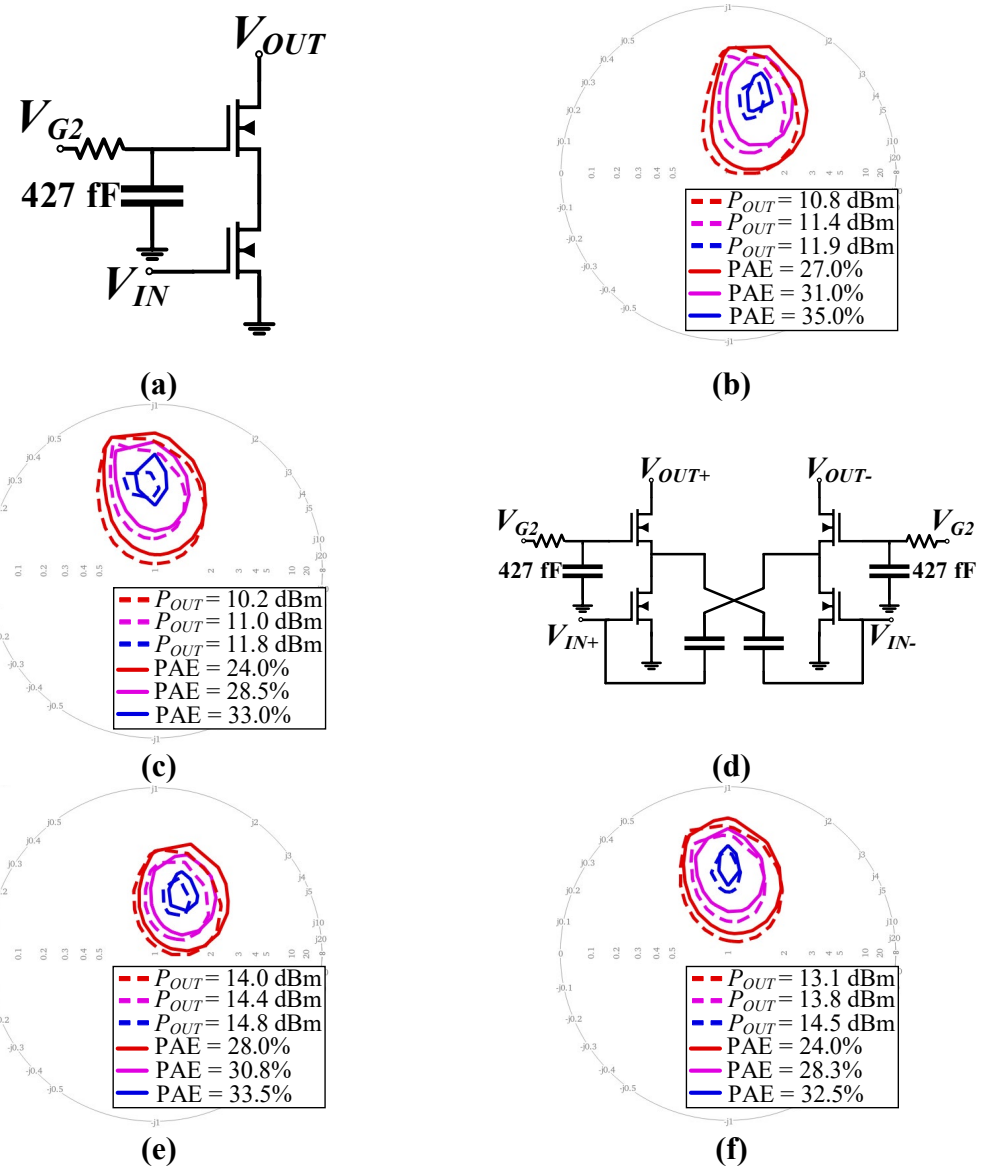


Figure 4.39: Load-pull Simulations

Single-ended cascode device pair (with a 427 fF capacitor on the cascode gate)(a) at (b) 24 GHz and (c) 37 GHz; and of the (d) differential cascode device pair with neutralization capacitors at (e) 24 GHz and (f) 37 GHz all at around OP_{1dB}.

4.3.2 Broadband CMOS FD-SOI PA Design

In this section, this work use two of the broadband PA design techniques introduced in Chapter 3 to realize broadband CMOS PAs: i.e., RC feedback and a higher-order matching network. In

addition, for these broadband PA designs this work also used a quasi-cascode topology, where the gate capacitor on the cascode FET is of a size that is neither large enough for the gate to have an excellent RF ground (i.e., a classic cascode device), nor small for a classic stacked PA design. Thus, this broadband design is of a "hybrid-cascode/stack" topology, as it is between a cascode and a stack PA topology. For the broadband PA designs, a smaller device size of 2 *x* 20 µm is used. These devices have a C_{gd} of 6 fF but a neutralization capacitor of 22 fF is used. Using this smaller device size, PAE and P_{OUT} load-pull simulations are performed in Cadence Spectre. First, these simulations are done on a single-ended "hybrid-cascode/stack" device pair with parasitics extracted up to the top metal layer as shown in the schematic in Figure 4.39 (a). These simulations are performed at around OP_{1dB} and indicate that at 24/37 GHz, the hybrid-cascode/stack device pair can achieve max. PAE of 35.0%/33.0% and $P_{OUT,MAX}$ of 11.9/11.8 dBm, respectively. Load-pull simulations are then also done on a *differential* hybrid-cascode/stack device pair with small neutralization capacitors (see Figure 4.39 (d)), and they achieve max. PAE and $P_{OUT,MAX}$ values of 33.5%/32.5% and 14.8/14.5 dBm at 24/37 GHz, respectively (still at around P_{1dB}). The optimal load impedance of max. PAE and $P_{OUT,MAX}$ can occur close to each other on the Smith Chart as indicated by the load-pull simulations, and thus these devices can almost be simultaneously optimized for both PAE and output power. Additionally, load-pull simulations suggest that these devices could achieve broadband performance as the optimal load does not move much when the frequency is changed from 24 to 37 GHz. Both topologies may also benefit from low devices mismatches, as reported by GF [61].

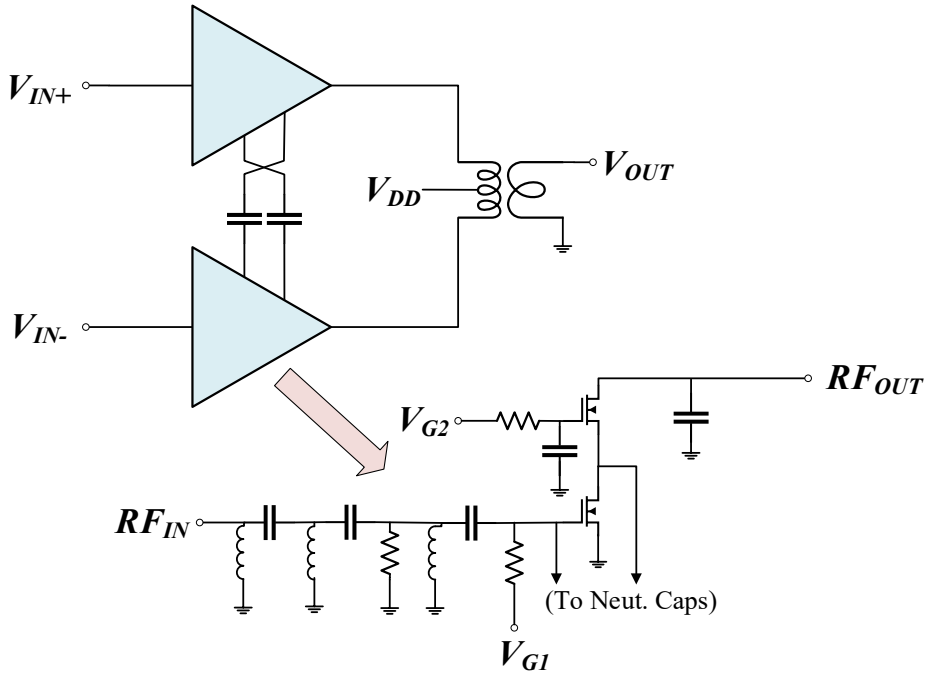
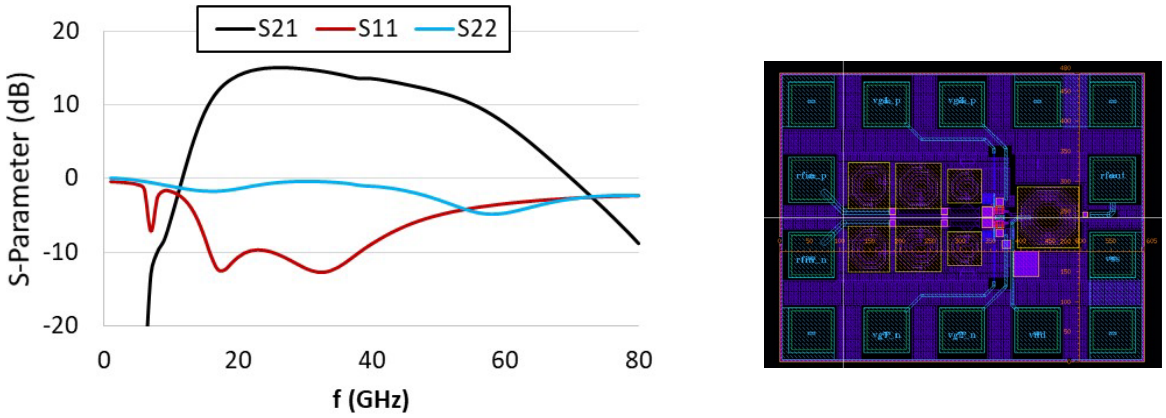


Figure 4.40: Schematic of Broadband Differential 22 nm FDSOI PA with a 3rd-Order Input Matching Network

4.3.2.1 Broadband CMOS SOI PA Using a 3RD-Order Input Matching Network

First, a broadband differential PA that utilizes a 3rd-order input matching network to broaden the BW was designed and investigated. Although this design was designed by another student, it is shown here as comparison against the broadband PA that utilizes RC feedback, which will presented next. Figure 4.40 shows the schematic of the differential broadband hybrid-cascode/stack CMOS-SOI PA design that utilizes a 3rd-order input matching network and neutralization capacitors. This integrated PA design includes an on-chip output balun from the GF PDK for output matching, to feed the V_{DD}, and to go from a differential input to a single-ended output. The small-signal 3-dB bandwidth of this design extends from 17 GHz to 49 GHz (absolute BW = $2(\frac{f_H - f_L}{f_H + f_L})$ =86.7%) with a max. S_{21} gain of 15.0 dB. This design also maintains S_{11} less than -5.0 dB across ~20 – 50 GHz as shown in Figure 4.41.



(a) **(b)**

Figure 4.41: Post-layout S-parameter Simulations of Broadband CMOS-SOI PA with 3rd-order Input Matching Network

Figure 4.42: shows the large signal simulations for this 3rd-order input matching broadband PA design, and it achieves a high simulated max. PAE of 36.6% at 20 GHz. This design also achieves max. PAE above 21% across 20 – 40 GHz (detailed numbers are listed in Table 4.8).

Table 4.8. Summary of Post-Layout Simulations for the 3rd-Order Input Matching Broadband 22FDX PA

Freq (GHz)	S_{21} (dB)	S_{11} (dB)	Max PAE (%)	$P_{OUT,\,SAT}$ (dBm)	OP_{1dB} (dBm)
20	13.9	-10.7	36.6	18.1	16.4
30	14.8	-12.1	28.4	17.1	14.9
40	13.5	-9.5	21.2	16.2	12.1
50	11.7	-5.0	13.1	14.5	9.9

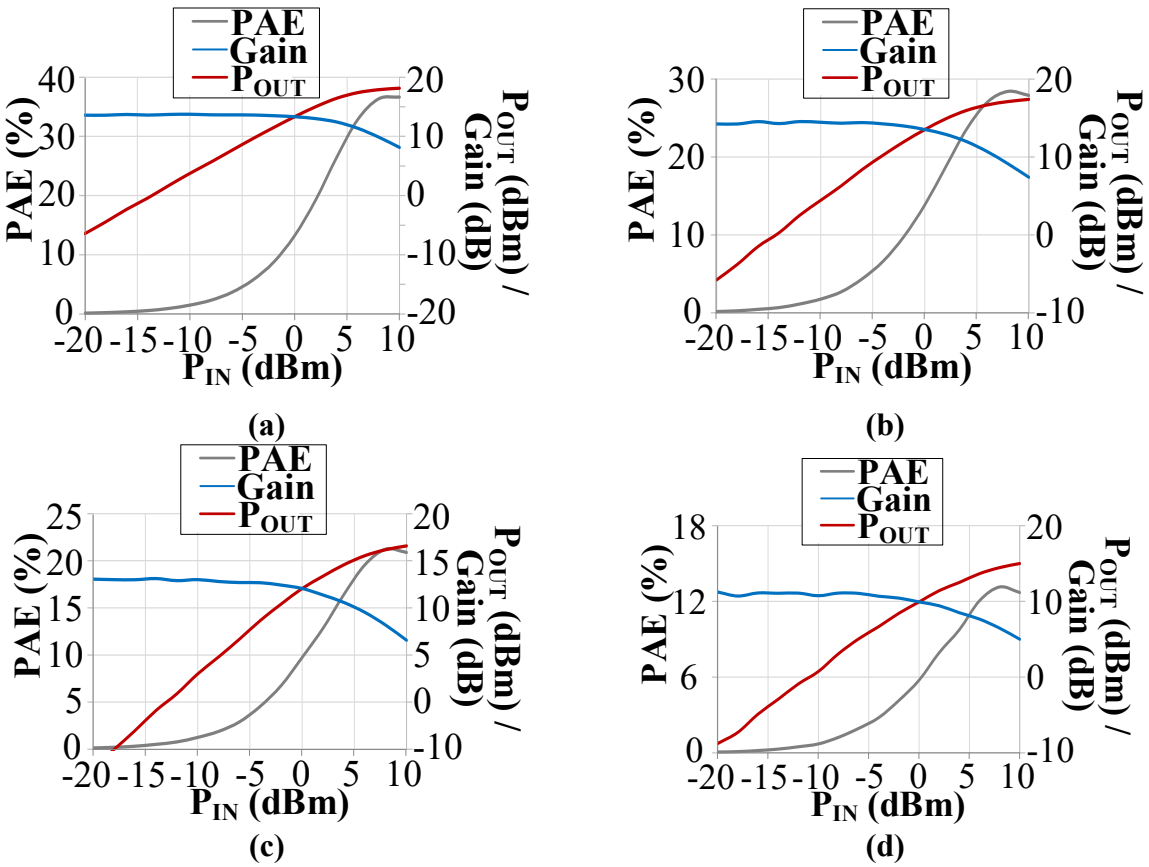


Figure 4.42: Post-layout P_{IN} vs. PAE, Gain and P_{OUT} Simulations of Broadband PA with a 3rd-order Input Matching Network at (a) 20, (b) 30, (c) 40, and (d) 50 GHz

4.3.2.2 Broadband CMOS SOI PA Using RC Feedback

The next broadband PA uses RC feedback to achieve a large BW (see Figure 4.43). After several attempts to get measurement data in these PAs and having suspected ESD issues, several different versions of ESD protected CMOS PAs were investigated and taped out and two different ESD protection versions will be discussed here. The first version (V1) offers less protection and only utilizes double diodes at all the DC pads. The second version (V2) has more ESD protection by also protecting the RF input by using the same diodes at all DC pads as well as a small PNP diode at the RF input pad.

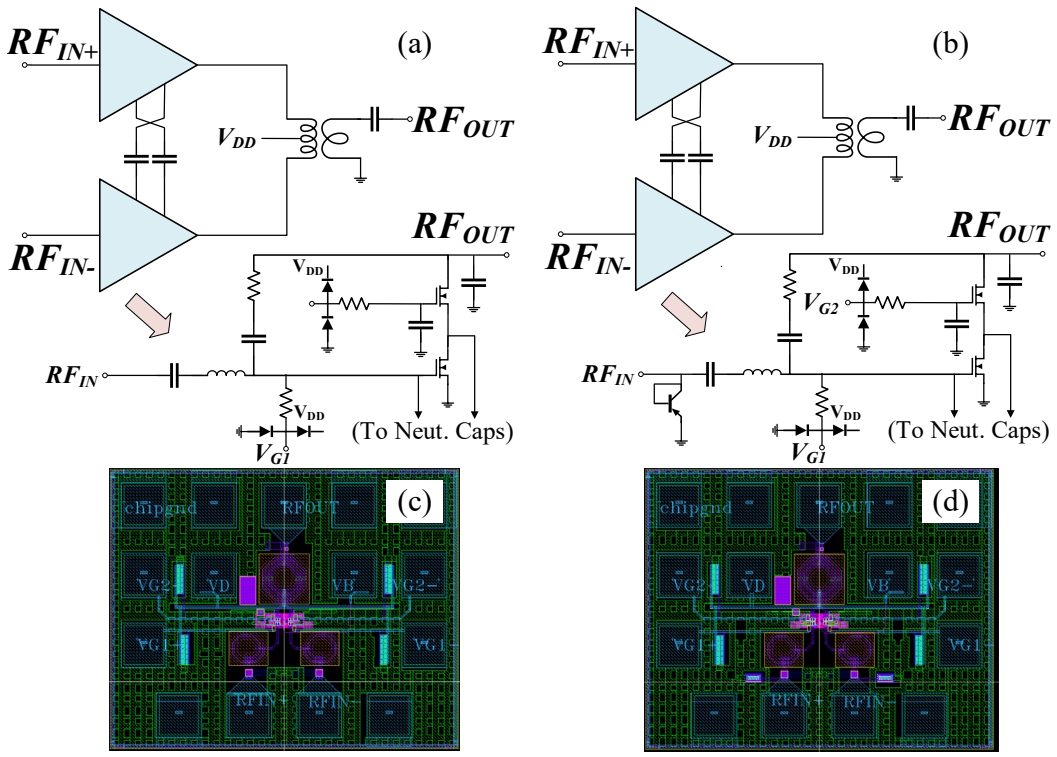


Figure 4.43: Schematics for (a) ESD V1; (b) ESD V2; and Layouts for (c) ESD V1; (d) ESD V2 of the Broadband CMOS SOI PAs with RC Feedback

PEX simulations shown in Figure 4.44 indicate that both PAs have good measured broadband results, with V1 ESD achieving small signal gain 3-dB BW of 20.0 – 47.0 GHz (absolute BW =80.6%) and max. S_{21} of 17.4 dB. The ESD V2 version achieves comparable small-signal 3-dB BW of 19.4 – 48.9 GHz (absolute BW 86.4%) with an expected gain degradation with max. S_{21} of 15.2 dB due to extra loss through the PNP diode at the RF input.

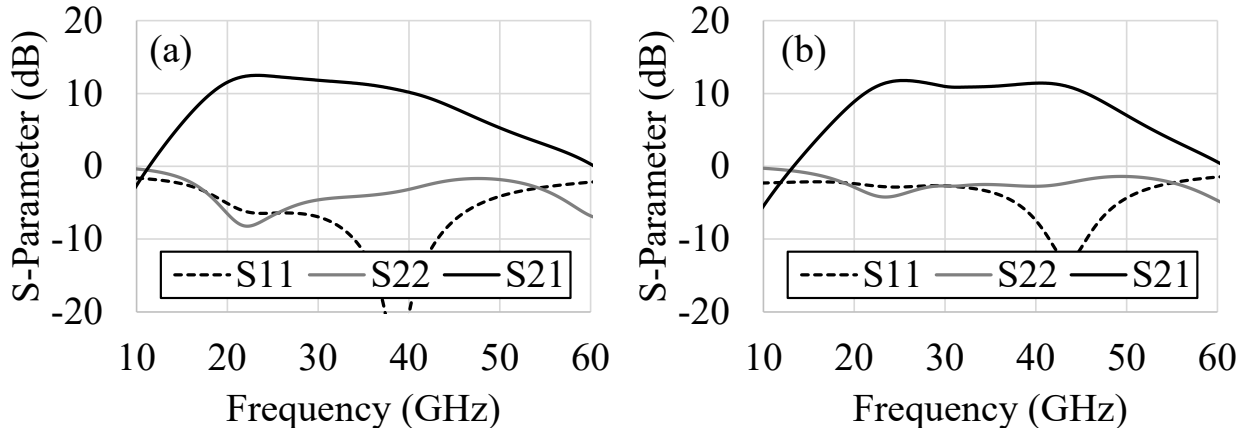


Figure 4.44: Post-layout S-parameter Simulations of Broadband CMOS SOI PA with RC Feedback for (a) ESD V1 and (b) ESD V2

In large signal PEX simulations, V1 at 24 GHz achieves OP_{1dB} of 14.3 dBm, PAE@P_{1dB} of 14.1%, $P_{OUT, SAT}$ of 17.8 dBm, and max. PAE of 37.2% as shown in Figure 4.45. The large signal simulations also show broadband results, and this PA maintains at least 20% max. PAE across the 20 – 39 GHz BW (more points are presented in Table 4.9). At 24 GHz, ESD V2 does see a degradation in PAE performance as it achieves PAE@P_{1dB} of 11.7% and max. PAE of 27.4%, with a slight degradation in output power with OP_{1dB} of 13.6 dBm, and $P_{OUT, SAT}$ of 17.2 dBm, as shown in Figure 4.46 and Table 4.10. The extra ESD diode is at the RF input and thus output power is not degraded much as gain is, when comparing ESD V1 vs. ESD V2. There is a fairly large degradation in PAE, which could be due to a frequency shift towards lower frequencies due to the diodes' parasitic capacitance, as max. PAE is achieved at lower frequencies for ESD V2.

When comparing the ESD V1 to the broadband CMOS-SOI version that uses a higher order input matching network, this design does achieve approximately the same max. PAE but suffers from lower $P_{OUT, SAT}$, which is to be expected, due to the loss at the output through the RC feedback. Interestingly, the RC feedback version achieves higher max. gain, which may be due to the flatness of the higher-order input matching network and the RC feedback being reduced so that PAE is not hurt much.

Table 4.9. Summary of Post-Layout Simulations for the ESD V1 RC Feedback Broadband 22FDX PA

Freq (GHz)	S_{21} (dB)	Max PAE (%)	PAE @P_{1dB} (%)	OP_{1dB} (dBm)	$P_{OUT, SAT}$ (dBm)
20	14.0	24.4	14.4	13.0	17.0
24	17.0	37.2	19.9	15.6	17.8
30	15.9	28.7	22.6	14.8	17.5
39	15.0	21.6	12.5	13.9	17.1

Table 4.10. Summary of Post-Layout Simulations for the ESD V2 RC Feedback Broadband 22FDX PA

Freq (GHz)	S_{21} (dB)	Max PAE (%)	PAE @P_{1dB} (%)	OP_{1dB} (dBm)	$P_{OUT, SAT}$ (dBm)
20	13.2	28.7	9.6	12.8	16.9
24	14.6	27.4	11.7	13.6	17.2
30	13.2	29.7	12.3	12.2	17.9
39	11.7	16.2	9.3	12.8	16.4

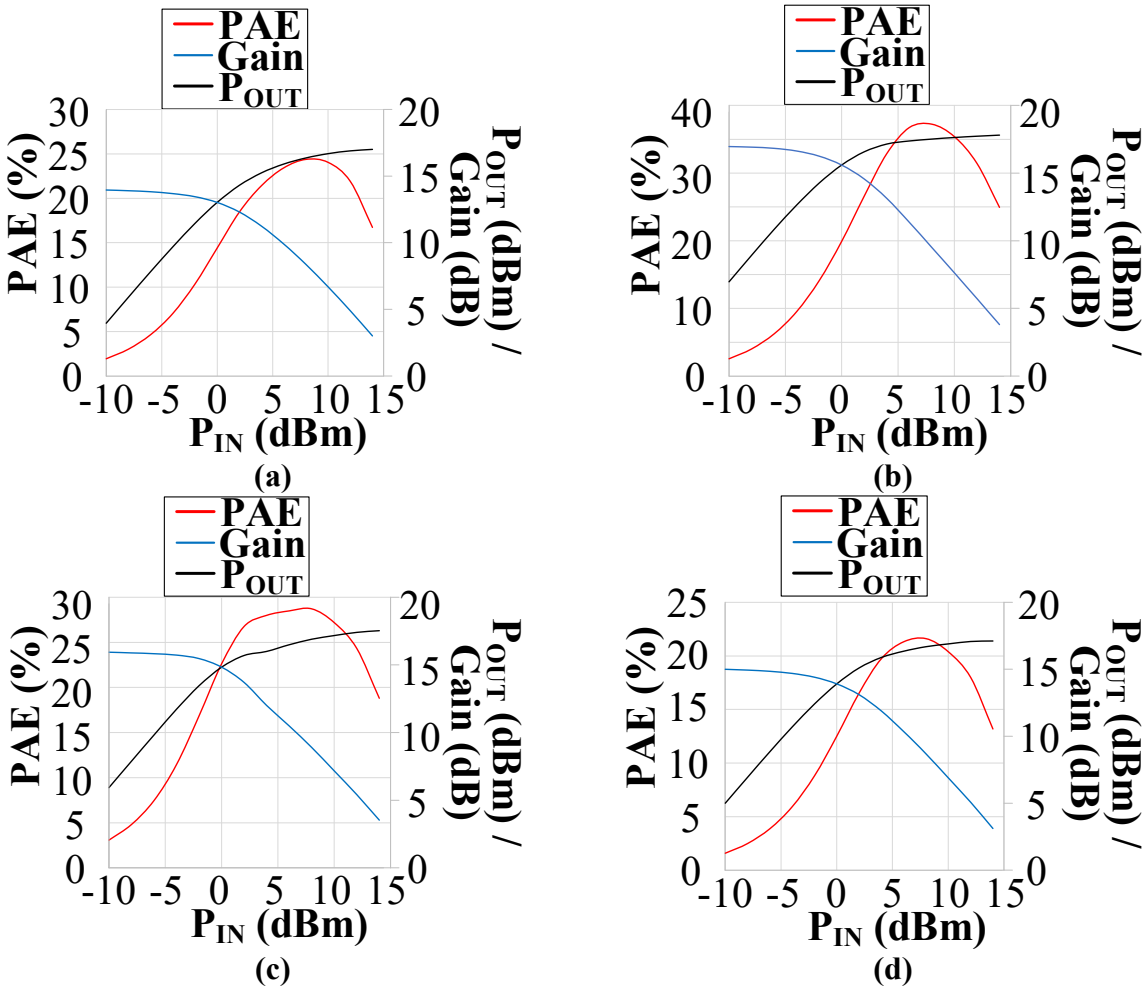


Figure 4.45: Post-layout P_{IN} vs. PAE, Gain and P_{OUT} Simulations of Broadband PA with RC Feedback ESD V1 at (a) 20, (b) 24, (c) 30, and (d) 39 GHz

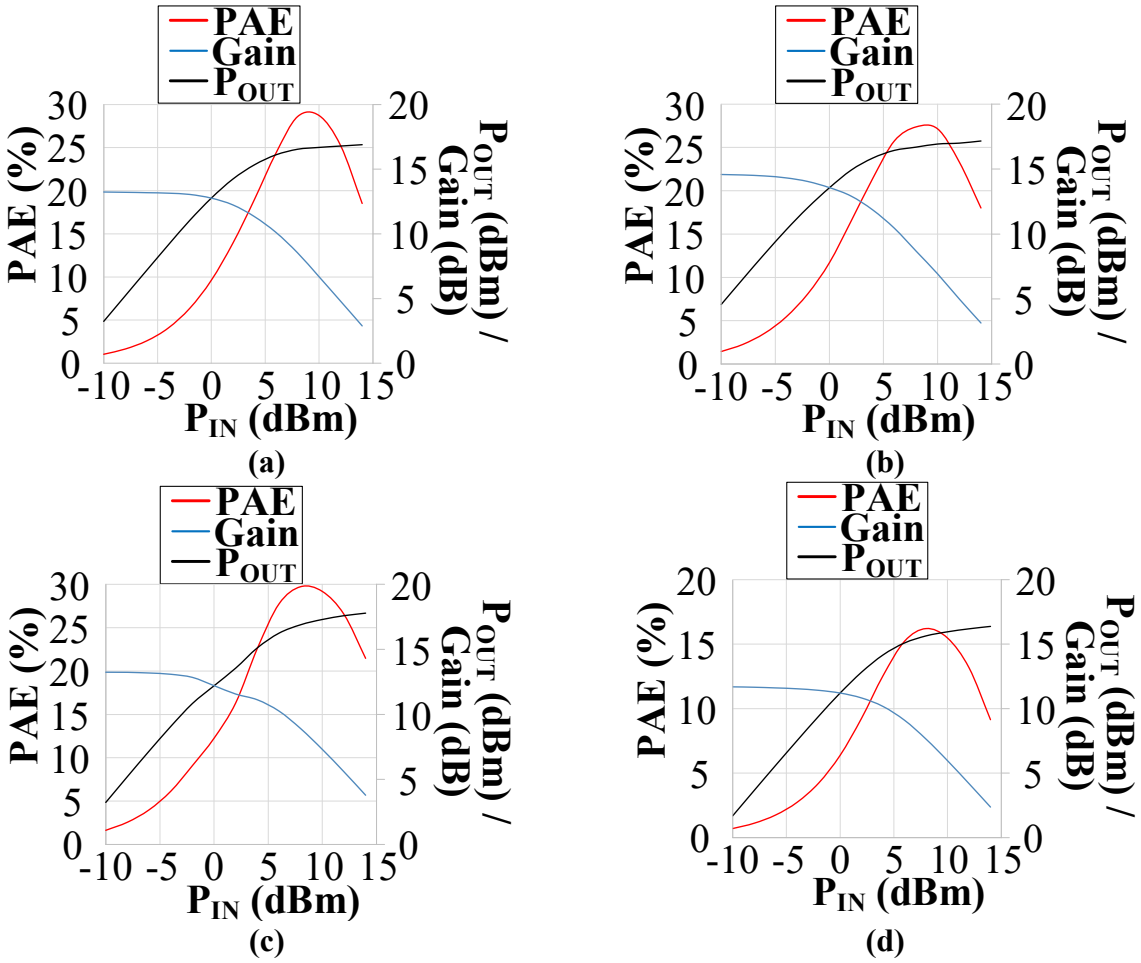


Figure 4.46: Post-layout P_{IN} vs. PAE, Gain and P_{OUT} Simulations of Broadband PA with RC Feedback ESD V2 at (a) 20, (b) 24, (c) 30, and (d) 39 GHz

Although only two broadband mm-Wave CMOS PAs with two ESD versions were presented, 5 different ESD versions were taped out to ensure that a 22FDX PA could be successfully measured. ESD V1, the version with the least amount of ESD protection, did yield measurement results and thus this version will only be discussed in measurements as extra ESD protection only degraded performance. The small-signal measurement results are shown in Figure 4.47 and the measurement data matches well with simulation. Measurement data achieves a max. S_{21} = 16.4 dB with an impressive 3-dB BW of 19.1 – 46.5 (absolute BW of 83.5%) while maintaining S_{11} < -5.5 dB across the band. Thus, measurement data sees only minimal degradation to the simulated small-signal gain and virtually no degradation in the targeted broadband design BW to cover the entire key 5G FR2 band of 24.25 – 43.5 GHz.

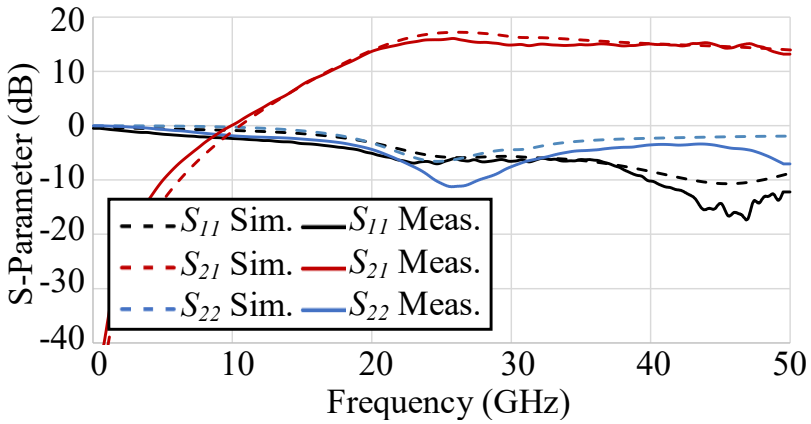


Figure 4.47: S-parameter Post-layout PEX Simulations vs. Measurement of the Broadband 22 nm CMOS FD-SOI PA with RC Feedback ESD V1

However, there is a large degradation in the large signal results as shown in Figure 4.48. Measurement shows that this broadband PA achieves at 24/28/37/44 GHz OP_{1dB} of 11.5/9.2/9.5/7.4 dBm with PAE@P_{1dB} of 18.6%/11.2%/11.5%/9.3%, $P_{OUT,\,SAT}$ of 14.6/14.0/13.6/10.9 dBm, and max. PAE of 26.1%/19.9%/ 18.5%/12.5 %, respectively. Figure 4.49 plots the measured max. PAE, S_{21} and $P_{OUT,SAT}$ from 20 – 44 GHz vs. frequency to show the broadband nature of this PA. For instance this PA maintains at least a max. PAE ≥ 12.5% and $P_{OUT,SAT}$ ≥ 11 dBm across the full large frequency range that was measured. In addition, it maintains max. PAE ≥ 15.1% and $P_{OUT,SAT}$ ≥ 12.9 dBm across 24 – 39 GHz. Thus, this PA in particular is able to maintain reasonable PAE across the n257 (26.5 – 29.5 GHz), n258 (24.25–27.5 GHz), and n261 (27.5 – 28.25 GHz) bands as well as practically all of the n260 (37 – 40 GHz) band.

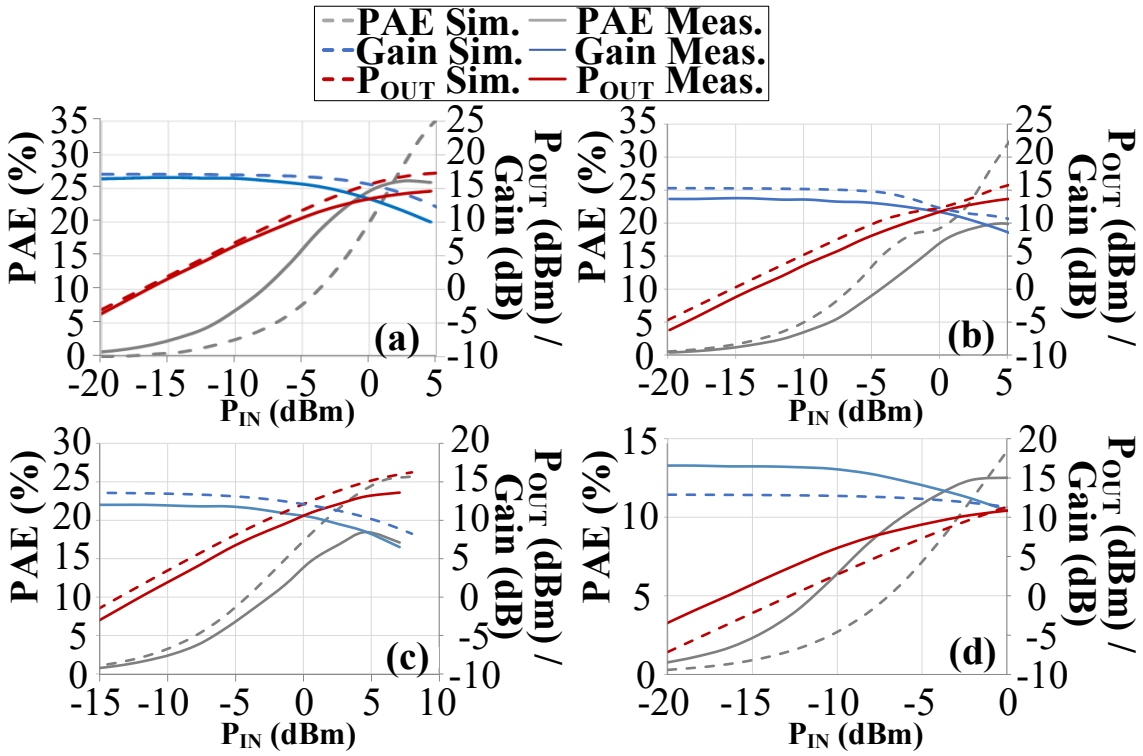


Figure 4.48: P_{IN} vs. PAE, Gain and P_{OUT} post-layout PEX Simulation vs. Measurement of the Broadband 22 nm CMOS FD-SOI PA with RC Feedback ESD V1 at (a) 24, (b) 28, (c) 37, and (d) 44 GHz

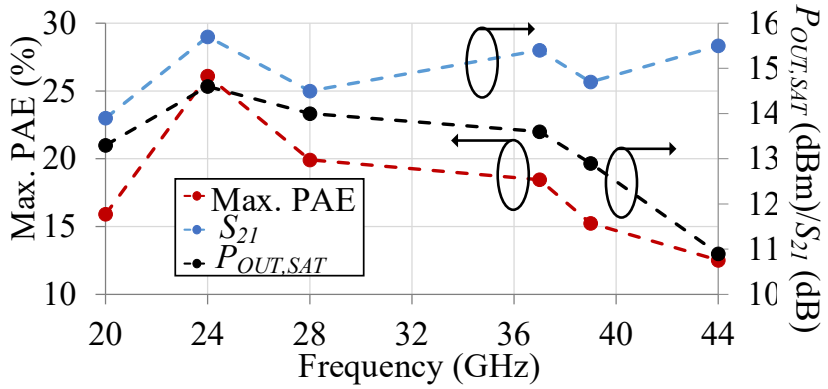


Figure 4.49: Measured Max. PAE, S_{21} and $P_{OUT,SAT}$ vs. Frequency of the Broadband 22 nm CMOS FD-SOI PA with RC Feedback ESD V1

Using the state-of-the-art mm-Wave PXIE (PCI express extensions for instrumentation) system by National Instruments (NI) [51], the PA's linearity is tested with 5G 256-QAM NR signals with the same PAPR of 8.0 dB with BWs of 50/100/400/9x100 MHz at 24 GHz (Figure 4.50). All of these measurements are with $P_{OUT,AVE}$ = ~7 dBm, and this PA achieves ACLR (adjacent

channel leakage ratio) -/+ of -28.0/-29.4 dBc (PAE_{AVE}= 7.3%) with BW= 50 MHz, -27.6/-28.8 dBc (PAE_{AVE} = 7.0%) with BW= 100 MHz, -27.3/-27.0 dBc (PAE_{AVE} = 7.7%) with BW= 400 MHz and -24.6/ -25.9 dBc (PAE_{AVE}= 8.1%) with BW= 9x100 MHz.

The effect of the instantaneous signal BW has on the linearity for this PA is investigated and the BW of a 256-QAM 5G NR signal (PAPR = 8 dB) is varied from 50 MHz to 9x100 MHz at 24 GHz and 28 GHz, with $P_{OUT,AVE}$ = ~7 dBm, and at 37 GHz and 39 GHz with $P_{OUT,AVE}$ = ~6 dBm (Figure 4.51). The linearity is not affected much when the BW is increased from 50 MHz to 100 MHz, but when the instantaneous signal BW increases from 100 MHz to 400 MHz, the PA's linearity degrades by ~1 – 2 dB. However, when increasing from 400 MHz to 9x100 MHz, the linearity becomes further degraded by ~3 dB and at all frequencies. The linearity across operating frequencies is not degraded much however, as when the PA's center frequencies change from 24/28 GHz to 37/39 GHz, its linear output power only degrades by ~1 dB.

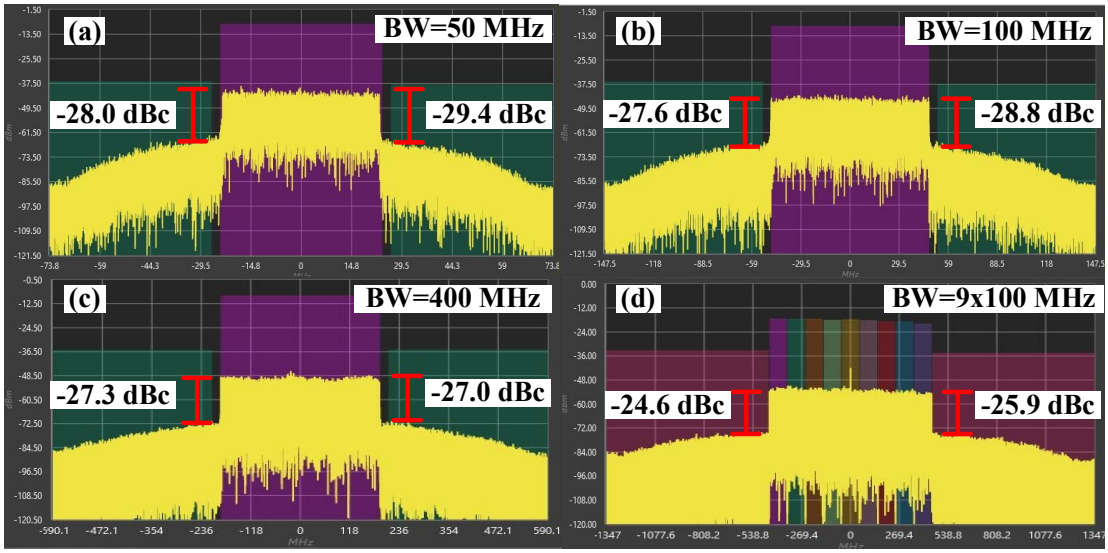


Figure 4.50: ACLR Measurements of the Broadband 22 nm CMOS FD-SOI PA with RC feedback ESD V1 at 24 GHz using a 256-QAM 5G NR Signal with PAPR = 8 dB for Instantaneous Signal BWs of: (a) 50 MHz, (b) 100 MHz, (c) 400 MHz, and (d) 9x100 MHz.

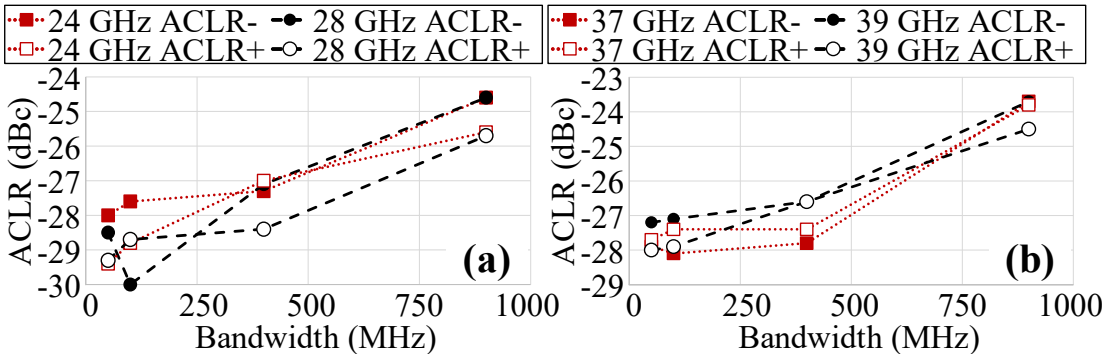


Figure 4.51: Measured ACLR+/ACLR- vs. Modulated Instantaneous signal BW using a 256-QAM 5G NR signal (PAPR = 8 dB) for the Broadband 22 nm CMOS FD-SOI PA with RC Feedback ESD V1 at the Operation Frequency of: (a) 24 GHz and 28 GHz ($P_{OUT,AVE}$ = ~7 dBm), and at (b) 37 GHz and 39 GHz ($P_{OUT,AVE}$ = ~6 dBm)

4.3.3 Adaptive Biasing Techniques for Linearity Enhancement

The design discussed in the Sec. 4.3.2 is expanded upon by improving the "linear PAE" of the PA, which is the PAE at say 6-dB power back-off from the max. P_{OUT} where the PA is much more linear than at its peak P_{OUT}. The exact level of power back-off from the peak P_{OUT} one should choose to determine the linear PAE of a PA depends on the input RF signal, especially on its PAPR level, and also on the intrinsic linearity behavior of PA's design vs. P_{OUT}. Therefore, many would simply choose the PAE@P_{1dB} as a good indicator of the PA's linear PAE performance. In our design, this work are able to improve the linear PAE of the broadband CMOS PA in Sec. 3.3.2 by adding an adaptive biasing circuit to the CS device (M3 in Figure 4.52) in the hybrid cascode/stack topology. To do this, RF input is AC-coupled via a capacitor to the gate of M1, which is biased in the *sub-threshold* region. As RF input power increases, the average voltage at M1's gate increases, and I_{DS} rises exponentially due to this sub-threshold biasing. This raises the $I{\cdot}R$ voltage drop through R_5 and thus increases the gate bias of M2, which is also biased in sub-threshold region. Subsequently, this increases the $I{\cdot}R$ drop through R_7 and finally the gate bias of the PA transistor M3 increases accordingly. This biasing method is different from many RF adaptive biasing circuits in literature [62-66] as it uses this sub-threshold biasing, which can be rather sensitive and quick to respond to the instantaneous variation of the RF input power level. Figure 4.52 shows the gate bias at M3 changes from 0.36 V to 0.57 V as the CW (continuous-wave) P_{IN} increases from -10 dBm to 10 dBm. This makes the PA operation move from class AB mode (threshold voltage V_T = 0.29 V) closer to Class A mode. Therefore, when the PA is in the power back-off region where high PAE is desired to achieve overall excellent PAE at $P_{OUT,AVE}$ and also with good PA linearity, this biasing network allows the PA to be biased in a class AB mode. When power increases and linearity becomes more critical, the biasing network will bias the PA hotter closer to a Class A mode and thus will be more linear. Our PA design is differential and uses two separate gates and thus two separate, but identical single-ended adaptive biasing circuits are used. This adaptive biasing network is added to the RC feedback design in Sec. 4.3.2 for both ESD-protected PA versions (Figure 4.53).

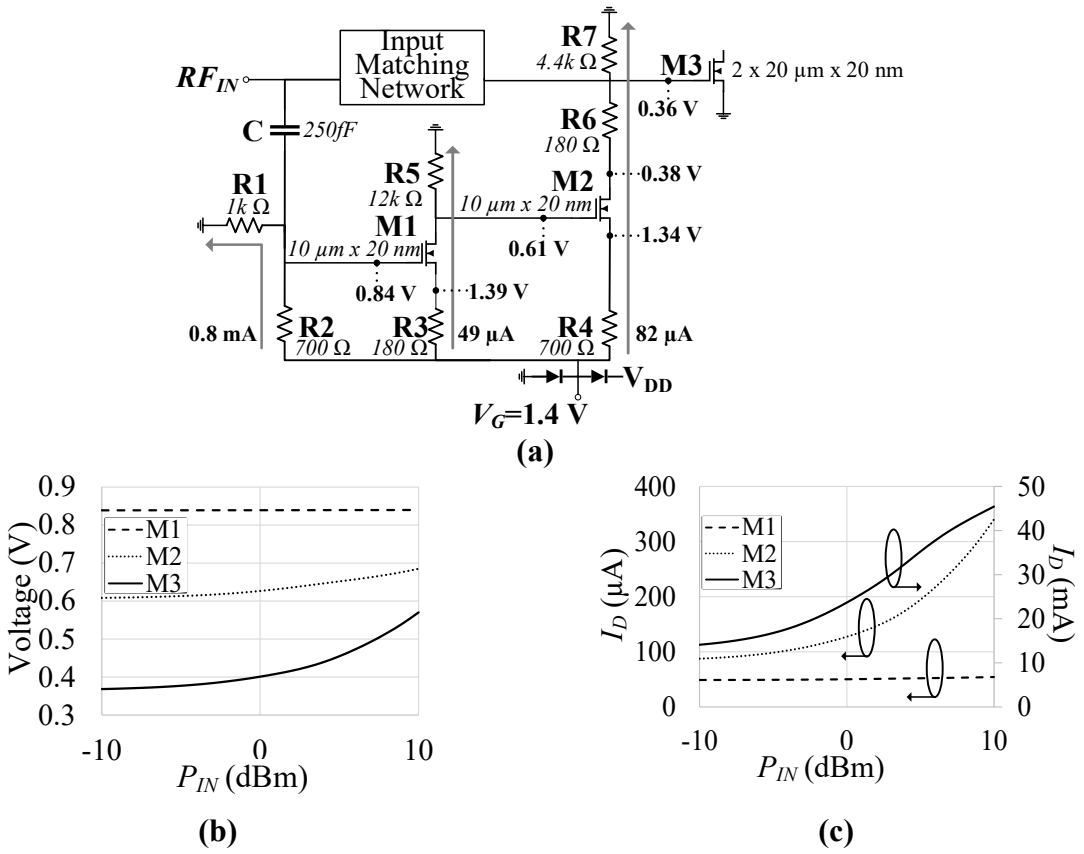


Figure 4.52: Schematic of Adaptive Biasing Network (a) and (b) DC Voltages and (c) DC Current with Increased RF Input Power in a CW Mode

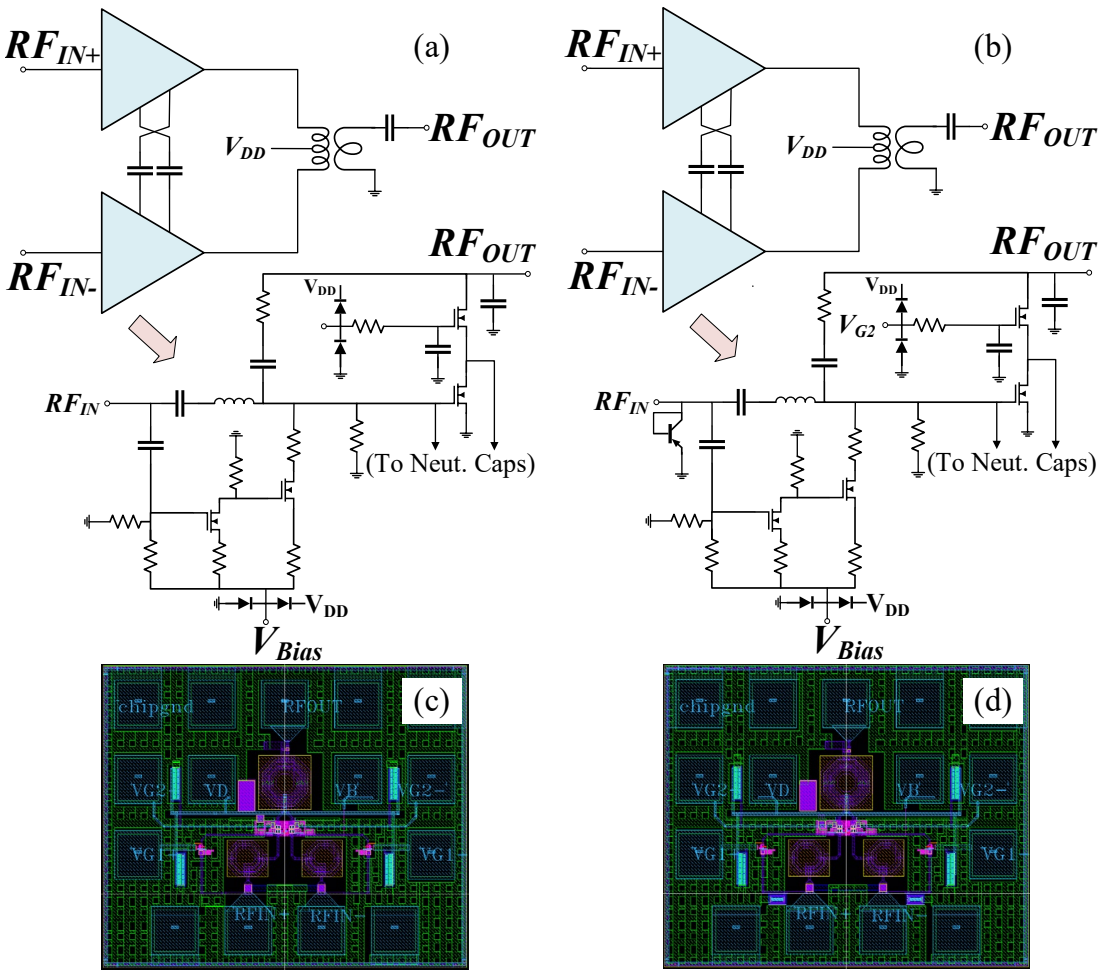


Figure 4.53: Full Schematic of Broadband ESD-protected CMOS SOI PAs with the Adaptive Biasing Network: (a) ESD V1; (b) ESD V2

The PEX simulated S-parameters for both of the adaptively biased PAs are shown in Figure. 4.54 and the ESD V1 PA achieves 3-dB BW of 17.8 – 42.0 GHz (absolute BW 80.9%) with a max. S_{21} of 12.5 dB, while the ESD V2 PA achieves max. S_{21} of 11.8 dB and 3-dB BW of 20.0 – 47.4 GHz (absolute BW 81.3%). Thus, the BW for the ESD V2 PA is about the same as the ESD V1 PA with a significant degradation in the S_{11} when the PNP ESD diode is added at the RF input.

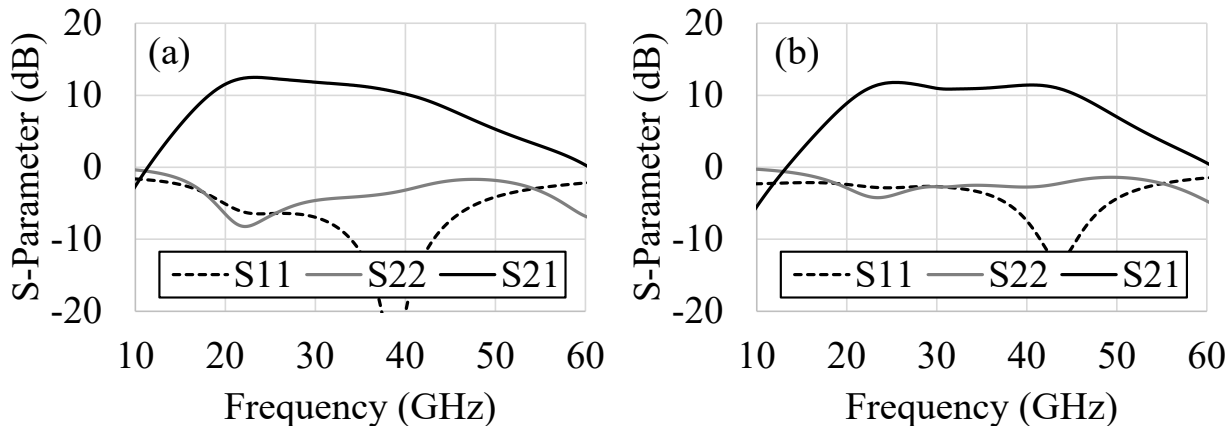


Figure 4.54: Post-layout S-parameter Simulations of Broadband PAs with RC Feedback and Adaptive Biasing for (a) ESD V1 and (b) ESD V2

The adaptively biased ESD V1/V2 PAs achieve max. PAE of 36.3%/32.7%, OP_{1dB} of 14.4/14.2 dBm with PAE@P_{1dB} of 29.2%/26.6% and $P_{OUT,\,SAT}$ of 17.8/17.7 dBm at 24 GHz, as shown in the large signal PEX simulations for the adaptive biasing PAs in Figures. 4.55 and 4.56 and Table 4.11 and Table 4.12. The considerable degradation in the PA large signal performance between V1 and V2 is reduced for the adaptive biased PAs compared to the fixed bias PAs, which may be due to extra frequency shift due to the parasitics of the adaptive bias network.

Table 4.11. Summary of Post-Layout Simulations for the ESD V1 Broadband 22FDX PA with Adaptive Biasing

Freq (GHz)	S_{21} (dB)	Max PAE (%)	PAE@P_{1dB} (%)	OP_{1dB} (dBm)	$P_{OUT,\,SAT}$ (dBm)
24	13.6	36.3	29.2	14.4	17.8
30	12.7	29.7	28.7	15.3	17.7
39	11.4	20.2	20.2	15.9	16.9

Table 4.12. Summary of Post-Layout Simulations for the ESD V2 Broadband 22FDX PA with Adaptive Biasing

Freq (GHz)	S_{21} (dB)	Max PAE (%)	PAE@P_{1dB} (%)	OP_{1dB} (dBm)	$P_{OUT,\,SAT}$ (dBm)
24	11.0	32.7	26.6	14.2	17.7
30	10.1	26.0	25.2	15.3	17.3
39	9.6	20.1	20.1	15.7	16.8

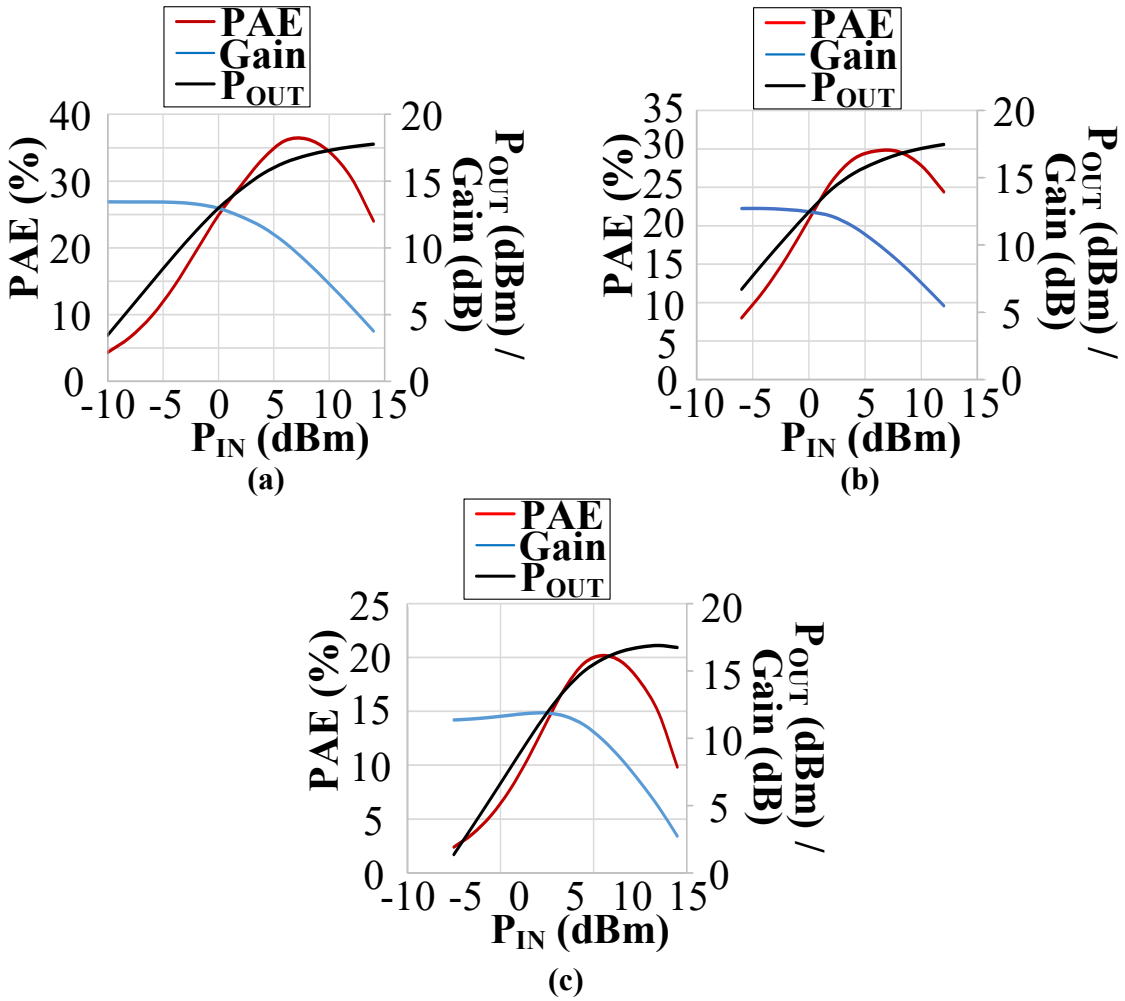


Figure 4.55: Post-layout P_{IN} vs. PAE, gain and P_{OUT} simulations of broadband PA with RC feedback and adaptive biasing for ESD V1 at (a) 24 GHz, (b) 30 GHz, and (c) 39 GHz

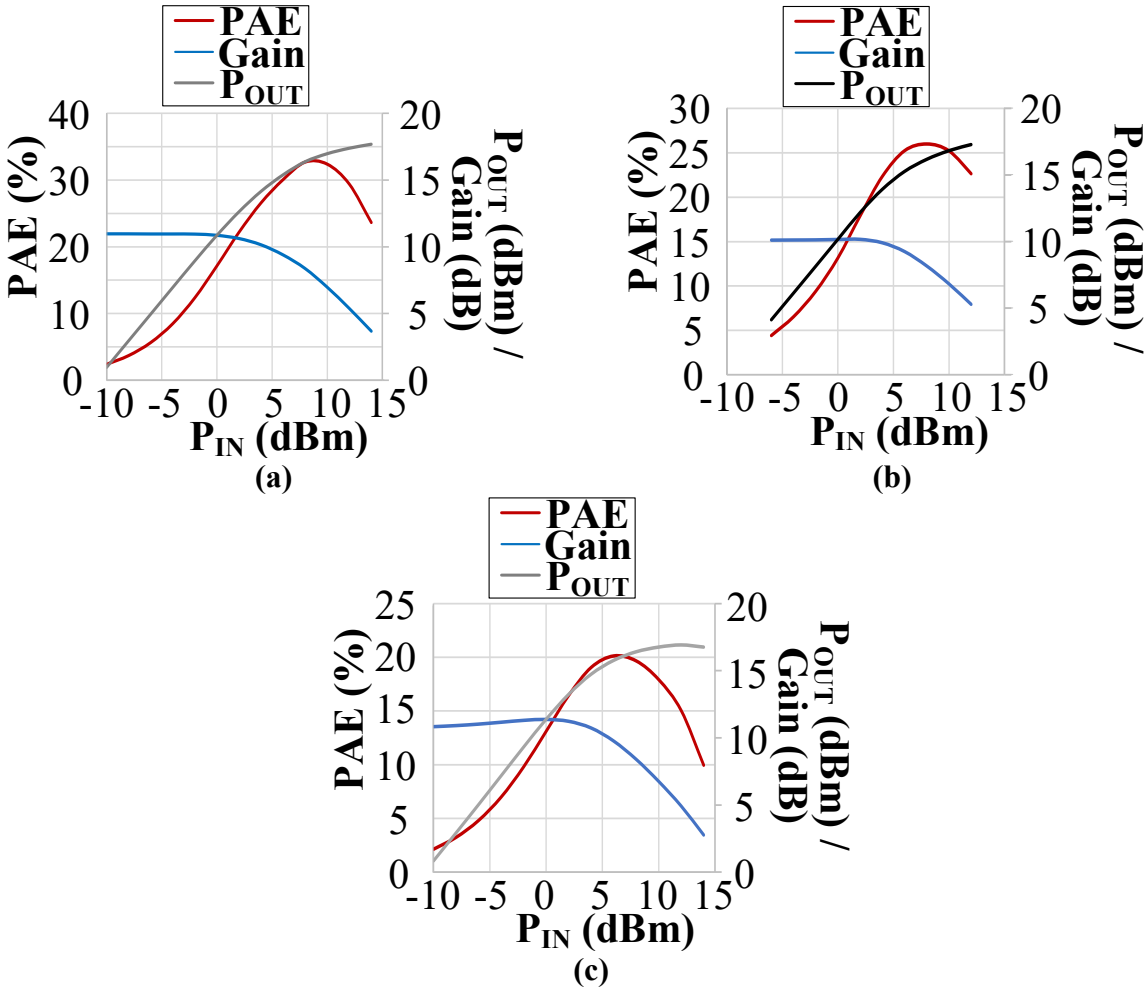


Figure 4.56: Post-layout P_{IN} vs. PAE, gain and P_{OUT} simulations of broadband PA with RC feedback and adaptive biasing for ESD V2 at (a) 24 GHz, (b) 30 GHz and (c) 39 GHz

Just as what had been observed in the fixed bias version, ESD V1 for the adaptive biasing circuit was found to provide enough ESD protection for these designs and test setup, and thus only ESD V1 measurements are shown here. Figure 4.57 shows the S-parameter measurement vs. post-layout PEX simulation results, which shows that this PA achieves a 3-dB BW of 18.7 – 42.0 GHz and a max. S_{21} = 14.4 dB (absolute BW of 76.8%) in measurement. Thus, the BW is slightly degraded in measurement from simulation; however, the small signal measured results match reasonably well with PEX simulation.

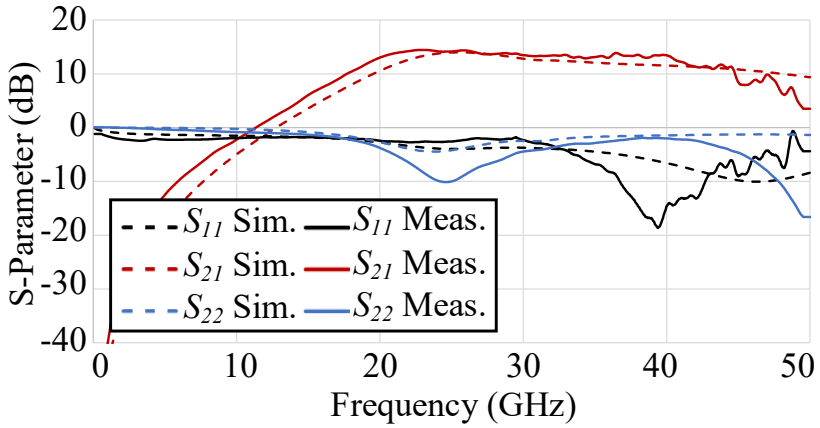


Figure 4.57: S-parameter Post-layout PEX Simulation vs. Measurement of the Broadband 22 nm CMOS FD-SOI PA with RC Feedback with Adaptive Biasing ESD V1

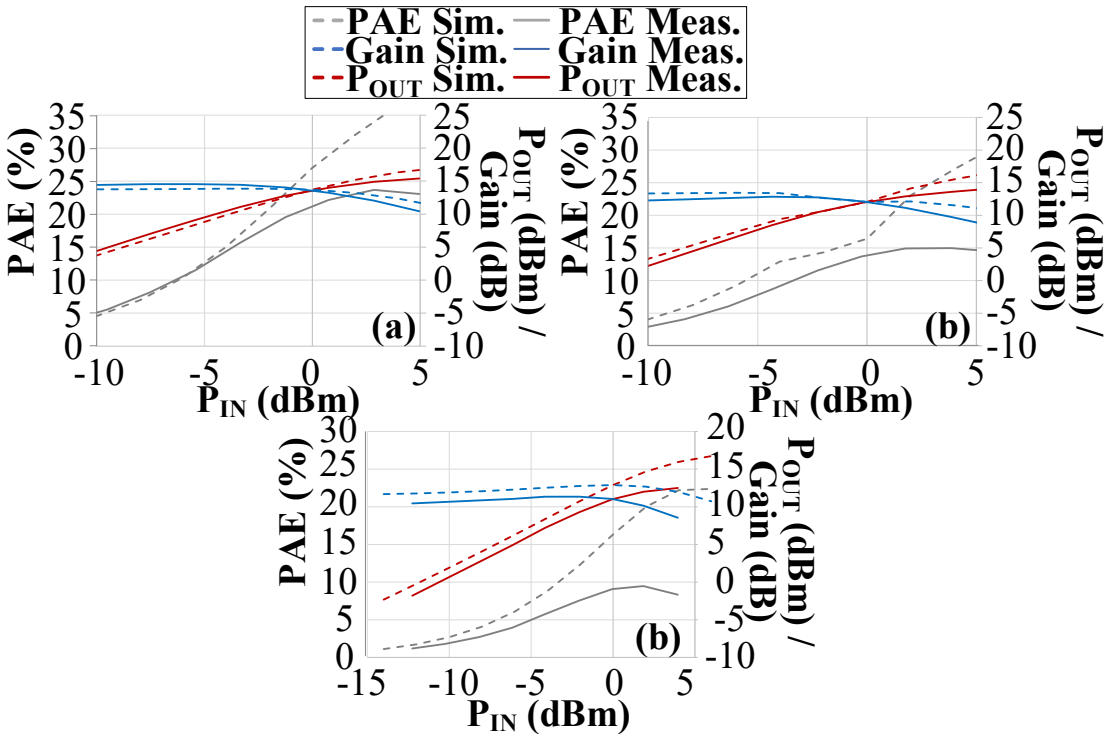


Figure 4.58: P_{IN} vs. PAE, Gain and P_{OUT} Post-layout PEX Simulations vs. Measurements of the Broadband 22 nm CMOS FD-SOI PA with RC Feedback and Adaptive Biasing ESD V1 at (a) 24 GHz, (b) 28 GHz, and (c) 37 GHz

There is also a significantly larger degradation in the large-signal measured performance from PEX simulations in the adaptively biased version, especially at higher frequencies and in P_{OUT}. At 24/28/37 GHz it achieves OP_{1dB} of 13.6/12.2/11.8 dBm with PAE@P_{1dB} of 22.0%/14.1%/9.3%, $P_{OUT,\,SAT}$ of 15.7/14.2/12.5 dBm, and max. PAE of 23.7% /15.0%/9.5 %, as shown in Figure 4.58.

Figure 4.59 shows the measured PAE@P_{1dB} vs. frequency as well as OP_{1dB} vs. frequency for the adaptive and fixed biased PAs from 24 – 39 GHz. This shows that adding the adaptive biasing network can improve the OP_{1dB} by ~2 dB across this frequency range. This adaptive biasing circuit is also able to improve PAE@P_{1dB} from 24 – 28 GHz by ~5%, however, it does not improve PAE@P_{1dB} at the higher frequencies above 34 GHz, likely due to the higher parasitics/mismatch from the addition of the adaptive bias circuit.

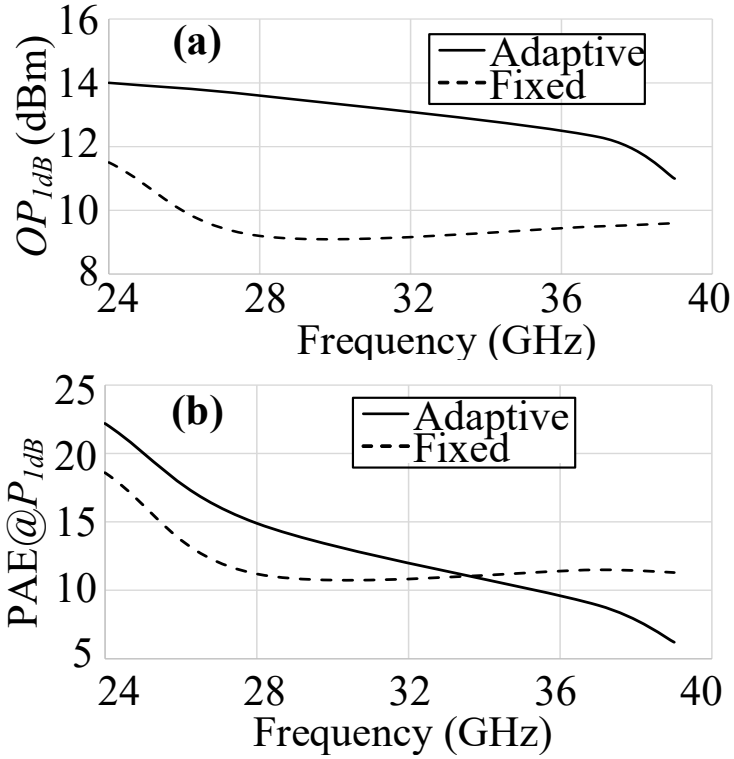


Figure 4.59: Large-signal Measurements

PAE@P_{1dB} vs. Frequency (a); and (b) OP_{1dB} vs. Frequency Comparisons for the Fixed vs. Adaptive Bias Broadband CMOS PAs with ESD V1 Design using CW RF Signal Inputs

In measurement, there is a large degradation in the large-signal performance for both the adaptive bias and fixed bias PAs, but this degradation is worse for the adaptive bias version, especially at higher frequencies. There was not an improvement in the PAE@P_{1dB} at the higher frequencies when adding the adaptive bias, however, the PAE@P_{1dB} for the fixed bias was higher than the adaptive bias PA's max. PAE at these higher frequencies. Thus, this work will also show post-layout PEX simulated PAE@P_{1dB} versus frequency as well as OP_{1dB} versus frequency of the fixed and adaptively biased PAs in Figure 4.60. There is at least a 5% PAE improvement at OP_{1dB} (i.e., at ~ 3-dB power back-off from $P_{OUT, SAT}$) across 24 – 40 GHz with the addition of the adaptive biasing network, and the maximum PAE improvement is at 24 GHz where the PAE@P_{1dB} increases from 14.1% to 29.2%. PAE@ 6-dB back-off is a typical metric for Doherty PAs [55] and this is improved from 9.5% to 19.2% with 24 GHz CW input, and from 4.2% to 11.2% at 37 GHz with the addition of the adaptive biasing network. Also, around 37 – 39 GHz, OP_{1dB} is higher by ~2 dB and is also consistently better across the frequency range

with the adaptive biasing. The fixed-biased V1 PA achieves max. PAE of 36.7%/22.7% and $P_{OUT,\,SAT}$ of 17.8/17.3 dBm at 24/37 GHz; and after the addition of the adaptive biasing network, the PA achieve max. PAE of 36.3%/21.7% and $P_{OUT,\,SAT}$ of 17.8/17.1 dBm. Thus, the adaptive biasing network does not degrade $P_{OUT,\,SAT}$ nor the max. PAE, while improving the PAE performance at power back-off in PEX simulation. The discrepancies between the measured vs. PEX large-signal simulated data may be at least partly caused by the inaccuracy of the R+C+CC post-layout parasitic extraction as the transmission line inductance parasitics are ignored. This work are currently working with the foundry to try to resolve the issues of their updated process stack that prevented us from using the supposedly more accurate EM simulation to investigations the causes of these measurement vs. modelled discrepancies as the adaptive biasing network requires much longer unmodeled transmission lines compared to the fixed biased PA.

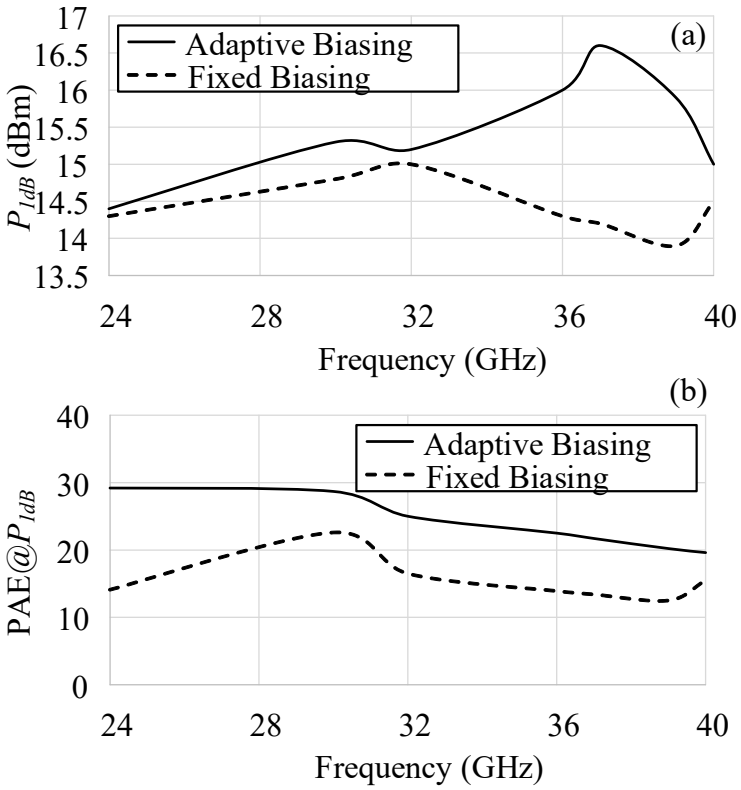


Figure 4.60: PEX large-signal Simulation

PAE@P_{1dB} vs. frequency (a); and (b) OP_{1dB} vs. frequency comparisons for the fixed vs. adaptive bias broadband CMOS PAs with ESD V1 design using CW RF signal inputs.

Table 3.6 shows a comparison to state-of-the-art broadband and narrowband mm-Wave 5G PAs with our ESD V1 fixed and adaptive biased PAs. Although these designs in the literature listed on Table 3.6 are all relatively narrowband PA, our adaptively biased wideband PA is able to achieve higher PAE@P_{1dB} at 24 GHz compared to [62] and [63]. Ref. [63] presented a similar comparison with a fixed biased PA version vs. an adaptive biased PA. Our measured data suggests that the adaptive biasing circuit used in ESD V1 PA can improve PAE@P_{1dB} from the

fixed bias design around the same ~5% [63], however, our PA was able to improve OP_{1dB} slightly more and across a large frequency range. The amazing work done in [55] showed a state-of-the-art Doherty PA with an impressive 52.1% absolute BW and ~18 dB gain in a 0.13 mm SiGe technology. However, this work suggests that the Doherty PA topology may be intrinsically limited from achieving BW significantly larger than ~ 50%, and as [55] has by far the largest circuit core size in Table 3.6 as well, this work believe it highlights the attractive benefits of the adaptive biasing circuit presented in this section, as our design is able to improve OP_{1dB} across a large frequency range and had the best 3-dB BW amongst all these works.

Table 4.13. Comparison of the CMOS-SOI Fixed and Adaptive Bias PAs to Other State-of-the-Art mm-Wave 5G Silicon PAs

Ref	Tech.	Design	Supply Volt. (V)	3-dB BW (GHz)	Freq. (GHz)	$P_{OUT,sat}$ (dBm)	OP_{1dB} (dBm)	PAE@ P_{1dB} (%)	Peak PAE (%)	Gain (dB)	Core size (mm^2)
[62]	90-nm CMOS	2-stage cascode w/ adaptive bias	2.4	Narrow band	21	20.4	18.5	13.3	17.3	26.9	0.5*
[63]	0.13 µm CMOS	2-stage w/ adaptive bias	1.2	Narrow band	24	16.0	13.3	15.6	17.7	15.6	0.36*
		2-stage w/ fixed-bias				15.2	12.1	11.7	18.5	17.2	
[64]	65-nm CMOS	Cascode w/ adaptive bias and dynamic feedback	2	24.25-27.5 (12.6%)	24.25	N/A	18.7	30*	37.2	15.3	0.19
[55]	130-nm SiGe	2-stage Doherty fixed-bias	1.5	23.3-39.7 (52.1%)	28	16.8	15.2	19.5	20.3	18.7	1.76
					37	17.1	15.5	21.6	22.6	18	
					39	17.0	15.4	20.7	21.4	15.6	
This work	22-nm FD-SOI	Differential cascode; fixed-bias	1.8	19.1-46.5 (83.5%)	24	14.6	11.5	18.6	26.1	16.4	0.07
					37	13.6	9.5	11.5	18.5	14.0	
This work	22-nm FD-SOI	Differential cascode; **adaptive bias**	1.8	18.7-42.0 (76.8%)	24	15.7	13.6	**22.2**	**23.7**	14.3	0.11
					37	12.5	11.8	**9.3**	**9.5**	13.4	

*Estimated from figure

4.3.4 22FDX Conclusion

22FDX is a state-of-the-art RF/mm-Wave technology that offers very high f_T and f_{MAX}; however, as it is still a CMOS technology, it intrinsically suffers from lower breakdown voltages compared to SiGe or III-V technologies. Thus, in this chapter this work discussed the methods that were used to increase the power such as differential operation and stacking/cascoding devices. After starting from a narrowband design, a broadband design was realized using RC feedback and a higher order input matching network as discussed in Chapter 3, together with the hybrid cascode/stack topology that is critical for broadband performance optimization. In this technology, this work had some ESD/oxide-reliability issues and were unable to get measurement data on some of these designs and thus this work tried several different ESD versions with RC feedback. After adding these ESD versions on-chip, measurements were finally successfully achieved, and this work did find good measurement to simulation agreement for small signal. This work has shown two ESD-protected broadband PA designs achieved similar BW and max. PAE in this chapter, but one with some degradation in the RF output power likely due to the parasitics associated with the ESD diodes at RF. The measured 3-dB of

this PA was 19.1 – 46.5 GHz with good max. PAE of 26.1% at 24 GHz, and it maintains max. PAE above 15.1% across the entire 24 – 39 GHz. This work then improved the PA linearity by adding an adaptive biasing circuit. This allows the PA to be biased in Class AB mode with higher PAE@P_{1dB}. As expected and desired, the adaptive biasing network does not have much effect on the PA BW, and large signal PEX simulations indicate that the adaptively biased PA is able to improve OP_{1dB} by ~2 dB across the 24 – 39 GHz frequency range. Thus, this technology was able to achieve reasonable results throughout the mm-Wave 5G FR2 band. There was some degradation in the adaptive biasing circuit.

4.4 SiGe Results and Discussions

Using GlobalFoundries' (GF) 9HP SiGe process, which is a 90 nm SiGe BiCMOS process, several different broadband PAs were designed. This technology features a high-performance npn HBT (hetero-junction bipolar transistor), which achieves peak fT/fMAX of 300 GHz/ 360 GHz, respectively, and breakdown voltage of 1.7 V by a combination of vertical and lateral scaling from previous GF's 0.13 □m SiGe BiCMOS technologies (i.e., 8HP) [67]. These designs also use a hybrid cascode/ stack configuration, like what had been done in the previous section with the 22FDX technology. Thus, this is able to create a data point for the SiGe processes against the CMOS FD-SOI processes on broadband mm-Wave PA design. This chapter is mostly based on post-layout simulations only, as there have been issues with the layouts, long fabrication cycles, etc., which will be discussed in the later part of the chapter and in the last chapter of this report for future works.

Just as what had been done with the 22FDX devices and the GaN devices, load-pull simulations were ran on the 8 x 4 μm 9HP devices used in the designs throughout this chapter. Figure 4.61 shows the load-pull simulations done at the fundamental frequency on a single-ended SiGe cascode 8 x 4 μm pair at 24 GHz and 37 GHz at around P1dB. This shows that it can achieve very good max. PAE of 43.9% and 38% at 24 GHz and 37 GHz, respectively. Comparing to the 22FDX load-pull simulations, these SiGe devices achieve much higher output power (~12 dBm OP1dB for the CMOS FD-SOI cascode pair vs. ~18 dBm OP1dB for the SiGe cascode pair), as well as higher max. PAE (35% for the CMOS FD-SOI cascode pair vs. ~44% PAE for the SiGe cascode pair). However, optimum loads for both PAE and output power are closer to 50 Ω for the 22 nm CMOS SOI technology compared to the 90 nm SiGe BiCMOS technology. This could affect the PA's broadband performance and favors the CMOS PA, and will be explored further later. In this chapter, the use of an RC feedback and/or a high-order input matching network is explored, as well as possibly using neutralization capacitors in this technology for broadband mm-Wave PA design.

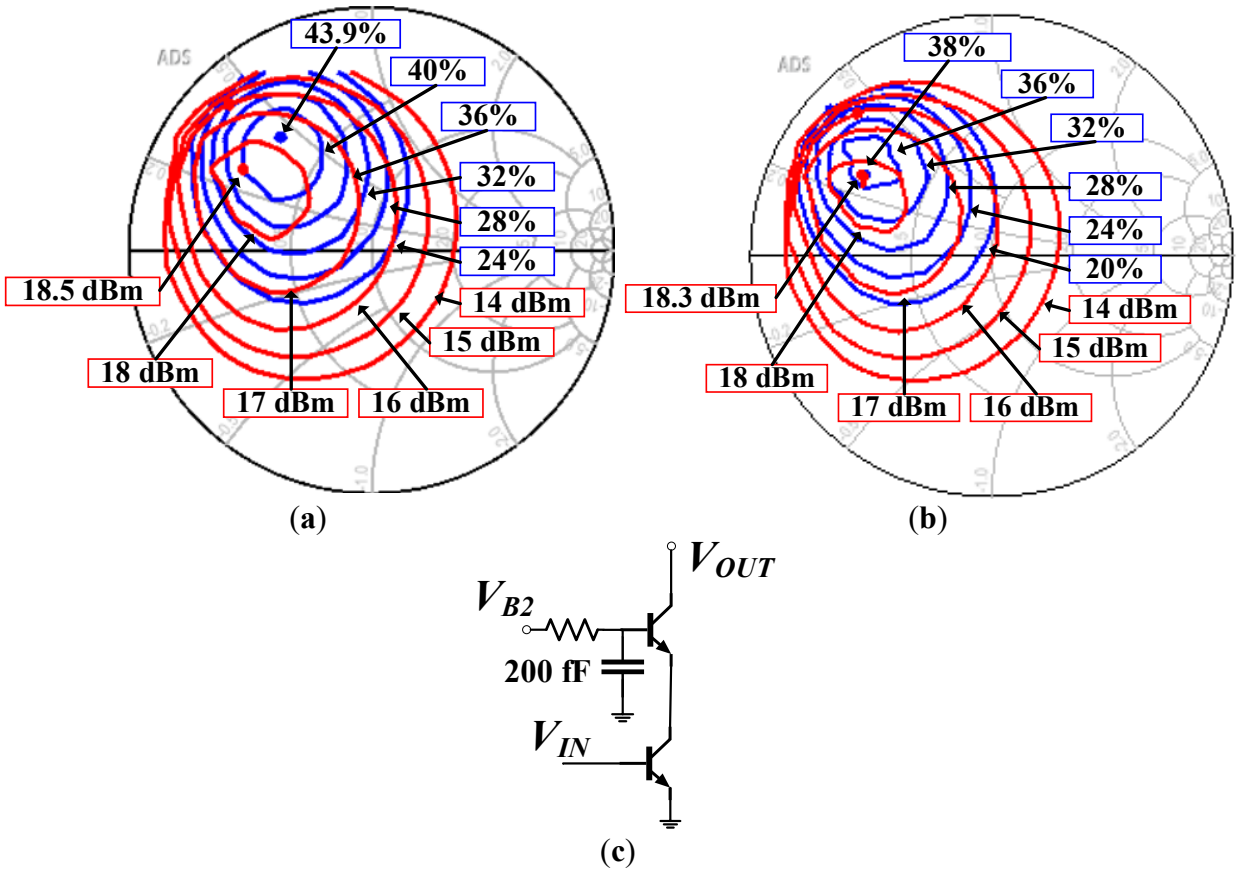


Figure 4.61: Load-pull Simulations at the Fundamental Frequencies

24 GHz (a); and (b) 37 GHz at around P_{1dB} of the (c) single-ended SiGe cascode 8 x 4 µm device pair (with a 200 fF capacitor on the cascode gate); assumed ideal on-chip ground.

Figure 4.62 shows the simplified PA schematic of a one-stage cascode SiGe PA, which uses a RC feedback path to help achieve broadband results. I_B is shown here as the base biasing current as it is being fed with an adaptive biasing circuit that can be switched on and off. All the simulations shown in this section will indicate the results of this PA when the adaptive bias switch is turned off and is thus similar to a fixed bias design. Thus, the adaptive biasing circuit is not shown here but will be shown later. All the simulations in this chapter use R+C+CC xRC parasitic-extraction (PEX) from Mentor Graphics' Calibre [60]. This SiGe PA design in simulation achieves max. S_{21} of 13.7 dB with a very good 3-dB BW of 13.3 – 57.1 GHz (absolute BW= 124.4%).

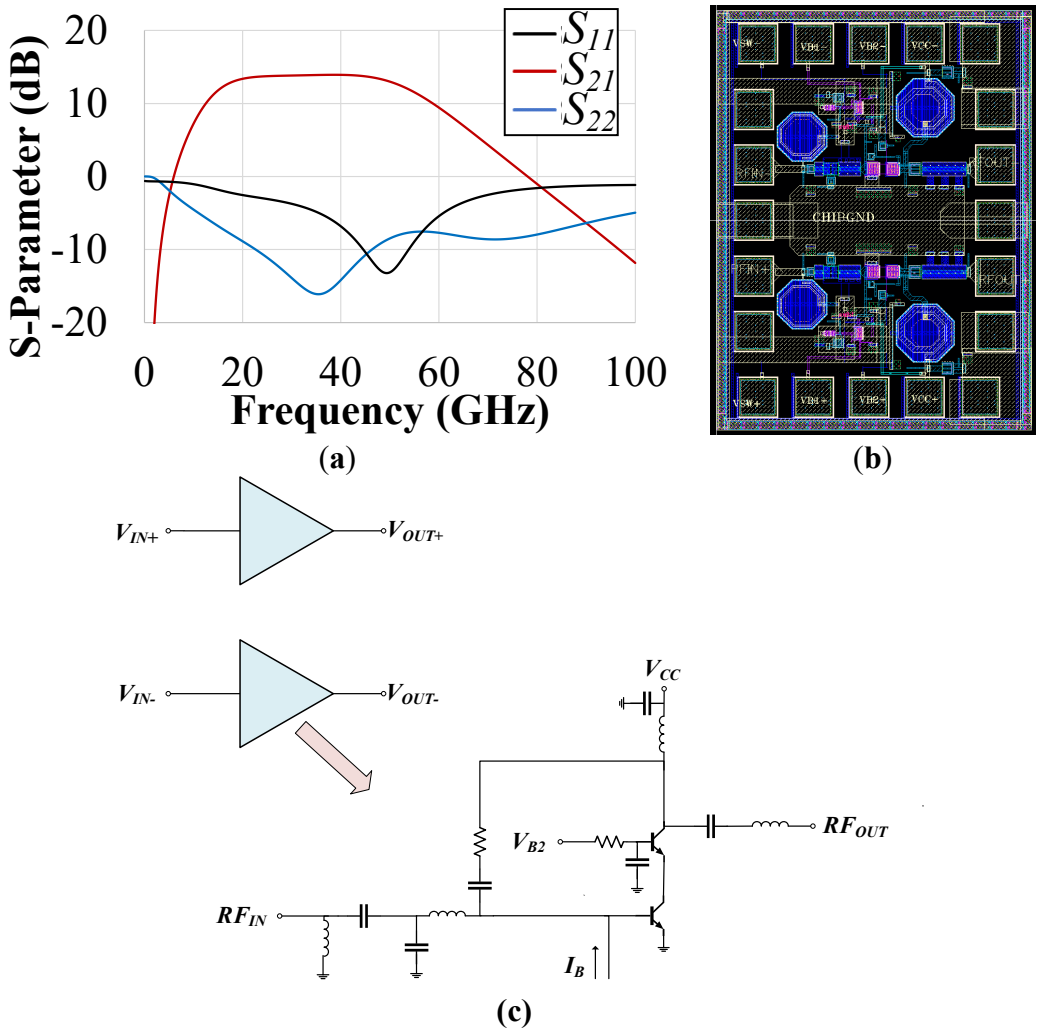


Figure 4.62: PEX Simulation of the S-parameters (a), (b) Layout and (c) Simplified Schematics of the Broadband Differential SiGe PA with RC Feedback

Figure 4.63 shows the large signal PEX simulation results of this PA, which suggests that it achieves a max. PAE of 33.4% at 18 GHz. Maximum saturated power of ~22 dBm is achieved, and the PA maintains within ~1 dB $P_{OUT,SAT}$ from 18 – 44 GHz. The large signal PEX results for this PA are summarized in Table 4.14.

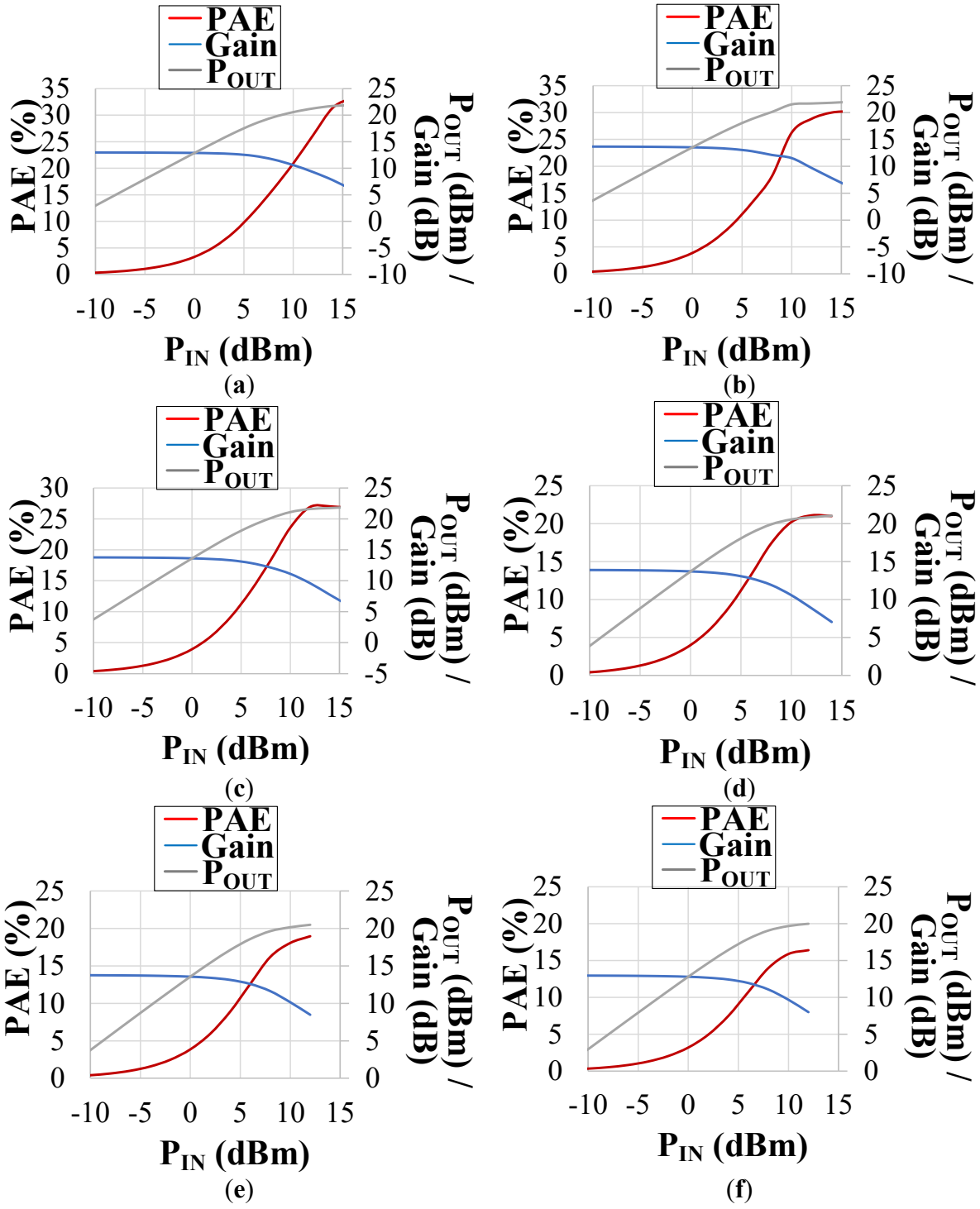


Figure 4.63: PEX Simulation data of the P_{IN} vs PAE, P_{OUT} and Gain for the Broadband SiGe PA with RC Feedback While the Adaptive Biasing Circuit is Turned off at (a) 18 GHz, (b) 24 GHz, (c) 28 GHz, (d) 39 GHz, (e) 44 GHz, and (f) 50 GHz

Table 4.14. Summary of Post-Layout PEX Simulations for the RC Feedback Broadband 9HP PA

Freq (GHz)	S_{21} (dB)	Max PAE (%)	PAE @ P_{1dB} (%)	$P_{OUT, SAT}$ (dBm)	OP_{1dB} (dBm)
18	13.0	33.4	13.9	21.9	18.9
24	13.7	30.3	13.2	22.0	18.8
28	13.8	27.0	13.4	22.0	18.9
39	13.9	21.1	13.2	21.1	18.8
44	13.8	19.0	12.6	20.7	18.6
50	13.0	16.4	10.7	19.7	17.9

4.4.1 Broadband SiGe PA with RC Feedback and Neutralization Capacitors

Next, the design from the previous section is taken and neutralization capacitors is added (Figure 4.64) to improve the maximum stable gain and reverse isolation [35]. This design's layout may not have been optimized as it should improve gain, but this work did not see those improved results in simulations as it achieves max. S21 of 12.5 dB. It does, however, provide a great 3-dB BW of 21.1 – 65.4 GHz (absolute BW = 102.4%). This may be due to the fact that this design is output matched for higher frequencies (i.e., higher than the frequencies of the design presented in 4.3.1).

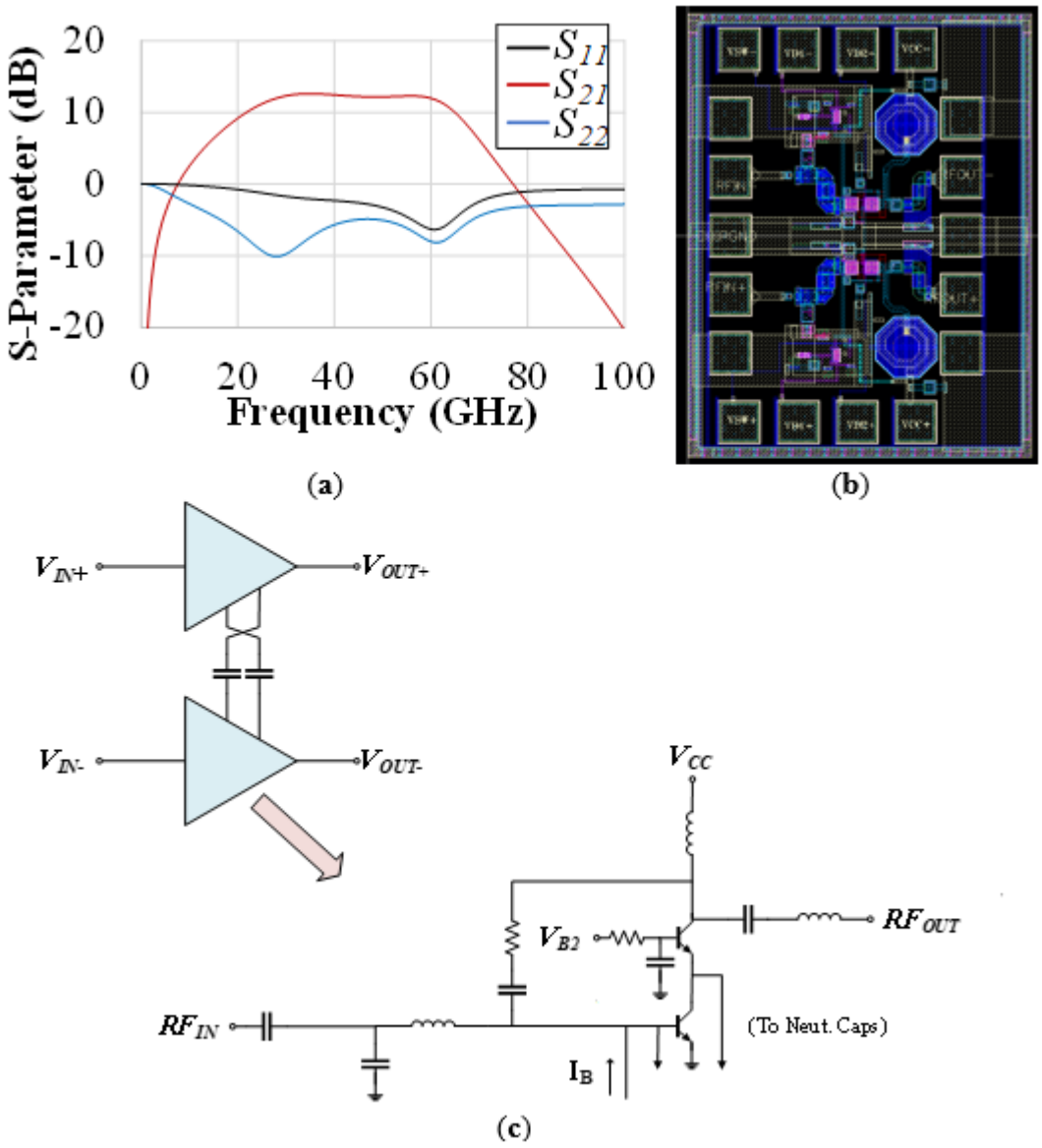


Figure 4.64: PEX Simulated S-parameters while the Adaptive Biasing Circuit is Turned off (a), (b) Layout and (c) Simplified Schematics of the Broadband Differential SiGe PA with RC Feedback and Neutralization Capacitors

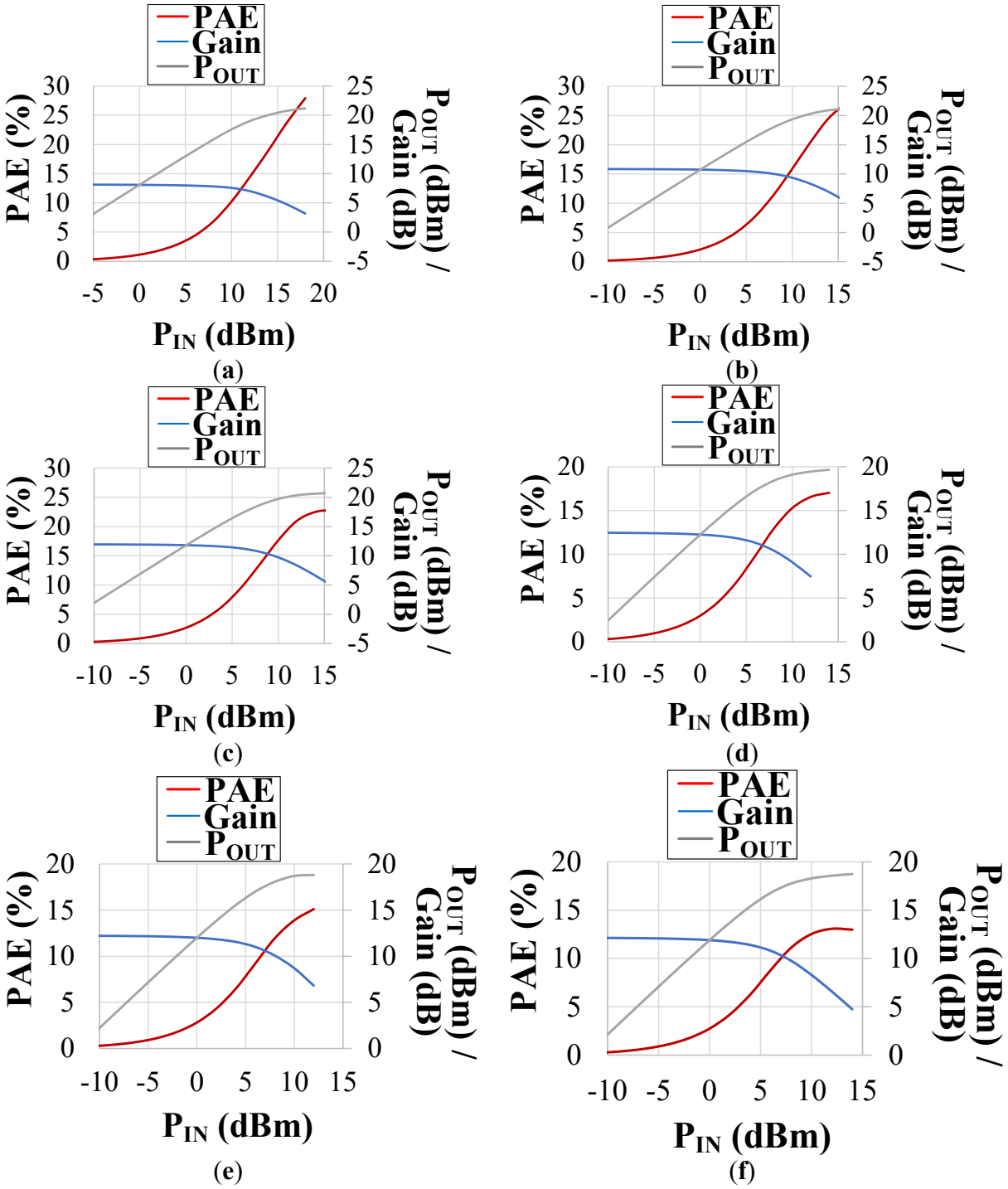


Figure 4.65: PEX Simulations of the P_{IN} vs PAE, P_{OUT} and Gain of the Broadband SiGe PA with RC Feedback and Neutralization Capacitors with the Adaptive Biasing Circuit turned off at (a) 18 GHz, (b) 24 GHz, (c) 28 GHz, (d) 39 GHz, (e) 44 GHz, and (f) 50 GHz

The PEX large signal simulations also show that the PA performance was degraded from the version without the neutralization capacitors. Max. PAE is achieved at 18 GHz for this design with a value of 27.9%, as opposed to the 33.4% for the version without the neutralization capacitors. Not only is the max. PAE performance degraded, but the large signal BW is also degraded as the 1-dB POUT,SAT BW reduces to ~18 – 39 GHz. The large signal results are summarized in Table 4.15, which also shows the large signal simulation results for the 22FDX design that uses RC feedback and neutralization capacitors for comparison reasons. This design achieves ~4 dB higher POUT,SAT but with lower max. PAE; however, this may be due to the design not being optimized. Gain is also lower for this design but achieves higher BW than that of the 22FDX design as presented in the previous section.

Table 4.15. Summary Table of PEX Simulation Data for the Broadband 9HP PA Using RC Feedback with Neutralization Capacitors vs. a Broadband 22FDX CMOS PA also Designed Using RC Feedback with Neutralization Capacitors

Tech.	Freq (GHz)	S_{21} (dB)	Max PAE (%)	PAE @ P_{1dB} (%)	$P_{OUT,\,SAT}$ (dBm)	OP_{1dB} (dBm)
9HP	18	8.2	27.9	14.5	21.2	19.0
	24	10.9	27.2	11.5	21.2	18.0
	28	12.0	22.9	11.6	20.8	18.0
	39	12.5	17.0	6.9	19.8	15.8
	44	12.2	15.1	6.5	18.8	15.5
	50	12.2	13.1	6.3	18.9	15.4
22FDX	20	14.0	24.4	14.4	17.0	13.0
	24	17.0	37.2	19.9	17.8	15.6
	39	15.0	21.6	12.5	17.1	13.9
	50	13.4	19.5	12.4	16.6	12.4

4.4.2 Broadband SiGe PA With 3rd-Order Input Matching and Neutralization Capacitors

The previous section showed a broadband SiGe PA designed using both RC feedback and neutralization capacitors in the 9HP process with very good $P_{OUT,\,SAT}$, while the gain was somehow not as high as this work had expected. In this section, therefore, this work remove the RC feedback while keeping the neutralization capacitors in the SiGe PA. This design achieves better max. S_{21} compared to both of the versions that use RC feedback with a value of 16.1 dB. This is to be expected as it does not have to sacrifice its gain to achieve higher BW like the RC feedback designs have to do. This same trend was also seen in the 22FDX designs. More importantly, it also achieves impressive 3-dB BW of 10.8 – 51.2 GHz (absolute BW of 130.3%) and thus achieves the best BW out of the three designs (the performance of the other two designs is tabulated in Tables 4.14 and 4.15).

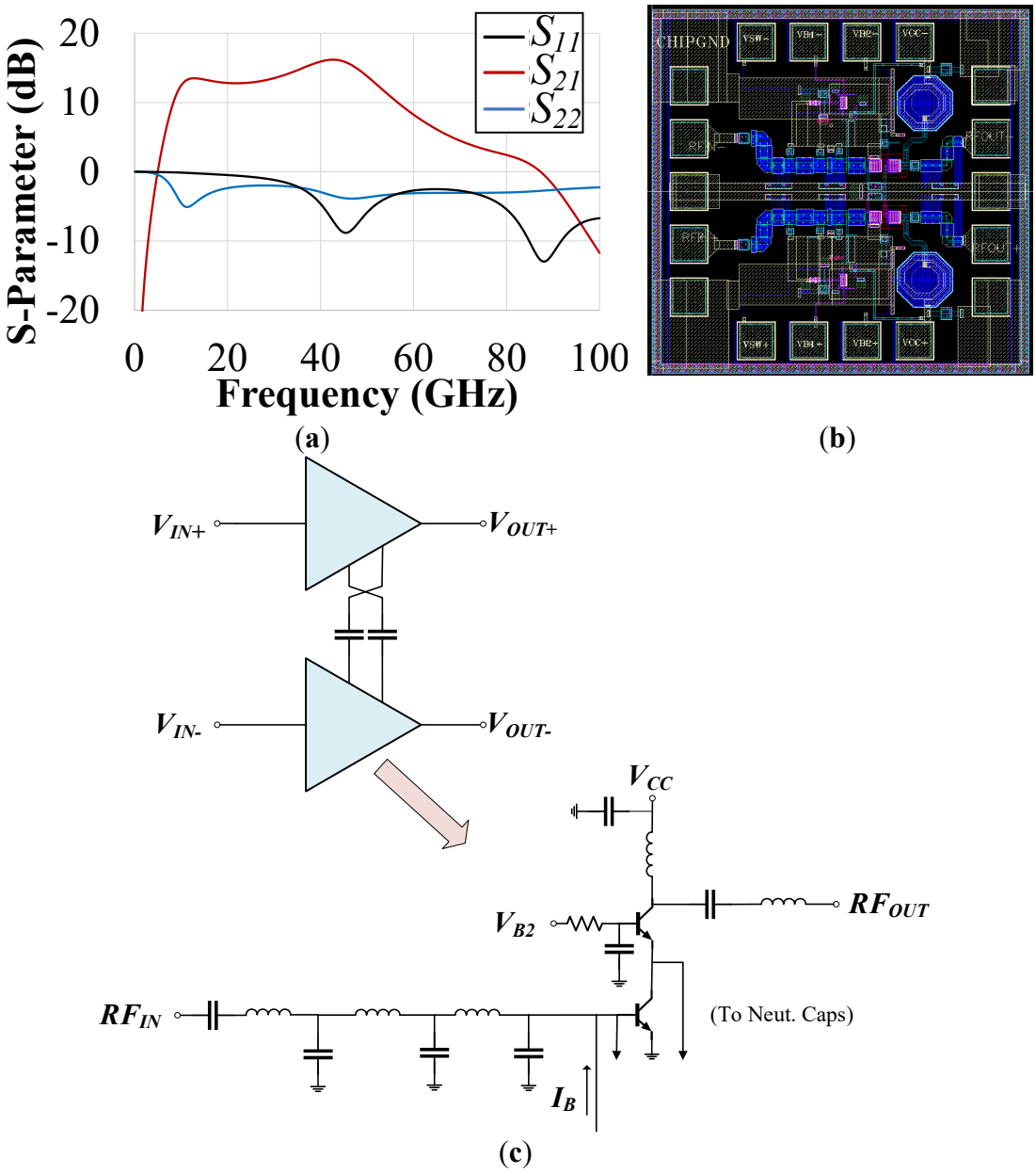


Figure 4.66: PEX Simulated S-parameters While the Adaptive Biasing Circuit is Turned off (a), Layout (b) and (c) simplified schematics of the Broadband Differential SiGe PA with 3rd-order Input Matching Network and Neutralization Capacitors, but without the RC Feedback

The large signal PEX simulations results for this PA are shown in Figure 4.67, which indicates that this PA achieves max. simulated PAE of 42.9% at 18 GHz, and thus this PA also achieves the best PAE out of all the PAs discussed in this chapter. Interesting, the 1-dB $P_{OUT,SAT}$ BW of this PA is the lowest out of the three PAs, as it achieves 1-dB $P_{OUT,SAT}$ BW of less than 18 – 39 GHz, likely due to having no RC feedback included. Table 4.16 shows a summary of the large

signal PEX simulations as well as the values from the 22FDX design that also uses a 3rd-order input matching network but also without the RC feedback. This SiGe design achieves higher PAE than that of the 22FDX design while also achieving better max. S_{21} and output power. This follows more of what would be predicted from the load-pull simulations. Comparing the data presented in Table 4.15 and Table 4.16, this work expect that broadband mm-Wave SiGe PA may still outperform their CMOS SOI PA counterparts on $P_{OUT,SAT}$ and maybe max. PAE. Measurement data is required to validate this point, though.

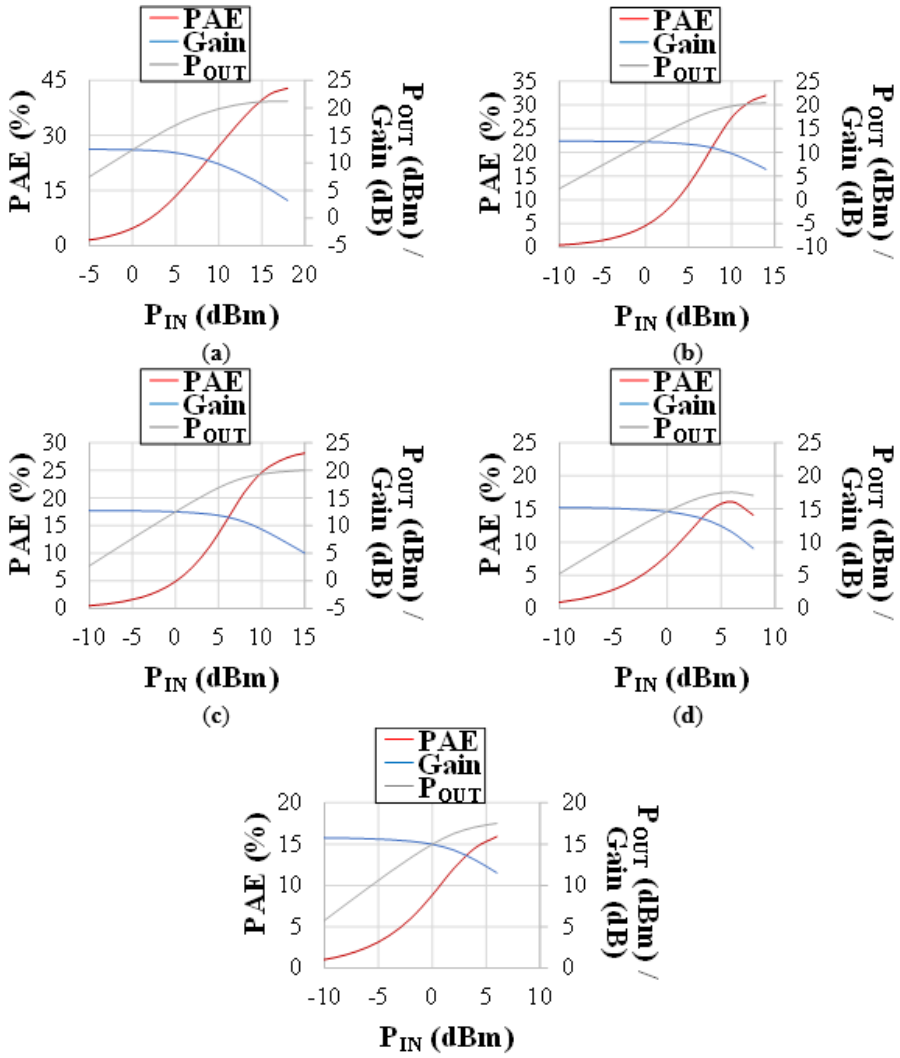


Figure 4.67: PEX Simulations of the P_{IN} vs PAE, P_{OUT} and Gain of the Broadband Differential SiGe PA with a 3rd-order Input Matching Network and Neutralization capacitors with no RC Feedback and the Adaptive Biasing Circuit Turned off at (a) 18 GHz, (b) 24 GHz, (c) 28 GHz, (d) 39 GHz, and (e) 44 GHz

Table 4.16. Summary of PEX Simulation Results for the Broadband SiGe PA Designed vs. a Broadband CMOS PA Both Designed using 3rd-Order Input Matching Network with Neutralization Capacitors

Tech.	Freq (GHz)	S_{21} (dB)	Max. PAE (%)	PAE @ P_{1dB} (%)	$P_{OUT,\,SAT}$ (dBm)	OP_{1dB} (dBm)
9HP	18	13.0	42.9	16.0	21.2	17.6
	24	12.8	32.1	15.9	20.5	17.6
	28	13.2	28.4	16.1	20.3	17.6
	39	15.7	16.1	11.5	17.7	16.1
	44	16.1	15.9	8.8	17.5	15.0
22FDX	20	13.9	36.6	26.4	18.1	16.4
	30	14.8	28.4	13.9	17.4	13.9
	40	13.5	21.2	6.8	16.6	12.1
	50	11.7	13.1	4.2	15.0	8.4

4.4.3 Adaptive Biasing Techniques for Linearity Enhancement in broadband SiGe PAs

Similar to what this work had been done with the 22FDX design, an adaptive biasing circuit is implemented in the 9HP process. As these designs use BJTs, the adaptive biasing circuitry will be fundamentally different where a base current is required, instead of supplying only a voltage to the gate of a MOSFET. Like what had been discussed in the 22FDX chapter, this circuitry allows the PA to be biased colder at lower RF input powers for better PAE at power back-off and biases the PA hotter as the RF power increases where linearity is more important. Unlike other PA topologies that improve PAE at power back-off while being naturally narrowband (e.g., Doherty PAs), several works have shown that the addition of an adaptive biasing circuit for a broadband PA can keep the PA still quite broadband [68, 69]. Since the IC vs. VBE is exponential for a BJT, this adaptive biasing circuit may not need to have as much of a change in VBE vs. RF PIN than that of the 22FDX adaptive biasing circuit to be effective. Figure 4.68 shows the circuit implemented in this design, which is based off the basic ideas presented in [68]; however, switches are added to this design with significant modifications vs. what is reported in [69] so that the adaptive biasing can be turned on and off. As PIN increases, the RF voltage signal goes up into the emitter of Q1 and is rectified at the base of Q1. After rectification, DC current through Q1 becomes higher, causing the voltage VCE across Q1 to decrease and VBE of the power amplifying device (Q4) to increase. RF is leaked through the capacitor C, and Q2 and Q3 to supply constant DC voltage to the base of Q1 and the PA device. Figure 4.68 (b) is the VBE of the PA device as PIN increases with the switch on and off, which shows that in the adaptive biasing state, the voltage at the base of the amplifying device increases with input power. Note that to see these significant adaptive biasing results, the bias at the base of the PA device only increases by ~35 mV whereas the 22FDX adaptive biasing circuit needed to increase by ~200 mV. The designs in this section are the same designs as the ones in the fixed bias versions from the previous sections but with the adaptive biasing switch turned on.

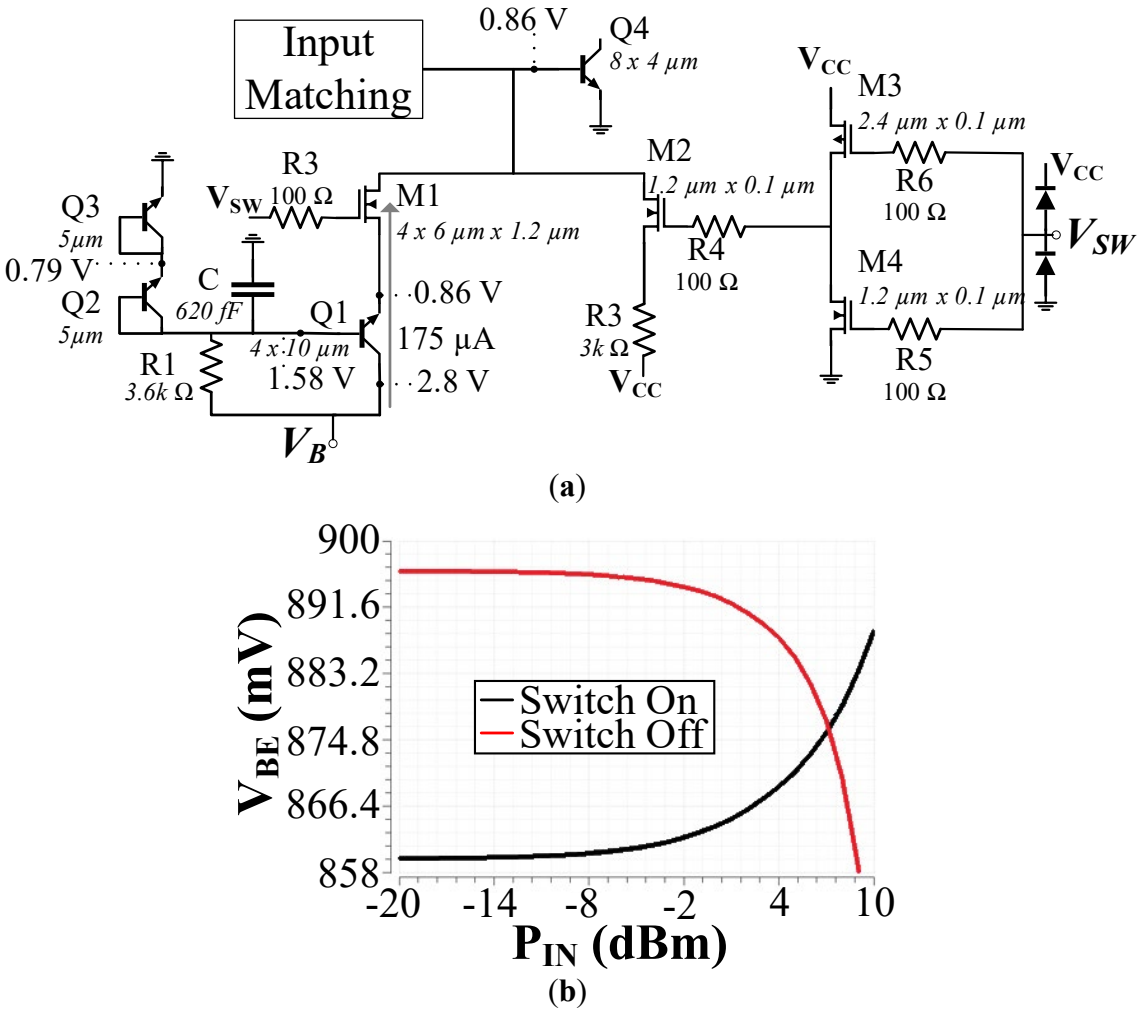


Figure 4.68: Schematic of the SiGe Adaptive Circuit 9 (a) and (b) Voltage vs. P_{IN} at the Input of the Power Amplifying Device (Q4)

4.4.3.1 Broadband SiGe PA With RC Feedback

The small signal BW of the differential broadband SiGe PA with RC feedback (but no neutralization caps) is not degraded when the adaptive biasing is turned on, with 3-dB BW of 12.9 – 54.7 GHz (absolute BW of 123.7%) as shown in Figure 4.69. The maximum power gain, though, is degraded with the adaptive biasing turned on, as it achieves max. S21 of 12.0 dB.

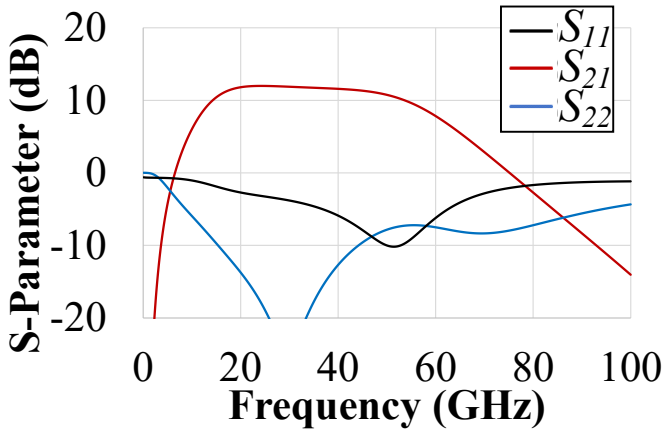


Figure 4.69: PEX Simulated S-parameters of the Broadband Differential SiGe PA with RC Feedback with the Adaptive Biasing Circuit Turned On

With the switch turned on for the adaptive biasing, this PA does experience some degradation in the max. PAE as it achieves max. PAE of 32% at 18 GHz, as shown in the large signal PEX simulations shown in Figure 4.70. However, the PAE@P1dB is greatly improved across the whole frequency band (Figure 4.71). The best improvement is at 18 GHz, which improves from 13.9% to 30.2%. There is ~ 1-dB improvement in the OP1dB across the BW. The results of the simulations are summarized in Table 4.17. This 9HP broadband PA version (with RC feedback) does have the largest increase in the PAE@P1dB compared to all of the other PAs that use adaptive biasing in this present work.

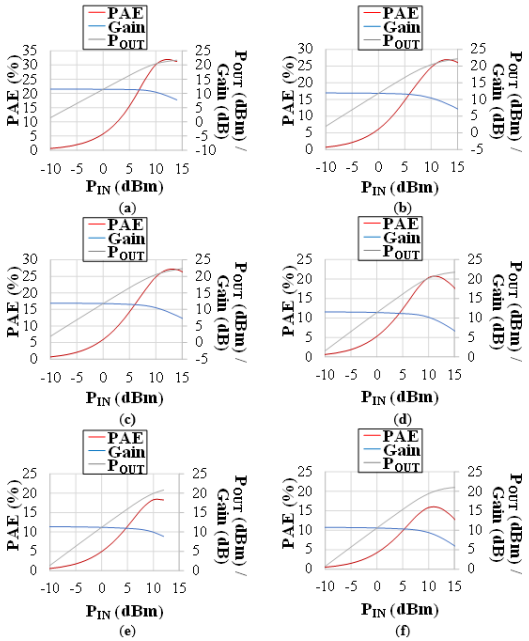


Figure 4.70: PEX Simulations of the P_{IN} vs PAE, P_{OUT} and Gain of the Broadband Differential SiGe PA (using RC feedback) with the Adaptive Biasing Circuit Turned on at (a) 18 GHz, (b) 24 GHz, (c) 28 GHz, (d) 39 GHz, (e) 44 GHz, and (f) 50 GHz.

Table 4.17. Comparison Table of PEX Simulations for the Adaptive Biased Broadband Differential SiGe PA with RC Feedback for Switch on vs. Switch Off

Switch	Freq (GHz)	S_{21} (dB)	Max PAE (%)	PAE @ P_{1dB} (%)	$P_{OUT, SAT}$ (dBm)	OP_{1dB} (dBm)
ON	18	11.5	32.0	30.2	22.0	20.5
	24	12.0	26.7	22.5	22.4	19.8
	28	11.9	27.0	22.9	22.5	19.9
	39	11.6	20.6	17.8	21.9	18.8
	44	11.4	18.3	16.3	20.8	18.6
	50	10.8	15.8	15.0	21.1	18.7
OFF	18	13.0	33.4	13.9	21.9	18.9
	24	13.7	30.3	13.2	22.0	18.8
	28	13.8	27.0	13.4	22.0	18.9
	39	13.9	21.1	13.2	21.1	18.8
	44	13.8	19.0	12.6	20.7	18.6
	50	13.0	16.4	10.7	19.7	17.9

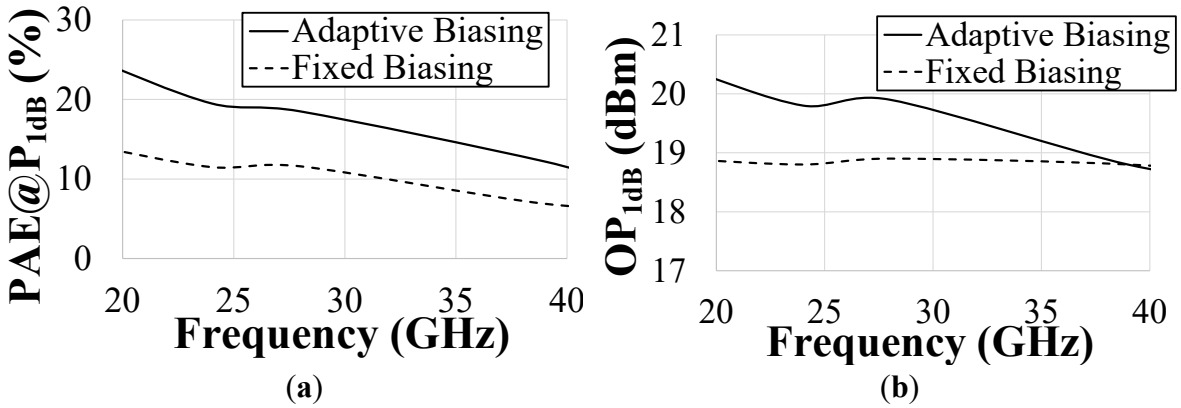


Figure 4.71: PEX Simulations (a) PAE@P_{1dB}, and (b) OP_{1dB} vs. Frequency with the Adaptive Biasing Circuit Turned on and Off of the Broadband Differential SiGe PA *with RC feedback*

4.4.3.2 Broadband SiGe PA With RC Feedback and Neutralization Capacitors

Next, this work will discuss the differential broadband SiGe PA design that utilizes both RC feedback and neutralization capacitors with the adaptive biasing turned on. The small signal gain is once again degraded when the adaptive biasing circuit is turned on in this broadband SiGe PA as shown in Figure 4.72. This PA achieves max. S21 of 10.0 dB with 3-dB BW of 17.9 – 65.7 GHz (absolute BW of 114.4%) in PEX simulaion, so the BW does not degrade when the adaptive biasing switch is turned on.

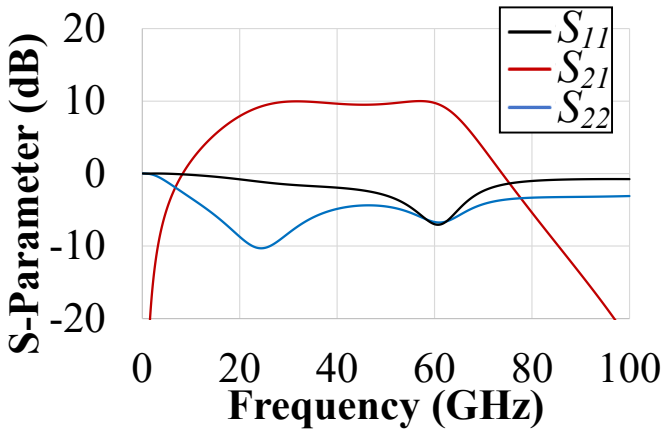


Figure 4.72: PEX Simulated S-parameters of the Broadband Differential SiGe PA with RC Feedback and Neutralization Capacitors with the Adaptive Biasing Circuit Turned on

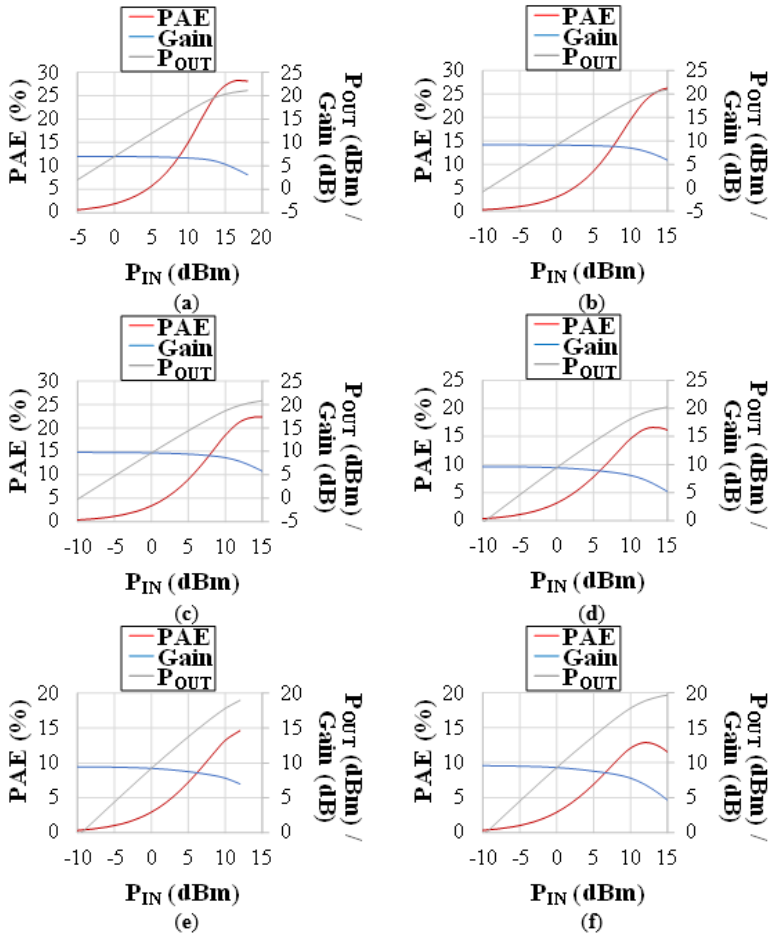


Figure 4.73: PEX Simulations of the PAE, P_{OUT} and Gain vs. P_{IN} of the Broadband Differential SiGe PA with RC Feedback and Neutralization Capacitors when the Adaptive Biasing Circuit Turned on at (a) 18, (b) 24, (c) 28, (d) 39, (e) 44, and (f) 50 GHz

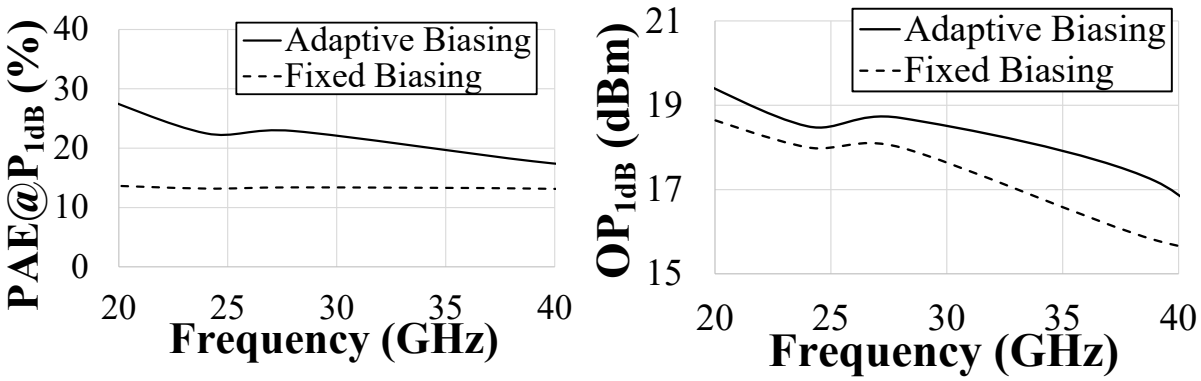
This adaptive biasing circuit is able to improve the PAE@P_{1dB} while not degrading the max. PAE for this version, and the large signal PEX simulations are shown in Figure 4.73. Table 4.18 shows a summary of the large signal PEX simulations. Interestingly, the PAE@P_{1dB} improves by ~10% at 18 GHz, but it did not improve as much as compared to the version with RC feedback only (cf. Table 4.17), especially at higher frequencies. However, the version using no neutralization capacitors did not improve OP_{1dB} much, while the OP_{1dB} did improve with the adaptive biasing circuit turned on for this design by ~ 1 dB as shown data in Figure 4.74). The similarly designed 22FDX CMOS PA with its adaptive biasing circuit is also shown in Table 4.19 (note a small difference is that the 22FDX PA does not include a switch to turn on and off the adaptive biasing circuit; so, the adaptive biasing is always on). Nonetheless, this SiGe PA achieves comparable PAE@P_{1dB} to that of the 22FDX PA at lower mm-Wave frequencies and is able to improve OP_{1dB} more than the 22FDX version, and with higher $P_{OUT, SAT}$.

Table 4.18. Comparison Table of the PEX Simulations for the Adaptive Biased Broadband Differential SiGe PA with RC Feedback and Neutralization Capacitors for Switch on vs. Switch Off

Switch	Freq (GHz)	S_{21} (dB)	Max PAE (%)	PAE @ P_{1dB} (%)	$P_{OUT, SAT}$ (dBm)	OP_{1dB} (dBm)
ON	18	7.1	28.1	25.8	21.1	19.9
	24	9.2	26.3	19.5	21.5	18.5
	28	9.8	22.3	18.5	21.4	18.7
	39	9.7	16.5	12.2	20.7	17.2
	44	9.5	14.7	8.4	19.0	14.6
	50	9.6	12.9	8.0	20.0	14.6
OFF	18	8.2	27.9	14.5	21.2	19.0
	24	10.9	27.2	11.5	21.2	18.0
	28	12.0	22.9	11.6	20.8	18.0
	39	12.5	17.0	6.9	19.8	15.8
	44	12.2	15.1	6.5	18.8	15.5
	50	12.2	13.1	6.3	18.9	15.4

Table 4.19. Summary of PEX Simulations for the Adaptive Biased Broadband Differential SiGe PA with RC Feedback and Neutralization Capacitors vs. Similarly Designed Adaptive Biased 22 nm CMOS SOI PA

Tech.	Freq (GHz)	S_{21} (dB)	Max PAE (%)	PAE @ P_{1dB} (%)	P_{SAT} (dBm)	OP_{1dB} (dBm)
9HP	18	7.1	28.1	25.8	21.1	19.9
	24	9.2	26.3	19.5	21.5	18.5
	28	9.8	22.3	18.5	21.4	18.7
	39	9.7	16.5	12.2	20.7	17.2
	44	9.5	14.7	8.4	19.0	14.6
	50	9.6	12.9	8.0	20.0	14.6
22FDX	20	7.8	14.3	13.9	16.2	14.7
	24	13.6	36.3	29.2	17.8	14.4
	39	11.4	20.2	20.2	16.9	15.9
	50	9.2	12.7	12.6	16.0	14.6



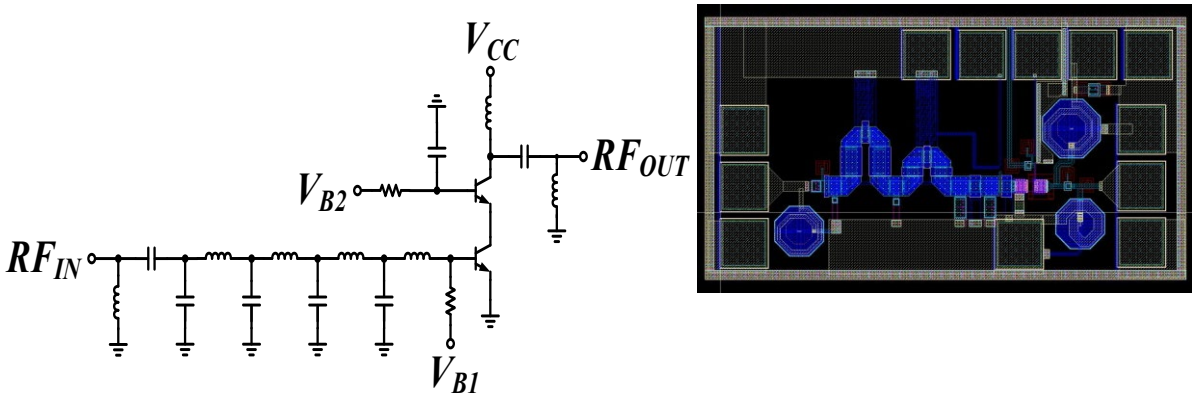
(a) (b)

Figure 4.74: PEX Simulations of (a) PAE@P_{1dB}, and (b) OP_{1dB} vs. Frequency with the Adaptive Biasing Circuit Turned On and off of the Broadband Differential SiGe PA with RC Feedback and Neutralization Capacitors

4.4.4 SiGe Earlier Works

Previously, single ended versions of some of the SiGe PAs were designed. However, at these frequencies, the ground node is very important and even a small reactance from the emitter to the ground can greatly degrade the performance especially on gain [70] (e.g., at 50 GHz, a 1 nH parasitic inductance from the ground bondwire has a high impedance of ~300 ohm, which is no longer a ground). Nonetheless, a single-ended version is presented in this section for discussions to show how it helped shape the differential SiGe PA designs that were shown in previous sections. In addition, this PA has measurement data and thus is reported here to show the degradation in the performance from simulations where an ideal emitter ground was assumed. Figure 4.75 shows the simplified PA schematic of a one-stage single-ended cascode SiGe PA

which uses 5th-order input matching. With V_{CC} = 2.4 V, V_{B1} = 0.9 and V_{B2} = 2.05, the PEX simulations (assuming again an ideal emitter to ground) suggests good S_{21} of 14 – 17 dB with reasonable S_{11} and S_{22} from 18 – 46 GHz (Figure 4.76).



(a) (b)

Figure 4.75: Simplified Schematics of the Broadband Single-ended cascode SiGe PA with 5th-order Input Matching Network (a); and (b) its Layout of 1085 µm *x* 581 µm

In this work, we assume again an ideal emitter to ground and ignore all ground parasitics (say, with a very large through-silicon-vias array connecting to an excellent ground outside the chip), this single-ended PA achieves its max. PAE of 36.8% at 30 GHz from PEX simulations. Figure 4.76 and Table 4.20 presents PEX simulation of the single-ended SiGe PA. In addition, the $P_{OUT,SAT}$ and max. PAE are plotted versus frequency, which shows that this PA is quite broadband in simulation. For instance, the peak PAE is above 22% for the frequency range 20 – 50 GHz.

Table 4.20. Summary of PEX Simulations for the Single-Ended Broadband SiGe PA with 5th-Order Input Matching and Parasitic Inductance Ignored

Freq (GHz)	S_{21} (dB)	S_{11} (dB)	Max PAE (%)	$P_{OUT,SAT}$ (dBm)	OP_{1dB} (dBm)
20	14.8	-4.2	24.8	18.4	12.7
35	16.4	-7.7	36.4	18.8	15.7
50	12.8	-19.6	22.1	16.8	14.7

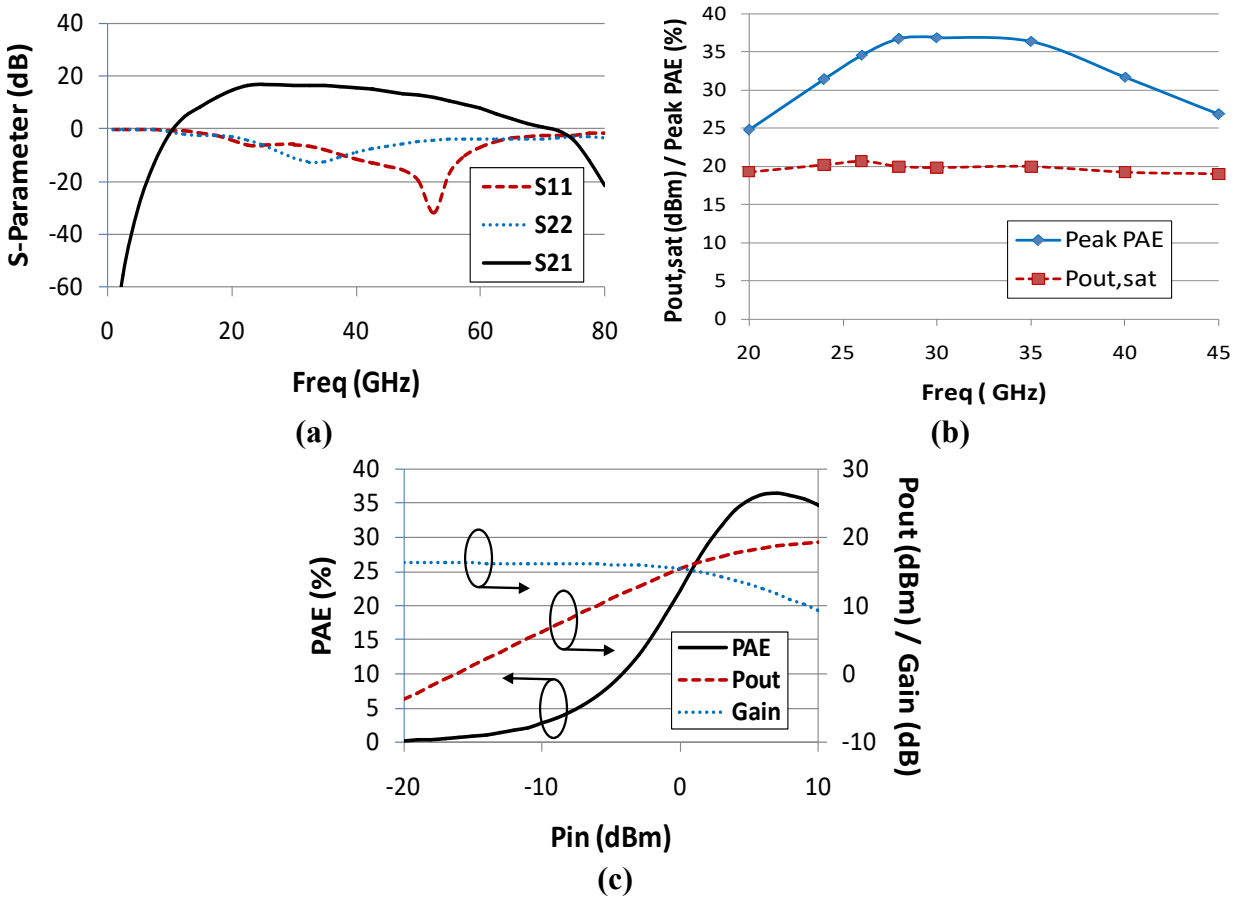


Figure 4.76: Broadband Single-ended cascode SiGe PA PEX Simulation

Small-signal (a), (b) max. PAE, $P_{OUT,\,SAT}$ vs. frequency and (c) large-signal P_{IN} vs. PAE, gain, P_{OUT} at 37 GHz. Note these PEX simulations assumed an ideal emitter to ground, thus ignoring all practical ground parasitics from on-chip interconnect to on-chip ground pad, and the ground parasitics connecting from chip-ground to external off-chip ground.

Measurements were taken on this PA and are shown in Figure 4.77. There is an obvious large degradation in the performance in both gain and BW from measurement vs. PEX simulation. The large signal measurement results also show a huge degradation from simulation and this PA only achieves a peak PAE of ~9%. The higher frequencies see a larger degradation in performance, which is most likely due to the PEX simulations ignoring all practical ground parasitics such as on-chip interconnect (i.e., from the emitter to the on-chip ground pad), and the ground parasitics connecting from the chip-ground to external off-chip ground (e.g., bondwires). For example, if there are large distances between the emitter of the CE device to the ground pad on-chip, this will add some parasitic inductance with more impedance to the ground node, degrading the gain. At lower frequencies, this distance will not be as important compared to higher frequencies, as the reactance is higher for the same inductance value at higher frequencies. Although the RF ground is probed with the GSG probes, this distance is still a lot longer than if a differential configuration is used, as in that case the ground is moved to the

common ground point shared by the differential pair. Thus, after this design, this work opted for a differential configuration. Unfortunately, this work still had issues with performance as described next.

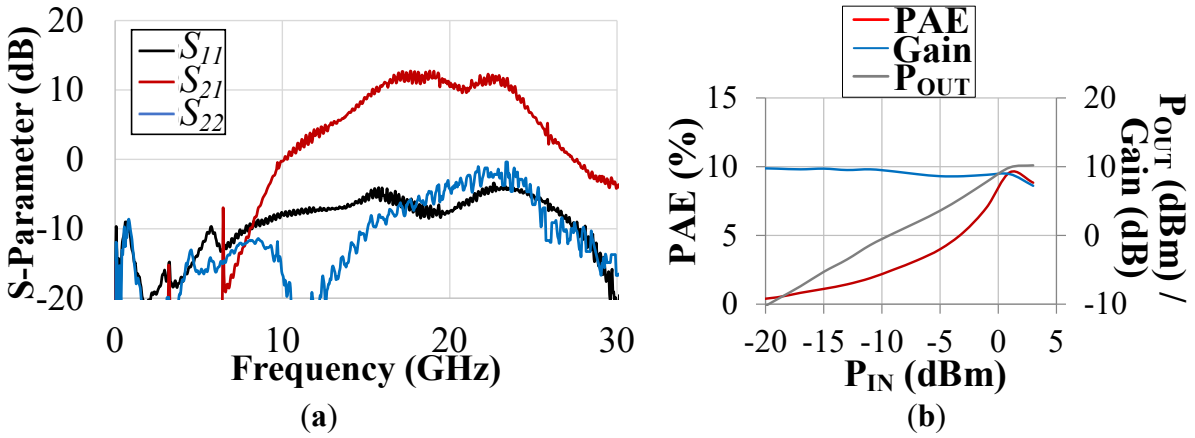


Figure 4.77: Measured S-parameters (a) and (b) Large Signal Measurements at 18 GHz of the Broadband Single-ended Cascode PA

The next error this work found in these SiGe PA designs was most likely due to a tiedown connection error, which were used in the hopes of passing the foundry's DRC (design rule checks). This work found this out after the differential SiGe PA designs were fabricated and shipped to us, and GF informed us that there were some high-density dual MIM (metal-insulator-metal) capacitors that could be shorted and asked us to check to see if the capacitors were indeed shorted. Using the setup shown in Figure 4.68, shorted capacitors were tested for. The V_{CC} pad is connected to the positive of a supply connected and then the RF_{OUT} pad to the other end of a supply. If the capacitors are shorted, then the DC blocking capacitor at the output of the PA would allow the current to flow. Instead of showing a short, it has an I-V curve showed in Figure 4.79, so a PA with a similar output configuration from a different MPW (multi-project wafer) tapeout was also tested to check these results. However, the previous tapeouts also showed this undesired current flow. In addition, GF had informed us that the capacitor that had the short was the dual-MIM capacitor, which is a different type of capacitor from what this work have been using. Thus, this current being drawn must have been coming from something else, and this work believe this work have found this design error, which will be explained below.

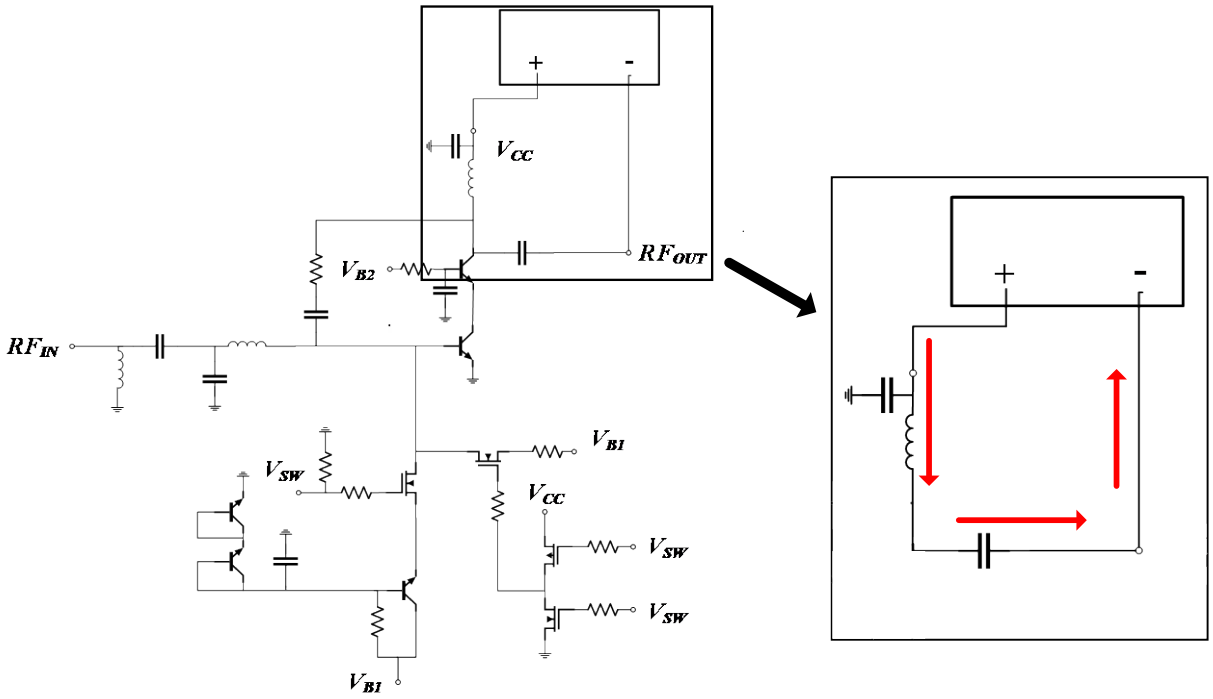


Figure 4.78: Schematic of the Setup used to check if the Capacitors had Shorts, Especially the One Connecting to the RF_{OUT} Node

To get rid of a DRC error, on each side of a capacitor, a tiedown was added. Unfortunately, the wrong polarity of the tiedown diode was used, and with a positive voltage, this diode was forward biased (Figure 4.69). To check this, the I-V curve of the tiedown model is shown in Figure 4.69 and it matches well with the odd I-V curve described above. The designs presented in 4.3.1, 4.3.2 and 4.3.3 have this tiedown issue but nonetheless are presented in this work as a comparison against the 22FDX PAs, as well as for comparisons against different topologies. This work believe, however, just like this work were able to fixed the ESD/oxide short issues to achieve good measurement data for CMOS PA as described in Section 4.2, this work have found all the errors of these SiGe PA design and expect to get reasonable measurement SiGe PA data once the latest MPW SiGe PA returned in a few more months.

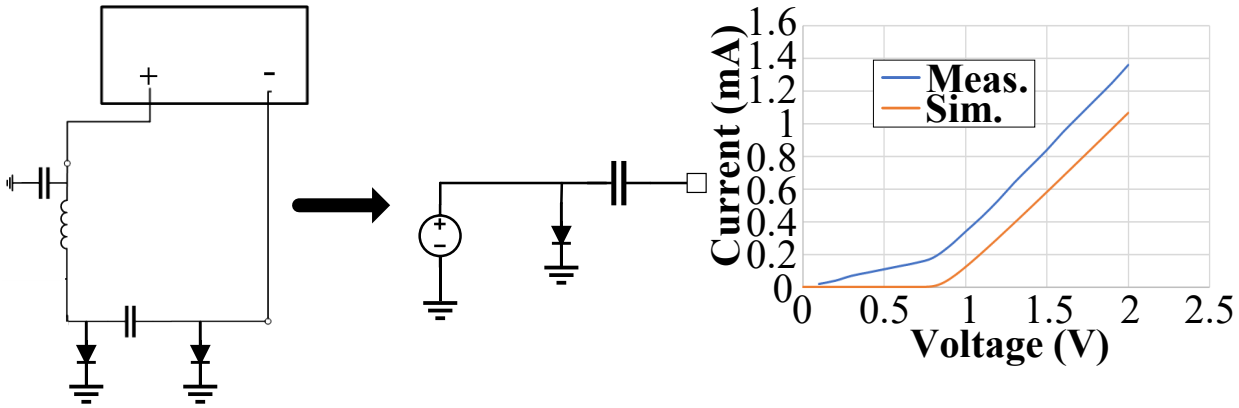


Figure 4.79: Schematic to Run the I-V Curve for the Tiedown Model (a) and (b) the I-V Curve of the Tiedown Model and the Measured I-V Curve from Biasing the V_{CC} Pad to the RF_{OUT} Pad

4.4.5 SiGe Conclusion

In this chapter, several different broadband SiGe PAs designed in GF's 9HP were discussed. In general, these PAs follow the same trend that this work saw in the CMOS FD-SOI PAs that using RC feedback degrades the performance, while achieving better BW compared to higher order input matching networks. In addition, in PEX simulations, these PAs achieved higher $P_{OUT,SAT}$ than those of the corresponding 22FDX CMOS PAs. A switchable adaptive biasing network was also designed and added to the SiGe PAs and it did show that it could improve the PAE at power back-off. However, measurement is needed to validate these results. In the process of taking data for these PAs, this work found many problems that have all been fixed in the newest tapeout, and are currently being tested.

4.5 Disucssions of Broadband Mm-Wave PAs designed in Silicon vs. III-V technologies

Throughout this present work, medium-power broadband mm-Wave PAs designed from several different semiconductor technologies have been discussed, as each technology its own intrinsic characteristics of output power, frequency response and passive performances. Generally, wide-bandgap III-V technologies have higher breakdown voltages and larger carrier transport mobilities compared to silicon technologies. In addition, III-V technologies tend to also provide better on-chip passives, due to the thicker process layers and their semi-insulating substrates. This is crucial for the high Q needed to achieve great power efficiencies and on-chip EM structures (e.g., baluns). However, silicon technologies offer more integrability and significantly lower costs, with the possibility for a one-chip solution and reducing the need for SiP (system-in-package) or heterogeneous integration. Thus, if performance specifications can be met with silicon processes, it may be advantageous to push for silicon-based PA products, especially for commercial uses. Thus, in this chapter, a closer comparison of the medium-power mm-Wave PAs designed in 22FDX technology vs. those designed in the HRL T3 GaN technology is presented and design trade-offs will be also discussed.

The GaN PDK (process design kit) used for comparison is that which is used earlier in this section, which is HRL Laboratories' T3 40 nm GaN HEMT (High Electron Mobility Transistor) technology on a SiC substrate. This technology achieves impressive V_{BR} of 50 V, f_T of 220 GHz and f_{MAX} of 400 GHz with a knee voltage of ~2 V, and $I_{D,MAX}$ of ~1.6 A/mm [24]. This 40 nm GaN technology will be used in a single-ended PA design (i.e., GaN PA #1) as well as a differential design (i.e., GaN PA #2) that were mentioned in earlier, but more details will be described here.

The fixed bias, differential cascode PA with RC feedback from the Section 4.2 used GlobalFoundries' 22FDX technology, which is a 22 nm FD-SOI (fully-depleted SOI) CMOS process. Devices in this technology achieve lower off-state leakage current due to the buried oxide layer and a fully depleted channel [71]. Our design uses SLVTNFET (i.e., super low threshold voltage NFET), which can achieve a peak f_T of ~350 GHz and peak f_{MAX} of ~370 GHz in the smallest device. The 22FDX technology also enables back-gate biasing, allowing to control the FET's threshold voltage (V_T) by back-gate to reduce off-state leakage current and/or adjust for V_T variation (from poly CD and short-channel effects), and can thus improve the performance and yield for nm-CMOS and possibly improve linearity as well [72].

Figure 4.80 shows the simulated f_T and f_{MAX} of the 40 nm GaN HEMT and 22 nm CMOS FD-SOI devices used in our mm-Wave PA designs. Although the 22FDX PDK offers PCell layouts up to mid-level metal layers, the parasitics up to the top metal layer are extracted using Calibre xACT R+C+CC extraction [4]. Here f_T and f_{MAX} are extrapolated from when H_{21} (small-signal current gain) and the value of G_{MAX} (maximum transducer power gain) are equal to unity, respectively (note: $G_{max} = |\frac{S_{21}}{S_{12}}|(K - \sqrt{K^2 - 1})$). For a fixed current density, it is clear from Figure 4.80(b) that f_{MAX} of the GaN device is much higher than those of the CMOS (by ~x2), suggesting it might be more suitable for low-power operations, even though Figure 4.80(a) also shows CMOS can reach about the same f_{MAX} as the GaN device at higher bias current (i.e., > 10 mA).

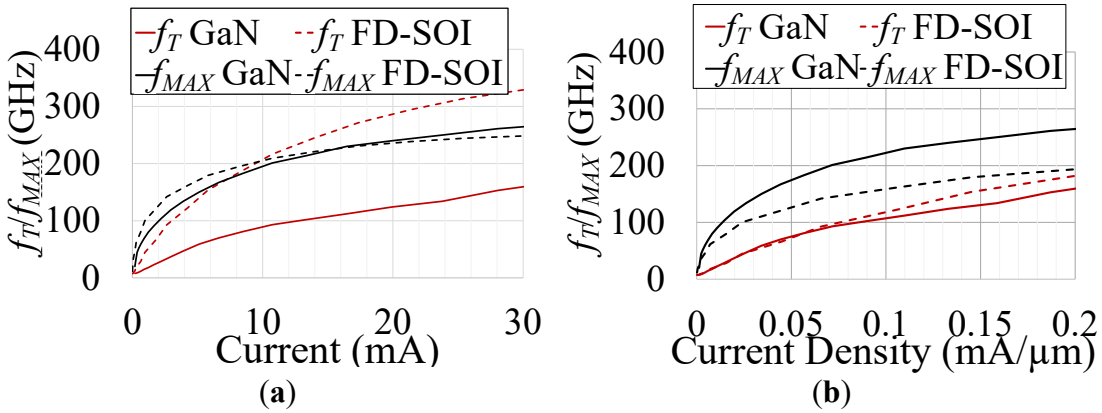


Figure 4.80: Simulated f_T and f_{MAX} of the 40 nm GaN HEMT (4 *x* 37.5 μm) and 22 nm CMOS FD-SOI (2 *x* 20 μm) PA Power Transistors with Parasitics Extracted to the Top Metal Layer and Plotted vs. (a) bias Current (mA); and (b) Current Density (mA/μm)

In each of the two technologies, this work have designed a differential PA, using neutralization capacitors to increase the maximum stable power gain (MSG) and reverse isolation, such as what had been discussed in Chapter 3. This technique has been explored in many previous works [5, 6] and in Chapter 3 and thus will not be discussed in detail in this chapter. The key is that the parasitic gate to drain capacitance, C_{gd}, can be reduced by adding the neutralization capacitor C_N, and thus the MSG of a differential amplifier can be increased [73, 74].

4.5.1 Design Methodology

Different design techniques and methodologies were explored using these two technologies to achieve very broad BW with good broadband PAE performance. For example, a high-order input matching network (i.e., 3rd-order) has been used for the GaN technology, which improves the BW by adding additional zeros and poles to the PA's transfer function. In the CMOS PA, RC feedback is utilized, which improves the BW with a small sacrifice to the maximum gain with feedback and by also adding an additional pole to the transfer function.

Load-pull simulations are done in both technologies to help designing these broadband PAs. For broadband operation, it is desirable to have the device's optimum load for PAE near 50 Ω so that minimal impedance transformation is needed, reducing the number of lossy components to realize the narrow-band impedance transformation. In addition, it would be great to have a very small reactance at the device's optimum load to minimize frequency dependence in the impedance matching to achieve excellent broadband performance.

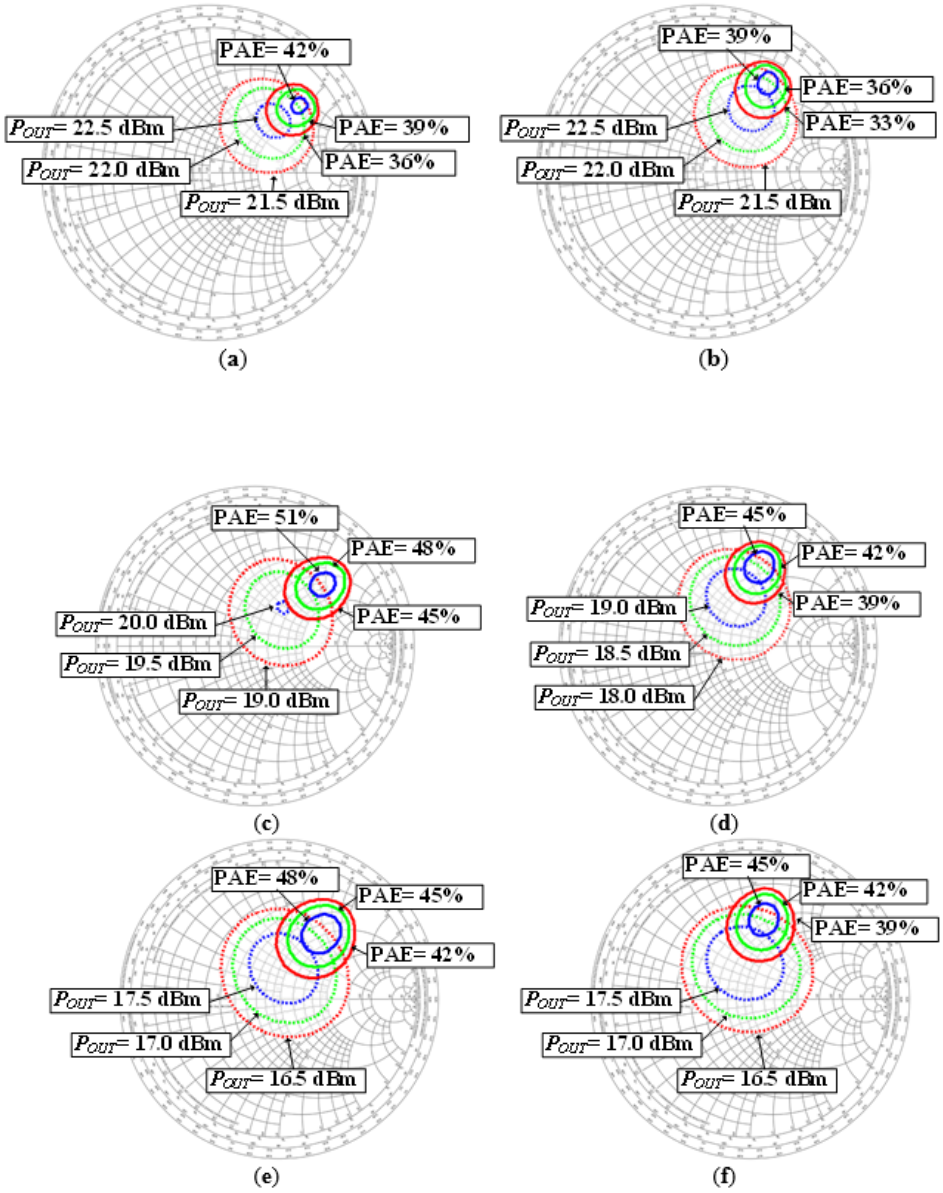


Figure 4.81: Load-pull Simulations of the 4 *x* 37.5 µm GaN Device at (a) 24 GHz and (b) 37 GHz for V_{DD} = 12 V; (c) 24 GHz; and (d) 37 GHz for V_{DD} = 6 V; (e) 24 GHz and (f) 37 GHz for V_{DD} = 4 V all at Around P_{1dB}.

Using load-pull simulations on several GaN devices of different sizes with measurement-based models done in Cadence AWR (Applied Wave Research) design environment, a 4 *x* 37.5 µm device is chosen for good trade-off of high PAE and gain. The fundamental load-pull simulations for max. PAE circles for the 4 *x* 37.5 µm device are shown in Figure 4.81 for V_{DD} = 4/6/12 V at 24 GHz and 37 GHz. Not only is the PAE lower for V_{DD} = 12 V compared to V_{DD} = 4/6 V, but the optimum load also has higher reactance (at 24 GHz max. PAE load for 12V is 1.39+2.35*j, while for 4V is 0.96 + 1.35*j), and thus it may be more difficult to achieve

broadband results with 12 V operation. First, a single-ended PA is designed with input and output matching networks, RF choke and 1 pF bypass capacitors all on-chip. Using the load-pull simulations, the output matching is designed using only 3 matching components (including the RF choke) to minimize loss for high PAE. To achieve good broadband S_{11} and increase the usable gain bandwidth, a 3rd-order input matching network is utilized (see Figure 4.83). The PA is biased at a class A/B mode for good trade-off of linearity and PAE. After this single-ended PA was designed and tested, a differential version was also designed where neutralization capacitors are added to increase the gain, as will be discussed later.

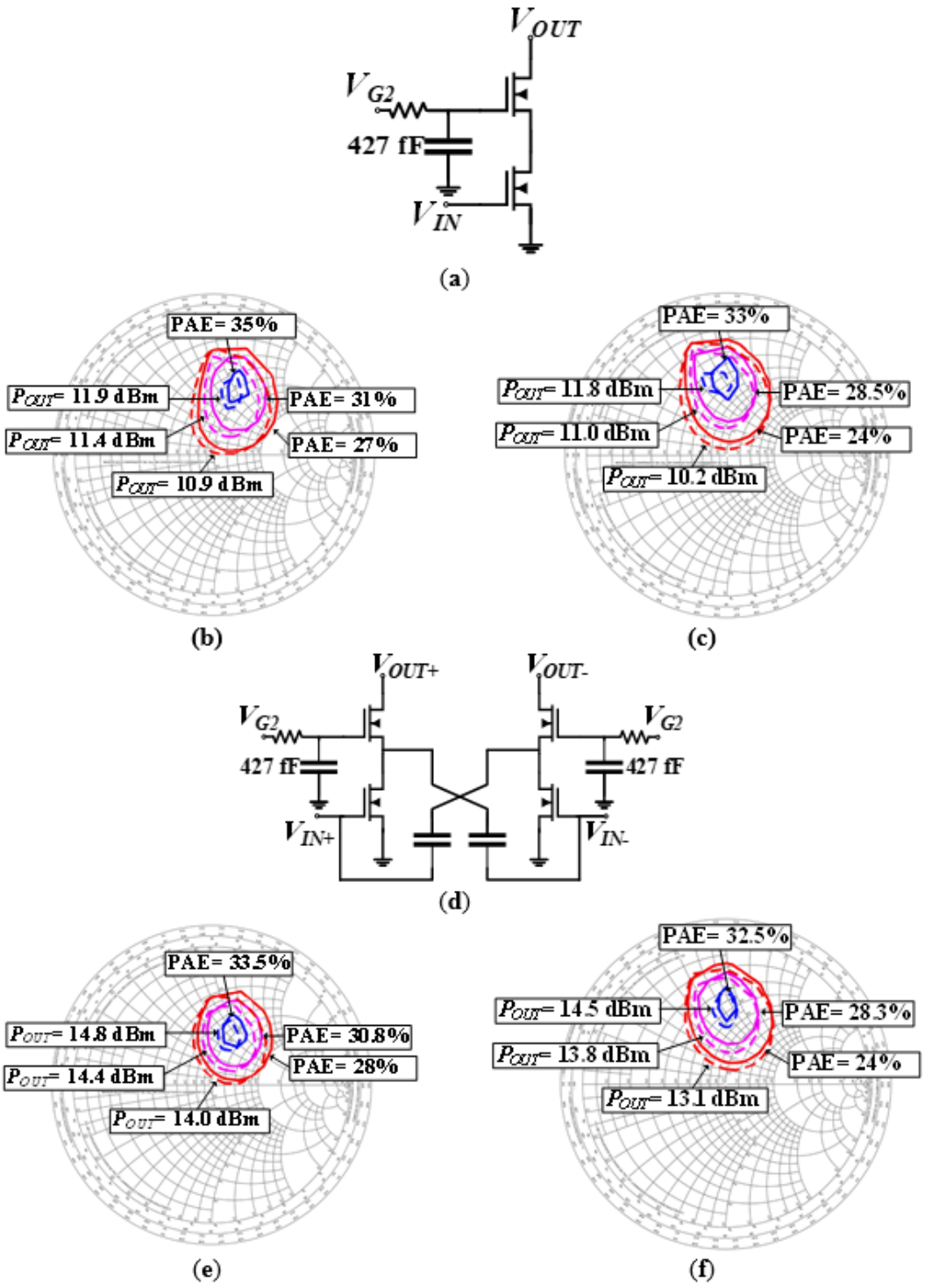


Figure 4.82: Load-pull Simulations

Single-ended cascode device pair (with a 427 fF capacitor on the cascode gate) (a) at (b) 24 GHz and (c) 37 GHz; and of the (d) differential cascode device pair with neutralization capacitors at (e) 24 GHz and (f) 37 GHz all at around P_{1dB}.

In the CMOS FD-SOI technology, PAE and P_{OUT} load-pull simulations are performed in Cadence Spectre. First, these simulations are done on a single-ended cascode device pair with parasitics again extracted up to the top metal layer as shown in the schematic in Figure 4.82(a). These simulations are done at around P_{1dB} and indicate that at 24/37 GHz, where the cascode device can achieve max. PAE of 35.0%/33.0% and $P_{OUT,MAX}$ of 11.9/11.8 dBm, respectively. Load-pull simulations are then also done on a differential cascode device pair with small neutralization capacitors (see Figure 4.82(d)), and they achieve max. PAE and $P_{OUT,MAX}$ values of 33.5%/32.5% and 14.8/14.5 dBm at 24/37 GHz, respectively (still at around P_{1dB}). The optimal load impedance of max. PAE and $P_{OUT,MAX}$ can occur close to each other on the Smith Chart as indicated by the load-pull simulations, and thus these devices can almost be simultaneously optimized for both PAE and output power. Additionally, load-pull simulations suggest that these devices could achieve broadband performance as the optimal load does not move far from 24 to 37 GHz.

As discussed previously, this differential PA design utilizes neutralization capacitors for gain and reserve isolation improvement. An RC feedback path is also added to improve the BW of this design. On-chip baluns and transformers are offered in this mature 22FDX PDK, and this design utilizes one of these center-tapped on-chip baluns to convert the differential output to a single ended RF_{OUT}, and for output matching and for feeding the V_{DD}. Due to this small technology node, ESD double diodes are added to all the gate pads to protect the PA from ESD events. The cascode device pair presented here is not quite designed in a classical cascode topology, as a gate capacitor of ~450 fF is used at the top cascode device in this work instead using a larger capacitor to make a CG (common-gate) device's gate a classical RF ground. This choice of "hybrid" design between a stacked vs. a cascode topology can still effectively mitigate the breakdown concerns by sharing the total voltage swing of the output of the PA across the bottom CS (common-source) and the top cascode device [75].

4.5.2 Results

For all of the measurements shown in this chapter, the RF input is probed and the DC voltages are provided by gold wire-bonded pads to a custom PCB (printed circuit board), where more bypass capacitors are added for better stability on all DC traces. Both CW and modulated 5G NR input signal will be used as the RF input signal and the PAs are measured with the state-of-the-art mm-Wave PXIE (PCI express extensions for instrumentation) system by National Instruments (NI), which can produce modulated 5G NR signals of up to 1 GHz BW and up to 44 GHz [51]. In the following discussions, besides the 3-dB BW conventionally used, BW of these PAs is often also compared by the absolute BW, defined as $2\cdot(\frac{f_H-f_L}{f_H+f_L})$ [76], where f_H is the upper frequency and f_L is the lower frequency of the 3-dB BW.

4.5.2.1 Single-Ended GaN (GaN #1) PA Measurement Results

Figure 4.83 shows the schematic of the single-ended broadband GaN PA as well as the S-parameter measurement vs. post-layout EM simulation. The EM simulations for the HRL GaN PDK are done using Cadence's AXIEM in AWR to include all layout parasitics. This PA

achieves max. S_{21} of 12.5 dB and a small-signal 3-dB BW of 18 – 38.7 GHz (absolute BW = 73.0%) at V_{DD} = 6 V, and S_{21} =10.3 dB with BW = 18 – 40.3 GHz (or an absolute BW = 76.5%) at V_{DD} = 4 V. Although not plotted here, S-parameter measurements with V_{DD} = 12 V shown in [77] achieved max. S_{21} =13.0 dB with BW = 18.3 – 32.7 GHz (absolute BW= 56.5%). Thus, as the load-pull EM simulations had suggested, lowering the drain voltage makes this design more broadband. The S_{21} modeling at V_{DD} = 4 V is not as accurate vs. at V_{DD} = 6 V, which is likely due to the 4 V model being constructed from extrapolation whereas the 6 V models are directly from measurements. However, this work sees that the S_{11} and S_{22} do match well with simulations for both supply voltages of 4 V and 6 V.

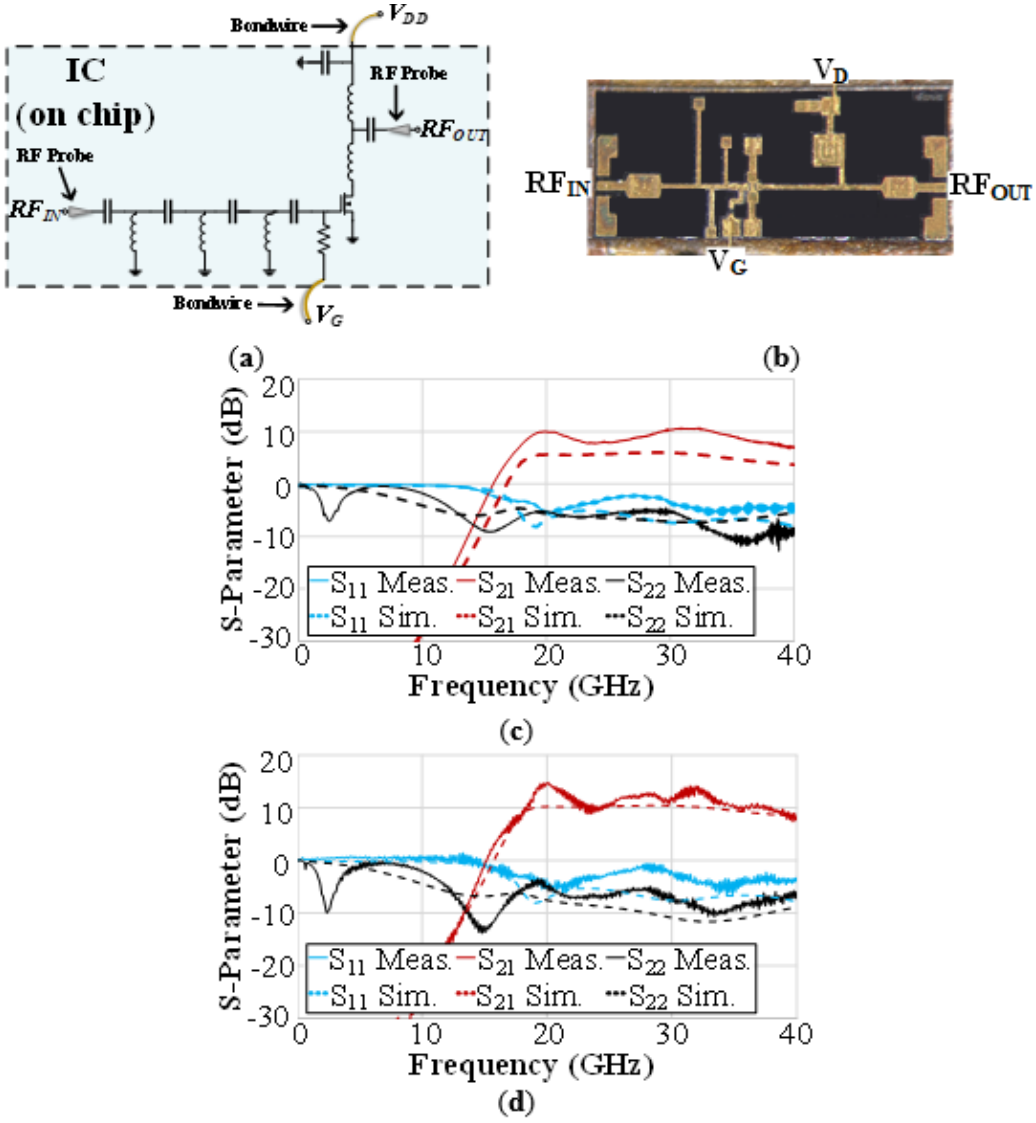


Figure 4.83: Simplified Schematics (a) and the (b) Micrograph of the Broadband Single-ended GaN PA (2.1 *x* 0.88 mm^2 with Pads) and its S-parameter EM PEX Simulations vs. Measurement with (c) V_{DD} = 4 V; and (d) V_{DD} = 6 V.

The large signal measurement results vs. post-layout EM simulations are shown in Figure 4.84 for V_{DD} = 4 and 6 V at 24, 28, and 44 GHz. This PA achieves max. PAE/P_{SAT} of 34.0%/ 18.6 dBm at 24 GHz, 42.1%/ 18.6 dBm at 28 GHz, and 21.6%/ 17.8 dBm at 44 GHz. With a 6 V supply, there is once again good agreement of measurement to simulation data and the PA achieves max. PAE/$P_{OUT,\ SAT}$ of 28.9%/ 20.1 dBm at 24 GHz, 34.6%/ 20.3 dBm at 28 GHz, and 19.1%/ 19.3 dBm at 44 GHz. Figure 4.85 shows the measured $P_{OUT,SAT}$ and max. PAE plotted across frequency, which highlights the broadband performance of this PA as it is able to maintain greater than ~20% PAE across the entire band of 18 – 40 GHz for V_{DD} = 4 V and greater than 14% PAE with V_{DD} = 6 V. The peak PAE for V_{DD} = 4 V is much higher at above 42% at 28 GHz.

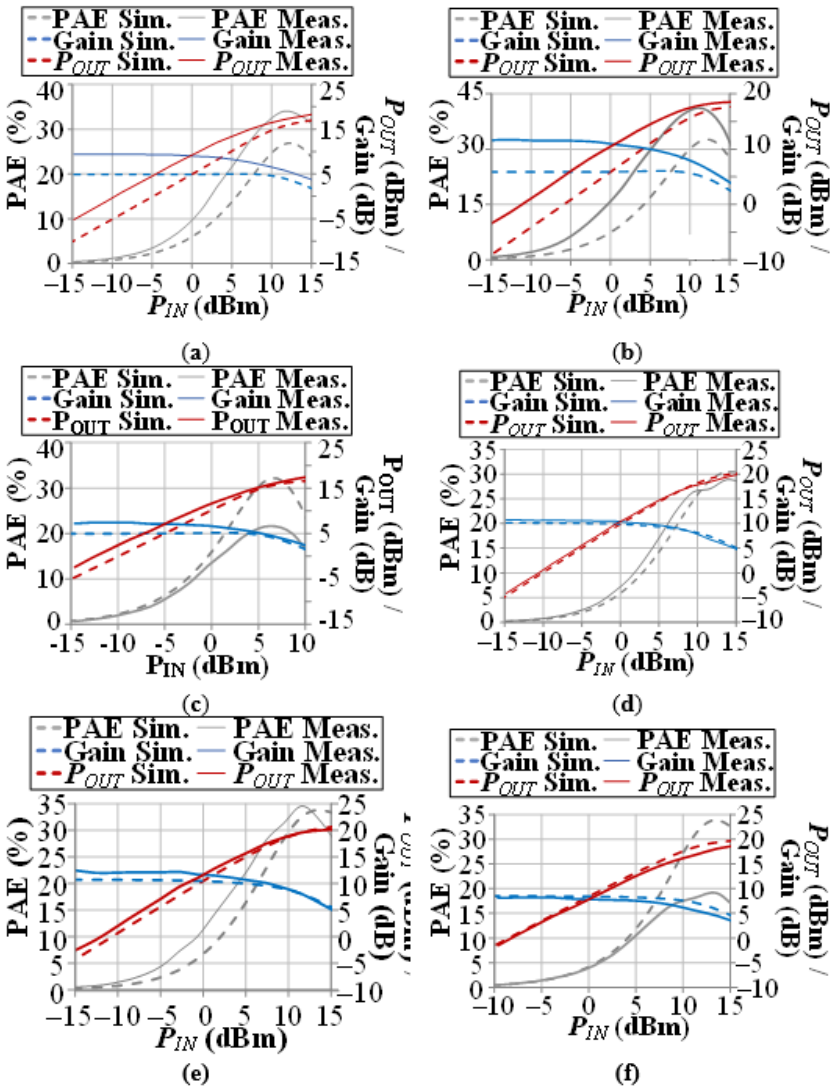


Figure 4.84: Large-signal EM PEX Simulation vs. CW Measurement of the Broadband Single-ended GaN PA with V_{DD} = 4 V at (a) 24, (b) 28, and (c) 44 GHz and V_{DD} = 6 V at (d) 24, (e) 28, and (f) 44 GHz

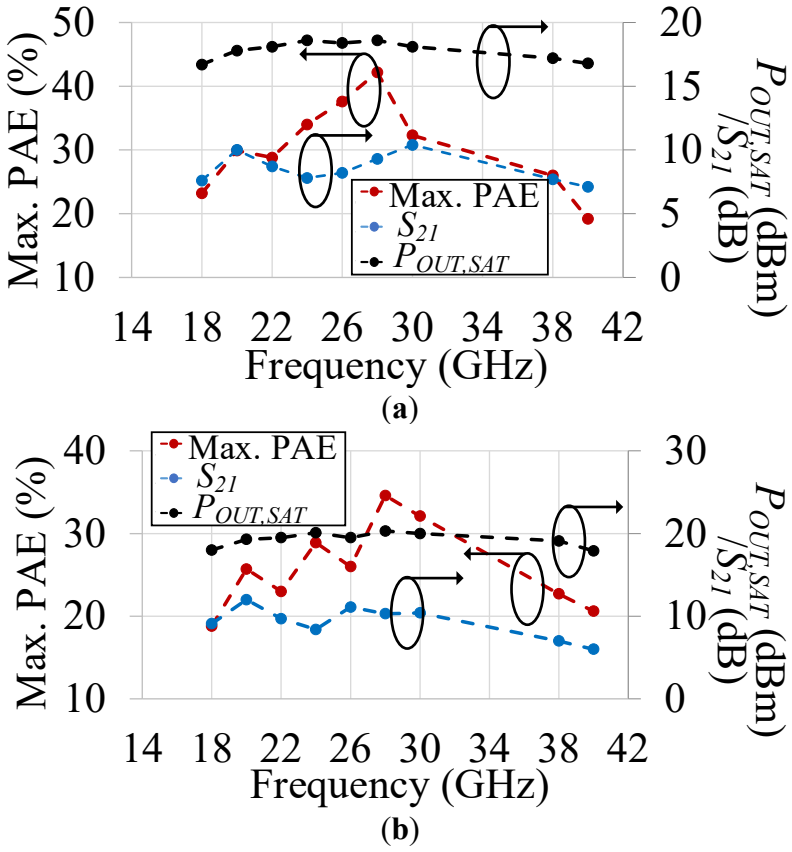


Figure 4.85: Measured Max. PAE, S_{21} and $P_{OUT,SAT}$ vs. Frequency of the Broadband single-ended GaN PA at (a) V_{DD} = 4 V and (b) V_{DD} = 6 V

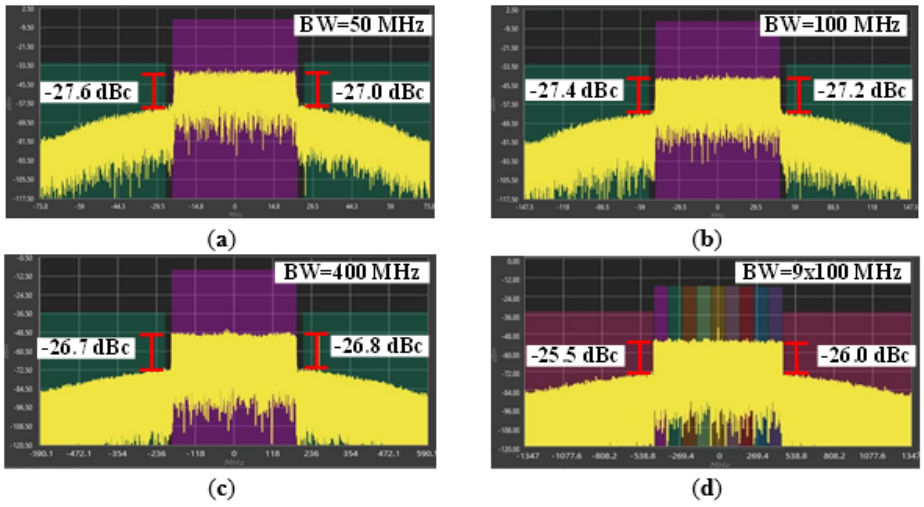


Figure 4.86: ACLR Measurements of the Broadband Single-ended GaN PA at 24 GHz using a (a) 50 MHz (b) 100 MHz (c) 400 MHz and (d) 9x100 MHz 256-QAM 5G NR Signal with PAPR = 8 dB.

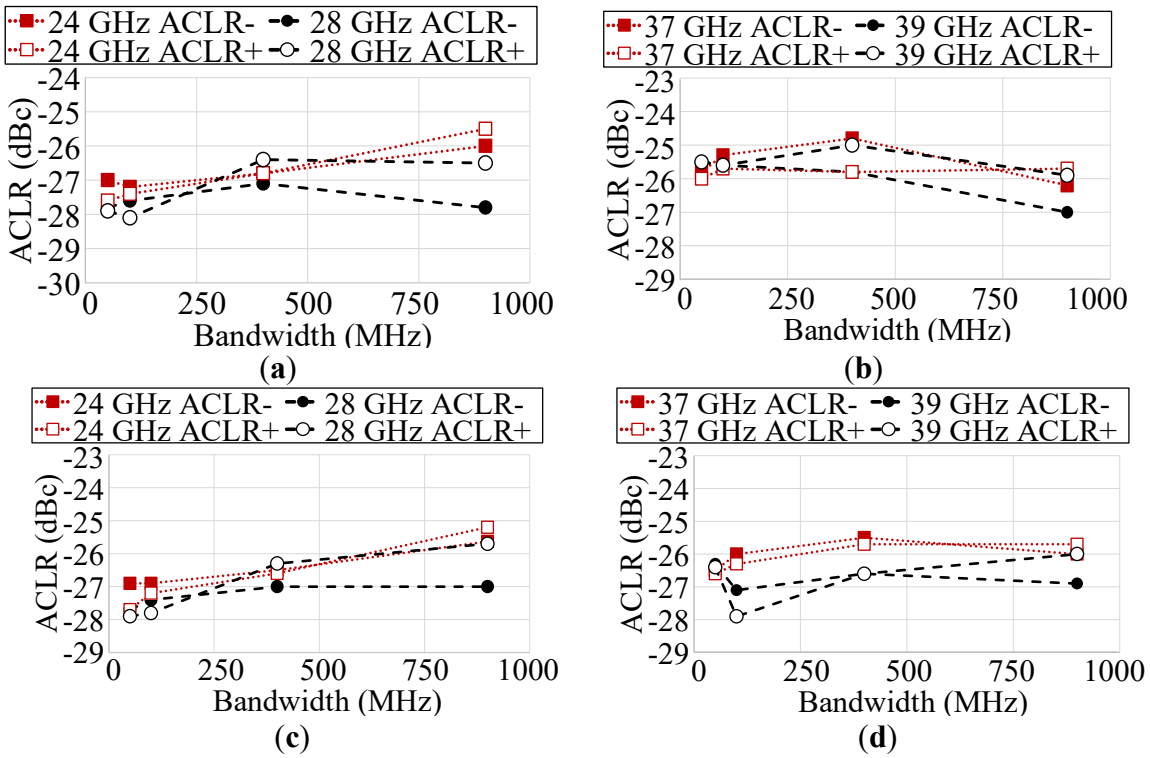


Figure 4.87: Measured ACLR+/ACLR- vs. 5G NR Instantaneous Signal BW (PAPR = 8 dB) for the Broadband Single-ended GaN PA with V_{DD} = 4 V at (a) 24 GHz and 28 GHz, and at (b) 37 GHz and 39 GHz; and with V_{DD} = 6 V at (c) 24 GHz and 28 GHz, and at (d) 37 GHz and 39 GHz.

PA Linearity is then tested with a 50, 100, 400 and 9x100 MHz 256-QAM modulated 5G NR inputs at PAPR (peak-to-average-power ratio) = 8 dB at 24 GHz and VDD = 4 V (Figure 4.86). With POUT,AVE = ~ 11 dBm, this PA achieves ACLR -/+ (adjacent channel leakage ratio) of -27.6/-27.0 dBc with BW = 50 MHz (PAEAVE = 13.3%), and -27.4/-27.2 dBc with BW = 100 MHz (PAEAVE =12.1%), -26.7/-26.8 dBc with BW = 400 MHz (PAEAVE = 11.8%), and -25.5/-26.0 dBc with BW = 9x100 MHz (PAEAVE = 12.0%). The signal BW is varied from 50 – 900 MHz at 24, 28, 37, and 39 GHz, and the measured ACLR vs. BW is plotted in Figure 4.87 all at POUT,AVE ~11 dBm when VDD = 4 V, and POUT,AVE = ~12 dBm with VDD = 6 V. Figure 4.87 shows that there is not a significant degradation in the PA linearity increasing the 5G NR signal BW from 50 MHz to 9x100 MHz at 28, 37, and 39 GHz, and only a slight degradation (~ 2 dB) in the measured ACLR at 24 GHz for both VDD = 4 V and 6 V. Additionally, there is minimal degradation on the linear output power going from 24/28 GHz to 37/39 GHz.

4.5.2.2 Differential GaN (GaN #2) PA PEX EM Simulation Results

The single-ended broadband GaN PA discussed above was then used to form a differential broadband mm-Wave 5G PA as shown in Figure 4.88, where the CS topology is used, and

neutralization capacitors are added for improved MSG and for comparison purposes against a reasonably similar differential FD-SOI CMOS PA that will be presented later in this chapter. Additional RC traps were added at the gates of these GaN transistors to further stabilize the PA, and this differential design has an area of 1.94 mm^2 (with pads), slightly larger than the 1.85 mm^2 area of the single ended design. PEX EM simulations indicate that this differential GaN PA achieves a max. S_{21} of 13.4 dB, with a 3-dB BW from 20.1 – 44.3 GHz (or an absolute BW of 75.2%) at V_{DD} = 6 V, which BW is comparable to the single-ended GaN #1 design, but with a significantly higher gain and P_{OUT}.

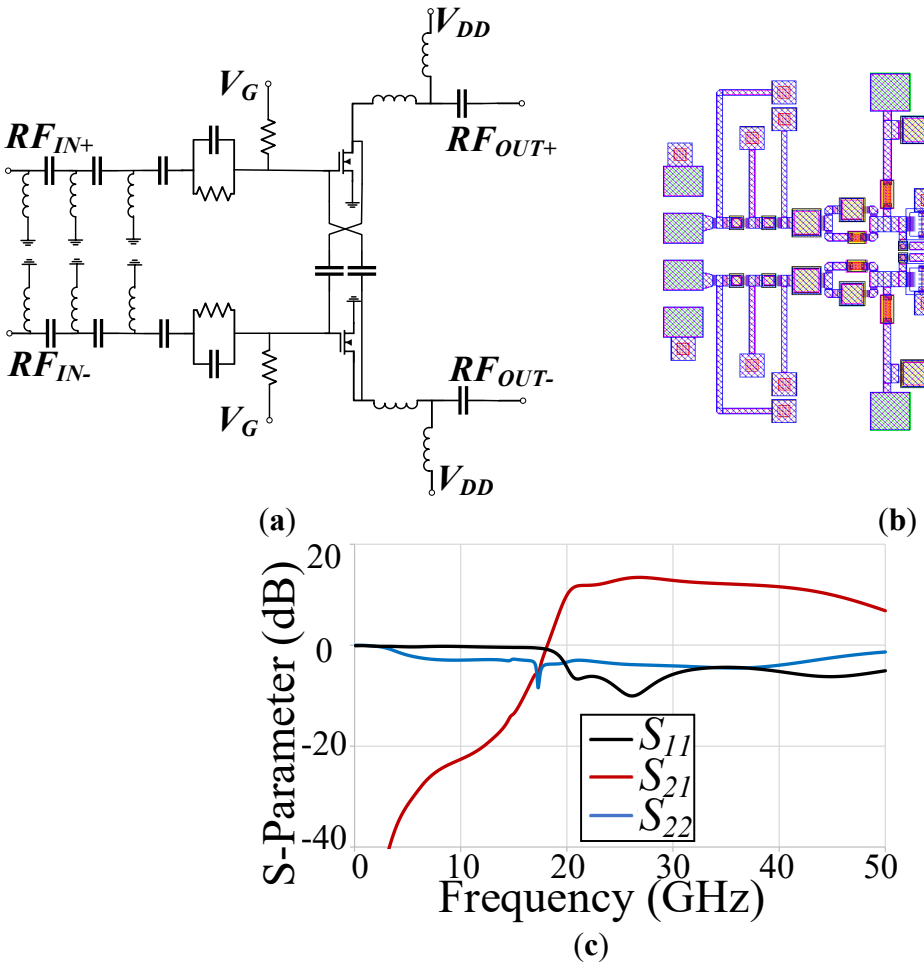


Figure 4.88: Simplified Schematics (a) and (b) the Layout of the Broadband Differential GaN PA (2.0 *x* 0.97 mm^2 with Pads); and (c) its S-parameter EM PEX Simulation Results

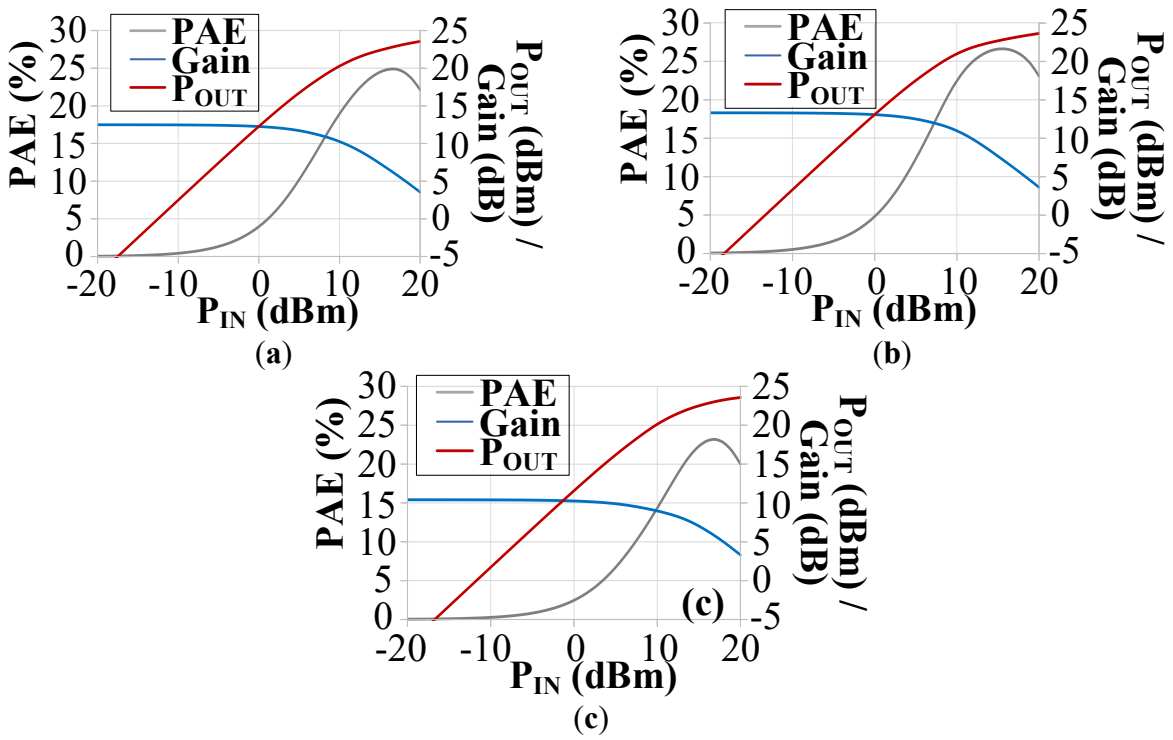


Figure 4.89: Large-signal EM PEX Simulations of the Broadband Differential GaN PA for CW Inputs at (a) 24, (b) 28, and (c) 44 GHz

The large signal EM simulations results for this differential GaN PA are shown in Figure 4.89, which indicates that this PA can achieve max. PAE of 24.9%/ 26.6%/ 23.3% and $P_{OUT,SAT}$ of 23.5/ 23.6/ 23.3 dBm at 24/ 28/ 44 GHz. Figure 4.90 shows the broadband nature of this PA, as it is able to achieve > 20% max. PAE across the 20 – 44 GHz band, very high simulated 1-dB $P_{OUT,SAT}$ BW while also achieving $P_{OUT,SAT}$ larger than ~23 dBm in the 5G FR2 band of interest. Compared to the measured GaN #1 PA, it achieves similar max. PAE, while having ~3 dB greater $P_{OUT,SAT}$ than the single-ended design. This work will discuss another broadband differential mm-Wave 5G PA designed in 22 nm FD-SOI CMOS next.

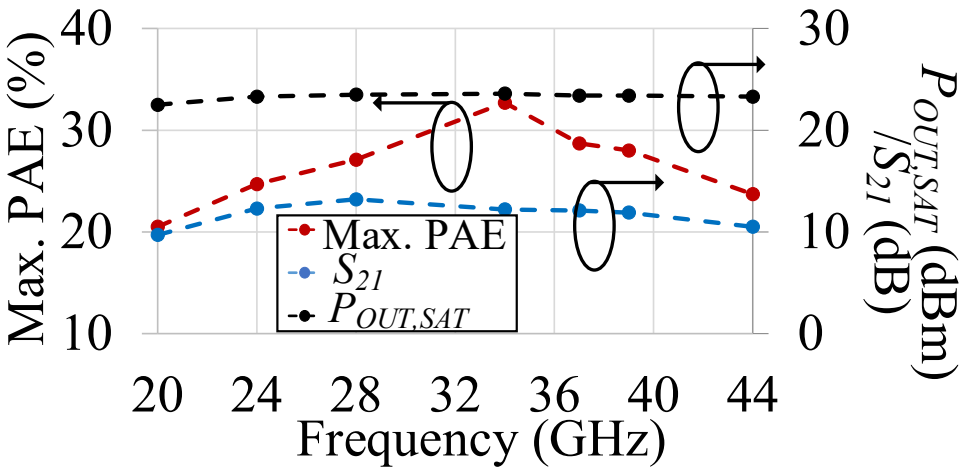


Figure 4.90: EM PEX Simulated max. PAE, S21 and POUT,SAT vs. Frequency of the Broadband Differential GaN PA

4.5.2.3 Differential Cascode CMOS SOI PA Measurement Results

Figure 4.91 presents the schematic of the differential cascode CMOS PA designed in the 22FDX technology, as well as the small-signal S-parameter measurement data compared to post-layout PEX simulations of this PA. Layout parasitics for this design was extracted using Mentor Graphic's Calibre R+C+CC extraction. Small-signal measurement data agrees well with the PEX simulations, exhibiting excellent broadband performance. PEX simulations achieve max. S_{21} small-signal gain of 17.4 dB with 3-dB BW of 20.5 – 47.4 GHz (or an absolute BW of 79.2%), while measurement achieves a 3-dB BW of 19.1 – 46.5 GHz, and a max. S_{21} = 16.4 dB (absolute BW of 83.5%). The RC feedback network allows for adequate input matching with S_{11} < -5.5 dB across the entire ~27 GHz band in both simulation and measurement. Thus, measurement data sees virtually no degradation on the targeted small-signal broadband BW to cover the entire key 5G FR2 band of 24.25 – 43.5 GHz, as indicated by the PEX simulations; only minimal degradation on measured vs. the simulated small-signal gain.

The effect of the RC feedback on this differential CMOS SOI PA design is also simulated in post-layout PEX simulations in Figure 4.91 (d), where the original design is compared to the same design with the only change being that the RC feedback is removed (and the PA layout re-extracted and re-simulated). This shows that the overall gain is reduced by ~2 dB when RC feedback is added, as this PA without the RC feedback achieves max. S_{21} = 19.6 dB. However, the BW is increased when RC feedback is added, as without it the 3-dB BW degrades to 20.9 – 39.6 GHz (or an absolute BW of 61.8%). Thus, the absolute BW degrades by ~15% without the RC feedback, and the input/output matching worsened considerably as well.

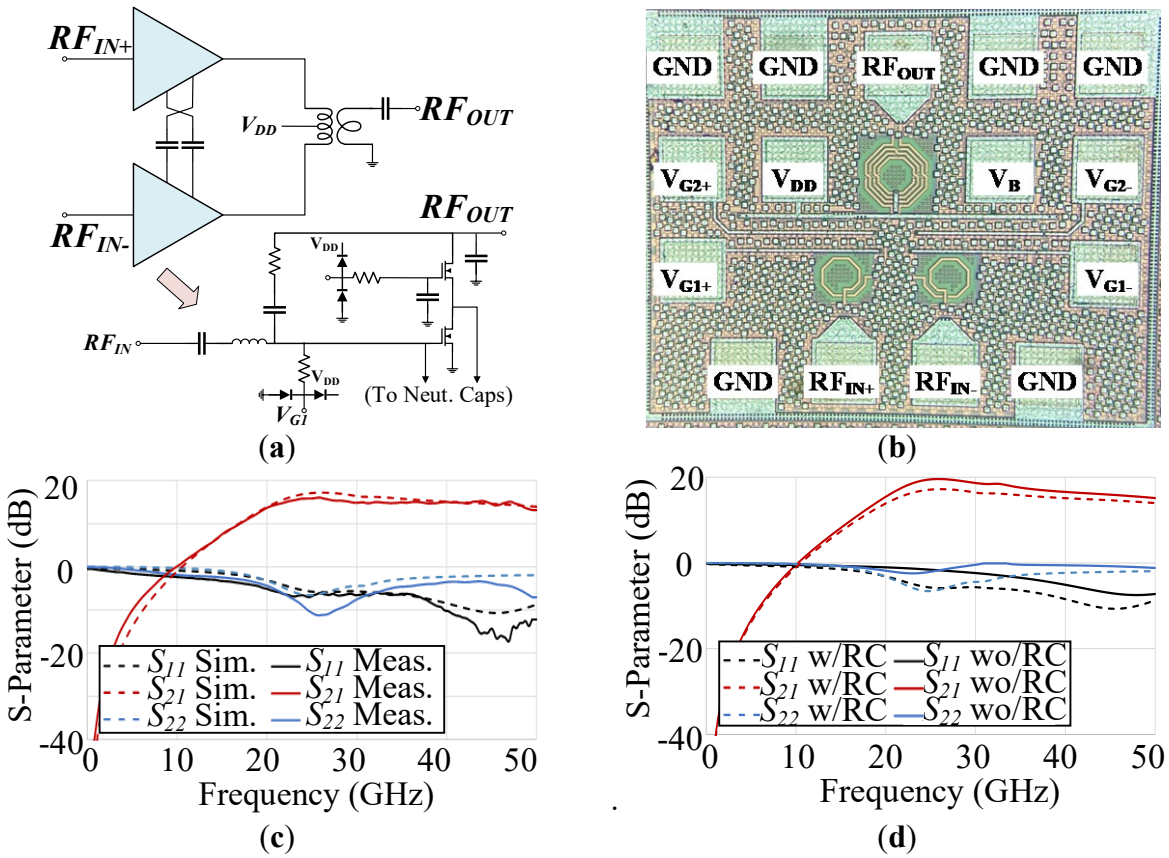


Figure 4.91: Simplified Schematics (a) and (b) Micrograph of the Broadband 22 nm CMOS FD-SOI PA (620 µm *x* 500 µm with pads); (c) its S-parameter Post-layout PEX Simulations vs. Measurement; and (d) a Comparison of its PEX S-parameters Simulations with and without the RC Feedback

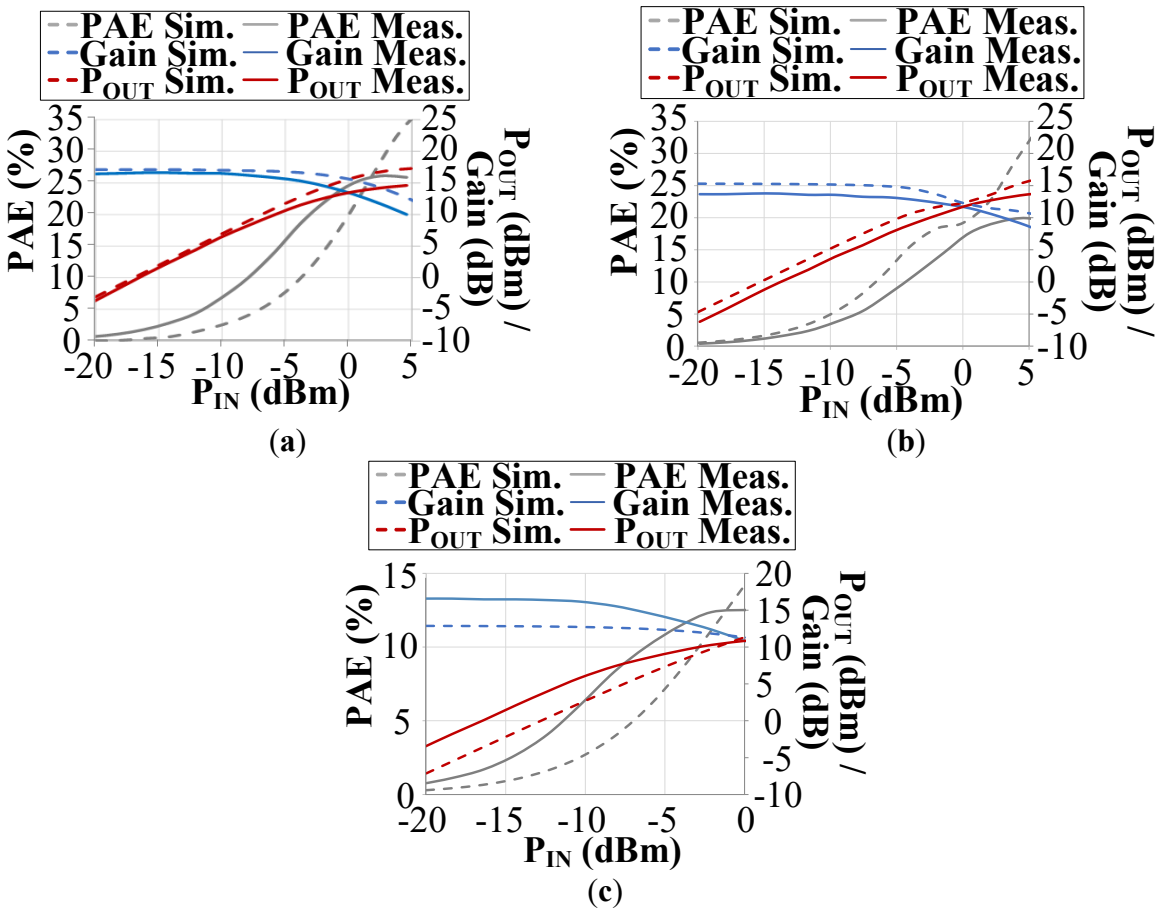


Figure 4.92: Large-signal Post-layout PEX Simulation vs. CW measurement of the Broadband CMOS FD-SOI PA at (a) 24, (b) 28, and (c) 44 GHz

The large-signal measured data vs. PEX simulation results at 24/ 28/ 44 GHz are shown in Figure 4.92, where a degradation in the large-signal measurement data from simulations is seen, likely due to inaccuracies in the large-signal transistor modeling. These figures show that at 44 GHz the measured gain is 3 dB higher than those of the PEX EM simulations. The measured gain values are usually reduced by 1-2 dBs from the simulated data at 24 – 39 GHz, while this broadband PA achieves at 24/ 28/ 44 GHz measured OP_{1dB} of 11.5/ 9.2/ 7.4 dBm with PAE $@OP_{1dB}$ of 18.6%/ 11.2%/ 9.3%, $P_{OUT,\,SAT}$ of 14.6/ 14.0/ 10.9 dBm, and max. PAE of 26.1%/ 19.9%/ 12.5 %, respectively.

Figure 4.93 plots the measured max. PAE, S_{21} and $P_{OUT,SAT}$ vs. frequency from 20 – 44 GHz, which shows this PA maintains a max. PAE ≥ 12.5% and $P_{OUT,SAT}$ ≥ 11 dBm across this frequency range. It achieves a max. PAE ≥ 15.1% and $P_{OUT,SAT}$ ≥ 12.9 dBm across 24 – 39 GHz, highlighting the broadband performance of this CMOS PA.

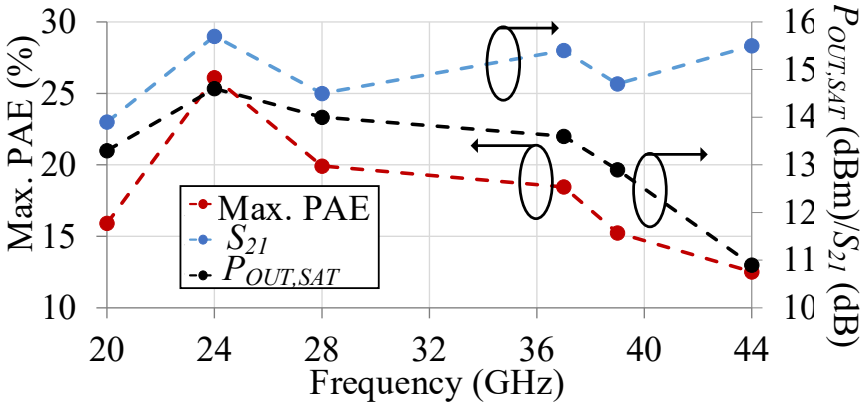


Figure 4.93: Measured Max. PAE, S_{21}, and $P_{OUT,SAT}$ vs. Frequency of the Broadband CMOS FD-SOI PA

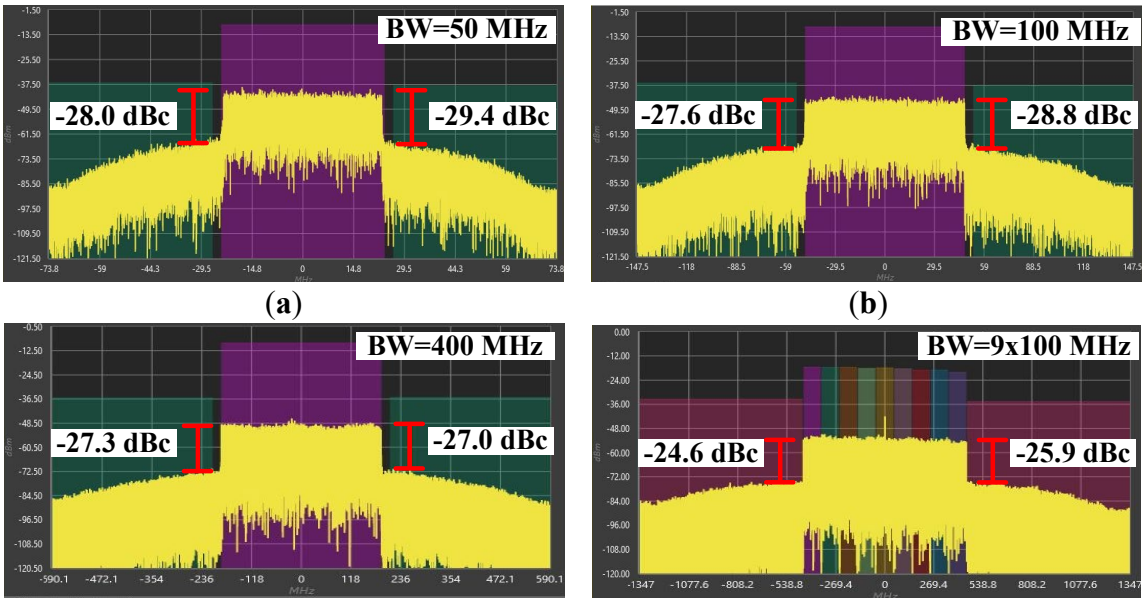


Figure 4.94: ACLR Measurements of the Broadband CMOS FD-SOI PA at 24 GHz using a 256-QAM Modulated 5G NR Signal with PAPR = 8dB at a signal BW of (a) 50 MHz, (b) 100 MHz, (c) 400 MHz, and (d) 9x100 MHz.

As what had been done with GaN #1 design, this CMOS PA's linearity is tested with 50/ 100/ 400/ 9x100 MHz 256-QAM NR input signals with the same PAPR = 8 dB and same NI PXI equipment at 24 GHz, and the PA output spectra are shown in Figure 4.94. With the same output power of $P_{OUT,AVE}$ = ~7 dBm, this PA achieves at the instantaneous signal BW = 50 MHz an ACLR -/+ of -28.0/-29.4 dBc (PAE_{AVE} = 7.3%); with BW = 100 MHz, -27.6/-28.8 dBc (PAE_{AVE} = 7.0%); with BW = 400 MHz, -27.3/-27.0 dBc (PAE_{AVE} = 7.7%), and with BW = 9x100 MHz, -24.6/-25.9 dBc (PAE_{AVE} = 8.1%).

Similarly, this PA's linearity is also tested at 50 – 900 MHz BW at several other frequencies in the 5G FR2 band. When varying the BW of a 256-QAM 5G NR signal (PAPR = 8 dB) at 24 GHz and 28 GHz, the $P_{OUT,AVE}$ is about 7 dBm, and at 37 GHz and 39 GHz, $P_{OUT,AVE}$ is approximately ~6 dBm. Figure 4.95 also shows interesting ACLR measurement data vs. signal BW. When the BW is increased from 50 MHz to 100 MHz, the linearity is not affected much, but when increasing from 100 MHz to 400 MHz, the PA's linearity degrades by a small but noticeable amount of ~1 – 3 dB. Then increasing the BW from 400 MHz to 9x100 MHz, the linearity becomes further degraded by an additional ~2 dB and at all frequencies measured. This CMOS PA's linear output power, though, only degrades by ~1 dB when its operating frequencies change from 24/28 GHz to 37/ 39 GHz.

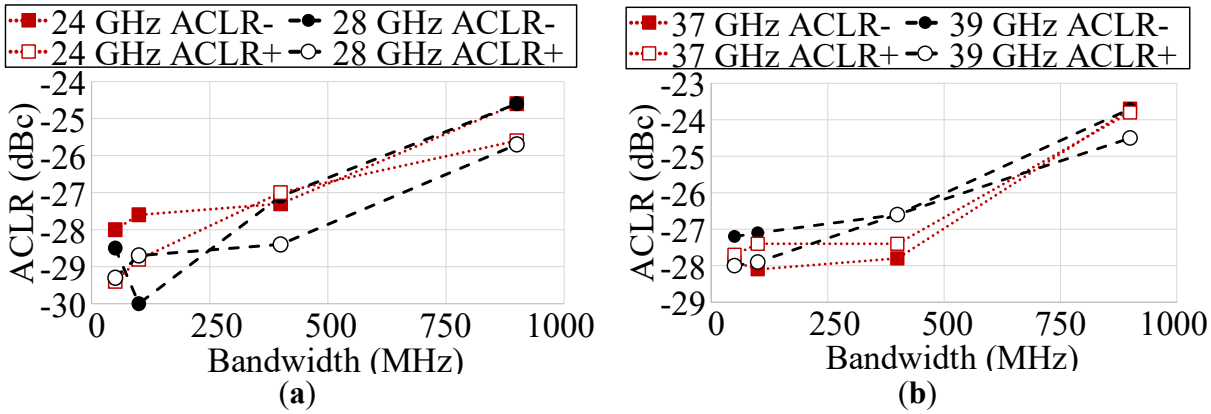


Figure 4.95: Measured ACLR+/ACLR- vs. Carrier BW of the broadband CMOS FD-SOI PA at (a) 24 GHz and 28 GHz and (b) 37 GHz and 39 GHz.

4.5.3 Discussion

In the previous sections, three different PAs from two different technologies were presented. Typically, GaN is used for higher power applications, but the designs in this work are all targeted to perform in the sub-Watt range. Small-signal measurements matched well with PEX simulations for both GaN #1 and for the CMOS PA. However, large signal measurement results did not match well for the CMOS PA, whereas large signal measurements for the GaN #1 for V_{DD} = 6 V matches quite well to simulation results. Although measurements have not been taken on GaN #2 as this design is in the process of being fabricated, measurements on GaN #1 had good agreement with EM simulations for V_{DD} = 6 V and thus will be compared to the other PAs here with V_{DD} = 6 V. Although the 22 nm FD-SOI CMOS PA used several power performance improvement techniques (i.e., cascode and differential operation), the comparison of the three PAs in Figure 4.96 and Table 4.21 show that the $P_{OUT,SAT}$ is significantly higher for the broadband single-ended or differential GaN PAs vs. the CMOS PA. This could be explained due to the superior breakdown performance of GaN over the CMOS technologies, enabling larger output voltage swings per device. GaN #2 and the 22FDX PA both used differential topology and have similar gain, but the PAE as well as P_{OUT} appears superior for the GaN #2 PA vs. those of the CMOS-SOI PA. However, the broadband differential CMOS FD-SOI PA is much smaller

than the GaN PAs in die size, with slightly higher power gain (but much lower $P_{OUT,SAT}$ vs. GaN PAs), and it also includes an output balun, highlighting the excellent integrability of this CMOS technology. Using aggressive 256 QAM modulated 5G NR input waveforms, great design insights can be gained from the measured ACLR vs. frequency on signal BW vs. linearity and $P_{OUT,Linear}$ for these two device technologies. When the signal BW is increased from 50 MHz to 900 MHz, the ACLR degrades by ~ 2 dBc for GaN #1 for both V_{DD} = 4 V and 6 V at 24 GHz and virtually does not degrade at 28, 37, and 39 GHz. However, for the CMOS PA, the ACLR degrades with this broadened signal BW by ~4 dBc at all the carrier frequencies tested. Thus, this 40 nm GaN/SiC technology appears to have better linearity against very wide GHz 256QAM modulated 5G NR signal across the FR2 band, and offers significantly higher $P_{OUT,Linear}$ and $P_{OUT,SAT}$ than the 22FDX CMOS technology. However, as this work do not have measured $P_{OUT,Linear}$ data for the differential GaN #2 yet, this work could not ascertain if the superior $P_{OUT,Linear}$ of broadband GaN PAs is mainly due to the device technology difference (i.e., GaN or FD-SOI), or by the cascode vs. common-source topology difference, or due to the single-ended vs. differential topology difference, or something else (such as the output balun and/or matching details). Therefore, more detailed studies with additional measurement data are required to illuminate and clarify this important point in the future.

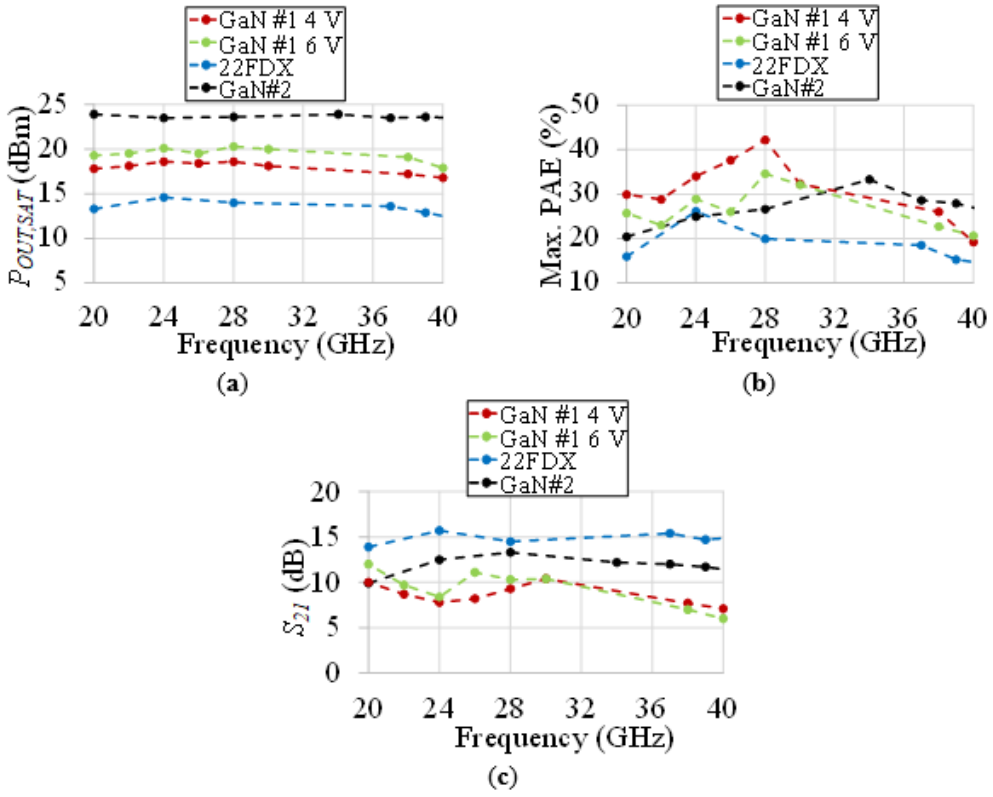


Figure 4.96 Measurements of the Broadband Single-ended GaN and the Broadband CMOS FD-SOI PAs and EM PEX Simulations of the Broadband Differential GaN for (a) $P_{OUT,SAT}$, (b) Max. PAE, and (c) S_{21} vs. Frequency

Table 4.21. Comparison of the Three Broadband mm-Wave PAs Presented in This Work

Tech.	Design	V_{DD} (V)	3-dB BW (GHz)	Freq. (GHz)	$P_{OUT,SAT}$ (dBm)	Peak PAE (%)	Gain (dB)	Signal Type	ACLR (dBc)@ P_{OUT}(dBm)
22nm CMOS FDSOI	Cascode with RC feedback; Diff.	1.8	19.1 – 46.5 (79.2%)	24	14.6	26.1	15.7	400 MHz 256-QAM 5G NR	-27@7.1 PAE=7.7%
								9x100 MHz 256-QAM 5G NR	-24.6@7.3 PAE=8.1%
				28	14.0	19.9	14.5	400 MHz 256-QAM 5G NR	-27.1@7.1 PAE=5.3%
								9x100 MHz 256-QAM 5G NR	-23.7@6.6 PAE= 6.2%
				39	12.9	15.2	14.7	400 MHz 256-QAM 5G NR	-26.6@6.4 PAE =5.8%
								9x100 MHz 256-QAM 5G NR	-24.2@5.6 PAE =5.0%
				44	10.9	12.5	15.5	N/A	N/A
40 nm GaN	3rd-Order Input Matching; Single-ended	4	18 – 40.3 (76.5%)	24	18.6	34	7.8	400 MHz 256-QAM 5G NR	-25.4@11.9 PAE=15.4%
								9x100 MHz 256-QAM 5G NR	-27.7@9.7 PAE=8.1%
				28	18.6	42.1	9.2	400 MHz 256-QAM 5G NR	-27.2@11.2 PAE=13.1%
								9x100 MHz 256-QAM 5G NR	-27@11.3 PAE=13.9%
				39	17.2	26.0	8.7	400 MHz 256-QAM 5G NR	-27@11.1 PAE=11.1%
								9x100 MHz 256-QAM 5G NR	-25.6@11.3 PAE=11.9%
				44	17.8	21.6	7.2	N/A	N/A
		6	18 – 38.7 (73.0%)	24	20.1	28.9	9.6	400 MHz 256-QAM 5G NR	-26.5@11.9 PAE=10.2%
								9x100 MHz 256-QAM 5G NR	-27@11.9 PAE=10.2%
				28	20.3	34.6	11.9	400 MHz 256-QAM 5G NR	-26.3@14.0 PAE=13.0%
								9x100 MHz 256-QAM 5G NR	-26.8@14.2 PAE=14.0%
				39	18.1	22.8	9.3	400 MHz 256-QAM 5G NR	-28.7@11.4 PAE=9.2%
								9x100 MHz 256-QAM 5G NR	-28@11.8 PAE =9.7%
				44	19.3	19.1	8.1	N/A	N/A
40 nm GaN*	3rd-Order Input Matching; Diff.	6	20.1 – 44.3 (75.2%)	24	23.5	24.9	12.5	N/A	N/A
				28	23.6	26.6	13.3	N/A	N/A
				39	23.6	27.9	11.7	N/A	N/A
				44	23.3	23.3	10.4	N/A	N/A

*EM PEX Simulated

Our GaN PAs are compared to other state-of-the-art medium-power broadband mm-Wave 5G PAs in Table 4.22, as well as against some GaN PAs in literature with higher power, as most available mm-Wave GaN PAs in literature are targeted for higher power applications but without optimizing for high PA linearity. Although GaN #2 still needs measurement results for validation. Table 5.2 shows that both of our GaN PAs achieve some of the best small signal 3-dB BW as well as good PAE. Additionally, the GaN #1 design achieved excellent measured BW and good linearity with aggressive 5G NR signal modulation and instantaneous ~1 GHz signal BW, which have not been reported in prior medium-power mm-Wave GaN PAs [51]. Depending on the application, this GaN technology allows for the V_{DD} be varied from 12 V to 4 V to achieve optimal trade-off of PAE and output power. Although operating this PA at V_{DD} = 4 V reduces P_{OUT} with an increase in cost, being able to vary the supply voltage like this is not as easily feasible for silicon-based stacked broadband mm-Wave PAs. Thus, this work conclude our GaN #1 PA exhibits excellent 3-dB BW, peak and linear PAE and $P_{OUT,Linear}$ with stringent 256-QAM modulation and rather large instantaneous signal BW of 9x100 MHz across the key 5G FR2 band; it is among the best broadband linear mm-Wave medium-power PAs in literature. Our 22 nm broadband CMOS SOI PA vs. other state-of-the-art broadband medium power mm-Wave PAs is also shown in Table 4.22. Our CMOS PA achieves the best small-signal 3-dB BW in literature, and it has obtained good broadband linearity/PAE_{LINEAR}. It is also tested with the most stringent modulation (i.e., 256-QAM) and has a rather large instantaneous signal BW (i.e., 400 MHz and 9x100 MHz).

Table 4.22. Literature Comparison of the Three Broadband mm-Wave Presented in This Work to Other Broadband State-of-the-Art Mm-Wave PAs

Ref.	Tech.	Design	Supply Volt. (V)	3-dB BW (GHz)	Freq. (GHz)	$P_{OUT,sat}$ (dBm)	Peak PAE (%)	Gain (dB)	Signal Type	ACLR (dBc)@ P_{OUT} (dBm)
[53]	65-nm CMOS	Multi-port load-pulling	1.1	26-42 (47.1%)	28	19	21	15	1 GHz 64-QAM OFDM	P_{OUT} = 7.5 PAE= 5.1%
					37	19.6	21.9	16	2 GHz 64-QAM OFDM	-25@9.8 PAE=10.2%
[57]	0.2 µm GaN on SiC	3-stage Harmonic Tuning	28	29-34 (55.1%)	33	39.5	36	25	-	-
[78]	0.1 µm GaN on SiC	One-order synthesized transformer network	12	18-40 (75.9%)	25	30	23.6	18**	-	-
[79]	0.15 µm GaAs	Transformer-Coupled	4	21.6-32.5 (40.3%)	28	26.5	31	12.6	64QAM 6Gb/s	-30@21.6 PAE=13.5%
									64QAM 9Gb/s	-30@19.9 PAE=9.5%
[55]	130-nm SiGe	2-stage Doherty	1.5	23.3-39.7 (52.1%)	28	16.8	20.3	18.2	64-QAM 500 MSym/s	-28.4@9.2 Coll. Eff.=18.5%
					37	17.1	22.6	17.1		-28.2@9.5 Coll. Eff.=19.2%
					39	17	21.4	16.6		-29.8@9.3 Coll. Eff. =17.2%
[80]	45nm SOI CMOS	Continuous Hybrid Class F/F^{-1}	2	23-40.5 (51.1%)	28	18.9	43.2	18.7	64-QAM 500 MSym/s	-28@10.3 PAE=13.1%
					37	18.9	37	18		-30.5@11.7 PAE 11.9%
					39	18.9	36	15.6		-28@11 PAE=10.2%
[81]	45nm SOI CMOS	Compensated Distributed Balun	2	25.8-43.4 (50.9%)	24	20.0	38.9	20.1*	800 MHz 64-QAM 2-CC OFDM 5G NR	-25.2@10.9 PAE=14.2%
					37	20.0	38.7	19.9*		-27.9@10.2 PAE=13.6%
					39	19.1	38.6	20.0*		-26.1@10.2 PAE=13.4%
This work	22nm CMOS FDSOI	RC feedback 1-stage diff.	1.8	19.1-46.5 (83.5%)	24	14.6	26.1	15.7	9x100 MHz 256-QAM 5G NR	-24.6@7.3 PAE=8.1%
					28	14.0	19.9	14.5		-23.7@6.6 PAE=6.2%
					37	13.6	18.5	15.4		-23.7@6.0 PAE=5.4%
					39	12.9	15.2	14.7		-24.2@5.6 PAE=13.9%
This work	40-nm GaN	3rd-order input match 1-stage	4	18-40.3 (76.5%)	24	18.6	34	7.8	9x100 MHz 256-QAM 5G NR	-27.7@9.7 PAE=8.1%
					28	18.6	42.1	9.2		-27@11.3 PAE=13.9%
					39	17.2	26.0	8.7		-27.9@10.8 PAE=12.6%
This work	40 nm GaN*	3rd-Order Input Matching; Differential	6	20.1 – 44.3 (75.2%)	24	23.5	24.9	12.5	N/A	N/A
					28	23.6	26.6	13.3	N/A	N/A
					39	23.6	27.9	11.7	N/A	N/A
					44	23.3	23.3	10.4	N/A	N/A

*EM PEX Simulated **Estimated graphically

4.5.4 Conclusion

This work presented three different, very broadband, linear, and efficient PA that can operate over the entire key mm-Wave 5G FR2 band of 24 – 44 GHz in two different state-of-the-art semiconductor IC technologies. Using a 3rd-order input matching network, a broadband single-ended 40 nm GaN PA was designed (i.e., GaN PA #1), achieving excellent performance from 18 to 44 GHz, with highest measurement max. PAE/ $P_{OUT,SAT}$ of 42.1% /18.6 dBm at 28 GHz at V_{DD} = 4 V. Small signal and large signal CW measurement data matched well with EM PEX simulations, with max. PAE above ~20% across the entire frequency band. When inserting a 256-QAM 5G NR signal varying in BW from 50 MHz to 9x100 MHz at 24, 28, 37, and 39 GHz, there is virtually no degradation in the linearity as measured by ACLR for this GaN #1 PA. This PA is used to design a broadband differential PA with neutralization capacitors in the same GaN technology (i.e., GaN PA #2), which achieves similar PAE and BW in PEX EM simulations as the single ended version, but with higher ~3 dB gain and higher $P_{OUT,SAT}$ as expected. Finally, a broadband 22 nm FD-SOI CMOS PA was designed, achieving excellent broadband results in the FR2 band with an RC feedback network and a differential topology using neutralization capacitors. It achieves a 3-dB BW of 19.1 – 46.5 GHz and good max. PAE of 26.1% at 24 GHz and maintains max. PAE above 15.1% across the entire 24 – 39 GHz. Compared to the GaN #1 PA, increasing the 256-QAM 5G NR signal BW from 50 MHz to 9x100 MHz degrades the ACLR linearity of the CMOS PA more, suggesting that the GaN PA may be able to deliver significantly higher $P_{OUT,Linear}$ and $P_{OUT,SAT}$ than their CMOS counterparts for mm-Wave 5G applications, albeit at a considerable higher cost with a lower level of monolithic integration.

5 FUTURE WORK AND CONCLUSIONS

Throughout this present work, there have been many circuits designed in PEX simulations that have not yet been validated with measurement data. Many designs are not available yet due to the IC fabrication time, but some of these designs have a high chance to be working, as they are modified/improved versions of previous designs. This work will list the PA circuits that will be measured after these ICs return from the foundries, and also discuss the future research work on high efficiency broadband mm-Wave PAs that can be continued to enable 6G and next-generations of communication networks.

5.1 Future GaN PAs

This work will start by discussing broadband high~~ly~~-efficient medium power mm-Wave GaN PAs that still need to be measured once the chips are back from being fabricated.

5.1.1 Class J GaN PA Stability Improvement

In Section 4.1, a Class J GaN PA was presented which showed rather promising measurement results. It was able to achieve measured max. PAE > 20% at 22 GHz and 26 GHz. However, there were large mismatches on the measured vs. EM simulated S_{22} and S_{11}, and when reducing the drain voltage to improve the PAE, the mismatch and the instability of the PA becomes even worse. The S-parameters from Section 4.1 are re-plotted in Figure 5.1, which shows S_{22} at 20 GHz with V_{DD} = 12 V is +4.6 dB and with V_{DD} = 6 V, it is +8.8 dB, thus there is a large mismatch and instability in this design which is exasperated with decreasing supply voltage. This PA was initially designed in simulation for V_{DD} = 12 V and thus lower supply voltages were not looked at. Thus, amplifier was simulated with a lower V_{DD}= 6 V (Figure 5.2), and it did show that at this biasing condition, S_{22} is positive and the amplifier is unstable at the same frequency of ~ 20 GHz as in measurements. Note that the measured S_{11} also becomes positive at ~ 28 – 30 GHz, but this was not seen in PEX simulation. This warrants for a re-design, keeping this mismatch and instability in mind, to hopefully improve the PA performance and especially stability as the modified Class J PA was taped out in January 2022.

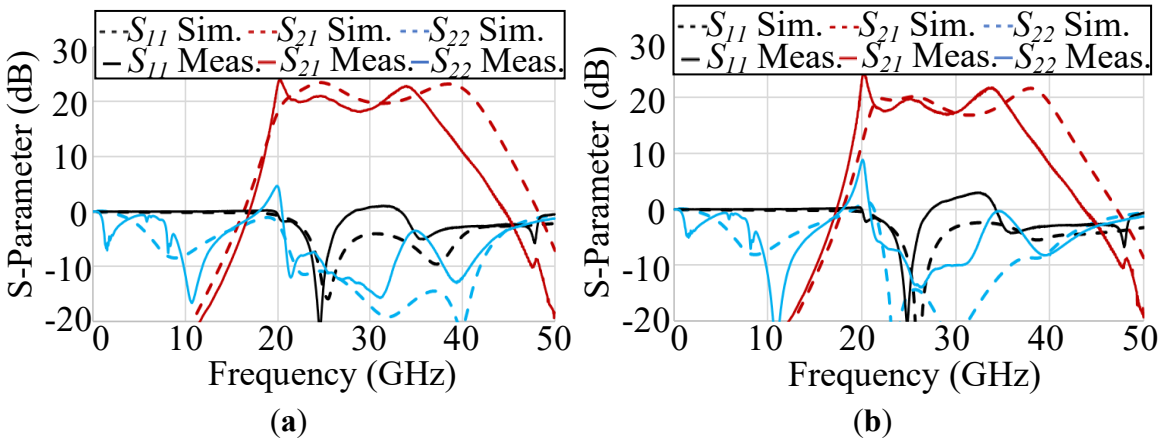


Figure 5.1: S-parameter Measurement vs. EM PEX Simulations at (a) V_{DD} = 12 V and (b) V_{DD} = 6 V of the Broadband GaN Class J PA from the first GaN Tapeout

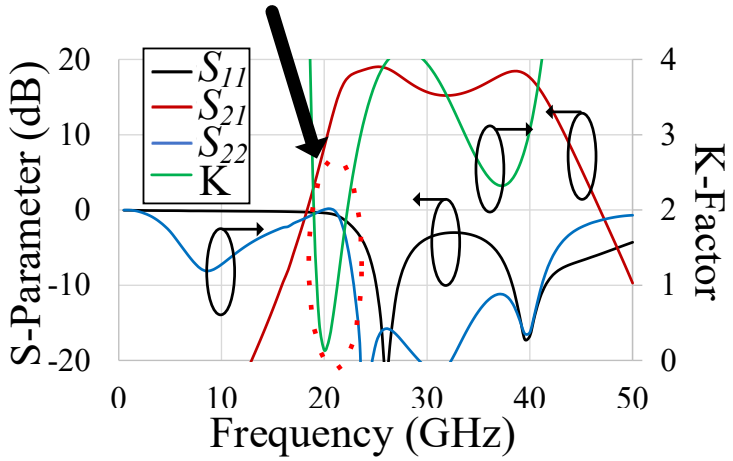


Figure 5.2: S-parameter EM PEX Simulations with V_{DD} = 6 V, Highlighting the Mismatch of the Broadband GaN Class J PA from the first GaN tapeout that Shows a Big Dip in Stability at ~20 GHz, Similar to what was Observed in Measurement

5.1.2 Asymmetrically Combined PAs

The asymmetrically combined GaN PAs shown in Section 4.1 have also been tested and unfortunately, shown to be unstable. For the single stage version, the PA was only simulated and designed with a Class AB biasing condition. However, in the process of turning on the design, it starts to oscillate. Going back into EM simulation, it was seen to be unstable under colder biasing points. Figure 5.3(a) shows the measurement vs. EM simulated S-parameter results with V_{DD} = 6 V, I_{D1} = ~1 mA and I_{D2} = ~3 mA. This suggests quite good measurement to simulation agreement at this biasing point. However, when turning on the PA past this point, it does begin to oscillate. When going back to simulation and reducing the drain voltage, or making the gate voltage more negative, the *k*-factor does drop below 1 in EM PEX simulations, so this may explain why the PA was not stable under colder biasing conditions (e.g., V_{G1} = V_{G2} = -0.4 V, V_{D1} = V_{D2} = 6 V in Figure 6.3 (b)). Thus, because there was good simulation agreement to

measurement with the colder biasing, this work can show good promise if the design could be stabilized in EM PEX simulations for the future work.

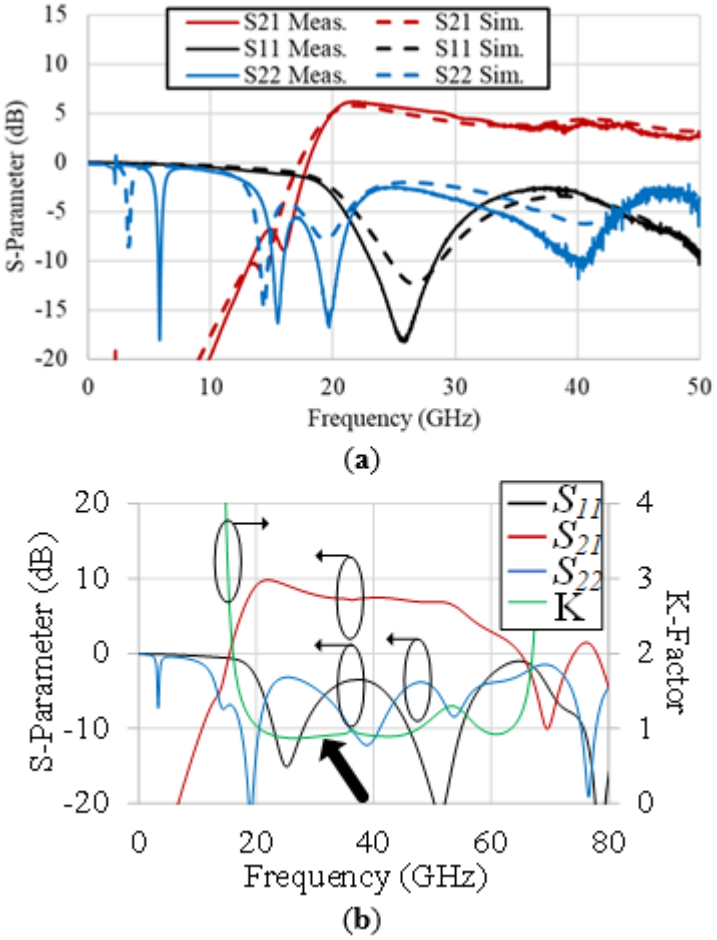


Figure 5.3: S-parameter Measurement vs. EM PEX Simulation with (a) I_{D1} = 1 mA and I_{D2} = 3 mA, and (b) S-parameter EM PEX Simulation Showing the Instability with Colder Biasing (V_{G1} = V_{G2} = -0.4 V V_{D1} = V_{D2} = 6 V) and of the Broadband GaN One-stage Asymmetrically Combined PA

The two-stage asymmetrically combined PA presented in Section 4.1 was also tested and had also shown unstable. Unfortunately, this PA could not be turned on enough to get gain before it would begin to oscillate (Figure 5.4). Going back into simulation, it was seen that the two-stage did have a lower frequency oscillation that was not seen in the initial design of this PA. The plan is to made it stable in simulation for the future work.

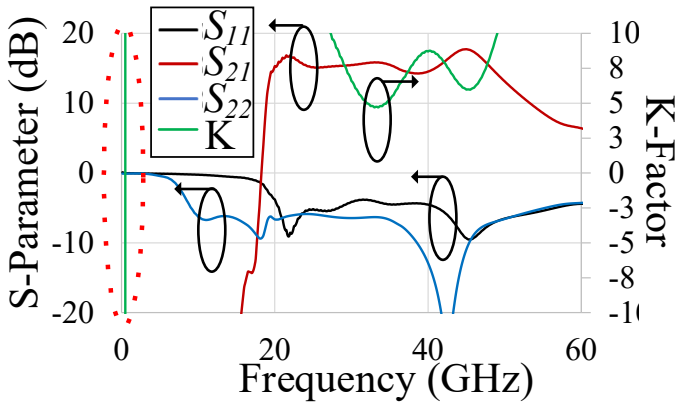


Figure 5.4: S-parameter EM Simulation with the Stability of the GaN Two-stage Asymmetrically Combined PA that Shows a Low Frequency Oscillation that was not Initially Seen

A three-stage asymmetrically combined PA was also designed, expanding upon the two-stage design shown here. This PA was designed to achieve $P_{OUT} > 1$ Watt and with gain ~20 dB. This PA has not been measured yet and is thus something that needs to be measured for my future plans. Figure 5.5 shows schematic as well as the S-parameter simulation of this PA, which is done with EM extraction using AXIEM again. This shows that it does achieve ~20 dB of gain but has a slightly narrower BW of ~20 – 50 GHz, as opposed to the 18 – 50 GHz that this work would have liked to achieve.

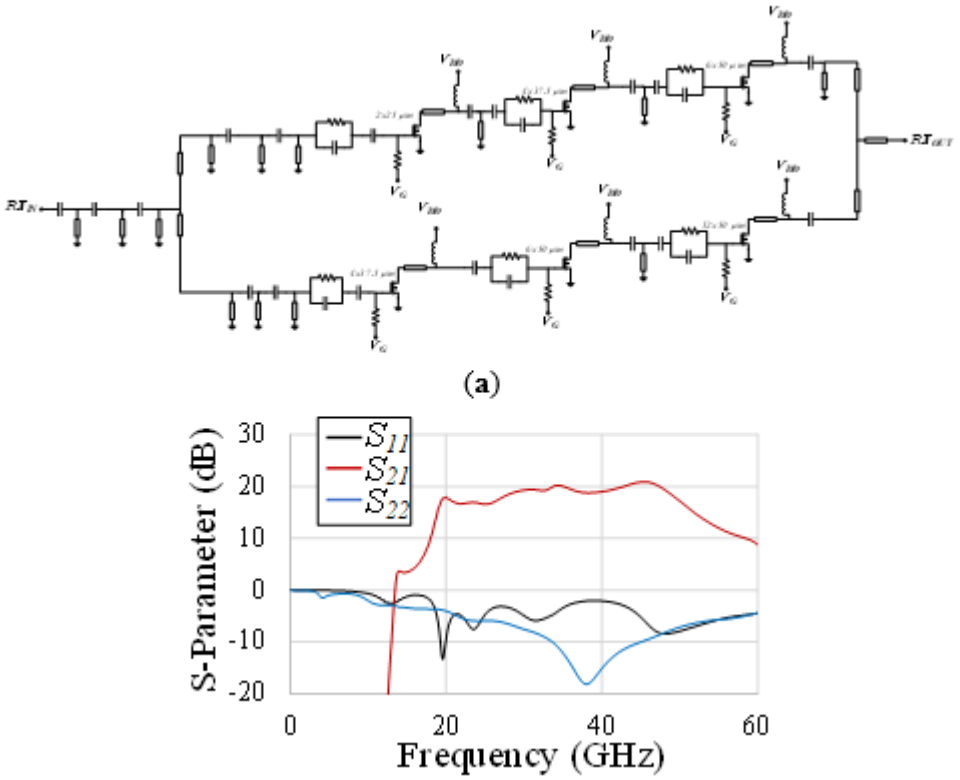


Figure 5.5: Schematic (a) and (b) S-parameter EM Simulation of the GaN Three-stage Asymmetrically Combined PA

The large signal EM simulations for the GaN three-stage asymmetrically combined PA are shown in Figure 5.6. It shows that at 38 GHz, the PA achieves impressive performance of 22.9% max. PAE with $P_{OUT,\,SAT}$ of 31.5 dBm and 18.8 dB small-signal gain. Thus, this PA is able to achieve the desired performance at this frequency; however, other frequencies do not perform as well, with 26 GHz having a large dip in max. PAE to ~8.5%. The performance of this PA at several different frequencies is shown in Table 5.1.

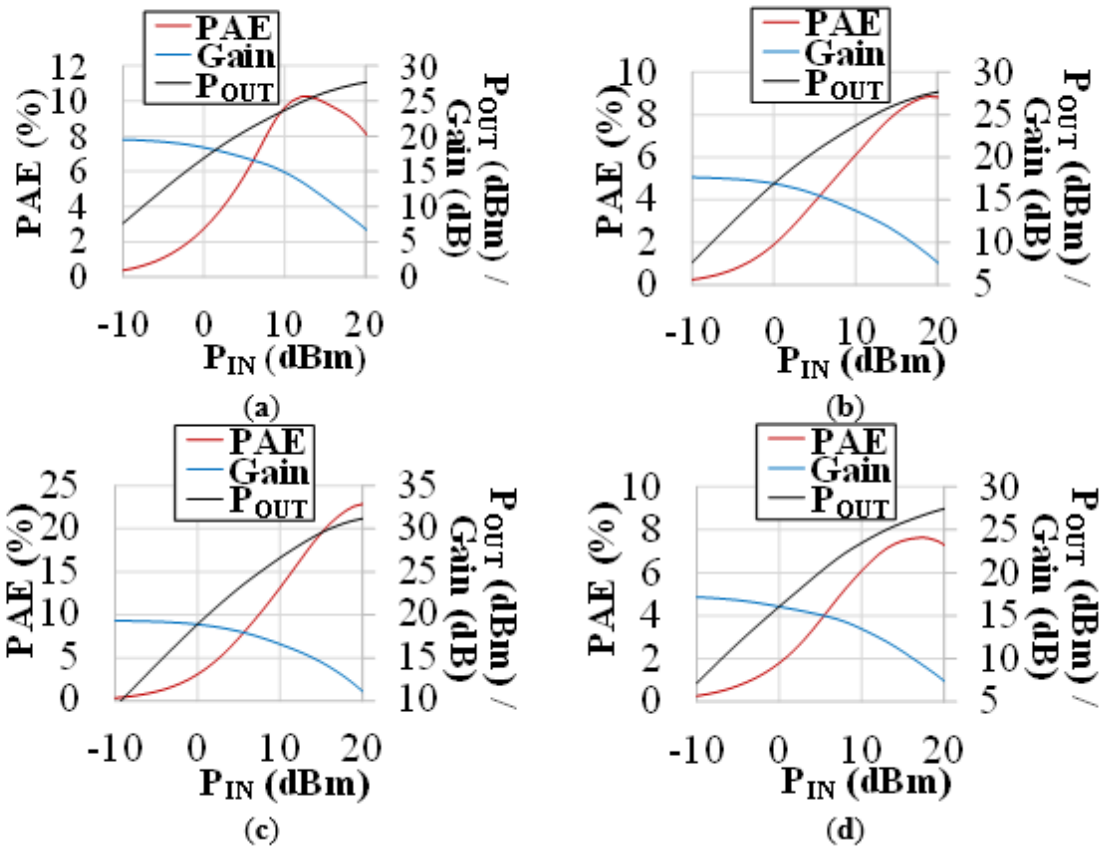


Figure 5.6: Large Signal EM Simulations at (a) 20 GHz, (b) 26 GHz, (c) 38 GHz and (d) 50 GHz of the GaN Three-stage Asymmetrically Combined PA

Table 5.1. Summary of the EM Simulation Results of the GaN Three-Stage Asymmetrically Combined PA

Freq. (GHz)	S_{11} (dB)	S_{21} (dB)	Max. PAE (%)	OP_{1dB} (dBm)	$P_{OUT,\,SAT}$ (dBm)
20	-9.6	18.0	10.3	17.6	26.9
26	-3.5	16.9	8.9	18.5	27.9
32	-5.7	19.2	15.2	18.3	30.8
38	-3.0	18.8	22.9	18.3	31.5
44	-4.0	20.5	14.3	18.8	29.9
50	-7.9	17.5	7.6	16.1	27.9

5.2 22FDX CMOS SOI PAS

In Section 4.2, several broadband mm-Wave high efficient CMOS PAs using GlobalFoundries 22FDX FD-SOI technology was reported. In this section, some improvements that have been made to further improve upon these designs will be discussed.

5.2.1 Broadband Cascode CMOS SOI PA with I/O Baluns On-Chip

First, the differential CMOS PA designs in Section 4.2 all used only an output balun. The next iteration of this work looked at adding an input balun to these PAs, as the use of transformers for wideband PAs has been reported [82]. Figure 5.7 shows the schematic and S-parameter simulations of the broadband hybrid cascode/stack 22FDX PA with RC feedback and both I/O baluns integrated on-chip. This design also uses *x*2 the device size of what was used in Section 4.2 (i.e., using 2 *x* 40 µm size devices). All the PEX simulations in this section are done in the same way as in Section 4.2, Calibre xACT R+C+CC extraction. It shows that the input matching is much better when using one of these broadband input baluns on-chip, and this work achieved great S_{11} of < -10 dB across the entire frequency band of over 37 GHz. This PA is still quite broadband and ESD-protected; and it achieves max. S_{21} of 17.4 dB with a small-signal 3-dB BW of 14.7 GHz – 51.8 GHz (absolute BW= 111.6%) in PEX simulations.

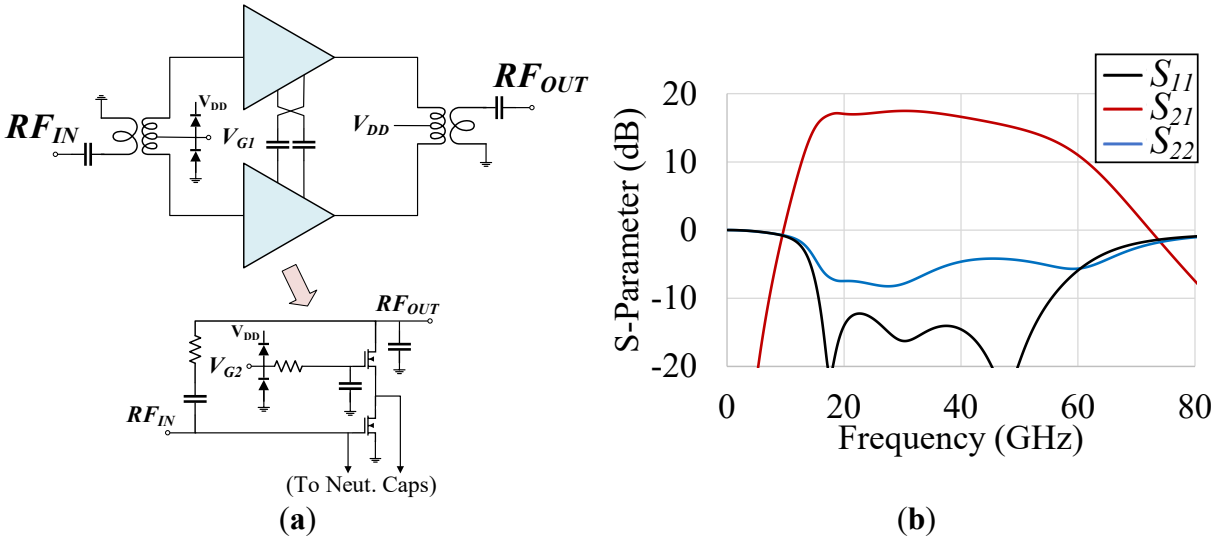


Figure 5.7: Schematic (a) and (b) S-parameter PEX Simulation of the 22FDX Broadband Hybrid Cascode/stack PA with RC Feedback and I/O Balun

The large signal PEX simulation results of this fully integrated CMOS PA at 24 GHz and 39 GHz are shown in Figure 5.8, and more data summarized in Table 5.2. The data suggests this PA achieves max. PAE at 24 GHz of 34.9%. At 24 GHz, this PA also achieves $P_{OUT,\,SAT}$ of 19.1 dBm, OP_{1dB} of 16.4 dBm and PAE@P_{1dB} of 17.9%. Thus, this PA achieves good results in PEX simulation, and this work are eager to test this PA when this work receive the dies back.

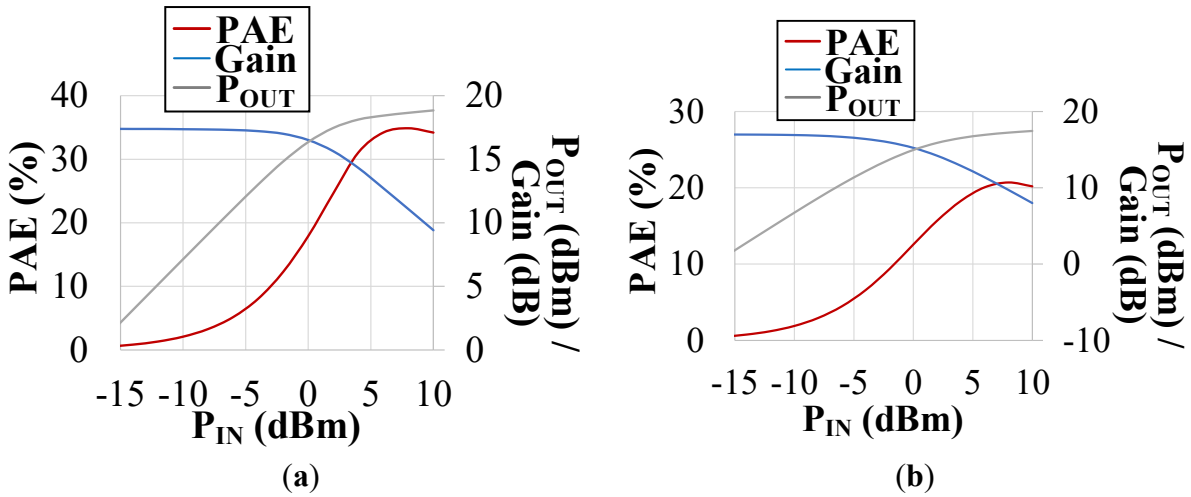


Figure 5.8: Large Signal PEX Simulations at (a) 24 GHz and (b) 39 GHz of the 22FDX Broadband Hybrid Cascode/stack PA with RC Feedback and Integrated I/O Baluns

Table 5.2. Summary of the PEX Simulation Results of the 22FDX Broadband Hybrid Cascode/Stack with RC Feedback and I/O Baluns On-chip

Freq. (GHz)	S_{11} (dB)	S_{21} (dB)	Max. PAE (%)	PAE@P_{1dB} (%)	OP_{1dB} (dBm)	$P_{OUT,\,SAT}$ (dBm)
18	-20.4	17.0	22.4	9.4	13.9	18.8
24	-12.4	17.1	34.9	17.9	16.4	19.1
34	-14.9	17.3	25.3	15.7	15.8	18.2
39	-14.2	16.7	20.7	9.4	13.7	17.8
50	-19.4	14.9	13.1	4.1	10.2	16.6

5.2.2 Broadband Stacked CMOS SOI PA

The previous broadband designs in Section 4.2 used a hybrid cascode/stacked-FET topology (between a classic cascode and a stacked PA), so this work also designed the next PA as a stacked PA for comparison. Note that a stacked topology was investigated in Section 4.2, but this was a narrowband design. Figure 5.9 shows the S-parameter PEX simulation results of this PA, where a small cap of 55 fF is used at the gate of the stacked NFET. Compared to the hybrid cascode/stacked PA described in Section 4.2, the gain of this stacked PA is lower as it achieves max. S_{21} of 15.1 dB with 3-dB BW of 18.2 GHz – 49.8 GHz. This PA does achieve similar S_{11} as the version presented in Section 4.2. An input matching balun such as the one that was presented in the previous section was not used, as reasonable simulation results were achieved without the input balun and this work had already successfully measured without the input balun on the hybrid cascode/stack.

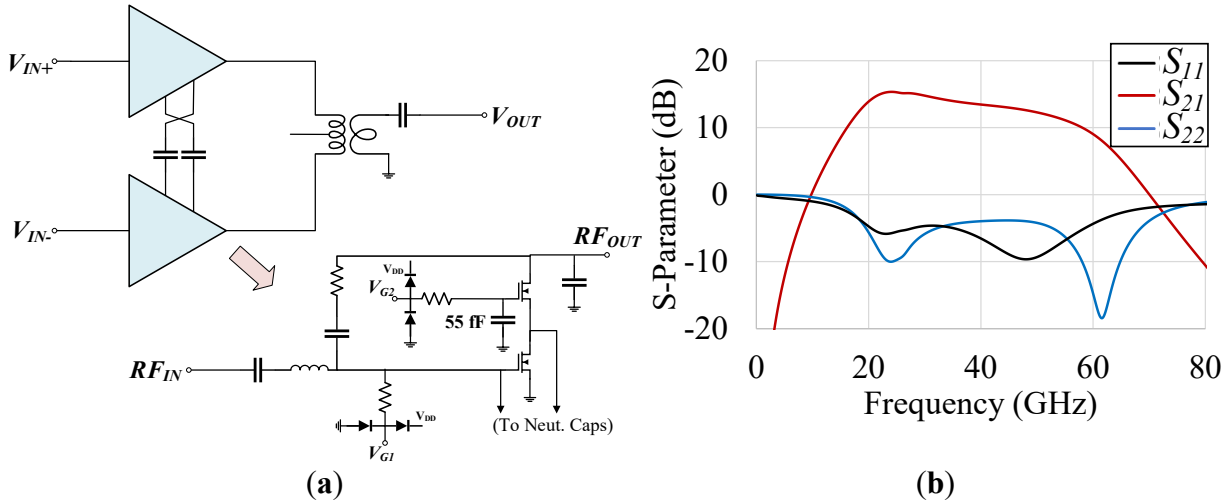


Figure 5.9: A Simplified Schematic (a) and (b) PEX Simulation of S-parameters for the 22FDX Broadband Stacked PA Design

Figure 5.10 shows the large signal PEX simulation results of the stacked PA at 24 GHz and 39 GHz, and this data as well as at other frequencies is summarized in Table 5.3. Compared to the PEX simulation results of the cascode PA presented in Section 4.2, this stacked PA achieves lower $P_{OUT,SAT}$ and OP_{1dB} than that of the cascode. For instance, at 24 GHz, this PA achieves $P_{OUT,SAT}/OP_{1dB}$ of 16.5 dBm/ 13.9 dBm, but the cascode achieves 17.8 dBm/ 14.3 dBm at 24 GHz. However, the max. PAE only degraded by ~3%. Although this PA does achieve inferior output power compared to the hybrid cascode/stack PA, the stacked version should have less stress across the top device, and thus may have better reliability performance; however, measurement results will need to be taken in the future to verify this point.

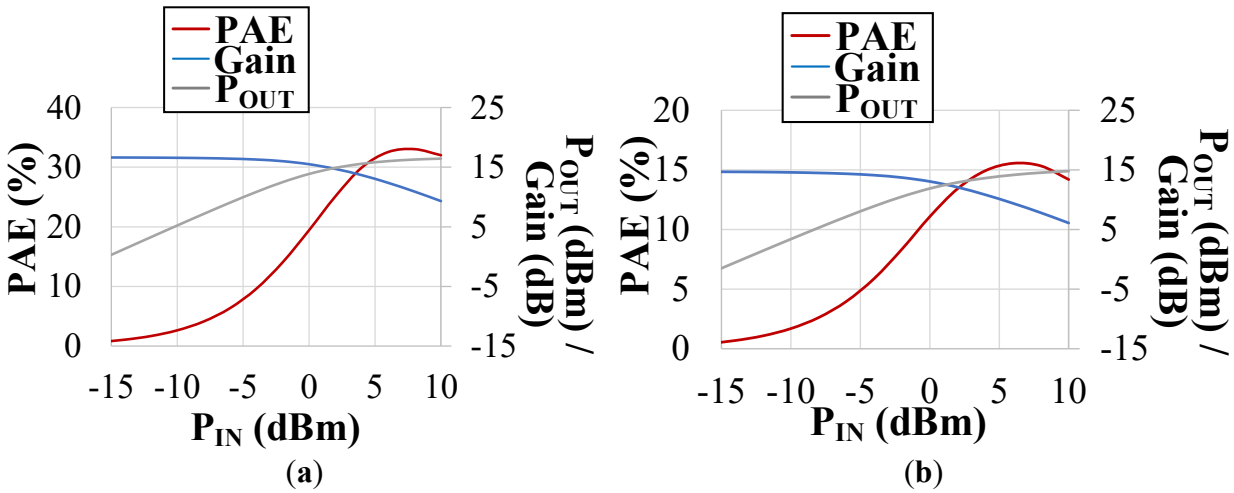


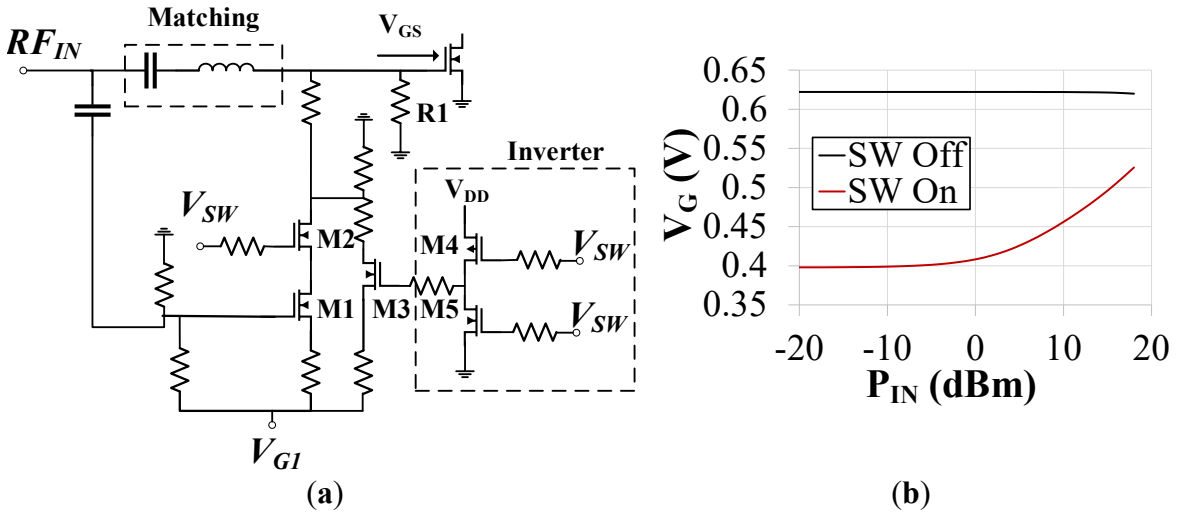
Figure 5.10: Large Signal PEX Simulation at (a) 24 and (b) 39 GHz of the 22FDX Broadband Stacked PA

Table 5.3. Summary of the PEX Simulation Results of the 22FDX Broadband Stacked PA

Freq. (GHz)	S_{11} (dB)	S_{21} (dB)	Max. PAE (%)	PAE@ P_{1dB} (%)	OP_{1dB} (dBm)	$P_{OUT,\ SAT}$ (dBm)
18	-3.5	12.1	14.9	9.3	11.0	14.1
24	-5.8	15.3	33.0	19.4	13.9	16.5
34	-4.8	14.0	18.3	9.9	11.2	15.1
39	-6.1	13.5	15.6	84	10.5	14.8
50	-9.3	12.3	12.7	6.3	9.3	14.1

5.2.3 Broadband Cascode CMOS SOI PA with Adaptive Biasing

The previous adaptive biasing circuit shown in Section 4.2 was then improved upon. That version had the FETs in the adaptive biasing circuit biased in the subthreshold region with minimum channel length that may be more susceptible to process variation [83], but the new design to be presented here is designed to have the FETs in the adaptive biasing circuit to be biased in triode region as in [62]. This is done as a MOSFET device in the triode region is a variable resistor and can charge/discharge considerably faster than the subthreshold devices. Figure 5.11(a) shows the new adaptive biasing circuit, and it begins similarly where RF is fed to the gate of M1 through a large capacitor. As the average input voltage at the gate increases, the voltage at the source increases due to the voltage drop through R1 and thus, the voltage at the gate of the PA device increases. In addition, a switch made out of M2 – M5 is added to turn on and off the adaptive biasing. When the V_{SW} = 0 V, M2 is off and the inverter, made of M4 and M5, turns on M3, which then turns on the biasing network (fixed bias to the PA). However, when V_{SW} = 1 V, M2 is on, and this turns on the adaptive biasing network as the inverter turns off M3. Figure 5.11(b) shows the P_{IN} vs. the voltage at the gate of CS device of the adaptive biasing PA (V_{GS}), which indicates that as P_{IN} increases from -20 dBm to 18 dBm, the voltage at the gate of the PA increases by ~ 0.15 V.



(a) (b)

Figure 5.11: Schematic of the Adaptive Biasing Network (a) and (b) P_{IN} vs. the voltage at the Gate (V_{GS}) of the Amplifying Device

The PEX simulation results of the S-parameters with the schematic of the entire adaptive biased differential CMOS PA using a hybrid cascode/stacked topology are shown in Figure 5.12. When the switch is turned on, the S_{21} reaches a maximum value of 15.7 dB with 3-dB BW of 19.7 GHz – 48.6 GHz; and when the switch is off, the max. S_{21} remains to be 15.7 dB and it achieves a 3-dB BW of 19.7 GHz – 50.2 GHz..

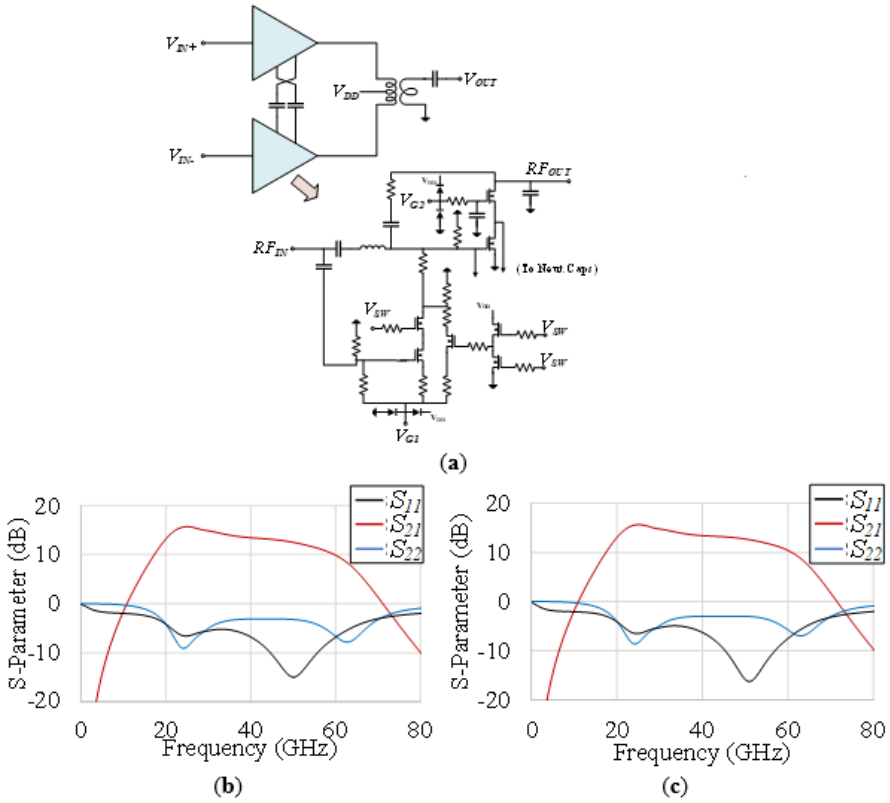


Figure 5.12: Schematic and PEX Simulations of S-parameters with the Switch Voltage "VSW" (a), (b) ON and (c) OFF for the 22FDX Broadband Hybrid Cascode/Stack PA with Adaptive Biasing

The large signal PEX simulations are shown at 24 GHz and 37 GHz with the switch voltage "V_{SW}" turned ON and OFF in Figure 5.13, and the data is summarized in Table 5.4. This shows that the PAE@P_{1dB} is able to improve by ~10% at 18 GHz and also at 24 GHz. Unfortunately, the performance seems to not be improved at higher frequencies above 34 GHz. However, this simulated performance of this adaptive-biased PA will need to be validated with measurements.

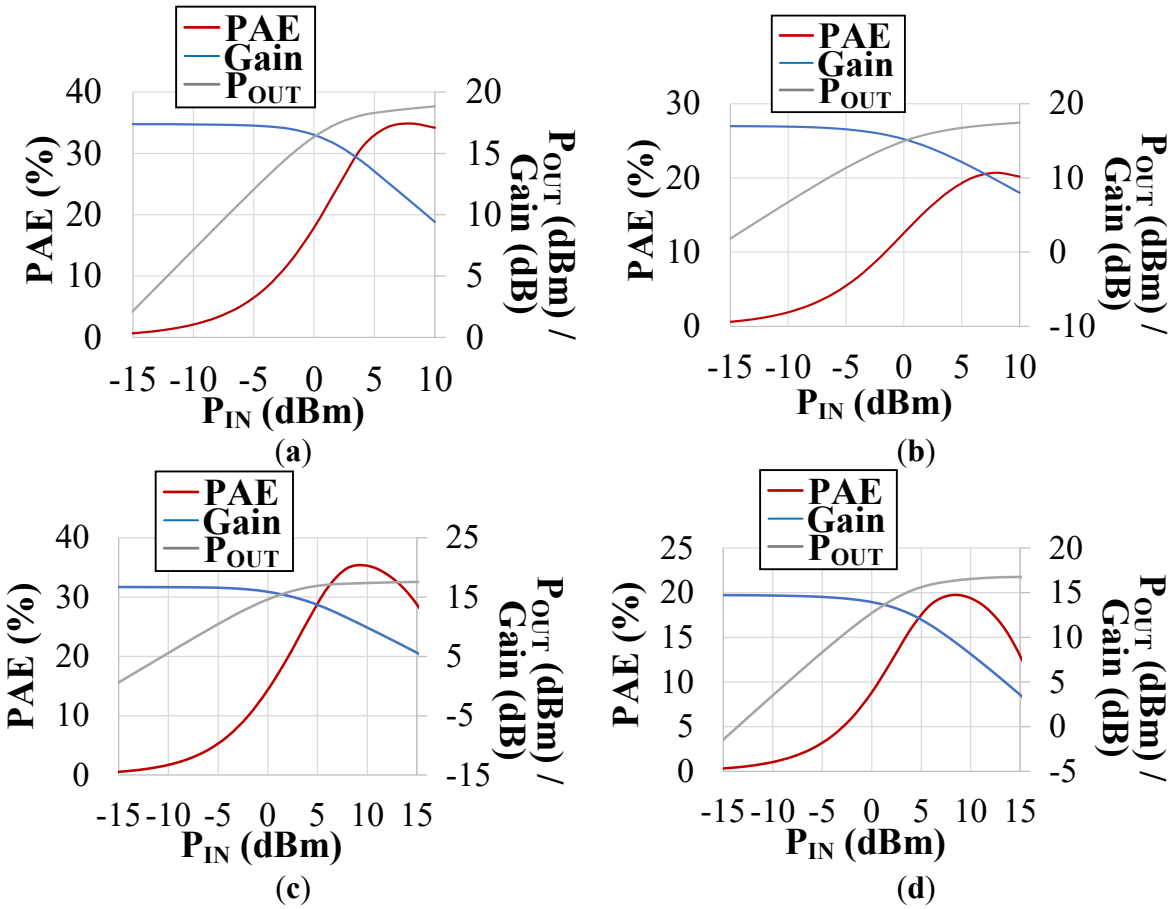


Figure 5.13: Large PEX Simulation with the Switch Voltage "V_{SW}" turned ON at (a) 24 GHz and (b) 39 GHz, and the "V_{SW}" turned OFF at (c) 24 GHz and (d) 39 GHz of the 22FDX Broadband Hybrid Cascode/stack PA with Adaptive Biasing

Table 5.4. Summary of the PEX Simulation Results of the 22FDX Broadband Hybrid Cascode/Stack PA with a Switchable Adaptive Biasing Network

Switch voltage "V_{SW}"	Freq. (GHz)	S_{11} (dB)	S_{21} (dB)	Max. PAE (%)	PAE@ P_{1dB} (%)	OP_{1dB} (dBm)	$P_{OUT,\,SAT}$ (dBm)
On	18	-4.1	13.0	30.7	**20.3**	14.9	17.2
	24	-8.6	15.5	33.2	**22.7**	15.2	17.2
	34	-5.0	14.0	22.7	**17.7**	15.4	16.7
	39	-5.9	13.4	20.1	11.5	12.6	16.7
	50	-15.8	12.7	17.0	9.7	12.0	16.3
Off	18	-4.2	13.1	31.3	13.4	14.3	17.2
	24	-6.5	15.5	32.8	14.4	14.6	17.2
	34	-5.3	14.1	22.0	12.3	14.0	16.7
	39	-6.4	13.4	20.0	12.4	14.1	16.7
	50	-15.0	12.4	16.8	9.9	13.3	16.4

5.3 Advanced 5G, 6G and Beyond

5G will continue to advance through the next few years, as Release 17 specifications is in the process of being published in 2022. Release 18 will begin to be studied in 2022 with its commercial deployment to be around 2025, which begins the release of 5G-Advanced. 5G-Advanced will build upon the 5G network and set the stage for 6G [84]. This will continue to be an important research topic, which is evident by the large amount of money being poured into developing these technologies from many governments across the world, as these technologies are critical to keep up with societal demands. For instance, the U.S. government has pledged $50 billion to be spent in the next 5 years for the development of their 5G network [85]. However, the mm-Wave 5G that this report focuses on is still in its early stage of market adoption and deployment. Currently, the FR2 band up to 52.6 GHz is being utilized but Release 17 will allow the full FR2 band up to 71 GHz [86]. Release 18 ("5G Advanced") plans to improve upon coverage and capacity as well as the experience of the user and making this network more energy efficient. Although the use of Release 17 will most likely start the process of *recommending* a functional framework to enable AI (artificial intelligence) and machine learning (ML) for the purposes of energy conservation, load balancing and network traffic management, 5G-Advanced will most likely have a larger focus on AI and ML and will *standardize* these to unlock the full potential of 5G by introducing intelligent networks as well an improving the user experience with eXtended Reality (XR)[84,86-87]. In addition, AI and ML solutions could also optimize multi-antenna systems such as MIMO (multiple-input multiple-output) antennas that were discussed earlier in this work. 5G-Advanced also aims to enable satellite to device communication [87].

Although there is still a lot of work to be done on 5G and 5G-Advanced, as technology progresses, new devices and new capabilities will need to be addressed for the 6G networks. Since this work are not sure what exactly these new innovations will be, this work cannot say with certainty what 6G will look like and thus some of the next conversations may be only ideas. However, the current consensus for the goals for the specifications will be achieving peak data rate of 1 Tb/s (as opposed to 10+ Gb/s for 5G) and latency of 100 μS, which is 1/10 of 5G. 6G will take advantage of higher mm-Wave frequencies, such as sub-THz (terahertz) frequencies (i.e., 100 GHz – 300 GHz) to accommodate even larger data rates. For instance, in the United States, the FCC opened an experimental 6G spectrum license in 2019, which allowed engineers to start developing 6G in the 95 GHz to 3 THz range [88].

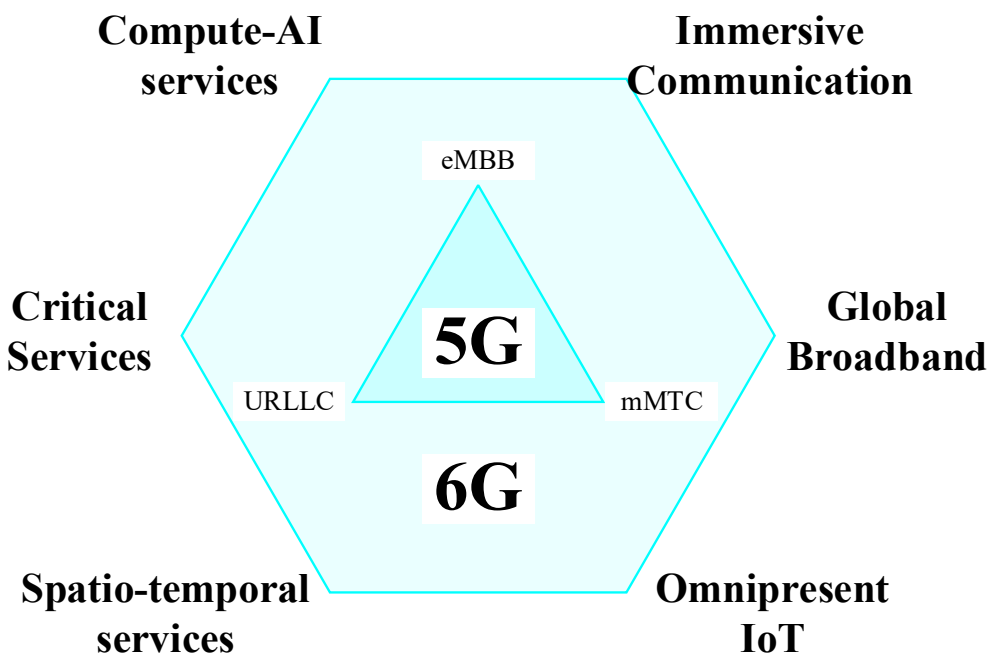


Figure 5.14: Ericsson's Vision of 6G Communication [89]

With the deployment of 6G, there will be even more of an emphasis on data and AI/ML. Ericsson, for example, envisions society to have wireless networks to be fundamental in all components of life, society, and industries. They give four drivers for 6G, which are trustworthiness, sustainability, application demands and simplifying life [89]. Figure 5.14 shows Ericsson's vision for 6G communication, which shows that it is expanding upon 5G with the 6 main characteristics for 6G, immersive communication, global broadband, omnipresent IoT, spatio-temporal services, critical services and compute-AI services. In addition, they envision a world that moves into a cyber-physical continuum where there is a connection between the physical and digital world through connected intelligent machines, internet of senses and a connected sustainable world [89]

Samsung, on the other hand, proposes three megatrends that are driving this research, frictionless networking, virtualization, and hierarchical AI [90]. They predict that there will be 500 billion connected devices by 2030, as machines will become the main user for 6G through AI. Some incredible applications that Samsung suggests are fully immersive 3D experiences (i.e., holographic-type communication made possible by 16k VR through at least 0.9 Gb/S streaming), digital twin (i.e., replicating physical beings to interact with reality via a virtual world) and a truly immersive XR with real-time audio, visual and haptic feedback for perfect remote operation, which would have applications for "digital health" as well as entertainment, science, education, and industries. [91]

5.4 Conclusions

5G eMBB (enhanced Mobile Broadband) promises 10^{+} Gb/s download speed and x100 more wireless devices compared to 4G with sub-1 mS latency time for UR/LL (ultra-reliable, low-latency) and mMTC (massive machine type communication), to meet all of these challenging specifications the higher mm-Wave frequencies in the FR2 band must be used. The current 5G FR2 band covers of 24.25 GHz to 52.6 GHz but the Release 17 will move this up to 71 GHz. For these multiple phased array antenna systems to function reliably, it is important for them to be energy efficient. Not only for shorter network latency time and reliability, but there is a strong emphasis on making these systems energy efficient going into 5G-Advanced and 6G networks for environmental purposes [92]. The RF/mm-Wave PA is frequently regarded as the most power-hungry component in a phased array system, and thus the research on highly efficient broadband PA design in mm-Wave/sub-THz frequencies remain highly relevant to the work going into 5G-Advanced and 6G. These new networks will also cover a large range of frequencies, and thus it may be advantageous to design power efficient broadband PAs to reduce system complexity, size and cost, especially in DoD (Department of Defense) applications. Thus, this present work of investigating the design of such PAs in several state-of-the-art technologies can be used as valuable information to help providing a roadmap in choosing semiconductor technologies and PA topologies for mm-Wave and sub-THz 5G/6G and DoD applications, as well as to gain design insights. It has been shown that GaN PAs can achieve superior power and linearity performance compared to the broadband mm-Wave PAs designed in silicon technologies, and if these GaN technologies can be massed produced (e.g., GaN on silicon) [51], it could drive the price down and thus may allow or GaN to be used in various medium-power and high-power PA applications. In addition, using RC feedback for mm-Wave PA design trades off the amplifier gain and thus PAE for large BW performance, but it keeps the size of the design smaller compared to using a higher order input matching network. The signals that are used in 5G and that will most likely be included in 5G-Advanced and 6G, and these high BW signals will still have high PAPR (peak-to-average power ratio) and thus efficiency at power back-off remains very important for commercial applications (but linearity at back-off is not critical for the majority of current DoD applications). Different adaptive biasing circuits in different silicon technologies were investigated as well as a Doherty topology to address these concerns. Wireless communication networks will continue to advance to help make our daily lives more convenient, but there are still many hurdles in highly-efficient broadband RF/mm-Wave/THz amplifiers circuits and systems design that the engineering communities must overcome.

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7 PUBLISHED WORKS

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[1] J.C. Mayeda, D.Y.C. Lie, J. Lopez, "Design of Broadband Highly Efficient Linear Power Amplifiers for mm-Wave 5G in 22nm FDSOI and 40 nm GaN/SiC", *Electronics,* 2022, 11(5), 683

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LIST OF SYMBOLS, ABBREVIATION, AND ACRONYMS

ACRONYM	DESCRIPTION
5G NR	Fifth-Generation New Radio
BiCMOS	Bipolar and Complementary MOS
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal-Oxide-Semiconductor
DoD	Department of Defense
E_g	Energy Bandgap
EM	Electromagnetic
FD	Fully-Depleted Silicon on Insulator
FEM	Front-End Module
f_{MAX}	Maximum Oscillation Frequency
FR2	Frequency Range 2
f_T	Cutoff Frequency
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GF	GlobalFoundries
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HRL	Hughes Research Labs
LNA	Low-Noise Amplifier
MIDAS	Millimeter-Wave Digital Arrays Systems
MIMO	Multiple Input Multiple Output
Mm-Wave	Millimeter-Wave
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PA	Power Amplifier
PAE	Power-Added-Efficiency
PAPR	Peak-to-Average-Power-Ratio
*p*HEMT	Pseudomorphic HEMT
P_{IN}	Input Power
P_{OUT}	Output power
P_{SAT}	Saturated Power
RF	Radio Frequency
SiGe	Silicon Germanium
SOI	Silicon-on-Insulator
V_T	Threshold Voltage