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MODELING AND TOPOLOGY EVALUATION FOR RECTIFIER CIRCUITS IN MEDIUM VOLTAGE DIRECT CURRENT SYSTEM

by

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Naval ship propulsion design is evolving from the traditional structure with a main engine driving a shaft through a reduction gear to a new architecture that uses electric drives powered from a direct current (DC) power distribution system. The goal of this thesis is to compare different medium voltage rectifiers interfacing an alternating current (AC) generator to a DC bus which can power the ship propulsion system. Power quality and efficiency of the power converters are the parameters used to compare four different rectifier circuit topologies: 2-level converter, 3-level converter, modular multi-level converter, and modular multi-level rectifier. Converter operating principles, design trade-offs, modeling characteristics, performance, and naval shipboard applicability are discussed in detail.

Using a power electronics simulation platform, the four power rectifier circuits and their controls are connected between a 6.6kV AC generator and a regulated DC bus that represents the shipboard platform. Inside each rectifier circuit, thermal properties of the chosen semiconductor switching devices and diodes are built in and losses are captured and analyzed in steady state operation. This study shows that the modular multi-level rectifier circuit is the most efficient, easiest to maintain, and the recommended topology for naval shipboard applications.

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MODELING AND TOPOLOGY EVALUATION FOR RECTIFIER CIRCUITS IN MEDIUM VOLTAGE DIRECT CURRENT SYSTEM

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LIST OF ACRONYMS AND ABBREVIATIONS

AC	alternating current
DC	direct current
EMI	electromagnetic interference
HVDC	high voltage direct current
IGBT	insulated gate bridge transistor
MMC	modular multi-level converter
MMR	modular multi-level rectifier
MVDC	medium voltage direct current
NAVSEA	Naval Sea Systems Command
PF	power factor
PI	proportional-integrational
PLECS	piecewise linear electrical circuit simulation
PWM	pulse width modulation
Qd0	quadrature-direct-zero reference frame
RPM	revolutions per minute
THD	total harmonic distortion

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I. INTRODUCTION

As the threat to national security increases, the communications and weapon systems that the U.S. Navy employs on naval vessels present power density challenges due to the need for dedicated power conditioning systems on alternate current (AC) distribution plants [1]. The U.S. Navy predominantly uses AC electrical distribution systems aboard naval vessels, while electric drive propulsion motors are powered from a direct current (DC) distribution system. DC power is obtained using gas-powered AC generators and AC/ DC switching power converters also called rectifiers. This study provides a topology comparison of four different active rectifier circuit topologies. For each converter circuit, the principle of operation is discussed in terms of switching cycles to create a DC current from a three-phase AC input. Each topology is designed to rectify the AC power provided from a generator to a stable DC bus, which can be used for shipboard electrical distribution. Each converter was evaluated for its steady state performance, where efficiency, voltage, current quality, and power losses are all studied to determine which of the chosen four represents the best choice for use in a medium voltage direct current (MVDC) distribution system. This study shows that the modular multi-level rectifier is the best choice for this type of operating environment and offers significant benefits.

A. SIGNIFICANCE OF RESEARCH

A study of efficient power converters is necessary in preparation for the future of naval warship power generation requirements. Distribution systems must be ready for a higher power demand, while maintaining volume and weight limitations inherent to ships. Power electronics are more complex than traditional means of power distribution because of their control systems, but they can be designed to facilitate ease of maintenance and system repair in the event of a failure.

With advancements in communications, weapons, and propulsion, AC distribution systems present power density challenges due to the need for dedicated power conditioning systems that can adequately provide for the increased loading [1]. Because of stability that must be afforded during significant power spikes of pulsed loads, traditional shipboard AC

systems do not have the power density required to meet transient load demands without additional large and costly energy storage systems [2]. Pulsed loads consist of high-powered lasers, high-powered electromagnetic systems, and high-powered electronic warfare systems that all work in conjunction to meet the missions of self and area defense [3].

Naval Sea Systems Command (NAVSEA) has incorporated electric propulsion systems on various ships, to include the Zumwalt class destroyer, and is focused on efforts to make electric ships part of the future fleet. The NAVSEA design practices and criteria manual states "The primary aim of the electric power system design will be for survivability and continuity of the electrical power supply. To ensure continuity of service, consideration shall be given to the number, size and location of generators, switchboards, and to the type of electrical distribution systems to be installed and the suitability for segregating or isolating damaged sections of the system" [3].

The electric drive motor in comparison to gas powered main engines has benefits ranging from size, efficiency, cost, and power availability for other high-power weapons and communication applications that are paramount to the mission of a warship [4]. The use of electric propulsion maximizes efficiency of the electrical distribution by minimizing heat losses and removing reactive power in transmission due to a DC-DC link bus voltage that provides power throughout the ship. The DC electrical power is then inverted at the location on the ship where AC power is required to drive a load. Electric drive motors offer the benefit of operating without a main engine that is directly coupled to the propeller. They are also smaller than their gas engine counterparts and run at closer to 100% of rated power [5]. They have an advantage of faster acceleration at lower speeds and can reach peak torque without having to increase revolutions per minute (RPM). Controlling the current into the electric drive motor controls the torque to the propeller. Since current can be controlled very quickly using power electronics devices, the acceleration rate can be much higher than that of a main engine where the rotational speed of the engine must change to change the speed of the propeller. Electric drive propulsion also allows for removal of the reduction gears on gas- and nuclear-powered ships. According to Ronald O'Rourke in a national defense strategy prepared for Congress, another benefit for ship

propulsion is the aspect of stealth by minimizing noise that comes from an AC bus transferring power throughout the ship [6].

Electric drive propulsion motors are powered from a DC distribution system where power is inverted back to an AC voltage and current at the motor. To achieve the demanded ship speed, an electric drive motor draws adequate AC current into the windings, which produces a torque and subsequently propels the ships. The electric drive configuration means that the propulsion of the ship is decoupled from the power the AC generator provides, and the AC generator will not have to change rotational speed based on a desired ship speed change. Thus, the AC generator can operate at different speeds optimized for efficiency at corresponding load conditions regardless of the motor speed. In addition, AC generator horsepower is directly proportional to its volume (rotor diameter squared multiplied by rotor active length) multiplied by its rotational speed, rotor flux, and stator [7]. In an electric propulsion system, the generator can rotate much faster and therefore theoretically provide the ability to reduce generator volume with the same power output. Lower volume corresponds to less weight and smaller machines that take up less space, which is a major advantage for ship systems.

While electric drive propulsion relies on DC power, the U.S. Navy predominantly uses AC electrical distribution systems aboard naval vessels. In traditional ship propulsion systems, an AC distribution plant is driven by three phase AC generators and the propulsion system uses a main engine to drive the shaft through a reduction gear. As the ship is commanded to speed up or slow down, the speed on the main engine is changed accordingly and the prime mover (shaft) rotates at much slower speeds than the generators for the distribution system. The operation of a motor at slower speeds means that it is heavier and takes up much more volume than machines that can rotate much faster and at constant speeds. The topologies being evaluated in this study will point to a recommended converter that can work effectively in an MVDC system and provide the necessary power requirement for the evolving needs of shipboard distribution.

B. RESEARCH PROBLEM SPACE

The system that is discussed throughout this document includes a gas-powered generator powering a stable DC bus, from which the DC voltage is inverted to AC by the motor drive unit for propulsion control [8]. With existing shipboard AC distribution systems, the frequency of the of the gas-powered generators must be adjusted to remain constant during all loading conditions. The need for frequency adjustment within existing systems greatly limits the operation of the gas generators and makes their operating points dependent on the loads, instead of operating at the most efficient condition [9].

This research is focused on MVDC distribution systems which allow the use of higher speed generators, thereby reducing their size and weight with respect to the generators currently in use. These smaller machines are not only significantly smaller and lighter but provide the additional benefits of lower torque and higher power density. Gas generators onboard military ships providing power for distribution systems have low efficiency values that are typically around 40% [9]. The decoupling of the MVDC system allows these generators to operate at a range of speeds that give greater flexibility of operation with fuel and power generation efficiency in mind.

An additional benefit of the MVDC systems is the efficiency that can be realized from the use of solid-state transformers in stepping up or down voltage levels. Solid-state transformers enabled by the semiconductor-based power electronics operate at a few kHz up to a few hundred kHz, leading to a much higher power density and a much lower weight compared to the traditional transformers used in a MVAC system [10].

C. RESEARCH QUESTION

In the context of an MVDC system, which converter topology is the best for efficient rectification in Naval propulsion?

D. APPROACH

Four active front end rectifier topologies are studied in this thesis: the classic 2-level converter, the T-type 3-level converter and the modular multi-level converter, which is widely used in industrial applications, and the new modular multi-level rectifier. All four

topologies are transformer-less configurations that achieve high power density and efficiency. They also have a much-improved power quality compared to a diode rectifier.

E. CHAPTER OVERVIEW

In Chapter II the benefits of using active rectifiers versus diode rectifiers are discussed together with the detailed operating principles of each converter. Chapter 3 introduces the control system architecture and its design. It also features an overview of the steps taken to model the topologies through simulations. Chapter 4 discusses simulation results for each topology and provides a comparison of benefits for use in shipboard MVDC systems. Lastly, Chapter 5 summarizes the results and suggests future work on the basis that the modular multi-level rectifier (MMR) is the most suitable choice in power conversion for naval shipboard distribution.

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II. OPERATION PRINCIPLES OF ACTIVE RECTIFIER TOPOLOGIES

In this chapter, the basic operation of an active rectifier is introduced, followed by the detailed operation of each different topology. The benefits of active rectifiers are explored, and that concept is carried into the design of each active rectifier topology. The operating principles of the four converters chosen for this study are discussed in detail in terms of how they operate, how they were be designed for simulation, and how they are controlled.

A. PASSIVE VS. ACTIVE RECTIFIERS

Typically, AC power from the generator is converted to DC through a rectifier. There are two types of rectifiers, passive rectifiers and active front end rectifiers. Passive rectifiers are bulky, lossy and costly [11]. Active rectifiers were utilized in this topology comparison study and provide many benefits as compared to passive rectifiers.

The passive rectifier, which is also called a diode rectifier, usually consists of a simple design of diodes arranged in a full bridge configuration. Although very unlikely to fail, they require the use of bulky and heavy capacitors for power factor (PF) correction [12]. Active rectifiers are much more complex due to the control circuitry that must be implemented into the design, but they do not require large capacitors for power factor correction, and they also provide the benefit of low harmonic current [12].

The passive rectifier consists of line-frequency transformers to improve the AC side power quality. The basic three-phase diode rectifier consists of 6 diodes, two diodes per phase. Diodes are inexpensive and simple in operation but are not controllable devices and draw currents with large harmonics of the fundamental frequency, which cause significant distortion in the source voltage [11]. In other words, even with a pure sinusoidal voltage source at the input, the diode rectifier input currents are heavily distorted. When the current is distorted, the source voltage becomes distorted, and all other loads connected at the point of common coupling are affected. Harmonics can be reduced by placing filters at the input

or connecting multiple diode rectifiers in parallel or in series with transformers, but the transformers and bulky and lossy.

Transformer-less active front end rectifiers reduce harmonics and are small enough that they no longer become a design constraint in shipboard applications. Instead of diodes, an active front end uses controllable switching semiconductors such as insulated-gate bipolar transistors (IGBTs), which can be controlled to draw a sinusoidal input current, to minimize the total harmonic components. The rectifier input current can still contain some harmonics, but at frequencies close to the switching frequency of the IGBTs, which is much higher than 60Hz and can be eliminated by LCL filters of moderate size and weight [11]. Other than the harmonics, the power factor at the generator terminal can also be controlled by an active rectifier to be close to unity. The high-power quality is one reason why active front end rectification was chosen for this topology study.

B. ACTIVE RECTIFIER BASIC OPERATION

The active rectifier needs to accomplish two main goals:

- control the DC bus voltage
- control the active and reactive power at the AC input

The main function of the active rectifier, like the diode rectifier, is to convert AC voltage into DC voltage. Unlike the diode rectifier, an active rectifier has the ability to keep the DC bus voltage constant. There are capacitors at the output of all rectifiers, as shown in the following figure. In Figure 1, the rectifier is on the left side providing constant current to the DC load on the right side.

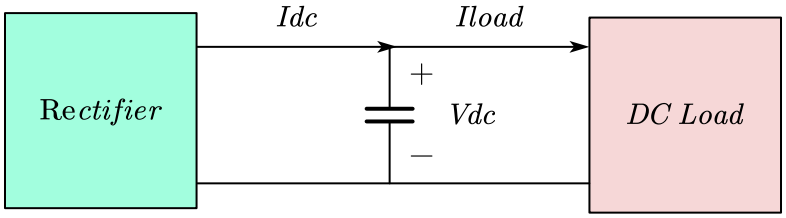

Figure 1. DC side capacitor equivalent circuit

I_{load} represents the load current. To keep the DC bus voltage *VDC* constant, the active rectifier needs to control its DC side output current I_{dc} to match I_{load}. If I_{dc} is higher than I_{load}, the capacitor or DC bus voltage increases. Otherwise, the DC bus voltage drops. Since the load current always varies, the active rectifier needs to change I_{dc} consistently.

During this regulation, the product of I_{dc} and V_{dc} equals the rectifier output power. To provide such power, the active rectifier needs to control the input power received from AC side.

As shown in Figure 2, the three-phase AC voltage sources at the generator terminal are modeled as V_{ga}, V_{gb} and V_{gc}. The active rectifier acts as a controlled three-phase voltage source (modeled as V_a, V_b and V_c). Thus, by controlling the amplitude and phase angle of the three-phase voltages, the three-phase currents I_a, I_b and I_c can be regulated, as well as the active power and reactive power. The detailed control method is explained in chapter 3. Figure 2 shows the ac side equivalent circuit for these modeled systems.

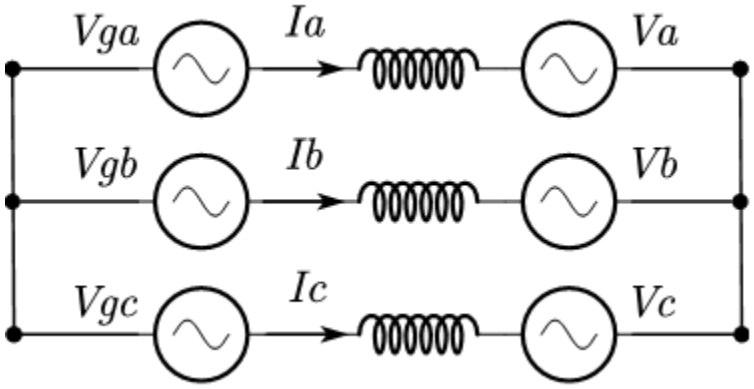

Figure 2. AC side equivalent circuit

C. TWO-LEVEL CONVERTER

The 2-level converter is the most basic three-phase voltage source converter topology widely used to reduce the AC input harmonic distortion compared to a 6-pulse rectifier circuit. The three-phase 2-level converters have IGBTs with anti-parallel diodes where 6-pulse rectifiers have thyristors or diodes. The anti-parallel diodes allow for current to be bi-directional. The 2-level converter can control the power flow in either way between the generator and DC bus. However, in Navy applications, where a gas turbine is used as the prime mover to drive the generator, inverted power from the DC bus to the AC turbine is unnecessary. Figure 3 shows the basic setup of the 2-level rectifier circuit configuration.

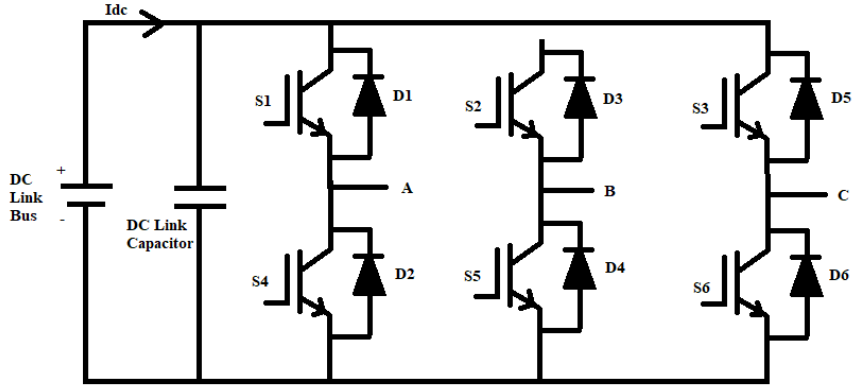

Figure 3. 2- level converter diagram

By controlling the gate signals of the switching devices, the switching devices can be turned on or off. When the top device, such as S1 is turned on and the bottom device S4 is turned off, the phase leg output voltage, such as the voltage at terminal A, is equal to the positive DC bus voltage. When the top device is turned off and the bottom device is turned on, the phase leg output voltage equals the negative DC bus voltage. Then by controlling the time distribution between the two voltage levels, i.e., using pulse width modulation (PWM), the average output voltage of such phase leg in each switching cycle is controlled to synthesize the required AC output voltage or DC output voltage.

One example is shown in Figure 4. The red waveform is the output PWM waveform of a 2-level converter, and the green wave represents the filtered sinusoidal voltage. It

should be noted that all devices in a 2-level converter must be rated at the full DC link voltage and load current because at each switching event, the IGBT switches the full DC link voltage and load current.

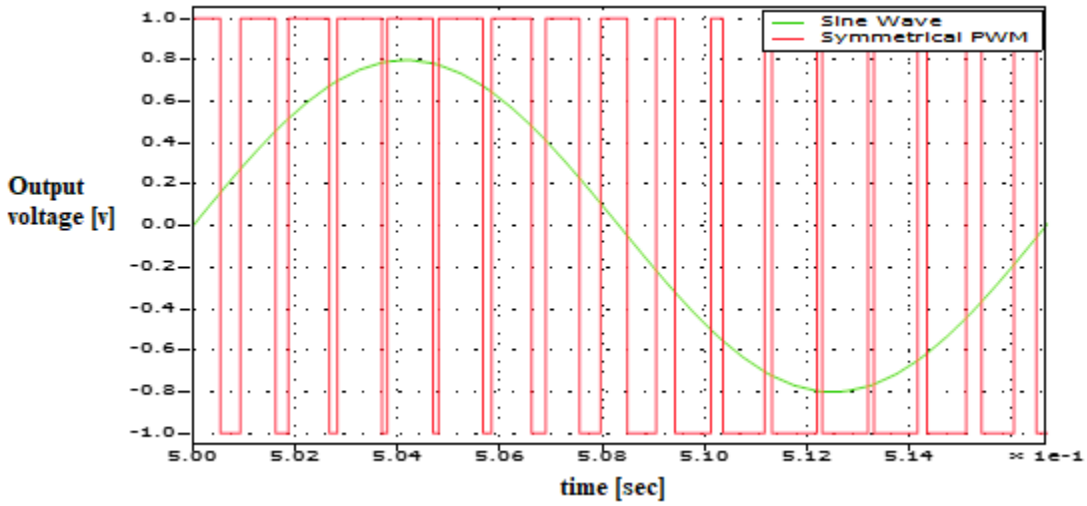

Figure 4. 2-level converter switching waveforms. Source: [13]

D. THREE-LEVEL T-TYPE CONVERTER

A 3-level T-Type converter topology is shown in Figure 5. It consists of the baseline 2-level converter with the additional bidirectional current capability devices that are placed into the circuit between the midpoint of the DC link and AC output terminals [13]. Each phase leg consists of four IGBTs with antiparallel diodes, named T1, T2, T3 and T4. When only T1 is turned on, the phase leg AC output voltage is equal to the positive DC bus voltage. When only T2 and T3 are turned on, the phase leg AC output voltage is equal to the neutral point voltage of the DC bus. When only T4 is turned on, the phase leg output voltage is equal to the negative DC bus voltage. In other words, there are three possible output voltage levels on the AC side, which is the reason for labeling this topology a 3-level converter. The 3-level converter is used in this thesis because this topology has been evaluated and the case has been made for its applicability in high-speed motor applications in [14]. There are many types of 3-level converter designs, and all have similar performance in terms of efficiency and THD. Because of the operating similarity, the analysis presented

here is valid for other 3-level converter topologies for this high-level system analysis. Figure 5 shows the 4-level T-type rectifier circuit configuration.

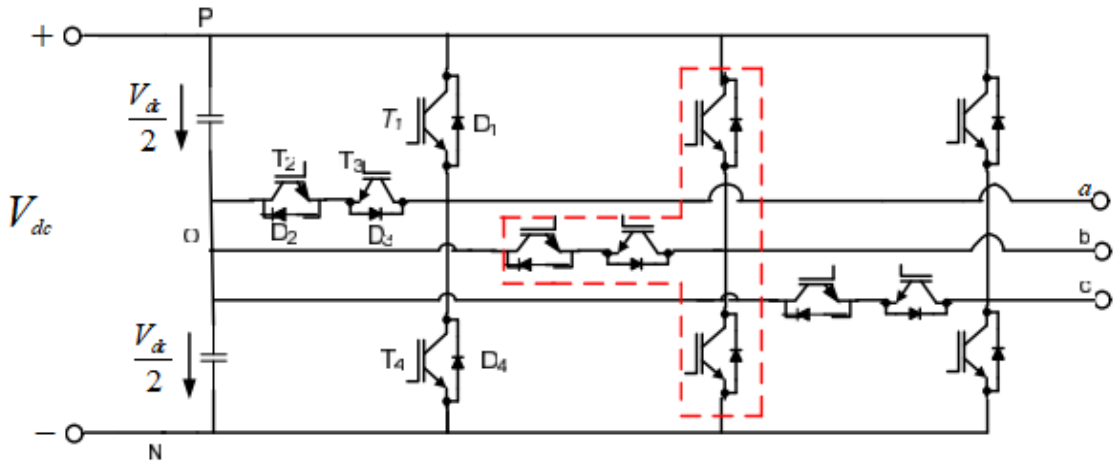

Figure 5. 3-Level T-Type converter circuit diagram. Source: [13]

Using pulse width modulation, the output sinusoidal voltage can be synthesized with the three voltage levels as shown in Figure 6. The red waveform is the output PWM waveform of the 3-level converter, and the green wave represents the filtered sinusoidal voltage. Compared to the 2-level converter, the sinusoidal waveform can be synthesized more accurately with the additional neutral point DC voltage level. In other words, the harmonic component in the 3-level converter is reduced compared to the 2-level converter with the same switching frequency, leading to a much lower harmonic components in the AC side current. Alternatively, a lower switching frequency can be used in a 3-level converter to achieve the same harmonic component of a 2-level converter. In this thesis, the harmonic component is quantified by total harmonic distortion (THD).

THD is the percentage of distortion of a waveform when the output is compared to the input of a sinusoidal component. A lower THD means the waveform has lower harmonic components compared with the fundamental component, or in other word, the waveform is closer to an ideal sinusoidal waveform.

In addition, it should be noted that in each switching event, the IGBT only needs to switch half of the total DC link voltage. Since the switching loss is roughly proportional to the voltage that the device blocks at each switching cycle, the switching losses in a 3-level converter can be reduced by half in comparison to a 2-level converter, at the same switching frequency, which is displayed in Figure 6.

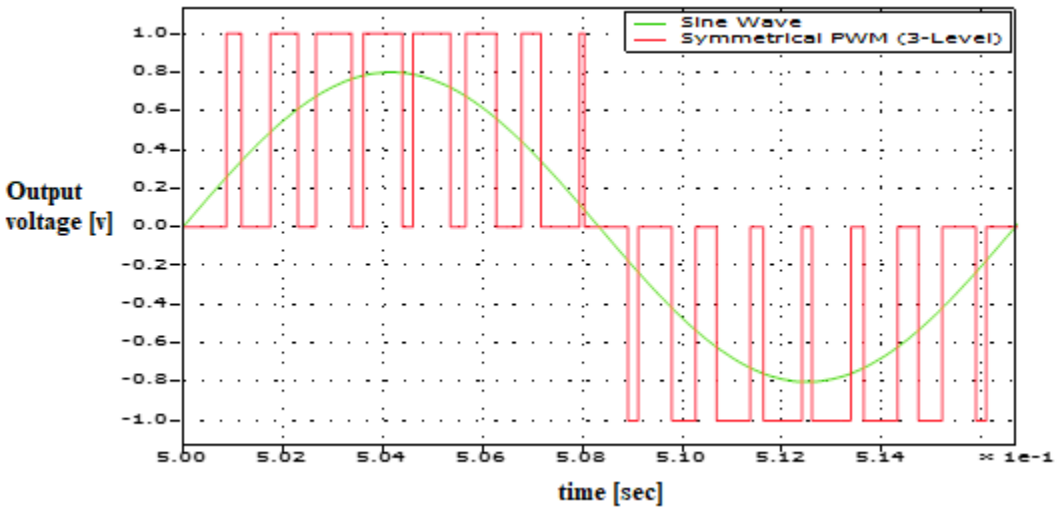

Figure 6. 3-level converter waveform. Source:[13]

E. MODULAR MULTILEVEL CONVERTER

The modular multilevel converter (MMC) is a mature topology which is very popular in high voltage DC (HVDC) application. Compared to the classic 2-level and 3-level converters, MMCs can generate theoretically unlimited voltage levels, i.e., hundreds of levels in HVDC application, which are used to synthesize the AC sinusoidal waveform accurately and without additional harmonic filters. On top of the extremely low harmonic level, the MMC also features low switching losses because each device only needs to be rated for a small fraction of the DC voltage.

The basic MMC topology is shown in Figure 7.

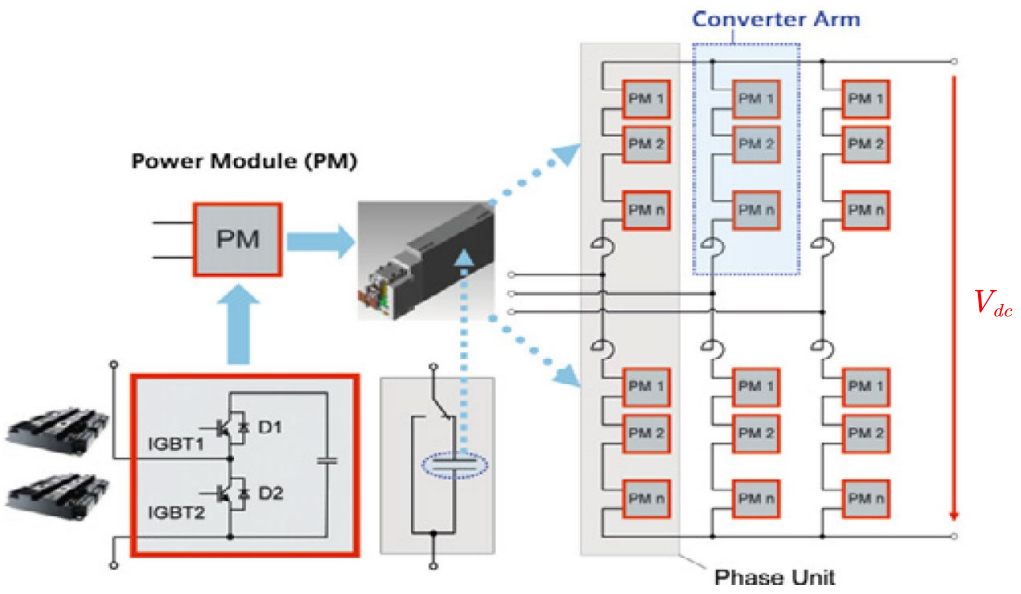

Figure 7. MMC power module configuration. Source: [14]

Each MMC phase leg includes two arms. Each arm consists of a few cascaded power modules and one arm inductor. Each power module has the same structure as a 2-level converter phase leg, including two IGBTs with anti-parallel diodes and one capacitor. By controlling the gates of the two IGBTs in one power module, the terminal output voltage of such power module can be either 0V or the voltage of the capacitor inside the module. Assuming the power module capacitor voltage is V_{cap} and there are N power modules in one arm, then by controlling all the gates of the power modules in the arm, the total voltage across such arm can be controlled to be any value between 0 and $N \cdot V_{cap}$.

One key benefit of MMC is that if one submodule fails in one arm, it can be bypassed and the system can continue operating at rated power if additional redundant modules are included.

Since there are two arms in each phase leg, the AC output voltage can be controlled if the top arm outputs the voltage difference between $+\frac{V_{dc}}{2}$ and the AC output voltage. The bottom arm outputs the voltage difference between the AC output voltage and $-\frac{V_{dc}}{2}$. The

total voltage of the two arms in one phase equals the DC side voltage as illustrated in Figure 8.

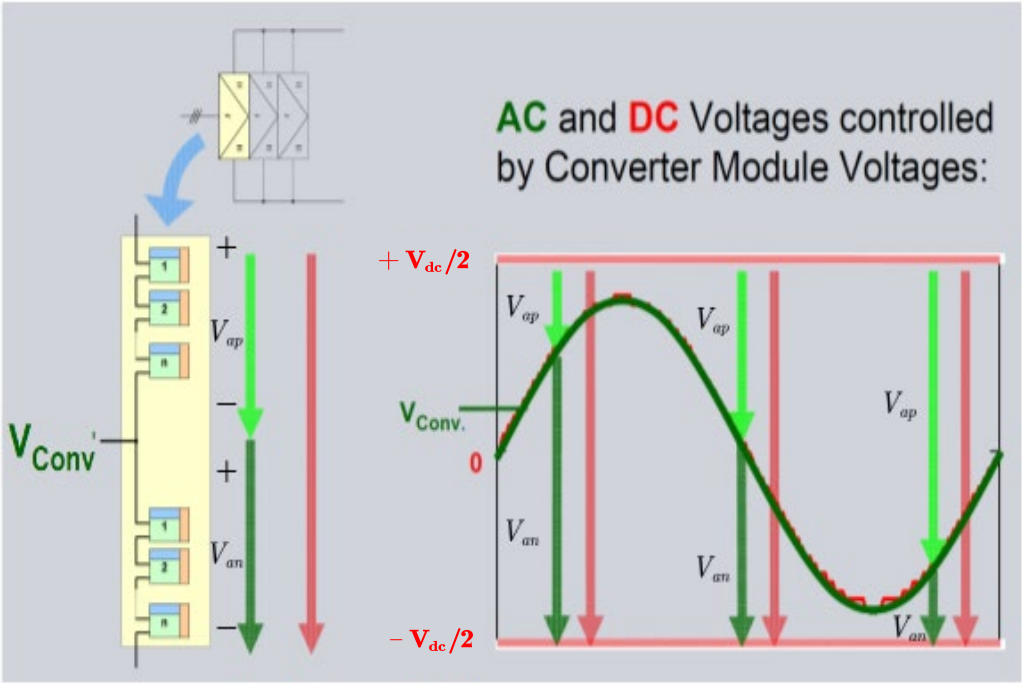

Figure 8. Converter arm voltage. Source: [14]

The relationship between the top arm voltage (V_{ap}), the bottom arm voltage (V_{an}), the DC bus voltage (+/-$\frac{V_{dc}}{2}$) and the AC side voltage V_{conv} can be summarized by the following:

$$V_{an} = V_{dc}/2 + V_{conv} \quad (1)$$

$$V_{ap} = V_{dc}/2 - V_{conv} \quad (2)$$

$$V_{an} + V_{ap} = 2 * V_{dc} \quad (3)$$

One key challenge related to MMCs is how to keep the capacitor average voltage constant, which means the net energy flowing into the capacitors inside each arm must be

zero during a fundamental cycle. To achieve this goal, the steady state current distribution is summarized in Figure 9 where the converter arms are represented as six controlled voltage sources. The AC side phase current in each phase is split evenly between the two arms and the DC side current is shared evenly among the three phase legs.

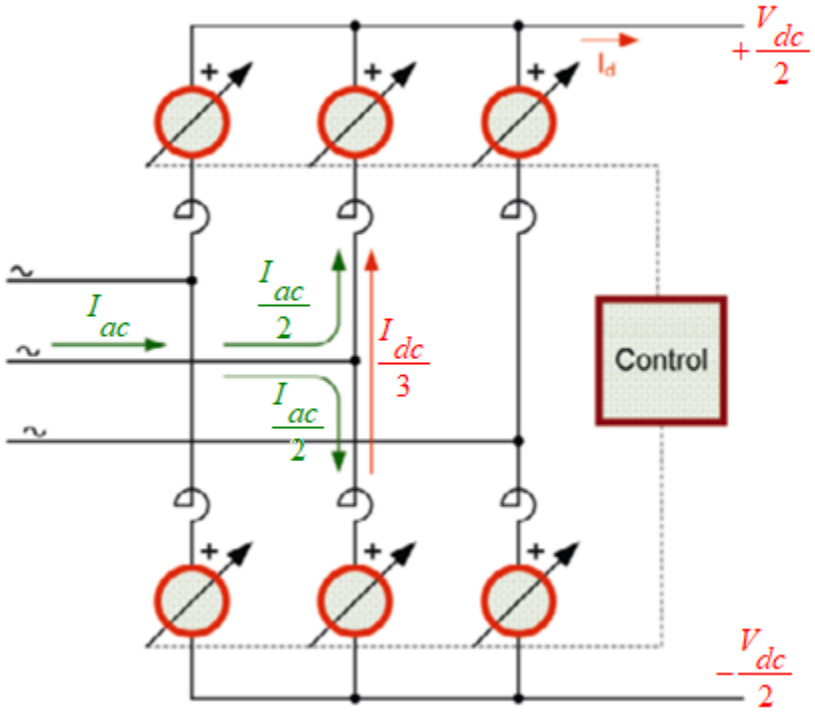

Figure 9. Arm current distribution. Source: [14]

With such current distribution, it can be proven that the net power of each arm is zero during a line cycle. However, each arm is in essence a single-phase system, which offers no way to eliminate 2nd order harmonics. So, the MMC requires a large capacitor for energy storage. Its internal storage requirement is determined by the AC fundamental frequency (60 Hz) and is approximately 40 kJ/MW for a 60 Hz system. [16]

F. MODULAR MULTILEVEL RECTIFIER

The MMR topology is depicted in Figure 10, and it consists of two components: 1) half bridge modules with Si IGBTS and Si diodes and 2) diode stacks. It should be noted

that, as in MMC, no harmonic filter or DC side capacitors are required and the failed module can be bypassed to keep the system operating at full power.

As seen in Figure 10, four diode stacks are added to each phase of the MMC topology, which consist of an upper arm and a lower arm. Each arm is built with series connected half bridge modules. Three phase midpoints are connected to construct a neutral point so that the arm voltage is no longer determined by only V_{ac} and V_{dc} as in the MMC. Instead, the midpoint voltage V_{mid} can be utilized to reshape the arm voltage, which makes it possible to reduce the maximum arm voltage. While a controlled switching device can turn off the current actively, the state of each diode is determined by the current polarity. Therefore, there are three possible working states for a single-phase MMR, as shown in Figure 11.

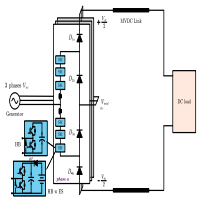

Figure 10. Topology of proposed modular multilevel rectifier. Source: [16]

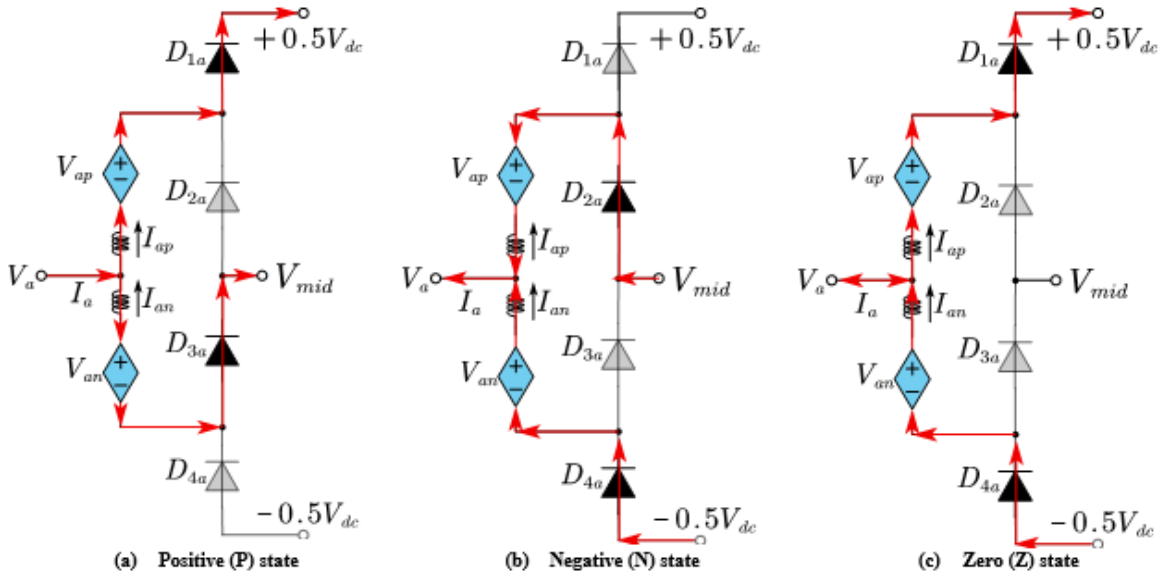

Figure 11. Basic states of a MMR phase leg. Source: [16]

As shown in Figure 11(a), when both the AC output voltage V_a and AC current I_a are positive, D_{1a} and D_{3a} are turned on and the phase leg is defined as being in a positive state. As shown in Figure 11(b), when both the AC output voltage V_a and AC current I_a are negative, both D_{2a} and D_{4a} are turned on and the phase leg is defined as being in a negative state. As shown in Figure 11(c), when the polarity of the AC output voltage and the AC output current are not determined, such as when the AC output voltage V_a or AC output current I_a cross zero, the diodes D_{1a} and D_{4a} turn on and the phase leg is defined as being in zero state. The switching between different states is controlled via the output voltages of the different arms. The states of the three phase legs over one line cycle is illustrated in Figure 12.

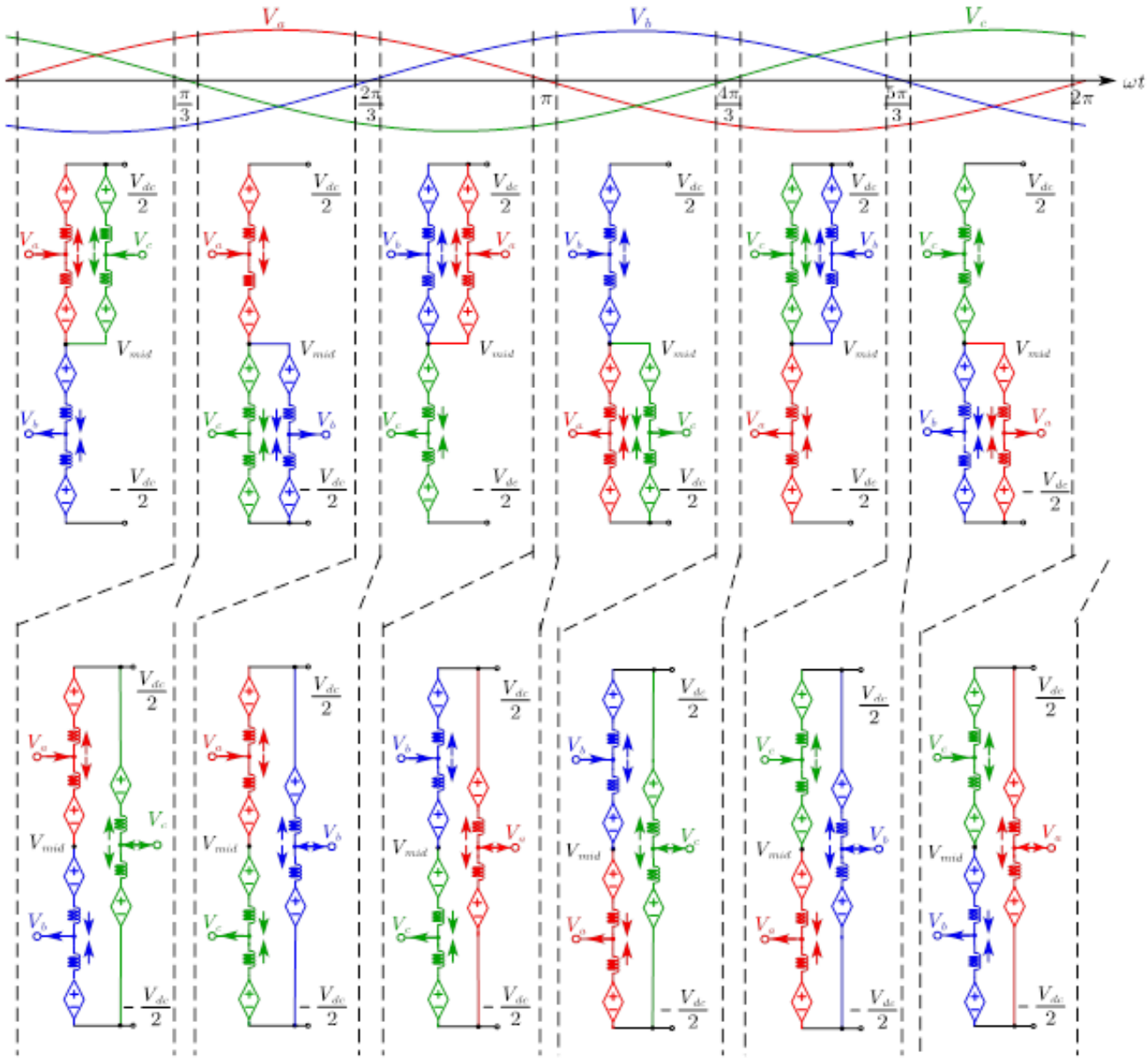

Figure 12. States of 3 phases in MMR over one line cycle. Source: [16]

From Figure 12, it can be found that, not like in an MMC, where all three phases are connected in parallel across the DC bus, at least two phases, in an MMR are connected in series between the DC bus. In other words, four arms are connected in series to block the DC bus voltage instead of two arms as in an MMC. So, the voltage rating or the total number of submodules of each arm in an MMR is only half as in an MMC. For example,

in a 12kV (+/-6kV) DC system, if the DC capacitor voltage of each submodule is 1kV, a MMC will require 12 submodules per arm or 72 submodules in total without additional redundancies. But for an MMR, only 6 submodules are required per arm or 36 submodules in total. Since the output AC voltage is synthesized by the submodules, both MMC and MMR can generate the same AC side voltage with 13 voltage levels (1kV per level between +/-6kV). With such high number of voltage levels, the harmonics current flowing on the AC side can be negligible without any filters and the electromagnetic interference (EMI) issues can be significantly mitigated due to much lower dv/dt in the MVDC system compared with the traditional 2-level and 3-level converters mentioned above. Please note that, even lower submodule voltages can be used to further improve the system harmonic performance with the penalty of higher system complexity since more submodules are needed. Compared to the MMC topology, the number of power modules is reduced by half, so the energy storage requirement is also reduced by half.

III. MODELING AND CONTROL

This chapter presents the system parameters, device thermal model, and performance evaluation criteria which is applied to the four active front end rectifier topologies.

A. SYSTEM PARAMETERS

In modeling a shipboard system for this comparison study, the parameters chosen for base calculations are as follows:

1. The total apparent power of the system is 35 MVA.
2. The three-phase AC line-to-line voltage at the generator output V_{ac} is 6.6 kV rms.
3. The DC output voltage of the rectifier V_{dc} is 12 kV.
4. The fundamental frequency is 60 Hz.

The AC rms phase voltage is

$$V_{ac\_rms} = \frac{V_{ac}}{\sqrt{3}} = 3810.51v \tag{4}$$

and the rms AC current is

$$I_{ac\_rms} = \frac{\frac{35MVA}{3}}{V_{ac\_rms}} \approx 3kA \tag{5}$$

Finally, the system base impedance is

$$Z_b = \frac{V_{ac\_rms}}{I_{ac\_rms}} = 1.2446\Omega \tag{6}$$

Assuming the generator equivalent impedance is 0.3 pu, which is an estimated value for the generators in Naval shipboard operations, the synchronous inductance of the machine can be calculated as

$$L_{gen} = \frac{0.3 * Z_b}{(2\pi * 60)} = 1mH \tag{7}$$

B. ACTIVE RECTIFIER CONTROL

The system topology of a generic active rectifier is shown in Figure 13. The input AC voltage source is modeled as an ideal voltage source in series with resistors and inductors, modeling its resistance and inductance per phase. The DC output has a DC capacitor.

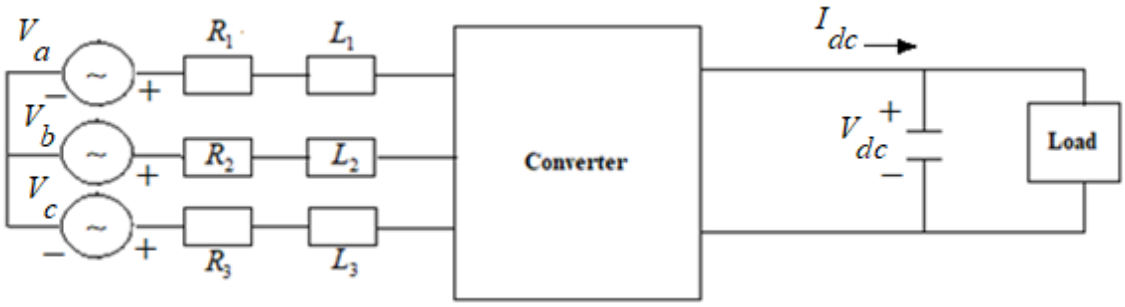

Figure 13. Rectifier control circuit

The goal of the rectifier control system is to regulate the output voltage V_{dc} to a constant value. The DC link voltage must be constant or vary within a specified limited range to meet the standard, no matter what the load requirement is. To achieve this target, the current I_{dc} is regulated to control V_{dc}. To achieve these control functions, a voltage control loop must be implemented, as shown in Figure 14.

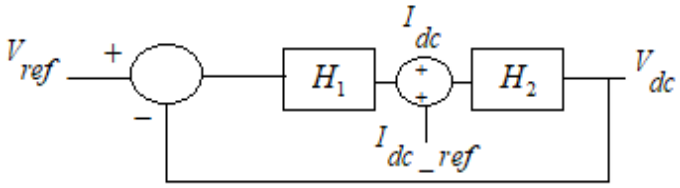

Figure 14. Voltage control system block diagram

In Figure 14, H_2 is describing the transfer function of the physical system on the DC side and H_1 represents the control system transfer function.

The relationship between the DC side current, DC side voltage and DC capacitor in frequency domain can be represented as

$$V_{dc} = \frac{I_{dc}}{sC} \tag{8}$$

where s is the Laplace variable used as derivative operator in this capacitor voltage equation. Then

$$H_2 = \frac{V_{dc}}{I_{dc}} = \frac{1}{sC} \tag{9}$$

H_1 is the transfer function of the control system and this design uses a proportional – integral (PI) controller for the control system in the rectifier. The PI control transfer function is represented by H_1, where K_{p_v} is the proportional gain and K_{i_v} is the integral control gain

$$H_1 = K_{p\_v} + \frac{K_{i\_v}}{s} \tag{10}$$

To control the system response as a first order control system (the input-output relationship is a first order differential equation) with bandwidth ω, the overall DC side open loop transfer function (T), which is calculated as the control system gain multiplied by the physical system gain, is represented by

$$T = H_1 * H_2 = \frac{\omega}{s} = (K_{p\_v} + \frac{K_{i\_v}}{s}) * (\frac{1}{sC}) \tag{11}$$

where K_{p_v} and K_{i_v} are the proportional and integral gains for the voltage control loop.

$$K_{p\_v} = \omega C \text{ and } K_{i\_v} = 0 \tag{12}$$

The control gains in equation (12) can achieve the closed loop voltage control required to keep the DC voltage constant.

Since the converters cannot generate or absorb energy, to control i_{dc}, the AC side active power needs to be controlled to match the active power delivered to the DC side, as shown in the following power equation:

$$P = I_{dc}V_{dc} = \frac{3}{2}I_d V_d \tag{13}$$

where i_d and v_d are variables on the direct axis (d-axis) of the quadrature-direct-zero (*qd0*) synchronous reference frame. This reference frame is used to rotate the reference of the AC sinusoidal voltage and current waveforms so that they are stationary and can be represented as DC signals. The *abc* to *qd0* transformation simplifies the control system used for the rectifiers analyzed in this thesis. The d-axis reference current on the AC side can be derived and utilized to control the rectifier voltage and current. Figure 15 shows how the three-phase voltage and current are represented as DC signals on the d-axis of the *qd0* reference frame.

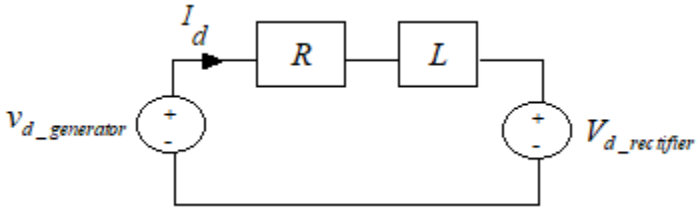

Figure 15. Rectifier AC side equivalent circuit on the d-axis

In Figure 15 the input voltage $V_{d\_generator}$ represents the d-axis component of the gas turbine generator voltage transformed from *abc* to *qd0*, and $V_{d\_rectifier}$ is the d-axis rectifier voltage on *qd0* reference frame.

The control system for the AC side current is shown in Figure 16, where H_4 represents the transfer function of the physical system on the d-axis of the *qd0* reference frame and H_3 represents the transfer function of the control system. $V_{d\_generator}$ is used as the feedforward term to achieve a faster dynamic response.

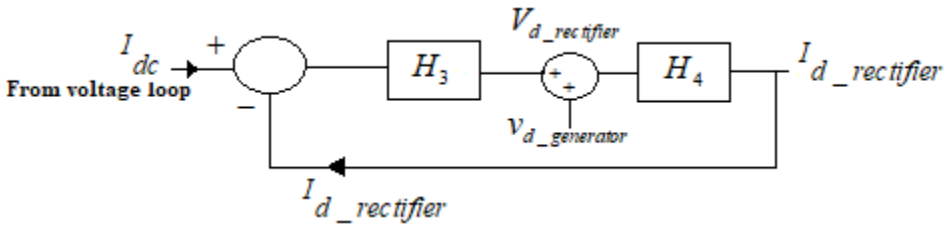

Figure 16. Current control system block diagram

To control rectifier current, $I_{d\_rectifier}$, the following equations are used to derive the values for the proportional and integral gains for the current control loop K_{p_i}, K_{i_i}.

The AC side system can be modeled in time domain in Eq. (14) or in frequency domain in Eq. (15) to (17).

$$V_{d\_rectifier} = L\frac{dI_{d\_rectifier}}{dt} + I_{d\_rectifier}R + V_{d\_generator} \tag{14}$$

$$V_{d\_rectifier} - V_{d\_generator} = LsI_{d\_rectifier} + I_{d\_rectifier}R \tag{15}$$

$$V_{d\_rectifier} - V_{d\_generator} = (Ls + R)I_{d\_rectifier} \tag{16}$$

$$\frac{V_{d\_rectifier} - V_{d\_generator}}{Ls + R} = I_{d\_rectifier} \tag{17}$$

The voltage $V_{d\_generator}$ is constant DC, therefore it has no effect on the transfer function H_4 and Eq (17) can be rewritten as

$$V_{d\_rectifier} = Lsi_{d\_rectifier} + I_{d\_rectifier}R \tag{18}$$

The transfer function of the physical system in the current loop, H_4 is

$$H_4 = \frac{1}{Ls + R}. \tag{19}$$

Similar to the voltage control loop, the overall AC side current open loop transfer function (T_2), the system response is also controlled as a first order control system with bandwidth ω_i.

$$T_2 = H_3 * H_4 = \frac{K_{p\_i}s + K_{i\_i}}{s} * \frac{1}{Ls + R} = \frac{\omega_i}{s} \tag{20}$$

$$K_{p\_i}s + K_{i\_i} = \omega_i(Ls + R) \tag{21}$$

$$K_{p\_i}s + K_{i\_i} = Ls\omega_i + R\omega_i \tag{22}$$

So,

$$K_{p\_i} = Ls\omega_i \tag{23}$$

$$K_{i\_i} = R\omega_i \tag{24}$$

When $V_{d\_generator}$ is added to the $V_{d\_rectifier}$, a feed forward system is created. $V_{d\_generator}$ is a value that is set to be close to the value that we know $V_{d\_rectifier}$ needs to be. As the control system begins making corrections to the signal, having a baseline close to the desired result makes finding the correct answer happen much more quickly. This allows the controller to reach steady state much faster. $V_{d\_generator}$ is a voltage signal that is close to the typical value of the control target. Knowing this allows the system to speed up the process of current correction to control the converter more quickly.

Following the design rule to decouple the voltage control loop from the current control loop, the control bandwidth is picked so that $\omega_i >> \omega_v$ and the measured current can follow the current command very quickly. In other words, when controlling the AC side current, the DC side voltage can be assumed to be constant, so in the simulation model the DC side is modeled as a constant DC voltage source. This can significantly simplify the control system design and speed up the simulation time.

The control system presented in this section is the basic control which is used for all rectifiers analyzed in this study. As the complexity of the converter topology increases with additional levels, there is a need for additional control circuitry specific to each converter design, which is briefly covered in Ch. 4.

C. DEVICE THERMAL MODEL

In this study, we used the piecewise linear electric circuit simulation (PLECS) software to evaluate the performance of each topology. PLECS is a software program that allows for system level analysis of power electronics. PLECS provides the ability to build the converter topologies, then easily analyze their performance. The software has pre-made features that facilitate efficient evaluation of power electronic circuit operation.

The heat sink tool in PLECS was utilized to calculate the losses in the semiconductor devices during the steady state operation of each rectifier topology. Data can be taken directly from the semiconductor data sheet and uploaded into the PLECS thermal library as characteristics that were feed into the heat sink tool. Thermal models were developed for the 2-level and 3-level converter from the data sheet of the TOSHIBA SILICON N-CHANNEL IEGT ST2100GXH22A [17] and their anti-parallel diodes (Infineon D2700) [18], which are rated 4.5kV 2100A. In the thermal imaging wizard of the PLECS software, the diode conduction losses are included. This concept is shown in the conduction loss graph for the two semiconductor devices used in the topology simulations. Turn-on losses, turn-off losses, and conduction losses were imported into the PLECS thermal imaging library and assigned to the switching devices in the converter circuit in the PLECS simulation. Figure 17 and Figure 18 capture the thermal inputs for the switching devices and respective diodes. As the PLECS software simulates the thermal models, the

semiconductor losses are calculated and scaled up for the number of devices used in the system. This is explained in further detail in the simulation results section of this study.

Figure 17 shows the final switching loss profile for the semiconductor switching device after the data has been uploaded into the thermal library. Figure 18 shows the conduction loss profile for the semiconductor device and anti-parallel diodes. The conduction power losses are calculated as the current multiplied by the voltage. All devices used in this study had thermal profiles built into the simulation software.

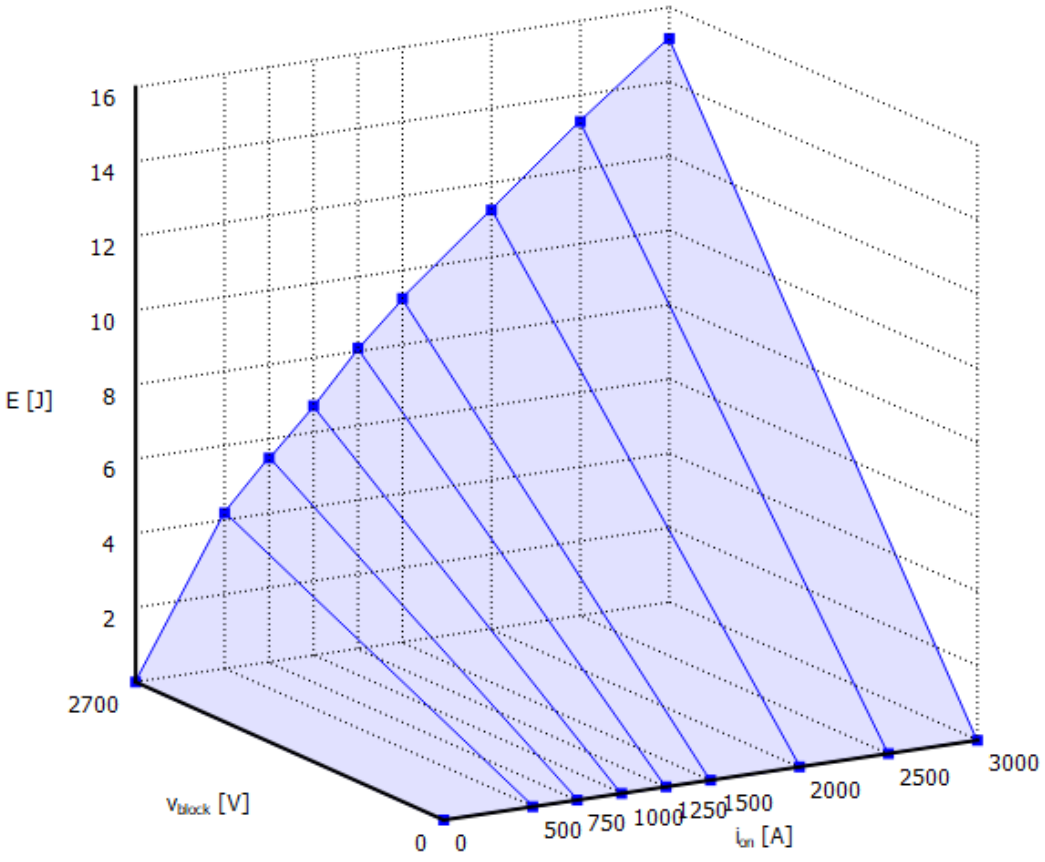

Figure 17. Switching loss thermal model for the Toshiba semiconductor

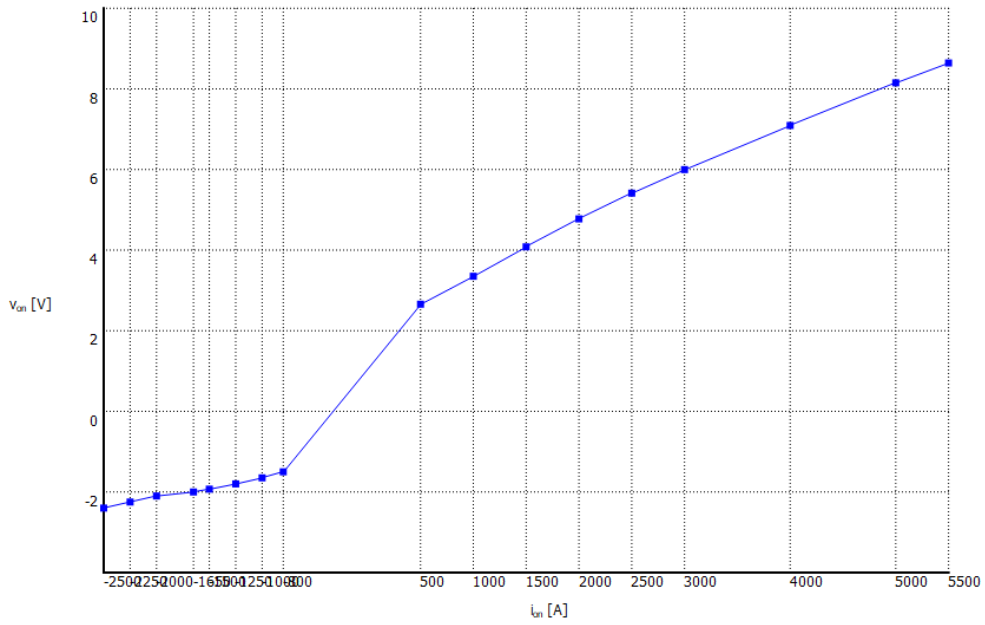

Figure 18. Conduction loss thermal model characteristics for Toshiba device

For the MMC and MMR topologies, the voltage that the switches need to block is 1kV, which is considerably lower than the 2 and 3-level converters, where the switches must block 4.5kV. Therefore, a different semiconductor was chosen; an Infineon dual IGBT module which has a large power density and more efficient power and thermal cycling capability than the devices used for the 2- and 3-level topologies [19]. The semiconductor device chosen for the MMC and MMR topologies was the Infineon FF1200R17KP4_B2. This device can block up to 1700V and has a current handling capability of 1200 A. Due to the limited current handling capability of the device, when the IEGT is used in 2 and 3-level converter circuits, two paralleled devices must be used so that the total current rating is doubled. Using the device datasheet [20], conduction loss and switching loss graphs were loaded into the thermal wizard as was done for the Toshiba device and diode for the 2-level and 3-level converter model.

For the switching devices in the MMC and MMR topologies, current values from the data sheet are doubled to simulate the case with two devices in parallel.

For the MMR topology design, a diode thermal model had to be defined for the diode stack which is rated at half of the DC bus voltage. For this, the same diode used in

the 2-level converter was used. Since these diodes switch at the fundamental frequency, when the current flowing through them is close to zero, the diode stack switching losses are ignored. Only the conduction losses are included in the thermal property for the diodes used in the diode stack.

D. KEY METRICS FOR COMPARISON

All four rectifier topologies were compared based on three performance metrics: the efficiency or power losses, the AC current harmonics, and the total energy storage requirements. The efficiency is obtained based on the simulated converter losses at rated power operating conditions (35MVA). The total energy storage was calculated based on the total energy stored in the capacitors. The harmonic performance is evaluated based on the THD of the AC side current.

Total harmonic distortion is a measurement of how much the voltage or current is distorted due to harmonics in the system in integer multiples of the fundamental frequency. It is defined as the ratio of the equivalent root mean square (RMS) voltage of all the harmonic frequencies (from the 2nd harmonic on) over the RMS voltage of the fundamental frequency. While the voltage at the fundamental frequency is the desired output voltage, its multiples cause unwanted distortion in the waveform. In (25) the squared harmonic voltages are added together, and the square root is taken. The result is then divided by the voltage at the fundamental and the THD given is a percentage of the output signal representing percent distortion of the voltage waveform.

$$THD = 100 \cdot \frac{\sqrt{\sum_{n=2}^{\infty} (V_{n\_rms})^2}}{V_{rms\_fundamental}} \tag{25}$$

Power electronics systems must be designed to produce voltages and currents with THD as low as possible because higher THD negatively impact system performance by reducing the power factor and overall efficiency.

The PLECS software includes a tool to calculate the THD which accounts for all harmonics and provides a realistic representation of power quality in the system.

IV. SIMULATION RESULTS

The models of the four active rectifier topologies are built using the PLECS software with the goal to compare their performance and the simulation results are presented in this chapter. It should be noted that, since one important metric to compare the four topologies is the efficiency, and the power electronic device conduction losses and switching losses are dependent on the device junction temperature, a dedicated thermal management system design is required for each converter system in the real application. So the device junction temperatures are set high enough to fully leverage the device power capability, but with sufficient margin from the maximum junction temperature for safety and reliability. However, since this thesis compares the four topologies at a high level, the ambient temperature is set to 125 degrees Celsius and very low thermal impedance between the device and ambient are used in all simulations. In other words, all thermal loss data is calculated with the assumption that the device junction temperature is 125 degrees Celsius for all four rectifiers.

A. TWO-LEVEL CONVERTER

The 2-level converter design consists of 3 legs (one leg per phase), with 12 semiconductor switching devices per leg. The devices chosen for this study are Toshiba IGBT rated 4.5 kV and 2.1 kA. Since each device in the 2-level converter must be able to handle $+\frac{V_{dc}}{2}$ to $-\frac{V_{dc}}{2}$, or 12 kV with additional transient overvoltage during switching and additional margin is necessary to cover the unbalanced voltage distribution among series connected devices, 6 IGBTs in series are designed per each device position with 26kV voltage blocking capability. Figure 19 shows a standard 2-level configuration with two devices per phase. Once the thermal characteristics are captured during simulation, results are then multiplied by the number of devices used in the system to achieve the 12 kV DC bus.

The switching frequency in the 2-level converter is 2kHz to achieve a good balance between power losses and harmonic performance. The current control bandwidth is set to

10% of the switching frequency. Figure 19 shows the circuit configuration as designed in PLECS.

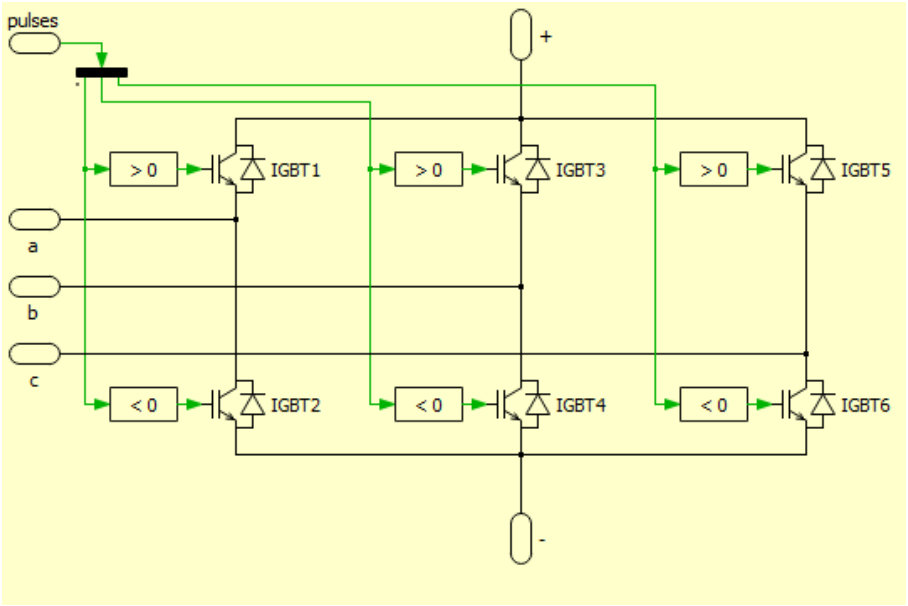

Figure 19. 2-level rectifier as modeled in PLECS

Figure 20 is the overall PLECS model of the 2-level topology. The 2-level converter shown in Figure 19 is placed into the block of Figure 20 labeled "2-level IGBT Conv." The 6.6 kV AC generator is modeled for this, as well as the other topologies, using three ideal sinusoidal voltage sources *Va*, *Vb*, and *Vc*, each in series with an inductor and a resistor. The regulated DC bus is represented as a DC source because the DC bus voltage is regulated to remain constant, and the DC current is controlled though the converter. The AC current is controlled in the *qd0* reference frame with the PI controllers pictured at the lower portion of Figure 20. From the current control in the *qd0* reference frame, the current signal is then transferred back into the *abc* frame and sent into the PWM block. The PWM signal then controls the switching of the IGBTs in the converter block to control the current drawn from the generator, which we analyze to evaluate the power quality at the input of the rectifier.

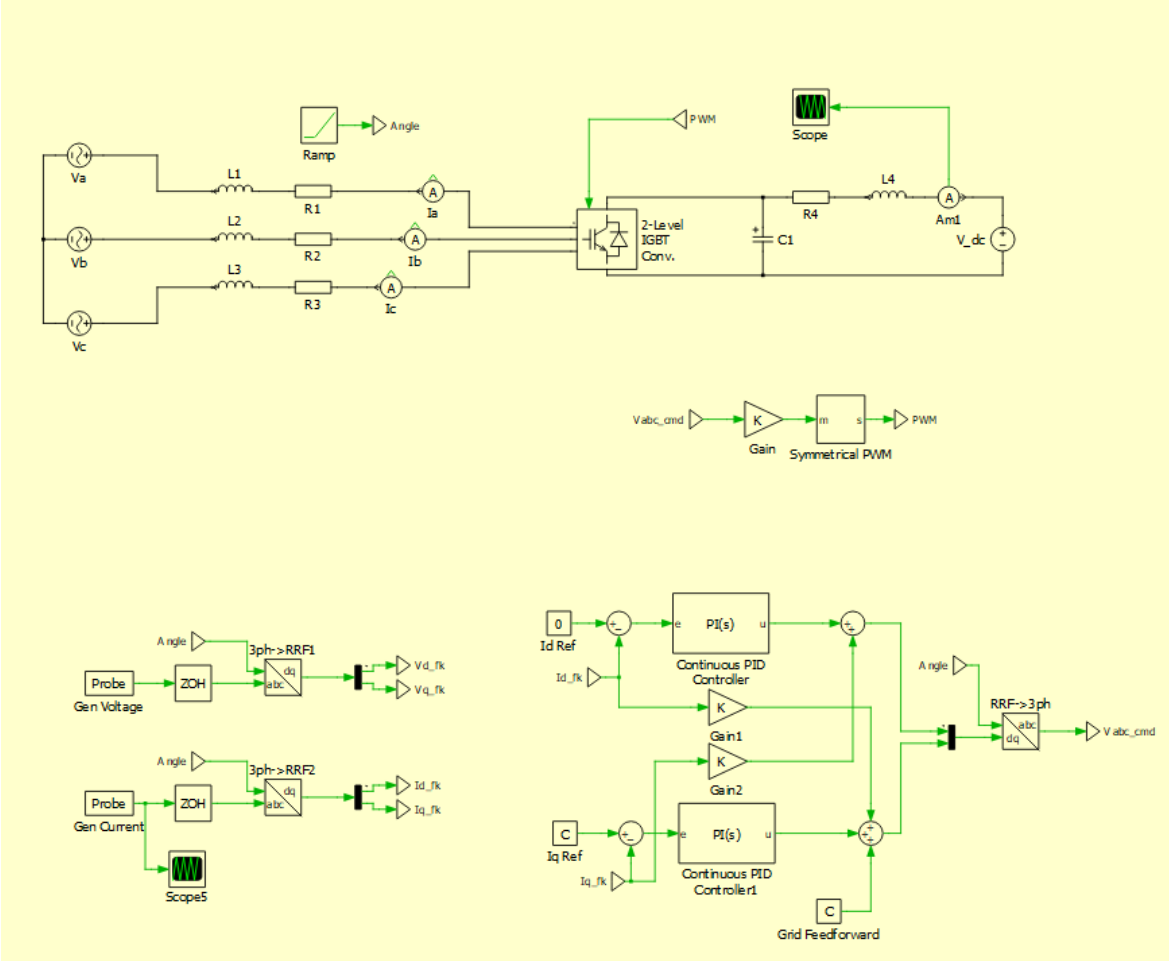

Figure 20. 2-level converter PLECS system configuration

The DC capacitance for the 2-level topology is sized to store the energy which equals to the product between the converter peak power and half of a fundamental cycle. The following equations are used to find the energy storage requirement and the corresponding capacitance.

$$Energy = \frac{35MW}{120Hz} = 292kJ \tag{26}$$

$$Energy = \frac{1}{2}CV^2 \tag{27}$$

$$C = \frac{2 * Energy}{V^2} = \frac{2 * 292kJ}{(12kv)^2} = 4mF \tag{28}$$

A “heat sink” tool from the PLECS library is used to compute the switching and conduction losses of IGBT1, as shown in Figure 21 As noted in section III.C, a 4.5 kV IGBT is used in the model of the 2-level converter. The conduction losses computed for one IGBT are multiplied by 36, which is the total number of switching devices and diodes in this rectifier topology. The switching losses must only be multiplied by 6 because the simulation software will scale up the switching loss for all devices connected in series automatically.

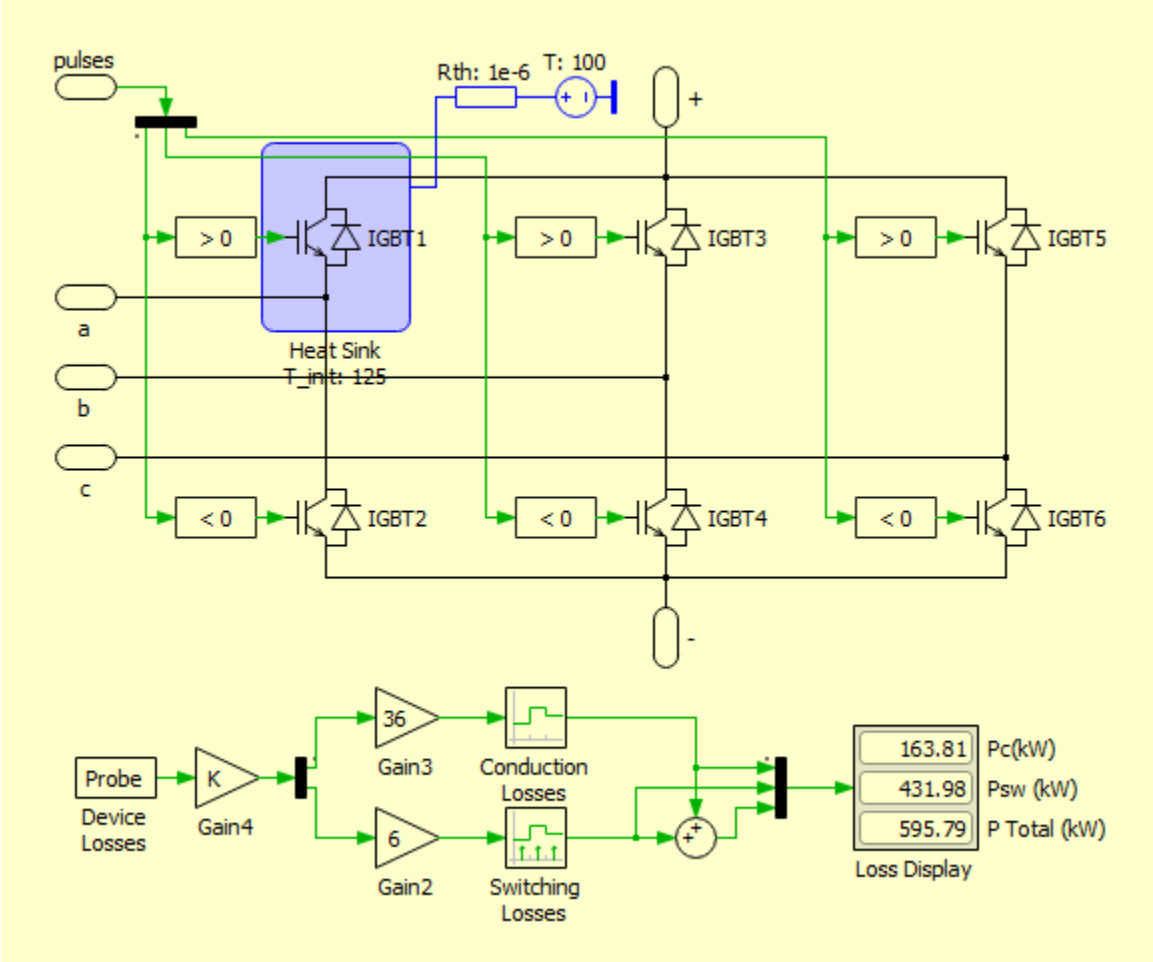

Figure 21. 2-level converter thermal modeling circuit configuration

The harmonic content of the source currents is the other parameter computed for comparison with the other rectifier topologies. From the time-domain current waveforms,

the Fourier analysis is performed to plot the current harmonics in the frequency-domain. The three-phase currents plotted in Figure 22 show significant distortion due to the harmonics of the switching frequency at 2kHz.

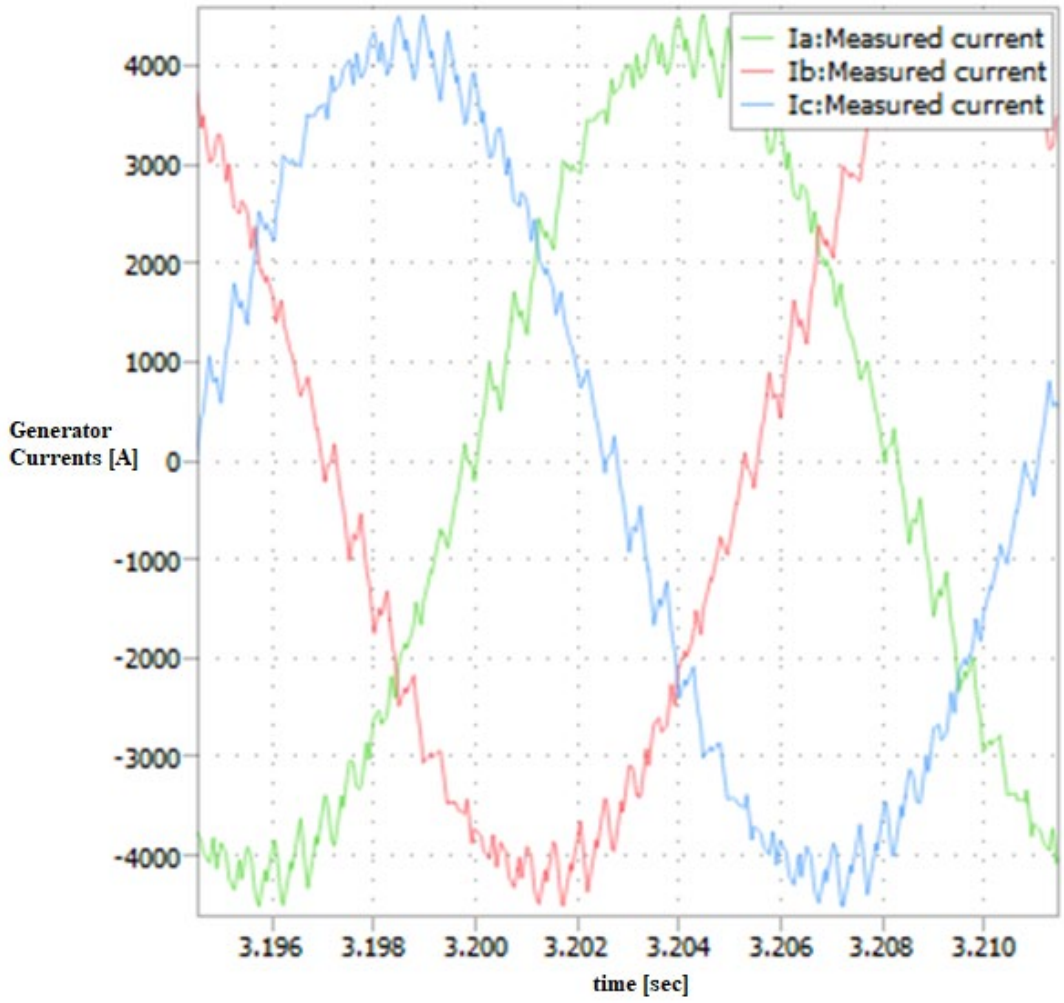

Figure 22. 2-level rectifier three-phase input currents

The low power quality displayed by the source currents in Figure 22 is expected from the 2-level converter switching at 2 kHz. Figure 3 is the conduction loss, switching loss, and total power loss displayed from simulation results. Figure 23 shows simulated power losses for 2-level rectifier operation.

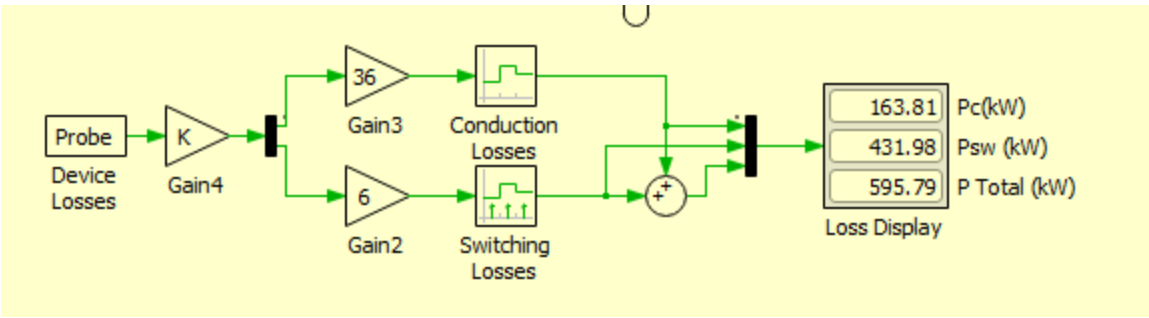

Figure 23. 2-level converter total switching and conduction losses

For this 2-level converter the sum of conduction and switching losses is just over 595 kW. For the 35 MW system that is being modeled, this shows that losses are roughly 1.7 % of the total power rating. Although this topology offers the advantages of a simple design, control, and implementation compared to multilevel topologies, it features significant power losses during steady state operation.

In this 2-level rectifier simulation, the THD is approximately 5.6 % for each of the three-phase currents drawn from the generator.

Figure 24 shows the source current frequency-domain plot obtained with the Fourier analysis. The distortion is in the signal is due only to the 2 kHz switching frequency and only two voltage levels for switching operations.

The harmonics observed that are significant contributors to the source currents THD are the side bands around the switching frequency (2 kHz) and two times the switching frequency. The first harmonic in Figure 24 is the fundamental frequency (60 Hz) with some smaller harmonics observed at 5 times the fundamental frequency (300Hz). While Figure 24 shows the Fourier spectrum up to 4.8k Hz, Figure 25 zooms on the fundamental frequency harmonics, showing the 5^{th} harmonic at 300Hz and the 7^{th} harmonic at 420Hz for the three-phase currents.

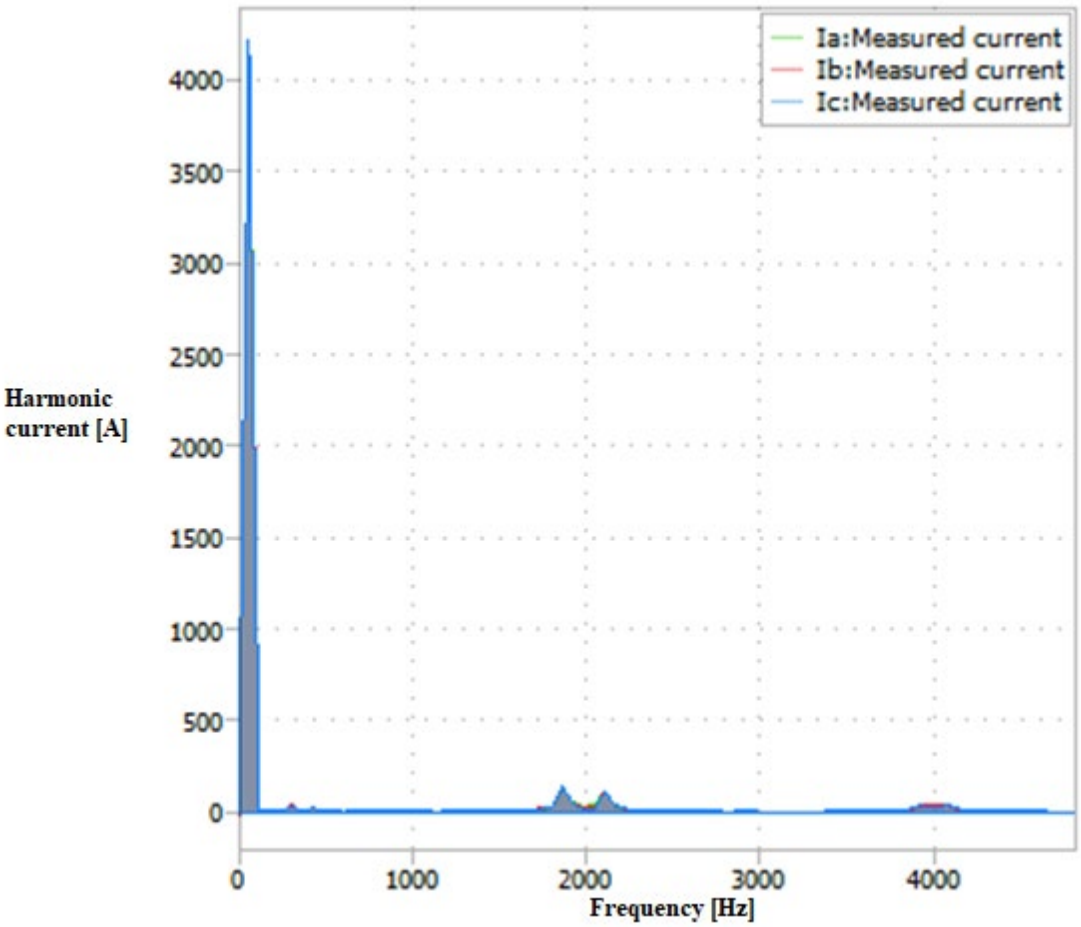

Figure 24. 2 level generator current Fourier analysis

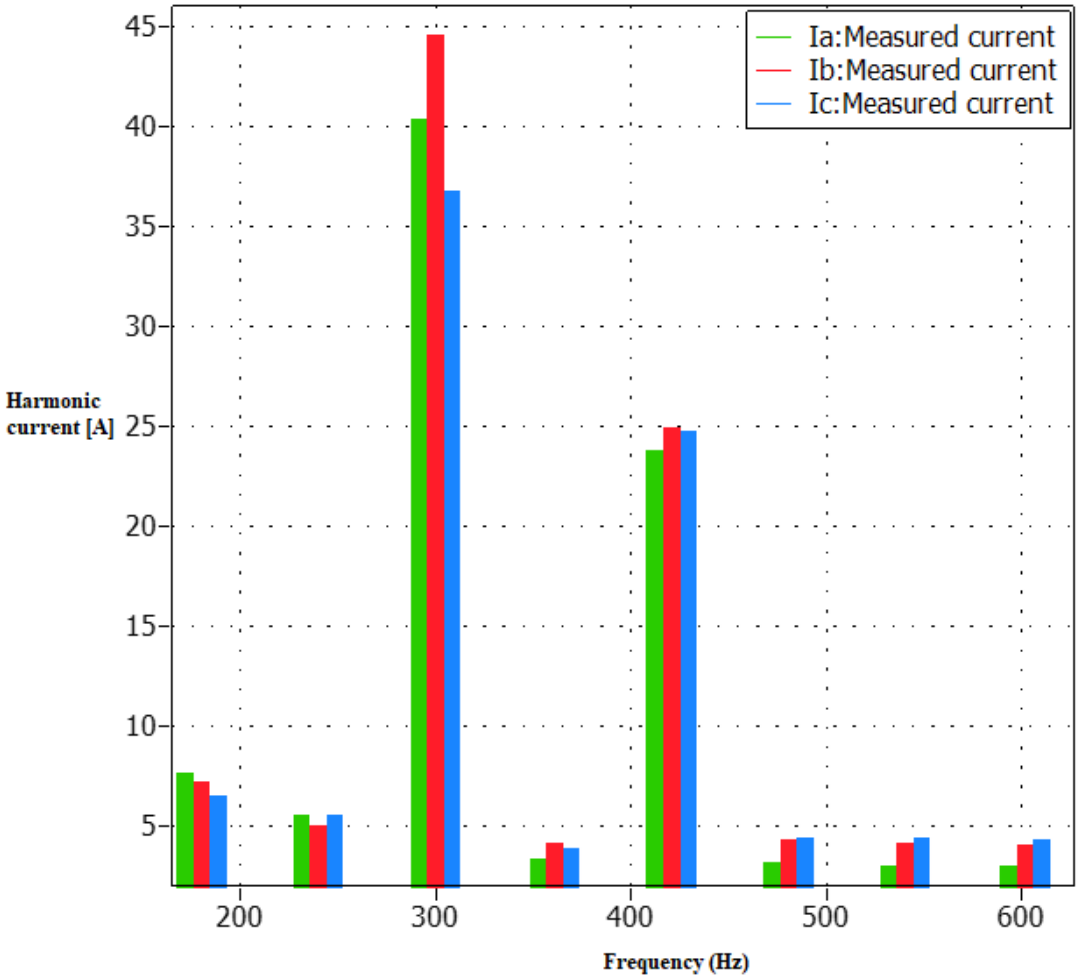

Figure 25. Harmonic feedback for 2-level converter at multiples of fundamental frequency.

The simulation results presented for the 2-level rectifier indicate that this topology is limited by power losses at high switching frequencies. This simulation is set at a 2 kHz switching frequency to be consistent with the other topologies monitored. At a higher switching frequency, the current distortion would be less, but switching losses would go up tremendously. Electromagnetic interference issues could be a potential problem and the need for more efficient harmonic filtering becomes apparent from the Fourier analysis presented. In addition to the added cost, weight, and size that the additional filter would cause, the need for high voltage capacitors makes this topology less attractive than multilevel rectifiers. Performance of the 2-level converter is not ideal for naval shipboard

applications because of the voltage level that is necessary for power distribution. The 2-level converter works well for low voltage applications but is not suitable for high voltage. The Fourier analysis showing harmonic current at multiples of the switching frequency.

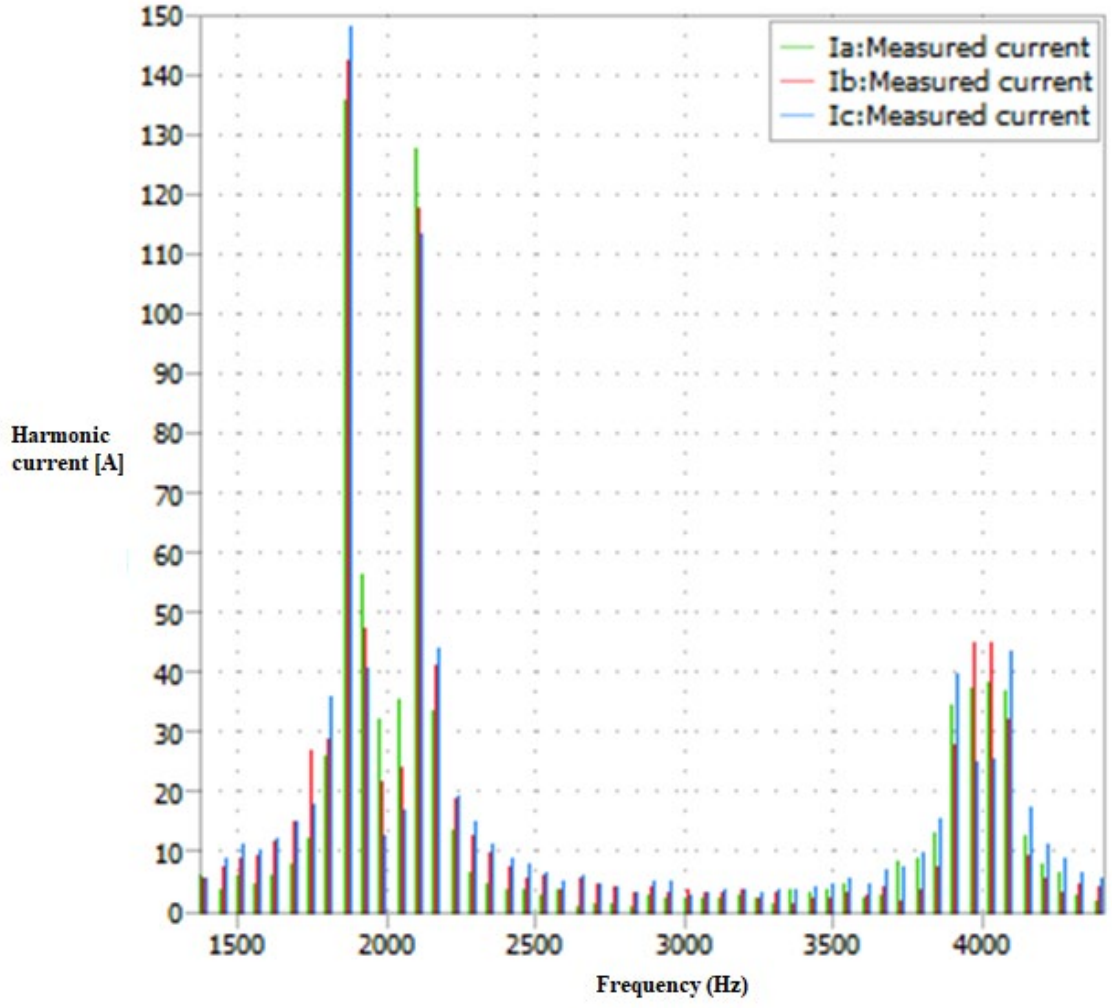

Figure 26. Fourier analysis for 2-level converter at multiples of switching frequency.

B. THREE-LEVEL T CONVERTER

The 3-level converter operates on the same basic concept of the 2-level converter except for the addition of the neutral point leg and 2 capacitors across the DC link bus. Energy storage requirements of the 3-level are the same as the 2-level topology. For the 3-

level, capacitance of each capacitor is doubled, but the voltage required for each capacitor is half, so the total energy in the capacitor is the same as in the 2-level converter. The IGBT design in the vertical legs remains the same as the 2-level design, with 36 total devices. For the neutral leg, 3 devices are used per simulated switch so that 18 total switching devices are used across the neutral leg. This is accounted for in the thermal loss calculation graph shown in Figure 30.

The switching frequency in the 3-level converter is set to 2 kHz to achieve a good balance between power losses and harmonic performance. Signal quality would be improved with a higher switching frequency, but 2 kHz is chosen in an effort to minimize switching losses.

Figure 27 is the PLECS model created for the 3-level T type converter. For each phase, the two IGBTs remain the same as the 2-level converter design, but there is an addition of two IGBTs in the neutral, or 3rd level.

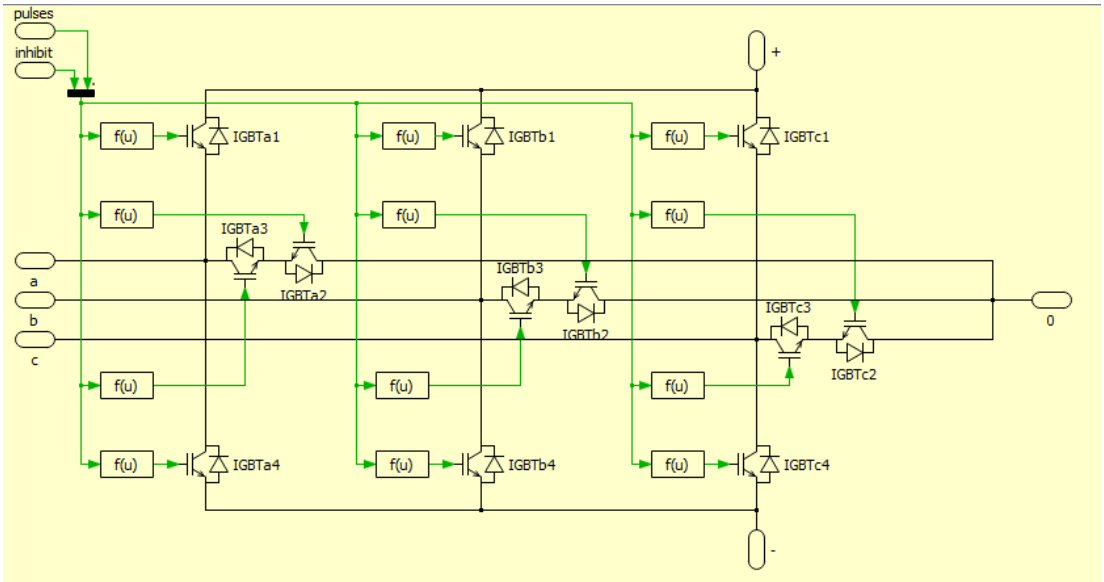

Figure 27. 3-level T type converter PLECS topology

Figure 28 shows the 3-level converter system configuration in which the 3-level rectifier shown in Figure 27 is placed between the AC source and the DC bus. The PI

controllers, PWM, capacitor voltage, generator current, and generator voltage circuits can be observed. The generator current from this display is evaluated to determine the power quality of this topology.

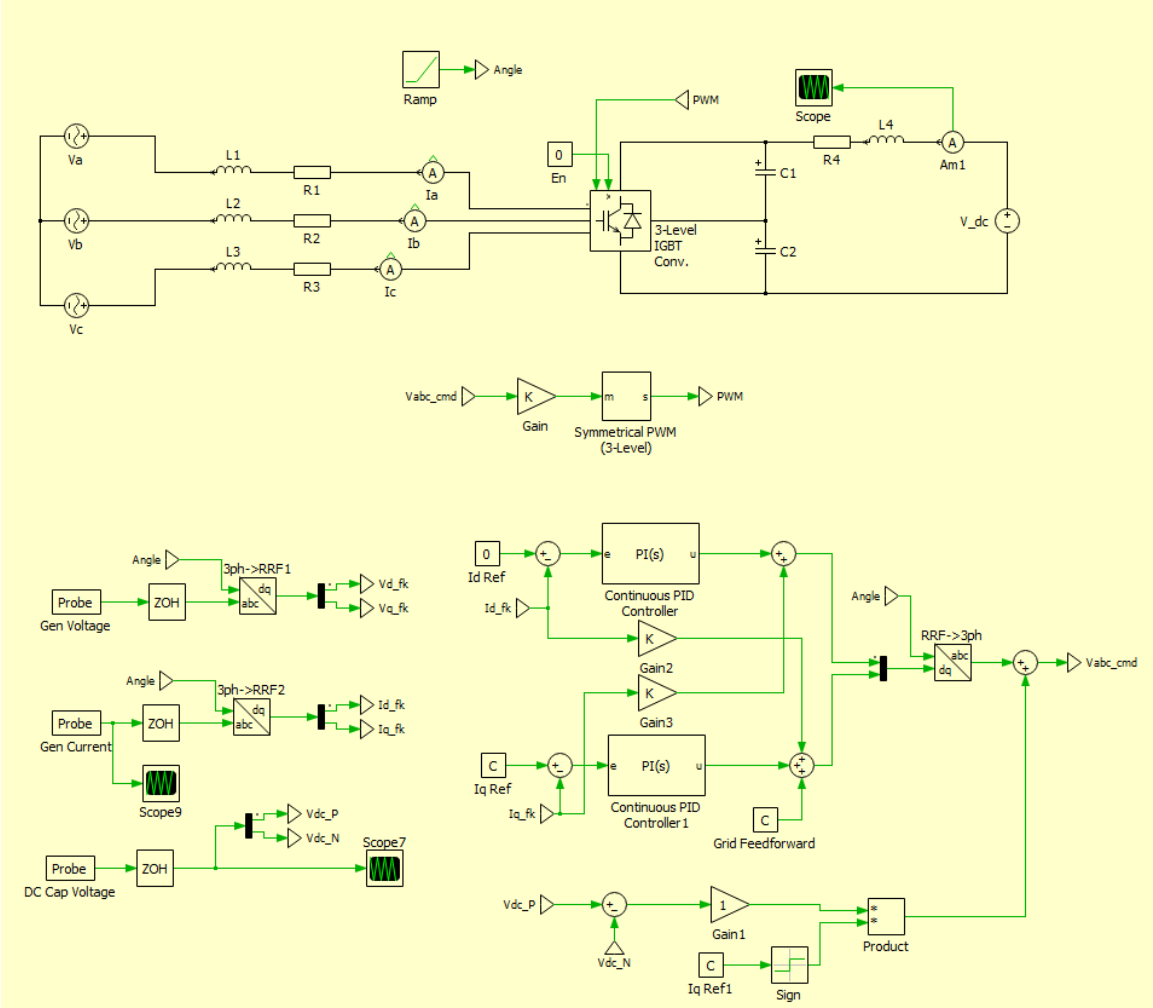

Figure 28. 3- level T type converter PLECS system configuration

In the 3-level T type converter, it is necessary to maintain the neutral point voltage. If the two capacitors are responsible for 6 kV each in the desired 12 kV DC bus voltage, the capacitors would have to be discharged at different rates to maintain balance. For this reason, an additional control circuit is implemented to control V_{DC} and ensure the capacitors are adequately balanced for stable operation.

The power losses computation using the PLECS heat sink tool described in the 2-level converter section is used to estimate the losses in the 3-level rectifier as well. The IGBT1 probe circuit in Figure 29 operates as in the 2-level rectifier, with the same gain multiplier. For the IGBT2 loss calculation tool, the neutral IGBTs from one phase are input into the probe and the gains are multiplied to represent number of total devices and switching pairs in the neutral leg. The power losses computed for the 3-level topology are shown in Figure 30.

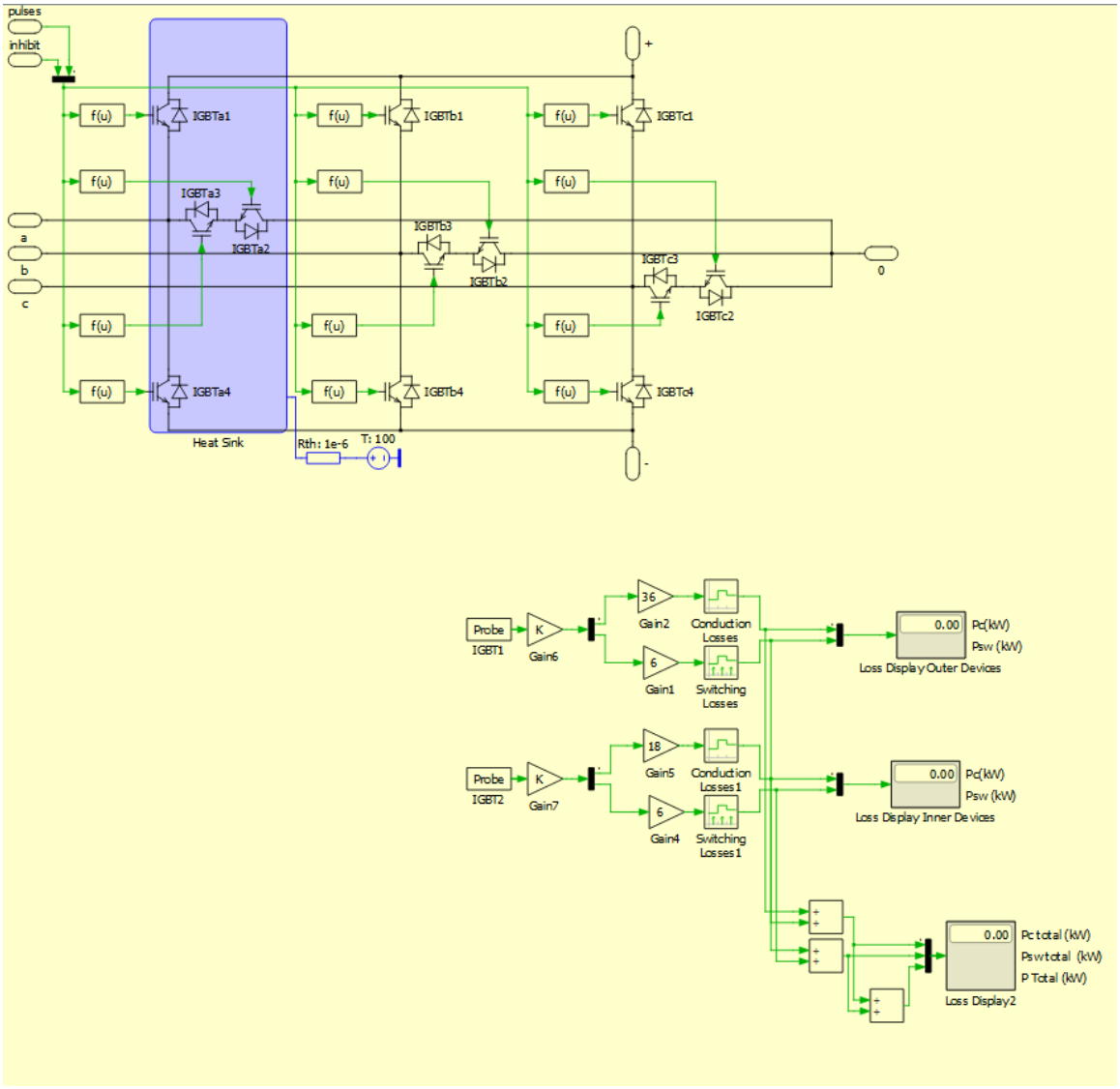

Figure 29. 3-level T type rectifier thermal modeling system in PLECS

Total simulated losses for the 3-level rectifier are shown in Figure 30.

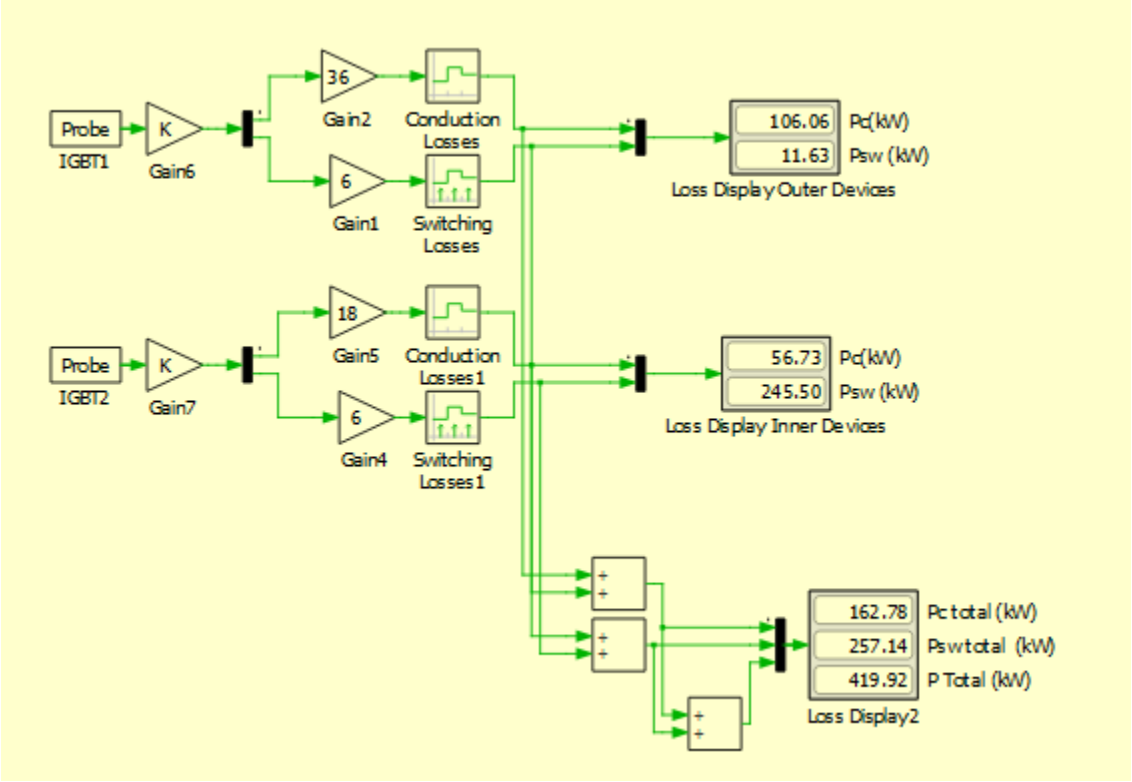

Figure 30. 3 level rectifier power loss results

The total losses in the 3-level rectifier are approximately 420 kW, which are lower than the 596 kW estimated for the 2-level converter. Even though the 3-level rectifier requires more switching devices than the 2-level rectifier, these devices only switch half of the voltage compared with the 2-level rectifier, so the total switching loss is lower. For the 35 MVA system being modeled, approximately 1.2% of total power is lost. While a significant improvement from the 2-level design, 420 kW is still a substantial amount of power losses affecting the efficiency of this topology.

The three-phase source currents drawn by the 3-level rectifier are plotted in Figure 31, showing significant switching frequency ripple.

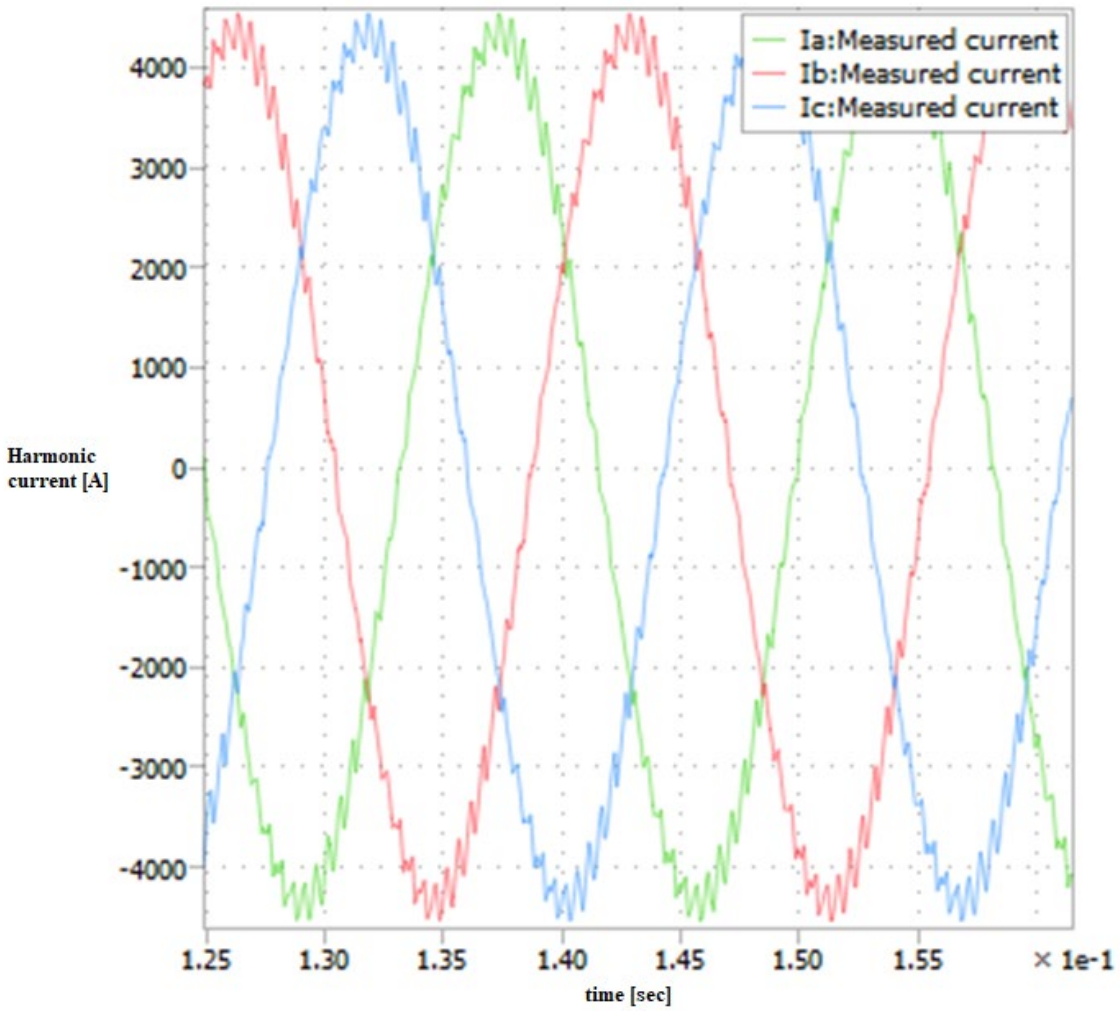

Figure 31. 3-level generator current waveform

The signal quality is greatly improved compared to the 2-level converter, but the overall power quality is still low. The current ripple is approximately 500A at the peaks of the sinewaves, which can have significant impact on the shipboard power grid.

The THD computed for the 3-level topology is approximately 3.97% across all three phases, showing an efficiency of just over 96%. The THD is almost half of the 2-level topology.

The Fourier analysis shown in Figure 32 features low harmonic content other than the switching frequency harmonics. In the 3-level converter, less harmonic distortion at

multiples of the fundamental frequency and switching frequency is observed in comparison to the 2-level converter.

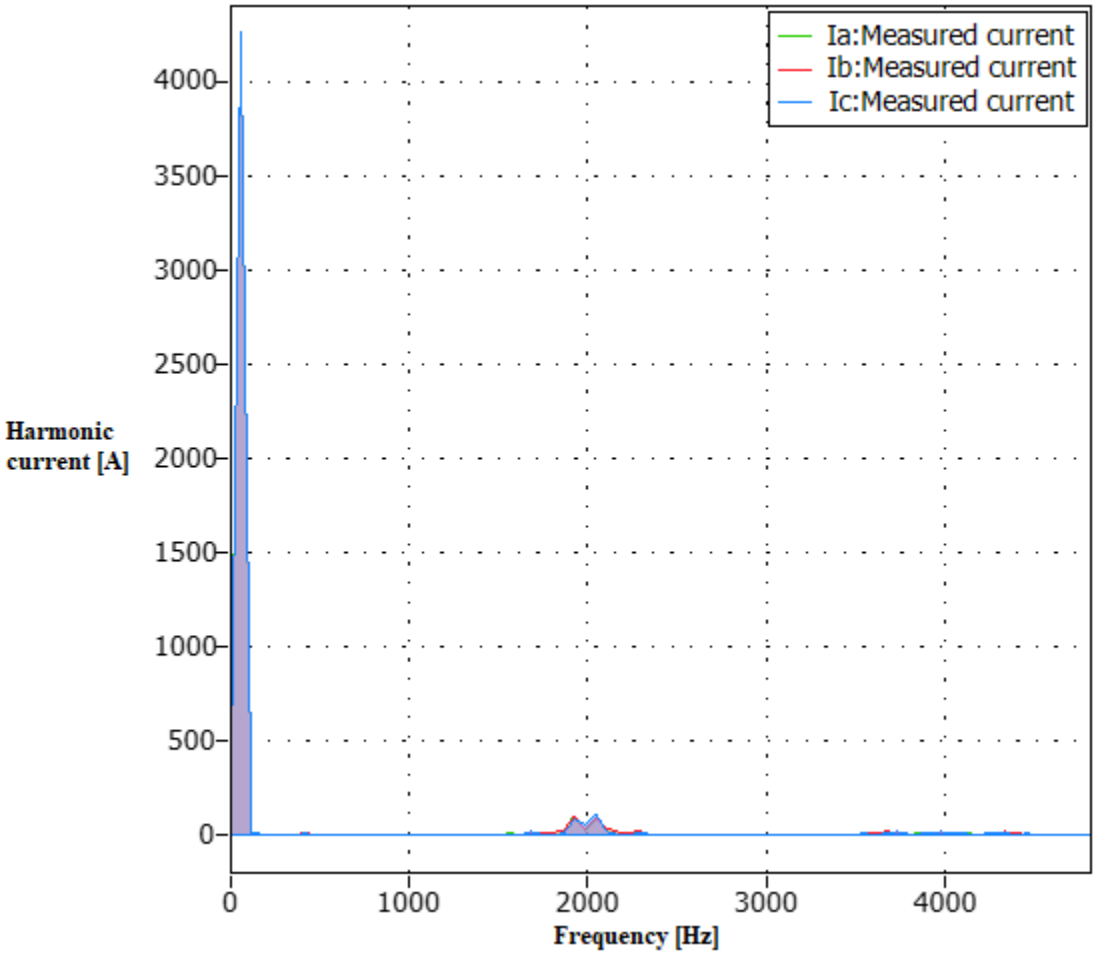

Figure 32. 3-level T type generator current Fourier analysis

Figure 33 is an enlarged view of the dominant harmonics observed in proximity of the switching frequency. The Fourier analysis performed on both topologies shows that harmonic currents are greatly reduced for the 3-level converter, which is a reason for the improvement in generator current THD.

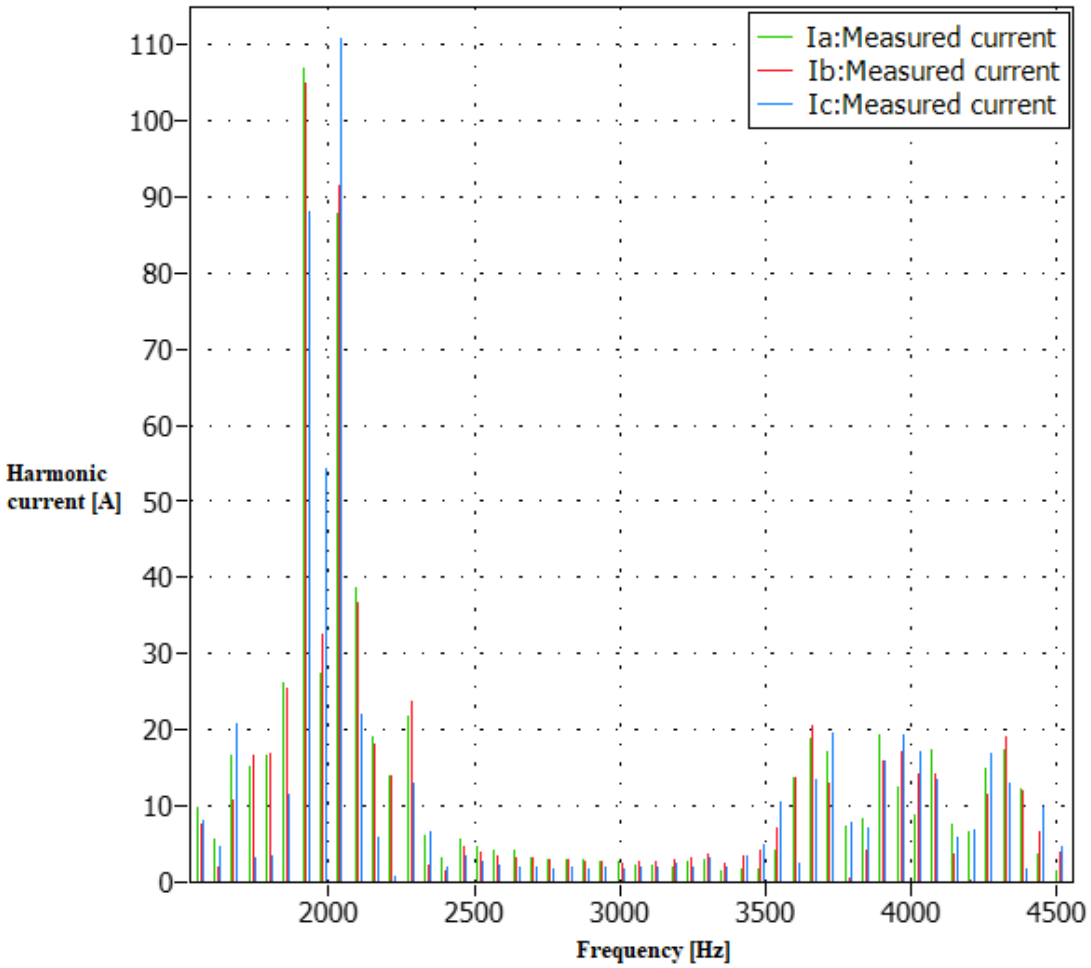

Figure 33. Fourier analysis for 3-level converter at switching frequency

Although the power quality is improved and the power losses are reduced in the 3-level rectifier compared to the 2-level topology, it is still an inefficient design for MVDC distribution systems and naval shipboard applications.

C. MMC

The MMC topology is a topology that also allows for bidirectional current flow. It can invert a DC current to a sinusoidal AC current output or rectify the generator AC current signal to regulate the DC bus. The MMC topology consists entirely of modules that can be bypassed without halting converter operation. The modules are 2-level converters with flying capacitors, arranged in series to form much smaller voltage steps that can more

effectively and efficiently model a minimally distorted sinusoidal signal [15]. These modules are connected so that they can be bypassed, and circuit operation continues with little impact to power quality. This promotes ease of maintenance and increased reliability of the overall topology. While the MMC offers improved reliability, its complexity is increased by the required control circuity that was discussed in Chapter II. Each capacitor is only shared by one phase leg and operates in theory as a single-phase system. This means that the capacitor only balances over 1 fundamental cycle. For the MMC, the capacitor energy storage requirement is 40kJ/MVA. In this MMC design, 12 switching devices are utilized per each of the 6 phase arms. The following equations show how the capacitance per module is calculated:

$$Energystorage = \frac{40kJ}{MVA} 35MVA = 1.4x10^6 Joules \tag{29}$$

$$CapacitorEnergy = \frac{Energystorage}{72} = 1.94x10^3 Joules \tag{30}$$

$$C = 2\frac{CapacitorEnergy}{(1x10^3 V)^2} = 40mF \tag{31}$$

In Figure 34, the PLECS heat sink tool used in the MMC topology is applied to the two IGBTs in one module.

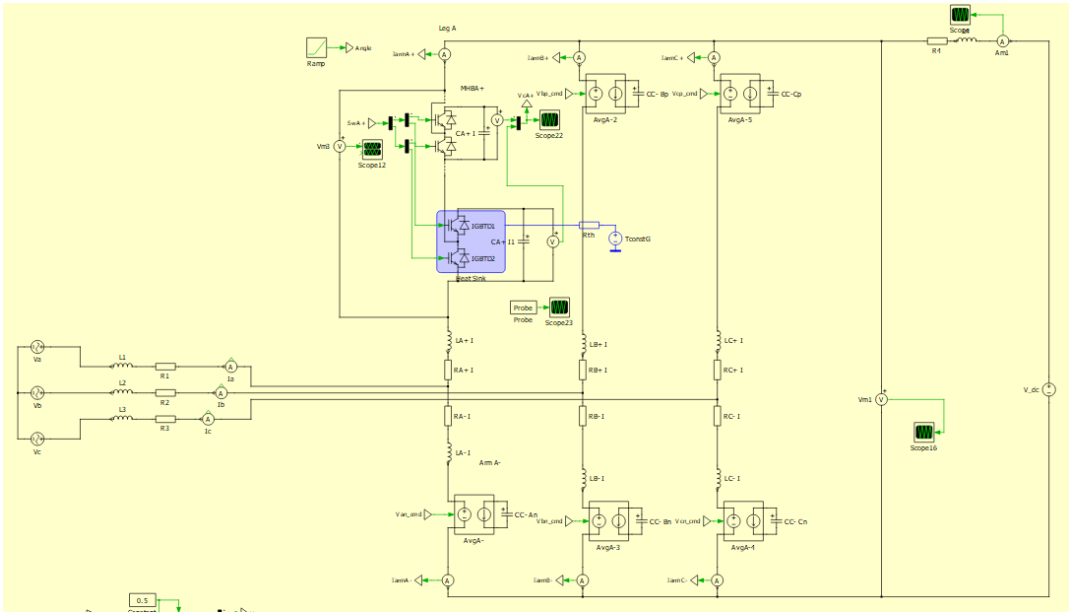

Figure 34. Modular multi-level converter PLECS circuit design

Figure 35 shows that the MMC control circuitry is much more complex than the control system required for the 2-level and 3-level topologies. Commands must be generated to control which module to switch on and begin conducting, capacitors within each module must be balanced, and current commands from each phase are fed into the PWM circuit to control the switching order.

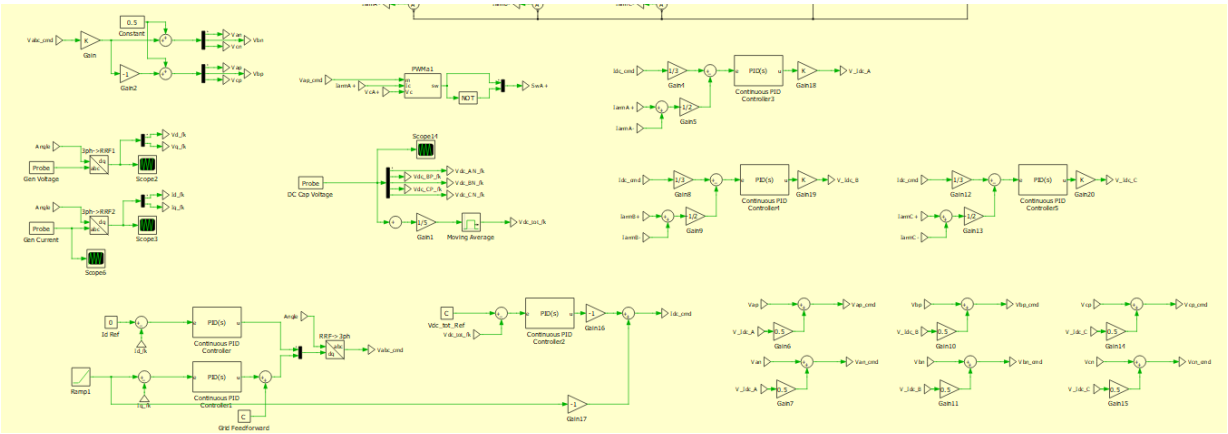

Figure 35. MMC control system circuits

The switching frequency for the MMC is set at 5 kHz for this study, however if the control algorithm is improved, the switching frequency can be reduced. The simulation results show that even with a 5kHz switching frequency, the switching losses of the MMC topology are reduced because only 1kV is switched in each switching event and the power quality is much higher compared to the 2- and 3-level devices because of the high voltage levels.

In the MMC topology, design is such that 12 levels are implemented, and the voltage level is small enough to get a much cleaner and more efficient generator current signal. With the smaller voltage at each level, design allowed for the use of a device rated at only 1.7 kV.

The generator current THD is greatly improved in the MMC due to the many additional levels. The generator current waveforms shown in Figure 36 show only minor ripple at the peaks.

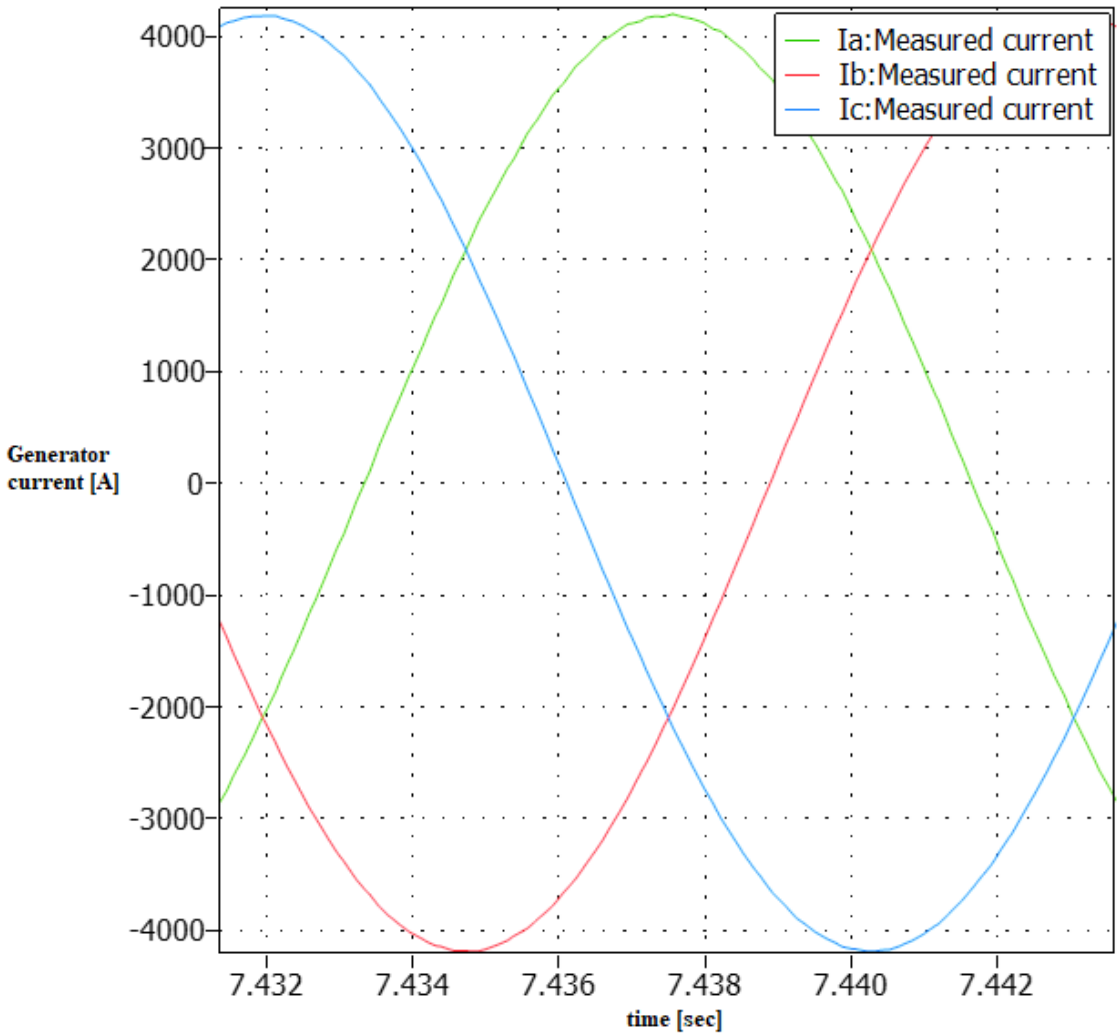

Figure 36. MMC generator current signal quality

THD for the MMC is displayed in Figure 37.

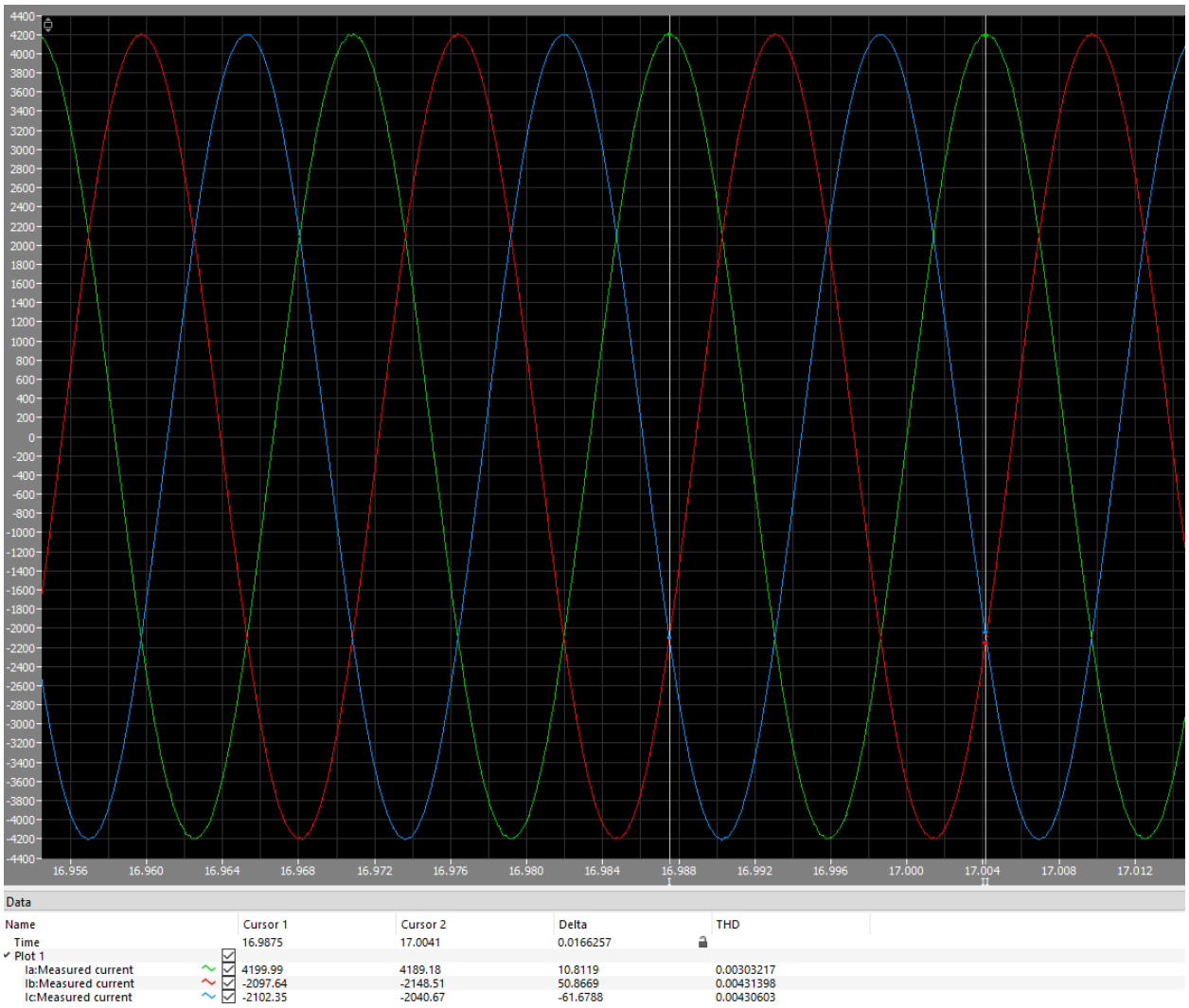

Figure 37. MMC THD calculation

The THD of the MMC topology is approximately 0.4% and no additional filtering capacitors are necessary on the DC bus.

When evaluating the harmonic content of the MMC generator current, low amplitude is observed at multiples of the fundamental frequency and there is no distortion observed at the switching frequency. Figure 38 shows the overall Fourier analysis spectrum up to 6 kHz, so that the response at the 5 kHz switching frequency can be observed.

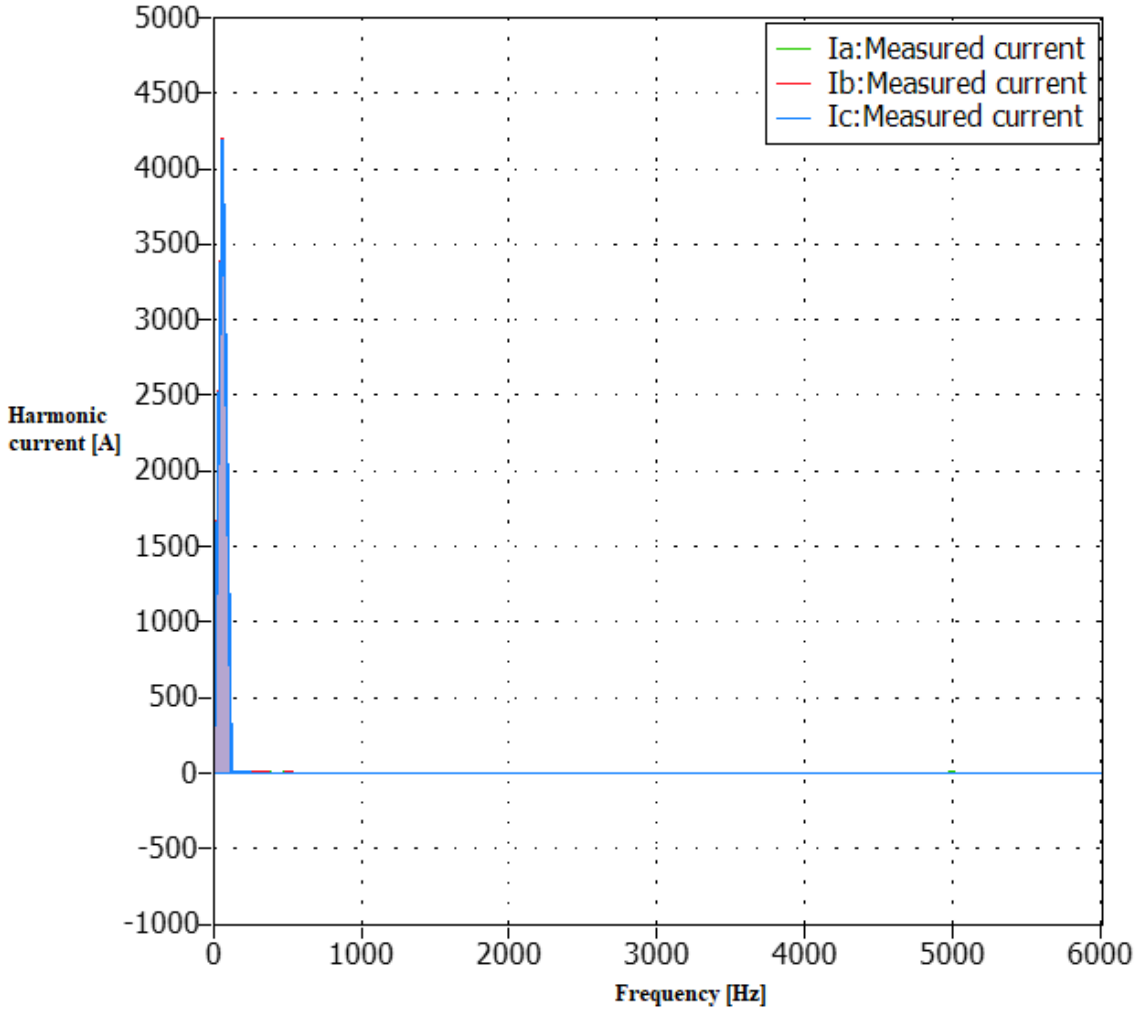

Figure 38. MMC Generator current Fourier analysis graph

One added benefit of the MMC in comparison to the 2 and 3-level topologies is that it did not require a high voltage and high capacitance capacitor for output signal filtering due to its flying capacitor in the modular design. Without additional high voltage capacitors on the DC bus, the MMC topology is much easier to implement in shipboard power systems. Figure 40 is an enlarged version of the Fourier analysis of the MMC generator current at the harmonics of the fundamental frequency. The peak current observed at 4 times the fundamental frequency (240 Hz) is 12A, which is a significant reduction from the 44A at the fifth harmonic observed in the Fourier transform of the 2-level converter. The harmonic current peak is displayed in Figure 39.

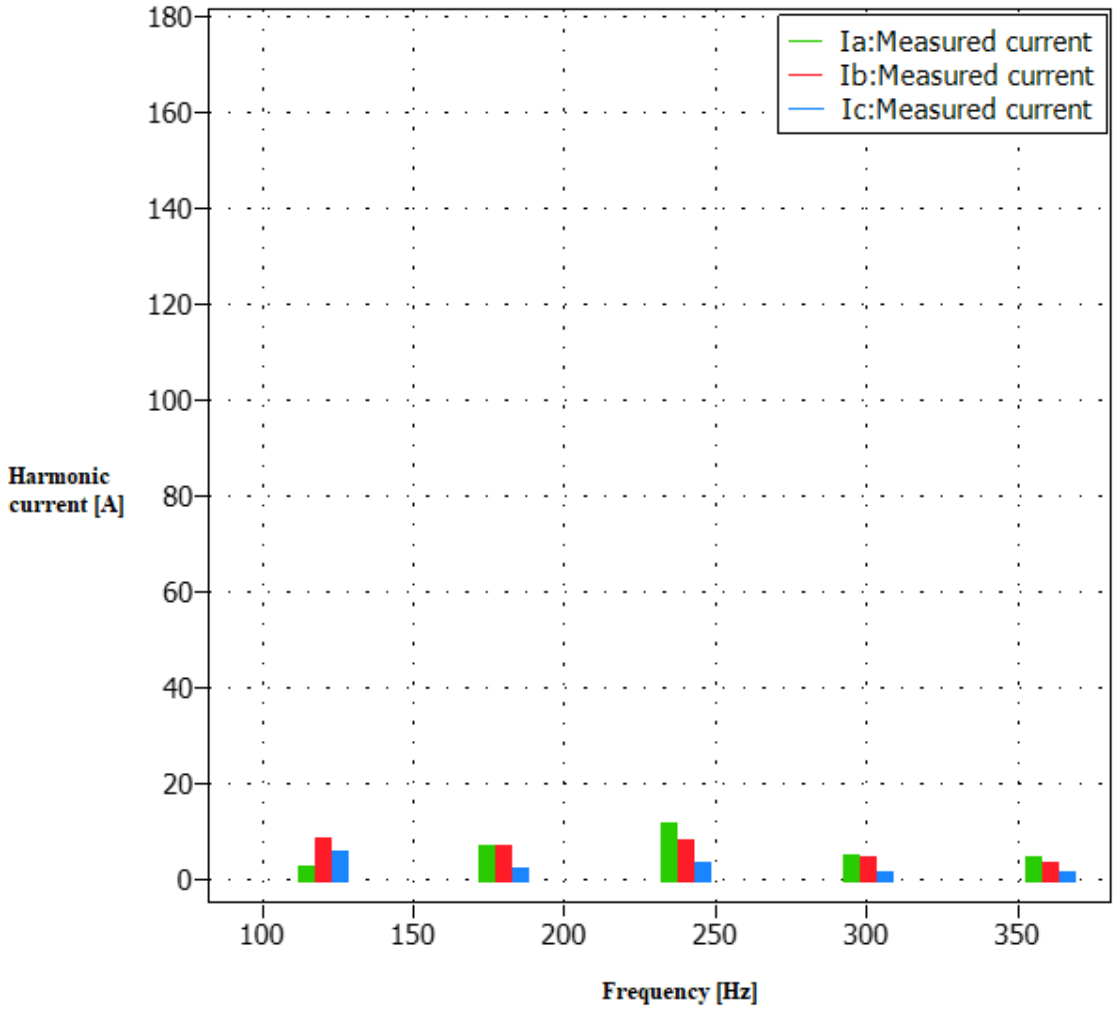

Figure 39. Fourier analysis at multiples of fundamental frequency for MMC.

Capacitor balancing accounts for a large portion of the additional control circuitry required for the MMC topology. In the PLECS MMC model, a sorting algorithm is implemented to achieve this function. Figure 40 shows that the control is working because the capacitor waveforms are balanced. In Figure 40, 12 capacitor voltages on one phase arm are observed during steady state operation. The capacitors are balanced well over one line cycle.

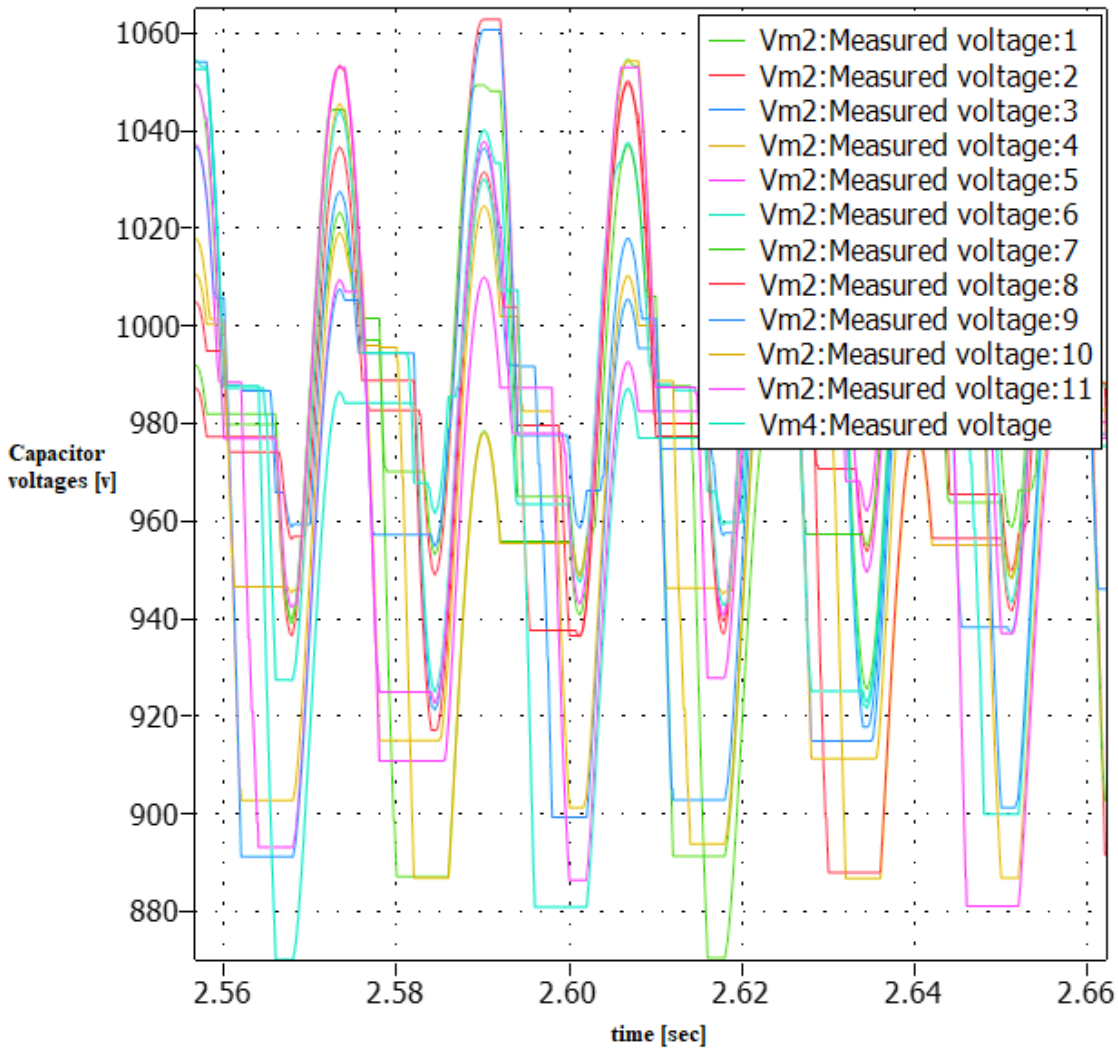

Figure 40. MMC capacitor balancing voltages

The calculated MMC conduction losses, switching losses and total losses are shown in Figure 41. The total losses were reduced to 291kW, leading to a 99.17% efficiency. The MMC topology offers a much-improved efficiency compared to the 2-level and 3-level devices, especially the switching losses. This is even when a lower switching frequency (2 kHz) is used for those topologies. The MMC topology can be utilized effectively for naval shipboard design, but its benefit of bi-directional current flow is unnecessary.

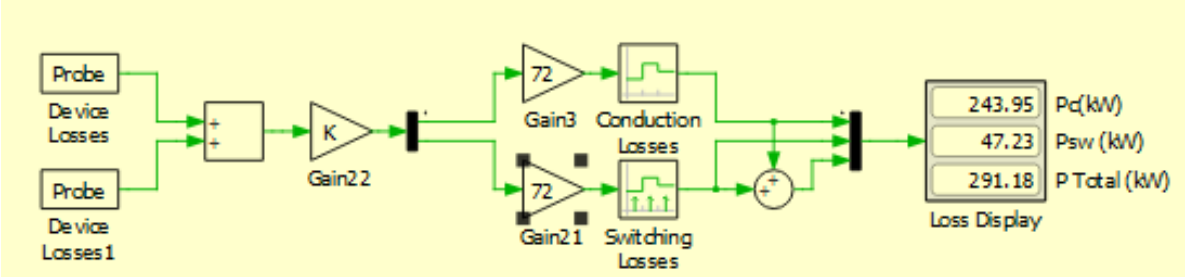

Figure 41. MMC power loss simulation results

D. MMR

The MMR topology operates on the same modular concept as the MMC, but half of the modules are replaced by a set of diode stacks. This setup offers volume reduction and loss reduction that are shown in the loss calculation simulation results. This topology is the only one that does not allow for bi-directional power flow, which is unnecessary for the shipboard power system that is being studied. The complexity of the control circuity remains the same and is the largest drawback of this topology. Like the MMC, the MMR topology features ease of maintenance and reliability due to the modular design. The reliability of the MMR is improved with respect to the MMC because it requires fewer modules and replaces some of them with diodes, which are more reliable and have greater power density. Figure 42 shows the PLECS configuration of the MMR topology.

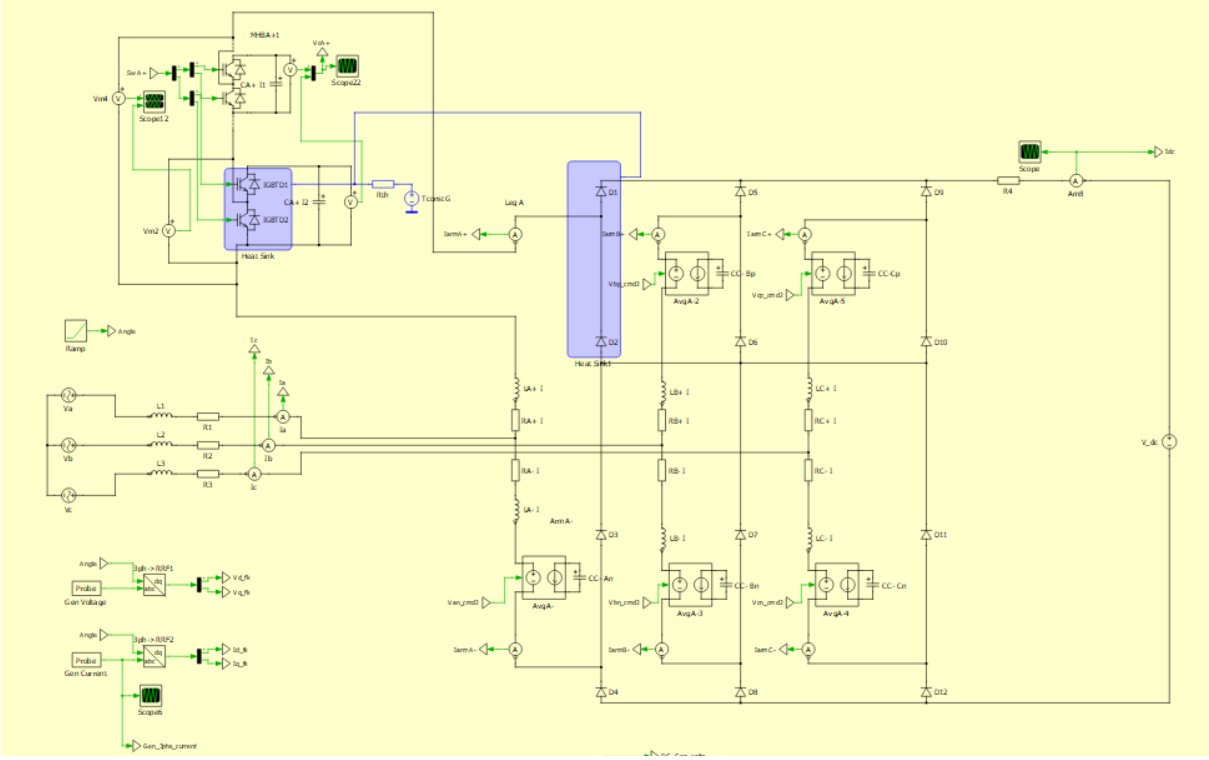

Figure 42. Modular multi-level rectifier overview

To be able to accurately measure device losses in the MMR topology, a PLECS heat sink tool is used on the IGBT modules just as it was used for the MMC, with an additional heat sink used to capture diode losses. The diodes modeled in this simulation are Infineon D2700U and capable of blocking 4.5 kV. The control circuit for the MMR system is shown in Figure 43.

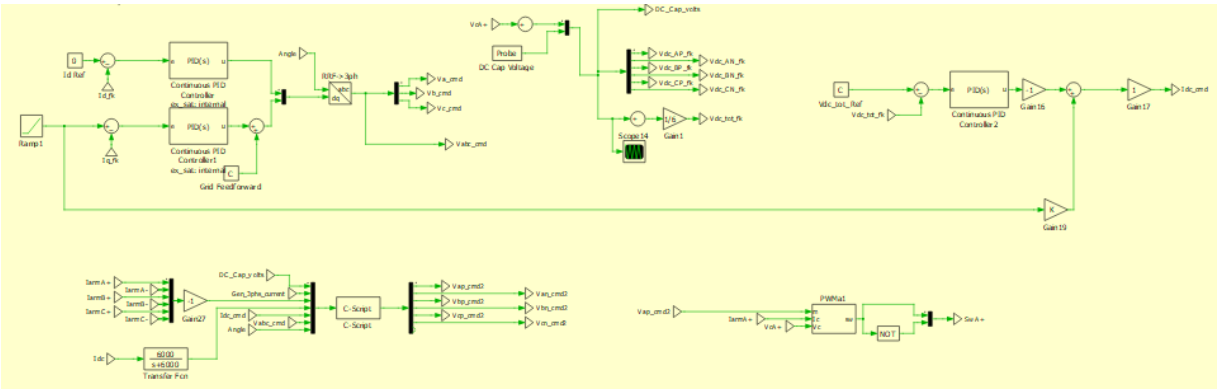

Figure 43. MMR command control system

Since the MMR topology for half of its design operation is the same as the MMC, the control circuitry used from capacitor balancing, phase current control, and switch signals are more complex than the control systems required for the 2-level and 3-level rectifiers. The switching frequency is set to 5kHz, as for the MMC.

The power quality is excellent for the MMR topology at steady state. Some minor distortion is observed at the peaks but can be further corrected in the control circuitry portion of the converter. The generator current waveform is shown in Figure 44.

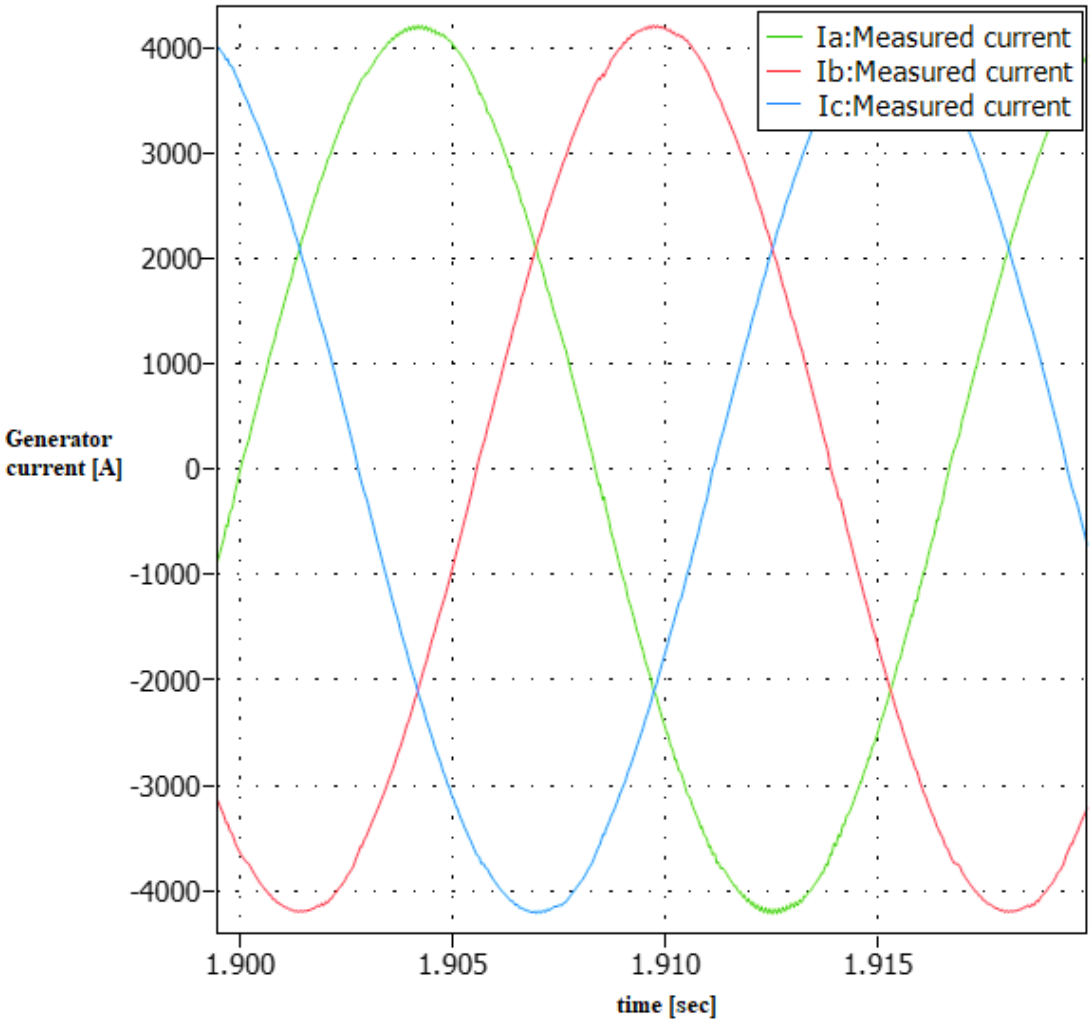

Figure 44. Generator current waveform

Total power loss for the MMR is just above 196 kW, making it the lowest losses of all four rectifier topologies. The MMR topology offers all the benefits to reduce losses as the MMC with lower rated switching devices, but only contains half of the switching modules of the MMC. The same module is picked for MMR as in MMC, so the total system energy storage requirement is reduced by half in MMR compared with in MMC.

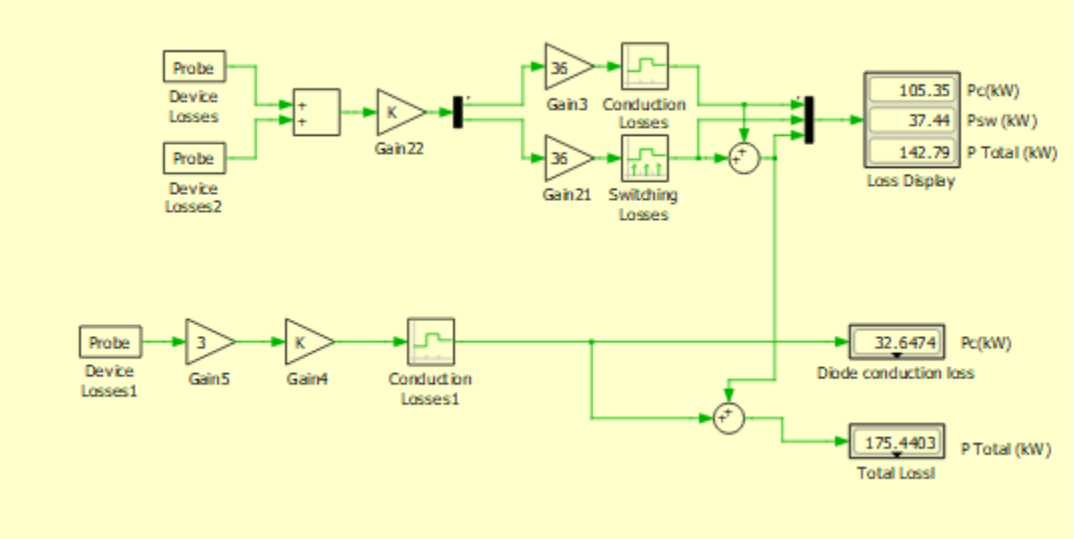

Figure 45. MMR simulation losses

The MMR capacitor balancing waveforms are similar to that of the MMC device, as shown in Figure 46. The MMR capacitor balancing control circuitry is still able to effectively balance the capacitors within the switching modules.

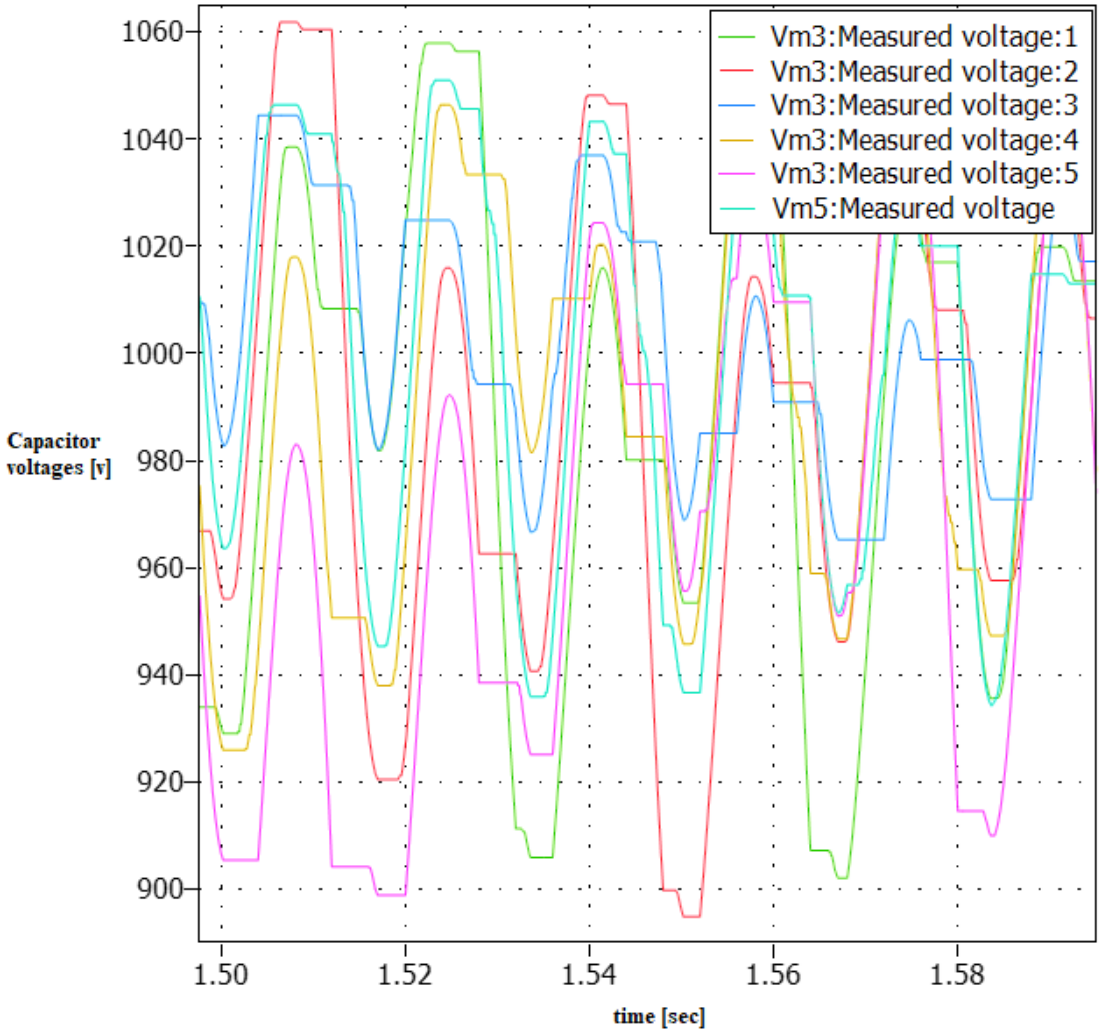

Figure 46. MMR Capacitor balancing voltage

The THD is under 1% for the MMR, which results in excellent power quality. The control system can be adjusted to mitigate the small distortion that is observed in the generator current waveform.

The Fourier analysis of the MMR generator currents in Figure 47 shows slight distortion at multiples of the fundamental frequency. Like the MMC device, no distortion is observed at the switching frequency, which is also set at 5 kHz.

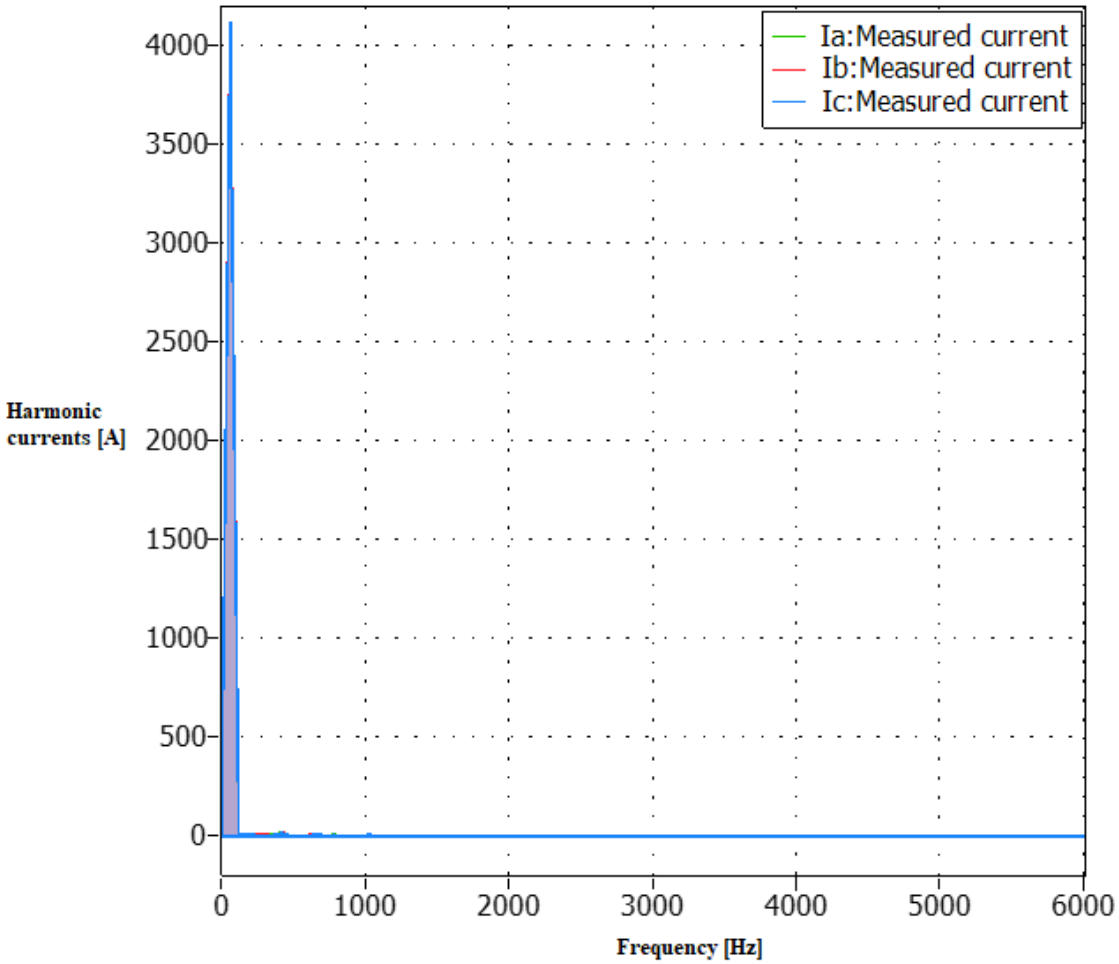

Figure 47. MMR Fourier analysis

Figure 48 is an enlarged view showing the distortion at multiples of the fundamental frequency. The largest spike in harmonic current is observed at 400 Hz, like the MMC topology and the peak is approximately 19A. This is an increase from the 12A observed for the MMC device, but still a considerable decrease from the 44A observed on the 2-level topology.

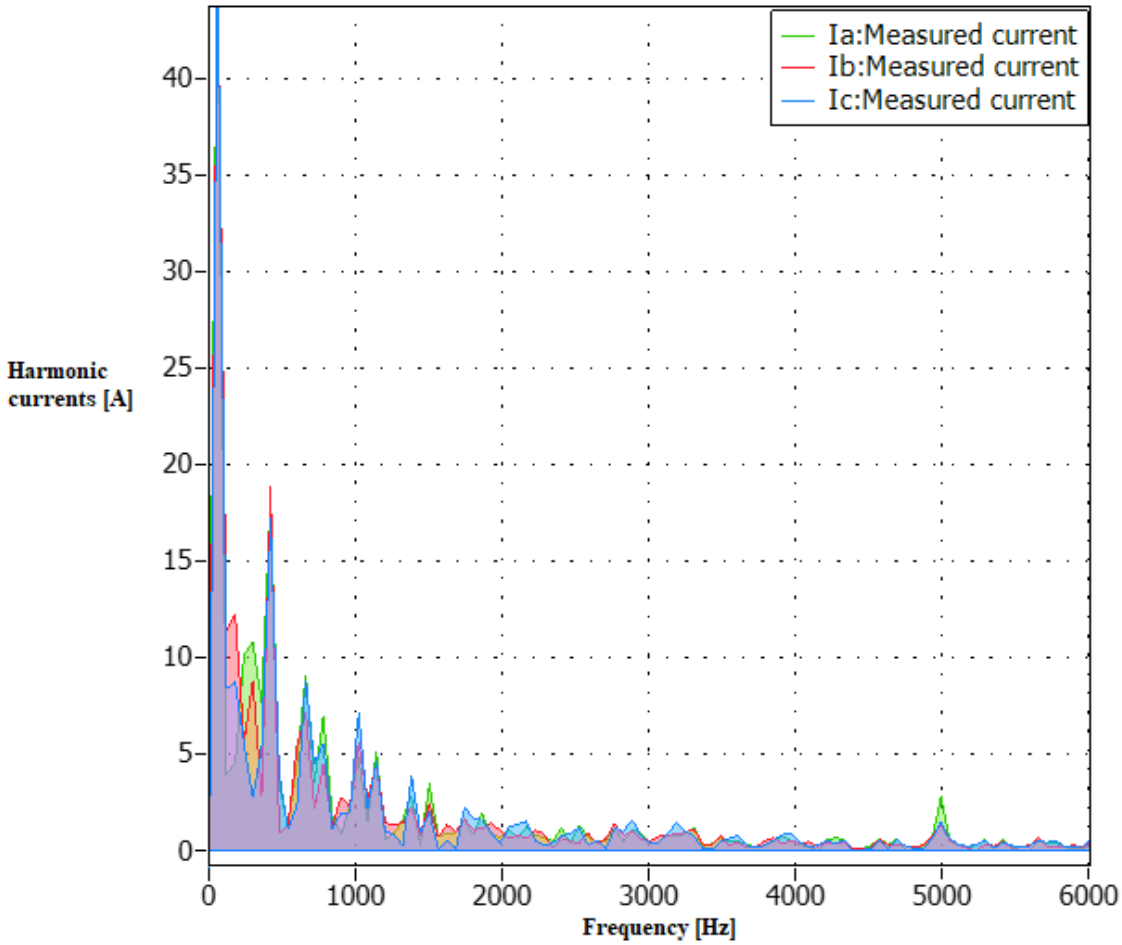

Figure 48. Fourier analysis at multiples of switching frequency for MMR.

Overall, the MMR topology is an excellent option for naval shipboard applications of power conversion. The aspect of one-directional current flow has no bearing on the shipboard power system and is preferred as power is never required to flow back to the AC generator.

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V. ANALYSIS OF SIMULATION RESULTS

The power losses and AC side current THD are summarized and compared in Table 1 for the four rectifier topologies.

Table 1. Loss, efficiency, THD results for all topologies under study

Topology	Conduction Losses (kW)	Switching Losses (kW)	Total Losses (kW)	Loss percentage (%)	THD(%)	Efficiency (%)
2-Level Converter	163.81	431.98	595.79	1.7	5.6	98.3
3-Level Converter	162.78	257.14	419.92	1.2	3.97	98.8
Modular Multilevel Converter	243.95	47.23	291.18	0.83	0.4	99.17
Modular Multilevel Rectifier	142.79	32.65	175.44	0.53	0.77	99.23

Table 1 shows that the MMC features higher conduction losses than the 2 and 3-level converters due to the lower voltage rating of the selected switching device. The switching losses are much lower in the MMC and MMR than in the 2-level and 3-level topologies. All simulations are performed for 35 MVA systems and the 2-level rectifier shows almost 2% total losses, which make this topology not suitable for such high power, high voltage application. The 3-level converter does not offer much improvement in the way of total losses, but it features improved power quality due to the additional voltage level. The MMC and MMR topologies clearly perform above the 2-level and 3-level topologies in efficiency, power quality, and THD. Since the MMR replaces half the number of IGBT devices required by the MMC by high voltage diodes, it further brings down the total losses to close to half a percent of the rated power. The only drawback of the MMR over the MMC is that the MMR does not allow bidirectional current flow, meaning that power could not be directed back to the AC side.

Lastly, looking at the energy storage requirement, the MMC and MMR require DC capacitors to store transient energy storage within one fundamental cycle. Table 2 compares the energy storage requirements and capacitance values for the four topologies. The MMC and MMR requires more energy storage than the classic 2-level and 3-level converters. This is the key drawback since it means more volume of capacitors. For Naval shipboard applications, where space and volume are a limiting factor, this could become a serious issue.

Table 2. Topology energy storage and capacitance calculations

Topology	Energy Storage (J)	Capacitance (F)
2-Level Converter	292,000	4.00E-03
3-Level Converter		
Modular Multilevel Converter	1.40E+6	4E-02
Modular Multilevel Rectifier	7.00E+5	

However, since MMR has reduced the capacitor volume by half compared with MMC, there is a chance that MMR can achieve similar or even less volume compared with the classic converters. For example, first, MMR will have less filter and thermal management components compared with the 2 or 3 level converters. Second, MMR, due to modular design, can utilize the space more efficiently, while the classic converters will have complicated mechanical layout, such as bus bars. Third, MMR only require low voltage capacitors, i.e. 1kV, but the classic converter will require one high voltage capacitor. To connect multiple low voltage capacitor in series to achieve high voltage means additional balancing circuit and design margin, which can increase volume of the capacitor related components. In addition, advanced control can also help to further reduce the energy storage requirement. Further detailed study is necessary to answer these questions.

VI. CONCLUSION AND FUTURE WORK

One of the major concerns with an MVDC shipboard power distribution system is the number of power converters that are required to supply the appropriate AC power for all AC loads on the ship. There are not many power electronics converters commercially available that can efficiently rectify a 6.6 kV AC input into a 12 kV DC output without significant current distortion. The MMR topology solves this problem.

The MVDC bus voltage is controlled by ac/DC power electronic converters installed between the AC generator and the DC bus. Constant voltage delivery over a wide range of generator speeds is essential to the operation of the power distribution system. With DC link voltage remaining constant to the input of the inverter for the electric drive motor, the current is the controllable variable required to produce enough torque necessary to have the propulsion motor bring the ship to the desired speed.

This research performed a comparative evaluation of 4 active rectifier topologies for MVDC shipboard applications, including 2 level, 3 level, MMC and MMR, based on different performance parameters including efficiency and power quality.

Based on the simulated conduction losses, switching losses, efficiency and power quality, the MMR is the topology with the best performance among the four rectifiers analyzed, except for a slightly larger THD than the MMC. The MMR can be a good fit for AC to DC rectification in warships because bidirectional current flow is not required.

The foreseeable future of naval propulsion includes power rectifiers and electric drives. The results of this study provide the foundation for future research targeting decreased cost and size for the rectifier topology in MVDC shipboard applications.

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