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A RELIABILITY STUDY ON THE EFFECTS OF HTOL AND HIGH-CURRENT DENSITY STRESS TESTING ON COMMERCIAL-GRADE VERTICAL N-TYPE PD/GAN SCHOTTKY DIODES

by

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Traditional silicon-based power electronics have approached their performance limits for high-power electronic applications. The U.S. Navy is actively pursuing the implementation of wide bandgap (WBG) semiconductor materials to realize reliable devices for use in high-power, high-current, and high-voltage applications. Gallium nitride (GaN) is a promising candidate for these applications due to its inherent material properties, and recent efforts to produce high quality bulk GaN have begun to enable the production of commercial-grade devices. However, much is still unknown regarding the reliability of GaN devices, especially Schottky diodes, which are often affected by issues involving barrier height inhomogeneity (BHI). First, a stress testing system capable of taking in-situ current-voltage-temperature (I-V-T) measurements while applying electrical stress was constructed. Next, a sample of commercial-grade vertical n-type palladium/gallium nitride (Pd/GaN) Schottky diodes were subjected to a series of step current and constant current stress tests. Current densities above 1.3 kA/cm^2 were achieved. Finally, the effects of electrical stress on material properties were observed through comparison of pre-, post-, and in-situ I-V-T data. The in-situ I-V-T measurements enabled degradation to be observed as a function of stress time. Results show that significant degradation to the material properties of the Schottky diodes occurs within the first few hours of stress testing.

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Traditional silicon-based power electronics have approached their performance limits for high-power electronic applications. The U.S. Navy is actively pursuing the implementation of wide bandgap (WBG) semiconductor materials to realize reliable devices for use in high-power, high-current, and high-voltage applications. Gallium nitride (GaN) is a promising candidate for these applications due to its inherent material properties, and recent efforts to produce high quality bulk GaN have begun to enable the production of commercial-grade devices. However, much is still unknown regarding the reliability of GaN devices, especially Schottky diodes, which are often affected by issues involving barrier height inhomogeneity (BHI). First, a stress testing system capable of taking in-situ current-voltage-temperature (I-V-T) measurements while applying electrical stress was constructed. Next, a sample of commercial-grade vertical n-type palladium/gallium nitride (Pd/GaN) Schottky diodes were subjected to a series of step current and constant current stress tests. Current densities above 1.3 kA/cm^2 were achieved. Finally, the effects of electrical stress on material properties were observed through comparison of pre-, post-, and in-situ I-V-T data. The in-situ I-V-T measurements enabled degradation to be observed as a function of stress time. Results show that significant degradation to the material properties of the Schottky diodes occurs within the first few hours of stress testing.

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LIST OF ACRONYMS AND ABBREVIATIONS

AC	Alternating Current
ALT	Accelerated Lifetime Testing
BHI	Barrier Height Inhomogeneity
C-V	Capacitance-Voltage
DC	Direct Current
DD	Double Diode
DUT	Device Under Test
FL	Fermi-Level
GaN	Gallium Nitride
GCU	General Control Unit
GPIB	General Purpose Interface Bus
HEMT	High Electron Mobility Transistor
HTOL	High Temperature Operating Life
IP	Internet Protocol
ISR	Interface Specific Region
I-V	Current-Voltage
I-V-T	Current-Voltage-Temperature
MS	Metal-Semiconductor
Pd	Palladium
PN	P-type-N-type
SBH	Schottky Barrier Height
Si	Silicon
SiC	Silicon Carbide
SD	Single Diode
TEC	Thermoelectric Cooler
TCU	Temperature Control Unit
WBG	Wide Bandgap

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I. INTRODUCTION

A. MOTIVATION

The U.S. Navy has been at the forefront of technological innovation in the United States. It revolutionized the use of steam engines, gas turbines, and nuclear power to enhance its sea power, increasing its ability to operate over greater distances for longer periods of time. In recent years, there has been an increasing interest in advancing electric power and energy systems; naturally, the U.S. Navy should lead the way for implementing such technology, continuing to enhance its power projection.

Critical research in the field of advanced electric power is already underway. The U.S. Navy is researching high-power electronic materials for solid-state power components, power conversion, and direct current (DC) distribution systems [1]. Enhancing electrical power systems reduces the dependence on consumable fuel systems of the U.S. Navy, a limiting factor for operations at sea.

Advanced combat systems, such as the railgun, high-energy lasers, high-power radars, and electronic warfare (EW) systems, all have demanding power and energy needs. These systems currently operate using bulky electrical power systems, relying on numerous alternating current (AC) components to produce and store energy in large battery banks which have inherently low power density. This poses a problem for outfitting naval vessels, which have limited space available and strict weight requirements. Advancements in high-power electronics will lead to an increase in floodable length of a ship, freeing up vital weight and space, and will enable the utilization of the abovementioned systems.

However, as with any military technology, power electronics need to meet high reliability standards. Although early reliability testing at academic facilities, such as the Naval Postgraduate School (NPS) and United States Naval Academy (USNA) has occurred, neither of these institutes presently has a robust and permanent means of conducting reliability testing for power electronic devices. Commercial systems capable of conducting standard high-temperature operating life (HTOL) testing and accelerated life testing (ALT) exist, but they are designed for large-scale research and are rather expensive.

They are capable of testing hundreds of devices at a time. NPS and the USNA have a need for a small-scale HTOL stress test system to conduct lower-level student research.

To meet the power requirements expected for the aforementioned systems, the U.S. Navy is exploring the use of several wide bandgap (WBG) semiconductors for power electronics [1], [2]. Due to their material properties, WBG materials show promise in their ability to outperform silicon devices for more robust power electronics. WBG semiconductors enable high operating voltages, faster switching frequencies, higher operating temperatures, and higher power densities. A key wide bandgap material that is being considered for use is gallium nitride (GaN), which promises to outperform traditional Si power devices and promises significant savings in power efficiency and density in power electronic circuits through its use as the baseline material for fabricating electronic devices. Though GaN has been in use for years by the Navy as a material for RF and optoelectronic applications, the technology to fabricate high power GaN devices on native (bulk) GaN substrates, a necessity for power devices, is still maturing, and much is still unknown regarding the reliability properties and long-term performance characteristics of devices fabricated on bulk GaN. A key basic power device is the Schottky diode, which is used in numerous power electronic applications due to the low switching speed and reasonably high blocking voltage capability of the device. While high power GaN Schottky diodes have been proven in research, little research has been conducted on the reliability of these devices. Understanding the reliability of high power GaN Schottky diodes is a requirement for successful integration into future Navy warfighting platforms.

B. RELATED WORK

In 2009, a doctoral student at Pennsylvania State University conducted research involving WBG semiconductors, as detailed in [3]. He investigated the Schottky contacts of several WBG semiconductors, namely silicon carbide (SiC), gallium nitride (GaN), and zinc oxide (ZnO). His research involved electrically characterizing Schottky diodes through current-voltage-temperature (I-V-T) measurements. He observed the effects of barrier height inhomogeneities (BHI) with respect to the Richardson constant. A portion of

his objective was to develop a new method of extracting the Richardson constant from electrical measurements.

In 2016, a student at NPS conducted reliability research on GaN [4]. Specifically, he accompanied characterization and reliability testing on vertical n-type GaN Schottky contacts. He conducted accelerated lifetime tests on multiple GaN Schottky contacts using a stress-measure-stress system. He completed 170 hours of testing at current densities of 2.3 kA-cm^{-2}. He examined the degradation physics of a variety of Schottky contact metals, including molybdenum, molybdenum-gold, and chromium-gold.

C. OBJECTIVE

This research effort was divided into two main objectives. The first was to design and build a small scale HTOL stress testing system capable of electrically stressing and characterizing Schottky diodes. The stress system was intended to be used at NPS and USNA for current and future reliability research. The system needed to conduct a series of stress-measure-stress tests over a course of several hours while taking simultaneously extracting in-situ characterization data through I-V-T measurements, under forward and reverse voltage bias. Once constructed and verified operational, the HTOL system was used to execute reliability tests on commercial vertical *n*-type GaN Schottky diodes.

The second objective of this work was to examine the effects of high current density electrical stress on vertical palladium (Pd) GaN Schottky diodes grown on high quality bulk GaN substrates. Stress testing was accomplished through stepped current and constant current tests. This effort investigated the presence of BHI and any impacts it may have on device degradation. This research examined observations of “single” and “double” diode characteristics present within our diodes. Pre- and post-stress I-V-T measurements were used along with in-situ I-V-T measurements to characterize devices before, during and after stress testing. I-V-T measurements were used to extract useful Schottky parameters, such as reverse leakage current, forward series resistance, barrier height, and inhomogeneity spreading factor. Finally, these parameters were analyzed as a function of stress time to better understand how these devices degrade over time.

Few reliability research efforts have focused on GaN Schottky diodes, and of those that have, many have yet to provide conclusive results. No specific stress testing research efforts on commercial vertical *n*-type GaN Schottky diodes involving in-situ measurements and observations of degradation as a function of stress-time could be found. Therefore, this research is unique and provides insight into how GaN Schottky diodes degrade and what effects high current density have on their material and electrical properties.

D. ORGANIZATION

Chapter II contains all the necessary background information for this research; it reviews GaN technology used for power electronics, the ideal and non-ideal theory for Schottky diodes, and relevant reliability research involving GaN. Chapter III summarizes the HTOL system design, construction, and performance characteristics. Chapter IV introduces the vertical n-type GaN Schottky diodes used in this research and discusses the experimental methodology. Chapter V presents the results and findings of this research. Finally, concluding remarks and recommendations for future work are included in Chapter VI.

II. BACKGROUND AND THEORY

This chapter presents the necessary background information required to understand the objective of this research. The chapter is separated into four sections. The first section includes a background of GaN technology as it applies to power electronics. The second and third sections review the ideal and non-ideal theory of Schottky diodes, respectively. Current reliability research involving GaN and HTOL testing for power electronic devices is presented in the fourth section.

A. GaN SEMICONDUCTOR TECHNOLOGY

Silicon (Si) has been the dominate material of choice for most semiconductor devices in the industry. Si has a high material abundance, relatively good semiconductor properties, and is easy to fabricate into electronic devices; however, it is reaching its performance limits [5]. Operational limits are strictly dependent on the material properties of Si. Researchers are investigating a variety of new WBG materials, specifically SiC and GaN, to replace Si power devices. SiC is currently the choice WBG semiconductor technology for many commercialized power electronics; however, GaN has potential to be the next technology for future power electronic devices due to the greater inherent mobility of charge carriers in the material, resulting in lower on-state resistances in devices. GaN technology is still maturing, and much is still unknown surrounding the reliability of GaN, making it a prime material for academic research. This section reviews the properties of GaN as they relate to Si and SiC, fabrication processes, and device structures of GaN.

1. GaN Material Properties

WBG semiconductors are described as any material having a bandgap substantially in excess of the bandgaps of materials currently in general use, such as Si [6]. This amount is further defined as a bandgap of 2.2 eV or higher. Both SiC and GaN have a bandgap in excess of 2.2 eV and therefore are classified as wide bandgap semiconductor.

Semiconductors have a large range of material properties, but only a few need to be discussed as they relate directly to power electronic applications. Relevant properties

include bandgap (E_g), critical electric field (E_c), carrier mobility (μ), and thermal conductivity [5]. A summary of these properties can be found in Table 1. Carrier mobility could be for holes or electrons, but electron mobility is generally the desired property used for power applications. Materials with larger bandgaps have lower intrinsic carrier concentrations which reduces reverse leakage current when a device is operating under blocking conditions. The critical electric field of a material is inversely related to the required thickness of the drift region of the material to achieve a desired breakdown voltage and on-state resistance. If the field strength is larger, the drift region thickness is smaller, reducing the resistance and subsequent conduction losses while in the on-state. Carrier mobility is proportional to the achievable power switching speeds; thus, a higher mobility enables power electronic device to operate at higher frequencies. Finally, thermal conductivity is related to the ability of the material to dissipate conducted heat losses. A higher value indicates the material is more effective at dispersing heat, which can lower system cost by reducing the need for external heat sinks.

Table 1. Relevant material properties of Si, SiC, and GaN. Adapted from [5].

Material Property	**Si**	**4H-SiC**	**GaN**
Bandgap (eV)	1.12	3.26	3.4
Critical electric field (10^6 V/cm)	0.3	3.5	3.3
Electron mobility ($cm^2/V \times sec$)	1500	650	990
Electron saturation velocity (10^6/sec)	10	20	25
Thermal conductivity ($W/cm^2 \times K$)	1.5	5	1.3

Based on the described material properties, GaN is a promising material for power electronics. Advantages of GaN comprise of a bandgap that is about three times greater than Si, slightly higher than SiC and a critical electric field that is 10 times greater than Si, and slighter smaller than SiC. The main disadvantage of GaN is its lower thermal conductivity, almost five times smaller than that of SiC and slightly smaller than Si [5].

2. GaN Device Structures

Before discussing fabrication methods used for GaN it is worth briefly introducing the two types of device structures, namely lateral and vertical. These structures are named

for the direction in which current flows through the device. Due to limitations in the fabrication process, GaN-based device structures have been primarily lateral, but recent research efforts have enabled more feasible vertical structures.

High electron mobility transistors, or HEMTs, are the primary example of a lateral device. GaN HEMTs have a high operating frequency and decent transport properties but require a large amount of space be left between the gate and drain to achieve high breakdown voltages [5]. Current density ratings of HEMTs are generally low, as large area lateral devices severely reduce switching times and are not practical. This limitation prevents the use of HEMTs in medium to high-power applications where large current density ratings are crucial. Figure 1 shows an example of a generic GaN HEMT structure.

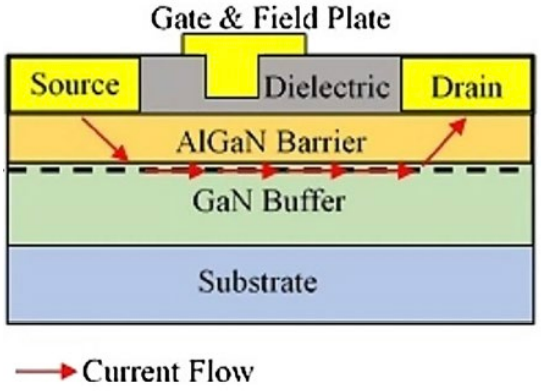


Figure 1. Generic cross-section schematic of Al/GaN/GaN HEMT structure. Source: [5].

Additional limitations of GaN lateral devices arise from the buffer layers. Buffer layers are susceptible to charge trapping, reducing device electrical and thermal performance. Increased stress across the buffer layers restricts their thickness, limiting breakdown voltages. Vertical structures are much more desirable for high-power applications. Since they do not require buffer layers and have thick epitaxial layers, they can achieve higher breakdown voltages while maintaining good electrical and thermal performance characteristics [7]. Example cross-sections of vertical GaN device structure are shown by Figure 2.

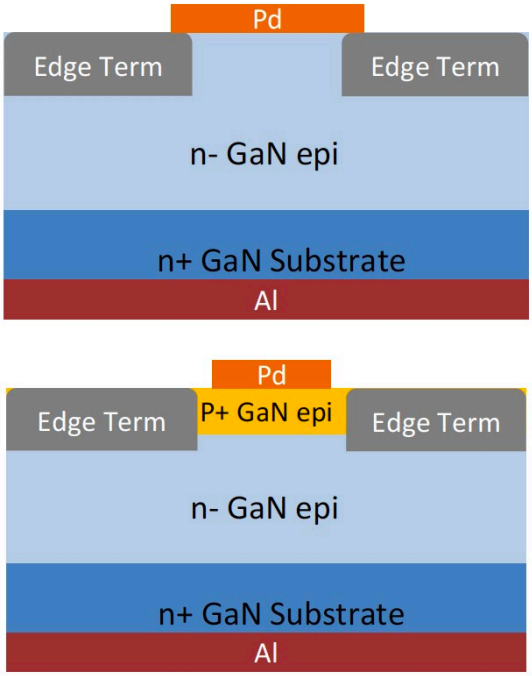


Figure 2. Schematic cross-sections of vertical Schottky (top) and PN (bottom) diodes. Source: [7].

3. Bulk GaN Fabrication

Despite the material advantages of GaN, there are additional technical hurdles that must be overcome to make it viable for commercialized power devices. Unlike Si and SiC which have well established and economic production processes for bulk substrates, GaN has historically lacked a growth process for achieving high-quality bulk native substrates [5]. GaN power devices have been fabricated using non-native substrates, namely Si, SiC, and Sapphire, limiting growth to lateral device structures with thin films of GaN. Furthermore, the processes used to fabricate GaN on non-native materials result in higher defect densities, greater than 10^8 cm^{-2}, making them less effective for power applications [7].

Fabrication of lateral GaN devices on foreign substrates has been effective and is the focus of several research efforts; see [8] through [10]. However, producing low-defect density bulk-GaN is critical to realizing reliable, high-performing vertical power devices. Researchers are actively pursuing methods to achieve affordable, low-defect density bulk-GaN for use in power device fabrication [11]. Ueno et al. was able to fabricate vertical

GaN Schottky barrier diodes with a forward current of 5A and blocking voltage of 600V on a bulk GaN substrate with a dislocation density less than 10^6 cm^{-2}. Additional strides in growth processes have allowed researchers to achieve defect densities below 10^5 cm^{-2} [7].

Nitride-based materials, such as GaN, cannot use traditional crystal growth methods. Epitaxial growth processes are required to fabricate high quality GaN substrates [5]. These methods include high pressure thermodynamic methods such as ammonothermal growth, and chemical reaction-based deposition methods such as liquid phase epitaxy (LPE), hydride vapor phase epitaxy (HVPE), and metalorganic chemical vapor deposition (MOCVD). The most widely used of method is MOCVD.

B. IDEAL THEORY OF SCHOTTKY DIODES

Schottky diodes are a fundamental electronic device. They can be found in electronic circuits as standalone components or as a part of Schottky contacts formed by gate metals of more complex power devices. Schottky diodes also serve as useful research platforms. Electrical characterization of Schottky diodes provide novel information as to the quality and performance characteristics of material substrates and epitaxial layers [3]. Moreover, Schottky diodes fabricated from WBG materials demonstrate desirable properties for applications in high-power electronics.

1. Energy Band Theory

Schottky barrier diodes are rectifying contacts formed at Metal-Semiconductor (MS) junctions. Ideal MS rectifying contacts have three assumed properties. First, the metal and semiconductor are assumed to be in intimate contact, without any additional layers between the two surfaces. Second, interdiffusion between metal and semiconductor has not occurred; Third, there are no surface charges or other surface defects, or impurities, at the MS junction [12]. Finally, the doping level of the semiconductor must be kept sufficiently low as to not allow tunneling current, which generally leads to the formation of ohmic contacts between the metal and the semiconductor.

As with any semiconductor, drawing the energy band diagram is essential to understanding the theory. The band diagrams for an ideal Schottky contact just before and

after equilibrium is reached can be seen in Figure 3. E_c, E_{FS}, E_i, and E_v are the same energies as they would be for the *n*-type material of a PN diode. E_0 is referred to as the vacuum level and is used in determining the work function (Φ) of a material. E_{FM} is the Fermi level of the metal, Φ_M is the metal work function, χ is the electron affinity, and Φ_S is the semiconductor work function.

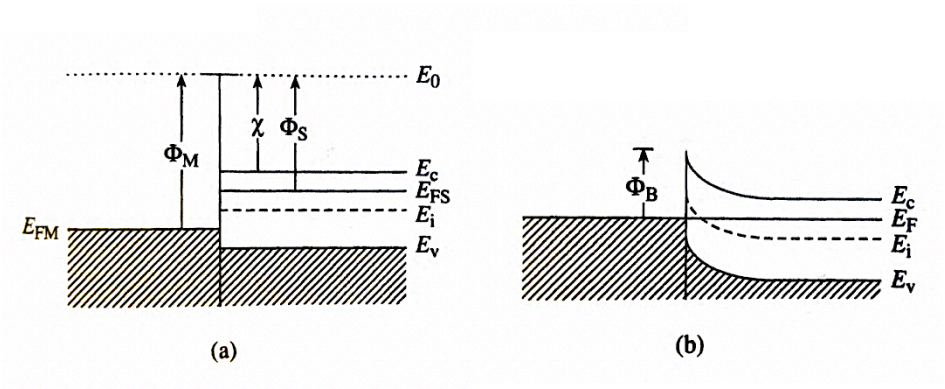
Φ_M is a basic property of the metal, varying from 3.66 eV to 5.15 eV [12]. Likewise, Φ_S is dependent on χ, an inherent property of the semiconductor, and the difference between E_c and E_{FS} under flat band conditions, shown in Figure 3(a).

$$\Phi_S = \chi + (E_c - E_F) \tag{1}$$

Figure 3(b) shows the band diagram of the Schottky contact once equilibrium has been reached. Electrons transfer from the semiconductor to the metal due to the availability of empty states at a lower energy, causing a depletion region and barrier to form until E_{FM} equals E_{FS}. Φ_B is known as the barrier height and for an ideal *n*-type Schottky diode is given by

$$\Phi_B = \Phi_M - \chi, \tag{2}$$

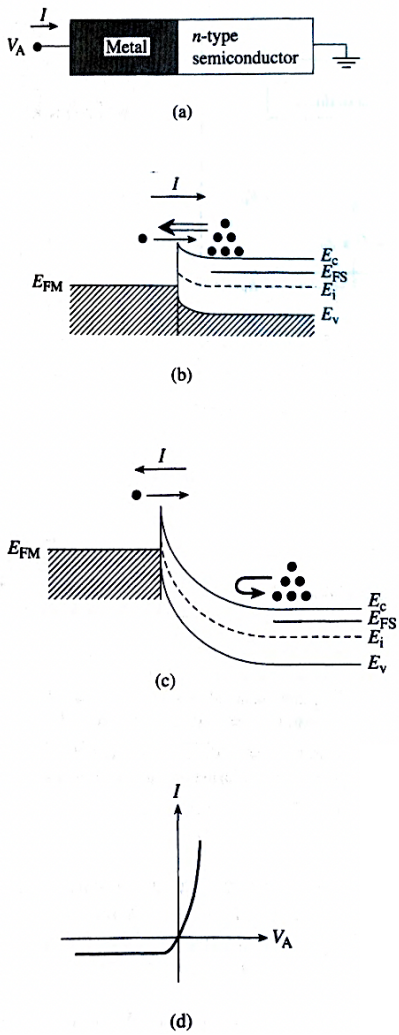
and is often referred to as the Schottky-Mott relationship.



(a) An instant after the contact formation. (b) Under the equilibrium conditions.

Figure 3. Energy band diagram for an ideal Schottky contact between a metal and an n-type semiconductor. Source: [12].

Appling a positive voltage across an *n*-type Schottky diode, based on the polarities described by Figure 4(a), lowers E_{FM} in relation to E_{FS}, reducing the perceived barrier. Electrons in the semiconductor will eventually flow exponentially over the barrier to the metal, forward biasing the device, as shown in Figure 4(b). If the polarity of the applied voltage is reversed then E_{FM} will raise above E_{FS}, increasing the perceived barrier to electrons in the semiconductor and blocking them from flowing into the metal as shown in Figure 4(c). In either case, the perceived barrier from the metal into the semiconductor remains the same and a constant, yet small, amount of leakage current flows into the semiconductor. Figure 4(d) shows the rectifying properties of the current-voltage (I-V) relationship for an ideal n-type Schottky diode [12].



(a) Definition of current and voltage polarities. (b) Energy band diagram and carrier activity when $V_A > 0$. (c) Energy band diagram and carrier activity when $V_A < 0$. (d) Deduced general form of I-V characteristics.

Figure 4. Response of the (n-type) MS contact to an applied DC bias. Source: [12].

2. Electrostatic Characteristics

As with the band theory, the electrostatics of a Schottky diode are comparable to many concepts derived from PN diodes [12]. For this analysis, doping levels, N_D, are assumed to be uniform through the device. Schottky diodes have a built-in voltage potential, V_{bi}, as described by

$$V_{bi} = \frac{1}{q}\left[\Phi_B - (E_c - E_F)\right]. \tag{3}$$

where q is the charge of an electron and is shown by Figure 5(a).

A depletion region forms at the MS interface and extends into the semiconductor until charge distribution becomes neutral again. In a PN diode, the depletion region extends into the *n*-side and *p*-side of the device, effectively neutralizing the effective charge polarity seen across the region by the opposing polarity. However, a Schottky diode does not have a p-side to balance out the effective charge build-up on the n-side. As a result, excess negative charge builds up on the metal side of the MS interface, provided by the free electrons in the metal [12]. Charge density, ρ, can be described as a δ-function at the interface with a constant distribution into the semiconductor for the width, W, of the depletion region and is shown in Figure 5(b).

$$\rho = \begin{cases} N_D, 0 \le x_n \le W \\ 0, x_n > W \end{cases} \tag{4}$$

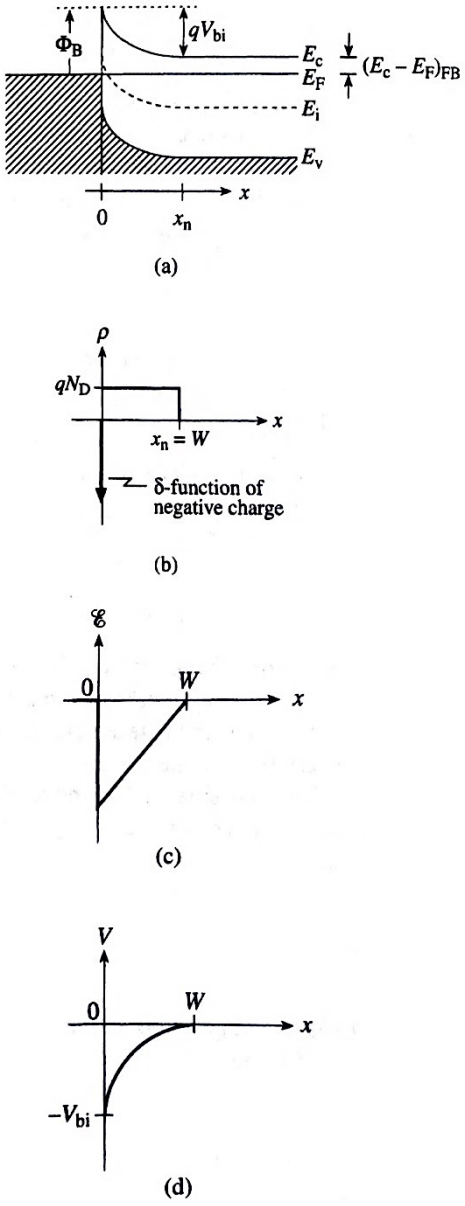
Using Poisson one-dimensional equation and solving Equation (4) for electric field yields the following solution:

$$\mathcal{E}(x) = -\frac{qN_D}{K_S\varepsilon_0}, 0 \le x_n \le W \tag{5}$$

which is graphically represented in in Figure 5(c). K_S is the dielectric constant of a material, 8.9 for GaN, and ε_0 is the vacuum permittivity. Knowing that the electric field is equal to the voltage potential divided by a known distance, the electrostatic potential is determined to be

$$V(x) = -\frac{qN_D}{2K_S\varepsilon_0}(W - x)^2, 0 \le x_n \le W. \tag{6}$$

Figure 5(d) shows the electrostatic potential.



(a) Band diagram at equilibrium. (b) Charge density at equilibrium. (c) Electric field at equilibrium. (d) Electrostatic potential as a function of position at equilibrium.

Figure 5. Electrostatic variables in an MS (*n*-type) diode under equilibrium conditions. Source: [12].

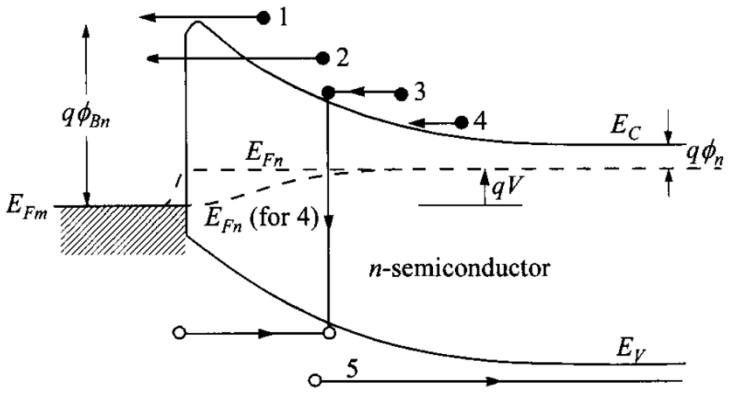
Finally, the depletion width can be deduced by solving the electrostatic potential at x equals to zero, yielding a solution identical to that of a p+-n junction [12].

$$W = \left[\frac{2K_S\varepsilon_0}{qN_D}(V_{bi} - V_A)\right]^{\frac{1}{2}} \tag{7}$$

3. Current Transport Process

The current transport processes within a Schottky diode are where the theory diverges from that of a PN diode. PN diodes are commonly referred to as minority carrier devices since the dominant current component under forward bias comes from the recombination of minority carriers in the depletion region. Schottky diodes, on the other hand, are considered to be majority carrier devices [12]. The dominant component of current transport for a high mobility *n*-type Schottky diode is due to thermionic emission [13].

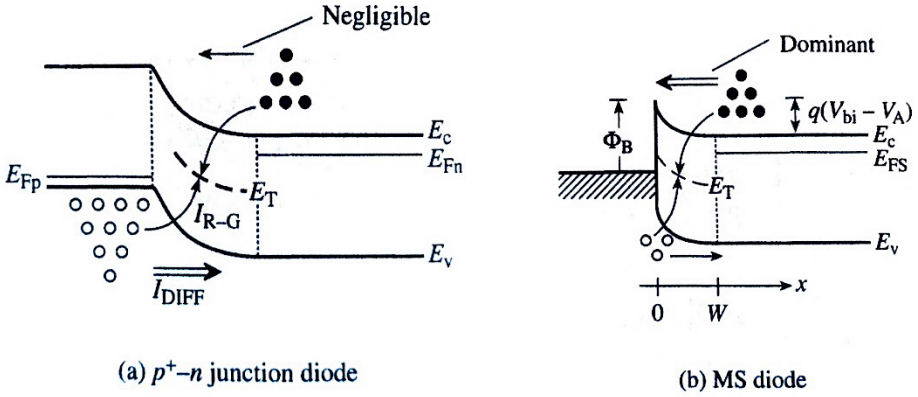
There are five independent mechanisms of current transport within a Schottky diode [13]. Minority carrier current transport processes within the depletion region, such as recombination-generation (R-G) and minority carrier injection still occur in a Schottky diode. Electrons can tunnel through the Schottky barrier and diffuse from the semiconductor into the metal. However, by time additional current transport processes become relevant, tunneling current adds such a small amount to the total current that it is generally considered negligible in Schottky diodes used for rectification purposes [12]. Figure 6 shows the five separate mechanisms of current transport in a Schottky diode.



Mechanisms of current transport are (1) thermionic emission, (2) quantum-mechanical tunneling, (3) recombination-generation, (4) carrier diffusion from the semiconductor to the metal, and (5) minority carrier injection.

Figure 6. Five observed current transport processes for a *n*-type Schottky diode. Source: [13]

Figure 7 shows the differences between the current transport processes of a PN diode and a Schottky diode, to include the negligible and dominant current components under forward bias.



(a) Current transport process of a p^+-n junction diode. (b) Current transport process of a MS (n-type) diode.

Figure 7. Negligible and dominant current components in forward biased. Source: [12].

If an electron traveling towards the surface of the MS interface has a high enough velocity, then it will be capable of overcoming the potential barrier. Assuming there are a certain number of electrons, each with a velocity great enough to surmount the barrier, then the total current can be derived for the group of electrons by summing the contribution from each electron [12]. Thermionic emission is considered a ballistic transport process for these reasons. It can easily be shown that the equation describing thermionic emission for an ideal Schottky diode is

$$I = I_{sat}\left(e^{\left(\frac{qV_A}{\eta kT}\right)} - 1\right), \tag{8}$$

and the saturation current component is given by

$$I_{sat} = AA^*T^2e^{\left(-\frac{q\Phi_B}{kT}\right)}. \tag{9}$$

A is the area of the diode, η is ideality factor, k is Boltzmann constant, q is the charge of an electron, V_A is the applied bias voltage, and T is the temperature. The ideality factor is assumed equal to one for the ideal theory. A^* is known as the Richardson constant and determined by

$$A^* = \frac{4\pi q m^* k^2}{h^3} \tag{10}$$

where m^* is the effective mass of an electron and h is Plank constant.

4. I-V and I-V-T Relationships

A distinct relationship between current and voltage is formed by Equations (8) and (9). A semi-logarithmic plot of theoretical and experimental I-V data for an example *n*-type GaN Schottky diode is shown in Figure 8. The plot can be divided into three separate regions [4]. Region I shows how the additional current components and other non-ideal factors add to the predicted current level as determined by thermionic emission alone. Region II shows the relationship once thermionic emission takes over as the dominant current component. Region III shows the limiting effects of series on-state resistance, lowering the expected current level.

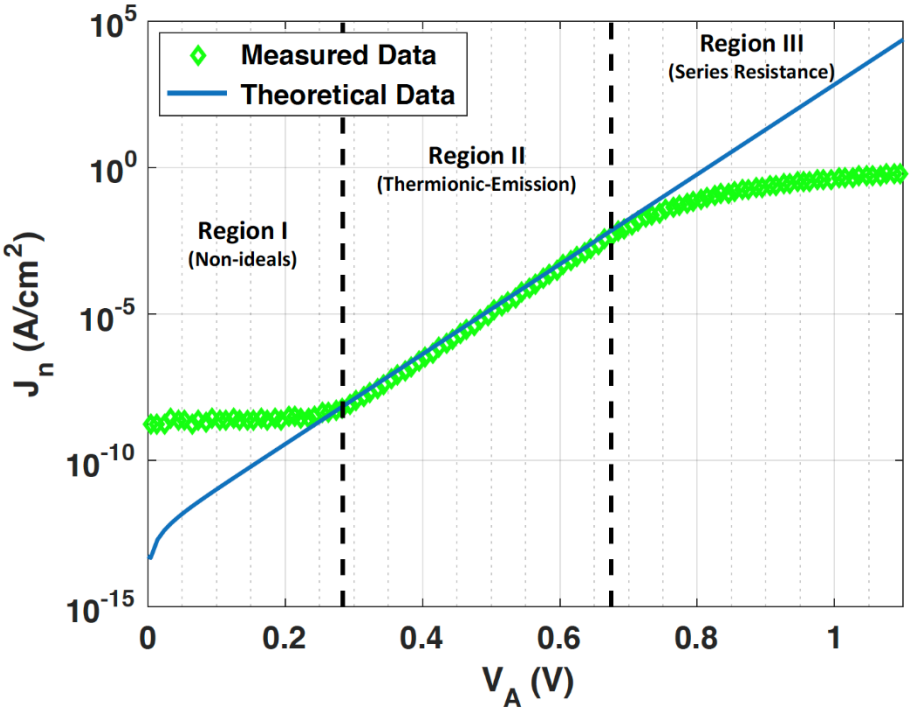


Figure 8. Theoretical and experimental semi-logarithmic I-V plot for an example *n*-type GaN Schottky diode. Source: [4].

A linear fit can be obtained by taking the natural logarithm of Equation (8) and applying it to region II.

$$ln(I) = ln(I_{sat}) + \frac{q}{\eta kT} V_A \tag{11}$$

The y-intercept of Equation (11) yields the I_{sat} and the ideality factor can be determined from the slope of the linear fit. Once the saturation current is determined, the barrier height can be determined by taking the natural logarithm of Equation (9) and solving for Φ_B.

$$\Phi_B = \frac{kT}{q} ln\left(\frac{AA^*T^2}{I_{sat}}\right) \tag{12}$$

Accurately determining the Richardson constant is critical to determining the correct barrier height of a Schottky diode. While the ideal Richardson constant is solely a function of the electron effective mass in the bulk of the semiconductor, measuring the

actual value of A^* can be difficult since it is highly dependent on individual MS contacts and depends on several factors, such as annealing temperatures, fabrication and metallization processes, and surface cleaning [14]. Researchers have shown small variations, less than 0.026 eV, from derived values for barrier height, even for large errors, up to a few orders of magnitude, in A^*, but a more accurate method for solving barrier exists using the temperature dependency of the I-V relationship. A^* can be determined for an individual Schottky contact from experimental data and solved independent of surface variations through I-V-T measurements. This method is known as the activation-energy analysis and involves determining I_{sat} at each temperature across a range [14].

An activation-energy analysis of the saturation current produces what is known as a Richardson plot and enables Φ_B, η, and A^* graphically determined. The Richardson plot is generated by plotting each calculated saturation current divided by temperature squared versus q/kT. Figure 9 shows an example of Richardson plot for a *n*-type GaN Schottky diode.

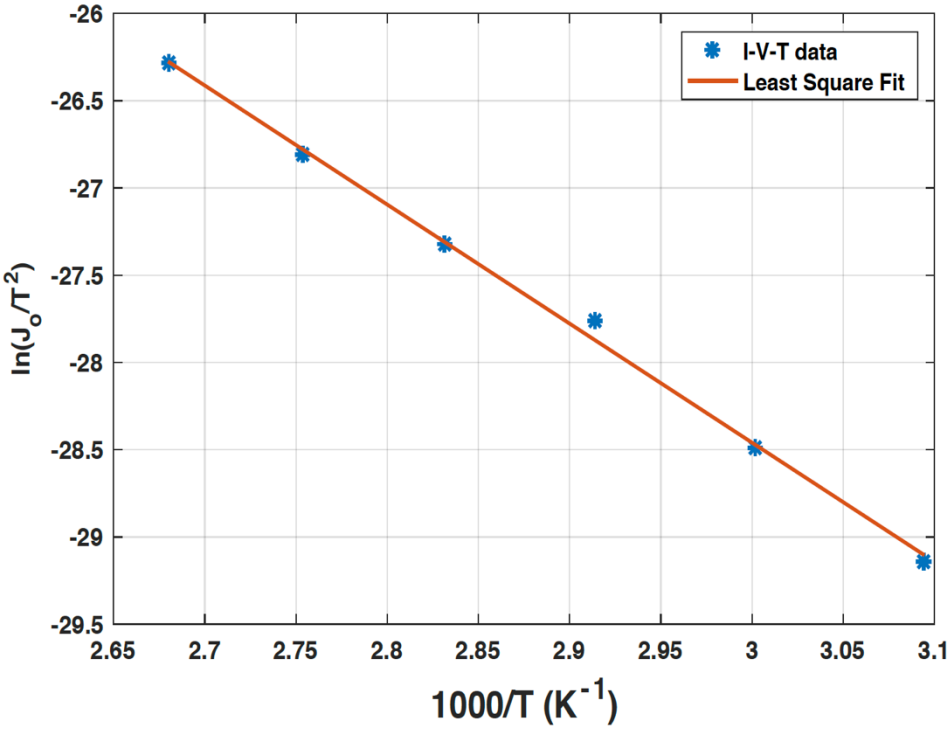


Figure 9. Richardson plot for a *n*-type GaN Schottky diode. Source: [4].

The Richardson constant and barrier height can be extracted from taking the natural logarithm of Equation (9) and using a linear fit. The example shown in Figure 9 uses a least-squares fit.

$$ln\left(\frac{I_{sat}}{AT^2}\right) = ln(A^*) - \frac{q\Phi_B}{kT} \tag{13}$$

A^* is determined from the y-intercept of the Richardson plot and Φ_B is solved from the slope of the linear fit.

C. NON-IDEAL THEORY OF SCHOTTKY DIODES

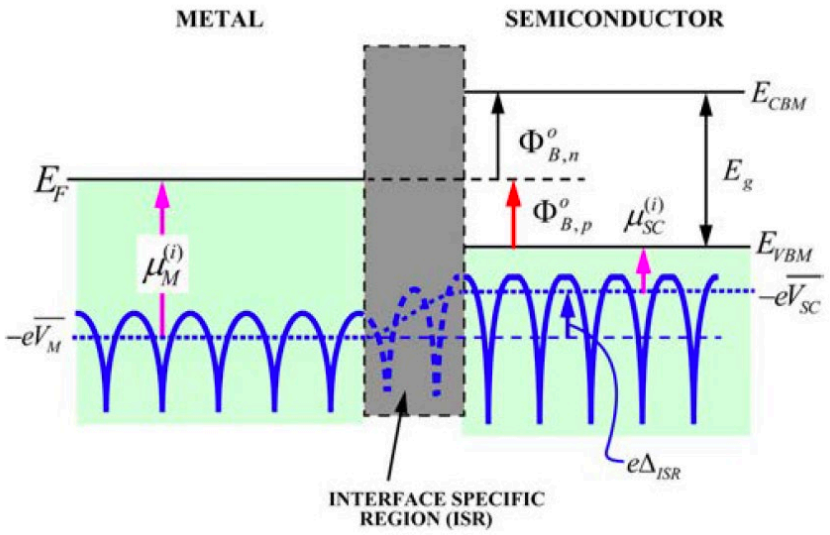
The ideal theory of a Schottky diode made several assumptions regarding the MS interface which made solving electrical processes and visualizing the energy band diagrams easier. The theory assumed a homogenous barrier with no physical or chemical interactions between the metal and semiconductor at the MS interface. However, experimentally measured values of the Schottky barrier height (SBH), as described by Equation (2), the current, as described by Equations (8) and (9), and ideality factor show a deviation from the Schottky-Mott model [14]. Experimental observations also show a non-linear relationship in I-V curves when the current is plotted on a logarithmic scale at the voltage ranges where the thermionic emission current should dominate.

Tung [14] determined that experimentally measured values of the SBH often described the average barrier height, vice the true SBH. His analysis of the SBH and use of the idea of barrier height inhomogeneity (BHI) also accounted for other experimentally observed phenomena which deviate from ideal theory. These phenomena include leakages and edge-related currents, greater-than-unity ideality factors, T_0 anomaly, temperature dependence of the ideality factor, and "soft" reverse characteristics [15].

1. Formation of the Schottky Barrier

The Schottky barrier that is formed from an MS interface is a critical component in determining the operating characteristics of a device. The SBH dictates many of the electrical properties for current transport across the device [14]. The ideal theory assumes a uniform distribution of states with an average electrostatic potential, yet there are innate

discontinuities between the electronic energy states at the MS interface which lead to non-linear I-V characteristics. Figure 10 shows the difference between the described electrostatic distribution.



Curved solid lines indicate the electrostatic potential energy. Dotted lines indicate average electrostatic potential.

Figure 10. Energy Band diagram at a MS interface. Source: [14].

The underlying physics behind the formation of Schottky barriers has been an unsettled topic of interest among researchers for decades and has been determined to be a complicated function of surface conditions, metal type, and variation due to differing chemical surface preparations used to fabricate Schottky diodes [15]. Atomic-level interactions between at the MS interface was the focus of early research. The concept of Fermi-level (FL) pinning was suggested as the main cause deviation from ideality and gave rise to interface specific region (ISR) models.

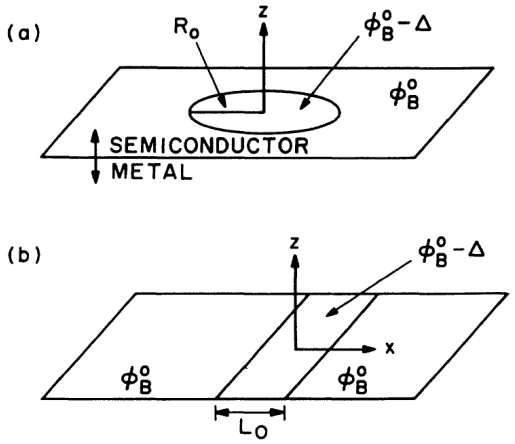
Two widely and historically used ISR models include the Bardeen model and the metal-induced gap states (MIGS) model. The Bardeen model explains FL pinning through the formation of a dielectric layer at the semi-conductor surface [16]. The dielectric layer is formed from the inherent space charge region of the Schottky diode and by a build-up

of electrons at the surface states, assuming the density of states is high enough. Once the MS interface is formed, the surface states charge causes a pinning effect on the FL, causing an energy-level independent of the work function. The MIGS model is based on the ideas that gap states, due to defects or foreign contaminant atoms, exist at the MS interface causing electronic states to exist within the energy band gap and similarly pinning the FL [4]. Both models to provide a qualitative means to analysis FL pinning of the Schottky barrier, but fail to explain the magnitude of deviation of the measured SBH and the physics at the atomic level within the ISR.

2. SBH Inhomogeneity and Potential Distribution

A more accurate and modern ISR model is the Equilibrium of Electrochemical Potential (EECP) model, proposed by Tung [17]. The EECP model explained observations of FL pinning due to polarization of interfacial chemical bonds between metal and semiconductor atoms, vice surface states or MIGS. Furthermore, his model provided an explanation for the Schottky BHI, since a change in chemical bonds across the MS interface from crystalline mismatches or other defects results in localized variations of the SBH [4].

Since the SBH will vary locally along the MS interface, the potential distribution can be approximated using a dipole-layer approach. Each potential variation across the layer of dipoles is treated as a perturbation in the analysis of the MS interface [15]. The most relevant form of SBH inhomogeneity to this research is that of a small region of low SBH surrounded by region of high SBH. The area of high SBH is assumed to be relatively uniform in comparison to the low SBH region. The low SBH region is modeled by either a small circular patch or a narrow semi-infinite linear strip, as shown by Figure 11.



(a) Potential distribution of a circular path. (b) Potential distribution of a narrow strip.

Figure 11. Example geometries used for potential distribution analysis. Source: [15].

It is important to note that the size of the low SBH patch affects the potential pinch-off within that region and has a significant impact on the transport properties of the MS interface. Potential pinch-off occurs because of the surrounding area of high SBH on the low-SBH region and is more easily achieved if patch is smaller in radius, or the strip is narrower. Figure 12 shows the effect of the size of the radius of a small circular patch under forward and reverse potential bias.

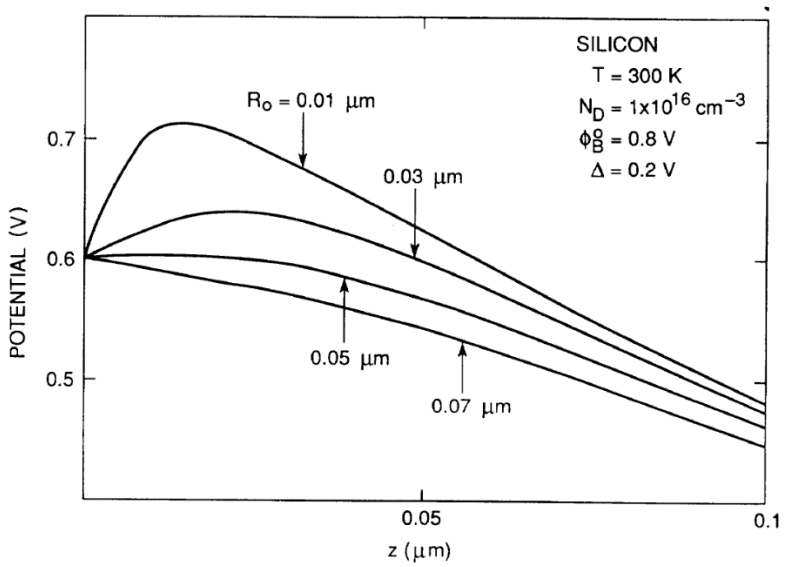


Figure 12. The effects of radius of low SBH patch on potential pinch-off. Source: [15].

The pinch-off creates a saddle point that and can be effectively represented by a point-dipole approximation. This phenomenon can be seen in Figure 13, which shows the horizontal cross-section of a three-dimensional potential difference along a narrow strip placed along the x = 0 axis and the potential well that develops around the low SBH strip and the surrounding high SBH region [15]. Essentially, the two-dimensional effect of the potential pinch-off in the low barrier height region is to make the effective barrier height for carriers traveling through the low SBH patch dependent upon the bias applied to the contact.

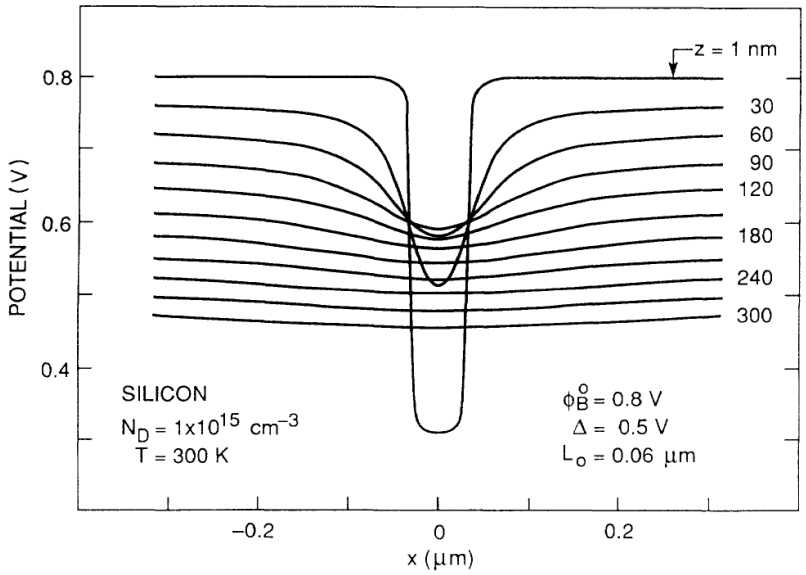


Figure 13. Potential distribution surrounding a narrow low SBH strip. Source: [15].

A detailed analysis of the potential distribution and the dipole-layer and point-dipole approximations is provided by Tung in [15].

3. Electron Transport

Once the electric potential surrounding the saddle point is determined, the current flowing through the region can be determined through some further analysis and modifications to the thermionic emission equation, Equation (8). Tung [15] goes through an in-depth analysis starting with an isolated region with low SBH then a Schottky barrier containing many low SBH regions, with a sharp distribution and with a broad distribution. From Tung analysis, the total current through the Schottky barrier with a sharp distribution is given by

$$I_{total} = AA^*T^2 e^{(-\beta\Phi_B^0)}\left(e^{(\beta V_a)} - 1\right) \times \left(1 + \frac{4c_1\pi\eta^{\frac{2}{3}}\gamma_0}{9\beta V_{bb}^{\frac{2}{3}}} e^{\left(\frac{\beta\gamma_0 V_{bb}^{\frac{1}{3}}}{\eta^{\frac{1}{3}}}\right)}\right), \qquad (14)$$

where β = 1/kT, c_1 is the total density of patches, and V_{bb} is the band bending at the MS junction, assuming a uniform SBH, Φ_B^0. The parameters η and γ will be defined later in this section. Using a more generalized statistical distribution of inhomogeneity, Equation (14) can be rewritten as

$$I_{total} = AA^*T^2e^{(-\beta\Phi_B^0)}\left(e^{(\beta V_a)} - 1\right) \times \left(1 + f(V_{bb})e^{\left(\beta^2\kappa V_{bb}^{\xi}\right)}\right). \quad (15)$$

A subsequent and more detailed explanation about the statistical analysis used and how Equation 15 is derived will be provided towards the end of this section.

The total current flowing through the Schottky diode is essentially made up of two distinct current components [15]. The first is the average current across the entire surface based on the uniform "high" barrier height, Φ_B^0. The second is the added current flowing through the low-SBH regions. The effective barrier height of the Schottky diode for this component is

$$\Phi_{eff} = \Phi_B^0 - \beta\kappa V_{bb}^{\xi}. \quad (16)$$

The effective SBH is a temperature dependent term despite the fact electrostatic barrier height of regions of low SBH are effectively independent of temperature [15]. The dependence upon temperature arises from the averaging of thermionic emissions across an inhomogeneous surface. Since Φ_B^0 is temperature dependent then I_{total} must also depend on temperature. Another noteworthy temperature dependence caused by BHI is that of the ideality factor, leading to greater-than-unity values. The ideality factor has dependence on temperature and voltage and can be approximated as

$$\eta_{tot} \approx 1 + \xi\beta\kappa V_{bb}^{\xi-1}. \quad (17)$$

The temperature dependence of the ideality factor has been observed experimentally across a variety of MS junctions and no one theory could properly account for the variance, commonly referred to as the "T_0 anomaly" [15]. It is shown to be present in any diode if the junction current can be written in the following form,

$$I_{total} = AA^*T^2e^{\left(-\frac{q\Phi_B^0}{k_B(T+T_0)}\right)}\left(e^{\left(\frac{qV_a}{k_B(T+T_0)}\right)} - 1\right). \quad (18)$$

Historically, the T_0 effect had been attributed to an exponential distribution of the density of interface states within an interface layer; however, the measured variation across similar devices was too great to be explained by this theory. BHI provides a better explanation of the dependence on temperature and is more consistent with observed results [15]. Two general observations can be made as the temperature is lowered across an inhomogeneous SBH. First, the ideality factor increases as the bias is increased and, second, as temperature is lowered for a device with low SBH regions, the measured junction current is dominated by regions of low SBH and therefore yields a higher ideality factor. Figure 14 shows these observations for a Silicon Schottky diode.

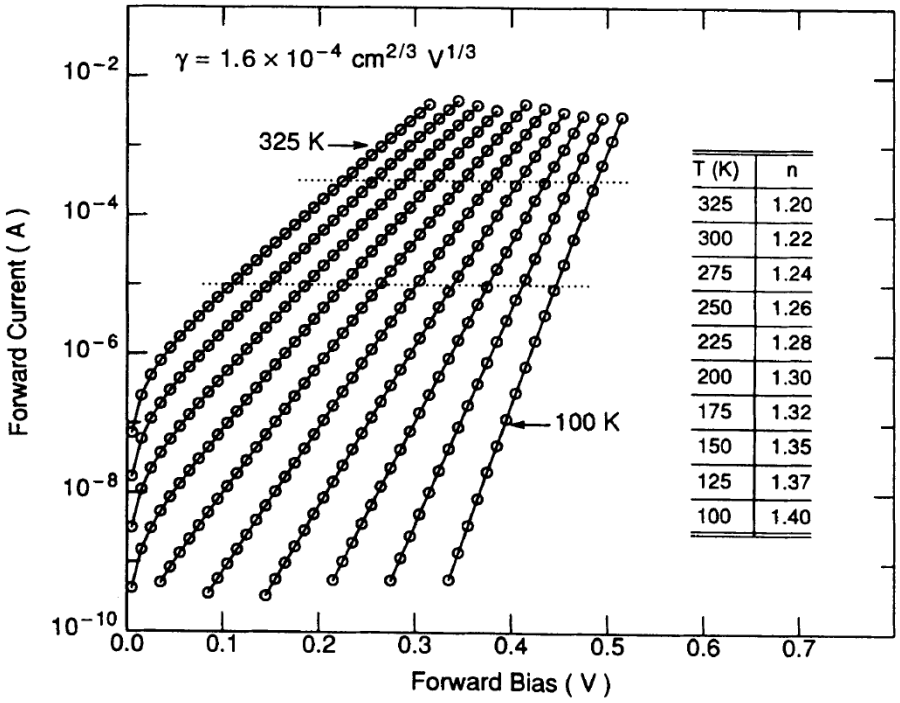


Figure 14. I-V traces of Si Schottky barrier at varying temperatures. Source: [15].

Tung analysis of BHI provides a set of topology specific parameters for a patch, and strip, and assumes a positive half-Gaussian statistical distribution of patch sizes, or

strips, with the mean of the distribution set to zero [15]. The regional density of patches is shown as N(γ)dγ and uses the random patch parameter γ between γ and γ + dγ.

$$N(\gamma) = \frac{\sqrt{2}c_1}{\sqrt{\pi}\sigma_1} e^{\left(-\frac{\gamma^2}{2\sigma_1^2}\right)}, \gamma > 0,$$
$$N(\gamma) = 0, \qquad \gamma < 0. \tag{19}$$

Figure 15 shows a generic example of a half-Gaussian distribution with varying values of sigma, σ, to better illustrate the concept described in Equation (19).

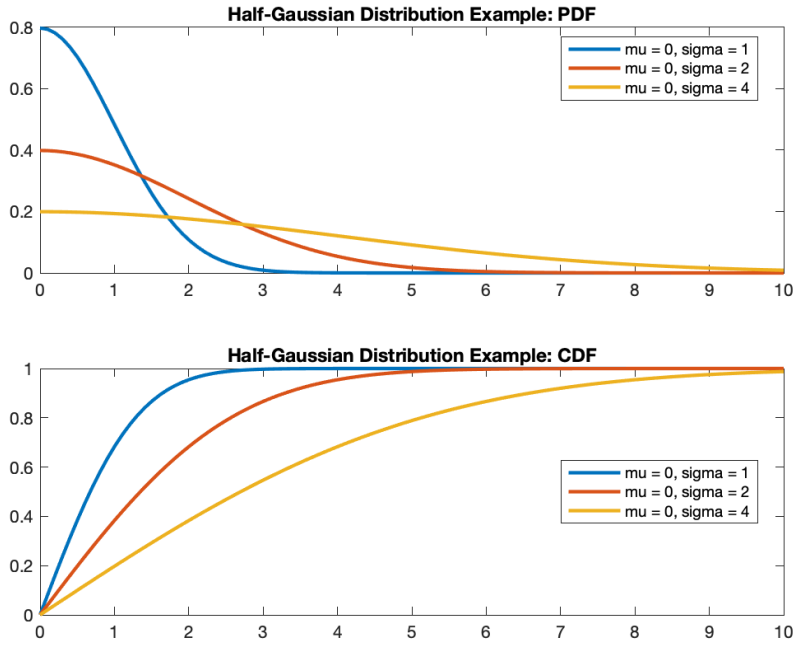


Figure 15. Half-Gaussian distribution example.

Assuming low SBH patches are spatially separated enough to not interact with each other, the total current at a given bias can be solved by applying the half-Gaussian distribution described in Equation (19) and integrating over all patches:

$$I_{total} = AA^{*}T^{2}e^{(-\beta\Phi_B^0)}\left(e^{(\beta V_a)} - 1\right) \times$$
$$\left\{\frac{4\sigma_1^2 C_1 \pi \eta^{\frac{1}{3}}}{9V_{bb}^{\frac{1}{3}}} e^{\left(\frac{\beta^2\sigma_1^2 V_{bb}^{\frac{2}{3}}}{2\eta^{\frac{1}{3}}}\right)} \times \left(1 + erf\left(\frac{\beta\sigma V_{bb}^{\frac{1}{3}}}{\sqrt{2}\eta^{\frac{1}{3}}}\right)\right) + 1\right\}. \quad (20)$$

The error function from Equation (20) can be reduced to equal 1 under typical environmental conditions, temperature, doping levels, and other material properties. In doing so, Equation (20) simplifies to equal Equation (15) as presented earlier in this section.

Tung electron transport parameters include two critical metrics which to describe the inhomogeneity of a Schottky contact. The first is the integrated spatial concentration of the patches or strips which the distribution is normalized to, represented as c_1 for circular patches and c_2 for strips, and given in units of cm^{-2}. The second is the measure of the statistical standard deviation, or spread, of inhomogeneity through the Schottky contact, denoted σ_1 for patches and σ_2 for strips. It is based on the random patch parameter, γ, which is a combination of physical properties of the patch to include size, as well as material characteristics such as the dielectric constant and doping level. Due to the units of the variables chosen for the distributions, the units of the standard deviation are given as $cm^{-2/3}eV^{-2}$. Table 2 shows Tung parameters for electron transport.

Table 2. Parameters for electron transport at an inhomogeneous Schottky barrier. Source: [15]

Parameter	Patch	Strip
ξ	2/3	1/2
κ	$\frac{\sigma_1^2}{2\eta^{2/3}}$	$\frac{\sigma_2^2}{2\eta^{1/2}}$
$f(\beta,V_{bb})$	$\frac{8c_1\sigma_1^2\pi\eta^{1/3}}{9V_{bb}^{1/3}}$	$\frac{c_2\pi\sigma_2^{3/2}\sqrt{\beta}\eta^{1/8}L_{strip}}{1.46V_{bb}^{1/8}}$

It is important to note that although the parameters for patches and strips are different, the total junction current for each case yields the same expression as shown by Equation (15). The constant values for ξ and κ and the function $f(\beta, V_{bb})$ are used for their respective patch parameters to solve for the total current.

BHI provides a useful understanding the physics taking place at an MS junction and more accurately describes the physics of electron transport through an inhomogeneous Schottky contact. It gives rise to one of the critical problems for power electronics through a phenomenon known as current crowding. Due to inhomogeneity of the Schottky contact, current tends to flood the areas of low SBH, limiting current in the device while simultaneously increasing the series resistance [15]. Higher series resistance drives up power consumption and higher device temperatures, negatively impacting the reliability of power devices.

D. GaN RELIABILITY RESEARCH

The study of GaN-based device structures has continued to gain popularity amongst researchers since the early 1980s. In 1983, Kahn et al. [18] examined the electrical and material properties of GaN. It was shown that GaN has a higher electron mobility and higher electric breakdown voltage than both Si and SiC. There results validated the theoretical advantages that GaN could have over Si and SiC for uses in power electronic applications.

As fabrication methods have improved, the theoretical expectations of the performance of GaN-based began to be realized, specifically for lateral RF devices. However, most reliability studies involving GaN have still concentrated on lateral devices, specifically high electron mobility transistors (HEMTS). Research concerning vertical GaN structures have targeted PN diodes and heterostructure field effect transistors (HFETs) [5]. Schottky GaN Schottky diodes are of particular interest for power electronics because their on-state voltage is approximately 3 times smaller than that of a GaN PN diode, resulting in significantly lower conduction losses.

1. Reliability Research Involving GaN Schottky Diodes

In 2001, Chen et al. [19] conducted a thermal stability study of Ni/Ta n-GaN Schottky contacts and observed the effects through electrical measurements. I-V measurements were taken after a variety of thermal annealing conditions were applied to the diodes. There experiment varied in annealing time from five minutes up to one hour and temperatures ranging from 300 ℃ up to 800 ℃. The team found that after one hour of annealing at 700 ℃, that a high quality Schottky diode with an ideality factor of 1.16 and a barrier height of 1.24 eV could be attained.

In 2008, Parish et al. [20] measured the forward bias I-V characteristics of n-GaN Schottky diodes over a large temperature range from 70 to 400 K . Their observations of the I-V curves showed a two-step kink on the semi-logarithmic plots, or double-diode type behavior. In their analysis the team used a model of two discrete diodes in parallel to fit the curves, each with a distinct SBH. They found one such barrier to correlate to the results expected for an ideal diode, matching Capacitance-Voltage (C-V) measurements and flatband I-V measurements, while the other exhibited a reduced SBH with temperature dependence.

In 2013, J. Shin et al. [21] investigated the barrier height inhomogeneity (BHI) of the gate metal for AlGaN/GaN Schottky diodes. Their analysis included electro-reflectance spectroscopy and X-ray photoelectron spectroscopy measurement for different types of Schottky gate metals, including Au, Pt, Pd, and Ni, and concluded the BHI on the gate metal depends on the type of Schottky gate metals used.

In 2016, R. P. Tompkins et al. [22] conducted I-V measurements on GaN power Schottky diodes and presented data on device characteristics including the breakdown voltage, V_b, specific on-resistance, $R_{on\text{-}sp}$, ideality factor, n, and barrier height, Φ_b. They also conducted I-V-T measurements, assessing properties as a function of temperature from 25 to 250 °C in increments of 25 °C.

2. HTOL Stress Testing Involving Commercial GaN Devices

HTOL testing has been critical to GaN research in evaluating its reliability. HTOL testing used for ALT, projecting the lifetime of commercial grade devices. Most recent studies involving GaN Schottky diodes have been conducted on experimental Schottky contacts, not fully packaged devices. Although this is useful for understanding how GaN Schottky contacts perform, it is not indicative of how a packaged device will perform. The process of packaging devices adds more variables that may impact the overall functionality and reliability of the device. However, in 2014, Wu et al. [23] conducted a series of high temperature DC stress tests on 600V GaN power switches, HEMTs, fabricated on Si.

In 2015, their work was continued by Kikkawa et al. [24] using devices that were fully packaged in TO-220 style casings which was unlike many research grade devices manufactured on bare contacts or with open cavities. High temperature reverse bias (HTRB), highly accelerated temperature and humidity stress test (HAST), temperature cycling (T/C), power cycling (P/C), and high temperature storage life (HTSL) were among the types of stress tests conducted. The team found that the TO-220 casings were suitable for high-speed application and no failures were found during the HTOL stress tests. Their research concluded that the tested devices were ready for commercialization and use in industrial power applications. The use of the tested devices would greatly reduce switching losses and overall system size when compared to traditional semiconductor devices [24].

III. EXPERIMENTAL STRESS TEST SYSTEM DESIGN

The design for the experimental stress testing system is introduced in this chapter. The first section is an overview of the HTOL stress testing system constructed for conducting electrical stress measurements. The second section discusses the construction of the system, focusing on the customized designs that enabled the stress testing methodology to be implemented. The third section presents temperature tuning and performance characteristics of the system. Finally, a brief summary of complete system functionality and challenges is provided in the fourth section.

A. HTOL SYSTEM OVERVIEW

The HTOL stress testing system was designed to conduct the required stress-measure-stress experiments over the course of several hours, with the possibility of running for multiple days. The design was loosely based on available commercial HTOL and ALT systems.

Modular, rack-mounted hardware and a robust software-controlled automated test structure were the key aspects to achieve this objective. Additional design aspects included: a simple user interface, responsive temperature and humidity control, and user display with near real-time data for system performance and device measurements.

Rack-mounted modules allowed the system to remain self-contained, streamlined and enabled efficient system operations. Changing the devices under test (DUT) was simple since individual modules could be easily removed from their rack and taken to an open area within the laboratory for removal and replacement. Troubleshooting or repairing module faults proved just as quick for the same reasons and if long term repairs were needed stress testing was unhindered since the system software was designed to handle one to five total test modules. However, based on available components, the system was initially designed and built with three individual test modules.

Multiple subsystems needed to be synchronized with one another and simultaneously adjusted throughout hours of testing to take exact measurements. It was not feasible for a person to manually have the desired level of precision to control the system.

Furthermore, human control would have injected more error into the testing process, making repeatable time-stamped testing unfeasible. Robust software control and automation was necessary to make the HTOL system practical for the desired stress-measure-stress testing.

Figure 16 and Figure 17 show the block diagram of the of the final system design and the assembled HTOL system, respectively.

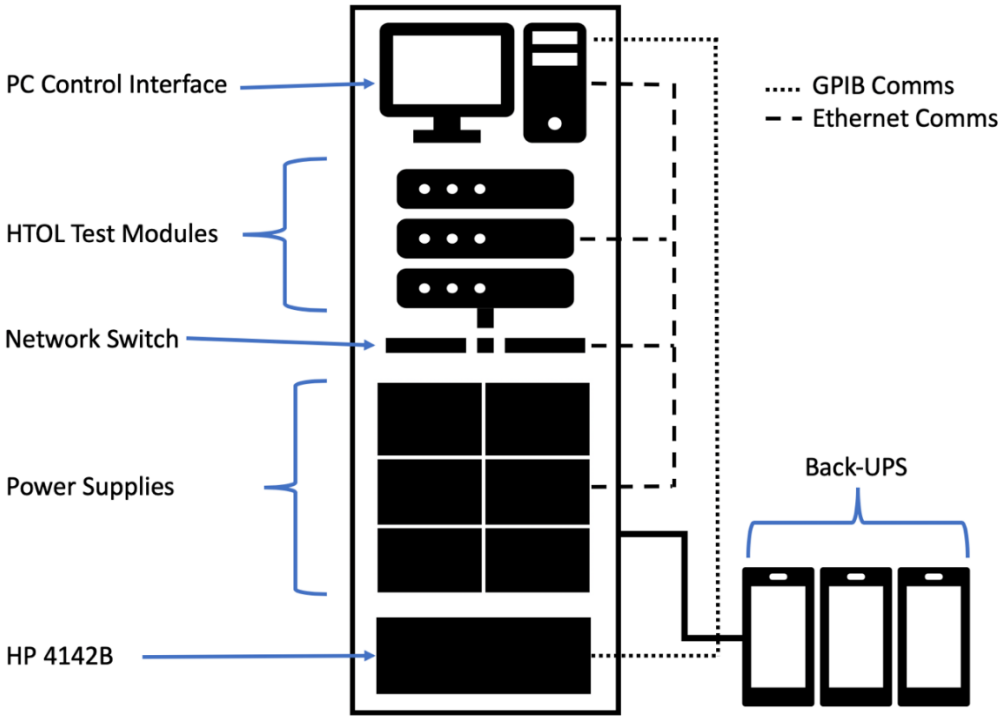


Figure 16. Block diagram of HTOL system with instrument control and communication paths.

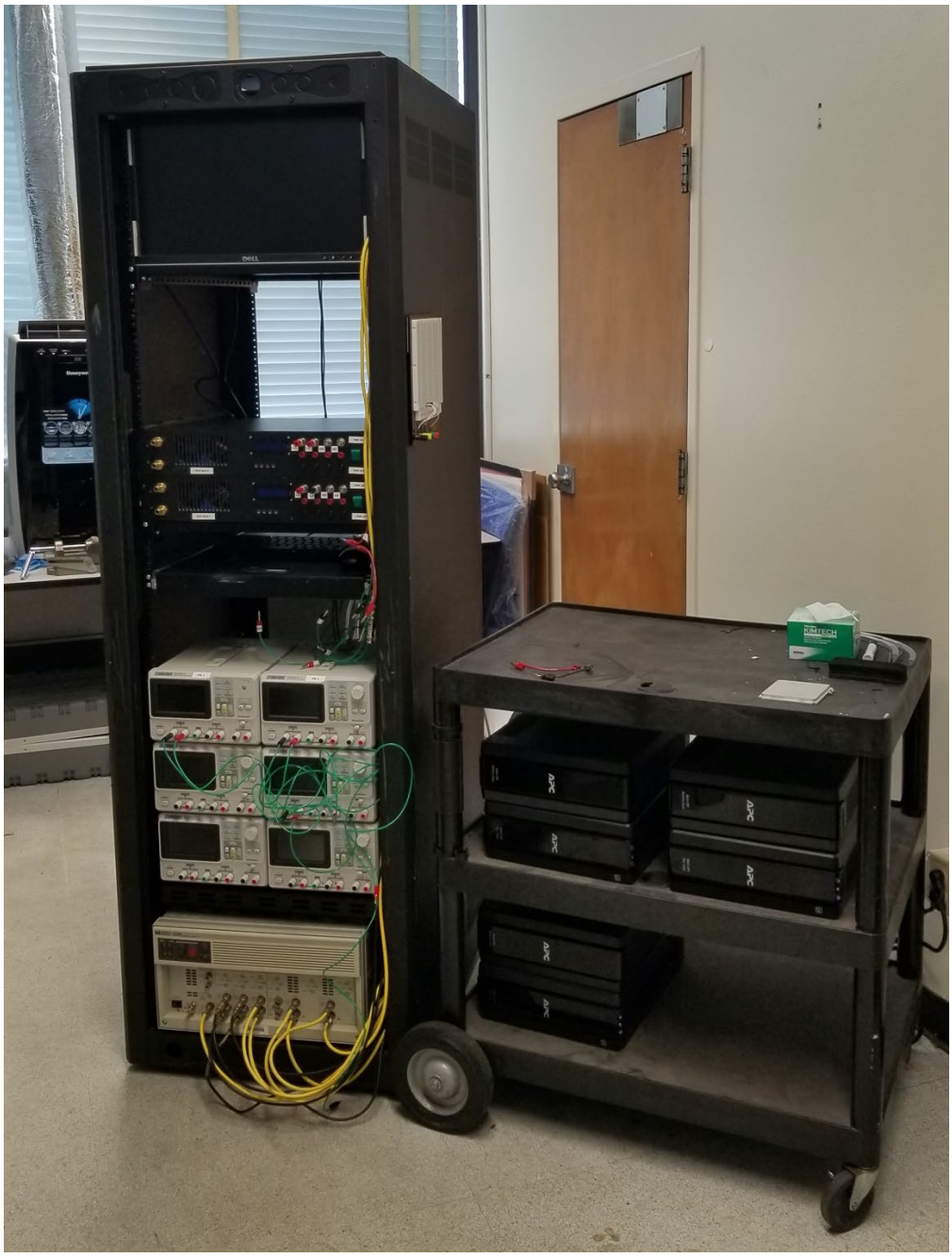


Figure 17. Image of constructed HTOL system with two stress test modules.

B. HTOL SYSTEM CRITICAL DESIGN ASPECTS

The HTOL stress testing system was designed to conduct DC stress-measure-stress measurements. It was constructed using many sub-systems, each with important hardware and software mechanisms. The primary commercial sub-systems utilized were the personal

computer (PC), Netgear 24-port gigabit switch, HP4142B DC Source/Monitor, Siglent programmable DC power supplies, and APC back-UPS. The PC was used as the primary means of system control and is where all data measurements were saved. The Netgear switch connected the communication paths of all sub-systems apart from the HP4142B, which used GPIB, as shown in Figure 16. The HP4142B was the voltage source and current monitor system used for I-V-T measurements. Siglent power supplies were current source and voltage measurement system for stressing the tested devices. Finally, all system components which required electrical power were connected to a sub-system of APC back-UPS to ensure tests were unaffected in the event the building lost power.

1. Custom Semiconductor Stress Testing Modules

Three identical testing modules were built for this research. Each module was designed to be capable of testing up to four devices simultaneously, allowing a system maximum of 12 DUTs. Modules were powered by 120 V AC/ 60 Hz line connected directly to a 5 V, 30 A DC power supply and a LED illuminated power switch. The two key custom sub-systems within each test module box were the DUT chamber with air foiled enclosure and the custom switch matrix. Figure 18 shows the internal design of one HTOL system test module.

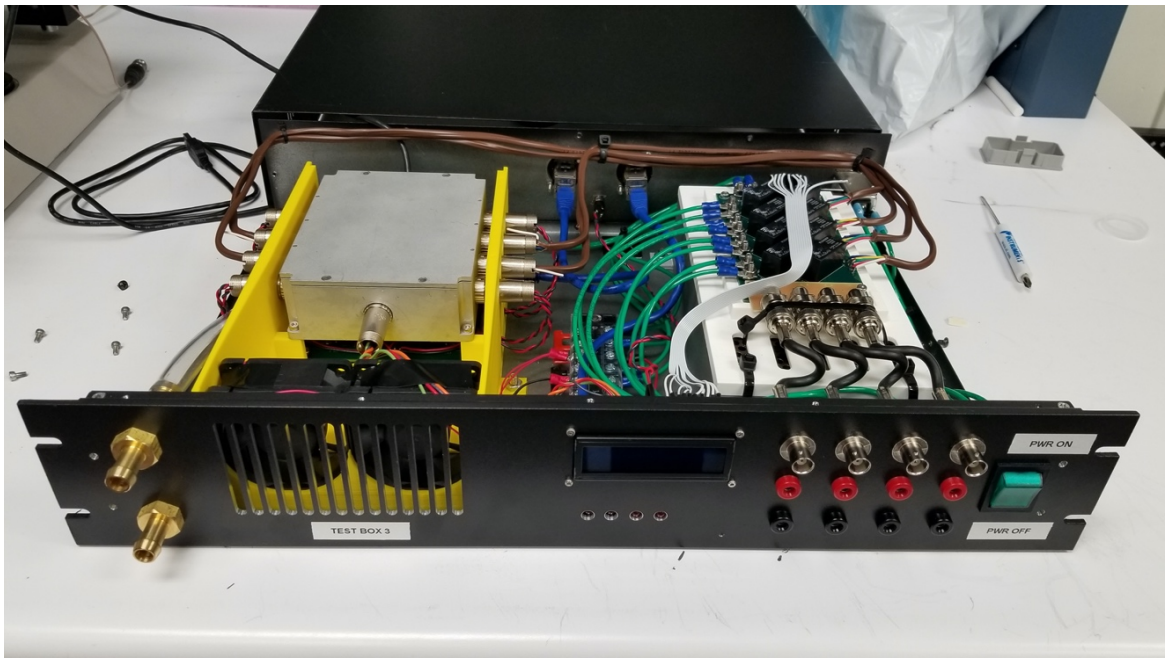
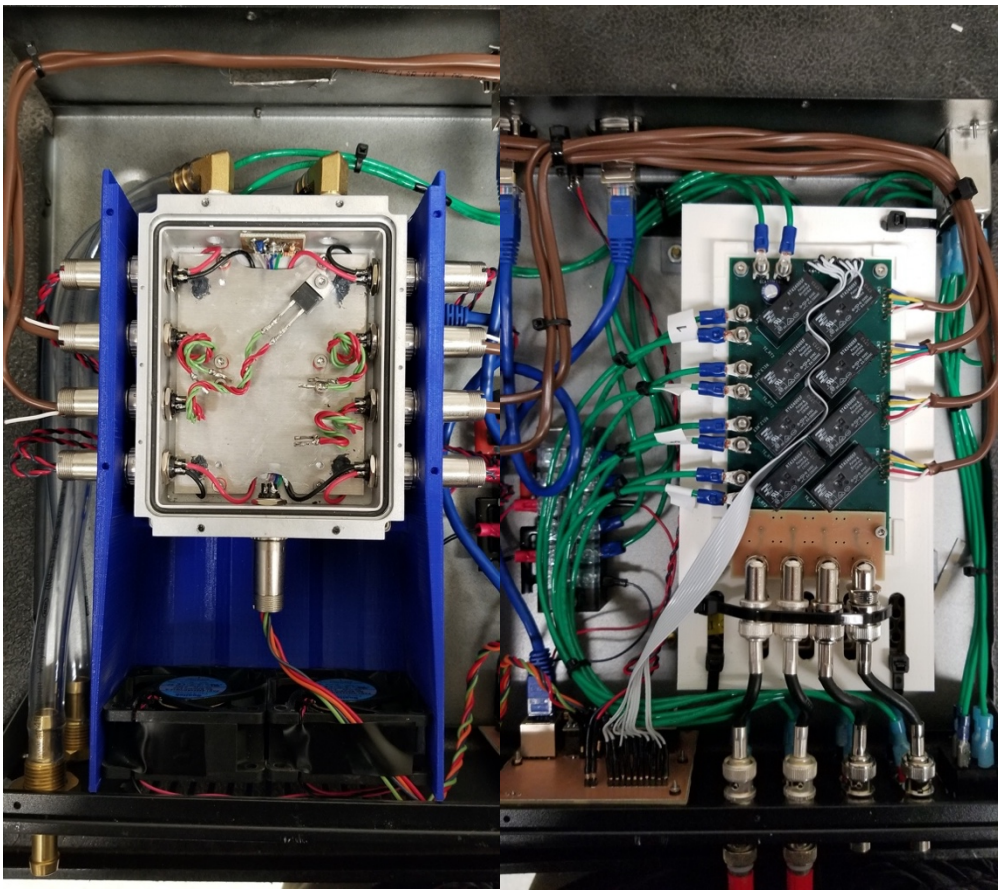


Figure 18. Image of an opened HTOL stress test module.

The DUT chamber was comprised of custom air-tight aluminum chamber, a custom circuit board to interface the hardware and software temperature control, and an air foil enclosure with two 5 V DC fans to regulate heat exchange from the DUT chamber to the outside environment. The DUT chamber served a housing structure for DUT and the heat sink for internal thermal processes. A nitrogen gas purging system was connected in series between all three DUT chambers through the two hoses running through back of the chamber. Humidity and local temperature readings were taken by a sensor along the rear, inner wall of each DUT chamber.

Each DUT chamber had a single large cold plate mounted on top of four 15-Watt thermoelectric coolers (TECs), providing a total cooling capacity of 60 W per DUT chamber. Thermal putty was used to create a good thermal contact between the TECs and the cold plate. Each quadrant of the cold plate was designed to have a single DUT mounted by screw directly to the cold plate. A single thermistor was secured with thermal epoxy as close as possible to the DUT region to minimize added errors in temperature measurements between the DUT and the thermistor.

The custom switch matrix circuit board enabled fast switching between each DUT while conducting I-V-T measurements. This was required since only one DUT could be measured at a time with the HP4142B. All internal mounts for the two circuit boards, DC power supply and DUT chamber were printed from polylactic acid (PLA) using 3D printing technology. Figure 19 shows the DUT chamber enclosure with a DUT installed and the custom switch matrix.



Opened DUT chamber with air foil enclosure (left) and custom switch matrix (right).

Figure 19. Close-up image of HTOL stress test module components.

2. Autonomous Control

The system needed to regulate local environmental conditions, such as temperature and humidity. Regulating local temperature was critical to mitigating excess heating of the

devices due to the surrounding environment during I-V-T measurements and stress intervals. Some self-heating was inevitable due to resistive characteristics of the DUT, but it was accounted for to the greatest extent to achieve less biased results. Humidity control was another critical component since the testing system was designed to handle open cavity devices. However, this aspect of the system was unused since the tested devices where fully packaged.

The system needed to operate autonomously within its own feedback loop, requiring no additional user inputs once a stress test was initiated. All control aspects were accomplished through two methods. Real-time control for temperature, humidity, and displaying system information on the digital display for each module was achieved using two mbed NXP LPC1768 microcontrollers located within each of the test modules. These microcontrollers were chosen because of their ability to prioritize functional code through a real-time threading process. They were also inexpensive, small, reliable, and already had built in functionality to communicate via ethernet connections. One microcontroller was used strictly as a temperature control unit (TCU) while the other was used as a general control unit (GCU), for all other real-time control aspects and displayed system data across the scrolling digital screen on each module face plate, as shown in Figure 20.

Figure 20. Image of three energized HTOL stress test modules.

Overall system control and monitoring occurred through a master LabVIEW program. Environmental measurements, device measurements and system performance were displayed through the computer monitor in the LabVIEW front panel, shown in Figure 21. The program was straightforward and used a series of GUI buttons to take the user through a series of windows to set up instruments, assign devices, set up the desired stress test and run or abort tests. All entered information was displayed after being entered, allowing the user to conduct a final check before commencing a test.

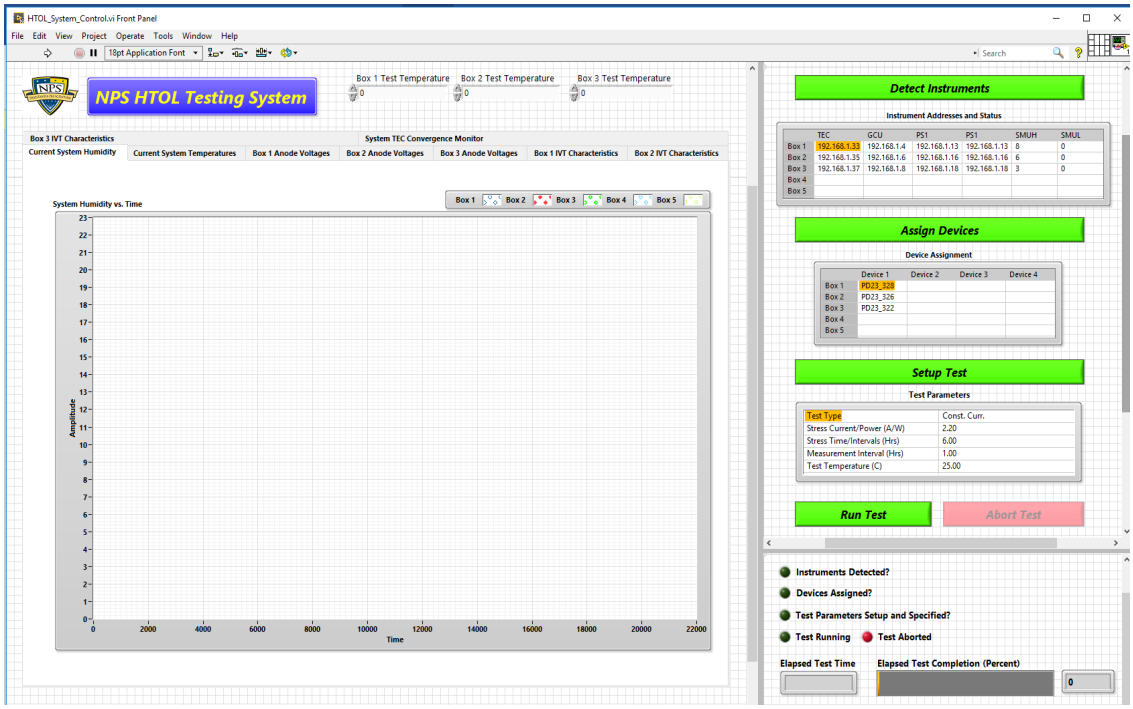


Figure 21. Screenshot of HTOL testing system control front panel in LabVIEW.

Each instrument or control unit required a unique IP address be assigned to ensure proper communication and control. Each component was assigned an available IP address through its own hardware interface or, in the case of the TCUs and GCUs, through the microcontroller coding using Mbed OS.

Table 3 contains a consolidated list of all assigned IP addresses used for the HTOL stress testing system.

Table 3. Assigned IP addresses.

Functional Description	Assigned IP Address
Gateway	192.168.1.1
CPU	192.168.1.2
Module 1 GCU	192.168.1.4
Module 2 GCU	192.168.1.6
Module 3 GCU	192.168.1.8
Siglent DC Power Supply 1	192.168.1.13
Siglent DC Power Supply 2	192.168.1.14
Siglent DC Power Supply 3	192.168.1.15
Siglent DC Power Supply 4	192.168.1.16
Siglent DC Power Supply 5	192.168.1.17
Siglent DC Power Supply 6	192.168.1.18
Module 1 TCU	192.168.1.33
Module 2 TCU	192.168.1.35
Module 3 TCU	192.168.1.37
Subnet Mask	255.255.255.0

C. HTOL SYSTEM TEMPERATURE CONTROL AND PERFORMANCE

Fast and stable temperature control was key to the design. Minimizing the time to reach a desired temperature allowed for quicker I-V-T measurements, reducing the amount of time between stress intervals. Precise temperature stability ensured set temperatures were repeatable and consistent for all I-V-T measurements.

Figure 22 shows the design schematic for the HTOL control loop.

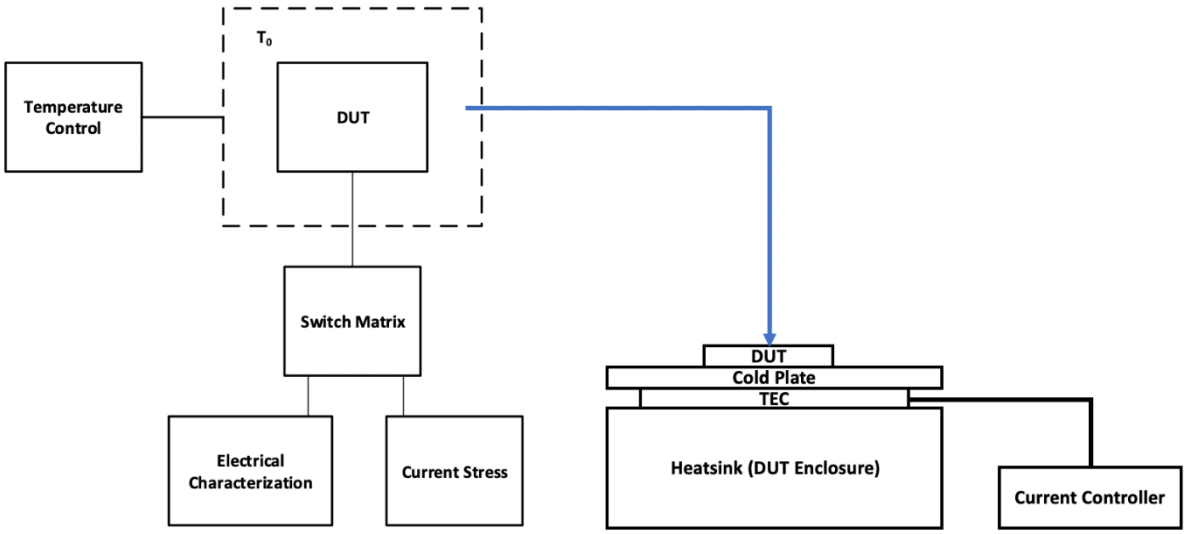


Figure 22. Block diagram of HTOL system control.

Temperature convergence was achieved through basic software control using a simple proportional-integral-differential (PID) loop. A simple LabVIEW program was used to manually tune the PID feedback. This method was applied simultaneously to all three testing modules. Figure 23 and Figure 24 show a controllable temperature range was achieved between 10 ºC and 60 ºC. Though there was slight variation in the response of each module, they were each able to achieve steady state with an error of less than 0.5 ºC. Each module converged to the set temperature within 30 seconds, and all reached a steady state within 60 seconds. The convergence time applied to increasing and decreasing temperature control.

Additional TEC temperature convergence curves are presented in Appendix A.

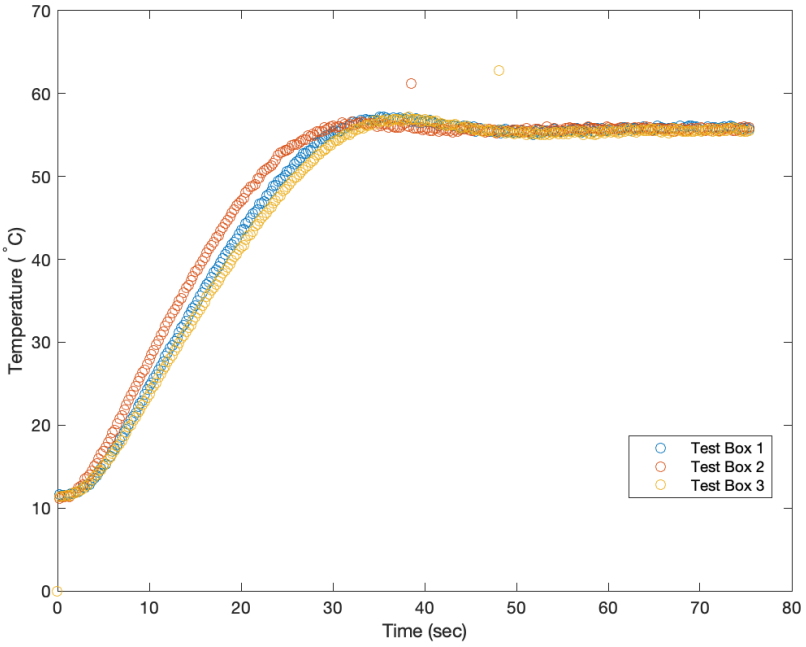


Figure 23. HTOL system TEC convergence from 10 ºC to 60 ºC.

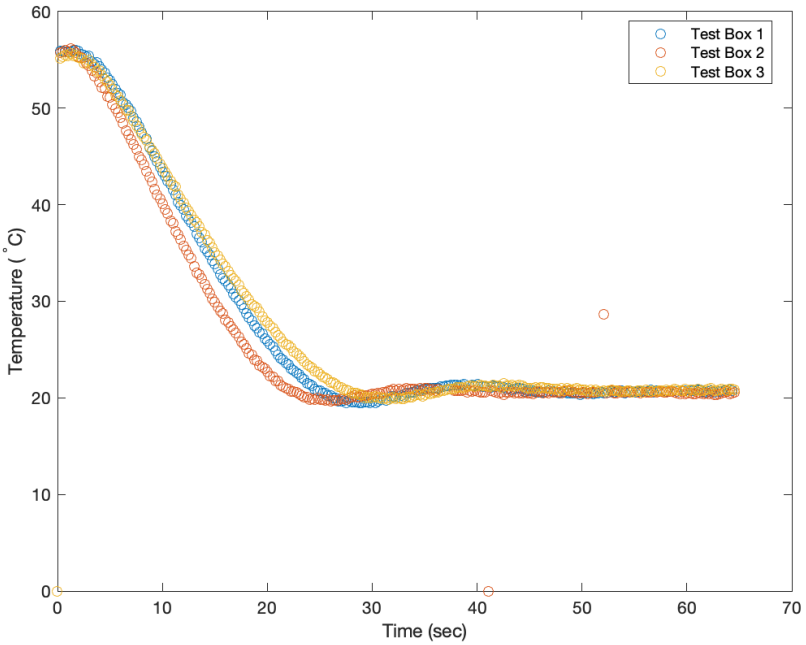


Figure 24. HTOL system TEC convergence from 60 ºC to 20 ºC.

HTOL stress testing system temperature remained consistent while electrically stressing three devices over a six-hour period, seen in Figure 25. During the experiment, each device was placed inside a separate DUT chamber and held at a constant temperature during the current stress interval. The three set stress temperatures were 30 ºC, 40 ºC, and 50 ºC for Modules one, two, and three, respectively. Even with the effects of device self-heating present, the temperature was held to within 1 ºC at 50 ºC, and less than 0.5 ºC for the lower temperatures.

However, based on applied current densities, an average of 20 W of power was dissipated by each DUT. Thus, this performance was significantly influenced by testing more than one device per DUT chamber with only a total of 60 W of cooling power available.

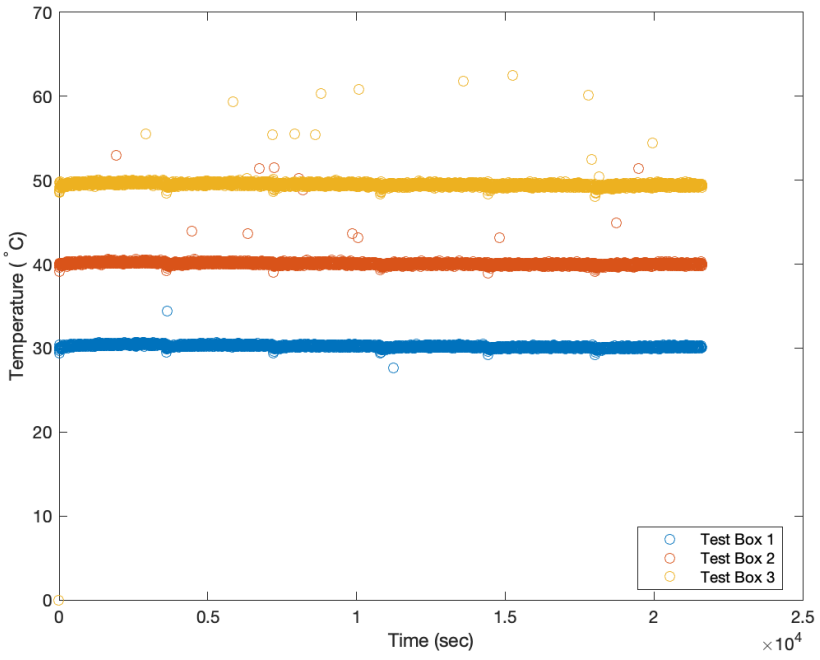


Figure 25. HTOL testing system temperature stability plot.

IV. PRE-STRESS CHARACTERIZATION AND EXPERIMENTAL METHODOLOGY

This chapter outlines the experimental methodology in three sections. The first section contains an overview of the commercial Pd/GaN Schottky diodes used for this research. Initial characterization and classification of the tested devices are introduced in the second section. Pre-stress measurements including I-V-T plots, Richardson plots, and resistance versus temperature plots are presented in the third section. Finally, section four explains the stress testing methodology implemented for this research.

A. COMMERCIAL GAN SCHOTTKY DIODE OVERVIEW

The commercial GaN-on-GaN Schottky diodes used for this research consisted of a MS interface made up by a Pd and n-type GaN contact. The epitaxial layer was vertically grown vertically grown on top of a bulk n^{++} GaN substrate using MOCVD. Each device is packaged in a TO-220 type plastic casing with a gold wire bond and backside ohmic contact. All devices used were from the same manufacturer lot. Figure 26 further depicts the device architecture of the Schottky diodes used for this research.

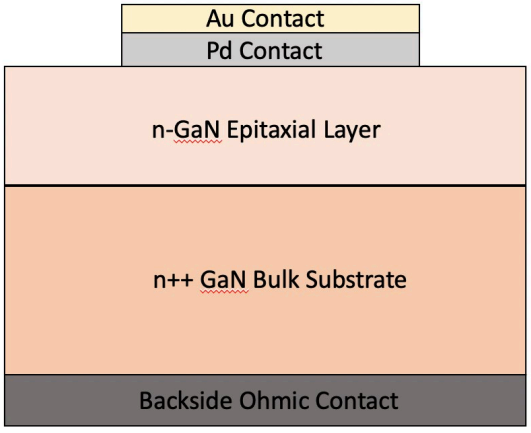


Figure 26. Commercial vertical *n*-type Pd/GaN Schottky diode architecture.

Prior to conducting any stress testing, over a hundred commercially packaged Pd/GaN Schottky diodes were characterized and classified.

Averages of critical device parameters are listed in Table 4.

Table 4. Table of device average values measured and calculated for Pd/GaN Schottky diodes.

Device Parameter	**Average Value**
Forward Resistance (R_{on})	2.81 Ω or 4.50 mΩ·cm^2
Ideality Factor (η)	1.44
Saturation Current (I_{sat})	0.665 nA
Reverse Leakage Current (I_{rev})	0.895 μA
Barrier Height (ϕ_b)	0.9 eV
Doping concentration (N_d)	2.48E+15 cm^{-3}

Barrier height and doping concentration were based on a smaller sample of devices.

The cross-sectional dimensions were approximated to be 0.04 centimeters long by 0.04 centimeters wide, with an area of 0.0016 centimeters squared. Linear regression methods were employed for determining the R_{on}, η, ϕ_b, and N_d from the I-V and I-V-T measurements. For the purpose of this research, I_{rev} was determined to be current value once the DUT reached -50 V.

B. INITIAL CHARACTERIZATION AND CLASSIFICATION PROCESS

Initial characterization was achieved through a set of I-V and C-V measurements. Measured device characteristics included forward resistance (R_{on}), ideality factor (η), saturation current (I_{sat}), and reverse leakage current (I_{rev}). Initial I-V measurements were conducted at room temperature to ascertain the aforementioned parameters. Forward bias was applied from 0 V to 3 V. Reverse bias was applied from 0 V to -50 V. The initial I-V measurements were also used to classify devices as either a single or a double diode. C-V measurements were used for a smaller set of devices to determine the approximate doping concentrations (N_d).

Table 5 shows the characteristics and classification of the Schottky diodes used for subsequent stress testing. A complete list of all devices initially characterized can be found in Table 8 and Table 9 of Appendix B.

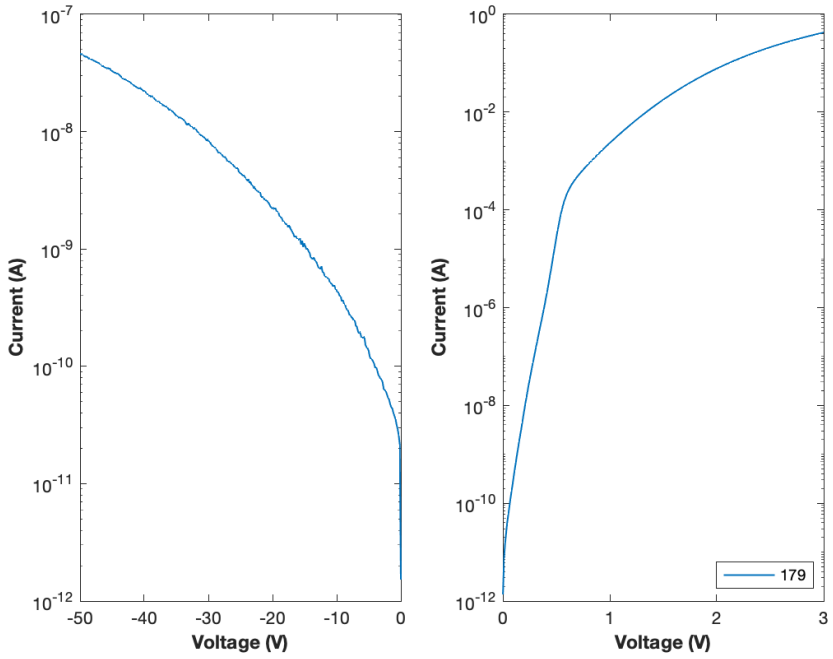
Table 5. GaN Schottky diode initial characterizations and classifications.

Device #	Ron (Ω)	Ideality Factor (*n*)	I_{sat} (A)	I_{rev} at -50 V (A)	Diode Notes (SD/DD)
19	2.82	1.24	1.69E-11	7.00E-08	DD
120	2.52	2.07	2.76E-09	9.00E-06	DD
143	1.88	1.13	7.47E-13	2.10E-09	SD
144	2.03	1.74	1.06E-09	1.30E-06	DD
149	2.25	1.95	8.60E-09	7.00E-08	DD
165	2.6	1.7	6.25E-10	1.40E-06	DD
178	2.51	2.02	1.09E-09	4.50E-07	DD
179	2.14	1.33	1.98E-11	4.60E-08	SD
322	4.05	1.21	7.80E-13	2.60E-08	SD
326	3.98	1.17	6.76E-13	5.80E-08	SD
328	2.46	1.22	8.26E-12	9.00E-07	SD

SD: Single Diode, DD: Double Diode

1. Device Classification

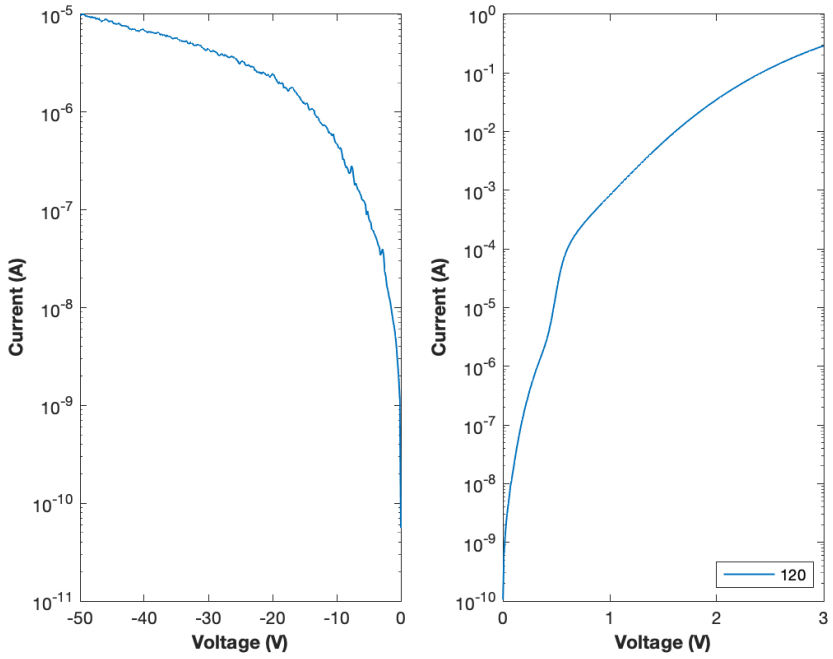
One of the first observations consistent with BHI came from the I-V plot. There was a clear non-linearity of the measured I-V relationships, identified graphically in the low voltage region of the semi-logarithmic I-V plot. As discussed in Chapter II, an ideal Schottky diode would exhibit a linear relationship in this region of the I-V plot. Thus, the more linear this region of the plot is, the nearer to unity the measured ideality factor was. If the devices tested were linear, or near linear, in this region then they were classified as a single diode (SD), such as device 179, as shown in Figure 27.



Reverse bias (left) and forward bias (right).

Figure 27. Device 179 I-V plot at room temperature, classified as a single diode.

Devices classified as SD generally had ideality factors between 1.25 and unity. Conversely, devices measured to have ideality factors above 1.25 generally displayed a non-linear relationship and were classified as double diode (DD). Device 120 was classified as DD, as seen from the graph in Figure 28. This description came from the two-step kink noticed in the low voltage region of the semi-logarithmic I-V plot, possibly behaving as two distinct diodes.



Reverse bias (left) and forward bias (right).

Figure 28. Device 120 I-V plot at room temperature, classified as a double diode.

The low voltage region was typically observed at or below 1 V while tested devices were in forward bias conditions. I-V plots for the remaining devices from Table 4 can be found in Appendix C.

2. Impurity Concentrations

C-V measurements were conducted for the eleven tested devices. Each measurement was taken using an Agilent Industries B1500A Semiconductor Device Parameter Analyzer. A reverse voltage sweep was conducted from 0.5 V to -20 V at frequency of 1 MHz.

The impurity, or doping, concentration for an MS junction can be approximated by using the relationship between the reverse bias voltage and the width of the depletion. Plotting the inverse capacitance squared versus reverse bias voltage should produce a straight line [25]. Equation (21) shows this relationship to be

$$\frac{1}{C^2} = \frac{2}{qK_s\epsilon_0 C_B}(V_R + \phi_B). \tag{21}$$

K_S is the relative dielectric constant of the material, a value of 8.9 for GaN. The slope of the line, as shown in Figure 29, will yield an approximation for the impurity concentration.

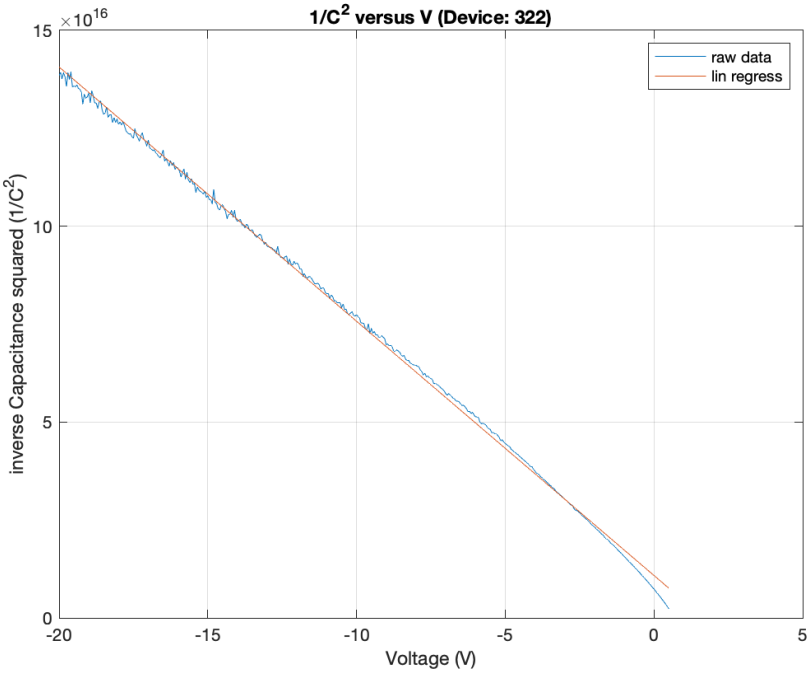


Figure 29. Device 322 C-V plot.

However, many of the measured C-V relationships resulted in slightly non-linear relationships, indicating a non-uniform doping concentration. Therefore, an alternative approximation was implemented by using the following equation

$$N(W) = \frac{2}{qK_s\epsilon_0}\left(\frac{1}{\frac{d\left(1/C^2\right)}{dV}}\right). \tag{22}$$

Equation (21) is for a n^+p junction with a varying impurity concentration [25]. The analysis works as a good model since the MS junction of a Schottky diode acts like a n^+p junction in many aspects. N_d values, as listed in Table 6, determined using Equation (22) were used for subsequent calculations for pre- and post-stress analysis.

Table 6. GaN Schottky diode impurity concentrations

Device #	Doping, N_d (cm^{-3})
19	2.95E+15
120	2.76E+15
144	2.06E+15
149	2.40E+15
178	2.43E+15
179	2.11E+15
322	2.45E+15
326	2.78E+15
328	2.42E+15

C. PRE-STRESS DEVICE MEASUREMENTS

Once the initial characterization and classification of devices was completed, devices selected for stress testing were further characterized using a larger temperature range to gain a better appreciation for the effects of temperature on the measured characteristics. Data collected from the I-V-T measurements were also used to determine pre-stress barrier heights and forward resistance values. This section will present the measurements for devices classified as SD and DD, in order to establish a comparison between the two classifications.

Additional measurements for other devices can be found in Appendix D, E, and F.

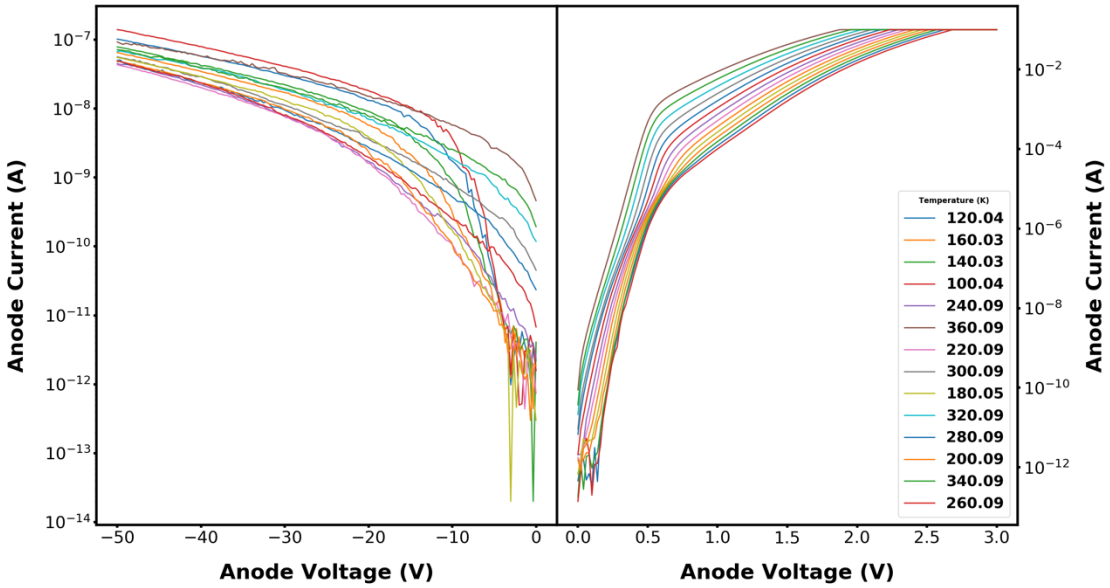
1. Pre-stress I-V-T Measurements

Pre-stress I-V-T measurements were conducted from 80 K to 400 K. This was accomplished using a vacuum chamber cryostat and liquid nitrogen. The HP 4142B was used for I-V sweeps. Software control was implemented through LabView programs to achieve automation for the I-V-T sweeps, temperature control process and data collection. As with the initial measurements, I-V sweeps were conducted in the forward and reverse directions. Temperature changes were made in 5 K increments. Measurements were

exported to comma separated variable, or .csv, files and imported to Python for pre-stress data analysis and plot generation.

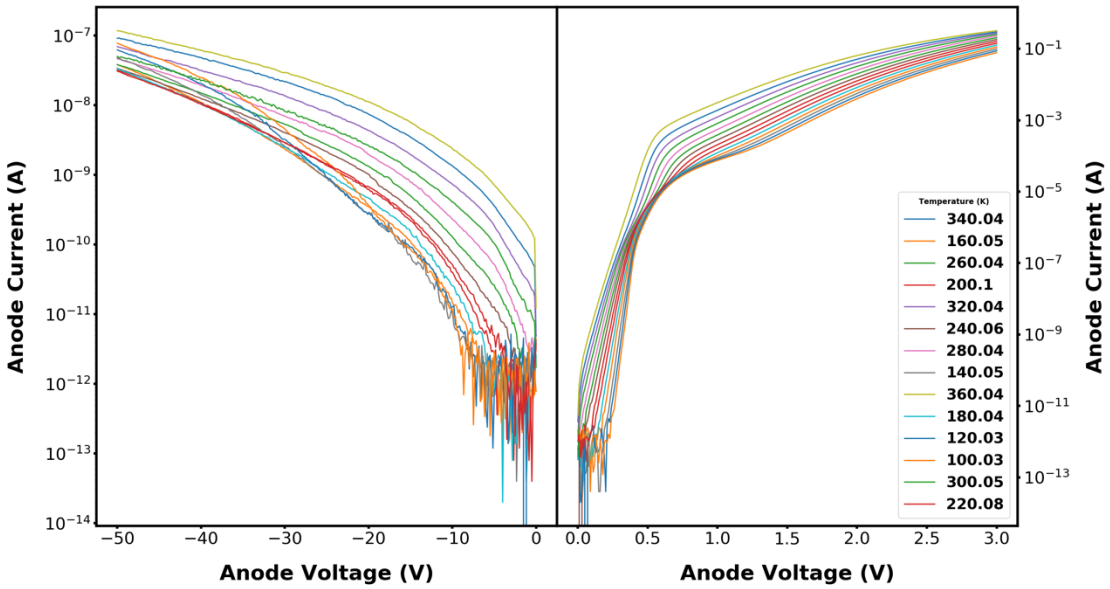
The experimental setup was limited by the number of available high-power units for the HP 4142B, thus any plots that are cut-off at 0.1 A were a result of using a low-power unit in the configuration. This only applied for forward bias and did not impact the analysis since the critical information was contained within the low-voltage region.

Figure 30 and Figure 31 show the I-V-T plots for device 179 and 120, respectively. Though measurements were taken at 5 K increments, the plots only include 20 K steps for better clarity between sweeps.



Reverse bias (left) and forward bias (right).

Figure 30. Device 179 (SD) pre-stress I-V-T plot.



Reverse bias (left) and forward bias (right).

Figure 31. Device 120 (DD) pre-stress I-V-T plot.

Varying temperature had two important effects on the I-V relationships for the devices. First, there was a noticeable increase in anode current in both the forward and reverse directions as temperature increased. This was less apparent in forward bias compared to reverse bias in which leakage currents increased almost a full level of magnitude in some devices between 80 K and 400 K. The second, and more important impact temperature had on devices was the classification of devices. At low temperatures, less than 120 K, all devices exhibited DD characteristics. Conversely, most devices began to exhibit SD characteristics at higher temperatures. The SD effect was harder to determine since it became more perceivable at or above 360 K which is close to the upper temperature limit was 400 K.

2. Pre-stress Barrier Height Measurements

Using the analysis methods presented in Chapter II, pre-stress Richardson plots were created to determine relative barrier height prior subjecting the devices to electrical stress. However, unlike the ideal examples provided, the test devices showed a non-linear relationship. This phenomenon was another early indicator to the presence of BHI.

Generally, the measured data was more accurately fitted by two lines, supporting the model of two diodes with different barrier height. One fit applied to the region with higher barrier height, which dominated at higher temperatures, and the other to a region with lower barrier height, which dominated at low temperature. Furthermore, the presence of two distant linear regions was observed regardless of a device being classified as SD or DD, indicating double-diode type BHI that was present even in devices that appear more like a SD.

Measured pre-stress barrier heights ranged between 0.79 eV and 1.08 eV for the higher region, taken from IV curves at high temperature and between 0.33 eV and 0.44 eV for the lower region, taken from IV curves at low temperature. The respective averages for each region were approximately 0.9 eV and 0.37 eV.

Figure 32 shows the Richardson plot for device 179.

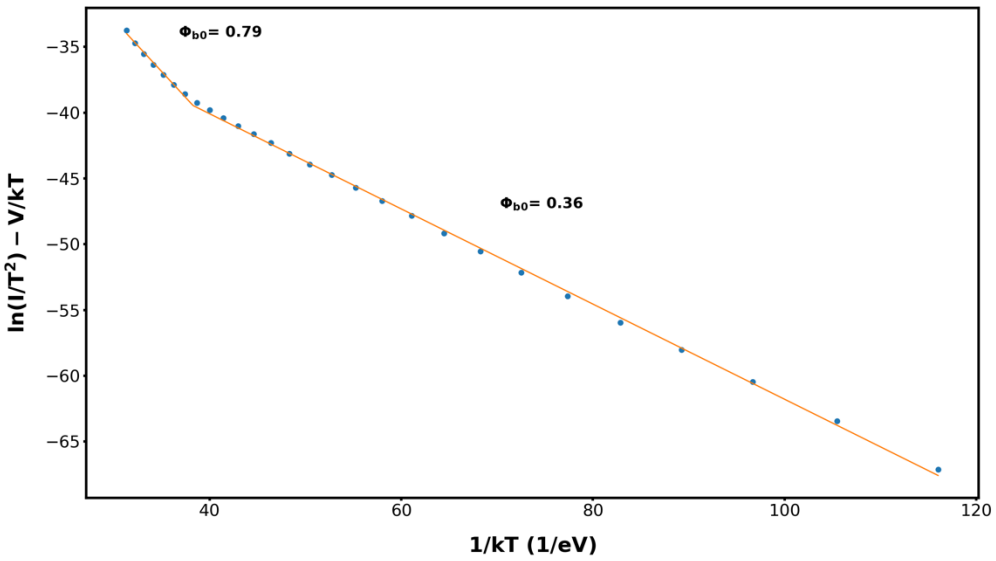


Figure 32. Device 179 (SD) pre-stress Richardson plot.

Figure 33 shows the Richardson plot for device 120.

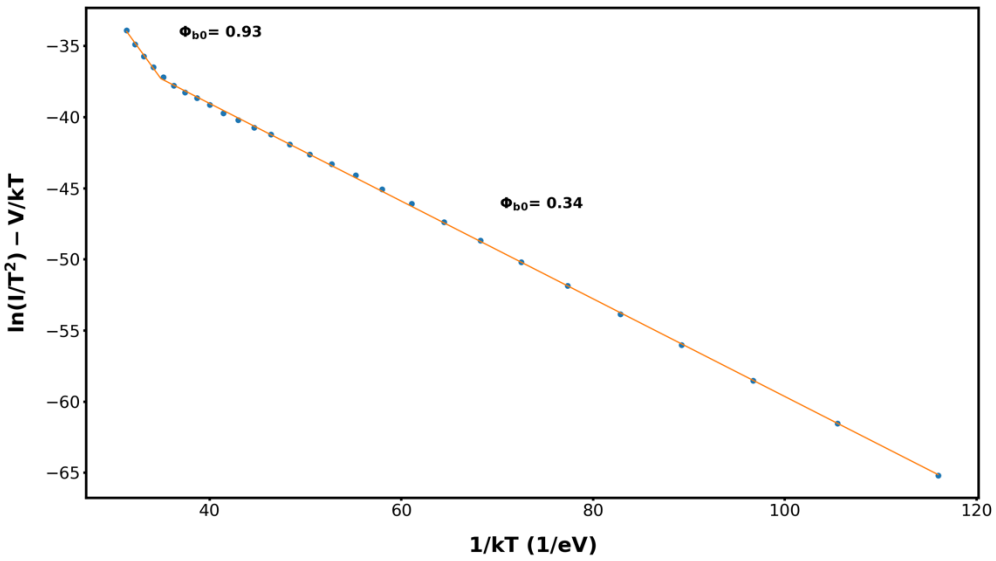


Figure 33. Device 120 (DD) pre-stress Richardson plot.

3. Pre-stress Forward Resistance Measurements

All pre-stress forward resistance measurements taken showed a semi-parabolic relationship with temperature, increasing at both low and high temperature regions. This behavior is expected as free carrier concentration is reduced at low temperature and mobility is reduced at high temperature, leading to higher resistance in both the low and high temperature regimes. Resistance measurements as a function of temperature ranged from about 1.8 Ω to 2.8 Ω, with most devices falling between 2 Ω and 2.6 Ω. The average resistance lows were around 200 K, and the range was generally between 150 K and 250 K. Device resistance did not appear to have a relation to whether a device exhibited more single or double diode characteristics. In many cases, devices classified as SD showed higher resistance values than those classified as DD.

Figure 34 shows the resistance-temperature relationship for device 179. The plot for device 120 is shown in Figure 35.

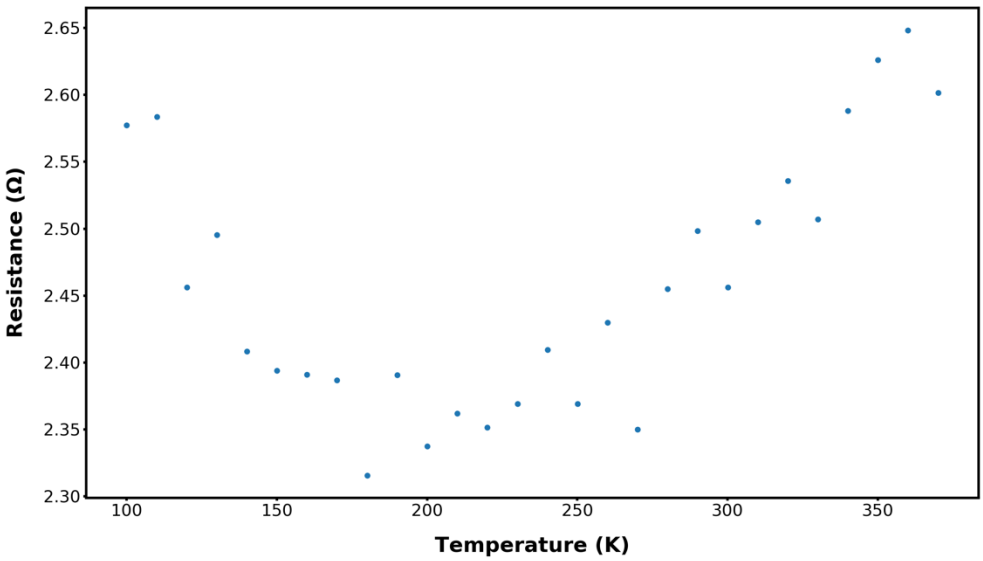


Figure 34. Device 179 (SD) pre-stress R_{on} versus temperature plot.

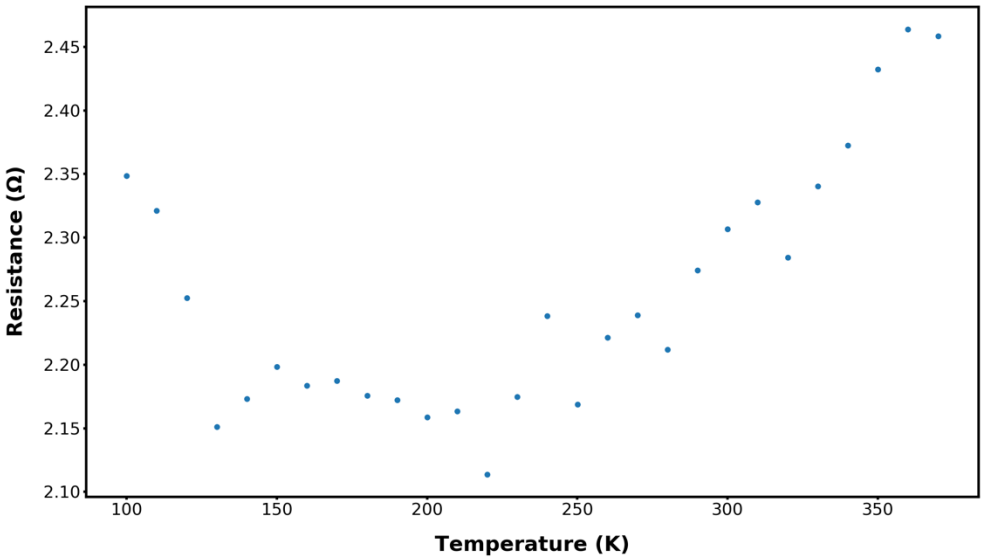


Figure 35. Device 120 (DD) pre-stress R_{on} versus temperature plot.

D. ELECTRICAL STRESS TEST METHODS

The stress test process utilized the same methodology that was used for device characterization. First, a series of preliminary tests to collect initial data about how the Schottky diodes would handle varying amounts of electrical current stress. Initial findings from the preliminary tests drove how the formal stress tests were set-up and conducted.

1. Preliminary Stress tests

Preliminary stress tests were used as a quick and simple method to determine the general current levels required to cause a device to fail. Individual devices were attached to an open cavity heat sync and stressed at varying magnitudes of electrical current. A DC fan was set up near the device to assist in cooling and mitigate localized self-heating of the device. A basic power supply was used to test and measure voltage and current across the Schottky diode. Voltage was increased until the desired current was achieved. Current levels ranged from 1.5 A up to 2.5 A. Devices would fail as either an open or a short and would be detected accordingly using the I-V measurements from the attached power supply. Current was increased by 0.25–0.5 A every 20–30 minutes manually until the device failed. Devices generally failed within a few minutes at current levels between 2.1 A and 2.4 A.

2. Formal Stress tests

Formal stress tests using the custom designed HTOL test system were developed and implemented following the preliminary stress tests. Four independent tests were conducted, and two different types of stress testing was applied, step-current and constant current. For each stress test conducted, at least one SD device and one DD device was tested for comparison. In addition to electrical stress, each DUT was subjected to a different thermal condition throughout the stressing intervals.

Table 7 shows the electrical and thermal stress testing conditions used for each device.

Table 7. GaN Schottky diode stress testing conditions

Device #	Stress Test	Current Levels (A)	Stress Temperature (°C)
19	Constant Current	2.1	50
120	Constant Current	2.1	40
143	Step-Current	1.7 - 2.3	40
144	Constant Current	2.2	30
149	Constant Current	2.2	40
165	Step-Current	1.7 - 2.3	30
178	Constant Current	2.2	50
179	Constant Current	2.1	30
322	Constant Current	2.2	50
326	Constant Current	2.2	40
328	Constant Current	2.2	30

The first stress test method applied was step-current which was similar to the preliminary stress tests in which current was incrementally increased throughout the stressing period. The total test time took approximately 12 hours since stressing was paused at 20-minute intervals to collect in-situ I-V-T measurements for analysis. I-V-T measurements for the in-situ data were taken from 10 °C to 50 °C at temperature increments of 5 °C, as limited by the design of the HTOL test system.

The second stress test method employed was a constant current test. In-situ data was collected at set time intervals throughout the stress test; however, a variable rate was applied throughout the test instead of a constant time interval as with the step-current stress test. I-V-T measurements, using the same method as the step-current test, were taken once per minute for the first six minutes, once every 10 minutes for the next hour and finally once per hour for the last six hours. This resulted in a total test time of about 18 hours.

All devices tested were subjected to thermal stress in addition to electrical stress. One of three thermal stress values, either 30 °C, 40 °C, or 50 °C, were used. Results obtained were used to analyze the effects of maintaining devices at a set temperature during the electrical stress window and if this thermal stress had any noticeable effects on the measured parameters.

V. IN-SITU RESULTS AND POST-STRESS CHARACTERIZATION

In-situ data collected during the electrical stress tests and post-stress characterization will be presented in this chapter. The first section will discuss in-situ stress test data for the step-current experiment. The second and third sections will discuss in-situ stress test data for the constant current tests. Lastly, the chapter concludes with post-stress measurements for the devices.

A. STEP-CURRENT STRESS TEST DATA

Devices 143 and 165 were subjected to step-current stress testing. The current sweep was from 1.7 A to 2.3 A, or approximately 1 kA/cm^2 to 1.4 kA/cm^2. Device 143 was held at a constant stress temperature of 40 ℃ while device 165 was held at a constant stress temperature of 30 ℃. Current was increased at increments of 0.1 A every hour resulting in a total stress time of approximately seven hours. Using in-situ data collected, the effects of electrical stress on reverse leakage current, barrier height, forward resistance, and inhomogeneity spreading were compiled and plotted.

1. Reverse Leakage Current

Measured reverse leakage currents remained relatively constant at current levels below 1.9 A. However, above 1.9 A, a noticeable degradation was observed, and the rate of degradation continued to increase until around 2.2 A. Similar responses for both devices were witnessed. Reverse leakage currents increased by approximately two orders of magnitude by the end of the stressing period.

Figure 36 shows the plots of reverse leakage current versus stress-time for device 143 The individual stressing windows for each step-stress current are divided by dashed lines on the plots.

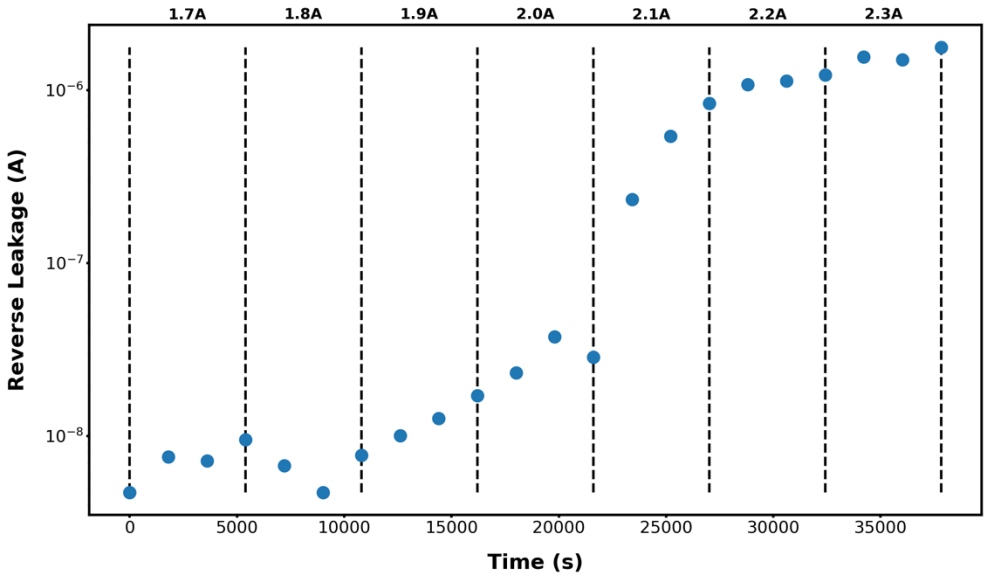


Figure 36. Device 143 (SD) I_{rev} versus stress-time plot.

Figure 37 shows the plots of reverse leakage current versus stress-time for device 165. There is an observed dip in the leakage currents measured at 2.2A, that are not consistent with the expected results. Although this experiment was set up in a mostly controlled environment, small variations in cold plate temperature can cause large jumps in measured leakage current on a logarithmic scale. Thus, the resulting dip is likely due to environmental interference or other anomalies with the test equipment.

Stress temperatures did not have a noticeable impact on the rate of degradation in leakage current between the two devices. Device 143 was held at the higher temperature and therefore was expected to have a quicker rate of degradation or a larger overall change in initial and final leakage current, however, this was not the case. Device 165 was classified as a DD due to its higher measured ideality factor and the majority of classified DD tested had higher initial leakage currents.

In both test cases, the rise in leakage current is exponential through the current regions of 1.9 A to 2.1 A. This behavior is consistent with the linear decrease in barrier heights for each device presented in the following section.

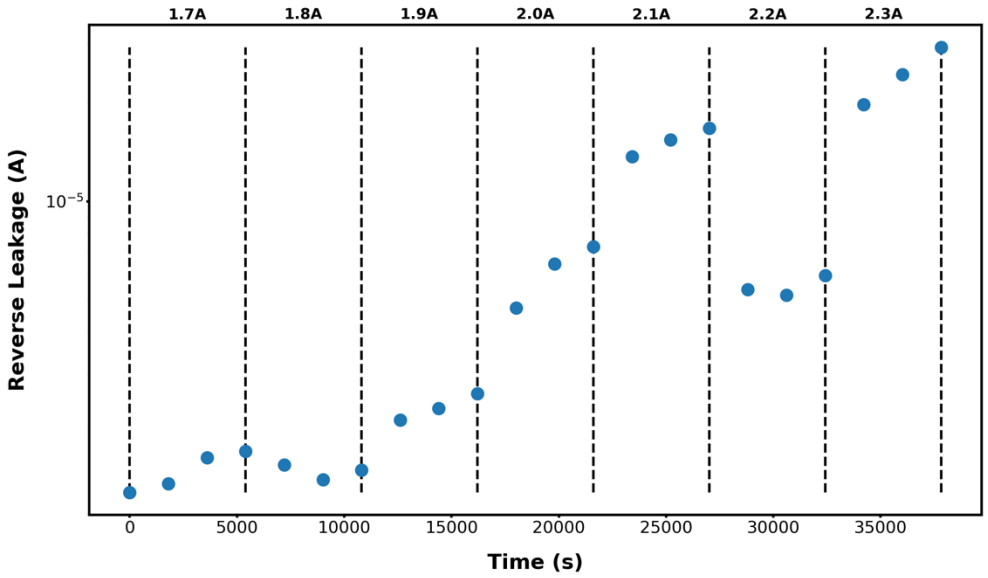


Figure 37. Device 165 (DD) I_{rev} versus stress-time plot.

2. Barrier Height

Comparable stress effects to the leakage current were observed for barrier height which also degraded over stress-time. Measured values remained mostly consistent below about 1.9 A; however, above 2.0 A the rate of degradation linearly increased until around 2.2 A where a steady state effect begins to develop. A general lowering of the barrier height was witnessed over the course of stress testing time for both devices. Device 143 saw a 25 % reduction in barrier height while device 165 had a 30 % reduction. As with the leakage currents, stress temperature did not present an appreciable effect on the rate of, or total, degradation of the barrier heights.

Figure 38 shows the in-situ measurements of the barrier height for device 143.

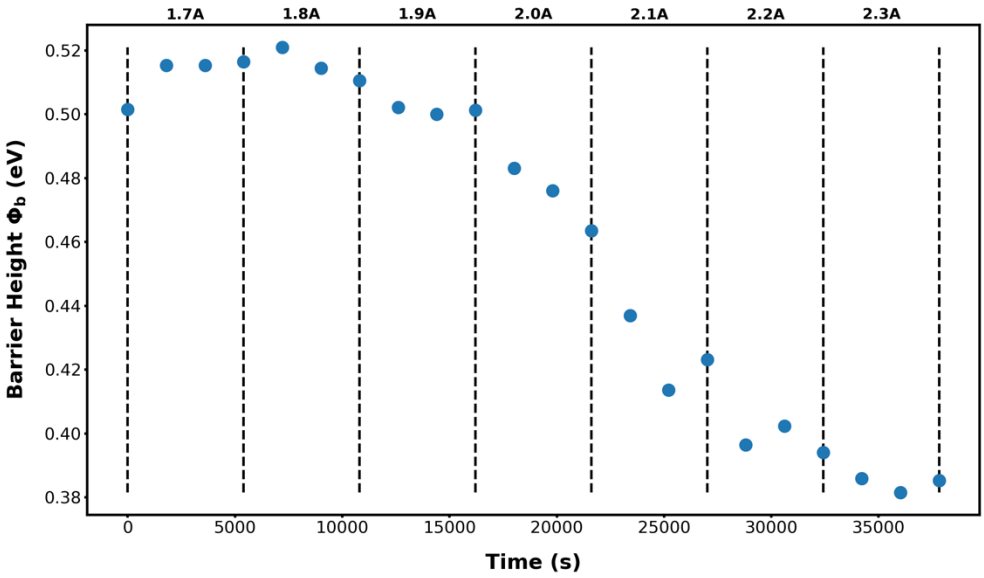


Figure 38. Device 143 (SD) Φ_b versus stress-time plot.

Figure 39 shows the in-situ measurements of the barrier height for device 165.

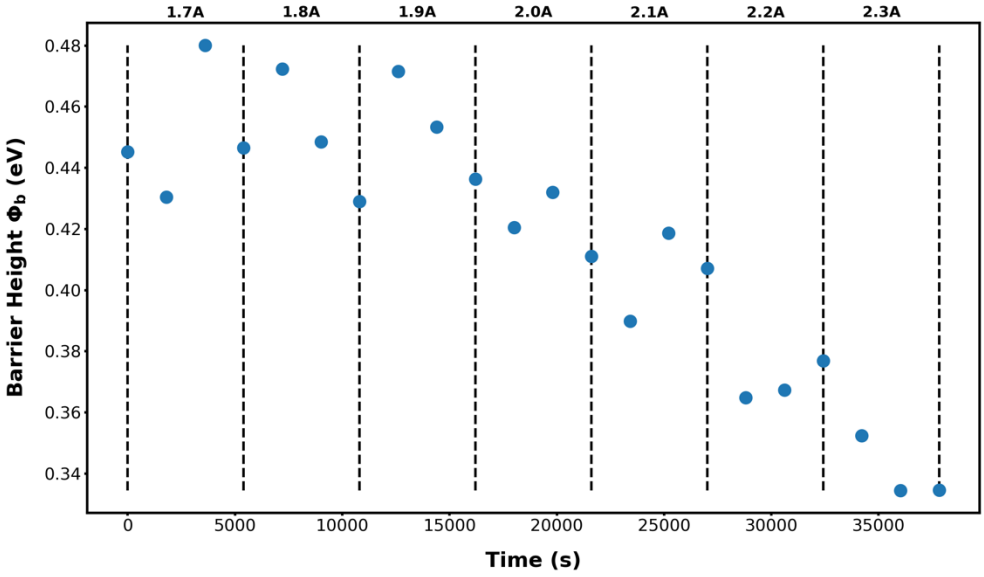


Figure 39. Device 165 (DD) Φ_b versus stress-time plot.

3. Forward Resistance

In-situ forward resistance measurements were mostly inconclusive for the step-stress test, even when considering the potential effects of the different stress temperatures used. Both devices had varying measurements between 2.8 Ω and 4.5 Ω, as shown in Figure 40 and Figure 41. If a linear regression were used to fit the data between the first and final resistances measured, then it is plausible the resistances increased over the entire stress time, which would be consistent with results from other devices and expected effects of electrical and thermal stress applied to the devices. Results from the constant current tests were more definitive and will be presented later in this chapter.

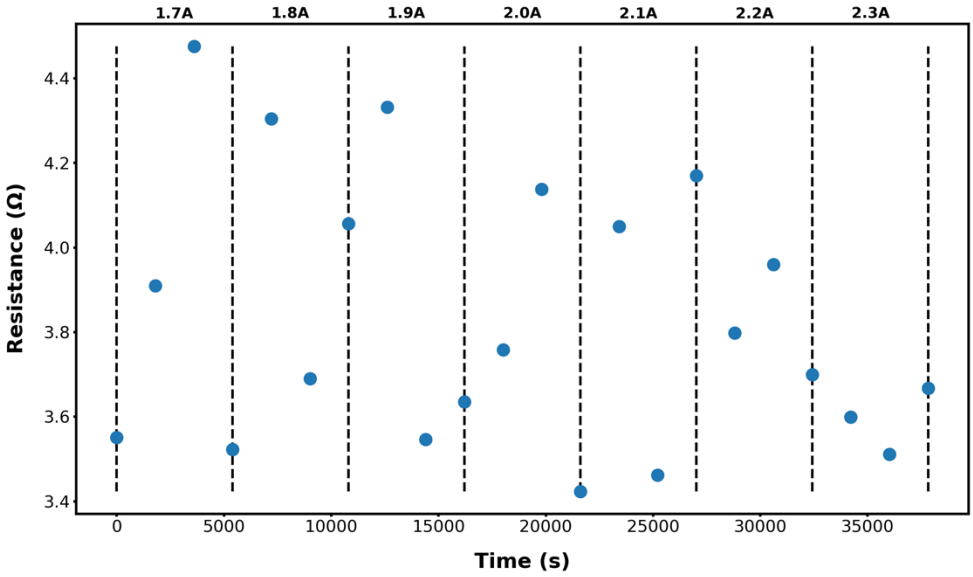


Figure 40. Device 143 (SD) R_{on} versus stress-time plot.

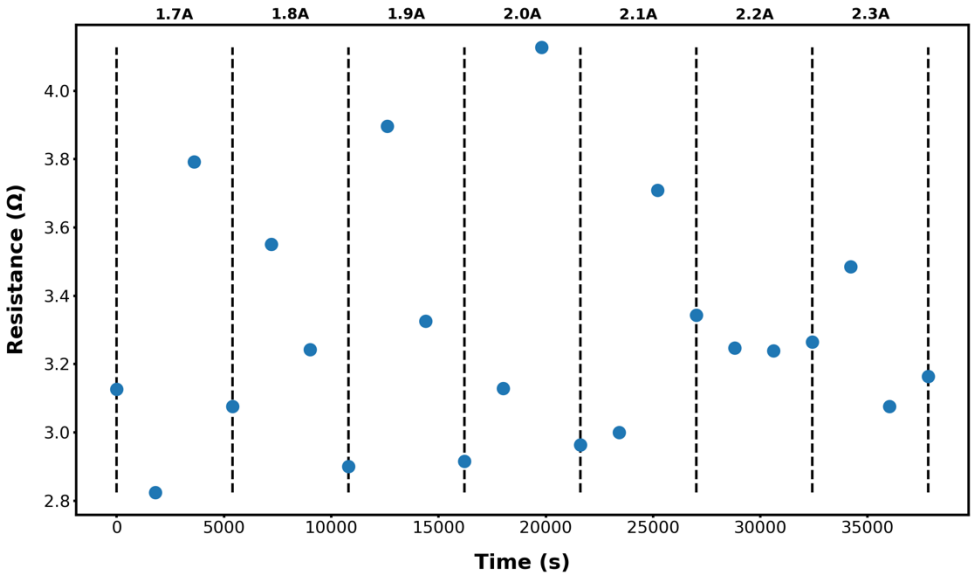


Figure 41. Device 165 (DD) R_{on} versus stress-time plot.

4. Inhomogeneity Spread

Inhomogeneity spread for both devices increased with stress-time and stress current. Although double diode behavior supported by barrier height data was noticed in all tested devices, the single patch distribution analysis of Tung was used to extract a measurement of BHI spread by fitting the model to the current at voltages below which the current is restricted by the device resistance. A noticeable change in degradation rate occurred above current levels of 2.0 A. The degradation continued to increase linearly throughout the remainder of the test. Inhomogeneity spread increased by approximately 29 % for Device 143 when compared to the initial values.

Figure 42 shows the inhomogeneity spread versus stress-time for device 143.

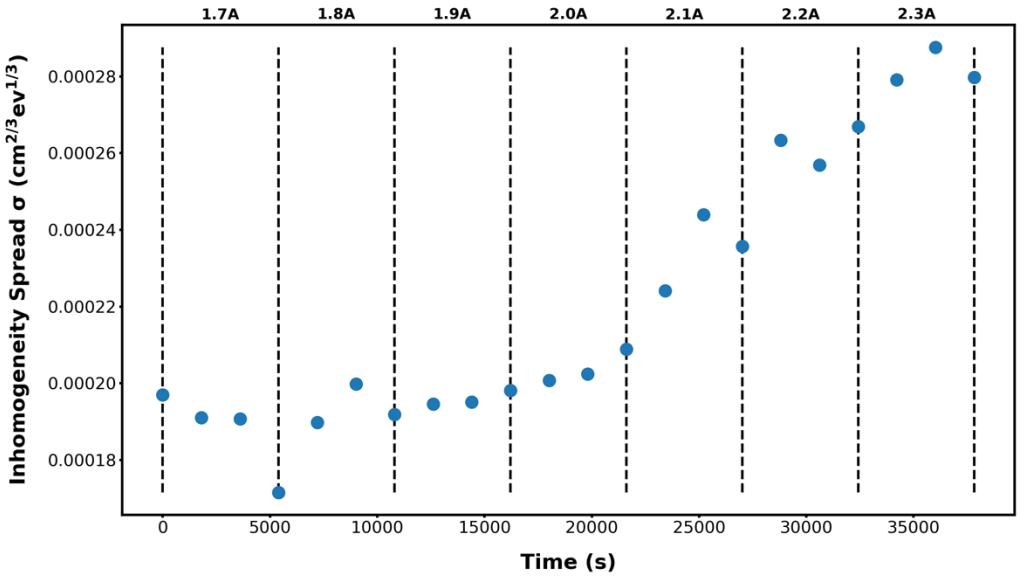


Figure 42. Device 143 (SD) σ versus stress-time plot

Device 165 also had an increase in inhomogeneity spread, but it was significantly larger when compared to the SD case shown in Figure 42. Device 165 had a 60 % increase, more than double that of device 143, over the same stress-time. This large delta was possibly due to device 165 already exhibiting stronger DD characteristics than device 143. Furthermore, since device 165 was held at a lower temperature than device 143 during the stress intervals, device temperature is not a likely contributor. It is also feasible that the relatively close stress temperatures were not different enough to have an observable impact since difference in stress temperatures was only 10 ℃. Subsequent tests had three devices and a temperature range of 20 ℃.

Figure 43 shows the inhomogeneity spread versus stress-time for device 143.

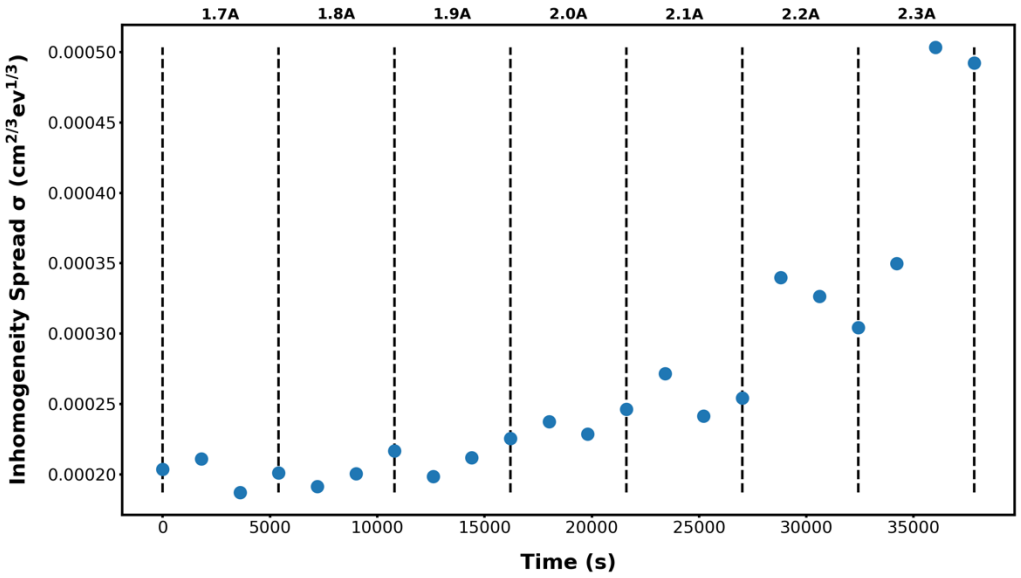


Figure 43. Device 165 (DD) σ versus stress-time plot

B. CONSTANT CURRENT STRESS TEST DATA: 2.1 A

Devices 19, 120, and 179, were stressed at a constant current of 2.1 A which is slightly more than 1.3 kA/cm^2. Respective thermal stress applied to the devices 19, 120, and 179 were 50 ℃, 40 ℃, and 30 ℃. This section presents data for a SD, device 179, and a DD, device 19, to provide a comparative overview like the previous section; however, there is a 20 ℃ range in stress temperature between the presented devices.

The step-current test indicated device parameters quickly degrade at or above current densities of 1.3 kA/cm^2. Therefore, a variable measurement time-rate was applied for this test to increase the number of data points collected at the early stages electrical stress. The goal was to capture the early rapid degradation and see if a steady state was reached after as a function of time. As with the step-current stress test, the effects of electrical stress on reverse leakage current, barrier height, forward resistance, and inhomogeneity spreading were compiled and plotted.

1. Reverse Leakage Current

Reverse leakage current degraded as expected for tested devices. The magnitude of degradation was relatable to observations from the step-stress experiment, approximately two orders of magnitude. Significant degradation appeared to occur within the first 30 minutes to an hour of testing prior to reaching a steady state within the last six hours.

Figure 44 shows the reverse leakage current versus stress-time for device 179.

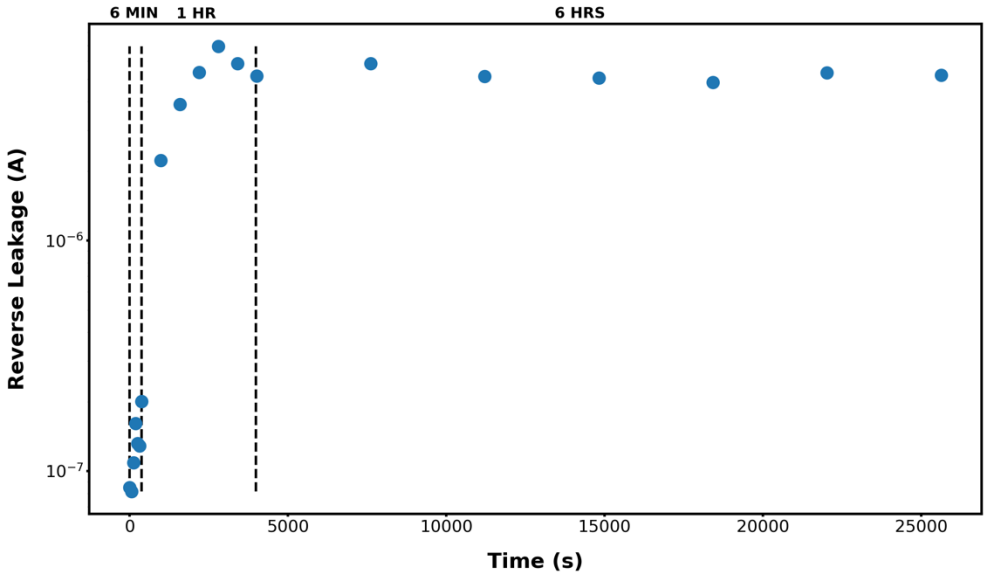


Figure 44. Device 179 (SD) I_{rev} versus stress-time plot

Figure 45 shows the reverse leakage current versus stress-time for device 19. The results do not show an appreciable effect of the stress temperatures used for the tested devices, despite the larger range used. This is likely due the magnitude of electrical stress and the effects the self-heating from high current density is having upon the devices, effectively drowning out any impact from the external stress temperature applied.

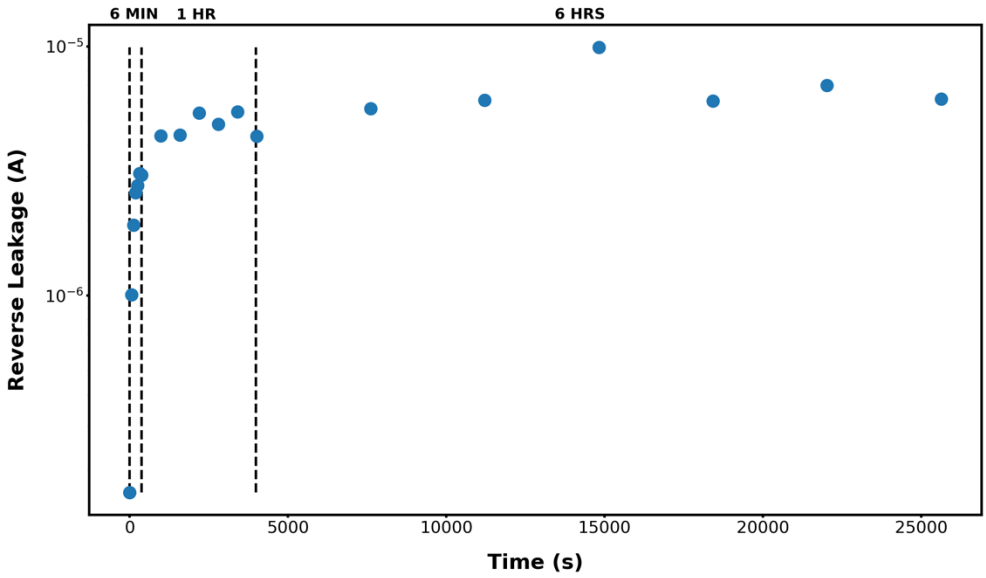


Figure 45. Device 19 (DD) I_{rev} versus stress-time plot

2. Barrier Height

Overall, barrier height measurements appeared to follow a similar tendency to the results of the step-current stress test in that barrier height degraded with stress time. A rapid lowering of the barrier height was observed for each device in the early stages of stressing before a near steady state was achieved. Barrier height for device 179 decreased approximately 0.1 eV, as shown in Figure 46, while the barrier height for device 19 decreased roughly 0.25 eV, indicated in Figure 47.

Effects of external thermal stress appeared negligible, as with previous results, when comparing devices. However, there was still a perceived exponential rise in leakage currents which correlated to the linear decrease in the barrier heights, as observed in the previous test. This was less apparent compared to the data collected from the previous test due to challenges with curve fitting the data from the early stages of stress testing. Analysis dependent on I-V-T data was limited by the temperature ranges of the HTOL stress test system.

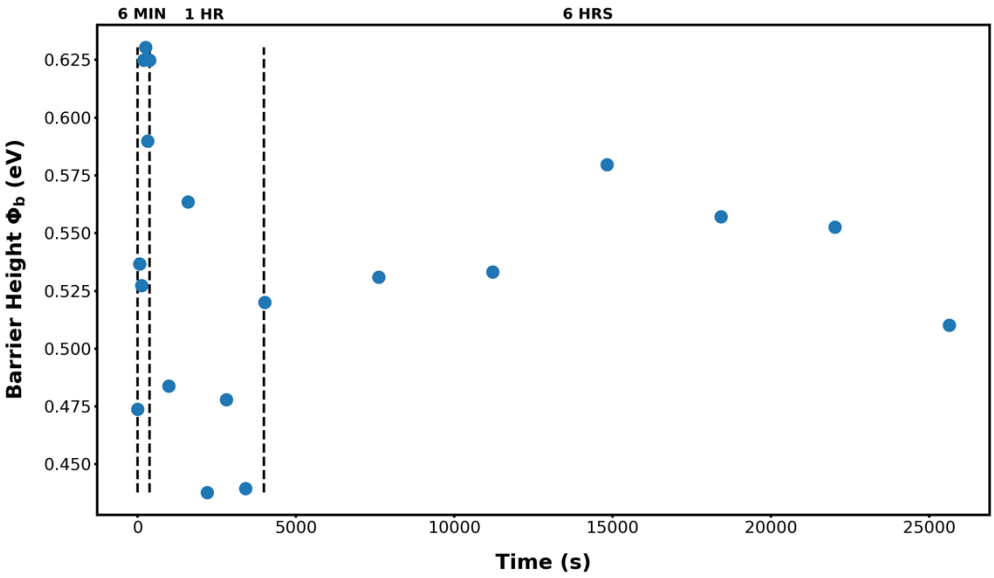


Figure 46. Device 179 (SD) Φ_b versus stress-time plot

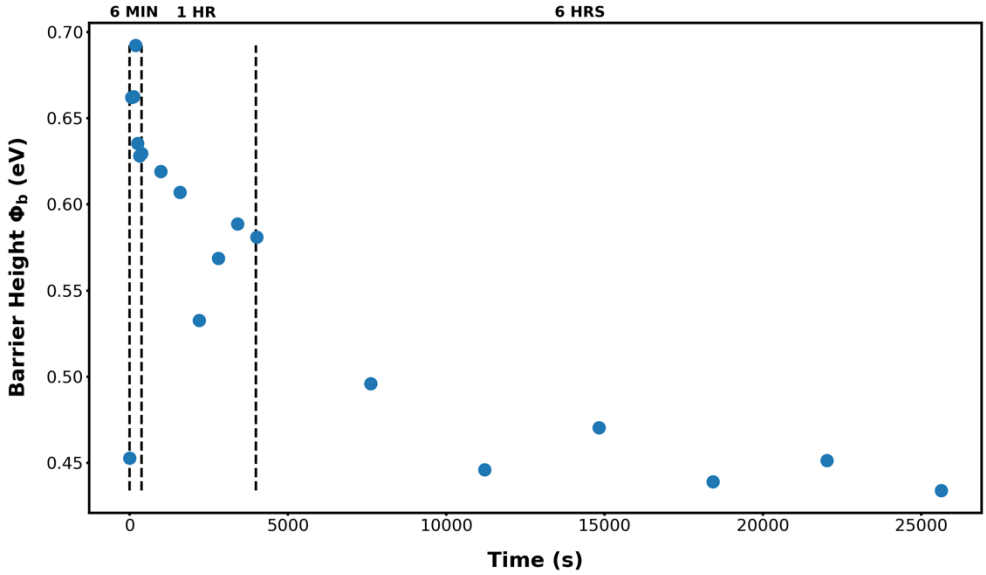


Figure 47. Device 19 (DD) Φ_b versus stress-time plot

3. Forward Resistance

In-situ forward resistance measurements taken during the constant current stress test showed a more identifiable trend than those from the step-stress test. Forward resistances generally increased as a function of stress-time, for both types of devices, SD and DD. In-situ resistance values increased on average 0.5 Ω to 0.7 Ω for tested devices. As with previous results from the constant-stress test, there was a rapid degradation before the values level off, or start to level off at the end of the stress time.

Figure 48 and Figure 49 display the forward resistance versus stress-time plots for device 179 and device 19, respectively.

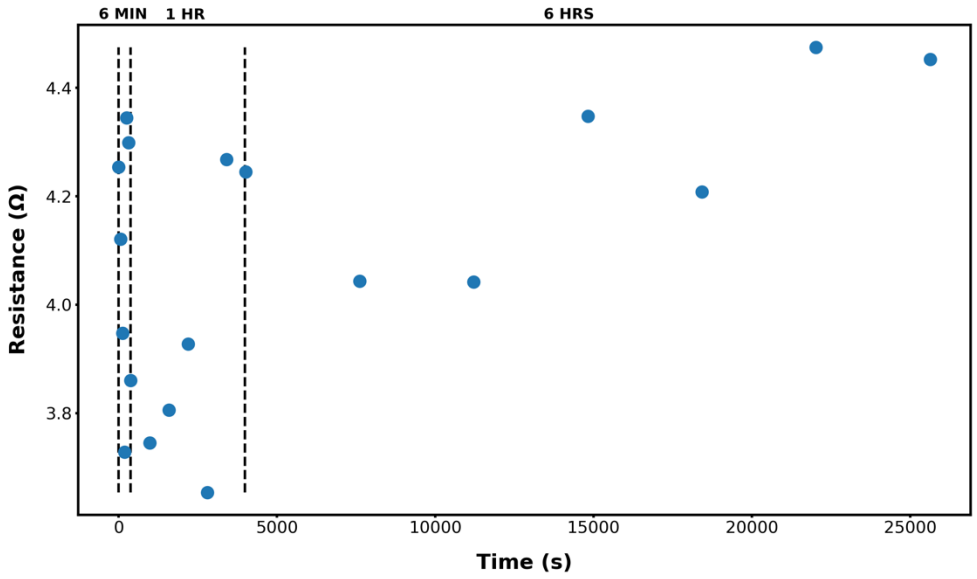


Figure 48. Device 179 (SD) R_{on} versus stress-time plot

There were no observable trends based on stress temperature, and any noticeable changes in measured device characteristics seemed to be linked to its initial characteristics and classification based on the degree of DD-type behavior observed.

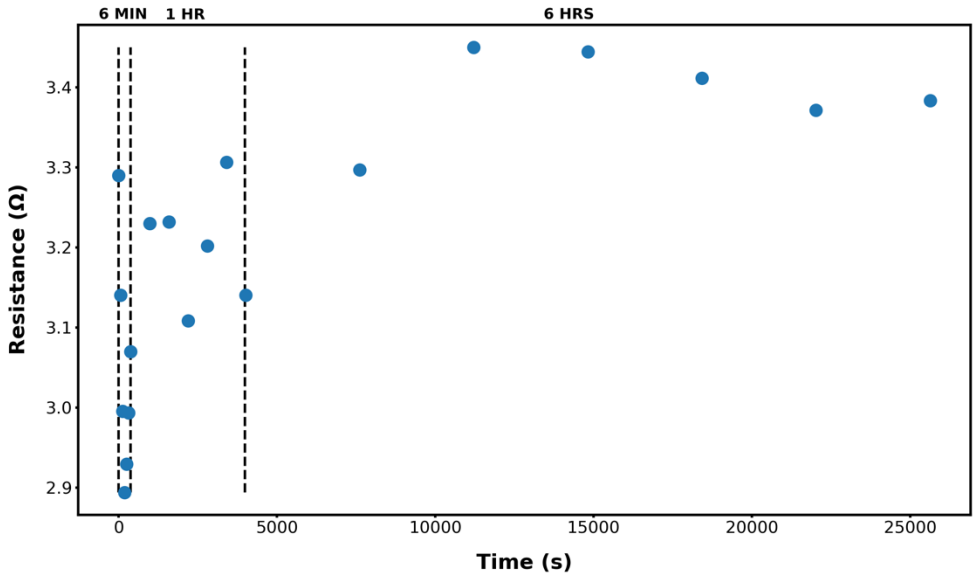


Figure 49. Device 19 (DD) R_{on} versus stress-time plot

4. Inhomogeneity Spread

Measurements of inhomogeneity spread produced mixed results between devices. Device 179 varied greatly before about four hours of testing before possibly showing an increasing trend in the last three hours; however, results were more questionable, but generally yielded a 10 % increase in spread if the irregular peaks detected in the first few hours are overlooked or assumed to be anomalous. Results for device 19 presented a more definitive trend which aligned with results from the step-stress test of increasing with stress time. Inhomogeneity spread increased approximately 25 % by the end of the stress test.

Applied thermal stress could not be conclusively assumed to be a factor in device degradation, indicating that other causes were the primary contributors. Devices classified as DD generally showed greater changes, especially for barrier height and inhomogeneity spread, during the in-situ stress measurements for the first two stress tests.

Figure 48 shows the results for device 179.

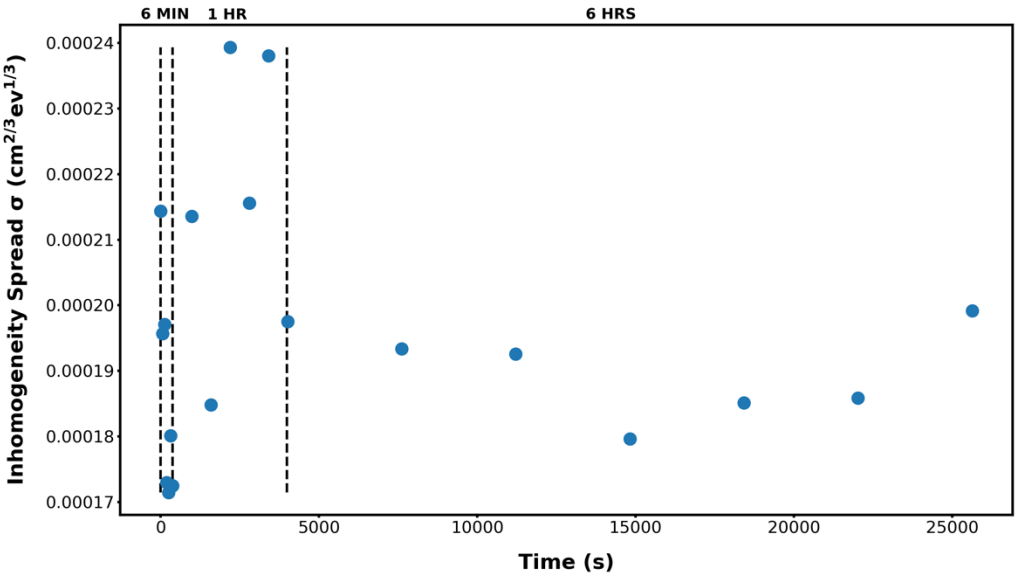


Figure 50. Device 179 (SD) σ versus stress-time plot

Figure 49 shows the results for device 19.

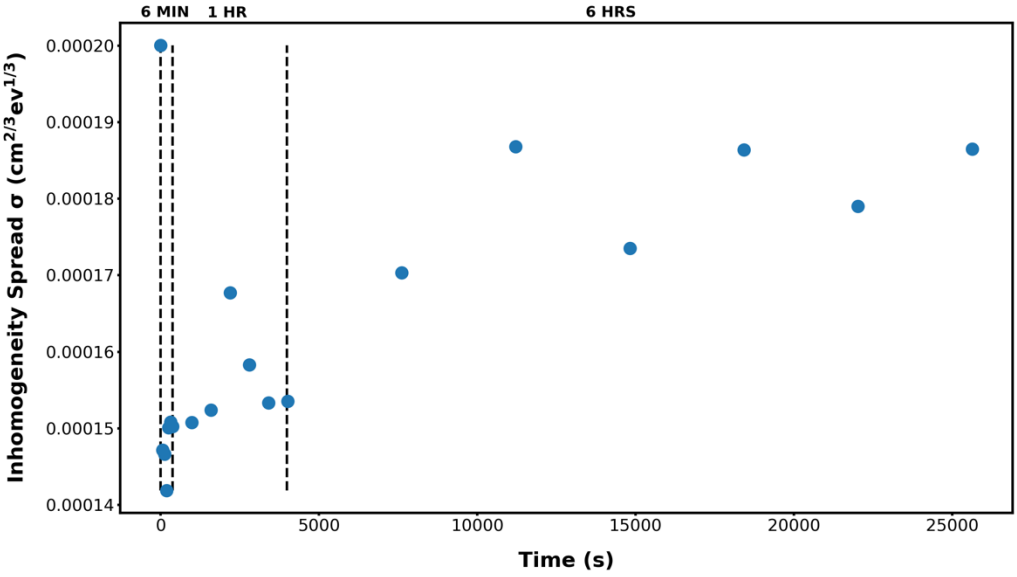


Figure 51. Device 19 (DD) σ versus stress-time plot

C. CONSTANT CURRENT STRESS TEST DATA: 2.2 A

The final two stress tests conducted were conducted at a constant current of 2.2 A, or just below 1.3 kA/cm^2 and each test had a set of SD or DD devices. The first test was conducted on a set of three SD devices, 322, 326, and 328 maintained at the corresponding temperatures, 50 ℃, 40 ℃, and 30 ℃. The second test was on a set of three DD devices, 144, 149, and 178 with each held at the respective stress temperatures of 30 ℃, 40 ℃, and 50 ℃. This resulted in a complete representation of stress test data for diodes exhibiting SD and DD characteristics at each of the three set stress temperatures. Reverse leakage current, barrier height, forward resistance, and inhomogeneity spreading were compiled and plotted as a function of stress-time.

Results from devices 328 and 178 will be presented in this section. These devices had a 20-degree temperature difference between applied thermal stress and followed the same trends discovered in the previous test; ultimately providing inconclusive evidence as to the effects thermal stress had on measured changes in device characteristics.

1. Reverse Leakage Current

Measurements of in-situ reverse leakage current remained consistent throughout all tests conducted and for all devices. Major degradation transpired within the first 30 minutes to hour of stress testing, followed by a period of reduced degradation rate and apparent steady-state. Reverse leakage currents reduced by two orders of magnitude.

Figure 52 presents the reverse leakage current versus stress-time plot for device 328 while Figure 53 shows the same for device 178.

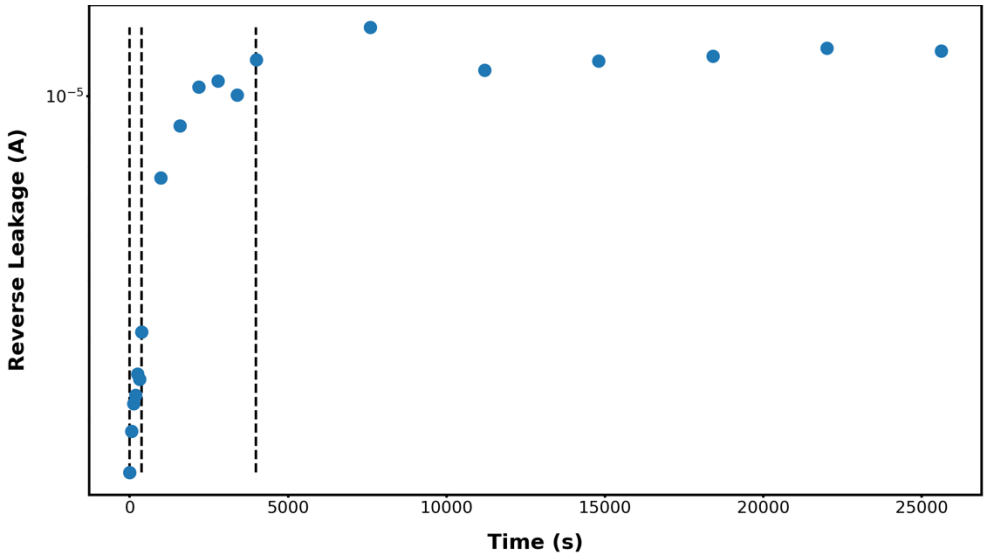


Figure 52. Device 328 (SD) I_{rev} versus stress-time plot

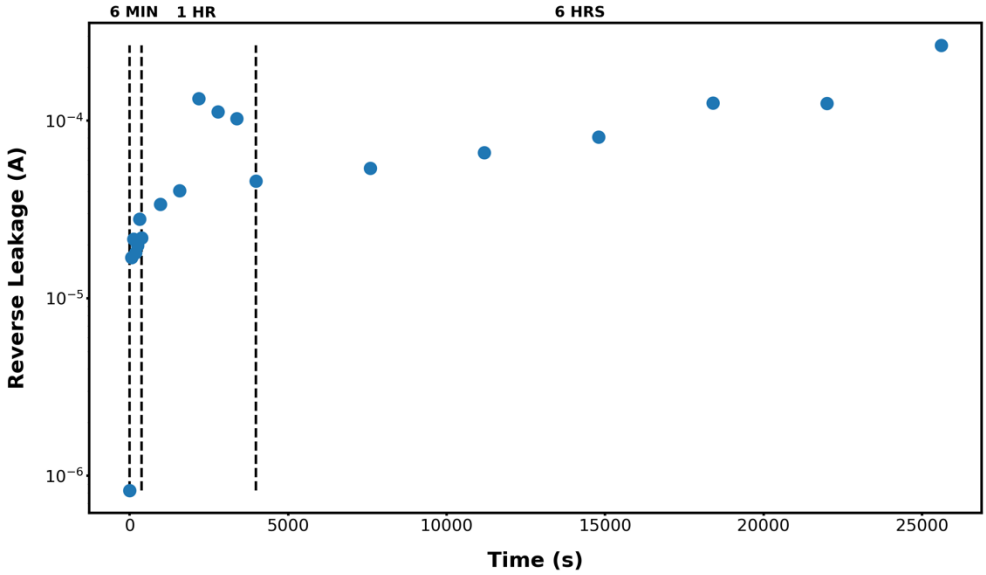


Figure 53. Device 178 (DD) I_{rev} versus stress-time plot

2. Barrier Height

Effective lowering of device barrier heights was determined through the in-situ analysis. Results were consistent between cases of SD and DD and compared to the previous test at 2.1 A, the degradation data collected from the tests are 2.2 A were more definitive. A rapid degradation was observed within the first 30 minutes to an hour followed by a prolonged period of near steady state. Barrier heights were reduced between about 30 % and 50 % over the entire stress-time, with DD devices showing a larger change when compared to the SD devices.

The plot of barrier height versus stress-time for device 328 can be seen in Figure 54.

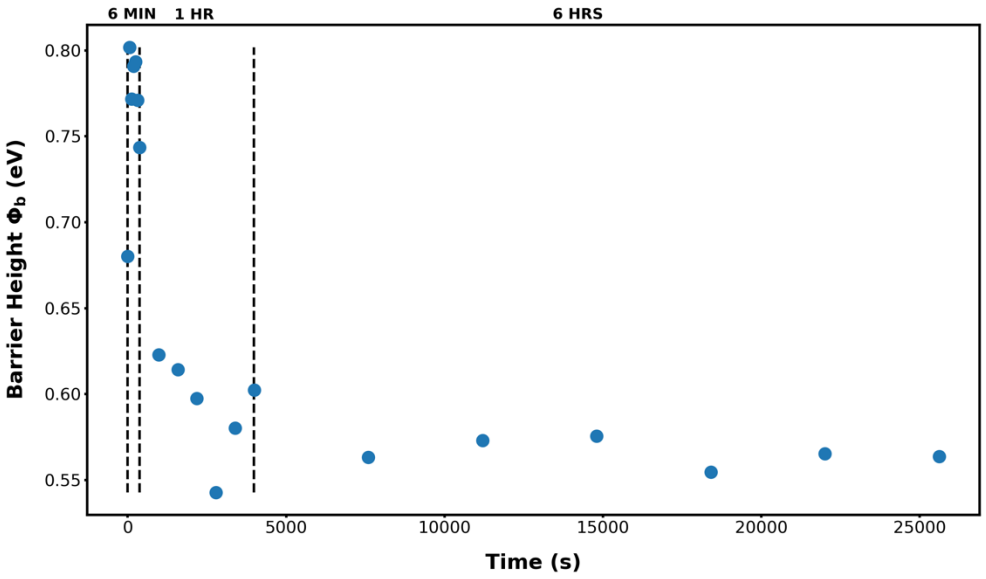


Figure 54. Device 328 (SD) Φ_b versus stress-time plot

Figure 55 shows the degradation of barrier height over stress-time for device 178.

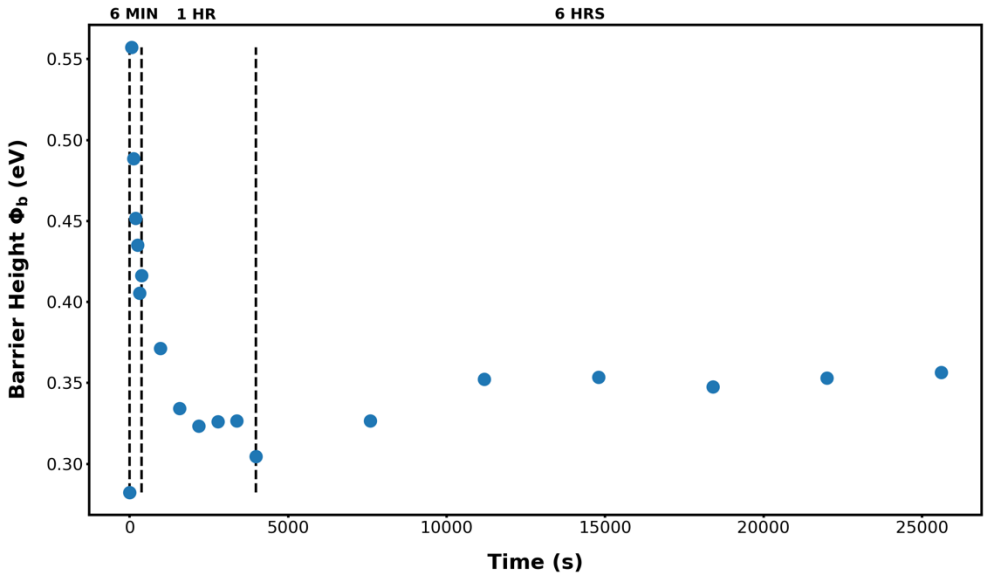


Figure 55. Device 178 (DD) Φ_b versus stress-time plot

3. Forward Resistance

The measured changes to resistance values were as expected and followed a comparative trend to the measurements taken during the stress test conducted at 2.1 A. In fact, the total change in resistance was slightly higher than the previous test and was likely due to the increased stress current. Forward resistances increased between 0.5 Ω and 1 Ω for both sets of devices.

Figure 56 shows the change in forward resistance over stress-time for device 328.

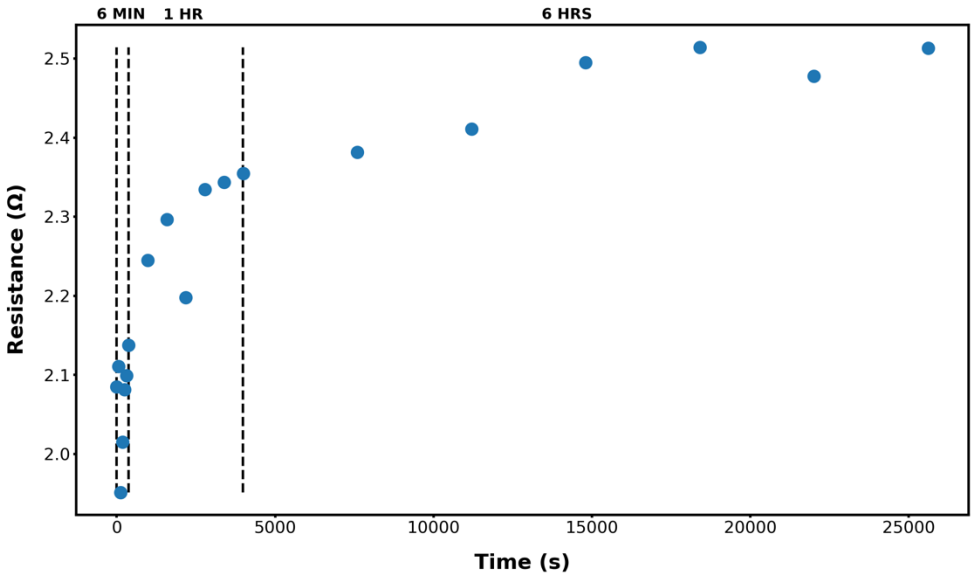


Figure 56. Device 328 (SD) R_{on} versus stress-time plot

The relationship of forward resistance stress-time for device 144 is found in Figure 57.

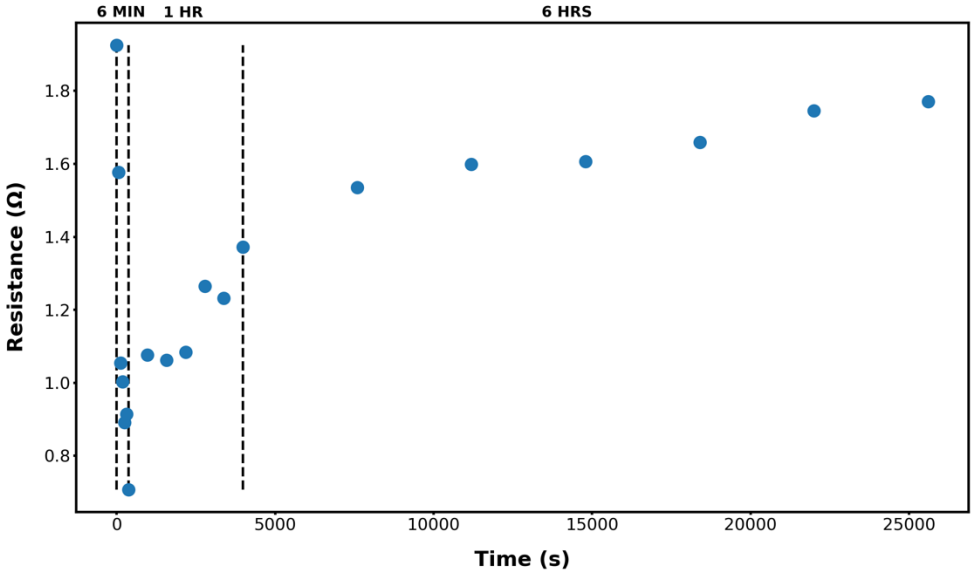


Figure 57. Device 144 (DD) R_{on} versus stress-time plot

4. Inhomogeneity Spread

The spread of inhomogeneity produced mixed results between the two sets of tests but was consistent within each set. Results were as anticipated for the SD set, showing the same rapid degradation over the first 30 minutes to an hour and tapering off for the remaining six hours. Inhomogeneity spread increased, by approximately 15–20 %, as a function of stress-time.

Figure 58 shows the plot of inhomogeneity spread versus stress-time for device 328.

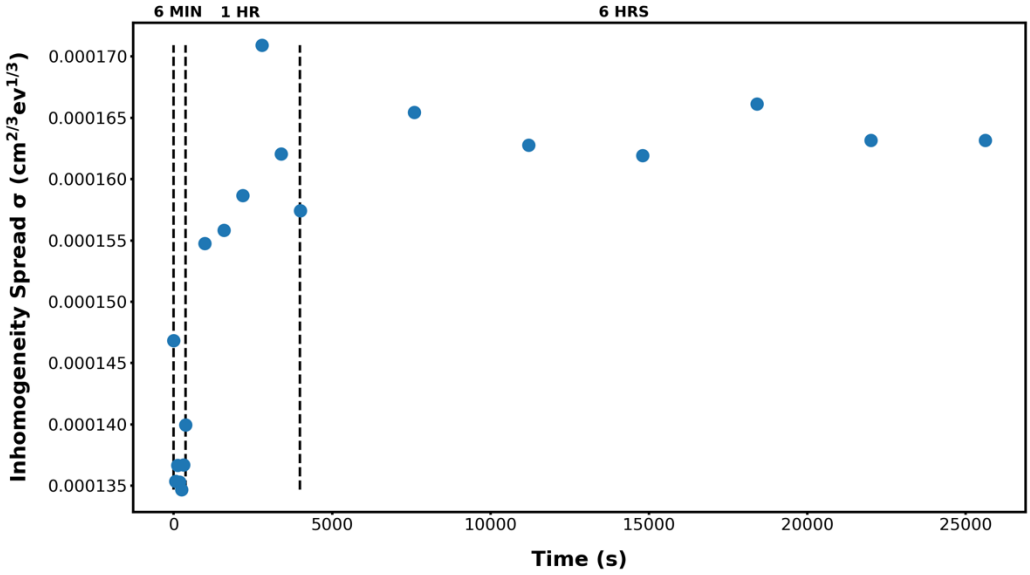


Figure 58. Device 328 (SD) σ versus stress-time plot

Results from the DD set of devices were not as expected and showed little to no change in inhomogeneity spread across the entire stress period. Though each device in the set showed the same data trends. Only device 178 showed any sign of a spread increase with stress time, yet it decreased to near initial values after about 2 hours of stressing, as seen in Figure 59. It is possible these measurements were anomalous since all other devices

up to this point showed a similar trend, though further testing would be required to substantiate these findings.

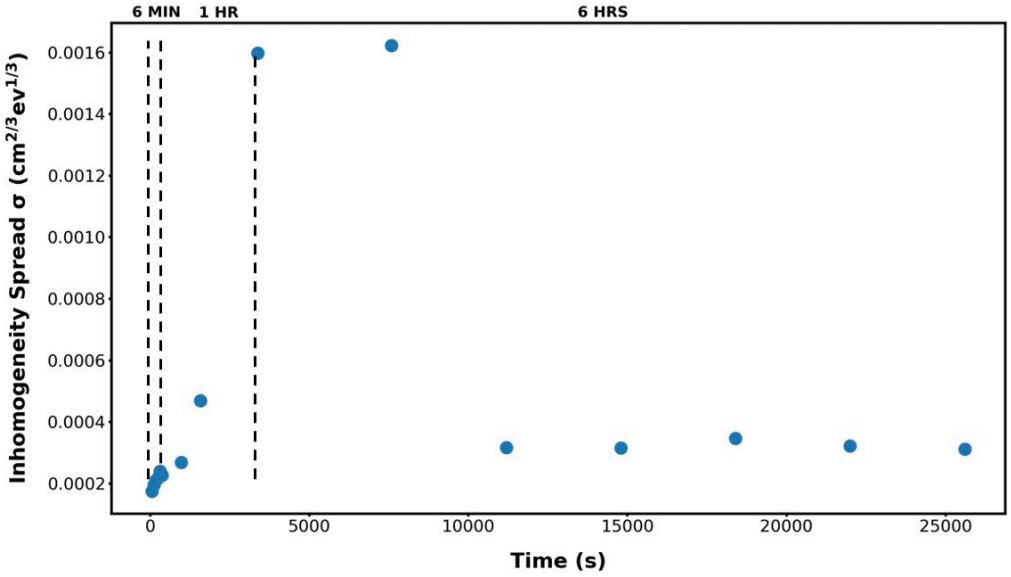


Figure 59. Device 178 (DD) σ versus stress-time plot

D. POST-STRESS DEVICE MEASUREMENTS

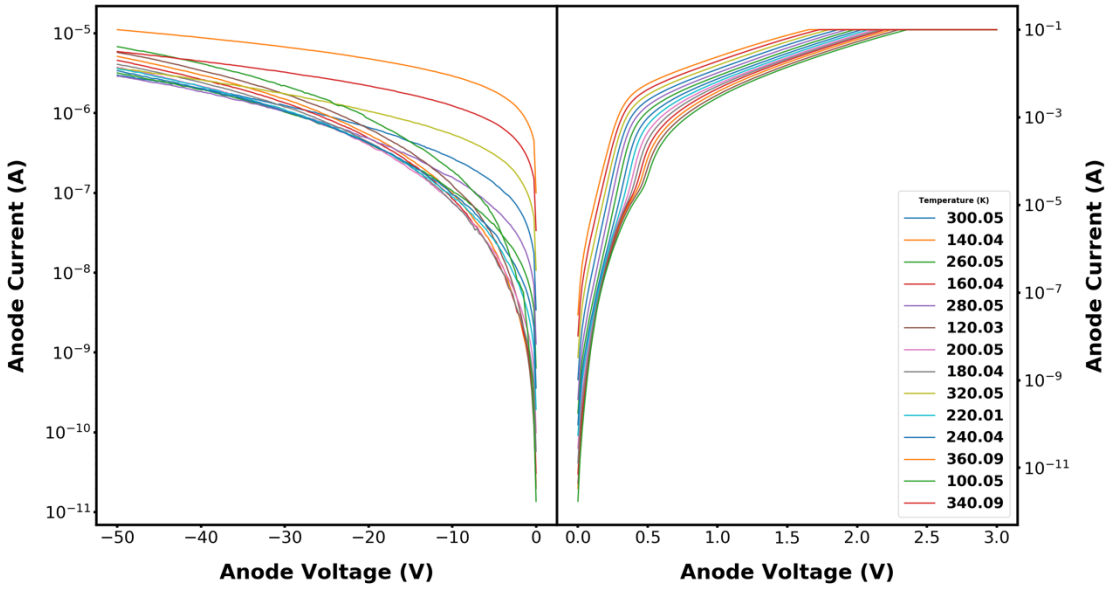
Although in-situ results were a useful tool for understanding how devices degraded with time, the post-stress characterization provided more definitive results since a wider temperature range could be achieved for I-V-T measurements. The same methods used for pre-stress characterization were applied on all devices that did not fail during stress testing to produce a set of post-stress I-V-T plots, Richardson plots, and forward resistance versus temperature plots.

Only device 322 failed during stress testing and failure occurred within the last hour of stressing. Cause of failure was determined to be from a combination of device characteristics and stress conditions. Device 322 had the highest pre-stress series resistance, was held at the highest of the three stress temperatures, 50 °C, and was subjected

to the highest current of 2.2 A. All these likely compounded causing the device to fail via a destructive thermal failure mechanism.

1. Post-stress I-V-T Measurements

Post-stress I-V-T measurements confirmed the changes observed through in-situ measurement to reverse leakage current for all devices. The reverse leakage currents had increased by two orders of magnitude when compared to pre-stress measurements, regardless of classification as SD or DD. The impact of temperature on the reverse leakage current and saturation current was identical to the pre-stress characterizations, increasing each as temperature increased, as shown by Figure 60 for device 179.

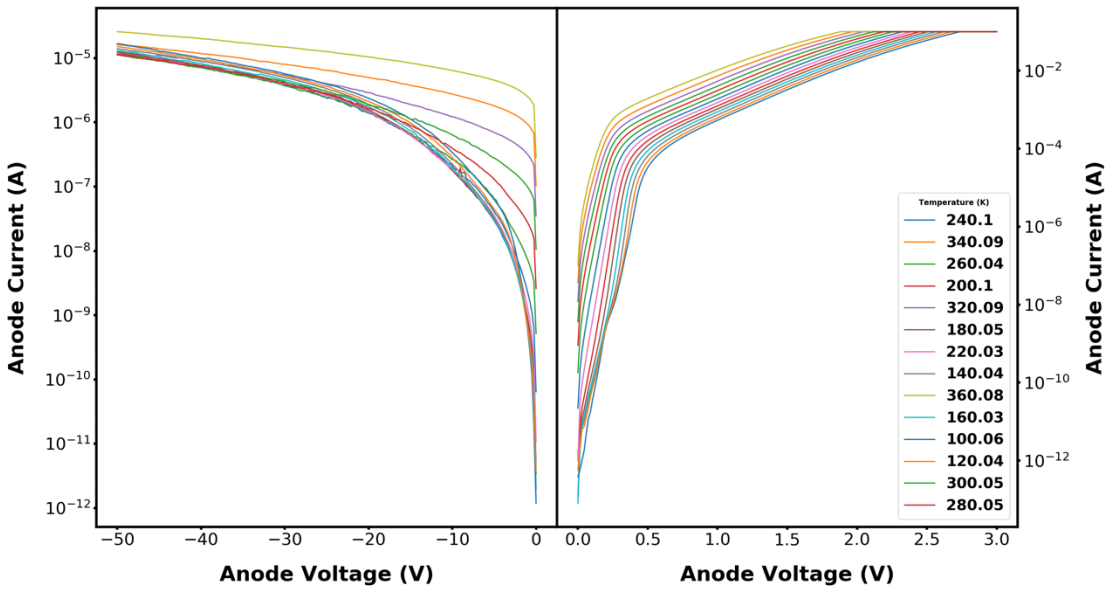


Reverse bias (left) and forward bias (right)

Figure 60. Device 179 (SD) post-stress I-V-T plot

Yet the most interesting observation came from the low voltage regions of the forward bias plots for devices previously classified as DD. The apparent presence of DD characteristics and the two-step kink in the I-V curve, in most cases, completely disappeared after subjecting the device to high current density electrical stress, as shown

by Figure 61. If the two-step kink was present, it was only at the low temperature ranges, below 120 K.



Reverse bias (left) and forward bias (right)

Figure 61. Device 120 (DD) post-stress I-V-T plot

A reduction in overall barrier height could account for this observation. If the barrier height were reduced enough, thermionic emission through the Schottky diode would occur at lower voltages and temperatures. It could be high enough to drown out at additional current flowing through the region of lower barrier height which was previously observed and only disappeared at high enough temperatures that thermionic emission through the higher barrier drowned out the region of lower barrier height.

Increased inhomogeneity spread could also be a factor causing the patches to expand to the point that the surface of the Schottky diode appears to be more uniformly distributed. Although not explored in this research there are other current effects that could contribute to the additional currents remaining at low temperatures, such as electron tunneling.

Additional post-stress I-V-T plots can be found in Appendix G.

2. Post-stress Barrier Height Measurements

Post-stress Richardson plots showed a drastic reduction in barrier height for all devices. The average barrier height of the higher region, after stressing was 0.46 eV and was just shy of a 50 % reduction from the average barrier height prior to stress testing. The area of low barrier height experienced a similar shift, with a post-stress average of 0.15 eV, a 60 % reduction. Higher barrier height regions ranged between 0.34 eV and 0.54 eV while the lower regions were between 0.12 eV and 0.19 eV. Reduction of barrier heights was independent of SD or DD classification.

Barrier heights for device 179 can be seen in Figure 62.

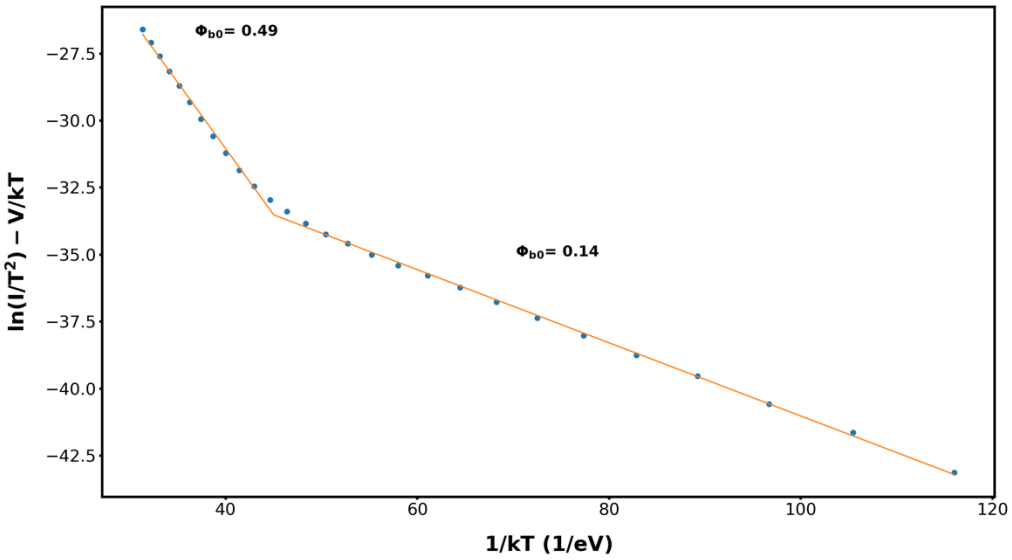


Figure 62. Device 179 (SD) post-stress Richardson plot

In addition to the effective lowering of the barrier height, the point of inflection between the two regions shifted to the right for most devices. Many of the post-stress results had this regional boundary appear at 60 1/eV, 20 1/eV higher when compared to the pre-

stress measurements where it normally occurred at or below 40 1/eV. This was observed for device 120, shown in Figure 63.

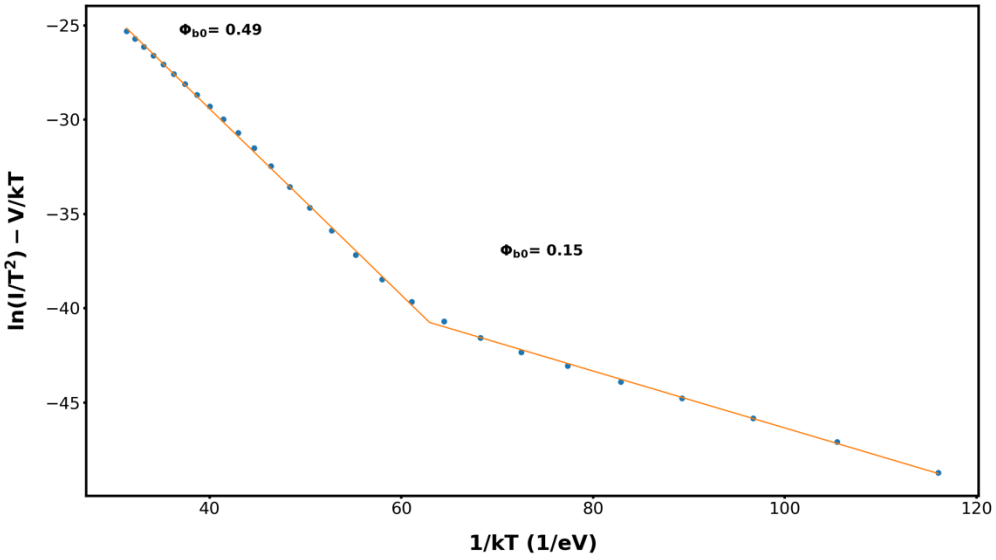


Figure 63. Device 120 (DD) post-stress Richardson plot

3. Post-stress Forward Resistance Measurements

Post-stress resistance versus temperature measurements displayed the same semi-parabolic relationship as the pre-stress measurements. While the in-situ resistance measurements generally showed an increase in resistance, post-stress resistance measurements showed a reduction in forward resistance values when compared to the pre-stress values for all devices. This phenomenon could be due to thermal annealing and the time it took to run subsequent I-V-T tests for devices after the stress test completed but more warrants further research.

As with the pre-stress resistance measurements, the parabolic low usually occurred between 150 K and 250 K and resistance values varied between 1 Ω and 3 Ω.

Figure 64 and Figure 65 show the plots of forward resistance as a function of temperature. The remaining resistance versus temperature plots are included in Appendix I.

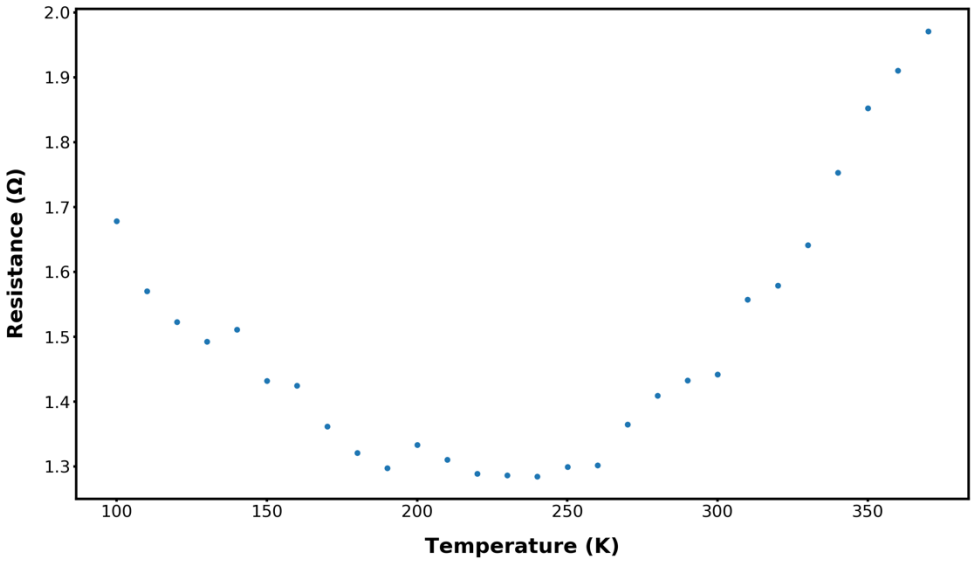


Figure 64. Device 179 (SD) post-stress R_{on} versus temperature plot

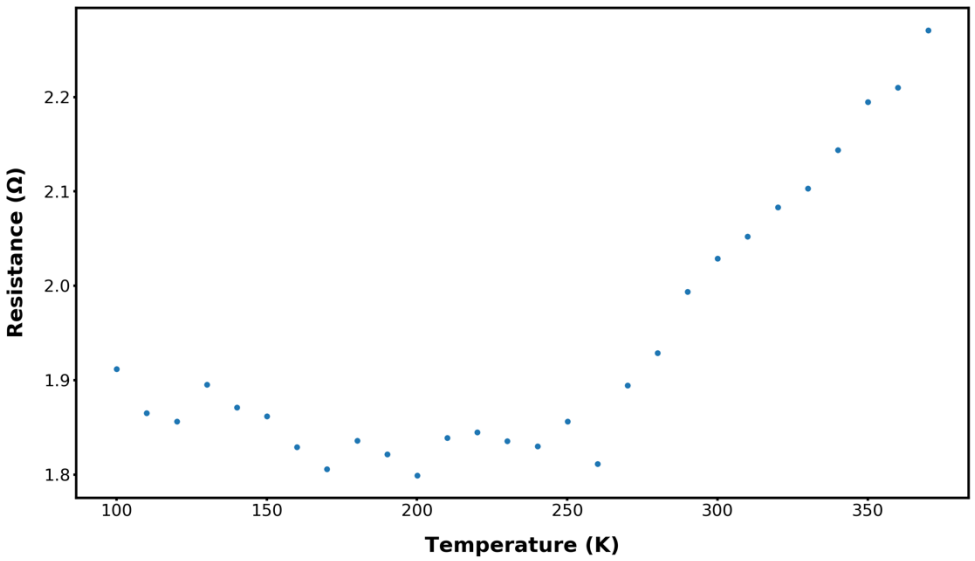


Figure 65. Device 120 (DD) post-stress R_{on} versus temperature plot

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VI. CONCLUSIONS AND FUTURE WORK

This chapter will summarize concluding remarks and present future work recommendations future work for the HTOL stress test system and the GaN Schottky research.

A. CONCLUSIONS

This research endeavor set out to accomplish two goals. The first was to design, construct and test an experimental HTOL stress test system. Though not the primary goal of this research, the HTOL stress test system was critical in enabling the types of desired stress measurements to be taken. The HTOL stress test system was successfully constructed and utilized to conduct a variety of lengthy stress tests on a batch of GaN Schottky diodes. It met the design criteria, making effective use of custom, modular, rack-mounted hardware with robust software-controlled automation. Furthermore, the system is durable and flexible by design and will hopefully be used by future students to conduct research both at the Naval Postgraduate School and the United States Naval Academy.

The second, and more important goal, was to study the effects of high current density electrical stress on commercial-grade vertical n-type Pd/GaN Schottky diodes. This goal was also achieved and in doing so lead to several useful conclusions can be made. BHI was present and a contributing factor for degradation of the tested devices. Tung theory of inhomogeneity provided a usable fit for the experimental data, though it was not exact and could be improved upon. Significant changes in key device characteristics were observed as a function of stress-time. Generally, devices subjected to current densities at or above 1.3 kA/cm^2 rapidly degraded prior to reaching steady state. The time constant for rate of degradation was between two and three hours. All devices, regardless of classification as SD or DD exhibited DD behavior at low temperatures, less than about 120 K. Most DD showed SD behavior at room temperature once subjected to a high enough currents and long stressing periods at, or once held at high enough temperature, above 360 K. Furthermore, there was no appreciable or observable impact of stress temperature on the devices, whether they were SD or DD. It is likely the effects of high current density

electrical stress overpowered the effects of external stress temperatures applied and this is another area for improvement from a test chamber perspective as well as an experimental design one by limiting the number of changing variables.

B. FUTURE WORK

Recommendations for future work includes modifications to the experimentally designed HTOL stress testing system and follow-on research regarding reliability studies with GaN Schottky diodes.

The experimental HTOL stress test system would primarily benefit by upgrading the stress testing modules and DUT chambers. The prototype design performed satisfactorily but had many drawbacks which given more time, and resources, could have been improved. A single TEC should be used instead of four independent TECs, allowing for greater temperature stability and control, and increased temperature range. Additionally, implementation of a physical hardware-based temperature controller would reduce the amount of software control required and provide a more accurate means of control. Although device self-heating was mitigated by the current design it was not perfect. Redesign of the cooling loop could make for a more stable environment for testing future devices. A water-based cooling cycle would be far superior to the nitrogen gas system used. And finally, rather than using 3D printed PLA material, upgrading the DUT chamber and internal housing components to Aluminum, or another metal, would improve the effectiveness of the modules to dissipate heat to the environment.

The GaN Schottky work conducted for this research would specifically benefit from further analysis of the data gathered in this experiment. The exploration of alternative analysis methods and curve fitting techniques could be used to refined calculations and achieve more conclusive results. Specifically, Tung model of analysis assumes a unimodal distribution which contradicts observed behavior of the double-diode effect. Using Tung model directly led to difficulties with curve fitting, especially in the lower voltage regions of devices with higher DD behavior. Since all devices exhibited some form of DD behavior, a bimodal distribution would be a more appropriate model.

Additionally, subjecting more devices to the same or similar methods of stress testing would allow for a better statistical analysis. The results from this research were merely preliminary and should be substantiated by increasing the sample size. Conducting constant current stress tests at 1.9 A and 2.0 A would provide a more complete picture for the results from this research. Modifying the stress tests to obtain more data points and over longer periods of time would be useful.

Finally, obtaining surface profile nanoscale images of the Schottky contact before and after stress testing would provide critical and definitive information regarding the presence of BHI and what the causes might be at the surface of the Schottky diodes. This could be achieved with atomic force microscopy, or more ideally scanning probe microscopy to directly characterize the Schottky barrier height. Finally, the use of smaller, unpackaged Schottky contacts devices under humidity control would remove any irregularities caused by the packaging process of the commercial devices.

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APPENDIX A. HTOL SYSTEM ADDITIONAL TEC CONVERGENCE CURVES

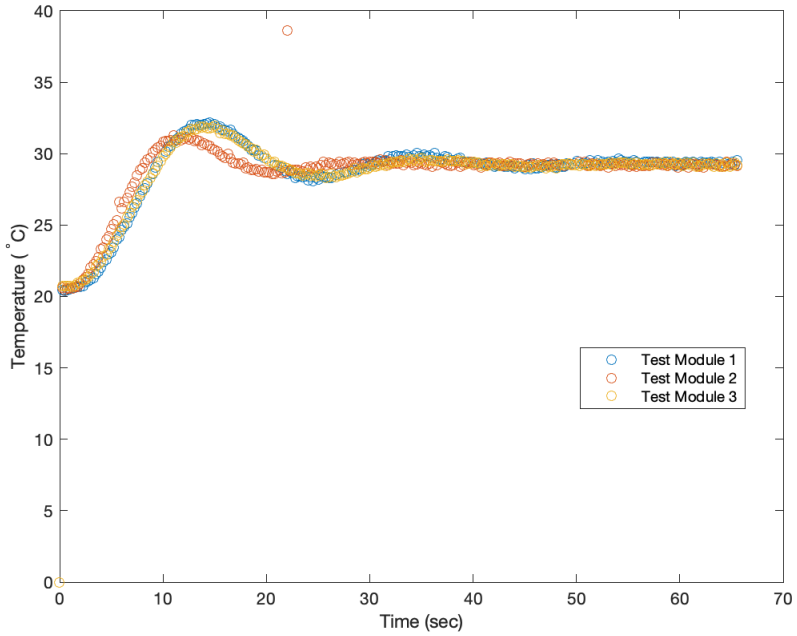

Figure 66. HTOL system TEC convergence from 20 ºC to 30 ºC.

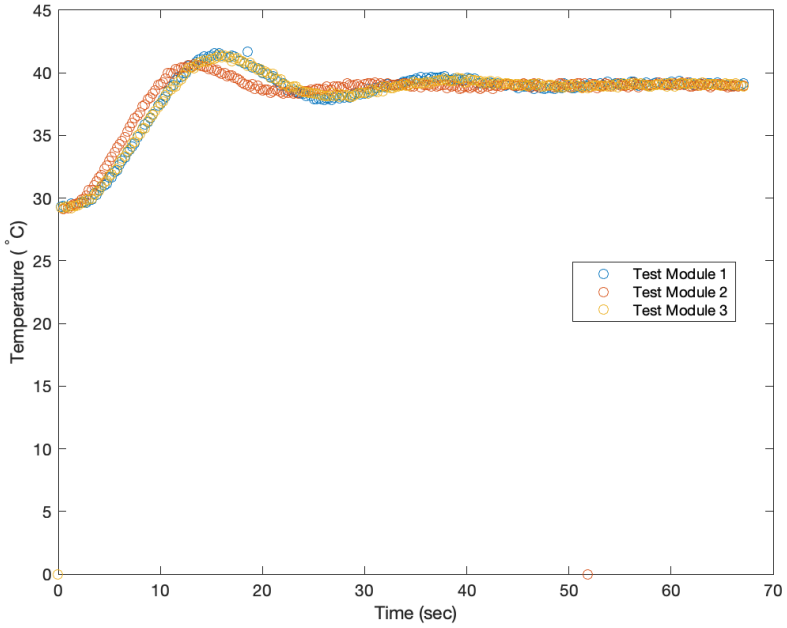

Figure 67. HTOL system TEC convergence from 30 ºC to 40 ºC.

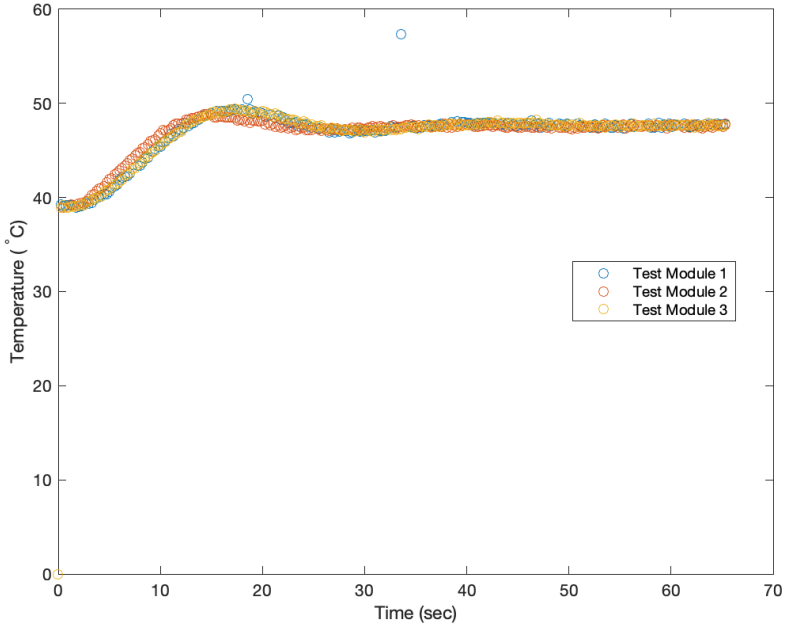

Figure 68. HTOL system TEC convergence from 40 ºC to 50 ºC.

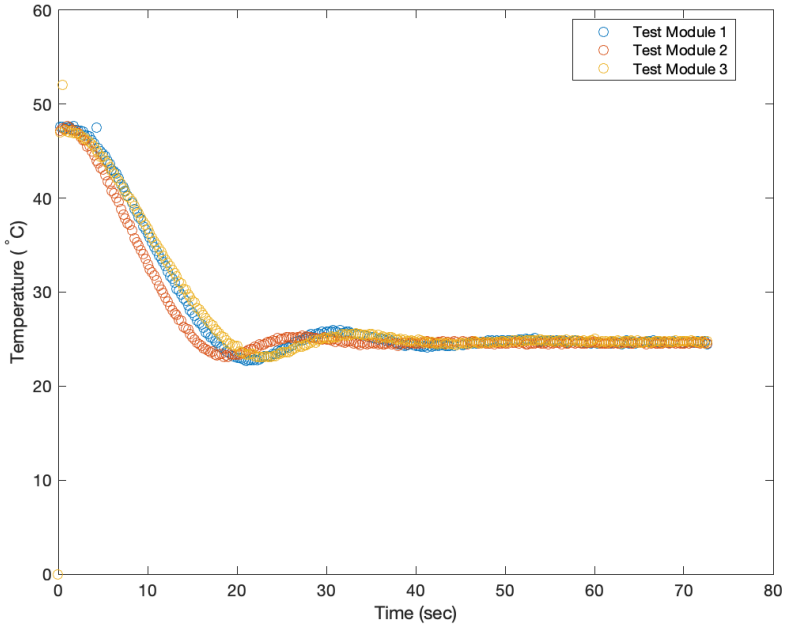

Figure 69. HTOL system TEC convergence from 50 ºC to 25 ºC.

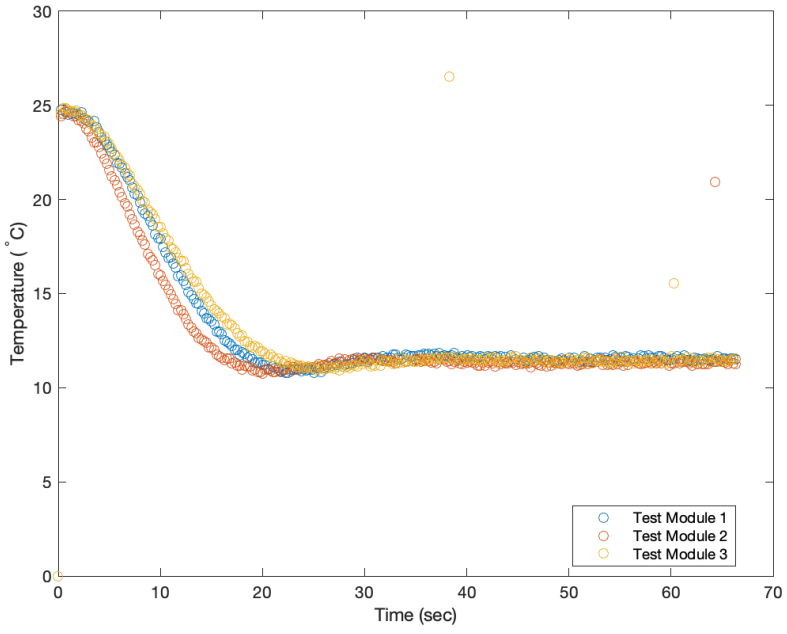

Figure 70. HTOL system TEC convergence from 25 ºC to 10 ºC.

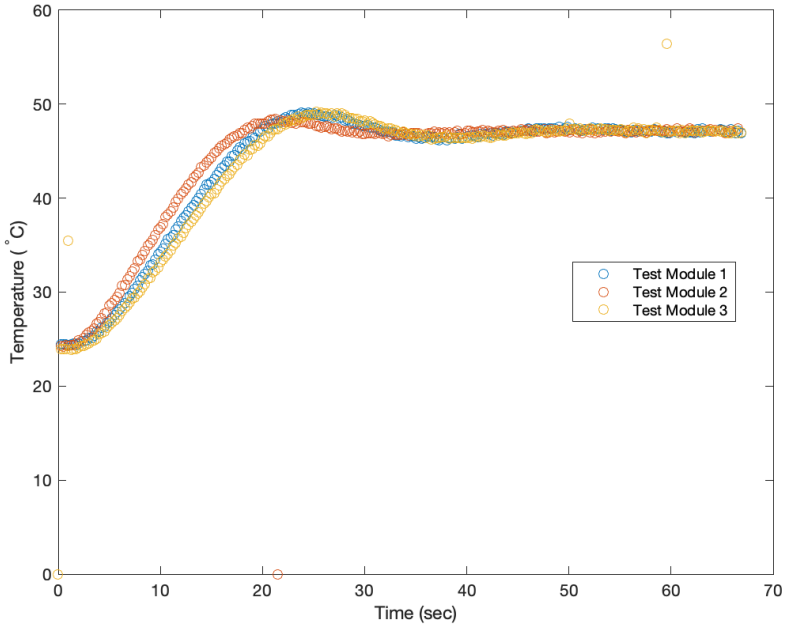

Figure 71. HTOL system TEC convergence from 25 ºC to 50 ºC.

APPENDIX B. COMPLETE TABLE OF CHARACTERIZED DEVICES

Table 8. Complete table of characterized Pd/GaN Schottky diodes, part 1 of 2

Lot #	Device #	Resistance (Ron)	Ron (mΩ*cm^2)	Ideality Factor (n)	Isat	Irev (@ -50 V)	Diode Notes (SD/DD)	Additonal Notes
NL	1	2.5	4	2.09	5.75E-09	2.20E-06	DD	
NL	2	3.52	5.632	1.2	3.76E-13	7.50E-08	SD	
NL	6	3.43	5.488	1.48	8.00E-12	2.20E-07	SD	
NL	9	2.94	4.704	1.84	1.08E-09	4.70E-07	DD	
NL	13	2.69	4.304	1.32	1.28E-12	1.60E-07	SD	
NL	16	3.09	4.944	1.34	6.44E-12	4.00E-07	SD	
NL	19	2.82	4.512	1.24	1.69E-11	7.00E-08	DD	
NL	20	2.79	4.464	1.25	1.07E-12	3.12E-08	SD	
NL	28	2.67	4.272	1.38	4.18E-12	8.00E-07	SD	
NL	30	2.89	4.624	1.09	1.28E-12	1.40E-08	SD	
NL	31	3.33	5.328	1.3	8.05E-13	1.10E-08	SD	
NL	35	3.14	5.024	1.95	1.17E-10	3.00E-06	SD/DD?	DD or SD Non-Linear?
NL	36	3.63	5.808	1.15	3.62E-13	3.75E-08	SD	
NL	37	2.87	4.592	1.3	2.48E-12	1.70E-08	SD	Non-linear
NL	43	2.1	3.36	1.34	8.57E-13	2.60E-07	SD	
1	11	2.02	3.232	1.65	8.21E-11	6.00E-07	SD/DD?	DD or SD Non-Linear?
1	17	2.21	3.536	1.62	2.65E-11	2.20E-07	SD/DD?	DD or SD Non-Linear?
1	19	3.16	5.056	1.24	8.97E-12	8.00E-06	SD/DD?	DD or SD Non-Linear?
1	20	2.52	4.032	2.07	2.76E-09	9.00E-06	DD	
1	22	3.15	5.04	1.29	5.14E-12	2.10E-06	SD	
1	23	2.12	3.392	1.25	3.71E-13	6.00E-09	SD	
1	27	2.83	4.528	1.61	3.74E-11	2.20E-06	SD	Non-linear
1	28	2.88	4.608	1.21	1.84E-12	3.50E-08	SD	
1	29	2	3.2	1.19	1.37E-12	5.20E-07	SD	
1	30	2.95	4.72	1.48	1.93E-11	2.10E-07	SD	Non-linear
1	31	2.54	4.064	1.14	1.14E-12	3.75E-07	SD	
1	34	3.85	6.16	1.36	7.58E-12	4.50E-06	SD	Non-linear
1	35	2.99	4.784	1.69	1.17E-10	5.00E-07	SD/DD?	DD or SD Non-Linear?
1	39	2.67	4.272	1.27	6.63E-12	5.00E-07	SD	
1	40	3.61	5.776	2.07	1.03E-09	2.50E-06	DD	
1	43	1.88	3.008	1.13	7.47E-13	2.10E-09	SD	
1	44	2.03	3.248	1.74	1.06E-09	1.30E-06	DD	
1	47	1.87	2.992	1.17	1.35E-12	5.00E-08	SD	
1	49	2.25	3.6	1.95	8.60E-09	7.00E-08	DD	
1	52	3.18	5.088	1.46	9.42E-09	5.50E-07	SD	Non-linear
1	58	2.73	4.368	1.53	1.40E-10	1.80E-06	SD/DD?	DD or SD Non-Linear?
1	62	2.67	4.272	1.25	2.47E-12	4.34E-08	SD	
1	64	1.99	3.184	1.84	2.07E-10	7.00E-07	SD	Non-linear
1	65	2.6	4.16	1.7	6.25E-10	1.40E-06	DD	Noisy Rev Char
1	66	2.22	3.552	1.61	1.22E-11	7.60E-06	SD	Non-linear
1	68	3.47	5.552	1.33	2.49E-12	4.00E-08	SD	
1	75	3.16	5.056	1.18	1.69E-12	7.00E-08	SD	
1	76	3.07	4.912	2.18	3.49E-10	7.00E-07	DD	
1	78	2.51	4.016	2.02	1.09E-09	4.50E-07	DD	
1	79	2.14	3.424	1.33	1.98E-11	4.60E-08	SD/DD?	DD or SD Non-Linear?
2	6	3.58	5.728	1.3	2.50E-11	6.00E-07	SD	Non-linear
2	7	2.34	3.744	1.19	6.16E-12	2.40E-07	SD	
2	8	2.92	4.672	1.7	4.84E-11	1.20E-07	SD/DD?	DD or SD Non-Linear?
2	9	2.74	4.384	1.37	5.77E-12	1.10E-07	SD	Non-linear. Noisy Rev Char
2	10	2.2	3.52	1.21	3.70E-12	1.40E-07	SD	
2	15	3.22	5.152	1.34	3.73E-12	8.00E-08	SD	Non-linear
2	16	2.02	3.232	1.16	3.16E-12	1.10E-07	SD	Noisy Rev Char
2	17	2.85	4.56	1.36	2.82E-12	2.20E-07	SD	Non-linear
2	19	1.81	2.896	1.15	3.14E-12	1.40E-07	SD	

Table 9. Complete table of characterized Pd/GaN Schottky diodes, part 2 of 2

Lot #	Device #	Resistance (Ron)	Ron (mΩ*cm^2)	Ideality Factor (n)	Isat	Irev (@ -50 V)	Diode Notes (SD/DD)	Additonal Notes
2	23	2.84	4.544	1.39	3.24E-12	5.80E-08	SD	Non-linear
2	25	2.68	4.288	1.61	9.40E-10	2.20E-07	DD	
2	29	2.64	4.224	1.13	3.26E-13	2.10E-09	SD	
2	31	2.81	4.496	1.17	2.82E-12	2.80E-07	SD	
2	33	3.8	6.08	1.31	4.30E-11	3.25E-06	DD	
2	35	2.99	4.784	1.31	6.40E-12	8.50E-08	SD	
2	38	2.47	3.952	1.13	2.06E-13	5.00E-10	SD	
2	39	2.26	3.616	1.31	1.30E-12	8.70E-08	SD	
2	48	2.57	4.112	1.99	2.07E-09	4.60E-08	DD	
2	49	2.41	3.856	1.15	4.84E-13	1.30E-06	SD	Noisy Rev Char
2	51	4.82	7.712	1.54	1.43E-11	2.20E-07	SD	Non-linear
2	61	2.6	4.16	1.29	6.53E-13	3.25E-08	SD	
2	63	3.17	5.072	1.23	6.62E-13	1.00E-07	SD	
3	5	2.28	3.648	2.08	6.25E-10	4.30E-06	DD	
3	6	3.15	5.04	1.38	2.32E-12	1.50E-07	SD	Non-linear
3	7	2.47	3.952	1.12	5.66E-13	6.50E-07	SD	Noisy Rev Char
3	9	2.52	4.032	1.21	6.22E-12	3.25E-06	SD	Noisy Rev Char
3	10	3.2	5.12	2.21	3.90E-09	1.60E-06	DD	
3	11	3.12	4.992	1.25	2.11E-11	2.60E-08	SD	
3	15	2.85	4.56	1.23	1.50E-12	7.00E-07	SD	
3	17	1.97	3.152	1.09	1.96E-12	2.20E-08	SD	
3	18	2.9	4.64	2.07	2.96E-10	1.40E-06	DD	
3	19	3.21	5.136	1.36	5.66E-12	1.50E-07	SD	Non-linear
3	20	3.37	5.392	1.6	9.03E-12	4.40E-08	SD	Non-linear
3	22	4.05	6.48	1.21	7.80E-13	2.60E-08	SD	
3	26	3.98	6.368	1.17	6.76E-13	5.80E-08	SD	
3	28	2.46	3.936	1.22	8.26E-12	9.00E-07	SD	
3	52	2.47	3.952	2.24	3.54E-09	9.50E-07	DD	
3	54	2.73	4.368	1.21	8.96E-13	4.00E-07	SD	
3	57	2.58	4.128	1.23	3.89E-12	1.70E-06	SD	
3	61	2.3	3.68	1.14	2.91E-12	1.60E-06	SD	Noisy Rev Char
3	62	3.2	5.12	1.12	6.99E-13	2.20E-09	SD	
3	63	3.13	5.008	1.2	3.39E-13	3.00E-09	SD	Noisy Rev Char
3	64	3.48	5.568	2	4.47E-09	7.70E-07	DD	Noisy Rev Char
11	21	2.65	4.24	1.34	5.23E-12	1.70E-07	SD	Non-linear
11	23	1.99	3.184	1.36	7.78E-11	2.00E-07	SD/DD?	DD or SD Non-Linear?
11	24	3.2	5.12	1.29	1.11E-11	2.50E-06	SD	
11	27	2.33	3.728	1.35	6.36E-12	1.05E-06	SD	Non-linear
11	31	2.22	3.552	1.34	1.67E-12	1.00E-08	SD	Non-linear
11	38	1.73	2.768	1.32	1.25E-11	8.40E-07	SD	Non-linear
11	41	3.24	5.184	1.3	3.22E-12	1.20E-07	SD	Non-linear
11	43	2.18	3.488	1.5	1.93E-10	2.60E-07	DD	Noisy Rev Char
11	49	3.66	5.856	2.63	1.08E-08	4.00E-07	DD	Noisy Rev Char
X	4	2.95	4.72	1.25	1.59E-12	8.50E-08	SD	
X	11	3.26	5.216	1.44	1.45E-11	8.00E-07	SD	Non-linear
X	14	2.71	4.336	1.39	2.01E-12	2.70E-07	SD	Non-linear
X	16	2.89	4.624	1.79	6.73E-09	3.00E-06	DD	
X	19	3.16	5.056	1.11	1.45E-12	1.50E-07	SD	Non-linear
X	20	3.5	5.6	1.21	7.23E-13	6.00E-08	SD	
X	23	3.28	5.248	1.06	1.22E-12	4.70E-08	SD	
X	26	2.64	4.224	1.41	2.07E-11	3.90E-06	SD	Non-linear
X	37	2.74	4.384	1.17	1.92E-12	1.20E-07	SD	
X	39	2.49	3.984	2.23	5.89E-09	2.90E-06	DD	
X	40	3.89	6.224	1.21	1.79E-12	1.25E-07	SD	
0	1	3.15	5.04	1.22	5.47E-13	5.00E-07	SD	Noisy Rev Char

APPENDIX C. INITIAL CHARACTERIZATION AND CLASSIFICATION I-V PLOTS

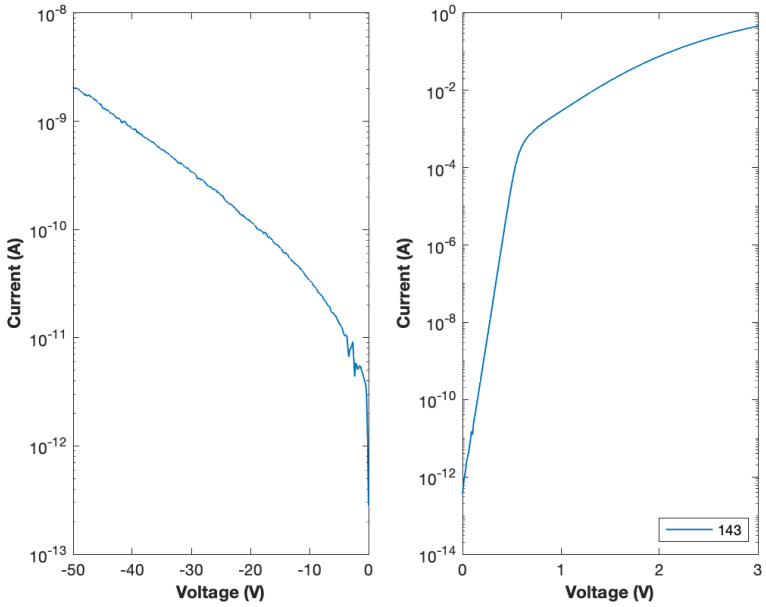

Figure 72. Device 143 I-V plot at room temperature

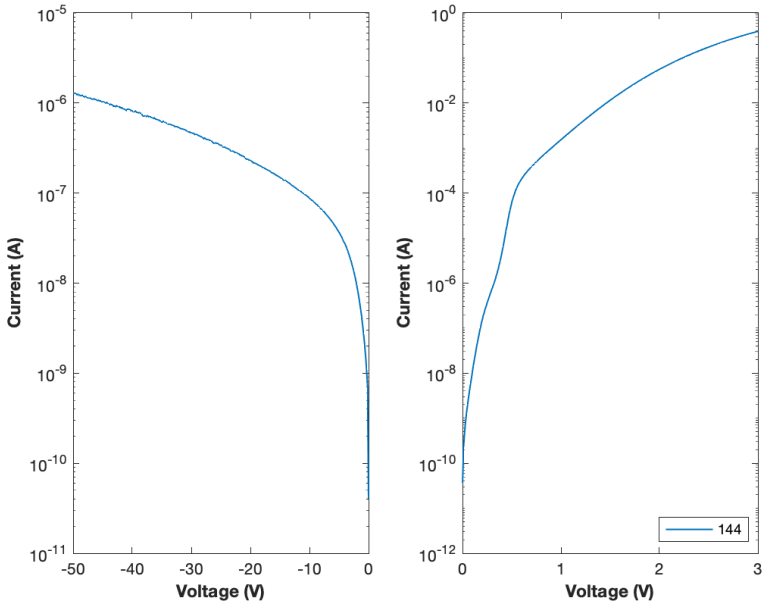

Figure 73. Device 144 I-V plot at room temperature

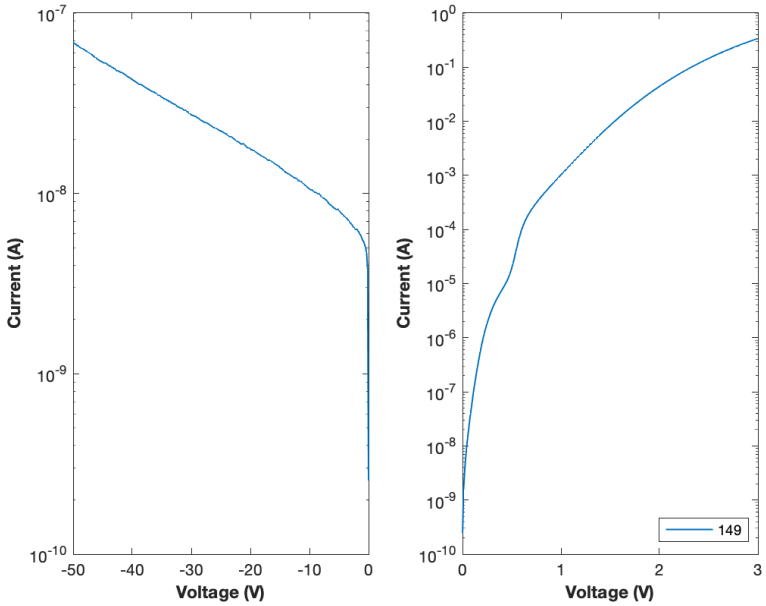

Figure 74. Device 149 I-V plot at room temperature

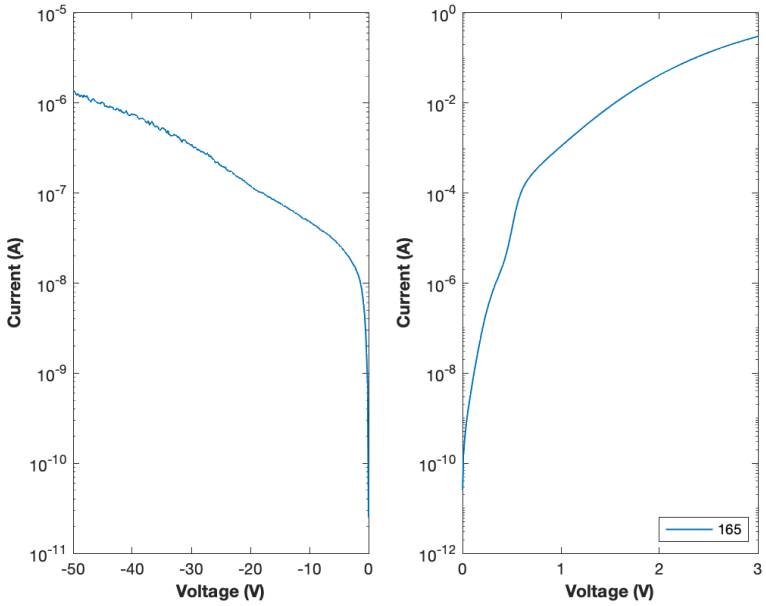

Figure 75. Device 165 I-V plot at room temperature

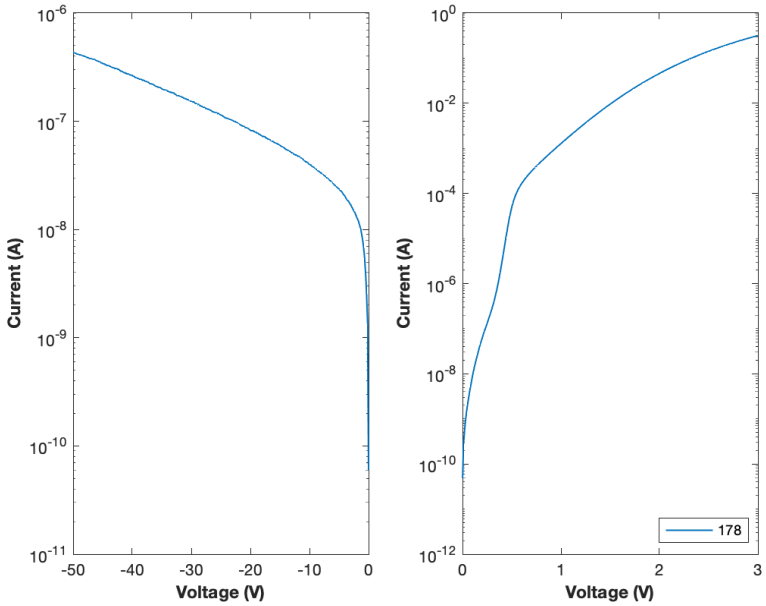

Figure 76. Device 178 I-V plot at room temperature

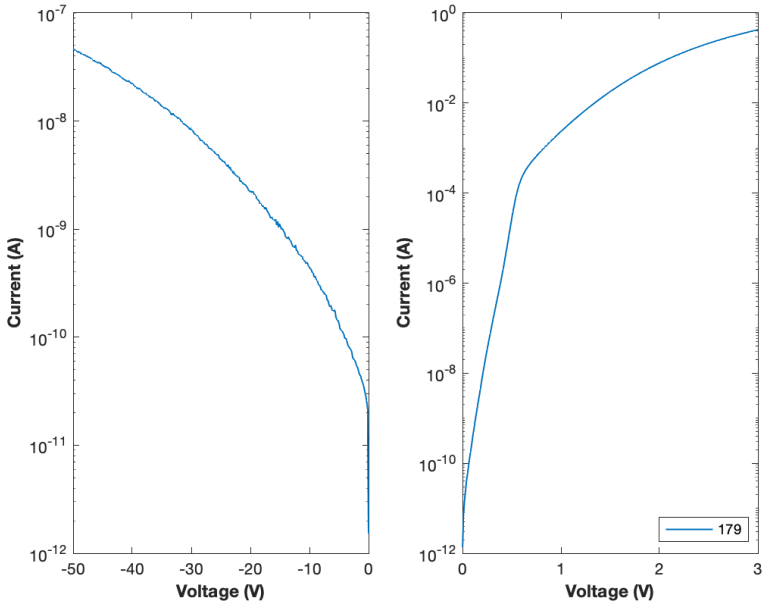

Figure 77. Device 179 I-V plot at room temperature

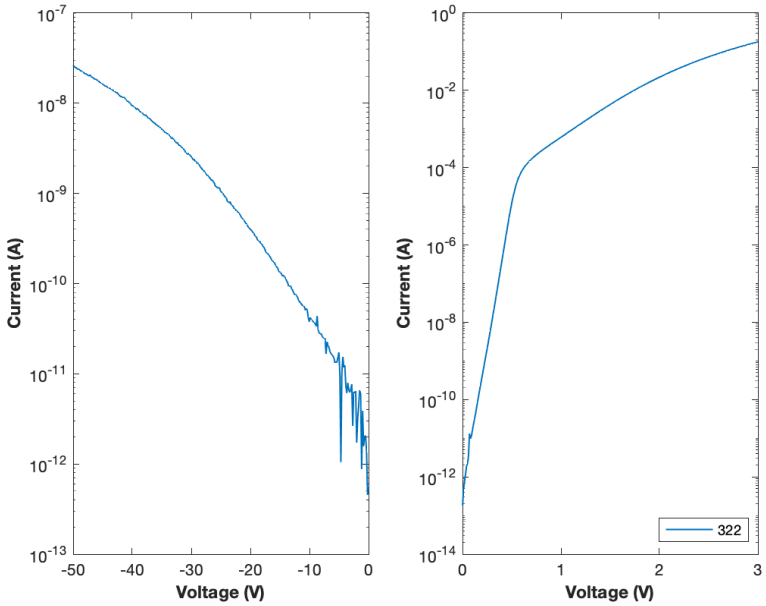

Figure 78. Device 322 I-V plot at room temperature

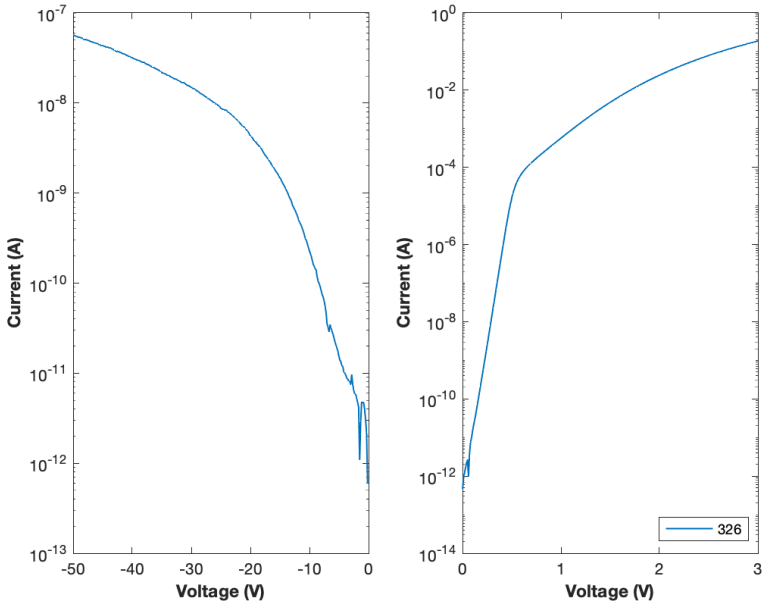

Figure 79. Device 326 I-V plot at room temperature

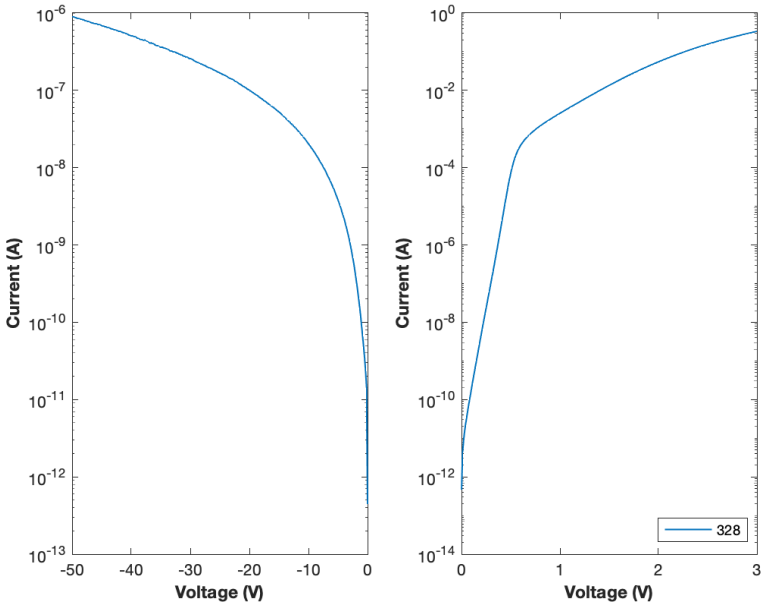

Figure 80. Device 328 I-V plot at room temperature

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APPENDIX D. PRE-STRESS I-V-T PLOTS

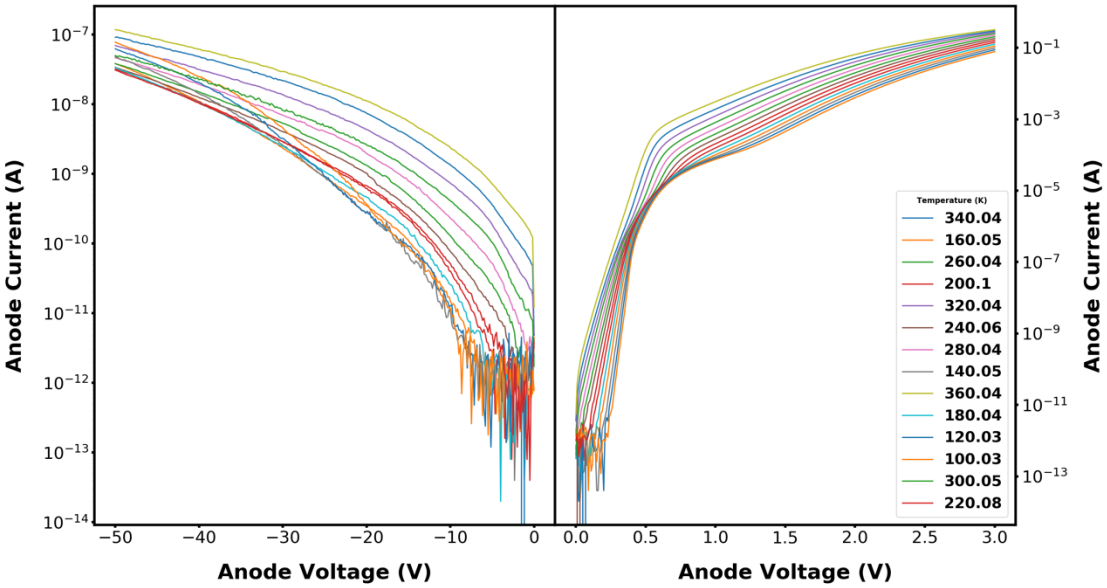

Figure 81. Device 19 pre-stress I-V-T plot

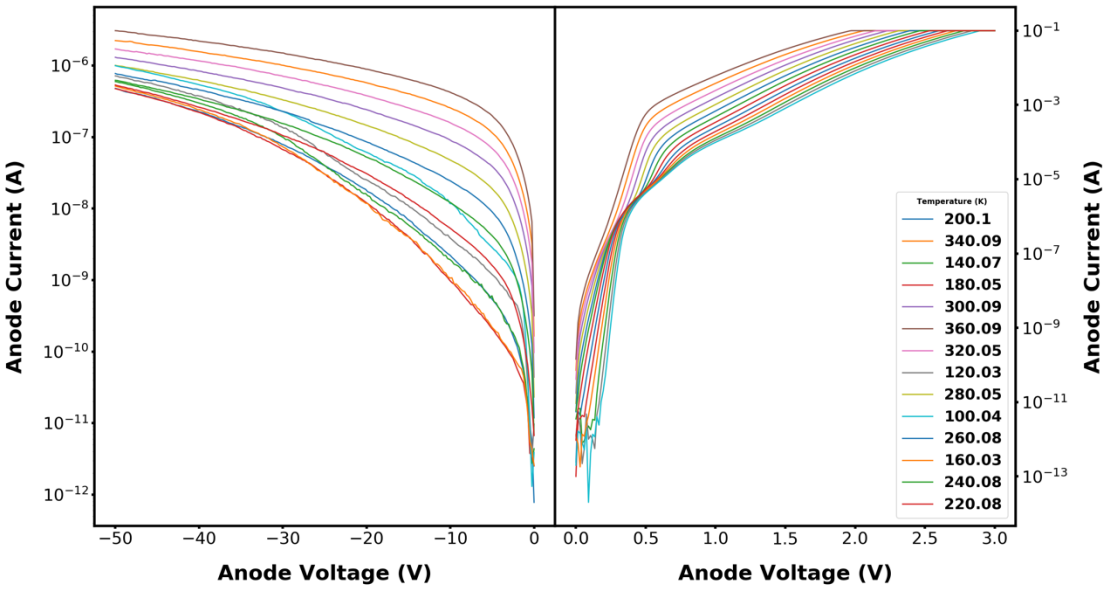

Figure 82. Device 144 pre-stress I-V-T plot

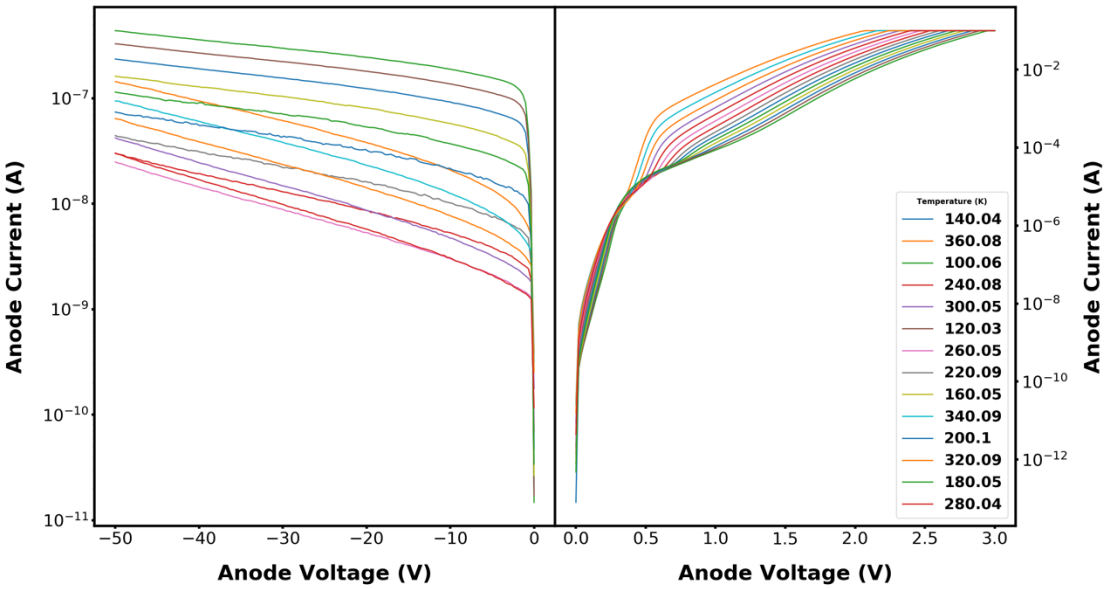

Figure 83. Device 149 pre-stress I-V-T plot

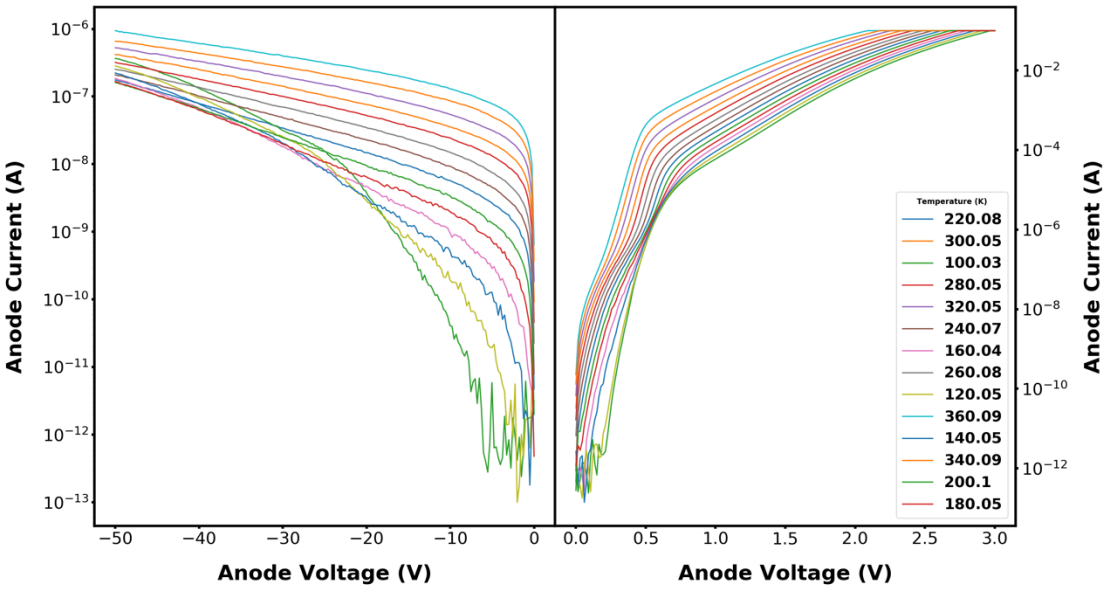

Figure 84. Device 178 pre-stress I-V-T plot

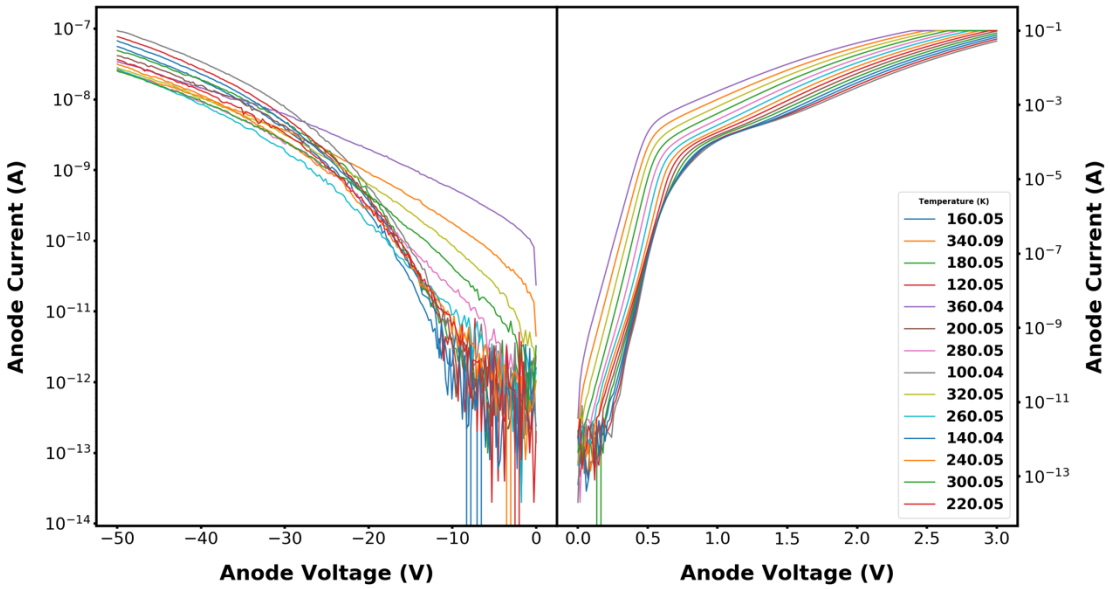

Figure 85. Device 322 pre-stress I-V-T plot

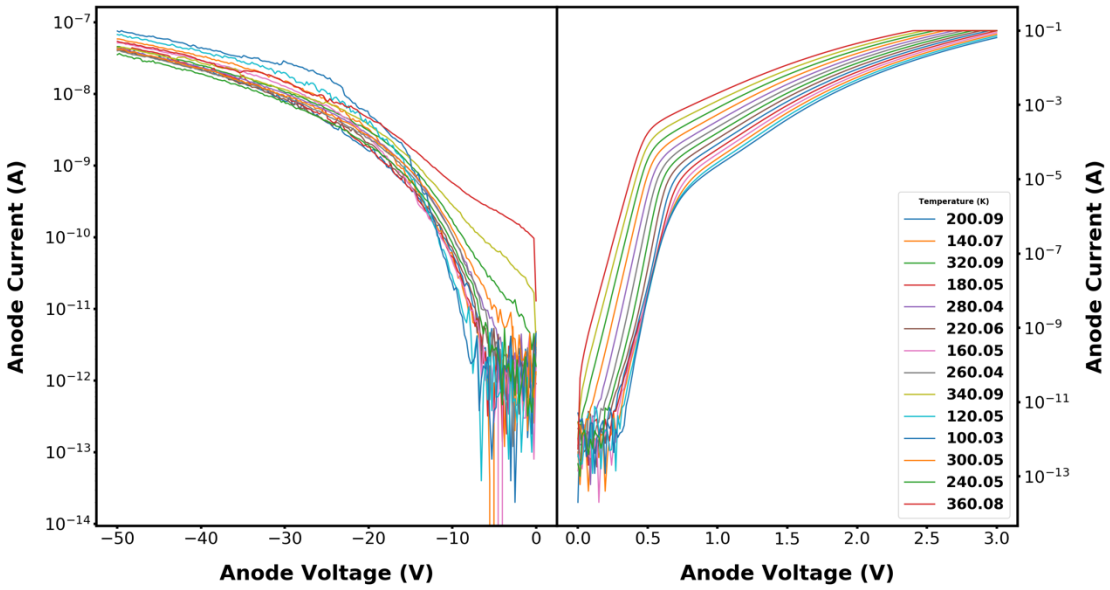

Figure 86. Device 326 pre-stress I-V-T plot

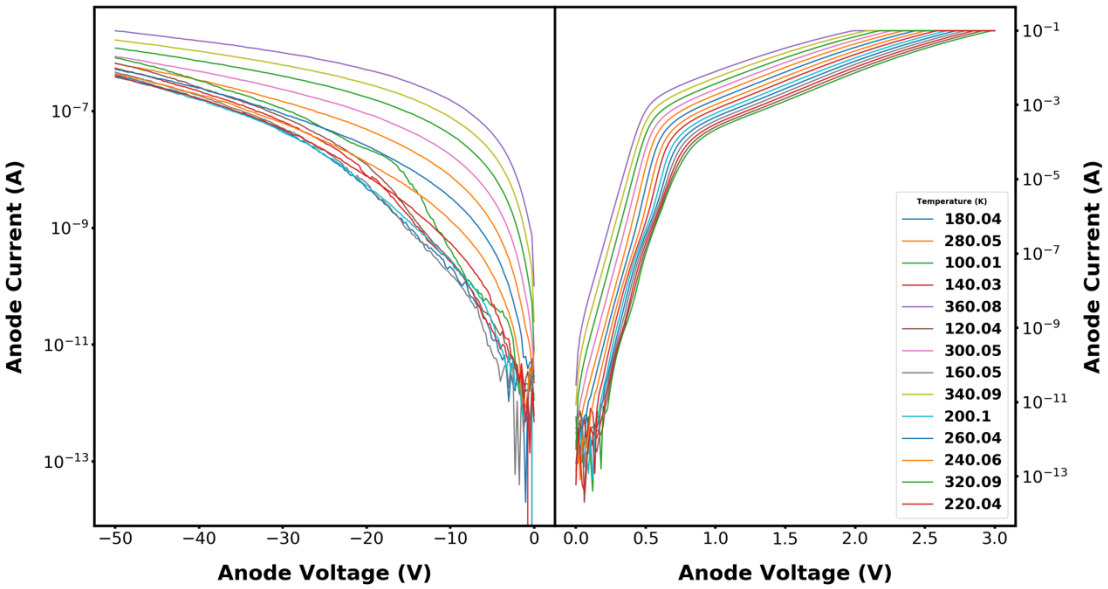

Figure 87. Device 328 pre-stress I-V-T plot

APPENDIX E. PRE-STRESS BARRIER HEIGHT MEASUREMENTS

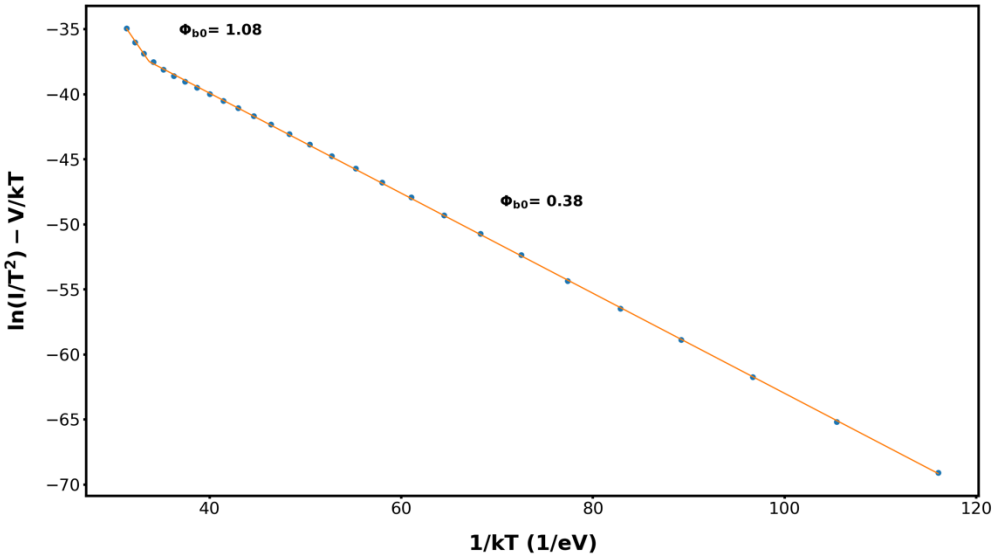

Figure 88. Device 19 pre-stress Richardson plot

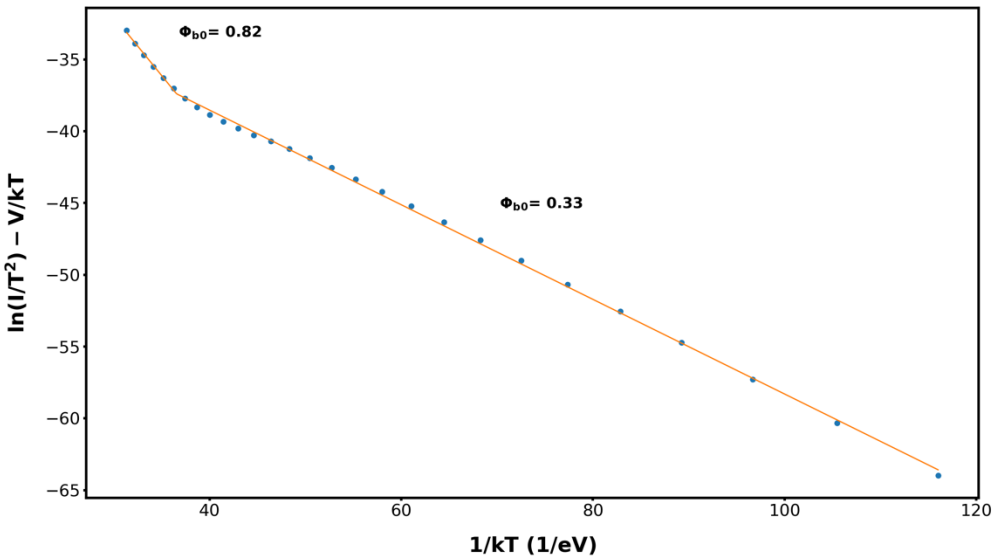

Figure 89. Device 144 pre-stress Richardson plot

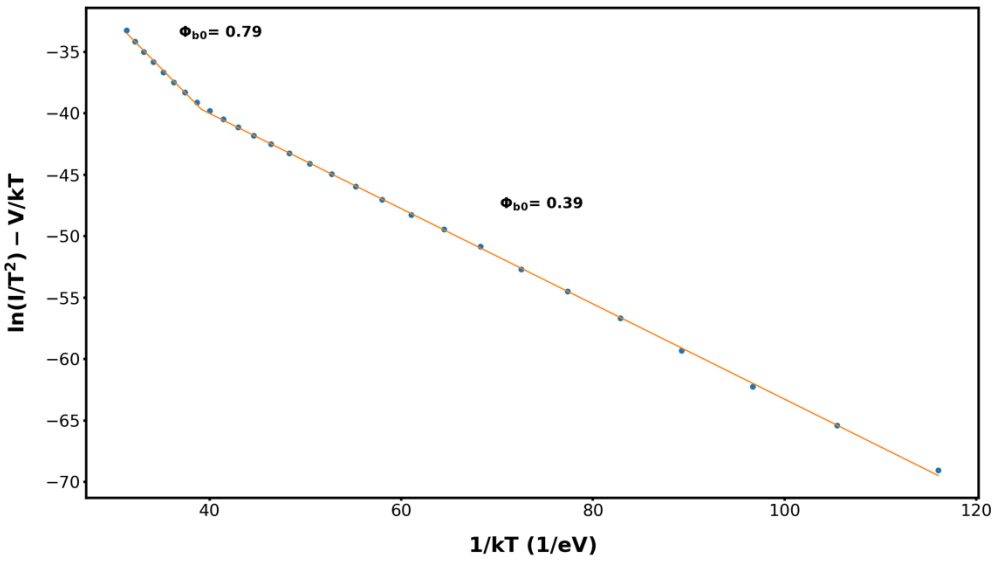

Figure 90. Device 178 pre-stress Richardson plot

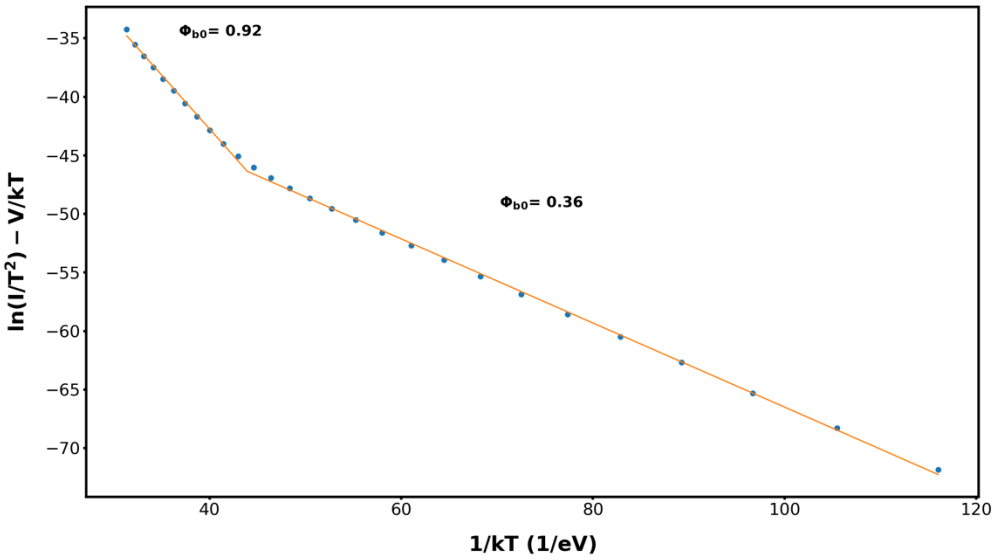

Figure 91. Device 322 pre-stress Richardson plot

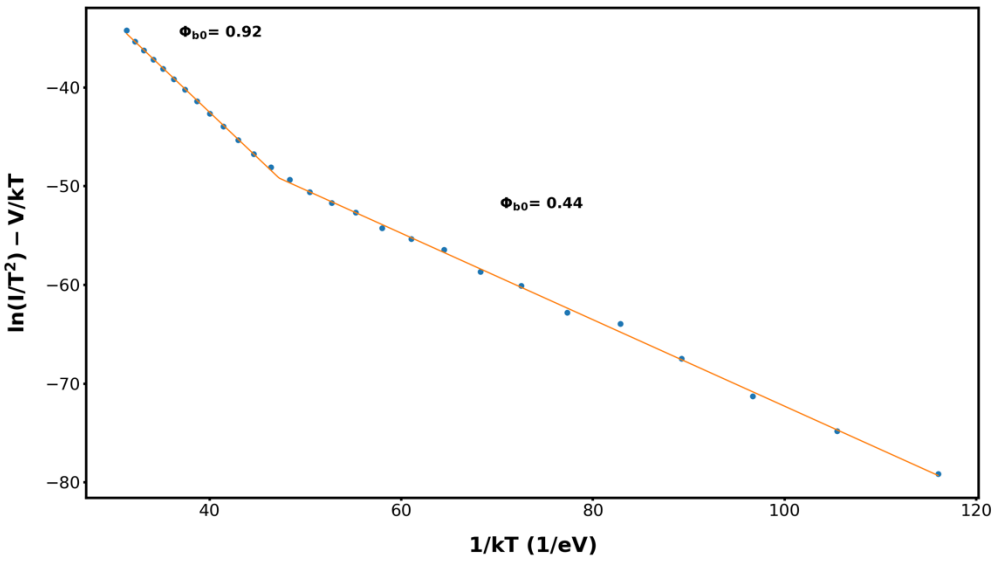

Figure 92. Device 326 pre-stress Richardson plot

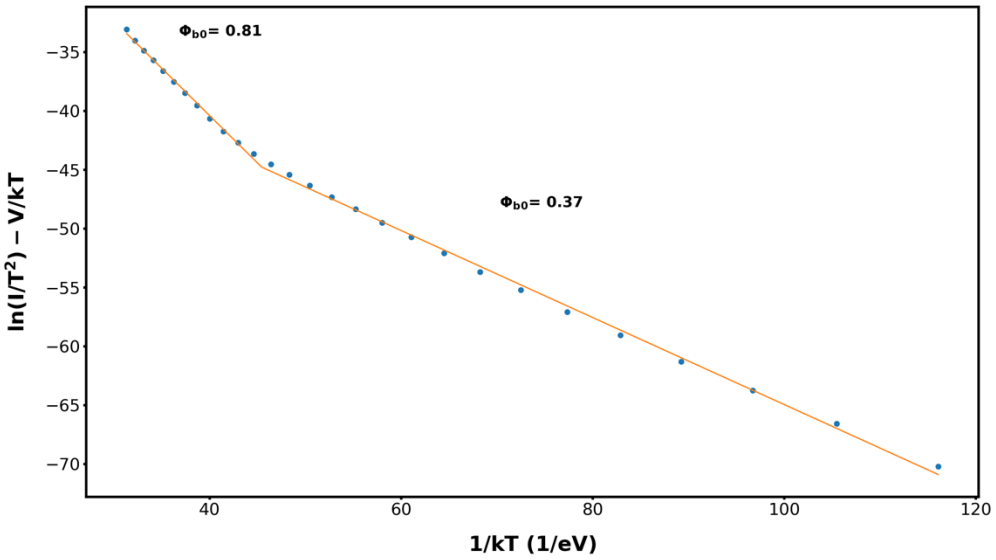

Figure 93. Device 328 pre-stress Richardson plot

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APPENDIX F. PRE-STRESS FORWARD RESISTANCE VERSUS TEMPERATURE MEASUREMENTS

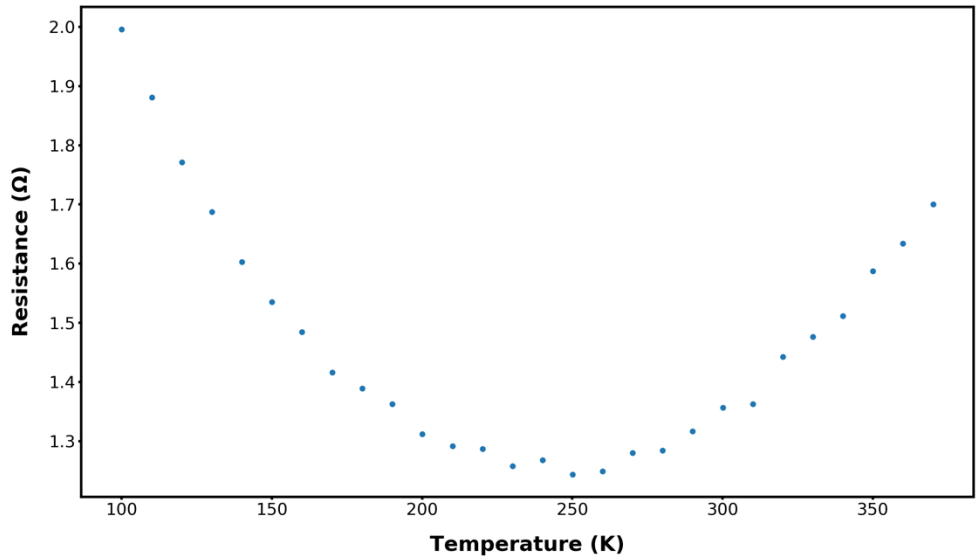

Figure 94. Device 19 pre-stress R_{on} versus temperature plot

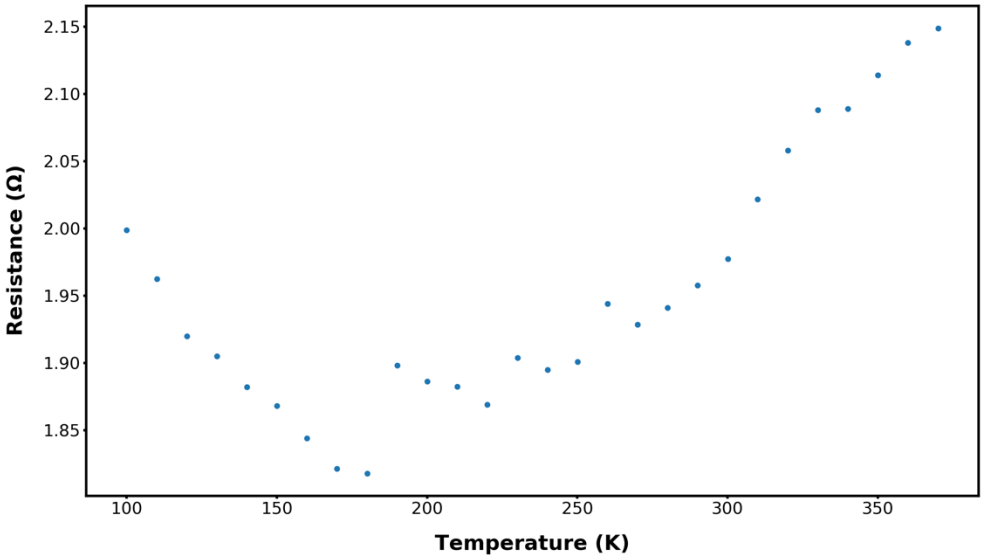

Figure 95. Device 144 pre-stress R_{on} versus temperature plot

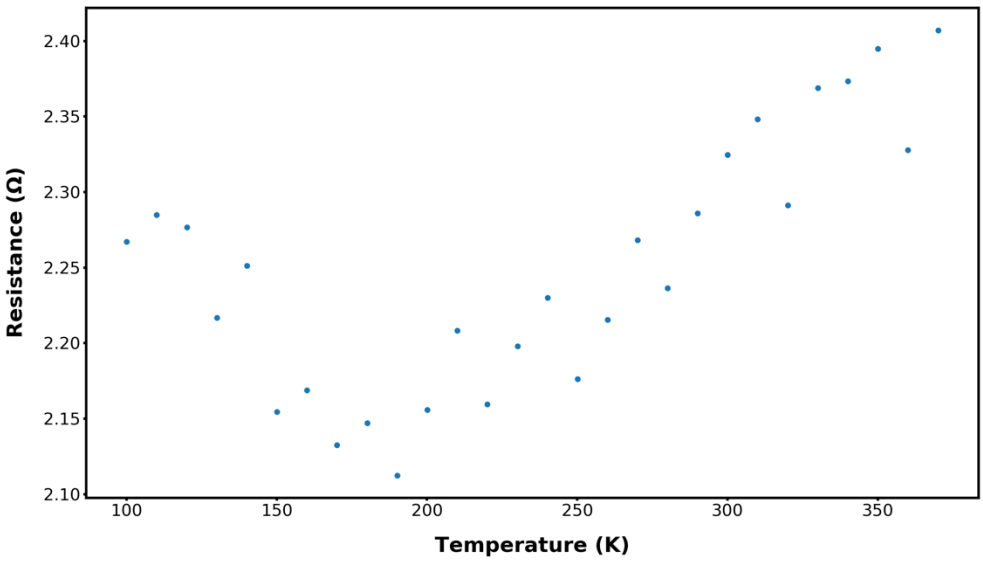

Figure 96. Device 149 pre-stress R_{on} versus temperature plot

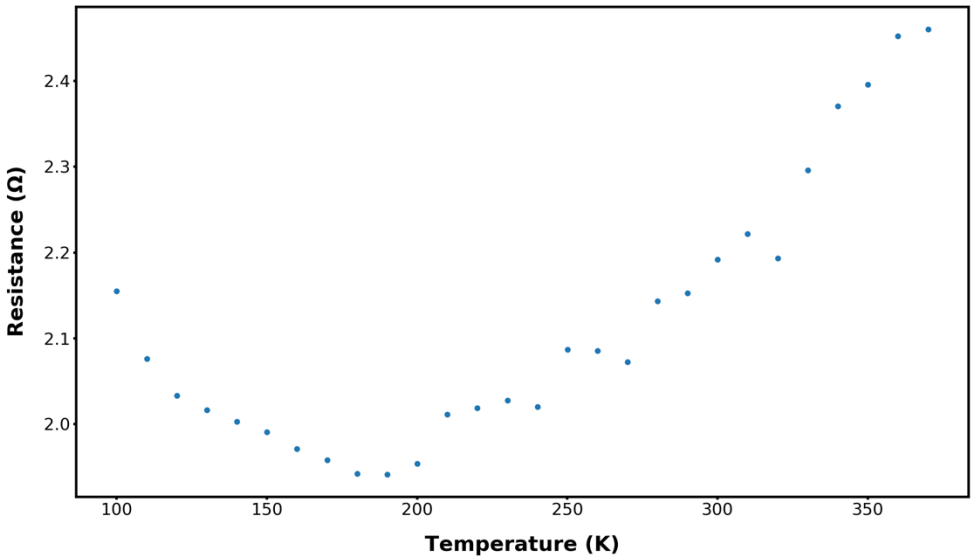

Figure 97. Device 178 pre-stress R_{on} versus temperature plot

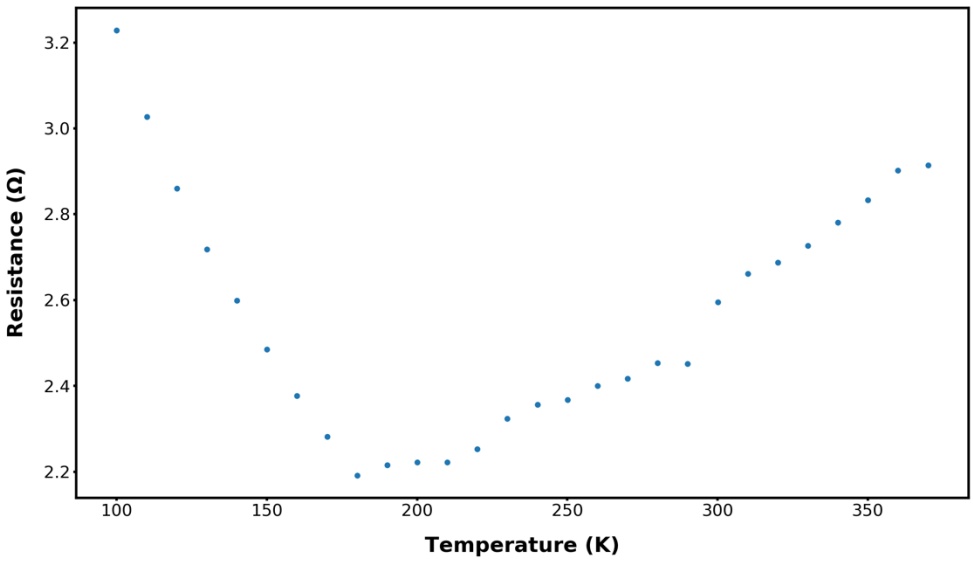

Figure 98. Device 322 pre-stress R_{on} versus temperature plot

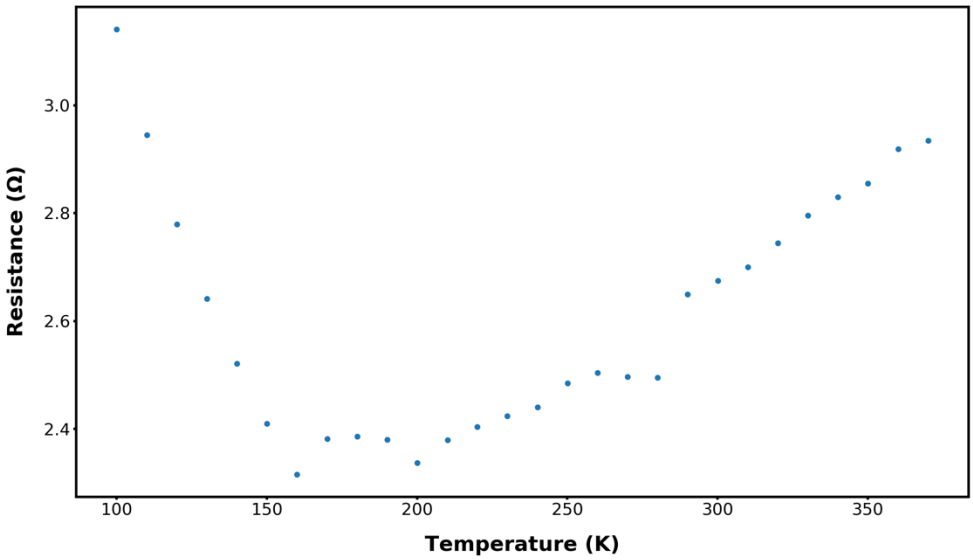

Figure 99. Device 326 pre-stress R_{on} versus temperature plot

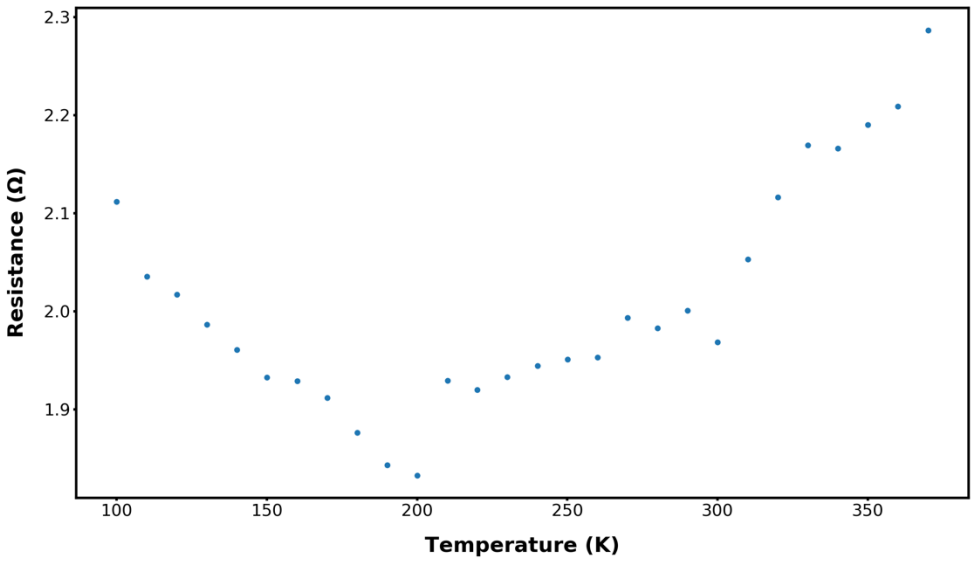

Figure 100. Device 328 pre-stress R_{on} versus temperature plot

APPENDIX G. POST-STRESS I-V-T PLOTS

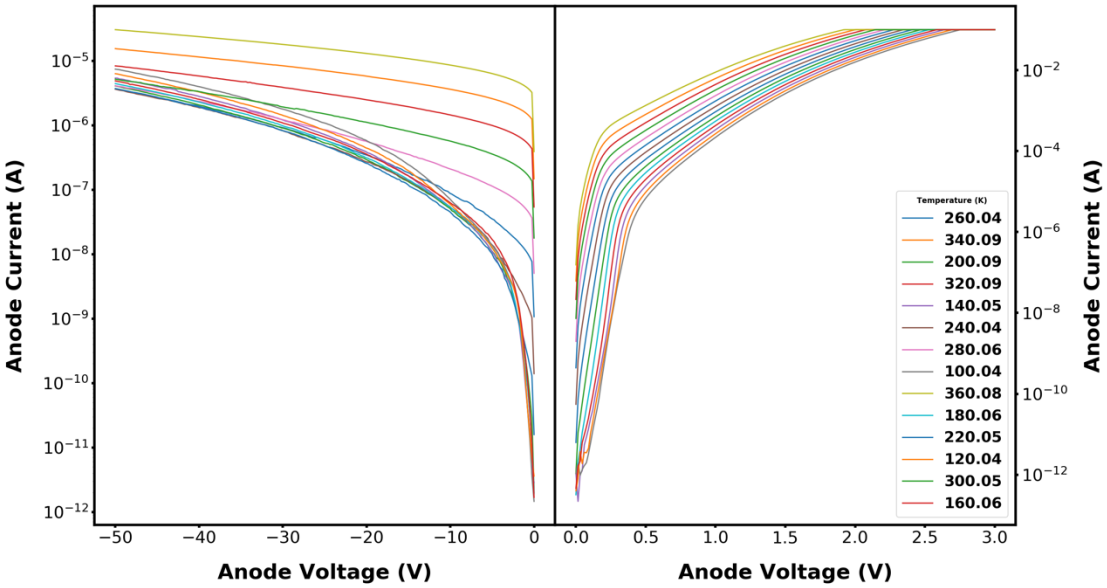

Figure 101. Device 19 post-stress I-V-T plot

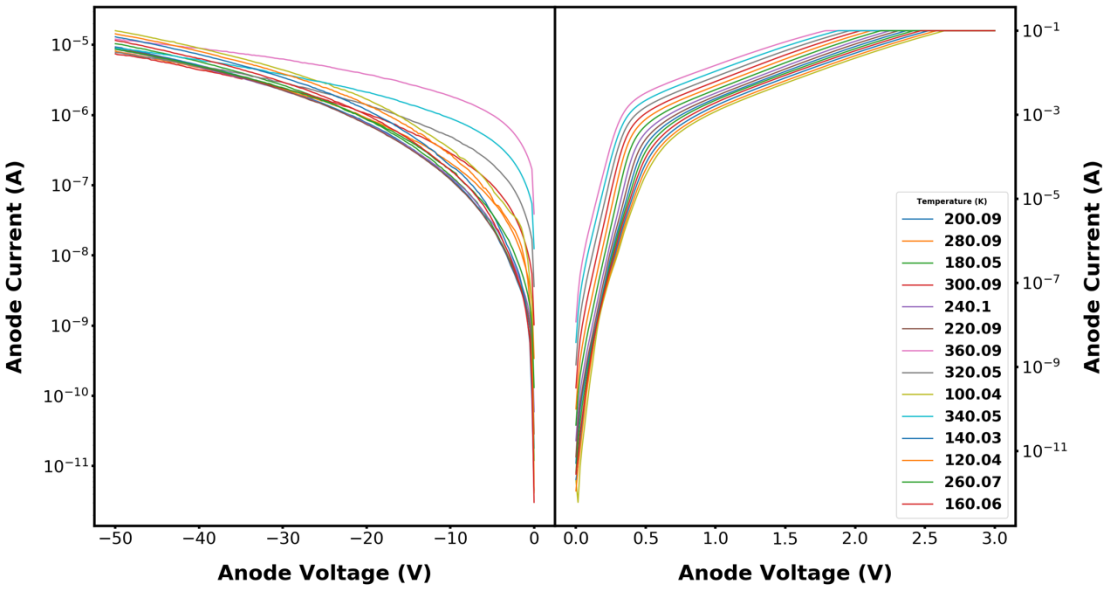

Figure 102. Device 144 post-stress I-V-T plot

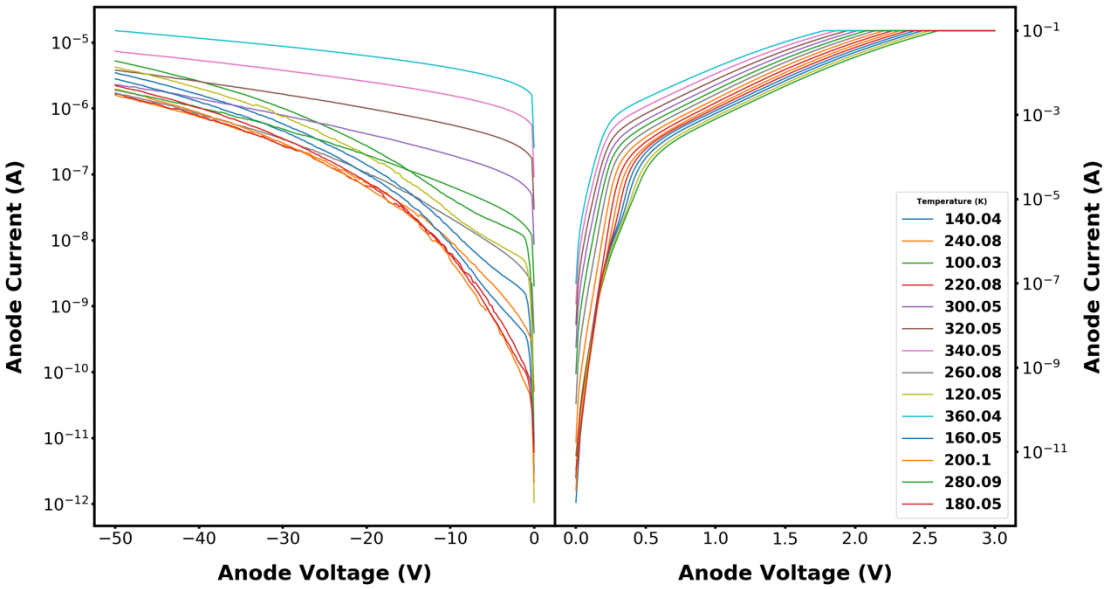

Figure 103. Device149 post-stress I-V-T plot

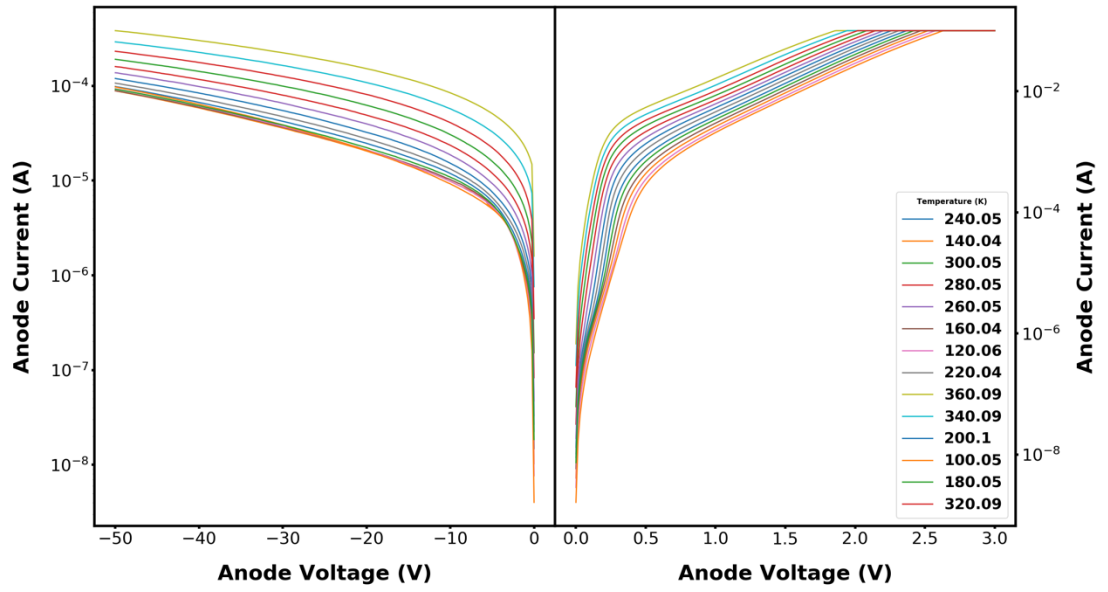

Figure 104. Device 178 post-stress I-V-T plot

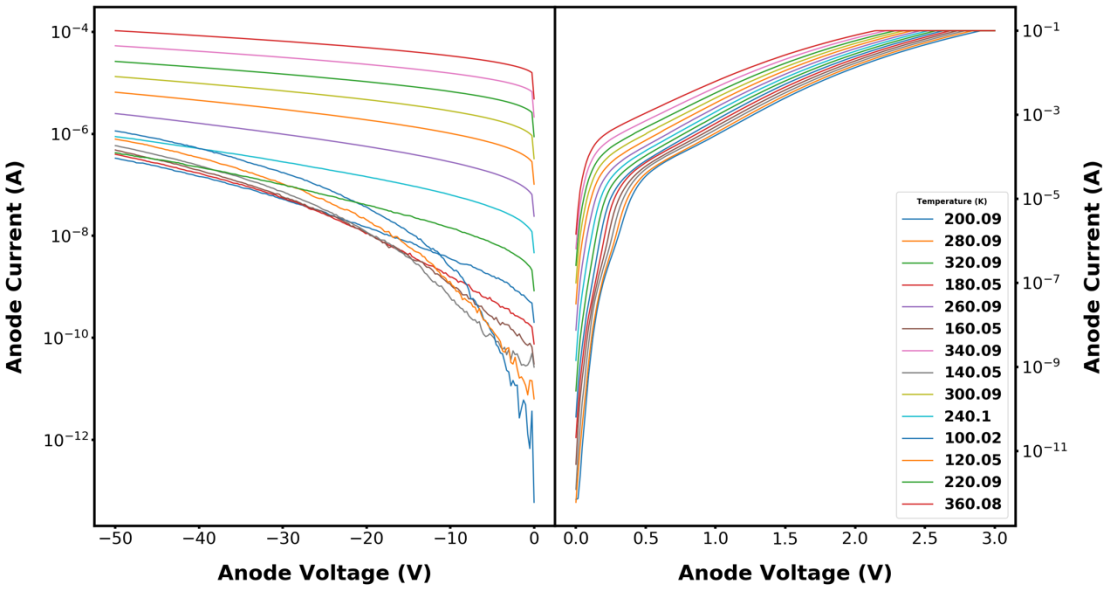

Figure 105. Device 326 post-stress I-V-T plot

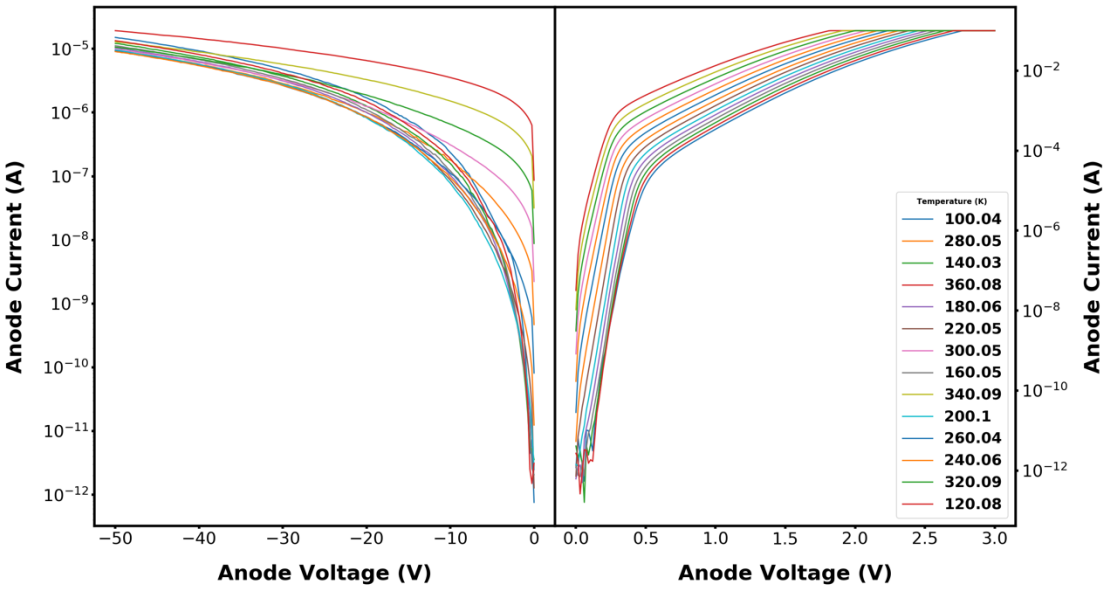

Figure 106. Device 328 post-stress I-V-T plot

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APPENDIX H. POST-STRESS BARRIER HEIGHT MEASUREMENTS

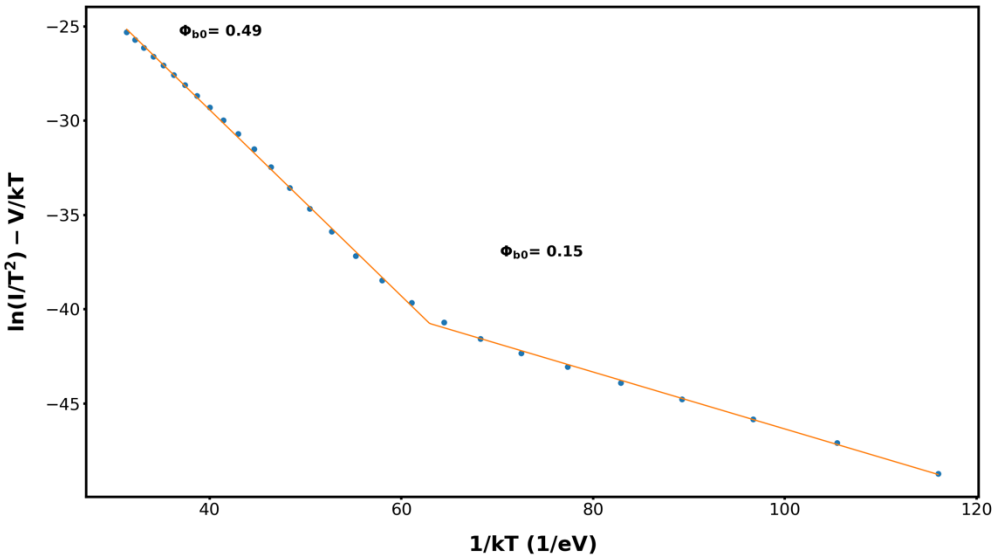

Figure 107. Device 19 post-stress Richardson plot

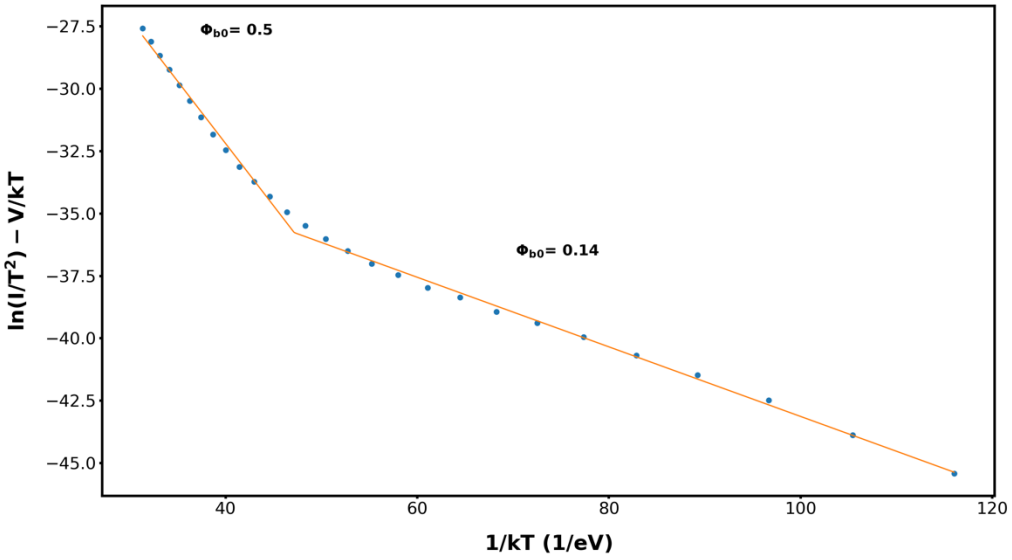

Figure 108. Device 144 post-stress Richardson plot

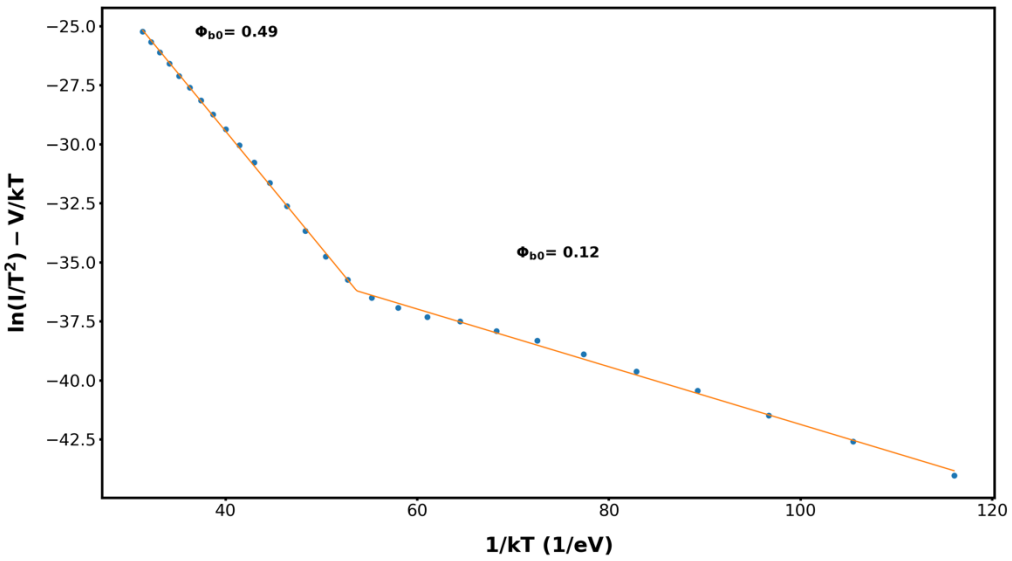

Figure 109. Device 149 post-stress Richardson plot

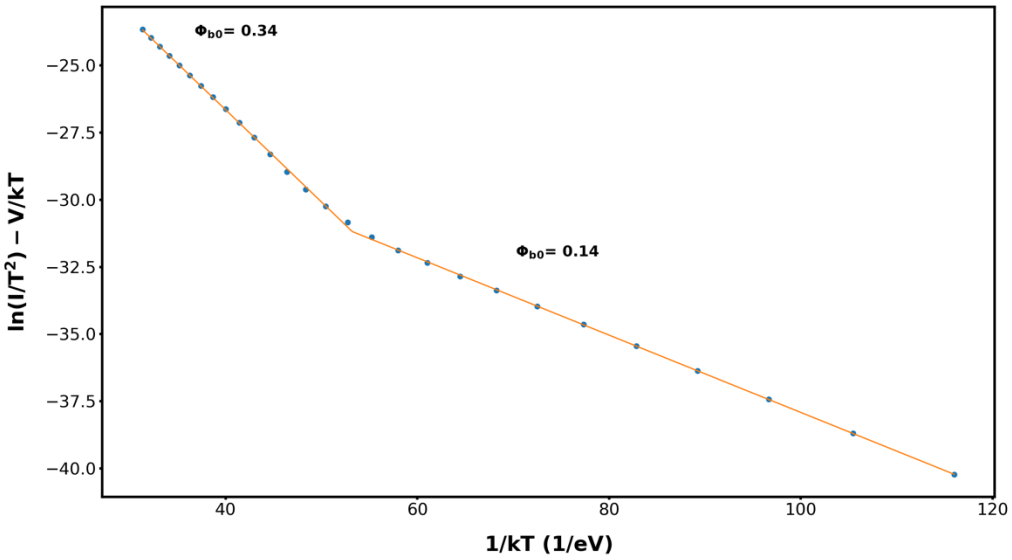

Figure 110. Device 178 post-stress Richardson plot

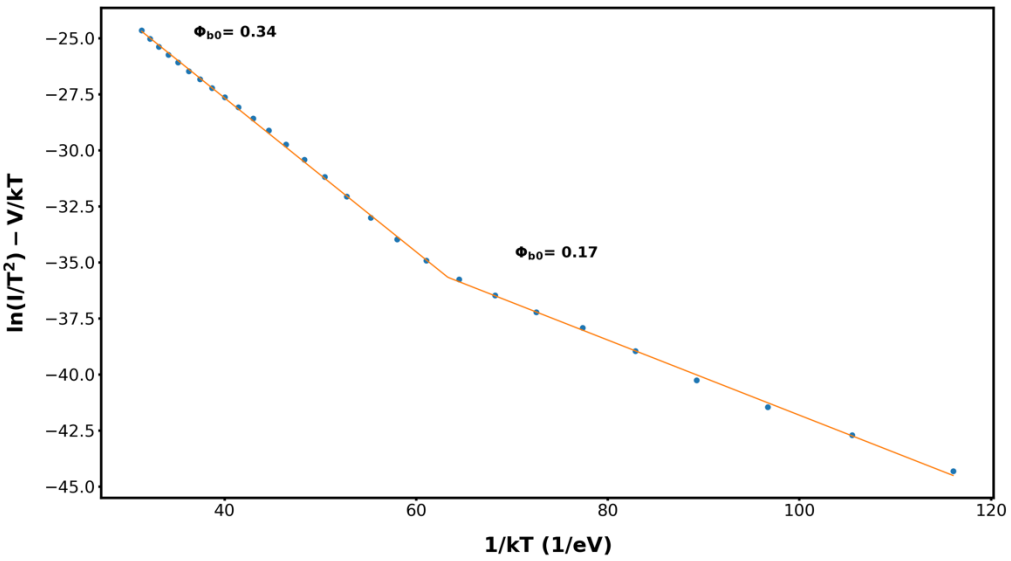

Figure 111. Device 326 post-stress Richardson plot

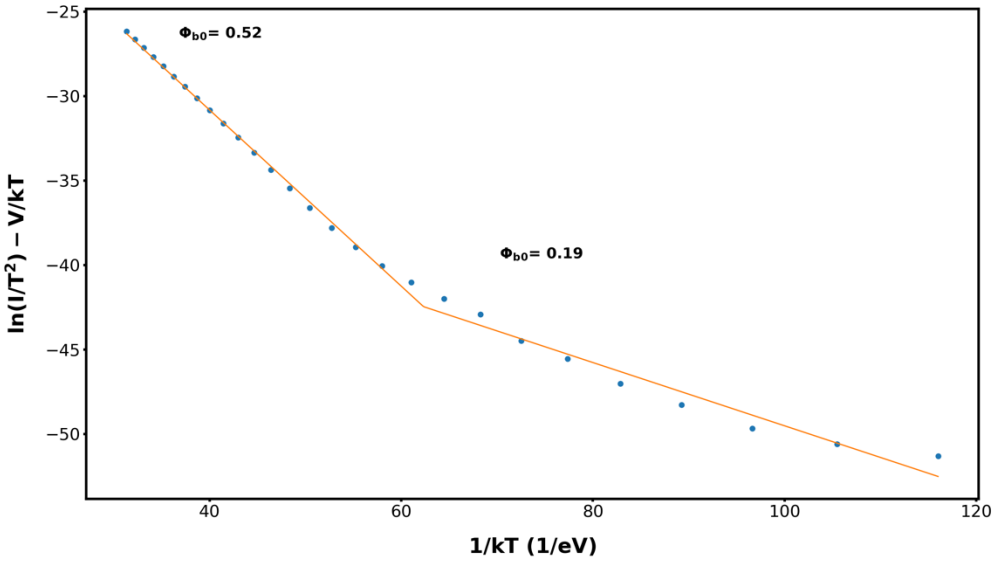

Figure 112. Device 328 post-stress Richardson plot

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APPENDIX I. POST-STRESS FORWARD RESISTANCE MEASUREMENTS

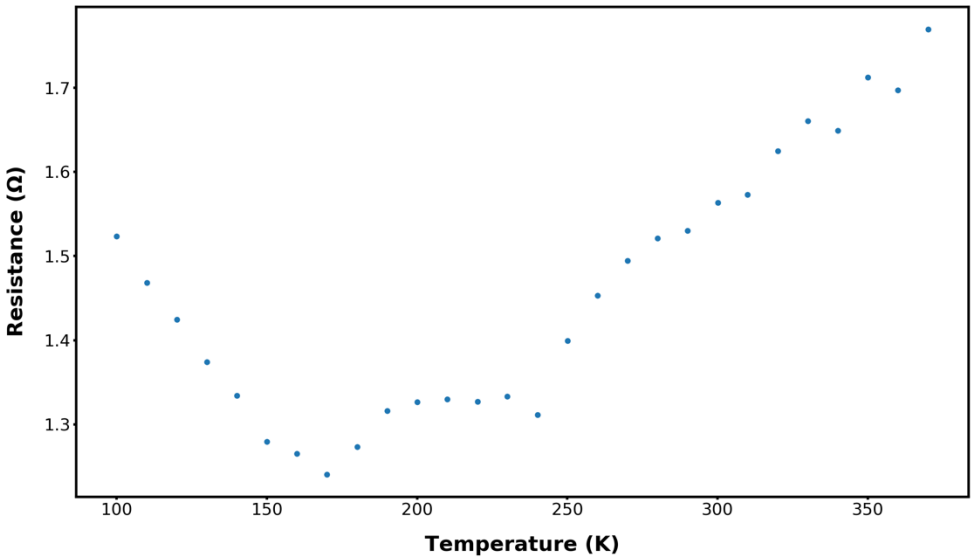

Figure 113. Device 144 post-stress R_{on} versus temperature plot

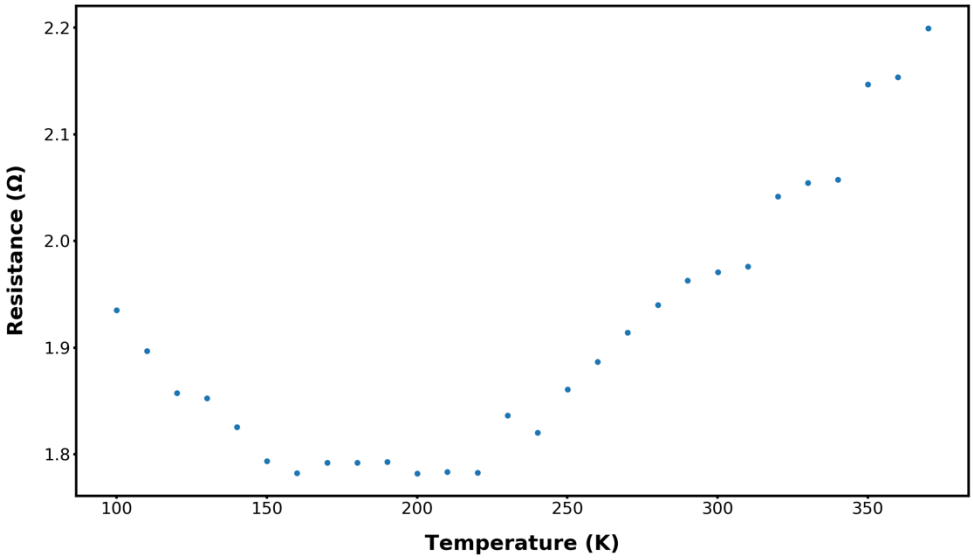

Figure 114. Device 149 post-stress R_{on} versus temperature plot

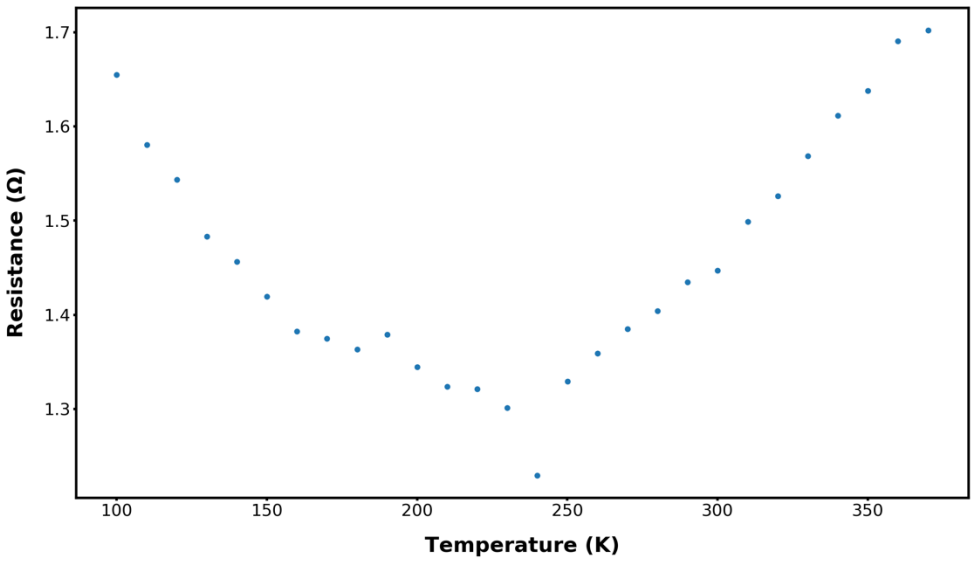

Figure 115. Device 178 post-stress for R_{on} versus temperature plot

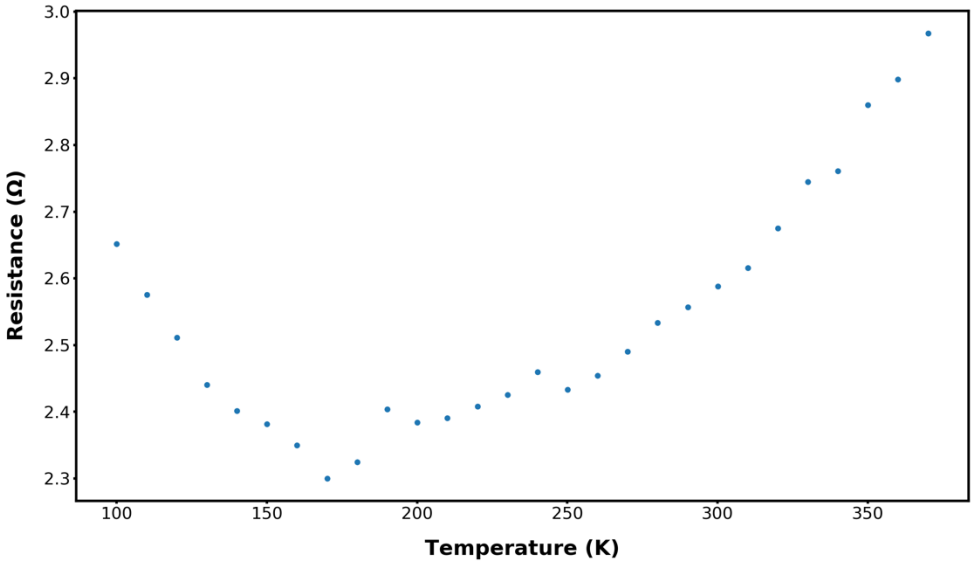

Figure 116. Device 326 post-stress R_{on} versus temperature plot

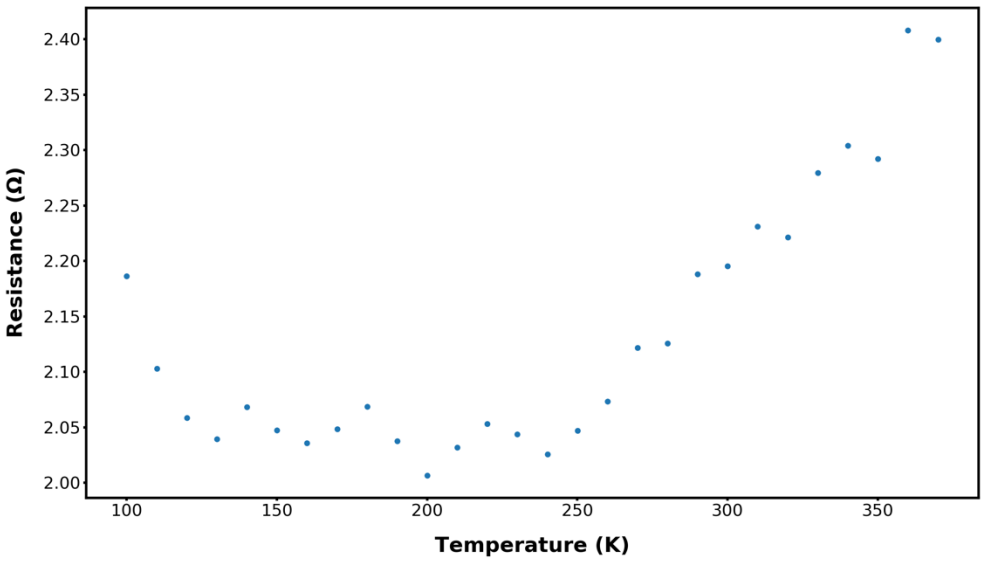

Figure 117. Device 328 post-stress R_{on} versus temperature plot

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