**Project Report**
**LSP-264**

# Photon-Counting Digital Focal Plane Array: FY19 Optical Systems Technology Line-Supported Program

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29 April 2020

**Lincoln Laboratory**
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
*LEXINGTON, MASSACHUSETTS*

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Massachusetts Institute of Technology
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*Group 87*

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## ABSTRACT

Visible imagers based on charge-coupled devices (CCDs) can be produced with large format and high pixel yield but typically operate at frame rates of a few Hz. For higher frame rate operation in photon-starved operation, arrays of Geiger-mode avalanche photodiodes (GmAPDs) operating in photon-counting mode are more attractive. To date, GmAPD arrays have been limited to modest formats (e.g., 256×256). Scaling to larger formats involves solving challenges in the GmAPD focal plane array (FPA), the readout integrated circuit (ROIC), the hybridization, and the packaging. One of the key challenges is developing a ROIC architecture that interfaces with GmAPDs and provides required power distribution to the APDs as well as internal to the ROIC and is capable of high data rates (10s of Gb/s).

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# 1. INTRODUCTION

## 1.1 PROBLEM STATEMENT

Visible imagers based on charge-coupled devices (CCDs) can be produced with large format and high pixel yields, but typically operate at frame rates of a few Hertz. For higher-frame-rate operation in photon-starved scenarios, arrays of Geiger-mode avalanche photodiodes (GmAPDs) operating in photon-counting mode are more attractive. To date, GmAPD arrays have been limited to modest formats (e.g., 256×256). Scaling to larger formats involves solving challenges in the GmAPD focal plane array (FPA), the readout integrated circuit (ROIC), the hybridization, and the packaging. One of the key challenges is developing a ROIC architecture that interfaces with GmAPDs and provides required power distribution to the APDs and ROIC while maintaining high data rate capability (10s of Gbps). Additionally, ROICs are limited in physical area because they are tiled out across a wafer during the fabrication process. The size of this tile, or reticle, is on the order of one square inch. Together with a relatively large (~25 μm) pixel pitch for both APD and ROIC pixel functionality reasons, the maximum imager size in a single die is approximately one megapixel. To achieve larger field of view for a camera, multiple focal planes can be tiled if the imager is designed to be abuttable on at least two sides.

## 1.2 PROGRAMMATIC CONCEPT

Scaling GmAPD FPAs to large-format, tiled arrays will allow for the development of wider field of view systems, thereby dramatically increasing the area coverage rate effectiveness for corresponding missions. Developing novel imagers requires research and development from semiconductor device design to materials science to electronics (ROIC) design as well as advanced packaging (e.g., hybridization, wire-bonding, etc.). For emerging imagers, such as those based on GmAPDs, each of those steps involves both technical risk and a long (often, multi-year) timeline. The relationship between figures of merit of a photon-counting imager, the impact of that metric on imager performance, the component primarily involves and the ultimate system impact is listed in TABLE 1. The first two characteristics (rows), photon detection efficiency (PDE) and noise rate (dark count rate or DCR), are primarily a function of the GmAPD FPA. The final four metrics are related primarily to the ROIC and are thus in the purview of this project. The existing MIT Lincoln Laboratory (MIT LL) photon-counting imagers, known as the Photon-Counting ROIC (PC ROIC) and the Digital Vision Sensor (DVS), are shown along with their performance characteristics.

In discussion with potential mission partners at MIT LL, the project developed a high-level list of desired functionality for an objective photon-counting imager based on GmAPDs. For funding, risk, and development time reasons, the progression from current state of the art to objective was broken into multiple steps as illustrated in TABLE 2. This project aims to develop the ROIC associated with the Pathfinder imager. The GmAPD characteristics are the subject of an Advanced Devices Line-funded effort led by Dr. Brian Aull. This project is addressing the remaining characteristics. A more detailed breakout of design parameters and performance characteristic goals is presented in TABLE 4. The key attributes that differ between the Pathfinder and Objective photon-counting imager are described in TABLE 5 along with the paths to achieve these improvements.

The bottom line of TABLE 2 is a technology choice rather than performance characteristics and describes the CMOS technology node in which the ROIC will be designed and fabricated. Although both 180-nm and 65-nm are old technologies by the standards of central processing unit (CPU) design, the cost and achievable complexity differences between the two are very different for imagers. A custom (full-wafer) fabrication in 180-nm CMOS costs approximately $200,000; whereas, a 65-nm CMOS fabrication is ~$1.6 million. Conversely, transistor density is approximately eight times higher in a typical pixel layout for 65-nm CMOS compared to 180-nm.

The key program goals are: demonstrating the first abuttable GmAPD ROIC, demonstrating a large-format photon-counting imager with very high (~100 kHz) ROI frame rate, and provide a simple design to allow demonstration of photon-counting imagers for a variety of applications.

### 1.3 TECHNICAL APPROACH

This project addresses key ROIC-related risks in the development of large-format photon-counting imagers. The digital pixel focal plane array (DFPA) ROIC technology developed at MIT LL has only been used for photodetectors operating in the linear mode (typically unity-gain photodiodes). The digital back end, including both the in-pixel resources and the data formatting and output channels, can be used for photon-counting imaging in the visible, near-infrared, and shortwave infrared with appropriate GmAPD FPAs. This application of a DFPA back end to photon-counting imaging has never been accomplished, however, so significant risks remain. In this project, a new ROIC with GmAPD front-end circuit with the DFPA back end is being designed and fabricated for hybridization with Si GmAPD FPAs. An auxiliary benefit of the ROIC development is that it can be used as a vehicle to test GmAPD FPAs fabricated at MIT LL.

To meet the design goals within the available time and budget, the ROIC design in 65-nm CMOS process at Global Foundries (GF) US is incorporating proven GmAPD analog front-end designs with digital focal plane array (DFPA) back end technology. Significant reuse from existing DFPA designs allowed for a much shorter design cycle. This decreased design time, coupled with cost sharing a 65-nm tape-out with several other MIT LL projects, allowed the time and budget goals to be met.

One high-level design decision is the number of sides of the FPA that can be made abuttable. TABLE 3 compares different abutment techniques. This project uses the middle (two-side abuttable) technique as a compromise between ROIC performance risk and ultimate benefit to the camera.

Another high-level design decision is the hybridization technique between GmAPD FPAs and the ROIC. Traditional bump bonding (typically thermo-compression bonding using a soft metal such as indium) is well proven, but it has device performance drawbacks. Specifically, the parasitic capacitance associated with the bump-bond pads as well as the bump bond itself leads to charge flow during a photo detection event (avalanche breakdown) sufficient to generate a few photons that can trigger false detections in neighboring pixels, a process known as optical crosstalk. The lower-stray-capacitance direct bond interconnect (DBI) process pioneered by Ziptronix is preferable from an imager performance standpoint, but requires more process development and time to accomplish. A third hybridization option is the use of copper micro-pillars through a company named Micross. This path allows for individual die hybridization, and has interconnect capacitance slightly higher than that of the DBI process and slightly lower than that of bump bonding. The goal of the design is to engineer the metal stack such that either micro-pillar or bump

bond can be used. Designing a metal stack to utilize DBI is untenable, as it requires the removal of several thick top metal power routing layers. Bump bonding allows more rapid, lower-risk verification of the ROIC, while micro-pillar enables higher performance in the ultimate configuration without the risk of losing full wafers to DBI processing errors.

### 1.4 SECTION 1 TABLES

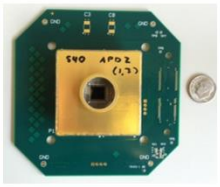
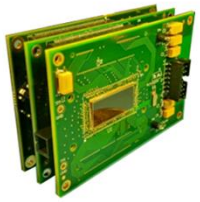
**TABLE 1**

**List of Key Photon-Counting Imager Figures of Merit along with the Imager Component Involved and the System Impact**

| Metric | Effect | Component | Impact |
|---|---|---|---|
| PDE | Increases SNR | APD | Area coverage rate and system cost (SWaP) |
| Noise rate | Decreases SNR | APD and hybridization | |
| Format | Increase imaged area | APD and ROIC | System cost (platform count) |
| Abuttability | Ability to tile | ROIC | |
| Frame rate | Sets time resolution | | Better performance (system specific) |
| Dynamic range | Measure range of signals | | |

**TABLE 2**

**Table Comparing Present and Planned Photon-Counting Imager Specifications and Design Targets**

| Metric | Photon-Counting ROIC | Digital Vision Sensor | Pathfinder | | Threshold | | Objective | |
|---|---|---|---|---|---|---|---|---|
| |  |  | | | | | | |
| PDE (%) | ≤ 5 | ≤ 5 | 30 | | 30 | | 50 | |
| Noise rate (Hz) | ~100 | ~100 | ~100 | | < 100 | | < 100 | |
| Format | 256x256 | 256x256 | 512x512 | | 0.5 Mpixel | | 1 Mpixel | |
| Abuttability | No | No | 2-side | | 2-side | | 4-side | |
| Frame rate (kHz) | 12** | 1 | 20 | 200* | 2 | 500* | 10 | 900* |
| Dyn. range (bits) | 1 | 10 | 2 | 1 | 8 | 1 | 8 | 1 |
| Pixel pitch (μm) | 25 | 30 | 25 | | 20 | | 20 | |
| CMOS tech | 180-nm | 180-nm | 180-nm | | 65-nm | | 65-nm | |

* Frame rate in ROI mode

** ROI only available at edge of imager and thus not listed

**TABLE 3**

**Comparison of Tiling Approaches for Extended-Format Imagers including Benefits and Challenges of Each Approach (Stop Light Color Coding)**

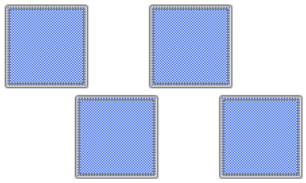
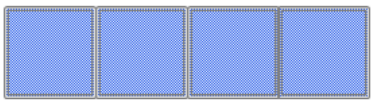
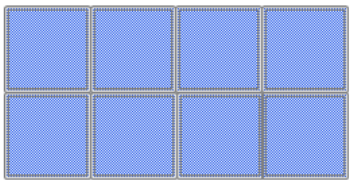
| "Pumpkin Teeth" | Linear Array | 2D Tile |
|---|---|---|
| 0-side abuttable  | 2-side abuttable  | 3- to 4-side abuttable  |
| Characteristics:<br>• Simpler ROIC<br>  • More perimeter for power and data pads<br>• Larger, more complex camera<br>  • Packaging<br>  • Alignment<br>  • Optics | Characteristics:<br>• Simpler camera mechanical design<br>  - Top and bottom areas for packaging, flexprints<br>  - Single interposer and package design<br>• ROIC power distribution and data output challenges | Characteristics:<br>• Most flexible FPA layout options<br>• New, challenging ROIC interface design and implementation<br>• New packaging and interconnection for digital ROICs<br><br>Future work can leverage 3D integration advances and advanced packaging development |

**TABLE 4**

**Key PC-DFPA ROIC Design Parameters Color Coded by Importance**

| Parameter | Numbers | Comments |
|---|---|---|
| Full frame format | ~0.3 Mpixel | e.g. 640 × 480 or 1024x256 |
| Full-frame frame rate | 10 kHz | |
| Bit depth | 3 | Estimate to be refined based on pixel layout |
| Region-of-Interest Size | ≤ 1024 | Baseline: Programmable |
| Number of Regions-of-Interest | 5 | |
| Region-of-Interest frame rate | ≥ 200 kHz | Baseline: Non-simultaneous with full frame |
| Pixel Pitch | 20 µm | Smallest APD pixel yet |
| Abuttability | 2-side | Limits control lines, power, etc. |

* green = firm; yellow = soft requirement

**TABLE 5**

**Key Metrics for Photon-Counting Imager Development at MIT LL and the Contribution of the PC-DFPA Program as well as the Future Path to the Objective Design**

| Metric | Addressed | Path to Objective |
|---|---|---|
| PDE | AD Line | AD Line or Ext. |
| Noise rate | AD Line | AD Line or Ext. |
| Format | ~4x increase (stand-alone useful) | Move to 65-nm CMOS (larger reticle) |
| Abuttability | Enable linear array of FPAs | Leverage ongoing 3D integration and packaging development (e.g., G81 proposal & ReImagine) |
| Frame rate | Make ROI mode accessible across entire FPA | Higher speed outputs |
| Dynamic range | Modest increase | Move to 65-nm CMOS |
| Pixel pitch | Reduce ~30% | |

# 2. ROIC DESIGN

## 2.1 ABUTTABLE LARGE-FORMAT ROIC

The MIT LL GmAPD detector arrays have been manufactured with a 25-µm pitch. The ROIC matches this pitch and will provide a 512×256 array of pixels. All previous ROIC design efforts have incorporated IO pads on all sides of the chip. To enable the abutment of ROICs on two sides, this ROIC will have IO pads on the north and south sides, leaving the east and west sides open to create large-format arrays in those directions. The pixel array will be situated as close to the chip edge as allowed by design rules to maintain a 25-µm pitch from chip to chip. **Error! Reference source not found.** illustrates the concept in block diagram format, along with a table comparing the desired ROIC characteristics with those anticipated for this design.

One challenge associated with two-side abuttability will be power distribution associated with the arming and disarming of the GmAPDs in such a large array. This is addressed in two ways: controlling the charge/discharge rate, and spreading out the pixel array arming in time. The charge/discharge rate is a function of the GmAPD capacitance and the sizing of the transistors in the charge/discharge path. Minimizing GmAPD and interconnect capacitance will be mitigated by careful layout. The transistors in the charge/discharge path will be sized to control the charge/discharge rate. To spread out the arming of GmAPDs across the pixel array, the ROIC will receive an ‘arm’ signal and distribute it to pixel columns. The first column of the array will arm, then after a delay, the next column will arm, and so forth. The delay from column to column will be long enough to allow each column to charge before moving onto the next column.

## 2.2 HIGH FRAME RATE REGION OF INTEREST

The desired full frame rate and ROI frame rate are 10 kHz and 200 kHz, respectively. To achieve these rates, the existing DFPA readout scheme is leveraged as illustrated in Figure 2. The DFPA scheme distributes a number of data output taps across the ROIC. Each output tap services a number of columns of pixel data based on the number of columns divided by the number of output taps. The output taps run at 1 Gb/s. The DFPA scheme allows the user to select using all taps, some taps, or just one tap. This design uses 16 output taps, allowing the user to select between using 1, 2, 4, 8, or16 output taps. Maximum frame rate (full frame or ROI) is achieved by selecting all 16 taps. With this scheme, a full frame (excluding photon-counting integration time) can be read out at a rate of 48 kHz, and a 32×32 ROI can be read out in excess of 206 kHz as seen in Figure 3.

To achieve the high data rates planned for this design, a high-speed serializer structure that has been tested and refined over several years of DFPA design cycles is reused here. Output data rates are guaranteed to operate at 1 Gb/s, and can potentially be run as fast as 2 Gb/s, which can potentially increase full frame and ROI frame rates.

## 2.3 USE OF SIMPLE LEVERAGED DESIGN

In an effort to reduce risk and focus on the challenges of a large-format/abuttable ROIC as well as maintaining high frame rate, this design leverages an existing GmAPD front-end circuit and an existing

DFPA (Digital Focal Plane Array) back end as illustrated in **Error! Reference source not found.**. The front-end circuit is leveraged from the 256×256 65-nm HECTIC (highly efficient counting and timing integrated circuit). The front end will be reduced to only provide a 'count' function, pixel disable, and asynchronous pixel hold-off and arm. The DFPA back end will leverage proven high-speed serial readout circuitry and current mode differential outputs to achieve high frame rates without the need for complex multiplexing of data output paths. The DFPA data output stream format is also leveraged. This format has minimal overhead and reduces the burden on data reception in the FPGA.

### 2.4 MODIFIED HECTIC FRONT END

The front-end circuit in this ROIC has the same topology as the HECTIC front-end circuit with key modifications to reduce power consumption during pixel arm and discharge. In Figure 1, seven transistors are identified by red circles. Each of these transistors has had their respective W/L sizing modified to decrease current. When compared to the original HECTIC front end, these changes reduce peak and nominal power draw during arm and discharge by close to 30%.

### 2.5 APD COLUMN ARM CONTROL

The arming of APDs can occur in two ways: simultaneous or staggered. A simultaneous arm will incur very large current draw if all pixels are in a state where they can be armed, such as on initial arm. In very low-light scenarios, when most pixels are armed and only a few need arming, then using simultaneous arm can greater increase the frame rate. However, in situations where most pixels need to be armed, staggered arm is preferred. In this mode, a pulse is injected in the southwestern most part of the ROIC and as the pulse is clocked from column to column, each column is armed. Therefore, only 256 pixels are armed at any given time, greatly reducing power draw. Figure 6 shows a single column instantiation of the arm circuit. Either the arm pulse is passed straight through a mux without delay, or it is delayed by virtue of clocking the pulse through a register. Figure 7 provides a visual depiction of staggered arm.

## 2.6 SECTION 2 FIGURES

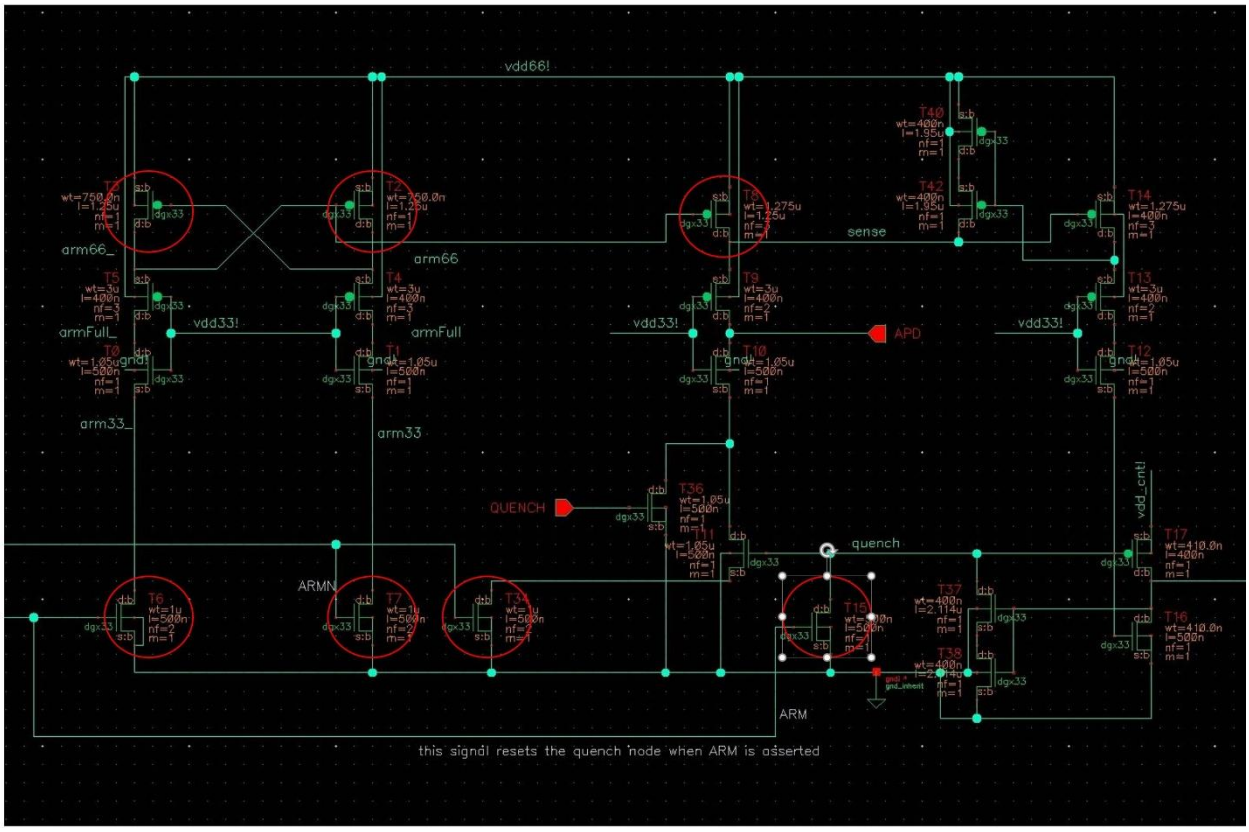



*Figure 1. PC-DFPA ROIC front-end circuit.*

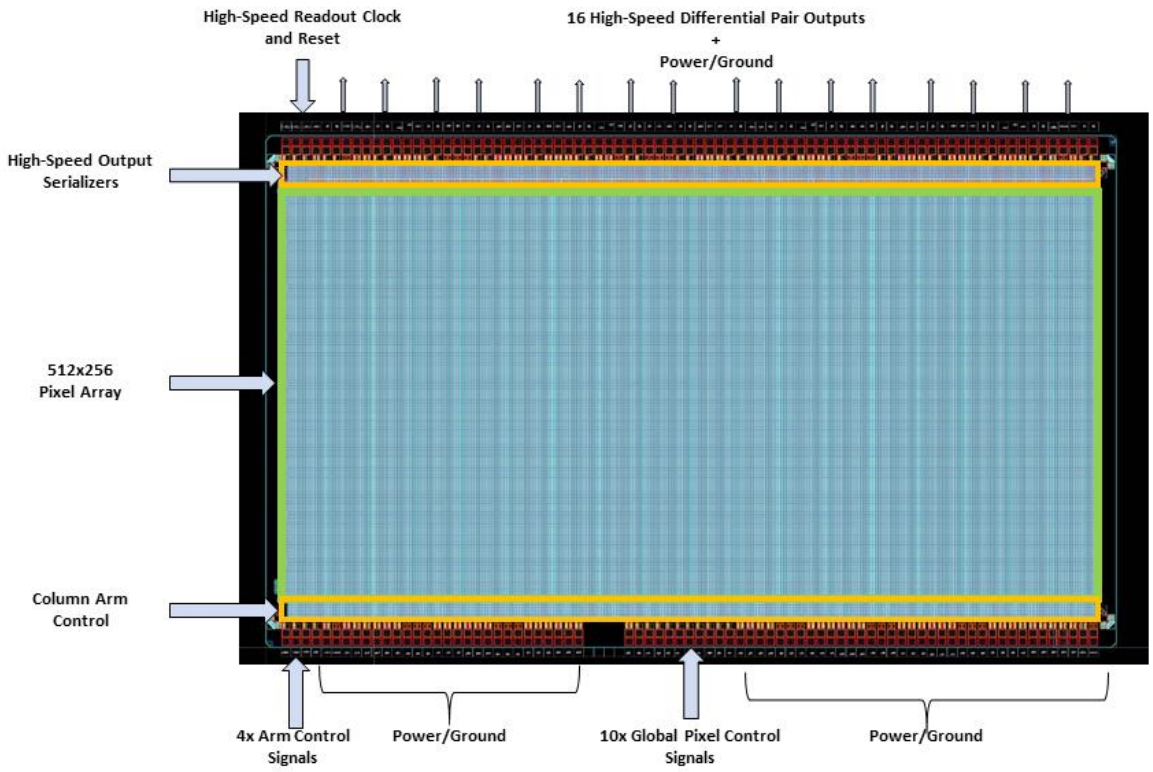



*Figure 2. PC-DFPA ROIC top-level layout.*

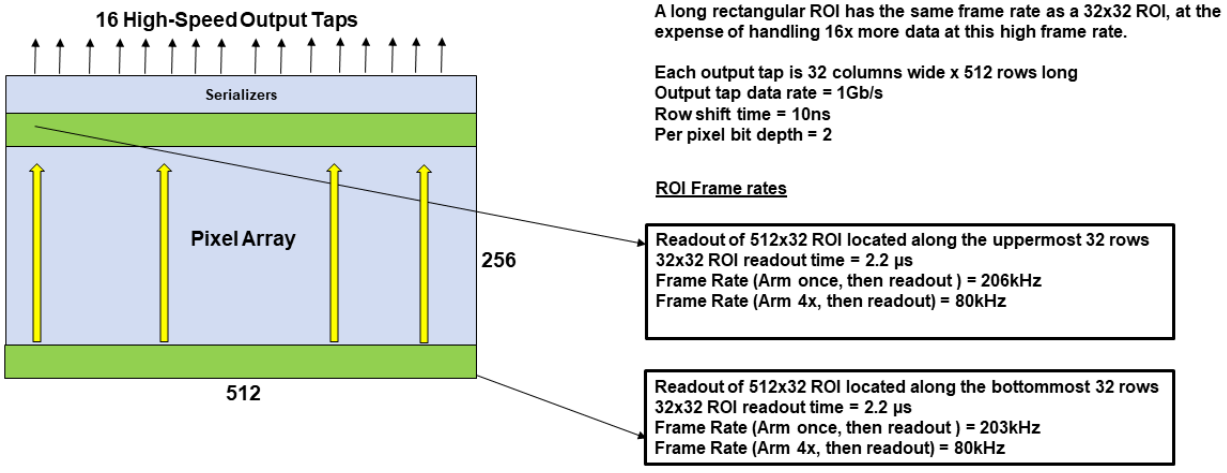



*Figure 3. ROI frame rates.*

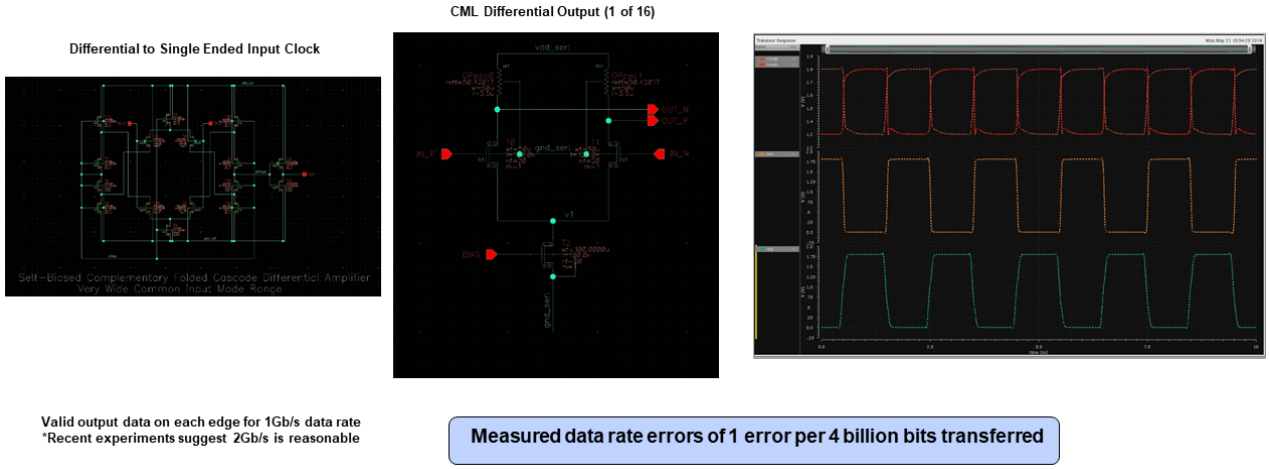



*Figure 4. High-speed CML clock.*

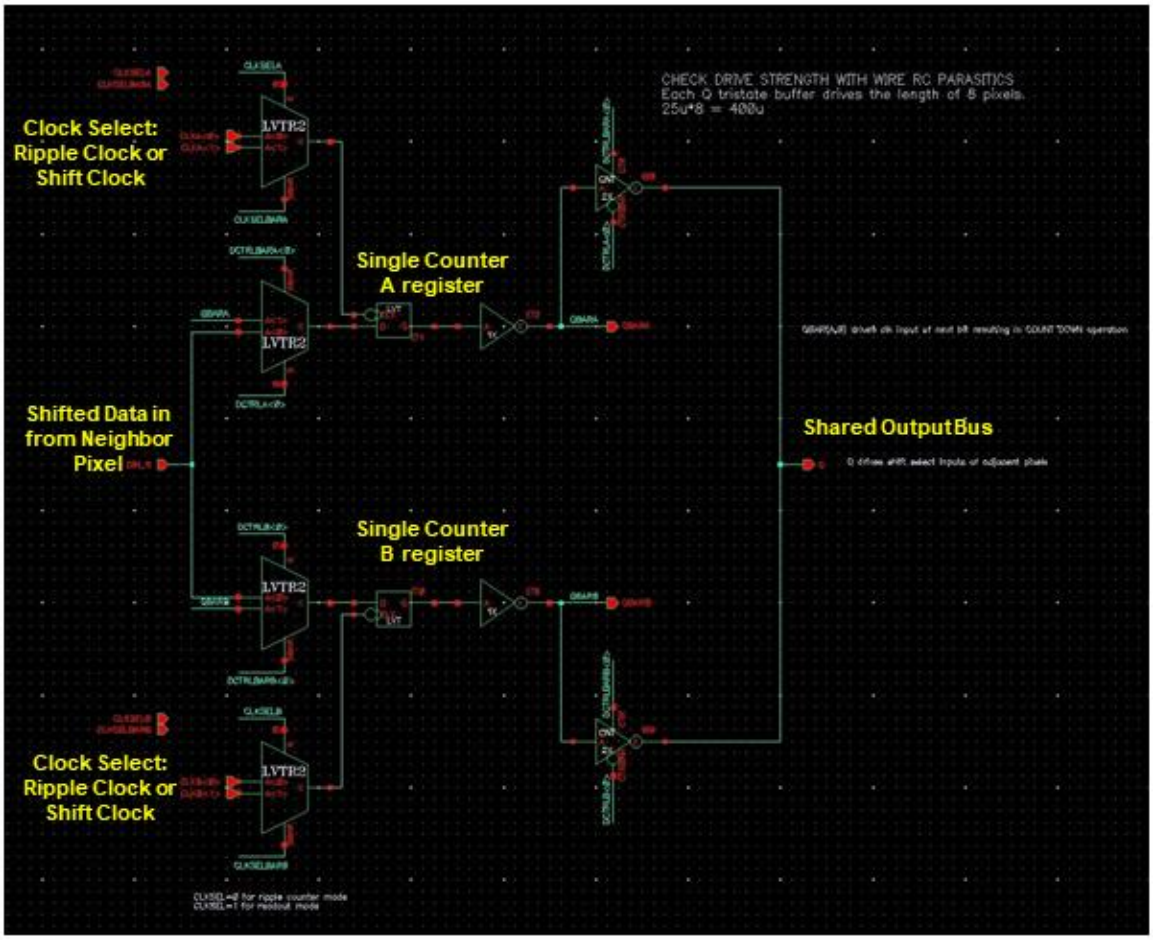



*Figure 5. Baseline pixel architecture.*

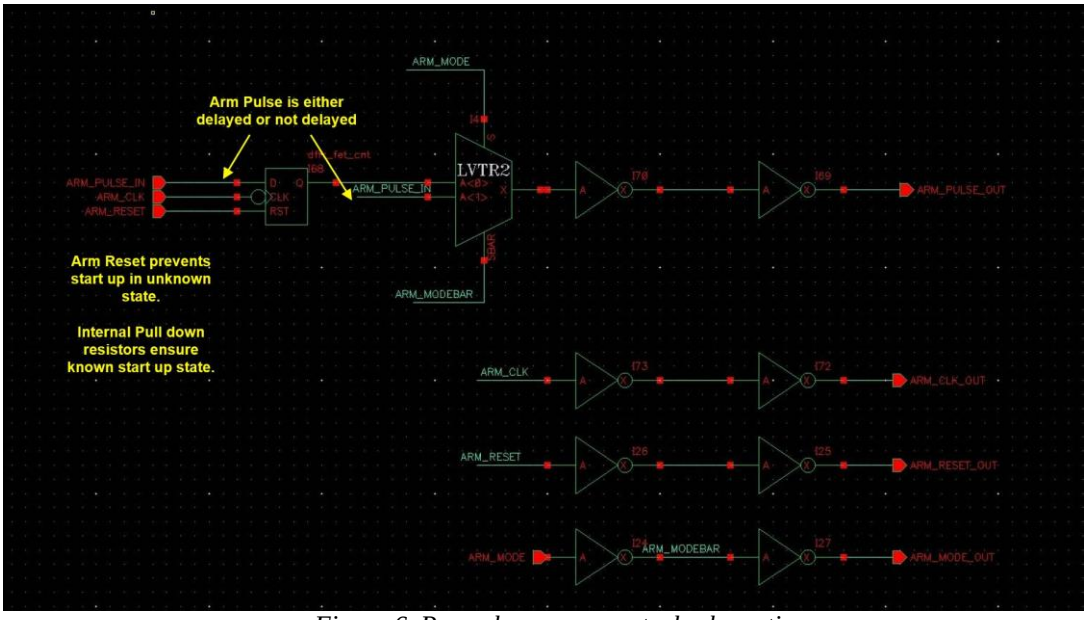



*Figure 6. Per-column arm control schematic.*

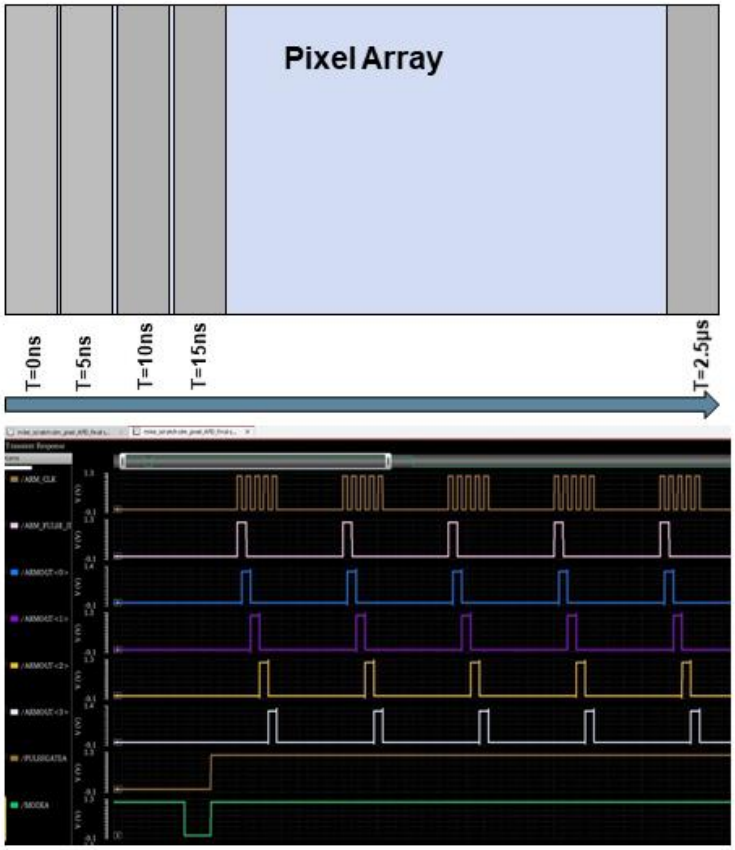



*Figure 7. Diagram depicting an arm pulse as it arrives in each column.*

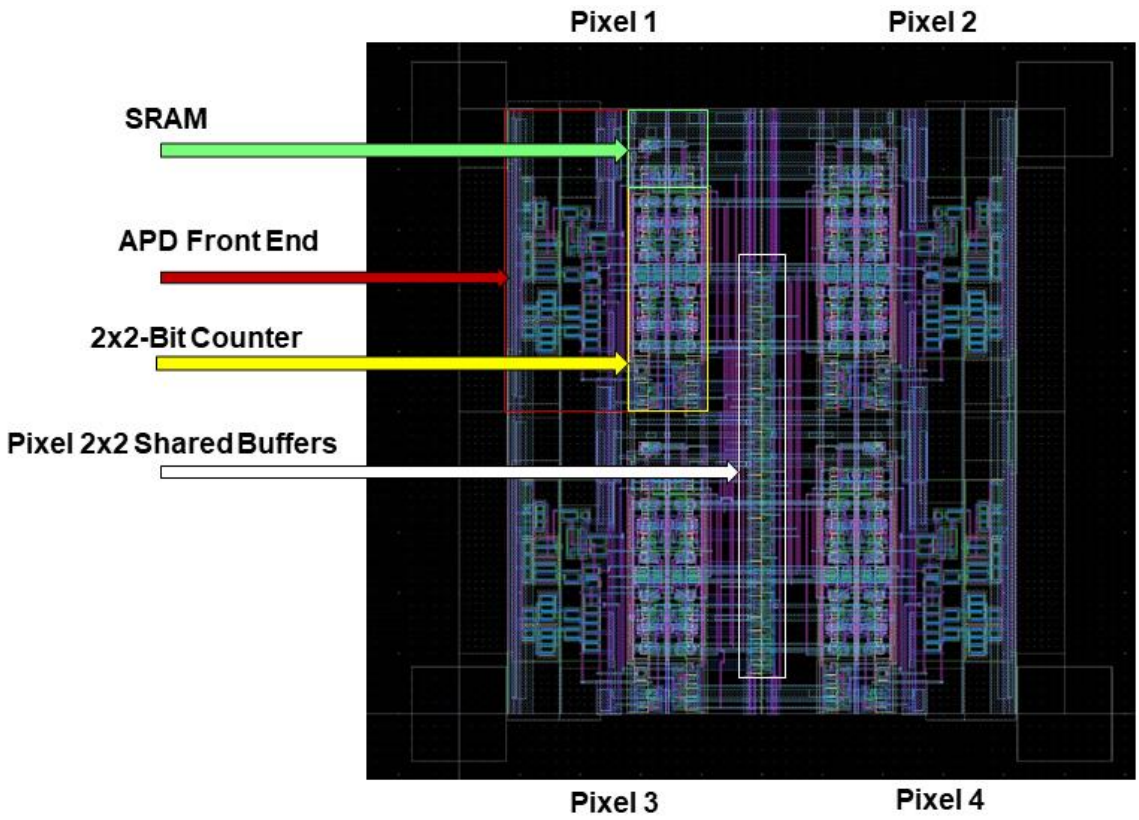



*Figure 8. Actual layout for 2×2 group of pixels.*

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## 3. CONCLUSION

The design and layout of the PC-DFPA finalized in May 2019, and will tape out at the end of September 2019. The design passes all LVS and DRC checks required for tape out. The ROIC meets or exceeds most desired specifications, with the exclusion of array size and wafer-scale 3D integration of detector arrays. The array size was limited to the available space on a shared Global Foundry reticle. The final specifications are shown below in Table 6.

**TABLE 6**

**PC-DFPA Final Specifications**

| Parameter | Final Specifications |
|---|---|
| Full-frame format | 512x256 |
| Full-frame frame rate | 48 kHz @1 Gb/s, 87 kHz @2 Gb/s |
| Bit depth | 2 or 4 |
| ROI size | No smaller than 32x8 (256) |
| Number of ROI | Varies |
| ROI frame rate | ≥203kHz |
| Pixel pitch | 25 µm (compatibility with AD-funded GmAPDs) |
| Abuttability | Two-side |
| CMOS tech | Global Foundries 65 nm low power |
| Hybridization capability | Individual die bump bond or copper micro-pillar |
| Number of high-speed outputs | Selectable up to 16 CML differential outputs |
| High-speed output data rate | Minimum guaranteed 1 Gb/s |
| APD arm control | Simultaneous or staggered by column |
| APD over-bias | 6.5V |
| Quench control | Per-pixel active quench and/or global quench |
| Pixel SRAM | Pixel disable/four-bit counter mode |
| Pixel functionality | Two-bit 'count while read' or four-bit 'count then read' |
| Number of wire bond pads | 81 North, 77 South |
| Number of input control lines | 14 |
| Power supplies | 6.6V, 3.3V, 1.8V, 1.2V, Ground, APD ANODE |

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