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3D Heterogeneous Integration Of Microwave/Millimeter-Wave Sensor And Communications Microsystems Using High-Aspect Ratio Micromachined "Building Block" Technology

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14. ABSTRACT
This project focused on the development of 3D heterogeneous integration strategies for RF/microwave/millimeter-wave Microsystems. Three thrust areas were explored. The first thrust area was the development of a 3D heterogeneous integration process based on the mechanical fit of high-aspect-ratio micromachined structures. In this effort, prefabricated power amplifier RFICs or MMICs were mated to a coplanar-waveguide carrier substrate through micromachined vertical interconnects realized in a high-aspect-ratio SU-8 process. This work transitioned into the second thrust area, which involved the development of liquid metal vertical interconnects. This novel

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Major Goals: Develop and demonstrate a novel 3D heterogeneous integration technology based on the mechanical assembly of microsystem building block ICs using high-aspect ratio micromachined interconnects.

Accomplishments: The overall goal of this ARO-funded project was the development of 3D heterogeneous integration strategies for microwave/millimeter-wave communications and sensing microsystems. Initial efforts were focused on a 3D “mechanical fit” technology in collaboration with Prof. Scott Barker’s group at the University of Virginia. In this technology, 3D high-aspect ratio pillar and socket structures are fabricated on MMIC and carrier substrates, and flip-chip
mated together to provide an interlocking “Lego-like” mechanical contact that would be relatively robust to thermal and mechanical stresses. Excellent microwave/mm-wave performance was demonstrated on passive structures, but efforts to integrate with active MMIC amplifiers were less successful.
Consequently, the novel concept of vertical liquid metal vertical interconnects for heterogeneous flip-chip integration of active integrated circuit chips with passive structures was developed under this program. The liquid metal interconnect approach offers the potential for high reliability RF/microwave interconnects, since the structures will absorb thermal and mechanical
stresses (e.g. CTE mismatch, vibration, etc.) unlike conventional rigid interconnect structures.
Initial proof-of-concept demonstrations of flip-chip integration of passive coplanar waveguide (CPW) test structures, and integration of active GaAs MMIC power amplifiers on CPW carrier substrates were successfully conducted. Building on the previous proof-of-concept active MMIC power amplifier chip integration using liquid metal vertical interconnects, the liquid metal interconnect technology was extended to the 3D Polystrata technology in collaboration with Nuvotronics LLC, Radford, VA. Microwave performance of passive test structures and a prototype integrated MMIC assembly were
performed, and testing for high power and temperature cycling performance was conducted.
In the future it is anticipated that this technology can be extended to the heterogeneous integration of 3D antenna arrays in Polystrata technology with silicon- and non-silicon-based radar transceiver and processing ICs. Efforts in millimeter-wave antenna, power combining/splitting, and monopulse processing IC design were conducted in parallel with Nuvotronics under separate funding.

Training Opportunities: Nothing to Report

Results Dissemination: Nothing to Report

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Honors and Awards: Sanjay Raman was elected Fellow of IEEE for his leadership in adaptive microwave and millimeter-wave integrated circuits.

Protocol Activity Status:

Technology Transfer: Nothing to Report

PARTICIPANTS:

Participant Type: Graduate Student (research assistant)
Participant: Parrish Ralston
Person Months Worked: **Funding Support:**
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Authors:
Keywords: Coplanar waveguide (CPW), mechanical fit, SU-8, vertical transition, W-band
Abstract: This paper presents the design, simulation, and measurement of a vertical RF interconnect with mechanical fit for 3-D heterogeneous integration. The mechanical fit is a flip-chip strategy employing interlocking SU-8, an ultra-thick photoresist, structures to prevent misalignment during assembly and increase the reliability of the interconnects. To determine the electromagnetic characteristics, such as insertion loss and the coupling between face-to-face chips, different test structures were fabricated and measured. Experimental results show excellent RF performance up to 110 GHz with low insertion loss (better than 0.1 dB per transition at 40 GHz).

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Authors:
Keywords: Flip chip, gallium alloys, monolithic microwave integrated circuits (MMICs), interconnects, PolyStrata, recta-coax, power amplifier
Abstract: Prior work has demonstrated a new process utilizing room-temperature liquid metal, Galinstan, as an interconnect material for flip-chip bonding. This interconnect forms a flexible bond between chips and carriers, and, therefore, a flip-chip assembly using this technology is much less susceptible to thermomechanical stresses. This paper applies this concept to interconnect GaAs MMIC chips to 3-D Polystrata transmission-line structures. Passive assemblies are utilized to model, test, and verify liquid–metal interconnections, giving average losses per liquid–metal transition of about 0.11 dB out to 26.5 GHz, low parasitics per transition, and demonstrated reliability after temperature cycling. A prefabricated GaAs MMIC chip is postprocessed for liquid–metal assembly. Measured results show, over theMMIC's 4.9–8.5-GHz frequency range, the system's overall reduction in gain of the MMIC is 1.4 dB or 0.7 dB per RF transition as compared with direct probing of the MMIC chip.
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3D Heterogeneous Integration of Microwave/Millimeter-Wave Sensor and Communications Microsystems Using High-Aspect Ratio Micromachined "Building Block" Technology

Final Report: Scientific Progress

Principal Investigator: Sanjay Raman
The Bradley Dept. of Electrical and Computer Engineering, Virginia Tech

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Problem Statement and Executive Summary

The overall goal of this ARO-funded project was the development of 3D heterogeneous integration strategies for microwave/millimeter-wave communications and sensing microsystems. Initial efforts were focused on a 3D "mechanical fit" technology in collaboration with Prof. Scott Barker's group at the University of Virginia. In this technology, 3D high-aspect ratio pillar and socket structures are fabricated on MMIC and carrier substrates, and flip-chip mated together to provide an interlocking "Lego-like" mechanical contact that would be relatively robust to thermal and mechanical stresses. Excellent microwave/mm-wave performance was demonstrated on passive structures, but efforts to integrate with active MMIC amplifiers were less successful.

Consequently, the novel concept of vertical *liquid metal* vertical interconnects for heterogeneous flip-chip integration of active integrated circuit chips with passive structures was developed under this program. The liquid metal interconnect approach offers the potential for high-reliability RF/microwave interconnects, since the structures will absorb thermal and mechanical stresses (e.g. CTE mismatch, vibration, etc.) unlike conventional rigid interconnect structures. Initial proof-of-concept demonstrations of flip-chip integration of passive coplanar waveguide (CPW) test structures, and integration of active GaAs MMIC power amplifiers on CPW carrier substrates were successfully conducted.

Building on the previous proof-of-concept active MMIC power amplifier chip integration using liquid metal vertical interconnects, the liquid metal interconnect technology was extended to the 3D Polystrata technology in collaboration with Nuvotronics LLC, Radford, VA. Microwave performance of passive test structures and a prototype integrated MMIC assembly were performed, and testing for high power and temperature cycling performance was conducted.

In the future it is anticipated that this technology can be extended to the heterogeneous integration of 3D antenna arrays in Polystrata technology with silicon- and non-silicon-based radar transceiver and processing ICs. Efforts in millimeter-wave antenna, power combining/splitting, and monopulse processing IC design were conducted in parallel with Nuvotronics under separate funding.

3D Integration of a 30 GHz SiGe HBT PA with Mechanical Fit

An existing 30 GHz SiGe HBT PA RFIC [1] designed at VT and fabricated in the Atmel SiGe2RF process was leveraged for a proof-of-concept demonstration of the proposed 3D integration strategy. The UVa team co-designed and fabricated coplanar waveguide (CPW)-based planar feeding structures on high-rho Si substrates, and interfaces to SU-8 defined high-aspect ratio vertical pins. In parallel, VT M.S. E.E. student Joe Wood (U.S. Citizen) developed a post-IC SU-8 process to fabricate mechanical fit structures on the prefabricated PA chip that interface with the UVa CPW carrier substrate. This included a planarization process which emplaced the PA chip into a micromachined cavity etched anisotropically into a sacrificial silicon substrate, allowing for SU-8 resist to be spun over the small die without planarity or edgebead issues. Figure 1 shows the layouts of the PA chip and the CPW carrier substrate. After the separate fabrication flows were completed, the PA chip was flip-chipped onto the CPW carrier substrate using a pick-and-place tool. It was found that a thermocompression bonding step was required to effectively mate the PA chip to the vertical interconnect structure on the carrier

substrate. This was unfortunate, since it somewhat mitigated an anticipated advantage of the mechanical fit assembly process. Figure 2 shows the PA chip with fabricated SU-8 mechanical fit structures and the final assembled structure.

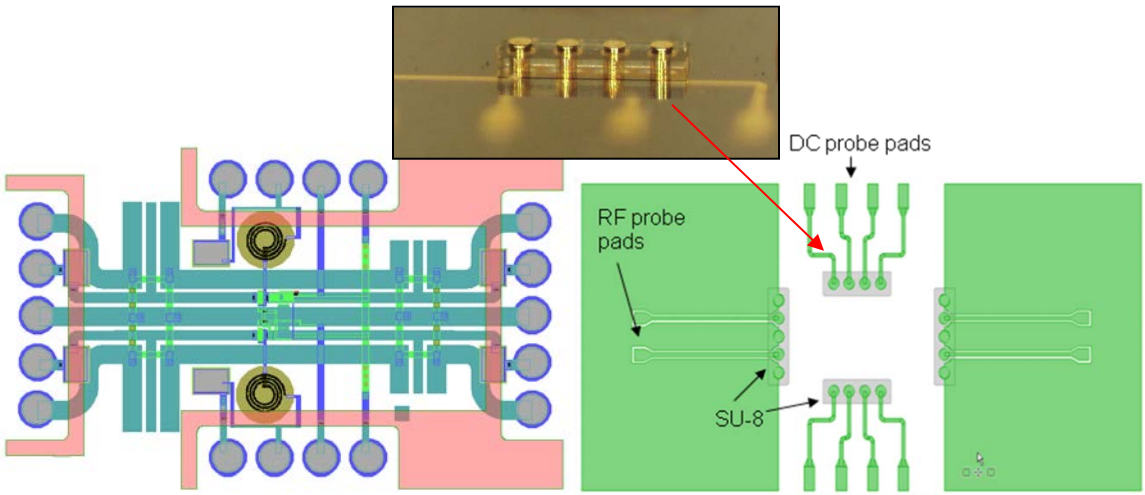

Figure 1: (left) Layout of 30 GHz SiGe HBT PA with SU-8 mechanical fit socket in red. (right) Layout of bottom carrier substrate with SU-8 vertical interconnect structure. (inset) Fabricated SU-8 vertical interconnect structure.

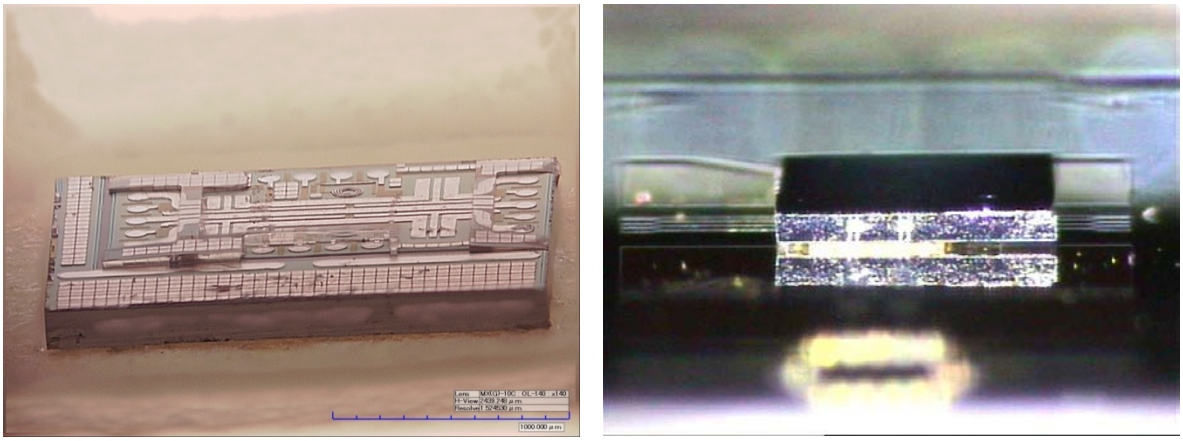

Figure 2: (left) 30 GHz PA chip with fabricated mechanical fit structures. (right) Assembled PA chip on top of CPW carrier substrate.

The S-parameters of the assembled PA structure were subsequently measured using on-wafer probes (Figure 3). This particular PA chip was an alternative design that had been fabricated that did not perform as well as the published design; due to the availability of sufficient samples for post-IC processing experiments, we continued to work with this design. However, for the purposes of characterizing the effects of the 3D integration process, the absolute performance of the PA chip was of secondary importance. Unfortunately, the performance of the assembled PA showed significantly higher insertion loss. This is believed to be due to inadequate contact between the vertical interconnect posts and the Aluminum pads on the PA chip. The presence of

poor contact is borne out by fitting lumped element models to the measured data which show large series resistance and capacitances arising in the signal and ground paths.

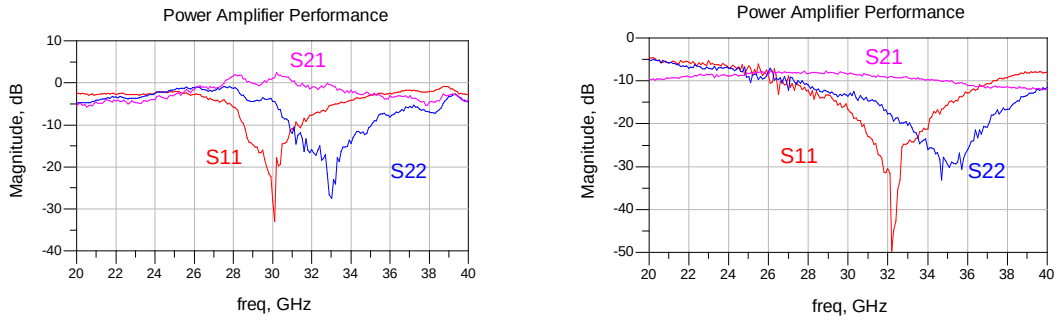

Figure 3: Measured 30GHz PA performance before and after assembly.

The contact difficulties experienced with the mechanical fit approach motivated our investigation of the liquid metal interconnect idea to be discussed further below.

In addition to the above work, we also collaborated extensively with Dr. Barker's group at UVa on a comprehensive microwave/mm-wave characterization of the passive 3D "mechanical fit" vertical RF interconnects and jointly published a paper on this work in *IEEE Transactions on MTT* in March 2012 [3].

Liquid Metal Vertical Interconnects

Initial work under this thrust was performed by Virginia Tech M.S. student Joseph Wood. Joseph completed his M.S. thesis work in March 2009 and subsequently joined BAE Systems, Nashua, NH. This work continued under Virginia Tech Ph.D. students Parrish Ralston (female, U.S. citizen) and Krishna Vummidi[1]. Parrish Ralston graduated with her Ph.D. in Electrical Engineering in May 2013 and joined Northrup Grumman Electronic Systems in Linthicum, MD. Krishna Vummidi completed his Ph.D. work in February 2011 and is now with Integrated Device Technology (IDT), San Jose, CA.

In the early stages of this work, the high aspect-ratio SU-8 interconnect structures developed under the mechanical fit thrust of this project were partially filled with a (room temperature) liquid metal, which in turn mated with vertical metal pin interconnects on the matching die or substrate. Amongst the liquid metals with melting points below room temperature, Gallium alloys (such as Gallinstan, 68.5% Ga, 21.5% In, 10% Sn) were selected since they are non-toxic. Galinstan also wets well to other metal surfaces, unlike Mercury, which improves electrical contact performance.

In the proposed approach, high aspect-ratio SU-8 interconnect structures were partially filled with a (room temperature) liquid metal, which were then mated with vertical metal pin interconnects on the matching die, acting in a sense as a micro-scale shock absorber. Figure 4

[1] Krishna's Ph.D. research also includes analysis of non-linear effects in RF MEMS devices and several additional publications not reported in this progress report are related to this work.

shows the CPW-based test structure for investigating the liquid-metal interconnect approach. For the preliminary study, silicon was used for both the top chip and bottom carrier substrates.

The process for depositing the liquid metal into the holes is straightforward. First drops of liquid metal were deposited on the surface of the SU-8 above the holes. Then, a rubber tool was used to force the liquid metal into the holes where it wets to the underlying CPW metal – basically a simple "micro-squeegee" approach. The top test chip structure was fabricated using a similar high-aspect-ratio process based on KMPR resist to form the electroplating mold for the vertical metal pins. The fabricated test structures are shown in Figure 5. In a final assembly step, the vertical metal posts on the top chip are "plugged" into the liquid-metal-filled sockets on the bottom test chip.

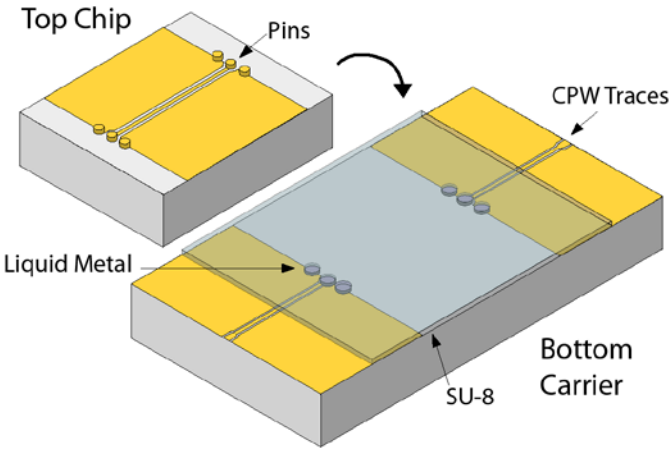

Figure 4: Coplanar-waveguide-based test structures for RF vertical liquid metal interconnects.

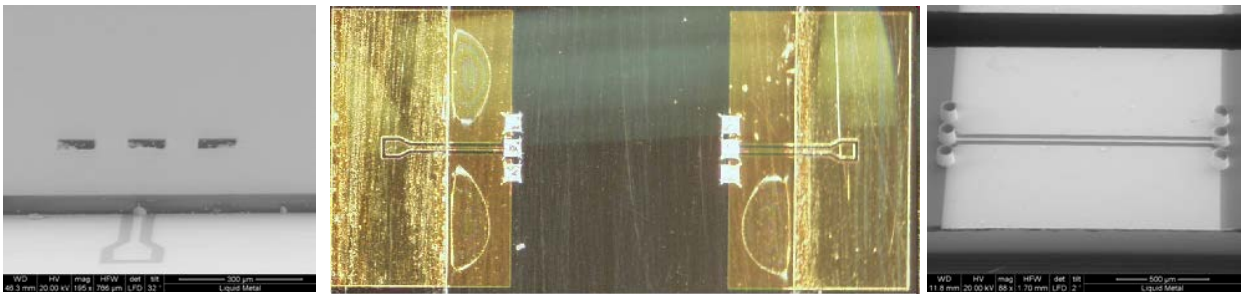

Figure 5: (left) SEM photograph of the fabricated structure, the darker gray region is the patterned SU-8. (center) Micrograph of the fabricated structure with liquid metal deposited in the holes. (right) SEM photograph of the top structure showing fabricated metal posts.

The S-parameters of the assembled structures were measured using wafer probes, and the loss of single transitions de-embedded from the measurements (Figure 6). Thermal cycling measurements consisting of more than 100 thermal cycles with temperatures varying from -40°C to 125°C over 80 minute intervals were also performed, indicating little effect on performance. The loss of the interconnects is ~0.4-0.5 dB up to about 20 GHz, and then starts to increase due to impedance mismatches arising from capacitive parasitics. The capacitive parasitics can be reduced by scaling the interconnects to smaller footprint dimensions, allowing for broader band high frequency operation.

The transition loss is believed to be dominated by the contacts between the liquid metal and the underlying CPW and the vertical pins; this is an area that bears further investigation. Note that the performance of the transition improved after thermal cycling, which may indicate an annealing effect on the metal-liquid metal interface. We also observed a decrease in the DC resistance with increasing current, which indicates that the interconnect performance may improve as the liquid metal is heated.

A paper on these results was presented at the *2009 International Microwave Symposium* [4]. A patent disclosure was also filed on the liquid metal vertical interconnect concept [5].

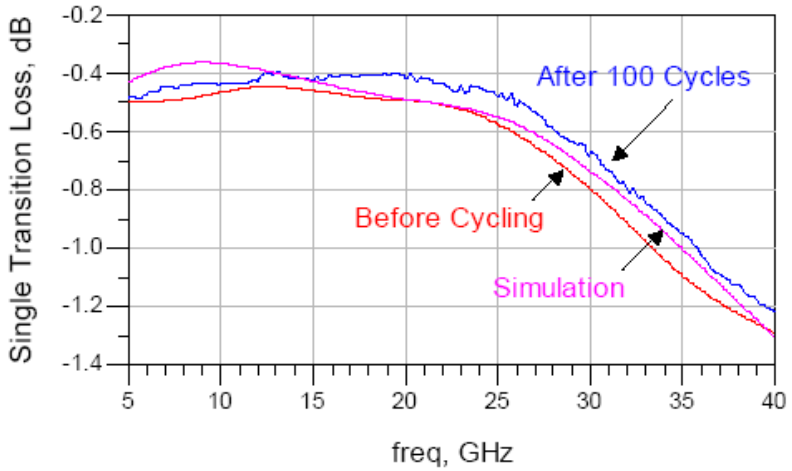

Figure 6: Simulated and measured (before and after thermal cycling) transition loss for liquid metal interconnects.

In the next stage of this work, an active 4.9-8.5 GHz GaAs power amplifier MMIC chip (Cobham MAAM-007523 chip) was heterogeneously integrated with a passive CPW probe transition network on the carrier substrate using the liquid metal vertical interconnect process. GaAs is an attractive material for these investigations since it has one of the largest CTE mismatches relative to silicon of the standard semiconductor materials used for MMICs. The collaboration with Cobham also provides a potential transition path for the liquid metal interconnect technology if proven to be beneficial.

Figure 7 shows a diagram of the proof-of-concept liquid-metal flip-chip scheme with GaAs MMIC, and an SEM micrograph of a flip-chip assembled MMIC on CPW carrier substrate.

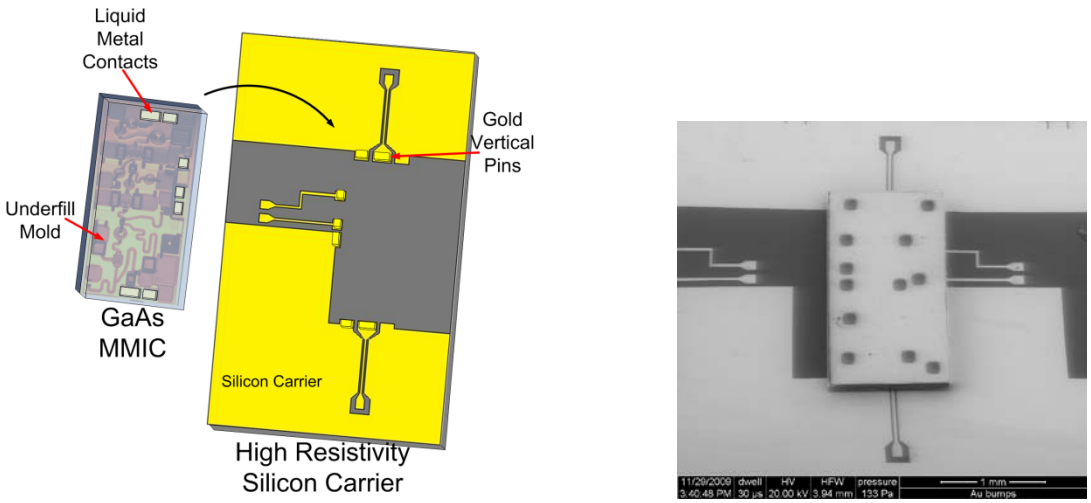

Figure 7: (Left) Diagram of liquid metal flip chip scheme with GaAs MMIC. (Right) SEM image of GaAs MMIC flip-chip mounted on the Si substrate with liquid metal interconnects.

Figure 8 shows the process flow for fabricating the liquid metal contacts on the GaAs MMIC chip. Due to the difficulty in depositing controlled amounts of liquid metal using the previous "squeegee" method [2], an innovative approach was developed by Parrish Ralston for the liquid metal deposition steps. In this approach, small micromachined cavities in a silicon handle wafer are filled with liquid metal and then frozen. The small frozen (liquid) metal pieces can then be straightforwardly transferred to the SU-8 receptacles on the target chip or substrate at which point they return to liquid state at room temperature, greatly improving control of the deposition.

Figure 9 shows the process flow for fabricating the corresponding metal pins on the silicon carrier substrate and final assembly of the chip. This approach was initially selected due to the relative simplicity of electroplating the metal pins on the carrier side. However, this is not the most ideal approach due to the fact that the SU-8 structures fabricated on the GaAs MMIC side result in additional parasitics that were not accounted for in the original MMIC design, and result in some detuning of performance. This could certainly be accounted for at design time, but a preferred approach is to fabricate the metal pins on the MMIC itself and the SU-8/liquid metal structures on the carrier substrate, and then flip chip with the pins inserted down into the liquid metal contact structures. The inductances of the pins would still need to be accounted for in design, but there would be much reduced parasitics due to the SU-8 structures as compared to the previous approach.

An alternative process was also developed that fabricates the gold pins on the MMIC chip, as shown in Figure 10. SU-8 structures are defined and liquid metal deposited on the carrier substrate side in a similar process to Fig. 2 above. The MMIC chip with gold posts is then flip chipped onto the carrier with corresponding liquid metal contacts. Unfortunately, fabrication issues ultimately prevented a full demonstration of this alternative process flow during the period of performance of the grant.

a) Spin and pattern thick photoresist onto sacrificial silicon wafer.
b) DRIE anisotropic cavity into Si wafer.
c) Place GaAs MMIC into cavity.
d) Spin and pattern thick photoresist, SU-8, on entire Si wafer and pattern to form holes over the bond pads.
e) Manually deposit frozen liquid metal in SU-8 cavities.

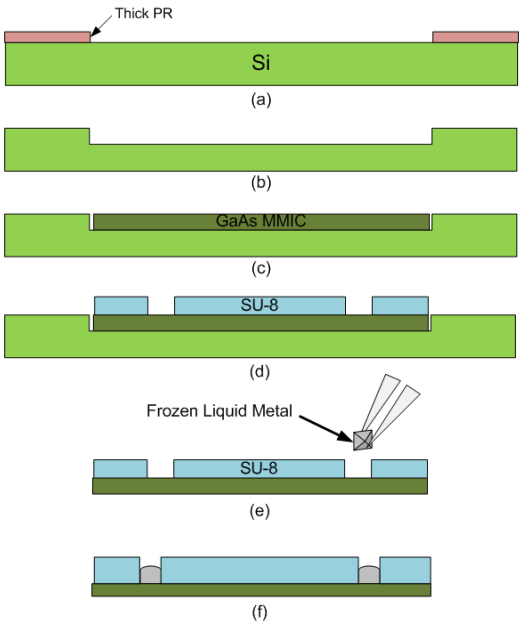

Figure 8: Process flow for liquid metal deposition on the MMIC chip.

a) Deposit titanium seed layer.
b) Pattern the titanium/gold CPW traces using a liftoff process.
c) Deposit and pattern KMPR for electroplating mold.
d) Electroplate gold pins.
e) Remove KMPR, remove the Ti seed layer, mount the GaAs chip onto the Si substrate.

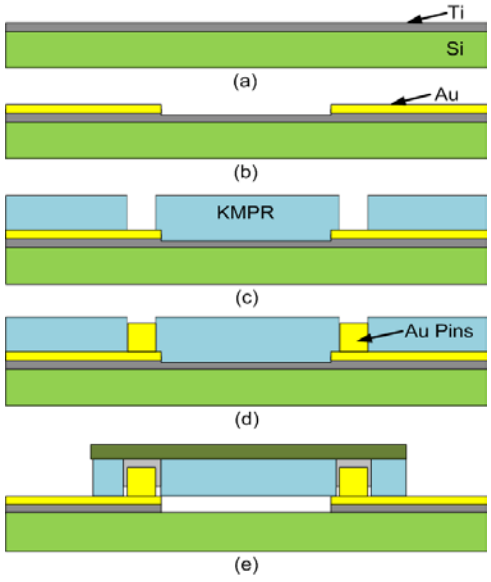

Figure 9: Process flow for fabrication of metal pins on the carrier substrate and final assembly of MMIC chip.

a) Spin and pattern thick photoresist onto sacrificial silicon wafer.
b) DRIE anisotropic cavity into Si wafer.
c) Place GaAs MMIC into cavity.
d) Spin and pattern thin film photoresist onto Si wafer.
e) Deposit titanium/gold seed layer onto surface of the silicon wafer.
f) Deposit and pattern KMPR for electroplating mold .
g) Remove KMPR and lift off thin film resist.

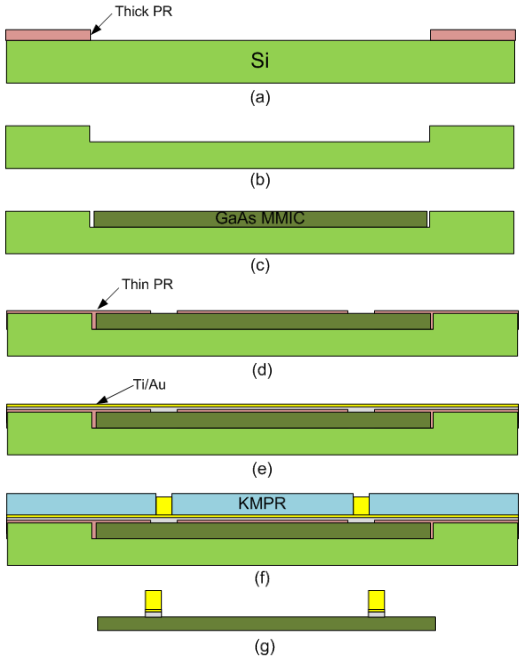

Figure 10: Process flow for fabrication of metal pins on the MMIC chip. SU-8 structures are defined and liquid metal deposited on the carrier substrate side in a similar process to Fig. 2 above. The MMIC chip with gold posts is then flip chipped onto the carrier with corresponding liquid metal contacts.

The S-parameters of the assembled amplifier structures (SU-8/liquid metal contacts on the MMIC side) were measured using ground-signal-ground (GSG) probes in contact with the CPW pads on the carrier substrate. These measurements were compared to bare die wafer-probe measurements of the MMIC probes themselves (Figure 11). The measurement of assembled structures is comparable with the bare die measurements, but with some degradation in gain and some shift in the input match. These deviations may be attributable to the parasitics due to the SU-8 structures on the MMIC chip, and also insufficient ground connection to the MMIC backside plane. The loss of single transitions were also de-embedded from the measurements and showed an average transition loss of ~1.7 dB. This loss is somewhat excessive, but is likely attributable to the observed amplifier gain degradation. A paper on these results was presented at the *2010 International Microwave Symposium* [6].

Liquid Metal Vertical Interconnects in Polystrata Technology

Following the above heterogeneous integration technology development on silicon CPW substrates, we extended the liquid metal vertical interconnect technology to the Nuvotronics Polystrata process. Polystrata is a multiple layer electroplating process (Figure 12) that enables complex 3D waveguiding structures with air dielectrics, resulting in very low loss at microwave/millimeter-wave frequencies. However, in order to fully realize the potential of this technology, it must be heterogeneously integrated with active circuits in various semiconductor technologies. We subsequently recognized that the liquid metal interconnect technology discussed above would be a potentially ideal candidate for active circuit integration in Polystrata.

The Polystrata-liquid metal integration efforts were conducted by Virginia Tech Ph.D. students Parrish Ralston and J. Marcus Oliver[2]

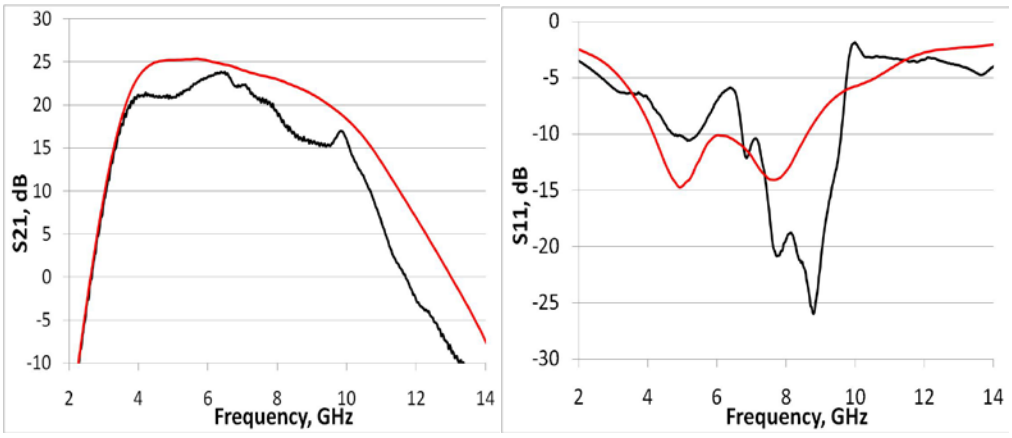

Figure 11: Measured S-parameters of the heterogeneously integrated MMIC power amplifier. The red curves are on-chip probe measurements of the MMIC amplifier itself. The black curves are the measured results with the liquid metal interconnects and silicon carrier substrate with CPW feedlines. The average deembedded transition loss over the 4.9-8.5 GHz operating range is ~1.7 dB.

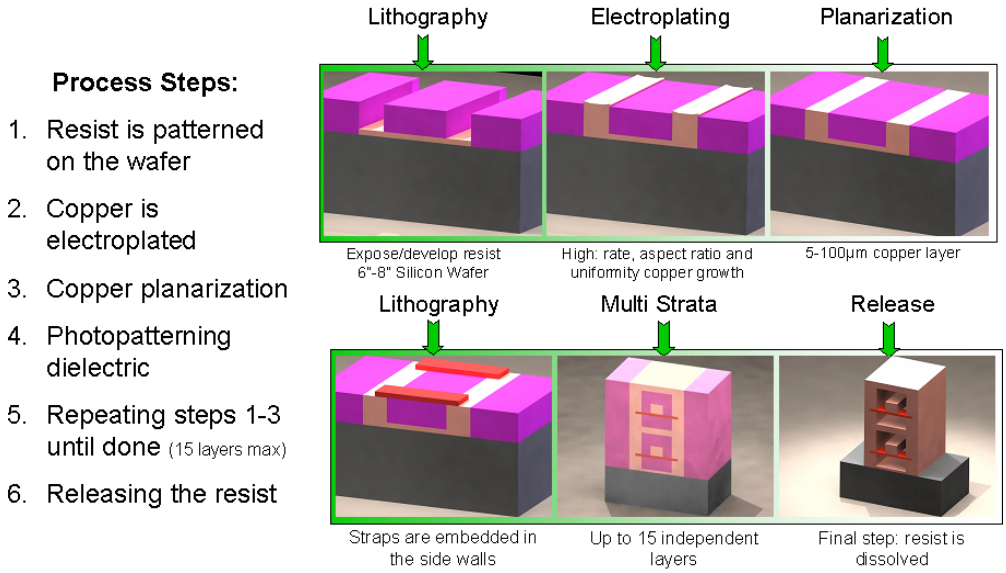

Figure 12: Nuvotronics Polystrata process flow. 15+ layers of Polystrata are possible, enabling complex 3D microwave structures.

This work was conducted in parallel with the various Polystrata mm-wave component development and MMIC integration efforts conducted with Nuvotronics under separate funding. For example, we developed W-band cavity backed antenna arrays (Figure 13, [7]) and a compact

[2] Marcus Oliver graduated with his Ph.D. requirements Spring semester 2012 and subsequently joined Nuvotronics, Radford, VA, as a member of the technical staff. Marcus continues to collaborate with VT personnel on various Polystrata integration projects.

W-band passive monopulse comparator network integrated with a similar 2x2 Polystrata antenna array (Figure 14, [8]). More recent work has focused on power combiners/splitters and integration with MMIC power amplifiers.

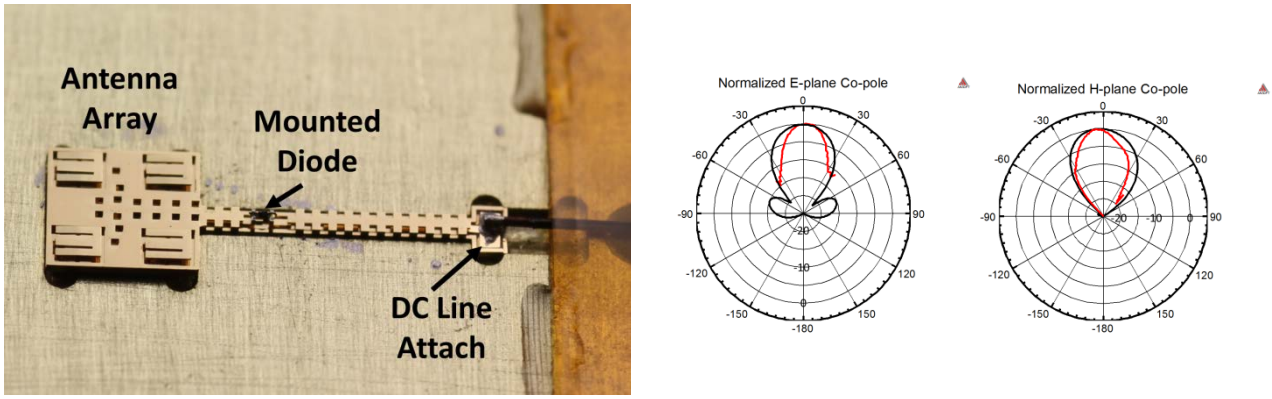

Figure 13: (Left) Mounted Polystrata antenna array with integrated diode detector and DC line. Diode and DC line are attached using silver conductive epoxy. (Right) Normalized E and H plane co-pol patterns: black – simulated with HFSS, red – measured [7].

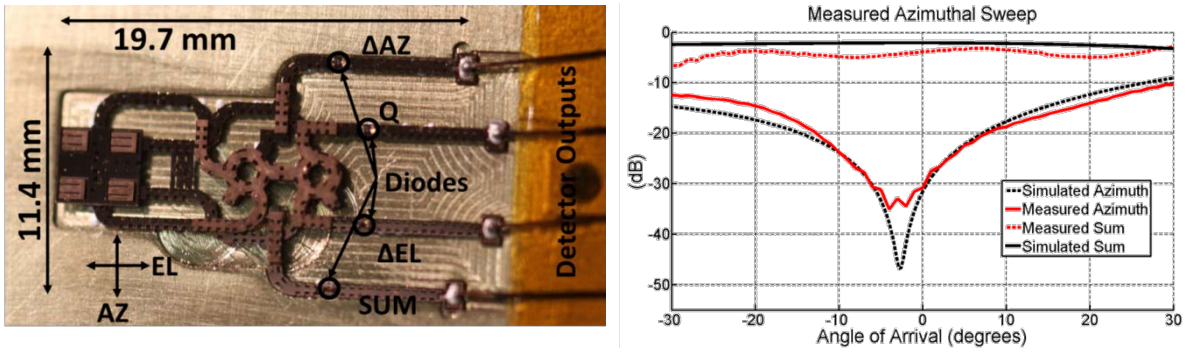

Figure 14: (Left) Polystrata W-band passive monopulse comparator integrated with a 2x2 antenna array and detector arrays, and (Right) comparison of measured and simulated azimuthal sum (Σ) and difference (ΔEL) patterns [8].

Figure 15 shows the process flow developed by Parrish Ralston for liquid metal interconnect deposition on prefabricated Polystrata structures, with metal pins fabricated on the Polystrata side of the assembly. The post-processing steps on the MMIC consist of definition of SU-8 cavities at the contact locations and then deposition of frozen liquid metal pieces into the cavities using the same process as presented in [6]. The MMIC is then flip-chipped onto the Polystrata frame with metal pins at the contact locations.

Figure 16 shows a 3D CAD rendering of the MMIC test structure fabricated for investigation of this approach. The M/A-COM 1629 two-stage GaAs driver MMIC, a very similar MMIC design to the one used in prior experiments, was utilized for the Polystrata integration experiments. The Polystrata test structure includes RF and DC probe pads corresponding to the MMIC layout, and a thermal/grounding backplane is co-fabricated in Polystrata for bonding to the backside of the MMIC. The backplane structure is an artifice needed due to the fact that the MMIC used was

designed for conventional wirebonding into a package, and therefore relied on backside grounding for design performance; this structure would not be required for MMICs specifically designed for flip-chip integration with Polystrata.

a) Place MMIC chip in DRIE-etched Si cavity.

b) Deposit and pattern SU-8 sockets over MMIC bond pads.

c) Remove chip from Si cavity and bond to copper backplane with H20-E conductive epoxy.

d) Place frozen liquid metal into SU-8 sockets.

e) Flip chip connection to PolyStrata frame.

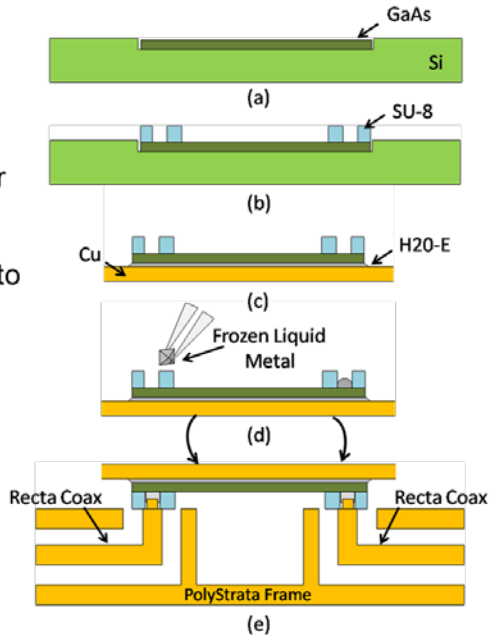

Figure 15: Process flow for liquid metal deposition on Polystrata structures. The MMIC chip has fabricated SU-8 sockets for liquid metal deposition, and is flip-chipped onto the Polystrata structure with metal pins.

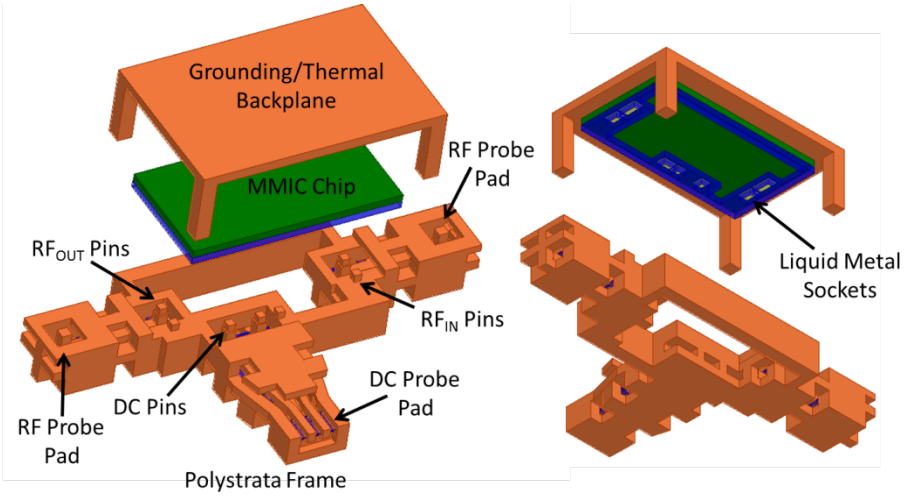

Figure 16: CAD view of Polystrata test structure for liquid metal integration of GaAs MMIC power amplifier.

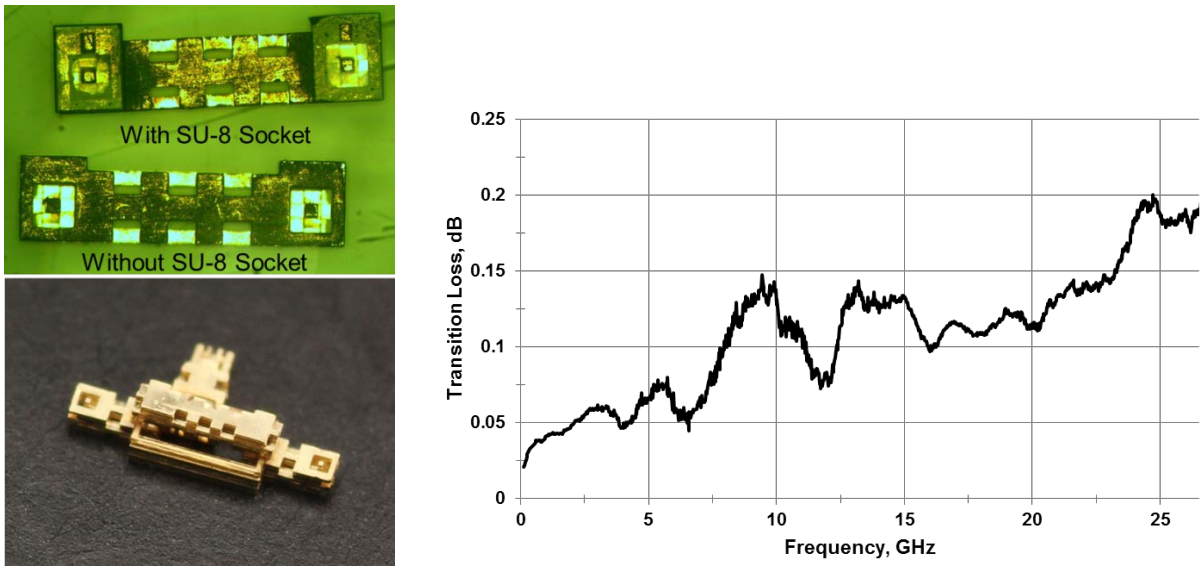

Figure 17: (Left) Micrograph of fabricated Polystrata test structure with rectacoax through line "jumper" in place of MMIC for structural validation and calibration purposes. (Right) Measured transition loss deembedded from two-port S-Parameter measurements of the Polystrata jumper structure.

In addition to the MMIC test structure, a Polystrata through "jumper" assembly was fabricated and integrated to enable characterization of the liquid metal Polystrata interconnections themselves. The jumper is designed to mate directly to the same vertical transitions implemented for the MMIC integration. Figure 17 shows microscope photographs of the fabricated Polystrata jumper test structure, and the measured transition loss deembedded from two-port S-parameter measurements of this structure. Over a range of 10MHz – 26.5GHz, the average loss per transition is 0.11dB; over the design bandwidth of the MMIC, the average loss is 0.08dB.

Figure 18 shows pictures of the fabricated Polystrata liquid metal interconnect MMIC test structure and the measured performance of the assembly compared to the directly probed MMIC performance. As can be seen, there is very good agreement between probed data and measured liquid metal assembly data. However, the deembedded average transition loss over the MMIC operating frequency range (4.9-8.5 GHz) is ~0.7dB, which is significantly higher than the through jumper measurements described above. The additional transition loss may be due to radiation losses, impedance mismatch issues arising from the SU-8 proximity to microstrip/inductors in the transistor matching networks, and, possibly, inadequate thermal grounding. The impedance matching issues may be reduced in the future by specifically designing the MMICs for such a liquid metal flip-chip transition structure, and by fabricating the pins on the MMIC side and the liquid metal sockets on the Polystrata side. Thermal management issues will require further investigation.

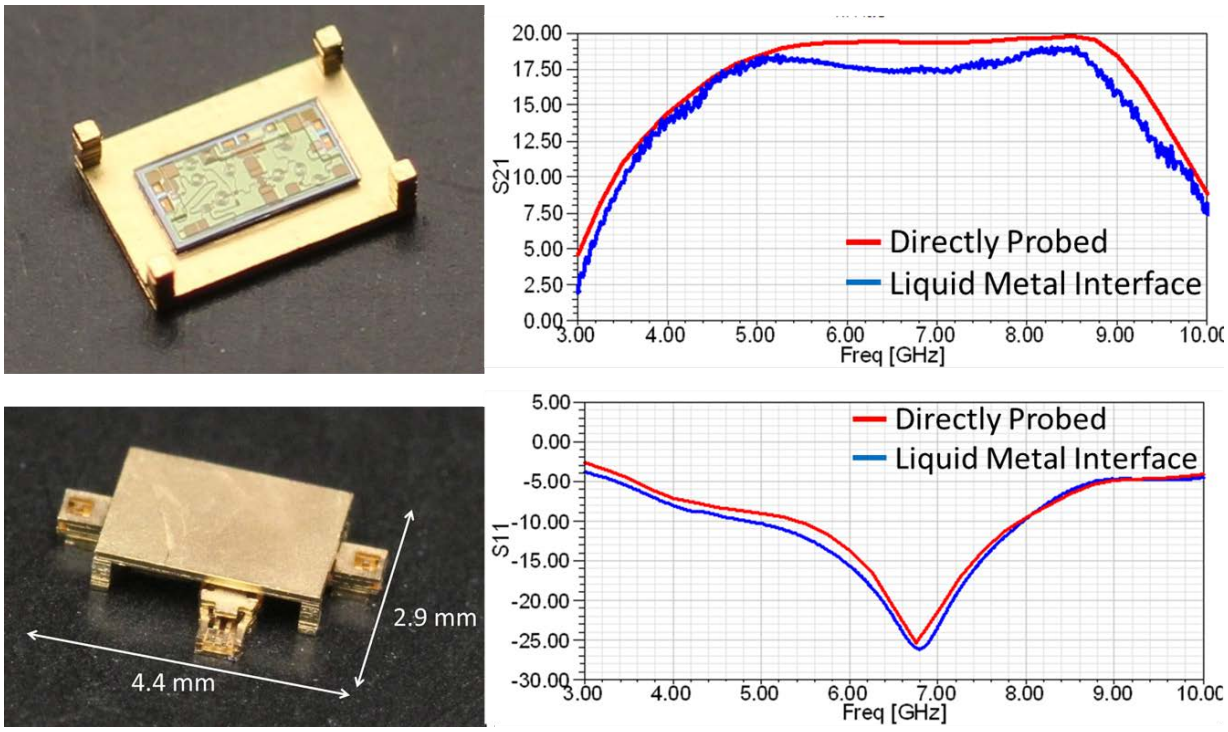

Figure 18: (Left) Microscope photographs of MMIC, with SU-8 liquid metal contact sockets, bonded on Polystrata thermal/grounding backplane, and then flip-chipped onto the Polystrata 3D interconnect test structure. (Right) Measured S-parameters of the liquid metal interconnect MMIC test structure compared to directly probed MMIC performance.

This Polystrata liquid metal interconnect MMIC integration work was initially reported at the *2011 IEEE Compound Semiconductor IC Symposium* [9], and was subsequently invited to be submitted as an expanded journal paper to the *IEEE Journal of Solid State Circuits*.

In the expanded journal paper a *single-interconnect* structure (as opposed to the two-port "jumper" structure discussed above) was introduced that enables direct deembedded RF measurement of the transition loss of a single liquid metal interconnect. Figure 19 shows renderings and a micrograph of the single-interconnect test structure. TRL calibration structures were also fabricated in the Polystrata run to facilitate calibration to reference planes directly on either side of the single transition. Figure 24 shows measured results in comparison to 3D full-wave HFSS simulations, and simulations of an extracted lumped element model. A scalable lumped element model was developed to enable designers to quickly simulate these interconnects in more complex circuits.

The expanded paper appeared in the October 2012 issue of the *IEEE Journal of Solid State Circuits* [10].

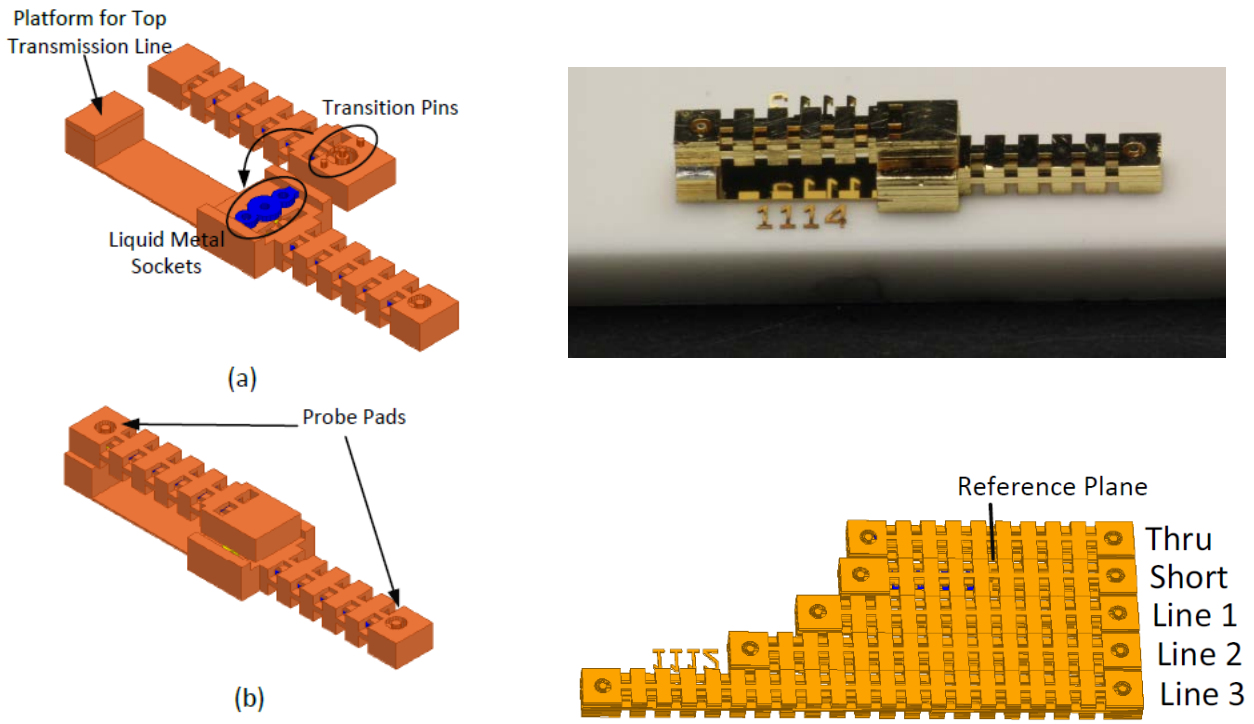

Figure 19: (Left) 3D renderings of a single PolyStrata liquid metal transition, (a) prior to assembly, showing the PolyStrata pins and (b) after assembly. (Right, top) A micrograph of a complete single transition assembly on an alumina substrate. (Right, bottom) Rendering of the TRL structure which was used for deembedding the probe points and transmission line features of the single transition assembly.

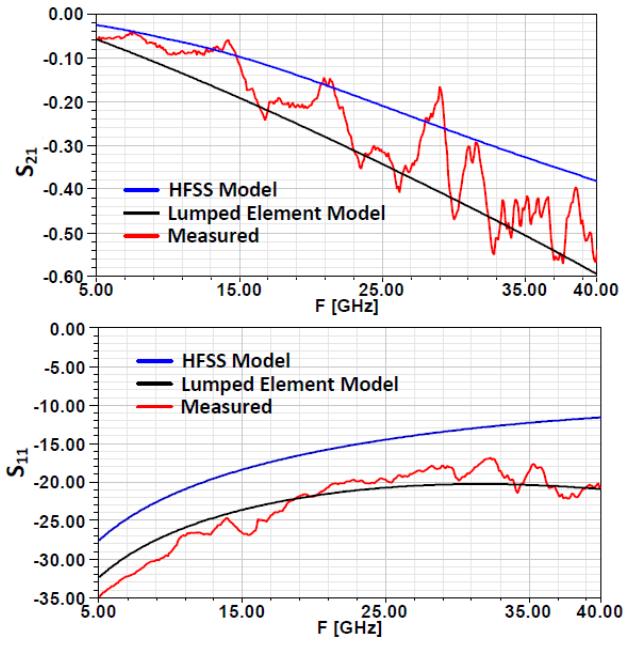

Figure 20: A comparison of a single liquid metal interconnect assembly measured results with HFSS simulation results and simulations of the extracted lumped element model of the assembly.

In addition to the Polystrata-MMIC integration demonstration, additional test structures were fabricated and employed for both temperature cycling and high-power microwave measurements. Temperature testing is important for two reasons: liquid metal interconnects will transition from liquid to solid when operating at low temperatures, and thermomechanical robustness is a key figure of merit for the proposed liquid metal interconnection. Power handling testing verifies that sufficient levels of high frequency current can be carried by liquid metal interconnections with minimal deterioration in performance, validating that the interface between the liquid metal and pad/pin surfaces is conformal and stable enough for high current conditions.

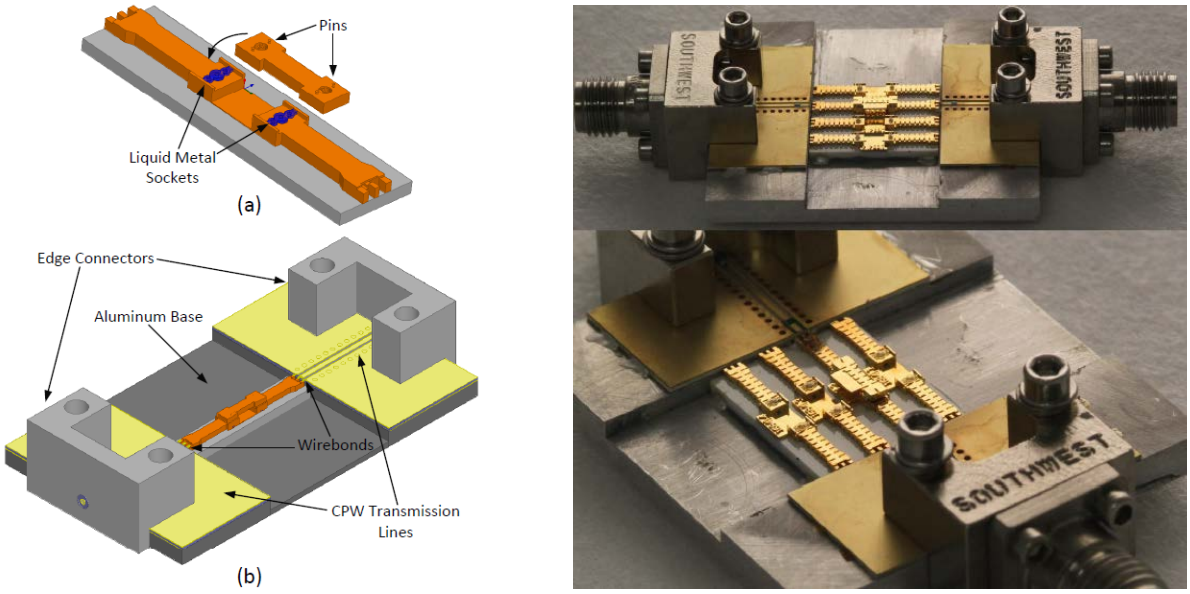

Figure 21: (Left) Renderings of (a) the high power PolyStrata liquid metal test transmission line, and (b) the completed high power test fixture. (Right) Photographs of the complete power test fixture assembly.

Figure 21 shows renderings and photographs of the temperature and power handling test structures. Reference “through line” structures were also previously characterized for power handling [11], and this provided a baseline to compare the power handling of the Polystrata liquid metal interconnects against. High power testing was performed at a continuous wave (CW) frequency of 2 GHz. Using standard, 50 Ω loads in a power test set up, an average of 1.4 A of AC current was passed through liquid metal interconnections. As seen in

Figure **22**, changes in the overall performance of the liquid metal interconnect test structure after high power testing were small. Over a frequency range of 0.01 - 8GHz the average transmission loss for each measurement varies from 0.65dB for the baseline measurement to 0.62dB for the measurement taken after applying 100 W of power to the liquid metal test fixture. The small dips in transmission loss in the 50W data set at 3.7 GHz and 4.6 GHz are likely due to the movements in the cable assembly creating slight resonances. Negligible changes in the overall performance of these high power, liquid metal interconnect test fixtures verify that these interconnects can withstand at least 100 W of CW power and 1.4A of current at 2 GHz. This performance exceeds

that of 1 mil wirebond interconnections and is comparable to the performance of flip chip solder connections.

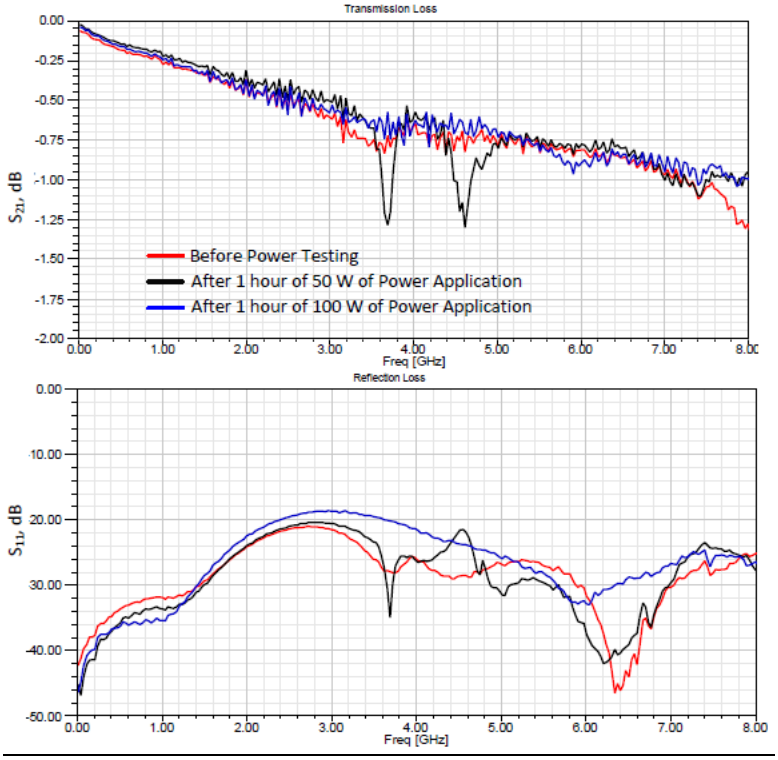

Figure 22: S parameter data of the liquid metal test fixture before and after high power testing.

The test fixture shown in Figure 21 was placed directly on a small ceramic heater attached to a thermally isolating platform for the temperature cycling measurements. The heater, with temperature control range from 0°C to 300°C, has a built-in thermocouple so that temperature of the ceramic was always known. The temperature of the thermally isolating platform, the ceramic heater, and the assembly can also be lowered by introducing dry ice around the platform and then insulating the test station with a Styrofoam box. This method allowed the temperature of the liquid metal assembly to reach a steady state temperature as low as -25°C. Once at this temperature, the dry ice was removed from the test fixture and the interconnect assembly allowed to warm to 0° C. After the temperature of the assembly exceeded 0°C, the ceramic heater was used to control the ramp up of temperature, until the assembly reached a temperature of 125°C. Small signal S-parameter data was recorded each time the temperature of the assembly increased by 10-15°C during this testing cycle.

The measured data reveals some unique behavior of metals that are under strain while approaching their melting point. As the temperature of the assembly was brought down to -25°C quickly, and while at this temperature, the S- parameter data changed little. The overall transmission loss of the assembly was reduced slightly, which is expected since resistive properties of metal are directly proportional to metal's temperature. However, as the temperature was slowly raised to a value close to Galinstan's melting point, creep deformation becomes more and more of a factor. Figure 23 compares the difference in transmission loss of the assembly at various temperature *relative to the transmission loss of a room temperature assembly*, where:

$$\Delta S_{21} = S_{21@TEMP} - S_{21AMBIENT} .$$

As the assembly warms to 0°C, the performance of the assembly drops off dramatically. As the temperature of the assembly exceeds the melting temperature of the Galinstan, the interconnect "repairs" itself; the average ΔS_{21} is less than -0.1dB for measured data at temperatures exceeding 45◦ C. This experiment was repeated multiple times and each time the results were very similar, with the performance of the assembly falling off as its temperature exceeded -10°C but then quickly recovering as the assembly temperature approached and exceeded room temperature. This performance deterioration of liquid metal connections while the metal is in a solid phase could potentially be a serious problem for applications that have "cold start" requirements. One solution that would alleviate this issue is the utilization of a liquid metal that has a lower melting point, such as different Galinstan alloys or mercury (albeit, with toxicity issues).

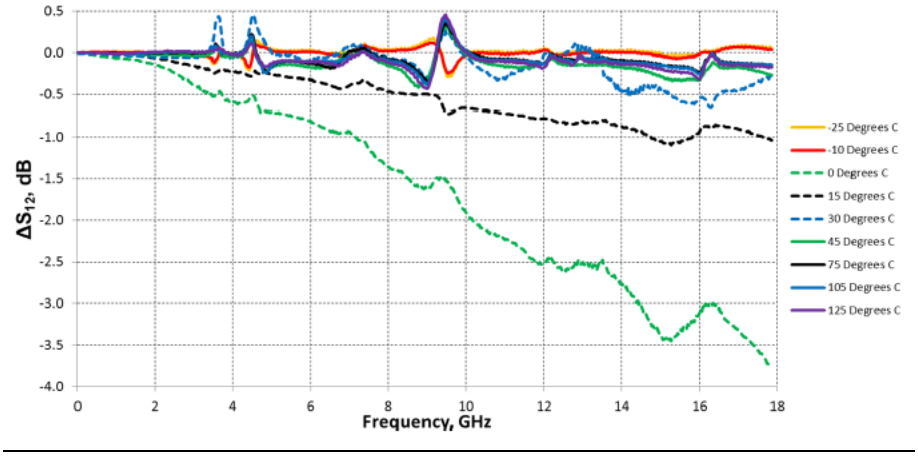

Figure 23: A comparison of the liquid metal assembly's transmission loss at different temperatures, *normalized to the performance of a liquid metal assembly at room temperature*. (Note that this data is in terms of ΔS_{21}, not S_{21}, which is why it is able to go above zero at some points in the frequency sweep).

The above high-power and temperature cycling characterization work has been submitted for publication in *IEEE Transactions on Microwave Theory and Techniques* [12].

Future Work

Future work indicated by this project includes a more extensive verification of liquid metal interconnects for commercial and military assemblies, for example, more extensive testing in accordance with MIL-STD-883. Another important area for future work is in the manufacturability of liquid-metal flip-chip interconnects at the chip or wafer scale. The liquid metal interconnect-based assemblies described in this dissertation were fabricated in a research and development lab environment; developing processing techniques for larger scale manufacturing is another essential step in making this type of interconnect a practical alternative to wirebonding or flip chip bonding. Particular topics that should be addressed in future work include: plating or bumping copper pillars onto MMICs at the wafer scale; surface finishing of

liquid metal interconnect pads in order to minimize resistive losses and enhance long term reliability; and parallel injection of liquid metals into sockets at the wafer-scale.

In addition, as mentioned above, W-band Polystrata monopulse antenna arrays and processor ICs are also under development at Nuvotronics under separate DoD finding. Future work is envisioned at the convergence of these two projects, and would involve development of the interconnect and coupling networks required to embed the processor IC within the Polystrata antenna and feed network structure using liquid metal interconnects (Figure 24).

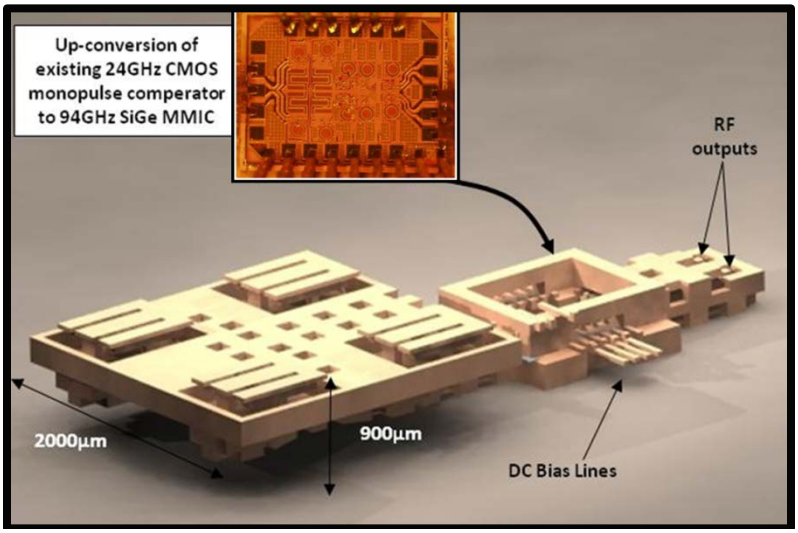

Figure 24: Proposed Polystrata monopulse architectures utilizing W-band cavity-backed patch antennas (top) fully passive monopulse comparator and antenna array (bottom) antenna array with integrated monopulse comparator IC.

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(* indicates students that have been supported by this ARO grant)

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