ARL-TR-8843 ● Oct 2019

V-Band Power Amplifiers in 90-nm Gallium Nitride (GaN)

by John E Penn and Khamsouk Kingkeo

NOTICES

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V-Band Power Amplifiers in 90-nm Gallium Nitride (GaN)

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Sensors and Electron Devices Directorate, CCDC Army Research Laboratory

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14. ABSTRACT

The CCDC Army Research Laboratory (ARL) has been evaluating and designing efficient broadband high-power amplifiers for future adaptive multimode radar systems in addition to other circuits for use in communications, networking, and electronic warfare. ARL successfully tested V-band power amplifiers using a 90-nm gallium nitride process being developed by Qorvo. This technical report summarizes the test results from the ARL die.

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1. Introduction

The CCDC Army Research Laboratory (ARL) has been evaluating and designing efficient broadband high-power amplifiers for future adaptive multimode radar systems in addition to other circuits for use in communications, networking, and electronic warfare (EW). ARL submitted several designs for fabrication as part of a collaborative research agreement with Qorvo and with our colleagues at the US Air Force Research Laboratory (AFRL) as part of an AFRL-led effort. The designs used a developing high-performance research gallium nitride (GaN) foundry process from Qorvo based on 0.09-µm high-electron-mobility transistors (HEMTs). A prior technical report documents the designs[1], with testing of the actual designs presented in this report.

2. ARL Die Plot

The fabricated designs submitted by ARL were placed on a 1.35-mm × 4.0-mm die site (Fig. 1). At the far left of the die is a very broadband distributed amplifier (DA) with gain to about 50 GHz using five parallel common source 2- × 40-µm HEMTs, while to its right is a similar DA with the first stage using a larger 4- × 40-µm HEMT for an expected improvement in efficiency but with a slightly lower gain bandwidth, up to 45 GHz.

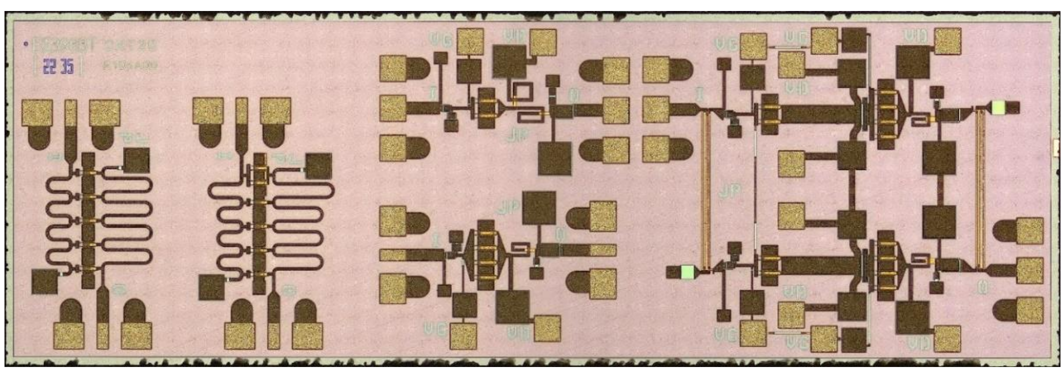

Fig. 1 Die photo of ARL power amplifiers and distributed amps (1.35 × 4.0 mm)

A two-stage power amplifier (PA) was designed to provide 1 W over at least a 10-GHz bandwidth, approximately 40 to 50 GHz. The 1-W PA (far right), one-stage 1/4-W PA (top middle), and one-stage 1/2-W PA (bottom middle) complete the die layout. The one-stage 1/4-W PA was deliberately placed next to the 1-W amplifier so that it could be ribbon bonded and tested as a three-stage PA with nearly 30 dB of small signal gain. The 1/4-W output power was shown to be sufficient to drive the two parallel first stages of the 1-W two-stage PA.

3. One-Stage 1/4-W Power Amplifier

The initial design goal was for at least 1 W of power over a 40- to 60-GHz band which, given the tradeoffs of efficiency, power, gain, stability, and available design time, quickly resulted in a compromise to limit bandwidth to about half of that initial 20-GHz bandwidth goal. While the larger 0.5-mm HEMT had a little less gain than the 0.25-mm HEMT, it had sufficient gain at 50 GHz for a simple two-stage design, with the 0.25-mm HEMT driving the 0.5-mm HEMT for an expected 1/2 W of output power from 45 to 55 GHz.

Both the driver and output stage PA were fabricated as individual one-stage amplifiers, and each achieved about 10 GHz of gain bandwidth with about 10 dB of small signal gain. Each single-stage PA achieved 1 W/mm (HEMT periphery) within the band. Figure 2 shows a plot of the single-stage 1/4-W PA (4 × 62.5 µm), which was flipped vertically on the die layout to put the gate and drain DC bias pads on the top edge of the fabricated die. There was variation in performance among the few die tested, but there was good agreement between the test results and the nominal simulations. Figure 3 shows good agreement in small signal s-parameters for two measured PAs (solid) versus the simulations (dotted) at a nominal DC bias of 13 V and 100 mA/mm drain-source current (IDS).

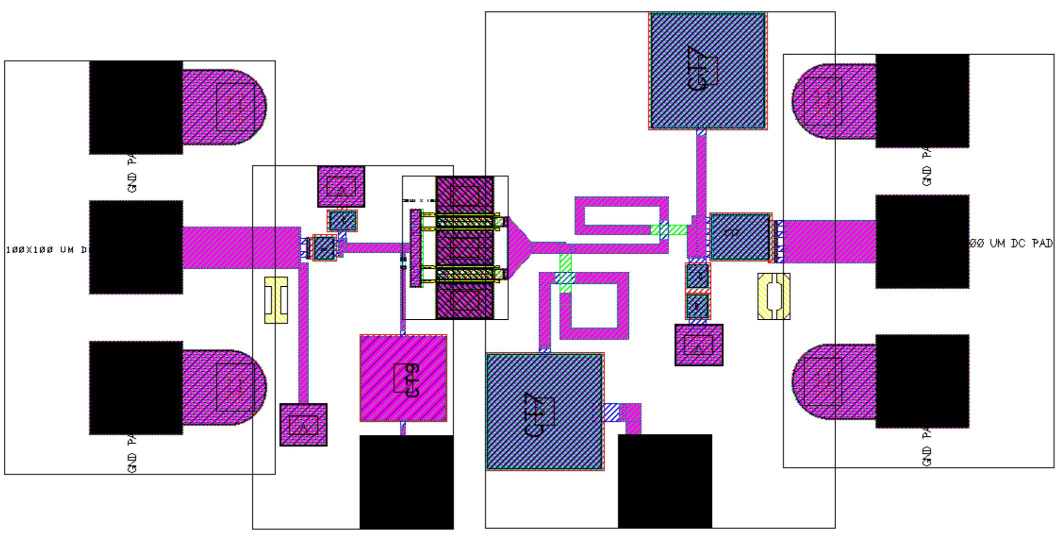

Fig. 2 Plot of one-stage 0.25-W PA (4 × 62.5 µm)

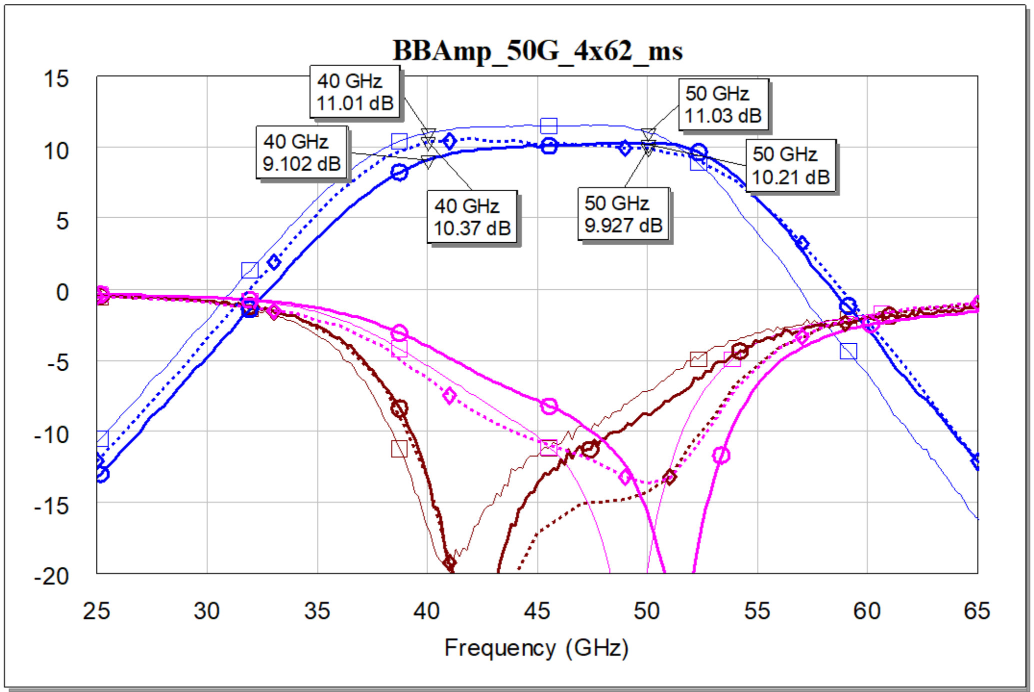

Fig. 3 Simulation and measurement of one-stage 0.25-W PA (4 × 62.5 μm)

Power and efficiency were measured for several die. Large 100-pf and 1000-pf caps had to be wire bonded to the bias pads to quell low-frequency oscillations (near 10 MHz) during the probe testing. Measurements at 12-V bias, near the 13-V target bias, resulted in nearly similar output power but slightly better efficiencies than the 13-V measurements. The output power goal was achieved from 40 to 50 GHz, but power added efficiencies (PAEs) were better over 42.5 GHz to 47.5 GHz, so those results are shown for one die at nominal bias. Figure 4 shows the PAE (blue) and output power (magenta) with simulations (dotted) versus measured (solid) at 42.5 GHz. Likewise, Fig. 5 shows power performance simulations versus measurements at 45 GHz with nearly 38% peak PAE, similar to the peak PAE at 42.5 GHz. Figure 6 shows power performance at 47.5 GHz with the measured PAE close to the simulated peak PAE.

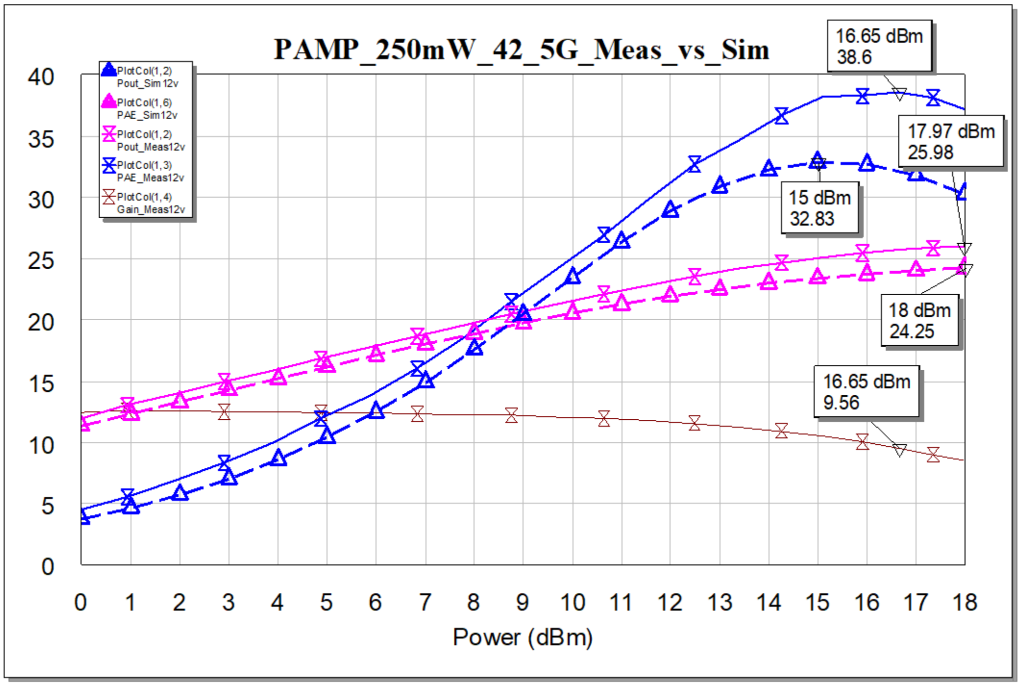

Fig. 4 Power performance simulation vs. measurement of one-stage 0.25-W PA (42.5 GHz)

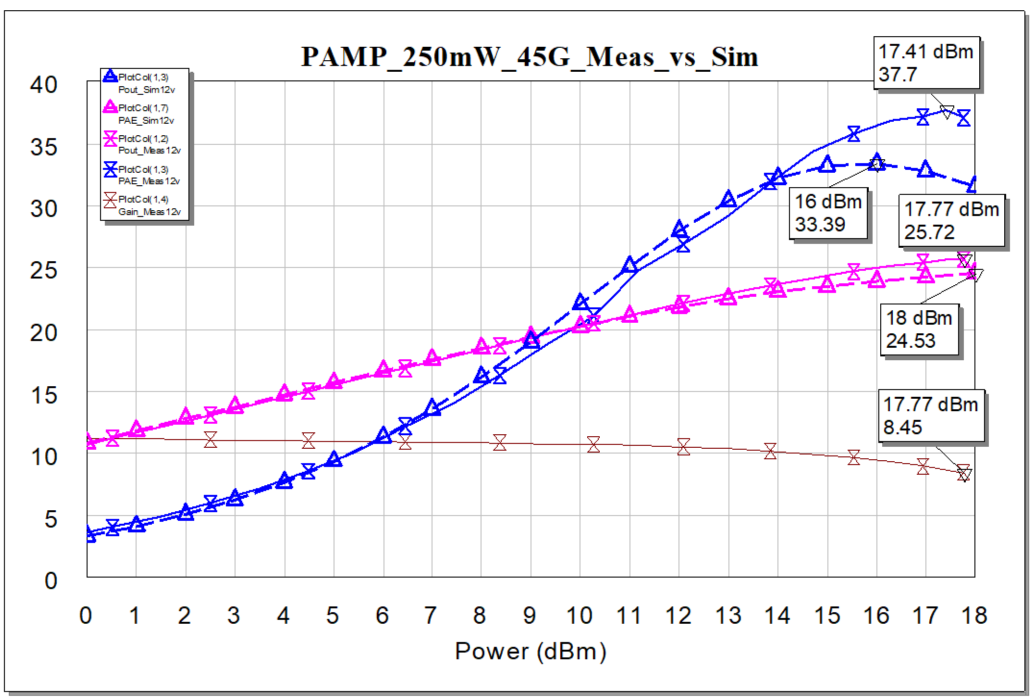

Fig. 5 Power performance simulation vs. measurement of one-stage 0.25-W PA (45 GHz)

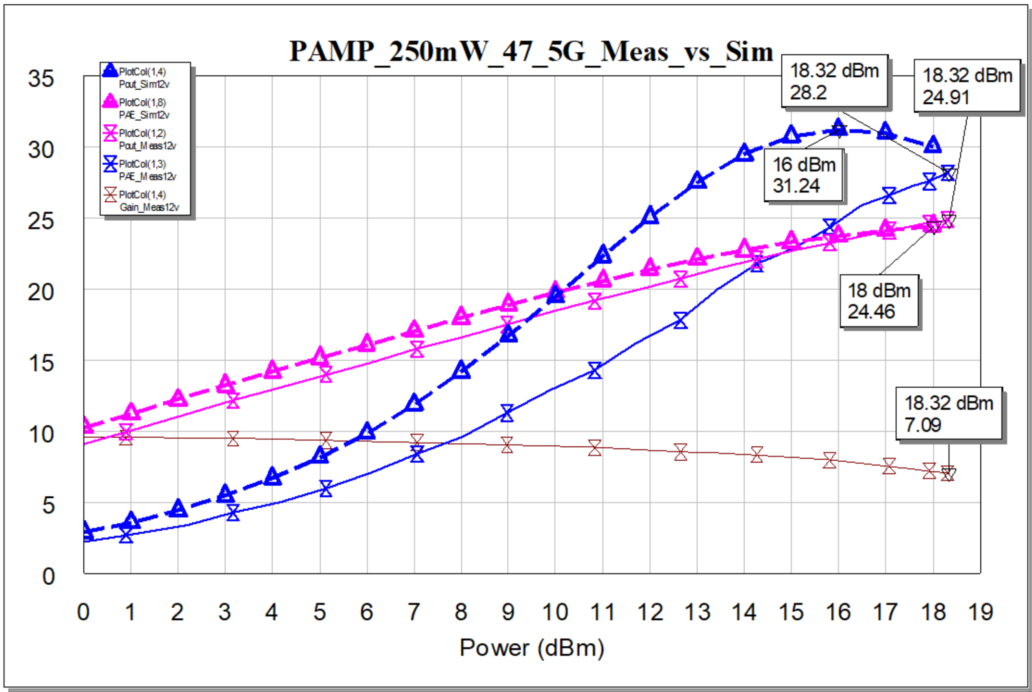

Fig. 6 Power performance simulation vs. measurement of one-stage 0.25-W PA (47.5 GHz)

4. One-Stage 1/2-W Power Amplifier

The output PA used a 0.5-mm HEMT (8 × 62.5 µm) to achieve nearly 1/2 W of power with nearly 10 dB of small signal gain from 40 GHz to 50 GHz. Both single-stage PAs achieved 1 W per mm (HEMT periphery) within the band. Figure 7 shows a plot of the single-stage 1/2-W PA (8 × 62.5 µm), which was placed so that the gate and drain DC bias pads were on the bottom edge of the fabricated die. There was variation in performance among a few die tested, but there was good agreement between the test results and the nominal simulations. Figure 8 shows good agreement in small signal s-parameters for two measured PAs (solid) versus the simulations (dotted) at a nominal DC bias of 13 V and 100 mA/mm IDS.

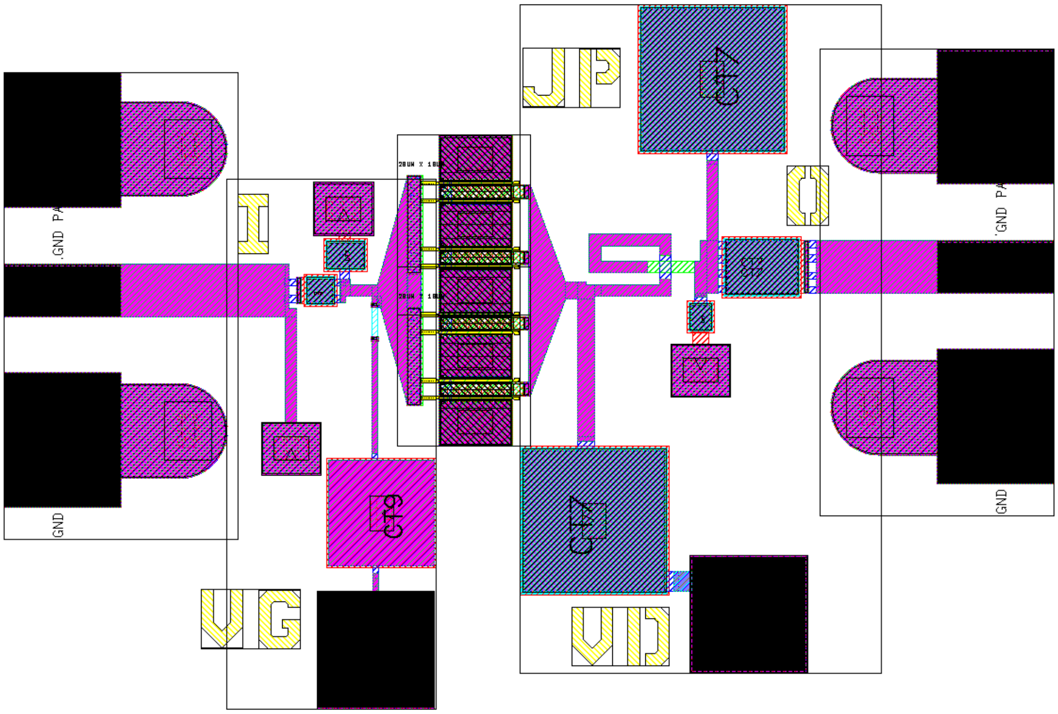

Fig. 7 Plot of one-stage 0.5-W PA (8 × 62.5 μm)

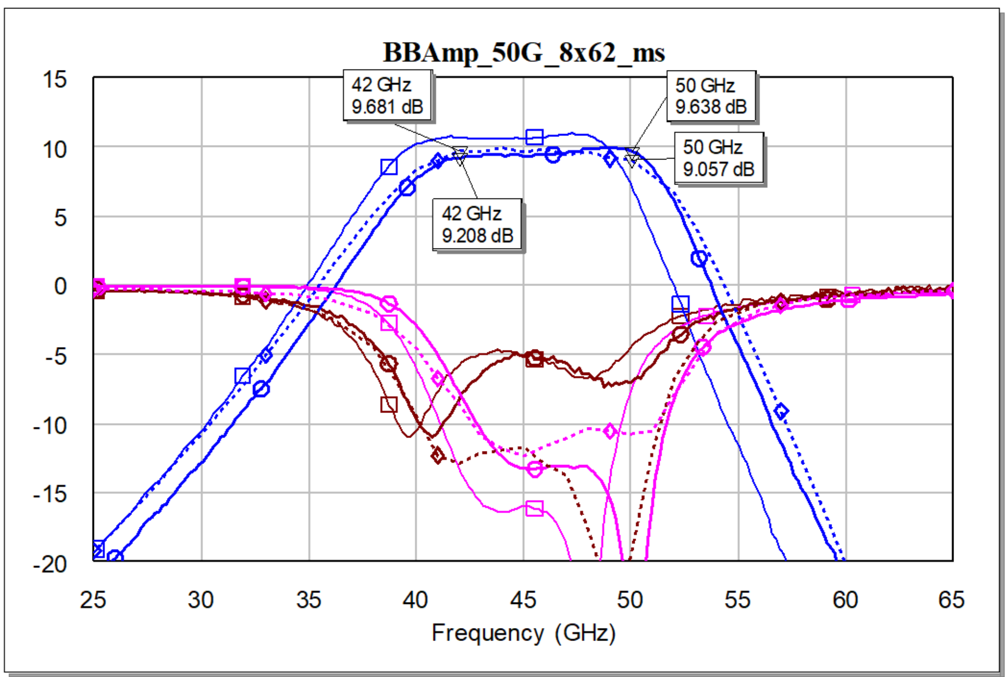

Fig. 8 Simulation and measurement of one-stage 0.5-W PA (8 × 62.5 μm)

Power and efficiency were measured for several die. Large 100-pf and 1000-pf caps had to be wire bonded to the bias pads to quell low-frequency oscillations (near 10 MHz) during the probe testing. As with the prior driver stage PA, measurements at 12-V bias, near the 13-V target bias, resulted in nearly similar output power but slightly better efficiencies than the 13-V measurements. The test setup had insufficient input drive level for the 1/2-W PA testing. Performance results are only shown at 42.5 GHz, but they agree well with simulations, achieving the goal of 1/2 W of output power. Figure 9 shows the PAE (blue) and output power (magenta) comparing simulations (dotted) versus measured (solid) at 42.5 GHz.

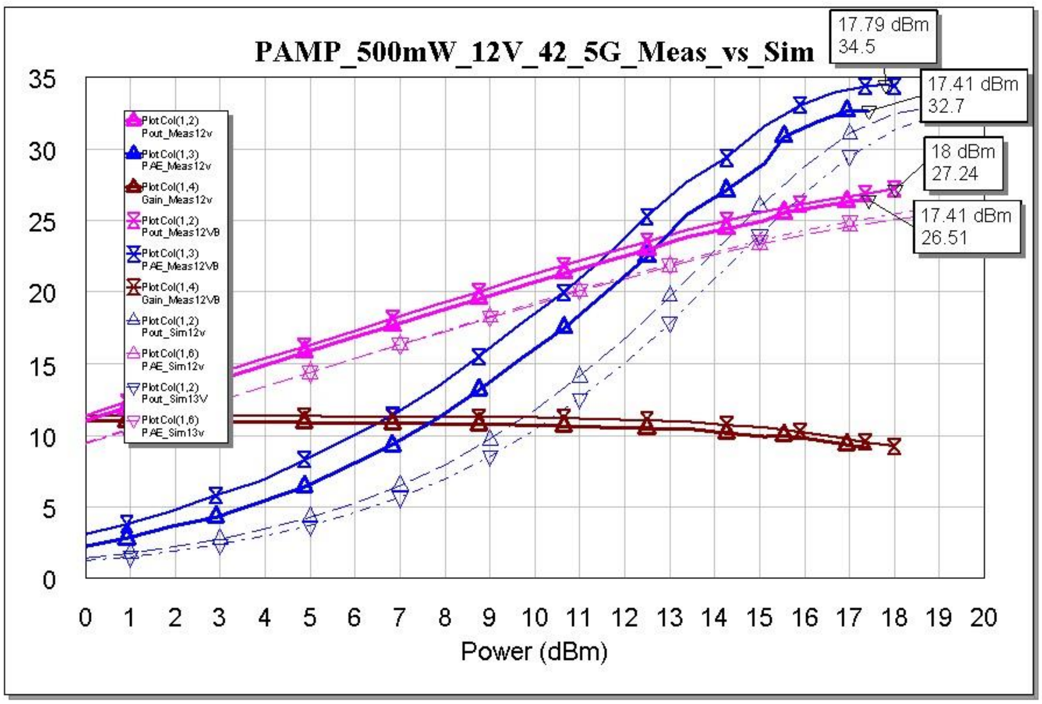

Fig. 9 Power performance simulation vs. measurement of one-stage 0.5-W PA (42.5 GHz)

5. Two-Stage 1-W Power Amplifier

The two-stage PA used Lange Couplers to combine two parallel two-stage 1/2-W amplifiers, each consisting of a 1/4-W first-stage PA driving the second-stage 1/2-W output PA. The interstage match was carefully designed to maximize flat broadband gain with stable 20-dB small signal gain. Figure 10 shows a plot of the two-stage 1-W PA (8 × 62.5 µm), which was placed so that the gate and drain DC bias pads were on both the top and bottom edges of the fabricated die. Gate pads were all connected using large decoupling resistors such that a single DC gate pad (voltage gate) could control all four HEMTs, while the driver and output stage HEMTs have separate DC drain pads (voltage drain). Figure 11 shows the measured s-parameters (solid) versus the simulations (dotted) for the two-stage 1-W PA. Large decoupling capacitors were wire bonded to the PAs to provide low-frequency stability while probe testing.

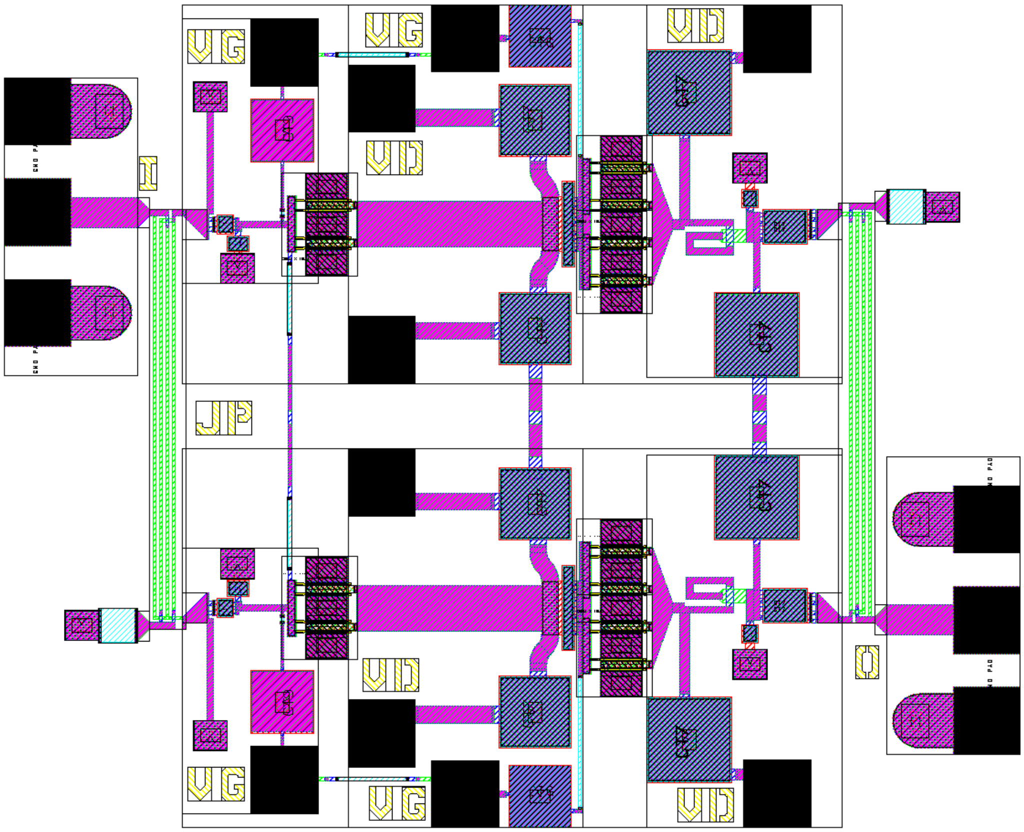

Fig. 10 Plot of two-stage 1-W PA (2X-8 × 62.5 µm)

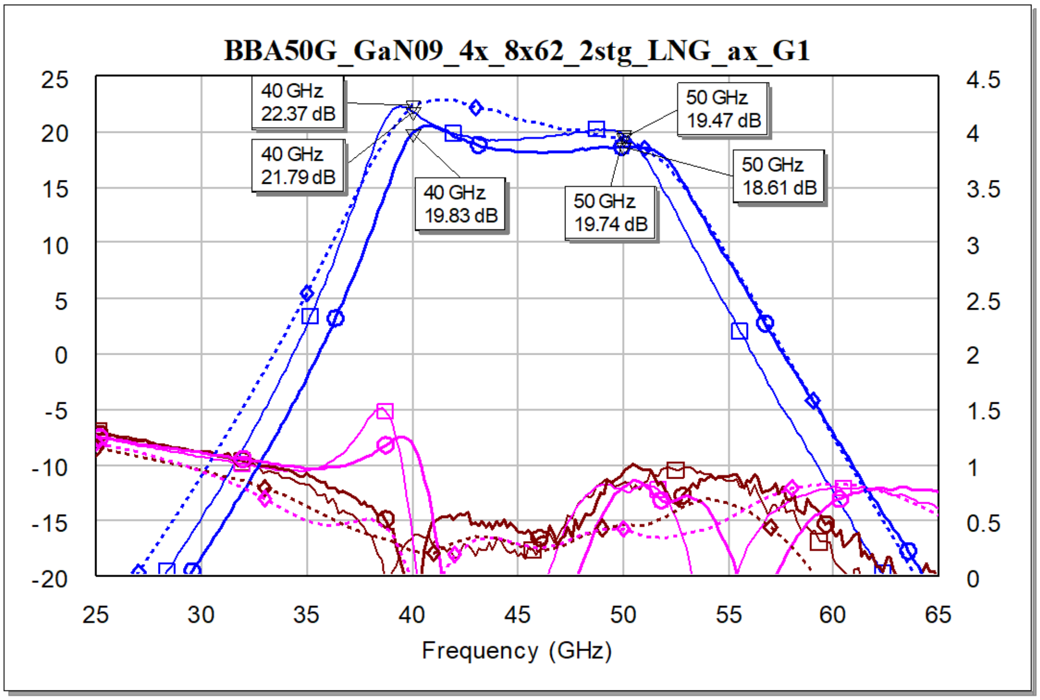

Fig. 11 Simulation and measurement of one-stage 0.5-W PA (8 × 62.5 µm)

Excellent power of 1 W was achieved from 42.5 GHz to 47.5 GHz with a slight power fall-off at the 40-GHz and 50-GHz gain bandwidth edges. Figure 12 shows the PAE (blue) and output power (magenta) simulations (dotted) versus measured (solid) at 42.5 GHz. Similar measured performance versus simulations are shown at 45 GHz and 47.5 GHz in Figs. 13 and 14, respectively.

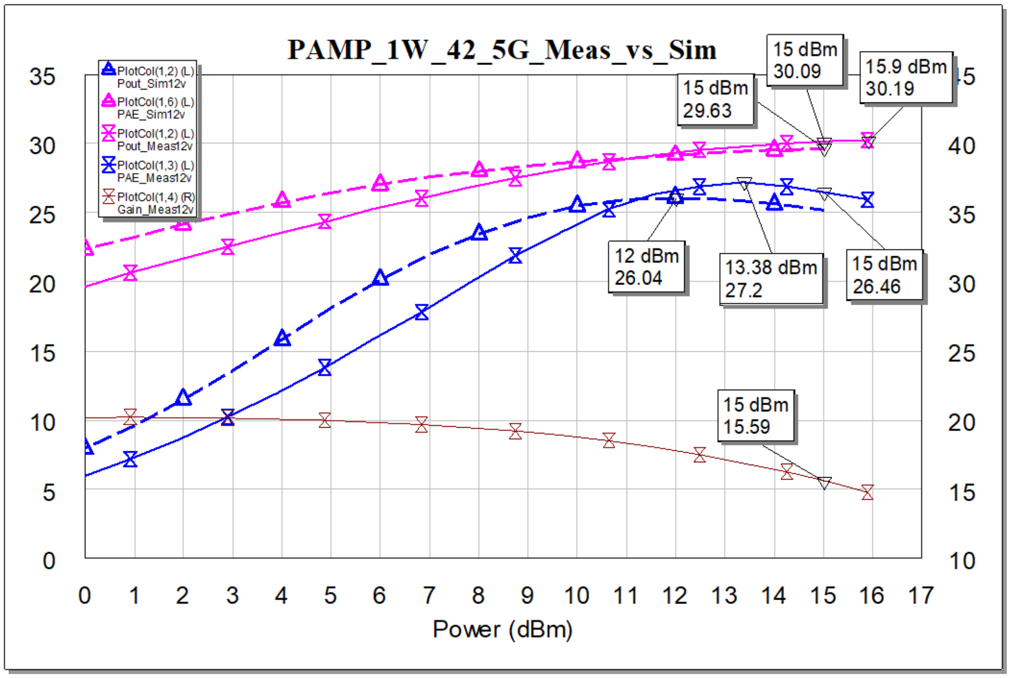

Fig. 12 **Power performance simulation vs. measurement of two-stage 1-W PA (42.5 GHz)**

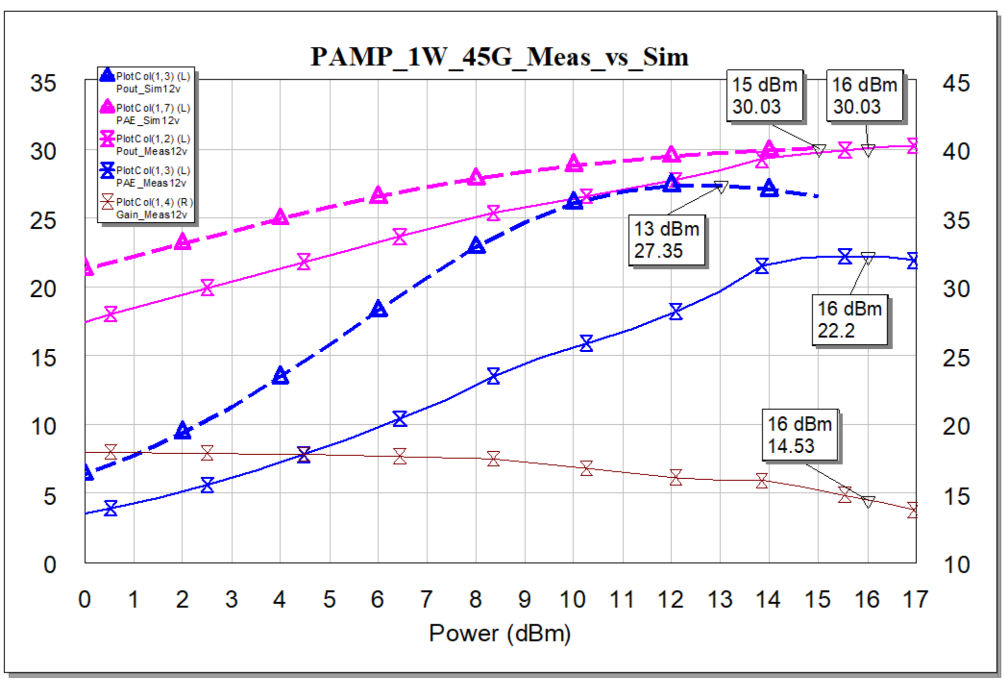

Fig. 13 **Power performance simulation vs. measurement of two-stage 1-W PA (45 GHz)**

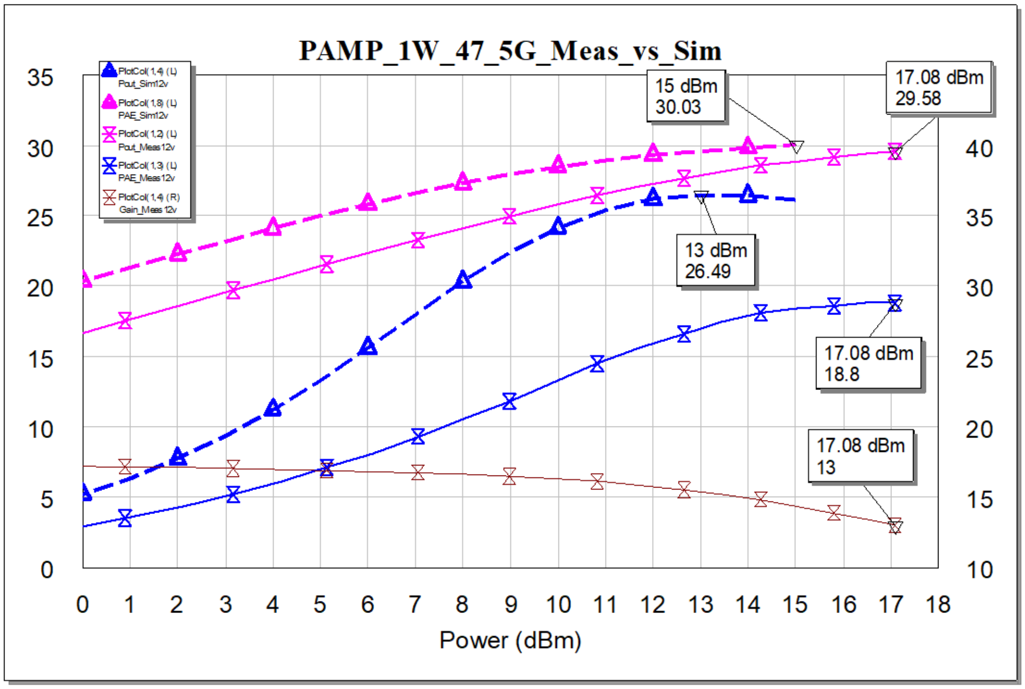

Fig. 14 Power performance simulation vs. measurement of two-stage 1-W PA (47.5 GHz)

6. Three-Stage 1-W Power Amplifier

The one-stage 1/4-W PA was deliberately placed next to the 1-W amplifier so that it could be ribbon bonded and tested as a three-stage PA with nearly 30 dB of small signal gain. The 1/4-W output power was sufficient to drive the two parallel first stages of the 1-W two-stage design. Figure 15 shows a photo of the one-stage 1/4-W PA ribbon bonded to drive the two-stage 1-W PA (8 × 62.5 µm). Figure 16 shows measured small signal s-parameters of the three-stage configuration versus simulation. A new layout with the 1/4-W driver stage combined with the two-stage 1-W PA could be made narrower, likely 2.0 mm × 1.35 mm. Measured power performance yielded more than 1 W from 42.5 GHz to 47.5 GHz. Figure 17 shows measured versus simulated performance at 42.5 GHz showing a measured peak PAE of 29% and more than 1 W of output power at an input drive of 1 dBm or more. At 45 GHz, PAE is slightly lower at 26% with greater than 1 W of output power for an input drive of 3.5 dBm or more. Measured versus simulated performance at 45 GHz is shown in Fig. 18. Power and efficiency dropped slightly at 47.5 GHz but was above 1 W with an input power of 7.5 dBm or more, yielding a peak PAE of 22%. Figure 19 shows measured power performance versus simulations at 47.5 GHz.

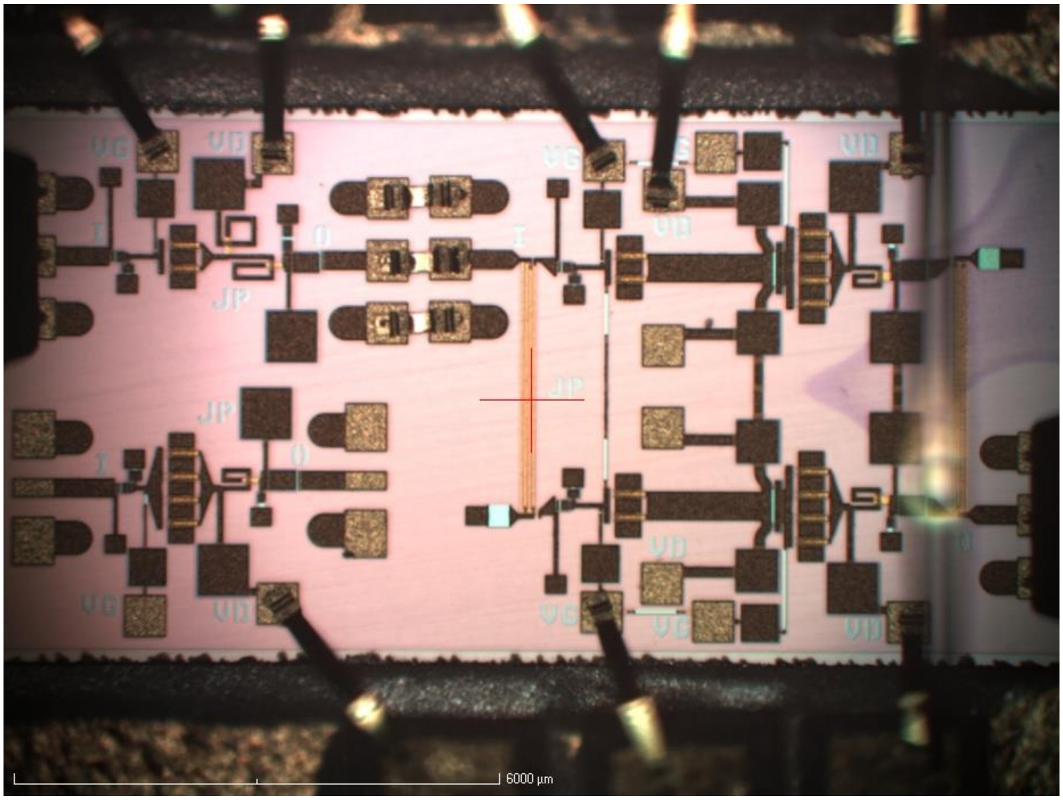

Fig. 15 Photo of die to test "three-stage 1-W PA" (~2.5 mm × 1.35 mm)

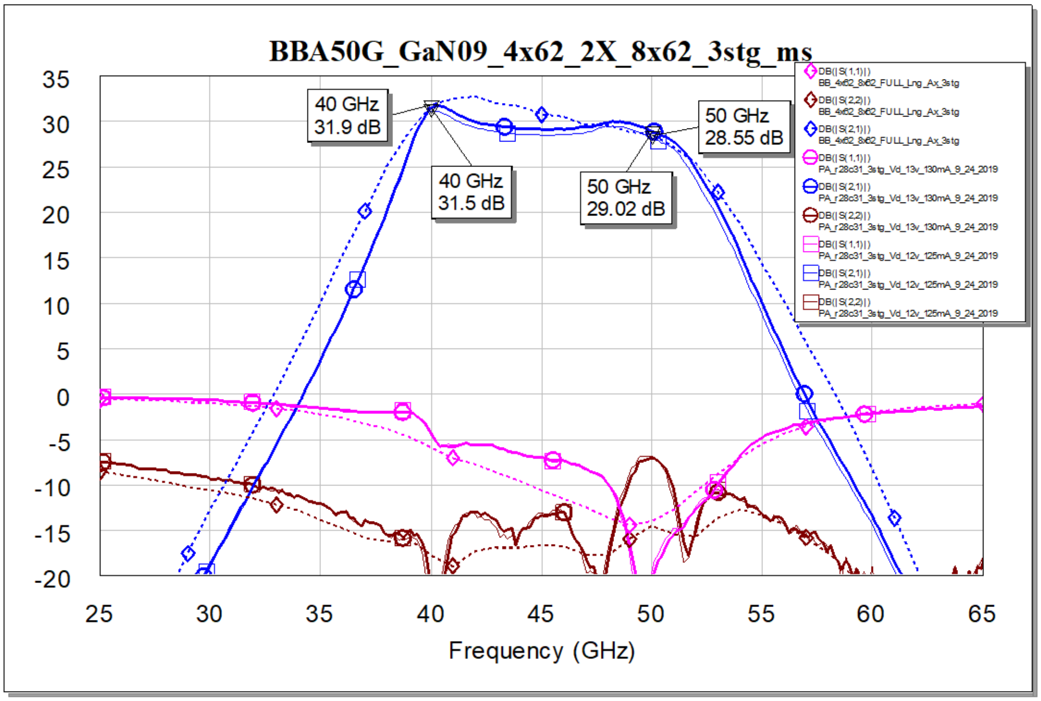

Fig. 16 Simulation and measurement of three-stage 1-W PA (2X 8 × 62.5 µm)

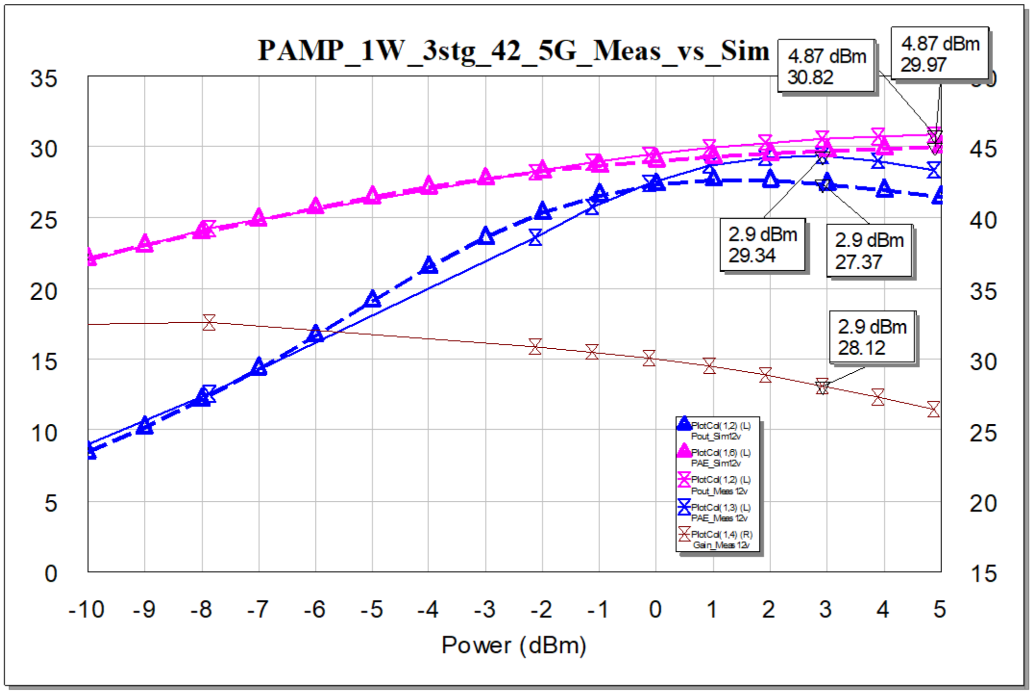

Fig. 17 **Power performance simulation vs. measurement of three-stage 1-W PA (42.5 GHz)**

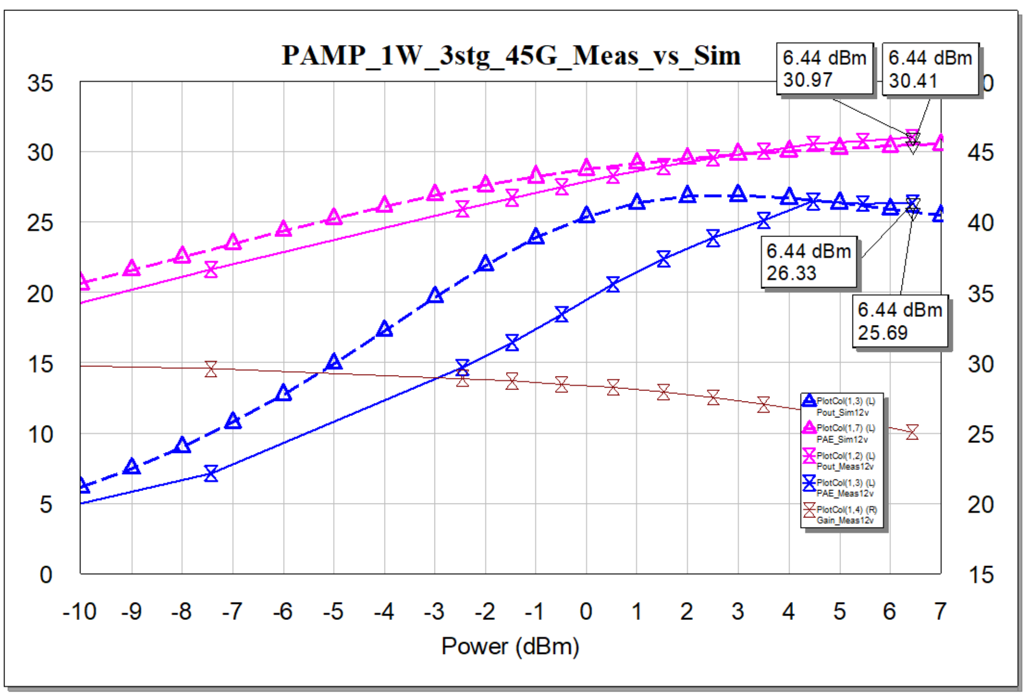

Fig. 18 **Power performance simulation vs. measurement of three-stage 1-W PA (45 GHz)**

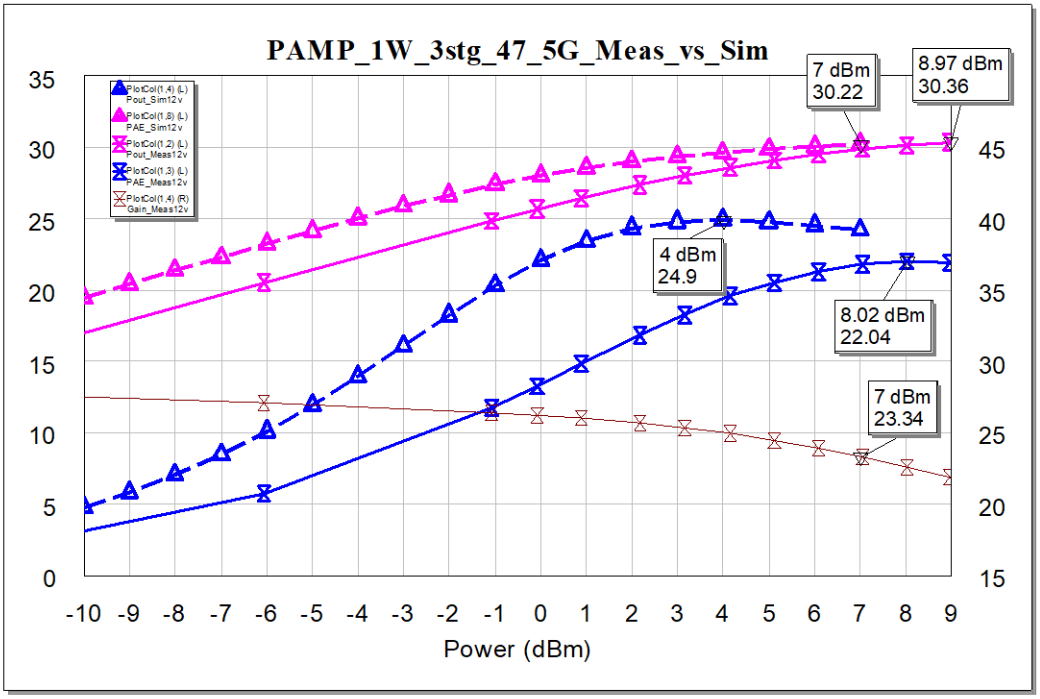

Fig. 19 **Power performance simulation vs. measurement of three-stage 1-W PA (47.5 GHz)**

7. Packaged Three-Stage 1-W Power Amplifier

The three stage 1W PA was packaged in a connectorized assembly (see Fig. 20). As noted, the one-stage 1/4-W PA was ribbon bonded to the two-stage 1-W amplifier to provide nearly 28 dB of small signal gain. Figure 21 shows measured small signal s-parameters of the three-stage PA probed die versus the approximately 2 dB lower small signal gain of the packaged amplifier. Even short wire bonds between the 50 ohm thin film microstrip lines and the diced amplifier die can have a significant impact on power and performance for these high frequencies, 40 to 50 GHz. A similar size package with a 50 ohm through microstrip connection to 2.4-mm connectors results in 1.1 to 1.3 dB of loss at these frequencies. Assuming half of this loss on each side of the mounted die, the packaging results in approximately a 15% loss in output power and efficiency compared to the previous probed die measurements. Measured packaged power performance yielded about 1 W from 42 GHz to 47.5 GHz. Figure 22 shows measured performance at 42 GHz showing a measured peak PAE of 26% and more than 1 W of output power at an input drive of 7 dBm. At 45 GHz, PAE is 27% with greater than 1.2 W of output power for an input drive of 6 dBm (Fig. 23). Power and efficiency dropped slightly at 47.5 GHz but was 0.92 W with an input power of 8 dBm, yielding a peak PAE of 21% (Fig. 24).

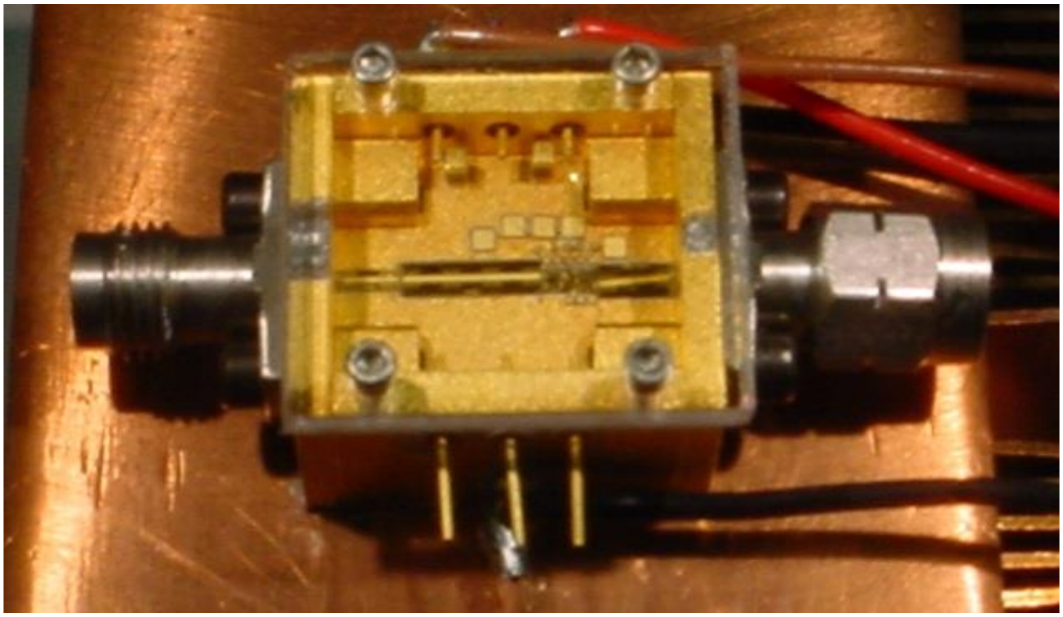

Fig. 20 Photo of packaged "three-stage 1-W PA"

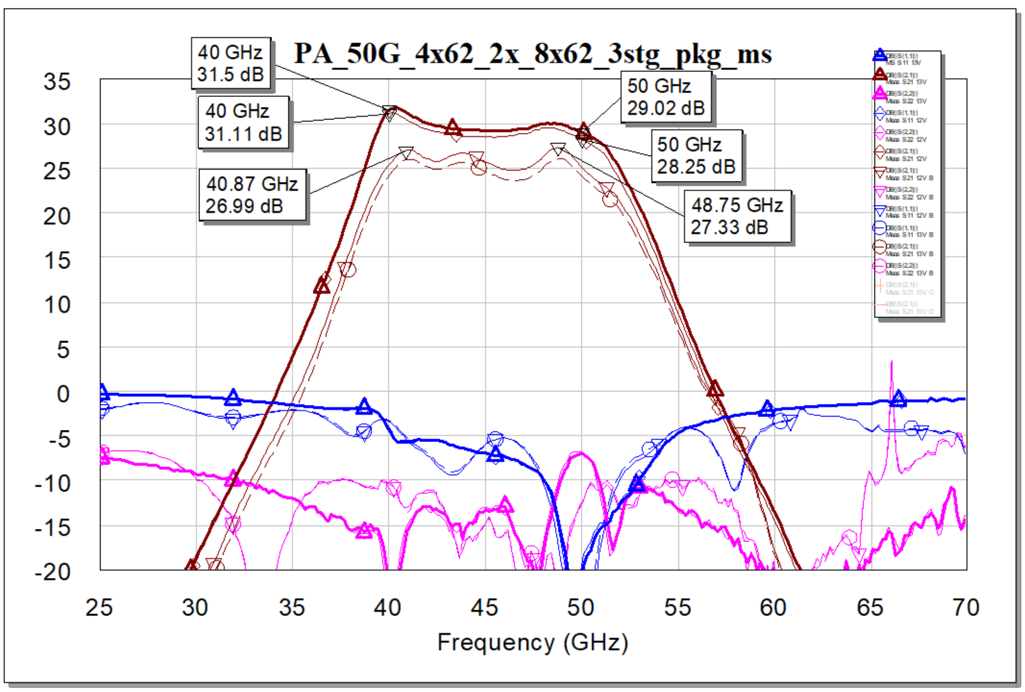

Fig. 21 Measurement of package vs. die for three-stage 1-W PA

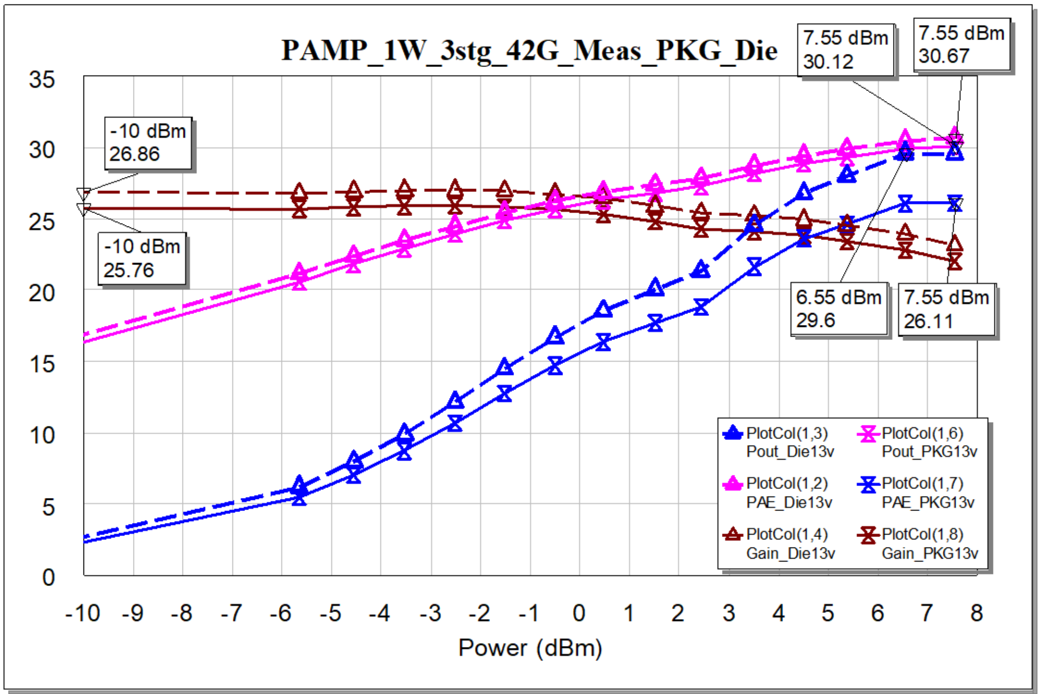

Fig. 22 Power performance at 42 GHz of packaged (solid) three-stage 1-W PA vs. die (dash)

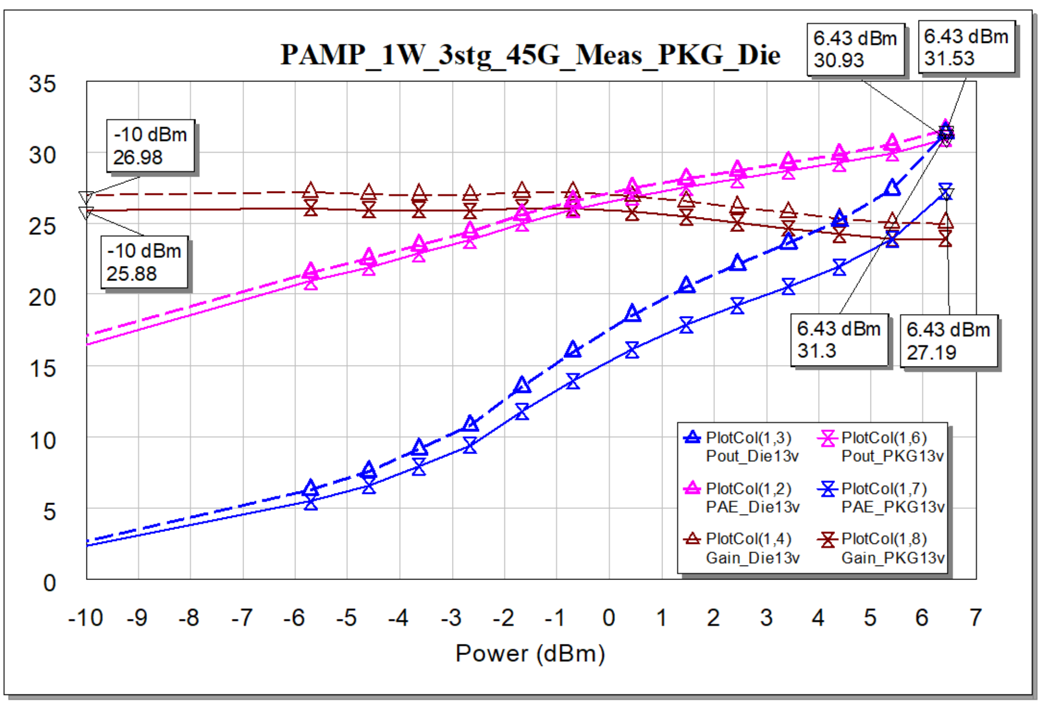

Fig. 23 Power performance at 45 GHz of packaged (solid) three-stage 1-W PA vs. die (dash)

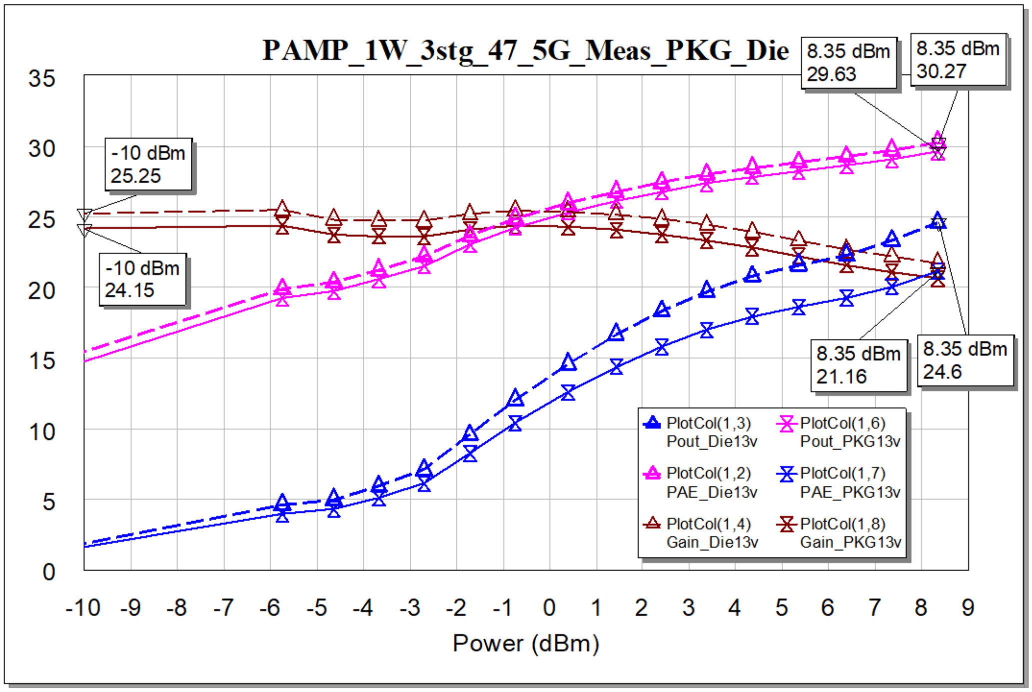

Fig. 24 Power performance at 47.5 GHz of packaged (solid) three-stage 1-W PA vs. die (dash)

8. Distributed Amplifier Testing

The two DAs were probe tested with external bias tees for gate and drain at the RF input and output. There is a lot of gain bandwidth in these two designs yielding very high gain at low frequency, with simulations showing gain increasing below 2 GHz up to about 25-dB gain at very low frequency. In initial testing, the DC bias was slowly increased until the amplifiers just started to exhibit gain. Both DAs appeared to go into self-destructive oscillations when the bias currents neared the nominal 100 mA/mm DC bias. An external large resistor to limit instantaneous current spikes from the power supplies enabled “safe” testing of the two DAs, while they were driven with a signal generator from 2 to 50 GHz. Just as the amplifiers exhibited gain at around 50 mA/mm, both DA designs would exhibit an oscillation. A spectrum analyzer showed the input signal as well as a secondary oscillation, which appeared to vary from about 3 to 6 GHz. The oscillation varied with DC bias as well as with the input power level of the input signal. Gain of the desired signal was much less than the expected 10-dB gain, possibly only a few decibels, whenever this oscillation occurred. While these two amplifiers have very large gain bandwidth, simulations did not predict this particular instability. Another possibility could be that the oscillation is higher than the 50-GHz upper limit of the spectrum analyzer and is folding back into the spectrum, appearing to be 3–6 GHz.

If there are discrete HEMTs available, of a similar 2 × 40-µm size, from other die on this wafer fabrication, measurements of those HEMTs may give insight into the current discrepancies between simulations and measurements of these two DA designs.

Using the large resistor to prevent destructive burnout, additional s-parameter measurements were performed on the two DAs. A small amount of broadband gain was achieved, up to 5 dB at 60 GHz, but the gain and DC bias were lower than desired. A re-simulation of the DA at a much lower current but similar low-drain voltages resulted in a similar gain curve. Input and output return loss measurements match the simulations over quite a bias range. Still, it does not make sense why the nonlinear model appears to match measured gain performance at such a low DC current. The desired bias is 13 V at 40 mA (IDS), but the measurements shown are between 4.6 V at 50 mA (IDS) to 6.6 V at 68 mA (IDS). Figure 25 shows the measured s-parameters of the DA (solid) versus a simulation at 3 V and 6 mA (dotted). Measured s-parameters of the nonuniform DA at similar low DC biases but without comparison to a simulation are shown in Fig. 26. At this point the two DAs have achieved partial success in testing, and the instability is unusual. A similar design of a previous DA design using Qorvo's 0.25-µm GaN process yielded good gain to 25 GHz,[2] but that DA had considerably less gain bandwidth than what is expected from this 0.09-µm GaN process.

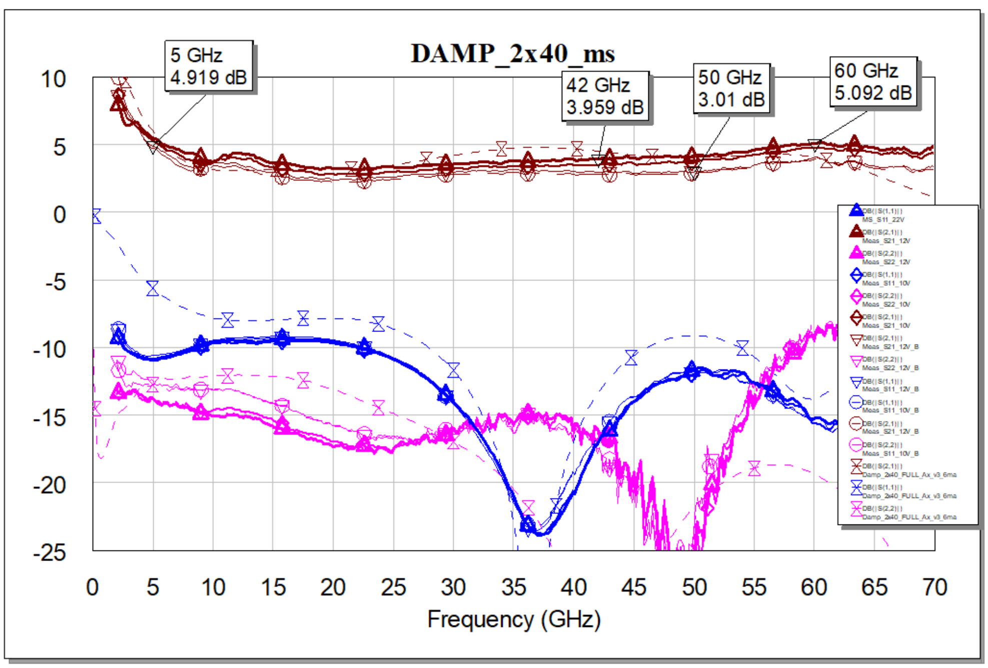

Fig. 25 S-parameter simulation (3 V, 6 mA [dash]) vs. measurements of DA (4.6 to 6.6 V [solid])

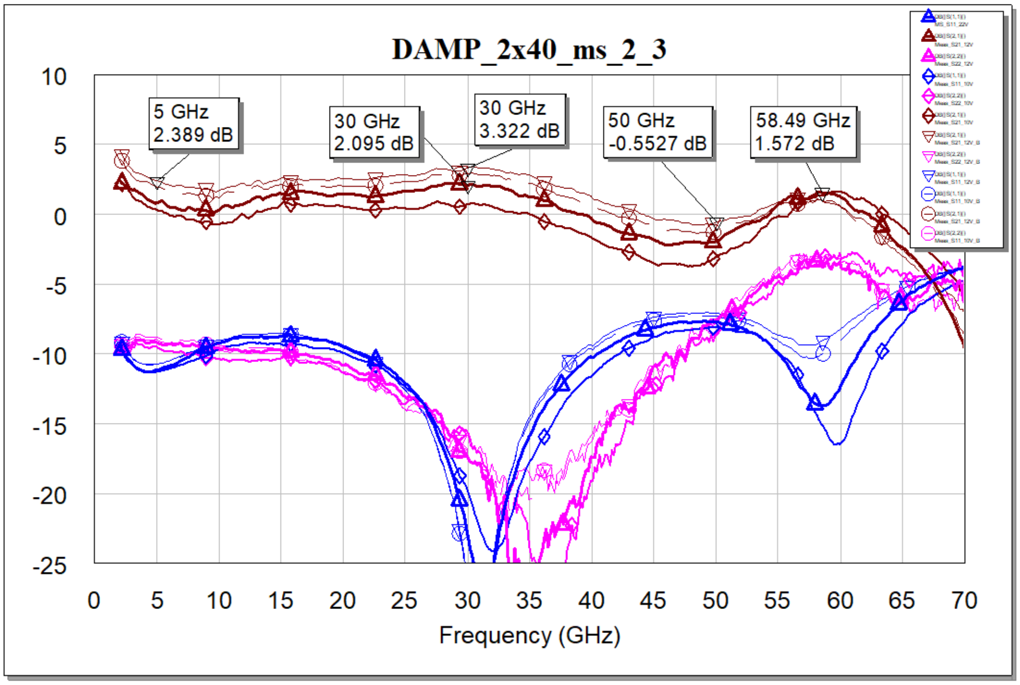

Fig. 26 S-parameter measurements of nonuniform DA (5 V, 50 to 80 mA)

9. Concluding Remarks

Various topologies for a V-band PA were evaluated using a high-frequency 90-nm GaN process from Qorvo. Three PAs were fabricated and successfully tested. A single-stage 1/4-W (0.25-mm) driver amplifier was tested along with a single-stage 1/2-W (0.5-mm) output stage. These individual amplifiers were the basis for a two-stage 1-W 40- to 50-GHz PA. For the two-stage design, very small compact Lange Couplers provided excellent input and output return loss with minimal loss in the two-way combiner to achieve nearly 1 W of output power. As a test of a three-stage amplifier, the one-stage 1/4-W driver amplifier was placed on the die such that it was wire bonded to the two-stage PA and tested as a three-stage amplifier, demonstrating flat 30-dB small signal gain across 10 GHz of bandwidth, 40 to 50 GHz, with better than 1 W of output power across most of the band with a slight reduction at the band edges. The two DAs designed have had only partial success in testing, possibly due to an unusual stability problem. Prior DAs with a similar topology have been successful, including a recent 0.25-µm Qorvo GaN design. Future designs could be resubmitted for fabrication in this recently developed 90-nm high-performance GaN process, either to improve on these current designs or to produce other circuits of interest.

10. References

1. Penn J. High-performance 90-nm gallium nitride (GaN) communications circuits. Aberdeen Proving Ground (MD): Army Research Laboratory (US); 2018 Aug. Report No.: ARL-TR-8445.

2. Penn J. Testing of 0.25-μm gallium nitride (GaN) monolithic microwave integrated circuit (MMIC) designs. Aberdeen Proving Ground (MD): Army Research Laboratory (US); 2018 Nov. Report No.: ARL-TR-8565.

List of Symbols, Abbreviations, and Acronyms

AFRL	Air Force Research Laboratory
ARL	Army Research Laboratory
CCDC	US Army Combat Capabilities Development Command
DA	distributed amplifier
DC	direct current
EW	electronic warfare
GaN	gallium nitride
HEMT	high-electron-mobility transistor
IDS	drain-source current
PA	power amplifier
PAE	power added efficiency
RF	radio frequency

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