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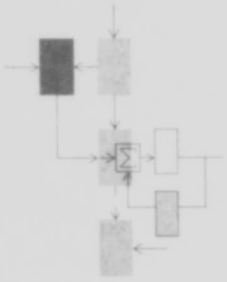

A HIGH-POWER SEMICONDUCTOR-MAGNETIC PULSE-GENERATOR CIRCUIT

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by
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Air Force Avionics Laboratory
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Radar Research Group
Electronic Systems Laboratory
Department of Electrical Engineering
Cambridge, Massachusetts 02139

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ERRATA SHEET

Location	Reads	Should Read
3-13, Fig. 3.5 caption	...R-F-Tube	...R-F-Tube Load
3-28, lines 4 and 5	...n... (3 places)	...$1/n_1$... (3 places)
3-30, Eq. 3.55b	$I_{Bp} = \frac{\pi}{n_1 T_o} \frac{\cos\theta}{1+\sin\theta} = \frac{I_{Ap}}{n_1} \cos\theta$	$I_{Bp} = \frac{\pi}{n_1 T_o} \frac{\cos\theta}{1+\sin\theta} Q_o = \frac{I_{Ap}}{n_1} \cos\theta$
3-32, 2nd line from bottom	...n...	...n_1...
3-33, Eq. 3.59 and preceding one	(ΔE_{C1} small) is a condition on these equations, not a term in the equations	
3-35, Eq. 3.61	$-G_n = \frac{dI_o}{dE_o} = -\frac{J_c}{E_o^2 T_r} = \frac{I_o}{E_o}$	$-G_n = \frac{dI_o}{dE_o} = -\frac{J_c}{E_o^2 T_r} = -\frac{I_o}{E_o}$
3-39, 1st line after Eq. 3.70	...by Eq. 3.70,...	...by Eq. 3.69,...
3-39, line before Eq. 3.71	...Eq.. 3.69...	...Eq. 3.67...
3-37, 2nd line after Eq. 3.65	...$\beta^2 \geq 1$,...	...$\beta^2 \leq 1$,...
4-19, line 4	...with...	...for...
4-22, line 6, paragraph 2	...unit...	...reset...
4-23, line 6, paragraph 4	...junction...	...stud...
4-27, Eq. 4.36	$n_g \ell A_{eff} = 2 \frac{\mu_o}{B_g^2} J_{st}$	$n_g \ell_g A_{eff} = 2 \frac{\mu_o}{B_g^2} J_{st}$
5-15, Fig. 5.10	Zero level is second horizontal line down from top.	
5-15, Fig. 5.11	Zero level is first line up from bottom.	
5-17, Table 5.1, units for A_3	...cu m	...sq m

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ERRATA SHEET

Location	Reads	Should Read
vi	5. Controlled Rectifiers S_{1a}, S_{1b} and S_{1c}	5. Controlled Rectifiers S_{3a}, S_{3b} and S_{3c}
2- 7, middle of page	...the switching operation, and traversal of the saturated region.	...the switching operation.
2- 7, 3rd line from bottom	...thickness, switching waveform, and (possibly) degree of saturation.	...thickness and switching waveform.
2- 8, last line	varries	varies
2- 8, footnote	...Hypernik V. Orthonik,...	...Hypernik V, Orthonik,...
2-12, line 3, Pt. 5	...affects...	...effects...
2-12, line 2, last paragraph	...cross section, and ρ...	...cross section in one turn and ρ...
2-13, first word	Therefore,	therefore,
2-13, Eq. 2.25b	$J_w = N^2 \rho \frac{\ell_w}{a} \int T_r i^2 dt$	$J_w = N^2 \rho \frac{\ell_w}{a} \int_{T_r} i^2 dt$
2-15, 3rd line from bottom, middle paragraph	...μ...	...η...
2-15, 3rd line from bottom	...less...	...more...
2-21, line 13, paragraph 2	...resulting from the diffusion of minority carries...	...results from the diffusion of minority carriers...
2-21, line 3, paragraph 3	...controller...	...controlled...
2-29, line 3, last paragraph	...manufactures...	...manufacturers...
3- 6, Eq. 3.4	$I_p \tau_p = \int_0^{\tau} i_L dt = C_2 E_{E2}$	$I_p \tau_p = \int_0^{\tau} i_L dt = C_2 E_{C2}$

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ERRATA SHEET

Location	Reads	Should Read
5-22, heading 5	5. Controlled Rectifiers S_{1a}, S_{1b}, and S_{1c}.	5. Controlled Rectifiers S_{3a}, S_{3b}, and S_{3c}.
5-24, line 4	...Th,...	...T_h,...
5-24, Temperature-rise table	...Energy-regulator	...Regulator-inductor
A-11, 4th line from bottom	...B'D' transformer, reset...	...B'D' transformer reset...

ABSTRACT

A circuit for generating high-power, high-voltage pulse trains is described that uses silicon controlled rectifiers for high-current, low-voltage power switching, and inductors and transformers having saturable-magnetic cores for high-voltage, high-speed switching. Figures of merit for saturable-inductor switches and a measure of power-switching capacity for controlled rectifiers are determined which provide a characterization of these devices that is especially useful for design purposes. A step-by-step circuit-design procedure is presented that is flexible enough so that selected performance attributes (such as smallest size and weight, or highest efficiency) can be emphasized by the designer. A laboratory breadboard semiconductor-magnetic pulse generator producing 1700 average watts in 1.6-microsecond pulses of over 1 megawatt peak power is described as an illustration of the circuit technique.

ACKNOWLEDGEMENT

This report is the result of an investigation involving the contributions of many individuals and extending over a period of several years. Among these contributions, special mention should be made of the work of Rolando Jordan ("Semiconductor-Magnetic Pulse Generators," by Rolando Luis Jordan, Master of Science Thesis, Department of Electrical Engineering, M.I.T.; June, 1962). The authors wish to thank Prof. J.F. Reintjes, Director of the Electronic Systems Laboratory, for his continuous and enthusiastic support of the program, and for his assistance in the preparation of Chapter V of this report.

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CHAPTER I

INTRODUCTION

Most high-power pulse-generator circuits in current use are of one of two kinds. In one a high-voltage hydrogen thyratron discharges a pulse-forming network into the load. In the other, pulses formed at low power level are delivered through a high-power vacuum-tube amplifier to the load.

Magnetic materials that saturate sharply offer the possibility of a third kind of pulse generator. In these a coil, wound on a saturable magnetic core, functions as a switch - - the switch is open if the core material is unsaturated, and closed if the core is saturated. Generation of brief pulses with saturable magnetic devices was accomplished at least thirty years ago.[1] During and since World War II, a few radar modulators have employed high-power magnetic switches.[2] Nevertheless, magnetic pulse generators have not been widely used, probably because, until recently, those not containing vacuum tubes have suffered serious deficiencies: low efficiency, excessive weight, output-pulse jitter, and a repetition frequency equal to the input-power frequency.

Saturable-inductor switches have important advantages over vacuum tubes and gas tubes with respect to mechanical ruggedness and life expectancy. They may also possess a higher upper limit of power-handling capacity. For these reasons, an effort has been made in the M.I.T. Electronic Systems Laboratory to develop pulse-generator circuits in which the deficiencies of all-magnetic pulse generators are overcome by combining saturable inductors with other solid-state

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1. Kiltie, O., "Transformer with Peaked Waves", Electrical Engineering, 51 (1932), pp. 802-804.

2. Peterson, E., "Coil Pulser for Radar," B.S.T.J., 25 (1946). p. 603; Melville, W.S., "The Use of Saturable Reactors as Discharge Devices for Pulse Generators", Proc. I.E.E., pt. III, 98 (Feb. 1951), pp. 185-207; Smith, E.J., Antin, J., and Lian, K.T., "Magnetic Modulators for Radar Applications", (Reports R-419-55, PIB-55, PIB-35, M.R.I., Polytechnic Institute of Brooklyn, April 1955)

devices of comparable ruggedness and life expectancy.

The first result of the effort, in 1957, was a 40-watt (average power) pulse generator in which a power transistor generated pulses of 300 - μs duration and saturable inductors compressed these pulses to achieve 24-kw, 1 - μs output pulses.[1] In 1958 a silicon controlled rectifier was substituted for the transistor; it produced 50-μs pulses which were compressed to 40-kw, 1.5-μs pulses (average power, 300 watts).[2] Since 1958, this controlled-rectifier-and-saturable-inductor circuit has been refined, an input-voltage regulator circuit has been added, a design procedure has been developed, and several models of the circuit operating at various average-power levels up to 2 kw have been constructed.[3]

Detailed performance data for one of these pulse generators are given in Chapter V. These data indicate that semiconductor-magnetic pulse generators offer advantages relative to their vacuum-tube and gas-tube counterparts not only in ruggedness and reliability, but also in size, and weight, and possibly in efficiency. Pulse jitter is not a problem, pulse shapes are those characteristic of line-pulsing modulators, and intervals between pulses are determined by input trigger pulses. Elimination of the deficiencies of all-magnetic circuits appears, indeed, to be complete.

Introduction of controlled rectifiers into the circuit suggests the possibility of eliminating the saturable inductors and using controlled rectifiers in the same way as hydrogen thyratrons. If long pulses are desired--in the millisecond range--such a circuit is practical.

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1. Krinitz, A., "A Transistor-Magnetic Pulse Generator for Radar Modulator Applications", (Report 7848-R-1, Servo. Lab., M.I.T., Sept. 1958). DDC No. AD 210 247.

2. Lassiter, E.M., "High-Power Pulse Generation Using Semiconductors and Magnetic Cores", (Tech. Memo. 7848-TM-2, Servo. Lab., M.I.T., Jan. 1959) DDC No. AD 213 521.

3. Cornew, R.W., "Solid-State High-Power Pulse Generators", (Tech. Memo. ESL-TM-134, Electronic Systems Lab., M.I.T., September 1961); Jordan, R.L., Price, C., and Swain, L.R., "Two Experimental Semiconductor-Magnetic Pulse Modulators", (Tech. Memo. ESL-TM-139, Electronic Systems Lab., M.I.T., May 1962), DDC No. 276 502; the latter paper is also published in Proceedings of the Seventh Symposium on Hydrogen, Thyratrons, and Modulators, May 1, 1962; pp. 240-259, DDC No. AD 296 002.

Shorter output pulses, however, require an increased ratio of controlled-rectifier power rating to average output power, and for pulse durations in the microsecond range, the controlled-rectifier utilization factor becomes impracticably low except in circuits requiring very little average power. In the semiconductor-magnetic pulse generator, saturable inductors increase the utilization factor both by delaying current build-up in the controlled rectifier (see Chapter II, Section B) and by pulse compression.

A. THE MAGNETIC PULSE GENERATOR

As a prelude to discussion of the semiconductor-magnetic pulse generator, the principle of pulse compression in an all-magnetic pulse generator is presented (1) to show why the all-magnetic circuit is undesirable, and (2) to prepare for the use of the pulse-compression principle in the semiconductor-magnetic circuit.

In Fig. 1.1, e is the voltage of an a-c power supply and L_0 is a linear inductor adjusted to resonate with C_1 at the frequency of e. The waveforms of e and e_{C1} in Fig. 1.2 are substantially those of conventional a-c resonance charging[1] because L_1 is in its nonconducting state except in the discharge interval T_1. During the discharge interval, L_1 is saturated and allows current to transfer charge from C_1 to C_2. Because L_2 is at this time nonconducting and C_2 is equal to C_1 in value, all the energy stored in C_1 (except for losses) is transferred to C_2. By proper design of L_1, T_1 can be made much less than T_0, the charging time for C_1. A similar process transfers the energy from C_2 to C_3, and from C_3 to the load. Each successive energy transfer occurs in a shorter time; the pulse is compressed as it travels from input to output of the generator. Current in the bias windings serves to reset the inductors to negative saturation in the period between energy transfers.

The disadvantages of this technique of high-power pulse generation are fairly obvious. If the duty ratio of the output pulse is low, a large volume of magnetic material is required to provide the

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1. Reintjes, J. F. and Coate, G. T., Principles of Radar, McGraw-Hill Book Company, Inc., New York, 3rd ed., (1952), pp. 174-176.

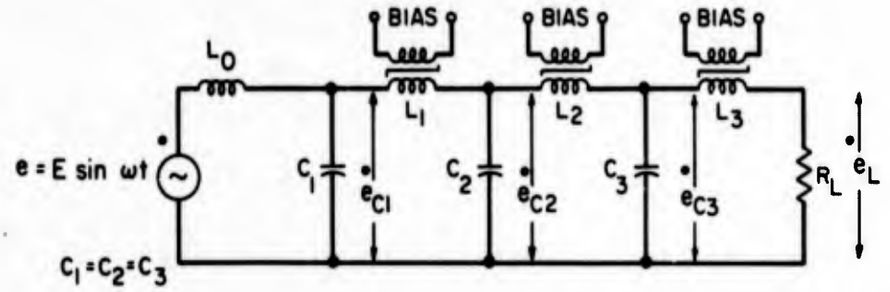

Fig. 1.1 All-Magnetic Pulse Generator

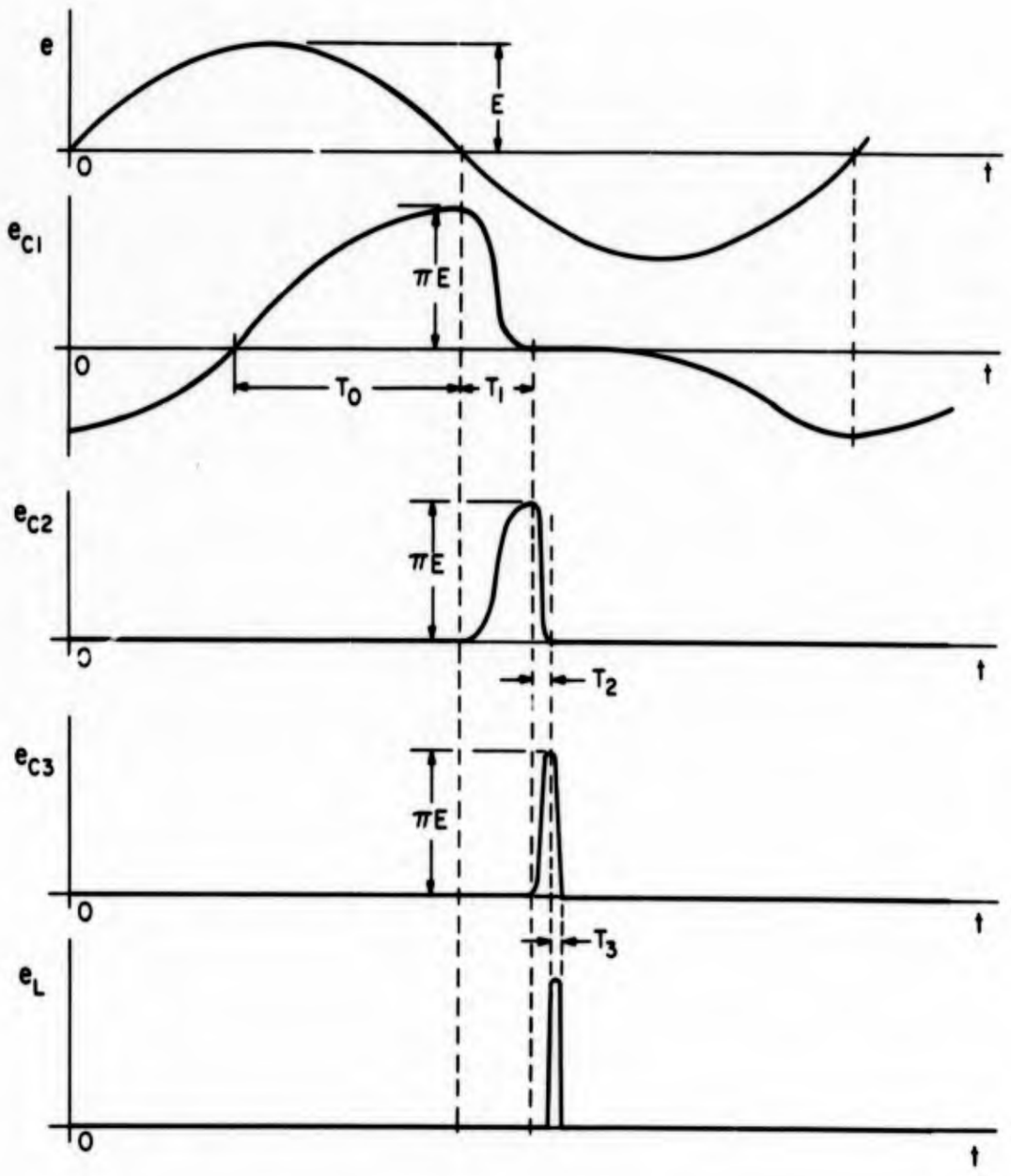

Fig. 1.2 Waveforms for Circuit of Fig. 1.1

attendent large amount of pulse compression, and this large core volume leads to large core losses. Furthermore, the capacitor volume is high because each compression stage requires a separate capacitor capable of storing the full pulse energy. The delay of the output pulses (the sum of the times required to saturate the several inductors) is long and is sensitive to input-voltage changes. Therefore, a very precisely regulated a-c supply is required to keep jitter of the output pulse to an acceptably low value. The repetition frequency is necessarily the same as the power-supply frequency.

B. THE SEMICONDUCTOR-MAGNETIC PULSE GENERATOR

The basic circuit for the semiconductor-magnetic pulse generator considered in this report is shown in Fig. 1.3. This circuit

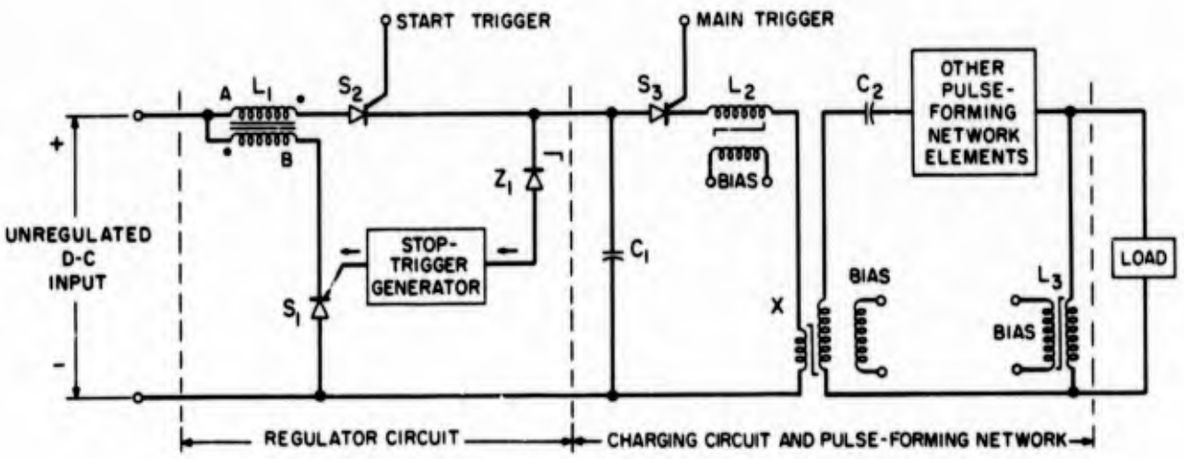

Fig. 1.3 Basic Circuit of the Semiconductor-Magnetic Pulse Generator

generates output pulses in three steps:

1. Energy is drawn from an unregulated power supply to charge capacitor C_1. The regulator circuit halts the charging of C_1 when a desired voltage is reached and returns to the power supply any energy then stored in inductor L_1.

2. Energy is next transferred from C_1 through a step-up saturable transformer to a high-voltage capacitor C_2. This process takes place during a time interval several times as long as the desired output-pulse duration.

3. Energy is then discharged from C_2 through a linear pulse-forming network into the load.

In more detail, operation of the circuit of Fig. 1.3 is as follows. A start trigger pulse turns on controlled rectifier S_2, which allows a current to pass through the linear inductor L_1 to charge C_1. During this period controlled rectifier S_1 is nonconducting. An avalanche reference diode Z_1 senses when a desired voltage greater than the input voltage appears across C_1, and at this instant an output signal from a stop-trigger amplifier causes S_1 to conduct. The turns ratio of the two-winding inductor L_1 is chosen so that when S_1 conducts the voltage across winding A is reduced. Thus the voltage across S_2 reverses, and conduction of S_2 terminates. Capacitor C_1 remains charged to the desired voltage, and energy stored in L_1 is returned to the power supply through current flow in winding B.

The pulse-compression circuit in Fig. 1.3 differs somewhat from that of a compression stage in Fig. 1.1; it contains a shunt inductor (transformer X) and series capacitor (C_2), rather than the reverse. Capacitor C_2 may be a single, high-voltage capacitor, or may represent the equivalent shunt capacitance of a pulse-forming network. The main trigger pulse turns on S_3 and so transfers charge from C_1 to C_2 through the saturated inductances of L_2 and L_3; other pulse-forming network elements exhibit nearly negligibly low impedance to the relatively slow charging pulse. Transformer X is unsaturated and functions as an ordinary step-up transformer during this process. The transfer of charge is delayed by the time required for saturation of L_2; thus S_3 has time to reach a state of very low forward resistance before the large charge-transfer current flows. When C_2 is completely charged, transformer X saturates and C_2 discharges through the secondary of X, the pulse-forming network, and the load. Little current flows through L_3 because the negative pulse voltage switches L_3 into its unsaturated high-impedance state. The discharge of C_2 is more rapid than the charge; that is, pulse compression occurs.

If the prime power supply is a single-phase or polyphase a-c source, an unregulated rectifier-filter circuit utilizing semiconductor

diodes can provide the d-c input power indicated in Fig. 1.3. The combination of such a rectifier with the regulator in Fig. 1.3 is far superior, as a means of charging C_1, to a conventional regulated d-c power supply. Substantially complete elimination of input-voltage fluctuations is necessary to prevent output-pulse jitter. Conventional circuits can provide the necessary transient performance only at large cost in complexity, weight, and inefficiency. The regulator in Fig. 1.3, on the other hand, is very efficient and (because it takes advantage of the nature of its load and in each cycle stabilizes only the final voltage to which C_1 is charged) eliminates input-voltage fluctuations substantially without regard to their waveform or rates of change.

If the prime power source is a battery, the regulator circuit in Fig. 1.3 provides an effective means of compensating the decrease of battery voltage during discharge. It has the disadvantage, however, that the choice of the voltage to which C_1 is charged is limited by available battery voltages. This disadvantage may be removed by adding a transformer-and-diode network between S_2 and C_1 in Fig. 1.3; however, an altogether different form of the regulator circuit is probably preferable for battery-source operation.

Many variations of the circuit in Fig. 1.3 are, of course, possible, and some may be desirable in particular applications. For long output pulses, the pulse-compression stage may be omitted and C_1 discharged directly through S_3, L_2, and the pulse-forming network into the load. For very short pulses, more than one compression stage may be desirable. The series-L compression stage of Fig. 1.1 may be substituted for the shunt-L stage in Fig. 1.3. The regulator circuit may be omitted if pulse jitter and pulse-amplitude regulation are not important.

Despite such possibilities, this report is concerned only with pulse generators based on the circuit of Fig. 1.3. This circuit was chosen for development because it seemed to offer special advantages in radar-modulator applications requiring voltage step-up between the controlled rectifier and the output. Use of shunt-L compression permits a single transformer to provide both the voltage increase and the saturable inductor of a pulse-compression stage. The compression

thus obtained is sufficient to provide reasonable controlled-rectifier utilization factors for output-pulse durations of the order of a microsecond.

CHAPTER II

SATURABLE INDUCTORS AND CONTROLLED RECTIFIERS

Essential to the successful design of a pulse generator utilizing the circuit of Fig. 1.3 is exploitation of the special characteristics of the power switching devices it contains. Therefore, in preparation for analysis and design calculations, this chapter reviews the operating principles and characteristics of saturable inductors and silicon controlled rectifiers.

A. SATURABLE INDUCTORS

A saturable inductor comprises one or more coils of wire on a ferromagnetic core. To obtain a sharp break between the saturated and unsaturated states, it is desirable that the B-H characteristics of core material be of the rectangular ("square-loop") form indicated in Fig. 2.1(a). Parameters of this characteristic are the coercive force H_c, the saturated flux density B_s, and the saturated incremental permeability μ_s marked on the figure.

Usually a saturable inductor is given both a main winding (a saturable transformer has two or more main windings) and a bias winding--see the circuit-diagram symbol in Fig. 2.1(b). A convenient convention is to relate algebraic signs of B and H in Fig. 2.1(a) to polarity dots in Fig. 2.1(b) as follows: Current i into a dotted terminal produces a positive value of H; a positive rate of change of B yields a positive voltage e at the dotted terminal (relative to the undotted terminal).

In order that the integral-of-e-vs.-i characteristic of the inductor may be almost as sharply rectangular as the B-H characteristic of the core material, it is necessary to eliminate air gaps in the core, to distribute H as uniformly as possible throughout the core, and to minimize flux set up outside the core by the current i. To this end, it is desirable to employ a tape-wound toroidal core having a low ratio of outside to inside diameter, to distribute the main winding uniformly around the toroid, and to place each main-winding turn as close to the core as insulation and conductor cross section permit.

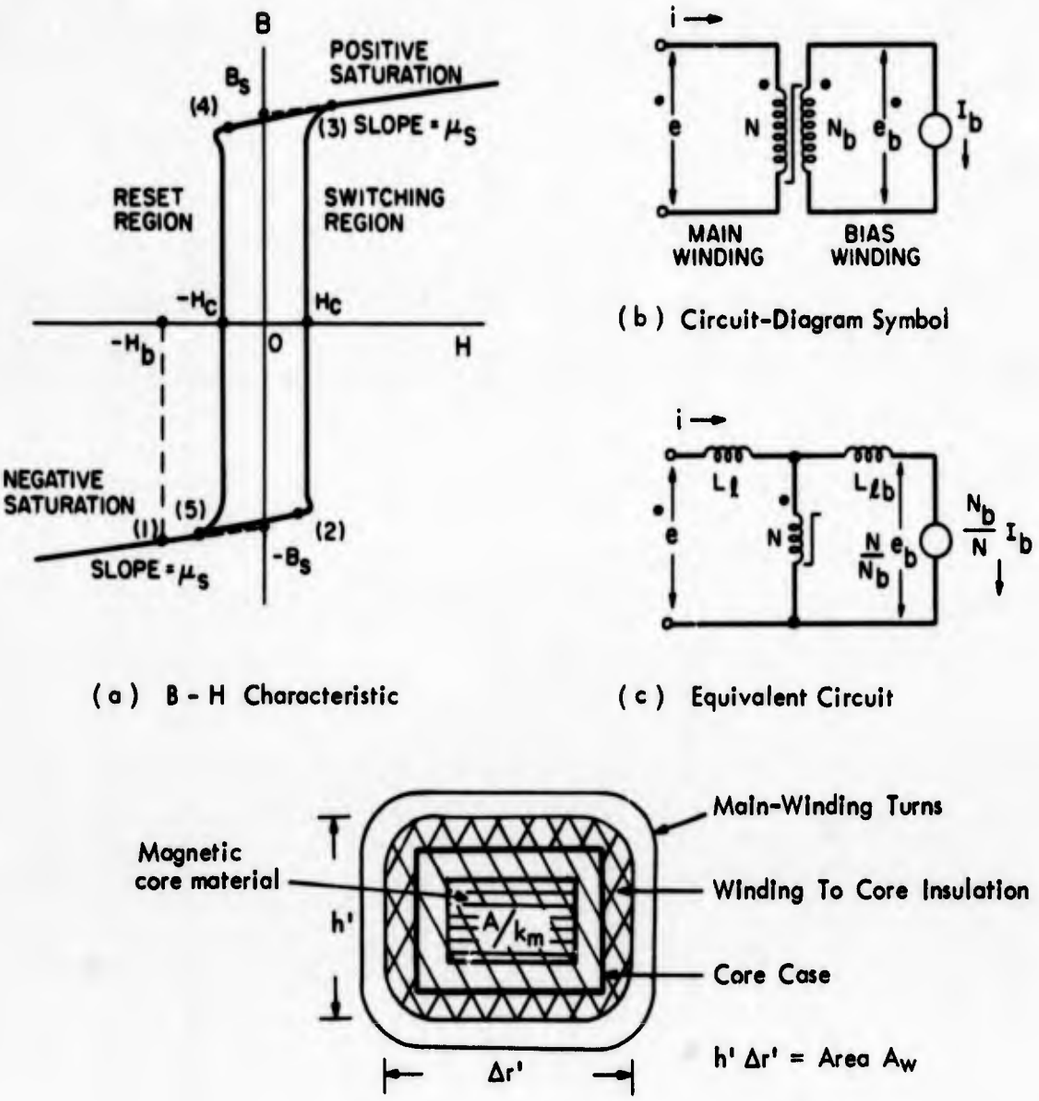

Fig. 2.1 The Saturable Inductor

The following discussion is restricted to saturable inductors of this kind.

Significant geometrical parameters of a toroidal core are the inner radius r, outer radius R, axial height h, cross-section area of magnetic material A, mean flux-path length ℓ, and volume of magnetic material V. Because of the near unity radius ratio R/r, ℓ may be taken to be the average of the inner and outer circumferences,

$$\ell = \pi(R + r) \qquad (2.1)$$

and the magnetic field intensity H at any point in the core may be approximated by the net magnetomotive force divided by ℓ. Insulation

necessary between layers of tape makes A less than the total core cross section h(R - r) (which area, in turn, is less than the cross-section area of the protective box in which tape-wound cores are usually mounted). Thus

$$A = k_m h(R - r) \tag{2.2}$$

where k_m is a stacking factor less than one. Since the volume of magnetic material is reduced in the same ratio as the cross-section area,

$$V = k_m \pi h (R^2 - r^2) = A \ell \tag{2.3}$$

1. Mode of Operation

Suppose in Fig 2. 1(b) that the main winding is initially open and that the bias current I_b (which is kept constant at all times) satisfies

$$I_b = \frac{H_b \ell}{N_b} \tag{2.4}$$

where N_b is the number of turns on the bias winding, and $H_b > H_c$. Initial operation at point (1) in the negative saturation region of Fig. 2.1(a) results.

Application of a voltage e to the main winding causes the operating point to move from (1). If e is negative, the operating point moves to the left in Fig. 2.1(a), and the main winding behaves as a very small inductance, the saturated inductance

$$L = \frac{N^2}{\ell} \mu_o \left[A_w + (\mu_r - 1) A \right] \tag{2.5}$$

where N is the number of turns on the main winding, μ_o is the permeability of air (0.4π microhenries per meter), μ_r is the relative permeability of the saturated magnetic material, and A_w is the area enclosed by the main winding - - larger than A because of the core case and the winding-to-case insulation [see Fig. 2.1(d)]. Equation 2.5 is an accurate expression for the single-layer-wound toroids of most interest. For preliminary calculations it is worthwhile to rewrite

Eq. 2.5 as if the only flux that links the main winding is flux in the magnetic core material, or

$$L = \frac{N^2}{\ell} \mu_e A \tag{2.6}$$

To allow for the other flux linkages implied in Eq. 2.5, an effective value μ_e of core saturated incremental permeability $\mu_s = \mu_o \mu_r$ is employed in Eq. 2.6, (see p. 2-8).

If e is positive, the operating point in Fig. 2.1(a) moves to the right and enters the switching region (or setting region) where i is limited to the value

$$I_{sw} = \frac{(H_b + H_c)\ell}{N} = \frac{N_b}{N} I_b + I_m \tag{2.7}$$

Here

$$I_m = \frac{H_c \ell}{N} \tag{2.8}$$

is the magnetizing current referred to the main winding. The current I_{sw} may be made small; thus the inductor may be given diode-like characteristics with I_{sw} playing the role of diode reverse current. If e is maintained positive after the time t_2 [at which the operating point reaches position (2) in Fig. 2.1(a)], the operating point moves steadily through the switching region and reaches point (3) at time t_3 when

$$\lambda = \int_{t_2}^{t_3} e\,dt = 2NB_s A \tag{2.9}$$

(For $H = H_c$, main-winding flux linkages other than core flux linkages are negligible.)

At point (3) the inductor saturates and the diode to which it is analogous is reversed. Further positive e values yield operation in the positive saturation region; current is again limited only by the saturated inductance L. For negative values of e, the current i cannot decrease below the positive value

$$I_r = \frac{(H_b - H_c)\ell}{N} = \frac{N_b}{N} I_b - I_m \qquad (2.10)$$

Throughout the reset region from point (4) to point (5) in Fig. 2.1(a), i remains constant at the value I_r while e is negative and a volt-time integral of magnitude λ is being built up. The equality in magnitude of areas under the e curve during switching and reset is an essential feature of saturable-inductor operation.

The above relationships may be obtained also from an equivalent circuit for Fig. 2.1(b) drawn in Fig. 2.1(c). The transformer of Fig. 2.1(b) is represented in the usual way as an ideal transformer plus magnetizing inductance (a one-winding saturable inductor) and leakage inductances (L_ℓ and $L_{\ell b}$). In Fig. 2.1(c) the ideal transformer is eliminated by referring all quantities to the main winding. The control of i by the bias current during switching and reset (see Eqs. 2.9 and 2.10) is evident in Fig. 2.1(c). Also evident, if the leakage inductance L_ℓ is negligible, is the turns-ratio relation between the main-winding and bias-winding voltages. The bias-winding voltage is important in the design of the circuit that maintains I_b constant.

Thus far the magnetizing current I_m has been treated as a constant. Actually I_m depends upon the speed with which switching and reset occur. In a semiconductor-magnetic pulse generator, a time of the order of milliseconds is usually available for reset, whereas the switching region may be traversed in less than a microsecond. For reasons given in Section A.4, it is a good approximation to associate a constant value of H_c with a slow reset operation, yet it is necessary to consider H variable during rapid switching. It is convenient, henceforth, to use H_c and I_m to represent the small, constant field intensity and magnetizing current in reset, to denote the smaller field intensity and magnetizing current of the d-c hysteresis loop by H_{co} and I_{mo}, and to represent the larger variable field intensity and magnetizing current during switching by H_c' and I_m', respectively. The reset quantities are several times the d-c-loop values, and for fast switching, I_m may be 10 to 50 times as large as I_m; even so, it is small relative to currents occurring after saturation.

2. Figures of Merit

The integral of voltage that must be applied to a linear inductor L to initiate a current i is $\lambda = Li$. Thus the stored energy $Li^2/2$ may be written alternatively $\lambda^2/2L$. For a saturable inductor, $\lambda^2/2L$ does not denote a specific stored energy, but it is nevertheless an important design parameter having the dimensions of energy. Equations 2.6 and 2.9 may be combined to yield

$$\frac{\lambda^2}{2L} = \frac{2B_s^2}{\mu_e} V \qquad (2.11)$$

Thus the magnetic-material volume V necessary in a saturable inductor is determined by the operating-conditions parameter $\lambda^2/2L$ and the core-material parameter $2B_s^2/\mu_e$. It is convenient to call $\lambda^2/2L$ the energy-switching capacity of the inductor, and $2B_s^2/\mu_e$ (the energy-switching capacity per unit volume of magnetic material) the energy-capacity figure of merit. This figure of merit is determined largely by the core material, but is somewhat affected (through μ_e) by the degree of saturation attained and the configuration of the winding.

The relationship of $\lambda^2/2L$ to the energy J_{st} stored in a saturable inductor at the point of peak saturation can be determined as follows. Because the energy absorbed by the magnetic field during switching is dissipated as core loss, J_{st} very nearly equals the peak energy that would be stored if the B-H characteristic lay along the B axis and the dashed saturation lines in Fig. 2.1(a). Thus if B_{max} is the peak flux density attained, the peak energy stored in the inductor is

$$J_{st} = V \int_{B_s}^{B_{max}} \frac{B - B_s}{\mu_s} \, dB = V \frac{2B_s^2}{\mu_e} \left(\frac{B_{max} - B_s}{2B_s} \right)^2 \qquad (2.12)$$

or by Eq. 1,

$$\frac{\lambda^2/2L}{J_{st}} = \left(\frac{\lambda}{\Delta\lambda} \right)^2 \qquad (2.13)$$

where

$$\Delta\lambda = N(B_{max}-B_s)A \qquad (2.14)$$

is the volt-time integral absorbed by the inductor during saturation. The ratio $\lambda/\Delta\lambda$ is determined by the circuit function of the inductor and may range, typically, from 1 to 100. It is the pulse-compression ratio provided by the inductor, expressed in terms of volt-time integrals rather than time intervals.

A second figure of merit may be defined in terms of the core loss in a cycle of operation

$$J_m = V \oint H\, dB \qquad (2.15)$$

This integral, which represents the area within the B-H loop for an actual operating cycle, may be split into portions pertaining to areas to the left and to the right of the B axis. The area to the left of the axis represents loss associated with the reset operation and is very nearly a rectangle of width H_c and height $2B_s$. The area to the right represents loss associated with the switching operation and traversal of the saturated region. Let $\phi(t_{sw})$ denote the ratio of right-hand to left-hand areas, t_{sw} being the switching time. Then

$$J_m = 2H_c B_s V\,[1 + \phi(t_{sw})]$$

and by Eq. 2.11

$$\frac{J_m}{\lambda^2/2L} = \frac{\mu_e H_c}{B_s}\,[1 + \phi(t_{sw})] \qquad (2.16)$$

Equation 2.16 specifies core loss per unit energy-switching capacity in terms of a <u>core-loss figure of merit</u> $\mu_e H_c/B_s$ and a factor $1 + \phi(t_{sw})$ dependent on speed of switching, core material, tape thickness, switching waveform, and (possibly)degree of saturation. By Eqs. 2.8 and 2.9, the resetting core loss $2H_c B_s V$ is equal to $I_m\lambda$. Hence

$$\frac{I_m\lambda}{\lambda^2/2L} = \frac{\mu_e H_c}{B_s} \qquad (2.17$$

3. Core Materials and Parameter Values

A number of square-loop magnetic materials are available. Among them 50-percent-nickel iron,[1] a highly grain-oriented nickel-iron alloy containing 50 percent nickel, offers a sharply rectangular B-H characteristic in combination with a high saturated flux density, low coercive force, and low saturated permeability- - hence a high energy-capacity figure of merit $2B_s^2/\mu_e$ and low core-loss figure of merit $\mu_e H_c/B_s$. All saturable inductors in the pulse generators to be described have used 50-percent-nickel iron in toroidal cores wound of 1-mil or 0.5-mil tape.

A thin tape is desirable from the standpoint of reducing eddy currents and thus reducing the magnetizing current and core loss at high switching speeds. On the other hand, thin tapes lead to undesirably low values of the stacking factor k_m. Typically, k_m is 0.75 for 1-mil tape, and 0.5 for 0.5-mil tape. Low stacking factors are undesirable primarily because they contribute to the increase of μ_e by flux outside the saturable material.

For 50-percent-nickel iron the saturated flux density B_s, though somewhat affected by temperature and tape thickness, may be taken for most design purposes to 0.4 webers per sq. m. Note that this flux density exists only within the magnetic-material area A, not throughout the total core area A_w.

The effective saturated permeability μ_e is less easy to specify. Despite the sharp-saturation characteristic of 50-percent-nickel iron, the incremental relative permeability μ_r remains somewhat greater than one throughout the saturation region usually of interest. Experience gained through construction and measurement of many saturable inductors with 50-percent-nickel iron cores has shown that the value $\mu_r = 2.3$ used with actual A and A_w values in Eq. 2.5 leads to accurate results. Relative values of A and A_w, however, vary considerably with inductor design, and μ_e varries correspondingly.

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1. Available from several manufacturers under various trade names including Deltamax, H. C. R. Metal, Hypernik V. Orthonik, Orthonal, Permenorm 5000Z, Permeron, and 49 Squaremu.

For preliminary design calculations, a rough estimate of L can be obtained from Eq. 2.6, using μ_e = 4 microhenries per meter. The effective value of the coercive force H_c for 50-percent-nickel iron to be used in calculating the core-loss figure of merit and the magnetizing current during reset is also somewhat indefinite. Even at the relatively slow speeds typical of reset, the effective H_c is appreciably greater than the half-width of the d-c loop (8 amp per m). For reasons given in the next section a value of 28 amp per m has been found to be a good approximation if the reset time lies between 100 and 4000 μs.

In terms of these values of B_s, μ_e, and H_c, the energy-capacity and core-loss figures of merit for saturable inductors using 50-percent-nickel-iron cores are:

$$\underline{\text{Energy Capacity Figure of Merit}} \quad \frac{2B_s^2}{\mu_e} = 10^6 \text{ joules per cu m} \qquad (2.18)$$

$$\underline{\text{Core-loss Figure of Merit}} \quad \frac{\mu_e H_c}{B_s} = 0.8 \times 10^{-4} \qquad (2.19)$$

4. Core Losses

Both core and main-winding losses in saturable inductors are important. Either may predominate, depending on the requirements of the application, and together these losses have significant effect on the efficiency attainable in semiconductor-magnetic pulse generators. Core losses are discussed in this section; winding losses are treated in Section 5.

Measured core-loss data for 50-percent-nickel iron operating under conditions typical of pulse-generator saturable inductors, unfortunately, are scant. Figure 2.2 presents a summary of data obtained from several sources--manufacturers' literature, a report[1] of the Polytechnic Institute of Brooklyn, and core-loss measurements made in this laboratory (both calorimetrically and by measuring areas of oscilloscope presentations of B-H loops). Data in the figure apply

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1. E. J. Smith, J. Antin, K. T. Lian, "Magnetic Modulators for Radar Applications", (Report R-419-55, PIB-351, M.R.I., Polytechnic Institute of Brooklyn, April 1955.)

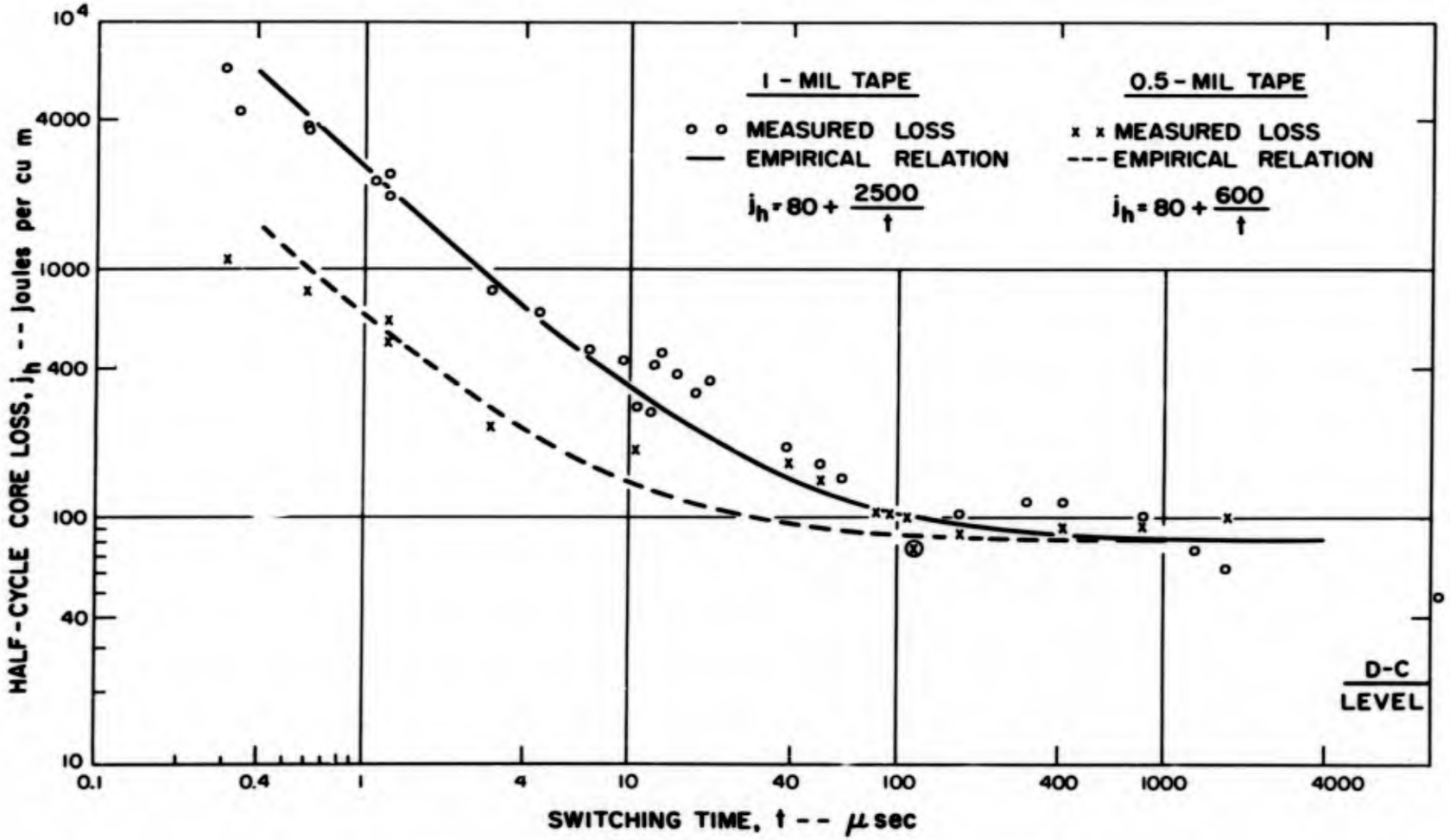

Fig. 2.2 Half-Cycle Core-Loss Data for 50 Percent-Nickel Iron in Tape-Wound Core

to a symmetrical B-H loop extending into both saturation regions, with switching time and reset time each equal to t; the function plotted, $j_h(t)$, is <u>half</u> of the energy loss per cycle per unit magnetic-material volume V. Because j_h equals the area of the portion of the B-H loop to either side of the B axis, the core loss per cycle in typical saturable-inductor operation with unsymmetrical B-H loop is very nearly

$$J_m = [j_h(t_{sw}) + j_h(t_r)]\ V \qquad (2.20)$$

where t_{sw} amd t_r denote the switching and reset times, respectively.

The dispersion of points in Fig. 2.2 is not surprising. Core loss depends not only on the switching time, but also on the switching waveform. Most of the data were taken with a switching-voltage waveform $1 - \cos(\pi t/t_{sw})$, but some of the points are for constant switching voltage. The peak field intensity is not known for many of the points. Some of the loss measurements were made with a reset time much longer than the switching time; for these the loss in the reset half of the cycle was estimated and subtracted from the measured loss to obtain the j_h values plotted. Also, it is suspected that many of the measurements were made with peak field intensities far in the saturation region. These measurements may have included as core loss large losses due to eddy currents occurring during saturation in the core laminations, metallic protective cores (and possibly in winding turns). As discussed below in Section 5, it has been found convenient to consider, in one category, the core loss associated with the switching and reset operations, and, in a separate category, losses in the winding, core material, and protective case (if metallic), associated with current flow in the saturation interval.

For each saturable inductor in the semiconductor-magnetic pulse generator of Fig. 1.3, the switching-voltage waveform approximates either the constant-voltage or the $1 - \cos(\pi t/t_{sw})$ shape. Therefore, in view of Fig. 2.2, it is assumed that for 50-percent-nickel-iron cores the empirical relations

$$\left.\begin{array}{ll} \text{For 1-mil tape:} & j_h = 80 + \dfrac{2500}{t} \qquad (2.21) \\ \text{For 0.5-mil tape:} & j_h = 80 + \dfrac{600}{t} \qquad (2.22) \end{array}\right\} \text{joules per cu m } (t \text{ in } \mu_s)$$

are adequate approximations for use in Eq. 2.20, providing the switching and reset times lie in the range of 0.4 to 4000 μs.

The relative constancy of j_h (at approximately 80 joules per cu m) over the range of typical reset times--100 to 4000 μs--is the reason for assuming a constant value of H_c during reset. In fact, dividing 80 joules per cu m by 2.8 webers per sq m ($2B_s$) yields, very nearly, the value 28 amp per m given for H_c in Section A.3. Note that for t greater than about 4000 μs, j_h decreases toward a final limit of 23 joules per cu m (half the area of the d-c hysteresis loop). Correspondingly, for very long reset times H_c decreases from 28 amp per m toward the d-c coercive force H_{co} of 8 amp per m.

The function $\phi(t_{sw})$ introduced in Eq. 2.16 is by definition equal to $j_h(t_{sw})/j_h(t_r)$. Thus, for t_{sw} between 0.4 and 4000 μs and t_r in the 100-to-4000-μs range, Eqs. 2.21 and 2.22 yield

$$\left.\begin{aligned} &\text{For 1-mil tape:} \quad \phi(t_{sw}) = 1 + \frac{31}{t_{sw}} \qquad (2.23) \\ &\text{For 0.5-mil tape:} \quad \phi(t_{sw}) = 1 + \frac{7.5}{t_{sw}} \qquad (2.24) \end{aligned}\right\} \quad (t_{sw} \text{ in } \mu s)$$

5. Winding Losses

Resistance losses in the main windings of saturable inductors in short-pulse modulators are markedly influenced by skin and proximity affects in the winding conductors. In consequence, both the amount of the loss and the optimum winding form are dependent on the duration of the inductor current pulse. This dependence is complex; only a few general principles of special importance are discussed here.

Let ℓ_w be the average length per turn, a_c the conducting-material cross section, and ρ the resistivity of the wire used in the inductor winding. The resistance of an N-turn winding is then $N\rho\ell_w/(\eta a_c)$, where η is a coefficient less than one introduced to account for skin and proximity affects--the crowding of fast-changing currents into portions of the conducting area nearest the core so that only the portion ηa_c of the cross section a_c is utilized. In terms of the total useful conductor cross section in the winding,

$$a = N\eta\, a_c \tag{2.25}$$

Therefore,

$$R = N^2 \rho \frac{\ell_w}{a} \tag{2.25a}$$

and the energy loss per cycle of operation is

$$J_w = N^2 \rho \frac{\ell_w}{a} \int_0^{T_r} i^2\, dt \tag{2.25b}$$

where i is the winding current and T_r the repetition period. Inasmuch as saturation-period currents are many times switching and resetting currents, the integral in Eq. 2.25(b) can be evaluated as $I_{max}^2\, T_{sat}/2$ where I_{max} is the peak value of a half-sine current pulse of duration T_{sat}. (For other saturation-interval current waveforms, T_{sat} is adjusted to an effective value--for example, twice the saturation time if the current pulse is rectangular.) Evaluating $I_{max} = H_{max}\, \ell/N$ in terms of

$$H_{max} = \frac{B_{max} - B_s}{\mu_e} = \frac{B_s}{\mu_e} \frac{\Delta\lambda}{\lambda}$$

yields, with the aid of Eqs. 2.3, 2.11, and 2.13,

$$\frac{J_w}{J_{st}} = \frac{\rho T_{sat}}{4} \frac{\ell}{a} \frac{\ell_w}{A} \tag{2.25c}$$

Inasmuch as ρ is determined by the conductor material (copper) and T_{sat} by the required operation of the inductor, minimizing the inductor loss ratio J_w/J_{st} requires maximizing:

(1) The ratio a/ℓ. This ratio may be considered an effective winding depth --when multiplied by ℓ (somewhat more than the winding length) it equals the useful conductor cross-section a.

(2) The ratio A/ℓ_w--or the area-to-perimeter ratio for the core times the ratio (less than one) of core perimeter to ℓ_w.

For d-c or very low-frequency inductors, the procedure, once a specific core has been chosen, is to maximize a/ℓ by selecting a wire size so that, with minimum space lost to insulation, the core window is

filled. In short-pulse modulators, skin and proximity effects (through their effect on η) place a practical limit on a/ℓ that is often far less than that corresponding to a full core window. In consequence the inductor losses are increased, and this increase cannot be avoided by using more copper in the winding. In fact, adding conductor cross section is doubly undesirable because it increases both the losses and the weight of the inductor.

One useful form of short-pulse inductor winding comprises a single-layer of turns arranged to fill the inner perimeter of the core-plus-insulation toroid as completely as possible. For some high-voltage windings, it may be possible to choose a wire size such that the required number of turns N exactly fills the available space. More often, however, to avoid requiring impracticably large wire, it is necessary to employ a K-filar winding, where K is an integer chosen so that KN strands of convenient-size wire fill the space available. For example, if K = 4, four strands of wire are laid side-by-side to form a four-element "tape", and N turns of this "tape" are wound on the core. The four strands are connected in parallel at each winding terminal; inter-strand insulation is necessary only between strands in different turns. It is essential that all strands of all turns fit in a single layer against the core insulation, and that the available winding space be filled as evenly and completely as possible. The wire diameter d (of a single strand) is immaterial, provided only that it is appreciably greater than the skin depth δ--which may be estimated as $2.6/\sqrt{f_{mc}}$ mils, where f_{mc} (in megacycles per second) is taken in the range of important frequency components of the current pulse. For current pulses of several microseconds duration, δ is of the order of 5 to 10 mils, and $d \gg \delta$ for wire strands of moderate size convenient for winding.

Losses in a single-layer winding are high (relative to losses in a well-designed low-frequency winding) because $\underline{a}$ in Eq. 2.25(c) is δ times the conductor-occupied part of the core-plus-insulation inner perimeter, which is somewhat less than ℓ. Thus a/ℓ is at most a few mils for current pulses in the several-microsecond range. Unfortunately, the losses cannot be reduced by increasing or decreasing wire size in the single-layer winding, or if the condition $d > \delta$ is maintained,

by providing more conductor cross-section in a multiple-layer winding. In a $d>\delta$ multiple-layer winding, the layers of conductors function much as the walls in a waveguide. Each interlayer space forms (with the conductors on either side) a substantially isolated small inductor in which losses (associated with skin-depth conduction in layers to either side) are high.

For short-pulse inductors, the only useful alternative to the single-layer winding is a multiple-layer construction in which the condition $d<<\delta$ is satisfied for individual strands. Then

$$\frac{\text{Loss in one turn of any one strand}}{\text{D-c loss in same turn of same strand}} \approx 1+\frac{1}{3}\left[\frac{H}{\Delta H}\left(\frac{d}{\delta}\right)^2\right]^2 \qquad (2.26)$$

where H is the magnetic field intensity in the vicinity of the strand of wire considered (caused by currents in all the layers of strands wound over it) and ΔH is the increment of H from one side of the strand to the other (caused by current in that strand). For strands nearest the core, $H/\Delta H \approx n$, the total number of layers of strands in the winding. Thus, if $t \approx nd$ denotes the portion of the total depth of winding occupied by conductors, then $t/d \approx H/\Delta H$, and Eq. 2.26 indicates that losses in the innermost layer of strands become large rapidly if t/d is allowed to increase much beyond δ/d. In effect, t/δ must be limited to a few times δ/d to avoid a decrease of μ in Eq. 2.25 that more than offsets the increase of a_c provided by increase of t.

The most practical means of producing multiple-layer windings with $d<<\delta$ is use of very finely stranded litz wire. In this wire many insulated strands are twisted together so that each occupies all possible positions to approximately the same extent. Thus the total flux linkages are the same for each strand, and, with the strands connected in parallel at the winding terminals, the current divides equally among the strands. For current-pulse durations of the order of 100 μs or more, litz-wire windings can be constructed to provide significantly less loss than single-layer windings. The advantage of the litz wire becomes less for shorter pulses, and disappears altogether when the skin depth becomes only a little less than the smallest available strand diameter. For example, suppose δ = 5 mils, and that 2-mil conductors with 2-mil-thick insulation are the smallest strands available. For $\delta/d=2.5$, a

winding with $t/\delta = \delta/d$, or $t = 12.5$ mils provides an a-c loss substantially equal to its d-c loss, so that $\underline{a}$ in Eq. 2.25(c) can be taken equal to $12.5/3 \approx 4$ mils times the core-plus-insulation inner perimeter--where the factor 1/3 enters because the perimeter is occupied about 2/3 by insulation and only about 1/3 by conductors. In comparison, for a single-layer winding $\underline{a}$ can be very nearly δ (5 mils) times the perimeter. Slightly less loss may be possible in a litz winding of somewhat larger t, but the improvement is sharply limited by the increased a-c/d-c loss ratic for $t/\delta > \delta/d$.

The fast-changing flux that causes skin and proximity effects in saturable-inductor windings also causes saturation-interval eddy-current losses in the magnetic-core material (as mentioned in connection with Eq. 2.20) and in the protective case for the core--if the case is metallic. It has been found convenient to account for these losses in connection with winding loss rather than with the major core loss; like winding loss, they are determined by saturation-interval current, whereas the major core loss is a function of switching and resetting voltage waveforms. Metallic-cased cores should be avoided (plastic cases are available) in short-pulse modulator applications because eddy-current losses in them are large, sometimes more than the loss in a single-layer winding. This loss occurs despite the fact that metallic cases are always split to avoid short-circuiting the inductor. For pulses of a few microseconds duration, skin depths in the case metal (usually aluminum) are much less than the metal thickness, and the loss associated with skin-depth conduction in $\underline{\text{each}}$ side of the case is a large fraction of the skin-depth-conduction loss in a (copper) single-layer winding. The same changing flux that causes these losses penetrates the saturated magnetic core material. The eddy-current losses produced, though not negligible, are usually relatively small because the magnetic tape is thin.

B. SILICON CONTROLLED RECTIFIERS

The controlled rectifier is a three-terminal PNPN silicon-semiconductor switching device with terminal characteristic similar to those of a thyratron. Units with rms current ratings of 1.6 amp

to 400 amp and peak voltage ratings (forward and reverse) from 25 to 1800 volts or more are available. The following discussion is limited to controlled-rectifier characteristics of concern in semiconductor-magnetic pulse generators.[1]

1. General Description

The active element of a silicon controlled rectifier is a silicon wafer about 0.01 in. thick and a few tenths of an inch across its faces. A relatively massive metal structure, the anode, covers all of one face and is used both for electrical connection and to conduct away heat. The cathode occupies the opposite face, except for a small area--either near the edge or in the center, depending on the manufacturer--reserved for the gate electrode. A low concentration of donor (N-type) impurities is provided throughout the silicon. To this is added an acceptor density distribution, grading from zero in a center layer to high at the electrode surfaces, and a very high donor concentration in a thin layer adjacent to the cathode. Thus is formed a PNPN layer structure (anode to cathode) in which the second P layer connects to the gate. The anode and center P-N junctions are substantially identical (except for orientation) and have excellent blocking characteristics when back-biased. The reverse saturation current of the cathode junction, in contrast, is high because of the mixed impurities in its vicinity.

The anode current i, anode voltage e, and gate current i_g of a controlled rectifier are defined with reference to the circuit-diagram symbol in Fig. 2.3(a). An anode static characteristic for $i_g = 0$ appears in Fig. 2.3(b). Note the distinct blocking and conducting states which give rise to switching applications of controlled rectifiers. Numerical values are typical for Type 2N689 rectifiers, for which the rms-current rating is 25 amp and the peak-voltage rating (forward and reverse) E_r is 500 volts.

For e negative, the blocking state is accounted for by the back-biased anode junction. (The center junction is forward biased, and the back-biased cathode junction absorbs little voltage because of its

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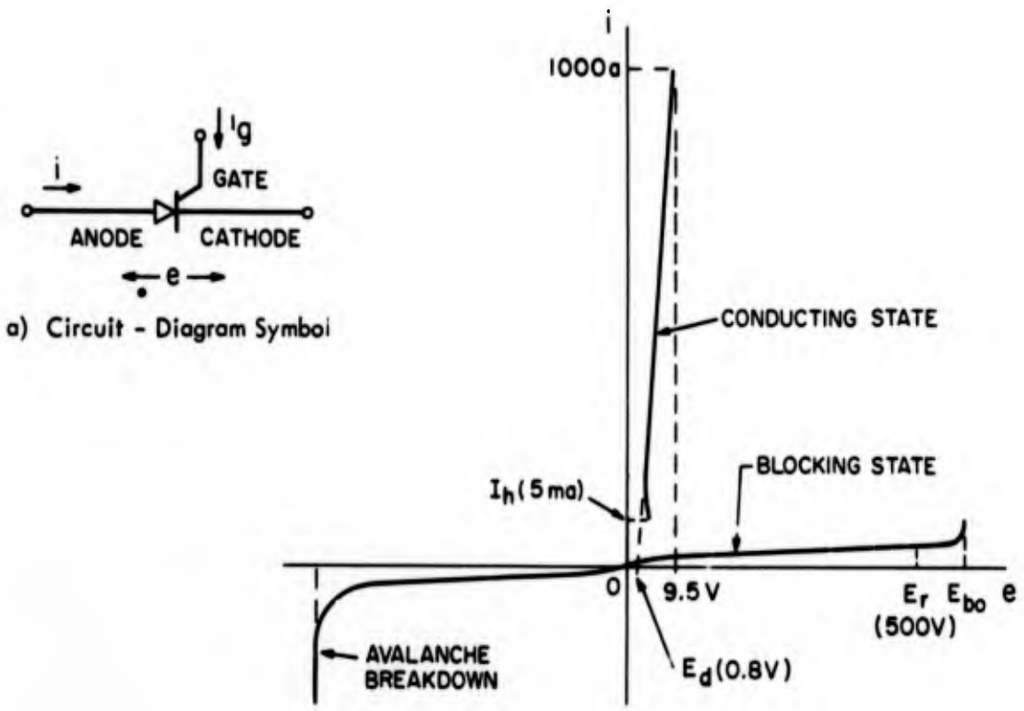
1 An excellent discussion of principles, construction, and characteristics of controlled rectifiers is given in: E. J. Diebold (editor), The Controlled Rectifier, Vol. I, (International Rectifier Corp., El Segundo, California, 1962).



a) Circuit - Diagram Symbol

b) Anode Static Characteristic for $i_g = 0$
(Numerical Values Apply to Type 2N689)

Fig. 2.3 Static Characteristic of Controlled Rectifier

high leakage current.) The voltage limit of the reverse blocking characteristic is imposed by ordinary avalanche breakdown; power dissipation sufficient to destroy the rectifier accompanies even moderately large avalanche currents.

For e positive, the center junction is back-biased and produces the blocking-state characteristic. Because of the symmetry of the anode and center junctions, the forward and reverse blocking characteristics are substantially alike. In forward blocking, however, thermally generated minority carriers in the central P and N region are augmented not only by avalanche multiplication but also by carriers injected at the forward-biased anode and cathode junctions. Avalanche multiplication depends on voltage drop, whereas the carrier-injection process becomes more efficient as current increases. Thus, avalanche multiplication yields the sharp increase in current at the forward breakover voltage E_{bo}, and above a critical current level (about 5 ma in the figure) the voltage drop decreases suddenly as the injected carriers become sufficient to sustain current. At

this point the rectifier switches to its conducting state; that is, it turns on.

The conducting state is characterized by high currents (and high minority-carrier densities in the central P and N regions) and low voltages. In fact, a reversed voltage drop occurs across the center junction, so that the total voltage e is more nearly that of a single conducting P-N junction than the sum of three junction voltages. To regain the blocking state, or turn off the rectifier, the current i must be reduced to less than the holding current I_h.

The gate terminal of a controlled rectifier provides a means of turning on the rectifier without application of a large anode voltage. A positive gate-cathode current i_g increases the anode current (by injecting electrons into the central P region) and turn-on occurs when the anode current becomes sufficient to provide a self-sustaining conducting state. A gate-current pulse of a few microseconds duration suffices. The minimum gate current required depends markedly on temperature and varies among units of a given type. For rectifiers of 25-amp rms rating, a typical value is 40 ma at 25 C (much larger currents--2 amp for the 2N689--are allowable, and should be used to ensure turn-on). This gate current must be delivered to a gate-circuit impedance approximately equivalent to a battery of 1 or 2 volts in series with a resistance of about 10 ohms.

In the semiconductor-magnetic pulse generator of Fig. 1.3 the breakover voltage of each controlled rectifier exceeds the applied forward voltage. Each rectifier is thus in its blocking state until turned on by a gate-current pulse.

Turn-off of each rectifier occurs when the circuit attempts to reverse the rectifier current. During the blocking interval, positive gate current must be avoided; it increases the anode current (and dissipation) and could cause undesired turn-on. A small negative gate voltage in this interval speeds the recovery of forward blocking capability (see Section B.2).

For controlled rectifier S_1 in Fig. 1.3, the reverse voltage to be blocked is usually considerably larger than the forward

voltage. Inasmuch as the controlled-rectifier characteristic is nearly symmetrical, it is often desirable to block most of the reverse voltage by means of a semiconductor diode of appropriate rating connected in series with S_1. For controlled rectifier S_2, forward voltage is applied very suddenly when capacitor C_1 is discharged. The rate of change of voltage (typically 100 volts per μs) may cause turn-on at a forward voltage less than the breakover value. (The changing voltage produces a displacement current in S_2 that adds to the normal current of the blocking state so that a current sufficient to initiate conduction occurs at lower voltage.) Circuits to limit the rate of applying voltage to S_2 are discussed in Chapter III, Section C. For controlled rectifier S_3, the conduction period is very short--of the order of 10 μs--thus special attention must be given to turn-on and turn-off times and their effects upon rectifier dissipation and current ratings. These topics are discussed in the three following sections.

2. Turn-on and Turn-off

Turn-on of a controlled rectifier begins in a very localized region of the central P and N layers--a region under an edge of the cathode and adjacent to the gate when gate current initiates turn-on. The boundaries of the high-current-density turned-on region then propagate across the rectifier. The time required to establish the conducting state over the entire junction area is considerably longer than the conventionally specified turn-on time. This latter is the time required, after application of gate current, for current in the rectifier and a resistive load to increase to 90 percent of its final value. So defined, turn-on time is a function of load resistance; under standard test conditions only a small fraction of the junction area is conducting when the 90-percent current point is reached. For example, the conventional turn-on time for a 25-amp (rms) rectifier is 2 μs. For the conducting area to spread over the entire junction of this rectifier requires on the order of 50 μs.

Turn-on time is not important in applications requiring long conduction periods, but is very important for rectifier S_3 in the pulse generator of Fig. 1.3. Current pulses in S_3 have durations of a few tens of microseconds, at most, and tremendously large peak values. If turn-on is not complete, these pulses must pass through

whatever fraction of the junction area is conducting. If the fraction is small, abnormally large power losses result and lead to excessive temperatures within the rectifier. To avoid this excess loss, it is desirable to limit current during turn-on and to apply the brief, high-current pulses after the turned-on fraction is large.

Turn-off of a controlled rectifier also requires time. The high densities of minority carriers in the central P and N layers must be reduced to the low densities of the blocking state. The excess carriers disappear by recombination in about 100 μs, but the process can be hastened by a reverse turn-off current. The rectifier remains conducting until the reverse current removes carriers from the vicinity of the anode junction. Thereafter, the anode junction recovers its reverse blocking capacity suddenly; a reverse voltage appears, and the current decreases more or less exponentially to its normal blocking-state value. The total minority-carrier charge moved by the reverse current equals the integral of current over the last several microseconds of forward conduction. After reverse-voltage recovery, the current resulting from the diffusion of minority carries outward from the center-junction region; this process must be substantially complete for the center junction to recover its forward-blocking capability. The time from reverse to forward recovery depends upon the rate of rise of the applied forward voltage; for rates less than 10 volts per μs, a time of about 15 μs suffices.

Turn-off time, like turn-on time, is important in short-pulse applications. For example, if inductor L_2 were omitted from the circuit of Fig. 1.3, the reverse-recovery time of controller rectifier S_3 would cause a partial discharge of capacitor C_2 after the transfer of charge from C_1 to C_2 is complete. If the charging interval is long, the charge lost is negligible. For short charging times, however, not only might a major portion of the C_2 charge be lost, but also significant rectifier power dissipation during turn-off is possible.

A useful current-limiting device, effective during both turn-on and turn-off, is a series hold-off inductor (saturable inductor L_2 in Fig. 1.3). This inductor is unsaturated and thus limits current during the switching intervals of the controlled rectifier. It saturates when S_3 is in its conducting state to permit large currents to transfer

charge from C_1 to C_2.

The essential features of hold-off inductor operation may be described by reference to the simplified circuit of Fig. 2.4. Initially

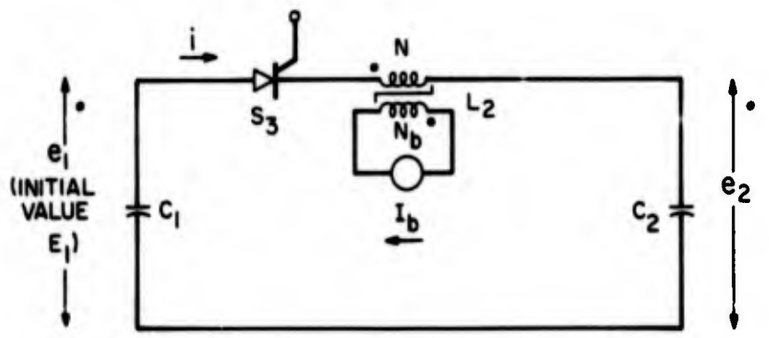


Fig. 2.4 Controlled Rectifier with Hold-Off Inductor

capacitor C_1 is charged to a positive voltage E_1, controlled rectifier S_3 is in its blocking state, hold-off inductor L_2 is biased in negative saturation by the current I_b, and capacitor C_2 is discharged. The blocking-state controlled-rectifier current i is too small to remove the operating point of L_2 from negative saturation. Upon application of a gate-current pulse to S_3, i increases to the limit $I_bN_b/N + I_m'$ imposed by L_2 (see Section A.1). The inductor parameters and bias current are chosen so that $I_bN_b/N + I_m'$ is large enough to ensure rapid turn-on of S_3, yet small enough to prevent excessive dissipation in S_3 during the turn-on interval.

The voltage E_1, originally blocked by the controlled rectifier, transfers quickly to inductor L_2 when the rectifier is triggered. This voltage remains across L_2 and i remains equal to $I_bN_b/N + I_m'$ throughout the hold-off interval, the time required for L_2 to switch from negative to positive saturation. By design of the inductor, the hold-off interval is made long enough and $I_bN_b/N + I_m'$ is large enough, so that when L_2 saturates the controlled rectifier is ready to conduct very large currents (possibly 1000 amp, peak, in a rectifier

of 25-amp, rms, rating).

Saturation of L_2 is equivalent to closing a switch in a series circuit comprising C_1, C_2, and the saturated inductance of L_2. The ensueing transient is a slightly damped sinusoid, and (if $C_1 = C_2$) transfers the charge originally on C_1 to C_2 in the first half-cycle of current oscillation. The inductor interrupts this oscillation a few degrees before the end of the half-cycle--when i decreases to $I_b N_b/N - I_m$ (see Section A.1), and reset of L_2 begins.

The current $I_b N_b/N - I_m$ must be much larger than the holding current of S_3. Then the reset voltage has a magnitude very nearly equal to $e_2 - e_1$. In Fig. 2.4 the large voltage stored on C_2 would reset L_2 in a time equal to the hold-off interval. In the pulse generator, however, transfer of energy from C_2 to the load quickly reduces the resetting voltage (for details, see Chapter III, Section B.1), and the resetting time is much longer. When L_2 saturates, reverse current flows in S_3 only long enough to remove the small minority-carrier charge associated with the current $I_b N_b/N - I_m$. Thus the conducting state terminates quickly and the rectifier recovers its reverse blocking characteristic with negligible turn-off dissipation. Shortly after the reverse recovery, S_3 recovers its ability to block forward voltage, at which point C_1 may be recharged to begin the next cycle of operation.

3. Power Dissipation

The power dissipated in the controlled rectifiers in a semiconductor-magnetic pulse generator is important primarily because its heating effect limits the current that may safely be passed through the rectifiers (see Section B.4); its contribution to over-all pulse-generator losses is usually small. In pulse-generator applications the energy dissipation during the blocking period is nearly always negligible. If hold-off inductors are utilized whenever current pulses are short, the dissipation during turn-off can also be ignored. Thus the total dissipation becomes the energy lost during the conducting interval, including the time required for turn-on.

After turn-on is complete, the high-current portion of the conducting state e-i characteristic of a controlled rectifier can be

approximated very closely by a straight line. That is

$$e = R_s i + E_d \tag{2.27}$$

where the rectifier resistance R_s is the reciprocal slope of the approximating line, and the diode voltage E_d is the e-axis intercept. Thus the instantaneous dissipated power is

$$p = R_s i^2 + E_d i \tag{2.28}$$

At the beginning of the conduction period, however, turn-on is incomplete and the rectifier power loss is greater than Eq. 2.28 specifies. If the increased loss is ascribed to an increase in rectifier resistance from R_s to xR_s caused by the reduced junction area in conduction,

$$p = xR_s i^2 + E_d i \tag{2.29}$$

Unfortunately only very limited data for determining x as a function of time for various rectifiers and applied-current waveforms are presently available. Data applicable if no hold-off inductor is employed are given by some manufacturers*. Of more interest for the circuit considered here are data applicable when a hold-off inductor delays the rise of current. Some measurements of turn-on times and losses with hold-off inductors performed at the Electronic Systems Laboratory indicate that turn-on speed is a function not only of the particular rectifier and the current during hold-off, but also of the height and width of the gate-current pulse. The optimum gate-current waveform in a given controlled-rectifier application is a fast-rising rectangular pulse of maximum allowable amplitude and a duration equal to the hold-off interval.

Of major interest is the total energy J_s dissipated in rectifier S_3 of Fig. 1.3 during each current pulse. The calculation of this energy can be simplified as follows. First, the dissipation during

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* N. Mapham, "The Rating of SCR's when Switching into High Currents", IEEE Conf. Paper CP-63-498, (IEEE Winter General Meeting, January 29, 1963); see also D. E. Burke and G. W. Albrecht, "RCA 40216 Silicon Controlled Rectifier: Design Considerations and Device Data for use in High-Current Pulse Applications", Application Note SMA-29, RCA Electronic Components and Devices, Somerville, N. J., December, 1963.

the hold-off interval can be ignored if, as is usual, the hold-off current is orders of magnitude less than the peak current. Second, the rectifier resistance xR_s, which varies during turn-on, may be replaced by a constant value equal to the actual resistance at the peak of the current wave. The total energy dissipated is little affected by this change since most of the energy is dissipated in a brief interval about the current peak. Thus

$$J_s = \int_o^T \left(xR_s i^2 + E_d i \right) dt \qquad (2.30)$$

where x is evaluated at the time of peak current. Since the current pulse is substantially the half sinusoid typical of resonant charging, of peak value I_p and duration T (see Chapter III, Section B.1), Eq. 2.30 yields

$$J_s = \frac{1}{2} \times R_s I_p^2 T \left(1 + \frac{4}{\pi} \frac{E_d}{xR_s I_p} \right) \qquad (2.31)$$

For low-duty-ratio pulse generators, the term $4E_d/\pi xR_s I_p$ in Eq. 2.31 is usually small--typically, $xR_s I_p$ is more than 10 times E_d. Under these conditions, and if the hold-off interval is sufficient to allow complete turn-on before the time of peak current, Eq. 2.31 simplifies to

$$J_s = \frac{1}{2} R_s I_p^2 T \qquad (2.32)$$

It is convenient to regard Eq. 2.32 as specifying a nominal value of energy loss. The actual energy loss is greater in accord with Eq. 2.31 if the duty ratio is large enough to make $4E_d/\pi xR_s I_p$ appreciable, or if the hold-off interval plus T/2 is inadequate to reduce x to 1 at the time of peak current.

4. Voltage, Current, and Power Ratings

The current in controlled rectifier S_3 in the pulse-generator circuit of Fig. 1.3 is a pulse of substantially half-sine form, duration T, repetition period T_r, and peak value I_p. The current during the hold-off interval preceding this pulse is too small to affect appreciably the rms value I and average value I_{av} of the rectifier

current. Thus

$$I^2 = \frac{1}{2} I_p^2 \frac{T}{T_r} \tag{2.33}$$

and

$$I_{av} = \frac{2}{\pi} I_p \frac{T}{T_r} = \frac{2\sqrt{2}}{\pi}\sqrt{\frac{T}{T_r}}\, I \tag{2.34}$$

The charge $I_{av} T_r$ transferred through the rectifier by the current pulse is very nearly the total charge initially on capacitor C_1. Thus, if E is the capacitor voltage blocked by S_3 prior to each current pulse, the initial energy stored in C_1--which, except for losses, is transferred through S_3 to C_2 and appears eventually in the output pulse--is

$$J_c = \frac{1}{2} E(I_{av} T_r) = \frac{\sqrt{2}}{\pi}\sqrt{TT_r}\,EI \tag{2.35}$$

Hence, the per-pulse energy-switching capacity of S3 is determined by the geometric mean of the pulse and repetition periods and the maximum allowable values of E and $\underline{I}$. If E_r denotes the allowable forward-blocking voltage (the applied reverse voltage is small in comparison) and I_r denotes the allowable rms current

$$P_r = E_r I_r \tag{2.36}$$

denotes the power-switching capacity of S_3, and the energy-switching capacity is obtained by writing P_r for EI in Eq. 2.35.

From an efficiency standpoint, increase of $\underline{I}$ to I_r to realize the full switching capacity is not always desirable. Combining Eqs. 2.34 and 2.35 with Eq. 2.31 yields the controlled-rectifier loss per-unit transferred energy,

$$\frac{J_s}{J_c} = \frac{\pi}{\sqrt{2}}\sqrt{\frac{T_r}{T}}\left(\frac{xR_s I}{E} + \frac{2E_d}{E}\right) \tag{2.37}$$

Thus J_s/J_c increases with $\underline{I}$, and (especially if the repetition frequency is low--T_r large) may become impractically large for $\underline{I}$ equal to I_r. Increase of E to the allowable value of E_r, on the other hand, is desirable both for utilization of the rectifier capacity and to reduce J_s/J_c.

The allowable forward voltage E_r is determined by the possibility of forward breakover prior to the trigger pulse. The breakover voltage is a function of temperature, but throughout a specified operating temperature range exceeds a minimum value specified by the manufacturer. For best utilization of the rectifier, current should be limited and cooling provided to maintain rectifier temperatures in the operating range. Under these

conditions E_r may be taken to be the specified mimimum breakover voltage.

The allowable maximum rms current for S_3 is less easy to determine. Current ratings (average and rms) ordinarily specified apply to controlled rectifiers operating at 50 to 400 cps in conventional power-rectifier circuits. (The rms rating is also the maximum allowable direct current.) These ratings are established to limit internal temperature differences resulting from the conduction of heat through thermal impedances within the rectifier. These temperature differences cannot be reduced by cooling exterior surfaces, and, if excessive, may lead to destructive thermal stress. For rectifier S_3, an rms current rating is desired that limits the temperature differences to the same values allowed in more conventional applications.

Detailed calculation of temperatures throughout the rectifier is a prohibitively difficult task. It is customary instead to calculate a fictitious junction temperature (defined as the uniform rectifier temperature that would give rise to the observed conducting-state voltage drop at low current). All temperature-dependent rectifier properties are supposed to be determined by this temperature, and safe current levels are assumed to be determined by the rise of junction temperature above stud temperature--the temperature of the exterior anode surface through which heat is removed. A second customary assumption is that the distribution of heat generated by power dissipation in the rectifier is invariant. Subject to this assumption,

$$T_j - T_s = R_{Th} P_s \tag{2.38}$$

where T_j and T_s are average junction and stud temperatures, P_s is total average power dissipated in the rectifier, and the junction-to-stud thermal resistance R_{Th} is a fixed parameter of the rectifier.

For controlled rectifier S_3, these assumptions require modification if turn-on is incomplete at the time of peak current. Heat is generated mainly in the turned-on portion of the junction area, and temperatures vary from maximum in this region to minimum in remote parts of the nonconducting area. The thermal resistance relating average temperature rise in the turned-on region to average power

dissipation is greater than R_{Th} because of the more constricted heat-flow path. In view of the shortness of this path, a reasonable (though somewhat conservative) assumption is that thermal resistance is increased in the same ratio as electrical resistance; that is, Eq. 2.38 becomes

$$T_j - T_s = xR_{Th}P_s \tag{2.39}$$

The junction temperature of S_3 varies about its average value T_j, rising to a maximum T_{jp} at the end of each current pulse, and falling to a minimum before the next current pulse. The stud temperature, on the other hand, may be assumed constant for usual pulse-generator repetition frequencies. The excess of T_{jp} over T_j can be estimated with the aid of additional simplifying assumptions--that the outflow of heat from the region in which it is generated is negligible during the brief (order of 10 μs) current pulse, and that the average temperature is midway between the maximum and minimum temperatures. Thus,

$$T_{jp} - T_j = \frac{J_s}{2C_{Th}/x} \tag{2.40}$$

where C_{Th} is the thermal capacity of the heat-generation region in a fully turned-on rectifier.

With the aid of Eqs. 2.31, 2.33, and 2.34, P_s may be written

$$P_s = \frac{J_s}{T_r} = xR_sI^2 + E_dI_{av} \tag{2.41}$$

In conventional rectifier applications, the second term on the right in Eq. 2.41 is often larger than the first. In semiconductor-magnetic pulse generators, however, I_{av}/I is usually so small that E_dI_{av} is negligible. Equations 2.34, 2.39, 2.40 and 2.41 may be solved for I to obtain an approximation for the allowable maximum rms current-handling capability I_r of a controlled rectifier as

$$I_r = \frac{I_{ro}}{x(\sqrt{y}+\sqrt{1+y})\sqrt{z}} \tag{2.42}$$

where

$$I_{ro} = \sqrt{\frac{(T_{jp} - T_s)_m}{R_{Th}R_s}} \tag{2.43}$$

$$y = \frac{2z}{\pi^2} \frac{E_d^2/R_s}{(T_{jp} - T_s)/R_{Th}} \frac{T}{T_r} \tag{2.44}$$

$$z = 1 + \frac{T_r}{2R_{Th}C_{Th}} \tag{2.45}$$

and $(T_{jp} - T_s)_m$ is the maximum allowable value of the junction-to-stud temperature difference.

The current I_{ro} may be considered to be a nominal allowable rms current, and x, $\sqrt{y} + \sqrt{1 + y}$, and $\sqrt{z}$ to be derating factors required to account for partial turn-on, high-duty-ratio operation, and peak junction temperatures in excess of average temperatures, respectively. Of these, only the turn-on factor is ordinarily of major importance. The duty-ratio factor is significant only if T/T_r is so large that $E_d I_{av}$ is important in Eq. 2.41. The peak-temperature factor differs significantly from one only if the repetition frequency is low, and in these applications accurate determination of I_r is ordinarily not necessary--because I is limited to less than its allowable value to secure reasonable pulse-generator efficiency (see Eq. 2.37).

This circumstance is fortunate in view of the difficulty of obtaining values for C_{Th}. Extrapolations of transient-thermal-impedance curves to times less than 100 μs suggested by rectifier manufactures* lead to estimates of $R_{Th}C_{Th}$ of the order of 1 ms. Thus for repetition frequencies above 1 kc the derating factor $\sqrt{z}$ is not likely to be large. The other rectifier parameters required in Eqs. 2.42 and

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* See especially R. Murray, Jr. (editor), Silicon Controlled Rectifer Designers' Handbook, (Semiconductor Div., Westinghouse Elec. Corp., Youngwood, Pa., Ed. 1, 1963), p. 4-9. The time constant (25 μs) given for C_T and a thermal resistance equal to the transient thermal impedance at 100 μs is multiplied by the ratio (about 40) of R_{Th} to this thermal resistance to obtain 1 ms.

2.43 are generally available. The thermal resistance R_{Th} is specified by manufacturers, and the electrical resistance R_s can be determined from a plot of the conducting-state characteristic. The allowable temperature difference $(T_{jp} - T_s)_m$ is dictated by the reliability requirements of the application. Manufacturer's current ratings are based upon an allowable temperature difference of about 60 C; a lower limit may be imposed if extreme reliability is required, especially if extensive temperature cycling is anticipated.

Rms currents as large as I_r are allowable only if cooling is provided to maintain the peak junction temperature within the allowable operating range. Thus, if the allowable junction temperature is 125 C and I_r is determined for $(T_{jp} - T_s)_m = 60$ C, the stud temperature must be maintained at not more than 65 C. Otherwise, I must be limited to a lower value determined from Eqs. 2.42 and 2.43 with $(T_{jp} - T_s)_m$ reduced to the difference between 125 C and the stud temperature that can be maintained. A major reason for limiting the junction temperature is the decrease of forward breakover voltage at high temperatures. Forward voltage is applied to rectifier S_3 only in a brief interval before each current pulse. At this time the junction temperature is below its average value; thus excess peak temperature, if it occurs, does not reduce the blocking capability of the rectifier. This circumstance also is fortunate in view of the uncertainty of peak-temperature values.

Because turn-on times generally increase with rectifier size, the use of a single large rectifier in a high-power pulse generator may lead to poor utilization of the rectifier cross-section--large values of x in Eqs. 2.37 and 2.42 lead to low efficiency and allowable current. An alternate possibility is a bank of smaller (and faster) rectifiers connected in series or parallel--or in a parallel combination of series strings. If all the rectifiers are alike, and if they share voltage and current equally, the allowable voltage of each unit is multiplied by the number in series, and the allowable current by the number in parallel. Hence the power-switching capacity P_r of a bank of n rectifiers is n times the individual-unit capacity. To achieve equal voltage drops across rectifiers in series, equalizing resistors may be connected across the rectifiers--the resistor currents should be

several times the possible imbalance of rectifier forward leakage currents. To achieve equal currents in parallel-connected rectifiers, and to assure that the hold-off interval ends at precisely the same instant in all paths, a multiple-winding hold-off inductor can be provided, with one winding for each string of rectifiers (see Chapter IV, Section B. 3).

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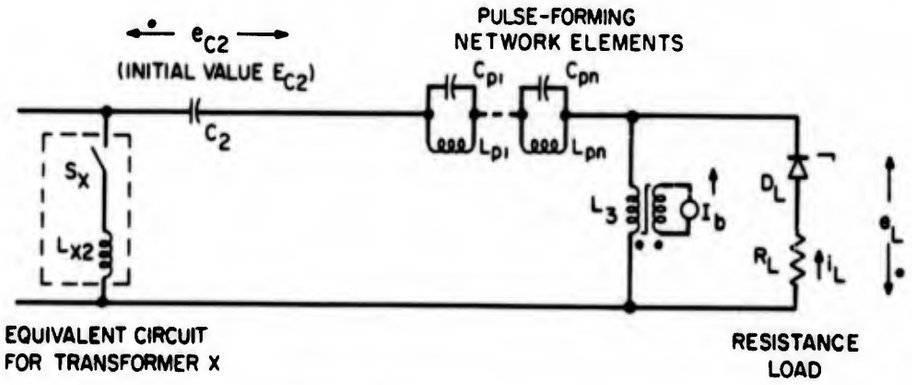
CHAPTER III

CIRCUIT ANALYSIS

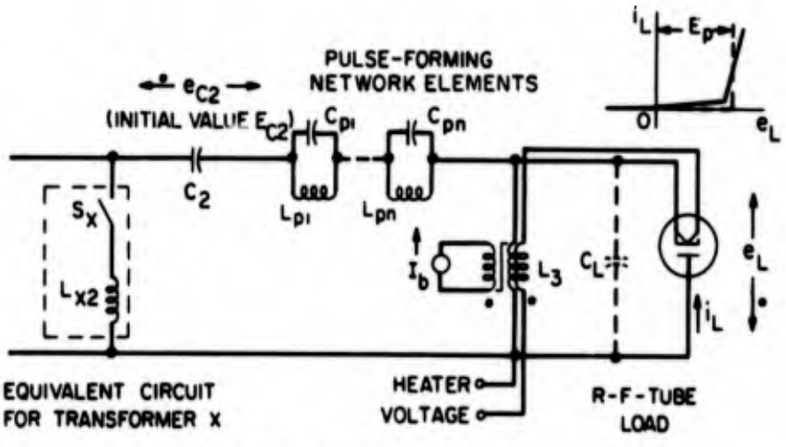
A brief description of circuit functions in the semiconductor-magnetic pulse generator of Fig. 1.3 has been given in Chapter I. In the present chapter, a detailed analysis of each portion of the circuit is presented--in output-to-input order. That is, discharge of the high-voltage capacitance C_2 through the pulse-forming network is considered first, charging of C_2 by discharge of the low-voltage capacitor C_1 next, and charging of C_1 to an accurately regulated voltage last.

A. THE PULSE-FORMING NETWORK

The portion of Fig. 1.3 of first concern is redrawn in more detail in Fig. 3.1; two forms of the circuit appropriate for two types of



(a) Resistance Load



(b) R - F - Tube Load

Fig. 3.1 Pulse-Forming Network and Load

load are shown. The substantial equivalence of either form to a conventional line-pulsing modulator is apparent if transformer X is thought of, as the figure suggests, as a switch S_X in series with L_{X2}, the saturated inductance of the transformer secondary winding. Prior to saturation of X, capacitance C_2 is charged to the voltage E_{C2}; closing of S_X to represent transformer saturation causes C_2 to discharge through the other pulse-forming network elements into the load.

Inductor L_3 saturates during the charging of C_2 to permit passage of a downward charging current. During the output pulse period, L_3 is unsaturated and blocks the full pulse voltage. Thus the function of L_3 is similar to that of the vacuum diode in a conventional line-pulsing modulator; it is called the diode inductor.

The pulse-forming network comprises, strictly speaking, not only the elements so labelled in Fig. 3.1, but also capacitor C_2 and inductor L_{X2}. Because of these elements, it may be convenient to use a Guillemin Type A pulse-forming network[1] formed by connecting parallel resonant circuits in series with C_2 and L_{X2}, as in the figure. Other Guillemin network types, all electrically equivalent, may be used in place of the Type A network. For example, a Type B network (L-C ladder structure) may also be used, with L_{X2} as the input inductor and C_2 split into the shunt capacitors of the ladder. More recently it has been pointed out that a Type E network (L-C ladder structure with equal capacitors and mutual coupling among inductors), slightly modified to provide for uncoupled external inductance equal to L_{X2}, can be used as well. The analysis presented in the remainder of this section presumes the use of a Type A network, with the understanding that any of the alternative and equivalent types can be substituted.

Operation of the pulse generator is dependent in several ways upon the voltage-current characteristics of the load. It is for this reason that slightly different circuits are indicated in Fig. 3.1 for (1) a load having the linear e_L, i_L characteristic of a resistor R_L, and (2) a vacuum-tube r-f generator having a nonlinear characteristic of the general form indicated by the solid line in Fig. 3.1(b). With a resistor

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[1] G.N. Glasoe and J.V. Lebacqz, Pulse Generators (Radiation Laboratory Series, Vol. 5; McGraw-Hill Book Co., N.Y., 1948), pp. 189-257; see especially Fig. 6.22, p. 201.

load, a series avalanche diode [D_L in Fig. 3.1(a)] is desirable to permit a small bias current to develop sufficient reverse voltage to reset L_3. This diode must have a large current rating since it must pass the output current pulse; the voltage rating can be small, of the order of 50 v. With a tube load, the shunt capacitance [C_L in Fig. 3.1(b)] is important because of its effect on the trailing edge of the voltage pulse. In Fig. 3.1 the saturated inductance of L_3 is made to serve as the shunt inductor that speeds the fall of voltage--it is located next to the load and designed to saturate at the end of the desired pulse. This position of L_3 also provides a convenient means of supplying heater current to a grounded-anode r-f tube--a bifilar winding on L_3 can be used, as shown.

Another possibility is a load connected by a pulse transformer to the pulse-generator output terminals. Such a pulse transformer has several disadvantages--its weight and losses add to the weight and losses of the pulse generator, its capacitance adds to C_L, and its leakage inductance L_l adds to L_{X2}. Since pulse-rise-time requirements limit the sum $L_l + L_{X2}$ (see Section A1), an increase in core volume (and hence core loss) of saturable transformer X is needed to provide the reduced value of L_{X2} required if an output transformer is used. Thus, whenever practicable, the step-up ratio of transformer X should be chosen to provide the required output voltage without use of an output transformer. In some high-voltage applications, additional voltage step-up at the output may be unavoidable because of two possible practical limitations: (a) the voltage ratings of the pulse-forming-network capacitors may become excessive; and (b) the pulse-forming-network impedance level may become too high. Undesirable effects of the output transformer may then be minimized by adding a secondary winding to diode inductor L_3, so that it becomes the output transformer.

1. Nominal Pulse Parameters

The Type A network, in common with the other voltage-fed Guillemin pulse-forming networks, is designed to produce a current pulse of specified shape when suddenly connected to a constant-voltage source. This condition applies as an approximation to the circuits of Fig. 3.1. Suppose that:

1. Magnetizing and bias currents in inductors L_2 (see Fig. 1.3) and L_3 are negligible during the pulse.
2. The saturated inductance L_{X2} is strictly constant throughout the pulse.
3. When S_X closes to begin the pulse, no energy is stored in any inductor or capacitance, except C_2.
4. Parasitic circuit elements, including losses and capacitor C_L, can be neglected.
5. The e_L, i_L curve of the load is an idealization of the r-f-tube characteristic in Fig. 3.1(b) represented by the dashed line, with vertical part at $e_L = E_p$.

Nominal pulse shapes predicted on the basis of these assumptions are considered in this section; the effects of deviations from the assumed conditions are discussed in Section A.2 of this chapter.

The charged capacitor C_2 can be considered a battery E_{C2} in series with an uncharged capacitor. Thus, subject to the assumptions made, the circuits of Fig. 3.1 comprise a Type A network connected by the closing of S_X to a constant-voltage source $E_{C2} - E_p$. The Guillemin design procedure for such a network begins with the determination of the Fourier sine series for a periodic current wave in which each half-cycle has the shape specified for the current pulse. From this series, a Type C network comprising a parallel connection of series-resonant circuits is determined; each resonant circuit is selected to pass one of the calculated Fourier components of current when connected suddenly to the constant-voltage source. For a complete (infinite) set of series circuits, then, the total current--if interrupted after the first half-cycle of the fundamental component--is a pulse of the specified form.

In practice, only a finite (and usually small) number of series-resonant circuits can be provided. In consequence, the current pulse obtained only approximates the specified pulse. The number of circuits necessary for a good approximation depends upon the pulse form specified. For a rectangular pulse, no finite number of circuits suffices to remove oscillations at the pulse edges (the Gibbs phenomenon). For

trapezoidal pulses, and more so for pulses with parabolic rise and fall curves, few circuits are needed for an excellent approximation--the exact number required to achieve a specified percentage ripple amplitude o the pulse top depends upon the fraction of the pulse duration occupied by the rise and fall times. Once a nominal pulse shape has been chosen, and the necessary number of series-resonant circuits determined, the Type C network may be changed by standard network-theory procedures to any of several equivalent forms. These are the various voltage-fed Guillemin networks, including the previously mentioned Types A, B and E networks.

In Fig. 3.2 is drawn a nominal current pulse of peak value I_p, total duration τ, and parabolic rise and fall. Associated with this current pulse, for the assumed constant-voltage load, is the rectangular voltage pulse e_L in Fig. 3.2. Interruption of the current i_L at the end of the pulse is provided by saturable transformer X, which begins to reset (S_X in Fig. 3.1 opens) when i_L attempts to reverse.

In order that all the energy stored initially on C_2 may be utilized in the pulse, the circuit parameters must be chosen so that

$$\frac{1}{2} C_2 E_{C2}^2 = \int_0^\tau i_L e_L \, dt = E_p \int_0^\tau i_L \, dt \qquad (3.1)$$

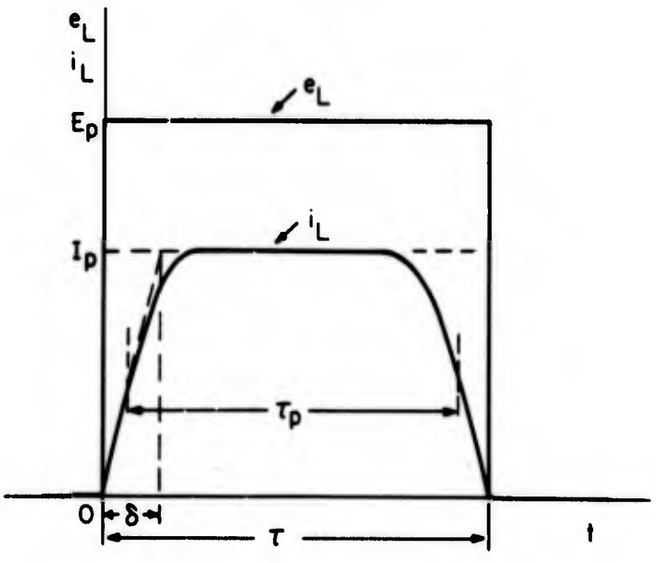


Fig. 3.2 Nominal Pulse Shapes

Since the current integral is the total charge C_2E_{C2} removed from C_2, Eq. 3.1 yields the relation necessary for matching the network to the load,

$$\frac{1}{2} E_{C2} = E_p \tag{3.2}$$

It is convenient to call E_p the nominal pulse voltage and I_p the nominal pulse current, and to define a nominal pulse energy

$$J_p = \frac{1}{2} C_2 E_{C2}^2 \tag{3.3}$$

and a nominal pulse duration τ_p such that

$$I_p \tau_p = \int_0^{\tau} i_L \, dt = C_2 E_{E2} \tag{3.4}$$

By Eqs. 3.2, 3.3, and 3.4,

$$J_p = E_p I_p \tau_p \tag{3.5}$$

and, if

$$P_p = E_p I_p \tag{3.6}$$

and

$$R_L = \frac{E_p}{I_p} \tag{3.7}$$

are the nominal pulse power and nominal load resistance, respectively, then

$$P_p = \frac{J_p}{\tau_p} = I_p^2 R_L = \frac{E_p^2}{R_L} \tag{3.8}$$

At the initial instant (t = 0 in Fig. 3.2) the voltages across the parallel-resonant circuits in Fig. 3.1 are supposed to be zero. Thus the voltage across L_{X2} is $E_{C2} - E_p$, or E_p if the load and network are matched, and the initial slope of i_L is E_p / L_{X2}. This initial slope may be expressed as I_p / δ, where δ is the time required for i_L to rise to its peak value at its initial rate--as indicated in Fig. 3.2. Hence

$$\frac{I_p}{\delta} = \frac{E_p}{L_{X2}}$$

and, by Eq. 3.7,

$$\delta = \frac{L_{X2}}{R_L} \tag{3.9}$$

Equation 3.9 may be compared with the relation

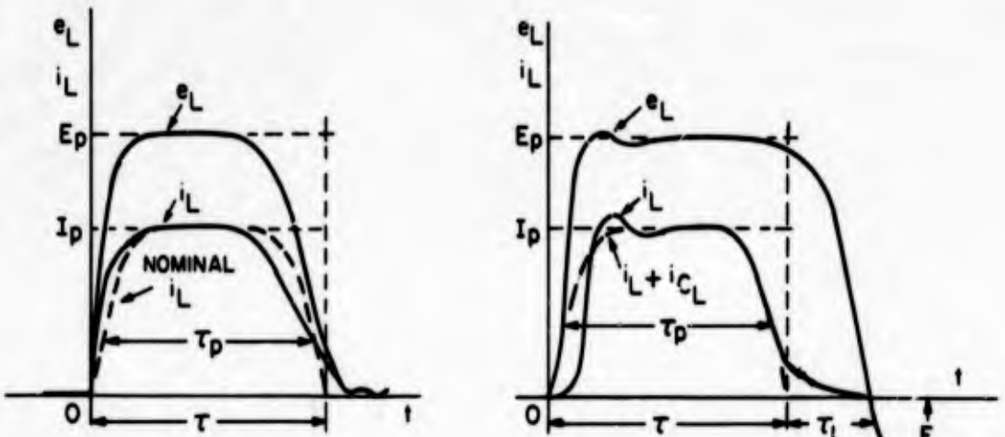
$$\tau_p = 2R_L C_2 \tag{3.10}$$

obtained from Eqs. 3.2, 3.3, 3.5, and 3.7. Thus, for a given nominal load resistance, the pulse duration τ_p depends on C_2, and the rise time (as measured by δ) depends on L_{X2}. Small values of L_{X2} require a large core volume for X; thus steep pulse edges are obtainable only at a price in saturable-transformer weight and core loss.

2. Actual Pulse Shapes

Because the conditions assumed in Section A. 1 are not fully met in a semiconductor-magnetic pulse generator, actual load-current and load-voltage pulses differ noticeably from the nominal pulses of Fig. 3.2. Losses associated with magnetizing and bias currents in L_2 and L_3, as well as losses in other circuit elements, reduce the pulse amplitudes slightly. (Except for C_L, other parasitic elements can usually be ignored, if network components are of high quality.) Stray initial energies alter the pulse shapes, but to some extent can be compensated by minor adjustment of parameter values. These stray energies result because switching of X prior to the pulse period leads to a small initial current in L_{X2}, and (more important) because the relatively rapid charging of C_2 required in a semiconductor-magnetic pulse generator causes some energy storage in network elements other than C_2. In the circuit with resistance load [Fig. 3.1(a)] energy also remains stored in the saturated inductance of L_3 at the end of the charging period. The most important cause of deviations from the nominal pulse shapes, however, is failure of the load to exhibit the assumed constant-voltage characteristic.

For a resistance load R_L, the excess of the nominal rectangular e_L pulse of Fig. 3.2 over the voltage $i_L R_L$ developed across the load by the nominal i_L pulse can be considered a voltage applied to the network to cause alteration of the i_L pulse. The excess voltage comprises positive spikes at the edges of the pulse and, because of the network capacitors, is applied largely across L_{X2}. Thus the actual current pulse rises more rapidly and falls less rapidly than the nominal pulse--as indicated in Fig. 3.3(a). The final portion of



(a) Resistance Load R_L

(b) R - F - Tube Load ($e_L = E_p$ for $i_L = I_p$)

Fig. 3.3 Typical Output-Pulse Shapes

the trailing edge of the pulse is made still less steep, because L_{X2} increases as the end of the saturation region is approached--and becomes infinite when reset begins. Thus adjusting the load resistance to less than the matching value R_L causes a negative charge to be trapped on C_2 at the end of the pulse, but does not produce an overshoot of the output pulse. Because the current pulse rises faster than it falls, energy remains in the network resonant circuits when S_X opens at the end of the pulse, and ringing oscillations persist for a considerable period after the pulse. Inasmuch as S_X is not a perfect open switch, these oscillations appear (greatly reduced in amplitude) in the output waveform.

For an r-f-tube load, when switch S_X first closes only the current in C_L and a small tube current [corresponding to operation below

the breakpoint of the e_L, i_L characteristic in Fig. 3.1(b)] delay the rise of e_L. Thus, if the load provides a voltage $e_L = E_p$ at an operating point for which $i_L = I_p$, the sum of the capacitor current and the electron current i_L conforms very closely to the nominal current pulse--see the dashed line in Fig. 3.3(b). The rise of the i_L pulse is therefore delayed because of current diverted to C_L, and discharge of C_L sustains i_L after the nominal pulse ends. The associated delay in the fall of e_L [(see Fig. 3.3(b)] is the major discrepancy between the nominal and actual pulse shapes when the load is an r-f tube.

To speed the fall of e_L at the end of the pulse, a linear shunt inductor, as used in conventional line-pulsing modulators, can be added to the circuit to build up during the pulse a current that discharges C_L rapidly after $t = \tau$. However, in addition to its usual disadvantages of sloping the top of the current pulse and reducing the output-pulse energy, such an inductor has a special disadvantage in the semiconductor-magnetic circuit. Because L_3 (unlike a vacuum diode) does not conduct when e_L becomes negative after $t = \tau + \tau_1$ in Fig. 3.3(b), it is difficult to obtain sufficient damping of the C_L-shunt-inductor oscillations to prevent subsequent large positive values of e_L.

In a semiconductor-magnetic pulse generator, saturation of L_3 at $t = \tau$ serves the purpose of the linear shunt inductor, but does not entail its disadvantages. At $t = \tau$, switch S_X in Fig. 3.1(b) is opened, and upon saturation of L_3, oscillations begin in the parallel circuit comprising C_L and L_3. Because of damping provided by the tube current and by small currents in the unsaturated transformer X and hold-off inductor L_2, the negative voltage e_L at the end of the first half-cycle of oscillation has a magnitude E [see Fig. 3.3(b)] much less than E_p. Subsequent variation of e_L is determined by the adjustment of bias current (see Section B.1). The time τ_1 required for e_L to fall to zero at the end of the pulse is a quarter-cycle of the L_3, C_L oscillation; that is, if L_3 denotes the saturated inductance of the diode inductor, approximately,

$$\tau_1 = \frac{\pi}{2}\sqrt{L_3 C_L} \qquad (3.11)$$

Of particular interest as measures of pulse-generator performance are the duration and energy of the output pulse. The nominal-pulse parameters τ_p and τ seem as convenient as any in specifying the output-pulse duration. The first is a reasonable, though somewhat vague, measure of the effective duration of the output pulse, and the second specifies the total pulse duration--exclusive of a low-energy "tail". The actual pulse energy is somewhat less than J_p because of losses in the pulse-forming network, and because some energy remains in storage elements at the end of the pulse.

Also of interest is λ_3, the integral of the pulse voltage e_L that must be blocked by L_3. For a resistance load, λ_3 is R_L times the current-pulse integral--which usually exceeds the nominal current integral C_2E_{C2} very slightly. By Eq. 3.4, therefore, λ_3 slightly exceeds $E_p\tau_p$. For the r-f tube load, it is desired that L_3 saturate at $t = \tau$ in Fig. 3.3(b). Thus λ_3 is measured to this time, and is, as the figure indicates, slightly less than $E_p\tau$. Thus, in general,

$$E_p\tau_p < \lambda_3 < E_p\tau \qquad (3.12)$$

the lower limit being approached for a resistance load, and the upper limit for a tube load.

B. THE CHARGING CIRCUIT

To be considered next is the portion of Fig. 1.3 detailed in Fig. 3.4(a). Each trigger pulse applied to controlled rectifier S_3 causes energy stored in low-voltage capacitor C_1 to transfer through the step-up saturable transformer X to the high-voltage capacitor C_2. The resultant energy in C_2 is used as described in Section A to produce an output pulse. The circuit of Fig. 3.4(a) may be completed on the right as in Fig. 3.1(a) for a resistance load, or as in Fig. 3.1(b) for an r-f-tube load.

1. Equivalent Circuit and Waveforms

To simplify the analysis, each saturable inductor or transformer in Fig. 3.4(a) is replaced by an equivalent one-winding inductor in the manner illustrated by Figs. 2.1(b) and 2.1(c). If the load is an r-f tube and if all circuit components are referred to the primary side of transformer X, the circuit of Fig. 3.4(b) results. Inductances L_{l1}

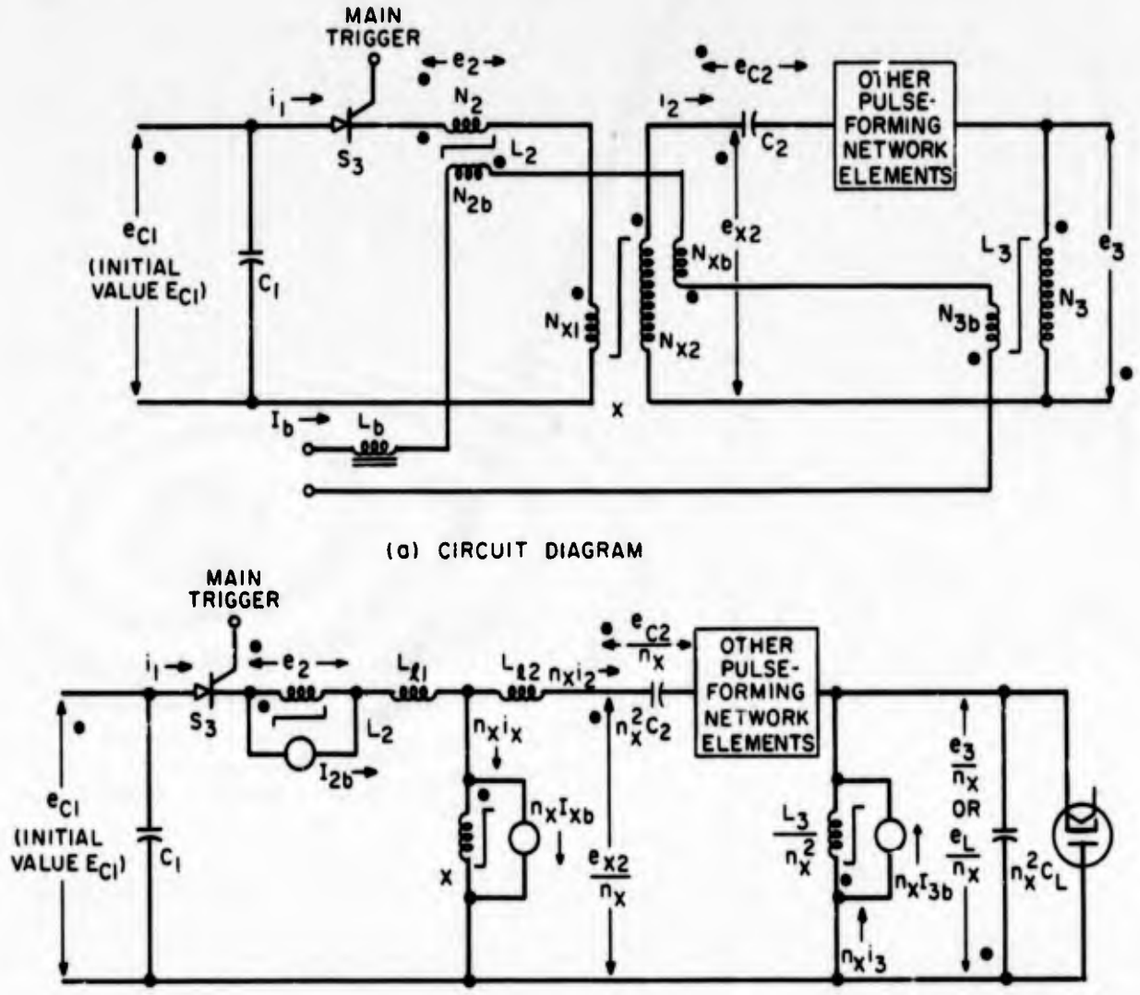


Fig. 3.4 Charging Circuit

and $L_{\ell 2}$ represent primary and secondary leakage inductances of X, both referred to the primary; other leakage inductances are incorporated into the saturated inductances of L_2 and L_3, or into the inductance L_b [see Fig. 3.4(a)] used to maintain the bias current I_b constant. The referred bias currents I_{2b}, I_{Xb}, and I_{3b} are given by

$$I_{2b} = \frac{N_{2b}}{N_2} I_b, \quad I_{Xb} = \frac{N_{Xb}}{N_{X2}} I_b, \quad I_{3b} = \frac{N_{3b}}{N_3} I_b \qquad (3.13)$$

where the N's represent the number of turns in the windings, as marked in Fig. 3.4(a), and the step-up turns ratio n_X of transformer X is

$$n_X = \frac{N_{X2}}{N_{X1}} \qquad (3.14)$$

It is assumed that the circuit attains a steady state, prior to each triggering of S_3, in which (1) capacitor C_1 is charged to the voltage E_{C1}, (2) the voltage across C_2 and the currents in $L_{\ell 1}$ and $L_{\ell 2}$ are zero, and (3) L_2, X, and L_3 are maintained in negative saturation by the bias currents I_{2b}, I_{Xb}, and I_{3b}. The voltage waveforms that ensue if S_3 is triggered at time t = 0 are shown in Fig. 3.5. (More precisely, the trigger pulse begins a fraction of a microsecond before t = 0, and voltage transfers from S_3 to L_2 at t = 0--see Section B.2, Chapter II.)

The first time interval in Fig. 3.5, of duration T_h, is the hold-off interval. In it, negligible voltage drop occurs across the conducting controlled rectifier, and C_1 is negligibly discharged because of the small current flow permitted by L_2. The inductor blocks the entire capacitor voltage E_{C1} and is switched from negative to positive saturation by this voltage. Thus L_2 must be designed to support the volt-time integral.

$$\lambda_2 = E_{C1} T_h \tag{3.15}$$

represented by the line-shaded area in the e_2 waveform.

The controlled-rectifier current i_1 during hold-off is the sum of the bias current I_{2b} and the magnetizing current I_{2m}' for L_2 (the prime is used because the switching time T_h is only a few microseconds--see Section A.1, Chapter II). This current also passes through the transformer primary and, if it exceeds $n_X(I_{Xb} + I_{Xm})$--where I_{Xm} is the transformer magnetizing current referred to the secondary winding--causes the transformer to begin to switch. However, bias currents are too small to charge C_2 appreciably during the hold-off interval; thus regardless of bias-current adjustment, the circuit may be analyzed as if during hold-off the transformer remained in saturation and C_2 received no charge.

The second time interval in Fig. 3.5, the charging interval of duration T, begins when the hold-off inductor saturates. The voltage E_{C1} then causes current to flow in a resonant circuit comprising C_1, $n_X^2 C_2$, the saturated inductances L_2 and L_3/n_X^2, and the leakage inductances $L_{\ell 1}$ and $L_{\ell 2}$. Aside from the effect of losses (caused by series resistances and the transformer current $I_{Xb} + I_{Xm}'$), the current

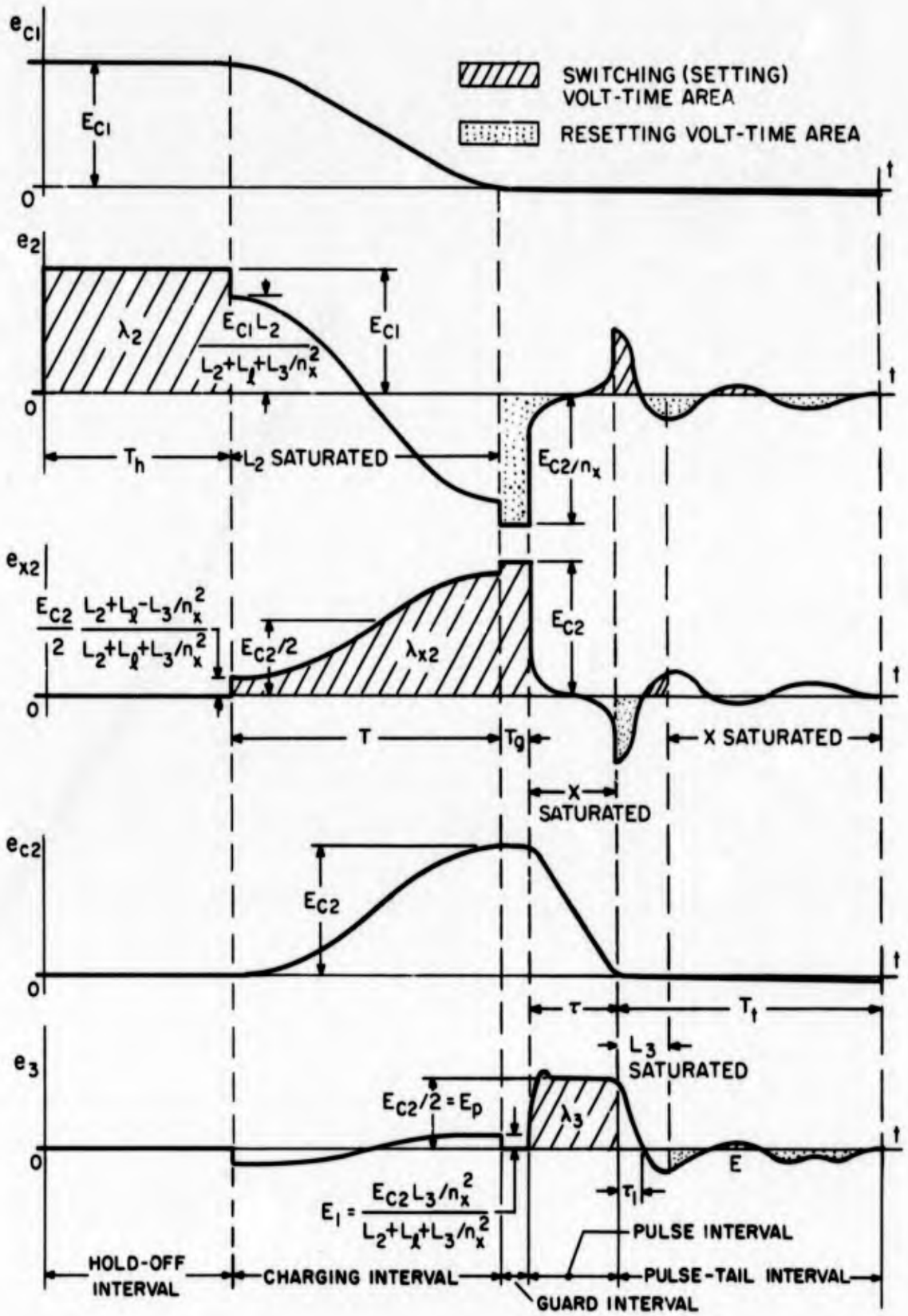


Fig. 3.5 Charging-Circuit Waveforms--R-F-Tube

and voltage variations are sinusoidal. The current-pulse duration corresponds very nearly to a half-cycle of oscillation, because its peak value is tremendously greater than the values $I_{Xb} + I_{2m}'$ and $I_{2b} - I_{2m}'$ at which it begins and ends.

The fraction of the energy originally stored in C_1 that is transferred to C_2 depends on the capacitance ratio. Under the assumption that losses are negligible and the current-pulse duration is precisely a half-cycle, the condition for complete energy transfer is

$$C_1 = n_X^2 C_2 \tag{3.16}$$

Under this condition e_{C1} decreases sinusoidally to zero in the charging interval, as in Fig. 3.5, and e_{C2} increases to

$$E_{C2} = n_X E_{C1} \tag{3.17}$$

The corresponding peak value of i_1 is

$$I_{1p} = E_{C1} \sqrt{\frac{C_1/2}{L_2 + L_\ell + L_3/n_X^2}} \tag{3.18}$$

where

$$L_\ell = L_{\ell 1} + L_{\ell 2} \tag{3.19}$$

is the total leakage inductance of X, referred to the primary, and the charging-interval duration is

$$T = \pi \sqrt{(L_2 + L_\ell + L_3/n_X^2)C_1/2} \tag{3.20}$$

The difference between the capacitor voltages e_{C1} and e_{C2}/n_X is a cosine wave of peak value E_{C1}. This voltage divides among the inductances L_2, L_ℓ, and L_3/n_X^2 to produce the charging-interval portions of the e_2 and e_3 waveforms drawn in Fig. 3.5. The corresponding part of the $e_{X2} = e_{C2} - e_3$ wave is symmetrical about $E_{C2}/2$; thus the integral of e_{X2} over the charging period is $E_{C2}\,T/2$.

The saturable transformer must be designed to support a volt-time integral λ_{X2} at least equal to $E_{C2}\,T/2$ in order that it not saturate before the charging of C_2 is complete. Generally a small excess of

λ_{X2} over E_{C2} T/2 is desirable to provide a short guard interval of duration T_g (see Fig. 3.5). This interval assures that small changes of λ_{X2} (caused by temperature change) or of E_{C2} cannot lead to premature termination of the charging interval. The guard interval is made short because increasing λ_{X2} requires increasing the core volume and core loss of X. A reasonable design objective is zero guard interval at the highest core temperature expected (see Chapter IV, Section B.3).

During the guard interval i_1 equals $I_{2b} - I_{2m}'$, because L_2 is being reset rapidly by the large negative voltage e_2. Similarly, the current $n_X i_X$ [see Fig. 3.4(b)] has the value $n_X(I_{Xb} + I_{xm}')$. If $n_X i_X$ exceeds i_1, the difference current $n_X i_X - i_1$ flows upward through L_3 and the load. If I_{3b} is sufficiently large, L_3 remains in saturation and e_3 falls to zero in the guard interval as indicated in Fig. 3.5. In any event e_3 is small, because the net current available is insufficient to charge C_L significantly during the brief guard interval.

The small guard-interval currents cannot charge capacitors C_1 and C_2 appreciably, nor produce noticeable voltage drops across the leakage inductances of X. Thus the condition $e_3 = 0$ assumed in Fig. 3.5 determines also the other guard-interval voltages shown. In consequence, the volt-time integral that the secondary winding of the transformer must support is the line-shaded area under the e_{X2} curve,

$$\lambda_{X2} = E_{C2}\left(\frac{T}{2} + T_g\right) \tag{3.21}$$

The remaining portions of the waveforms in Fig. 3.5 depend upon the pulse-forming network and the load, as discussed in Section A. The waveforms drawn apply for an r-f-tube load connected as in Fig. 3.4(b). In the pulse interval of duration τ, e_3 is the load voltage pulse e_L of Fig. 3.3(b), and the voltages e_{C2} and e_{X2} are derived from the corresponding pulse of $i_L + i_{CL}$. The integral of this current is the charge taken from C_2 and determines the fall of the e_{C2} wave from E_{C2} to zero. The derivative of the current multiplied by the saturated inductance L_{X2} of the transformer secondary yields the voltage e_{X2}. Since e_3 equals e_L, its integral over the pulse interval (the line-shaded area in Fig. 3.5) is given by Eq. 3.12, Section A.2, and L_3 must be designed to support the volt-time integral

$$\lambda_3 = E_p \tau \tag{3.22}$$

Since L_2 begins the pulse interval with a small degree of reset (represented by the guard-interval dot-shaded area of the e_2 wave in Fig. 3.5), it limits the current i_1 through C_1 to a small value and e_{C1} remains substantially zero during the pulse. The voltage e_2 is therefore the negative of the transformer primary voltage--which equals e_{X2} times the ratio of the mutual inductance of the saturated transformer to L_{X2}. Thus during the pulse the operating point of L_2 traces a minor reset-and-set B-H loop, with negligible net change in degree of reset. (The integral of the transformer voltage is determined by the net change of $i_L + i_{CL}$, which is zero.)

The difference between e_{X2} and $e_{C2} - e_3$ is absorbed by oscillatory voltages developed across the resonant circuits of the pulse-forming network. These oscillations are started by the steep leading edge of the current pulse, and ideally are terminated by the trailing edge. In practice, the current pulse is never precisely the same as the nominal current pulse (see Sections A.1 and A.2), and quenching of the oscillations at the end of the pulse period is not complete. The residual oscillations have significant effect on waveforms after the end of the pulse period. For purposes of Fig. 3.5, however, these effects are ignored; the figure is drawn as though not only the energy in C_2 but also that in all other elements of the pulse-forming network were zero at the end of the pulse.

The pulse ends and the pulse-tail interval of duration T_t begins when the operating point of transformer X moves, with decreasing output-pulse current, from saturation into reset. At this time L_3 saturates and discharges the load capacitor C_L; thus e_3 decreases from E_p to -E in a damped half-cycle oscillation (see Section A.2). At the end of the half-cycle, L_3 begins reset, and simultaneously the transformer re-enters positive saturation. (If no energy remains in the network resonant circuits, the pulse-tail dot-shaded and line-shaded areas of the e_{X2} wave are equal, because the corresponding e_3 areas are equal--L_3 begins and ends the half-cycle at its threshold of saturation.) Thus the oscillatory

discharge current transfers from L_3 to the transformer secondary as it reverses sign. The transformer may remain saturated, and L_3 in reset, throughout subsequent cycles of the oscillation (as indicated in the figure), or X and L_3 may saturate alternately, depending on the magnitude of the oscillatory current and the adjustment of bias currents. When X is saturated, the waveform of e_3 is not that of a damped sinusoid because resonant circuits of the pulse-forming network, as well as C_L and L_{X2}, influence the current. It is in this period that residual resonant-circuit energies not accounted for in Fig. 3.5 affect the waveforms most noticeably.

If a linear resistor is substituted for the r-f tube load, waveforms prior to the pulse interval are almost as drawn in Fig. 3.5. The major change is that, if L_3 is a substantial fraction of the total charging-circuit inductance, division of the charging current between L_3 and the load leads to a residual current in L_3 at the end of the charging period. This current maintains voltage across the load during the guard interval. Moreover, energy remaining in the saturated inductance L_3 at the end of the guard interval influences the shape of the output pulse (see Section A.2).

Waveforms during the pulse period, for a resistor load, are derived from the e_L and i_L pulses of Fig. 3.3(a). For the circuit of Fig. 3.1(a), L_3 must be designed to support a λ_3 at least equal to $E_p\tau_p$ (Eq. 3.12). If λ_3 is made equal to $E_p\tau$ (Eq. 3.22), L_3 does not saturate at the end of the pulse, and the pulse terminates in the manner described in Section A.2.

The waveforms in Fig. 3.5 span only a small fraction of the total period between trigger pulses. The remainder of the period is available to return the circuit to its initial state, in preparation for the next trigger pulse. Details of this resetting operation are discussed in Section B.3 and in Appendix A. Note here, however, that controlled rectifier S_3 does not turn off at the end of the charging interval. It is inductor L_2, not the rectifier, that prevents reversal of i_1. Because of the bias current I_{2b}, the inductor maintains a small forward current in S_3 until it is completely reset, long after the end of the period covered by Fig. 3.5.

2. Power and Energy Ratings

The volume, weight, and cost of a semiconductor-magnetic pulse generator depend upon the power and energy ratings of its components. Thus it is important to establish required values of these ratings for components in the charging circuit of Fig. 3.4(a).

For capacitors C_1 and C_2, the quantity of interest is the peak stored energy--that is, the nominal pulse energy J_p for C_2 and the charging-circuit energy

$$J_c = \frac{1}{2} C_1 E_{C1}^2 \tag{3.23}$$

for C_1. (Losses in the charging circuit make J_c somewhat greater than J_p.) Inasmuch as the dielectric volume of a capacitor is, for fixed voltage gradient, proportional to capacitance and to the square of voltage rating, the peak stored energy is the major determinant of capacitor volume and weight. The allowable stored energy per unit volume is determined by the dielectric material, by the working voltage, and by dielectric and conductor requirements imposed by operating conditions. Very high voltage levels, voltage levels less than about 1,000 v, short charging or discharging times, and high repetition frequencies lead to small allowable values of stored energy per unit volume.

For controlled rectifier S_3, the quantity of interest is the power-switching capacity P_r defined in Section B.4 of Chapter II. By Eq. 2.35 and 2.36 of that section, the required value of P_r is

$$P_r = \frac{\pi J_c}{\sqrt{2}\sqrt{TT_r}} \tag{3.24}$$

This equation determines the size and number of controlled-rectifiers needed in the S_3 position--provided the resulting rectifier losses are not excessive. If the repetition frequency is low, more or larger rectifiers may be necessary to maintain high-pulse-generator efficiency (see Eq. 2.37).

For transformer X, the quantity of interest is the energy-switching capacity defined in Section A.2 of Chapter II,

$$J_X = \frac{\lambda_{X2}^2}{2L_{X2}} \tag{3.25}$$

where λ_{X2} is the volt-time integral supported by the secondary winding, and L_{X2} is the secondary saturated inductance. By Eq. 2.11, J_X determines the volume of magnetic material required in the transformer core. The total transformer volume and weight also are largely determined by J_X, but depend also on insulation requirements.

The required value of J_X can be determined by evaluating λ_{X2} and L_{X2} in Eq. 3.25. For a lossless charging circuit, Eq. 3.21 determines λ_{X2}, and $J_p = J_c$. Thus, by Eqs. 3.3, 3.9, and 3.10,

$$J_X = J_c \frac{\tau_p}{2\delta} \left(\frac{T + 2T_g}{\tau_p} \right)^2 \tag{3.26}$$

For a charging circuit with losses, Eq. 3.26 is only approximately correct, but the error is small if the losses are not excessive. The charging-circuit energy J_c rather than the smaller nominal pulse energy J_p is used in Eq. 3.26 to ensure that the calculated J_X is never less than the true required energy-switching capacity of the transformer. Note that J_X is determined not only by J_c but also by an output-pulse shape factor $\tau_p/2\delta$ and by the square of the pulse-compression ratio $(T + 2T_g)/\tau_p$.

The energy-switching capacities required in the hold-off and diode inductors,

$$J_2 = \frac{\lambda_2^2}{2L_2} \tag{3.27}$$

and

$$J_3 = \frac{\lambda_3^2}{2L_3} \tag{3.28}$$

are not completely determined by the charging-circuit requirements. Individual values of λ_2 and λ_3 are specified by relations in Section B.1, but only the sum of the inductances L_2 and L_3/n_X^2 is fixed. By Eq. 3.20

$$L_2 + \frac{L_3}{n_X^2} = \frac{2T^2/\pi^2 - L_\ell C_1}{C_1} \tag{3.29}$$

The term $L_\ell C_1$ may usually be neglected in comparison with $2T^2/\pi^2$. For ordinarily close coupling of the primary and secondary transformer windings, a reasonable estimate of L_ℓ is L_{X2}/n_X^2. The corresponding value of $L_\ell C_1$ is (by Eqs. 3.9, 3.10, and 3.16),

$$\frac{L_{X2}}{n_X^2} C_1 = R_L \delta C_2 = \frac{\delta \tau_p}{2}$$

Typically $\sqrt{\delta \tau_p}$ is less than T/10, and $L_\ell C_1$ is at most a few percent of $2T^2/\pi^2$.

Equations 3.27 and 3.28 may be used to eliminate L_2 and L_3 from Eq. 3.29, and Eqs. 3.15 and 3.22 may then be employed to evaluate λ_2 and λ_3. If the approximations $E_p = E_{C2}/2 \approx n_X E_{C1}/2$ and $L_\ell C_1 \approx 0$ are introduced, the relation obtained is

$$\frac{T_h^2}{J_2} + \frac{(\tau/2)^2}{J_3} = \frac{2T^2/\pi^2}{J_c} \tag{3.30}$$

Any combination of J_2 and J_3 values that satisfies Eq. 3.30 meets both the blocking interval requirements (set by λ_2 and λ_3) and the conducting-interval requirement (that the duration of the charging interval be T).

One possibility is to select J_2 and J_3 so that the sum $J_2 + J_3$ is a minimum--and hence the total core volume of the hold-off and diode inductors is a minimum. Equation 3.30 requires that changes in J_2 and J_3 occur so that

$$\frac{T_h^2}{J_2^2} dJ_2 + \frac{(\tau/2)^2}{J_3^2} dJ_3 = 0$$

At the point of minimum $J_2 + J_3$, however,

$$dJ_2 + dJ_3 = 0$$

and therefore, for minimum total core volume,

$$\frac{J_2}{J_3} = \frac{T_h}{\tau/2} \tag{3.31}$$

or, because of Eqs. 3.15, 3.22, 3.27 and 3.28

$$\frac{J_2}{J_3} = \frac{\lambda_2}{\lambda_3/n_X} = \frac{L_2}{L_3/n_X^2} = \frac{T_h}{\tau/2} \tag{3.32}$$

Equations 3.30 and 3.31 yield

$$\left.\begin{aligned} J_2 &= \frac{\pi^2}{2} J_c \frac{(T_h + \tau/2)T_h}{T^2} \qquad (3.33) \\ J_3 &= \frac{\pi^2}{2} J_c \frac{(T_h + \tau/2)\tau/2}{T^2} \qquad (3.34) \end{aligned}\right\} \text{(For minimum } J_2 + J_3\text{)}$$

Many applications require a diode-inductor saturated inductance less than the value provided by this minimum-core-volume condition. Reduced L_3 may be necessary (1) to provide faster fall of voltage at the end of the output pulse, or (2) to reduce the output voltage that occurs during the charging interval--see the e_3 waveform in Fig. 3.5. For an r-f-tube load with shunt capacitance C_L, the voltage fall time, shown as τ_1 in Figs. 3.3(b) and 3.5, is equal to $\pi\sqrt{L_3 C_L}/2$ (see Eq. 3.1). Evaluating L_3 by means of Eqs. 3.29 and 3.32 and neglecting $L_\ell C_1$ yields

$$\tau_1 = \frac{T}{2}\sqrt{\frac{\tau}{T_h + \tau/2}}\sqrt{\frac{C_L}{C_2}} \qquad \text{(For minimum } J_2 + J_3\text{)} \tag{3.35}$$

The output voltage during the charging period has a peak value

$$E_1 = E_{C2} \frac{L_3/n_X^2}{L_2 + L_\ell + L_3/n_X^2}$$

as marked on the e_3 curve in Fig. 3.5. Hence, if L_ℓ is neglected and the L_2/L_3 ratio of Eq. 3.32 is used,

$$E_1 = E_p \frac{\tau}{T_h + \tau/2} \qquad \text{(For minimum } J_2 + J_3\text{)} \tag{3.36}$$

If either τ_1 or E_1, given by Eqs. 3.35 and 3.36 is unacceptably large, a smaller value can be had by reducing L_3 to α times its minimum-core-volume value. (A simultaneous increase of L_2 must be provided to maintain $L_2 + L_3/n_X^2$--and hence T--constant.) The value of α is chosen small enough so that the new values of τ_1 and E_1,

$$\tau_1 = \frac{T}{2} \sqrt{\frac{\alpha\tau}{T_h + \tau/2}} \sqrt{\frac{C_L}{C_2}} \tag{3.37}$$

and

$$E_1 = E_p \frac{\alpha\tau}{T_h + \tau/2} \tag{3.38}$$

are acceptable. Because $L_2 + L_3/n_X^2$ is maintained constant, Eq. 3.30 is still satisfied, and the required energy-switching capacities become

$$J_2 = \frac{\pi^2}{2} J_c \frac{(T_h + \tau/2) T_h}{T^2[1 + (1-\alpha)\tau/2T_h]} \tag{3.39}$$

and

$$J_3 = \frac{\pi^2}{2} J_c \frac{(T_h + \tau/2)\tau/2}{\alpha T^2} \tag{3.40}$$

According to Eq. 2.11, the required core volumes for the saturable transformer and inductor can be had by dividing the energy-switching capacities of Eqs. 3.26, 3.39, and 3.40 by the energy-capacity figure of merit $2B_s^2/\mu_e$. Similarly, Eq. 2.17 yields the magnetizing currents

$$I_{Xm} = \frac{1}{2} \frac{\mu_e H_c}{B_s} Q_2 \frac{T + 2T_g}{\delta\tau_p} \tag{3.41}$$

$$I_{2m} = \frac{\pi^2}{4} \frac{\mu_e H_c}{B_s} Q_1 \frac{T_h + \tau/2}{T^2[1 + (1-\alpha)\tau/2T_h]} \tag{3.42}$$

and

$$I_{3m} = \frac{\pi^2}{4} \frac{\mu_e H_c}{B_s} Q_2 \frac{T_h + \tau/2}{\alpha T^2} \tag{3.43}$$

where Q_1 and Q_2 denote the peak capacitor charges $C_1 E_{C1}$ and $C_2 E_{C2}$, respectively, and the approximation $J_c = J_p$ is used.

An idea of the relative volumes of magnetic material required in the transformer and inductors may be gained by making simplifying approximations in Eqs. 3.26, 3.39 and 3.40. To this end, neglect $2T_g$ in comparison with T and $\tau/2$ relative to T_h, and assume $\tau_p/\pi^2\delta$ to be one. If the transformer and inductors utilize cores of the same material, the magnetic-material volumes V_X, V_2, and V_3 of the transformer, hold-off inductor, and diode inductor, respectively, are proportional to J_X, J_2, and J_3. Thus the simplified equations yield

$$V_2 \approx 2\alpha \frac{T_h}{\tau} V_3 \tag{3.44}$$

and

$$V_X \approx \left(\frac{T^2}{\tau_p T_h}\right)^2 V_2 \tag{3.45}$$

Typically α is somewhat less than one, and T_h/τ is somewhat greater, so that V_2 ranges from about equal to V_3 to a few times larger. In contrast, T is usually larger that T_h and much larger than τ_p, so that V_X is many times larger than V_2 or V_3.

A similar simplification of Eqs. 3.41, 3.42, and 3.43 yields the approximate magnetizing-current relationships,

$$\frac{I_{2m}}{n_X} \approx \alpha I_{3m} \tag{3.46}$$

and

$$I_{Xm} \approx 2 \frac{T^3}{\tau_p^2 T_h} \frac{I_{2m}}{n_X} \tag{3.47}$$

Thus, if all currents are referred to the same side of the transformer, the magnetizing currents of the diode and hold-off inductors are equal for $\alpha = 1$, and the transformer magnetizing current is greater than either in about the ratio of core volumes.

3. Resetting Modes

Section B. 1 has described the operation of the charging circuit from the time of triggering controlled rectifier S_3 to the end of the output pulse. After the pulse, and before the next triggering of S_3, the saturable inductors and transformer must be reset to negative saturation, charges acquired by C_2 must be removed, and capacitor C_1 must be recharged to the voltage E_{C1}.

To avoid possible damage to the controlled rectifier in the first cycle of operation, bias currents should be established before trigger pulses are applied to S_3. For this purpose, it is sufficient that the bias currents satisfy

$$I_{2b} > I_{2mo}, \quad I_{3b} > I_{3mo}, \quad I_{Xb} > I_{Xmo} \tag{3.48}$$

where I_{2mo}, I_{3mo}, and I_{Xmo} denote inductor and transformer magnetizing currents corresponding to the d-c coercive force (see Sections A. 1 and A. 4 of Chapter II). These bias currents also suffice if the controlled rectifier is triggered at a very low repetition rate, but considerably larger bias currents are generally needed to accomplish reset in the time available at repetition frequencies of practical interest. A larger value of I_{2b} may also be required to speed the turn-on of S_3 during the hold-off interval. Bias currents too small to provide complete reset prior to each trigger pulse may lead to excessive losses, to wild variations in the output-pulse amplitude and timing, or even to destruction of controlled rectifiers. On the other hand, indiscriminate increase of bias currents does not necessarily lead to rapid resetting, and may needlessly increase the pulse-generator losses.

Bias ampere-turns $N_b I_b$ applied to any saturable inductor (see Fig. 2. 10) produce a main-winding reset current I_r that gives rise to voltages across other elements in the saturable-inductor circuit. The principal pulse-generator bias-circuit design problem is to assure that, for each saturable element, $N_b I_b$ is large enough so that the resulting voltage that appears across the main winding is sufficient to reset the core in the time allowable. The problem also involves avoiding, as far as possible, energy-wasting set-and-reset operations, and excessively fast resetting. Further, it involves obtaining a desired turn-on current for S_3 in the hold-off interval, and selecting I_b so that N_b is

not so high for any inductor that excessive voltage is developed in the bias circuit when the saturable-inductor main winding is supporting a large switching voltage.

Analysis of the resetting operation is difficult because it may occur in a great variety of different modes, depending not only on bias current adjustments but also on small residual voltages that may remain stored on C_1 and C_2 at the end of the output pulse. Each mode presents a separate and often tedious analysis problem. Moreover, the numerical results obtained are of limited utility because of their dependence on the uncertain residual capacitor voltages. The practical procedure is unquestionably to make final bias-current adjustments experimentally (see Chapter IV, Section B.3, "Bias Circuit and Bias Inductor"). A detailed analysis of one particular resetting mode, plus a discussion of other possible modes for the case where the load is an r-f tube, is presented in Appendix A. This painstaking treatment has been appended to this report, not so much to present equations for reset times and losses, as to provide an understanding of the way in which reset is achieved and of the general principles that should be kept in mind when making experimental adjustments.

4. The Bias Circuit

In Fig. 3.4, the bias circuit comprises the bias windings on two saturable inductors and the saturable transformer, a bias inductor L_b, and a d-c power supply capable of forcing an average current I_b through the circuit d-c resistance. The bias inductor absorbs voltages developed across the bias windings of the three saturable inductors during the pulse-generation cycle; its function is to keep I_b constant within prescribed limits.

Two important design parameters of inductor L_b are its inductance and the maximum energy it must store. Refer to Figs. 3.4(a) and 3.5. In the interval T_p from the start of the trigger to the end of the output pulse, the volt-time integral λ_b that tends to increase I_b is

$$\lambda_b = \int_{T_p} \left(\frac{N_{23}}{N_2} e_2 + \frac{N_{Xb}}{N_{X2}} e_{X2} + \frac{N_{3b}}{N_3} e_3 \right) dt$$

By Eq. 2.10, this can be written as

$$\lambda_b = \frac{I_{2r} + I_{2m}}{I_b}\left(\lambda_2 - E_{C1}T_g\right) + \frac{I_{Xr} + I_{Xm}}{I_b}\lambda_{X2} + \frac{I_{3r} + I_{3m}}{I_b}\lambda_3$$

If all the saturable inductors use the same core material, then Eqs. 2.17, 3.2, and 3.5 combined with the above lead to

$$\lambda_b = \frac{1}{I_b}\left[J_p \frac{\tau I_{3r} + 2(T_h - T_g)I_{2r}/n_X + (T + 2T_g)I_{Xr} - T_g I_{2m}/n_X}{I_p \tau_p} + \frac{\mu_e H_c}{B_s}(J_2 + J_3 + J_X)\right] \tag{3.49}$$

If the current is allowed to change during the pulse generation cycle by a total amount $\Delta I = \beta I_b$, then

$$L_b = \frac{\lambda_b}{\Delta I} = \frac{\lambda_b}{\beta I_b} \tag{3.50}$$

The peak stored energy in L_b is

$$\frac{1}{2}L_b I_b^2(1 + \beta/2)^2 \approx \frac{1/\beta + 1}{2} I_b \lambda_b \tag{3.51}$$

To the extent that the bias current remains constant, there is no interchange of power between the main and bias windings, and the total bias-circuit loss is $R_b I_b^2$, where R_b is the d-c resistance of the bias circuit. The varying voltage applied to L_b and the associated change ΔI of I_b causes some core loss in L_b. Energy to supply this loss is derived from the pulse-generator circuit--however, this loss is usually very small.

5. Pulse Jitter

There are three causes of time jitter in the output pulse train of the semiconductor-magnetic modulator: (a) jitter in the trigger-pulse source; (b) pulse-to-pulse variations in the turn-on time of S_3; and (c) fluctuations in the delay time $T_d = T_h + T + T_g$.

Careful selection or design of the trigger-pulse source is the obvious step to minimize jitter arising from (a). Turn-on time variations in S_3 are minimized when the trigger-current pulse satisfies

the requirements (short rise time and large amplitude) for fast turn-on time (see Chapter II, Section B.3). Jitter in S_3 turn-on time can be expected to be on the order of 5 ns rms or less.

The major cause of jitter in the output pulse train is (c). To the extent that the energy-regulator circuit can maintain E_{C1} constant in the face of prime-power-source voltage variations, jitter in T_d can be kept small.

Note that, by Eqs. 3.15 and 3.21,

$$T_d = T_h + T + T_g = \frac{\lambda_2}{E_{C1}} + \frac{T}{2} + \frac{\lambda_{X2}}{n_X E_{C1}}$$

Differentiation yields

$$dT_d = -\left(\frac{\lambda_2}{E_{C1}} + \frac{\lambda_{X2}}{n_X E_{C1}}\right) \frac{dE_{C1}}{E_{C1}}$$

and

$$dT_d = -(T_d - T/2) \frac{dE_{C1}}{E_{C1}} \qquad (3.52)$$

Equation 3.52 provides a means of estimating the regulation $\frac{dE_{C1}}{E_{C1}}$ required at C_1 to restrict the jitter to dT_d. For example, assume that a modulator with $T_h = 3\ \mu s$, $T = 6\ \mu s$, and $T_g = 0.5\ \mu s$ must exhibit no more than $dT_d = 0.01\ \mu s$ jitter. Then the regulation required at C_1 is, by Eq. 3.52,

$$\left|\frac{dE_{C1}}{E_{C1}}\right| = \frac{0.01}{3 + 6 + 0.5 - 3} \approx 0.15 \text{ percent}$$

Amplitude jitter in the output pulse will be the same as that in E_{C1}; if E_{C1} is closely regulated to avoid time jitter, the amplitude jitter will be negligibly small.

C. THE VOLTAGE REGULATOR

The final portion of the circuit of Fig. 1.3 to be considered in detail is the voltage regulator, shown in essential form in Fig. 3.6. A start-trigger pulse turns on controlled rectifier S_2, so that C_1 resonantly charges from C_0 and the unregulated d-c power supply. When the voltage e_{C1} on C_1 reaches the desired regulated value E_{C1},

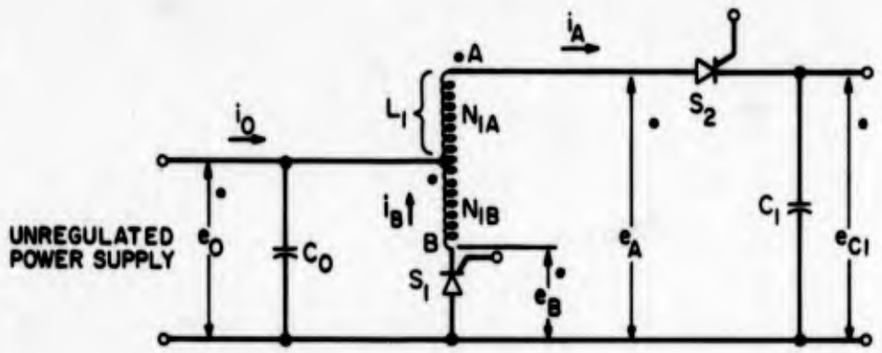


Fig. 3.6 Basic Voltage-Regulator Circuit

a level-sensing circuit (not shown) delivers a stop-trigger pulse to S_1, thereby connecting the lower end of winding B to ground. This connection impresses the power-supply voltage e_o across winding B, so that the voltage across winding A becomes N_{1A}/N_{1B} = n times e_o and e_A becomes $(n + 1)e_o$. Choice of n so that this value is less than E_{C1} causes a reverse voltage across S_2; conduction in S_2 ceases and the voltage E_{C1} remains across C_1 until the main trigger pulse initiates the charging-circuit operations described in Section B. Energy stored in L_1 returns to C_0 through current flow in winding B; the cycle is complete after the current i_B ceases to flow in winding B.

Of concern here are the development of the conditions required for regulation to occur, the determination of the effect of leakage inductance between windings A and B on regulation, the establishment of stability criteria to be satisfied in the design of the associated power supply, and the magnitudes of peak voltages and rms currents experienced by the circuit components. These points will be established by considering first the basic circuit of Fig. 3.6, and second, combination of that circuit with an unregulated power supply.

1. The Basic Regulator Circuit

Throughout the analysis that follows, it is assumed that C_0 of Fig. 3.6 is large relative to C_1, so that e_0 varies but little from the constant value E_0 during each regulation cycle. The waveforms of Fig. 3.7 are keyed to the basic circuit of Fig. 3.6; the time origin in Fig. 3.7 coincides with the leading edge of the start-trigger pulse. As discussed in Section B of this chapter, and in Appendix A, a negative

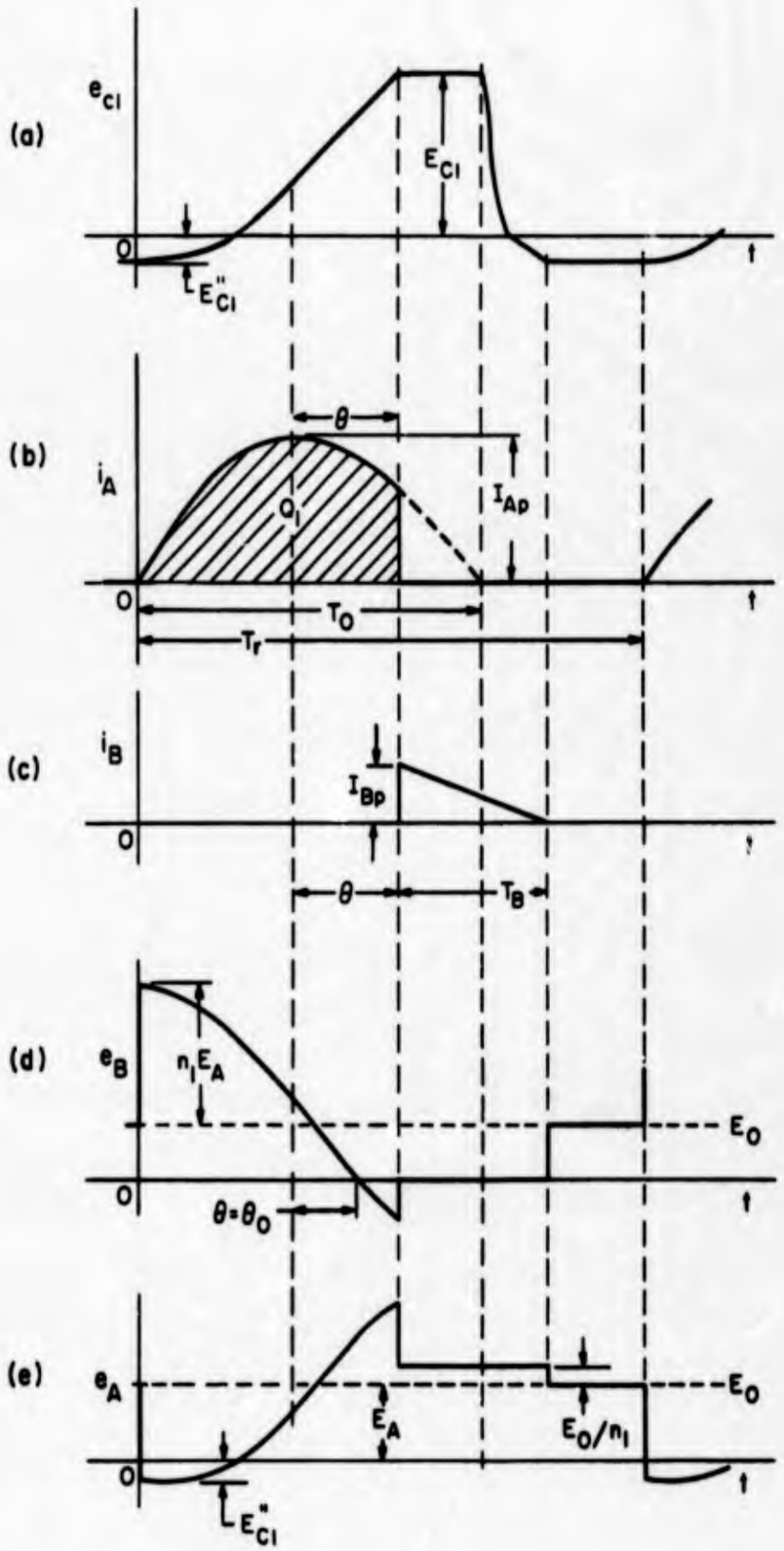


Fig. 3.7 Voltage-Regulator Waveforms

voltage builds up across C_1 during the saturable-inductor reset interval. For this reason, $e_{C1} = -E_{C1}''$ in Fig. 3.7(a) at t = 0. Define $\gamma = E_{C1}''/E_{C1}$ (γ is always positive for this circuit). The charge transferred from the power supply in charging C_1 from $-E_{C1}''$ to the regulation value E_{C1} is therefore

$$Q_o = (1 + \gamma)C_1 E_{C1} \tag{3.53}$$

The charge Q_o is represented by the shaded portion of the current waveform i_A through winding A, Fig. 3.7(b). Note that i_A is the result of abrupt truncation by regulator action of a train of half-sine pulses of duration $T_o = \pi\sqrt{L_1 C_1}$. The peak value of i_A is

$$I_{Ap} = \frac{\pi}{T_o} \frac{Q_o}{1 + \sin\theta} \tag{3.54}$$

where, as indicated in Fig. 3.7, θ is measured from the time of peak current.

A current ramp i_B [Fig. 3.7(c)] results each time winding B is switched across E_o to interrupt i_A. The ramp duration is

$$T_B = \frac{n_1}{\pi} T_o \frac{1 + \gamma}{1 - \gamma \sin\theta} \cos\theta \tag{3.55a}$$

The peak value of i_B occurs at the start of the ramp and is

$$I_{Bp} = \frac{\pi}{n_1 T_o} \frac{\cos\theta}{1 + \sin\theta} = \frac{I_{Ap}}{n_1} \cos\theta \tag{3.55b}$$

Conditions for Regulation

Three conditions must be satisfied if the circuit is to operate as described above and yield close regulation of the voltage to which C_1 is charged. These are:

Condition 1 -- Range of θ. Controlled rectifier S_1 cannot turn on until the voltage at Point B in Fig. 3.6 is negative with respect to ground. As shown in Fig. 3.7(d), e_B becomes zero for $\theta = \theta_o$, where

$$\sin\theta_o = \frac{1}{n_1(1 + \gamma) + \gamma} \tag{3.56a}$$

Also, S_2 cannot conduct beyond the first half-cycle of the i_A sinusoid. Thus,

$$\theta_o < \theta < \pi/2$$

and corresponding to these θ limits,

$$E_{o\,min} = \frac{1-\gamma}{2} E_{C1} \qquad (3.56b)$$

(to ensure that C_1 can be charged to a voltage as high as E_{C1}) and

$$E_{o\,max} = \frac{E_{C1}}{1 + 1/n_1} \qquad (3.56c)$$

(to ensure that the charging process can be interrupted at a voltage as low as E_{C1}). The ratio a of the allowable extremes of E_o is called the regulation range,

$$a = \frac{E_{o\,max}}{E_{o\,min}} = \frac{2}{(1+1/n_1)(1-\gamma)} \qquad (3.56d)$$

For reasonable values of n_1 and γ, $a \approx 2$.

Condition 2 -- Limits for T_o The regulation cycle of operation described above must be completed within the repetition period T_r. That is,

$$T_o(\frac{1}{2} + \frac{\theta}{\pi}) + T_B < T_r \quad \text{(for all } \theta) \qquad (3.57a)$$

As θ decreases from $\pi/2$ toward $\theta = \theta_o$, the duration of the i_A pulse decreases from T_o to $T_o(1/2 + \theta_o/\pi)$, whereas the i_B-pulse duration increases from zero to $T_o \cot\theta_o$. In consequence, the sum, which is the left-hand member of Eq. 3.60, passes through a maximum for some θ, and this maximum must be less than T_r. For γ small, the maximum occurs for $\sin\theta$ between $\sin\theta_o$ and $\sin\theta_o + \gamma$, and is such that Eq. 3.57(a) becomes

$$\frac{T_r}{T_o} > \frac{1}{2} + \frac{1}{\pi}\left[\frac{1}{(1+\gamma^2)\sin\theta_o} + \frac{1}{2}(1-\gamma^2)\sin\theta_o + \gamma\right] \qquad (3.57b)$$

In particular, if $\gamma = 0$, the maximum occurs for $\theta = \theta_o$, and Eq. 3.57(b) simplifies to

$$\frac{T_r}{T_o} > \frac{1}{2} + \frac{n_1 + 1/2\, n_i}{\pi} \qquad (3.57c)$$

Condition 3 -- C_o Requirement. A minimum limit must be placed on C_o in order that e_o may be maintained almost constant (over a repetition period) for the preceding analysis to be valid. Analysis of the circuit becomes prohibitively complex if this assumption is not made. The requirement that the change in e_o be very small relative to the mean value E_o may be written

$$\frac{\Delta Q}{C_o} \ll E_o \qquad \text{(for all } \theta\text{)} \qquad (3.58a)$$

where ΔQ denotes the charge that leaves C_o during the i_A pulse and is replaced by i_B and power-supply current during the remainder of the repetition cycle. For large n_1 and small γ, ΔQ is greatest for $\theta = \theta_o$. Then

$$\Delta Q = \left(1 - \frac{T_o}{4T_r}\right) Q_o$$

and by Eqs. 3.53 and 3.57, Eq. 3.58(a) becomes

$$C_o \gg 2\,\frac{1+\gamma}{1-\gamma}\left(1 - \frac{T_o}{4T_r}\right) C_1 \approx 2\,C_1 \qquad (3.58b)$$

If n is large and γ small, therefore, the analysis is valid if C_o is at least 10 times as large as C_1.

Regulation Due to Leakage Inductance

Leakage inductance between A and B in Fig. 3.6 adversely affects the regulation characteristics of the circuit. Refer to the equivalent circuit of Fig. 3.8, where the role of leakage inductance is emphasized. Windings A and B of L_1 are represented by an ideal transformer of

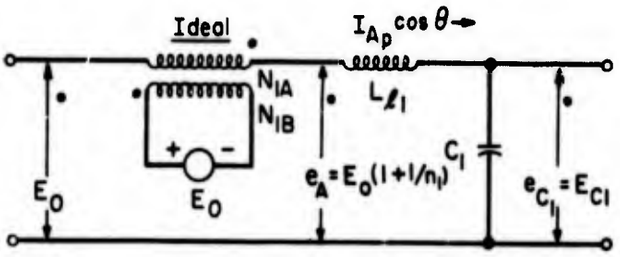


Fig. 3.8 Equivalent Circuit Showing Effect of $L_{\ell 1}$

turns ratio n_1, plus the leakage inductance $L_{\ell 1}$ -- the total leakage inductance between windings, referred to winding A. The instantaneous currents and voltages shown in the figure apply immediately after S_1 is triggered to terminate charging of C_1. The effect of L_1 is to delay interruption of the current to C_1 by the time required for the voltage $E_{C1} - E_o(1 + 1/n_1)$ across $L_{\ell 1}$ to reduce the current from its initial value $I_{Ap}\cos\theta$ to zero. Inasmuch as the current decreases at a substantially constant rate, this delay causes C_1 to charge to a voltage higher than E_{C1} by the small but significant amount

$$\Delta E_{C1} = \frac{I_{Ap}\cos\theta\, L_{\ell 1}\, \dfrac{I_{Ap}\cos\theta}{E_{C1} - E_o(1 + 1/n_1)}}{2C_1} \quad (\Delta E_{C1} \text{ small})$$

This result can be used to show that the regulation as a function of E_o, for small changes ΔE_{C1}, is

$$\frac{\Delta E_{C1}}{E_o - E_{o\,min}} = \frac{\Delta E_{C1}}{\Delta E_o} = (1 + \gamma)\,\frac{L_{\ell 1}}{L_1}\,\frac{E_{o\,max}}{E_{o\,max} - E_o} \quad (\Delta E_{C1} \text{ small}) \tag{3.59}$$

where $\Delta E_o = E_o - E_{o\,min}$ denotes the excess of E_o above the minimum value required for regulation.

The voltage input-output characteristics of the regulator circuit sketched in Fig. 3.9 show the effect of $L_{\ell 1}$.

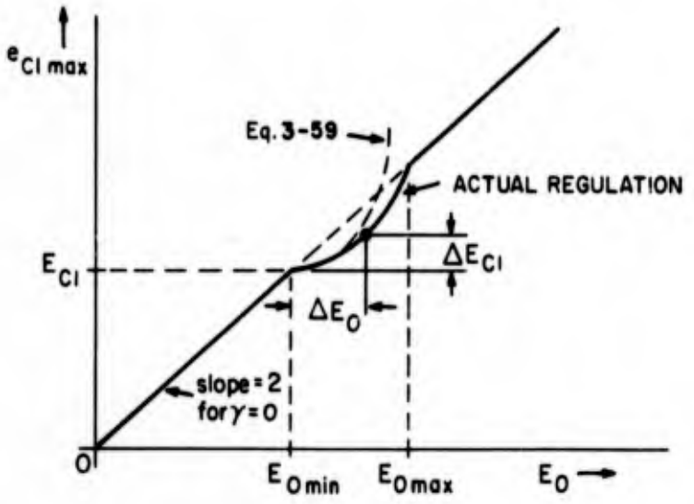


Fig. 3.9 Regulation Characteristic Showing Effect of $L_{\ell 1}$

Equation 3.59 provides an accurate description of the circuit behavior in the interval just above $E_o = E_{o\,min}$; for larger ΔE_o, the equation predicts poorer regulation than actually results. At the top of the regulation range ($E_o = E_{o\,max}$), $e_{C1\,max}$ lies on the straight line of slope 2 that applies outside the range. The best regulation occurs for $E_o \approx E_{o\,min}$, and is

$$\frac{\Delta E_{C1}}{\Delta E_o} = \frac{2L_{\ell 1}/L_1}{1 - 1/n_1 + (1 + 1/n_1)} \approx 2\,\frac{L_{\ell 1}}{L_1} \qquad (E_o \approx E_o\text{min}) \qquad (3.60)$$

2. Regulator with Power Supply

Up to this point no consideration has been given to the effects of power-supply internal impedances on regulator action. To be presented here are expressions describing the operation of the regulator in conjunction with a power supply. The power supply is assumed to be fed by an a-c line and to produce unregulated, filtered, direct current. Because θ is decreased by the regulator as the power-supply output voltage rises, the average regulator input current is decreased. Thus, the input resistance of the regulator is negative over most of the regulation range. To avoid sustained (and possibly destructive) oscillation of the combined regulator and power-supply circuits, certain stability

relationships to be set forth must be satisfied.

An equivalent circuit for the power supply is shown in Fig. 3.10. The power-supply output current i_o and voltage e_o are identical with the regulator input current and voltage shown in Fig. 3.6. The filter

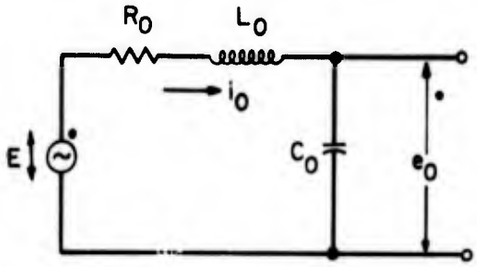


Fig. 3.10 Power-Supply Equivalent Circuit

inductor and capacitor are L_o and C_o, respectively. The equivalent internal d-c power-supply voltage E, proportional to a-c line voltage, and the effective resistance of the power supply R_o, are the $i_o = o$ intercept and slope, respectively, of the power-supply output e-i curve.

Basic Relations. In the relations that follow, it has been assumed that within a single repetition period the output current i_o remains relatively constant at the value

$$I_o = \frac{J_c}{E_o T_r}$$

where

$$J_c = \frac{1}{2}(1 - \gamma^2) C_1 E_{C1}^2 = \frac{1}{2}(1 - \gamma) Q_o E_{C1}$$

is the energy delivered to C_1 in one cycle of operation. The equivalent negative input conductance $-G_n$ of the regulator, calculated from the equation for I_o, is

$$-G_n = \frac{dI_o}{dE_o} = -\frac{J_c}{E_o^2 T_r} = \frac{I_o}{E_o} \qquad (3.61)$$

When $E_o = E_{o\,min}$, G_n assumes its maximum value G_{no}. Thus

$$G_n = \left(\frac{E_{o\,min}}{E_o}\right)^2 G_{no}$$

and

$$G_{no} = 2\,\frac{1+\gamma}{1-\gamma}\,\frac{C_1}{T_r}$$

The regulation range a' defined in terms of maximum and minimum allowable values of E (rather than E_o as for a) can be calculated from Fig. 3.10 in terms of a and the voltage drop across R_o, taking into account I_o variation. The result is

$$a' = \frac{E_{max}}{E_{min}} = \frac{2}{(1+1/n_1)(1-\gamma)}\;\frac{1+\frac{1}{4}(1-\gamma^2)(1+1/n_1)^2 R_o G_{no}}{1+R_o G_{no}}$$

$$\approx 2\,\frac{1+R_o G_{no}/4}{1+R_o G_{no}} \qquad (3.62)$$

A similar calculation yields the over-all voltage regulation as influenced by both $L_{\ell 1}$ and R_o,

$$\frac{\Delta E_{C1}}{\Delta E} = (1+\gamma)\,\frac{L_{\ell 1}}{L_1}\;\frac{E_{o\,max}}{E_{o\,max}-E_o}\;\frac{E_o}{E_o - R_o G_{no} E_{o\,min}} \qquad (3.63)$$

where ΔE denotes a change in E. The best regulation still results for $E_o \approx E_{o\,min}$, and is

$$\frac{\Delta E_{C1}}{\Delta E} = \frac{2L_{\ell 1}/L_1}{[1-1/n_1+\gamma(1+1/n_1)]\,[1-R_o G_{no}]} \approx \frac{2}{1-R_o G_{no}}\;\frac{L_{\ell 1}}{L_1} \qquad (3.64)$$

Comparison of Eqs. 3.62, 3.63, and 3.64 with Eqs. 3.57(d), 3.59, and 3.60 indicates that, because of R_o, both the regulation range and the regulation achieved are less for the over-all circuit than for the regulator alone.

Filter Design and Circuit Stability. A large filter capacitor C_o is essential to the regulator operation (see Condition 3, Section 1). A

filter inductor L_o may also be used to reduce power-supply ripple or to limit peak current in the power-supply rectifiers. Particularly in applications requiring small output-pulse jitter, a large L_o is desirable to provide ripple attenuation in addition to that provided by regulator action. For the L_o-C_o combination the ripple attenuation factor is

$$\frac{1/\omega C_o}{\omega L_o} = \left(\frac{1}{2\pi} \frac{T_{rip}}{T_f}\right)^2$$

where T_{rip} is the period of the lowest-frequency power-supply ripple and $T_f = \sqrt{L_o C_o}$ is the filter delay time.

The selection of L_o and C_o values is determined by the ripple-attenuation and over-all regulation and regulation-range requirements of the application. Ripple attenuation determines T_f, and hence the product $L_o C_o$. The other requirements relate to the circuit stability and place a limit on the ratio L_o/C_o in a manner to be described.

The power-supply-and-regulator circuit has two possible unstable modes. One is a d-c, or switching mode which results if the denominator $E_o - R_o G_{no} E_{o\,min}$ in Eq. 3.63 becomes zero. Then an output voltage ΔE_{C1} is sustained even for $\Delta E = 0$--that is, the circuit switches to one extreme or the other of its regulation range. The parameter

$$\beta^2 = R_o G_{no} \frac{E_{o\,min}}{E_o} \qquad (3.65)$$

is introduced to measure the degree of approach to this instability. For $\beta^2 \geq 1$, the circuit is stable, but the over-all regulation is inferior to that of the regulator alone--for example, by a factor of 1/2 for $\beta^2 = 1/2$. The reduction of regulation range ($\underline{a}'$ in comparison with $\underline{a}$) also depends on β^2 -- for example, $a'/a = 3/4$ if $\beta^2 = 1/2$ and $E_o = E_{o\,min}$. This d-c regulation and regulation-range consideration dictates a maximum value β_{max} of β that can be permitted in any application.

The second possible instability is an a-c mode comprising oscillation at the resonant frequency of L_o and C_o. Positive damping is provided by R_o, and negative by G_n, so that the net damping factor is

$$\alpha = \frac{1}{2}\left(\frac{R_o}{\sqrt{L_o/C_o}} - \frac{G_n}{\sqrt{C_o/L_o}} \right) \tag{3.66}$$

Any $\alpha > 0$ prevents oscillation and is sufficient insofar as d-c regulation is concerned. However, somewhat large α values, generally near $\alpha = 1$ (critical damping) are desirable with respect to transient performances--to prevent input-voltage fluctuations from initiating ringing oscillations that are only partly suppressed by regulator action. Transient performance requirements thus determine a minimum value α_{min} of α that can be permitted.

The values of α_{min} and β_{max} appropriate to an application together determine a necessary value of L_o/C_o. Inasmuch as β has its maximum value for $E_o = E_{o\,min}$ (see Eq. 3.65), and α is a minimum for $G_n = G_{no}$, it is sufficient to require

$$R_o G_{no} \leq \beta_{max}^2$$

and

$$\frac{R_o}{\sqrt{L_o/C_o}} - \frac{G_{no}}{\sqrt{C_o/L_o}} \geq 2\alpha_{min}$$

Combining these equations yields

$$\frac{L_o}{C_o} + 2\alpha_{min}\sqrt{\frac{L_o}{C_o}} \leq R_o \leq \frac{\beta_{max}^2}{G_{no}} \tag{3.67}$$

or, in order that some range of values may be available to R_o, C_o/L_o must exceed $\xi\, G_{no}$, where

$$\xi = \alpha_{min} + \sqrt{\frac{\alpha_{min}^2 + \beta_{max}^2}{2}} \tag{3.68}$$

The parameter ξ is one at the stability limit $\alpha_{min} = 0$, $\beta_{max} = 1$. For the larger α_{min} and smaller β_{max} values usually necessary, ξ is larger--of the order of 2 to 5. Evaluating G_{no} yields, with the definition of T_f,

$$C_o \geq 2 \frac{1+\gamma}{1-\gamma} \xi \frac{T_f}{T_r} C_1 \qquad (3.69)$$

and

$$L_o = T_f^2 / C_o \qquad (3.70)$$

If C_o is given the minimum value allowed by Eq. 3.70, the power-supply internal resistance must have the maximum value allowed by Eq. 3.69,

$$R_o = \frac{\beta_{max}^2}{2} \frac{1-\gamma}{1+\gamma} \frac{T_r}{C_1} \qquad (3.71)$$

For more freedom in power-supply design, a larger value of C_o may be used. Note, however, that this procedure permits smaller, not larger, values of R_o. Thus rectifier and inductor resistances must be controlled to yield R_o no larger than the value of Eq. 3.71. Smaller R_o values can be increased, without loss of efficiency, by introducing commutating inductances in series with individual rectifiers of a full-wave or polyphase power supply.

Both Eq. 3.69 and Eq. 3.58(b) (Condition 3 of Section 1) specify a minimum value for C_o. Ordinarily, satisfying Eq. 3.69 ensures that Condition 3 is met and the basic regulator-circuit analysis is applicable.

3. Peak Voltages and RMS Currents.

Of concern in the design of the voltage-regulator circuit are the peak voltages and rms currents to be handled by the controlled rectifiers S_1 and S_2, and by the windings of inductor L_1.

Expressions for the quantities of interest are presented in Tables 3-1 and 3-2. In Table 3-2 the general expression for rms current as a function of θ is given first, followed by the maximum value (for $\theta = \theta_o$) of interest in component design. Useful approximations to the maximum values are also shown.

Table 3-1

Voltage-Regulator Circuit -- Peak Voltages

Component	Peak Voltage
Inductor L_1	
Terminal A to Ground	E_{C1}
Terminal B to Ground	$n_1(1 + \gamma)E_{C1}$
Tap to Ground	$\dfrac{E_{C1}}{1 + 1/n_1}$
Per Turn	$\dfrac{E_{C1}}{(N_{1A} + N_{1B})\sin\theta}$
Controlled Rectifier S_1	
Inverse	$n_1(1 + \gamma)E_{C1}$
Forward (maximum for $\theta = \pi/2$)	$\dfrac{n_1(1 + \gamma) + (\gamma - 1)}{2} E_{C1}$
Controlled Rectifier S_2	
Inverse	$(1 - 1/a)E_{C1}$
Forward	$\left\{ \begin{matrix} E_{C1} \\ [1/(1 + 1/n_1) + \gamma]E_{C1} \end{matrix} \right\}$ Whichever is greater

Table 3.2

Voltage-Regulator Circuit -- Rms Currents

I_A

$$I_A = \sqrt{\frac{1}{T_r}\int_0^{(\pi/2+\theta)T_o/\pi} I_{Ap}^2 \sin^2(\pi t/T_o)\,dt}$$

$$= \frac{\pi}{2}\,\frac{\sqrt{1+\dfrac{2\theta+\sin 2\theta}{\pi}}}{1+\sin\theta}\,\frac{Q_o}{\sqrt{T_o T_r}}$$

$$I_{A\,max} = I_A\Big|_{\theta=\theta_o} = \frac{\pi}{2}\,\frac{\sqrt{1+\dfrac{4/\pi}{n_1(1+\gamma)+\gamma}}}{1+\dfrac{1}{n_1(1+\gamma)+\gamma}}\,\frac{Q_o}{\sqrt{T_o T_r}}$$

For $n_1 \gg 1$,

$$I_{A\,max} \approx \frac{\pi}{2}\,\frac{Q_o}{\sqrt{T_o T_r}}$$

I_B

$$I_B = \sqrt{\frac{1}{T_r}\int_0^{T_B} I_{Bp}^2 (1 - t/T_B)^2\,dt} = \sqrt{\frac{\pi}{3n_1}\,\frac{(1+\gamma)\cos\theta}{1-\gamma\sin\theta}\,\frac{1-\sin\theta}{1+\sin\theta}}\,\frac{Q_o}{\sqrt{T_o T_r}}$$

$$I_{B\,max} = I_B\Big|_{\theta=\theta_o} = \sqrt{\frac{\pi(1+\gamma)}{3n_1}\,\frac{\sqrt{1-\left(\dfrac{1}{n_1(1+\gamma)+\gamma}\right)^2}}{1-\dfrac{\gamma}{n_1(1+\gamma)+\gamma}}\,\frac{1-\dfrac{1}{n_1(1+\gamma)+\gamma}}{1+\dfrac{1}{n_1(1+\gamma)+\gamma}}}\,\frac{Q_o}{\sqrt{T_o T_r}}$$

$$\approx \frac{1}{\sqrt{n_1}}\sqrt{\frac{\pi}{3}\,\frac{n_1-(1-n_1\gamma)}{n_1+1}}\,\frac{Q_o}{\sqrt{T_o T_r}}$$

For: $n_1 \gg 1$, $\gamma < 1/n_1$

$$I_{B\,max} \approx \frac{1}{\sqrt{n_1}}\,\frac{Q_o}{\sqrt{T_o T_r}}$$

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CHAPTER IV

DESIGN PROCEDURE

The preceding chapters provide fundamental circuit operating principles essential to an understanding of the semiconductor-magnetic pulse generator. Presented in this chapter is a design procedure, based on these principles, that has been devised with the objective of reducing pulse-generator specifications to a working, experimental circuit in as straightforward a manner as possible.

After essential pulse-generator operating specifications have been determined, the procedure is to evolve a preliminary circuit design. The preliminary design is then breadboarded, and parameters that cannot be predicted with reasonable accuracy are adjusted experimentally. Design proceeds from the output circuit to the prime-power input. The output and charging circuits are considered together in the trial design; and experimental refinement of these portions of the pulse generator is accomplished before design of the voltage regulator is begun.

A. SPECIFICATIONS FOR DESIGN

Before the design process can begin, the requirements placed on the circuit must be known in detail. Following is a summary of key parameters and other information needed.

1. Type of Load

The voltage-current characteristics of the load, along with load stray capacitance, influence the output pulse shape and the choice of pulse-forming network. The output-circuit design procedure given in Section B applies directly to a vacuum-tube load, such as a magnetron, having stray capacitance C_L. Modifications to this procedure required in the case of a resistance load are suggested by the analysis of Chapter III, Section A. Special requirements of the load, such as open-circuit and short-circuit protection, should be noted.

2. Output Pulse Characteristics

Of concern for design are the current-pulse peak amplitude I_p, nominal rise time δ, nominal width τ_p, shape of the rising portion (parabolic, trapezoidal, or other) and slope and ripple of the pulse top.

Specification of the peak pulse voltage E_p and fall time τ_1 is also required. The magnitude E_1 of peak allowable pre-pulse output voltage must be controlled for some tube loads, as must the amplitude of positive and negative voltage peaks that occur after the pulse. The time delay between main trigger pulse and output pulse is of concern for some applications (in a semiconductor-magnetic pulse generator, this delay is usually 5 to 10 or more times τ_p). The amount of amplitude or time jitter in the output pulse train influences the design of the voltage-regulator circuit. The repetition rate $1/T_r$, together with the pulse shape, voltage, and current, set the average power requirement on the pulse generator.

3. Prime Power Source

The type (a-c or d-c),voltage,and regulation of the prime power source influence the design of the voltage regulator and associated input circuit. Voltage, frequency, and number of phases of an a-c source control the choice of input transformer (if any), rectifiers, and ripple filter. A d-c source connects directly to the voltage regulator--except that capacitor C_o may be retained to shunt a-c impedance in the source, or (for a battery) to permit storage rather than dissipation of energy returned each cycle by current in winding B of inductor L_1. Source regulation determines both the regulation range and the stabilization factor required of the regulation circuit.

4. Environment

The most important environmental specifications needed for design are the ambient temperature range and the means of cooling available. The controlled-rectifier maximum junction temperature cannot, for most types, exceed 125 C; temperature rise from stud to junction is usually limited to about 60 C. Controlled-rectifier storage temperature is usually limited to 150 C. The ambient-temperature specifications and means of cooling provided must be compatible with the controlled rectifiers. Shock, vibration, salt spray, humidity, and altitude requirements influence final packaging rather than the basic circuit design.

5. Design Objectives

Of major importance to the pulse-generator design is the relative importance of various design goals in the application of interest. For example, the relative importance attached to reliability, efficiency, small size and weight, and cost must be taken into account to achieve a balanced design since, in general, maximum reliability and efficiency cannot be provided simultaneously with minimum size, weight and cost. Special design requirements not considered in this report may be important in certain applications. For example, a means may be needed for protecting the load and pulse-generator components during fault conditions common in some high-power r-f generators. The fault protection may provide for dissipating safely the output-pulse energy during the fault--or, better, a means for storing the energy for use after the fault terminates.

B. THE OUTPUT AND CHARGING CIRCUITS

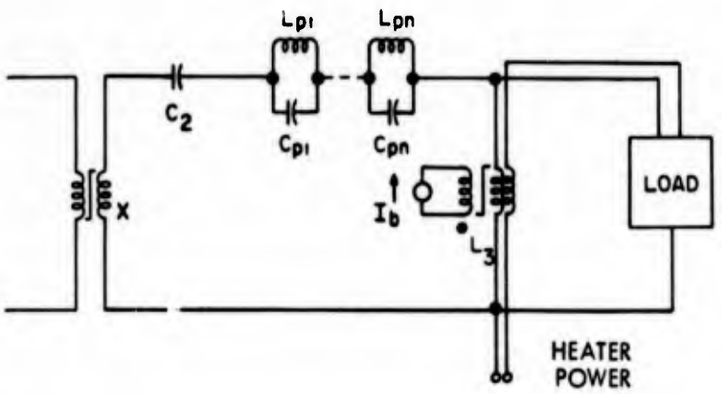
1. Output-Circuit Trial Design

The over-all design procedure for the output circuit (Fig. 3.1) is similar to the one that would be followed in designing a conventional, line-pulsing modulator. First, the particular circuit configuration best suited to the design specifications must be decided upon. This determination is influenced by the operating point desired on the e-i characteristics of the load (that is, by values required for E_p, I_p, and $R_L = E_p / I_p$), by limitations on pulse-forming-network voltage ratings or characteristic impedances readily achievable, and, perhaps most of all, by the designer's experience.

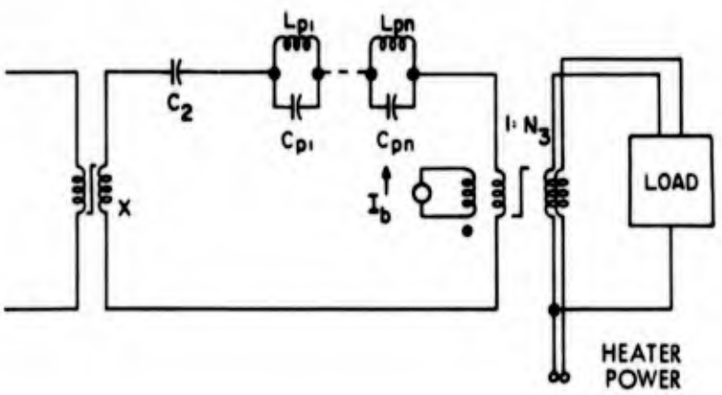
For reasons previously stated (Chapter III, Section A) the entire voltage step-up required between capacitor C_1 and the load should be provided by saturable transformer X whenever practicable. Subject to this condition, the output circuit has the form drawn in Fig. 4.1(a). Here L_3 is shown with a bifilar winding to permit heater power to be supplied to a grounded-anode vacuum-tube load. Although a Type A network configuration is shown, any equivalent pulse-forming network can be used. In low-voltage circuits (say E_p a few thousand volts or less) inductor L_3 can be replaced by a semiconductor diode with a saving in weight and loss.

In certain applications the circuit of Fig. 4.1(a) may be undesirable because a very high required E_p makes the associated pulse-forming network rating of $2E_p$ difficult to achieve. More likely, if the required E_p is high in a low-power application, the network characteristic resistance needed to match R_L may be inconveniently high. A step-up ratio at the output is thus desirable to match a network of convenient impedance (of the order of 50 ohms or so) to the higher impedance load. This ratio is best achieved as in Fig. 4.2(b) by adding a bifilar high-voltage winding to L_3; n_3 denotes the ratio of turns in the high-voltage winding to the turns in the pulse-network winding. Note that the need for the output step-up, as in Fig. 4.1(b), is determined by the pulse-forming network and output requirements--not by a limit on step-up ratio achievable in transformer X. Ratios of at least 50 are obtainable without difficulty.

Once an output-circuit configuration is chosen, the determination



(a) No output-voltage step-up.



(b) Voltage step-up winding on L_3.

Fig. 4.1 Output Circuit

of components begins. For selection of the pulse-forming network, the nominal parameters of the output pulse, E_p, R_L, τ_p, and δ are significant. If an output step-up ratio n_3 is used, E_p and I_p (and derived parameters, such as $R_L = E_p / I_p$) denote values referred to the pulse-network side of the output transformer. Also important are the nature of the load (i.e., linear resistor or nonlinear vacuum tube), and the applicable environmental and reliability conditions.

The pulse network may be designed from first principles or purchased to meet the above specifications from a company specializing in pulse-network design.[1] A Type A or Type B network can be used, although the Type E is generally preferred by pulse-network specialists.

Two pulse-forming network parameters are important to the design of the remainder of the circuit. One is the series inductance

$$L_S = \delta R_L \tag{4.1}$$

associated with the specified nominal rise time δ. If a Type A or Type B network is employed and no output step-up is used, the entire inductance L_S is available as saturated secondary inductance L_{X2} of transformer X; the core volume required for transformer X varies inversely with L_{X2}. If output step-up is used, the leakage inductance of the output transformer (referred to the primary) must be subtracted from L_S to determine L_{X2}. Similarly, if a Type E network is employed, some of L_S may be required to be retained in the network section. Thus, an inductance less than L_S is available to be split between output-transformer leakage inductance (if any) and L_{X2}.

The other pulse-network parameter is the equivalent low-frequency capacitance C_2, important in the design of the charging circuit. For a Type A network, C_2 is the series capacitance; for a Type B or Type E network, C_2 is the sum of all the shunt capacitances. For any network,

$$C_2 = \frac{\tau_p}{2R_L} \tag{4.2}$$

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[1] Chap. III, Sec. A; also, G.N. Glasoe and J.V. Lebacqz, Pulse Generators (Radiation Laboratory Series, Vol. 5; McGraw-Hill Book Co., N.Y., 1948), pp. 189-257. See also Chap. III, Sec. 1 of this report.

After selection of the pulse network and calculation of C_2 and the external portion of L_S, certain parameters of the diode inductor L_3 and the saturable transformer X can be determined. The number of windings required on L_3 and the turns ratio n_3 (if L_3 is a step-up transformer) are determined by the initial choice of Figs. 4.1(a) and 4.1(b) and the pulse-network impedance. The peak voltage across L_3 is E_p (or $n_3 E_p$ for the high-voltage winding), and the volt-time integral (referred to the low-voltage winding) may be taken to be

$$\lambda_3 = E_p \tau \tag{4.3}$$

(see Chapter III, Section A.1), where τ is the over-all pulse duration ($\tau = \tau_p + 4\delta/3$ for a pulse with parabolic rise and fall). Similarly, the peak voltage across the secondary of transformer X is $2E_p$, and the required secondary saturated inductance is L_S less the portion of L_S in the pulse network (if Type E) and less an allowance for leakage inductance in L_3 (if output step-up turns are used).

At this point, design of L_3 cannot be completed because its saturated-inductance value is not determined. If the load is a vacuum tube, specifications on maximum pulse-tail time τ_1 and load capacitance C_L set a maximum limit on L_3 (see Eq. 3.11),

$$L_3 \leq \frac{4}{\pi^2} \frac{\tau_1^2}{C_L} \tag{4.4}$$

However, a more restrictive requirement may be set by the allowable peak value of the prepulse voltage (see Eq. 3.5) which is determined by the charging-circuit design. Similarly, the saturable-transformer design cannot be completed because its turns ratio and volt-time integral are not yet determined. Furthermore, if output step-up turns are used on L_3, the value of L_{X2} depends on the allowance for leakage inductance in L_3 -- and thus on completion of the L_3 design.

In summary, preliminary design of the output circuit yields a choice of (1) the circuit of Figs. 4.1a or 4.1b, and (2) the pulse-forming network, together with certain initial data to be used in the design of the saturable transformer and diode inductor.

2. Charging-Circuit Trial Design

Design of the charging circuit, depicted schematically in Fig. 3.4a, proceeds with the aid of the equivalent circuit of Fig. 3.4b, in which all element values are referred to the low-voltage side of transformer X. At present, the one component for which the least detailed pulse-service performance data is available is controlled rectifier S_3. It is thus recommended that the charging circuit be designed on an iterative basis, and that the design begin with the trial selection of a controlled-rectifier type for S_3. The selection should be from among the best fast-turn-on, short-pulse-service controlled rectifiers available. Then S_3 will comprise either a single controlled rectifier of the selected type or a series or parallel bank of them as discussed at the close of Chapter II, Section B4.

Associated with the trial selection of a controlled rectifier (or rectifiers) is the selection of the voltage E_{C1} to which capacitor C_1 is to be charged. From the viewpoint of the controlled rectifier, E_{C1} should be the rated blocking voltage at maximum junction temperature of the rectifier. From the viewpoint of minimizing the volume and weight of C_1, however, E_{C1} should be at least 1000 v. Thus, either a very high-voltage controlled rectifier, or two lower-voltage units in series, is necessary--or a low-voltage capacitor of large volume must be used. Series connection of controlled rectifiers is to be avoided, if practicable, because of triggering and voltage-division problems. A further consideration in the choice of E_{C1} is the relatively fixed relation of voltage-regulator input and output voltages. If the prime source is a d-c source, E_{C1} is fixed at about twice the minimum source voltage regardless of capacitor and controlled-rectifier considerations. With an a-c source, an input transformer can be used to adjust the input voltage, but the advantage of so doing must be weighed against the weight and loss of an input transformer.

With the controlled rectifier (or array of rectifiers) and voltage E_{C1} chosen, the next step is to evaluate the rectifier power switching capacities

$$P_r = n_r E_r I_r \tag{4.5}$$

where E_r is the rated blocking voltage (or less as required by the selection of E_r), and n_r is the number of rectifiers in the array. Determination of I_r is a more formidable problem. First determine the nominal rated current from Eq. 2.43

$$I_{ro} = \sqrt{\frac{(T_{jp} - T_s)_m}{R_{Th}R_s}} \tag{4.6}$$

from manufacturer's published specifications. The maximum allowable average junction-to-stud temperature rise $(T_{jp} - T_s)_m$ for prevailing controlled rectifier types in average-reliability service is presently about 60 C, provided that cooling is sufficient to hold the stud at 65 C or less (see Chapter II, Section B.4). The junction-to-stud steady-state thermal resistance R_{Th} is usually stated as an average over many samples; the maximum value should be used. The incremental, high-current forward resistance R_s of the fully turned-on rectifier can be determined from the conducting-state e-i curve at high currents.

To determine I_r in Eq. 4.5, derating factors must be applied to I_{ro} to account for partial turn-on, duty cycle, and repetition rate (see Eqs. 2.42 and 2.45 and the related discussion). It is in the determination of these factors, as well as in the initial selection of a controlled rectifier, that trial-and-error enters the design. For the first trial it is reasonable to ignore the duty-cycle factor and to calculate the repetition-rate factor on the assumption that $R_{Th}C_{Th}$ in Eq. 2.45 is 10^{-3} sec. (See Chapter II discussion pertaining to Eq. 2.45). To specify reasonable values for the partial turn-on factor x is more difficult. Reasonable values range from x = 1 (fully turned on) for very long output pulses to x = 2 (half turned on at the start of the charging pulse) for τ_p of the order of a microsecond and to higher x for shorter τ_p. Values of hold-off time T_h and hold-off current I_h necessary to provide the assumed x cannot be determined prior to actual test of the completed circuit, but a rough estimate for use in the trial design can be made from rectifier manufacturer's data (see Chapter II, Section B.4).

The trial derating factors yield a value of I_r and, by Eq. 4.5, of P_r. The corresponding charging time is

$$T = \frac{\pi^2}{2T_r}\left(\frac{J_c}{P_r}\right)^2 \qquad (4.7)$$

where T_r is the specified repetition rate, and J_c is the energy stored on C_1. (Use $J_c = 1.15\ J_p$ as an initial trial, to account for losses.) The value of T calculated can be used in Eqs. 2.42 and 2.44 to determine whether or not the duty-cycle derating factor can be ignored as at first assumed. If necessary, this factor can be introduced and T adjusted accordingly.

Comparison of T with τ_p yields a preliminary check on the initial controlled-rectifier choice. If T is of the order of 2 to 5 times τ_p, the choice is probably reasonable, and the design should proceed. A longer T is likely to lead to excessive saturable-transformer weight and loss; a larger controlled rectifier (or more units of the type chosen) should be considered. A shorter T suggests that a rectifier (or rectifiers) of smaller power-switching capacity may suffice. The T/τ_p ratio of 2 to 5, like the initial choice of x, is suggested only for first-trial purposes. Both values should be altered as seems desirable on the basis of component sizes and losses determined as the design proceeds.

Once a reasonable value of T is determined, an estimate of saturable-inductor core volumes can be obtained. First, the energy-switching capacities of the three saturable elements is calculated with the aid of Eqs. 3.26, 3.29, and 3.40, as

$$J_X = \frac{\tau_p}{2\delta}\left(\frac{T + 2T_g}{\tau_p}\right) J_c \qquad (4.8)$$

$$J_2 = \frac{\left(T_h + \tau/2\right) T_h}{T^2\left[1 + (1 - \alpha)\tau/2T_h\right]}\ J_c \qquad (4.9)$$

$$J_3 = \frac{\pi^2}{2}\ \frac{(T_h + \tau/2)\,\tau/2}{\alpha\, T^2}\ J_c \qquad (4.10)$$

Take $T_g = 0$ in Eq. 4.8 (see Section 3). The parameter α in Eqs. 4.9 and 4.10 should be adjusted to meet specifications of maximum allowable pulse-tail duration τ_1 and prepulse voltage E_1. The equations are:

$$\tau_1 = \frac{T}{2}\sqrt{\frac{a\tau}{T_h + \tau/2}}\sqrt{\frac{C_L}{C_2}} \qquad (4.11)$$

$$E_1 = E_p \frac{a\tau}{T_h + \tau/2} \qquad (4.12)$$

For $a = 1$, the total core volume for L_2 and L_3 is minimized. Smaller values of a may be necessary to reduce τ_1 or E_1 to the required size. If a semiconductor diode is used in place of L_3, then a in Eq. 4 9 should be taken as 0; Eqs. 4.10, 4.11, and 4.12 then no longer apply.

The core volumes can now be estimated from the general relation

$$V = \frac{J}{2B_s^2/\mu_e} \qquad (4.13)$$

The value of B_s used in Eq. 4.13 should be determined from manufacturer's specifications for a core temperature equal to the maximum ambient temperature plus a 30-to-50 C rise to account for core and winding losses; J in Eq. 4.13 is determined by Eqs. 4.8, 4.9, and 4.10. An accurate value of μ_e (which depends on winding construction) cannot be determined at this stage in the design. An approximate value--such as μ_e = 4 microhenries per meter for 50-percent-nickel iron--may be used.

At this point, the consequences of the initial choices of controlled-rectifier switching capacities and turn-on factor x should be reviewed. For a given controlled rectifier, x (and hence T) can be decreased by increasing the hold-off time; thus the saturable-transformer core volume can be decreased at the cost of increased core volume in the two saturable inductors (see Eqs. 4.8, 4.9, and 4.10). Since the inductor volumes change much more rapidly with T_h than does the transformer volume (especially if full turn-on is approached), minimum total weight and loss is likely to result when the transformer core is considerably larger than the inductor cores. By changing the type or number of controlled rectifiers the saturable-transformer volume may be changed roughly in proportion to the change in charging time T produced by the change of the rectifier switching capacity. If in the process x is adjusted to maintain T_h/T constant, the saturable inductors are

little affected; otherwise the effect of simultaneous T and T_h/T changes must be considered. In weighing saturable-element core volumes against the cost of controlled rectifiers, it should be remembered that total volumes are much greater than core volumes--by a factor of at least 5 for the saturable transformer (the bulkiest of the saturable devices).

Once a trial design is worked out that appears satisfactory in terms of controlled rectifiers and saturable-element volumes, a rough calculation of major circuit losses is in order as a final check on the merit of the design. Controlled-rectifier switching loss can be estimated from Eq. 2.37,

$$J_s = \left(\frac{\pi}{2} \sqrt{\frac{T_r}{T}} \frac{xR_s I_r}{E_r} + \frac{2E_d}{E_r} \right) J_c \qquad (4.14)$$

Magnetic-core switching loss is estimated from Eq. 2-16 for each element as

$$J_m = \frac{\mu_e H_c}{B_s} \left[1 + \phi(t_{sw}) \right] J \qquad (4.15)$$

where $\phi(t_{sw})$ is given in Eqs. 2.23 and 2.24 for 50-percent-nickel iron, and J is the energy-switching capacity of the element. The value of B_s used here should be the elevated-temperature value, as before. Winding loss J_w in the saturable-core elements can be important; unfortunately, there is no accurate way of estimating it in narrow-pulse applications, short of making a paper design of the entire inductor. At this stage of the design process, a reasonable procedure is to assume the winding loss to be equal to the core loss in long-pulse applications ($\tau_p > 10\mu s$) and somewhat larger, but not more than twice the core loss, in short-pulse applications.

There are other losses in the charging and output circuits, but they are generally smaller than the losses considered thus far. Thus a reasonable idea of the over-all efficiency can be had by computing the ratio

$$\frac{\text{Output Energy}}{\text{Major Losses}} = \frac{J_p}{J_s + \Sigma(J_m + J_w)} \qquad (4.15a)$$

A ratio of about 5 may be considered reasonable in ordinary applications, but the value to be sought depends upon the importance of efficiency and light weight in relation to controlled-rectifier cost in the pulse generator of interest.

Once the loss ratio of Eq. 4.15a is computed--and the trial-design procedure repeated with a new selection of controlled rectifier if the first loss ratio is unsatisfactory--the trial design is complete. At this point, specific controlled-rectifier and pulse-forming-network choices have been made, and values have been assigned to key quantities that serve as the basis for design of the remaining circuit elements. These quantities are:

Charging-circuit input voltage E_{C1} and pulse energy J_c.

Hold-off current I_h and time T_h.

Controlled-rectifier power-switching capacity P_r and charging interval T.

Saturable-element energy-switching capacities, J_X, J_2, and J_3 (and the corresponding core volumes), and the diode-inductor parameter α.

Pulse-network peak voltage $E_{C2} = 2E_p$, characteristic resistance R_L, energy-storage capacitance C_2, and series inductance L_S.

Diode-inductor volt-time integral λ_3 and turns ratio n_3 (if used as an output transformer).

3. Detailed Design -- C_1 to Load

The results of the trial-design procedure listed above provide a starting point from which to proceed in the detailed design of the pulse-generator circuit from the load back to the low-voltage capacitor C_1. As each component is designed, a more accurate assessment can be made of circuit weight and efficiency; if necessary, changes can be made in the over-all circuit design to take into account the more accurate data.

Diode Inductor L_3. Manufacturers' catalogs of saturable-magnetic cores should be searched for a core of the approximate volume given by the evaluation of Eq. 4.13 for L_3. Select only cores having nonmetallic

cases to minimize eddy-current losses. The winding placed on this inductor must provide for the previously determined value of λ_3 (see Section B.1) in accord with the relation (Eq. 2.9)

$$\lambda_3 = 2N_3 B_s A \tag{4.16}$$

Equation 4.16 may be solved for N_3. Inasmuch as the tail-clipping performance of L_3 depends on λ_3, B_s should be evaluated for an estimated average core temperature. At higher temperatures, the output pulse will be terminated by premature saturation of L_3; at lower temperature some tail-clipping effect will be lost. Remember that A is the cross-sectional area of the magnetic material only; some catalog core listings require that the area given be reduced by the appropriate stacking factor. Inductor L_3 must provide not only the required λ_3 value, but also the correct saturated inductance

$$L_3 = \frac{\lambda_3^2}{2J_3} \tag{4.17}$$

where J_3 is given by Eq. 4.10. Inasmuch as the initial-design value of μ_e is approximate and because the volume of the core selected is likely to differ somewhat from the trial-design value, only an approximate agreement of the saturated inductance (see Eq. 3.9)

$$L_3 = \frac{N_3^2}{\ell_3} \mu_e \left[A_w + (\mu_r - 1) A \right] \tag{4.18}$$

of the actual diode inductor with the required value of Eq. 4.17 is to be expected. (In Eq. 4.18, A_w is given the minimum value made necessary by winding-to-core insulation required for the output-pulse voltage.) If L_3 in Eq. 4.18 is too small, A_w (and hence L_3) can be increased by adding more insulation to the core. If L_3 is too large, a larger magnetic core is needed. It may be necessary to use two different cores of similar inside and outside diameters, wound as a single core, to satisfy the requirements. Alternatively, some manufacturers will supply, at a nominal extra cost, cores in heights larger by increments of 1/32" than the heights listed in the catalog; the availability of such

cores means that the required L_3 and λ_3 can both be provided with a core of close to minimum volume. For use in a breadboard circuit, it is recommended that the standard core size that comes closest to satisfying both the λ_3 and L_3 requirements be chosen, even if some excess volume (and hence loss) results; the minimum-volume core can be selected after breadboard evaluation is completed.

The inductor winding should conform to the recommendations of Chapter II, Section A, and Section A.5. Where a bifilar high-voltage winding is desired, an even number of strands must be used to make up the bifilar winding. A configuration such as that of Fig. 4.2 is recommended for the high-voltage winding so that the winding may

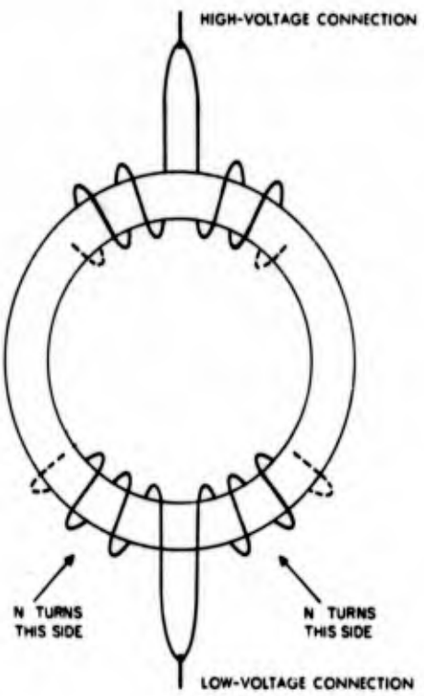

Fig. 4.2 Winding Configuration of N-Turn Toroidal Inductor

cover the entire core length and at the same time the high- and low-voltage ends may be separated by the longest distance possible. Individual insulated turns should be touching on the inside of the toroid, and equally spaced on the outside edge. A thermocouple junction placed at the low-voltage end of the winding facilitates monitoring inductor temperature during subsequent circuit evaluation.

As soon as the main winding is completed, both λ and the saturated

inductance should be checked in a circuit such as the one discussed in Appendix B, and adjustments in construction made where appropriate. Leakage inductance of L_3 when wound as a step-up-transformer can be measured in the conventional way. The procedure is to short-circuit the high-voltage winding and measure the inductance at the low-voltage winding terminals. Loss in the partially completed inductor can be calculated with substantially higher accuracy than before, using the exact volume of the magnetic core selected and the details of the winding (see Chapter II, Section A.5).

Addition of sufficient insulation outside the main winding of L_3 to withstand the operating voltage between the main and bias windings is the final step in the construction of the breadboard inductor. The bias winding itself is added later. Vacuum and pressure impregnation with high-grade transformer oil is suggested for breadboard high-voltage saturable inductors. The oil permits drastic modifications to be made on the components with relative ease, yet provides high-quality insulation.

Transformer X. The high-voltage winding is placed next to the core to minimize the saturated inductance L_{X2}. The design and construction of this winding proceed substantially as described above for L_3. The core selected for the transformer should have a volume approximately equal to L_S/L_{X2} times the value calculated from Eqs. 4.8 and 4.13. Here, as in Section B.1, L_S is the effective series inductance of the pulse-forming network, and L_{X2} is the portion of L_S available as transformer saturated inductance -- L_S less the internal part of L_S (for a Type E network), and less the leakage inductance of L_3 (if L_3 is a step-up transformer). The factor L_S/L_{X2} enters because Eq. 4.8 assumes L_{X2} to be equal to L_S. The high-voltage winding placed on this core must absorb the volt-time integral

$$\lambda_{X2} = E_{C2}\left(\frac{T}{2} + T_g\right) \tag{4.19}$$

where T_g is the guard interval. It is recommended that the transformer be designed to provide $T_g = 0$ at the highest expected core temperature. This assures that T_g is always positive, but not excessive. Such an assumption was implicit in the trial design procedure of Section D, and

leads to

$$\lambda_X = \frac{1}{2} E_{C2} T \tag{4.20}$$

The design and adjustment of the high-voltage winding to absorb λ_3 and provide precisely the required L_{X2} follows the procedure outlined for L_3.

The next step is the design of the primary winding. The required secondary-to-primary turns ratio, $n_X = N_{X2}/N_{X1}$ is not exactly the desired voltage ratio E_{C2}/E_{C1} because of the effect of losses. An estimate of this effect can be made with the aid of the relation

$$\frac{1}{2} C_1 E_{C1}^2 = \frac{1}{2} C_2 E_{C2}^2 + \Delta J \tag{4.21}$$

which represents the division of the energy initially stored in C_1 into energy transferred to the pulse network and dissipated energy ΔJ. If the dissipated energy is small, Eq. 4.21 is very nearly the same as

$$\frac{1}{2} C_1 E_{C1}^2 = \frac{1}{2} C_2 \left(E_{C2} + \frac{\Delta J}{C_2 E_{C2}} \right)^2 \tag{4.22}$$

Thus, E_{C1} is the voltage required in a <u>lossless</u> circuit to produce a pulse-network voltage $E_{C2} + \Delta J/C_2 E_{C2}$. To the extent that the lossless-circuit capacitance ratio $C_1/C_2 = n_X^2$ is maintained and provides complete energy transfer in the actual circuit, therefore

$$n_X = \frac{E_{C2} + \Delta J/C_2 E_{C2}}{E_{C1}} \tag{4.23}$$

serves as an estimate of the required turns ratio. In Eq. 4.23, E_{C1} and E_{C2} are given the trial-design values, and an estimate of ΔJ is obtained by adding estimated losses in S_3, L_2 and the transformer to the calculated loss in L_3.

Ordinarily, N_{X2} is only a few times the required n_x, and thus the number of primary turns $N_{X1} = N_{X2}/n_X$ is very small. Since this number must be an integer, the selection of values available for n_X is limited, and it is usually not possible to provide precisely the value specified by Eq. 4.23. If L_3 is constructed as a step-up transformer, it may be possible to accommodate the limited choice of n_X values by a

small change in N_3. Otherwise, E_{C2} is usually fixed within narrow limits by output-pulse specifications, and it is necessary to adjust E_{C1} to satisfy Eq. 4.23. However, if the trial-design value of E_{C1} is E_r (the rated blocking voltage of S_3) no increase is allowable. Thus, the n_X value next above that specified by Eq. 4.23 (with $E_{C1} = E_r$) must be used, together with a somewhat reduced value of E_{C1}.

With n_X, and hence N_{X1}, determined, the transformer can be wound. The high-voltage winding should be constructed as described for the main winding of L_3 and insulated appropriately from the core and the primary winding. To minimize skin-effect losses, the primary winding should be a multifilar single-layer or litz winding arranged to cover as nearly as possible the entire perimeter of the toroid. If S_3 comprises a number of controlled rectifiers in parallel, a separate primary winding should be provided for each parallel string of rectifiers. Each such winding may be multifilar, and each should comprise N_{X1} turns. Further details are given below in connection with similar multiple windings required on the hold-off inductor.

The design of the completed transformer can be partially checked as follows. The values of λ_3 and L_{X2} can be measured in the circuit of Appendix B. Leakage inductance can be measured by short-circuiting all primary windings and measuring the resultant secondary inductance. Dividing the result by n_X^2 yields L_ℓ, the leakage inductance referred to the primary. Core and winding losses for the specific core chosen and windings constructed can be calculated by the methods of Chapter II, Section A.5. Note that significant winding loss is associated with two high-current periods: (1) The pulse period, when the transformer is saturated and pulse current flows in the secondary. Here the discussion of Chapter II, Section B.5 applies. (2) The charging period, when the transformer is unsaturated and large currents producing opposing magnetizing forces flow in the two windings. If both windings are single-layer, the magnetic field is confined to the interwinding space, and the losses are those associated with skin-depth conduction in the adjacent conductor surfaces. The total calculated transformer loss should be checked against the estimate used in determining ΔJ in Eq. 4.23, and the values n_X and E_{C1} adjusted if necessary.

Capacitor C_1. The turns ratio n_X fixes the value of capacitor C_1 at

$$C_1 = \frac{C_2}{n_X^2} \tag{4.24}$$

and the final value selected for E_{C1} determines the capacitor voltage rating. It is essential to use a high-quality (low-inductance, low-loss) pulse capacitor here.

Hold-off Inductor L_2. Calculations of core volume and number of turns for L_2 proceed in the same way as for L_3. The saturated inductance to be provided to realize the trial-design value of T is, by Eq. 3.20,

$$L_2 = \frac{2T^2}{\pi^2 C_1} - \left(L_\ell + \frac{L_3}{n_X^2} \right) \tag{4.25}$$

where L_ℓ and L_3 are measured values for the transformer and diode inductor, respectively. The volt-time integral to be absorbed is

$$\lambda_2 = E_{C1} T_h \tag{4.26}$$

where T_h is the trial-design hold-off interval and E_{C1} is the revised value of capacitor-C_1 voltage determined in the transformer design. The core volume for L_2 is then determined from Eq. 4.13 using $J_2 = \lambda_2^2 / 2L_2$ and Eqs. 4.25 and 4.26 (rather than Eq. 4.9 for J_2) in order to make use of the L_ℓ and L_3 measurements. Selection of the core, determination of the number of turns, and adjustment of the winding to achieve the desired L_2 value then proceeds as before.

The number of turns required on L_2 is usually very small, so that a multifilar winding is necessary to cover the toroid perimeter. If S_3 is a single controlled rectifier (or several rectifiers in series) the winding strands are connected in parallel, as usual. If, however, S_3 comprises n_r rectifiers in parallel, the multifilar nature of the winding can be utilized to reduce unbalance of current (and hence of dissipation) among the rectifiers. The total number of strands K in a K-filar winding is made a multiple of n_r and divided into n_r equal groups. The transformer primary is divided similarly, and each group of hold-off-inductor strands is connected to the rectifier and to one group of transformer-

primary strands. The several rectifier-inductor-transformer circuits thus obtained are connected together only where they join the remainder of the circuit. Thus leakage inductances between the n_r parts of the inductor and transformer windings are in series with any unbalanced components of controlled-rectifier currents and tend to equalize the current distribution. If the currents are balanced, the leakage impedances have no effect in the circuit. To maximize the current-equalizing effect, the leakage impedance should be large. Thus, it is desirable not to interweave strands of the n_r groups, but to locate them in separate sections around the core--as illustrated for $n_r = 3$ in Fig. 4.3. (Each of the windings of N_2 turns illustrated represents one group of K/3 strands of a K-filar total winding). The n_r separate windings should together cover the toroid perimeter as uniformly as possible in order that the saturated inductance and losses may be as nearly as possible the same as in a single K-filar winding of N_2 turns.

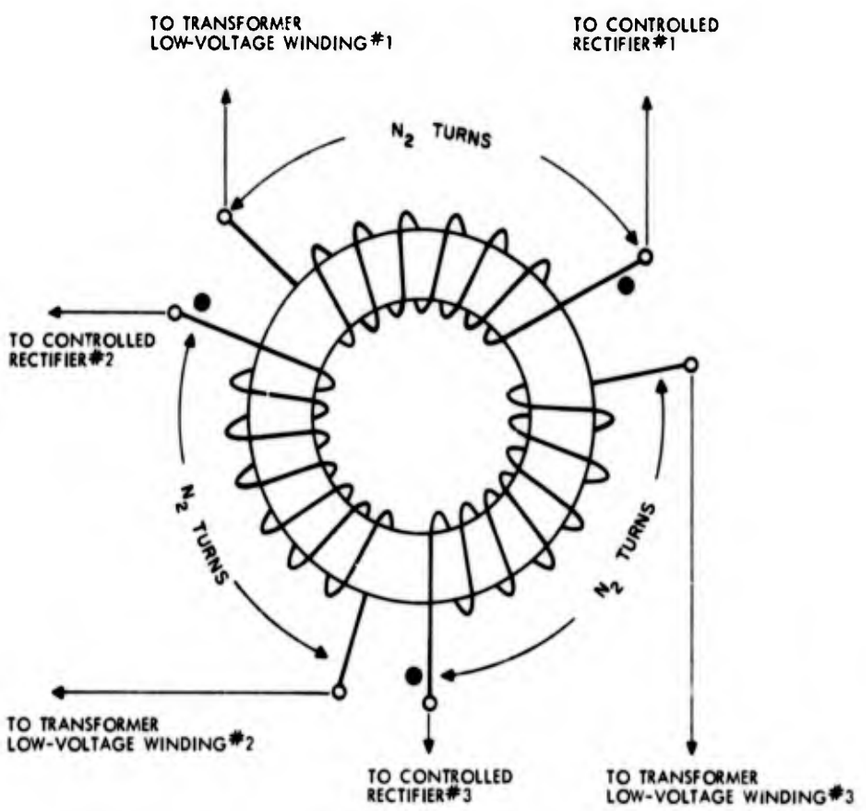

Fig. 4.3 Hold-Off Inductor Winding Configuration for 3 Parallel Discharge Paths

For the completed hold-off inductor, λ_2 and L_2 can be measured, again using the Appendix-B circuit, and the core and winding losses can be calculated. For use in the bias-circuit design, it is desirable also to determine the magnetizing current in L_2 during hold-off,

$$I_{2m}' = j_h \frac{\ell_2}{2N_2 B_s} \tag{4.27}$$

where j_h is evaluated by means of Eq. 2.21 or 2.22 for $t = T_h$, and ℓ_2 is the magnetic path length for the L_2 core. The current I_h in L_2 during the hold-off interval is, by Eq. 2.7,

$$I_h = \frac{N_{2b}}{N_2} I_b + I_{2m}' \tag{4.28}$$

where I_b is the current provided in a bias winding of N_{2b} turns. Since a value for I_h (for n_r rectifiers in parallel, n_r times the individual-unit turn-on current) has been assumed in the trial design, and I_{2m}' may be a significant part of I_h, its value influences the design of the bias circuit.

Bias Circuit and Bias Inductor. The bias circuit includes the bias inductor L_b, bias windings on the saturable transformer and two saturable inductors, and the bias supply. As explained in Appendix A, paper design of the bias circuit is complicated and the results are unreliable because of the large effects of small voltages that remain on C_1 and C_2 at the end of the output pulse. In comparison with such analysis, experimental adjustment of bias turns and bias current is almost trivially simple. Thus, the design procedure given here is intended only to provide a starting point for experimental adjustment; it is offered with the understanding that bias-circuit adjustments are among the first to be made when the breadboard circuit is operated.

An initial requirement on the bias circuit is that the bias ampere-turns for L_2 satisfy Eq. 4.28. That is,

$$N_{2b} I_b = N_2 (I_h - I_{2m}') \tag{4.29}$$

where I_{2m}' is given by Eq. 4.27 and I_h is the trial-design value. Minimum-loss reset modes (see Appendix A, Section 4) are more likely

if

$$\frac{I_{2r}}{n_X} > I_{3r} \tag{4.30}$$

and

$$I_{Xr} > I_{3r} \tag{4.31}$$

where, for each saturable device,

$$I_r > \frac{N_b I_b}{N} - \frac{H_c \ell}{N} \tag{4.32}$$

and I_r and N refer to the main winding (the high-voltage winding for the transformer), N_b and I_b refer to the bias winding, ℓ is the magnetic path length in the core, and H_c is the field intensity during reset (28 amp per meter for 50-percent-nickel iron).

A value for $N_{2b}I_b$ is specified by Eq. 4.29, and in consequence a maximum limit on $N_{3b}I_b$, and a minimum limit on $N_{Xb}I_b$ are established by Eqs. 4.30, 4.31, and 4.32. Select convenient values for each N_bI_b that satisfy these limits, and then choose I_b small enough to permit use of conveniently small bias-winding wire, yet large enough to avoid bias windings with so many turns that high-voltage insulation problems occur in the bias circuit. (The only significant bias-winding loss is d-c dissipation.) The choice of I_b and wire size should provide for a considerable range of variation of I_b during experimental adjustment of the bias circuit, as well as for changes in the number of turns on each bias winding. Bias-winding turns are placed around the toroids in any convenient configuration, but should be kept safely removed from high-voltage terminals and arranged so that changes in numbers of turns can be made easily.

Because of the range of I_b to be provided, an adjustable bias supply and an over-size inductor L_b are required in the breadboard circuit. The physical size of the inductor depends largely on the maximum value of the energy $J_b = L_b I_b^2/2$ to be stored. An air gap in the inductor core will undoubtedly be necessary. The inductance L_b should be large enough to limit the current change

$$\Delta I_b = \frac{\lambda_b}{L_b}$$

to a small fraction of the minimum bias current; λ_b is the time integral of voltage across the three series-connected bias windings during the hold-off, charging, and pulse periods (see Chapter III, Section A). If $I_{b\ max}$ and $I_{b\ min}$ denote maximum and minimum values of I_b to be used, and if $\Delta I_b = I_{b\ min}/4$, then

$$J_b = \frac{1}{2} L_b I_{b\ max}^2 = 2\lambda_b \frac{I_{b\ max}^2}{I_{b\ min}} \qquad (4.33)$$

where λ_b is evaluated for the maximum number of turns expected to be needed in each bias winding. Thus, large ratios $I_{b\ max}/I_{b\ min}$ make J_b large and require a physically large inductor. Once the most desirable bias-current adjustment has been determined, a compact power supply and a small inductor can be designed for the final circuit. The assumption $\Delta I_b = I_b/4$ is arbitrary, but has been found satisfactory with respect to both bias-current smoothing and physical size of the final-circuit inductor L_b.

Ordinarily, a considerable deviation of I_h from the trial-design value can occur before an effect in controlled-rectifier turn-on is noticeable. Thus, in the experimental adjustment of the bias circuit it is not necessary to maintain $N_{2b}I_b$ at precisely the value specified by Eq. 4-29. Even so, it is not certain that the other two bias-circuit objectives (adequately fast reset and near-minimum unit loss) can be achieved simultaneously with the desired rate of controlled-rectifier turn-on. Difficulties caused by limitations on the range of I_b or on the number of bias-winding turns can be met by redesign of the bias circuit. More fundamental difficulties may require reconsideration of the entire trial design. In particular, if adjusting $N_{2b}I_b$ to realize the trial-design I_h (within the allowable limits) leads to unreasonably fast or slow reset of L_2, a new design based on different controlled-rectifier turn-on rate may be in order. Unduly fast reset of L_2 increases the reset loss; the trade-off between this loss and increased loss in S_3 for lower I_h determines the optimum I_h. Slow reset of L_2 is a difficulty only if it prevents completing the reset cycle in the time allowed--or increases losses by requiring overly fast reset of the other saturable elements.

4. Experimental Design Evaluation

The foregoing trial design and detailed component designs provide the data necessary for construction of a breadboard model of the pulse-generator charging and output circuits. Operation and testing of this model is desirable to permit experimental adjustment of the bias circuit, pulse-forming network, C_1, and other elements, as well as to permit measurement of losses and over-all evaluation of performance. Design changes based on this evaluation may be made as necessary.

Measurement Instrumentation. For low-repetition-frequency checking of output pulse shape and bias-circuit performance, a d-c power supply can be used to charge C_1 through a large resistor R_{ch}. The current E_{C1}/R_{ch} should be five or ten times smaller than the holding current of S_3, so that S_3 can recover forward blocking capability between pulses. For partial-to-full-repetition-frequency testing, a high-power d-c supply can be used to charge C_1 through a resonant inductor and a suitable controlled rectifier.

The trigger source for S_3 should deliver a fast-rising current pulse of the maximum height allowed for S_3 and of a duration equal to T_h. It is advisable to arrange an interlock so that C_1 cannot be charged unless the bias current I_b is established.

A small hole drilled deep into the mounting stud of S_3 to accept a thermocouple junction facilitates measuring S_3 dissipation at higher repetition frequencies. With S_3 mounted in the pulse-generator heat sink and cooled in the same way as it will be when the pulse generator is operating, obtain a plot of S_3 power dissipation vs. steady-state junction-temperature rise above the cooling-medium temperature. To obtain this plot, trigger S_3 into the conducting state, and force various measured d-c currents I_J through the junction. Measure junction voltage drop E_J for each current; and calculate the power dissipated, $E_J I_J$. Stud temperature rise is determined from the stud thermocouple voltage, measured against a reference thermocouple immersed in the heat-sink cooling medium. When the pulse-generator is operated, the power-temperature plot is entered at the temperature rise for that operating condition, and the corresponding S_3 power

dissipation is read.

Sampling windings of two or three turns each can be placed around each saturable inductor core for viewing main-winding voltage waveforms. When the sampling winding voltage falls to zero, the core is reset. If a resistive load is used in preliminary testing, a series avalanche diode may be included for resetting L_3 (see Chapter III, Section A). A peak-reading voltmeter connected across C_1 is helpful in establishing the precise value of E_{C1} immediately prior to triggering S_3. Other instrumentation required is the same as used for conventional pulse-generator circuits.[1]

Test Procedure. Initial testing should be at a repetition rate of only a few pulses per minute. Check for the presence of an output pulse, and observe saturable-element sampling windings to determine the order in which the cores reset, and the reset times. Adjust bias current and bias-winding turns as discussed in Section 3, and check the degree of discharge of C_1 (minor adjustment may be needed to secure complete discharge), the charging time T, the hold-off time T_h, the guard interval T_g, the controlled-rectifier dissipation, and the output-pulse shape. Fine adjustment of C_1 or of pulse shape should not be attempted at this point, because the decrease of B_s that accompanies the core-temperature rise at full-power operation may influence the C_1 discharge and the output pulse, as well as decreasing T_h, T_g, and (if I_b is constant) the resetting times.

Once adequately fast resetting is obtained and the circuit operation is as desired in other respects, the repetition rate may be increased. If the expected controlled-rectifier dissipation is close to the safe maximum, a gradual increase in repetition rate while monitoring controlled-rectifier temperatures may be advisable--especially if current unbalance among rectifiers in parallel is possible. At the design-value repetition rate, final adjustment of C_1 and the pulse network can be made, the dissipation in S_3 can be measured, the effects of core heating can be assessed, and the attainment of design objectives

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[1] T.A. Weil, "Simple Techniques to Measure High-Power Pulses," Electronic Design, (Part I: Oct. 11, 1965, v. 13, no. 21; Part II: Nov. 8, 1965, v. 13, no. 23).

evaluated. Detailed performance measurements as required by the application can be made.

C. THE VOLTAGE REGULATOR AND POWER SUPPLY

Design of the voltage regulator circuit, shown schematically in Fig. 3.6, proceeds from specifications for E_{C1}, the repetition period T_r, and the characteristics of the prime-power source. The value of capacitor C_1, and the voltage E''_{C1} are known from the design and experimental evaluation of the output and charging circuits; it remains to choose controlled rectifiers S_1 and S_2, and to design inductor L_1.

It is assumed here that the prime-power source is an a-c power line, and that an unregulated d-c power supply that can be represented by the equivalent circuit of Fig. 3.10 is used between the line and regulator circuit. Given the expected range of prime-power-source voltage variations, select a turns ratio n_1 for inductor L_1 that, by Eq. 3.56d, yields a value of $\underline{a}$ somewhat larger than the power-source voltage range. (The regulation range a' of Eq. 3.62 that takes into account power-supply internal impedances is likely to be only slightly less than $\underline{a}$ and can be checked toward the end of the design process.) A value $n_1 = 3$ is typical where a regulation range approaching the maximum is required; larger values usually lead to large $L_{\ell 1}/L_1$, and correspondingly poor regulation.

Next, select a trial value of T_o that satisfies Condition 2 (see Eqs. 3.57a,b and c) and also provides sufficient time for L_2 to reset and for S_3 to recover forward-voltage-blocking capability. In low-repetition-frequency pulse generators, the trial T_o should be considerably less than the maximum allowable value because the smaller value makes L_1 smaller (and less lossy). However, too small a T_o increases dissipation in S_2, and makes regulation more sensitive to time delays in the voltage-level sensing circuit connected across C_1. The optimum T_o can be determined only by evaluating trial-design results.

Next, select a controlled rectifier for S_2 that satisfies the voltage requirements given in Table 3.1, and that can handle the worst-case current pulse. Since rms current increases and pulse duration decreases as θ decreases (see Chapter III, Section C.1), the worst case is $\theta = \theta_o = \sin^{-1} 1/[\, n_1(1+\gamma)+\gamma\,]$, where $\gamma = E''_{C1}/E_{C1}$. The corresponding rms current is the maximum of I_A in Table 3.2, or approximately $\pi Q_o/2\sqrt{T_o T_r}$ for large n_1 -- where $Q_o = C_1(E_{C1} + E''_{C1})$ -- and the pulse duration is $T_{\theta_o} = T_o(1/2 + \theta_o/\pi)$. Difficulty in satisfying the current requirement may necessitate increasing T_o. Protection of S_2 against high rates of voltage change and the associated danger of premature triggering can be had with a series diode and a shunt resistor (see diode D_2 and resistor R_2 in Fig. 5.1).

A switching device to satisfy the voltage (Table 3.1) and worst-case current requirements on S_1 should be selected next. A high-voltage diode in series with a controlled rectifier (with appropriate voltage-dividing resistors) is recommended for use as S_1 inasmuch as a reverse-voltage rating much greater than the forward-blocking-voltage rating is usually needed. Because the peak value and duration of the S_1 current pulse both increase with decrease of θ, the worst case is again $\theta = \theta_o$. The rms current (see Table 3.2) is then approximately $Q_o/\sqrt{n_1 T_o T_r}$, and the duration is approximately $T_o/\pi \sin\theta_o$.

When controlled rectifiers for S_1 and S_2 have been chosen, and a reasonable T_o duration determined, the design of L_1 can begin. The regulation capability of the circuit is set primarily by $L_{\ell 1}/L_1$; thus a major objective in the inductor design is very close coupling between the main winding and the auxiliary winding of n_1 times as many turns. Other requirements on the inductor are: (1) a main-winding inductance

$$L_1 = \frac{T_o^2}{\pi^2 C_1} \tag{4.34}$$

and (2) a stored energy at the peak of the current wave

$$J_{st} = \frac{1}{2} L_1 I_{Ap}^2 = \frac{[1/(1 + 1/n_1) + \gamma]^2}{1 - \gamma^2} J_c \qquad (4.35)$$

where $J_c = C_1 E_{C1}^2/2$ is the peak energy stored in C_1, (3) minimum possible loss--certainly small enough loss to prevent overheating, and (4) minimum size and weight.

Substantially the entire energy J_{st} must be stored in air gaps provided in the inductor core. Let ℓ_g be the length of each of n_g air gaps in the magnetic circuit, and let A_{eff} be the effective cross-sectional gap area that takes into account fringing. For small gap lengths A_{eff} is obtained by supposing each side of the cross section of the magnetic core to be increased by ℓ_g.

For a flux density B_g in the gap, the stored energy density is $B_g^2/2\mu_o$; thus the required air-gap volume is

$$n_g \ell A_{eff} = 2 \frac{\mu_o}{B_g^2} J_{st} \qquad (4.36)$$

Similarly, the inductance L_1 is determined almost entirely by gap flux and magnetizing force; the one-turn inductance is $\mu_o A_{eff}/\ell_g$, and

$$N_{1A}^2 = \frac{\ell_g}{\mu_o A_{eff}} L_1 \qquad (4.37)$$

where N_{1A} is the number of turns required on the main winding.

Equations 4.36 and 4.37 and the requirement that the auxiliary winding contain $N_{1B} = n_1 N_{1A}$ turns comprise the specific conditions to be met by inductor L_1. Within the limits allowed by these conditions, the inductor geometry, core material and peak flux density, and winding construction may all be varied to minimize leakage inductance, loss, size, and weight. The air-gap volume is related fundamentally to the total inductor size -- increasing A_{eff} increases the core cross section, whereas increasing ℓ_g increases the winding perimeter that must be provided (by Eq. 4.37, N_{1A} depends on ℓ_g). Thus minimum air-gap volume, or by Eq. 4.36, maximum B_g, is desired. In consequence, a peak flux density B_s in the magnetic material as large as saturation properties permit should be used. A linear inductor is

not required; therefore, it is not curvature of the B-H characteristic in itself that limits B_s, but rather the associated rapid increase of core loss with B_s. In fact, it can be shown that to obtain a minimum-loss inductor the core-material figure of merit that should be maximized is B_s^2/j_m -- where j_m is core loss per unit volume per cycle under the operating conditions of inductor L_1. Beyond the maximum B_s^2/j_m point in the saturation region, the loss per unit volume increases with B_s faster than the core volume is decreased by designing for higher B_s.

The first step in the design of L_1 is selection, from manufacturers' catalogs of cut cores, of a magnetic material, a lamination thickness, and a peak flux density B_s. The guide to this selection is maximization of B_s^2/j_m, and ideally data applicable to an elevated operating temperature anticipated for L_1 should be used. Practically, it may be necessary to base the material and lamination-thickness choices on lower-temperature data, and to estimate j_m from curves published for sinusoidal voltage excitation. (A reasonable estimate is T_{θ_o}/T_r times the loss at a frequency $1/T_{\theta_o}$, where T_{θ_o} is the minimum duration of the I_A pulse given above.) Rated B_s^o values may be used in choosing the material; for the selected material and lamination thickness, consideration of other B_s values may yield a minor reduction of B_s^2/j_m. The final determination of B_s for use in the inductor design should take into account a conservative (high) estimate of core temperature rise to be expected in inductor operation.

The next step in the inductor design is choice of an available core using the material selected. If the core cross-section dimensions are x and y, evaluating A_{eff} in Eq. 4.36 as $(x + \ell_g)(y + \ell_g)$ and B_g as $B_s xy/A_{eff}$ yields a quadratic equation in ℓ_g. Solving this equation determines ℓ_g, and hence N_{1A} and N_{1B}. Construction of windings of N_{1A} and N_{1B} turns on the selected core then yields the desired inductor.

A few general guidelines can be offered with respect to both core selection and winding construction. Usually, skin and proximity effects are of considerable importance, especially in the main winding. Thus, the useful winding depth is limited (see Chapter II, Section A.5), the winding should cover as large a fraction of the core perimeter as is

practicable, and a litz-wire winding (or even a single-layer winding if T_o is very short) should be considered. Proportioning of the main and auxiliary windings for equal effective current densities (rms currents divided by per-turn cross section as reduced by skin and proximity effects) and interleaving of the windings (to reduce leakage inductance) are generally desirable. However, the interleaving should be limited to interleaved layers of the two windings -- interleaved turns in a layer increase losses because insulation then occupies a larger fraction of the available winding length. The balance between core and winding loss can be adjusted by changing the magnetic path length but not the core cross section. A longer core increases core volume and loss, but decreases winding loss because of the greater core perimeter provided. If ℓ_g is small relative to core cross-section dimensions, decreasing the core cross section and simultaneously increasing the magnetic path length to maintain constant core volume provides a means of reducing winding loss without increasing the core loss. The winding loss is decreased because the perimeter available for the winding increases nearly in proportion to ℓ_g (provided ℓ_g is small; see Eq. 4.36), and hence more rapidly than N_{1A} (see Eq. 4.37).

Once the paper design of L_1 is complete, the inductor can be constructed and its performance evaluated. Operating L_1 with C_1 in a resonant-charging circuit connected to a dummy load provides a convenient means of measuring T_o and estimating the losses in L_1. The circuit should be adjusted for a peak charging current I_{A_1}. Energy lost in L_1 is the major circuit loss and may be estimated from the relation of the maximum C_1 voltage to the input voltage. The test may be performed at any convenient repetition rate, but a full-power test at the pulse-generator rate and lasting for several hours is especially useful. It provides a means of determining whether or not L_1 will overheat and also gives a measure of losses under actual elevated-temperature operating conditions. The leakage inductance $L_{\ell 1}$ can be determined by measuring the winding-A inductance with winding B short-circuited. On the basis of the test results, the design of L_1 may be accepted, or a new design attempted, possibly beginning with altered n_1 or T_o values.

To complete the pulse-generator input section, a rectifier-filter power supply and a stop-trigger generator must be designed. The design of the power supply is conventional, except that the effects of internal resistance R_o, filter inductance L_o, and filter capacitance C_o on the over-all regulation, regulation range $\underline{a}'$, and stability must be taken into account as outlined in Chapter III, Section C.2. The values of over-all regulation and regulation range that can be achieved provide a final test of the acceptability of the regulator design. One possible circuit for the stop-trigger generator is indicated in Fig. 5.1. Any alternative circuit that performs the function of producing a trigger pulse for S_1 with the shortest possible delay, after e_{C1} reaches the desired value E_{C1}, may be used. The voltage reference in this circuit must, of course, be stable within narrower limits than those required of E_{C1}.

The complete power-supply-and-regulator circuit can be tested with C_1 and the same dummy load used in testing L_1. Regulation, regulation range, and efficiency can be measured. If satisfactory, this input circuit can be combined with the previously tested charging and output circuits for the final evaluation of the complete pulse generator.

CHAPTER V

EXPERIMENTAL PULSE GENERATOR

Several experimental semiconductor-magnetic pulse generators have been designed, constructed and tested in this Laboratory. The results of one such effort are described in this chapter.

The development of this particular circuit paralleled the development of much of the present theory behind its operation, and was instrumental in helping to establish and solidify the theory presented in the preceding chapters. For this reason, the circuit described in this chapter is conceded not to be the best design that can be achieved now, in light of present understanding of the circuit behavior. Nevertheless, it does serve as a valuable example of what has been achieved in physical and electrical characteristics with the basic circuit design that is the subject of this report.

A. SPECIFICATIONS AND SUMMARY OF RESULTS

The following parameters were taken as arbitrary design goals:

Peak output-pulse power, P_p	1 megawatt
Peak output-pulse voltage, E_p	10 kv
Average output power, P_{av}	2 kw
Pulse duration (at 50-percent voltage amplitude)	1.7 microseconds
Repetition frequency	1200 pulses per second
Load resistance, R_L	60 ohms, resistive
Over-all efficiency	80 percent
Prime power	208v, 400 cps, 3 phase

Because no definite application was involved, rigorous specifications were not placed on rise and fall times of the output pulse nor upon pulse jitter. In the design of the pulse-forming network, a parabolic-shaped waveform with $\delta = 0.25$ (see Chapter III, Section A.1) was assumed for the pulse front edge. Since all-magnetic modulators have been the subject of much criticism in the past because of susceptibilitv to pulse jitter (see Chapter I, Section A), one goal of the experimental effort was to demonstrate with the experimental circuit that an essentially jitter-free train of output pulses could be achieved. Output-pulse

jitter was less than 5 ns for power-line voltage fluctuations prevailing in the laboratory (see Section B.2). The experimental pulse generator essentially met the balance of the design goals. The actual pulse generator exceeded the peak power output which was set for the unit; the average power was somewhat less. The following characteristics were measured at a repetition rate of 1 kc:

Output-pulse power, peak P_p	1.1 megawatt
Output-pulse voltage, E_p (Average value)	9.1 kv
Average output power, P_{av}	1.77 kw
Pulse duration (at 50-percent voltage amplitude)	1.7 microseconds
Repetition frequency	1000 pulses per sec
Power supply efficiency	96 percent
Over-all efficiency	70 percent
Output-pulse jitter	less than 5 nanoseconds

The experimental pulse generator was operated for a total of 290 hours. Operation was at full output power except for short intervals while calibrations and adjustments were being made at reduced repetition frequency. During the test, the unit was instrumented so that electrical quantities could be measured and temperatures at critical points monitored. Testing was interrupted several times during the 290-hour interval; the longest continuous run was 137.2 hours. Although circuit operation became intermittent near the end of the test period, the unit operated failure-free for a period of 200 consecutive hours, and the failure that then occurred was forward breakdown of a controlled rectifier known to have been damaged before the test began, (see Section D).

B. CIRCUIT DESCRIPTION AND PERFORMANCE

The basic circuit of Fig. 1.3 can be realized in many configurations. Distinguishing features of the configuration used in the experimental pulse generator are described in this section, followed by waveform photographs illustrating circuit performance.

1. Circuit Description

The over-all circuit of the experimental pulse generator is given in Fig. 5.1, and a photograph of the breadboard unit, as set up for test,

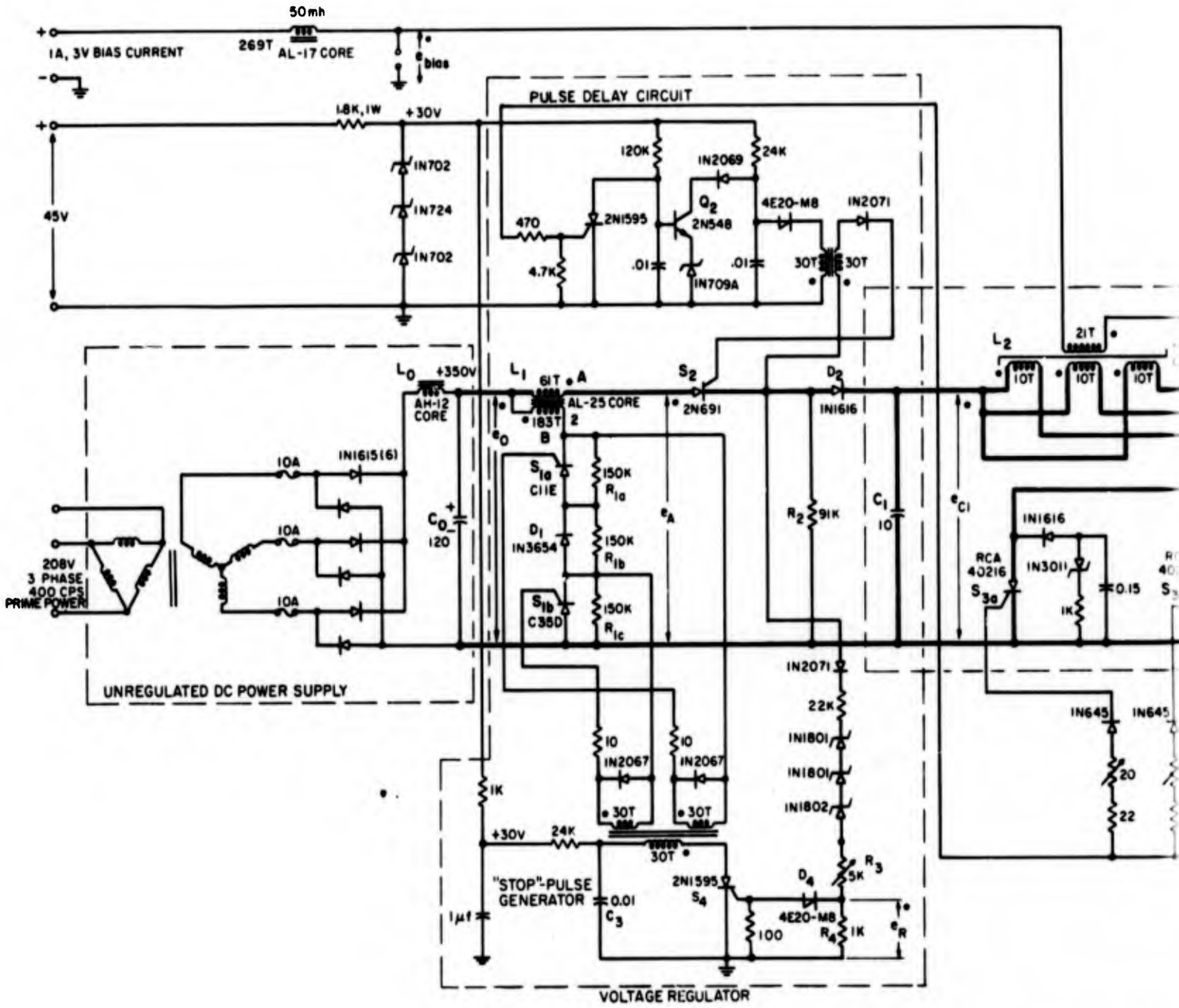
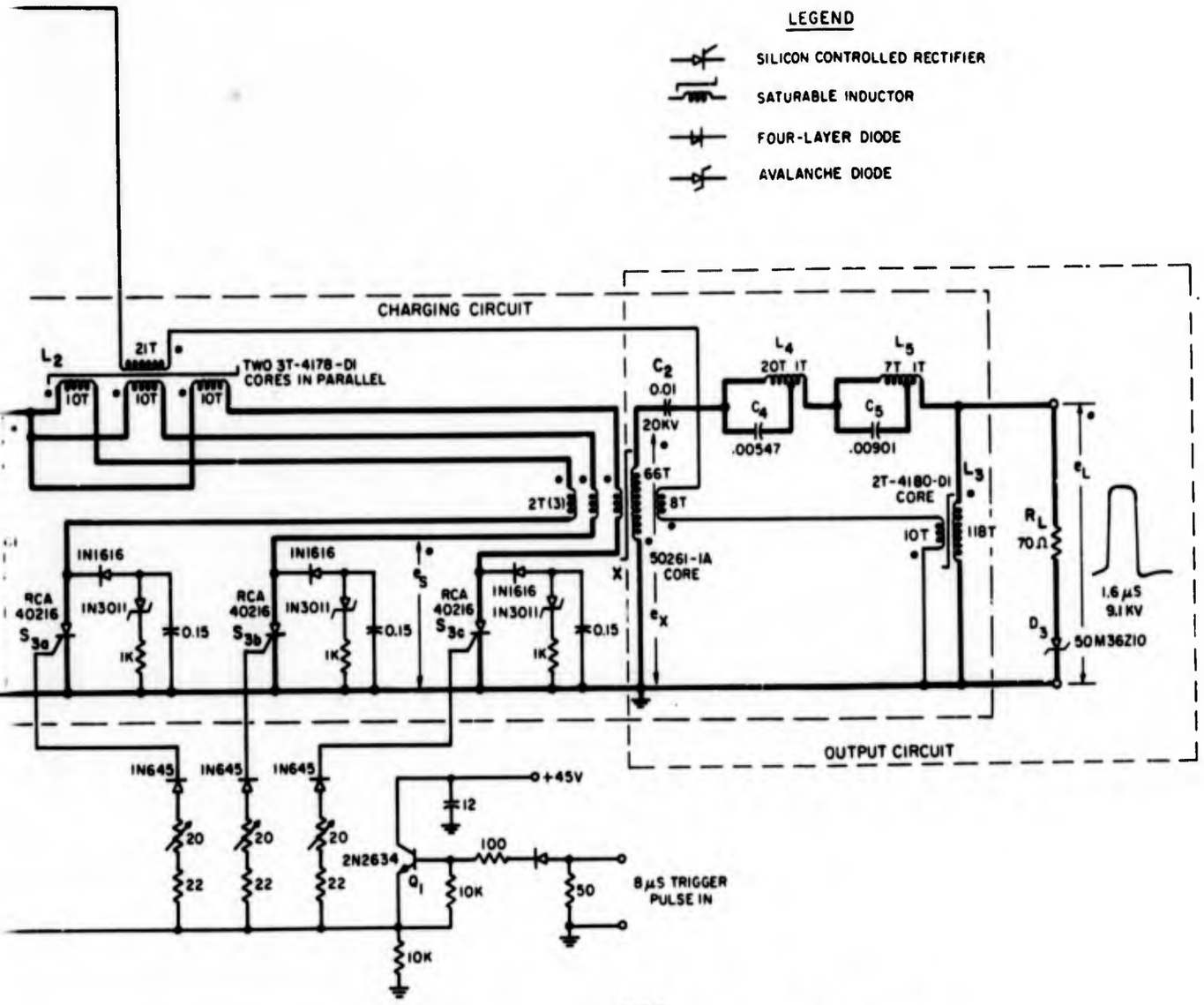


Fig. 5.1 Experimental Pulse Gener

A



NOTE:
ALL RESISTANCE VALUES IN OHMS
ALL CAPACITANCE VALUES IN MICROFARADS

perimental Pulse Generator

B

is shown in Fig. 5.2. The configuration of key components in the experimental circuit (shown in Fig. 5.1 as connected by heavy lines) is essentially the same as in Fig. 1.3. Diode inductor L_3 is connected directly across the 70-ohm resistor load. Avalanche diode D_3, in series with the load, permits resetting voltage (approximately 36 v) to be developed across L_3 without requiring large reset current through R_L (see Chapter III, Section A); the voltage drop across D_3 is negligible during the output pulse. A three-section, Type A pulse-forming network is comprised of high-voltage capacitor C_2, the resonant circuits formed by C_4 and L_4 and C_5 and L_5, and the saturated inductance L_{X2} of the high-voltage windings of Transformer X. Taps on the windings of L_4 and L_5 permit minor adjustments in output pulse shape.

Voltage step-up from E_{C1} = 660 v to $2E_p$ = 18.2 kv is provided entirely by saturable transformer X. One end of each of three separate low-voltage windings on X is connected to the anode of each of the three controlled rectifiers (S_{3a}, S_{3b}, and S_{3c}) that make up S_3. The other transformer low-voltage winding connections are to three separate windings on hold-off inductor L_2. The diode, resistor, and capacitor network across each S_3 controlled rectifier is included to prevent any reverse currents that might occur during experimental adjustments from damaging the rectifiers; experience has proven that the network is not needed. Trigger pulses for S_3 are derived from a high-current emitter follower Q_1 and fed to the controlled-rectifier gates through a diode-resistor network that assures precise gate-pulse current-amplitude control--each S_3 gate-current pulse is of 800-ma peak amplitude.

The voltage-regulator circuit is connected to C_1 through diode D_2. When voltage-regulator action turns S_2 off, the voltage E_{C1} across C_1 is blocked by D_2, and the cathode of S_2 is returned to ground through resistor R_2. Thus, D_2 and R_2 prevent the rapidly changing C_1 discharge-voltage transient that occurs during the charging interval T from appearing across S_2, so that misfire of S_2 during T is avoided.

The stop-pulse generator delivers trigger pulses to controlled rectifiers S_{1a} and S_{1b} when the charging voltage on C_1 reaches the regulation value E_{C1}. The instantaneous voltage on C_1 is sensed

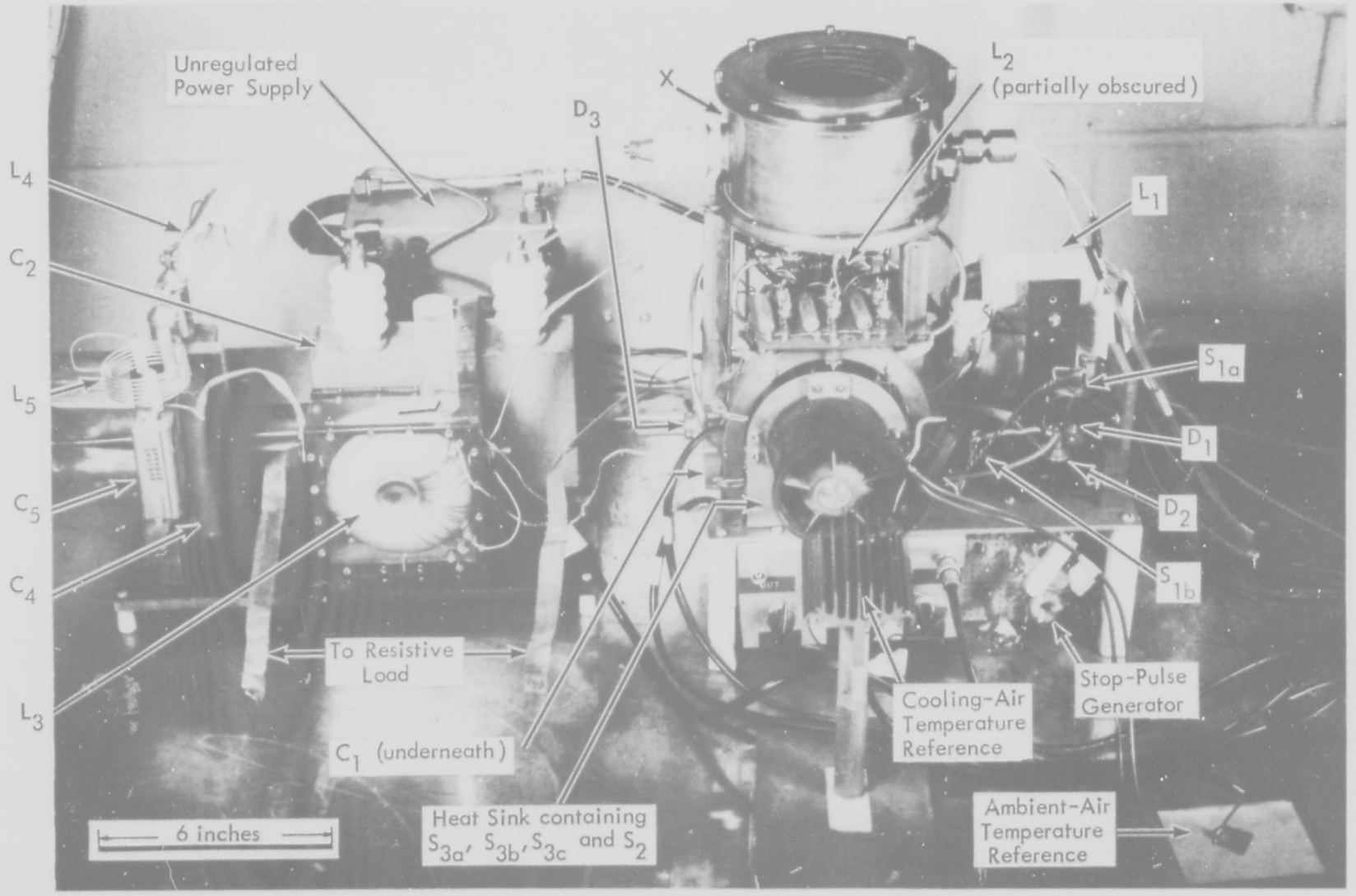


Fig. 5.2 Breadboard Circuit for Life Test

through D_2 by a string of avalanche reference diodes and current-limiting resistors. The magnitude of regulation voltage E_{C1} is adjusted by potentiometer R_3, which sets the current level in the sensing circuit. Four-layer diode D_4 conducts when the voltage across resistor R_4 reaches the diode firing voltage (approximately 20 v), and a gate pulse is delivered to S_4. Capacitor C_3 discharges through S_4 and the primary winding of a pulse transformer; a pair of identical windings on the pulse-transformer secondary delivers the stop-trigger pulses to the gates of S_{1a} and S_{1b}.

Diode D_1 absorbs one-third of the reverse voltage appearing between point B and ground during the beginning of the C_1 charging cycle to lower the inverse-voltage requirements on S_{1a} and S_{1b}. Voltage-equalizing resistors assure that leakage-current differences among D_1, S_{1a}, and S_{1b} do not influence the division of voltage across them.

The unregulated d-c power supply comprises an output capacitor C_o, filter choke L_o, 3-phase full-wave diode bridge rectifier, and 3-phase power transformer. Prime power is drawn from a 400-cycle, 3-phase line.

The pulse-delay circuit is adjusted to provide a trigger pulse to S_2 to initiate charging of C_1 after S_3 recovers forward blocking capability. The delay circuit is activated by the same trigger pulse that is supplied to S_3, and approximately 170 μs later generates the S_2 trigger pulse.

Bias current is provided by a 3-volt, 1-amp d-c supply. The 50-millihenry bias inductor maintains current constant to within about 25 per cent; winding turns are insulated to withstand the maximum total voltage appearing across the series-connected bias windings -- for this circuit, approximately 1500 v.

The major components, with the exception of C_1, are visible in Fig. 5-2. The pulse-forming network and diode inductor together weigh 12.5 lb. Weights of some of the components on the regulator and charging-circuit chassis (28.4 lb.) and the power-supply chassis (20.2 lb.) are believed to be higher than necessary. In light of present understanding of the circuit-design procedure, and from the experimental data gathered on components during the tests, weight reduction in at least the following two components could be made without sacrificing performance;

Saturable Transformer X: The brass housing, which weighs nearly 10 lb., was designed to accomodate a much higher transformer temperature rise than was actually experienced. A major reduction in size of the oil-expansion bellows, accompanied by an over-all reduction in the case size, would save 5 to 7 lb.

400-cps Power Transformer: This unit was made to withstand the abuse typical of an experimental circuit-development program, and is generously over-designed by between 5 and 8 lb.

2. Circuit Performance

Waveforms of voltage across the output terminals are shown in Fig. 5.3.* The times labelled on the photographs are measured with respect to the leading edge of the S_3 trigger pulse, where t = 0. In Fig. 5.3(a), the prepulse voltage E_1 falls to -1400 v shortly after the beginning of the charging interval T, and rises to approximately +800 v immediately prior to saturation of X and the start of the output pulse. Peak current in L_3 during the charging interval is approximately 45 amp. Figure 5.3(b) shows more clearly the shape of the output pulse; the leading edge occurs approximately 10.7 μs after the leading edge of the S_3 trigger pulse. The guard interval T_g for this circuit is zero. Smaller voltages appearing across the output terminals during resetting of X and L_3 are shown in Fig. 5.3(c). As confirmed by other measurements (see Chapter IV, Section B.4), transformer X resets approximately 100 μs after t = 0; in Fig. 5.3(c), transformer reset is accompanied by a jump in e_L from approximately -36 v (the avalanche-diode voltage) to zero. The jump occurs when residual energy on C_2 is discharged through the load by reset saturation of X. Twenty microseconds later, e_L jumps back to the avalanche-diode voltage where it remains until L_3 is reset. Notice the appearance

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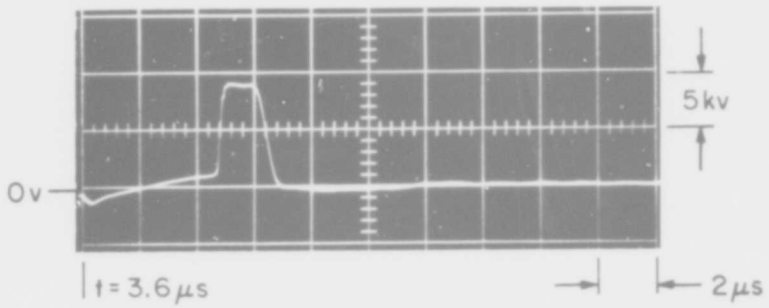
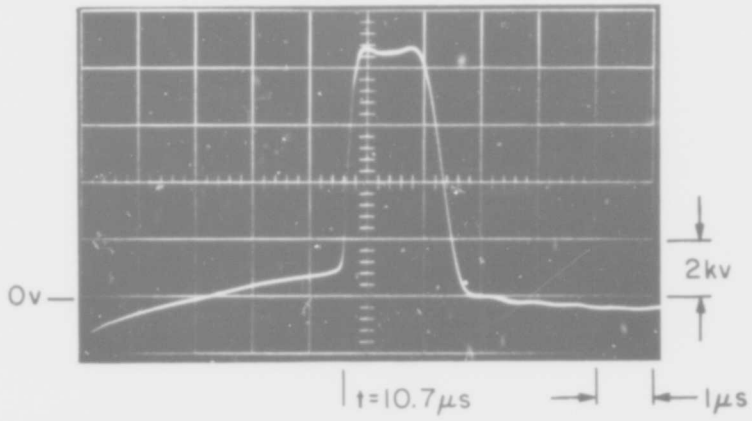
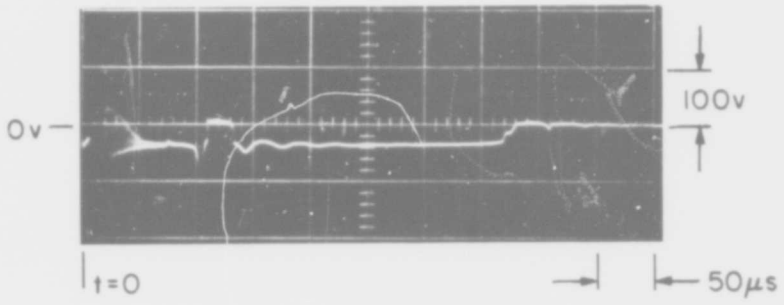
* For all the waveforms shown in the chapter, scales are labelled according to oscilloscope nominal vertical-gain and time-axis settings. Parallax error in some of the photographs gives the appearance that peak voltages are lower than stated. In the transformation of oscilloscope-waveform information to design and performance values, all measurements have been corrected for parallax error.



a) Output Pulse, Showing E_1



b) Output Pulse Shape



c) Resetting Voltages

Fig. 5.3 Load-Voltage e_L Waveforms

after t = 400 microseconds of small, triangular-shaped pulses of rapidly diminishing amplitude, a sign that minor setting and resetting of X and L_3 occur after major reset is complete (see Appendix A, Section 1). Other measurements indicate that no additional voltage appears across the load for the remaining 500 μs of the repetition period, confirming that both L_3 and X are completely reset.

The voltage e_X across the high-voltage winding of X (see Fig. 3.1) is shown in Fig. 5.4 for the 50-μs period following the triggering of S_3. The voltage falls from zero at the end of the hold-off interval (t = 5.1 μs) to -18.2 kv at the end of the charging interval. The transformer core saturates at t = 10.7 μs to switch the pulse-forming network across L_3 and the load. Residual energy stored in the network after the output pulse interval is dissipated during the subsequent ringing.

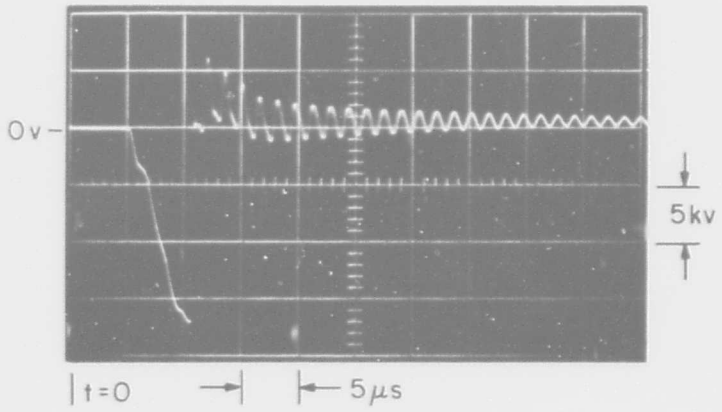
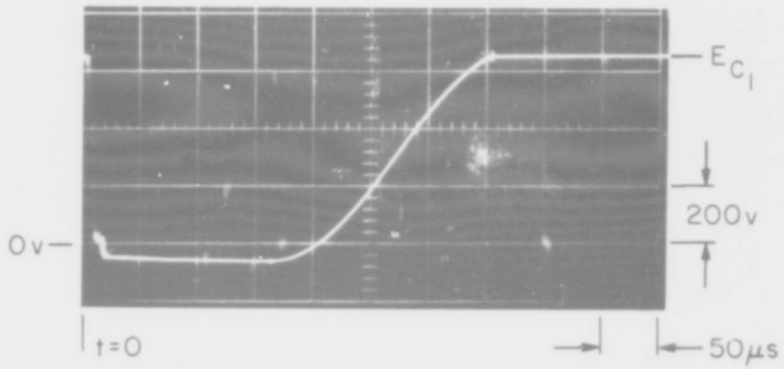
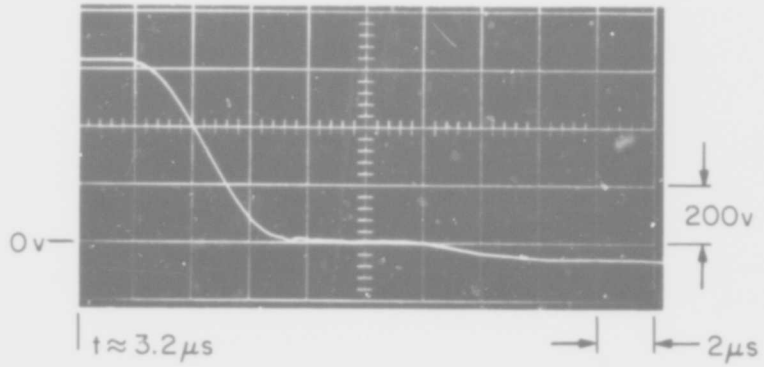


Fig. 5.4 Voltage e_X (Across Transformer High-Voltage Winding)

Figure 5.5a shows the discharge and charging of capacitor C_1 (see Fig. 3.5). Here E''_{C1} (see Fig. 3.7) is seen to be approximately 55 v; E_{C1} is set at 660 v. The shape of the discharge waveform is more evident in Fig. 5.5(b). The small negative jump in e_{C1} at the start of the charging interval T is caused by capacitor self inductance. Note that the charging interval T measures about 5.6 μs. Shortly after the end of the charging interval the voltage across C_1 begins to go negative, as L_2 begins resetting.



a) Discharge and Charging Waveform



b) Discharge Waveform

Fig. 5.5 Capacitor C_1 Voltage e_{C1}

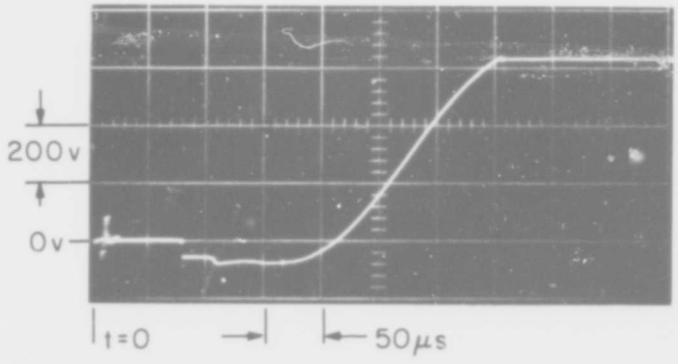


Fig. 5.6 Voltage e_S across S_{3C}

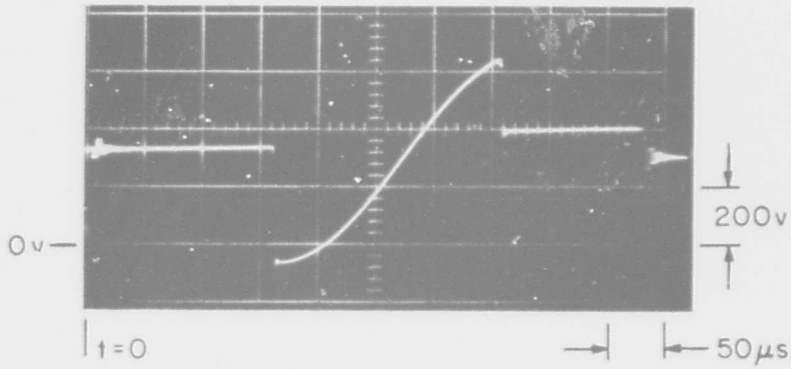
As shown in Fig. 5.6, S_3 remains conducting after the discharge interval until $t \approx 80\ \mu s$; the abrupt negative jump in S_3 voltage at this time indicates that L_2 has completed reset, and S_3 has turned off. Each of the three S_3 controlled rectifiers passes a half-sine current pulse of 615 amperes peak amplitude during the charging interval. Figure 5.6 shows that the voltage across S_3 during the current pulse reaches a maximum of +80 v, the combined effect of rectifier forward resistance and inductance of the rectifier and associated connections.

Voltage-regulator action is illustrated by the waveforms of Fig. 5.7, which have their idealized counterparts in Fig. 3.7. Figures 5.7(a) and (b) show the action of L_1 at terminals A and B. At $t = 170\ \mu s$, charging of C_1 begins when the pulse-delay circuit triggers S_2 into conduction. The charging of C_1 is interrupted by regulator action at $t \approx 360\ \mu s$. The voltage e_R across R_4 in the stop-pulse generator is shown in Fig. 5.7c. The positive-going, ramp-like portion of the waveform begins after the avalanche diodes in the sensing circuit conduct; the voltage goes to zero when four-layer diode D_4 fires, triggering S_4. Jitter in the latter portion of the e_R waveform indicates that the prime-power source voltage is fluctuating; this fluctuation is compensated by the regulator as it lengthens or decreases the duration of the C_1 charging period as required to charge C_1 to E_{C1} volts.

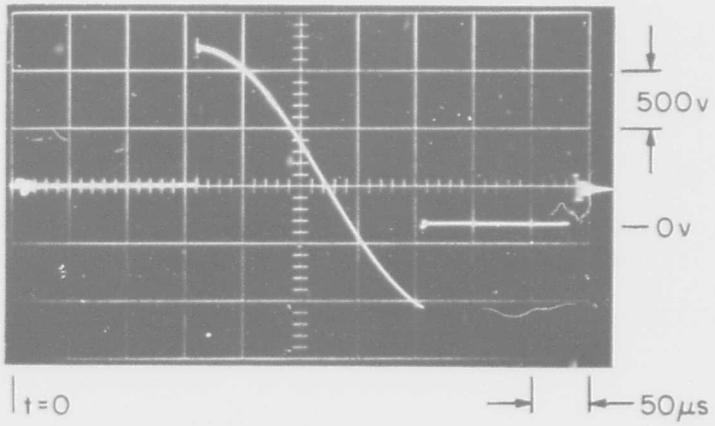
Measured characteristics of the voltage regulator, with R_3 adjusted to give $E_{C1} = 612.5$ v, are shown in Fig. 5.8. Similar characteristics apply for R_3 set to give $E_{C1} = 660$ v. For E_o between 340 and 400 v, $e_{C1\ max}$ changes a total of 7.5 v. Hence, the regulation, as defined in Eq. 3-59, is $\Delta E_{C1}/\Delta E = 7.5/60 \approx 0.12$, or 12 per cent. The regulation range a was not measured, but is more than adequate to accommodate the range of voltage variation exhibited by the laboratory prime-power source.

Power-supply output voltage e_o is shown in Fig. 5.9 over two output-pulse repetition periods. The voltage decreases during charging of C_1 (starting at $t = 170\ \mu s$, $1170\ \mu s$, ...), and rises slowly during the remainder of each repetition period, when the regulator is disconnected from C_1.

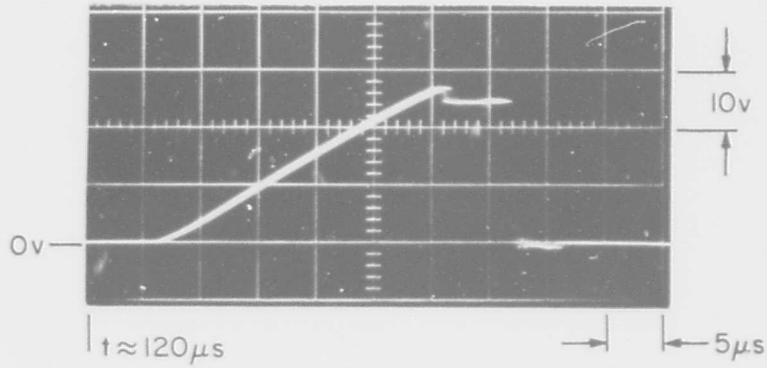
The voltage across bias inductor L_b during the guard, charging, and pulse intervals is shown in Fig. 5.10. No significant voltage is present throughout the remainder of the repetition period.



a) Voltage e_A



b) Voltage e_B



c) Voltage e_R

Fig. 5.7 Regulator-Circuit Voltage Waveforms

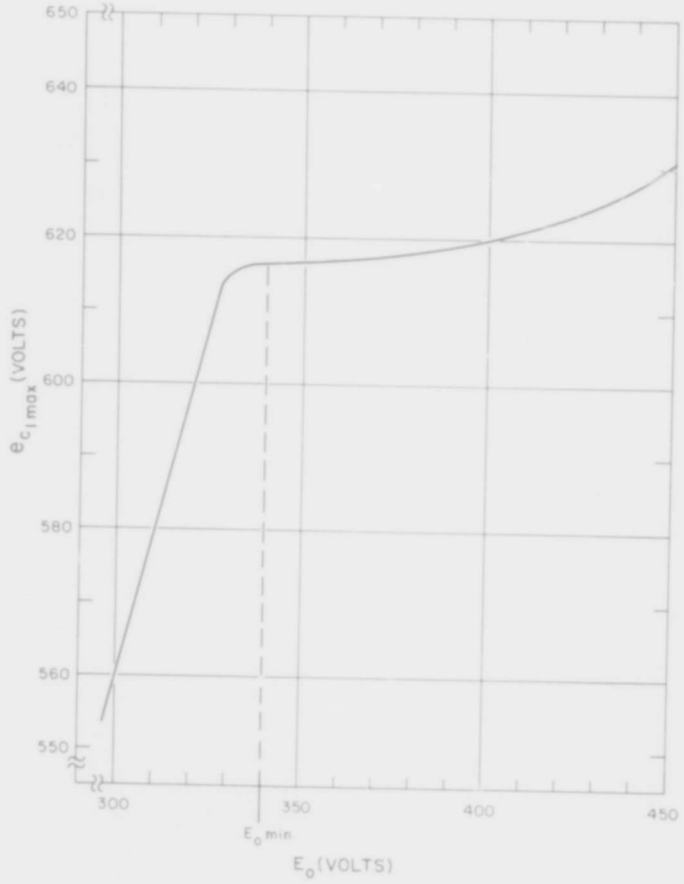


Fig. 5.8 Measured Regulation for E_{C1} = 612.5 V

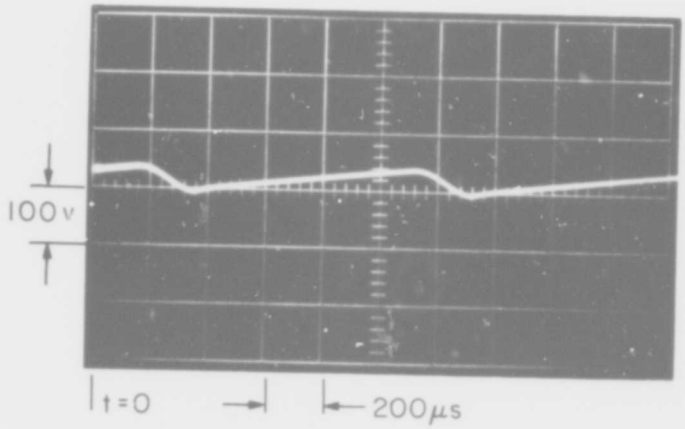


Fig. 5.9 Power-Supply Output Voltage e_o

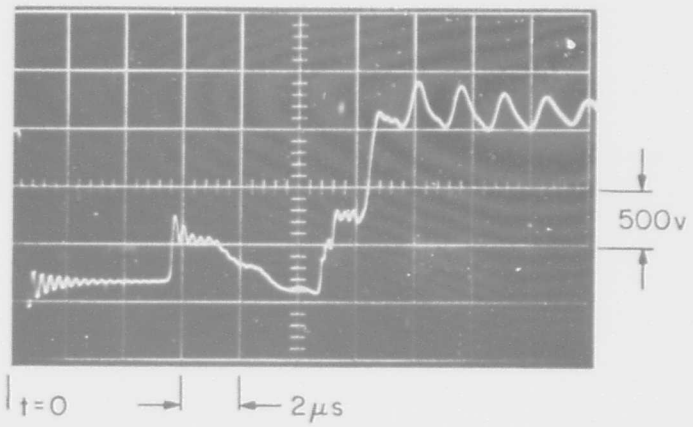


Fig. 5.10 Bias inductor L_b Voltage e_b

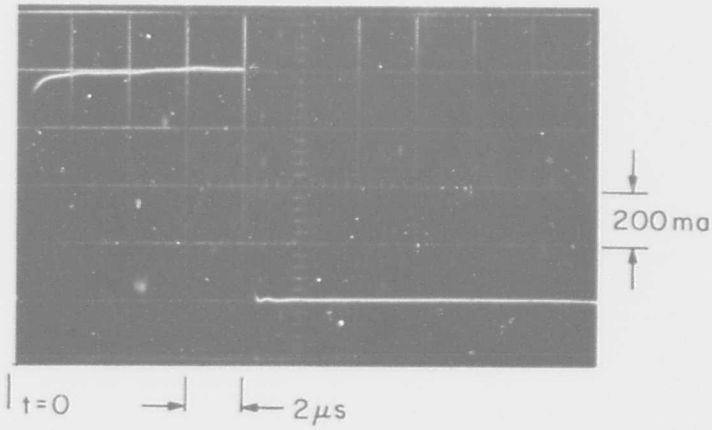


Fig. 5.11 Gate-Current Pulse for S_{3a}

The gate-current pulse used to trigger each controlled rectifier in S_3 resembles that shown in Fig. 5.11 for S_{3a}. Here the peak amplitude of 800 ma is the maximum allowable for the controlled rectifier; the 8-μs duration is unnecessarily long and need be only about 6 μs, or slightly longer than T_h.

C. COMPONENT CONSTRUCTION AND SELECTION

The circuit components of major interest in the experimental breadboard circuit are the saturable-core magnetic elements L_3, X, and L_2, linear charging inductor L_1, and the controlled rectifiers used for S_3. Constructional details for the magnetic elements are presented in this section, along with a brief discussion of some aspects of

controlled-rectifier selection.

1. Diode Inductor L_3

Specifications for diode inductor L_3 are summarized in Table 5.1; the completed unit, immersed in transformer oil, is shown in its plastic housing in Fig. 5.2. Both the λ_3 and L_3 measurements given in the table were made in a circuit similar to the one described in Appendix B. The λ_3 value is for room temperature; at operating temperature it is only slightly less.

The 2T4180-D1 core case is aluminum; it was selected before eddy-current losses in such cases were observed to be a problem Because total losses in L_3 were found to be small, as indicated by temperature-rise measurements (see Section D), the inductor with the metal-cased core was used in the extended circuit tests even

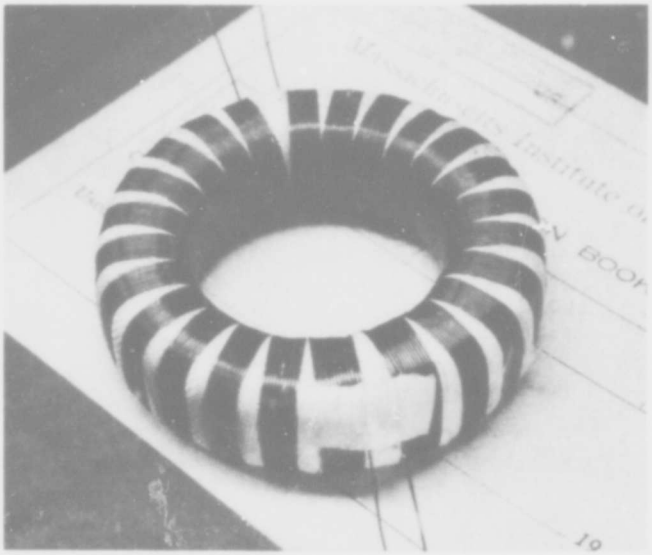


Fig. 5.12 Diode Inductor L_3 High-Voltage Winding Construction

though losses in this component could be reduced somewhat by eliminating the metal case.

The diode-inductor main-winding configuration conforms to the recommendations of Chapter IV, Section B.3. Figure 5 12 is a photograph of the partially constructed inductor, showing the main winding split into two identical halves to provide 180-degree

Table 5.1

Experimental Saturable Inductor L_3

MEASURED VALUES	
λ_3	2.04×10^{-2} volt-seconds
L_3	29.3 microhenries
MAGNETIC CORE	
Type	2T4180-D1 (Arnold Engineering Co.)
Material	Deltamax (50-percent-nickel iron)
Lamination thickness	1 mil
V_3	1.32×10^{-5} cu m
A_3	6.05×10^{-5} cu m
ℓ_3	0.219 m
MAIN WINDING	
N_3	118 turns, No. 24 wire
Configuration	See Fig. 5.12
Winding to core case insulation thickness	Approximately 100 mils
BIAS WINDING	
N_{3b}	10 turns, No. 16 wire
Bias-winding to main-winding insulation thickness	Approximately 150 mils
TRANSFORMER OIL	Dow-Corning 200 fluid

separation between high and low-voltage terminals. Note that the inner diameter of the insulated toriod is wound with all turns touching. Insulation thickness is built up with plain, 7-mil-thick fiberglas tape. The completed inductor is vacuum impregnated with low-viscosity silicone transformer oil, and operates completely immersed in it.

2. Transformer X.

Characteristics of transformer X are listed in Table 5.2. Measurement of λ_X was at room temperature. In operation, λ_X decreases to approximately 0.056 v-sec as transformer losses heat up the core. The 50261 core has a phenolic composition case, selected to eliminate metal-case eddy-current losses. Enough holes are drilled in the case to admit impregnating transformer oil and avoid any entrapment of air. The core was purchased without the usual silicone shock-absorbing grease to prevent contamination of impregnating transformer oil. Construction of the high-voltage winding is similar to that of L_3. A thermocouple junction was inserted in the high-voltage winding at the grounded end for monitoring internal temperature. Turns of the three multifilar low-voltage windings are spread out to cover as much as possible of the toroid circumference to minimize leakage inductance between them and the high-voltage winding. The completed transformer is vacuum impregnated with transformer oil. Figure 5.2 shows the completed unit in a brass housing. A bellows in the top of the housing is designed to accommodate oil expansion corresponding to oil temperature of 250 C, based upon performance of a previous transformer. Because of the nonmetallic core, transformer losses were much less than in the unit it replaced (see Section D), and oil temperature stayed well below the anticipated rise.

3. Hold-off Inductor L_2

The hold-off inductor, barely visible in Fig. 5.2 behind the controlled-rectifier heat sinks and under the brass housing for transformer X, is described in Table 5.3. The three main windings, positioned as in Fig. 4-3, are placed on a pair of identical cores that

Table 5.2

Experimental Saturable Transformer X

MEASURED VALUES	
λ_{X2}	6×10^{-2} volt-seconds
L_{X2}	32 microhenries
MAGNETIC CORE	
Type	Type 50261 (Magnetics, Inc.)
Material	Orthonol (50-percent-nickel iron)
Lamination Thickness	1 mil
V_X	6.91×10^{-5} cu m
A_X	3.02×10^{-4} sq m
ℓ_X	0.23 m
HIGH-VOLTAGE WINDING	
N_{X2}	66 turns, No 19 wire, bifilar wound
Configuration	As in Fig. 4.2
Winding to core case insulation thickness	Approximately 110 mils
LOW-VOLTAGE WINDINGS	
N_{X1}	Three separate windings, 2 turns each, wound with 7 strands No. 16 wire
Low-voltage to high-voltage interwinding insulation thickness	Approximately 110 mils
BIAS WINDING	
N_{Xb}	8 turns, No. 16 wire
Bias to low-voltage winding insulation thickness	Approximately 7 mils
TRANSFORMER OIL	Dow-Corning 200 fluid

Table 5.3

Experimental Saturable Inductor L_2

NUMBER OF MAIN WINDINGS	3
VOLT-TIME INTEGRAL λ_2	3.3×10^{-3} volt-seconds (measured)
SATURATED INDUCTANCE L_2	0.32 microhenries each winding, for equal currents in all windings (calculated)
MAGNETIC CORE	
Number	2
Type	3T 4178-D1 (Arnold Engineering Co.)
Material	Deltamax (50-percent-nickel iron)
Lamination Thickness	1 mil
V_2	2.18×10^{-5} cu m
A_2	1.21×10^{-4} sq m
ℓ_2	0.18 m
MAIN WINDINGS	
Number	3
N_2, each section	10 turns, No. 16 wire, trifilar wound
Configuration	See Fig. 4-3
Insulation	Formvar coating on wires
BIAS WINDING	
N_{3b}	21 turns, No. 16 wire
Insulation	Plastic coating on wire

are taped together and wound as one core. Each main winding comprises three strands of No. 16 wire. Construction is open, as insulation requirements are met easily with the enamel coating on the main winding turns and the extruded plastic coating on the bias winding.

In this inductor design, the total current I_h supplied to each rectifier during the hold-off interval T_h is approximately 2.2 amp; magnetizing current drawn from C_1 is 1.6a, and the balance of 0.6 amp. is reflected bias-winding current.

4. Charging Inductor L_1

Design of the experimental two-winding charging inductor, described in Table 5.4, involved a compromise between skin-effect winding

Table 5.4

Experimental Linear Inductor L_1

MEASURED INDUCTANCE L_1	0.535 microhenries
MAGNETIC CORE	
Type	AL-98 (Arnold Engineering Co.)
Material	Silectron
Lamination thickness	4 mils
A_1	3.59×10^{-4} sq m
ℓ_g	0.535 cm
Core weight	1.81 lb
WINDING A	
N_{1B}	183 turns, No. 19 wire, bifilar wound
Configuration	Single layer
Winding-to-core insulation	Teflon tape
WINDING B	
N_{1B}	183 turns, No. 19 wire
Configuration	Single layer
Interwinding insulation	Teflon tape

losses on the one hand and a large value of leakage inductance L_1 on the other. The relatively large leakage inductance (6.8 μh) exhibited by the experimental unit is largely the result of constructing both windings in single layers to minimize skin-effect copper losses. Since this component was constructed, a more thorough understanding of winding losses has been gained; it is now felt that substantial improvement in design of L_1 is possible through use of litz wire of appropriate size (to reduce losses) and the interleaving of windings A and B (to reduce leakage inductance, thereby improving the regulation attainable by the voltage regulator).

A high operating temperature was anticipated in the construction of L_1. Insulation on the magnetic wire used in both windings was chosen to withstand 150 C continuous service; insulation between winding A and the core, and between windings as well, is Teflon sheet. The spacers in the magnetic path that set the air-gap length are Teflon blocks.

5. Controlled Rectifiers S_{1a}, S_{1b}, and S_{1c}.

The controlled rectifiers used for S_3 are selected RCA Type 40216 units, exhibiting leakage currents of less than 1 ma at 125 C and at 700 v forward blocking voltage. The acceptability of these units for the experimental pulse generator was determined experimentally; these units operated cooler than any of the other types tested at the time (December, 1963) the selection was made. The effect of hold-off inductor action on controlled-rectifier power dissipation in this circuit is to increase the power switching capacity of the rectifiers by approximately 50 per cent. Using manufacturer's data for calculating device power dissipation, the charging current waveform (half-sine pulses, 615 a peak, 5.6 μs duration, 1,000 per sec) would lead to 42 watts rectifier dissipation in the absence of the hold-off inductor, or some 12 watts higher than the maximum dissipation set by the manufacturer. By comparison, the average dissipation measured in the experimental circuit was approximately 27 watts.

The three S_3 controlled rectifiers are operated in a blower-cooled heat sink that exhibits 0.8 C per watt thermal resistance to ambient air. Thus, maximum rectifier mounting-stud temperature during

operation at 25 C ambient was held below 50 C.

D. TEST PROCEDURES AND RESULTS

The experimental pulse generator was operated for a total of 290 hours. During this period, the circuit delivered full output power for all except the first few hours while preliminary measurements and adjustments were made. Temperature rise above room temperature ambient air was monitored continuously, by means of thermocouple junctions and a multichannel recorder, at the following points: exterior of the diode-inductor housing, in one Teflon air-gap spacer in the core of L_1, in the main winding of saturable transformer X, and in the oil in the saturable transformer-housing. Power dissipation in each of the controlled rectifiers S_{3a}, S_{3b}, and S_{3c} was measured with thermocouples inserted in holes drilled in the studs, and calibrated as described in Chapter IV, Section B.4. A peak-reading voltmeter across C_1 provided a constant check on the value of E_{C1}. Voltage waveforms were observed with a broadband oscilloscope and a variety of compensated high-voltage probes.

Initial operation was at a repetition rate of less than one pulse per second. As soon as the presence of an output pulse was confirmed, the rate was raised to approximately 10 pulses per second, and saturable-inductor resetting waveforms were taken. Minor adjustments in bias current and bias-winding turns were made to achieve the proper order and duration of resetting. The repetition frequency was gradually increased to 1000 pulses per sec over a period of a few hours, during which time critical temperatures, voltages, and voltage waveforms were examined carefully for signs of operational difficulty. At the 1-kc rate, it was observed that one of the three controlled rectifiers was dissipating the maximum allowable power; this established 1 kc as the maximum repetition rate for testing.

Output-pulse energy was calculated from the load-voltage waveform to be 1.77 joules per pulse (1770 average watts), and the average power delivered by the power line to the d-c power supply was measured at 2,540 watts, giving an over-all circuit efficiency of approximately 70 per cent.

Short-term pulse jitter was measured between the leading edges of the trigger and output pulses at less than 5 nanoseconds, peak-to-peak, in the face of normal fluctuations of the 400-cps line voltage. From Eq. 3-52 and the measured values of regulation, Th, and T, the output jitter as a function of prime-power supply-voltage changes dE is approximately

$$|dT_d| = (10.7 - 5.6/2)(0.12)\frac{dE}{12} \approx 0.95\frac{dE}{E}\ \mu s$$

For example, if the prime-power supply fluctuations dE amount to 10 v rms in 208 v rms, then jitter in the output pulse train would be only $dT_d \approx 45$ ns rms.

At full output power, power dissipation in controlled rectifiers S_{3a}, S_{3b}, and S_{3c} was 30.2, 26.5, and 25.0 watts, respectively.

The magnetic components reached steady-state temperatures approximately 1.3 hours after full-power output was established. Temperature rises above ambient were as follows:

Diode inductor housing	4 C
Energy-regulator air-gap spacer	120 C
Saturable-transformer main winding	65 C
Saturable-transformer oil	22 C

Although the internal temperature of the diode inductor was not monitored, it was observed that the transformer oil in the diode-inductor housing expanded only very slightly, thus confirming that L_3 exhibits very little loss. The temperature rise suffered by L_1 is high, although this component functioned without failure throughout the test. The saturable-transformer temperature rise is satisfactorily small, and could be permitted to be larger if the weight saving made possible by reducing the housing size is important.

Table 5.5 is the circuit operating profile over the entire test period. No trouble was experienced until after 200 hours after initial turn-on, when the power-transformer fuses opened. Thorough examination of the circuit failed to reveal the cause of failure, and the circuit restarted immediately, to run for over 37 additional hours in a trouble-free

Table 5.5

Experimental Pulse Generator Operating Profile

Event	Elasped Time (Hours)
Initial Turn-on	0
Preliminary Tests Completed; Begin Continuous Operation at Full Output Power	7.3
End of Run No. 1; Shut Down	12.5
End of Run No. 2; Shut Down	62.8
Run No. 3 Terminated by Open Fuse	200.0
End of Run No. 4	205.9
Run No. 5 Terminated by Open Fuse	237.1
End of Last Run	280.1

manner. Fuses were lost again at 237.1 hours; again, no reason for the failure was evident. Between 237.1 hours and the termination of the test at 280.1 hours, several additional runs of 6 to 9 hours each were conducted. Each run terminated when fuses opened.

The nature of the repeated circuit failure, and the lack of any unusual behavior prior to the failure, suggested the possibility of degradation of controlled-rectifier forward-blocking-voltage characteristics. Misfiring of any one of the three rectifiers comprising S_3 during the charging of C_1 places a short-circuit across the power supply, and the fuses open. Similar results obtain if S_2 misfires while S_3 is discharging C_1. Tests of the controlled rectifiers showed that the forward voltage that could be blocked by S_{3a} at 125 C junction temperature had indeed decreased from over 800 v to less than 500 v. All other controlled rectifiers and diodes tested within ratings.

The reduced blocking capability of S_{3a} is unquestionably the cause of the circuit failure. In fact, failure of S_{3a} was rather to be expected, because of an accident that occurred in assembly of the life-test circuit--the cathode terminal of this rectifier suffered a blow that caused a barely perceptible crack in the ceramic insulator that forms one of the two hermetic seals between metal electrodes. The damaged unit was used in the experimental circuit regardless, because no spare controlled rectifier having the required blocking-voltage capability was available. The crack was sealed with epoxy in an effort to avoid contamination of the junction. Apparently this makeshift repair did not suffice to prevent eventual failure of the device.

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APPENDIX A

RESETTING MODES WITH AN R-F TUBE LOAD

1. A PARTICULAR MODE

Consider first the following specific conditions:

a. The load is an r-f tube.

b. The capacitor voltages e_{C1} and e_{C2} are precisely zero at the end of the output pulse.

c. The inductor L_b in Fig. 3.4(a) is large enough to maintain bias currents constant throughout the operating cycle.

d. The bias currents lie within certain ranges determined by conditions developed below.

To simplify the form of equations to be written, it is convenient to define the resetting currents as

$$I_{2r} = I_{2b} - I_{2m} \tag{A.1}$$

$$I_{3r} = I_{3b} - I_{3m} \tag{A.2}$$

and

$$I_{Xr} = I_{Xb} - I_{Xm} \tag{A.3}$$

During reset e_3 and de_3/dt are small relative to pulse values. Thus, if the load is an r-f tube, both the electron current and the current in C_L may be ignored, and the condition

$$\frac{i_1}{n_X} + i_3 = i_X \tag{A.4}$$

applied in Fig. 3.4(b). Assume that bias currents are adjusted so that the pulse period terminates, as in Fig. 3.5, with the transformer in saturation and L_2 and L_3 resetting. Since the resetting voltages are small, the current i_1 in L_2 is approximately I_{2r}, and the current i_3 in L_3 is approximately I_{3r}. For the transformer to remain in sat-

uration, it is necessary[1] that i_X be greater than I_{Xr}. By Eq. A. 4, therefore, the first of the assumed bias-current conditions is

$$I_{Xr} < \frac{I_{2r}}{n_X} + I_{3r} \qquad (A.5)$$

Waveforms for the resetting mode considered are drawn in Fig. A. 1, These waveforms are continuations of those in Fig. 3.5, but are drawn to an expanded voltage scale and contracted time scale. The time origin is shifted to the end of the pulse interval, and the reset intervals for L_2 and L_3 (marked T_{L2} and T_{L3} in Fig. A. 1) include the pulse-tail interval T_t of Fig. 3.5.

It is assumed in the figure that $T_{L2} > T_{L3}$. Thus, throughout the T_{L3} interval, the constant currents I_{2r} and I_{3r} in the resetting inductors charge capacitors C_1 and C_2 respectively, and produce the negative-going ramps in the e_{C1} and e_{C2} waveforms. At the end of the interval, $-e_{C1}$ and $-e_{C2}$ have the values

$$E_{C1}' = \frac{I_{2r}}{C_1} T_{L3} \qquad (A.6)$$

and

$$E_{C2}' = \frac{I_{3r}}{C_2} T_{L3} \qquad (A.7)$$

respectively. Except for the pulse-tail oscillations, the saturated-transformer voltage is zero; hence, the capacitor voltages appear also across the inductors, as marked in the figure.

Reset of L_3 is complete and the interval T_{L3} terminates when the first dot-shaded area of the e_3 wave in Fig. A. 1 equals the switching area λ_3 of Fig. 3.5. By Eq. 3.22, therefore,

---

1 To maintain the transformer strictly in saturation, i_X must exceed $I_{Xb} - I_{xmo} = I_{Xr} + (I_{Xm} - I_{Xmo})$. If $I_{Xb} - I_{Xmo} > i_X > I_{Xr}$, the transformer begins to reset simultaneously with L_2 and L_3, but (unless i_X is very nearly equal to I_{Xr}) at a rate so low that only a negligible degree of reset is attained before i_X is altered by completion of the L_3 reset. For practical purposes, such operation is equivalent to the transformer remaining in saturation.

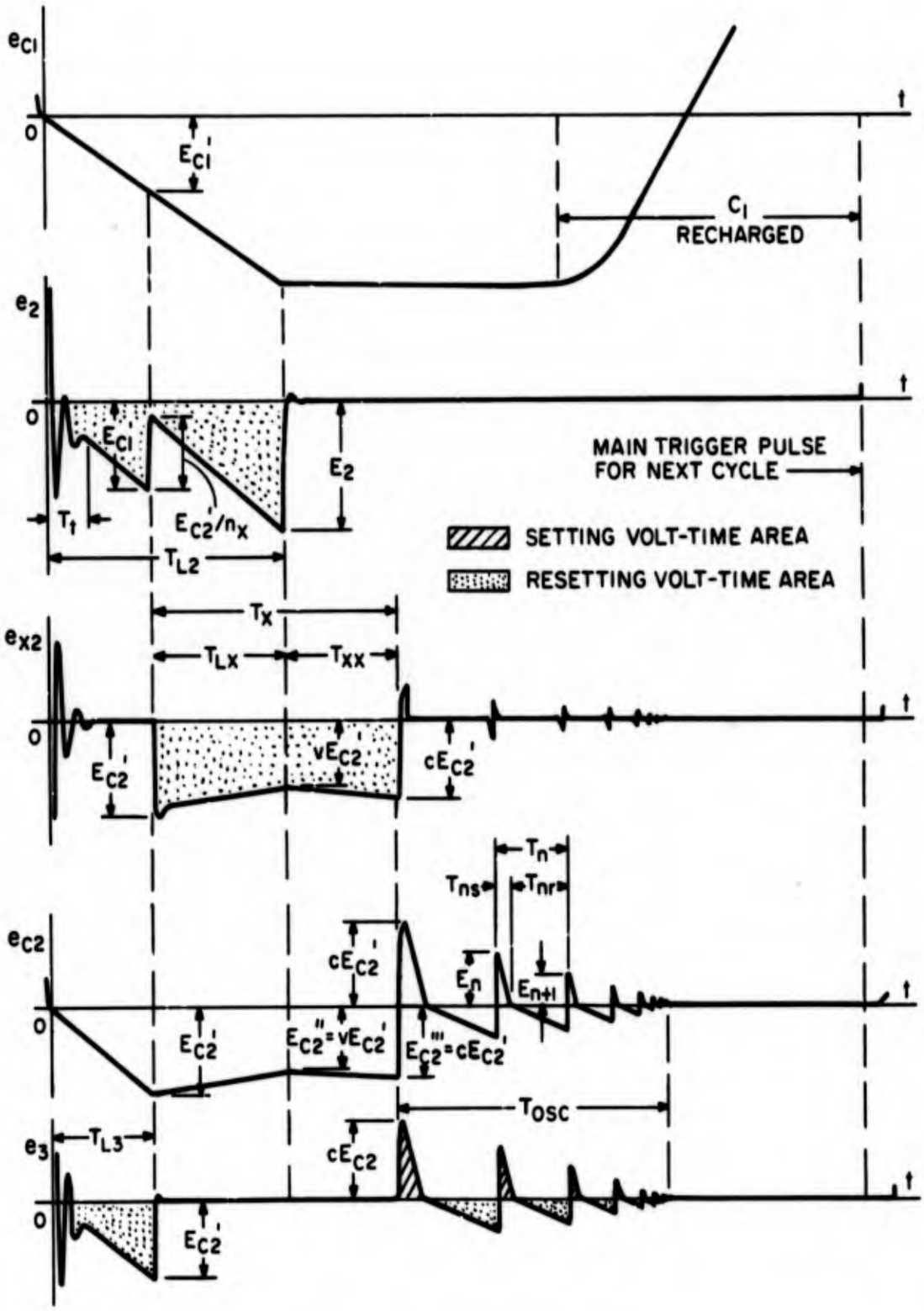

Fig. A.1 Waveforms for a Particular Resetting Mode

$$\frac{1}{2} E_{C2}' T_{L3} = E_p \tau$$

or (A.8)

$$T_{L3} = \sqrt{\frac{Q_2 \tau}{I_{3r}}}$$

The assumption that $T_{L2} > T_{L3}$ requires the switching area λ_2 of Fig. 3.5 to exceed the reset gained by L_2 in the guard interval and in the T_{L3} interval. Thus, by Eq. 3.15

$$E_{C1} T_h > E_{C1} T_g + \frac{1}{2} E_{C1}' T_{L3}$$

or, by Eqs. A.6 and A.8,

$$\frac{I_{2r}}{n_x} < 2 \frac{T_h - T_g}{\tau} I_{3r} \qquad (A.9)$$

Equation A.9 states a second assumed bias-current condition.

When L_3 saturates, its voltage falls to zero as rapidly as discharge of C_L permits. The capacitor voltage $-E_{C2}'$ therefore transfers to the transformer secondary and reset of the transformer begins. Simultaneously, the transformer primary voltage becomes $-E_{C2}'/n_x$ and a positive jump of this amount occurs in the e_2 wave. In Fig. A.1 it is assumed that E_{C2}'/n_x is less than E_{C1}', so that e_2 remains negative, L_2 remains in reset, i_1 remains equal to I_{2r}, and the slope of the e_{C1} wave remains unchanged. By Eqs. A.6 and A.7, this assumption leads to a third assumed bias-current condition,

$$\frac{I_{2r}}{n_x} > I_{3r} \qquad (A.10)$$

In order that Eqs. A.9 and A.10 may both be satisfied, and the resetting mode of Fig. A.1 be possible, it is necessary that

$$2 \frac{T_h - T_g}{\tau} > 1 \text{ or } T_h > T_g + \tau/2 \qquad (A.11)$$

This condition is usually satisfied; if τ is short enough to justify using pulse compression, a value of T_h in excess of $T_g + \tau/2$ is

necessary for controlled-rectifier turn-on.

After saturation of L_3 and throughout the interval marked T_{LX} in Fig. A.1, both L_2 and the transformer are assumed to remain in reset. Thus the current i_X (see Fig. 3.4b) is maintained at the value I_{Xr} by the transformer, and the charging current for C_2, $i_X - i_1/n_X$, has the value $I_{Xr} - I_{2r}/n_X$. At the end of the T_{LX} interval $-e_{C2}$ and $-e_{X2}$ each have the value

$$E_{C2}'' = E_{C2}' + \frac{I_{Xr} - I_{2r}/n_X}{C_2} \; T_{LX}$$

The ratio of E_{C2}'' to the beginning-of-the-interval voltage E_{C2}' is

$$\nu = \frac{E_{C2}''}{E_{C2}'} = 1 + \frac{I_{Xr} - I_{2r}/n_X}{I_{3r}} \; \frac{T_{LX}}{T_{L3}} \qquad (A.12)$$

For the transformer to remain in reset throughout the T_{LX} interval requires

$$\nu \geq 0 \qquad (A.13)$$

Implicit in Eq. A.13 is a fourth assumed bias-current condition.

In Fig. A.1 it is assumed that L_2 completes its reset and terminates the T_{LX} interval before reset of the transformer is complete; that is, the transformer switching area λ_{X2} of Fig. 3.5 is assumed to exceed the portion of the dot-shaded e_{X2} area contained in the T_{LX} interval in Fig. A.1. In terms of the ratio b of the transformer reset area in the T_{LX} interval to the total reset area λ_{X2}, this assumption is

$$b < 1 \qquad (A.14)$$

where by Eq. 3.21 and Eqs. A.7 and A.8,

$$b = \frac{E_{C2}' \frac{1+\nu}{2} T_{LX}}{E_{C2}(T/2 + T_{L3})} = (1+\nu) \frac{\tau}{T + 2T_g} \; \frac{T_{LX}}{T_{L3}} \qquad (A.15)$$

Implicit in Eq. A-14 is a fifth assumed bias-current condition.

The hold-off inductor completes its reset when the dot-shaded e_2 area in Fig. A.1 equals the switching area λ_2 of Fig. 3.5, less

the guard-interval reset. For $b < 1$, the dot-shaded e_2 area equals the corresponding area under the e_{C2} wave less the area $b\lambda_{X2}/n_X$ under a plot of the transformer primary voltage. Thus

$$\frac{1}{2}\frac{I_{2r}}{C_1}T_{L2}^2 - \frac{bE_{C2}(T/2 + T_g)}{n_X} = E_{C1}(T_h - T_g)$$

$$T_{L2} = \sqrt{\frac{Q_1[2(T_h - T_g) + b(T + 2T_g)]}{I_{2r}}} \qquad (A.16)$$

Upon saturation of L_2, the voltage $-E_2$ (see the e_2 wave of Fig. A.1) transfers from L_2 to the controlled rectifier S_3, and the current i_1 is quickly interrupted by S_3--provided T_{L2} is sufficiently long to allow decay of the high densities of controlled-rectifier minority carriers generated during the charging period. Thereafter, the capacitor voltage e_{C1} remains constant as in Fig. A.1 until the regulator circuit begins to recharge C_1 in preparation for the next cycle of operation.

After L_2 saturates, the transformer remains in reset for an additional interval of duration T_{XX}. Because of the interruption of i_1, the current charging C_2 becomes I_{Xr}, and the ratio of the value E_{X2}''' of $-e_{C1}$ or $-e_{C2}$ at the end of the T_{XX} interval to E_{C2}' is

$$c = \frac{E_{C2}'''}{E_{C2}'} = \frac{E_{C2}'' + \frac{I_{Xr}}{C_2}T_{XX}}{E_{C2}'} = \nu + \frac{I_{Xr}}{I_{3r}}\frac{T_{XX}}{T_{L3}} \qquad (A.17)$$

Inasmuch as the dot-shaded area of the e_{X2} waveform must equal the switching area λ_{X2},

$$E_{C2}(T/2 + T_g) = bE_{C2}(T/2 + T_g) + E_{C2}'\frac{a + c}{2}T_{XX}$$

or, by Eqs. A.7 and A.8,

$$\frac{T_{XX}}{T_{L3}} = \frac{1 - \nu}{\nu + c}\frac{T + 2T_g}{\tau} \qquad (A.18)$$

Equations A.17 and A.18 yield

$$c = \sqrt{\nu^2 + (1 - b)\frac{T + 2T_g}{\tau}\frac{I_{Xr}}{I_{3r}}} \qquad (A.19)$$

where the positive root is selected because E_{C2}''' cannot be negative. In order that c be real, it is necessary that the radicand be positive (or zero), and thus

$$\frac{I_{Xr}}{I_{2r}} \geq -\frac{\nu^2}{1 - b}\frac{\tau}{T + 2T_g} \qquad (A.20)$$

constitutes a sixth assumed bias-current condition.

If any three of the quantities I_{2r}, I_{3r}, and I_{Xr}, ν, and b are given, Eqs. A.8, A.15, and A.16 determine the other two (in terms of T_h, T, T_g, and τ). Thus, the resetting times are determined; T_{L3} by Eq. A.8, T_{L2} by Eq. A.16 and T_X (see Fig. A.1) by the relation

$$\frac{T_X}{T_{L3}} = \frac{T_{LX} + T_{XX}}{T_{L3}} = \left(\frac{b}{\nu + 1} + \frac{1 - b}{\nu + c}\right)\frac{T + 2T_g}{\tau} \qquad (A.21)$$

derived from Eqs. A.15 and A.18.

At the end of the T_X interval, the transformer and both inductors are in negative saturation, but, if $c > 0$, the resetting operation is not complete. Energy stored in C_2 remains to be dissipated in a damped nonsinusoidal oscillation of the form shown in the T_{osc} interval of Fig. A.1.

Upon saturation of the transformer, capacitor C_2 discharges through the saturated inductances of the transformer secondary and diode inductor in series. After the first half-cycle of oscillation, which reverses the capacitor voltage, the discharge is interrupted because both the transformer and the inductor, being fully reset, can block positive capacitor voltage. The current is limited to the smaller of the two setting currents--$I_{Xb} + I_{Xm}$ for the transformer and $I_{3b} + I_{3m}$ for the inductor. It is assumed in Fig. A.1 that $I_{3b} + I_{3m}$ is smaller, that is, a seventh bias-current condition,

$$I_{Xr} > I_{3r} - 2(I_{Xm} - I_{3m}) \qquad (A.22)$$

is assumed. Subject to this condition, the transformer remains in negative saturation and L_3 begins to set after the capacitor-voltage reversal.

The diode inductor receives a small degree of set while capacitor C_2 is being discharged by the current $I_{3b} + I_{3m}$. When the capacitor voltage changes sign, the inductor changes from set to reset, and the capacitor current decreases to the value I_{3r}. When the reset volt-time area equals the set area, L_3 again saturates, and the preceding cycle repeats, beginning with reversal of the capacitor voltage. This process continues in cycles of decreasing amplitude and duration as losses absorb the energy initially in C_2. Eventually an amplitude too low to remove the operating point of L_3 from saturation is reached.

Because both sinusoidal reversals and linear changes of e_{C2} are involved, it is difficult to calculate accurately the time T_{osc} from completion of transformer reset to the final steady-state condition of complete reset. However, if E_{C2}''' is appreciable, the period of the sinusoidal oscillation is very short relative to the initial linear-change period, and an approximate value of T_{osc} can be had by summing the linear-change periods under the assumption that these persist to zero amplitude.

To this end, let E_n denote the capacitor voltage e_{C2} at the beginning of the nth cycle of oscillation, and let T_n denote the period of that cycle, equal to the sum of the setting time T_{ns} and resetting time T_{nr} (see Fig. A.1). Then, since

$$E_n T_{ns} = E_{n+1} T_{nr}$$

and

$$E_n = \frac{I_{3b} + I_{3m}}{C_2} T_{ns} = \frac{I_{3b} - I_{3m}}{C_2} T_{n-1,\,r}$$

therefore

$$\frac{I_{3b} + I_{3m}}{C_2} T_{ns}^2 = \frac{I_{3b} - I_{3m}}{C_2} T_{nr}^2$$

and

$$\frac{E_n}{E_{n+1}} = \frac{T_{ns}}{T_{n+1,s}} = \frac{T_{nr}}{T_{n+1,r}} = \frac{T_n}{T_{n+1}} = \frac{T_{nr}}{T_{ns}} = k$$

where

$$k = \sqrt{\frac{I_{3b} + I_{3m}}{I_{3b} - I_{3m}}} = \sqrt{1 + 2I_{3m}/I_{3r}}$$

Thus

$$T_{osc} = T_1(1 + 1/k + 1/k^2 + \ldots) = \frac{T_{1s}(1+k)}{1 - 1/k} = \frac{C_2 E_{C2}'''}{I_{3r}} \frac{k+1}{k(k-1)}$$

and since E_{C2}''' equals cE_{C2}',

$$\frac{T_{osc}}{T_{L3}} = c \frac{I_{3r}}{I_{3m}} \left(1 + \frac{I_{3m}/I_{3r}}{\sqrt{1 + 2\, I_{3m}/I_{3r}}}\right) \qquad (A.23)$$

For $I_{3r}/I_{3m} > 0.8$, the factor in parenthesis differs from 2 by less than 10 percent. To this approximation,

$$\frac{T_{osc}}{T_{L3}} = 2c \frac{I_{3r}}{I_{3m}} \qquad (A.24)$$

2. MODE DIAGRAM

Consider now all resetting modes obtainable by bias-current adjustment if the basic restrictions of an r-f-tube load, no residual capacitor voltages, and constant bias currents still apply. Resetting-current ranges in which each mode obtains may be represented by plotting mode-region boundaries in the space of the resetting currents I_{2r}, I_{3r}, and I_{Xr}. Inasmuch as only the region $I_{3r} > 0$ is of interest and (for the most part) the mode boundaries depend only on the ratios $(I_{2r}/n_X)/I_{3r}$ and I_{Xr}/I_{3r}, this plot may be simplified to the two-dimensional mode diagram of Fig. A.2.

In this figure, the line AA' divides the upper region in which resetting begins with L_3 in saturation from the lower region in which Eq. A.5

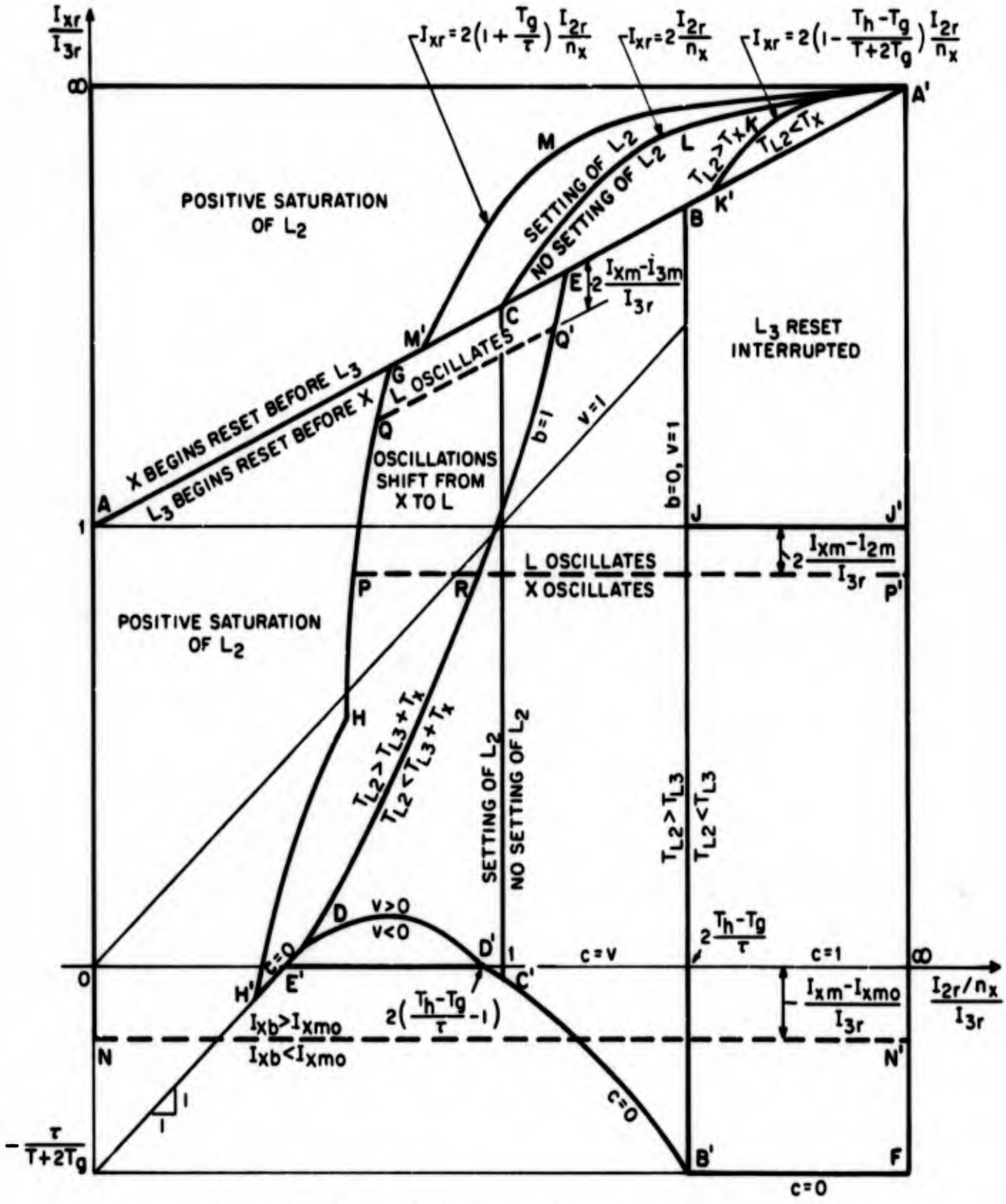

Fig. A.2 Mode Diagram for R-F Tube Load and Zero Residual Voltages

applies and reset begins as in Fig. A.1. The line BB' divides the region to the right in which $T_{L2} < T_{L3}$ (or L_2 completes reset before L_3) from the region to the left in which Eq. A.9 and the waveforms of Fig. A.1 apply. Similarly the line CC' divides the left-hand region in which e_2 becomes positive when the transformer begins to reset from the right-hand region in which Eq. A.10 applies and L_2 resets continuously.

The lineDD' is a plot of the parametric relation obtained by placing $\nu = 0$ in the equations

$$\frac{I_{2r}/n_X}{I_{3r}} = \frac{2\,\frac{T_h - T_g}{\tau} + b\,\frac{T + 2T_g}{\tau}}{\left(1 + \frac{b}{1+\nu}\,\frac{T + 2T_g}{\tau}\right)^2} \qquad (A.25)$$

and

$$\frac{I_{Xr}}{I_{3r}} = \frac{\nu^2 - 1}{b}\,\frac{\tau}{T + 2T_g} + \frac{I_{2r}/n_x}{I_{3r}} \qquad (A.26)$$

obtained from Eqs. A.8, A.15 and A.16. Above DD', $\nu > 0$ as in Fig. A.1, and below this line $\nu < 0$ so that e_{X2} becomes positive and transformer reset is interrupted by a setting interval. A similar parametric relation obtained by placing b = 1 in Eqs. A.25 and A.26 yields the line ED. To the right of ED, b < 1 as in Fig. A.1; to the left $T_{L2} > T_{L3} + T_X$--that is, the transformer completes reset before L_2.

The line B'D' also is obtained from Eqs. A.25 and A.26, under the condition

$$\nu^2 = -(1-b)\,\frac{T + 2T_g}{\tau}\,\frac{I_{Xr}}{I_{3r}} \qquad (A.27)$$

on this line c = 0 (see Eq. A.19);above it Eq. A.20 applies and the waveforms of Fig. A.1 obtain. Below B'D' transformer,reset is impractically slow; in the T_{XX} interval of Fig. A.1, e_{X2} rises nearly to the zero axis (because I_{Xr} is negative) and levels off when the small resetting voltage so decreases the magnetizing current that

the effective resetting current becomes zero. The lines B'F, E'D', are H'E' are similar boundaries for the $T_{L2} < T_{L3}$, $\nu < 0$, and $T_{L2} > T_{L3} + T_X$ regions, respectively. The portion of the line B'D'DE to the left of CC' is, strictly speaking, obtainable from Eqs. A.25 and A.26 only in the limiting case of very large I_{3r}; otherwise the change of charging current for C_1 during setting of L_2 must be taken into account.

The region to the left of line CC' is divided by line GHH'. Between CC' and GHH', L_2 is partially set by reversal of e_2 when transformer reset begins. To the left of GHH', the setting of L_2 proceeds to positive saturation. Discharge of C_2 into C_1 through L_2 and L_3 then interchanges the values of the voltages $n_X e_{C1}$ and e_{C2}. Subject to the assumption that I_{3r} is large (so that the change in charging rate of C_1 when L_2 begins to set may be ignored), the line HH' is described by

$$\frac{I_{Xr}}{I_{3r}} = 1 + \frac{I_{2r}/n_X}{I_{3r}} - \frac{1 + 2\,T_g/\tau}{(I_{2r}/n_X)/I_{3r} + 2T_g/\tau}\left(1 - \frac{I_{2r}/n_X}{I_{3r}}\right) \qquad (A.28)$$

and the line GH is determined parametrically by

$$\frac{I_{2r}/n_X}{I_{3r}} = \frac{T/\tau}{\left(1 + t_X\right)^2} \qquad (A.29)$$

and

$$\frac{I_{Xr}}{I_{3r}} = \frac{I_{2r}/n_X}{I_{3r}} + \frac{1}{t_X}\left(\frac{T + 2T_g}{\tau t_X} - 2\right) \qquad (A.30)$$

Different relations define HH' and GH because (for points to the right of these lines) setting of L_2 may terminate either when a negative-going ramp of e_2 crosses the zero axis (line HH'), or when the transformer completes reset (line GH--the parameter t_X in Eqs. A.29 and A.30 equals T_X/T_{L3}).

The region to the right of line BB' is divided by the line JJ'. Below this line, reset of L_3 is complete when transformer reset begins, as in Fig. A.1. Above JJ', reset of L_3 is interrupted when L_2 completes its reset, and is completed after the transformer is reset.

The region above line AA', in which reset begins with inductor L_3 in saturation and L_2 and X resetting, is divided by the lines A'KK', A'LC and A'MM'. To the right of A'KK', the hold-off inductor completes reset before the transformer: to the left the transformer completes reset first. To the right of A'LC reset of L_2 is continuous, whereas to the left, L_2 is set during the period of transformer reset. To the left of AMM', the setting of L_2 continues to positive saturation.

The three dashed lines in Fig. A.2 depend in position on the value of I_{3r}. For very large I_{3r}, line NN' lies on the $(I_{2r}/n_X)/I_{3r}$ axis, PP' lies at $I_{Xr}/I_{3r} = 1$, and QQ' lies on AA'. As I_{3r} decreases, all three lines move downward. For any specific I_{3r} value, only the portion of the diagram above line NN' is available, because of the condition $I_{Xb} > I_{xmo}$ in Eq. 3.48. The line PP' separates the upper region in which oscillations of e_3 occur during the T_{osc} interval, as in Fig. A.1 (see Eq. A.22) from the lower region in which L_3 remains saturated and the final oscillations appear in the e_{X2} waveform. (In the region QQ'RP the oscillations appear first in the e_{X2} waveform and shift to e_3 when L_2 saturates.) Below line PP' the duration of the final oscillations is determined by an equation analogous to Eq. A.24 but applicable to the transformer--for $I_{xr} > 0.81_{xm}$,

$$\frac{T_{osc}}{T_{L3}} = 2c\,\frac{I_{Xr}}{I_{xm}} \qquad (A.31)$$

3. OTHER MODES OF RESET

The resetting modes represented by regions in Fig. A.2 do not exhaust all possibilities. Current flow into the load during reset, voltages remaining across capacitors C_1 and C_2 at the end of the output pulse, and cyclic variations of the bias current I_b in Fig. 3.4(a) all influence the resetting operation and alter the mode diagram.

If the load is a linear resistor R_L, current in the load affects reset of L_3. The resetting current I_{3r} develops a constant voltage $I_{3r}R_L$ across the load and L_3. The reset volt-time area $I_{3r}R_LT_{L3}$ is, by Eq. 3.12, approximately equal to $E_p\tau_p$, and the energy J_R dissipated in R_L during reset is therefore

$$J_R = I_{3r}\lambda 3 = \frac{E_p^2\tau_p^2}{R_L T_{L3}} = J_p\frac{\tau_p}{T_{L3}} \qquad (A.32)$$

(see Eq. 3.8.) If fast resetting of L_3 is required, the loss J_R becomes a significant percentage of the nominal pulse energy J_p. To avoid this loss, a diode may be placed in series with R_L. In high-power pulse generators, however, diode voltage ratings sufficient to block inverse voltages that occur in the charging interval may be impractical. If so, an avalanche diode, such as D_L in Fig. 3.1(a), may be used. The avalanche voltage is chosen only high enougn to provide adequately fast resetting of L_3. Residual voltages on C_1 and C_2 are important because even though the discharge of each capacitor is substantially complete in terms of energy, the residual voltage may be greater than the capacitor voltages required for reset at normal speeds. For example, 0.01 percent of the initial energy remaining in a capacitor corresponds to 1 percent residual voltage, and reset voltages of about this magnitude suffice in a pulse generator having a 0.001 duty ratio.

If a positive voltage remains on C_1 at the end of the output pulse, and if reset begins with the transformer in saturation, L_2 is first set to positive saturation--thus eliminating the reset gained in the guard interval. The voltage across C_1 is then reversed by discharge of the capacitor through L_2 and the transformer primary. The negative voltage thus acquired by C_1 speeds the subsequent reset of L_2. A negative residual voltage on C_1 speeds reset of L_2 without first eliminating the guard-interval reset. In a similar way, a positive residual voltage on C_2 is reversed by discharge through the transformer secondary and L_3, and the resultant negative voltage--or an originally negative C_2 voltage--speeds the resetting of L_3 and X.

4. EVALUATION OF MODES

The details of a resetting mode are of no practical importance, provided that the following conditions are met: (1) reset is accomplished in the time available, (2) current in controlled rectifier S_3 during hold-off meets the rectifier turn-on requirements, and (3) pulse-generator efficiency is not reduced by unnecessary losses during reset.

The unavoidable losses during reset are the core losses associated with a relatively slow resetting of each of the three saturable devices from positive to negative saturation. In some modes excess losses are introduced. The loss in a linear load resistance during reset of

L_3 (J_R in Eq. A.32) is an example. For modes to the left of line CC' in Fig. A.2 excess loss occurs because of the minor hysteresis loop traced when reset of L_2 is interrupted by a setting interval. A similar excess loss occurs in L_2 if a positive residual voltage on C_1 causes initial setting, and also in the transformer if $\nu < 0$. If the voltage across C_2 is not zero when reset of X and L_3 is first completed, excess loss occurs because energy then in C_2 is dissipated in the final oscillations. Excess loss occurs if any element is reset more rapidly than necessary to such an extent that its magnetizing current exceeds the normal reset value.

In Fig. A.2, the only modes free of excess loss are those represented by points on the portion of the lower boundary line (c = 0 to avoid final-oscillation losses) to the right of line CC' ($I_{2r}/n_X > I_{3r}$ to avoid minor-loop losses) and not close to point D' (I_{Xn}/I_{3r} moderately large to avoid excessively fast resetting of L_3). Additional no-excess-loss modes may be made possible by a negative residual voltage on C_1. The negative voltage shifts line CC' to the left, and if of sufficient magnitude, may eliminate minor-loop loss in L_2 along line DH'. Modes requiring $I_{Xr} < 0$ are of limited usefullness, because I_{3r} cannot be increased beyond the value for which line NN' passes through the mode point, and resetting is correspondingly slow. Modes represented by line DE' are free of this difficulty.

In some modes excess loss exists but is too small to be of practical significance. For example, on DE' minor-loop loss is negligible even though line CC' passes to the right of the mode point, provided the setting volt-time area is small. Similarly, if the guard-interval reset of L_2 is small, the minor-loop loss associated with reversal of positive residual voltage on C_1 is negligible; thus positive as well as negative residual voltage may be used to obtain fast resetting with low loss on line DE'. Excess loss occasioned by final oscillations also is generally small for mode points for which c is no greater than one--provided extremely fast resetting is not attempted. Thus mode points a little above line DE' or points near the $(I_{2r}/n_X)/I_{3r}$ axis and to the right of CC' are often useful. In contrast, mode points near or above line PP' are generally undesirable--excess losses may be large because of the large value of c, and (often more important) initial reset of L_3

and X must be accomplished in a fraction of the reset period to allow time for slow decay of the final oscillations (see Eqs. A.24 and A.31).

An idea of resetting speeds obtainable without important final-oscillation loss when c is limited to one may be had by considering operation at the intersection of line BB' and the $(I_{2r}/n_X)/I_{3r}$ axis in Fig. A.2. Equations A.7 and A.8 yield

$$T_{L3} = \frac{E_{c2}}{E_{c2}'} \tau$$

and Eq. A.21 then gives

$$T_{L2} = T_{L3} + T_X = \frac{E_{C2}}{E_{C2}'} \left(\frac{T}{2} + T_g + \tau \right) \qquad (A.33)$$

For c = 1, the capacitor voltage at which oscillations begin is equal to $-E_{C2}'$. Thus if the final oscillation loss is to be limited to 1 percent, E_{C2}/E_{C2}' in Eq. A.33 can be made 10. Typically $T/2 + T_g + \tau$ is about $5\,\tau_p$ and T_{L2} may be half the repetition period T_r; thus a duty ratio of about 0.01 is attainable. Reset of L_2 in half the repetition period allows time for S_3 to recover its forward blocking capability, and thereafter, for capacitor C_1 to be recharged. Because $T_{L2} = T_{L3} + T_X$, ample time is available for the final oscillation to decay. (The interval T_{osc} is short relative to T_{L3}, though not zero for $I_{Xr} = 0$ as the approximate Eq. A.31 indicates.)

Duty ratios much in excess of 0.01 may lead not only to significant excess resetting losses, but also to difficulty in resetting L_2 rapidly enough with the bias current permitted by controlled-rectifier hold-off-interval requirements. During hold-off, the controlled-rectifier current (see Section B.1) is

$$I_h = I_{2b} + I_{2m}' = I_{2r} + I_{2m} + I_{2m}' \qquad (A.34)$$

Use of Eq. 3.42 and evaluation of Q_1 as $2I_{1p}/\pi$ times T (where I_{1p} is the peak value of the half-sine pulse of controlled-rectifier current) yields

$$\frac{I_{2m} + I_{2m}'}{I_{1p}} = \frac{\pi}{2} \frac{\mu_e/H_c}{B_s} \frac{T_h + \tau/2}{T\left[1 + (1-\nu)\tau/2T_h\right]} \left(1 + \frac{I_{2m}'}{I_{2m}} \right) \qquad (A.35)$$

Similarly, Eq. A-16 yields

$$T_{L2} = \frac{2}{\sqrt{\pi}} \sqrt{T(T_h - T_g) + b(T/2 + T_g)} \sqrt{\frac{I_{1p}}{I_{2r}}} \qquad (A.36)$$

This equation applies directly to the resetting mode of Fig. A.1 and may be extended to apply throughout the region to the right of line GHH' in Fig. A.2 if b is taken to be zero to the right of BB' and one to the left of EDH'.

In Eq. A.35, the factor $\mu_e H_c/B_s$ is 0.8×10^{-4} for 50-percent-nickel iron (Eq. 2.19), the time-ratio fraction is typically somewhat less than one, and the factor in parenthesis is about 5 for usual hold-off times (see Fig. 2.2). Thus $(I_{2m} + I_{2m}')/I_{1p}$ is of the order of 10^{-4}. Optimum values of I_h/I_{1p} with respect to controlled-rectifier turn-on are not yet known (see Sections B.2 and B.3 of Chapter II), but it is estimated that a range of I_h/I_{1p} values extending at least from 0.005 to 0.05 is satisfactory. Smaller values may reduce turn-on speed; larger values may cause appreciable dissipation during hold-off. Relative to this range of I_h/I_{1p}, $(I_{2m} + I_{2m}')/I_{1p}$ values near 10^{-4} are negligible, and thus Eq. A.34 requires that I_{2r}/I_{1p} lie between 0.005 and 0.05.

To maintain I_{2r}/I_{1p} greater than 0.005 requires, by Eq. A.36, that T_{L2} be less than $16\sqrt{T(T_h - T_g) + b(T/2 + T_g)}$--no matter how long a time may be available in the repetition period for reset of L_2. In applications requiring very short output pulses, this maximum value of T_{L2} may be less than 100 μs and the resetting loss of L_2 correspondingly larger than normal (see Fig. 2.2). Residual capacitor voltages cause faster resetting of L_2 for the same I_{Xr} values, and thus may produce large resetting losses with output-pulse durations in the microsecond range. In the opposite extreme, the maximum limit 0.05 on I_{2r}/I_{1p} leads, in resetting modes to which Eq. A.36 applies, to a minimum T_{L2} of $5\sqrt{T(T_h - T_g) + b(T/2 + T_g)}$. Faster reset of L_2, when required to obtain high repetition frequencies, may be achieved with the aid of residual capacitor voltages, or a mode point to the left of line GHH' in Fig. A.2. The maximum obtainable repetition frequency is thus not determined by resetting requirements,

but rather by the characteristics of controlled rectifier S_3, and the circuit that recharges capacitor C_1. The rectifier determines minimum values for T_h, T, T_{L2} (for decay of minority-carrier densities), and the time for forward-blocking recovery after current i_1 is interrupted. Recharging of C_1 determines the minimum interval from forward-blocking recovery of S_3 to the next triggering.

APPENDIX B

MEASUREMENT OF SATURABLE-INDUCTOR VOLT-TIME INTEGRAL AND SATURATED INDUCTANCE

The circuit of Fig. B.1 provides a simple means of determining saturated inductance L_s and the volt-time integral λ of a saturable inductor. The inductor L under test is connected into the circuit as shown, and a d-c power-supply voltage E of perhaps a few hundred volts is connected to the left-hand terminals. A few bias turns are wound loosely on L and connected to a bias supply containing an inductor L_B large enough to maintain the bias current constant to within one percent or so.

Switch S is depicted as a controlled rectifier, although other switches may be suitable; S should switch relatively rapidly, and exhibit negligible voltage drop during the main current pulse. The switching rate is controlled manually, and need be a few pulses per minute at most. Resistor R_2 is a low-inductance, low-resistance current-viewing shunt so that v is an accurate replica of the waveform of current i. The value of C, a high-quality pulse capacitor, is chosen so that the peak value I_p of i(t) is the same as L experiences in the pulse-generator circuit. Resistor R_1 is made large, so that $E/R_1 \ll I_p$.

In operation, S is triggered at t = 0, and the voltage Ξ on C is impressed across L. The current wavefore i(t) appearing at the viewing terminals resembles that of Fig. B.2. Little current flows after t = 0 until L absorbs a volt-time integral λ, at which point it saturates to pass the desired half-sine current pulse of peak amplitude I_p. The measurement cycle ends shortly after the current pulse amplitude reacnes zero. At that time, the voltage E across C attempts to reverse i; L becomes unsaturated; S opens; and C begins to recharge back to E. Inductor L then resets slowly; after reset is complete, the procedure may be repeated.

Values of t_h and Δt can be read from a photograph of the waveform of i(t). Then

$$\lambda = \frac{t_h}{E} \qquad (B.1)$$

and

$$L_s = \frac{(\Delta t)^2}{\pi^2 C} \qquad (B.2)$$

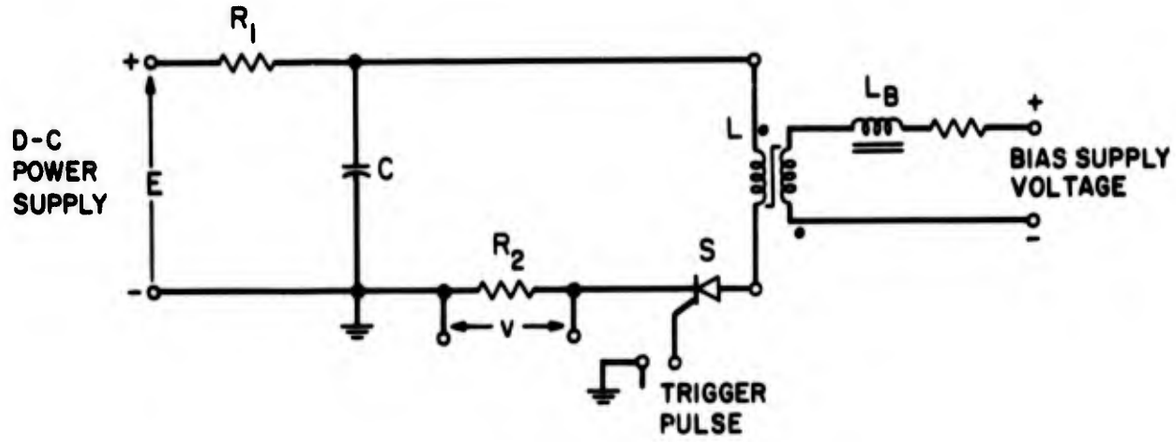

Fig. B.1 Saturable-Inductor Test Circuit

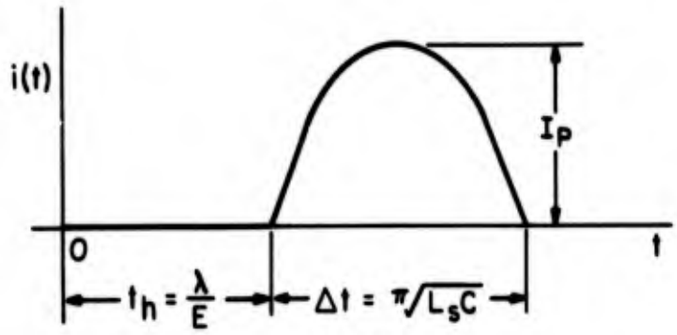

Fig. B.2 Current i(t) in Fig. B.1