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APPLICATION OF P-N-P-N DIODES TO MAJORITY LOGIC CIRCUITS

THESIS

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Preface

This report is the result of my attempt to apply P-N-P-N diodes in majority logic circuits. I have assumed the reader has a knowledge of basic circuit theory and is familiar with Boolean Algebra and binary logic circuits. The discussion on majority logic is by no means complete; it was presented so that a reader would gain some insight on the functional requirements of a majority logic device.

The bibliography which follows the text represents most of the current efforts in both the subject of majority logic and P-N-P-N diode research. It should provide a source of more detailed information for a reader that is interested in either subject.

I wish to acknowledge my indebtedness to my thesis advisor, Lt. M. Kabrisky, for his interest in my work and his many helpful suggestions. I am also grateful to my wife who graciously relinquished her demands on my time during the preparation of this report and to my typist, Mrs. Elisabeth Rath, for her efforts in transcribing my notes.

Robert A. Hamann

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Abstract

The static characteristics of a two terminal P-N-P-N diode are discussed. Switching of this diode is controlled by varying the applied voltage and current. Majority logic is then considered. Functions can be converted to majority form from Boolean expressions using an axiomatic majority-decision logic; majority logic circuits can be analyzed with Karnaugh maps. A three input majority logic circuit using P-N-P-N diodes and passive circuit elements is presented. An analysis of the circuit shows that it is possible to obtain any number of outputs with component tolerances of 5%. The operating frequency is less than 200 KC. The circuit is practical for application where high speed is not required and diodes can be obtained at a low cost.

APPLICATION OF P-N-P-N DIODES TO MAJORITY LOGIC CIRCUITS

I. Introduction

The purpose of this investigation was to determine whether majority-decision logic circuits could be built with P-N-P-N diodes. A P-N-P-N diode is a four-layered semiconductor switch that exhibits a negative resistance region in its volt-ampere characteristic curve. The property of negative resistance can be used to achieve signal gain in logic circuits.

Majority logic is a threshold logic with a weighting factor of unity. When a majority of the inputs is present, the majority-decision circuit or device emits an output signal. When there is less than a majority of inputs present, there is no output. A majority-decision device or circuit by definition must be capable of accepting a minimum of three inputs.

The investigation was limited to designing a three-input majority-decision circuit module and presenting several applications of this module. The P-N-P-N circuit module is capable of driving several inputs of similar modules. The design data and operating characteristics of the module

are tabulated. Several Boolean functions were converted to equivalent majority-logic, and circuits constructed with the P-N-P-N modules are presented that solve the functions. Usually the majority-logic circuits use fewer decision elements than the conventional Boolean circuits; therefore, the majority-logic circuits are simpler.

The results of the study show that it is possible to build majority-logic circuits with P-N-P-N diodes. The P-N-P-N module has one advantage over the design of a majority-logic circuit with tunnel diodes presented by W.F. Chow (Ref 2). The output of the P-N-P-N logic module is capable of driving any number of inputs of similar modules.

II. Description of a P-N-P-N Diode

A P-N-P-N diode is a two terminal four-layered semiconductor switch. The diode is very similar in physical appearance to a transistor except that there is no base lead; the two leads are attached to the outer layers of the semiconducting material (Fig. 1). Most commercial units are produced from a silicon crystal. The four layers are obtained by controlled diffusion of impurities resulting in a P-N-P-N structure. The circuit symbol used for the P-N-P-N diode is a circled number four. The four stems from the number of layers in the device and the slanting line of the number indicates the forward direction of current in the diode when it is in the low-resistance, high conduction condition.

The operation of the diode can be analyzed by considering the diode as a combination of two complementary transistors, two resistors and an avalanche diode connected as shown in Fig. 2. The P-N-P-N device performs the same functions as the complementary-transistor circuit. The analysis by Moll et al (Ref 9) proceeds from this viewpoint; however, a complete understanding of the physics of the device is not a prerequisite for understanding the remainder of this report. A knowledge of the volt-ampere character-

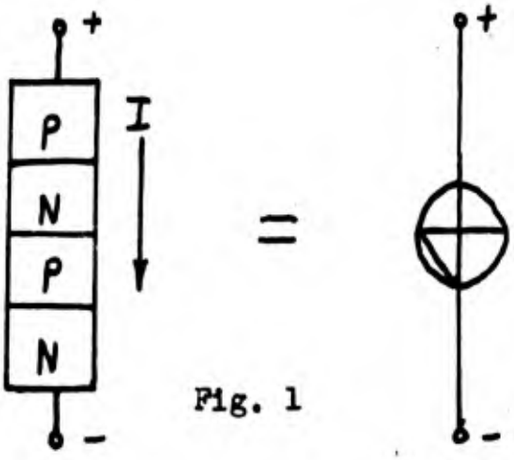


Fig. 1

P-N-P-N Diode And Circuit Symbol

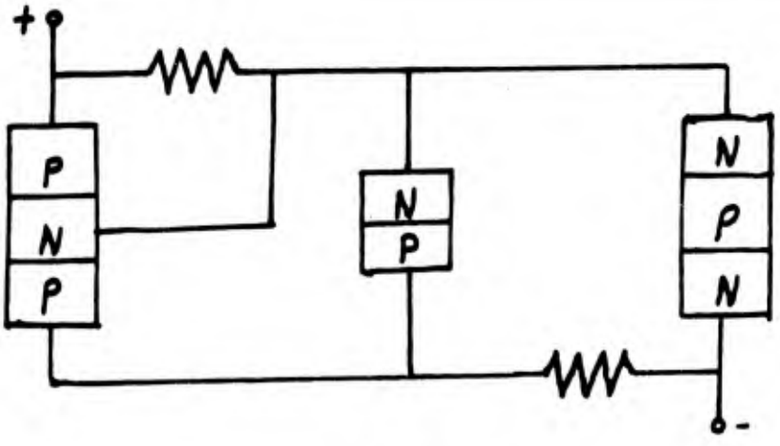


Fig. 2

Equivalent Circuit for a P-N-P-N Diode

istics of the diode is sufficient. The following discussion is limited to P-N-P-N diodes, but the analysis would be similar for any open-circuited stable device (S shaped volt-ampere characteristic).

A typical volt-ampere curve for the P-N-P-N diode can be represented as shown in Fig. 3. The diode is an open-circuited stable device with three operating regions in the switching directions. Regions I and III correspond to the two stable states. Region I is the "off" or high resistance state; Region III is the "on" or low resistance state. These two regions are separated by a non-linear negative resistance, Region II. The value of voltage and current at the break points or boundaries of the Regions is of special interest. The diode begins to switch "on" when the voltage reaches the breakover voltage (V_B). Inherent feedback in the diode allows the current to increase while the voltage decreases until the diode is fully "on" in Region III. The dynamic resistance in this state is only a few ohms so the current is essentially controlled by the external circuit resistance. Voltage drop across the diode in the "on" state is about one volt. The diode will remain in this low resistance state as long as sufficient current flows through it. When the current falls below the value of holding current (I_h), the device will switch back to the high

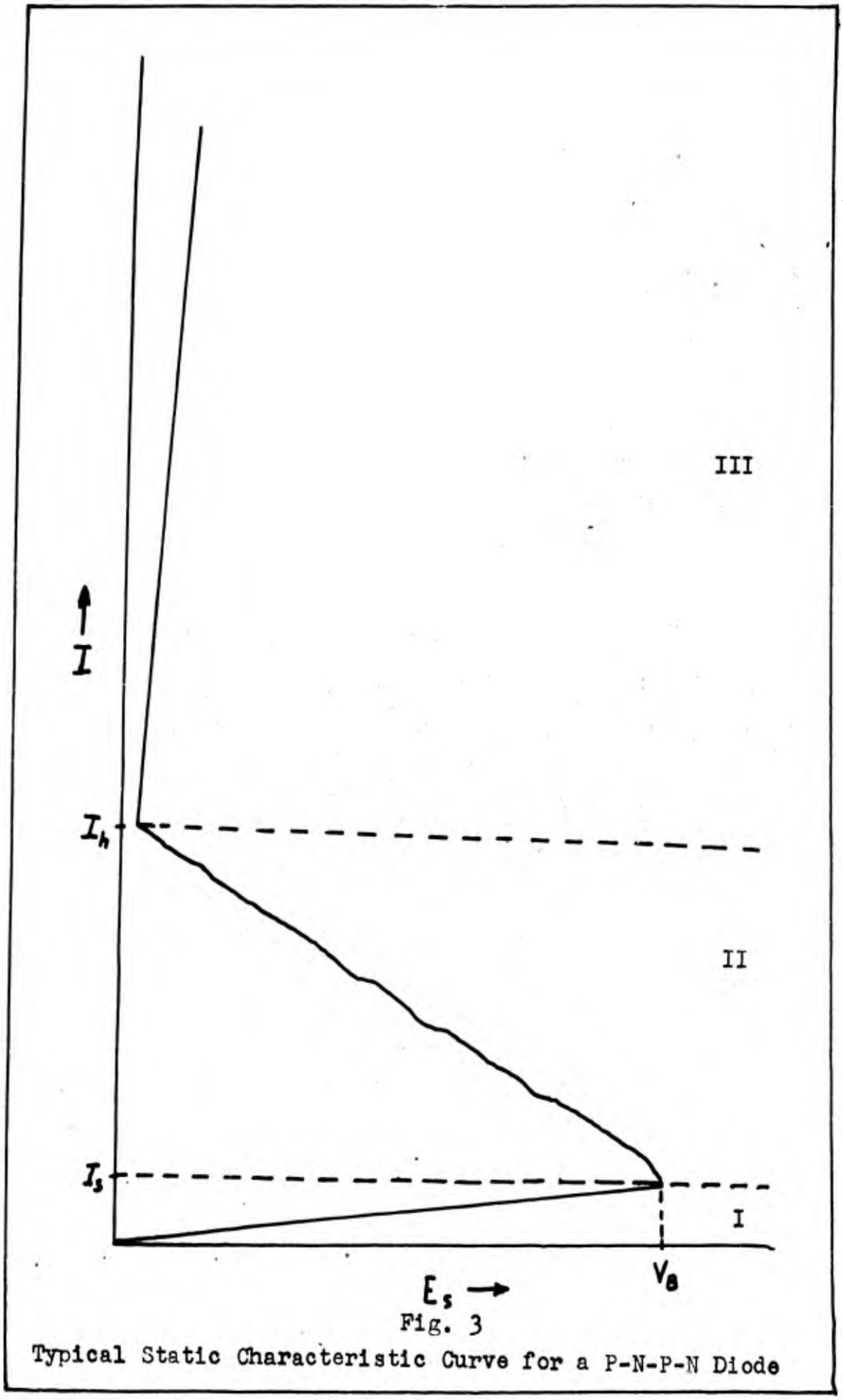


Fig. 3

Typical Static Characteristic Curve for a P-N-P-N Diode

resistance or "off" state. The resistance in this state is above one megohm for all values of voltage below V_B. If the polarity of the applied voltage is reversed, the diode will exhibit a very high resistance until the reverse breakdown voltage (V_{RB}) is reached. Then Zener breakdown occurs at approximately 60% of the rated V_B. Diodes are available with breakover voltages (V_B) from 20 to 200 volts $\pm$ 10% and with holding currents (I_h) from 1 to 50 ma.

III. Majority Logic

Devices

A majority-decision device is a special case of a binary threshold logic device. A binary threshold logic device has several inputs that can be weighted independently, a summing circuit, and an organ that will produce an output when a given threshold is reached. Mathematically this can be expressed as follows:

When $\sum_{i=1}^{n} w_i x_i \geq T$ then output = 1

$\sum_{i=1}^{n} w_i x_i < T$ then output = 0

Where x_i are binary inputs

w_i are respective weighting functions

T is the threshold value of the output device.

If all of the weighting functions w_i are set equal to one, then a three input threshold device is reduced to a

majority-decision organ, when $1 \leq T \leq 2$. By definition, a majority-decision element is a device that accepts several binary inputs and produces an output when it determines that a majority of inputs is present. That is, the output will be "1" if and only if at least two of the inputs are "1" S when three input devices are being considered. The discussion that follows is limited to three-input, one-output devices.

Algebra

Ordinary Boolean equations cannot, in general, represent majority-decision networks because Boolean algebra contains no single symbol to denote the majority-decision operation. Early attempts to apply Boolean algebra to the design of majority-logic networks resulted in the inefficient use of the majority-decision device. By making one of the three inputs unconditional, Wigington succeeded in showing that all logic functions of two variables could be built with the majority organ and a negation operation (Ref 12). This method depends on the fact that an unconditional input reduces the majority device to a two input AND or OR gate. If the unconditional input is a "1", the device will function as an OR gate; if it is a "0" the device becomes an AND gate. Once this has been accomplished, familar design techniques can be used to construct a logic circuit. A

binary adder stage using this conventional design technique is shown in Fig. 6. This method is straightforward, but it fails to exploit the logical properties of the majority element. It can lead to inefficient circuit designs with respect to the numbers of elements required.

Unconditional inputs restrict the use of the majority-decision device. When an unconditional input is used, only two conditional inputs can be processed by each element instead of three. The number of decision elements necessary to process a given function is increased and in this sense the majority-decision device is restricted. This method does have two advantages. The first is that it permits familiar conventional design techniques and, second, it allows for a flexible computer design. The gates in a computer constructed of majority-decision elements with an unconditional input could be made to function as AND or OR gates depending on the value of the unconditional input.

Lindaman suggested pairing the symbol "#" as a notation for the majority-decision operator (Ref 7). The symbol is defined by

$$A \# B \# C \equiv AB + AC + BC$$

The introduction of this new symbol allows the majority-decision operation to be directly represented. This facilitates

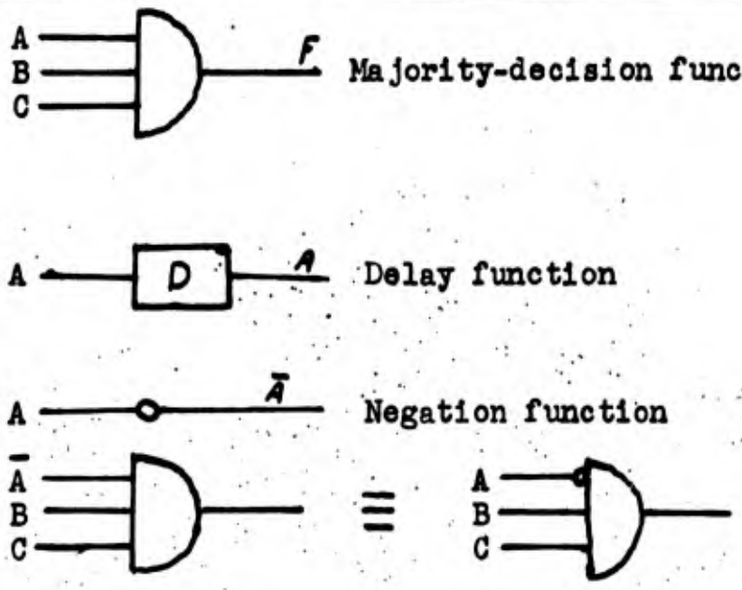


Fig. 4

Graphical Conventions

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

F = ABC + AB + AC + BC

Where "1" represents a true value

And ABC is the intersection of the three variables

And + is the conjuction

Fig. 5

Truth Table for Majority-Decision Elements

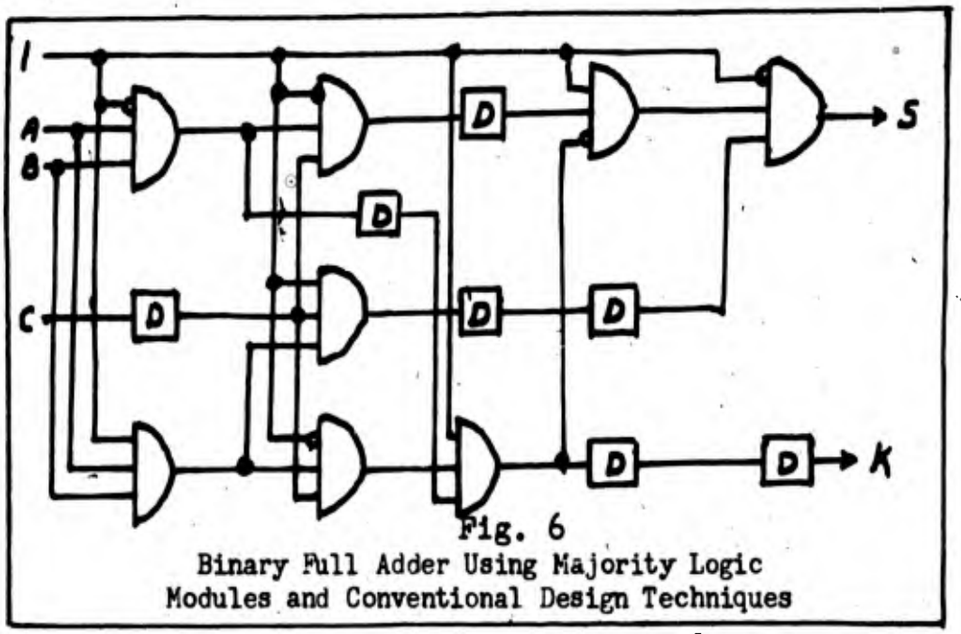


Fig. 6
Binary Full Adder Using Majority Logic
Modules and Conventional Design Techniques

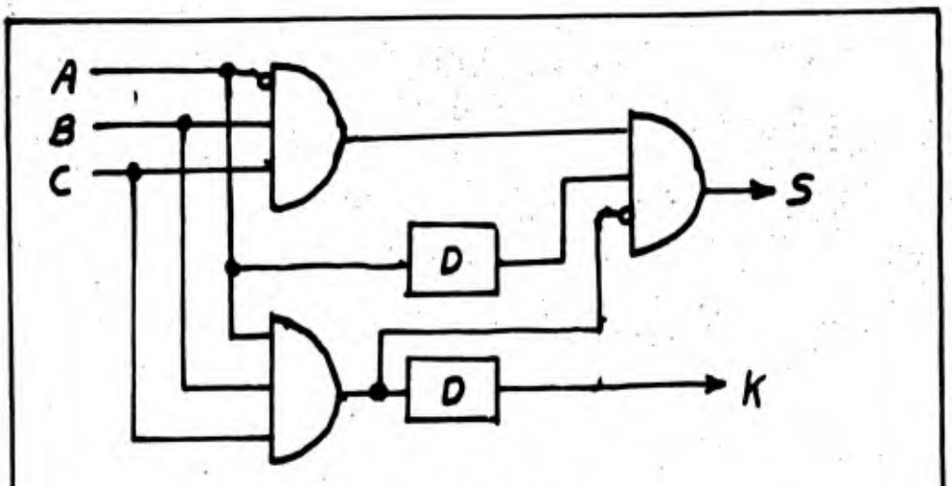


Fig. 7
Binary Full Adder Using Majority Logic
Modules and Majority Logic Design Techniques

a different method of design that does not require unconditional inputs and usually produces a simpler circuit. For example, the binary adder stage designed by the conventional method (Fig. 6) is much simpler when the augmented Boolean algebra is used (Fig. 7). Lindaman postulated that the simplest circuit is one which requires the fewest number of decision elements or, if the number of decision elements is the same, the fewest number of delay elements. The simplest circuit is usually the most economical and also the fastest. The addition of a majority-decision operator to Boolean notation provided a new method of design. This new method was capable of producing minimal logical designs because it did not restrict the majority-decision device.

Rules for using the new notation had to be formulated. The original work of Lindaman was expanded and an axiomatic majority-decision logic was developed (Ref 3). The new algebra consists of a set of ten axioms. They are a list of unproven propositions that provide a sufficient basis for the derivation of all provable theorems within the system. Fourteen theorems are derived that provide the identities required to manipulate expressions in axiomatic majority-decision logic. Boolean axioms can be derived as theorems of the new logic. In this sense, majority-decision logic includes Boolean algebra. It is used to convert Boolean expressions to majority-decision logic.

Analysis of Majority Circuits

With a given circuit, an analysis proceeds as follows. Majority logic circuits can be analyzed with the aid of Karnaugh maps. The output will always map into a "T" with the three inputs in the center block of the "T". (See example page 15) An examination of the map will show that blocks adjacent to the center will contain two of the three input variables. When the individual units are connected in a circuit, the output of each unit will be the majority of the true signals present in the Karnaugh maps of the driving units. Any circuit can be analyzed by this simple procedure.

Analysis of Karnaugh Maps

The procedure for finding the output of a majority decision element is as follows:

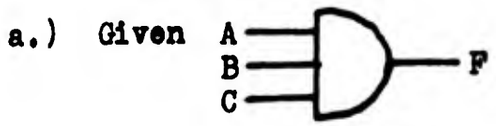
Step 1. Draw four Karnaugh maps.

Step 2. Map the three inputs.

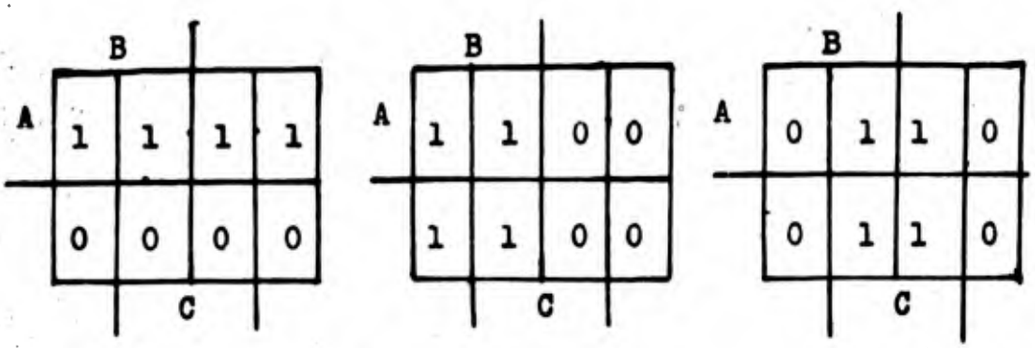
Step 3. On the remaining map, place a true value in the individual blocks if at least two true values appear in the corresponding blocks of the input maps. This is a map of the output function. The Boolean expression is the conjunction of the min terms present in this map.

Two examples are given.

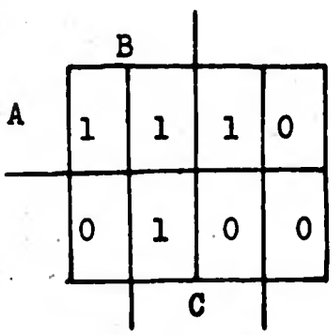
a.) Given



Find F



Maps Of The Inputs



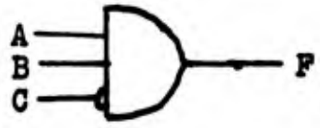
Map Of F

The output F = ABC + AB + AC + BC

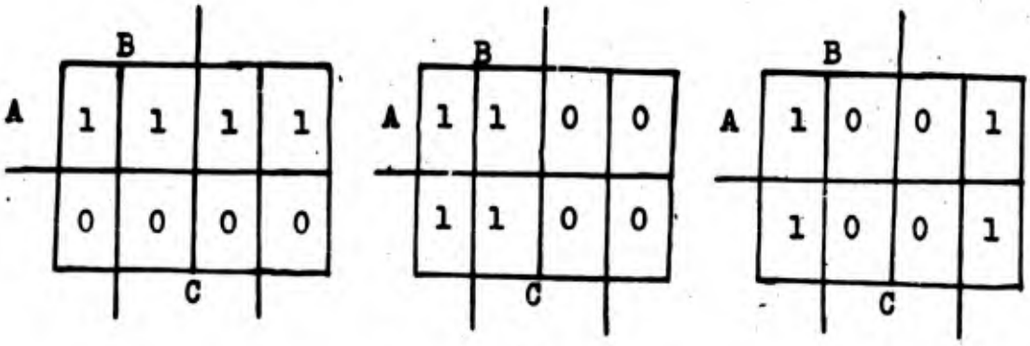
Simplified F = AB + AC + BC

This is the output that was expected since it is the definition of a majority-decision operator.

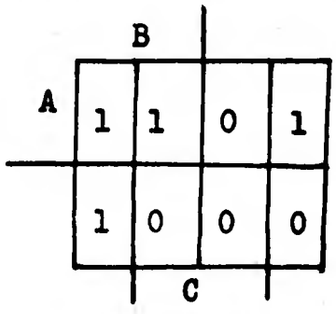
b.) Given:



Find F



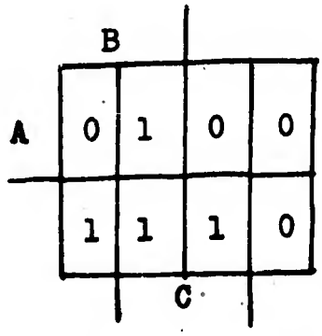
Maps Of The Inputs



Map Of F

An examination of the output map reveals that the function always plots into a "T" considering blocks at the extremities of the map adjacent. Also the center of the "T" is the min term corresponding to the presence of the three inputs. These facts make it possible to write the output by inspection. For example the output of the element

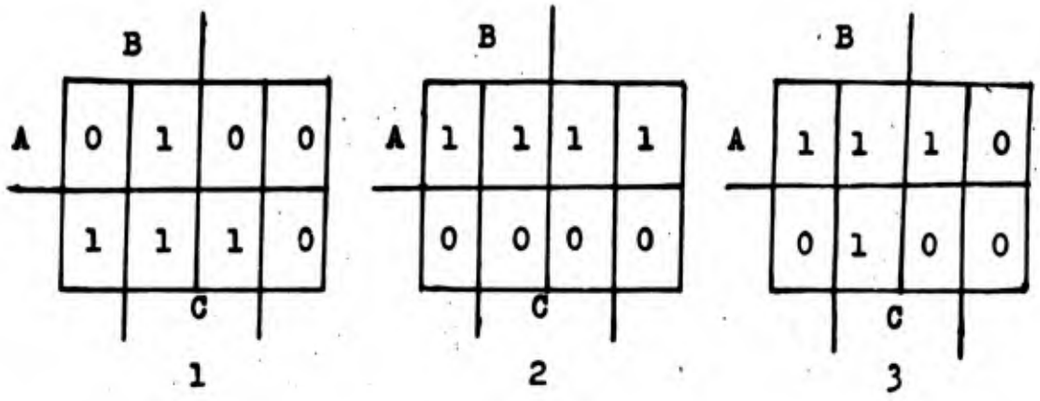
can be maped immediately to



by placing a "1" in the min term block ABC and completing the "T".

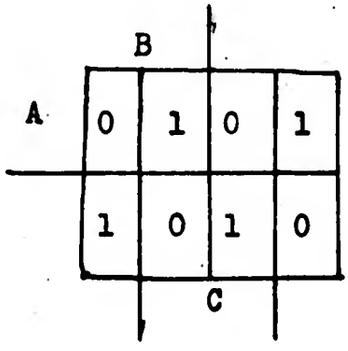
When the majority-decision elements are cascaded, the output of the second stage cannot, in general, be written by inspection. The output will be a "T" of the inputs, but these inputs are functions of the conditional inputs to the first stage. The information that is usually desired from circuit analysis is to express the output in terms of the original inputs. This information can be obtained by mapping the outputs of the first stage elements by inspection and then proceeding as outlined previously. When additional stages are present, this step is repeated until the final output is mapped. An analysis of the full adder circuit (Fig. 7) by this method is given below.

The outputs of the first stages at 1, 2 and 3 are by inspection.



The function at 3 is the carry output of the full adder. Inputs to the second stage are the functions at 1 and 2, and the negation of the carry output.

The output of the second stage by mapping is



The function expressed as a conjunction of the min terms present is $F = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$ which is indeed the sum output of a full adder.

IV. Circuit Design

Objectives

The objective of this study was to determine the feasibility of a majority-decision logic module using only P-N-P-N diodes and passive circuit elements. The P-N-P-N diode would be used as the active element to perform the necessary switching process and to supply the required power gain to the output.

Operation in an asynchronous mode is in general desirable. Asynchronous operation is faster and would eliminate the requirement of having clock synchronism and the difficulties attendant to this.

Another objective of the study was to achieve a high fan in and fan out ratio without substantial loss in operating speed. The fan in ratio is the number of inputs that a module can accept and still produce the required logic output function. A requirement of majority logic is to have an odd number of inputs to avoid the indeterminate case so that the fan in ratio for a majority-decision module is (2N + 1) where N is some positive integer. The fan out ratio is defined as the number of succeeding inputs that can be driven by the output of one module. The only requirement imposed is that the number be a positive integer.

The fan in and fan out ratios can be considered figures of merit for logic modules. If the fan in ratio is high, more information can be processed by a single module. This permits a greater flexibility in computer design. Also, the problem solution time is proportional to the number of cascaded modules required to preform the operation. Cascading may be reduced in some cases as the fan in ratio is increased. The number of modules required to preform a complex function is also reduced, depending on design techniques, if large fan out ratios are allowed.

Considerations

The characteristics of the active element limit the logic module design. An examination of the static characteristics of a P-N-P-N diode (Fig. 3) will show that a prescribed positive voltage (20-200 VOLTS) must appear across the diode (resistance greater than a megohm) before it will switch to the high conduction or "on" state. Once the diode is on, it can only be turned off by reducing the current flowing through it below the minimum value of holding current. This point on the static characteristic curve corresponds to less than a 1 volt drop across the diode. This is a severe requirement for the control or trigger circuit. It

must be capable of raising the voltage across a 20 volt diode by at least 4 volts to turn the diode on if we allow, say, for a minimum turn-on tolerance of 10%. It must also function to turn the diode off. The diode must be in one of its allowed states anytime a simple majority or more of the inputs are present and revert to the opposite state whenever less than a single majority of inputs appear.

The ultimate speed of operation for any logic module is governed by the properties of the device. Every device has distributed capacitance, therefore, it will have a finite time constant. The P-N-P-N diode has a turn-on time of .1 u sec. and a turn-off time of .2 u sec. The theoretical upper frequency limit of the single diode with no external connections can be approximated by the reciprocal of twice the time constant. For the P-N-P-N diode this upper frequency limit becomes 1.67 mc. It is virtually impossible to achieve the upper frequency limit in any practical circuit; the external circuit parameters will act to increase the time constant. Another consideration is that the succeeding stages must be able to detect some threshold value of the output. A circuit operating at its maximum theoretical frequency would have a nearly sinusoidal output where the peak of the wave would correspond to the threshold value. The output must be above the threshold value for a finite length

of time to activate succeeding states, therefore, the actual operating frequency will, of necessity, be less than the theoretical value. Frequencies of operation of about 10% of the theoretical maximum are typical in practical application.

Approach

The objective of asynchronous operation apparently cannot be achieved with a simple passive input trigger circuit. Some inputs can always be present in this mode; therefore, the voltage change contributed by one of the inputs would have to be capable of switching the diode. The difference in voltage levels needed to switch the diode on and off must be at least equal to the forward breakdown voltage of the switching diode. A voltage swing of this magnitude from a passive circuit is not possible since the input to the trigger circuit must come from the switching action of the diode. Consequently, the input voltage will be less than that required to switch the diode in both directions. With these limitations, asynchronous operation was dropped and the design of the logic module proceeded with the assumption that it would operate synchronously. Synchronous operation eliminates the requirement of having the trigger circuit turn the diode off. A second diode can preform this function when it is part of a monostable

flip-flop circuit.

Some part of the logic module has to sum the inputs to determine when the majority threshold is reached. Each input must contribute less than $\frac{1}{N}$ and more than $\frac{1}{N+1}$ of the majority threshold value where N is a positive integer related to the number of inputs by the equation: No. of inputs = 2 N + 1. The allowable tolerance on each input depends inversely on the number of inputs. When circuit losses and the magnitude of the required trigger voltages are considered, a large fan-in ratio using-passive elements is impractical from an engineering viewpoint. As on illustrative example, the majority logic module shown in Fig. 8 was designed using a fan-in ratio of three and assuming synchronous operation.

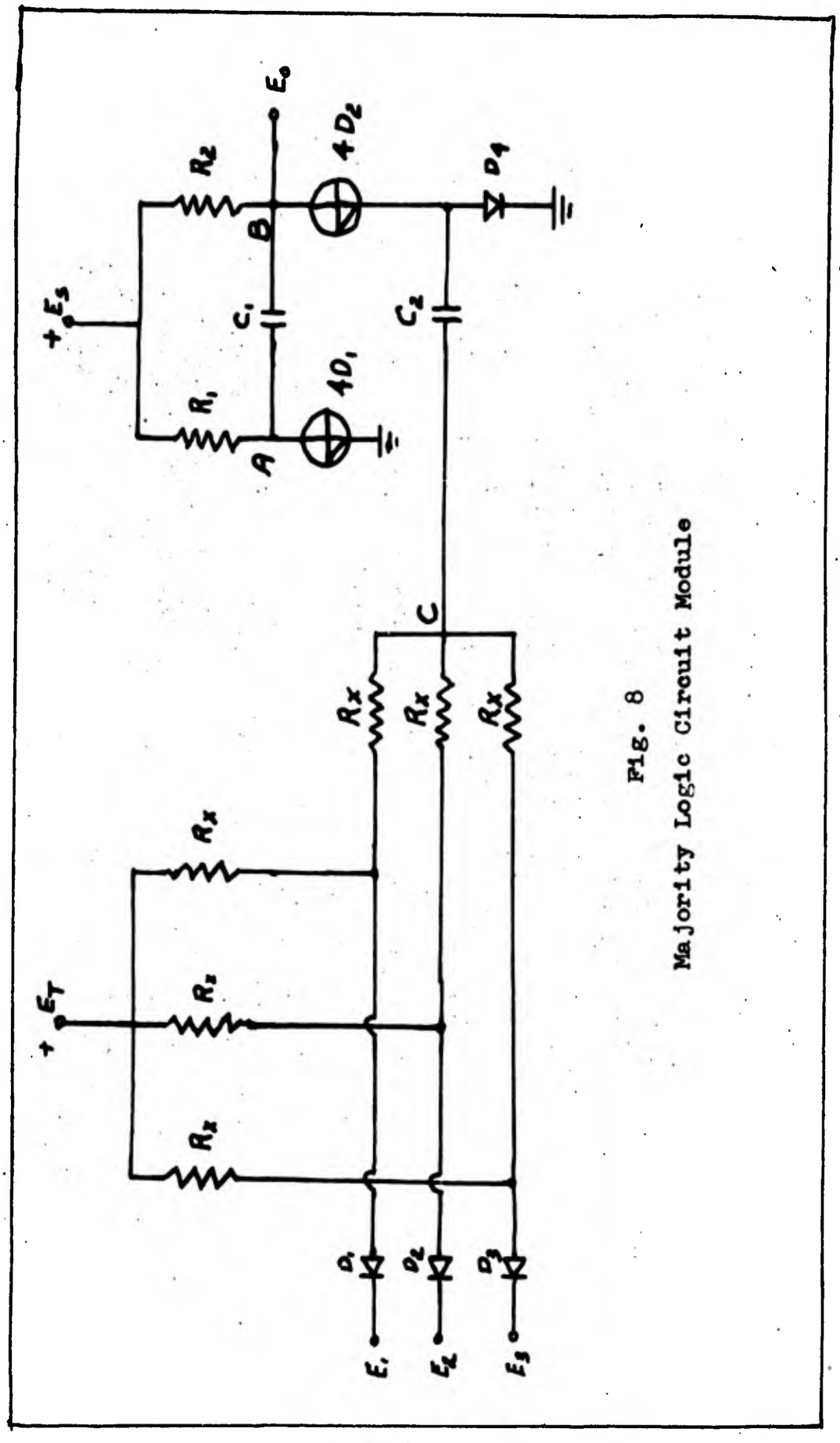


Fig. 8

Majority Logic Circuit Module

V. Majority Logic Circuit Module

Description of Operation

The logic module is a single-shot (or monostable) multivibrator circuit that is triggered whenever a majority of the inputs is present. The three inputs are E_1, E_2 and E_3 and the output is E_o. E_T is the trigger voltage supply and E_S is the supply for the switching diodes $4D_1$ and $4D_2$. The forward breakdown voltage, V_B, of the switching diodes are chosen so that $4D_1$ is normally on and $4D_2$ is off. The input voltage is restricted to zero or to a positive value greater than or equal to E_T; a "true" input is defined to be ground potential. A true output is also defined to be approximately ground potential; therefore, there is no phase reversal between the input and the output.

Synchronous operation is necessary to provide the correct output. A voltage greater than or equal to E_T will be present at the input terminals during the "interpulse" time. Interpulse time is the time between the trailing edge of an input pulse and the beginning of the next possible input pulse. During this time, the capacitor C_2 is charged to the potential E_T. The capacitor C_1 will charge to a potential difference from B to A of E_S volts.

During dynamic operation when input pulses are present, the potential of point C drops to a value determined by the number of inputs that are present. The magnitude of this voltage drop will be transferred through C_2 and appear as a negative potential at diode $4D_2$. The voltage difference across $4D_2$ is increased by an amount large enough to switch the diode on when two or more inputs are present. Point B is grounded when $4D_2$ is switched on. The action of C_1 causes the potential at A to fall to $-E_S$ volts placing a reverse bias on $4D_1$ and switching it off. Voltage on C_1 rises toward a value of E_S at a rate determined by R_1C_1. When this voltage reaches V_B of $4D_1$, it switches on placing A at ground and a reverse bias on $4D_2$ through C_2. $4D_2$ switches off and will remain in this state until another trigger pulse is injected through C_2. All of the input terminals are reset to a voltage greater than or equal to E_T and the cycle is complete.

The output voltage E_o is determined by the condition of $4D_2$. $4D_2$ is on when a majority of inputs is present, thus E_o is at ground potential and gives the required true indication. E_o is equal to E_S when $4D_2$ is off.

Analysis of Operation

Necessary Circuit Conditions. An analysis of the circuit operation will yield the necessary circuit condition for

correct operation and fix the tolerance of the various parameters. The following analysis proceeds with the assumptions listed below:

1) The supply voltages E_T and E_S do not vary.
2) All capacitors are perfect.
3) Diodes D_1 - D_4 are ideal.
4) E_S is always large enough to switch diode $4D_1$ on.
5) $E_T \leq E_S$

Let the fractional resistor tolerance be P and the variation of the forward breakdown voltage, V_B, of $4D_2$ be η, then the maximum voltage at C when one input is present is

$$V_{c\ max} = \frac{E_T}{2}\left[1+P\right] \tag{1}$$

and the minimum is

$$V_{c\ min} = \frac{E_T}{2}\left[1-P\right] \tag{2}$$

the maximum voltage at C with two inputs is

$$V_{c\ max} = \left[\frac{1+P}{5-3P}\right] E_T \tag{3}$$

and the minimum is

$$V_{c\ min} = \left[\frac{1-\rho}{5-3\rho}\right] E_T \tag{4}$$

V_B for $4D_2$ must be greater than E_S to assure monostable operation. Assume that this value is taken to be some constant, β greater than the supply voltage. $4D_2$ will then switch somewhere between

$$V_{4D_2} = \beta E_s [1-\eta] \tag{5}$$

and

$$V_{4D_2} = \beta E_s [1+\eta] \tag{6}$$

or the minimum trigger voltage, V_T, that must be supplied is

$$V_{T\ min} = E_s [\beta - \beta\eta - 1] \tag{7}$$

and the maximum would be

$$V_{T\ max} = E_s [\beta + \beta\eta - 1] \tag{8}$$

the maximum trigger voltage generated with one input must be less than the minimum trigger voltage necessary for switching. The trigger voltage is

$$V_T = E_T - V_C \tag{9}$$

so

$$\frac{E_T}{2}\left[1+\rho\right] \leq E_s\left[\beta - \beta\eta - 1\right] \tag{10}$$

also, the minimum V_T generated with two inputs must switch the diode

$$4\left[\frac{1-\rho}{3-3\rho}\right] E_T \geq E_s\left[\beta + \beta\eta - 1\right] \tag{11}$$

In order to facilitate further analysis assume typical diodes $4D_1$ and $4D_2$ with nominal current capacity of 50 ma D.C. current; on these units a concomitant maximum power dissipation of 50 mw is specified. Their forward resistance is less than 2 ohms when I = 25 ma so for diode $4D_1$

$$\frac{E_s}{R_1[1-\rho]} \leq 50 \times 10^{-3} \tag{12}$$

$4D_2$ will have a duty cycle less than unity so

$$50 \times 10^{-3} \geq \left[\frac{E_S}{R_2[1-P]} + \frac{K E_T}{R_X[1-P]} \right] \times L \times D.C. \quad (13)$$

where K is the number of inputs the stage is driving. The maximum limits on the constant, β, can be determined by applying assumption (5) to equation (11) which yields

$$\beta_{max} = 1.8 \quad (14)$$

If a minimum of 5 volts in excess of the rated V_B is used to satisfy assumption (4) then $E_S = 25$. Allowing a 5 volt margin to prevent $4D_2$ from switching on yields $\beta = 1.2$ for the general case. Therefore

$$1.2 \leq \beta \leq 1.8 \quad (15)$$

Optimum β

E_T was calculated and expressed as a function of E_S for several values of β and diode tolerances. This data is presented in table I. The effect of resistor tolerance on E_T is shown in table II for a diode tolerance of .05. A plot of E_T verses E_S for three values of β assuming perfect

components is shown in Fig. 9. It can be seen that as β increases, the range of E_T increases for any given supply voltage. The lower limit of E_T is the trigger voltage necessary to produce a minimum drop of V_B across the switching diode when two inputs are present. The upper limit of E_T is determined by the maximum voltage one input would place on the switching diode. The most reliable operation would occur when E_T is midway between these limits. In a practical application, E_T should be selected to provide a switching voltage 10% greater than V_B when switching is desired and still have the maximum voltage 10% below V_B with only one input present.

The upper limit of E_T can never be greater than E_S for proper operation. This restriction decreases the permissible range of E_T for large values of β. Any variation of the circuit parameters will also reduce the range of E_T for any β. These effects are shown in Fig. 10. Figure 11 shows the relationship of resistor and diode tolerance for various values of β. $\beta = 1.6$ appears to be the optimum for the selection of circuit components. Diode tolerance is seen to be more citical than that of the resistors.

Optimum Speed

The speed of operation is a function of the circuit time constants. When R_2 is made much larger than R_1 and K

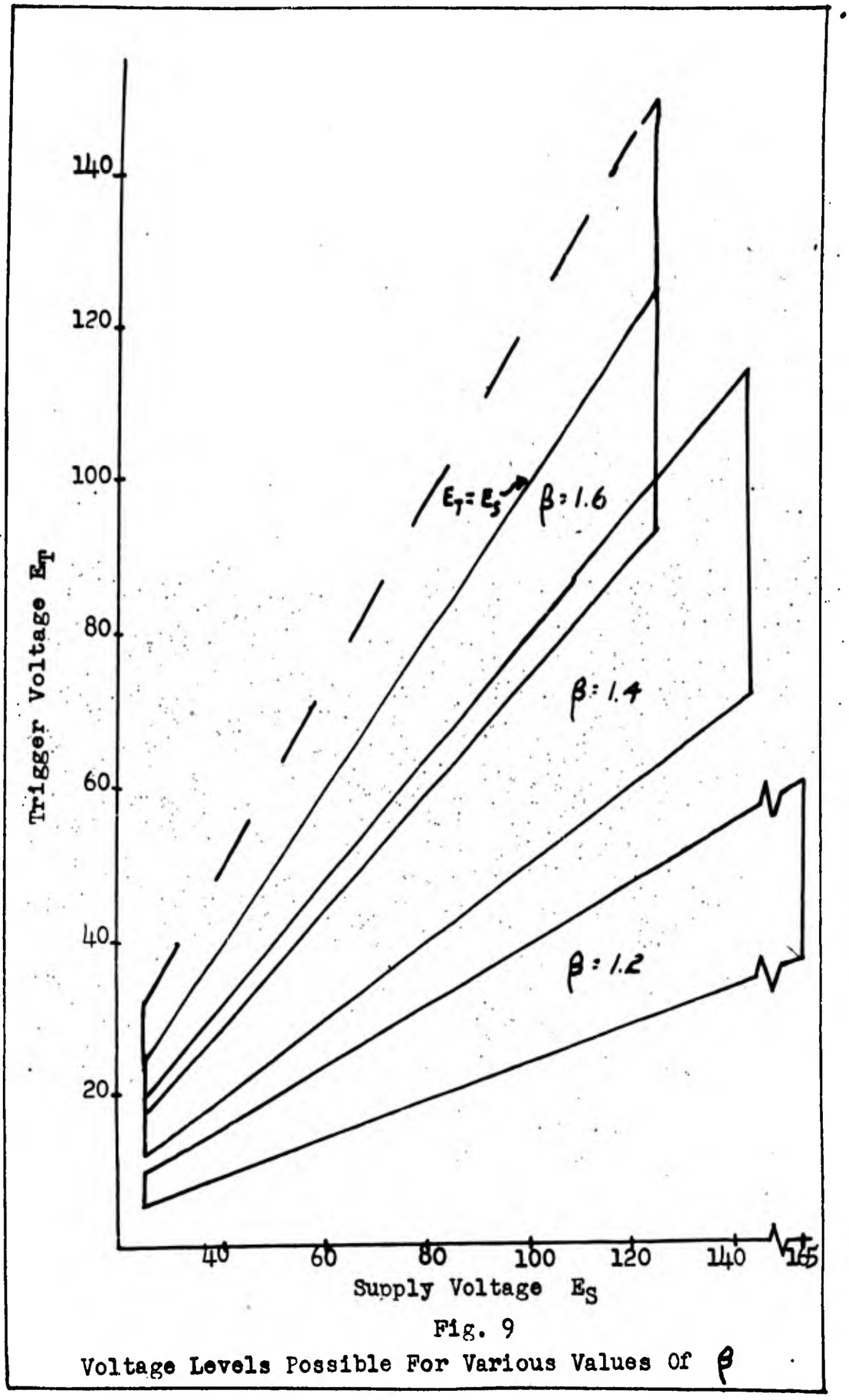


Fig. 9

Voltage Levels Possible For Various Values Of β

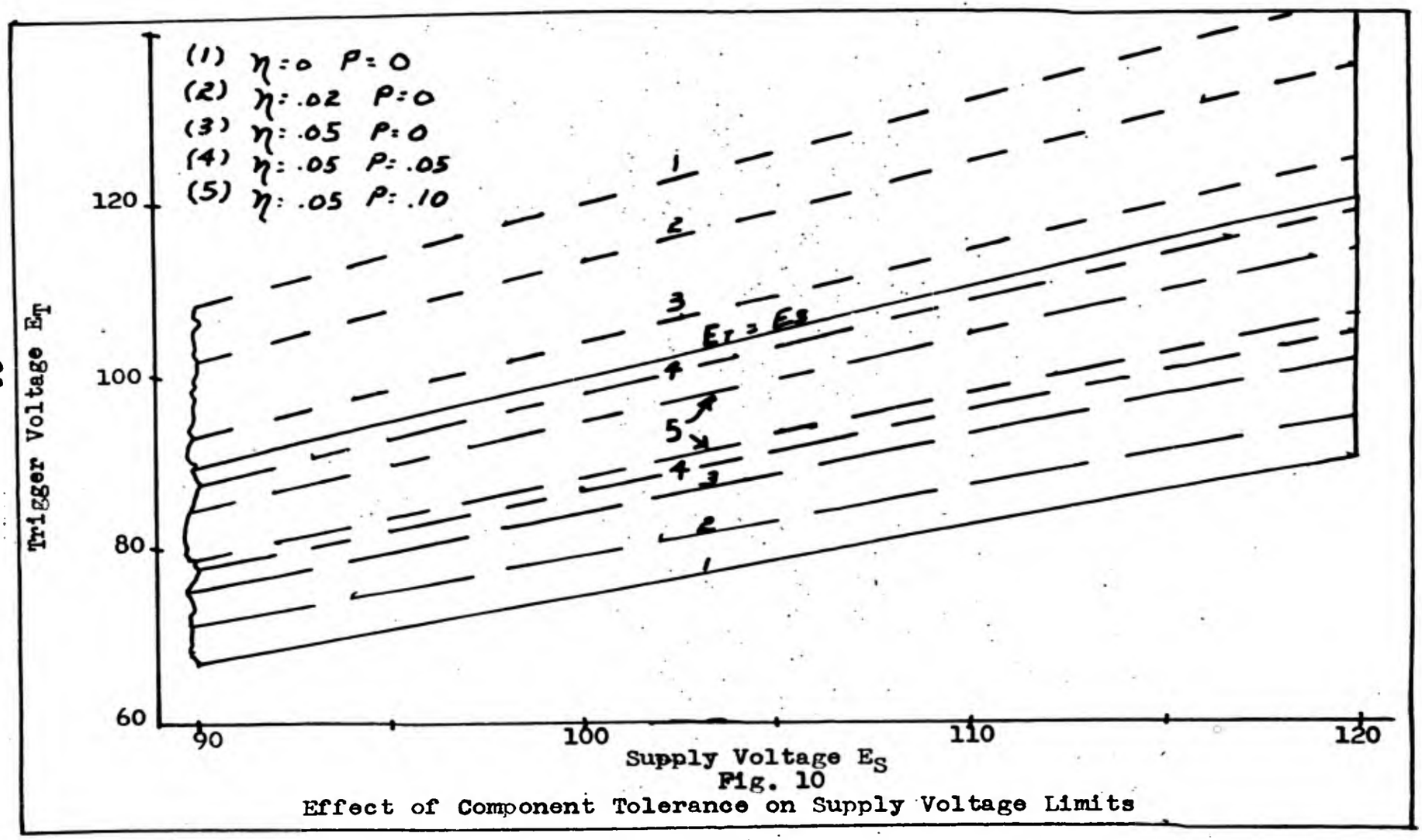


Fig. 10
Effect of Component Tolerance on Supply Voltage Limits

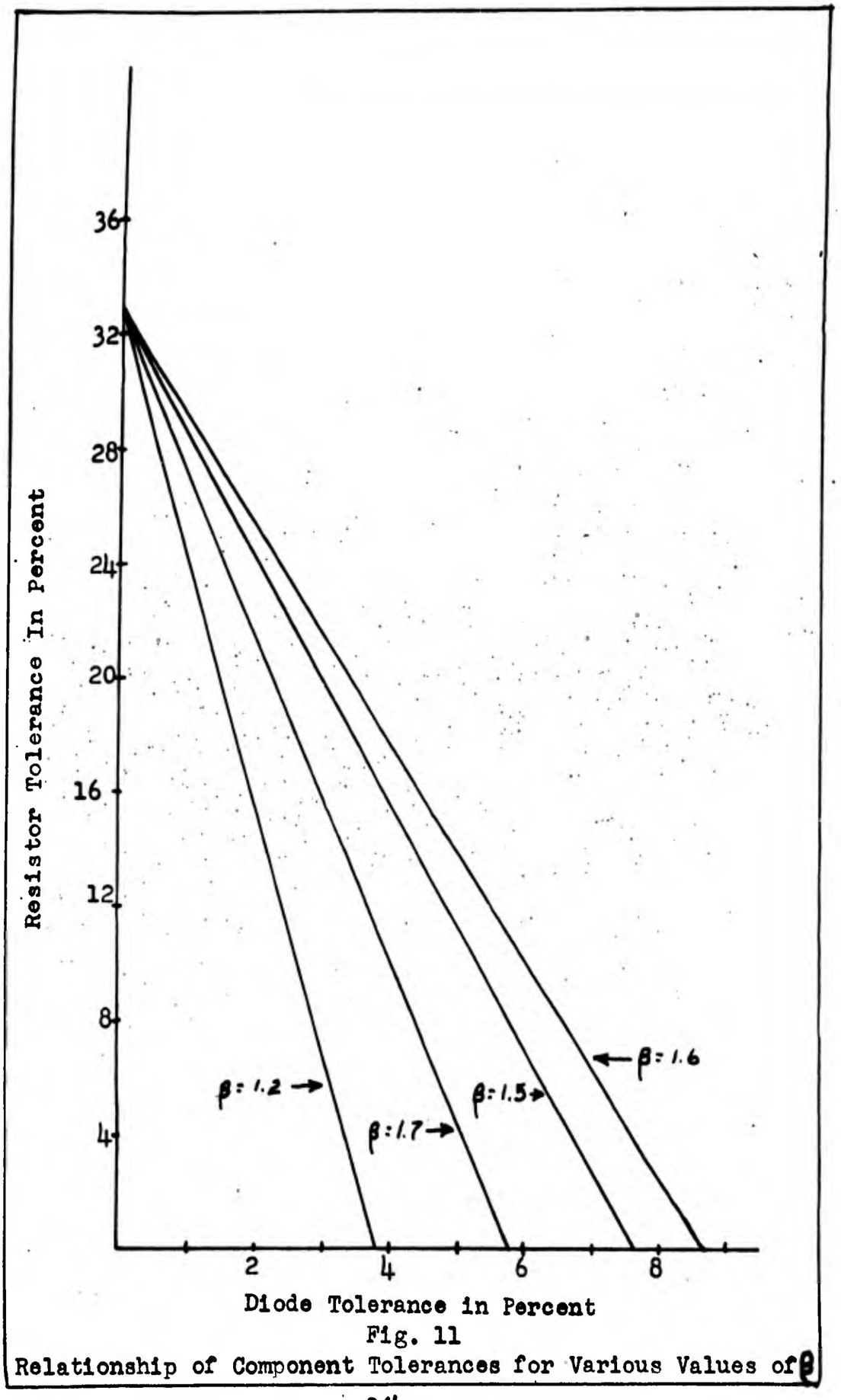


Fig. 11

Relationship of Component Tolerances for Various Values of β

is defined to be the number of inputs E_0 will drive. The important time constants are

$$\tau_1 = R_1 C_1 \tag{16}$$

$$\tau_2 = \frac{2 R_x C_2}{3} \tag{17}$$

$$\tau_3 = \frac{R_x C_1}{K} \tag{18}$$

Internal capacitance of P-N-P-N diodes is less than 200 $\mu\mu f$ and its effect is minimized when C_1 and C_2 are at least 20 times greater. To facilitate further analysis, let C_1 and C_2 be .002 μf. τ_1 will determine the minimum pulse duration and the greater of τ_2 and τ_3 will set the minimum interpulse time. Let τ_s equal the larger of τ_2 and τ_3, then the equation for maximum frequency of operation becomes approximately

$$f = \frac{1}{2[\tau_1 + \tau_s]} \tag{19}$$

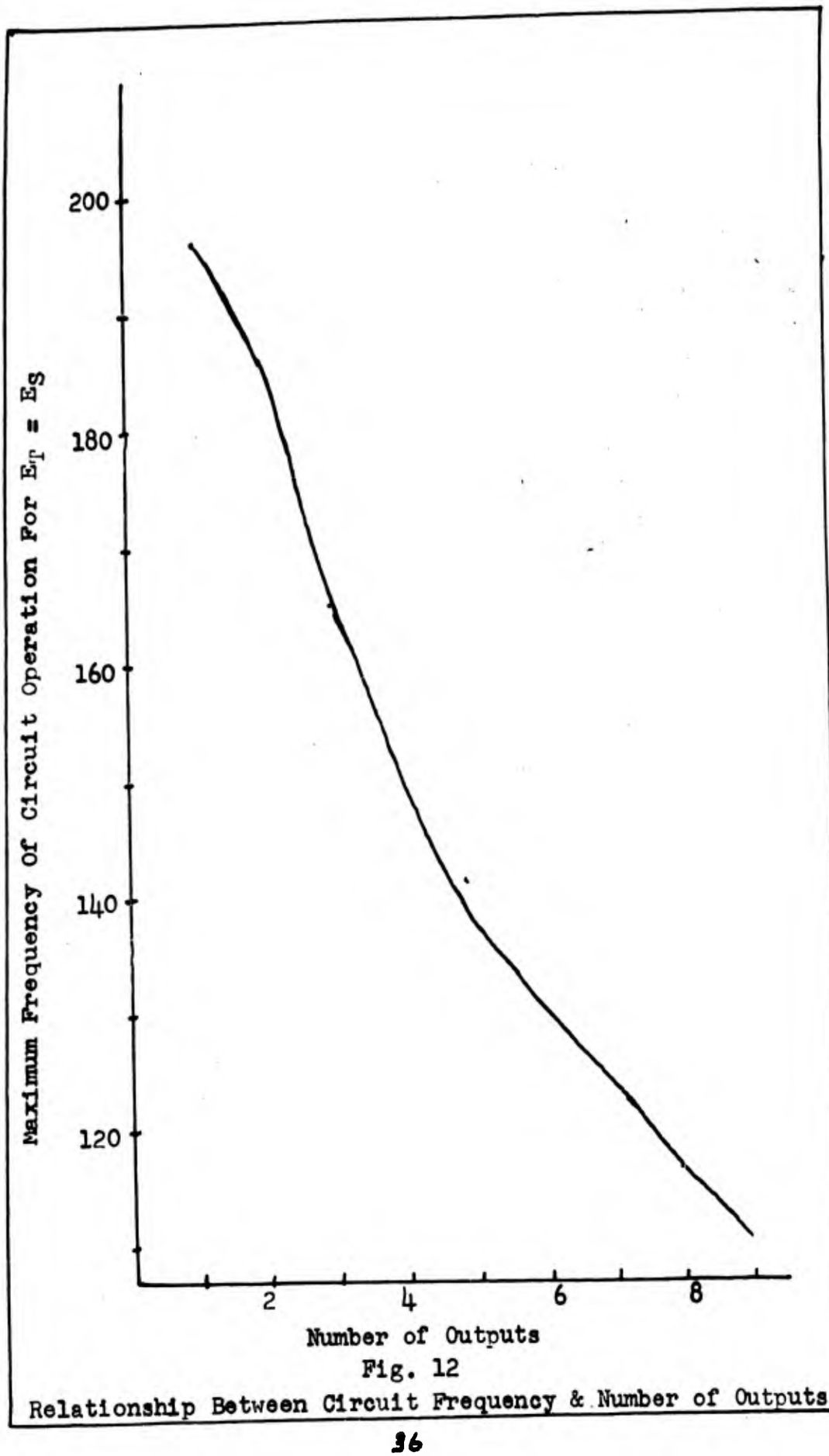


Fig. 12

Relationship Between Circuit Frequency & Number of Outputs

τ_1 and τ_3 must be as long as the switch off time for the diodes; therefore, the theoretical frequency limit of the circuit is 1.25 mc. This limit cannot be reached without exceeding the current ratings for the diodes. The limits that can be obtained are shown in Fig. 12. The curve is valid for the case where $E_T = E_S = 25$ volts, any increase in voltage will lower the frequency limit. If the voltage is doubled, the frequency limit will be halved. The maximum obtainable frequency occurs where only one output is desired and is 197 KC.

Summary and Conclusions

It has been shown that it is possible to build majority logic circuit elements using two terminal P-N-P-N diodes and passive circuit. The circuit presented in this study will accept at least three inputs; the input impedance is infinite. An output pulse from a source of virtually zero impedance will occur whenever two or more of the inputs are present. Modules can be cascaded by connecting an output of one module directly to the input of a succeeding module since no phase reversal occurs between the inputs and the output of a module. The output of a module can drive any desired number of inputs. This is an improvement over the majority logic circuit using tunnel diodes presented by Chow (Ref 2). The number of outputs in the Chow tunnel diode circuit was severely limited by the diode current tolerance; a diode current tolerance of less than 4% was necessary to obtain two outputs.

The frequency of operation for modules presented here is rather low. It also decreases appreciably when the number of outputs is greater than two; thus, the number of outputs would have to be optimized for a particular application.

The turn-off characteristics of the P-N-P-N diode limit its usefulness in majority logic circuits. Reverse bias necessary to switch the diode off had to be obtained from an additional active element within the module rather than from the input pulses. This has an adverse effect on circuit operation frequency and increases the required number of circuit components.

This circuit might find application where diodes could be obtained cheaply, where speed of operation was not a limiting factor, and where a simple basic logic element of good versatility was desired.

Some limitations presented by the two-terminal device can be overcome by using three-terminal active elements in majority logic circuits where a small signal can switch the device in both directions. More inputs could be accepted where a lower threshold value is possible; however, a phase reversal between the inputs and the output usually results when a three-terminal device is used. An investigation to determine the feasibility of using three-terminal devices in majority logic circuits should be undertaken.

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Appendix A

Tables Of Possible Trigger Voltage Range

Table I
Trigger Voltage Range For Various Values Of β And Diode Tolerance

	$\eta = 0$		$\eta = .01$		$\eta = .02$		$\eta = .03$		$\eta = .04$		$\eta = .05$	
β	$E_S \le E_T \le E_S$		$E_S \le E_T \le E_S$		$E_S \le E_T \le E_S$		$E_S \le E_T \le E_S$		$E_S \le E_T \le E_S$		$E_S \le E_T \le E_S$	
1.2	.25	.4	.265	.376	.28	.352	.296	.328				
1.3	.375	.6	.392	.574	.408	.548	.424	.522	.44	.496	.457	.47
1.4	.5	.8	.518	.772	.536	.644	.552	.716	.57	.688	.588	.66
1.5	.625	1	.645	.97	.663	.94	.681	.91	.70	.88	.72	.84
1.6	.75	1	.77	1	.79	1	.81	1	.83	1	.85	1.
1.7	.875	1	.897	1	.913	1	.94	1	.96	1	.98	1

Table II
Trigger Voltage Range For Various Values Of β And Resistor Tolerance

$\eta = .05$

β	Max P	P	$E_s \leq E_T \leq E_s$	
1.3	.015	.01	.46	.465
1.4	.08			
		.01	.59	.655
		.05	.60	.63
1.5	.12			
		.01	.724	.83
		.05	.735	.80
		.10	.748	.765
1.6	.14			
		.01	.855	1
		.05	.87	.99
		.10	.885	.947
1.7	.015			
		.01	.985	1

Vita

Robert A[redacted] Hamann was born on [redacted] in [redacted], the son of Arthur Frederick Hamann and Helen Mildred Hamann. After completing his work in 1951 at [redacted], he enrolled at the University of [redacted] He graduated in June 1955 with the degree of Bachelor of Science in Electrical Engineering. After receiving his commission as Lieutenant in the USAF Reserve, he entered active duty in January 1956. His military assignments prior to his coming to the Air Force Institute of Technology was as Communications Officer in AACS and as Project Engineer at Air Force Cambridge Research Center.

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This thesis was typed by Mrs. Elisabeth Rath

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