Report on

THE ENIAC

(Electronic Numerical Integrator and Computer)

Developed under the supervision of the
Ordnance Department, United States Army

OPERATING MANUAL

Report Documentation Page

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Moore School of Electrical Engineering

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June 1, 1946

A REPORT ON THE ENIAC

(Electronic Numerical Integrator and Computer)

Report of Work under Contract No. W-670-ORD-4926

Between

Ordnance Department, United States Army
Washington, D. C.

and

The University of Pennsylvania
Moore School of Electrical Engineering
Philadelphia, Pa.

ENIAC OPERATING MANUAL

by

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and

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Moore School of Electrical Engineering
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INTRODUCTION TO REPORT ON THE

ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTOR (ENIAC)

0. INTRODUCTION

The Report on the ENIAC consists of five separately bound parts, as follows:

1) ENIAC Operating Manual

2) ENIAC Maintenance Manual

3) Part I, Technical Description of the ENIAC

Volume I - Chapters I to VI

4) Part I, Technical Description of the ENIAC

Volume II - Chapters VII to XI

5) Part II, Technical Description of the ENIAC

Included with the Operating Manual and Parts I and II of the Technical Descriptic are all drawings (see Table 0.3 below) which are required for understanding these reports. The Maintenance Manual assumes access to the complete file of ENIAC drawings.

Part I of the Technical Description is intended for those who wish to have a general understanding of how the ENIAC works, without concerning themselves with the details of the circuits; it assumes no knowledge of electronics or circuit theory. Part II is intended for those who require a detailed understanding of the circuits. Its organization, to a great extent, duplicates that of Part I so as to make cross referencing between the two parts easy.

The ENIAC Operating Manual contains a complete set of instructions for operating the ENIAC. It includes very little explanatory material, and hence assumes familiarity with Part I of the Technical Description of the ENIAC. The ENIAC Maintenance Manual includes description of the various test units and procedures for testing, as well as a list of common and probable sources of trouble. It assumes a complete understanding of the circuits of the ENIAC, i.e., a knowledge of both Parts I and II of the Technical Description of the ENIAC.

The Report on the ENIAC and the complete file of ENIAC drawings constitute a complete description and set of instructions for operation and maintenance of the machine. The drawings carry a number of the form PX-n-m. The following tables give the classification according to this numbering system.

TABLE 0.1

Values of n	Division
1	General
2	Test Equipment
3	Racks and Panels
4	Trays, Cables, Adaptors, and Load Boxes
5	Accumulators
6	High Speed Multiplier
7	Function Table
8	Master Programmer
9	Cycling Unit and Initiating Unit
10	Divider and Square Rooter
11	Constant Transmitter
12	Printer
13	Power Supplies

TABLE 0.2

Values of n	Subject
101-200	Wiring Diagrams
201-300	Mechanical Drawings
301-400	Report Drawings
401-500	Illustration Problem Set-Ups.

The reader of this report will be primarily interested in the types of drawings listed in the following paragraphs. A table on page 4 gives the corresponding drawing number for each unit of the ENIAC.

1) Front Panel Drawings. These drawings show in some detail the switches, sockets, etc., for each panel of each unit. They contain the essential instructions for setting up a problem on the ENIAC.

2) Front View Drawings. There is one of these drawings for each kind of panel used in the various units of the ENIAC. These show the relative position of the trays and the location of the various neon lights. Since these drawings show the neon lights, they can be used to check the proper operation of the various units.

3) Block Diagrams. These drawings illustrate the logical essentials of the internal circuits of each unit. That is, resistors, condensers, and some other electrical details are not shown; but complete channels (paths of pulses or gates representing numbers or program signals) are shown in all their multiplicity. These drawings will be of interest to those who are interested in Parts I and II of the Technical Report.

4) Cross-section Diagrams. These drawings are electronically complet except that only one channel is shown where there is more than one. Thus, these drawings show every resistor and condenser and any other electronic elements belonging to any circuit. These drawings will be of particular interest to the maintenance personnel and to those reading Part II of the technical report.

5) Detail Drawings. All other drawings of the ENIAC come under this heading. A complete file of drawings is available at the location of the ENIAC.

Table 0.3
ENIAC DRAWINGS

Unit	Front Panel	Front View	Block Diagram	Cross - Section
Initiating Unit	PX-9-302 9-302R	PX-9-305	PX-9-307	
Cycling Unit	PX-9-303 9-303R	PX-9-304	PX-9-307	
Accumulator	PX-5-301	PX-5-305	PX-5-304	PX-5-115
Multiplier	PX-6-302 6-302R 6-303 6-303R 6-304 6-304R	PX-6-309	PX-6-308	PX-6-112A 6-112B
Function Table	PX-7-302 7-302R 7-303 7-303R	PX-7-305	PX-7-304	PX-7-117 7-118
Divider and Square Rooter	PX-10-301 10-301R	PX-10-302	PX-10-304	
Constant Transmitter	PX-11-302 11-302R 11-303 11-303R 11-304 11-304R	PX-11-306	PX-11-307	PX-11-116 11-309 (C.T. and R.
Printer	PX-12-301 12-301R 12-302 12-302R 12-303 12-303R	PX-12-306	PX-12-307	PX-12-115
Master Programmer	PX-8-301 8-301R 8-302 8-302R	PX-8-303	PX-8-304	PX-8-102

Other drawings of particular interest:

Floor Plan	PX-1-302	IBM Punch and	PX-12-112
A.C. Wiring	PX-1-303	Plugboard	PX-12-305
IBM Reader and	PX-11-119	Pulse Amplifier and	PX-4-302
plugboard	PX-11-305	Block Diagram	PX-4-301

Interconnection of Multiplier and Accumulators PX-6-311
Interconnection of Divider and Accumulators PX-10-307

The front view drawings and the large front panel drawings (whose numbers do not end with "R") are bound as a part of the Operator's Manual.

Included with the report is a folder containing all the drawings listed in the above table except the large front panel (see above) drawings.

1. GENERAL INSTRUCTIONS FOR OPERATING PERSONNEL

1. Inform maintenance personnel immediately of any trouble and note same in the log book.

2. Occasionally check the filament fuse indicator lights (refer to front view drawings bound in this volume); if any are out turn off the d-c power (switch is located on a-c distribution panel, see PX-1-304).

3. If ENIAC shuts down from overheating do not try to restart; call maintenance personnel. If any panel runs consistently much hotter than the others, do the same.

4. The d-c power should be turned on only with operation switch (either on cycling unit or on the hand control) turned to "continuous". After the d-c has been on a few seconds it may be turned to either of the other two positions. Failure to follow this rule causes certain d-c fuses to blow, -240 and -415 in particular.

5. As a general matter certain units not being used may have their heaters turned off. In such cases it is unnecessary to remove the d-c power or even to turn off the d-c power when turning on these units. On the other hand th three panels of the constant transmitter must be turned on or off simultaneously.

6. Do not remove any covers, front or back.

7. Do not open d-c fuse cabinet with the d-c power turned on. This not only exposes a person to voltage differences of around 1500 volts but the

person may be burned by flying pieces of molten fuse wire in case a fuse should blow.

8. Padlocks are provided for locking the d-c power off. Lock the power off and carry the key with you as long as you are working on the machine.

9. Do not remove accumulator interconnector plugs, or function table or IBM machine connector cables, while the d-c is on. All other front panel plugs may be safely moved while the power is on.

10. Do not pull directly on wire or cable; always use the plug case as a grip.

11. Do not put sharp bends in cables or hang anything on them.

12. Do not leave cables dangling on the floor.

13. Do not pound or force plugs; if they do not respond to steady pressure notify maintenance personnel.

14. Do not leave IBM cable connectors or portable function table connectors lying out in the open, keep in the receptacles provided. Also, make use of the ramps to protect the cables of any such units which are connected to the ENIAC.

15. Do not force any switches.

16. Keep the door to the room closed to keep out dust, avoid stirring up or producing dust.

17. Always move the portable function tables with care. Keep the brakes on when not moving them.

2. PROBLEM SET UP REMARKS

2.1. NEED FOR SYSTEMATIC CHECKS

Since the ENIAC makes use of a hierarchy of channels (first, in that a

number of units may be carrying on computations simultaneously; second, in that it always handles ten to twenty digits of a number simultaneously; and third, in that certain units use a coded system giving four channels for each digit) running a standard check problem is not a sufficient check on the accuracy of the results. Thus, in arranging a problem for the ENIAC provision should be made for occasional systematic checks of all the units.

Procedures for systematic checking are described in some detail in the maintenance manual. Brief procedures will be outlined here for the numerical units. The following test procedures are not comprehensive tests and the experienced operator will perhaps use variations of them. In particular, the tests given below are not designed to check the operation of the various program controls. However, they are designed to check the numerical circuits in each unit and to a considerable extent check the program control used to carry out the test.

2.2. TESTING AN ACCUMULATOR

Cards should be prepared as follows:

1. P 11111 11111
2. P 00000 00001

The numbers should be so placed on a card that one group in the constant transmitter, say A_{LR}, corresponds to these numbers. Next, a master programmer stepper should be used to transmit the first number into the accumulators which are to be tested eighteen times. At this time the accumulators should read

M 99999 99998

and all stages of each decade have been checked as well as the delayed carry-over circuits. Now the stepper (used above) should cause the reader to read the next card and the number to be transmitted to the accumulators twice. This should

give

P 00000 00000

and checks the direct carry-over circuits. Note that this test assumes that the significant figure switch is set to "10". If this is not so the operator can modify the above procedure to take care of this.

This test does not check the following circuits (for a complete checking procedure see the maintenance manual):

Transmission circuits	Input channels (except for the one used)
Clearing circuits	Program controls (except for the one used)
Repeater ring	

2.3. TESTING THE MULTIPLIER

The following set of cards should be prepared.

Card	Multiplier A_{LR} (say)	Multiplicand B_{LR} (say)
1	P 00000 00000	P 11111 11111
2	P 11111 11111	P 11111 11111
3	P 11111 11111	P 22222 22222
.....		
10	P 11111 11111	P 99999 99999
11	P 22222 22222	P 11111 11111
12	P 22222 22222	P 22222 22222
.....		
82	P 99999 99999	P 99999 99999
83	P 11111 11111	M 11111 11111
84	M 11111 11111	P 11111 11111
85	M 11111 11111	M 11111 11111

On a second set of cards, or on these same cards in different fields the proper answers should be punched. Note that these answers will depend upon when ten or twenty digit products are used, that is, whether the product accumulators are used as ten or twenty digit accumulators.

There are two methods of using these cards to check the numerical circuits of the multiplier. One is to have the answer on the same card and arrange for its transmission to the product accumulators with its sign changed (or the sign of one of the factors may be changed). In this case the whole sequence of cards in run and the presence of "zero" in the product accumulators indicates (with high probability since there could be compensating errors) that the numerical circuits are all right.

A second method is to run the test and cause the answers to be punched on other cards. These results may then be compared with standard answers by use of the reproducing punch.

This procedure does not check the following:

Rounding off circuits

Program controls (other than the one used).

2.4. TO TEST A FUNCTION TABLE

An accumulator is used to build up the argument. A program control on the function table has its function switch set to "-2" and a second switch has its argument set to "+2".

The programming is so arranged that the "-2" program is activated and the output sent to an accumulator associated with the printer. The result is punched on a card, "one" is added to the argument, and the process repeated.

The master programmer can be used to repeat the "-2" program 96 times and then alternately activate the "-2" and the "+2" program four more times. (Or various other schemes may be devised to obtain all 104 entries to the function table.) The cards punched in this manner can then be compared with a standard deck.

Note that the above check is not a systematic check of the numerical circuits as a whole. In other words this check should be repeated if any switches on the portable table (or on panel No. 2) are changed.

Furthermore, the above procedure does not check the various program controls of the function table.

2.5. TO TEST THE DIVIDER AND SQUARE ROOTER

The divider and square rooter can best be checked by performing test division problems and square root problems. Drawing PX-10-111 gives the neons which should be lit at various places in the process. The operator can check against this by going through the problem at one addition time.

2.6. CONSTANT TRANSMITTER TEST PROCEDURE .

The 1, 2, 2', 4 channels in the constant transmitter can all be checked simultaneously by reading cards with nine punches on them. Since it is undesirable that the same number be punched in all columns of a card (this weakens a card increasing the probability of "jamming" in the feeding mechanism of the IBM machines) it is suggested that cards be prepared as follows.

1) 9's in groups A_{LR} and B_{LR}
2) 9's in groups C_{LR} and D_{LR}
3) 9's in groups E_{LR} and F_{LR}

4) 9's in groups G_{LR} and H_{LR}

5) Four more cards similar to above but with minus punches.

The programming should be arranged so that the numbers are transmitted into accumulators when they can be inspected visually or perhaps punched on other cards and compared with a standard deck using the reproducing punch.

Note that J_{LR} and K_{LR} should be checked in a similar manner. (These only need be checked for the numbers used in the set-up provided they are re-checked any time that some of the switch settings are changed.)

This procedure does not check all the program controls.

2.7. PRINTER TEST PROCEDURE

The printer can be tested by causing all possible digits in each channel to be punched and by checking the PM delays. The following cards should be prepared.

1) P 01234 56789
2) P 11111 11101
3) P 11111 11011
. . . . . .
10) P 01111 11111
11) P 11111 11111

The programming should be arranged to cause the numbers on the test cards to be read by the IBM reader, transmitted to the printing accumulators, and the result punched. The resulting cards may be compared with a standard deck by use of the reproducing punch.

Card number one has the numbers 0 to 9 punched in it to prevent the same digit from being punched all across a card.

If any decades of the master programmer are used in printing they may be checked at this time by transmitting the program pulse (used to activate the above sequence) into each decade direct input.

This constitutes a complete test of the printer.

2.8. TESTING FOR TRANSIENT FAILURES

If transient failures are suspected a master programmer stepper should be used to repeat the appropriate test (such as one of those above) a large number of times.

In case of an accumulator this can be done using only one card (say, P 99999 99999) and using a second program control set to αC (receive on α and correct) to obtain the one pulse in the units decade.

For the multiplier it becomes necessary to punch the answers on the cards with the factors (see 2.3) and cause these to be transmitted to the product accumulators for each multiplication. If more than ten digit answers are used the adjusted answer to card 83 must be carefully prepared in order to get minus the answer from the constant transmitter to the product accumulators (since the constant transmitter only complements at most ten digits at a time).

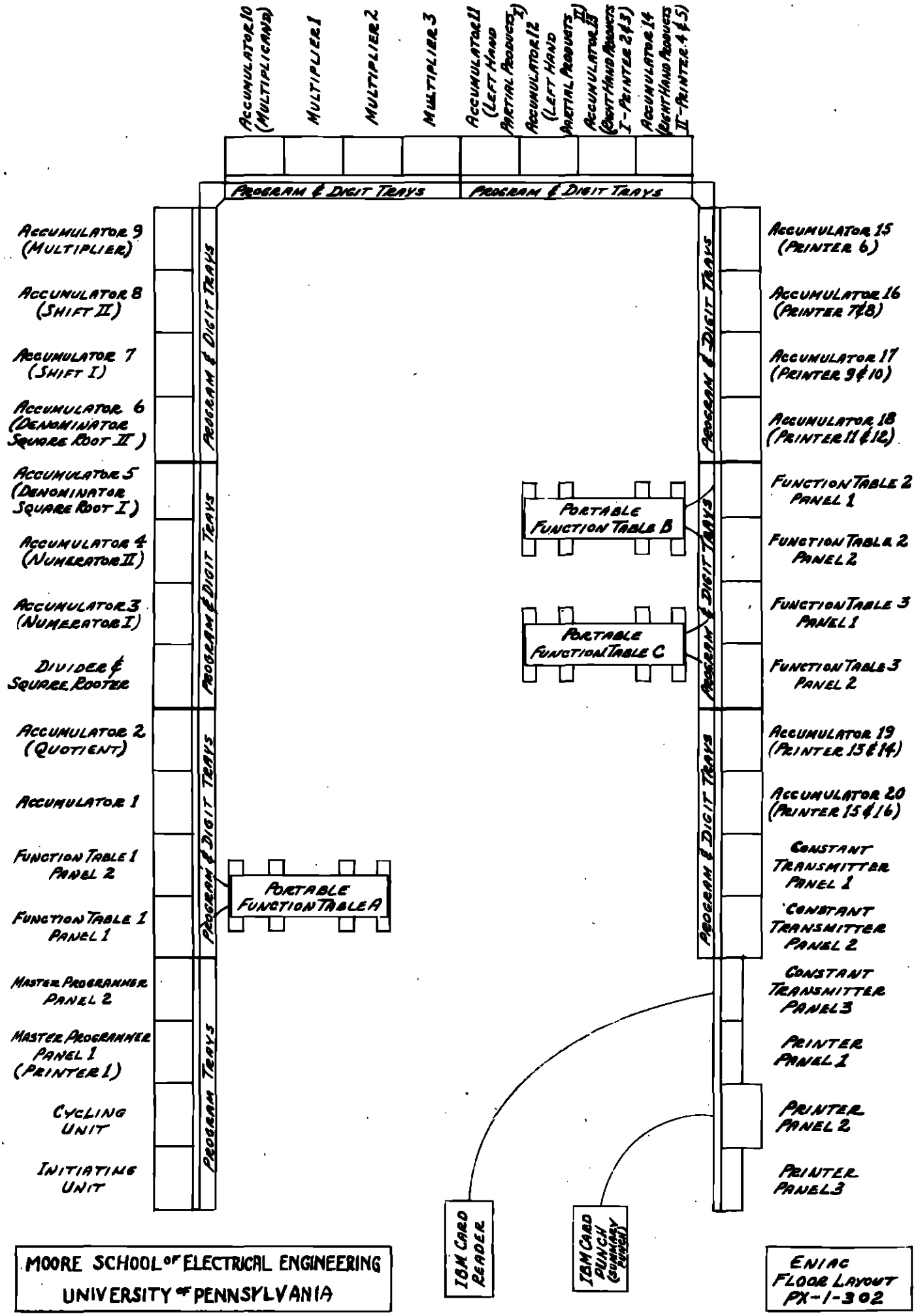
Repetition of a function table test is straight forward. It may be worth while to receive into a twenty digit accumulator and repeat the transmission 10^4 times, say, and see if the proper number is obtained.

The square root of zero is perhaps the easiest test to repeat on the divider-square rooter.

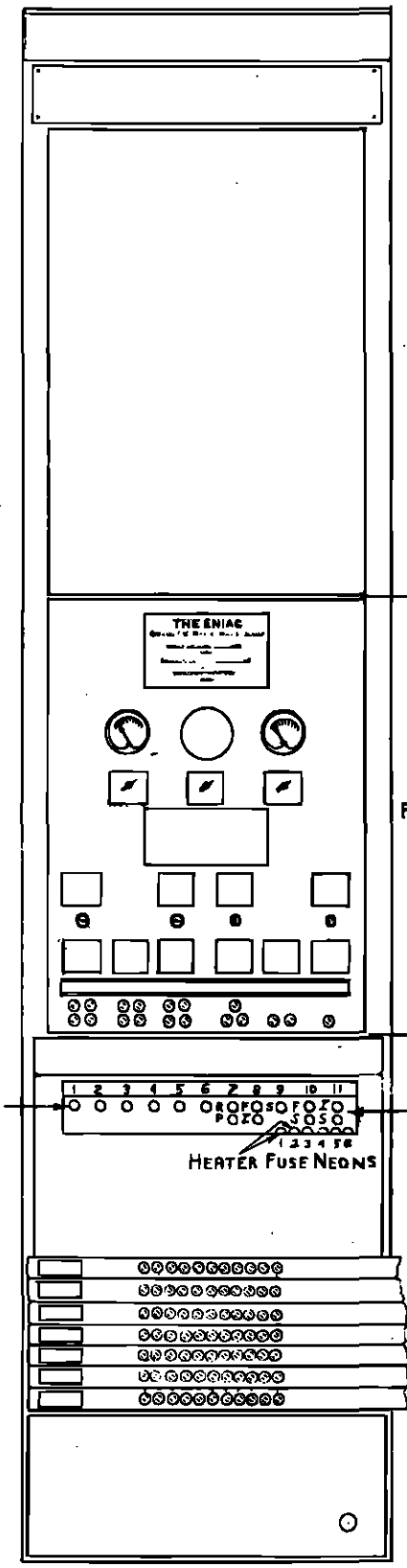
The constant transmitter can be caused to transmit any group repeatedly to some accumulator. Dust particles may cause transient relay failures, so avoid stirring up dust in the ENIAC room. Also, if any relay case is removed, always

replace in exactly the same position in order not to disturb dust inside the case.

Transient failures in the printer are probably relay failures. See maintenance manual for list of probable failures.

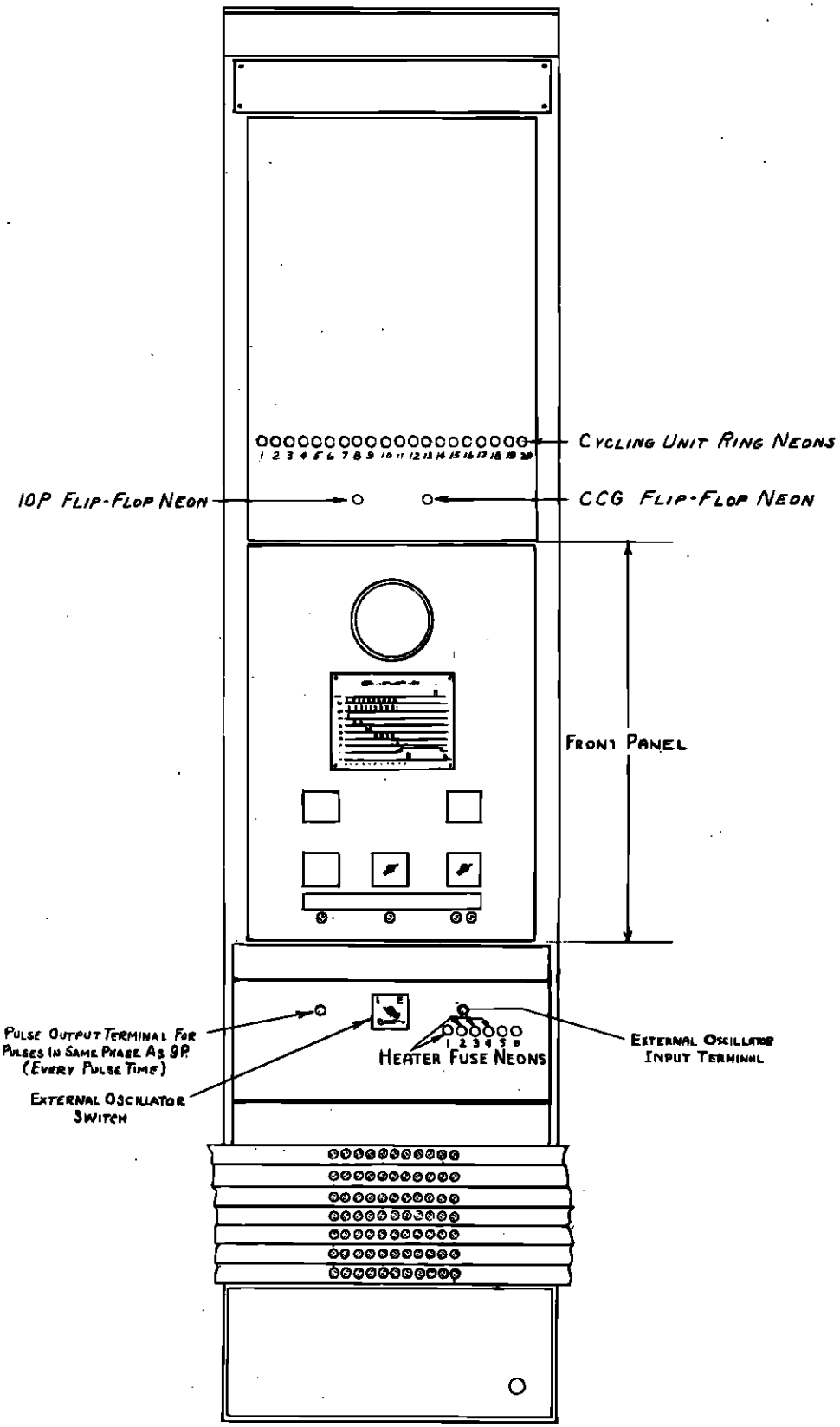

Accumulator 10 (Multiplicand)
Multiplier 1
Multiplier 2
Multiplier 3
Accumulator 11 (Left Hand Partial Products I)
Accumulator 12 (Left Hand Partial Products II)
Accumulator 13 (Right Hand Products I - Printer 2 & 3)
Accumulator 14 (Right Hand Products II - Printer 4 & 5)
Program & Digit Trays
Program & Digit Trays
Accumulator 9 (Multiplier)
Accumulator 8 (Shift II)
Accumulator 7 (Shift I)
Accumulator 6 (Denominator Square Root II)
Accumulator 5 (Denominator Square Root I)
Accumulator 4 (Numerator II)
Accumulator 3 (Numerator I)
Divider & Square Rooter
Accumulator 2 (Quotient)
Accumulator 1
Function Table 1 Panel 2
Function Table 1 Panel 1
Master Programmer Panel 2
Master Programmer Panel 1 (Printer 1)
Cycling Unit
Initiating Unit
Program & Digit Trays
Program & Digit Trays
Program & Digit Trays
Program & Digit Trays
Program & Digit Trays
Program & Digit Trays
Program Trays
Portable Function Table A
Portable Function Table B
Portable Function Table C
Accumulator 15 (Printer 6)
Accumulator 16 (Printer 7 & 8)
Accumulator 17 (Printer 9 & 10)
Accumulator 18 (Printer 11 & 12)
Function Table 2 Panel 1
Function Table 2 Panel 2
Function Table 3 Panel 1
Function Table 3 Panel 2
Accumulator 19 (Printer 13 & 14)
Accumulator 20 (Printer 15 & 16)
Constant Transmitter Panel 1
Constant Transmitter Panel 2
Constant Transmitter Panel 3
Printer Panel 1
Printer Panel 2
Printer Panel 3
IBM Card Reader
IBM Card Punch (Summary Punch)
Moore School of Electrical Engineering
University of Pennsylvania
Eniac Floor Layout PX-1-302

1	12-18-45
2	2-6-47



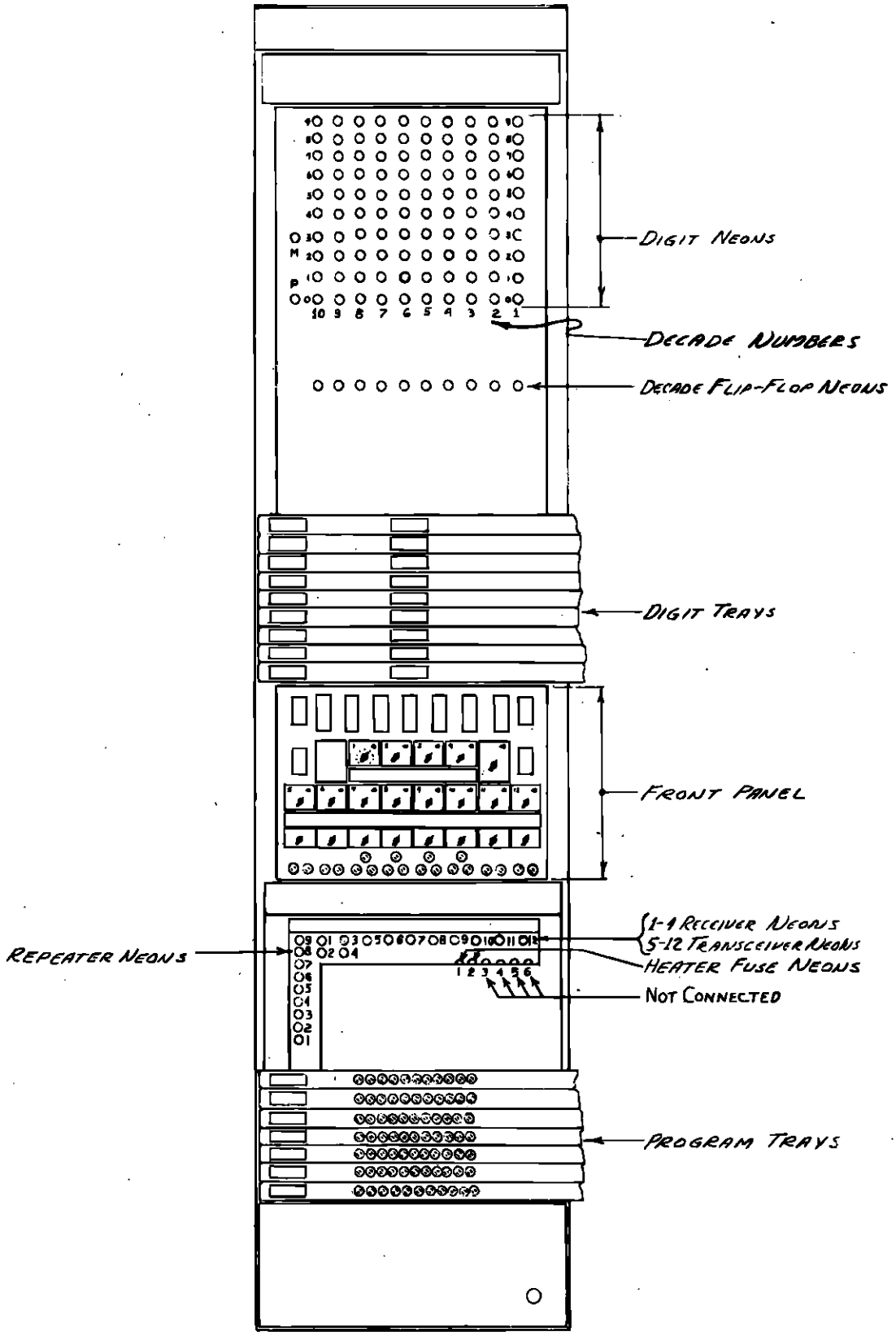
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INITIATING UNIT FRONT VIEW
PX-9-305



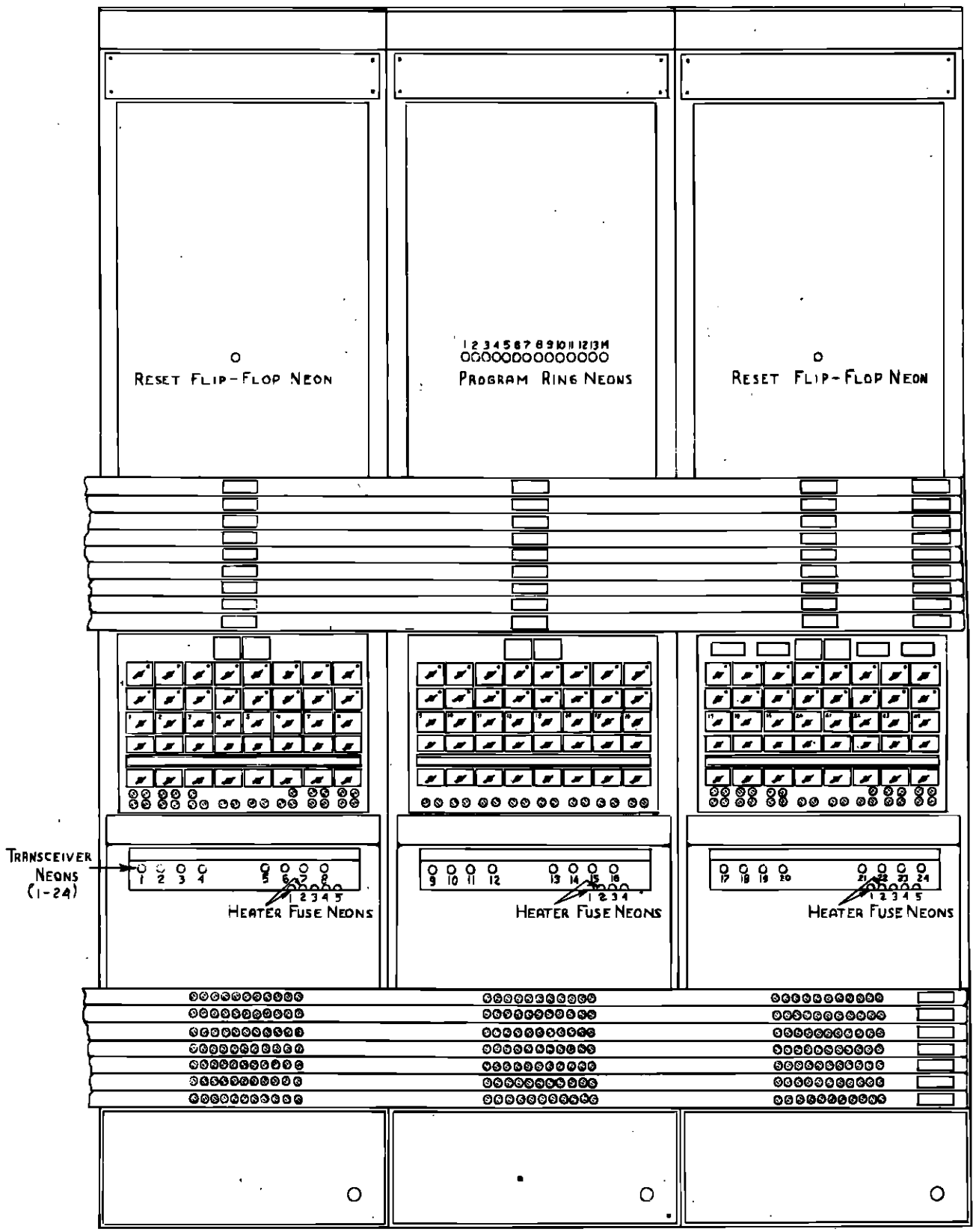
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CYCLING UNIT
FRONT VIEW
PX-9-304



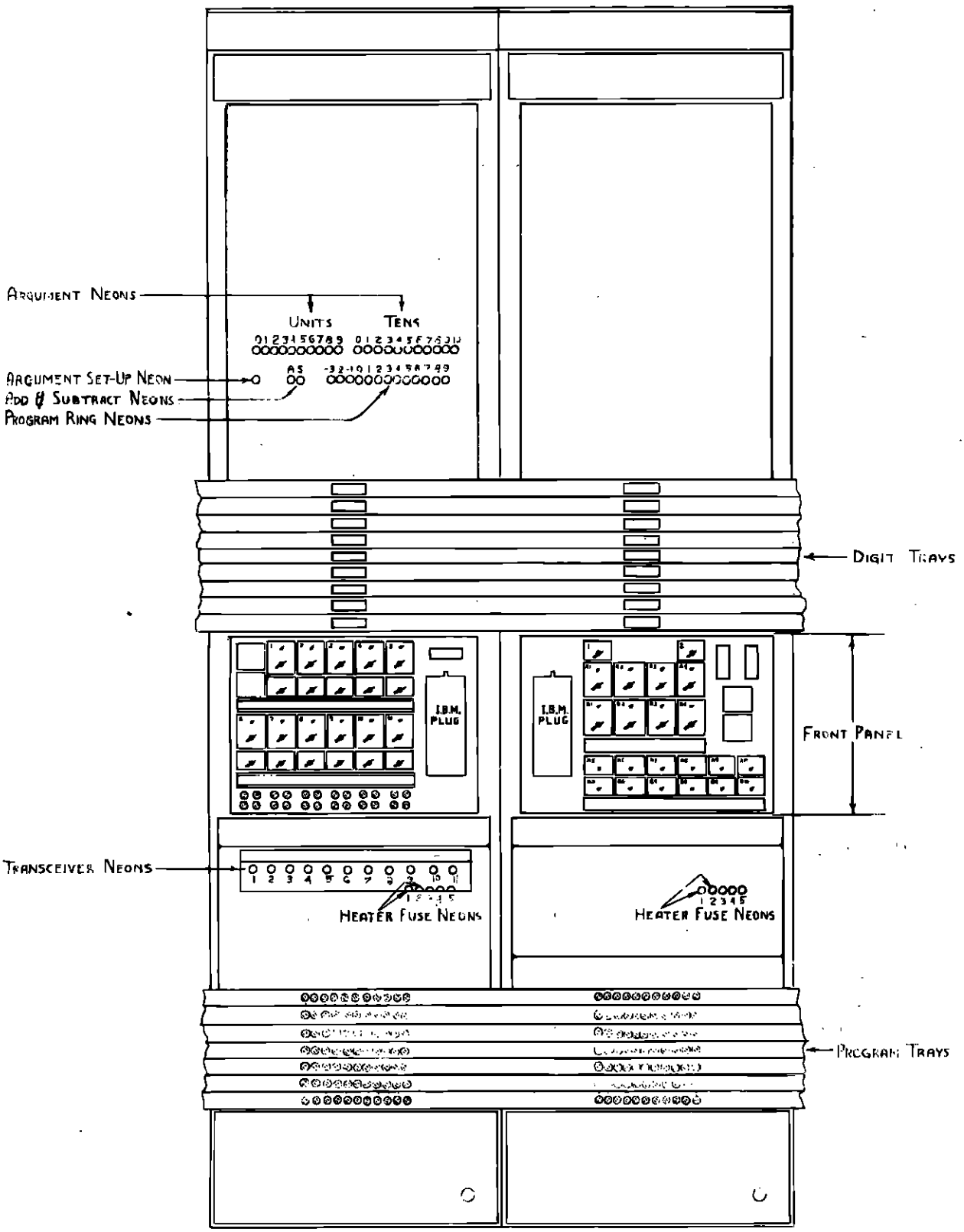
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ACCUMULATOR
FRONT VIEW
PX-5-305



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HIGH SPEED MULTIPLIER
FRONT VIEW
PX-6-309



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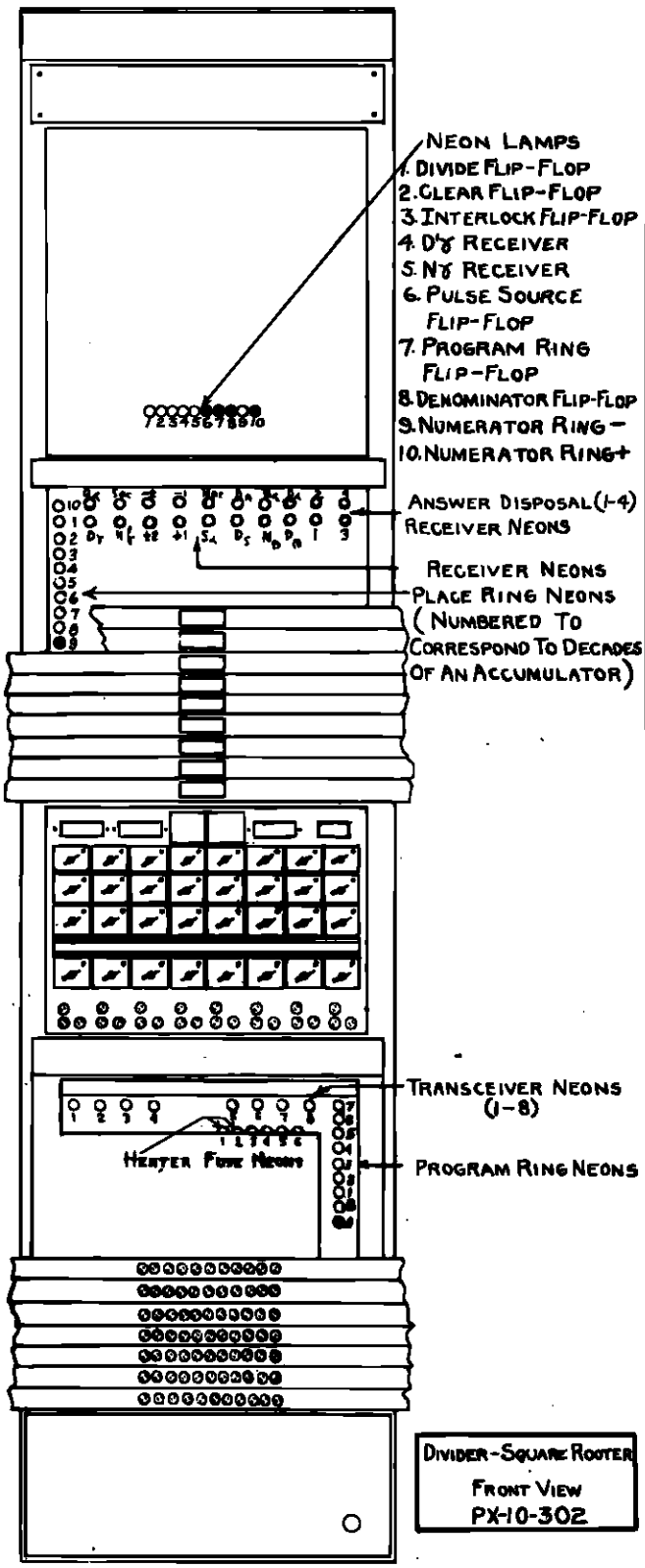
FUNCTION TABLE FRONT VIEW
PX-7-205

NEONS ON DURING DIVISION

ADD. TIME	PROG. RING	PLACE RING	RECEIVER	1	2	3	4	5	6	7	8	9	10
							D'γ	Nγ			D	N⁻	N⁺
I-1	A	9		①					ON	ON	ON		ON
2	B	9		ON					ON	ON	②	③	
3	1	9		"					ON	ON	"	"	
II-1	A	i*	D_A OR D_S	"				ON	ON		"	③	
2	A	i	-1 OR +1, Q≠C	"					ON		"	"	
S 1	A	CYCLES	N_{AC}, S≠C	"			ON		ON		"	"	
S 2	A	i-1	S_{AC}, N'γ	"					ON		"	CYCLES	
III 1	A	10-p	N_{AC}, S≠C	"			ON				"	③	
2	B	"	S_{AC}, N'γ	"							"	CYCLES	
3	1	"	D_S OR D_A	"				ON			"	③	
4	2	"	D_S OR D_A	"				ON			"	"	
5	3	"	D_S OR D_A	"				ON			"	"	
6	4	"	D_S OR D_A	"				ON			"	"	
7	5	"	D_S OR D_A	"				ON			"	"	
8	6	"		"							"	"	
9	7	"	(+1 OR -1, Q≠C)**	"							"	"	
IV-1	7	"		"		④			⑤		"		
2	7	"		"	⑥	"			"		"		
TRANSCEIVER OFF	A	9	1, 2, OR NEITHER	ON					ON	ON	ON		ON

NEONS ON DURING SQUARE ROOTING

ADD. TIME	PROG. RING	PLACE RING	RECEIVER	1	2	3	4	5	6	7	8	9	10
							D'γ	Nγ			D	N⁻	N⁺
I-1	A	9		①					ON	ON	ON		ON
2	B	9							ON	ON	"		ON
3	1	9							ON	ON	"		ON
4	A	9	Dγ, +1						ON		"		ON
II-1	A	i*	D_S OR D_A					ON	ON		"	③	
2	A	i	+2 OR -2 Dγ						ON		"	"	
S 1	A	CYCLES	-1 OR +1 S≠C, N_{AC}				ON		ON		"	"	
S 2	A	i-1	-1 OR +1 N'γ, S_{AC}				ON		ON		"	CYCLES	
III-1	A	10-p	-1 OR +1, S≠C, N_{AC}				ON				"	③	
2	B	"	N'γ, S_{AC}								"	CYCLES	
3	1	"	D_A OR D_S					ON			"	③	
4	2	"	D_A OR D_S					ON			"	"	
5	3	"	D_A OR D_S					ON			"	"	
6	4	"	D_A OR D_S					ON			"	"	
7	5	"	D_A OR D_S					ON			"	"	
8	6	"									"	"	
9	7	"	(-2 OR +2, Dγ)**								"	"	
IV-1	7	"				④			⑤		"	"	
2	7	"			⑥	"			"		"	"	
TRANSCEIVER OFF	A	8	3, 4, OR NEITHER						ON	ON	ON		ON



DIVIDER-SQUARE ROOTER
FRONT VIEW
PX-10-302

FOOT NOTES

① ON IF PREVIOUS PROGRAM WAS A DIVISION.

② ON IF DENOMINATOR IS POSITIVE WHEN RECEIVED IN DENOMINATOR ACCUMULATOR.

③ IF BEFORE DENOMINATOR IS ADDED TO OR SUBTRACTED FROM NUMERATOR, THE NUMERATOR IS POSITIVE, NEON #4 IS ON; OTHERWISE NEON #3 IS ON.

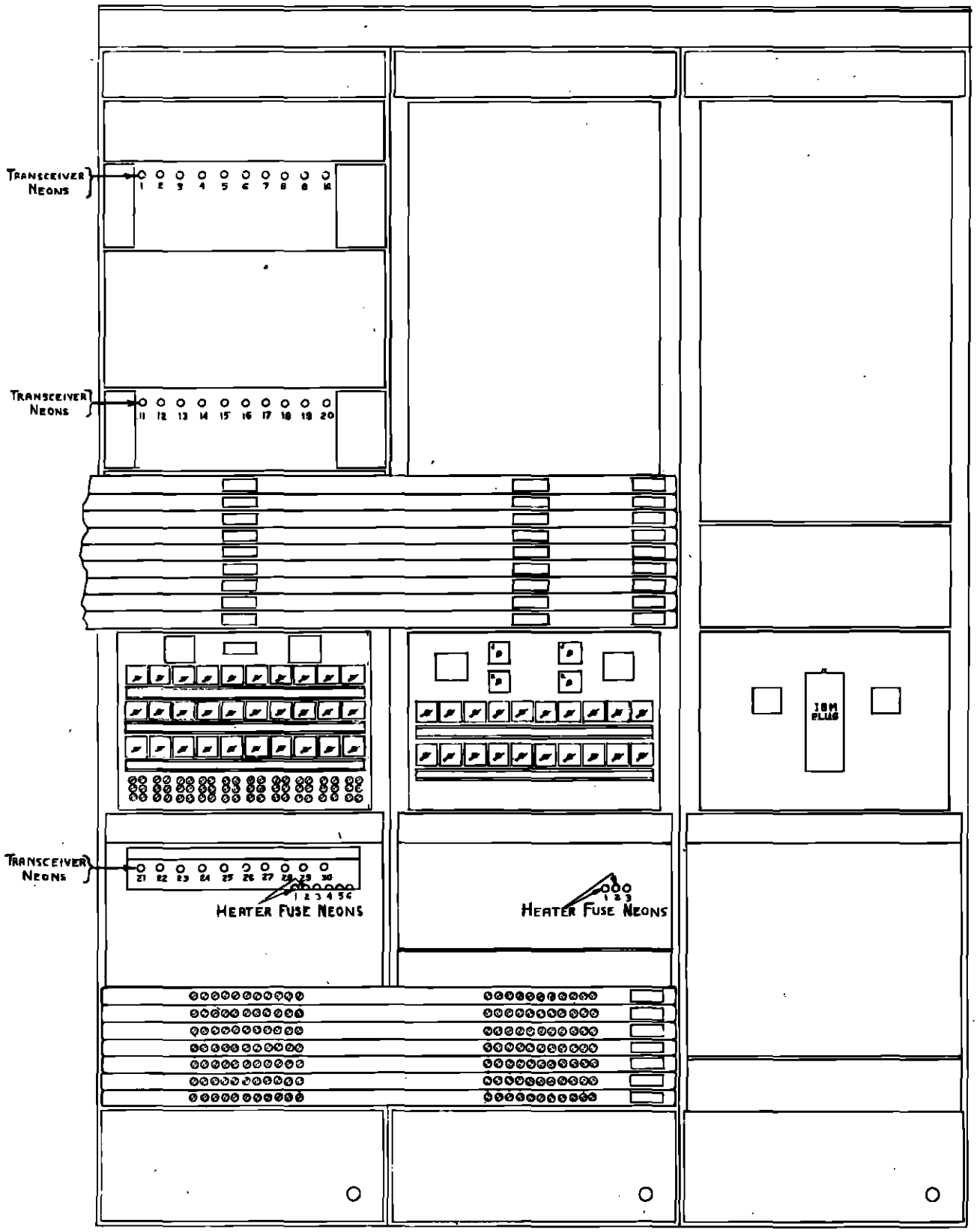
④ GOES ON WHEN INTERLOCK PULSE IS RECEIVED.

⑤ GOES ON ONE ADDITION TIME AFTER III-9

⑥ GOES ON: a- IN NI CASE, TWO ADDITION TIMES AFTER III-9.
b- IN I CASE, IN WHICHEVER OCCURS LATER: TWO ADDITION TIMES AFTER III-9 OR ONE ADDITION TIME AFTER NEON 7

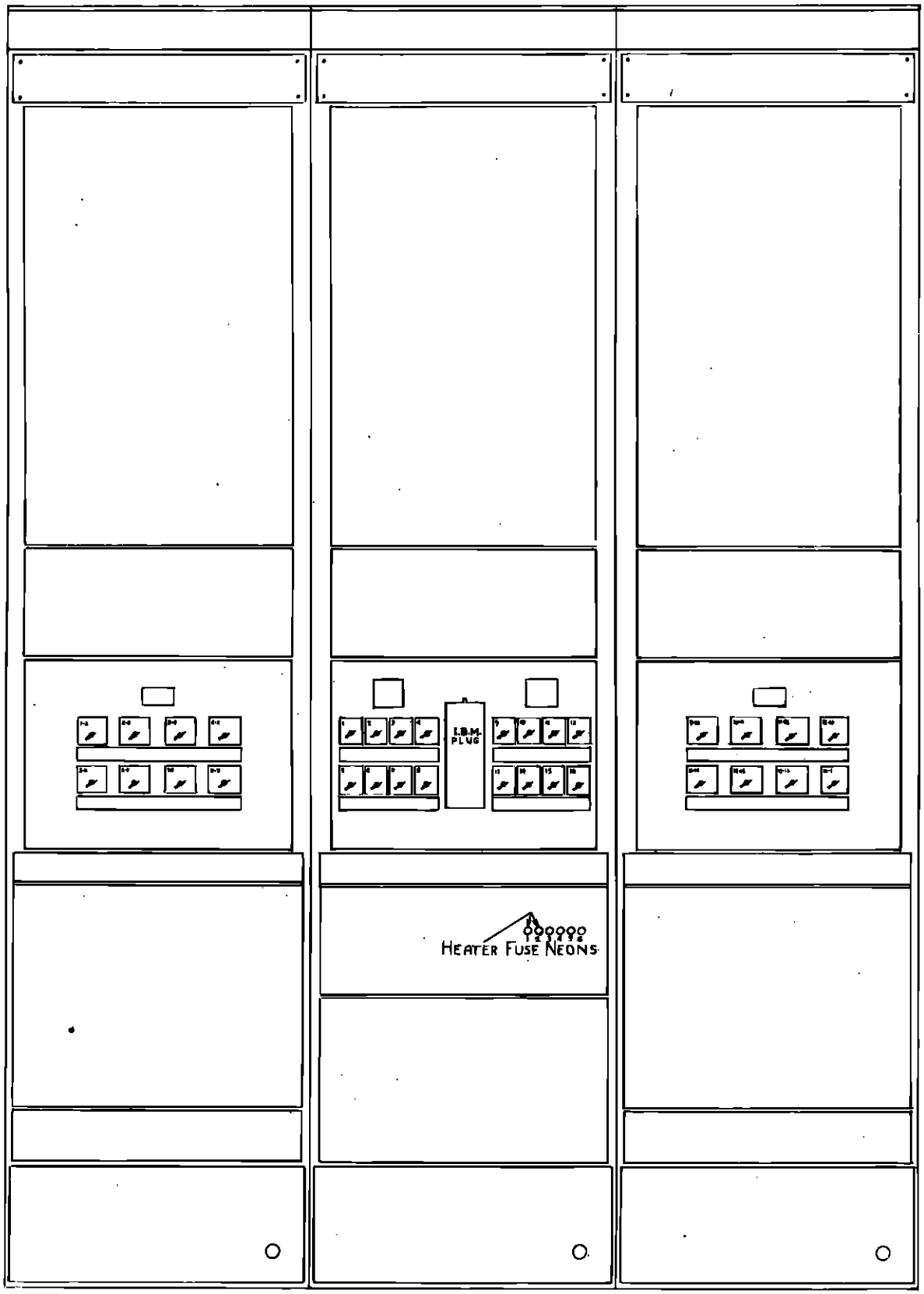
* $9 \geq i \geq 10\text{-}p$ WHERE p IS THE SETTING OF THE PLACES SWITCH.

** ONLY IF NO OVERDRAFT RESULTS.



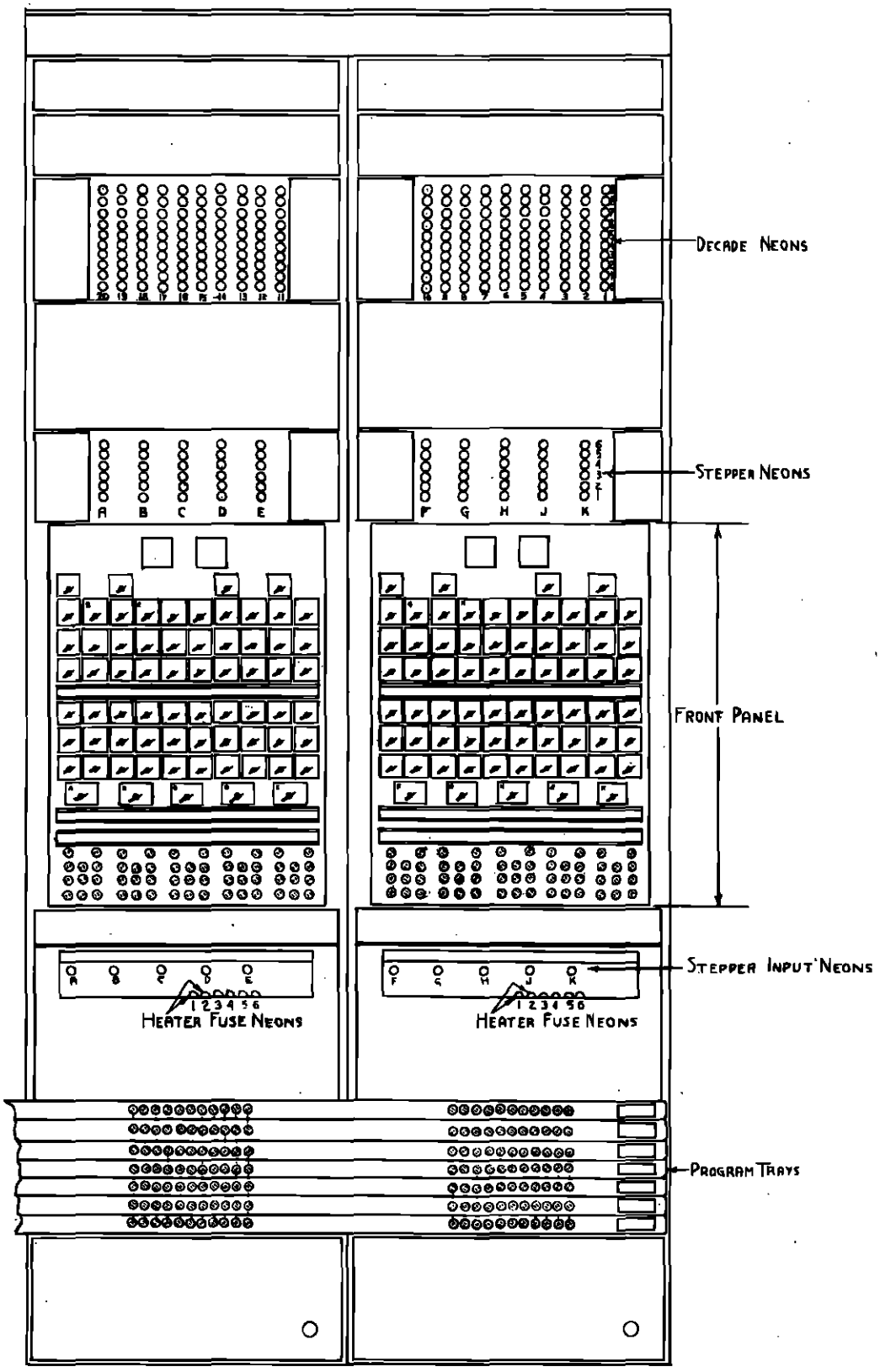
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CONSTANT TRANSMITTER FRONT VIEW PX-11-506



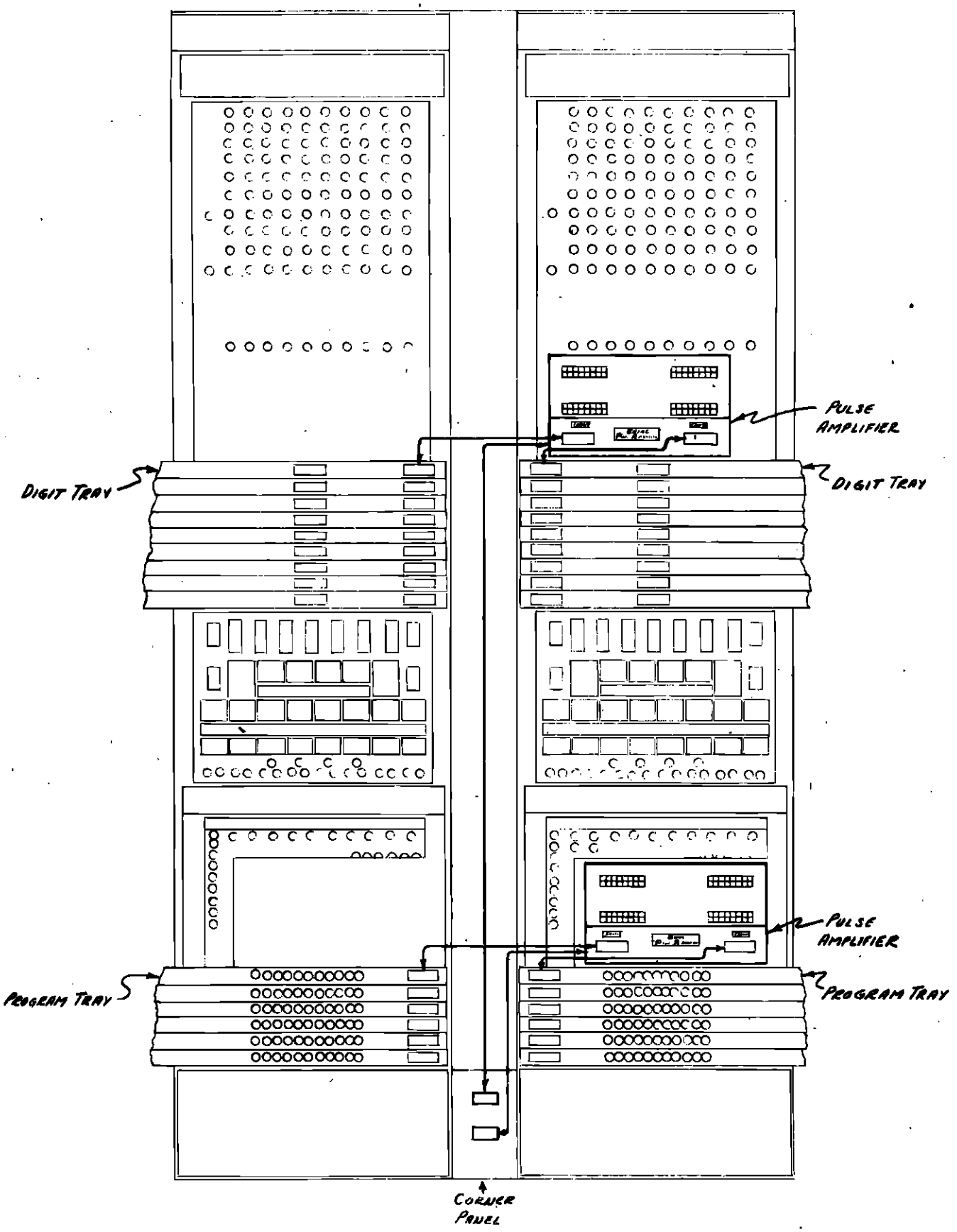
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PRINTER
FRONT VIEW
PX-12-306



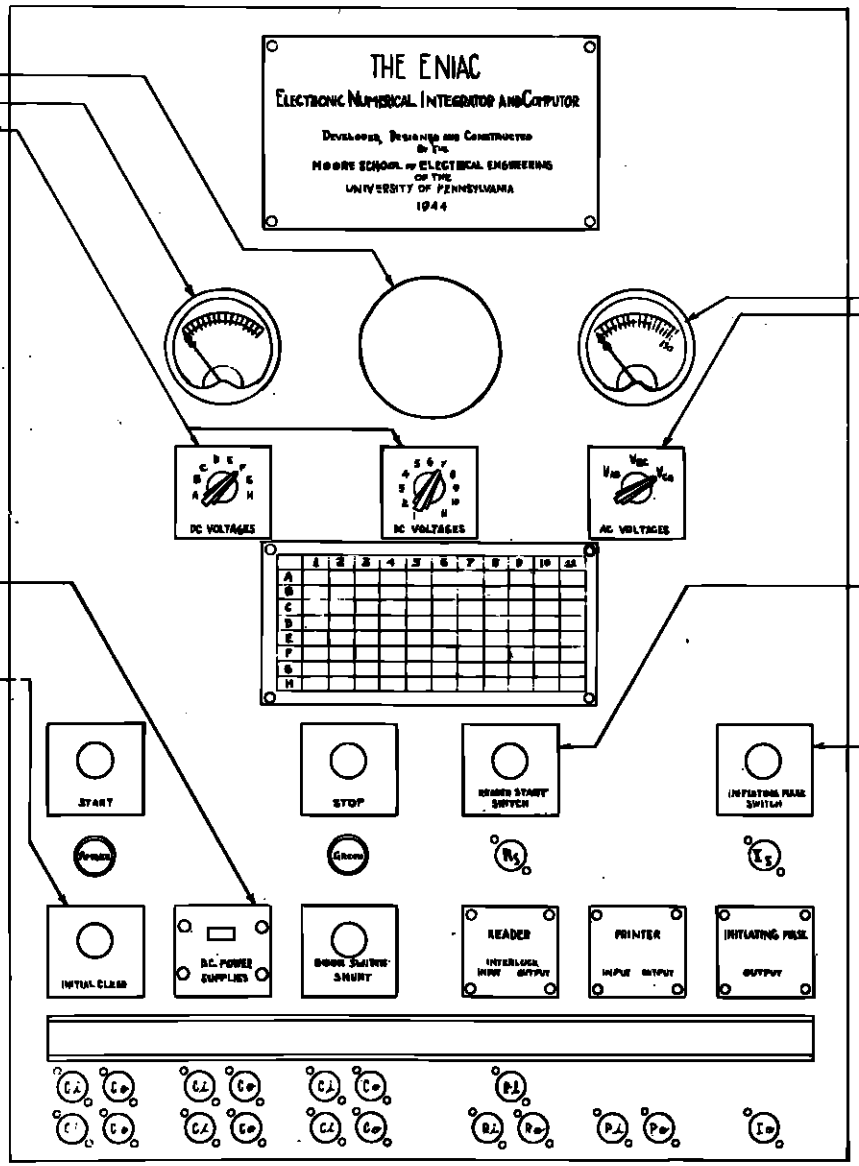
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MASTER PROGRAMMER FRONT VIEW
PX-8-303



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PULSE AMPLIFIER
INTERCONNECTION DIAGRAM
PX-4-302



D-C voltage hum oscilloscope

D-C voltage meter

D-C voltage selector switches

D-C voltage chart

White numbers on the voltage chart indicate voltages at the ends of a power supply. Black numbers indicate voltage pairs in which at least one voltage is derived from a bleeder tap.

Behind the voltage chart are the oscilloscope adjustments.

The d-c voltage amplitude and the a-c hum amplitude of every voltage of the ENIAC may be measured with respect to some other voltage at this panel.

Start and stop switches

Pushing the start switch turns the amber light on and starts the initiating sequence for the ENIAC, turning on the d-c power supplies, the heaters of the various panels, and the fans, and operating the initial clear. When this sequence has been completed, showing that the ENIAC is ready to operate, the GREEN light goes on.

Pushing the stop switch turns the ENIAC off, including the heaters, the d-c power supplies, and the fans.

D-C power supplies clock

This shows the number of hours the d-c power supply filaments have been on.

Initial clear switch

Though the ENIAC is initially cleared whenever the start switch is operated, an initial clear switch is provided so that the operator can clear the machine without turning it off.

The operation selector switch on the cycling unit must be set at Cont. for initial clearing to take place.

Selective clear program controls

C_1 - program pulse input terminal for selective clear program control.

C_o - program pulse output terminal for selective clear program control.

Whenever a program pulse is supplied to a C_1, all accumulators set to SC will be cleared, and a program pulse will be emitted from the corresponding C_o one addition time later. For more helps of associated transceivers see PX-9-305.

Door Switch Shunt

Ordinarily the ENIAC will not operate with any of the doors off. This is a safety feature, since removing the doors exposes dangerous voltages. If it is necessary to operate the ENIAC with the doors off, this may be done by holding this switch closed.

A-C voltage meter

A-C voltage selector switch

By means of this switch and meter the three phases of one of the two bus systems supplying 110 volts a-c to the filament transformers of the various units may be measured.

R_1 - pulse input terminal for reader interlock

R_i - pulse input terminal for reader

R_o - program pulse output terminal for reader

These terminals serve to do with the operation of the IBM card reader. Whenever a pulse is supplied to R_i the IBM reader starts to put a new card in position. After the card is read and the relays have set up the constant transmitter gates the information is ready to be taken from the constant transmitter. A pulse is emitted from R_o after the constant transmitter is ready and after a pulse has been received on R_1. The operation of the constant transmitter program controls is described on PX-11-305.

Reader start switch

R_s - Terminal for paralleling the reader start switch

Operation of the reader start switch starts IBM card readers. After the card has been read a pulse is emitted from R_o.

R_s is a terminal for paralleling the reader start switch with a switch which may be carried anywhere around the ENIAC and which is connected to this terminal via a program line which has no load box, or by means of a special cable.

Initiating pulse switch

I_s - Terminal for paralleling the initiating pulse switch

I_o - Program pulse output terminal for initiating pulse

Whenever the initiating pulse switch is pushed a single program pulse (i.e., a gated OFF) is emitted from I_o. This pulse may be used to initiate any sequence of operations set up on the ENIAC.

I_s is a terminal for paralleling the initiating pulse switch with a switch which may be carried anywhere around the ENIAC and which is connected to this terminal via a program line which has no load box, or by means of a special cable.

Note: Portable Control Station is shown on PX-9-303.

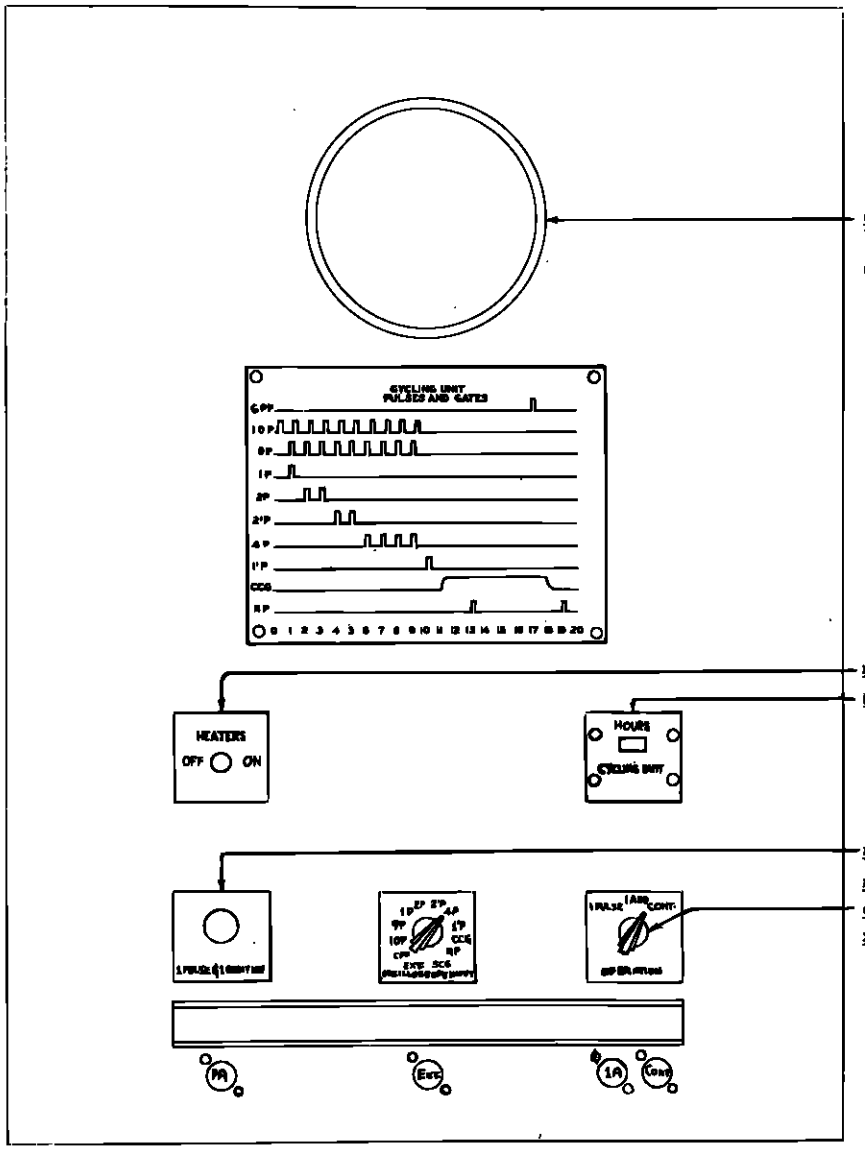
P_i - pulse input terminal for printer

P_o - program pulse output terminal for printer

Whenever a pulse is received on Pi the IBM punch starts to operate and the printer relays start to pick up. A pulse is emitted from P_o as soon as the relays are set up. Any time after this pulse is emitted Pi may again be stimulated, but this will not cause a second punching until the first is finished.

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INITIATING UNIT FRONT PANEL			
MATERIAL	FINISH		SCALE
Drawn by: J.EBERT DEC. 1944	Checked by: AVD 11/1/45	Approved by: 7-16-45	PX-9-302

2 1



Oscilloscope on which can be seen the cycling unit pulses and gates, the selective clear gate (sCG) (when it is programmed), or any external signal transmitted to the terminal marked "Ext.". The cycling unit pulses and gates to be seen are shown on the accompanying chart, behind which are the oscilloscope adjustments. The oscilloscope input switch selects the signal to be shown on the oscilloscope. A signal may be transmitted to the terminal "Ext." on a program line which has no load box.

Heater switch

Heater clock

Push button for 1 pulse time or one addition time

PA= Terminal for paralleling this push button

Operation selector switch

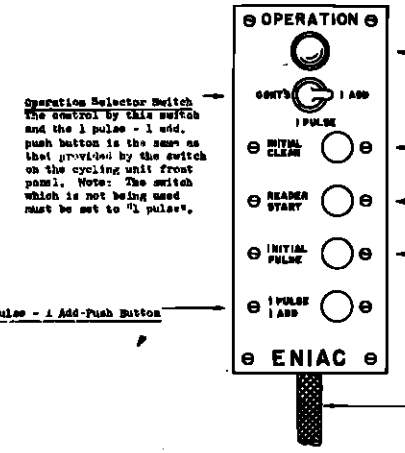
1A and Cont. = Terminals for paralleling the operation selector switch

—The cycling unit has three modes of operation, selected by the switch or its associated terminals (1A, Cont.):

1) Cont. = The pulses and gates are given out continuously.
2) 1 Add. = The pulses and gates for one addition time are emitted whenever the push-button for 1 pulse time or 1 addition time is pushed.
3) 1 Pulse = The pulses and gates for one pulse time are emitted whenever the push-button for 1 pulse time or 1 addition time is pushed.

—Portable push buttons may be used in connection with terminals PA, 1A, and Cont. These may be plugged into a program line which has no load box and that line plugged into the terminals.

1) A push button connected to PA parallels the 1 pulse and 1 Add. push button.
2) Push buttons connected to 1A and Cont. enable the operator to parallel the operation selector switch. When this switch is set to the 1 Pulse position, holding closed the button connected to 1A gives the 1 addition time mode of operation, while holding closed the button connected to Cont. gives continuous operation.



Operation Selector Switch
The control by this switch and the 1 pulse - 1 add. push button is the same as that provided by the switch on the cycling unit front panel. Note: The switch which is not being used must be set to "1 pulse".

Green Pilot Light
Same as on Initiating Unit Front Panel

Push Buttons
Control provided is the same as provided by corresponding push buttons on Initiating Unit Front Panel - See PX-9-302.

1 Pulse - 1 Add-Push Button

Cable

Portable Control Station

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CYCLING UNIT FRONT PANEL		
MATERIAL	FINISH	SCALE
Drawn by: J.R.DELSACK DEC.1944	Checked by:	Approved by:

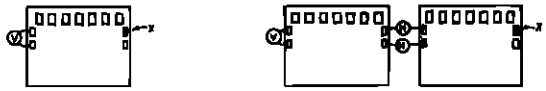
PX-9-303

The digit terminals are to be connected to the digit trunks (trays) (see PX-5-305) by the digit cables for receiving and transmitting numbers. The operation of these terminals is governed by the program controls of the accumulator. (Thus digit pulses transmitted on a trunk to which the α terminal is connected are received only if the accumulator is programmed to receive on α).

Multiplication by powers of ten may be accomplished by means of shifters (PX-4-104) which transpose the digit wires. Shifters must be placed only in digit input terminals, not in digit output terminals.

Deleters (PX-4-109) are used in connection with the significant figures switch; they may be placed only in digit output terminals.

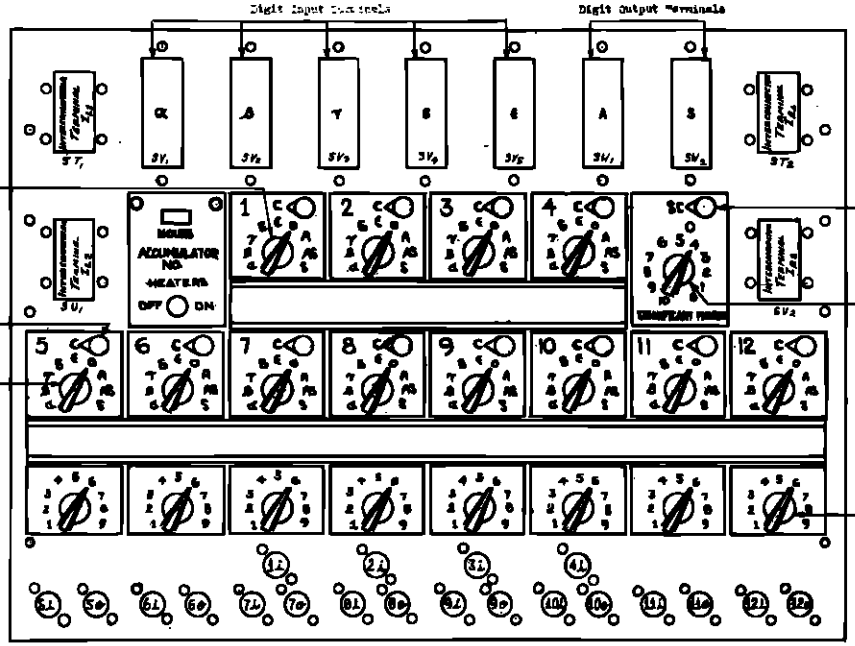
Accumulator Interconnection - Diagram



1p decade accumulator — 20 decade accumulator

V: Acc. interconnector cable (vertical) (PX-5-121)
H: Acc. interconnector cable (horizontal) (PX-5-110)
X indicates position of acc. interconnector terminal load box (PX-5-109)

Note: Each of the 24 program controls of the 20 decade accumulator governs the operation of all decades and of the common programming circuits of both accumulators.



Switches 1-4: Operation switches for non-repeat program controls.

Clear correct switch

Switches 5-12: Operation switches for repeat program controls.

Selective clear switch
If this switch is set to $\Sigma\alpha$ the accumulator is cleared whenever a program pulse is transmitted to one of the selective clear inputs of the initiating unit.

Significant figures switch
This switch determines which decade (if any) is cleared to 5 instead of 0 whenever the accumulator is cleared and on which line the subtract pulse is transmitted on a subtract transmission. It does not govern the deletion of non-significant digits; this must be done by means of deleters (PX-4-109) (When the switch is set to m, deleter number m should be used, etc.)

If the switch is set to m, decade 10-m (counting from the right) is cleared to 5, and the subtract pulse is transmitted on digit line 11-m.

When a 20 decade accumulator is formed, the two significant figure switches are to be used as follows:

(A) When 9 or less significant figures are desired, the left hand switch is set to the number desired and the right hand switch to 10.

(B) When 10 or more significant figures are desired, the left hand switch is set to 10 and the right hand switch set so that the sum of the two switch readings equals the number of significant figures desired.

Repeat switches for repeat program controls 5-12
Each switch governs the number of addition times its repeat program control operates.

Terminals 1i, 2i,..., 4i
Program pulse input terminals for non-repeat program controls 1-4 respectively.

Terminals 5i,.....12i
Program pulse input terminals for repeat program controls 5-12 respectively.

Terminals 5o , 6o 12o
Program pulse output terminals for repeat program controls 5-12 respectively.

Non-repeat program controls 1-4.

These operate for one addition time and emit no program output pulse.
Each control consists of
1) Program pulse input terminal (when stimulated with program pulse causes program control to program operation in accordance with its switch settings)
2) Operation switch
3) Clear-correct switch
4) Associated receiver (for neon bulbs see PX-5-305)

Repeat program controls 5-12.

These operate for n addition times, where n is the setting of the repeat switch.
Each control consists of
1) Program pulse input terminal (when stimulated with program pulse causes program control to program operation in accordance with its switch settings).
2) Program pulse output terminal (emits program pulse at end of nth addition time)
3) Operation switch
4) Clear-correct switch
5) Repeat switch
6) Associated transceiver (for neon bulbs see PX-5-305)

Operation switches and clear-correct switches:
These operate together in the following manner:

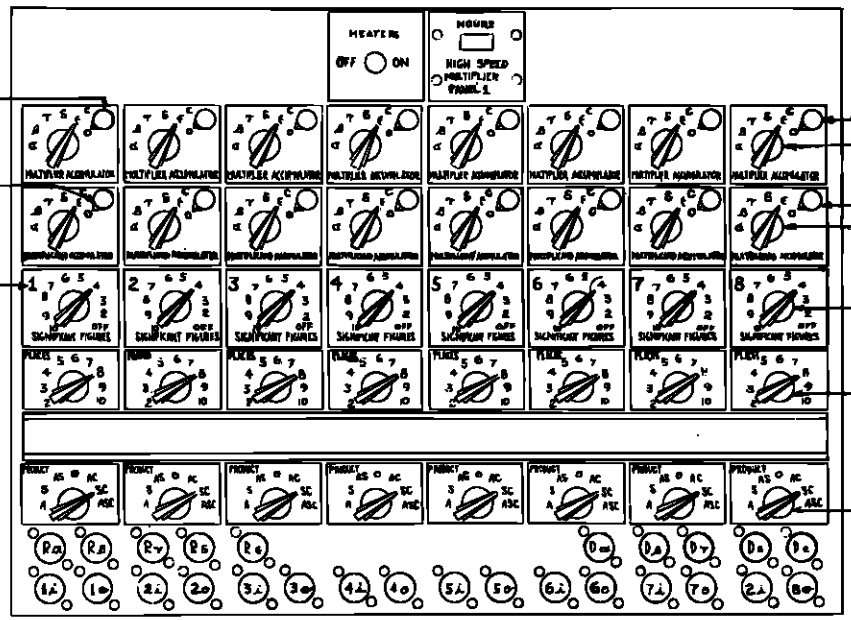
Operation switch setting	Operation programmed by operation switch	Operation programmed by clear-correct switch if set to C.
α	Receive on α digit input terminal	A correct pulse (an internally gated 1' pulse) is placed in the units decade at each addition time.
β	Receive on β digit input terminal	
γ	Receive on γ digit input terminal	
δ	Receive on δ digit input terminal	
ϵ	Receive on ϵ digit input terminal	
0	Nothing	The accumulator is cleared at the end of the last addition time of the program.
A	Transmit on add digit output terminal	
AS	Transmit on both add and subtract digit output terminal	
S	Transmit on subtract digit output terminal	

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ACCUMULATOR FRONT PANEL

MATERIAL	FINISH	SCALE

Drawn by:	Checked by:	Approved by:	
J.EDELSACK DEC. 1944	[illegible] 11/12/45		PX-5-301 Was PX-5-JUA



Multiplier Acc. Clear Switch

Multiplicand Acc. Clear Switch

Number of the program control to which the switches in a given column belong and to which the corresponding numbered program input and program output terminals belong.

Multiplier Accumulator Clear Switch

This governs the clearing of the multiplier acc. by means of the static cable running into the multiplier acc. PM plug-in unit. If this switch is set on C, the multiplier is cleared during the last addition time of the multiplication.

Multiplier Accumulator Receive Switch

Whenever a program pulse is received on a program input terminal of a given program control, a pulse is immediately emitted from Pα - Pε, or not at all, accordingly as the multiplier acc. function switch of that program control is set on α - ε, or C respectively. These pulses may be used to cause the multiplier acc. to receive the multiplier during the next addition time by having them transmitted to properly set multiplier acc. program controls, i.e. by connecting Pα - Pε to five program pulse inputs of the multiplier acc. (#9) and setting the corresponding operation switches to receive on α - ε respectively.

It is to be noted that all 24 multiplier program controls cause pulses to be emitted on Pα - Pε so that only five multiplier acc. program controls are required to receive all 24 multipliers.

Multiplicand Accumulator Clear Switch

This operates the same as the multiplier acc. clear switch except that it governs the clearing of the multiplicand acc.

Multiplicand Accumulator Receive Switch

This functions the same as the multiplier acc. receive switch except that it gives out program pulses on terminals Dα to Dε and may be used with the multiplicand acc. (#10).

Significant Figure Switch

Multiplier Places Switch

Product Disposal Switch

Terminals 1i, 2i, ...24i
Program pulse input terminals for program controls 1-24 respectively.

Terminals 1o, 2o 24o
Program pulse output terminals for program controls 1-24 respectively.

Terminals Pα - Pε
Program pulse output terminals associated respectively with α, β, γ, δ, ε on the 24 multiplier accumulator function switches.

Terminals Dα - Dε
Program pulse output terminals associated respectively with α, β, γ, δ, ε on the 24 multiplicand accumulator function switches.

There are 24 multiplier program controls, each consisting of

1) Program pulse input terminal (when stimulated with program pulse causes program control to program multiplication in accordance with its switch settings).
2) Program pulse output terminal (emits program pulse on completion of multiplication).
3) Multiplier acc. receive switch
4) Multiplier acc. clear switch
5) Multiplicand acc. receive switch
6) Multiplicand acc. clear switch
   — described on this drawing
7) Significant figures switch
8) Places switch
   — described on PX-6-305
9) Product disposal switch — described on PX-6-304
10) Associated transceiver — for neon bulbs see PX-6-309

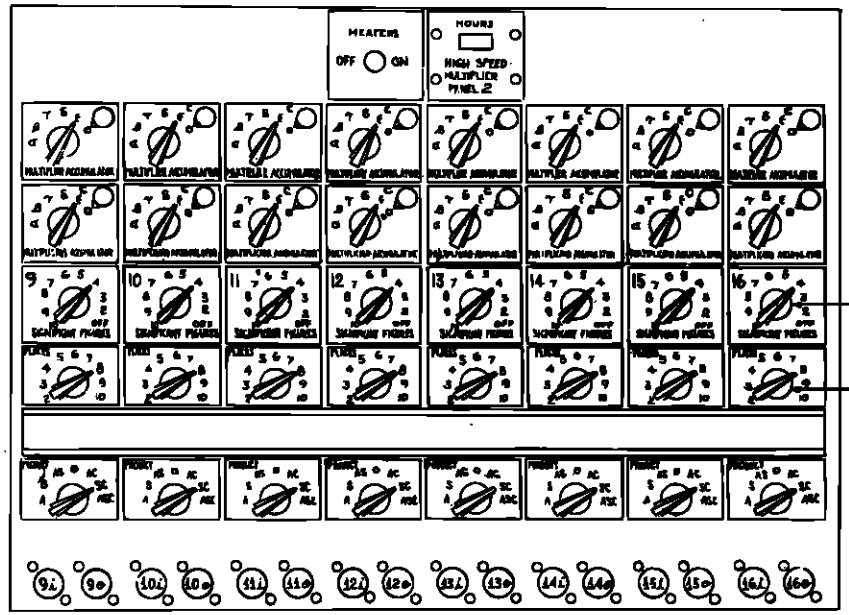
The high-speed multiplier operates in conjunction with four or six associated accumulators. These are the multiplier acc. (#9), the multiplicand acc. (#10), the left-hand partial products acc. (#11 and perhaps #12) and the right-hand products acc. (#13 and perhaps #14). For a diagram showing the interconnections of the high-speed multiplier with its associated accumulators see PX-6-311.

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HIGH-SPEED MULTIPLIER FRONT PANEL NO. 1

MATERIAL	FINISH	SCALE

Drawn by:	Checked by:	Approved by:	
J.ENGELSKA DEC 1944	awb 11/6/45		PX-6-302



Significant Figures Switch

This switch may be used to give a variable round-off; i.e., a product which is rounded off in a different place for each program control. This switch governs the addition of 5 pulses into the proper place of the left-hand product acc. (#11, 12) during the second addition time of the multiplication.

It does not control the deletion of the non-significant digits of the product nor the placing of the subtract pulse in the proper channel of the product on a subtract transmission. Since these vary with the setting of the significant figures switch, they must be taken care of at the accumulator which receives the product. Hence in cases where every product is to be rounded-off to the same number of places, it is best to use the round-off facilities of the right-hand product acc. (#13, 14).

Places Switch

This governs the number of places of the multiplier that are to be used in the multiplication. The multiplier digits are used from left to right, so that the most significant digits are used first. The places referred to are the places of the multiplier acc. counted from the left.

The places switch is completely independent of the significant figures switch. The reason for this is that all digits of the multiplicand are used in the multiplication process. The only purpose of the places switch is to save time.

Time schedule for multiplication

A multiplication requires from 6 to 14 addition times (depending upon the setting of the places switch) including the time required for receiving the multiplier and multiplicand, but not including the time required for disposal of the product.

Addition time [Program input pulse received at end of nth addition time]	Operation
1	Multiplier and multiplicand received
2	Five round-off pulses transmitted to left-hand product acc. (#11, 12)
3	Multiplicand multiplied by first place (10th decade) of multiplier and left and right hand components transmitted to left and right hand product acc.
p+2	This is continued up to the p+2 addition time, where p setting of places switch
p+3	Complement corrections are made when necessary.
p+4	Accumulated left hand products are added into accumulated right hand products.

[Program output pulse and answer disposal pulse emitted at end of p+4th addition time]

MOORE SCHOOL OF ELECTRICAL ENGINEERING UNIVERSITY OF PENNSYLVANIA			
HIGH-SPEED MULTIPLIER FRONT PANEL NO. 2			
MATERIAL	FINISH		SCALE
Drawn by: J.EWELSMEN DEC. 1944	Checked by:	Approved by:	PX-6-303

Important note concerning the partial products digit output terminals

These terminals are to be semi-permanently connected to the α digit input terminals (see note on terminals 1,r) of the product accumulators (#12, 12, 13, 14) by trays or cables not used for any other purpose. No load boxes are to be used. The digit pulses emitted from these terminals are not supplied from transmitters, but from inverter tubes which cannot be connected in parallel with anything else and which have their own resistors. Hence the α digit input terminals of the product accumulators cannot be used for receiving any other numbers.

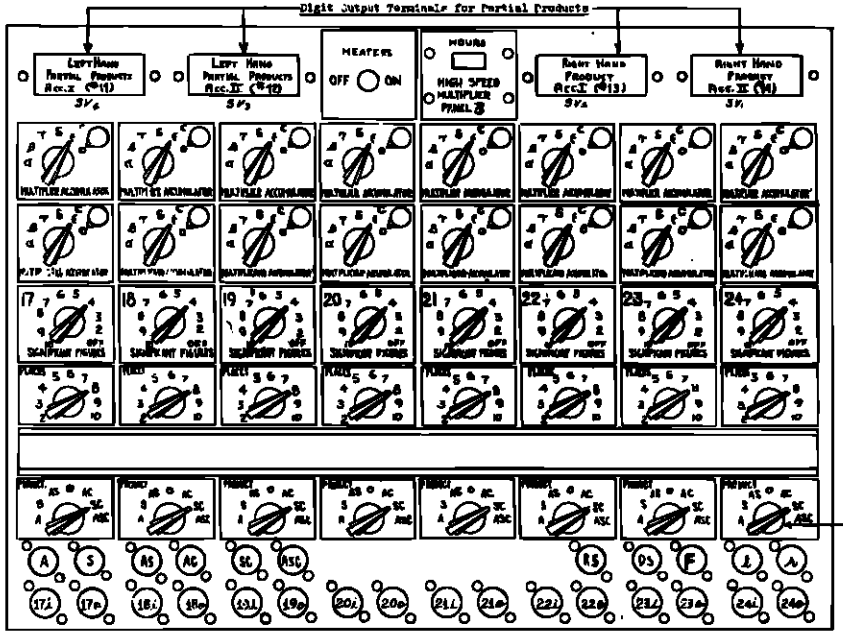
No shifters or deleters are to be used. Accumulators 11 and 12 and accumulators 13 and 14 are paired when more than eight places is desired in the product.

The load on these outputs must be kept as small as possible. Recommended method of connection is:

L.H. #1 By special cable to accumulator 11.
L.H. #2 By short cable to tray (only one tray), and short cable to Accumulator 12.
R.H. # 1 By special cable to Accumulator 13.
R.H. # 2 Similar to L.H. #2 and Accumulator 13.

See also drawing PX-6-311

Digit Output Terminals for Partial Products



Product disposal switch

This switch operates in conjunction with program pulse output terminals A through ASC and provides program facilities for the disposal of all 2^{2n} products using at most 6 program controls of the right-hand product accumulator (#13, 14).

At the end of the $p+4$th addition time (i.e., at the same time as the program output pulse is emitted) a program pulse is emitted from A-ASC according to the setting of the product disposal switch of the program control being used.

Semi-permanent connections may be established by connecting A through ASC to six program pulse inputs of the right-hand product acc. (#13, 14) and setting the corresponding operation switches and clear-correct switches to transmit on A-ASC. The program control output pulse may be used to stimulate that unit of the ENIAC which is to receive the transmitted product.

Terminals A-ASC
Program output terminals associated respectively with A, S, AS, AC, SC, ASC, on product disposal switch.

Terminals RS, RC, F
Program pulse output terminals for transmitting pulses used in the programming of each multiplication:

RS - A program pulse is emitted at the end of the $p+2d$ addition time if the multiplier is negative. Semi-permanent connections must be established so that this pulse programs the multiplicand acc. to transmit subtrant and the right hand product accumulator I(#13) to receive.

RC - A program pulse is emitted at the end of the $p+2d$ addition time if the multiplicand is negative. Semi-permanent connections must be established so that this pulse programs the multiplier acc. (#9) to transmit subtrant and the left hand partial products acc. I (#11) to receive.

F - A program pulse is emitted at the end of the $p+3d$ addition time. Semi-permanent connections must be established so that this pulse programs the left hand partial products accumulator (#11, 12) to transmit add (without shifting) and clear and programs the right hand product accumulator (#13, 14) to receive, or vice-versa.

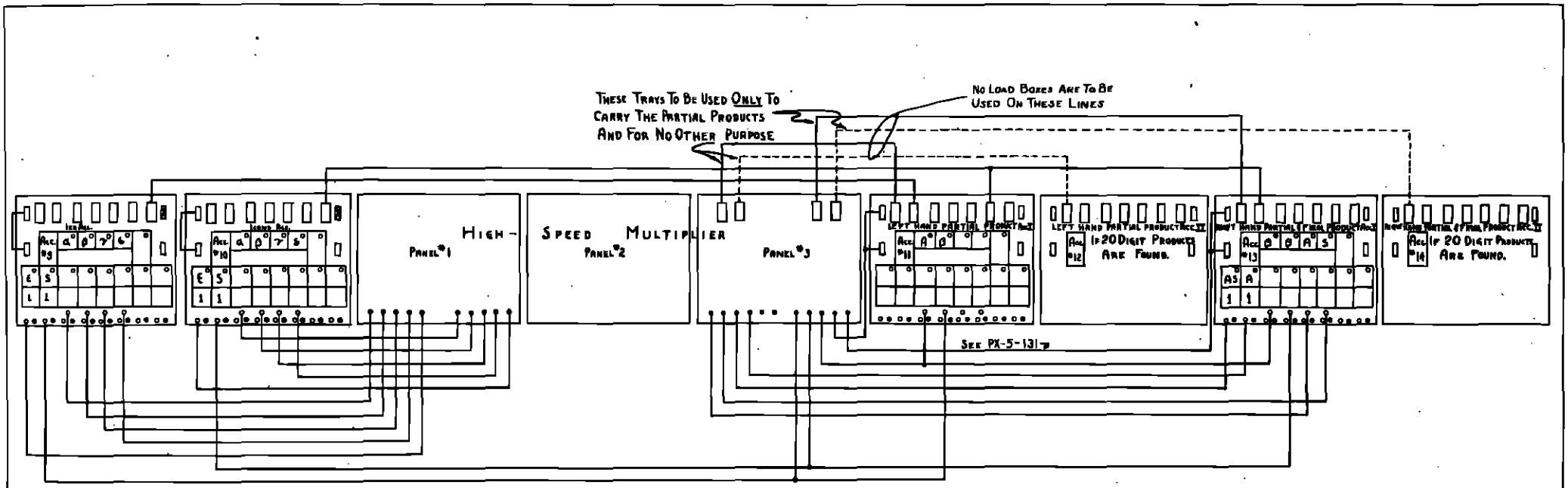
Terminals l,r
Receiver cathode follower buffer output lines. These are to be used to program the product acc. to receive the partial products. The following semi-permanent connections are to be established.

1. l is to be connected via acc. interconnector cable [Alt.] (PX-6-131) into the interconnector terminals 1_{11} and 1_{12} of left-hand partial products acc. I (#11). The α digit input terminal is to be used to receive the partial products.
2. r is to be similarly connected into right-hand product accumulator I (#13). Likewise, the α digit input terminal is to be used to receive the partial products.

MOORE SCHOOL OF ELECTRICAL ENGINEERING UNIVERSITY OF PENNSYLVANIA		
HIGH-SPEED MULTIPLIER FRONT PANEL NO. 3		
MATERIAL	FINISH	SCALE
Drawn by: J.EWELSKK DEC. 1944	Checked by:	Approved by:

PX-6-304

1



Note— Horizontal Lines Above The Units Represent Digit Trays. The Dotted Lines Represent Trays Which Need Be Used Only When 20 Digit Products Are Found.

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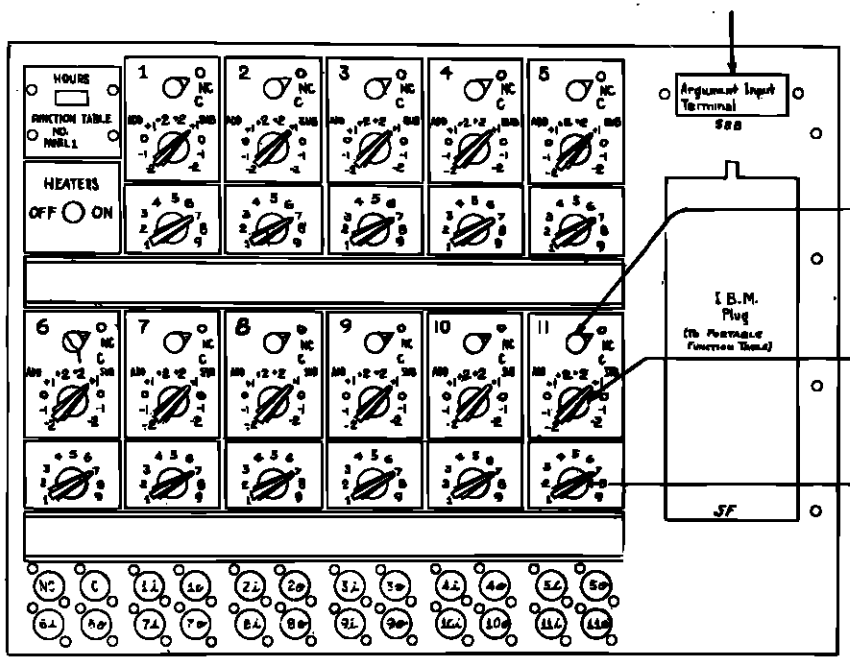
Interconnection Of High-Speed Multiplier With Associated Accumulators ~ PX-6-311

Argument input terminal

This input is open for reception of the two-digit argument during the 2nd addition time of operation. The units place is received on line 1, the tens place on line 2. Shifters (PX-4-104) should be used in this terminal to shift the argument if it comes from other decades than the 5th and 6th. The other lines of this terminal are unconnected, so a delater is not required.

The accumulator which transmits the argument may be programmed from terminals NC and C.

The function table automatically clears its argument at the end of each operation.



There are eleven program controls on each function table. Each program control consists of a program pulse input terminal (which, when stimulated with a program pulse, causes the program control to program the looking up of a function value), a program pulse output terminal (which emits a pulse on completion of the operation), the three switches described below, and an associated transceiver (for neon bulbs see PX-7-305).

Argument reception switch

This switch operates in conjunction with program pulse output terminals NC and C and may be used to program an accumulator or accumulators to transmit the argument.

At the end of the 1st addition time a program pulse is emitted from NC or C if this switch is set on NC or C respectively. Semi-permanent connections may be established by connecting NC and C to program input terminals of the argument accumulator and setting the corresponding operation switches to transmit and transmit-and clear respectively.

Operation switch

This switch determines whether the function value (add) or its complement (subtract) is transmitted.

It also determines whether the function value of the argument received, or the function value of one of the neighboring arguments, is transmitted. Thus positions -2, -1, 0, +1, +2 give f(n-2), f(n-1), f(n), f(n+1), f(n+2) respectively, where n is the argument.

Operation repeat switch

This switch determines the number of times the function value is transmitted.

Note that 4 addition times are required for the function table to set up, receive the argument, etc. This loss of time must be taken account of in programming the accumulator which receives the value of the function. Thus if that accumulator is programmed with the same pulse that programs the function table with its repeat switch set to 9, it could receive the value of the function only 5 times.

Terminals 1i, 2i,.....11i
Program pulse input terminals for program controls 1-11 respectively

Terminals 1o , 2o 11o
Program pulse output terminals for program controls 1-11 respectively

Terminal NC
Program pulse output terminal associated with NC on argument reception switch.

Terminal C
Program pulse output terminal associated with C on argument reception switch.

Time Schedule for Function Table

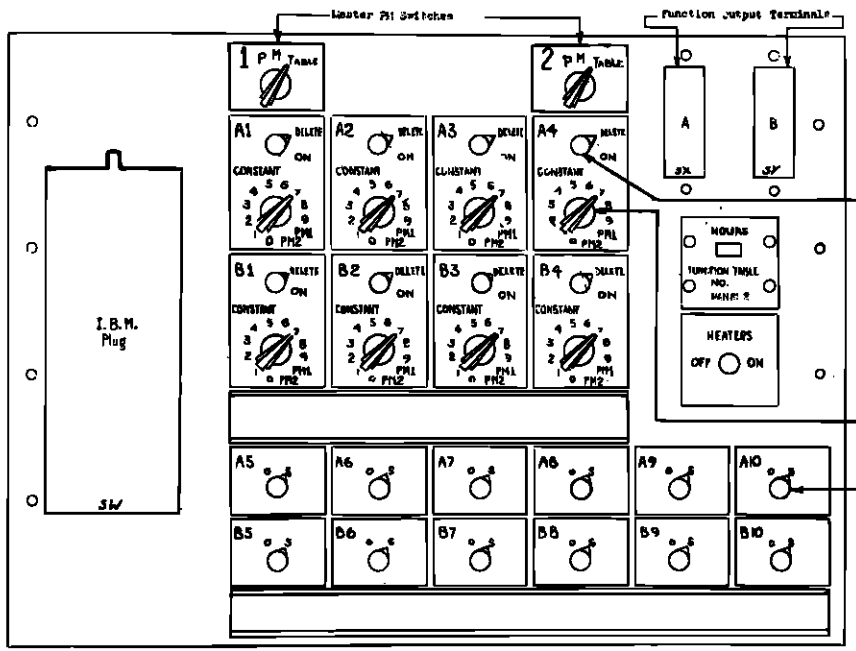
Addition time	Operation
(Program input pulse received at end of 0th addition time)	
1	Circuits set up
2	Argument received
3	Argument modified by the addition of 0 to 4 pulses. At 4th pulse time portable function table starts to set up.
4	Function table finishes setting up
5	Value of function transmitted
r+4	This is continued up to the r+4-th addition time, where r is the setting of the function repeat switch.
(Program output emitted at end of r+4th addition time)	

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FUNCTION TABLE FRONT PANEL NO. 1

Drawn by:	Checked by:	Approved by:	PX-7-302
[illegible] DEC.1944	[illegible] 1/25/45		

1



Sample row of switches on portable function table showing connection to function output terminals.



For a positive number, set PM to P and set the number on the switches.
For a negative number, set PM to M and set the complement of the number with respect to 10^8 on the switches.

Function output terminals

The digit pulses representing the value of the function are transmitted from these terminals. A connection table appears below. These terminals are to be connected to the digit trunks (trays) (see X-7-305) by the digit cables for transmission of the function value to another unit of the ENIAC.

It is to be noted that the division of the eight constant digit switches and the 12 function table entries into the groups A and B was an arbitrary one, and by means of special adapters (PX-4-110) these can be regrouped in any manner.

Table showing connections of function output terminals

Line	Terminal A	Terminal B
12	Ground	Ground
11	PM 1	PM 2
10 (Billions place)	Constant digit switch A^8	Constant digit switch B^8
9	Constant digit switch A^7	Constant digit switch B^7
8	Constant digit switch A^6	Constant digit switch B^6
7	Constant digit switch A1	Constant digit switch B1
6	Subtract pulse switch A10 (Left hand six entries of portable function table add)	Subtract pulse switch B10 (Right hand six entries of portable function table add)
5	Subtract pulse switch A9	Subtract pulse switch B9
4	Subtract pulse switch A8	Subtract pulse switch B8
3 (Hundreds Place)	Subtract pulse switch A7	Subtract pulse switch B7
2 (Tens Place)	Subtract pulse switch A6	Subtract pulse switch B6
1 (Units Place)	Subtract pulse switch A5	Subtract pulse switch B5

Digit delete switch

When the digit delete switch is set to delete the constant digit switch is disconnected from its function output terminal, otherwise it is left connected.

Digits which are constant for all the values of a function may be set up on the constant digit switches.

If these switches are set to PM1 or PM2, the outputs of the corresponding master PM switches are fed through these switches to the output terminals. This feature is used when some of the left hand places of a function with both positive and negative values are zeros; these switches then supply zeros when the transmitted number is positive and nines when the transmitted number is negative, thus avoiding the use of shifters at the receiving terminals.

Constant digit switch

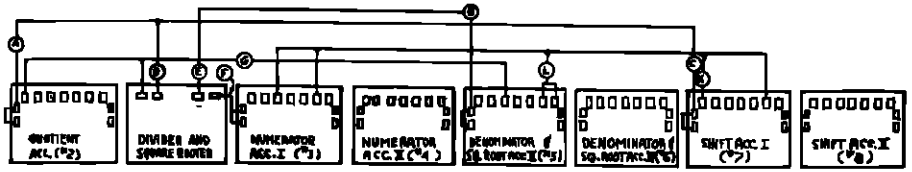
Subtract pulse switch

On a subtract transmit these switches feed a subtract pulse onto their corresponding function output terminal lines if they are set to 5. Thus the switch corresponding to the units digit of the function should be set to 5; the others feeding onto the same digit trunk should be set to 0.

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FUNCTION TABLE FRONT PANEL NO. 2			
MATERIAL	FINISH		SCALE
Drawn by: J.ENSLOW DEC.1944	Checked by: AWG 1/6/45	Approved by:	PX-7-303

1

Diagram Showing Semi-permanent Connections to be Made Between Divider-Square-Rooter and its associated Accumulators



(In dividing the quotient is built up here. This acc. is not used in square-rooting.)

(The numerator or quantity to be square-rooted is to be placed here.)

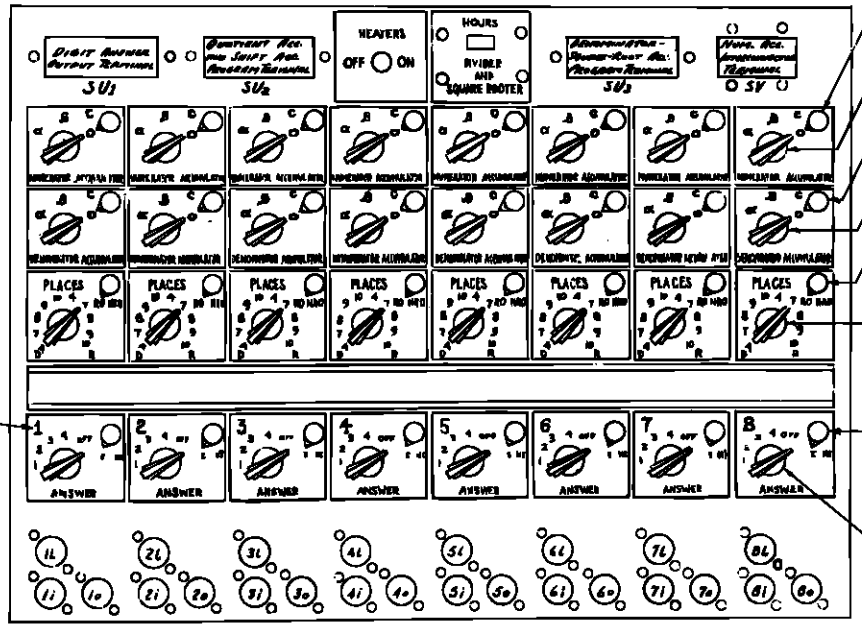
(In dividing the denominator is to be placed here. In square rooting twice the square root is built up here.)

Notes on cables:

No digit tray load box is to be used on any of these connections

(A) Accumulator interconnector cable (quotient) (PX-5-134)
(B) Acc. interconnector cable (denom.&R.) (PX-5-136)
(C) Acc. interconnector cable (shift) (PX-5-135)
(D) Standard digit cable, with adapters (divider) (PX-4-114) plugged into program terminal.
(E) Standard digit cable, with adapters (divider) (PX-4-114) plugged into program terminal.
(F) Acc. interconnector cable (divider) (PX-5-137)
(G) Trunk to transmit digit pulses for quotient and square root.
This trunk is not to be used for any other purpose, since the pulses emitted are not supplied from transmitters but from inverter tubes which cannot be connected in parallel with anything else. These inverters have their own load resistors, so no load box is to be used in connection with them.
(K) Standard digit trunk (with load box) using +1 shifter in α input of the shift accumulator.
(L) Standard digit trunk transfer (with load box).

There are eight divider square rooter program controls, each consisting of a program pulse input terminal (which, when stimulated with a program pulse, causes the program control to program an operation, in accordance with its switch settings), a program pulse output terminal (which emits a program pulse on completion of the operation, including interlocking) the eight switches described below, and an associated transceiver (for neon bulbs see PX-10-302).



Number of the program control to which the switch and pulse terminals in a given column belong.

Terminals 1L, 2L.....8L - Program pulse input terminals for program controls 1-8 respectively. When stimulated with program pulse causes program control to program division or square-root in accordance with its switch settings.

Terminals 1i, 2i.....8i - Interlock pulse input terminal.
If the interlock switch of a given program control is set at N, these terminals are not used.
If the interlock switch is set at I, a pulse must have been received on any interlock terminal since the last non-interlock operation or initial clearing of the divider before a program output pulse is emitted. The interlock pulse may be a program pulse or a digit pulse or pulses.

Terminals 1o, 2o.....8o - Program pulse output terminals for program controls 1-8 respectively. Emits program pulse after both the operation is completed and an interlock pulse is received (if interlock switch is set at I).

Numerator Accumulator Clear Switch
This governs the clearing of the remainder by means of the static cable running into the numerator accumulator PM plug-in unit. If this switch is set on C, the numerator accumulator is cleared of its remainder during the last addition time of the division or square root.

Numerator Accumulator Receive Switch
When semi-permanent connections are made, this switch programs the numerator accumulator to receive on the α and β digit input terminals during the first addition time of the dividing or square-rooting.

Denominator-Square-Root accumulator Clear Switch
This switch operates the same as the numerator accumulator clear switch except that it governs the clearing of the denominator-square-root accumulator.

Denominator-Square-Root Accumulator Receive Switch
When semi-permanent connections are made, this switch programs the denominator and square root accumulator to receive on the α and β digit input terminals during the first addition time of the dividing or square-rooting.

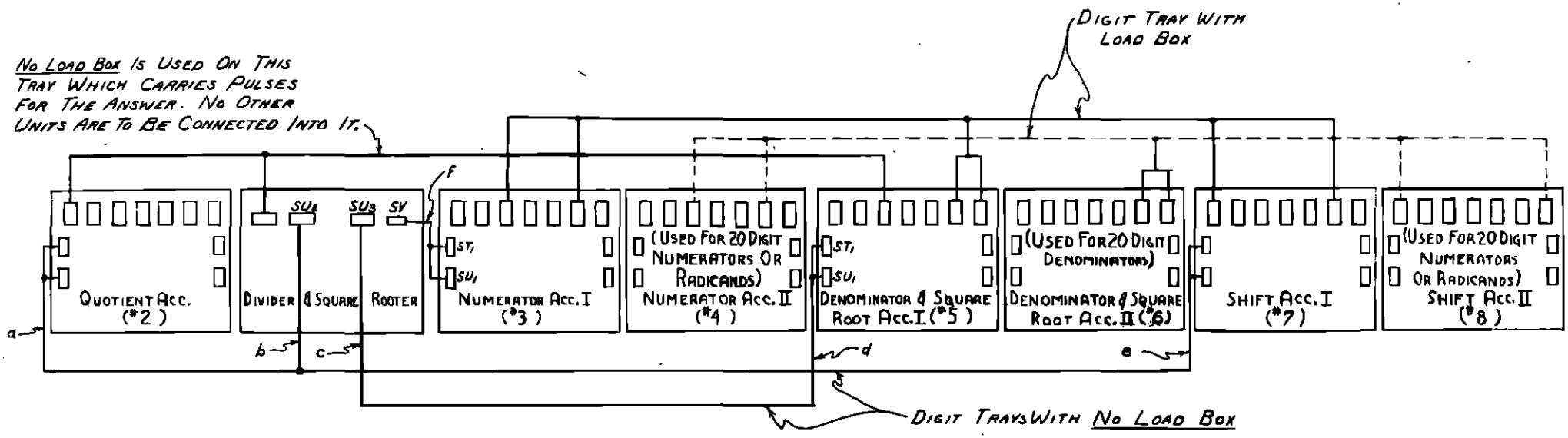
Round-Off Switch
When set to RO this switch causes the answer to be rounded off in the last place.
Note: Even when the number (s) operated on are such as to give an exact answer this switch must be set to RO to give the correct answer.

Divide-Square-Root and Places Switch
This switch selects which process is carried out and the number of places (counting from the 10th decade, i.e. the highest place) of the answer.
Note: The digit answer output terminal is so wired that the answer is built up starting in the 9th decade (counting from the right). For ordinary operation the numerator (or number to be rooted) and denominator should be placed so that there is a 0 in the 10th decade of their accumulators. If the number to be rooted has an odd (even) number of places to the left of the decimal point it should be placed so that the left-hand digit is in an odd (even) numbered decade. Hence the answer will have at least one place less than the setting of the places switch.

Interlock Switch
This switch is used whenever another operation or set of operations is carried on simultaneously with the division or square-rooting.
An average division (in which there is a zero in the 10th decade of the answer accumulator) or square-rooting takes 13p addition times, where p is the setting of the places switch.
If interlocking is used, and the interlock pulse arrives after the operation has been completed, a program output pulse is emitted during the second addition time following.

Answer Disposal Switch
This switch may be used to program transmission of the quotient or twice the square-root during the first addition time following the completion of the operation. The program control output pulse will then be used to stimulate that unit of the ENIAC which is to receive the answer.
Positions 1 and 2 are normally used to govern the quotient accumulator. The operation they perform is determined by adapter (divider) (PX-4-114). Thus if PX-4-114A is used
Disposal 1 - Causes quotient acc. to add transmit.
Disposal 2 - Causes quotient acc. to add transmit and clear.
Similarly, positions 3 and 4 are normally used to govern the denominator-square-root accumulator.

MOORE SCHOOL OF ELECTRICAL ENGINEERING UNIVERSITY OF PENNSYLVANIA			
DIVIDER AND SQUARE ROOTER FRONT PANEL			
MATERIAL	FINISH		SCALE
Drawn by: J. EDELSACK DEC. 1944	Checked by: [illegible] 10/19/45	Approved by:	PX-10-301



Item	Description	Refer To
ST_1, SU_1	Accumulator Interconnector Terminals	PX-5-105
SU_2, SU_3, SV	Divider & Square Rooter Programming Terminals	PX-10-108
a	Special Cable From Digit Tray To ST_1 & SU_1 On Quotient Acc.	PX-5-134
b, c	Adaptors From SU_2 To Digit Tray Or From SU_3 To Digit Tray	PX-4-114A, A & AC Adaptor PX-4-114B, A & S Adaptor PX-4-114C, AC & SC Adaptor
d	Special Cable From Digit Tray To ST_1 & SU_1 On The Denom. & Sq. Root Acc.	PX-5-136
l	Special Cable From Digit Tray To ST_1 & SU_1 On The Shift Acc.	PX-5-135
f	Special Cable From SV To ST_1 & SU_1 On The Numerator Acc.	PX-5-137

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Interconnection Of Divider & Square Rooter With Associated Accumulators ~ PX-10-307

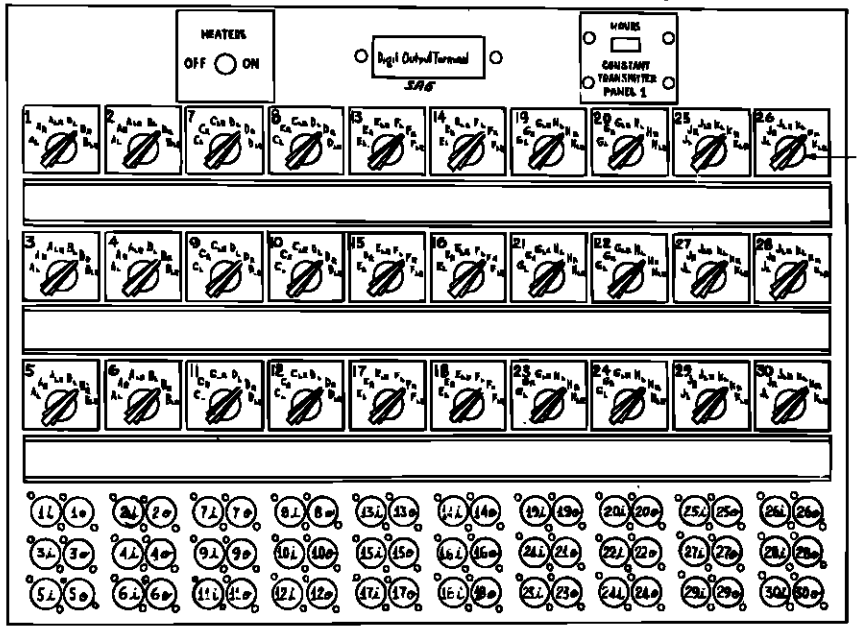
Digit Output Terminal

Whenever the transmission of a constant is programmed digit pulses representing this constant are emitted from this terminal. This terminal is to be connected to a digit trunk (tray) (See PX-11-306) by a digit cable for transmission of the constant to another unit of the ENIAC.

A table showing the connecting of this terminal for left-hand and right-hand five digit groups, and combined left and right-hand ten digit sets, appears below. It should be noted that a left-hand five-digit group would be received in the left-hand half of an accumulator and a right-hand five-digit group would be received in the right-hand half if no shifter were used.

Line	10-digit number (LR)	5-digit left-hand number (L)	5-digit right-hand number (R)
12	Ground	Ground	Ground
11	PM (of L)	PM (of L)	PM (of R)
10	Billions place	Ten-thousandths place	PM' (of R)
9	. . . . .	. . . . .	PM" (of R)
8	. . . . .	. . . . .	PM* (of R)
7	. . . . .	Tens place*	PM' (of R)
6	. . . . .	Units place	PM" (of R)
5	. . . . .	Nothing	Ten-thousandths place
4	. . . . .	Nothing	. . . . .
3	Hundreds place	Nothing	. . . . .
2	Tens place	Nothing	Tens place
1	Units place	Nothing	Units place

*Thus 4 pulses are transmitted on these lines when the constant is positive, 9 pulses when it is a complement. Hence it is unnecessary to use a shifter on a receiving accumulator to receive this constant into the units to ten-thousands decades of that accumulator.



Constant selector switch

Terminals 1i, 2i,..... 30i
Program pulse input terminals for program controls 1-30

Terminals 1 , 2 .....,30
Program pulse output terminals for program controls 1-30

General Explanation of the Constant Transmitter

The constant transmitter has a capacity of 100 digits and 20 signs. These are divided into 10 sets (A,B,.....J, K,) each consisting of 10 digits and 2 signs. Eight of these sets (A,B,....G) are supplied from IBM cards through the IBM reader when proper connections are made on the IBM reader plug board (see PX-11-305). Two of these sets (J,K) are supplied from the constant set switches and PM set switches of panel 2 (see PX-11-303).

Each set may be further divided into two groups, a left-hand group and a right-hand group, each consisting of 5 digits and a sign. This division must remain fixed throughout a given set-up. For example, if the C set is divided into five-digit groups, then any or all of the constant selector switches 7 to 12 may be set to C_L or C_R but not to C_{LR}. Conversely, if the E set is not divided, then any or all of the constant selector switches 13 to 18 may be set to E_{LR} but not to E_L or E_R.

The IBM reader is programmed from the initiating unit (see PX-9-302). The IBM reader controls and plug-board are described on PX-11-305.

Constant Transmitter Program Controls

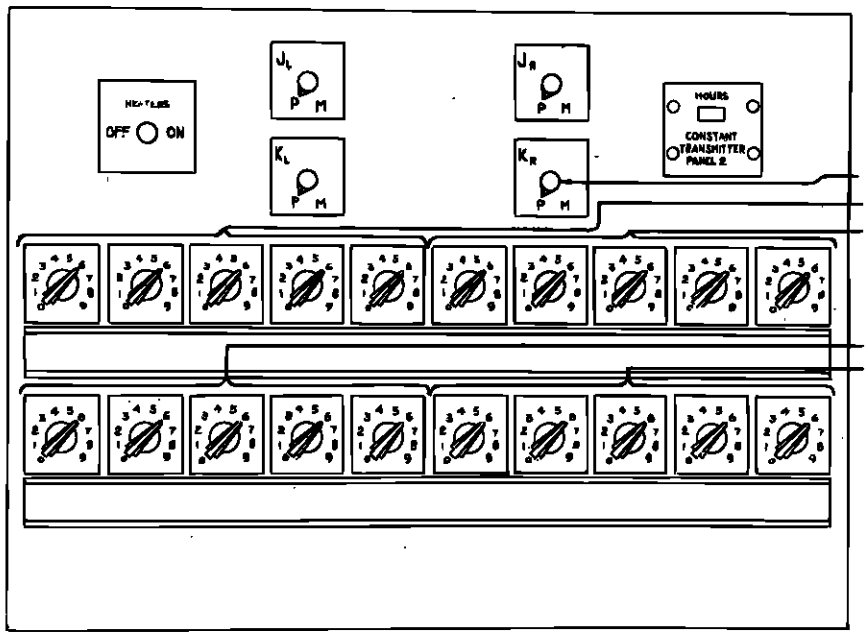
There are 30 constant transmitter program controls, each capable of transmitting certain of the constants over the digit output terminal. Only one program control can be used at a time, hence only one number can be transmitted at a time.

Each program control consists of

1) Program pulse input terminal (when stimulated with program pulse causes program control to program transmission of number set on its constant selector switch)
2) Constant selector switch
3) Program pulse output terminal (emits program pulse after constant has been transmitted, i.e., one addition time after the program pulse input terminal has received a pulse.
4) Associated transceiver (for neon bulbs see PX-11-306)

Program controls 1-24, which transmit constants read from the IBM cards, cannot be used during the operation of the card reader, except during the first 50 addition times of this operation. That is, after a pulse is supplied to R1 on the initiating unit (front panel (see PX-9-302), these controls may be used during the 50 subsequent addition times, but not thereafter until a pulse is emitted from R0.

MOORE SCHOOL OF ELECTRICAL ENGINEERING UNIVERSITY OF PENNSYLVANIA			
CONSTANT TRANSMITTER FRONT PANEL NO.1			
MATERIAL	FINISH		SCALE
Drawn By: J.EDELSACK DEC.1944	Checked By: J.W.M. 9/1/45	Approved By:	PX-11-302
1			

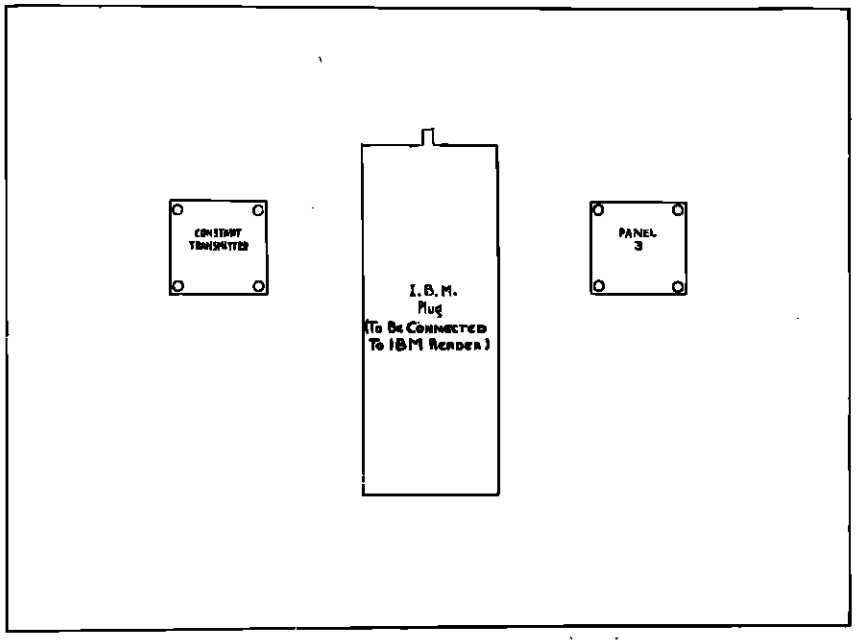


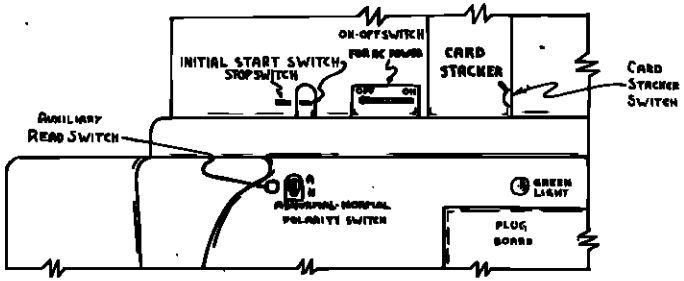
For a positive number, set the PM to P and set the number on the switches.
For a negative number, set the PM to M and set the complement of each digit with respect to 9 on all but units switch where the complement with respect to 10 is set.
For a two-digit number, both PM switches should be set to the sign of the number.

MOORE SCHOOL OF ELECTRICAL ENGINEERING UNIVERSITY OF PENNSYLVANIA		
CONSTANT TRANSMITTER FRONT PANEL NO. 2		
MATERIAL	FINISH	SCALE
Drawn by: J.EDELSACK DEC.1944	Checked by:	Approved by:

1

PX-11-303





Note: Do not change polarity switch while motor-generator is on.

MOORE SCHOOL OF ELECTRICAL ENGINEERING UNIVERSITY OF PENNSYLVANIA		
CONSTANT TRANSMITTER FRONT PANEL NO.3		
MATERIAL	FINISH	SCALE
Drawn by: J.ENGELSACK DEC.1944	Checked by:	Approved by:

PX-11-304

The Polarity Switch

Located on the front of the IBM Reader is a double pole double throw switch which changes the polarity on the holding coils of the relays which control the group selection and the reset control. By plugging this switch one can either wire these circuits on the plug board in the manner indicated there or in the reverse manner. This gives the following types of control:

(A) With the polarity switch in normal position.
The common terminal "C" is then wired to some hub of the #1 reading brushes and the group selection hubs are wired to hubs of the digit selector. Thus, all controlling is done by various punches in one column. The variety of things controled is given by plugging to different digits (12, 11, 0,.....,9) of the digit selector.

(B) With the polarity switch in abnormal position.
In this case "C" is wired to some digit on the digit selector and the group selection hubs are wired to various columns. Here, all the control is obtained by a certain punch (for example, a 12 punch) with different things being controlled by plugging to different columns.

Plugging Illustrations

(a) This shows the common hub "C" wired to column 21. The two hubs above and below C are connected so the wire could have gone to either of them. Note that besides the wire (a) one could connect this upper hub for C to some other column, say 2, getting an "or" control. That is, if a certain number (12, 11, 0,.....,9) is punched in column 21 or column 2 then whatever hub under group selection was plugged to that number of the digit selector causes the corresponding group selection relays to operate.

(b) This wire causes the reset control to operate whenever there is a 12 punch in column 21; that is, a card with such a punch is called a master card.

(c and d) These leads cause information in storage relay groups 6 and 7 to be held as long as cards come through without a 12 punch in column 21. Whenever a card with a 12 punch in column 21 (a master card) comes along the information in groups 6 and 7 will be dropped and new information will be put in from this master card. Immediately, the reader will go on to read the next card.

(e) If a card has a 6 punched in column 21 this lead causes group selection relays for group 12 to be activated giving a circuit from 0 through B instead of A.

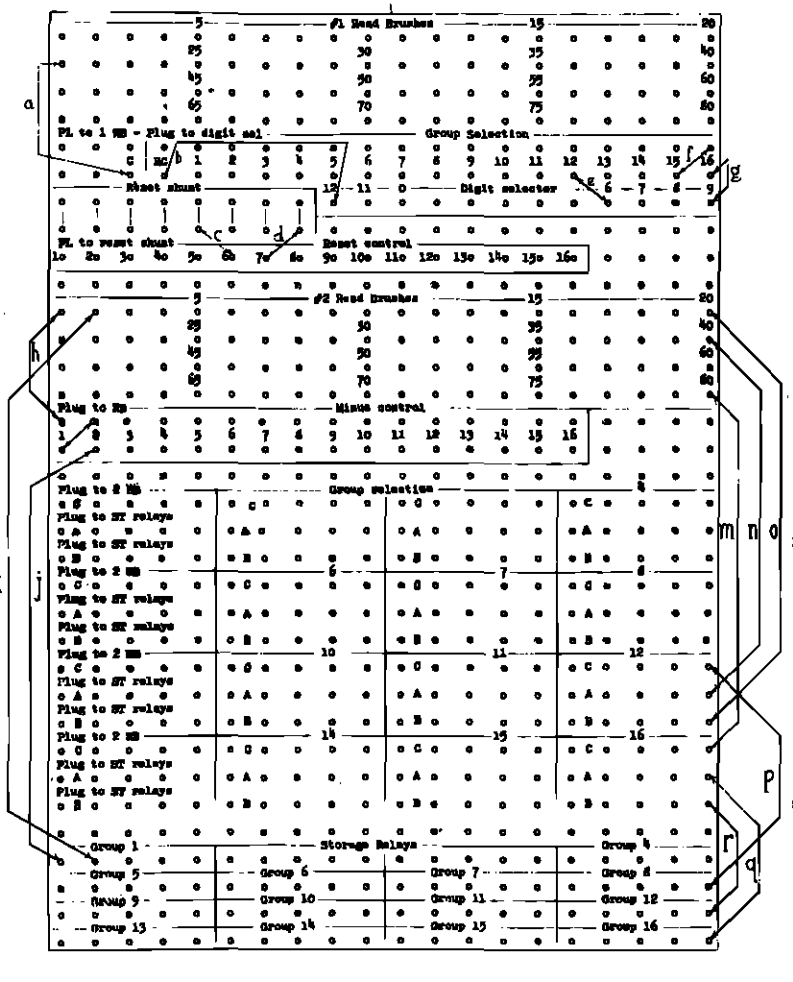
(f and g) If a 9 is punched in column 21 groups 15 and 16 group selection relays will be activated. Diagonal leads such as (f) enable one to operate as many groups as desired from just one punch.

(h, j, and k) This shows the plugging to handle ten digit negative numbers. The PM punch is in column 1 and, by the diagonal connection in the minus control, the PM relays for groups 1 and 2 are operated by this one punch. The first digit reaches the storage relays through (j). (k) illustrates the plugging for the rest of the digits.

(n, o, and p) If there is a 6 punch in column 21 the digit from column 20 will go to the fifth digit of group 8. Otherwise, the digit from column 40 will go there.

(m, q, and r) If there is a 9 punch in column 21 the digit in column 60 will be the fifth digit of group 12. Otherwise, it will be the fifth digit of group 16.

NOTE: If during the course of a computation the IBM reader should run out of cards the starting relay [see PX-11-307] will be closed so the moment new cards are dropped in, the reader will go through a cycle. To make sure that the reader does not fail to read this first card the stop button should be held down until the cards are firmly in place.



#1 Read Brushes

The #1 Read Brushes read the card before the #2 Read Brushes do. The #1 brushes are used for control purposes and the #2 brushes for reading the numbers and their PM's.

Group Selection

The hubs numbered from one to sixteen control the group selection relays whose terminals are located on the lower half of the plug board. These are double hubs, that is, the hub above and below the number are common. The single hub located to the left of these and labeled RC controls the reset control. The features of group selection and reset control are described below. For details see the IBM reader wiring diagram PX-11-119.

Reset Control and Reset Shunt

Certain groups of relays (depending upon plug board arrangements) may be caused to hold their information while a sequence of "detail" cards are read. This is accomplished by connecting the corresponding terminals under Reset Control to any of the Reset Shunt terminals. To change the information which is being held in these relays a "master" card is inserted in the sequence of cards. A particular punch on this master card can cause the hold information to drop out and as the master card passes the #2 Reading Brushes new information can be stored in these relays until the next master card comes along. Whenever such a master card is read the Reader will immediately read the next detail card before it gives out a computing signal to the ENIAC.

WARNING: The detail cards either must not contain information in the fields corresponding to the relays that are holding master card information or else group selection must be used to prevent such information from disturbing the hold relays.

Group Selection Relays

There are sixteen five pole double throw relay switches, called the group selection relays. The common terminals are labeled "C" and normally the circuit is through the terminals labeled "A". When activated (picked up) the circuit is through "B". These circuits are isolated (internally) from the other circuits of the reader so there are many other possible plugging arrangements other than those indicated on the plug board.

Minus Control

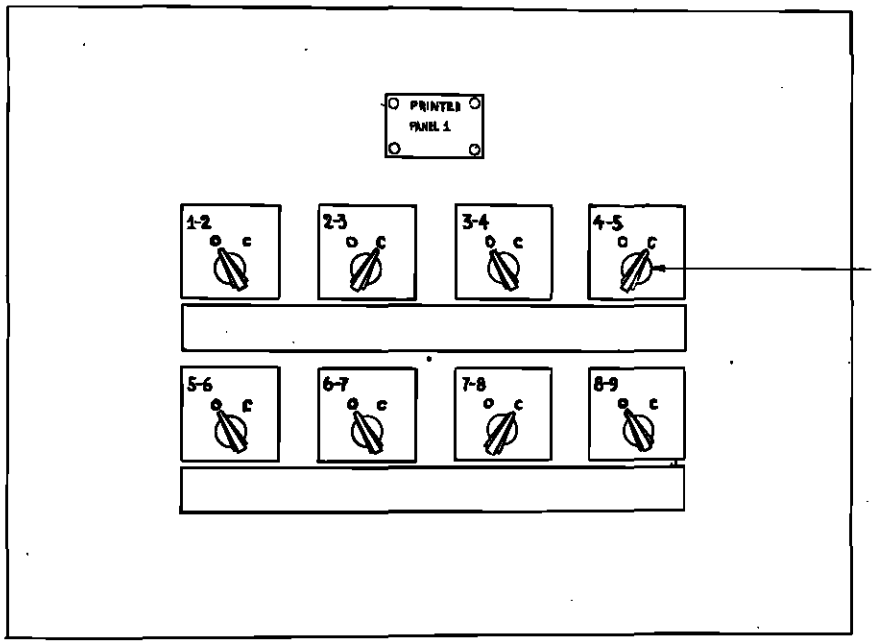
By means of cams in the Reader these terminals connect to the PM relays of the Constant Transmitter only when the IBM card is in positions 11 and 12, that is, when the PM punches would be under the #2 Read Brushes. The two hubs, above and below the group number, are common. Usually, the punch for minus indication will occur in the same column that a digit punch appears. Thus, the same reading brush will indicate the PM of the number and later as the positions zero to nine pass under the brush indicate the digit punched. Other cams (called coding cams) energize the numerical circuits only during the zero to nine part of the cycle enabling the digit punch in that column to cause the proper relays to be set up in the Constant Transmitter. The coding cams consist of two groups, one group is used for positive numbers and the other group causes complements (with respect to $10^{n}-1$) to be set up by storage relays. The PM relays determine which set of coding cams are used.

Storage Relays

The storage relays are located in the Constant Transmitter There are essentially four relays associated with each digit. That is, four relays representing respectively 1, 2, 2^2, and 2^3 can, in various combinations, represent any digit from zero to nine. These four relays are indirectly (through vacuum tube circuits) associated with the 1, 2, 2^2, and 2^3 pulses sent out by the cycling unit. That is, each relay opens a gate tube which through an inverter opens a second gate tube. This second gate tube passes the 1, 2, 2^2, or 2^3 pulses.

For positive numbers the hubs of the #2 reading brushes can be wired directly to the hubs of the storage relays in any order whatsoever. Negative numbers must be handled in groups which are multiples of five. To indicate the negative number there will be an 11 or 12 punch in some column. The wire from the hub representing this column must go to the minus control hubs of all the storage relay groups used for this negative number. There must also be a connection to the hub corresponding to this digit in the storage relays. See the examples shown to the left.

MOORE SCHOOL OF ELECTRICAL ENGINEERING UNIVERSITY OF PENNSYLVANIA			
I. B. M. READER PLUG BOARD			
MATERIAL	FINISH		SCALE
—	—		—
Drawn by: J. Cummings Aug 4, 1945	Checked by: D. Eckert 12-7-45	Approved by:	PX-11-305



Coupling Switch

This switch couples two groups of digits together when it is set to the C position. It provides for the carryover when an ENIAC complement is converted to a true value.
The switches on this drawing and PX-12-303 are set for the arrangement shown in the table below.

Table Showing Original Set of Decades Connected to the Printer

Printer Group	Decades from
1	Master Programmer, Panel 1, Decades 14-16
2	Accumulator 13, Decades 6-10
3	Accumulator 13, Decades 1-5
4	Accumulator 14, Decades 6-10
5	Accumulator 14, Decades 1-5
6	Accumulator 15, Decades 6-10
7	Accumulator 15, Decades 6-10
8	Accumulator 16, Decades 1-5
9	Accumulator 17, Decades 6-10
10	Accumulator 17, Decades 1-5
11	Accumulator 18, Decades 6-10
12	Accumulator 18, Decades 1-5
13	Accumulator 19, Decades 6-10
14	Accumulator 19, Decades 1-5
15	Accumulator 20, Decades 6-10
16	Accumulator 20, Decades 1-5

MOORE SCHOOL OF ELECTRICAL ENGINEERING UNIVERSITY OF PENNSYLVANIA			
PRINTER FRONT PANEL NO. 1			
MATERIAL	FINISH		
Drawn by: J. EDELSACK DEC. 1944	Checked by: A.W.B. 6/5/45	Approved by:	PX-12-301

General Explanation of Printer

The printer operates from the static outputs of accumulator and master programmer decades. The cables connecting the decade static terminals to the printer lie in a trough at the top of the front of the machine. A table, showing the original set of connections, appears on PX-12-301. Every accumulator decade and PM unit and every master programmer decade has a static output terminal.

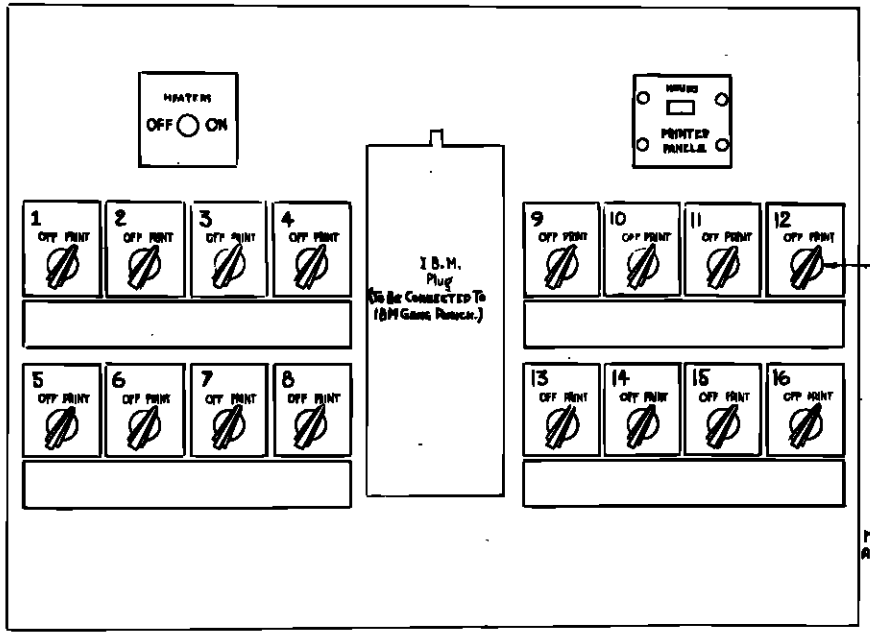
The numbers to be printed are divided into sixteen groups of 5 digits and a PM, numbered from 1 to 16. The printing switches determine which groups are connected to the IBM gang punch. Drawing PX-12-305 shows the IBM gang punch plug board and gives instructions for connecting it up.

Any group of five digits and a PM may be connected to an adjacent group by means of the coupling switch, so that 10 digit, 15 digit, etc. numbers may be punched.

When the numbers to be printed is a complement (i.e., the PM counter registers 9), the true value of the number is punched along with an 11 punch to indicate that it is negative.

Whenever information in the master programmer is printed adaptor PX-12-114 B must be used at the printer plugs on panel 2 so as to ground the unread PM lead going into the printer.

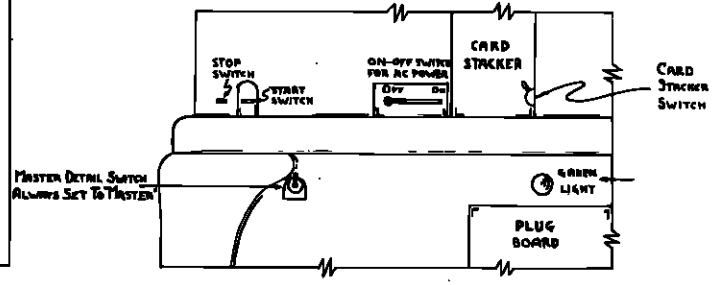
The printer is programmed from the initiating unit [see PX-9-302]. Controls on the IBM gang punch are explained on PX-12-305.



Printing switch.

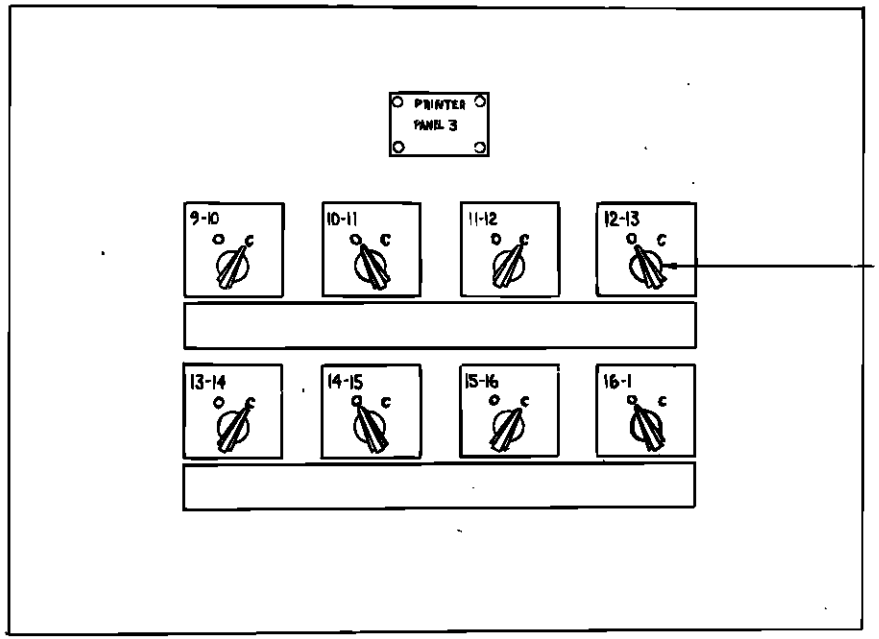
This switch connects (in the "print" position) or disconnects (in the "off" position) the voltage supply to the buffer tubes of its group, so that these tubes do (or do not) operate the relays when the printer is programmed. For the group of digits to be punched it is necessary not only that this switch be set to "print" but also that proper connections be made on the IBM gang punch plug board [see PX-12-305].

This switch must be turned off if the decades to which the group is connected are not turned on.



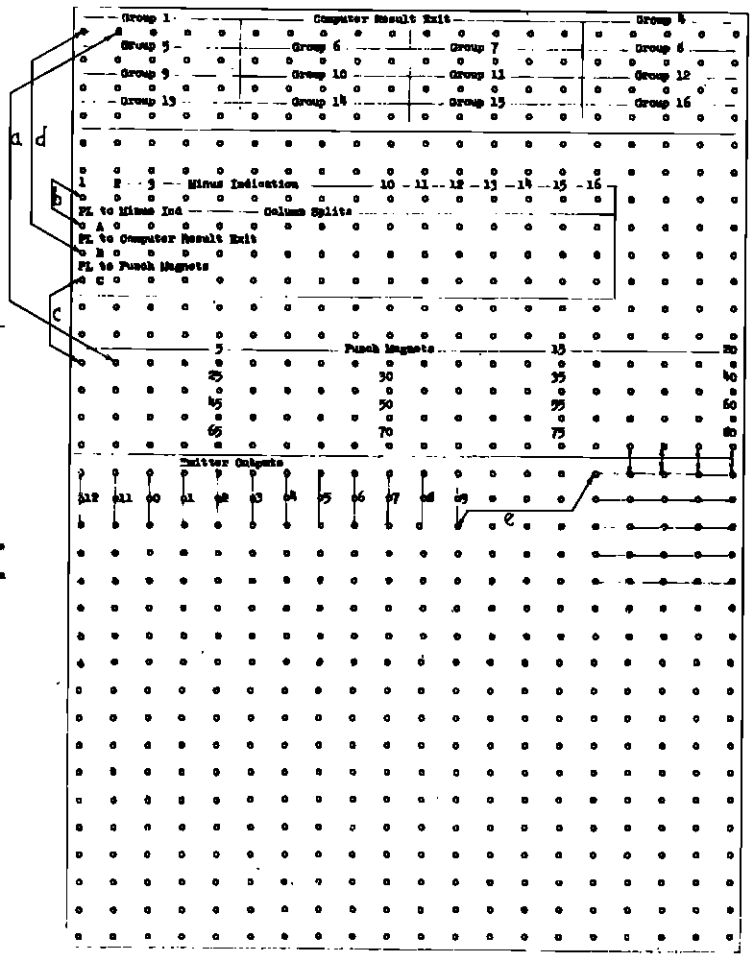
MOORE SCHOOL OF ELECTRICAL ENGINEERING UNIVERSITY OF PENNSYLVANIA			
PRINTER FRONT PANEL NO. 2			
MATERIAL	FINISH		SCALE
Drawn by: J. EDELSACK DEC. 1944	Checked by:	Approved by:	PX-12-302

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MOORE SCHOOL OF ELECTRICAL ENGINEERING UNIVERSITY OF PENNSYLVANIA			
PRINTER FRONT PANEL NO. 3			
MATERIAL	FINISH		
Drawn by: J. EDELSACK DEC. 1944	Checked by:	Approved by:	PX-12-303

PLUG BOARD FOR GANG PUNCH



Computer Result Exit

These hubs connect directly to the digit relays in the printer. To punch positive numbers they can be plugged to the punch magnet hubs in any desired arrangement. Thus, it is possible to place the digits coming from the group 1 relays in any five of the eighty columns on the IBM card.

Minus Indication.

The sixteen hubs under minus indication go directly to the PM relays of the sixteen groups. The minus indication of any group could be punched in any of eighty columns on the card simply by connecting the corresponding minus indication hub with the particular column hub of the punch magnets.

Usually, however, the minus indication will appear above some digit of the number on the card. To place the minus indication (an 11 punch) above the first digit of the number the minus indication of the corresponding group is plugged to one of the terminals labeled "A" under column splits. The hubs "B" and "C" directly under the A-hub used are to be plugged, respectively, to the digit hub (Computer Results Exit) above which the minus punch is desired and to the corresponding hub of the punch magnets.

The column splits is simply a sixteen pole double throw relay switch. This switch is controlled by a cam in the IBM punch which causes the "C" hubs to be connected to the respective "A" hubs during the 11 position of the card and to the "B" hubs during the 0,.....,9 position of the card.

Emitter Outputs

If one of these hubs is plugged to a punch magnet hub the corresponding number will be punched in that column of the card. The five rows of five common hubs to the right of the emitter outputs enable one to punch the same number in more than three columns. The connection labeled (e) on the diagram causes nines to be punched in the columns 77,.....80 on the card. Connections such as these cause the corresponding number to be punched in every card. This can be used to give identifying numbers to the cards or to punch dates on the cards. Alphabetic punching cannot be done on this machine.

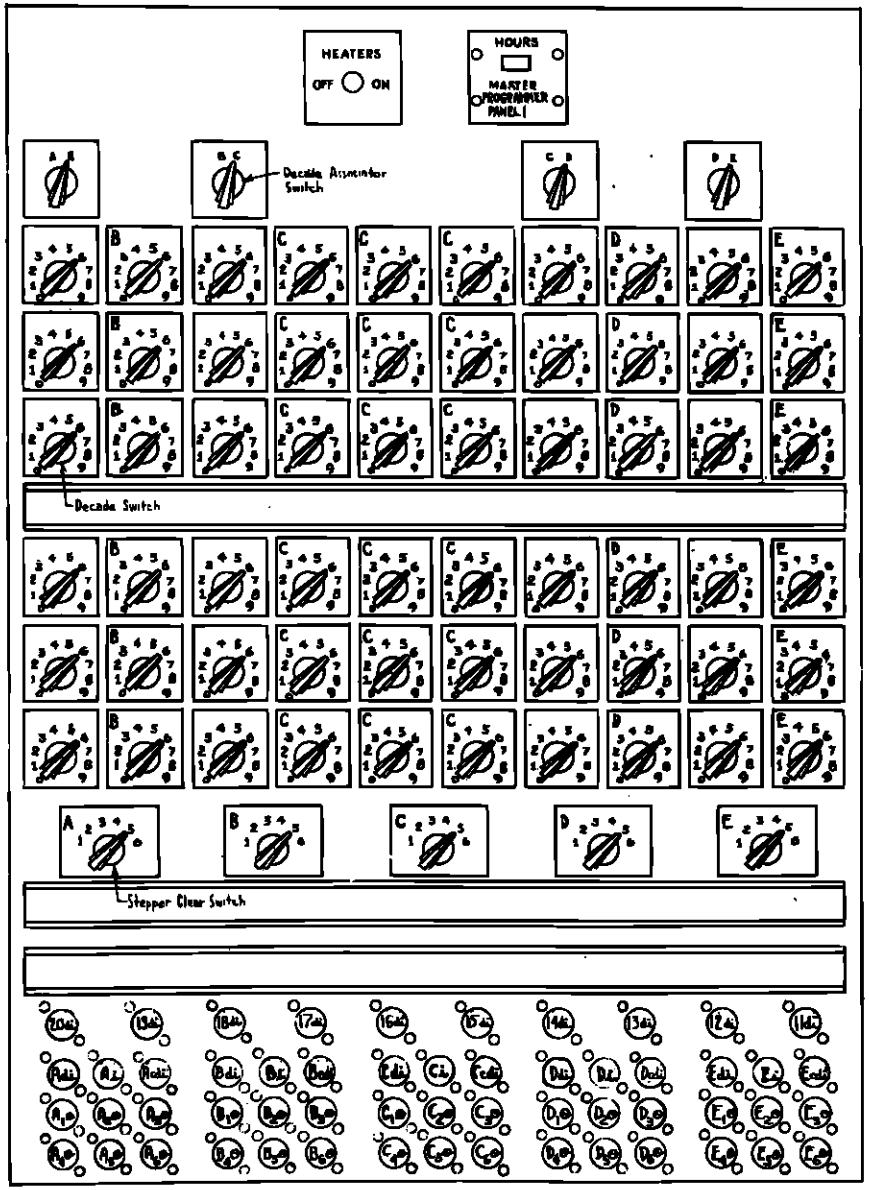
Plugging Illustrations

(a) This illustrates the type of plugging in columns where no minus indication is desired.

(b, c, and d) When the 11 position of the card is under the punches there is a connection through leads (c) and (d) from the punch magnet hub to the minus indication. If the group 1 PM relays were activated a signal will arrive at this time causing the 11 to be punched in column 1 on the card. If the 11 punch indicating a negative number were desired in column 2 leads (a) and (c) must be interchanged at the punch magnet hubs and leads (a) and (d) interchanged at the computer exit hubs. Then the first column of the computer exit comes directly to the first column punch and the second column leads go through the minus indication hubs and the column split.

(e) These connections will cause nines to be punched in the last four columns on the card.

MOORE SCHOOL OF ELECTRICAL ENGINEERING UNIVERSITY OF PENNSYLVANIA			
I.B.M. GANG PUNCH PLUG BOARD			
MATERIAL	FINISH		SCALE
—	—		—
Drawn by: J. Chu 12-7-45	Engineer by: [illegible] 12-7-45	Approved by:	PX-12-305



Stepper terminals

A_1.....K_1	Stepper program pulse input terminals
$A_1 0$.....$A_6 0$;..$K_1 0$....$K_6 0$	Stepper program pulse output terminals
Adi.....Kdi	Stepper direct input terminals
Acdi.....Kcdi	Stepper clear direct input terminals

Decade terminals

Dd120,....Ddil	Decade direct input terminals

General Explanation of Steppers and Decades

A stepper is a six stage ring counter. It has the following associated with it:

1) Stepper program pulse input terminal
2) Six stepper program pulse output terminals, one associated with each stage of the stepper.
3) A group of decades (of from 0 to 5, depending upon the stepper and the settings of the decade associator switches. The n ($n=0,\ldots,5$) decades of each group are interconnected by a direct carry-over circuit (there is no delayed carry-over circuit) enabling them to count (not accumulate) $10^n - 1$ pulses.
4) Stepper clear switch
5) Stepper direct input terminal
6) Stepper clear direct input terminal
7) Each decade has a direct input terminal

The operation of a stepper and its associated equipment is as follows:

At the end of the initial clear each stepper is left on the 1st stage and each decade is cleared to 0.

Suppose a program pulse is received on a stepper program pulse input terminal. One addition time later a program pulse is emitted from the program pulse output terminal corresponding to the stage the stepper is on at the time it is emitted and a program pulse is sent to the units decade of the group of associated decades.

Whenever a group of decades counts to the number set on those decade switches corresponding to the position of the stepper, one addition time later these decades are cleared to zero and the stepper is either stepped to the next position, or (if it is on the position set on its stepper clear switch) cleared to the first position. Though the decades will count either program pulses or digit pulses, any pulse which might cause this clearing and stepping action must be a program pulse.

The decades count both the pulses supplied to the associated stepper's program pulse input terminal (with a one addition time delay) and those supplied to the decade direct input terminals. No set-up is permissible which might lead to pulses being supplied to a decade from both sources simultaneously, or from a decade direct input terminal and a carry-over from a previous decade simultaneously.

An example illustrating a common application of a stepper in programming will show how items 1 through 4 operate together. Consider stepper D, and suppose that decades 12 and 13 are associated with it and that its stepper clear switch is set to 4. Then four two-digit numbers ($n_1,\ldots,n_4$) may be set up on the decade switches, each number associated with the corresponding stage (1,.....4) of the stepper and hence with the corresponding program pulse output terminals ($D_1 0,\ldots,D_6 0$). Whenever a program pulse is received on D_1 a pulse is emitted from one of the output terminals (one addition time later). The first n_1 pulses received on D_1 are emitted from $D_1 0$; the next n_2 pulses received on D_1 are emitted from $D_2 0$... ..., the last n_4 pulses received on D_1 are emitted from $D_4 0$, and the stepper and its associated decades are then left in their original state, ready to repeat the process. The time schedule of these operations is as follows:

Program Pulse	Operation
0	Input program pulse (to Di)
1	Output program pulse emitted (from $D_1 0,\ldots D_6 0$) Decade stepped to next stage
2	In case the decades register the number set up on the decade switches, all decades (associated with stepper D) are cleared to zero and the stepper (D) is stepped to the next stage or (if it is on the position 4) it is cleared to the first stage.

To disassociate a decade from its stepper pull out gate tube 63 in the stepper plug-in unit. See block diagram PX-8-304.

Terminals Ai, Bi.....Ki — Stepper program pulse input terminals

Terminals $A_1 0$.....$K_1 0$ — Stepper program pulse output terminals associated with Stage 1

$A_2 0$.....$K_2 0$ — Stage 2.....

$A_6 0$.....$K_6 0$ — Stage 6

One addition time after a program pulse is supplied to an input terminal (such as Di) a program pulse is emitted from the output terminal corresponding to the stage the stepper is on at the time it is emitted (thus if the stepper is at position 4, when the pulse is emitted it comes from $D_4 0$), and a unit is added to the contents of the associated decades.

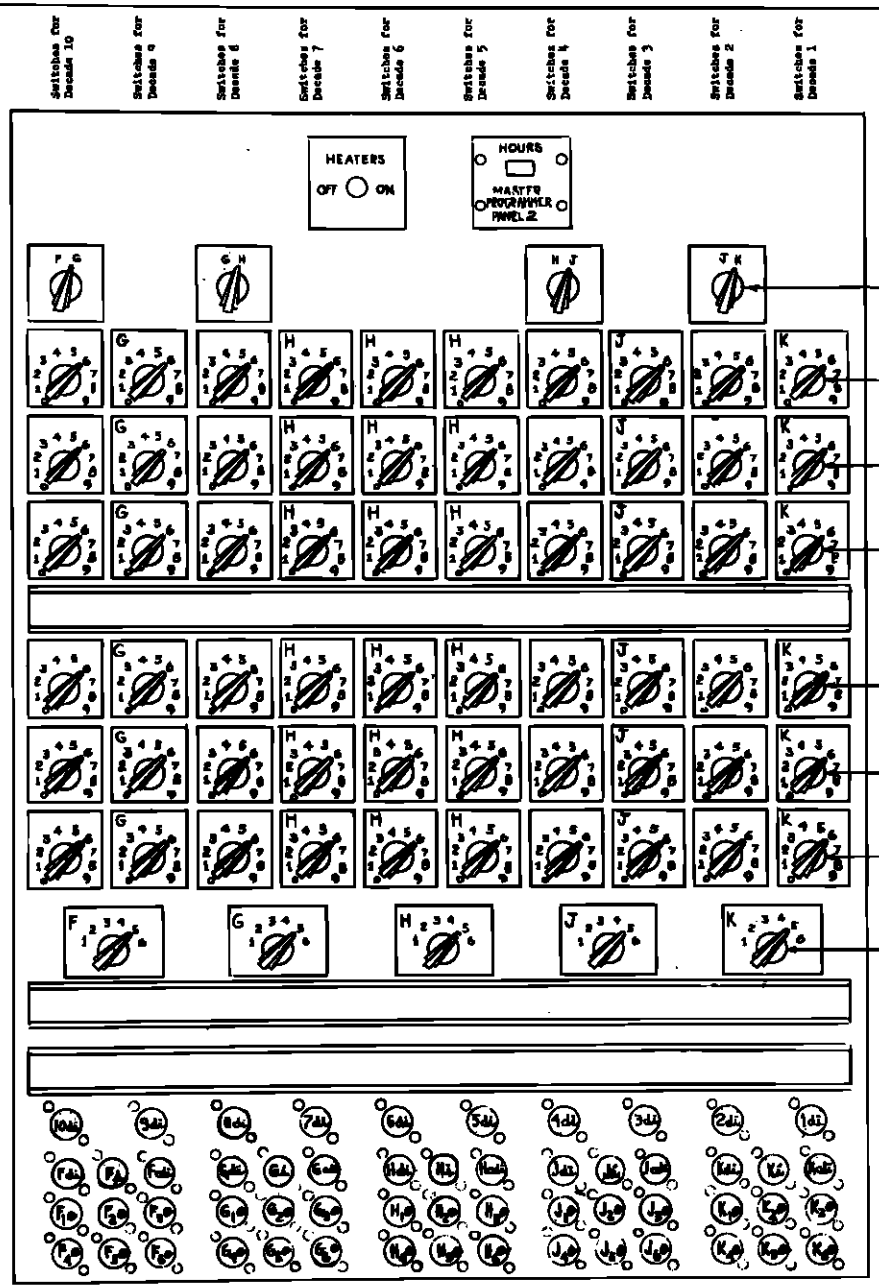
Terminals Acdi.....Kcdi — Stepper clear direct input terminals.

A pulse supplied to this terminal will clear the stepper to the first position. If a clearing pulse and a stepping pulse arrive at the same time, the stepper will be cleared, not stepped.

MOORE SCHOOL OF ELECTRICAL ENGINEERING UNIVERSITY OF PENNSYLVANIA		
MASTER PROGRAMMER FRONT PANEL NO. 1		
MATERIAL	FINISH	SCALE
Drawn by: J.CHELSKEY DEC. 1944	Checked by: J.B 10/12/45	Approved by:

PX-8-301

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To disassociate a decade from its stepper pull out gate tube 63 in the stepper plug-in unit - See Block Diagram PX-8-304.

Decade Associator Switches

Decades provided with these switches may be connected to the decades associated with either of two steppers. Thus if the J-K switch is set to K, decade 2 is connected in series with decade 1, while if it is set to J decade 2 is made the units decade associated with stepper J, and decade 3 (formerly the units decade associated with that stepper) becomes the tens decade of that stepper, i.e., is put in series with decade 2.

Decade switches associated with the 1st stages of the steppers.

Decade switches associated with the 2nd stages of the steppers.

Decade switches associated with the 3rd stages of the steppers.

Decade switches associated with the 4th stages of the steppers.

Decade switches associated with the 5th stages of the steppers.

Decade switches associated with the 6th stages of the steppers.

Stepper clear switch

This switch determines the number of stages of the stepper and associated decade switches which are used. After the stepper gets to the stage set on its clear switch and counts to the number set on the corresponding decade switches it clears to its first position instead of stepping to the next position.

Terminals 1di.....20di - Stepper direct input terminals.

Pulses supplied to one of these terminals will be counted by the stepper. These pulses may be either program pulses or digit pulses. If digit pulses are used the stepper clear switch must be set to 0.

The stepper will count modulo c, where c is the setting of the stepper clear switch.

A program pulse is emitted from one of the stepper program pulse output terminals one addition time after a program pulse is received on the stepper program pulse input terminal. This pulse is emitted from the terminal corresponding to the state of the stepper at the time it is emitted. The stepper may be stepped or cleared at the same time without effecting that pulse.

No pulse should be supplied to this terminal at the same time as a stepping action is caused by the decades.

TERMINALS 1di, 2di, ...,20di - Decade direct input terminals associated respectively with decades 1, 2,....,20. (counted from right to left)

Pulses supplied to these terminals will be counted by the decades. These pulses may be either program or digit pulses, though any pulse which steps the decades to the number set up on the decade switches corresponding to position of the stepper must be a program pulse, and any pulse which causes a carry-over must be a program pulse.

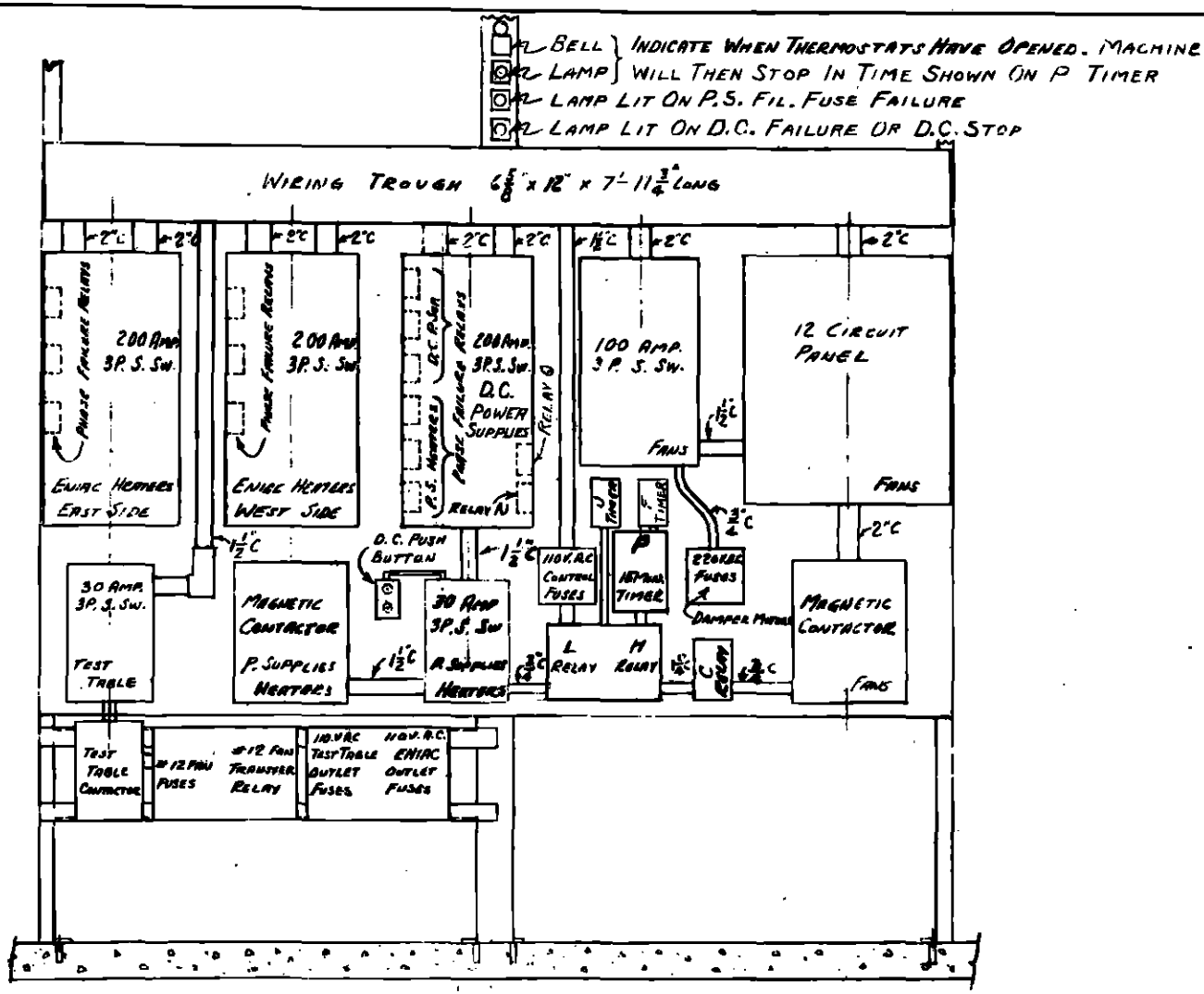
No program pulse should be supplied to the decade direct input of the units decade of a stepper one addition time following the reception of a program pulse on the program pulse input terminal of that stepper.

Pulses can be fed into the direct input terminals of decades other than the units decade only at times when there are no carry-over pulses from previous decades of the set.

MOORE SCHOOL OF ELECTRICAL ENGINEERING UNIVERSITY OF PENNSYLVANIA		
MASTER PROGRAMMER FRONT PANEL NO. 2		
MATERIAL	FINISH	SCALE
Drawn by: J.EBERT DEC.1944	Checked by:	Approved by:

PX-8-302

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REVISIONS		
F & P Timers Revised & Relays, Indicating Lamps & Bell Added.	J. Cummings	1-30-46

MOORE SCHOOL OF ELECTRICAL ENGINEERING UNIVERSITY OF PENNSYLVANIA			
A. C. Power Distribution Rack			
Material	Finish		Scale
Drawn by J. Cummings 12-21-45	Checked by J. Cummings 12-21-45	Approved by:	PX-1-304

Report on

THE ENIAC

(Electronic Numerical Integrator and Computer)

Developed under the supervision of the
Ordnance Department, United States Army

MAINTENANCE MANUAL

UNIVERSITY OF PENNSYLVANIA
Moore School of Electrical Engineering
PHILADELPHIA, PENNSYLVANIA

June 1, 1946

A REPORT ON THE ENIAC

(Electronic Numerical Integrator and Computer)

Report of Work under Contract No. W-670-ORD-4926

Between

Ordnance Department, United States Army
Washington, D. C.

and

The University of Pennsylvania
Moore School of Electrical Engineering
Philadelphia, Pa.

This is copy No. 19
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this report.

THE MAINTENANCE MANUAL

by

C. Chu
J. A. Cummings
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H. D. Huskey
T. K. Sharpless
R. F. Shaw

Moore School of Electrical Engineering
University of Pennsylvania

PREFACE

The Report on the ENIAC consists of five separately bound parts, as follows:

1. ENIAC Operating Manual
2. ENIAC Maintenance Manual
3. Part I, Technical Description of the ENIAC
   Volume I (Chapters I to VI)
4. Part I, Technical Description of the ENIAC
   Volume II (Chapters VII to XI)
5. Part II, Technical Description of the ENIAC

Included with the Operating Manual and Parts I and II of the Technical Description are all drawings (see table 0.3 below) which are required for understanding these reports. The Maintenance Manual assumes access to the complete file of ENIAC drawings.

Part I of the Technical Description is intended for those who wish to have a general understanding of how the ENIAC works, without concerning themselves with the details of the circuits; it assumes no knowledge of electronics or circuit theory. Part II is intended for those who require a detailed understanding of the circuits. Its organization, to a great extent, duplicates that of Part I so as to make cross referencing between the two parts easy.

The ENIAC Operating Manual contains a complete set of instructions for operating the ENIAC. It includes very little explanatory material, and hence assumes familiarity with Part I of the Technical Description of the ENIAC. The ENIAC Maintenance Manual includes description of the various test units and procedures for testing, as well as a list of common and probable sources of trouble. It assumes a complete understanding of the circuits of ENIAC, i.e. a knowledge of both Parts I and II of the Technical Description of the ENIAC.

The Report on the ENIAC and the complete file of ENIAC drawings constitute a complete description and set of instructions for operation and maintenance of the machine. The drawings carry a number of the form PX-n-m. The following tables give the classification according to this numbering system.

TABLE 0.1

Values of n	Division
1	General
2	Test Equipment
3	Racks and Panels
4	Trays, Cables, Adaptors, and Load Boxes
5	Accumulators
6	High Speed Multiplier
7	Function Table
8	Master Programmer
9	Cycling Unit and Initiating Unit
10	Divider and Square Rooter
11	Constant Transmitter
12	Printer
13	Power Supplies

TABLE 0.2

Values of m	Subject
101-200	Wiring Diagrams
201-300	Mechanical Drawings
301-400	Report Drawings
401-500	Illustration Problem Set-Ups.

The reader of this report will be primarily interested in the types of drawings listed in the following paragraphs. A table on page 4 gives the corresponding drawing number for each unit of the ENIAC.

1) Front Panel Drawings. These drawings show in some detail the switches, sockets, etc., for each panel of each unit. They contain the essential instructions for setting up a problem on the ENIAC.

2) Front View Drawings. There is one of these drawings for each kind of panel used in the various units of the ENIAC. These show the relative position of the trays and the location of the various neon lights. Since these drawings show the neon lights, they can be used to check the proper operation of the various units.

3) Block Diagrams. These drawings illustrate the logical essentials of the internal circuits of each unit. That is, resistors, condensers, and some other electrical details are not shown; but complete channels (paths of pulses or gates representing numbers or program signals) are shown in all their multiplicity. These drawings will be of interest to those who are interested in Parts I and II of the Technical Report.

4) Cross-section Diagrams. These drawings are electronically complete except that only one channel is shown where there is more than one. Thus, these drawings show every resistor and condenser and any other electronic elements belonging to any circuit. These drawings will be of particular interest to the maintenance personnel and to those reading Part II of the technical report.

5) Detail Drawings. All other drawings of the ENIAC come under this heading. A complete file of drawings is available at the location of the ENIAC.

Table 0.3
ENIAC DRAWINGS

Unit	Front Panel	Front View	Block Diagram	Cross - Section
Initiating Unit	PX-9-302 9-302R	PX-9-305	PX-9-307	
Cycling Unit	PX-9-303 9-303R	PX-9-304	PX-9-307	
Accumulator	PX-5-301	PX-5-305	PX-5-304	PX-5-115
Multiplier	PX-6-302 6-302R 6-303 6-303R 6-304 6-304R	PX-6-309	PX-6-308	PX-6-112A 6-112B
Function Table	PX-7-302 7-302R 7-303 7-303R	PX-7-305	PX-7-304	PX-7-117 7-118
Divider and Square Rooter	PX-10-301 10-301R	PX-10-302	PX-10-304	
Constant Transmitter	PX-11-302 11-302R 11-303 11-303R 11-304 11-304R	PX-11-306	PX-11-307	PX-11-116 11-309 (C.T. and R.)
Printer	PX-12-301 12-301R 12-302 12-302R 12-303 12-303R	PX-12-306	PX-12-307	PX-12-115
Master Programmer	PX-8-301 8-301R 8-302 8-302R	PX-8-303	PX-8-304	PX-8-102

Other drawings of particular interest:

Floor Plan	PX-1-302	IBM Punch and Plugboard	PX-12-112 PX-12-305
A.C. Wiring	PX-1-303		
IBM Reader and plugboard	PX-11-119 PX-11-305	Pulse Amplifier and Block Diagram	PX-4-302 PX-4-301
Interconnection of Multiplier and Accumulators			PX-6-311
Interconnection of Divider and Accumulators			PX-10-307

The front view drawings and the large front panel drawings (whose numbers do not end with "R") are bound as a part of the Operator's Manual.

Included with the report is a folder containing all the drawings listed in the above table except the large front panel (see above). A complete file of drawings is available at the location of the ENIAC.

I. INTRODUCTION TO MAINTENANCE MANUAL

1.1 Structure of Maintenance Manual

The maintenance manual devotes a chapter to each unit of the ENIAC including one chapter to the a-c supply circuits. These various chapters were written by the people who designed or helped to design the respective unit.

Each chapter contains a list of the wiring diagrams and test charts referring to the circuits of that particular unit. It contains a section giving a testing procedure for the particular unit. Note that test procedures for each unit are also given in the operating manual. In each chapter there is also a list of possible failures and their remedies. As time goes on the conscientious maintenance man will do well to keep a log book listing for each unit failures encountered, their symptoms, and the remedy.

1.2 Notes and Warnings to Maintenance Personnel

1) Keep in touch with operating group for any trouble which may develop. Note repairs and troubles in log book. Keep log of all tube failures - list each tube.

2) This machine contains a number of dangerously high voltages. Avoid working on any part while DC is on.
   Do not leave off any covers. Remember the shells of the metal tubes are at high potential with respect to the frame.

3) Never operate machine with any DC fuses out except for special tests. When replacing a DC fuse be sure they are put in correctly - i.e. washer in cupface out.

4) Make periodic check on ventilating fans.

5) Do not pound on plugs or plug-in units to get them in; use steady pressure. Avoid pulling on wires or cables to remove plugs; use case for grip.

6) Keep covers on relays as much as possible; replace in same position to avoid spilling onto relay contacts dust which may have collected.

7) Return all plug-in units and cables to proper racks when not in use.

8) DON'T'S

   (a) DON'T leave doors or coverplates leaning against relays or tubes or front panels.

   (b) DON'T hang probes on wires in trays.

   (c) DON'T mark panels with chalk or stick paper labels on them.

   (d) DON'T drop solder, nuts, lock washers, etc., inside machine and leave them there. GET THEM OUT!

1.3 General Remarks on Testing

1.3.1 Standard Test Problems

Standard test problems check for continuity of the programming set-up unless there are attached subsequences which operate simultaneously. Generally a standard test problem cannot be designed so as to test the numerical circuits completely. However, it comes much closer to completely

checking the program control and common programming circuits.

1.3.2 Systematic Unit Tests

Systematic tests such as those described in the operating manual are designed to check the numerical circuits and common programming circuits. If repeated with different program controls, they check the program control circuits. The chapters of this manual give some other testing methods for certain of the units.

1.4 Responsibility of Maintenance Personnel

1) To have studied the four manuals (Operating Manual, Technical Reports I and II, and the Maintenance Manual) sufficiently to thoroughly understand the operation of each unit and the operating of the ENIAC as a whole.
2) Knowing that a particular unit is failing to be able to find and remedy that failure.
3) Knowing of the existance of a failure in the ENIAC to be able to assist the operating personnel in localizing the failure to particular units. However, the duty of isolating numerical and programming failures to a particular unit belongs primarily to the operating personnel.

1.5 ENIAC Drawings

The maintenance personnel should have access to a file of drawings at the location of the ENIAC. As part of the file of drawings there is a complete catalog of all the drawings of the ENIAC. Only a few of the drawings are referred to in the various reports and in case of difficulty with particular circuits the maintenance man should refer to the catalog for

any other drawings which may be of help.

Drawings which will be of particular help for maintenancing will be the various block diagrams and the cross-section diagrams of each unit.

1.6 General Remarks on Trouble Shooting

After a test problem has indicated a failure it becomes a problem of localization.

1.6.1 Find the Unit that Failed

To the operating personnel the type of failure found in the test problem may indicate the unit (or kind of unit) in which the failure occurred. Various unit tests (such as those described in the operating manual) may be performed to assist in this localization process.

1.6.2 Finding the Circuit that Failed

The various unit tests are designed to localize the failure to a particular circuit. Complete knowledge of part II of the technical report and efficient use of block diagrams will help in this process.

1.6.3 Circuit Failures

The most frequent failure in circuits is burned out tubes. Replace tubes in suspected circuits and test the tubes removed (see Section on use of the tube testor). Note that cathode failures in metal case tubes can be detected at removal time by comparing case temperature with that of other tubes.

If all the tubes in the suspected circuits test all right a static test of the circuits is indicated to check against failures in wiring, resistors, or condensers. To assist in static and dynamic testing test charts have been prepared and certain test equipment built (see The charts have detailed instructions giving switch settings, voltages,

pulse rise, duration, and fall times, pulse amplitudes, et cetera.

The following principles in trouble shooting are worth noting.

1) If a circuit operates when it shouldn't look for failure of an inverter tube.

2) If a circuit does not operate when it should look for failure of a gate or a buffer.

1.7 Transient Failures

Transient failures can usually be found by repeated programming of the suspected unit. As explained below certain test equipment has been built to assist in finding transient failures.

Practically all circuits in the ENIAC were designed with at least a 2 to 1 safety factor. Thus, parameters (such as loads, voltages, et cetera) can be varied considerably without effecting the operation of a normal unit.

Thus, to assist in finding transient failures certain test equipment (namely, a variable oscillator and variable power supply equipment) has been built. The variable oscillator can be plugged into the cycling unit and the ENIAC operated at frequencies above or below the standard frequency of 100 kc. The variable power supply can be used to vary the voltages in a unit and thus increase the probability of failure.

II. INITIATING UNIT

2.1 Circuits of the Initiating Unit

Tables 2.0 and 2.1 give a list of drawings pertaining to the Initiating Unit. The Interconnection diagram, PX-1-301, shows the location of the plug-in units and gives the numbers of the chassis drawings.

Table 2.0

INITIATING UNIT PLUG-IN UNITS

No. of units used in Initiating Unit	Plug-in Unit	Wiring Diagram	Static and Dynamic Test Chart
19	Cycling Unit Transmitters	PX-9-102A	PX-9-123
6	Transceivers	PX-5-147	PX-5-129
2	Initiating Pulse Units	PX-9-105	PX-9-125
1	Reader- Printer Starting Unit	PX-9-104	PX-9-122
1	Reader Interlocking Unit	PX-9-103	PX-9-124
1	Reader Transmitter Unit	PX-9-106	PX-9-121

Table 2.1

OTHER INITIATING UNIT CIRCUITS

Name	Wiring	Static Test Chart
Oscilloscope	PX-9-115	PX-9-126
DC Voltmeter	PX-9-118, 119 A, 119B	
Initial Clear Relay	PX-9-115, 119	
AC Voltmeter	PX-9-118A, 119	
Start, Stop, and Door Switch Shunt	PX-9-119 (see Block Diagram PX-9-307)	

2.2 Testing Program

Tests for each of the plug-in units are described on the test charts listed and covered in the section on the use of the Test Bench.

Tests on the plug-in units in place in the unit are outlined below.

A) Cycling Unit Transmitters

With cycling unit on continuous operation observe CPP, 9P, 1'P, RP on Oscilloscope on cycling unit. Presence of pulses of at least one inch amplitude and equal width for each pulse indicates all is well. If not replace one or more of the associated cycling unit transmitters. If no pulse at all, check on gates which produce the missing pulses for presence of pulse at output. Block diagram PX-9-307 will be most useful here.

B) Selective Clear Transceivers

Connect each to a program line carrying continuous program pulses, then observe neon lights. If any unit fails, replace it.

C) Initiating Pulse Units

One of these units is used to produce a pulse synchronized with the Eniac when the initiating pulse switch is pushed. The other produces a synchronized pulse when the printer finishes an operation. To check the first, connect output to input of one selective clear transceiver, set cycling unit on 1 add operation. Push initiating pulse switch, upper neon should light; pulsh 1 pulse 1 add switch, lower neon should light, push 1 pulse 1 add switch again, both neons out and transceiver neon should light.

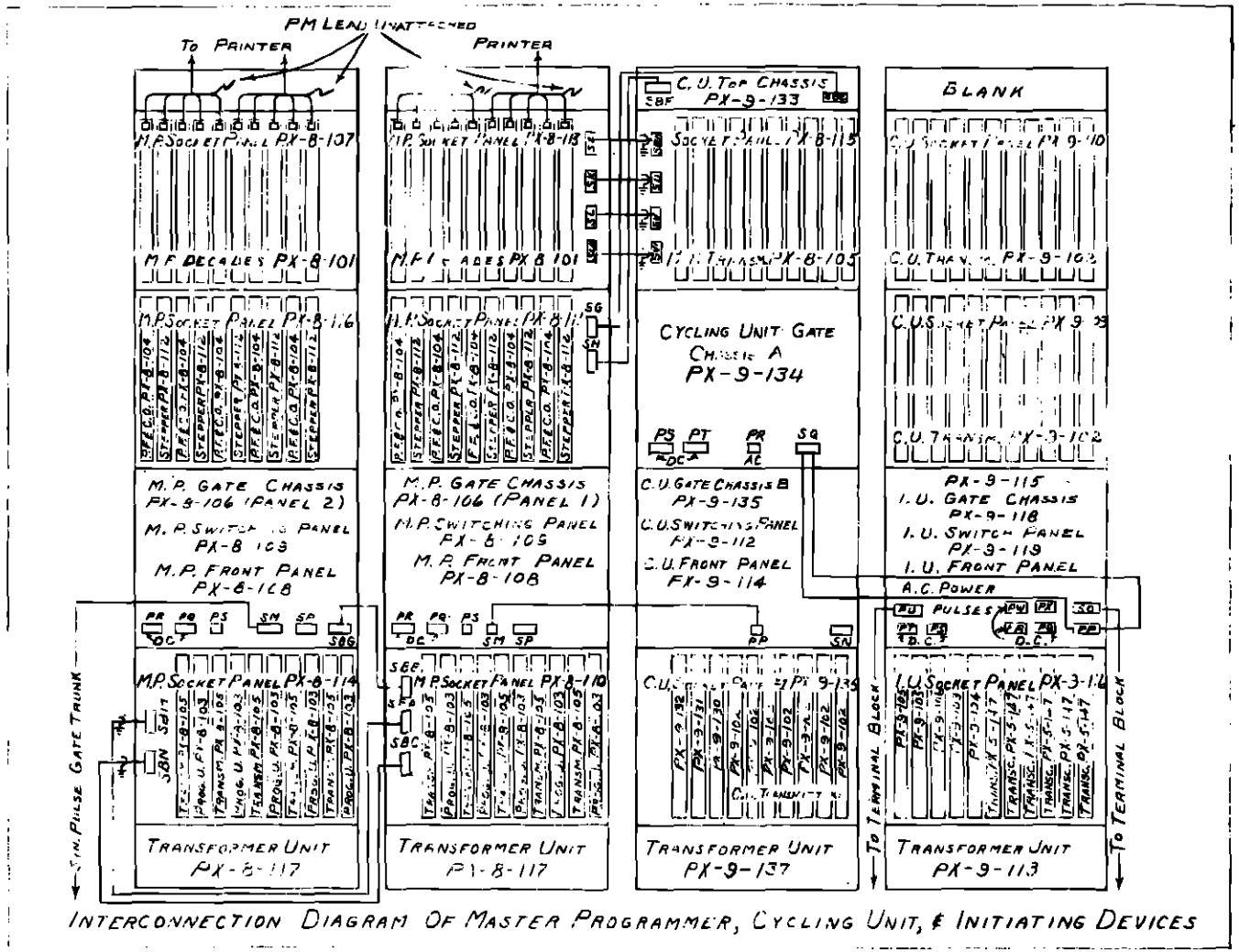
To test the other, connect printer into a program chain. This will also test printer section of Reader-Printer Starting Unit.

D) To test Reader-Printer Starting Unit, Reader Interlocking Unit, Reader Transmitter Unit, plug reader output into selective clear transceiver to check presence of output pulse. Set Cycling Unit on 1 add time. Push reader start switch, reader start neon on, reader interlock neon on, IBM reader should feed card, reader finish neon on. After card feed push 1 add button, reader start neon out, reader synchronizing neon on. After next 1 add push reader interlock neon out, reader synchronizing neon out, transceiver neon on.

E) The Oscilloscope section needs no special mention as to service. The standard tests for the RCA 155A' scope are applicable with the exception that the sweep frequency operates at approximately 60 CPS.

F) Servicing of the two voltmeter circuits is straightforward - checks for open circuits, short circuits, rosin joints, loose connection, etc.

G) The initial clear relay circuits are shown on PX-9-307. The time constant of the condenser relay circuit is sufficient that the relay should stay closed for not less than 1/2 second. In case of trouble look for failure of condenser or relay.



Interconnection Diagram Of Master Programmer, Cycling Unit, & Initiating Devices

Transformer Unit in Panel 1 was PX-8-114; Transformer Unit in Panel 2 was PX-8-110.

1	2/7/45	Interconnections revised. Pulses added.
2	4/18/45	
3		Master Programmer Panels & Initiating Unit Panel Brought Up To Date. Cycling Unit Gates Menum Mered, SBE & SBF, PRPSPT, Indicated. Decade Spare Cables of M.P. Shown.

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M.P., C.U. & I.U. INTERCONNECTION DIAGRAM

Material	Finish	Scale

Drawn by:	Checked by:	Approved by:	
C.J.McC	R.J.A.	J.H. Sharpless	PX-1-301
Jan. 1, 1945	11 Jan 45	1-11-45	

III. CYCLING UNIT

3.1 Circuits of Cycling Unit

The cycling unit panel includes ten transmitter plug-in units of the master programmer (see Chapter X) as well as the circuits of the cycling unit proper. The following tables and PX-1-301 give the pertinent drawings and show the position of the plug-in units.

Table 3.1

PLUG-IN UNITS

Number of Units	Name	Wiring Diagram	Static and Dynamic Test Charts
10	Master Programmer Transmitters	PX-8-105	PX-8-122
6	Cycling Unit Transmitters	PX-9-102A	PX-9-123
1	Cycling Unit Carry Gate Transmitter	PX-9-102B	PX-9-123
1	Cycling Unit Off-beat Unit	PX-9-130	PX-9-139
1	Cycling Unit Oscillator	PX-9-131	PX-9-140
1	On-beat Unit	PX-9-132	PX-9-141

Table 3.2

CHASSIS CIRCUITS

Name	Position (tubes)	Wiring	Test Chart
Top chassis	1 and 2	PX-9-133	Static: PX-9-128 PX-9-128A
Gate A	21 to 40	PX-9-134	
Gate B	41 to 60	PX-9-135	Dynamic: PX-9-129

3.2 Testing Procedure

The routine testing of the cycling unit is best carried out in the following manner. With the operations switch on continuous and the oscillator switch on Internal, the various pulses and the carry gate are examined on the viewing scope. Their presence is not sufficient for satisfactory operation but the pulses must all be of approximately the same shape and all signals at least one inch high. Next, the external oscillator should be plugged in and the switch set to External, the tens pulses should be examined on the viewing scope. The frequency should be increased until either a shift of 1 pulse to the right is observed in the tens pulses or one or more neon bulbs in cycling unit ring glow. The frequency at which this occurs should be at least 160 kc. At this top speed the other pulses and gate should be again examined. The most common difficulty in the cycling unit is failure of the ring to count at these high frequencies. This can usually be traced to trouble in the ring pulse standardizer.

The 1 addition time mode of operation as well as the one pulse time mode must also be tested. Test the 1 add mode at 100 kc and also at the top

frequency. Presence of the tens pulses must also be checked. This is done by programming a chain of two programs, one event of which is to tell an accumulator to transmit. Then, continued pushing of the 1 pulse 1 add switch should result in the program chain stopping along and on the one program, the accumulator cycling, as evidenced by the neons flashing, but the same number remaining in the accumulator. The same test should be made under 1 pulse time operation requiring, of course, 40 pushes of the switch to go through the two program sequence. Should any of the above tests fail the 1 add gate, ring stop gate, 10 pulse flip-flop, and 10 pulse gate should be investigated first.

Trouble in the Viewing Scope may result from disturbed DC voltages which are produced in the top panel or due to failure of the sweep circuit which is located on Gate Chassis B, PX-9-135. This circuit is similar to one used in the A-R Scope, type 256B, but uses different tubes. A discussion of this type of circuit will be found in the A-R Scope Manual.

IV. ACCUMULATOR

4.1 Accumulator Circuits

The following tables and PX-5-302 give the numbers of drawings and the location of various accumulator circuits.

Table 4.1

ACCUMULATOR PLUG-IN UNITS

Number of Units	Plug-in Unit	Wiring Diagram	Static and Dynamic Test Chart
10	Decade	PX-5-133	PX-5-126
1	PM Clear	PX-5-108	PX-5-127
2	Receiver	PX-5-148	PX-5-128
8	Transceiver	PX-5-147	PX-5-129
1	Repeater	PX-5-149	PX-5-120

Table 4.2

ACCUMULATOR DRAWINGS

Name	Position (tubes)	Wiring	Test Chart
Gate Chassis	41 to 60	PX-5-117	Static: PX-5-123 Dynamic: PX-5-124

4.2 Testing Procedure

4.2.1 Numerical Circuits

(a) Receiving failures.

Using the accumulator test cards described in the operating manual (section 2.2) the constant transmitter can be used to transmit numbers into an accumulator.

In case of failure in this sort of test, there are two possible procedures:

1) Shift to another input and repeat the test.

2) Program a transmission at one pulse time speed.

Either of these procedures will generally determine whether the failure is in the decade unit or in the input gate circuits. If the failure is in the decade unit replace it (repairing of plug-in units is discussed in the section on the test bench, Chapter XII).

Any systematic test should involve receiving numbers on all five inputs.

4.2.2 Transmission Failures

With a number such as F 44444 44444 in the doubtful accumulator, it should be programmed to add its contents to another accumulator at a one pulse time rate. The receiving accumulator should be known to be operating correctly, of course.

Consecutively, or simultaneously by using a second accumulator to receive, the subtract transmission circuits can be checked.

4.3 Common Programming Circuits

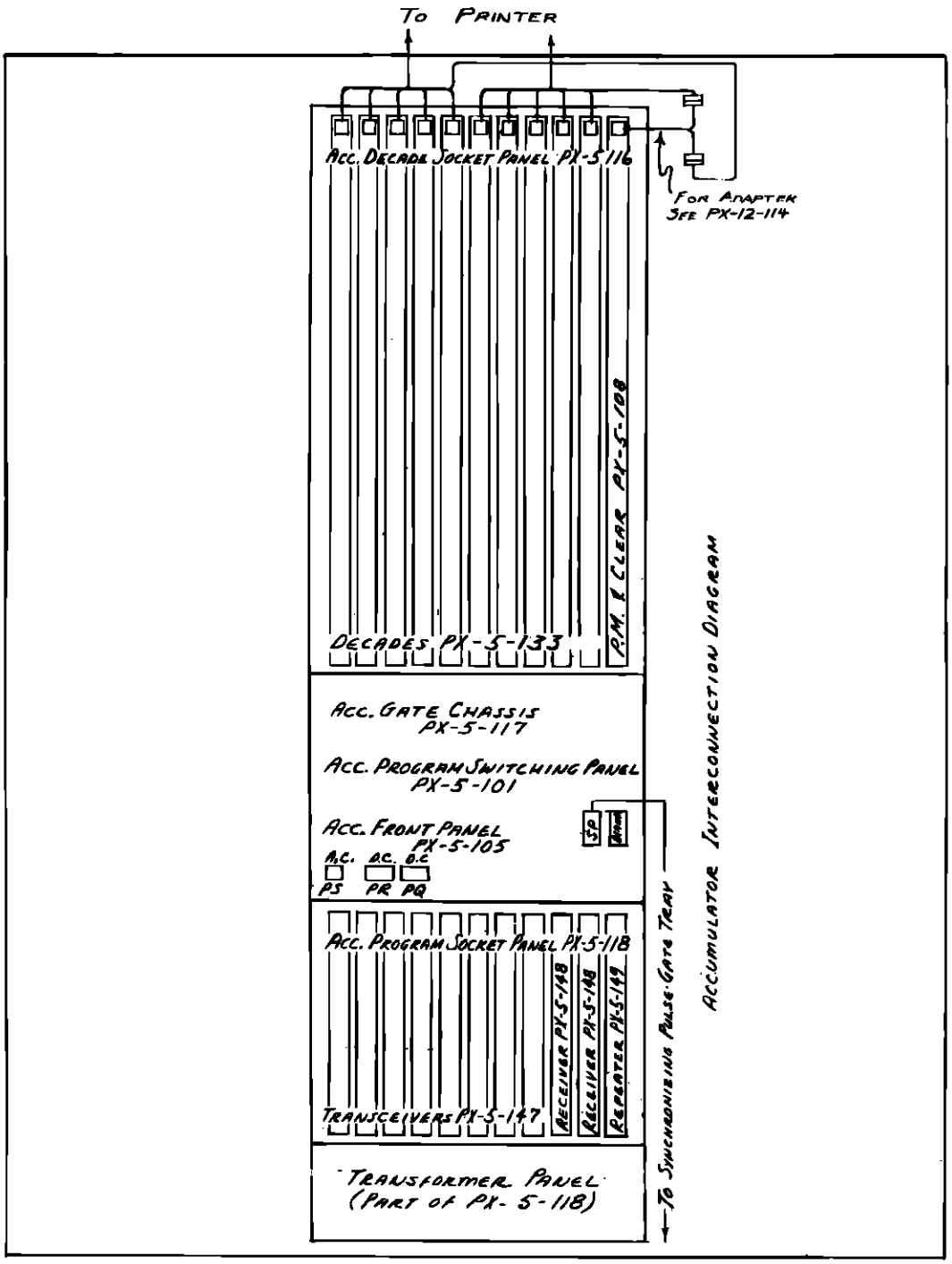
Simultaneously failure in all ten channels (or eleven channels in some cases) persisting with various program controls indicates failure

in common programming circuits.

4.4 Program Control Failure

If only one fails replace it. If more than one transceiver fails look for trouble in common programming circuits perhaps checking other transceivers. Failure of more than one program control flip-flop to reset indicates possible failure in the repeater ring circuits.

DECADE STATIC OUTPUTS, PM LINES AND PM ADAPTOR ADDED. J Sumney 3-21-45 | 1



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ACCUMULATOR INTERCONNECTION DIAGRAM

Drawn by	Checked by	Approved by
	J Sumney 7-2-45	

MATERIAL / FINISH / SCALE /

PX-5-302

V. HIGH SPEED MULTIPLIER

5.1 Multiplier Circuits

The circuits of the multiplier are located on three panels. The interconnection diagram, PX-6-301, shows the position of the various circuits and the following table gives the numbers of some of the pertinent drawings.

Table 5.1

PLUG-IN UNITS OF THE MULTIPLIER

Number used	Name	Wiring Diagram	Test Charts
24	Transceiver	PX-5-147	PX-5-129
6	Buffer Units	PX-6-107	PX-6-130
2	Receiver	PX-5-148	PX-5-128

5.2 Testing Procedure

The multiplier lends itself nicely to a routine automatically programmed test. The details of this test are given in the ENIAC Operating Manual.

In case of failure in the above test, the program should be stepped through by one addition time steps and the partial products appearing in the product accumulators inspected. This procedure if done in conjunction with tracing the numbers course through the multiplier (by use of the block diagram, PX-6-308) may locate the failure. If this fails to locate trouble, step by addition times to the region of failure, then by pulse times.

Table 5.2

CHASSIS DRAWINGS

Name	Position		Wiring	Test Charts
	Panel	Tubes		
Ior Selector	1	3 - 20	PX-6-101	Static:
R.H. Multiplier Table	1	21 - 40	PX-6-102	Panel 1 PX-6-122
L.H. Multiplier Table	1	41 - 60	PX-6-103	Panel 2 PX-6-126
Ior Top Chassis	3	1 and 2	PX-6-105	Panel 3 PX-6-128
Gate	2	41 - 60	PX-6-108	Dynamic:
Gate	3	41 - 60	PX-6-109	Panel 1 PX-6-123
Icand L.H. Selector	2	21 - 40	PX-6-110	Panel 2 PX-6-127
Icand R.H. Selector	2	3 - 20	PX-6-110	Panel 3 PX-6-129
R and L Shifter	2	3 - 20 and 21 - 40	PX-6-111	

By checking the pulse groups arriving at the product accumulators (and comparing this with the actual products of the digits of the numbers being multiplied) bad tubes may be found.

5.3 Possible Failures

1) Failure of gate tubes in multiplier selector would cause table to pass nine pulses.

2) Failure of gate tubes in multiplicand selector or in shifter would cause zero pulses to arrive at the corresponding place in the partial product.

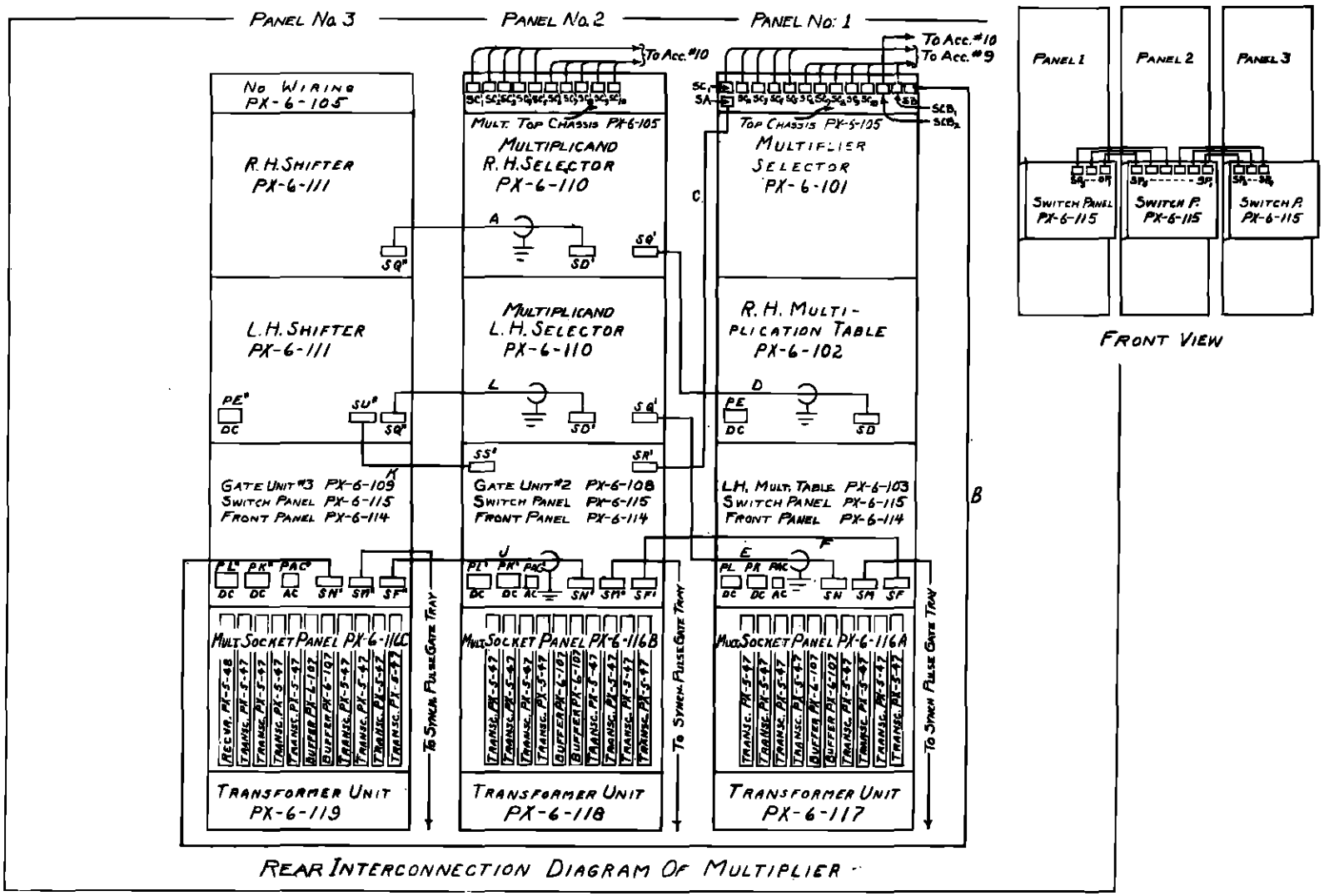
3) Failure of buffer or inverters in the channels may cause either of the above effects.

4) Failure of table output gates would cause 1, 2, 2', or 4 pulses to fail to reach the product accumulator.

5) Failure of drivers on the output would cause a digit to be missing from each partial product.

6) Failure of program control transceivers.

7) Failure of common programming circuits.



REAR INTERCONNECTION DIAGRAM OF MULTIPLIER

FRONT VIEW

SEPT. FINAL REVISION
ADDED: SC_1 TO SC_{10} & SC_1 TO SC_{10} FRONT VIEW - INTERCONNECTING CABLES, $3P_1$ TO $3P_6$. SYNCH. PULSE GATE LINE TO TRAY. FRONT AND SWITCH PANEL IDENTIFICATION ON THIRD GATE CHASSIS DOWN, EACH PANEL. LINES BETWEEN 58 & SCB_1 & SCB_2 REMOVED.
Y.H. 9-18-45

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INTERCONNECTION DIAGRAM OF HIGH-SPEED MULTIPLIER

MATERIAL	FINISH	SCALE
/	/	/

Drawn by:	Checked by:	Approved by:	
C.J.McC JAN. 8, 1945	F.R.B.t. Michael Aug. 17, 1945	Y.H. 9-18-45	PX-6-301

VI. DIVIDER AND SQUARE ROOTER

6.1 Divider and Square Rooter Circuits

The following tables give the numbers of some of the pertinent drawings of the divider and square-rooter. PX-10-303 shows the positions of the chasses and the plug-in units.

Table 6.1a

DIVIDER AND SQUARE ROOTER PLUG-IN UNITS

Number of Units	Name	Wiring	Test Charts
10	Receivers	PX-5-148	PX-5-128
8	Transceivers	PX-5-147	PX-5-129
2	Buffers	PX-6-107	PX-6-130
1	Repeater	PX-5-149	PX-5-130
1	Decade Ring (Master Programmer)	PX-8-101	PX-8-125

Table 6.1b

DIVIDER AND SQUARE ROOTER CIRCUITS

Name	Position	Wiring	Test Charts
Gate No. 1	3 - 20	PX-10-106	Static: PX-10-115A-D
Gate No. 2	41 - 60	PX-10-105	
Top	1 and 2	PX-10-112	Dynamic: PX-10-116A-C

6.2 Checking the Operation

Since the divider and square rooter works in conjunction with a number of accumulators the first thing to do is to systematically check all

these accumulators (see Chapter IV).

Drawings PX-10-403 and PX-10-404 show the numbers occuring at various places in the accumulators during sample division and square root problems. These problems may be done at one addition rate after a failure is indicated.

Since part of the control circuits go to accumulators via cables and trays the operator should carefully check these when trouble is suspected. The presence of the proper adaptors, et cetera, should be verified.

Note that the square root of zero is the simplest test problem that the unit can be caused to do.

6.2.1 Program Control Failures

If any transceiver remains "on" then it should be replaced. If more than one remains on, then the common programming circuits should be inspected. Check in particular to see if the program ring cycles as it should. If the program ring cycles as it should, inspect the clearing circuits.

6.2.2 Numerical Circuit Failures

Check the quotient place ring and the various pulse gates including the $\pm$ 1 or $\pm$ 2 receivers.

6.2.3 Common Programming Circuit Failures

Using the block diagram and a sample division or square root problem the operator should proceed at one addition time (and perhaps repeat at one pulse time rate) rate and note the first circuits which fail to operate (as indicated by the neon lights on the front panels). Reference should be made to PX-10-302.

REVISIONS

PX-8-101 Alter at Decade Ring

1

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DIV. INTERCONNECTION DIAGRAM

MATERIAL	FINISH	SCALE
/	/	/

Drawn by	Checked by	Approved by:	
JLP 6/29/45	C. Shu		PX-10-303

TABLE 6-2

DIVISION - ILLUSTRATIVE PROBLEM

Problem: Divide P 0 2090070 000 by P 0 230 000 000. Round answer off to 4 places. No interlock.

Period	Add. Time	Quotient Accumulator		Numerator Accumulator		Denominator Accumulator	Shift Accumulator	
		Receives	Stores after Receiving	Receives	Stores after Receiving	Receives during period 1 and stores thereafter.	Receives	Stores after Receiving
I	1			P 0 209 070 000	P 0 209 070 000	P 0 230 000 000		
	2							
	3							
II	4			M 9 770 000 000	M 9 979 070 000			
	5	P 0 100 000 000	P 0 100 000 000					
shift	6			~~~			M 9 790 700 000	M 9 790 700 000
	7			M 9 790 700 000	M 9 790 700 000		~~~	
	8			P 0 230 000 000	P 0 020 700 000			
	9	M 9 990 000 000	P 0 090 000 000					
shift	10			~~~			P 0 207 000 000	P 0 207 000 000
	11			P 0 207 000 000	P 0 207 000 000		~~~	
	12			M 9 770 000 000	M 9 977 000 000			
	13	P 0 001 000 000	P 0 091 000 000					
III	14			~~~			M 9 770 000 000	M 9 770 000 000
	15			M 9 770 000 000	M 9 770 000 000		~~~	
	16			P 0 230 000 000	P 0 000 000 000			
	17			P 0 230 000 000	P 0 230 000 000			
	18			P 0 230 000 000	P 0 460 000 000			
	19			P 0 230 000 000	P 0 690 000 000			
	20			P 0 230 000 000	P 0 920 000 000			
	21							
	22	P 0 000 000 000	P 0 091 000 000					
IV	23							
	24		Program output pulse and answer disposal signal is transmitted					
	25		Answer is transmitted from quotient accumulator.					

DX-10-404

TABLE 6-3

SQUARE ROOT - ILLUSTRATIVE PROBLEM

Problem: Find $\sqrt{\text{P 0 081 360 400}}$. Round answer off to 4 places. No interlock

Period	Add. Time	Numerator (Radicand) Accumulator		Denominator (2 root) Accumulator		Shift Accumulator	
		Receives	Stores after receiving	Receives	Stores after receiving	Receives	Stores after receiving
I	1	P 0 081 360 400	P 0 081 360 400				
	2						
	3						
	4			P 0 100 000 000	P 0 100 000 000		
II	5	M 9 900 000 000	M 9 981 360 400				
	6			P 0 200 000 000	P 0 300 000 000		
shift	7			M 9 900 000 000	P 0 200 000 000	M 9 813 604 000	M 9 813 604 000
shift	8	M 9 813 604 000	M 9 813 604 000	M 9 990 000 000	P 0 190 000 000		
	9	P 0 190 000 000	P 0 003 604 000				
	10			M 9 980 000 000	P 0 170 000 000		
shift	11			P 0 010-000 000	P 0 180 000 000	P 0 036 040 000	P 0 036 040 000
shift	12	P 0 036 040 000	P 0 036 040 000	P 0 001 000 000	P 0 181 000 000		
	13	M 9 819 000 000	M 9 855 040 000				
	14			P 0 002 000 000	P 0 183 000 000		
III	15			M 9 999 000 000	P 0 182 000 000	M 8 550 400 000	M 8 550 400 000
	16	M 8 550 400 000	M 8 550 400 000				
	17	P 0 182 000 000	M 8 732 400 000				
	18	P 0 182 000 000	M 8 914 400 000				
	19	P 0 182 000 000	M 9 096 400 000				
	20	P 0 182 000 000	M 9 278 400 000				
	21	P 0 182 000 000	M 9 460 400 000				
	22						
	23			M 9 995 000 000	P 0 180 000 000		
IV	24						
	25		Program output pulse and answer disposal signal is transmitted.				
	26		Answer is transmitted from denominator accumulator.				

VII. FUNCTION TABLE

7.1 Function Table Circuits

The function table is located on two panels and there is the portable table which plugs into both panels. Tables 7.1 and 7.2 give some of the pertinent drawing numbers and PX-7-301 shows the location of the various circuits.

Table 7.1

PLUG-IN UNITS

Number of Units	Name	Wiring	Test Charts
11	Transceivers	PX-5-147	PX-5-129
1	Portable Table	PX-7-134 and PX-7-135	

7.2 Operation Test

A test sequence similar to that described in section 2.4 of the operating manual is set up. After initially clearing, set cycling unit to 1 add, and run through 3 or 4 complete cycles of the program, observing both the neons on upper panel of function table, and numbers in accumulators. Push initiating button, then 1 pulse-1-add button repeatedly; when program ring is on second (-2) stage, next push of button will cause argument to be sent to function table; next push should cause units ring to move 2 stages further; second push after this should cause function to be transmitted to accumulators and function table rings to be cleared.

After this preliminary check, return cycling unit to continuous operation, initially clear, and run through 100 argument values. At each stage of this process the accumulators should indicate the argument and the

Table 7.2

FUNCTION TABLE CIRCUITS

Name	Position		Wiring	Static Test Charts	Dynamic Test Charts
	Panel	Tubes			
Top	1	1 and 2	PX-7-119	PX-7-137 A and B	PX-7-138
Upper Function Selector	1	11 - 20	PX-7-120		
Lower Function Selector	1	21 - 40	PX-7-121		
Gate	1	41 - 60	PX-7-122		
Top	2	1 and 2	PX-7-126	PX-7-139	PX-7-140
Gate A	2	3 - 20	PX-7-127		
Gate B	2	21 - 40	PX-7-128		
Gate C	2	41 - 60	PX-7-129		
Gate D	2	61 - 80	PX-7-130		

corresponding function as set up on the portable table. To check -2 and -1 arguments, set function table program switch to -2 and initially clear; then function shown for 0 argument is that set on -2 row of switches and that shown for 1 argument is that set on -1 row (Note that, since correction pulse goes into argument accumulator at beginning of cycle, zero argument cannot be transmitted immediately after initially clearing; to get zero argument, either cycle around until argument accumulator shows 100, or pull out argument input cable at function table). To check 100 and 101 arguments, set program switch to +2 and cycle around until argument accumulator shows 98 and 99 respectively.

If in the preceding tests the program switch is set to "subtract" instead of "add", leaving all subtract pulse switches at "0", the function transmitted should be the nines complements of the numbers set on the switches.

7.3 Test Procedure

7.3.1 Rings - frequency

To check frequency tolerance of rings, pull out tubes specified and feed variable oscillator output to pin 8 of socket from which tube was removed in case of argument register; pin 3 in case of program ring; use a series condenser; other side of oscillator output goes to ground. Connect oscilloscope to any convenient static output; these points are the ones to which are connected wires in the cable going to neon bulbs on front panel. Rings should count at frequencies up to 180 kc.

To test ring	Pull out tubes
Units	D42
Tens	H42
Program	D49, E49, F49

7.3.2 Rings Voltage Tolerance

Use adaptor made for this purpose together with variable power supply; rings should be cycled continuously at 100 kc using variable frequency oscillator as in checking frequency tolerance. Rings should count at voltages from 120 to 300 volts.

7.3.3 Oscilloscope Check of Function Table Outputs

As additional check on operation, set up continuous program. No argument is used. Observe output by plugging triple connector into output socket, with a tray load box plugged into one of the three outputs; the scope probe can then be inserted in one of the other outputs. With program set to 0 and "add", the number of pulses observed on each channel should be the same as the number set on the corresponding switch. Operation of subtract pulse switches can be checked by observing appearance of 1' pulse on an output channel when corresponding subtract pulse switch is set to "S". On PM channels, 9 pulses should appear if either table or master switch is set to "M". PM positions on constant switches are most conveniently checked by observing result of changing corresponding master PM switch from "P" to "M" or vice versa.

7.4 Trouble Shooting Procedure

In the following list will be found a number of cases of abnormal operation together with their probable causes and remedies. Before making

any other tests, see that no switches are set half-way between detent positions.

a. All rings operate continuously - may be defective transceiver; check to see if any transceiver neons remain on. If only one remains on, replace defective unit. If more than one remain on, check clear gates (A48, B48, C48) and clear tubes (A49, B49, C49); also initial clear buffer (D48).

b. Program ring cycles continuously but argument register remains cleared - check repeater input gates (D49, E49, F49).

c. Program ring fails to cycle - check as in b. above; also check pulse former tubes (G49, H49, J49). Also check ring tubes, particularly if ring stalls on any except first stage.

d. Argument is not received but shifting takes place normally - check tubes K48, L48; if only one digit of argument is received, check D42, H42.

e. Neither argument nor shift pulses received - check pulse formers (B42, C42, A41; also J42, K42, L42). Check ring tubes if this fails; if ring stops on any except first stage (zero position), it is almost certain that a ring tube is defective.

f. Erroneous transmission or failure of transmission for ten adjacent argument values, others OK - check corresponding selector input gates (on top chassis of panel 1).

g. Erroneous transmission or failure of transmission for all arguments having a given units digit (for example, 8, 18, 28, 38, etc.) - check vertical drivers (row 28 on panel 1).

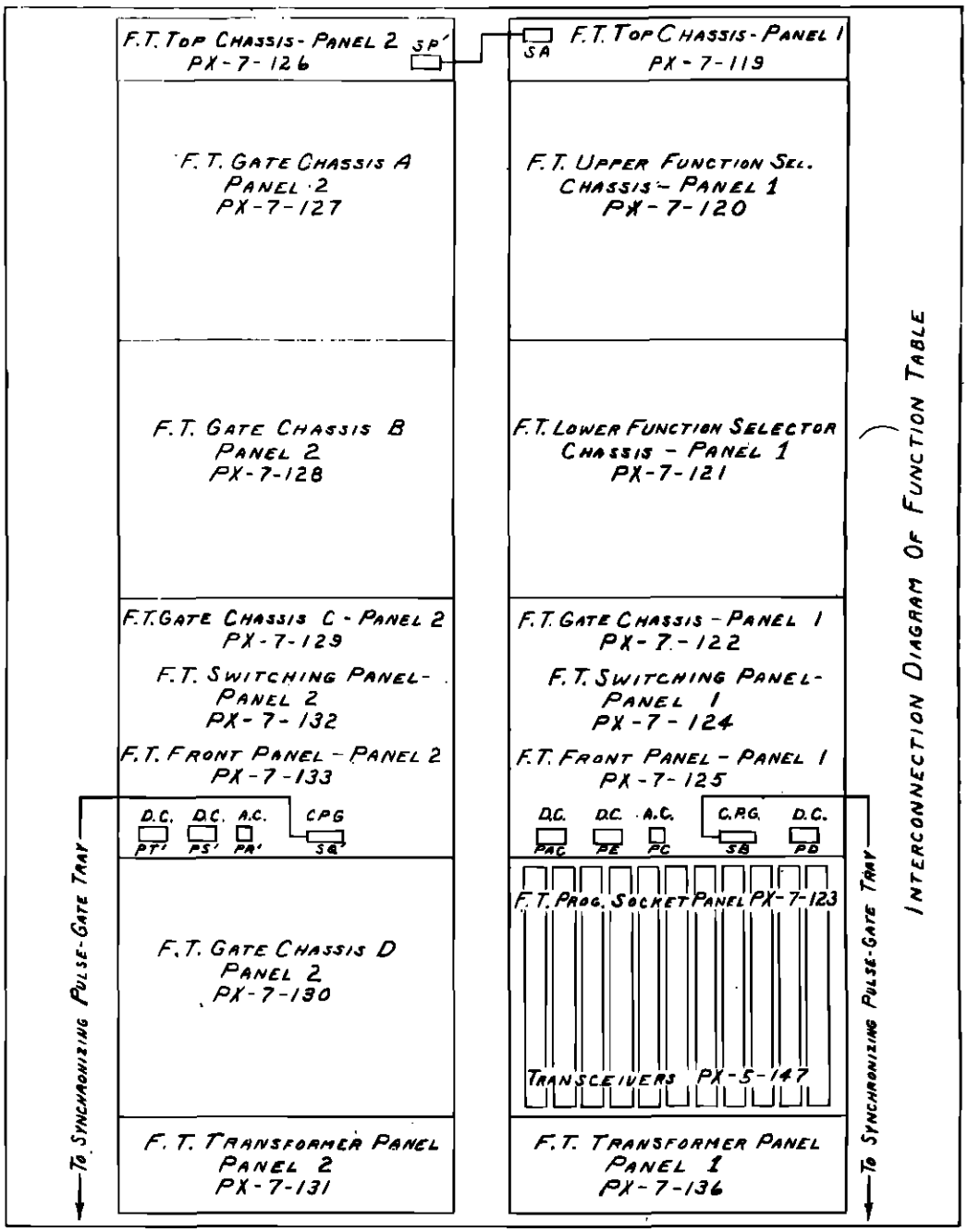
h. Combination of f. and g. - check 807 selector tube at intersection of defective row and column.

i. No number transmitted on a given digit channel - check tubes corresponding to that digit which appear in block marked "table controlled digit output channel" or "master switch and constant transmitter" on drawing PX-7-118. If PM channel is defective, check corresponding tubes.

j. Failure of a given figure to be transmitted on any channel - check corresponding tubes on panel 2 (see block marked "output gates and driver circuits" on drawing PX-7-118).

k. Spurious transmission on a given digit channel - check corresponding output gate inverters and output gates.

REVISIONS	
GENERAL REVISIONS.	
SEMI-FINAL REVISION.	
R.T. Shaw 6-27-45	1



MOORE SCHOOL OF ELECTRICAL ENGINEERING UNIVERSITY OF PENNSYLVANIA			
FUNCTION TABLE INTERCONNECTION DIAGRAM			
Drawn by: CJMcC JAN. 8, 1945	Checked by: RDJ 9 June 45	Approved by: RDJ 27 June 45	PX-7-301
MATERIAL	FINISH		SCALE

VIII. CONSTANT TRANSMITTER AND IBM READER

8.1 Circuits of the Constant Transmitter

The following tables give the drawings pertinent to maintaining the constant transmitter. PX-11-301 shows the location of the various plug-in units and chasses.

Table 8.1

PLUG-IN UNITS

Number Used	Name	Wiring	Test Charts
30	Transceivers	PX-5-147	PX-5-129
2	Pulse Boosters	PX-11-115	PX-11-125

8.2 Operation Test

An operation test is described in section 2.6 of the operating manual. The actual test cards (with nines punches) should be used here since (due to the "1", "2", "2'", and "4" channels) the constant transmitter may operate correctly with certain numbers but not others.

The various program controls can be checked by repeating the above test and successively using different program controls.

Note that the PM circuits of groups J_{LR} and K_{LR} were originally wired so as to provide the correct pulse automatically. This would mean that negative numbers would be set up as complements with respect to 10^n-1. The various manuals instruct the operator to set up negative numbers as complements with respect to 10^n. This means that the tubes A'29, A'30, A'70

Table 8.2

CHASSES AND RELAY CIRCUITS

Name	Position		Wiring	Static Test Charts	Dynamic Test Charts
	Panel	Tubes			
Top	1	1 and 2	PX-11-101A	PX-11-121	PX-11-122
Gate	1	41 - 60	PX-11-104		
Top	2	1 and 2	PX-11-101B		
Gate A	2	10 - 20	PX-11-108		
Gate B	2	21 - 40	PX-11-109	PX-11-123	See note below
Gate C	2	41 - 60	PX-11-110		
Gate D	2	61 - 80	PX-11-111		
Relay Strip	3		PX-11-118		

Note that there is no dynamic test chart for panel two. These circuits, being relay controlled, operate too slowly to be observed on an oscilloscope.

A'71
and should be removed from the constant transmitter. Note that these tubes are shown on the wiring diagrams but not on the block diagram, PX-11-307.

8.3 Possible Failures in Constant Transmitter

Possible faults, their probable causes and cures, are listed below.

a. Failure to transmit anything on one digit channel, regardless of group used - check corresponding column of tubes on gate chassis of panel 1 (see cross-section).

b. Erroneous transmission of one digit in a particular group - check corresponding matrix gate on panel 2.

c. Erroneous transmission of one digit in several groups - check corresponding pulse gate inverters on panel 2.

8.4 The IBM Reader

If the operation test shows failures which are not caused by tube failures such as indicated above (section 8.3) then the relay circuits should be checked.

A crank can be used to slowly turn the reader through a card cycle and someone can watch the coding relays CC_1 to C_8 on the schematic diagram on PX-11-116) and the digit relays (see PX-11-309).

If all these relays operate properly but the constant transmitter does not transmit the proper number then the gate chasses should be rechecked, and perhaps a static test (using the static test chart) is indicated.

If the coding relays do not operate properly check the coding cams in the reader (or call an IBM service man to do this).

Also check the IBM reader plug-board for a loose connection in case of failure in one channel.

For general failures in the IBM reader call the IBM service man. In all such cases it is the responsibility of the maintenance personnel to definitely locate the failure as being in the IBM reader proper.

REVISIONS

SOCKETS ON PX-11-101A & B CORRECTED; ALSO PLUGS ON PX-11-109 & PX-11-109.

SEMI-FINAL REVISION	1
H Gaul 6/22/1945	

MOORE SCHOOL OF ELECTRICAL ENGINEERING
UNIVERSITY OF PENNSYLVANIA

CONSTANT TRANSMITTER INTERCONNECTION DIAGRAM

Drawn by:	Checked by:	Approved by:
CJMcC Jan. 4, 1945	9 Jan 44	

MATERIAL / FINISH / SCALE /

PX-11-301

IX. THE PRINTER AND IBM PUNCH

9.1 Circuits of the Printer

The printer contains no plug-in units. The gate chasses and relay circuits are listed in the following table.

Table 9.1

PRINTER CIRCUITS

Name	Position		Wiring	Test Charts
	Panel	Tubes		
Gate A	2	3 - 20	PX-12-104	Static: PX-12-111
Gate B	2	21 - 40	PX-12-105	
Gate C	2	41 - 60	PX-12-106	
Gate D	2	61 - 80	PX-12-107	
Relay Strip	1 and 3	1 - 80	PX-12-103	
IBM Punch			PX-12-112	

9.2 Test Procedure for the Printer

Inspection of PX-12-307 shows that the printer contains a tube for each digit in each column of the card besides the PM circuits. This means that any systematic check of the printer must involve the transmission of all possible digits to all the accumulators (or master programmer) from which printing is done and a card printed after each transmission. Since it is not advisable to punch the same number in all columns of a card a testing sequence similar to the following is suggested.

Cards should be prepared as follows. In some ten digit group, say corresponding to A_{LR}, in the constant transmitter, the following numbers

should be punched.

(1) P 0123456789
(2) P 1234567890
(3) P 2345678901
. . . . . .
(10) P 9012345678
(11) M 0123456789

These cards are then placed in the IBM reader and the programming arranged as follows:

1) IBM reader reads the first card.

2) The numbers of A_{LR} are transmitted to all accumulators which participate in the printing. It is also suggested that at each card reading one's be transmitted into all decades of the master programmer which participate in the printing.

3) The printer prints the number in the accumulators and the master programmer.

4) The accumulators are selective cleared.

5) The process repeats until all the cards have been read.

Note, that if, due to the type of problem on the ENIAC, it is inconvenient to selective clear all the accumulators involved, the cards for the reader may be prepared as follows.

(1) P 01234 56789
(2) P 11111 11101
(3) P 11111 11011
(4) P 11111 10111
. . . . . .
(10) P 01111 11111
(11) P 11111 11111

The cards punched in the above test may be compared visually or they may be compared with a standard set in the reproducing punch.

9.3 Types of Failure and Remedy

1) Failure of motor generator on punch

   a) Check a-c power supply.

   b) Check interconnection to ENIAC.

2) Failure of punch to operate when programmed.

   a) Card magazine empty.

   b) Card hopper full.

   c) Failure of starting circuits in initiating unit. (see Chapter II).

   d) Failure of starting relay in printer (PX-12-103).

   e) Failure of punch starting circuits (PX-12-112).

3) Punch continues to operate.

   a) Starting circuits in initiating unit (see Chapter II).

   b) Check reset cam in punch (PX-12-112).

4) Punch operates but fails to feed a card.

   a) Check condition of bottom card in magazine.

   b) Possible mechanical failure in feed mechanism. Call IBM service department.

5) Punch fails to punch card.

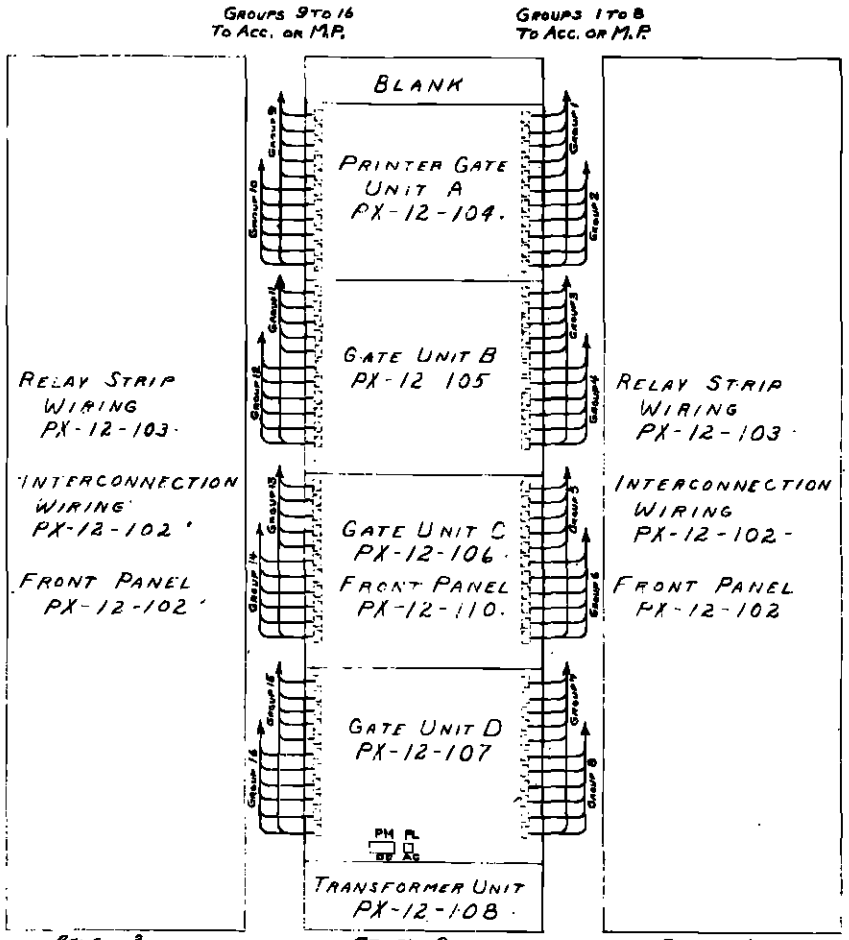
   a) Inspect digit relays (PX-12-103) back of panels No. 1 or No. 3 to see if these pick-up. If these pick-up and card is not punched then failure is in IBM punch or interconnection cable. If these fail to pick-up then check starting relay (PX-12-103) and interlock cam. If these

pick-up but fail to hold check holding cam.

6) Fails to punch in a particular column. Check the corresponding tube, relay, or jumper connection on plug-board. (See PX-12-104 to 107, PX-12-103, PX-12-305.)

7) Multiple punches in some columns. Check against multiple program pulses circulating in the ENIAC. Check tubes in the associated columns.

8) Intermittent extraneous punchings. Check associated relays for spring tension. Vibration may cause the relay to gradually pick up.



INTERCONNECTION DIAGRAM OF PRINTER

GROUPED STATIC INPUT CABLES TO PRINTER ADDED
J. Cummings 5-21-45 | 1

MOORE SCHOOL OF ELECTRICAL ENGINEERING UNIVERSITY OF PENNSYLVANIA			
PRINTER INTERCONNECTION DIAGRAM			
MATERIAL	FINISH	SCALE	
/	/	/	
Drawn by: CJMcC APRIL 6, 1945	Checked by: J. Cummings 4-9-45	Approved by:	PX-12-304

X. MASTER PROGRAMMER

10.1 Circuits of the Master Programmer

Note that 10 of the master programmer transmitters are located on the cycling unit, see PX-1-301. The following tables give a list of the plug-in units and chassis circuits of the master programmer.

Table 10.1

PLUG-IN UNITS

Number of Units	Name	Wiring	Test Charts
20	Decade	PX-8-101	PX-8-125
10	Program	PX-8-103	PX-8-123
10	Pulse Former and Carry-over	PX-8-104	PX-8-124
20	Transmitter	PX-8-105	PX-8-122
10	Stepper	PX-8-112	PX-8-126

Table 10.2

CHASSES CIRCUITS

Name	Position		Wiring	Test Charts
	Panel*	Tubes		
Gate	1 and 2	41 - 60	PX-8-106	Static: PX-8-120A PX-8-120B PX-8-118 Dynamic: PX-8-121

*Note that the two panels of the master programmer are identical in their functions. Thus the gate chasses are identical on the two panels. However, the plug-in units are not arranged the same, some being on the cycling unit panel.

10.2 Operation Tests

Most tests can be made using only the initiating pulse.

a. Initially clear. Feed initiating pulse into each decade direct input in turn. Decades should step once for each pulse. If next decade to the left is coupled to the one being pulsed, it should step once each time decade being pulsed goes from 9 to 0. When decades associated in a group register number set on top row of decade switches, they should clear on next pulse.

b. Make some test on steppers, using stepper direct input. Check operation of stepper clear switch by setting to various positions; stepper should count up to position corresponding to switch setting and then clear back. Since clearing is done by CPP only 1 add time after coincidence, it appears to be caused by pulse which puts decades into final position.

c. Check stepper direct clear input by first running stepper up to some stage other than first, as in (b), and then pulsing stepper direct clear input. This should clear stepper.

d. Check overall operation of each stepper by feeding pulses to regular program input. Decades associated with program in use should register each pulse, and after a number of pulses equal to number set on top decade switches, decades should clear and stepper move up. Similar action should take place for each of the six stepper stages and each of the six corresponding sets of decade switches.

e. To check outputs, use same procedure as in d., and feed output to another program input. Output pulses, one for each input pulse,

should be obtained as long as stepper is on stage corresponding to output being used; when stepper moves up, pulses should be obtained from next output, etc.

f. If it is desired to check operation at normal speed, a continuous program can be set up using two selective clear transceivers, feeding output of each into input of the other, and use this series of pulses in tests d. and e. above. Outputs may, if desired, be observed on oscilloscope.

10.3 Trouble Shooting

Several possible faults are listed below, together with their probable causes and cures.

a. Decade or stepper fails to cycle and will not clear to first or zero stage - replace decade or stepper.

b. Decade clears but does not cycle - replace pulse former - carry-over unit.

c. Decades initially clear but fail to clear on reaching coincidence with switch settings - check coincidence gates, parallel gates, stepper output inverters; if none of these are at fault replace program plug-in unit.

XI. A.C. EQUIPMENT AND POWER SUPPLIES

11.1 Introduction

This chapter covers the following topics:

1) A.C. power and control system.

2) Starting sequence.

3) Power supplies, bleeder, and condensers.

4) Common failures.

5) Ventilating system maintenance.

11.2 A.C. Power and Control System

The complete diagram for the power and control wiring is shown on drawing PX-1-101. The rack from which the A.C. power is distributed to the ENIAC heaters, to the fans and to the power supplies is shown on PX-1-304. Simplified wiring diagrams of the power system and control circuits are shown on the following:

PX-1-303	Power System Block Diagram
PX-9-307	Cycling Unit and Initiating Unit Block Diagram.

11.2.1 Fuses

Fuse sizes are shown on the drawings as follows:

A.C. Main Fuses	PX-1-101
Power Supply Heater Fuses	PX-13-111
Power Supply Plate Fuses	PX-13-111
D.C. Circuit Fuses	PX-13-102

These d-c circuits and the power supply heater circuits use Western Electric alarm type fuses in the following sizes: 1/4 amp, 1/2 amp, 1 1/3 amp, 2 amp, 3 amp, and 5 amp. In certain cases (those marked 5S on PX-13-102) the 5 regular ampere fuse was found to be inadequate. Western Electric Company does not manufacture these fuses in larger than 5 ampere rating. The 5S fuse is made by refilling a 5 amp. Western Electric fuse (catalog No. 35H)with a new link of Advance alloy round wire, 0.0126 inches in diameter.

11.3 Starting Sequence

Drawing PX-1-112 is a chart designed to aid in locating troubles in the main power sources which may develop during either the starting operations, or during running operation but affecting the main power sources or auxiliaries (fans).

In using the chart it should be remembered that since each step is dependant on the previous step, the point at which the sequence fails should be determined so that possible troubles beyond that point need not be investigated.

When trying to locate trouble which has turned the entire machine off certain safety switches on the a-c distribution panel should be opened. This prevents any testing (by going through portions of the starting sequence) from subjecting the tubes to numerous heating and cooling cycles (which would increase the probability of failure of the tubes). If this is done certain protective relay circuits may be shunted for testing purposes without endangering the ENIAC. Furthermore, the control wiring, contactor and relay adjustment, and entire starting sequence may then be tested without turning the main power on provided the under-voltage release and phase failure relays are shunted.

11.4 Power Supplies, Bleeders, and Condensers.

The following drawings show the wiring from the a-c sources shown on PX-1-101 through the power supplies to the point where the d-c terminates at each unit as noted.

11.4.1 Supplies

PX-13-104	Standard Power Supply Wiring Diagram
PX-13-108	Power Supply and Wiring Diagram

11.4.2 Bleeders

PX-13-106	Power Supply to Bleeders Interconnections
PX-13-112	Bleeder Wiring Diagram
PX-13-102	D-C Voltage Chart (shows bleeder to d-c panel connections)

11.4.3 Condensers

PX-13-102	D-C Voltage Chart (shows d-c panel to condenser connections)
PX-13-109	Power Supply Condenser Wiring Diagram

11.5 Common Failures

11.5.1 D-C Undervoltage

If, after attempting to turn the d-c on by depressing the d-c start button, the d-c trips off at the end of the 10 second initial clearing period, usually the trouble is caused by an undervoltage from one of the 28 power supplies (undervoltage in supply Z will not trip d-c). Proper procedure to locate trouble is as follows:

1. Turn d-c on again by d-c start button and check power supply fuses by observing neon lamps in top of d-c fuse cabinet.
2. If 1. does not detect the trouble, place a jumper across the series stop circuit which runs through the undervoltage relays

(relays are located in one of the by-passing condenser cabinets). Turn d-c on again and note which relay fails to hold when pick-up relays drop out. Caution: 1500 volts d-c potential on some relay contacts. Check corresponding power supply for a tube with a faulty heater. Caution: After replacing a power supply tube allow 1 minute warm-up time before turning d-c on.

3. If no tubes are faulty check line fuses in power supply fuse panel, by removing pull-out block, and testing with an ohm-meter, or some other continuity checking device.

4. Do Not forget to remove jumper across undervoltage relays.

11.5.2 D-C Fuse Failures

Quite frequently the operator forgets to set the operation switch on "Continuous" before turning on the d-c. This will result in the blowing of a d-c fuse.

Locating a blown d-c alarm fuse is usually not difficult, for these fuses have indicators which stand out when the fuse has blown. Occasionally, however, the fuse wire may stretch, but not break (if it is operating near its rating) permitting the alarm contact to close and tripping the d-c off. In such cases, a persistant and close inspection may be required to locate the offending fuse. The correct sizes of fuses are shown on drawing PX-13-102.

Under certain conditions, on turning on the d-c the machine will trip off before completion of the 10 second period due to blowing a d-c fuse. The blown fuse may be caused by an undervoltage in one of the d-c supplies, and it is suggested that this possibility be investigated before assuming that the trouble is in one of the ENIAC units.

Control Circuit Voltage		Relay or Contactor	Location of Relay or Contactor	Picked-Up By Closing Of	Held Thru These Contacts in Series	Possible Cause of Operation or Failure (3)	Location of Hold Contacts	Remarks
(4)	(4)	A	Machinery Lab. Box of Contactor B.	Start Push Button on Initiating Unit Front Panel See PX-9-302	B_1		Mach. Lab. - Cont'r B Box	
	220	Auxiliary Relay			P_1	Door Open & Shunt Switch Not Pushed Thermostat Operation - See Relay C Below.	A.C. Distribution Rack See PX-1-304	
					Stop Push Button		Init. Unit - See PX-9-302	
	220	B - ENIAC Main Heaters Cont'r	Machinery Lab.	A_1	A_1		In Machinery Lab. Box of Contactor B	
					B_1			
	220	E. Fan Cont'r.	A.C. Distribution Rack	A_3	A_3		do	
110		Amber Pilot Lt.	Initiating Unit	A_4	A_4		do	
	220	D. Power Supplies Heaters Cont'r	A.C. Distribution Rack	E_1	Q_1	Power Supply Heater Fuse Failure - See Q Below	A.C. Distribution Rack	
					E_1			
110		F 2 Minute Timer	do	D_1	ENIAC & P.S. Heater Phase Failure Relays (1)	Fuse Blowing or Failure of One or More Phases of Power Source	do	(1) These Relays Are Adjusted To Hold Without Chattering And To Drop Out On Reduction To 60% of Rated Voltage
					D_1			
					F_1			(2) Will Trip D.C. Off At End of 10 Sec. Initial Clearing Period.
	220	G Power Supply Plate Contactor	Machinery Lab	F_1	L_1	Pressing D.C. Stop Button Blowing of D.C. Alarm Fuse Phase or Main Fuse Failure of Power Source Under-Voltage of One or More of 280 D.C. Power Supplies (2) Phase or Main Fuse Failure in Power Supply Plate Circuit (2)	do	
	220	H - Initial Clear Relay	A.C. Distribution Rack	G_1	G_1		In Machinery Lab. Box of Cont'r. G.	The Initial Clear Relay Drops Out When K_4 Opens At End of 10 Second Period of J Timer.
					K_4			
	220	J - 10 Sec Timer	do	G_1	K_4		do	
	220	M - U.V. Pick Up	By Pos. Condenser Cab't	G_1	K_4		do	
	220	K - Auxiliary Relay	Machinery Lab Box of Cont'r G.	J_1	G_1		do	Pressing Initial Clear Push Button Causes Green Pilot To Go Off For 10 Seconds While M, J, M & K Recycle
					K_1		do	
					Initial Clear Push Button		Initiating Unit	
110		Green Pilot	Initiating Unit	K_3	K_3	Initial Clearing Any Relay in Cabinet, D.C. To Be Off - See G Above	Machinery Lab Box of Cont'r G	
110		C Blower Relay	A.C. Distribution Rack	Normally Picked Up	46 Door Switches	Door Removal or Switch Out of Adjustment	Top of Door En Unit	Temporarily Shunted
					43 Thermostats	Overheating Caused By: 1 - Dirty Filters, 2 Damper in Duct Closed, 3 Inlet Dampers Closed, 4 Fan Stoppage	In Duct Work Above Each Unit	(3) C Introduces A Delay Which May Be Set Up To 15 Min. To Permit Time To Correct A Fault (Such As A Blown Fan Fuse) Before Machine Trips Off
110		P - Blower Emergency Timer	do	C_1	C_1	See Reasons For C Above	A.C. Distribution Rack	
110		L D.C. Cut-Off Relay	do	D.C. Stop Push Button D.C. Alarm Fuse Relays N_1	D.C. Start Push Button L_2	See Reasons For L, Opposite G Above	do	Relay Is Not Normally Picked Up. D.C. Alarm Fuse Relays Are Located In A Box Beside A.C. Fuse Panel.
110		Q Power Supply Cut-Off Relay	do	P.S. Heater Blown Fuse Relays	Q_2	Power Supplies Heaters Alarm Fuse Failure	do	All P.S. Htr. Power Is Automatically Turned Off To Permit Safe Replacement of Fuse - Use of Safety Switch Also Recommended.
					D.C. Start Push Button			
110		N Auxiliary Relay	do	Normally Picked-Up	K_1		Machinery Lab.	
					D.C. Under Voltage Relays (1)	Circuit Fuse Blown or Tube Failure	Condenser Cab't	
					P.S. Phase Failure Relays (1)	Power Failure or Main Plate Fuse Blown	A.C. Distribution Rack	

(3) Such Causes As Open Circuit Due To Broken Wires, Dirty or Pitted Contacts, Loose Screw Connections Are Obvious, And Will Not Be Mentioned.

(4) Failure of 220 Volt Control Fuses (Located In Contactor B Box In Machinery Lab.) Will Cause Machine To Stop. Failure Of 110 V. Control Fuse Turns Off D.C. Alarm & Green Pilot Lights.

(5) Dropping Out of C Relay Is Indicated By A Bell And Light - See PX-1-304.

(6) D.C. Under Voltage Relays Are Adjusted To Drop Out When Voltage Across Holding Resistor Drops To 90% of Rated Value.

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MAINTENANCE CHART
ENIAC STARTING SEQUENCE

SCALE. —			
DRAWN BY	CHECKED BY	APPROVED BY	
J. Cummings 4-8-46	J.K. Adams 5-6-46		PX-1-112

11.5.3 D-C Undervoltage Release Relays

PX-13-113 shows the connections and arrangement of these relays which are located in the by passing condenser cabinet and connected to the d-c at that point.

11.5.4 D-C Panel to ENIAC Units

PX-13-102	D-C Voltage Chart
PX-13-107	Chart for D-C Wiring in Power Trough. This chart will aid in determining what voltage appears on each terminal of the blocks located in the power wiring trough.
PX-13-115 A and B	D-C Wiring in Power Trough. These drawings enable one to trace each voltage from the panel to the various terminal blocks at the ENIAC units on which it appears.

11.5.5 Replacement and Design Data

PX-13-103	Power Supply Drains
PX-13-104	Standard Power Supply Wiring Diagram
PX-13-108	Power Supply Z Wiring Diagram
PX-13-109	Power Supply Condenser Wiring Diagram
PX-13-110	Measurements on Chokes
PX-13-111	Power Supply Data Chart
PX-13-112	Bleeder Wiring Diagram
PX-13-114	Power Supply Specifications
PX-13-116	Power Supply Replacement Part Test Data.

11.6 Ventilation System

11.6.1 Fans

The fans used in ventilating the ENIAC are American Blower Utility Sets No. 250C.

1. Speed Adjustment.

Each fan unit is equipped with adjustable motor sheaves. The speed of these units may be increased by adjusting the motor sheave until the desired air delivery is obtained. To increase the fan speed (correct speed is 770 RPM) the movable flange of the motor sheave must be turned toward the fixed flange. An Allen wrench is provided to loosen the set-screw locking the flange. After the flange has been turned the required amount, the setscrew should be tightened locking the flange in place. Caution: The flange must be in such a position that the locking screw rests on the flats and not on the threaded protion of the hub. If necessary, the bolts should be adjusted as described below. All set screws should be carefully checked and tightened at least four times per year.

2. V-Belt Drives

Belt tension should be just sufficient to eliminate excessive sag on the slack side. To adjust the belt tension loosen the bolts holding the motor mounting plate to the vibration dampeners. The mounting plate may then be moved vertically up or down to the desired position and the bolts tightened. On unit, Model No. 250C, the motor may readily be moved horizontally for minor belt adjustments.

To replace belts, remove the belts from the sheaves, then remove the bolts from the ends of the bearing support, tilt the bearing support member until belts can be removed and the replacement made over the ends of

the support member. Belts may also be replaced by removing bearing cap and pulling belts through the shaft hole in bearing support.

The following are typical V-Belts to be used for replacing belts which may become worn or may break: Dayton A38, Thermoid No. 1400, Browning VRA-FHP-138.

3. Motor Bearings

The fan motors are provided with ball bearings. Ball bearings are filled with grease before leaving the factory. This grease should be replenished each six months.

Grease should be applied to the bearing from tubes which may be obtained from the Fafnir Bearing Co. or local ball bearing distributors. High pressure grease guns force too much grease into the bearings and through seals and therefore should not be used. Use only grease having the following general specifications:

1. Consistency a little stiffer than vaseline maintained with minimum change over ambient temperatures encountered.
2. Melting point preferably above 150° C.
3. Freedom from separation of oil and soap under operating and storage conditions.
4. Freedom from abrasive matter, acid and alkali.

The following greases or equivalents are recommended: Keystone 44, Master M31, Alemite 38.

4. Fan Bearings

Fans are equipped with self aligning sleeve bearings of the bronze bushing type. The oil is distributed by means of graphite packed oil grooves. Do not remove this graphite. Do not insert any piping or pipe fittings

between oil cup and bearing. Fill the bearing with a good grade of mineral oil of SAE viscosity No. 40. To fill the oil reservoir of fan bearings, place nozzle of oil can in the bottom of the oil cup, forcing in the oil until the reservoir and cup are full. For room temperature 100° F or above, use SAE No. 50 or 60. This type and grade oil is the same as used in automobile motors. Inspect bearings at least once every 30 days.

5. Failure

Should a single fan stop, this will probably be caused by a fuse blowing in the fan circuit. These fuses are located in the fan panel - see drawing PX-1-304. The fuses used to protect the fans from overloads are special, but readily available. These fuses are Bussman Manufacturing Company's 6.25 amp 230 Volt Cartridge Type Fusetrons. Only fuses having a thermal time delay characteiristic and rated at 6.25 amperes should be used for these fans. Otherwise all motor protection (danger of burning-out windings) is lost. Another acceptable fuse is Shawmut Manufacturing Company's "Thermatrip".

Should these fuses blow a second time after having just been replaced, the motor should be inspected for causes of overload such as lack of oiling, worn bearings, tight belts, etc., and for grounds.

All fans stopping at once may be caused by a failure of the fan source of power caused by fuse operation, or manual opening of one of the circuit safety switches located on the a-c distribution rack and in back of the machinery laboratory switchboard. Fan power is unregulated and is separate from ENIAC power - see PX-1-101.

11.6.2 Air Filters

The air filters used in the doors at the rear of the ENIAC are "Dustop" air filters as manufactured by the Owens-Corning Fiberglas Corp. Similar filters by other manufacturers may be used but care should be taken to select a filter which uses a fireproof adhesive similar to the Lindall adhesive used by Owens-Corning Fiberglas Corporation.

Two sizes of filters are used: 10" x 20" x 2", and 20" x 20" x 2", two of the former being used only in those places where one 20" x 20" x 2" cannot be conveniently installed, i.e., in the bottom inlet on the two inlet doors, and in the two bottom inlets on the three inlet doors.

In the Moore School installation the 20" x 20" x 2" filters are also used in the fresh air inlet chamber.

The frequency of changing the filters depends on prevailing dust conditions and can best be determined by examination and experience. An indication of the filter's condition can be obtained by the temperature guages in the ducts above each unit. With new filters, the temperature rise in each unit will be approximately 11° F above room ambient. Should a considerably larger rise occur, and visual examination of the filter indicates that they are quite dirty, they should be changed.

11.6.3 Door-of-Unit Dampers

These dampers are those which adjust the flow of air through the above mentioned air filters. Tests have proven that for uniform temperature to exist within the cabinets, 75 % of the air should enter through the lower intake, and 25 % through the upper. The dampers should be adjusted accordingly, with the fins of the dampers so adjusted as to drive the incoming air toward the bottom of the cabinet. All fins of any one damper

should assume the same angle so as to insure the uniformity of the filter's dust collection.

11.6.4 Recirculating Dampers

The ventilating ducts are arranged with automatic dampers which tend to keep the ENIAC room at the temperature set on the controlling thermostats (the two thermostats which are set on the building wall behind accumulators 9 and 15). The dampers are so arranged that when the room temperature rises above thermostat setting, more air will be exhausted to the outside and less into the room and vice versa.

The wiring diagram for this system is shown on drawing PX-1-101. The manufacturer's (Minneapolis-Honeywell Regulator Co.) catalog numbers are also given on this drawing. In the diagram shown it may have been necessary to interchange the B and W wires to obtain proper operation. The location of the damper motor circuit fuses is shown on drawing PX-1-304.

11.6.5 Service Required by Recirculating Damper Motors

Inasmuch as all moving parts of the damper motor are immersed in oil, periodic lubrication is not necessary. The cover should be left on the motor at all times to protect the motor from dust and mechanical injury.

It should be noted that the balancing relay armature is adjusted to "make" contact on one side when the relay is de-energized.

All set screws on the motor-to-damper linkages should be checked once each month.

Listed below are causes and effects of certain conditions which may exist in the control circuit.

1. Broken red wire or blue wire in control circuit: Motor will run to the closed position and stay there.

2. Broken white wire in control circuit: Motor will run to the open position and stay there.

3. Loose or dirty contact on control potentiometer: Motor will run to the close position when the wiper on the control potentiometer is at a position where a poor contact is established.

4. Insufficient voltage: The sensitivity of the control circuit will be reduced, and the power of the motor will be materially lessened by a voltage drop.

11.6.6 Room Thermostats

Setting of Room Thermostats. T-92A - Turn temperature setting screw on top of thermostat until indicator points to the desired average room temperature on the scale.

Adjustment of Room Thermostats. Factory calibration - All thermostats are carefully calibrated at the factory and no attempt should be made to change any adjustment other than those mentioned under "Setting" unless the thermostat is found to be out of calibration after being in actual operation for several hours.

Thermostats with non-adjustable differentials (T92A) are calibrated so that the sliding contact is at the center of the potentiometer coil when the room temperature is equal to the setting of the indicator.

Care must be exercised in checking the adjustment of these thermostats since heat from the potentiometer coil affects the thermostat calibration and the reading of the cover thermometer (if used) to the extent of about 3°. The thermostat should therefore not be checked until it has been in operation with the power on and with the cover in place for at least

an hour. To check the adjustment, (this should be done as quickly as possible, before the heat from the potentiometer can be dissipated, and to prevent heat from your hands or breath from affecting the calibration) remove the cover and set the indicator to the room temperature as indicated on the cover thermometer or other reliable thermometer placed near the thermostat. Then observe whether the sliding contact is in the proper position (see preceding paragraph). If it is not, turn calibration screw (on bottom of thermostat) to the right or left as necessary to correct the adjustment (turn to the right to move slider to the right). Each 1 1/2 turns is equal to approximately 1°.

11.6.7 Thermostats for ENIAC Protection

These temperature controllers are of Minneapolis-Honeywell Regulator Company's manufacture and are rated as follows:

Remote Bulb Controller

Catalog No. T-615A

Range +65° to 140° F

5 ft. Tubing with Bulb

Method of Setting and of Adjusting

1. Turn adjusting screw at top of box until the indicator on the outside of the case is opposite the desired "cut-out" temperature. "R to W" contacts make on temperature rise - "R to B" makes on temperature fall. Scale divisions are marked numerically. Each Farenheit division (on the left) equals 10° and each Centigrade division (on the right) equals 5°. The notations "L" and "H" represent the low and high end of the scale range.

2. On T615A Controller, the differential between cut-in and cut-out temperatures may be increased by turning adjusting screw to the

right, which raises the indicator from "A" toward "H" on the differential scale. The equivalent number of degrees for each division from A to H varies with each scale range and with the point at which the indicator on the main scale is set. The approximate values however are as follows: If the main scale indicator is set near the low end (65° F) each division from "A" to "H" equals approximately 3 2/7°, at the high end each division equals approximately 1 3/7°.

For direct acting controls, the cut-in temperature plus the differential equals the cut-out temperature, and for reverse acting controls, the cut-out temperature plus the differential equals the cut-in temperature.

Mercury Switch Adjustment: If the operating differential of the controller is considerably smaller than that for which the indicator is set, the mercury switch may be out of adjustment. This sometimes occurs when a broken switch is replaced. Before making any adjustments, however, be sure that the difficulty is not due to the controller being "off level." Note the level indicator.

The adjustment may be checked as follows: Set the differential indicator approximately at mid-scale, and the temperature indicator so that the operating lever rests lightly against its upper stop. Press down on the left hand end of the operating lever until it is about midway between its upper and lower stops and just touches the differential lever. This movement should not cause the mercury to change ends in the switch. Further downward pressure on the operating lever will force it to the lower stop carrying the differential lever with it and will cause the switch to tilt and shift the mercury. Now, allow the operating lever to slowly return to midway between stops and note that the mercury should not shift

its position. Allow the operating lever to return to its upper stop and the switch should tilt back to its original starting position.

If the switch does not operate in this manner, turn the eccentric screw slightly to the right or left as necessary and re-check as outlined above.

To Replace Mercury Switch: Note that the arrangement of the contacts and flexible leads and make sure that they are in proper position when the new switch is in place. Use the point of a knife to pry the switch clip loose from the mercury switch - never attempt to break it loose with your fingers. Wrap two layers of friction tape around the switch to take the place of the ambroid cement before placing the switch in the clip. Check the adjustment as outlined above.

Correct Temperature Setting of Thermostats

The correct cut-out temperature is 120° F, for the ENIAC units. The ventilating system was designed to permit approximately 11° rise over ambient temperature with new air filters. This would permit satisfactory operation on days during which the ambient temperature was 100° F allowing a safety margin.

The equipment in the power supply and bleeder cabinets will not be endangered if the temperature rises 20° F, and so the thermostats may be set up to 130° F if found necessary.

The absolute maximum temperature to which any of the ventilated equipment can be safely subjected is 180° F, including the thermostat bulb and due consideration being given to the possibility of "hot-spots" it is felt that the aforementioned settings are reasonable.

12.1 List of Test Equipment

Item	Drawing	Quantity	Remarks
Bench	PX-2-120 2-121 2-111 2-112 2-113 2-114	1	2-111 signal wiring, 2-112 power wiring, 113 switch panel, 114 fuse and by-passing, 120 transformer, 121 tube panel.
Power Supplies	PX-2-102 2-103 2-104	1	6 supplies PX-2-102 2 supplies PX-2-103 1 bleeder PX-2-104
Synchronizing Unit	PX-2-115 2-108	1	Front Panel PX-2-115 Wiring Diagram PX-2-108
Synchronizing Unit Supply	PX-2-107	1	
Test Oscilloscope	PX-2-110	1	Includes probe with 4 detachable ends. Connects to Synchronizing unit by cable.
Test Oscillator	PX-2-117	1	Connects to synchronizing unit by 1 conductor cable.
Variable Power Supply	PX-2-118	1	Connects to bench by four conductor cable.
HiPot Supply	PX-2-119	1	
Tube Tester	PX-2-116	1	
Voltohmist Jr.		1	
Simpson Meter		1	
12 Conductor Shielded Cable		2	Connects only into sockets marked "S".
12 Conductor Non-Shielded Cable		5	3 connect synchronizing unit to its supply.
4 Conductor Connection Cable		2	1 connects variable supply to bench.
2 Conductor Connection Cable		1	Connects synchronizing supply to AC
12 to 10 Conductor Special Cable		1	To connect pulse amplifier to bench
Load Box with 220 Ω resistors	PX-4-103	1	For output load on pulse amplifier.

12.1 List of Test Equipment (cont'd)

Item	Drawing	Quantity	Remarks
Tube Circuit Plug-in Tester		2	
Plug-in Unit Pullers		2	For use in removing units from ENIAC.
Current Flow Test Set		1	Used to adjust relay- consists of tool box and contents.
Static Tester	PX-2-109	1	For use with static test charts for ENIAC panel.
Book of Photostats of Wiring and Test Drawings		1	Plug-in unit drawings.
Service Logs		3	1 for ENIAC, 2 for units.
Push Switch and Cord		1	For manual pulse devices.
Screwdriver		1	
Diagonal Cutters		1	
Long Nose Pliers		1	
Soldering Iron		1	
Variable Power Supply Adaptor		1	For connecting variable power supply to Multiplier, Cycling Unit, and Function Table panels.

12.2 Description and Maintenance

The following chart (Table 12.2) lists the uses of the outputs of the synchronizing unit illustrated in drawing PX-2-302 as used in testing the plug-in units as illustrated in drawing PX-2-301.

Table 12.2

Plug-in Unit	Drawing		Fixed	Scope	Variable	Train	
	Wiring	Test				+	-
PM and Clear Unit	PX-5-108	PX-5-127			Clear Tubes	Trans. Tubes	PM Counter
Acc. Decade Unit	5-133	5-126			Carry Out	Trans. Tubes	Ring
Acc. Transmitter Unit	5-147	5-129	Sets F.F.		Resets F.F., transmitter		
Acc. Receiver Unit	5-148	5-128	Sets F.F.		Resets F.F.		
Acc. Repeater Unit	5-149	5-130			Ring (if trans. used)		Ring (if no trans. used)
Mult. Buffer Unit	6-107	6-130			Drives buffers		
M.P. Decade Unit	8-101	8-125				+ and - train operate MPPF unit	
M.P. Program Unit	8-103	8-123	Sets F.F.		Resets F.F.	Drives stopper gate	
M.P. Pulse Former and Carry Over	8-104	8-124				Drives PF through inverter	Drives PF direct
M.P. Transmitter Plug-in Unit	8-105	8-122				Drives trans. gate	
M.P. Stopper Plug-in Unit	8-112	8-126					Drives ring
C.U. Transmitter Plug-in Unit	9-102A 9-102B	9-123					Drives inverters
Reader Interlock Unit	9-103	9-124	Push button sets unsyn. F.F.		Sets syn.f.f.		Resets syn. f.f.

Table 12.2 (cont'd)

Plug-in Unit	Drawing		Fixed	Scope	Variable	Train	
	Wiring	Test				+	-
Reader Printer Starting Unit	PX-9-104	PX-9-122	Push Button resets reader f.f.		Set reader and printer f.f.		Resets printer f.f.
Initiating Pulse Plug-in Unit	9-105	9-125	Push Button sets unsyn. f.f.		Sets syn. f.f. Resets both f.f. and trans. pulse		
Reader Transmitter Plug-in Unit	9-106	9-121			Sets and resets f.f.		
Cycling Unit Delay Line and Off Beat P.S. Unit	9-130	9-139					Drives Pulse Standardizer
Cycling Unit Oscillator, Manual Pulser Unit	9-131	9-140	Push Button operates Pulse former				
Cycling Unit On-beat Pulse Standardizer and Amp-Plug-in unit	9-132	9-141					Drives Pulse Standardizer and Amp.
Constant Transmitter Pulse Booster Unit	11-115	11-125		Drives Buffer			
Pulse Amplifier	4-116	4-118				Drives Input Buffers	

12.2.1 Maintenance of Test Equipment

Static and dynamic test charts are provided for the synchronizing unit and the test oscilloscope. Their numbers are PX-2-112 and PX-2-110 respectively. The variable power supply, the test oscillator, and the regulated power supplies are essentially of standard design so that maintenance can easily be provided by direct use of the wiring drawings given in the list in section 12.1. The test bench is essentially a wiring distribution socket panel similar in most respects to the socket panels of the ENIAC proper. The fusing and AC power control features are copies of similar equipment for the ENIAC. Familiarity with ENIAC maintenance in these respects provide ample background which together with the wiring diagrams appropriate to the test equipment are all that is necessary for test equipment maintenance. However, a word should be added concerning the special tube chassis in the test bench. This chassis contains a few tubes from the accumulator gate chassis, PX-5-117, essential to the coupling of transceiver and repeater plug-in units when jointly operated as desired in testing from time to time (see illustration in block diagram PX-2-301). The circuits are direct copies of the similarly named tubes on drawing PX-5-117 and no difficulty in maintaining them will be encountered if this reference is kept in mind. The static panel tester is essentially a wiring distribution panel and no particular problems should be encountered in maintaining it. Its use is described in section 12.3 below. The tube tester contains no special equipment and can best be maintained with reference to its wiring drawing. A word of caution on the tube tester, however, is that when some of its fuses blow, erratic and unusual operation may occur so that before concluding some important failure has occurred,

the fuses should be checked. The operation of the tube tester is described in the detailed instructions engraved on its panel.

12.3 Use of Test Charts

There is provided a static and dynamic test chart for each plug-in unit as listed in section 12.1 and on drawing PX-2-123, a copy of which is inside the left panel door of the test table. Also listed on PX-2-123 are the names and wiring drawing numbers of the individual plug-in units. The description on the static-dynamic test drawing for each unit describes in detail the instructions necessary for carrying on the test program in accordance with the chart in section 12.2.

For the ENIAC "gate" panels, those sections which are not removable plug-in units, there is provided static and dynamic test charts just as there are for the plug-in units themselves. A list of these charts is given in a table at the beginning of each chapter for the units of the ENIAC under the column "Test Charts". A special static tester, PX-2-109, was designed for use with these charts. By reference to drawing PX-5-109 and the "legend" and note above the panel illustration on each static test chart, full information is found for the use of the static tester.

12.4 Use of Test Equipment with ENIAC Proper

The variable test oscillator, the variable power supply, and the test oscilloscope provide conveniences in testing the ENIAC.

12.4.1 Test Oscillator

In the cycling unit panel of the ENIAC there is a socket and switch provided so that the test oscillator may replace the crystal controlled oscillator normally used in the ENIAC. By connecting the test

oscillator, the ENIAC may be operated at faster or slower speeds providing means of checking the frequency tolerance in built-in rings, and perhaps in localizing certain types of faulty operation.

12.4.2 The Variable Power Supply

By the same token, the variable power supply may be connected into function table, multiplier, and cycling unit by the use of variable power supply adaptor, PX-4-120, to provide voltage tolerance tests on built-in rings in the ENIAC.

12.4.3 Test Oscilloscope

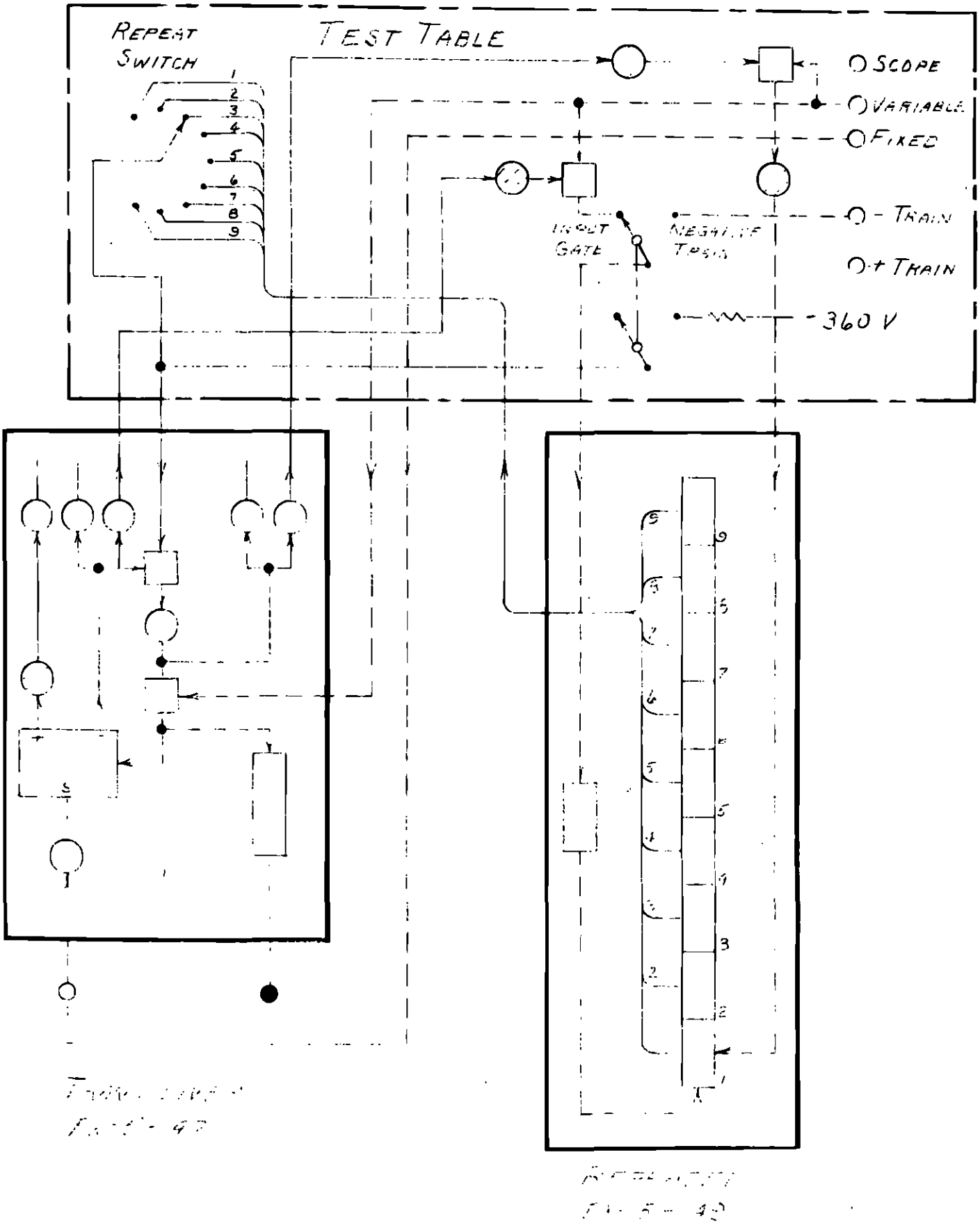
The test oscilloscope is especially adaptable for synchronization from the central program pulses (CPP) of the ENIAC, and a special blanking circuit also provides for turning "on" or "off" any section of the sweep by control of the central program pulses.

12.5 Plug-in Unit Test Voltages

In most instances the plug-in units are tested with the voltages given on the wiring diagrams. However, in some cases it was expedient to test at different voltages. The table below gives these changes.

Plug-in Unit	Wiring Diagram Voltages	Test Table Voltages
Master Programmer Program (PX-8-103)	+290	-180
	+220	-250
	+365	-105
	+460	- 10
	+300	-170
Master Programmer Transmitter (PX-8-105)	+ 95	+ 20
	+150	+ 75
	+230	+150
Master Cycler Reader Printer Starter (PX-9-104)	+200	+150
Master Cycler (PX-9-102)	-345	0
	-475	-130
	-120	+225
	-295	+ 50
Constant Transmitter Pulse Booster (PX-11-115)	+110	+105

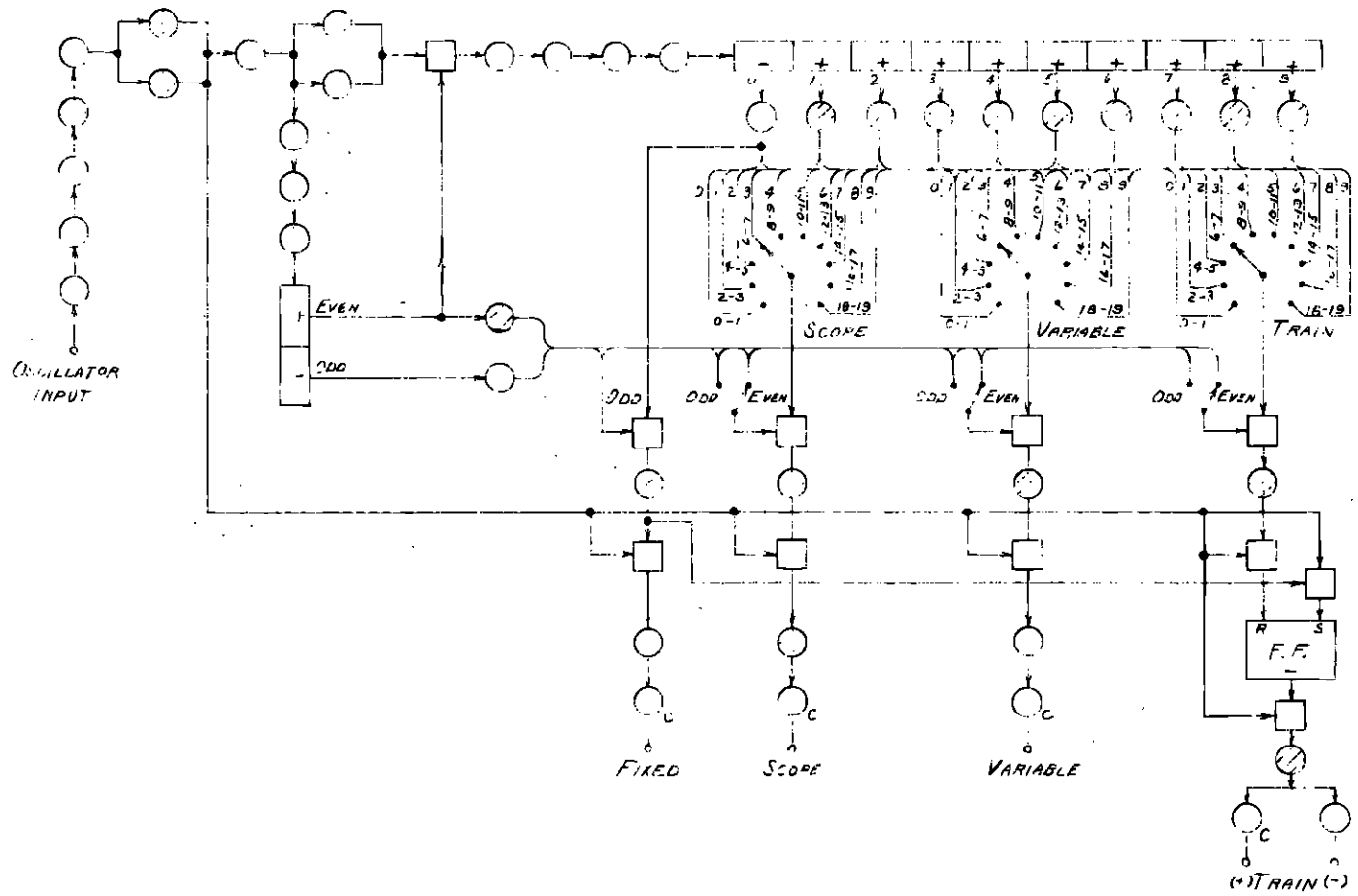
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DRAWN BY	
CHECKED BY	
APPROVED BY	

SCALE

PX-2-301



REVISED

MOORE SCHOOL OF ELECTRICAL ENGINEERING
UNIVERSITY OF PENNSYLVANIA

T.E. SYNCHRONIZING UNIT BLOCK DIAGRAM

SCALE			
DRAWN BY: CJMcC, MAY 5, 1946	CHECKED BY: Husky	APPROVED BY:	PX-2-302

A REPORT ON THE ENIAC

(Electronic Numerical Integrator and Computer)

Report of Work under Contract No. W-670-ORD-4926

Between

Ordnance Department, United States Army
Washington, D. C.

and

The University of Pennsylvania
Moore School of Electrical Engineering
Philadelphia, Pa.

PREFACE

The Report on the ENIAC consists of five separately bound parts, as follows:

1. ENIAC Operating Manual
2. ENIAC Maintenance Manual
3. Part I, Technical Description of the ENIAC
   Volume I (Chapters I to VI)
4. Part I, Technical Description of the ENIAC
   Volume II (Chapters VII to XI)
5. Part II, Technical Description of the ENIAC

Included with the Operating Manual and Parts I and II of the Technical Description are all drawings (see table 0.3 below) which are required for understanding these reports. The Maintenance Manual assumes access to the complete file of ENIAC drawings.

Part I of the Technical Description is intended for those who wish to have a general understanding of how the ENIAC works, without concerning themselves with the details of the circuits; it assumes no knowledge of electronics or circuit theory. Part II is intended for those who require a detailed understanding of the circuits. Its organization, to a great extent, duplicates that of Part I so as to make cross referencing between the two parts easy.

The ENIAC Operating Manual contains a complete set of instructions for operating the ENIAC. It includes very little explanatory material, and hence assumes familiarity with Part I of the Technical Description of the ENIAC. The ENIAC Maintenance Manual includes description of the various test units and procedures for testing, as well as a list of common and probable sources of trouble. It assumes a complete understanding of the circuits of ENIAC, i.e. a knowledge of both Parts I and II of the Technical Description of the ENIAC.

The Report on the ENIAC and the complete file of ENIAC drawings constitute a complete description and set of instructions for operation and maintenance of the machine. The drawings carry a number of the form PX-n-m. The following tables give the classification according to this numbering system.

TABLE 0.1

Values of n	Division
1	General
2	Test Equipment
3	Racks and Panels
4	Trays, Cables, Adaptors, and Load Boxes
5	Accumulators
6	High Speed Multiplier
7	Function Table
8	Master Programmer
9	Cycling Unit and Initiating Unit
10	Divider and Square Rooter
11	Constant Transmitter
12	Printer
13	Power Supplies

TABLE 0.2

Values of m	Subject
101-200	Wiring Diagrams
201-300	Mechanical Drawings
301-400	Report Drawings
401-500	Illustration Problem Set-Ups.

The reader of this report will be primarily interested in the types of drawings listed in the following paragraphs. A table on page 4 gives the corresponding drawing number for each unit of the ENIAC.

1) Front Panel Drawings. These drawings show in some detail the switches, sockets, etc., for each panel of each unit. They contain the essential instructions for setting up a problem on the ENIAC.

2) Front View Drawings. There is one of these drawings for each kind of panel used in the various units of the ENIAC. These show the relative position of the trays and the location of the various neon lights. Since these drawings show the neon lights, they can be used to check the proper operation of the various units.

3) Block Diagrams. These drawings illustrate the logical essentials of the internal circuits of each unit. That is, resistors, condensers, and some other electrical details are not shown; but complete channels (paths of pulses or gates representing numbers or program signals) are shown in all their multiplicity. These drawings will be of interest to those who are interested in Parts I and II of the Technical Report.

4) Cross-section Diagrams. These drawings are electronically complete except that only one channel is shown where there is more than one. Thus, these drawings show every resistor and condenser and any other electronic elements belonging to any circuit. These drawings will be of particular interest to the maintenance personnel and to those reading Part II of the technical report.

5) Detail Drawings. All other drawings of the ENIAC come under this heading. A complete file of drawings is available at the location of the ENIAC.

Table 0.3
ENIAC DRAWINGS

Unit	Front Panel	Front View	Block Diagram	Cross - Section
Initiating Unit	PX-9-302 9-302R	PX-9-305	PX-9-307	
Cycling Unit	PX-9-303 9-303R	PX-9-304	PX-9-307	
Accumulator	PX-5-301	PX-5-305	PX-5-304	PX-5-115
Multiplier	PX-6-302 6-302R 6-303 6-303R 6-304 6-304R	PX-6-309	PX-6-308	PX-6-112A 6-112B
Function Table	PX-7-302 7-302R 7-303 7-303R	PX-7-305	PX-7-304	PX-7-117 7-118
Divider and Square Rooter	PX-10-301 10-301R	PX-10-302	PX-10-304	
Constant Transmitter	PX-11-302 11-302R 11-303 11-303R 11-304 11-304R	PX-11-306	PX-11-307	PX-11-116 11-309 (C.T. and R.)
Printer	PX-12-301 12-301R 12-302 12-302R 12-303 12-303R	PX-12-306	PX-12-307	PX-12-115
Master Programmer	PX-8-301 8-301R 8-302 8-302R	PX-8-303	PX-8-304	PX-8-102

Other drawings of particular interest:

Floor Plan	PX-1-302	IBM Punch and Plugboard	PX-12-112 PX-12-305
A.C. Wiring	PX-1-303		
IBM Reader and plugboard	PX-11-119 PX-11-305	Pulse Amplifier and Block Diagram	PX-4-302 PX-4-301

Interconnection of Multiplier and Accumulators PX-6-311
Interconnection of Divider and Accumulators PX-10-307

The front view drawings and the large front panel drawings (whose numbers do not end with "R") are bound as a part of the Operator's Manual.

Included with the report is a folder containing all the drawings listed in the above table except the large front panel (see above). A complete file of drawings is available at the location of the ENIAC.

PART I

TECHNICAL DESCRIPTION OF THE ENIAC

by

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*In an envelope attached to the back cover.

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TECHNICAL DESCRIPTION OF ENIAC, PART I

Drawings bound with the text are given with a page reference. Those contained in a separate folder are listed without a page reference. Drawings referred to, but not included, in this report are marked with an asterisk. The last category of drawings are a part of the complete file of drawings at the ENIAC location.

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I. INTRODUCTION

1.1. BRIEF DESCRIPTION OF THE ENIAC

1.1.1. What the ENIAC Does

The Electronic Numerical Integrator and Computer (ENIAC) is a high-speed electronic computing machine which operates on discrete variables. It is capable of performing the arithmetic operations of addition, subtraction, multiplication, division, and square rooting on numbers (with sign indication) expressed in decimal form. The ENIAC, furthermore, remembers numbers which it reads from punched cards, or which are stored on the switches of its so called function tables, or which are formed in the process of computation, and makes them available as needed. The ENIAC records its results on punched cards from which tables can be automatically printed. Finally, the ENIAC is automatically sequenced, i.e., once set-up (see Sections 1.1.4. and 1.4. and subsequent chapters) to follow a routine consisting of operations in its repertoire, it carries out the routine without further human intervention. When instructed in an appropriate routine consisting of arithmetic operations, looking up numbers stored in function tables, etc., the ENIAC can carry out complex mathematical operations such as interpolation and numerical integration and differentiation.

The speed of the ENIAC is at least 500 times as great as that of any other existing computing machine. The fundamental signals used in the ENIAC are emitted by its oscillator at the rate of 100,000 per second. The interval between successive signals, 10 micro-seconds, is designated by the term pulse time. The time unit in which the operation time for various parts of the ENIAC is reckoned is the addition time. An addition time is 20 pulse times or 200 micro-seconds (1/5000 th of a second). An addition time is so named because it

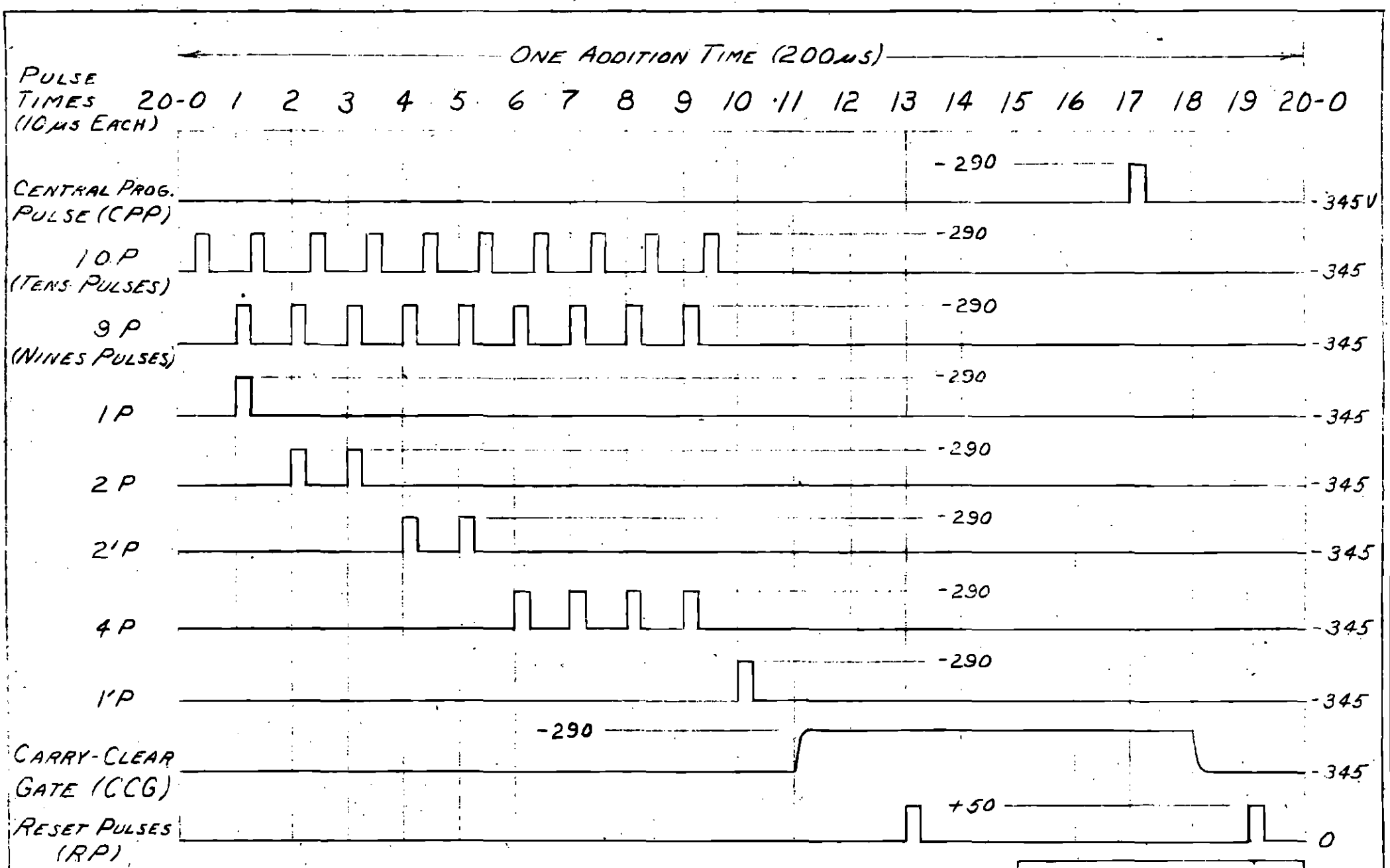
is the time required to complete an addition. Other operations require an integral number of addition times (see Table 1-1).

1.1.2. The Units of the ENIAC

The ENIAC proper consists of 40 panels arranged in U shape, 3 portable function tables, a card reader, and a card punch (see PX-1-302). The term unit of the ENIAC is used to refer to one or more panels and associated devices (such as the portable function tables, for example) containing the equipment for carrying out certain specific related operations.

The units of the ENIAC can be classified functionally into 4 categories: arithmetic, memory, input and output, and governing. The arithmetic units include 20 accumulators (for addition and subtraction), 1 high-speed multiplier, and 1 combination divider and square rooter. There are two primary memory aspects in the ENIAC: memory for numbers and memory for programming instructions. The constant transmitter, 3 function tables, and the 20 accumulators provide numerical memory. The constant transmitter with its associated card reader reads from punched cards, numbers that are changed in the course of a computation and makes these numbers available to the computer as needed. Numbers that remain constant throughout a computation are stored on the switches of the constant transmitter or of the portable function tables and emitted when needed. The accumulators, not only function arithmetically, but also can be used to store numbers which are computed in one part of a computation and required in other parts. All units have program controls (see Sections 1.1.4. and 1.3.1.) which contribute to the programming memory in the following ways:

1) by recognizing the reception of a program input signal which stimulates the unit to perform



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CYCLING UNIT
PULSES & GATES
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2) by causing the programming circuits (see Section 1.3.) to operate (as specified by the setting of program switches when there are options regarding the operation to be performed)

and 3) on the completion of the operation, by emitting a program output signal which, by means of program cable connections to program lines (see Section 1.1.4.) is brought to other units to cause them to operate. The program cable connections and switch settings are established before the computation begins.

The kind of programming described in points 1, 2, and 3 above is described as local programming memory because it is taken care of locally at each unit for that unit. The master programmer provides a certain amount of centralized programming memory by coordinating the local programming of the other units.

The input devices for the ENIAC consist of the card reader and the constant transmitter mentioned above in connection with numerical memory. The printer and card punch record computed results.

The governing units of the ENIAC are the initiating unit and the cycling unit. The initiating unit has controls for turning the power on and off, starting a computation, initial clearing, and other special functions. The cycling unit converts 100 kc sine waves emitted by its oscillator into a fundamental train of signals repeated every addition time (i.e. repeated 5000 times per second). These signals include various sequences of pulses and a gate. The term pulse is used to refer to a voltage change (either positive or negative) from some reference level and the restoration to the reference level which takes place in a short time, between 2 and 5 micro-seconds. The term gate also refers to a voltage change and the restoration to the reference level but differs from a pulse in duration. In the ENIAC a gate lasts for at least 10 micro-seconds.

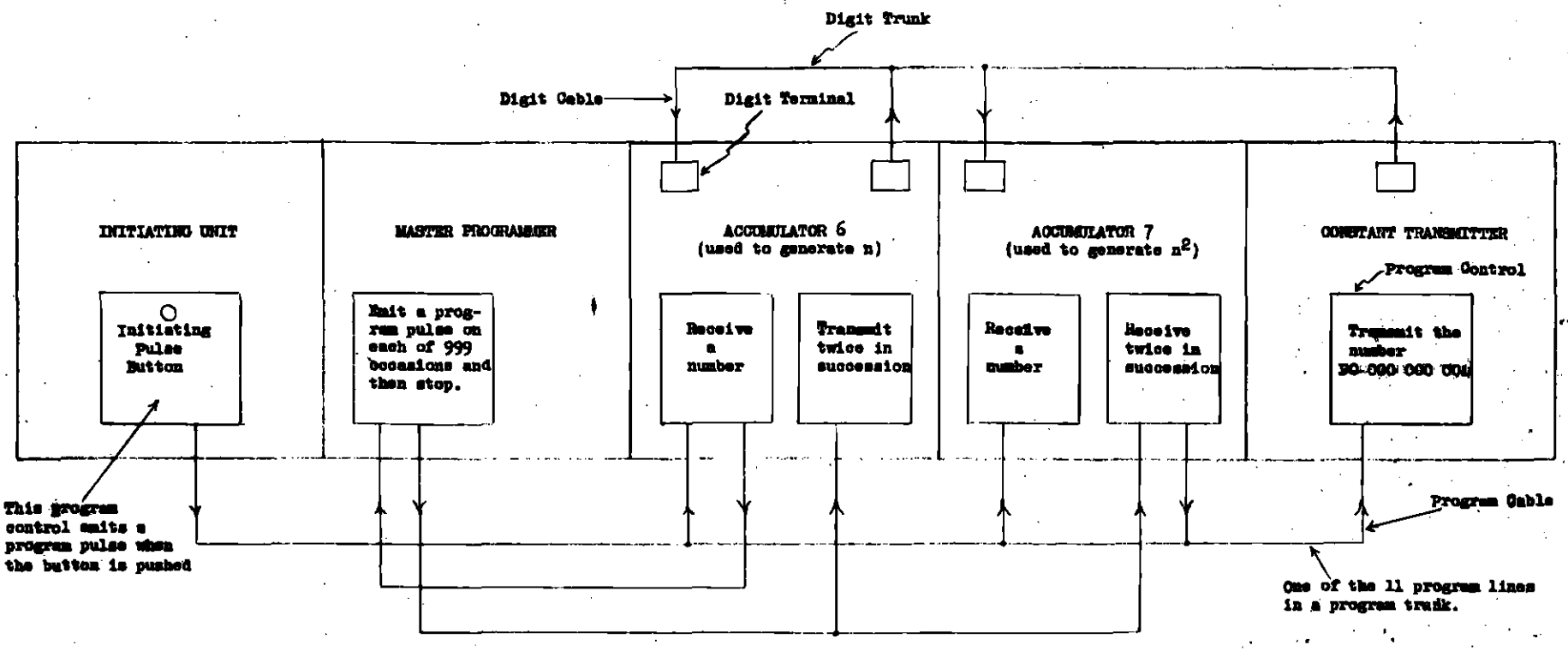
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TABLE 1-1

UNITS OF THE ENIAC

UNIT	TOTAL NO.	OPERATIONS	OPERATION TIME (1 addition time = 1/5000 of a second)
Accumulator	20	1. Stores a 10 digit signed number. 2. Receives a number and adds it to its contents. 3. Transmits its contents and/or the negative. (2 and 3: on r successive times ($1 \leq r \leq 9$).	1. Continues to do so until instructed to clear. 2. r addition times. 3. r addition times.
High Speed Multiplier	1	Multiplies a signed multiplicand having as many as 10 digits by a signed multiplier of p digits (where $2 \leq p \leq 10$).	p + 4 addition times.
Divider and Square Rooter	1	Finds a p (where p = 4, 7, 8, 9, 10) digit quotient or square root for arguments with up to 10 digits.	Approximately 13 p addition times (also see p. VI (31)).
Function Table (including an associated portable function table)	3	1. Each function table stores by means of switch settings a total of 1248 variable digits and 208 signs in such a way that 12 digits and 2 signs are associated with an argument between -2 and 101. In addition, 8 digits constant throughout the range of the argument can be remembered. 2. Function table selects and transmits the functional value (12 variable digits, 2 signs, and 8 constant digits) or the negative of the functional value associated with a particular value of the argument. The transmission may be done r times ($1 \leq r \leq 9$) in succession.	2. 4 + r addition times for looking up the functional value and transmitting it r times.
Constant Transmitter and Reader	1	1. Constant transmitter stores 80 digits and 16 signs which the reader reads from punched cards and stores 20 digits and 4 signs set up manually on its switches. 2. Constant transmitter emits a signed 5 or 10 digit number.	1. The reader scans a card and causes 80 digits and 16 signs punched on the card to be stored in the constant transmitter in approximately 1/2 second. 2. 1 addition time.
Printer and Punch	1	The printer receives information for 80 digits and 16 signs from accumulators and the master programmer and causes this information to be punched on cards from which it can be printed.	80 digits and 16 signs are punched on a card in approximately 0.6 second.
Master Programmer	1	Coordinates the local programming of the other ENIAC units.	1 addition time.
Cycling Unit	1	Emits the fundamental train of pulses and the gate upon which other ENIAC units operate and which, thus, keeps them in synchronism with one another.	In each addition time (also see Chapter III).
Initiating Unit	1	Has controls for turning power on and off, starting the ENIAC, clearing the ENIAC, and other special functions.	

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ORDER OF OPERATIONS

1. When the initiating pulse button is pushed, accumulators 6 and 7 receive from the constant transmitter the digit 1 in the units place.

2. The master programmer determines whether to continue or to terminate the computation.

3. Accumulator 6 transmits its contents twice and accumulator 7 receives twice so that when this operation is completed, accumulator 6 holds the No. 1 and accumulator 7 holds the No. 3.

4. Accumulators 6 and 7 each receive 1 unit from the constant transmitter so that, as a result of this operation, accumulator 6 holds the No. 2 and accumulator 7 holds the No. 4.

5., 6., 7., Repeat items 2., 3., 4., respectively, etc.

SCHEMATIC DIAGRAM OF PROGRAM SEQUENCE FOR GENERATING n, n^2, for $1 \leq n \leq 1000$

Figure 1-1

The nomenclature for and the temporal order of the cycling unit pulses and gate are shown on PX-9-306.

Table 1-1 lists the units of the ENIAC, their operations, and operation times.

1.1.3. Representation of Digits by Pulses

With a few exceptions digits are communicated from one unit of the ENIAC to another in pulse form. Digit trays stacked above the front panels running from accumulator 1 to the second panel of the constant transmitter are used for this transmission. A digit tray has 11 wires and a ground. Each of ten wires carries the pulses for one place of a 10 place decimal number. To represent the digit n (where $0 \leqslant n \leqslant 9$) in a particular decimal place, n pulses are transmitted over the wire associated with that particular decimal place. The 11th wire is used for the transmission of sign information. No pulses are transmitted for sign plus and 9 pulses for sign minus (see the discussion of complements below). Pulses are transmitted over all 11 conductors simultaneously.

Each digit tray is 8 feet long and runs past 4 panels of the ENIAC. A 12 point terminal at each end of a tray makes it possible to connect a number of trays serially by means of jumper cables so as to form a digit trunk passing as many units of the ENIAC as desired. Spaced at two foot intervals on the digit trays are additional 12 point terminals. Units which are to communicate with one another in the course of a computation have their digit input and/or output terminals connected by means of digit cables to these 12 point terminals on a digit trunk. A resistance load box is plugged into an unused terminal on either the first or last tray of a digit trunk. This makes it possible to connect varying numbers of units in parallel into a digit trunk. At any given time, only one 10 digit number with its sign may be transferred over a particular digit

trunk. More than 1 unit may listen to this number. Through the use of more than one digit trunk, several different numbers may be transferred simultaneously. (also Section 1.1.5.).

The units of the ENIAC transmit numerical information by emitting appropriate numbers of the 9 pulses or of the 1, 2, 2' and 4 pulses and the 1' pulse (see PX-9-306) which they receive from the cycling unit. Addition is performed in accumulators by means of 10 decade counters (see Section 1.2.2.), one counter for each decimal place of a 10 digit number, and a binary counter for sign plus (P) or minus (M). These counters are advanced one step by each pulse received. The decade counters and PM counter of an accumulator are so interconnected that provision is made for carry over. Subtraction is performed by adding the negative of the subtrahend to the minuend.

In order to avoid the necessity for cycling counters backwards, the negative of a number is represented as a complement with respect to a power of ten. Let us consider the decimal point to be located at the extreme right of an accumulator. Then the complement with respect to 10^{10} of the positive number stored in an accumulator as $P + \sum_{i=0}^{9} a_i \cdot 10^i$ is formed by transmitting 9 pulses for sign M and by transmitting the digit pulses for $10^{10} - \sum_{i=0}^{9} a_i \cdot 10^i$. Similarly, the complement with respect to 10^{10} of the negative number stored as $M + \sum_{i=0}^{9} b_i \cdot 10^i$ is formed by transmitting no pulses for sign P and by transmitting the digit pulses for $10^{10} - \sum_{i=0}^{9} b_i \cdot 10^i$. For example, the complement with respect to 10^{10} of P0 000 023 407 is M9 999 976 593; the 10^{10} complement of M9 307 504 000 is P0 692 495 000. As will be shown in the chapter dealing with the accumulator (Chapter IV), the mechanics of transmitting the digit pulses for a complement with respect to 10^{10} actually consist of transmitting first the

pulses for $\sum_{i=0}^{9} (9-a_i) \cdot 10^i$ and then of transmitting one more pulse in the 10^0 decade place. The terms $9-a_i$ are called nines complements.

If desired, operations may be performed on n digits where $n \leq 10$. Here, we consider the significant figures to be located as far to the left as possible in the accumulator with the decimal point to the immediate right of the last significant figure at the right. Then, the digits for a complement with respect to 10^n are formed by emitting nines complements in all decade places and then by emitting an additional pulse in the n^{th} decade place from the left.

Because the counters in an accumulator are so connected that there is carry over not only from each decade counter to the one on its left but also from the 10^{th} decade counter to the binary counter for sign, the usual arithmetic properties obtain when complements are used in addition and subtraction. In this connection, it should be noted that even though, in the above discussion, we implied that sign P indicates a positive number and sign M a negative number, these signs may have another meaning. For example, if an accumulator holds P9 999 999 999, the carry-over to the PM counter which results when a positive number not in excess of 10^{10} is added to this number, causes the accumulator to register sign M. Here the M indicates that the sum is off scale.

1.1.4. Programming by Means of Pulses, Switches and Cables

Before a computation can be performed on the ENIAC, not only must the digit input and output terminals of the units be connected into digit trunks for the communication of numerical data, but also the units must be set up so as to recognize when they are to operate and which particular operations are to be performed. Program controls and program trays and cables are used to instruct the ENIAC in the programming requirements for a particular computation.

Each unit of the ENIAC has one or more program controls. These controls are either of the repeat or non-repeat type. Non-repeat program controls have an input terminal for a program signal and a receiver(see below and Section 1.2.4.). Repeat controls have both an input and an output terminal for a program signal and a transceiver (see below and Section 1.2.4.) or some logically equivalent device. Each program control on a unit which is capable of more than one operation or which is capable of performing operations in a variety of ways has a set of program switches.

Receivers and transceivers alike have the following properties: 1) they have two stable states which will be referred to as the normal and abnormal states; 2) when a program input signal is received, they are set into the abnormal state; 3) they are so connected (through the program switches, if any) to the programming circuits (see Section 1.3.) that, in the abnormal state, they cause the programming circuits to function appropriately; and 4) when the required routine has been completed, they are reset to the normal state so that activity in the unit ceases. When the set of instructions either set up on the program switches of a repeat control or built into the programming circuits have been completed, moreover, the transceiver of a repeat program control causes a central programming pulse (CPP on PX-9-306) to be emitted as a program output pulse from the program control's output terminal.

The program trays, like the digit trays are 8 feet long, contain 11 wires and a ground, and have 12 point terminals at each end, so that as many trays as desired can be jumper connected to form a program trunk. As in the case of digit trunks, too, a resistance load is plugged into an unused terminal at one end of a program trunk. Each of the 11 lines running the length of a program trunk is referred to as a program line. The program trays differ from the digit

trays only in that at two foot intervals the program trays have a set of 11 two point program terminals (1 wire and a shield) instead of a 12 point digit terminal. Input and output terminals of program controls are connected to the program lines by means of program cables.

The procedure for instructing the ENIAC in its routine, then, consists of setting program switches on the units so that, when stimulated by a program input pulse, the program controls will cause the units to carry out a set of specific operations. The temporal order in which the operations are to follow one another is determined by the manner in which program pulse input and output terminals are connected to program lines. All program controls whose program pulse input terminals are connected into the same program line start to operate simultaneously when that program line carries a program signal. If one of the program controls thus stimulated is a repeat program control and if its program pulse output terminal is connected to a second program line all program controls whose program input terminals are connected to this second program line start to operate when the routine set up on the repeat program control has been completed.

The schematic diagram of Figure 1-1 illustrates the method of setting up an extremely simple computation. Each rectangle within the square that symbolizes a unit of the ENIAC represents a program control with program pulse input terminal and output terminal and possibly program switches. The instructions set up on the program switches of a program control are described inside the box representing the program control.

1.1.5. Synchronized System

All units of the ENIAC operate in synchronism with one another, i.e., all units that start to operate at the same time complete their operations either at the same instant or at times that differ by an integral number of addition

times. The phrase "complete an operation" covers not only finishing the numerical processes involved in the operation but also the emission of a program output signal.

The basis of this synchronization is the fundamental train of pulses and a gate emitted by the cycling unit and delivered to all units of the ENIAC by means of a set of jumper connected trays called the synchronizing trunk. These trays are physically the same as the digit trays. The central programming pulse (CPP) emitted by the cycling unit in pulse time 17 of every addition time cycle plays a major role in such synchronization since the program output pulse which a repeat program control emits upon the completion of a program results from allowing a CPP to pass. The units of the ENIAC, moreover, have been so designed that in order to complete their operations they require the pulses and gate of either one addition time cycle or of an integral number of addition time cycles.

Even though the electromechanical devices used with the ENIAC, the reader and the card punch, do not take an absolutely definite number of addition time cycles to complete their operations, these units have been integrated into the synchronized system since they have been provided with program controls which emit a CPP as a program output pulse. Units of the ENIAC can even operate in parallel with the card reader since the reader does not emit a program output pulse signifying the completion of reading until it has received as an interlock pulse a program output pulse from some other unit of the ENIAC to indicate that the sequence carried on in parallel with reading has been completed.

In this report, incidentally, we will follow the convention that an addition time has its origin 3 pulse times after the CPP as shown on PX-9-306. This means that we will talk about a program's being stimulated at the end of

addition time i and being carried out in addition time i + 1 by means of the cycling unit pulses and gate emitted during addition time i + 1.

Because the units of the ENIAC operate in synchronism with one another and because multiple digit and program trunks have been provided, the operator can schedule parallel operations when planning the set-up of a problem. For example, the multiplier can be operating while several accumulators are performing additions and subtractions and while the divider is finding a quotient. Naturally, the scheduling of parallel operations requires that the operator plan for the use of separate digit trunks for the various operations and, in some cases, requires that attention be given to the number of addition times needed for the operations.

1.2. ELECTRONIC ELEMENTS

The circuits of the ENIAC are designed around a relatively small number of basic electronic elements. The following discussion, while wholly inadequate to convey any real knowledge of vacuum tubes or their action, is intended to enable the reader to obtain a formal acquaintance with some of the phenomena and terminology connected with the ENIAC.

The simplest tube used is the triode, so called because it has 3 characteristic elements, namely the cathode (surface which gives off electrons), the plate or anode (surface which receives electrons), and the grid (which controls the current passing through the tube). In addition, there is a heater to bring the cathode to the temperature required for it to emit electrons. Sometimes, 2 triodes are housed in one envelope. We shall refer to these as two tubes. Other tubes used in the ENIAC are multigrid tubes, for example, the pentode which has 3 grids.

To say that a tube is "on" or conducting means that with the usual convention of sign, current is flowing from the plate to the cathode. This implies that the plate is at a slightly higher voltage than the cathode, but that this voltage drop is trifling compared to the drop when the tube is "off" or non-conducting. Thus, if a tube is turned "off", i.e. changes from conducting to non-conducting, the voltage of the plate is raised and that of the cathode is lowered. Hence the plate emits a positive signal and the cathode one that is negative. If the tube is turned on these signs are reversed. Within appropriate limits, a tube is conducting if its grid (or grids) is (or are) kept above a certain voltage, non-conducting if below that voltage. Thus a tube is turned on by applying a positive signal to its grid (or grids), turned off by a negative signal.

In all cases, vacuum tubes in the ENIAC circuits are used only as on-off devices instead of as amplitude sensitive devices, i.e., the presence or absence of a signal depends on whether a tube is conducting or not-conducting and not on any measured magnitude of current and voltage. Furthermore, the machine has been so designed that signals are not constantly being degenerated but instead are regenerated from time to time out of the fundamental train of pulses and a gate emitted by the cycling unit.

1.2.1. Single Tube Elements

1.2.1.1. Buffers and Cathode Followers

Buffers and cathode followers are normally non-conducting tubes with a single input and a single output. When a positive signal is applied to the grid of a buffer, the output, taken off the plate side, is negative. In the cathode follower, where the output is taken off the cathode, the application of a positive signal to the grid results in the emission of a positive signal.

When the outputs of a number of buffers or cathode followers are connected together to a common load resistor, the resulting circuit provides for the logical "or" since when any one of the buffers or cathode followers receives a positive signal, the circuit emits a negative or positive signal respectively.

1.2.1.2. Inverters

An inverter is a tube whose grid is normally at a positive potential so that the tube is conducting. When a negative signal, applied to the grid, drives the tube to cut off, the output taken off the plate, is a positive signal. A positive signal is necessary to operate a gate tube as will be described in Section 1.2.1.3.

1.2.1.3. Gate tubes

A gate tube is a multiple grid tube with two inputs and an output normally taken off the plate. A gate tube emits a negative signal when both of its input grids are brought from a negative cut off voltage to a positive voltage. Thus, a gate tube is used to note the coincidence of two positive signals and hence corresponds to the logical "and".

A positive signal applied to one grid of a gate tube is said to "open the gate", since when this happens a positive signal reaching the other grid makes the tube conduct and hence emit a signal. The term "gate" is used in two senses: In one it means a gate tube (as described above) and in the other, the signal, lasting 10 μs or longer, which is used to open a gate tube (see Section 1.1.2.).

1.2.2. Multi-Tube Elements

1.2.2.1. Flip-Flops

The basic electronic memory device of the ENIAC is the flip-flop. A flip-flop consists essentially of a pair of triodes so connected that at any

given time only one of the pair can be conducting. When a certain one of the tubes is conducting (and the other is not), the flip-flop is said to be in the normal state; when the other tube is conducting (and the first is not), the flip-flop is in the abnormal state. A flip-flop has two inputs and two outputs. A pulse received on one input (the set input), throws the flip-flop into the abnormal state in which state it remains until restored to the normal state by a pulse received at its second (or reset) input. When the flip-flop is in the normal state, one output is positive and the other negative. In the abnormal state, the polarity of its outputs is reversed.

Corresponding to each flip-flop in the ENIAC, there is a neon lamp. The neon lamp is so connected to its corresponding flip-flop that, with the exception of some neons in the divider and square rooter, the neon is lit when the flip-flop is in the abnormal state. Drawing PX-10-302 indicates when the neons in the divider and square rooter are lit.

These neons provide one of the most important visual checks on the operation of the ENIAC. In addition to the continuous mode of operation at the 100 kc rate, the ENIAC has 2 special modes of operation, 1 addition time and 1 pulse time operation, which permit the operator without disturbing the flip-flop memory, to stop the ENIAC at some point to examine the neons and, thus, to determine whether or not the proper sequence of events is taking place.

1.2.2.2. Counters

The counters of the ENIAC, in general, consist of a number of flip-flops arranged in sequence and interconnected so that the following characteristics result:

1) At any given time, only one flip-flop can be in the abnormal state and all others must be in the normal state.

2) The reception of a pulse at the input to the counter causes the flip-flop which is in the abnormal state to be reset and causes its successor to be set.

3) The counter can be cleared so that a specific stage comes up in the abnormal state and all others in the normal state.

Each flip-flop of a counter is called a stage and the reception of a pulse at a counter is said to advance the counter to the next stage. All counters in the ENIAC are ring counters, i.e., the first and last stages are so connected that if the counter is in its last stage and a pulse is received, the last stage is reset and the first stage is flipped into the abnormal state.

In accumulators, a 10 stage (decade) ring counter is used for each place of a 10 place number. Each stage of a decade counter corresponds to one of the digits between 0 and 9 inclusive.

The sign of a number is handled by means of a PM counter which differs somewhat from the other ENIAC counters. The PM counter has 2 tubes, one for sign P and for sign M. Each tube, here, is called a stage. The two tubes are so connected that only one of them can be conducting at a given time. Each pulse received cycles the PM counter 1 stage. Notice, that while the PM counter uses 2 tubes as does a flip-flop, it differs from an ordinary flip-flop in that it has but one input. The PM counter is also a ring counter.

Since each stage of a counter (other than the PM counter) is a flip-flop, one or both of its outputs are available for controlling other circuits. In the decade counters mentioned above, for example, one set of such outputs (which are referred to as the static outputs) can be used to deliver to the printer information about the number stored in a given accumulator. Ring counters are also used in the programming circuits of most ENIAC units. Here the outputs of the various stages are taken to gates.

1.2.2.3. Standard Transmitters

To meet the power needs resulting from the large capacitance associated with the interconnection circuits (digit trays, program trays, digit cables, etc.) and the high speed with which pulses are transmitted in the ENIAC, and also to provide positive output pulses (since positive pulses are required to operate gate tubes in the receiving units), the pulse outputs of all units (except the digit pulse output of the high-speed multiplier and the divider and square rooter) are passed through standard transmitters. A transmitter consists essentially of an inverter tube whose output is fed to the grids of 2 amplifying tubes which have their plates connected in parallel. The cathodes of the amplifier tubes are connected in parallel to ground through a resistor and the output of the transmitter is taken off between cathode and ground. As previously mentioned, varying numbers of output transmitters can be connected to the same program line or digit trunk since a load resistor is not built into each transmitter but is instead plugged into the trunk line.

The answer output circuits of the high-speed multiplier and of the divider and square rooter consist of inverter tubes with built-in load resistance. Therefore, the answer output terminals on these units are connected directly to the appropriate digit input terminals through a cable without resistance load or through a digit tray with no load box plugged into it. No other units may be connected in parallel into such a digit tray.

1.2.2.4. Receivers and Transceivers

Receivers and transceivers are used in the ENIAC to note the reception of a program pulse and to activate the programming circuits when a program pulse is received. As mentioned earlier, receivers are found in non-repeat program controls and transceivers in repeat program controls. In the divider and square rooter

and in the high speed multiplier, however, there are a few examples of receivers which are not parts of program controls. Also, the reader, printer, and initiating pulse program controls are exceptional repeat program controls in that they do not contain transceivers.

To describe and illustrate the use of receivers and transceivers we shall refer to the program controls of an accumulator in which these devices are used in typical fashion (see drawing PX-5-304).

The receiver consists of an input buffer (66), a flip-flop (64, 65), an inverter (the left hand tube numbered 62), a cathode follower (63), a buffer (62), and a reset gate (61). An input pulse received at the program pulse input terminal associated with a receiver, passes through buffer 66 and sets the flip-flop of the receiver. The normally positive output of the flip-flop passes through the inverter and cathode follower and then through a program switch which routes it to a set of gates. Similarly, the normally negative output of the flip-flop, through buffer 62, is routed through program switches to another set of gates. Notice that before the reception of a program pulse, the outputs of the receiver are such that the gates remain closed; when the receiver is set, its output signals open the gates to which they are delivered and cause the unit to carry out the routine specified on the associated program switches. The CPP, which occurs 20 pulse times after the program input pulse which sets the receiver, passes through gate 61 (held open by the normally negative output of the flip-flop through buffer 62) and resets the receiver. Thus, a receiver is always reset one addition time after it has been set. Notice that the same receiver must not be stimulated on successive addition times since one addition time after a receiver is set it attempts to reset itself.

A transceiver, like a receiver, has an input buffer (69), a flip-flop

(66, 67), an inverter (65), cathode follower (64), and a reset gate (68). The transceiver, however, has several additional buffers (61), and (63), an extra gate (62) and inverter (65) and a standard transmitter (70, 71, 72). The transceiver elements which resemble receiver elements function in precisely the same fashion. The resetting of a transceiver, however, differs from that of a receiver. Transceivers usually operate in conjunction with a program ring counter or, as in the accumulator case, with a repeater ring counter. In the illustrative example being discussed here, one output of the transceiver is taken to gate K50. When the transceiver is set, gate H50 is open so that a CPP is allowed to pass through and cycle the repeater ring (64-72) each addition time that the transceiver remains in the abnormal state. Each point on the repeat switch (used to specify the number of times in succession that an operation is to be repeated) of an accumulator repeat program control is connected to one stage of this ring. When the repeater ring reaches the stage specified on the repeat switch, gate 62 receives a positive signal from that stage of the ring. The coincidence of a signal from the repeater ring and from the normally negative output of the flip-flop causes gate 62 to emit a signal which is inverted into a positive signal by inverter 65. The output of tube 65, through the buffers 63, goes on to stimulate certain clearing actions in the accumulator, and delivered to gate 68, allows the next CPP to pass through this gate. The output of gate 68 not only resets the transceiver but also passes through the standard transmitter (70, 71, 72) to be emitted from the program pulse output terminal of the program control. Notice that a transceiver remains set throughout the number of addition times required to complete the program specified on its associated switches, is reset at the end of the addition time in which the program is completed and emits a program output pulse when it is reset. At least one addition time should intervene between the

transmission of a program output pulse and the next stimulation of a repeat program control in order to allow the control's transceiver to reset itself.

1.2.2.5. Plug-In Units

Wherever possible the design of elements of the ENIAC has been standardized and these elements have been used repeatedly in various units. Furthermore, to increase the ease of testing and replacing faulty components, many of these standardized elements have been designed as plug-in units.

The receivers and transceivers are of this nature. Each receiver plug-in unit has two receivers. A transceiver plug-in unit has just one transceiver. Another type of plug-in unit is the accumulator decade plug-in unit which consists of a decade ring counter, a pulse standardizer for shaping pulse input to the decade, carry over circuits, output transmitters, etc. In all, there are a total of 20 different types of plug-in units. These are enumerated on PX-2-123 where references are also made to detailed drawings of the plug-in units.

1.3. CLASSIFICATION OF ENIAC CIRCUITS: Numerical and Programming

The circuits of most ENIAC units can be conveniently described according to 2 classifications, numerical and programming. The numerical circuits are those which operate on the pulses or static signals which represent digits or sign. For example, in an accumulator the decade and PM counters or in the printer the tubes which are set up by the static outputs of counters whose information is to be punched on a card are classified as numerical circuits. The programming circuits are concerned with the following activities:

1) Recognizing when and how a unit is to function.

2) Stimulating the numerical circuits to operate appropriately.

3) Emitting a program output pulse to signify completion of a program.

In the case of certain units a further subdivision of the programming classification into program controls (see Section 1.1.4.) and common programming circuits is desirable. The program controls, then, are charged with activities 1 and 3 above and the common programming circuits with activity 2.

1.3.1. Program Controls

The accumulator, high speed multiplier, divider and square rooter, and function table have multiple sets of program controls. These program controls include not only a receiver or transceiver, program pulse input terminal and possibly program pulse output terminal but also program switches for describing the procedure to be followed when the program control is stimulated. In each of these units, any one of the program controls, when stimulated by the reception of a program input pulse, can activate the common programming circuits. The buffers and cathode followers in the receivers and transceivers of these program controls serve to isolate one program control from the others. In the constant transmitter, which has a total of 30 program controls each consisting of a transceiver, program pulse input and output terminals, and a program switch, each group of six program controls operates a set of programming circuits in common. In the remaining ENIAC units the program controls and programming circuits are closely integrated with one another.

If a unit has more than one program control, in general, only one control should be operating at any given time so that inconsistent demands are not made on the common programming circuits or the numerical circuits of the unit.

1.3.2. Common Programming Circuits

In the previous section it was pointed out that the stimulation of a program control of a unit results in activating the unit's common programming circuits. It should be pointed out that in a few cases the common programming

circuits of a unit can be entered without going through a program control. For example, several accumulators are used in conjunction with the high speed multiplier. These accumulators receive components of the product as they are emitted from the multiplier. Ordinarily, to stimulate reception of a number, a program input pulse must be delivered to an accumulator program control having its program switch set to a receive setting. Then, the output of the receiver or transceiver of the program control activates the programming circuits so that reception takes place. The multiplier, however, has been designed so that it contains receivers which are set when the associated product accumulators should receive components of the product. These receivers in the multiplier are directly connected to the common programming circuits of the associated accumulators so that reception is stimulated when the multiplier's receivers are set even though no program controls on the accumulators are stimulated. Several such examples of direct entry into the common programming circuits of accumulators are to be found in the chapters dealing with the high speed multipler and the divider and square rooter.

1.4. PROGRAMMING THE ENIAC

In this portion of the Technical Manual for the ENIAC, Part I, much emphasis will be given to the planning of computations to be performed.

1.4.1. Preparatory Formulation of the Problem

Starting with the mathematical equations which describe a problem, such as the total or partial differential equations for example, the operator must first break the equations down into a form involving the arithmetic operations of which the ENIAC is capable. Another necessary preliminary step consists of planning for the storage of numerical data. The initial conditions and other

constants basic to the computation will be given to the ENIAC by means of punched cards and the setting of switches on the constant transmitter. Arbitrary functions and other constants can be stored in the function tables. Numbers formed in the course of a computation and required in subsequent parts of a computation can be stored in accumulators. Should the quantity of numbers to be stored for further computation exceed the accumulator storage capacity, such numbers can be punched on cards by the printer unit and later can be inserted into the ENIAC again by means of the card reader and constant transmitter.

1.4.2. Planning the Programs and Program Sequences

For each arithmetic operation in the computation, one or more of the ENIAC's program controls will have to be set-up by the connection of program cables and possibly the setting of program switches. For example, if the numbers a and b are each stored in an accumulator and if a+b is to be formed in the accumulator containing b, then the accumulator which stores a, must be instructed to transmit and the one storing b, must be instructed to receive the transmitted number.

The instructions given to a single program control are referred to as a program. It is possible for a number of programs to be carried out in different units simultaneously. In general, however, only one program at a time can be performed in a given unit.

A unit carries out the program set up on one of its program controls when a pulse is delivered to the program control's program pulse input terminal, i.e., when the program control is stimulated. If a number of programs are to be performed in parallel, all of the program controls involved must be stimulated either by a pulse carried on the same program line or by pulses from different program lines which are activated at the same time.

The operator ties individual programs together into a program sequence in which one collection of programs is automatically stimulated upon the completion of another collection of programs by delivering the program output pulse of the program control used for a program of the first collection to a given program line and by picking up the stimulating pulse for all programs of the second collection from that same program line (see Section 1.1.4.)

1.4.3. Programming on Higher Levels

Certain program sequences of a computation may have to be iterated a number of times. The iteration of a program sequence into a program chain is accomplished through the use of the master programmer. This unit can also link together a number of chains or chains and sequences into a new program sequence which itself is to be iterated into a chain, etc.

The master programmer has a number of program controls each of which has a single input for program pulses and multiple program pulse output terminals. Each time a program input pulse is received, a pulse is emitted from one of the output terminals. The circuits of each control cause a pulse to be emitted from a given terminal a certain number of times which may be specified by the setting of a switch or in some other way and then to be emitted from another output terminal. Thus, the iteration of a program sequence into a chain can be accomplished by delivering the final program pulse of the sequence to a master programmer control and by picking up the initial pulse for the sequence from the program line to which the appropriate master programmer output terminal is connected. Another sequence or chain is linked to the first chain by picking up its initial pulse from the program line to which a second output terminal of the master programmer is connected, etc.

1.4.4. Special Linking of Program Sequences by Magnitude Discrimination

Not only can programs be linked together sequentially as described above in Sections 1.4.2, and 1.4.3 but, in addition, the ENIAC can be instructed to choose one of several program sequences depending on the magnitude of some number. This type of programming is referred to as magnitude discrimination.

In one form of magnitude discrimination, two numbers, a and b, are compared. If $a \geqslant b$, one program sequence is followed and in the opposite case, a second program sequence is stimulated. It is also possible to carry out more extensive magnitude discrimination programs in which the choice of program depends on a particular digit in some decimal place of a number.

Magnitude discrimination is accomplished by means of an accumulator and the master programmer. In such programs which will be discussed in greater detail in chapters IV and X, sign or digit pulses are used to stimulate program controls.

1.5. EQUIPMENT ASSOCIATED WITH THE ENIAC

In addition to the 40 panels, the portable function tables, the card reader and card punch which constitute the ENIAC proper, the ENIAC has certain associated ventilating, power, and testing equipment.

1.5.1. Ventilating Equipment

The ENIAC's 18,000 vacuum tubes generate a considerable amount of heat. An elaborate system of fans and blowers is used to drive off this heat. Each panel, moreover, has a thermostat which prevents the temperature inside the panel from exceeding 115°F by turning off the power to the ENIAC if this limit is exceeded. The ventilating system uses 240 V, three phase unregulated power.

1.5.2. Power Equipment

In addition to the a-c power for the heaters of its tubes and for the card reader and card punch, the ENIAC requires 78 different d-c voltages. These requirements are met in the following way:

Two hundred forty volt, three phase, regulated a-c is taken to power and auto-transformers which convert it into 110 V, 3 phase a-c. This power is carried on 3 buses in a power trough located along the front and bottom of the ENIAC panels. From this trough, the heaters and also the outlets below constant transmitter panel 3 and printer panel 2 are supplied with a-c power as long as the ENIAC's a-c power is turned on. The outlets below the other ENIAC panels are always alive.

The 240 V, 3 phase, regulated a-c is also taken to gas rectifier tubes in the ENIAC's 29 power supplies. The filaments of these tubes use 240 V, 3 phase, a-c. Through the use of bleeders the 78 d-c voltages are obtained. These voltages are carried to the ENIAC units by means of the d-c cables in the power trough mentioned above.

The power equipment is housed in 7 panels apart from the ENIAC and electrolytic condensers for filtering the d-c from the rectifier circuits are located in three condenser cabinets.

Only the control circuits for the power supplies are discussed at any length in this report (see Chapter II). The ENIAC MAINTENANCE MANUAL can be consulted for further details.

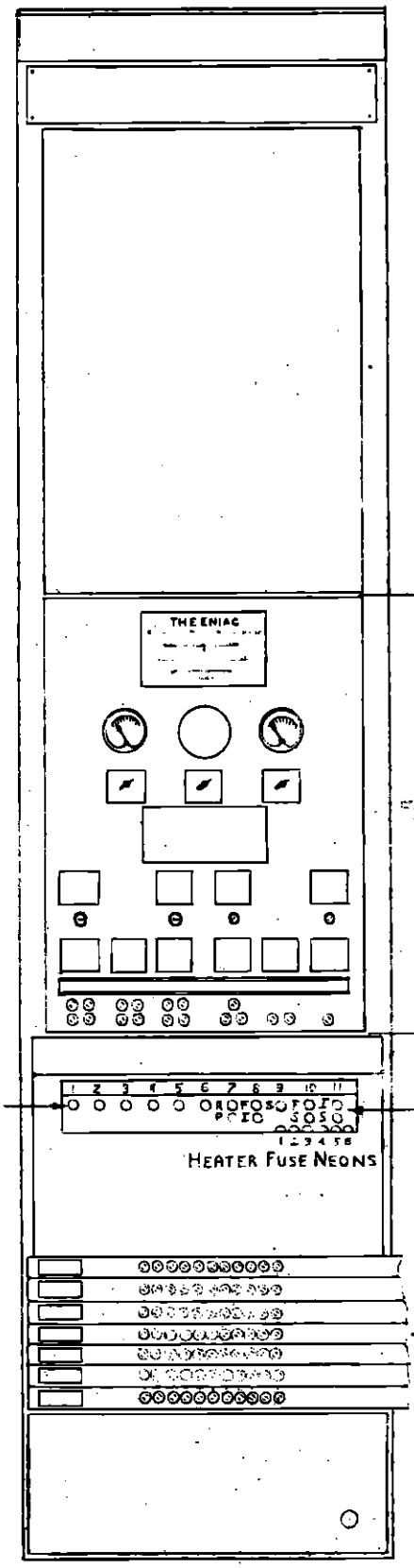
1.5.3. Special Test Equipment

A number of special testing devices are used with the ENIAC. These include a tube tester, a hi-pot test unit, a static tester, and a test table with its own power supplies, synchronizing unit, variable oscillator, and oscilloscope.

The test table and its associated equipment are used to examine the 20 different types of plug-in units. The synchronizing unit, variable oscillator, and a device for varying d-c voltages make it possible to reproduce the operating conditions found in the ENIAC or to generate certain test conditions. The equipment associated with the test table is portable so that it can also be used for testing the ENIAC proper.

The static tester is essentially an adaptor which plugs into the d-c cables so as to make possible measurements of the voltages on tube pins. The hi-pot test unit is used to detect insulation faults in cables. The standard tube tests can be made on the types of tubes used in the ENIAC by means of the tube tester.

In addition to the above special testing devices, the standard electrical measuring instruments are used for the ENIAC. Certain meters have also been built into the initiating unit (see Chapter II) and the cycling unit includes an oscilloscope for rather rough examination of the fundamental train of signals.



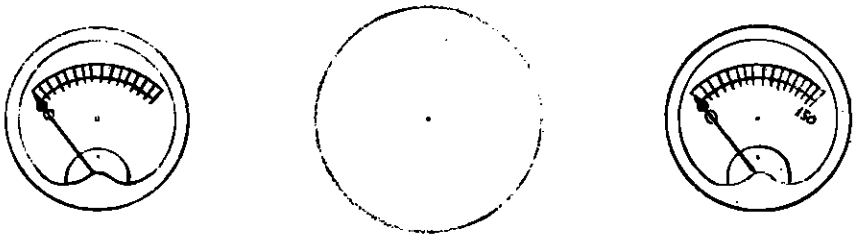
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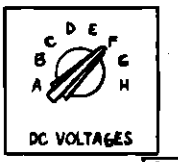
INITIATING UNIT FRONT VIEW
PX-9-305

THE ENIAC

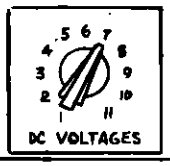
ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTOR

DEVELOPED, DESIGNED AND CONSTRUCTED
BY THE
MOORE SCHOOL OF ELECTRICAL ENGINEERING
OF THE
UNIVERSITY OF PENNSYLVANIA
1944





DC VOLTAGES



DC VOLTAGES



AC VOLTAGES

	1	2	3	4	5	6	7	8	9	10	11
A											
B											
C											
D											
E											
F											
G											
H											

START

STOP

READER START SWITCH

INITIATING PULSE SWITCH

AMBER

GREEN

Back Cover Switch Shunt

INITIAL CLEAR

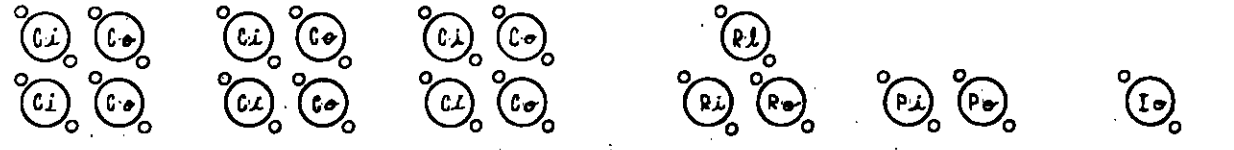
D.C. POWER SUPPLIES

DOOR SWITCH SHUNT

READER
INTERLOCK INPUT OUTPUT

PRINTER
INPUT OUTPUT

INITIATING PULSE
OUTPUT



Ci - pulse input terminal for selective clearing.
Co - pulse output terminal for selective clearing

Rl - pulse input terminal for reader interlock signal.
Ri - pulse input, terminal for reader.
Ro - pulse output terminal for reader

INITIATING DEVICE
FRONT PANEL
PX-9-302 B

II. INITIATING UNIT

The initiating unit of the ENIAC is the device which contains controls for turning the power on and off, for initiating a computation, for initial clearing, and for selective clearing a group of accumulators, as well as program controls for the reader and printer. Certain devices for testing the ENIAC are also located on the initiating unit.

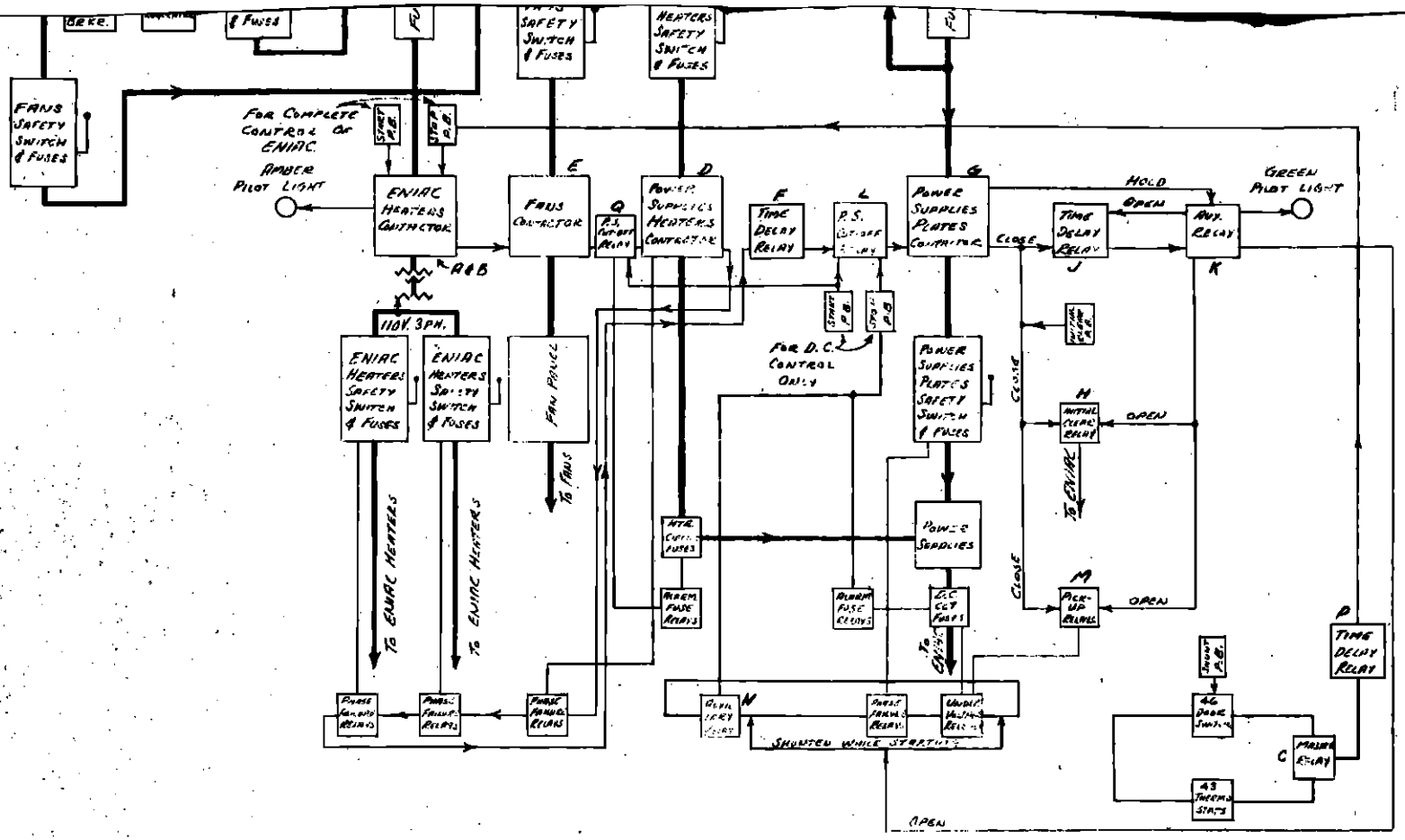
The following topics are discussed in this chapter: Section 2.1, starting and stopping the ENIAC power and initial clearing; Section 2.2, reader and printer program controls on the initiating unit; Section 2.3, initiating a computation; Section 2.4, selective clear program controls; and Section 2.5, testing features. The following drawings are referred to in this section:

Initiating Unit - Front View	PX-9-305
Initiating Unit - Front Panel	PX-9-302
Cycling Unit and Initiating Unit Block Diagram	PX-9-307
Power System Block Diagram	PX-1-303
A-C Power Distribution Rack	PX-1-304

2.1. STARTING, STOPPING AND INITIAL CLEARING

Nearly all the characteristic functions of the ENIAC depend on d-c power. This, however, is derived from 240 volt, 3 phase, a-c. The latter has some immediate uses in addition to furnishing the d-c. There are in all five principal uses for the a-c power. These are as follows:

1) for the heaters of the numerous tubes of the ENIAC units.
2) for the heaters of the rectifier tubes in the ENIAC's power supplies which convert a-c into the different d-c voltages.



Switch added in Line To Power Supplies Filament Contactor	1	P & Q added. All Heater Phase Failure Relays Revised	3
J. Cummings 7-30-45		J. Cummings 3-4-46	
P.G. Street & Stop Push Buttons added. Location of all Protective Devices Referenced.	2	Nomenclature Revisions	4
J. Cummings 11-23-45		J. Cummings 4-25-46	

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Power System Block Diagram

Material	Finish	Scale
—	—	—

Drawn by:	Checked by:	Approved by:
J. Cummings 7-9-45	J. Cummings 7-9-45	

PX-1-303

3) for the plates of the rectifier tubes.

4) for the fans which dispel the great amount of heat generated by the preceding

5) for the control circuits needed in starting and stopping the ENIAC power, in furnishing protection to various circuits, and in initial clearing.

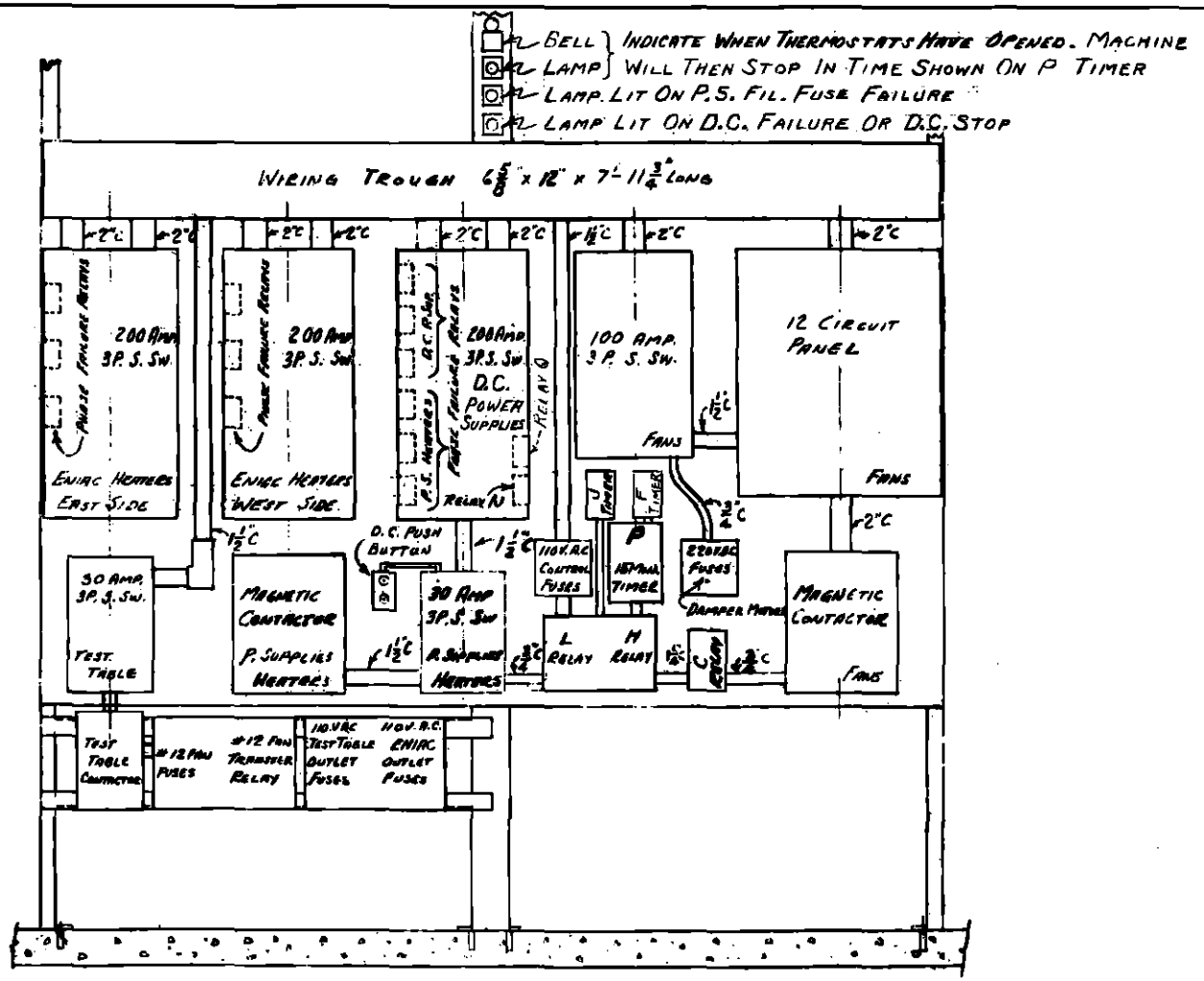
The first four items referred to above are identified by the corresponding numbers on PX-1-303. The last item is noted there as control circuits and is more explicitly dealt with on PX-9-307. The control circuits govern the connection of the other items to the a-c lines, cause d-c to be supplied to the units of the ENIAC, and control the initial clearing of these units.

Program controls for these circuits are found on the initiating unit. Other auxiliary program controls and elements of the control circuits are found on the power distribution rack, the condenser cabinets, and the units of the ENIAC themselves. In this section we shall discuss the events involved in starting and stopping the ENIAC (Section 2.1.1.) and in initial clearing (Section 2.1.2.)

2.1.1. Starting and Stopping the ENIAC

In this discussion it is assumed that the main a-c safety switch is closed. By a "safety switch" is meant one whose opening not merely cuts off power, but actually opens all lines of the circuit controlled by the switch. We also assume here that the 2 safety switches for the ENIAC heaters and those for the fans and for the heaters and plates of the power supplies are all on. With the last 2 switches off, only the a-c circuits can operate; with any of the others off, neither a-c nor d-c can.

When the start button on the initiating unit (see PX-9-302) is



REVISIONS

F & P TIMERS REVISED. 2 RELAYS, INDICATING LAMPS & BELL ADDED. J. Cummings 1-30-46 1

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A. C. POWER DISTRIBUTION RACK

MATERIAL	FINISH	SCALE
/	/	

Drawn by	Checked by	Approved by:	
J. CUMMINGS 12-21-45	J. CUMMINGS 12-21-45		PX-1-304

depressed, the amber pilot light goes on immediately and the following sequence of events takes place: the ENIAC heaters and the power supply heaters are connected to the a-c and the ventilating system is turned on. One minute later, after the heaters have had an opportunity to warm up, the plates of the power supply tubes are connected to the a-c. Simultaneously, initial clearing, which lasts for 10 seconds, begins. After the ENIAC has been initially cleared, the green pilot light on the initiating unit goes on and the ENIAC is ready to operate.

The heaters clock on the front of the initiating unit, which keeps count of the number of hours that the power supply heaters are on, starts to record as soon as the start button is pushed. On each of the remaining 39 panels of the ENIAC, there is also a heaters clock and an on-off switch for the heaters. When the a-c is turned on, the heaters in a panel go on only if the switch for that panel is in the "on" position. The associated heaters clock records the number of hours that the heaters of the panel are turned on.

Before a more detailed discussion of the starting sequence is given, the elements involved in various phases of starting will be pointed out on the schematic diagram of the a-c control circuits shown on PX-9-307. The elements enclosed within the heavy lines are not in the initiating unit. The 28 under-voltage release relays and their 14 associated pick-up relays (designated by M) are located in the condenser cabinets. In the Moore School installation the power supply heater fuse relays and the d-c fuse relays are in a cabinet beside the d-c fuse cabinet and relays A, B, and, K are located in the machinery laboratory. The remaining items, except for the door switches and thermostats which are in the ENIAC panels, are on the power distribution rack in the ENIAC room (see PX-2-304).

Relays A and B connect the heaters of the ENIAC units to the 3 phase a-c power. Relay D is the power supply heaters contactor. F, an adjustable timer which has been set for 1 minute, provides for the delay between the turning on of the power supply heaters and plates. When timer F has counted the specified period of time, relay G is activated. This relay connects the plates of the power supplies to the a-c so that the d-c is turned on when relay G is activated. Timer J which has been set for 10 seconds and relay H, the main initial clear relay, are activated after the d-c is turned on. Relays 3 and 4, auxiliary initial clear relays, are each responsible for the emission of one of the signals involved in initial clearing (see Section 2.1.2.). Ten seconds after timer J starts to count, relay K is activated and the initial clear period is terminated, thus bringing the starting sequence to an end.

It can be seen on PX-9-307 that in addition to the start and stop buttons on the initiating unit which operate both the a-c and d-c circuits, separate d-c start and stop buttons have been provided. Through the use of the d-c stop button, only the d-c circuits (controlled by relay G), can be turned off, leaving the a-c circuits unaffected. With the a-c power on, pushing the d-c start button connects in the d-c circuits and causes initial clearing to take place. Isolation of the d-c from the a-c circuits has been provided in order to make possible leaving the heaters turned on even when the ENIAC is not to be operated or when there is a failure (see the discussion of protective circuits below) in the d-c circuits. This has been done because it is hoped that, by cutting down the number of times that the heaters are turned on and off, tube life will be lengthened.

It is to be noted that the operation selector switch on the cycling unit must be set at continuous when the power is turned on. In Section 2.1.2.

where initial clearing is discussed, it is pointed out that when the power is first turned on, a number of flip-flops may come up in the abnormal state and it is also remarked that the resetting of these often depends on the pulses and gates emitted by the cycling unit. These pulses are not given out immediately unless the ENIAC is in continuous operation. The danger of having these flip-flops remain in the abnormal state is that, as a result, a number of tubes that should be off most of the time and on only a short period of time (i.e. tubes in circuits that have been designed for a low duty cycle) remain on for a long time and thus cause damage to themselves and other elements.

Certain protective devices included in the control circuits are also shown on PX-9-307. Of these the most important are relays C, Q, N, and L. The action of these will be discussed in the following paragraphs. Their distinguishing characteristics are as follows: under proper operating conditions C and N are on; L and Q are off. C may be turned off by a thermostat or a door switch. Since it is believed undesirable to turn off the heaters unless it is absolutely necessary, C acts through a timer P which may be set between 5 and 15 minutes. When this time has elapsed and the trouble has not been remedied, both a-c and d-c circuits are turned off. The other three relays act without any delay but affect only the d-c. Relay Q is turned on by the blowing of any heater fuse. This cuts off the d-c power supply including its heaters. Relay N is turned off by phase in the plate supply or under-voltage in the output of a d-c power supply. The effect is to turn on L. This is also accomplished by the d-c stop button or the failure of a d-c fuse. When L is turned on or when there is any phase failure in the heaters, the plate supply to the rectifiers is cut off, but the heaters are left on. The distinction between N and L is that there is a provision for inhibiting the action of N during starting. These actions will

now be discussed in more detail.

Relay C is a master relay which controls both a-c and d-c circuits. This relay, which is activated when the a-c safety switch is closed, operates in conjunction with the door switches (see below), thermostats, and timer P. Found at the back of each ENIAC panel and at the front of the power supply and condenser cabinets, is a door switch. When the cover of a panel or cabinet is removed, the door switch on the panel opens,* causing relay C to be deactivated. If, however, the door switch shunt button on the initiating unit (see PX-9-302) is held down while the cover is off, relay C is not deactivated. Relay C is also deactivated when a thermostat opens as a result of the overheating of a unit. When relay C is not activated contact C_1 closes and timer P which is set for 5 minutes starts to operate. First its clutch (CL) is thrown in, and next the motor (M) is connected into the circuit through contact CL_1. A warning lamp above the power distribution rack (see PX-1-304) also lights. Necessary repairs can be made on the machine during this 5 minute period, (which may be adjusted to as much as 15 minutes if more repair time is required). If, at the end of 5 (or 15) minutes, the condition which caused relay C to be deactivated has not been corrected, then contact P_1 opens and relay A is deactivated. This turns off both the a-c and d-c circuits. The start button on the initiating unit is used to turn the power on again after the fault has been corrected.**

The door switches have been provided as a safety measure for both personnel and the machine since the opening of a panel exposes dangerous voltages

*At the present time, there is a permanent shunt for the door switches so that removing a cover does not cause relay C to be deactivated. The description in the text above applies to the intended method of operation of the door switches.

**If both the amber and green pilot lights are off, the start button on the initiating unit must be used. If only the green pilot light is off, the power may be turned on through the use of the d-c start button.

(as much as 1500 volts in the case of the d-c) and also, by drawing air from the ventilating system to the open panel, may cause another unit to overheat.

Relay Q protects the d-c circuits and the power supplies. When Q is activated, contact Q_1 opens so that relay D is de-energized. This turns off the power supply heaters and causes contact D_1 to open. With contact D_1 open, F is de-energized so that contact F_1 opens and relay G, the d-c contactor is deactivated. Relay Q is activated when a contact on one of the power supply heater fuse relays closes. This latter event takes place if a power supply heater fuse blows. If the d-c is turned off because Q has been activated, the d-c start button on the power distribution rack must be used to turn the power on again.

The remaining protective devices shown on PX-9-307, relays L and N with their associated devices, control only the d-c circuits, leaving all heaters turned on in case of a failure. If one of these circuits detects a failure and turns the machine off, the power can be turned on again through the use of the d-c start button. The main and power supply heater phase failure relays connected in series with timer F detect faults in the three phase which goes to the heaters of the ENIAC and of the power supplies. These phase failure relays are activated so that the contacts shown on PX-9-307 are closed under proper operating conditions. In the event of a phase failure, F is de-energized so that contact F_1 opens and relay G drops out. As soon as the fault is repaired, timer F is again activated and, one minute later, contact F_1 closes.

Relay L is the d-c cut-off relay. When this relay is activated, contact L_1 opens so that relay G is de-energized. This results in cutting off the d-c power. With the a-c on (so that contact A_4 is closed), relay L can be picked up through the closing of the d-c stop button, the activation of the d-c

fuse relays when a d-c fuse blows, or the non-activation of relay N (see the discussion of relay N in the next paragraph).

Relay N operates in conjunction with the power supply phase failure relays and the under-voltage release relays. The power supply phase failure relays in this circuit detect faults in the three phase a-c which goes to the plates of the power supply tubes. These relays are activated and their contacts closed under proper operating conditions. There is an under-voltage release relay for each power supply. During the starting sequence while initial clearing takes place, relays M are activated. These relays provide the high voltage required to pick up the under-voltage release relays. After the starting sequence is completed, the under-voltage release relays remain activated and their contacts are closed unless the voltage emitted by a d-c power supply drops below a specified level. During the initial clear period while the under-voltage release relays are being picked up, contact K_2 of relay K provides a circuit which shunts the under-voltage release relays and the power supplies phase failure relays.* Thus, relay N is activated and contact N_1 is open at all times unless a fault is selected.

The starting sequence which takes place when the start button in the initiating unit is pushed is described chronologically in Table 2-1. In some cases, a contact is classified as both a pick up and hold contact for a circuit, since the contact must close for the circuit to operate and since the circuit continues to operate only so long as the contact remains closed. In other cases, the pick up and holding functions are performed by separate contacts.

When the stop button on the initiating unit is pushed, the ENIAC is

*Timer J should not be set for less than 10 seconds since this delay is required when turning the d-c on to permit the under-voltage release relays to pick up before the shunt across them is removed.

TABLE 2-1

CHRONOLOGICAL DESCRIPTION OF STARTING SEQUENCE

Activated Relay or Circuit Element	Pick Up Contact (contact whose closing causes circuit to operate)	Hold contacts (Contacts which must remain closed for circuit to continue to operate).
A-auxiliary start relay	Start switch - closed when start button is pushed	Stop switch - normally closed P_1 - closed unless timer P has been activated for 5 minutes.* B_1 - closes immediately after A is activated.
B-main start relay and ENIAC heaters contactor.	A_1	A_1 B_1
E-fans contactor	A_3	A_3
D-power supply heaters contactor	E_1	E_1 Q_1 - closed unless Q is activated.*
Amber start pilot and power supply heaters. clock.	A_4	A_4
F-one minute timer	D_1	D_1 Main and power supply heaters phase failure relays - closed unless a fault is detected.*
G	F_1 - closes after F has counted out 1 minute	F_1 L_1 - closed unless L is activated.*
H-Main initial clear relay J-10 sec. timer M-under voltage release pick-up relays	G_1	G_1 K_4 - closed until K is activated.
K-relay which terminates initial clear period.	J_1 - closes after timer has counted 10 seconds.	K_1 G_1 Initial clear switch - remains closed unless I.C. button is pushed.
Green ready pilot	K_3	K_3

*See discussion of protective devices included in Section 2.1.1.

completely turned off. Relay A, then B, E, D, G, H, and K are de-energized.

When only the a-c circuits are on, and the d-c start button is pushed, the following events take place: Relay L is deactivated, and through contact F_1 (closed provided that the a-c is on and there is no phase failure in the power for the ENIAC and power supply heaters) and L_1 (closed when L is deactivated), relay G is picked up. This turns the d-c on and then initial clearing follows as indicated on Table 2-1.

When the d-c stop button is pushed, relay L is activated. Since contact L_1 then opens, relay G drops out and the d-c is disconnected. Contact G_1 also opens, causing relay K to drop out.

With regard to the matter of interrupting a computation, it might be pointed out that it is not necessary to push the stop button on the initiating unit or the d-c stop button for this purpose. Even though the power is turned on, a computation can be stopped in a number of different ways. If a program cable which delivers a program output pulse to a program tray is removed, the computation in progress ceases with the program whose program output pulse is eliminated in this way. If the card reader exhausts the cards in its magazine (see Section 8.3.) the computation is terminated with the program just before the one in which reading would take place. A computation ceases, similarly, when the cards in the magazine of the card punch are exhausted (see Section 9.1.).

2.1.2. Initial Clearing

When the ENIAC is turned on, it is a matter of chance as to which flip-flops in the various counters, both numerical and program ring, or which program flip-flops (in receivers, transceivers and common programming circuits) will come up in the abnormal state. It is obvious that a computation must start with the numerical and program rings in the clear position and with program

flip-flops in the normal state in order that the correct answer may be obtained. Furthermore, if a flip-flop in a transceiver or a program control flip-flop such as the printer start flip-flop (see Section 9.1.) comes up in the abnormal state, not only is the associated program commenced, but also, upon the completion of the program, an output pulse is transmitted which, in turn, may stimulate another program control, etc. Thus, it is also necessary before starting a computation to break program chains or sequences which are accidentally begun when the ENIAC is turned on. Furthermore, it is convenient to be able to stop a computation at a certain point (without turning the ENIAC power off), erase all data stored in accumulators and the master programmer, and then start afresh.

The initial clear circuits in the ENIAC provide for the contingencies mentioned above. The initial clear circuits consist of the initial clear push button on the initiating unit, relays H and K which were referred to in Section 2.1.1. and initial clear relays 3 and 4 (see PX-9-307). When the ENIAC's power is turned on, initial clearing takes place automatically immediately after the d-c goes on (see Section 2.1.1.). The initial clear push button is pushed when, with the power already on, it is desired to clear the accumulators and the master programmer. It is to be noted, that the operation selector switch on the cycling unit must be set at continuous for initial clearing to take place. Relay H is the main initial clear relay. When activated, this relay causes initial clearing to take place. Relay K terminates the initial clear period. Initial clear relay 4 is responsible for emitting the initial clear gate (ICG) which, in general, clears the counters used for either numerical or programming purposes. Initial clear relay 3 causes the master programmer clear gate (MPC) to be emitted. The MPC is used in the master programmer to break program sequences (see the discussion in the latter part of this section.)

When the start button on the initiating unit or the d-c start button is pushed, relay K is not activated so that relay H and the ten second timer J are picked up through contacts G_1 and K_4. At the end of 10 seconds, contact J_1 on the timer closes. Through J_1, relay K is picked up. From then on, relay K holds through contact K_1 and the initial clear switch which is normally closed.

When the power has been on and the initial clear button is pushed, relay K is de-energized so that K_4 closes. Since G_1 remains closed as long as the d-c is on, relay H and timer J are then picked up through G_1 and K_4.

When relay H picks up, contact H_1 closes, thus activating relay 3. Contact 3-1 then closes and the MPC is emitted. As a result of the activation of relay 3, contact 3-3, which is normally closed, opens, Now with 3-3 closed, there is a circuit which allows a small amount of current to flow through the coil of relay 4 but not enough to pick this relay up, and very little passes through the large resistor to the condenser. While 3-3 is open, however, the condenser is charged.

Ten seconds after relay H is activated, K is activated. Contact K_4 opens and H is, thus, deactivated. This causes contact H_1 to open and relay 3 to drop out. At this time, contact 3-3 closes. This allows the condenser to discharge through the coil of relay 4. In this way, relay 4 is activated and contact 4-1 is closed. With contact 4-1 closed, the initial clear gate is emitted. Initial clear relay 4 is restored to the normal state with contact 4-1 again open in about 1/2 a second when the condenser has discharged.

As can be seen from the discussion above, the 10 second period (when the green light is off and when timer J is operating) designated by the phrase initial clear period, is actually devoted to the master programmer clear signal. The initial clear gate comes on after the MPC goes off and lasts for about 1/2

TABLE 2-2 - INITIAL CLEARING OF ENIAC UNITS

UNIT	ITEM	MANNER OF INITIAL CLEARING OR RESETTING
Accumulator	Flip-flops in receivers and transceivers.	No provision for direct reset of receivers or transceivers. However, if a F.F. comes up in the abnormal state, the program set up on the associated switches is carried out and, in a maximum of 9 add. times, the F.F. is reset.
	Decade flip-flops	Normally negative output of decade F.F. gates RP through gate 18 so that a decade F.F. in abnormal state is reset.
	Repeater ring	CPP gated through E50 by ICG resets repeater ring.
	Decade counters and PM counter	CCG gated through E44 by ICG clears counters.
Multiplier	Flip-flops in transceivers	Reset in maximum of 14 add. times (see Accumulator).
	Program ring	If program ring is not in stage 1, CPP is gated through J'44. ICG holds G'44 open so that output of J'44 is passed to prog. ring. Thus the ring is cycled to stage 1. When prog. ring is in stage 1, J'44 is closed so that no other CPP are admitted to cycle the ring.
	Reset flip-flops	Normally negative output of a reset F.F. which comes up in abnormal state opens G49 or L'50 so that a CPP is passed to reset the F.F.
	L and R receivers	ICG gates CPP through E'47 to reset these receivers.
	Ra-Rε, Da-Dε, and answer disposal receivers	Reset by CPP.
Divider and Square Rooter	AT PRESENT, ICG gates a CPP through E50. The output of E50 gives rise to CL and CL' pulses so that clearing is accomplished as follows:	
	Flip-flops in transceivers	No provision for direct reset, since the reset signal from transceivers in the divider comes from the clear F.F. and the present method of init. cl. does not ensure that the clear F.F. will be set during init. cl. Since a divider program may last longer than init. cl. finishing a program cannot be depended on for resetting program controls in this unit.
	Program ring	Cleared to stage A by CL' signal.
	Pulse source flip-flop	Reset by CL'.
	D'_γ, +1, and -1 receivers	Reset by CL'.
	Program ring flip-flop	Reset by CL.
	Numerator Binary Ring	Cleared to stage P by CL.
	Denominator flip-flop	Reset by CL.
	Answer Place Ring	Cleared to stage 1 by CL.
	Clear flip-flop	Reset by CL.
	Interlock flip-flop	Reset by CL' gated through E48 by ICG.
	Interlock coincidence flip-flop	NOT RESET by the present method.
	S_{AC}, N'_γ, S_α, N_{AC}, D_γ, Q_α, +2, -2 answer disposal and argument accumulator receivers.	Reset by CPP.
	N_γ, D_A, D_S	Reset by GP emitted after pulse source flip-flop is reset.
	It is planned to modify the design of the divider in such a way that the interlock coincidence F.F. will be eliminated and also so that the transceivers will be reset during the init. cl. period.	
Function Table	Flip-flops in transceivers	Reset in a maximum of 13 add. times (see Accumulator).
	Argument flip-flop and Add. and Sub. flip-flops	Reset by CPP gated through C48 by ICG.
	Program ring	Cleared to stage -3 by CPP gated through B48 held open by ICG.
	Units and tens argument counters	Cleared by CPP gated through A48 by ICG.
Constant Transmitter	Flip-flops in transceivers	Reset in 1 add. time (see Accumulator).
Reader	Start flip-flop	Reset by CPP gated through 63 by ICG.
	Interlock flip-flop Finish flip-flop Synchronizing flip-flop	Reset by CPP gated through 71 by ICG.
Printer	Start flip-flop	Reset by CPP gated through 71 by ICG.
	Finish F.F. is set by CPP gated through 71 by ICG. Then GPP gated through 66 sets synchronizing F.F. Normally negative output of synchronizing F.F. gates CPP through 69 so that: Finishing and Synchronizing flip-flops are reset by the output of gate 69.	

Under the present method of initial clearing, a card may be fed to the reader or punch in the period between the turning on of the power and the resetting of the start flip-flop.

Master Programmer	MPC holds stepper output gates closed so that master programmer cannot emit a program output pulse.	
	Stepper input flip-flops	Reset by CPP gated through 69 if F.F. is in abnormal state.
	Stepper Counters	Cleared to stage 1 by CPP gated through C47 by ICG.
	Master programmer decade counters	Cleared to stage 0 by CPP gated through B44 by ICG.

a second. Both the MPC and ICG are carried to the other units of the ENIAC in the d-c voltage cable.

At the time of writing of this report, the MPC is taken only to the master programmer's stepper output gates (see Section 10.3.1.). The MPC, a negative signal closes down these gates so that no program output pulse can be emitted by the master programmer while the MPC is on. Although a program sequence may be initiated because the flip-flop of some transceiver comes up in the abnormal state, it is impossible for a program sequence lasting 10 seconds (of continuous operation) not to go, at some time in that period, to the master programmer. Since the master programmer, however, cannot transmit a program output pulse while the MPC is on, program sequences which have started accidentally are broken here.

The way in which the initial clear gate is used in the units of the ENIAC to prepare them for computation is shown on Table 2-2. The reader will probably find it convenient to refer to this table in connection with Chapters IV-X. The circuit elements referred to in Table 2-2 can be identified on the block diagrams for the various units. The reader will notice that in many cases clearing depends on the carry clear gate and the central programming pulse emitted by the cycling unit. It is for this reason, that the cycling unit must be in continuous operation for initial clearing to be accomplished.

On Table 2-2, two difficulties inherent in the present method of initially clearing the divider and square rooter are noted. One of these difficulties, that the flip-flops in the transceivers may not be reset by the end of the initial clearing period, arises from the fact that in the divider and square rooter, as in the other units of the ENIAC, no special provision has been made for directly resetting the transceivers. In other units of the ENIAC, this causes

no difficulty. For, suppose that a transceiver in the high-speed multiplier comes up in the abnormal state when the power is turned on. The multiplier then proceeds, during the time that the MPC is on, to carry out the program set-up on the switches associated with that transceiver. In a maximum of 14 addition times the program is completed and the transceiver is reset.

In the divider and square rooter, however, there is no upper limit on the length of time required for a division program (division by zero, for example, requires an infinite length of time). Therefore, if a division program is started because a transceiver comes up in the abnormal state when the ENIAC is turned on or because an accidentally begun program sequence stimulates it, there is no certainty that the program will be completed and the transceiver be reset by the end of the initial clear period.

Plans have been made to revise this initial clearing difficulty by causing the clear flip-flop in the divider and square rooter to be <u>set</u> during the initial clear period. Since the clear flip-flop in the abnormal state causes the CL and CL' signals to be emitted, any flip-flops now reset by CL and CL' will also be reset by the modified method of initial clearing. The CL signal also resets the clear flip-flop. The normally negative output of the clear flip-flop provides a reset signal for the divider and square rooter's transceivers.

Until the initial clearing process for the divider and square rooter is modified, the operator can circumvent this first difficulty by setting the operation switches on this unit at square root instead of divide and the interlock switches at NI (no interlock). Since the maximum time for a square rooting program is 400 addition times (less than a tenth of a second), an accidentally begun square rooting program is certain to be completed by the end of the initial clear period. The reason for setting the interlock switches on the program

controls at NI is that, even though a program were completed, a program output pulse would not be emitted and the transceivers would not be reset unless the interlock flip-flop also came up in the abnormal state or unless some program sequence, accidentally started, provided for an interlock pulse.

The second difficulty, that no provision has been made for resetting the interlock coincidence flip-flop, is also to be remedied. Plans have been made for making a small modification in the divider and square rooter's common programming circuits which will eliminate the need for this flip-flop. Until this modification is made, the operator must pay particular attention to the interlock coincidence flip-flop neon (see PX-10-302) before starting a computation. When the interlock coincidence flip-flop is in the normal state, this neon is off. If this flip-flop comes up in the abnormal state at the end of initial clearing, initial clearing should be repeated until this flip-flop does come up in the normal state.

2.2. READER AND PRINTER PROGRAM CONTROLS ON THE INITIATING UNIT

2.2.1. Reader Program Controls

Certain reader program controls are found on the initiating unit (see PX-9-302 and 9-307). These include the reader start flip-flop and program pulse input terminal (Ri), the reader interlock flip-flop and interlock pulse input terminal (Rl), the reader finish flip-flop, the reader synchronizing flip-flop and program pulse output terminal (Ro), and associated gates, buffers, and inverters. The reader start button is also on the initiating unit.

The reader start flip-flop is flipped into the abnormal state either when Ri is pulsed or when, at the beginning of a computation (see Section 2.3.), the reader start button is pushed. When the start flip-flop is in the abnormal

state, a start relay in the constant transmitter is activated so that the reader is stimulated to read a card and cause information read from the card to be stored in the constant transmitter. A little less than half way through the card reading cycle (see Chapter VIII), a reset signal from the reader resets the start flip-flop, so that, even though reading is not yet completed, the start flip-flop is capable of again being flipped into the abnormal state (by the reception of a pulse at Ri) to remember that reading is to take place again.

When reading is completed, the reader emits a finish signal which causes the reader finish flip-flop to be flipped into the abnormal state. The interlock flip-flop is flipped into the abnormal state when an interlock pulse arrives at Rl or, at the start of a computation, when the reader is stimulated to read by the reader start button. The reader interlock flip-flop makes it possible to carry on a sequence of programs in parallel with reading and then to stimulate the next program sequence when both reading and the parallel sequence have been completed since no program output pulse is emitted from terminal Ro unless the interlock flip-flop is flipped into the abnormal state (see below). If a computation does not call for a sequence in parallel with reading, the operator can provide an interlock pulse by sending the pulse which goes to Ri also to Rl.

The coincidence of signals from the interlock and finish flip-flops causes gate 69 to emit a signal. The output of gate 69 gates a CPP through gate 62 which then sets the reader synchronizing flip-flop. The CPP gated through 68 by the normally negative output of the synchronizing flip-flop gates a CPP through 68 and, thus, provides a reader program output pulse which is emitted from terminal Ro. The reason that the synchronizing flip-flop and gate 68 are used after gate 62 is to ensure a program output pulse of the proper

shape and in synchronism with other program pulses.

Neons correlated with the flip-flops mentioned above are shown on PX-9-305. Program controls for the reader in addition to those on the initiating unit are discussed in Chapter VIII.

2.2.2. Printer Program Controls

The printer program controls on the initiating unit include the printer start flip-flop and program pulse input terminal, the printer finish flip-flop, the printer synchronizing flip-flop and program pulse output terminal, and associated gates, buffers, and inverters. Neons correlated with the flip-flops appear on PX-9-305.

A program input pulse received at Pi flips the printer start flip-flop into the abnormal state. This causes a start relay in the punch to be activated so that the tubes in the printer are set up for the data to be printed and so that a card punching cycle is initiated (see Chapter IX). About 1/4 way through the card punching cycle, the punch emits a finish signal which resets the start flip-flop and sets the printer finish flip-flop. The output of the finish flip-flop in the abnormal state gates a CPP through gate 66. The output of 66 sets the printer synchronizing flip-flop whose output gates a CPP through gate 69. The output of gate 69 is transmitted from PO as a program output pulse.

The printer program controls are discussed in greater detail in Chapter IX.

2.3. INITIATING PULSE FOR A COMPUTATION: Reader Start Button and Initiating Pulse Button.

Once the starting sequence is completed (amber and green pilot lights are on), the ENIAC is ready to begin computing. To stimulate the computation to

begin, however, a program pulse must be delivered to the input terminals of the program controls on which are set up the programs that begin in the first addition time of the computation. Two alternative methods exist for stimulating the beginning of a computation.

If the first event of a computation consists of the reading of a card, the computation can be started by pushing the reader start button on the initiating unit (see Section 2.2.1.). When reading is completed, then, a program output pulse is emitted from terminal Ro. This pulse can be used to stimulate the programs of the computation which immediately follow reading. As was noted in Section 2.2.1, pushing the reader start button also results in setting the reader interlock flip-flop so that no interlock pulse need be provided for a reading initiated by the reader start button.

The terminal marked R_s on PX-9-302 parallels the reader start switch and is used for remote control (see Section 2.2.1.).

The second procedure for initiating a computation is to connect the terminal marked Io (see PX-9-302) to the same program line as the input terminals of the program controls used for the first programs of the computation. When the initiating pulse button is pushed, the initiating pulse input flip-flop (see PX-9-307) is set. Its output allows a CPP to pass through gate 66 and set the synchronizing flip-flop. The output of the synchronizing flip-flop gates a CPP through gate 69 which resets the input and synchronizing flip-flops and causes a program pulse to be emitted from terminal I_o. Neons correlated with the flip-flops mentioned above are shown on PX-9-305.

The initiating pulse button has a second important use in connection with testing the ENIAC. One of the chief techniques for localizing errors in either the machine or the set-up of the machine is to operate the ENIAC in the

one addition time mode or in the one pulse time mode. Here, the pulses for one addition time or 1 pulse time at a time respectively are given out in sequence every time the 1 pulse - 1 addition time button on the cycling unit is pushed (see Chapter III). In this way, there is an opportunity to observe the numerical and programming neons. Frequently, it is more convenient to proceed through a portion of the computation with the ENIAC operating in its normal or continuous mode and then to switch to 1 addition time or 1 pulse time operation than it is to progress through the entire computation non-continuously. This may be arranged by disconnecting the program cable which delivers the pulse used to initiate the programs which are to be examined non-continuously. We call this point where the program cable is removed a break point. When the initiating pulse button is pushed, the computation begins and progresses to the break point. With the necessary switch made in the cycling unit (see Chapter III), computation in the non-continuous mode can be stimulated by delivering the initiating pulse from terminal I_o to the program line from which the program cable was removed. The reader will notice that after the initiating pulse button is pushed, two addition time cycles, one in which a CPP passes through gate 66 and one in which a CPP passes through gate 69, are required before the initiating pulse is delivered.

The emission of the initiating pulse may also be stimulated by remote control. The terminal marked I_s on PX-9-302 is used to parallel the initiating pulse switch with a switch which may be carried anywhere around the ENIAC room and which is connected to I_s via a program line which has no load box.*

*Also see the discussion of the portable control box in Section 11.6.

2.4. SELECTIVE CLEAR CONTROLS

There are 6 selective clear program controls on the initiating unit. Each control consists of a transceiver with a program pulse input (Ci) and output (Co) terminal on the front panel. The six selective clear transceiver outputs are connected in parallel to a line of the synchronizing trunk. When a selective clear transceiver is stimulated, its flip-flop emits a signal called the selective clear gate (SCG). One addition time later, the transceiver is reset by a CPP and a program output pulse is emitted. Neons associated with the selective clear program controls are shown on PX-9-305.

The selective clear gate is delivered by the synchronizing trunk to the 20 accumulators. When the SCG is given out, any accumulator whose selective clear switch is set at SC clears in accordance with the setting of its significant figures switch (see Section 4.2.3.). Notice that selective clearing lasts but one addition time and clears only the decade and PM counters of accumulators. The selective clear feature provides a convenient means of clearing the group of accumulators which store data for the printer (see Chapter IX) after printing takes place (see the illustrative problem discussed in Sections 8.7 and 9.5.).

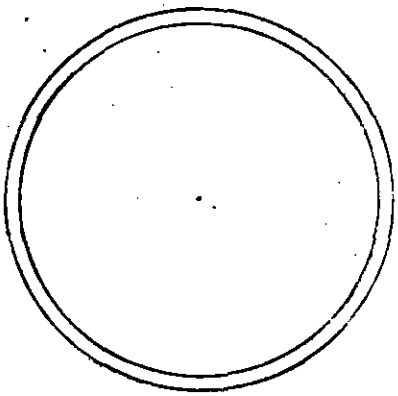
2.5. DEVICES FOR TESTING THE ENIAC

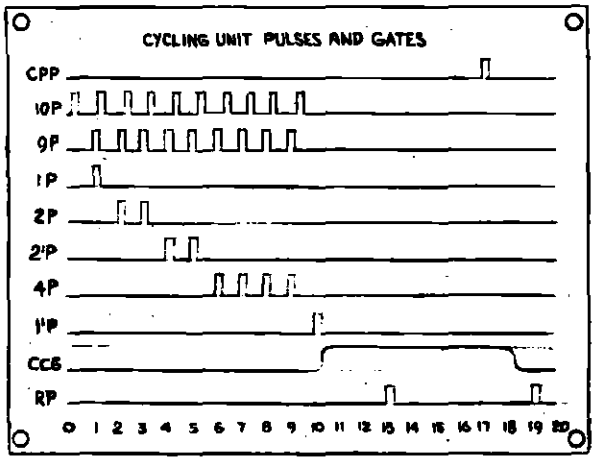
Located on the initiating unit (see PX-9-302) are the following devices for testing the ENIAC: d-c voltage meter and associated voltage selector switches, d-c voltage hum oscilloscope, and a-c voltage meter and voltage selector switch.

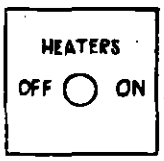
The d-c voltage meter together with the two d-c voltage selector switches provide a means of examining any of the ENIAC's 78 d-c voltages. The

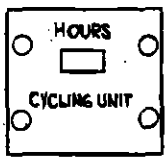
d-c voltage chart below the selector switches indicates which voltage is measured as a result of the combination of settings on the switches.

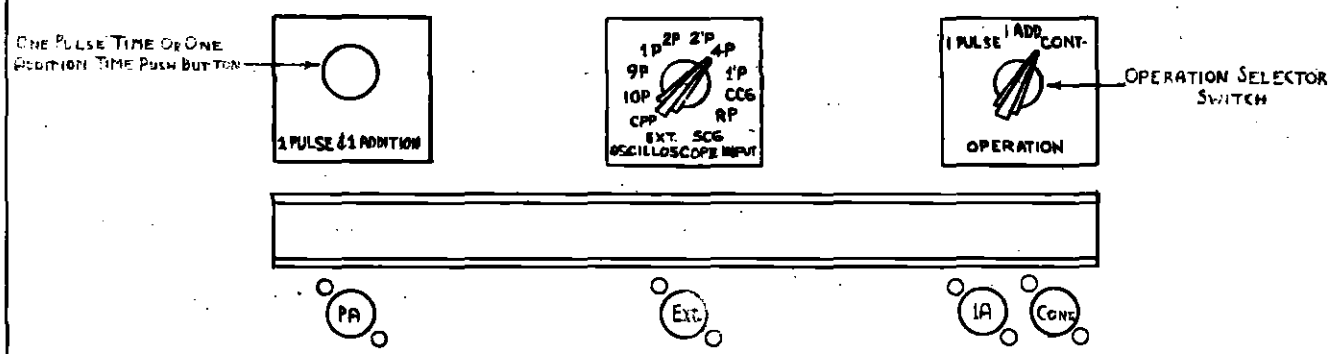
The a-c voltage meter and switch are used to measure the three phases of one of the two bus systems supplying 110 volt a-c to the filament transformers of the various units. Further details concerning the use of the testing devices mentioned above as well as others not located at the initiating unit are to be found in the ENIAC MAINTENANCE MANUAL.









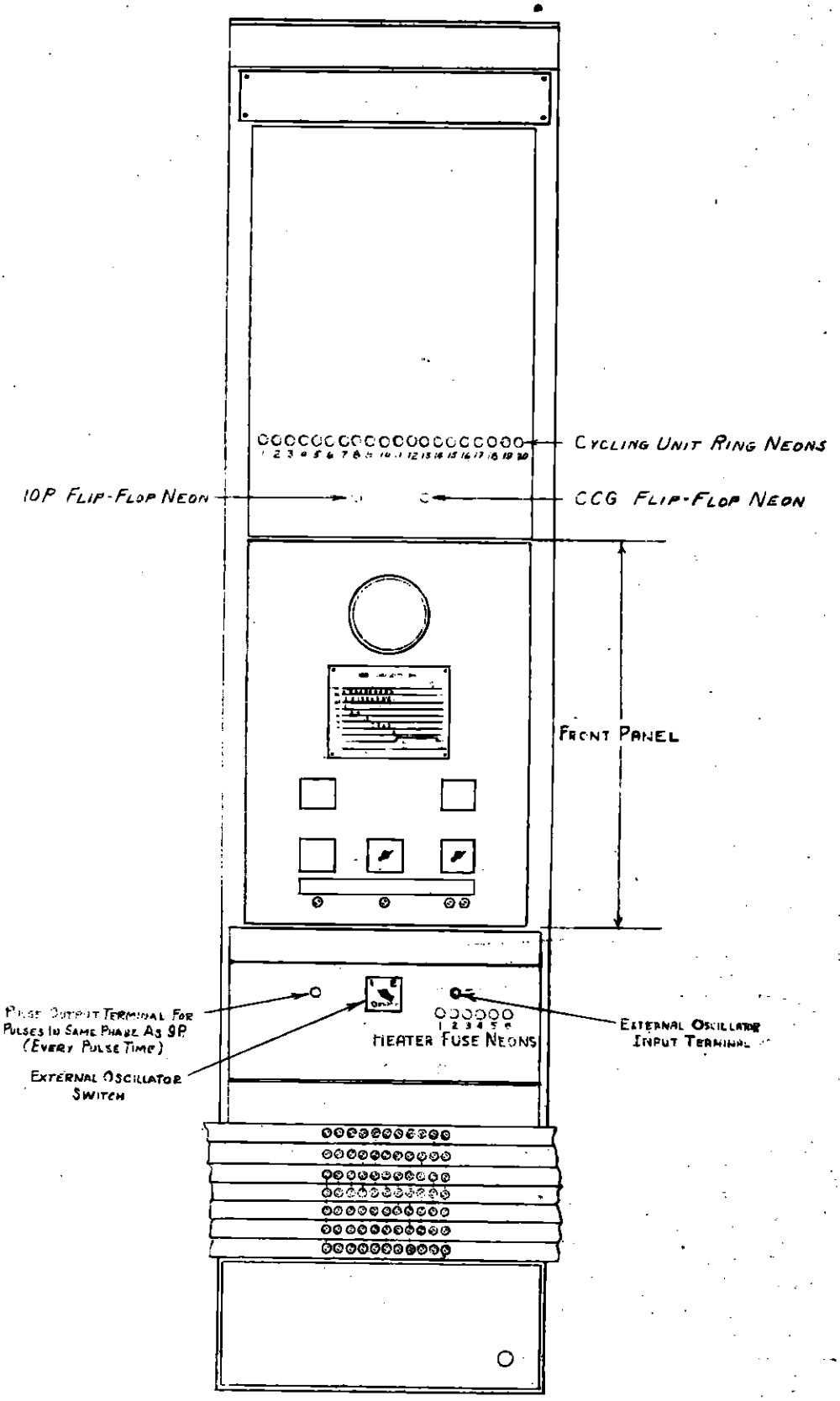


(PA) - Input Terminal For Paralleling One Pulse Time Or One Addition Time Push Button.

(1A) & (CONT) - In Terminals For Paralleling Operation Selector Switch.

(Ext.) - External Oscilloscope In Terminal.

CYCLING UNIT
FRONT PANEL
PX-9-303 R



MOORE SCHOOL of ELECTRICAL ENGINEERING
UNIVERSITY of PENNSYLVANIA

CYCLING UNIT FRONT VIEW
MK-5-304

III CYCLING UNIT

The cycling unit of the ENIAC is the device which provides pulses and a gate for the other units to operate on and which, thus, keeps the units operating in osynchronism with one another.

Normally a quartz crystal oscillator emits 100 kc sine waves which are converted into pulses spaced at a 10 μs interval by a pulse standardizer. The fundamental time unit for the ENIAC, a pulse time, is thus 10 μs. The output of the pulse standardizer goes to the so called on beat circuit which contains another pulse standardizer and tubes for power amplification. The on beat circuit emits pulses (through one of its 3 outputs) to the off beat circuit. The off beat circuit shapes, amplifies and delays the pulses which it receives. One output of the off beat circuit, delayed 1.25 μs after the on beat pulses, is taken to a 20 stage ring counter (neons correlated with the stages of the ring are shown on PX-9-304) which controls certain gates and flip-flops. The off beat pulses, delayed 2.5 μs after the on beat pulses, are taken to a gate which is controlled by a flip-flop, in turn, controlled by the ring. Other gates associated with the ring pass on beat pulses. The ring with its associated flip-flops and gates is responsible for producing a pattern of pulses repeated every 20 pulse times (or every addition time). The gate and each of the 9 different kinds of pulses (see PX-9-306) emitted every addition time are each carried on one of the 11 leads of the synchronizing trunk (see Chapter II for the use of the 11th lead). The various units of the ENIAC are connected into the synchronizing trunk so that they can pick up the pulses needed for their operation.

The pulses generated by the cycling unit or pulses from some external source can be viewed on the screen of an oscilloscope built into the cycling unit.

This chapter will cover the following topics: sources of pulses and gates, Sec. 3.1; methods of operation of the cycling unit and ENIAC, Sec. 3.2;

cycling unit oscilloscope, Sec. 3.3. Reference will be made to the following drawings:

Front Panel of the Cycling Unit	PX-9-303
Front View of the Cycling Unit	PX-9-304
Block Diagram of the Cycling Unit and Initiating Unit	PX-9-307
Cycling Unit Pulses and Gates	PX-9-306

3.1. PULSES AND GATES AND THEIR SOURCES

3.1.1. The Pulses and Gates

The nine different kinds of pulses and the gate emitted by the cycling unit every 200 μs are shown on PX-9-306. The 10P are classified as off beat pulses; all other pulses as on beat. Each of the 10P, 9P, 2P, 2'P, 4P, the 1P, 1'P and CPP are roughly the same in shape and alike in duration (namely, 2 μs). They differ fron one another in the line of the synchronizing trunk over which they are transmitted, the part of the addition time cycle in which they are emitted, and the purposes for which they are used in the ENIAC.

The 9P, the 1'P, the 1, 2, 2', and 4P are commonly used as digit pulses. An accumulator transmits the number stored in it or the complement of the number stored in it by gating appropriate numbers of the 9P over the various lines of the digit output. In the transmission of complements from an accumulator, the 1'P is gated and allowed to pass over the lead which carries the extreme right hand significant figure being stored in the accumulator to make a tens instead of nines complement. The 1, 2, 2', and 4 pulses are used particularly where information stored in static form is converted into pulse form, e.g. in the high speed multiplier, the function table, the divider-square-rooter, and the constant transmitter. By suitable combinations of the 1, 2, 2', and 4 pulses any number between 1 and 9 can be formed. The 10P are used only in accumulators. They serve to cycle each counter around back to the position

it starts from when the transmission of a number and/or its complement from an accumulator takes place (see Sec. 4.3.1).

The carry clear gate (which lasts from pulse time 11 to 17) is used to cause the clearing of accumulators which, at the operator's option, may or may not take place after transmission from an accumulator (see Sec. 4.2.3.). The carry clear gate also allows a carry over pulse to pass from a decade counter to the decade counter immediately to the left if carry over takes place in the reception of a number by an accumulator (see Sec. 4.3.2). Carry over can take place in two ways: delayed or direct. In delayed carry over, the first reset pulse passed through a gate (which is controlled by a flip-flop that remembers that carry over is to take place) is gated by the carry clear gate so that it can reach the next decade. The second reset pulse resets this flip-flop. Direct carry over takes care of carry overs which result from carry over. In this latter form, the pulse which necessitates carry over (and not the reset pulse, as above) is the one which the carry clear gate allows to pass to the next decade counter. The reset pulse is emitted twice, once during the emission of the carry clear gate for delayed carry over and once after the carry clear gate to reset carry over flip-flops which may be set after delayed carry over takes place. The first reset pulse is also used to reset a flip-flop (the same one used for carry over in reception) which is set in the process of transmitting from an accumulator.

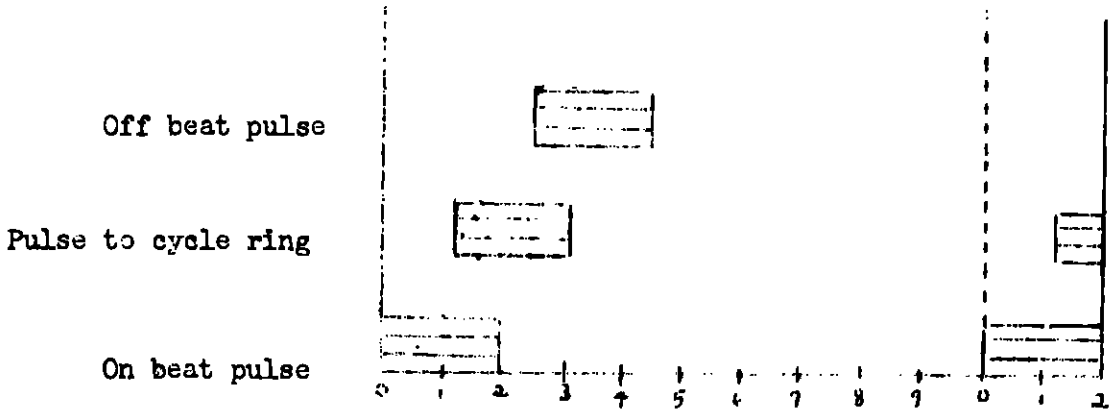
The principal uses of the central program pulse (emitted at pulse time 17) are the provision of the program pulses needed to stimulate program controls and the resetting of the receivers and transceivers in these program controls.

3.1.2. Sources of the Pulses and Gates

A block diagram of the circuits of the cycling unit which are involved in generating the pulses and gates emitted by this unit appears on the left hand half of PX-9-307.

The oscillator (61, 63) emits 100 KC sine waves which the pulse standardizer (K, L26) converts into pulses spaced at 10 μs intervals.

In continuous operation (see Sec. 3.2.) each pulse from the oscillator and pulse standardizer circuit is delivered to the on beat circuit. A special pulse standardizer in this circuit (tubes 61 and 62 and the 1 μs delay line) produces rectangular pulses 2 μs broad. The on beat circuit has 3 outputs. One of the outputs is brought to a terminal labelled on beat pulse output terminal (see PX-9-304). For every pulse received by the on beat circuit, a pulse in phase with the 9P is emitted from this terminal. These pulses are used in the test equipment of the ENIAC (see ENIAC MAINTENANCE MANUAL). Another output of the on beat circuit delivers pulses to gates associated with various stages of the cycling unit ring and the third output delivers pulses to the off beat circuit.



Duration in μs

Figure 3-1

The off beat circuit routes these pulses through a 2.5 μs delay line. This delay line is tapped at half its length, for the pulses which cycle the ring counter. The pulses delayed the full 2.5 μs, called the off beat pulses, are delivered to gate L30 (see Fig. 3-1 for a chronological comparison of the on beat and off beat pulses and the pulses which cycle the ring).

The off beat pulses pass through L30 to produce the 10P as long as gate L30 is held open by the 10P flip-flop (L29) in the abnormal state. This flip-flop is flipped into the abnormal state when the ring counter is in stage zero and remains in this state until reset by a signal from gate A30 (which is controlled by stage 10 of the ring). The 10P neon correlated with this flip-flop is shown on PX-9-304.

Stage 1 of the ring controls gate K30. The on beat pulse passed through gate K30 gives rise to the 1P and the first of the 9P. Stage 2 of the ring controls gate J30. The on beat pulse passed through gate J30 gives rise to the first of the 2P and the second of the 9P, etc. In this way, the 1, 2, 2', and 4P, and the 1'P are generated in the chronological order shown on PX-9-306.

When the cycling unit ring reaches stage 11, gate B27 opens to pass an on beat pulse. This signal sets the carry clear gate flip-flop, E27 (see PX-9-304 for the associated neon). This flip-flop remains in the abnormal state for the next 7 pulse times, being reset by an on beat pulse gated through gate H27 which is controlled by stage 18 of the ring. The signal from the carry clear gate flip-flop in the abnormal state produces the CCG.

While the carry clear gate is on, an on beat pulse gated through gate C27 (which is controlled by stage 13) produces a reset pulse. The second reset pulse is produced when the ring is in stage 19.

A signal from stage 17 of the ring gates an on beat pulse through gate 27 to produce a CPP.

All of the cycling unit pulses and gates shown on PX-9-306 are passed through cycling unit transmitters (61-70, 21-30, or 3-12) for power amplification before transmission from the cycling unit.

It is expected that most of the time the ENIAC's oscillator circuit with its 100 kilocycle rate will be used in the cycling unit. If for any reason it is desired to operate the ENIAC at some other rate, a different

oscillator can be plugged in and used to supply pulses to the on beat circuit. When the oscillator switch (see PX-9-304) is set at Ext. and an external oscillator is plugged into the external oscillator input terminal at the right of this switch, the fundamental pulses for the cycling unit are derived from the external oscillator. When the cycling unit's oscillator supplies the fundamental pulses, the oscillator switch is set at Int. It is to be noted that the time constants for the ENIAC's circuits have been designed for a frequency of 100 KC and certain safety factors have been included on this basis. If a higher frequency is used, these safety factors will be lost so that the reliability of the ENIAC will be decreased.

3.2. METHODS OF OPERATION

The cycling unit can be set up so that the ENIAC operates in one of 3 modes:

1) continuous operation at the fundamental frequency of the oscillator used.
2) one addition time operation in which the cycling unit supplies the pulses for only one addition time cycle at the oscillator rate with a wait of any length desired by the operator between addition times.
3) one pulse time operation in which the cycling unit supplies the pulses of the addition time cycle one at a time with a wait of any length desired by the operator between pulses.

Continuous operation is the natural method of operation of the ENIAC. One addition time or one pulse time operation is used for testing and checking purposes. One addition time operation is particularly useful in checking a set-up that is put on the ENIAC. Before actually running through a complete computation continuously, the operator can cause the ENIAC to progress through one cycle of the computation addition time by addition time. By observing the neon bulbs in the various units, he can then check to see that the units are

operating properly and that switch settings and cable connections have been made correctly to carry out the contemplated set-up. To test whether or not a particular unit is functioning properly, 1 addition time, or, for finer discrimination, one pulse time operation can be used.

The cycling unit controls which are used for the various modes of operation are the operation selector switch and the 1 pulse time-1 addition time push button (see PX-9-303). When the operation selector switch is set at Cont., the cycling unit emits the pulses and gates continuously. When this switch is set at 1 Add, the pulses and gates for 1 complete addition time cycle are given out every time the 1P-1A button is pushed. With the switch set at 1 Pulse, the pulses or gates of the addition time cycle are given out in chronological sequence, one each time the 1P-1A button is pushed. It might be mentioned that all three modes of operation are possible whether the ENIAC's oscillator or an external oscillator is used to supply the fundamental pulses.

Continuous or non-continuous operation is accomplished by allowing all pulses or only certain pulses from the oscillator circuit to reach the on beat circuit (and then the off beat circuit, and the ring with its associated gates). The continuous relay, the 1 addition time relay, gates L 28 and L 27 and the 1 pulse - 1 addition time push button (see PX-9-307) are used for this purpose. It might be pointed out that gate L 27 is connected to the normally positive output of stage zero of the ring. Thus L 27 is closed when the ring is in stage zero and open at all other times.

In continuous operation, the requirements are that the circuit containing gates L 27 and L 28 shall pass all of the pulses from the oscillator and that accidentally pushing the 1 pulse - 1 addition time push button shall have no effect. The requirements are met in the following way: with the

operation switch set at continuous (as shown on PX-9-307) the continuous relay is activated so that contacts 1 and 3 are closed and the 1 addition time relay is not activated so that contact 6 is closed. Now with contact 1 closed, the cathode of tube 70 (at the left) floats and the tube is, therefore, inoperative. Since this tube is not conducting, a positive voltage is applied to gate L 28. The circuit through contact 3 delivers to the pulse standardizer K-L 26 and then to gate L 28 the oscillator pulses which then pass through gate L 28.

When the operation switch is set at 1P or 1A respectively, only the pulse which results from pushing the 1 pulse - 1 addition push button or only 20 oscillator pulses immediately following the pushing of the button are to reach the on beat circuit. Let us, therefore, consider the circuit containing the 1 pulse - 1 addition push button. Tubes 68 are normally on and tubes 69 constitute a flip-flop with but one stable state (a non-standard flip-flop for the ENIAC). The normally positive output of this flip-flop is taken to tube 70 and the normally negative output is used to reset the flip-flop immediately after it is set. When the push button is pushed, tubes 68 go off and the flip-flop is set momentarily; otherwise, this flip-flop remains in the normal state.

When the operation switch is set at 1^P, neither the continuous nor the 1 addition time relay is activated so that contacts 6, 4, and 2 are closed. The circuit through contact 2 connects the cathode of tube 70 (at the left) to -40V so that, with the flip-flop (69) in the normal state, tube 70 is on. The negative output of this tube holds L 28 closed. Only when the push button is pushed is tube 70 turned off so as to open gate L 28. The positive pulse from tube 70 (at the left) also passes through the other tube of the same number and, through contacts 6 and 4, is delivered to the pulse standardizer and, finally, gate L 28.

In 1 addition time operation, contacts 5, 4, and 2 are closed. The circuit through contact 2, as described above, causes gate L 28 to be opened momentarily when the 1 pulse - 1 addition time button is pushed. The circuit through contacts 5 and 4 delivers the oscillator's pulses to the pulse standardizer and the gates L 27 and L 28. The first oscillator pulse passes through gate L 28. This pulse results, finally, in cycling the ring from stage zero to stage 1 so that the subsequent 19 pulses from the oscillator pass through gate L 27. When the ring reaches stage zero again, L 27 is closed and L 28 does not open again unless the 1 pulse - 1 addition button is pushed. In case the cycling unit has been running in the 1 pulse time mode and is switched into the one addition time mode in the midst of an addition time cycle, the pulses and gates for the remainder of the addition time are given out immediately (since gate L 27 is open), whether or not the 1 pulse - 1 addition button is pushed.

Controls are provided which enable the operator to control the method of operation of the cycling unit when he is standing near some unit different from the cycling unit. The PA, 1A, and Cont. input terminals (shown on PX-9-303) make this possible. Portable push buttons may be used in connection with these terminals by plugging them into program lines (with no load box) which are in turn connected to each of the terminals PA, 1A, and Cont.

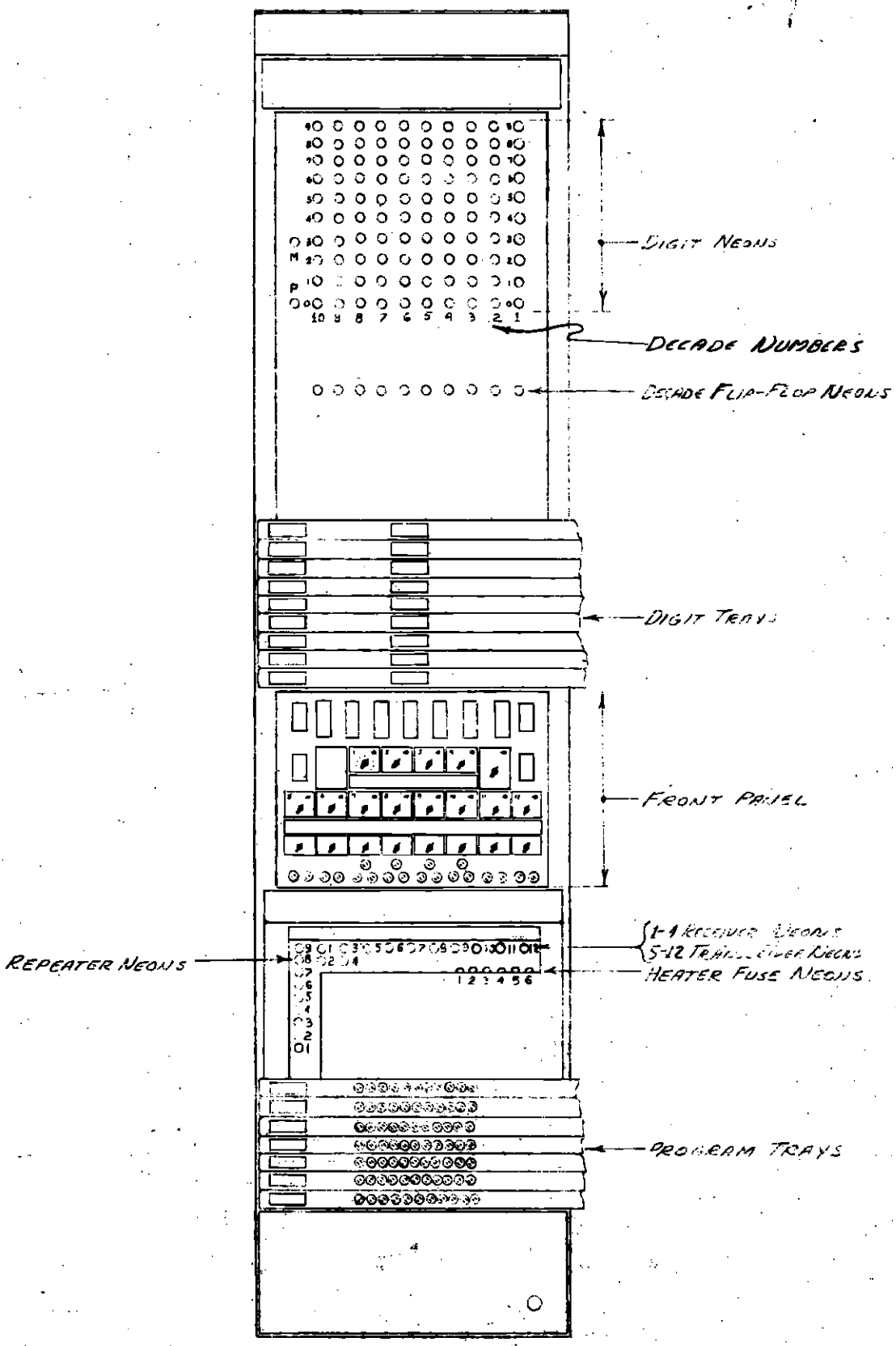
A push button connected to terminal PA parallels the 1 pulse - 1 add addition time push button. Portable push buttons connected to the 1A or Cont. terminals can be used only when the operation selector switch is set at 1 Pulse, since, with either of the other settings, the mode of operation circuits are locked so that they cannot be entered except from the operation selector switch. Closing the button connected to terminal 1A causes the 1 addition time relay to be activated; closing the button connected to the Cont. terminal causes the continuous relay to be activated.

A more convenient method of operating the 1 pulse time - 1 addition time push button and the operation selector switch from any place in the ENIAC room is provided by the portable control box. This box, which parallels certain controls found on both the initiating unit and the cycling unit, is discussed in Section 11.6.

3.3. THE CYCLING UNIT OSCILLOSCOPE

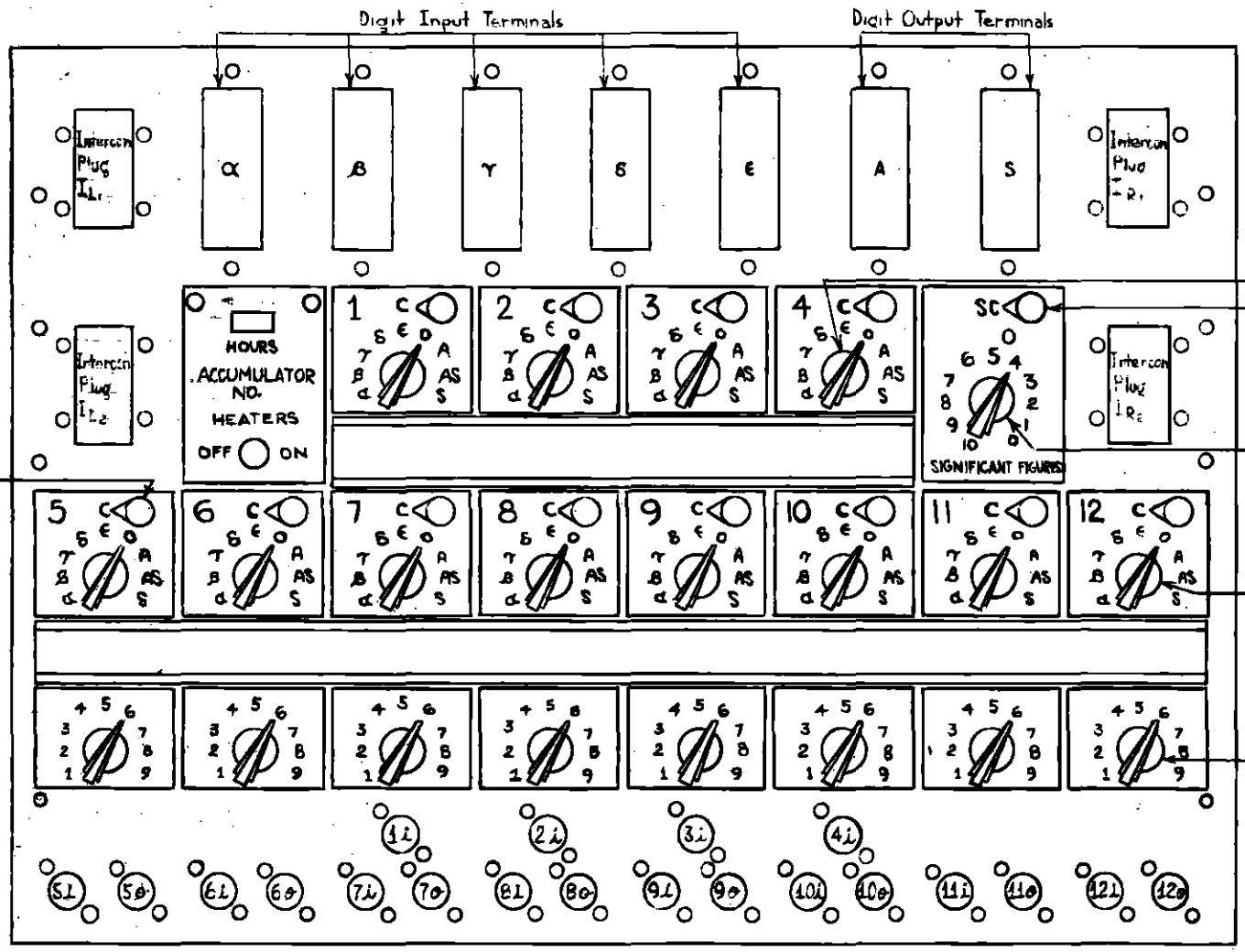
An oscilloscope whose screen is shown on PX-9-303 is built into the cycling unit. The oscilloscope input switch with its 12 positions makes it possible to view any of the groups of cycling unit pulses or gates, the selective clear gate, or any external signal brought to the cycling unit through terminal Ext. below the switch.

It might be noted that the main purpose of the oscilloscope is to make possible verification of the presence of the pulses and to provide a rough check on their amplitudes. When viewed on the screen, the cycling unit pulses and gates should be approximately an inch high as indicated by the line on the oscilloscope screen. Because of their reflection in the lines of the synchronizing trunk, the cycling unit pulses and gates seen on the oscilloscope screen do not have the symmetrical square shape shown on the chart below the screen.



MOORE SCHOOL OF ELECTRICAL ENGINEERING
UNIVERSITY OF PENNSYLVANIA

ACCUMULATOR
FRONT VIEW
PX-5-305



TERMINALS $1i, 2i, \cdots, 12i$
Program pulse input terminals

TERMINALS $5\theta, 6\theta, \cdots, 12\theta$
Program pulse output terminals

ACCUMULATOR
FRONT PANEL
PX-5-301R

IV ACCUMULATOR

The accumulator serves as a memory and arithmetic unit. Each accumulator can store and operate on a number having as many as 10 digits with its sign indication. Two accumulators can be interconnected by special plugging of their interconnector terminals so that they can store and operate on a signed number with as many as 20 digits. Programming memory is provided by the transceivers of the accumulator's 8 repeat program controls. Repeat switches included in the repeat program controls make it possible for an accumulator to remember that it is to transmit a program output pulse 1 to 9 addition times after receiving a program input pulse. In addition to 8 repeat program controls, the accumulator has 4 non-repeat program controls which have receivers and can, therefore, receive but not transmit a program pulse.

Because an accumulator is capable of receiving a number or of transmitting the number and/or the complement of the number stored in it, an accumulator is capable of performing the operations of addition or subtraction. Repeat program controls on the ENIAC make it possible for the accumulator to receive or transmit repetitively from one to nine times when a given repeat program control is stimulated. Each accumulator has 5 digit input channels through any one of which it can receive a 10 digit signed number. Mechanical shifters plugged into these input terminals make it possible to receive the incoming number shifted to the right or left. Thus, the accumulator, through repeated addition, can carry out the multiplication of a number by a constant having one or more digits.

The ability to do addition and subtraction and the presence of transceiver units in the accumulator also make it possible for the ENIAC to compare the magnitudes of two numbers in accumulators and, on the basis of this discrimination, choose which of 2 alternative program courses is to be followed.

The accumulator can clear its contents to zero in all decades or can

clear so that zero remains in all decades but one and a five remains in that one (clear to 5). The ability to clear to 5 in a given decade combined with the possibility of plugging a deleter into an accumulator's digit output terminal or terminals makes it possible to use the accumulator to round off numerical results.

The static outputs of various stages of the 10 decade counters and the binary PM counter of an accumulator can be connected to other units such as the high speed multiplier or printer so that these units can receive information about the number stored in a given accumulator statically. (see Sec. 4.3.3.).

The following topics regarding the accumulator will be discussed in this chapter: Sec. 4.1, program controls; Sec. 4.2, common programming circuits; Sec. 4.3, numerical circuits; Sec. 4.4, use of accumulators for fewer or more than 10 digit computations; and Sec. 4.5, problems illustrating the use of accumulators. Reference will be made to the following diagrams:

Accumulator Front View	PX-5-305
Accumulator Front Panel	PX-5-301
Accumulator Block Diagram	PX-5-304

4.0. GENERAL SUMMARY OF THE ACCUMULATOR

Each accumulator has 12 program controls (see PX-5-301). Four of these are non-repeat program controls; eight are repeat.. Each of the 12 program controls has an operation switch for specifying the operation (receive, transmit, or neither) which the accumulator is to perform and a clear-correct switch. In addition, each non-repeat control has a receiver with a program pulse input terminal; each repeat program control has a transceiver with program pulse input and output terminals and a repeat switch. Neons associated with the 4 receivers and 8 transceivers are shown on PX-5-305.

The 12 program controls operate common programming circuits (see PX-5-304), the receive circuits, the transmit circuits, the clear circuits

(including the significant figures switch and selective clear switch), and a circuit which enables the accumulator to pick up the 1'P. The repeat switches of the 8 repeat program controls also operate in conjunction with the 9 stage repeater ring circuit. The repeater neons (see PX-5-305) are correlated with the stages of the repeater ring.

The programming circuits common to all 12 program controls operate the accumulator's numerical circuits (see PX-5-304). The accumulator's numerical circuits consist of 10 decade plug in units and a PM-clear plug in unit. Each decade plug in unit consists of a decade (10 stage ring) counter, a decade flip-flop (16, 17), a stage nine gate (14), reset pulse gate (18), carry over gates (19 and 20), A and S output gates (21 and 22 respectively) and transmitters, a pulse standardizer and several inverter tubes. Each decade counter stores 1 digit of a number and plays a part in the reception or transmission of one digit of the total of 10 digits that the accumulator can handle. The decade flip-flop has 2 purposes: (1) In reception it remembers if carry over is to take place; (2) in transmission it controls the A and S output gates. Gates 14, 18, 19, and 20 participate in the carry over process. Gate 18, moreover, controls the resetting of the decade flip-flop. The decades are numbered from right to left so that units decade counts as decade 1 and the 10^9 decade, as decade 10. There is a neon bulb associated with each stage of a decade counter and with the decade flip-flop (see PX-5-305).

The PM-clear unit contains a binary ring (PM) counter, A and S output gates and transmitters, a pulse standardizer, and amplifier tubes for the clear signal. There is also a special transmitter for the 1'P used when the accumulator transmits subtractively. The PM counter has stage P for positive numbers, and stage M for negative numbers (which are treated as complements in the ENIAC). It should be noted that pulse input to the PM counter can come not only from the PM lead of a digit input terminal, but also can result from

carry over from the 10th decade. This latter fact makes possible the correct addition or subtraction of signed numbers. Neons correlated with the stages P and M of the PM counter are shown on PX-5-305.

When storing the number +2 345 098 765, the accumulator's face will have the appearance shown on PX-5-305 (a) where a darkened circle denotes a lit neon bulb, and the corresponding stages of the various counters will be in the abnormal state.

The negative of a number is represented in the ENIAC by the complement of the number with respect to 10^{10}*. An accumulator stores the number -2 345 098 765 in the form M+(10^{10}-2 345 098 765) or M+(7 654 901 235). When an accumulator is storing -2 345 098 765, the digit neons appear as in Px-5-305 (b) and the corresponding stages of the counters are in the abnormal state.**

The decade counters and PM counter transmit their digit output through either or both of 2 terminals, the A (add) and S (subtract) output terminals. The number stored in an accumulator is emitted over the A terminal; the complement, over the S terminal. The counters can receive their inputs from any one of 5 input terminals identified by the letters α, β, γ, δ, ε. The decade counters and the PM counter of an accumulator receive or transmit the information for all 10 digits and sign simultaneously (the transmission of the pulses for each digit is, however, serial).

4.1. PROGRAM CONTROLS AND THE SIGNIFICANT FIGURES AND SELECTIVE CLEAR SWITCHES

As stated earlier, each accumulator has 12 program controls: four non-repeat controls (consisting of receiver with program pulse input terminal, operation switch and clear-correct switch) and 8 repeat controls (consisting of transceiver with program pulse input and output terminals, operation switch, clear-correct switch, and repeat switch). In this section the possible settings

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* Also see Sec. 4.1.4.

**When two accumulators are interconnected to form one 20 decade accumulator, complements are taken with respect to 10^{20}.

and uses of program control switches will be described. The significant figures switch and selective clear switch which are more properly classified as part of an accumulator's common programming circuits are also described here. The switches are shown on PX-5-301. Neons correlated with the 12 program controls are shown on PX-5-305.

4.1.1. The Operation Switch

The operation switch has 9 positions: α, β, γ, δ, ε, O, A, S, AS. If the operation switch of a stimulated program control is set at one of the settings α, β, γ, δ, or ε, the accumulator receives the pulses representing any number transmitted over the digit tray to which the corresponding digit input terminal is connected. Obviously, if that input terminal is not connected to a digit tray or is connected to a tray not carrying pulses at the time the control is stimulated, the accumulator receives no pulses. This point will be referred to in Sec. 4.1.2, in connection with the clear-correct switch.

If the operation switch is set at A, S, or AS, the accumulator transmits its contents, the complement of its contents, or both respectively when the control is stimulated.

The setting O instructs the accumulator to neither receive nor transmit. This setting is useful on non-repeat or repeat control operation switches when it is desired to clear an accumulator without receiving or transmitting (see Sec. 4.1.2.). When set on the operation switch of a repeat program control, the setting O provides a means of obtaining a program output pulse delayed from 1 to 9 addition times without, however, disturbing the contents of the accumulator. (See the discussion of dummy programs in Sec. 4.5.).

4.1.2. The Clear-Correct Switch

The clear-correct switch can be set at either C or O. The accumulator's interpretation of the setting C depends on the setting of the associated

operation switch.

If a stimulated program control's operation switch is set at one of the transmit settings (A, S, or AS) or is set at O, the accumulator clears either to zero in all decades or to zero in all decades except one in which it clears to 5. The setting of the significant figures switch (see Sec. 4.1.4) determines whether clearing is to zero or 5 and, if to 5, in which decade the 5 appears.

With the operation switch set to a receive setting α, β, γ, δ, or ε, the setting C of the clear-correct switch gives the instruction "pick up the 1'P from the synchronizing trunk and put it in the first decade". If there are no digit pulses coming to the digit input terminal when the control set up in this way is stimulated, the accumulator simply picks up the 1'P. If there are actually pulses coming to the digit input terminal, these are first received and then, when the cycling unit emits the 1'P, this pulse also is picked up and put into the first decade. A "receive - C" program in which digits are received and the 1'P is picked up is, however, not possible when the digits are being transmitted as a complement from another unit in such a way that the 1'P from the digit tray also arrives in units place. (See Sec. 4.3.1.)

There are at least three occasions when the "receive -C" setting of a program control proves useful. If a given accumulator is being used to store the independent variable, the accumulator can be programmed to pick up the 1'P whenever it is desired to increase the value of the independent variable by one (see the illustrative problem of Chapter VIII). In some problem set-ups, an accumulator may receive from the S output terminal of the product, quotient, or two root accumulator, a complement with respect to 9 in all decades instead of a 10^{10} complement (see Chapters V and VI and Sec. 4.3.1.). Also, an accumulator may receive a number transmitted as a complement by a second accumulator and shifted to the right enroute so that

the original 1'P needed to make a tens complement (see Sec. 4.3.1.) is lost. The missing pulse, in either case, can be picked up through a "receive -C" program.

4.1.3. Repeat Switch

The repeat switch (which is found only on repeat program controls) can be set to any number between one and nine inclusive. The accumulator carries out whatever operation is set on the associated operation switch as many times as is specified by the setting of the repeat switch. Each repetition requires one addition time so that if the repeat switch of a control is set at r ($1 \leq r \leq 9$), r addition times must be allowed for the program set up on that control. The transceiver of a repeat program control emits a program output pulse at the end of r addition times.

It is to be noted that if the clear switch of a repeat program control is set at C in connection with an O or transmit setting of the operation switch, clearing of the accumulator takes place but once, at the end of the r^{th} addition time. The setting C in connection with a receive setting of the operation switch of a repeat program control causes the accumulator to pick up the 1'P in each of r addition times.

If the number a is stored in one accumulator and the number b in another accumulator, $a \pm rb$ (where $1 \leq r \leq 9$) may be formed in the first accumulator through the use of a repeat program control on each accumulator. The operation switch of the control on the first accumulator should be set at a receive setting and the repeat switch, at r. The operation switch of the second accumulator's control should be set at A (if $a+rb$ is to be formed) or at S (if $a-rb$ is to be formed) and the correlated repeat switch, at $R \geq r$. (see Problem 1, Sec. 4.5.)

In a similar fashion, it is possible to form $a \pm b \sum r_i 10^{k-i}$. In this case where the coefficient of b has more than one digit, shifters (see Secs. 4.5 and 11.2) are used to effect multiplication by powers of 10.

Notice that if the coefficient of b has p digits, p program controls will usually have to be used on the receiving accumulator but fewer than p may suffice on the transmitting accumulator. For example, 234b may be formed in an accumulator through the use of one program control (set-up to transmit additively 9 times) on the transmitting accumulator. Three program controls must be used on the receiving accumulator: one set up to receive, say on α, 4 times; another set up to receive on β, 3 times; a third set up to receive on γ, twice. A shifter which shifts numerical data 1 place to the left should be used at the β input terminal and one which shifts numbers two places to the left, at the γ input terminal of the receiving accumulator. As an example of the circumstances under which fewer than p program controls suffice on the transmitting accumulator, consider the case of forming 998b. This can be done by programming the accumulator which stores b to transmit subtractively twice and then additively once and by programming the receiving accumulator to receive twice thru an input terminal without a shifter and once thru an input terminal with a shifter that displaces data 3 places to the left (i.e. form 998b as 10^3b - 2b).

4.1.4. The Significant Figures Switch

The significant figures switch is a part of the common programming circuits which function when the accumulator transmits subtractively or when the accumulator clears. The significant figures switch has eleven positions, 0, 1, ..., 10. These numbers refer to the number of significant figures, counted toward the right from the PM counter, to be retained in the accumulator.

If the significant figures switch on an accumulator is set at s ($0 \leq s \leq 10$), when clearing takes place, decade 10-s (i.e. the $s+1^{st}$ decade from the left) clears to five and all other decades to zero. When a single accumulator is used, this means that the accumulator is cleared to zero in all decades if its significant figures switch is set at 10. If two accumu-

lators (see Sec. 4.4.2.) are interconnected to form a 20 decade accumulator, the setting s=10 on the left hand accumulator causes it to clear to zero in all decades; the right hand accumulator then clears in accordance with the setting of its significant figures switch. For example, if 11 significant figures are to be stored in the 11 left hand decades of a 20 decade accumulator, the significant figures switches of the left and right hand accumulators respectively are set at 10 and 1.

The setting of the significant figures switch also determines the decade place into which the 1'P is put when an accumulator transmits subtractively. With the significant figures switch of an accumulator set at s, the 1'P is transmitted over the lead for decade place 11-s, i.e., the s^{th} decade place from the left. If the significant figures switch of an accumulator is set at 0, this means that the 1'P is not transmitted when subtractive transmission takes place. It is to be noted that the 1'P is picked up and put into units decade of an accumulator (which, in the case of 2 interconnected accumulators, mean the 20th decade from the left) when a "Receive-C" program control is stimulated regardless of the setting of the significant figures switch.

Notice, that as far as rounding off a number in an accumulator is concerned, the setting of the significant figures switch provides only for getting the correct s digits from the left. The significant figures switch setting has nothing to do with deleting the non-significant digits at the right. The operator provides for the deletion of non-significant figures by placing a deleter at the output* terminal or terminals of the accumulator storing s significant figures (see Secs. 4.5 and 11.2). When printing of an s significant figure result is to take place from an accumulator and the non-significant figures at the right have not been deleted, deletion can be

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* The deleters constructed at present can be used only at digit output terminals. Special deleters, however, can be constructed for use at digit input terminals.

provided for in the set up of the IBM punch plug board (see Sec. 9.4 for an illustration).

4.1.5. The Selective Clear Switch

The selective clear switch has two positions, SC and O. When the selective clear signal is transmitted from the initiating unit (see Chapter II), all accumulators whose selective clear switches are set at SC clear; those accumulators whose selective clear switches are set at O do not clear.

4.2. COMMON PROGRAMMING CIRCUITS

4.2.1. The Receive Circuits

When the receiver or transceiver of a program control whose operation switch is set at a receive setting (α, β, γ, δ, or ε) is stimulated, a signal from the normally positive output of the flip-flop is delivered (after passing thru an inverter and a buffer) by way of one deck of the operation switch to the receive circuits of the accumulators. The receive circuits include gates A through E 47, buffer tubes (A-C 48, A, C. E, G, and J 46, and A-D 49), and the 5 sets of receive gates A-L 41, ..., A-L 45 for the digit input terminals α through ε respectively.

The signal from the deck of the operation switch (referred to above) applied to the set of receive gates corresponding to the setting of the switch, opens the 11 receive gates for that digit input channel. Simultaneously, then, the digit pulses for the 10 decade places and the PM place are received in the accumulator. The pulses for each place are routed to the appropriate counter with each pulse received at a counter cycling it one stage.

The signal applied to one of the gates A-E 47 allows the carry clear gate to enter the accumulator and play its role in the carry over process (see Sec. 4.3.1.).

4.2.2. The Transmit Circuits

If a stimulated program control is set up for transmission (operation switch set at A, S, or AS), a signal from the normally positive output of the flip-flop opens one of the gates F, G, or H47 so that the 10 P are admitted

to each of the decades of the accumulator. The role played by the 10 P in transmission is described in Sec. 4.3.1. The signal from the flip-flop also opens gate F49 (if S), J49 (if A) or gates G and H49 (if AS) so that the 9P can pass to the A and/or S output gates of the 10 decades and the PM unit. In S or AS transmission, moreover, gate M42 or M41 is opened to pass the 1'P. The 1'P passing through deck 3 of the significant figures switch is routed to the lead of the S output terminal specified by the setting of the significant figures switch. The manner in which the A and S gates are controlled so that the correct number of digit pulses (or 9P) are emitted over each decade place lead is described in Sec. 4.3.1.

4.2.3. The Clear Circuits

The clear circuits include gate M44, decks 1, 2, 1A, and 2A of the significant figures switch and the clear tubes in the PM unit.

If an accumulator is stimulated to transmit and clear, a signal from buffer 62 of receivers or buffer 63 of transceivers is applied to gate M44 so that the carry clear gate (CCG) is passed to the PM-Clear unit. The clear signal from the PM tubes goes directly to the upper connections of stages 1, 2, 3, 4, 6, 7, 8 and 9 in all decades causing these stages to be flipped into the normal state. With the significant figures switch set at s, the signal from the clear tubes is routed through deck 2A to the upper lead of the zero stage in decade 10-s and through deck 1 to the upper connection to stage 5 in all decades except decade 10-s. Decks 1A and 2 of the significant figures switch are return circuits from the flip-flops. Thus, stage zero is left in the abnormal state in all decades except decade 10-s in which stage 5 is left in the abnormal state.

Notice that gate M44 can be opened to pass the CCG either by the initial clear gate (see Chapter II) or by the selective clear gate (provided that the accumulator's selective clear switch is set at SC.), as well as by

the flip-flop mentioned above.

4.2.4. Circuit for Admitting the 1'P to Units Decade

A signal from the normally negative output of a transceiver's flip-flop, through a buffer and then passing through the clear correct switch and one of the receive points on the operation switch reaches gates E49 and E50 after passing through the inverter G50. These gates, when opened, allow the 1'P to pass through to units decade of the accumulator.

4.2.5. Repeater Ring Common to Repeat Program Controls

The eight repeat program controls on an accumulator operate the 9 stage repeater ring circuit in common. A signal from the normally negative output of the flip-flop of such controls and then through buffer 61 opens gate H50 so that a CPP can reach the repeater ring to cycle it one stage per addition time. When the ring reaches stage r, the output signal from this stage, passing through point r on the repeat switch, causes gate 62 in the transceiver to emit a signal. The signal from 62 opens gate 68 which passes a CPP. The resulting pulse resets the transceiver's flip-flop and passes through the transmitter as a program output pulse. The signal from gate 62 also opens gate K50 so that a CPP passing through it clears the repeater ring back to stage 1 at the same time as the transceiver is emitting a program output pulse.

4.3. NUMERICAL CIRCUITS

4.3.1. Operation of the numerical circuits in transmitting a number and/or its Complement.

When an accumulator is stimulated to transmit its contents and/or the complement of its contents, the 10P are routed simultaneously to each of the 10 decade ring counters of the accumulator. Each of the 10P cycles the counter one stage. Thus, if the stage corresponding to 7 is in the abnormal state before any of the 10P is received, after receiving one pulse, the stage

TABLE 4-1

A and S TRANSMISSION

Accumulator stores P 0 000 000 007 - Significant figures switch is set at 10

Pulse Time	9P emitted over A leads PM 10 987 654 321	9P emitted over S leads PM 10 987 654 321	As result of receiving 10P acc. registers	Comment
0-17				Program input pulse is received.
18				
19				
1-0			P 1 111 111 118	
1		1 1 111 111 111	P 2 222 222 229	
2		1 1 111 111 111	P 3 333 333 330*	*Indicates that decade flip flop is in abnormal state.
3	0 0 000 000 001	1 1 111 111 110	P 4 444 444 441*	
4	0 0 000 000 001	1 1 111 111 110	P 5 555 555 552*	
5	0 0 000 000 001	1 1 111 111 110	P 6 666 666 663*	
6	0 0 000 000 001	1 1 111 111 110	P 7 777 777 774*	
7	0 0 000 000 001	1 1 111 111 110	P 8 888 888 885*	
8	0 0 000 000 001	1 1 111 111 110	P 9 999 999 996*	
9	0 0 000 000 001	1 1 111 111 110	* *** *** *** P 0 000 000 007	
10		0 0 000 000 001		1'P is emitted over the lead for units decade because s = 10.
11				
12				
13				Reset pulse resets all decade flip-flops.
14				
15				
16				
17	Program output pulse is transmitted if repeat control is used. Receiver (of non-repeat control) or transceiver (of non-repeat control) is reset.			

corresponding to 8 is in the abnormal state, and stage 7 not. After receiving 10 pulses, the stage corresponding to 7 is in the abnormal state again (See Table 4-1).

Meanwhile the accumulator changes the 9P into digit pulses in the following way: Let d be the digit stored in a given decade counter before the reception of any of the 10P. Then as the 10P are received, 9-d of the 9P pass through gate 22 to be emitted over a lead of the subtract output terminal. That one of the 10P which cycles the decade counter from stage 9 to zero, also passes through gate 14 and sets the decade flip-flop. With the decade flip-flop in the abnormal state gate 22 is closed and 21 open so that the subsequent d pulses of the 9P group are passed over the corresponding decade place lead of the add output terminal. The first of the RP resets the decade flip-flop.

So far in this discussion mention has been made of transmitting through the subtract output terminal the complement of a number stored in an accumulator with respect to 9 999 999 999. Complements with respect to 10^{10} are provided by the accumulator's transmitting over the subtract output lead corresponding to decade s from the left (where s is the number of significant figures stored in the accumulator), the 1'P.

The transmission of sign indication is accomplished in a somewhat different manner. The S and A gates, 16 and 15 respectively, of the PM unit are controlled by stages P and M respectively of the PM counter. When a positive number is stored in an accumulator which is transmitting, a positive voltage from stage M holds gate 16 open so that the 9P are emitted over the PM lead of the subtract output terminal; no pulses are transmitted over the PM lead of the add output terminal since gate 15 is closed. If the sign of the stored number is M, gate 16 remains closed and 15 is opened so that no PM pulses are transmitted through the subtract output terminal, while 9 pulses

are transmitted through the add output terminal.

4.3.2. Operation of the Numerical Circuits in Receiving a Number

The digit pulses received through the 11 input gates (see Sec. 4.2.1.) are routed simultaneously to the PM counter and the ten decade counters. Each pulse a decade counter receives cycles it one stage. The PM counter receives zero sign pulses for a positive number and 9 for a negative number. Each pulse received by the PM counter cycles it one stage so that the reception of an even number of pulses leaves the PM counter unchanged while the reception of an odd number of pulses has the effect of cycling the PM counter to the opposite stage.

If a given counter stores the digit d before reception and p ($9-d < p \leq 10$) digit pulses are received, carry over takes place from that counter to the next one at the left (whether the PM or a decade counter). So called delayed carry over takes care of such carry-overs which result from incoming digit pulses. If a given counter, c, is in stage 9 and there is a carry over from the counter c-1, then, it is also necessary for carry over to take place from counter c to counter c+1. Carry overs which result from carry overs in this way are effected by a direct carry over process.

When a given counter is cycled to stage 9, a signal from this stage opens gate 14 so that the next pulse received by the decade (whether digit or carry pulse) not only cycles the counter back to stage zero but also passes through gate 14 and sets the decade flip-flop (16, 17). In delayed carry over, the decade flip-flop continues to remember that a carry over must take place but no further action is taken while the digit pulses (the 9P and the 1P) are being received. The signal from the normally negative output of the decade flip-flop opens gate 18 so that the reset pulse is passed (in pulse time 13 of the addition time cycle). This pulse resets the decade

flip-flop and also goes to gate 20. Now, in receive programs, the receive programming circuits allow the carry clear gate to reach and open gate 20, so that the pulse from gate 18 passes through to the next decade at the left.

The need for direct carry over arises after the first reset pulse is emitted by the cycling unit (since it is this reset pulse which gives rise to the need for direct carry over) so that carry over resulting from carry over must be treated differently. The carry pulse which passes through gate 14 goes to gate 19. Since the carry clear gate remains on for 7 pulse times, gate 19 is held open to pass this pulse to the next decade at the left. The carry clear gate, as a matter of fact remains on long enough for a carry pulse to proceed from units decade to the PM counter of 2 interconnected accumulators (with a safety factor). Notice, that even in direct carry over, the decade flip-flop is flipped into the abnormal state. The 2nd reset pulse, which is emitted after the carry clear gate goes off, resets the flip-flop in this case (see PX-9-306)

A number may be received in an accumulator so that a digit appearing in the i decade of the transmitting unit is received in the i decade of the receiving unit by connecting the digit output terminal of the transmitting unit to some digit trunk by the standard cable for that purpose, and then connecting the same digit trunk to one of the 5 digit input terminals of the receiving accumulator by a standard cable. However, if it is desired to receive a number transmitted from decade i of the transmitting unit in decade i + k of the receiving accumulator (where k may be either positive or negative), the number must be passed through a shifter enroute from the transmitting to the receiving unit. It is usually most convenient to plug ordinary shifters into a digit input terminal of the receiving unit. A number may be <u>shifted to the left</u>

TABLE 4-2

RECEPTION INVOLVING DELAYED CARRY OVER

Accumulator Stores M 9 832 104 707 and Receives P 0 000 000 004

Pulse Time	Accumulator Receives PM 10 987 654 321	Accumulator Stores After Receiving PM 10 987 654 321	Comment
0-17			Program input pulse received.
-18			
-19			
1-0	0 0 000 000 001	M 9 832 104 708	
1	0 0 000 000 001	M 9 832 104 709	
2	0 0 000 000 001	M 9 832 104 700*	*Decade flip-flop in abnormal state.
3	0 0 000 000 001	M 9 832 104 701*	
4			
5			
6			
7			
8			
9			
10			
11			
12			
13	0 0 000 000 010	M 9 832 104 711	Reset pulse resets decade flip-flop and causes carry pulse.
14			
15			
16			
17			Program output pulse emitted if repeat control is used, and program control is reset.

either by an ordinary shifter plugged into a digit input terminal or by a special shifter plugged into a digit output terminal. A number may be shifted to the right only through an ordinary shifter plugged into a digit input terminal (see Sec. 11.2).

Table 4-2 illustrates the way in which an accumulator receives a number and also the delayed carry over process.

4.3.3. Static Communication Between an Accumulator and Another ENIAC Unit

The high-speed multiplier receives its arguments and the printer data to be printed in static form from accumulators. The divider and square rooter also receives information about the signs of the arguments statically. The term static is used to distinguish this kind of communication between an accumulator and another unit from the usual dynamic transmission in which an accumulator transmits d pulses for the digit d and 0 or 9 pulses for sign P or M respectively.

A unit which receives the static outputs of an accumulator has an array of vacuum tubes* corresponding to the flip-flops of the counters in an accumulator. For example, the ier selectors in the high-speed multiplier (see Sec. 5.3) which receive the multiplier from the multiplier accumulator statically consist of a 10 by 10 array of vacuum tubes. Each of the tubes in a column of the array corresponds to one of the flip-flops in a decade counter of an accumulator; each column in the array, to a decade counter in an accumulator. Two standard 55 conductor cables (carried in the static cable trough which runs along the tops of the ENIAC units) are used to deliver the static outputs of the accumulator which stores the multiplier to the ier selectors. The normally negative output of the flip-flop representing digit d

*Two double triodes in one envelope are referred to here as 2 tubes.

in decade counter c is connected by one of the leads in these cables to the corresponding tube in the ier selectors. Thus, 100 of the 110 leads are used. An additional lead in one of the cables goes from the flip-flop for stage M in the accumulator's PM counter to a tube in the high-speed multiplier which represents sign M of the multiplier. In this way, when flip-flop d of counter c is in the abnormal state (because that counter stores the number d) the tube in row d and column c of the ier selectors is turned on. The other tubes in column c of the ier selectors do not go on.

Similar connections are made to tubes in the printer from the counters of accumulators which store data for printing (see Sec. 9.4). In some cases data is printed from only 5 decades and the PM of an accumulator so that only 1 cable connects such an accumulator to corresponding tubes in the printer. The master programmer also has decade counters which are similar in some respects to the decade counters of an accumulator (see Sec. 10.2.). These, too, can be connected statically to the printer.

In the case of the divider and square rooter only sign indication is communicated statically from the accumulators which store the numerator (or radicand) and denominator.

The length of time required for the information stored in an accumulator to be communicated in static form to another unit depends on the length of the leads from the accumulator to the unit. Approximately an addition time is required to turn on the tubes in the high-speed multiplier and in the divider and square rooter because the accumulators statically connected to these units are near them. A somewhat longer time is required in the case of the printer.

4.4. USE OF ACCUMULATORS FOR FEWER THAN OR MORE THAN TEN DIGITS

4.4.1. Use of an Accumulator to Store Two Numbers

In some problems it may be desirable to put emphasis on the number of different numbers which can be stored in accumulators so that they will be readily available for computations rather than on the number of significant figures carried in the computation. While the accumulator has been designed to handle 10 digit numbers, it is possible to store in an accumulator two numbers with the same sign if their combined number of digits is 10 or fewer or with different signs if their combined number of digits is fewer than 10. In the first case the PM counter is used for the common sign. In the second case, one of the decade counters is used as a PM counter for the purpose of registering sign indication for one of the numbers with stage 0 representing sign P and stage 9, sign M.

When the numbers are transmitted to other units for computational purposes, they can be isolated from one another by the use of special deleters, adaptors, and/or shifters. It is to be noted, however, that if subtractive transmission takes place from an accumulator storing two numbers, only one of the numbers will be a correct tens complement since the other will lack the 1'P needed to make such a complement.

An example involving the use of an accumulator to store two different numbers simultaneously is given in the illustrative problem of Sec. 8.7.

4.4.2. Interconnection of Two Accumulators to Form a Twenty Decade Accumulator

Another option available to the operator is whether an accumulator is to be used alone as a 10 decade accumulator with 12 program controls or as a 20 decade accumulator with controls for 24 programs. This option results from the fact that certain of the accumulator's circuits have been left open at the

accumulator's interconnector terminals (indicated on PX-5-304 by the symbol —┤ ├—). The circuits so treated include the receive, transmit, clear, and pick up the 1'P circuits, and the input to units decade and the carry over input to the PM counter from decade 10. By special connections of the accumulator's interconnector terminals (I_{L_1}, I_{L_2}, I_{R_1}, and I_{R_2} on PX-5-301), these circuits are closed in one way to make the accumulator function as a 10 decade accumulator and in a different way to interconnect two accumulators so that they form a 20 decade accumulator.

If a single accumulator is used as a 10 decade accumulator, the following interconnections must be made:

(a) vertical interconnector cable must be plugged from interconnector terminal I_{L_1} to I_{L_2}

(b) load box must be placed at interconnector terminal I_{R_1}.

If two accumulators U and U' (where U is assumed to be the left hand accumulator) are to be used as a 20 decade accumulator, the required interconnections are:

(a) vertical interconnector cable from I_{L_1} to I_{L_2}

(b) horizontal interconnector cables from I_{R_1} to I'_{L_1} and from I_{R_2} to I'_{L_2}

(c) load box at I'_{R_1}

The significant figures switch of the left hand accumulator should be set to 10 and in the right hand accumulator to s' where $0 \leq s' \leq 10$ if 10 + s' significant figures are desired. If fewer than 10 significant figures are desired, the left hand switch is set to this number and the right hand

switch to 10.

For a given program only 1 program control is used. In reception, each accumulator receives its ten digits over one of its 5 digit input terminals. If the standard jumper cable for interconnecting accumulators is used, each accumulator receives its 10 digits through the digit input terminal on its front panel bearing the same designation (α-ε) as the setting of the operation switch used to program the reception. Each accumulator transmits its digit output through its own digit output terminals. In the transmission of complements the 1' pulse is emitted over the decade place lead of the last significant figure being retained. The 20 decade accumulator clears to zero in all decades except possibly one where clearing is to 5. Clearing is to zero in all decades if both s and s' are 10. In "receive -C" programs, the 1' pulse is put into the 20th decade from the left.

More than 2 accumulators should not be interconnected with one another as described above since the carry clear gate does not last long enough to provide safely for direct carry over across more than 20 decades; nor are the program control buffers designed to operate more than 2 accumulators.

4.5. ILLUSTRATIVE PROBLEMS

Matters relevant to setting up accumulators for certain specific purposes will be discussed in the following pages. Sec. 4.5.1. illustrates the set-up for a very simple computation involving only accumulators. Sec. 4.5.2. treats of the use of dummy programs, and Sec. 4.5.3. deals with the use of accumulators for magnitude discrimination programs. Examples of the use of accumulators in conjunction with other ENIAC units are found at the end of Chapters VI - IX.

The examples will be described with the aid of set-up tables and

set-up diagrams. The set-up table is designed to give a comprehensive plan of the computation showing the programs the units will perform and their numerical contents at various addition times in the computation. The set-up diagrams show the cable connections which must be made between the units and program or digit trays to carry out the computations and also indicate the settings of switches which are parts of the common programming circuits.

The set-up tables are given with addition times as the independent variable. A double column is devoted to each unit. In the left hand half the program is described; in the right hand half, the contents of the unit as a result of the program are shown. For accumulator programs, symbols appear on three levels, e.g.

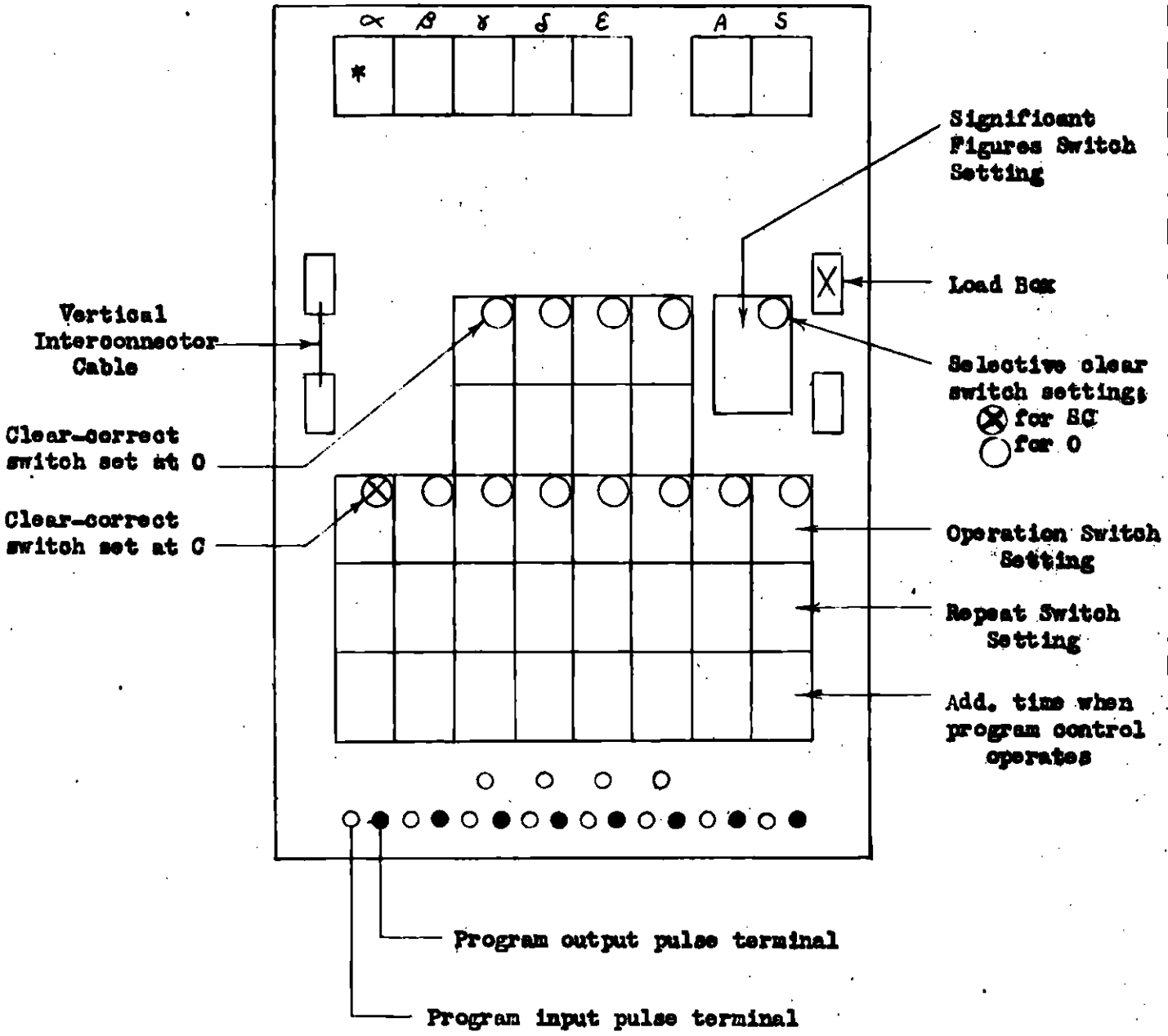


The symbols have the following interpretations:

(1) (i) at the upper right of the first level indicates that the program is set-up on program control i

(2) j-k designates a program pulse with j representing the tray and k the line in the tray on which the program pulse is carried. A program input pulse which occurs, say, at pulse time 17 (CPP time) of addition time 0, is written at the left on the first level of the addition time 1 line. A program input pulse which is derived from a digit pulse so that it occurs, not at CPP time, but at some other time in the addition time cycle, let us say pulse time 5 of addition time 1, is written at the left of the third level on the line corresponding to addition time 1. A program output pulse is always written at the right of level

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*A shifter, deleter, or adaptor plugged into a digit terminal is described in the digit terminal box as follows:

A shifter which shifts numerical data k places to the left or right respectively by the symbol +k or -k.

A deleter which eliminates the digits carried on certain decade places leads by the letter d followed by the numbers of the decade place leads deleted.

An adaptor by the letter a. A description of the adaptor appears in a convenient place on the diagram.

Fig. 4-1

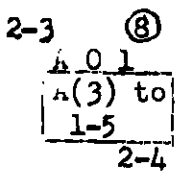
SET-UP DIAGRAM SYMBOLS FOR ACCUMULATOR

three. An arrow ending on the addition time line in which the program is completed and program output pulse is transmitted intervenes between level 2 and level 3 for programs lasting more than one addition time. In such cases, the program output pulse is written at the right of the arrow tip on the line for the addition time at the end of which the program is completed and the program output pulse is transmitted.

(3) The symbols in the second level represent the settings of the operation, clear-correct, and repeat switches reading from left to right.

Thus, the illustrative group of symbols above at the left, has the following meaning: A program pulse (derived from a CPP) which is picked up from line 8 in program tray 1 stimulates program control 5 to cause the accumulator to transmit additively one time and then to clear. Upon completion of the program, a program output pulse is emitted to line 9 in program tray 1.

On some occasions, as noted above, digit pulses will be used in lieu of program pulses. A program in which such a digit pulse is generated might be written as in the sample below.



This group of symbols describes the following program: The program pulse delivered to the program input terminal of control 8 causes the accumulator to transmit additively once without clearing. The digit pulses carried on the add output lead for decade place 3 are delivered to line 5 of program tray 1.

The program output pulse from control 8 is carried on line 4 of program tray 2.

The symbol ——— in the contents column is used to indicate that an accumulator is cleared. It is always written on the line corresponding to the addition time at the end of which clearing takes place.

The conventions on the set-up figures for accumulators are described in Figure 4-1.

4.5.1. Computation in Accumulators

The computation described here consists of generating n, n^2, and n^3 respectively in accumulators 6, 7, and 8. It is desired to terminate the computation when $n^3 \geq 9\ 000\ 000\ 000$.

The basic computation which is repeated until the limit specified on n^3 is reached is arrived at inductively. Assuming that n, n^2, and n^3 are stored in accumulators 6, 7, and 8 respectively we can proceed to $(n+1)^3$ and $(n+1)^2$ by adding $3n^2$, 3n, and then 1 to n^3 and by adding 2n and then 1 to n^2 (see Table 4-3).

To terminate the computation at the desired point we make use of the fact that the complement of 9 in a decade place other than that of the extreme right hand significant figure is zero. Now, we stimulate repetition of the computing cycle each time by the program output pulse of a dummy program control whose program input pulse is derived from the digit pulse or pulses on the subtract output lead for decade 10 of accumulator 8. As long as the digit in the 10th decade is different from 9, this control receives and therefore, transmits a program output pulse which stimulates the iteration. When 9 appears in the 10th decade, this dummy program control receives and, therefore, emits no program output pulse so that the computation is terminated.

The question as to why the S digit output of the 10th decade is

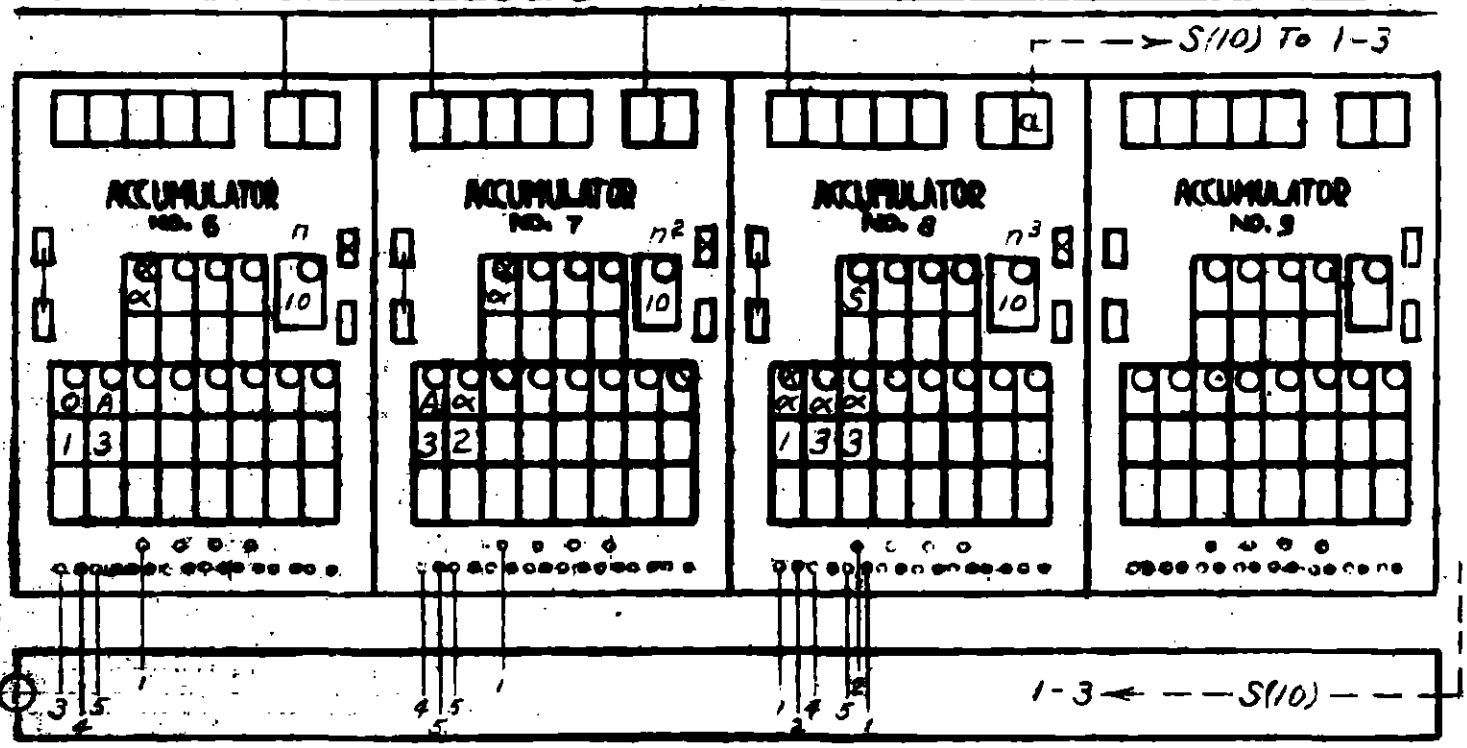


Fig. 4-2

Set-Up Diagram for Problem of Generating n, n^2, and n^3 as long as $n^3 < 9\,000\,000\,000$

TABLE 4-3

SET-UP TABLE FOR GENERATING n, n^2, n^3

Computation is terminated when $n^3 \geq$ 9 000 000 000

Unit Add. Time	Accumulator No. 6		Accumulator No. 7		Accumulator No. 8	
0	Initiating Pulse from initiating unit to program line 1-1					
1	1-1 ① α C 1	1	1-1 ① α C 1	1	1-1 ⑤ α C 1 1-2	1
2	⑤ 1- 0 0 1 1-3 1-4				1-2 ① S 0 1 S (10) to 1-3	
3			1-4 ⑤ A 0 3		1-4 ⑥ α 0 3	2
4						3
5			1-5			4
6	1-5 ⑥ A 0 3		1-5 ⑥ α 0 2	2	1-5 ⑦ α 0 3	5
7				3		6
8					1-1	7
9	1-1 ① α C 1	2	1-1 ① α C 1	4	1-1 ⑤ α C 1 1-2	8
10	⑤ 0 0 1 1-3 1-4				1-2 ① S 0 1 S (10) to 1-3	

Initial Sequence

Basic Computing Sequence Repeated as long as $n^3 <$ 9 000 000 000

delivered to a program control which does nothing but transmit a program output pulse instead of being delivered to one of the controls used for computing may be raised at this point. The answer lies in the fact that the digit pulses do not begin to pour out of the S output terminal until pulse time 1 in the addition time cycle. This would mean that a computing program initiated by a digit pulse would start after at least one of the 1OP and one of the 9P had been emitted by the cycling unit. Since these pulses play a vital role in computing programs, such programs must be initiated before the digit pulses are emitted. For this reason digit pulses may be used to initiate computing programs only under certain restricted conditions. Instead digit pulses should be converted into a true program pulse through the use of a dummy program (see Sec. 4.5.2.) and the computing program can then be initiated by the program pulse which results from the dummy program.

4.5.2. Dummy Programs

A dummy program is defined as one in which the operation and clear-correct switches are set at 0 and the repeat switch at r where $1 \leq r \leq 9$. Dummy programs are always set-up on repeat program controls. The dummy program has at least 3 important functions: 1) conversion of digit pulses into program pulses, 2) delay of a program pulse, and 3) isolation of programs from one another.

The discussion in Sec. 4.5.1. regarding use 1) may be summarized as follows: To ensure that units receive all of the pulses needed for arithmetic operations, computational programs must usually be initiated by program pulses occuring at the time of the CPP. Where the stimulation of subsequent programs depends on digit pulses, the digit pulses should be converted into a program pulse by being brought to a dummy program control. The program output pulse

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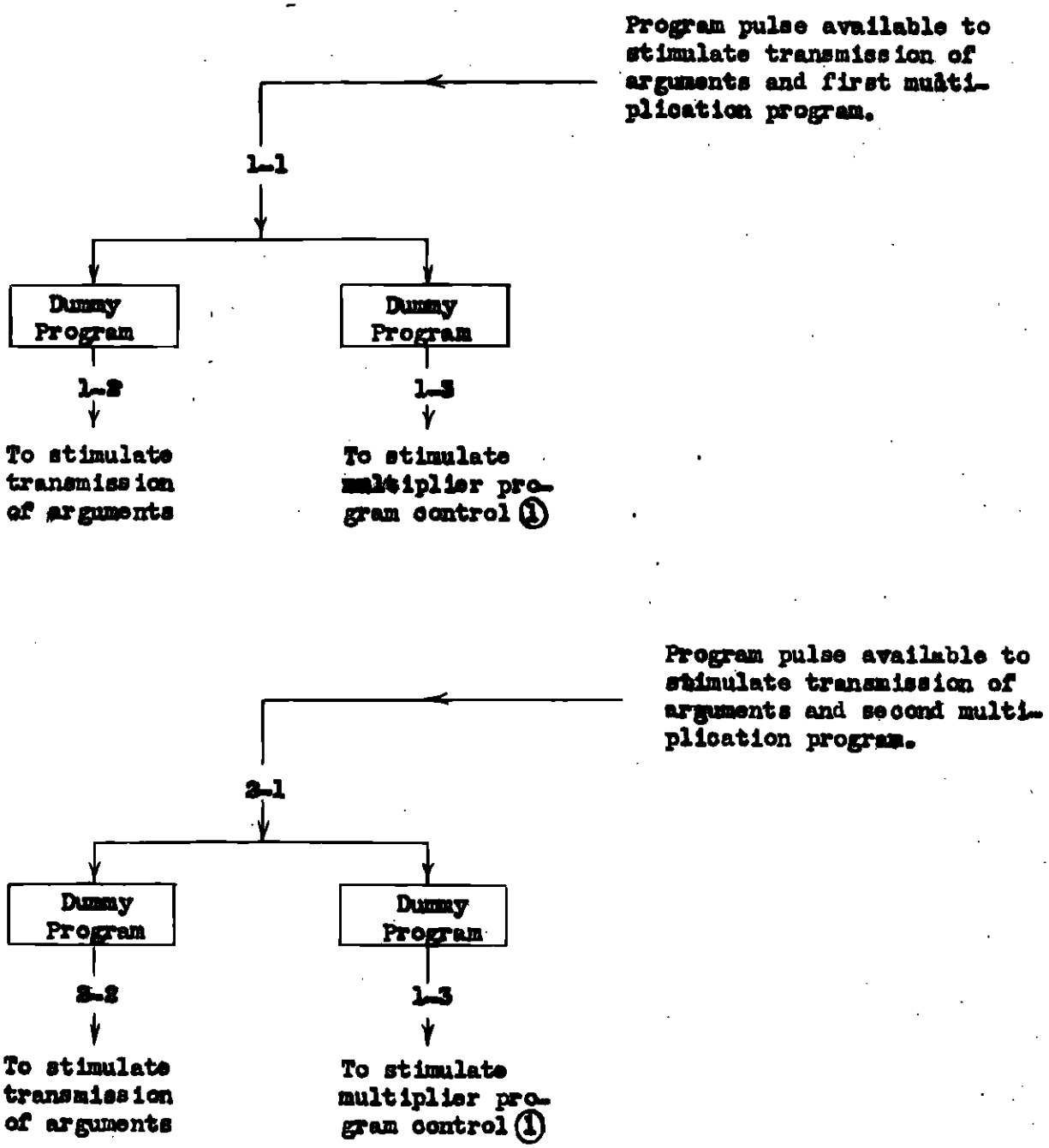


Fig. 4-3

USE OF DUMMY PROGRAMS TO ISOLATE PROGRAM PULSES

from the dummy program control can then be used to stimulate computing programs.

The need for the second contribution (delay) of dummy programs becomes apparent in setting up a fairly complicated problem in which a number of programs are carried out in parallel. As an example of this need, the reader is referred to the illustrative problem of Sec. 8.7.

Suppose that at some point in a computation one program pulse is available to stimulate a multiplier program control and also to stimulate the transmission of the arguments for the multiplication program. Let us suppose further that the same multiplier program control is to be stimulated at some later time but that the arguments for the multiplication program, this time, are to be obtained in a different way. Obviously, the program pulse that stimulates transmission of the arguments must be isolated from the pulse that stimulates the multiplier program control for, otherwise, the units which transmit the arguments for the first multiplication cannot be suppressed from transmitting when the second multiplication program takes place.

The desired isolation can be provided for through the use of dummy programs in the manner suggested in Figure 4-3. The lines which carry program pulses have been labelled with program tray and line numbers for illustrative purposes.

4.5.3. Magnitude Discrimination Programs

As mentioned in the opening paragraphs of this chapter, the ENIAC is capable of discriminating between program sequences by examining the magnitude of some numerical result. In this section one possible method of carrying out such a magnitude discrimination program in an accumulator is discussed.

Let us assume that the critical quantity upon whose magnitude the choice of subsequent programs depends is x so that when $x < b$, program P_1 is

PX-401

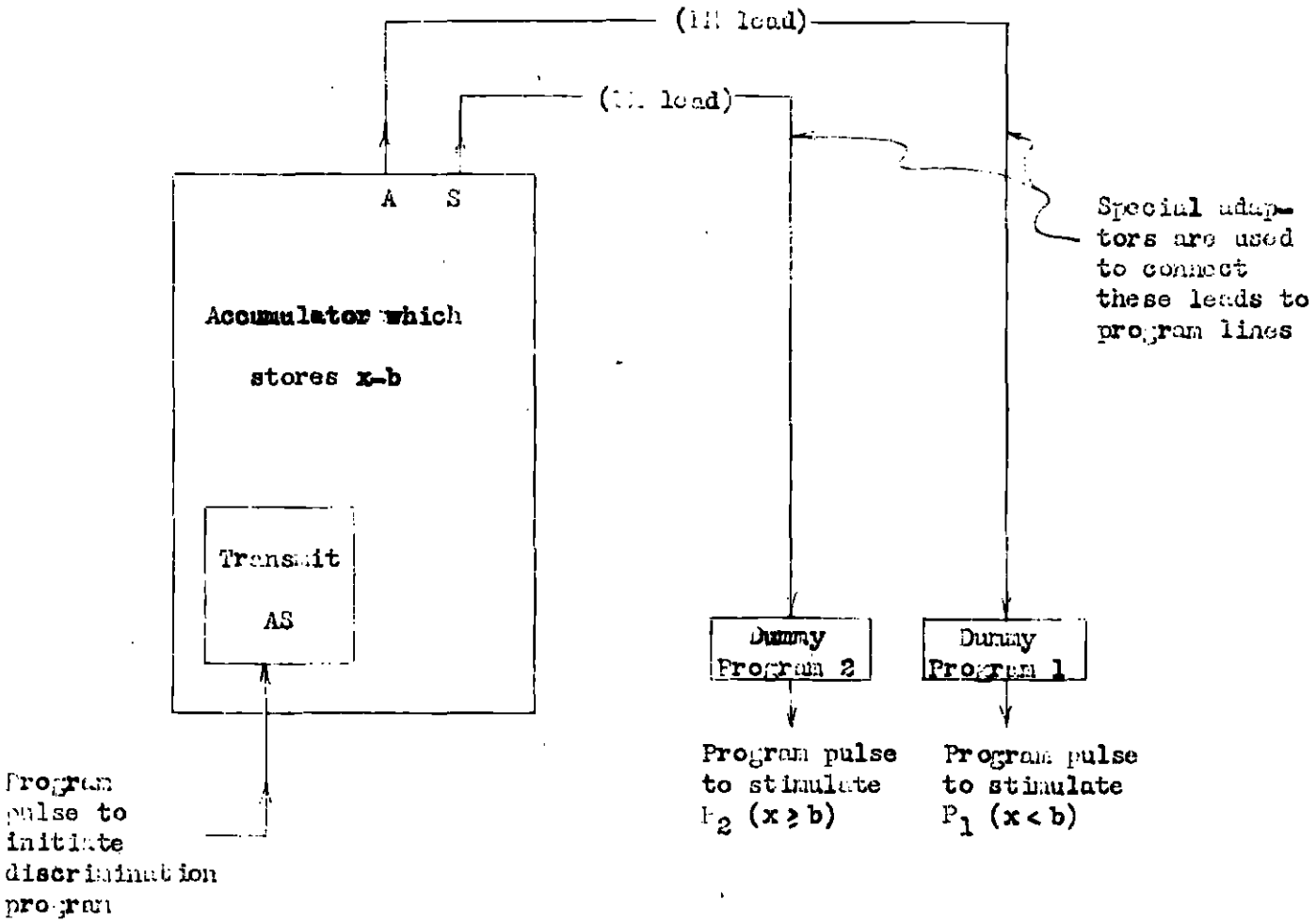


Fig. 4-4

MAGNITUDE DISCRIMINATION PROGRAM

to be stimulated and that when $x \geq b$, program P_2 is to be stimulated. The magnitude discrimination program is possible because 9 digit pulses are transmitted for sign indication M and none for sign indication P.

Let us form the quantity x-b in some accumulator. Then, using a special adapter, connect the PM lead of the A output terminal of this accumulator to the program pulse input terminal of one dummy program control and the PM lead of the S output terminal to the program pulse input terminal of a second dummy program control as indicated on the schematic diagram of Figure 4-4.

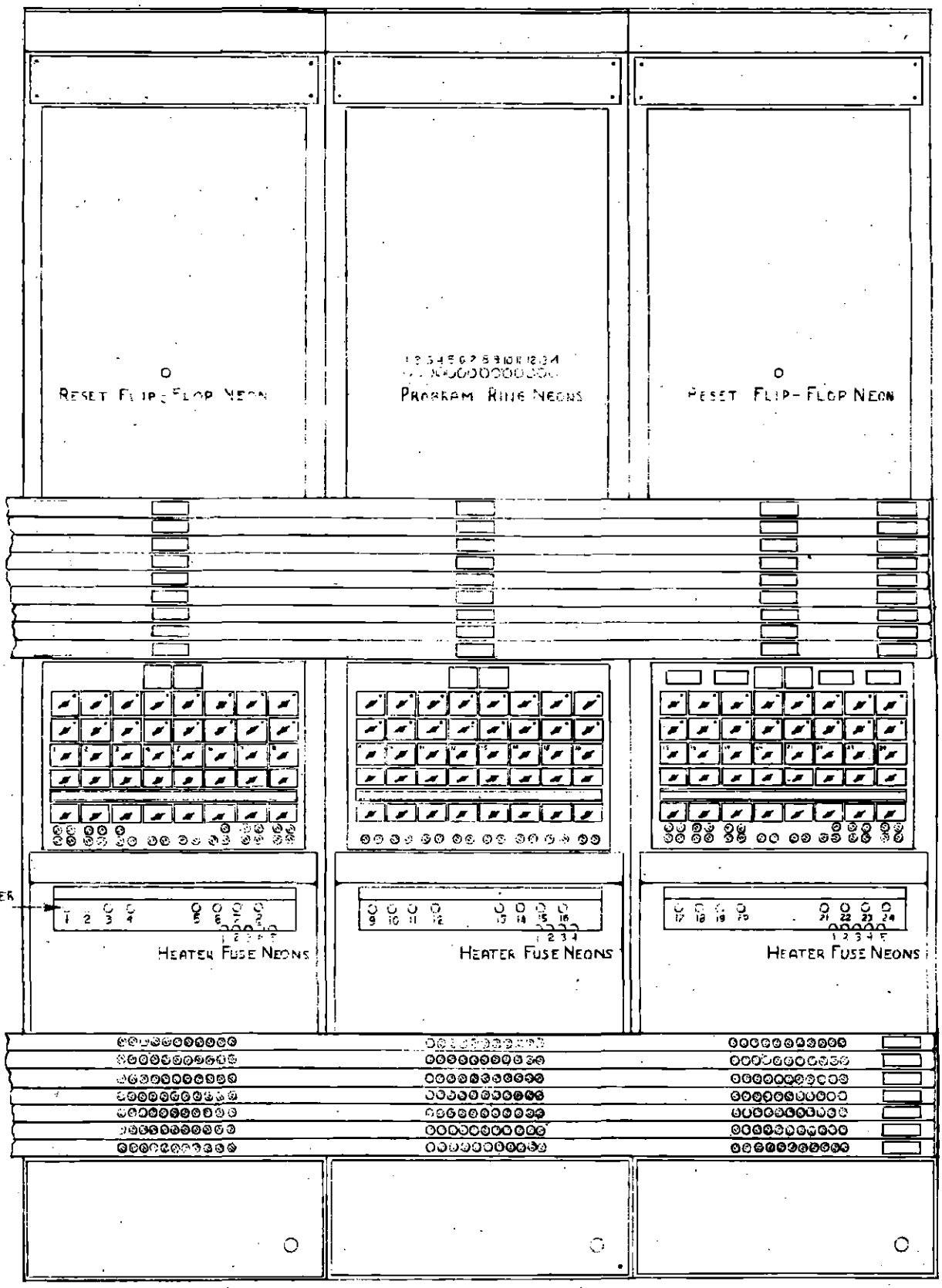
Obviously when $x < b$, a positive number is emitted over the S terminal and a negative over the A terminal so that only dummy program control 1 is stimulated to emit a program pulse. Similarly, when $x > b$, the number emitted over the A terminal is positive and that over the S terminal, negative so that only dummy program control 2 is stimulated to emit a program pulse.

Even though both the number zero and its complement are represented in the ENIAC by P 0 000 000 000, the case $x = b$ (or $x - b = 0$) can still be treated in the same way as $x > b$ (or $x - b > 0$). For recall, when a positive number is transmitted from an accumulator, the A output gate of the PM counter remains closed and the S gate opens to allow the 9P to pass to the PM lead of the S output terminal.* These 9P received at the program pulse input terminal of dummy program control 2 cause the emission of a program output pulse to stimulate P_2.

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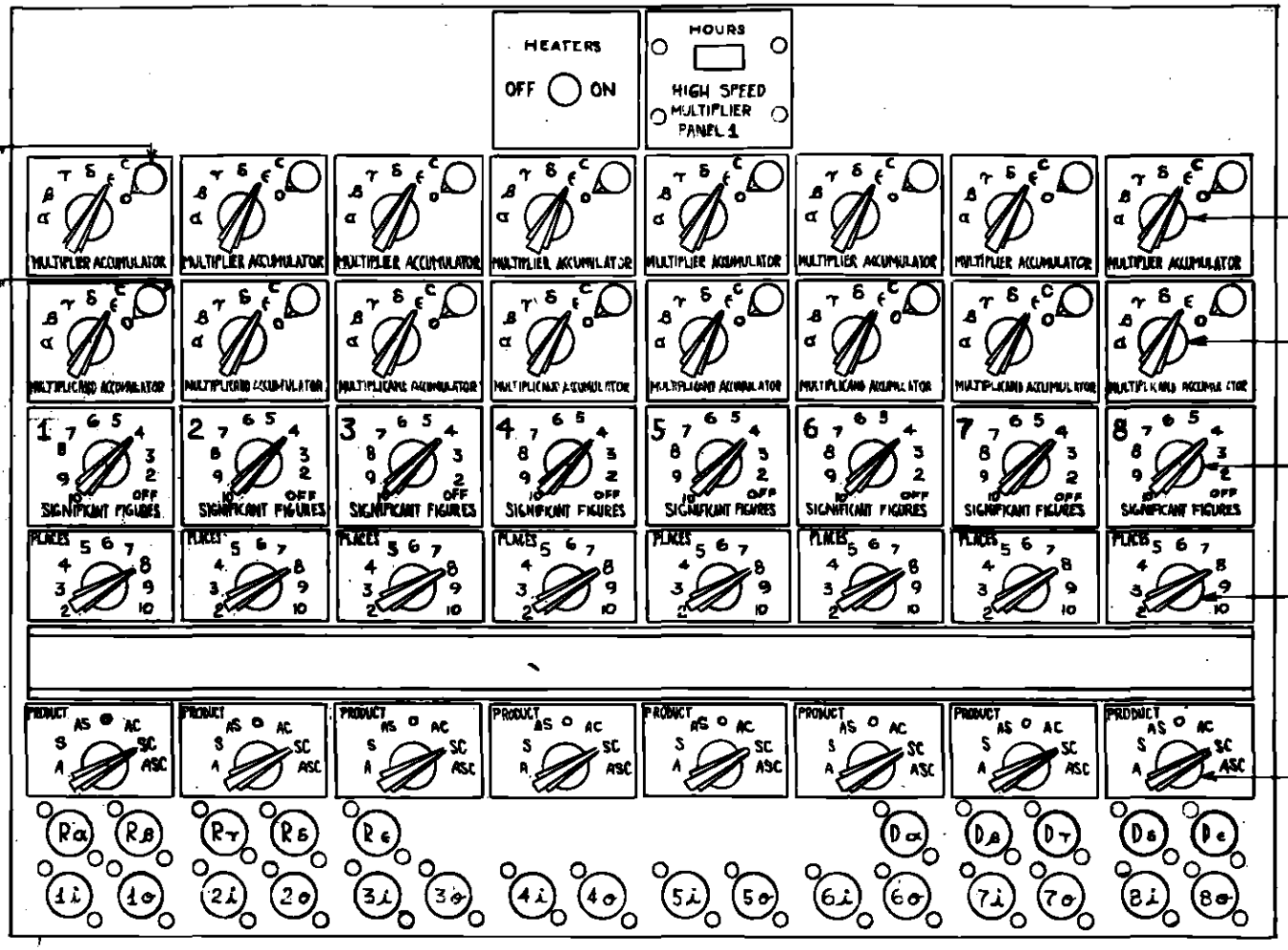
*Notice that when an accumulator which stores zero transmits subtractively to a second accumulator, this second accumulator receives, at first, M 9 999 999 999. Later, in the pulse time of the 1'P, the transmitting accumulator emits this pulse so that the receiving accumulator then stores P 0 000 000 000 after direct carry over proceeding from units decade to the PM counter has taken place.

In a problem in which accumulators are not urgently needed for storage or computational purposes, this set-up of a magnitude discrimination program is satisfactory. However, in general, this method has the disadvantage that no numerical programs other than one magnitude discrimination program can be carried out in an accumulator so set up, since both digit output terminals of the accumulator are completely associated with the magnitude discrimination program. The same magnitude discrimination can be effected without completely tying up either digit output terminal of an accumulator if the master programmer is used. A magnitude discrimination program involving the master program is described in Sec. 10.6.2. of the master programmer chapter.



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HIGH SPEED MULTIPLIER
FRONT VIEW
PX-6-309



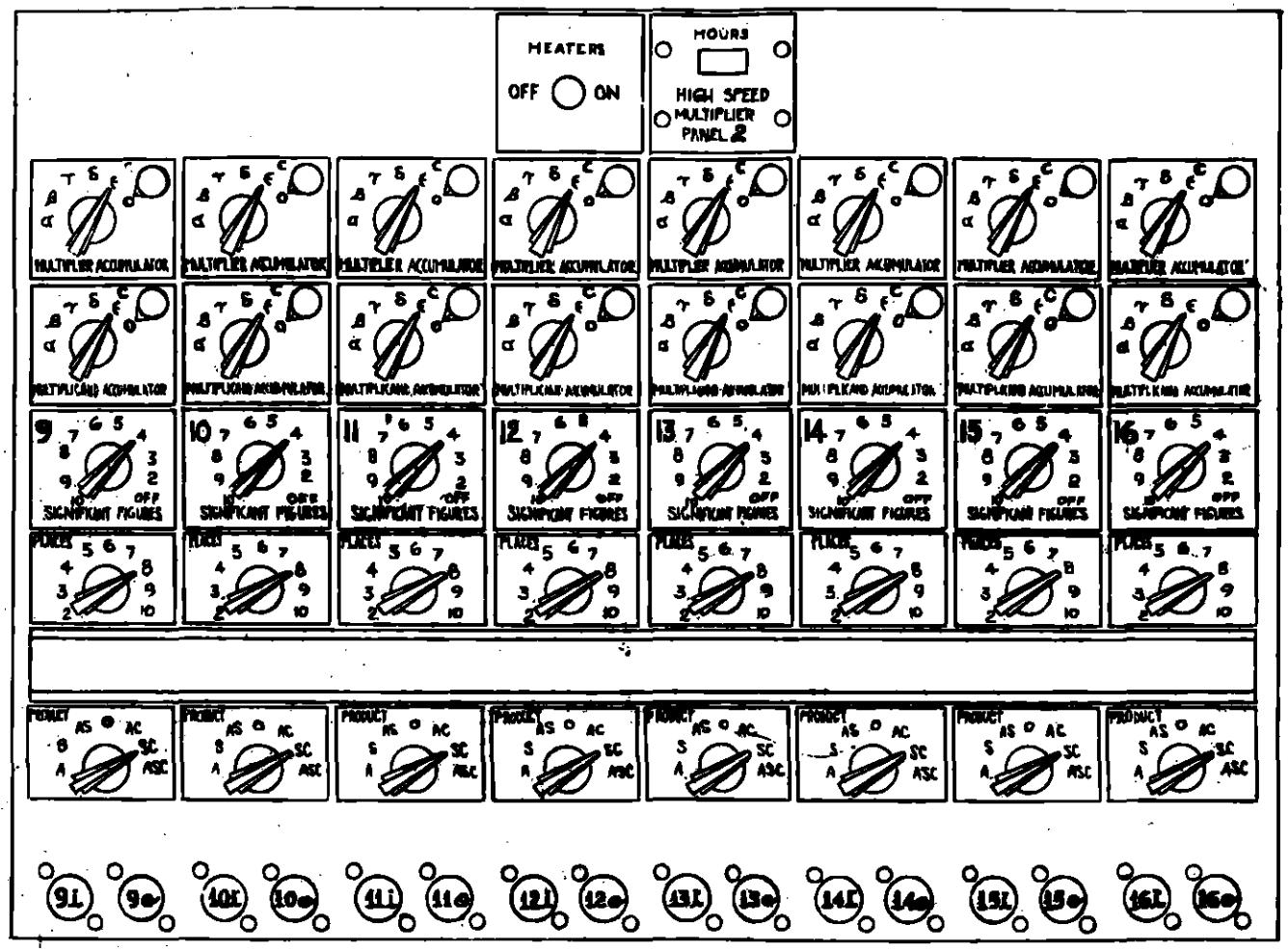
TERMINALS $1i, 2i, \cdots, 24i$
Program input pulse terminals for programs 1-24 respectively.

TERMINALS $1o, 2o, \cdots, 24o$
Program output pulse terminals for programs 1-24 respectively.

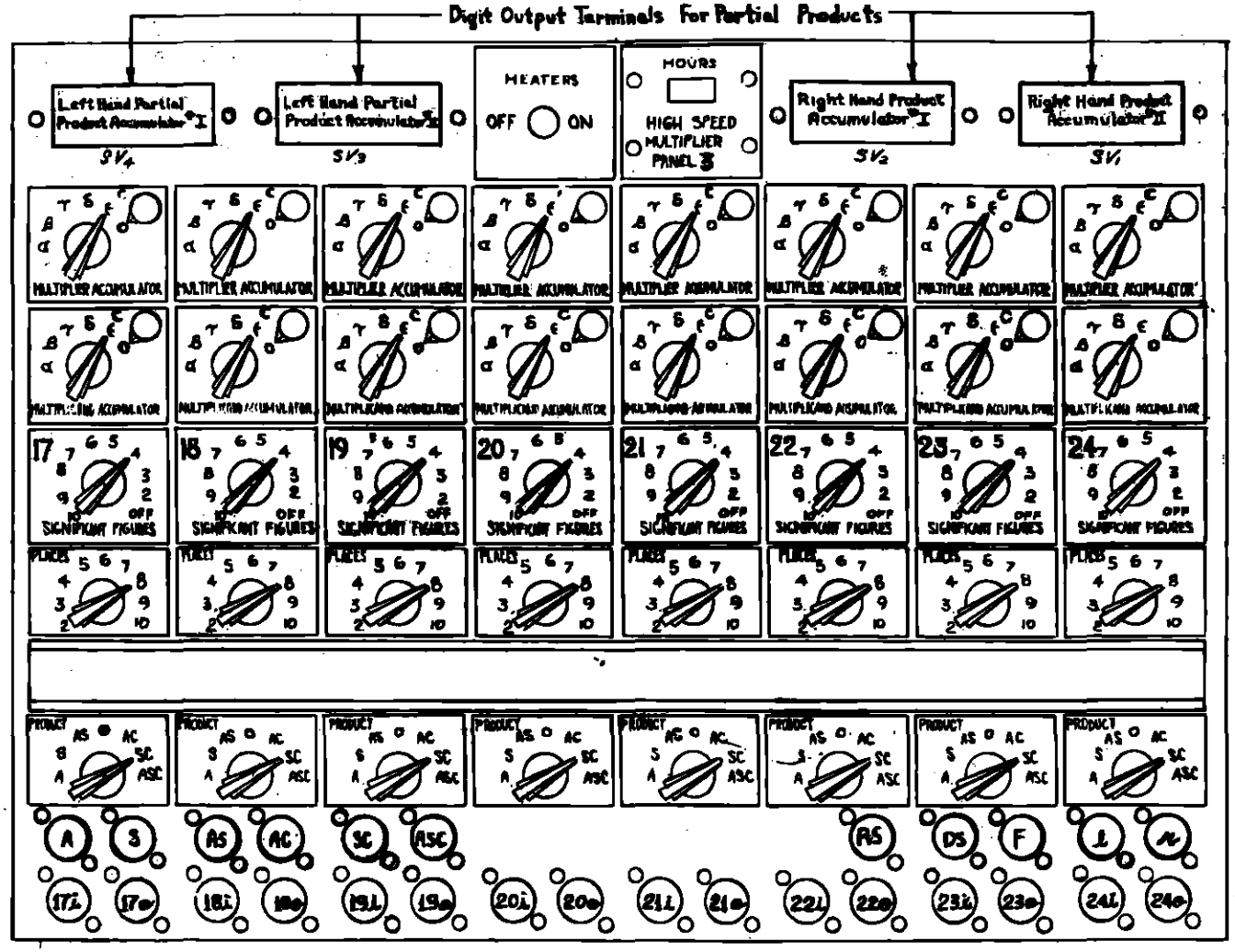
TERMINALS $R\alpha$-$R\epsilon$
Program output pulse terminals associated respectively with $\alpha, \beta, \tau, \delta, \epsilon$ on the 24 multiplier accumulator Receive switches.

TERMINALS $D\alpha$-$D\epsilon$
Program output pulse terminals associated respectively with $\alpha, \beta, \tau, \delta, \epsilon$ on the 24 multiplicand accumulator receive switches.

HIGH SPEED MULTIPLIER FRONT PANEL NO 1
PX-6-302R



HIGH SPEED MULTIPLIER
FRONT PANEL NO. 2
PX-6-303R



TERMINALS A-ASC

Program output pulse terminals associated respectively with A, S, AS, AC, SC, ASC, on product disposal switch.

TERMINALS F, RS, DS, ℓ, r

Program output terminals for transmitting following signals which occur during multiplication cycle:

ℓ and r - left and right hand accumulators respectively receive partial products.

RS and DS - correct for negative multiplicand and/or multiplier respectively.

F - left hand accumulator transmit contents to right hand accumulator, (or vice versa).

HIGH SPEED MULTIPLIER FRONT PANEL NO. 3 PX-G-304R

V HIGH-SPEED MULTIPLIER

The high-speed multiplier finds the product of a signed multiplicand with as many as 10 digits by a signed multiplier of p digits ($p \leq 10$) in p+4 addition times. This high-speed is possible because products are obtained through the use of a multiplication table rather than by repeated addition.

Not only does the high-speed multiplier find products, but it also has facilities for controlling certain programming features in accumulators associated with it: 1) It can instruct the argument accumulators to receive and clear or not clear at the end of the multiplication; 2) It can signal the final product accumulator to dispose of the product; 3) It delivers to associated accumulators programming signals used in the multiplication process.

The following topics will be discussed in this chapter: Sec. 5.1, program controls; Sec. 5.2, common programming circuits; Sec. 5.3, numerical circuits; Sec. 5.4, Interrelation of high-speed multiplier and associated accumulators; Sec. 5.5, illustrative problem set-ups. Reference will be made to the following diagrams:

Front View	PX-6-309
Front Panels	PX-6-302, 303, and 304
Block Diagram	PX-6-308
Interconnection of High-Speed Multiplier with Associated Accumulators	PX-6-311

5.0. GENERAL SUMMARY

The high-speed multiplier operates in conjunction with 4 or, possibly, 6 accumulators. Two accumulators, the ier (multiplier) and icand

(multiplicand) accumulators, store the arguments. The accumulators used for this purpose have the static outputs of their counters connected to the multiplier. Also, the PM-clear unit is statically connected to the multiplier so that these accumulators can be cleared by a signal from the multiplier at the end of a multiplication program and so that the high-speed multiplier may take proper cognizance of the signs. If products having 8 or fewer significant figures are required, two accumulators are used for storing the products which the multiplier emits in pulse form through the digit output terminals on panel 3. These accumulators are referred to as the LHPP (left hand partial products) and RHPP (right hand partial products) accumulators. Where products of more than 8 significant figures are desired, a pair of interconnected accumulators may be used as the LHPP accumulator and another pair as the RHPP accumulator. The role of the LHPP and RHPP accumulators will be discussed in greater detail below. Either the LHPP or RHPP accumulator may be used as the final product (FP) accumulator.

The high-speed multiplier has 24 program controls (8 on each of its 3 panels) on which can be set up 24 essentially different multiplication programs. In a problem in which there are more than 24 basic multiplications, each multiplier control can be used on a number of different occasions with the aid of the master programmer or sequences of dummy programs.

Each program control consists of a transceiver with program pulse input and output terminals, multiplier and multiplicand accumulator receive switches, multiplier and multiplicand accumulator clear switches, a significant figures switch, a multiplier places switch, and a product disposal switch. The argument accumulator receive switches enable the operator to specify the digit input terminals through which the ier and icand accumulators shall receive their

arguments for a given program. The significant figures switch setting determines into which decade place of the LHPP five round off pulses are transmitted for a given program. The setting of the places switch determines how many of the multiplier's digits are used for the program and, therefore, how long the multiplication takes (see below and Sec. 5.2.). Instructions for the transmission of the product from the final product accumulator can be set up on the answer disposal switch.

The 24 program controls operate the common programming circuits which include a 14 stage program ring with associated gates, inverters and buffers, the ier accumulator and ieand accumulator receive circuits with program pulse output terminals Ra-Rx and Da-Dx on front panel 1, argument accumulator clear circuits, the product disposal circuit with program pulse output terminals A, S, ..., ASC on front panel 3, and the argument accumulator clear circuits.

The program ring with its associated tubes clocks the progress of multiplication programs. Gates A'47 and A'46 which admit the 1'P and 4P are the round off gates. Gates B'-K'46 operate in conjunction with the places switch to terminate the program when the specified number of places of the ier have been used and, in conjunction with gate F'48, to clear the ring to stage 13 at this time. The program ring, ultimately, also controls a circuit for correcting products if either or both of the arguments are negative (see discussion below), the l and r receiver circuits which emit static signals to program the partial products accumulators to receive, the circuit which emits the F pulse to stimulate the collection of the partial products in the final product accumulator, and the reset circuits for the program controls.

The outputs of stages 3 through 12, by means of the buffer tubes B'-L' 42, control the high-speed multiplier's numerical circuits so that multiplication by each digit of the ier takes place successively.

The numerical circuits consist of the multiplier selector gates, the multiplication table, the coding gates which pass the 1, 2, 2', and 4P, the multiplicand selector gates and the shifters. The multiplication table stores the products of numbers between 1 and 9 by numbers between 0 and 9 by means of a resistance matrix. The table actually consists of 2 tables, the tens and units tables, used for storing the tens and units digits of these products respectively. For example, the multiplication table remembers the product of 4 x 9 by storing 3 in the tens table and 6 in the units table.

The ier selector tubes are set up by the static outputs of the ier accumulator counters. Each column in this array of tubes is dedicated to 1 decade place of the ier; each row, to one of the digits between 0 and 9. When the program ring signals for multiplication by the ier digit in a particular decade place, the activated ier selector gate for that decade place emits a signal to the multiplication tables.

Static signals for the products of all digits between 1 and 9 by the particular ier digit are emitted from the multiplication table and converted into pulse form at the coding gates. The products from the tens and units tables respectively then go to the left and right hand sets of multiplicand selector gates. These gates are set up by the static outputs of the icand accumulator so that only the products appropriate to the digits of the icand are allowed to pass.

These partial products then go to the left and right hand shifters. Each set of shifters consists of a 10 by 10 array of gates. The gates on each

row are controlled by one stage of the program ring and the outputs of the gates are connected diagonally so that products are shifted successively one place to the right as multiplication by the ier digits progresses from left to right. The products are emitted from the 4 digit output terminals on panel 3 of the high-speed multiplier with those from the tens table being emitted by the terminals LH partial products accumulators I and II and those from the units table, by the terminals RH product accumulators I and II. The terminals identified by II and I respectively take care of the digits for decade places $10^0 - 10^9$ and $10^{10} - 10^{19}$.

Notice, that the high-speed multiplier transmits only the digits of the product but not the sign. For positive arguments, this results immediately in the correct signed product. If either or both of the arguments are negative, certain correction terms are needed to produce the correct signed products. From Table 5-1 in which the correction terms for the various cases are tabulated, it can be seen that whenever an argument is negative, the product obtained from the multiplication tables must be corrected by 10^{10} times the complement of the other argument. In the case where both arguments are negative, moreover, the sign of the product must be corrected. The programming circuits (see Sec. 5.2.) provide for the last correction by causing the 1'P to be transmitted over the PM lead of the digit output terminal RH product accumulator I. The programming circuits provide for the other corrections by causing the emission of program output pulses at the RS and/or DS output terminals. The operator must interconnect the multiplier with its associated accumulators so that these pulses stimulate the corrections to take place (see PX-6-311 and Sec. 5.4.).

TABLE 5-1

CORRECTION TERMS FOR NEGATIVE IER AND/OR ICAND.
R and D represent the absolute values of the ier and icand respectively.

	Case 1 Ier positive Icand negative	Case 2 Ier negative Icand positive	Case 3 Ier and Icand both negative
ier	P + (R)	M + (10^{10} - R)	M + (10^{10} - R)
icand	M + (10^{10} - D)	P + (D)	M + (10^{10} - D)
Product obtained from multiplication tables	P + (10^{10} R - RD)	P + (10^{10} D - RD)	$\underbrace{P+10^{20}}_{=M}$ + (RD - 10^{10}R - 10^{10}D)
Correction term needed	M + 10^{10} (10^{10} - R)	M + 10^{10} (10^{10} - D)	M + [P + 10^{10}(R)] + [P + 10^{10}(D)]
Correct signed product	M + (10^{20} - RD)	M + (10^{20} - RD)	P + (RD)

To summarize the discussion of the previous pages, multiplication of a 10 or fewer digit icand by a p digit ier required p + 4 addition times. These addition times are used for the following purposes:

1. reception of arguments
2. setting up of selector tubes and round off in LHPP accumulator
3. . . . p+2. } obtaining the partial products (icand)x (1 digit of the ier) successively for the p digits of the ier
- p+3. correcting products in case either one or both of the arguments are negative
- p+4. collecting the partial products so as to form the final product and clearing of the argument accumulators.

Tables 5-2 and 5-3 offer examples illustrating the operation of the high-speed multiplier. Although either the LHPP or RHPP accumulator can be used for forming the final product, we assume here, as in PX-6-311, that the RHPP accumulator is used for this purpose.

5.1. PROGRAM CONTROLS

Each of the high-speed multiplier's 24 program controls consists of a transceiver with program pulse input and output terminals, argument accumulator receive switches and clear switches, a significant figures switch, a places switch, and a product disposal switch. Neons correlated with the transceivers are shown on PX-6-309.

5.1.1. The Multiplier and Multiplicand Accumulator Receive Switches

Each of the argument accumulator receive switches has the positions α, β, γ, δ, ε, and 0. Associated with the points α-ε on the switch for the ier accumulators are the program pulse output terminals $R\alpha$-$R\varepsilon$ and, for the icand

TABLE 5-2

MULTIPLICATION OF M 8 198 630 400 by P 2 800 000 000

Description of Program: Multiply icand by 2 places of the ier
Round answer off to 8 places
Clear ier and icand accumulators after multiplication
Transmit product from final product accumulator

Add. Time	Ier accumulator stores PM 10 987 654 321	Icand accumulator stores PM 10 987 654 321	LHPP accumulator (I) Receives PM 10 987 654 321	LHPP accumulator (I) Stores after receiving PM 10 987 654 321	RHPP and FP Accumulator (I) Receives PM 10 987 654 321	RHPP and FP Accumulator (I) Stores after receiving PM 10 987 654 321
1	P 2 800 000 000	M 8 198 630 400	M 8 198 630 400			
2			0 0 000 000 050	P 0 000 000 050		
3			1 011 100 000	P 1.0011 100 050	0 628 626 080	P 0 628 626 080
4			0 607 642 030	P 1 618 742 080	0 048 245 402	P 0 676 874 482
5			M 7 200 000 000	M 8 818 742 080		
6					M 8 818 742 080	M 9 495 616 562
	Program output pulse and product disposal signal are emitted.					
7	Product is transmitted from product accumulator.					

TABLE 5-3

Multiplication of M 8 198 630 400 by M 2 800 000 000

Description of Program: Multiply icand by 3 places of ier
Do not round answer off
Clear ier and icand accumulators
Retain product in final product accumulator

Add. Time	Ier accumulator stores	Icand accumulator stores	LHPP accumulator (I) Receives	LHPP accumulator (I) Stores after receiving	RHPP and FP accumulator (I) Receives	RHPP and FP accumulator (I) Stores after receiving
	PM 10 987 654 321	PM 10 987 654 321	PM 10 987 654 321	PM 10 987 654 321	PM 10 987 654 321	PM 10 987 654 321
1	M 2 800 000 000	M 8 198 630 400				
2						
3			1 011 100 000	P 1 011 100 000	0 628 626 080	P 0 628 626 080
4			0 607 642 030	P 1 618 742 030	0 048 248 402	P 0 676 874 482
5			0 000 000 000	P 1 618 742 030	0 000 000 000 1'P 0 000 000 000	P 0 676 874 482 M 0 676 874 482
6			P 7 200 000 000	P 8 818 742 030	P 1 801 369 600	M 2 478 244 082
7					P 8 818 742 030	P 1 296 986 112
		Program output pulse is transmitted				

accumulator, Dα-Dε. If one of these switches is set at a receive point, a program pulse received on a program input terminal is retransmitted through the corresponding terminal Rα-Rε or Dα-Dε when the program control of which the switch is a part is stimulated. The operator sets up program controls on argument accumulators so that a pulse transmitted in this way will cause reception to take place as specified (see PX-6-311 and Sec. 5.4.).

The argument accumulator receive switches have been provided in order to simplify the programming of multiplications. Once the connections between some or all of the terminals Rα-Rε, Dα-Dε and the argument accumulators are made and switches have been set up accordingly on the argument accumulators, the operator does not need to provide the argument accumulators with a separate program pulse to stimulate them to receive whenever a multiplication is to take place. The one program pulse which stimulates the performance of the multiplication also stimulates the reception of the arguments provided that they can both be received during the first addition time of the multiplication.*

If an argument accumulator receive switch is set at 0, no pulse to stimulate reception of the corresponding argument is transmitted. The setting 0 is used for multiplication programs in which the argument is held over from the previous program (see Sec. 5.1.2.) or in programs in which it is desirable to stimulate the argument accumulator independently to receive its argument.

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*If, for example, both the ier and icand are received directly from the constant transmitter, the argument accumulators cannot both receive their arguments in the same addition time because the constant transmitter transmits but one number in an addition time.

5.1.2. Multiplier and Multiplicand Accumulator Clear Switches

Clear circuits in the high-speed multiplier are connected to the PM-clear units of the ier and icand accumulators. If an argument accumulator clear switch is set at C, the high-speed multiplier's clear circuits emit a clear signal towards the end of addition time p+4 which causes the corresponding argument accumulator to clear. In programs for which a clear switch is set at O, no clear signal is transmitted to the corresponding accumulator.

5.1.3. The Significant Figures Switch

The setting of the significant figures switch determines to which decade place of the LHPP accumulator 5 pulses for round off are transmitted. If this switch is set at $2 \leq s \leq 9$, the five round off pulses are sent to decade 10-s of LHPP accumulator I. For s=10, the round off pulses are sent to decade 10 of LHPP accumulator II.* No round off pulses are emitted in a program for which the significant figures switch is set at "off".

The significant figures switch provides greater flexibility in the round off options for the 24 programs than would be possible if the only round off control available were the significant figures switch on the final product accumulator. If, however, the round off requirements on all multiplication programs are the same, the significant figures switches of the multiplier program controls can be set at off and the significant figures switch on the final product accumulator can be set appropriately.

Notice that the setting of the significant figures switch of a multiplier program control does not cause the final product accumulator to emit the 1'P (needed for a complement with respect to 10^{10}) when the product is disposed of subtractively. Whether or not this pulse is put in, and the

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*Unless 2 pairs of interconnected accumulators are used to receive the partial products, the round off pulses emitted for s=10 are lost.

decade in which it is put, depend on the setting of the significant figures switch on the final product accumulator (see Sec. 4.1.4.). If a product is disposed of subtractively in such a way that the 1'P is not transmitted by the final product accumulator, the 1'P can be put in at the receiving accumulator (see Sec. 4.1.2.).

5.1.4. Places Switches

If the places switch of a program control is set at p (where $2 \leq p \leq 10$), the high-speed multiplier multiplies the entire icand by the p left hand digits of the ier whenever this program control is used. Such a program lasts p+4 addition times and a program output pulse is emitted by the transceiver p+4 addition times after the reception of the program input pulse.

5.1.5. Product Disposal Switch

The points A, AS, ..., ASC on the product disposal switch together with the program pulse output terminals A, S, ..., ASC at the left of panel 3 of the high-speed multiplier make it possible for this unit to direct the transmission of the product from the final product accumulator.

At the end of addition time p+4 when the high-speed multiplier program control emits a program output pulse, a pulse is also emitted from the terminal A, S, ..., or ASC corresponding to the point at which the product disposal switch is set. The product disposal program pulse output terminals which are used should be connected to program pulse input terminals on the final product accumulator (see PX-6-311). If a product disposal switch of a given program control is set at 0, the high-speed multiplier does not emit a product disposal pulse when this program control is used.

The program switches on the final product accumulator may, but need not necessarily, be set so as to correspond to the labelling of the

product disposal terminal from which the stimulating pulse comes. For example, if in a given program it is convenient to dispose of some product subtractively twice, and then clear and, moreover, no multiplication program requires ASC disposal, then the ASC output terminal can be connected to a repeat program control on the final product accumulator set up for subtractive transmission repeated 2 times with clearing. Notice that with such a set-up the point ASC on the product disposal switch no longer has the meaning transmit A and S simultaneously and clear but, rather, the meaning established by the set up of the program control on the final product accumulator.

In a course like the previously described one care must be exercised to prevent conflicting programs. Since during the first two addition times of a multiplication program, the RHPP accumulator has a completely non-active role, product disposal lasting 2 addition times is possible (with the RHPP accumulator used as the FP accumulator) even though a new multiplication program is initiated when the product disposal signal is emitted. If the product is disposed of repetitively r times (where $r > 2$), the next multiplication program must be initiated no sooner than $r-2$ addition times following the product disposal signal. It might also be mentioned at this point that repetitive reception of an argument cannot be accomplished through the use of the terminals Rα-Rε or Dα-Dε since the arguments must be received no later than the end of addition time 1 of a program in order to allow sufficient time for the selectors to set up.

5.2. COMMON PROGRAMMING CIRCUITS

5.2.1. Argument Accumulator Receive Circuits

A program input pulse delivered to a program control is routed

TABLE 5-4

CHRONOLOGICAL OPERATION OF HIGH SPEED MULTIPLIER'S PROGRAMMING CIRCUITS

Note: It is assumed here that ten-decade accumulators are used for the partial products.

Add. Time for 2 digit multiplier	Stage of Ring Counter	EVENT: In High Speed Multiplier's programming circuits	EVENT: In associated accumulators
End of Add. time 0	1	1) Program input pulse is received and retransmitted to ier and/or icand accumulators	1) See addition time 1.*
1	1	1) Ring cycles to stage 2 at CPP time.	*Ier and icand accumulators receive arguments.
2	2	1) 1P passed by B'47 sets l and r receivers. 2) 1'P gated through A'47 and 4P through A'46 are delivered to round off gates. 3) Ring cycles to stage 3.	1) LHPP and RHPP accumulators' "receive on σ" circuits are activated. 2) LHPP accumulator receives five round-off pulses.
3	3	1) Signal from stage 3 opens ier selector K gates so that multiplier tables are entered with first from the left ier digit. 2) Signal from stage 3 opens A" shifter gates. 3) Ring cycles to stage 4.	1 and 2) LHPP accumulator receives tens digits of "icand x first ier digit" in decade places 10 through 1. RHPP accumulator receives units digits of "icand x first ier digit" in decade places 9 through 1.
4	4	1) Signal from stage 4 opens ier selector J gates and shifter B" gates. 2) Signal from B'46 gates a 1'P through L'47. 3) Signal from B'46 gates CPP through B'46 to initiate RS and DS corrections if R and/or D are negative. 4) Signal from B'46 gates CPP through B'48 to provide reset signal for l and r receivers. 5) Signal from B'46 allows CPP to pass through F'48 to clear ring to stage 13.	1) LHPP accumulator receives tens digits of second P.P. in decade places 9 through 1. RHPP accumulator receives units digits of second P.P. in decade places 8 through 1. 2) PM counter of RHPP accumulator receives 1'P if both ier and icand are negative. 3) See addition time 5.** 4) LHPP and RHPP accumulators' "receive on σ" circuits cease to be activated.
5	13	1) Signal from stage 13 allows CPP to pass through D49 and K'50 to the reset flip-flops for program controls 1-8 and 17-24. 2) Signal from stage 13 gates a CPP through A'47 so that F pulse is emitted 3) Ring cycles to stage 14.	**RS and/or DS corrections are made (see addition time 4). 2) See addition time 6.***
6	14	1) Signal from stage 14 goes to reset gates of program controls 9-16 to reset these controls. All other program controls are reset by signals from reset flip-flops. 2) Icand and ier accumulator clear signals are emitted. 3) Program output pulse and product disposal signal are emitted. 4) Ring cycles to stage 1.	***LHPP and RHPP are combined. 2) Argument accumulators clear.
7	1		Product is transmitted from final product accumulator.

immediately through buffers (61 and 62 on program control 1, for example) to the argument receive switches for that control. Each receive point on these switches connects to one of 5 output circuits consisting of buffer, inverter, standard transmitter, and program pulse output terminal (Rα-Rε or Dα-Dε on front panel 1). The program output pulse transmitted in this way is taken to a program control on the argument accumulator to stimulate reception of the argument (see Sec. 5.4.).

5.2.2. Program Ring and Associated Circuits

When a high-speed multiplier program control is stimulated, the signal derived ultimately from the normally negative output of the flip-flop holds gate F'44 open so that a CPP is admitted to cycle the program ring one stage per addition time. The effect of signals from various stages of the ring on the round off, partial product receiver, complement correction, final product collection (F pulse), and program control reset circuits are discussed in this section. Mention is also made of the effect of signals from the ring on the numerical circuits which are discussed in greater detail in Sec. 5.3. Table 5-4 summarizes the chronological operation of the programming circuits for the case of a 2 place multiplier.

The program ring is in stage 1 when a program input pulse is received by some program control at the end of, let us say, addition time zero. During addition time 1, the argument accumulators receive their arguments (see Sec. 5.2.1.) and, at the end of addition time 1, the ring cycles to stage 2.

A signal from stage 2 opens gate B'47. The 1P passed through this gate sets the l and r receivers early in addition time 2. These receivers

are not reset until the end of addition time p+2 (see discussion below). As long as these receivers are set, a static signal is delivered to the l and r terminals on front panel 3. These signals, brought to interconnector terminals on the left and right hand partial products accumulators (see Sec. 5.4.), stimulate the reception, through the α input terminal, of the round off pulses (see discussion immediately following), the partial products emitted during the succeeding p addition times, and the 1'P to correct the sign of the product when both the ier and icand are negative. Since the l and r signals are brought directly into the "receive on α" programming circuits of the product accumulators, no program controls need be set up to program the reception of the partial products.

The signal from stage 2 of the ring also opens gates A'47 and A'46 so that the 1'P and 4P are passed. These five pulses, used for round off of the product, are delivered to the gates A"-H" and K" 45. Each of these gates is connected to a point on the significant figures switches as indicated on PX-6-308. The normally positive output of the activated program control's flip-flop through inverter 65, buffer 64, and point s on the significant figures switch, opens one of these gates so that the round off pulses are emitted over the lead for decade place 10-s of the left hand partial products digit output terminal I or over the lead for decade place 10 of the left hand partial products digit output terminal II.

In addition time 3, a signal from stage 3 through B'42 and inverter L1 is applied to the ier selector gates for the 10th decade place, K 2-11, and through inverter B'41, to the shifter gates A" 30-21 and 10-1. In this way, multiplication by the first digit of the ier takes place with the products being emitted on the leads for decades 10-1 of the digit output terminal LHPP

accumulator I and on the leads for decades 9-1 of the digit output terminal RHPP accumulator I, and for decade 10 of RHPP accumulator II. Similarly, in addition times 4, 5, ..., p+2, the ring causes multiplication by successive digits of the ier and the emission of the products shifted over one place to the right each time.

The places gates numbered B'-K'46 emit a signal on the coincidence of a signal from the normally negative output of the flip-flop (and buffer 61) passing through point p on the places switch and a signal from stage p+2 of the ring. The signal emitted by one of these gates terminates the multiplications by successive ier digits, causes complement correction to take place, and resets the l and r receivers.

The phase of the multiplication program in which the tables are used is terminated as follows: A CPP passed through gate F'48 at the end of addition time p+2 clears the ring to stage 13. At the same time, a CPP passed through gate E'47 resets the l and r receivers.

During addition time p+2, the signal from one of the places gates allows a 1'P to pass through gate L"47 and a CPP, through gate B"46. A static output signal from stage M of the ier accumulator's PM counter holds gate B"47 open so that gate B"47 passes the output of gate B"46 to the DS output terminal on panel 3. Similarly, if the icand is negative, the output of gate B"46 passes through gate C"47 to the RS terminal. The gates L"47, 45, and 43 are so arranged in series that the 1'P is allowed to reach the PM lead of terminal RHPP accumulator I only if both the ier and icand are negative. This latter pulse is received in the right hand partial product accumulator because the r receiver is not reset until the end of addition time p+2 after this pulse

has been emitted. With the associated accumulators set up as shown on PX-6-311, the pulses transmitted from terminals RS and DS stimulate the carrying out of the complement corrections (shown on table 5-3.) during addition time p+3.

At the end of addition time p+3, a CPP passes through gate A"47 which is held open by a signal from stage 13 of the ring. This pulse, transmitted through terminal F on panel 3, is used to stimulate the collection of the partial products into the final product (see PX-6-311 and Sec. 5.4.).

At the end of addition time p+4, the activated program control is reset and a program output pulse is transmitted. This resetting is accomplished in one way for program controls (9-16) on panel 2 and in a slightly different way for program controls (1-8 and 17-24) on the first and third panels.

The signal from stage 14, early in addition time p+4, is brought directly to gate 62 of transceivers on the second panel. This gate, controlled by the normally negative output of the flip-flop, then emits a signal which passes through inverter 65 and opens gate 68. The CPP passed through gate 68 at the end of addition time p+4 resets the flip-flop and is transmitted as a program output pulse.

Gate 62 of a transceiver on the first or third panel also gets a reset signal early in addition time p+4. This signal, however, is derived from one of the reset flip-flops (E, F 49 on panel 1 or L", K" 49 on panel 3). A signal from stage 13 opens gates D49 and K"50 to allow a CPP to pass and, thus, set the reset flip-flops on panels 1 and 3 respectively. The normally negative output of these flip-flops is then brought to gate 62 in the associated transceivers. Neons correlated with the reset flip-flops are shown on PX-6-309.

5.2.3. Argument Accumulator Clear Circuits

The reset signal, whether from stage 14 or from the reset flip-flops (see discussion immediately above), causes gate 62 of the stimulated transceiver to emit a signal early in addition time p+4. This signal, through inverter 65 and buffer 63, passes through the ier and/or icand accumulator clear switches to one or two of the argument accumulator clear gates B, D, F, and H30. The argument accumulator clear gates are so connected to points on the clear switches that gate H30 is opened if only the ier accumulator is to be cleared, gates D30 and F30 if both argument accumulators are to be cleared, and gate B30 if only the icand accumulator is to be cleared. Towards the end of addition time p+4, the carry clear gate (CCG) passes through the opened clear gate (or gates) to the PM-clear unit of the accumulator (or accumulators) to cause the clearing of the argument accumulators as specified by the settings of the argument accumulator clear switches.

5.2.4. Product Disposal Circuits

There are 6 product disposal circuits A, S, ..., ASC each consisting of a program pulse output terminal on panel 3, a transmitter, a gate D", E", ..., or J"47 and, a buffer D", E", ..., or J"46. Each of these circuits is connected to the corresponding point A, AS, ..., ASC on the product disposal switch.

The signal emitted by gate 62 of the stimulated program control when the reset signal arrives, passes through inverter 65, buffer 63 and the product disposal switch to the buffer of the appropriate product disposal circuit. Thus, the gate in such a circuit is held open to pass a CPP at the end of addition time p+4. This pulse, emitted from one of terminals A, S, ..., ASC at the end of addition time p+4, is used by the operator to stimulate

disposal of the product (see Secs.5.1.5. and 5.4.) which takes place during addition time p+5.

5.3. NUMERICAL CIRCUITS

The numerical circuits of the high-speed multiplier consist of the ier selector gates, the tens and units multiplication tables, the coding gates, the left and right hand icand selector gates, the left and right hand shifters, and the 4 digit output terminals, LH partial products accumulators I and II and RH product accumulators I and II on panel 3 (see PX-6-308).

The ier selectors consist of a 10 by 10 array of gates. The ier selector gate in row i (i = 0 to 9 from bottom to top) and column j (j = 10 to 1 from left to right) receives, as one input, the static output of stage i in decade counter j of the ier accumulator and, as its second input, a signal from stage 13-j of the multiplier ring. The output signal from a gate in row i activates row i of the multiplication tables.

In the tens table there are eight groups of vertical conductors corresponding to icand digits 2 to 9 and in the units table, 9 groups of vertical conductors corresponding to icand digits 1 to 9. The basic products are remembered by means of a pattern of connections between the horizontal conductors (from the ier selectors) and the vertical conductors (to the coding gates). Each of the vertical conductors is labelled so as to indicate the pulses (1, 2, 2', or 4) which are brought to the coding gate to which it is connected. No conductor is needed for icand equal to one in the tens table since the tens digit of any one digit ier by icand equal to one is zero.

Now, a signal from a gate in row i of the selectors is delivered through the connections between row i of the tables and the vertical conductors

to the coding gates. Since the output of the ier selector gate is negative the signals from the multiplication tables have an inhibitory effect on the coding gates to which they are delivered. Notice that for ier equal to zero, all coding gates are turned off. The 1, 2, 2', or 4P are allowed to pass through only the coding gates which receive no signal from the multiplication tables.

Suppose, for example, that the digit in the tenth decade place of the ier is 2. Then during addition time 3, the tube K9 emits a signal. The digit pulses passed by the coding gates as a result are shown in Table 5-5.

The pulses passed by the coding gates associated with the tens and units multiplication tables are brought through buffers and inverters to the left and right hand icand selector gates respectively. The left hand selectors consist of a 10 by 8 array of gates with the tubes in row i (i = 2 to 9 from bottom to top) corresponding to digit i of the icand and the tubes in column j (j = 10 to 1 from left to right) to decade place j of the icand. Similarly, the right hand icand selectors consist of a 10 by 9 array of gates with each of the 9 rows corresponding to a digit of the icand between 1 and 9. The static outputs of the icand accumulator's decade counters provide one input for the icand selector gates. The second input for the icand selector gates on row i consists of the pulses passed by the coding gates associated with icand i. Out of the collection of products transmitted by the coding gates, the icand selector gates select the products needed for the particular icand set up in them. For example, when the icand M 8 198 630 400 is multiplied by the first digit of the ier P 2 800 000 000 (see the illustrative problem of table 5-2), the product pulses passed by icand selector gates are shown

TABLE 5-5

PARTIAL PRODUCTS EMITTED BY THE MULTIPLICATION TABLES FOR IER = 2

	Icand	Coding Gates which receive signals from multiplication tables	Pulses passed by coding gates.
↑ TENS TABLE ↓	2	G48	none
	3	G47, F46	none
	4	G46, F46	none
	5	F45, E45	1P by G45
	. . .	. . .	. . .
↑ UNITS TABLE ↓	1	G29, E29, D29	2P by F29
	2	R28, E28	4P by D28
	3	G27, F27	2'P by E27 and 4P by D27
	. . .	. . .	. . .

in Table 5-6.

Corresponding to each set of icand selector gates is a set of shifters. Each set of shifters consists of a 10 by 10 array of gates. The pulses for the partial product "ier" digit by icand digit in decade place j" are routed through buffers and inverters to the shifter gates in column j (j=10 to 1 from left to right). The second input for the gates in row i (i= 3 to 12) comes from stage i of the program ring. The outputs of the shifters are connected diagonally to the leads of the digit output terminals, LH partial products accumulators I and II and RH product accumulators I and II, in such a way that the partial products are emitted one decade place further to the right as multiplication by successive ier digits takes place. The partial products for icand by first ier digit are emitted over the leads for decade places 10-1 of the left hand partial products accumulator I, decade places 9-1 of right hand partial products accumulator I, and decade place 10 of right hand partial products accumulator II.

Notice that the pulses for the partial products are emitted from inverter tubes instead of standard transmitters. For this reason, the digit output terminals on panel 3 must be connected to input terminals on the partial products accumulators by means of digit trays or cables to which no other units are connected in parallel. No load boxes are used on these digit trays (see Sec. 5.4.).

5.4. INTERRELATION OF THE HIGH-SPEED MULTIPLIER AND ITS ASSOCIATED ACCUMULATORS

5.4.1. Interconnections for Numerical and Programming Data

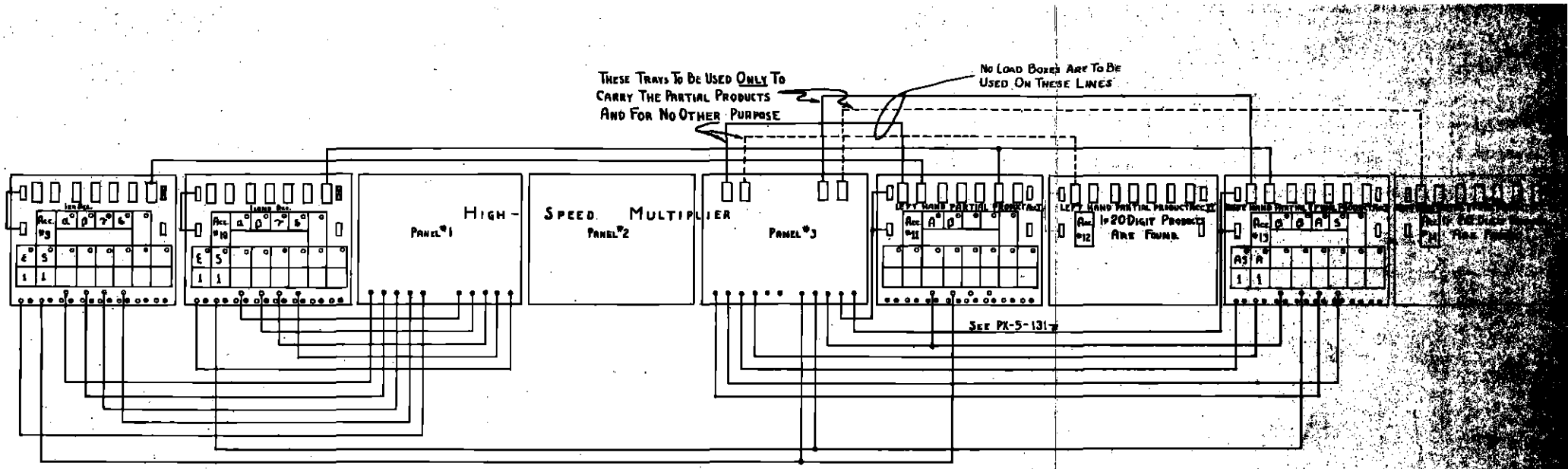
The 10 decade counters of the ier accumulator (9) are connected statically to the ier selector gates. Similarly, the decade counters of the icand

TABLE 5-6

SELECTION OF PRODUCTS BY ICAND SELECTORS WHEN ICAND M 8 198 630 400

IS MULTIPLIED BY FIRST DIGIT OF IER P 2 800 000 000

Decade Place	Left Hand Icand Selector Gate	Pulses Passed	Right Hand Icand Selector Gate	Pulses Passed
10	L'22	1	L'2	6
9	———	0	K'9	2
8	J'21	1	J'1	8
7	H'22	1	H'2	6
6	G'24	1	G'4	2
5	F'27	0	F'7	6
4	———	0	———	0
3	D'26	0	D'6	8
2	———	0	———	0
1	———	0	———	0



Note— Horizontal Lines Above The Units Represent Digit Trays. The Dotted Lines Represent Trays Which Need Be Used Only When 20 Digit Products Are Found.

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accumulator (10) are connected to both sets of icand selector gates. Stage M of the ier accumulator is statically connected to gates B"47 and L"45 and stage M of the icand accumulator, to gates C"47 and L"43 of the complement correction circuit (see Sec. 5.2.2.). Fifty leads in each of 4 55-conductor cables are used for the static outputs of the 20 decade counters involved. An additional lead in each of 2 of the cables carries minus sign data. These cables are brought from accumulators 9 and 10 to the selector gates in the high speed multiplier by way of the static cable trough which runs along the top of the ENIAC panels.

Only accumulators 9 and 10 which are next to the high-speed multiplier can be used as the ier and icand accumulators since only one addition time, the 2nd, is allowed (with a safety factor included) for the set-up of the arguments in the selectors. If longer static leads were used to deliver the arguments to the selectors, more time than has been provided would be needed to set up the arguments. As a matter of fact not even the ier and icand accumulators can be interchanged since the time constants have been measured on the basis that the further accumulator (9) is connected to the ier selectors on panel 1 and the nearer accumulator (10), to the icand selectors on panel 2 of the high-speed multiplier.

The outputs of gates B, D, F, and H50 in the clear circuits (see Sec. 5.2.2.) are also connected to the PM clear units of the argument accumulators.

All the other connections between the multiplier and its associated accumulators for numerical and programming purposes are made through digit or program trays or cables. These are shown on PX-6-311.

5.4.1.1. Programming Connections for "Receive Argument" Instructions

The terminals Rα-Rε are connected to program pulse input terminals on the ier accumulator. The program switches associated with these terminals are set up appropriately. Similarly terminals Dα-Dε are connected to program pulse input terminals on the icand accumulator. Although PX-6-311 shows all of the Rα-Rε Rα-Rε and Dα-Dε terminals connected, it is, of course, necessary to make connections only for the terminals which are used.

5.4.1.2. Connections for Partial Product Reception

The signals emitted through the l and r terminals on panel 3 of the high-speed multiplier during addition times 2 through p+2, are delivered to the "receive on α" programming circuits of the partial products accumulators by means of cables (see PX-5-131) running from the l and r terminals to interconnector terminals on the LHPP and RHPP accumulators respectively. The digit output terminals on panel 3 of the high-speed multiplier are connected to the α input terminals of the partial products accumulators. If products with 8 or fewer significant figures are required, the dotted digit connections may be omitted.

To repeat the statement made in Sec. 5.2.2, no other units can be connected in parallel to the trays used to carry the partial products and no load box should be used on these trays.

5.4.1.3. Connections for Complement Correction

The S output terminals of the ier and icand accumulators are connected to the β input terminals of LHPP Accumulator I and RHPP Accumulator I respectively for the purpose of delivering to these accumulators the correction terms required if either or both of the arguments are negative (see Table 5-1).

with these digit connections, the following program connections must be made:

1) from terminal RS on panel 3 to a control on the ier accumulator set up for subtractive transmission and to a control on the LHPP accumulator set up for reception on β.

2) from terminal DS on panel 3 to a control on the icand accumulator set up for subtractive transmission and to a control on the RHPP accumulator set up for reception on β.

A second method of making the complement correction connections is possible. The S output terminals of the ier and icand accumulators may be connected to the β input terminals of RHPP accumulator I and LHPP accumulator I respectively. In this case the program connections are as follows:

1) from terminal RS to the ier accumulator and to the RHPP accumulator

2) from terminal DS to the icand accumulator and to the LHPP accumulator.

5.4.1.4. Connections for Final Product Collection

PX-6-311 shows the partial product accumulators set-up so that the RHPP accumulator also serves as the final product accumulator. The A output terminal of the LHPP accumulator is connected to the β input terminal of the RHPP accumulator and the F terminal on panel 3 is connected to a control on the LHPP set up for reception on β. Since the RHPP accumulator is free for two addition times at the beginning of multiplication programs and the LHPP accumulator is free for only one addition time (see Sec. 5.1.5.), there is a slight advantage in using the RHPP accumulator as the final product accumulator if repetitive disposal of the product is contemplated. Otherwise, by suitable digit tray and programming connections, the LHPP accumulator can just as well be made to serve as the final product accumulator. Notice that it is not necessary to use a shifter at the β input terminal of the FP accumulator in collecting

the partial products in one accumulator because the high-speed multiplier's shifters align the partial products so that they can be combined properly.

5.4.1.5. Programming Connections For Product Disposal Instructions

PX-6-311 shows several of the A, S, ..., ASC terminals on panel 3 connected to program controls on the final product accumulator which are set-up for transmission. As mentioned earlier in Sec. 5.1.5., the meanings taken on by the points A, S, ..., ASC on the product disposal switch depend entirely on the set up of the program controls on the final product accumulator to which the terminals A, S, ..., ASC are connected.

5.4.2. Position of Decimal Point in Product Accumulator

The position of the decimal point of the product can easily be deduced from the description of the way in which the shifters route the partial products (see Sec. 5.3.). If r, d, and f respectively represent the number of decade places that the decimal points of the ier, icand, and final product are removed from the PM place in their respective accumulators (r, d, and f are positive or negative according as they are counted toward the right or left of the PM counter), then

$$f = r + d$$

This formula is illustrated in the table below.

ier	r	icand	d	product	f
P 1. 000 000 000	1	P 1. 000 000 000	1	P 0 1.00 000 000	2
P 0 03.0 000 000	3	P.4 000 000 000	0	P 0 P1.2 000 000	3
P 0 03.0 000 000	3	10^{-2}(P.4 000 000 000	-2	P 0. 012 000 000	1

5.5. ILLUSTRATIVE PROBLEMS

Programs set up on the high-speed multiplier are described in the high-speed multiplier column of set-up tables as follows:

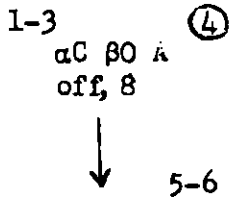
1) On the first level, i-j, at the left, represents the line from which the program input pulse comes and (k), at the right, the program control

2) On the second level, the first pair of symbols (α, ..., ε, or 0 followed by C or 0) represents the settings of the ier accumulator receive and clear switches; the second pair of symbols represents the settings of the icand accumulator receive and clear switches; the third symbol (A, ..., ASC, or 0) the setting of the product disposal switch; A special meaning assigned to one of the points on the product disposal switch is indicated by an asterisk and an explanatory note at the top of the high-speed multiplier column.

3) On the third level, the first symbol (2, ..., 10, or off) specifies the significant figures switch setting; the second symbol, the places switch setting.

4) On the fourth level, located on the addition time line in which the program is completed, the symbol m-n designates the program output pulse.

Thus, the following symbols



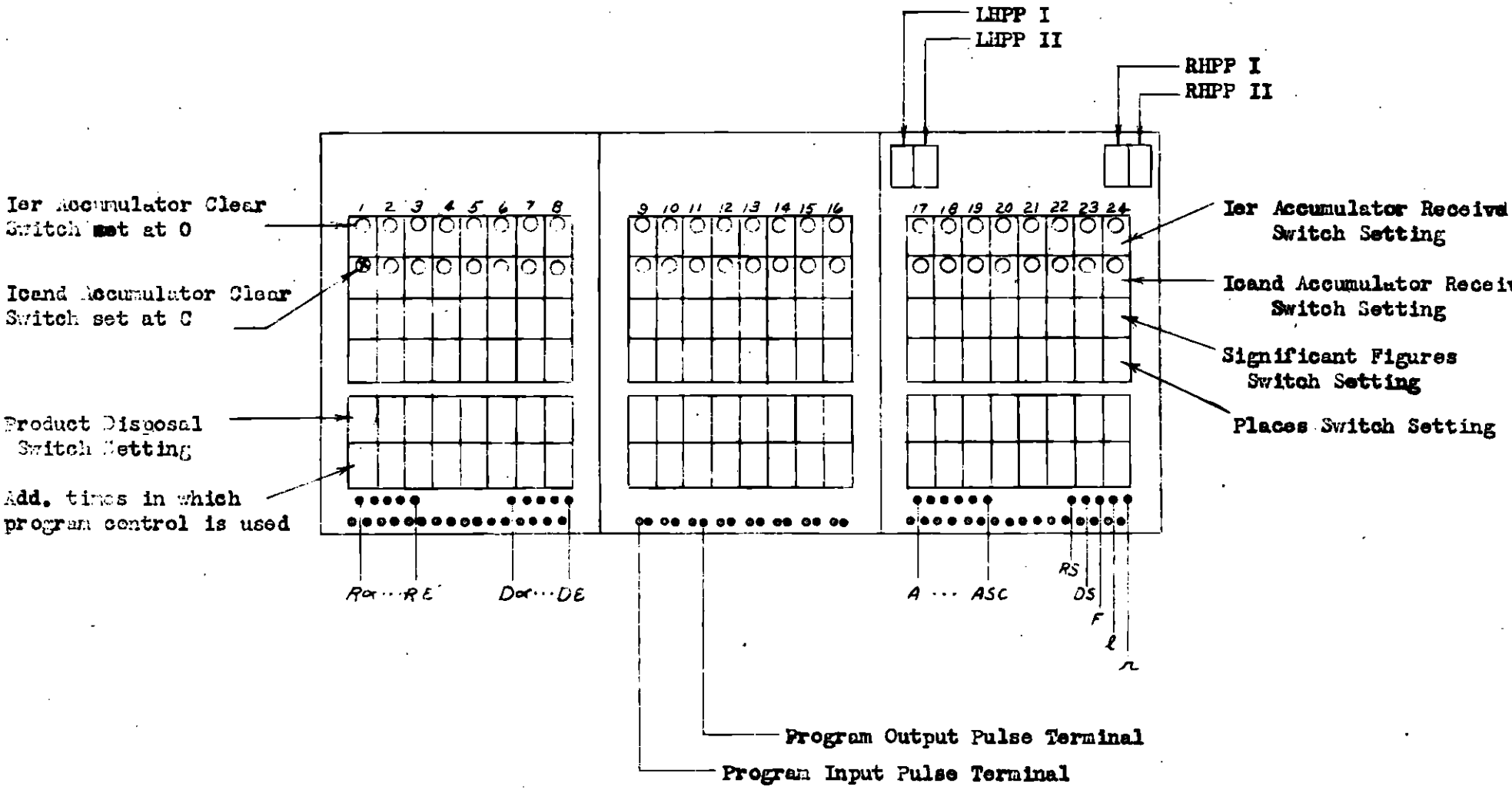
describe a program set up on high-speed multiplier control 4. The program input pulse comes from line 3 of program tray 1. The ier accumulator receives its argument through its α input terminal and the icand accumulator receives the icand through its β input terminal. The ier accumulator is, and the icand accumulator is not cleared at the end of the program. The product is transmitted additively from the final product accumulator. The product is not rounded off and 8 multiplier places are used. The program output pulse is transmitted to line 5-6. If the program input pulse 1-3 were received, say, at the end of addition time 6, all the above symbols except the arrow and the program output pulse would appear on the addition time 7 line. The arrow would run from the line for addition time 7 to the line for addition time 18. The program output pulse symbol would appear on line 18.

No symbols are written in the columns for accumulators associated with the high-speed multiplier when these accumulators carry out programs (receiving the arguments, for example) stimulated by the high-speed multiplier. The set-up diagrams, however, indicate the semi-permanent connections made between the high-speed multiplier and these accumulators.

For the symbols used on the set-up diagrams see Fig. 5-1 below.

5.5.1. <u>One Program Control Devoted to Each Multiplication</u>

The problem of Sec. 7.5.1. which describes the way in which the ENIAC can be set up to perform quadratic Lagrangian interpolation illustrates one method of using the program controls on the high-speed multiplier. Here it is assumed that the interpolation is carried out as part of a computation which does not come anywhere near exhausting the program control facilities of the high-speed multiplier. Since sufficient program controls are available, one control is devoted to each multiplication program.



The terminals on associated accumulators to which terminals Rα-RE, Dα-DE, A-ASC, RS, DS, and F are connected are marked with a corresponding symbol.

Fig. 5-1

SET-UP DIAGRAM CONVENTIONS FOR HIGH-SPEED MULTIPLIER

The stimulating pulses for the various multiplication programs are derived directly from the main programming sequence and the multiplier's program output pulses go back to the main programming sequence (see Table 7-4).

5.5.2. One Program Control Used Repeatedly

The computation discussed in section 6.5 which consists of forming

$$x = \frac{\sqrt{a} + \sum_{i=1}^{3} x_i^3}{b} + cd$$

illustrates the repeated use of a given high-speed multiplier program control. In this computation, the three pairs of multiplications to form the terms x_i^2 and then x_i^3, while they involve different arguments, can be handled by one pair of multiplier controls. Here again the pulses which stimulate the multiplication programs as well as the ones which stimulate transmission of x_1, x_2, and x_3 to the argument accumulators are derived from the main program sequence. However, after each term x_i^3 is formed and received in another accumulator from the final product accumulator, the program sequence goes to the master programmer for instructions as to whether or not the multiplier program controls used repeatedly for the formation of x_i^2 and x_i^3 are to be used again and, if so, with which argument (see Table 6-13).

The problem of Sec. 6.5. also illustrates the use of one of the points on the product disposal switch to effect repeated transmission from the final product accumulator.

5.5.3. Isolation of Program Sequences Which Stimulate Transmission of Arguments to Argument Accumulators, Multiplication Programs, and Reception of Products From Product Accumulators.

In Sec. 8.7 is described a problem in which there is a basic computation sequence involving 17 multiplications. This basic sequence is repeated 10 times in the course of the problem. One program control is devoted to each of 12 of the multiplications and the remaining 5 multiplications are taken care of by either of 2 program controls. Each time the basic computation sequence is repeated, arguments stored in different units of the ENIAC are used. Also, within each sequence, the location of one of the arguments required in the 5 multiplication programs which are performed on 2 program controls, as mentioned above, varies. Furthermore, in alternate repetitions of the basic computing sequence, 6 of the 17 products are received by way of different input terminals in the accumulators to which the final product accumulator transmits.

The set up for this problem is summarized in Table 8-13 As much of the basic computing sequence as is constant for all 10 repetitions is handled in one predominant program sequence. In this predominant program sequence, the same program input pulse which stimulates a multiplication program also stimulates the accumulators which store arguments for the multiplication to transmit them and the program output pulse from a multiplier program control not only stimulates the reception of the product from the final product accumulator, but also initiates the next multiplication program. The program pulses for thie predominant sequence are carried in program trays 7 and 8 (see Table 8-13.

Branching off the predominant program sequence and carried on in parallel with it are three sequences. The sequence whose stimulating program pulse is carried on program line 6-11 is concerned with procuring appropriate arguments in the cases where the location of argument varies from repetition to repetition. A second sequence whose program pulses are carried on program tray 9 is concerned with selecting which of 2 multiplier controls is to be used for 5 of the 17 multiplications and with stimulating the transmission of an appropriate argument. A third sequence whose program pulses are carried on trays 10 and 11 handles the reception of 6 of the 17 products from the final product accumulator.

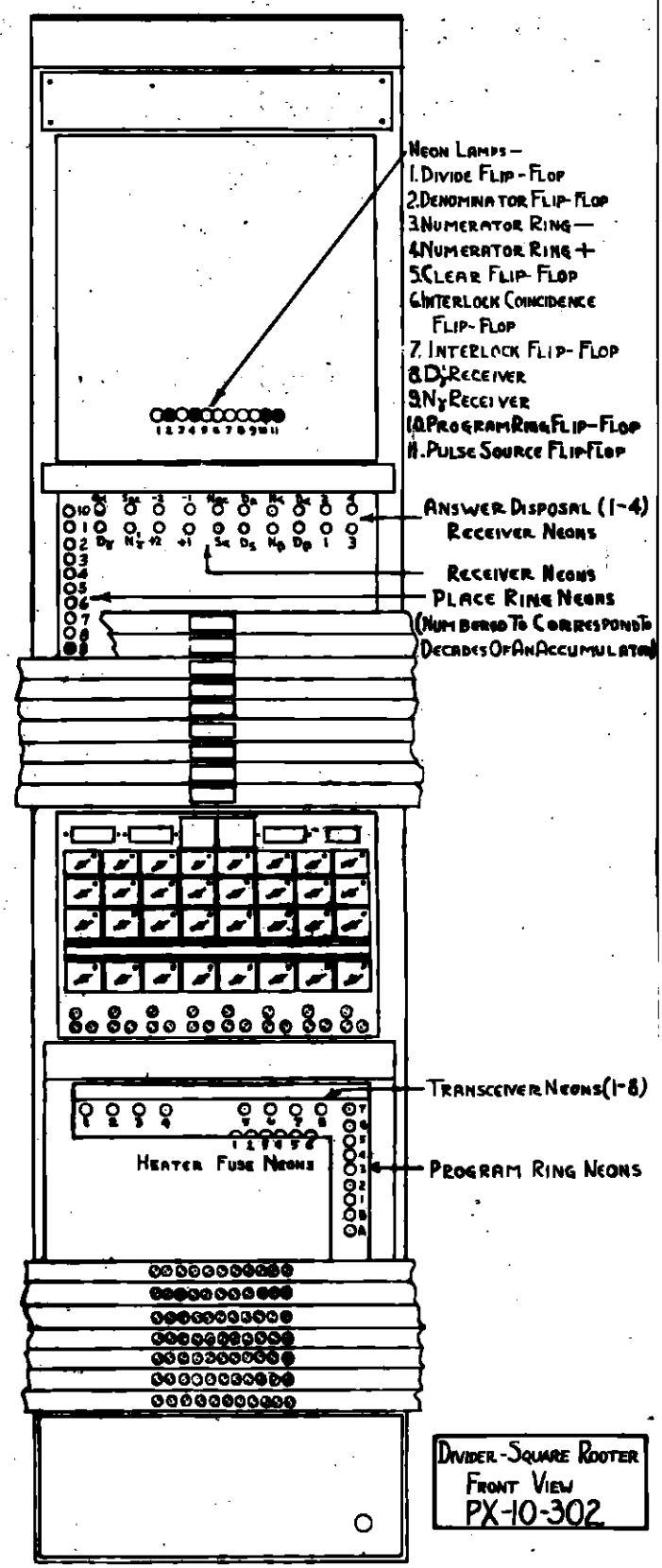
The iteration of the predominant sequence with its branches 10 times is provided through the use of the master programmer.

Neons On During Division

Add. Time	Prog. Ring	Place Ring	Receiver	1	2 D	3 N⁻	4 N⁺	5	6	7	8 D_Y'	9 N_Y	10	11
I-1	A	9		①	ON		ON						ON	ON
2	B	9		ON	②	③							ON	ON
3	1	9		"	"	"							ON	ON
II-1	A	i^*	D_A or D_S	"	"	③						ON		ON
2	A	i	-1 or +1, Q_α	"	"	"								ON
S 1	A	Cycles	N_{AC}, S_α	"	"	"					ON			ON
S 2	A	$I-1$	S_{AC}, N_Y'	"	"	Cycles					ON			ON
III 1	A	10-p	N_{AC}, S_α	"	"	③					ON			
2	B	"	S_{AC}, N_Y'	"	"	Cycles								
3	1	"	D_S or D_A	"	"	③						ON		
4	2	"	D_S or D_A	"	"	"						ON		
5	3	"	D_S or D_A	"	"	"						ON		
6	4	"	D_S or D_A	"	"	"						ON		
7	5	"	D_S or D_A	"	"	"						ON		
8	6	"		"	"	"								
9	7	"	(+1 or -1, Q_α)**	"	"	"								
IV-1	7	"		"	"				⑤	④				⑤
2	7	"		"	"		⑥	"	"					"
Transceiver Off	A	9	1, 2, or Neither	ON	ON		ON						ON	ON

Neons On During Square Rooting

Add. Time	Prog. Ring	Place Ring	Receiver	1	2 D	3 N⁻	4 N⁺	5	6	7	8 D_Y'	9 N_Y	10	11
I-1	A	9		①	ON		ON						ON	ON
2	B	9			"		ON						ON	ON
3	1	9			"		ON						ON	ON
4	A	9	$D_{Y'}+1$		"		ON							ON
II-1	A	i^*	D_S or D_A		"	③						ON		ON
2	A	i	+2 or -2, D_Y		"	"								ON
S 1	A	Cycles	-1 or +1, S_α, N_{AC}		"	"					ON			ON
S 2	A	$i-1$	-1 or +1, N_Y', S_{AC}		"	Cycles					ON			ON
III-1	A	10-p	-1 or +1, S_α, N_{AC}		"	③					ON			
2	B	"	N_Y', S_{AC}		"	Cycles								
3	1	"	D_A or D_S		"	③						ON		
4	2	"	D_A or D_S		"	"						ON		
5	3	"	D_A or D_S		"	"						ON		
6	4	"	D_A or D_S		"	"						ON		
7	5	"	D_A or D_S		"	"						ON		
8	6	"			"	"								
9	7	"	(-2 or +2, D_Y)**		"	"								
IV-1	7	"			"	"			⑤	④				⑤
2	7	"			"	"		⑥	"	"				"
Transceiver Off	A	9	3, 4, or Neither		ON		ON						ON	ON



Divider-Square Rooter
Front View
PX-10-302

Foot Notes –

① · On If Previous Program Was A Division.

② · On If Denominator Is Positive When Received In Denominator Accumulator.

③ · If, Before Denominator Is Added To Or Subtracted From Numerator, The Numerator Is Positive, Neon *4 Is On; Otherwise Neon *3 Is On.

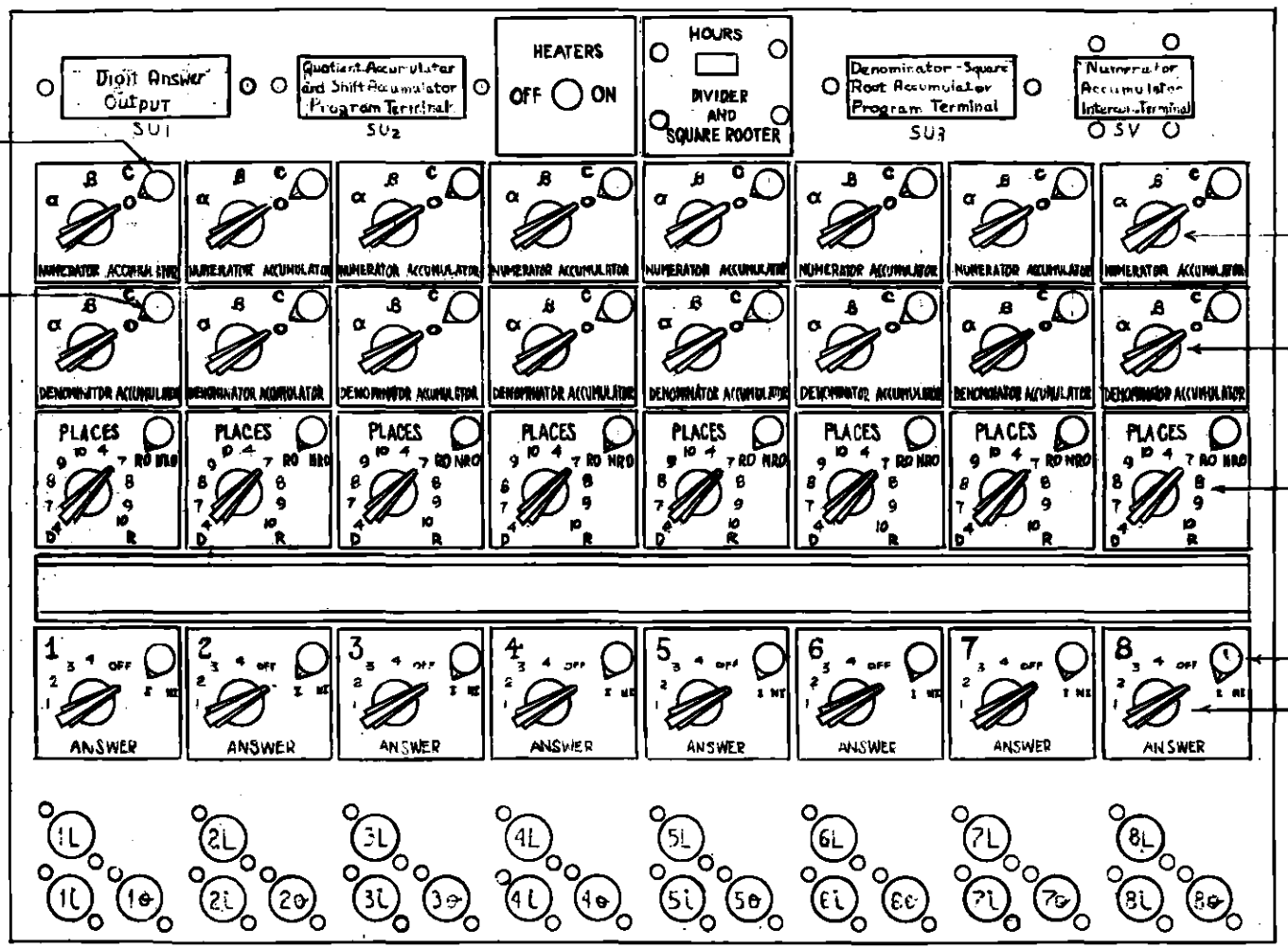
④ · Goes On When Interlock Pulse Is Received.

⑤ · Go On One Addition Time After III-9

⑥ · Goes On: a- In NI Case, Two Addition Times After III-9.
b- In I Case, In Whichever Occurs Later: Two Addition Times After III-9 Or One Addition Time After Neon 7.

** Only If No Overdraft Results.

* $9 \geq i \geq 10-p$ Where p Is The Setting Of The Places Switch.



Terminals 1ℓ, 2ℓ, ..., 8ℓ
Program input pulse terminals for programs 1-8 respectively.
Terminals 1e, 2e ..., 8e
Program output pulse terminals for programs 1-8 respectively.
Terminals 1L, 2L, ..., 8L
Interlock input pulse terminals for programs 1-8 respectively.

DIVIDER AND SQUARE ROOTER
FRONT PANEL
PX-10-501R

VI. DIVIDER AND SQUARE ROOTER

The divider and square rooter is the unit which enables the ENIAC to carry out the operations of division and square rooting. The time required to complete these operations depends on the number of places required in the answer and the digits in each place of the answer. If it is assumed that the average digit of the answer is 5 and if p designates the number of places in the answer, approximately 13 p addition times* are consumed in division or square rooting.

The first section of this chapter contains a general summary of the divider and square rooter. Sections 6.1, 6.2, and 6.3 respectively cover the program controls, common programming circuits, and numerical circuits of this unit. Information pertinent to the interrelation of accumulators associated with the divider and square rooter appears in Section 6.4, and 6.5 includes an illustrative set-up for computations involving the divider and square rooter. The following diagrams will be referred to in this chapter:

Front View of the Divider and Square Rooter	PX-10-302
Divider and Square Rooter Front Panel	PX-10-301
Divider and Square Rooter Block Diagram	PX-10-304
Interconnection of Divider and Square Rooter with its Associated Accumulators	PX-10-307

6.0. GENERAL SUMMARY

The divider and square rooter carries out a division or square rooting by operating as a central programming agent for a group of associated accumulators (see Section 6.4). In division the associated accumulators are the numerator (dividend) accumulator, the denominator (divisor) accumulator, shift accumulator,

*In Section 6.2 a formula for calculating exactly the number of addition times required for a given division or square root is given.

and quotient accumulator; in square rooting the associated accumulators are the numerator (radicand) accumulator, the shift accumulator, and the denominator (twice the root) accumulator. The divider controls these accumulators in the sense that at various periods of the operation cycle, it transmits to these accumulators program signals appropriate to the period of the computation and the quantities involved in the computation and in the sense that it provides the answer accumulator with the numerical data from which the answer is ultimately formed.

The operation cycle, whether for division or square rooting, divides itself rather clearly into 4 periods: period I in which the stage is set for the following periods, period II during which the operation itself proceeds, period III, the round off period, and period IV, the interlock and clear period. When a divider and square rooter program control is stimulated, the events which occur in the four periods mentioned above, depend, to some extent, on the way in which the program control is set up. (cf. Section 6.1 and the illustrative examples in Tables 6-2 and 6-3).

In addition to a transceiver with program pulse input and output terminals, each of the 8 program controls contains an interlock pulse input terminal and 8 program switches (see PX-10-301). The program switches provide the operator with options as to:

1) reception of the arguments by the argument accumulators (numerator and denominator accumulator receive switches)
2) clearing of one or both of the argument accumulators upon completion of the program (numerator and denominator accumulator clear switches)

3) choice between the operations of division and square rooting (divide-square root and places switch)

4) the number of places to be obtained in the answer (divide-square root and places switch)

5) round-off or no round-off of the answer (round-off switch)

6) whether or not the transmission of a program output pulse is to wait on the divider-square rooter's reception of an interlock input pulse (interlock switch)

7) transmission of the answer from the quotient or denominator accumulator (answer disposal switch).

During period I of a division, the divider and square rooter emits signals which stimulate the argument accumulators to receive the arguments in accordance with option 1 above and sets up certain of its common programming circuits (see Section 6.2) in accordance with option 3.

Period II, for division, includes combinations of a basic division sequence and a shift sequence. When the numerator and denominator have like signs, the denominator is subtracted from the numerator and the quotient is increased by one unit in a particular decade place; when the signs of the arguments are unlike, the denominator is added to the numerator and the quotient is decreased by one unit in a particular decade place. When the remainder from the numerator after an addition or subtraction of the denominator shows an overdraft (i.e. a change in sign from the one which the remainder carried before the addition or subtraction), the basic division sequence is interrupted. Then the remainder is transmitted from the numerator accumulator to the shift accumulator where it is received shifted over one place to the left. Next the numerator

accumulator again receives the numerator from the shift accumulator. The basic division sequence is repeated with the quotient respectively increased or decreased by one unit after every time a subtraction or addition of the denominator takes place. After a shift sequence, however, the unit is added to or subtracted from a decade place of the quotient one further to the right than before the shift sequence.*

Square roots in the ENIAC are obtained by a method which makes use of the fact that $\sum_{i=1}^{a} (2i - 1) = a^2$ and which is analogous to a method often used to find square roots on electric or manual desk computing machines.

Period I for square-rooting not only covers the reception of the numerator (or radicand) and the set-up of certain circuits in the divider and square rooter, but also provides for the reception of one pulse in the 10^8 decade of the denominator (twice the root) accumulator.

In the basic square-rooting sequence of period II, odd numbers successively increasing (and accumulated in the denominator accumulator) are subtracted from the radicand until an overdraft occurs. Then odd numbers successively decreasing are added to the radicand. The ENIAC finds by this procedure twice the square root (formed in the denominator accumulator) since the answer is increased or decreased by two units after each addition or subtraction takes place. Period II, in square rooting as in division, includes a shift sequence which takes place whenever the remainder from the radicand indicates a change of sign. The square root shift sequence provides for transmission of the radicand to the shift accumulator to shift it one place to the left and the return of the shifted radicand to the numerator or radicand accumulator. The shift sequence, further-

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*From the time that period II begins until just after the first overdraft, one unit is added to or subtracted from the 10^8 decade of the quotient in the basic division sequence. After the first shift sequence, the 10^7 decade of the quotient is worked on by the divider etc.

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TABLE 6-1

EXTRACTION OF SQUARE ROOTS BY THE DIVIDER AND SQUARE ROOTER - Period II

PROBLEM: To find $\sqrt{R}$ where $R = N^2 - e$

Assume $10^{2n-2}a_0^2 + 10^{2n-3}2a_0a_1 + 10^{2n-4}(2a_0a_2 + a_1^2) + 10^{2n-5}(2a_0a_3 + 2a_1a_2) + \cdots + a_n^2$

So that* $N = 10^{n-1}a_0 + 10^{n-2}a_1 + 10^{n-3}a_2 + \cdots + a_n$ where the a_i are integers between 0 and 9

When the square rooting commences, the numerator accumulator holds N.

OPERATION PERFORMED ON CONTENTS OF NUMERATOR ACCUMULATOR	REMAINDER IN NUMERATOR ACCUMULATOR AS A RESULT OF OPERATION IN COLUMN 1.	CONTENTS OF DENOMINATOR (TWO-ROOT) ACCUMULATOR
In basic square rooting sequence before first overdraft, SUBTRACT $10^{2n-2}\sum_{i=0}^{i=0}(2a_i+1) = 10^{2n-2}a_0^2 + 10^{2n-2}(2a_0+1)$	$10^{2n-2}(2a_0+1) + 10^{2n-3}(\cdots) + 10^{2n-4}(\cdots) + \cdots$	AFTER OVERDRAFT OCCURS BUT BEFORE SHIFT SEQUENCE $10^{n-1}[2a_0+1] = 0$ AT END OF FIRST ADDITION TIME OF SHIFT SEQUENCE $10^{n-2}[2a_0+1]$ AT END OF SHIFT SEQUENCE $10^{n-1}[2a_0+1] = 10^{n-1}$
After first shift sequence, but before second overdraft ADD $10^{2n-4}[2(2a_0+1)][10-a_1] - 10^{2n-4}\sum_{i=0}^{i=0}(2a_i+1)$ $= 10^{2n-3}(2a_0+1) - 10^{2n-4}(2a_0a_1) - 10^{2n-4}a_1^2$	$10^{2n-3}(2a_0a_1) + 10^{2n-4}(2a_0a_2 + a_1a_2) + \cdots + a_1^2 + e$	AFTER OVERDRAFT OCCURS BUT BEFORE SHIFT SEQUENCE $10^{n-2}[2(10a_0+a_1)+1] = 10^{n-2}[2(10a_0+a_1)+1] = 0$ $2[10^{n-2}a_0 + 10^{n-3}a_1] = 10^{n-1}$ AT END OF FIRST ADDITION TIME OF SHIFT SEQUENCE $2[10^{n-2}a_0 + 10^{n-3}a_1]$ AT END OF SHIFT SEQUENCE $2[10^{n-2}a_0 + 10^{n-3}a_1] + a_2^2$

* Compare N with the column showing the contents of the denominator accumulator and note the displacement of the answer. (See Sec. 6.4.3.)

more, provides for the subtraction or addition respectively of one unit first in the decade place in which twice the root was previously increased or decreased by two units in the basic square root sequence and then in a decade place one further to the right. After a shift sequence the basic square root sequence is repeated until overdraft occurs. Table 6-1 shows the contents of the radicand accumulator and of the twice the root accumulator at various times in period II of square rooting.

Period II is terminated and period III initiated when an overdraft occurs and when the divider and square rooter has found the number of places (counting toward the right from the PM decade) of the answer specified by the setting of the divider-square root and places switch of the answer. In division, period III includes the shifting of the numerator one place to the left as in the shift sequence of period II. Then, if round-off is specified by the setting of the program control, the denominator is subtracted from or added to the numerator (if the numerator's remainder and the denominator have like or unlike signs respectively) five times. If overdraft does not result from these subtractions or additions, the quotient is respectively increased or decreased by one unit in the last place from the left required by the setting of the places switch. Period III of square rooting is similar to that for division except for two details. In square rooting this period covers the shifting of the radicand's remainder and the addition or subtraction of one unit in the decade place of twice the root which, in the previous basic square root sequence, was decreased or increased by two units. Also, in square-rooting as in division, if round-off is specified, the contents of the denominator accumulator are then subtracted from or added to the contents of the numerator accumulator. If no overdraft

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TABLE 6-3

SQUARE ROOT - ILLUSTRATIVE PROBLEM

Problem: Find $\sqrt{\text{P 0 081 360 400}}$. Round answer off to 4 places. No interlock

Period	Add. Time	Numerator (Radicand) Accumulator		Denominator (2 root) Accumulator		Shift Accumulator	
		Receives	Stores after receiving	Receives	Stores after receiving	Receives	Stores after receiving
I	1	P 0 081 360 400	P 0 081 360 400				
	2						
	3						
	4			P 0 100 000 000	P 0 100 000 000		
II	5	M 9 900 000 000	M 9 981 360 400				
	6			P 0 200 000 000	P 0 300 000 000		
shift	7			M 9 900 000 000	P 0 200 000 000	M 9 813 604 000	M 9 813 604 000
shift	8	M 9 813 604 000	M 9 813 604 000	M 9 990 000 000	P 0 190 000 000		
	9	P 0 190 000 000	P 0 003 604 000				
	10			M 9 980 000 000	P 0 170 000 000		
shift	11			P 0 010 000 000	P 0 180 000 000	P 0 036 040 000	P 0 036 040 000
shift	12	P 0 036 040 000	P 0 036 040 000	P 0 001 000 000	P 0 181 000 000		
	13	M 9 819 000 000	M 9 855 040 000				
	14			P 0 002 000 000	P 0 183 000 000		
III	15			M 9 999 000 000	P 0 182 000 000	M 8 550 400 000	M 8 550 400 000
	16	M 8 550 400 000	M 8 550 400 000				
	17	P 0 182 000 000	M 8 732 400 000				
	18	P 0 182 000 000	M 8 914 400 000				
	19	P 0 182 000 000	M 9 096 400 000				
	20	P 0 182 000 000	M 9 278 400 000				
	21	P 0 182 000 000	M 9 460 400 000				
	22						
	23			M 9 995 000 000	P 0 180 000 000		
IV	24						
	25		Program output pulse and answer disposal signal is transmitted.				
	26		Answer is transmitted from denominator accumulator.				

TABLE 6-2

DIVISION - ILLUSTRATIVE PROBLEM

Problem: Divide P 0 2090070 000 by P 0 230 000 000. Round answer off to 4 places. No interlock.

Period	Add. Time	Quotient Accumulator		Numerator Accumulator		Denominator Accumulator	Shift Accumulator	
		Receives	Stores after Receiving	Receives	Stores after Receiving	Receives during period 1 and stores thereafter.	Receives	Stores after Receiving
I	1			P 0 209 070 000	P 0 209 070 000	P 0 230 000 000		
	2							
	3							
II	4			M 9 770 000 000	M 9 979 070 000			
	5	P 0 100 000 000	P 0 100 000 000					
shift	6			~~~~~			M 9 790 700 000	M 9 790 700 000
	7			M 9 790 700 000	M 9 790 700 000		~~~~~	
	8			P 0 230 000 000	P 0 020 700 000			
	9	M 9 990 000 000	P 0 090 000 000					
shift	10			~~~~~			P 0 207 000 000	P 0 207 000 000
	11			P 0 207 000 000	P 0 207 000 000		~~~~~	
	12			M 9 770 000 000	M 9 977 000 000			
	13	P 0 001 000 000	P 0 091 000 000					
III	14			~~~~~			M 9 770 000 000	M 9 770 000 000
	15			M 9 770 000 000	M 9 770 000 000		~~~~~	
	16			P 0 230 000 000	P 0 000 000 000			
	17			P 0 230 000 000	P 0 230 000 000			
	18			P 0 230 000 000	P 0 460 000 000			
	19			P 0 230 000 000	P 0 690 000 000			
	20			P 0 230 000 000	P 0 920 000 000			
	21							
	22	P 0 000 000 000	P 0 091 000 000					
IV	23							
	24		Program output pulse and answer disposal signal is transmitted					
	25		Answer is transmitted from quotient accumulator.					

results, twice the root is increased or decreased by two units.

Period IV is identical in both division and square rooting. In this period, ring counters (see below and Section 6.2,) in the divider and square rooter are cleared and certain flip-flops are reset so as to ready the divider and square rooter for the next program. A program output pulse is transmitted either to indicate the completion of the operation or the reception of an interlock input pulse as well at the completion of the operation. The divider-square rooter signals for the disposal of the answer in accordance with the setting of the answer disposal switch at the end of period IV and the numerator and denominator accumulators clear or do not clear in accordance with the settings of the numerator and denominator accumulator clear switches.

The events described above are motivated by the divider and square rooter's common programming circuits (see Section 6.2). The answer which is accumulated in the quotient accumulator in division or in the denominator accumulator in square rooting is supplied by the numerical circuits (see Section 6.3) of the divider and square rooter.

The common programming circuits of the divider-square rooter which are operated by the program controls may be divided roughly into 3 categories: circuits which are concerned solely with programming within the divider-square rooter (internal programming circuits); circuits which program the associated accumulators as well as other circuits within the divider (internal - external programming circuits); and circuits concerned solely with programming the accumulators associated with the divider and square rooter (external programming circuits).

The internal programming circuits (see PX-10-304) include the program

ring circuit, the overdraft circuit, the sign indication circuit, the divide flip-flop, and the interlock and clear circuit.

The program ring circuit contains a flip-flop called the pulse source flip-flop which controls the emission of certain specialized pulses (see Section 6.2) used only in the divider and square rooter. Which pulses are emitted depends on whether division or square rooting is the operation and also on the period of the computation. The 9 stage program ring directs the progress of the computation by providing gates for particular signals suitable to the phase of the computation at various times. The cycling of the program ring is controlled by the program ring flip-flop and by certain of the special pulses whose emission in turn, is controlled by the pulse source flip-flop.

The overdraft circuit has for its purpose the sensing of overdrafts. It consists of a binary ring counter (called the numerator ring) for registering the sign of the numerator. This ring is cycled only during period I and just after the numerator is shifted to the shift accumulator in periods II and III. In addition to the numerator ring, the overdraft circuit has four gates each of which is connected to a stage of the numerator ring and statically to the PM counter of the numerator accumulator. As long as the remainder from the numerator remains the same as it was before an addition or subtraction of the denominator, this circuit emits an NO (no overdraft) signal. When the numerator's remainder changes sign an O (overdraft) signal is emitted.

The sign indication circuit compares the signs of the numerator and denominator emitting a like sign signal when numerator and denominator have the same sign and an unlike sign signal when the signs of the numerator and denominator differ. The denominator flip-flop in this circuit is set only if the

denominator is negative. The denominator flip-flop feeds to each of four gates which have for their second input static leads from the PM counter of the numerator accumulator.

The divide flip-flop is used to remember whether the operation being performed is division or square rooting. This flip-flop affects programming only during the round off period at which time its intervention results in the emission of the instructions which distinguish period III for division from period III for square rooting.

The interlock and clear circuit which consists of the interlock flip-flop, the interlock coincidence flip-flop, the clear flip-flop and the various gates operated by these flip-flops, during period IV, emits signals which clear the divider and square rooter's rings and reset certain of its flip-flops.

The circuits which are both internal and external programming circuits are those containing the receivers which, when set, motivate the accumulators associated with the divider and square rooter to perform certain suboperations involved in division and square rooting and which also stimulate other programming circuits within the divider and square rooter to function (see Section 6.2). The receivers included in this category are the N_γ, D_A, D_S, Q_α, D_γ, D'_γ, S_α and N_{AC} and S_{AC} and N'_γ receivers. Signals from these receivers are delivered to the associated accumulators by means of special cables leading from the quotient accumulator and shift accumulator program terminal, the denominator and square root accumulator program terminal, and the numerator accumulator interconnector terminal (see PX-10-301) to interconnector terminals on accumulators corresponding to the names of the terminals on the divider and square rooter.

The N_γ receiver stimulates the reception, via the numerator accumulator's γ input channel, of the denominator or the complement of the denominator when either of these quantities is transmitted from the denominator accumulator as a result of the setting of the D_A or D_S receivers during the basic division or square rooting sequence of period II or in round off during period III.

The Q_α receiver controls the reception, via the quotient accumulator's α channel, of the units which are used to form the quotient and which are transmitted by the divider and square rooter whenever the basic division sequence of period II takes place or at the end of period III in round off programs if no overdraft results from the addition or subtraction of five times the denominator from the numerator.

The D_γ receiver controls the reception by the denominator accumulator via its γ channel of the +2 or −2 units transmitted by the divider and square rooter every time the basic square rooting sequence of period II occurs or in period III if no overdraft occurs after the addition or subtraction of 5 times twice the square root in period III of round off programs. Another receiver, the D'_γ receiver also controls reception via the denominator accumulator's γ channel of numerical data which ultimately forms twice the square root. This receiver, however, is used to program the reception of the single unit (+ or −) transmitted first in a given decade place and then in a decade place one further to the right during the square rooting shift sequence of period II and to program the reception of a single unit just once at the beginning of period III for square rooting.

The S_α, N_{AC}, S_{AC}, and N'_γ receivers control events which occur during the shift sequence of period II and at the beginning of period III for either

division or square rooting. The first two receivers stimulate the transmission (with clearing) of the contents of the numerator accumulator to the shift accumulator which receives this data through its α channel. A shifter which shifts numerical data one place to the left is placed at the α input terminal to accomplish the shifting of the numerator. The numerator is then cleared out of the shift accumulator and returned to the numerator accumulator via the numerator accumulator's γ input channel as a result of the setting of the S_{AC} and N'_{γ} receivers.

The circuits which are used solely for external programming are the numerator and denominator accumulator clear circuits and the N_{α}, N_{β}, D_{α}, D_{β}, receivers and answer disposal receivers 1, 2, 3, and 4. Signals from the external programming circuits are delivered to the associated accumulators in exactly the same way as are the signals from the circuits which are both internal and external programming circuits.

The N_{α} and N_{β} receivers correspond respectively to the points α and β on the numerator accumulator receive switches and are used to stimulate the reception of the numerator (or radicand) by the numerator accumulator at the beginning of a program. The D_{α} and D_{β} receivers have a similar function. Whether these receivers actually stimulate reception through the α or β input channels or through some other channels depends, of course, on the manner in which the interconnector plugs of the cables leading from the divider and square rooter to the numerator and denominator accumulators are wired. The plugs, (see Section 6.A) used at present, however, stimulate reception in accordance with the labelling on the numerator accumulator and denominator accumulator receive switches.

The instructions given to the quotient or denominator accumulator as a result of the setting of one of the four answer disposal receivers depend on

the wiring of the interconnector plugs used to deliver the divider and square rooter's programming instructions to the answer accumulators (see Section 6.4).

The answer is built up in the quotient accumulator (in division) or in the denominator accumulator (in square rooting) out of numerical data produced by the numerical circuits of the divider and square rooter. These circuits, which are discussed in greater detail in Section 6.3, include the +1, -1, +2, -2 receivers, gates controlled by the above mentioned receivers which pass the 1, 2, 2', 4, 9, or 1' pulses, the 10 stage place ring, and 10 pairs of digit output gates with each pair controlled by a stage of the place ring.

The answer is formed one unit (in division) or two units (in square rooting) at a time in a particular decade place from the digit pulses passed through the 1, 2, 2', 4, 9, and 1' pulse gates and routed into appropriate decade places by the 10 pairs of gates controlled by the places ring. Sign indication M belonging to any component of the answer is derived from the 9P delivered to the PM lead of the answer output terminal on the divider and square rooter front panel.

6.1. PROGRAM CONTROLS

The divider and square rooter has 8 program controls each consisting of a transceiver with program pulse input and output terminals on the divider and square rooter front panel, an interlock pulse input terminal, a numerator accumulator and a denominator accumulator receive switch, a numerator accumulator and denominator accumulator clear switch, a divide-square root and places switch, a round-off switch, an answer disposal switch, and an interlock switch.

6.1.1. The Numerator Accumulator and Denominator Accumulator Receive Switches.

The numerator accumulator and denominator accumulator receive switches of the divider and square rooter have the same purpose as the multiplier accumulator and multiplicand accumulator receive switches of the high-speed multiplier (see Section 5.1.). These two sets of switches on the divider-square rooter enable the operator to control the stimulation of the reception of the arguments entering into a divider and square rooter program centrally at the divider and square rooter instead of locally at the associated accumulators. The instructions specified by the setting of the receive switches on the divider and square rooter, however, are transmitted statically to the numerator and denominator accumulator via cables leading from the denominator-square root accumulator program terminal and the numerator accumulator interconnector terminal on the divider and square rooter's front panel to interconnector terminals respectively on the numerator accumulator and denominator accumulator. It is to be noted that in the case of the high-speed multiplier, the instructions set-up on the receive switches are transmitted in pulse form from pulse output terminals on front panel 1 of the high-speed multiplier to program pulse input terminals on the ier and icand accumulators. In the case of the high-speed multiplier it is necessary to set-up ier and icand accumulator program controls corresponding to the R_α--R_ε and D_α - D_ε terminals on the high-speed multiplier. In the case of the divider and square rooter it is not necessary to set up program controls on the numerator and denominator accumulators since the receive instructions are delivered directly into the common programming circuits of these accumulators.

The numerator accumulator and denominator accumulator receive switches differ also from the high-speed multiplier's receive switches in that the former

offer the operator only two options as to the accumulator input channel through which reception is to take place. The cables used to connect the numerator accumulator interconnector terminal and the denominator and square root accumulator program terminal to the numerator and denominator accumulator interconnector terminals have been so wired that if either or both of the numerator or denominator accumulator receive switches be set to α or β, the corresponding accumulator receives its argument through the α or β input channel respectively (see Section 6.4.2.).

If it is not desired to stimulate the reception of an argument on any given program or if it is desired to control the reception of either or both arguments for a given program locally at the appropriate accumulator (by delivering a program input pulse to a suitably set up program control on the accumulator either before or simultaneously with the program input pulse that stimulates the divider and square rooter program control), then one or both receive switches can be set to 0 (off).

When the receive switch of a given program control is set to a setting different from 0, the divider and square rooter emits the receive instructions at the same time as the program control's transceiver is set by the program input pulse so that the accumulator correlated with the receive switch receives its argument during the 20 pulse times immediately following the reception of a program input pulse by the divider and square rooter (see Section 6.2).

6.1.2. The Numerator Accumulator and Denominator Accumulator Clear Switches.

The numerator accumulator and denominator accumulator clear switches control the clearing of the numerator and denominator accumulators respectively. These switches have two positions: C (clear) and 0 (off). If a clear switch is set to C, the clear circuits (see Section 6.2.) in the divider and square rooter

emit a clear signal during the last addition time of a program just before the transmission of a program output pulse. This signal is delivered by means of static leads from the divider and square rooter to the PM-Clear Unit of the accumulator corresponding to the receive switch set at C in the addition time at the end of which the divider and square rooter emits a program output pulse.

Since the denominator accumulator is used as the answer accumulator in square rooting programs and since answer disposal takes place in the addition time following the transmission of a program output pulse (see Table 6-10), it is obvious that the answer would be lost before it could be transmitted to another unit if the denominator accumulator clear switch were set at C for square rooting programs. The answer disposal switch together with a suitable adaptor (such as the one shown on PX-4-114A or PX-4-114C-see Section 6.4.2) plugged into the denominator square root accumulator program terminal provide a correct method for clearing the denominator accumulator without loss of the answer in square rooting programs.

6.1.3. The Divide-Square Root and Places Switch.

The divide-square root and places switch provides a means of choosing which of the divider and square rooter's operations is to be performed on a given program and of specifying the number of places in the answer (counting from the PM counter toward the right as seen from the front of the unit) to be found. The five left hand positions of this switch specify division to 4, 7, 8, 9, or 10 places and the five right hand positions, square rooting to 4, 7, 8, 9, or 10 places (see Section 6.4.3.). The number of places chosen by the operator for a given program will depend on the accuracy requirements of the computation and on the alignment of the arguments in the argument accumulators.

See Section 6.4 for a discussion of the relationship between the location of the decimal point in the argument and answer accumulators.

The setting of the divide-square root and places switch like the setting of the significant figures switch of the high-speed multiplier, has no effect on the putting in of the 1'P pulse when the answer is disposed of subtractively from the answer accumulator. Which decade the 1'P is put into in subtractive disposal depends on the setting of the significant figures switch on the answer accumulator. If programs with different round off requirements are performed, it may be necessary to supply the 1'P at the accumulators which receive complements from the answer accumulator.

6.1.4. The Round Off Switch

The round off switch offers the operator a choice between obtaining an answer rounded off (RO) or not rounded off (NRO) to the number of places specified by the setting of the divide-square root and places switch. In general, division or square rooting programs in which 10 or fewer answer places are required will either be performed with round off or else round off will be taken care of in an accumulator after the divider has found more answer places than are required. To obtain answers with 11-19 places (see Sections 6.2 and 6.4), two programs are necessary. The first one, in which the first 10 left hand digits are found, should be performed without round off. The result of the second program should be rounded off whether as part of the second divider program or in an accumulator after the divider program.

It should be noted that under certain circumstances, twice the square root obtained through a round off program may be in error by 2 units in the last place found. For example, the divider and square rooter produces the answer

P0002 when $2\sqrt{0}$ is found to four places in a round off program. The reason for this slight inaccuracy becomes apparent when it is remembered that round off of square roots as carried out by the divider is only approximate. Let R represent the remainder from the radicand and let p + 2x be the number stored in the denominator accumulator at the end of addition time III - 2 where 2x is the extreme right hand digit of the answer found (so that, at this time p is the answer less 2x). Assume that k answer places have been found and, for simplicity, let us say that the decimal point in the numerator and denominator accumulator occurs k places from the left. If k is odd (so that R, the remainder from the radicand before round off, is greater than or equal to zero) the decision to change or not change the answer by 2 units in the last place depends on whether R-5p-10x does not or does show an overdraft. If round off were carried out exactly, the quantity R-5p-10x-2.5 would be examined instead. Thus, the rounded off answer is inaccurate when $R-5p-10x \geq 0$ and when $R-5p-10x-2.5 < 0$. It can easily be seen, then, that the rounded off answer obtained in square rooting programs is correct except when

$0 \leq (5p + 10x) - |R| < 2.5$ for an even number of places

or $0 \leq |R| - (5p + 10x) < 2.5$ for an odd number of places

6.1.5 The Answer Disposal Switch.

The answer disposal switch on the divider and square rooter is comparable to the product disposal switch on the high-speed multiplier in that the former enables the operator to provide for the stimulation of the disposal of the answer from the answer accumulator without the necessity of delivering a program input pulse to the answer accumulator specifically for this purpose. The answer disposal switch on the divider and square rooter, however, offers the

operator only 4 optional methods of disposal in contrast with the 6 options of the product disposal switch on the high-speed multiplier.

The answer disposal signals emitted by the divider and square rooter, moreover, are static signals which are delivered to the quotient and/or denominator accumulator by means of cables connecting the quotient accumulator and shift accumulator program terminal and/or the denominator-square root program terminal to interconnector terminals on the quotient and/or denominator accumulator. Points 1 and 2 of the answer disposal switch refer to the disposal of the quotient and points 3 and 4 to the disposal of twice the root. The exact meaning conveyed by their settings, however, depends on the wiring of the adaptors and interconnector cables used to carry instructions from the program terminals on the divider and square rooter to interconnector terminals on the associated accumulators (see Section 6.4.2) since the instruction signals are brought directly into the accumulators' common programming circuits. In the high-speed multiplier, on the other hand, the instructions specified by the settings A, S, AS, AC, SC or ASC of the product disposal switch, depend on the set-up of the product accumulator program controls which receive product disposal pulses from the A, S, AS, AC, SC, or ASC pulse output terminals on panel 3 of the high-speed multiplier.

6.1.6. The Interlock Switch.

The setting of the interlock switch determines the conditions for the occurrence of the final addition time of a divider and square rooter program (i.e. the addition time when a program output pulse, answer disposal signal, signal for clearing the argument accumulator's and signals for clearing certain circuits within the divider and square rooter are emitted). If the interlock

switch is set at no interlock (NI), the final addition time occurs during the second addition time following the completion of the actual numerical operations involved in a division of square rooting (i.e. during the second addition time of period IV). If the interlock switch is set at I (interlock), not only must period III be completed, but also the divider and square rooter must have received an interlock input pulse before the divider and square rooter program can be considered completed. In the interlock case, the final addition time takes place during the second addition time following whichever of the 2 events hereinafter listed occurs later in the cycle of operations: 1) completion of period III; 2) the reception by the divider and square rooter of an interlock input pulse (see Table 6-10).

The interlock feature of the divider and square rooter is desirable when a division or square rooting program occurs simultaneously with another sequence of programs and is to be followed by a second sequence using either the same units as are used by the sequence in parallel with the division or square rooting or using results obtained from the parallel sequence and results of the division and square rooting.. By using the final program output pulse of the sequence in parallel with the division or square rooting as an interlock input pulse and then using the divider and square rooter's program output pulse as the initial program input pulse for the sequence which is to follow the division, the operator insures the completion of all of the programs of the parallel sequence before the commencement of the second sequence.

Had the interlock feature been omitted from the design of the divider and square rooter, the operator, under the same circumstances as those described in the previous paragraph, would have faced two equally disagreeable alternatives:

1) never to schedule a parallel sequence lasting between the minimum time to maximum time for completing a division or square rooting
2) to compute the maximum number of addition times required to complete the division or square rooting program and then to use the final program output pulse of the sequence in parallel with the division or square rooting to produce eventually (after a delay consistent with the maximum division or square rooting time) an initial program input pulse for the second sequence.

6.2. COMMON PROGRAMMING CIRCUITS

6.2.1. Status of the circuits before a transceiver is stimulated.

Before a program input pulse is received by a transceiver to stimulate a given program control, but immediately after initial clearing or the completion of a previous program, the status of certain important components of the divider and square rooter's common programming circuits may be summarized as follows:

In the program ring circuit, the pulse source flip-flop and the program ring flip-flop are in the so called normal state. The program ring (whose stages are designated by A, B, 1, 2, ..., 7) is in stage A. The observer viewing the divider and square rooter from the front (see PX-10-302) observes that the pulse source and program ring flip-flop neons are lit as is program ring neon A.

The numerator ring of the overdraft circuit is in stage P (the corresponding neon is lit) and the denominator flip-flop of the sign indication circuit is in the normal state (with the denominator flip-flop neon lit). If the previously completed program was a square rooting program, the divide flip-

flop is in the normal state and the divide flip-flop neon is off. Otherwise this flip-flop is in the abnormal state and its corresponding neon is on. The interlock, interlock coincidence, and clear flip-flops are in the normal state (and their corresponding neons are off). The receivers of the internal and external-internal programming circuits are all in the normal state and the neons corresponding to them are off.

In the numerical circuits, the place ring is in stage 1 (and the place ring neon numbered 9 on PX-10-302 is on). The +2, -2, +1, and -1 receivers are in the normal state (and their corresponding neons are off).

6.2.2. The Program Ring Circuit.

As soon as a program control of the divider and square rooter is stimulated, period I is initiated. The characteristics of period I as evidenced in the divider and square rooter's program ring circuit are given in the following paragraphs.

The pulse source flip-flop remains in the normal state so that a 1'P is gated through F6 to produce a $1'P_1$ and a CPP is gated through F4 to produce a CP pulse every addition time. If the program control's divide-square root and places switch is set at a divide setting and the round-off switch at round-off or no round-off, then GP is gated through K6 or L6 respectively to produce a divide pulse (DP); if the divide-square root and places switch is set at a square root setting and the round off switch at RO or NRO, GP is gated through K3 or L3 respectively to produce a square root pulse (SRP).

During period I, also, the program ring flip-flop remains in the normal state so that DP or SRP is gated through A10 or A11 respectively to cycle the program ring 1 stage per addition time.

In the third addition time of period I, the program ring is in stage 1. A signal from this stage gates a GP through gates A7 and through B7 clearing the program ring back to stage A and flipping the program ring into the abnormal state at the end of addition time 3. This marks the termination of period I for division; period I for square rooting lasts one addition time longer. (See Table 6-4 and Table 6-7).

During period II the pulse source flip-flop remains in the normal state so that GP, $1'P_1$ and either DP or SRP continue to be emitted at the end of every addition time. Since the program ring flip-flop is in the abnormal state (and gates A10 and A11 are closed) neither DP nor SRP can cycle the program ring. The program ring, therefore, continues to register stage A throughout this period.

Period II is terminated and period III initiated when an S pulse (this is a pulse produced by the divider and square rooter when a shift sequence is about to begin - see below) is gated through E6 as a result of the coincidence of a signal from the stage of the place ring corresponding to the places setting of the divide-square root and places switch and a signal from this same switch. The pulse produced in this way is designated on PX-10-304 by the symbol SS. The SS pulse flips the pulse source flip-flop into the abnormal state.

During period III, then, $1'P_1$ and GP (and therefore either DP or SRP) cease to be emitted. Instead, a CPP is gated through F5 at the end of every addition time to produce a pulse designated by III P. III P cycles the program ring 1 stage per addition time during period III. Also, if the round-off switch has been set at RO, III P is gated through K4 or K5 (when the divider-square root and places switch is set respectively at a square-rooting or division point)

to produce a round off pulse (ROP) at the end of every addition time in period III. Notice that ROP is emitted only if round off is to take place.

Period III is terminated when the program ring has been cycled through its 9 stages. Period IV is initiated when a CPP is gated through L50 to produce an F pulse and through E3 to produce an F' pulse. The F' pulse resets the pulse source flip-flop into the normal state so that in period IV (as in periods I and II) $1'P_1$, GP and SRP or DP are emitted.

6.2.3. The Interlock and Clear Circuit.

The F pulse sets the interlock coincidence flip-flop. Then the next CPP gated through J49 if the interlock switch is set at I and the interlock flip-flop* has been set as a result of the reception of an interlock input pulse is gated through H50 (controlled by the interlock coincidence flip-flop). The signal gated through H50 resets the interlock coincidence flip-flop and sets the clear flip-flop. The setting of the clear flip-flop results in the emission of a reset signal for the transceiver and the emission of the CL and CL' pulses.** The CL and CL' pulses are responsible for the condition of the program ring circuit, the place ring, the numerator ring, and the denominator flip-flop prior to the commencement of a divider and square rooter program (see Section 6.2.1).

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* It is to be noted that the interlock flip-flop is insensitive to which of the 8 interlock input terminals has been pulsed. An interlock input pulse received at any of the interlock input terminals sets this flip-flop regardless of which program control on the divider and square rooter has been stimulated. This flip-flop is also insensitive, in some respects, to the time of reception of the interlock input pulse. An interlock input pulse received any time after the completion of one divider and square rooter program (and this may even be before the stimulation of the next divider and square rooter program) serves to flip the interlock flip-flop for the next divider and square rooter program.

** The only distinction between CL and CL' is that CL' is taken off before buffer E48 and CL after the buffer.

6.2.4. The Overdraft and Sign Indication Circuits.

The overdraft and sign indication circuits receive the information upon which they operate (in the case of the overdraft circuit, the sign of the contents of the numerator accumulator and in the case of the sign indication circuit, the sign of the denominator) by means of static leads from the numerator and denominator accumulators' PM counters. The N^- and N^+ lines carry sign signals if the contents of the numerator accumulator are respectively negative or positive. The D^- line delivers a signal to gate B1 of the sign indication circuits only if the denominator is negative.

The overdraft circuit consists of a numerator (binary) ring whose stages represent sign P and sign M and 4 gates (F1, F2, G1, G2). Each of the 4 gates receives one input from the numerator ring and the other from either the N^+ or N^- line. The gates F1, F2, G1, G2 may be thought of as (M, N^-), (M, N^+), (P, N^-), and (P, N^+) gates where the first symbol in a parenthesis designates the stage of the numerator ring and the second the numerator sign line to which the gate is connected.

The numerator ring clears to stage P at the end of a program and, in the midst of a program, can be cycled only during period I or at specific times in periods II and III. In period I, when the program ring is in stage B, a GP is gated through D6, the resulting signal is gated through K1 to cycle the numerator ring from stage P to M only if the numerator is negative. During period II and III, the numerator ring can be cycled only when L1 opens to pass a CPP. Gate L1, however, is open only when the S_α receiver is set and this receiver is set only after an overdraft has occured.

Thus, the 4 gates receive information about the current sign indica-

tion of the contents of the numerator accumulator over the static leads from the numerator accumulator's PM circuit. The numerator ring, on the other hand, registers the sign of the contents of the numerator accumulator before the denominator is either subtracted from or added to the contents of the numerator accumulator. The 4 gates in the overdraft circuit compare the current with the past sign of the contents of the numerator accumulator. The coincidence of signals to gate F1 (M, N^-) or G2 (P, N^+) leads to the emission of an NO signal. Similarly gate F2 or G1 emits an O signal upon the coincidence of signals on both inputs.

As long as an NO signal is emitted the basic operation sequence of period II is performed. When an O signal is emitted, the basic operation sequence is interrupted either by a shift sequence or by the initiation of period III. The O and NO signals produce these results by inhibitory actions since no inverters intervene between the gates of the overdraft circuit and the gates to which O and NO are delivered. When NO is emitted, gate D12 is closed and gate D11 passes a signal which gates a GP through D9. The resulting pulse is designated by P.* The P pulse, in period II, initiates the basic operation sequence; and in period III, initiates the 5 subtractions or additions of the denominator to the contents of the numerator accumulator by setting the Ny receiver and either the D_S or D_A receiver. In period III, moreover, when NO is

*The P pulse is produced in other ways when the sensing of overdraft is irrelevant or unnecessary. At the end of period I in division, a signal from stage 1 of the program ring gates DP through B8 to produce a P pulse. Also, after shifting of the numerator accumulator's contents in period II, a signal from the N'y receiver gates a GP through C9 to produce a P pulse. In period III, the P pulse is produced when a signal from stage B of the program ring gates an ROP through C8.

emitted, gate K12 passes a signal (emitted when a signal from stage 6 of the program ring opens gate J13 so that an ROP can pass) which motivates the correction of the answer in accordance with the state of the divide flip-flop (see Section 6.2.4). When the 0 signal is emitted, gates D11 and K12 are closed and gate D12 passes a signal from the D_γ or Q_α receiver which, in turn, gates a CP through E9 to produce an S pulse. The S pulse motivates the shift sequence of period II or, when gated through E6 to produce an SS pulse (see Section 6.2.2) initiates period III.

The sign indication circuit is quite similar to the overdraft circuit in its components and functioning. This circuit consists of 4 gates (D1, D2, E1, E2) and a flip-flop, the denominator flip-flop. Each gate is connected to one of the 2 output leads from the denominator flip-flop and to either the P or M stage of the numerator ring. The denominator flip-flop is in the normal state when a program commences and can be flipped into the abnormal state to remember the fact that the denominator is negative at only one specific time* in the course of a divider and square rooter program. This one specific time is addition time 2 of period I when gate D6, held open by a signal from stage B of the program ring, passes a GP which can then pass through gate B1 to flip the denominator flip-flop if the contents of the denominator accumulator are negative. Once flipped, the denominator flip-flop remains in the abnormal state until reset by CL in period IV.

If the denominator is positive (and therefore the denominator flip-flop is in the normal state) and the contents of the numerator accumulator

*It is for this reason that the divider and square rooter is unable to find the real coefficient of i when the radicand is negative.

before a subtraction or addition of the denominator are positive or negative. (so that the numerator ring registers P or M respectively), then gates E1 or E2 respectively emits a like sign or unlike signal. Similarly, gates D2 and D1 emit a like or unlike sign signal respectively,

The like and unlike sign signals are also delivered to gates without the intervention of inverters so that these signals, like the O and NO signals, produce their effects by an inhibitory action.

The like sign signal closes gate B11 so that gate B10 passes a P pulse (see Section 6.2.4) which sets the D_S receiver. The unlike sign signal closes gate B10 so that gate B11 passes a P pulse which sets the D_A receiver. The coincidence of like or unlike sign signal and a signal from the round-off flip-flop also determines which receivers of the internal - external programming circuits and of the numerical circuits are set in period III (see Section 6.2.7).

6.2.5. The External - Internal Programming Circuits.

A program input pulse delivered to a program pulse input terminal of the divider and square rooter immediately passes through the numerator and denominator accumulator switches whence it sets the N_α or N_β and D_α or D_β receivers. Thus, during addition time 1 of period I, the numerator and denominator accumulators receive their arguments if this reception is controlled by the divider and square rooter.* At the end of addition time 1, a CPP resets these receivers and they do not function again in any subsequent period of the program.

The N_γ and D_A or D_S receivers function during period II and, if round-off is specified, during period III. The P pulse (see Section 6.2.4) sets the N_γ receiver at the same time that it sets the D_A or D_S receiver (depending on

* The arguments may of course, be received prior to this if their reception is controlled locally at the accumulators.

whether the unlike or like sign signal is being emitted. During period II, GP resets these receivers one addition time after they have been set. In period III of round off programs, the N_γ and D_A or D_S receivers remain set throughout addition times 3, 4, 5, 6, and 7. At the end of addition time 7 an ROP gated through D4 by a signal from stage 5 of the program ring resets these receivers. Thus, the denominator is subtracted from or added to the contents of the numerator accumulator 5 times in round off programs.

During period II, when DP or SRP is being emitted, the setting of the N_γ receiver leads, one addition time later, to the setting of the Q_α (if DP) receiver or the D_γ (if SRP) receiver. Simultaneous with the setting of the Q_α receiver, DP sets the +1 receiver if the D_S receiver was previously set or the -1 receiver if the D_A receiver was previously set. Similarly, in square rooting programs, the +2,or -2 receiver is set at the same time as the D_γ receiver is.

During period III of round off programs, the setting of the D_γ or Q_α receiver does not result from the setting of the N_γ receiver, but, instead, takes place if a ROP is gated through K12 because NO is emitted. The ROP is then routed to set either the D_γ or Q_α receiver by means of gates controlled by the round off flip-flop. This same ROP and other gates controlled by the round-off flip-flop effects the setting of the +2 or -1 receiver (if the D_S receiver was set during addition times 3-7) or the -2 or -1 receiver (if the D_A receiver was previously set).

During period II, the emission of an O signal leads to the emission of an S pulse (see Section 6.2.4). The S pulse sets the S_α and N_{AC} receivers. A CPP gated through K7 as a result of the setting of the S_α receiver causes the setting of the S_{AC} and N'_γ receivers. Thus, in either division or square rooting,

the shifting of the contents of the numerator accumulator one place to the left is provided for.

The S pulse also sets the D'_γ receiver and, gated through G9 or H9 by a signal from the +2 or -2 receiver respectively, sets the -1 or +1 receiver. The D'_γ receiver and the +1 or -1 receiver remain set for 2 addition times in period II for square rooting. They are reset when a CPP is gated through C13 after the NO state of affairs is restored in the overdraft circuit. Since the D'_γ and +1 or -1 receivers remain set for 2 addition times and, since the place ring is not cycled until the second addition time (see Section 6.3), the correction of twice the root as described in Section 6.0 (a change of one unit first in one decade place and then in a decade place one further to the right) takes place. It is to be noted that in period II for division, the D'_γ receiver is set but that there is nothing for the denominator accumulator to receive at the time since neither the +1 nor the -1 receiver is set in division. DP resets the D'_γ receiver in the division case one add.time after its setting.

At the beginning of period III, also, the S pulse sets the S_α and N_{AC} receivers and one addition time later the S_{AC} and N'_γ receivers are set. In period III, the D'_γ receiver is set and either the +1 or the -1 receiver is also set in the case of a square rooting program. It is to be noted, however, that III P resets the D'_γ receiver and the +1 or -1 receiver one addition time after their setting in period III so that twice the square root is corrected by only one unit in the last answer place.

When the clear flip-flop is set (see Section 6.2.3), Gate 62 in the transceiver emits a signal which has 3 effects: 1) passing through the answer disposal switch, it sets the answer disposal receiver (1, 2, 3, 4) specified

by the setting of this switch; 2) passing through the numerator and denominator accumulator clear switches, it allows the carry clear gate to pass through gate A49 (if only the denominator accumulator is to be cleared), through gates A48 and B49 (if both the numerator and denominator accumulators are to be cleared), or through gate B48 (if only the numerator accumulator is to be cleared); 3) it gates a CPP through 68 to provide the transceiver's reset signal and a program output pulse.

Thus clearing of the numerator and/or denominator accumulators takes place a little prior to the emission of a program output pulse and answer disposal signal.

6.2.6. The Divide Flip-Flop.

The divide flip-flop is set or reset during period I of divider and square rooter programs. In division programs DP flips this flip-flop into the abnormal state (and turns on the corresponding neon); in square rooting programs, SRP resets this flip-flop if it was previously flipped into the abnormal state in a division program.

The effects of this flip-flop on the divider and square rooter's common programming circuits become apparent in addition time 8 of period III for round off programs when an ROP is gated through J13 by a signal from stage 6 of the program ring. If the signal from gate J13 is gated through K12 as a result of the emission of the NO signal, then, in the division case, this signal is gated through J10 to set the Q_a receiver and through gate J8. The signal from gate J8 is gated through G8 to set the +1 receiver or through gate H8 to set the -1 receiver when the like or unlike sign signal respectively is emitted. Similarly, in the square rooting case, the D_y receiver is set by a signal gated

TABLE 6-4

DIVISION - INITIAL SEQUENCE - PERIOD I

Requires three addition times: 1-3

Add. Time (and Prog. Ring stage)	Signal	Effect	Comment
0 (H)	1) Program input pulse	1) a) Sets transceiver in the divider b) Sets N_α or N_β and/or D_α or D_β receivers	1) a) b) The numerator and/or denominator are then received by the numerator and/or denominator accumulator respectively in add. time 1.
1 (A)	1) CPP	1) Gated through F4* by a signal from the pulse source flip-flop (in the normal state) produces a GP pulse.	1) This effect occurs in every subsequent add. time of a division program except during period III.
	2) GP	2) Gated through K6 or L6 produces a DP pulse.	2) This effect occurs in every subsequent add. time of a division program except during period III.
	3) DP	3) a) Gated through A10 by a signal from the program ring flip-flop, cycles the program ring to stage B. b) Sets the divide flip-flop if this flip-flop is in the normal state.	3) a) b) This turns on the divide flip-flop neon.
2 (B)	1) GP gated through D6 by a signal from stage B of the program ring.	1) Is then gated through gate K1 by the N^- signal so that the numerator binary ring is cycled to stage N in the event that the numerator is negative.	
	2) D^- signal	2) Is gated through D1 by the output of gate 6. Output of gate P1 sets the denominator flip-flop in the event that the denominator is negative	2) This turns off the denominator flip-flop neon.
	3) DP	3) Cycles the program ring to stage 1	
3 (1)	1) DP	1) a) Gated through B6 by a signal from stage 1 of the program ring produces a P pulse	
	2) P	2) a) Sets the N_γ receiver b) Gated through B10 when the like sign signal closes B11 sets the D_S receiver or gated through B11 when the unlike sign closes B10 sets the D_A receiver.	2) a and b) Then during add. time 4, the numerator accumulator receives either the complement of the denominator or the denominator. At the end of add. time 4, GP resets these receivers. The setting of these receivers is the event described (in the table for period II) as occurring in add. time d=3+2n for n=o.
	3) GP	3) a) Gated through A7 by a signal from stage 1, clears the program ring to stage A. b) Gated through B7 flips the program ring flip-flop.	3) a) b) The program ring flip-flop neon is turned off at this time.

* ☐ refers to "gate".

TABLE 6-5

DIVISION PERIOD II - BASIC DIVISION SEQUENCE

Requires two add. times: d+1 and d+2

Add. Time (and Prog. Ring Stage)	Signal	Effect	Comment
	For n=o, this add. time is counted as part of period I For n>o, this add. time coincides with add. time s+2 of period II or add. time d+2 of period I		
d =3+2n for n=o For n≥o see period I (A)	1) P pulse derived from GP gated through D9 as a result of the coincidence of the NO signal and a signal from the Q_α receiver, or GP gated through C9 by a signal from the N'_γ receiver, or (see period I) DP gated through E8 by a signal from stage 1 of the program ring.	1) a) Sets the N_γ receiver. b) Gated through B10 when the like sign signal closes B11. P sets the D_S receiver or gated through B11 when the unlike sign signal closes B10. P sets the D_A receiver.	1) During add. time d+1, then, the numerator accumulator receives either the complement of the denominator (when the numerator and denominator have the same signs) or the denominator (when the numerator and denominator have unlike signs). While these receivers are set, the corresponding neons are on. At the end of add. time d+1, these receivers are reset by a GP.
d+1 (A)	1) DP	1) a) Gated through L10 by a signal from the N_γ receiver, sets the Q_α receiver. b) Gated through G11 by a signal from the D_S receiver, sets the +1 receiver or, gated through H11 by a signal from the D_A receiver, sets the -1 receiver.	1) During add. time d+2, then, the quotient accumulator receives 1 in a given decade place if the denominator was subtracted from the numerator or receives the complement of 1 if the denominator was previously added to the numerator. The neons corresponding to these receivers are on as long as the receivers are set. The Q_α receiver is reset by a CPP and the +1 or -1 receiver is reset by a DP at the end of add. time d+2.

SHIFT SEQUENCE

Requires two add. times: s+1, s+2

Add. Time (and Prog. Ring Stage)	Signal	Effect	Comment
	This add. time coincides with add. time d+2 above		
s =3+2n for n≥o (A)	1) S pulse produced when a GP is gated through E9 as a result of the coincidence of an O signal and a signal from the Q_α receiver.	a) Sets the S_α and N_{AC} receivers. b) Sets the D'_γ receiver. c) If gated through E6 as a result of the coincidence of signals from the places switch and place ring, produces an SS pulse (see Table 6-6).	a) During add. time s+1, the numerator is transmitted (with clearing) from the numerator accumulator and received in the shift accumulator. At the end of add. time s+1, a CPP resets the S_α receiver and N_{AC} receiver. b) There is no numerical effect on the division from the setting of the D'_γ receiver since there is no data for the denominator accumulator to receive during add. time s+1. This receiver is reset at the end of add. time s+1 by a DP. c) SS pulse terminates period II and initiates period III.
s+1 (A)	1) Signal from the S_α receiver.	1) a) Gates $1'P_1$ through L45 to produce $1'P_2$ which cycles the place ring 1 stage. b) Gates a CPP through L1 so that the numerator binary ring is cycled 1 stage. c) Gates a CPP through K7 so that the N'_γ and S_{AC} receivers are set.	1) a) b) As a result O ceases to be emitted and NO is emitted instead. c) Then the shift accumulator transmits (and clears) its contents to the numerator accumulator during add. time s+2. At the end of add. time s+2, a CPP resets the N'_γ and S_{AC} receivers.

TABLE 6-6

DIVISION PERIOD III – ROUND OFF OR NO ROUND OFF

Items relevant only to the round-off case are circled
Requires 9 add. times: 1-9

Add. Time	Signal	Effect	Comment
	This add. time coincides with add. time d+2 of period II		
0 (A)	1) S pulse produced when a GP is gated through B9 as a result of the coincidence of an O signal and a signal from the Q_α receiver.	1) a) Sets the S_α and $H_{\Delta C}$ receivers. b) Sets the D'_γ receiver. c) Gated through B6 as a result of the coincidence of signals from the places switch and place ring, produces an SS pulse.	1) a) During add. time 1, then, the numerator accumulator transmits (and clears) its contents to the shift accumulator. A CPP resets these receivers in add. time 1. b) Since during add. time 1, there is no numerical data on the tray from which the D_γ channel receives, there is no numerical result from 1 b).
	2) SS pulse	2) Sets the pulse source flip-flop.	2) At this time, the pulse source flip-flop neon is turned off.
1 (A)	1) CPP	1) a) Gated through L1 by a signal from the S_α receiver, cycles the numerator binary ring. b) Gated through K7 by a signal from the S_α receiver, sets the $S_{\Delta C}$ and H'_γ receivers. c) Gated by P6 produces a III P pulse.	1) a) So that NO ceases to be emitted and O is emitted by the sign indicating circuit. b) So that, during add. time 2, the numerator accumulator receives the number transmitted (with clearing) from the shift accumulator. At the end of add. time 2, these receivers are reset by a CPP. c) This pulse is produced in every subsequent add. time of period III.
	2) III P	2) a) Gated by K5 produces ROP. b) Cycles the program ring to stage B c) Resets the D'_γ receiver.	2) a) ROP is produced in every subsequent add. time of period III if round off is specified.
2 (B)	1) III P 2) ROP 3) P	1) Cycles program ring to stage 1 2) Gated through C3 by a signal from stage B of the program ring produces a P pulse. 3) Sets H_γ and D_Δ or D_δ receiver depending on whether unlike sign or like sign signal is emitted.	1) 2) 3) These receivers remain set during add. times 3,4,5,6, and 7. (see below) They are reset at the end of add. time 7. Therefore, the numerator accumulator receives either the denominator or its complement five times.
3 (1)	1) III P	1) Cycles program ring to stage 2	
4 (2)	1) III P	1) Cycles program ring to stage 3	
5 (3)	1) III P	1) Cycles program ring to stage 4	
6 (4)	1) III P	1) Cycles program ring to stage 5	
7 (5)	1) ROP 2) III P	1) Gated through D4 by a signal from stage 5 of the program ring, resets the H_γ and D_Δ or D_δ receivers. 2) Cycles the program ring to stage 6.	
8	1) ROP 2) III P	1) Gated through J13 by a signal from stage 6 of the program ring produces a signal which, if gated through K12 by NO, passes through J10 to set the Q_α receiver and through J8. The signal from J8 passes through G8 when the like sign signal is emitted and sets the +1 receiver or passes through H8 to set the -1 receiver when the unlike sign signal is emitted. 2) Cycles the program ring to stage 7.	1) Thus, if the subtraction or addition of 5 times the denominator which takes place during add. times 3 through 7 does not produce an overdraft, during add. time 9 the quotient is increased (when numerator and denominator have like signs) or decreased (when numerator and denominator have unlike signs) by 1 unit in the last place at the right as specified by the setting of the places switch. At the end of add. time 9, III P resets and the +1 or -1 receiver and a CPP resets the Q_α receiver.

TABLE 6-7

SQUARE ROOT PERIOD I

Requires four add. times: 1-4

Add. Time (and Prog. Ring Stage)	Signal	Effect	Comment
0 (A)	1) Program input pulse	1) a) Sets transceiver in the divider and square rooter. b) Sets N_α or $N\beta$ receiver	1) b) The numerator is then received by the numerator accumulator during add. time 1.
1 (B)	1) CPP	1) Gated through F4 by a signal from the pulse source flip-flop, produces a GP pulse.	1) This effect occurs in every subsequent add. time of a square root program except during period III.
	2) GP	2) Gated through L3 or K3 produces a SRP	2) This effect occurs in every subsequent add. time of a square root program except during period III.
	3) SRP	3) a) Gated through A11 by a signal from the program ring flip-flop, cycles the program ring to stage B. b) Resets the divide flip-flop if this flip-flop is in the abnormal state.	3) b) This turns off the divide flip-flop neon.
2 (1)	1) GP gated through D6 by a signal from stage B of the program ring.	1) Gated through K1 by the N^- signal cycles the numerator ring to stage 11 if the radicand is negative.	1) The divider and square rooter, however, does not find the real coefficient of i correctly if the radicand is negative.
	2) SRP	2) Cycles the program ring to stage 1.	
3 (A)	1) SRP	1) a) Gated through K6 by a signal from stage 1 of the program ring, sets the D_γ receiver. b) Gated through G7 by a signal from stage 1 of the program ring, sets the +1 receiver.	1) a and b) Thus, during add. time 4, the denominator (twice the root) accumulator receives 1 pulse in the 10^0 decade. At the end of add. time 6, a CPP resets the D_γ receiver and a CPP gated through as a result of the coincidence of the NO signal and a signal from the D_γ receiver, resets the +1 receiver.
	2) GP	2) a) Gated through A7 by a signal from stage 1, clears the program ring to stage A. b) Gated through B7 by a signal from stage 1 flips the program ring flip-flop.	2) b) The program ring flip-flop neon is turned off at this time.

TABLE 6-8

SQUARE ROOT PERIOD II - BASIC SQUARE ROOT SEQUENCE

Requires two add. times; r+1, r+2

Add. Time	Signal	Effect	Comment
	For n=o, this add. time coincides with add. time 4 of period I. For n>o, this add. time coincides with add. time s+2 or r+2 of period II.		
r (4+2n for n ≥ 0) (A)	1) P pulse derived from GP gated through D9 as the result of the coincidence of a signal from the D_Y receiver and an NO signal or GP gated through C9 by a signal from the H'_Y receiver (after a shift sequence).	1) a) Sets the N_Y receiver. b) Gated through B10 when the like sign signal is emitted, sets the D_S receiver or gated through B11 when the unlike sign signal is emitted, sets the D_A receiver.	1) a and b) Thus, during add. time r+1, the numerator accumulator receives the complement of the denominator (when N and D have like signs) or receives the denominator (when N and D have unlike signs). These receivers are reset by GP at the end of add. time r+1.
r+1 (A)	1) SRP	1) a) Gated through L9 by a signal from the N_Y receiver sets the D_Y receiver. b) Gated through G12 or H12 respectively by a signal from the D_S or D_A receiver sets the +2 or -2 receiver.	1) a and b) Thus, in add. time r+2, the denominator accumulator receives two in a given decade place of the complement of 2 if the denominator was previously subtracted or added respectively. The D_Y receiver and the +2 and -2 receivers are reset by a CPP at the end of add. time r+2.

SQUARE ROOT - SHIFT SEQUENCE

Requires two addition times: s+1, s+2

Add. Time	Signal	Effect	Comment
		This add. time coincides with add. time r+2	
s (=4+2n for n ≥ 1) (A)	1) S pulse produced when a GP is gated through E9 as a result of the coincidence of an O signal and a signal from the D_Y receiver.	1) a) Sets the S_a and H_{AC} receivers. b) Sets the D'_Y receiver. c) Gated through G9 by a signal from the +2 receiver, sets the -1 receiver or gated through E9 by a signal from the -2 receiver, sets the +1 receiver. d) If gated through E6 as a result of the coincidence of signals from the places switch and places ring produces an SS pulse (see Table 6-9).	1) a) As a result, the shift accumulator receives the numerator from the numerator accumulator which transmits and clears during add. time s-1. At the end of add. time s+1, a CPP resets these receivers. b and c) During add. time s+1, then, the denominator accumulator receives the complement of 1 or receives 1 in a given decade place if during the previous sequence, the denominator accumulator received +2 or -2 respectively in the same decade place. The D'_Y receiver and the +1 or -1 receiver remain set through add. time s+2. d) SS pulse initiates period III. (See chart for period III.
s+1 (A)	1) Signal from the S_a receiver.	1) a) Gates $1'P_1$ through L45 to produce $1'P_2$ which cycles the place ring one stage. b) Gates a CPP through L1 so that the numerator binary ring is cycled 1 stage. c) Gates a CPP through E7 so that the H'_Y and S_{AC} receivers are set.	1) b) As a result O ceases to be emitted and NO is emitted instead. c) During add. time s+2, then, the numerator accumulator receives the contents of the shift accumulator which transmits and clears. At the end of add. time s+2, a CPP resets the H'_Y and S_{AC} receivers.
	2) See 1 c) of addition time s.	2) The D'_Y and +1 or -1 receiver remains set.	2) Therefore, during add. time s+2, the denominator accumulator receives +1 or the complement of 1 but this time one decade place further to the right than during add. time s+1. At the end of add. time s+2, GP gated through C11 by a signal from the H'_Y receiver resets the D'_Y receiver and the +1 or -1 receiver.

TABLE 6-9

SQUARE ROOT PERIOD III - ROUND OFF OR NO ROUND OFF PERIOD

Requires nine add. times; 1-9

Items relevant to the round off case only are circled

Add. Time	Signal	Effect	Comment
	This add. time coincides with add. time r+2 of period II.		
0 (A)	1) S pulse produced when a GP is gated through E9 as a result of the coincidence of an 0 signal and a signal from the Q_α receiver.	1) a) Sets the S_α and N_{AC} receivers.	1) a) During add. time 1, then, the numerator accumulator transmits (and clears) its contents to the shift accumulator. A CPP resets these accumulators in add. time 1.
		b) Sets the D'_Y receiver.	b and c) Thus, during add. time 1, the denominator accumulator receives the complement of -1 or +1 in a given decade place if in the previous square root sequence, +2 or its complement respectively was received in that decade place. At the end of add. time 1, III P (see below) resets the D'_Y and +1 or -1 receivers.
		c) Gated through G9 by a signal from the +2 receiver, sets the -1 receiver or gated through H9 by a signal from the -2 receiver sets the +1 receiver.	
		d) Gated through E6 as a result of the coincidence of signals from the places switch and place ring produces an SS pulse.	
	2) SS	2) Sets the pulse source flip-flop.	2) At this time, the pulse source flip-flop neon is turned off.
1 (A)	1) CPP	1) a) Gated through L1 by a signal from the S_α receiver cycles the numerator binary ring.	1) a) So that NO ceases to be emitted and 0 is emitted instead.
		b) Gated through K7 by a signal from the S_α receiver, sets the S_{AC} and D'_Y receivers.	b) So that during add. time 2, the numerator accumulator receives the numerator from the shift accumulator which transmits and clears. At the end of add. time 2, a CPP resets these receivers.
		c) Gated by F5 produces a III P.	c) This pulse is produced in every subsequent add. time of period III.
	2) III P	2) a) Gated by K4 produces an ROP pulse.	2) a) ROP is produced in every subsequent add. time of period III if round off is specified.
		b) Cycles the program ring to stage B.	
		c) Resets the D'_Y receiver and the +1 or -1 receiver.	
2 (B)	1) III P	1) Cycles program ring to stage 1	1)
	2) ROP	2) Gated through C8 by a signal from stage B of the program ring produces a P pulse.	2)
	3) P	3) Sets N_Y receiver and D_A or D_S receiver if the unlike or like sign signal respectively is emitted.	3) These receivers remain set during add. times 3.4.5.6.7. They are reset at the end of add. time 7 (see below). Therefore, the numerator accumulator receives either the denominator or its complement five times.
3 (1)	1) III P	1) Cycles program ring to stage 2.	
4 (2)	1) III P	1) Cycles program ring to stage 3.	
5 (3)	1) III P	1) Cycles program ring to stage 4.	
6 (4)	1) III P	1) Cycles program ring to stage 5.	
7 (5)	1) ROP	1) Gated through D4 by a signal from stage 5 of this program ring resets the N_Y and D_A or D_S receivers.	
	2) III P	2) Cycles the program ring to stage 6.	
8 (6)	1) ROP	1) Gated through J13 by a signal from stage 6 of the program ring produces a signal which if gated through K12 by NO, passes through J9 to set the D_Y receiver and passes through J12. The signal from J12 passes through E13 when the like sign is emitted and sets the +2 receiver or passes through F13 when the unlike sign signal is emitted and sets the -2 receiver.	1) Thus, if the subtraction or addition of 5 times the denominator which occurs during add. times 3 through 7 does not produce an overdraft, during add. time 9, the quotient is increased (when N and D have like signs) or decreased (when N and D have unlike signs) by 2 units in the last place at the right as specified by the setting of the places switch. At the end of add. time 9, III P resets the +1 or -1 receiver and a CPP resets the D_Y receiver.

TABLE 6-10

PERIOD IV FOR EITHER DIVISION OR SQUARE ROOT - INTERLOCK OR NO INTERLOCK PERIOD

Requires 2 add. times: 1, 2.
Items relevant to the interlock case only are circled.

Add. Time	Signal	Effect	Comment
		This add. time coincides with add. time 9 or period III	
0 (7)	1) CPP	1) a) Gated through L60 by a signal from stage 7 or the program ring, produces an F pulse. b) Gated through E3 by a signal from stage 7 or the program ring produces an F pulse.	1)
	2) F	2) Sets the interlock coincidence flip-flop.	2) This turns on the interlock coincidence flip-flop neon.
	3) F'	3) Resets the pulse source flip-flop.	3) So that the pulse source flip-flop neon is turned on again.
1 (7)	1) CPP	1) Gated through F4 produces a GP.	These three pulses continue to be produced every add. time of period IV but have no effect on the division or square rooting.
	2) GP	2) Gated through K6 or L6 produces a DP or through K3 or L3 produces a SRP.	
	3) 1'P	3) Gated through F6 produces $1'P_1$.	
	4) CPP	4) Gated through K49 in the NI case or (gated through J49 in the I case) produces a signal which is gated through E50 to set the clear flip-flop and to reset the interlock coincidence flip-flop.	4) The clear flip-flop neon goes on at this time and the interlock coincidence flip-flop neon goes off.
2 (7)	1) CPP	1) Gated through F49 by a signal from the clear flip-flop, produces a CL' pulse.	
	2) CL'	2) a) (Gated through L48 by a signal from the interlock switch, resets the interlock flip-flop.) b) Clears the program ring to stage A. c) After passing through buffer E48 becomes a CL pulse.	
	3) CL	3) a) Resets the clear flip-flop. b) Clears the numerator binary ring to stage P. c) Resets the denominator flip-flop. d) Clears the place ring to stage 1. e) Resets the program ring flip-flop.	
	4) Signal resulting from the coincidence of the transceiver's being set and the clear flip-flop's being set.	4) a) Allows the carry clear gate to pass to the numerator and/or denominator accumulator clear circuits if clearing is specified. b) Gates a CPP through G8 to provide a reset signal for the transceiver and a program output pulse. c) Gates a CPP to set one of the four answer disposal receivers.	c) Thus, during the add. time following the divider's program output pulse, the answer is disposed of in accordance with the setting of the answer disposal switch. At the end of add. time 3, the answer disposal receiver is reset by a CPP.

*If the interlock input pulse is not received until k addition times after add. time 0 of period IV, this event and all events listed next to add. time 2 occur k addition times later than that indicated in this table.

through J9 and either the +2 or -2 receiver on the coincidence of a signal from gate J12 and either the like or unlike sign signal respectively.

6.2.7. Chronological Description of the Common Programming Circuits.

Tables 6-4, 6-5, and 6-6 summarize the operation of the common programming circuits during periods I, II, and III respectively of a division program. The corresponding summaries for the square rooting case are found in tables 6-7, 6-8, 6-9. Table 6-10 summarizes the events of period IV for both square rooting and division.

Below the title, each table carries a statement indicating the number of addition times required to complete the events of the period. In some cases, the events which occur in the last addition time of the period are listed in the comment column beside the events of the next to the last addition time instead of on a separate line (e.g. the events of addition time 4, period I for square rooting in table 6-7). This is done when the event described occurs, not in the common programming circuits of the divider and square rooter, but rather in an associated accumulator.

The overlapping of periods is also indicated on the tables. For example, addition time 3 of period I for division overlaps with addition time d of period II for the first basic division sequence. Thereafter, addition time d overlaps with the second addition time of the basic division sequence or with the second addition time of the shift sequence.

It is recommended that tables 6-4 through 6-10 be compared, at this time, with the illustrative problems in tables 6-2 and 6-3.

From the tables, it appears immediately that the exact number of

addition times required to complete any given division program* is

14+2 (p-2) + 2 (number of additions or subtractions of the denominator)

and that the number of addition times for any given square rooting program is

15 + 2 (p - 2) + 2 (number of additions or subtractions of the contents of the denominator accumulator)

where p is the number of places specified by the setting of the divide-square root. Since overdraft can never occur in division by zero, division by zero consumes an infinite number of addition times. If denominator equal to zero is a computational possibility, the operator should precede division programs by discrimination programs with the purpose of avoiding such divisions.

6.3. NUMERICAL CIRCUITS

The 10 stage place ring in the divider and square rooter serves to route the numerical data for the partial quotient or twice the square root into particular decade lines at particular times. The stages of this ring numbered 10, 1, 2, ..., 9 on PX-10-304 correspond respectively to decades 10, 9, ..., 1 of an accumulator. The place ring neons numbered 10, 9, ..., 1 on PX-10-302 correspond respectively to stages 10, 1, 2, ..., 9 of the place ring. It is to be noted that in period II for division or square rooting respectively, $\pm$ 1 or $\pm$ 2 units are put into the 10^8 decade place of the answer first. A digit different from zero (or the complement of zero if the quotient is negative) occurs in the 10^9 decade place of the answer only if the divider and square rooter puts in more than 10 pulses before the first shift sequence of period II

*Provided that the divider and square rooter need not mark time waiting for an interlock input pulse.

or, if 10 pulses are put in before the first shift, and carry over from the addition of one or two pulses at the end of round off cause carry over to the 10th decade place. The neon numbered 10 on PX-10-302 newer lights.

At the end of a divider and square rooter program this ring clears to stage 1. During the course of a program, the place ring can be cycled only during period II and then, only at the end of the first addition time (s + 1) of each shift sequence. The cycling of this ring is accomplished by the $1'P_2$ pulse which is produced when the $1'P_1$ pulse (see Section 6.2.2.) is passed through L45 by a signal from the S_α receiver.

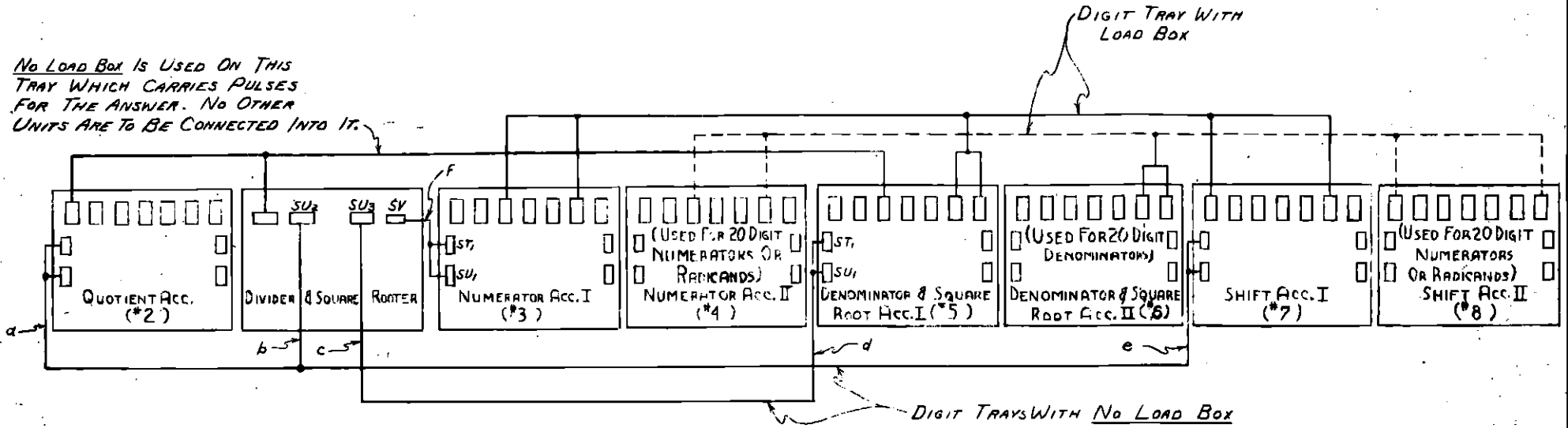
While the place ring has been classified as one of the numerical circuits, one of its functions is purely a programming function. Stages 3, 6, 7, 8, and 9 of the ring are connected respectively to gates C41, B41, A41, A42, and A43. The second inputs to these gates are connected respectively to points 4, 7, 8, 9, and 10 of the divide-square root and places switch. Upon the coincidence of a signal from the place ring and the divide-square root and places switch, the appropriate gate emits a signal which allows an S pulse to pass through gate E6. The resulting SS pulse terminates period II by flipping the pulse source flip-flop into the abnormal state.

The place ring carries out its numerical functions by its control of the 2 sets of answer output gates (B through L42, and B through L43). One gate from the group with No. 42 and one from the group with No. 43 is connected to each stage of the place ring. The second input to these gates comes from a line carrying digit pulses gated through the 1, 2, 2', 4, 9, and 1' pulse gates by the setting of the +1, -1, +2, or -2 receiver.

The routing of digit pulses into the appropriate decades by the place

ring can probably best be explained by means of numerical examples. Let us assume that at some time in the course of a computation the place ring is in stage 2 (this implies that one shift sequence has been completed thus far in the computation) and that the +1 receiver is set at the end of some addition time d+1 of period II. Then, in addition time d+2, gate L46 passes the 1P and all of the other gates of this group are closed. This single pulse is delivered to all of the gates B through L42. Since the place ring is in stage 2, however, the only open gate of this group is J42. Therefore, one pulse is emitted in decade place 8 (corresponding to the 10^7 decade of an accumulator) and no pulses are emitted over any of the other leads of the answer output terminal.

Next, let us consider another case. Suppose that the place ring is in stage 2 and that the -2 receiver is set at the end of some addition time r+1 of period II. Then in addition time r+2, 7 pulses formed from the 1, 2, and 4P passed through gates K47, J47, and H47 respectively are delivered to gates B through L42, the 9P passed through gate G47 are delivered to the gates B through L43 and to the PM lead of the answer output, and the 1'P passed through B46 is delivered directly to the answer output lead for units decade. Since the ring is in stage 2, gate J42 is the only open gate of the group B through L42 and gate J43 is the only closed gate of the group B through L43. Thus, 7 pulses are emitted over lead 8 of the answer output terminal and 9 pulses are emitted over all of the other leads including the PM lead. In the first half of addition time r+2, then, the denominator accumulator receives from the answer output terminal of the divider and square rooter M 9 979 999 999. At the time of the 1'P during addition time r+2, the 1'P passed through B46 is put into the units decade place of the answer output so that by the end of addition time r+2, the



Item	Description	Refer To
ST_1, SU_1	Accumulator Interconnector Terminals	PX-5-105
SU_2, SU_3, SV	Divider & Square Rooter Programming Terminals	PX-10-108
a	Special Cable From Digit Tray To ST_1 & SU_1 On Quotient Acc.	PX-5-134
b, c	Adaptors From SU_2 To Digit Tray Or From SU_3 To Digit Tray	PX-4-114A, A & AC Adaptor PX-4-114B, A & S Adaptor PX-4-114C, AC & SC Adaptor
d	Special Cable From Digit Tray To ST_1 & SU_1 On The Denom. & Sq. Root Acc.	PX-5-136
e	Special Cable From Digit Tray To ST_1 & SU_1 On The Shift Acc.	PX-5-135
f	Special Cable From SV To ST_1 & SU_1 On The Numerator Acc.	PX-5-132

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denominator accumulator receives from the divider and square rooter M 9 980 000 000 which is the complement of 2 in the 10^7 decade place.

It is to be noted that in the divider and square rooter as in the high-speed multiplier, standard transmitters have not been used in the answer output circuit. Therefore, the numerical data for the answer must be delivered to the quotient or denominator accumulator via either a digit tray used for no other purpose or else by means of a special cable made for this purpose. No load box is used on this digit tray.

6.4. INTERRELATION OF THE DIVIDER AND SQUARE ROOTER AND ITS ASSOCIATED ACCUMULATOR.

6.4.1. Interconnections for numerical data.

PX-10-307 shows the interconnections which must be made among the accumulators associated with the divider and square rooter to carry out division or square rooting programs when arguments of 10 or fewer places are involved. Divisions involving arguments with from 10 to 20 places may be handled by interconnecting accumulators 3 and 4 (for 20 digit numerators) and accumulators 5 and 6 (for 20 digit denominators). In this case another digit tray is used to connect the add output terminal of the right hand numerator accumulator to the α input terminal of the right hand shift accumulator and a second additional tray to connect the add output terminal of the right hand shift accumulator to the γ input terminal of the right hand numerator accumulator. If the denominator has more than 10 digits, the add and subtract output terminals of the right hand denominator accumulator are also connected into the latter tray.

It is to be noted that no mention has been made of interconnecting a pair of accumulators to accumulate quotients or two-roots having between 10

and 20 places. The reason for this omission is that the divider and square rooter is incapable of finding such answers in one operation because the place ring has but 10 stages and the answer output terminal but 11 leads (and a ground).

Quotients with between 10 and 19 places can be found by performing 2 division programs serially. With the divide-square root and places switch of the program control used for the first division set at 10, 9 or 10 places (depending on the relative placement of the numerator and denominator in the argument accumulators - see Section 6.4.3) of the answer are found. The round off switch of the first program control should be set to NRO and the argument accumulator clear switches to 0. When the first division program is completed, the quotient as thus far obtained is then transmitted from (and cleared out of) the quotient accumulator to the left hand accumulator of a pair external to the divider and square rooter system. The left hand accumulator of this pair should be stimulated to receive this quotient through some input channel, say α. Then the α input terminal of the right hand accumulator should not be connected to the same tray as the A output terminal of the quotient accumulator. Because of the setting of the round off and argument clear switches, the divider and square rooter can then proceed on its second program, the division of the remainder from the numerator by the denominator. The quotient obtained in this way contributes 9 more places of the answer. The number stored in the 10^8 decade place of the quotient accumulator after the second division belongs in the 10^9 decade place of the right hand accumulator and the number stored in the 10^9 decade place of the quotient accumulator belongs in the units decade place of the left hand accumulator. If the numerator and denominator before the first division program have like signs, the remainder from the numerator after the

first program and the denominator have unlike signs so that the quotient obtained by the second division program is necessarily negative. Therefore the second quotient must be transmitted to the pair of interconnected accumulators with its sign indication. The second quotient may be properly received in the pair of accumulators if these accumulators receive the second quotient from the quotient accumulator through an input channel different from the one used for receiving the first quotient, say the β input channel and the β input terminals of both the left and right hand accumulators should be connected to the tray to which the A output terminal of the quotient accumulator is connected. Special adaptors and shifters must then be used at the β input terminals of the right and left hand accumulators. The right hand accumulator's β input terminal should have plugged into it a shifter which shifts the data one place to the left. The left hand accumulator's β input terminal should have an adaptor which connects the left hand accumulator's PM input and 10^9, 10^8, ..., 10^1 decade place input leads to the PM line of the digit tray and which connects the 10^0 decade place input lead to the 10^9 decade place line of the digit tray.*

If 9 or 10 decade places of twice the root are found by a given square rooting program, it is possible to find about as many places again of the root

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*If it is known that the numerator and denominator for all division programs will always have like sign and if the first division program is stopped after 9 places instead of 10, then the denominator and the remainder from the numerator again have like sign so that the quotient obtained from the second division is positive. Under such circumstances the second quotient should be so shifted that information from the 10^8 and 10^9 decade leads of the quotient accumulator add output is received in the units and tens decade places of the left hand accumulator and the other digits of the second quotient are received in the right hand accumulator shifted over two places to the left. The connections of the PM lead of the output of the quotient accumulator to the PM and 10^9 - 10^3 decade place leads of the input to the left hand accumulator may obviously be omitted.

(notice, not twice the root) by dividing the remainder from the radicand by twice the root as thus far found. The procedure for obtaining the final answer in a pair of interconnected accumulators external to the divider and square rooter system of accumulators is similar to that for the case discussed above for division. However, if it is desired to accumulate the root in the pair of interconnected accumulators, twice the root (resulting from the first program) should be multiplied by 0.5 before its reception in the left hand accumulator or, if it is desired to accumulate twice the root in the final accumulator, the quotient (resulting from the second program) should be multiplied by two before its reception by the pair of interconnected accumulators.

6.4.2. Interconnections for Programming Instructions.

PX-10-307 shows the interconnections which must be established between the divider and square rooter and its associated accumulators for the purpose of communicating programming instructions. For information about the wiring of the various program terminals on the divider and square rooter see PX-10-108, and for the wiring of the accumulator interconnector terminals which receive signals from the divider and square rooter program terminals see PX-5-105. On PX-10-108, SU_2 refers to the quotient accumulator and shift accumulator program terminal, SU_3 to the denominator-square root accumulator program terminal, and SV to the numerator accumulator interconnector terminal. ST_1 and SU_1 on PX-5-105 refer to the accumulator interconnector terminals designated by I_{L1}, and I_{L2} respectively on PX-5-301.

The numerator accumulator interconnector terminal on the divider and square rooter is connected directly to the left hand interconnector terminals on the numerator accumulator by means of the numerator accumulator interconnector

cable shown on PX-5-132. The correspondence of the points α and β on the numerator accumulator switch and the α and β input channel receive circuits in the numerator accumulator is established by the wiring of the plugs of this cable.

Adaptors which will be discussed further below are plugged from the denominator-square root accumulator program terminal and from the quotient and shift accumulator program terminal to two different digit trays. The denominator square root accumulator interconnector cable shown on PX-5-136 carries programming instructions to the denominator-square root accumulator's left hand interconnector terminals from the tray connected through an adaptor to the divide-square root accumulator program terminal on the divider. The quotient accumulator interconnector cable shown on PX-5-134 and the shift accumulator interconnector cable shown on PX-5-135 carry instructions to the quotient and shift accumulators' left hand interconnector terminals respectively from the digit tray connected through an adaptor to the quotient and shift accumulator program terminal on the divider and square rooter.

The adaptors referred to in the preceding paragraph are shown on PX-4-114 A, B, and C. These adaptors may be used interchangeably at either the denominator-square root accumulator program terminal or at the quotient and shift accumulator program terminal. Leads 1-7 on the plug and socket of all the adaptors are wired in the same way; but, to provide flexibility in the meanings assigned to the points 1, 2, 3, and 4 on the answer disposal switch, some or all of leads 8. 9 10, and 11* on the plug are wired in different ways

*Leads 8 and 10 on the quotient and shift accumulator program terminal correlate with points 1 and 2 of the answer disposal switch, and leads 8 and 10 on the denominator-square root accumulator program terminal correlate with points 3 and 4 of the answer disposal switch. Leads 9 and 11 on both program terminals are associated respectively with 8 and 10 for answer disposal instructions which involve clearing.

to leads on the sockets of the various adaptors.

When used with the standard quotient accumulator interconnector cable (PX-5-134) or denominator square root accumulator interconnector cable (PX-5-136) the adaptors referred to provide the following answer disposal options:

PX-4-114A	{transmit additively without clearing transmit additively with clearing
PX-4-114B	{transmit additively transmit subtractively
PX-4-114C	{transmit additively with clearing transmit subtractively with clearing

To illustrate the way in which these adaptors function let us consider a case in which adaptor PX-4-114A is plugged into the quotient accumulator and shift accumulator program terminal and adaptor PX-4-114C into the denominator-square root accumulator program terminal. Then the points on the answer disposal switch have the following meanings:

1 - transmit the quotient additively without clearing

2 - transmit the quotient additively with clearing

3 - transmit twice the root additively with clearing

4 - transmit twice the root subtractively with clearing

For computations in which other answer disposal option combinations than those provided by the 3 adaptors described above are needed, additional adaptors can be custom made.

6.4.3. Relationship between Alignment of the Arguments and the Answer.

The operator must exercise considerable care in the placement of the arguments in the argument accumulators for division or square rooting programs in order to make the most efficient use of the divider and square rooter.

PX-10-412

TABLE 6-11

POSSIBLE PLACEMENT OF RADICAND (also see Table 6-12)

Period	Add. Time	Numerator (Radicand) Accumulator		Denominator (Two Root) Accumulator		Shift Accumulator	
		Receives	Stores after receiving	Receives	Stores after receiving	Receives	Stores after receiving
Example A							
I	1	P 0 900 000 000	P 0 900 000 000				
	2						
	3						
	4			P 0 100 000 000	P 0 100 000 000		
II	5	M 9 900 000 000	P 0 800 000 000				
	6			P 0 200 000 000	P 0 300 000 000		
	7	M 9 700 000 000	P 0 500 000 000				
	8			P 0 200 000 000	P 0 500 000 000		
	9	M 9 500 000 000	P 0 000 000 000				
	10			P 0 200 000 000	P 0 700 000 000		
	11	M 9 300 000 000	M 9 300 000 000				
	12			P 0 200 000 000	P 0 900 000 000		
shift	13	~~~~		M 9 900 000 000	P 0 800 000 000	M 9 000 000 000	M 3 000 000 000
Example B							
I	1	P 2 401 000 000	P 2 401 000 000				
	2						
	3						
	4			P 0 100 000 000	P 0 100 000 000		
II	5	M 9 900 000 000	P 2 301 000 000				
	6			P 0 200 000 000	P 0 300 000 000		
	7	M 9 700 000 000	P 2 001 000 000				
	8			P 0 200 000 000	P 0 500 000 000		
	9	M 9 500 000 000	P 1 501 000 000				
	10			P 0 200 000 000	P 0 700 000 000		
	11	M 9 300 000 000	P 0 801 000 000				
	12			P 0 200 000 000	P 0 900 000 000		
	13	M 9 100 000 000	M 9 901 000 000				
	14	~~~~		P 0 200 000 000	P 1 100 000 000		
shift	15			M 9 900 000 000	P 1 000 000 000	M 9 010 000 000	M 9 010 000 000

PX-10-013

TABLE 6-12

INCORRECT PLACEMENT OF RADICAND

Period	Add. Time	Numerator (Radicand) Accumulator		Denominator (Two-digit) Accumulator		Shift Accumulator	
		Receives	Stores after receiving	Receives	Stores after receiving	Receives	Stores after receiving
Example C							
I	1	P 2 500 000 000	P 2 500 000 000				
	2						
	3						
	4			P 0 100 000 000	P 0 100 000 000		
II	5	M 9 900 000 000	P 2 400 000 000				
	6			P 0 200 000 000	P 0 300 000 000		
	7	P 9 700 000 000	P 2 100 000 000				
	8			P 0 200 000 000	P 0 500 000 000		
	9	M 9 500 000 000	P 1 600 000 000				
	10			P 0 200 000 000	P 0 700 000 000		
	11	M 9 300 000 000	P 0 900 000 000				
	12			P 0 200 000 000	P 0 900 000 000		
	13	M 0 100 000 000	P 0 000 000 000				
	14			P 0 200 000 000	P 1 100 000 000		
	15	M 8 900 000 000	(M 8 900 000 000)				
	16			P 0 200 000 000	P 1 300 000 000		
shift	17	~~~~~		M 9 900 000 000	P 1 200 000 000	M 9 000 000 000	(M 9 000 000 000)

THE WRONG ANSWER WILL RESULT BECAUSE THE SIGNIFICANT FIGURE, 8, OF THE REMAINDER FROM THE RADICAND (see add. time 15) IS THROWN AWAY WHEN SHIFTING TAKES PLACE (see add. time 17).

From the fact that the divider and square rooter place ring allows one unit to pass to the 10^8 decade of the two root accumulator at the beginning of a square rooting program, it is obvious that the divider and square rooter proceeds on the assumption that the decimal point of the radicand occurs an even number of places (either right or left) from the PM place of the numerator accumulator. The operator therefore, must align the radicand in the numerator accumulator so that THE DECIMAL POINT OF THE RADICAND OCCURS AN EVEN NUMBER OF PLACES TO THE RIGHT OR LEFT OF THE NUMERATOR ACCUMULATOR'S PM POSITION.

A comparison between the square rooting example in Table 6-3 and the examples in Tables 6-11 and 6-12 also points to another consideration concerning the placement of the radicand. Examples A and B show radicands placed so that the correct answer will be obtained. Example C shows a radicand placed in such a way that the divider and square rooter cannot possibly obtain the correct answer. The examples in Tables 6-11 and 6-12 have all been carried through the first addition time of the first shift sequence since the reason for the impossibility of example C shows up at that time. In examples A and B (and also in table 6-3) when the remainder from the radicand is shifted the 9 at the extreme left is thrown away. This 9 (preceded by sign M) is not a significant figure since it is merely the complement of a non-significant zero at the left. In example C, however, the figure 8 at the far left of the remainder from the radicand is thrown away when shifting takes place. This figure (preceded by sign M), the complement of the digit 1, is a significant figure. Therefore, when the basic square rooting sequence is resumed after the completion of the shift sequence,,it will be resumed with an incorrect remainder from the radicand. A significant figure of the remainder from the radicand will be thrown away in

the first shift sequence whenever the first two decade places at the extreme left of the radicand accumulator are occupied by the number 25 or any greater number. Therefore, in general, AT LEAST ONE ZERO SHOULD PRECEDE THE FIRST NON ZERO DIGIT (at the extreme left) OF THE RADICAND.

If the radicand's decimal point occurs n (positive to the right; negative to the left) decade places from the PM, the decimal point of twice the root occurs $\frac{n}{2} \pm \frac{1}{2}$ places from the PM. For example, in the computation of table 6-3, if the decimal point is considered to occur between the digits 1 and 3 of the radicand, then n is 4 and the decimal point of twice the root occurs 3 places to the left of the PM or after the digit 8. The rule given above may be derived from considerations arising out of the material in Table 6-1.

From the fact that the divider emits +1 or -1 unit in the 10^8 decade for every repetition of the basic division sequence until the first shift sequence of period I, it can be seen that if the first non-zero digit at the left of the denominator occupies the same decade place of the denominator accumulator as the second (from the left) non-zero digit of the numerator does in the numerator accumulator, then the first (from the left) non-zero digit of the quotient occupies either the first of second decade place to the left of the PM in the quotient accumulator (see Section 6.3). If the standard alignment of the denominator is defined to mean the alignment in which the first non-zero digit of the denominator occurs one decade place further to the right than does the first non-zero numerator digit, then shifting the denominator k places to the left or right of the standard alignment, results in shifting the alignment of the quotient k places to the right or left respectively of the position described above. Since with the standard alignment of the denominator, the

first (from the left) non-zero digit of the quotient may occupy the extreme left decade of the quotient accumulator, it follows immediately that THE FIRST (from the LEFT) NON-ZERO DENOMINATOR DIGIT MUST NEVER OCCUR IN A DECADE PLACE TWO OR MORE TO THE RIGHT OF THE DECADE PLACE OF THE FIRST (from the LEFT) NON-ZERO DIGIT OF THE NUMERATOR or else the quotient may exceed the capacity of the quotient accumulator.

Another restriction on the placement of the denominator is that THE FIRST (from the LEFT) NON-ZERO DENOMINATOR DIGIT MUST NOT OCCUPY THE FAR LEFT DECADE PLACE OF THE DENOMINATOR ACCUMULATOR. The reason for this restriction is similar to the reason for not placing the first non-zero radicand digit in the extreme left hand decade place of the numerator accumulator (see Table 6-12). If this rule is violated, a significant figure of the remainder from the numerator may be discarded when the first shift sequence of period II occurs.

If the decimal points of the numerator, denominator, and quotient respectively occur n, d, and q places from the PM place (where n, d, and q are positive when counted toward the right from the PM place), then q may be predicted by the following formula:

$$q = n - d + 2$$

The following tabulation based on the example in table 6-2 illustrates this rule.

Numerator	n	Denominator	d	Quotient	q
P 0 209.070 000	4	P 0 230 000 000	3	P 0 091.000 000	4
P 0.209 070 000	1	P 0 23.0 000 000	3	P.0 091 000 000	0
P 0.209 070 000	1	P 0 230. 000 000	4	(P.0 091 000 000)x10^{-1}	-1

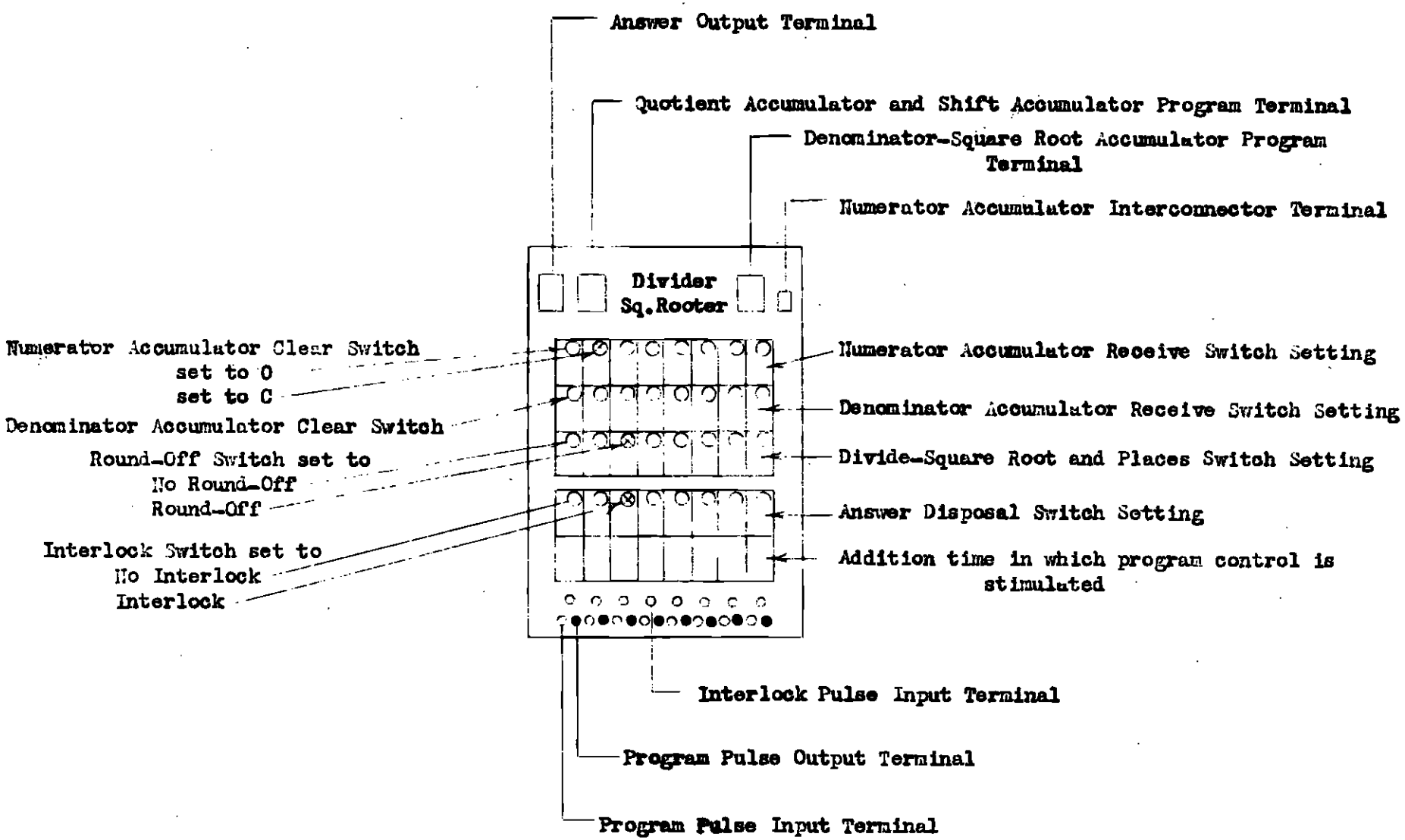


Figure 6-1

SYMBOLS USED FOR DIVIDER AND SQUARE ROOTER ON SET-UP DIAGRAM

6.5. ILLUSTRATIVE PROBLEM SET-UP

Table 6-13 contains instructions for setting up the units of the ENIAC to carry out a computation illustrating typical situations which arise when the divider and square rooter is used. The symbols used in this table with reference to accumulators and the high-speed multiplier have been previously taken up in chapters II and V. The master programmer is used in this set-up to route a program pulse received by it over a given program line (1-2) into 3 different program lines (2-4, 2-5, and 2-6) on 3 different occasions. For details concerning this use of the master programmer see Chapter X. The instructions to the master programmer appear in the double column immediately after the addition time column of Table 6-13. The first half of the double column shows the input terminal to which the program pulse from line 1-2 is delivered. The second half of the column designates the program output terminal (A_1o, A_2o, or A_3o) through which the master programmer delivers the program output pulse and the program line to which the program pulse output terminal is connected (2-4, 2-5, or 2-6).

The set-up table instructions given to the divider and square rooter occupy 5 levels. These instructions appear in the following order:

1) on the first level, i-j represents the program input pulse and (k) the program control number
2) on the second level,
   the first pair of symbols represents the numerator accumulator receive and clear switch settings,
   the second pair of symbols represents the denominator accumulator receive and clear switch settings,

the last symbol represents the answer disposal switch setting (1, 2, 3, 4, or 0). The code for 1-4, which depends on the adaptor used, is given at the head of the divider and square rooter column.

3) on the third level,

the first pair of symbols represents the setting of the divide-square root and places switch,

the next symbol represents the round off switch setting.

4) on the fourth level the setting of the interlock switch (I or NI) is given. In interlock programs the program line from which the interlock pulse is received is noted in a parenthesis next to the symbol I.

5) on the fifth level, which is written on the line for the addition time* which represents the last one of the program, the program output pulse is written.

For example, the group of symbols shown at the left below describes the following instructions:

Add. Time	Divider 1 = AC 3 = AC 2 = SC 4 = SC
I - 5	1-1 (5) αC 00 4 R8 RO I (2-6)
	↓
End of div. program	↓ 1-3
II - 1	

In addition time I-5 a program pulse from line 1-1 stimulates control 5 to carry out a square rooting program to 8 places with round off. The radicand is received via the α input channel of the numerator accumulator and the numerator accumulator is

*The practice adopted here with regard to counting addition times is to identify addition times by a roman numeral and arabic numeral. A new roman numeral is used when a division program is completed and addition times are then counted from arabic numeral 1 again.

cleared at the end of the program. The interlock pulse is received from program line 2-6. At the end of the program a program output pulse is emitted over line 1-3. Twice the square root is disposed of subtractively from the denominator accumulator which is then cleared.

The conventions used with regard to the divider and square rooter in set-up diagrams are explained in Figure 6-1 and those relating to the master programmer in Figure 10-1 of Chapter X.

The computation described in Table 6-13 consists of forming X where

$$X = \frac{\sqrt{a} + \sum_{i=1}^{3} x_i^3}{b} + c.d$$

It is assumed that the quantities a, 2b, c, d, x_1, x_2, and x_3 have been formed before this computation begins and they are stored in the units indicated in the table on the line corresponding to addition time zero. The ranges of these quantities are indicated on the table and the fact that a quantity's decimal point occurs n decade places from the PM is symbolized by $[n]$ where n is positive when counted toward the right.

The computation of $\sqrt{a}$ begins in addition time I-1 and the computation of $\sum_{i=1}^{3} x_i^3$ proceeds in parallel with this. Only two program controls on the high-speed multiplier are devoted to the 6 multiplications involved in forming $\sum x_i^3$. To do this, however, 3 stages of master programmer stepper A (see Chapter X) and 3 dummy programs (set up on program controls 5, 6, and 7 of accumulator 9) are used. While approximately the same amount of equipment is required as would be the case if 6 multiplier programs were used, this procedure may be desirable in computations where so many multiplications are performed

that multiplier program controls are at a premium.

Program control (9) of the high speed multiplier is used for the computation of x_i^3. One addition time before this control is stimulated, however, the accumulator which stores the particular x_i needed is stimulated to transmit twice to the ier and icand accumulator. Since the high-speed multiplier is stimulated in time for only the second transmission, the ier and icand accumulators receive not $2x_i$ but only x_i.

x_i^3 is formed immediately after x_i^2 through the use of high-speed multiplier program control (10). The number x_i remains in the ier accumulator from the previous multiplication and x_i^2 is received in the icand accumulator from the final product accumulator. When this multiplication is completed, $2x_i^3$ is transferred to accumulator 12. The multiplier is made to stimulate the disposal of twice the product stored in the product accumulator by setting the product disposal switch at SC and connecting the SC output terminal on panel 3 of the multiplier to a program control on accumulator 13 which is instructed to transmit two times additively with clearing.

The master programmer in this problem serves to pick out the argument which is to be used whenever multiplier program control (9) is to operate and indirectly stimulates the performance or non-performance of the program set-up on multiplier control (9). The former action occurs because the master programmer's output pulse is delivered to a program control on the appropriate accumulator; the latter effect occurs because the master programmer's output pulse is delivered to dummy program controls whose output pulses, in turn, are

PX-10402 (a)

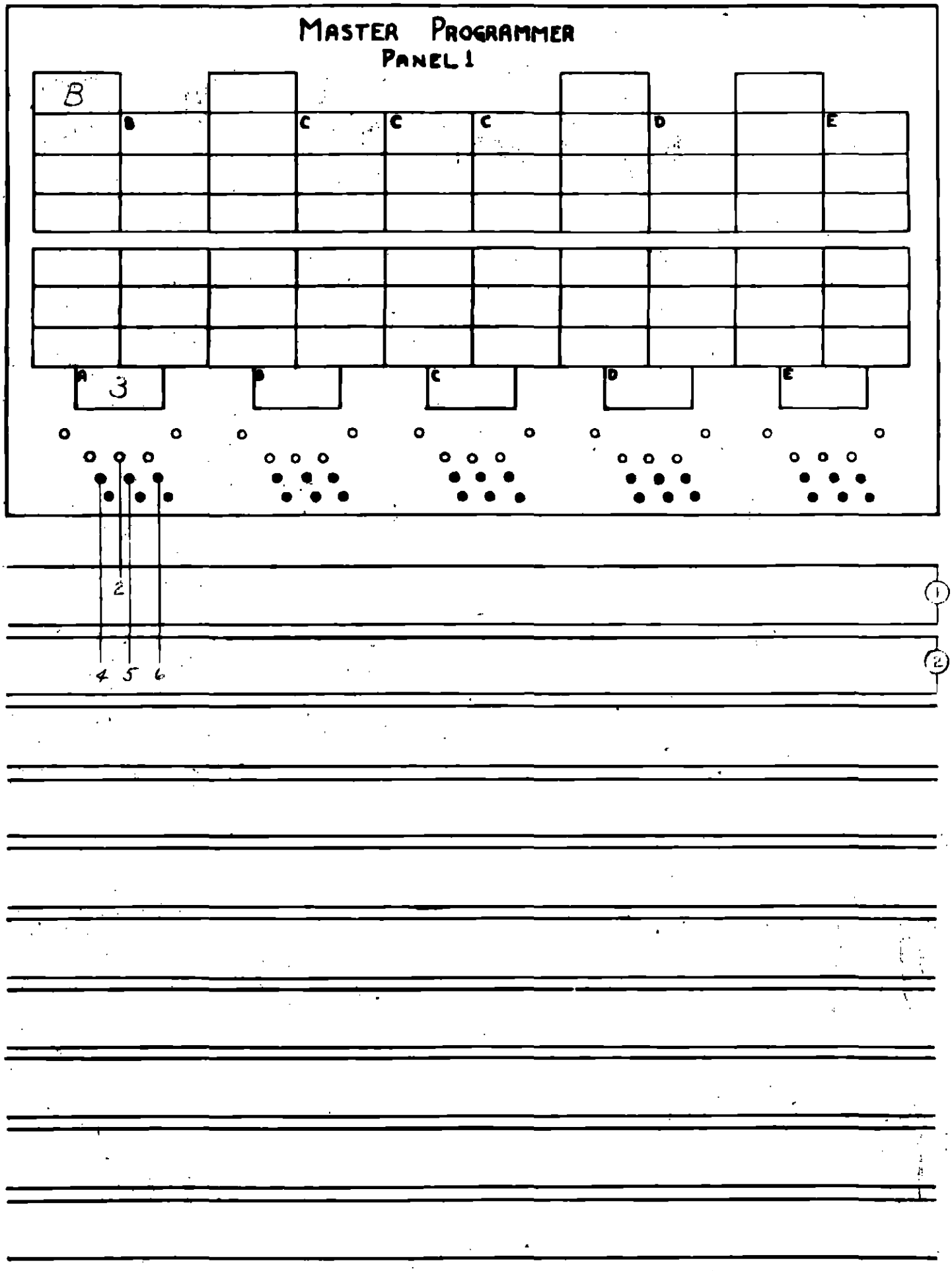


Fig. 6-2 (a)

SET-UP DIAGRAM FOR COMPUTATION OF $\frac{\sqrt{a} + \sum_{i=1}^{3} x_i^3}{b}$ + cd.

PX-10-102 (b)

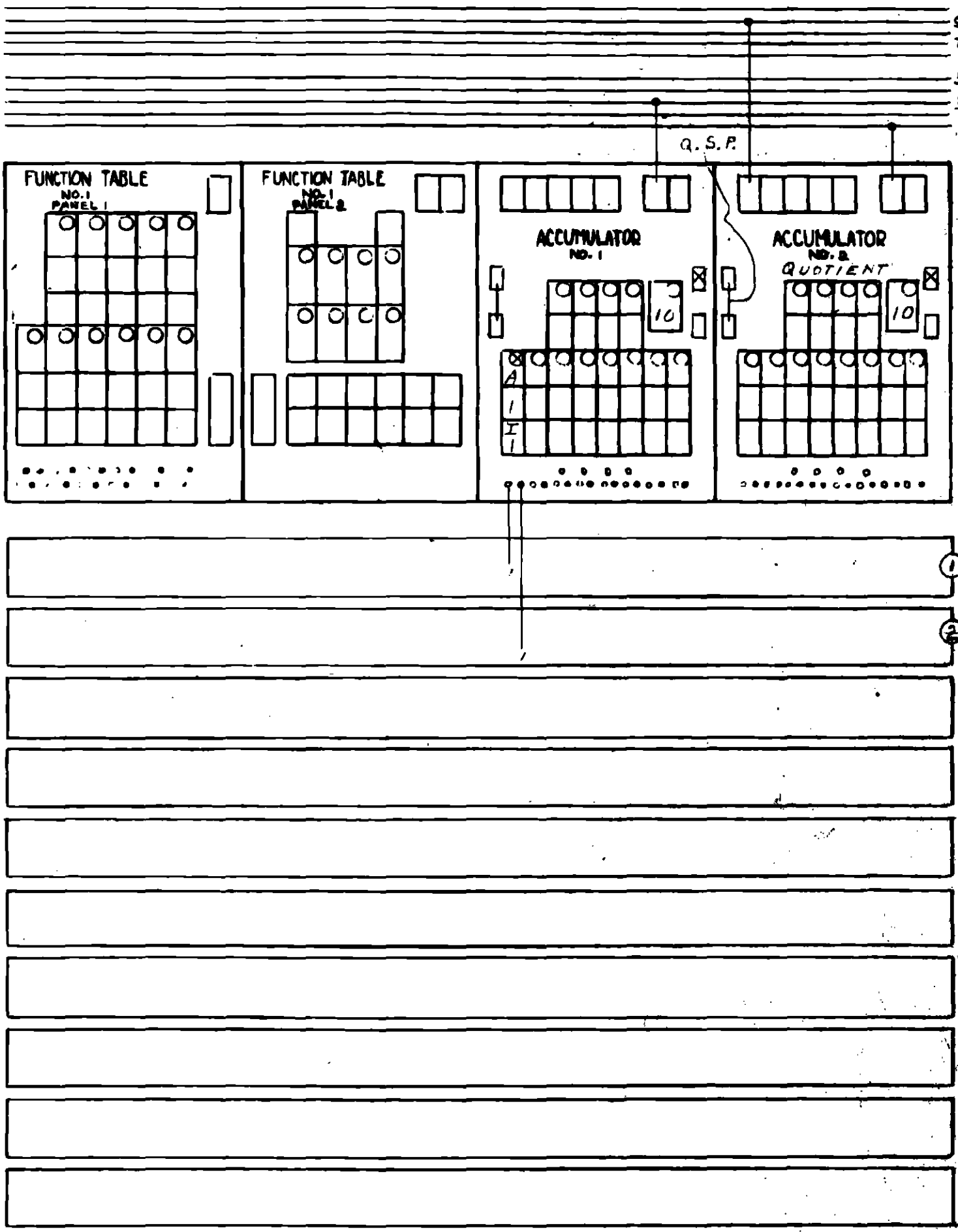


Fig. 6-2 (b)

SET-UP DIAGRAM FOR COMPUTATION OF $\frac{\sqrt{a} + \sum_{i=1}^{3} x_i^3}{b} + cd$

PX-10-402 (c)

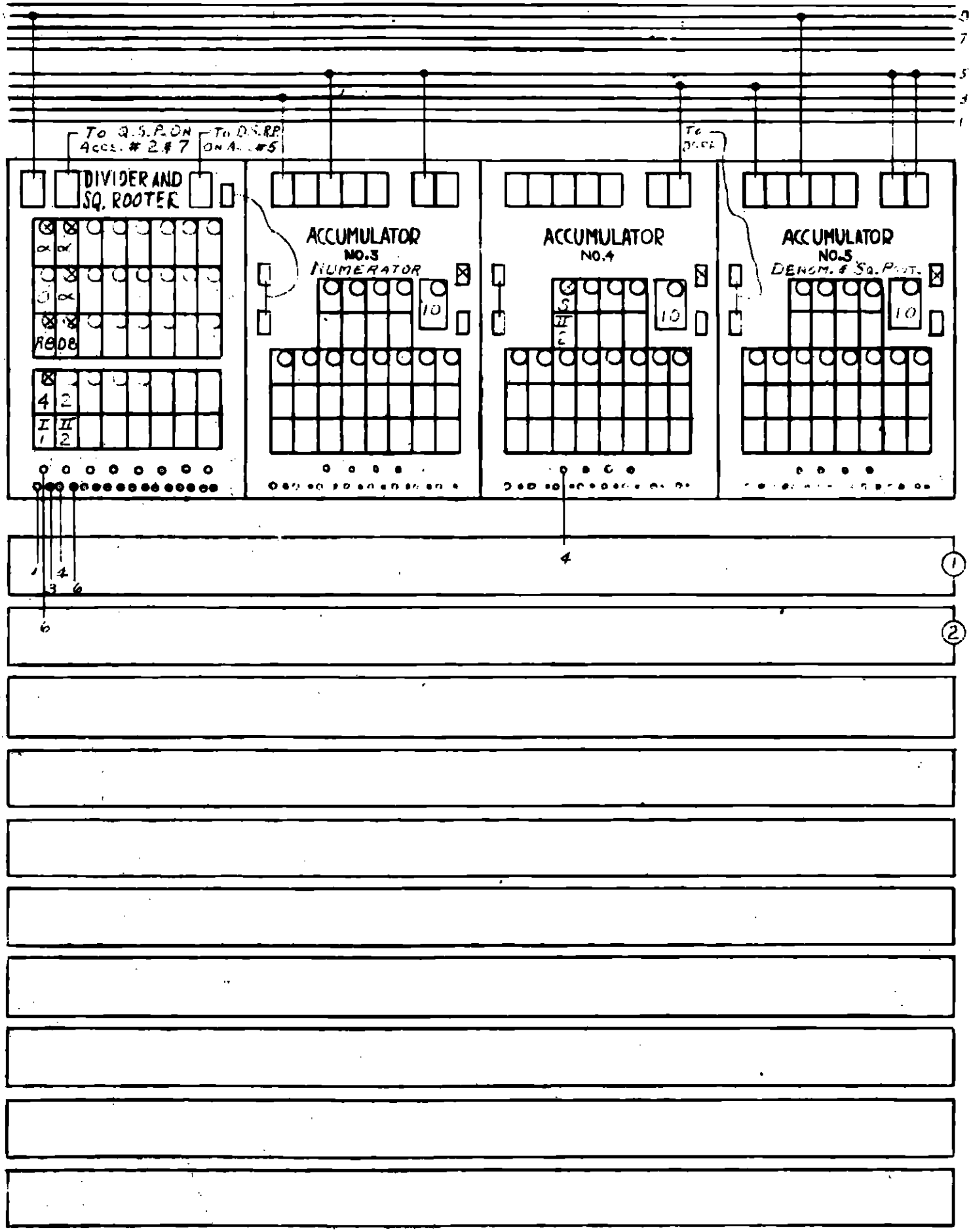


Fig. 6-2 (c)

SET-UP DIAGRAM FOR COMPUTATION OF $\frac{\sqrt{a} + \sum_{i=1}^{3} x_i^3}{b} + cd$

PX-10-402 (4)

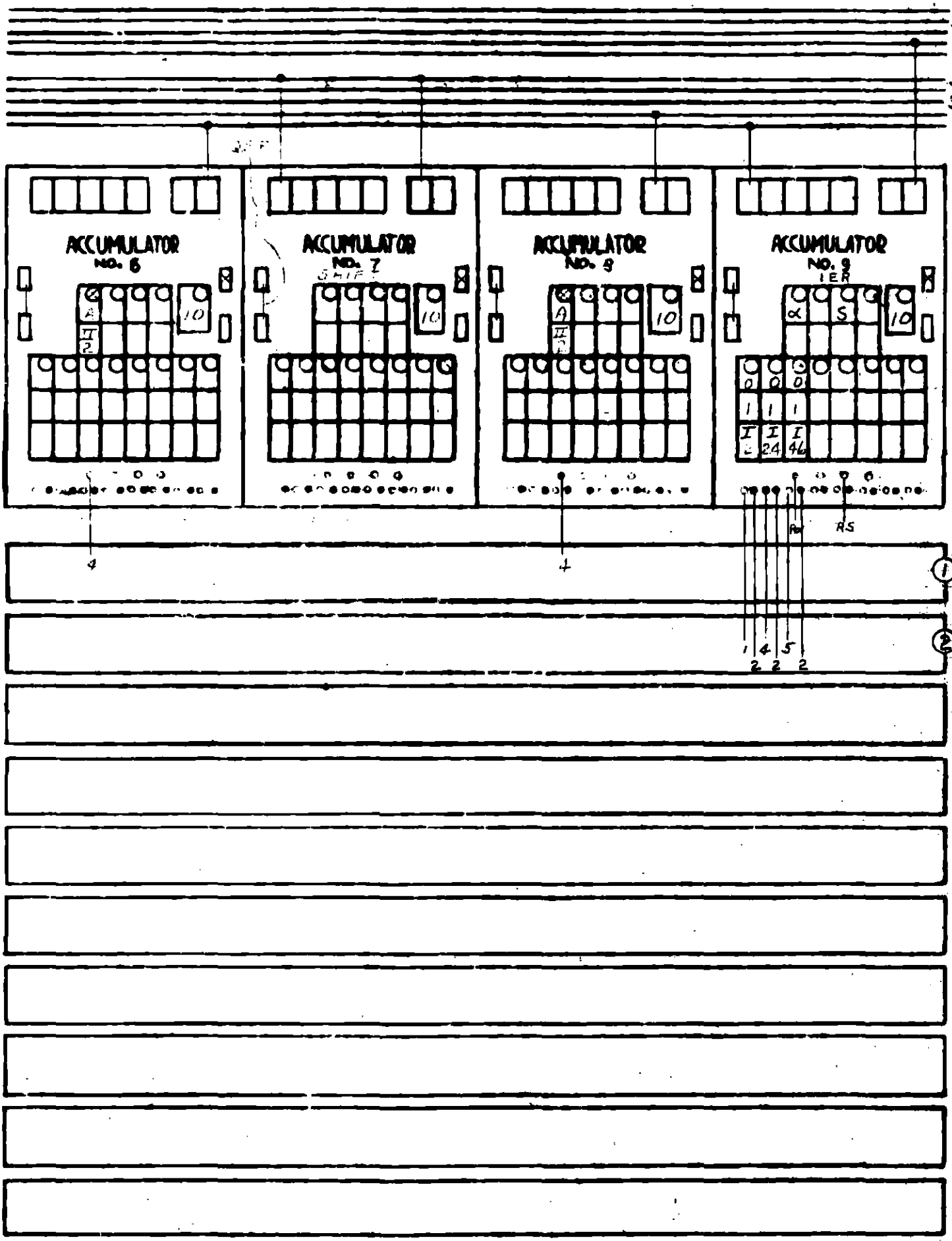


Fig. 6-2 (d)

SET-UP DIAGRAM FOR COMPUTATION OF $\frac{\sqrt{a} + \sum_{i=1}^{3} x_i^3}{b} + cd$

PX-10-402 (E)

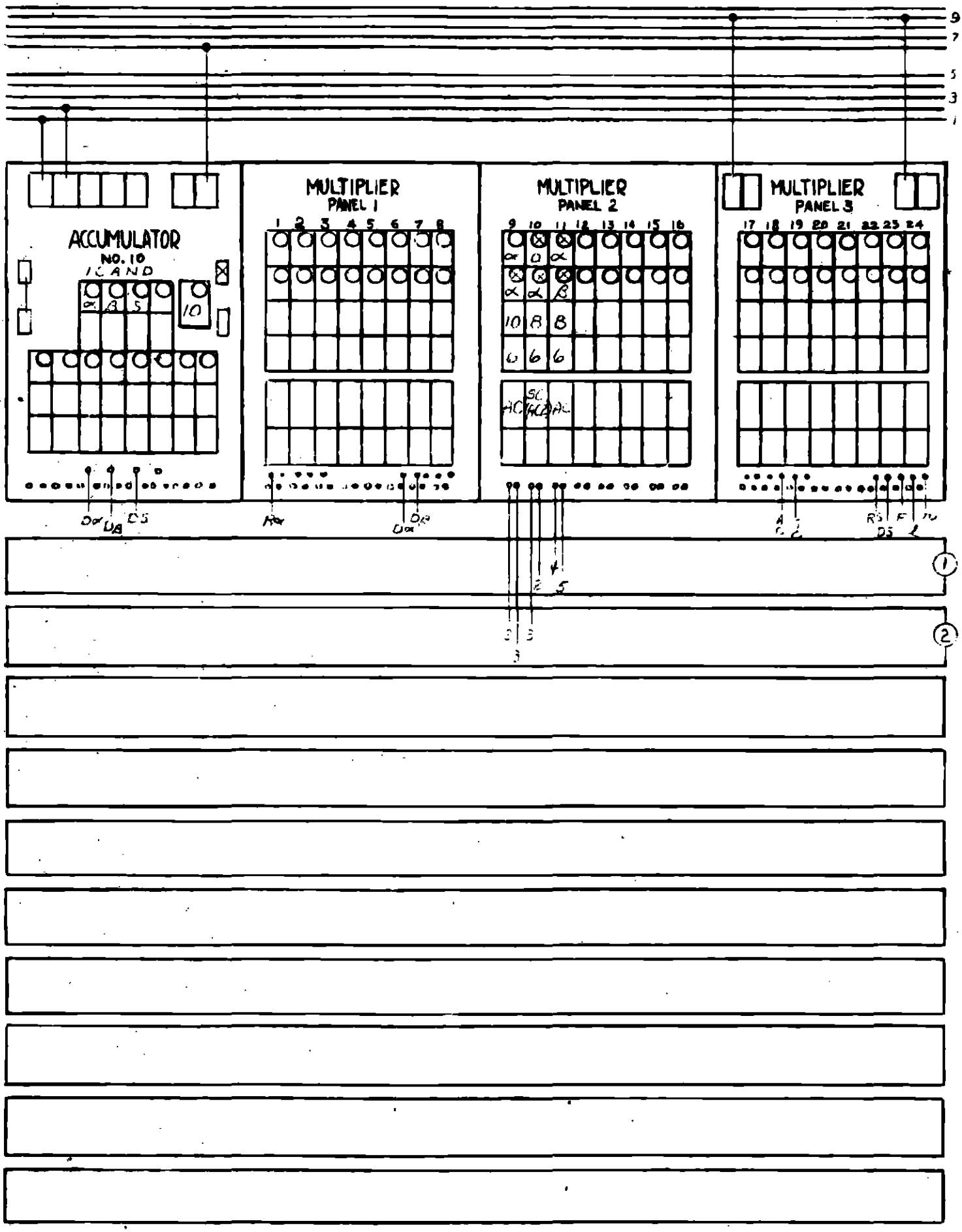


Fig. 6-3 (a)

SET-UP DIAGRAM FOR COMPUTATION OF $\frac{\sqrt{a}+\sum_{i=1}^{3} x_i^3}{b} + cd$

PX-10-10Z (F)

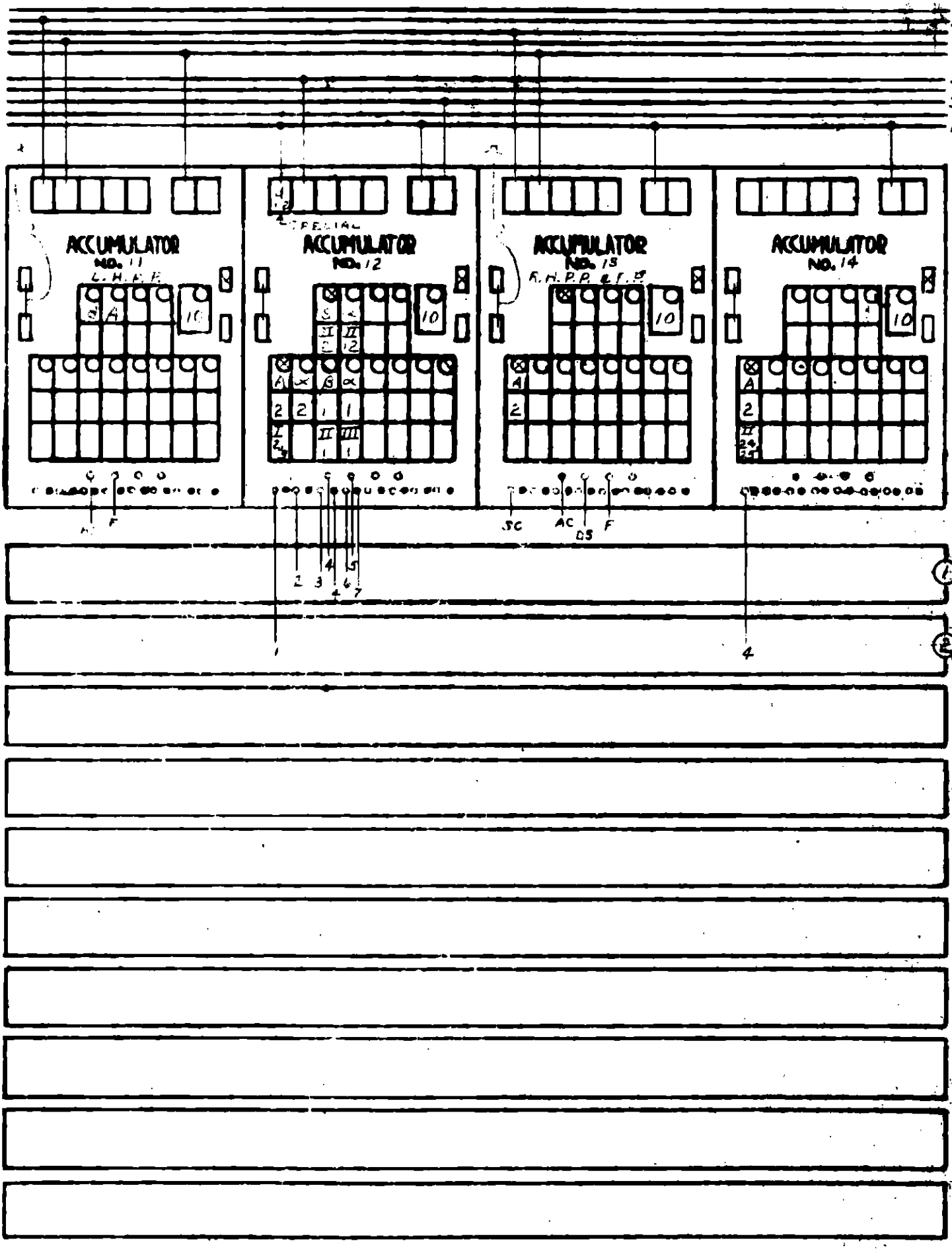


Fig. 6-2 (f)

SET-UP DIAGRAM FOR COMPUTATION OF $\frac{\sqrt{b}+\sum_{i=1}^{3} x_i^3}{b}$ + cd

PK-10-492 (4)

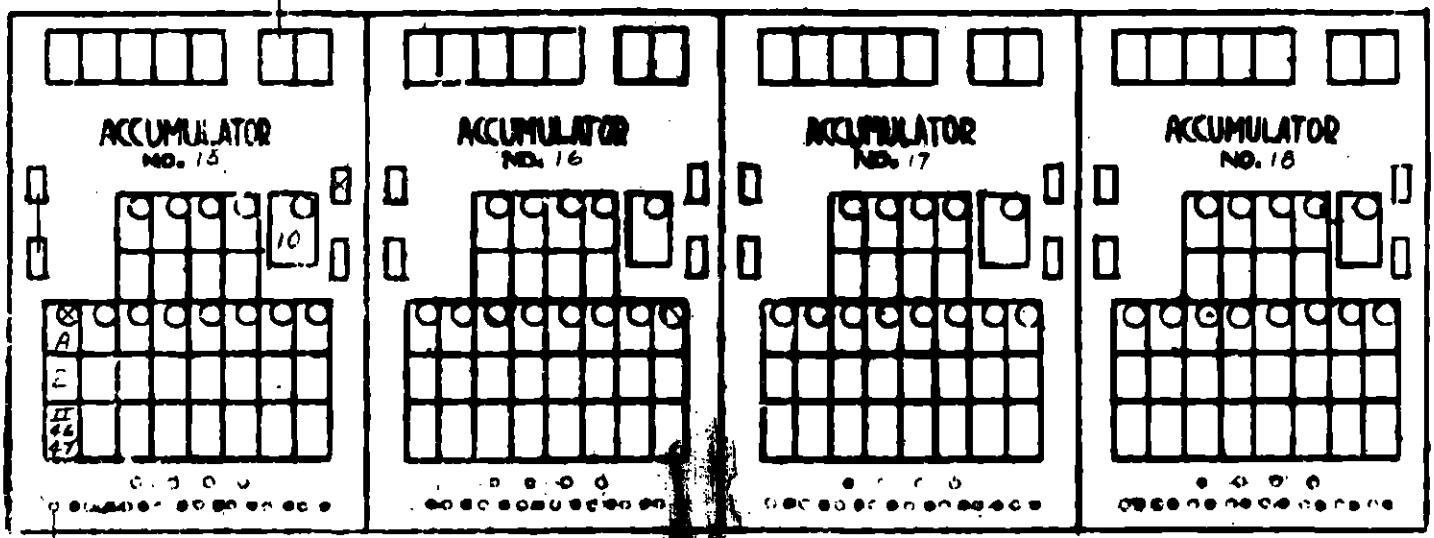
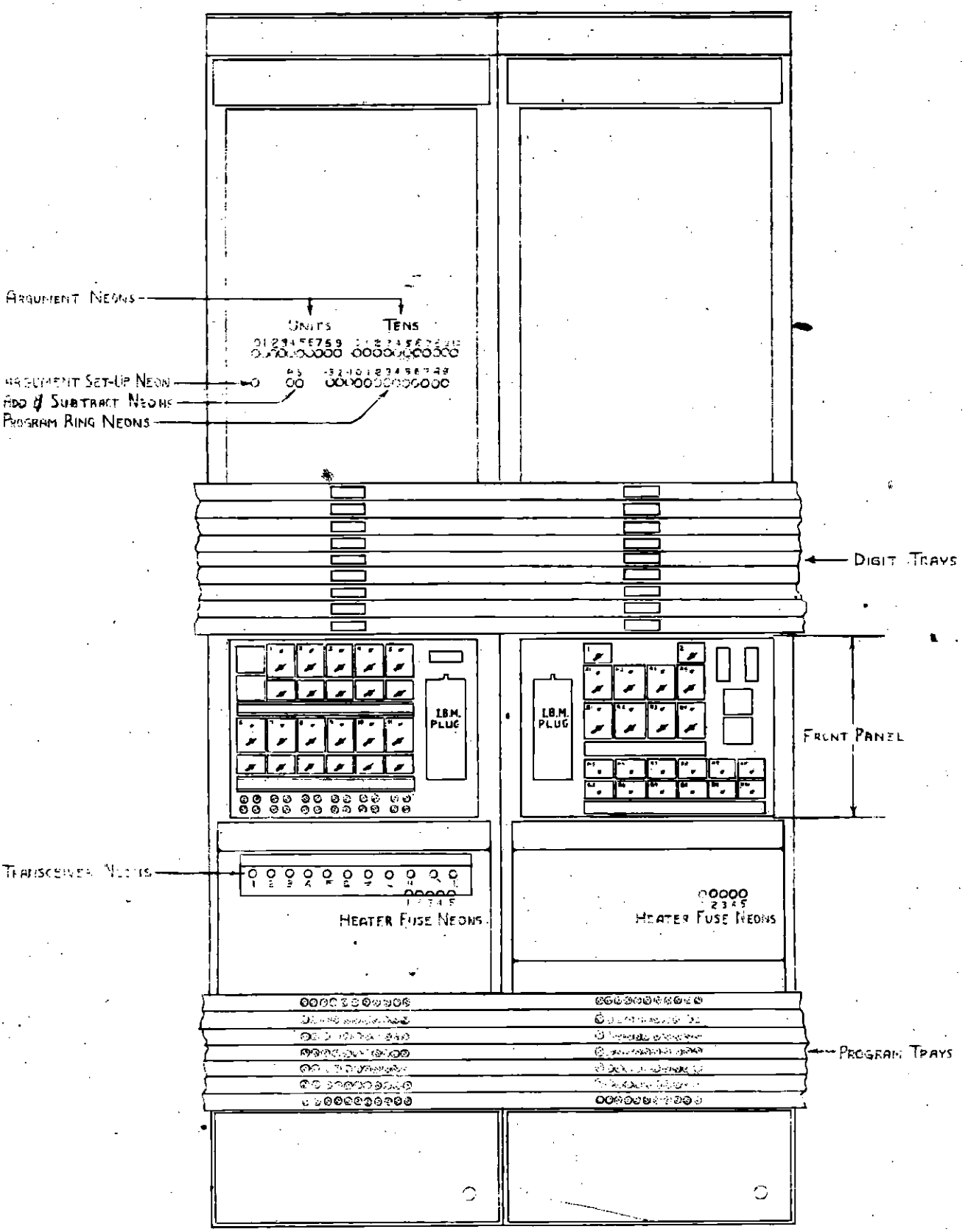


Fig. 6-2 (g)

SET-UP DIAGRAM FOR COMPUTATION OF $\frac{a \sum_{i=1}^{3} x_1^3}{b} + cd$

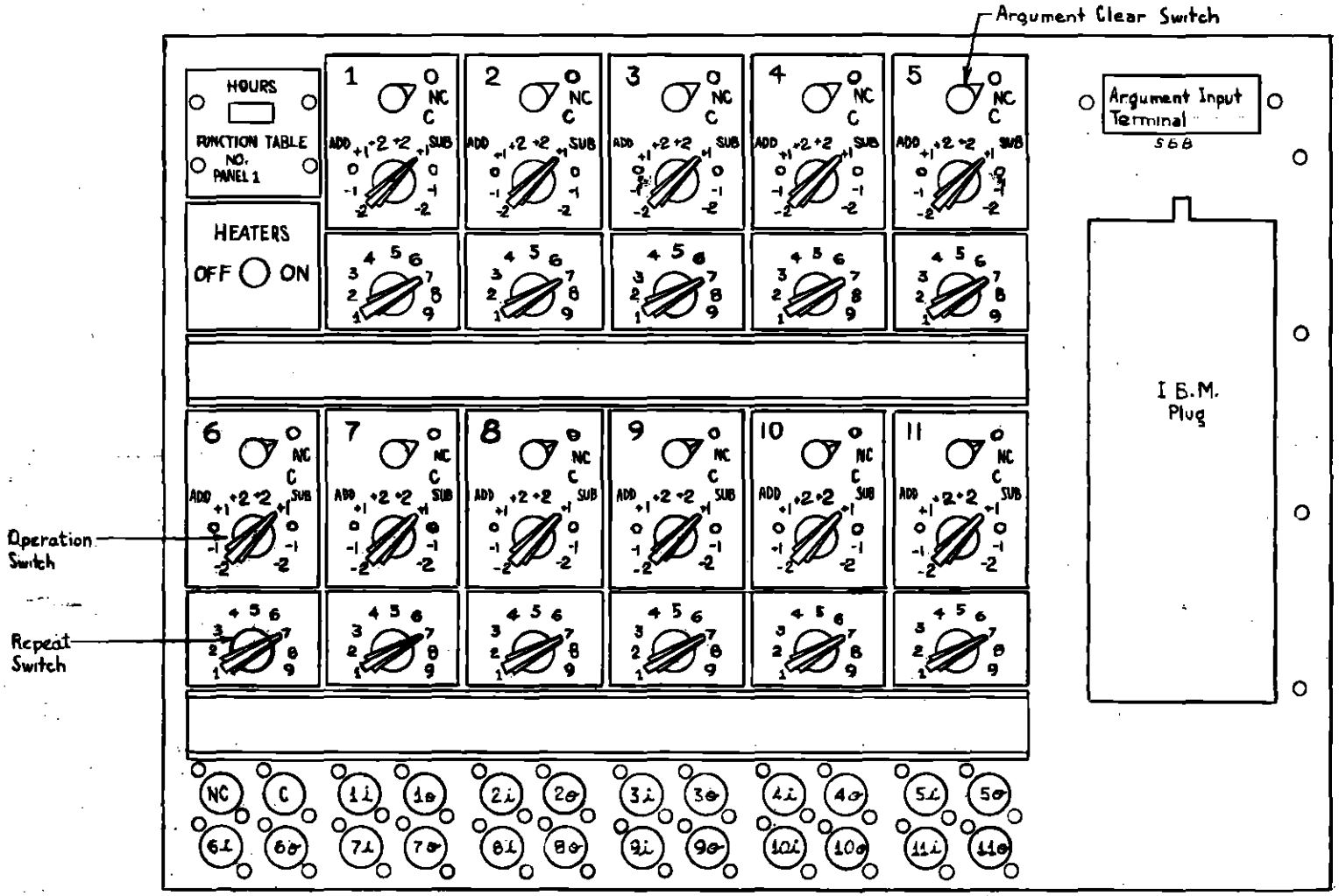
delivered to program control (9) as long as this multiplication program is to be repeated. After the third sequence of two multiplications has been performed, the output of the master programmer is delivered to the interlock pulse input terminal of the divider and square rooter to inform this unit that $2\sum x_i^3$ has been formed and that the division of $2\sqrt{a} + 2\sum x_i^3$ by 2b can take place whenever the divider and square rooter has completed the formation of $2\sqrt{a}$.

When the divider and square rooter has completed the computation of $2\sqrt{a}$ the result is transmitted (during addition time II-1) to accumulator 12 which has been storing $2\sum x_i^3$. In the next addition time, the divider and square rooter commences the division program (set up on program control (2) and the high speed multiplier begins the multiplication of c x d (set up on program control (11)). When the multiplication program is completed, c x d is transferred to accumulator 12 which also receives $\frac{\sqrt{a} + \sum xi^3}{b}$ when the division program is completed. Thus, by the end of addition time III-1, accumulator 12 stores X and emits a program pulse (carried on line 1-7) which can be used to stimulate the next computation sequence if any.



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FUNCTION TABLE
FRONT VIEW
PX-7-305



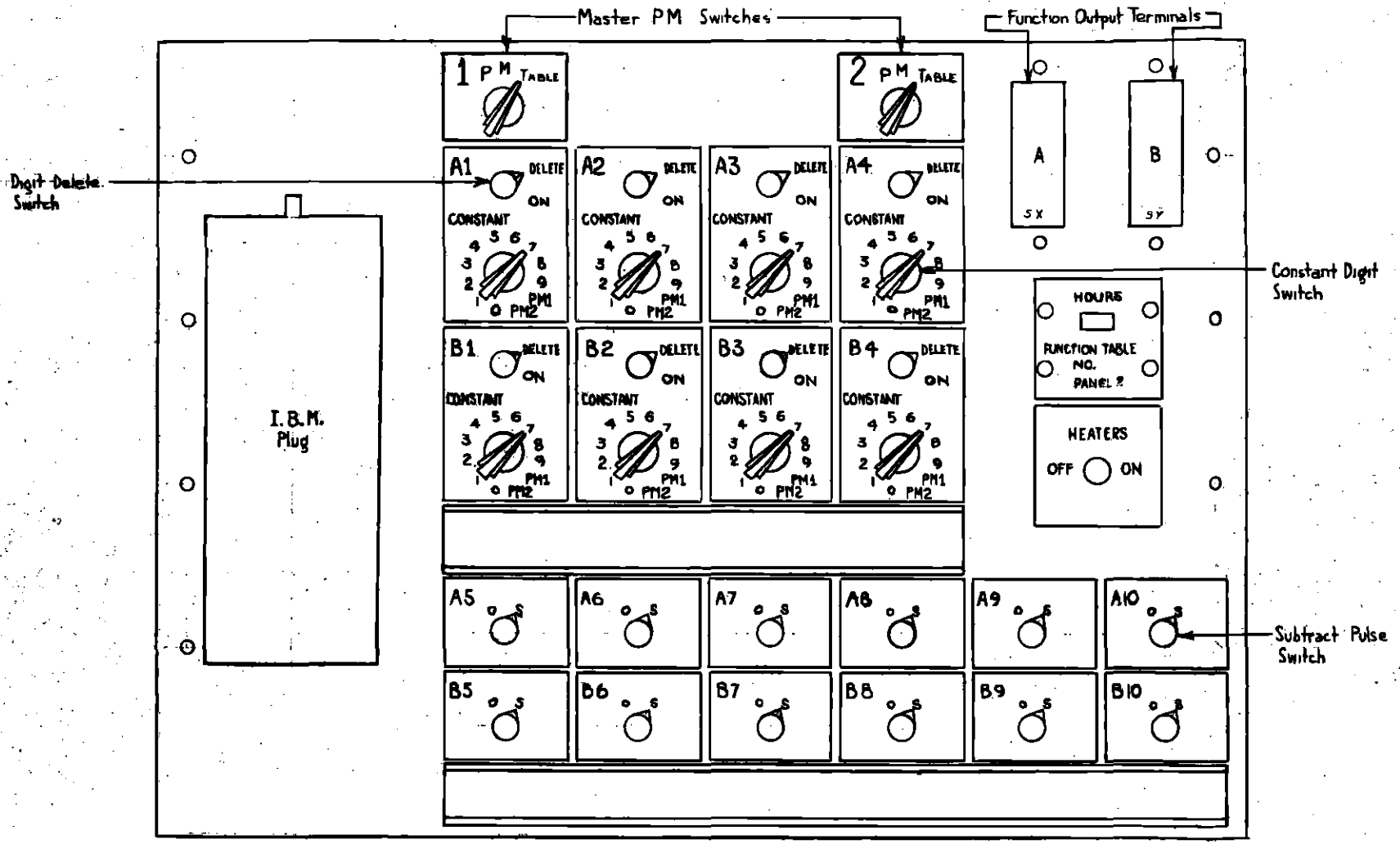
TERMINALS 1i, 2i ---11i
Program input pulse terminals for programs 1-11 respectively.

TERMINALS 1o, 2o ---11o
Program output pulse terminals for programs 1-11 respectively.

TERMINAL NC
Program output pulse terminals associated with NC on argument clear switch.

TERMINAL C
Program output pulse terminals associated with NC on argument clear switch.

FUNCTION TABLE
FRONT PANEL NO. 1
PX-7-302R



FUNCTION TABLE
FRONT PANEL NO.2
PX-7-303 R

VII FUNCTION TABLE

The ENIAC contains three function table units each of which can be used to store values of one or more functions tabulated against an independent variable and can be programmed to look up and transmit the values so stored. The function table is useful not only for storing and selecting values of a function (as the term is ordinarily defined) but also makes it possible to store and have readily available any numerical data which can be tagged with two digit numbers increasing monotonically between 0 and 99. Thus, a function table could be used to store the coefficients and constant terms of a system of simultaneous equations or programmatic information. The function table requires r+4 addition times to look up the value of a function and transmit it repetitively r times.

The following pages will be concerned with: program controls (7.1) common programming circuits (7.2); numerical circuits (7.3); storage of programming information in the function table (7.4); and illustrative problem set-ups (7.5). Reference will be made to the following diagrams:

Function Table Block Diagram	PX-7-304
Function Table Front View	PX-7-305
Function Table Front Panels	PX-7-302, 303

7.0. GENERAL SUMMARY OF THE FUNCTION TABLE

The function table can store 104 entries of one or more functions with each entry associated with an argument between -2 and 101. By an entry is meant 12 digits any one or all of which may vary from entry to entry and

two signs, either variable or constant. In addition, 8 digits, constant throughout the range of the table, may be set up manually on switches.

If a is the argument (where $o \leqq a \leqq 99$) and f (a) is the information stored in the function table line corresponding to value a of the argument, the function table can be programmed to look up f(a-2), f(a-1), f(a), f(a+1), f(a+2), or the complement of any of the preceding and, furthermore, can be programmed to transmit the number looked up repetitively from one to nine times. Four addition times are required for looking up the value of a function and one more addition time is needed for each transmission of the functional value.

The function table can also exert some program control on the accumulator used to store the argument since it is capable of transmitting a program pulse to stimulate the argument accumulator to transmit the argument to the function table and then either to clear or not clear. In addition, the function table is capable of receiving a pulse which will stimulate it to carry out the operations noted above and then, of transmitting a program output pulse.

The physical appearance of the function table can be seen on PX-7-305. The function table has the two panels shown here and in addition, a portable function table (see ENIAC Floor Layout, PX-1-302) which extends into the center of the floor. As its name implies, the portable function table can be moved around and, any of the tables (A, B, C on PX-1-302) can be used with any one of the function tables. The portable function table will be discussed in greater detail in Sec. 7.3.

In its components and method of operation the function table is very much like the high-speed multiplier. The numerical circuits consist of a portable function table (analogous to the multiplication tables), argument counters, argument input gates (analogous to the ier selector gates), table output gates (analogous to the coding gates in the high-speed multiplier), and the 1, 2, 2', 4, and 9P gates.

There is a difference, however, between the high-speed multiplier and the function table in the way in which the argument is fed to the function table. Here, the argument is delivered in pulse form (rather than in the form of static outputs) to the function table where it is set up in the argument counters (a decade ring counter for units place with carry-over to the 11 stage counter used for tens place of the argument). The argument input gates are then set up by the static outputs of the argument counters in the function table.

The function table's numerical circuits also include 8 constant digit switches which have a purpose similar to that of the table output gates except that the former are used only for digits which remain the same throughout the table. A sign which remains constant over the whole table can be set up on one of the two master PM switches. The subtract pulse switches make it possible to transmit the 1'P over the leads for certain places when the function table transmits subtractively so that complements with respect to 10 can be emitted.

The common programming circuits of the function table consist of a 13 stage program ring analagous to the program ring in the high-speed multiplier, the argument correct gates (F-L44) which make it possible to look up

f(a-2), f(a-1), f(a), f(a+1), f(a+2), the add and subtract gates and the flip-flops (C and D 46, 47) they control which make it possible for either the function or its complement to be looked up, and the argument flip-flop which controls the setting up of tens place of the argument in the argument selectors. There are also circuits for clearing the program ring and the argument counters, and for resetting flip-flops. The C and NC transmitters and their output terminals on front panel 1 which can deliver a pulse to the argument accumulators to stimulate transmission of the argument may also be counted among the common programming circuits.

The programming circuits mentioned above can be operated by any one of the function table's eleven program controls. Each program control includes a transceiver with program pulse input and output terminals on front panel 1 correlated with an operation switch, an argument clear switch, and a repeat switch.

The r+4 addition times required for the looking up of a function and its repetitive transmission r times are spent in the following way:

0 Program input pulse is received

1 Function table emits C or NC program output pulse to stimulate transmission of argument.

2 Function table receives digit pulses for the argument.

3 Argument stored in the argument counters of the function table is corrected to the value specified on the operation switch

4 Appropriate line of the portable function table is activated.

5 Functional value is transmitted for the first time.

4+r Functional value is transmitted for the r^{th} time and a program output pulse is emitted after the r^{th} transmission.

7.1. PROGRAM CONTROLS

A pulse received at one of the 11 program input terminals of the function table stimulates the function table to carry out the program set up on the program switches of the control of which that input terminal is a part. Each program control offers the operator options as to:

1) which of five "lines" of the table is to be entered for a given value of the argument,
2) whether the entry tabulated on the specified line or its complement is to be looked up and transmitted,
3) whether or not transmission of the argument to the function table is to be stimulated by the function table,
4) the number of times (from 1 to 9) in succession the function table is to transmit the value looked up.

The function table follows the program instructions set-up on the control in a fashion similar to that discussed previously (see accumulator and high-speed multiplier, for example). A pulse received at an input terminal flips the flip-flop of the transceiver into the abnormal state. As a result, signals from the transceiver (indirectly through inverters and/or buffers) pass through the program switches and then proceed to cause the common program-

ming circuits (see Sec. 7.2.) to operate appropriately. As in units previously discussed, also, the reset signal for the transceiver's flip-flop comes from the unit's program ring and passes through the repeat switch of the control. After the function has been transmitted the number of times indicated by the setting of the repeat switch, the flip-flop is reset and a program output pulse is transmitted.

It is to be noted that the program output pulse is emitted after the function is transmitted. Therefore, the output pulse cannot be used to stimulate an accumulator to receive the function, but a pulse from some other source must be provided for this purpose four addition times after a function table transceiver is stimulated.

Program neons on front panel 1 (see PX-7-305) each correlated with a program control enable the observer to see which program control has been stimulated at a given time and, hence, which program should be in operation.

7.1.1. The Operation Switch

The operation switch has ten possible positions. The five left hand (add) positions are used when it is desired to transmit the value tabulated on a certain line; the five right hand (subtract) positions specify transmission of the complement. If a is the argument received in the function table (where $o \leq a \leq 99$), the setting -2, -1, ..., or 2 respectively specifies that line a-2, a-1, ..., or a+2 of the portable function table is to be entered.

The function table is especially well adapted to interpolation by means of algebraic interpolation polynomials of degree 1, 2, 3, or 4 since, by setting up several program controls, the operator can readily produce functional values for values of the argument surrounding the one for which the

interpolation is being carried out. Interpolation of degree higher than the fourth can also be done. However, in order to obtain several of the entries required for such higher degree interpolation, the argument must be changed before its transmission to the function table. For example, to interpolate by means of the Newton Gregory forward interpolation formula out to sixth differences requires f(a), f(a+1), ..., f(a+6). The entries f(a), f(a+1), f(a+2) can be obtained in succession by using three program controls with operation switches set at 0, 1, 2, and by feeding a to the function table. The remaining entries may be produced by forming a' = a+5 in the accumulator in which the argument is stored and then using program controls set-up to produce f(a'-2), f(a'-1), ..., f(a'+1).

7.1.2. Argument Clear Switch

The argument clear switch can be set at C, NC, or 0. If, on a given program control, the switch is set at C or NC, at the end of the first addition time, a program output pulse is transmitted from the correspondingly labelled terminal on front panel 1 (see PX-7-302). If, the argument clear switch is set at 0, no pulse is transmitted from either the C or NC program pulse output terminals.

The operator can utilize the C or NC pulse to stimulate transmission of the argument to the function table by connecting the C and NC terminals to suitably set up program controls on the argument accumulator or accumulators. If the argument for a given function table is always stored in one accumulator, the C terminal can be connected to a program control on the argument accumulator set up for transmission with clearing and the NC terminal, to a program control set-up for transmission without clearing. If, on the other hand, the

argument for a given function table is stored sometimes in one accumulator and sometimes in another, the operator may find it convenient to use the C pulse to stimulate transmission of the argument from one accumulator and the NC pulse to stimulate transmission from the other argument accumulator.

When the argument clear switch is set at 0, the operator must provide, independently, for a program pulse to stimulate the transmission of the argument to the function table (unless the argument is to be zero). Such a pulse must be delivered to the argument accumulator one addition time after the program pulse which stimulates the function table program control since the argument must be received in the function table during the second addition time of a program.

7.1.3. The Repeat Switch

The purpose and use of the function table repeat switch is the same as that of the accumulator repeat switch. It enables the operator to secure, on any given program, repetitive transmission of the function looked up r times (where $1 \leq r \leq 9$) and causes a program output pulse to be transmitted when the last repetition has been accomplished, r+4 addition times after the reception of a program input pulse.

7.2. COMMON PROGRAMMING CIRCUITS

The device used to clock the advance of the function table through the sequence of suboperations involved in looking up and transmitting a functional value is the program ring counter (usually abbreviated as the program ring). This is a thirteen stage counter with the first stage labelled -3

(see PX-7-304) and the last 9. The program ring neons (shown on PX-7-305) are correlated with the 13 stages of the program ring.

The program ring clears to stage -3 when initial clearing takes place and whenever a function table program is completed. The reception of a program pulse by any transceiver results in opening a gate (D, E, or F49) which allows the ring to receive a CPP each addition time as long as the transceiver's flip-flop remains in the abnormal state. Each CPP then cycles the ring 1 stage. In this section, the program ring and its effect on associated gates and flip-flops are discussed (see Table 7-1 for a summary).

During the first addition time of a function table program (i.e. while the ring is in stage -3), gate J48 is opened so that the next CPP (after the one received by the transceiver) can pass through it and then out through whichever of the gates H(46) or H(47) is open as the result of the setting of the argument clear switch to NC or C respectively. This pulse is the one referred to in Sec. 7.1.2. as the NC or C pulse.

Simultaneous with the transmission of the C or NC pulse, the program ring cycles to stage -2. During this addition time, the second of the program, a signal from stage -2, opens gates D42 and H42, the gates to the units and tens place argument counters to allow the argument to be received in the argument counters.

In the third addition time a signal from stage -1 allows 0, 1, 2, or 3 (depending on the setting of the operation switch) pulses to pass through gate E42 and be delivered to the argument counters so as to correct the argument to the value specified by the operation switch setting (see Sec. 7.3.2.) During this addition time, too, gate F47 is open so that the 1' pulse trans-

TABLE 7-1

CHRONOLOGICAL OPERATION OF THE FUNCTION TABLE'S PROGRAMMING CIRCUITS

Add. Time	Stage of Program Ring	EVENT
End of 0	-3	1) Program input pulse is received
1	-3	1) Signal from stage -3 gates CPP through gate J48. Output of gate J48 gated through gate H46 or gate H47 by normally positive output of transceiver's flip-flop is emitted as C or NC pulse. 2) CPP gated through D, E, or F49 cycles program ring to stage -2.
2	-2	1) Signal from stage -2 opens gates D and H42 so that argument can be received in argument counters. 2) Program ring cycles to stage -1.
3	-1	1) Signal from stage -1 opens gate E42 to allow the argument correct pulses to pass through to the argument counter for units place. 2) Signal from stage -1 gates 1'P through gate F47. Output of gate F47 sets argument flip-flop. 3) Program ring cycles to stage 0.
4	0	1) Signal from stage 0 gates CPP through gate G48. Output of gate G48 gated through gate E47 or gate E46 by normally negative output of transceiver's flip-flop sets Add or Subtract flip-flop respectively. 2) Program ring cycles to stage 1
5	1	1) Signal from A or S flip-flop in the abnormal state allows 1, 2, 2', 4 and 9P to pass through certain of the pulse gates to provide the function table with the pulses for the functional value. 2) Program ring cycles to stage 2 unless the repeat switch is set at 1.
. . .	. . .	. . .
4 + r	r	1) Functional value is transmitted for the r^{th} time. 2) Signal from stage r of the program ring passes through point r on the repeat switch to gate 62 in the transceiver. Signal emitted by gate 62 gates CPP through gate 68 to provide a reset signal for the transceiver and a program output pulse. 3) The signal from gate 62 also gates a CPP through gate C48 to provide a reset signal for flip-flops B, C, and D46-47 and gates a CPP through gate B48 and gate A48 which clears the program ring to stage -3 and the argument counters to zero.

mitted in this addition time is allowed to pass and thus to flip flip-flop B46--47 into the abnormal state. This provides a negative signal to turn off the tubes marked B11 and B, C, .., L1 and thus to allow the argument input gates to set up in accordance with the number registered in the argument counters. Flip-flop B46-47 is referred to as the argument flip-flop and its operation is correlated with the argument neon on front panel 1 (see PX-7-305).

During the fourth addition time the argument selector gates finish setting up. In this time, too, a signal from stage zero, opens G48 so that the next CPP can be passed through it (at the time of the fourth CPP after the one received by the transceiver). The pulse passed through gate G48 then passes through gate E46 or E47 (E46 is open if the operation switch is set at a subtract point; E47 is open if the operation switch is set at an add point) thus (in the fifth addition time) flipping the subtract or add flip-flop respectively into the abnormal state. The subtract and add flip-flops control the transmission of the complement of a function and the function respectively (see Sec. 7.4.). These two flip-flops are correlated with the add and subtract neons on PX-7-305.

In the fifth addition time the program ring is on stage 1. In this addition time and in every subsequent one until the transceiver's flip-flop is reset, the functional value which has been looked up is transmitted. The stages from 1 to 9 of the program ring are correlated with the points 1-9 respectively on the repeat switch. When the program ring reaches stage r, the number set up on the repeat switch, a signal from stage r passes through the repeat switch and opens the transceiver's reset gate (62). This results

in the activation of the function table's clear circuits so that the ring is cleared to stage -3, the argument counters are cleared to zero, and the three programming flip-flops mentioned above are reset by the next CPP. The opening of the reset gate also results in allowing the next CPP (i.e. the (4+)th after the one that stimulated the program control) to pass through gate 68 and then to reset the transceiver's flip-flop and to be transmitted as a program output pulse.

7.3. NUMERICAL CIRCUITS

7.3.1. Storage: Portable Function Table, Master PM Switches, Digit Delete and Constant Digit Switches, Subtract Pulse Switches.

The function table can be set up to store 104 entries each consisting of 20 digits, and 2 signs. Twelve of the digits, variable from entry to entry, are tabulated on the switches of the portable function table. The remaining 8 digits must be constant throughout the range of the argument. These are set up on the constant digit switches. The signs may be either variable or constant. Function output terminals A and B on panel 2 are each responsible for the transmission of a sign, 4 constant digits, and 6 variable digits (see Table 7-2). Whenever the function table is stimulated, information is emitted simultaneously through both function output terminals.

The function table permits great flexibility in the way in which it is set up and used. One sign and as many as 20 digits may sometimes be used for a single function. The 2 PM's, one with k and the other with 20-k (where $0 \leq k \leq 20$) digits, can be used for 2 functions. As a matter of fact, more than 2 signed functions can be stored by setting up numbers zero and nine for sign

indication P and M respectively on switches ordinarily used for digits provided that these switches are not required for digits. Of course, in cases where the digits for a single function are transmitted through both function output terminals, it may be necessary to use adaptors, shifters and/or deleters in order to receive the functional value properly lined up in another unit.

The portable function table is arranged with 26 rows and 28 columns of switches on each of its 2 faces. Each face, thus, has the switches for 52 entries with the 14 columns of switches for 26 entries appearing on the left half of the face and, those for the succeeding 26 entries on the right half. The sign and 6 digits set up on the first 7 switches (at the left) are emitted over terminal A; the next 6 digits and sign, over terminal B (see Table 7-2). Positive functional values are set up with sign P and the digits for the absolute value of the function. Negative values are set up as complements, i.e. with sign M and the digits for the absolute value subtracted from some power of 10.

The adjective "variable" is used to describe the type of function table discussed above in which the values of the function are set up manually on switches and which, with changed switch settings, can be used for storing different functions on different occasions. At present, one variable type is used with each function table unit. As the need arises, portable function tables of the fixed type in which the pattern of connections is permanently wired can be constructed and used in place of the fixed type. Such a permanent table would have the advantages of always being available for use without the necessity for tearing down a function already set up on switches, of being less expensive to build, and of being considerably smaller in size than the variable type.

Master PM switches 1 and 2 on panel 2 (see PX-7-303) of the function

TABLE 7-2

FUNCTION OUTPUT TERMINAL LEADS AND ASSOCIATED SWITCHES

Lead	Associated Switches for Terminal A		Associated Switches for Terminal B	
PM	Master PM Switch 1 and Portable Function Table Switch in Column 1		Master PM Switch 2 and Portable Function Table Switch in Column 14	
10	Constant Digit and Digit Delete Switches A4		Constant Digit and Digit Delete Switches B4	
9	Constant Digit and Digit Delete Switches A3		Constant Digit and Digit Delete Switches B3	
8	Constant Digit and Digit Delete Switches A2		Constant Digit and Digit Delete Switches B2	
7	Constant Digit and Digit Delete Switches A1		Constant Digit and Digit Delete Switches B1	
6	Portable Function Table Switch in Column 2	Subtract Pulse Switch A10	Portable Function Table Switch in Column 8	Subtract Pulse Switch B10
5	Portable Function Table Switch in Column 3	Subtract Pulse Switch A9	Portable Function Table Switch in Column 9	Subtract Pulse Switch B9
4	Portable Function Table Switch in Column 4	Subtract Pulse Switch A8	Portable Function Table Switch in Column 10	Subtract Pulse Switch B8
3	Portable Function Table Switch in Column 5	Subtract Pulse Switch A7	Portable Function Table Switch in Column 11	Subtract Pulse Switch B7
2	Portable Function Table Switch in Column 6	Subtract Pulse Switch A6	Portable Function Table Switch in Column 12	Subtract Pulse Switch B6
1	Portable Function Table Switch in Column 7	Subtract Pulse Switch A5	Portable Function Table Switch in Column 13	Subtract Pulse Switch B5

table are associated with the PM leads of terminals A and B respectively. These switches have the positions P, M, and Table. If the sign to be emitted over one of the terminals is constant throughout the range of the table, this constant sign may be set up on the associated master PM switch instead of on the 104 PM switches of the portable function table. For a sign varying from entry to entry however, the appropriate sign is tabulated in the PM column of the portable function table with each entry and the corresponding master PM switch is set at Table.

For each of the 8 decade places which can be filled with a constant digit, there is a digit delete switch with the positions "delete" and "on" and an associated constant digit switch with the positions 0, 1, ..., 9, PM1, and PM2. (See Table 7-2 for the decade place leads associated with these switches.)

With a digit delete switch set at delete, no pulses are transmitted over the decade place lead associated with the delete switch. With a delete switch set at on and the associated digit switch at d (where $0 \leq d \leq 9$), d or 9-d pulses are transmitted over the correlated decade place lead according as additive or subtractive transmission respectively takes place. With a digit delete switch set at "on" and the associated constant digit switch set at PM1 or PM2 the sign pulses emitted respectively over the sign lead of the A or B function output terminals are duplicated on the correlated decade place lead. This is true whether the pulses emitted over the sign lead are those specified on a portable function table PM switch or on the master PM switch.

When the function output of a terminal is to be received in an accumulator with the variable digits in decade places at the right and with no other information provided for b (where $1 \leq b \leq 4$) decade places at the left (such as

constant digits or digits from another function output terminals), and when some or all function values emitted may be negative, the PM1 or PM2 setting of b of the constant digit switch provides a means of filling these decade places at the left with the nines needed to represent a negative number. If all entries associated with a function output terminal are tabulated as either positive or negative numbers (i.e. with the master PM switch set at P or M), the same end may be achieved by setting b constant digit switches at 0 or at 9 respectively. (See Table 7-3 which follows the discussion of the subtract pulse switches).

The digit delete switch correlated with a decade place lead is set at delete when it is desired to leave a decade place completely blank as is required, for example, if a variable digit from another function output terminal is to be inserted in that place.

The subtract pulse switches A and B 5-10 have the positions 0 and S. If a subtract pulse switch is set at S, when subtractive transmission takes place (see Sec. 7.3.3.), the 1'P is emitted over the decade place lead associated with the switch (see Table 7-2) to make a 10's instead of a 9's complement. Complements with respect to 9 are emitted in the decade place leads associated with subtract pulse switches which are set at 0 (see Sec. 7.3.3.). In the usual applications of the function table, at most one of the A and/or one of the B subtract pulse switches would be set at S. There is, however, nothing in the design of this unit to preclude setting a greater number of these switches at S if the operator so desires.

7.3.2. Input to the Portable Function Table: Argument Counters and Table Input Gates.

During the second addition time of a program, the argument is received

TABLE 7-3

ILLUSTRATIONS OF THE USE OF SWITCHES ON PANEL 2 OF THE FUNCTION TABLE

LINE	SETTING OF PORTABLE FUNCTION TABLE SWITCHES
x	P 123 000 795 642 M
x + 1	M 764 000 421 508 M

EXAMPLE 1

Setting of Constant Digit Switches: (All Digit Delete Switches set at "On".)

A4 at PM1	B4 at PM2
A3 at PM1	B3 at PM2
A2 at PM1	B2 at PM2
A1 at 3	B1 at PM2

Subtract Pulse Switches: A8 at S B5 at S (all others at 0)

Transmit	For Argument	Number Emitted	
		Over Terminal A	Over Terminal B
Add.	x	P 0 003 123 000	M 9 999 795 642
Add.	x+1	M 9 993 764 000	M 9 999 421 508
Sub.	x	M 9 996 877 999	P 0 000 204 358
Sub.	x+1	P 0 006 236 999	P 0 000 578 492

EXAMPLE 2

Setting of Constant Digit Switches:

A3 at 0	B4 at 9
A2 at 0	B3 at 9
A1 at 0	B2 at 9
	B1 at 9

Digit Delete Switch A4 set at "Delete" (all others set at "On").
All Subtract Pulse Switches set at 0.

Transmit	For argument	Number Emitted	
		Over Terminal A	Over Terminal B
Add.	x	P 0 000 123 000	M 9 999 795 642
Add.	x+1	M 0 000 764 000	M 9 999 421 508
Sub.	x	M 0 999 876 999	P 0 000 204 357
Sub.	x+1	P 0 999 235 999	P 0 000 578 491

in the function table's argument counters through the argument input terminal on front panel 1*. This terminal is so wired that UNITS AND TENS PLACE OF THE ARGUMENT MUST BE RECEIVED IN THE FUNCTION TABLE ON THE LEADS FOR THE DECADE PLACES 1 AND 2 RESPECTIVELY. This may be provided for by placing a shifter at the argument input terminal if arguments delivered to the function table will always require shifting the same number of places or, if at various times there will be different shifting requirements, by placing shifters at the argument accumulator's digit input terminals. The units and tens argument neons on front panel 1 are correlated with the stages of the argument counters as indicated on PX-7-305.

In the third addition time, the argument stored in the argument counters is corrected by from 0 to 4 pulses chosen from the 1, 2, and 2' pulses in accordance with the operation switch setting. The argument counters are so connected to the argument or table input gates that if x is the number registered in the argument counters, the table input gate for argument x-2 sets up (during the set up period from the middle of the third addition time through the fourth). Therefore, if the operation switch is set at -2 no correction pulses are added to the argument counters; if the operation switch is set at -1, one pulse is added to the number set up in the argument counters, etc.

The table input gates consist of 104 gates (each connected to a line of the portable function table corresponding to a value of the argument between -2 and 101). Each table input gate has as one of its inputs a signal from a stage of the units argument counter and as its other input a signal from a stage of the tens counter. When the argument counters receive the argument a from the argument accumulator and the operation switch of the control which has been

*The argument input terminal on the function table, like the digit terminals on accumulators, has 12 points. Only the leads for units and tens place, however, are operative.

stimulated is set at i (i = -2, -1, ..., +2), table input gate a + i emits a signal to line a + i of the portable function table.

7.3.3. Function Output

The functional values transmitted from the A and B output terminals on panel 2 are compounded out of the 1, 2, 2', 4, and 9P. These pulses are admitted to the function table through the 1, 2, 2', 4, and 9P gates. The pulses passed through these gates are delivered to the table output gates, the constant digit switches, and the master PM switches. The gates and switches mentioned above allow appropriate numbers of pulses to reach the A and B output circuits which include standard transmitters (see PX-7-304) and the digit output terminals on front panel 2.

7.3.3.1. Transmission of Information Stored on Portable Function Table Switches.

Associated with each of the 12 digit columns of the portable function table is a column* of table output gates for digits. Each of these columns has 10 gates, one for each digit from zero to 9 inclusive. A pair of PM table output gates, one for sign P and one for sign M, is associated with each of the 2 sign columns.

One input to the table output gates for digits comes from the circuits containing the 1, 2, 2', 4, and 9P gates. These latter gates are so controlled by the add. and sub. flip-flops (see Sec. 7.2.) and so connected to the table output gates that when additive transmission takes place (and the add. flip-flop is, thus, in the abnormal state), d pulses reach the table output gates corresponding to digit d; when subtractive transmission takes place (and the sub. flip-flop

*The block diagram of the function table shows the table output gates rotated by 90° from their actual position in the function table where they are arranged in rows. Refer to the cross section diagram for the position in the function table itself.

is, thus, in the abnormal state), 9-d pulses reach the table output gates corresponding to digit d.

The signal from the table input gate corresponding to argument a+i, routed through the 12 digit switches on line a+i, holds open the table output gates corresponding to the digits set up on the line so that the pulses delivered to these gates from the 1, 2, 2', 4, and 9P gates can pass through.

The transmission of sign indication stored in the sign columns of the portable function table is accomplished similarly. The table output gate connected to point P on the sign switches receives 0 or 9 pulses from the 9P gate and the output gate connected to point M receives 9 or 0 pulses from the 9P gate according as the add or subtract flip-flop is in the abnormal state. The pulses passed by one of the pair of table output gates for sign are routed through "Table" on the associated master PM switch to be emitted over one of the PM leads.

With a master PM switch set at P or M (instead of table) the sign pulses emitted by one of the table output gates for sign cannot reach the output circuit. The transmission of a constant sign set up on one of the master PM switches takes place in the following manner: The same number of pulses are delivered to the points P and M respectively on the master PM switches as are delivered to the table output gates associated with digits 0 and 9. Thus, if a master PM switch is set at P, zero or nine pulses are passed through this switch to the associated function output terminal's PM lead according as additive or subtractive transmission takes place. The case where a master PM switch is set at M is taken care of similarly.

7.3.3.2. Transmission of Information Stored on Constant Digit Switches.

The 1, 2, 2', 4, and 9P gates deliver d pulses (in additive transmission) or 9-d pulses (in subtractive transmission) to the point d (where $0 \leq d \leq 9$) on a constant digit switch. Thus, if one of these switches is set at d, d or 9-d pulses pass through it, then through the correlated digit delete switch to the associated decade place lead of a function output terminal.

The points PM1 and PM2 receive the pulses passed by master PM switches 1 and 2 respectively. In this way, a constant digit switch allows the same number of pulses as are transmitted over one of the PM leads to reach the decade place lead associated with the constant digit switch.

If a digit delete switch is set at "delete", the circuit from the correlated constant digit switch to the associated decade place lead is interrupted so that the pulses which arrive at the constant digit switch from the 1, 2, 2', 4, and 9P gates or from the master PM switch cannot reach the function output terminals.

7.3.3.3. Role of the Subtract Pulse Switches

The subtract flip-flop controls the gates A' and B' 64 so that these gates open to pass the 1'P when subtractive transmission takes place. The output of gates A' and B' 64 is routed through the subtract pulse switches set at S to the associated decade place leads of the function output terminals.

7.4. STORAGE OF PROGRAMMING DATA BY MEANS OF THE FUNCTION TABLE

When only a part of a total function table storage capacity (3744 variable digits and 624 variable signs for the 3 function tables) is required for the tabulation of numerical data, the remaining storage capacity can be used as

memory for programming instructions. This can be done either with a function table operating in the same way as described in Sec. 7.3. when numerical functions are stored and transmitted or, more conveniently, with a small change in the circuits containing the 1, 2, 2', 4, and 9P gates.

First, let us consider the use of the unmodified function table for programming memory. Suppose there are, say, 14 different programs (P_1 - P_{14}) one or more of which are to be stimulated at various times in a computation. We could then assign one column on a portable function table to each of the 14 programs and assign one line of the portable function table to each occasion on which it is necessary to make a choice as to which of the 14 programs is or are to be stimulated. Then the switches on a given line of the portable function table are set at P or 0 in the columns corresponding to programs which are not to be stimulated and at M or a number different from zero in the columns corresponding to programs which are to be stimulated. An accumulator is set aside to store the argument for the function table.

Now, when choice of program is required, a program pulse is sent to a function table program control set up for additive transmission. In the fifth addition time following the program input pulse, digit pulses are emitted over function output terminals in the decade place leads corresponding to switch settings different from P or zero. At the end of the fifth addition time a program output pulse is emitted. The digit pulses are taken through adaptors at the function output terminals to lines in program trays and then to dummy programs for conversion to program pulses. The program output pulses of the dummy programs are taken to the program controls on which are set up those of the 14 programs which are to be stimulated (see Fig. 7-1). The function table's program output

Argument	Switch Settings on Portable Function Table Refer to Program														Interpretation
	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P_8	P_9	P_{10}	P_{11}	P_{12}	P_{13}	P_{14}	
-2	M	0	0	0	0	0	0	0	0	0	0	0	0	P	Stimulate program P_1
-1	M	9	0	0	0	0	0	0	0	0	0	0	0	P	Stimulate programs P_1 and P_2
0	P	0	9	0	9	0	0	0	0	0	0	0	0	M	Stimulate programs P_3, P_5 and P_{14}
etc.															

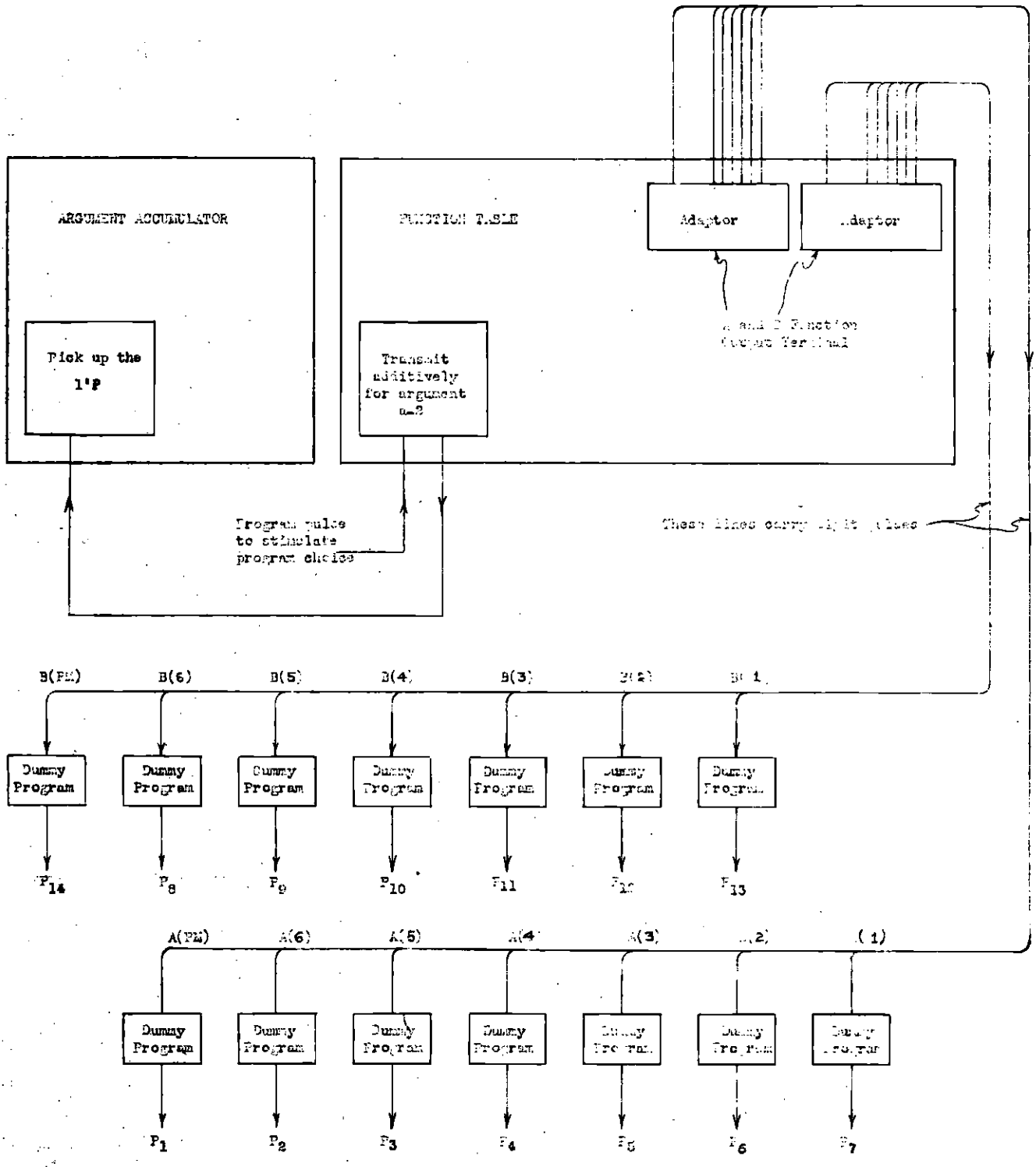


Figure 7-1

USE OF UNENCIPHERED FUNCTION TABLE TO STORE PROGRAMMING INFORMATION

pulse can be taken to a program control of the accumulator containing the argument which is set-up for a "receive -C" program in order to increase the value of the argument by one.

In the example shown on Fig. 7-1, all 14 columns of switches on a program table are devoted to the storage of programming information. With the function table in its unmodified form, however, there is no reason why some of the columns cannot be used for numerical data and others for programming data (see Sec. 7.5.3.).

The disadvantage inherent in using the function table in its unmodified form to store programming information is the necessity for expending dummy programs to convert the digit pulses emitted from the function output terminals into program pulses (see Sec. 4.5.2.). With only a small amount of labor the function table can be adapted so that program pulses are transmitted from the function output terminals instead of digit pulses. The simplest way to make this change is to disconnect the 9P gates (B' and L'4) from the line in the synchronizing trunk which carries the 9P and to connect these gates, instead, to the line which carries the CPP. This may be done by means of an adaptor at the point where the synchronizing cable plugs into the back of panel 2. No wiring changes are necessary. The required adaptor is shown on PX-4-119. If this change is made, when the function table transmits additively, a CPP is emitted over the decade place leads corresponding to portable function table (or even constant digit switches) set at either M or 9. Notice, these CPP are emitted from the function table at the end of the fifth addition time. As always, no pulse of any kind is emitted over a decade place lead whose corresponding switch is set at P or 0. In this way, the necessity for converting digit pulses into program

pulses is obviated. The pulses emitted from the function output terminals can be taken directly to the program controls on which are set up the various programs among which a choice is made.

It should be noted that a numerical function cannot be set-up alongside of programming data on a given portable function table when this modification is made unless the function is pathologic to the extent that its tabulated values never have the digit 9 or sign M.

The use of a modified function table to store programming information is illustrated in the problem described in Sec. 8.7.

In connection with this discussion of the role of the function table as programming memory, mention might also be made of the fact that the function table's program controls provide a convenient way of delaying a program pulse from 5 to 13 addition times. This use of the function table is also involved in the illustrative problem of Sec. 8.7.

7.5. ILLUSTRATIVE EXAMPLES OF THE USE OF THE FUNCTION TABLE IN INTERPOLATION

The function tables have been designed so as to make them particularly well suited for interpolation. One or more function tables or parts of them can be used to store the values of a function. The coefficients of the various terms of the interpolation formula used may either be stored in a function table or may be generated as needed by means of accumulators and the high speed multiplier. Various types of interpolation formulas can be employed with ease. There seems, however, to be a small advantage in using the Lagrangian formulas which involve functional values rather than formulas which involve differences since a pair of accumulators must always be tied up to find a difference unless storage space

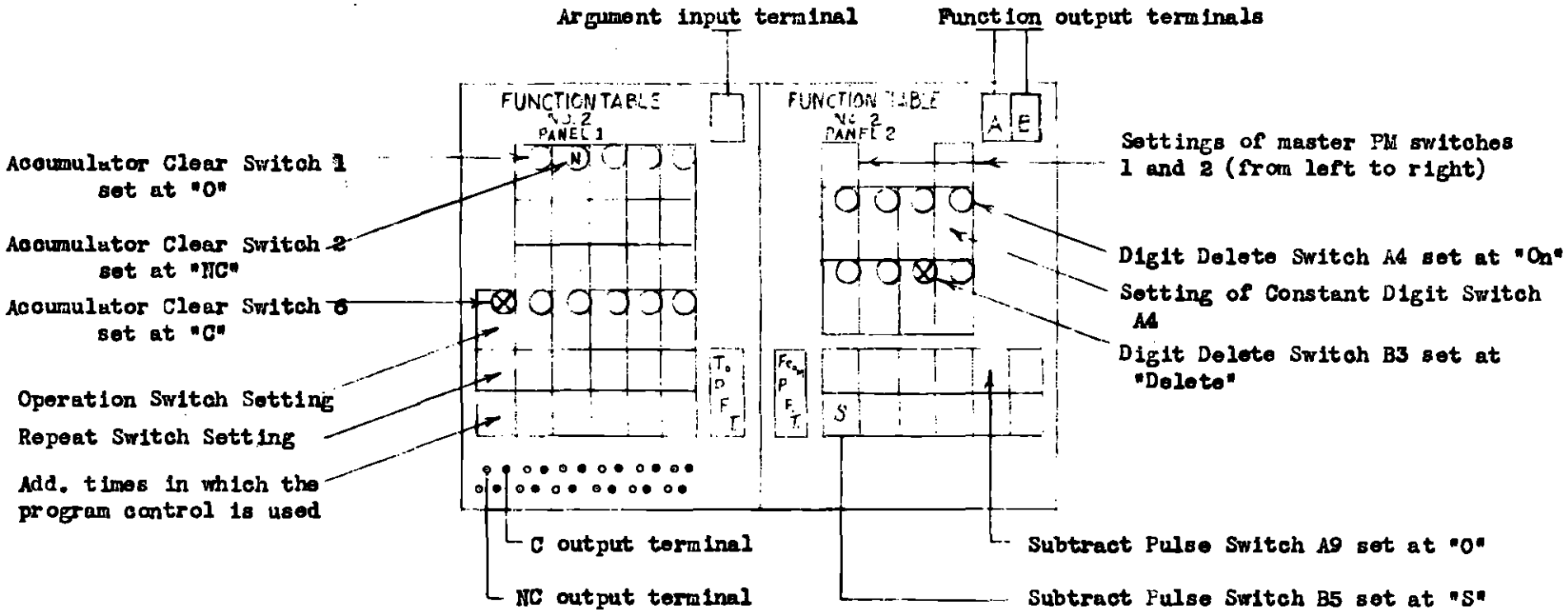


Figure 7-2

SET-UP DIAGRAM CONVENTIONS FOR THE FUNCTION TABLE

in the function table is used for the tabulation of differences.

In set-up tables, the following symbols are used for the function table:

1) On the first level i-j refers to the program input pulse, and (k) to the program control number.
2) On the second level,

   1st symbol (A or S) followed by a signed number (-2, -1, ..., or +2) is the operation switch setting.

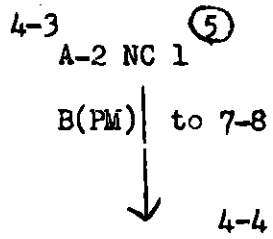
   2nd symbol (C, NC, or O) is argument clear switch setting.

   3rd symbol (1, 2, ..., or 9) is repeat switch setting.

3) On the third level, at the right of the arrow tip i-j refers to the program output pulse.

When the function table is used for the storage of programming information, the connections from the decade place leads of the function output terminals to program lines are noted along the arrow from the second to the third level.

Thus, the symbol



is interpreted as follows: The program pulse carried on lines 4-3 stimulates program control 5 so that the function table transmits f(a-2) once. The NC pulse stimulates transmission of the argument. Program control 5 emits a program output pulse to line 4-4. The output of the PM lead of function output terminal B is taken through an adaptor to program line 7-8.

Figure 7-2 shows the conventions used for the function table in set-up diagrams.

PX-7-033a

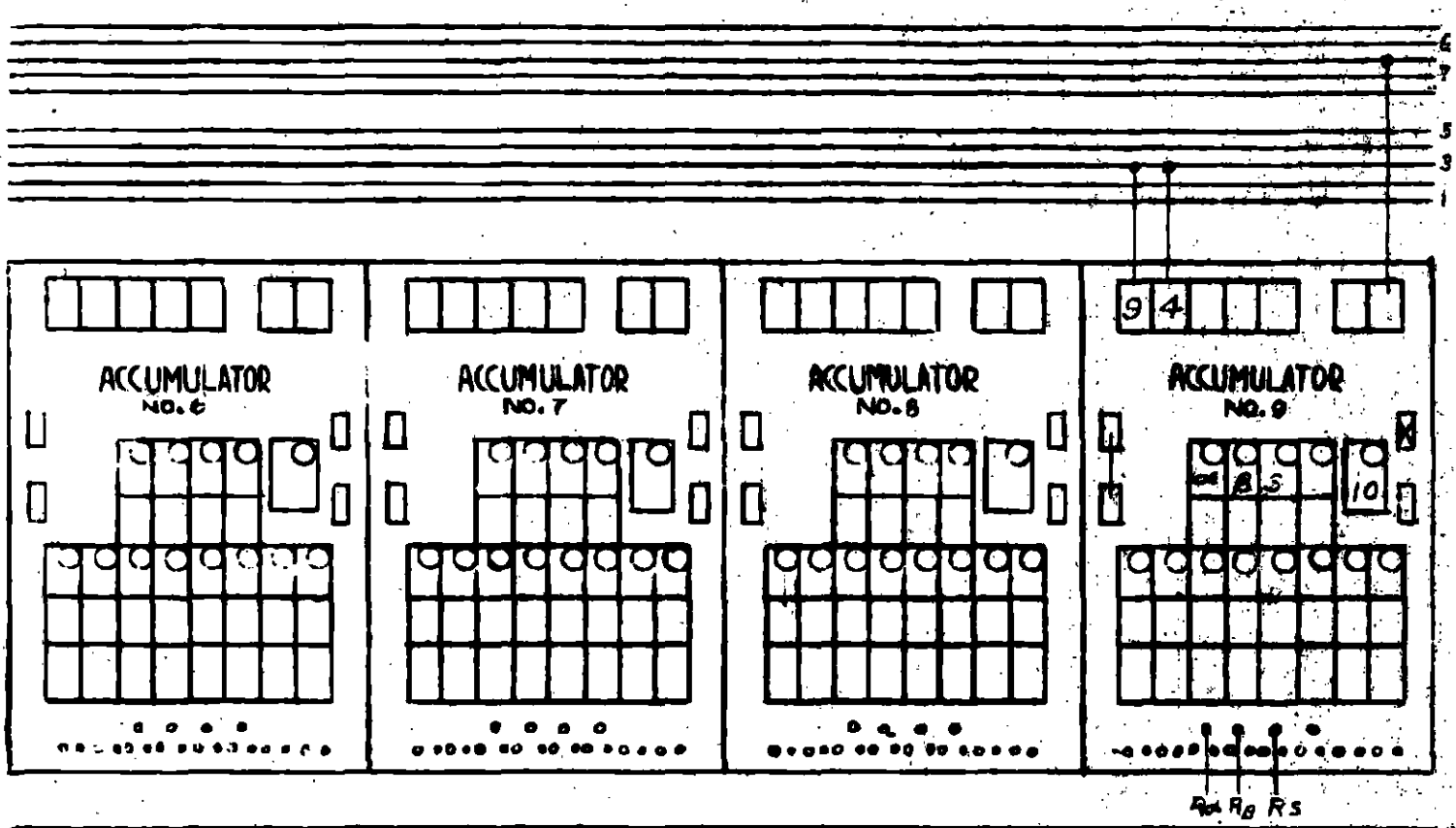


Fig. 7-3 (a)

Quadratic Lagrangian Interpolation – Set-Up Diagram

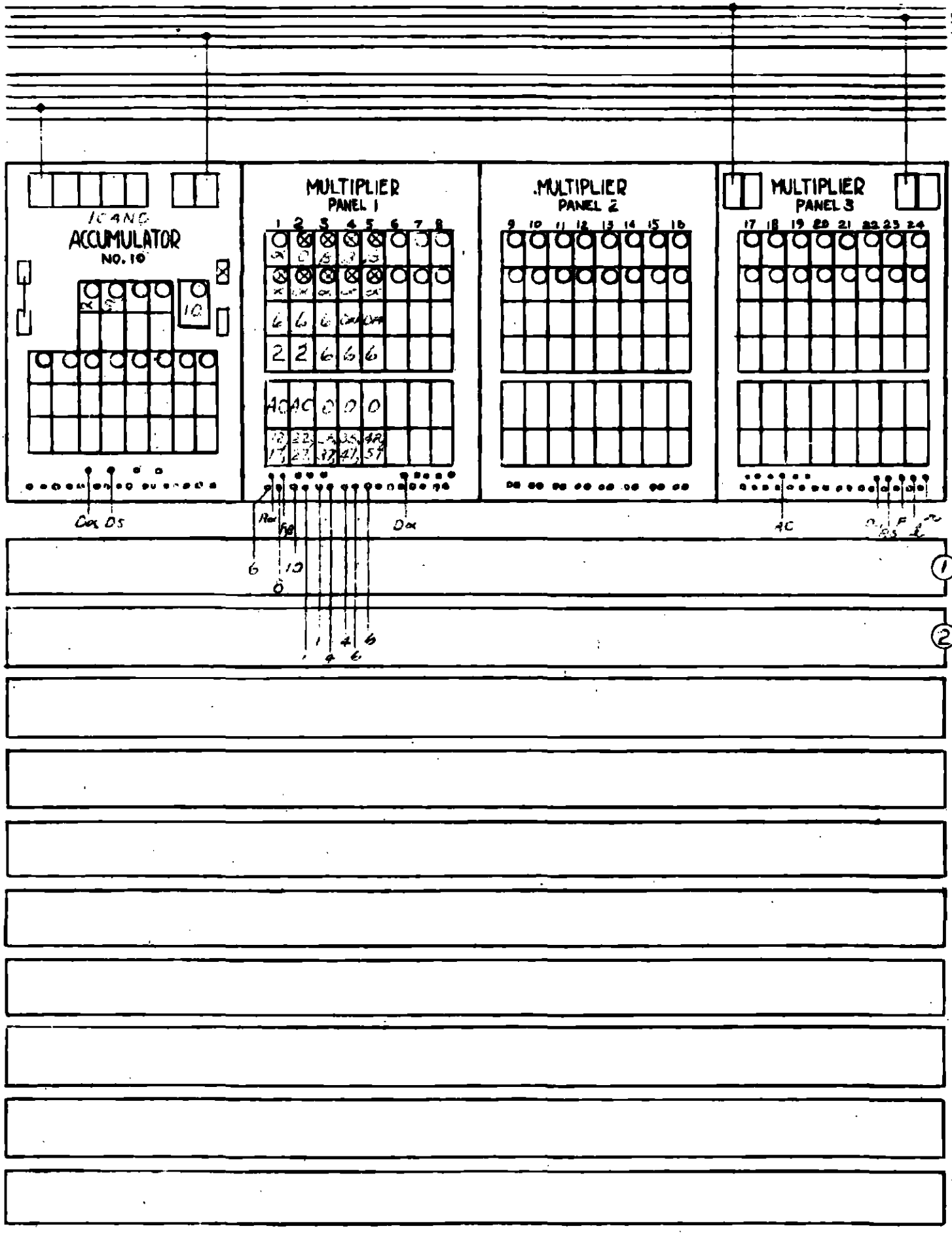


Fig. 7.3 (b)

Quadratic Lagrangian Interpolation - Set-Up Diagram

PX-7 403c

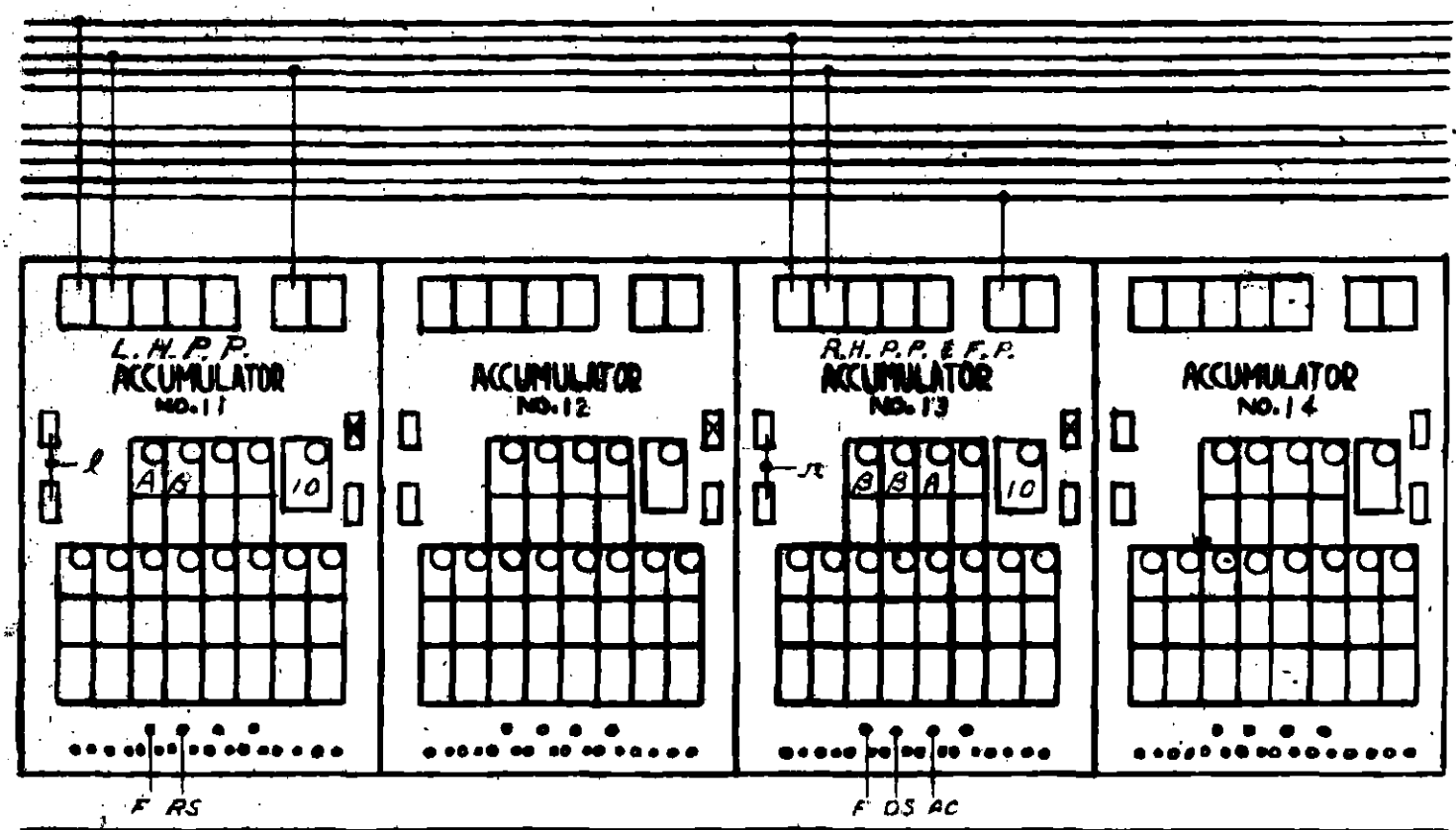


Fig. 7-3 (c)

Quadratic Lagrangian Interpolation – Set-Up Diagram

PX - 4034

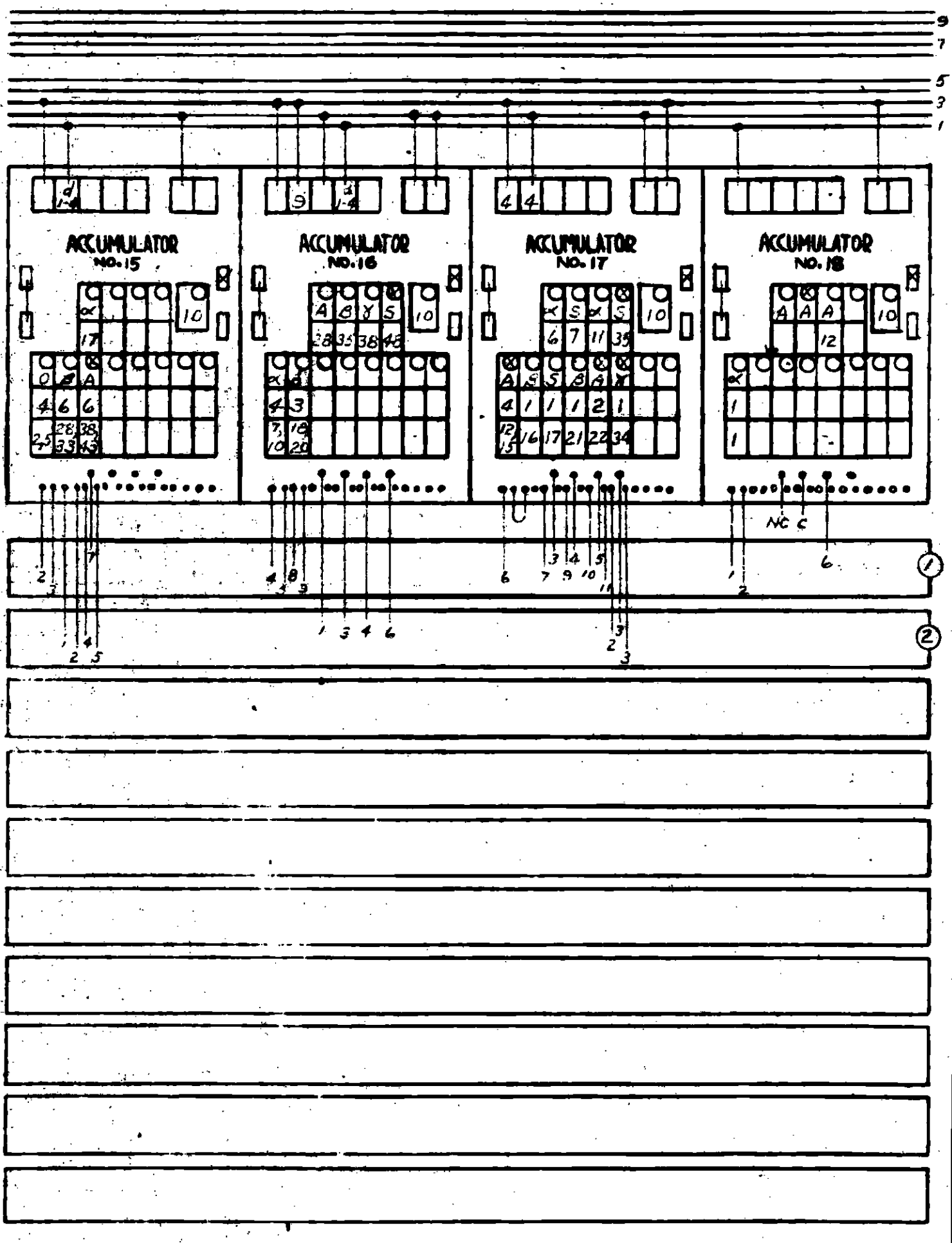


Fig. 7-3 (d)

Quadratic Lagrangian Interpolation - Set-Up Diagram

PX-7-403e

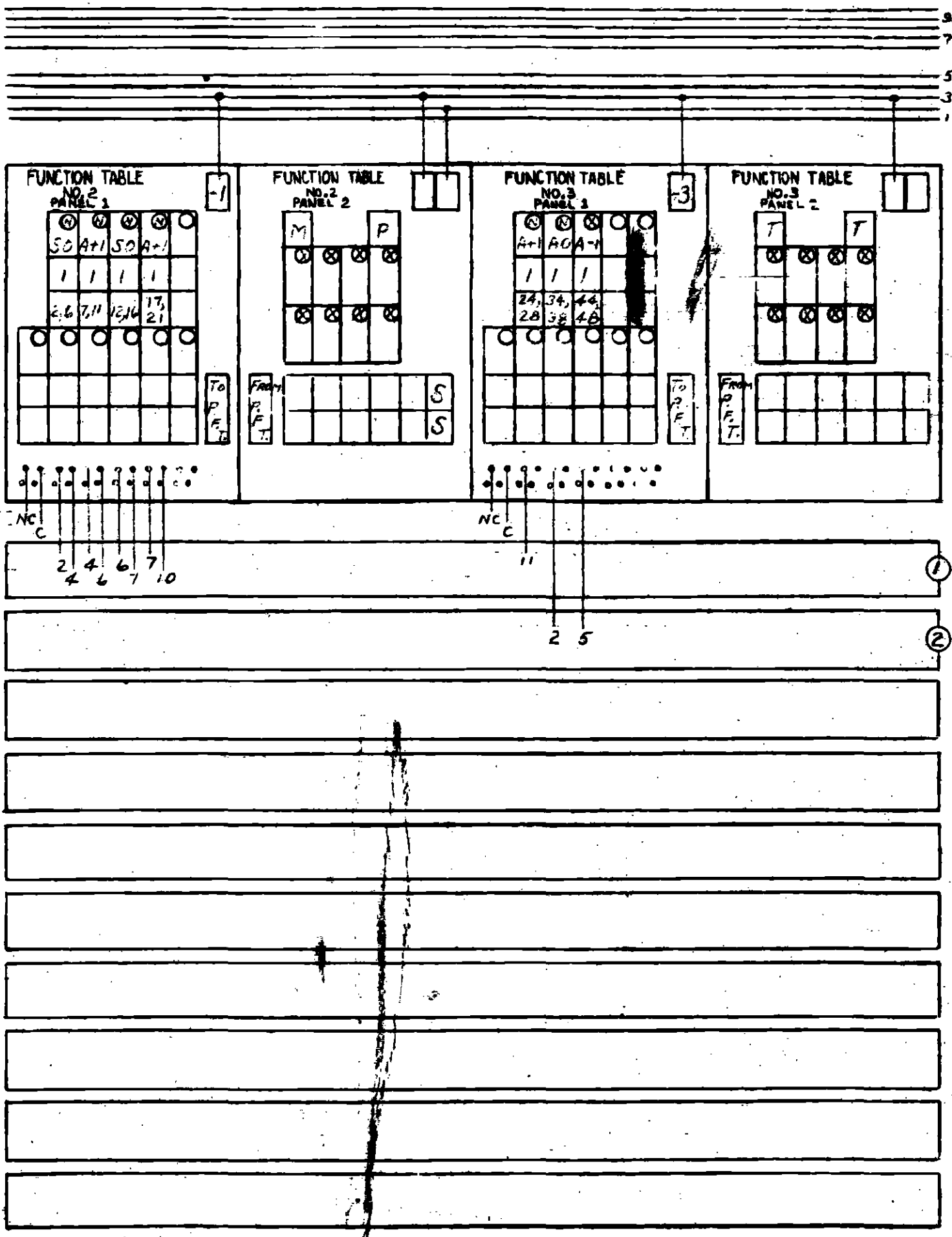


Fig. 7-3 (e)

Quadratic Lagrangian Interpolation - Set-Up Diagram

7.5.1. Quadratic Lagrangian Interpolation

In the following pages a set-up for quadratic Lagrangian interpolation for equal intervals is suggested. The interpolation formula is given by

$$f(x) = \sum_{i=-1,0,1} C^{(i)}(x_2,x_3,x_4) \cdot f_i(x_0,x_1)$$

where

$$x = \sum_{j=0}^{4} x_j \cdot 10^{1-j} \quad \text{and } 0 \leq x \leq 99$$

and where $f_i(x_0, x_1) = f_i(x_0, x_1 + i)$

Even though it is cumbersome, the notation $x = \sum_{j=0}^{4} x_j \cdot 10^{1-j}$ is employed because it is useful in indicating the shifters and deleters required in certain phases of the problem.

The computation is described with the aid of Table 7-4, in which the set-up of the units involved is formulated, and Figure 7-3, which shows how to set up the units to carry out the instructions given in Table 7-4.

The values of $C^{(0)}$ and $C^{(1)}$ are stored in function table 2 in such a way that the former are emitted over the lines for decade places 1-6 of terminal A and the latter, over the lines for decade places 1-6 of terminal B. These coefficients are stored at intervals of 0.01 for $x_2 \cdot 10^{-1} + x_3 \cdot 10^{-2}$ starting with zero and ending with 1.00. Linear interpolation is used to find $C^{i}(x_2,x_3,x_4)$. The symbols $C_C^{(i)}$, $C_I^{(i)}$, and $\Delta C^{(i)}$ will be used as follows:

$$C_0^{(i)} = C^{(i)}(x_2,x_3,0)$$

$$C_1^{(i)} = C^{(i)}(x_2, x_3+1,0)$$

$$\Delta C^{(i)} = C_1^{(i)} - C_0^{(i)}$$

Thus, $C^{(i)}(x_2, x_3, x_4)$ is given by the formula

$$C^{(i)}(x_2, x_3, x_4) = C_0^{(i)} + \frac{1}{10} \cdot x_4 \cdot \Delta C^{(i)}$$

$C^{(-1)}$ has not been tabulated in a function table since it can be found readily from the relationship

$$C^{(-1)} = 1 - \sum_{i=0,1} C^{(i)}$$

$C^{(0)}$ and $C^{(1)}$, rather than a pair including $C^{(-1)}$ were chosen for tabulation on the portable function table to save a small amount of tabulation labor. For the range zero to one inclusive of the independent variable, $C^{(0)}$ and $C^{(1)}$, are both positive and have zero and one as their minimum and maximum values. Therefore, sign indication need not be tabulated with each entry but may, instead, be handled by setting the master PM switches to P. The coefficient $C^{(-1)}$ has as its maximum value on this range of the argument, zero, and, as its minimum -0.12500. Were $C^{(-1)}$ tabulated, all entries would have to carry sign indication (and the master PM switch would be set to Table) in spite of the fact that the only non-negative functional entry is zero corresponding to argument zero. It might at first appear that zero could be tabulated as M 0 000 000 000, but if we recall that M 0 000 000 000 actually represents 10^{10} + P 0 000 000 000 it can be seen that this procedure would be incorrect.

$C^{(1)}$ and $C^{(0)}$, then, are tabulated on the portable function table associated with function table 2 on sides A and B respectively. Six decade places are used for each coefficient with the units place digit tabulated in the column for decade place 6 and the various decimal places (tenths place, etc.) occupying the remaining decade places, 5 through 1. The digit delete switches A4 - A1 and B4 - B1 are set to "delete" since there are no digits constant through-

out the range of the argument for either $C^{(0)}$ or $C^{(1)}$. Since the coefficients $C^{(i)}$ find their way ultimately to the multiplier, it is desirable to have them located as far to the left as possible. The digit output of function table 2 is, therefore, shifted four places to the left before its reception in an accumulator. The shifter is designated by the number 4 in a box denoting a digit input terminal on Figure 7-3.

The function f(x) is tabulated on the portable function table associated with function table 3. It is assumed, here, that only 6 variable digits are tabulated for this function and that these occupy the switches for decade places 1-6. Since f_i (i= -1, 0, 1) too, enters into multiplications, the function output of function table 3 is also shifted 4 places to the left before its reception in the ier accumulator.

Accumulator 18 serves as the argument accumulator for both function tables. This set-up assumes that x is stored in this accumulator so that x_0 occupies the fifth decade place. A -1 shifter (which shifts a number one place to the right) is used at the argument input terminal of function table 2 to place x_2 and x_3 respectively in decade places 2 and 1 of the input and a -3 shifter is used at the argument input terminal of function table 3 to place x_0 and x_1 respectively in the proper decade lines of this input.

Detailed descriptions of the programs involved in the interpolation are given in Table 7-4. We wish, however, to call attention to the procedure used for stimulating the reception in an accumulator of functional values transmitted by the function table. Consider, for example, the programs involved in looking up $-C_0^{(0)}$. In addition time 12, program pulse 1-6 stimulates function table 2 to look up $-C_0^{(0)}$. Accumulator 17 is to receive this functional value when it is emitted during addition time 16. To provide for this reception, we

take advantage of the fact that another program commences at the same time that function table 2 is stimulated, the program in which accumulator 17 transmits its contents to the multiplier. Even though only 1 transmission is required, the repeat switch on control 5 of accumulator 17 is set at 4 so that at the end of addition time 15 there will be a program pulse available to stimulate the reception of $-C_0^{(0)}$. This procedure saves the use of a special dummy program to delay a pulse until addition time 16.

The use of the high-speed multiplier in this computation is also worthy of note. During addition times 12 through 17 and 22 through 27 the multiplier is occupied in forming products required in the linear interpolation for $C^{(1)}$ and $C^{(0)}$ respectively. For each of these multiplications, the significant figures switch is set at 6. In view of the accuracy of the ier and icand and their positions in the ier and icand accumulators, the last significant figure of the product occurs in the eighth place from the left. These products, however, are added to numbers stored in either accumulator 16 or 15 which have their last significant figure 6 places from the left. The products referred to above are, therefore, rounded off to 6 significant figures and passed through deleters which delete decade lines 1-4 (counting units decade as 1) before reception in accumulator 16 or 15. This deleter is designated by d 1-4. Thus, by addition times 18 and 28 respectively, $C^{(1)}$ and $C^{(0)}$ appear in accumulators 16 and 15 respectively correct to 5 significant figures with the last significant figure appearing in decade 5 (from the right).

The products $f_i \cdot C^{(i)}$ (for i = 1, 0, -1) are formed during addition times 28-37, 38-47, and 48-57 respectively and are retained in accumulator 12 for collection to form f(x). Since the coefficients $C^{(i)}$ will in general not exceed 5 significant figures, these products, too, will have no more than 5 significant figures with the last significant figure appearing in the sixth

decade place from the left due to the positions of the ier and icand. Only the program in which $f_i \cdot C^{(1)}$ is formed, calls for round off to 6 figures, however, since the addition of five pulses in decade place 3 is required only once to produce the correctly rounded off sum of 3 products. For the other two multiplications $f_0 \cdot C^{(0)}$ and $f_{-1} \cdot C^{(-1)}$. The significant figures switch is set at "off".

It might be of interest to the operator to notice that of the 57 addition times required to carry out this quadratic Lagrangian interpolation routine, all but 15 are used for multiplications. In general, the principle that the number of multiplications involved in a computation determines approximately the duration of the computation is a reliable one.

7.5.2. Biquadratic Lagrangian Interpolation

Biquadratic Lagrangian interpolation can be carried out in a fashion similar to that described above for quadratic Lagrangian interpolation with a few minor alterations. The formula for biquadratic interpolation is

$$f(x) = \sum_{i=-2,}^{2} C^{(i)}(x_2, x_3, x_4) \cdot f_i (x_0, x_1)$$

Here, as in the quadratic interpolation, one of the coefficients need not be tabulated since

$$\sum_{i=-2}^{2} C^{(i)} = 1$$

The four coefficients needed may, as a matter of fact, be tabulated on one* portable function table to permit interpolation for $C^{(i)}(x_2, x_3, x_4)$

---

*This assumes that six decimal places for these coefficients will provide the required accuracy. If greater accuracy is required it is probably preferable to generate the coefficients rather than use up two function tables for storing them.

from a tabulation of $C^{(i)}(x_2, x_3, 0)$ since the $C^{(i)}$ need be tabulated only for $0 \leq x_2 \cdot 10^{-1} + x_3 \cdot 10^{-2} \leq .51$. For $0.5 \leq x_2 \cdot 10^{-1} + x_3 \cdot 10^{-2} < 1$, f(x) may be computed by backward interpolation using the formula

$$f(x) = \sum_{i=-2,-1,\ldots,2} C^{(i)}(x_2', x_3', x_4')\, f_i\, (x_0, x_1 + 1)$$

where

$$x_2' \cdot 10^{-1} + x_3' \cdot 10^{-2} + x_4' \cdot 10^{-3} = 1 - (x_2 \cdot 10^{-1} + x_3 \cdot 10^{-2} + x_4 \cdot 10^{-3})$$

If the coefficients chosen for the tabulation are $C^{(i)}$ (for i = -2, -1, 1, 2), they may be set up on the portable function table as shown in Table 7-5.

To produce $C_0^{(i)}$ and $C_1^{(i)}$ for i = -2 or 2 the function table operation switches must be set at -2 and -1 respectively. Before $C_0^{(i)}$ and $C_1^{(i)}$, for i = 1 or -1, can be looked up, the argument (x_2, x_3), or (x_2', x_3') if backward interpolation is used, must be corrected to (x_2+5, x_3) or $(x_2' +5, x_3')$. The operation switches used in the programs of looking up $C_0^{(i)}$ and $C_1^{(i)}$, for i = 1 or -1, must be set at zero and 1 respectively.

If the suggested method of tabulating the interpolation coefficients and of carrying out the interpolation is followed, obviously two alternative interpolation routines, a forward and a backward routine, must be set-up.

The forward interpolation routine differs from the routine for quadratic Lagrangian interpolation only in that there are two additional product terms $f_i \cdot C^{(i)}$ to be formed. The backward interpolation routine must cover the use of the backward interpolation formula, the correction of the argument (x_0, x_1) to $(x_0, x_1 + 1)$ and the correction of the argument (x_2, x_3, x_4) to

TABLE 7-5

TABULATION OF BIQUADRATIC LAGRANGIAN INTERPOLATION COEFFICIENTS ON THE PORTABLE FUNCTION TABLE

Arg.	A OUTPUT Master PM switch 1 set at P. Decade places 1-6 used as shown below.	B OUTPUT Master PM switch 2 set at Table. PM place and decade places 1-6 used as shown below.
-2	$C^{(-2)}(00) = .000\ 000$	$C^{(2)}(00) = +\ .000\ 000$
-1		
.	$0 \leq C^{(-2)} \leq .023\ 427$	$-\ .039\ 464 \leq C^{(2)} \leq 0$
.		
49	$C^{(-2)}(51) = .023\ 427$	$C^{(2)}(51) = -\ .039\ 464$
50	$C^{(1)}(00) = .000\ 000$	$C^{(-1)}(00) = +\ .000\ 000$
51		
.	$0 \leq C^{(1)} \leq .480\ 016$	$-\ .155\ 767 \leq C^{(-1)} \leq 0$
101	$C^{(1)}(51) = .480\ 016$	$C^{(-1)}(51) = -\ .155\ 767$

(x_2', x_3', x_4'). The criterion for which routine is to be followed is a magnitude discrimination program to determine whether $x_2 < 5$ or $x_2 \geq 5$. In the former case, the forward interpolation routing is followed; in the latter case, the backward interpolation routine is used.

The disadvantage of the method suggested above for biquadratic Langrangian interpolation is that it requires a backward as well as a forward routine. This disadvantage is eliminated in an alternative method to be described below.

For the purpose of this discussion, we will abandon the notation used above and in section 7.5.2. Instead, x will be considered as $x = n + h$ where n is the integer closest to x and where $-.5 \leq h \leq .5$. The number n, thus, is an integer between 0 and 99 inclusive. In this notation f(x) is given by

$$\sum_{i=-2}^{2} C^{(i)}(h) \cdot f_i(n) \quad \text{or} \quad \sum_{i=-2}^{2} C^{(i)}(h) \cdot f(n+i)$$

To find n, the round off facilities of some accumulator are used and the number $x + 0.5$ is formed. Then n is the tens and units digits of $x + 0.5$. Now, the number $x + 0.5$ or $n + k$ where $k = h + 0.5$ is stored in some accumulator.

Instead of tabulating coefficients $C^{(i)}(h)$ then, consider tabulating $B^{(i)}(k) = C^{(i)}(h)$ for the range $0 \leq k \leq 1$, where the coefficients $B^{(i)}(k) = C^{(i)}(k)$ have the following useful properties:

1) $\sum_{i=-2}^{2} B^{(i)}(k) = 1$ and 2) $B^{(-i)}(k) = B^{(i)}(1-k)$

We can then tabulate $B^{(i)}(k)$ for $0 \leq k \leq 1$ for two values of i. By property 2 above, $B^{(i)}(k)$ for two other values of i can be found, and the fifth value of B can be found by property 1.

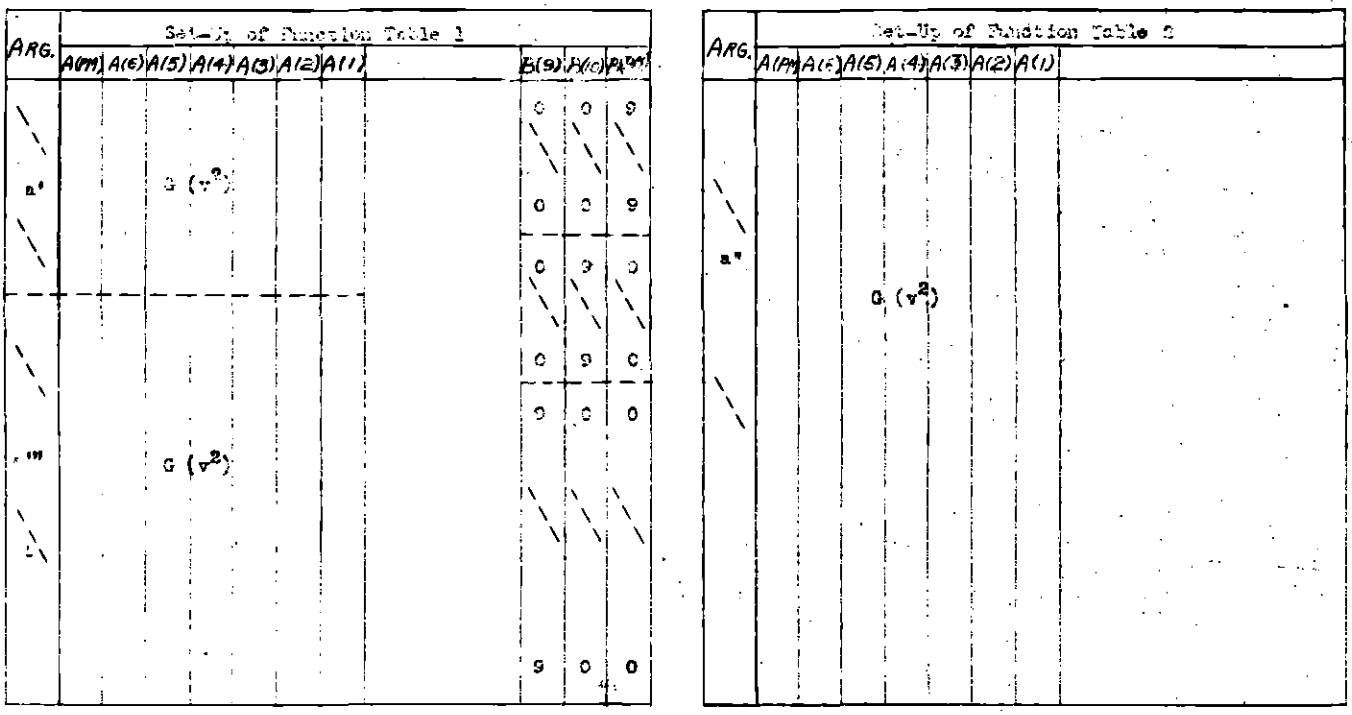
7.5.3. The Drag Function of the Exterior Ballistics Equations

When the ENIAC is used for the computation of firing tables, the problem of tabulating the drag function (G) used in the exterior ballistics equations is likely to require considerable thought due to the behavior of this function in the region of the velocity of sound. It would appear that the drag function had best be tabulated against v^2 as is done for hand computation of trajectories to avoid the necessity for extracting square roots. It will also be necessary to use more than one portable function (or more than part of one portable function table) to list the values of the drag function since one portable function table will certainly have to be devoted to the values of G in the neighborhood of the velocity of sound. G before and after sound may be tabulated on one or two portable function tables depending on which G function is used and the accuracy requirements of the computation.

To determine what transformation to make on v^2, which function table to enter, and possibly, even which interpolation routine to follow, it will then be necessary to carry out a magnitude discrimination program on v^2 similar to the one used on y' in the printing discrimination sequence of problem 2 in Chapter X (Master Programmer).

An alternative and, probably, simpler method of determining which function table to enter for a given value of the argument can be used if this information is stored on portable function table switches not required for the tabulation of G. One column of a portable function table is required for each function table or portion of a function table used in tabulating G.

Here a preliminary transformation of variable which maps the entire range of the argument onto the interval 0 and 99 is made. The portable function table which stores program data is entered with this argument. The function out-



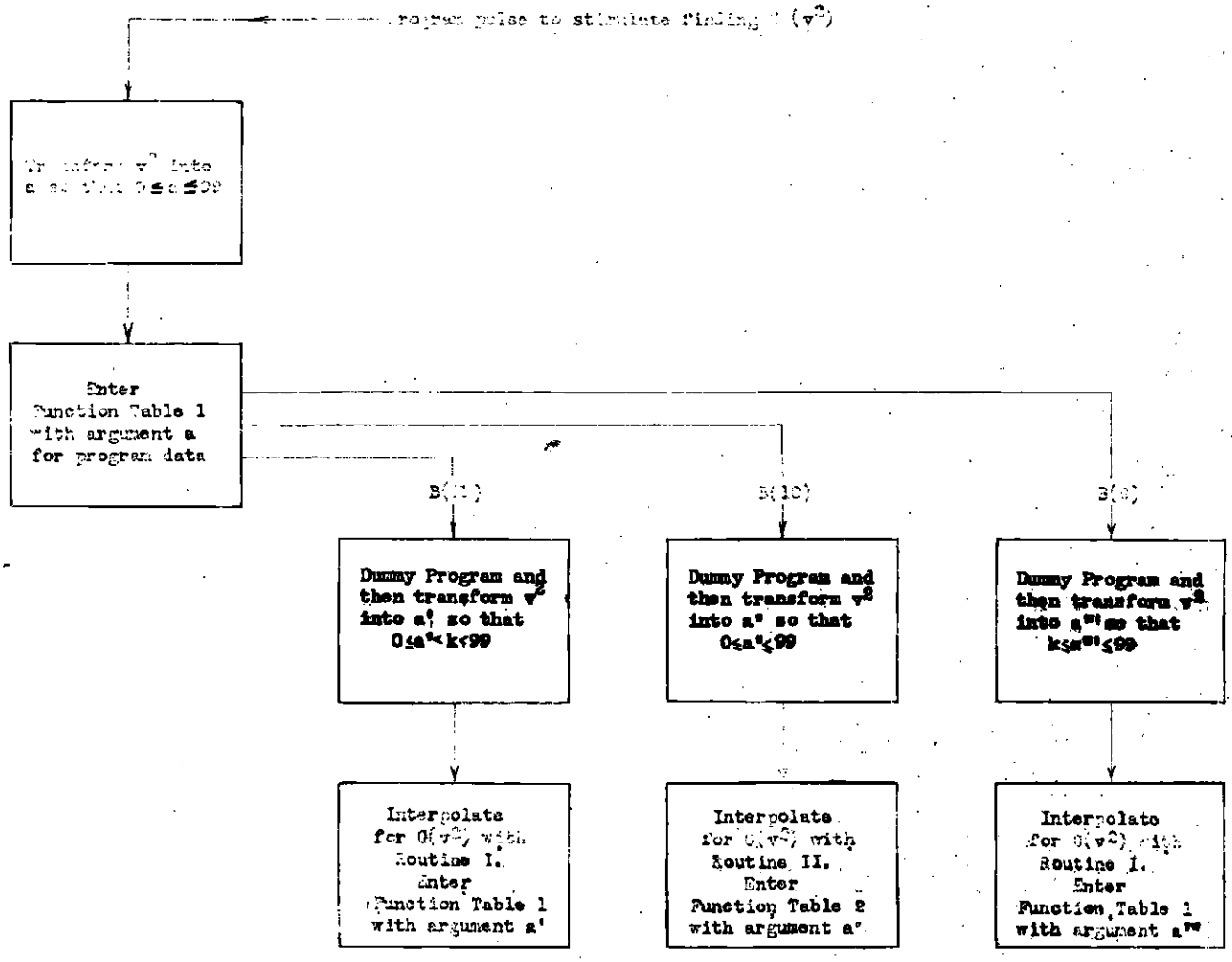


Figure 7-4

Storage of the G Function and Programming Instructions Regarding Use of the Tabulated Function

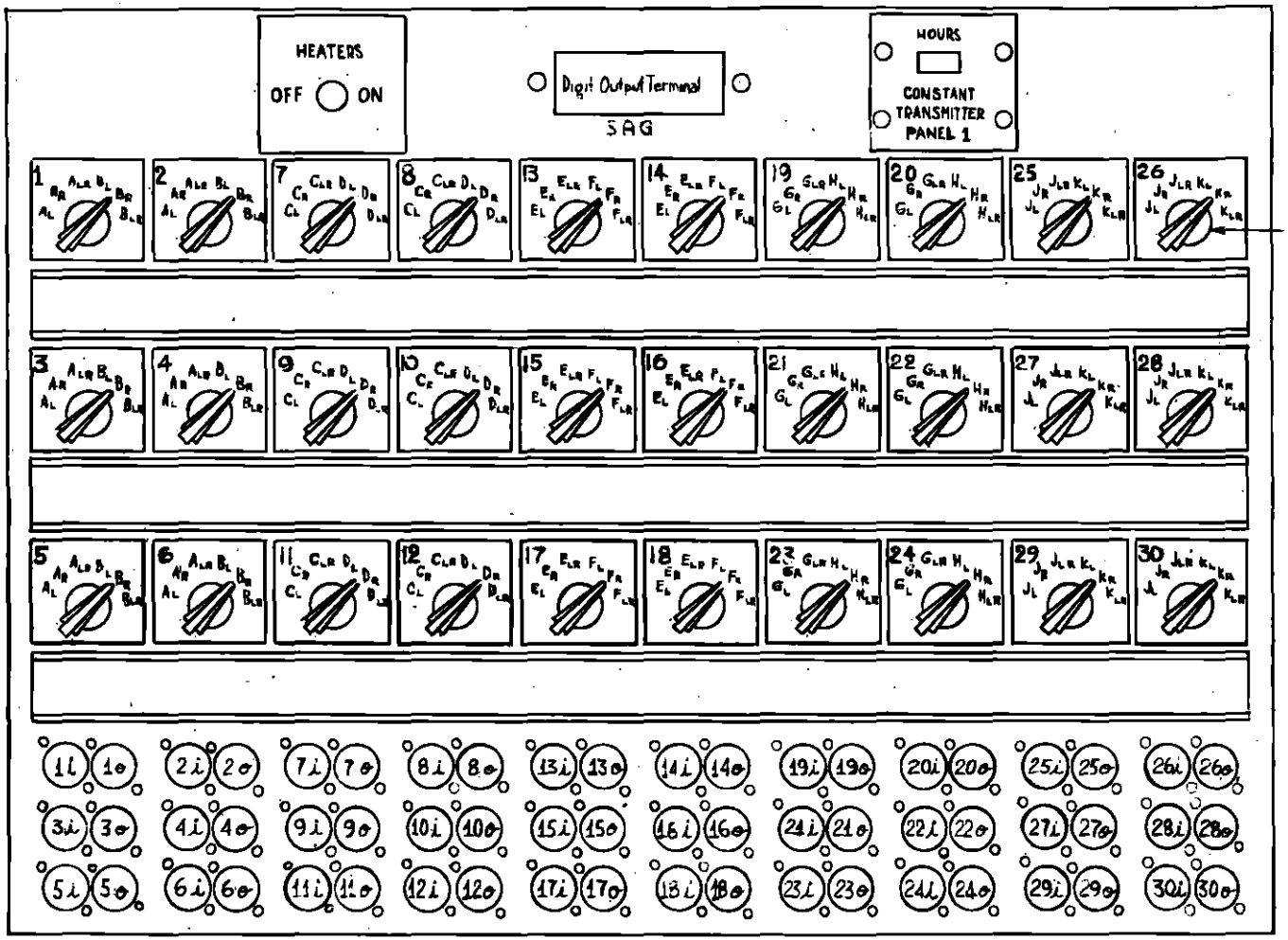
put of the decade place leads used for program choice are converted to a program pulse through the use of a dummy program. The resulting program pulse is then taken to a program control which initiates a suitable interpolation routine. (See Figure 7-4).

Another consideration which is likely to arise is that of making the most efficient use of the variable digits of the function table. Throughout the major part of the velocity of sound region, tenths place of the G function is occupied by the digit zero. However, for convenience in interpolation, it may be desirable to extend the tabulation on the portable function table devoted to the neighborhood of the velocity of sound so that some entries in which tenths place is occupied by the digit one instead of zero are also included.

If the obvious method of tabulation (PM column devoted to sign indication and variable digit columns to tenths, hundreds, etc., places) is followed, most of the entries will waste a place on the non-significant figure zero in tenths place in order to accommodate the few entries that have digit one in tenths place. However, since the G function does not change sign and since there is no reason for transmitting both the functional value stored and its complement, it is possible to resort to an artifice that will result in the storage of an additional significant figure without the use of an extra place of the portable function table.

The artifice consists of tabulating tenths place of the G function in one of the so called PM columns making sign P correspond to digit zero and sign M to digit one. The problem of converting the 9 sign pulses transmitted from the function table entries carrying sign M to a single digit pulse can be solved very simply by transmitting the PM channel of the function output to an unused transceiver input and then transmitting the transceiver's output to the digit

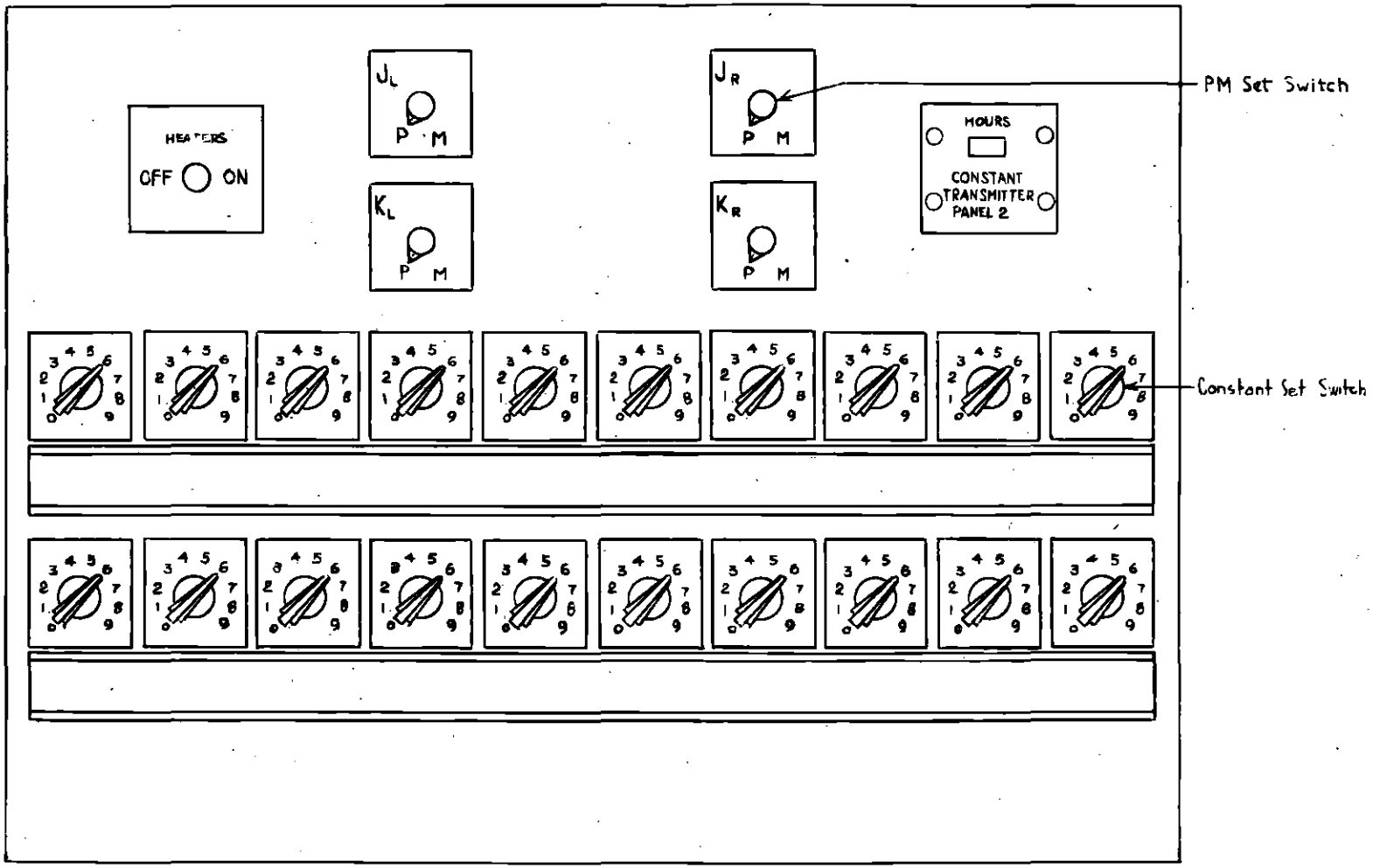
input terminal channel devoted to tenths place at the unit receiving the functional value. Thus, when sign P is stored, no pulses will be transmitted from the PM channel of the function output terminal and therefore the transceiver, receiving no pulse, will transmit no output pulse so that the unit receiving the functional value will receive zero pulses in the decade channel devoted to tenths place. When sign M is stored, 9 sign pulses received by the transceiver cause the transceiver to emit one pulse which is received in tenths place by the unit receiving the function output of the function table. Obviously, if this strategem is resorted to, the program of receiving the functional value from the function table must be set up on an accumulator repeat program control whose repeat switch is set at 2 in order to allow time for the accumulator's reception of a pulse from the transceiver which converts the 9 sign pulses into a digit pulse.



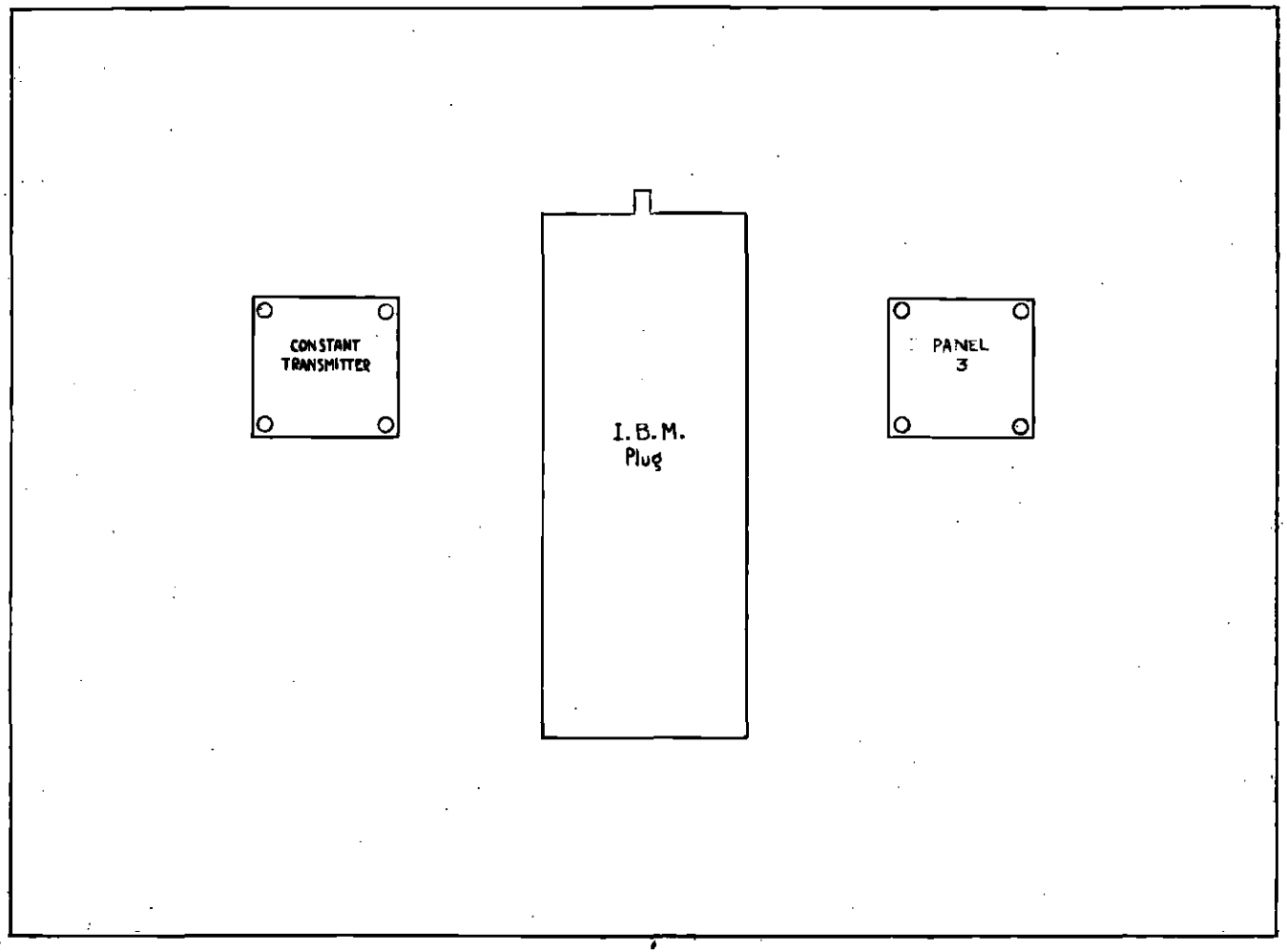
TERMINALS 1i, 2i, ---, 30i
Program input pulse terminals associated respectively with constant selector switches 1-30.

TERMINALS 1o, 2o, ---, 30o
Program output pulse terminals associated respectively with constant selector switches 1-30.

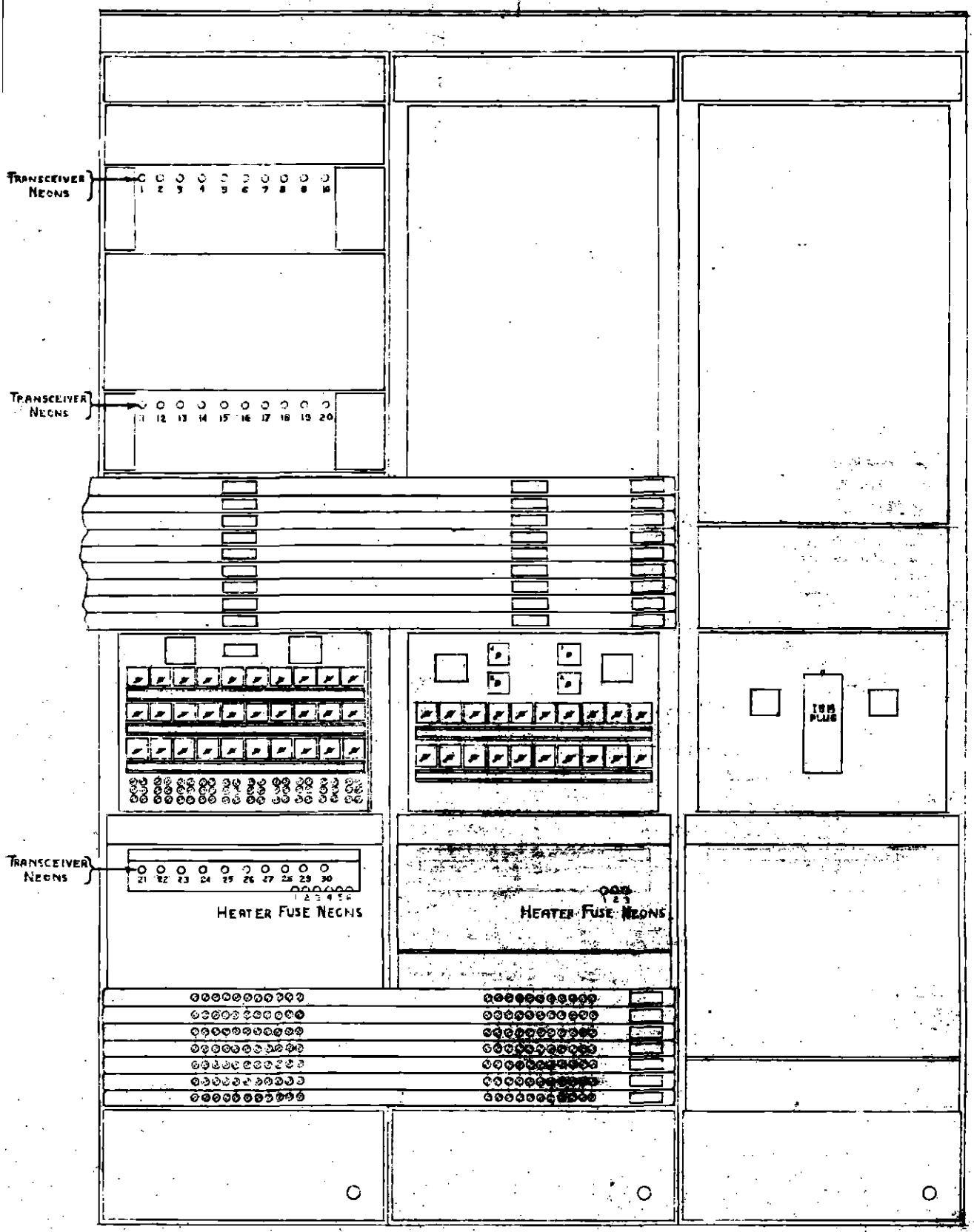
CONSTANT TRANSMITTER FRONT PANEL NO.1
PX-11-302R



CONSTANT TRANSMITTER FRONT PANEL NO. 2
PX-11-303 R



CONSTANT TRANSMITTER
FRONT PANEL NO. 3
PX-11-304 R



MOORE SCHOOL OF ELECTRICAL ENGINEERING
UNIVERSITY OF PENNSYLVANIA

CONSTANT TRANSMITTER
FRONT VIEW
PX-11-306

VIII. CONSTANT TRANSMITTER AND IBM READER

The constant transmitter operating in conjunction with an IBM card reader provides another form of memory for the ENIAC (see also, the function table and accumulator). The input rate for this memory is relatively slow; the output rate is rapid. The reader reads standard IBM cards at the rate of approximately 1/2 a second per card* and causes the data recorded on the card to be stored in relays located in the constant transmitter. The 80 digits which can be read from a card may be broken up into 5 digit or 10 digit groups with sign indication so that as many as 16 signed numbers may be read from a card. In addition, the constant transmitter can remember 20 digits and 4 signs set up manually on switches located on front panel 2 of this unit. These 20 digits may be broken up also into groups of either 5 or 10 digits with sign indication. Once stored in the relays or on the manual set switches of the constant transmitter, numerical data can be obtained in pulse form for use in any arithmetic unit of the ENIAC in one addition time.

The first four sections of this chapter are devoted to the IBM reader as follows: Section 8.1, program controls, Section 8.2, plug board, Section 8.3, programming circuits, and Section 8.4, numerical circuits. The program controls and numerical circuits of the constant transmitter are discussed in Sections 8.5, and 8.6, respectively. An illustrative problem set-up appears in Section 8.7.

In this chapter, reference will be made to the following drawings:

Constant Transmitter and Reader Cross Section	PX-11-309
IBM Reader Wiring	PX-11-119
IBM Reader Plug Board	PX-11-305

*The rate is 160 cards per minute when the reader reads continuously without stopping and may be either 120 or 160 cards per minute when the reader stops between readings.

Activation of IBM Reader Relays in Reading a Detail-Master-Detail Card Sequence	PX-11-308
Constant Transmitter Front View	PX-11-306
Constant Transmitter Front Panels	PX-11-302, 303, 304
Constant Transmitter Block Diagram	PX-11-307
Constant Transmitter Cross Section	PX-11-116
Initiating Unit - Front View	PX-9-305
Initiating Unit Front Panel	PX-9-302

8.0. GENERAL SUMMARY OF THE READER AND CONSTANT TRANSMITTER

8.0.1. IBM Cards

The IBM reader operates on standard IBM cards. These cards have 80 columns and each column has 12 positions. The first two positions (reading down from the top) are designated by 12 and 11. The remaining ten positions correspond to the numbers 0 to 9 and are printed to indicate this correspondence. Data is stored on these cards by means of card punches. The group of columns used to indicate the digits for a given number is called a field.

Any of the 80 columns on the card may be used to store either numerical data or control data (i.e. information which instructs the reader how to dispose of the numerical data stored on the card or on succeeding cards). A column used for storing numerical data will have one of the positions zero to 9 punched. Negative numbers are indicated by an 11 punch which can appear in addition to a digit punch, in any one of the columns used for the various places of the number. No sign indication punch is used for positive numbers. Columns used for control purposes can have multiple punches. In addition, a column used for numerical data can carry a 12 or 11 punch for control purposes provided that an 11 punch

does not appear in the same column for sign indication. The distinction between an 11 punch for control purposes and one for sign indication is made as a result of the wiring of the reader plug board (see Section 8.2.).

8.0.2. The Card Reader (refer to Px-11-309 and PX-9-302)

The IBM card reader scans cards and causes numerical data (with sign indication) located in any field of the card to be stored in any groups of constant transmitter storage relays specified by the operator (see Section 8.2. and group selection in Section 8.3.). The aforementioned operations are designated by the phrase card reading. True negative numbers on the cards are converted into nines complements in the process of being stored in the constant transmitter and into tens complements during transmission from the constant transmitter. Moreover, the IBM reader can recognize 2 classes of cards namely, master and detail cards. The reader causes numerical data read from a master card to be stored in constant transmitter storage relays and held until the next master card is read at which time the information read from the previous master card is dropped out and replaced by data on the new master card. Detail card information is dropped out whenever a new card, either master or detail, is read.

Certain controls for starting and stopping the reader are found on the initiating unit and others on the reader itself. The reader is stimulated to read a card which is in position to be read when the reader start button on the initiating unit is pressed at the beginning of a computation (see Chapter II, Section 2) or at the beginning or in the course of a computation when the reader program pulse input terminal (Ri) on the initiating unit is pulsed. Pushing the emergency start switch on the IBM reader itself also causes card reading to take place. When the reader is started initially and there are cards in its magazine but not in position to be read (see Section 8.1.), the initial start switch on

the reader must be pushed to move a card into the reading position.* The reader stops reading when the cards in its magazine have been exhausted, or its hopper is filled, when the stop switch on the reader is pressed, or when the reader's motor generator is turned off (see Section 8.1.).

Also found on the initiating unit are a reader interlock pulse input terminal (Ri) and a reader program pulse output terminal (Ro). Since reading takes a not absolutely definite time for completion, the ENIAC has been so designed that an interlock pulse must be received and card reading must be completed before the reader will emit a program output pulse which can be used to initiate the phase of the computation which follows card reading. One exception to this statement is noted in Section 8.1.1.

8.0.3. Card Reading (refer to PX-11-309 and PX-11-119)

The operator specifies the criterion for master or detail cards and also the correspondence between positions on the card and storage relays in the constant transmitter by means of the setting of the polarity switch located on the reader and by the manner in which the reader plug board is wired (see Section 8.2.). The reader recognizes its instructions with regard to these matters through the punches made on the various cards.

The programming equipment (see Section 8.3.) in the reader which carries out the instructions consists of relays and cams which make and break contact at various times. The programming relays, in general, are used as follows: Each relay has either a pick-up (P) coil, a hold (H) coil or both** and 4 contacts some or all of which may be used. The hold coil of a relay is connected in series through one of its contacts, called the hold contact, to a timing cam.

*When cards are in position to be read, the initial start switch cannot stimulate card reading.

**Where one type of coil is missing, the functions of both types are performed by the one used.

Some stimulus, a particular punch on a card or the activation of another relay, perhaps, causes the P coil of a relay to pick up. The H coil then holds the relay through its hold contact until the cam with which the relay is in series breaks contact.

PX-11-119 shows the various relays and cams. The several components of a relay are often found on different parts of the diagram. The relay location chart at the top of PX-11-119 gives the location on the diagram of the P and H coils and the points of contact (A and B lower and upper). The timing cams are designated on this drawing by P1 - P10. The times at which the cams make and break contact are also noted here with M and B respectively identifying the make and break times. The times are given according to the IBM scale which divides the card reading cycle into 14 subdivisions designated by 14, 12, 11, 0, 1, ..., 8, 9, 13. The cycle begins half a unit before 14 and ends half a unit after 13. For the reader, the time divisions are approximately equal. More complete timing information about the cams is given on PX-11-309.

The cards are read by being passed under each of two continuous rolls. Eighty brushes located below the card make contact with the continuous roll where the card has been punched. The reader by means of the 80 brushes scans all 80 columns of a card simultaneously beginning at time 12 with line 12 in all columns and then the 11 line in time 11 and, finally, in time 9, the 9 line.

There are two continuous rolls each with a set of 80 brushes, roll No. 1 with the control brushes and roll No. 2 with the read brushes. Each card is read in two cycles. At the start of the i^{th} card reading cycle, card i is in front of continuous roll No. 2 making contact with card lever contact No. 1 for continuous roll 2 (CR No. 2, CLC No. 1) and card i + 1 is in front of continuous roll No. 1 making contact with card lever contact No. 1 for continuous roll No. 1

(CR No. 1, CLC No. 1). During the i^{th} reading cycle, card i is moved under roll No. 2 and scanned by the read brushes for numerical data. This data is ultimately delivered through the connections made on the plugboard to the lines which go to relays in the constant transmitter. While card i is passing under continuous roll No. 2, card i + 1 is passing under continuous roll No. 1 where it is read by the control brushes. The control brushes pick up instructions with regard to how card i + 1 is to be treated and deliver these instructions via plugboard connections to the programming circuits of the reader (see Section 8.3.) As card i + 1 moves under continuous roll No. 1, card i + 2 moves out of the magazine so that cards will be in position for the i + 1 st reading cycle. The second or numerical reading cycle for a card does not necessarily follow immediately after the first or control cycle. The second cycle takes place when the reader is stimulated to start reading. However, when a master card is read, the second cycle for the detail card immediately after the master card takes place without delay.

8.0.4. Storage of Card Data in the Constant Transmitter

The circuits involved in converting numerical data punches into a storage form usable by the Eniac itself are:

80 read brushes	(see PX-11-309, 11-119)	In the reader
Coding cams CB1, CB2, ..., CB9	(see PX-11-309, 11-119)	
16 groups of 8 coding relays each	(C_1, C_2, ..., C_8 on PX-11-116, 11-309)	In the Constant Transmitter
16 pairs of PM relays	(PM' and PM" on PX-11-116, 11-309)	
6 PM isolating relays	(labelled R on PX-11-116, 11-309)	
80 groups of 4 storage relays each	(the storage relays for the first group are labelled 1-1, 1-2, 1-2', and 1-4 on PX-11-116).	

Information from the 80 columns on the IBM card is ultimately stored in the 80 groups of storage relays. The 80 groups of storage relays control 80 groups of four constant selector gates each (see PX-11-307) and these gates in turn, control the gates which allow the 1, 2, 2', and 4 pulses respectively to pass when a constant is being transmitted from the constant transmitter.

Each 5 digit group with sign indication is set up in the storage relays and PM' and PM" relays as a result of the interaction of the coding cams, a contact on one of the 6 PM isolating relays, the pair of PM relays, a group of 8 coding relays, and the 5 leads from the read brushes which read the columns belonging to that group of 5 digits.

8.0.5. Transmission of Data from the Constant Transmitter (refer to PX-11-302, 11-303, 11-309, and 11-307)

On panel 1 (see PX-11-302) of the constant transmitter are found 30 program controls and associated neons (see PX-11-306). Each program control consists of a transceiver with program pulse input and output terminals and an associated constant selector switch. Each group of 6 program controls is concerned with the transmission of 20 digits. The program controls numbered 1-24 handle the 80 digits read from IBM cards and those numbered 25-30 the 20 digits set up manually on the constant set switches located on panel 2 (see PX-11-303). The letters A, B, ..., G, H on the constant selector switches refer to the 8 groups of 10 digits each which can be stored in the constant transmitter from IBM cards; J and K refer to the 20 digits set up manually on the set switches located on panel 2. Subscripts L and R refer respectively to the left and right hand groups of 5 digits (each with sign indication) of a 10 digit group. Ten digits with a single PM are designated by subscript LR. (See Section 8.2, for the correspondence between storage relay hubs on the plug board and the points A_L, A_R, ..., H_R on

the constant selector switches.) The digit output of the constant transmitter is emitted through the output terminal on panel 1 (see PX-11-302).

Any or all of the 6 constant selector switches of a group may be set so as to call for the transmission of any one 5 digit or 10 digit signed number controlled by that group of switches. The only restriction is that if a constant selector switch be set so as to call for the transmission of either the L or R 5 digits of a 10 digit group, none of the other 5 switches may be set so as to call for the transmission of the same 10 digits as a group (LR). Conversely, if 10 digits are combined by an LR setting of a constant selector switch, the same 10 digits can never be broken up into 5 digit L or R groups on any of the remaining 5 constant selector switches.

The points on the constant selector switches are connected to the constant selector gates. For these gates the 2nd input comes from a storage relay or a constant set switch and may, in either case, be a digit or a PM.

The constant selector gates whose second inputs are numerical in nature, control the 1, 2, 2', and 4 pulse gates which allow suitable combinations of the 1, 2, 2', and 4 pulses to be passed over the 10 digit leads of the constant transmitter's digit output terminal (located on panel 1). The constant selector gates whose second inputs are derived from minus sign indication, control gates which allow the 9 pulses to pass over the PM lead and possibly the 5 left hand leads of the digit output terminal and which allow the 1' pulse (needed to produce a tens instead of nines complement) to pass over either the units place or 10^5 place lead of the digit output terminal.

8.1. PROGRAM CONTROLS OF THE IBM READER (Refer particularly to PX-11-119)

The reader program controls located on the reader are the initial start switch, the emergency start switch, the on-off switch and the green motor generator signal light, and a stop switch. Relay 3 in the reader is the start relay for the clutch magnets which cause the card feed mechanism to operate. Also inside the reader are certain circuit elements which function in conjunction with the program controls for starting the reader: magazine card lever contact (Mag CLC) and relay 1, card lever contact No. 1 for continuous roll No. 1 (CR No. 1, CLC No. 1) and relay 2, card lever contact No. 2 for continuous roll No. 1 (CR No. 1 CLC No. 2), and the card stacker switch. Card lever contact No. 1 for continuous roll No. 2 (CR No. 2, CLC No. 1) with relay 60, and relay 59 in the reader play a part in the emission of reset and finish signals by the reader and are discussed in greater detail in Section 8.3.3.

Located at the initiating unit (see PX-11-307) are other program controls for the reader: the reader start button, the reader program pulse input terminal (Ri)and start flip-flop, the reader interlock pulse input terminal (Rl) and flip-flop, the reader finish flip-flop, the reader synchronizing flip-flop, program output pulse transmitter, and program pulse output terminal (Ro).

The only program control for the reader that is housed in the constant transmitter is the reader start relay.

The green motor generator signal light goes on when the reader is plugged into a source of power provided that the on-off switch is on. The reader can be plugged into any of the a-c outlet terminals found at the base of each unit of the ENIAC. Power is supplied to the outlets below panel 2 of the printer and panel 3 of the constant transmitter only when the ENIAC's heaters are on; all

Table 8-1 - READER PROGRAM CONTROLS

Program Control	Location	Use
1) On-off switch	Reader	Turns reader's motor generator on or off. Green signal light is on when generator is running.
2) Initial Start Switch	Reader	Used to move first card of a deck into position for reading and to move last two cards through the reader.
3) Ri and start flip-flop and start relay.	Initiating Unit Constant Transmitter	When Ri is pulsed, start F.F. is set, start relay is activated, and card reading takes place subject to items 6, 7, and 8. Program output pulse is transmitted at the end of reading subject to items 9, 10, and 11.
4) Emergency Start Switch	Reader	Parallels the circuit of item 3. The reader continues to read subject to items 6, 7, 8 as long as this switch is closed. Does not usually cause the emission of a program output pulse when reading is completed since in the usual applications no interlock pulse is provided when this switch is used. It is chiefly used for testing the reader and constant transmitter.
5) Reader Start Button	Initiating Unit	Can be used to initiate the first card reading of a computation provided that the set-up does not call for a sequence in parallel with the first card reading. The initial start switch should be pushed immediately before or after the reader start button if all cards are in the magazine and there is not a card in position for reading.
6) Card Stacker Switch	Reader	Prevents operation of items 2-5 when card stacker is filled.
7) Mag. CLC and relay 1	Reader	Prevent card reading by items 3-5 when magazine is empty.
8) CLC No. 1 for CR No. 1 and relay 2	Reader	Prevent card reading by items 3-5 when there is no card before continuous roll 1.
9) CLC No. 1 for CR No. 2 and relay 60	Reader	Prevent reader from emitting a reset signal for the start F. F. and a finish signal if there is no card before continuous roll 2.
10) Relay 59	Reader	Prevents reader from emitting a reset or finish signal until the detail card following a master card passes under the read brushes associated with roll 2.
11) R1 and interlock flip-flop	Initiating unit	Note the reception of an interlock input pulse.
12) Finish flip-flop - Synchronizing flip-flop and Ro.	Initiating unit	Provide for the transmission of a program output pulse when reading, initiated by item 3, is completed provided that an interlock pulse is received. For reading initiated by item 5, program output pulse is transmitted 2 addition times after reading is completed.

other outlets are alive even when the heaters are off. Switching the on-off switch to the off position turns the reader's power off completely; the reader can be prevented from reading temporarily by holding down the stop key.

The foregoing reader controls and others still to be discussed are summarized in table 8-1.

8.1.1. Program Input and Output Circuits

The usual method for stimulating the reader to read a card in the course of a computation is to deliver a program pulse to Ri. A pulse received at Ri sets the reader flip-flop and, thus, causes the start relay to be activated. Now, with contacts 1A and 2A closed and with the card stacker switch closed, the circuit to relay 3 is closed through a contact on the start relay (shown on PX-11-307). When relay 3 is energized, the clutch magnets which cause the card feed mechanism to operate are activated. Notice that relay 3 can be activated as the result of the setting of the start flip-flop only if there is at least one card in the magazine (so that relay 1 is activated through Mag CLC), there is a card waiting to be read by the control brushes (so that relay 2 is activated through CLC No. 1 of CR No. 1) and, the card stacker is not filled to capacity (so that the card stacker switch is closed).

During the period 12.0 - 12.5 which is about 1/7th the way through a reading cycle, the reader emits (via line 129) a reset signal for the start flip-flop in the initiating unit provided that a detail, and not a master card, is passing under the read brushes and provided that there is a card in contact with CLC No. 1 of CR No. 2 (see Section 8.3.3.). After the start flip-flop is reset, if another pulse is received at Ri, this flip-flop is capable of remembering that another reading cycle is to take place after the completion of the one in which the reader is engaged. The operator is cautioned that a pulse delivered to Ri

before the start flip-flop has been reset is lost.

During the period 9.5 - 13.0, at the end of a card reading cycle, a finish signal is emitted by the reader (via line 127) provided that the card whose numerical reading is being completed is not a master card and provided that there is a card in front of continuous roll No. 2 waiting to be read (see Section 8.3.3.). The finish signal sets the reader finish flip-flop. When an interlock pulse is received and the interlock flip-flop, therefore, is set, gate 69 acting on the coincidence of signals from the finish and interlock flip-flops, emits a signal which allows a CPP to pass through gate 62. The output of gate 62 sets the reader synchronizing flip-flop. A CPP gated through gate 68 by the normally negative output of the synchronizing flip-flop resets the finish, interlock, and synchronizing flip-flops and passes through the reader program output transmitter to be emitted through Ro as a program output pulse.

Pushing the reader start button initiates the same actions as pulse input to Ri, but also sets the interlock flip-flop. Hence no interlock pulse need be provided to obtain a program output pulse for a reading initiated by this control.

The reader start button is intended for use at the start of a computation whose first program consists of card reading with no program sequence in parallel. Provision has been made for the setting of the interlock flip-flop by the reader start button since, with no parallel sequence for the first card reading, it would otherwise be impossible to provide the interlock pulse without which the reader does not emit a program output pulse (also see Section 8.1.3, for the procedure for reading the first card of a deck).

8.1.2. Emergency Start Switch

The emergency start switch parallels the operation of the circuit con-

sisting of Ri, the start flip-flop, and the start relay. As long as this switch is closed, relay 3 is activated under the same restrictions as were noted above in the discussion for the circuit which this switch parallels. Just as in that case, card reading takes place and a reset and a finish signal are emitted. The reset signal has no effect since the start flip-flop is not flipped into the abnormal state. The finish signal does, however, set the finish flip-flop. If an interlock pulse is not delivered to R1 for a reading initiated by the emergency start switch, no program output pulse is emitted by Ro even though the finish flip-flop is set. Since no output pulse is transmitted, the finish flip-flop is not reset. Therefore, reading initiated by the emergency start switch does not leave the reader program controls in their normal state.

In a reading initiated by the controls discussed in Section 8.1.1, the reader stops after one detail card or after the detail card following one or more master cards. When the emergency start switch is used, the reader continues to read as long as this switch is held closed.

The emergency start switch provides a convenient means of testing the reader and constant transmitter. It has the advantage that no program tray connections are needed. If, moreover, there is a problem set up for computation on the ENIAC when the reader is tested, the use of the emergency start switch has the advantage that no program output pulse to stimulate other programs is emitted when reading is completed (unless an interlock pulse is received).

8.1.3. Initial Start Switch - Procedure for reading the first card of a deck.

Above it was pointed out that not only must the magazine have cards in it and the card stacker not be filled to capacity, but also, there must be a card in position before continuous roll No. 1 for card reading to be stimulated by pulse input to Ri, by the reader start button, or by the emergency start switch.

When the first reading is to be stimulated with cards in the magazine but no card in contact with CLC No. 1 of CR No. 1, the initial start switch is used. When the initial start switch is closed, relay 3 is activated through contact 2B which is closed because there is no card in contact with CR No. 1, CLC No. 1. The first card of the deck is thus pushed under continuous roll No. 1 and read by the control brushes. If the initial start switch alone is pushed, then the reader stops before this first card goes through a numerical cycle. If the start flip-flop is set(by the reception of pulse at Ri or by pushing the reader start button) after the initial start switch is pushed, relay 3 is then activated through contacts 1A and 2A so that the first card goes through a numerical reading cycle. Reset and finish signals are emitted in the course of this cycle provided that the first card is not a master card.

If desired, the start flip-flop may be set first and then the initial start switch can be closed. This switch then causes the first card to go through a control brush reading. Since there is no card in contact with CR No. 2, CLC No. 1, relay 60 is not activated and therefore, no reset or finish signals are emitted in this reading cycle. The start flip-flop thus remains activated, and, relay 3 is then activated through contacts 1A and 2A. A cycle in which the first card is read for numerical data follows immediately and, provided that card No. 1 is not a master card, reset and finish signals are emitted.

Notice that relay 3 can be activated as a result of pushing the initial start switch only through contact 2B or the upper B contact of relay 1. Thus, the initial start switch can be used only when all cards are in the magazine so that 2B is closed or, at the end, when the magazine is empty so that the upper B contact of relay 1 is closed.

If n cards are placed in the magazine at the beginning of a computation,

the cycle in which card n-1 is read under continuous roll No. 1 and card n-2 under continuous roll No. 2 is the last cycle which can be initiated by pulse input to Ri, or by pushing either the reader start button or the emergency start switch. For, during this cycle, the n^{th} card moves out of the magazine into position before continuous roll No. 1. With the magazine empty, Mag CLC does not make contact and relay 1, therefore, is not activated so that the reading of cards n-1 and n could be brought about only by holding down the initial start switch. The necessity for using this switch to cause the reading of the 2 final cards of interest to the computation can, obviously, be avoided by placing at least 2 dummy cards at the bottom of the deck (which becomes the top of the deck when the cards are placed in the magazine - see the note on PX-11-309).

If blank cards are used at the end of a deck and if they are not withdrawn by the use of the initial start switch before the magazine is refilled, the operator should anticipate difficulty if the set-up is one in which the reader's program output pulse stimulates the divider and square rooter to carry out a division program for which the denominator is derived from the card just read. For, when the magazine is refilled, the blank cards remaining from the last deck are the first cards read and the output pulse emitted when one of these has been read causes the divider to embark on an infinite process, division by zero. This difficulty can be circumvented by causing the reader's program output pulse to be suppressed for the dummy cards. If the plug board is wired so that the reader can recognize master cards and if the dummy cards are punched with master card instructions (see Section 8.2.), no program output pulse will be emitted as long as the dummy cards are read since the reader does not emit either a reset or a finish signal for a cycle in which a master card passes under continuous roll No. 2 (see Section 8.3.3.).

8.2. POLARITY SWITCH AND PLUG BOARD

The IBM plug board is a characteristic device belonging to IBM units. It is a detachable board containing a large number of single hole terminals called hubs. When the board is in place for operation, these hubs are connected to some line in the permanent wiring of the machine. Numerous small insulated lengths of wire are provided by which these hubs may be connected in pairs (occasionally in larger groups), thereby connecting in each case two or more lines in the permanent wiring. This process is called wiring the plug board. It may be done in an enormous variety of ways, thus achieving corresponding flexibility in programming. The possibility of detaching the board as a whole from the machine not only facilitates the process of wiring, but, by the use of spare boards, enables one to keep on hand a number of boards with programs wired up.

The wiring of the plug board establishes, among other things, the correspondence between columns carrying certain data on the cards and the relays storing the same data in the constant transmitter. It provides also for storage relay groups which may be used for negative numbers in order to isolate minus indications from numerical data.

There is on the reader a polarity switch whose setting, in conjunction with the wiring, contributes to program control. Among the more important types of programming accomplished by the wiring of the reader plug board are those for reset control and group selection.

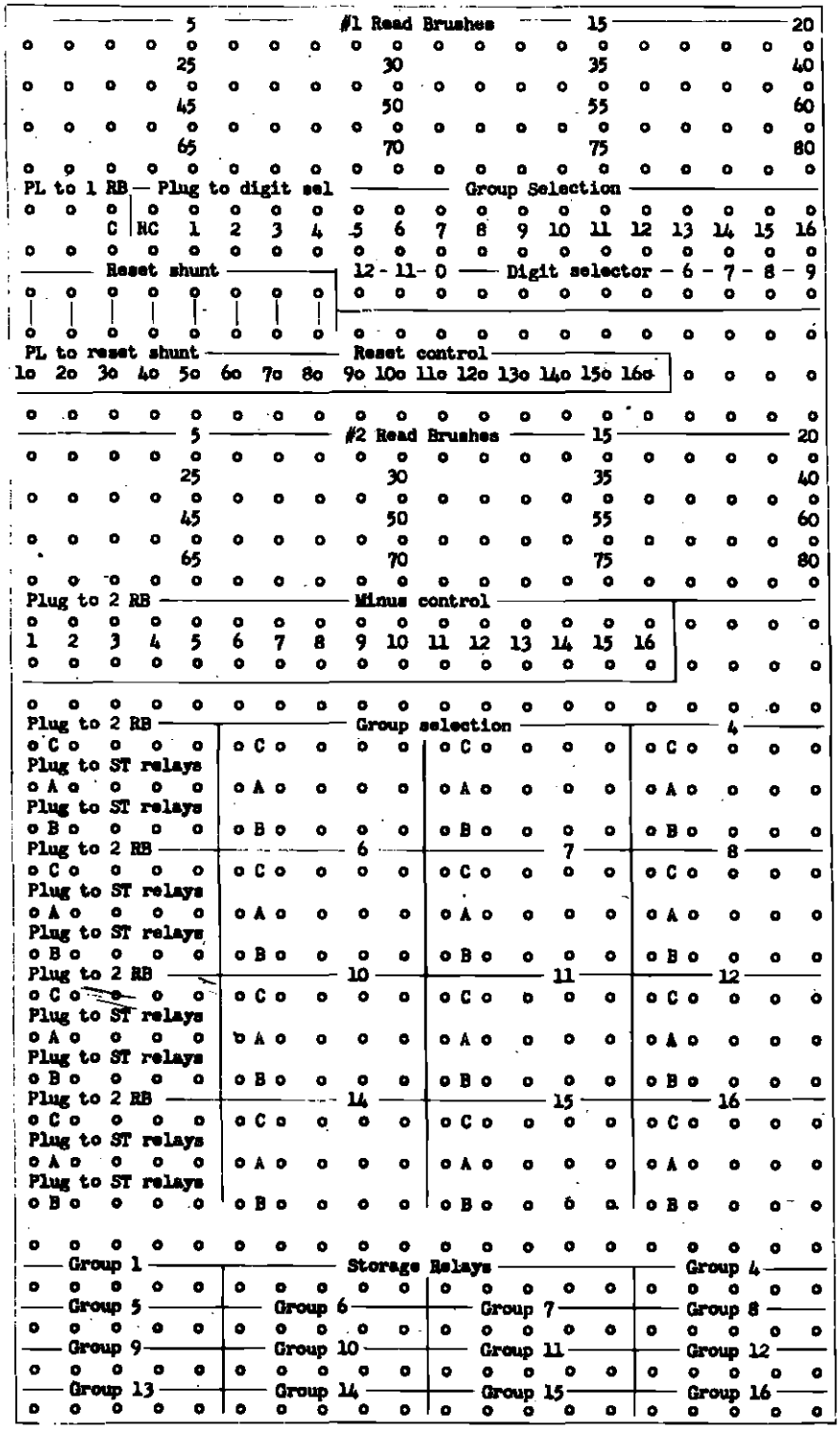
The IBM plug board for the reader is shown on PX-11-305. The various hubs are labelled on this diagram but certain additional words of explanation may be helpful.

The No. 1 read brush hubs appear in lines 1-4 of the plug board. These

TABLE 8-2

CORRESPONDENCE BETWEEN STORAGE RELAY HUBS AND POINTS ON CONSTANT SELECTOR SWITCHES

Storage Relay Group	Point on C.S.Switch	Storage Relay Group	Point on C.S.Switch	Storage Relay Group	Point on C.S.Switch	Storage Relay Group	Point on C.S.Switch
1	A_L	2	B_L	3	C_L	4	D_L
5	E_L	6	F_L	7	G_L	8	H_L
9	A_R	10	B_R	11	C_R	12	D_R
13	E_R	14	F_R	15	G_R	16	H_R



IBM READER
PLUG BOARD
PX-11-305R

hubs connect to the control brushes and their numbering corresponds to that of the columns on an IBM card.

The two hubs on lines 5 and 6 which are above and below the letter C, are common, i.e., internally connected. One or both of these hubs may be used for control purposes. The hubs to the left of the C hubs are unused.

The single hub marked RC on line 6, the 16 reset shunt hubs which appear at the left of lines 7 and 8, and the reset control hubs on line 9 are used for the reset control programming instructions discussed below. The numbering of the reset control hubs corresponds to the numbering of the 16 five digit groups of storage relays in the constant transmitter (see Table 8-2).

The group selection hubs on lines 5 and 6 which are common hubs and those on lines 18-29 are used for group selection instructions as explained later in this section. The group selection hubs on lines 18-29 are arranged in 16 five digit groups. For each digit there are three hubs, C, A, and B. When group selection (see below) takes place the C and B hubs are internally connected; otherwise C and A are connected. Each of the group selection hubs above a number on line 5 is common with the hub below the same number on line 6. Each pair of hubs on lines 5 and 6 corresponds to the A-B-C group of the same number on lines 18-29.

The minus control hubs appear on lines 15 and 16. Each hub above a number is common with the one below the same number. Minus punch information is routed through these hubs to the PM' and PM" relays of the correspondingly numbered groups in the constant transmitter.

The No. 2 read brush hubs are the outputs of the No. 2 read brushes. Numerical data read from any of the 80 columns of an IBM card is delivered to the correspondingly numbered hub of this group.

The storage relay hubs on lines 31-34 connect to contacts on the constant transmitter's coding relays and ultimately to the storage relays. The correspondence between the numbering of the 16 five digit groups here and the labelling of the points on the constant selector switches is shown in Table 8-2.

The two kinds of programming instruction which the reader recognizes are reset control and group selection. The reset control instruction refers to distinguishing between master and detail cards. As long as detail cards are read, the reader causes information stored in the storage relays as a result of the reading of the previous detail card to be dropped out before new detail information is stored, and also causes information stored in the storage relays as a result of the reading of the last master card to be retained (provided the plug board is so wired). Reset control operates when a master card is read. This means that the reader causes all information, both master and detail, to be dropped out of the storage relays and new master information from the master card to be placed in storage. Also, when reset control takes place, the card following the master card (usually a detail card) is read immediately after the master card. No reset or finish signal is emitted until the reading of a card is completed.

The group selection instruction, which may be given for either a master or detail card, makes it possible for data from one field to be placed normally in certain storage relays, and, when group selection operates, in a different group of storage relays.

A second form of group selection instruction is used when it is desired to store in one set of storage relays information which normally occurs in a given field of the card, but which is found in a different field of the card when group selection is to occur.

The first form of group selection is convenient when using a set of cards, perhaps master and detail, which are so punched that the same field used for master information on the master card, on the detail card is used for detail information. The second form of group selection would be useful for a set of cards consisting of two subsets in which there appeared data for the same quantity sometimes in one field and sometimes in another.

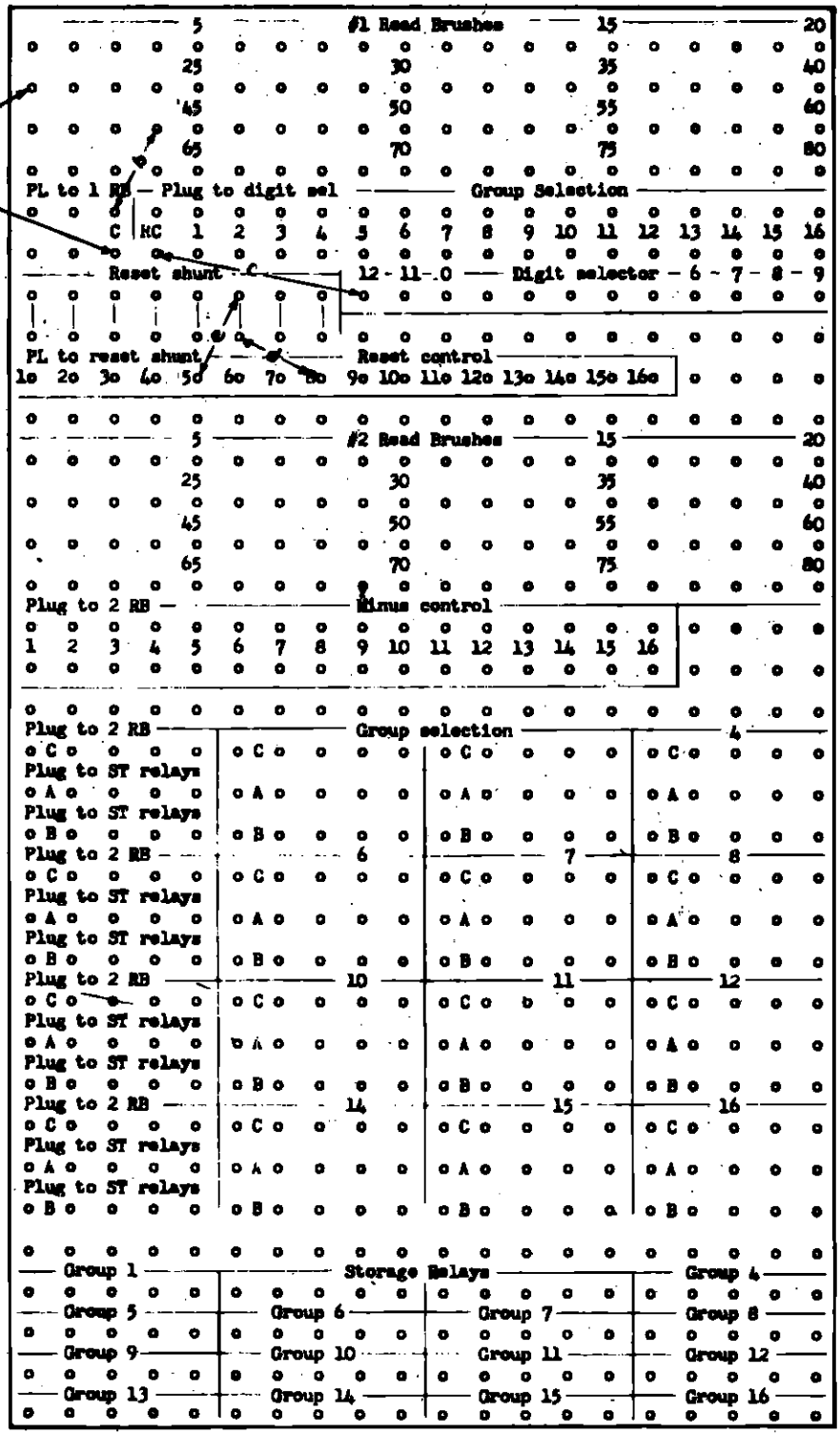
The polarity switch has two positions, normal and abnormal. With the polarity switch in the normal position, programming instructions for reset control and/or group selection are always specified in a given column of the card with different instructions being specified by different punches. With the polarity switch in the abnormal position, programming instructions are given by a specific punch with the different instructions being distinguished by the different columns in which the specific punch appears. The polarity switch makes possible this flexibility by interchanging the connections to the source of power so as to make the polarity consistent with plug board wiring. It is important to note that the setting of the polarity switch must not be altered when the reader's motor generator is on (green signal light is on).

With the polarity switch in the normal position, the column which is to contain punches for programming instructions is specified by plugging from one of the C hubs to the No. 1 read brush hub corresponding to that column. If desired, the control punch may appear in either column i or j. This latter instruction is specified by plugging one of the common C hubs to the i hub and the other C hub to the j hub of the No. 1 read brushes.

The particular punch appearing in the given column (or columns) which is to signal for reset control is specified by plugging from the RC hub to the digit selector hub corresponding to the particular punch. A punch read no later

IBM READER PLUG BOARD

Illustrative plugging arrangement for Reset Control Instructions with the Polarity Switch in the Normal Position.



INSTRUCTIONS

(The line which carries the instruction appears in parenthesis)

When a 12 punch (c) appears in column 21 (a) or in column 44 (b), reset control is to operate (c). The reset control consists of dropping out the master information stored in group 5 (e) and group 8 (d) storage relays.

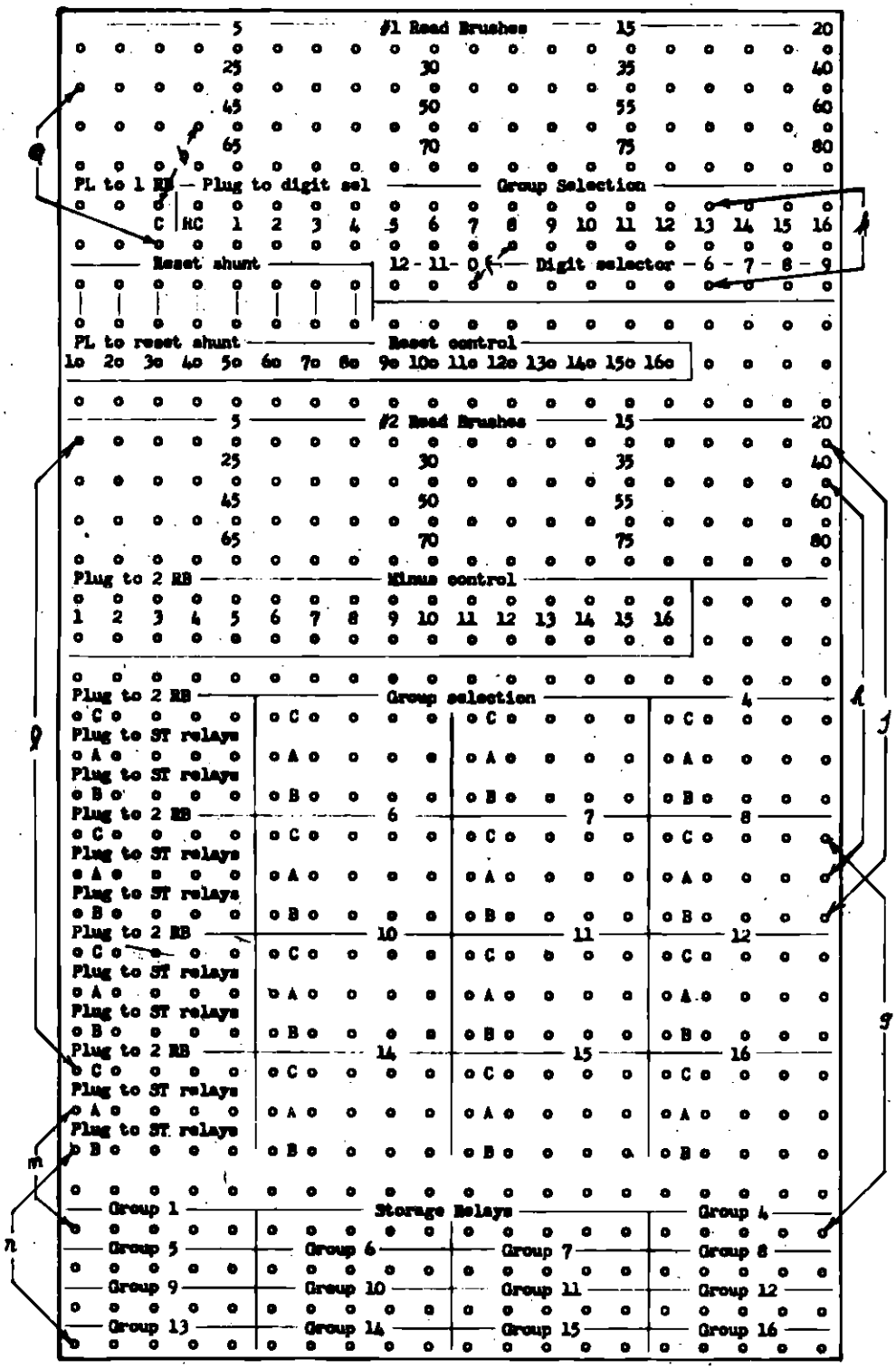
IBM READER PLUG BOARD PX-11-30521

in the card reading cycle than a 6 punch should be used to stimulate reset control in order to allow sufficient time for the reset control programming circuits to function properly (see Section 8.3.1.). Finally, the master information group* (or groups) is (or are) specified by plugging from the reset control hubs correlated with the group (or groups) to any of the reset shunt hubs. Drawing PX-11-305 R1 presents an illustrative plugging for reset control instructions when the polarity switch is in the normal position.

With the polarity switch in the normal position, the particular punch (in the column or columns specified by the plugging from C to the No. 1 read brushes) which gives a group selection instruction is specified by the plugging from the digit selector hubs to the group selection hubs immediately above. The card fields and storage relay groups involved in the group selection and the manner in which they are involved are designated by the plugging from the No. 2 read brushes to the group selection hubs on lines 18-29 (corresponding to the ones used on lines 5 and/or 6) and then from these hubs to the storage relay hubs. Group selection in which data from either of 2 fields on the card is placed in a single storage relay group is provided for by plugging the 5 hubs of the storage relay group to the C hub of the group selection hubs and by plugging the five No. 2 read brush hubs from which data is normally taken to the A hubs and the five No. 2 read brushehubs from which data is taken when group selection occurs to the B hubs of the group selection hubs on lines 18-29. Group selection in which data from one field on the card is ordinarily put in one group of storage relays but in another group when group selection takes place is specified by plugging the No. 2 brush hubs for the card field to the C hubs and the A hubs of the group selection relays to the usual storage relay hubs and the B hubs to the hubs of the storage relays used when group selection takes place.

*Master information group is used to mean the group of constant transmitter storage relays which stores information from a master card, releasing it only when a new master card is recognized.

Illustrative plugging arrangement for Group Selection Instructions with the Polarity Switch in the Normal Position,



INSTRUCTIONS

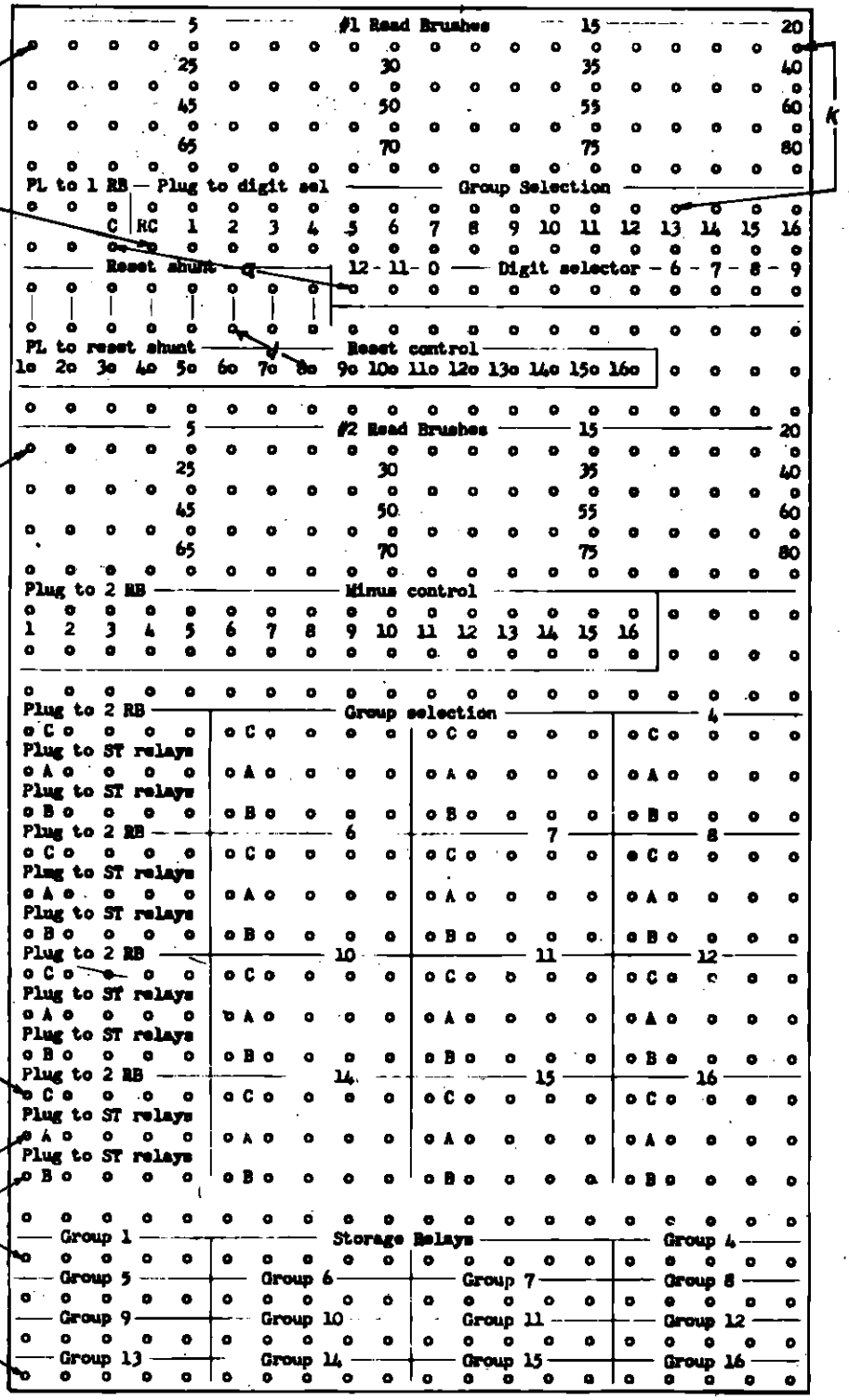
When a 0 punch (f) appears in either column 21 (a) or column 44 (b), the 5th digit of group 4 storage relays (g) will come from column 20 of the card (j). Otherwise, the 5th digit of group 4 storage relays will come from column 40 of the card (h).

When a 6 punch (k) appears in either column 21 (a) or column 44 (b), the digit appearing in column 1 of the card (l), will be put in the storage relays for the first digit of group 13 (n); otherwise it will be put in the storage relays for the first digit of group 1 (m).

IBM READER PLUG BOARD PX-11-3052

IBM READER PLUG BOARD

Illustrative plugging arrangement for Reset Control and Group Selection Instructions with the Polarity Switch in the abnormal position.



INSTRUCTIONS

When a 12 punch (a) appears in column 1 (c), reset control (c) takes place for the group 8 storage relays (d).

When a 12 punch (a) appears in column 20 (k), then data from column 1 on the card (l) is put in the first digit storage relays for group 13 (n). Otherwise data from column 1 is put in the storage relays for the first digit of group 1 (m).

IBM READER PLUG BOARD PX-11-305 R3

PX-11-305 R2 illustrates plugging for both types of group selection if the polarity switch is in the normal position. It is to be noted, incidentally, that group selection for more than one group may be made to depend on the appearance of a given punch in the control column. For example, if group selection for groups 12 and 13 were desired on the presence of a 6 punch, this could be specified by making connection k as shown on PX-11-305 R2 and, in addition, cross connecting the other group selection hub 13 to either of the group selection hubs numbered 12.

With the polarity switch in the abnormal position, control is indicated by a specific punch and the different forms of control by the various columns in which the specific punch occurs. The particular punch is designated by plugging from one of the C hubs to the digit selector hub corresponding to that punch. The fact that reset control is to take place because this special punch occurs in a given column of the card is indicated by connecting the RC hub to the No.1 read brush corresponding to that column. A connection from a group selection hub to a read brush hub indicates that group selection is to take place when the particular punch appears in the column corresponding to the No. 1 read brush hub. PX-11-305 R3 shows a plug board arrangement for programming instructions when the polarity switch is in the abnormal position.

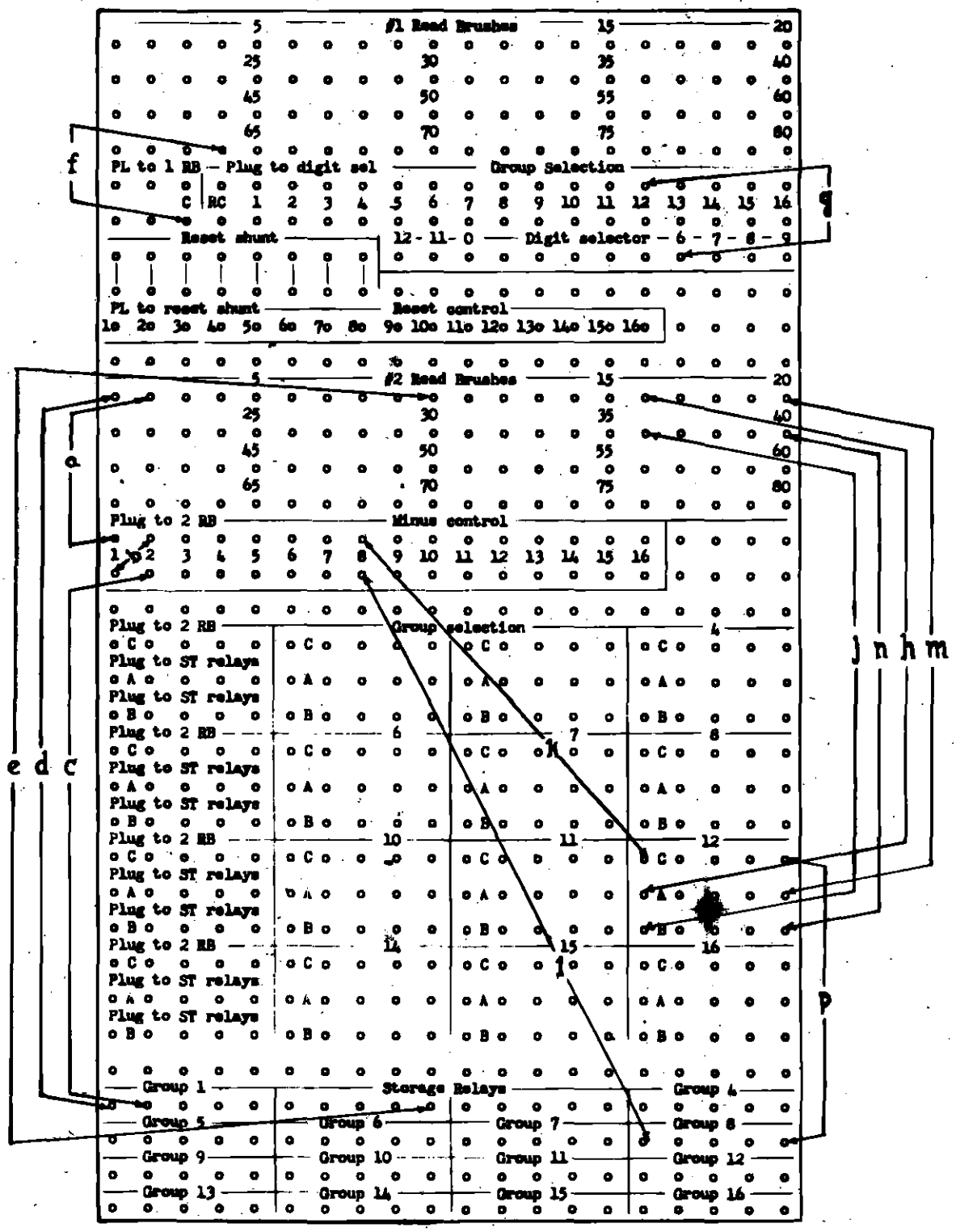
The No.2 read brush hubs associated with card fields used for positive numbers only may be plugged to the storage relay hubs directly or through the group selection hubs in any manner desired. Card fields which at some time carry negative numbers require special minus control wiring of the plug board so that minus sign indication can be delivered to the PM' and PM" relays in the constant transmitter and so that the digital information appearing in the same column can be delivered to the proper storage relays.

Minus control plugging consists of connecting the No.2 read brush hub associated with the column in which the minus punch appears to all the minus

ILLUSTRATIVE PLUG BOARD CONNECTIONS

For

CARD FIELDS STORING NEGATIVE NUMBERS



Lines (a), (b), (c), (d), (e) illustrate plugging for a 10 digit negative number which occupies group 1 and 2 storage relays. Since the minus punch is assumed to come from column 2 of the cord, hub 2 of the #2 read brushes is connected to a minus control hub for group 1 (a). Because storage relay groups 1 and 2 are used for this number, the other minus control hub for group 1 is cross connected to a minus control hub for group 2 (b). The other minus control hub for group 2 is connected to the hub for the 2nd digit of group 1 storage relays. Lines (d) and (e) show the plugging for the first and last digits.

Lines (h), (j), (k), (l), (m), (n), (p) illustrate plugging for a 5 digit negative number, in which the minus punch appears in the same card column as the first digit and for which group selection occurs.

IBM READER PLUG BOARD PX-11-305R4

control hubs having the same numbers as the groups of storage relays in which the information from that card field is stored and then connecting from these minus control hubs to the storage relay hub corresponding to the storage position of the numerical data in the column containing the minus punch. The No.2 read brush hubs for the columns of the same field which do not carry a minus punch are plugged directly to the appropriate storage relays.

Where group selection intervenes between the No.2 read brushes and the storage relays, in the "C to No.2 read brushes - A and B to storage relay" type of group selection, minus control plugging is conveniently done from No. 2 read brush to minus control hub (or hubs) to C group selection hub and then from A or B hub to storage relay hub. In the "C to storage relay - A and B to No2 read brush" type of group selection, minus control plugging may be carried out from C hub to minus control hub (or hubs) and then to storage relay hub. An illustrative plug board arrangement for minus control plugging is shown on PX-11-305 R4.

8.3. PROGRAMMING CIRCUITS OF THE READER (Refer to PX-11-119 and PX-11-309)

The programming circuits of the reader consist of the reset control, group selection, reset signal, and finish signal circuits. The discussion for the first 2 circuits will be made with the assumption that the polarity switch is in the normal position and that the plug board is wired accordingly.

8.3.1. Reset Control Circuits

Information remains stored in the 16 groups of storage relays in the constant transmitter by virtue of the signals delivered over lines 81-96 when the corresponding contacts on the storage holding relays 4-6 are closed. Relays 4-6 are activated during period 11.0 through 13.7 while cam P2 makes contact. When P2 breaks at 13.7, contacts on all the storage holding relays release so that

at this time information is always dropped out of all storage relay groups for which a shunt connection has not been made from reset control hubs to reset shunt hubs on the plug board. The contacts on all the reset shunt relays 56-58 remain closed and thus cause the retention of information in the storage relay groups which they control by reason of plug board wiring. The contacts on relays 56-58 release to allow information in these storage relay groups to be dropped out only when relays 56-58 are activated.

When a master card is read relays 56-58 are activated through the interaction of the control brushes, the emitter, and reset control relay 23. The emitter has a moving arm which makes contact with the 12 digit selector hubs in synchronism with the reading of the corresponding punches on the card.

In reset control plugging, it is to be recalled, a connection is made between a control brush hub and the C hub which is internally connected to the pick up coil of R23 and to the RC hub and also between the RC hub and a digit selector hub which is internally connected to the emitter. The signal on this line when the reset control punch is read causes the pick up coil of R23 to be picked up. The hold coil of R23 holds until cam P5 breaks contact at time 13.7. While R23 is activated, contact B of this relay is closed so that relays 56-58 pick up when cam P8 makes contact at time 8. These relays hold until cam P9 breaks at 12.5. Thus, in the period that relays 56-58 are activated the contacts on these relays used for reset shunting are open so that information is dropped out of the storage relays holding master information as well as out of the detail information groups. The timing of the events discussed above is shown on PX-11-308.

The fact that relay 57 is activated when reset control takes place also has repercussions on the reset and finish signal circuits which will be discussed in Section 8.3.3.

From the time that Ri is pulsed for the reading of card i + 1 until 13.7 in the cycle for card i + 1 when data from card i is dropped out, the constant transmitter may be called on to transmit data from card i. This period can safely be taken as 50 addition times.

8.3.2. Group Selection Circuits

There are two sets of group selector relays, 7-22 and 24-55. Each of relays 7-22 controls a pair consisting of an even and the immediately succeeding odd numbered relay of the collection 24-55. Three contacts of each even numbered relay and two of each odd numbered relay of the collection 24-55 are used to produce a circuit between the B and C hubs (instead of between the A and C hubs) of a five digit group when one of the relays 7-22 and, thus, a pair of the relays 24-55 is activated.

Group selection plugging from a control brush hub to a C hub which is internally connected to the pick-up coils of relays 7-22 each of which, in turn, is connected internally to one of the group selector hubs (1-16) and, thence, by plug board connection to a digit selector hub and finally to the emitter allows the signal which occurs when a group selection punch is read to pick up the appropriate relay of the assemblage 7-22. Once picked up, such a relay (or relays) holds until cam P5 breaks contact at 13.7. While one of the relays 7-22 is activated the corresponding pair of relays of the 24-55 collection is activated through the B contact of its controlling relay when cam P6 makes contact at time 9.7. This pair of relays then holds until time 9.5 (when cam P7 breaks contact) of the reading cycle following the one in which the group selection punch is recognized. Thus, in the numerical reading cycle of a card for which group selection takes place, the circuit between read brushes for groups effected by group selection and storage relays is by the B-C route instead of the A-C route.

The timing of the events described above is shown on PX-11-308 where it is assumed that group selection is stimulated by some punch on master card m.

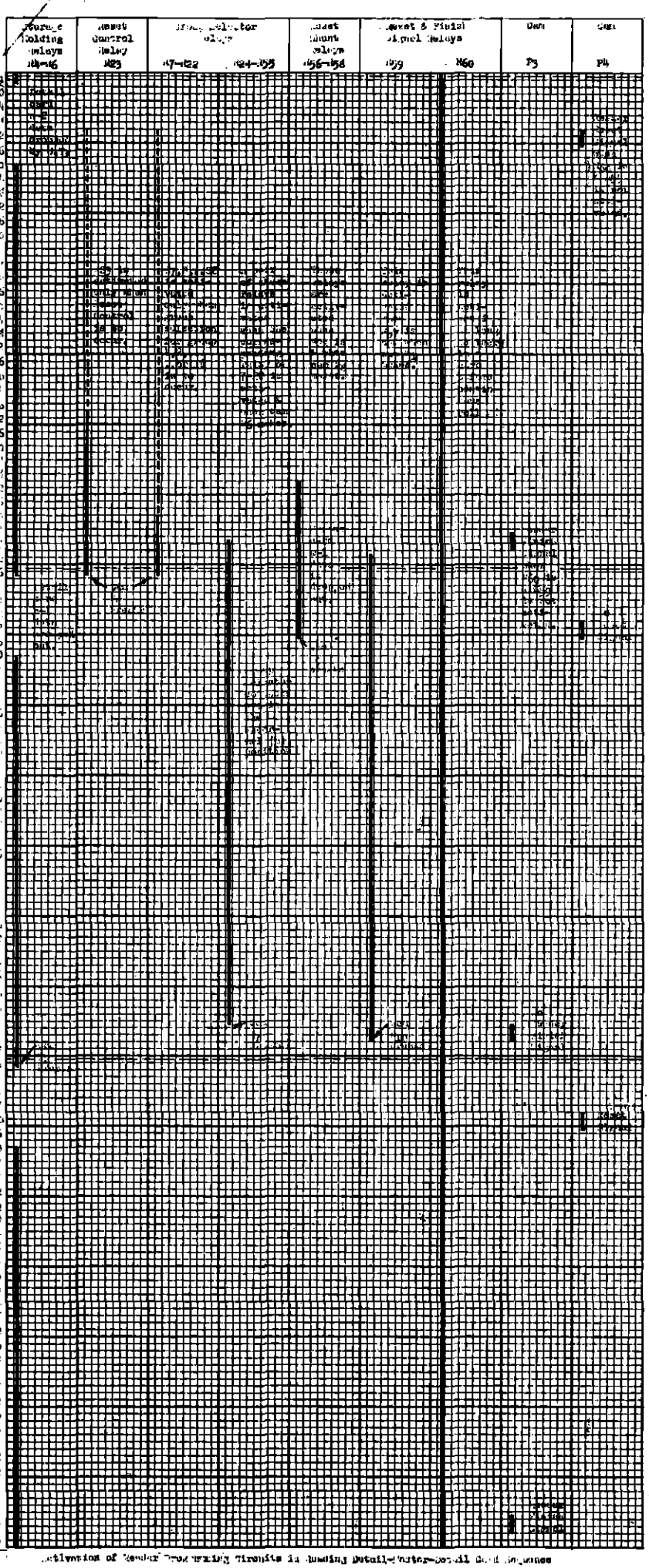
8.3.3. Reset and Finish Signal Circuits

Provided that relay 60 is activated and relay 59 is not, a reset signal is emitted via line 129 during the period 12.0 - 12.5 when cam P4 makes, and a finish signal is emitted via line 127 during the period 9.5 - 13 when cam P3 makes.

Relay 59 is activated when cam P1 makes (13.1 - 14.9) through contact R-57 AU provided that relay 57 has been activated; R59 holds until 13.0 when cam P10 breaks. Now, in Section 8.3.1, it was pointed out that relay 57 is activated during the period 8.0 - 12.5 which is the end of the control reading cycle and the beginning of the numerical cycle for a master card. Thus, when cam P4 makes during 12.0 - 12.5 and a master card is entering its numerical cycle, no reset signal is emitted. Recalling the discussion in Section 8.1, concerning the reader program controls in the initiating unit, one can see that since the start flip-flop is not reset, the start relay remains activated (until a reset signal is emitted during 12.0 - 12.5 in the next reading cycle) and that the reader, therefore, proceeds with a cycle following the one in which numerical data is read from the master card before it stops.

Similarly, since relay 59 remains activated through time 13.0 of the numerical reading cycle for a master card, no finish signal is emitted and therefore no program output pulse can be emitted through Ro on the initiating unit until the reader has gone through a numerical reading cycle for the detail card following the master card.

The timing of the activation of the various elements involved in producing reset and finish signals when a sequence consisting of detail-master-detail



Activation of Reader Processing Circuits in Reading Details of Interpretation Card Columns

cards is read is shown on PX-11-308.

Relay 60 is not activated when there is not a card in position to move under continuous roll No. 2 (i.e. when CR No. 2, CLC No. 1 is open). This circumstance can arise when a card jams in passing under continuous roll No.1,when the reader is started (from rest) by pushing the reader start button or by the reception of a pulse at Ri and then depressing the initial start key (see Section 8.1.3.), or when the last card of a deck is passing under continuous roll No. 2.

The previous discussion may be summarized as follows: In general, when a detail card passes under continuous roll No. 2, the reader emits a reset signal during the period 12.0 - 12.5 of the cycle or when the card reading cycle is about 1/7th completed. This signal resets the start flip-flop so that subsequent to the reset signal, this flip-flop is capable of noting the reception of a program pulse by Ri. With a safety factor included, about 750 addition times should be allowed from the time that Ri is stimulated until it is stimulated again if all cards ir a deck are detail cards. Also, a finish signal is emitted at the end of every cycle in which a detail card is scanned by the read brushes. Thus, about 2500 addition times elapse between the time when a detail card reading cycle commences and a program output pulse is emitted (provided that an interlock pulse has been received).

No reset or finish signals are emitted in the numerical cycle for a master card. These signals are, however, emitted during the numerical cycle for the detail card following a master card. When decks containing both master and detail cards are used, approximately 3200 addition times may elapse between the reception of a program input pulse at Ri and the resetting of the start flip-flop and a program output pulse may not be emitted until about 4400 addition times (as many as 2500 addition times for the reading of the master card and about 1900 for the detail card) after reading is stimulated.

No reset or finish signals are emitted if a card jams in passing under continuous roll No. 1 and no finish signal is emitted for the last card of a deck.

8.4. NUMERICAL CIRCUITS OF THE READER

The circuits in the reader which are used for numerical purposes are:

1) coding cams CB1-CB8 which emit signals to activate the coding relays in the constant transmitter via lines 115-122 (see PX-11-119)
2) coding cam CB9 which activates the constant transmitter's PM isolating relays by means of a signal carried on line 114
3) the read brushes which, by means of plug board wiring to the storage relay hubs, remit numerical indication signals over lines 1-80 to contacts on the coding relays and thence to the storage relays and which, by means of plug board wiring to the minus control hubs, remit minus indication signals over lines 97-112 to the PM' and PM" relays in the constant transmitter.

These circuits will be discussed in greater detail in Section 8.6, NUMERICAL CIRCUITS OF THE CONSTANT TRANSMITTER.

8.5. PROGRAM CONTROLS AND PROGRAMMING CIRCUITS OF THE CONSTANT TRANSMITTER

The 30 program controls (see PX-11-307 and 11-302) of the constant transmitter, each consisting of a transceiver, program pulse input and output terminals, and a constant selector switch, are subdivided into 5 groups of 6 program controls each. Groups 1 through 5 respectively consist of the following program controls 1-6, 7-12, 13-18, 19-25, and 25-30. The 30 transceiver neons associated with the program controls are shown on PX-11-306.

Each constant selector switch of a group of 6 is connected in parallel with the other 5 switches of the group to the programming circuits which elect for transmission a signed 5 or 10 digit number from among the 4 signs and 20 digits controlled by that group. For example, any of the first six switches can be used to select for transmission either of the signed ten digit numbers A_{LR} or B_{LR} or one of the 4 signed five digit numbers, A_L, A_R, B_L, or B_R. However, because of the way these six switches are connected in parallel, it is not possible to elect the transmission of a signed 5 digit L or R group on one switch and the transmission of the signed 10 digit LR group having the same letter on another switch.

For each 5 digit group (whether read from cards or set up manually) there are 20 constant selector gates (4 gates per digit). For the first 5 digits in the storage relays, for example, these gates are numbered B' - L' 1 and B' - L' 21 (see PX-11-307). These gates emit a signal on the coincidence of a signal from a constant selector switch and the activation of the storage relay to which the constant selector gate is connected or on the coincidence of a signal from a constant selector switch and a signal from one of the constant switches.

Also associated with each 5 digit card group is a minus selector gate and a complement correction selector gate. Each 5 digit group that can be set up on the switches located on panel 2 of the constant transmitter has a minus selector gate but not a complement correction selector gate.

These gates emit signals on the coincidence of a signal from a constant selector switch and a signal from either a minus setting on a PM set switch or from an activated PM' or PM" relay. The minus selector gates control the putting in of the 9P for sign indication when a negative number is transmitted and the complement correction selector gates control the putting in of the 1'P needed to make a tens complement when a number punched on a card as a negative number

TABLE 8-3

GATES CONTROLLED BY POINTS ON FIRST 6 CONSTANT SELECTOR SWITCHES.

POINT	GATES CONTROLLED BY FIRST DECK	FUNCTION OF GATE	GATES CONTROLLED BY SECOND DECK	FUNCTION OF GATE
A_L	A'1 (2nd input from PM relay for A_L group)	L M S	B' - L' 1	constant selection for group A_L
			BI - L' 21	
	A'21 (2nd input from PM relay for A_L group)	L C C S	(2nd inputs from storage relays)	
A_R	A'41 (2nd input from PM relay for A_R group)	R M S	B' - L' 41	constant selection for group A_R
			B' - L' 61	
			A' 61 (2nd input from PM relay for A_R group)	R C C S
A_{LR}	A'1	L M S	B' - L' 1 B' - L' 21	constant selection for group A_L
			B' - L' 41 B' - L' 61	constant selection for group A_R
			A' 61	R C C S
B_L	A'2	L M S	B' - L' 2	constant selection for group B_L
	A'22	L C C S	B' - L" 22	
B_R	A'42	R M S	B' - L' 42 B' - L' 62	constant selection for group B_R
B_{LR}	A' 2	L M S	B' - L' 2 B' - L' 22	constant selection for group B_L
			B' - L' 42 B' - L' 62	constant selection for group B_R
			A' 62	R C C S

is emitted from the constant transmitter. Negative numbers are set up as tens complements on the switches of panel 2 so that no complement correction selector gates had to be provided for those groups.

Associated with the five-digit groups having subscript L are left minus selector (LMS) and, in the case of card groups, left complement correction selector (LCCS) gates; while the groups with subscript R have right minus selector (RMS) and right complement correction selector (RCCS) gates. The 10 digit LR groups have LMS gates and RCCS gates. The LMS gates control the passing of the 9P to only the PM lead; the RMS gates, to the PM lead and 5 left hand places as well. The LCCS gates or RCCS gates respectively control the putting in of the 1'P in the 5th or 10th decade place from the left.

When a constant transmitter program control is stimulated, signals from the 2 decks of the control's constant selector switch are delivered to the appropriate constant, minus, and complement correction selector gates. Table 8-3 illustrates how the points on the first 6 constant selector switches are connected to the various selector gates. The question of how the selector gates affect the digit pulses emitted from the digit output terminal will be taken up in Section 8.6.2.

The constant chosen for transmission is emitted through the digit output terminal on panel 1 of the constant transmitter during the 20 pulse time period following the reception of the program input pulse. The program control used emits a program output pulse at the end of the addition time in which the constant is transmitted.

The constant transmitter can be stimulated to transmit a constant stored on the manual set switches at any time in the course of a computation. Constants read from a given card can be called for any time in the period between the pro-

gram output pulse emitted by the reader when that card is read and 50 addition times after the reader is stimulated to read the succeeding card (see Section 8.3.1).

In general, only one program control on the constant transmitter can be stimulated in a given addition time. Circumstances may, however, arise in which the operator would desire to stimulate two program controls simultaneously.

Consider, for example, a set-up in which the following rather particularized conditions are found:

1) accumulator program controls are nearly exhausted
2) 5 digit numbers are used
3) both arguments for a multiplication program are derived from the constant transmitter.

If the normal method of using the constant transmitter were used, both the ier and icand for the multiplication could not be transmitted simultaneously from the constant transmitter and received in the argument accumulators by means of the semi-permanent programming connections (Rα-Rε and Dα-Dε). Therefore, an additional program control on one of the argument accumulators would have to be expended. Under certain specialized conditions which do not conflict with the way in which the leads of the digit output terminals are used (see Section 8.6.2.1), two constant transmitter program controls can be stimulated simultaneously provided that a total of no more than 10 digits and a PM are called for.

Another special case which can arise is that the constant transmitter's program controls may not be adequate in number for some set-up. Under certain circumstances (see Section 8.6.2.1.) the LR setting of a constant selector switch makes it possible to obtain 2 five digit constants at the expense of only one program control.* This procedure, however, must never be used if at any other time in

*Another way to circumvent a shortage of constant transmitter program controls is, of course, to make use of the master programmer.

the computation the L or R group identified by the same letter A, B, ..., K is called for separately as mentioned earlier in this section.

8.6. NUMERICAL CIRCUITS OF THE CONSTANT TRANSMITTER

8.6.1. Storing Information from Cards in the Constant Transmitter

Digital information is stored in five-digit blocks each using 5 groups consisting of 4 storage relays each. PM indication for each 5 - digit block is stored in the associated PM' and PM" relays. Each storage relay bears the designation i-j where i identifies the particular one of 80 digits and where j has the value 1, 2, 2' or 4 of the pulse code in which the digits are transmitted from the constant transmitter. The digits read from a card are coded in the 1, 2, 2', 4 code by means of coding cams in the reader and the PM, isolating PM' and PM", and coding relays in the constant transmitter before being put in storage.

The pick up coils of the 6 PM isolating relays are connected via line 114 to coding cam CB9 which makes contact while PM punches are read (see PX-11-307). The PM' and PM" relays for each 5-digit block are connected through a contact on one of the PM isolating relays (labelled R on the schematic diagram shown on PX-11-116) to the line (97-112) which carries the minus indication signal for that block of digits. If a minus punch is read for the group, the PM' and PM" pick up and hold until information is dropped out when a new card is read or when reset control takes place. Since the isolating relay contact is closed only during the period 14.5 - 11.5, digit information punched in the same column as a minus punch cannot activate the PM' and PM" relays.

The pair of PM relays serves not only to remember sign indication, but also aids in converting true negative numbers on the cards to nines complements. When the PM relays are activated by a minus punch, the coding relays (C_1-C_8) used

TABLE 8-4 - ACTIVATION OF CONSTANT TRANSMITTER STORAGE RELAYS

Punch	Energized Coding Cams	Activated Coding Relays	Activated Storage Relays
0	none		
-0	CB1 CB3 CB5 CB7	C_1 or C_2 C_3 or C_4 C_5 or C_6 C_7 or C_8	1 2 2' 4
+1	CB2	C_1 or C_2	1
-1	CB3 CB5 CB7	C_3 or C_4 C_5 or C_6 C_7 or C_8	2 2' 4
+2	CB4	C_3 or C_4	2
-2	CB1 CB3 CB7	C_1 or C_2 C_3 or C_4 C_7 or C_8	1 2 4
+3	CB2 CB4	C_1 or C_2 C_3 or C_4	1 2
-3	CB5 CB7	C_3 or C_4 C_7 or C_8	2 4
+4	CB8	C_7 or C_8	4
-4	CB1 CB7	C_1 or C_2 C_7 or C_8	1 4
+5	CB2 CB8	C_1 or C_2 C_7 or C_8	1 4
-5	CB7	C_7 or C_8	4
+6	CB4 CB8	C_3 or C_4 C_7 or C_8	2 4
-6	CB1 CB3	C_1 or C_2 C_3 or C_4	1 2
+7	CB2 CB4 CB8	C_1 or C_2 C_3 or C_4 C_7 or C_8	1 2 4
-7	CB3	C_3 or C_4	2
+8	CB4 CB6 CB8	C_3 or C_4 C_5 or C_6 C_7 or C_8	2 2' 4
-8	CB1	C_1 or C_2	1
+9	CB2 CB4 CB6 CB8	C_1 or C_2 C_3 or C_4 C_5 or C_6 C_7 or C_8	1 2 2' 4
-9	none		

for a five digit block are connected to the odd numbered coding cams. Otherwise the coding relays are connected to the even numbered coding cams.

Each of the 4 coding cams CB1, CB3, CB5, and CB7 or CB2, CB4, CB6, and CB8 is connected through contacts on the PM' and PM" relays to the pick up coils of a pair of coding relays (one even numbered and one odd numbered relay). Various combinations of the coding cams make contact as the different digit punches are read by the read brushes (see the coding cam time table and Table 8-4). When a coding cam makes contact it activates the pair of coding relays to which it is connected. The coding relay picks up and holds as long as the associated coding cam makes contact.

A signal for a punch appearing in one of the first 3 places of a 5-digit block is delivered to one contact on each of the odd numbered coding relays and a signal for either of the 2 remaining places of the block to a contact on the even numbered coding relays. Only the contacts on relays activated at the particular time when the punch is read are closed so as to allow the punch signals to reach the storage relays.

A signal carried on the i lead (i=1, 2, ..., 80) and passing through a contact on coding relay C_1 or C_2 sets up the i-1 storage relays; a signal through a contact on coding relays C_3 or C_4, the i-2 relays; a signal through a contact on C_5 or C_6, the i-2' relay; and a signal through a contact on C_7 or C_8, the i-4 relay. Table 8-4 shows which coding cams are energized as the different punches are read, the coding relays that are activated as a result, and the storage relays which are set up when a given line is passing over the read brushes if such a punch appears in a column of the card. The hold contacts on the storage relays for groups A_L through H_R are connected to lines 81-96 respectively so that, once set up, these relays hold until a new card is read or until reset control takes

TABLE 8-5

USE OF DIGIT OUTPUT LEADS FOR CONSTANT SELECTOR SWITCH SETTINGS L, R, or LR

Lead	L	R	LR
PM	0 or 9 sign pulses	0 or 9 sign pulses	0 or 9 sign pulses
10	digit pulses	0 or 9 sign pulses	digit pulses
9	digit pulses	0 or 9 sign pulses	digit pulses
8	digit pulses	0 or 9 sign pulses	digit pulses
7	digit pulses	0 or 9 sign pulses	digit pulses
6	digit pulses and 1'P for negative L group	0 or 9 sign pulses	digit pulses
5		digit pulses	digit pulses
4		digit pulses	digit pulses
3		digit pulses	digit pulses
2		digit pulses	digit pulses
1		digit pulses and 1'P for negative R group	digit pulses and 1'P for negative LR group

place.

8.6.2. Transmitting Information from the Constant Transmitter

In general, only one signed 10 digit or signed 5 digit number can be transmitted from the constant transmitter in an addition time. The digit output terminal on panel 1 of the constant transmitter has 10 digit leads and a PM lead. Each of the 10 digit leads is fed by 4 coding gates, the 1, 2, 2', and 4P gates. The digit leads for the fifth and tenth decade places from the left can also receive pulses from a gate which passes the 1'P. The PM lead and the digit leads for the first five decade places from the left are connected to gates which pass the 9P (see PX-11-307 and Table 8-5).

8.6.2.1. Constants read from a card

The 1, 2, 2' and 4P gates for the first decade place from the left are controlled by the 4 constant selector gates which receive one input from the 1, 2, 2' and 4 storage relays for the first digit of the L group, and the 2nd input from an L or LR point on a constant selector switch; the 1, 2, 2', and 4 pulse gates for the second decade place from the left are controlled by the constant selector gates which receive one input from the 1, 2, 2' and 4 storage relays for the second digit of the L group and the 2nd input from an L or LR point on a constant selector switch, etc.

The gates which allow the 1' pulse to pass to the 5th or 10th from the left decade place leads respectively are controlled by the left or right complement correction selector gates. The gates, which allow the 9P to pass to the PM lead or to the PM lead and the first 5 decade place leads from the left, are controlled respectively by the left or right minus selector gates.

When a constant transmitter program control is stimulated, the selector gates chosen by the setting of the constant selector switch (see Table 8-3) emit a

PX-11-40

TABLE 8-6

SIMULTANEOUS STIMULATION OF TWO CONSTANT TRANSMITTER PROGRAM CONTROLS

A_L^+ refers to a group A_L storing a positive number; A_L^-, to a group A_L storing a negative number. D.P. is used for the phrase "digit pulses".

Switch settings / Lead	A_L and B_R	A_L and B_R	A_L and B_R	A_L and B_R	A_L and B_{LR}	A_L and B_{LR}	A_L and B_{LR}	A_R and B_{LR}	A_R and B_{LR}	A_{LR} and B_{LR}	A_{LR} and B_{LR}
	A_L^+ and B_R^+ set up in storage relays	A_L^+ and B_R^- set up in storage relays	A_L^- and B_R^- set up in storage relays	A_L^- and B_R^+ set up in storage relays	where only A_L^+ and B_R are set up in storage relays	where only A_L^- and B_R^+ are set up in storage relays	where only A_L^- and B_R^- are set up in storage relays	where only A_R^+ and B_L^- are set up in storage relays	where only A_R^- and B_L^+ are set up in storage relays	where only A_L^- and B_R^+ are set up in storage relays	where only A_L^+ and B_R^- are set up in storage relays
PM	0		9P		0	9P	9P	9P		9P	0
10	D.P. for A_L		D.P. for A_L		D.P. for A_L	D.P. for A_L	D.P. for A_L	D.P. for B_L		D.P. for A_L	D.P. for A_L
9	"	Impossible since 9P for sign of B_R are emitted over leads 6-10	"	Impossible since 9P for sign of B_R are emitted over leads 6-10	"	"	"	"	Impossible since 9P for sign of A_R are emitted over leads 6-10	"	"
8	"		"		"	"	"	"		"	"
7	"		"		"	"	"	"		"	"
6	"		" and 1'P		"	" and 1'P	" and 1'P	" (no 1'P)		" (no 1'P)	"
5	D.P. for B_R		D.P. for B_R		D.P. for B_R	D.P. for B_R	D.P. for B_R	D.P. for A_R		D.P. for B_R	D.P. for B_R
4	"		"		"	"	"	"		"	"
3	"		"		"	"	"	"		"	"
2	"		"		"	"	"	"		"	"
1	"		"		" and 1'P	"	" and 1'P	"		"	" and 1'P
Comment	Simultaneous stimulation of two program controls set up for A_L and B_R transmission is possible when: 1. A_L and B_R are always positive or 2. A_L may be A_L^- but B_R is always B_R^+ provided that the accumulator which receives B_R has a deleter for suppressing sign.				Simultaneous stimulation of 2 program controls set up for A_L and B_{LR} transmission is possible when only 5 digits A_L and B_R groups are set up in the storage relays and when: 1. A_L and B_R are both always positive or both always negative or 2. A_L may be A_L^- but B_R is B_R^+ provided that a PM deleter is used at the accumulator which receives B_R.			Simultaneous stimulation of two program controls set up for A_R and B_{LR} transmission is possible when only 5 digit A_R and B_L groups are set up in the storage relays and when: 1. A_R and B_L are both always positive or 2. B_L is always B_L^- and A_R always A_R^+ provided that the accumulator which receives A_R has a PM deleter and provided that the 1'P is supplied at the accumulator which receives B_L.		Simultaneous stimulation of two program controls set up for A_{LR} and B_{LR} transmission is possible when only 5 digit A_L and B_R groups are set up in the storage relays and when: 1. A_L and B_R are both always positive or 2. A_L and B_R are both always negative provided that the 1'P is put in at the accumulator which receives A_L or 3. A_L may be A_L^- but B_R is always B_R^+ provided that a PM deleter is used at the accumulator which receives B_R.

signal if their corresponding relays have been activated. The signals thus emitted open the gates controlled by such selector gates and allow appropriate numbers of pulses to be transmitted over the 11 leads of the digit output terminal. The leads of the digit output terminal transmit information as shown in Table 8-5.

In Section 8.5, the statement was made that two constant transmitter program controls could be simultaneously stimulated or 2 five digit constants could be transmitted simultaneously provided that no logical conflict existed in the demands thus put on the leads of the digit output terminals.

Consideration of Tables 8-3 and 8-5 shows the cases in which the simultaneous stimulation of two program controls is possible. Certain possible cases are tabulated in Table 8-6 (cases not shown can be argued similarly). The illustrations of Table 8-6 involve groups A and B but any other pair of groups (with both not necessarily being controlled by the same group of 6 constant selector switches) can be treated in the same way.

Similarly, it can be seen that a 5 digit L and a five digit R subgroup of the same ten digit group can be called for simultaneously by the stimulation of one constant transmitter program control set up for LR transmission when:

1) Both subgroups are always positive
2) The left subgroup is always positive and the right subgroup always negative provided that the sign of the right subgroup is corrected at the receiving accumulator. This involves picking up the 1'P in units decade of some accumulator and then transmitting it to the PI decade of the accumulator which receives the R group.
3) Both subgroups are always negative provided that the 1'P needed for a tens complement is provided at the accumulator which receives the left subgroup.

8.6.2.2. Constants set up on set switches

The transmission of the J and K groups of constants is similar to that for groups A-H except that there are no complement correction selector gates for these constants and the other selector gates receive one input from the set switches instead of from storage relays.

Notice that since no provision has been made for converting negative numbers into complements in the case of the J and K groups, negative numbers must be set up on these switches as complements and, since no complement correction gates have been provided for these groups, tens complements must be set up.

8.7. ILLUSTRATIVE PROBLEM

A problem illustrating the use of both the reader and constant transmitter is discussed in this section.

In set-up tables, the symbol $\frac{i-j}{Ri}$ is written on the line corresponding to the first addition time of a reading program. For example, a reading program which is stimulated by the program pulse 2-3 emitted at the end of addition time 6 is written on the line for addition time 7. Similarly $\frac{i-j}{Rl}$ is used to indicate the reader interlock pulse. The symbol $\frac{Ro}{i-j}$ designates the program output pulse which the reader emits and is written on the line corresponding to the addition time in which reading is completed. On set-up diagrams Ri, Rl, and Ro have been drawn in the same relative position as they appear on PX-9-302. The reader start button is circled for a computation initiated by it.

The instructions for the constant transmitter are given in a double column on set-up tables. The left half shows the program input pulse and program control number on the first level, the setting of the constant selector switch on the second level, and the program output pulse on the third level. In the right

TABLE 8-8

Computations to form ${}_tN_k$, the t^{th} term of Quantity N_k, where k = 0, 1, ..., and 5.

$t = 1, 2, 3, 4, 5$

(1) $= x_{r+1,2}x_{r+2,3}$

(2) $= x_{r+3,4}x_{r+4,5}$

(3) = (1) . (2)

(4) $= x_{r,1}$. (3) $= {}_tD_0$

(5) $= a_r$. (3) $= {}_tD_1$

(6) $= x_{r,1} \cdot x_{r+2,3}$

(7) = (2) . (6)

(8) $= a_{r+1}$. (7) $= {}_tD_2$

(9) $= x_{r+1,2} \cdot x_{r,1}$

(10) = (2) . (9)

(11) $= a_{r+2}$. (10) $= {}_tD_3$

(12) $= x_{r+2,3} \cdot x_{r+4,5}$

(13) = (9) . (12)

(14) $= a_{r+3}$. (13) $= {}_tD_4$

(15) $= x_{r+3,4} \cdot x_{r+2,3}$

(16) = (9) . (15)

(17) $= a_{r+4}$. (16) $= {}_tD_5$

t	r^*
1	1
2	2
3	3
4	4
5	5

$t = 6, 7, 8, 9, 10$

(1) $= x_{r-1,2}x_{r-2,3}$

(2) $= x_{r-3,4}x_{r-4,5}$

(3) = (1) . (2)

(4) $= x_{r,1}$ (3) $= -{}_tD_0$

(5) $= a_r$. (3) $= -{}_tD_1$

(6) $= x_{r,1} \cdot x_{r-2,3}$

(7) = (2) . (6)

(8) $= a_{r-1}$. (7) $= -{}_tD_2$

(9) $= x_{r-1,2} \cdot x_{r,1}$

(10) = (2) . (9)

(11) $= a_{r-2}$. (10) $= -{}_tD_3$

(12) $= x_{r-2,3} \cdot x_{r-4,5}$

(13) = (9) . (12)

(14) $= a_{r-3}$. (13) $= -{}_tD_4$

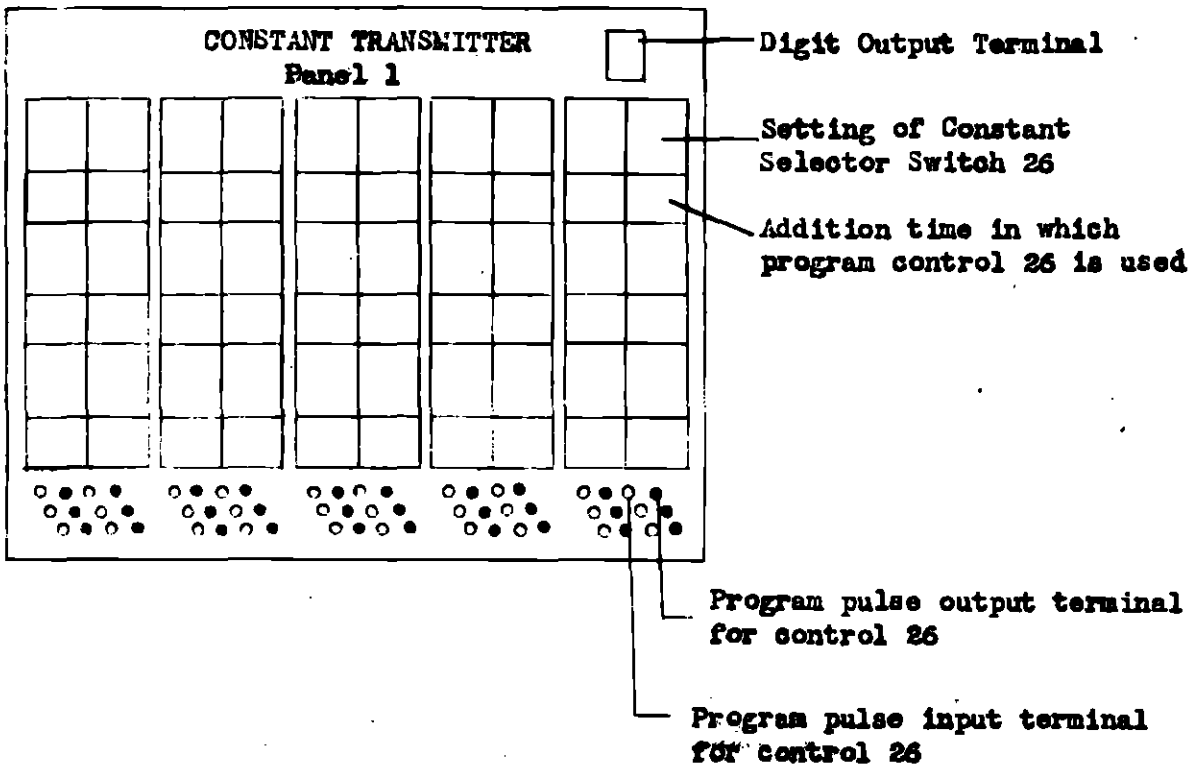
(15) $= x_{r-3,4} \cdot x_{r-2,3}$

(16) = (9) . (15)

(17) $= a_{r-4}$. (16) $= -{}_tD_5$

t	r^*
6	5
7	6
8	7
9	8
10	9

* all subscripts r, r+1, ..., r-1, ..., are mod 5



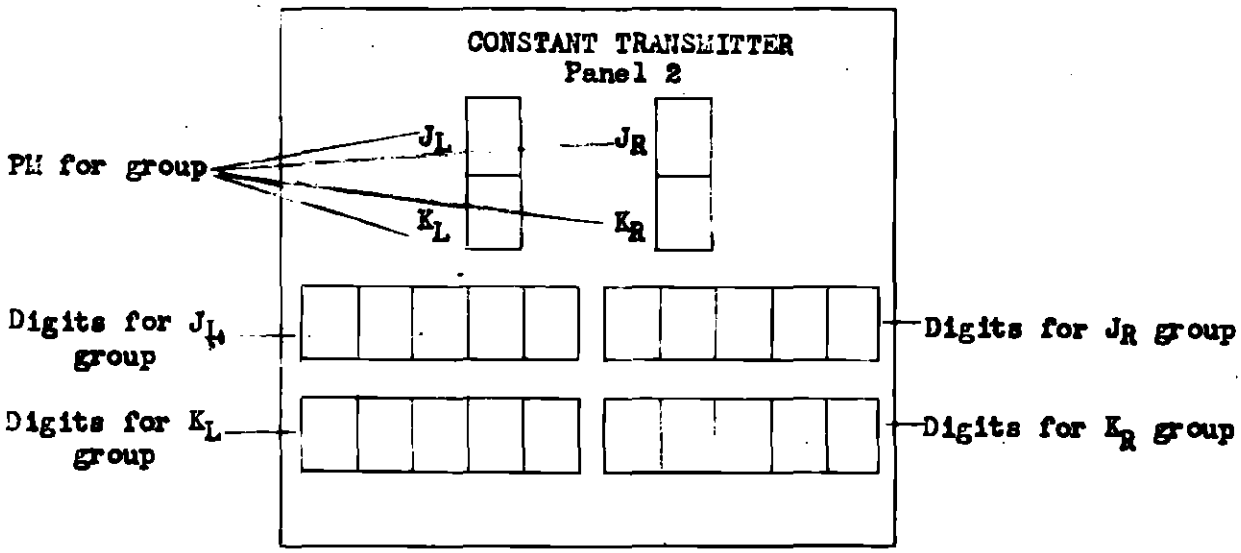


Fig. 8-1

SET-UP DIAGRAM CONVENTIONS FOR CONSTANT TRANSMITTER

TABLE 8-7

TERMS OF N_k

No.	t = 1	t = 2	t = 3	t = 4	t = 5	t = 6	t = 7	t = 8	t = 9	t = 10
N_0	$x_{11}x_{22}x_{33}x_{44}x_{55}$	$x_{21}x_{32}x_{43}x_{54}x_{15}$	$x_{31}x_{42}x_{53}x_{14}x_{25}$	$x_{41}x_{52}x_{13}x_{24}x_{35}$	$x_{51}x_{12}x_{23}x_{34}x_{45}$	$-x_{51}x_{42}x_{33}x_{24}x_{15}$	$-x_{11}x_{52}x_{43}x_{34}x_{25}$	$-x_{21}x_{12}x_{53}x_{44}x_{35}$	$-x_{31}x_{22}x_{13}x_{54}x_{45}$	$-x_{41}x_{32}x_{23}x_{14}x_{44}$
N_1	$a_1\ x_{22}x_{33}x_{44}x_{55}$	$a_2\ x_{32}x_{43}x_{54}x_{15}$	$a_3\ x_{42}x_{53}x_{14}x_{25}$	$a_4\ x_{52}x_{13}x_{24}x_{35}$	$a_5\ x_{12}x_{23}x_{34}x_{45}$	$-a_5\ x_{42}x_{33}x_{24}x_{15}$	$-a_1\ x_{52}x_{43}x_{34}x_{25}$	$-a_2\ x_{12}x_{53}x_{44}x_{35}$	$-a_3\ x_{22}x_{13}x_{54}x_{45}$	$-a_4\ x_{32}x_{23}x_{14}x_{55}$
N_2	$x_{11}a_2\ x_{33}x_{44}x_{55}$	$x_{21}a_3\ x_{43}x_{54}x_{15}$	$x_{31}a_4\ x_{53}x_{14}x_{25}$	$x_{41}a_5\ x_{13}x_{24}x_{35}$	$x_{51}a_1\ x_{23}x_{34}x_{45}$	$-x_{51}a_4\ x_{33}x_{24}x_{15}$	$-x_{11}a_5\ x_{43}x_{34}x_{25}$	$-x_{21}a_1\ x_{53}x_{44}x_{35}$	$-x_{31}a_2\ x_{13}x_{54}x_{45}$	$-x_{41}a_3\ x_{23}x_{14}x_{55}$
N_3	$x_{11}x_{22}a_3\ x_{44}x_{55}$	$x_{21}x_{32}a_4\ x_{54}x_{15}$	$x_{31}x_{42}a_5\ x_{14}x_{25}$	$x_{41}x_{52}a_1\ x_{24}x_{35}$	$x_{51}x_{12}a_2\ x_{34}x_{45}$	$-x_{51}x_{42}a_3\ x_{24}x_{15}$	$-x_{11}x_{52}a_4\ x_{34}x_{25}$	$-x_{21}x_{12}a_5\ x_{44}x_{35}$	$-x_{31}x_{22}a_1\ x_{54}x_{45}$	$-x_{41}x_{32}a_2\ x_{14}x_{55}$
N_4	$x_{11}x_{22}x_{33}a_4\ x_{55}$	$x_{21}x_{32}x_{43}a_5\ x_{15}$	$x_{31}x_{42}x_{53}a_1\ x_{25}$	$x_{41}x_{52}x_{13}a_2\ x_{35}$	$x_{51}x_{12}x_{23}a_3\ x_{45}$	$-x_{51}x_{42}x_{33}a_2\ x_{15}$	$-x_{11}x_{52}x_{43}a_3\ x_{25}$	$-x_{21}x_{12}x_{53}a_4\ x_{35}$	$-x_{31}x_{22}x_{13}a_5\ x_{45}$	$-x_{41}x_{32}x_{23}a_1\ x_{55}$
N_5	$x_{11}x_{22}x_{33}x_{44}a_5$	$x_{21}x_{32}x_{43}x_{54}a_1$	$x_{31}x_{42}x_{53}x_{14}a_2$	$x_{41}x_{52}x_{13}x_{24}a_3$	$x_{51}x_{12}x_{23}x_{34}a_4$	$-x_{51}x_{42}x_{33}x_{24}a_1$	$-x_{11}x_{52}x_{43}x_{34}a_2$	$-x_{21}x_{12}x_{53}x_{44}a_3$	$-x_{31}x_{22}x_{13}x_{54}a_4$	$-x_{41}x_{32}x_{23}x_{14}a_5$

hand half the constant transmitted is specified. The symbols are written on the line for the addition time in which the constant is transmitted.

The set-up diagram conventions for the constant transmitter are shown on Figure 8-1.

The master programmer is also used in the illustrative problem of this section. In most cases, the symbols used are explained where they appear. For further details see Chapter X.

The illustrative problem of this section consists of forming the six quantities N_0 through N_5 each of which is the sum of the 10 terms shown on Table 8-7. We assume that the N_k are to be evaluated for 100 different sets of values x_{ij} but that the a_i do not vary from set to set. We assume, also, that the numbers x_{ij} and A_i are $5_{\wedge}^{\text{digit}}$ numbers between 0.1 and 1.0 and, further, that the numbers x_{ii} are non-negative for all sets.

The numbers a_2, a_3, a_4, and a_5 will be stored on the constant set switches. The numbers x_{ij} and a_1 are to be introduced into the ENIAC by means of punched cards. The subject of storing these numbers will be treated in more detail presently. At this point, however, we wish to describe the routine which will be used to form the numbers N_k.

Table 8-8 presents a sequence of multiplication programs which could be used to find the one term for each of the numbers N_k. From one value of t to another, the most striking change in the computations consists of using different sets of the x_{ij}. One distinction between the computations for $t = 1$ through 5 and those for $t = 6$ through 10 consists of the fact that in the former the A_i are required in ascending order of subscript and in the latter, in descending order of subscript. A second point of difference is that in the first class we are interested in the terms (4), (5), (8), (11), (14), and (17) and in the second class, in the

negatives of them. The operations of forming terms (1) through (17) will be referred to as the multiplication sequence. In order to provide for the differences noted above this sequence will be modified as multiplication sequence A or B for t = 1 through 5 or t = 6 through 10 respectively. The quantities N_0 through N_5 will be found by repeating each of the modifications of the multiplication sequence 5 times.

Now we return to the matter of storing the numbers x_{ij} and a_i. In all, 26 numbers are to be introduced from punched cards. Since, only 16 five digit constants can be obtained in one card reading, at least 2 readings are required for each system of equations. Since, furthermore, the constants are needed repeatedly in different combinations, either they must be read repeatedly from cards on which they occur in different combinations, or at least 10 of them must be read from 1 card and stored in accumulators to be available when the card containing the remainder of them is read. The latter course is adopted here. The constants needed to form the terms listed in columns t = 1 and t = 6 (see Table 8-7) are read from a card and transferred to accumulators. Then, computations start for these values of t and meanwhile the reader scans the card containing the remaining numbers. As it turns out, only 8 accumulators are available for storing the 10 numbers read from the 1st card. Therefore, in each of 2 accumulators, we store a pair of numbers, one in the 5 left hand decades and the other in the five right hand decades. The 2 pairs of numbers are chosen from the x_{ii} terms, since it is easiest to store two positive numbers in one accumulator.

One further consideration influences the manner in which the constants are stored. The x_{ij} and a_i are all destined to go to the multiplier unit and we wish the resulting products to be similarly located in the decades of the product accumulator. One way to accomplish this is to align the numbers similarly in the argument accumulators, let us say at the extreme left. This, then, requires that

TABLE 8-9

STORAGE OF CONSTANTS

FIRST CARD

Constant Transmitter Group	Constant	Accumulator to which constant is transferred
A_L	x_{22}	1L
A_R	x_{11}	1R
B_L	x_{44}	2L
B_R	x_{33}	2R
C_L	a_1	8L
C_R	x_{55}	3R
D_L		
D_R	x_{51}	4R
E_L	x_{24}	5L
E_R		
F_L		
F_R	x_{15}	6R (clear at end of 3rd. M.S.)
G_L		
G_R		
H_L	x_{42}	7L (clear at end of 3rd M.S.)
H_R		
J_L	a_2	
J_R	a_3	
K_L	a_4	
K_R	a_5	

SECOND CARD

Constant Transmitter Group	Constant	Accumulator to which constant is transferred
A_L	x_{12}	
A_R	x_{21}	
B_L	x_{32}	
B_R	x_{31}	
C_L	x_{52}	
C_R	x_{41}	
D_L	x_{14}	
D_R	x_{13}	
E_L	x_{34}	
E_R	x_{23}	
F_L	x_{54}	
F_R	x_{43}	
G_L	x_{53}	6R (after third M.S.)
G_R	x_{25}	
H_L	x_{35}	7R (after fifth M.S.)
H_R	x_{45}	
J_L	a_2	
J_R	a_3	
K_L	a_4	
K_R	a_5	

TABLE 8-10

SET-UP ANALYSIS FOR EVALUATION OF THE NUMBERS N_k

INITIAL SEQUENCE: Read

1-1* Transfer constants from constant transmitter to accumulators

2-1 Read in parallel with sequence 2.1 and 2.2

2.1-1 Multiplication Sequence A

Form Terms (1) - (17) for i = 1
Receive Terms (4), (5), (8), (11), (14), and (17) from product accumulator's A output via α input channel of accumulators 14, 16, 17, ..., and 20 respectively.

2.2-1 Multiplication Sequence B
Form terms (1) - (17) for i = 6
Receive terms (4), (5), (8), (11), (14), and (17) from product accumulator's S output via β input channel of accumulators 14, 16, 17, ..., and 20 respectively.

3-1 Send Interlock Signal to Reader

4-4 Multiplication Sequence

4.1-1 A for i = 2, 3, 4, 5 in turn
4.2-1 B for i = 7, 8, 9, 10 in turn.

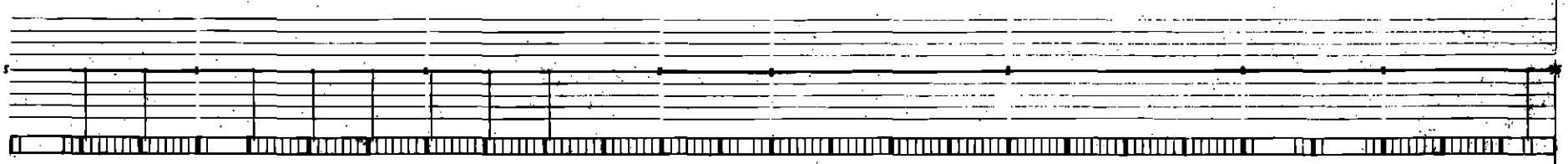
5-1 Read and, in parallel, print and then selective clear

*The number following a dash indicates how many times the sequence identified by the number preceding the dash is to be repeated.

numbers stored in the right hand side of an accumulator or a constant transmitter group be shifted to the left upon reception in an argument accumulator and that those stored at the left, not be shifted. Then, to make the computations for all ten columns precisely alike, all numbers which are used in the same programs from one multiplication sequence to another must be similarly located with regard to side left or right of storage facility. This plan calls for storing x_{ij} for j even at the left and for j odd at the right. This necessitates moving certain x_{ij} with odd j out of left hand constant transmitter groups (where they are temporarily located for want of free right hand groups) into right hand accumulator groups when the latter become available because the numbers they store at first are no longer needed. Table 8-9 shows a plan for the storage of constants required in this computation.

We return to a broad discussion of the plan for the computation. For each set of numbers x_{ij}, one card containing 10 of them is read. These numbers are put in storage in accumulators. Immediately, computation of the terms in columns t = 1 and t = 6 of table 8-7 starts and the reading of a card with 16 more numbers begins. When the reading of the 2nd card is completed, computation for the terms in the remaining columns of table 8-7 is carried out. As the various terms of the N_k are computed they are emitted from the product accumulator both additively and subtractively. In multiplication sequence A, these products emitted additively are received in accumulators 14, 16, 17, ..., 20; in multiplication sequence B, the products emitted subtractively are received in these same accumulators. After 10 repetitions of the multiplication sequence, the 6 numbers N_k are stored in the accumulators mentioned above. The values are printed, and the accumulators which store N_k are then selectively cleared. While printing takes place, the first card for the next set of x_{ij} is read. This plan is summarized in table 8-10.

TABLE I-11
SET-UP TABLE



ANALOG TIME	I.U.	M.P.	F.T. #1	Acc. #1	Acc. #2 Q	DIV.	Acc. #3 N	Acc. #4	Acc. #5 D	Acc. #6	Acc. #7 S	Acc. #8 RT2	Acc. #9 Iter	Acc. #10 Iconst	MULT.	Acc. #11 LHPP	Acc. #12	Acc. #13 RHPP & 3P	Acc. #14	Acc. #15	Acc. #16	Acc. #17	Acc. #18	F.T. #2	F.T. #3	Acc. #19	Acc. #20	C.T.
1-1																			0.05		0.05	0.05	0.05			0.05	0.05	
2																												
3																												
4																												
5																												
6																												
7																												
8																												
9																												
10																												
11																												
12																												
13																												
14																												
15																												
16																												

PX-11-401

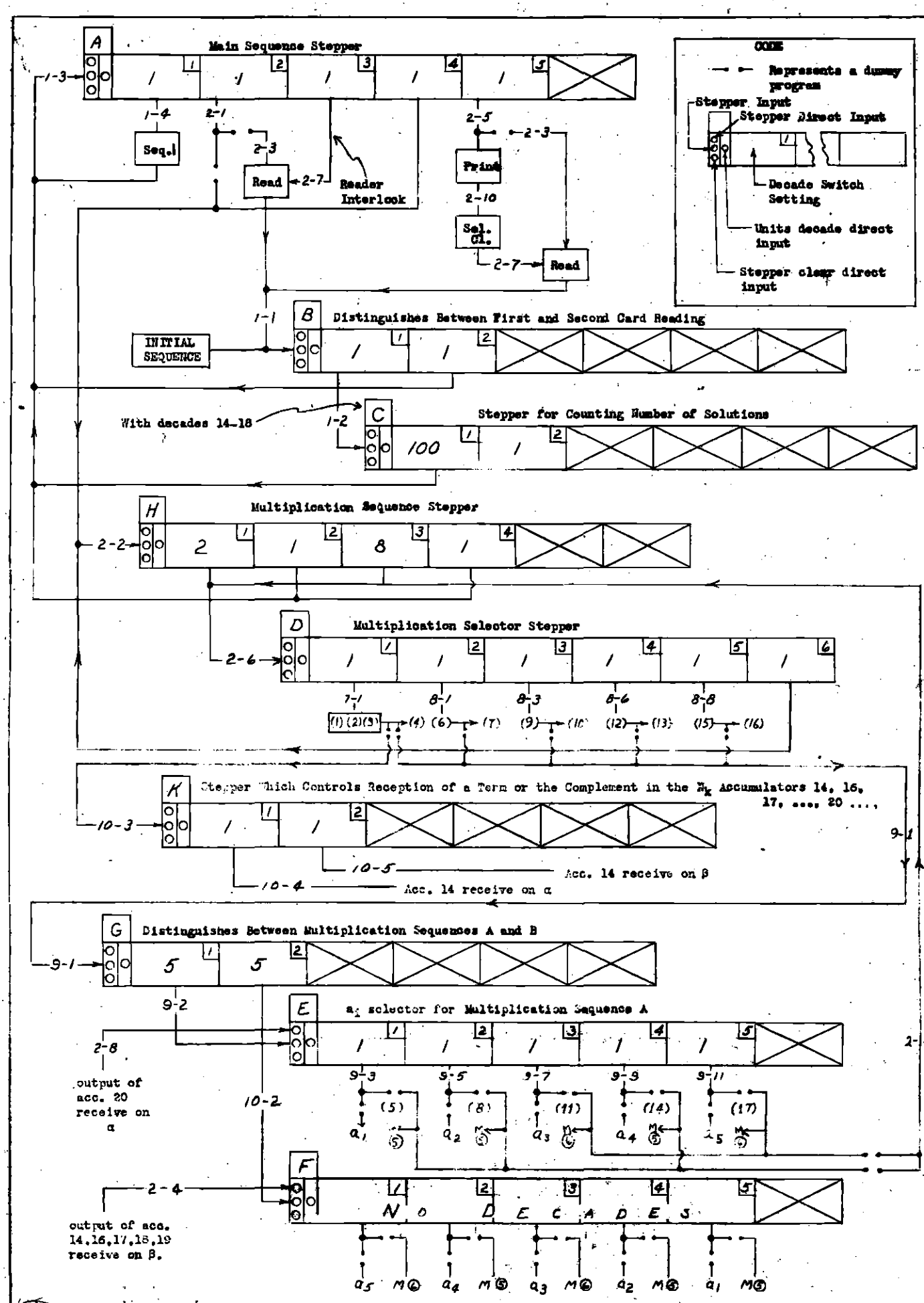


Fig. 8-2
MASTER PROGRAMMER LINES
EVALUATION OF N_k

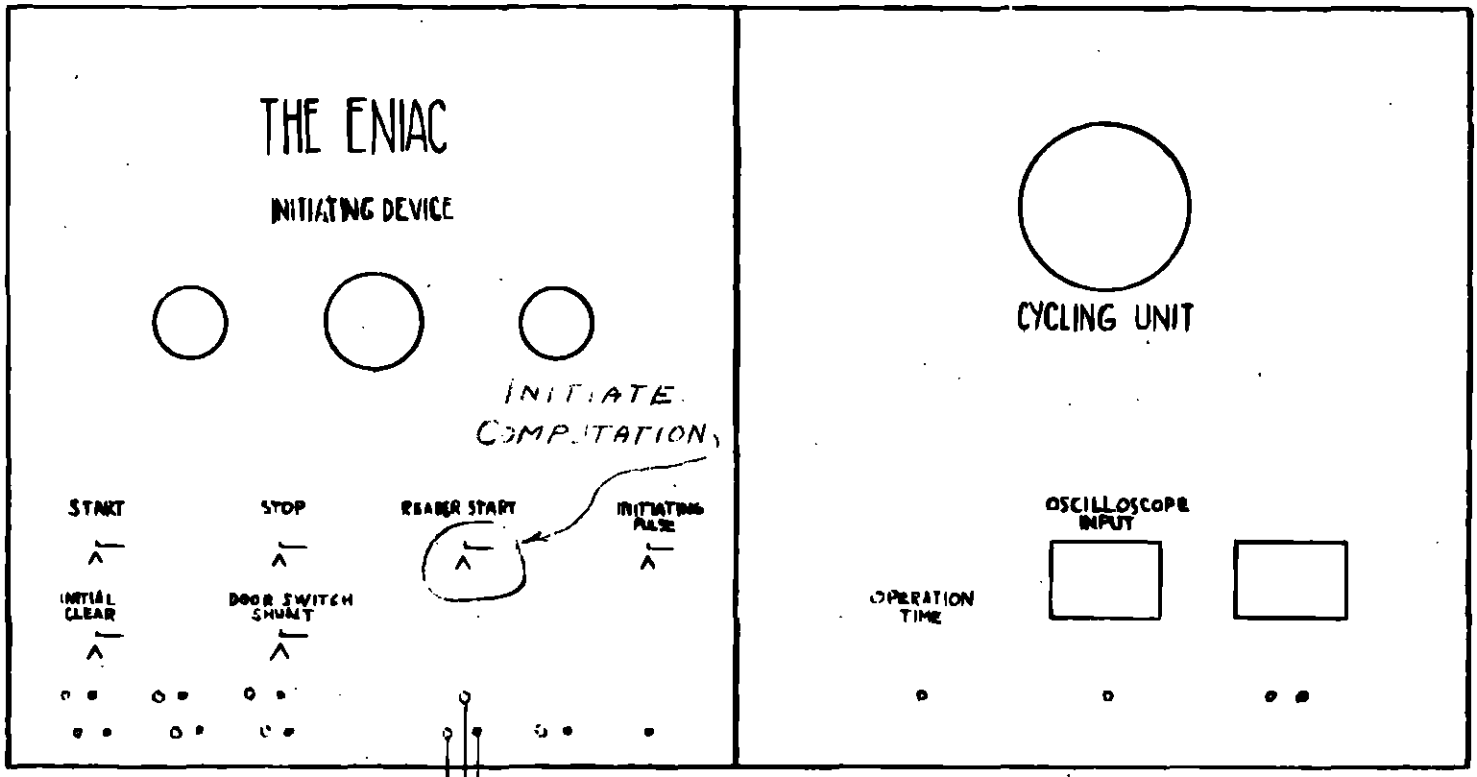
Figure 8-2 shows how the main program sequences are linked together by the master programmer. Stepper B is used to determine whether reading is the first for a system of equations (stage 1) or the second (stage 2). For the first reading, stepper B shifts control to stepper C which counts the number of solutions and then routes control to stepper A which directs the main sequences of the problem.

The output of stage 1 of stepper A stimulates the sequence in which constants from the first card are put in storage in accumulators. The output of stage 2 stimulates the reader and also goes to stepper H which controls the multiplication sequence. The output of stage 3 provides an interlock pulse for the reader. Control is shifted to stepper H again by the output of stage 4. The output of stage 5 stimulates the reader and printer. The output of the reader goes back to stepper B, etc.

Specific details for the set-up of sequence 1 are given in Table 8-11. On the line for addition time I-1, the symbol $0.0^{5}5$ in the contents column for accumulators 14, 16, 17, ..., 20 which will store the N_k terms indicates that the decimal point occurs one decade place to the right of the PM counter and that these accumulators clear to 5 in the 6th decade from the PM place. During addition times 4-13, the constants x_{ii} (for i = 1-5), x_{51}, x_{24}, x_{15}, x_{42}, and a_i are transferred from the constant transmitter to accumulators 1-8. Notice that constant transmitter program controls (1) and (2) set at A_L and A_R respectively are used serially for the transmission of x_{22} and x_{11} instead of one control set at A_{LR} as would be possible since both constants are positive. The reason this must be done is that when the second card is read, we must enter A_L and A_R separately for x_{12}, x_{21} (see Table 8-9) which may or may not be positive.

The multiplication sequence of the problem which is repeated once as

PX-11-405(a)



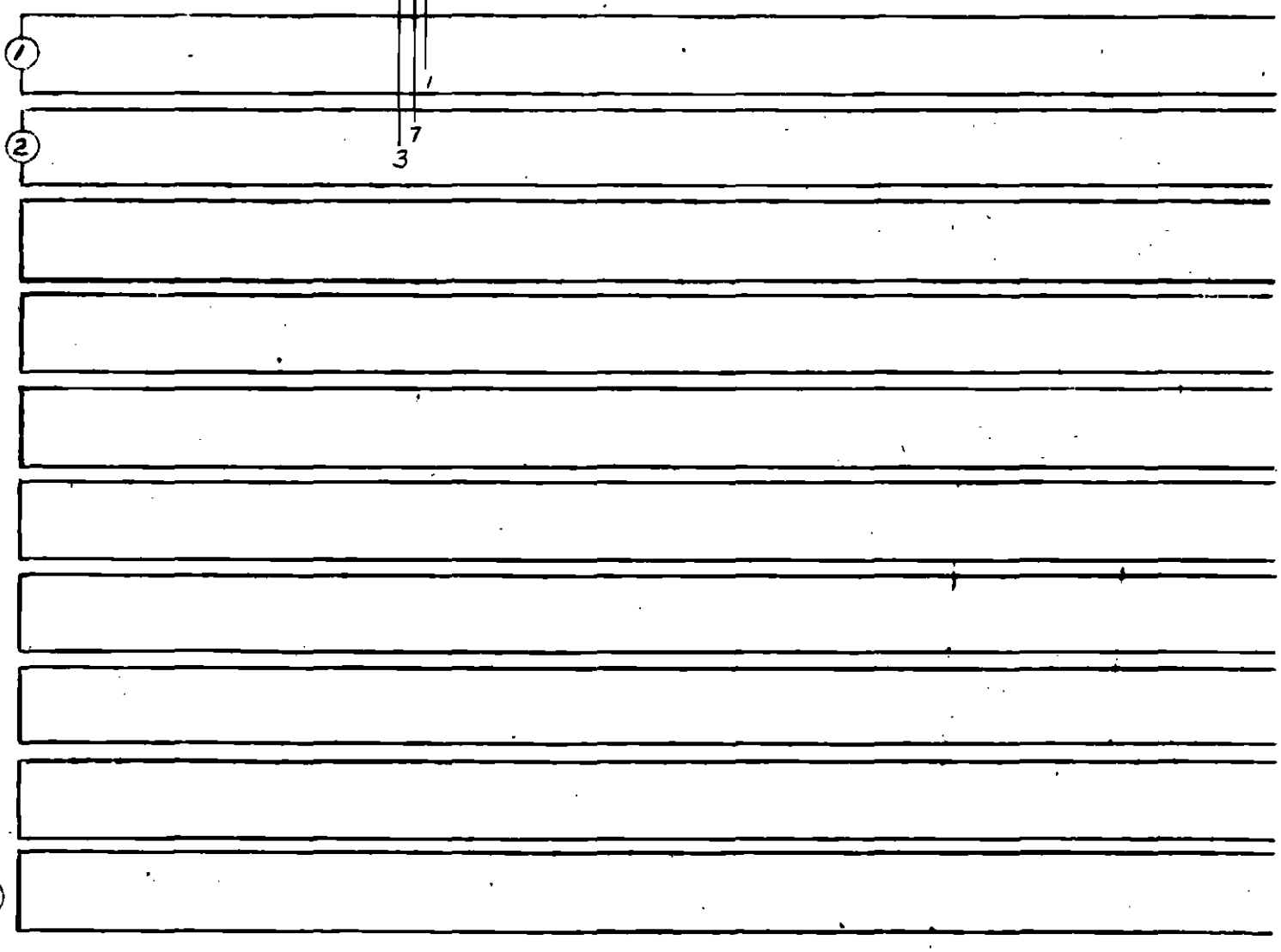


Fig. 8-3 (a)

SET-UP DIAGRAM FOR SEQUENCE 1 AND SEQUENCE 2.1

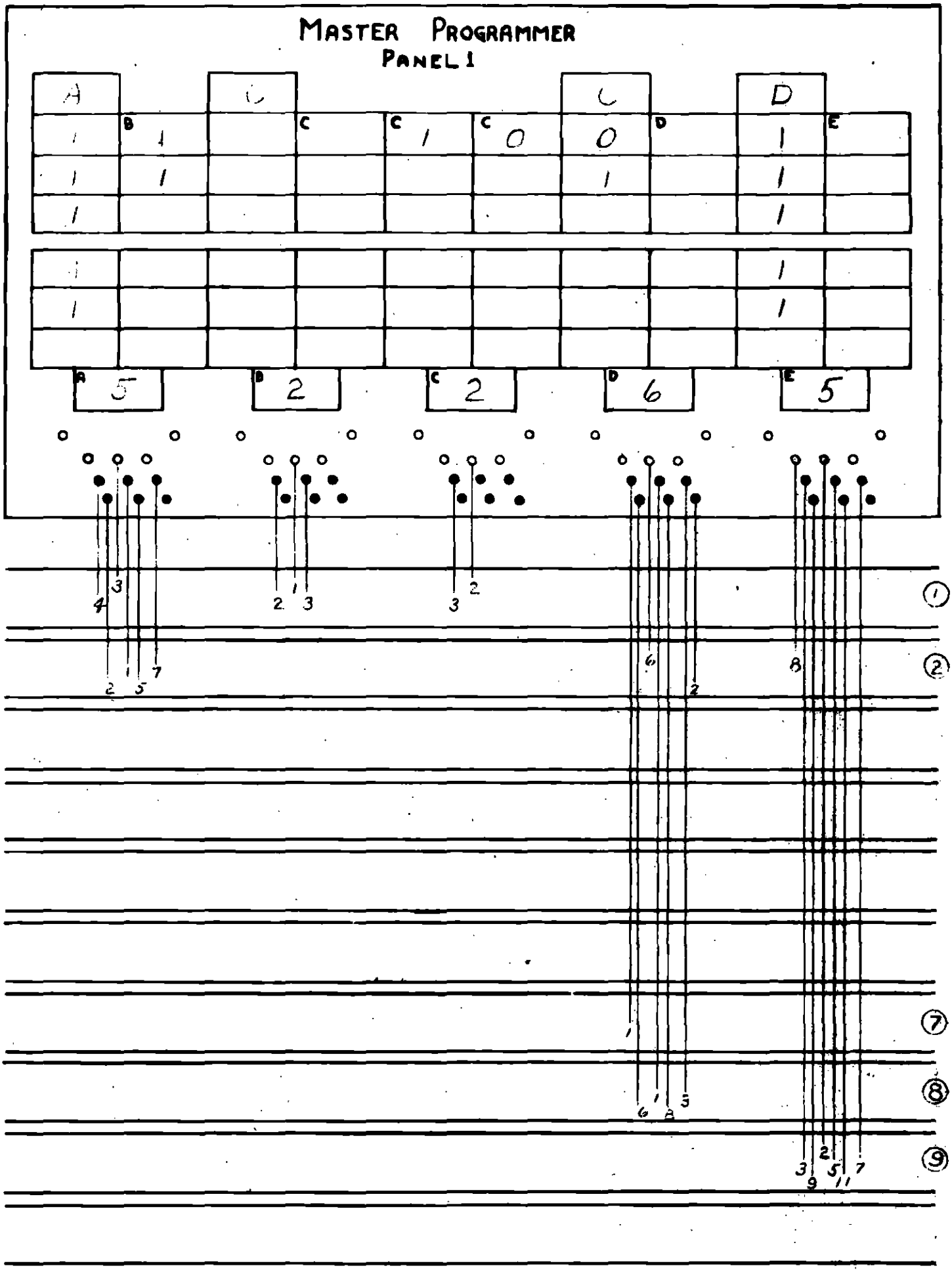


Fig. 8-3 (b)

SET-UP DIAGRAM FOR SEQUENCE 1 AND SEQUENCE 2.1

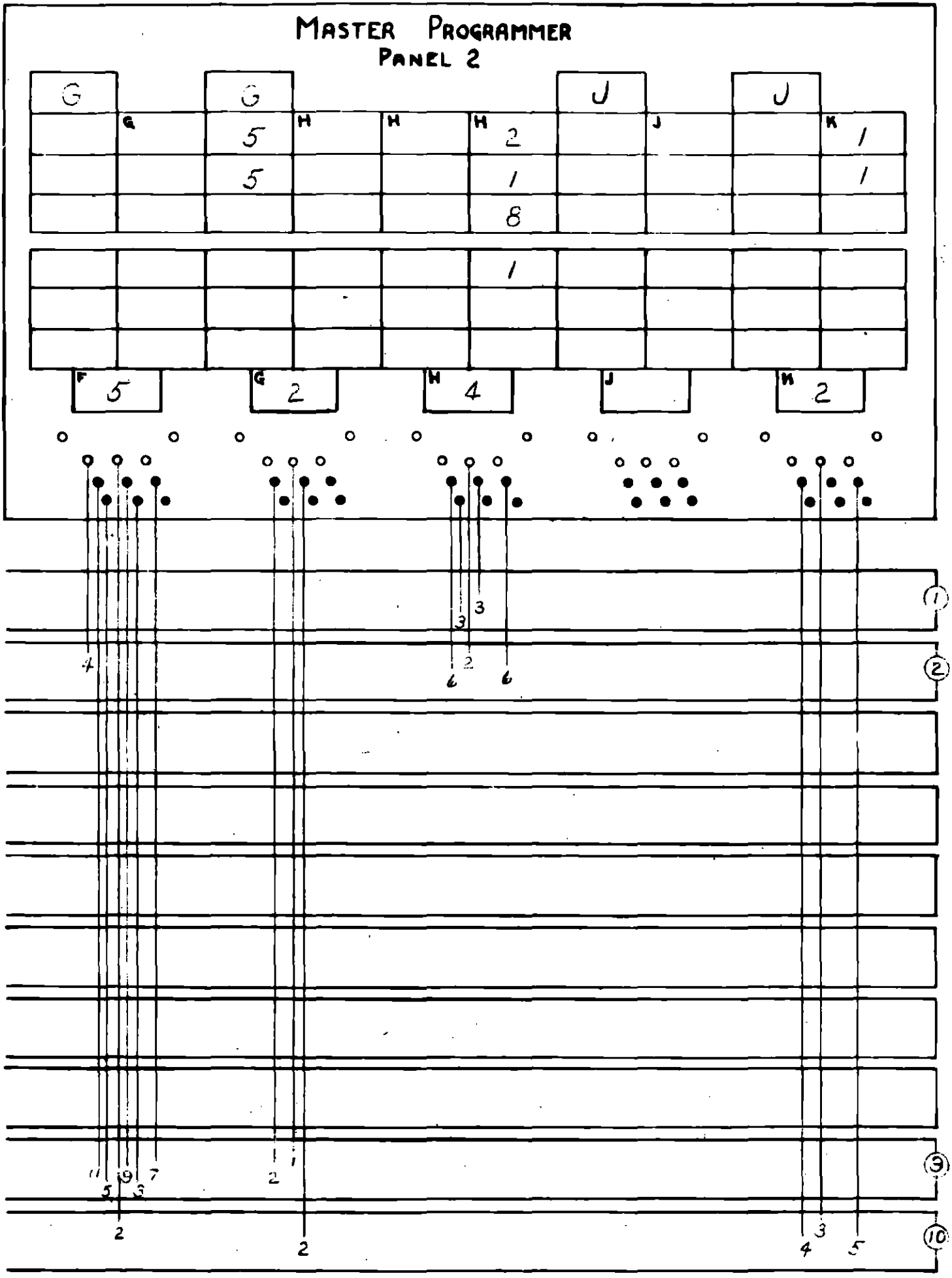


Fig. 8-3 (c)

SET-UP DIAGRAM FOR SEQUENCE 1 AND SEQUENCE 2.1

PX-11-405 (d)

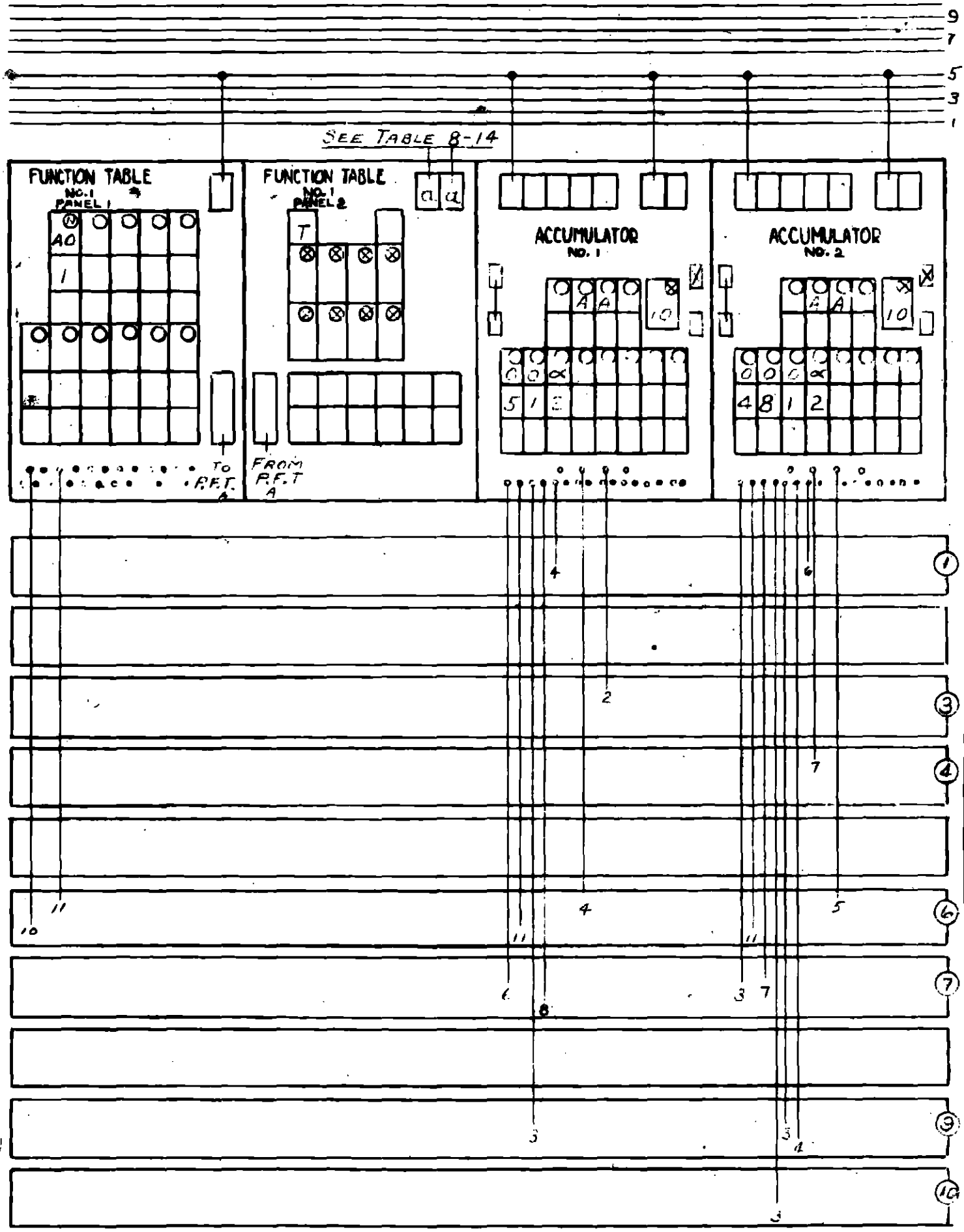


Fig. 8-3 (d)

SET-UP DIAGRAM FOR SEQUENCE 1 AND SEQUENCE 2.1

PX-11-005 (e)

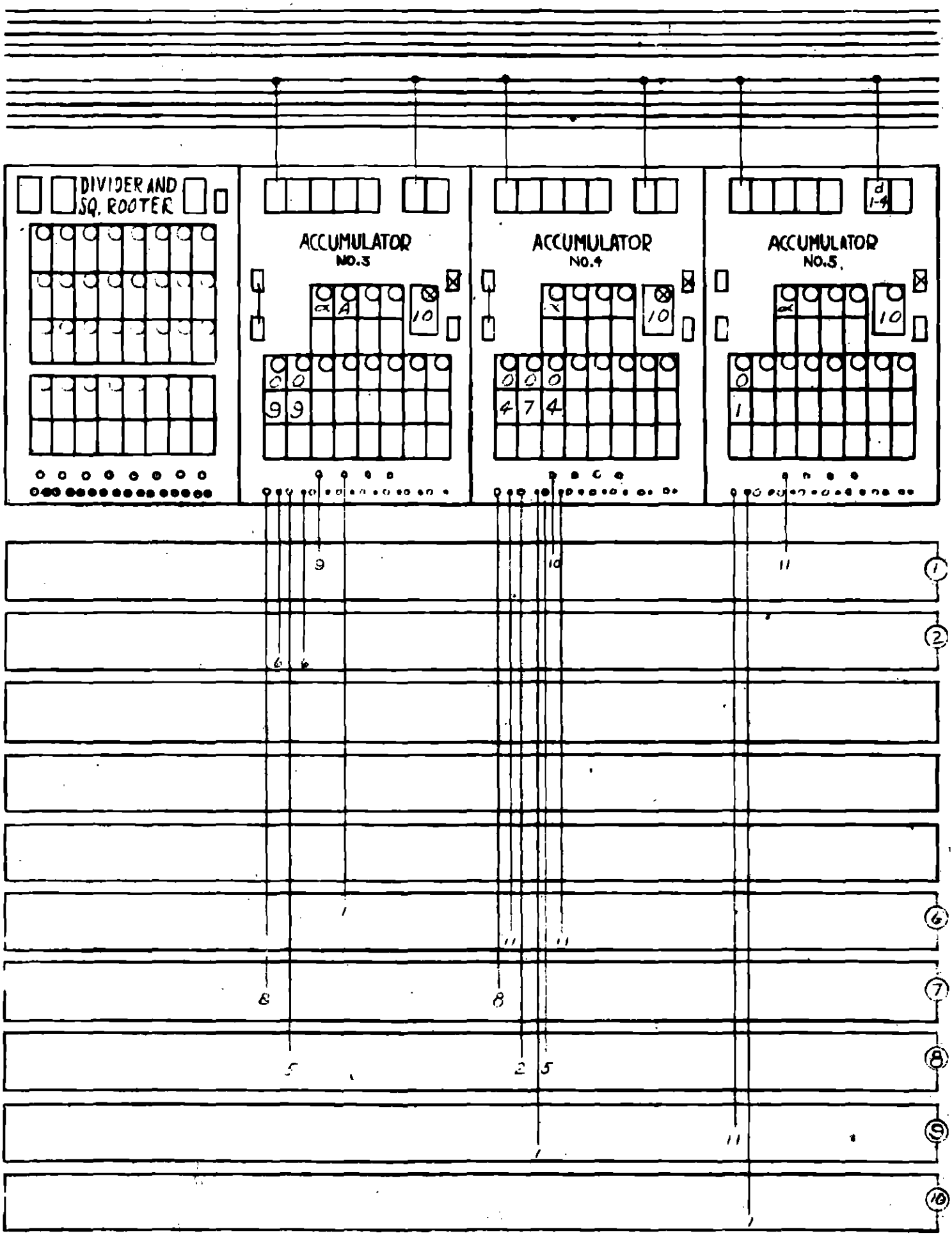


Fig. 8-3 (e)

SET-UP DIAGRAM FOR SEQUENCE 1 AND SEQUENCE 2.1

PX-11-405(F)

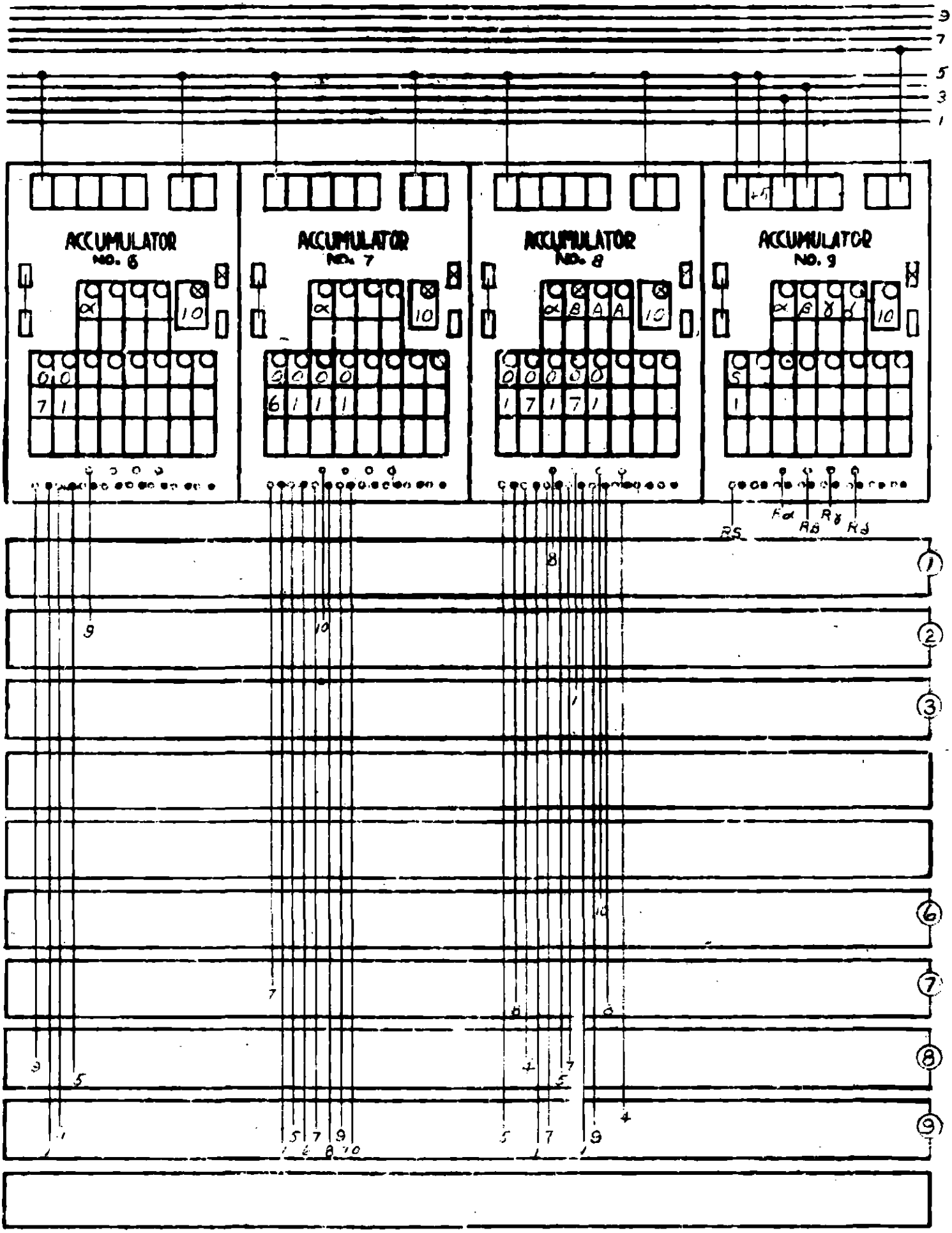
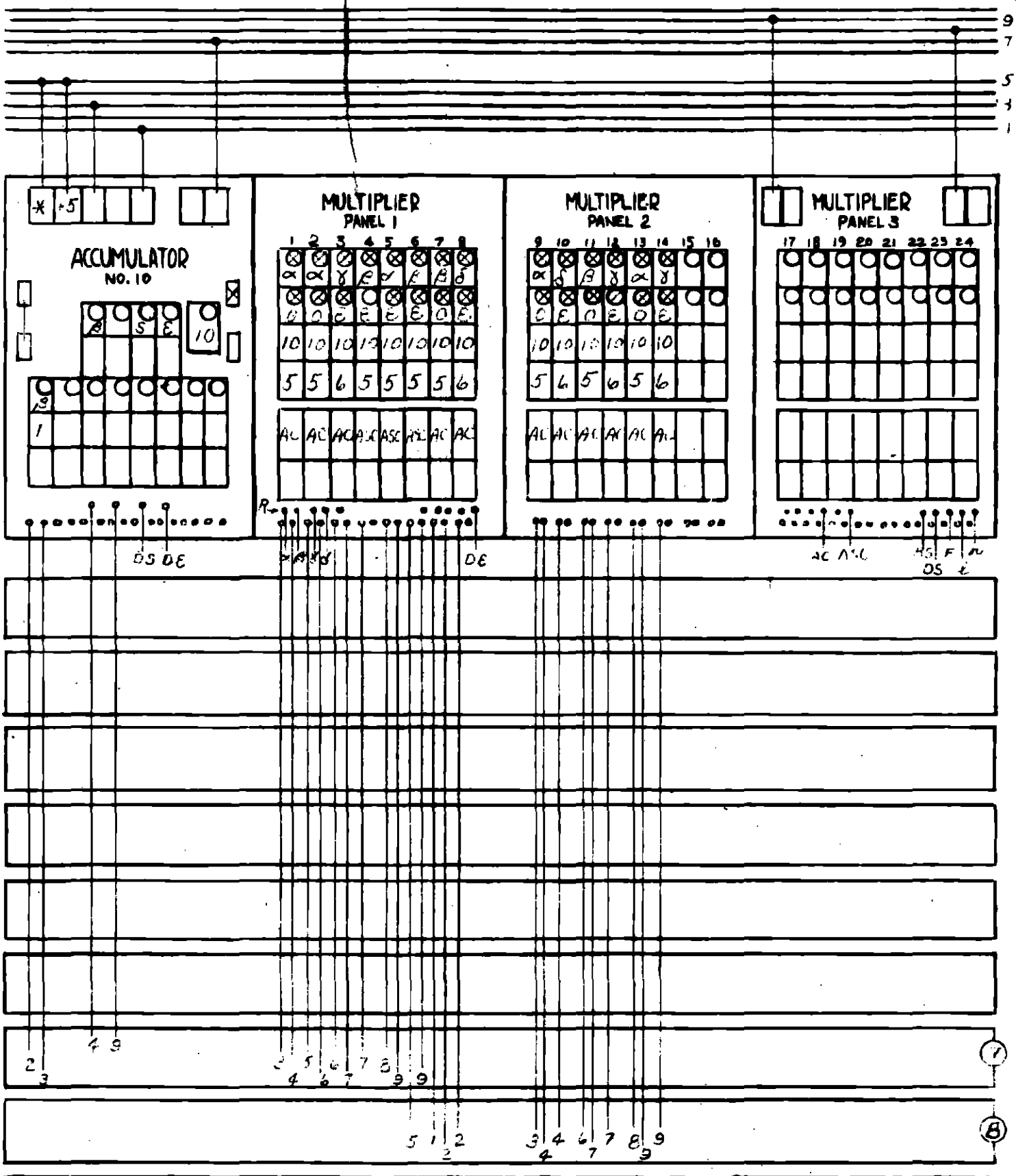


Fig. 6-3 (f)

SET-UP DIAGRAM FOR SEQUENCE 1 AND SEQUENCE 2.1

PX-11-405(g)



* Special d 1-5 for use at digit input terminal.

Fig. 8-3 (g)

SET-UP DIAGRAM FOR SEQUENCE 1 AND SEQUENCE 2.1

PX-11-403(4)

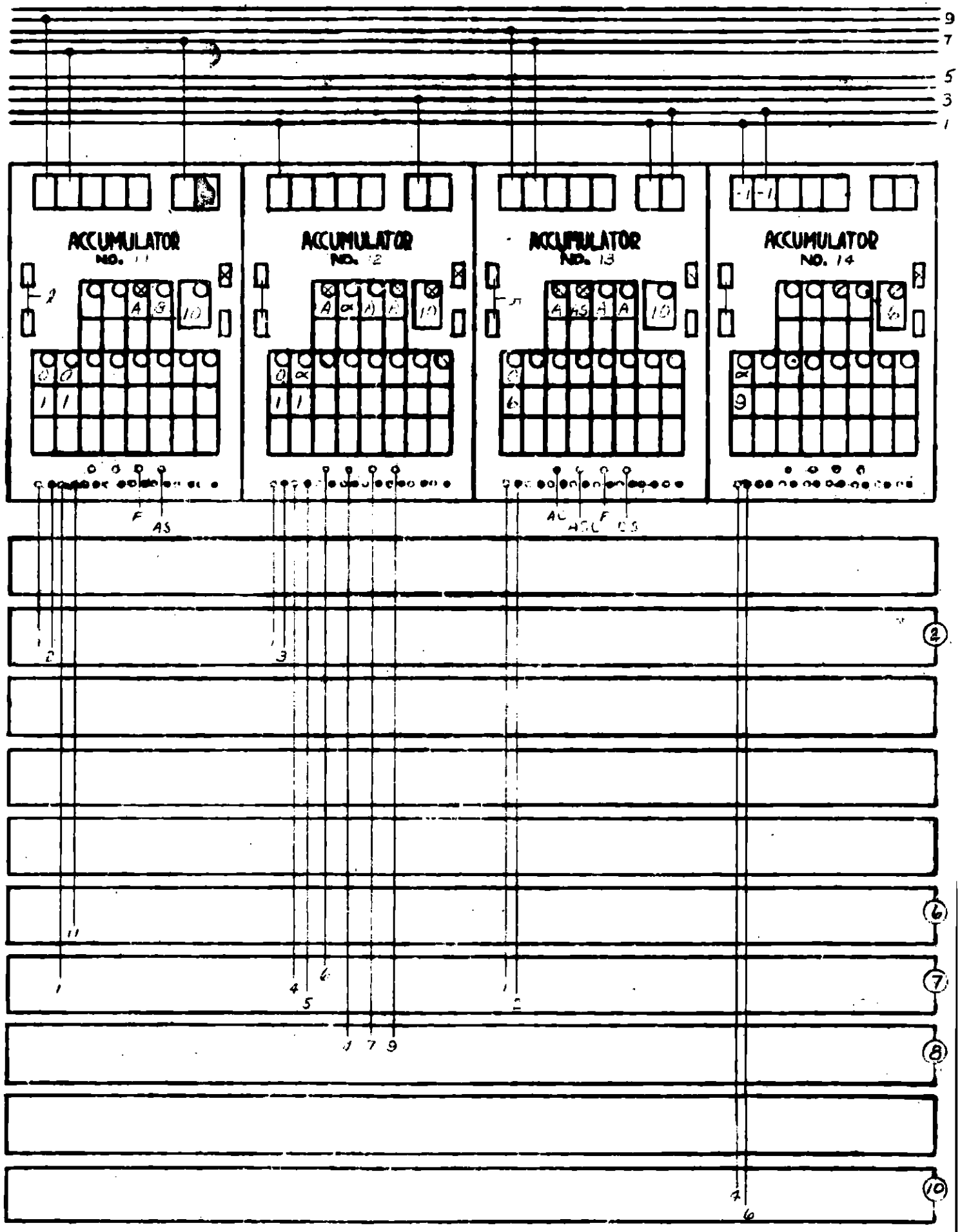


Fig. 8-3 (h)

SET-UP DIAGRAM FOR SEQUENCE 1 AND SEQUENCE 2

80

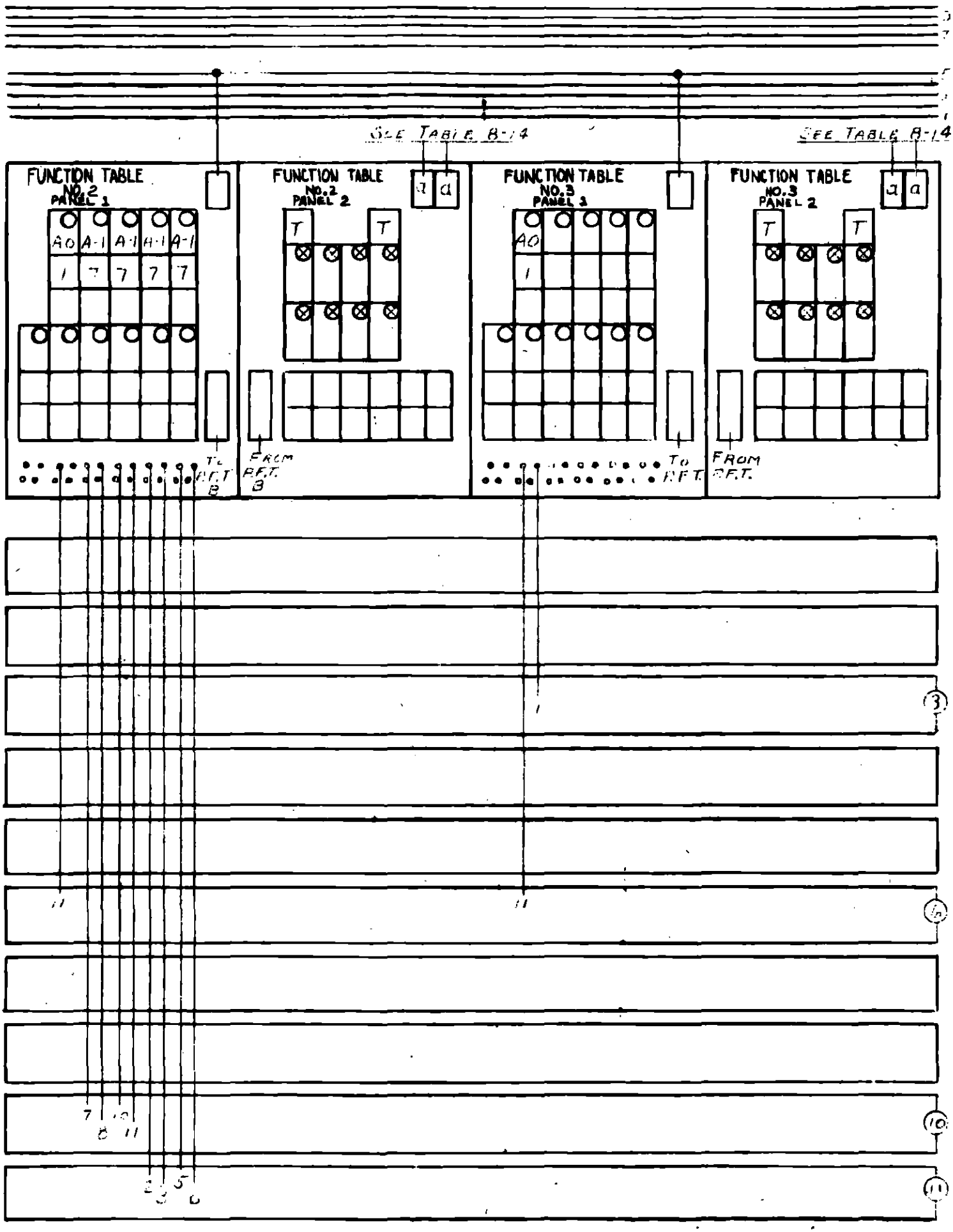


Fig. B-3 (j)

SET-UP DIAGRAM FOR SEQUENCE 1 AND SEQUENCE 2.1

PX-11-405(K)

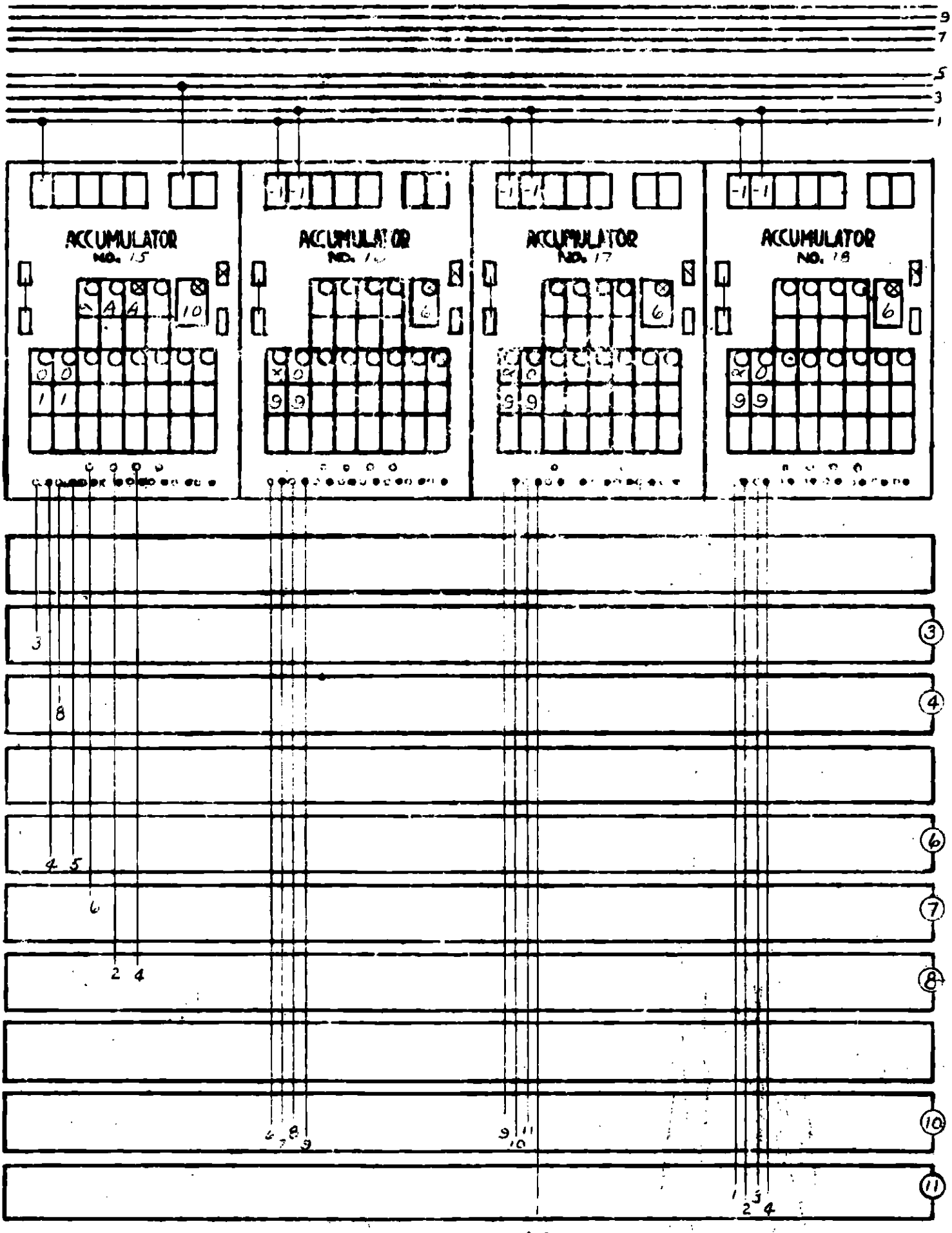


Figure 8-3 (k)

SET-UP DIAGRAM FOR SEQUENCE 1 AND SEQUENCE 2.1

PX-11-4057

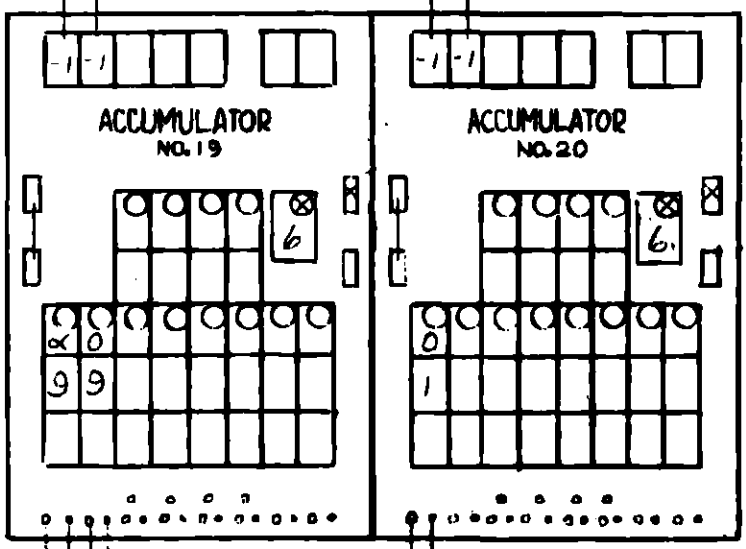


Figure 8-3 (1)

SET-UP DIAGRAM FOR SEQUENCE 1 AND SEQUENCE 8.1

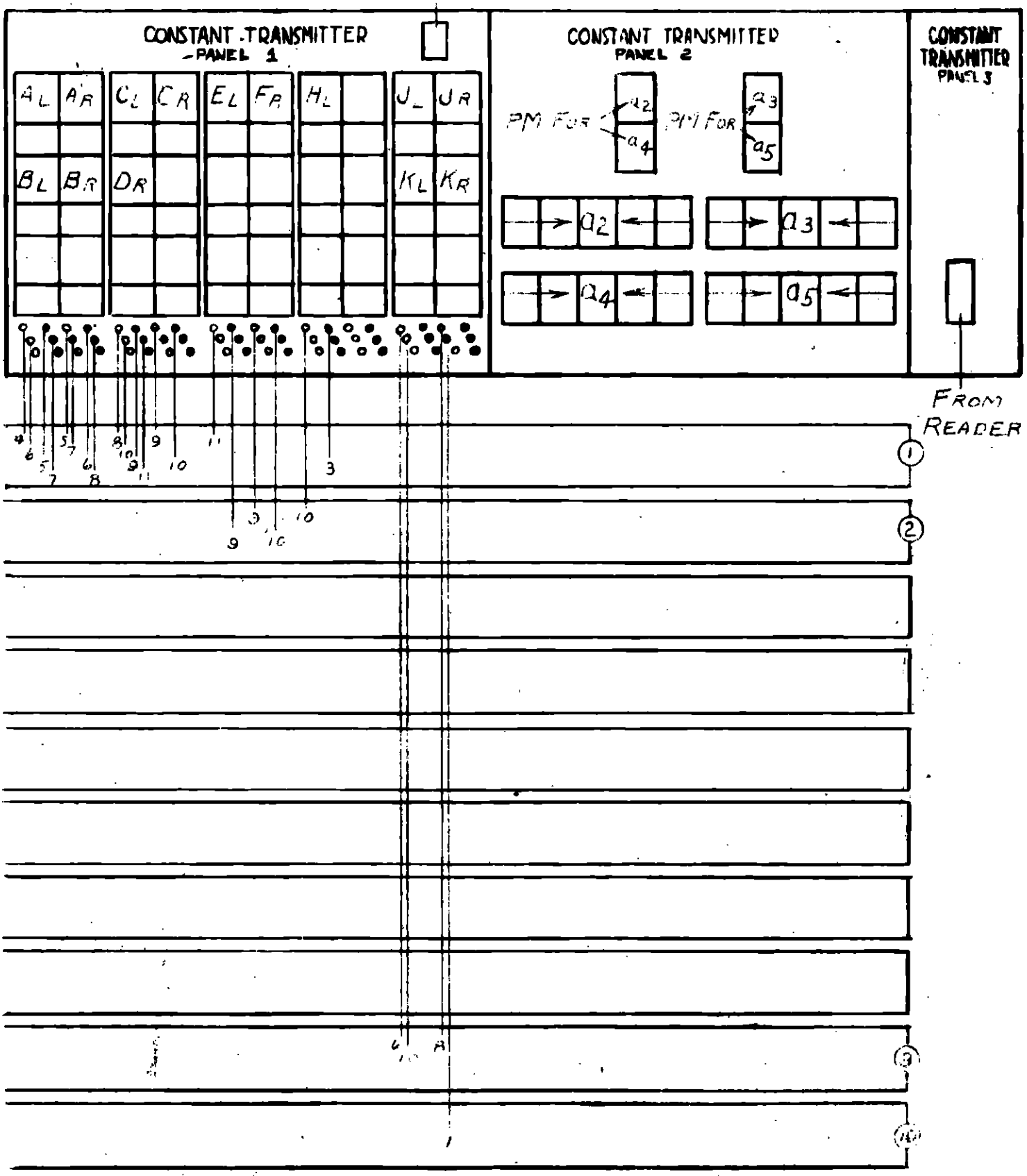


Fig. 8-3 (m)

SET-UP DIAGRAM FOR SEQUENCE 1 AND SEQUENCE 8.1

2.1, once as 2.2, four times as 4.1, and four times as 4.2, is described with the aid of the following tables and figures:

Table 8-8	Computations to form $_tN_k$
Table 8-9	Storage of Constants
Table 8-13	Set-Up Table for Sequence 2.1
Table 8-14	Set-Up of Function Tables for Programming Transmission of Constants
Figure 8-2	Master Programmer Links
Figure 8-3	Set-Up Figure for Sequences 1 and 2.1

Table 8-9 shows that the $x_{i,2n}$ and a_{2n} are stored either in left hand constant transmitter groups or in the five left hand decades of accumulators and that the $x_{i,2n+1}$ and a_{2n+1} are stored at the right. Therefore, to make the most efficient use of the high-speed multiplier, the $x_{i,\ 2n+1}$ are shifted five places to the left when they are received in the ier or icand accumulators. A +5 shifter (which shifts numerical data 5 places to the left) is used at the β input terminals of the ier and icand accumulators and arguments of the form $x_{i,2n+1}$ are received over the β input channel. Also, because certain accumulators store 2 numbers, it is necessary to delete the five right hand digits of an icand received from a left hand group when the icand is of the form $x_{i,2n+1}$. A d 1-5 deleter is used at the α input terminal of the icand accumulator for this purpose. A similar deleter is not needed at the ier accumulator since the high-speed multiplier uses only as many places of the ier as specified on the places switch.

Examination of Table 8-8 shows that the 17 multiplications of the multiplication sequence fall into three groups with characteristics as shown below:

All 17 multiplications are arranged in a predominant sequence with

TABLE 8-12

ANALYSIS OF MULTIPLICATION SEQUENCE

Group	Multiplications	Characteristics
A	(3), (7), (10), (13), and (16)	Arguments derived from same source and products received from product accumulator in same way for all 10 repetitions.
B	(1), (2), (6), (9), (12) and (15)	Arguments located in different places for the various repetitions. Products received from product accumulator in same way for all repetitions
C	(4)	Ier located in different places from repetition to repetition. Product received from A or S output of product accumulator on alternate repetitions
D	(5), (8), (11), (14) and (17)	Ier located in different places for the various repetitions. Furthermore, ier must be received sometimes on α and sometimes on β input terminal of ier accumulator. Products transmitted respectively from A or S output of product accumulator are received through α or β input channels of accumulators 14, 16, 17, ..., 20 on alternate repetitions.

PX-11.408

TABLE 6-14

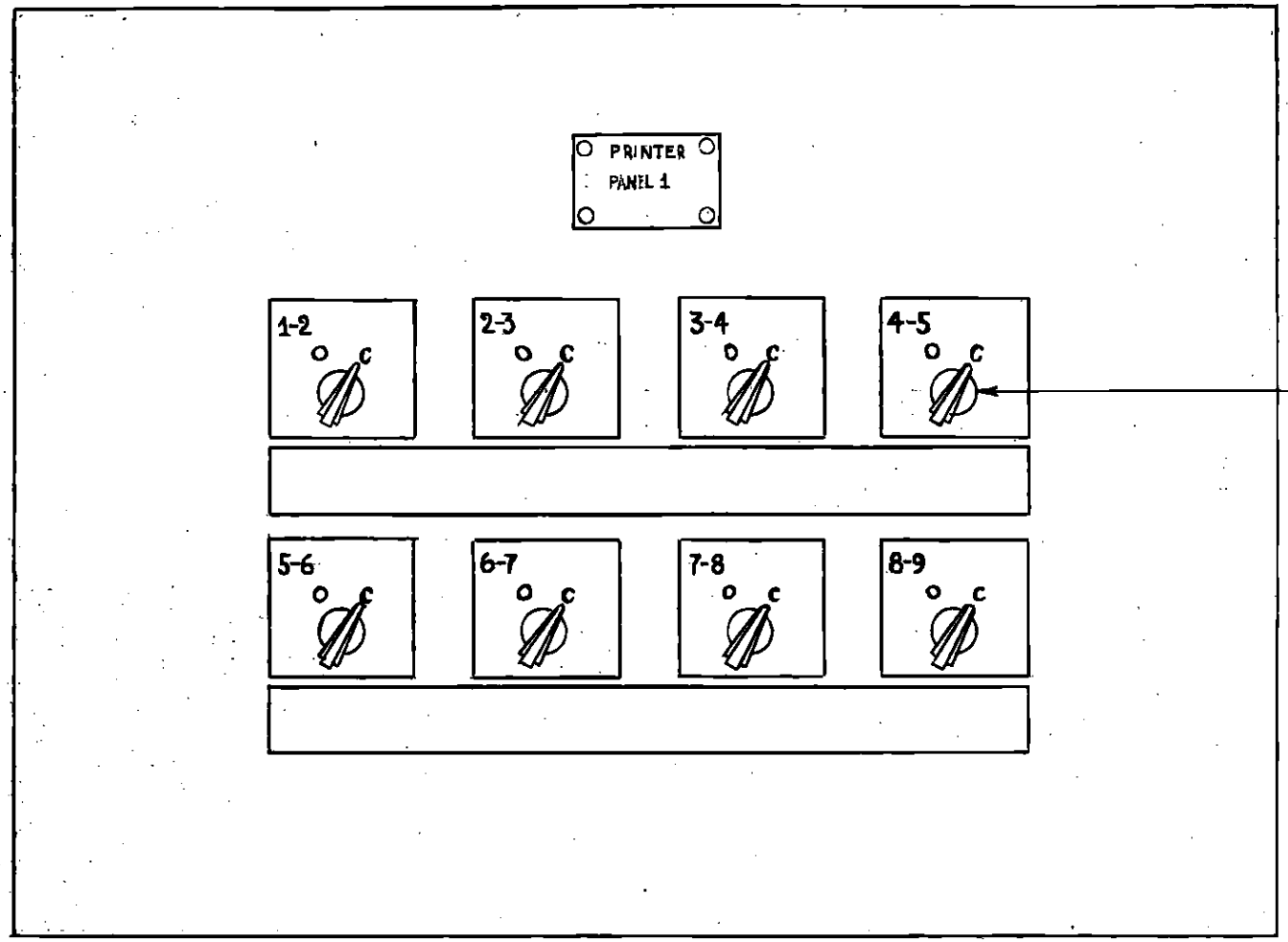
SET-UP OF FUNCTION TABLES* FOR PROGRAMMING TRANSMISSION OF CONSTANTS

	FUNCTION TABLE 1														FUNCTION TABLE 2													FUNCTION TABLE 3						
Lead / Arg.	PM1	A5	A6	A7	A8	A9	A10	B5	B6	B7	B8	B9	B10	PM2	PM1	A5	A6	A7	A8	A9	A10	B5	B6	B7	B8	B9	B10	PM2	PM1	A5	A6	A7	A8	A9	A10
0		9															9																		
1																		9															9		
2	M																																		
3		9															9																		
4	M	9																																	
5																		9															9		
6																	9	9																	
7 etc																																			
Use	←														— Transmit														→ Replace						
	x_{11}	x_{11} x_{22}	x_{12}	x_{13}	x_{13}	x_{14}	x_{15}	x_{21}	x_{21}	x_{23}	x_{23}	x_{24}	x_{25}	x_{31}	x_{31}	x_{32}	x_{33}	x_{33} x_{44}	x_{34}	x_{35}	x_{41}	x_{41}	x_{42}	x_{43}	x_{43}	x_{45}	x_{51}	x_{51}	x_{52}	x_{53}	x_{53}	x_{54}	x_{55}	x_{15} by x_{53} in acc. 6R	x_{42} in acc. 7L by x_{35} in acc. 7R
(i) immediately or (d) with one add. time delay	i	d	d	i	d	d	i	i	d	i	d	d	i	i	d	d	i	d	d	i	i	d	d	d	d	i	i	d	d	i	d	d	i		
Program line used for signal	3-2	3-3	3-4	3-5	3-6	3-7	3-8	3-9	3-10	3-11	4-1	4-2	4-3	3-3	4-5	4-6	4-7	4-8	4-9	4-10	4-11	5-1	5-2	5-3	5-4	4-5	5-6	5-7	5-8	5-9	5-10	5-11	6-1	6-2	6-4

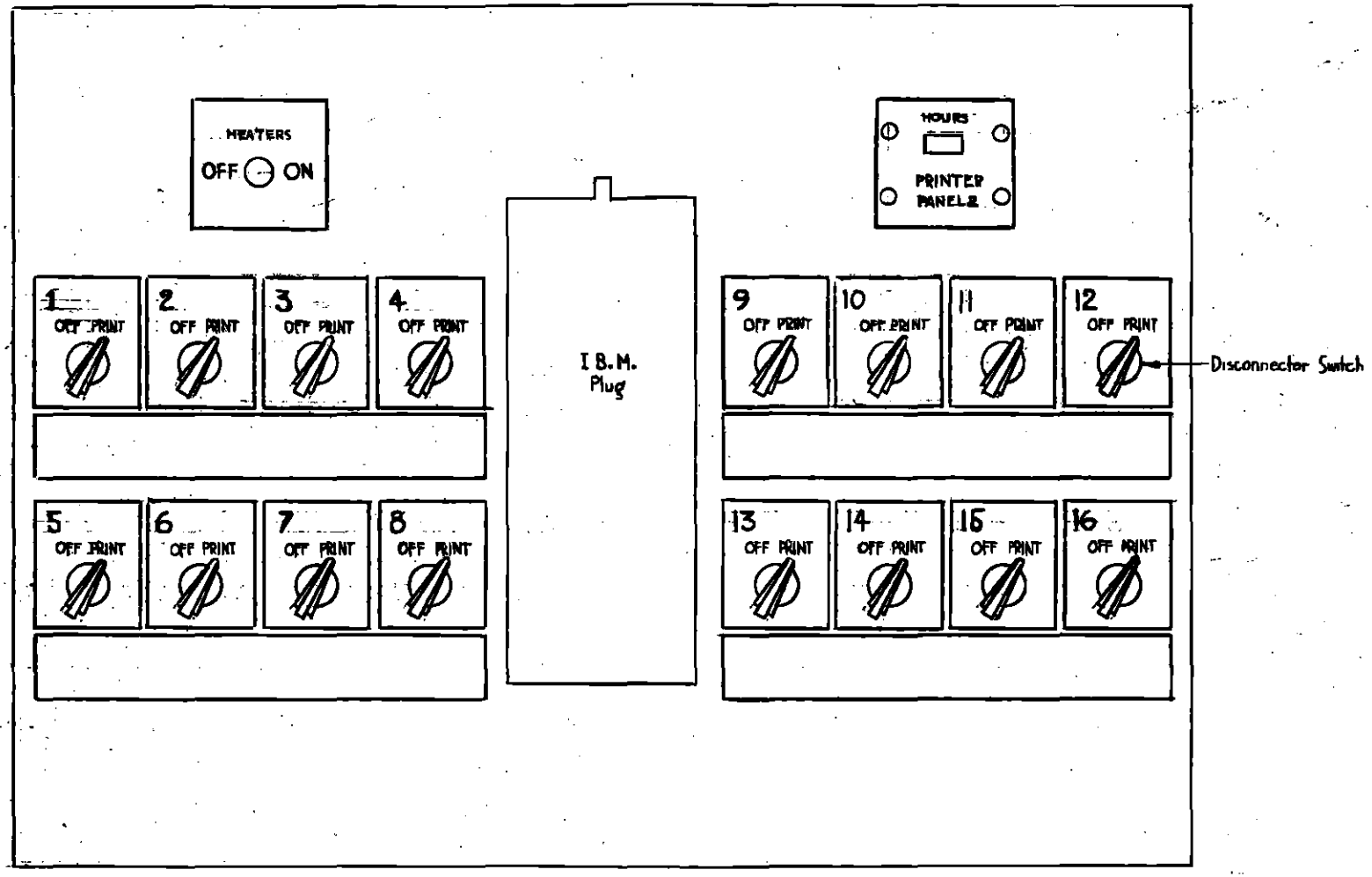
* It is assumed here that the function tables have been modified for the storage of programming data as suggested in Sec. 7.4. Furthermore, an adaptor is used at the function output terminals to take information from digit terminals to program terminals.

multiplication (1) leading to multiplication (2) etc. For group A, the predominant sequence also procures the arguments and stimulates accumulators to receive the products. The program pulses for this predominant sequence are carried in program trays 7 and 8. For group B, the predominant sequence includes the stimulation of the high-speed multiplier program controls used and also the stimulation for receiving products from the product accumulator. An auxiliary program sequence (carried in program trays 3-6) obtains from function tables 1, 2, and 3 programming instructions for procuring the arguments for the multiplications of group B. Group C is handled in the same way as group B except for the manner of stimulating reception of the product which is described below. The predominating sequence goes to steppers G and either E or F for instructions as to which argument to use and which high-speed multiplier program control to stimulate for a multiplication in group D (the program pulses in this sequence are carried on lines 9-1 through 10-2). A third auxiliary sequence (whose program pulses are carried in trays 10 and 11) stimulates the reception of the products from the product accumulator for groups C and D. Stepper K of the master programmer controls this third sequence.

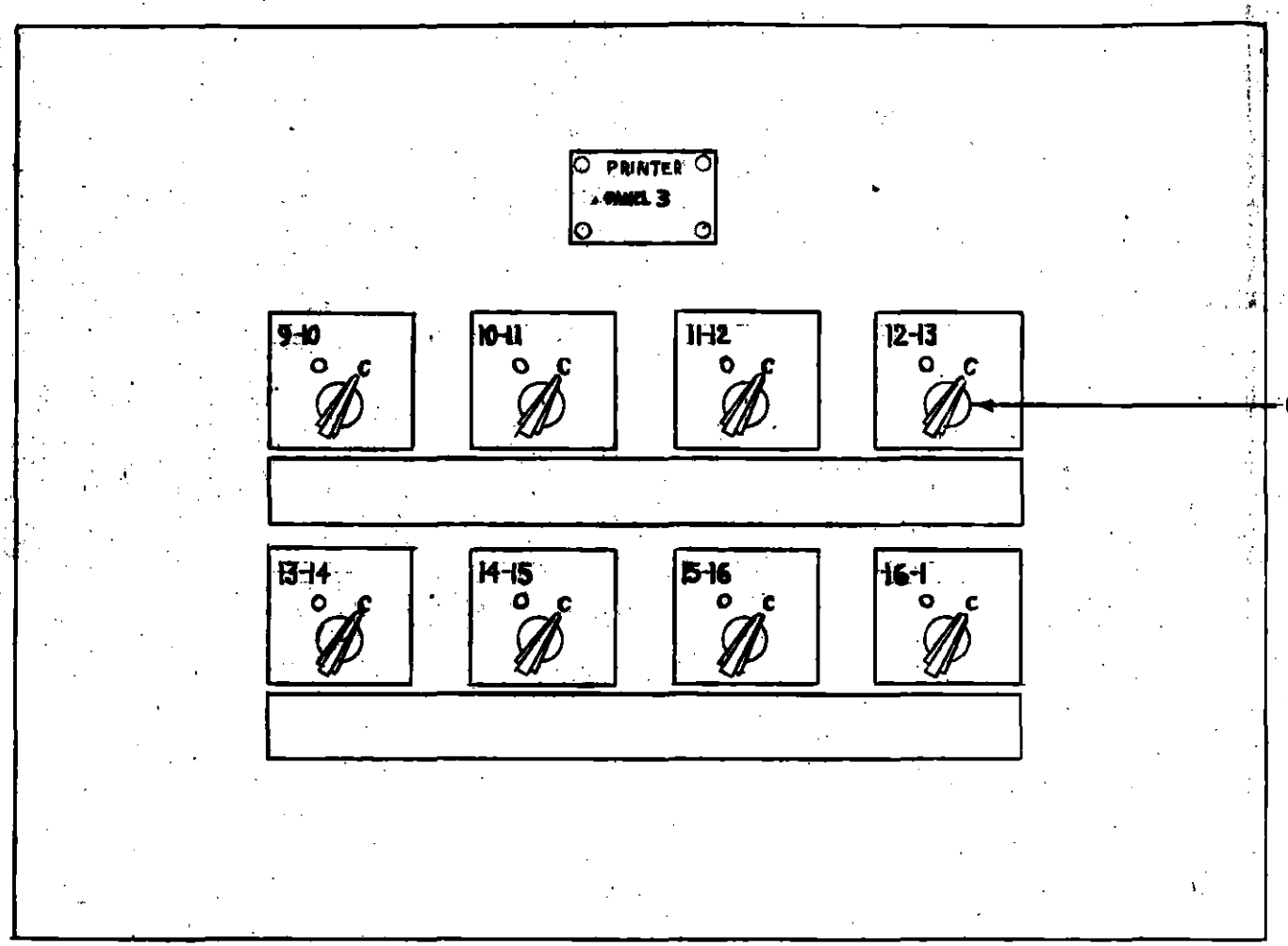
The set-up shown in Table 8-13 actually lists the events of sequence 2.1, Sequence 2.2 in which the terms ${}_6N_k$ are computed resembles sequence 2.1 except for the constants chosen for the multiplications of groups B, C, D, and E and the fact that reception of terms for the various N_k in accumulators 14, 16, 17, ..., 20 is through the β input channel. Sequence 4 is carried out in the same way as sequence 2 with the multiplication sequences A and B alternating. Sequence 5 in which the final results are printed is described in Section 9.5.



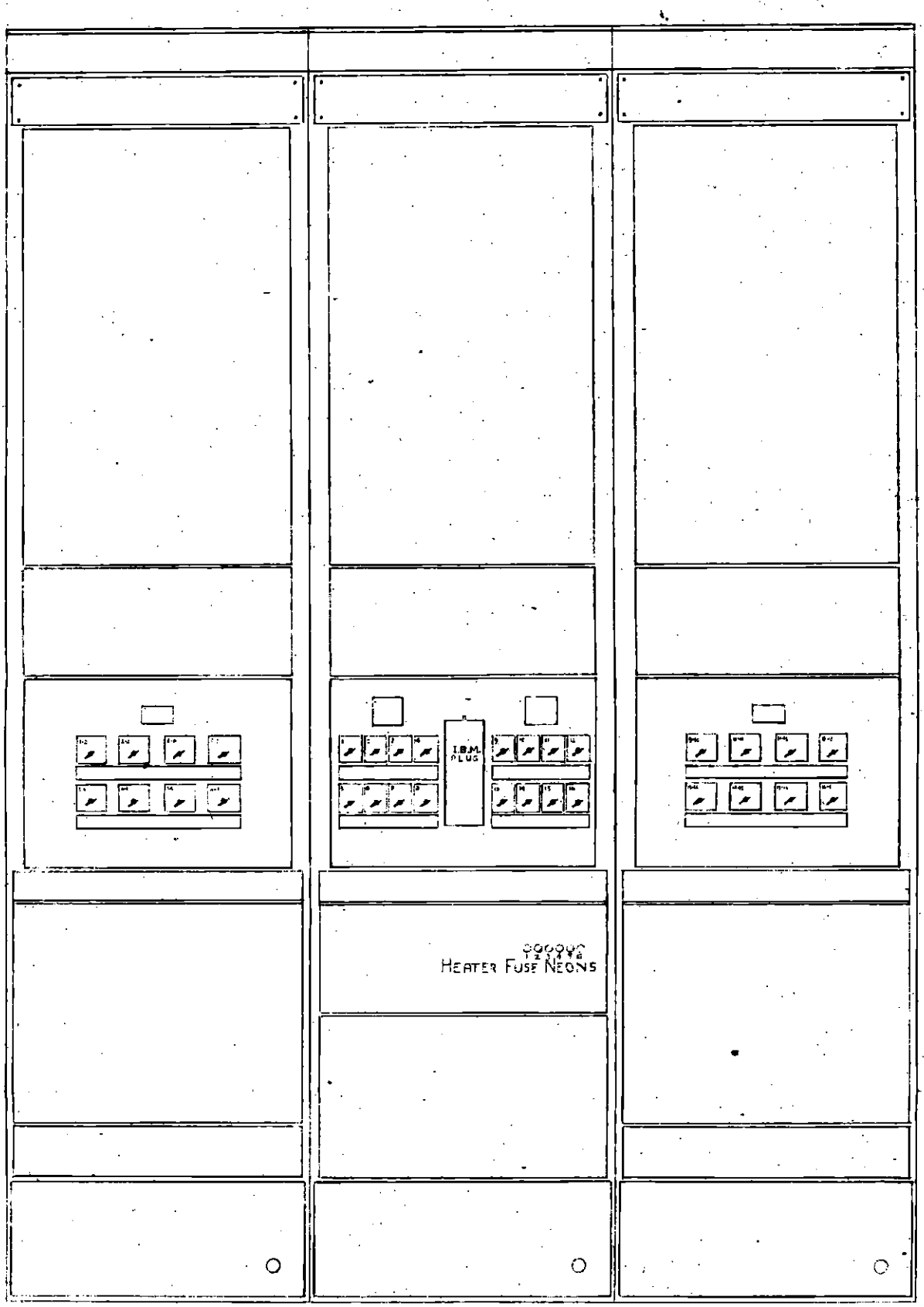
PRINTER
FRONT PANEL NO.1
PX-12-301R



PRINTER
FRONT PANEL NO.2
PX-12-302 R



PRINTER
FRONT PANEL NO.3
PX-12-303R



MOORE SCHOOL of ELECTRICAL ENGINEERING
UNIVERSITY of PENNSYLVANIA

PRINTER
ORDNANCE
PX-12-306

IX. PRINTER AND IBM GANG PUNCH

The ENIAC records 80 digits with as many as 16 signs on a standard IBM card (see Chapter VIII) by means of the printer which is connected to a modified IBM gang punch. Data to be recorded is delivered from the static outputs of master programmer decades and accumulator counters to the printer. Cards may be punched at the rate of approximately 100 per minute. When printing takes place, the counters from which data is recorded are tied up for about 150 ms. or 750 addition times which is only part of the total printing time (0.6 sec.).

The printer and IBM gang punch will be discussed in this chapter along the following lines: Sec. 9.1, programming circuits; Sec. 9.2, plug board of the IBM gang punch; Sec. 9.3, numerical circuits; Sec. 9.4, units connected to the printer. An illustrative problem is discussed in Sec. 9.5. The following diagrams will be referred to:

IBM Card Punch	PX-12-112
Printer Block Diagram	PX-12-307
Printer Front Panels	PX-12-301, 302, 303
Printer Front View	PX-12-306
IBM Punch Plug Board	PX-12-305
Initiating Unit Front View	PX-9-305
Initiating Unit Front Panel	PX-9-302

9.0 GENERAL SUMMARY OF THE IBM PUNCH AND PRINTER

Data stored in electronic counters of certain units of the ENIAC (see Sec. 9.4 for a list) is taken to an array of tubes in the printer by static output leads which run along a trough at the top of the ENIAC.

For each 5 digit group (of the total of 80 digits which can be punched on one card) there are 5 rows of 10 tubes each for the input of digital data. These tubes are labelled by a letter from A to E followed by a number between 0 and 9 inclusive. In addition, for each 5 digit group, there are 3 tubes for recording minus indication belonging to the group. Associated with each input tube is a printer relay. The printer relays for digits are labelled in the same way as are the tubes. The relays for minus sign indication are labelled M1, M2, and C_o. The last relay, C_o, is referred to as the carry-over relay. A printer relay is activated when its associated tube goes "on". The hold contacts on these relays are connected to the holding cam in the punch (see PX-12-112) so that when this cam breaks at time 9.5 in the card punching cycle* the printer relays release.

It is to be noted that the input tubes and printer relays are set up in accordance with the digital information as it is stored in the accumulators connected to the printer, i.e. complements** are set up as such. Complements are converted to negative numbers before punching takes place through the intervention of relays C_1 through C_5, the PM relays, M1 and M2, and the carry-over relay, C_o. The carry-over cam in the punch (see PX-12-112) also plays a part in this conversion.

In the IBM punch, as in the reader, there is an emitter with 12 stages (12, 11, 0, ..., 9 with stage 11 the minus punch stage). Certain stages of the emitter are connected through so called PM transfer contacts on the minus relays (M1 and M2) to contacts on the printer relays which

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*The card punching cycle is divided into 14 units as is the card reading cycle discussed in Sec. 8.0.3.

**In this chapter, the word complement is restricted to mean the complement of a positive number.

register digital information. The latter, in turn, are connected through transfer contacts on the relays C_1 through C_5 to lines which carry signals for punches in the various columns to the computer result exit hubs on the IBM punch plug board (see PX-12-305). By means of plug board wiring, these signals can be delivered to the punch magnets (see PX-12-112) for any desired column of the card.

Each of the 80 punch magnets operates a lever with a little head on it. When a punch magnet is activated, the lever moves forward and a hammer bar in the punch hits the head of the lever against a punch shaft. Thus, a hole is punched in the column with which the lever is associated. Since, throughout the punching, the card moves forward in synchronism with the emitter, the hole is punched in the digit row corresponding to the activated printer relay for that column.

Data may be punched in all 80 columns of the card or, if desired, certain columns or 5 digit groups may be left blank. If the print switch of a 5 digit group (see PX-12-302), which has the positions "print" and "off", is set at off, the printer input tubes for the group of numbers do not set up and punch signals for that group are not delivered to the IBM punch (see Secs. 9.2 and 9.4). No punch is made in a column for which there is no plug board connection between computer result exit hub and punch magnet hub.

The total of 80 digits can be broken up into signed 5, 10, 15, ..., or 80 digit groups by means of the coupling switches on panels 1, and 3 of the printer. The numbering on these switches corresponds to the numbering of the printer relay groups (see Secs. 9.2 and 9.4). When a coupling switch is set at C, the 2 five digit groups whose numbers appear on that coupling

switch are considered as one for sign indication purposes and for complementation. If two adjacent coupling switches are set at C, the three groups whose numbers appear on the switches are considered as a single 15 digit group, etc. The use of PM adaptors is also involved in the coupling or isolation of five digit groups (see Sec. 9.4).

Certain programming circuits for both the printer and punch are located in the initiating unit of the ENIAC and others are in the punch itself. Located at the initiating unit (see PX-12-307 and 9-302) are the printer program pulse input terminal, start flip-flop (68, 69), finish flip-flop (64, 65), synchronizing flip-flop (67, 68), program output pulse transmitter (70 - 72) and terminal. Neons correlated with these flip-flops are shown on PX-9-305. The start flip-flop operates a printer start relay located in the printer.

On the punch there are start and stop switches and a master-detail switch (which should, however, always be set at master). Inside the punch are found a start relay (R10), the motor hold relay (R9 and H.D. No. 1 motor relay, relays 1 and 3 which are associated respectively with the die card lever contact (Die CLC on PX-12-112) and the magazine card lever contact (Mag. CLC .), and relay 23. The program controls in this and the preceding paragraph have to do with starting and stopping the printer and punch and will be discussed at greater length in Sec. 9.1.

In addition to the switches and relays mentioned above, two of the cams in the punch, the interlock and reset cams, act as programming circuits. The timing for these cams is shown on PX-12-112 and 12-307. When the interlock cam makes contact, and when the starting relay located in the printer (see PX-12-307) is activated as a result of the reception of

a program pulse by the printer program pulse input terminal, the input tubes are connected to 20V, which allows all groups with print switch set at print to set up. When the interlock cam breaks (12.8-13.3), the input tubes cannot set up. The reset cam which makes in the period 11.2 to 11.8 provides a reset signal for the start flip-flop (68, 69) and sets the printer finish flip-flop (64, 65) which results, finally, in the transmission of a program output pulse by the printer (see Sec. 9.1).

9.1 PROGRAMMING CIRCUITS OF THE PRINTER AND IBM PUNCH

A program pulse received at the printer program pulse input terminal on the initiating unit flips the printer start flip-flop (68, 69) into the abnormal state. The resulting signal from the start flip-flop energizes the start relay in the printer.

Provided that there is at least one card in the magazine (so that Mag. CLC is closed and relay 3 is activated) and provided that there is a card in the punch position (so that Dic CLC is closed and relay 1 is activated), the signal from the printer start relay carried to the punch over circuit I-11 activates R23. As long as the printer stop switch is not thrown and under the conditions noted above for Mag. CLC and Die CLC the circuit to the punch start relay (R10) through R23 BL is now closed so that R10 is activated. Now, with contact R10 BL closed, the motor hold relay (R9) and the H.D. No. 1 motor relay in parallel with it are activated so that the drive motor starts up. Also, with R10 BU closed the printer clutch is activated so that a card is pushed through the punching apparatus. R10 holds through its hold contact R10 AL until cam P5 breaks at time 9 in the punch cycle.

With all the cards in the magazine and no card in the punch position, the printer cannot be started by the procedure described in the previous paragraph since Die CLC is open when there is no card in the punch position. If the start switch on the punch is depressed first, one or more cards (depending on how long this switch is depressed) move out of the magazine so that subsequently the punch and printer can be stimulated to operate by a program pulse received at Pi on the initiating unit.

The chronological operation of the punch, once the printer start relay is activated*, is summarized in Table 9-1.

The signal from the reset cam (during 11.2-11.8) is taken back to the printer program control circuit in the initiating unit via line 38. This signal resets the printer start flip-flop and sets the printer finish flip-flop. With the printer finish flip-flop in the abnormal state, a CPP is gated through [66] so that the printer synchronizing flip-flop is set. Thus, gate 69 is opened to allow a CPP to pass to the program output pulse terminal. Notice that the printer start flip-flop is reset so that it can recognize that a new printing program is to take place if another program input pulse is received and a program output pulse is transmitted about 750 addition times after Pi is stimulated or about 1/4 through the punching cycle.

If the printer is engaged in a printing program and another program input pulse reaches Pi before the start flip-flop is reset, naturally, the reception of this second program input pulse is not noted. Therefore, if printing programs are to follow closely on one another,

*About 10 ms elapse between the reception of a program pulse at Pi and the beginning of the card punch cycle.

TABLE 9-1

CHRONOLOGICAL OPERATION OF PUNCH

Time in Card Punch Cycle	Event
D = 13.5	Punch starts - interlock cam is making contact
14.5	Holding cam makes
12.8	Interlock cam breaks
11.0	Minus punches are made
11.2	Reset cam makes
11.8	Reset cam breaks
0 . . . 9	Digit punches are made
9.5	Holding cam breaks so that printer relays release
13.3	Interlock cam makes again so that input tubes can set up for next printing
13.5	Punch stops unless Pi received program pulse during period 11.2 - 13.5

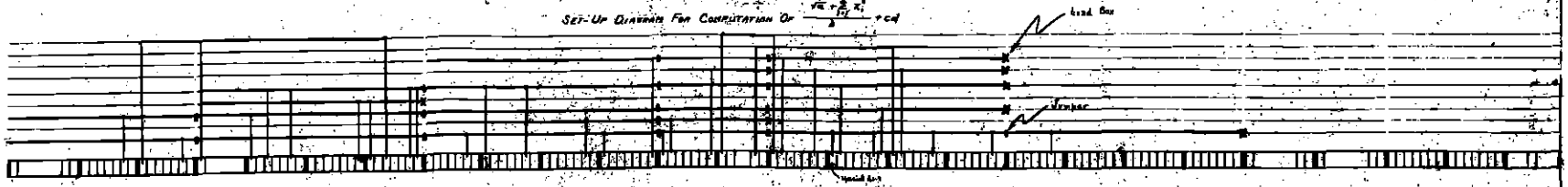
the programming sequences that culminate in a pulse to Pi should be initiated by a program output pulse from Po, the printer's program output pulse terminal, so that there will be no danger of the printer's receiving a program input pulse while the start flip-flop is in the abnormal state.

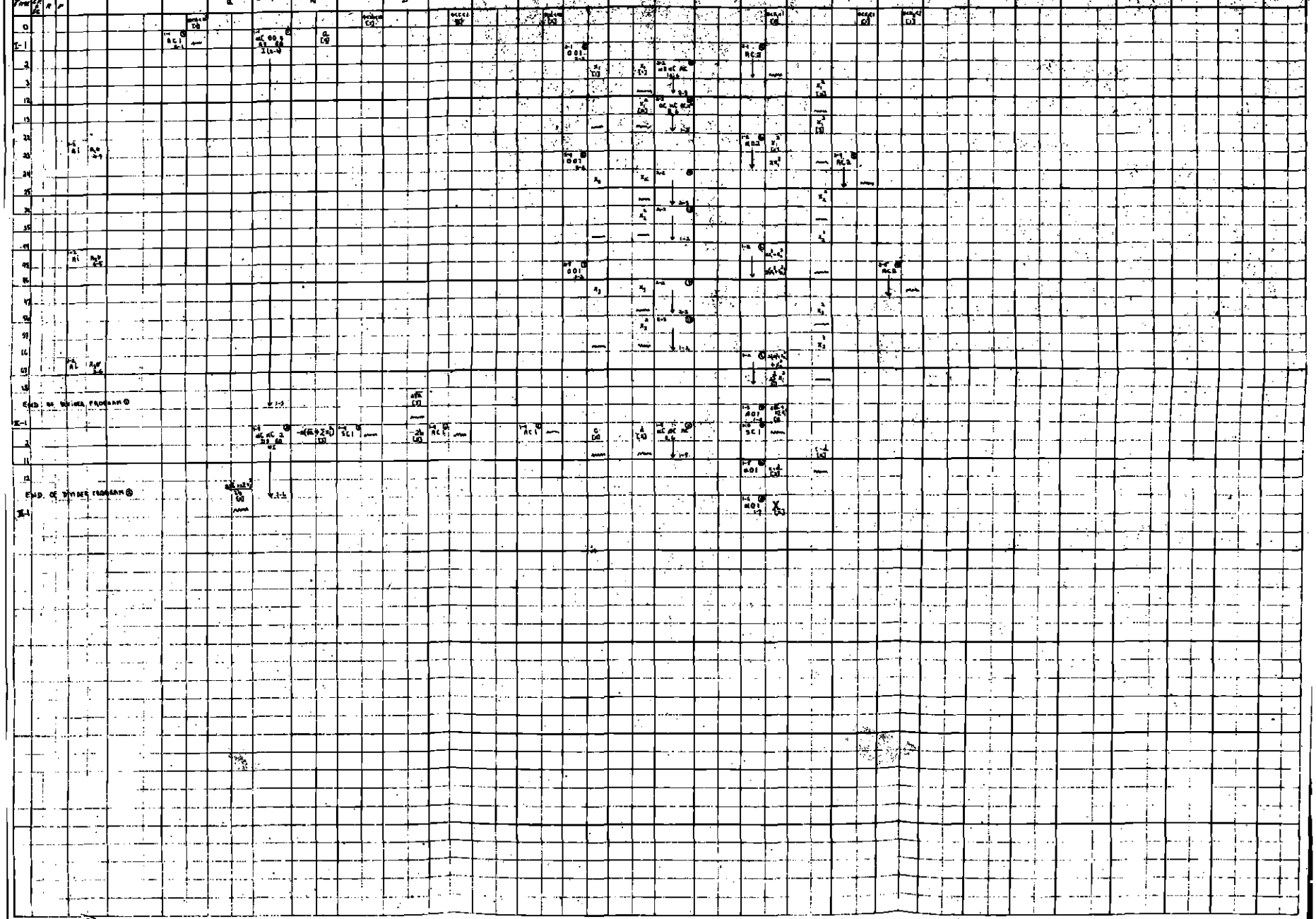
If the printer receives a program input pulse while engaged in printing but after the start flip-flop has been reset, then the start flip-flop is again flipped into the abnormal state. The printer and punch continue with the punching cycle in which they are engaged. Since the interlock cam breaks at time 12.8 (before the start flip-flop is reset) the printer input tubes cannot set up for the second printing program until at least time 13.3 in the punch cycle when the interlock cam once again makes contact (see Sec. 9.3 and Table 9-1). When the first punch cycle is completed, the printer and punch immediately start a second cycle in the event that Pi is pulsed between the resetting of the start flip-flop and the completion of the cycle.

When the interlock cam breaks at time 12.8 (without a safety factor, about 150 ms after Pi is stimulated) the printer input tubes drop out their information so that the units which are connected statically to the printer are free for computing purposes again. Before this time, such units cannot be called upon for computational programs. Program sequences which require computations in units connected to printer groups whose print switches are in the print position and which partly parallel printing should be initiated by the program output pulse from the printer, so that there will be no danger on this score. Units not connected to the printer are, of course, not affected by printing programs and can be used for computing programs throughout printing if such a set-up is desired.

TABLE SETUP

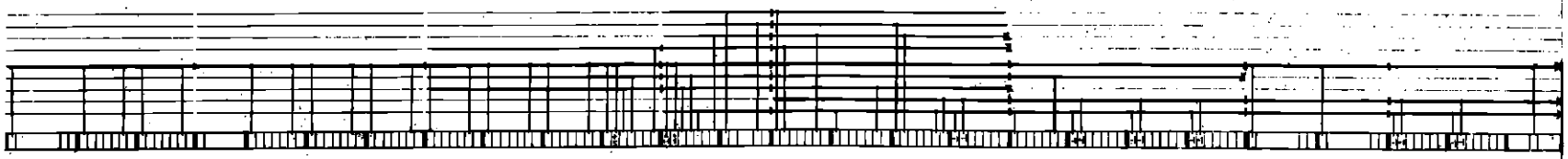
SET-UP DIAGRAM FOR COMPUTATION OF $\frac{\sqrt{a}+\frac{b}{c}x^2}{d}+e$





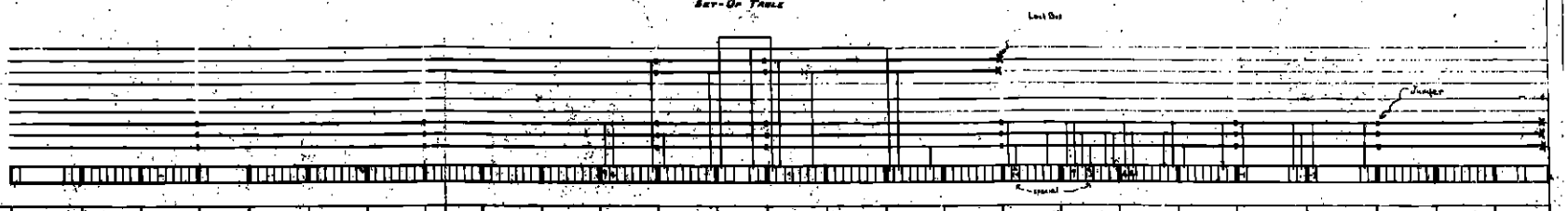
PX-10-414

TABLE 8-13a
SET-UP TABLE



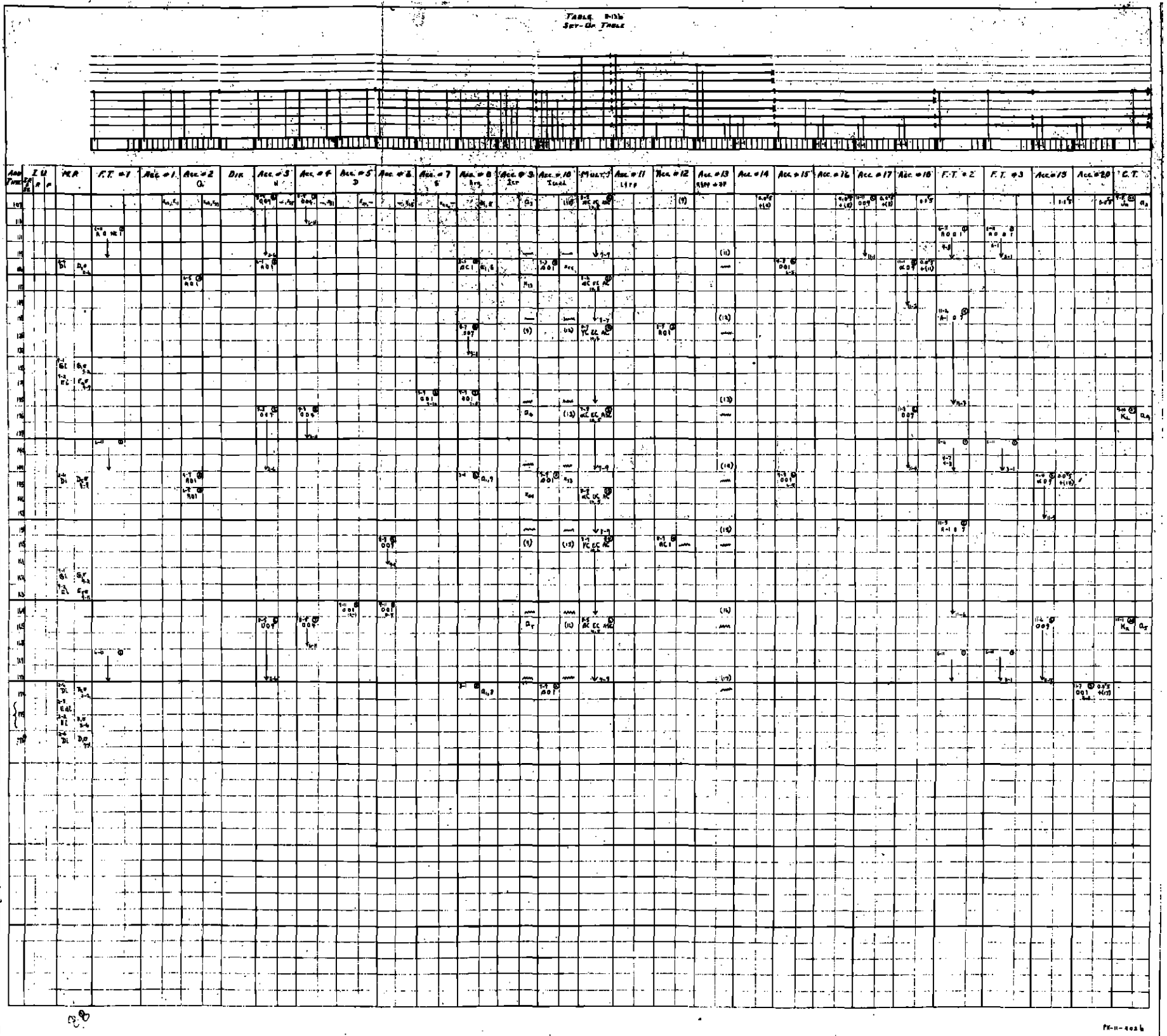
ADD TIME	E.U.	M.P.	F.T. #1	Acc. #1	Acc. #2	DIR.	Acc. #3	Acc. #4	Acc. #5	Acc. #6	Acc. #7	Acc. #8	Acc. #9	Acc. #10	MULT.	Acc. #11	Acc. #12	Acc. #13	Acc. #14	Acc. #15	Acc. #16	Acc. #17	Acc. #18	F.T. #2	F.T. #3	Acc. #19	Acc. #20	C.T.
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TABLE 7-4
SET-UP TABLE

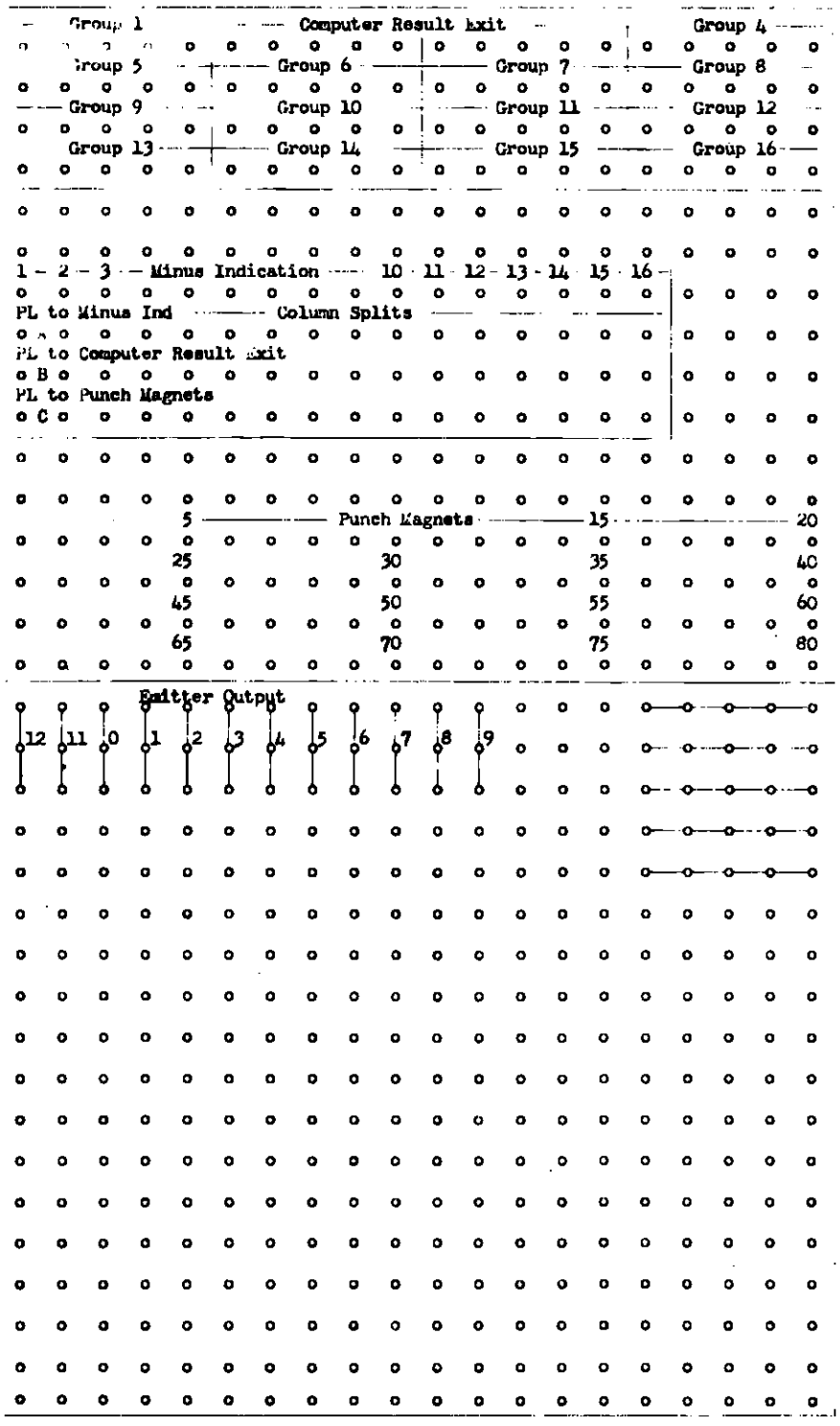


Acc. Func.	I.U.	PEA	F.T. #1	Acc. #1	Acc. #2	Div.	Acc. #3	Acc. #4	Acc. #5	Acc. #6	Acc. #7	Acc. #8	Acc. #9	Acc. #10	Mult.	Acc. #11	Acc. #12	Acc. #13	Acc. #14	Acc. #15	Acc. #16	Acc. #17	Acc. #18	F.T. #2	F.T. #3	Acc. #19	Acc. #20	C.T.
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PX-7-404


TABLE B-13b
SET-UP TABLE
Acc Time
I.U.
M.R.
F.T. #1
Acc. #1
Acc. #2
Div.
Acc. #3
Acc. #4
Acc. #5
Acc. #6
Acc. #7
Acc. #8
Acc. #9
Acc. #10
Mult.
Acc. #11
Acc. #12
Acc. #13
Acc. #14
Acc. #15
Acc. #16
Acc. #17
Acc. #18
F.T. #2
F.T. #3
Acc. #19
Acc. #20
C.T.

PLUG BOARD FOR GANG PUNCH



IBM Gang Punch
Plug Board
PX-12-3052

When the interlock cam makes contact again at time 13.3, the printer input tubes do not set up again in a given punch cycle unless Pi receives a program input pulse during the period 11.2-13.5 since the input tubes are connected to the interlock cam through a contact on the start relay.

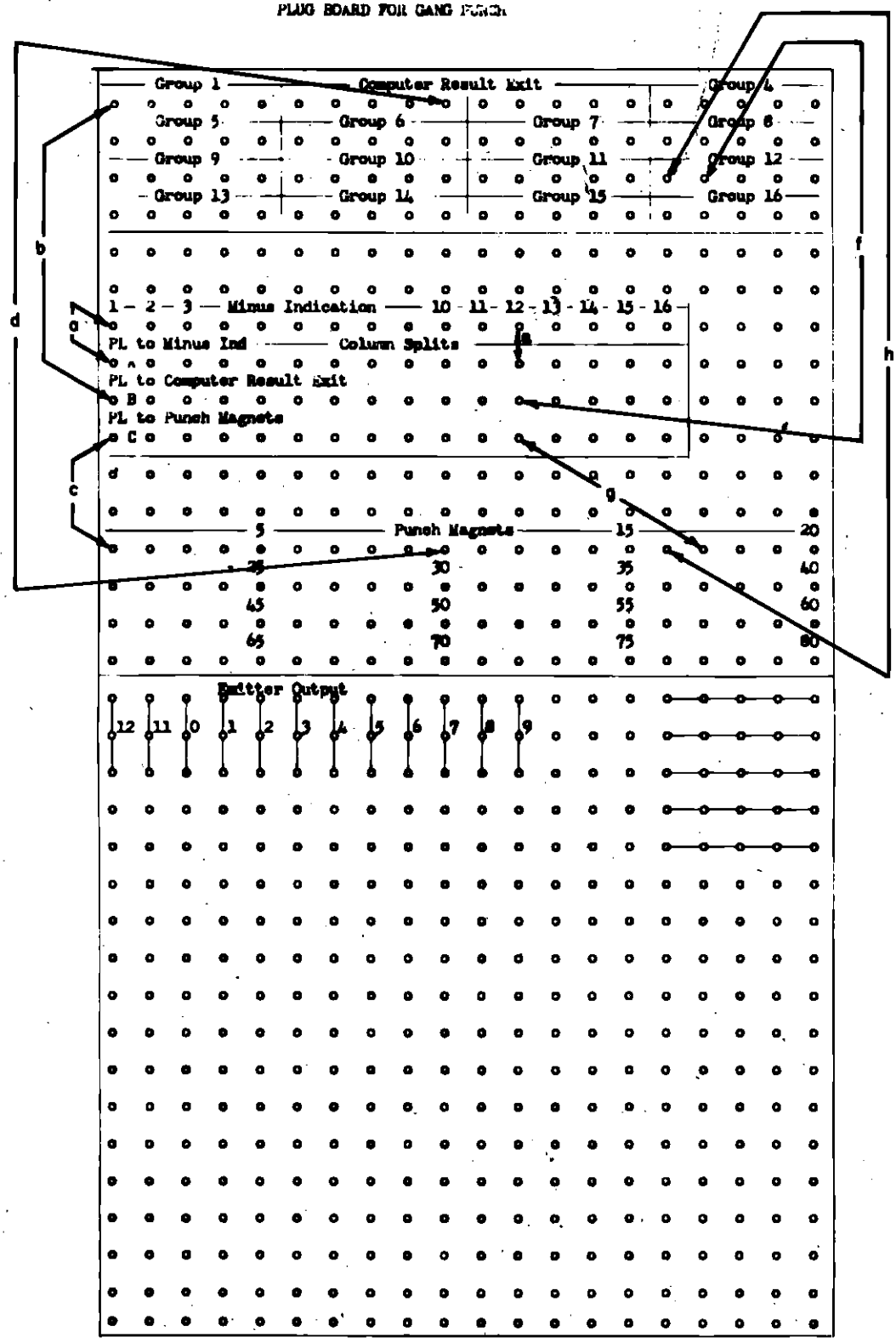
In the printer, as in the reader, a design is used in which a pulse stimulates successively the unsynchronized flip-flop, a gate, the synchronizing flip-flop, another gate, and the transmitter. This insures the emission of a program output pulse synchronized with the pulses in the rest of the ENIAC and of the proper shape.

It is to be noted that in this discussion a number of elements in the punch such as R22, R7, R8, R2, and R14 have not been mentioned. Discussion of these relays which, in a standard summary punch are functionally significant, has been omitted since in the card punch, as it has been modified for connection with the printer, they serve no logical purpose.

9.2 IBM GANG PUNCH PLUG BOARD

The IBM gang punch plug board is shown on PX-12-305. The computer result exit hubs appear at the top. These hubs are classified in 16 groups of 5 hubs each. The numbering of the groups here corresponds to the numbering of the groups of printer tubes and associated relays in the printer (see Sec. 9.4 for a list of the units connected to the various printer groups). From the printer relays that store digital information the computer result exit hubs receive signals via the cable that connects the printer to the punch. Each minus indication hub receives a signal from a contact on the M2 relay of the printer group bearing the same number as appears above the minus indication hub, if that printer group stores a complement.

PLUG BOARD FOR GANG PUNCH



PLUGGING FOR NEGATIVE NUMBERS

The 10 digits stored in the printer relays for groups 1 and 2 are to be printed in the columns 1-10 of the card (b,....d). Minus sign indication for these digits (a) is to be punched in column 1 (e).

The digits for the first and second places of printer group 12 (f and h) are to be punched in columns 96 (h) and 17 (g) respectively. The minus punch for group 12 (e) is to appear in column 17 (g).

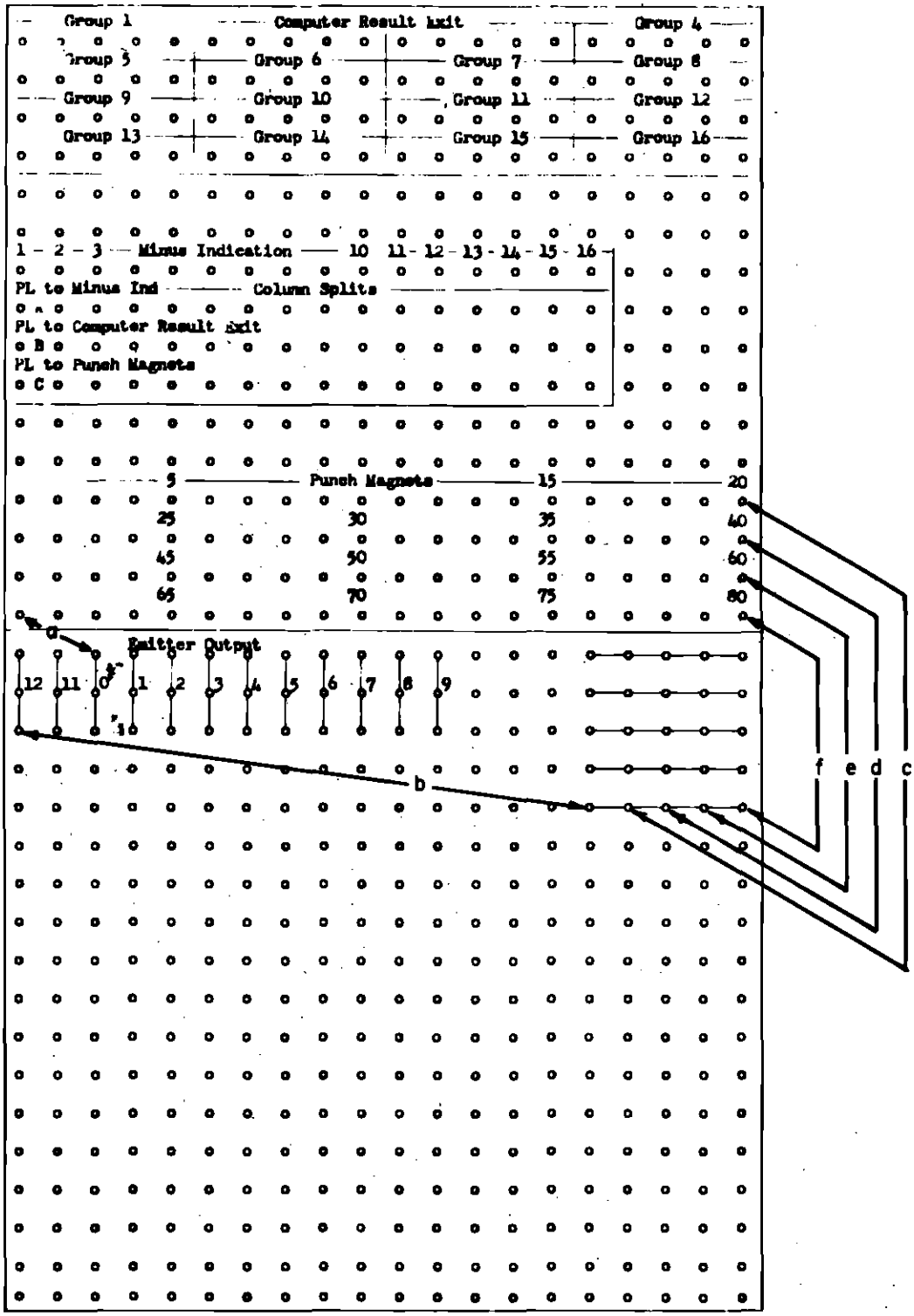
IBM GANG PUNCH
PLUG BOARD
PX-12-305R1

The 16 groups of 3 column split hubs on the gang punch plugboard are similar in operation to the group selection hubs on the reader plugboard but differ from the group selection hubs in purpose. On PX-12-112, it can be seen that there is normally a circuit from the B to C hubs but that when the column split relays (R11, R12, R17, and R18) are activated at the time when cam P2 makes (13.0-11.6) the circuit is from the A to C hubs. Thus, while minus punches are made there is a circuit from A to C, and while digit punches are made, there is a circuit from B to C.

The 80 punch magnet hubs are connected to the punch magnets each of which has responsibility for one of the 80 columns on the card.

The computer result exit hubs for printer groups which will always be used for recording positive numbers may be connected directly to the punch magnet hubs for the columns in which those numbers are to be punched. Special plugboard connections must be made for printer groups that record numbers which may or may not be complements. For such a printer group, the correspondingly numbered minus indication hub should be connected to an A hub of the column split hubs. The computer result exit hub which receives a signal for the digit to be punched in the same column as the minus punch for the group is connected to the B hub <u>below</u> the A hub chosen. The C hub is then connected to the punch magnet hub corresponding to the column in which both the digit and minus punch are to be made. Connections are made directly from computer result exit hubs to punch magnet hubs for the columns in which the minus punch does not occur. An example of the plugging required for the first and last digits of a ten digit negative number when the minus punch is to appear in column 1 is shown on PX-12-305 R1. Notice that while 2 printer groups record this number, only one minus indication

PLUG BOARD FOR GANG PUNCH



USE OF THE EMITTER OUTPUT HUBS AND COMMON TERMINALS

Line a: A zero punch is to be made in column 61.

Lines b,c,d,e,f: A 12 punch (b) is to be made in columns 20 (c), 40 (d), 60 (e), and 80 (f).

IBM GANG PUNCH PLUG BOARD PX-12-3052

hub is connected to an A hub of the column splits. This minus indication hub could just as well have been the group 2 hub instead of the group 1 hub as shown on PX-12-305 R1.

Corresponding to each of the 12 stages of the emitter there are 3 hubs. If an emitter output hub is connected to a punch magnet hub, the digit corresponding to the emitter output hub is punched in the column associated with the punch magnet hub whenever a card is punched. By means of connections from emitter output to punch magnet hub, a given digit punch can be made in as many as three columns.

To the right of the emitter output hubs are 5 groups of common terminals. All 5 terminals connected by a horizontal line are common. By plugging from an emitter output hub to one of a group of 5 common terminals and from each of the other four common terminals of the group to punch magnet hubs, the punch is instructed to punch the digit selected in 4 columns (see the illustrative example of PX-12-305 R2).

9.3 NUMERICAL CIRCUITS OF THE PRINTER AND PUNCH

If the print switch of a 5 digit group is in the print position, at the beginning of the card punching cycle while the interlock cam is making contact, the cathodes of all 53 printer input tubes for the group are connected through a contact on the printer start relay to a source of the required voltage for allowing the set up of these tubes. Thus when a program input pulse is received at Pi, the digit tubes connected through the static leads to the stages of counters in the abnormal state go on. The tubes associated with relays M1, M2 and C_o are connected to the static lead from the M stage of the PM counter of the unit from which the digits for the group come so that these tubes go on only if the number to be printed

is a complement. Thus if the number M 1 234 500 000 is stored in an accumulator which has its PM counter and five left hand decade counters connected to group 1 of the printer, the minus tubes M1, M2, and C_o and the digit tubes A1, B2, C3, D4, and E5 go on at this time. The "on" tubes activate the relays associated with them.

In addition to the hold contacts, two contacts for each of the digit relays, in other words, a total of 100 contacts for a 5 digit group, are arranged in a 10 by 10 array. PX-12-307 shows these contacts arranged so that the horizontal lines 2i-1 (where i = 1, 2, ..., 5 and where i = 1 identifies the bottom line) have the contacts for the relays used to represent the digits 9, 8, 7, ..., 0 and the horizontal lines 2i have the contacts for relays used to represent the digits 0, 9, 8, ..., 1 reading from left to right. Each vertical column of relay contacts is connected to one of 2 stages of the emitter through a PM transfer contact on either relay M1 or M2. The labelling on PX-12-307 indicates how these vertical lines are connected to stages j or 9-j of the emitter (reading from left to right j = 9 to 0) according as the PM relays M1 and M2 are in the normal state (when the group is a positive number) or the abnormal state (when the group is a complement).

In this manner the process of converting a complement into a negative number by subtracting the digits in each decade place from 9 is provided for. To complete the conversion, it is necessary to subtract from 10 instead of 9 the extreme right hand digit of the complement or the first from the right non zero digit of the complement and to leave the zero digits to the right of the first non zero digit. For this purpose, the relays C_1 through C_5 are used. If the coupling switches of a given 5 digit group are in the 0 position, and the number set up in the printer relays for that group is a complement (so that relay C_o is activated), then, when the carry over cam makes (13.6-9.4), the relay C_5 which is associated with the first place at

the right of the 5 digit group is activated. Relay C_4 is activated only if C_5 is activated and contact E0 is closed (as is the case when the first from the right digit of the group is a zero). Similarly, C_3 is activated only if C_5 and C_4 are and contact D0 is closed, etc. The case in which two or more 5 digit groups are coupled together by means of the C setting on one or more coupling switches is similar to this except that it is the C_5 relay for the group of highest number which is activated if the number registered in the printer groups is a complement. The C_4, C_3, ... relays for this highest numbered group are activated or not depending on the presence or absence of zeros in the right hand places of the complement.

Now either an odd (reading from the bottom up) line or its immediate even successor is connected through a transfer contact (on one of the relays C_1 through C_5) to a line which carries a punch signal back to the computer result exit hubs. An even numbered line is connected to a punch signal line only when the relay C_1, C_2, ..., or C_5 corresponding to that punch signal line is activated; otherwise punch signals come from the odd numbered lines.

A signal for a digit punch results from the establishment of a circuit from an emitter stage through a PM transfer contact, through a contact on a digit relay through a transfer contact to a computer result exit hub. A signal for a minus (11) punch reaches a minus indication hub as a result of a circuit from stage 11 of the emitter through a contact on relay M2.

Table 9-2 illustrates the process of converting data stored in the printer relays into punches on an IBM card. It is assumed that the coupling switch for the printer relay group in which the numbers are stored

TABLE 9-2

OPERATION OF NUMERICAL CIRCUITS OF PRINTER AND PUNCH
Coupling Switches set at 0

NUMBER to be PUNCHED	EMITTER STAGE	is connected through PM TRANSFER CONTACT	to a Contact on RELAY	which is connected through TRANSFER CONTACT	to COMPUTER RESULT EXIT HUB
P 13057	0	M1	C0	C_3	3
	1	M1	A1	C_1	1
	3	M1	B3	C_2	2
	5	M2	D5	C_4	4
	7	M2	E7	C_5	5
M 13057	11	Minus punch is made			
	3	M2 (A)	E7	C_5 (A)	5
	4	M2 (A)	D5	C_4	4
	6	M1 (A)	B3	C_2	2
	8	M1 (A)	A1	C_1	1
	9	M1 (A)	C0	C_3	3
M 13570	11	Minus punch is made			
	0	M2 (A)	E0	C_5 (A)	5
	3	M2 (A)	D7	C_4 (A)	4
	4	M2 (A)	C5	C_3	3
	6	M1 (A)	B3	C_2	2
	8	M1 (A)	A1	C_1	1

is in the 0 position. The symbol (A) after a relay number indicates that the relay is activated. The table is arranged to indicate the chronological order in which the punches are made. The punching of the first number P 13057 is a straightforward example of what happens when a positive number is punched. The case, M 13057, illustrates the conversion of a complement into a negative number, and the case, M 13570, illustrates the conversion of a complement with at least one zero at the far right.

9.4 UNITS CONNECTED TO THE PRINTER

The static outputs of the counters in any accumulator or in the master programmer can be connected to the printer input tubes. To deliver information for five digits and a sign to the printer, a 55 conductor cable is used. Each of 50 leads connects the static outputs of 1 stage of one of the 5 decade counters to a printer input tube . Another lead delivers the static output of the M stage of the PM counter to the minus indication tubes associated with the 50 printer tubes for the 5 digits*. The 16 cables used for the 80 digits and 16 minus signs that can be punched are carried in a trough which runs along the top of the ENIAC.

At the time of writing of this report, the following connections have been established between units of the ENIAC and printer groups:

---

*When 10 digits and sign are printed from a given accumulator, the static output of stage M is connected to the PM lead in each of 2 static output cables through the use of adaptor A on PX-12-114. When 5 digits without sign indication are printed from an accumulator or from the master programmer, no connection is made to the PM lead in the static cable, and adaptor B shown on PX-12-114 is connected to the socket in the printer which goes to the PM tubes of the 5 digit group.

Printer Groups	Connected to
1*	Master Programmer decades 14 - 18
2 and 3	Accumulator 13 - 10 decades and PM
4 and 5	Accumulator 14 - 10 decades and PM
6	Accumulator 15* - decades 6-10 and PM
7 and 8	Accumulator 16 - 10 decades and PM
9 and 10	Accumulator 17 - 10 decades and PM
11 and 12	Accumulator 18 - 10 decades and PM
13 and 14	Accumulator 19 - 10 decades and PM
15 and 16	Accumulator 20 - 10 decades and PM.

The static outputs of decades 1-5 of accumulator 15 are also delivered to the printer in the static output trough but the leads are not plugged into the printer input sockets. If it is desired to print 10 digits from accumulator 15 and none from the master programmer, the leads from the master programmer should be pulled out and those from accumulator 15 plugged in instead. Notice that a ten digit negative number cannot be printed from accumulator 15 since there is no way to couple together groups 6 and 1. It is, however, possible to print either of the following from accumulator 15:

1) A ten digit positive number

2) Two five digit numbers with the left hand number having any sign and the right hand number only a plus sign.

The connections made to the printer make it possible to use the printer in a moderately flexible way. For example, even though ten decades of an accumulator are connected to the printer, it is not necessary that all

ten columns be punched when data from this accumulator is printed. If there are five or fewer significant figures of a result to be printed from an accumulator which has 10 decades connected to the printer and if those figures are located in the five left hand or five right hand decade places of the accumulator, the punching of columns in which the non-significant figures are located can be avoided by setting the print switches of the higher or lower numbered five digit group respectively to off. If the significant figures are at the left of the accumulator the coupling switch which carries the numbers of the 2 printer groups connected to that accumulator must certainly be set at 0 so that complementation will be carried out correctly. If the significant figures are at the right of the accumulator, the coupling switch may be set at either C or 0.

Another method which eliminates the punching of non-significant zeros consists of omitting plug board connections between punch magnets and those computer result exit hubs which receive the non-significant zeros.

Another procedure which is possible under certain circumstances consists of printing two five digit numbers from an accumulator which has 10 decades and its PM connected to the printer. When the two numbers stored in the accumulator always have the same sign, the standard PM adaptor labelled A on PX-12-114 which connects stage M of the accumulator's PM counter to the static leads which go to the printer PM tubes for both five digit groups is used. The coupling switch for the two printer groups is set at 0 so that tens complements are taken in converting each number into a negative number when the common sign is M.

When one of the five digit numbers is always positive and the other may be either positive or negative, the static connection from the

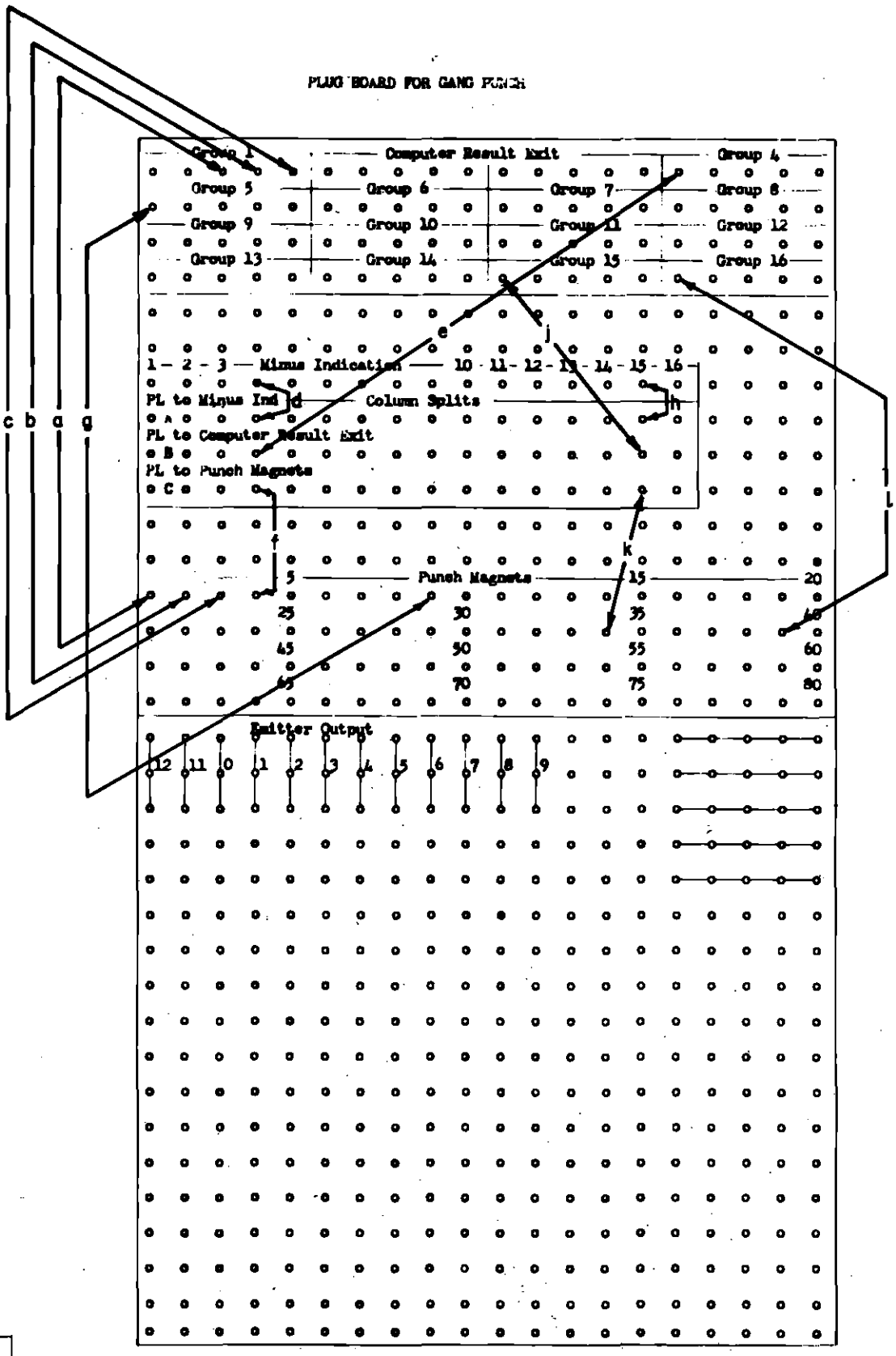
accumulator's PM counter to the PM tubes for the positive group is broken for, otherwise, complements would be taken for both five digit groups and both groups would be printed as negative numbers. In this case, moreover, the adaptor labelled B on PX-12-114 is connected to the socket in the printer which goes to the PM tubes of the positive group. This adaptor grounds the grid of the PM tubes. The coupling switch associated with the two printer groups is set at 0 so that a tens complement will be taken in converting numbers with sign M into negative numbers.

If both five digit numbers may have different signs and if one of the five digit numbers is not known to be always positive, there is no way to print both numbers correctly from one accumulator.

9.5 ILLUSTRATIVE PROBLEM SET-UP

The printing sequence of the problem discussed, in part, in Chapter VIII is taken here to illustrate the use of the printer. The problem may be summarized briefly as follows: Six numbers, N_k (for $0 \leq k \leq 5$), are formed in accumulators 14 and 16-20 by the end of sequence 4 (see Tables 8-8 and 8-10. Since the significant figures switches on these accumulators are set at 6 (see Figure 8-3), the values are correct to 6 figures. The four irrelevant right hand digits, however, have not been deleted. Master programmer decades 14-18 (associated with stepper C) store the identification number for the results.

In sequence 5, the numbers N_k are printed and the reading of constants for the next computation proceeds in parallel. When printing is completed, selective clearing takes place. The program output pulse from a selective clearing transceiver provides a reader interlock pulse. The reader program output pulse goes back to the master programmer (see Figure



PLUGBOARD WIRING FOR PRINTING IDENTIFICATION NUMBERS AND VALUES OF N_k

Lines a, b, c: wiring for identification number

Lines d, e, f, g: wiring for first and last digits of N_0

Lines h, i, k, l: wiring for first and last digits of N_5

IBM GANG PUNCH
PLUG BOARD
PX-12-30523

8-2 from which will come a program output pulse to stimulate the computations for the next system of equations.

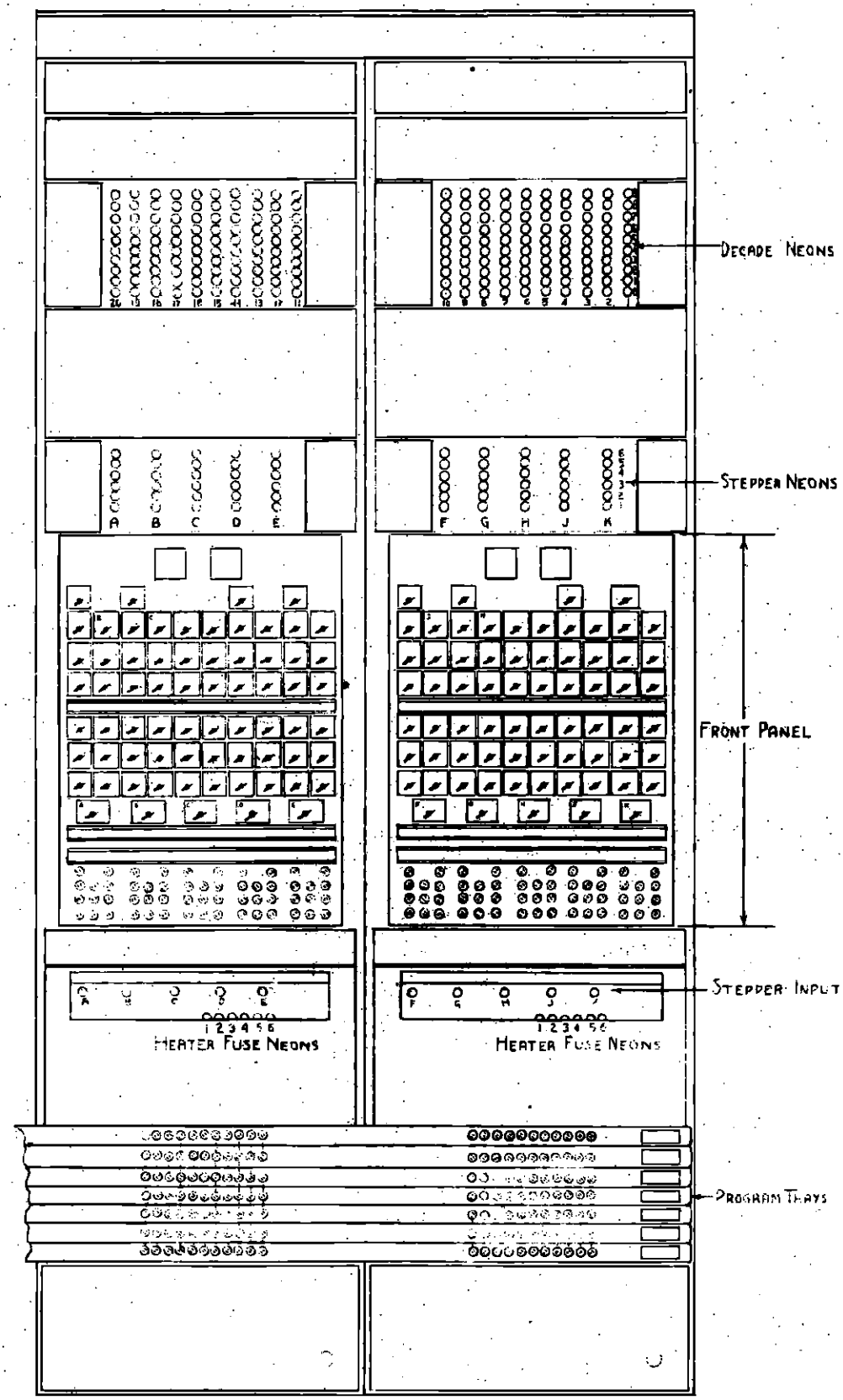
The set-up for this sequence, sequence 5, is shown on Table 9-3 and Figure 9-1 (a and b) is a set-up diagram for this sequence. Master programmer decades 14-18 are connected to printer group 1 and, therefore, the coupling switches 1-2 and 16-1 are set at 0 (see Figure 9-1). Since 6 digits are being printed from accumulators 14, 16, 17, ..., 20, coupling switches 4-5, 7-8, 9-10, 11-12, 13-14, and 15-16 are set at C. All other coupling switches are set at 0. The print switches for the 13 printer groups used here are set at print with all others set at off.

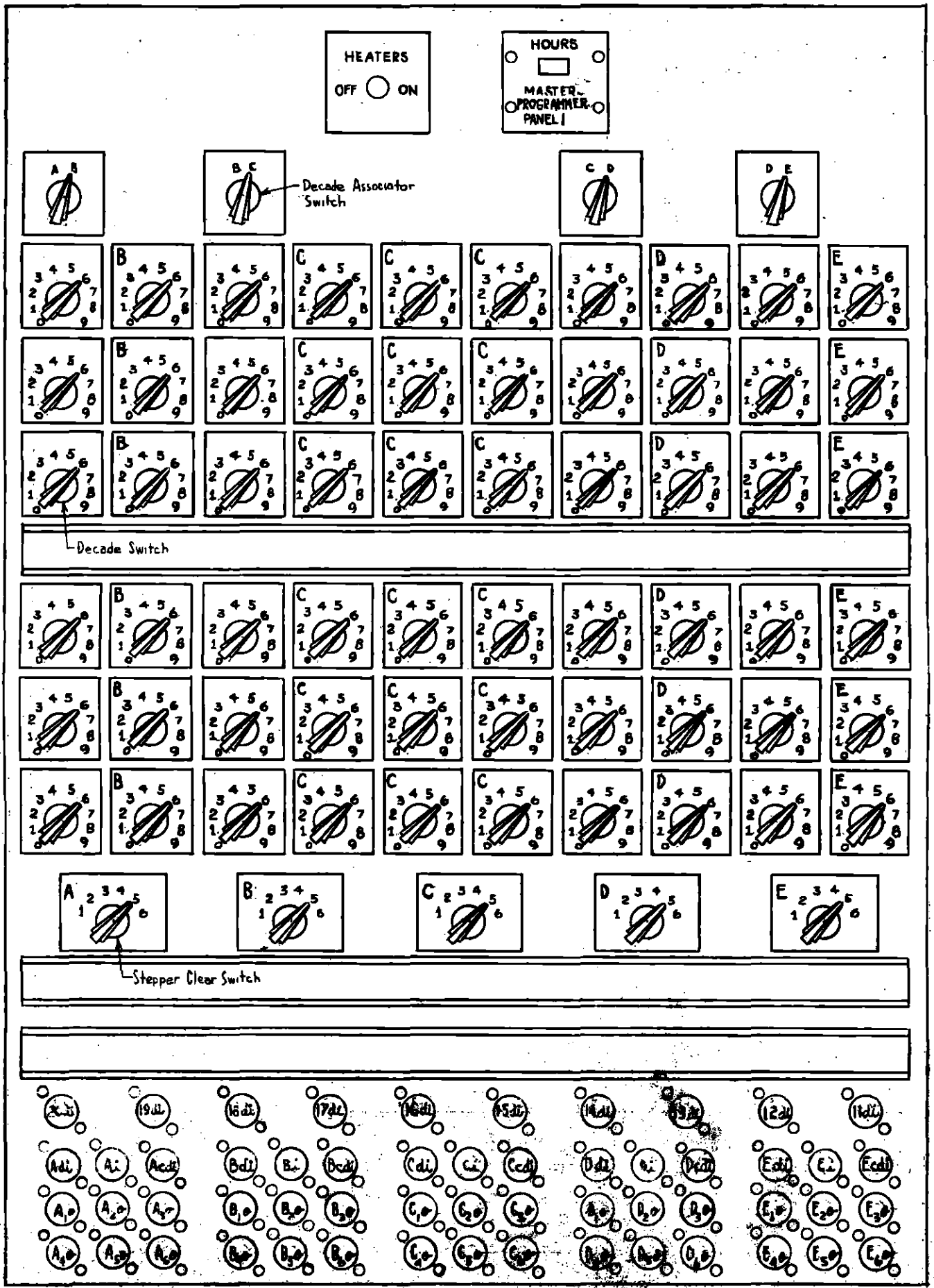
A possible plug board wiring for printing the numbers involved is shown on PX-12-305 R3. Notice that even though 10 digits are set up in the printer groups for each value of N_k, only 6 digits are printed since connections from computer result exit hubs to punch magnet hubs for the four digits at the right in each pair of five digit printer groups are omitted.

TABLE 9-3

SET-UP FOR SEQUENCE 5 - EVALUATION OF N_k

Add. Time	Selective Clear	Reader	Printer	Accumulator 14		Accumulator 16	Accumulator 17	Accumulator 18	Accumulator 19	Accumulator 20
V-0					$N_1+0.0^55$	$N_1+0.0^55$	$N_2+0.0^55$	$N_3+0.0^55$	$N_4+0.0^55$	$N_5+0.0^55$
V-1			2-5 Pi	2-5 0 0 1 2-3						
2		2-3 Ri								
VI-1			Po 2-10							
2	2-10 C_1 2-7									
3		2-7 Rl								
VII-1		Ro 1-1								

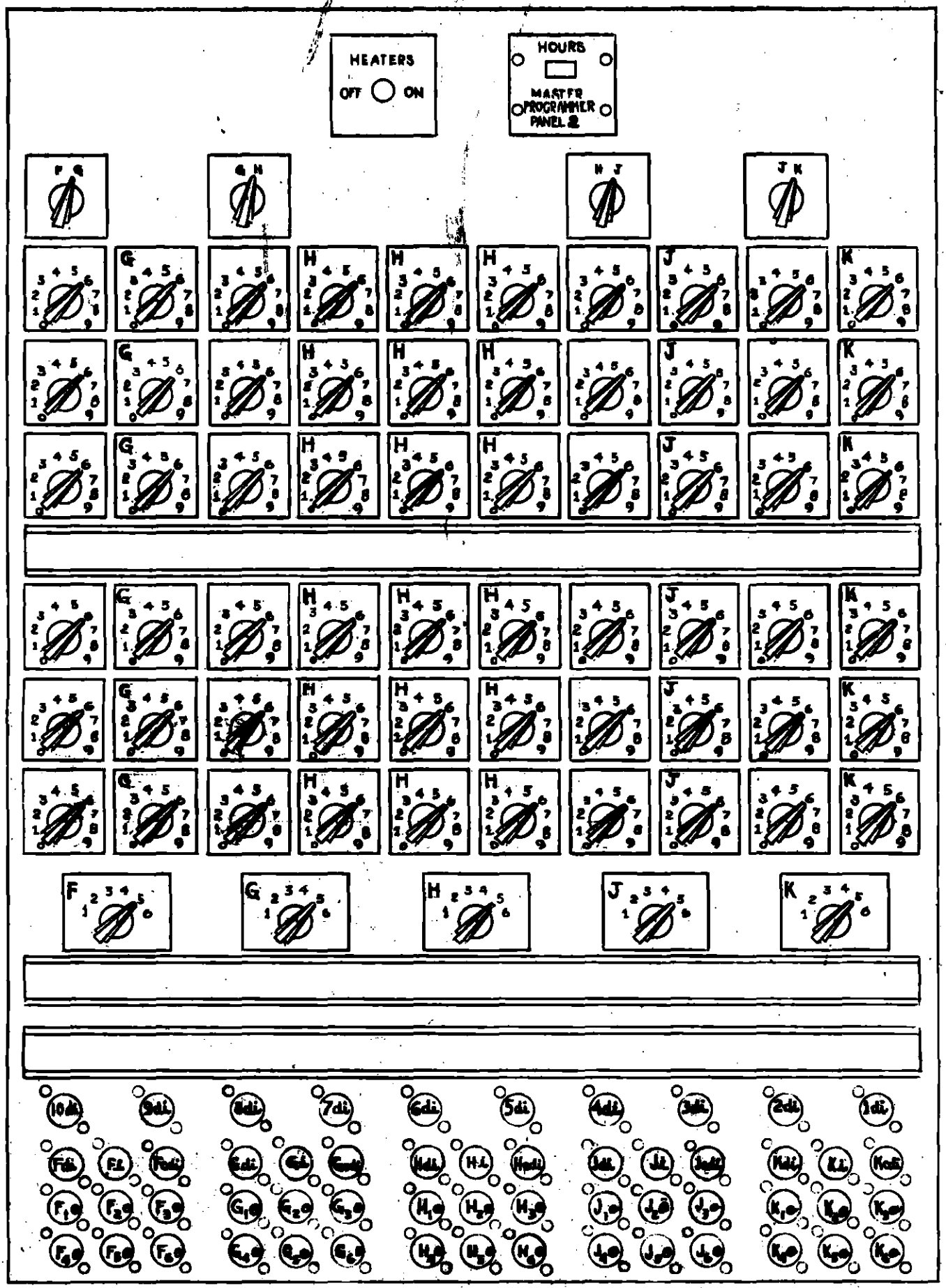

DECADE NEONS
STEPPER NEONS
A B C D E
F G H J K
FRONT PANEL
STEPPER INPUT NEONS
1 2 3 4 5 6
HEATER FUSE NEONS
1 2 3 4 5 6
HEATER FUSE NEONS
PROGRAM TRAYS



TERMINALS Ai, Bi, ---Ki - Stepper input
TERMINALS Adi, ---Kdi — Stepper direct input
TERMINALS Acdi, ---Kcdi — Stepper clear direct input

TERMINALS $A_1o, A_2o, \ldots A_6o$
Stepper output terminals, associated respectively with stages 1, ---6 of stepper A

MASTER PROGRAMMER
FRONT PANEL NO. 1
PX-8-301R



TERMINALS 1di, 2di---, 20di — Decade direct input terminals associated respectively with decades 1, 2, ---20 (counted from right to left).

MASTER PROGRAMMER FRONT PANEL NO. 2 PX-8-3028

X. MASTER PROGRAMMER

The master programmer is a central programming unit whose primary function is to direct and stimulate the performance of the program sequences of various levels which enter into a computation. While the master programmer is capable of stimulating the performance of individual programs, it is usually not required for this purpose. It is, however, essential to use the master programmer to accomplish the iteration of a program sequence into a chain (see Section 1.4.) or to link together chains and program sequences. The master programmer can link programs together either serially or on the basis of magnitude discrimination. The master programmer may also be used as a counter in that it is capable of storing numbers (without sign, however) and also of adding by counting pulses. This latter feature enables the operator to store values, say of the independent variable, in the master programmer. Certain decades of the master programmer have been connected to the printer so that a number stored in these decades can be printed.

Sections 1, 2, and 3 of this chapter are concerned with the components of the master programmer. The programming of the master programmer is discussed in Section 4, and the uses of the master programmer are considered in Section 5. Illustrative set ups involving the master programmer are found in Section 6. Reference will be made to the following diagrams:

Master Programmer Front View	PX-8-303
Master Programmer Front Panels	PX-8-301, 8-302
Master Programmer Block Diagram	PX-8-304

10.0 GENERAL SUMMARY

The master programmer has ten steppers (identified by the letters A-K on PX-8-301 and 302). The basic property of a stepper is that it has one input and 6 outputs. By means of the 6 output terminals, a pulse received at a stepper input terminal from a given program line can be routed to one of 6 program lines.

Each stepper has a 6 stage counter. The output terminal through which a pulse is emitted when a stepper input is stimulated depends on the stage of the stepper counter at the time when the pulse is transmitted.

The master programmer also includes 20 master programmer decades (numbered 1-20 beginning with the extreme right hand decade on panel and ending with the extreme left hand decade on panel 1). By means of decade associator switches as many as five decades can be combined into a group, and, as a group, associated with a stepper.

The group of decades associated with a stepper counts one each time the stepper is pulsed. Each decade has associated with it 6 decade switches, one for each stage of a stepper counter. When the stepper counter is in stage s and when the decades associated with a stepper register the number set up on the decade switches belonging to stage s of the associated stepper, the stepper advances from stage s to stage s+1 and the decades associated with the stepper clear to zero. Thus, the decades and decade switches make it possible for a stepper to emit a pulse from the output terminal associated with stage s of the stepper on the number of occasions specified by the settings of the stage s decade switches and then to emit a pulse from the output terminal associated with stage s+1 of the stepper counter.

Besides the preceding there are other features of the master programmer which provide means of controlling the stepper counters and decade counters. Each decade counter has a direct input (labelled by the decade number followed by di). Each pulse received at a decade direct input terminal cycles the decade counter one stage. Similarly each pulse received at a stepper direct input terminal (di preceded by the stepper letter) cycles the stepper counter 1 stage. A stepper is cleared to stage 1 by pulse input to its clear direct input. (cdi preceded by the stepper letter). A stepper clear switch associated with each stepper unit makes it possible to use a stepper counter as a c stage counter where $1 \leq c \leq 6$.

10.1. DECADE ASSOCIATOR SWITCHES

Certain decades are permanently associated with one another and, as a group, with a particular stepper. For example, decades 15, 16, and 17 are permanently associated with one another and with stepper C. Other decades (decades 12, 14, 18, and 20 on panel 1, for example) can be associated by means of a decade associator switch with either of the 2 steppers whose identifying letters appear on the switch and thus, with the other decades permanently connected to that stepper. Notice that steppers A and F may be used without any associated decades.

The decades of a group are connected to one another for the purpose of carry-over and, as a group, are associated with a stepper to provide one of the signals which can cycle the stepper counter at certain times (see Section 10.2.2.).

10.2. MASTER PROGRAMMER DECADES

The master programmer decades will be described with reference to the diagram for decade 11 on PX-8-304. Each master programmer decade consists of 6 decade switches each with an associated inverter (B41, 42, or 43), and a decade ring counter with a clear circuit (inverters 1* and B45 and gate B44), a carry over circuit (gate 28 and tubes 30), and an input circuit containing pulse standardizer 25-27 and buffer 31. Neons associated with stages 0 through 9 of the decade counters are shown on PX-8-303.

10.2.1. Decade Counter: Input and Carry Over Circuits

Decade counter D (where $1 \leq D \leq 20$) can be cycled by input to its decade direct input terminal, from the carry over circuit of decade D-1 (if there is a decade D-1 associated with it), or, in the case of units decade of a group associated with a stepper, from the stepper input circuit (see Section 10.3.1.) Pulse input to the decade direct input cycles the decade counter immediately, but there is a one addition time delay between the pulsing of the stepper input and the cycling of the decade counter which results (see Section 10.3.1.).

When a given decade counter is cycled to stage 9, gate 28 (in the case of decade 11) opens so that the next pulse delivered to the decade not only cycles the counter back to stage zero, but also passes through the gate and tubes 30 to be delivered to the next decade at the left if there is one. The time between successive digit pulses is not sufficient to allow safely for the carry over process. For this reason digit pulses should not be fed to the decade direct input terminal (also see Section 10.2.2.). Input to the decade derived from pulsing the stepper input terminal (see Section 10.3.) comes at the time of the CPP so that there is sufficient time for carry over.

*Tube 1 and the decade ring counter are mounted in a plug-in unit.

10.2.2. Decade Switches and Decade Counter Clear Circuits

Each decade switch is correlated with one of the 6 stages of the stepper counter associated with the decade. A decade switch in the top row is associated with stage 1; a switch in the bottom row, with stage 6.

The operator sets up on the decade switches corresponding to stage s of a stepper the number which the decades associated with the stepper must register for the stepper to advance from stage s to stage s+1 and for the decade counters to be cleared back to zero. For example, if decades 12 and 11 are associated with stepper E and if the switches in the second row from the top are set at 3 and 8 respectively, then stepper E will advance from stage 2 to 3 and the decades will clear back to zero when this pair of decades stores the number 38.

Each point on a decade switch is connected to the normally positive output of one of the stages of the decade counter. The negative signal from a stage in the abnormal state turns off the inverter associated with a switch set at the corresponding number. All inverters for the stage s decade switches are connected to the stage s stepper cycling gate (see Section 10.3.2.) of the associated stepper. When the stepper counter is in stage s, the stage s stepper cycling gate emits a signal provided that all the inverters for stage s switches of decades associated with the stepper are turned off.

The output of the stepper cycling gate is taken (through an inverter) to the gates numbered 44 (preceded by B, C, ..., or L) of the decades associated with the stepper. The CPP passed through these gates clears the decade counters associated with the stepper. The output of the stepper cycling gates also goes (through inverter 64) to gate 63 in the stepper. The CPP which is thus allowed to pass through gate 63 causes the stepper counter to cycle one stage at the

same time that the associated decades are being cleared. The necessity for providing sufficient time for gates 44 and 63 to set up before the arrival of the CPP they are to pass is a second reason for feeding only program pulses to the decade direct input terminals (also see Section 10.3.2.2.)

10.3. STEPPERS

Each of the 10 steppers (A-K) consists of a 6 stage stepper counter, a stepper-counter input, a stepper clear circuit, a stepper input (as distinguished from the stepper-counter input), and 6 outputs. For convenience, the elements of these circuits will be identified with reference to the drawing for stepper E.

The stepper input circuit consists of a stepper input terminal, an input flip-flop (66, 67) and input gate (69), buffers (65 and 70) and an inverter (68). Each of the 6 outputs consists of an output gate (61-69), a standard transmitter, and an output terminal.

The stepper-counter input circuit includes a pulse standardizer (21-23) an inverter (61) and buffer (62) and can be entered either through the stepper direct input terminal and buffer 61 or through the circuit containing the stepper cycling gates (B, C 48-50), inverter 64, and gate 63.

The stepper clear circuit contains an inverter (C46), the stepper clear direct input terminal and buffer B46, the stepper clear switch, inverter B46 and gate B47.

10.3.1. Stepper Input and Output Circuits

A program pulse received at the end of addition time t or a group of digit pulses received early (see below) in addition time t+1 by the stepper input terminal sets the input flip-flop. The normally negative output of this flip-flop then opens gate 69 so that a CPP passes through at the end of addition time

t+1. It is to be noted that if digit pulses are fed to the stepper input, they must be pulses which begin to be emitted before the 4P (i.e. no later than pulse time 6) in order to allow time for gate 69 to set up and pass the CPP which arrives at the end of the addition time. Since, in general, one does not know in advance the magnitude of a number, this restriction on the digit pulses which may be delivered to the stepper input is equivalent to saying that the only digit pulses which may be brought to a stepper are sign pulses since the 9P for sign begin to be emitted early enough in the addition time cycle.

The output of gate 69 has three effects:

1) It resets the input flip-flop*.
2) Passed through inverter 68, cathode follower 70, and buffer A43, it causes the associated group of decade counters to be cycled one stage in units place.
3) Passed through inverter 68 and cathode follower 70, it is delivered to the stepper output gates.

Each of the 6 output gates is controlled by the normally positive output (through an inverter) of a stage of the stepper counter. Thus the pulse from cathode follower 70 is passed through the gate and the transmitter corresponding to the stage in which the stepper counter is at the end of addition time t+1.

If, when the stepper counter is in stage s, the stepper input alone is pulsed, the output pulse is thus emitted from the terminal associated with stage s. It is, however, possible to pulse both the stepper input and stepper direct input

*Since this flip-flop is reset at the end of addition time t+1, a stepper input must not be pulsed in successive addition times. The same restriction is also pertinent to the use of program controls on other units.

terminal (see Section 10.3.2.1.) at the same time. If this is done, the output pulse is emitted from the terminal corresponding to the stage to which the stepper counter is cycled by the end of addition time t+1 as a result of the pulses delivered to the stepper direct input terminal.

10.3.2. Cycling a Stepper Counter

A stepper counter which has associated decades can be cycled either by pulses received at the stepper direct input terminal or as a result of the fact that the decades have counted to the number set on the decade switches corresponding to the stage in which the counter is. A stepper without decades (steppers A and F can be used in this way) can be cycled only by pulse input to the stepper direct input terminal.

10.3.2.1. Stepper Direct Input

A pulse received at a stepper direct input terminal is delivered through tubes 61 and 62 and the pulse standardizer to the stepper counter. Each pulse, whether program or digit, delivered to the stepper direct input causes the counter to be cycled one stage immediately. Notice, no output pulse is emitted when a stepper direct input is pulsed.

10.3.2.2. Stepper Cycling Gates

Each stepper cycling gate receives as one input, the normally positive output (through an inverter) of a stage of the stepper counter and as its second input, the outputs of the inverter tubes connected to s stage decade switches of all the decades associated with the stepper. These inverter tubes have their plates connected in parallel to a common load resistor. The circuit containing the inverters and stepper cycling gates is such that even if only one of the inverters connected to a switch is on, the gate remains closed. In this way, a stepper cycling gate, emits a signal only if, when the stepper counter is in

stage s, all the associated decade counters have reached the stages specified by their s stage decade switches.

The output of a stepper cycling gate causes a CPP to be passed through each of the gates 63 and 44 (preceded by B, C, ..., or L). The output of gate 63 causes the stepper counter to be cycled one stage, and the output of the gates 44 (preceded by B, C, ..., L) clears the associated decade counters.

Notice that the clearing of the decade counters and stepping of the stepper takes place one addition time after the decade counters arrive at the number specified by the decade switch settings whether the decades arrive at this number because of pulse input to the decade direct or stepper input terminal. Thus, if the stepper input is pulsed at the end of addition time t or early in addition time t+1 and the decade counters, as a result, reach the setting of the decade switches at the end of addition time t+1, the decade counter clears to zero and the stepper counter advances one stage at the end of addition time t+2. But, if the decade counters reach the switch settings as a result of pulsing the decade direct input at the end of addition time t, the stepping and clearing takes place at the end of addition time t+1.

10.3.3. Clearing a Stepper Counter

A stepper counter clears back to stage one as the result of pulse input to its clear direct input terminal or as the result of receiving a pulse when it is in stage c (the number set up on the stepper clear switch).

10.3.3.1. Stepper Clear Switch

Each point of the stepper clear switch is connected to the normally negative output of a stage of the stepper counter. If c is the setting of the stepper clear switch, then, when the stepper counter reaches stage c, the signal which passes through the clear switch opens gate B47. In this way, the next

TABLE 10-1

PROPERTIES OF MASTER PROGRAMMER INPUTS

t = addition time when terminal is pulsed unless otherwise noted.
s = stage of stepper counter before a pulse is received.
d_s = number set up on decade switches associated with stage s of stepper counter.
c = number set up on stepper clear switch

INPUT TERMINAL	PULSE INPUT	EFFECT OF RECEPTION OF A PULSE	ADDITION TIME EFFECT OCCURS
Stepper Input	Program pulse at end of add. time t or PM pulses during add. time t+1.	1. Output pulse is transmitted through output terminal corresponding to stage s of stepper counter.	t + 1
		2. Decade counters cycle 1 stage in units place	t + 1
		3. If input cycles decade counters to d_s	
		a. decade counters clear to zero	t + 2
		b. stepper counter cycles to (s+1) mod c	t + 2
Stepper Input A or F with decades dissociated	Program pulse at end of add. time t or PM pulses during add. time t+1.	1. Output pulse is transmitted through output terminal corresponding to stage s of stepper counter.	t + 1
		2. (No decade counters)	
		3. (No decade counters)	
Stepper Direct Input	Digit or program pulse	1. No output pulse is transmitted	
		2. Decade counters do not cycle	
		3. Stepper counter cycles 1 stage for each pulse received.	immediately
Stepper Direct Input A or F with decades dissociated	Digit or program pulse	1. No output pulse is transmitted	
		2. (No decade counters)	
		3. Stepper counter cycles 1 stage for each pulse received.	immediately
Stepper Input	Program pulse at end of add. time t	1. Output pulse is transmitted through output terminal associated with stage (s+p) of stepper counter.	t + 1
and Stepper Direct Input	Program pulse at end of add. time t or p digit pulses during add. time t+1.	2. Decade counters cycle 1 stage in units place.	t + 1
		3. Stepper counter cycles 1 stage for each pulse received at stepper direct input terminal.	immediately
		4. If decade counters are cycled to stage d_{s+p}	
		a. decade counters clear to zero	t + 2
		b. stepper counter cycles to (s+p+1) mod c.	t + 2
Stepper Input	Program pulse at end of add. time t	1. Output pulse is transmitted through stage (s+p) mod c.	t + 1
and Stepper Direct Input A or F with no decades	Program pulse at end of add. time t or p digit pulses during add. time t+1.	2. (No decade counter)	
		3. Stepper counter cycles 1 stage for each pulse received.	immediately
Decade Direct Input	Program pulse	1. No output pulse is transmitted	
		2. Decade counter cycles one stage	immediately
		3. If decade counters are cycled to stage d_s	
		a. decade counters clear to zero	t + 1
		b. stepper counter cycles to stage (s+1) mod c	t + 1
Stepper Clear Direct Input	Program pulse or digit pulses	1. Stepper counter clears to stage 1	immediately

pulse from buffer 62, whether derived from the stepper cycling gate circuit or from pulse input to the stepper direct input, is gated through B47 after passing through inverter B46. The output of gate B47 inverted by C46 clears the stepper counter back to stage 1.

The circuit containing the stepper clear switch and gate B47 requires more time than that between successive digit pulses if it is to operate reliably. For this reason, if digit pulses are ever brought to a stepper direct input terminal, the stepper clear switch must be set at 6. With the stepper clear switch set at 6, clearing to stage one results from the fact that the stepper counters are ring counters.

10.3.3.2. Stepper Clear Direct Input

Pulse input to the stepper clear direct input terminal passes through buffer B46 and inverter C46 and immediately clears the stepper.

If another pulse attempts to cycle the stepper at the same time that the stepper clear direct input is pulsed, the clearing action will predominate because the clear circuit spreads its signal out in time sufficiently for this purpose.

10.4. PROGRAMMING THE MASTER PROGRAMMER

One aspect of master programmer control is provided by the switch settings (decade associator, decade, and stepper clear). The other aspect is the input terminal (decade direct, stepper, stepper direct, or stepper clear direct) which is pulsed. Table 10-1 summarizes the properties of the master programmer inputs.

It is to be noted that in the master programmer, each stepper with its associated decades functions as a unit independently of the other steppers

and decades. For this reason, it is possible to stimulate some or all of them simultaneously.

It is even permissible to pulse more than one of the input terminals of a given stepper-decade combination simultaneously. For example, a decade direct input terminal and a stepper input terminal may be pulsed simultaneously because the cycling of the decade counters due to the former is completed before that due to the latter begins. A stepper input and stepper direct input terminal may also be pulsed simultaneously because the latter affects only the stepper counter and does so immediately while the former affects the decade and, if it affects the stepper counter, does so two addition times after the input. On the other hand, the stepper direct input should not be pulsed two addition times after the stepper input or one addition time after a decade direct input because of the conflict that would arise if the decade counters were thus cycled to the settings of the decade switches.

10.5. USES OF THE MASTER PROGRAMMER

The program controls of the master programmer make this unit suitable for link or digit program control of sequences or chains, for accumulating values of an independent variable (or even serial numbers), and for extending the program control facilities of other units.

10.5.1. Link Program Control

The master programmer's contribution to the link programming of sequences, sequences iterated into a chain, chains of chains and various other program hierarchies is the program output pulses which can be transmitted through any of its 60 output terminals.

10.5.1.1. The stimulation of sequences

The operator can provide for the stimulation of any given sequence by connecting the input terminals of the first program controls used in the sequence to the same program line that one or more program output terminals of the master programmer are connected. To stimulate that particular sequence, then, a pulse must be delivered to a stepper input at a time when the stepper counter will be in the stage associated with one of the master programmer output terminals mentioned in the previous sentence. Control of the stage of the stepper counter may be exercised through the settings of the decade switches or by pulsing the stepper direct input or stepper clear direct input. The pulse which must be delivered to the stepper input terminal in order to obtain a program output pulse may be derived from the program output terminal of one of the transceivers used in the last program of the sequence (see problem 1, Section 10.6.) or, in more complex problems, may even be obtained from another master programmer output terminal (see problem 2, Section 10.6.)

10.5.1.2. Iteration of the sequences of a chain

To secure the iteration of the sequence of a chain n times the master programmer must be set up to transmit a program output pulse through an output terminal which feeds to the initial programs of the sequence n times and then to transmit a pulse through an output terminal which does not feed to that sequence. This can be accomplished by setting at n the decade switches associated with the stepper output terminal which feeds to the first programs of the sequence and by delivering to the stepper input the terminal pulse of the sequence. A pulse to initiate the chain must be delivered to this stepper input. Then on each of n successive occasions whenever the stepper input receives a pulse, a pulse will be transmitted to stimulate the sequence. The nth pulse delivered

to this stepper input will, moreover, clear the decade counters to zero and cycle the stepper counter 1 stage so that the delivery of another pulse to the stepper input will result in the transmission of an output pulse through a terminal other than the one which, above, was described as being connected to the first program controls of the sequence.

10.5.1.3. The stimulation of program hierarchies

In general one stage of a stepper counter must be devoted to the stimulation of a single sequence or to the stimulation of a chain of iterated sequences. To link together a number of different sequences (where some or all of the sequences may be chains) requires the use of a stepper with one stage of the stepper counter devoted to each sequence or chain. A number of sequences, each consisting of several subsequences of the kind referred to in the previous sentence, requires the use of one stepper for the main sequences and one stepper for each of the subsequences.

A stepper must have associated with it by means of a decade associator switch sufficient decades to count the maximum number of iterations involved in any chains controlled by that stepper. If for any reason, there are not sufficient decades for this purpose, the decade switches correlated with several successive stages of a stepper may be set so that the sum of the decade switch settings is the required number and the corresponding outputs hooked together to the same program line.

The clear switch of the stepper must be set to the number of sequences (or sequences of chains) to be controlled by the stepper. If the number of sequences to be linked exceeds 6, several steppers may be used sequentially.

10.5.2. Digit Program Control

If it is desired to use two or three function tables to list the values

of a single function instead of merely one, digit control of the program of looking up a function is needed so that the table appropriate to the value of the independent variable may be entered. This control can be supplied very easily by using the master programmer.

For illustrative purposes, let us say that three function tables are to be used (the case in which only two are used may be treated similarly except for minor details). Then a transformation of the independent variable will be made which will cause its values to lie between zero and 299 inclusive. The program P_i (for $i = 1, 2, 3$) is defined as the program of entering function table i for a tabular value. The problem, then, is to stimulate the performance of P_i if the digit in hundreds place of the independent variable is $i - 1$.

The operator must connect three successive program output terminals of a stepper to three program lines which are in turn connected, one each, to the program input terminals on function tables 1, 2, and 3 respectively and must provide for the pulsing of the stepper direct input by digit pulses from the hundreds decade line of the accumulator storing the independent variable. The digit pulses may be those transmitted out of the accumulator's add or subtract output. Which stepper output terminals are made to correspond to programs P_1, P_2, and P_3 respectively depends on whether digit pulses from the add or subtract output terminal are used. The stepper input must also be pulsed (either at the end of the addition time just before the stepper direct input receives the digit pulses or some time subsequent to that) so that an output pulse will be transmitted by the stepper through the output terminal associated with the stage to which the stepper has been cycled by the digit pulses. And finally, the stepper clear direct input should be pulsed after the digit discrimination has been completed so that the stepper will be ready for use in the next digit dis-

crimination program when needed.

A conceivable motive for pulsing the stepper direct input with digit pulses from the subtract output might be avoidance of tying up the accumulator's add output. If digit pulses from the subtract output are used, 9, 8, or 7 pulses will be received at the master programmer's stepper direct input if the hundreds place digit of the argument is respectively 0, 1, or 2. Then the stepper output terminals corresponding to stages 4, 3, and 2 (with the stepper clear switch set at 6) respectively of the stepper counter should be so connected as to deliver the stimulating program pulses for programs P_1, P_2, and P_3 respectively. If digit pulses from the add output terminal are used, then the stepper output terminals corresponding to stages 1, 2, and 3 respectively of the stepper counter should be so connected as to deliver the stimulating pulse for programs P_1, P_2, and P_3 respectively.

Steppers A or F with zero decades associated are especially suited to digit discrimination programs. Any other stepper, however, may be used. If a stepper with decades is employed, two alternative methods for setting the decade switches exist:

1) the decade switches corresponding to stage 1 of the stepper counter may be set at a number exceeding the number of times the digit discrimination program will occur;
2) the decade switches corresponding to the various stages of the stepper may all be set at 1.

Whether a stepper with or without decades is used, provision must be made for clearing the stepper counter back to stage one sometime before the next digit discrimination program occurs. This may be done by pulsing the stepper clear direct input. If the stepper input is pulsed in addition time t,

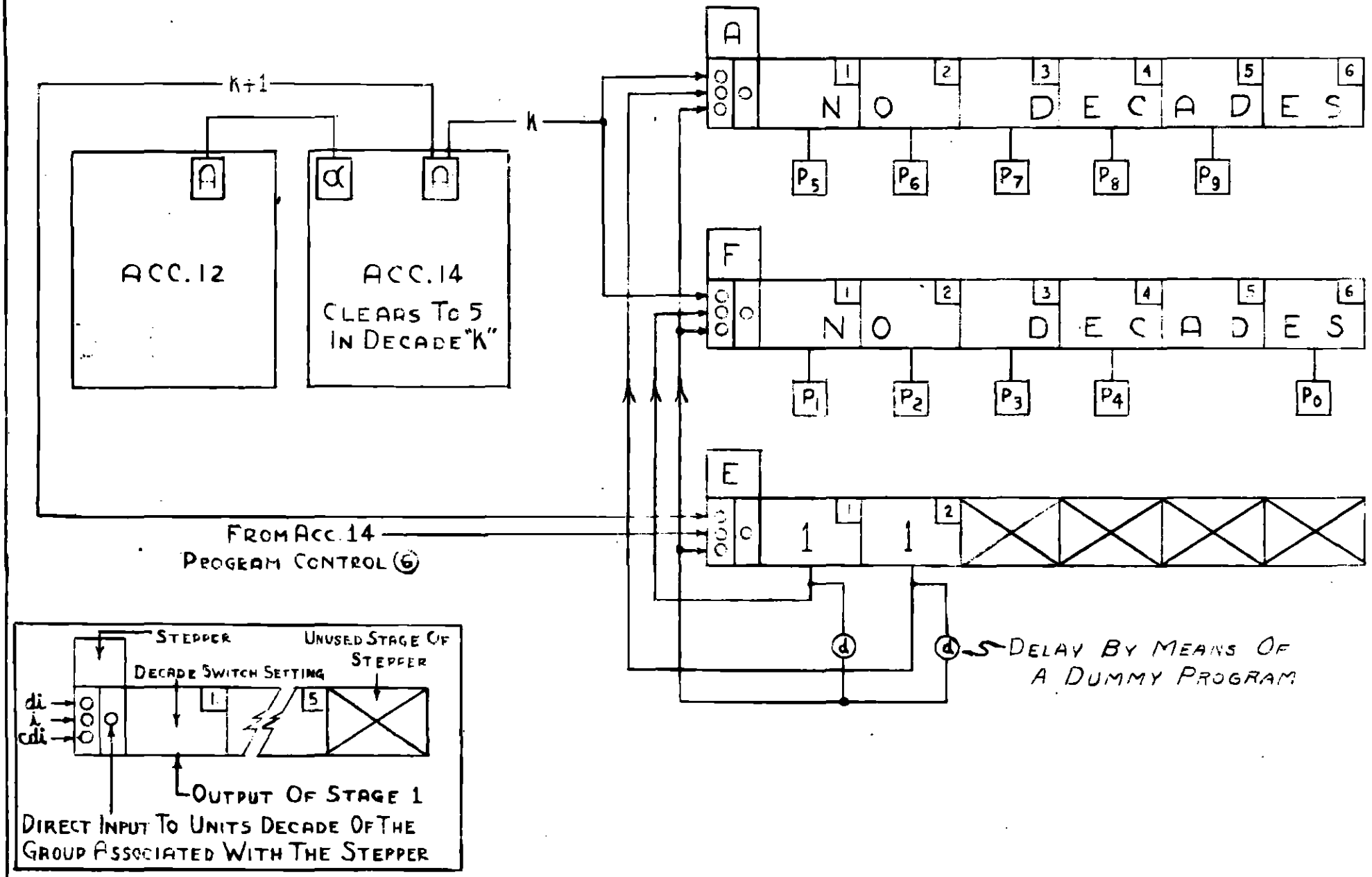
TABLE 10-2

SET-UP FOR STIMULATING PROGRAM P_i

(i=0, 1, ..., 9) if digit i appears in k^{th} decade of Accumulator 12

Unit Add. Time	Acc. 12	Acc. 14 (clears to 5 in decade k)	Master Programmer Master Input	Master Programmer Master Output
1	1-1 ① A 0 1	1-1 ⑤ α 0 1 1-2		
2		1-2 ⑥ A 0 1 [A(k+1) to 2-1] [A(k) to 2-2] 2-3	Edi 2-1 Adi 2-2 Fdi 2-2	
3			2-3 Ei	*{E_1^o 2-4 / E_2^o 2-5}
4	*{2-4 ⑤ / 2-5 ⑥} 0 0 2		*{2-4 Fi / 2-5 Ai}	F_1^o to P_1; F_2^o to $^2P_2$; F_3^o to $^3P_3$; F_4^o to $^4P_4$; F_6^o to $^6P_0$; A_1^o to P_5; A_2^o to P_6; A_3^o to $^3P_7$; A_4^o to $^4P_8$; A_5^o to P_9
5	↓ 2-6			
6			2-6 A, E, and F cdi	

*Braces are used here to mean "or".



USE OF MASTER PROGRAMMER TO STIMULATE P_i IF DIGIT i APPEARS IN DECADE K OF ACC. 12

FIG. 10-1

PX-8-102a

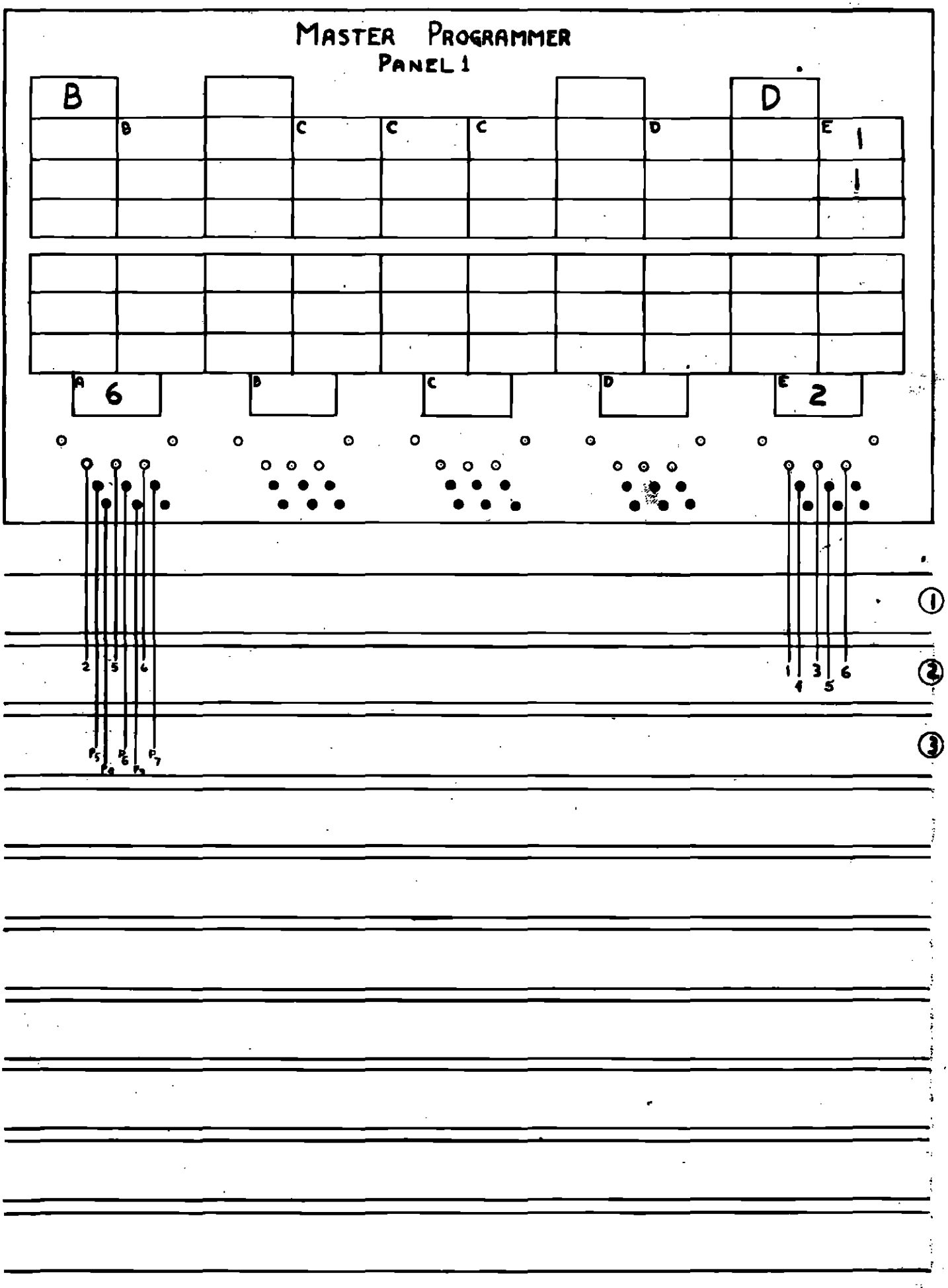


Fig. 10 – 2 (a)
Digit Discrimination Program
To stimulate P_i if digit i appears in decade k of accumulator 12.

PX-8 402 b

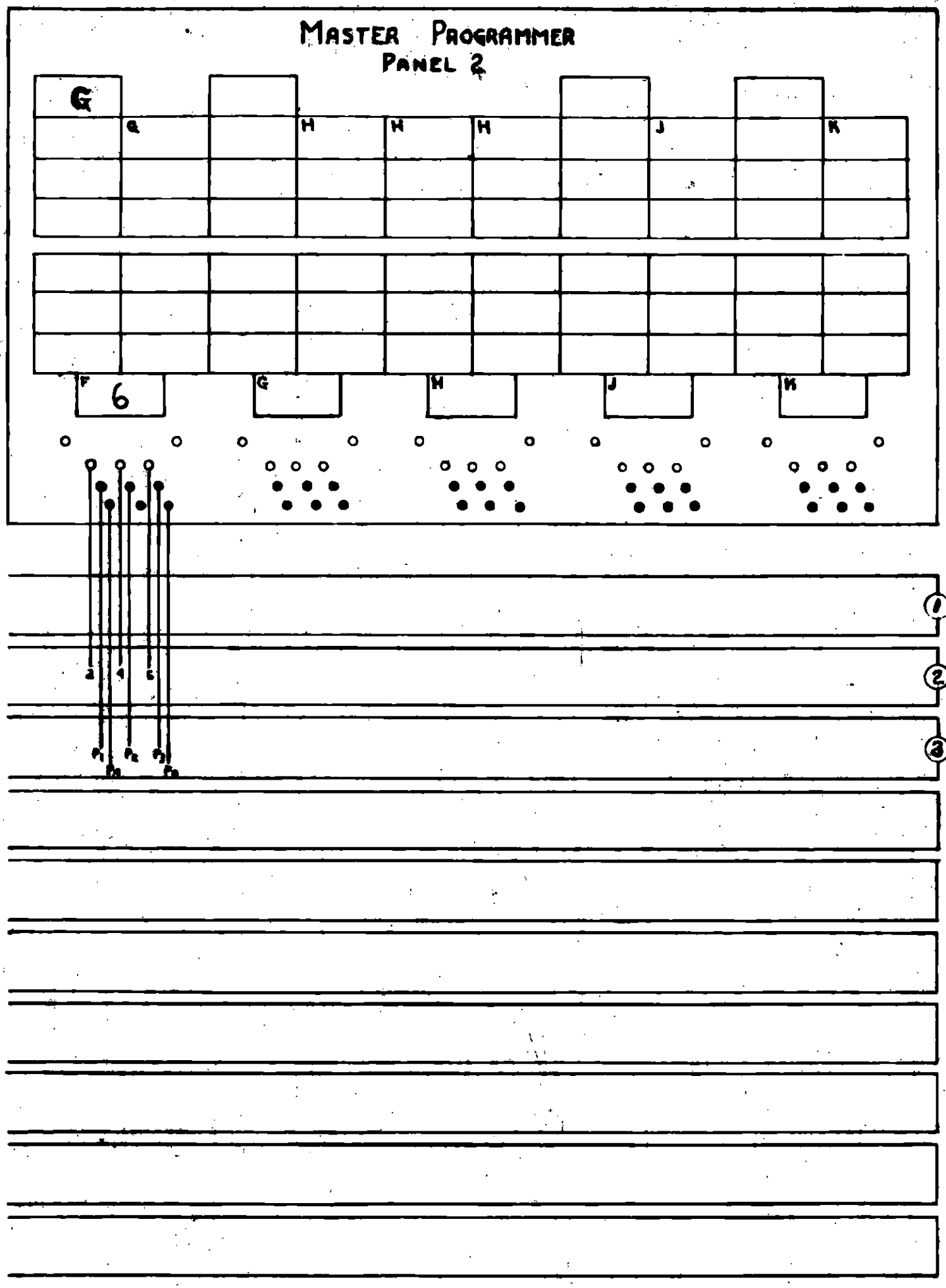


Fig. 20- 2 (b)

Digit Determination Program

To obtain the P_1 if digit 4 appears in thirds b of 100.12

PX-8-402c

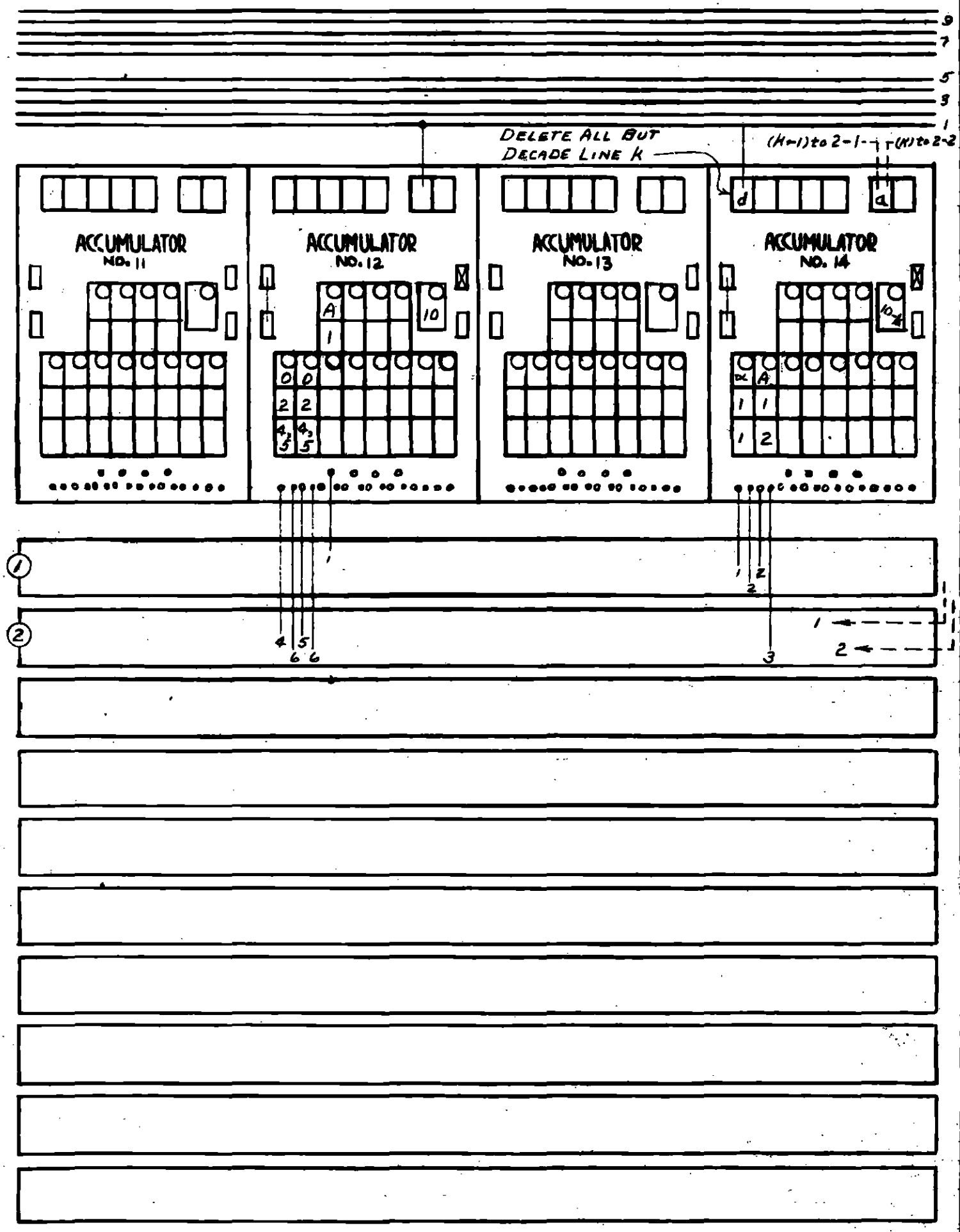


FIG. 10-2(c)

DIGIT DISCRIMINATION PROGRAM TO STIMULATE P_i
IF DIGIT i APPEARS IN DECADE k OF ACC. 12

the stepper clear direct input may be pulsed in addition time t+1 when a stepper without decades is used or when a stepper with decades whose stage one decade switches have been set at a number greater than the number of times digit discrimination occurs is used. This allows sufficient time for the stepper to emit a program output pulse from the output terminal corresponding to the particular stage to which the digit pulses cycled the stepper. If there are decades associated with the stepper used for digit discrimination and if the decade switches of the various stages used are set at 1, the stepper counter should not be cleared to stage 1 sooner than the end of addition time t+2 since, in addition time t+2, a pulse will try to cycle the stepper counter due to the fact that the decade counter has been cycled to stage 1.

A digit discrimination program where the possibilities are limited to 6 consecutive digits may be treated in a fashion similar to that described above except for obvious modifications. A digit discrimination program calling for the stimulation of P_i if digit i (where $o \leq i \leq 9$) appears in decade k requires more extensive modification.

This problem may be handled in two steps: 1) discriminate to determine whether the digit is between zero and four inclusive or between 5 and 9 inclusive; 2) using two different steppers for the two ranges mentioned above, discriminate among 5 consecutive digits.

Table 10-2 shows one possible method of carrying out this problem and Figure 10-1 presents a visual summary of this set-up. Figure 10-2 (a, b, and c) shows the program and digit connections and switch settings required to carry out this digit discrimination program. The notation for the master programmer in Table 10-2 and in Figure 10-2 is explained at the beginning of Section 10.6.

Step 1 of this digit discrimination program is handled by transmitting

the number stored in accumulator 12 to accumulator 14 where it is received through a special deleter which eliminates all of the decade lines except decade k. The significant figure switch on accumulator 14 is set to 10-k so that this accumulator clears to 5 in decade k. Now, if the digit stored in decade k of accumulator 12 does not exceed 4, decade k+1 of accumulator 14 will store zero; if the digit stored in decade k of accumulator 12 is between 5 and 9 inclusive, decade k+1 of accumulator 14 stores 1.

The next step of the program consists of transmitting the addition output of decade line k+1 from accumulator 14 to the direct input of stepper E and simultaneously the digit pulses of the output of decade line k to the direct inputs of steppers A and F. The program output pulse from the program control on accumulator 14 used for the previously mentioned program is delivered to the input terminal of stepper E. If the digit stored in decade k of accumulator 12 does not exceed 4, the output terminal corresponding to stage 1 of stepper E delivers a pulse to Fi. Stepper F, acting on the information which it received from the addition output of accumulator 14, then transmits an output pulse to stimulate program P_0, P_1, ..., or P_4. If the digit stored in decade k of accumulator 12 exceeds 4, the output terminal corresponding to stage 2 of stepper E delivers a pulse to A_i. Stepper A then emits a pulse to stimulate P_5, P_6, ..., or P_9.

The pulse output from the terminals corresponding to stages 1 and 2 of stepper E is also taken to a program control on accumulator 12 whose repeat switch is set at 2. The output pulse from this transceiver is used to clear steppers A, E, and F back to stage 1.

10.5.3. Accumulating Values of an Independent Variable

The master programmer is a convenient unit for accumulating, storing

and printing values of the independent variable. This may be done by delivering to a decade direct input, the number of pulses by which the value of the independent variable is to be increased at a given time or by pulsing a stepper input. In the latter case, the stepper input must be pulsed in several different addition times if the independent variable is to be increased by more than 1 unit at a time. At the present time, decades 14 through 18 inclusive, are connected to the printer. Therefore, it is desirable to choose from among these the decades to be used for the accumulation of the independent variable.

The decade switches associated with the stepper counter stage involved in accumulating the independent variable should be set to a number one higher than the maximum value of the independent variable to be counted so that the decade counters will not clear to zero before printing is accomplished (see Section 10.2.2.). After the last printing takes place, the decade counters may be cleared to zero by feeding one more pulse to either the decade direct input or to the stepper input after printing. In the event that the criterion for printing the final result is something other than a certain value of the independent variable (see Problem 2 of Section 10.6.), it may be necessary to include a program sequence designed to clear the decade counters.

10.5.4. Extending the Program Control Facilities of Other Units

Should the number of program controls on a particular unit prove inadequate for some computation, the master programmer may be employed so as to make possible the repeated use of program controls on that unit at various times in the set-up.

One way to accomplish this is to deliver the final pulse of the

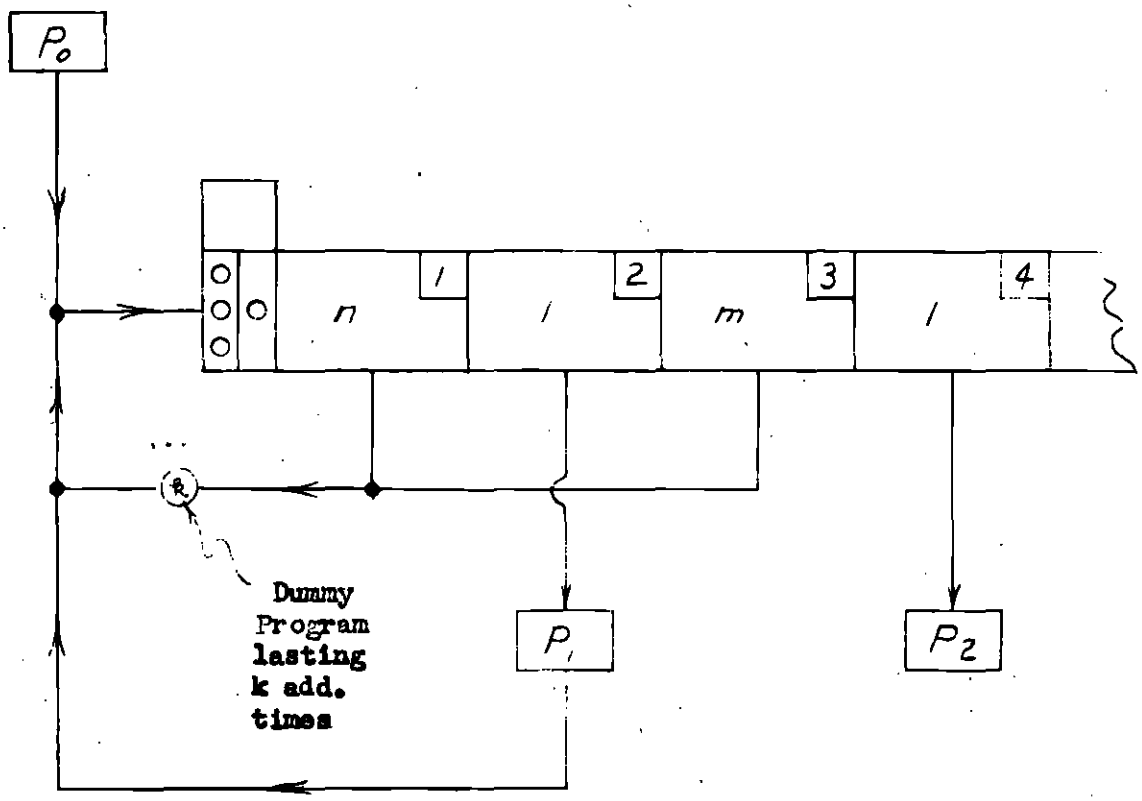
sequence which precedes the program set-up on a repeatedly used program control . to that control. Then the program output pulse of the program which is used repeatedly goes to the master programmer stepper which determines which sequence to stimulate subsequently.

Let us suppose, for example, that program control 26 on the constant transmitter is to be used twice in a computation, with programs P_0 and P_1 respectively preceding and following the first use of this constant transmitter control and with programs Q_0 and Q_1 respectively preceding and following the second use of the same constant transmitter control. By delivering the program output pulse of the controls on which programs P_0 and Q_0 are set up to the program pulse input terminal of control 26 on the constant transmitter, provision is made for stimulating this control on each occasion. If, however, the program output pulse of program control 26 must stimulate program P_1 once and the next time, program Q_1, this cannot be done directly. Instead, the output of program control 26 is taken to a master programmer stepper which determines whether to stimulate program P_1 or Q_1.

When high-speed multiplier or divider and square rooter program controls are used repeatedly in this way, the problem of stimulating the accumulators which store the arguments to transmit may arise. The function table or another master programmer stepper may be used to provide for this stimulation. The illustrative problem of Section 8.7. illustrates the repeated use of high-speed multiplier program control through the use of the master programmer (see Figure 8-2 with particular attention to the use of steppers D-K).

In Section 4.5.2. the use of dummy programs set up on accumulators for the delay of a program pulse was suggested and, in Section 7.4. the use

PX-8-4008



Program Sequence P_1 follows P_0 after a delay of $n(k+1)+1$ addition times

Program Sequence P_2 follows P_1 after a delay of $m(k+1)+1$ addition times

Fig. 10-3

USE OF MASTER PROGRAMMER TO DELAY A PROGRAM PULSE

of a function table program to achieve a longer delay than is possible with a single accumulator control was mentioned. An alternative method of delaying a program pulse, and one which is practicable for long delays, can be achieved through the use of the master programmer. This use of the master programmer is illustrated in Figure 10-3.

10.6. ILLUSTRATIVE PROBLEM SET-UPS

Two problems are offered in this section to illustrate the use of the master programmer in central programming. Problem 1 uses only link control to stimulate its sequences. Problem 2 is more complex involving both link and magnitude control and the use of the master programmer to accumulate the independent variable.

Both problems are described with reference to a set-up analysis table, a figure showing the master programmer links, and a set-up diagram. For problem 2, moreover, there is a set-up table.

In the set-up analysis tables a decimal notation is used to identify the program sequences and subsequences. The number separated from the sequence identification decimal by a dash indicates the number of times the sequence is to be iterated into a chain. For example, the symbols

2-6
2.1 - 10 integrate
2.2 - 1 print

are used to mean that sequence 2, which consists of a subsequence, 2.1, to be iterated into a chain by its successive performance 10 times and another subsequence, 2.2, to be performed only once, is itself to be iterated 6 times.

In set-up tables, (see Table 10-5) instructions for the master

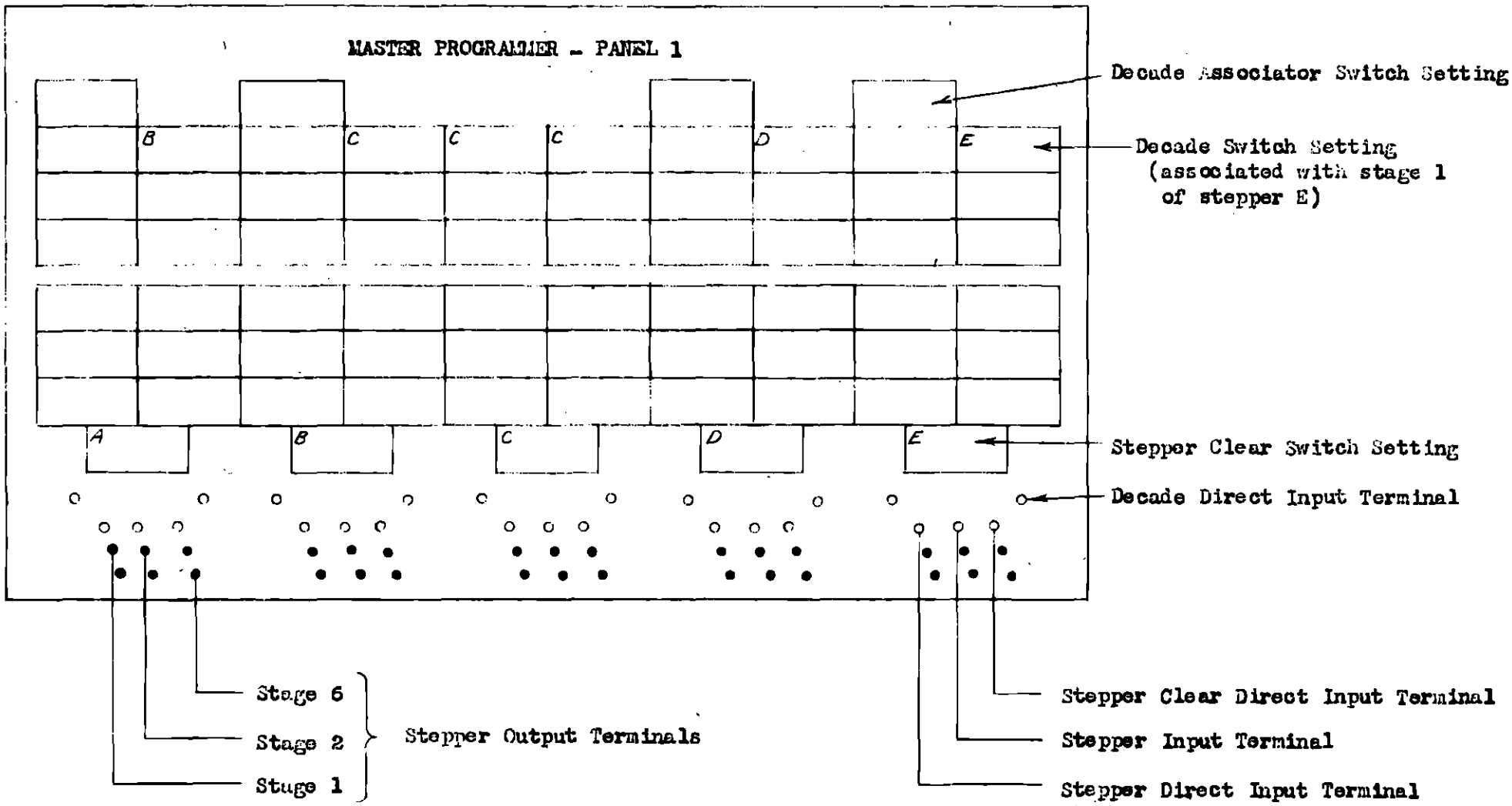
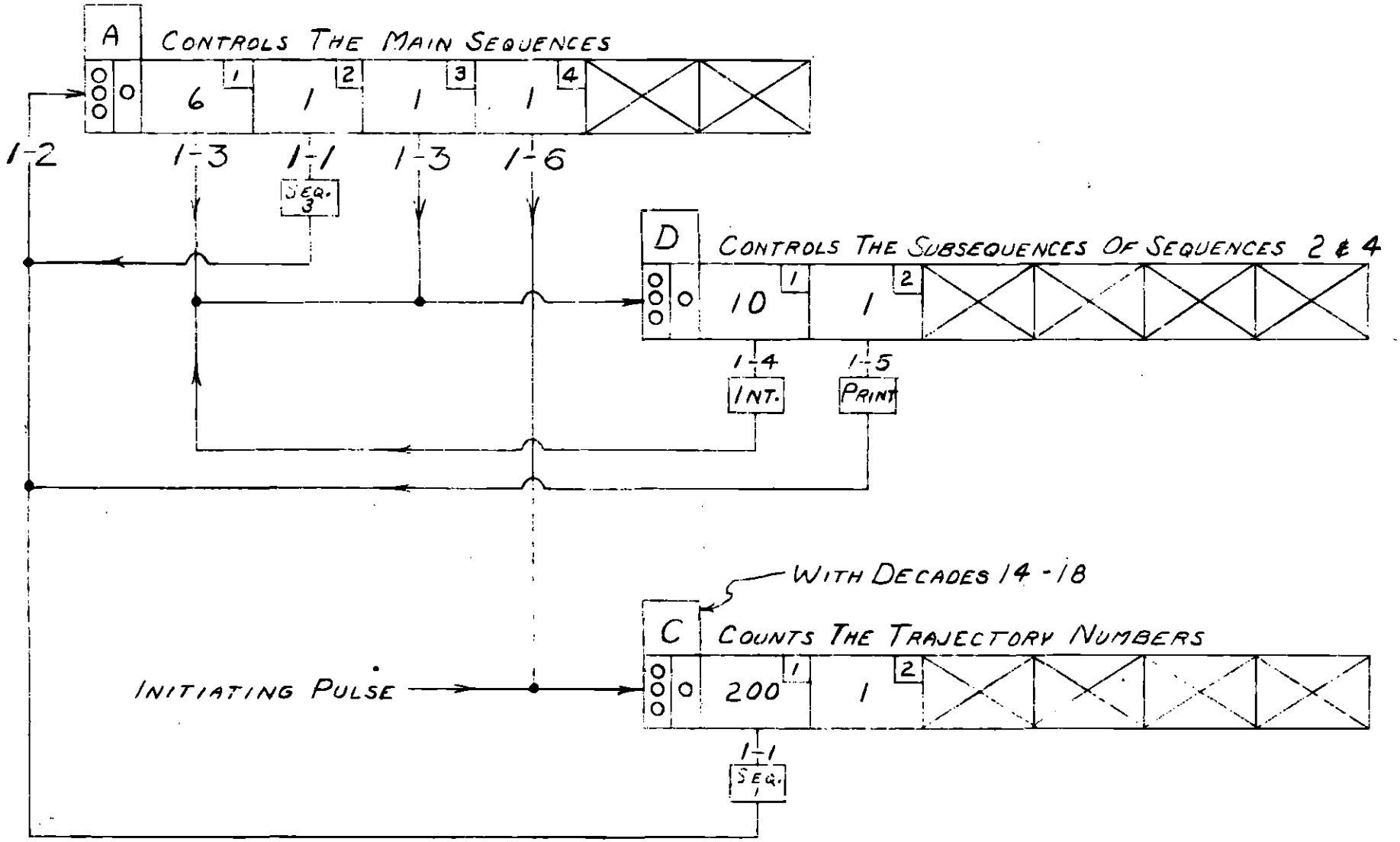


Fig. 10-4

MASTER PROGRAMMER SET-UP DIAGRAM CONVENTIONS



MASTER PROGRAMMER LINKS — PROBLEM 1

FIG. 10 - 5

programmer are given in a double column. The input terminal and program line from which it receives a pulse appear in the left hand half of the column. The program line designation appears above or below the symbol for the input terminal according as the line carries a program pulse or digit pulses. The output terminal through which a program output pulse (if any) is transmitted and the program line to which the output pulse is delivered appear in the right hand half of the column.

The set-up diagram conventions for the master programmer are shown in Figure 10-4.

The master programmer link diagrams are essentially block diagrams designed to summarize the way in which the various program sequences of a problem are tied together by the master programmer. The conventions used in these diagrams appear at the lower left of Figure 10-1. On these diagrams, we have used two different symbols for dummy programs, namely —•— and ⓓ. This is done to distinguish between the purposes for which the dummy programs are used. A dummy program used to isolate program pulses is symbolized by —•—; one used to achieve a delay of d addition times by ⓓ.

10.6.1. Problem 1

Problem 1 suggests a possible method of setting up the ENIAC to compute the trajectories needed to make an anti-aircraft table. The number of trajectories to be computed has arbitrarily been taken as 200. The number of integration steps performed before printing has also been arbitrarily taken as 10, and it is assumed here that 60 integration steps will adequately cover the required range. Obviously, numbers other than these could be chosen at the operator's discretion and convenience. Sequences 3 and 4 (see Table 10-3 and Figure 10-5) together constitute a test run.

TABLE 10-3

SET-UP ANALYSIS -- PROBLEM 1

1-1 Selective clear
Read
Transmit from Constant Transmitter to Accumulators

2-6
2.1 - 10 integrate

2.2 - 1 print

3-1
Selective clear
Read
Transmit from Constant Transmitter to Accumulators

4-1
4.1 - 10 integrate

4.2 - 1 print

PX-8-404

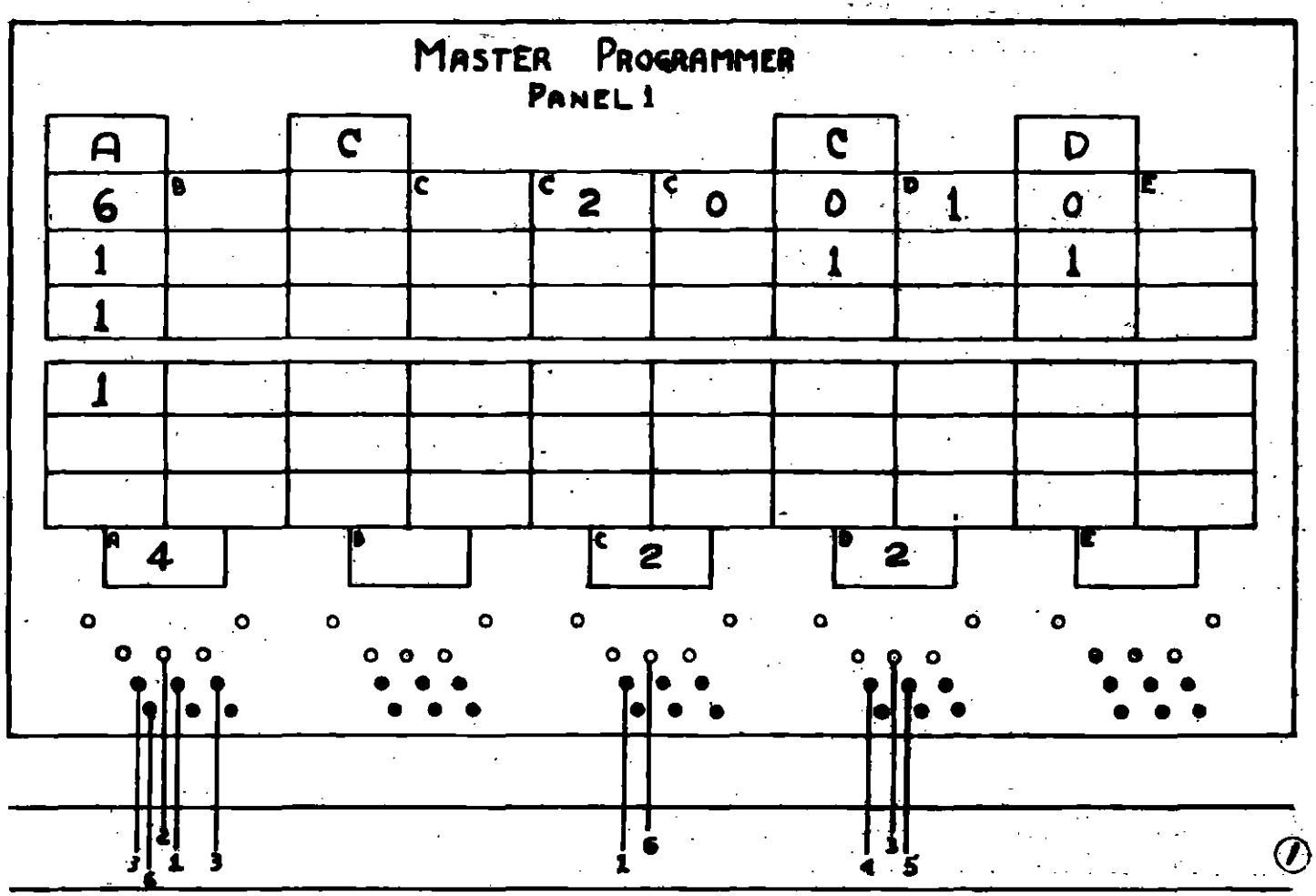


Fig. 10 - 6
Set-Up Diagram - Problem 1

In sequence 3, this set-up assumes that the initial conditions for the test run will be read from an IBM card different from the one which held the initial conditions for the previous trajectory. This is not meant to indicate that such a procedure is the only possible one. Depending on the amount of information to be put on the IBM cards or to be set up on the constant set switches of the constant transmitter, the initial conditions of the test run could be put on the same IBM card as those for the previous trajectory or set-up manually on the constant transmitter.

Stepper C (with decades 14-18 associated) is used to count the number of trajectories (see Section 9.4.). After 200 trajectories have been computed further computation sequences will not be initiated. As stepper C is set up here, the 200th card will be punched with serial number zero.

Four stages of stepper counter A are used to advance the computation through its four main sequences. Stage 1 of stepper counter D is devoted to the chain of 10 integrations (2.1-10 and 4.1-10) and stage 2 to the printing sequence (2.2-1 and 4.2-1).

10.6.2. Problem 2

This problem set-up again involves the sequential computation of a number of trajectories. Here, however, the set-up is one that would be suitable for ground gunfire trajectories. Results are printed not after a constant number of integration sequences (and thus, at even intervals of time if time is the independent variable) but, instead, only in the neighborhood of the summit and ground. This is accomplished by following each integration sequence with a test to determine the magnitude of y' or y. When the projectile goes below ground, computations cease, a test run is performed, and then the next trajectory is initiated.

TABLE 10-4

SET-UP ANALYSIS — PROBLEM 2

1-1 Initial Sequence
Read IBM card and selective clear
Transmit initial conditions from constant transmitter to accumulators.

2- Until $y+c_2 < 0$ (see Seq. 2.5) below.

2.1-1 Integrate

2.2- Repeat as long as $y'-c_1 \geq 0$

Test $y'-c_1$ and then integrate

2.3- Repeat as long as $y'+c_1 \geq 0$

Test $y'+c_1$, print, and then integrate

2.4- Repeat as long as $y - c_2 \geq 0$

Test $y - c_2$ and then integrate

2.5- Repeat as long as $y + c_2 \geq 0$

Test $y + c_2$, print, and then integrate

3-1 Print

4-1 Clear the decades of the master programmer which have been accumulating the independent variable and clear all other steppers which require clearing in preparation for the next trajectory computation.

5-1 Test run

5.1-1 Transfer initial conditions from constant transmitter to accumulators*

5.2-10 Integrate

5.3-1 Print

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*It is assumed here that the initial conditions for the test run are set up on the constant set switches of the constant transmitter or read from the IBM card for the previous trajectory so that a new card need not be read for the test run's initial conditions.

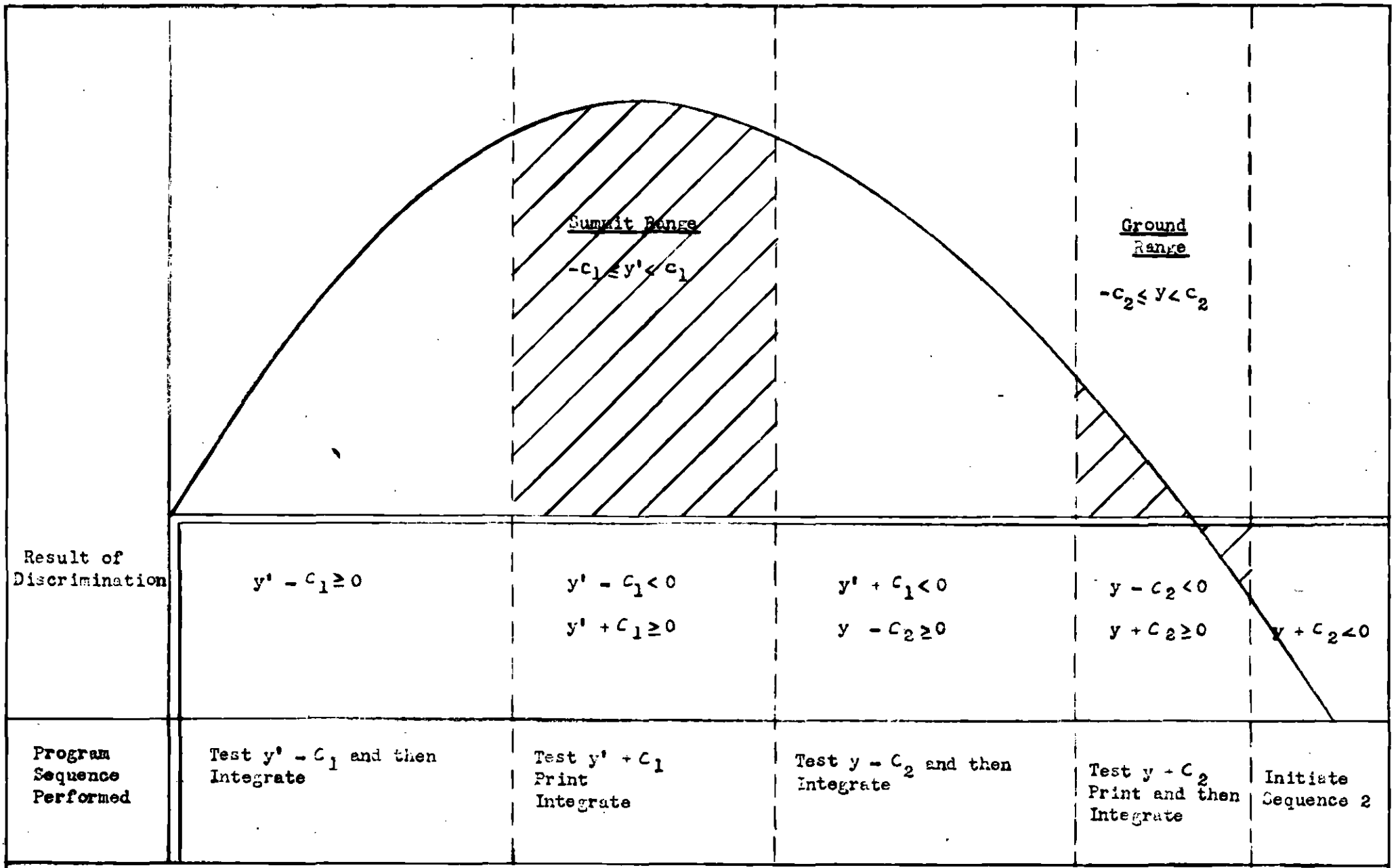


FIGURE 10-7

SUBSEQUENCES OF SEQ. 2 - PROBLEM 2

The sequences of this problem are defined in table 10-4. Sequences 1 through 3 cover the computations for a trajectory. The breakdown of sequence 2 into its component subsequences is shown pictorially in Figure 10-7.

It is assumed in this set-up that the value of the independent variable is stored in and printed from decades 14-18 (associated with stepper C) of the master programmer. Computation, for a given trajectory, ceases, not at a fixed value of the independent variable, but when the projectile has gone past ground range (see Figure 10-7). This means that the decade switches associated with stage 1 of stepper counter C must be set at a number safely in excess of the highest value of the independent variable that can be expected in any of the trajectory computations. (For the problem under discussion, we will arbitrarily take this number to be 80.0 with tenths place registered in master programmer decade 14). Furthermore, we cannot depend on clearing decades 14-18 as a result of arriving at the setting of the decade switches associated with stage 1 of stepper C. For this reason, sequence 4 is included in the set-up. The details for carrying out this sequence will be explained in section 10.6.2.2.

Sequence 5 constitutes a test run. The plan of the problem calls for a test run after each trajectory has been completed.

The master programmer links for this problem are shown in Figure 10-8. Steppers A, C, D, E, and F are used.

Stepper A controls the main sequences of the computation with the output of stage i stimulating sequence i+1. Stepper C records the value of the independent variable and steppers C and D have been so interrelated as to make possible the clearing of decades 14-18 after the projectile goes below ground. The same integration sequence is performed as a subsequence of both sequence 2 and sequence 5.* Stepper E is used to choose the routine to be performed after

* On sequence 2, however, the integration sequence is accompanied by programs concerned with accumulating the independent variable. In Sequence 5, we do not record the independent variable.

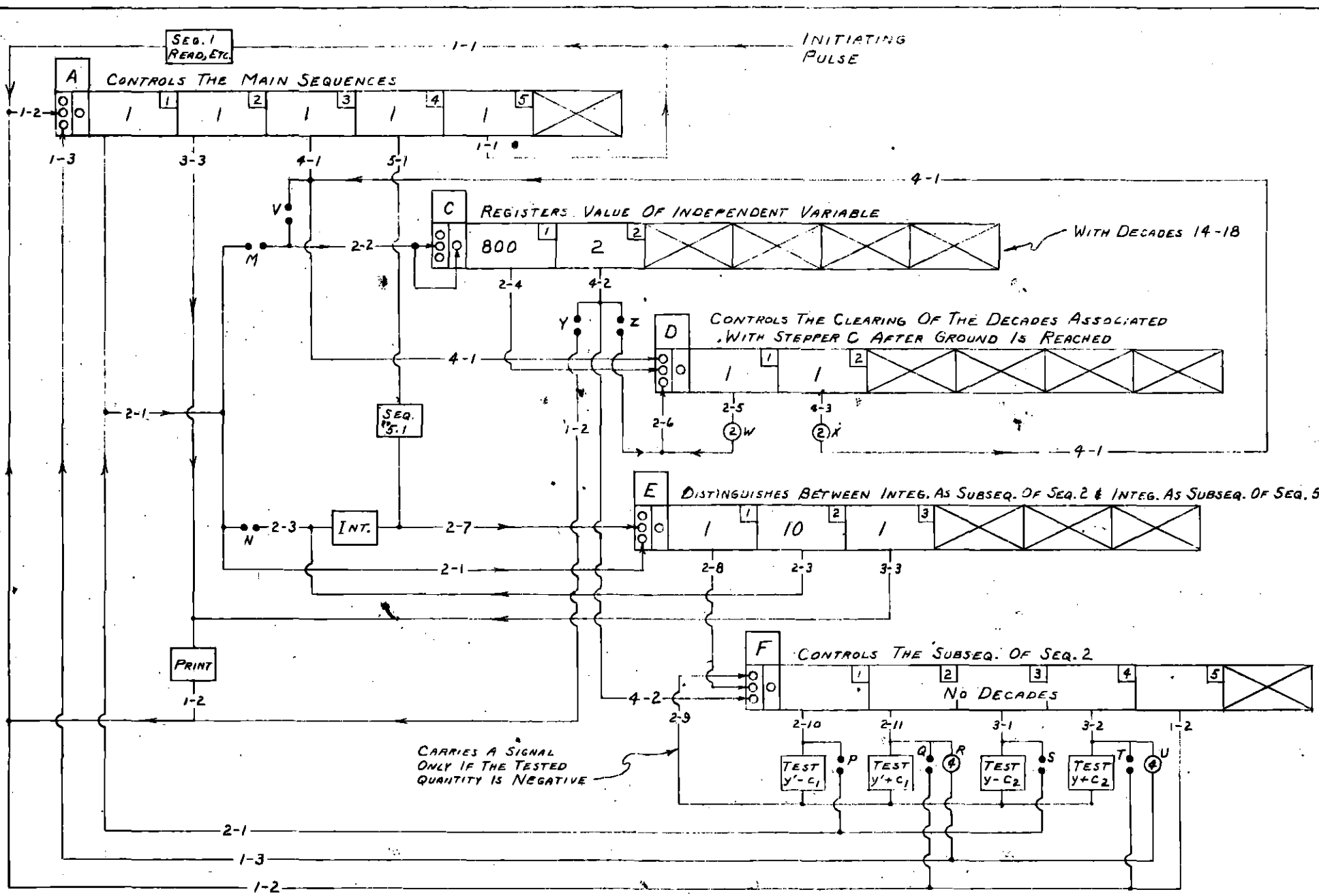


FIG. 10-8
MASTER PROGRAMMER LINKS—PROBLEM 2

1 1-17-46
2 4-2-46
3 4-15-46

PX-8-406

integration, with stage 1 motivating the routine in sequence 2, and either stage 3 or 4, the routine in sequence 5. Stage one of stepper E routes control to stepper F. This stepper participates in sequence 2, determining which of the subsequences of sequence 2 is to be performed at any given time.

10.6.2.1. Sequences 1, 2, and 3.

The initiating pulse, at the very beginning of a computation, and thereafter, the output of stage 5 of stepper A stimulates the performance of sequence 1 and thus initiates the computations for a trajectory and its test run.

The final pulse of sequence 1, pulse 1-2, goes to stepper A. Pulse 2-1, delivered by $A_1 0$, stimulates the performance of sequence 2.1 (integration) and also causes the value of the independent variable to be increased. It is assumed here that the increment to the independent variable is 0.2 (see Section 10.6.2.2.). Pulse 2-1, thru dummy program M goes to the direct input of decade 14 and to Ci to produce the required increment. Dummy program M is used to isolate the pulse which goes to Ci and to 14 di from the pulse which stimulates the integration sequence since, in sequence 4, we shall desire to stimulate Ci and 14 di without stimulating the other programs initiated by pulse 2-1 (also see Section 10.6.2.2.). Dummy program N intervenes between 2-1 and the pulse which stimulates the integration sequence, pulse 2-3, since, in sequence 5, it is necessary to stimulate the integration sequence without stimulating the associated programs of sequence 2. Pulse 2-1 is also taken to E cdi to return stepper E to stage 1 as long as sequence 2 is performed.

The terminal pulse of the integration sequence, pulse 2-7, goes to Ei and the output of $E_1 0$ stimulates Fi. Before the summit range, stepper F is in stage 1 so that pulse 2-10 is emitted. This pulse stimulates the performance of

the test on $y'-c_1$ (see Section 10.6.2.4. for details of the tests in sequences 2.2-2.5) and through dummy program P, brings the computation back to 2-1 which initiates the programs discussed in the previous paragraph. Dummy program P isolates the integration sequence from the test of $y'-c_1$ so that later (as in sequence 2.4) the integration maybe performed with a different test. As long as $y'-c_1$ remains non-negative stepper F remains in stage 1. When $y'-c_1$ is negative for the first time, the test on this quantity yields pulse 2-9 which advances stepper F to stage 2. While the test on $y'-c_1$ goes on, the pulse emitted by dummy program P, initiates the integration sequence.

When the integration sequence is completed, pulse 2-7 is emitted, and then pulse 2-8. This time, stepper F is in stage 2 so that pulse 2-11 is emitted by stepper F. Pulse 2-11 stimulates the test on $y'+c_1$ and, through dummy program Q, causes the emission of pulse 1-2. Since pulse 1-2, given out as the terminal pulse of sequence 1, advances stepper A to stage 2, this time, pulse 1-2 causes stepper A to emit pulse 3-3 (and advance to stage 3). This pulse stimulates printing. Pulse 2-11 is also taken to dummy program R for a delay of 4 addition times. Dummy program R emits pulse 1-3 which clears stepper A back from stage 3 to stage 1 so that when the printing is completed with the emission of pulse 1-2, stepper A again emits pulse 2-1 (and advances to stage 2). Pulse 2-1 stimulates the performance of the integration sequence and associated programs. Sequence 2.3 is then repeated until $y'+c_1$ becomes negative. At that time stepper F advances to stage 3. Whenever integration is completed in this phase of sequence 2, pulse 3-1 is given out. This pulse stimulates the test on $y-c_2$ and, through dummy program S, stimulates the integration sequence as was described above for sequence 2.2.

When $y-c_2$ becomes negative, stepper F is advanced to stage 4. In this part of sequence 2, pulse 3-2 stimulates the test of $y+c_2$ and, through dummy programs T and U, stimulates printing and then integration as described above for sequence 2.3.

When $y+c_2$ is negative for the first time pulse 2-9 is given out so that stepper F advances to stage 5.

Thus, when the integration initiated after the test which yields $y+c_2 < 0$ has been completed, pulse 1-2 is emitted by $F_5 0$.

Pulse 1-2 finds stepper A in stage 2 so that pulse 3-3 is given out and printing is stimulated. This completes sequence 3.

We note that at the end of sequence 3 the following state of affairs exists in the master programmer:

Stepper	Stage of Stepper	Stage of associated decades
A	3	0
C	1	d $\leq$ 800
D	1	0 (see Section 10.6.2.2.)
E	2	0
F	5	no decades.

10.6.2.2. Clearing the Decades which Store the Independent Variable: - Sequence 4

In the course of sequence 2, we have been increasing the value of the independent variable by 2 in decade 14 with every repetition of the integration sequence. Pulse 2-2, taken to the decade direct input, accounts for an increase of 1 unit and, taken to Ci, accounts for an increase of one more unit. Pulse 2-2 also causes pulse 2-4 to be emitted. This pulse goes to Di causing stepper D to advance to stage 2 and pulse 2-5 to be emitted. This pulse, delayed for two addition times by dummy program W, restores stepper D to stage 1 as long as

sequence 2 is in progress.

At the end of sequence 3 (the last printing for a trajectory), pulse 1-2 is delivered to Ai. Pulse 4-1 is then given out by A_3O and stepper A advances to stage 4.

Pulse 4-1 advances stepper D to stage 2 and, through dummy program V, goes to both Ci and 14 di. Since we assumed that the settings of the decade switches associated with stage 1 of stepper C safely exceeded the maximum value of the independent variable, stepper C is found in stage 1 at this time. Thus 2-4 is given out to stimulate Di and, because 4-1 advanced stepper D to stage 2, pulse 4-3 is emitted. One addition time after pulse 4-3 is given out stepper D cycles back to stage 1. However, pulse 4-3, delayed for two addition times by dummy program X, yields 4-1. Pulse 4-1 then causes the repetition of the programs described at the beginning of this paragraph.

Now, let us assume that the last printing for a trajectory takes place when the independent variable has the value 10^{-1} (800 -2m). Then, the output of A_3O causes the decades of stepper C to register 800 -2 (m-1) and, finally, causes dummy program X to emit a pulse for the 1st time. This, in turn causes the decades of stepper C to advance to 800-2(m-2) and causes dummy program X to emit pulse 4-1 for the 2nd time etc. The (m-1) st pulse emitted by dummy program X causes decades 14-18 to reach 800 and also causes the emission of 2-4 which results, finally, in the emission of pulse 4-1 by dummy program X for the m^{th} time. Stepper C advances to stage 2 and its decades clear to zero before the m^{th} pulse from dummy program X causes Ci to be pulsed again. Therefore, this time pulse 4-1 causes pulse 4-2 to be emitted from C_2O. Pulse 4-2 goes to F cdi to restore this stepper to stage 1. Since the m^{th} pulse emitted by dummy program X steps D to stage 2, it is necessary also to clear stepper D in preparation for the

PX-8-407a

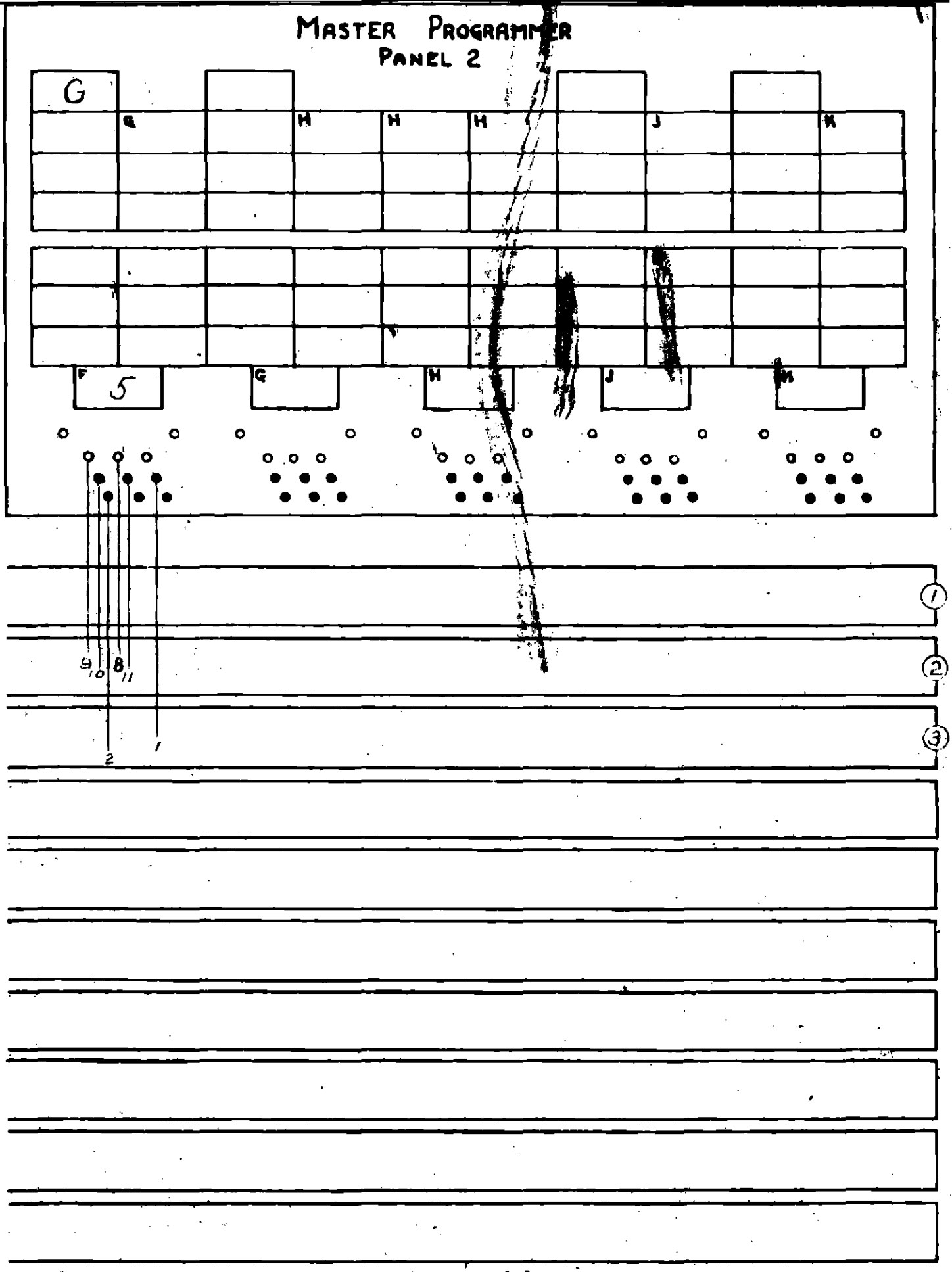


Fig. 10-9 (a)

Set Up Diagram For Tests on y and y' - Problem 2

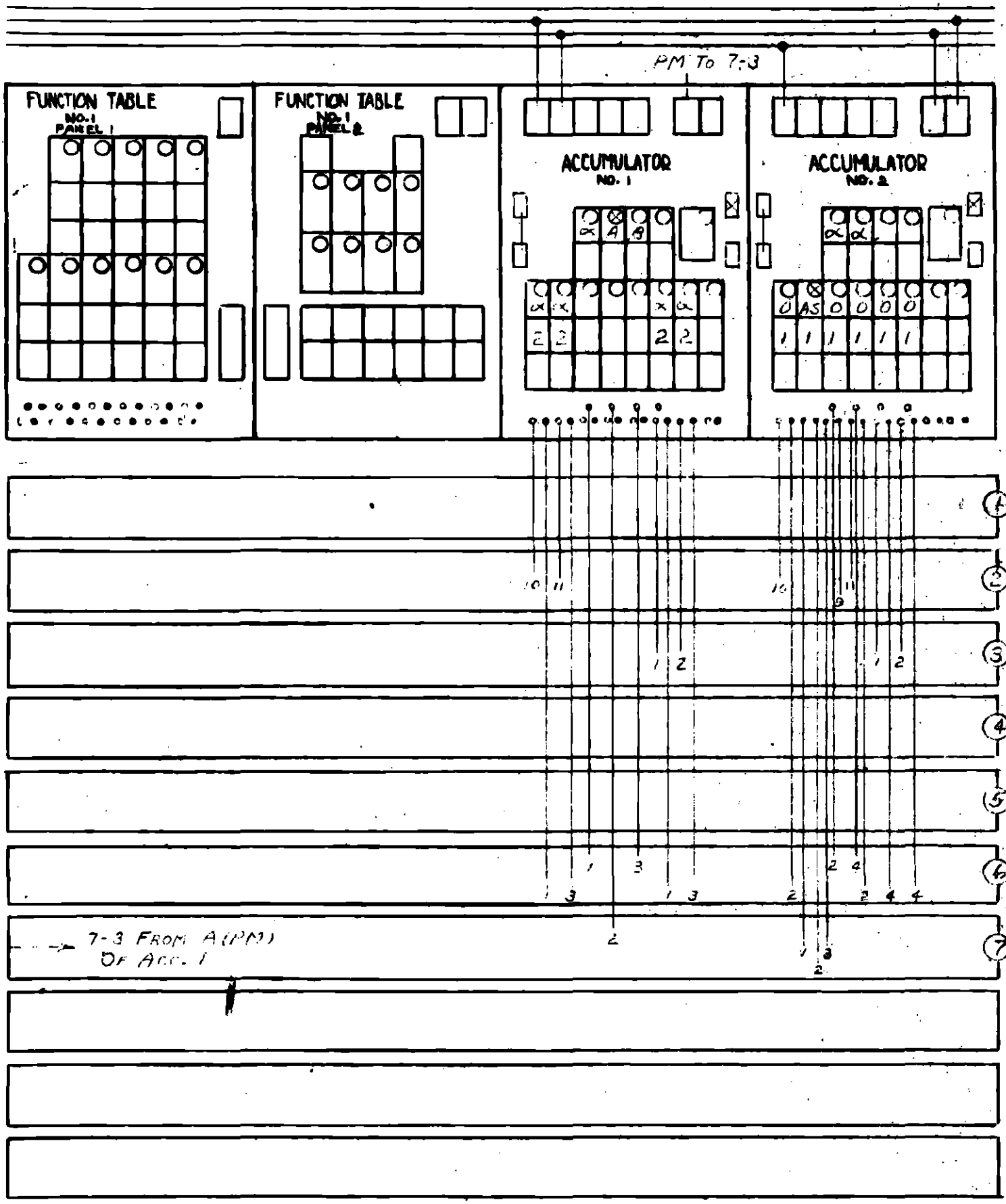


Fig. 10-9 (b)

Set-Up Diagram For Tests on y and y' - Problem 2

PX-8-407c

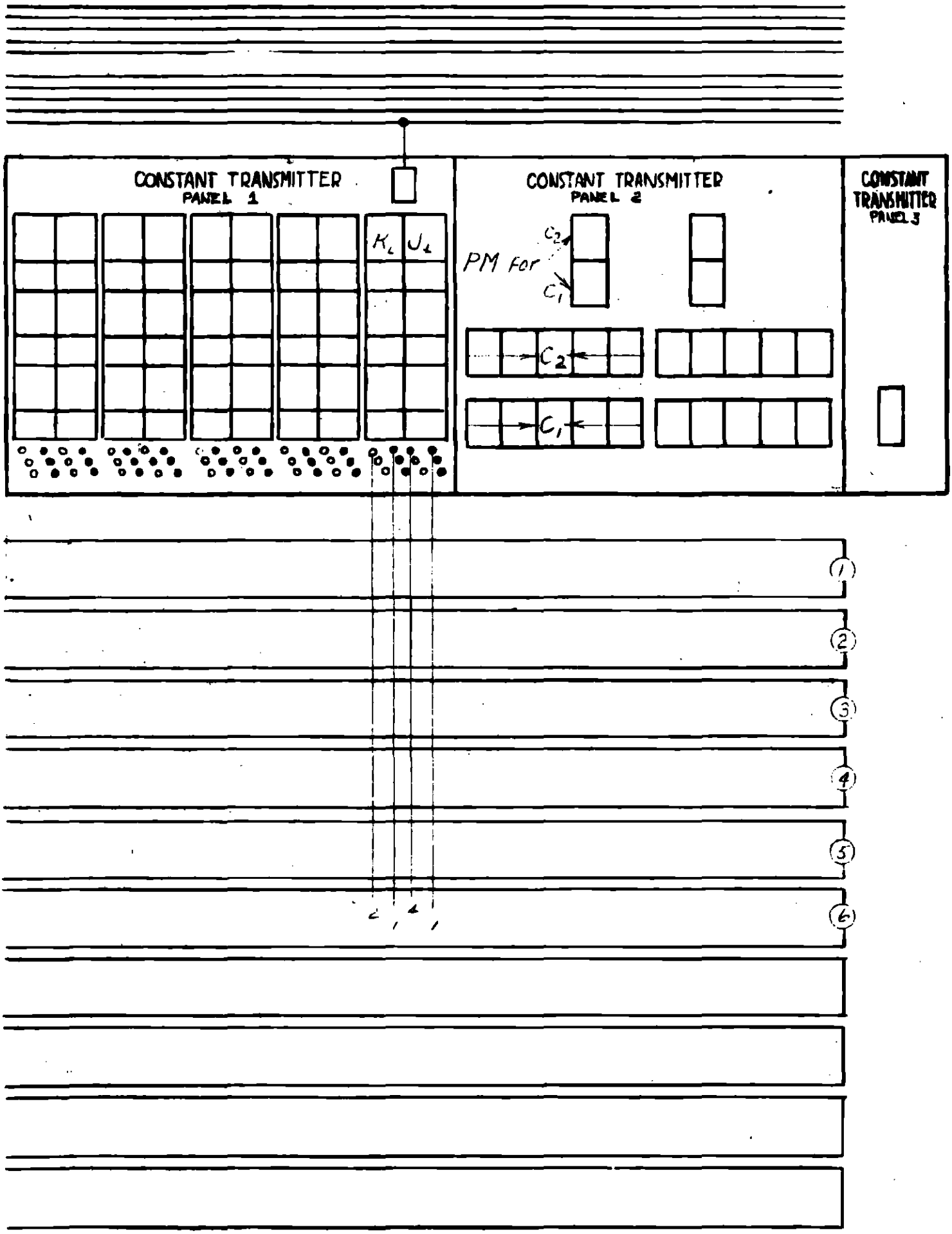
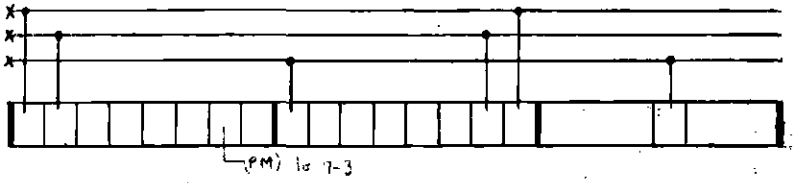


Fig. 10-9 (a)

Set Up Diagram For Tests on y and y' - Problem 8

TABLE 10-5

SET-UP TABLE FOR TESTS ON y^1 AND $\bar{y}$ – PROBLEM 2



	Add. Time	Master Programmer		Accumulator 1		Accumulator 2		Constant Transmitter	
Test of y^1-c_1	1	2-8 7i	7,σ 2-10						
	2			2-10 ⑤ α02	y^1	2-10 ⑤ U01 6-2			
	3			↓ 6-1		6-2 ① α01	C_1	6-2 ㉕ K_L 7-1	C_1
	4			6-1 ① α01	y^1-C_1	7-1 ⑥ AS C1 7-2	~~~		
	5			7-2 ② AC1 [H, (PM) to 7-3]	~~~	⑦ 001 1-3 2-9			
	6	2-9 7di							
Test of y^1+c_1	1	2-8 7i	7_2σ 2-11						
	2			2-11 ② α02	y^1	2-11 ② C01 6-2			
	3			↓ 6-3		6-2 ① α01	C_1	6-2 ㉕ K_L 7-1	C_1
	4			6-3 ③ B01	y^1+C_1	7-1 ⑥ AS C1 7-2	~~~		
	5			7-2 ② AC1 [2(PM) to 7-3]	~~~	⑦ 001 7-3 2-9			
	6	2-9 7di							
Test of $y-c_2$	1	2-8 7i	7_3σ 3-1						
	2			3-1 ③ α02	y	3-1 ⑦ 001 6-4			
	3			↓ 6-1		6-4 ② α01	C_2	6-4 ㉖ J_L 7-1	C_2
	4			6-1 ① α01	$y-C_2$	7-1 ⑥ AS C1 7-2	~~~		
	5			7-2 ② AC1 [H(PM) to 7-3]	~~~	⑦ 001 7-3 2-9			
	6	2-9 7di							
Test of $y+c_2$	1	2-8 7i	7_4σ 3-2						
	2			3-2 ⑪ α02	y	3-2 ⑩ 001 6-4			
	3			↓ 6-3		6-4 ② α01	C_2	6-4 ㉗ J_L 7-1	C_2
	4			6-3 ③ B01	$y+C_2$	7-1 ⑥ AS C1 7-2	~~~		
	5			7-2 ② AC1 [1(PM) to 7-3]	~~~	⑦ 001 7-3 2-9			
	6	2-9 7di							

trajectory to follow the test run. This is done by the output of dummy program Z. Pulse 4-2, through dummy program Y, yields 1-2 which goes to Ai. Pulse 5-1, the output of A_4O, initiates sequence 5.

It is to be noted that the method described above for clearing stepper C requires that the settings of the decade switches for stages 1 and 2 be multiples of the increment to the independent variable.

10.6.2.3. Sequence 5.

The output of A_4O stimulates the performance of sequence 5-1 in which the accumulators used for integration and printing are cleared and in which the initial conditions for the test run are transferred from the constant transmitter to accumulators. The last pulse of sequence 5.1, pulse 2-7, is delivered to Ei. Pulse 2-3, emitted from E_2O, stimulates the performance of the integration sequence. After 10 integrations have been stimulated, E advances to stage 3 so that pulse 2-7, delivered to Ei at the end of the 10th integration, causes 3-3 to be emitted. Pulse 3-3 stimulates printing and the output of the printing , pulse 1-2, causes stepper A to emit pulse 1-1 from A_5O and then to return to stage 1. Pulse 1-1 initiates the computations for the next trajectory. No provision has been made for counting the number of trajectory computations and terminating computations after a specified number. Instead, we rely upon the exhaustion of the cards in the reader's magazine to terminate computation (see Chapter VIII).

10.6.2.4. Tests on y and y'

The tests on $y'-c_1$, $y'+c_1$ etc. included in sequence 2 are described with the aid of Table 10-5 and Figure 10-9 (a-c). All 4 tests have been planned in such a way as to use the same program controls wherever possible. In table 10-5 the program controls used in each of the 4 tests are stimulated by pulses carried in program tray 7; those controls common to only 2 of the tests are stimulated by pulses carried in program tray 6.

XI. SYNCHRONIZING, DIGIT, AND PROGRAM TRANSMISSION SYSTEMS AND SPECIAL EQUIPMENT

There are three principal types of dynamic communication between units of the ENIAC: 1) communication of the synchronizing pulses and gates, 2) digit pulse communication, and 3) program pulse communication. These three types of communication are accomplished through the use of conductors mounted in trays, which, except for their outlets, are identical for all three purposes. Each tray has a ground and 11 conductors separated from one another by metal shields and has the dimensions 8 ft. x 9 in. x 1.25 in. Since each panel of the ENIAC is two feet wide, each tray extends the length of 4 panels. Found at both ends of a tray is a 12 point terminal. Trays can be connected serially to one another by jumper connections between these end terminals. Communication of types 1 and 2 above is by means of so called digit trays. These have twelve point terminals at 2 foot intervals. The digit tray is shown on PX-4-102. Program trays which have a set of 11 two point (1 wire and ground) outlets at 2 foot intervals are used for communication of type 3. The units of the ENIAC are connected into these trays by means of digit or program cables.

The synchronizing, digit, and program transmission system and associated equipment such as load resistors, shifters, deleters, etc. are discussed in the following sections: Transmission of Synchronizing Pulses and Gates, Section 11.1; Transmission of Digit Pulses, Section 11.2; and Transmission of Program Pulses, Section 11.3. Pulse amplifiers which may be used in either the digit or program transmission system are discussed in Section 11.4.

The semi-permanent connections between accumulators and the printer, high-speed multiplier, and divider and the interconnection of accumulators are treated in Section 11.5.

A portable control box which parallels certain controls on the initiating and cycling units is discussed in Section 11.6.

11.1. SYNCHRONIZING TRUNK

Nine digit trays connected in series by jumpers from the synchronizing trunk which delivers to the other ENIAC units the 9 trains of pulses and the carry clear gate emitted by the cycling unit and the selective clear gate emitted by the initiating unit. The synchronizing trunk runs around the back of the ENIAC below the ventilating panels from the initiating unit up until (but not including) panel 3 of the constant transmitter. The lines marked (1) through (11) on PX-4-102 are used for the following pulses or gates:

(1) CPP	(6) RP
(2) IP	(7) 1'P
(3) 9P	(8) CCG
(4) 10P	(9) 2P
(5) SCG	(10) 2'P
	(11) 4P

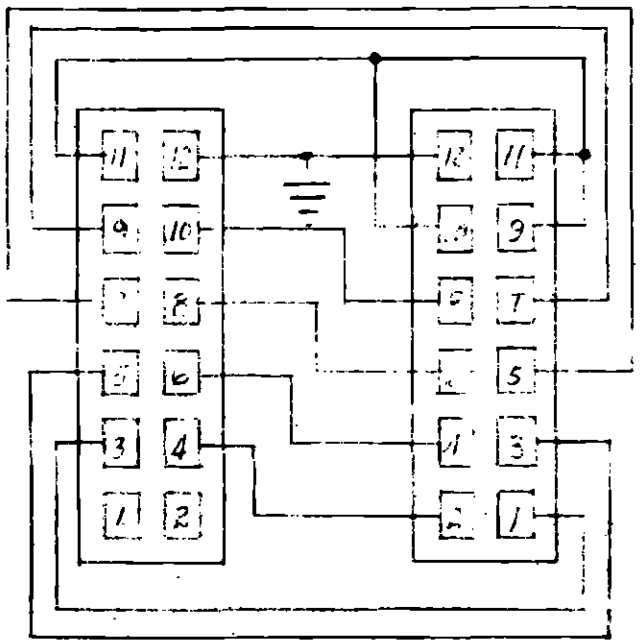
A cable with a 12 point plug at either end is used to bring into each unit the fundamental pulses and gates.

11.2. DIGIT TRANSMISSION

11.2.1. Digit Trunks

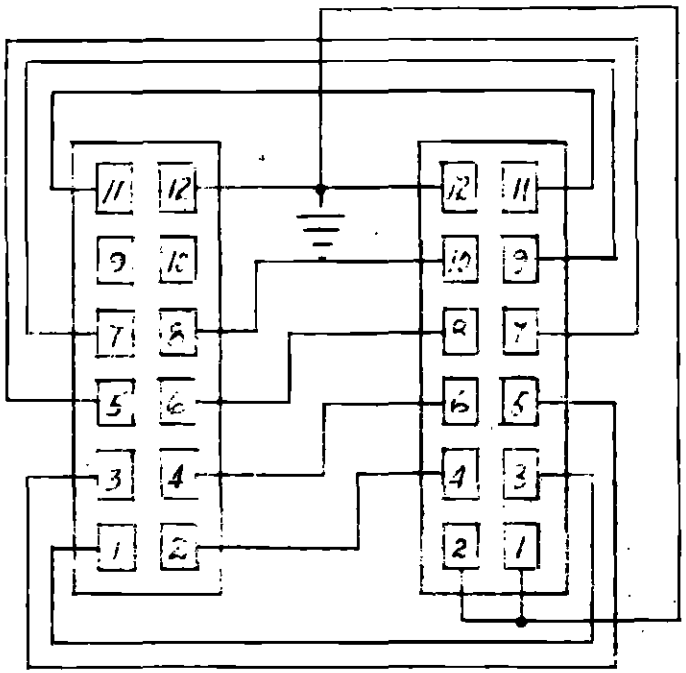
Seventy-two digit trays (in addition to the 9 trays for the synchronizing trunk) have been built for the ENIAC. These trays can be stacked on a shelf above the switch panels of the units from panel 1 of function table 1 to panel 2 of the constant transmitter inclusive. As many as 8 trays on one level can be

-2 SHIFTER



S P

+2 SHIFTER



S P

REVISIONS

DRAWING NUMBER WAS PX-4-104 NOW PX-4-104A

SENT FINAL REVISION RTA Allen 7/3/45 1

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SHIFTER (-2 & +2)

MATERIAL	FINISH	SCALE
—	—	—

Drawn by:	Checked by:	Approved by:
MSM OCT 28/1944	A Cael Coleman, Jr.	RTA 10/30/44

PX-4-104A

connected by jumpers. The load resistor (or load box) shown on PX-4-103 is plugged into an unused terminal usually on either the first or last tray of a set of jumper connected trays (certain exceptions to this statement are noted in Section 11.2.4.). The digit input and output terminals on the various units are connected into the digit trays by means of digit cables. A three-way plug is used at a digit tray terminal when more than one digit terminal of a unit is connected to a particular digit tray terminal. The term digit trunk is used to refer to a set of jumper connected digit trays, the load box at one end, and the digit cables which connect units to the set of digit trays.

In digit trunks, the lines marked 1 through 10 on PX-4-102 carry the digit pulses for decade places 1 through 10 respectively and line 11 carries the PM pulses (also see Section 11.2.2.).

11.2.2. Shifters, Deleters, and Adaptors

Shifters, deleters, or adaptors, used between digit cables, and digit terminals on the units, when it is desired to establish a special relationship between the decade place leads of the transmitting and receiving digit terminals, consist of specially wired 12 point plug and socket assemblies. Shifters are used to effect multiplication by powers of 10, deleters to eliminate digit pulses on certain decade place leads, and adaptors for other special purposes such as taking digital information to program lines.

The shifters which have been constructed at present are shown on PX-4-104 A-E. While in some cases special shifters could be built for use at digit output terminals, these shifters are for use only at digit input terminals. The terminology used here is that a +n shifter (for n positive) multiplies a number by 10^{n} (or shifts data n places to the left); a -n shifter multiplies a number by 10^{-n} (or shifts data n places to the right).

The following connections are made between the socket (S) and plug (P) leads of the +n shifters:

S [PM] ⟶ P [PM]

S [n left hand decade places] ⟶ Not connected to anything

S [decade places i] ⟶ P [decade places i + n] respectively

Ground ⟶ P [n right hand decade places]

The connections established in the -n shifters are the following:

S [PM] ⟶ P [PM and n left hand decade places]

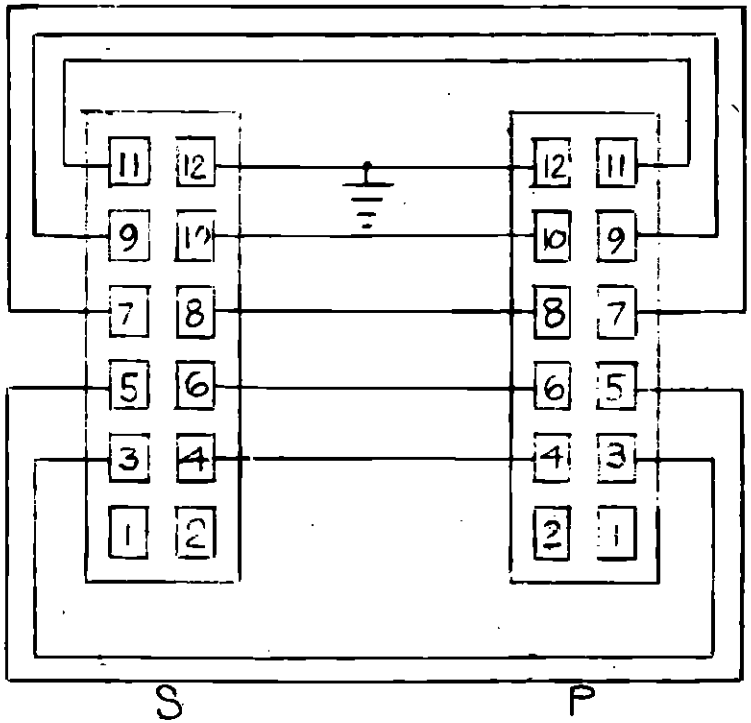
S [decade places i] ⟶ P [decade places i - n] respectively

S [n right hand decade places] ⟶ Not connected to anything

Notice that connections in the shifters for translating numbers n places to the right are made in such a way as to duplicate the PM pulses in the n left hand decade places of the receiving unit. Thus, for example, the number carried in a digit tray as M 4 823 000 000 is received through a -3 shifter in an accumulator as M 9 994 823 000. Because of the necessity of duplicating sign pulses in the n left hand decade places when a negative number is shifted to the right, a right hand shifter could not be designed for use at a digit output terminal for such a shifter would cause the PM transmitter to be loaded with the capacity of two or more lines in the digit trunk and would tie these lines together, thus making the trunk a special purpose trunk.

From the description of the +n and -n shifters above, it can be seen that if a +n shifter were used at a digit output terminal, the shift with regard to the n left hand decade places transmitted would be equivalent to that which results when a -n shifter is used at a digit input terminal. However, this interchange cannot be made because, in the case of a negative number, sign pulses

EXAMPLE:
DELETER NO. 8



DELETER NO.	OMIT CONNECTIONS	
9	S ① TO P ①	
8	S ① TO P ①	S ② TO P ②
7	S ① TO P ① S ③ TO P ③	S ② TO P ②
6	S ① TO P ① S ③ TO P ③	S ② TO P ② S ④ TO P ④
5	S ① TO P ① S ③ TO P ③ S ⑤ TO P ⑤	S ② TO P ② S ④ TO P ④
4	S ① TO P ① S ③ TO P ③ S ⑤ TO P ⑤	S ② TO P ② S ④ TO P ④ S ⑥ TO P ⑥

CONNECTIONS REV SEQ.
CHG A
SEMI-FINAL REVISION 7-9-45 | 1
EXAMPLE SHOWN
[illegible] 7-23-45 | 2

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DELETERS

MATERIAL	FINISH	SCALE

Drawn by:	Checked by:	Approved by:
J. EDELSACK OCT. 30, 1944	[illegible]	[illegible] 10/30/44

PX-4-109

are not duplicated in the n left hand decade places. Similarly a -n shifter cannot be used at a digit output terminal to accomplish a shift to the left because the n right hand decade place leads at the receiving end are not grounded.

The deleters which have been constructed are tabulated on PX-4-109. The deleters omit socket to plug connections for the leads associated with the decade places which are deleted. The deleters on PX-4-109 are designed for use at digit output terminals. Special deleters could be built for use at digit input terminals. Such deleters would ground the plug leads for the deleted decade places.

Certain special adaptors which combine shifting and deleting characteristics have also been constructed. These are shown on PX-4-117. These adaptors have the following properties:

3A	5 place to the right shifter with sign deletion
5A	5 left hand and PM place deleter
8A	1 place to the right shifter with sign deletion
4A	5 place to the left shifter with output of decade place 5 brought also to the PM lead
6A	3 place to the left shifter with sign deletion
10A	PM deleter
7A	5 place to the right shifter with sign deletion.

Adaptors for use at 12 point terminals on the divider and square rooter which function in a programming capacity are described in Section 6.4.2.

11.2.3. Load Units for Digit Trunks

The capacity to ground of any line in a tray is approximately 120 micro-farads. This capacity, plus that of the short jumper used to connect one tray to the next, is called a load unit. The capacity of a three foot cable

for connecting a digit input or output terminal to a digit tray is roughly equal to a load unit. Adaptors have negligible capacity. In order to obtain pulse rise times within the proper limits for safe and reliable operation of the ENIAC, the total number of load units (which equals the number of jumper connected trays plus the number of digit cables plugged into the trays) of a given digit trunk must not exceed 60 (also see Section 11.4.)

11.2.4. Special Uses of Digit Trays Without Load Boxes

A load box is used on all digit trunks formed by connecting digit trays together. Because the trays have been designed so that the load resistor is plugged into the unused terminals of one of the end trays of a trunk, the flexibility of being able to connect varying numbers of digit terminals to the trunks is possible.

In a few special cases, the resistance has been built into circuits of the units and certain single digit trays connected to these units by digit cables are used without load boxes. No other units may be connected in parallel into these trays.

In the case of the divider and square rooter (see PX-6-311), the following associated digit trays are used without load boxes:

1) the single digit tray* which carries components of the answer from the answer output terminal to the quotient accumulator's α input terminal and to the denominator accumulator's γ input terminal.
2) the digit tray** which carries programming instructions from the

*Running from the divider and square rooter to accumulator 5. A special short cable connects this digit tray to the α input terminal on the quotient accumulator and another cable connects this tray to the γ input terminal of the denominator accumulator.

**A single tray running from the divider and square rooter to accumulator 5 is used. Special cables (see PX-10-307) are plugged from this tray to the interconnector terminals on accumulators 2 and 7.

quotient and shift accumulator program terminal on the divider and square rooter to interconnector terminals on accumulators 2 and 7

3) the digit tray which carries programming instructions from the denominator and square root accumulator program terminal to accumulator 5.

In the case of the high-speed multiplier, a digit tray without load box is used to connect each of the three partial products output terminals LHPP II, RHPP I and II to the appropriate accumulator. A special short digit resistor cable without load connects the LHPP I terminal to accumulator 11 and, for safest operation, the three lowest digit trays are used for the other three partial products.

11.3. PROGRAM TRANSMISSION

11.3.1. Program Lines

Eighty one program trays have been constructed for the ENIAC. These trays, like the digit trays, are 8 feet long, have 11 wires and a ground, and at either end, have 12 point terminals so that a number of program trays can be jumper connected to form a program trunk. The program trays, however, have a group of eleven 2 point terminals spaced at 2 foot intervals instead of the 12 point terminals found on digit trays. A program pulse input or output terminal of a unit is connected to a program tray by means of a program cable which has a two point plug on each end (1 wire and a shield). In general, a load box (see PX-4-103) is plugged into an unused terminal at one end of program trunk. The term program line is used to refer to one conductor running the length of a set of jumper connected program trays and the program cables plugged into the conductor.

Fifty digit - program adaptors have been made. Each of these consists of a box with a 12 point digit plug connected to a group of 11, 2-point program sockets. These adaptors make it possible to use digit trays as program trays.

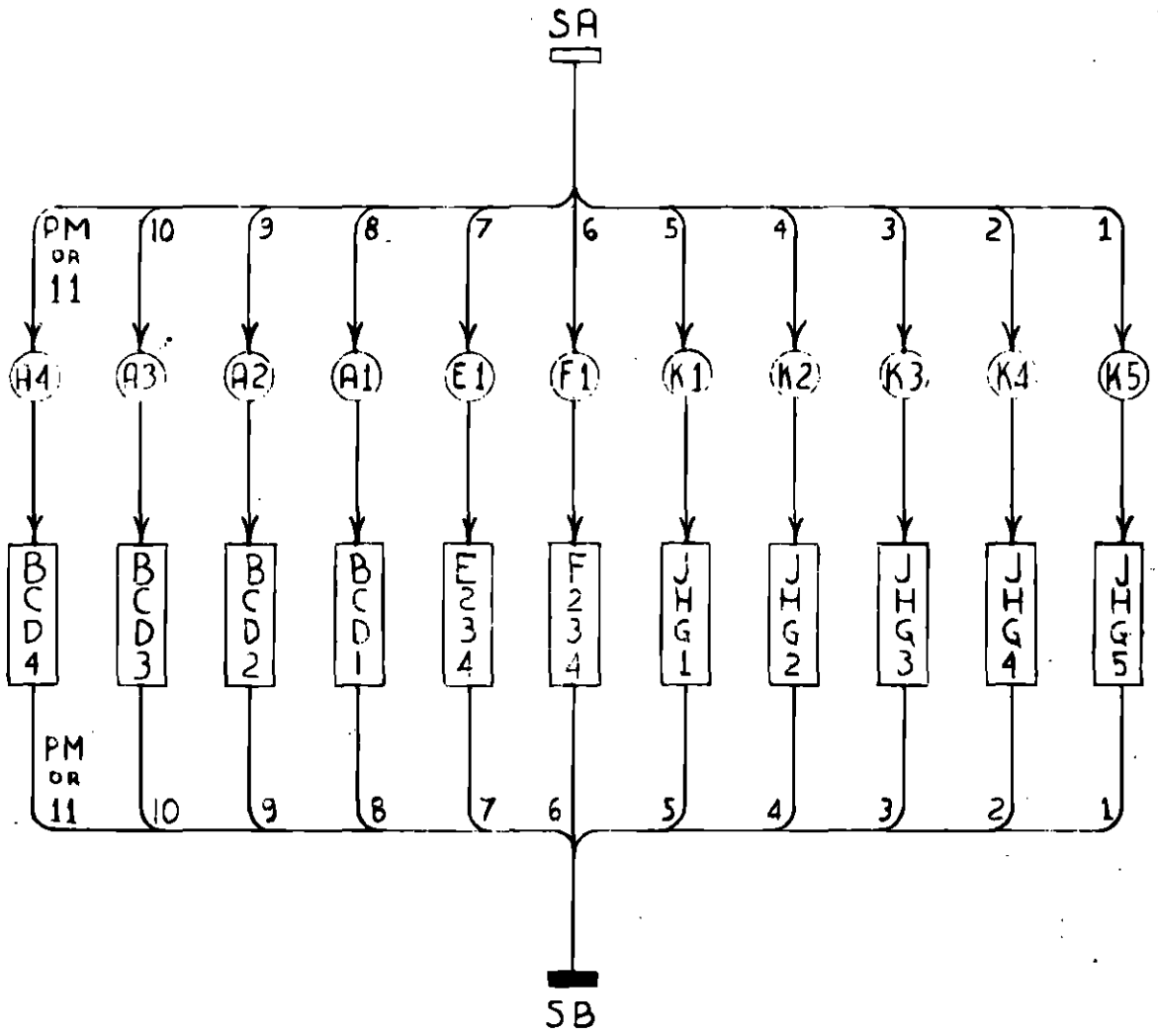
11.3.2. Special Program Cables

In addition to the standard program cables, a number of special U and Y program cables have been assembled. The U cable has a 2 point terminal on either end and a built in load. It is used to connect two program terminals on the same unit or on adjacent units without going into a program tray. The Y cable has three 2 point plugs. This latter type is used when it is desired to connect 2 program terminals on the same unit and also to connect to a program line.

11.3.3. Load units for Program Trays

In the case of program lines, as in the case of digit trunks, the number of load units must be restricted in order to provide suitable time constants for safe and reliable operation of the ENIAC. For program lines which carry only program pulses the total number of load units (number of jumper connected program trays through which the line runs and program cables plugged into the line) must not exceed 120. A program line which carries digit pulses, a case which can arise in magnitude discrimination programs for example, must not have more than 60 load units. The more stringent restriction of load units is made for lines carrying digit pulses particularly because the short interval between successive digit pulses makes necessary an especially short rise and fall time for digit pulses for safe resolution of these pulses. Also, the digit pulses are slightly broader than the program pulses so that even in the case where only 1 digit pulse is transmitted in a given addition time, for the most reliable operation, it is best to restrict the number of load units to 60.

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CODE

- INPUT SOCKET
- OUPUT SOCKET
- BUFFER
- TRANSMITTER

DRAWN BY H. CALDWELL ECKERT	PULSE AMPLIFIER BLOCK DIAGRAM	SCALE
CHECKED BY		PX-4-301
APPROVED BY		

11.3.4. Special Program Lines Without Load Resistor

Program lines without a load resistor are used to carry stimulating signals to the following program input terminals:

I_S and R_S on the initiating unit (see PX-9-302)

PA, 1A, and Cont. on the cycling unit (see PX-9-303).

If desired, special program cables without resistance load may be used instead of lines in program trays. Also, see Section 11.6. for a discussion of the portable control box which can be used to parallel these terminals.

11.4. PULSE AMPLIFIER

Three pulse amplifier units (and chassis for two more) have been constructed. The pulse amplifier unit provides a means of circumventing the load limit restriction (see Sections 11.2.3. and 11.3.3.) on the total number of digit terminals or program terminals that can be connected for communication with one another and also is capable of being used to isolate program pulses.

This device contains eleven identical circuits, each consisting of a buffer and transmitter (see PX-4-301). A signal delivered to the pulse amplifier by way of one of the leads of the 12-point terminal at the left of its front face, passes through the associated buffer and transmitter and is emitted from the corresponding lead of the output terminal on the right side. Power for the pulse amplifier is obtained by connecting the terminal on the left face to one of the four 12-point terminals at the bottom of the diagonally placed panels at either end of the wall containing the high-speed multiplier.

If two trays are connected by a pulse amplifier, each tray may have as many as the maximum number of load units specified for that type (digit or program). Furthermore, data transmitted through the tray connected to the input

PX-4 32

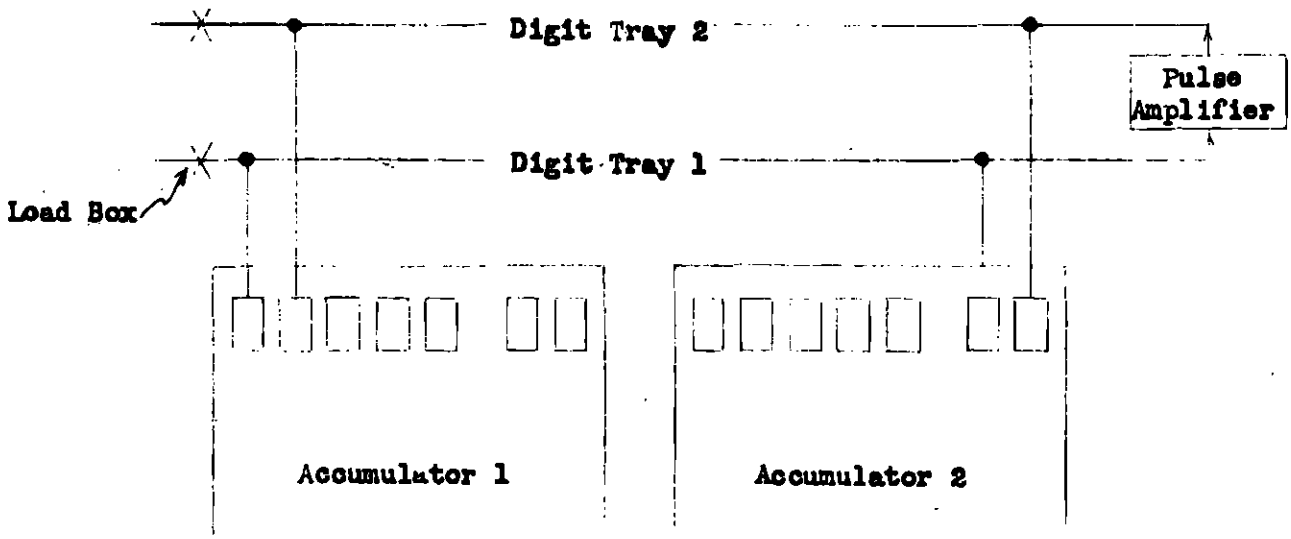


Fig. 11-1

DIGIT TRAYS CONNECTED BY PULSE AMPLIFIER

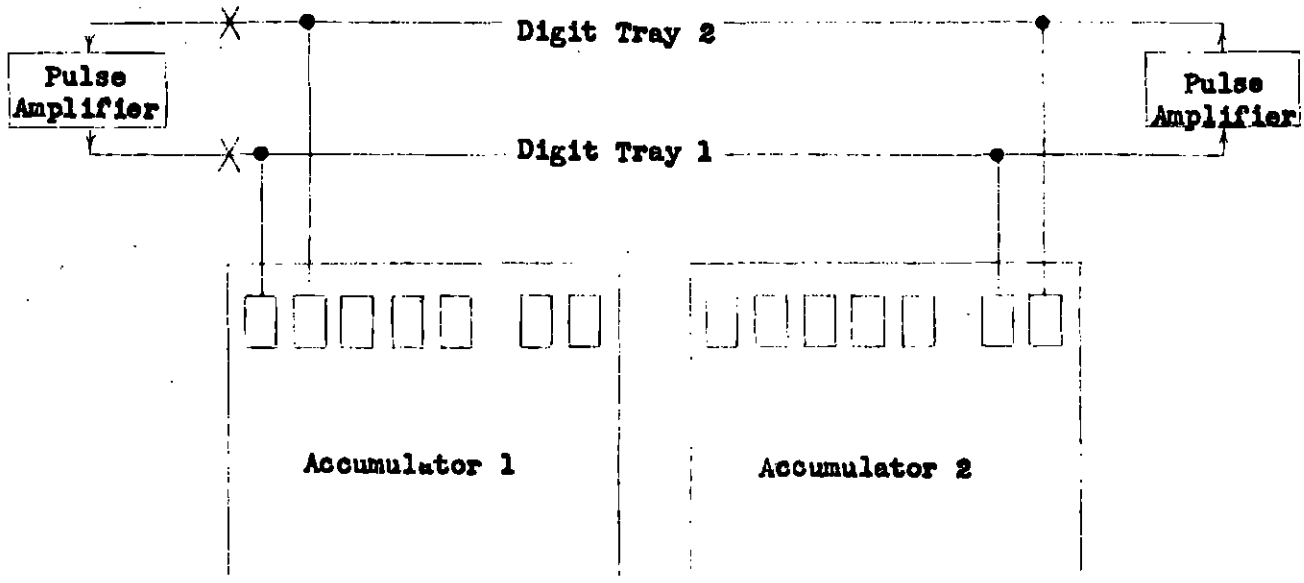
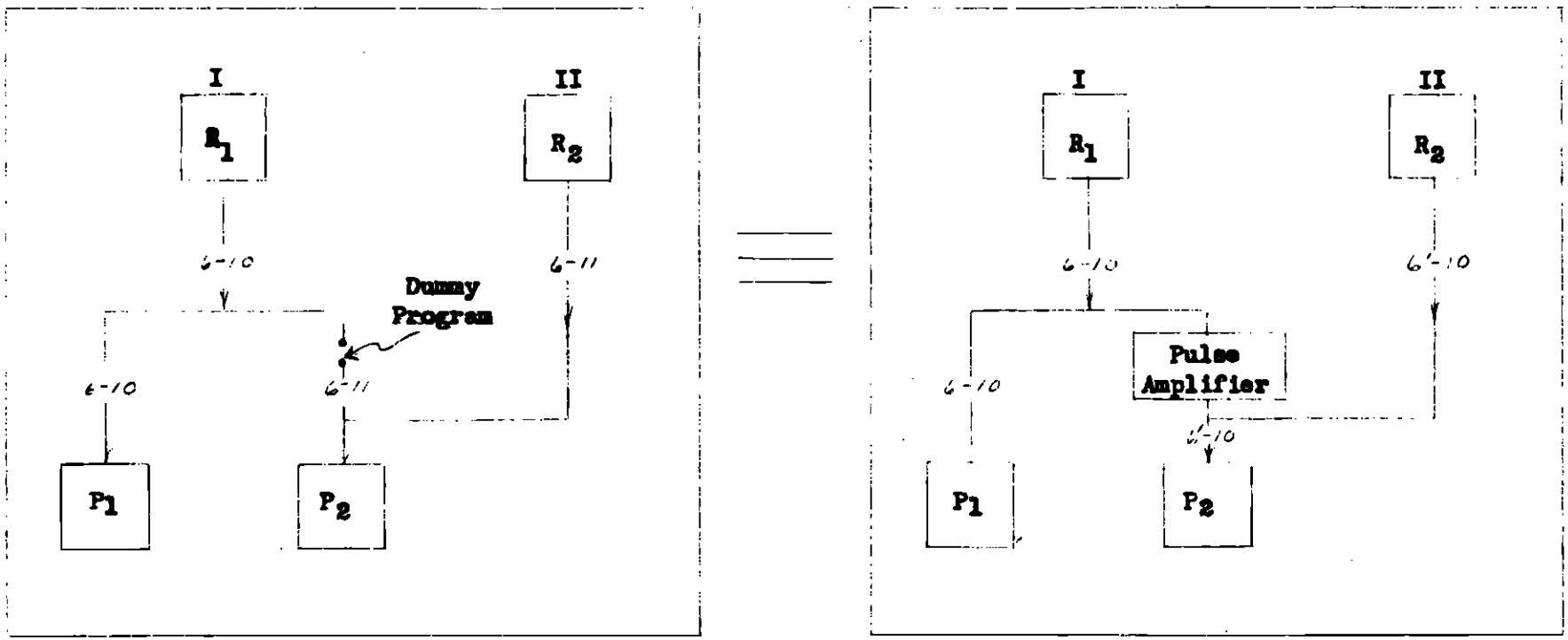


Fig. 11-2

BIDIRECTIONAL COMMUNICATION IN PULSE AMPLIFIER CONNECTED TRAYS



I: Programs P_1 and P_2 follow program R_1.

II: At some other time in the computation, program P_2 (without program P_1) follows program R_2.

Program tray 6 is connected to the input and 6' to the output of a pulse amplifier.

Fig. 11-3

ISOLATION OF PROGRAMS THROUGH THE USE OF A PULSE AMPLIFIER

of the pulse amplifier is communicated to the tray connected to the pulse amplifier's output. Data carried on the tray connected to the pulse amplifier's output, however, is not communicated to the tray connected to the input. For example, in Figure 11-1, the α input of accumulator 1 can receive from only the A output of accumulator 2; the β input of accumulator 2 can receive from both the A and S outputs of accumulator 2.

Through the use of 2 pulse amplifiers, two trays can be connected so that there is bidirectional communication between them. In Figure 11-2, for example, both the α and β inputs on accumulator 1 can receive from either the A or S outputs of accumulator 2.

The unidirectional communication in one of two trays connected by a pulse amplifier provides a means of using a pulse amplifier instead of one or more dummy program controls to isolate program pulses. In Figure 11-3, the schematic drawing shows two set-ups that are logically equivalent: one uses a dummy program control; the other, a pulse amplifier.

11.5. SPECIAL INTERCONNECTION OF UNITS

11.5.1. Connections to the Printer

The units whose static outputs are delivered to the printer so that data stored in them can be recorded are listed in Section 9.4. The reader is also referred to the following diagrams:

Static Output Cable	PX-4-111
Printer Adaptors	PX-12-114

11.5.2. The High-Speed Multiplier and Its Associated Accumulators

The accumulators connected to the high-speed multiplier for the communication of digital and programming information are discussed in Section 5.4.

Reference is also made to the following diagrams:

Interconnection of High-Speed Multiplier with Associated Accumulators	PX-6-311
Static Output Cable	PX-4-111
Accumulator Interconnector Cable (Multiplier)	PX-5-131

11.5.3. The Divider and Square Rooter and Its Associated Accumulators

The connections established between the divider and square rooter and its associated accumulators are described in Section 6.4. The interconnection of these units is pictured on PX-10-307 and, on this same drawing, reference is made to the drawings of special cables and adaptors used.

11.5.4. Interconnection of Accumulators

In Section 4.4.2. the interconnector terminal connections for using one accumulator as a 10 decade accumulator or for using 2 accumulators as a 20 decade accumulator are discussed. The following diagrams are relevant to that discussion:

Accumulator Interconnector Terminal Load Box	PX-5-109
Accumulator Interconnector Cable (Vertical)	PX-5-121
Accumulator Interconnector Cable (Horizontal)	PX-5-110
Accumulator Program Front Panel	PX-5-105

11.6. PORTABLE CONTROL BOX

Certain initiating unit and cycling unit controls which are particularly useful in testing the operation of the ENIAC have been described in Chapters II and III. These controls include:

Initial Clear Switch	Section 2.1.2.
Reader start switch and terminal R_S which parallels the switch	Section 2.2.
Initiating Pulse Switch and terminal I_S which parallels the switch	Section 2.2.
Operation selector switch for switching from 1P to either 1A or continuous operation, and the terminals 1A and Cont. which parallel this switch	Section 3.2.
1 Pulse or 1 Addition Time Switch and the terminal PA which parallels this switch	Section 3.2.

In Chapters II, and III there was described the direct operation of these controls at the initiating and cycling units or, except for the initial clear control, from anywhere in the ENIAC room with the aid of special program lines without load resistor.

The portable control box provides a third and more convenient means of operating these controls and the initial clear button. By means of a cable the portable control box is connected directly into the circuits of the controls mentioned above. This cable is long enough to permit the use of the control box anywhere in the ENIAC room. The controls on the box reading from top down are:

1) Operation selector switch for switching to 1 addition time or continuous operation when the operation selector switch on the cycling unit is set at 1 pulse time.

2) Initial clear button which, when pushed, causes initial clearing to take place. (Operation selector switch must be set at Cont. when initial clear button is pushed.)

3) Reader start button which is used to stimulate the reading of a card. Terminal R_0 emits a pulse when reading initiated in this way is completed, without the reception of an interlock pulse at R1.

4) Initial pulse button which, when pushed, causes a program output pulse to be emitted from terminal I_0 on the cycling unit.

5) 1 Pulse - 1 Addition push button. With the operation selector switch set at 1P or 1A respectively, one pulse or the 1 addition time sequence of pulses is given out each time this button is pushed.

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[illegible] CITY, N.Y., U.S.A.

A REPORT ON THE E[illegible]

[illegible]tronic Numerical Integrato[illegible]

[illegible] of Work under Contract [illegible]

Between

Ordnance Department [illegible]
Washington, D. C.

and

The University of [illegible]
[illegible] School of Electric[illegible]
Philadelphia, Pa.

Pennsylvania. University. Moore School of Electrical Engineering

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PART II

TECHNICAL DESCRIPTION [illegible]

by

Dr. Harry D. Hua[illegible]

Moore School of Electric[illegible] Engineering
University of Pe[illegible]

Pennsylvania. University. Moore school electrical engineering
29 Jan 50 Electronic Engineering Library

0. [illegible]

[illegible] ENIAC consists [illegible] parts, as follows:

[illegible] ing Manual

[illegible] enance Manual

[illegible] al Description [illegible]

[illegible] I - Chapters [illegible]

[illegible] nical Description [illegible]

[illegible] ume II - Chapters [illegible]

[illegible] Technical Description [illegible]

Included with the [illegible] Manual and Part [illegible] Technical Description are all drawings (Table 0.3 below) which are [illegible] understanding these reports. The Maintenance Manual assumes access to [illegible] file of ENIAC drawings.

[illegible] Part I of the Technical Description [illegible] those who wish to have a general understanding of how the ENIAC works [illegible] concerning themselves with the details of the circuits; it requires [illegible] knowledge of electronics or circuit theory. Part II is intended for those [illegible] a detailed understanding of the circuits. Its organization, [illegible], duplicates that of Part I so as to make cross referencing between [illegible] easy.

The ENIAC Operating Manual contains [illegible] of instructions for operating the ENIAC. It includes very little [illegible] material, and hence assumes familiarity with Part I of the [illegible] tion of the ENIAC. The ENIAC Maintenance Manual includes descriptions of the various test units and procedures for testing, as well as a list of [illegible] possible sources of trouble. It assumes a complete understanding of the [illegible] of the ENIAC, i.e. a knowledge of both Parts I and II of the Technical [illegible] tion of the ENIAC.

The Report on the ENIAC and the complete file of ENIAC drawings constitute a complete description and set of instructions for operation and maintenance of the machine. The drawings carry a number of the form PX-n-m. The following tables give the classification according to this numbering system.

TABLE 0.1

Values of n	Division
1	General
2	Test Equipment
3	Racks and Panels
4	Trays, Cables, Adaptors, and Junction Boxes
5	Accumulators
6	High Speed Multiplier
7	Function Table
8	Master Programmer
9	Cycling Unit and Initiating Unit
10	Divider and Square Root
11	Constant Transmitter
12	Printer
13	Power Supplies

TABLE 0.2

Values of m	Subject
101-200	Wiring Diagrams
201-300	Mechanical Drawings
301-400	Report Drawings
401-500	Illustration Problem Set-Ups.

The reader of this report will be primarily interested in the types of drawings listed in the following paragraphs. A table on page 4 gives the corresponding drawing number for each unit of the ENIAC.

1) Front Panel Drawings. These drawings show in some detail the switches, sockets, etc., for each panel of each unit. They contain the essential instructions for setting up a problem on the ENIAC.

2) Front View Drawings. There is one of these drawings for each kind of panel used in the various units of the ENIAC. These show the relative position of the trays and the location of the various neon lights. Since these drawings show the neon lights, they can be used to check the proper operation of the various units.

3) Block Diagrams. These drawings illustrate the logical essentials of the internal circuits of each unit. That is, resistors, condensers, and some other electrical details are not shown; but complete channels (paths of pulses or gates representing numbers or program signals) are shown in all their multiplicity. These drawings will be of interest to those who are interested in Parts I and II of the Technical Report.

4) Cross-section Diagrams. These drawings are electronically complete except that only one channel is shown where there is more than one. Thus, these drawings show every resistor and condenser and any other electronic elements belonging to any circuit. These drawings will be of particular interest to the maintenance personnel and to those reading Part II of the technical report.

5) Detail Drawings. All other drawings of the ENIAC come under this heading. A complete file of drawings is available at the location of the ENIAC.

Table 0.3
[illegible] DRAWINGS

Unit	Front Panel	Front View	Block Diagram	Cross - Section
Initiating Unit	PX-9-302 9-302R	PX-9-305	PX-9-307	
Cycling Unit	PX-9-303 9-303R	PX-9-304	PX-9-307	
Accumulator	PX-5-301	PX-5-305	PX-5-304	PX-5-115
Multiplier	PX-6-302 6-302R 6-303 6-303R 6-304 6-304R	PX-6-309	PX-6-308	PX-6-112A 6-112B
Function Table	PX-7-302 7-302R 7-303 7-303R	PX-7-305	PX-7-304	PX-7-117 7-118
Divider and Square Rooter	PX-10-301 10-301R	PX-10-302	PX-10-304	
Constant Transmitter	PX-11-302 11-302R 11-303 11-303R 11-304 11-304R	PX-11-306	PX-11-307	PX-11-116 11-309 (C.T. and R.)
Printer	PX-12-301 12-301R 12-302 12-302R 12-303 12-303R	PX-12-306	PX-12-307	PX-12-115
Master Programmer	PX-8-301 8-301R 8-302 8-302R	PX-8-305	PX-8-304	PX-8-102

Other drawings of particular interest:

Floor Plan	PX-1-302	IBM Punch and Plugboard	PX-12-112
A.C. Wiring	PX-1-303		PX-12-305
IBM Reader and plugboard	PX-11-119 PX-11-305	Pulse Amplifier and Block Diagram	PX-4-302 PX-4-301

Interconnection of Multiplier and Accumulators PX-6-311
Interconnection of Divider and Accumulators PX-10-307

The front view drawings and the large front panel drawings (whose numbers do not end with "R") are bound as a part of the Operator's Manual.

Included with the report is a folder containing all the drawings listed in the above table except the large front panel (see above). A complete file of drawings is available at the location of the ENIAC.

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TECHNICAL DESCRIPTION OF THE ENIAC, PART II.

This part of the report describes in some detail the circuits used in the various units of the ENIAC. Only sufficient programming details, that is, switch settings and plugging details, will be given to enable the reader to understand the circuits. For more detailed programming and illustrative set-ups the reader is referred to the corresponding chapters and sections of part I of this report.

I. GENERAL DESCRIPTION OF THE ENIAC

This chapter describes the arrangement of the units of the ENIAC, gives a summary of its mode of operation, and describes certain vacuum tube and circuit arrangements which are used repeatedly in the units of the ENIAC.

1.1. Brief description of the ENIAC.

The ENIAC is an extremely high speed electronic numerical computing device. It performs sequences of computations (without manual attention except for setting up) which are made up of the following operations.

1. Reading initial data from IBM cards
2. Addition
3. Subtraction
4. Multiplication
5. Division
6. Square-rooting
7. Looking up function values in function tables
8. Punching the results on IBM cards.

Generally, the units of the ENIAC have been designed to carry on the above operations using ten digit decimal numbers. In case greater accuracy is desired provision has been made to carry on the above operations using twenty digit decimal numbers. Actually there is an upper limit to the number of different steps of computation that can be performed without the attention of the operator, but this upper limit has been made high enough to handle a very large class of computing problems.

The ENIAC is a discrete variable rather than a continous variable device. Consequently, errors in computation arise only from mathematical considerations (such as truncation, that is, the replacing of derivatives by difference quotients, and rounding-off errors) or from failure of some circuit in the device. Careful attention was given to minimizing failures and for

easy location and repair of them when they occur. The ENIAC uses the decimal system, and handles negative numbers by means of complements with respect to 10^n.

1.1.1. Units of the ENIAC

Table 1-1 gives a list of the units of the ENIAC, the number of program controls of each, and the purpose of each unit. Essentially, the number of program controls determines how many times that unit may be used for a different purpose in a particular sequence of computations.

The Initiating Unit. Besides a hum oscilloscope to check the a-c supply lines and voltmeters to read the various a-c and d-c voltages, the initiating unit has the following switch controls:

1) Start Switch - Turns on the cooling fans and the heaters. The amber light indicates that the switch has been thrown.

2) D-C On-Off Switch.- This switch is located on the fuse panels. It can be used to turn the d-c power on and off.

3) Stop Switch - Turns off all the power.

4) Initial Clear - Clears all the units in preparation for starting a sequence of computations. Green light comes on when initial clear has occurred.

5) Door shunt switch - Enables the ENIAC to be operated for checking purposes with some of the back covers off.

6) Reader Start Switch - Causes the IBM Reader to read a card and then give out a program pulse which can be used for starting a sequence of computations. The Reader can be caused to operate by a program pulse as well as by use of this switch.

7) Initiating Pulse Switch - This switch causes a synchronized program pulse to be given out. This can be used to start a sequence of computations.

The initiating unit contains selective clear program controls by which certain predetermined accumulators can be caused to clear. The printer program controls are also located in the initiating unit. A clock which measures the time the power supply heaters are on is also located on this panel.

Cycling Unit. This unit produces the pulses which are used to represent digits or program signals, and causes the various units of the ENIAC

TABLE 1-1

Units of the ENIAC

Number of units	Name of unit	Number of program controls per unit	Purpose
1	Initiating unit	6	Control center for starting and stopping computations. Contains six selective clear program controls.
1	Cycling unit	---	Pulse and gate producing unit which causes the other units of the ENIAC to operate in synchronism.
20	Accumulator	12	Each accumulator can store ten digit numbers, add numbers (transmitted by other units) to its contents, or transmit its number and/or its complement to other units and clear.
1	High-Speed Multiplier	24	This unit makes use of built-in multiplication tables to perform high-speed multiplication.
1	Divider-Square rooter	11	This unit divides two, ten or twenty digit numbers and extracts the square roots of ten or twenty digit numbers.
3	Function table	11	These units can look up the values of functions. The values of the functions must be set up on switch panels by the operator.
1	Constant Transmitter and IBM reader	3	This unit reads initial data from IBM cards, sets it up on relays and transmits it electronically. The IBM reader program control is located in the initiating unit.
1	Printer and IBM punch	1	This unit causes the results of sequences of computations to be punched on IBM cards. The IBM Gang punch program control is located in the initiating unit.
1	Master programmer	---	This is a program control device which decides when to change from one sequence of computations to another, or when to print and when to read more initial data.
Program trunks and digit trunks			These are transmission lines which make it possible to transfer numbers and program signals from unit to unit as needed.

to operate in synchronism. Table I-2 lists the kinds of pulses and gates that are produced at this unit and transmitted to the other units over the cycling trunk.

Accumulator. Depending upon the switch settings, digit trunk connections, and program trunk connections an accumulator can accomplish the following things:

1) Store a ten digit number or its complement and a PM indication determining which it is.

2) Transmit over a digit trunk the number, its complement, or both. After transmitting it may or may not clear as desired.

3) Add to its contents a positive or negative number transmitted by some other unit of the ENIAC, properly indicating the sign of the sum.

4) All accumulators may transmit their contents by means of static cables to either the multiplier or the printer. Certain accumulators are semi-permanently connected to the printer. The sign indication is transmitted to the divider in this manner.

Multiplier. The multiplier multiplies a ten digit multiplicand by an n ($n \leq 10$) digit multiplier in $n+4$ addition times and rounds off the answer to any prescribed number of places if so desired. To do this, the multiplier makes use of four or six accumulators. This high-speed multiplication is accomplished by means of built-in multiplication tables.

Divider-Square Rooter. This unit can divide ten or twenty digit numbers and can extract the square root of a ten or twenty digit number. If p is the setting of the places switch a division takes $10 + 2$ (number of trial subtractions) $+ 2p$ addition times.

Function Table. The function table working in conjunction with either a variable or a permanent table can transmit any one of 104 values of a function (or if less than seven digits is needed 208 values of the function). To facilitate interpolation, arrangement has been made to transmit any one of the four neighboring values if desired. If a functional value is to be transmitted r times ($1 \leq r \leq 9$) the process of obtaining the functional value takes

TABLE 1-2

Kind of pulse or gate		Remarks
CPP	Central Program Pulse	Used as a program pulse.
10P	Tens Pulses	Used to cycle the decades of accumulators when transmitting a number over the add or subtract outputs.
9P	Nines Pulses	Various combinations of these pulses are used to represent the digits 0, 1, ..., 9.
1P	One Pulse	A coded system makes use of various combinations of these groups to represent the digits 0, 1, 2, ..., 9.
2P	Two Pulses	
2'P	Two-primed Pulses	
4 P	Four Pulses	
1'P	One-primed Pulse	Generally used as a correction pulse in taking complements (negative numbers).
CCG	Carry-Clear Gate	Used to take care of carry-over in the decades of the accumulators and to clear accumulators when so programmed.
RP	Reset Pulses	These pulses are used to reset decade flip-flops in the accumulators and to provide the delayed carry-over pulse.

The time unit of operation for the ENIAC is one addition time. This is normally a time interval of 200 micro-seconds. An addition time is divided into 20 pulse times, each 10 micro-seconds long. The pulses listed in the above table arrive via the cycling trunk at each unit of the ENIAC once each addition time. The pulse times at which the various pulses and gates are produced is illustrated by PX-9-301 or by the diagram appearing on the front panel of the cycling unit.

+ 4 addition times.

Constant Transmitter and IBM Reader. The IBM reader can read sixteen groups of positive or negative five digit numbers from an IBM card and cause these to be set up on relays in the Constant Transmitter. Four other groups of five digit numbers may be set up on panel three of the Constant Transmitter. Provision has been made for combining these five digit groups to make ten digit groups. When desired, the Constant Transmitter can transmit any of these groups of numbers to various other units of the ENIAC. Transmission of a number by the constant transmitter takes one addition time, but reading and setting up relays to change a number takes longer.

Printer and IBM Gang Punch. The printer can be connected by static cables to eighty decades (and sixteen PM units) located in either accumulators or in the master programmer. When so programmed the printer will cause the IBM punch to punch as many as eighty digits (again associated in groups of five or its multiples for PM purposes) and 16 PM indications on the IBM card. Thus, the numbers registered in these printing accumulators or in certain decades of the Master Programmer can be punched on an IBM card.

Master Programmer. Whole sequences of computations can be arranged locally, that is, by setting switches and plugging cables at the various units of the ENIAC. The master programmer is particularly designed to cause certain sequences of computations to repeat, or to keep track of how many sequences are performed, or by means of digit or sign control to change the sequences when variables reach prescribed values, or combinations of these operations.

1.1.2. Digit Trunks.

A digit tray is about eight feet long and has eleven lines. Ten of these lines carry the pulses representing the ten different digits of a ten digit number and the eleventh carries pulses representing the PM indication.

s takes several trays to extend around to the various units. Several trays onnected together with jumper cables and with one load box plugged in forms digit trunk. These digit trays rest on brackets just above the front panels of the units.

1.1.3. Program Trunks.

Program trays are similar to digit trays except for the type of outlet sockets. Several trays interconnected with jumpers and one load box plugged in constitute a program trunk. The program trays rest below the front panels of the units.

1.1.4. Static Cables

Whenever the decades of an accumulator are connected by static cables to some other unit it means that every stage in every decade and at least one stage of the PM counter is connected to the proper points of the other unit (printer, for example). To accomplish this, two 55 conductor cables are used. In the case of the accumulator to printer connections, only 51 leads of each cable are used, that is, 50 for five decades and the other line for PM indication. An adaptor is used at the accumulator end to connect both PM lines to the M static output of the PM counter. In the case of the static connections to the Master Programmer the PM line is not used, but an adaptor (see 9.2) must be inserted in the printer to keep the PM relays from operating.

1.2. FUNDAMENTAL ELECTRONIC UNITS OF THE ENIAC

There are certain fundamental circuits which are repeated many times throughout the ENIAC. We shall discuss a number of these here. In the course of the following discussion we shall use the terms "pulse" and "gate" with the following meanings:

Pulse: A pulse is a positive or negative change in potential which has a duration of about two to five micro-seconds (μsec.)

Gate. A gate is a positive or negative change in potential which a duration of ten micro-seconds or more. The Carry-Clear Gate (see -306), for example, lasts for 70 micro-seconds.

It will be seen that the same type of electronic units located in different parts of the ENIAC operate at different absolute voltage levels. For example, the flip-flop illustrated (PX-1-105) operates in a voltage range from -555 volts to -360 volts. Other flip-flops operate in ranges of from -85 to +110 volts and from -920 to -725 volts. The power supply produces a range of voltages from -920 volts to +550 volts.

Throughout this report the following convention will be followed with regard to input and output circuits. An input or output will always be represented by only one lead. The return circuit should always be thought of as going back to some point on the bleeder of the power supply. For example, the cathode of a tube may be at zero volts and the output may come from the plate with a range of potential of from 100 volts to 150 volts, say. Instead of using this output with respect to zero it may be used with respect to -20 volts giving an input potential for the next circuit of from 120 volts to 170 volts. Thus, the reference point varies a great deal from circuit through the ENIAC, and it seems impractical to try to represent the return circuits on such diagrams as PX-1-105 to PX-1-110.

1.2.1. Flip-flop.

A flip-flop is a four tube vacuum circuit which is the electronic analogue of an electric switch. Two of the tubes (T_3 and T_4 on PX-1-105) constitute the flip-flop itself, that is, a circuit with two stable states. The other pair of tubes (T_1 and T_2) are called triggering tubes.

The triggering tubes. Assuming that no signal is arriving over the set input, the grid of T_1 is at saturation. This causes the tube to conduct. Thus, if a negative signal of the proper magnitude arrives over the set input the grid will fall below cut-off and the tube will cease to conduct.

In order to secure reliable operation it has been a design principle that in all such cases the grid should be driven three times below cut-off. Furthermore, to provide for the increase in tube resistance with aging, the applied signal has been so arranged that it will always be at least two and one half times below cut-off.

The flip-flop. If the trigger tube T_1 goes off the grid of T_3 will rise well above the cathode potential and T_3 will start conducting. The plate potential of T_3 will drop and this drop in potential will be carried through the condenser C_4 to the grid of T_4 tending to cause T_4 to go off. As T_4 starts to go off its plate potential rises through condenser C_3 this causes the grid of T_3 to rise even faster. Thus, the whole process accelerates. Tube T_3 becomes conducting and T_4 goes off. This being a stable condition, the tube T_3 remains on and T_4 off until such time as trigger tube T_2 goes off.

The output potential at O_1 is -490 volts and of O_2 is -430 volts. After the flip-flop is set by an incoming signal at S the potentials of O_1 and O_2 are interchanged, and they will remain this way until a reset signal arrives at R.

Note that the condensers C_1 and C_2 isolate the DC circuits so the input to the flip-flop may operate at a voltage level which is sometimes as much as 600 volts above the level of the flip-flop.

The general plan will be to connect the outputs O_1 and O_2 to the grids of tubes whose cathodes are at a potential between these two output potentials. For example, in receivers and transceivers these outputs go to the grids of 6SN7's whose cathodes are at -450 volts. Thus, -490 volts is well below cut-off for the one tube whereas -430 volts is far above cut-off for the other one. In this manner static voltages produced by a flip-flop are transmitted to other circuits.

The neon light is visible on the front panel. It is lighted when the flip-flop is set, that is when tube T_3 is conducting.

2.2. Counters

PM Counters. The PM counter is a binary ring counter. That is, it has two stable states and just one input line. A first incoming signal will step it from stage one to stage two whereas the second incoming signal will step it back to stage one. Thus, an even number of pulses arriving over the input line will leave it in its initial condition whereas an odd number leaves it in the other state.

The tubes T_1 and T_2 in PX-1-109 act as triggering tubes. Whenever a positive signal arrives on the input both of these tubes begin to conduct. This causes the grids and plates of both T_3 and T_4 to take a negative swing. Since T_4 is off it has no effect there, but T_3 is caused to go off. As T_3 goes off its plate becomes more positive and through condenser C_3 the grid of T_4 also takes a positive swing. As T_4 begins to conduct its plate takes a negative swing and this through condenser C_2 further causes tube T_3 to go off.

The static output circuits are very similar to the outputs of the flip-flop described above. The positive output has the high potential (relative to the other output) whenever the PM counter is registering a positive number. With tube T_3 conducting and T_4 not (as illustrated) the neon bulb labeled P will be lit and the one labeled N not.

A counter similar to the PM counter is used in the divider-square rooter.

Decade ring counters. A decade ring counter is a ten stage (with two tubes per stage) ring counter with ten different stable states. Each stage has two tubes which will be called respectively tube I and tube II. Only one tube of each stage is conducting. If tube I is conducting that stage will be said to be in state I; if tube II is conducting then that will be said to be in state II. The stable state of the whole ring is with one stage in state I and the other nine stages in state II. The circuits (see the cross

tion PX-5-115 or the decade wiring diagram PX-5-133) are so arranged that one stage is in state I and a pulse is received it will go into state II and the next following stage will go into state I. Pulses that step the ring are negative and are introduced on all the cathodes of the tubes II. This pulse has little effect on the stages in state II but causes the stage in state I to go into state II. As this stage goes from state I to II the carry-over circuit causes the next following stage to go into state I. The fact that this carry-over pulse (through the 50 μf. condenser) will be in conflict with the stepping pulse applied to the cathode requires careful design to obtain reliable operation. Thus, the stepping pulse must be of precise shape and duration, and the carry over pulse must over-ride it. This is accomplished by putting the incoming pulses through a pulse standardizer (see section 1.2.7.) and by using the proper circuit parameters in the decade ring circuit.

The two cathode resistors for tubes in state I and tubes in state II are so chosen to permit only one mode of operation, namely, one stage in state I and the other nine stages in state II.

Other ring counters. There are a number of other ring counters in the various units of the ENIAC. Essentially they differ from the decade ring counters only in the number of stages they contain. A list of these ring counters follows:

a) The repeater ring. (See PX-5-115) The repeater ring is used in each accumulator to count the number of times a particular repeat program control operates. This ring and its pulse standardizer are built in one plug-in unit. This same plug-in unit is used in the Divider-Square rooter for a different purpose, see (d) below.

b) The cycling unit ring. (See PX-9-307) There is a twenty stage ring counter in the cycling unit which controls what happens during the twenty pulse times of an addition time.

e) The multiplier ring. (See PX-6-308) This ring controls the ceps of multiplication. It consists of fourteen stages, ten of which are ociated with the ten digits of the multiplier which may be used in multi- ication.

d) The divider-square rooter program ring. (See PX-10-304) This ng controls the beginning and final parts of the processes of division or quare rooting. It is a nine stage ring which with its pulse standardizer is entical with the repeater ring plug-in units. (see a) above)

e) The divider-square rooter place ring. (See PX-10-304) This en stage ring keeps track of the place in the division or square rooting rocess. This ring is identical with the master programmer decade rings (see i) below).

f) The function table argument ring counters. (See PX-7-304) These rings (a units ring of ten stages and a tens ring of eleven stages) receive the argument from an accumulator.

g) The function table program ring. (See PX-7-304) This thirteen stage ring controls the setting up of the function table networks and counts the number of times (up to nine) the functional value may be transmitted.

h) Master programmer decade rings. (See PX-8-304) There are twenty decade rings located on the two panels of the master programmer. These can be used to count the number of times certain sequences of computations are performed.

i) Master programmer stepper rings. (See PX-8-304) There are ten six stage rings which are associated with the ten steppers of the master programmer. These control the output of the program pulses given out by the master programmer.

1.2.3. Gate Tubes.

Besides being able to count and record pulses at high rates it is necessary to control the pulses, switching them into one unit or another.

In order to do this quickly, electronic switching is used. A vacuum tube used as a switch so as to allow or deny passage of pulses or other signals is known as a gate. Gate tubes are used in the ENIAC for a variety of control purposes. They connect the input channels of any given accumulator to particular digit trays when desired. They are used in the carry-over circuits to pass carry over pulses. Each programming circuit contains many gate tubes.

Most of the gating or switching in the ENIAC is accomplished by the use of multiple grid vacuum tubes. Various gate tube circuits are illustrated on diagram PX-1-106. If there is no input signal to either control grid of the gate tube of PX-1-106, the second control grid is at about -40v. This is well below cut-off for that grid (cut-off is -14 volts for 6SA7 with the first control grid connected to the cathode). Moreover, the first control grid is at -40 volts which is well below cut-off (-7 volts if second control grid is connected to the cathode), so the tube is not conducting and the potential on the output is near +160 volts. If any positive signal (of about 50 volts) arrives on either control grid the tube will not conduct. Thus, any signal arriving on the first input has no effect. However, if a signal arrives on both grids the tube will conduct and the plate potential will drop. For example, input 2 may connect to the plate of an inverter tube (see section 1.2.6.) which is normally on. If this inverter tube is conducting and the circuit parameters are properly arranged the potential of control grid 2 will be well below cut-off and any signal arriving on control grid 1 will not be passed. When the inverter is off the second control grid is at about +20 volts and any positive signal arriving at the first control grid will be passed.

The resistance and voltages and even the type of tube used in gating circuits varies from circuit to circuit throughout the ENIAC. Various situations are illustrated on the cross sections of the units of the ENIAC.

A gate tube may be called a coincidence tube, since an output will be obtained only if the signals applied to the inputs one and two coincide in

time. Two other types of coincidence circuits used respectively in the Function Table and the Master Programmer are illustrated on PX-1-106.

In the case of the triple coincidence circuit all three of the tubes 1, 2, and 3 must go off before the two control grids of the 807 (tube 4) are sufficiently positive for it to conduct. In the Master Programmer circuit any one of the tubes 2, 3, 4, 5, or 6 being on is sufficient to hold the second control grid potential below cut-off. Thus, the gate (tube 1) will conduct only when there is a positive signal on the first input and the five tubes (2, 3, 4, 5 and 6) are off.

The positive gate potentials which must be supplied to a gate tube for switching purposes can be obtained from the outputs of a flip-flop (see section 1.2.1.). With the proper relationship of supply voltages for the gate tube and the flip-flop one of the outputs of the flip-flop may be connected directly to one of the control grids of the gate tube. The effect obtained is that of a switch which may be opened or closed at desired times by pulses applied to the S or R inputs of the flip-flop.

As a matter of policy the grids are driven to saturation when the tubes are on and they are three to four times below cut-off when off. This means the circuits are not amplitude sensitive, that is, a considerable change in supply potentials and in tube conductance (due to aging) will not effect the reliability of operation. Furthermore, to avoid coincidence problems pulses are never used to gate other pulses; that is, at least one grid of a gate tube is always operated by a gate voltage.

1.2.4. Buffer Tubes.

Many occasions arise in which it is necessary to couple two or more circuits, say, A, B, C, etc., to another circuit, X, so that any one, say A, can operate X without affecting the others, B, C, etc. This can be done by the use of buffer tubes as illustrated on PX-1-107. If such a tube has its grid below cut-off then any change in plate potential will not cause any disturbance

in the potentials of the grid or cathode circuits. Thus, the plates of a number of such tubes (representing the circuits A, B, C, etc.) may be connected together to the input of the circuit X. If the grid of one of these buffer tubes receives a positive signal the tube will go on causing a negative input signal to circuit X. This will cause no disturbance in the grid potentials of the tubes which do not go on. On the other hand no harm is done if more than one buffer tube goes on.

A good illustration of the action of buffer tubes is given on the accumulator cross section PX-5-115. There are eight clear gate buffers (CL. G. B., tube 63) with the plates (CB_T) all connected to the grid of an inverter tube (J50 in the gate unit). If any one of these buffers begins to conduct the potential on all the plates and on the grid of J50 will fall. The only effect will be that J50 will go off. Although the grids of these clear gate buffers are directly connected to the gate tubes 68 in the transceivers, these gates are not disturbed in the other seven transceivers.

1.2.5. Cathode Followers.

A cathode follower is illustrated on PX-1-107. The input of this tube is connected to the plate of an inverter tube which is normally on. This holds the grid potential of the cathode follower below cut-off. If a signal turns this inverter tube off the grid will rise to about 50 volts and the cathode follower will begin to conduct. As the tube goes on the cathode will rise in potential giving a positive output. This rise in potential is limited by the grid potential.

Thus, in the case of a cathode follower a positive input gives a positive output.

1.2.6. Inverter Tubes

If a positive pulse or gate, rather than a negative one, is required (in order to operate another gate tube, for example), then an additional tube must be inserted in the circuit. This tube is known as an "inverter". It is

normally conducting, and when a negative potential is applied to its grid, so as to bias it to cut-off, a positive change in plate potential takes place. This may then be used to operate other tubes, normally non-conducting in the desired way.

The role of a gate tube is that of the logical "and" while a buffer is similar to a logical "or". Arrangements of inverters such as illustrated on PX-1-106 also corresponds to the logical "and".

1.2.7. Pulse Standardizer.

It has been mentioned that in the operation of a counter it is necessary that the input pulses have a certain shape and magnitude. Distortion of pulses because of the capacitance of interconnecting circuits and because of passage through various gate tubes makes it necessary to use pulse-standardizing circuits at the counter input to secure reliable operation. The pulse standardizer circuit includes a flip-flop different from that discussed in 1.2.1. in that one of its states is only semi-stable.

After an input pulse has flipped the circuit, it will flip back to its original state in a time determined by the circuit constants and practically independent of the input pulse. (See PX-1-110).

The explanation of this action is as follows: the values of R_5, R_6, and R_7 are such that when tube T_3 is conducting, the current through R_6 biases tube T_2 to cut-off. If a negative pulse is applied to the input, T_1 goes off and tube T_2 is turned on, and the voltage at the plate of tube T_2 drops because of the current through R_4. This voltage drop is transmitted to the grid of tube T_3 through the capacitor C_1, and tube T_3 is thereby cut off. However, this negative bias is gradually lost because current then flows through R_5 to the grid and the capacitor C_1, therefore after a time which depends on the product R_3C_1, tube T_3 is no longer biased to cut-off; and as it begins to conduct, the increased current through R_6 begins to bias tube T_2 to cut-off again. This change in tube T_2 reacts on tube T_3, and the action is accelerated, flipping

the circuit back to its original state.

When used to supply properly shaped pulse to a counter this circuit includes a power output tube, T_4.

Special pulse standardizer. A diagram of the special pulse standardizer appears on PX-1-110. The diagram shows a switch on the input; actually, there are three of these circuits all located in the cycling unit (see PX-9-307). and the respective inputs come from (a) the initiating pulse switch on the front panel of the initiating unit, (b) the reset cam of the IBM punch, and (c) from the finish cam of the IBM reader.

If the switch is closed the condenser C_1 will discharge through the 4.7K resistor. The time constant for this discharging action is slightly more then 2 miliseconds. Thus, the switch should be closed for a period of at least this many miliseconds. As the condenser discharges the grids of tube T_1 drop in potential and the tube goes off.

After the switch is opened the time constant for charging is about 50 miliseconds. Therefore, if the switch were pushed again before the condenser had recharged, the tube T_1 would have not began to conduct again and there would be no output pulse the second time. The time constants here are purposely slow (compared to the speed of operation of the ENIAC) to prevent any chattering of the contacts of the switch (or other transient effects) from causing more than one pulse to be given out.

As tube T_1 goes off its plate potential rises causing tube T_2 to conduct. The flip-flop action of tubes T_2 and T_3 gives a negative pulse to the condenser C_2 causing the tube T_4 to go off. Whether T_2 remains off or not (it will remain off as long as the switch is closed) the grid of T_4 will charge up through the 180K resistors causing the tube to conduct again. The time that tube T_4 is off is, therefore, independent of the length of time that the switch makes contact. Note that releasing the switch causes T_2 to go off

giving a positive signal through the condenser to the grid of T_4. Since T_4 is already conducting this positive pulse has no effect.

1.2.8. Transmitter

PX-1-108 shows the details of a transmitter circuit. Because of the large capacitances associated with the interconnection circuits, such as digit trays, program trays, and patch cords, it is necessary to use power tubes working into relatively low load resistances in order to transmit pulses from one unit to another at the rate of 100,000 pulses per second. These pulses are positive in order to operate gate tubes and buffer tubes in the accumulators. The diagram of PX-1-108 illustrates the method of achieving this.

The output, or transmitter, tubes have a low resistance in the cathode circuit, 220 ohms. This load resistance is located in a load box and is plugged into a socket in the digit or program trunk into which the transmitter output is fed. The load resistance cannot be connected permanently to the cathodes of the transmitter tubes since depending upon the jumper connections made on the front panel several transmitter tubes may feed into the same line. Thus, just one load box must be plugged into each digit and each program trunk.

The transmitter tubes are normally off. Since the output load is essentially a large capacitance, the positive pulse can be produced quickly only by driving the grids of these output tubes positive with respect to their cathodes. In order to make the output pulse amplitude stable, the grid must be sufficiently positive so as to reach the saturation current for the tube. Considerable grid current will then flow, and it is necessary to provide another tube, known as the driver tube, capable of maintaining the required grid potential under these conditions. The driver tube is actually a smaller power tube. It is normally conducting, and is cut off by a negative pulse input to its grid.

When a signal arrives at the driving tube the grid drops from about -105 volts to approximately -165 volts. This causes the driver tube to go off raising the grid potential of the transmitter tubes. As the transmitters go on the cathode potential rises to about 45 volts.

The digit outputs of the divider and multiplier do not have standard transmitters. They have inverter tubes with built in load resistances. Thus, the lines that these tubes feed into must not have load boxes and for reliable operation the pulses should not be fed into a transmission system exceeding the loading rules stated in the operator's manual.

1.2.9. Receiver Plug-in Unit:

The wiring details of a receiver appear on the accumulator cross section (PX-5-115 while a block diagram representation of the receiver appears on PX-5-304 (accumulator block diagram). For a detail wiring diagram of a receiver plug-in unit the reader is referred to PX-5-148.

The incoming signal arrives at a buffer (tube 66) turning it on. This causes a drop in the plate potential, that is, this tube inverts the signal. The negative output of this buffer is used to set the flip-flop (64, 65 say). The positive (that is, positive after initial clearing) output of the flip-flop feeds into what is called a fast buffer output (62 and 63). This is an inverter (62) operating a cathode follower (63). The inverter is normally on. When the flip-flop is set the decrease in potential on the output turns the inverter off and the cathode follower on. This gives a positive gate on the output. The normally negative output of the flip-flop goes to a buffer tube (62) forming what is called the slow buffer output. The time constant for this output is much longer than that of the so called fast buffer output; this explains the terminology.

The negative output of the flip-flop also goes to the grid of a gate tube (61). When the flip-flop is set this gate can pass a reset signal causing the flip-flop to reset. In the case of receivers used in the accumu-

lators the other grid of this gate is connected to the central program pulse (CPP) line. Since the set signal is usually a CPP gated at some other unit of the ENIAC the receiver will start to come on at about pulse time 17 (or slightly later depending upon the time constants of the intervening path) of one addition time. At pulse time 17 of the next addition time the reset gate (the time constants are such that this does not open in time to pass a resetting CPP which would conflict with the setting program pulse) pass a CPP which resets the flip-flop. Thus, the receiver is on for one addition time. In other units (in particular, in the divider and multiplier) the reset pulse passes through other gates which allow the receiver to remain on more than one addition time.

I.2.10. Transceiver Plug-in Unit.

As with the receiver the wiring details of a transceiver appear on the accumulator cross section PX-5-115 and a block diagram representation appears on the accumulator block diagram PX-5-304. For a detailed wiring diagram of a transceiver the reader is referred to PX-5-147.

As far as the fast buffer output is concerned the transceiver is identical with a receiver. On the normally negative output of the flip-flop are two buffers (61) giving two slow buffer outputs. This line also feeds a reset gate (62). The output of the reset gate goes through an inverter (65) to two more buffer outputs (63) and to a gate (68) which passes a CPP. The CPP passed by this gate resets the flip-flop and goes through a transmitter.

The usual mode of operation is as follows. An incoming program pulse goes through a buffer (69) and sets the flip-flop. The gates provided by the fast and slow buffer outputs are used to cause the unit to perform a certain task. When the task is finished a signal arrives at the gate opened by the normally negative (now positive) output of the flip-flop. The gate passes this signal turning off an inverter giving two more output gate signals

and opening another gate to pass a CPP. This CPP resets the flip-flop and is transmitted (via cables and program trunk) to some other unit to program the next step in the computation. The delayed buffers (63) furnish gate signals which may perform the final parts of an operation such as the case of an accumulator.

1.3. BLOCK AND CROSS SECTION DIAGRAMS.

Chapters II to X are devoted to descriptions of the various units of the ENIAC. The descriptions of the units will, in general, be given in terms of block diagrams and cross section diagrams. A block diagram uses circles and rectangles to represent various electronic devices, and has the following purposes:

1) to aid in understanding the various circuits and their operation without going into details.
2) to enable people with computational problems to understand the ENIAC sufficiently (irrespective of their electronic background) so as to adapt their problems to it.
3) to assist the maintenance man in finding mechanical and electrical failures.

Cross section diagrams give typical circuits in all detail, that is, all resistors, condensers, inductances, tubes, all voltages, et cetera, are given. If a unit contains many circuits which are practically identical, only one appears on the cross section. The cross sections have the following purposes:

1) to enable the person with an electronic background to understand in detail how the ENIAC operates.
2) to assist the service man in making proper replacements of parts.

As a general practice in the following chapters, programming details (switch settings and plugging of interconnectors) will be described only to the extent required to understand the circuits. For more detailed programming and

illustrative set-ups the reader is referred to the corresponding chapter and sections of part I of this report.

As standard practice on all block diagrams the following conventions will be followed:

1) Broken lines indicate pulse carrying lines while solid lines carry gates.
2) Tubes (except for stages of rings and pulse standardizers) which are normally conducting are shaded, others not. The word "normally" here means immediately after initially clearing, or in the case of the cycling unit, the situation which exists when the ring is at stage zero and no pulse is coming from the oscillator.
3) Plug-in units will be represented by rectangles with heavy borders.

II. INITIATING UNIT

The initiating unit, as the name implies, contains the controls which start and stop (turn on and turn off the power) the ENIAC. There is a push button on the initiating unit front panel (see PX-9-302) which initially clears the ENIAC, that is, it clears all decades to their zero stage, clears PX rings to their first (P) stage, repeater rings to stage one, and program controls to their unactivated state, and so forth. The program terminals and controls for the IBM reader and punch are located on this panel. From these controls program pulses can cause the reader to read a new card, or the printer to print the numbers registered in certain accumulators and possibly some decades of the master programmer. Also there is a push button by which the reader may be caused to read a new card. When the card reading is finished and an interlock signal has arrived, a program pulse is given out from one of the terminals on the front panel (see PX-9-302, terminal R_0). The interlock signal is a program pulse indicating the ENIAC has finished some other sequence of computations which was going on simultaneously with the card reading. In manual operation, by the push button, no interlock signal is needed. Likewise, when the printer relays have set at the beginning of the card punching cycle a program pulse is obtained from a terminal on the front panel (terminal P_0). These pulses can be carried over lines of a program trunk to some other unit of the ENIAC, causing some other operation to take place. There is another push button which produces what is called an initiating pulse (at terminal I_0) that can be used similarly to the reader and printer program output pulses. There are six

program input and output terminals (C_1 and C_o on PX-9-302) associated with six transceivers which transmit the selective clear gate over the cycling unit trunk. This selective clear gate (SCG) goes to each of the twenty accumulators and causes those which are so set (set to selective clear) to clear. There is another push button which shunts out the door switches and allows the ENIAC to be operated with the doors of some of the units off, this is called the door switch shunt.

2.1 STARTING AND STOPPING SEQUENCE AND INITIAL CLEAR

The following descriptions will be given in terms of diagrams PX-1-101 (Power and control wiring for the ENIAC) and PX-9-307 (Cycling unit and initiating unit block diagram). The right hand portion of PX-9-307 shows the circuits located either in the initiating unit or on the switching and fuse panels. The left hand portion shows the circuits of the cycling unit.

2.1.1 Normal Initial Conditions

The normal state with the ENIAC turned off is to have relays C and H (see the simplified control circuits on upper right corner of PX-1-101 or see the lower right hand corner of PX-9-307) activated.

In series with relay C are 46 door switches (shunted out by the door switch shunt - see PX-9-302), and 43 thermostats. If any one of these 89 contacts is open then relay C will be unactivated, and, as explained below, this makes it impossible to turn the ENIAC on. The thermostats are located in the tops of the various units which contain vacuum tubes. If the temperature of any one of these units rises above 115° the corresponding thermostat contact will open and turn the ENIAC

off or prevent it from being turned on (until the unit cools down). When the doors are off of the backs of the various units a person is exposed to voltage differences amounting to as much as 1500 volts. Each such door operates a door switch which will cause relay C to drop out (unless the door switch shunt is operated)

When relay C_1 drops out the P timer starts (this timer may be set to run from 0 to 15 minutes before it closes its contact P_1). During the period that the timer is running, a bell will ring to indicate that this timer is about to turn the ENIAC off (if it has been turned on). This turning off is accomplished by opening contact P_1 which opens the holding circuit of the auxiliary relay A. This in turn causes all the contactors and certain auxiliary relays to drop out shuting off all power (dc and heater) to the ENIAC.

Thus, if a thermostat opens the circuit, or if the back cover is removed opening a door switch (when the door switch shunt is not operated) the P timer starts, a bell rings, and at the end of the period (0 to 15 minutes), all power is shut off from the ENIAC. This time interval gives the operator time to perhaps correct the fault (for example, check the ventilation system) before the power goes off. This system is designed to minimize the number of times the heaters are turned off and on since this turning off and on has been found to cause numerous tube failures (burned out heaters and heater-cathode shorts).

The relay K has in series with it the power supply heater phase failure relays (3 relays), the power supply phase failure relays (3 relays), and the under voltage release relays (28 relays). All these contacts are open when the power is off, thus, a contact on relay K (contact K_2) shunts these circuits until relay K is activated. Since relay K is not activated

until a minute and ten seconds after the start button is operated or ten seconds after the d-c power comes on, this allows the under voltage release relays and the phase failure relays to pick up. In other words, there is no undervoltage or phase failure protection during this ten second interval. If there is an undervoltage (because of failure in some power supply) or a phase failure, then one of these relays will drop out (or not be picked up when the machine is started) and the relay N will drop out when relay X is activated. As explained below this will shut off the plate supply to the power supplies, and consequently turns off the d-c to the EMLC. This leaves all the heater voltages on but turns off the d-c.

2.1.2 Complete Starting Sequence

(1) Push start push button (on initiating unit front panel, PX-9-302).

Relay A is activated (assuming relay C is activated).

Contactor B is activated by a contact on relay A. This turns on the EMLC heaters picking up the heater phase failure relays (6 relays). Relay A is now held by contacts P_1 and B_1. Contactor B is held by contacts A_1 and B_1.

The start pilot (amber light on initiating unit front panel) and the power supply time recorder (on initiating unit front panel, tells total time that the power supply heaters have been on) are turned on by contact A_4 on relay A. If any d-c fuses are blown then a circuit through contact A_4 and a contact on one of the d-c fuse relays causes relay L to pick up. This would prevent the d-c power from being turned on by preventing contactor G from being activated. If any of the power supply

filament fuses are blown the relay Q will pick up and hold on contact Q_2.

Contactor E is picked up by contact A_3 on relay A. This supplies power to the fans in the ventilating system.

Contactor D is picked up by contact E_1 on contactor E (assuming that relay Q is inactivated). This furnished power to the power supply heaters.

The one-minute timer F is started by a contact D_1 on contactor D provided heater phase failure relays have picked up. This timer runs for one minute and then the contact labelled F_1 is closed. This contact remains closed as long as power is applied to the timer, that is, as long as contactor D is activated. Whenever power is removed the contacts open and the timer resets itself.

After one minute the power supply contactor G is picked up by the timer contact F_1 (assuming relay L is not activated). This contact furnishes power to the plates of the rectifiers in the power supply and thus furnishes d-c power to the EDLAC.

Relays H and I and the ten second timer J are picked up by contact G_1 on contactor G. The initial clear relay No. 1 (H) operates certain relays in the initiating unit which produce the initial clear gate (ICG) (see Section 2.1.2). The 14 undervoltage release pick-up relays shunt the resistances in series with the coils of the undervoltage release relays. Since the drop-out point for a relay is considerably below the pick-up point the resistances in series with the coils are adjusted so that a small drop in voltage from one of the power supplies will cause the relay to drop out and thus shut off the d-c power (by releasing relay H which picks up relay L). The pick-up point is then too

high for these relays to be picked up by the voltage from the power supplies. Thus, for a period of ten seconds (during the running of the ten second timer) the relays E cause these resistances to be shunted with smaller resistances to enable the relays to pick-up.

Ten seconds later the contact J_1 closes on the ten second timer. This causes relay K to pick up. Relay K holds on a circuit through contacts G_1, K_1, and the initial clear push button. When relay K is activated, contact K_4 opens, releasing relays E and E, and allowing the timer J to reset. Contact K_2 opens applying the phase failure and under voltage protection (since relay E is also released). Contact K_3 closes turning on the ready pilot (green light on initiating unit panel).

The green light indicates that the power is on and that the ENIAC has been initially cleared (as described in Section 2.1.2) and is ready to start computations.

2.1.3 The d-c off Sequence

Push the d-c stop button. This causes relay L to be activated. Relay L remains activated by circuit through d-c start button and holding contact L_2. Contact L_1 opens dropping contactor C. This shuts off the plate supply to the power supply and thus shuts off the d-c to the ENIAC. Contact G_1 opens dropping relay K (this puts the initial clear circuits into their normal initial state).

If a d-c fuse blows, one of the d-c fuse relays will pick up. This will activate relay L and have the same effect as pushing the d-c stop button. If the voltage from any one of the various power supplies is subnormal, one of the undervoltage release relays will drop out. If there is a phase failure in the voltage to either the ENIAC heaters or to

the power supply heaters or plates one of the phase failure relays will drop out. In any of these last cases relay N will drop out closing the contact N_1. This, again, has the same effect as pushing the d-c stop button.

Frequent turning off and on of the heaters of the tubes is undesirable because this tends to increase the number of heater failures. Thus, the d-c on and off circuits are provided so that the heaters may be left on continuously while the d-c can be turned off when the machine is not in use or when parts must be replaced.

A locking arrangement is provided so that personnel may padlock the d-c start and stop buttons and prevent anyone from turning on the d-c while someone is working on the machine.

Should one of the power supply heater fuses blow, one of the three power supply heater fuse relays will operate. This will pick up relay Q, which by opening the contact Q_1, will turn off all power to the power supply. (Contactor D will be deactivated removing heater power. Timer contact F will open since contact D_1 has opened deenergizing timer F, and hence the plate supply through contactor G will also be turned off). With power supply heaters deenergized it is safe to replace a heater alarm fuse, although it is recommended that additional precaution be taken by opening safety disconnect switch which has been provided. If the safety disconnect switch is used, it must be again closed before attempting to turn on the d-c power.

2.1.4 The d-c on Sequence

Push the d-c start button. This causes relay L to drop out. The d-c contactor G is picked up by a circuit through contacts F_1 and L_1.

The rest of the sequence is exactly like the last part of the sequence described above (see Section 2.1.2).

If the power supply a-c and d-c has been turned off from a heater fuse failure, pushing the d-c start button will turn it on since relay Q will be released permitting contactor D to pick-up through Q_1. The rest of the sequence is exactly like the last part of the sequence described above (Section 2.1.2). It should be noted that when relay Q trips off the d-c, an extra one minute (over a relay L tripping) will elapse between the pushing of the d-c start button and the initially cleared signal since timer F is now introducing tube warm-up delay.

2.1.5 The Initial Clear

Near the end of the starting sequence (see Section 2.1.2) relay H is activated during the period that the ten second timer J is running. Thus, for a period of ten seconds initial clear relay No. 3 (in the initiating unit) is activated by a circuit through contact H_1. This changes the potential on the screens of certain gates in the master programmer from +150 volts to zero volts (this is called the master programmer clear - MPC). This change in potential prevents the corresponding gates from conducting and, thus, during this ten second period no program pulses are transmitted from the master programmer. For a more complete description of this situation see Section 10.3.2.

Another contact on initial clear relay No. 3 opens allowing a 125 mf. condenser to charge up during the ten second interval. At the end of the ten second interval relay K is picked up by the contact J_1. Contact K_4 opens dropping relays H and K and allowing the ten second timer J to reset. As H drops initial clear relay number three drops

changing the bias on the screens of the gates in the master programmer (MPC) back to +150 volts. Another contact on this relay closes allowing the 125 mf. condenser to discharge through the coil of initial clear relay No. 4. This relay is activated for a period of about one second and changes the potential on the initial clear line from -345 volts to -290 volts. This produces the initial clear gate (ICG). This initial clear line goes around to the various units by way of the d-c wiring channel.

The initial clear circuits work automatically at the end of a starting sequence or with a d-c on sequence. The initial clear sequence also takes place when the initial clear push button is operated (on front panel of the initiating unit, see PX-9-302).

There follows a list of things which take place in the various units during the process of initially clearing.

(1) Initiating Unit (See PX-9-307).

The initial clear gate (ICG) three gates which pass central program pulses (CPP) which reset the reader and printer start flip-flops (65, 66, and 68, 69 on PX-9-104) and the reader interlock, reader finish, and the reader synchronizing flip-flops (67, 68 and 70, 71 on PX-9-103 and 63, 64 on PX-9-106). (See sections 8.2 and 9.1.2.)

(2) Cycling Unit (PX-9-307).

The initial clear gate is not used in the cycling unit.

(3) Accumulator (PX-5-304).

The ICG gates central program pulses which cause the decades and the PX counter to clear back to their first stages (or possibly some decade may clear to five for round-off purposes) and the repeater ring

(associated with the transceivers) to clear back to stage one. (See Sections 4.2.3 and 4.1.2.)

(4) High Speed Multiplier (PX-8-308).

Here the ICG gates central program pulses which step the program ring to stage one (see Section 5.3) and which reset the l and r receivers (which control the product accumulators in the process of receiving the partial products).

(5) Divider and Square Rooter (PX-10-304).

The ICG gates central program pulses producing C1 and C1' pulses which perform the clearing actions as described in Section 6.2.9. Actually these pulses clear the program ring, the quotient place ring, and the numerator binary ring, and reset numerous flip-flops.

(6) Function Table (PX-7-304).

The ICG gates central program pulses which clear the argument rings, the program ring and resets certain flip-flops (see Section 7.4.4).

(7) Constant Transmitter (PX-11-307).

The ICG is used only in the reader control circuits which are located in the initiating unit, see (1) above.

(8) Printer (PX-12-307).

The ICG is used only in the IBM punch control circuits which are located in the initiating unit, see (1) above.

(9) Master Programmer (PX-8-304)

The ICG gates central program pulses which clear the decade rings and the stepper rings (see Sections 10.2.1 and 10.3.1).

If any program pulses get started in the trays and jumpers which extend around the machine (they might get started when the d-c

power comes since certain flip-flops may come on in the set or abnormal position) they will run out any sequence which an operator has plugged in. However, if any of these sequences pass through the master programmer the pulses will not pass here during the initial clear period (because the master programmer clear (MPC) blocks the program output gates, see Section 10.3.2. The period during which the initial clear is on is ample (including a safety factor) for any manually plugged sequences to run out (assuming that no one has plugged in any complete cycles of programs which do not pass through the master programmer). Then, after the initial clear sequence is completed (and the ready pilot goes on) the machine is ready to start any sequence of computations which may be programmed.

2.2 INITIATING PULSE PROGRAM CONTROL

The initiating pulse plug-in unit is activated by a push button and produces a program pulse which is synchronized with the ENIAC. This pulse appears at a terminal I_o on the front panel (PX-9-302) and can be carried around the program trunk system to any unit of the ENIAC.

This unit is pictured in the upper right hand corner of PX-9-307. Closing the initiating pulse push button causes the special pulse standardizer (tubes 61 and 62) to set the flip-flop (64 and 65). This opens the gate 66 which passes a central program pulse (coming from the cycling trunk) setting flip-flop 67 and 68. This flip-flop opens gate 69 passing a CPP which resets both flip-flops and goes through the transmitter to the output terminal I_o (see PX-9-302) on the front panel.

The two flip-flops operating as described above always provide a standard output program pulse. Gate 66 may open in such a way that only part of a CPP is passed. If it fails to operate flip-flop 67 and 68 no harm is done since flip-flop 64 and 65 is not reset and the next CPP is passed full strength by gate 66. Then the flip-flop 67 and 68 has one full addition time in which to set up so gate 69 is open and passes a standard program pulse. This pulse then resets the flip-flops and is transmitted.

There is no cross section diagram of this circuit. Clearly, since there is no parallelism of circuits in this unit, a cross section must be as detailed as the actual wiring diagram of the circuit. The number PX-9-105 in the corner of the drawing of the plug-in unit refers to the wiring diagram.

2.3 OTHER FEATURES

2.3.1 Selective Clear Controls

There are six transceivers located in the initiating unit with program input and output terminals on the front panel. The output of the cathode followers of the respective transceivers is connected to a line of the cycling trunk and provides the selective clear gate (SCG). This gate is used to clear any of the twenty accumulators depending upon the settings of their selective clear switches (see Section 4.2.3).

Thus, whenever a program pulse enters one of the terminals C_i the selective clear gate is provided for a period of one addition time and a program pulse is transmitted out of the terminal C_o at the end of the addition time. These transceivers are reset by a CPP after one addi-

tion time. A more detailed block diagram representation of a transceiver appears on PL-5-304.

2.3.2 Reader and Printer Program Controls

Control circuits for the IBM reader and the IBM going punch are located on plug-in units (see the four plug-in units below the initiating pulse plug-in unit on PL-9-307) located in the initiating unit.

These circuits are described in detail in the discussion of the constant transmitter (Chapter VIII) and of the printer (Chapter IX).

2.4 TESTING FEATURES

On the front panel of the initiating unit there appears a hum oscilloscope, an a-c voltmeter, and a d-c voltmeter. These are used to check the amount of hum on the a-c power lines supplying the SILAC, the voltages on the three phase lines supply the a-c power, and the d-c voltages put out by the power supply. Two switches enable the operator to check every d-c voltage used in the machine. A table of proper values and tolerances appears on this panel.

For a complete discussion of testing procedures, et cetera, the reader is referred to the maintenance manual (part III of this report).

III. CYCLING UNIT

The cycling unit produces the pulses which are used to represent digits and to control the operation of units of the ENIAC. Also the carry-clear gate (CCG) is produced in the cycling unit. The pulses produced in the cycling unit control the timing of the operations and enables the various units to operate in synchronism.

The following table gives a list of the pulses or gates produced in the cycling unit. Also appearing in the table is the principle purpose of each pulse or gate.

TABLE 3-1

Pulse or gate	Abbreviation	Purpose
Central Program pulse	CPP	A program pulse used to control the activity of the various units of the ENIAC.
Tens pulses (off beat)	10P	Used to cycle the decades of the accumulator during the process of transmission of the number (or its complement) registered in the accumulator.
One pulse	1P	A coded system in the multiplier, function tables, and the constant transmitter makes use of combinations of these pulses to represent the digits zero to nine.
Two pulses	2P	
Two-primed pulses	2''P	
Four pulses	4P	
Nine Pulses	9P	Some of these pulses are used to represent the digits zero to nine.
One-primed pulse	1'P	In the process of taking the complement this pulse is used to obtain the complement with respect to 10^n instead of 10^n-1.
Reset pulse	RP	This pulse is used to reset flip-flops in the accumulator decade units and to provide a carry-over pulse in the process of addition.
Carry-clear gate	CCG	This gate controls the carry over process when adding in an accumulator and produces the clearing action when so desired.

The pulses and gates listed in the table above are produced in the cycling unit once each addition time. PX-9-306 shows the temporal order of these pulses and gates. These pulses and gates along with the selective clear gate from the initiating unit (see 2.3.1.) are distributed around to each unit of the EDVAC by the cycling trunk.

An addition time is normally 200 micro-seconds long. Each addition time is divided into twenty parts called pulse times, each ten micro-seconds long. All of the pulses except the 10P are produced at the beginning of a pulse time and all have a duration of about two micro-seconds. The tens pulses (10P) pass through a 2.5 micro-second delay line and thus arrive at the beginning of the second quarter of a pulse time. The tens pulses, 10P, are used to cycle decades in the accumulators (see 4.3.) during the process of transmitting the contents of the accumulator. These off-beat pulses are produced 2.5 micro-seconds late for timing reasons which will be explained in the chapter on the accumulator (see 4.3.1.).

3.0. INTRODUCTION

The block diagram of the cycling unit along with that of the initiating unit appears on PX-9-307. In the upper left corner is the oscillator plug-in unit. To the right of this are the relays which determine the mode of operation: continuous, one addition time, or one pulse time. Below the oscillator plug-in unit are two more plug-in units containing pulse standardizers and delay lines. Near the middle is the twenty stage ring which counts out the pulse times of an addition time. Below the ring are pulse gates, then the amplifiers, and finally the transmitter plug-in units. The outputs of the transmitter plug-in

units go to the cycling unit trunk which carries the various pulses and gates around to each unit of the ENIAC.

3.1. THE OSCILLATOR AND PULSE FORMERS.

3.1.1. The Oscillator

The crystal oscillator always oscillates at a frequency of 100 kilocycles. Whether or not the output of the oscillator is used depends upon the setting of the external oscillator switch and the continuous and one addition time relays. The socket and the external oscillator switch makes it possible to operate the ENIAC with an external oscillator, and, more important, to operate the ENIAC at different frequencies for purposes of checking (for example, to check safety factors).

Note: If the ENIAC is operated at a frequency exceeding 100 kilocycles the safety factors may be lost and reliable operation cannot be expected.

The continuous and one addition time relays cause the oscillator (external or internal) to be connected through the pulse standardizer K-L 26 to the gates L27 and L28 for continuous and one addition time but not for one pulse time operation. Of the three modes of operation the first (continuous) is the normal mode and the following description will be in terms of this mode. The other two modes (one addition time and one pulse time) are for purposes of checking and will be described in section 3.3.

When the continuous relay is activated the cathode circuit of tube 70 is opened, thus turning tube (70) off and, therefore, opening gate L28. That is, since tube 70 is not conducting the plate potential is relatively high, and, therefore, one of the control grids of the gate L28 is sufficiently high

that any positive signal on the other grid will cause it to conduct. Hence, the output of the oscillator goes through the contacts on the continuous relay to the pulse standardizer K-L 26 and through the gate L 28 to the on-beat plug-in unit.

The pulse forming circuit, composed of a special pulse standardizer (tubes 68, and 69, see section 1.2.7.) and tube 70, serves no other purpose than that described above in continuous operation. Its role in one addition time and one pulse time operation will be described in 3.3.

3.1.3. The on-beat plug-in unit

Tubes 61, 62, 63 of the on-beat unit constitute a pulse standardizer. This circuit differs from the usual pulse standardizer in that it has a one micro-second delay line on the plate supply of tube 62. By reflection this delay line helps to produce a square pulse with a length of two micro-seconds.

The output of tube 63 goes to tubes 68 and 67 and thence to a socket located underneath the front panel. Thus, pulses (which are in phase with the nine pulses 9P) arrive at this terminal in the following ways:

a) for continuous operation one pulse each pulse time,

b) for one addition time operation twenty pulses (one each pulse time) each time the push button is operated, and

c) for one pulse time operation one pulse each time the push button is operated.

The output of tube 63 also goes to tubes 65, 64, and 66 and on to the pulse gates controlled by the ring. These pulses are gated by the ring to produce all pulses sent out by the cycling unit except the tens pulses (10P).

The third output of tube 63 goes to the off-beat pulse former plug-in unit and enters a 2.5 micro-second delay line.

3.1.4. The off-beat plug-in unit

From a center tap on the 2.5 second delay line pulses go through a pulse standardizer (tubes 67, 68, 69, and 70) and thence to step the ring. This pulse standardizer is similar to the usual pulse standardizer (used in accumulators) except that it has two driving tubes (67 and 68) operating in parallel.

The end output of the delay line goes through another pulse standardizer to the tens pulses gate L30. This pulse standardizer also has a one micro-second delay line to obtain square pulses of 2 micro-second length.

The pulses which step the ring arrive 1.25 micro-seconds after those that go to the pulse gates which are opened and closed by the stages of the ring. This means that the ring has 8.75 micro-seconds in which to step from one stage to the next, and for reliable operation the ring is designed to step to the next position in appreciably less time than this.

3.2. THE RING AND ITS ASSOCIATED GATES AND FLIP-FLOPS

3.2.1. The tens pulses (10P)

When the ring is on stage 0 gate K27 is open. Thus the first pulse of the addition time passes K27 and sets the flip-flop L29. This flip-flop must open gate L30 inside of 2.5 micro-seconds in order to pass the first of the tens pulses arriving from tube 61 in the off-beat pulse former. Thus, this is not a standard flip-flop; that is, the triggering tubes are omitted in order to improve the time constant. Also, the output time constant is less than for a standard flip-flop.

The output of gate K27 also goes to trigger the scope which is

located on the cycling unit. This gives one addition time sweeps on the scope.

The flip-flop L29 remains set until the ring reaches stage ten. At that time the output of gate A30 resets the flip-flop. Note that in order to not pass more than ten pulses the flip-flop must reset in less than 2.5 micro-seconds.

The output of L30 goes to a two stage amplifier (L41 to L46) and thence to two transmitter plug-in units. A transmitter consists of two stages with five tubes operating in parallel in each stage.

3.2.2. The 1, 2, 2', 4 and 9 pulses.

The one pulse (1P)

When the ring is at stage one gate K30 is opened to pass a one pulse. The pulse goes through an amplifier system (K41, K42, K43, K44, K46, and K47) to a transmitter plug-in unit.

The two pulses (2P).

Stages two and three of the ring open gates J30 and H30 to pass pulses to form the two pulses. After being preamplified by J41, J42, H41, and H42 they are combined and further amplified by J43, J44, J46, and J47, and then fed to a transmitter plug-in unit.

The two-primed pulses (2'P)

Stages four and five open gates G30 and F30 which pass pulses to make up the two-primed pulses. As with the two pulses these are amplified and taken to a transmitter plug-in unit.

The four pulses (4P).

Stages six, seven, eight, and nine open gates E30, D30, C30, and B30 to pass pulses which make up the four pulses. These are amplified and taken to a transmitter plug-in unit.

The nine pulses (9P)

The one, two, two-primed, and four pulses are taken to buffers K45, J45, G45, and E45 and then combined to make up the nine pulses. Then they pass through a two stage (six tubes in parallel) amplifier (A 24 and 25 to F24 and 25) and then to four transmitter plug-in units.

3.2.3. The one-primed pulse (1'P).

Stage ten opens two gates A30 and A27. Gate A30 passes a pulse which resets the tens pulse flip-flop. Gate A27 passes the one-primed pulse through amplifiers A26, B26, A23 to E23 and F23 to K23 and then to three transmitter plug-in units.

3.2.4. The carry clear gate (CCG)

Stage eleven of the ring opens gate B27. This gate passes a pulse which sets the flip-flop E27. The negative output of the flip-flop goes through amplifier tubes D26 and D27 to a transmitter plug-in unit. When this flip-flop is set this output takes a positive swing and the transmitter gives a positive gate on its output. Note that this amplifier system is direct coupled all the way through. The carry-clear flip-flop is reset when the ring r reaches stage eighteen. The length of this carry-clear gate (70 micro-seconds) is about 1 3/4 times that needed for carry over in a twenty decade accumulator, that is, when the carry over takes place there may be a string of carry overs from the first decade down to the twentieth. This gives a seven to four safety factor which is somewhat less than the two to one which is attained in most parts of the ENIAC.

The nine pulses (9P)

The one, two, two-primed, and four pulses are taken to buffers H45, J45, G45, and K45 and then combined to make up the nine pulses. Then they pass through a two stage (six tubes in parallel) amplifier (A 24 and 25 to F24 and 25) and then to four transmitter plug-in units.

3.2.3. The one-primed pulse (1'P).

Stage ten opens two gates A30 and A27. Gate A30 passes a pulse which resets the tens pulse flip-flop. Gate A27 passes the one-primed pulse through amplifiers A26, B26, A23 to E23 and F23 to K23 and then to three transmitter plug-in units.

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3.2.5. The reset pulse (RP)

Stages 12, 14, 15, and 16 of the ring do not operate any gates. Stage 13 opens gate C27 and passes a reset pulse. Stage 19 opens gate J27 which also passes a reset pulse. Thus, in each addition time there are two reset pulses, one when the ring is at stage 13 and another when it is at stage 19. The output of the gates C27 and J27 goes to an amplifier system E26, G26, G to J 24 and 25. The output of this amplifier goes to three transmitter plug-in units.

3.2.6. The central program pulse (CPP)

Stage 17 opens gate G27 which passes the central program pulse. Since this pulse is used more places by far than any other pulse in the ENIAC it goes through the largest amplifier system. This pulse goes through tubes F27, F26 and E26, then to a two stage (ten tubes in parallel) amplifier (A22 to K22 and A21 to K21). The output now goes to nine transmitter plug-in units which constitutes a two stage amplifier with forty-five tubes in parallel in each stage.

3.3. ONE PULSE AND ONE ADDITION TIME OPERATION

These two modes of operation are provided for purposes of checking the operation of the ENIAC and to check the set-up of the problem. If the answer to a check problem is not correct then it becomes a matter of isolating the fault. This generally can be done by operation in the one addition time mode. Then, operation in the one pulse time mode will generally further help to diagnose the fault. For further discussion on these points see part I of this report.

3.3.1. One addition time operation

In this case the transfer contact on the continuous relay holds the cathode of tube 70 (in the oscillator unit) at -40 volts. This tube is normally on and will go off only upon receiving a negative signal from tube 69 which gets its stimulus from the push button.

The length of this pulse sent to gate L28 must be long enough to be sure to let a pulse from the oscillator through (at least ten microseconds). This first pulse which passes gate L28 steps the ring from stage zero to stage one. Since one of the control grids of gate L27 is connected to the negative static output of stage zero, gate L27 is opened as long as the ring is not at stage zero. Thus, the pulses from the oscillator (via K-L 26) continue to step the ring until it reaches stage zero again. Hence, each time the one pulse or one addition time switch is pushed the ring cycles through all twenty stages and the cycling unit gives out the various combinations of pulses which represent one addition time. Note that the pulse sent to gate L28 by 70 must not last as much as one addition time or else operating the one addition time push button may cause the ring to cycle twice.

3.3.2. One pulse time operation.

In this case neither the continuous relay nor the one addition time relay are activated. This means that the oscillator output is not connected at all. The output of the first triode of 70 goes both to the second triode and to gate L28. The output of the second triode goes through contacts on the one addition time relay and the continuous relay to the pulse standardizer K-L26 and through the gate L28. Thus, each time the push button is operated one pulse is fed into the on beat plug-in unit.

The wide pulse from tube 70 which is applied to gate L28 is delayed (because of the time constants of the path through the relay and the pulse standardizer) and differentiated (narrowed) by the pulse standardizer circuit. This assures its being gated at L28 by the wide pulse from tube 70 on the other control grid.

IV. ACCUMULATOR.

An accumulator is a unit of the ENIAC which is capable of performing the following operations:

1) Storing a ten digit number along with the proper indication of its sign.
2) Receiving numbers (positive or negative) from other units of the ENIAC and adding them to numbers already stored, properly indicating the sign of the sum.
3) Rounding off its contents to a previously determined number of places.
4) Transmitting the number held, or its complement with respect to 10^{10}, without losing its contents (this makes it possible to add and/or subtract from the contents of one accumulator those of another).
5) Clear its contents to zero (except for a possible round off five, see 4.2.3.).
6) Information stored in certain accumulators may be transmitted statically to certain other units (see Section 1.1.4.)

The registering of ten digit numbers is accomplished by the use of decade ring counters (See 1.2.2.) and a PM (plus-minus) counter. The circuits which carry the various groups of pulses representing numbers and signs (including the decade plug-in units and the PM-Clear plug-in unit except for the clear tubes) will be called the numerical circuits. The accumulator contains common programming circuits which in each operation of the accumulator determine which of the above listed operations the unit performs. The accumulator contains a number of program control circuits (eight repeat program control circuits and four non-repeat program control circuits) which can be used at various times to cause the common programming circuits to make the

accumulator perform one of the above operations.

Thus, usually each program control circuit will be used at most once in each sequence of computations whereas portions of the common programming circuits are used each time the accumulator performs an operation. No two program controls are used simultaneously. Actually by making use of the master programmer it is possible to use one program control circuit several times in a given sequence of computations. The operation performed by the numerical circuits (controlled by the common programming circuits) is determined by the various switch settings of the particular program control used.

When activated by an incoming program pulse (arriving via jumper connections from program trays to the accumulator front panel) the program control circuit provides certain gates to the common programming circuits which in turn supply certain gates or pulses to the numerical circuits and thus cause the accumulator to perform a certain operation. At the end of the operation (which may last as many as nine addition times if a repeat program control circuit is used) the program control circuit gives out a program pulse which may be taken to other units of the ENIAC causing them to perform the next step in the sequence of computations.

4.0. INTRODUCTION.

This description of an accumulator will be given in terms of the block diagram PX-5-304 and the cross-section diagram PX-5-115. In the upper center and upper right of the block diagram there are eleven rectangles representing the ten decade plug-in units and the PM-clear unit (on the left). Just to the left of the PM-clear unit are seen the five decks of the significant figure switch. In the lower left hand corner are seen one receiver plug-in unit and two transceiver plug-in units. As indicated on the drawing there is one other receiver plug-in unit and six other transceivers making a total of four receivers located on two plug-in units and eight transceivers

each located on a separate plug-in unit. Just above the code block and below the decade units are the α, β, γ, δ, and ε input gates of which only α and ε are shown in detail.

As indicated above, the circuits of an accumulator are divided into three groups for purposes of explanation. First, there are the program control circuits which comprise the circuits of the receiver and transceiver plug-in units, their associated switching circuits, and the repeater plug-in unit. Second, the common programming circuits connect by means of interconnection plugs (see, for example, the terminals marked ST 6, 7, and 8 on the left edge of PX-5-304) to the program control circuits. Third and last, there are the numerical circuits which extend from the input plugs SV_1, ..., SV_5 through the decades and PM unit to the output plugs SW_1 and SW_2 (at the top of the block diagram). The common programming circuits directly control the numerical circuits by opening certain gates and in some cases introducing certain pulses into the numerical circuits. The following table summarizes the gates and pulses produced by the program control circuits and by the common programming circuits.

TABLE 4-1.

Program Control Circuits				Common Programming Circuits	
Switch settings			Gates provided at	Gates Provided	Pulses Provided
Operation Switch	Clear Switch	Repeat Switch			
α	0	—	SU 1	Carry gate to tubes 19 and 20 in the decades and α input gates opened.	None
β	C	—	SU 2	Carry gate as above and β input gates opened.	
			SU 10	Gates E49 and E50 opened.	1' pulse added in first decade
A	0	1	SU 6	Gates H47 and J49 opened.	Tens pulses to cycle decades and Nines pulses for transmission over add output SW_1
AS	0	—	SU 7	Gates G47, G49, H49, and M41 opened.	Tens pulses to cycle decades, Nine pulses for transmission over add output and subtract output, and One-primed pulse for transmission over SW_2
S	0	—	SU 8	Gates F47, F49, and M42 opened.	Tens pulses to cycle decades, Nines pulses for transmission over subtract output, and One-primed pulse for transmission over SW_2
A	C	—	SU 6	Same as for A above	Same as for A above
			SU 9	Opens M44 passing CCG to clear tubes in the PM-Clear unit.	

4.1. THE PROGRAM CONTROL CIRCUITS

4.1.1. General description of a non-repeat program control circuit

Suppose that a program pulse arrives over the input terminal 11 (lower left corner of PX-5-304). This positive pulse will cause one half of 66 (tube 66 is a 6SN7, a double triode tube) to become conducting. The drop in plate voltage will send a negative pulse into the flip-flop[1] causing it to be set. The indicated polarity of the output will then be reversed and half of 62 will go off (become non-conducting), causing the cathode follower[1] 63 to go on. The output of 63 comes from the cathode; therefore, when the tube becomes conducting the cathode potential rises with respect to that of the plate giving a positive gate voltage on the output. This output goes to deck 3 of the operation switch. If the operation switch is set at α, β, γ, δ, or ε this positive gate voltage appears on the interconnection terminals labeled SU 1 to 5. If the switch is set at A, AD, or S then the gate appears on SU 6, 7, or 8. The fast output (cathode follower) is used there since these circuits must be set up before the 10 pulses arrive. The other output of the receiver flip-flop (which is positive after being set) opens the gate 61 (that is, allows a pulse on the first grid to cause the tube to conduct) and turns the buffer 62 on. This gives a negative voltage swing on the output which goes through the clear-correct switch and deck 2 of the operation switch. If the switch is set at α to ε, this signal appears on terminal SU 10 and will cause the correction to take place. If set at 0, A, AS, or S the signal turns the inverter F50 off and the buffer (the other half of F50) on, giving a negative gate at SU 9 and will cause the accumulator to clear. After the gate 61 in the receiver is opened, the CPP (Central Program Pulse) arriving at the end of the addition time resets the flip-flop. The time constants are such that

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1) For a detailed discussion of flip-flops, gate tubes, buffers, and inverters see Section 1.2.

gate 61 does not open in time to cause any conflict with the CPP which activates the receiver.

4.1.2. General description of a repeat program control circuit

Now, suppose a program pulse arrives at a transceiver, say at input terminal 5i. As in the receiver this pulse sets the flip-flop and within 15 μs.[1] gives the positive gate through deck 3 of the operation switch to the interconnection terminals SU 1 to 5 or SU 6, 7, or 8. The other output (which is now positive) of the flip-flop turns the buffer tubes 61 on and opens the gate tube 62. If the clear switch is setting on clear, the negative gate output of tubes 61 goes through two decks of the operation switch and appears at SU 9 and at SU 10. The two tubes F50 are in the line from the receivers to raise the circuit to the d-c voltage level of outputs of the transceivers. The cross section of the receiver and transceiver (see PX-5-115) shows that the plate supply of the buffer 62 in the receiver is -345 whereas the plate supply of the buffer 61 in the transceiver is -235 volts. The negative gate from the right hand buffer 61 in the transceiver will turn the inverter J50 off giving a positive swing to one of the grids of the gate tube H50. The central program pulses (CPP) arriving at tube H50 will now be passed on into the repeater ring. (The CPP that stimulated the program control will not be passed). They go through the pulse standardizer (tubes 61, 62, and 63) and step the ring. If the repeat switch is set at 3 (as illustrated), then at the third addition time the ring will have stepped to stage three giving a positive gate through the repeat switch to the gate tube 62 in the transceiver. Note, that one repeater ring is used

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1) This follows the practice that circuits are designed to operate in not more than half of the time which would suffice, for example, the 10 pulse gates (F-4, 47, connected to SU 6, 7, and 8) must be open inside of 32 μs. (After CPP sets receiver or transceiver) in order to pass the first ten pulse. Actually, the time constant for these circuits depend upon the setting of the program switches. The maximum time constant occurs on a circuit when two accumulators are interconnected to form a twenty digit accumulator and all program switches are set to activate that circuit.

by all the repeat program controls. This causes the inverter 65 to go off opening the gate 68 and turning the buffers 63 on. The output from one of the buffers 63 goes through the clear switch and the operation switch giving a negative gate at S' 9. The output of the other buffer 63 turns the tube J50 off opening the gate K50 (this process of opening gate K50 takes about 100 μs.) The IPP at the end of the third addition time passes this gate and turns the inverter K49 off (it over-rides the stepping pulse from H50) clearing the repeater ring back to stage one. The gate 68 being open, the central program pulse arrives at the end of the third addition time, resets the flip-flop and feeds through the transmitter (tubes 70, 71, and 72) giving a program output pulse which can be used to operate some other unit during the fourth addition time.

4.2. THE COMMON PROGRAMMING CIRCUITS

4.2.1. The receiving circuits.

The receiving circuits cause the accumulator to add to its present contents any ten digit signed number arriving through the input plugs SV_1 to SV_5. This addition is accomplished by opening the proper set of receiving gates (L to A 41, L to A 42, ..., or L to A 45), and by providing for the carry-over between the various decades.

Suppose that an activated program control has its operation switch set on α. This applies a positive gate to SU 1. The interconnector cable carries this to $ST_1$1, then it will cause tube C48 to become conducting and turn off the inverter J46. The positive gate from J46 opens the gate tubes L41 to A 41 and any digit or PM pulses arriving at the plug SV_1 will be transmitted into the corresponding decade or PM unit. Also, the positive gate from $ST_1$1 will open the gate tube E47 allowing the carry-clear gate (CCG) to be passed to the inverters A to D 49. The output from these inverters then opens the carry gates 19 and 20 in each decade. This carry-over will be explained in detail when the numerical circuits are taken up. (see Sec. 4.3.1.).

If the clear switch is set on C and the operation switch on S, then a negative gate will be applied to inverter G50 turning it off and opening the gates E49 and E50. This passes the 1' pulse through the interconnector terminals ST_2 14 and 15 into the first decade of the accumulator. This provides for the correction of negative numbers where some of the last digits have been lost by the use of deleters (see Section 11.2.)

4.2.2. The add and subtract transmission circuits.

Suppose the operation switch of an activated program control is set at AS. Then a positive gate will appear at SU 7 and be transferred by the interconnector jumper to ST_1 7. Then it will open the gate tubes G47, G49, H49, and M41. G47 will pass the cycling pulses (10 P) to the inverter H48 and the cathode follower L46. The output of L46 operates the buffers B, D, F. H, and K 46 resulting in the decades being cycled through all ten stages back to where they started. G49 will pass the 9 pulses to the inverter E 48 and the cathode follower D48. From there these pulses go to the gate tubes 22 in the decades and the gate tube 16 in the PM unit. Similarly, H49 will pass 9 pulses through C48 and F48 to the gates 21 and 15. M41 passes a 1' pulse through the transmitter (23, 24 and 25 in the PM unit) to the interconnection terminals SU_1 17. From there it goes to the significant figure switch and into one of the output terminals of the subtract output SW_2.

If the operation switch is set at A then the cycling pulses (10P) are provided by gate H47 and the 9 pulses (9P) are supplied to the add gates 21 of the decades and 15 of the PM unit by the gate J49. If the switch is set at S then the cycling pulses are provided by F47 and 9 pulses are sent to the subtract gates 22 of the decades and 16 of the PM unit by gate F49; also, M42 provides the correction pulse (1'P). If the clear switch of the activated program control is set at C then at the end of the operation (one addition time in the case of receivers and one to nine addition times in the case of transceivers depending upon the setting of the repeat switch) a negative

gate voltage will appear at SU 9 and from ST_1 9 it will turn off the inverter J50 opening the gate M45. This passes a carry-clear gate (CCG) to the clear tubes (1 to 10 in the PM-Clear unit).

4.2.3. General description of the clear circuits

For purposes of rounding off numbers the decades of an accumulator are provided with clear-to-five circuits. To the left of the PM unit is seen the significant figure switch. The setting of this switch determines which decade clears to 5. All other decades clear to zero. For example, to round off to three significant figures the seventh decade is cleared to five before the number to be rounded off is put in the accumulator.

Inspection of a decade plug-in unit on the cross-section PX-5-115 shows that clearing any stage in the ring is accomplished by a direct connection to the clear tubes (1 to 10 in the PM unit) labeled "clear T", and a return circuit labeled "clear R" which returns to a resistance. The block diagram shows that all stages except zero and five connect directly to the clear tubes and the resistance, whereas, stages zero and five connect to four decks of the significant figures switch. The significant figures switch effectively reverses the connections to the zero-five leads in one decade causing the decade to clear to five instead of to zero.

With the significant figures switch setting as illustrated, the ninth decade will clear to five, giving numbers with one significant figure. A clear signal coming from the clear tubes in the PM unit will go directly to the upper connections to stages 1, 2, 3, 4, 6, 7, 8, and 9 in all decades; through deck one of the significant figures switch, it will go to the upper connections to the fifth stages in all decades except the ninth (corresponding to one significant figure) and in the ninth through deck 2A it will go to the upper connection of the zero stage. The return circuits come back in a similar manner through decks 2 and 1A.

The clear signal arises by a carry-clear gate being passed by tube M44 to the inverter M43 and thence to tube 1 in the PM unit. If the accumulator is being used with the multiplier or divider the clear gate may be introduced directly into the PM unit as illustrated. The gate M44 will be opened to pass a carry-clear gate in the following cases.

a) If the ENIAC is initially cleared the initial clear gate (ICG) arrives through the buffer M45.

b) If the accumulator is set to selective clear and the selective clear gate (SCG) is provided at the initiating unit (see 2.3.1.) then the inverter J50 is turned off by the signal from the buffer A48.

c) Or, if the program control switch of an activated program circuit is set to O, A, AS, or S and the clear switch to C then at the end of the operation a negative gate appears at ST_1 9 which turns off the inverter J50 and opens the gate M44.

The ICG also clears the repeater ring back to stage one by gating a CPP at K50.

4.2.4. A description of the interconnection features

The outputs of the program control circuits appear at terminals SU located on the front panels. Just above these are the terminals ST. It is expected that the usual plan will be to operate as a ten digit accumulator. In this case a jumper is plugged from the terminals SU_1 to ST_1 (PX-5-121) and a load box is placed in ST_2. This effectively connects together the interconnector terminals located next to each other on the block diagram PX-5-304. In case of twenty digit operation all the program controls must operate in parallel; this means that the load resistors for these circuits cannot be built in since what is correct for separate operation would not be correct when they are operating in parallel. Thus, the load resistors are on a unit which is plugged into the front panel. Only one such unit is used with each accumulator or with each pair of accumulators when con-

nected to form a twenty-digit accumulator.

If two accumulators are to be interconnected to form a twenty digit accumulator then the terminals SU_2 and ST_2 of the left hand accumulator are jumped respectively to SU_1 and ST_1 of the right hand, SU_1 of the left hand is jumped to ST_1 of the left hand, and a load box is placed in ST_2 of the right hand accumulator. This makes the carry-over from the tenth decade of the right hand accumulator go into the first decade of the left hand and the 1' pulse (correction pulse) go into the first decade of the right hand accumulator. The "IO" output of the significant figure switch of the left hand accumulator goes to the input of the significant figure switch of the right hand accumulator. The "O" output of the right hand significant figure switch goes to the input of the units decade of the left hand accumulator.

A list of connections for ten and twenty digit operation are given in tables 4-2 and 4-3. Note that the PM unit of the right hand accumulator is not used in twenty digit operation.

4.3. NUMERICAL CIRCUITS

4.3.1. General description of a decade plug-in unit.

The pulse standardizer (tubes 11, 12, and 13) consists essentially of four triodes (11 being a double triode 6SN7). The output of tube 12 goes both to tube 13 and the gate 14. The output of 13 goes to the decade ring. In the block diagram the large numbers in the stages of the ring represent the positions of the tube while the small number just outside the respective stages represents the digit corresponding to that stage. After clearing, the ring is setting at zero (for a detailed discussion of the operation of ring counter circuits, see 1.2.2.).

Receiving Numbers. If five pulses arrive on the digit input they will pass through the pulse standardizer and step the ring up to position five. Pulses will also go to the gate tube 14 but will have no effect since the second grid of that tube is negative being connected to the negative output

TABLE 4-2

Vertical interconnecter cable. (PX-5-121)
Just one used for either a 10 or 20 digit accumulator.

SU_1	ST_1	
1	1	These connections enable any program control circuit to cause the common programming circuits to make the accumulator receive on channels
2	2	
3	3	
4	4	
5	5	
6	6	These connections enable any program control circuit to cause the common programming circuits to make the accumulator transmit on A, AS, or S.
7	7	
8	8	
9	9	This connection takes care of the clearing action.
10	10	This connection provides for the correction pulse.
11	11	
12	12	
13	13	This connection in the ST_1 end takes the carry of the 10th decade into the input of the PM unit.
14	14	
15	15	
16	16	
17	17	This connection takes the correction pulse transmitted by the transmitter (23-25) in the PM-Clear unit to the input of the significant figure switch.
18	18	Terminal 18 is a ground connection in each case.

Note that the load box plugs into terminal ST_2 and has jumpers which connect terminals 14 and 15 and 16 and 17. This takes the correction pulse into the units decade input (units decade of right hand accumulator in case of twenty-digit operation) and the 16 to 17 connection takes the "10" output of the significant switch to the units channel of the subtract output.

TABLE 4-3

Horizontal interconnector cable. (PX-5-110).

SU_I	ST_I	
1	1	These connections cause any program control to cause the two accumulators to act in unison when receiving on α to ε .
2	2	
3	3	
4	4	
5	5	
6	6	These connections cause the accumulators to act in unison when transmitting on A, -S, or S.
7	7	
8	8	
9	9	This connection causes the clear circuits to act in unison.
10	10	This connection allows any program control to provide the correction pulse at terminal $ST_2 14$ of either accumulator.
11	11	
12	12	
13	13	
14	14	
15	15	For upper cable this connection takes the output of the 10th decade of right hand accumulator to 1st decade input of the left hand accumulator.
16	16	This connection in upper cable takes "0" output of significant figure of right hand accumulator into the units channel of the subtract output of the left hand accumulator.
17	17	This connection takes "10" output of the significant figure switch of the left hand accumulator to the input of the significant figure switch of the right hand accumulator.
18	18	Terminal 18 is a ground connection in all cases. The connections 15, 16, and 17 serve no purpose in the lower interconnector cable (between terminals SU_1 and SU_2).

of the ninth stage of the decade ring. Suppose that six more pulses arrive. Four of these will step the ring up to position nine. The fifth will step the ring from nine to zero and will pass through the gate 14 setting the decade flip-flop and turning the inverter 15 off producing a positive pulse at gate 19. Since the incoming digits arrive before the carry gate goes on (see PX-9-301) this pulse does not pass gate 19. The sixth pulse steps the ring from zero to one. The carry gate comes on later in the addition time, opening gates 19 and 20. Since the flip-flop has been set the reset pulse RP (which arrives just after the carry gate comes on) is passed by gate 18 through the inverter 15 and through gate 20 to the digit input of the next decade to the left. This is called the delayed carry-over. Thus, six plus five is eleven.

Suppose that a decade registers nine and a carry-over arrives from the next decade to the right. This carry-over pulse besides stepping the ring from nine to zero also passes through gate 14 turning off the inverter 15. This gives a positive pulse to gate 19 and since the carry gate is still on, there is a carry-over to the next decade to the left. This is called the direct carry-over. If all decades register nine, one may have a sequence of nineteen such carry-overs in the case of a twenty-digit accumulator so the carry gate has been made sufficiently long to provide for this possibility.

Transmission of numbers. The above description of a decade unit has been in terms of receiving numbers. Now consider an activated program with the program switch set to AS, say. In this case the cycling pulses are arriving at the digit input, there is no carry over since the carry gates A to D 47 are not open, and the nines pulses (9P) are arriving at the gates 21 and 22 in the decade. As indicated in the diagram, normally (after initially clearing) gate 22 is open. Suppose the decade registers the digit three. What happens during the twenty pulse times of an addition time is

illustrated in the table 4-4. Note, that the tens pulses arrive 2 1/2 μs. after the nines pulses; this gives the decade ring 7 1/2 μs. in which to step and also 7 1/2 μs. for the flip-flop (16, 17) to be set. If the operation switch is set at A instead of AS the only difference is that the 9 pulses do not appear at gate 22 and the 1' P is not provided. In case the switch is set at S the 1' P is provided and the 9 P appear only at gate 22. If the clear switch is set to C then at pulse time 10 the carry-clear gate appears at gate tube M45 and the decades are cleared back to zero.

4.3.2. General description of a PM - Clear plug-in unit.

The PM-Clear unit contains a binary counter to register the sign (PM) of numbers. Since the binary counter is much simpler than the decade counter the pulse standardizer is also simpler. It contains three tubes in two envelopes (a 6SN7 for tube 11 and 12 is a 6V6). For a detailed discussion of PM counters see Tubes 1 to 10 are part of the clear circuits and have been described in section 4.2.3. Tubes 15 to 22 comprise the transmitter circuits which transmit the sign indication over the add and subtract outputs. Tubes 23 to 25 form a standard transmitter for the 1' pulse (used to give complements with respect to 10^n instead of 10^n-1, where n is the setting of the significant figures switch.)

An odd number of pulses arriving at the PM binary counter will change its resulting position. An even number of pulses will leave it the same as it was to start with. If the number registered by the accumulator is positive and an activated program control has its operation switch set to AS then nine pulses will pass gate 15. If the registered number is minus then nine pulses will be transmitted through gate 15 over the add output and none will go past gate 16.

TABLE 4-4

Pulse time	General pulses	Cycling pulses (2 1/2 μ sec. late)	Decade Registers	Pulses trans. over SW_2 (subtract)	Pulses trans. over SW_1 (add)
16			3		
17	CPP		3		
18			3		
19	RP		3		
0			3		
1		1st	4	1st	
2		2nd	5	2nd	
3		3rd	6	3rd	
4		4th	7	4th	
5		5th	8	5th	
6		6th	9	6th	
7		7th	0		1st
8		8th	1		2nd
9		9th	2		3rd
10		10th	3	1'P if decade corresponds to last sig. figure	
11			3		
12			3		
13	RP		3		
14			3		
15			3		
16			3		

V. THE HIGH SPEED MULTIPLIER

The high speed multiplier is a unit of the ENIAC capable of forming the product of two ten digit numbers in thirteen addition times (0.0026 secs.). It is called a high speed multiplier because, by making use of multiplication tables, it is able to produce a product much more rapidly than if the method of repeated additions were used. In the method of repeated addition a maximum of nine addition times must be allowed for each digit of the multiplier giving a possible total of ninety addition times for a ten digit multiplier.

The method of multiplication used by the high speed multiplier is to multiply the entire multiplicand by each digit of the multiplier in turn and to sum the resulting products taking into account their proper decimal positions. Thus, only one addition time is required for each multiplier digit (plus three extra addition times for operations that must be performed for each multiplication).

The circuits are so arranged that the digit of the multiplier which is being used at a particular time excites a bus of two multiplication tables, a tens table and an units table. The product of two single digits is usually a two digit number; thus, the output of the tens table is the tens digit of the products of the multiplier digit and the digits one to nine inclusive, while the output of the units table is the units digit of the products of the multiplier digit and the digits one to nine inclusive. The use of the two tables makes it possible for the partial products to be received simultaneously into two accumulators without interference.

Since the product of two ten digit numbers is usually a twenty digit number it will be necessary to use two accumulators interconnected to form a twenty digit accumulator to receive the right hand (units) partial

products and similarly for the left hand (tens) partial products. Thus, for ten digit multiplication the high speed multiplier will work in conjunction with six accumulators, one for the multiplier, one for the multiplicand, two for the left hand partial products, and two for the right hand partial products.

Throughout most of the discussion of this chapter it will be assumed that accumulators 9 and 10 are used for the multiplier and multiplicand, respectively, that accumulators 11 and 12 (connected to form a twenty digit accumulator) receive the left hand products, and that accumulators 13 and 14 (also used as a twenty digit accumulator) receives the right hand products. The setting of the respective program controls on these last (two twenty digit) accumulators determines whether the final product appears in 11 and 12 or 13 and 14.

After the multiplying operation has been carried out for each digit of the multiplier (certain complement corrections may be needed) the right and left hand products are collected into one accumulator. In the fourteenth addition time (for a ten digit multiplication) the product may be transmitted to some other unit and simultaneously the multiplier and multiplicand accumulators may receive the next numbers to be multiplied.

5.0. INTRODUCTION. This description of the multiplier will be given in terms of the block diagram PX-6-308 and the cross section diagrams PX-6-112 and PX-6-112A. In the upper left corner of the block diagram is seen the multiplier selector. To the right of this (upper center) is the tens multiplication table and in the upper right corner is the units multiplication table. Below the tables are the table gates which pass the 1, 2, 2', and 4 pulses. Below the gates are the two multiplicand selectors, one for the tens table and one for the units table. The output of the multiplicand selectors goes to the shifters and thence to the digit outputs.

These circuits comprise what will be called the numerical circuits.

To control the operation of these numerical circuits there are the common programming circuits. The common programming circuits consist of the multiplier ring (located on the block diagram under the multiplier selector), the round-off circuits (A' 46 to 49, A" to H" 45, and K" 45), the complement correction circuits (B" 46 to 50, C" 46 to 50, and L" 43 to 47), the receiving circuits (H, J, and L 41 to 50), the product disposal circuits (D" to J" 46 to 50), the clear circuits (A to L 11), reset circuits (to the right of the ring), and below the reset circuits a receiver to cause the product accumulators to receive the partial products and a circuit (A" 47 to 50) to cause the collection of the right and left hand products.

There remains the program control circuits. These consist of twenty four transceivers, their associated switches and buffer tubes. Associated with each transceiver we have the following switches: a) places switch, b) multiplier and multiplicand clear switches, c) significant figures switch, d) multiplier receive switch, e) multiplicand receive switch, and f) the product disposal switch.

The program control circuits, the common programming circuits, and the numerical circuits will be described in detail in the next three sections. The fourth section will be devoted to examples.

5.1. PROGRAM CONTROL CIRCUITS.

5.1.1. The buffer plug-in units. As shown in the block diagram there are two buffers on the program input lines to each transceiver. There are eight transceivers located on each of the three panels of the multiplier. The sixteen buffers for each panel are located on two plug-in units. The tubes in these plug-in units are numbered from 61 to 68. Note that tubes 61 and 62 are associated with the first program circuit. Those numbered

63 and 64 would be associated with the second program circuit and so forth. This buffer system means that at most five program controls need be used in each of the multiplier and the multiplicand accumulators in order to receive the multipliers and multiplicands for all possible multiplications.

A program pulse arriving on terminal Ii, for example, would turn the buffers 61 and 62 on giving a negative pulse at the receive switches (see 5.2.3). Depending upon the setting of these switches pulses may be obtained out of one of the terminals R_0 to R_9 and one of D_0 to D_9.

5.1.2. Transceivers. These transceivers are standard, that is, they are identical with the transceivers used in the accumulators, the function tables, the divider, and the constant transmitter. This simplifies the problem of maintaining operation, since, if any one fails the unit can be pulled out and a spare put in.

5.1.3. Program control switches. With each transceiver there are the following switches:

a) Places switch. This switch determines how many digits of the multiplier are used in the multiplication. Since the time required for a multiplication is n+3 where n is the number of digits in the multiplier the time required for a problem can be materially shortened if fewer than ten digits of the multiplier can be used. With the place switch setting at 8 (as illustrated) the multiplier ring will step to stage 10 using eight digits of the multiplier. The inverters G' 45 and H' 45 being off the gate H' 46 will turn the inverter F' 47 off and on the next addition time a CPP will pass gate F' 48 and through the inverters C' 47 and D' 47 will clear the ring to stage 13.

b) Multiplier and Multiplicand clear switches. Depending upon

the setting of these switches the following four possibilities arise:

	'Ier Clear Switch	'Icand Clear Switch	Result
(1)	O	O	Neither multiplier or multiplicand accumulators clear.
(2)	C	O	An activated program causes inverter J 30 to go off opening the gate H 30. This gate passes the CCG to the inverter G 31 which turns the buffer J 29 on. The output of J 29 goes directly to the clear tubes 2 to 10 in the PM unit of the multiplier accumulator.
(3)	O	C	In this case A 31 goes off opening the gate B 31. The CCG turns off the inverter C 30 which in turn causes the buffer H 29 to conduct. The output of H 29 goes directly to the clear tubes of the multiplicand accumulator.
(4)	C	C	Here the inverter E 30 goes off opening the gates D 30 and F 30. As above, the clear gate is passed into the two sets of clear tubes in the respective PM units.

c) Significant figures switch. Depending upon the setting of the significant figures switch a 5 is put into one of the decades of the left hand product accumulators. If the switch is setting on 2 (as illustrated) at the second addition time the digit 5 will be passed by gate H" 45 into decade number 8 of product accumulator number 11 (corresponding to digit output terminal SV_4).

d) Multiplier receive switch. This switch determines whether the multiplier accumulator receives the multiplier on the input terminals α, β, γ, δ, or ε. The program pulse arriving over li, for example, turns the buffer 61 on giving a negative pulse through the switch turning inverter H 46 off (if the switch is setting as illustrated). This causes the buffer H 46 (these are the two triodes of a 6SN7) to conduct and the transmitter J to L 46 gives a program pulse out of the terminal R_ε located

on the front of panel one. This will normally be connected to the input of a receiver or a transceiver located in the multiplier accumulator and the corresponding program switch will be set to receive on ε .

e) Multiplicand receive switch. This switch operates in a manner entirely analogous to the multiplier switch described above.

f) Product disposal switch. Suppose that the product is finally collected in accumulators 13 and 14. The setting of the product switch determines what the pair of accumulators (operating as a twenty digit accumulator) do with the numbers. Suppose the disposal switch is setting on SC (as illustrated). The program which started the multiplication set the flip-flop (66, 67 in transceiver) and so opened the gate 62 in the transceiver. At the end of the multiplication the reset signal arrives, passes gate 62 and turns off the inverter 65. This turns on the buffer 63 giving a negative gate through the disposal switch turning off inverter E" 46 opening gate E" 47. At the beginning of the next addition time a CPP is passed through the transmitter E" 48 to 50 to the terminal SC on front panel number three. Generally, the operator will connect this output to the input of a program control circuit on accumulators 13 or 14, say, and the corresponding program switch will be set to S and the clear switch to C. If needed, the other outputs A, S, AS, AC, and ASC, can be connected to the inputs of program control circuits on accumulators 13 and 14 (or 11 and 12 if the product is collected here) and the corresponding switches set accordingly.

5.2. COMMON PROGRAMMING CIRCUITS.

5.2.1. The multiplier ring. This is a fourteen stage ring which controls the timing of the multiplication process. Whenever a program control circuit is activated the inverter H' 44 goes off opening the gate F' 44. This gate then passes central program pulses through the pulse standardizer E' to B' 44 to step the ring. Whenever the ring is not at stage one the gate J' 44 is open. This passes central program pulses to the inverter H' 44 and thence to the gate G' 44. If the initial clear gate is on the CPP pass G' 44 and step the ring until it arrives at stage one.. When

it reaches stage one J' 44 closes shutting off the CPP.

This method of initial clearing by stepping the ring to stage one is used here since, as described below, the regular clearing circuits operate in conjunction with the places switch to clear the ring to stage 13 in the process of terminating the multiplication.

Suppose that program control 1 has been activated. The multiplier ring steps (at the end of the next addition time) to stage two turning A' 45 on and the inverter B' 45 off. This opens the gates A' 46 and 47 which pass the 4 pulses and the 1' pulse to give a five in some decade of accumulators 3 or 4. The output of B' 45 also goes to gate B' 47 which gates a 1 pulse. This 1 pulse turns the inverter B' 48 off and thence sets the two receivers. The outputs of these two receivers come to front of panel three. (See PX-6-304). From there these gate signals will be taken by special interconnecting jumpers to interconnector terminals ST_1 1 on accumulators 11 and 12 and accumulators 13 and 14. Inspection of the accumulator block diagram PX-5-304 shows that this will cause the product accumulators to receive the partial products over the input digit terminals a . This is an example of a receiver located in one unit operating the governing circuits of another unit.

The timing is important here:

Pulse time	17	18	19	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	CPP steps ring to second stage		1 P sets receivers to cause partial prods. to be received						4 P start				1' P arrives							

Thus, in one addition time the ring steps to the second stage, the product accumulators are set to receive, and the five pulses for the round-off are put into the proper decade. The CPP that steps the ring could not be used to operate the receivers because of the time it takes for B' 47

to open.

The next addition time the ring steps to stage three. B' 42 goes on and inverter L 1 off opening the gates for the tenth digit of the multiplier (gates K 2 to K 11). Depending upon the tenth digit of the multiplier one of the lines through the multiplication tables will carry a negative gate (which will turn off certain pulse gates). At the same time inverter B' 41 will go off causing the bottom row of gates in the two shifters to open. Thus, the tens partial product will feed into accumulator 11 and the units partial product into decades 1 to 9 of accumulator 13 and decade 10 of accumulator 14. Notice that the units product is already shifted one place to the right. Thus, when the right and left hand products are collected at the end of the multiplication no extra shifting will have to be done.

As the ring steps from 3 toward stage 12 the gates for successive digits of the multiplier are opened and the gates on corresponding levels in the shifters are opened.

If the place switch is setting on 8 the inverter G' 45 is off opening gate H' 46. When the ring reaches stage 10 the inverter H' 45 goes off causing the gate H' 46 to go on and the inverter F' 47 to go off. This opens the gate F' 48 and at the end (pulse time 17) of the addition time a CPP turns the inverters C' 47 and D' 47 off clearing the ring to stage 13 (this clear signal overrides the stepping signal which would normally step the ring to stage 11). The output of F' 47 also gates a CPP at the end of the addition time at E' 48 which turns the inverter F' 49 off causing the receiver flip-flops to reset. This causes the product accumulators to stop receiving the partial products. The output of F' 47 also opens the gates B" 46 and L" 47. The CPP gated by B" 46 ultimately gives a program pulse out RS if the multiplier is negative and out DS if the multiplicand is negative. If both multiplier

and multiplicand are negative L" 47 gates a 1' pulse which finally goes into the PM channel to accumulator 13.

When the ring steps to stage 13 the inverter L' 45 goes off and gates D 49, K" 50, and A" 47 are opened. At the 14th addition time D 49 gates a CPP which sets a flipflop causing programs 1 to 8 to reset. At the same time K" 50 likewise causes programs 17 to 24 to be reset. A" 47 gates a CPP during the 14th addition time which will generally be used to collect the right and left hand products. This pulse is transmitted to terminal F on the front panel. From there it will be jumped by the operator to a program tray and then used to program transmission of the left hand partial product, say, and the reception of this left hand product by accumulators 13 and 14.

Stage 14 of the ring causes programs 9 to 16 to be reset. The ring is located on panel two of the multiplier, so the gates 62 in transceivers 9 to 16 can be operated directly by the output of the ring. Since transceivers 1 to 8 are on panel one a special flip-flop (E and F 49) set by a CPP during the 1st addition time (passed by gate E 49 which is opened by stage 13 of the ring) provides the reset signal. Similarly, another flipflop (L" and F" 49) resets programs 17 to 24.

From stage 14 the ring steps back to stage 1 and stops. At this time the transceiver gives an output program pulse.

5.3. Initial Clearing.

The initial clear gate is applied to the multiplier only through gate J ... This gate is open only when the program ring is not in stage one. Thus, the effect of applying the initial clear is to cause the program ring to step around to stage one and stop.

In the case of the multiplier program ring the initial method of clearing is used for another purpose. Since the number of places in the multiplier word is odd only four stages in program 2 contribute

between the setting of the places switch of an activated program and the stage on which the ring is setting will open gate F'48 causing the ring to "clear" to stage 13.

As with the accumulators there is no need to initially clear the transceivers. Any program pulses which get started in the programming circuits are allowed to run through the sequence (all sequences are broken at the master programmer, see 10.5), and then the decades of various units are cleared.

5.4. NUMERICAL CIRCUITS.

5.4.1 The multiplier selector. The multiplier selector is an array of one hundred gate or coincidence tubes. There is a tube for each possible digit in each place of the number. When the multiplier ring is at stage three the gates for the tenth digit of the multiplier will be open. If the first digit of the multiplier is 4, for example, then the static output of that stage of the tenth decade of the multiplier accumulator will be energized and the tube K 7 will conduct giving a negative gate to the inverter L 7. When this inverter goes off the tubes L 26 and K 26 go on giving a negative gate on line 4 into the multiplication tables.

5.4.2. The tables and the table gates. The 1, 2, 2', and 4 pulses come from the cycling unit trunk to buffers D 45 and 47 and E and F 48. From the buffers each pulse goes to an inverter and then to the table gates. Inspection of the cross section PX-6-112(A) shows that the table network is such that normally the second grids on the table gates are sufficiently positive that they pass the 1, 2, 2', and 4 pulses. Thus, the multiplication table is a so called "complementary" table, that is, all the gate tubes normally pass the 1, 2, 2' and 4 pulses and are turned off by the table if they are not wanted.

The digits of the multiplier are represented by the horizontal

lines through the table. The digits of the multiplicand are represented by the vertical groups of lines as labeled at the top of the table. In multiplying one times nine (consider one as the multiplier) the lines of the last column of the units table have no connections to the horizontal line 1. This allows gates D to G 21 to pass nine pulses which is the units part of the product of nine and one. In the tens table for the same two numbers there are connections to all four vertical lines. This means that gates D to G 41 will be closed, which is correct since the tens part of the product of 1 and 9 is 0.

Now, consider six times seven. On the horizontal line for six in the units table in the column for seven there are connections to 1, 2', and 4 but none to the 2 lines. This means that gate F 23 will be open and will pass two pulses but D, E, and G 23 will be closed. In the corresponding place in the tens table there are connections to the lines for 1 and 2. Therefore, the gates E and G 43 will be closed while D 43 will be open and will pass 4 pulses. Notice that zero in the multiplier must be connected to all vertical lines in the table so as to stop all pulses from going to the multiplicand selector. Also, note that zero gates are not needed in the multiplicand selector.

5.4.3. The multiplicand selectors. The output of the table gates for the nine column in the tens table goes to the top row of gates in the left hand multiplicand selector. The output of the eight column goes to the second row, and so forth. There is no need for a units column or a units row in the tens selector since one times any digit gives zero in the tens place. Similarly, in the units table the output of the nines column goes to the top row of the selector, et cetera.

Suppose the digits of the multiplicand are 98765 43210 and the multiplier digit is six. In the tens selector gates L' 21, K' 22, J' 23, ..., D' 28 will be open and will respectively pass 5, 4, 4, 3, 3, 2, 1, 1

pulses. In the units selector gates L' 1, K' 2, J' 3, ..., C' 9 will be open and will respectively pass 4, 8, 2, 6, 0, 4, 8, 2, 6 pulses. These pulses will feed through a inverter-buffer-inverter sequence into the shifter. If the six was in the third place of the multiplier then the gates H" 30 to H" 21 and H" 10 to H" 1 will be open in the respective shifters. Thus, the partial products of this step in the multiplication will arrive in the product accumulators in the following manner:

Acc. 11	Acc. 12	Acc. 13	Acc. 14
00000 00544	33211 00000	00000 00048	26048 26000

The output of the shifter passes through the driver tubes (A" to K" 44, for example). This is quite different from the standard transmitters used on the output of an accumulator (see PX-5-304).. This means that for reliable operation the product accumulators should be close to the multiplier and a short tray with no load box used to carry the partial products to the accumulators.

With the interconnector cables in use at the present time the partial products are received over the α inputs to the accumulators. Since the capacity on the outputs of the driver tubes mentioned above is limited (for the capacity limits here see the operators manual), the α inputs to the accumulators used to receive the partial products must not be used for any other purpose.

Note that rows of shifter gates are opened only when the program ring is on stages 3 to 12. Thus, when not multiplying (program ring is at stage 1) pulses (passed by the table gates and the multiplicand selector) are not passed by the shifter gates.

5.5. EXAMPLE.

Operation of multiplier.

Addition and pulse time	Description
0.17	Program pulse arrives at transceiver. This pulse passes buffers (61 and 62, for example) and depending upon the setting of the multiplier and multiplicand receive switches may be transmitted again. Gates F'44, K'46 and K" 45 (assuming the places switch is at 10 and that the significant figure switch is at 10) are opened.
1.17	A CPP passes F'44 to step the program ring to stage 2. Gates A' 46 and 47 are opened, as is gate B'47.
2.1	One pulse passes gate B'47 to set the l and r receivers.
2.6 to 2.10	Four pulses and a one primed pulse pass gates A' 46 and 47 to give five pulses out channel 10 of SV_3
2.17	The program ring steps to stage 3. The output of stage three causes the multiplication of the multiplicand by the first digit of the multiplier to take place.
3.17	The program ring steps to stage 4 and multiplication by the second digit takes place.
4.17	The program ring steps to stage five, and so forth.

11.17	The program ring steps to stage 12, opening gate F'48, E'49, B"46 and L"47. Multiplication by the tenth digit of the multiplier takes place.
12.10	1'P passes L"47 and (if both multiplier and multiplicand are negative) will be transmitted into the PM unit of accumulator 13.
12.17	A CPP passes F'48 clearing the ring to stage 13 opening gates D49, K"50, and A"47. A CPP passes E'48 to reset the l and r receivers. A CPP passes gate B"46 and may pass B"47 and/or C"47 to cause the complement corrections.
13.17	The program ring steps to stage 14. CPP pass gates D49 and K"50 to set the flip-flops E, F49 and K", L"49. A CPP passes gate A"47 to be transmitted to program the product collection (this pulse appears at terminal F).
14.10	The CCG may pass one or two of the gates B,D,F, or H 30 to cause the multiplicand and/or the multiplier accumulator to clear.

14.17 CPP pass gate 68 in the activated transceiver to reset it and to give an output program pulse. A CPP may pass one of the gates D" to J" 47 to program the product disposal. The program ring steps back to stage 1.

VI. DIVIDER AND SQUARE-ROOTER

The divider and square-rooter performs the operations of dividing and square-rooting ten and twenty digit numbers. To carry out these operations with ten and twenty digit numbers it makes use of four and seven accumulators, respectively. Thus, the divider and square-rooter unit itself is essentially a programming circuit which controls the operation of the associated accumulators.

The process of division is that of repeated subtraction. Thus, the numerator is in one accumulator and the denominator in another. The denominator is subtracted until an overdraft occurs. At this time the numerator is shifted (by transmitting to a shift accumulator and transmitting back with a shifter in the digit line). Note that the overdraft was not corrected as in some methods of division used on computing machines. Instead, signs are changed and the denominator is alternately subtracted and added between the shifts. The quotient is built up by the divider sending +1 or -1 into the proper decade of the quotient accumulator for each subtraction.

The process of square rooting is likewise accomplished by repeated subtractions (the quantity subtracted being increased by two each time in the proper decade). The number to be square rooted is placed in the numerator accumulator and the numbers to be subtracted are built up in the denominator accumulator. When an overdraft occurs the number in the numerator accumulator is shifted (similar to the shift in dividing) and certain corrections are made to the number in the denominator accumulator and the subtraction process is repeated. As the process continues twice the square root is built up in the denominator accumulator.

6.0. INTRODUCTION

Description of the divider will be given in terms of the block diagram PX-10-304. For purposes of description the circuits of the divider square-rooter will be divided as follows:

1) Program controls. The program control circuits consist of eight transceivers and their associated switches. These switches and their purposes are as follows:

a) Numerator receive switch. During the first addition time of the division this switch may be used to cause the numerator accumulator to receive either α or β.

b) Denominator receive switch. During the first addition time of the division this switch may be used to cause denominator accumulator to receive on α or β.

c) Numerator clear switch. At the end of the division or root process this switch may be used to cause the numerator accumulator to clear.

d) Denominator clear switch. At the end of the process this may be used to cause the denominator accumulator to clear.

e) Interlock switch. This switch decides whether or not the interlock feature is used. Suppose this switch is setting on II. At the end of the division or root process the various flip-flops and rings in the divider square-rooter are cleared and an output program pulse is transmitted. If this switch is on I then this clearing process and output pulse does not occur until both a signal is received on one of the interlock inputs, (upper left corner of PX-10-304), and the division or root process is completed.

f) Answer disposal switch. This switch is connected to four receivers and thus gives four possible ways of disposing of the answer (that is,

four ways it could be transmitted).

g) Round-off switch. This switch decides whether the answer to the division or the square rooting process be rounded off.

h) Division-Square root and place switch. This switch determines whether the process is division or square rooting and how many places are used. There is a choice of 4, 7. 8, 9, or 10 places.

2) The common programming circuits. In the divider-square rooter (as in other units) the common programming circuits comprise all of the circuits except the program controls (described above) and the numerical circuits (described just below).

3) Numerical circuits. The numerical circuits of the divider-square rooter comprise the place ring and its associated gates (lower right hand corner of PX-10-304), the pulse gates (just above and to the right of the place ring), and the "1", "-1", "2", and "-2" receivers which open these gates.

6.1. PROGRAM CONTROLS

There are eight standard transceivers to receive the incoming program pulses. As in the case of the multiplier the incoming program pulse is immediately retransmitted to cause the numerator and denominator accumulators to receive their numbers without the loss of time. This retransmission takes place through buffers located on a separate plug-in unit (there are two such plug-in units altogether). Two such buffers, 67 and 68, are illustrated in the lower left corner of PX-10-304.

6.1.1. Numerator and denominator receive switches

The buffers 67 and 68 (described above) feed two switches located on the front panel, namely, the numerator and denominator receive switches. Each

of these switches have three settings, α, β and 0. The four outputs of these two switches go through inverters (B4, B5, A4, and A5) to four receivers (located on two plug-in units). The outputs of these receivers come to output sockets located on the front panel. The outputs may be connected directly to the common programming circuits of the respective accumulators by use of a special interconnector cable (See section 11.6.4.).

6.1.2. The numerator and denominator clear switches

The output of one of the buffers 63 (in the transceiver) goes to the numerator and denominator clear switches. This buffer 63 goes on only at the end of the division or rooting process (and possibly after an interlock signal) when clearing is taking place. The output of the switches (three outputs: numerator, denominator, or both) goes to inverters C49 and D49 and thence to gates A48, A49, B48, and B49. These gates pass the carry clear gate (CCG) through the inverters A47 and/or B47 and buffers A46 and/or B46. This signal goes directly to the clear tubes in the PM-Clear units of the corresponding accumulators (see PX-5-C7). The following table illustrates what happens with the various settings of these switches:

TABLE 6-1

Num. Clear Switch	Denom. Clear Switch	Effect (as tube 63 in transceiver goes on)
0	0	None
C	0	D49 goes off and gate B48 passes a CCG through the inverter B47 and buffer B46 to the clear tubes in the numerator accumulator.
0	C	Half of C49 goes off and gate A49 passes a CCG through A47 and A46 to the clear tubes of the denominator accumulator.
C	C	The other half of C49 goes off and gates A48 and B49 pass CCG's through A47 and A46 in one case and B47 and B46 in the other.

6.1.3. Interlock Switch

The setting of this switch determines whether the interlock feature is used or not. If this switch is setting at "NI" the buffer 61 (in the transceiver) causes the inverter L49 to go off and the gate K49 to open. The CPP's passed here turn the inverter H49 off. The gate H50 is opened at the end of the division or square rooting process and the CPP's from H49 are passed to provide the clearing action.

If the interlock switch is setting at "I" the other half of L49 is turned off and L48 is open. In order for a CPP to get through to gate H50 the flip-flop H, J 48 must be set opening gate J49. This flip-flop is set only when a signal arrives over one of the interlock inputs turning on one of the buffers F 46 to 48 or G48. (This pulse may arrive during the division or root process or even before it starts).

Thus, if the switch is set on "I" the clearing signals and the output program pulse are not provided until; (1) the division or square rooting process is completed and the control ring steps down to stage seven, and (2) a program signal has arrived over one of the interlock input terminals and set the flip-flop H, J48. Note that the interlock flip-flop H, J48 is not reset unless the program control being used is set to "I". This means that a number of divisions or square roots may be done and then the interlock feature be used at the end even though the interlock pulse arrived during one of the earlier divisions.

6.1.4. Answer disposal switch

This switch has five positions, four of these go respectively to four receivers and the fifth is an "off" position. At the end of the division or square rooting process (and after the interlock signal has arrived if the interlock switch is at "I") the buffer 63 (in the transceiver) goes on. This

may (depending upon the setting of the switch) cause one of the inverters E46 or E47 to go off opening one of the gates C or D 46 or 47. The CPP passed by one of these gates will turn the corresponding inverter C or D 48 or 49 off activating the corresponding receiver. The outputs of this receiver go directly (provided the operator connects them) to the common programming circuits of the quotient accumulator or to the denominator accumulator depending on the interconnector cable used (see section 11.6.4.) The timing of the operation of these circuits is explained in sections 6.4.1 and 6.4.2.

6.1.5. Round-off Switch

The round-off switch is a double-pole, double-throw switch which determines whether the answer is to be rounded off or not. One pole of the switch operates in case of division and the other in case of square rooting and works in conjunction with one deck of the root-divide and place switch. The four terminals connect to four inverters (the four triodes of L4 and L5) which in turn connect to the gates L3, K3, K4, K5, K6, and L6. These gates provide the division pulse (DP), the square root pulse (SRP), and the round-off pulse (ROP).

6.1.6. Root-Divide and Place Switch

Of the two decks of this switch one (the one on the right on PX-10-304) determines whether the process is to be division or square rooting. This deck takes the output of buffer 61 in the transceiver to the round-off switch described above. The other deck determines how many places the answer is to contain. This switch handles two jobs. This means that the number of places used in a division or a square rooting is restricted to 4, 7, 8, 9, or 10.

6.2. THE COMMON PROGRAMMING CIRCUITS

The common programming circuits, which constitute most of the divider, will be divided into sections as indicated below. This subdivision is a logical one, that is division is with respect to the purpose of the particular circuit and not with respect to physical location. To a considerable extent this division is indicated on the block diagram PX-10-304 by the spacing between circuits. The subdivisions are:

a) The pulse source circuit. This circuit centers around the pulse source flip-flop E 4 and 5 located to the right of the program control circuits on the block diagram. The circuit extends up to and including the gates L3, K3 to K6, and L6.

b) The program ring circuits. The program ring is located on the upper left portion of the block diagram. This circuit includes the program ring flip-flop A, B 6 and the associated gates.

c) The sign indication circuit. This circuit (located in the upper right hand corner of the block diagram) includes the denominator flip-flop, the numerator ring, and the sign indicating matrix (just below).

d) The over-draft circuit. This circuit determines when the numerator changes sign, that is, when there has been an overdraft. This circuit is located at the top center of the block diagram.

e) The add-subtract circuit. This circuit programs the trial additions or subtractions and is located directly under the numerator ring and the sign indication circuit. Its left hand part consists of the N_α receiver and the D_γ and Q_γ receivers. The right hand part consists of the D_S and D_A receivers and the associated gates, inverters, and buffers.

f) The round-off circuit. The round-off circuit is located practically in the midst of the add-subtract circuits. It consists of the round-off flip-flop L 11 and 12 and the associated gates and inverters. It includes the gates G8, H8, E13, and F13.

g) The root correction circuit. This circuit is essentially the receiver D_γ and the root reset lines.

h) The shift circuit. The shift circuit is below the overdraft circuit and to the right of the pulse source circuit. At the time of over-draft it causes the number in the numerator accumulator to be transmitted to the shift accumulator and then to be transmitted back again. A shifter is used on the input (α) to the numerator accumulator so that the number is shifted one place to the left when it comes back from the shift accumulator. The shift circuits comprise the S_α, N_A, S_A, and N_α receivers and their associated gates and inverters.

i) The clear and interlock circuits. The clear circuits are located in the upper left hand corner of PX-10-304 to the left of the program ring. These circuits determine when the division or rooting process has finished and (depending upon the setting of the interlock switch of an activated program control) perhaps when some other sequence of computations is finished (as indicated by the output program pulse of that sequence arriving over one of the interlock inputs). Since a division or root process is of unknown length this allows the operator to carry on other computations simultaneously and then to follow with another sequence of computations only when both the division or root process and the other sequence are completed.

6.2.1. The pulse source circuits.

The pulse source flip-flop is normally in a state which causes gates

F4 and F6 to be open. The flip-flop is in this position except for period III (see PX-10-305 or PX-10-306, the division and square rooting time tables). Thus, during periods I, II, and IV central program pulses pass gate F4, go through the inverter G4 and the cathode followers G3 and H4. This produces a general pulse (GP) which does the following things

(1) goes to gates K6 and L6 to produce a division pulse (DP),

(2) goes to gates L3 and K3 to produce a square root pulse (SRP),

(3) goes to gate A7 to clear the program ring,

(4) goes to gate B7 to set the program ring flip-flop,

(5) goes to gate D9 to produce a "P" pulse which causes an add-subtract cycle to take place (see the time tables PX-10-305 and PX-10-306),

(6) goes to gate E9 to cause a shift cycle to take place,

(7) goes to gate C11 to produce a root reset pulse,

(8) goes to gate C9 to produce a "P" pulse which starts another add-subtract cycle after a shift cycle is completed, and

(9) goes to gate D6 (top of drawing) to step the numerator ring and set the denominator flip-flop in case of negative signs.

The gate F6 passes the one-primed pulse and during a shift cycle this pulse passes gate L45 to step the quotient place ring. Using the 1'P here allows extra time for the quotient ring to step and set up its array of gates.

During period III the flip-flop E 4, 5 is set. This opens the gate F5 and the central program pulses pass the inverter G5 and the cathode follower A12 to produce a third period pulse (IIIP). This third period pulse does the following things:

(1) goes through the buffer C12 and the inverter D13 to give a root reset pulse,

(2) goes to the gates K4 and K5 to produce a round-off pulse (ROP),

(3) goes through the buffer and inverter A12 and the buffer A13 to the pulse standardizer of the program ring.

The pulse source flip-flop is set during a shift sequence by a pulse passing gate E6. This gate will be opened by the inverter D50 going off, and this is caused by a coincidence between the setting of the place switch and the position of the quotient place ring as detected by one of the gates A to C 41, A42, or A43. This flip-flop is reset either by the program ring reaching stage seven and opening gate F3 to pass a CPP or by a C1' pulse arriving at the buffer F3 from the clear circuits. The C1' pulse resets this flip-flop when initially clearing whereas the CPP passing E3 indicates the division or rooting is completed and by resetting E4, 5 prevents the program ring from stepping until A, B, C is reset and another program control is activated.

6.2.2. The program ring circuits.

Normally (after initially clearing) the program ring flip-flop (A, B 6) causes the gates A10 and A11 to be open. Thus, as the process of division or square rooting starts the DP pulses or the SRP pulses pass one of these gates and (going through the inverter A12 and buffer A13 to the pulse standardizer) step the program ring. In two addition times (see section 6.4.1.) the program ring will step to stage one. The output of this stage opens gates A7 and B7. A7 passes a general pulse (GP) which turns off the inverter A9 clearing (the clear signal overrides any stepping signal) the program ring back to stage one. At the same time a GP passes gate B7 to set the program ring flip-flop (A, B 6). This closes the gates A10 and A11 preventing the division pulses (DP) or the

square rooting pulses (SRP) from stepping the program ring again. After this the program ring remains in stage one until the third period pulse (IIIP) is produced. The IIIP will then cause the ring to step through all nine positions.

The positions of the program ring at all times is listed in the division and square rooting times tables PX-10-305 and PX-10-306. The following table gives the effect of each position of the program ring.

TABLE 6-2a

Period I		
Position of program ring	Division	Square rooting
A		
B	Gate D4 is opened to pass a general pulse (GP) through the inverter D5 to the gates K1 and B1 to set the numerator binary ring and the denominator flip-flop in case of negative signs.	Same as for division.
1	(1) Opens gates A7 and B7 to clear program ring and to set the program ring flip-flop. This causes the ring to clear to zero and remain there until period III.	(1) Same as for division.
	(2) Opens gate B8 which passes a division pulse (giving a P pulse) starting the first add or subtract cycle (IP).	(2) Opens gates K8 and C7. These pass square rooting pulses (SRP) which cause +1 to be placed in the denominator accumulator to start the square root process.

TABLE 6-2a (Cont'd.)

Position of program ring	Period III (Operation is same in division or square rooting)
A	
B	Opens gate C8 to pass a round-off pulse (ROP) giving a P pulse which starts the add or subtract process. Gate D6 is opened but with no effect since general pulses (GP) are not produced in this period.
1	No effect since GP, DP, or SRP pulses are not produced this period.
2	
3	
4	
5	Opens gate D4 to pass an ROP giving a reset pulse which terminates the add or subtract process started above.
6	Opens gate J13 passing an ROP through the inverter K13 to gate K12. In case of no over-draft K12 passes this pulse through the inverter K11 into the round-off circuits.
7	Opens L 50 which passes a CPP to the clear circuits and opens E3 resetting the pulse source flip-flop.

6.2.3. The Sign Indication Circuit

In division this circuit (which consists of the gates B1, K1, L1; the flip-flop C 1 and 2, the binary ring H 1, 2; and the matrix of gates D1, D2, E1, E2) detects the initial signs of the numerator and denominator and, thus, determines whether the denominator is to be added or subtracted and whether +1 or -1 is to be put into the quotient. In the case of square rooting, after the process is started these circuits serve exactly the same purpose as in

division; that is, after an over-draft the arithmetical process must be changed from addition to subtraction (or vice versa) and the sign of the two's added into the denominator accumulator must be changed.

In period 2 of the process (division or square rooting) the gate D6 is opened by the program ring stepping to stage B.

If the denominator is negative, the negative static output of the Pd-Clear unit of the denominator accumulator causes gate D1 to open. If the numerator is negative the static output of the negative stage of the Pd ring of the numerator accumulator causes gate K1 to open. Thus, when the program ring steps to stage B a general pulse (GP) passes gate D6, turns the inverter L5 off and may pass gates B1 and K1 (depending upon the signs of the numerator and denominator).

Thus, after the program ring has reached stage B there are four possible situations as illustrated in the following table.

TABLE 6-2b

Numerator Sign	Denominator Sign	Matrix gate on	Result
+	+	E1	B10, G8, E13 are open. B10 passes a pulse which sets the D_S receiver causing the denominator to be subtracted.
+	-	D1	B11, H8, F13 are open and denominator will be added.
-	+	E2	B11, H8, E13 are open.
-	-	D2	B10, G8, E13 are open

Note that the arrangement of the gate tubes in this circuit is not the usual plan followed elsewhere in the ENIAC. Usually, there is an inverter between two gates. If the first gate tube begins to conduct it causes the inverter to go off. The resulting positive signal causes the second gate tube to conduct (assuming the other control grid is sufficiently positive). Here in the sign indication circuit (the same is true in the overdraft circuit, see section 6.2.4.) there is no inverter between the gate tubes. The plates of E1 and D2 are connected to one control grid of the gate tubes B11, H8, and F13. Thus, if gate E1 or D2 is conducting the grids of the three gates are held below cut-off and none of them can conduct. On the other hand, if neither E1 and D2 are conducting then their plate potential is relatively high and the gates B11, H8, and F13 will conduct if a relatively positive signal is applied to their other control grids.

Note that the denominator flip-flop is changed only at the beginning of the process, that is, it does not change its state during the process of division or square rooting. On the other hand, the numerator ring is stepped at the start for negative numerators and, in any case, is stepped during each shift sequence. At the end of the process the clear pulse (C1) arrives from the clearing circuits and resets the flip-flop and clears the numerator binary ring.

6.2.4. <u>The over-draft circuit</u>

The over-draft circuit is another matrix of gates similar to that in the sign indication circuit. This matrix is fed by the output of the numerator ring and by the static outputs of the PM ring in the numerator accumulator. The setting of the numerator ring is fixed during the process of addition or subtraction (in both division and square rooting) and its setting

depends upon the original sign of the numerator and the number of shifts which have occured. When the PM sign of the numerator changes indicating an over-draft the static leads to the overdraft circuit change their potential causing a different gate to conduct.

As explained in the next section (6.2.5.) the add-subtract cycle takes two addition times. Thus, there is a full addition time after each trial addition or subtraction for the PM static lines from the numerator accumulator and the over-draft circuits to set up.

Thus, the sign indication circuits remember the sign of the denominator by the denominator flip-flop (remains unchanged throughout the whole process) and the sign of the numerator (by the numerator binary ring) (changes after each over-draft); and the over-draft circuit detects a change in sign of the numerator (or radicand in case of square rooting).

After the program ring has reached stage B (in period I), allowing the numerator ring to be stepped if necessary, gate G2 will be conducting if the numerator is positive.or else F1 in case the numerator is negative. Then gate D12 is closed and gate D11 is open. Gate D11 being open leads to the production of a pulse P which causes the add-subtract cycle to take place. When an overdraft occurs F2 or G1 is conducting, causing gate D11 to close and D12 to open. This leads to a shift sequence, that is the numerator is sent to the shift accumulator and then transmitted back through a shifter which moves it one place to the left.

6.2.5. <u>The add-subtract circuit</u>

The add-subtract circuit consists essentially of five receivers and their associated gates and inverters. These five receivers are (1) D_A which programs the denominator accumulator to transmit the denominator over its add

output, (2) D_S which programs the denominator accumulator to transmit the denominator over the subtract output, (3) N_α which programs the numerator accumulator to receive on α (this receiver is on the gate chassis instead of on a plug-in unit), (4) Q_γ which programs the quotient accumulator to receive on γ, and (5) D_γ which programs the denominator to receive on γ. Receiver Q_γ is used only in the process of division and receiver D_γ is used only in the process of square rooting.

At the start of an add-subtract cycle a P pulse passes gate B10 or gate B11, turns off the inverter B12 or B13, and activates the D_S or the D_A receiver, respectively. These receivers are reset by a signal from the buffer C5 or the gate D4. If the receiver D_S is activated the fast buffer output from a cathode follower goes (by way of interconnecting cables) to the common programming circuits of the denominator accumulator causing that accumulator to transmit over its subtract output. The slow output of the D_S receiver goes through the inverter C11 and opens the gates G11 and G12. The receiver D_A operates in a similar manner causing the denominator to be transmitted over the add output of the accumulator and the gates H11 and H12 to be opened.

The same P pulse which causes the D_A or D_S receiver to be activated also activates the N_α receiver (C, D 7, E7, F7, D8). The output of the cathode follower F7 goes to the common programming circuits of the numerator receiver and causes it to receive on α. The slow output goes through the buffer and inverter E7 and L8 to open the gates L9 and L10.

L9 or L10 pass square root pulses (SRP) or division pulses (DP) which set the D_γ or Q_γ receivers, respectively. The division pulse (DP) which passes L10 to set the Q_γ receiver also passes G11 or H11 to set the +1 or the -1 receivers in the numerical circuits (see section 6.3.) Similarly, in the process

of square rooting the SRP which activates the D_y receiver also passes G12 or H12 to set the +2 or the -2 receiver.

The slow buffer outputs of the D_y and the Q_y receivers join and connect to the grid of the inverter C10. Thus, when either D_y or Q_y is activated the inverter C10 will go off, the buffer E6 on, and the inverter F3 off giving a positive signal to the gates D11 and D12. If this addition or subtraction did not produce an overdraft gate D11 will be open, the inverter D10 will go off opening D9. This gate passes a general pulse (GP) producing another P pulse which starts another add-subtract cycle. If there has been an overdraft then gate D12 conducts starting a shift cycle (see section 6.2.8.)

6.2.6. The round-off circuit

The round-off procedure consists of subtracting the denominator from the numerator five times (in the case of square rooting, twice the square root is subtracted five times from what remains of the radicand in the numerator accumulator). If there is an over-draft nothing is done. If there is no over-draft then, depending upon the signs and whether the process was division or square rooting, a +1, -1, +2, or -2 is added to the quotient or to the denominator (twice the square root).

The round-off procedure occurs during period III (see PX-10-305 and PX-10-306) which is inaugurated by coincidence between the position of the quotient-place ring and the position of the root-divide-places switch as detected by one of the gates A41, B41, C41, A42, or A43. The subtraction (or addition) is started by a round-off pulse (ROP) being gated by C8 when the program ring is at stage B. This activates the N_α and the D_A r D_S receiver (the Q_y or D_y and the ±1 or ±2 receivers are not activated since no DP or SRP pulses are produced in period III). Since general pulses are not produced in this period, the D_A or D_S and the N receivers are not reset until the ring reaches stage 5.

At that time a reset signal is produced by an ROP pulse being gated by D4. When the program ring reaches stage 6 an ROP pulse is gated by J13, and if there has been no over-draft this pulse is passed by gate K12.

The divide-root flip-flop remembers whether the process was square rooting or division and accordingly decides whether to send ± 1 or ± 2 and whether to send them to the denominator accumulator or to the quotient accumulator.

In case of division the pulse which may be passed by gate K12 passes gate J10 to set the Q_y receiver and it passes gate J8 to activate the +1 or the -1 receiver (depending upon the signs this pulse may pass gate G8 to activate the +1 receiver or else it would pass the gate H8 to set the -1 receiver).

6.2.7. The root correction circuit

In the process of square rooting, after an over-draft has occurred it is necessary to correct the number appearing in the denominator accumulator. In the case of a subtraction cycle the number being subtracted (that is, the number in the denominator accumulator) is being increased by two each time. After an over-draft occurs one more two is added on, then one must be subtracted at the same place and another one must be subtracted in the next place to the right. If it is an addition cycle, then two is being subtracted from the number in the denominator each time, and after the over-draft one more two is subtracted, then one is added on and another one added in the next place to the right.

The circuits are so arranged that there is always one more "two" added or subtracted after the actual over-draft occurs. The root correction circuits take care of the adding or subtracting the "one".

After an overdraft occurs a general pulse (GP) passes gate E9 starting the shift process, setting the flip-flop (A, F 10) of the D'_γ receiver, and passing gate H9 or G9 to set the +1 or the -1 receiver. These receivers remain activated for two addition times, since the root reset signal is not produced until the N'_γ receiver is set, opening gate C11. The quotient place ring is automatically stepped (by gate L45 being opened) in between, so that the first ± 1 goes into one place in the answer and the next one goes into the next place to the right.

6.2.8. The shift circuit

When an over-draft occurs gate E9 is opened. This passes a general pulse (GP) which goes through the inverter F9 and sets the N_A and the S_α receivers. These receivers cause the numerator to transmit on add and clear, and the shift accumulator to receive on α. The slow buffer output of the S_α receiver goes through the inverter L8 to three gates. One of these gates, L1, passes a central program pulse which steps the numerator ring changing the sign in the sign indication circuits in preparation for the next add-subtract cycle. Another gate, L45, passes a 1' pulse (1'P), coming from gate F6, which goes to the pulse standardizer L-J, J1 and thence to step the quotient place ring. The third gate, K7, passes a central program pulse which activates the S_A and the N'_α receivers. These receivers cause the number now in the shift accumulator to be transmitted and cleared and received by the numerator accumulator.

The slow buffer output of the N'_α receiver goes through the inverter C10 to open the gates C9 and C11. C9 passes a general pulse (GP) to produce a P pulse which starts the next add or subtract cycle. C11 passes a general pulse to produce a root reset pulse which is essential to reset the D'_γ and the +1 or -1 receivers in the case of square rooting. In the case of division this circuit is not used since division pulses are passed by the buffer C12 to pro-

duce a root reset pulse each addition time.

6.2.9. The interlock and clear circuits

These circuits consist of three flip-flops and associated gates and inverters. One flip-flop (H, J48) remembers whether the interlock signal has arrived or not (the interlock signal is the output program pulse for the last operation of the sequence of computations which goes on simultaneously with the root or division process). Another flip-flop (K, J 50) remembers the fact that the division or root process is finished. These two flip-flops open gates J49 and H50 which pass a central program pulse serially setting the flip-flop G, F 50. The interlock flip-flop H, J 48 may be by-passed in case the interlock switch is set at "NI". In this case the CPP passes gate K49 instead of gate J49. The pulse passed by H50 resets the flip-flop K, J 50.

The output of flip-flop G, F 50 opens gate 63 in the activated transceiver and gate F49. A CPP passes gate F49 and the inverter E49 to provide the Cl' pulse. Thus, CL' is a positive pulse. In some places a negative pulse is needed for the clearing action so the Cl' pulse goes through a buffer E48 to produce the Cl pulse—a negative pulse.

The Cl' pulse does the following:

(1) May pass gate L48 (depending upon the position of the corresponding interlock switch) to reset the interlock flip-flop H, J 48.

(2) Turns on the buffer A8 causing the program ring to clear back to stage A.

(3) Turns on the buffer F3 resetting the flip-flop E 4, 5.

(4) Turns on the buffer C13 producing a root reset pulse which resets the D_y receiver (E, F 10) and the +1 and -1 receivers.

The C1 pulse does the following:

(1) Resets the flip-flop G, F 50.

(2) Resets the denominator flip-flop C 1, 2.

(3) Turns off the inverter K2 causing the numerator binary to be cleared.

6.2.10. The initial clear

The initial clear gate opens gates E50 and K48. E50 passes a CPP to the inverter E49 producing the C1' pulse (see above). The CL' pulse not only passes buffer E48 to produce the C1 pulse but also passes gate K48 to reset the interlock flip-flop H, J 48. The action of the C1 and C1' pulses in this case is exactly as described in the section above.

6.3. NUMERICAL CIRCUITS

The numerical circuits comprise the quotient place ring and its associated gates, the L1, -1, +2, and -2 receivers, the pulse gates. All of these circuits are located on the lower right hand corner of the block diagram PI-10-304.

6.3.1. The quotient-place ring

The quotient place ring causes the ± 1 or ± 2 which go to make up the quotient or the square root to arrive in the proper decade of the quotient or denominator accumulator. Also this ring causes the division or root process to be terminated when the proper number of places (as determined by the divide-root-place switch, see section 6.1.6.) in the answer have been computed. The ± 1 and ± 2 receivers open combinations of gates which pass groups (of the 1, 2, 2', 4, or 9 pulses) of pulses which represent the numbers +1, -1, +2, or -2.

The static output of each stage of this ring goes directly to one gate

tube and through an inverter to another gate tube. Thus, most of the gates connected to the ring are normally open and those connected via the inverters are normally closed. The ring clears to stage one (tube 29). Then, normally (after initially clearing) gate K43 will be open and all of the gates B42 to L42 will be open except K42. As the ring steps through various positions, one of the gates B43 to L43 is always open, and all except one of the gates B42 to L42 are conducting.

In the following discussion assume that the quotient place ring is at stage 1 and the cases where the receivers +1, -1, +2, and -2 are each activated will be discussed in succession.

(1) +1 receiver is activated. This causes gate L46 to be open passing a one pulse (1P) through the inverter and buffer system K45, J45, and H45. Of the gate tubes B to L42 only K42 is open. Thus the one pulse passes this gate to the inverter K44 and appears on the ninth channel of the output plug.

(2) -1 receiver is activated. This causes gates B45, G to K46 to be opened. Gate G46 passes the nine pulses (9P) through the buffer and inverter system F45, E45, D45, and E45 to the gate tubes B to L 43. Since all these gate tubes except K43 are open nine pulses appear on all channels except channel nine (including the PM channel). The gates H to K 46 pass the 2P, 2'P, and the 4P through the buffer and inverter system K45, J45, and H45 to the gate tubes B to L 42. Since only K42 is open this gives eight pulses on channel nine. The gate B45 passes the 1'P directly to the inverter B44 of channel one. Thus, before the 1'P arrives the quotient has received the number

M98999 99999.

After the 1'P arrives the accumulator has received the number

M99000 00000,

which represents the number -01000 00000.

(3) +2 receiver is activated. The gate L46 is open. This gate passes the 2P to the buffer and inverter system and then to the gates B to L 42. Gate L42 passes these pulses into channel nine.

(4) -2 receiver is activated. Gates B46 and C to K 47 are open. L47 passes nine pulses into the PM channel and through all the gates B to L 43 except L3. Gates H, J, and L47 pass the 1P, 2P, and the 4P to give seven pulses through gate L42 into the ninth channel. B46 passes the 1'P into the first channel. Before the 1'P arrives the denominator accumulator receives

M97999 99999.

After the 1'P arrives the denominator accumulator has received

M98000 00000,

which represents the number -02000 00000.

The quotient place ring is stepped by a 1'P passing gates F6 and L45. Gate F6 is open except in period III (the round-off period) and gate L45 is opened once each shift cycle.

The quotient place ring also performs a second function. Suppose the places switch is set at eight. Then, when the quotient place ring reaches stage seven (there may be eight digits in the quotient) the gate A41 (just under the place source circuits) will conduct turning the inverter I5C off and opening gate I2. After the add-subtract cycles corresponding to this position of the quotient place ring have taken place (producing possibly an eight digit quotient or before now, the next shift cycle starts. At this time the output of gate I2 passes gate I2 setting the place source flip-flop (I4, 5). This closes the

gate F6 and thus the quotient place ring is stepped no farther, even though the shift of the number in the numerator accumulator takes place. This means that the number which may be added or subtracted as a result of the round off procedure is put in this same place (that is, in channel three).

6.4. EXAMPLES

The following table gives the setting of the program control switches in the different examples:

	Example 1	Example 2
Numerator receiver switch	α	α
Numerator clear switch	C	C
Denominator receive switch	β	0
Denominator clear switch	C	0
Interlock switch	I	NI
Answer disposal switch	1	1
Round-off switch	RO	RO
Root-divide place switch	D 8	R 10

6.4.1. A division example

Addition and pulse time	Discussion
0.17	Program pulse arrives at buffers 67, 68, and 69. The output of buffer 67 activates the D_β receiver. The output of buffer 68 activates the N_α receiver. The output of buffer 69 activates the transceiver in the divider. The output of the cathode follower 64 opens the gate A41. One of the buffers 61 gives a signal through the interlock switch to open the gate L48. The other buffer 61 gives a signal through the root-divide and round-off switch to open gates K5 and K6.

Addition and pulse time	Discussion
1.1 to 1.10	The numerator and denominator accumulators are receiving the numerator and denominator. (It is assumed that the program pulse which activates the divider is used to cause the transmission of the numerator and denominator from whatever units contain them.
1.17	A general pulse (gated CPP) passes gate K6 to provide the first division pulse (DP). This DP passes gate A10 to step the program ring to stage B. The output of stage B opens gate D6. During this time the PM static lines from the numerator and denominator to the sign indication circuits are setting up.
2.17	Another DP steps the ring to stage 1 causing gates B8, A7, and B7 to open. A general pulse (GP) passes gate D6 which may or may not step the numerator ring and/or the denominator flip-flop depending upon the signs of the respective quantities.
3.17	A GP passes gate A7 clearing the program ring back to stage A. A GP passes gate B7 setting the flip-flop A, B 6 closing the gates A10 and A11. A DP is passed by gate B8 producing a first P pulse. This P pulse activates the N_α receiver and either the D_A or the D_S receiver (depending upon the signs). Activating the N_α receiver causes gate L10 to open. Say that the signs are alike then the D_S receiver will be set and thus gate G11 opened.
4.17	A DP passes gate L10 and activates the receiver Q_γ. This causes gates D11 and D12 to be opened. A DP passes gate G11 setting the +1 receiver. A GP passes the buffer C5 and resets the N_α and the D_S receivers.
5.1	Gate L46 passes a one pulse (1P) which passes gate K42 to go into the ninth decade of the quotient accumulator.
5.17	A DP passes the buffer C12 to reset the +1 receiver. The Q_γ receiver is reset by a CPP. Assuming there has been no over-draft gate D9 passes a GP to produce the next P pulse. This P pulse sets the N_α and the D_S receivers.
6.17	Same as 4.17.
7.17	Assuming there has been an over-draft the gate E9 passes a GP which sets the N_γ and the S_α receivers. This causes gates L45, K7, and L1 to be opened.
8.1 to 8.9	The numerator is being transmitted to the shift accumulator.

Addition and pulse time	Discussion
8.10	A 1'P passes gate F6, L45 and steps the quotient place ring to stage 2. The numerator accumulator clears.
8.17	A CPP passes gate K7 activating the $S_{\hat{A}}$ and N_{α} receivers. The activating of receiver N_{α} opens the gate C9.
9.17	A GP passes gate C9 to produce a P pulse. This starts an add cycle (since the numerator ring has been stepped). That is, this P pulse activates the N_{α} and the D receiver. Activating the $D_{\hat{A}}$ receiver causes gate H11 to be opened.
10.17	As in 4.17 the Q_{γ} receiver is activated and a DP passes gate H11 to set the -1 receiver.
. . . . .	. . . . .
0.10	A 1'P passes gates F6 and L45 to step the quotient ring to stage 7. The N_{α} and $S_{\hat{A}}$ receivers are set. Gate A41 begins to conduct opening gate E6.
1.17	Gate C9 passes a GP to provide a P pulse which activates the N_{α} and the D_S receivers.
2.17	A DP passes gate L10 setting the Q_{γ} receiver. A DP passes gate G11 setting the +1 receiver. Assuming there has been an overdraft gate D12 begins to conduct opening gate E9.
3.17	A DP resets the $\pm$1 receivers. A GP passes gate E9 activating the S_{α} and the N receivers. This pulse from E9 passes E6 to set the pulse source flip-flop E 4, 5. Thus, this is the last addition time in which general pulses (GP) and therefore division pulses (DP) are produced. As before the output of the S_{α} receiver opens gates K7, L45, and L1.
4.10	Gate F6 is now closed so no 1'P is passed.
4.17	CPP's pass gates K7 and L1 to set the $S_{\hat{A}}$ and the N receivers and to step the numerator ring, respectively. A CPP passes gate F5 to produce the first IIIP pulse. This IIIP pulse goes through the buffer A12 to step the program ring to stage B. It also passes gate K5 to produce a round-off pulse (ROP).
5.17	An ROP pulse (a IIIP gated by K5) passes gate C8 to produce a P pulse which activates the N_{α} and $D_{\hat{A}}$ receivers. A IIIP pulse passes the buffer A12 to step the program ring to stage 1.

Addition and pulse time	Discussion
6.1 to 6.9	The denominator is added to the numerator.
6.17	A IIIP pulse steps the program ring to stage 2. The N_a and D_A receivers are not reset since there are no GP's to pass the buffer C5.
7.17	A IIIP steps the program ring to stage 3.
8.17	A IIIP steps the program ring to stage 4.
9.17	A IIIP steps the program ring to stage 5. This opens the gate D4.
10.1 to 10.10	The denominator is added to the numerator for the fifth time. Suppose that this does not produce an overdraft in which case gate K12 remains open.
10.17	An ROP pulse passes gate D4 to reset the N_a and the D_A receivers. A IIIP steps the program ring to stage 6, opening gates E3 and J13.
11.17	An ROP pulse passes gate J13, K12 (assuming there was no overdraft), and gates J8 and J10. The output of J10 sets the Q_y receiver. The output of J8 is passed by gate F8 or G8 depending upon the signs and sets the +1 or the -1 receiver. A IIIP steps the program ring to stage 7. A CPP passes E3 to reset the pulse source flip-flop.
12.1 to 12.10	+1 or -1 is added into one decade of the quotient accumulator.
12.17	A CPP passes F4 and K6 to produce a DP which resets the +1 or the -1 receiver. A CPP passes L50 to set the flip-flop K, J 50.

. . . . . .

(Wait for interlock pulse)

0.17	Interlock pulse (program output pulse of some other unit) turns on one of the buffers F 46-48 and G48 setting the flip-flop H, J 48.

Addition and pulse time	Discussion
1.17 (13.17)*	A CPP passes J49 and H50 to set the flip-flop G, F 50 and reset K, J 50. Flip-flop G, F 50 causes gate 62 in the transceiver to open.
2.10 (14.10)	The carry-clear gate passes gates A48 and A49 and appears at terminals on the front panel.
2.17 (14.17)	A CPP passes F49 to produce the C1 and C1' pulses. The C1' pulse does the following (1) passes gate L48 to reset H, J 48. (2) passes buffer A8 to clear the programming (3) passes buffer F3 to reset the pulse source flip-flop E 4, 5. (4) passes buffer C13 to reset the D_γ receiver (E, F10, F11, E11, E12) and the ± 1 receivers. The C1 pulse does the following (1) the flip-flop A, B 6 to reset. (2) resets the denominator flip-flop C 1, 2. (3) turns off the inverter K2 clearing the numerator binary ring. A CPP passes gate 68 in the transceiver resetting it and being transmitted. A CPP passes D46 to activate one of the answer disposal transceivers.

6.4.2. A square root example

Addition and pulse time	Discussion
0.17	Program pulse arrives at buffers 67, 68, and 69. The output of buffer 68 activated the N_α receiver, and the output of 69 activates the transceiver in the divider. The output of the cathode follower 64 opens the gate A43. One of the buffers 61 gives a signal through the interlock switch to open the gate K49. The other buffer 61 gives a signal through the root divide and round-off switch to open gates K3 and K4.

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*Read this time if interlock signal arrives before completion of division process.

Addition and pulse time	Discussion
1.1 to 1.10	The radicand accumulator (same as numerator) is receiving the number to be square rooted.
1.17	A GP (A CPP passes by gate F4) passes gate K3 to produce the first square root pulse (SRP). This SRP passes gate A11 to step the program ring to stage B, opening gate D6.
2.17	Another SRP steps the program ring to stage 1 causing gates A7, B7, K8, and G7 to open. A GP passes D6 but has no effect on the denominator flip-flop since the denominator contains the number +00000 00000 at this time. If the radicand were negative the binary ring would be stepped.
3.17	An SRP pulse passes gates K8 and G7 setting the D_y and the +1 receivers, respectively. A GP passes gate A7 clearing the program ring back to stage A. A GP passes gate B7 setting the flip-flop A, B 6 causing the gates A10 and A11 to close.
4.17	The output of the D_y receiver passes gate D11, opens gate D9 which allows a GP to be passed producing the first P pulse. This P pulse activates the N and the D_S receivers (since the denominator consists of +1 in a certain decade).
5.1 to 5.10	The +1 in the denominator is subtracted from the radicand.
5.17	A GP resets the N_a and the D_S receivers (from buffer C5). An SRP passes gate L9 to set the D_y receiver and gate G12 to activate the +2 receiver.
6.1 to 6.10	+2 is added into the denominator giving 3.
6.17	A CPP resets the D_y and the +2 receivers. Assuming there is no overdraft gate D11 is conducting and thus, D9 passes a GP to produce the next P pulse.
7.17	An SRP activates the D_y and the +2 receivers. Assuming there is an over-draft this time gate D12 conducts opening gate E9.
8.17	A GP passes gate E9 and sets the S_a and N_a and D_y receivers, and it passes gate G9 to set the -1 receiver.

Addition and pulse time	Discussion
9.I to 9.10	-1 is added to the +5 that was in the denominator accumulator. The radicand is transmitted to the shift accumulator. A'P steps the quotient ring.
9.17	A CPP passes K7 to activate the S_{Δ} and the N_{α} receivers and passes gate L1 to step the numerator ring.
10.1 to 10.10	-1 is again added to the +40 in the denominator accumulator giving +39. The radicand is transmitted back (through a shifter) to the numerator accumulator.
10.17	A GP passes gate C11 to reset the D_{γ} and the -1 receivers. A GP passes gate C9 to produce another P pulse.
. . . . .	. . . . .
0.10	A 1'P passes gates F6 and L45 to step the quotient ring to stage 9, causing gate A43 to conduct and, thus, opening gate E6.
0.17	The S_{Δ} and N_{α} receivers are set by a CPP through gate K7. The numerator binary is stepped to minus (a minus radicand)
1.17	A GP passes gate C9 to produce a P pulse. This pulse activates the N_{α} and the D_{β} receivers.
2.17	An SRP passes gates L9 and G12 to set the D_{γ} and the +2 receivers, respectively. Assuming there has been an overdraft gate E9 opens.
3.17	A GP passes gate E9 activating the S_{α} and the N_{Δ} receivers, and passes gate E6 to set the pulse source flip-flop E4, 5. Thus, this is the last addition time in which GP pulse, and therefore, SRP pulse will be produced.
4 to 11	What happens during these addition times is exactly a repetition of what happens in the case of division (explained in example 1).
12.17	A CPP passes gates K49 and H50 (opened by the program ring being at stage 7) and sets the flip-flop G, F 50.

Addition and pulse time	Discussion
13.17	A CPP passes gate F49 producing C1 and C1' pulses. The C1 pulse resets the coincidence flip-flop G, F 50, and clears the quotient ring and the numerator ring. The C1' pulse clears the program ring, resets the pulse source flip-flop (E 4, 5), and resets the D_y and the +1 and -1 receivers. The C1 pulse resets the flip-flops A, B 6, and C 1, 2. The output of the coincidence flip-flop causes the gate 62 in the activated transceiver to conduct, which in turn opens the gates B48, one of the gates C46, D46, D47, or E47 (for answer disposal), and gate 68 in the transceiver.
14.10	The carry-clear gate passes gate B48 and clears the numerator accumulator.
14.17	A CPP passes gate 68 and is transmitted as an output program pulse. A CPP passes gate D46 and activates the first answer disposal receiver.

VII FUNCTION TABLE

There are three function tables in the ENIAC; each stores the values of a function for 104 values of the argument. Associated with each function table is a portable function table supporting an array of switches on which the operator can set the values of the function. For each value of the argument the portable table has twelve digit switches and two PM switches (thus, the portable table has 1248 digit switches and 208 PM switches).

Panel #2 (the right hand panel) contains eight master digit switches and two master PM switches. These are for setting any digits (as many as eight) that are the same for all values of the argument. The PM master switches can be used when all function values set up in the table are of the same sign, making it unnecessary to set the PM switches of the table.

Thus, altogether, for each value of the argument there are twenty digits (eight of which are the same for all arguments and twelve of which can vary from argument to argument) and two PM signs (determined either by the master PM switches or by the settings of the various PM switches on the portable table). The two PM signs enable the operator to set up the values of two functions for each argument allotting the twelve variable digits and the eight master digits to the two functions in any manner. This allotting of digits to the two functions requires special adapters at the two function table outputs (see Section 11.6.5.).

Four of the master switches (A_1 to A_4) feed lines 7 to 10 of the A output. Master switches B_1 to B_4 feed channels 7 to 10 of the B output. The PM_1 master switch feeds the PM channel of the A output and PM_2 master switch feeds the PM channel of output B. The left hand six columns of switches on the portable table feed channels 1 to 6 of the A output. The right hand six columns

of switches feed; the lines one to six on the B output.

If one desires to transmit any other combination of these channels into one digit trunk then the appropriate adapter must be constructed (see Section 7.3.9.).

The function table transmits in five addition times the functional value (or any of four neighboring functional values depending upon the setting of the argument switch—this is for interpolation purposes). By using the repeat switch the function table may transmit the functional value n times ($1 \leq n \leq 9$) in $n+4$ addition times.

7.0. INTRODUCTION

In the upper right hand corner of the block diagram PX-7-304 appear the switches of the portable function table. In the upper left hand corner are the units and tens argument rings. Between these and the table switches are the table input gates or table selectors. Below the argument rings (left center of the diagram) is the program ring, and below this, two program control circuits (there are nine other program control circuits) are illustrated. At the bottom center of the diagram are the pulse gates which pass combinations of the 1, 2, 2', 4, and 9 pulses to make up pulse representations of the digits 0, 1, 2, ..., 9. To the right of this are the master switches (which are used to set up digits which do not change for all 104 values of the argument) and in the right hand corner are the transmitter circuits.

The table output gates and all circuits below them (on the diagram) including the pulse gates are located on the right hand panel (panel #2) of the function table. The switches (in the upper right corner) are on the portable unit. All other circuits (including the rings, the flip-flops, and the program

control circuits) are located on the left hand panel (panel #1) of the function table.

There are three complete function tables. Each one is identical with the others so anything said in the following discussion applies to all three.

For purposes of discussion the circuits of the function table are divided into three types. The program control circuits comprise the eleven transceivers and their associated switches. The common programming circuits comprise the program ring and its associated gates, the argument flip-flop, the subtract flip-flop, and the add flip-flop. The balance of the circuits make up the numerical circuits. The numerical circuits include the argument rings, the table input gates, the portable table, the table output gates, the pulse gates, the constant switches, PM master switches, delete switches, subtract pulse switches, and the output transmitters.

7.1. THE PROGRAM CONTROL CIRCUITS

7.1.1. The Transceivers

There are eleven transceivers located in the #1 panel of the function table. These are standard, that is, they are exactly the same as those used in the accumulators and most other units of the ENIAC.

7.1.2. The Argument Reception Switch.

The buffer which feeds this switch (that is, the cathode follower in the transceiver) serves two functions, namely, to control the transmission of the argument and the stepping of the program ring. The argument reception switch has three possible settings controlling the reception of the argument from some other unit of the ENIAC. On all three settings the fast buffer out-

put (tube 64) of a transceiver goes to gates D49, E49, or F49, one of which passes central program pulses which step the program ring. If the switch of the activated program control circuit is set on NC, a central program pulse passed by gate J48 (opened by stage -3 of the program ring so that J48 is open at the beginning of the program) will turn inverter H48 off, and pass gate H46. The pulse will then go through the transmitter J-L 46, and appear on the front panel (terminal labeled NC, see PX-7-302). From there it can be taken (via jumpers and program trays) to some other unit of the ENIAC to program the argument transmission. If the switch were set at C the action would be similar except the output pulse would pass gate H47 and be transmitted from the transmitter J-L 47. Supposedly, the NC circuit would be used when the argument is not to be cleared in the transmitting accumulator, and C is to be used when it is to be cleared.

These circuits are controlled by the fast buffer outputs (tubes 64 and 65) of the transceivers. Since these outputs have a small time constant the input circuits to the gate tubes have extra capacity purposely added. This delays the opening of these gates; keeping them from opening in time to pass part of the same CPP which activated the transceiver.

7.1.3. The Program Switch.

Deck 1 of the program switch determines whether plus or minus the functional value is to be transmitted. When set on A (add), and a program control is activated, the output of tube 61 in the transceiver causes the inverter E48 to stop conducting, opening the gate E47. When the ring is in stage zero this gate passes a pulse which sets the add flip-flop (tubes C46, 47). If the program switch is on S, then inverter E48 (the other triode) stops conducting, opening gate E46. Then, when the ring is on stage zero the subtract flip-flop

D46, 47 is set. The timing of these operations is illustrated in section 7.2.1.

Deck 2 of the program switch determines whether the functional value itself or one of the four neighboring values is to be transmitted. If the reader will check the connections from the argument rings to the switches of the table he will note that the table number is exactly two less than the number registered in the argument rings. Thus, if x denotes the argument then normally the function table would transmit f(x-2). The number transmitted and the corresponding setting of the program switch is as follows:

Program switch setting	Number transmitted	Number in argument rings
-2	f(x-2)	x
-1	f(x-1)	x+1
0	f(x)	x+2
+1	f(x+1)	x+3
+2	f(x+2)	x+4

If the program switch is set at +1, for example, gates H44 and J44 will be opened by the output of the buffer 61 of the transceiver. When the program ring is at stage -1 gate E42 will be opened and three pulses will pass H44 and J44 through the inverter E44 and gate E42 and into the units argument ring. This changes the argument from x to x+3 and the function table will now transmit f(x+1). Note that stage -1 of the program ring must open gate E42 in time to pass a 1P. Since the gate is physically close to the ring there is no difficulty in doing this with the usual two to one safety factor.

7.1.4. The Repeat Switch

This switch determines how many times the functional value is transmitted. If it is set at 3 (as illustrated) the functional value will be transmitted once when the ring is set at stage one, again at stage two, and the third time at stage three. The output of stage three (which is now positive) will go through terminal three on the repeat switch and open gate 62 in the transceiver. This causes the inverter 65 to go off and opens gate 68 giving an output program pulse at the end of this addition time. The output of the buffer 69 turns off the inverter D48 opening gates A48, B48, and C48. These pass central program pulses (CPP) which clear all three rings and reset all three flip-flops.

Thus, the functional table will transmit a functional value n times in n+4 addition times where n is any number between one and nine. Note that the accumulator which is to receive the function must be programmed to receive during either the whole n+4 addition times, or during the last n of the n+4. Consequently, if it is programmed simultaneously with the function table, it can receive the function only 5 times using a single transceiver. If, however, it can be programmed 4 addition times later than the function table, the setting of its repeat switch can be the same as that of the function table, and the function table can transmit to it the full 9 times.

7.2. THE COMMON PROGRAMMING CIRCUITS

7.2.1. The Program Ring

The program ring is a thirteen stage ring located on the left center of the block diagram. The following table illustrates what happens at each stage of the ring.

TABLE 7-2

Addition Time	Ring Stage	Effect
0	-3	Program pulse is received at a transceiver.
1	-3	At pulse time seventeen of this addition time the ring steps to stage -2, and, (depending upon the setting of the program switch), a pulse may be transmitted by J-L 46 or J-L 47. Usually the pulse transmitted here will be used to program the argument transmission from some other unit of the ENIAC.
2	-2	The buffer K48 will go on turning the inverter L48 off, opening the gates D42 and H42; allowing the argument to be received.
3	-1	Depending upon the setting of the program switch certain of the gates F44 to L44 may have been opened. Thus, from zero to four pulses are passing the inverter E44 and at this addition time these pass the gate E42 and enter the units argument ring. Gate F47 is also opened, allowing a 1' pulse to set flip-flop B46-B47; this flip-flop, through buffer A46, turns off inverters B1 to L1 and A11, in turn permits one of the table input gates to conduct and energize one entry of table.
4	0	The output of the zero stage opens the gate G48. At pulse time seventeen of this addition time a central program pulse (CPP) passes this gate, turning off the inverter F48. Depending upon the setting of the program

TABLE 7-2 CONT'D.

		switch, either gate E46, or E47 is open. Thus, the output of the inverter F48 sets either the add or the subtract flip-flop causing either the function value or minus the functional value to be transmitted during addition time 5 (and subsequent addition times for repeat switch settings above 1).
5	1	Certain of the pulse gates are opened during this addition time, and the functional value is transmitted over the digit output (SX and SY in lower right hand corner). The output of stage 1 of the program ring connects to terminal 1 on all the repeat switches.
6	2	The functional value is transmitted a second time.
7	3	The functional value is transmitted for the third time, and (if the repeat switch is set on three as illustrated) gate 62 is opened in the transceiver. Then buffer 63 turns off inverter D48 opening gates A48, B48, and C48, causing the rings to clear and the flip-flops to be reset.

7.2.2. The Argument Flip-Flop

The argument flip-flop B 46-47 is set by a 1' pulse passing gate F47. This gate is opened when the program ring is at stage -1. When the flip-flop is set it turns on buffer A47 which turns off the inverters B1 to L1 and A 11. This determines the time at which one of the table input gates conducts.

7.2.3. The Add and Subtract Flip-flops and the Pulse Gates

The following table gives a list of the gates opened and the effect when the add or the subtract flip-flop is set.

TABLE 7-3

Channel	Add						Subtract					
	1P	2P	2'P	4P	9P	Total pulses	1P	2P	2'P	4P	9P	Total pulses
0	-	-	-	-	-	0	-	-	-	-	L'4	9
1	K'4	-	-	-	-	1	-	K'1	K'2	K'3	-	8
2	-	-	J'2	-	-	2	J'4	J'1	-	J'3	-	7
3	H'4	-	H'2	-	-	3	-	H'1	-	H'3	-	6
4	-	-	-	G'2	-	4	G'4	-	-	G'3	-	5
5	F'4	-	-	F'3	-	5	-	-	-	F'2	-	4
6	-	E'1	-	E'3	-	6	E'4	-	E'2	-	-	3
7	D'4	D'1	-	D'3	-	7	-	-	D'2	-	-	2
8	-	C'1	C'2	C'3	-	8	C'4	-	-	-	-	1
9	-	-	-	-	B'4	9	-	-	-	-	-	0

The outputs of the pulse gates go to transmitting circuits, (amplifiers) (tubes B' to L', 5 to 10). The outputs of these transmitting circuits go to the various table output gates, the zero-nine channels go to the P and M terminals on the PM master switches, and through buffers B'63 to L'63 they all go to various terminals on the constant switches.

7.2.4. Use of the Function Table for Programming:

The function table can be used to obtain program pulses on any of as many as 14 channels when a particular program control circuit is excited. The choice of output channel is controlled by any two digits of the number used as an argument, and registered in the argument accumulator.

To accomplish this, an adapter must be used in back of the function table on the cycling unit trunk. This adapter (PX-4-119) adds a central program pulse to the 9P lines of the function table panel #2.

Now, suppose that all the switches, on the portable table, for a particular argument are set to one; with the exception of one switch, which is set to "nine". Whenever the function table is programmed and the appropriate argument is stored in the argument accumulator a CPP will be transmitted over the channel corresponding to the switch which was set to "nine."

The nine pulse lines are used for this purpose since they also feed the PM switches. Consequently, the portable table can be used to give output pulses on any of fourteen channels (that is, twelve digit channels and two PM channels).

7.2.5. Initial Clear

The initial clear gate opens gates A48 to C48. The output of C48 resets the argument flip-flop (B46-47) and the add and subtract flip-flop (C46-47 and D46-47). Gates A48 and B48 operate in parallel to turn off three inverters A49 to C49. A49 and B49 in parallel cause the argument rings to clear. C49 causes the program ring to clear.

If the buffer 63 in any transceiver conducts, (as it will at the end of an operation for which its program control was activated), the inverter D48 stops conducting, opening the gates A48 to C48 giving the same effect as the initial clear gate.

7.3. THE NUMERICAL CIRCUITS

7.3.1. The Argument Rings

When the gates D42 and H42 are opened (at stage -2 of the program

ring) the two digits of the argument arrive over channels five and six of the input terminal and going through the pulse standardizers (J-L 42 and A41, B-C 42) step the units and tens rings to the proper position. When the program ring reaches stage -1, zero to four pulses may be passed by one of the gates F44 to L44 through gate E42, to step the units ring the corresponding number of positions. If this causes the units ring to step through stage nine gate A42 will be opened to pass the carry over pulse. This pulse goes through the inverter and buffer G42 and steps the tens ring one place. Note that the tens ring has eleven stages; also there is never any delayed carry-over problem. The argument will never exceed nine in the tens place but the carry over may give ten, thus, the extra stage.

Consider the control of the table selectors by the rings. After clearing (as illustrated) the rings each set at stage zero. This causes the inverters K2 and K26 to be non-conducting. Suppose that a program control is activated, and the argument is zero. Then when the argument flip-flop is set the inverter L1 conducts raising the potential of both grids of the table input gate (or table selector) K12. Incidentally, one control grid of several other table input gates will swing positively at this time, (for example, gates K13, K25, and K11, and others not illustrated), but since the other grid remains below cut-off, (because other inverters associated with the tens ring remain on), the tubes do not conduct. A similar statement is true for the gates A to K 12.

Thus, when the program ring is at stage -1, one of the table input gates begins to conduct and one of the horizontal buses of the portable table has a negative swing of potential.

The action of these inverters and gates is explained in some detail in section 1.2.3.)

7.3.2. The Table Input Gates

There are 104 table input gates corresponding to the argument values of -2, -1, 0, 1, 2, ..., 100, and 101. This gives a range of argument values of 0, 1, ..., 99 with the extra values on each end for purposes of interpolation. Of the two control grids of each gate tube, one connects to the output of an inverter controlled by the proper stage of the units ring, and the other control grid connects to the outputs of two inverters; one controlled by the tens ring, and the other by the argument flip-flop. In order for any particular gate tube to conduct all three inverters must be non-conducting. Thus, even though the argument arrives in the rings earlier, none of the table input gates conduct until the argument flip-flop is set at stage -1 of the program ring. Note that this flip-flop is set by a one primed pulse (1'P). The timing here is illustrated by table 7-4.

TABLE 7-4

Addition Time	Pulse Time	Activity
0	17	Programming pulse arrives at the function table.
1	17	Argument transmission is programmed and receiving gates (F47, D42) are opened.
2	17	Program ring steps to stage -1 opening gates E42 and F47.
3	1 to 5	Argument adjustment takes place by 0, 1, 2, 3, or 4 pulses passing gate E42.
	10	Argument flip-flop is set by 1'P.
	17	Program ring steps to stage 0 opening gate G48.
4	17	Program ring steps to stage 1 opening gate 62 in the transceiver (provided the repeat switch is at one) and a control program pulse passes gate G48 to set the add or the subtract flip-flop.
5	1 to 10	Functional value is transmitted.
	17	Control program pulse passes gate 68 in the transceiver to be transmitted and to reset flip-flop. CPP also passes gates A48, B48, and C48 to clear rings and reset flip-flops.

7.3.3. The Portable Table

The portable table is a switching network built as a separate unit, and connects to the function table unit through two IBM type plugs. Since the portable table is on wheels, the operator may quickly interchange it with one connected to any other function table.

Each portable table mounts 208 PM (sign) indication switches (two for each argument value) and 1248 digit switches (12 for each argument value). There are 104 PM switches and 624 digit switches on each side of the portable table.

7.3.4. Table Output Gates

The nine terminal on each of the 104 switches in the sixth column of the portable table connects to the inverter B'11. The output of this inverter goes to the gate B'12, which when opened will pass either nine or zero (no) pulses depending on whether the associated program control is on add, or subtract program respectively.

The ten positions of the switches in each column go to ten inverters. Each output from the ten inverters goes to one grid of ten gates, the other grids being fed by the pulse gates.

Thus, if horizontal bus 11 is energized and the sixth column digit switch is at 7 (as illustrated) the inverter D'11 will cease conducting and the gate D'12 will open. This gate will then pass 7 or 2 pulses depending upon the setting of the argument switch of the associated program control circuit.

There are 120 inverters and 120 output gates on the digit channels. The two PM channels feed four more inverters and gates (C' to K' 61).

The outputs of the digit gates (labeled A5 to A10, and B5 to B10) go through inverters and buffers to transmitters, (these transmitters use a

6L6 in place of the usual 6V6) and then to terminals SX and SY. The outputs of the PM gates go to the PM master switches (PM_1 and PM_2 associated with the A and the B outputs respectively).

7.3.5. The PM Master Switches

The PM master switches make it possible to determine the sign for all the table entries at once instead of setting the individual PM switches on the portable function tables. This is useful only if all entries are of the same sign.

There is a PM master switch associated with each output (SX and SY). These switches determine the sign indication transmitted on the channel of the respective outputs. Each switch has three settings, Table, P, and M. The following table gives results of various settings of these switches.

Master switch setting	Pulses transmitted over the PM channel	
	Add flip-flop set	Subtract flip-flop set
P	0	9
M	9	0
Table	0 or 9 depending upon the setting of the corresponding PM switch on the portable table.	

7.3.6 The constant switches and the delete switches

There are eight constant switches, four associated with each of the outputs SX and SY. If the first few digits of a function are the same for all arguments used, these switches simplify the procedure for setting up the values of the function. Therefore, when some program control is activated the numbers set on these constant switches (or complements) will be transmitted over the corresponding channels regardless of the value of the argument.

The outputs of the transmitters associated with the pulse gates comes through buffers B'63 to L'63 to ten of the positions on each of these

switches. Two other terminals on each of these switches make available the outputs of the two PM master switches here. This is to help provide the proper complements.

The delete switches are provided on each of these channels in case the operator desires to transmit nothing on one or more channels.

7.3.7. The Subtract Pulse Switches

Since the complementation provided by the add or subtract flip-flops and pulse gates gives complements with respect to $10^n - 1$, it is necessary to provide a correction pulse to get complements with respect to 10^n. The correct pulse switches enable the operator to provide this correction pulse in any of six channels on each output, namely, A5 to A10 and B5 to B10.

The output of the subtract flip-flop goes through the inverter D45 to the gates A'64. The 1'P is passed by these gates through the inverter A'63 to the buffers A'61, A'62 to L'62.

These subtract pulse switches enable the operator to divide the 12 variable digits set up on the portable table into arbitrary groups and cause each group to give complements with respect to 10^n.

7.3.8. The output transmitters

The outputs of the constant switches go through the delete switches directly to transmitters. The outputs of the table output gates go through an inverter and a buffer to transmitters. Special adapters can be easily built to rearrange the outputs and allow transmission onto a single digit trunk.

If the operator desires, for example, to set up a ten digit function on the table and his function is such that the constant switches cannot be used then six of the digits can be obtained from channels A5 to A10. The other four must come from four of the channels B5 to B10 and a special adapter must

be used to get these ten digits onto one digit trunk.

7.3.9. Adapters

In designing an adapter for use on the function table outputs there are two points to watch. First, the function table outputs (which are to be used) are connected in a one-to-one manner to terminals corresponding to the trunk lines to be used. Secondly, if negative numbers are to be transmitted, then any unused lines, corresponding to accumulator decades between the PM unit and the first decade used, must carry 9 pulses in order to give the proper complements. This second objective can be accomplished by connecting the outputs of some of the master digit switches (A_1 to A_4 or B_1 to B_4) to the corresponding lines. The PM_1 and PM_2 positions of the master switches provides 9 pulses at the proper times.

If for any reason the master digit switches cannot be used for this purpose the adapter can be made to transmit the number onto the trunk using only channels adjacent to the PM line (line 11). In this case a shifter can be used on the input to the accumulator. The shifter provides for the extra "nines" needed for complementing purposes (see section 11.3.)

VIII. THE CONSTANT TRANSMITTER AND IBM READER

The constant transmitter stores eighty digits on relays and twenty digits on constant set switches. Provision is made for twenty PM signs, sixteen associated with the numbers stored on relays and four associated with the numbers set on the switches. One of these PM signs is associated with each five digits. Thus, the constant transmitter can store twenty five-digit numbers and their proper signs. Provision is made to associate certain groups in pairs to form ten digit numbers. In one addition time the constant transmitter can transmit to some other unit of the ENIAC any group of five or certain groups of ten digits and the associated sign.

Whenever it is desired to set up new constants on the relays in the constant transmitter, the IBM reader must be programmed to read a new card. This does not change the digits set on the constant set switches; these have to be changed manually.

The reader completely reads a card and stores the information on relays in the constant transmitter in 0.48 seconds. After about 0.3 seconds the starting circuits of the IBM reader are reset and will be able to remember a second signal to read (generally this fact is insignificant since computations cannot be started until the initial data is read into the constant transmitter and, also, there is no program output from the reader to start any computation until the end of the reading cycle). If in some manner it is arranged to program the next reading of a card before the first cycle is completed (this must not occur before say 0.4 seconds after the initial read program and this only allows a 33% safety factor) then, due to the clutch not dropping out, the reader will read a card in 0.36 seconds.

Thus, the reader can read normally as many as 125 cards per minute not allowing for any computations in between. On the other hand, since each IBM time unit corresponds to about 170 addition times, and there is an interval of about 1.2 units between the finish pulse and the dropping of the holding cam contact, it seems that even though the output of the reader is used to reprogram the reader that this same pulse can be used to cause transmissions from the constant transmitter safely (safety factor = 2:1). During the period of 100 addition times after this pulse, numbers could be transmitted from the constant transmitter. By the device mentioned above the speed of reading can be increased to as much as 160 cards per minute.

The description given here will be in terms of the following diagrams: 1) Constant Transmitter Cross Section PX-11-116, 2) Constant Transmitter Block Diagram PX-11-307, 3) Constant Transmitter and Reader Cross section, and 4) IBM Reader Diagram PX-11-119. The discussion will be divided up into the following sections: 1) Constant transmitter program controls, 2) IBM reader program controls, 3) Numerical circuits of the constant transmitter, 4) IBM reader, and 5) Examples.

8.1. CONSTANT TRANSMITTER PROGRAM CONTROLS

8.1.1. The groups of numbers

As indicated above the constant transmitter stores twenty five-digit numbers and as many as twenty PM signs. These are divided into five-digit groups called A_L, A_R, B_L, B_R, ..., H_L, H_R, J_L, J_R, K_L, and K_R. The first sixteen groups A_L to H_R are read from IBM cards while the last four groups J_L to K_R are set on the constant set switches.

8.1.2. Transceivers

There are thirty transceivers in the constant transmitter. These are associated in groups of six. The first six transceivers control the first four five digit groups of numbers A_L to B_R. The next six control the groups C_L to D_R, et cetera. Finally, the last six transceivers control the groups J_L to K_R which can be set on the constant set switches (see panel two of constant transmitter, PX-11-303).

Two transceivers of a group of six are illustrated on PX-11-307. These are for programs numbered one to six and control the first four five-digit groups of numbers. The output from the cathode follower (tube 64, see PX-5-30) of each transceiver connects to two decks of the associated constant selector switch. The cathode follower is used to drive the switch because fast operation of the circuit is required to make possible transmission of a constant during the addition time following the addition time in which the program pulse is received. The other outputs of the transceiver are unused.

8.1.3. The Program Control Circuits

Associated with the relays of groups one to four (likewise for five to eight, nine to twelve, and thirteen to sixteen) there are eighty-eight gate tubes. In each group there are four gate tubes for each of the five digits (as the 1, 2, 2', and 4 coded system is used to form the digits) and two gates associated with the Pm indication. There are six constant selector switches associated with each such set of 88 gate tubes (switches one to six with groups one to four, for example). The output terminals of these switches go directly to the grids of the gate tubes.

Switches 25 to 30 are associated with the gates controlled by the constant set switches on panel two of the constant transmitter. There are only

64 gates associated with these switches since the gates associated with the correction pulse are omitted. (This means that the operator sets up complements here as complements with respect to 10^n and not 10^n-1).

Whenever a program pulse is received on the input terminal of a program control, at H say, the output of the cathode follower (tube 64 in the transceiver plug-in unit) goes to the two decks of the constant selector switch. The results of the various settings on this switch are given in the following table.

TABLE 8-1

Constant Selector Switch	Result	
	Deck 1	Deck 2
A_L	The cathode follower potential opens the PM gates A'1 and A'21.	The cathode follower potential opens the digit gates for group 1, that is gates B' to L', 1 and 21.
A_R	Gate A'41 (PM) is opened.	The PM gate A'62 and digit gates B' to L', 41 and 61 are opened. (A'61 controls the correction pulse).
A_{LR}	The PM gate A'1 is opened.	The PM gate A'62 and the digit gates B' to L' 1, 21, 41, and 61 are opened.
B_L	The PM gates A'2 and A'22 are opened.	The digit gates B' to L' 2 and 22 are opened.
B_R	The PM gate A'42 is opened.	The PM gate A'63 and the digit gates B' to L' 42 and 62 are opened.
B_{LR}	The PM gate A' 2 is opened.	The PM gate A' 63 and the digit gates B' to L' 2, 22, 42, and 62 are all opened.

Since the constant selector switches are connected in parallel, within any group of the same alphabetical letter "back circuits" would be created

should one switch be turned to L or R when another is turned to LR. For example, in the first group of six constant selector switches, if one is set at A_{LR}, no other can be set at A_L or A_R without transmitting superfluous digits (in the case of a positive number), or the extraneous transmission of 9P and 1'P over certain channels (negative number). This means that if the number stored on groups one and two relays is transmitted as a ten digit number, then at no other place in the computation can it be considered two five-digit numbers, or vice versa.

If an activated program control has its switch set to A_L, the five digits of group one will be transmitted on channels 6 to 10. If the number is negative nine pulses will be transmitted over the PM channel (A'1 turns off the inverter A'11 opening the gate L43) and the correction pulse will be transmitted over channel 6 (A'21 turns off the inverter A'11 opening the gate E45). In this case nothing is transmitted over channels one to five.

If an activated program control has its switch set at A_R the five digits of group 2 will be transmitted over channels one to five. If this number is negative nine pulses will be transmitted over channels six to ten and over the PM channel (A' 41 turns off the inverter A'51 opening the gates F to K 45 and L44) and the correction pulse will be transmitted over channel one (A'62 turns off the inverter A'61 opening the gate A45). The nine pulses transmitted over channels six to ten give the complement with respect to 10^{10} and make it unnecessary to use a shifter in the digit transmission line.

If an activated program control has its constant selector switch set at A_{LR} the ten digits of groups one and two will be transmitted over channels one to ten. If the number is negative nine pulses will be transmitted over the PM channel (A'1 turns off the inverter A'51 opening the gate

143) and the correction pulse will be transmitted over channel one (A'62 turns off the inverter A'61 opening the gate A45).

The groups one to sixteen (or A_L to H_R) behave in a manner similar to above. The gates associated with the constant set switches (J_L to K_R) behave similarly except for the correction pulse (as explained above, or see Section 8.3.2.).

8.2. Reader Program Controls

The reader program controls are located in the initiating unit (see PX-9-307). The IBM reader can be caused to read a card, (provided certain conditions are fulfilled in the reader), either by a program signal arriving at terminal Ri on the front panel (PX-9-302) or by pushing the reader start button on that panel.

8.2.1. Starting

If the reader start button is pushed the resulting pulse goes through the special pulse standardizer (61 and 62, reader start unit, see PX-11-307). The output of the special pulse standardizer turns off the inverters 63 causing the buffer 72 (PX-9-104) to go on. This sets the flip-flops (65, 66) and(67, 68). The driving tube 64 goes on closing the starting relay (located in the constant transmitter (Panel #3). If a program pulse is used to start the reader it comes in over Ri turning on the buffer 67 and setting the flip-flop (65, 66), but not the flip-flop (67, 68).

8.2.2. Resetting

After the reader starts to read the card a signal (a gate voltage) comes back over connection 129 (see PX-11-307) from the reader causing the flip-flop 65 and 66 to reset. This signal occurs early in the card reading cycle (when the minus indication is being read—before the digits are read

(see the cam time-table on PX-11-120). After this reset signal has arrived any subsequent program pulse arriving over R_1 sets the flip-flop and closes the starting relay. This causes the reader to continue and read the second card before stopping. The reset signal arrives from 800 to 1200 addition times after the print program signal.

8.2.3. The Finish Signal

Just as the IBM reader finishes reading the card a signal is sent over connection 127 to the special pulse standardizer (65, 66) causing the flip-flop 70 and 71 to be set. This opens the gate 69 and if the flip-flop 67 and 68 is then set the inverter 61 (Px-9-106) will go off opening the gate 62. The CPP passed here sets the flip-flop 63 and 64 opening gate 68. This passes a CPP which goes through the transmitter (65-67) to the reader program output R_0. This same pulse goes through the inverter and buffer 69 and resets all three flip-flops.

The flip-flop 63 and 64 is a synchronized flip-flop, that is, it is set by a CPP gated by 62. The flip-flop 70 and 71 is not synchronized since it is set by a signal from the IBM reader. Thus, the gate 62 may be opened in such a way that it will pass only part of a CPP. If it fails to set the flip-flop 63 and 64 no harm is done since the next CPP will also be passed by 62 and will set the flip-flop 63 and 64. This flip-flop being set by a CPP will open the gate 68 in ample time for the next CPP. This arrangement insures that a standard synchronized program pulse is transmitted out or R_0.

8.2.4. Interlock

Since the process of reading a card takes a very large number of addition times it is desirable to be carrying on part of the computation while this is being done. There will be a place in the sequence of computations

where the numbers in the constant transmitter are used for the last time. At this addition time the reader may be programmed to read the next card. Since, generally, it will not be known which process, that of reading the next card or that of completing the rest of the sequence of computation, will be finished first, an interlock feature is provided. The final output program pulse of the sequence of computation is plugged to R_1. Thus, flip-flop 67 and 68 is set at the end of the sequence of computations while flip-flop 70 and 71 is set when the reader is finished. Only when both of these things have happened will the gate 69 conduct and open the gate 62, finally giving a program pulse out of R_0.

The reader start button through buffer 64 also sets the interlock flip-flop (67 and 68). Therefore, when the reader start button is pushed the reader reads a card and a reader program output pulse is obtained at R_0 at the proper time.

The initial clear gate causes all of these flip-flops to be reset. Note that when the ENIAC is turned on the starting flip-flop (65 and 66) may come on in the set position and before a CPP arrives to reset it the reader may read one card.

8.3. NUMERICAL CIRCUITS OF THE CONSTANT TRANSMITTER

The numerical circuits of the constant transmitter comprise the sixteen groups of storage relays and their associated gates (A' to L' 1 to 10, et cetera), the constant and PM set switches (on panel 2) and their associated gates, the inverters (A' to L' 11, et cetera) and the pulse gates (A to K 41 to 44; A, E to K 44; L 43 and 44), and the inverters, buffers and transmitters (A to L 46 to 50).

8.3.1. The Storage Relays and their Gates

This description of the storage relays will be given in terms of the constant transmitter cross section drawing PX-11-116. On that drawing there appears a wiring diagram of group one relays, a schematic diagram of group one relays, a coding cam time table, and a cross section of the electronic circuits.

As the IBM card goes through the reader the positions on the card pass under the reading brushes in the following order (see the cam time table PX-11-120 or the small table on PX-11-116).

12, 11, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9,

There are eighty columns on the card and all of these pass under the reading brushes at once. Punches in the 11 position will be used to indicate minus signs, while punches in, say, position four represent the digit four in that column.

To simplify the following discussion it will be assumed that leads numbered one to eighty of the Reader connections go directly to the corresponding reading brush. Actually, these eighty connections may be made in any desired manner simply by rewiring the plug-board on the Reader, see PX-11-305.

The relay labeled R_{AB} (schematic diagram of group one relays, PX-11-116) is a PM isolating relay which handles the first three groups (A_L, A_R, and B_L). Referring to PX-11-120 it is seen that cam C89 makes contact during the reading of the eleven position on the card. If there happens to be an 11 or 12 punch in whatever column the minus indication for group one is placed, say column one, a circuit will be made through connection 97, contact R_{AB}, and the pick-up coils of relays PM_1 and PM_2. When these relays are picked up they are held by a contact on PM_2. This holding is controlled

by connection 81 (for group one) and lasts at least (it may last longer, see Section 8.4.5.) until the next card has begun to be read.

The following table gives the various combinations of coding relays that are closed during the various positions of the card reading.

TABLE 8-2

Card position	12	11	0	1	2	3	4	5	6	7	8	9
With no minus indication				C_1		C_1		C_1		C_1		C_1
					C_3	C_3			C_3	C_3	C_3	C_3
											C_5	C_5
							C_7	C_7	C_7	C_7	C_7	C_7
With minus indication			C_1		C_1		C_1		C_1		C_1	
			C_3	C_3	C_3	C_3			C_3	C_3		
			C_5	C_5								
			C_7	C_7	C_7	C_7	C_7	C_7				

The reader can check this table in the following manner. If the number is positive the coding relays C_1 to C_8 are connected in pairs to the coding cams CB2, CB4, CB6, and CB8. The coding cam time table shows that as position seven of the card, for example, is under the reading brushes coding cams CB2, CB4, and CB8 are making contact. If seven was punched in the first column storage relays 1-A, 1-B, and 1-D will be activated through the contacts on coding relays C_1, C_3, and C_7. Contacts on the storage relays will cause gate

tubes L'1, K'1, and K'21 to be opened ultimately causing the 1, 2, and 4 pulses (altogether seven pulses) to be transmitted over channel ten. If there had been a minus indication punch the PM relays (PM_1 and PM_2) would be closed (and held by the circuit through connection 81) and the coding relays would be connected to coding cams CB1, CB3, CB5, and CB7. If again, seven were punched in the first column, only cam CB3 is making contact when the seven passes under the reading brushes and the contact on C_3 causes storage relay 1-B to be picked up. Ultimately, this causes the two pulses (complement of seven) to be transmitted over the tenth channel. Since the PM relays are closed, a contact on PM_1 causes gates A'1 and A'21 to be opened. These gates provide (for a five digit number) for the minus indication (nine pulses on the PM channel) and for the correction pulse (to give complements with respect to 10^n).

8.3.2. The Constant and PM Set Switches

PX-11-307 shows that these switches connect directly to the gates for the numbers J_L to K_R. Only the switches for the first and tenth digits are drawn out in detail for the groups J and K. There are four PM switches, so these twenty digits can be used in groups of five and the signs of any one group set independent of the others. If they are to be used for ten digit numbers then both PM switches (J_L and J_R, for example) must be set to P or to M depending upon the number.

The constant set switches consist of four parts mounted on two decks. The moving portion makes contact in such a manner as to open the 1, 2, 2', and 4 gates in various combinations corresponding to the digit to which the switch is set. The gates opened by various switch settings is indicated by the crosses in the following table.

TABLE 8-3a

Gates	Switch Setting									
	0	1	2	3	4	5	6	7	8	9
1		X		X		X		X		X
2			X	X			X	X	X	X
2'									X	X
4					X	X	X	X	X	X

In the case of negative numbers read from cards the coding relays automatically take the complements with respect to 10^n-1. This is not true of the constant set switches for groups J_L to K_R, that is, in setting up a negative number on these switches the operator must take the complement himself. No correction pulse is provided by these PM switches so negative numbers are set up as complements with respect to 10^n. The following table illustrates various switch settings.

TABLE 8-3b

Number to be set up	PM Settings		Switch Settings									
	J_L	J_R	1	2	3	4	5	6	7	8	9	10
+23456 on J_L and +78901 on J_R	P	P	2	3	4	5	6	7	8	9	0	1
-12345 on J_L and +78901 on J_R	M	P	8	7	6	5	5	7	8	9	0	1
12345 on J_L and -78901 on J_R	P	M	1	2	3	4	5	2	1	0	9	9
12345 67890 on J_{LR}	P	P	1	2	3	4	5	6	7	8	9	0
-12345 67890 on J_{LR}	M	P	8	7	6	5	4	3	2	1	1	0

8.4. THE IBM READER

The IBM Reader will be described in terms of the wiring diagram M-11-119. At the top of this drawing are tables which give the locations of the relays and cams. Note that the various parts of one relay (for example, the hold coil, pick-up coil, and various contacts) may be located in widely different places on this drawing. The tables at the top locate all of these parts. The terminal posts are located in the panel behind the motor generator. The connections to the IBM plug (which plugs into a socket on the constant transmitter panel number three) are pictured in the upper right corner of the drawing.

8.4.1. The a-c Circuits

The Reader receives its a-c power by a standard 110 volt plug which plugs into a socket on the bottom of panel three of the constant transmitter. Power is furnished to this plug only when the ENIAC is turned on, plugs at the bottom of other panels, except printer panel #2, have power on them all the time. The a-c power goes through a switch located on the Reader to the motor-generator and through contacts (on H. D. relay at 1A) on a relay (pick-up coil at 2B) to the drive motor. Thus, when the power comes on the motor generator starts up. When it reaches speed the 40 volts d-c cause the green light (on the front of the Reader) to come on and the H. D. relay to close starting the drive motor. The H. D. relay prevents the drive motor from operating in case of failure of the motor generator.

8.4.2. Starting circuits

When cards are initially placed in the magazine, the magazine card lever contact (Mag. at CLC at 2B) is closed. This causes Relay R-1 to pick-up. At this time neither the auxiliary read switch nor the ENIAC starting relay

(in the constant transmitter, see PX-11-307) can cause the reader to operate since Relay 2 is not activated.

If in this case, the initial start key is pushed, the reader will operate, (assuming card stacker switch closed, that is, there are not too many cards in the card stacker) and feed a card into position before continuous roll #1 (that is, in position ready to be read by the control #1 reading brushes). When the card is in position here, relay R-2 is activated by card lever contact #1. Now either the auxiliary read switch or the ENIAC starting relay can cause a card to be read. The initial start switch, since relays R-1 and R-2 are each activated, cannot cause a card to be read at this point. Thus, upon closing either the auxiliary read switch, or the ENIAC starting relay the card passes under the #1 (control) reading brushes and stops in position before the #2 read brushes.

If any of the control arrangements (like plugging to control hubs on the plug-board) are being used the "control" instructions are now remembered by certain relays in the Reader. Note, that this memory depends upon the 40 volt output of the motor-generator on the reader.

With the first card in position before the #2 read brushes, a card lever contact (CLC #1) causes R-60 to be activated. If the auxiliary read switch is again operated this card will be read by the #2 read brushes and the (signed) numbers stored in the constant transmitter relays.

In practice the relay timing is such that in initially placing cards in the reader (by placing cards in the magazine and depressing the initial start key)the reader may feed cards up to position before the #2 read brushes by running through two cycles. In this case it is ready to immediately read the first card. If the first card was fed only into position before the #1 or control

brushes (one cycle) no harm is done. If the reader is now programmed to read, relay R-60 being open, it will read the 1st card by the control brushes and no reset or finish signal will be given out. Then, the starting relay still being closed, the reader will immediately start another cycle in which the first card passes under the #2 brushes. When the cards are in position, relays #1 and #2 are activated by the card contact levers, (Magazine CLC., CR. #1, CR. #2) and the start key becomes ineffective. After relays #1 and #2 are activated, contacts on them (at 3B) enable the auxiliary start key to cause a card to be read. A starting relay located in the constant transmitter (see PX-11-307) has a contact connected in parallel with this auxiliary start key. A unit located in the initiating device (described in 8.2.) causes this starting relay to close and thus causes the reader to read a card.

8.4.3. Numerical Circuits

There are two sets of 80 reading brushes, the first (#1) are the control brushes and the second (#2) are the ones which read the numbers and their signs. The number two reading brushes (at 6B) read the numbers and PM signs on the cards and via connections on the plug board carry the corresponding signals to the storage relays in the following ways:

(1) Directly to the storage relays (hubs located at 6D).

(2) For a column in which the PM punch occurs the connection is from the reading brush hub to one of the PM hubs (labeled "minus control" on the plug-board) (at 6D on PX-11-119) and from the other PM hub to the corresponding storage relay hub.

(3) Or, if desired, the connections from the reading brushes to the storage relays may be by way of the group selector relay contacts (at 6B and 6C). In this manner certain control punches may cause information from one set of reading brushes to go to either

one of two sets of storage relays, or such control punches may cause one set of storage relays to receive information from one of two sets of reading brushes (see Sections 8.4.4. and 8.4.5.)

8.4.4. Group Selection

There are sixteen five-pole, double-throw relay switches (relays R24 to R55, two relays to each switch, hold coils at 4C and 5C, contacts at 6B and 6C). The coils at 4C and 5C serve for picking up and for holding. These five-pole, double-throw switches may be used to rearrange the information coming into the storage relays. These relays are picked up by contacts on relays 7 to 22 (at 4C and 5C) in series with the cam P6. Once they are picked up they are held by cam P7.

Referring to the cam time table (PX-11-12C) we see that relays 7 to 22 may be picked up any place in the card cycle, that is, from any punch (since cam P5 makes contact all this time). If any of these relays have picked up, cam P6 will cause the corresponding relays 24 to 55 to pickup at the end of the card cycle. Once they are picked up cam P7 holds them until the end of the next card cycle. Since the card going under the control brushes will go under #2 read brushes exactly one card cycle later, this means that a group selection control punch will activate the group selection relays during the time the card is passing under the #2 read brushes.

8.4.5. Reset Control and Reset Shunt

The storage holding relays (contacts at 7B, pick up coils at 3C) 4, 5, and 6 cause the relays in the constant transmitter to hold their information. The time table shows that cam CB10 causes these relays to hold from position 12 on one card until 13.7 on the next card. That is, the information read from one card is normally dropped out at the beginning of the reading of the next card.

By plugging from the reset control hubs to the reset shunt the corresponding constant transmitter relays can be caused to hold their information until such time as the relays 56 to 58 are activated.

By proper plugging on the plug board connection can be made from the #1 read brushes through the pick up coil of relay 23 to the digit selector. When relay 23 is activated relays 56 to 58 will be picked up by cam P8 at 8.5 in the card cycle. A contact on relay 57 and cam P1 causes relay 59 to pick up at 9.5 in the card cycle. This is shown on P -11-308.

Suppose that reset control is operated from a "three" punch in some column in what will be called a master card. Cards without this "three" punch (in that same column) will be called detail cards.

At the end of a cycle in which such a master card passed under the control (#1) brushes relays 23, 56 to 58, and 59 have all picked up. During the next card cycle the master card will pass under the #2 read brushes. Relay 59 holds until near the end of this cycle preventing either a reset or a finish signal. Inspection of the reader starting circuit on PX-11-307 shows that the starting flip-flop (65,66) is still set and that the starting relay is still activated so the reader immediately goes on to read another card. The relays which are shunted (by plugging reset control to reset shunt on the plug board) will hold the information read from the master card until another master card comes along. New information will be put into the other relays for each detail card.

8.4.6. Coding Cams

The coding cams are located at 6A and 7A on PX-11-119. They directly operate the coding relays located in the constant transmitter. See 8.3.1.

8.4.7. Reset Signal

Cam P4 produces the reset signal at time 12 in the card cycle. This signal will be sent to the constant transmitter (actually to the initiating unit) only if relay 60 is activated and relay 59 is not. Relay 60 is activated only when cards are in position at the #2 read brushes (see CR#2 at 3B, that is, continuous roll #2). Relay 59 is activated only when a "master" card (a card with a punch operating reset control relay 23) is at the #2 read brushes.

8.4.8. Finish Signal

Cam P3 produces the finish signal at time 9.5 in the card reading cycle. As with the reset signal this signal is obtained only if relay 60 is activated and relay 59 is not.

IX. PRINTER AND IBM GANG PUNCH

The printer causes eighty digits and as many as sixteen PM signs which are stored in certain accumulators and possibly the master programmer to be punched on IBM cards. In the case of complements (which represent negative numbers) the printer relays cause the IBM punch to punch the true negative number and a corresponding sign indication (an 11 punch).

When operating continuously the IBM punch can punch a card in 0.61 seconds. However when starting from rest, the inertia of the punching mechanism makes the punching time 0.82 seconds. The units of the ENIAC associated with the printer (eight accumulators, say, and five decades of the M.P. do not have to wait while the complete punching cycle takes place but only 0.4 seconds. If the punch is programmed before the end of the first cycle to punch a second card then the two cards will be punched in 1.4 seconds. However, if the second program signal comes anytime after the first cycle is completed the punch essentially loses a cycle (because of the clutch dropping out) and the punching of two cards will take at least 2.0 seconds.

Therefore, if there is no more than approximately 2,000 addition times between printing programs, the punch will punch almost 100 cards per minute. A small increase in the number of addition times between printing programs will cut this down to not more than 50 cards per minute. It should be emphasized that while all these figures are valid at the time of writing, they may vary with time, temperature, punch wear, and so forth.

The program control circuits for the printer are located in the initiating unit. When programmed to print, the IBM punch will start, the

relays in the printer will be set up by the static outputs of the various decades and Pii units, a reset signal will come from the punch to the program control circuit, and the punch will complete the punching cycle. The reset signal can be used to continue computation in the ENIAC. Since the set up time of the relays is small compared to the time for punching a card this arrangement prevents undue waste of time while the card is being punched. When the card punching cycle is completed an interlock signal comes from the punch to the printer allowing the relays to set up anew provided another print program signal came along in the meantime. This constitutes a mechanical interlock arrangement.

On the printer there are sixteen "print" switches which enable the operator to print or not print any one of sixteen groups of five digit numbers and the associated Pii indication. There are sixteen coupling switches which make possible the printing of groups with ten or more digits. These coupling switches serve no purpose when printing positive numbers. In printing negative numbers they take care of the carry over in the process of taking the complements and also gang the Pii relays for the coupled groups.

The description of the printer will be given in terms of the following drawings:

Printer Cross Section	PX-12-115
Printer Block Diagram	PX-12-307
IBM Gang Punch	PX-12-112

The discussion will be divided up in the following manner: 9.1, Program Control Circuits, 9.2, Numerical Circuits of the Printer, 9.3, IBM Gang Punch, and 9.4, Examples.

9.1 PROGRAM CONTROL CIRCUITS

The printer program control circuits comprise most of two plug-in units in the initiating device (PX-9-104 and PX-9-105) and the printing switches located on panel two of the printer. The circuits located in the initiating device are represented in block diagram form on PX-12-307 (lower left corner) or PX-9-30, and in detail on PX-12-115.

9.1.1 The Printing Switches

The printing switches simply disconnect the power (+200 v line) to the digit and PM relays of each group. Thus, if the print switch for a particular group is set at "off", the relays of that group cannot pick-up and thus nothing will be punched in the corresponding position on the card.

9.1.2 Starting Circuit

Any pulse arriving at the printer program input terminal P_1 (see PX-9-302) will (through the buffer 67) set the flip-flop (68 and 69). This causes the driver 70 (which has its cathode at +20 volts, and has the starting relay as its load) to come on, closing the starting relay (located in the printer panel No. 3). This flip-flop will be reset by a signal arriving from the punch through the buffer 72. (It can be reset by an EC, see Section 9.1.5.)

9.1.3 Reset and Program Output

After the printer relays have set up, (these relays set up when the interlock cam makes contact and the starting relay is activated) near the beginning of the card punching cycle (at card time 11.2) the reset signal will arrive at the printer from the punch. This signal passes through the special pulse standardizer 61 and 62 (in unit PX-9-105, see PX-12-307; for a description of this circuit see Section 1.2.7). The

utput of this pulse standardizer sets the flip-flop 64 and 65 and also through the inverters 63 provides a reset signal for the starting flip-flop described above.

The flip-flop 64 and 65 opens the gate 66 passing a CPP which sets the flip-flop 67 and 68. The output of this flip-flop gates a CPP (gate 69) which resets the two flip-flops passing through the transmitter 0 to 72, and appears at the printer output terminal P_o on the initiating nit front panel (see FX-9-302). At the time of writing this report, tarting with the punch at rest about 1900 addition times elapsed between reception of a program pulse at P_1 and the output program from P_o. is time will probably vary with respect to temperature and age of the ch among other things.

This double flip-flop arrangement is a synchronizing device. ce the timing of the reset pulse depends upon the mechanical operation the punch it will generally not be synchronized with the CPP in the C. The output of the gate 66 will be synchronized, but it cannot be mitted since the flip-flop 64-65 may be set at such a time that it ld pass a substandard pulse. If the CPP passed by 66 is weak and does set the flip-flop 67-68 no harm is done for the next CPP (64-65 is reset in this case) will be standard and will set 67-68. The circuits rising these flip-flops and their associated gate tubes are relatively w (the rise time is on the order of 50 μ seconds). Thus, if a CPP sets flip-flop 67-68, the gate 69 will open only in time to safely pass the which arrives one addition time later, and the output of gate 69 will be a standard pulse. Note that this program output occurs before ard punching cycle is completed (assuming the punch starts from rest

and at the time of writing this report this time was approximately 1950 addition times).

9.1.4 The Interlock Cam

The interlock cam makes contact near the end of the punching cycle (card time 13.3) and breaks near the P1 punch of the next card cycle (time 12.8) (see the time table on PX-12-307). This cam and a contact on the starting relay (in series) connect the cathodes of all the tubes in the printer to +20 volts. When this circuit is open the cathodes rise (see the 2K, 10 watt resistor near the starting relay on PX-12-307) to about 200 volts. Since this is about the same potential as the plates, any signal on the grids (and generally there will be signals on certain of the static outputs) will not cause any of the tubes to go on and set up their corresponding relays.

The printer may again be programmed to print any time after the reset signal has arrived (see Section 9.1.3). However, except for the activation of the starting relay, nothing will happen until the end of the cycle which the punch is in; until the interlock cam makes contact. This furnishes a mechanical interlock arrangement. The second print signal cannot cause any tubes to conduct and relays to set up in the printer until the first punching cycle is complete. At time 9.5 in the first cycle, the holding cam breaks contact releasing all relays in the printer. At time 13.3 the interlock cam makes and (provided the start relay is activated) the printer relays set up in the new way and a second card is punched.

Table 9-1 gives the timing of the printing sequence.

TABLE 9-1

Mt. Time	Time secs.	Card Time	Activity
0	0	D	Printer program pulse arrives (at initiating unit). Starting relay closes (in printer). IBM punch starts and relays set up.
		13.6	Carry-over cam makes
		14.5	Holding cam makes.
		12.8	Interlock cam breaks (this turns off all tubes in printer and, thus, releases the accumulators and master programmer for other activities).
		11	PM indications are punched.
1900 to 2000	.4	11.2	Reset cam closes causing 1) Starting flip-flop to reset 2) Printer program output pulse to be transmitted. ENIAC proceeds with other computing
		11.8	Reset cam breaks.
		0	
		1 to 9	Digits are punched.
		9.36	Carry-over cam breaks.
		9.45	Holding cam breaks
850	.6	13.3	Interlock cam makes. Relays will set-up again as soon as starting relay is closed. Note that the next printing signal may arrive any time after the reset cam breaks, that is, any time <u>after</u> 11.5.
		D	Punch stops unless starting relay has been closed.

Clearly, the programming in the ENIAC must not be arranged so that a second print program input pulse arrives at P_i before the reset signal has been given out by the punch and the flip-flop 68-69 has been reset. Hence, no pulse should be supplied to the printer program input until after a pulse has been omitted from the printer program output P_o. Any pulse arriving after the reset signal but before the end of the card punching cycle (that is, during the period 11.2 to D) will be remembered and will cause the punch to continue and punch the next card.

9.1.5 Initial Clear

The only place that the initial clear gate is used in the printer circuits is to reset the starting flip-flop 68-69 (PX-9-104 in the initiating unit). The characteristics of the tubes in these circuits are such that whenever the power is turned off or turned on (in spite of the automatic initial clear) the starting relay will be closed long enough to cause the punch to feed a card through.

9.2 THE NUMERICAL CIRCUITS OF THE PRINTER

Of the sixteen relay groups, groups one and sixteen and parts of groups two and fifteen are represented on PX-12-307. Assume that the plug-board is so wired that the columns (A, B, C, D, and E) correspond to the first five columns on the IBM card. Suppose, furthermore, that the PM indication for this five digit group is to be punched in column one or A.

There are fifty digit triodes in group one (actually 25 6SN7's) and three PM triodes. The grids of these tubes connect directly by a 51 line cable to the static outputs of the decades and PM unit of an accumulator. Just one PM line goes to the three grids of the PM tubes.

The tubes in each column are denoted by A0 to A9, B0 to B9, et cetera; that is, the second symbol denotes the digit represented by that tube being on. The grids of these tubes are connected to the normally negative outputs of the stages of the decade rings. The PH line in the cable goes to all three PH tubes (the tubes driving the carry-over relay C_0, and the PH relays H_1 and H_2).

The leads from the emitter arrive at the upper left corner of PL12-307. These emitter leads go through transfer contacts on the relays H_1 and H_2 to the various digit levels in the five columns of relays.

All the digit and PH relays have holding contacts connecting them to a line controlled by the holding cam. The holding cam makes at the beginning of the punch cycle (at IBM time 14.5, see Table 9-1) and breaks at the end of the cycle (at 9.45). These holding contacts cause any relays which are picked up by tubes conducting to remain up until the end of the cycle. Thus, the printer tubes need to conduct only long enough to safely pick up the relays. This determines the length of contact made by the interlock cam (13.3 to 12.8) (note that if the punch stops between cycles then the tubes begin to conduct at time D = 13.5 when the starting relay is activated). Once the relays are picked up the tubes can be turned off by the interlock cam and all the units which connect statically to the printer groups whose print switch is "on" can then be released to participate in further computations.

If the interlock cam has made contact and the starting relay is closed, then one digit relay (in each column) picks up, corresponding to the actual number registered in the decade of the accumulator or master programmer. All three PH relays will pick up together if the number is negative.

Suppose the number P12345 is registered in the decades and Pi unit of an accumulator associated with group one relays. If the print switch of group one is set to print and the starting relay is closed (assuming the interlock cam is making contact) then the tubes A1, B2, C3, D4 and E5 will conduct closing relays A1, ..., E5.

As the card passes under the puncher, pulses arrive from the emitter over the emitter lines. Since the above number was positive all three Pi relays (C_0, H_1 and H_2) are unactivated. This means that there is a connection from emitter line "one" through the transfer contact on H1, through the contact on A1 to the transfer contact on C1, and on to the punch magnet (via the punch plug board) for column one on the card. Thus, when the one position on the card is under the first column punch a signal from emitter line "one" will (through this circuit) cause "one" to be punched in the first column of the card. The circuits for the above number and for M12378 are illustrated by the rows in the following tables. In these tables (A) denotes that the relay is in the abnormal or activated position while (N) means that the relay is in the normal position.

The resistance-capacitance circuits found on the contacts of the carry over relays (and on one contact of the starting relay) are to prevent arcing at the contacts. The protection is necessary only on contacts which carry relative heavy loads, and not only prolongs the life of the relay but provides more reliable operation.

In the case of the number M12370, the minus indication will cause relay C_0 to be activated which in turn (assuming the coupling switch 1-2 is set to "0") causes C_5 to operate. Since the last digit is zero, relay E0 (group 1 relays) will be activated which will cause C_4 to operate.

TABLE 9-2

Circuits For The Number P12378

Emitter Line	P1 relay transfer contact	Digit relay contact	Carry-over relay transfer contact	Line to punch magnet (via plug-board)
1	M1 (N)	A1	C_1 (N)	1
2	M1 (N)	B2	C_2 (N)	2
3	M1 (N)	C3	C_3 (N)	3
7	M2 (N)	D7	C_4 (N)	4
6	M2 (N)	E8	C_5 (N)	5

TABLE 9-3

Circuits For The Number M12378 (-87622)
(Relays C_0, C_5, M_1, and M_2 are now activated, C_1 to C_4 normal, Coupling Switch at 0.)

Emitter Line	P1 relay transfer contact	Digit relay contact	Carry-over relay transfer contact	Line to punch magnet (via plug-board)
8	M_1 (A)	A1	C_1 (N)	1
7	M_1 (A)	B2	C_2 (N)	2
6	M_1 (A)	C3	C_3 (N)	3
2	M_2 (A)	D7	C_4 (N)	4
2	M_2 (A)	E8	C_5 (A)	5

Note: In the above tables (N) means the relay is in normal or unactivated position while (A) means it is in the abnormal or activated position.

The carry relays C_1, C_2 and C_3 will not be activated so the circuits take complements with respect to ten (modulo ten) in the units and tens place and with respect to nine in the other places.

It is essential that the carry over cam breaks before the holding cam does. If the holding cam were to break first, then a string of carry over relays which may have picked up would be dropped by the contact on relay C_0 and since the carry over relays which have picked up are connected in parallel the load here would soon burn up the contact on C_0. Since the carry over cam breaks first (at 9.36 as against 5.45 for the holding cam) the contact on C_0 will not be breaking any current.

There is one PI unit in each accumulator and there are two sets of PI relays (one set with each five digit group). Thus, to print ten digit negative numbers the PI static output must be connected to both sets of PI tubes. This is accomplished by the use of an adapter which connects the two PI lines to the one static output. In case of twenty digit operation an adapter must be used to connect the four sets of PI tubes to the PI static output of the left hand accumulator.

The adapters for the ten digit operation are installed in the backs of the respective accumulators. This adapter (see PX-12-114A) is a plug and two sockets; the plug goes into the PI static socket (on the PI-clear plug-in unit) and the two sockets receive the two PI lines of the two static cables. The adapters for more than ten digit operation are best installed in the printer (behind front panel No. 2) (those for ten digit operation could be installed here, too).

To make it possible to print the actual numbers registered in certain decades (regardless of sign) there is a ground lug on the printer

plugs which normally connect to the static PU leads. Another adapter (a socket with a jumper inside, see PX-12-114B) used here grounds the grids of the PU tubes. This prevents them from conducting; if the grids are allowed to "float" the tubes may or may not conduct. Such an adapter must be used, for example, whenever printing numbers from decades in the master programmer.

9.3 THE IBM GANG PUNCH

The IBM gang punch will be described in terms of diagram PX-12-112. This punch was constructed in the following manner: An unfinished standard gang summary punch was removed from the assembly line and certain details, such as cams and column split relays were added to make a punch for use with the ENIAC. This means there is some unused apparatus in the punch; for example, there is a set of control reading brushes and the continuous roller is in for the regular set of reading brushes. This also explains why there are shunts on some relay contacts. The master-detail switch located on the front of the punch simply acts as an on-off switch for the punch magnets ("on" corresponds to "master").

9.3.1 The a-c Circuit

The a-c connection is normally plugged to the outlet on the bottom of panel two of the printer. Power is furnished to this outlet only when the ENIAC is turned on. Outlets on all other panels except panel three of the constant transmitter have power all the time. Thus, if it is desired to operate the punch without turning on the ENIAC one of the outlets of one of the other printer panels may be used.

When the a-c power is turned on H.D. relays No. 2 and No. 3 close starting the motor generator and closing the 40 volt d-c circuit. The

green light on the front of the punch indicates that the motor generator is operating properly. The drive motor is started by the closing of contacts on M.D. relay No. 1. The pick up coil for this relay is in parallel with R9. R9 is picked up by a contact on R10 and another contact on R10 operates the clutch. Thus, relay 10 is the starting relay.

9.3.2 The Starting Circuit

There are three card lever contacts,

1) Die card lever contact (Die CLC)

2) Magazine card lever contact (Mag. CLC)

3) Brush card lever contact (Br. CLC)

which activate relays 1, 3, and 7. These card lever contacts determine if the cards are being fed in properly. There is a die contact which determines if the punch die is in proper position. If the die contact is open, neither the start key on the punch, nor the starting circuits of the ENIAC will operate the punch. The various card lever contacts are bypassed by the start key on the punch. Thus, it can be used to feed the cards into position when they are first put into the magazine.

If the magazine runs out of cards the punch will stop. If the starting relay is closed the printer relays will pick up and the punch will operate the moment new cards are placed in the magazine. The operator should hold down the stop key when putting new cards in this case. Otherwise, the punch may start before the cards are firmly seated and may fail to feed the first card.

To start the punch, the ENIAC completes the circuit from terminals one to eleven. This, through contacts on relays 1 and 3, closes R23. A contact on R23 causes R10 to close. Contacts on R10 cause R9, relay

M.D. No. 1, and the clutch to pick up. Relay 9 and M.D. relay No. 1 are held by R10 and by the continuously running cam (C.R. cam). Relay 10 in turn is held by cam P5. Thus, when the starting relay is closed in the printer, relays 9 and 10 pick up and hold until the end of the card punching cycle. At that time they drop out as does M.D. No. 1. The clutch drops out when relay 10 drops and the drive motor coasts to a stop.

Note that the operator must use the initial start switch to feed cards into position when starting, since with cards only in the magazine the ENIAC starting circuits will not operate.

A card stacker switch opens the starting circuit when too many cards are in the stacker. When the cards are removed the machine will continue to operate in the proper manner.

9.3.3 The Column Splits (PL Circuits)

The pick-up coils of the column split relays are located at 5C on PL-12-112. These relays are activated by cam P2 during the time that the 11 and 12 positions of the card are passing under the punches (actually, from 13.6 until 11.6). The relays act as a sixteen-pole, double-throw switch (see the contacts at 7 and 8 A and B) and connect the punches (via plug-board connections) to the minus indication terminals (at 8D) during the 11 and 12 positions of the card and to the computer result exit terminals (8D) during the rest of the card cycle. This makes it possible to punch a PL indication and a digit of a number in the same column.

9.3.4 The Punch Magnets

The circuits to the punch magnets is completed by contacts on relays 43 to 56. These relays are activated by a circuit through the

master-detail switch (with switch setting on 'master'), a normally closed contact on R14, and cam P12 (makes at 14.3 and breaks at 9.3).

9.3.5 The Emitter

The emitter is located at 10C. It turns in synchronism as the card passes under the punch magnets, that is, the emitter connects to line 3, for example, when position three is under the punches. If the circuit is completed from emitter line three back to the punch magnets then three will be punched.

9.3.6 The Plug-board

Instructions for plug-board connections appear on PX-12-305. The eighty-digit outputs appear on eighty hubs on the plug-board. The eighty punch magnets appear on eighty other hubs. Thus, information can be rearranged on the card in any desired manner.

X. MASTER PROGRAMMER

The master programmer occupies two panels. The two panels are practically identical in function and in appearance. The Block diagram PX-8-304 refers to the left hand panel; however, by changing some of the terminology, it can refer equally well to the right hand panel. Thus, in the following discussion only the left hand panel will be considered. In the left hand panel the decades are numbered from 11 to 20 (reading from right to left as in an accumulator) and the steppers are named A, B, C, D, and E (from left to right). In the right hand panel the decades are numbered from 1 to 10 and the steppers are named F, G, H, J, and K.

10.1. INTRODUCTION.

The Master Programmer contains only program circuits, there being no numerical or common programming circuits. The program circuits will be divided into two types, namely, stepper circuits and decade counter circuits or decade units. The decade counter circuits are represented on PX-8-304 by the ten rectangles along the top of the drawing. The five steppers are represented by the rectangles along the bottom. The decade counter circuits are divided into groups, each group being associated with a stepper. To give flexibility decade associator switches are provided which change a decade circuit from one group to another.

10.2. DECADE COUNTER CIRCUITS.

10.2.1. Decade ring. The decade rings used in the master programmer are ten

ge ring counters located on plug-in units. The clear inverter (tube 1) also located on the same plug-in unit. The pulse standardizer and the ry circuits associated with the ring are on a separate plug-in unit. In t, for each pair of decades the pulse standardizers (21-23 and 25-27) and ry circuits (24, 28-31) are on one plug-in unit.

Provision is made for making static cable connections to any decade g of the master programmer. This would enable the operator, for example, register an independent variable in certain decades of the master programmer to print it whenever desired.

The normally positive outputs of the stages of the decade ring go to respective positions on the six decade switches. The common connection of h switch connects to the grid of the inverter tube B 41-43 for decade 11). there is a coincidence between the setting of any decade switch and the ition of the decade ring the corresponding inverter will be turned off. ce all the switches are illustrated as setting at "7" all the inverters ld be turned off if the decade ring was stepped to stage seven.

The carry circuit. Whenever a decade is stepped to stage "nine" static output causes gate 28 to open. If another pulse is fed into the se standardizer the ring will step to zero and a pulse will pass gate 28 gate 24 for even numbered decades), go through the inverter and buffer 30 thence to an association switch or, in some cases, directly to the input of pulse standardizer for the next decade to the left.

The carry circuit is spread over parts of three plug-in units and, s, necessarily has a very poor time constant. Actually, the rise time for

the circuit comprised of stage nine of the ring and gate 28 on a separate plug-in unit (four times the time constant) - approximately the time for the signal to reach 97% of its maximum amplitude is on the order of one-half an addition time. Thus, any sequence of digit pulses which would produce a carry-over cannot be fed into the decades of a master programmer during any one addition time. There are other situations (see the discussion of clear circuits below) where digit pulses cannot be fed into these decades.

The clear circuits. This ring is cleared by a CPP passing gate B44, for example, and turning off the clear inverter (tube 1) on the decade plug-in unit). This clear circuit is operated either by the initial clear gate arriving at the buffer B45, say, or by the operation of one of the coincidence gates (B, C, 48-50) in the stepper circuits (E). Generally, one of these coincidence gates will conduct when there is a coincidence between the position of the stepper ring, the settings of a number of decade switches and the position of the corresponding decade rings.

Since the clearing is accomplished by a CPP passing gate B44 (in decade 11) the decade cannot be stepped by any number of digit pulses (arriving over the direct input 11di) which will step it past a coincidence position. This restriction is not because of the time constants. Actually, for the clearing to take place the ring must come to (and stay on) the coincidence position (that is, the position corresponding to one of the decade switch settings) so that gate 63 is set up at pulse time 17; and pulse time 17 is some time (at least seven pulse times) after the last digit pulse arrived. In fact.

dit pulses should not be used to step this ring to a coincidence position. e rise time of this clearing circuit, (as well as the stepper clear circuits) on the order of one-half an addition time (10 pulse times). Thus, the circuit an be expected to operate satisfactorily only when stepped to the coincidence sition with a program pulse (CPP). Note that the time constant of these ircuits vary considerably depending upon the positions of the association witches and the stepper considered.

Note that there is no provision for delayed carry-over (as in an ccumulator). This means that two associated decades cannot be stepped simul-aneously in a manner which produces a carry-over.

0.3. THE STEPPER CIRCUITS.

0.3.1. The stepper ring. The stepper contains a six stage ring located on plug-in unit. On the same plug-in unit is a pulse standardizer and a set of nverter tubes connected to the outputs of the ring. All of these circuits use he tubes numbered from 21 to 32. The set of outputs of the ring which go hrough the inverters go to two sets of six gates each, B and C 48 to 50 and he gates numbered 61, 65, and 69. The other outputs of the stages of the ing go to the respective positions on the stepper clear switch. The common erminal of this switch goes to gate B47. When B47 is open any pulse arriving rom the inverter 61 and buffer 62 will clear the stepper back to stage one. he stepper will clear to stage one in the following cases:

a) When the initial clear gate is applied, gate C47 opens letting hrough a CPP1 which turns the inverter C46 off clearing the ring.

b) A pulse arriving over the clear direct input (cdi) turns the

uffer B46 on and the inverter C46 off.

c) If the stepper is set at stage five and the stepper clear switch is at five (as illustrated) the gate B47 will be open. A pulse passed by gate 63 or from the buffer 61 on the stepper direct input (di) will turn the inverter 61 off and the buffer 62 on. This will cause the inverter B46 to go off causing the gate tube B47 to conduct. This in turn causes the clear inverter C46 to go off and clear the ring.

The stepper clear circuit. The stepper clear circuits will not operate in one pulse time (the rise time for this clear circuit is about one half an addition time).. This means that the stepper ring can be stepped with digit pulses only if the ring is not stepped onto the coincidence position (that is, onto the stage corresponding to the setting of the stepper clear switch).

The stepper direct input. A direct input (through buffer 61) is provided to step the stepper ring. In this case the associated decade units ring is not stepped and no output program pulse is obtained. Note (above) the restrictions on the kinds of pulses supplied to this input.

The stepper input. The flip-flop (66,67) and the associated gate 69 has a time constant approximately equal to that of the slow buffer output of a transceiver. This means that this input (E_1 for example) must never be pulsed later than pulse time four. That is, it can be pulsed by a CPP, 9P, 1P, 2P, or 3P; but not by 4P, 1'P, or generally by any digit output of an accumulator.

Note that if E_1 and E_{cdi}, for example, are pulsed simultaneously, the stepper will clear first and the output pulse will be from E_1.

2.3.2. The program transmitters.

In the lower right hand corner of the rectangle (PX-8-304) containing the stepper circuits there are six gates and six standard transmitters. One of these gates will be open depending upon the position of the stepper ring. Any pulses arriving from the buffer 70 will be transmitted through one of these channels. In the illustration the stepper is setting at stage one so any pulses from 70 will be transmitted through the left hand gate 61 and will appear on the output terminal E_1o. Note that a lead comes from the master programmer clear (MPC) to all these gate tubes. Inspection of the cross section PX-8-102 shows that this lead goes to the screens of these gate tubes (6SA7's). Whenever the initial clear is activated a relay located in the initiating unit changes these screen voltages from +150 to 0 volts. This blocks these gates, that is, even if a signal arrives on both control grids the tube will not conduct. As explained in section 2.1.2. the effect of the initial clear is to clear decades back to their first stages and let the program circuits run out their sequences. By program jumpers various program controls in the machine may be connected in a sequence that will take several hundred addition times to run out. These sequences may be tied together by the master programmer so they would take a very long time to run themselves out or even repeat indefinitely. To prevent this tying together and, thus, make the time for initial clearing reasonably short the output gates in the master programmer are blocked in this manner. A period of about one half second will be sufficient (including a safety factor) for any possible sequence set up in the other units of the ENIAC to run out, therefore, the initial clear lasts for approximately one half second.

0.3.3. The program receiving circuit.

The input program will ordinarily come in by the terminal Ei causing e buffer 65 to go on setting the flip-flop 66 and 67 . The output then kes a positive swing opening gate 69. The next CPP is passed resetting e flip-flop and turning off the inverter 68. This causes the cathode llower 70 to go on giving a positive pulse to the grids of the gates , 65, and 69. This also turns the buffer A43 on giving a negative pulse the pulse standardizer of decade 11.

As described above, 10.3.2, one of the six gates (61, 65, 69) is open pending upon the position of the stepper. Thus, for every pulse put into Ei pulse is sent into decade 11 and a pulse comes out of one of the terminals o to E_6o. one addition time later.

Pulses fed into Edi cause the stepper to step, and pulses fed into ldi ause the decade to step. Neither of these cause any pulses to be given t at the outputs E_1o to E_6o.

0.3.4. The coincidence gates. The coincidence gates are the tubes B and C to 50 for stepper E. Whenever any one of these gets a signal on both grids e inverter 64 goes off and the gate 63 is opened. This passes the next PP to the inverter 61 and the buffer 62. The output of 62 goes to the ulse standardizer 21, 22, and 23. stepping the ring and it also turns the inverter B46 off. If the gate B47 is open the clear signal from C46 afely overrides the stepping signal from the pulse standardizer and the ring lears back to stage one. Also, a pulse on the clear direct input (edi, B46) r a CPP passed by gate C47 (when initial clear is activated, will safely (that s with adequate safety factor) override any stepping signal.

The output of the stepping gates also goes to the clear circuits in the decade counter causing the decade to clear back to zero. Again, this clear signal overrides any stepping signal.

Stepper E, with the decade associator switch for decade 12 setting as illustrated, has only one decade associated with it. Consider stepper D. This stepper has decades 12 and 13 associated with it. Looking at stepping gate E48 it is seen that one of the grids connects to both the inverter D41 and through the D-E associator switch, to the inverter C41. If either inverter is conducting the grid on E48 will be sufficiently negative to prevent it from conducting. This constitutes a multiple coincidence arrangement. That is, in order for E48 to conduct three inverters must go off, namely, C41, D41, and 2 in the stepper ring unit. Consider stepper C. If five decades are associated with stepper C then in order for the stepping gate G48 to conduct the inverter in the stepper ring unit must go off along with the five inverters in the respective decade units.

Steppers A and F may be used without any associated decades. When the A-B association switch (or the F-G) sets at B the screens of the coincidence gates (L, K, 48-50) are switches from +150 to 0 volts. This prevents any of these gates from conducting and, thus, gate 63 never conducts. This means that the stepper ring can be stepped only by pulses introduced over the direct input. The stepper clear direct input functions as before. Any pulses arriving over the program input will be transmitted over one of the six outputs depending upon the position of the stepper ring.

Any of the other steppers may be made to operate in the above manner by removing the gate 63 in the plug-in unit. Note, that the only difference

is the operation of these other steppers (as compared to A or E) is that certain decades will count the pulses coming in on the stepper program input. These decades will clear at positions depending upon the settings of the decade switches but there will be no corresponding change in the stepper position. This clearing could be prevented and, thus, the total number of program pulses counted by removing the coincidence gates (D, E, 48-50, for example) instead of gate 63.

10.4. ASSOCIATION SWITCHING.

All the decade units are exactly alike, and the stepper units only differ with respect to the number of decades that can be associated with each one. PX-8-304 shows that decade 12 can be associated with either stepper D or E. Decade 14 can be associated with either C or D, decade 18 with either B or C, and decade 20 with either A or B. When decade 20 is associated with stepper B then stepper A has no associated decade (see above)

The decade associator switch is a nine pole double throw switch. The six poles on the left handle the outputs of the inverters associated with the decade switches. The seventh pole takes care of the clear circuit, the eighth the input to the next decade on the left, and the ninth the input of the decade to be associated. In the case of decade 20, since there is no decade to the left, the eighth pole takes care of the input to decade 20, and the ninth pole is used to change the screen bias of the coincidence gates.

Consider the associator switch for decade 12. As illustrated this decade is associated with stepper D. The following table illustrates what happens for the two positions of the associator switch for decade 12:

TABLE 10 - 1

	Associated with D	Associated with E
Outputs of the inverters C41 to C43	Go to stepping gates E and D 48 to 50.	Go to stepping gates B and C 48 to 50,
Decade clear input (to C45)	Goes to the output of the stepping gates E and D 48 to 50.	Goes to the output of the stepping gates B and C 48 to 50.
Input to decade 13	Goes to the carry over circuit of decade 12.	Goes to the buffer A44 of stepper D.
Input to decade 12	Goes to the buffer A44 of stepper D.	Goes to the carry over circuit of decade 11.

Thus, when decade 12 is associated with stepper E, decade 11 acts as a units decade and 12 as a tens decade in counting the number of program pulses coming in at the terminal Ei. Therefore, the two decades can count as many as 99 pulses coming in at Ei. When decade 12 is associated with stepper decade 11 acts as a units decade in counting the number of pulses coming in at E_i and cannot count more than 9 pulses. In this case decade 12 acts as a units decade in counting the number of pulses coming in at Di.

Consider stepper C. If both decades 14 and 18 are associated with stepper C then the five decades (14 to 18) can count as many as 99, 999 pulses arriving at terminal C_i.

XI. THE TRANSMISSION SYSTEM AND SPECIAL DEVICES

This chapter contains a description of the digit and program trunks which carry the pulses representing digits or program signals from one unit to another. Also various special devices such as shifters, deleters, adapters, static cables, and so on, are described in this chapter.

11.1 TRAYS AND TRUNKS

It is necessary to transmit pulses representing digits or program signals from one unit of the ENIAC to another. Furthermore, this must be done in an entirely different manner for each new problem that is put on the ENIAC. Thus, the interconnection systems must be very flexible. For this purpose trays and jumpers are used.

11.1.1 Trays

A tray is essentially an eleven wire transmission line, capable of being connected to other trays and to the digit terminals and program terminals of the various units.

Each tray is eight feet long, nine inches wide, one and a quarter inches deep, and open at the bottom. It contains eleven wires separated from each other by metal shields. The trays are placed on top of one another so that they will actually be shielded on all sides. Each tray is equipped with outlets on each end so that it may be connected to other trays by means of jumpers. It also has outlets every two feet of its length so that it may be connected to the program and digit terminals of the various units of the ENIAC. These outlets are of two kinds:

A digit tray, - shown in drawing PX 4-29, has for each outlet a twelve-contact plug (eleven wires and ground).

A program tray, - shown in PX-4-101, has for each outlet a set of eleven two-terminal plugs (one wire and ground). At each end of the program tray is a twelve contact plug to facilitate its connection by a jumper to another program tray.

These trays are stacked on the front of the various units of the EDLAC, some above and some below the program control panels. Generally, the program trays will be placed below the control panels and the digit trays will be placed above. There is room for about twelve trays to fit above and twelve below the control panel of a unit, although a much smaller number will ordinarily be sufficient.

11.1.2 Jumpers

Cables or jumpers are used to connect the trays to the digit terminals and program terminals. There are two kinds of jumpers. One, a program jumper, consists of a single wire and ground and is used to connect a socket on a program tray to a program socket on one of the units. The other, a digit jumper, has eleven wires and a ground and is used to connect an outlet on a digit tray to a digit terminal of a unit. This last type of jumper is also used to connect trays together.

11.1.3 Trunks and Lines

A single wire and ground, running through several program trays, jumpers or program cables and thus connecting a number of program terminals to one another, is called a program line. A set of eleven wires and ground used to transmit a ten-digit number and its sign and running through several digit trays, jumpers or cables, is called a digit trunk.

One set of digit trays (9) are connected together to form the cycling unit trunk. This carries the various pulses and gates produced by the cycling unit around to the various units of the ENIAC. Nine trays are sufficient here since the printer does not connect to this trunk. See PX-9-307.

11.1.4 Load Boxes

Each wire of a digit trunk and each program line has one load resistor connected to it. These resistors are assembled in boxes, (see PX-4-103) and one box is to be plugged into an otherwise unused outlet at the end of one of the end trays of each set connected together by jumpers. As explained in Section 1.2.8, this makes it possible to have the flexibility of being able to connect varying numbers of digit and program terminals to the trunks and program lines.

11.1.5 Load Units

The pulses and gates transmitted over the trays must have rise times better than 1/2 microseconds. This sets an upper limit to the value of the time-constant, RC, where R is the equivalent resistance of the transmitter, and C is the capacity of the trays and interconnector cables. The value of R has been made low by using two triodes (pentodes connected as triodes) in parallel, with the load in the cathode circuit. To lower it further would require more tubes and appreciably more power. It is therefore necessary to design the trays and connecting cords so that the maximum C to be driven is never larger than 5,000 micromicrofarads. Capacities from one line to another must be kept to a small fraction of the capacity to ground, in order to avoid cross-talk effects.

The flexible shielded cable which is available for use in making interconnection cables has a capacity of about 30 micromicrofarads per foot. If each cable is three feet long, and 30 such cables are used on a given trunk line, the capacity thus added may be of the order of 3500 mmfd. This leaves no more than 1500 mmfd. capacity for the trays and their short interconnection cables or jumpers. If eight trays are used, a tray and its jumper must have a capacity less than 200 mmfd. Since an eight foot length of shielded cable would have more than this, it is not possible to use this for running digit trunks and program lines the length of the EDVAC. Special coaxial lines would not only be expensive, but would excessively complicate the job of connecting in the sockets which are to occur every two feet.

The tray design which has been adopted is nearly equivalent to a coaxial line with convenient openings every two feet. The shielding is not perfect, but cross-talk is reduced to less than five per cent for even the worst combination of conditions. The maximum cross-talk then amounts to a two-volt pulse, which can have no effect since it is applied to the grids of input tubes biased at -20 volts, with cut-off at -8 volts.

Clearly, there cannot be too many jumpers connected to a particular digit trunk or program line or else the capacity given above would be exceeded. To assist the operator in determining the maximum safe loading the following term is introduced.

<u>One load unit</u> is a capacity of 160 micromicrofarads. The following devices will each be called one load unit:

(1) A program or digit cable. If the cable is only three feet long, it will account for about 90 mmfd. The balance is allowed for the portion of the circuits which will be internal at the particular panel to which the cable is connected.

(2) A tray and its short jumper for connecting to the next tray. The tray accounts for about 120 mmfd. and the balance easily accounts for the jumper.

The standard transmitters used on the regular program and digit outputs (not certain multiplier and divider outputs) are designed to transmit into a line containing not more than 60 load units. Actually program transmitters can transmit into as many as 120 load units with the usual 2:1 safety factor.*

11.2 DELETERS

A deleter is usually used to delete non-significant figures, and is therefore used on the add or subtract output digit terminals. Various types of deleters and the connections made in each are illustrated on drawing PX-4-109. A deleter merely open-circuits the lines corresponding to unwanted digits. Note that when a deleter is used on the output of an accumulator the significant figure switch should be set to the number of figures not deleted. In this case, the subtract pulse will be sent out over the line belonging to the significant figure furthest to the right, next to the deleted digits. Thus, the subtract pulse is not deleted.

11.3 SHIFTERS

A shifter is used to shift the digit lines to either the right or the left, and is placed on the input terminals of an accumulator. Thus, a shifter is generally used to multiply by powers of 10.

*The reason for this is the difference in shape of the CPP as compared to the IOP.

an example of a +2 and a -2 shifter are given on PX-4-104A.

A + shifter. A + shifter multiplies by positive integral powers of ten. In the case of a +2 shifter (PX-4-104A) any pulses arriving over the units channel (terminal 1 of the socket "S") goes to terminal 3 (hundreds) of the plug (P). The plug is inserted in the input digit terminal of the accumulator. Note that terminals 9 and 10 of the socket are not connected and that terminals 1 and 2 of the plug are connected to ground. This grounding prevents the grids of the corresponding input gates from picking up any cross-talk or other noise.

A - shifter. The - shifter multiplies by negative integral powers of ten. In this case, the unused terminals of the socket (see PX-4-104A) are not connected but the unused channels of the plug "P" must be fed with nine pulses in case of a negative number in order to give the proper complement. Thus, if M99430 is multiplied by one tenth the result is M999430. Thus, the PM line (terminal 11 on S) must be connected to terminals 9, 10, and 11, on P in the case of a -2 shifter. An adapter of this type must be used on the input to an accumulator since otherwise the PM transmitter would have to drive three different digit lines instead of just one digit line and three grids of the input gates to the accumulator.

11.4 PULSE AMPLIFIER UNIT

A pulse amplifier unit consists of eleven standard transmitters which interconnect to trunks. Since the buffer unit transmits in only one direction, two units would be needed to completely interconnect two trunks. In counting the load units on a particular digit trunk, for example, the input to the buffer unit counts as only one load unit and

since the buffer unit contains its own transmitters none of the load units of the trunk transmitted into count as being on the first trunk. Thus, these buffer units allow the operator to practically double the number of units which may be connected together via a digit trunk system.

The buffer units are designed to sit on top of a group of program or digit trays. The units contain their own transformers for supplying the heater voltages. The d-c power and the a-c power for the heaters is furnished by sockets located near the floor between accumulators nine and ten and between accumulators fourteen and fifteen.

A block diagram of a buffer unit is given in drawing PX-4-301.

11.5 STATIC OUTPUTS

Each decade and PM unit of every accumulator has a static output socket, accessible from the back. To avoid capacity loads on the counter circuits, a large resistance is placed in series with each static output line. The time constant thus introduced into the static output circuits is large enough so that one addition time must be allowed for the operation of other circuits from these outputs. However, because the system is a static one, there is no cross-talk problem, and unshielded wires can be used for the static cables.

Static cables are used to interconnect units in the following cases:

(1) To connect the multiplier and multiplicand accumulators to the multiplier, see PX-6-301.

(2) To connect certain accumulators and perhaps certain decades of the master programmer to the printer, see PX-12-304.

(3) To connect the PL unit of the numerator and denominator accumulators to the divider, see PL-10-303.

PL-4-111 shows the wiring connections of a static cable.

11.6 SPECIAL DEVICES

11.6.1 Special Program Jumpers

As well as the regular program jumpers described in Section 11.1.2, there are loaded program jumpers and Y program jumpers.

A loaded program jumper is to be used when connecting one program output directly to another program input. The jumper is physically characterized by having an extra long plug at one end which contains the built-in load resistor. Such a jumper must never be used in connection with a program line which enters a tray system which has its own load box.

A Y-program jumper is a jumper with three plugs attached. It is used to connect two nearby program terminals (input or output) to the same program line. It has no built-in resistor so one connection must go to a program tray system which has a load box.

11.6.2 Accumulator Interconnection Cables

There are special interconnection cables and load boxes for use with accumulators which determine whether they act as ten digit accumulators or whether two accumulators act as a twenty digit accumulator. For a description of these cables, see PL-5-301.

11.6.3 Multiplier Interconnection Cables

The multiplier interconnection cables fall into two classifications. First, those that connect the multiplier to its associated

accumulators, and secondly, those that interconnect the three multiplier panels. In the latter classification, damage to circuit elements and short circuits across the power supply may be caused by erroneously plugging a cable into the wrong socket. This possibility is avoided by removing prongs from plugs, and filling corresponding socket holes (where not used) in such patterns that erroneous connections are impossible.

Reference should be made to the following diagrams:

Interconnection of High-Speed Multiplier with Associated Accumulators	PX-6-311
Static Output Cable	PX-4-111
Accumulator Interconnector Cable (Mult.)	PX-5-131

Cross reference should be made to the Operator's Manual, PX-6-304.

11.6.4 Divider Interconnection Cables and Adapters

Since the divider and square rooter serves largely to program its associated accumulators, those interconnections which must be established between the two units mentioned for the purpose of communicating program instructions are made through cables as illustrated on PX-10-307, which drawing makes further reference to special cables and adaptors used.

Cross reference should be made to the Operator's Manual, PX-10-307.

11.6.5 Function Table Adapters

In order to disconnect the 9F gates (B' and L'4) from the synchronizing trunk line carrying the 9P, and to connect these gates to

the line carrying the CPP in the same trunk, an adaptor (PX-4-119) is used. This adaptor is connected where the synchronizing pulse trunk plugs into the back of panel No. 2 of the function table.

11.6.6 Other Adaptors

The remaining adaptors may be classified as; 1) special digit adaptors, 2) digit-program adaptors, and 3) printer adaptors.

The first group consists of adaptors which combine shifting and deleting characteristics and are shown on PX-4-117.

The second group servos to make possible the use of digit trays as program trays. Each adaptor (there are 50) consists of a box with a 12-prong digit plug at one end, connected to a mounted group of 11, two-opening program sockets at the other. These correspond to the 12-prong sockets in the digit trays, and the two-prong plugs on program cables.

The third group consists of two adaptors. Adaptor A (PX-12-114) connects the static output of stage 1' (of the printer interconnection cable to accumulator or master programmer decade counter stages) to the P1 lead in each of two static output cables. Adaptor B is used when no connection is desired to the P1 lead in the static output cables. Adaptor B is also shown on PX-12-114.