



SILICON PROCESSORS USING ORGANICALLY RECONFIGURABLE TECHNIQUES (SPORT)

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14. ABSTRACT The development of reconfigurable photonic circuitry has been pursued using Silicon waveguide networks, PIN diode-actuated photonic crystal switches, and low-voltage, high-frequency EO modulators based on organic materials. Processing advancements in these materials, such as a solution poling method (SPARC) offer new device formats, manufacturable processing, and decreased drive voltages. A proof-of-concept device architecture was fabricated and indicated that SPARC processing may afford deposition, poling and patterning OEOM waveguides in a single step. An all-polymer waveguide phase modulator was fabricated with $V_{\pi} = 1.67$ V using 16 mm electrodes, and was found to be stable over 2,500 mW·hr of 1550 nm irradiation at 25°C in air. Dual-slot hybrid silicon/organic modulators in two architectures, both vertical and horizontal, have been fabricated. The vertical configuration modulator has yielded a $V_{\pi} \cdot L = 0.33$ V·cm. An etch-based process for producing nanoscale slot modulators was developed. A reconfigurable photonic switch network was produced, resulting in a 32 μ m slow light-based photonic crystal switch with a group index of 92, maintaining bandwidth for data rates exceeding 350 Gb/s. Switches were fabricated with PIN diodes for actuation, showing reconfiguration speeds with rise and fall times of 14 ns and 11 ns respectively.					
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SILICON PROCESSES FOR ORGANICALLY RECONFIGURABLE TECHNIQUES

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Subject: Final Performance Report Supplement to Dr. Gernot Pomrenke

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Summary of Program Accomplishments:

During the Silicon Processes for Organically Reconfigurable Techniques (SPORT) program, it was identified that low drive voltage, high speed EO modulators would play the central role in the expansion of computational capability through massively-parallel silicon-based processor nodes. The SPORT program has produced multiple record demonstrations of all-polymer waveguide modulators (APWMs) and hybrid silicon/organic “dual slot” modulators. New modulators, including those that combine the performance of the “dual slot” design with the manufacturability of the APWM process have also been designed. In support of these efforts, new processing techniques have been developed for organic EO materials (OEOMs), and “poling” processes have been developed to achieve 100% “poling efficiency” in waveguide devices. Recently-developed OEOMs have been integrated into all device architectures, and have achieved r_{33} values exceeding 100 pm/V in device. Finally, a high-speed optical switching network has been developed and fabricated, based on PIN diode-actuated photonic crystal switches that feed passive silicon waveguides.

The most commonly cited tradeoff to OEOMs-based devices is the poor reproducibility and sensitive process constraints of the organic materials. Most notably, OEOMs require a step known as “poling” in order to induce EO activity. Understanding the materials, their instabilities, as well as their processing methodologies and poling dynamics have been paramount to the success of the program. In order to navigate many of these pitfalls, an in-Situ Modulated Reflection-mode Ellipsometer (ISME) was constructed to fully parameterize the poling process for thin film slab waveguide/poling capacitor (SWPC) devices. This instrument, and the poling processes gained from it, has been duplicated for the poling of modulator devices. The EO activity is accurately and precisely measured using an Attenuated Total Internal Reflection (ATR) apparatus, also constructed for the SPORT program.

In order to condense and simplify the processing steps required for OEOMs, a new, simultaneous deposition and poling process has been developed in support of the SPORT program. This method, known as the solution phase-assisted reorientation of chromophores (SPARC) process, has been reduced to practice towards producing SWPC devices. ATR measurements on these thin films reveal a 30% increase in the EO activity of the OEOM films after thermal poling and recover about 50% the EO activity of thermally-poled films without poling. A simple proof-of-concept device

architecture was fabricated and indicates the morphological changes induced by SPARC processing may be harnessed to afford a single fabrication step to deposit, pole and pattern OEOM waveguides.

An all-polymer phase modulator has also been fabricated and is being applied to applications in imaging and RF detection/generation. This modulator exhibits a V_π of 1.67 V with 16 mm single drive electrodes, which is nearly 30% lower than the record $V_\pi L$ product for a comparable device in peer-reviewed literature. New organic EO host materials developed at UD for the SPORT program offer increased thermal stability and EO activity, and are predicted to further reproduce this $V_\pi L$. Testing of long-term operational stability has concluded that this V_π does not increase over 2,500 mWhr of 1550nm irradiation at room temperature in air. This modulator is currently being engineered to reduce optical loss, and to increase manufacturability and bandwidth. This design is also being augmented to produce an amplitude modulator and is currently being applied to monolithically integrated nanophotonic devices.

The dual-slot hybrid silicon/organic modulator has also been pursued in two different architectures, each requiring significantly different fabrication approaches. For the original design, the horizontal configuration, a full fabrication process was developed to assemble the layered structure using two bonded substrates. Upon the completion of a mask set used for the multi-layered structure, deposition and pattern processing for the titanium dioxide were developed, allowing the realization of the 3 μm TiO_2 films required in the design. The use of amorphous and poly-crystalline silicon films were explored to use as the high index optical material to for the optical slot while minimizing propagation losses. PECVD depositions have shown ideal refractive indexes with lower optical losses, however, RF sputtered silicon exhibits more mechanical resilience to post-processing. Additionally, preliminary RF slot waveguide samples have been fabricated using the developed processing, while using 450k PMMA as a passive slot material and bonding medium.

The vertical architecture of the dual-slot modulator has been fabricated, poled, and tested. The progress that has led to this point has been iterations of electron beam lithography to define and optimize the silicon-clad (optical) slot, followed by SEM micrographs to diagnose alignment conditions, electrical isolation, polymer backfilling, and RF-slot cladding depositions. The RF slot cladding, TiO_x , is deposited by sputtering and patterned via a liftoff resist patterned by electron beam lithography. The TiO_x is then annealed at the highest possible temperatures to approach the high RF-index rutile phase. Coplanar waveguide electrodes were carefully aligned to the dual slots and fabricated using ultraviolet lithography and electroplating. The OEOM is then deposited via spin processing and poled using techniques optimized by the ISME instrument. This device has currently been fabricated with a 0.9 mm interaction length, shortened in order to reduce e-beam lithography write times until the device can be fabricated and poled in higher yield. These prototype devices have yielded $V_\pi L = 0.65 \text{ Vcm}$ in single drive phase modulation. This design implemented in push-pull amplitude modulation could yield drive voltages below 500mV before optical losses increase to a level which is prohibitive for testing.

As part of the SPORT effort, new fabrication routes for the dual-slot modulator are also being probed. Because the optical loss of our short slot devices is currently around -30dB, which is a typical result for slot waveguides, we are exploring methods to more reliably produce low-loss optical slot waveguides. One method to achieve nanoscale slot waveguides from Silicon with crystallographically smooth sidewalls has been developed as part of this effort. The method relies

on crystal plane-selective etching properties of alkaline etchants and a 45° slot sidewall angle. This technique greatly enhances the manufacturability of silicon slot waveguides as it can generate nanometer scale features defined by micron scale patterning techniques.

A reconfigurable photonic switch network was fabricated, resulting in a 32 μm slow light-based photonic crystal switch with a group index of 92, maintaining bandwidth for data rates exceeding 350 Gb/s. The group index was determined by numerical optimization, which was performed on the slow light photonics crystal directional couplers. Focus was on maximizing the slow light effect with a group index of 92 resulting for short device length of 32 μm , while keeping the group velocity dispersion to less than 150 ps^2/mm for data rates exceeding 350 Gb/s on a 50 GHz ITU grid. Photonic crystal switch elements were fabricated with integrated PIN diodes for free-carrier injection. Switches were fabricated with PIN diodes for actuation, showing reconfiguration speeds with rise and fall times of 14 ns and 11 ns respectively.

Full Report of Accomplishments:

1.1) Organic EO Materials and Processing Strategies

Organic electro-optic materials (OEOMs) are superior materials due to their high electro-optic (EO) activities, fast switching speeds, and linear optical properties[1]. The high EO activity translates directly into reduced power consumption and reduced device lengths[2], favoring OEOMs in applications driven by SWaP. The mechanism of optical nonlinearity in OEOMs is fundamentally different than that of Lithium Niobate and other inorganic materials, and allows ultrafast switching speeds and intrinsic bandwidths that are orders of magnitude higher than any other known EO material[3]. Additionally, the lack of dispersion in dielectric properties of the material between the RF and optical regimes allows excellent phase matching. For these reasons, OEOMs are being explored as the EO material in a variety of devices including modulators[4], ring resonators[5], etc. which have broad application in telecommunications and imaging.

Despite these promising properties, OEOMs have yet to be a large-scale market success because of the lack of reproducibility and complexity associated with their processing. OEOMs are widely known to be susceptible to heat, moisture, and light, and are degraded by common fabrication routes that rely on these parameters (e.g. photolithography). Most notably, many researchers cite the “poling” process to be the biggest bottleneck to integrating OEOMs into devices.

1.2) Materials Processing and Poling: Introduction to Poling

The poling step is required because the EO response arises from asymmetry at the molecular level. If the hyperpolarizable molecules that comprise the film are not arranged, or ordered, the molecular asymmetry is broken at the bulk level and the EO activity vanishes. Because Lithium Niobate is a noncentrosymmetric crystalline material, it does not need to be “poled.” Polymeric and organic materials are inherently amorphous, and a process to align the molecules is needed to create a noncentrosymmetric material. The state-of-the-art OEOMs rely on the chemical synthesis of an EO molecule, or chromophore, which is commonly doped into an inert polymer host. This amorphous and conformal film is typically deposited by spin deposition. This film is then poled, which induces EO activity in the material, which is typically quantified by the magnitude of the dominant element in the r tensor, r_{33} . This tensor element is related to the noncentrosymmetric order parameter $\langle \cos^3\theta \rangle$ by:

$$r_{33}(\omega) = N\beta_{zzz}(-\omega; 0, \omega) \langle \cos^3 \theta \rangle \frac{-2g(\omega)}{n(\omega)^4}$$

In this relationship the N is the number density of chromophores in the film (molecules per cubic centimeter), $\beta_{zzz}(-\omega; 0, \omega)$ is the frequency, ω , dependent first molecular hyperpolarizability (electrostatic units), $g(\omega)$ is the Lorentz-Lorentz-Onsager local field factor, and $n(\omega)$ is the linear refractive index.

Thermally-enabled electric field poling (TEEFP) is accomplished by heating the material to allow rotation of the chromophores. This rotation is then preferenced through the application of a DC electric field on the order of MV/cm. The chromophores inherently exhibit an internal electric field, which can align them to oppose the applied “poling” field. When the material is cooled down the rotational freedom of the chromophores decreases to prohibit relaxation back to a disordered state. The TEEFP process requires careful attention to a number of experimental variables. The temperature and poling voltage must be precisely controlled because the thermal energy required to align the chromophores is extremely close to the conditions for dielectric breakdown of the material. The magnitude of the poling field is proportional to the EO activity observed, thus the challenge of OEOMs is to approach, but not exceed, breakdown conditions.

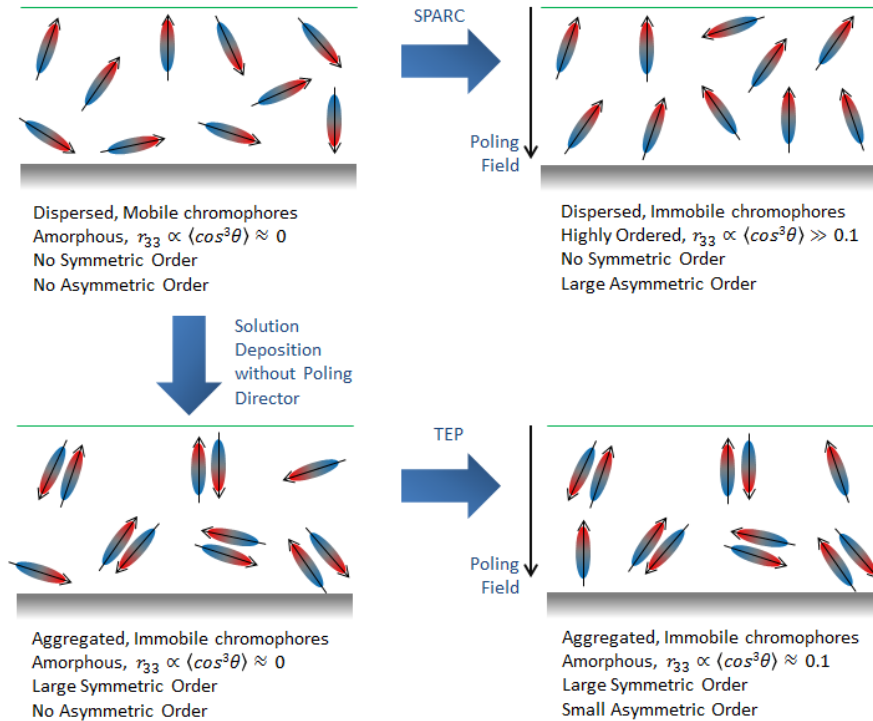


Figure 1. Cartoon illustrating the process of SPARC (top left to top right) and TEEFP (top left, bottom left to bottom right). The chromophores in the film are depicted as elliptical in shape and the arrow designates their internal electric dipole moment. In this figure the ensemble average $\langle \cos^3 \theta \rangle$ is related to the angle θ between the modulation (or poling) electrodes and the molecular axis of the chromophore. These estimations of $\langle \cos^3 \theta \rangle$ for TEEFP are reported in the literature[6] where $0 < \langle \cos^3 \theta \rangle < 1$, essentially attenuating the ideal r_{33} by a factor of 10. Contrary to popular belief, spin-processing does not natively introduce in-plane order to OEOMs. This has been shown in recent literature[6].

Intuitive guidance over the dynamics of poling can be expressed as the competition between an approximate Langevin (Brownian) interaction between the poling field vector and the dipole moment of the chromophore, and the same Langevin interaction between neighbor dipole moments. This competition is commonly written:

$$\langle \cos^3 \theta \rangle = \frac{\mu_0 f E_p}{5kT_p} \left[1 - L^2 \left(\frac{W}{kT_p} \right) \right]$$

In this relationship μ_0 is the static, ground state dipole moment of the chromophore, f reports the local field factors which attenuate interaction with the poling field E_p . Here k corresponds to the Boltzmann constant and T_p the temperature at which these interactions occur, L is the Langevin function and W is the dipolar correlation function describing chromophore interactions. For some recent applications it might be important to note that this relationship assumes a monolithic OEOM and also that for TEEFP, that T_p is the (elevated) poling temperature which is influenced by the glass transition temperature of the polymer-chromophore composite.

1.3) Materials Processing and Poling: Motivations for SPARC Processing

Over the past decade and longer, EO activities have advanced through chemical modifications of OEOMs. These modifications produce larger molecular nonlinearities, but also increase the internal electric field of the chromophore, μ . This aids the poling of the chromophores by linearly enhancing the interaction with the poling field (μE), but that requires that the chromophores were not already aggregated, as depicted in the bottom-right of Figure 1. The fundamental nature of the field internal to the chromophores in solution phase is that the deleterious effect of aggregation (μ^2) outweighs the benefit to poling (μE). Furthermore, it must be noted that molecular mobility in solution far outweighs the mobility of a glass-rubber transition in polymeric hosts. As such, the SPARC process is designed to achieve the full potential of the incredible efforts levied by synthetic chemistry groups over the last several decades[7]. Because modern OEOMs exhibit asymmetric order that corresponds to approximately 10% of the achievable r_{33} [6], it is anticipated that SPARC could afford EO activities many-fold the reported values. If the method does not induce higher asymmetry in the film, it could also allow a larger concentration of chromophores to be doped into the film while lowering the threshold for mass symmetric aggregation. The EO activity is linearly related to the concentration of chromophores, which means that SPARC could enhance the EO activity of the OEOM by allowing higher doping levels of ordered chromophore.

SPARC should also enhance EO coefficients by acting as a pretreatment of films, which may undergo successive TEEFP. Symmetric aggregation may be reduced due to SPARC processing, but may also require TEEFP to break the symmetry of the molecules in the film. SPARC processing has also been pursued as a singular method to induce EO response in OEOM films. Either of these approaches may realize the theorized enhancement of molecular order and the corresponding increase in the EO coefficient of the films. Because all of these effects are based on processing, this enhancement should translate to any OEOM and most device architectures. As such, SPARC could become the new paradigm for processing OEOMs and will grow alongside the development of new chromophores and EO materials.

Many other performance metrics of OEOM devices will benefit from the SPARC method. Some of these benefits are related to the lack of high-temperature processing required for traditional thermal poling. TEEFP would be prohibitive for devices that incorporate temperature-sensitive components[8]. Delamination and internal strain caused by thermal expansion is also avoided.

A historically-accepted tradeoff of OEOMs is that the poling temperature and thermal stability of the material are coupled. With the understanding that the poling temperature sets an upper limit on the thermal stability of the OEOM, and using the above equations, the qualitative relationship $\text{thermal stability} < T_p \propto \frac{1}{r_{33}}$. This tradeoff can be broken by using the mobility of the solution phase to enable poling of OEOMs, such as by the methods presented here. In doing so, we also enable materials and devices which are not compatible with the high electric field strengths and temperatures normally required for TEEFP.

1.4) Materials Processing and Poling: Slab-capacitor Devices for Thin Film Measurement

In order to apply a non-contact poling director while the solution of OEOMs is being deposited, a corona discharge method is being explored. Corona discharge has largely been abandoned as a means to pole OEOMs but historically has been used in combination with thermal poling to induce order. Corona discharge requires that a very strong potential, about 10,000 VDC, is applied to a sharp needle above a ground plane. The ground plane is completely insulated by the OEOM such that the gaseous atoms charged at the corona needle are attracted to the ground plane and collect at the surface of the insulating layer. This generates a strong electric field across the small insulator thickness, resulting in the MV/cm field strengths required for poling. As the spin solvent evaporates the charges will collect on the top of the forming-film, and the material will pole without the deleterious aggregation introduced in traditional poling.

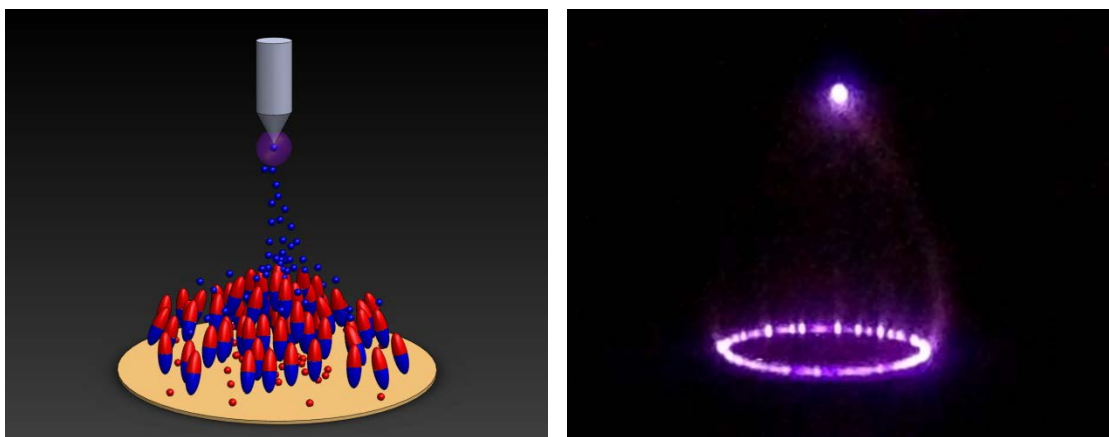


Figure 2. A cartoon (left) to reflect some of the interactions in the SPARC concept: In the cartoon the blue spheres represent electrons carried by gaseous species, and the red spheres are holes in the gold-colored ground plane. The elliptical species represent chromophores which have an inherent internal field. The needle sits above the plane and stimulates the corona discharge (purple glow). An image of the violet fluorescence observed from a corona discharge generated by the SPARC apparatus is shown on the right.

1.5) Materials Processing and Poling: Experimental Apparatus

Proper equipment for SPARC processing requires the nearly self-exclusive combination of fast, balanced mechanical rotation and chemical resistance for spin processing combined with careful atmospheric control and kilovolt-scale high voltage conduction/isolation/insulation required for corona discharge. Generating a stable corona discharge alone is not a trivial task. Point-to-plane models for this apparatus are not readily available in the literature and the data published is typically decades old and entirely phenomenological. Additionally, triggering a visible corona discharge is often attributed to unreliable environmental fluctuations, such as ambient UV light or radiation, rather than carefully controlled conditions. A stable corona discharge was generated, which glows on the order of hours, under potentials far higher than point-to-point models predict, presumably due to the lack of localization of an electric field about a conductive plane. This discharge is shown in Figure 2. It is useful to note that careful attention to the gaseous environment of the corona discharge also produces an environment for processing that rivals the atmospheric control of a cleanroom. The first devices utilizing SPARC were simple slab devices. This device architecture offers the highest throughput as well as the most straightforward measurement of OEOM properties. The deposited films are also shown in Figure 3.



Figure 3. An image of the experimental apparatus constructed to produce OEOM films subjected to SPARC processing and a series of films the resulted from initial trials: (left), under standard SPARC conditions (middle) and under longer exposure to the corona discharge with a patterned ground electrode (right).

1.6) Materials Processing and Poling: Results and Characterization of Film Morphologies

The morphology of the thin films indicates that the corona discharge has a profound impact on the OEOM solution and, more importantly, the film that results from the deposition. The region directly under the needle is visibly darkened, which corresponds to a large increase in thickness. This conclusion was confirmed by white light interferometry, which measured a thickness of 8-10 microns on the darkest region and 700-800 nm for the lighter periphery of the film. Identical processing was carried out on polymer films that contained no chromophore, and the film morphology was not altered by SPARC processing. This undoped polymer film was flat, and this result was also confirmed by white light interferometry. Because the film is transparent, an image is not included in this report. Based on these results, it could be concluded that the film morphology resulting from SPARC is due to the coulombic interaction between the dipolar chromophores and the strong field stimulated by charge carriers collected on the forming-film. The change in

morphology in the film when chromophores are present is indicative of a change to the underlying molecular distribution of the chromophores doped in the film. In order to determine whether this perturbed underlying molecular distribution corresponds to a change in the molecular orientational distribution, these films were subjected to measurement of EO activity by Attenuated Total Internal Reflection (ATR).

1.7) Materials Processing and Poling: Attenuated Total Internal Reflection

The best-known method for accurately determining the EO coefficient of an OEOM film is known as attenuated total internal reflection, or ATR[9], [10]. ATR is a prism coupling technique that measures EO activity as a shift in the angle of total internal reflection induced by an applied modulation field. Shown in Figure 4, ATR offers precise measurement of the EO activity (all non-vanishing elements of the $\mathbf{r}$ tensor for OEOMs) for slab waveguide formats. An additional advantage of the ATR apparatus is that it can very precisely measure the refractive index of the OEOM, which provides very specific feedback when simulating device designs that integrate a specific material. For this study the ATR was sourced by a diode laser centered at 1310 nm.

For this study, ATR was used to characterize the EO activity of IKD-1-50, a material developed by Larry Dalton at the University of Washington, Seattle. This chromophore was doped at 25% into poly(methyl methacrylate) and co-dissolved into 1,1,2-trichloroethane. All materials were purified using multiple procedures to reduce the conductivity of the solutions.

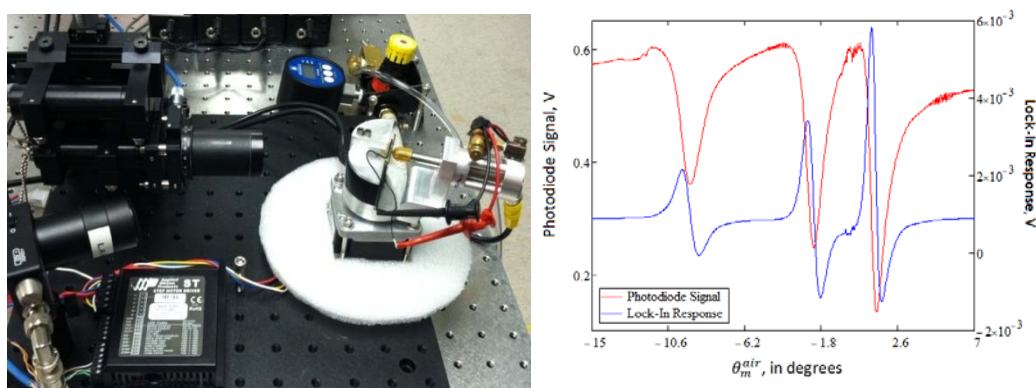


Figure 4. An ATR apparatus is shown. The graph displays the raw data from the measurement of a material (IDK-1-50 provided by Larry Dalton at UW) that reproducibly displays an EO activity of $r_{33}=170 \pm 10$ pm/V.

1.8) Materials Processing and Poling: EO Activity Results

One of the most promising aspects of the SPARC process is that it is compatible with nearly any material that can be poled under TEEFP conditions. As such, the EO activity will be expressed relative to TEEFP samples characterized using identical conditions. For the materials studied here, the SPARC process was able to generate roughly 40-50% the r_{33} values of films poled using TEEFP. These results exemplify the potential of SPARC processing to offer the first demonstration of simultaneous deposition and poling of organic EO material solutions. It is anticipated that this result will approach >100% of the EO activity of the control group as the SPARC method and apparatus is refined.

Films processed using SPARC poling resulted in a 30% enhancement in EO activity when compared to the control group. The control group was processed and deposited in an identical fashion but with

0 VDC potential between the corona needle and ground plane. Both groups involve TEEFP, making SPARC a pretreatment of films used to discourage symmetric pairing during solution deposition.

A control group of samples deposited at 0 VDC and without TEEFP reproducibly showed values of $r_{33} < 3$ pm/V. These results are preliminary because of the large change in film thickness induced during SPARC deposition. ATR requires flat films to accurately measure angles of total internal reflection. Because of this increased error associated with ATR measurement on non-planar films, a device demonstration that utilizes SPARC poling was also pursued to quantify the enhancement in EO activity afforded by SPARC as well as to qualify the utility of SPARC as a method to produce poled OEOM films.

1.9) Materials Processing and Poling: Proof-of-Concept Device Architecture for SPARC Processing

In order to provide a preliminary test of the SPARC concept in a waveguide device, travelling wave, coplanar gold electrodes were deposited and patterned on a UV15 coated silicon substrate. UV15, the most ubiquitous cladding material used in OEOM devices, was deposited using spin deposition followed by UV flood and overnight annealing at 100°C. The electrodes were evaporated and patterned using NR2 photoresist and a wet etchant. The electrodes were 100 nm thick, 10 micrometers apart, and also connected to larger pads which were used for electrical contact. A coarse schematic of the device is shown in Figure 5. OEOM solutions were dripped down the electrodes and, once entirely coated, a DC bias was placed between the electrodes. The leakthrough current was measured to evaluate the resistivity of the OEOM solution as a function of the time after deposition. The resistivity varies over 4-5 orders of magnitude, settling to the lower value over a period of 3-4 minutes.

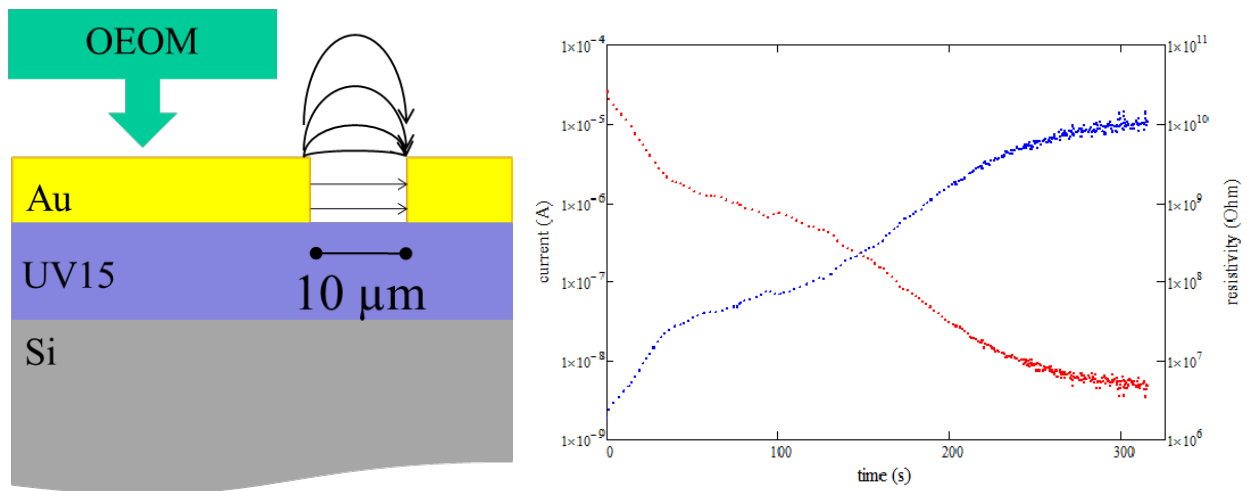


Figure 5. Schematic of the isolated coplanar electrodes used to demonstrate SPARC processing (left) and a measurement of current at 50 VDC as a function of time (right).

These devices were examined using optical microscopy which revealed a drastic degree of damage to the OEOM as the current flowing between the electrodes increased. This damage is thought to be boiling and decomposition as a result of joule heating the OEOM solution. Figure 6 shows several

optical microscope images for samples deposited under 0 to 500 VDC. To limit the extent of joule heating, another sample was deposited with a power supply set to operate as a current source limited to 1100 VDC. The damage induced in this sample is comparable to the damage visible in the sample deposited at 0 VDC. During the final phases of solidification, the OEOM in this device experienced fields greater than 100 V/micrometer.

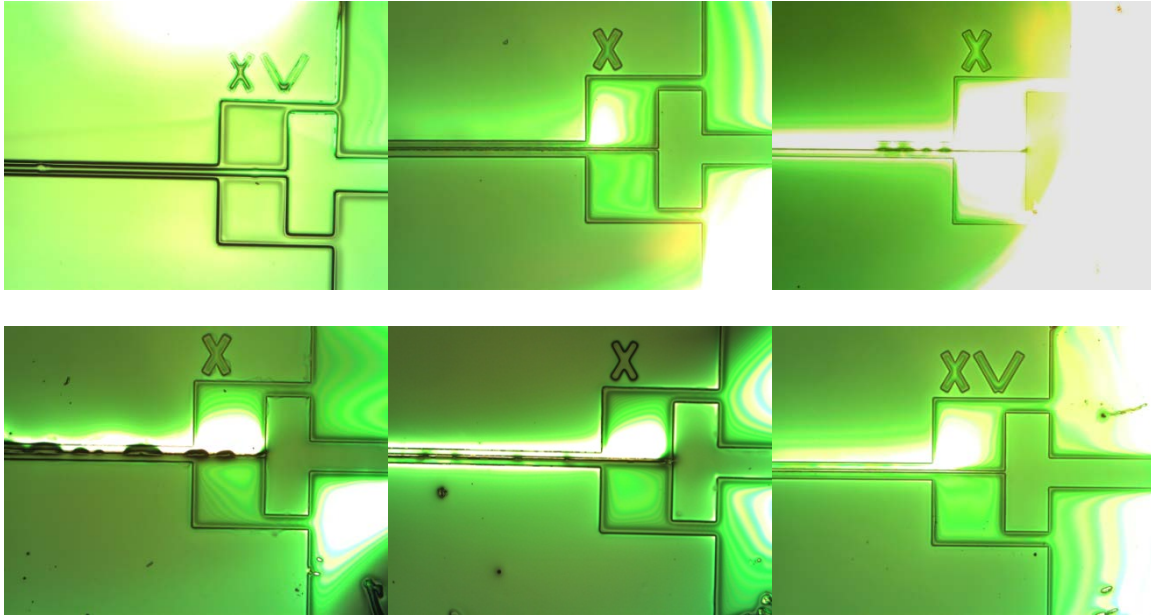


Figure 6. Optical microscope images of the device shown in Figure 5 on which OEOM was deposited using the method described above. Various voltages were applied between the coplanar electrodes: 0 V (top left), 25 V (top middle), 50 V (top right), 100 V (bottom left), and 500 V (bottom middle) all limited to <1A of current. Another device was limited to 1100 V while the power supply was limited to 20 microamperes (bottom right).

However, in each case when a voltage was supplied between the electrodes during deposition of the OEOM solution, the electrode charged with positive carriers is coated with a thinner OEOM film after solidification. This observation arises from the increased brightness of the top positive electrodes in the dark field microscope images in Figure 6. This result suggests that the SPARC technique may afford the capacity to not only deposit and pole the OEOM, but also to pattern the material in a single processing step. Various electrode architectures, materials and deposition methods are currently being explored in order to determine the feasibility of this concept. An example from one of these approaches is shown in Figure 7.

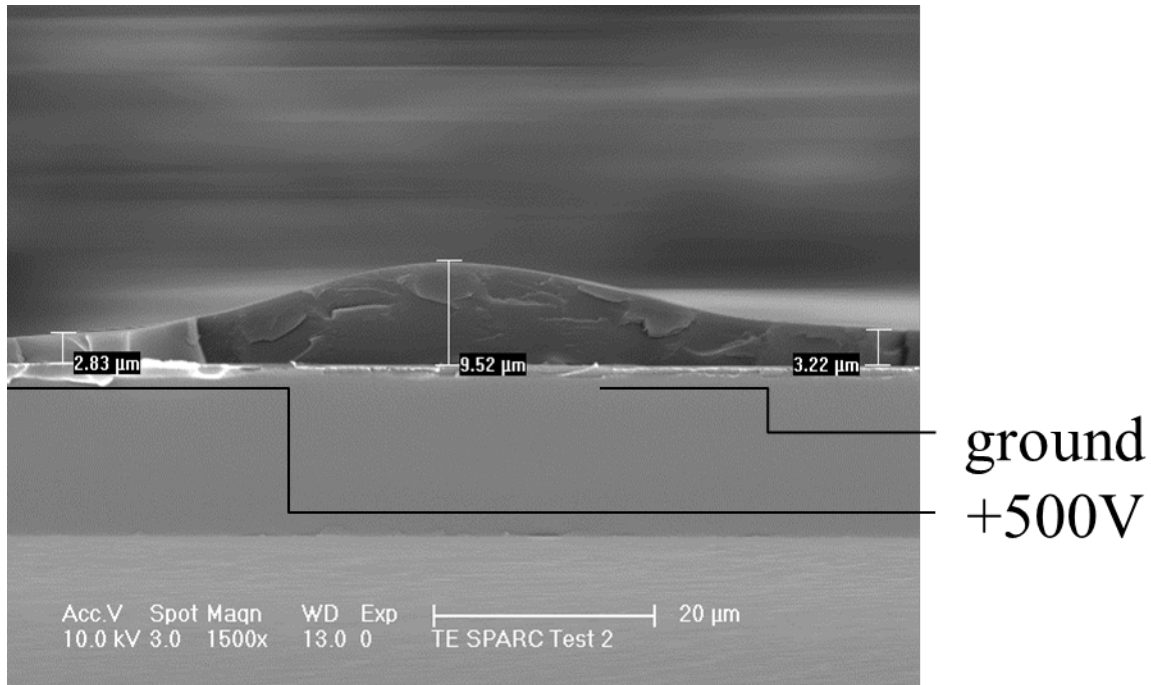


Figure 7. Micrograph of a cross-section of the SPARC sample taken using scanning electron microscopy. The electrodes are not clearly visible at a magnification which allows visualization of the OEOM film. As such, the electrodes are labeled and were biased according to the labels on the right of the image.

A number of interesting observations can be taken from the cross-sectional view of one of the electrode patterns explored as a preliminary attempt to pattern OEOM solutions using SPARC processing. First is the confirmation that the thickness of the OEOM varies on top of the positively and negatively charged electrodes. It is also interesting that the region in between the electrodes is the thickest, corresponding to a minimum in the μE interaction potential. It can be predicted that this minima occurs only in instances of bulk noncentrosymmetric order. This raised region is roughly the dimension of the typical mode size of a single-mode optical fiber, but lacks the defined shape to guide a single mode which is needed for modulation. Various experimental techniques are being explored to refine the shape that results from SPARC processing, in tandem with carefully chosen cladding and blocking layers, in order to exploit the morphology induced by SPARC processing to result in single-step deposition, poling and patterning of OEOM waveguides. Such a demonstration will be the first of its kind.

2.1) Development of an All-Polymer Waveguide Modulator

Leveraging efforts in collaboration with Air Force Research Laboratory, a portion of the SPORT effort has been associated with the development of an all-polymer waveguide modulator (APWM). This modulator is designed for the generation and detection of RF energy, and thus requires an antenna structure to feed the electrodes which traverse the modulation region of this device, which can be coupled to various optical components to detect a phase shift resulting from the EO effect. Because of the nature of coupling free space radiation, the waveguide stack must be composed of materials which exhibit low refractive indices in the RF domain. For this application slot-like modulators, or those which contain silicon, cannot be used, and an all-polymer waveguide stack was pursued. This design also carries the benefit of being simple to fabricate and offers great potential towards monolithic integration with Silicon components. As such, this device has been explored for applications related to the SPORT effort.

The foremost challenge with designing an OEOM waveguide is developing a fabrication process that will not damage the material either by high temperatures, exposure to UV light, or contact with an incompatible solvent. In particular, patterning the OEOM to provide lateral confinement for a waveguide mode proves difficult as many standard patterning techniques involve steps that could cause the EO chromophores to undergo photochemical decomposition. The most common technique [11] [12] [13] to circumvent this issue is to pattern the bottom cladding layer and then spin deposit the OEOM core and subsequent cladding layer, which results in an inverted ridge waveguide structure as shown in Figure 8.

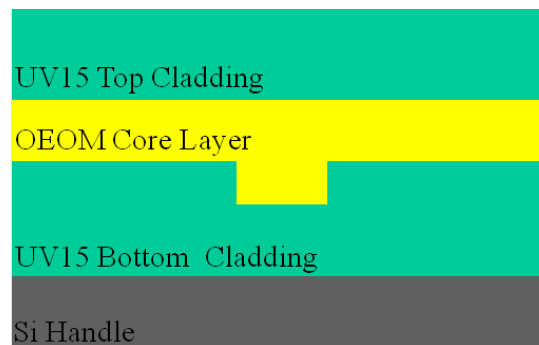


Figure 8. Inverted ridge waveguide structure

The sequence of processing steps used to fabricate an inverted ridge waveguide offers the freedom to develop a patterning step without considering the stability of the OEOM. Only the temperature during curing steps and the possibility of incompatible solvent contact need be considered in subsequent processing steps. Because of these advantages, the modulator presented in this work utilizes an inverted ridge waveguide, the fabrication of which is detailed in the following section.

2.2) All-Polymer Waveguide Modulator: Fabrication and Processing

The choice of material for vertical waveguide cladding layers has important implications in both operation and fabrication. Primary amongst operational concerns is poling efficiency. Experimental results have indicated that EO activity increases linearly with poling field strength. Therefore conductive cladding layers that would focus the field directly across the OEOM core would provide

the greatest poling efficiency; however, this is offset by the additional conduction loss that would be introduced by the close proximity of the optical mode to a conductive material. This tradeoff is broken by using an electrically insulating cladding material that has a higher dielectric strength than the OEOM under poling conditions.

Significant work has been accomplished towards developing cladding materials that find a balance between conductivity for poling efficiency and low loss optical propagation [14] [15] [16] [17]. However, the performance enhancement gained by some of these exotic cladding materials comes at the expense of fabrication complexity, including material synthesis processes that can impede manufacturability. A primary goal of this research is to develop a modulator that is based on a simple scalable fabrication process without large sacrifices to performance parameters.

2.3) All-Polymer Waveguide Modulator: Fabrication and Processing Methodology

The fabrication process for this modulator was designed with special attention given to yield, time, and cost. The modulator core is comprised of IKD-1-50, an EO chromophore which is doped into a polymer host and cladding layers are made of a commercially available polymer material. All patterning is done using standard 365 nm UV lithography and transferred via an O₂ plasma RIE etch.

Both the top and bottom cladding layers of this device are spin-deposited layers of UV15 (Masterbond, NJ, USA); a low index, UV curable resin. This material is commercially available on the liter scale and affords optical quality coatings without further treatment. Device substrates of UV15 are made on 4" wafers of Si with a uniform coating of 10 nm of Ti and 100 nm of Au to serve as the ground plane electrode for poling and modulating. The bottom UV15 film is cured in a two-step process: first a UV flood exposure of 10 J/cm² sets the surface quality afforded by spin deposition, and then an overnight thermal curing at 110°C *in vacuo* fully anneals the film to ensure it is sufficiently robust for subsequent processing steps. Individual samples are cleaved from these substrate wafers to ensure uniform thickness and eliminate the possibility of edge effects that could adversely affect the waveguide patterning.

Patterning is done using a negative resist soft mask and plasma etch pattern transfer. The process is simplified by leveraging the similar etching rates of UV15 and SU-8 in an O₂ plasma to combine the pattern transfer and mask removal steps into one. A 0.5 µm thick layer of SU-8 2000.5 is deposited and patterned using standard contact lithography at 365 nm. The device is then etched in an O₂ ICP RIE plasma where the UV15 and SU-8 are concurrently etched, resulting in a trench comparable in depth to the original SU-8 thickness, and full removal of the soft mask.

Solutions of OEOM are prepared with 25% IKD-1-50 in poly(methyl methacrylate), dissolved in 1,1,2-trichloroethane. The percent of solids by weight is controlled to yield layers with thickness of 1-1.5 µm. Spin deposition over the relatively shallow trench depth of < 1 µm in UV15 results in a largely uniform layer with only a small indentation over the etched trench that does not significantly inhibit mode guiding. The deposited OEOM film is thermally cured under vacuum at 85°C overnight.

A dilution-filter-reconstitution step for the top cladding layer was developed to ensure a pristine thin film is deposited without exposing the OEOM core layer to the solvent necessary for filtering the viscous UV15. The UV15 is diluted to 70% by weight in acetone, filtered through a 0.2 µm filter into a clean vial, and then transferred to a vacuum chamber for ~20 hours to draw off the solvent.

The result is a solution that is >90% UV15 and free of any particulates that can be safely spin deposited onto an OEOM layer without degrading the film.

The reconstituted UV15 is spun for 5-10 minutes at 6000 rpm to obtain films from 2 μm - 5 μm thick. This spin process leverages the fact that UV15 will not solidify until it is exposed to UV light or baked at temperatures > 100°C. This means that the layer will continually thin during a long spin deposition at room temperature. Using elongated spin times rather than solvent dilution yields thin films without damaging the OEOM.

The top cladding layer curing process is modified so as to not damage the OEOM layer. The flood UV curing dose is reduced to 5 J/cm², at which no decomposition to the OEOM has been observed. Once the OEOM is deposited, subsequent process temperatures need to be kept below the poling temperature (T_p) when not in the presence of a poling field as this will result in molecular mobility which will allow centrosymmetric dipole-dipole pairing that will reduce the efficacy of a successive poling step. A thermal cure at 100°C for ~20 hours sufficiently cures the top cladding layer without exposing the OEOM to temperatures above the T_p of 110°C.

Top electrodes are 200 nm thick layers of Au deposited in an electron beam evaporator. The electrode structure includes a 4 mm long by 3.5 mm wide contact pad feeding into four fingers, each 50 μm wide and 1.2 cm long as shown in Figure 9. The four guides are poled simultaneously, allowing for multiple modulation measurements per poling process and providing redundancy against guide obstructing defects.

The electrode structure is aligned with the waveguides by alignment marks that are patterned during the waveguide lithography step. The patterning is done in a positive photoresist AZ-5214 with a process involving bake steps of 90°C, well below the T_p of the OEOM, and then transferred using a commercial Au wet etch.



Figure 9. Top electrode configuration over optical waveguides

The final step is end facet preparation. Conventional cleave and polish techniques used for preparing optically smooth waveguide end facets are expensive both in time, yield, and infrastructure. Additionally, polishing polymer stack waveguides was observed to tear and delaminate the polymer stack, rather than smooth it. A method of cryo-cleaving was developed to achieve highly smooth polymer waveguide end facets while also greatly simplifying the end facet preparation process. The device is scribed and then immersed in liquid nitrogen where it remains submerged until the boiling subsides, indicating that it is uniformly frozen. The device is then removed from the liquid nitrogen and immediately cleaved over a sharp edge such as a razor blade before it begins to thaw. The Si cleaves along its crystal planes and the polymer layers crack cleanly with it. A finished device end facet is shown in Figure 10.

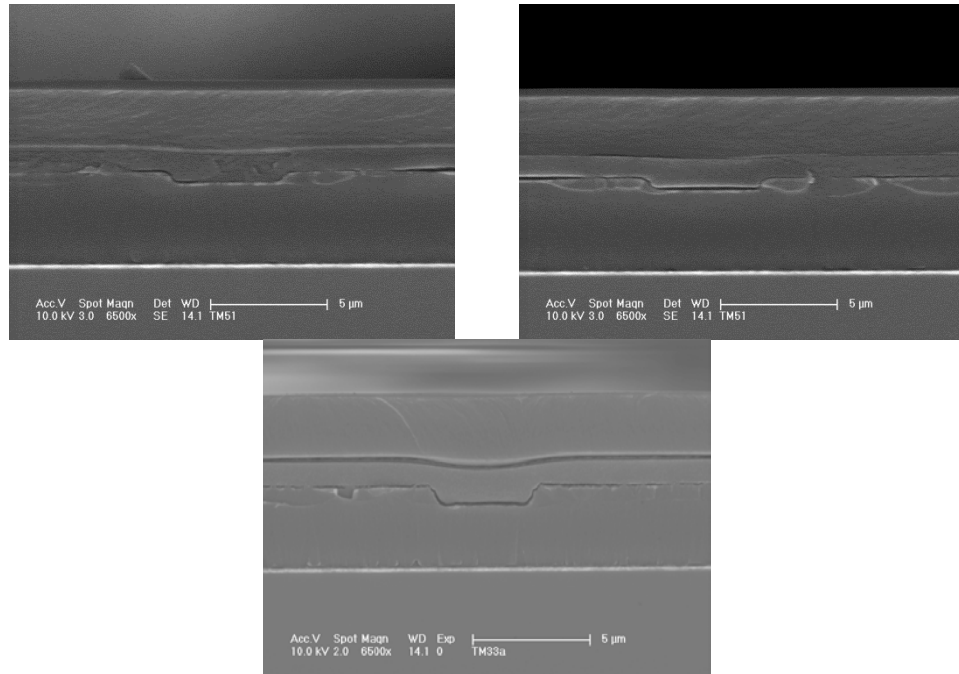


Figure 10. Cryo-cleave prepared end facets

2.4) All-Polymer Waveguide Modulator: FDFD Modeling

Optimal waveguide dimensions were determined for both operational efficiency and fabrication ease. The finite difference frequency domain (FDFD) mode solver method [18] was implemented to determine the number of modes supported for a given set of dimensions, and to calculate the mode confinement. Trench depths were determined to be 0.5-1 μm for optimal OEOM core deposition and etch process capabilities. The index of UV15 has been reported [12] as 1.504 at 1550 nm and the index of the IKD-1-50 solutions used in this device have been measured to be 1.65 at 1550 nm by the attenuated total internal reflection technique [19]. Simulated cross-sections of devices with varied guide dimensions indicated that a single mode would be supported for guide widths up to 4 μm across.

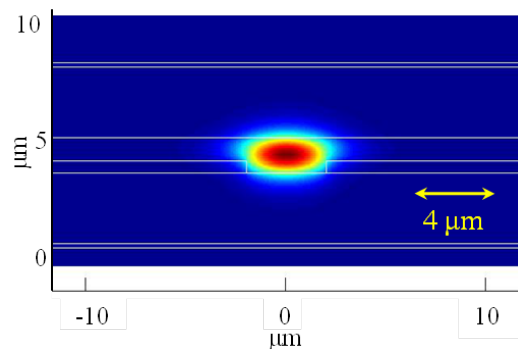


Figure 11. Single TM mode at 1550 nm

The waveguide discussed in this research is 4 μm across, with a trench depth of 0.5 μm , and a 1 μm thick OEOM layer. These dimensions support a single TM mode, are within fabrication tolerances, and calculations show 72% of the mode is confined in the OEOM.

2.5) All-Polymer Waveguide Modulator: Device Poling

To break the inherent centrosymmetry of the amorphous OEOM films, the devices are thermally poled to allow for 2nd order nonlinear characteristics, *i.e.* Pockel's effect, to be observed and utilized. The devices are heated to an optimal poling temperature, T_p , just below the glass transition temperature of the polymer host, while in the presence of a strong electric field. Once T_p is reached, the electrostatic forces between the now-mobile polar molecules in the film and the applied poling field orient the chromophores with the field in an asymmetric arrangement. The poling field is maintained across the device until the temperature is lowered back down to room temperature, at which temperature there is insufficient molecular mobility for the chromophores to return to a centrosymmetric arrangement.

Significant research has been performed in pursuing efficient poling process for OEOMs [20] [21] [22] and modulator poling routines in this study are based on much of that work. Devices are poled on a thermally-enabled poling apparatus with a heating stage, nanoampere resolution current measurement, and in an enclosed, N_2 -filled chamber. All of the equipment to control or monitor poling is interfaced to a PC and the poling process is automated in the LabVIEW environment. This apparatus is shown in Figure 12. The automation routines greatly aid the reproducibility in EO activity afforded by the poling process. The patterned modulation electrodes and Ti-Au ground plane electrode are used to apply the poling field, as they are well aligned with the OEOM in the core of the waveguide.

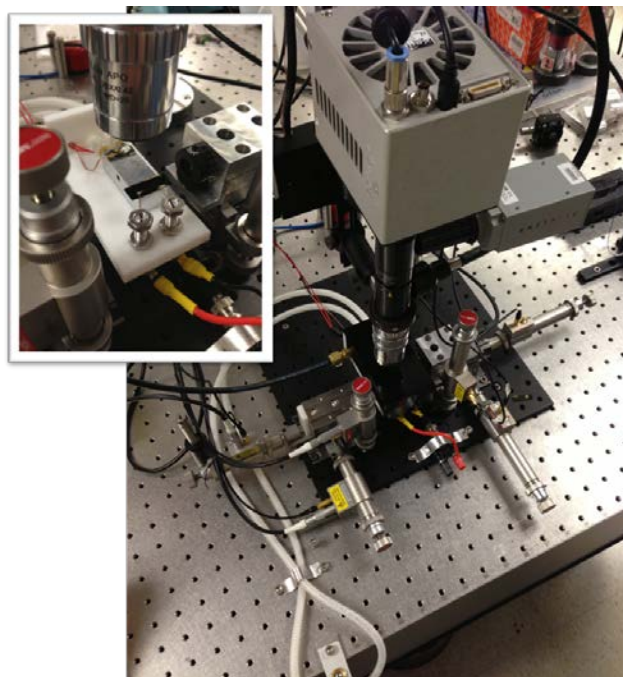


Figure 12. Apparatus used for poling OEOM Waveguides and characterizing EO Modulators, with inset of a sample mounted to a heating stage.

The structure of the modulators prevent the use of the *in-situ* simple reflection technique [23] for monitoring EO activity while poling. Instead, current feedback is used to monitor the mobility of charge carriers in the film as it is heated to T_p . As the voltage is ramped up and the temperature is gradually increased, the current measured across the device slowly rises. Once the temperature reaches T_p , the charge carriers generated across the film are mobilized and swept towards the position of lowest energy, resulting in an increase in measured current. This current peak suggests that there is sufficient molecular mobility in the film to afford chromophore rotation influenced by the DC poling bias. Current peaks were found to be on the order of 5-20 μA . A sample poling trace is shown in Figure 13.

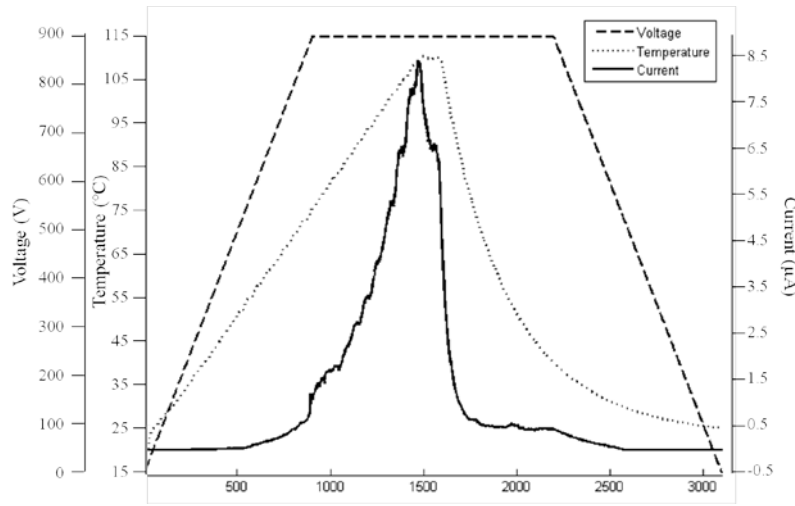


Figure 13. Poling trace of current (solid), temperature (dotted), and applied voltage (dashed) as a function of time in seconds on the x-axis.

Poling tests determined that the devices could withstand poling fields of up to 120 V/ μm without dielectric breakdown in the OEOM or UV15 layers. However samples poled at these higher fields did not provide proportionally lower drive voltages as a result of increased EO activity, and in many cases these samples had greatly reduced EO activity. To avoid shorting and electrode ablation caused by applying high voltages to the 200 nm thick top electrodes of these test devices, a conductive paste is applied to provide a robust contact point. In future device iterations thicker top electrode layers will be electroplated and electrical contact will be made via wire bonding.

2.6) All-Polymer Waveguide Modulator: Polarization Rotation Measurement

Values of V_π are measured using a polarization rotation technique. 1550 nm 45° polarized light is launched into the waveguide via end fire coupling with a lensed fiber. The output is focused by a lens through a 45° polarizer onto a photodiode. As the light traverses the guide, the vertical modulation field induces an unequal phase shift in the vertical and horizontal components of the field, resulting in a polarization rotation. As the polarization is rotated into and out of the plane of the polarizer, the intensity of light reaching the photodetector is modulated in amplitude. This intensity is easily calculated using Jones matrices to be

$$I_{out} = \frac{1}{2} [1 + \cos(\Delta\phi_v - \Delta\phi_h)] \quad (1)$$

assuming an input field of unity amplitude. $\Delta\phi_v$ and $\Delta\phi_h$ are the vertical and horizontal phase shifts that result from Pockels effect and are given by

$$\Delta\phi_v = \frac{\pi}{\lambda} n^3 r_{33} \Gamma \frac{V}{d} L \quad (2)$$

and

$$\Delta\phi_h = \frac{\pi}{\lambda} n^3 r_{13} \Gamma \frac{V}{d} L. \quad (3)$$

Note that the horizontal component phase shift is a factor only because of the 45° polarized input light. In a purely TM phase modulator, only vertical light will be launched and there will be no counteracting horizontal phase shift resulting from r_{13} modulation. To account for this, the experimentally verified approximation that $r_{13} \approx \frac{1}{3} r_{33}$ is used to back out a pure TM modulator V_π . The total phase shift $\Delta\phi = \Delta\phi_v - \Delta\phi_h$ is

$$\Delta\phi = \frac{\pi}{\lambda} n^3 (r_{33} - r_{13}) \Gamma \frac{V}{d} L. \quad (4)$$

Substituting the approximation for r_{13} and solving for the voltage V that results in a π phase shift yields

$$V_{\pi, 45^\circ} = \frac{3}{2} \frac{d}{L} \frac{\lambda}{n^3 r_{33} \Gamma}. \quad (5)$$

The equation for V_π in a pure TM phase modulator is solved for in a similar manner:

$$V_{\pi, TM} = \frac{d}{L} \frac{\lambda}{n^3 r_{33} \Gamma}. \quad (6)$$

Comparing (5) and (6) shows that

$$V_{\pi, 45^\circ} = \frac{3}{2} V_{\pi, TM}. \quad (7)$$

Therefore when reporting V_π values acquired from the polarization rotation technique, the measured values are multiplied by a factor of 2/3.

2.7) All-Polymer Waveguide Modulator: Modulation Results and r_{33} Estimation

Modulators were characterized using a symmetric triangle wave modulation voltage. Successive device iterations were fabricated to lower V_π predominantly through thinning of top and bottom cladding layers to lower the electrode gap d while maintaining the electrode length at $L=1.5$ cm. The minimum V_π was measured as 3.3 V via the polarization rotation measurement, indicating a pure TM V_π of 2.2 V, measured on a device with a 7.5 μm electrode gap as shown in Figure 14. The voltage length product of this modulator could approach 2 Vcm in dual (push-pull) drive, which is comparable to the record demonstration to date for a TM-mode or inverted ridge waveguide based modulator structure [24].

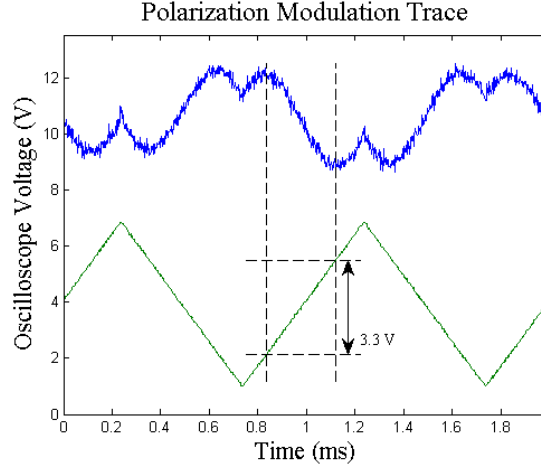


Figure 14. Oscilloscope data from polarization rotation measurement

Further thinning of the electrode gap resulted in poor mode guiding due to proximity to electrodes and cladding layer defects that became more prevalent in thin film depositions.

In-device r_{33} values were estimated using a combination of measured and calculated data. From the expression for V_π it is straightforward to solve for

$$r_{33} = \frac{d}{L} \frac{\lambda}{n^3 V_\pi \Gamma}. \quad (8)$$

V_π was measured as discussed above. The electrode length L is lithographically defined to be 1.6 cm. Scanning electron microscope (SEM) images were taken of finished device cross-sections to measure the electrode gap d and other waveguide dimensions. These measured dimensions were used in a new FDFD simulation to account for fabrication tolerances. The calculated field distribution is inserted into a modified expression for the overlap integral Γ that accounts for the optical mode not being entirely confined within an EO material. This expression assumes that the low frequency modulation voltage creates an electric field throughout the waveguide core with a spatial distribution represented by a two dimensional step function of magnitude V/d in the OEOM, and 0 in the UV15 cladding. The overlap integral then simplifies to

$$\Gamma = \frac{\iint_{OEOM} |E_{opt}(x, y)|^2 dx dy}{\int \int_{-\infty}^{+\infty} |E_{opt}(x, y)|^2 dx dy}. \quad (9)$$

Calculated values of r_{33} were found to be in the range of 60-100 pm/V. The r_{33} values calculated are compared with ATR measurements for the same material and frequency in Figure 15. It is shown that, for samples poled at less than 100 V/ μ m, the poling efficiency of SWPC devices can be duplicated in a waveguide device. This result, to the best of our knowledge, has not been demonstrated in the literature. A substantial effort is currently underway to better understand the poling dynamics in a dielectric stack in order to achieve higher poling efficiencies for higher EO activity OEOMs.

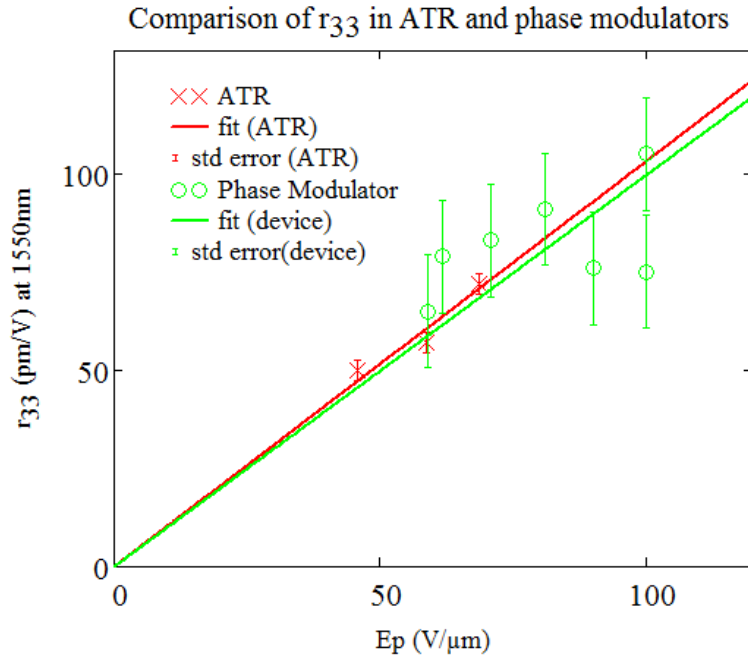


Figure 15. EO activity for organic EO materials in phase modulator (green) and SWPC (red) formats at 1550nm as a function of poling field

The phase modulator was also subjected to long term operational testing while periodically measuring the V_{π} of the device. Although the measurement was significantly impacted by DC drift, a common and readily controlled phenomenon in EO modulators, there was not observed to be any change in the V_{π} of the device over an irradiation window of 2500mWhr. This measurement was taken at 25°C and in air with 20mW launched into the waveguide. This result is important because one of the greatest tradeoffs of polymer modulators is their operational stability, which we show (in Figure 16) to be much better than expected.

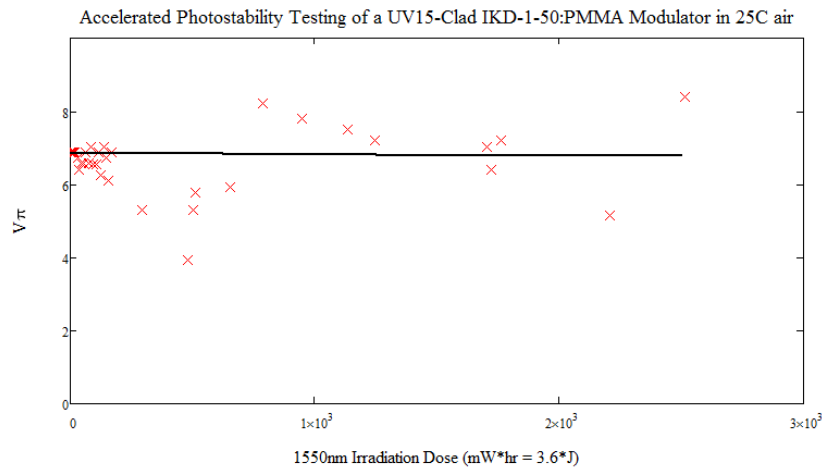


Figure 11. Accelerated operational lifetime testing of a phase modulator.

2.8) All-Polymer Waveguide Modulator: Reduced Optical Loss

Preliminary measurements of insertion loss yielded a best result of 16 dB in a 19 mm long device, referenced to maximum throughput of direct input to output fiber coupling. Significant loss is suffered at the input due to poor mode overlap with the input fiber and additional scattering loss is introduced throughout the length of the guide due to sidewall roughness.

Efforts towards developing a patterning process to produce guide dimensions that will better match the fiber and waveguide mode profiles are underway, as is work towards a new reactive ion etch (RIE) chemistry that produces a smoother sidewall finish. Figure 17 shows results towards these improved RIE processes, where the decrease in surface roughness is apparent.

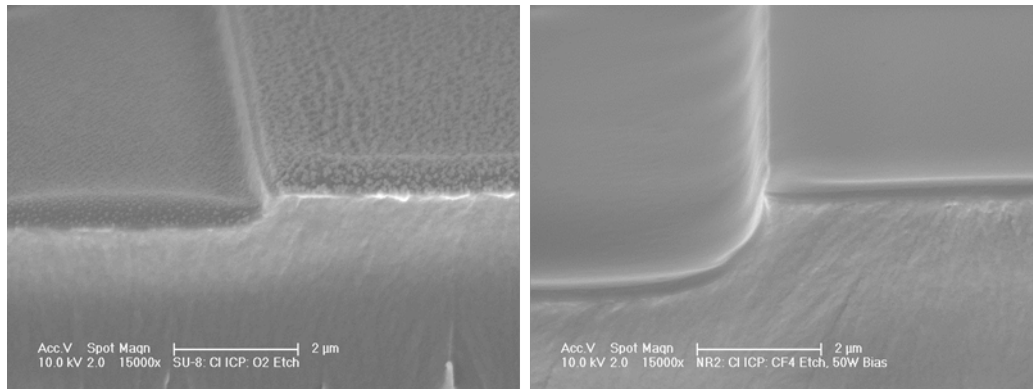


Figure 17. SEM micrographs of trench features resulting from soft mask RIE pattern transfer using O₂ (left) and CF₄ (right)

The left micrograph in Figure 17 shows a trench defined by a SU-8 soft mask, which is transferred by an O₂ plasma etch. As mentioned previously, the SU-8 is consumed by the etch, which limits the depth of the trench to the thickness of the SU-8 coating in proportion to the etch rates of the UV15 and SU-8. Because the SU-8 is etched much faster than the UV15, the trench depth is confined to less than 500nm. However, the newly-developed process for patterning trenches in the UV15 cladding material uses the commercial photoresist NR-2, which etches at a reduced rate compared to UV15. This allows deeper trenches to be etched into the UV15, thereby better matching the mode size and shape of the waveguide to the mode of the optical fiber coupling to it. After etching, the NR-2 soft mask is removed, exposing the smooth surfaces above the trench that result from spin deposition.

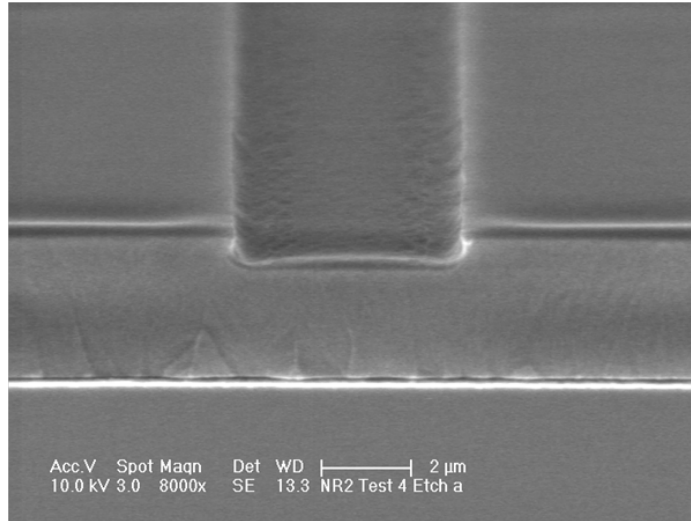


Figure 18. SEM micrograph a waveguide trench resulting from ICP pattern transfer using O_2/CF_4 etch chemistry

In addition, the NR-2 soft mask allows the use of an O_2/CF_4 RIE chemistry, which produces a smoother etch, higher etch anisotropy and reduces the widening of the trench's sidewalls. An example of the results of this new etch process is included in Figure 18. Full devices using these improved etched processes have produced an EO phase modulator with a total insertion loss of 12.8 dB, a 3dB improvement over previous results.

2.9) All-Polymer Waveguide Modulator: Integration of High EO Activity Materials

Device performance is heavily dependent on the material properties of the core OEOM and the simple fabrication process of this device allows for “plug and play” integration of various OEOMs. Recent effort on the APWM has focused on the new etch processes described in the previous section, as well as the integration of SEO250, an OEOM commercially available through Soluxra, Inc., Seattle, WA. The refractive index of SEO250 has been measured to be 1.71 and the EO activity of the material has been measured by ATR to be $r_{33} = 170$ pm/V at 1550nm. Compared with the previously material, IKD-1-50 ($n = 1.57$, $r_{33} = 100$ pm/V), the $n^3 r_{33}$ product can be expected to increase by up to a factor of 2, which would lower the drive voltage V_π by more than 50%. Additionally the higher index contrast between core and cladding materials yields highly confined, more circularly shaped modes in narrower waveguides. This can be predicted to improve optical confinement in the OEOM and fiber mode overlap, as can be seen in Figure 19.

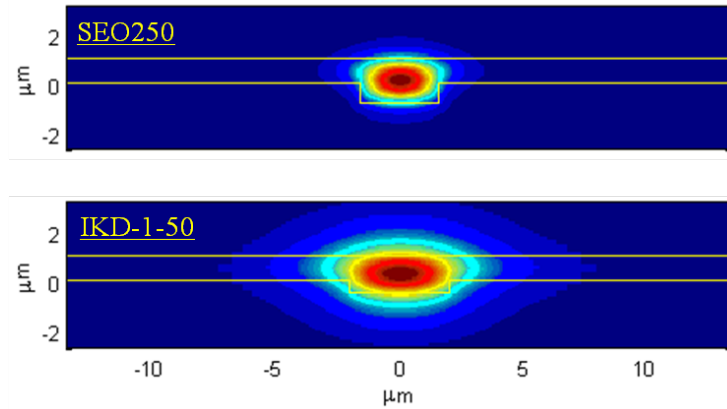


Figure 19. Fundamental TM mode profile for SEO250 device (top) and IKD-1-50 device (bottom)

Integration of SEO250 was achieved with minimal modification to the original fabrication process. The higher poling temperature and thermal stability of SEO250 relaxes the constraints on temperature sensitivity, and all solvent compatibilities achieved for IKD-1-50 transferred to the SEO250 material system. Figure 20 shows an SEM micrograph of a cleaved waveguide cross-section.

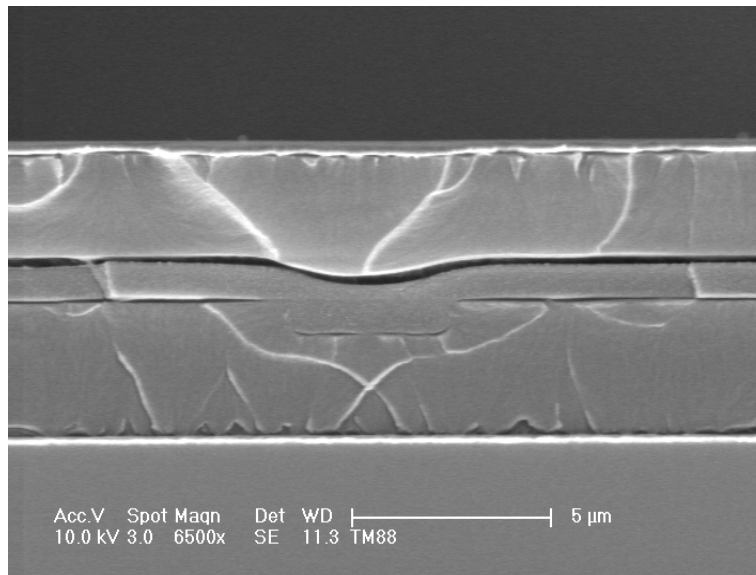


Figure 20. SEM micrograph of a cleaved APWM containing an SEO250 core material.

Minor changes in the poling recipe to account for the higher poling temperature ($\sim 132^{\circ}\text{C}$) including slower temperature and voltage ramp rates were implemented to achieve consistent poling traces. Devices were successfully poled with fields up to $90 \text{ V}/\mu\text{m}$ with peak currents up to $11.5 \mu\text{A}$.

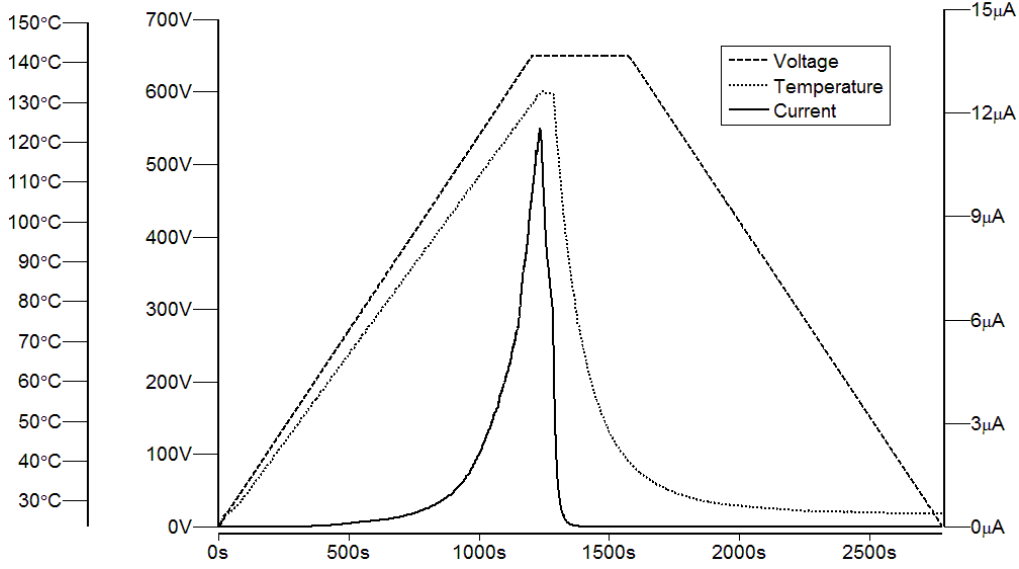


Figure 21. Poling trace for SEO250 APWM device with poling field of 90 V/ μm

Modulation testing was performed using the polarization rotation technique used for all previous devices. The higher index of the OEOM ridge layer caused a higher susceptibility to power leakage into slab modes leading to ambiguous modulation results to due multimode waveguiding. Depositing a thinner SEO250 film suppressed these slab modes and resulted in V_π measurements as low as 2.5 V. This corresponds to a TM V_π of 1.67 and is the lowest measured drive voltage to date. Integration into a push-pull device could reduce the drive voltage to an expected value of 0.83 V.

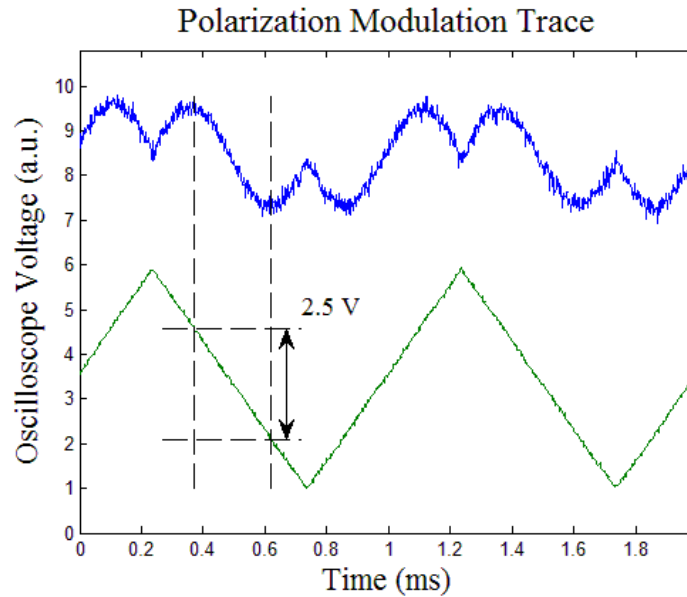


Figure 22. Polarization rotation modulation trace for an SEO250 core APWM.

An in device r_{33} of 107 pm/V was estimated using dimensions from an SEM cross sectional image and a calculated confinement factor using an FDFD mode solution. The device was poled with a field of 84 V/ μm . Efforts are underway towards optimizing the poling process to achieve the higher

r_{33} values expected from this material. These higher EO activity and lower insertion losses measured in the SEO250 APWM devices makes this modulator architecture an increasingly competitive platform for many EO applications.

Another milestone for this work is high frequency operation. The modulation electrodes are in a microstrip electrode configuration capable of supporting a traveling RF wave. RF modeling and design will be done to ensure low loss wave propagation, impedance matching to the RF feed connector, and wave velocity matching with the optical wave. The low dispersion of OEOMs makes velocity matching an easier process than with materials such as LiNbO_3 or Si whose characteristics change significantly over broad bandwidths. Once the device structure has been modified to support high frequency modulating fields the THz response times of OEOMs will be leveraged to modulate over very wide bandwidths.

A significant amount of work has also been put towards increasing the manufacturability of this device, which is a major advantage of all-polymer modulators. Towards this goal, steps have been taken to increase the scale, yield, and throughput of the device's manufacture. Wafer-scale processing is currently being optimized to increase the number of devices which are fabricated in parallel. Die-scale fabrication inherently decreases the variability in device performance, but requires significant attention to processing conditions and new fabrication equipment. In order to increase the yield of the fabrication process, new deposition and material pre-processing techniques are also being explored. New cladding materials are also being evaluated, and, if successfully integrated, will reduce the time required for a wafer run by more than 50%. When these advancements are utilized, the manufacture of this device will be suited for large scale fabrication and integration into high-complexity multiplicative systems, such as metamaterial antenna arrays.

2.10) All-Polymer Waveguide Modulator: Amplitude Modulator Simulations

In addition to the fabrication and testing of phase modulators, designs have been developed for integration into a Mach-Zehnder amplitude modulator. The intended structure splits and recombines a single waveguide mode into and out of two symmetric phase modulator waveguides via a 3 dB MMI coupler, and separates the two structures by bending waveguides defined by a rising cosine function. An MMI coupler was chosen to perform the splitting to minimize device length and the accompanying propagation loss.

The MMI coupler was designed using analytical methods for rough estimation of device parameters, and then optimized using FDTD and a particle swarm optimization algorithm available in the Lumerical Solutions software. The resulting device effectively couples > 45% of light into each of the output arms according to 2.5D FDTD (2D FDTD with the third dimension compressed using the effective index method).

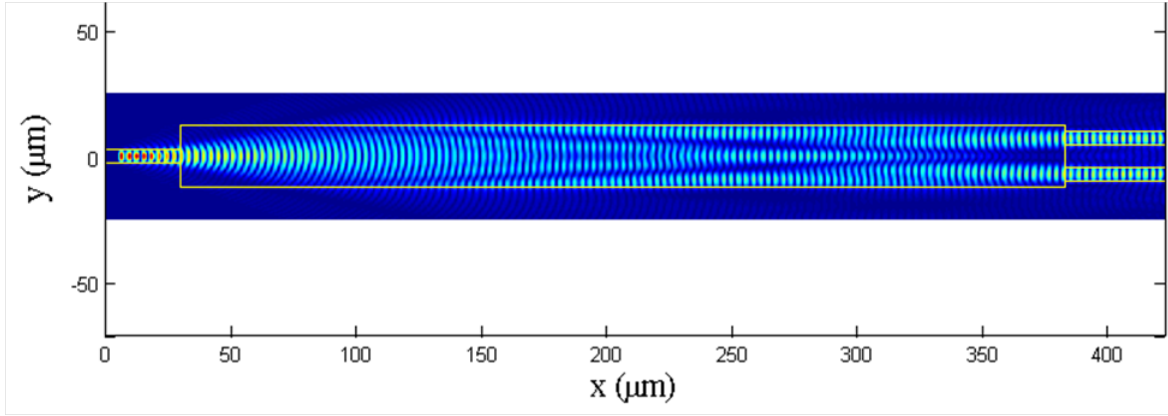


Figure 23. 2.5D FDTD simulation of an optimized MMI cavity showing the propagation of 1550nm light.

The design for the bending section of waveguide was done using an analytical expression developed in Marcuse *Light Transmission Optics*, for bending loss per unit length as a function of radius of curvature. The smooth bending structure is defined by $y = \frac{w_{bend}}{2} \left(1 - \cos \left(\frac{\pi x}{L_{bend}} \right) \right)$ where w_{bend} is vertical distance the bend covers, and L_{bend} is the length over which it bends. Using this expression the radius of curvature and associated bending loss is calculated at discrete points and summed up to estimate total bending loss.

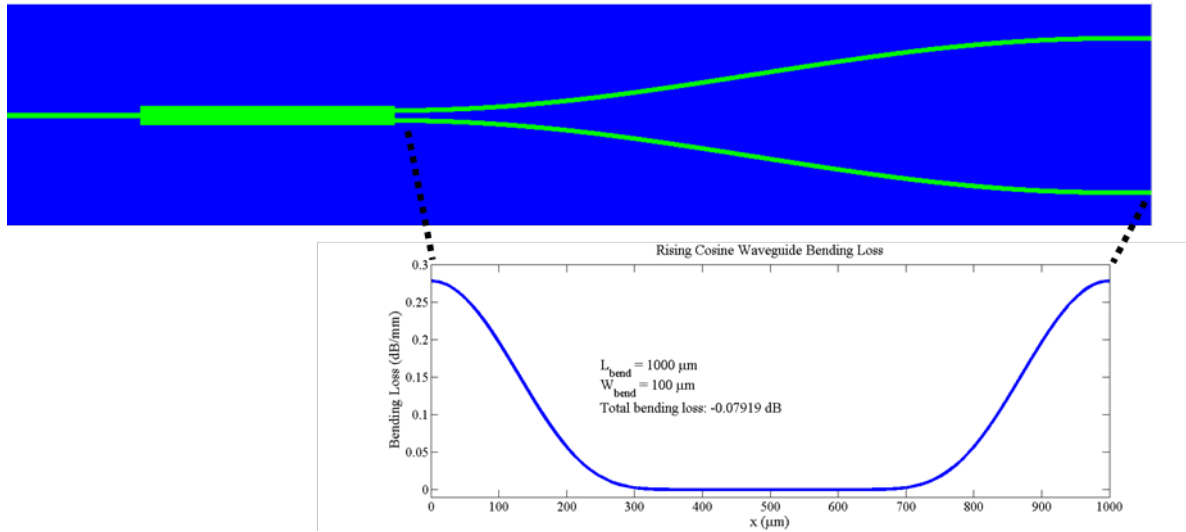


Figure 24. Depiction of the MMI splitter and cos-bend (above) and plot of the cos-bend loss per length (below).

This calculation resulted in a theoretical bending loss of 0.08 dB for a waveguide bending up 100 μm over 1 mm. Four of these structures will be integrated to split from the MMI to the modulation regions and recombine the beam post modulation. The input side of the proposed structure is shown in Figure 24.

2.11) All-Polymer Waveguide Modulator: High Frequency Operation

An ultimate goal of this endeavor is to achieve high frequency operation with continuous bandwidth down to DC frequencies. OEOMs show very little frequency dispersion, effectively bypassing the issue of matching optical and RF velocities that is often a major roadblock in other material systems. The first investigation of high frequency modulation has taken place in the form of simulations using HFSS software. The device is depicted in Figure 25. A CPW electrode on top of a Liquid Crystalline Polymer (LCP) substrate will be contacted with a commercially available SMA to CPW converter. The signal conductor of the CPW can be wirebonded to a microstrip transmission line which is patterned on top of an OEOM. The OEOM device can be bonded to the LCP substrate in order to allow for wirebonding.

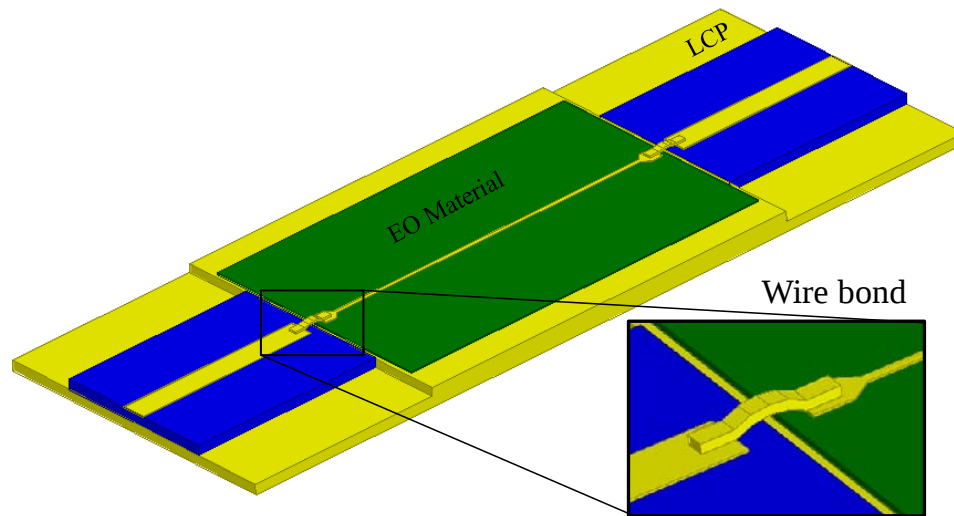


Figure 25. Depiction of the device modeled for RF characterization of OEOMs

This device has been simulated in HFSS using a loss tangent of 0 and a dielectric constant of 2.6. The s-parameters of this device are shown in Figure 26. $S_{12} > -2\text{dB}$ between 0 and 60GHz, indicating that sufficient RF energy will be coupled into the microstrip transmission line, allowing for characterization of the OEOM.

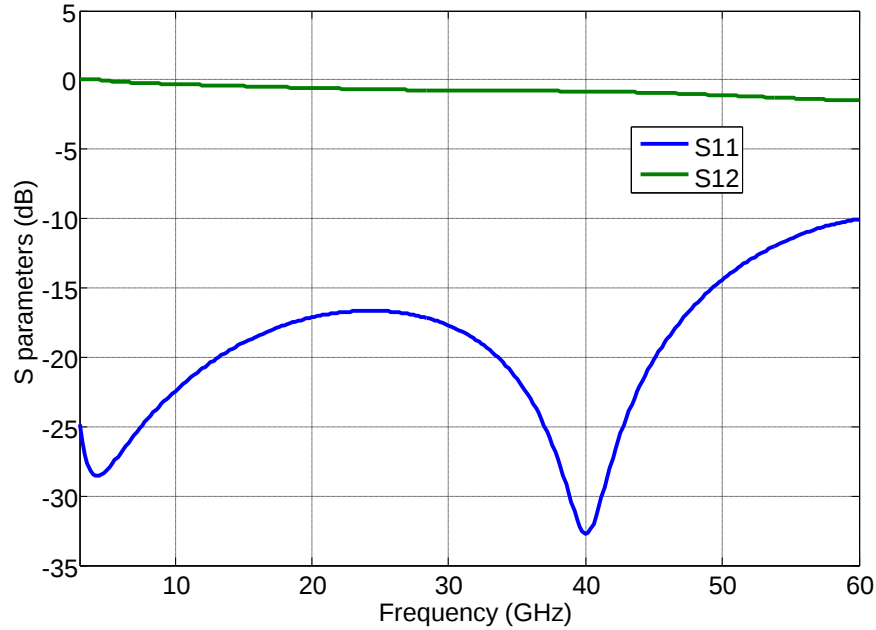


Figure 26. HFSS simulation of S-parameters for the device depicted in Figure 25

The exact, frequency dependent dielectric constant and loss tangent of the organic EO material and cladding can be then used to inform the design and simulation of a modulator chip. The structure of a modulator, similar to the device in Figure 25, will be a waveguide structure buried under the microstrip transmission line, fed by wirebonds to a CPW patterned on an LCP substrate. The microstrip transmission line will have two bends and will be fed from the long ends of the device, allowing an optical fiber to couple to the waveguide on the short device edges.

The microstrip transmission line electrode that carries the modulation signal as the top electrode of the all-polymer waveguide modulator is capable of being optimized to efficiently propagate a traveling wave RF mode. However, the top electrodes currently fabricated are on the order of 75nm, and would not be impedance matched to any high frequency source. In order to improve the impedance matching, electroplating is commonly implemented to increase the thickness of metal electrodes. The primary fabrication challenge is electroplating a sufficiently thick electrode on top of the OEOM-containing waveguide without damaging the polymer structure. An electroplating process that does not raise the temperature of the device above 100°C and avoids any incompatible solvent contact was developed and demonstrated as a proof of concept. Shown below are the electroplated top electrode and the undamaged waveguide cross section post electroplating.

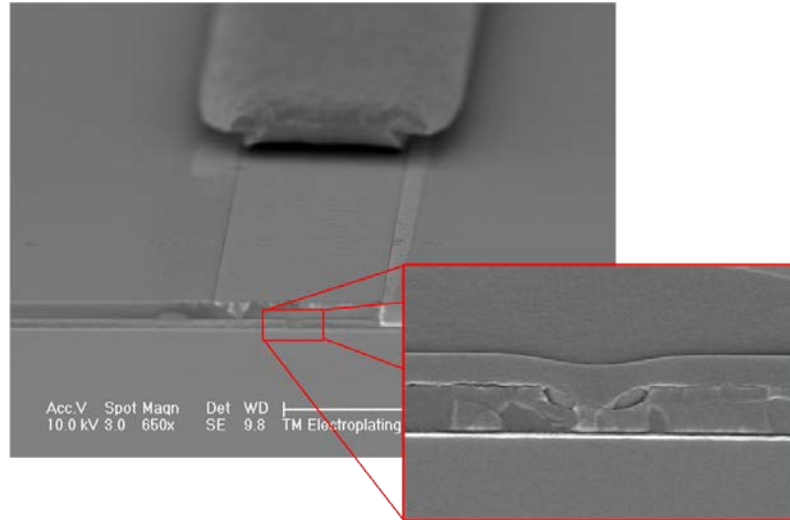


Figure 27. Complete waveguide structure with electroplated top electrode (left). Waveguide structure was undamaged as is seen in the cross section (right).

3.1) Horizontal Configuration Dual-Slot Waveguide Modulator

The effort towards chip-scale optical interconnects is supported by the development and demonstration of high speed, low drive voltage EO modulators. The APWM discussed in the previous section carries the benefit of being highly manufacturable, but is prohibited from containing high dielectric constant materials, i.e. Silicon, which may drastically enhance the device's performance. These materials are commonly employed in a number of photonic devices, most notably utilizing their high refractive index at optical frequencies in order to achieve “slot” enhancement of an optical field within a nano-scale gap. This enhancement, owed to the condition of continuity on the normal component of electric field flux density across an interface, can be leveraged to achieve high modal overlap in the OEOM. This potentially offers unprecedented modulation efficiency, providing that the RF mode can also be similarly confined in the EO material. This challenge is particularly difficult without introducing metal electrodes, and thereby optical loss, within the vicinity of the optical mode. To this end we designed an EO modulator which utilizes the wavelength difference between the RF and optical regimes in order to infiltrate an RF slot waveguide with an optical slot waveguide. This design, depicted in Figure 28(a), confines the RF and optical modes in a nanoscale region of the device which can be backfilled with low index EO material. Towards this purpose OEOMs are best suited. This device was reported to offer < 300 mV drive voltages with bandwidth exceeding 250 GHz, making it ideal for the applications pursued in this effort.

In addition to high-speed modulation, parallel waveguides of this design would also function as a switch for DC applied voltage, and would have the additional advantage of extremely low power consumption, since the EO effect requires no electric current to flow. The dual horizontal slot waveguide modulator can function as a complementary element of the envisioned integrated system-on-a-chip with Coupled Photonic Crystal Waveguide elements, perhaps as a driver for adding a high-speed data stream on to a carrier beam supplied by the integrated sources.

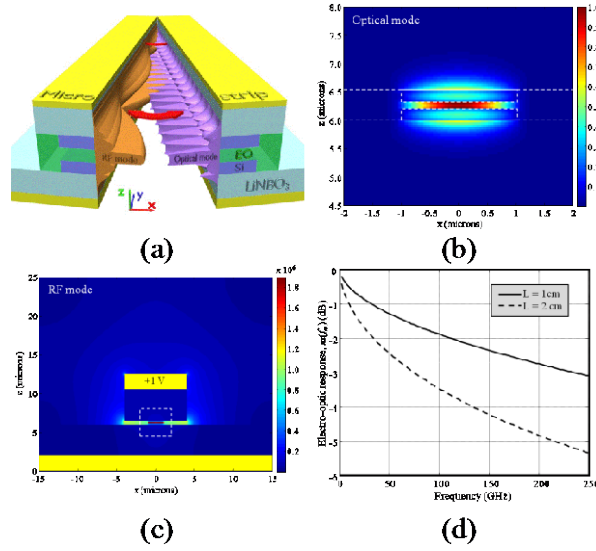


Figure 28. (a) Schematic layout of dual nano-slot waveguide, where the middle cut of the waveguide shows three-dimensional RF and optical mode profiles in the middle plane along the waveguide propagation direction. (b), Optical electric field distribution at a wavelength of 1.55 μm . (c) RF electric field distribution at a frequency of 100 GHz with 1V applied to the signal electrode. The colorbar scale confirms the field concentration near 2 MV/m within the low index EO polymer infiltrated slot. (d) Electro-optical response of the proposed modulators with different modulator lengths of 1 and 2 cm.

As depicted in Figure 28(a), the dual horizontal slot waveguide consists of a lower index organic EO polymer sandwiched by two silicon membranes. The slot waveguide is then enclosed in a microstrip line with ferroelectric materials, i.e., LiNbO_3 or TiO_2 , as its cladding layers. These ferroelectric materials have low optical refractive indices and very high RF dielectric constants compared to silicon. As a consequence, strong optical and RF modes can be simultaneously established in the nano-slot where the nonlinear EO polymer resides, as shown in Figure 28 (b) and (c), thereby leading to a large mode overlap. In addition, the high-dielectric-constant material potentially allows for an increased electrode separation between signal and ground without significantly scarifying the electric field confinement in the slot. As a result, the driving signal mode will experience reduced conduction loss. This becomes of particular importance for operation of the modulator at high frequencies. In addition, the device is carefully optimized to minimize an index mismatch between RF and optical guiding modes as low as 0.007 at high frequencies. Preliminary simulation results demonstrate the DC electro-optic response and half-wavelength voltage-production $V_\pi \cdot L$ of 0.1–0.2 V·cm can be achieved for this design, which is about two orders magnitude lower than that of conventional LiNbO_3 EO modulators. The electro-optic response, as shown in Figure 38(d), demonstrates the proposed device is capable of ultra-high speed operation. Silicon nano-membrane technology will be directly employed for the fabrication of the proposed EO modulators.

3.2) Horizontal Dual-Slot: Design

In the efforts towards developing a high-speed dual-slot modulator, a fabrication process was developed along with an analysis of coupling from fiber to waveguide and then to a slot waveguide. This process focused on increasing the yield of transferring the silicon optical waveguide layers into a horizontal slot waveguide configuration while the substrate immediately behind the area of interest is removed. This completed process is depicted in Figure 29 shown below, and allows independent fabrication of two individual passive device stacks that are then assembled by using the OEOM as an intermediate bonding layer. The first substrate is fabricated by depositing the gold signal electrode and titanium dioxide film and silicon via liftoff. The 3 μm titanium dioxide film is deposited using a reactive sputtering process using a simultaneous DC and RF argon/oxygen plasma. The second (top) substrate is fabricated using the same processing as the first, however conformal depositions are performed to reduce the need of critical chip-to-chip registration during the bonding of the two substrates. The sandwiched substrates with a coplanar OEOM film, results in a structure that replicates the designed geometry to align the RF and optical mode.

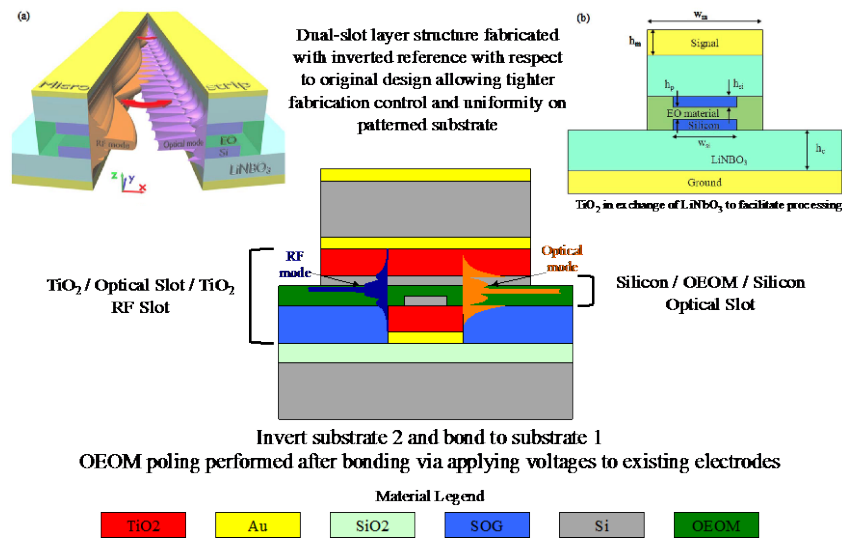


Figure 29. Developed fabrication process of horizontal dual-slot waveguide, showing completed layered structure formed by the individual fabrication of two substrates and the bonding of the two substrates by OEOM

Upon the development of the discussed fabrication process, a mask set was fabricated to allow the optical and RF fields to couple into the dual-slot structure, shown on the left. Shown on the right in Figure 29, is a concept rendering of a finished dual horizontal slot waveguide modulator showing one patterned modulator on Substrate 1 (S1) with Substrate 2 (S2) bonded over top with electrical contact for the ground plane. Processing allows multiple modulators on S1 to be patterned in parallel, such that one S2 can be dimensioned and bonded to multiple samples at once.

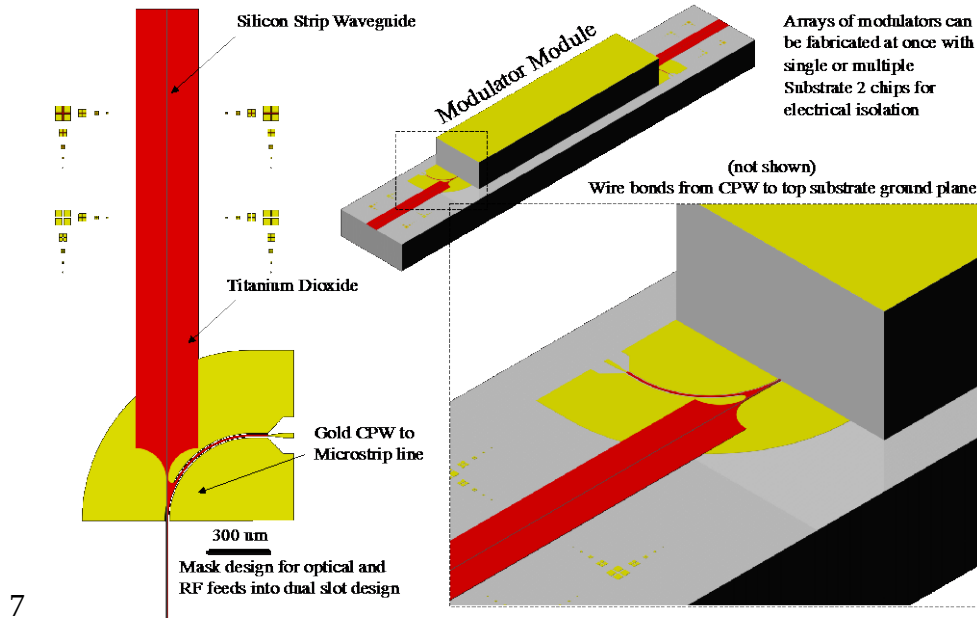


Figure 30. Concept rendering of assembled dual horizontal slot waveguide modulator

3.3) Horizontal Dual-Slot: Fabrication

Initial fabrication processing was focused on the reactive sputtering process to deposit 3 μm thick TiO_2 films using lift-off. The gas ratio of argon:oxygen 10:3 was found to reactively deposit an optically transparent titanium dioxide film from titanium targets while maximizing the deposition rate. Additionally, in this processing, a photoresist film of Futurrex NR-9 1500PY is spun and patterned, and using the inherent shadowing of a sputtered film on high aspect ratio features, liftoff of a 3 μm film is achieved with only a 1.5 μm resist feature. The resultant titanium dioxide structures on SiO_2 and on a gold CPW-to-Microstrip line are shown in Figure 40. Some surface roughness is visible, however this is to be addressed using a spin-on-glass (SOG) backfill process with a mechanical surface lapping or RIE process. The reduction of surface roughness is critical since the roughness of the silicon in the optical slot waveguide is defined by the underlying substrate roughness.

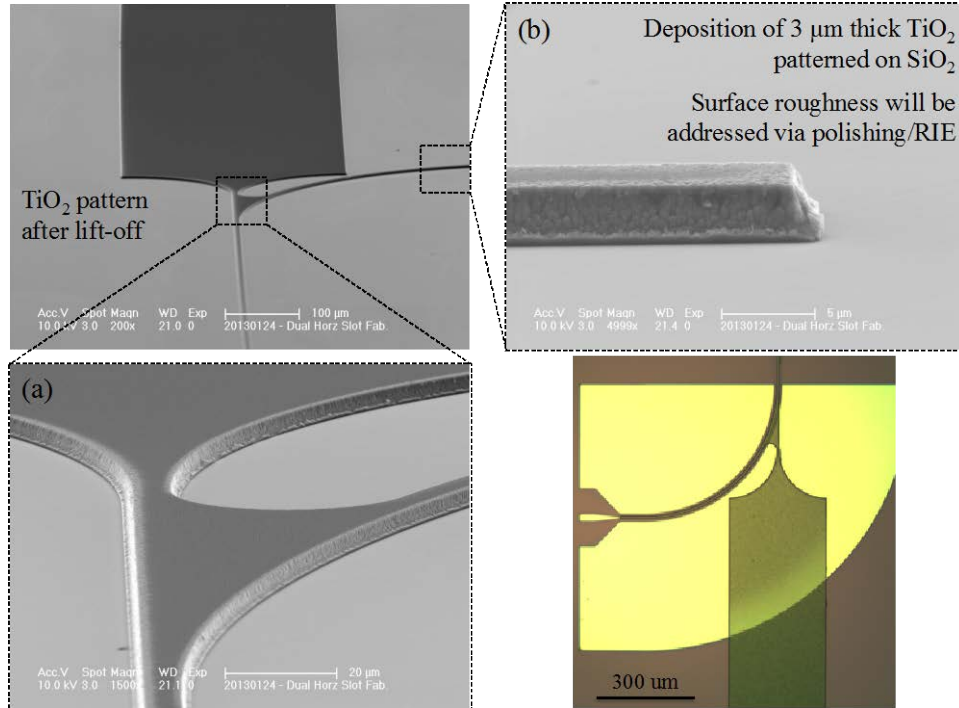


Figure 31. Patterned titanium dioxide film deposited via reactive sputtering of a titanium target using 10:3 Ar:O₂ plasma. The patterned was fabricated using liftoff processing on both silicon dioxide substrates and gold CPW-to-Microstrip metallization. (a,b) Magnified angle view showing clean liftoff of 3 μm film

During the initial fabrication of the layer stack for the patterning and lift-off of the titanium dioxide layer on top of the CPW-to-Microstrip metallization, premature delamination of the masking photoresist occurred mid-deposition, causing the TiO₂ film to be deposited in unwanted regions. To alleviate the issues of premature delamination, a titanium film of 100 nm was deposited on top of the gold during the original evaporation of the CPW metallization. Additionally, an O₂ and Ar plasma clean is performed on the sample immediately before the sputter deposition of the TiO₂ to remove any organics and surface oxides from the previous metallization lift-off and residuals from the resist development of the NR9. The resultant processing increased the yield of performing a lift-off of the thick TiO₂ film without premature delamination of the masking resist during the sputter process.

Upon the fabrication of the two substrates S1 and S2, a passive version of the dual horizontal waveguide structure for RF characterization was assembled by spinning a layer of 450k PMMA A4 without active chromophore onto S1 structure and then flipped and bonded a smaller chip of S2 on top of S1. The exposed PMMA on the underlying substrate was then removed using an O₂ plasma clean to facilitate electrical contact of the CPW region. The assembled device structure is shown in Figure 32.

3.4)

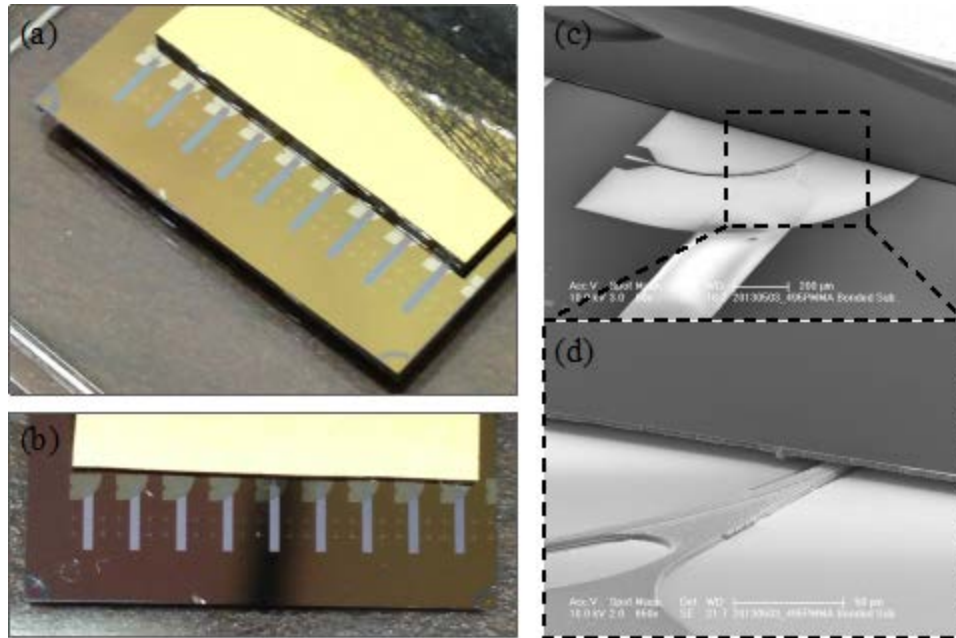


Figure 32. (a,b) angled and top view of an assembled array of dual slot waveguides; (c,d) SEM images of assembled structure.

This bonded device offers a proof of concept for the fabrication process. However, to achieve the nanoscale confinement of an optical mode, the OEOM bonding layer is required to be a uniform 100nm thick film. This thickness is much less than the average step-height resultant from the patterned materials on each substrate, making the bonding process incompatible without a significant degree of planarization of each substrate prior to bonding. Efforts towards this end are underway, utilizing deposited planarization films and counter-etching the surface profile for the preparation of an ultra-fine surface lapping procedure to achieve the sub-5 nm roughness to support operation. In tandem with the development of a planarization procedure, efforts towards the production of this modulator are being shifted to the vertical configuration, which are articulated in the following sections.

4.1) Vertical Configuration Travelling-Wave Dual-Slot Modulator

In parallel with the effort to fabricate the dual slot waveguide modulator in a horizontal configuration, production of this device in the vertical configuration has also been pursued. To realize the dual-slot modulator based on vertical geometry requires deposition and/or nano-scale patterning of (at least) four types of distinct materials:

- Metal: to form electrodes for the RF waveguide.
- Organic electro-optic material: low-refractive-index material exhibiting second-order nonlinearity that fills the slot where the interaction between the optical and the RF modes takes place.
- High-index optical, high-index RF material: to confine both the RF and the optical electromagnetic fields in the slot region. In our research we use silicon here for availability of material and relative ease of processing.
- Low-index optical, high-index RF material: to confine RF field, and to separate the optical mode from the metal electrode. In our research, we narrowed the choice to titanium dioxide, which can be deposited via reactive sputtering or by oxidizing evaporated titanium.

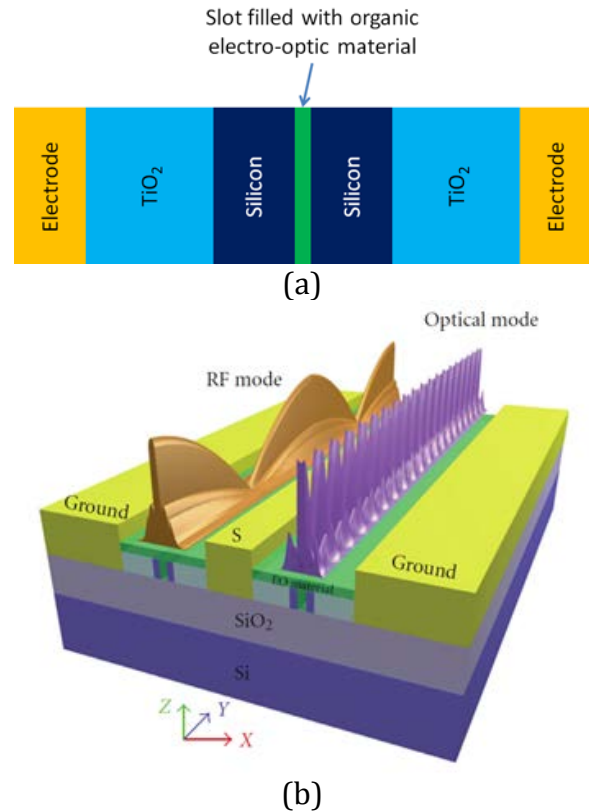


Figure 33. (a) Section across an ideal dual-slot modulator. (b) 3-dimensional depiction of a push-pull modulator with overlaid RF and optical fields.

Figure 33 (a) shows an idealized geometry of a dual-slot modulator indicating the placement of the various materials listed above. Figure 33(b) shows an artist's rendition of a modulator utilizing the dual slot concept; note that both the RF and optical fields are collocated in each of the slots forming a push-pull modulator—for clarity, the figure shows either mode in each of the arms.

The device is fabricated in the following sequence of steps:

1. The slot waveguide is patterned in silicon on insulator (SOI) using e-beam lithography and reactive-ion etching. Here, we take advantage of the fixed-beam moving-stage (FBMS) of our tool, which enables defining long waveguide without the necessity of stitching fields, and a Bosch-like process for defining vertical sidewalls in silicon.
2. Cladding flanking the waveguide is defined using UV or electron beam lithography.
3. TiO_x is deposited and lifted off outside of the cladding regions, or can be deposited without a pattern due to the aspect ratio of the slot
4. Metal electrodes are patterned by UV lithography and electroplating.
5. EO polymer is deposited and poled.

Each of the steps listed above must be optimized to produce a modulator with the required low V_π , and sufficiently low losses to be useful in the application considered in this project. To this end, in developing the fabrication process for the device, we have pursued several threads, as presented below.

4.2) Vertical Dual-Slot: Introducing Moiré Alignment Marks for Improved Overlay

The cladding defined using UV lithography in step 2 of the fabrication process must be very well aligned with the waveguide—too much of an overlap with the waveguide, or too wide a gap between the silicon and TiO_2 would compromise the performance of the device. Yet, the waveguide is only several hundred nanometers wide, and the resolution of an optical alignment system is at best a micron. As a result, conventional alignment marks are inadequate to the required overlay accuracy. Therefore, in this project, we developed a Moiré-based alignment.

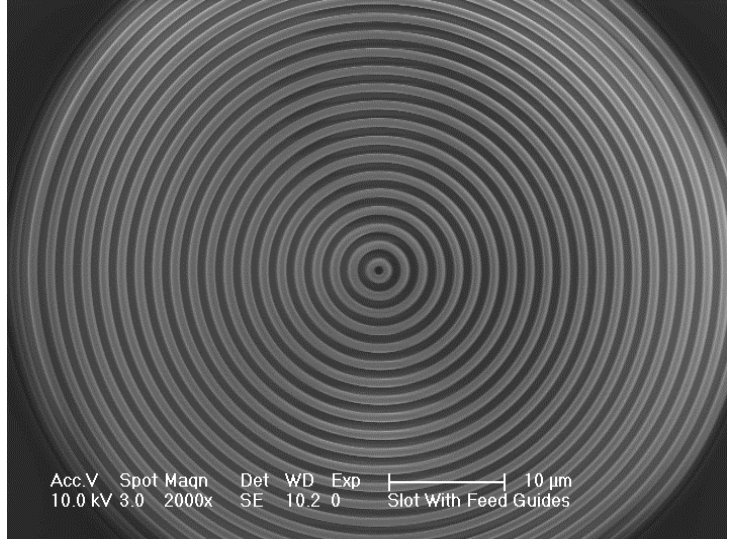


Figure 34. Moiré alignment mark consisting of a set of concentric rings.

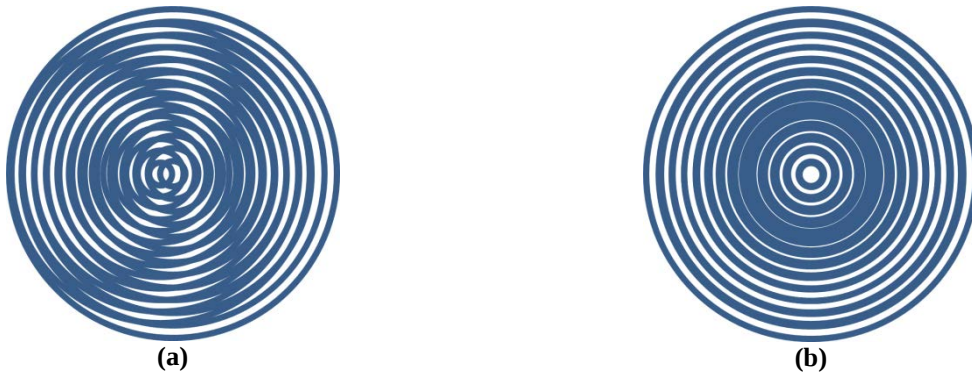


Figure 35. Depiction of the overlay of Moiré alignment marks. (left) Misaligned by about $\frac{1}{2}$ of the ring pitch. (right) Perfectly aligned.

To this end, the alignment marks consist of a set of concentric rings as shown in Figure 21. The pitch between the rings on the photo-mask differs slightly from the pitch in the rings patterned using e-beam lithography. As a result, when overlaid in the mask aligner, a distinct Moiré pattern emerges, Figure 35, that has visible features considerably larger than the feature size of the rings themselves. In our case, we used 10% difference in pitch between the photo-mask- and the e-beam-defined alignment marks, which allowed us to see misalignment 10 times smaller than would be otherwise possible. In fact, thanks to using this type of alignment mark, we are no longer limited in our alignment accuracy by the mark visibility, but rather by the mechanical adjustment of the micrometer screws in the mask aligner: we can see misalignment of a hundred nanometers, which is

smaller than the minimum adjustment that can be done using the micrometer screws. Such overlay accuracy is adequate for this project.

4.3) Vertical Dual-Slot: Design and Fabrication of a Transition to a Broken Slot waveguide

For the proper operation of the slot waveguide, the two arms of the waveguide that are separated by the slot must be electrically isolated. Yet, the waveguide starts as a single-mode solid waveguide without the slot to allow efficient coupling to the optical fiber. The slot is introduced only in the later section of the waveguide, as shown in Figure 36. As a result, silicon forms a continuous path that essentially shorts the RF electric field used for modulation. Therefore, it is necessary to introduce a cut to isolate the two arms of the slot waveguide from the Y split.

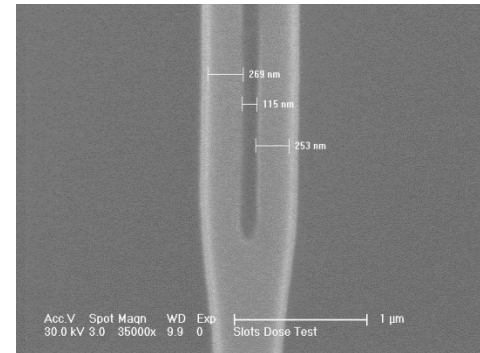


Figure 36. Y-split of a waveguide to introduce slot.

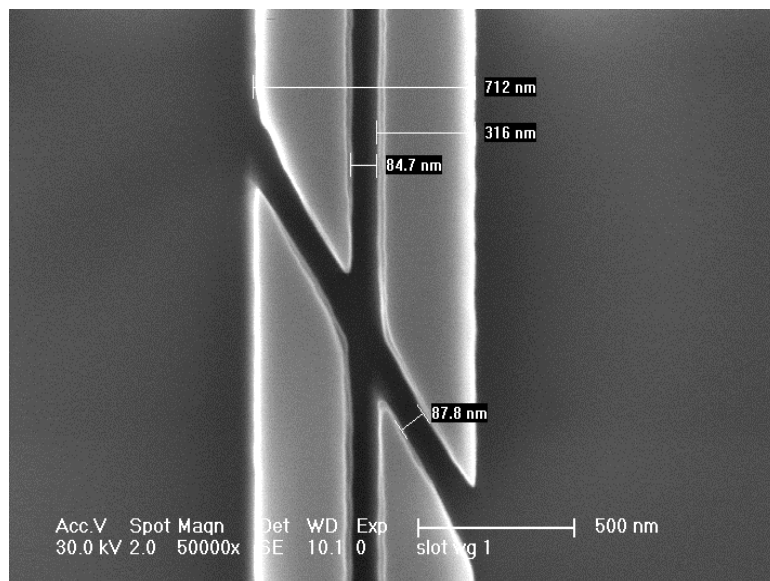


Figure 37. Cut across a slot waveguide for electrical isolation of the two arms.

The cuts used in the existing literature limit the practicality of the device as they require careful alignment of the cut to the slot; in fact the required alignment accuracy is beyond the ability to pattern for our state-of-the-art e-beam lithography tool. Therefore, for this project, we developed a different cut geometry that is more tolerant to misalignment, Figure 37. The electromagnetics simulations of optical modes transitioning from a single mode waveguide to an isolated (broken) slot mode are shown in the figure below. This design represents the best result from many iterations of various coupler designs and parameters without sacrificing attention to the limitations of nanofabrication. Endfire coupling to a single-mode waveguide, which transitions on-chip to a slot waveguide, is necessary to avoid prohibitive coupling loss penalties.

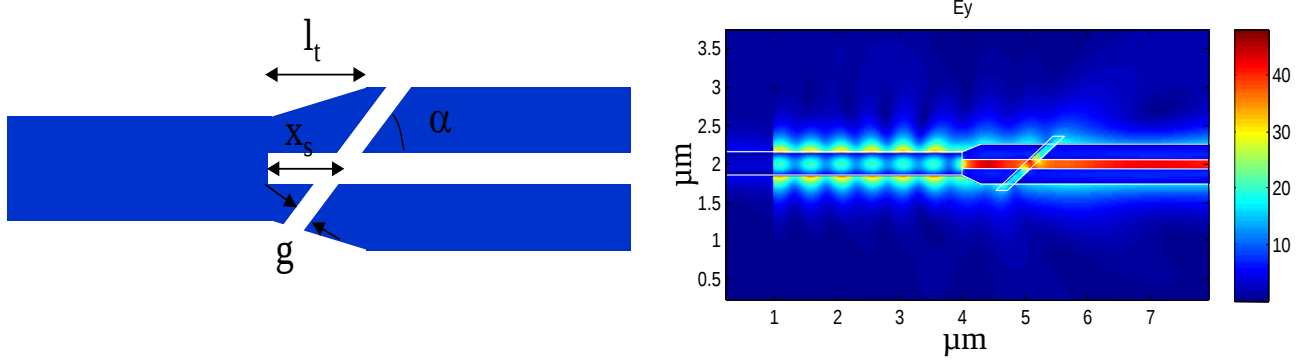


Figure 38. Parameterized depiction of the 300 nm wide single-mode silicon waveguide to 120 nm wide broken slot waveguide transition. This design utilized the following parameters $x_s=1\ \mu\text{m}$, $l_t=300\ \text{nm}$, $g=60\ \text{nm}$ using 200 nm silicon ribs to clad the slot. This device exhibited 82% coupling efficiency to the slot waveguide.

To achieve high coupling efficiency, the width of the cut must be kept as small as possible. Here, we are limited by the resolution of the lithography tool and by the etch process. Figure 37 shows that thus far we were able to reduce the width of the cut to below 100 nm. While very small, we are still working on reducing it further to improve the optical coupling to the slot section of the waveguide.

4.4) Vertical Dual-Slot: Titanium Dioxide RF-Slot Cladding

As pointed out above, the cladding must be positioned precisely around the silicon slot waveguide. At the same time, the material must be of optical quality to ensure efficient guiding of the optical beam with minimal losses. To achieve a high quality TiO_x film, we explored several methods of deposition including direct sputtering of TiO_x , reactive sputtering of titanium in oxygen-rich atmosphere, and evaporation of titanium followed by oxidation. The first method suffers from relatively low rate and questionable quality of the film. In the case of the evaporation of titanium followed by oxidation, we discovered that the process must be carried out in several steps: trying to deposit the target thickness of titanium in one step leads to cracking of the film due to stresses induced by the introduction of oxygen. Whereas films produced by multi-step deposition/oxidation can have high quality observed under SEM inspection, this method routinely resulted in high optical losses compared to slots clad with TiO_x deposited using reactive sputtering.

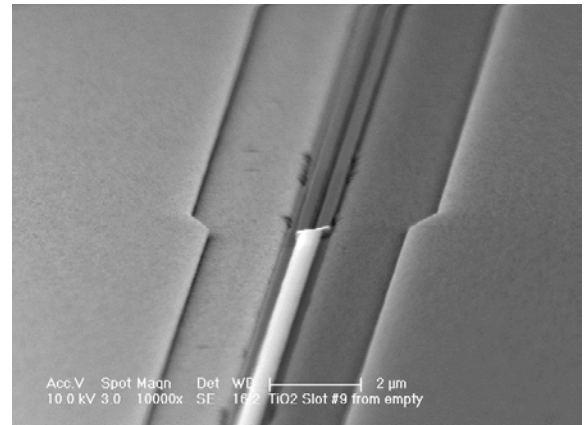


Figure 39. Dual-slot waveguide modulator following the deposition and lift-off of titanium dioxide.

Figure 39 shows the device following the deposition and lift-off of titanium dioxide. In this case, high quality TiO_x films have been obtained, and the cladding pattern is well aligned to the silicon waveguide. There still remain gaps between the silicon ridges and the TiO_x cladding; we are currently in the process of analyzing if such gaps would compromise the performance of the device,

and if so, to what extent. At the same time, we are also working on methods to limit the size of these gaps or eliminate them entirely.

In this figure, of interest is pointing out that the section of the waveguide without the slot appears brighter than the section with the slot. The difference in contrast is the result of electrical isolation of the ridges by patterning the cut as discussed above. In other words, the ridges are electrically floating, which in the scanning-electron-microscope (SEM) imaging manifests itself as a different contrast compared to a section that is electrically grounded. This SEM contrast is a diagnostic tool that provides an easy way to determine whether the cut across the waveguide indeed introduced electrical isolation as required for the operation of the dual-slot modulator.

It is our experience that the highest quality TiO_x coatings have resulted from a blanket coating the silicon optical slot using our reactive sputtering system. By carefully calibrating the sputtering process, we can take advantage of the shadowing effect which is apparent in Figure 35 outside the slot, to prevent the filling of the optical slot. Instead we see a narrowing of the slot from 100 nm to about 50 nm after deposition of 300 nm of TiO_x . This reduction in slot width should increase both optical and RF mode confinement, lowering the V_π of the device. Perhaps more importantly though, is that no lengthy alignment process is necessary. Being able to avoid liftoff entirely leads to higher throughput of devices and a much cleaner slot, as re-deposition of debris into the slot is not an issue (which can be seen in Figure 39).

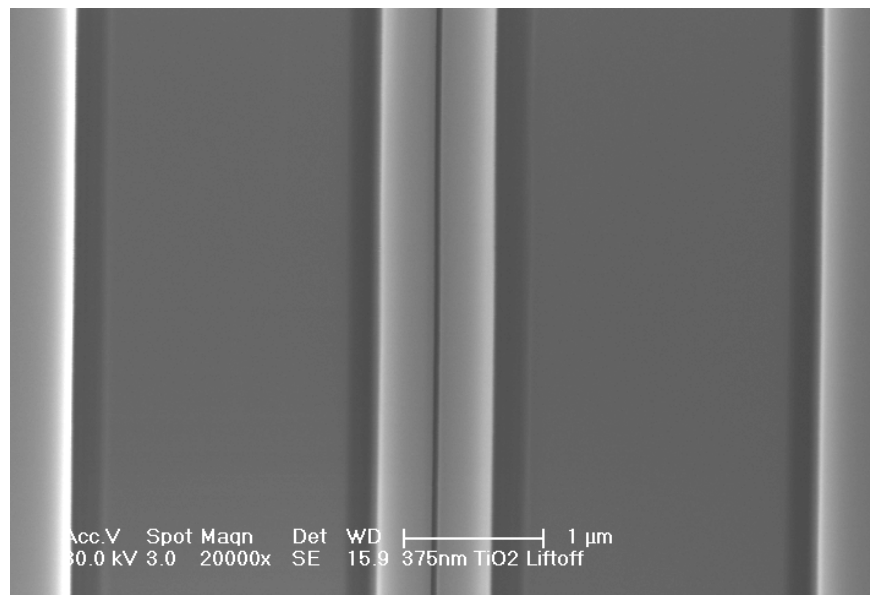


Figure 40. Blanket coated dual slot waveguide showing 50 nm slot width.

4.5) Vertical Dual-Slot: Patterning Electrodes for Poling and Low-Frequency Test

The electrodes are patterned using conventional UV lithography and electroplating. Since Gold does not adhere well to the dielectric layer of titanium dioxide, an additional thin pure Titanium layer can be used for adhesion during later processing routes. Since the placement accuracy of the electrodes is not as critical as that of the cladding, conventional alignment marks are used that allow about 1 μm overlay alignment. Figure 36 shows the dual-slot waveguide modulator with metal electrodes (white areas on the left and right sides of the image) patterned outside of the cladding regions. Note that the metal appears much brighter than silicon under the SEM, and in this case caused the saturation of the secondary-electron detector to produce white bands.

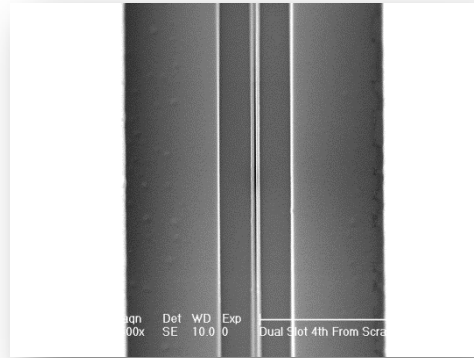


Figure 41. Dual-slot modulator with patterned cladding and metal electrodes.

We have found that the throughput of devices and cost efficiency can be greatly enhanced by depositing aluminum electrodes during a long evaporation cycle. The Aluminum is then capped with 20 nm of Gold to prevent oxidation. Hochberg *et. al.* have demonstrated that aluminum electrodes are substantially conductive at the frequencies of interest at this time.

4.6) Vertical Dual-Slot: Polymer Back-Fill

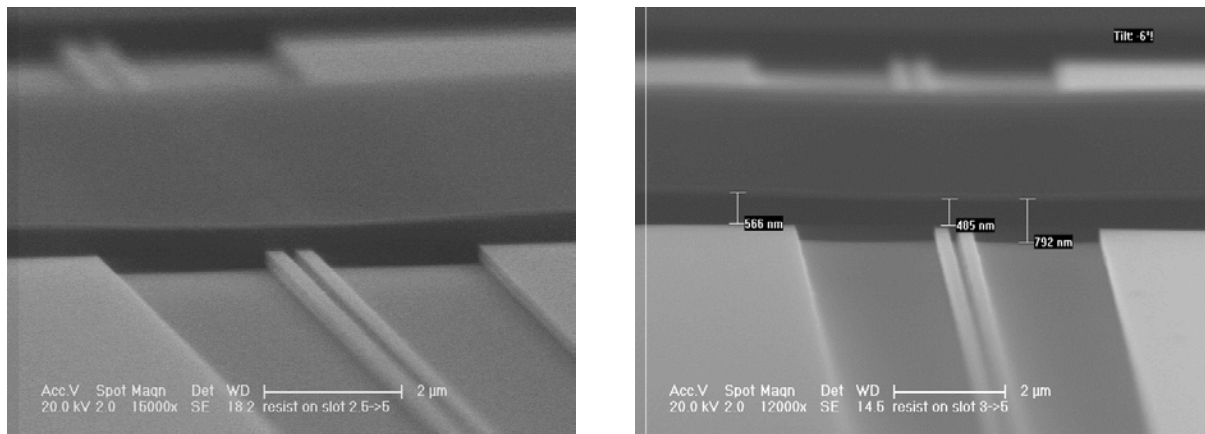


Figure 42. Dual slot filled with polymer.

The final step in the fabrication of the dual-slot modulator is the deposition of the electro-optic polymer in such a way as to ensure that it fully infiltrates the slot, and poling it by applying high DC voltage to the metal electrodes patterned in the previous step. Due to the high cost of electro-optic polymer, in the fabrication-process development, we used a less expensive substitute to minimize the expense. Although we anticipate that the introduction of chromophores, the component that endows the organic electro-optic material with the second-order nonlinearity, to the polymer host

will alter its properties to some extent, the change will be sufficiently small to allow the use of the developed process with only minor modifications.

Figure 42 illustrates our progress in the controlled deposition of polymer within the dual-slot-waveguide modulator. The images clearly show that the polymer fully infiltrates the slot as required for the operation of the modulator. Furthermore, the figure shows excellent quality of the film, which is only barely perturbed by the presence of the surface features underneath. This result allows us to be optimistic about the ability to back-fill the slot with the EO polymer used in the final device.

For initial poling experiments, the OEOM IKD-1-50 doped 25 (w/w)% in PMMA, was deposited using a standard spin deposition technique followed by a 65°C soft bake step and an overnight 85°C anneal *in Vacuo*. This material has been extensively tested using thin film SWPC devices as well in simple phase modulator formats including the APWM described in above. It was selected for this study because it has exhibited highly reproducible processing and high EO activity, >100 pm/V in device at 1550nm.

4.7) Vertical Dual-Slot: Production and Poling of Prototype Devices

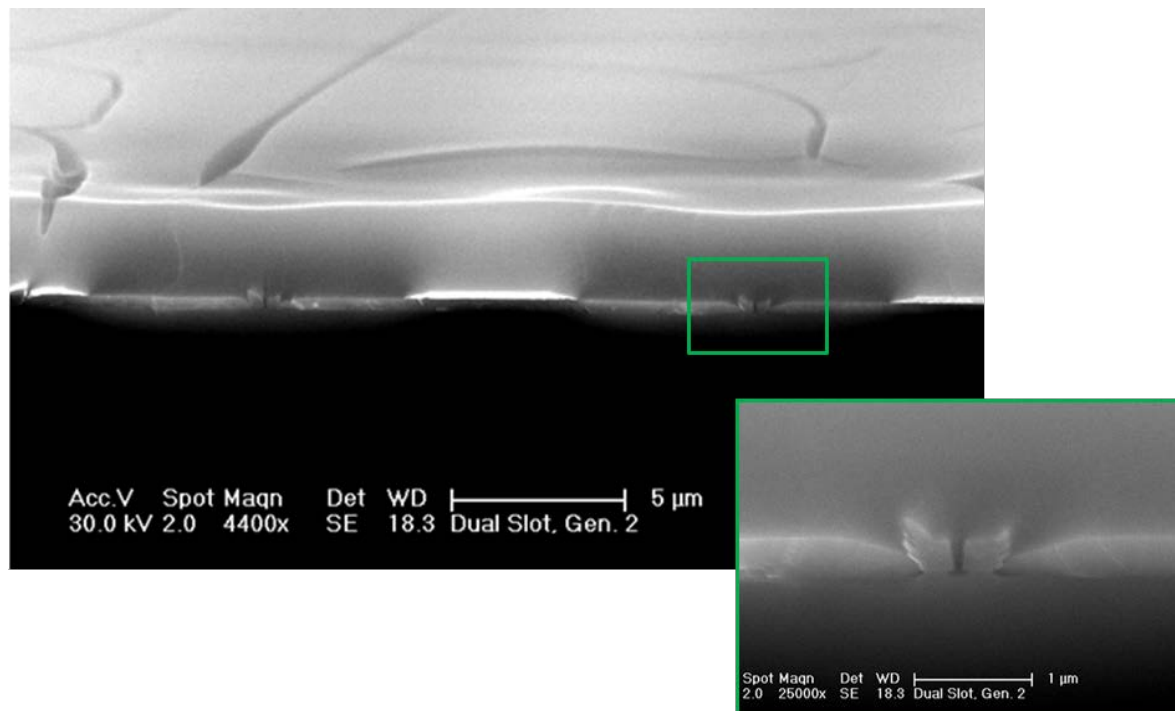


Figure 43. Completed dual slot modulator showing integrated optical and RF slots, as well as 500nm aluminum electrodes and slot-infiltrated OEOM. The inset shows the Silicon slot, including “wings” of TiO_x that result from the liftoff process.

The culmination of the fabrication steps explored in the previous sections is shown in figure above. It has also been observed that the most successful devices, measured largely with poling current as the feedback parameter, are a result of reactive sputtering of the TiO_x with liftoff resist patterned using e-beam lithography, rather than the blanket coating alternative mentioned above. The sample is then annealed in an N₂ environment at about 700°C. This process converts the sputtered

amorphous TiO_2 to a higher dielectric constant, low optical index "rutile" form. Several other annealing recipes were attempted but did not reproduce the optical loss and poling efficiency of this procedure. Simple needle-probe landing pads are implemented during the prototype fabrication phase, and are shown in the figure below. Also visible in the figure are baffles, which serve to reduce the loss of guided energy via radiation into slab modes.

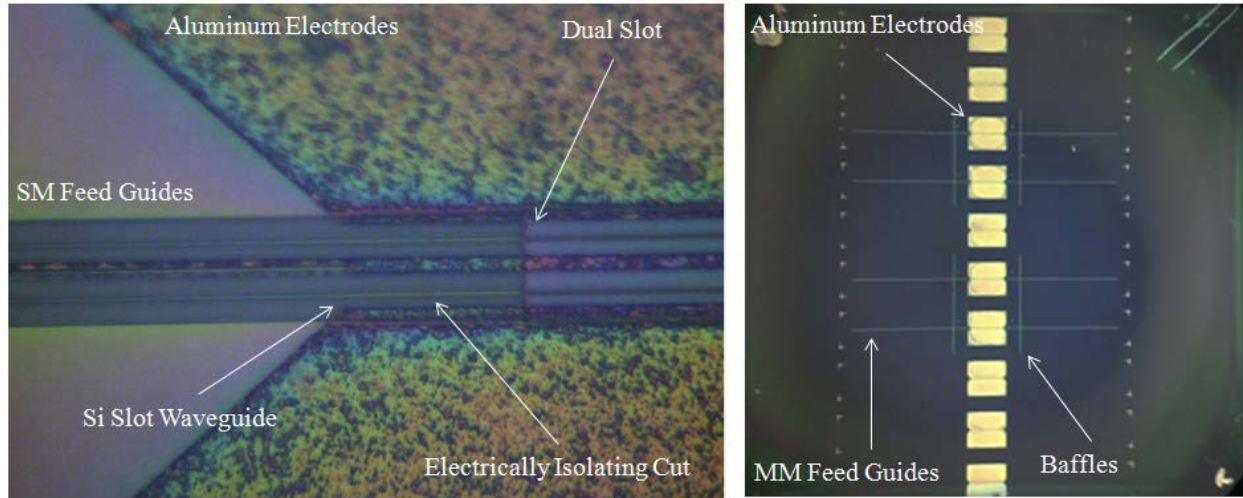


Figure 44. Fabricated devices with OEOM deposited, immediately before the poling process.

These CPW electrodes were probed during poling in a manner which would allow push-pull operation when an RF mode is launched down the GSG transmission lines. All CPWs are fabricated with a signal electrode width of $6\ \mu\text{m}$ and ground-signal gaps of $7\ \mu\text{m}$. For each device slot region was $0.9\ \text{mm}$ in length. The device was poled using identical equipment and procedures to the APWMs detailed above. Typical poling voltages, temperatures and leakthrough currents for two samples are plotted below.

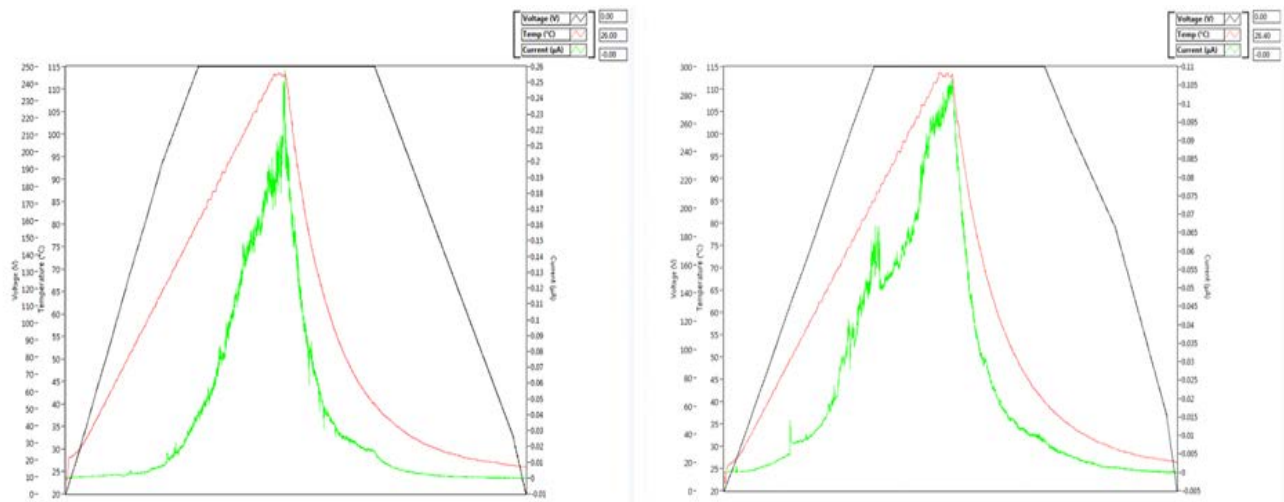


Figure 45. Consecutive poling traces of different waveguides on same sample.

It is worth noting that the dielectrical phenomenon that give rise to an enhancement of the modulating field present in the RF slot also enhance the poling field in the OEOM. For example, after applying a field of 300 V across a 14 μm electrode gap we were able to back out an r_{33} of 60 pm/V $\pm$ 10%. This material routinely affords 1 pm/V of EO activity per applied volt during poling, which would result in an $r_{33} = 21$ pm/V without enhancement afforded by this device.

4.8) Vertical Dual-Slot: Characterization of V_π

In order to observe modulation in the devices, each was coupled to a 2.5 μm mode field diameter lensed optical fiber via endfire coupling. Drive voltage were characterized as straight-through phase modulators using the polarization rotation technique described above. Although the polarization method is best suited for waveguides that propagate a TE and TM polarized mode, it can also be applied to slot waveguides if the mode orthogonal to the slot mode (in this case TM) is supported without radiating to slab modes or otherwise spatially dislocated to prohibit coupling to the single-mode silicon ridge output guide. This assumption is supported for the vertical configuration dual slot waveguide modulator by the FDFD simulations shown below.

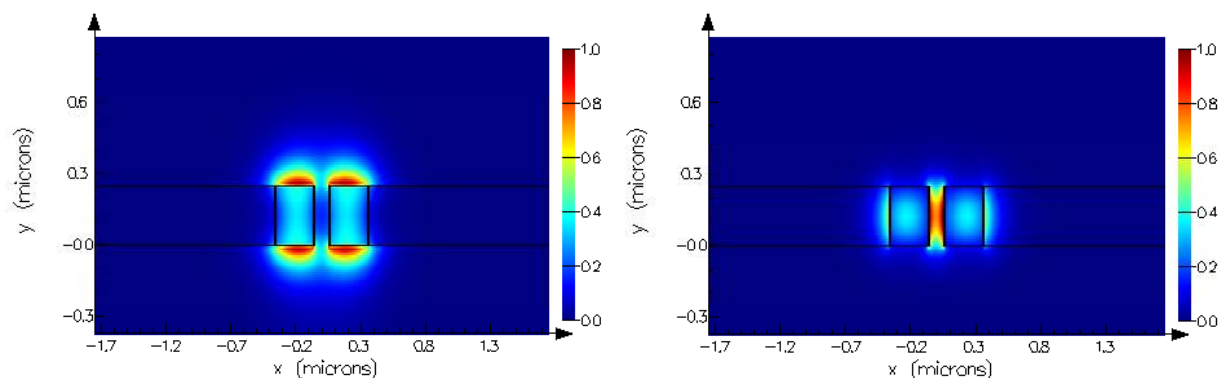


Figure 46. FDFD simulations of vertically-polarized electric field intensities for the TM mode (left) and horizontally-polarized for the TE mode (right) for standard dimensions of the slot waveguide cross-section afforded using the fabrication process outlined above.

The assumption from the polarization rotation method that the phase shift induced in the TM mode is 1/3 (due to $3r_{13} = r_{33}$) the shift induced in the TE mode. This assumption is incorrect for this device because:

- 1) The poling field is not enhanced in the regions where the TM mode is localized. As a result, these regions are poled under less electric field than inside the slot.
- 2) The TM mode is not confined in the EO material.
- 3) The modulation field is not enhanced outside of the slot region, where the TM mode is localized.

Due to these conditions, we assume that the TM mode acts a reference arm in the polarization rotation method. This assumption serves to overestimate the V_π (i.e. any modulation of the TM

mode will cause the V_π to be *higher* than reported here). Given the conservative nature of these measurements, it has been determined that the polarization method, albeit not most suited for this waveguide design, will serve as an adequate measurement of drive voltage until an amplitude modulator can be fabricated.

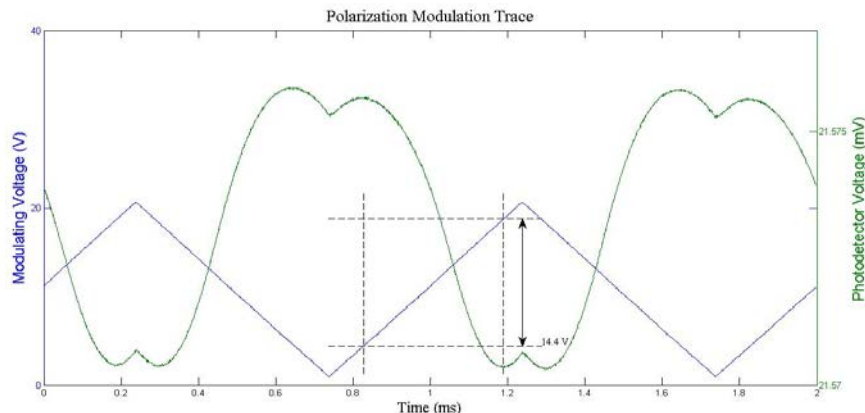


Figure 47. Modulation data for our extraordinary result.

The best result from the poling studies is displayed above, and is currently being reproduced. This measurement indicates a $V_\pi = 14.4$ V when modulated across the ground electrodes of a CPW electrode. Modulating each arm independently in a GSG CPW configuration would half this V_π , = 7.7 V. This translates to a $V_\pi L$ of 0.65 Vcm or 0.324 Vcm if modulated in push-pull (dual drive).

This best result indicates that the material exhibited an EO coefficient of approximately 60 pm/V in the slot waveguide. This device was poled at 300 V, and we expect a roughly 4-fold enhancement of the poling field in the slot (calculated by the multiphysics package in Matlab). The material used in this study typically exhibits a poling efficiency of 1 pm/V per V/ μ m at 1550 nm—as such, we would anticipate an EO coefficient of roughly 75 pm/V. Given these results, we believe we are close to achieving the highest poling efficiencies and EO activities ever reported in a slot waveguide device.

Currently, efforts are underway to increase the length of the interaction region of the device in order to reduce the V_π measured for a device. Balancing the loss penalty for longer slot lengths will be paramount towards this goal. Optical loss is commonly cited as the largest drawback inherent to slot waveguides. In parallel with fabricating devices with increased interaction length, we have explored numerous etch recipes, slot designs and post processing steps to reduce the optical loss incurred in the slot waveguide by reducing the sidewall roughness of the silicon slot claddings. This process is described below. Following optimization of the optical loss and drive voltage, electroplated gold CPW structures with RF probe landings, which have also been developed in parallel efforts, will be integrated into the low drive voltage modulator.

4.9) Vertical Dual-Slot: Reducing Roughness by Oxidation

To achieve low- V_π operation of the modulator, it is necessary for the RF and optical modes to interact as they propagate along the waveguide for as long a section as possible. Ultimately, the interaction length is limited by the losses incurred in both the optical and the RF modes. The bulk of

the optical losses are due to the scattering from random features present on the sidewalls of the waveguide, or sidewall roughness. Minimizing sidewall roughness is particularly important for the surfaces of the slot itself where, by design, the field is the strongest, and therefore scattering contributes the most to the losses. While in lithographically defined sidewalls, the roughness can be as small as 10-20nm, such figures are still significant given that the slot is only about 100 nm wide.

Therefore, we have looked into ways to reduce roughness by post-processing. In particular, we considered oxidation as a way to smooth out the sidewalls. Figure 48 shows a comparison of the same waveguide before and after oxidation. It illustrates an improvement that can be expected by using post-processing oxidation to achieve smoother sidewalls. It should be pointed out that the smoothing is obtained at the cost of dilating the slot and therefore reducing the modulation efficiency since the field enhancement in the wider slot is less pronounced. It remains to be seen if this tradeoff is sufficiently beneficial to the performance of the modulator to justify an additional step in the fabrication process.

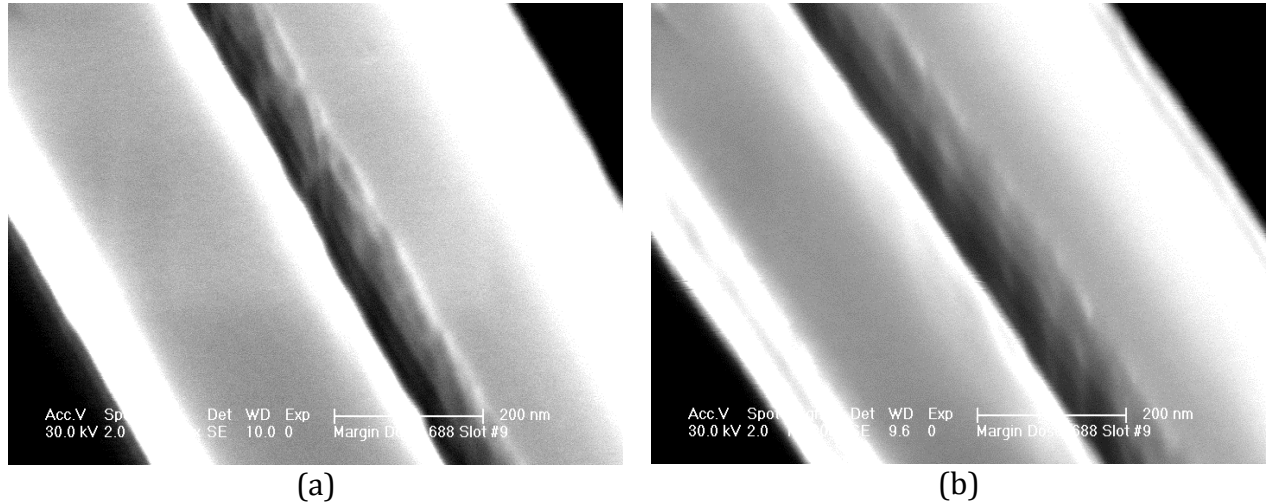


Figure 48. Comparison of sidewall roughness before (a) and after (b) oxidation/removal.

4.10) Vertical Dual-Slot: Electroplating Gold Electrodes for High Frequency Modulation

Important features of the dual slot waveguide modulator are the 50Ω impedance, and low RF losses. These are provided by a coplanar waveguide electrode design that utilizes a ground-signal gap of $6 \mu\text{m}$ and an electrode height of $2.2 \mu\text{m}$. The ratio of the height to the gap is crucial for maintaining a 50Ω impedance. The $2.2 \mu\text{m}$ height minimizes the resistance, and thus RF loss of the electrodes, which maximizes the operating bandwidth. Due to the large height of the electrodes, conventional techniques such as physical vapor deposition are impractical. For this reason electroplating was pursued. SEM micrographs from the first tests of integration of electroplated gold CPW electrodes are shown below.

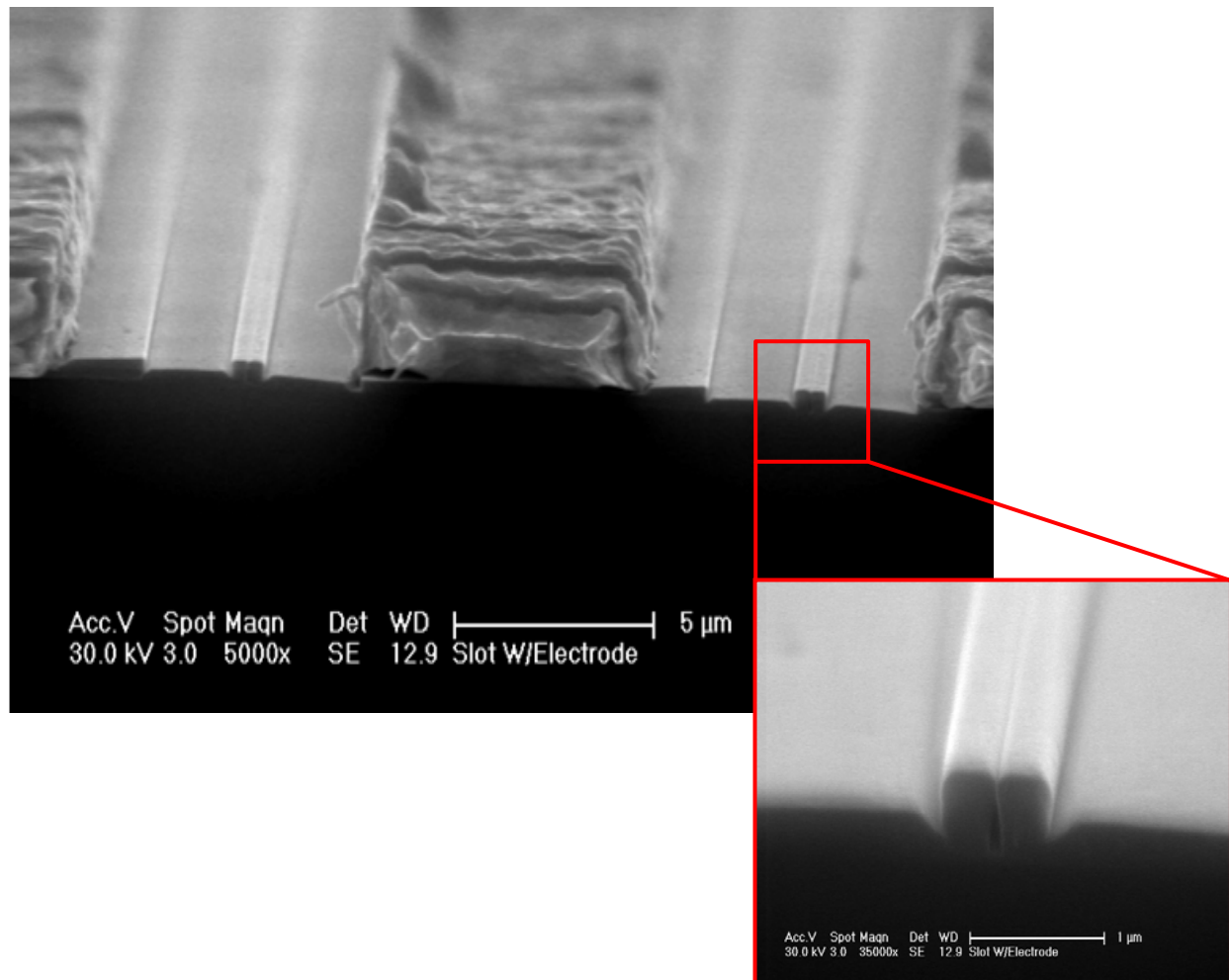


Figure 49. Low loss blanket coated dual slot waveguide with electroplated gold electrodes.

Electroplating requires an aligned resist template on a metal seed layer in order to form the pattern, and calibration of plating speed to avoid surface roughness. Further efforts towards improving the quality of electroplated electrodes have greatly reduced the apparent roughness. Since the electrodes are formed using standard ultraviolet lithography, alignment marks matching those on a CPW photomask were added to the electron beam lithography pattern. This allowed electrodes to be added to multiple waveguide pairs simultaneously, while maintaining the required precision. Figure 39 shows a pair of silicon optical slot waveguides contained within a coplanar waveguide resulting in our proposed push-pull configuration. The distance between the ground and signal electrodes, as well as the TiO_x buffer layer, are designed to minimize optical loss.

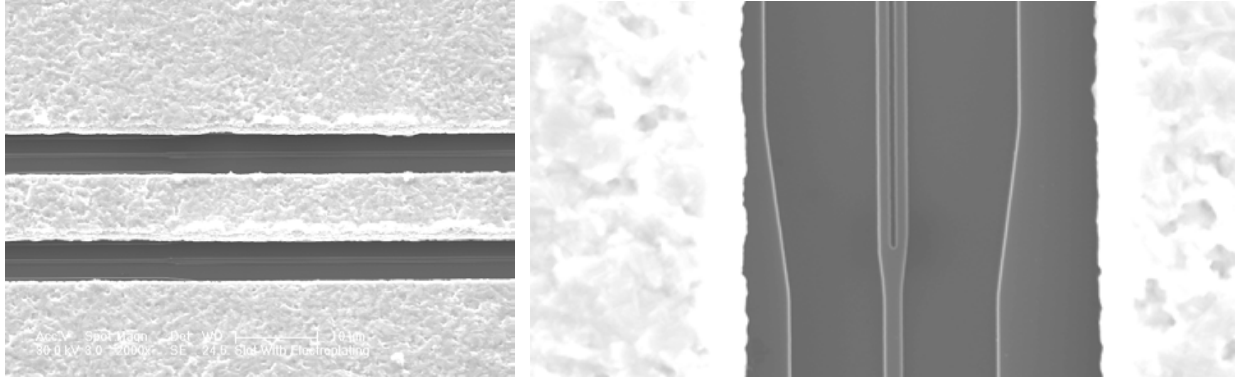


Figure 50. Dual slot waveguide between electroplated ground and signal electrodes (left) with detail of slot coupling region (right)

4.11) Vertical Dual-Slot: CPW Electrode Patterns and RF Probe Launch Integration

Figure 50 shows an aligned and electroplated CPW with an inlay of the launch area for RF testing. This device is ready for poling. The curved design of the CPW allows the optical and RF signal to be launched orthogonally, this eases testing and provides for future integration. The figure also serves to illustrate the correct height of the electrodes as well as the smooth vertical sidewalls. The signal pad of the electrodes, as well as the gap between signal and ground taper outwards towards the launch in order to allow for the use of high speed RF probes which can be connected via coaxial cables to RF measurement equipment such as network analyzers. This will soon allow us to characterize high speed phase and intensity modulation along with RF loss and propagation velocity, which is the major advantage of the dual slot geometry compared to current state of the art silicon-organic modulators.

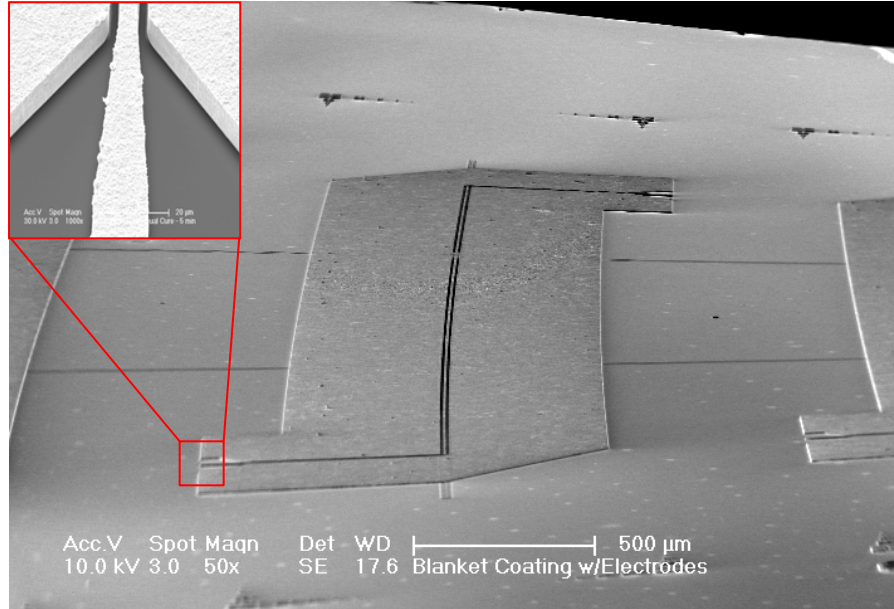


Figure 51. Curved gold CPW with RF launch area inset. The optical waveguides extend through the gold and are visible in front and back of the CPW. The dark marks in the back of the micrograph are alignment marks.

4.12) Vertical Dual-Slot: V-Groove Optical Slot

Whereas we have found solutions to many of the problems we anticipated at the onset of the research project, there still remain significant challenges in realizing the dual-slot modulator concept. Among them is the device yield. The number of steps required to fabricate a modulator is fairly large, and given a finite yield at every step, the overall device yield is thus reduced. Therefore, our focus here is on increasing the yield of individual steps by tightening process control. Another problem is the surface roughness discussed in one of the sections above. The oxidation and oxide removal reduce the surface roughness to some extent, they also lead to the dilation of the slot, which reduces the field enhancement, and compromises the V_{π} . Therefore, we are exploring other options that would produce both smooth sidewalls and field enhancement such as an anisotropic wet etch using potassium hydroxide. The device resulting from this etch has been termed the “V-Groove” optical slot, and is shown in Figure 52.

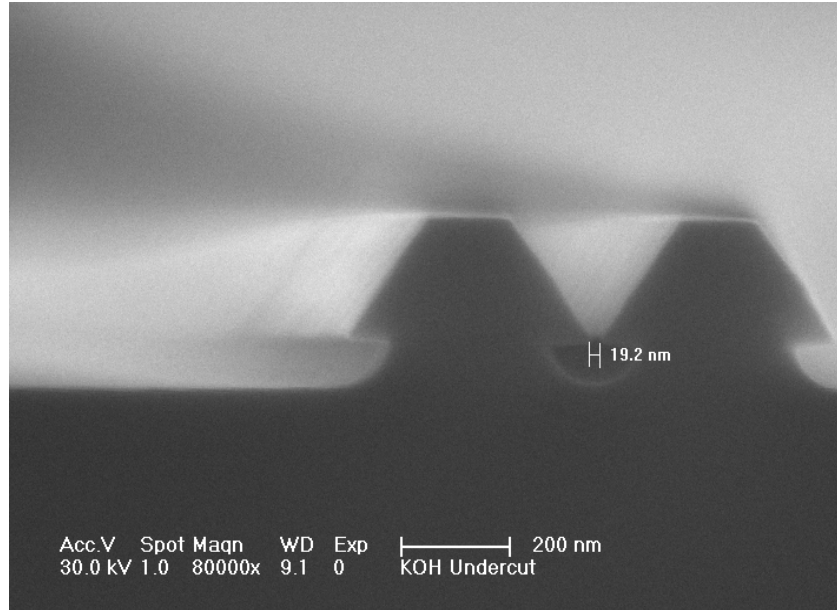


Figure 52. V-groove style optical waveguide.

The V-Groove slot design helps to mitigate several fabrication difficulties involved in the conventional vertical sidewall design. Compared to the previously discussed devices it may ease challenges associated with the TiO_2 liftoff, polymer back filling of the slot waveguide, and optical losses due to sidewall roughness. Furthermore, the design leverages a "lightning rod effect" to concentrate the optical and RF modes to the base of the slot, which could potentially lead to a lower V_π device. A V-groove style optical waveguide is shown in Figure 53. This device features angled sidewalls which are fabricated through the use of potassium hydroxide (KOH) etching. When integrated into the dual slot design this produces an attractive modulator with similar properties to the conventional dual slot design.

As shown, the slot width can be reduced to less than 20 nm because of the KOH etching process, which etches in from the e-beam exposed pattern, rather than straight down. This means we can pattern a slot area of hundreds of nanometers and still see a slot width less than 50nm. The properties of this type of modulator are summarized in the table below (simulated with a very conservative slot width of 100nm and an r_{33} of 100 pm/V).

$V_\pi L$ (V cm, @ DC)	0.414
Z_c (Ohms, @ 100GHz)	43.2
RF Loss (dB/cm, @ 100GHz)	10.91

The $V_\pi L$ of this modulator is slightly larger than that of the conventional dual slot waveguide due to the width of the top portion of the V-groove, however, this design is still attractive due to the possibility for reduced optical loss and the probability of a smaller slot as mentioned. Figure 36 shows how the optical and RF modes are localized to the base of the slot region in this design.

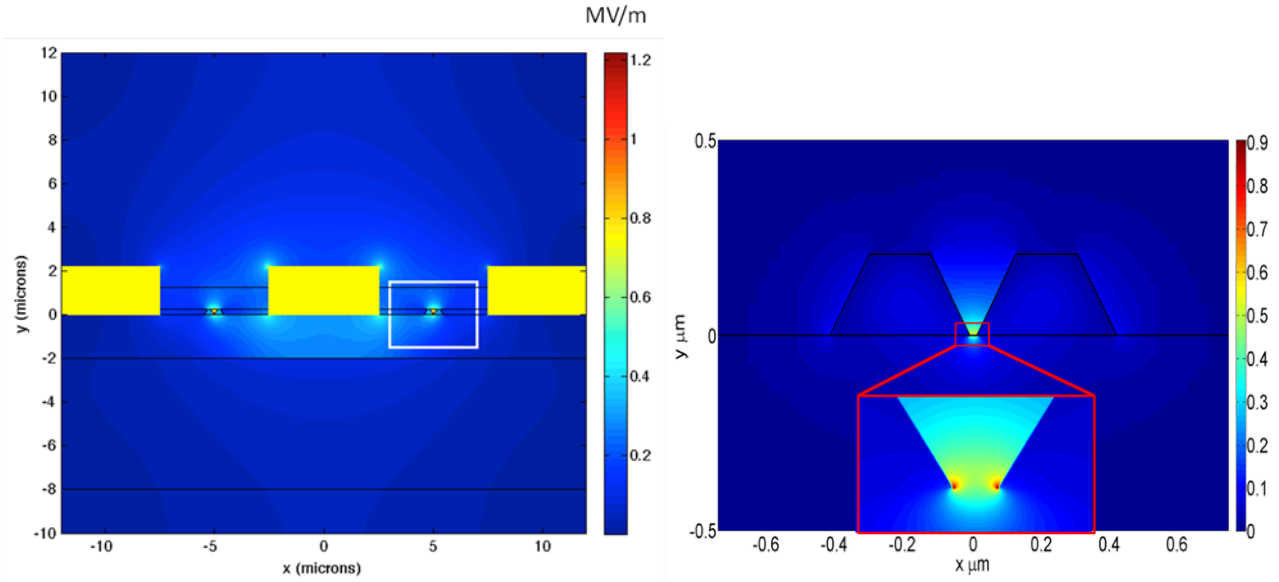


Figure 53: Optical and RF modal patterns for v-groove style dual slot modulator. (left) x-directed electric field at 100 GHz, for 1 V applied potential and (right) x-directed electric field pattern normalized to total electric field intensity at 1550 nm.

The fabrication process for the V-groove style dual slot modulator is shown in Figure 54. The important distinction of this process from that used for the conventional dual slot modulator is the use of KOH etching instead of an iterative dry etch process which results in the scalloping of the slot sidewalls. The selectivity of KOH to the $\langle 100 \rangle$ plane over the $\langle 111 \rangle$ plane results in smooth, low loss, sidewalls at a 54.7° angle to the substrate plane.

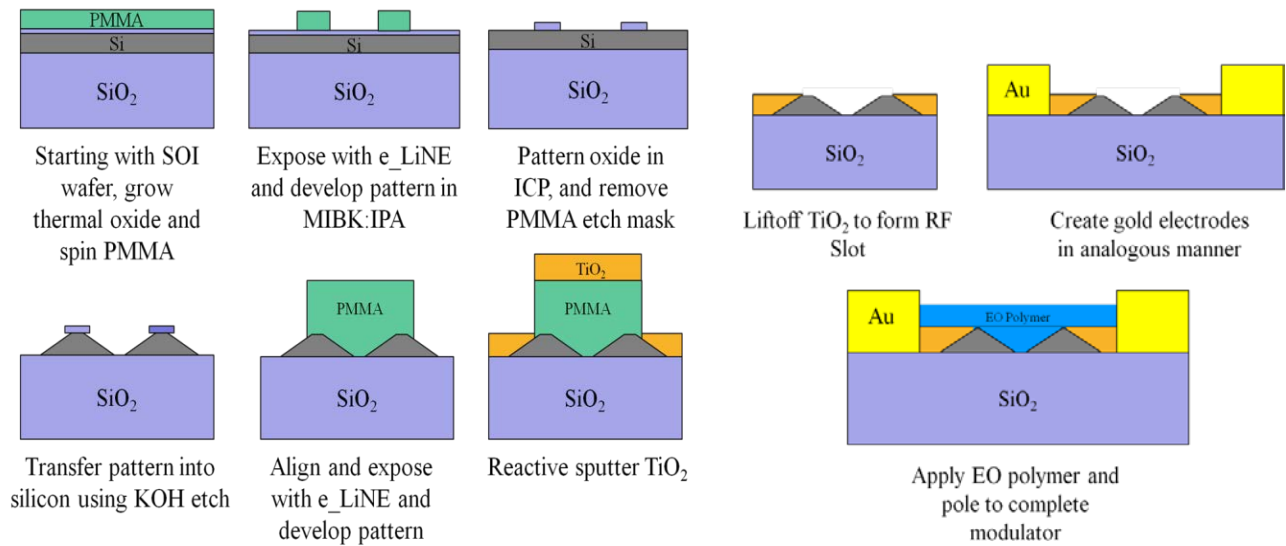


Figure 54. V-groove dual slot modulator fabrication process

5.1) Optical Backplane Switching Fabric

In this task we have explored preliminary designs of reconfigurable photonic processing units. The use of silicon for low loss dielectric waveguides, switches, and modulators has been shown in recent years to provide the same benefits as optical fiber on the chip scale and also to be amenable to current fabrication techniques. Nonetheless, improvements to the current scheme of utilizing high index contrast waveguides for carrying information can be made. Our solution to the growing intrachip communication requirement is to augment the use of dielectric waveguides with active, planar, 2D photonic processing units. In this task, unit cell designs were created to perform basic optical processing functionalities including filtering, switching, and modulation. In this task we have designed and demonstrated the ability to route and reconfigure optical signals through wavelength selective switches. To achieve this goal, we fabricated and characterized an optical backplane switching elements for use in a large-scale optical cross-connect (OXC).

Our solution to the growing intra-chip communication requirement is to augment the use of dielectric waveguides with active, planar, 2D photonic crystal (PhC) devices. In particular, one such device, the slow-light PhC waveguide coupler, can selectively couple light between two output waveguides. Our objective has been to integrate this directional coupler with dielectric waveguides using silicon on insulator (SOI) platform in order to form the basis of an optical communication fabric for on chip communication. Our proposed OXC with integrated PIN actuated PhC switches is shown in Figure 55, where several switch elements are oriented to allow a reconfigurable connection between ports 1-4.

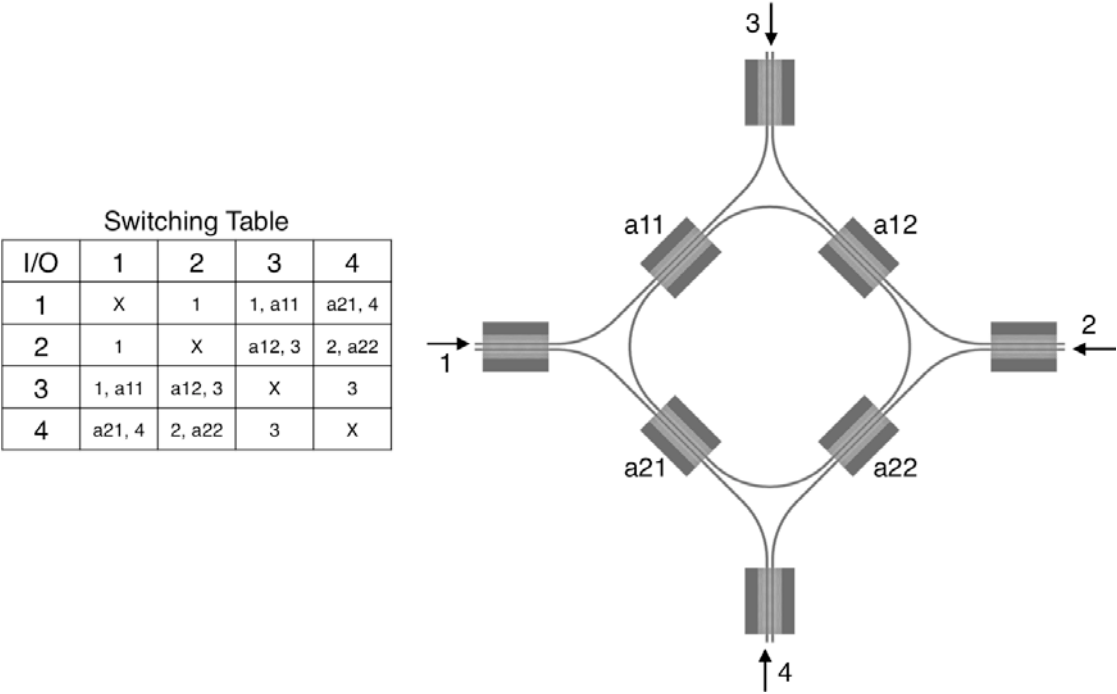


Figure 55. A composed switching table, evaluating the “Honeycomb” node design for optical signals that passively couple to the Bar port within a single CPhCWG element

5.2) Switching Fabric: Engineering Slow Light and Dispersion

In the design of the optical PhC switch element, a triangular lattice patterned in silicon with air cladding is used to establish a photonic bandgap. Silicon is chosen because of its low cost, high availability and its access to fabrication techniques that have been established by CMOS processing and previous telecommunication photonic systems work. To establish a crystal lattice with a desirable photonic bandgap, 2D Plane-Wave Expansion Method (PWEM) of the crystal lattice is employed to interrogate the design space for achieving an adequate bandgap for the switches operation. The 2D PWEM assumes the crystal lattice is infinite in the direction orthogonal to vectors $\mathbf{a}_1$ and $\mathbf{a}_2$, while the structure is periodic in the plane defined by the coplanar lattice vectors $\mathbf{a}_1$ and $\mathbf{a}_2$. Performing PWEM calculations in 2D as apposed to 3D greatly reduced simulation times, allowing for a broad sweep of design parameters for coarse design work. The 2D photonic crystal is created through a periodic dielectric material with a dielectric permittivity of 12.04, simulating silicon at the optical C-Band telecommunication wavelengths. A photonic bandgap for a transverse electric (TE) mode can be formed by the PhC, by designing a structure with a radius to lattice constant ratio (r/a) = 0.3, shown in Figure 56.

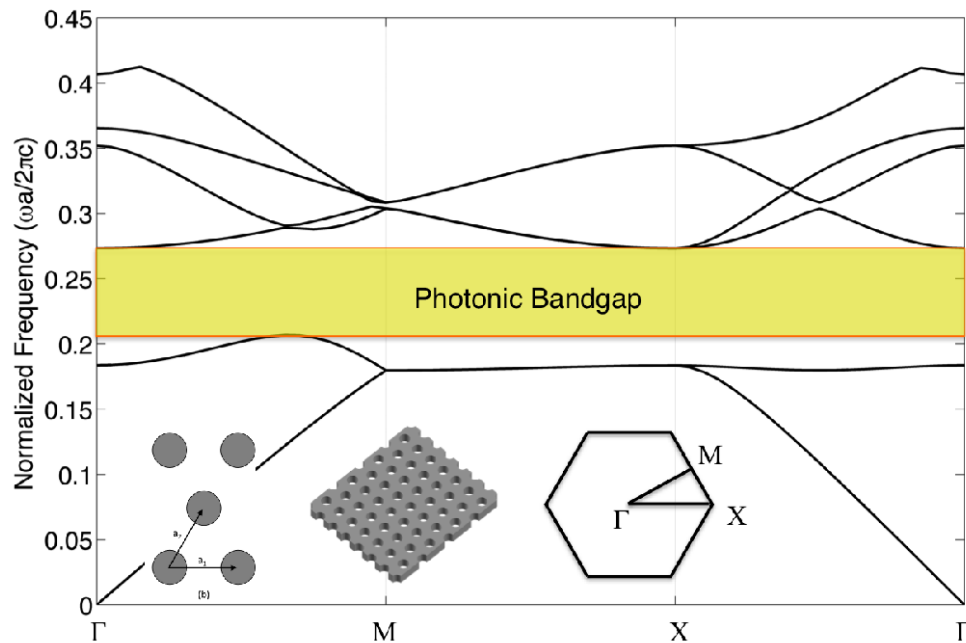


Figure 56. A plot of a photonic bandgap formed within a triangular photonic crystal lattice, solved using a TE mode in 2D PWEM; (subset) Rendering of PhC lattice with reciprocal-space of the lattice outlining the irreducible Brillouin zone

Upon the establishment of the photonic bandgap, an optical waveguide can be made by making a line defect in the crystal structure by the removal of a row of holes. The line defect creates an allowed state of propagation within the PhC with minimal loss, creating the ability to confine and route light within a photonic crystal, analogous with a conventional strip waveguide, thus allowing coupled photonic crystal waveguides for the use of the optical switch within the designed OXC.

Unique to photonic crystal structures, is the ability to tune the propagation constants of the optical signal and engineer a level of slow light into the Coupled Photonic Crystal Waveguide (CPhCWG).

Tuning the dispersion properties is performed through the dilation of three rows of air holes within the PhC, running parallel with the line defect waveguides, shown in Figure 57. The effect of the hole dilation on the band structure of the CPhCWG element is visible by comparison between the even and odd modes of several levels of perturbations. The bands were simulated using 3D PWEM with a normalized background hole size of $r/a = 0.3$, while the dilated holes radius r_2/a was ranged from 0.3 to 0.4125. It is visible from Figure 57, that as r_2/a increases for the three rows of holes, the band resembling the odd mode develops a region in the middle that becomes flat with a smaller slope. This flat region, where the change in k-space is large with small change in the normalized frequency is the regime of slow light. By adjusting the r_2/a parameter, the dispersion band slope of the odd mode can be tuned to achieve the right shape for the appropriate slow light factor. It is also visible that as r_2/a increased to an extreme value of 0.4125, the odd mode breaks down to where more than just an even and odd mode exists for a chosen frequency.

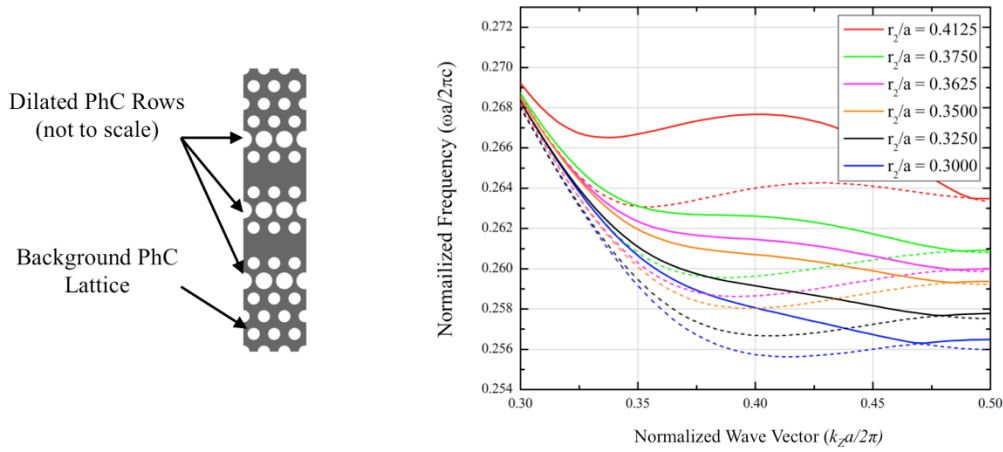


Figure 57. (left) A region of the simulated CPhCWG element with the two line defect waveguides and the bordering dilated rows or air holes; (right) A plot showing the large variance in the dispersion bands as a function of the magnitude of dilation of the three rows of holes

5.3) Switching Fabric: FDTD Simulation of a Single CPhCWG Switch Element

Using the findings discussed above, the r_2/a constant was chosen to be 0.35 to achieve a degree of slow light with group index of $n_g=92$. However, coupling into the slow light photonic crystal cannot be achieved by butting a silicon strip waveguide up to the $r_2/a=0.35$ lattice structure without accruing a -2.2 dB coupling loss through the switch. However, a method to increase coupling into the PhC via the strip waveguides termination with relation to the line defect waveguide termination was used initially, where the waveguide terminated within a PhC hole. To additionally increase the coupling efficiency in and out of the PhC for the wavelengths of operation, the first four and last four lattice sites are adiabatically tapered from $a = 480$ nm to 400 nm, shown in Figure 43. This adiabatic taper increases the coupling efficiency through the CPhCWG elements to only a 0.45 dB loss per element. With the increased coupling efficiency, the resultant spectrum of the CPhCWG is shown in Figure 43. This adiabatic taper increases the coupling efficiency through the CPhCWG elements to only a 0.45 dB loss per element. With the increased coupling efficiency, the resultant spectrum of the CPhCWG is shown in Figure 58.

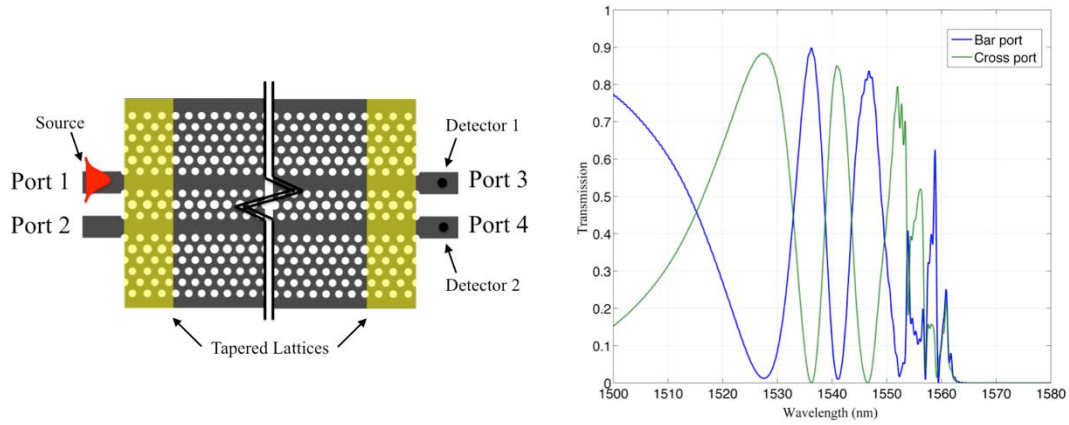


Figure 58. (left) An illustration showing the simulated structure with the first and last four lattice sites adiabatically tapered to increase the coupling efficiency between strip and line defect waveguides; (right) The resultant spectrum of the CPhCWG including the coupling addition, showing a flatter power transmission across the operational wavelengths up to 1550 nm.

5.4) Switching Fabric: Switching Properties and Mechanisms

In the efforts to design and fabricate a wavelength selective filter (WSS), the ability to modulate the state of the photonic switch is what separates the device from many other passive optical elements. With regards to the CPhCWG, making the element function as a tunable WSS is desired for reconfiguration of the coupling states dependent on the propagating signal wavelength for a transparent OXC. The ability to tune the element would allow the active reconfiguration of a switch to selectively launch a signal between the “Bar” state to the “Cross” state, through the method of applying an external stimulus. For the CPhCWG, the modulation is driven by a change in the index of refraction of the silicon that makes up the PhC element. The magnitude of change needed in the silicon’s refractive index was determined through 2D FDTD, through the modification of the effective index of the simulation. It was found that the effective index must be modulated by $\Delta n_{\text{eff}} = -0.009$ in order to fully change the coupling state of the CPhCWG element, shown in Figure 44 by the shifted spectrum from different n_{eff} values. For future reference, the change in n_{eff} approximately correlates with the real change in the refractive index to within 5% thus for further calculations the assumption is made that the change in effective index is approximately the change required within the silicon’s index. Additional function of a splitter can be attained by partially tuning the coupled waveguide structure to shift the transmitted spectrum. The extent of coupling between the guides for this CPhCWG element can be estimated by achieving a 1 nm red shift in the spectral response with a positive effective index shift of approximately 0.00195.

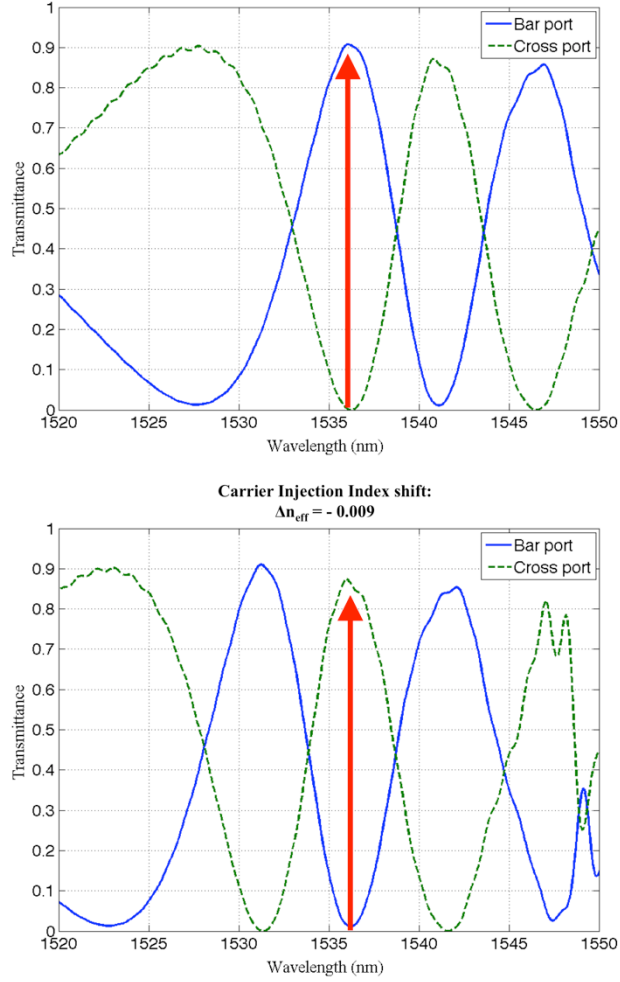


Figure 59. Two transmitted spectrums shown with a relative 0.009 modulation in the effective index to fully change the coupling state of the CPhCWG from (top) “Bar” to (bottom) “Cross”

5.5) Switching Fabric: EO Effect with PIN Diode Free-Carrier Injection

The electro-optic effect achieved through free-carrier injection via a PIN diode allows for fast switching speeds in comparison to conventional thermal tuning. Through the use of the current density equations, if an electrical current is passed through a cross-sectional area, the relation between the current density and the change of injected free-carriers can be calculated. Further, from the free-carrier concentration change, the resultant shift in the refractive index of silicon can be estimated. For the CPhCWG element discussed, requiring an index shift $\Delta n = -0.009$, a current density (J) required to inject the critical amount of free-carriers is $J \sim 2 \times 10^4 \text{ A/cm}^2$.

The mechanism used in this work to modulate the refractive index of silicon, thus changing the coupling state of the CPhCWG, is free-carrier injection via a PIN diode. The PIN diode is designed to span across the CPhCWG element, where the intrinsic region overlays the PhC while the n-type and p-type regions are placed on opposing sides, shown in Figure 60.

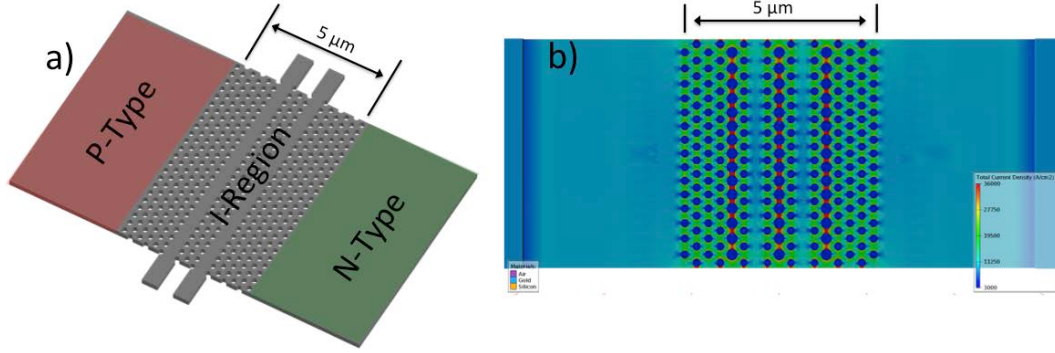


Figure 60. (a) Illustration showing the relative geometry of the PIN diode to the CPhCWG, with the highly doped silicon regions positioned at the extents of the PhC; (b) A preliminary image showing localized regions of increased current densities due to the patterned I-region

The use of the PIN diode allows the placement of the highly doped n-type and p-type regions away from the optical mode, maintaining an intrinsic level of doping when the diode is unbiased, reducing unwanted optical losses that occur in the presence of high impurity concentration. Under forward bias, the PIN diode injects carriers into the I-region of the diode, thereby modulating the index of the silicon and tuning the CPhCWG element to the “On” state, shifting the coupling state of the waveguides. When returning to the “Off” state of the coupler, the PIN diode also has the added benefit of being able to reverse bias the diode, to sweep carriers from the I-region, aiding in the transition between the “On” to Off” state. Preliminary simulations for assessment of the I-V trace with respect to different doping concentrations ranging from 10^{17} to 10^{19} cm^{-3} are chosen due to the ability to achieve the concentrations using conventional fabrication methods, showing a necessary current on the order of 1-2 mA, yielding operational powers of approximately 1-3 mW.

5.6) Switching Fabric: Fabrication and Characterization of CPhCWG with PIN Diode Switching

With the chosen PIN diode geometry, the PIN diodes were fabricated with and without a PhC in the I-region, to measure the PhC’s effect on the PIN diodes’ I-V characteristics, shown in Figure 46. The PIN diodes were fabricated to have an I-region that measured $5 \mu\text{m}$ wide and $16 \mu\text{m}$ in length, shown in Figure 46(c). The PIN diodes were fabricated without the PhC’s, shown in Figure 61(b) and (c), while others were fabricated with a PhC coinciding with the I-region, shown in Figure 61 (d).

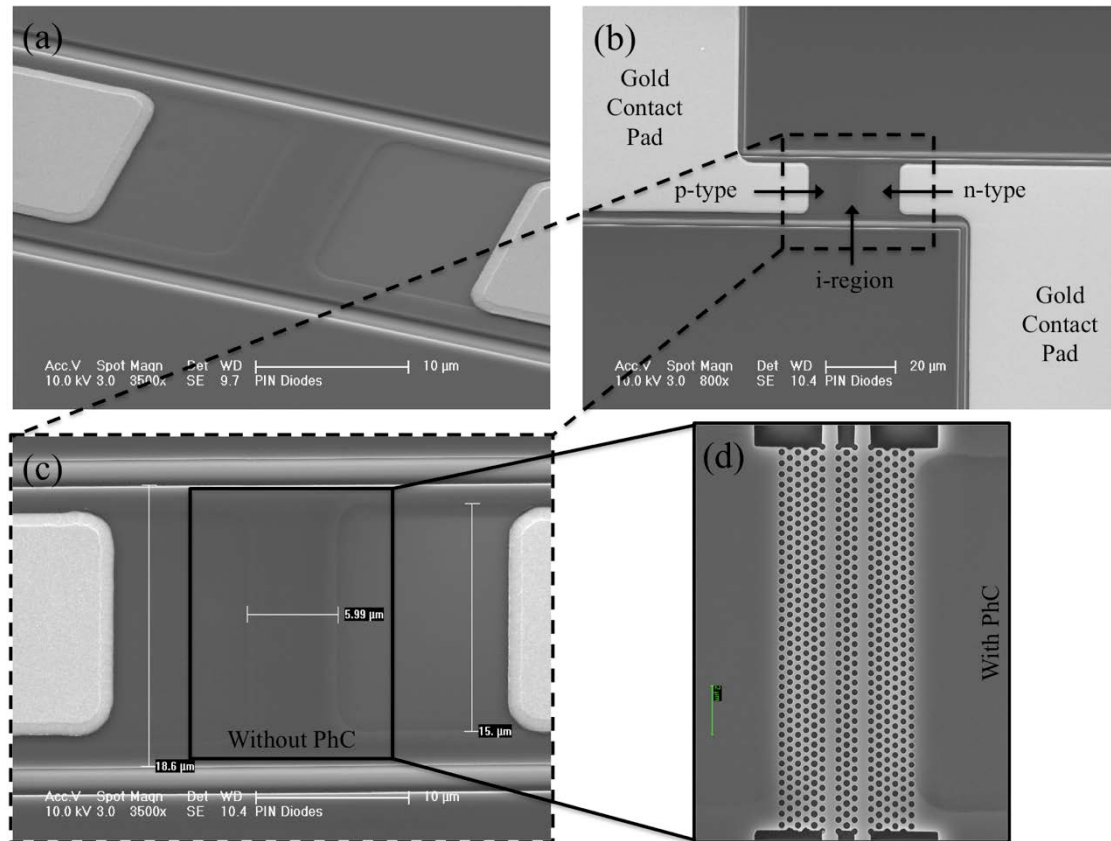


Figure 61. SEM images of fabricated PIN diodes (a) Angled SEM image of diode without PhC; (b) Top view of diode indicating contacts and doped regions; (c) Closer view of callout within (b); (d) SEM image of a diode with PhC in I-region

Similar to the previous testing, the PIN diodes I–V characteristics were measured with and without the integrated PhC by sweeping through a voltage range with a current compliance of 1 mA, shown in Figure 62. As expected, the resultant I–V traces show an increase in the power consumption of the PhC–PIN diode relative to the diode without the PhC due to a higher series resistance from the removal of the silicon due to the PhC. However, despite the increase in power, the operational voltage is still relatively low, at 1.7 V. Also, as fabrication techniques have been optimized, the operational voltage has been reduced to approximately 1.3 V, reducing the difference in performance between diodes with and without the PhC.

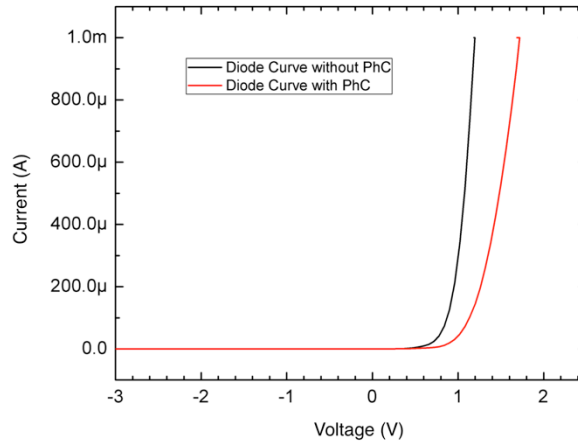


Figure 62. Experimental I–V traces of two PIN diodes that are fabricated with and without the CPhCWG element within the I-region of the diode.

To measure the diodes ability to modulate the current density passing through the CPhCWG element, a resistor was placed in series with the diode, allowing the monitoring of current passing through the circuit by measuring the voltage drop across the resistor, shown in Figure 63.

The diodes were initially tested by biasing the diodes with a square wave that had a low voltage of 0 V and high voltage of 1.3 V, which generated the required current density modulation for switching. However, the measured current contained strong resonances when transitioning between voltages, which cross the “knee” of the I–V characteristic curve, resulting in rise and fall times of 20 ns and 30 ns respectively. Resonances in the electrical drive signals were found to be dominating at frequencies above 5 MHz, and were reduced by operating the diode along the approximate linear region of the I–V curve just above the “knee.” This was accomplished by applying a DC bias across the diode of 1 V, while driving the diode with a square–wave. As a result of operating the diode within the near linear regime of the I–V curve with the DC bias, the voltage modulation needed to achieve the same change in current density is only 0.39 V, shown in Figure 63. The measured current through the circuit with an applied 20 MHz square wave, showed operational speeds with rise and fall times of 8 ns and 5 ns respectively.

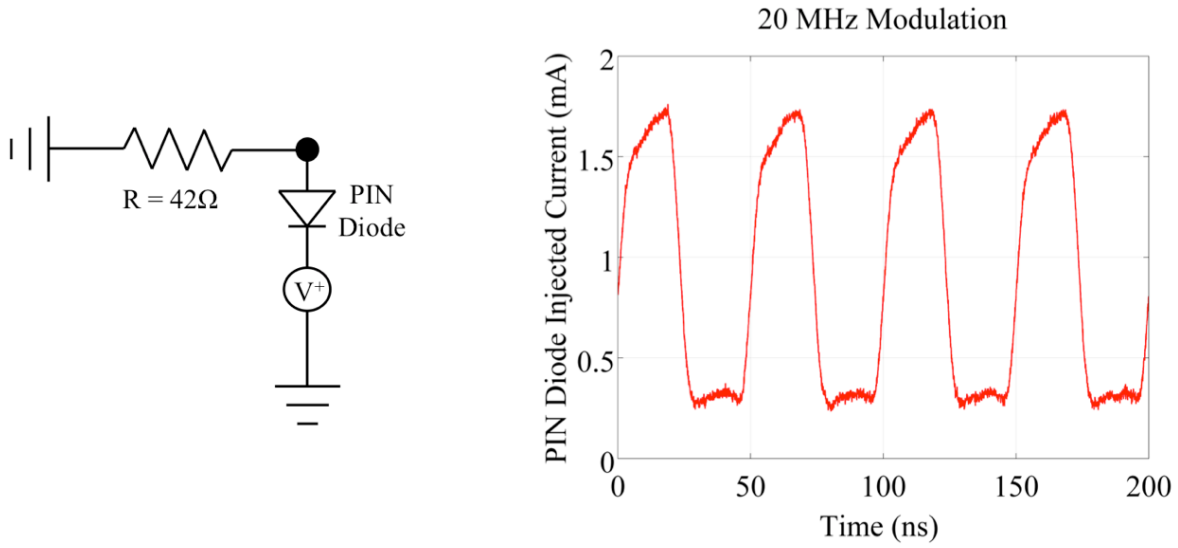


Figure 63. (left) Circuit diagram showing PIN diode placed in series with resistor, using voltage drop across resistor to measure current within circuit; (right) shows measured current modulation with biased 20 MHz square-wave.

5.7) Switching Fabric: Optical Switching with PIN Diode

Once the PIN diode's I–V characteristics were measured with the integrated CPhCWG, the diodes effect on the optical response of the elements were tested while modulating the CPhCWGs' refractive index with the PIN diode. As discussed in Section 5.5, the modulation of the refractive index is designed to modulate the coupling states of the CPhCWG, diverting an optical signal from one port the next. This was achieved by fabricating a set of CPhCWG elements with integrated PIN diodes, including strip waveguides for optical coupling in and out of the photonic element. The device fabricated, shown in Figure 64(left), was characterized first by measuring the passive optical spectrum of the CPhCWG. The collected spectrum from the Bar port, shown in Figure 64(right), is used to determine the wavelength of the optical signal used during the modulation of the element with the diode.

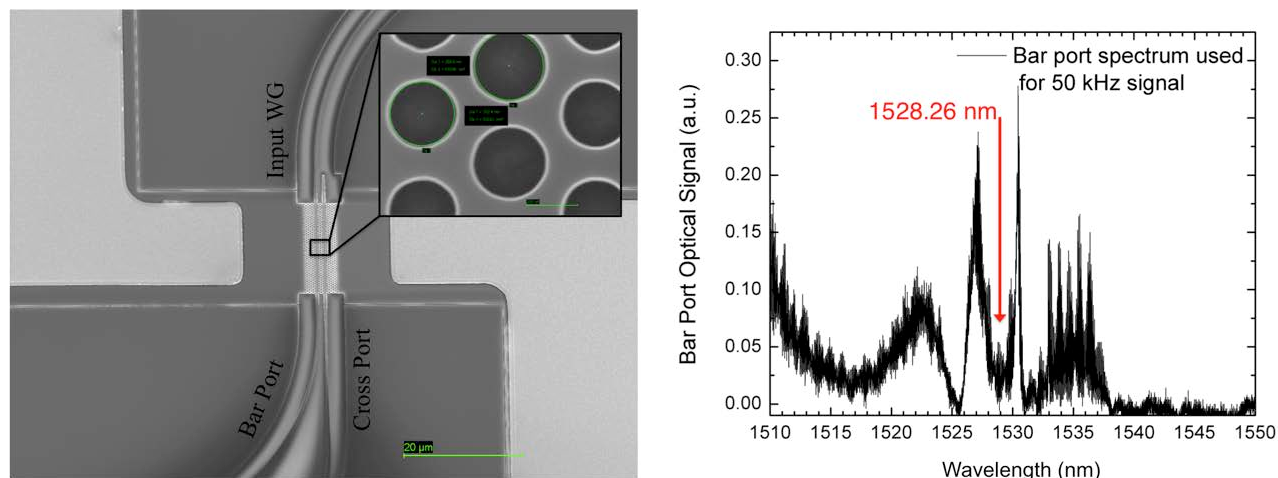


Figure 64. (left) SEM image of fabricated CPhCWG with integrated PIN diode and inset showing magnified view of PhC holes; (right) Experimentally measured optical spectrum, used to identify wavelength used to monitoring active switching.

Through observation of the optical spectrum, the wavelength of 1528.26 was chosen as the probing optical signal for active switching, since the signal passively couples to the Cross port when the PIN diode is in the “Off” state and would couple to the Bar port when the PIN diode is under bias in the “On” state. Thus, by monitoring the optical signal’s intensity at the Bar port, when the CPhCWG transitions from the “Off” to “On” state, the measured intensity will increase when the coupling state changes. This method assures that any increase in signal is due to the modulation of the PhC, as opposed to measuring a decrease in the optical signal, which could be due to a change in alignment or optical absorption.

The CPhCWG was actively tested by probing the gold contact pads with tungsten probes and electrically biasing the PIN diode with a signal generator to switch the optical coupling state. Shown in Figure 65 is the measured modulated optical signal when the switch couples light into the Bar port when turned on, with rise and fall times of 14 ns and 11 ns respectively.

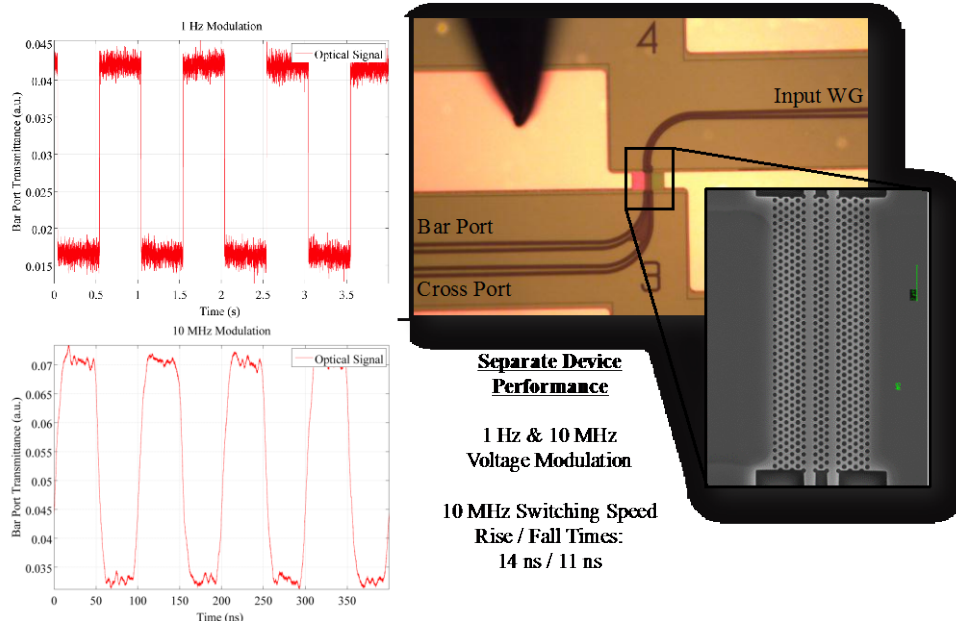


Figure 65. (right) Optical microscope image of PIN diode with CPhCWG element, showing tungsten needle probing gold contact in top left of image; (inset) SEM of CPhCWG within fabricated device; (left) Modulated optical signal at 1 Hz and 10 MHz measured from collecting Bar port signal, showing measured rise and fall times of 14 ns and 11 ns respectively.

In summary, a photonic crystal directional coupler was designed to serve as a tunable photonic switch, which served as a fundamental building block to realize a chip scale OXC. Device size and dispersion were closely considered when refining the optical properties of the CPhCWG element. Methods to tune the CPhCWG element were explored, settling on the use of PIN diodes to induce a refractive index change large enough to modulate the coupling state of the photonic switch. The finalized CPhCWG design was then shown to function as a fundamental element for a transparent OXC when used in architectures such as the “Honeycomb” design. Additionally, the CPhCWG was fabricated and characterized showing reconfiguration of the optical switching state to less than 15 nanoseconds.

Acknowledgments

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Appendix I: References

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Appendix II: Outputs

Journal Publications

1. D.L. Eng, S.T. Kozacik, I.V. Kosilkin, J.P. Wilson, D.D. Ross, S. Shi, L. Dalton, B.C. Olbricht, and D. W. Prather, "Simple Fabrication and Processing of an All-Polymer Electro-Optic Modulator," *J. Sel. Top. Quant. Elec.*, Special Edition on Optical Modulators. *In Press*. (2013).
2. G. J. Schneider, J. Murakowski, C. A. Schuetz, S. Shi, and D.W. Prather, "Radio frequency signal-generation system with over seven octaves of continuous tuning," *Nature Photonics*, 7, 118-122, (2013).
3. T. Baehr-Jones, T. Pinguet, P. L Guo-Qiang, S. Danziger, and D.W. Prather, and M. Hochberg, "Myths and rumors of silicon photonics," *Nature Photonics*, 6, 206-208, (2012).
4. J. Murakowski, G. J. Schneider, and D.W. Prather, "Dynamically induced nonlinearity in a resonant-cavity interferometric modulator," *Optics Express*, 20, 14683-14697, (2012).
5. J. N. Mait, R. D. Martin, C. A. Schuetz, and D.W. Prather "Millimeter wave imaging with engineered point spread functions," *Optical Engineering*, 51, 091606-1- 091606-9, (2012).
6. E. Jacobs, R. Appleby, and D.W. Prather "Special Edition Guest Editorial: Terahertz Millimeter Wave Imaging," *Optical Engineering*, 51, 091601-1- 091601-2, (2012).
7. J. P. Wilson, C. Schuetz, T. Dillon, P. Yao, C. Harrity, and D.W. Prather, "Passive 77 GHz millimeter-wave sensor based on optical upconversion," *Applied Optics*, 51, p 4157-4167, (2012).
8. J. Macario, P. Yao, S. Shi, A. Zablocki, C. Harrity, R. D. Martin, C. A. Schuetz, and D.W. Prather, "Full spectrum millimeter-wave modulation," *Opt. Express* 20, 23623-23629 (2012).
9. J. P. Wilson, C. A. Schuetz, T. E. Dillon, D. L. K. Eng, S. Kozacik, and D.W. Prather, "Display of polarization information for passive millimeter-wave imagery," *Optical Engineering* 51, 091607-1- 091607-8, (2012).
10. J. P. Samluk, C. Schuetz, T. Dillon, R. D. Martin, E. L. Stein, D. Mackrides, J. Wilson, A. Robbins, S. Shi, C. Chen, P. Yao, R. Shireen, J. Macario and D.W. Prather, "Demonstration of Passive W-Band Millimeter Wave Imaging Using Optical Upconversion Detection Methodology with Applications," *Journal of Infrared, Millimeter, and Terahertz Waves*, 33, p 1076-1084, (2012).
11. M. J. Zablocki, A. Sharkawy, O. Ebil, and D. W. Prather, "Nanomembrane transfer process for intricate photonic device applications," *Optics Letters* v 36, p 58-60 (2011).
12. S. Shi, D.W. Prather, "Ultrabroadband Electro-Optic Modulator Based on Hybrid Silicon-Polymer Dual Vertical Slot Waveguide," *Advances in OptoElectronics*, v 2011, p 714895, (2011).
13. M. J. Zablocki, A. Sharkawy, O. Ebil, and D. W. Prather, "Nanomembrane transfer process for intricate photonic device applications" *Optics Letters* 36, 58-60 (2011)
14. S. Shi and D.W. Prather Ultra-broadband electro-optic modulator based on hybrid silicon-polymer dual vertical slot waveguides invited paper for *special issue on optical waveguide and resonator cavities*, *Advances in Opto-Electronics*, 1-6, v 2011(714895) (2010).
15. S. Shi and D. W. Prather, "Dual rf-optical slot waveguide for ultrabroadband modulation with a subvolt V- π " *Applied Physics Letters*, v 96, n 20, #201107 (2010).
16. N. Dutta, P. Yao, A. Sharkawy, G. J. Schneider, S. Shi, and D. W. Prather, "Fabrication of Uniform Large Area Polymer 'Woodpile' Photonic Crystals Structures with Nanometer-Scale

Features” *Journal of Micro/Nanolithography, MEMS, and MOEMS* (JM3), v 9, n 2, 0230003 (2010).

17. N. Dutta, P. Yao, S. Shi, and D. W. Prather, “Fabrication of Large Area 3D ‘Fishnet’ Optical Metamaterial Structures” *Waves in Random and Complex Media* (WRCM), v 20, n 2, p 289-297 (2010).
18. M. Zablocki, A. Sharkawy, O. Ebil, S. Shi, D. W. Prather, “Electro-Optically Switched Compact Coupled Photonic Crystal Waveguides Directional Coupler” *Applied Physics Letters*, 96, 081110 (2010).

Book & book chapters

1. D.W. Prather, S. Shi, A. Sharkawy, and J. Murakowski “Photonic Crystal Technologies: From Theories to Practice”) in the book “Photonic Bandgap Structures: A Novel Technological Platform for Physical, Chemical and Biological Sensing” Bentham Science Publishers (2012)

Selected Peer-Reviewed Conference Proceeding Articles

1. B.C. Olbricht, D.L. Eng, S.T. Kozacik, D.D. Ross, and D. W. Prather, “Processing of Organic Electro-Optic Materials: Solution-Phase Assisted Reorientation of Chromophores,” *Proceedings of SPIE - The International Society for Optical Engineering*, v 8622, *Organic Photonic Materials and Devices XV*, (2013).
2. D.L. Eng, S.T. Kozacik, B.C. Olbricht, S. Shi and D. W. Prather, “All-Polymer Modulator for High Frequency Low Drive Voltage Applications,” *Proceedings of SPIE - The International Society for Optical Engineering*, v 8622, *Organic Photonic Materials and Devices XV*, (2013).
3. S.T. Kozacik , M. Murakowski , M. Konkol , S. Addya , D. L. K. Eng , B. C. Olbricht , M. J. Zablocki , A. Sharkawy , J. Murakowski , S. Shi , Dennis W. Prather, “Progress towards dual vertical slot modulator for millimeter wave photonics.” *Proceedings of SPIE - The International Society for Optical Engineering*, v 8624, *Terahertz, RF, Millimeter, and Submillimeter-Wave Technology and Applications VI*, (2013).
4. Y. Zhang, J. Bai, S. Shi, and D.W. Prather “Ka-band patch antenna array,” *Antennas and Propagation Society International Symposium*, p 1-2, (2012),
5. J. Bai, S. Shi, D.W. Prather, and R. Nelson “Wideband, electrically-small, planar, coupled subwavelength resonator antenna with an embedded matching network” *Antennas and Propagation Society International Symposium (APSURSI)*, p 1-2, (2012).
6. D.W. Grund, G. J. Schneider, G. A. Ejzak, J. Murakowski, and D.W. Prather “Toward an integrated silicon-photonic module for widely tunable narrow-line RF source using injection-locking ” *GROUP IV Photonics (GFP)*, p 213-215, (2012),
7. M. J. Zablocki, M. Roman, D.W. Prather and A. Sharkawy” Photonic Crystal WDM cross connect with reconfigurable OCDMA functionality” *2012 IEEE Avionics, Fiber- Optics and Photonics Technology Conference*, p 18-19, (2012).
8. J. P. Wilson, C. A. Schuetz, T. E. Dillon, P. Yao, E. D. Martin, D.W. Prather, “Polarization sensitive millimeter-wave imaging sensor based on optical up-conversion scaled to a distributed aperture” *Infrared, Millimeter and Terahertz Waves (IRMMW-THz)*, (2012).

9. B. C. Olbricht, S. Kozacik, D. Eng, M. Roman, D.W. Prather, "Solution phase-assisted reorientation of chromophores." In *Organic Photonic Materials and Devices XIV*; Tabor, C.; Kajzar, F.; Kaino, T.; Koike, Y., Eds.; SPIE, 2012; Vol. 8258, p. 82580T.
10. B. C. Olbricht, S. Kozacik, D. Eng, M. Zablocki, M. Murakowski, S. Shi, D. W. Prather, "Hybrid Organic-Silicon Dual RF-Optical Nanoslot Waveguide" *2011 8th IEEE International Conference on Group IV Photonics (GFP)*, p65-67.
11. D. Eng, S. Kozacik, B. C. Olbricht, S. Shi, D. W. Prather, "Broadband low-drive voltage polymer electro-optic modulator." In *RF and Millimeter-Wave Photonics II*; Nelson, R. L.; Prather, D. W.; Schuetz, C.; Schneider, G. J., Eds.; SPIE, 2012; Vol. 8259, p. 82590C.
12. S. T. Kozacik, D. L. K. Eng, M. J. Zablocki, M. Roman, A. Sharkawy, J. Murakowski, B. C. Olbricht, S. Shi, D. W. Prather, "Dual vertical slot modulator for millimeter wave photonics." In *RF and Millimeter-Wave Photonics II*; Nelson, R. L.; Prather, D. W.; Schuetz, C.; Schneider, G. J., Eds.; SPIE, 2012; Vol. 8259, p. 82590D.
13. B. C. Olbricht, S. Kozacik, D. Eng, M. Zablocki, M. Murakowski, S. Shi, D. W. Prather, "Hybrid Organic-Silicon Dual RF-Optical Nanoslot Waveguide" *8th Inter. Conference on Group-IV Photonics* (IEEE, London, 2011).
14. D. W. Grund, Jr., B. C. Olbricht and D. W. Prather, "Quantum dot composite light sources" *Proc. SPIE* 7953, 795302 (2011); doi:10.1117/12.875227
15. A. Sharkawy, O. Ebil, M. Zablocki, S. Shi, and D. W. Prather, "Chip-scale photonic interconnects for reconfigurable computing" *Proc. SPIE* 7609, 76090O (2010).
16. A. Sharkawy, O. Ebil, P. Yao, E. Kelmelis, M. Zablocki, S. Shi, C. A. Schuetz, and D. W. Prather, "Organically enabled silicon-based photonic/RF-photonic applications" *Proc. SPIE* 7599, 75990L (2010).

Provisional Patents:

1. *Simple Fabrication Process of all Polymer Electro Optic (EO) Modulator Implementing UV15 as Bottom and Top Cladding Layers With a Simple Cryo-Cleaving End Facet Preparation Technique.* D.L.K. Eng, B.C. Olbricht, D.W. Prather. USPTO Application Number 61760673.
2. *Process for Solution Phase-Assisted Reorientation of Chromophores.* B. C. Olbricht and D. W. Prather . Provisional Patent filed with the US Patent and Trademark Office, Feb. 14, 2011.

Appendix III: Data

Effort: Solution Phase-Assisted Reorientation of Chromophores

EO activity, unpoled films	< 3pm/V maximum @1310nm
EO activity, conventionally poled films	170 pm/V maximum @1310nm
EO activity, SPARC films repoled	220 pm/V maximum @1310nm
EO activity, SPARC films without TEEFP	75pm/V maximum @1310nm
SPARC Poling Voltages	10,000VDC

Effort: All-Polymer Waveguide Modulator

Interaction Length	1.6 cm patterned
V_{π} incorporating IKD-1-50	2.2 V, minimum
Optical Loss Value, IKD-1-50	16 dB, minimum
In Device r_{33} , IKD-1-50	105 pm/V, maximum @ 1550nm
V_{π} incorporating SEO250	1.7 V, minimum
In Device r_{33} , IKD-1-50	107 pm/V, maximum @ 1550nm
Optical Loss Value, SEO250	12.8 dB, minimum
s_{12} , High Frequency Test Device	-2 dB, minimum, simulated

Effort: Dual-Slot Modulator, Vertical Configuration

Slot Width	120 nm, typical
Slot Transition with Break Throughput, Optical	82%, simulated
Minimum Break Thickness Achieved	88 nm
Interaction Length	0.9 mm patterned
V_{π}	14.4V minimum
Optical Loss	30 dB minimum
In Device r_{33} , IKD-1-50	60 pm/V, maximum @ 1550nm

Effort: Optical Backplane Switching Fabric

PIN Diode Actuation Voltage	1.3 V
Diode Rise Time	8 ns
Diode Fall Time	5 ns
Optical Switch Time	< 15 ns