
# PROCESS DEVELOPMENT FOR THE FABRICATION OF SPHEROIDAL MICRODEVICE PACKAGES UTILIZING MEMS TECHNOLOGIES

THESIS

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## Abstract

Sub-$mm^3$ spherical microrobots are being researched as a path towards reconfigurable wireless networks and programmable matter. The microrobot design requires a spheroidal microdevice package compatible with solar energy collection, wireless sensing, and electrostatic actuation mechanisms to be developed. Throughout this research, a variety of MEMS fabrication techniques were evaluated with regards to their applicability to the packaging process. $SF_6$-based plasma was determined to be a preferable alternative to wet HNA etching when producing repeatable bulk isotropic etches in silicon. The effect of silicon crystal orientation on etch variance and anisotropy was also investigated. HNA polishing was demonstrated as an effective method of reducing undercutting, surface roughness, and anisotropy. MatLab image processing routines were developed and incorporated into etch analysis, providing an efficient method of data collection. A method of performing sophisticated wafer alignment and photolithography processes by leveraging existing cleanroom devices was proposed. This research established a path forward for an advanced packaging scheme designed to move microelectronics packages away from the planar circuit board configurations of the past and into the autonomous architectures of the future. The proposed design is applicable to a wide variety of microelectronics applications while meeting the requirements of the sub-$mm^3$ spherical microrobot system.

*To Mom and Dad, for always encouraging me to explore…*

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PROCESS DEVELOPMENT FOR THE FABRICATION OF SPHEROIDAL MICRODEVICE PACKAGES UTILIZING MEMS TECHNOLOGIES

# I. Introduction

## Background

Research into the field of micro-robotics may have initially been inspired by Professor Feynman's famous "There's Plenty of Room at the Bottom" speech in 1959 [1], but recent advances in MEMS (microelectromechanical systems) technologies have enabled micro-robotics to become viable for the modern world. In general, micro-robots are much more simplified than their large scale counterparts, with most possessing only limited actuation and sensing capabilities. However, due to their small size (usually on the mm scale), micro-robots can be produced in large numbers at low cost, making them attractive for swarm robotics applications, where their simplicity is seen as a benefit rather than a hindrance. Another potential application of micro-robots lies in reconfigurable matter. The term "reconfigurable matter" may bring to mind images of the T1000 from the Terminator movie series, but serious research has been devoted to the topic in the last 10-15 years. Despite the mounting interest in the fields of microrobotics, nanorobotics, and programmable matter, attempts at manufacturing viable hardware components have been woefully outnumbered by theoretical proposals for new applications.

In response to this need for innovative device fabrication solutions, researchers at AFRL's Sensors Directorate have demonstrated a sub-$mm^3$ spherical robotic structure, into which they planned to integrate energy collection, energy storage, computation,

sensing, and actuation [2, 3]. Although the initial AFRL robot design eventually presented a few insurmountable challenges, there have been ongoing attempts to develop a more feasible fabrication strategy while still maintaining the general size and shape constraints as well as the use of wafer-level micromachining. The many novel aspects of this design, including its spherical shape, CMOS compatibility, and electrostatic actuation allow for a variety of potential applications such as swarm robotics and reconfigurable matter to be explored. The research effort described herein will focus on exploring the viability of combining bulk micromachining methods such as deep isotropic etching with common surface micromachining methods such as projection photolithography, thin film deposition, and sacrificial layer etching to produce nearly perfect spheres for use in a new spherical micro-robot structure. Similar processes have been used in attempts to fabricate hemispherical gyroscopes and inertial confinement fusion targets; however, this research effort represents an innovative approach to microrobotics and microdevice packaging in general. The aim of this introductory chapter is to further clarify the research problem by offering justification for this study, defining the scope of the problem, briefly introducing the methodology, materials, and equipment to be employed, and the standards for success.

**Justification**

The aforementioned microrobot design is a joint effort between AFIT, AFRL and a team at the University of Michigan. Currently AFRL is primarily responsible for developing the structural component of the design, while the researchers at the University of Michigan are focused on miniaturizing the logic, power, and communications systems.

This research project will be conducted with the aim of developing a viable process for the fabrication of a spheroidal microdevice package which meets the needs of the proposed microrobot design. The current design of the spherical microrobot system requires precise integration of many microscopic components; therefore, successful completion of this effort will represent significant progress in producing functional microrobots. These novel microrobots have a broad range of potential applications valuable to the Air Force and the civilian world, including 4-D modeling, wireless sensing, distributed networking, energy harvesting, and micro-locomotion.

**Scope**

Successful completion of this project will depend on targeting specific problems faced in the fabrication process and developing techniques to overcome these challenges. While the spherical structure is just a subsystem of the larger microrobot, at this point the advances being made on other parts of the project are of little concern to this research effort. Therefore, size, shape, and material restrictions will be taken into account; however, specific details involving the integration of the "brains" of the robot into the packaging structure will not be addressed. This restriction is enforced primarily to obtain a proper scope to the project, but is also a result of the power and logic components simply not being much further along in development at this point. Additionally, all processes will be limited to those which are capable of being performed in the AFIT and AFRL cleanroom facilities. Finally, this research will be done solely as a feasibility study; that is, I will not seek to develop and compare multiple methods of fabrication.

## Methodology

The first experimental component of the research effort will involve the fabrication of near-perfectly hemispherical cavities in silicon wafers. Therefore, the first question to be addressed is what masking materials and etchants, and etch parameters are necessary to conduct a precise and repeatable isotropic etch on silicon. In addition to performing the etches, appropriate measurement and characterization techniques must be selected or developed to obtain valuable data from the etch results. After completing the large scale isotropic etch study, the hemispherical cavities must be prepared for patterning and deposition processes. Methods for refining the etch cavities to meet desired parameters will be explored, with experimental results tracked using many of the same techniques from the isotropic etch study. Processes for performing three-dimensional photolithography processes will also be investigated, using conventional spin-coating methods as well as newer photoresist deposition technologies. After the development of appropriate etching, surface preparation, and photolithography methods, the research focus will shift towards the development of an integrated process for microdevice package fabrication. Experimental results from the etching, surface preparation, and photolithography studies will be utilized in conjunction with known thin film deposition, sacrificial layer etching, and packaging techniques to develop a process for fabricating spheroidal microdevice packages.

## Materials and Equipment

A wide array of tools and equipment is available in both the AFIT and AFRL cleanrooms. Chrome masks can be laser-written in the AFIT cleanroom, allowing for

quick changes to photolithographic processes. In addition, a wide array of photoresists and acids are available, and the Trion® RIE system can be programmed for numerous chemical vapor etch recipes. Silicon dioxide can be grown at AFIT or AFRL, and AFRL offers Low Pressure Chemical Vapor Deposition (LPCVD) of materials such as silicon nitride. Additionally, AFRL and AFIT co-own a Deep Silicon Etching (DSE) tool which can perform more complex etch processes than AFIT's Trion® RIE system. Metal sputtering or evaporation can be performed at AFIT. The backside-alignment machine in the AFRL cleanroom may also be the only way of reliably aligning the two wafers for bonding the hemispheres, although other novel methods are likely to be explored as well. 1000 μm-thick <111>-oriented silicon wafers will be purchased to supplement AFIT's current supply of <100>-oriented, 525 μm-thick silicon wafers. Novel photoresists designed for 3D photolithography may also be purchased if required.

**Summary**

The recent advancements in MEMS technology and the ever-shrinking size of electronics in the modern world have spawned a number of innovative research efforts within the burgeoning field of microrobotics. One such effort is the development of a sub-$mm^3$ spherical micro-robot with integrated energy collection, energy storage, computation, sensing, and actuation by a team of researchers at AFIT, AFRL, and the University of Michigan. As part of AFIT's contribution, this research effort will focus on developing innovative fabrication methods for the production of spheroidal microdevice packages. Ultimately, these packages are envisioned as being applicable to not only the proposed spherical microrobot, but to a wide array of emerging research fields, such as bioMEMS,

wireless sensing, distributed networking, and programmable matter, among others. Subsequent chapters will detail MEMS packaging techniques and previous fabrication efforts found in relevant background literature, the methodology for experimental design and testing, results and analysis of the experimental data, and provide recommendations for continued research.

# II. Literature Review

## Chapter Overview

This research effort investigates a novel method of microdevice packaging which is envisioned as a particularly viable path towards miniaturization and autonomy. The exploration of microrobotics and, more specifically, programmable matter, provides the motive for targeting the fabrication of a spheroidal package. In order to obtain a better understanding of my research path, it is necessary to explore the previous research and current state of technology in programmable matter, microrobotics, microfabrication, and microdevice packaging. This is accomplished through an extensive review of the journal articles, research studies, books, and other scholarly documents related to the aforementioned areas. As a first measure, I will discuss notable previous attempts at both programmable matter systems and microrobotic systems in order to provide perspective on how this project relates to previous and ongoing work in the field. Next, I will introduce the reader to the world of MEMS, which encompasses most of the processes and practices discussed hereafter. Finally, I will explore appropriate theory and experimental results which will serve as a guide for the microfabrication efforts which will be detailed extensively in Chapters 3 and 4. As a whole, this chapter informs the reader of the theory and previous research relevant to this effort, as this will serve as the foundation for decision making throughout this thesis.

**Previous AFRL Research**

This research stems from previous efforts at the Air Force Research Laboratories to create sub-$mm^3$ autonomous robot systems using MEMS technologies [2, 3]. The previously envisioned microrobots, shown in Figure 1, consist of a spherical shell with integrated energy collection, energy storage, computation, sensing, and actuation capabilities. Fabricating the spherical shell from silicon (Si), silicon dioxide ($SiO_2$), or a combination of both is a stated goal, as these materials are compatible with many common fabrication methods and allow for future integration of complementary metal-oxide-semiconductor (CMOS) circuitry within the shell itself [2]. The proposed design calls for a shell thickness of approximately 0.5-2.5 μm. The shell would contain conductive polysilicon electrodes necessary for the robot's movement, as well as the transistors and circuitry needed to control the voltage applied to the plates. The structure will also need to include an arm or support of some kind for a circuit region which would house the robot's logic and support the capacitor and solar cell [2].

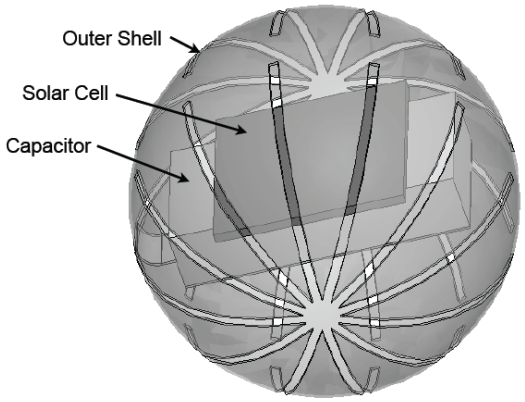


**Figure 1. Artistic rendering of spherical micro-robot design from previous AFRL research [2].**

Electrostatic actuation can be accomplished via a series of electrodes embedded in the shell. By biasing the electrodes relative to their neighbors, it is possible to create an attractive force on a conducting surface, which can be modeled as a series of capacitors over a conducting plate, as illustrated in Figure 2.

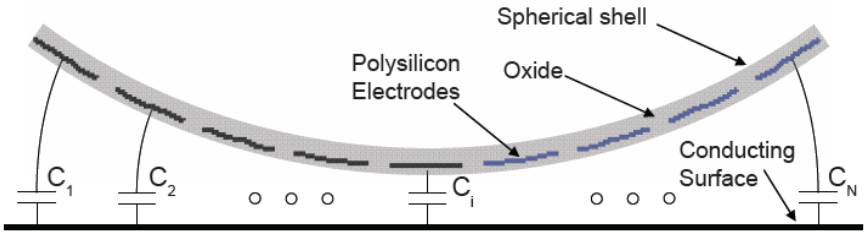


**Figure 2. Schematic representation of electrostatic microrobot actuation mechanism [2].**

The initially proposed fabrication technique relied on the residual stresses present in wafers of silicon-on-insulator material [2]. All device fabrication is accomplished using planar processes, after which the device and oxide layers are released from the silicon handle wafer. Upon release, the 2D shapes curl into a sphere thanks to the high residual stresses found in the thermally grown $SiO_2$ layers. A detailed explanation of the so-called “black wax” method of fabrication is provided in Figure 3.

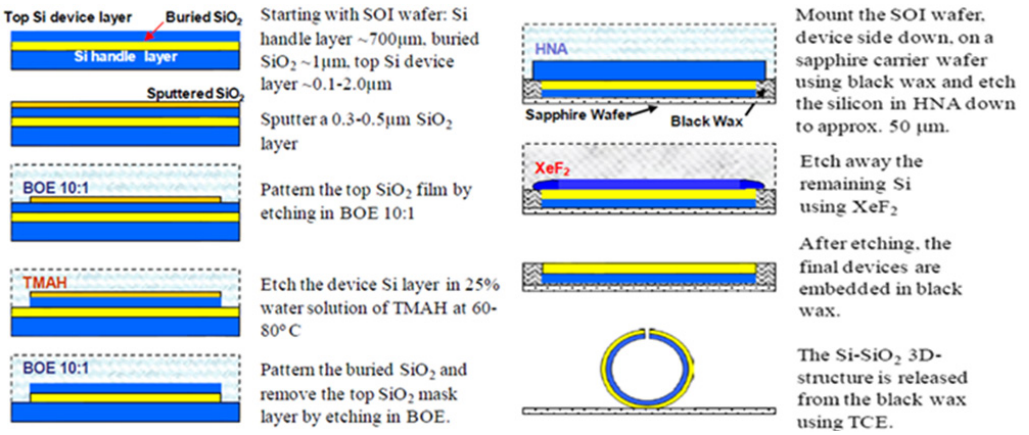


**Figure 3. Black wax method for patterning SOI device layers and releasing Si-$SiO_2$ spherical shells as described by AFRL [3].**

However, to create a spherical structure from a 2-D shape, bending ideally needs to occur on two axes. Unfortunately, once bending begins along one axis, a beam becomes much more resistant to bending along its other axis. Therefore, AFRL's best solution to date has been patterning ribbons, petals, or ridged ribbons which radiate from a central point, as shown in Figure 4.

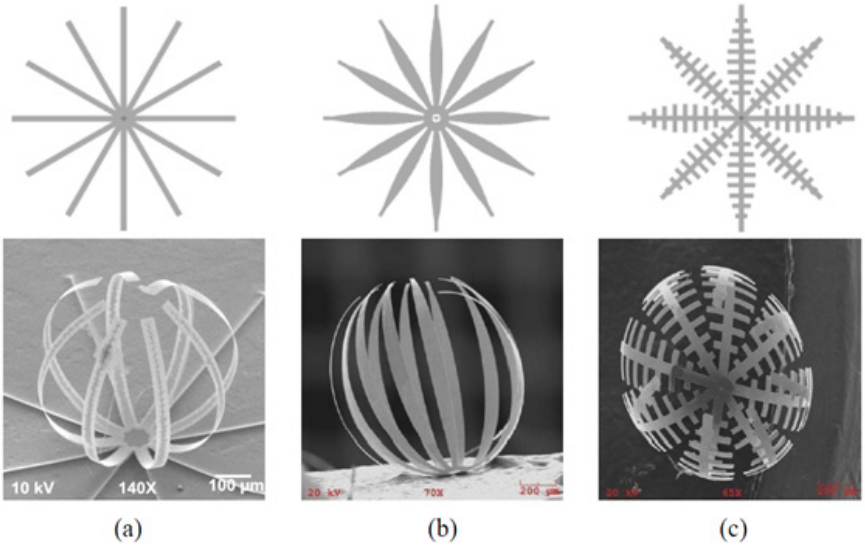


**Figure 4. Planar layouts and SEM images of released (a) ribbon (b) petal and (c) ridged ribbon designs from AFRL [3].**

AFRL matured the black wax process to a point at which it yields >50% of the devices per substrate, and has taken measurements of two-layer spheres with device layers from 0.55 μm to 1.3 μm to verify the bending model. Experimental shells were found to have diameters between 0.6 mm and 3.5 mm, with the results matching a theoretical bending model with reasonable accuracy [3].

Despite these successes, the fabricated shells were found to be lacking in a number of areas. First, a step to mount logic and power systems could not be successfully integrated into the fabrication process without disrupting the residual stress bending. Secondly, the surface area of the finished shells represents well below 50% of the surface area of the enclosed spherical volume. Increased surface area allows for better actuation characteristics, the integration of advanced devices into the shell itself, and improved stiffness and survivability. Finally, the method does not provide a hermetic or even enclosed environment for the protection of enclosed microdevices. Therefore, the spherical shell discussed throughout this document is being developed with the intent of addressing these shortcomings and providing an improved microdevice packaging solution which can be applied to microrobotics, remote sensing, and programmable matter.

**Programmable Matter**

The AFRL effort to create autonomous micro-robots can be more broadly characterized as an attempt to advance the state of programmable matter research. Materials capable of changing their shapes or other physical properties have existed in science fiction under various names for decades, with prominent examples such as the

T1000 from James Cameron's Terminator series and the Replicators from the Stargate universe [4]. However, the term *programmable matter* was first used by Toffoli and Margolus, who envisioned an "indefinitely-extended mesh architecture" which could be realized through the use of hardware or virtual simulation to compute a "fine-grained simulation of physical systems." [5]. While Toffoli and Margolus's work centered on computational logic and the software component of programmable matter, other researchers have made attempts to synthesize physical programmable material. Silicon-based quantum dots [6], nanotechnology [7], synthetic biology [8], and metamaterials [9] have all been proposed as possible approaches to synthesizing material with programmable properties. In particular, nanotechnology has spawned many proposals for intelligent materials made up of millions of tiny robots, such as the "utility fog" theorized by Dr. J. Storrs Hall in 1993 and shown in Figure 5 [10]. Unfortunately, both science fiction and theoretical proposals outpace actual scientific breakthroughs and fabrication capabilities; therefore, despite twenty-plus years of research, no group or individual has claimed to successfully create programmable matter.

**Figure 5. Artistic rendering of 100 micron diameter "utility fog" robot [10].**

### *Self-Reconfigurable Modular Robotics*

A self-reconfigurable modular robot is an autonomous kinematic machine which, in addition to actuation, sensing, and control, displays the capability to change its own shape by rearranging a set of identical modules. The field of reconfigurable modular robotics emerged after Fukuda, *et al*. demonstrated the cellular robot (CEBOT) in 1988 [11]. Whereas programmable matter began life in the computer science and electrical engineering regime, reconfigurable modular robotics emerged on the macro scale with a strong mechanical engineering flavor. This mechanical emphasis is evidenced in the structures of the PolyBot G3, created by the Palo Alto Research Center (PARC) in 2002, the Molecube system demonstrated by Cornell in 2005, and the SuperBot system from the University of Southern California in 2006, which are all seen in Figure 6. Left to right: PolyBot G3 from PARC, Molecubes from Cornell, and SuperBot from USC. below [12]. One might suggest simply scaling down these previously demonstrated robots; however, as previously pointed out by Slocum [13], the complex geometrical shapes and precise manufacturing tolerances vital to these designs' successful actuation simply cannot be replicated at the microscale with modern surface micromachining processes.

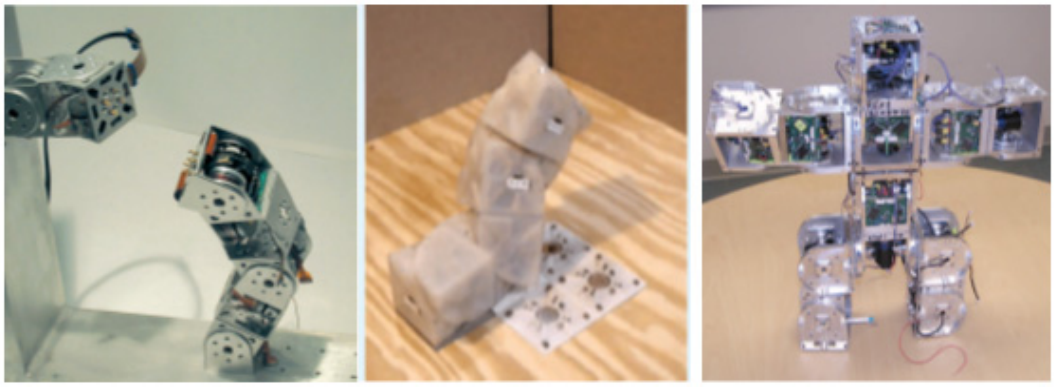

**Figure 6. Left to right: PolyBot G3 from PARC, Molecubes from Cornell, and SuperBot from USC [12].**

### *Solid-State Microrobotics*

To circumvent the difficulties associated with fabrication of micromechanical parts, programmable matter researchers have shifted their focus towards solid-state, non-mechanical structures and actuation mechanisms. Modular microrobot systems employing electromagnetic or electrostatic actuation mechanisms can be classified as solid-state microrobots. The first notable attempt at a solid state system was the Claytronics project initiated by Goldstein, *et al*. at Carnegie Mellon and Intel in 2002 [14]. These modular robot prototypes, or "catoms," moved relative to one another by energizing adjacent magnetic coils arranged around a cylindrical structure, as seen in Figure 7 [15].

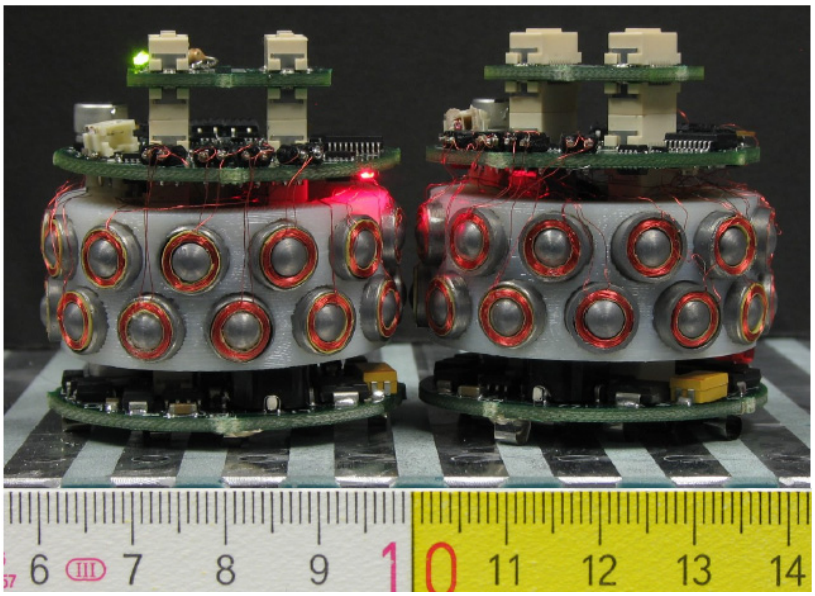


**Figure 7. Cylindrical prototype catoms. These microrobots are each 44 mm in diameter, with 24 electromagnets arranged around the diameters [14].**

A similar project to the Claytronics catoms is the work done on the Robot Pebbles system by Gilpin, *et al*. at MIT. The Robot Pebbles, shown in Figure 8, utilize a custom-designed electropermanent magnetic actuation mechanism which is calculated to improve connection strength while reducing power requirements. The group sees the Robot Pebbles as a path towards a "smart sand" programmable matter system, however the current module size is still 12 mm per side, and the assembly admittedly still relies on extensive "GSWT," or graduate student with tweezers, interaction [16, 17].

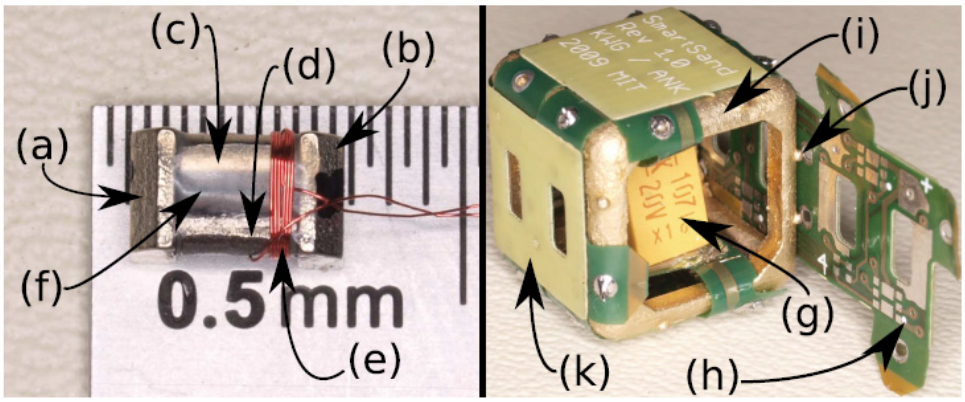


**Figure 8. Robot Pebbles system from MIT, showing (a,b) electropermanent magnet poles, along with (c) Alnico and (d) NdFeB magnets. The magnets are wrapped with (e) #40 AWG wire and held together with an epoxy (f). The capacitor (g) used to power the cube is soldered to the flex circuit (h), which attaches to the brass frame (i) via a set of nubs (j). The magnets protrude 0.25 mm through the cutouts in the cube faces (k) [16].**

As discussed previously, the proposed design from AFRL relies on an electrostatic actuation mechanism. Electrostatics are a popular method for microactuation, as electrostatic force generally scales with dimension at a first or second order, allowing for high forces over small areas, although the high requisite voltages propose some challenges [18]. Using a 90 V limit, Reid, *et al*. calculated that a sphere 0.7 mm diameter or less with 39 equally spaced electrodes would be capable of climbing a vertical surface. The estimated power requirement for 300 rpm (1.2 cm/s) movement is then approximately 1 μW [2]. This power could be provided by a photovoltaic cell similar to the 400 μm by 400 μm PV cell proposed by Bellew, *et al*., which demonstrated a power output of 62.8 $\mu W/mm^2$ at a peak voltage of 88.5 V [19].

The goal of this research is to develop a novel packaging scheme which is compatible with a variety of microdevices and microrobot prototypes, similar to those discussed above. A spheroidal shape, transparent outer shell, and sealed environment are all characteristics which allow such a package to fulfill the needs of many varied

applications. However, for such devices to ever be truly viable, production techniques must be considered that allow for precise and efficient mass fabrication. In the modern world, microelectronics fabrication techniques represent the pinnacle of precise manufacturing at the microscale, and hence are targeted as the viable path forward.

**Microelectromechanical Systems**

The trend of miniaturization and multiplication in microelectronics fabrication has followed Moore's Law since the 1960's, leading to modern processes with 22 nm or better resolution [20]. However, many of the fabrication techniques originally developed for the semiconductor industry have been repurposed to create microelectromechanical systems, or MEMS devices. According to Ki Bang Lee, in *Principles of Microelectromechanical Systems*, MEMS are, "systems that include at least one set of electrical and mechanical components for a specific purpose," and range in size, "from 1 μm to a few hundred micrometers, and the overall size is approximately less than 1 mm" [21] . The first MEMS device, designed by Nathanson, *et al*. in 1965, was an electrostatically actuated cantilever used to filter or amplify electrical signals. Today, MEMS devices have expanded to include diverse capabilities, due to a wide array of actuation mechanisms and sensing mechanisms. However, from Nathanson's first cantilever design to today's most complex devices, micromachining methods adopted from microelectronic fabrication techniques have formed the backbone of what came to be known as MEMS fabrication technology [21].

Micromachining methods can be divided into *bulk micromachining*, which focuses on etching away a silicon (or other crystalline material) substrate, and *surface*

*micromachining*, which uses layers of deposited films to build mechanical parts above the substrate's surface. The complex structures which can be patterned using surface micromachining have made it the popular focus of MEMS researchers ever since Nathanson built his first cantilever [22]. MEMS devices fabricated with a commercial surface micromachining process are shown in Figure 9. Despite the popularity of high resolution surface micromachining approaches for research projects, bulk micromachining is actually the more prevalent technology in commercially available MEMS devices [23].

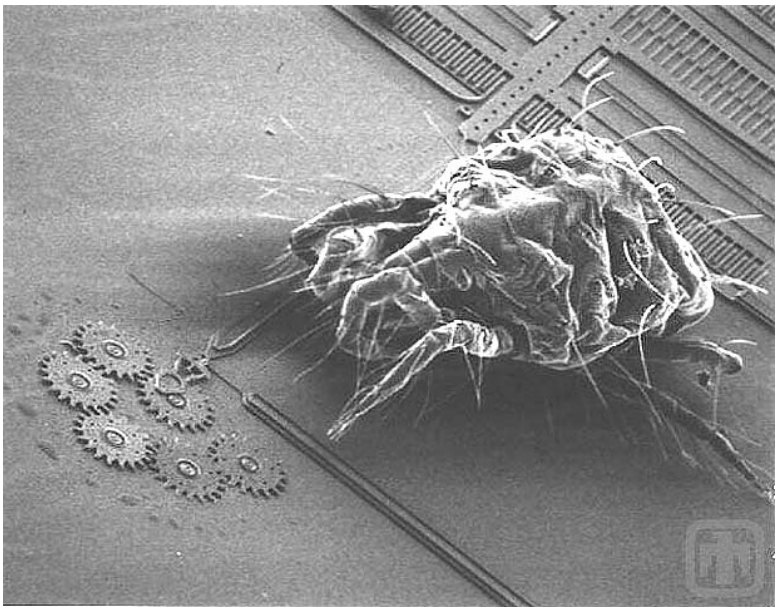

**Figure 9. A MEMS electrostatic comb drive actuator with associated gear train is dwarfed by a spider mite. The devices shown were created in polysilicon using the Sandia Ultra-planar Multi-level MEMS Technology 5, or SUMMiT V$^{TM}$, surface micromachining fabrication process. Courtesy of Sandia National Laboratories [24].**

While surface and bulk micromachining processes are responsible for patterning devices, no MEMS fabrication process is complete without proper packaging and assembly, which can be accomplished through wafer bonding, flip-chip technology borrowed from the microelectronics world, or autonomous assembly [22]. To develop the improved microdevice packaging solution presented in this thesis, a variety of fabrication methods which span the breadth of MEMS technologies are analyzed.

***Bulk Micromachining***

The practice of selectively removing large amounts of material from a crystalline substrate is commonly referred to as bulk micromachining, and is usually accomplished via some chemically-assisted etching process. Etches can be performed in aqueous chemistries, known as *wet etching*, or in chemical vapors and plasmas, with the latter two methods known as *dry etching*. Furthermore, etches can be *isotropic*, rounded with equal etch rates in all directions, or *anisotropic*, which is defined by flat surfaces and sharp angles [23]. With the stated goal of this research being the development of a process to create a spheroidal microdevice package, isotropic etching is most important.

Three common etchants used for isotropic etching of silicon are sulfur hexafluoride ($SF_6$) plasma, xenon difluoride ($XeF_2$) vapor, and an aqueous solution known as HNA. The solution HNA is composed of hydrofluoric acid (HF), nitric acid ($HNO_3$), and acetic acid ($CH_3COOH$), although similar but slightly inferior results can be obtained using water in place of the acetic acid. Of these three, wet etching in HNA with sufficient agitation generally produces the smoothest, most uniform, and most spherical etch fronts, while etching at significantly higher rates than either $SF_6$ or $XeF_2$ [23].

HNA Etching

The chemical system of HNA was studied extensively by Robbins and Schwartz in the 1950's and 1960's and is used commonly in semiconductor fabrication [25-27]. Robbins and Schwartz's work provided the basis for much of what we know about the HNA system today and linked various etch compositions to experimentally determine etch rates, as seen in Figure 10. For example, an etch composed of 70 parts $HNO_3$/20 parts $CH_3COOH$/10 parts HF is expected to demonstrate an etch rate of approximately 33 μm/min in bulk silicon.

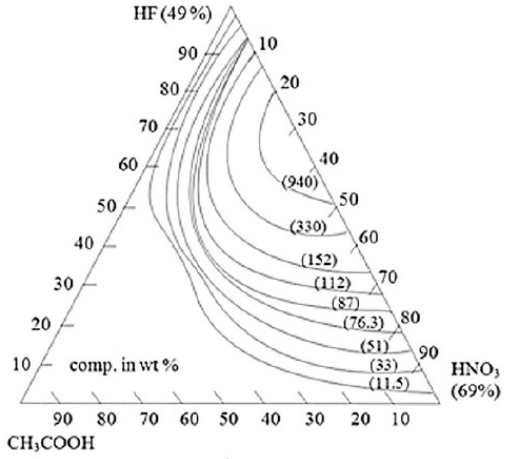


**Figure 10. Curves of constant silicon etch rate (μm/min) as a function of etchant composition in the system of HF, $HNO_3$, and $CH_3COOH$, from Hamzah, *et al.* [28]**

The etching of silicon by HNA is really a three part reaction. First, holes are produced by $HNO_3$ as it oxidizes Si, according to Equation 1. In this process the $HNO_2$ re-enters the reaction to produce more holes until the reaction has stabilized and a steady-state concentration of $HNO_2$ is reached.

$$HNO_3 + H_2O + HNO_2 \rightarrow 2HNO_2 + 2OH^- + 2H^+ \quad (1)$$

Next, the $OH^-$ groups combine with the oxidized Si to form $SiO_2$, releasing hydrogen gas ($H_2$) in the process, according to Equation 2.

$$Si^{4+} + 4OH^- \rightarrow SiO_2 + H_2 \quad (2)$$

Finally, the HF dissolves the $SiO_2$ according to Equation 3.

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \quad (3)$$

Therefore, the (albeit simplified) overall reaction can be described by Equation 4.

$$Si + HNO_3 + 6HF \rightarrow H_2SiF_6 + HNO_2 + H_2O + H_2 \quad (4)$$

Acetic acid provides a better sustained reaction than water due to its low polarity, which prevents the dissociation of $HNO_3$ into $NO_3^-$ and $H^+$. This promotes better oxidation of the silicon surface [29].

The characteristics of HNA etch results are highly dependent on etch composition, temperature, and agitation. At high HF and low $HNO_3$ concentrations, the etch is limited by the rate of oxidation and is more likely to be affected by crystal orientation, dopants, and temperature. At nearly equal concentrations of both HF and $HNO_3$, with low diluent concentrations, the etch rate is maximal; although, the etch is more difficult to control and can lead to rough, pitted surfaces. Finally, at high $HNO_3$ and low HF concentrations, the etch rate is controlled by the ability of the HF to dissolve $SiO_2$, resulting in a truly polishing etch with less dependence on temperature and anisotropies of 1% or less due to crystal orientations [29]. The effect of temperature on HNA etches was studied by Robbins and Schwartz, with an example plot of a reaction's temperature dependence provided in Figure 11.

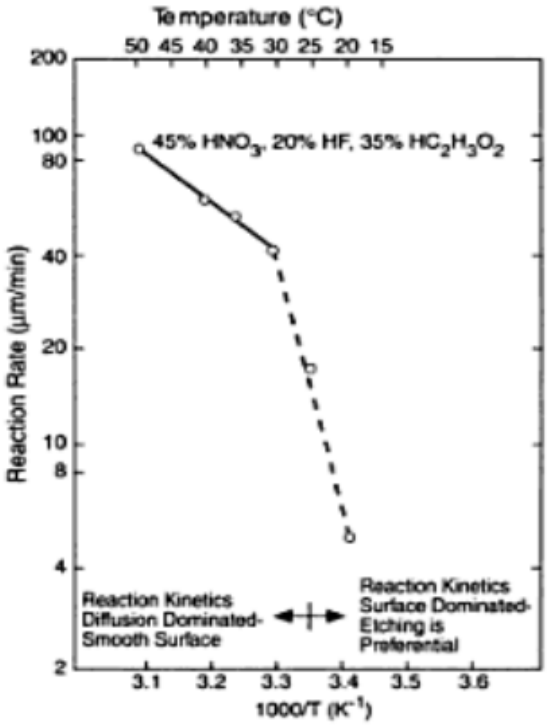


**Figure 11. Temperature dependence of the etch rate of Si in HNA, showing a higher activation energy below 30°C and a lower activation energy above this temperature, as indicated by the change in slope. From Robbins and Schwartz [27].**

While agitation has always been recommended to promote a more isotropic profile [23, 29], more recent research by Lee, *et al*. indicates that vertical agitation is necessary to facilitate periodic degassing. The degassing interval is especially critical to prevent etch shallowing and promote a truly hemispherical profile [30]. The gases formed in HNA etching are not to be neglected, as previous research studies have successfully used the gaseous etch byproducts as a method of limiting the etch progress. However, this method creates oblate hemispheroids, with lateral etch rates nearly 50% higher than vertical etch rates [31-32]. The information gathered from these studies provides valuable reference for researchers interested in fabrication techniques involving bulk isotropic etches conducted with HNA.

Plasma Etching

Apart from wet chemical etching exists dry plasma-assisted etching, which relies on a low pressure gas being ionized through the application of a strong electric field. This creates a plasma made up of equal numbers of positively and negatively charged particles, as well as a number of neutral (often chemically reactive) species. The heavy positive ions can be accelerated by the electric field to bombard the surface and perform physical sputter etching, or the neutral gaseous species can be transferred to the surface to perform chemical etching. Chemical etching yields high etch rates, good selectivity, and generally isotropic profiles, while physical etching generally exhibits less selectivity, higher surface damage, and more anisotropic profiles. In order to take advantage of both etch mechanisms, a process called reactive ion etching (RIE) is commonly utilized. In RIE, the wafer is held by the bottom electrode of a parallel plate diode, with the plasma above its surface. This configuration, shown in Figure 12, creates a large negative bias at the wafer surface, which, when combined with low operating pressures (<500 mTorr), results in heavy bombardment of energetic ions to augment the chemical etching [33].

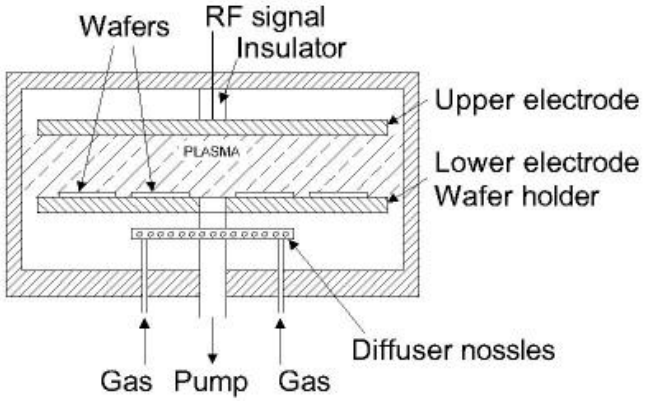


**Figure 12. Schematic of typical parallel-plate RIE system [34].**

While RIE allows researchers to blend chemical and physical etch methods to obtain precise results, it generally cannot create deep anisotropic etches or achieve truly high etch rates. As the field of MEMS grew, demand for a system with such capabilities increased, until the invention of Deep Reactive Ion Etching (DRIE), or the Bosch Process. The Bosch Process is specifically designed to achieve deep, vertical sidewalls by alternating isotropic, fluorine-based plasma etches with fluorocarbon-based sidewall passivation processes. Although originally envisioned for anisotropic etching, certain characteristics of DRIE systems make it an intriguing option for performing large, precise isotropic etches. More specifically, DRIE systems generally have large capacity turbo molecular pumps, a purely inductively coupled plasma, independent wafer bias controls, and high efficiency wafer cooling. These systems allow for high gas flow rates and increased plasma power, uniformity, and control, which ultimately lead to vastly increased etch rates [35]. An example schematic of an inductively coupled plasma etch system is provided in Figure 13.

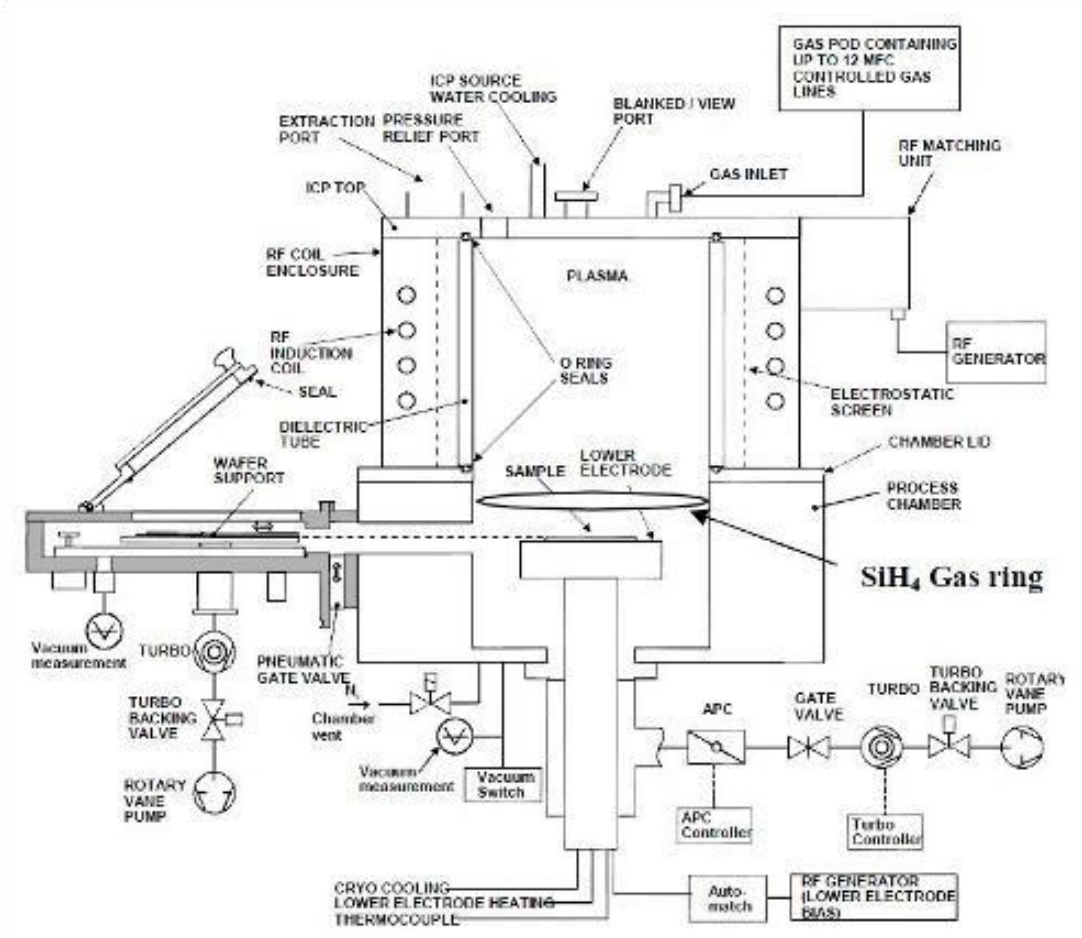


**Figure 13. Example schematic of a typical ICP-powered DRIE system [35].**

$SF_6$ is a popular silicon etchant due to the ability to strip away its fluorine (F) atoms in a plasma. Furthermore, it has been shown that the etch rates achieved with $SF_6$ are approximately a full order of magnitude higher than those of $CF_4$. This is partially due to the greater number of atomic fluorine atoms, but also because $SF_6$ does not polymerize Si surfaces like freons such as $CF_4$ and $CHF_3$ do. The precise composition of an $SF_6$ plasma is extremely complicated and depends on a number of plasma parameters, but is described in great detail by Picard, *et al*. [36]. Additionally, it has been determined that the addition of small amounts of $O_2$ into the plasma further increases the number of F

atoms. However, excess $O_2$ competes with the fluoride reactions, which can slow the etch and increase anisotropy [37]. As a Si surface is exposed to the released F atoms, a Si-F crust forms on approximately the first 5 layers of atoms. More F atoms then penetrate through this layer to attack subsurface Si-Si bonds, eventually releasing silicon in one of two gaseous products, $SiF_2$ or $SiF_4$. Most silicon (70-95%) leaves the surface as $SiF_4$, which is a stable product. The $SiF_2$ is a free radical that subsequently reacts with additional F atoms to create more $SiF_4$ and an excited state of $SiF_3$, which exhibits chemiluminescense at ~500 nm. Equations 5-9 describe the reaction branches. The overall etch mechanism of Si in $SF_6$ and other fluorine-containing plasmas is detailed by Daniel Flamm [38].

$$3F + F - Si \rightarrow SiF_4 \tag{5}$$

$$F + F - Si \rightarrow SiF_2 \tag{6}$$

$$SiF_2 + 2F \rightarrow SiF_4 \tag{7}$$

$$SiF_2 + F(F_2) \rightarrow SiF_3^*(+F) \tag{8}$$

$$SiF_3^* \rightarrow SiF_3 + h\nu_{continuum} \tag{9}$$

Vapor Etching

A final method of achieving isotropic etches in silicon is vapor-phase etching. The most popular vapor etchant of silicon is $XeF_2$, which can be sublimed from its solid state at room temperature and pressures below 1 torr [23]. Other halogen fluorides such as $ClF_3$, $BrF_3$, and $IF_5$ can be used in the same manner, although they can present more safety concerns. Although again relying on the reaction of fluorine with silicon, the

kinetics and rates of molecular ($F_2$) plasmaless etching are much different than those observed in atomic (F) etching. The reaction is approximately described by Equation 10.

$$2XeF_2 + Si \rightarrow 2Xe + SiF_4 \quad (10)$$

$XeF_2$ exhibits extremely high selectivity for aluminum, silicon dioxide, silicon nitride, and photoresist, making it a useful etchant for deep etches or post processing on CMOS circuits. However, the high surface roughness (~10 μm) associated with $XeF_2$ inhibits its use in many applications, although many research efforts have been aimed at mitigating this issue [23, 39, 40].

***Surface Micromachining***

Surface micromachining is an additive process which is used to build structures on top of the surface of a substrate. Structures are created by patterning layers of different materials using photolithography, film deposition, and etching. In general, as structure or micromachine complexity increases, so does the number of layers necessary to successfully fabricate it. An example surface micromachining processes might begin with the deposition of a sacrificial layer, usually a photoresist, $SiO_2$, or silicon nitride. Next, a photoresist layer is deposited and patterned. If a structure is to be attached, or anchored, to the substrate, this photoresist layer will serve as a mask for etching away the underlying sacrificial layer in these windows. A structural layer of metal or hard film can then be deposited. Another layer of photoresist may be deposited and patterned to define a desired geometry in the structural layer. Etching is performed on the structural layer, photoresist is removed, and another etch process removes the sacrificial layer, leaving a

free-standing structure attached to the substrate only at its anchor(s). Figure 14 illustrates this process.

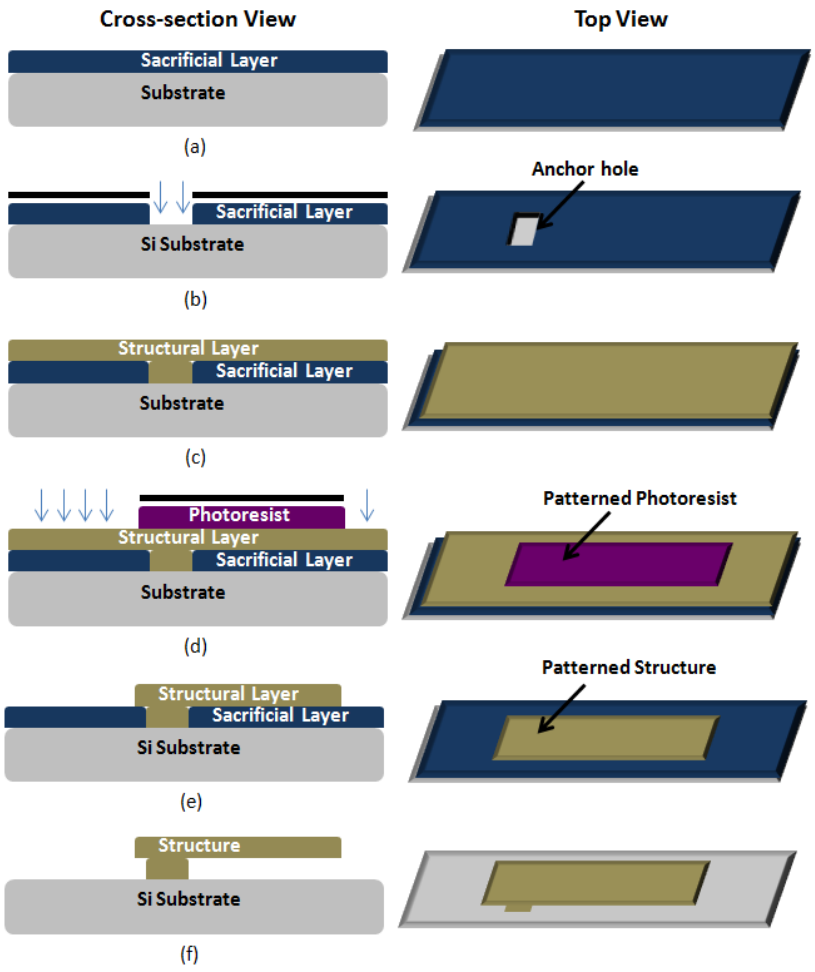


**Figure 14. Example surface micromachining process showing the fabrication of a cantilever beam. The process steps include: (a) sacrificial layer deposition, (b) sacrificial layer patterning with photomask and removal to create anchor hole (c) structural layer deposition, (d) photoresist patterning with second photomask and developer, (e) structural layer etching using photoresist as mask, and (f) sacrificial layer etch to release cantilever structure.**

In any surface micromachining process, the position of subsequent photomasks is critical to obtaining desired results; hence, a system of alignment marks and mask windows must be devised to ensure proper positioning. Simple structures, such as the

cantilever beam shown in Figure 14, can generally be fabricated in research cleanrooms such as those at AFIT or AFRL. Meanwhile, commercial MEMS foundry processes such as SUMMiT V™ from Sandia National Laboratories or PolyMUMPs® from MEMSCAP are typically used for more complex structures [41] [42].

Photolithography

At the heart of nearly every microelectronics or MEMS project is a process known as photolithography, which is used to define regions where etching or film deposition will take place. In photolithography, geometric patterns are transferred to a layer of photosensitive material called *photoresist* using ultraviolet light. Depending on the photoresist chemistry, areas exposed to ultraviolet radiation either become more soluble and easily wash away in a developer (known as a positive photoresist) or less soluble and difficult to remove (a negative photoresist). While the two types of photoresist may appear similar to the human eye, their chemical composition is very different. Positive resists are composed of a photosensitive compound, a base resin, and an organic solvent. The solvent keeps the photoresist in its liquid form until evaporating as the photoresist is spread across the wafer in a process known as spin coating. After coating, the photoresist is insoluble in developer until the photosensitive compound absorbs enough UV radiation to change the resin's chemical structure, making it soluble in specially selected developer solutions. Negative photoresists are polymers combined with a photosensitive compound. The photosensitive compound absorbs UV radiation and converts it into chemical energy to promote a polymer cross-linking reaction. Once cross-linked, negative photoresist is insoluble in its developer and forms a highly durable film [33].

The photolithography process generally begins with the creation of a photomask, which is a glass substrate covered with a layer of chrome and photoresist. The photoresist is precisely exposed using a laser or electron beam lithography system and later developed to reveal the chrome layer beneath. The exposed areas of this chrome layer are removed in a chemical bath before the last of the photoresist is stripped, leaving transparent windows in some areas and reflective chrome in others. This photomask is then used to pattern photoresist over the entire surface of a wafer in a single exposure from a non-directional light source, allowing for multiple wafers to be patterned with the same design in minimal time [33]. This optical shadow printing technique is depicted in Figure 15.

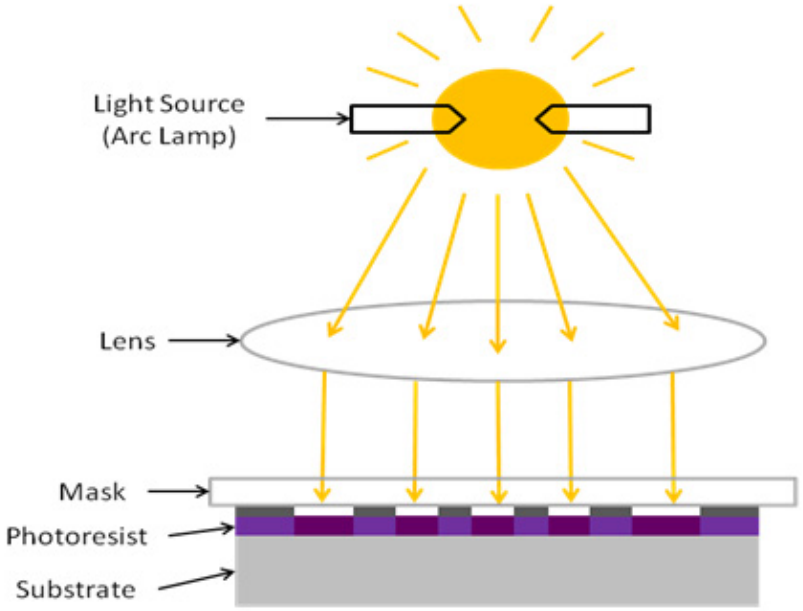


**Figure 15. Simplified schematic of lithographic patterning wafers using a chrome mask and photoresist. Modified from [33].**

The photolithography processes developed for surface micromachining are best suited for creating thin layers with very mild surface topography. In this research project, the application of bulk micromachining to create deep hemispherical cavities prior to surface micromachining creates a number of challenges. High aspect-ratio photolithography on severe surface topographies is a particularly challenging aspect of the proposed research.

As mentioned previously, the most common method of coating a wafer with photoresist is spin coating, in which liquid droplets of photoresist are placed in the center of the wafer and spread to its edges as the wafer is spun at high rates (often ~4000 rpm). On a planar surface, this creates a smooth, uniform coating over the wafer. However, over severe topography, such as a 300 μm deep through-Si via (TSV) or a 500 μm hemispherical cavity, spin coated resists perform very poorly. The two biggest problems experienced are photoresist pulling back from sharp edges at the top of an etched cavity, and photoresist pooling in the bottom of an etched cavity, as shown in Figure 16 [43].

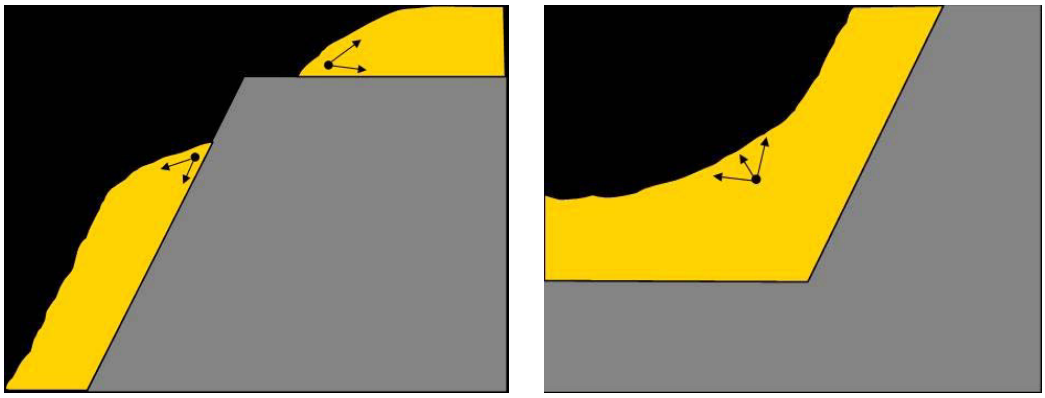

**Figure 16. Left: The physical behavior of a liquid-spin coated photoresist at a sharp edge, as surface tension and gravity work to pull the photoresist away from the edge. Right: The typical pooling of liquid photoresists in the corners of etched cavities due to surface tension [43].**

Therefore, in an effort to overcome these phenomena, new coating methods and photoresists have been developed [44]. The first of these methods involves the electroplating of photoresist. This is known as electrodeposition, and is made possible with special photoresists developed by Shipley Ltd, known as PEPR 2400 and Eagle 2100 ED. The photoresists are actually aqueous solutions containing positively charged "micelles" which collect on the cathode of a plating bath. By coating a wafer in a thin conductive layer, the wafer surface can be made into the cathode while using a stainless steel plate as an anode. Bath temperature, voltage, and concentration of photoresist solids determine the final coating thickness; however, the process is self-terminating after only a few seconds, as the photoresist forms an insulating film over the conductive wafer surface. Ultimately, electrodeposition produces the most uniform coverage of photoresist over severe topographies, and can even be used to coat cavities with vertical walls [45] [46]. The experimental performance of Eagle 2100 ED photoresist is shown in Figure 17.

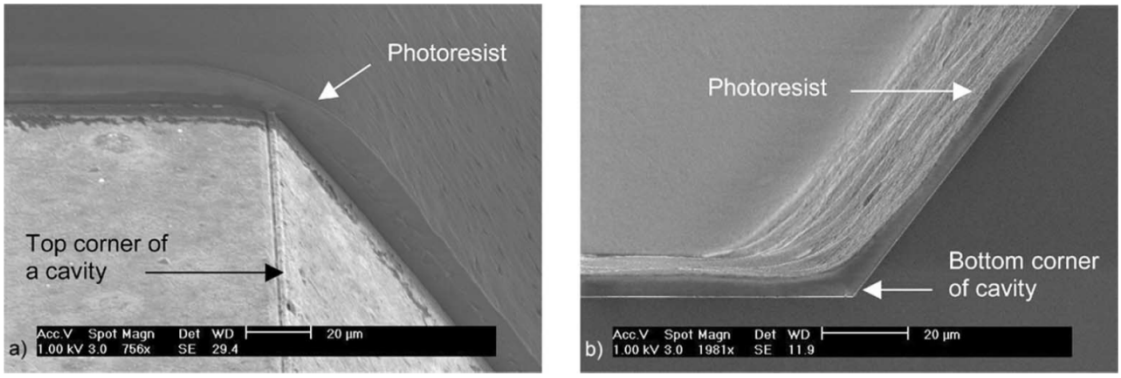


**Figure 17. SEM photographs of electrodeposited photoresist at a) an obtuse corner of a 375 µm deep etched cavity in Si, and b) the bottom corner of the same cavity [46].**

Another newly popular method for patterning 3D surfaces is spray coating. For many years, commercial solutions formulated specifically for spray coating did not exist, so researchers mixed conventional photoresists with solvents such as methyl-ethyl ketone (MEK) and metoxy-propyl acetate (PGMEA) to adjust properties such as evaporation rate and viscosity [47]. A popular commercial spray coating system is the EVG 101 offered by EV Group, which utilizes an ultrasonic nozzle to dispense small photoresist droplets with a mean diameter of approximately 20 µm [48]. Resists must be diluted to viscosities below 20 centiStokes to ensure compatibility with the ultrasonic nozzle. Besides viscosity and evaporation rate, parameters such as wafer spin speed, nozzle scanning speed and distance from substrate, spray pressure, and wafer temperature all affect the uniformity of deposited films over different topographies. In general, a higher evaporation rate reduces the flow of photoresist away from edges and into corners, although this also results in a rougher surface [47]. Ultimately, a careful selection of process parameters can allow for conformal coatings with uniformities over large features

nearly equal to those produced by electrodeposition. A good example of a conformal spray coated photoresist layer produced in an EVG 101 system can be seen in Figure 18.

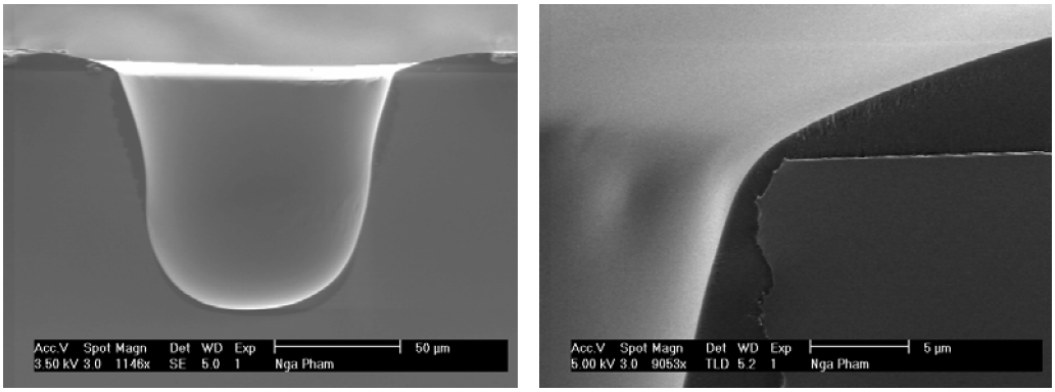


**Figure 18. Left: an SEM photograph of a 100 µm deep trench in Si coated in a spray coated layer of AZ4562 photoresist. Right: Close-up view of trench edge showing a continuous layer of photoresist [49].**

The main problem with both electrodeposition and spray coating using systems such as the EVG 101 is the cost associated with the required equipment [44]. In an effort to enable low-cost prototyping and research, MicroChem Corporation has created a self contained aerosol spray-can complete with photoresist and propellant. The photoresist, solvent, and propellant are released through a specially designed nozzle to eliminate bubbling and create uniform coatings. This formulation, known as MicroSpray$^{TM}$, is available as a positive photoresist or as a negative SU-8 based photoresist [50]. An SEM image highlighting the uniform coverage of SU-8 MicroSpray$^{TM}$ is shown in Figure 19.

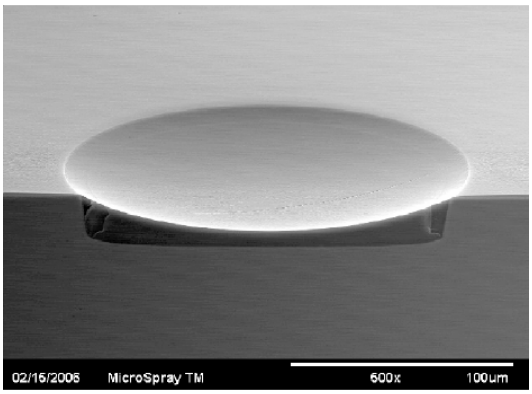


**Figure 19. SEM Image of SU-8 Microspray$^{TM}$ photoresist coating a silicon cavity [50].**

These newly developed photoresist materials and processes offer a variety of options for coating large 3D structures on semiconductor wafers. However, producing a conformal coating of photoresist is just the first step in achieving high resolution photolithography on severe topography.

Once the photoresist is deposited, it must be exposed. In shadow printing, the minimum line width, or feature dimension, is strongly dependent on the gap between the mask and the wafer surface. In the case of patterning at the bottom of an etched cavity, the gap between the mask and surface is equal to the depth plus the thickness of photoresist at the top surface. This effect is similar to switching from a contact lithography process to a proximity lithography process, as shown in Figure 20.

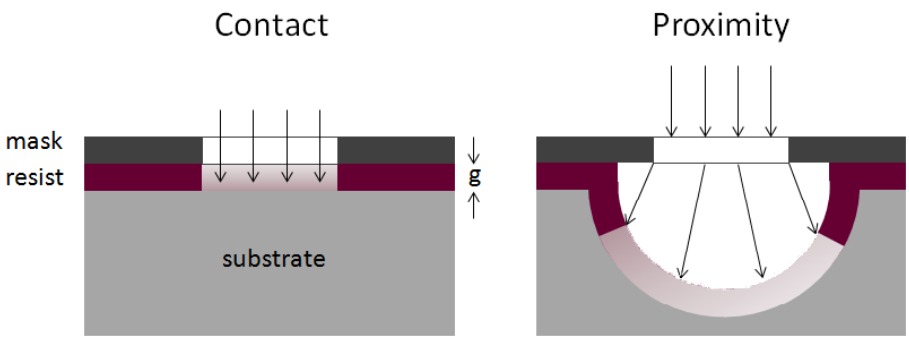


**Figure 20. Illustration of exposure characteristics at different mask-substrate separations.**

The minimum achievable line width is described mathematically in Equation 11,

$$l_m \cong k\sqrt{\lambda g} \tag{11}$$

where $k$ is a process-related constant, and $\lambda$ is the wavelength of exposure radiation [33, 49]. Therefore, to accurately pattern the inner surface of the hemispherical cavities, it is necessary to determine the loss of resolution at the different locations within the cavity. In order to correctly establish this relationship, diffraction effects within the photoresist layer must also be studied, especially for thick resists at large distances from the photomask, as pointed out by Pham, *et al*. [49]. An outstanding example of this effect in a 20 µm thick positive photoresist layer is shown in Figure 21.

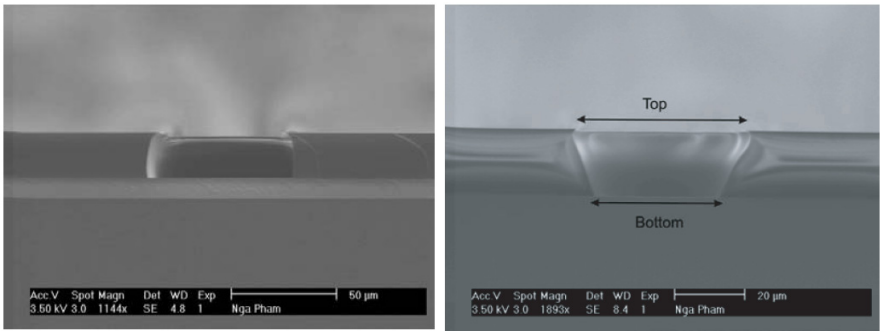


**Figure 21. Pattern on a 20 µm thick positive photoresist layer at different exposure gaps; left: hard contact, and right: proximity exposure with a gap of 120 µm [49].**

## Film Deposition

There are four common methods of depositing a layer or film: evaporation, sputtering, oxidation, and chemical vapor deposition (CVD). Evaporation and sputtering are physical processes which are commonly used to deposit metals, although just about any material can be sputtered onto a wafer. In evaporation, a crucible full of metal is heated until evaporation, at which point it travels in straight lines through a vacuum region to be deposited on a wafer. This directionality results in a non-conformal coating, which is desirable for metal lift-off processes used with many thick photoresists. To obtain conformal layers with a physical process, sputtering is typically used. In any sputtering system, a sample of target material is placed across from the substrate and bombarded by heavy Argon ions, eventually ejecting pieces of the target material onto the substrate. To perform metal sputtering, a DC bias can be used, while an RF sputtering system is necessary to deposit insulating materials. When working with silicon, thermal oxidation can also be used to "grow" a layer of $SiO_2$. This is achieved by heating a wafer to between 900 and 1200°C while exposing it to pure oxygen or water vapor. The growth rate of the oxide is 46% into the silicon surface and 54% outward from the original surface. Additionally, the reaction is slowed by the time it takes the oxidant to diffuse through the previously grown oxide layer. For this reason, thermal oxidation is generally not used to grow films greater than 1 μm in thickness. An $SiO_2$ growth rate chart is provided in Figure 22.

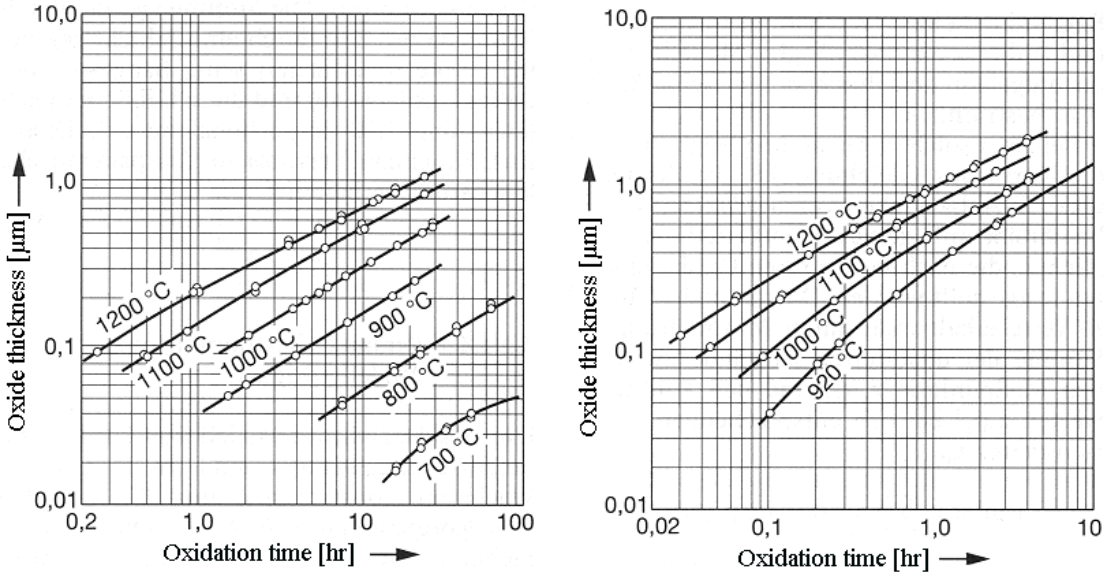


**Figure 22. $SiO_2$ growth rates for dry oxidation (left) and wet oxidation (right) at various temperatures [51].**

The final film deposition process of interest, CVD, uses the reaction of chemicals to deposit a layer on the substrate. CVD can be performed at atmospheric pressure (APCVD), low pressure (LPCVD), and with the assistance of an RF-generated plasma (PECVD). Depending on the gases introduced and processes used, a number of different films can be deposited, including polycrystalline silicon (polysilicon), silicon dioxide, and silicon nitride. A slightly expanded discussion of film deposition is available in Lee's *Principles of Microelectromechanical Systems* [21], while much more in-depth explanations are offered in *Fundamentals of Semiconductor Fabrication* [33] and *Fundamentals of Microfabrication* [29].

***Packaging***

The final step in any microelectronics fabrication process is the packaging of the finished structure. If the integrated circuit or MEMS transducer is the brains of the

system, the packaging can be thought of as the nervous and skeletal systems, providing electrical interconnects, cooling, structural support, and protection [33]. As with most MEMS technologies, many of the packaging processes used today were first explored as methods for packaging integrated circuits. However, as the MEMS industry has grown, the unique packaging requirements for MEMS devices have sparked the development of many new and complex MEMS packaging techniques. According to *Advanced MEMS Packaging*, MEMS packages are usually custom-built and can account for up to 80% of the total product cost [52].

The MEMS packaging process is commonly broken down into a four level hierarchy. The zero level involves device encapsulation; these processes are commonly performed over an entire wafer, and are thus commonly referred to as wafer level packaging techniques. First level packaging processes include the dicing, separation, attachment, connection, and encapsulation of wafer segments called dies. These two packaging levels are generally the most complex, and are responsible for the majority of continuing MEMS packaging techniques. The second and third levels involve the attachment of die packages to substrates (such as printed circuit boards), and the assembly of multiple boards into modules. These levels use much of the same technology which has been matured by the integrated circuit manufacturing community [53].

The premise of this research is to completely remove third level packaging and create a novel second level packaging method which replaces planar substrates with spheroidal thin film capsules. These spheroidal thin film capsules will enclose a conventionally packaged 3D stack of integrated circuit chips containing microprocessors, capacitors, and solar cells. To accomplish this innovative second level packaging process,

two first level processes (flip chip bonding and localized thermal bonding) will be especially useful.

### Flip Chip Bonding

One of the most mature technologies in integrated circuit manufacturing is flip chip bonding, which utilizes solder bumps to connect a chip to its package. This technology was introduced under the name Controlled Collapse Chip Connection, or C4, by IBM in 1964. It has received the moniker "flip chip" bonding to denote the use of the device side of the chip is bonded face down on the substrate wafer. This is accomplished by patterning solder bumps on metal seed pads which have been previously deposited on the chip surface. Pick-and-place alignment tools are then used to flip and align the solder-coated chip surface to evaporated metal bonding pads on the substrate. Once the chip is satisfactorily aligned to the substrate, it can be held in place with a number of adhesives. The chip and substrate are then joined by reflowing the solder with local heating or large area heating in an oven. One particularly useful element of this process is the self-alignment due to surface tension that occurs once solder bumps begin to flow under increasing heat and draws the two metal bonding surfaces into near-perfect alignment. Understandably, flip chip bonding is attractive for its low cost, reliability, and high throughput capability as opposed to a process such as manual wirebonding. In recent years, solderless flip chip technology has been developed using bumps of organic polymer pastes [33]. A comprehensive analysis of flip chip bonding is provided in the *Microelectronics Packaging Handbook* [54].

Localized Thermal Bonding

Localized thermal bonding approaches have been an area of recent research interest, as the limitations of direct Si-Si wafer bonding, anodic bonding, and glass frit bonding become more apparent. These processes generally require large, extremely smooth surface areas, and only work for a limited number of materials. Therefore, techniques utilizing seal rings of various materials have been developed to bond surfaces with limited planar surface areas and less-than-ideal surface roughness. Many of these techniques have been developed specifically with chip capping in mind, but could be repurposed for this research application. Polymer adhesives such as benzocyclobutene (BCB) and epoxy-based photoresists such as SU-8 can be spin-deposited and patterned to form sealing rings that bond with heating in the range of 100-250 °C. Solder rings can also be used to form sealing rings, although the more expensive Au-Sn solder is preferred for applications requiring a hermetic seal. Finally, electroplated gold can be used in either eutectic bonding with Si (which occurs at 363 °C) or in gold-to-gold thermocompression bonding (at ~300 °C and 0.5 MPa applied pressure) [52-53]. An extremely comprehensive study on seal ring bonding methods was sponsored by DARPA, monitored by AFRL, and performed by teams from Raytheon, MIT, UC-Berkeley, and Sandia National Laboratories. During this study, the UC-Berkeley team demonstrated successful Au-Au thermocompression bonding with seal widths of only 25 μm, in a process referred to as hexsil microcapping [55]. A schematic of the hexsil process is provided in Figure 23.

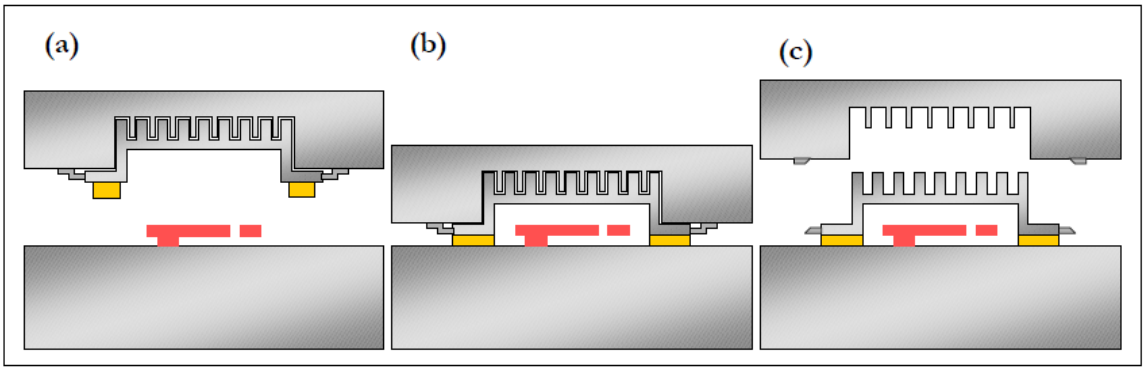


**Figure 23. Schematic of UC-Berkeley designed hexsil cap transfer process; (a) hexsil cap is fabricated on "donor" wafer and aligned with MEMS wafer, (b) the two wafers are brought together and bonded, and (c) the wafers are separated, breaking the cap tethers in the process [55].**

## Particularly Relevant Prior Research

Throughout the last 40 years, many research efforts have focused on creating hemispherical structures in materials such as silicon or glass. These efforts have utilized a variety of wet and dry etch chemistries as well as physical micromachining methods to achieve bulk isotropic micromachining. Additionally, a number of unique masking and wafer processing techniques have been proposed and evaluated. Finally, these research efforts have presented a number of novel methods to monitor progress throughout processing and to characterize completed structures. The following research projects may have been undertaken for applications seemingly unrelated to microdevice packaging, but each project contains elements which have inspired this research.

### *Inertial Confinement Fusion Targets*

The first attempt at creating hollow spherical structures using solid-state processes was made by Wise, *et al*. in 1979. The goal of this research was to investigate the applicability of semiconductor fabrication techniques to the creation of sub-mm$^3$ hollow

spherical shells which hold fusion reactor pellets. Wise and his team proposed a method using $HF/HNO_3$ etching of bulk silicon to create an array of hemispherical cavities. A mask aperture 25% of final hemisphere diameter was found to generate the most isotropic etches with "vigorous" agitation in a solution of 90% $HNO_3$ and 10% HF. Next, two processes were proposed to create hemispheres from either poly-(methyl methacrylate) (PMMA) or metal, or from doped silicon. The first process is described in Figure 24 , while the second is related in Figure 25. PMMA hemishells were successfully released using the first process, and were reported on in the paper. The second process was proposed, but never completed, although Wise expressed confidence in its ability to produce spherical shells [56].

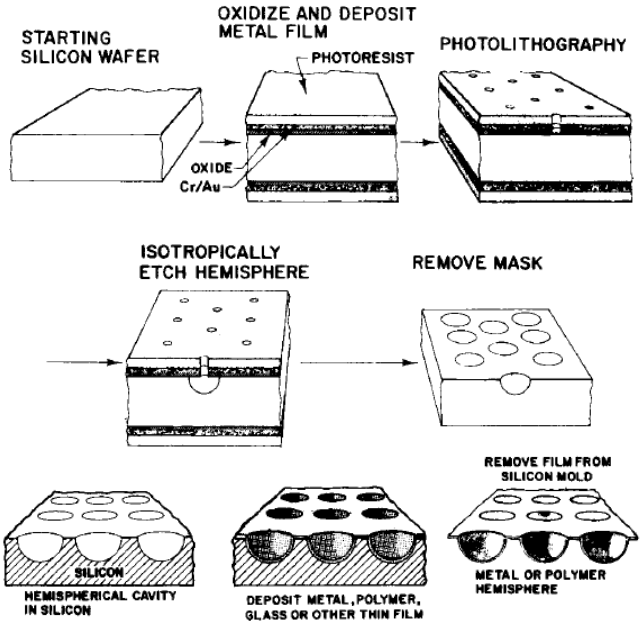


**Figure 24. Process of creating metal or polymer hemispheres from silicon molds; proposed by Wise, *et al.* for use in creating inertial confinement fusion targets [56].**

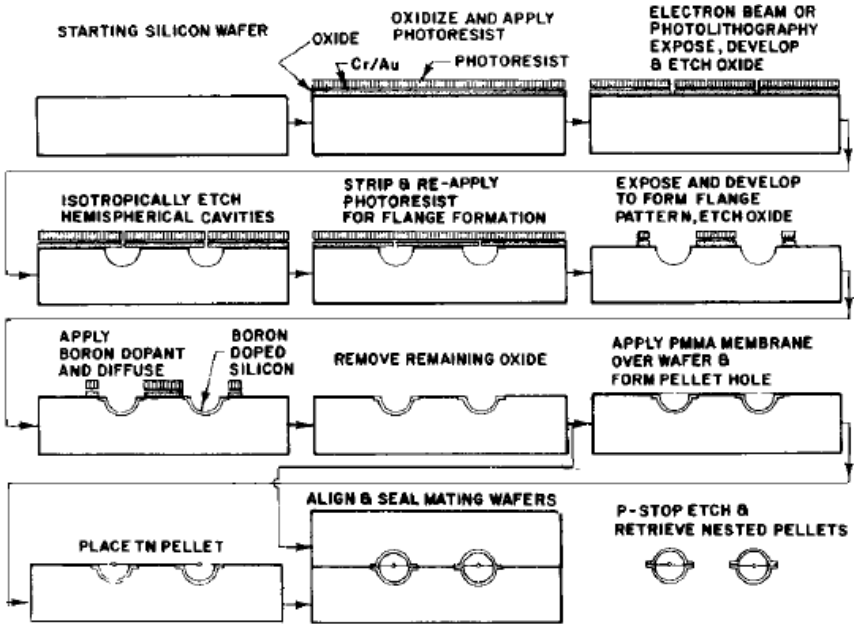


**Figure 25. Process of creating doped hollow silicon hemispheres with centered nuclear fuel pellets; proposed by Wise, *et al.* for use in creating inertial confinement fusion targets [56].**

### *Silicon Microlens and Microlens Mold Fabrication*

More recently, researchers have begun to explore various techniques of creating silicon microlenses and microlens molds with bulk etching. A 2005 study by Larsen, *et al*. investigated the isotropic etch results of $SF_6$ in an ICP source. The etch profiles under various ICP configurations, etch lengths, and mask openings are presented. However, the longest etch performed only lasted 760 seconds, and the deepest etch reached only 61 microns past the wafer surface. Nevertheless, the results provide valuable information on $SF_6$ etch parameter effects and the time progression of the "isotropic" etch. The authors also studied maskless $SF_6$ etching, as they desired a shallower profile for their lens application. The etches were analyzed with white light interferometry and SEM imaging [57]. Figure 26 illustrates the three-part etch process used to obtain the final profile.

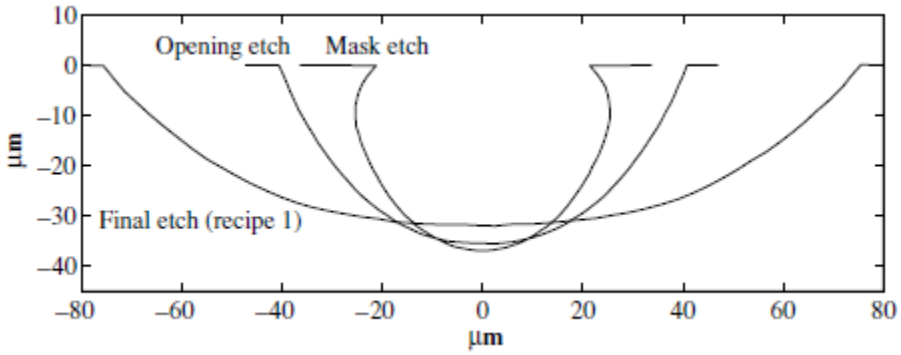


**Figure 26. Etching profiles for masked $SF_6$ ICP etch, followed by two separate unmasked $SF_6$ etch processes to create microlens molds; from Larsen, *et al.* [57].**

A 2009 paper by Albero, *et al*. also investigated isotropic etching of silicon as a method to fabricate microlens molds. However, rather than using an $SF_6$ dry etch process, the same 90:10 $HNO_3$:HF mixture proposed by Wise, *et al*. was used for etching. The hard masking scheme shown in Figure 27 was used in place of a Au-Cr mask. Various size etch holes were created, although all the resultant profiles strongly favored lateral etching to vertical etching, with the disparity increasing with larger mask openings [58].

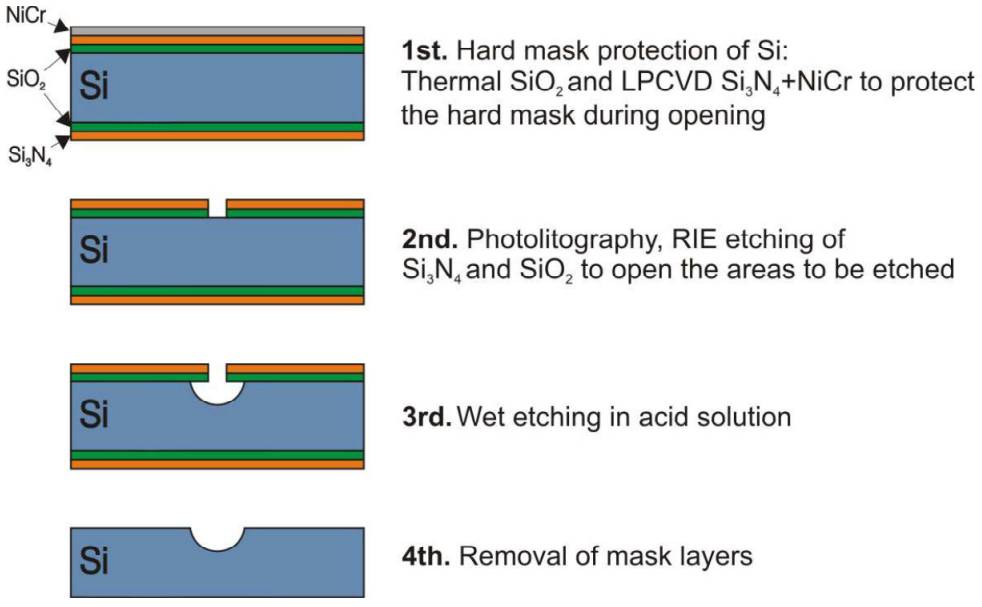


**Figure 27. Process steps used to fabricate the microlens molds from Albero, *et al.* [58].**

A final study involving microlens fabrication was completed in 2012 by Lee, *et al*. This study explored $XeF_2$ etching as well as HNA etching. The authors concluded that, while the etch rate of $XeF_2$ was easily controlled and the sphericity was acceptable, the surface roughness was too rough for use in a lens. No mention of attempts at HNA polishing on the $XeF_2$ cavity is made. The researchers also studied various HNA masking layers before settling on thick (>1 μm) layers of Au/Cr. The most interesting part of this study, however, was the focus on improving vertical/horizontal etch uniformity. A specially designed PTFE jig (shown in Figure 28) was used to vertically agitate wafers while immersed in an HNA bath which also incorporate magnetic stirring, temperature control, and HNA solution ratio control. Periodic degassing of the wafer surface via vertical agitation was found to have distinct effects on the cavities' vertical/horizontal profiles [30].

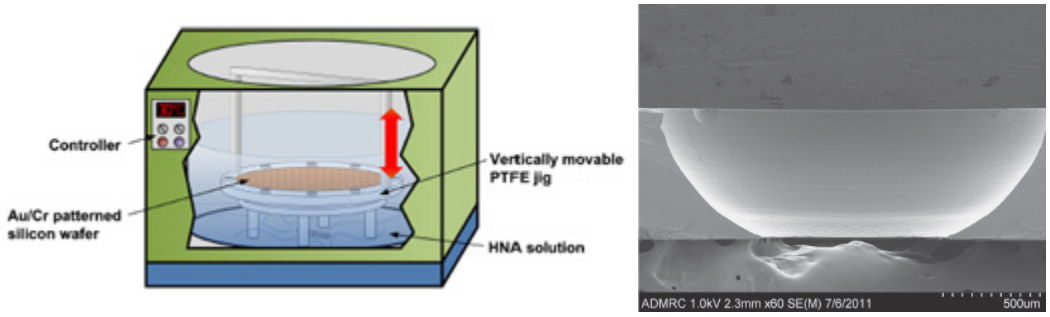


**Figure 28. Left: HNA etchant system designed by Lee, *et al*. to incorporate vertical agitation in HNA etching in an effort to increase vertical etch rates. Right: Hemispherical cavity formed with vertical degassing performed at 60 minutes intervals [30].**

### *Hemispherical Shell Resonators*

A number of very recent studies have also explored some unique MEMS fabrication techniques as possible ways to produce hemispherical shell resonators, which have applications in communication and inertial navigation. A 2011 paper by Pridhodko, *et al*. describes wafer-level glass blowing as one potential method of creating nearly perfect spherical resonators. To perform the glass blowing, a 100 μm thick Pyrex glass wafer was bonded to a silicon wafer which had been patterned with 0.5 mm diameter holes etched 0.8 mm deep with DRIE. The wafer stack is heated above 850°C, the softening point of Pyrex, and the expansion of hot air trapped inside the cavity forces the flat glass to be blown into symmetric spherical shapes. Surface roughness of the outer shell was measured to be below 0.9 nm, and metal traces could be added before glass blowing and survive the process. An illustration of the process is provided in Figure 29 [59].

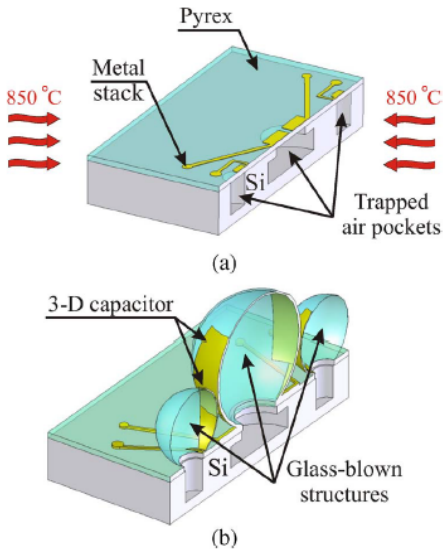


**Figure 29. Illustration of a 3D spherical shell resonator fabricated using wafer-level glass blowing. (a) Planar structure before glass blowing. (b) 3D structure after glass blowing. From [59].**

Another interesting paper involving hemispherical shell resonators is a 2012 conference paper from Chan, *et al*. This research group utilized micro electro discharge machining (μEDM) to perform the bulk machining of silicon. A single electrode was translated across the wafer surface to machine multiple cavities in a two-step process. The electrode is machined from polycrystalline diamond (PCD), and exhibits 20 μm of wear after completing both the rough machining and finish machining of 200 features. However, after the two-step μEDM process, the silicon surface exhibits significant roughness. This surface roughness necessitates a short HNA polishing step before CVD can be used to deposit a low temperature oxide layer and a 1 μm thick structural layer of CVD diamond. Further surface machining steps are taken to pattern the structural layer before etching back the substrate and sacrificial layers to expose the anchored hemispherical resonator. SEM images of micromachining steps and finished resonators are shown in Figure 30. This study also used MATLAB image processing techniques to analyze 2D optical microscope images and extract quantitative measurements of the finished features [60]. This image processing can be seen in Figure 31.

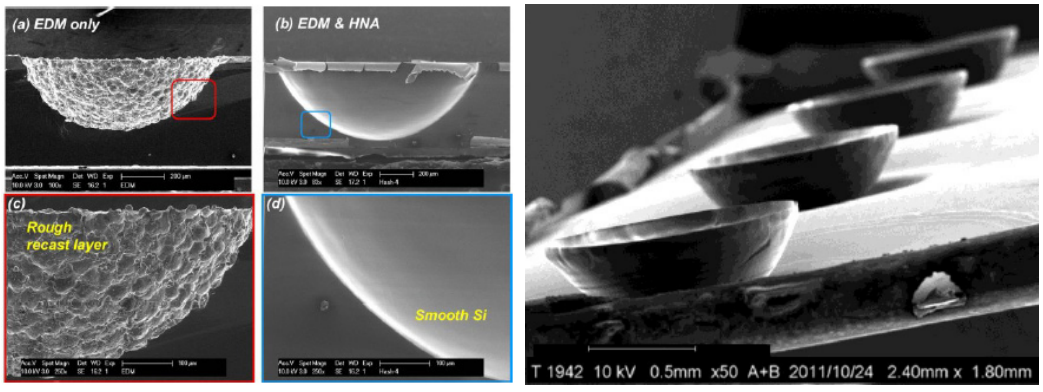


**Figure 30. Left: SEM images of (a&c) silicon surface after μEDM processes and (b&d) the same silicon surface after HNA chemical polishing. Right: Released hemispherical resonators made from CVD diamond and anchored to Si substrate [60].**

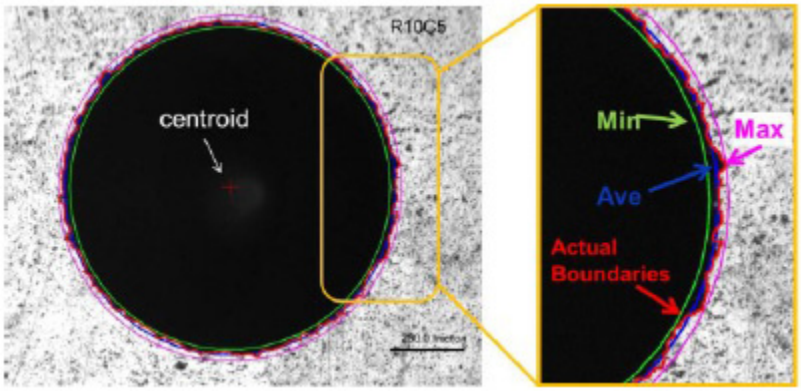


**Figure 31. Image processing steps performed on 2D optical microscope images of μEDM-produced cavities in Si. Edge identification algorithms are used to detect the rim boundary (red line), maximum radius (magenta line), and minimum radius (green line). From these measurements, average radius (blue line), centroid (red cross) and rim roughness and eccentricity (not pictured) can all be calculated [60].**

### *Investigation of Anisotropy in Isotropic Silicon Etching*

A final study with particular relevance to the chosen research topic is that which was undertaken by Svetovoy, *et al*. to precisely analyze anisotropy in HNA etches. The etch was performed with no agitation, which is known to reduce anisotropy. Over 800 images were collected of <100> <110> and <111>-oriented Si wafers at different etch durations. The key findings of this study were that the anisotropy in <100> and <110>-oriented Si wafers can reach 9%, whereas <111> Si orientations display a maximum anisotropy of 1.5%. Additionally, anisotropy increases as mask aperture becomes relatively smaller than the final etch diameter. Finally, the first anisotropy harmonic in <111>-oriented Si wafers can spontaneously rotate 60° as the etch progresses, which means the hexagonal shape of different cavities across the wafer surface may not always be identically oriented. Although these phenomena are all described for HNA etching specifically, they are in better than 0.4% agreement with theory predicted by crystal symmetry. The representative images of this study are provided in Figure 32 [61].

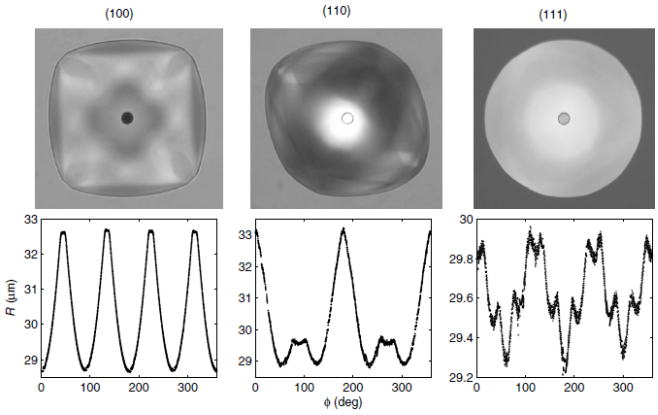


**Figure 32. Top: Optical microscope images of cavities etched for 50 min in wafers of different orientations. Bottom: Under-etch radius as a function of the polar angle $\varphi$ [61].**

## Summary

This chapter presented background literature and previous research which is critical to the understanding of this research project and its place in the current state of technology. As this research is an AFRL-sponsored project and an offshoot of previous AFRL efforts, the origins of the microrobot concept at AFRL were discussed. Ultimately, the previous goal of creating a microrobot structure has been broadened to creating a novel process for microdevice packaging. However, the package concept still has strong ties to the programmable matter and modular reconfigurable robot worlds. The proposed method of microdevice packaging will rely on a collection of MEMS microfabrication techniques. Various bulk and surface micromachining methods were introduced, along with common packaging techniques. Particular attention was devoted to bulk isotropic etching and 3D photolithography, which represent two significant challenges. Finally, similar fabrication attempts spanning the last 40 years were presented, with particularly notable or useful contributions highlighted. The ideas and knowledge relayed in this chapter will form a basis for the decisions made in the ensuing methodology chapter.

# III. Methodology

## Chapter Overview

The primary focus of this research is the exploration of the MEMS fabrication processes necessary to produce a hollow spheroidal package approximately 1 mm in diameter. While certain parts of this research project have been demonstrated in previous research efforts, the overall size and complexity of this design requires new process combinations and fabrication strategies to be considered. Throughout the course of this project, these approaches will be demonstrated, and success or failure will be measured using a variety of tools available at both AFIT and AFRL. The ultimate goal is the demonstration of an efficient fabrication process which reliably produces uniform microdevice packages in accordance with AFRL's research goals. This chapter will provide an overview of the investigations of each process considered as a path to microdevice package fabrication and testing.

## Isotropic Etching

The first process step of the fabrication process chosen for study was the creation of hemispherical cavities in silicon wafers. Hemisphere fabrication attempts were made using bulk micromachining, or, more specifically, isotropic etching techniques. Although discussed in Chapter 2, the bulk isotropic machining methods utilizing $XeF_2$ and μEDM are not available in the AFIT or AFRL cleanrooms, and are therefore outside the scope of this research.

### *HNA Etch Studies*

Based on the reported success of HNA etching in previous research, it was chosen as the first etchant system to investigate [30, 56, 58]. Keeping the results of these previous efforts in mind, the efficacy of different mask materials, the etch performance at varying compositions, and the effects of replacing stirring with agitation from an ultrasonic bath were chosen for further investigation. This was accomplished by performing wet HNA etches on silicon samples and observing the results with optical microscopy and a profilometer.

All wet HNA etching must be performed in polyethylene beakers with polytetrafluoroethylene (PTFE) tools while under a fume hood, as HF is known to attack glass and polystyrene [62]. Additionally, trionic gloves must be worn on top of nitrile or latex gloves, along with apron, goggles, and a face shield being used for personal protection against the very aggressive acids used in this etch. To produce HNA solutions, hydrofluoric, nitric, and acetic acids with concentrations of 49%, 70%, and 99.9% by weight are mixed together at various ratios.

In order to pattern the masking materials, a chrome photomask was written with 3 μm resolution using the Heidelberg® laser writing system. The photomask used to pattern these wafers was designed with a number of 0.8”x0.8” reticles, each containing an array of circles of constant diameter. The diameter of circles varied from reticle to reticle, and were chosen based off Equation 12. According to McLelland, *et al*., Equation 12 describes the mask aperture diameter necessary to create a gas-limited etch of radius *a* [31].

$$d_{mask} = \frac{2a - 400\mu m}{1.8} \tag{12}$$

Therefore, seven different reticles were designed, with aperture sizes chosen to create etched hemispheres ranging from 600-1200 μm in diameter. Mask openings were generously spaced according to the projected size of the completed etches in an effort to avoid thermal interactions between neighboring etch locations.

In order to determine an appropriate masking material, two studies were performed. The first study was conducted on samples masked only with SU-8 photoresist, using HNA solutions mixed at different ratios. SU-8 photoresist was chosen based on its reputation for surviving many harsh etch environments in which other conventional photoresists are typically stripped away. Masking with only a photoresist would be the easiest, quickest, and least costly process, and was therefore explored first. To test the SU-8 photoresist's robustness against the HNA etch, samples were etched in two different HNA solutions. The two different solutions were mixed at ratios of 20:70:10 H:N:A and 10:70:20 H:N:A. These ratios were chosen based on previous research, which indicated they were not overly aggressive while still offering an acceptably high etch rate and good surface finish [28].

In the next study, samples from wafers masked with layers of $SiO_2$, $Si_3N_4$, and SU-8 were exposed to an HNA etch in order to ascertain the benefit of the additional hard masking layers. Samples were etched using fresh solutions of 20:70:10 and10:70:20 H:N:A compositions, with no agitation.

Finally, in an attempt to increase etch rate, promote degassing of the etch cavity, and develop a deeper, more isotropic etch profile, ultrasonic agitation was introduced.

One additional sample was etched at 10:70:20 H:N:A composition. The results of all the wet HNA etch trials are presented in Chapter 4.

***Reactive Ion Etch Studies***

In the AFIT cleanroom, the Trion RIE system is configured to perform etches with gaseous mixtures of $O_2$, $CF_4$, $CHF_3$, and $SF_6$. Etching using the Trion was therefore considered as a potential method for performing the isotropic etches necessary. $SF_6$ plasma, which was discussed in Chapter 2, was chosen for its relatively high etch rates of silicon, as indicated in the studies performed by Williams, *et al*. [63] [64]. Additionally, many $SF_6$ mixes had been used extensively and characterized by past AFIT researchers. Consulting these records, it was found that bulk silicon etch rates in the Trion system were generally in the range of 2.0 to 3.5 μm/min. While these etch rates would be acceptable in many processes, processing times of ~3 to 4 hours would be necessary to achieve 500 μm-deep etches. Therefore, an attempt to increase etch rates was made by altering the RIE RF power setting. Each etch was conducted in 30 minute intervals, with optical microscopy and profilometer readings used to evaluate etch progression. The results of this experiment are detailed in Chapter 4.

***Deep Silicon Etch (DSE) Studies***

The AFIT/AFRL owned Plasma-Therm VERSALINE® Deep Silicon Etch (DSE) system was investigated as another isotropic silicon etching method. This modified DRIE system offers ICP powers up to 2500 W, and independent RF Biases as high as 200 V, along with $SF_6$ flow rates as high as 300 sccm while maintaining chamber pressures anywhere from 5 to 100 mTorr. It was therefore hypothesized that this tool would be capable of producing the deep, isotropic cavities desired. However, in order to achieve

the desired results, the normally anisotropically-tuned process parameters need to be modified. Therefore, an etch study was conducted to determine the optimal process parameters.

In order to conduct this study, twelve 0.5" x 0.5" samples were patterned with 334 μm-diameter openings in SU-8, in the same manner as discussed previously. Prior to dicing and SU-8 patterning, an Omnicoat surface pretreatment from MicroChem was added. This pretreatment is designed to allow SU-8 to lift off with immersion in a bath of Remover PG heated to 80°C for 30 minutes. The ability to remove the SU-8 masking layer was desirable, as it would allow for further study of the completed etch profiles. Once the etches were complete, their profiles were examined using a variety of methods. First, an optical microscope was used to assess the diameter of the etch hole without the need to remove the masking layers. This is possible because the etch pit is clearly visible as a darker circle underneath the somewhat transparent mask layers. A quick measurement with the scale on the optical microscope can relay an estimate of etch diameter, and more detailed observation can relate some visual information on the smoothness and uniformity of the etch. However, to obtain more exact measurements of the etch holes, including depth, diameter, and anisotropy, the Zygo® optical surface profiler is used to render a 3-D image using white light interferometric measurements (IFM). Without removing the masking layers, a complete image of the cavity cannot be obtained, but the bottom and edges of the cavity can be discerned quite easily, as shown in Figure 33. Three cavities were chosen from across each sample surface, and measured to determine smallest and largest diameter as well as ultimate depth. Finally, SEM images of select samples were taken by cleaving the silicon wafers through the center of

a row of etched cavities and examining the cavities from an angle. This method provided crisp images of the cavities, as demonstrated in Figure 34, but failed to provide much more relevant information than white light interferometry. The results of these measurements are provided in Chapter 4.

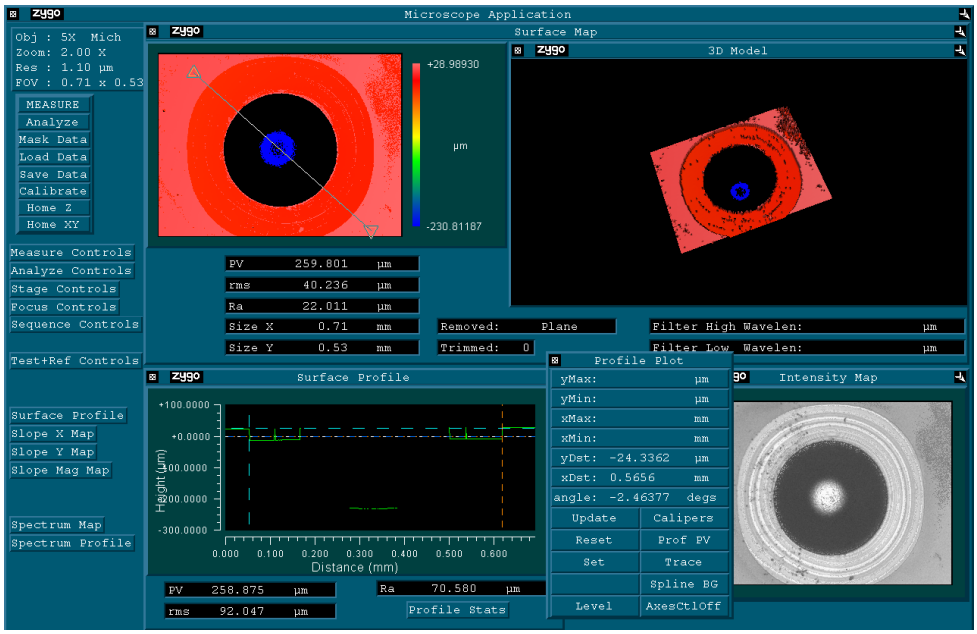


**Figure 33. Screenshot of a Zygo® white light IFM taken on Sample 10 of the DSE parameter etch study.**

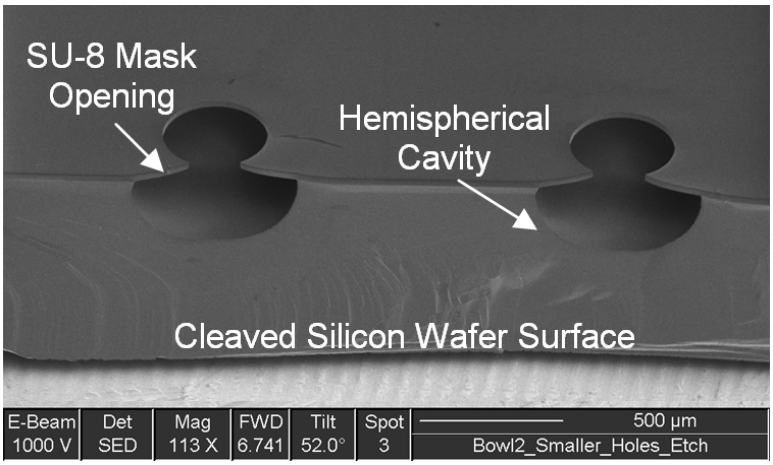


**Figure 34. SEM image of hemispherical cavities in silicon etched with $SF_6$ RIE. This 30 minute etch had a demonstrated isotropic etch rate of approximately 8 µm/min.**

In an attempt to reduce the number of independent variables in the previous study, mask aperture size and etch time had been held constant. However, it was hypothesized that the etch progression in terms of final etch size to original mask opening had an equally important role in determining the etch profile. To test this hypothesis, a new wafer was patterned with Omnicoat and SU-8, reverting back to the original mask with its varying aperture sizes. The chosen wafer was a 3" n-type silicon wafer 1000 μm-thick, with a surface crystal orientation of 5° off the <111> plane. Although previous etches had not penetrated through the entire thickness of the 525 μm-thick wafers, the intent was to continue etching until at least one reticle of cavities reached an average depth of 500 μm. This meant the thicker wafer would be necessary to provide a bit of buffer room for the possibility of an over-etch. Additionally, the use of a <111>-oriented Si wafer would allow for a comparison of anisotropy in DSE-produced cavities on differently oriented wafers. This wafer was then etched for one hour total time, with measurements taken at 30, 40, 50, and 60 minutes. This was accomplished by stopping the etch, removing the wafer from the DSE system, taking multiple IFMs in each reticle, and replacing the wafer before resuming the etch. The results of this study are also detailed in Chapter 4.

**HNA Polishing**

In most isotropic etches, a small area of undercutting is observed around the cavity perimeter. Essentially, the maximum etch diameter does not occur at the surface of the wafer, but rather it occurs a few microns below the surface, leaving an overhanging "lip" of silicon behind. This lip makes depositing a continuous layer of photoresist over the interior surface of the cavity nearly impossible, and would result in a severe departure

from the desired spherical shape of the finished package if left untreated, as shown in Figure 35.

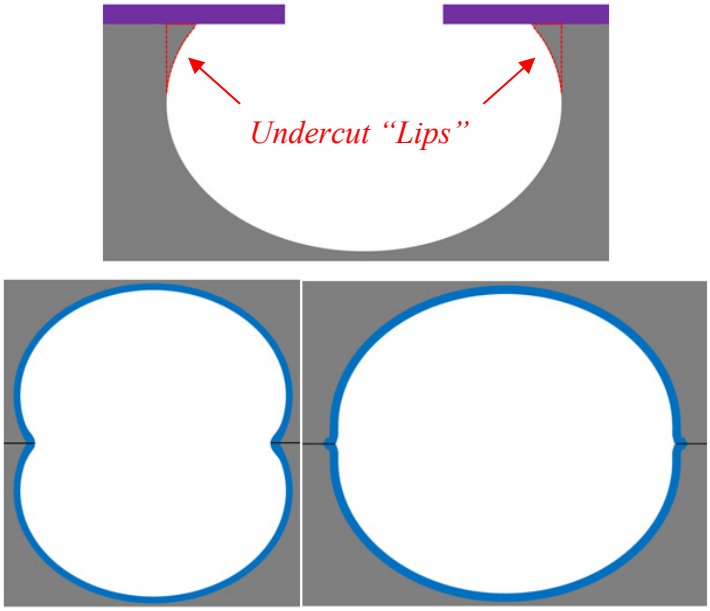


**Figure 35. Top: Illustration of the formation of overhanging lips due to isotropic etch undercutting. Bottom Left: Illustration of an abnormally-shaped sphere which would be produced without the removal of undercut lips. Bottom Right: Illustration of improved spheroidal package after successful HNA removal and rounding of undercut lips.**

In addition to this undercutting, the surface roughness of isotropic etch cavities can be highly variable. In order to achieve a smooth package shell, a cavity surface roughness of less than 100 nm is desired prior to film deposition. In an effort to simultaneously remove the undercut lip and reduce surface roughness, a polishing HNA etch was investigated. This etch is conducted after the removal of SU-8 masking layers so that the undercut lip may be etched from multiple directions, leading to pronounced deterioration. As described in Chapter 2, HNA etches leave highly polished surfaces at high $HNO_3$ and low HF concentrations. Referencing Hamzah, *et al*., a smoothly etched

surface with reasonable etch rate (~3 μm/min) should be achieved at a 10:80:10 H:N:A composition, as indicated in Figure 36 [28].

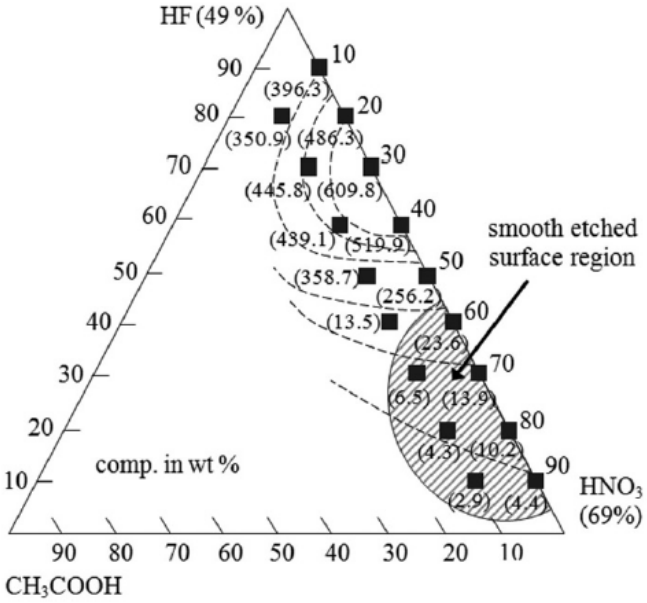


**Figure 36. Experimental HNA etch rate pyramid from Hamzah, *et al.* detailing the region of etchant compositions which produce a highly polished surface [28].**

To conduct this study, samples from the DSE studies are stripped of masking layers and cleaved so that a row of cavities is bisected, revealing their cross-sections. The cross sections are photographed and measured using an optical microscope. Etching is then performed in the same manner and with the same safety precautions as in the previous HNA study, although the silicon samples are simply held with a pair of tweezers and gently agitated while immersed in the HNA solution. The wafers are withdrawn from the solution at 1 minute, 3 minutes, 6 minutes, and 10 minutes total etch time to observe and measure etch progress. Measurements taken on the optical microscope characterize the removal of the undercut lip, while IFM data are used to examine the samples' surface roughness. Results of this study are discussed in Chapter 4.

### MatLab Image Processing Tools

As mentioned previously, optical microscopy, profilometer measurements, and IFM data were used to characterize etch results. One drawback of these methods is that they are very time consuming in terms of researcher man hours. Therefore, a method of image processing and analysis using the commercially available software MatLab was proposed. The three-part analysis process is as follows: a complete sample is imaged via the optical microscope, small area images are stitched together using image correlation methods, and MatLab image processing techniques are applied to recognize etch cavity dimensions at the wafer surface. This allows each etch cavity on a sample to be analyzed without overly taxing the graduate student. Further MatLab processing can be performed to replicate the etch cavities' geometries and export the data in a format compatible with commercial layout software such as L-Edit or AutoCAD. This final step could allow for the automatic generation of subsequent masking layers based off previous etch results. The findings of this work are presented in Chapter 4.

### Photoresist Deposition and Patterning

One of the goals of this project is to determine a method to pattern metal traces onto the interior surfaces of the cavity shells. As discussed in Chapter 2, a burgeoning interest in 3D photolithography led to the development of spray coated and electroplated photoresists. These alternatives have been given sufficient praise for their efficacy, although their associated processing complexity is greatly increased. Therefore, before completely abandoning the idea of spin-coated photoresist, a few of the available photoresists in the AFIT cleanroom were selected and deposited on HNA-polished

samples. The photoresists included Shipley Microposit® S1805 and S1818 photoresists, as well as MicroChem SF11. After patterning a bi-layer photoresist stack of SF-11 and S1818, metal trace layers were evaporated to evaluate the potential for metal lift-off processes using these photoresists. Some results of these trials are discussed in Chapter 4.

# IV. Results and Analysis

## Chapter Overview

In the previous chapter, a variety of experiments and fabrication processes were designed with the intent of discovering an efficient, reliable way to produce hollow spherical packages approximately 1 mm in diameter. In this chapter, the data and observations from these experiments are presented and analyzed. Results are compared to those generated by similar prior research efforts, while background literature is referenced in an attempt to explain apparent anomalies. The results of bulk isotropic etching using HNA, RIE, and DSE are compared with regards to etch consistency and profile characteristics. The advantages and disadvantages of each etch are discussed in terms of their suitability for use in a final fabrication process. The impact of silicon crystal orientation on etch performance is also examined to provide a recommendation as to which substrate orientation is better suited for this application. HNA polishing is explored as a method of improving cavity parameters such as surface roughness, the extent of undercutting, and etch anisotropy. Techniques for photolithographic patterning and metal deposition over severe topographies are investigated and discussed. Finally, a new process for factoring etch results into successive masking layers using MatLab image processing techniques is proposed, developed, and evaluated.

## Wet HNA Etching

The first proposed solution for producing bulk isotropic etches was the use of wet HNA etching. As shown in Chapter 3, this etchant has been studied extensively by previous researchers and used in many similar fabrication attempts. However, HNA

etches had not been commonly performed to this point in the AFIT cleanroom. Therefore, many of the process specifics for performing these etches had to be explored. The effectiveness of different masking materials, etch compositions, and agitation methods were all evaluated with regards to the fabrication of large, hemispherical cavities.

***Sample Preparation***

To begin research, three 525 μm thick, <100>-oriented n-type silicon wafers were selected and prepared. The wafers were cleaned with a standard solvent cleaning process using acetone, methanol, isopropanol, and DI water, followed by a 5 minute hot plate bake at 200°C to complete dehydration. The first wafer would be patterned with only SU-8 photoresist to investigate its masking ability in the various etchants. The other two wafers were transferred to the AFIT thermal oxidation furnace where a dry oxidation process was performed for 8 hrs at 1000 °C. The Filmetrics F20® film thickness measurement tool was used to determine the layer thicknesses as 0.172 and 0.163 μm, respectively. After measurement, a 0.1 μm-thick $Si_3N_4$ layer was deposited by LPCVD at AFRL. These layers are to serve as a hard mask material similar to that reported in the research of Albero, *et al*. [58].

All three wafers were coated with MicroChem SU-8 2025 photoresist using a spin-coating process at 3000 rpm for 30 seconds. The coated wafers were pre-baked using a two-step hot plate process, with an initial temperature of 65°C for 2 minutes, followed by a 5 minute bake at 95°C. The wafers were then exposed using the Karl Suss MJB3 mask aligner and UV lithography system. The system uses an operational wavelength of 365 nm, with a nominal power output of 9.3 $mW/cm^2$. For good exposure characteristics, MicroChem recommends a 365 nm radiation dose of 150-160 $mJ/cm^2$

[65]; corresponding to an 18 second exposure in the MJB3 system. The wafers were post-expose baked on hot plates at 65°C for 1 minute and 95°C for two minutes. This is done to facilitate polymer cross-linking, which is a crucial step in developing negative tone photoresists such as SU-8. Finally, the wafers were developed in a manually agitated bath of SU-8 developer for 5 minutes to remove photoresist from the unexposed areas and clear the etch openings. After developing, the wafers were post baked for 15 minutes at 250°C to enhance SU-8 robustness. Tencor profilometer measurements determined the SU-8 layer thickness to be 17.8±0.2 μm across the wafer surfaces. Because HNA does not attack $Si_3N_4$, the LPCVD $Si_3N_4$ layer had to be removed from the mask openings on the hard masked samples. To accomplish this, a 140 sec RIE etch using 40 sccm $CF_4$ and 3 sccm $O_2$ at 50 mTorr and 100 W RF power was performed in the Trion RIE system. At the conclusion of the patterning process, measurements made with optical microscopy verified the patterns had been transferred into the SU-8 photoresist (and $Si_3N_4$ where applicable) at the desired dimensions.

***SU-8 Masking Only***

Two HNA wet etch trials were conducted on samples masked with only a single layer of SU-8. The first etch trial was conducted at a composition of 20:70:10 H:N:A. In this trial, the formation of small ~100-200 μm gaseous bubbles was accompanied by a yellowish-orange color which began to spread throughout the acid bath. However, after approximately 210 seconds of elapsed etch time, the corner of the SU-8 layer began to visibly separate from the substrate. After 250 seconds, the entire SU-8 layer had peeled off and was seen floating in the bath. At this point the sample was removed for

observation under the optical microscope. The average etch hole diameter was determined with optical microscopy and found to be 444 μm, from an original mask aperture diameter of 334 μm. These results corresponded to a 13.2 μm/min silicon etch rate on the sample before the mask failed.

This result was not entirely unexpected, as many sources indicated that photoresist did not hold up well in the powerful oxidizing environment of the HNA etch system. However, SU-8 is considered to be an extremely robust photoresist, and can be nearly impossible to remove once hard-baked onto a silicon wafer. Therefore, a second trial was conducted at an etch composition of 10:70:20 H:N:A, which should demonstrate a drastically reduced etch rate, according to Robbins and Schwartz's studies. Although the reaction was notably less active, as indicated by reduced bubbling and color change, this experiment failed when the SU-8 peeled away from the wafer between 360 and 430 seconds of immersion time. Based on a 7 minute etch, the average silicon etch rate was calculated to be 9.57 μm/min for the lower concentration acid. The results from these two trials confirmed that photoresist alone, even one as robust as SU-8, would be an insufficient masking material for this application. Therefore, further trials with SU-8 masking alone were not performed, and this method of masking was abandoned.

***$Si_3N_4/SiO_2$ Hard Masking***

As discussed in the sample preparation section, two additional wafers were coated with a thermal oxide and an LPCVD $Si_3N_4$ layer to create a hard masking layer. Two hard-masked samples (patterned with 222 μm-diameter apertures) were selected and etched in the same conditions as the SU-8-only samples previously mentioned. The etch

behavior was observed to be similar to the earlier etches, as the SU-8 layers began to peel at 315 and 390 seconds, respectively. The etches were allowed to progress until each SU-8 layer had been completely separated from the substrate. At this point, the wafers were removed from the HNA and examined under the optical microscope. During this examination, the underlying hard mask layers were found to be severely damaged, as can be seen in Figure 37. The average etch diameter was found to be 390 µm in the 20:70:10 solution and 368 µm in the 10:70:20 solution. These correspond to average silicon etch rates of 16.0 µm/min and 11.2 µm/min, respectively.

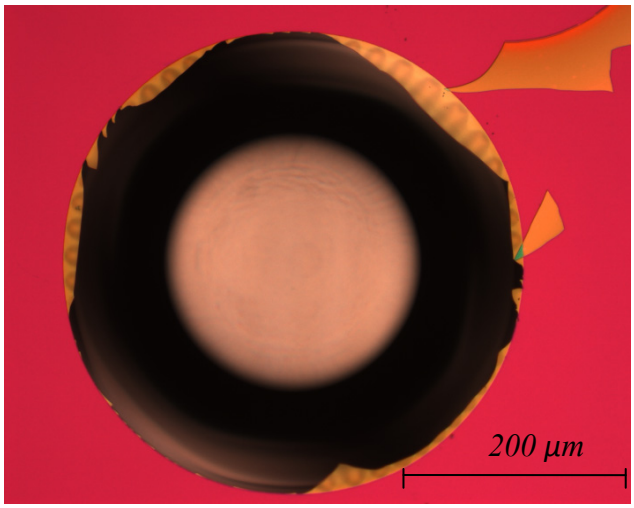


**Figure 37. Optical Microscope Image showing damaged $Si_3N_4/SiO_2$ hard mask layers after SU-8 peel away in 20:70:10 HNA etchant.**

To further investigate these results, a $CF_4$ etch was performed in the Trion RIE to target the $Si_3N_4$ layer. After this etch, the previously colorful mask layers were removed, leaving only small pieces of the $SiO_2$ layers behind. This result is shown in Figure 38.

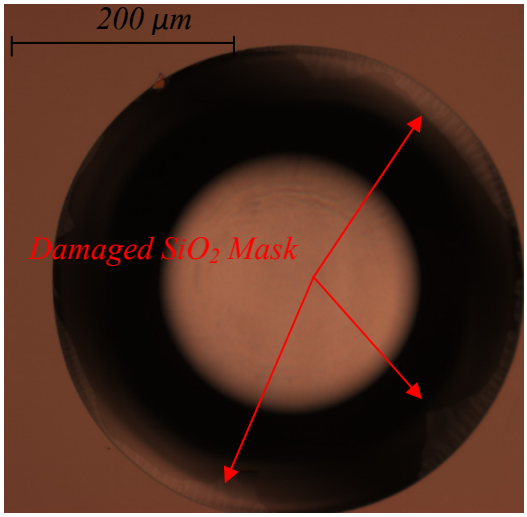


**Figure 38. Optical Microscope Image showing damaged $SiO_2$ hard mask layers after SU-8 peel away in 20:70:10 HNA etchant and RIE removal of $Si_3N_4$.**

After obtaining these results, two new hard-masked samples (patterned with 388 µm-diameter apertures) were dipped in 7:1 buffered oxide etch (BOE) for 2 minutes before HNA etching was initiated. The original intent of this step was to remove the $SiO_2$ layer from the mask openings before beginning HNA etching. However, it was observed that the SU-8 layers lifted off the samples almost instantaneously upon contact with BOE. In this case, however, the $SiO_2/Si_3N_4$ masking layers were observed to be intact, although some slight peeling can be observed around the mask edges, as seen in Figure 39.

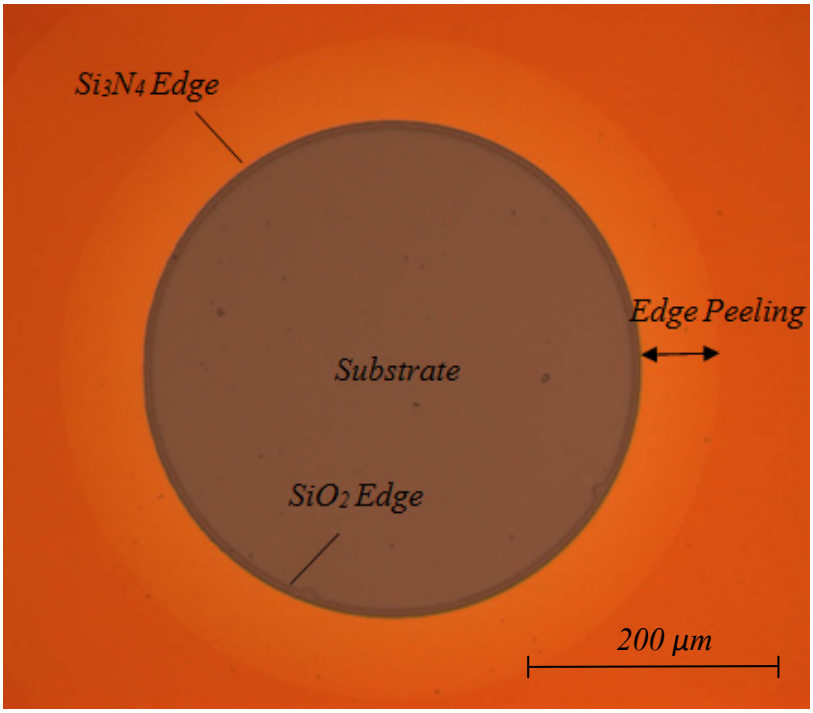


**Figure 39. Hard masked sample after 2 minute 7:1 BOE etch has lifted off SU-8 and cleared $SiO_2$ from mask opening.**

The increased survivability of the hard mask layers in BOE is most likely due to the support of the silicon substrate. In HNA, the SU-8 peeling was initiated around the sample edges, with the photoresist layer curling towards the center of the sample due to residual stress. By this time, the hard mask layers had already been undercut significantly, allowing undercut areas of the hard mask layers to be torn from the substrate by the highly stressed SU-8. Alternatively, the BOE etch did not attack the silicon substrate before the SU-8 was lifted away, leaving the hard mask layers sufficiently supported by the silicon substrate to improve survivability.

Despite this improvement, the results of the subsequent etches did not show marked improvement over the earlier etches. Each etch was conducted in 1 minute

intervals, with optical microscope observations and profilometer measurements made at each stop. The hard masking layers were stripped from the sample in 20:70:10 HNA before the 2 minute mark was reached, having etched only 18.8 μm laterally and 16.1 μm vertically. In 10:70:20 HNA, the hard masking layers were stripped before the 3 minute etch stop. At that point, the silicon etch had proceeded 14.4 μm laterally and 18.5 μm vertically. The average silicon etch rates in these trials were lower than those observed previously, most likely due to the 1 minute etch intervals, which helped to mitigate any temperature effects on the etch.

***HNA Etching Process with Ultrasonics***

The final attempt to use HNA etching involved the addition of ultrasonic agitation. The previous trials had not been performed with agitation, although literature certainly suggested its importance. This trial was conducted on a hard-masked sample at 10:70:20 H:N:A composition. The results of this experiment are best described as disastrous, as the reaction quickly gained energy and the temperature of the water bath surrounding the acid beaker heated from 21°C to at least 48°C. More importantly, the small bubbles and orange-yellow coloring were replaced by excessive bubbling and thick plumes of dark orange to brownish smoke. Before the silicon sample could be removed from the acid bath, the etch had progressed all the way through the thickness of the wafer. In its final state, the wafer had been thinned considerably, and a pattern of large circular windows had been patterned across a very rough silicon surface.

A partial explanation for this effect can be found in Robbins and Schwartz's work, where the HNA system's reliance on temperature is described [27]. This relationship was charted earlier in Figure 11, which shows a pronounced increase in etch

rate with increased temperatures. As temperature increases, the equilibrium of $NO_2$ and $N_2O_4$ (which are formed during the dissociation of $HNO_3$) shifts towards $NO_2$, promoting more rapid oxidation of the silicon surface and the appearance of a brownish yellow color. According to the Australian National University, the brown vapor observed in this experiment is most likely excess $NO_2$ gas leaving the solution. [66].

Given the unpredictable nature of the HNA etch and the difficulties experienced in producing an effective mask layer, compounded with the grievous safety concerns of dealing with such volatile and toxic chemicals, it was decided that wet HNA etching was not the best choice of methods to produce the hemispherical etch cavities needed for this work.

**Reactive Ion Etching**

As discussed in Chapter 3, the primary concern with the Trion RIE system was that a bulk etch requiring a final etch depth of 500 μm would simply take far too long. This was based on previous AFIT researchers only achieving bulk silicon etch rates of 2.0 to 3.5 μm/min. However, these etch rates were observed when operating the Trion RIE with 200-250 W of RF power. Without being able to increase the $SF_6$ flow rates, the best method to increase the etch rate is to increase RF power. The Trion RIE system is capable of generating up to 600 W RF power. Therefore, three etches were performed at RIE powers of 600 W, 300 W, and 200 W, respectively. The $SF_6$ and $O_2$ flow rates were held constant at 52 sccm (system maximum) and 5 sccm, respectively. Chamber pressure was held at a relatively high 300 mTorr to promote an isotropic etch profile.

Three hard-masked etch samples were chosen for these experiments, each with 444 µm-diameter apertures patterned in an SU-8 masking layer. The standard $Si_3N_4$ RIE etch and a 2 min BOE etch were used to clear aperture openings of hard mask layers. Samples were etched in 30 minute intervals, allowing etch progression to be monitored with optical microscopy and profilometer measurements.

At 600 W RF power the SU-8 and hard mask layers were stripped entirely in less than 30 minutes. Final cavity diameters were an average of 675 µm, with an average depth of 48.7 µm. This corresponds to a lateral etch rate of 3.85 µm/min and a vertical etch rate of 1.62 µm/min over a 30 minute period. An optical image of a representative cavity from this trial is shown in Figure 40.

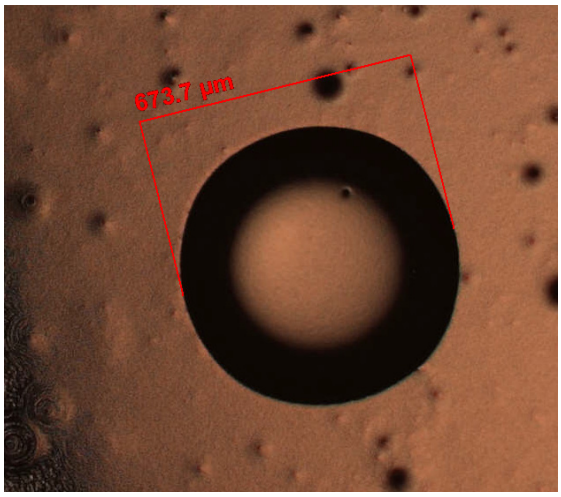


**Figure 40. Representative cavity from 600 W $SF_6$-$O_2$ RIE trial. Original mask aperture was 444 µm, although it was removed during the RIE process. Cavity depth is 48.7 µm.**

At 300 W RIE power the SU-8 and hard mask layers were removed between the 30 and 60 minute etch stops. Final cavity diameters were an average of 640 µm, with an average depth of 80 µm. This corresponds to a lateral etch rate of 1.63 µm/min and a vertical etch rate of 1.33 µm/min over a 60 minute period.

A final trial was conducted at 200 W RIE power; in this trial the SU-8 masking layer survived 90 minutes of etching without any visible effects. At each measurement interval, the etch had progressed 16, 30.5, and 50.5 µm laterally, and 44, 65, and 84 µm vertically. Therefore, the average etch rates were only 0.56 µm/min laterally and 0.93 µm/min vertically. A series of photographs showing the etch progression on a representative cavity from this trial is shown in Figure 41.

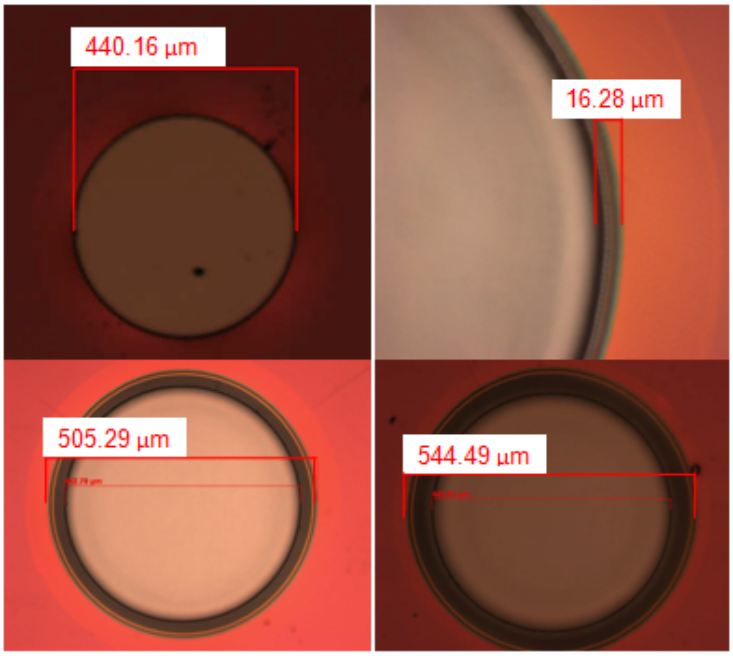


**Figure 41. Upper left: Original mask opening. Upper right: 30 minute etch progression. Lower left: 60 minute etch progression. Lower Right: 90 minute etch progression.**

The etch rates exhibited in this study were extremely low for a bulk etching application attempting to etch several hundred microns. However, SU-8 masking layers were unable to withstand the higher RIE powers which would lead to increased etch rates. Therefore, another method of plasma etching was explored.

**DSE Parameter Studies**

The AFIT/AFRL owned Plasma-Therm DSE system allows for precise variation of etch parameters. Additionally, its ICP technology and wafer cooling allows for lower temperatures at the wafer surface, increasing the survivability of photoresists such as SU-8. Although the system is designed to create deep anisotropic profiles, an investigation was made into its ability to perform isotropic etches at a high rate. In order to determine the appropriate settings for such an etch, a parameter study on ICP power, $SF_6$ flow rate, RF bias, and chamber pressure was performed. Etches were conducted on 12 samples at 12 different system settings, with each etch lasting 20 minutes.

Table 1 shows the selected parameters for each test run, as well as key results. The highlighted green cells represent the best result in each category of concern with regards to etch progression.

**Table 1. DSE Parameter Study Trial Runs and Results**

| Sample | ICP Power (W) | $SF_6$ Flow Rate (sccm) | RF Bias (V) | Chamber Pressure (mTorr) | V/L Etch Ratio | $R_{min}/R_{max}$ | Vert. Etch Rate (μm/min) |
|---|---|---|---|---|---|---|---|
| 1 | 1250 | 300 | 200 | 60 | 0.7631 | 0.9795 | 10.68 |
| 2 | 1250 | 200 | 200 | 60 | 0.7527 | 0.9761 | 10.12 |
| 3 | 1250 | 100 | 200 | 60 | .07535 | 0.9562 | 9.55 |
| 4 | 1250 | 250 | 10 | 60 | 0.7284 | 0.9610 | 9.97 |
| 5 | 1250 | 250 | 80 | 60 | 0.7489 | 0.9558 | 10.69 |
| 6 | 1250 | 250 | 150 | 60 | 0.7889 | 0.9594 | 10.84 |
| 7 | 2500 | 250 | 200 | 60 | 0.5656 | 0.9898 | 7.98 |
| 8 | 1700 | 250 | 200 | 60 | 0.6717 | 0.9893 | 9.53 |
| 9 | 1000 | 250 | 200 | 60 | 0.4519 | 0.9960 | 5.31 |
| 10 | 1700 | 300 | 200 | 60 | 0.8075 | 0.9620 | 11.18 |
| 11 | 1700 | 300 | 200 | 100 | 0.8676 | 0.9505 | 12.32 |
| 12 | 1700 | 300 | 200 | 80 | 0.8404 | 0.9429 | 11.85 |

Figure 42 provides a graphical depiction of the results of the DSE parameter studies.

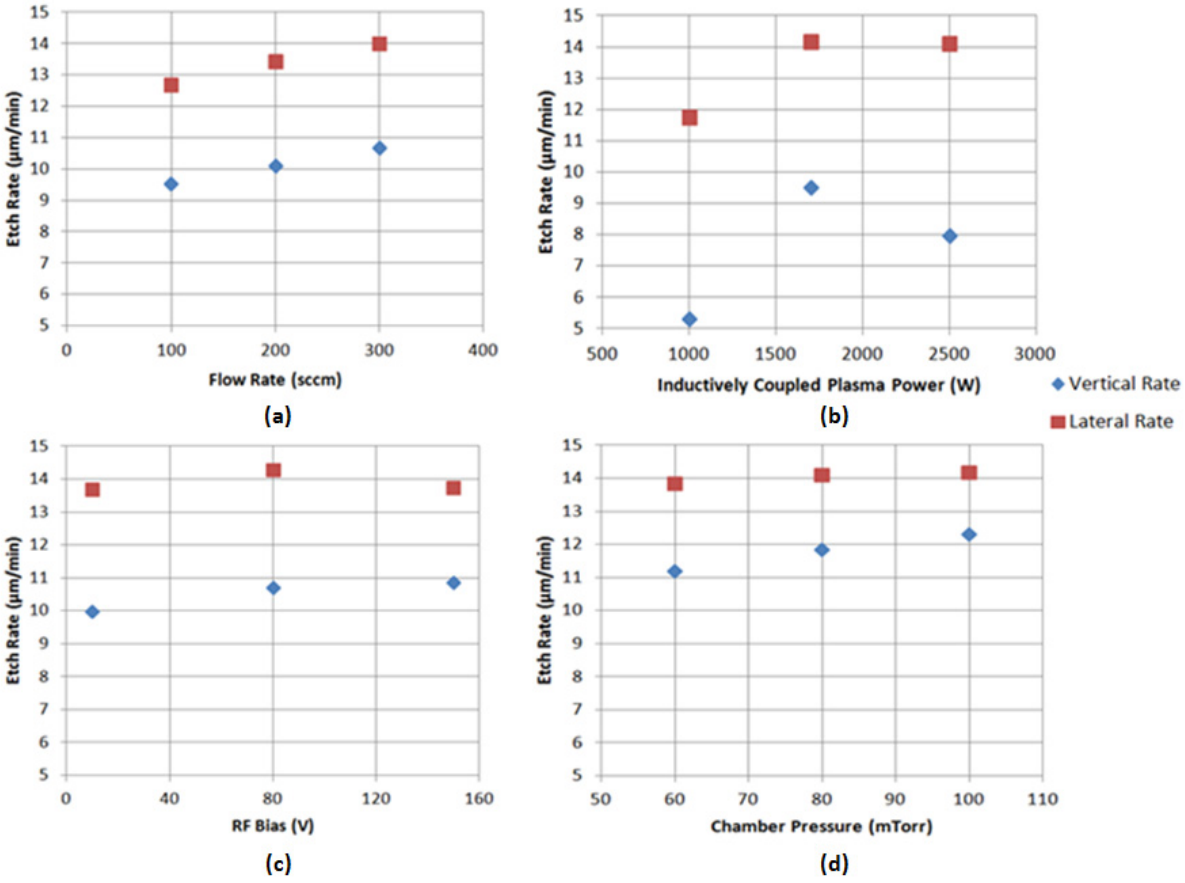


**Figure 42. a) Dependence of silicon etch rate on $SF_6$ flow rate in the DSE system. The V/L etch ratio is almost unchanged with increasing flow rates, although overall etch rates increase linearly with increased flow rate. b) Effect of ICP Power on Si etch rate in DSE. The V/L ratio is highest at 1700 W, as are the overall etch rates. c) Impact of varying RF Bias on Si etch rate in DSE system. V/L etch rate seems to improve with increased bias, although overall etch rate appears to suffer. d) Effect of chamber pressure on otherwise optimized Si etch in DSE system. Increasing pressure improves V/L etch ratio as well as overall etch rates.**

Analyzing Table 1 and Figure 42, both V/L etch ratio and overall etch rates appear to depend on process parameters, although $R_{min}/R_{max}$, which is used to measure anisotropy, does not appear to be strongly correlated to any DSE parameter. From the presented data, it can be seen that Sample 11's parameters represent the best mix for a highly isotropic etch without exceeding the DSE system's specified operating limits.

With the system parameters determined, the fabrication variables of time and mask opening were varied and investigated. The key finding from this study was the relationship between mask opening diameter and final cavity diameter. To achieve an optimal isotropic etch with a vertical/lateral etch ratio of 1.0, it was found that the mask opening should be 1/2.3 or 43.5% of the final desired hemisphere diameter, as shown in Figure 43. Therefore, to produce 1 mm diameter spheroidal packages, the mask should be patterned with 435 μm apertures.

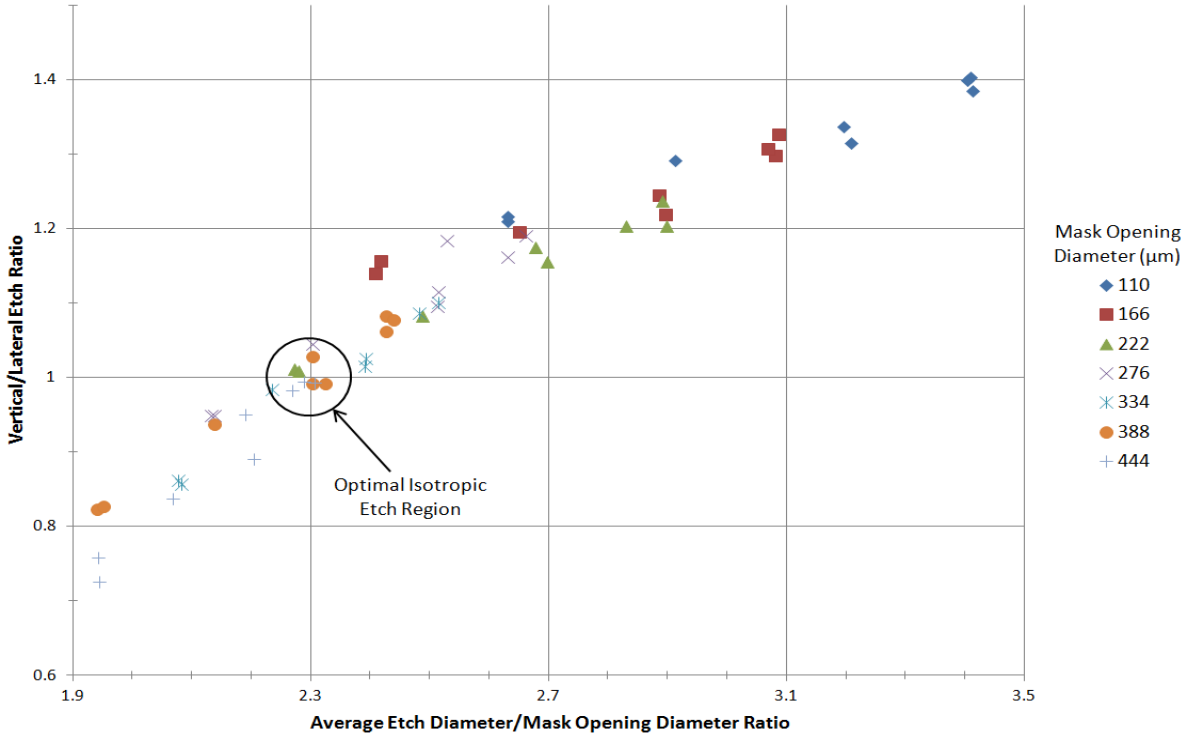


**Figure 43. V/L etch ratios as a function of etch progress in $SF_6$ DSE process with various mask apertures. A V/L etch ratio of approximately 1 (which indicates isotropy) is achieved when the average etch diameter is approximately 2.3x the original mask aperture.**

The results of these studies demonstrate that the DSE machine is a highly viable option for producing large isotropic etches in silicon. The observed etch rates are approximately 10x higher than those produced with similar chemistries in a parallel plate RIE system. Furthermore, the reduced process temperatures facilitate masking with SU-8 alone, which greatly reduces processing time and complexity. Finally, greater control of system parameters allows the researcher to make small changes to the etch process and effectively fine tune the expected results. However, there are some observable drawbacks of the $SF_6$-based plasma etch used in the DSE process. First, the etch leaves the silicon with a surface roughness between 1 and 3 μm, which is higher than desired. Secondly, the area of undercutting is observed to extend up to 50 μm beyond the cavity lip in some cases. Also, these etches clearly demonstrate an increased level of preferential etching based on the crystalline planes in silicon, as opposed to wet isotropic etching in HNA. Finally, the etch performance across the sample surface varies slightly, leading to minor variances from cavity to cavity. In the following research, HNA polishing is employed as an attempt to reduce the surface roughness and undercutting left by the DSE process. Additionally, MatLab image processing will be employed to analyze the differences in anisotropy and the cavity variance across samples.

**MatLab Analysis**

In order to characterize the differences in anisotropy observed in etches performed on <100> and <111>-oriented Si wafers, a MatLab image processing code was developed. Samples from each wafer type were imaged after DSE completion using the optical microscope. The MatLab program provided details of the geometry of the cavities

at the wafer surface. Two commonly used descriptors for circular shapes are eccentricity and circularity. However, these failed to adequately describe the observed shapes, so a third descriptor, $R_{min}/R_{max}$, which had been used previously in the DSE study, was calculated to supplement these descriptors.

From this study, a few noticeable trends emerged. First, the final dimensions of cavities formed by DSE on <100>-oriented Si wafers demonstrated less variance across a sample surface. The DSE-produced cavity profiles from a <100>-oriented Si sample and those from a <111>-oriented Si sample are compared in Figure 44. In these images, the impact of the four-fold rotational symmetry of the <100>-oriented Si and six-fold symmetry of the <111>-oriented Si is clearly demonstrated. Figure 45 plots the maximum and minimum radii of each cavity, along with their corresponding centroids. In addition to the greater size variance found in the <111>-oriented Si samples, the centroids of these cavities are also less consistent.

The MatLab code makes all measurements and generates all plots in terms of pixels; however, from the optical microscope resolution and scaling settings the length of a pixel can be determined to be 0.712 μm. This number can be used to determine cavity dimensions in microns, if desired. The average values of key cavity measurements from both samples are provided in Table 2.

**Table 2. Average values of various cavity measurements in <100> and <111>-oriented Si after DSE process.**

| Crystal Orientation | Cavity Area | Perimeter | Equiv. Diameter | $R_{min}/R_{max}$ | Circularity | Eccentricity |
|---|---|---|---|---|---|---|
| <100> | 0.197 $mm^2$ | 1.65 mm | 0.501 mm | 0.9430 | 1.1027 | 0.0634 |
| <111> | 0.173 $mm^2$ | 1.56 mm | 0.470 mm | 0.9344 | 1.1196 | 0.1105 |

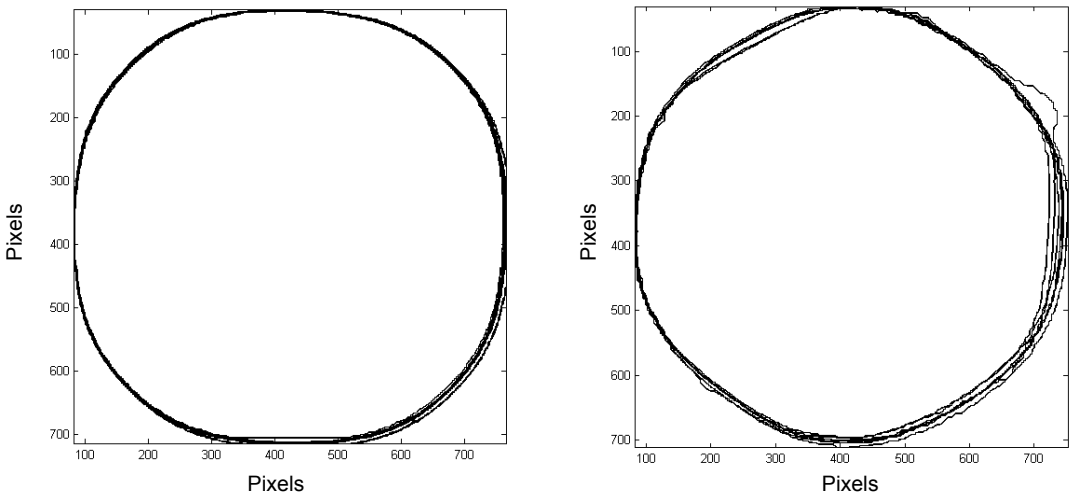


**Figure 44. Left: 28 DSE-produced cavity profiles from a <100>-oriented Si sample are overlaid, demonstrating four-fold rotational symmetry and limited variance in profile size. Right: 8 DSE-produced cavity profiles from a <111>-oriented Si sample are overlaid, demonstrating six-fold rotational symmetry and increased variance in profile size and shape.**

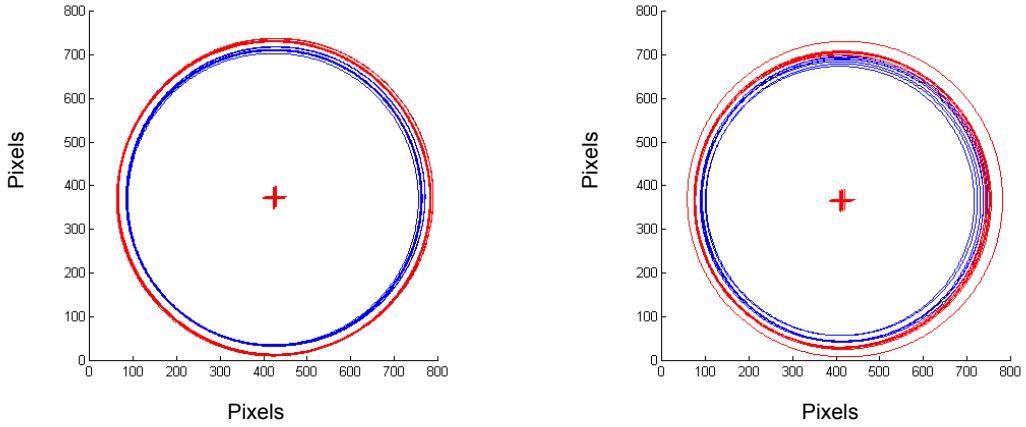


**Figure 45. Left: Minimum (blue) and maximum (red) radii of DSE-produced cavities in a <100>-oriented Si sample are overlaid; the tight grouping corresponds to a consistent cavity profile. Right: Minimum and maximum radii of DSE-produced cavities in a <111>-oriented Si sample are overlaid; the variance between individual cavity shapes is illustrated in the broadened rings.**

From the numerical results alone, it would be tough to draw a conclusion as to which crystal orientation produced a more circular etch profile. MatLab analysis will be used again in the following section to characterize the results of HNA polishing.

**HNA Polishing**

As discussed previously, HNA can be used as a polishing etch at high $HNO_3$ and low HF concentrations. A 10:80:10 H:N:A solution was prepared in a PTFE beaker for use in the following study. Samples from the DSE studies were stripped of masking layers and cleaved so that a row of cavities was bisected, revealing their cross-sections. Figure 46 shows the cross-section of a cleaved etch cavity after DSE cavity formation and prior to HNA polishing steps. The wafers are withdrawn from the solution at 1 minute, 3 minutes, 6 minutes, and 10 minutes total etch time to observe and measure etch progress. An optical microscope was used to photograph and measure the cross-sections at each time step. Figure 47 shows the cross-section of the same cavity pictured in Figure 46 after 10 minutes of HNA polishing.

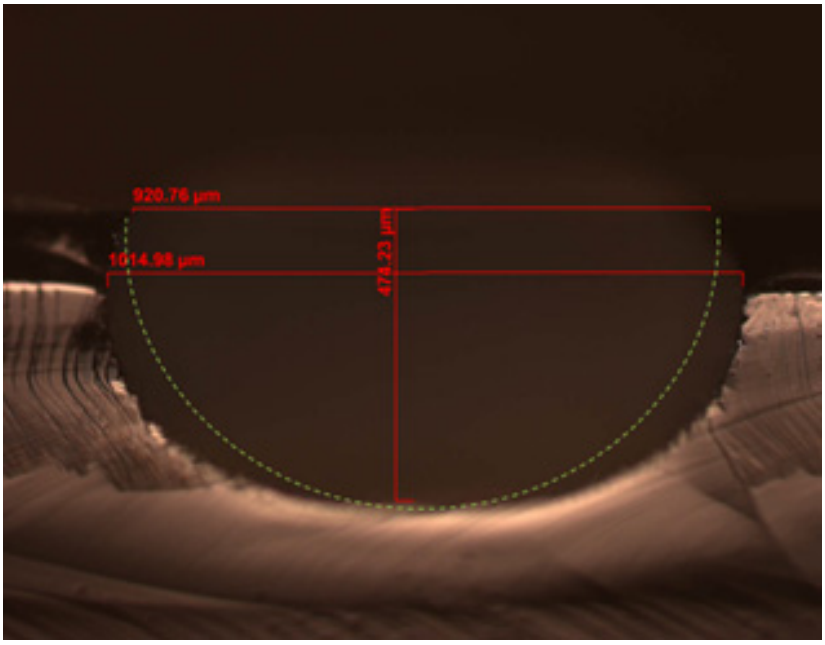


**Figure 46. Cross-section of DSE-produced cavity taken by optical microscope before HNA polishing. The green line represents an ideal hemispherical profile.**

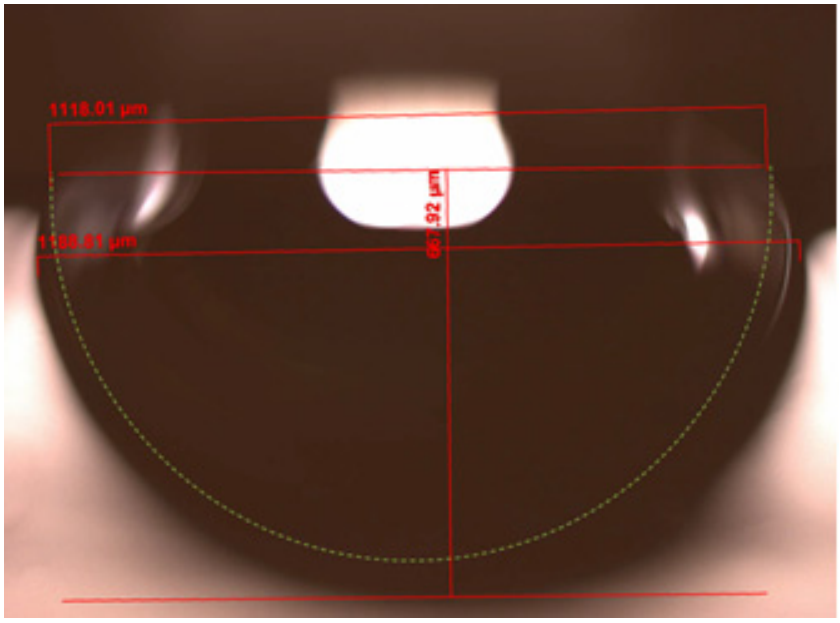


**Figure 47. Cross-section of DSE-produced cavity after 10 minutes of 10:80:10 HNA polishing. The green line represents an ideal hemispherical profile. Bright reflections of the smoother silicon surfaces make imaging by optical microscope much more difficult.**

The first sample chosen for measurement contained an array of etch cavities which had been etched by DSE for 60 minutes with 1700 W ICP power, 300 sccm $SF_6$ flow rate, 200 V RF Bias, and a chamber pressure of 100 mTorr. Masking had been performed by SU-8 patterned with 388 μm-diameter apertures. After cleaving, eight cavity cross-sections were visible for observation under the optical microscope. The average measurements for each etch step are shown in Table 3. It can be seen that undercutting is reduced as the etch progresses, although it does not appear to be completely eliminated. Furthermore, the etch is much more aggressive than anticipated, with etch rates increasing as the continuous time in the solution is increased.

**Table 3. Average cavity measurements from HNA polishing sample.**

| Etch Time (min) | Surface Dia. (μm) | Max. Dia. (μm) | Undercut | Depth (μm) |
|---|---|---|---|---|
| 0 | 930.4 | 990.5 | 6.5% | 463.5 |
| 1 | 946.5 | 1008.5 | 6.6% | 474.2 |
| 3 | 974.3 | 1037.5 | 6.5% | 516.1 |
| 6 | 1036.2 | 1095.2 | 5.7% | 584.7 |
| 10 | 1143.1 | 1190.3 | 4.0% | 685.9 |

After 10 minutes of etching, the sample was cleaved through its middle to determine if the interior cavity profiles were different than those on the edges. Somewhat surprisingly, these cavities exhibited no residual undercutting. Rather, the cavities were observed to exhibit the rounded cavity lips which had been originally desired. An example is shown in Figure 48.


**Figure 48. Cross-sectional profiles of two DSE-produced etch cavities after 10 minutes of 10:80:10 HNA polishing. The green lines represent ideal hemispherical profiles. The cavity lips near the center of the sample have achieved the desired rounded profile.**

A Zygo® white light interferometer was also used to determine the impact of HNA polishing on surface roughness. Under an optical microscope, qualitative observations suggested that surface roughness was greatly reduced, however it is impossible to determine the exact extent of this improvement. Using IFM allowed more detailed measurements to be made. Representative IFM measurements taken before and after HNA polishing are shown in Figure 49 and Figure 50. The surface roughness within the DSE cavity was found to be on the order of 0.1-0.2 μm, which was reduced below 10 nm across the observable surface after HNA polishing.

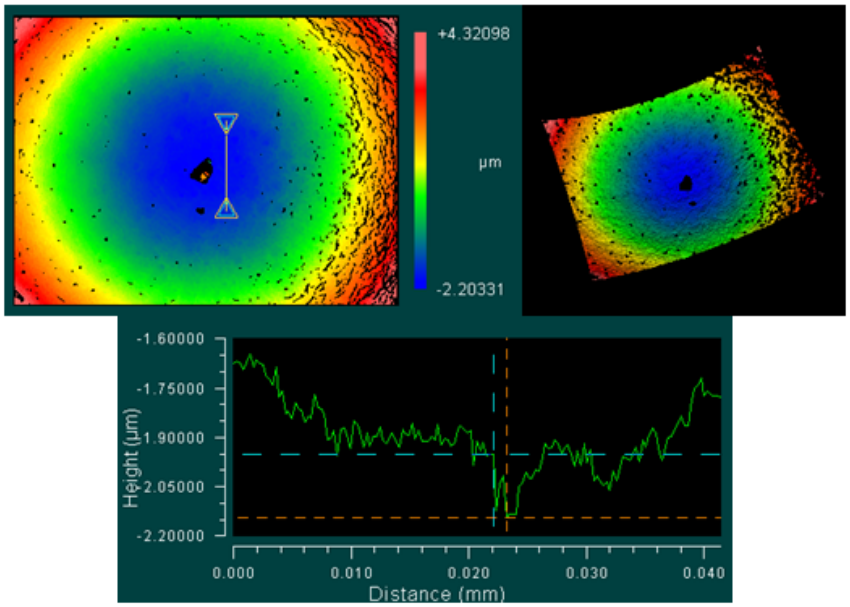


**Figure 49. Zygo® IFM results of DSE cavity prior to HNA polishing. The maximum surface roughness is measured to be ~0.2 µm at the bottom of this representative cavity.**

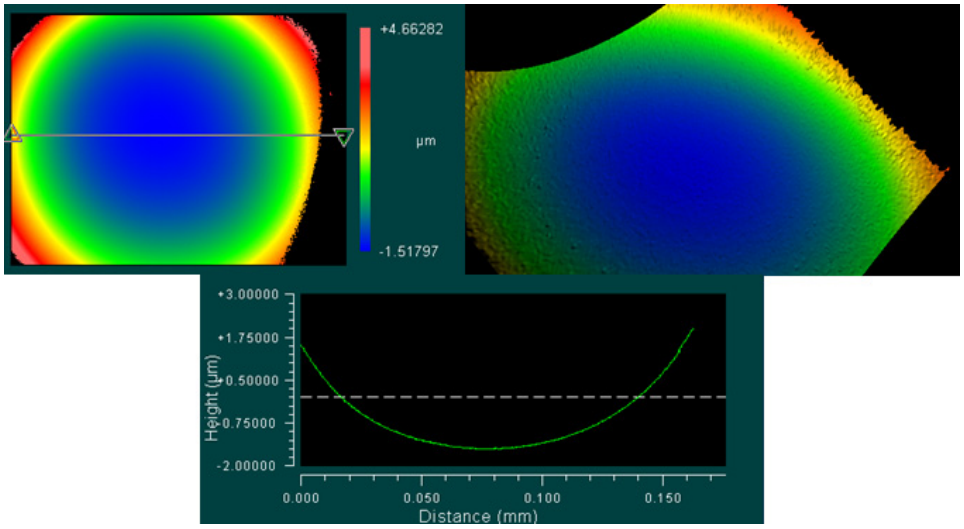


**Figure 50. Zygo® IFM results of hemispherical cavity after 10 minutes HNA polishing. The maximum surface roughness is below 10 nm across the bottom of this representative cavity.**

Another sample, which had been patterned with 80 µm x 80 µm gold alignment marks, was etched for only 75 seconds in 10:80:10 HNA. The gold alignment marks were removed from the sample during the HNA etch, although their profiles remained as 1-5

µm bumps on the otherwise flat silicon surface. The silicon surface was further analyzed under IFM to obtain a more detailed surface profile. These images revealed that the cavity lips had indeed been rounded off, but the extent of rounding varied around the perimeter of each cavity. Furthermore, the polishing tended to create ~1.5 µm-deep valleys between adjacent cavities. These effects are shown in Figure 51 and Figure 52.

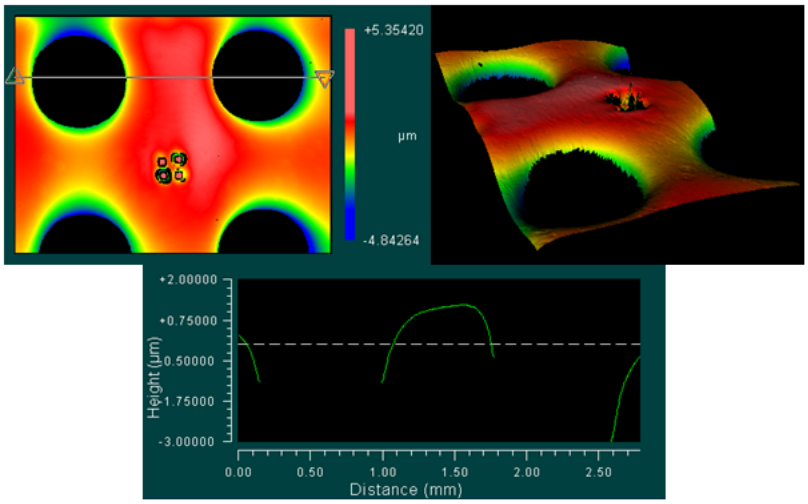


**Figure 51. Zygo® IFM results of hemispherical cavity after 75 seconds HNA polishing. The extent of rounding on the cavity lip varies with position around the diameter.**

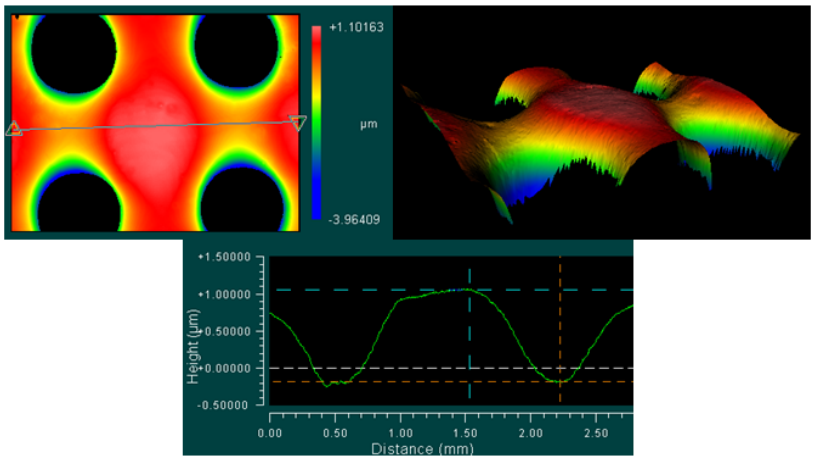


**Figure 52. Zygo® IFM results of hemispherical cavity after 75 seconds HNA polishing. A valley formed between adjacent cavities is measured to be approximately 1.2 µm-deep.**

Finally, MatLab image analysis was applied to evaluate the effects of HNA polishing on cavities etched in differently oriented wafers. All the previous HNA polishing trials had been performed on <111>-oriented Si samples. The final sample (which formerly contained gold alignment marks) was imaged over its entire surface using the optical microscope. The previously-examined <100>-oriented Si sample was etched in a new 10:80:10 HNA mixture for 75 seconds, before being imaged again to determine the HNA's effect. Figure 53 provides a comparison of cavity profiles by overlaying the cavity boundaries as we had previously. Figure 54 provides information on the maximum and minimum radii of these etch cavities and the relative locations of their centroids.

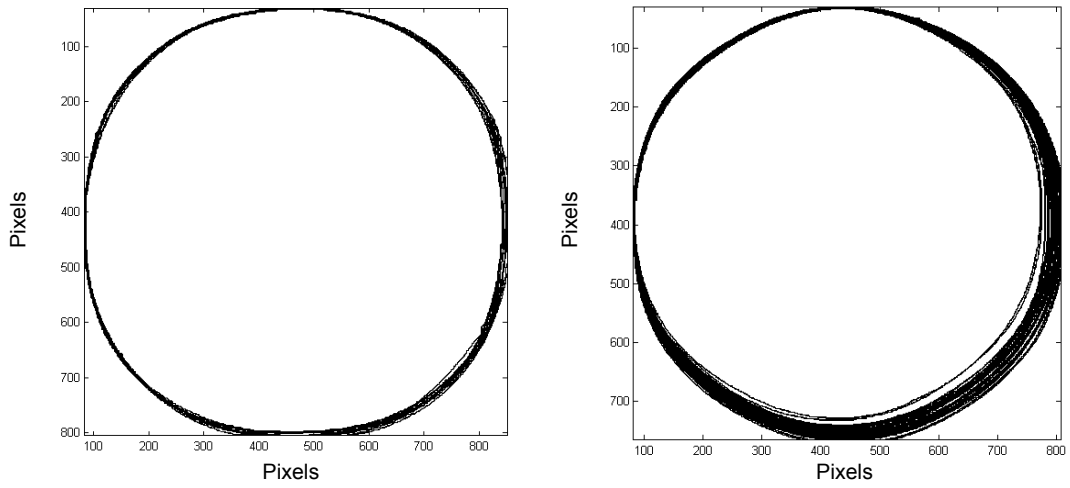


**Figure 53. A comparison of cavity shapes in <100>-oriented Si (Left) and <111>-oriented Si (Right) after polishing for 75 seconds in 10:80:10 HNA. The anisotropy in the <111>-oriented Si sample is greatly reduced by the HNA polish, although size variances are still persistent.**

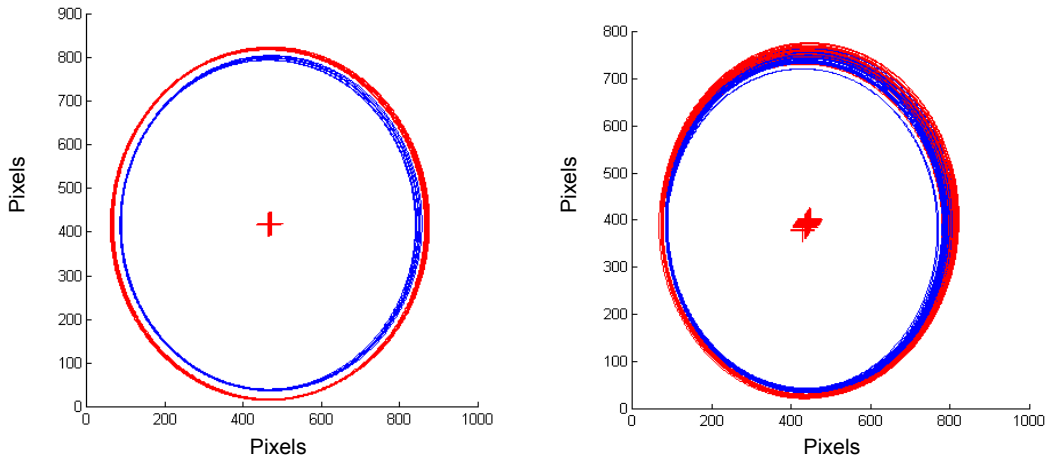


**Figure 54. A comparison of minimum (red) and maximum (blue) radii in <100>-oriented Si (Left) and <111>-oriented Si (Right) after polishing for 75 seconds in 10:80:10 HNA. The HNA polishing step only exaggerates any size and location variances originally created with the DSE process.**

The results of this trial matched expectations, as the hexagonal geometries of the <111>-oriented Si samples had a much more pronounced response to HNA polishing than the rectangular cavities in the <100>-oriented Si sample. A qualitative visual assessment must be used in conjunction with the data presented in Table 4. in order to make this determination, however, as only $R_{min}/R_{max}$ appears to agree with intuition. Using only circularity or eccentricity to determine the most circular etch holes, one would think the original <100>-oriented Si cavities were the most circular of those tested.

**Table 4. Average measurements of bulk isotropic cavity etches calculated with MatLab Image processing programs.**

| Sample | Equiv. Diameter | $R_{min}/R_{max}$ | Circularity | Eccentricity |
|---|---|---|---|---|
| <100> Before HNA | 500.9 ± 1.4976 µm | 0.9430 ± 0.0041 | 1.1027 ± 0.0009 | 0.0634 ± 0.0199 |
| <100> After HNA | 560.3 ± 2.5974 µm | 0.9434 ± 0.0060 | 1.1073 ± 0.0026 | 0.1475 ± 0.0298 |
| <111> Before HNA | 469.9 ± 3.8975 µm | 0.9344 ± 0.0169 | 1.1196 ± 0.0044 | 0.1105 ± 0.0388 |
| <111> After HNA | 514.5 ± 6.8766 µm | 0.9696 ± 0.0051 | 1.1092 ± 0.0012 | 0.1235 ± 0.0270 |

The results of these studies demonstrate that HNA can be used to effectively polish the cavity surfaces and simultaneously provide the rounded edges desired for easier photoresist patterning. While the chosen 10:80:10 HNA solution acted much more rapidly than suggested in previous literature, it can be regulated by breaking up the total etch time into shorter intervals. This practice combats the effects of rising temperatures on etch progression. Additionally, the HNA polishing step was observed to reduce to some extent the anisotropy originally present in the DSE cavities. There were, however, a few areas of concern after these studies. First, the cavity lip profiles show various degrees of rounding after the HNA polishing. A more uniform result would be certainly be desirable. Coupled with this variance is the formation of shallow valleys between etch cavities, which could cause significant problems with bonding attempts in the future. However, increased separation between cavities may be able to reduce the severity of these occurrences. Another possible remedy for this problem would be the application of a short chemical mechanical polishing (CMP) step, designed to remove approximately the top 2 μm of the wafer and leave a smooth, planar surface behind.

**Photoresist Deposition and Patterning**

In order to fabricate the desired packages, photolithography must be accomplished over the severe topography created by the bulk micromachining steps. A few of the photoresists available in the AFIT cleanroom were deposited using conventional spin-coating methods. The coating qualities were observed using optical

microscopy, with key results provided. Figure 55 shows a number of problems which were observed in using S1805 photoresist. First, the low-viscosity resist pulls back from sharp edges, leaving a 5-20 μm ring around the cavity lip uncoated by photoresist. This also creates a thicker, 5-7 μm-thick, "bead" of photoresist which forms further away from the cavity lip. Finally, the resist pools in the bottoms of the etched cavities, with thicknesses up to 10 μm observed on cleaved samples. These variations in thickness are fairly extreme compared to the average thickness of 0.5 μm on large planar areas of the wafer surface.

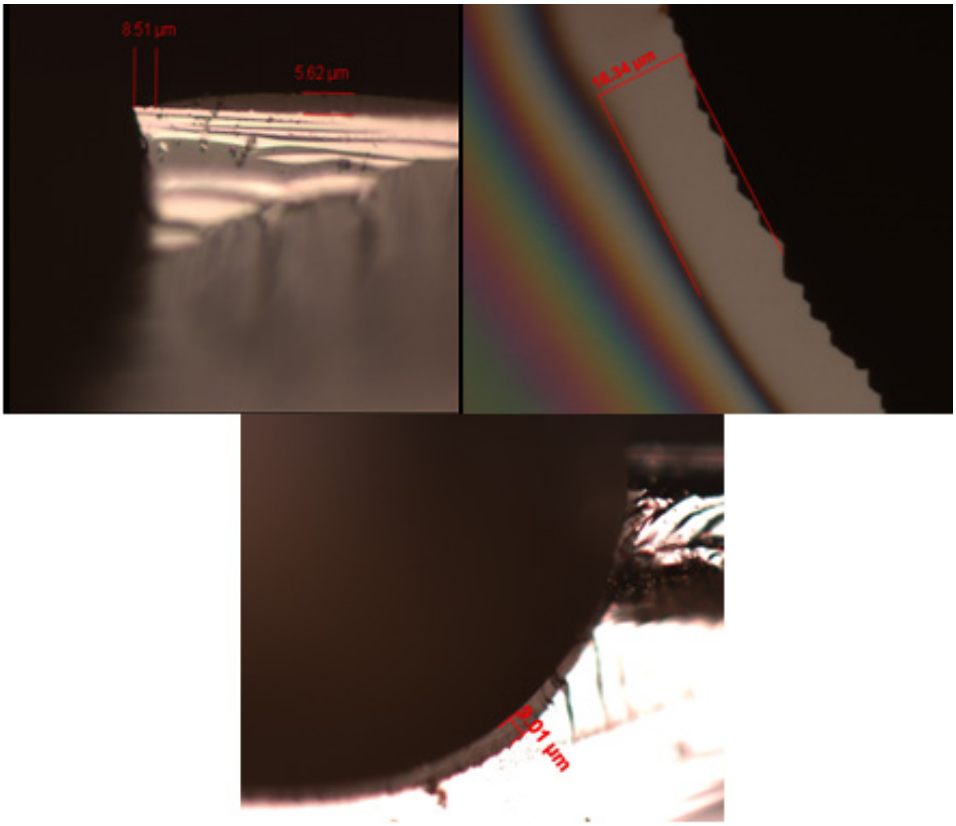


**Figure 55. Three problems with S1805 photoresist are shown. Top Left: A cross-sectional view of a representative cavity lip shows the photoresist pulling away from the cavity edge and forming a thick bead. Top Right: A top view of the cavity lip showing a more severe case of photoresist pull back. Bottom: A cross-sectional view shows the pooling of photoresist at the cavity bottom.**

After noting these problems with the S1805 photoresist, the more viscous S1818 photoresist was chosen for evaluation. As anticipated, the edge pull back problem was reduced, however the S1818 exhibited a severe pooling problem. Photoresist thickness within the cavities varied between 10 µm and 40 µm, while surface thickness was measured between 1.1 and 2.5 µm. Figure 56 shows an example of S1818 pooling.

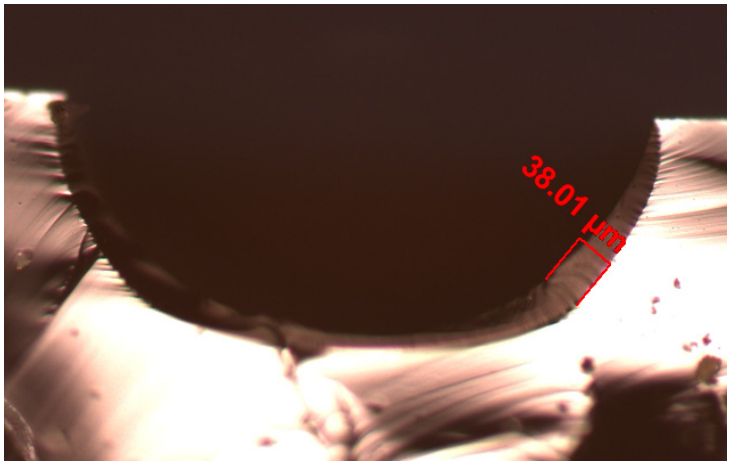


**Figure 56. Cross-sectional image detailing pronounced pooling effect of S1818 photoresist in DSE-produced hemispherical cavities.**

The final resist chosen for evaluation was MicroChem's polydimethylgutarimide (PMGI) photoresist SF11. This photoresist is a popular choice for sacrificial layers and as the undercut layer in bi-layer lift-off processing. Therefore, obtaining good results with SF11 would facilitate the patterning of metal traces inside the etched cavities. Overall, SF11 performed much better than either S1800 series photoresist. The coatings produced were generally conformal to the etched cavity, and edge pull back was not observed. However, the photoresist coating is still considerably thicker inside the etched cavities, at approximately 4-8 µm, than the ~1 µm coating at the wafer surface. Figure 57 shows the conformal coating at the bottom and along the sides of an etched cavity.

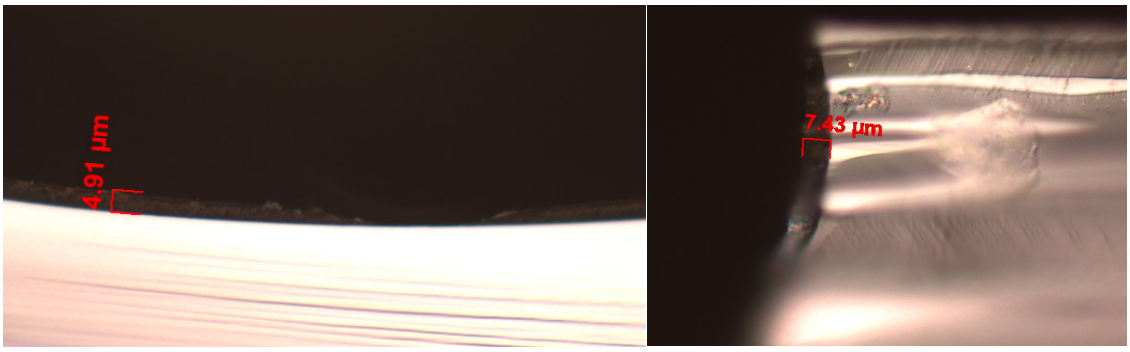


**Figure 57. SF-11 coverage of a DSE-produced etch cavity. The pooling and edge pull-back phenomena are not observable, although the photoresist inside the cavity is still considerably thicker than that deposited across the planar wafer surface.**

In an attempt to further characterize the suitability of SF-11 for the 3D photolithography needed in this application, a simple lift-off process test was conducted. A bi-layer photoresist lift-off stack was patterned over DSE-produced cavities in a <111>-oriented Si wafer sample. The cavities chosen for this experiment had an average depth of ~503 µm, in order to best represent the dimensions of the final hemisphere diameter. First, SF-11 was deposited using a standard 3000 rpm, 30 second spin cycle, followed by a 5 minute hot plate bake at 270 °C. Next, a layer of S1805 photoresist was deposited, again using a 3000 rpm 30 second spin cycle, with a 2 minute, 110 °C hot plate bake. The S1805 was exposed with a simple pattern of small circles in the MJB3 system. Because the thickness of the S1805 was unknown, and overexposure did not pose any problem, this exposure was conducted for 30 seconds to ensure completion. The S1805 was developed using a 1:5 solution of 351:DI water while spinning at 500 rpm. As with the exposure time, the standard developer cycle was lengthened from 45 seconds to 2 minutes to ensure all unexposed S1805 had been removed from the sample. An optical inspection ensured the 1805 had been accurately patterned before proceeding. Finally, the SF-11 was exposed using the Deep-UV system in 200 second increments. Each exposure

and subsequent 60 second development step in SAL 101 developer is designed to remove approximately 1.5 μm of SF-11. Based on the results from the earlier analysis, this process was repeated 4 times to assure SF-11 in the cavity had been properly exposed and developed. Using optical measurements, circular patterns of SF-11 could be seen within the cavities and across the wafer surface, as shown in Figure 58.

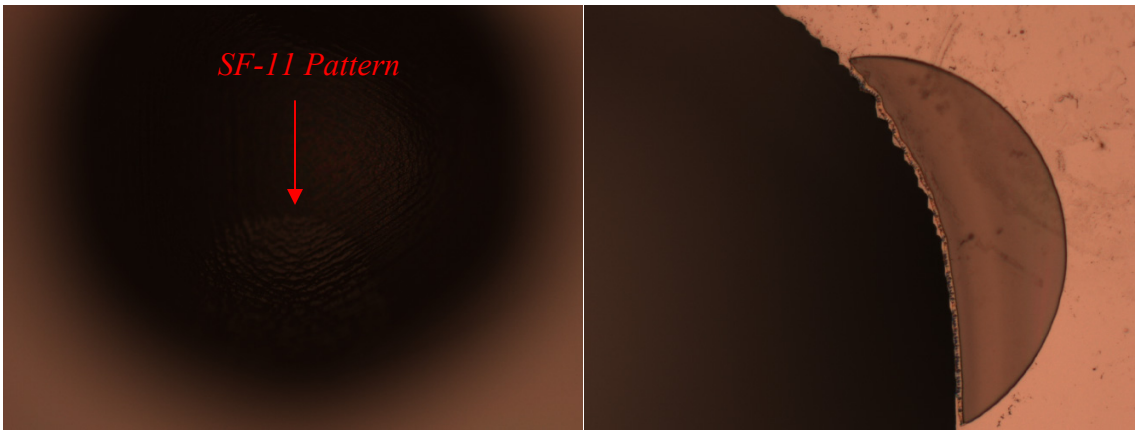


**Figure 58. (Left) SF-11 patterned within a 500 μm-deep hemispherical cavity; by focusing on the cavity bottom the wafer surface is blurred. (Right) SF-11 patterned at the surface of a similar cavity. Note the photoresist at the surface has pulled back from the cavity edge as observed previously.**

After the patterns had been transferred to the photoresist layers, a 100Å/1000Å Ti/Au layer was evaporated onto the sample. Lift-off was attempted using a bath of Remover PG heated to 70 °C. Despite over two hours in the heated bath and the addition of a 30 minute ultrasonic agitation period, the lift-off within the cavities did not occur reliably. The optical microscope was used to observe the success of the lift-off process. An image of the sample in its final state is shown in Figure 59.

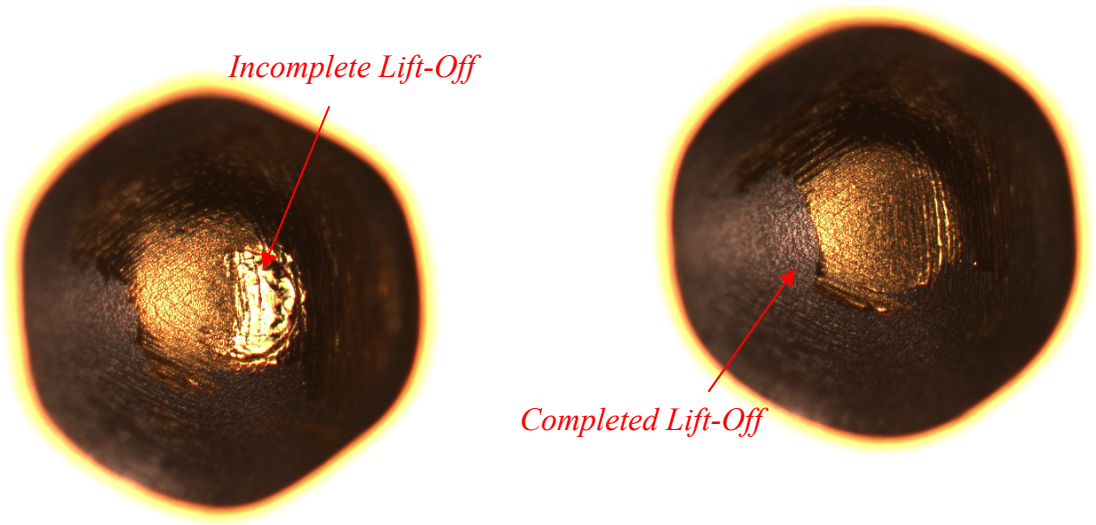


**Figure 59. Two adjacent hemispherical cavities from the SF-11 metal lift off trial demonstrate the unreliability of this method of pattern transfer.**

Unfortunately, time constraints limited any further exploration of this process, which must be studied much more extensively to discover a suitable technique for pattern transfer on such severe topographies. Although the 3D photolithography and metal lift-off processes were not perfected, a method for patterning and aligning completed hemispheres was developed with the assumption that these processes could be successfully completed in future work.

### Closed-Loop Alignment Techniques

At the outset of this research, a stated goal was to discover an isotropic etch process which would reliably create identically-sized hemispherical cavities. After much experimentation with wet HNA etching, RF-powered $SF_6$ reactive ion etching, and the ICP-powered $SF_6$ DSE process, this goal appears unattainable. The variances observed between cavity profiles are large enough to make traditional photomask alignment techniques ineffective. The addition of an HNA polishing step provided the benefit of

smoothing the cavity surfaces and rounding the cavity lips, but led to increased variances between cavities. Therefore, a new method for patterning and aligning an isotropically etched sample using a combination of optical microscopy, MatLab image processing techniques, and laser lithography was proposed.

This process requires the use of alignment marks which can be recognized by the Heidelberg μPG 101 direct-write laser lithography system. The previously created photomask used for sample preparation did not include alignment marks, so a new mask pattern was created by using the Heidelberg system to directly expose a layer of SU-8 photoresist which had been deposited over the surface of a 1" x 1" <111>-oriented Si sample. Two layers of Omnicoat were deposited prior to the SU-8 to facilitate its removal after the patterning process. The mask pattern included a 12 x 12 array of 440 μm-diameter mask apertures, as well as 4 x 4 arrays of 80 μm x 80 μm alignment marks. After exposure and development of the SU-8 and Omnicoat, a 100Å/1000Å Ti/Au layer was evaporated onto the sample surface. Next, a layer of S1818 photoresist was deposited and patterned using the previous photomask, so that the gold alignment marks were protected by circles of S1818 after development. With the alignment marks protected by the S1818 layer, the unprotected Ti/Au layer was removed with a wet chemical etch. Figure 60 shows a set of alignment marks and cleared etch apertures after this step.

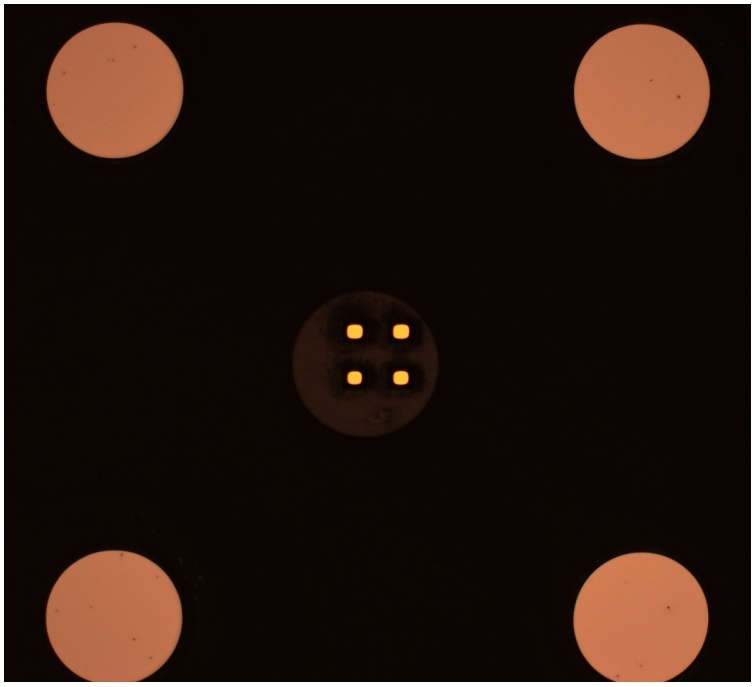

**Figure 60. A set of gold alignment marks protected by S1818, surrounded by four 440 um-diameter openings in the SU-8 masking layers.**

With the alignment marks patterned, the wafer was etched for 40 minutes using the now-standard DSE process parameters of 1700 W ICP power, 300 sccm $SF_6$ flow rate, 200 V RF Bias, and a chamber pressure of 100 mTorr. After etching, the SU-8 was removed using an ultrasonically agitated acetone bath. The optical microscope was used to take overlapping images of the entire sample surface, with the images being exported to MatLab to complete image stitching (or mosaicing).

The MatLab stitching code used was sourced from the MatLab file exchange, with some modifications made to better suit the intended application [67]. Three images displaced in the x-direction are combined by using correlation between the columns of shared edges. For example, the column in which the highest correlation between the first and second image is observed is chosen as the cropping point for the right edge of the

first image. The second image is then butted up against the first, and the same process is performed on the edge it shares with the third image. Figure 61 provides an example of three successfully stitched sample regions.

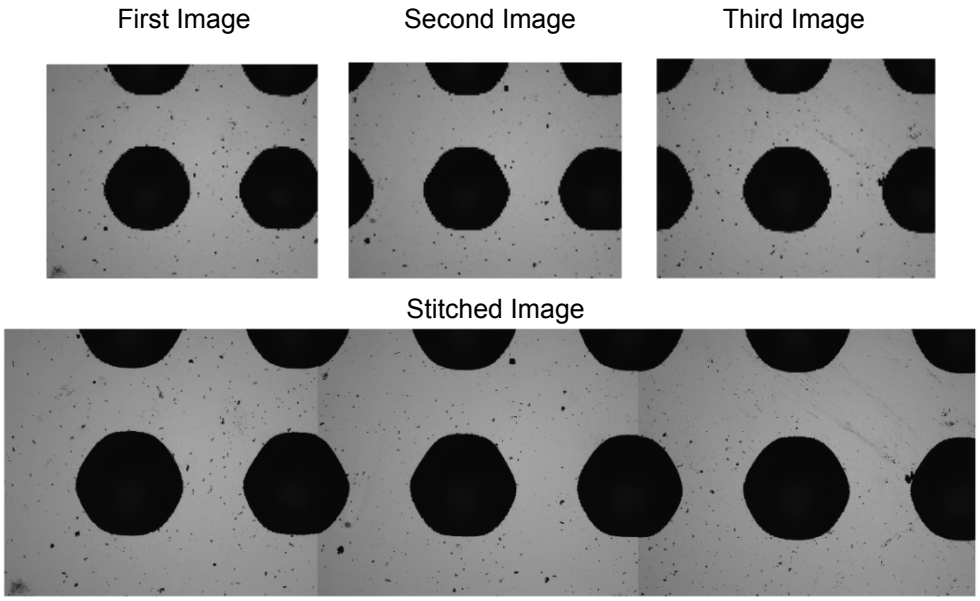


**Figure 61. An example of the MatLab-based image stitching process used to obtain a detailed image of the entire sample surface.**

The stitching code was further modified to allow for the stitching of three separate stitched images displaced in the y-direction. However, the previous stitching had made the dimensions of each picture slightly different, and resulted in minor x-direction displacements. To circumvent this issue, zero padding was performed on the images, although this is not a fully automated process. The user must decide whether zero padding is needed on the left or right side of the image to get good correlation values and an accurate stitching result. An example of this vertical stitching is provided in Figure 62.

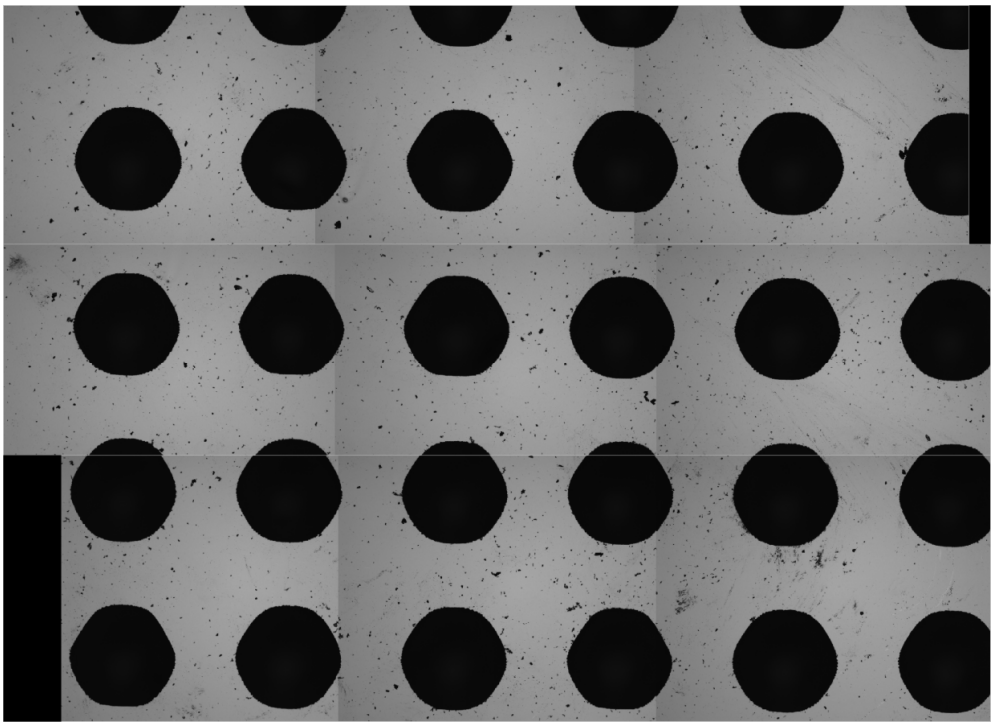

**Figure 62. A 3x3 array of stitched optical microscope images formed using automated horizontal stitching followed by a user-defined vertical stitching process.**

Finally, a series of image processing steps is completed on the image to reduce noise before exporting the result to L-Edit. In this process, the grayscale image is converted to a binary image, which in turn can be read into L-Edit using the Import Image feature. These pictures were taken at an original resolution of 1300x1030 pixels, which has a pixel length of 2.137 μm. By retaining the native resolution throughout all MatLab processing steps, the image can be imported into L-edit using the known pixel size, creating a mask layer which exactly replicates the wafer surface. The image is imported as a single cell, but the polygon relating to each cavity can be edited individually by flattening the cell, if desired. Figure 63 provides an example of a mask layout created in L-Edit using this method.

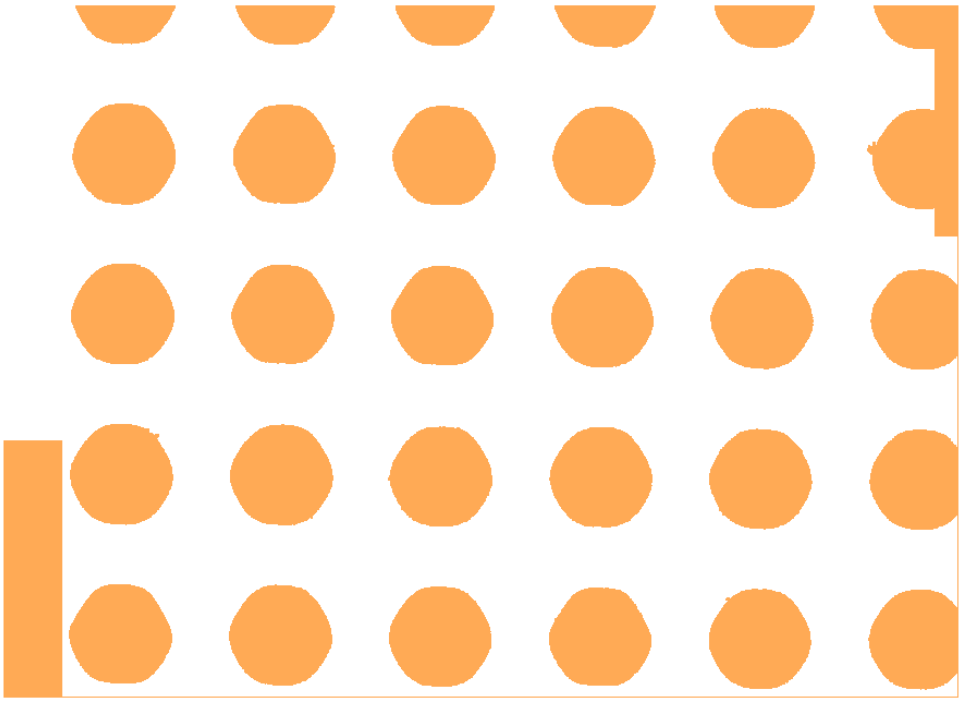

**Figure 63. An L-Edit mask layout created by importing a stitched image of the wafer surface captured with the optical microscope. This layout can be exported to common cleanroom systems such as the Heidelberg µPG 101 laser lithography system.**

As demonstrated above, this process was extremely successful on the DSE-processed samples. However, the HNA polishing step caused some unanticipated difficulties with the implementation of this method. First, the Ti/Au alignment marks, which were to be used to automatically align the sample for laser lithography, were removed in the polishing solution. Additionally, the smoothed, uniform surface of the sample and cavity lips severely affected the accuracy of the image stitching program. The correlation between images is greatly reduced due to the lack of noise features, causing errors in image placement to be common. An example of this is shown in Figure 64.

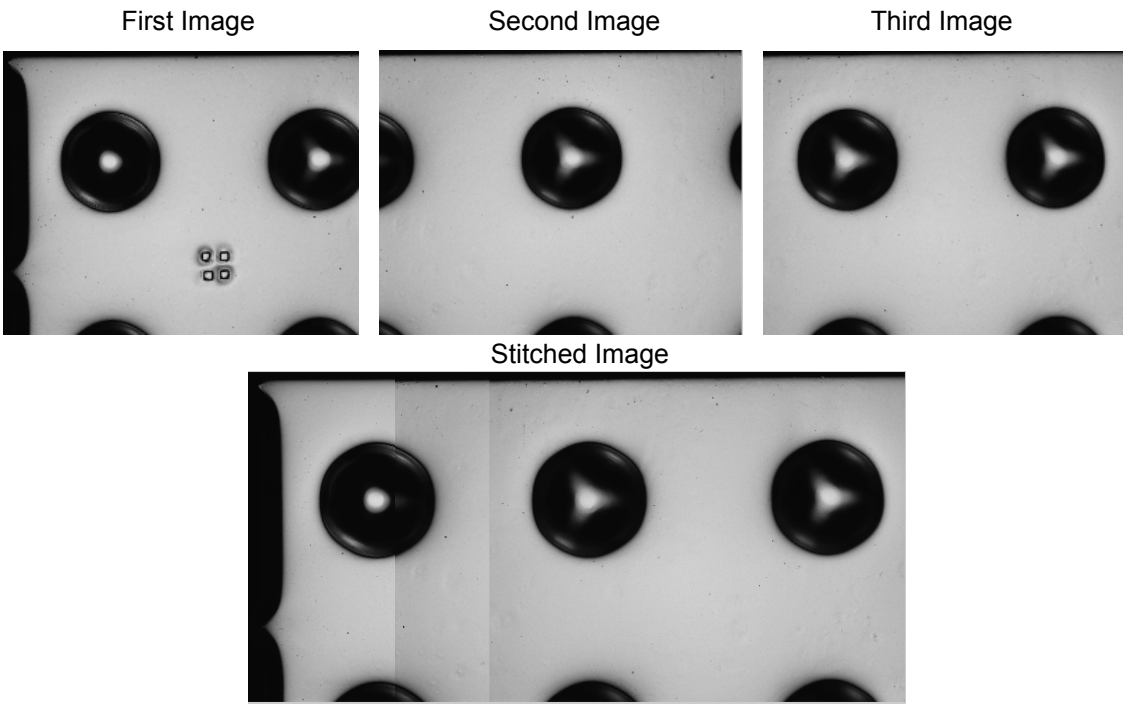


**Figure 64. An unsuccessful attempt to stitch together images of an HNA-polished sample. The lack of noise features in the images hinders the performance of the correlation algorithm which is used to properly place images. The remnants of a set of removed Ti/Au alignment marks are visible in the first image.**

In order to circumvent the problems with stitching accuracy, a simple process is proposed. First, a layer of photoresist such as S1805 can be deposited across the surface. By patterning this photoresist layer with random geometric patterns, additional non-circular features will be available for reference, hopefully boosting the correlation values between adjacent images. Even though the Ti/Au alignment marks were removed, their outlines still provide enough contrast to be used for alignment in the Heidelberg system. Unfortunately, due to time constraints, these proposed steps were not performed, and must be left for following researchers.

**Summary**

In this chapter, the data and observations from a number of experiments were presented and analyzed. First, the results of bulk isotropic etching using HNA, RIE, and DSE were compared with regards to etch consistency and profile characteristics. Ultimately, bulk HNA etching was abandoned after being found to be highly variable and difficult to control. The difficulties in working with HNA stemmed from its high sensitivity to temperature, which was difficult to regulate using available tools. RIE methods were also abandoned due to low observed etch rates (for this application) when operating at powers which offered suitable mask survivability. The ICP-powered DSE system offered the best blend of etch rate, controllability, and selectivity. A study of the system parameters determined settings of 1700 W ICP power, 300 sccm $SF_6$ flow rate, 200 V RF Bias, and a chamber pressure of 100 mTorr to be ideal for producing bulk isotropic etches. The etch progression with respect to mask aperture and time was also studied. From this, a clear trend in the ratio of vertical and lateral etch rates was established. Using this information, hemispherical cavities of various dimensions can be created simply by changing original mask apertures and etch durations.

Next, a MatLab image processing program was developed to analyze the differences in DSE-formed cavity anisotropies in <100> and <111>-oriented Si samples. The results provided show the variance in <100>-oriented Si cavity dimensions to be much lower than that observed in <111>-oriented Si cavities. The <100>-oriented Si samples demonstrate four-fold rotational symmetry, while the <111>-oriented Si samples exhibit a six-fold symmetry. However, the extent of anisotropy is nearly equal in either substrate orientation, according to all three geometry statistics (eccentricity, circularity,

and $R_{min}/R_{max}$). HNA polishing was demonstrated as an effective method for reducing cavity surface roughness, undercutting, and anisotropy all in a single process step. MatLab image analysis was used to supplement optical microscope, profilometer, and IFM measurements during this experiment. The anisotropy in <111>-oriented Si samples was significantly reduced after HNA polishing, whereas little effect was observed on <100>-oriented Si samples.

The results of photolithographic patterning and metal deposition efforts were also discussed. Available photoresists including S1805, S1818, and SF-11 were evaluated for their suitability in patterning over severe surface topographies. Problems such as photoresist pull-back from cavity edges and pooling at the cavity bottoms were especially noticeable when using the S1800 series photoresists. SF-11 provided a better conformal coating; however, an attempt to perform metal-lift off using a bi-layer stack of SF-11 and S1805 failed to produce an acceptable result. Based on these results, alternative methods of photoresist deposition must be explored to provide a viable process for the required 3D lithography steps.

Finally, a new process of creating successive masking layers using MatLab image processing techniques was proposed, developed, and evaluated. The image stitching algorithm successfully created precise, high resolution images of the wafer surface when performed on DSE-produced cavities. These images were then successfully transferred to L-Edit, where they can be used as a basis for subsequent masking layers. Unfortunately, the image stitching algorithm failed to produce the same quality results on HNA-polished samples, so further development of this process is needed.

# V. Conclusions and Recommendations

## Chapter Overview

Previously conducted AFRL studies have investigated the feasibility of creating spherical microrobot shells capable of electrostatic actuation. As the residual stress bending methods used in these earlier efforts were determined to have critical limitations in shell performance and fabrication feasibility, a new fabrication process was sought. This chapter provides a summary of the thesis research conducted in an effort to address these shortcomings.

## Conclusions of Research

This research effort was begun with the intention of developing a novel process to mass fabricate spherical packages using MEMS fabrication techniques available in the AFIT and AFRL cleanrooms. In order to properly tackle the challenges presented by this project, a thorough review of relevant background research was conducted. The relevant findings of this literature review were presented in Chapter 2. The earlier AFRL microrobot fabrication efforts were discussed to provide the reader with insight into the rationale for conducting this research. This research effort was linked to the field of programmable matter, and more specifically to recent projects in the areas of solid-state, self-reconfigurable modular robotics. The technology and mechanisms behind MEMS fabrication technologies used in this research were also studied and discussed in detail. Finally, a number of particularly relevant research studies and fabrication attempts involving spherical micromachining on silicon wafers were presented. The knowledge

gained from the review of MEMS fabrication processes was combined with the experiences of previous researchers to formulate an approach to accomplish this research.

Chapter 3 detailed the selected methodology for undertaking the experimental aspect of the research effort. First, a number of etch studies involving wet HNA etching, RF-powered RIE etching, and the ICP-powered DSE process were designed to determine an appropriate method for performing a precise, repeatable isotropic bulk silicon etch. Next, a study on the effectiveness of HNA as a polishing etch was developed. Additionally, a standard photolithography process using common materials was designed to assess the suitability of these materials and processes for the patterning of wafer surfaces exhibiting severe surface topography. Finally, a wide array of measurement techniques, including optical and scanning electron microscopy, profilometer and white light interferometer depth measurement, and MatLab image analysis, were presented as viable methods to evaluate the performance of various process elements.

The results of the selected experiments were presented in Chapter 4. Due to the extreme variability in etch results and the difficulties encountered in properly masking and controlling the bulk HNA etch, it is not recommended as a method for creating the desired hemispherical etch cavities without substantial process development efforts. $SF_6$ plasma etching using the DSE tool was determined to be the preferred method for bulk silicon etching, as it offered the best blend of etch rate, controllability, and selectivity. A study of the system parameters determined ideal settings for producing bulk isotropic etches in silicon. Furthermore, a relationship between etch profile diameter, mask aperture diameter, and cavity isotropy was discovered and documented. The variance between DSE-formed cavity diameters across a sample surface is significantly smaller in

<100>-oriented Si than <111>-oriented Si. HNA polishing was also demonstrated as an effective method for reducing cavity surface roughness, undercutting, and anisotropy all in a single process step. Additionally, <111>-oriented Si did display a more circular etch profile than <100>-oriented Si after a short HNA polishing step. As suspected, conventional photoresist materials and processing methods failed to provide the sufficiently conformal coatings necessary to enable accurate and reliable metal patterning. Finally, MatLab image processing techniques were shown to be a valuable method for data collection and analysis on cleanroom fabrication processes. Furthermore, a method of incorporating previous etch results into the development of successive masking layers was proposed, developed, and evaluated. This fabrication method leverages the capabilities of MatLab, L-Edit, and the Heidelberg laser lithography system in forming a closed-feedback photolithography alignment system.

**Significance of Research**

While the proposed design of these spherical microdevice packages was specifically developed with the integration of the proposed autonomous microrobot design in mind, it can be applied as an innovative packaging scheme for a wide variety of microdevices. As technological advances continue to reduce the size of integrated circuits, energy collection and storage devices, and memory chips, advanced packaging solutions must be proposed to properly leverage emerging capabilities. This research effort establishes a path forward for a highly ambitious, yet potentially revolutionary packaging scheme which proposes to take microelectronics packaging away from the planar restrictions which have been in place for over a half century. Successful

completion of this project would enable countless new applications in burgeoning fields such bioMEMS, wireless sensing, distributed networking, microrobotics, and programmable matter, among others.

This research provided a number of more immediate impacts to the AFIT, AFRL, and greater research community. First, a number of non-standard fabrication techniques were studied and documented, advancing the knowledge base for future cleanroom users here at AFIT. The characterization of isotropic etch performance in the typically anisotropically-etching DSE tool is particularly useful to researchers who may experience frustration performing isotropic etches in less powerful RIE tools. $SF_6$ plasma-based isotropic etching of silicon was characterized at depths and etch rates not found in available literature. The success of this study ultimately presents a viable alternative to wet HNA or vapor $XeF_2$ etching, which each pose significantly more complications in processing. Furthermore, the anisotropic tendencies demonstrated by different crystal orientations in Si during $SF_6$ plasma etching were found to be significant, yet not in complete agreement with those previously observed during wet HNA etching. A method of HNA polishing which was not well documented in previous research was found to be an effective method for alleviating the commonly encountered problems of undercutting, surface roughness, and anisotropy. The development of MatLab image processing routines and their incorporation into etch analysis provides future AFIT researchers with powerful tools for rapid data collection. Furthermore, the development of the closed-loop photolithography process leverages the capabilities of existing cleanroom devices to perform sophisticated wafer alignment and patterning processes capable of drastically improving process throughputs. Finally, the comprehensive survey of similar fabrication

attempts and relevant processing techniques can be seen as a considerable aid to future research on this project.

**Recommendations for Future Research**

Admittedly, the large scope of this project far outweighed the capabilities of a single graduate student, leaving many areas of this process development open for further research. Before discussing additional processing steps, recommendations for improvement on completed work can be made. First and foremost, the MatLab image processing algorithms could be drastically improved by someone with a more extensive background in the field of image processing. With the patterning of additional reference points, the entire wafer surface could be mapped, as shown in Figure 65. This process would provide a wealth of additional information detailing etch progression.

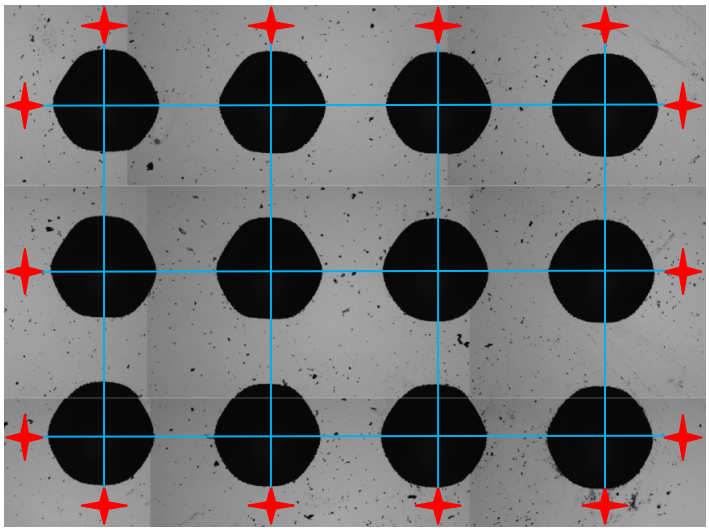

**Figure 65. Proposed etch cavity MatLab mapping method for implementation in future research.**

Another area which was addressed but not completed is the photoresist patterning. The aerosolized spray photoresist from MicroChem was purchased with the intent of

being used in this research, however on-base materials safety requirements delayed the acquisition of this photoresist by approximately 4 months. Future research evaluating the effectiveness of this low-cost spray photoresist solution would be especially intriguing.

The complete envisioned fabrication process contains many processes which were not addressed in this research. In fact, the experiments conducted to this point only fully characterize two process steps, while partially addressing photoresist patterning requirements and wafer alignment techniques. A schematic of the full proposed fabrication process is shown in Figure 66.

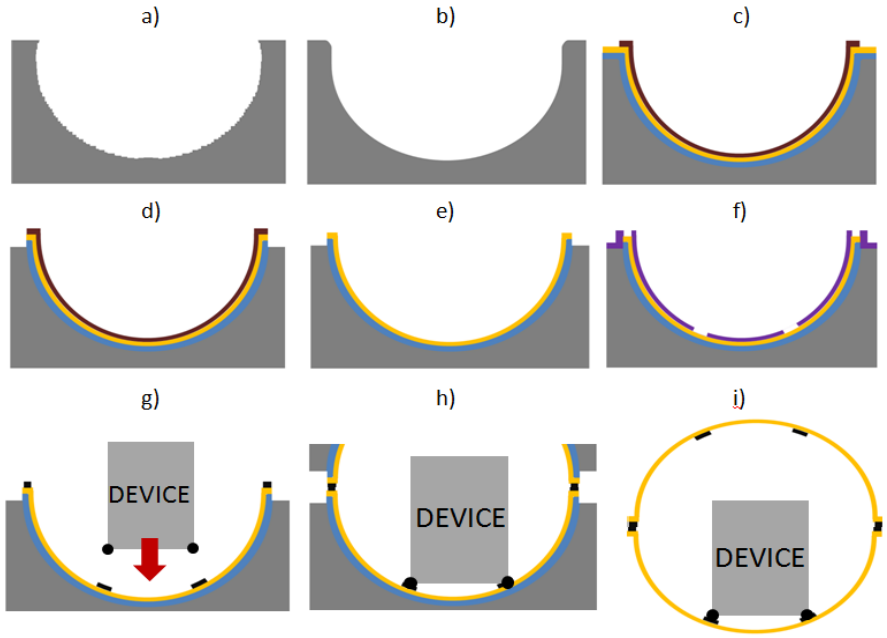


**Figure 66. Proposed package fabrication process. The cross section of a silicon wafer is shown after a) isotropic SF6 etch, b) polishing performed by HNA c) CVD deposition of sacrificial and structural layers as well as photoresist patterning d) etching of unwanted CVD layers e) removal of protective photoresist f) coating and precision patterning of lift-off photoresist layer g) metal deposition, lift off, and flip chip bonding of device package h) thermocompression bonding of hemispheres and i) etching of silicon wafer and sacrificial layers to release completed device.**

According to the proposed process flow, chemical vapor deposition and metal patterning techniques must be evaluated, along with etch chemistries for suitable removal

of sacrificial layers. In order to avoid the complexities of repeatedly fabricating large hemispherical cavities, the proposed process utilizes two identically (or as near to identical as possible) patterned silicon wafers as a reusable mold. However, the greatest challenge for future research is most likely posed by the high degree of accuracy required for successful bonding of wafer hemispheres. While it is envisioned that the bonding process can borrow significantly from the lessons learned in the previous AFRL-directed packaging study, this particular application will be pushing the boundaries of known packaging methods.

Once the spheroidal package has been successfully demonstrated, the research focus can return to the integration of microrobotic components into the package. The actuation capabilities of released microspheres patterned with internal metal electrodes can be tested through the use of an external electrode array designed by and housed at AFRL/RY. The electrode array is pictured in Figure 67 and has been previously demonstrated to successfully actuate the stress-fabricated microspheres [3].

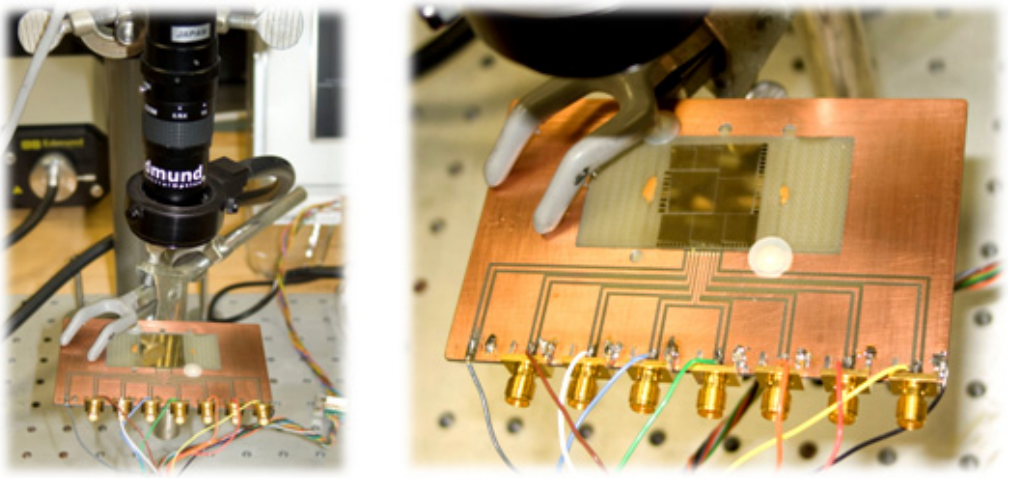

**Figure 67. AFRL/RY external electrode actuation array designed to test spherical microrobot actuation performance [3].**

**Summary**

This research effort contributed to the development of a novel process to mass fabricate spherical packages using MEMS fabrication techniques. Important contributions to the overall research effort included a comprehensive survey of available fabrication technologies, the characterization of bulk isotropic etch processes, and the development of innovative wafer evaluation and alignment techniques. Throughout the course of this research, a basic process flow for the fabrication of a highly ambitious, yet potentially revolutionary packaging scheme was developed. In addition to applications in a wide array of emerging research fields, the proposed design meets the needs of the autonomous microrobot design which inspired this research project.

## References


[1] A. Junk and F. Riess, "From an idea to a vision: There's plenty of room at the bottom," *American Journal of Physics,* vol. 74, no. 9, pp. 825-830, 2006.

[2] J. R. Reid, V. Vasilyev and R. T. Webster, "Building Micro-Robots: a path to sub-mm3 autonomous systems," *Processes of Nanotech 2008,* 2008.

[3] V. S. Vasilyev, J. R. Reid and R. Webster, "Microfabrication of Si/SiO2-Spherical Shells as a Path to Sub-mm3 Autonomous Robotic Systems," in *Materials Research Society Fall Meeting*, Boston, MA, 2008.

[4] "Programmable matter," Wikipedia, the free encyclopedia, 2 July 2013. [Online]. Available: http://en.wikipedia.org/wiki/Programmable_matter. [Accessed 9 August 2013].

[5] T. Toffoli and N. Margolus, "Programmable matter: Concepts and realization," *Physica D: Nonlinear Phenomena,* vol. 47, no. 1-2, pp. 263-272, 1991.

[6] A. P. Alivisatos, "Semiconductor Clusters, Nanocrystals, and Quantum Dots.," *Science,* vol. 271, no. 5251, pp. 933-937, 1996.

[7] K. E. Drexler, Engines of Creation: The Coming Era of Nanotechnology, Garden City, NJ: Anchor, 1986.

[8] D. Ferber, "SYNTHETIC BIOLOGY: Microbes Made to Order," *Science,* vol. 303, no. 5655, pp. 158-161, 2004.

[9] D. Schurig, J. J. Mock, B. J. Justice, S. A. Cummer, J. B. Pendry, A. F. Starr and D. R. Smith, "Metamaterial Electromagnetic Cloak at Microwave Frequencies," *Science,* vol. 314, no. 5801, pp. 977-980, 2006.

[10] J. S. Hall, "Utility Fog: A Universal Physical Substance," in *Vision-21: Interdisciplinary Science and Engineering in the Era of Cyberspace*, NASA, 1993, pp. 115-126.

[11] T. Fukuda, S. Nakagawa, Y. Kawauchi and M. Buss, "Self organizing robots based on cell structures--CEBOT," *Proc. IEEE/RSJ Int. Conf. Intelligent Robots and Systems (IROS),* pp. 145-150, 1988.

[12] M. Yim, W.-M. Shen, B. Salemi, D. Rus, M. Moll, H. Lipson, E. Klavins and G. S. Chirikjian, "Self Reconfigurable Robot Systems: Challenges and Opportunities for the Future," *IEEE Robotics & Automation Magazine,* pp. 43-52, March 2007.

[13] A. H. Slocum, "Precision machine design: macromachine design philosophy and its applicability to the design of micromachines.," *Micro Electro Mechanical Systems, 1992, MEMS '92, Proceedings. An Investigation of Micro Structures, Sensors, Actuatros, Machines and Robot. IEEE.,* pp. 37-42, February 1992.

[14] S. Goldstein, T. C. Mowry, J. D. Campbell, M. P. Ashley-Rollman, M. De Rosa, S. Funiak, J. F. Hoburg, M. E. Karagozler, B. Kirby, P. Lee, P. Pillai, J. R. Reid, D. D. Stancil and M. P. Weller, "Beyond Audio and Video: Using Claytronics to Enable Pario," *AI Magazine,* pp. 29-45, 2009.

[15] B. Kirby, J. Campbell, B. Aksak, P. Pillai, J. Hoburg, T. Mowry and S. C. Goldstein, "Catoms: Moving Robots Without Moving Parts," *American Association for Artificial Intelligence,* pp. 1730-1731, 2005.

[16] K. Gilpin, A. Knaian and D. Rus, "Robot Pebbles: One Centimeter Modules for Programmable Matter through Self-Disassembly," *IEEE International Conference on Robotics and Automation (ICRA),* pp. 2485-2492, 2010.

[17] A. Knaian, "Electropermanent Magnetic Connectors and Actuators: Devices and Their Application in Programmable Matter, Ph.D. Thesis," MIT Electrical Engineering and Computer Science, Cambridge, MA, 2010.

[18] T. Srinivasan, "Scaling in the Microworld," Berkeley Sensor and Actuator Center, Berkeley, CA, 2003.

[19] C. Bellew, S. Hollar and K. Pister, "An SOI process for fabrication of solar cells, transistors, and electrostatic actuators," *International Conference on Solid-State Sensors and Actuators,* vol. 2, pp. 1075-1078, 2003.

[20] Intel Corporation, "Moore's Law and Intel Innovation," Intel, 2014. [Online]. Available: http://www.intel.com/content/www/us/en/history/museum-gordon-moore-law.html. [Accessed 8 February 2014].

[21] K. B. Lee, Principles of Microelectromechanical Systems, Hoboken, NJ: John Wiley & Sons, Inc. , 2011.

[22] J. M. Bustillo, R. T. Howe and R. S. Muller, "Surface Micromachining for Microelectromechanical Systems," *Proceedings of the IEEE,* vol. 86, no. 8, pp. 1552-1574, 1998.

[23] G. T. Kovacs, N. I. Maluf and K. E. Peterson, "Bulk Micromachining of Silicon," *Proceedings of the IEEE,* vol. 86, no. 8, pp. 1536-1551, 1998.

[24] MEMS at Sandia, "MEMS Image Gallery," Sandia National Laboratories, 2008. [Online]. Available: http://mems.sandia.gov/gallery/images.html. [Accessed 8 February 2014].

[25] H. R. Robbins and B. Schwartz, "Chemical etching of silicon -- I. The system HF, HNO3, H20, and HC2C3O2," *Journal of the Electrochemical Society,* vol. 106, no. 6, pp. 505-508, 1959.

[26] H. R. Robbins and B. Schwartz, "Chemical etching of silicon --II. The system HF, HNO3, H20, and HC2C3O2," *Journal of the Electrochemical Society,* vol. 107, no. 2, pp. 108-111, 1960.

[27] B. Schwartz and H. R. Robbins, "Chemical etching of silicon-- III. A temperature study in the acid system," *Journal of the Electrochemical Society,* vol. 108, no. 4, pp. 365-372, 1961.

[28] A. A. Hamzah, N. A. Aziz, B. Y. Majiis, J. Yunas, C. F. Dee and B. Bais, "Optimization of HNA etching parameters to produce high aspect ratio solid silicon microneedles," *Journal of Micromechanics and Microengineering,* vol. 22, no. 9, p. 095017, 2012.

[29] M. J. Madou, Fundamentals of Microfabrication: The Science of Miniaturization, Second Edition, Boca Raton: CRC Press, 2002.

[30] J. K. Lee, J. C. Choi, W. I. Jang, H.-R. Kim and S. H. Kong, "Electrowetting Lens Employing Hemispherical Cavity Formed by Hydrofluoric Acid, Nitric Acid, and Acetic Acid Etching of Silicon," *Japanese Journal of Applied Physics,* vol. 51, no. 06FL05, 2012.

[31] S. R. McLelland, A. Grobnic, R. James, J. S. Wight and M. G. Stubbs, "Micromachined Hemispheroidal Cavity Resonators," *IEEE Tansactions on Microwave Theory and Techniques,* vol. 56, no. 4, pp. 982-990, 2008.

[32] C.-H. Han and E.-S. Kim, "Study of Self-Limiting Etching Behavior in Wet Isotropic Etching of Silicon," *Japenese Journal of Applied Physics,* vol. 37, no. 12B, pp. 6939-6941, 1998.

[33] G. S. May and S. M. Sze, Fundamentals of Semiconductor Fabrication, John Wiley & Sons, Inc., 2011.

[34] MEMS & Nanotechnology Exchange, "Etching Processes," [Online]. Available: https://www.mems-exchange.org/MEMS/processes/etch.html. [Accessed 8 Febrauary 2014].

[35] Oxford Instruments Plasma Technology, "The Bosch Process for Etching Micro-Mechanical Systems (MEMS) - Principles, Advances and Applications," AZoNano, 24 September 2013. [Online]. Available: http://www.azonano.com/article.aspx?ArticleID=2738. [Accessed 27 January 2014].

[36] A. Picard, F. Turban and B. Grolleau, "Plasma diagnostics of a SF6 radiofrequency discharge used for the etching of silicon," *Journal of Physics D: Applied Physics,* vol. 19, no. 6, pp. 991-1005, 1986.

[37] R. Legtenberg, H. Jansen, M. de Boer and M. Elwenspoek, "Anisotropic Reactive Ion Etching of Silicon Using SF6/O2/CHF3 Gas Mixtures," *Journal of the Electrochemical Society,* vol. 142, no. 6, pp. 2020-2028, 1995.

[38] D. L. Flamm, "Mechanisms of silicon etching in fluorine- and chlorine-containing plasmas," *Pure & Applied Chemistry,* vol. 62, no. 9, pp. 1709-1720, 1990.

[39] K. Sugano and O. Tabata, "Reduction of surface roughness and aperture size effect for etching of Si with XeF2," *Journal of Micromechanics and Microengineering,* vol. 12, no. 6, pp. 911-916, 2002.

[40] P. B. Chu, J. T. Chen, R. Yeh, G. Lin, J. C. P. Huang, B. A. Warneke and K. S. J. Pister, "Controlled Pulse-Etching with Xenon Difluoride," in *International Conference on Solid-State Sensors and Actuators*, Chicago, 1997.

[41] MEMS at Sandia, "SUMMiT VTM Overview," Sandia National Laboratories, 2008. [Online]. Available: http://www.mems.sandia.gov/tech-info/summit-v.html. [Accessed 9 February 2014].

[42] MEMSCAP, "PolyMUMPs," 2012. [Online]. Available: http://www.memscap.com/products/mumps/polymumps. [Accessed 9 February 2014].

[43] K. Fischer and R. Suss, "Spray Coating -- a Solution for Resist Film Deposition Across Severe Topography," in *IEEE/SEMI International Electronics Manufacturing Technology Symposium*, 2004.

[44] J. O'Brien, P. J. Hughes, M. Brunet, B. O'Neill, J. Alderman, B. Lane, A. O'Riordan and C. O'Driscoll, "Advanced photoresist technologies for microsystems," *Journal of Micromechanics and Microengineering,* vol. 11, pp. 353-358, 2001.

[45] P. Kersten, S. Bouwstra and J. Petersen, "Photolithography on micromachined 3D surfaces using electrodeposited photoresists," *Sensors and Actuators A,* vol. 51, pp. 51-55, 1995.

[46] N. P. Pham, E. Boellaard, J. N. Burghartz and P. M. Sarro, "Photoresist Coating Methods for the Integration of Novel 3-D RF Microstructures," *Journal of Microelectromechanical Systems,* vol. 13, no. 3, pp. 491-499, 2004.

[47] N. P. Pham, J. N. Burghartz and P. M. Sarro, "Spray coating of photoresist for pattern transfer on high topography surfaces," *Journal of Micromechanics and Microengineering,* vol. 15, pp. 691-697, 2005.

[48] Stanford Nanofabrication Facility, "SNF Labmembers Wiki -- EVG 101 Spray Coater," Stanford University, 2014. [Online]. Available: https://snf.stanford.edu/SNF/equipment/optical-photolithography/resist-coat/ev101-spray-coater/evg-101-spray-coater. [Accessed 10 February 2014].

[49] N. P. Pham, D. S. Tezcan, W. Ruythooren, P. De Moor, B. Majeed, K. Baert and B. Swinnen, "Photoresist coating and patterning for through-silicon via technology," *Journal of Micromechanics and Microengineering,* vol. 18, p. 9pp, 2008.

[50] MicroChem, "Products -- Microspray," 2006. [Online]. Available: http://www.microchem.com/Prod-Microspray.htm. [Accessed 14 September 2013].

[51] H. Foll, "The Importance of Silicon Dioxides," Kiel University, Germany, [Online]. Available: http://www.tf.uni-kiel.de/matwis/amat/elmat_en/index.html. [Accessed 10 February 2014].

[52] J. H. Lau, C. K. Lee, C. S. Premachandran and Y. Aibin, Advanced MEMS Packaging, New York: McGraw-Hill Companies, Inc., 2010 .

[53] H. Baltes, O. Brand, G. K. Fedder, C. Hierold, J. G. Korvink and O. Tabata, Advanced Micro & Nanosystems Volume 1: Enabling Technology for MEMS and Nanodevices, Weinheim, Germany: Wiley-VCH Verlag GmbH & Co. , 2004.

[54] R. R. Tummala, E. J. Rymaszewski and A. G. Klopfenstein, Microelectronics Packaging Handbook, New York: Van Nostrand Reinhold, 1989.

[55] T. Schimert, R. Howe, M. Schmidt and S. Montague, "Vacuum Packaging for Microelectromechanical Systems (MEMS)," Air Force Research Laboratory Information Directorate, Rome, New York, 2002.

[56] K. D. Wise, T. Jackson, N. A. Masnari, M. G. Robinson, D. E. Solomon, G. H. Wuttke and W. B. Rensel, "Fabrication of hemispherical structures using semiconductor technology for use in thermonuclear fusion research," *Journal of Vacuum Science Technology,* vol. 16, no. 3, pp. 936-939, 1979.

[57] K. P. Larsen, J. T. Ravnkilde and O. Hansen, "Investigations of the isotropic etch of an ICP source for silicon microlens mold fabrication," *Journal of Micromechanics and Microengineering,* vol. 15, pp. 873-882, 2005.

[58] J. Albero, L. Nieradko, C. Gorecki, H. Ottevaere, V. Gomez, H. Thienpont, J. Pietarinen, B. Paivanranta and N. Pasilly, "Fabrication of spherical microlenses by a combination of isotropic wet etching of silicon and molding techniques," *Optics Express,* vol. 17, no. 8, pp. 6283-6292, 2009.

[59] I. P. Pridhodko, S. A. Zotov, A. A. Trusov and A. M. Shkel, "Microscale Glass-Blown Three-Dimensional Spherical Shell Resonators," *Journal of Microelectromechanical Systems,* vol. 20, no. 3, pp. 691-701, 2011 .

[60] M. L. Chan, P. Fonda, C. Reyes, J. Xie, H. Najar, L. Lin, K. Yamazaki and D. A. Horsley, "Micromachining 3D hemispherical features in silicon via micro-EDM," in *IEEE 25th International Conference on Micro Electro Mechanical Systems (MEMS)*, Paris, 2012.

[61] V. B. Svetovoy, J. W. Berenschot and M. C. Elwenspock, "Experimental investigation of anisotropy in isotropic silicon etching," *Journal of Micromechanics and Microengineering,* pp. 2344-2351, 2007.

[62] R. White, "Isotropic Silicon Etching using HF/Nitric/Acetic Acid (HNA)," 6 June 2007. [Online]. Available: http://engineering.tufts.edu/microfab/index_files/SOP/SiliconEtch_HNA_SOP.pdf. [Accessed 24 August 2013].

[63] K. R. Williams and R. S. Muller, "Etch Rates for Micromachining Processing," *Journal of Microelectromechanical Systems,* vol. 5, no. 4, pp. 256-269, 1996.

[64] K. R. Williams, K. Gupta and M. Wasilik, "Etch Rates for Micromachining Processing--Part II," *Journal of Microelectromechanical Systems,* vol. 12, no. 6, pp. 761-778, 2003.

[65] MicroChem, "SU-8 2000 Permanent Epoxy Negative Photoresist," [Online]. Available: http://microchem.com/pdf/SU-82000DataSheet2025thru2075Ver4.pdf. [Accessed 24 August 2013].

[66] ANU Centre for Sustainable Energy Systems (CSES), "HNA (HF:Nitric:Acetic) Etch - Full Procedure," February 2009. [Online]. Available: http://sun.anu.edu.au/files/ltbfp_HNA_Etch.pdf. [Accessed 28 January 2014].

[67] P. Kamble, *Stitching Three Images Using Correlation,* MATLAB CENTRAL File Exchange, 2013.

[68] S. Hollar, A. Flynn, C. Bellow and K. Pister, "Solar powered 10mg silicon robot," *IEEE International Conference on Micro Electro Mechanical Systems,* pp. 706-711, 2003.

## Vita

Second Lieutenant Ryan M. Dowden is a proud native of Slinger, Wisconsin. He graduated from the United States Air Force Academy with a Bachelor of Science degree in Mechanical Engineering in May 2012. Upon graduation, he received his commission as an officer in the United States Air Force, and was selected to serve as a 62E – Developmental Engineer. His first assignment was to the Air Force Institute of Technology to pursue a Master's of Science in Electrical Engineering. Upon graduation from AFIT, he will join the 453d Electronic Warfare Squadron at Lackland AFB.

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**14. ABSTRACT**

Sub-mm$^3$ spherical microrobots are being researched as a path towards reconfigurable wireless networks and programmable matter. The microrobot design requires a spheroidal microdevice package compatible with solar energy collection, wireless sensing, and electrostatic actuation mechanisms. Throughout this research, MEMS fabrication techniques were evaluated with regards to their applicability to the packaging process. $SF_6$-based plasma was determined to be a preferable alternative to wet HNA etching when producing repeatable bulk isotropic etches in silicon. HNA polishing was demonstrated as an effective method of reducing undercutting, surface roughness, and anisotropy. MatLab image processing routines were developed and incorporated into etch analysis, providing an efficient method of data collection. A method of performing sophisticated wafer alignment and photolithography processes by leveraging existing cleanroom devices was proposed. This research established a path forward for an advanced packaging scheme designed to move microelectronics packages away from the planar circuit board configurations of the past and into future autonomous architectures. The proposed design is applicable to a variety of microelectronics applications while meeting the requirements of the sub-mm$^3$ spherical microrobot system.

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