



Actuation and Response in Microsystems

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THz and nm Transistors for 1-1000 GHz Electronics

***Mark Rodwell
University of California, Santa Barbara***

The End (of Moore's Law) is Near (?)

It's a great time to be working on electronics !

Things to work on:

InP transistors: extend to 3-4 THz → GHz & low-THz ICs

GaN HEMTs: powerful transmitters from 1-300 GHz

Si MOSFETs: scale them past 16 nm

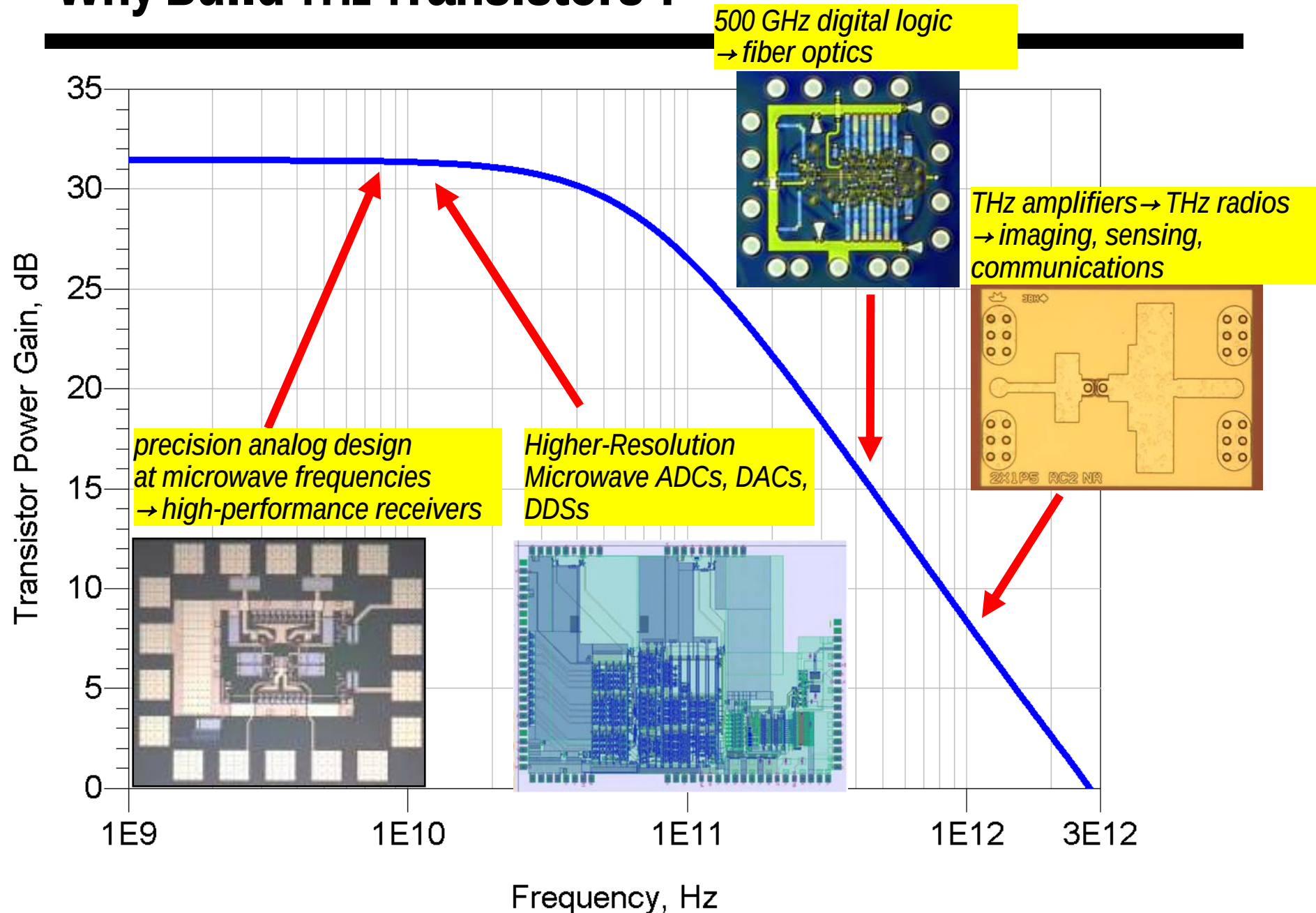
III-V MOSFETs: help keep VLSI scaling (maybe)

VLSI transistors: subvert Boltzmann → solve power crisis

mm-wave VLSI: massively complex ICs to re-invent radio

Why THz Transistors ?

Why Build THz Transistors ?



How to Make THz Transistors

Frequency Limits and Scaling Laws of (most) Electron Devices

$$\tau \propto \text{thickness}$$

$$C \propto \text{area} / \text{thickness}$$

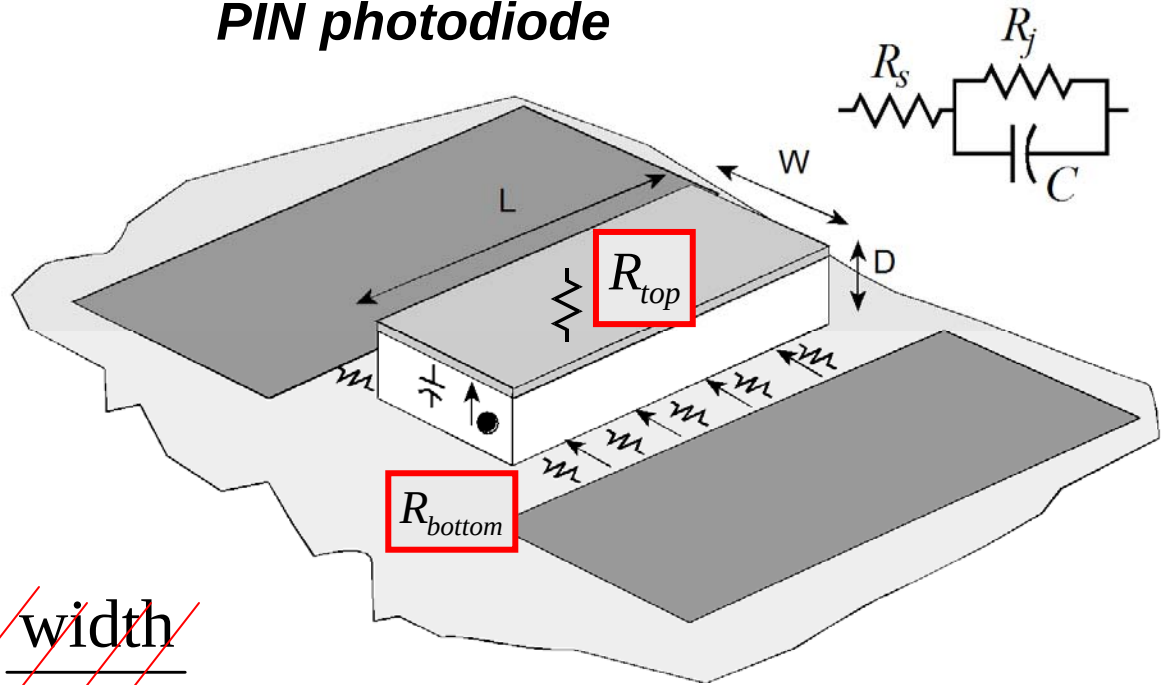
$$R_{top} \propto \rho_{contact} / \text{area}$$

$$R_{bottom} \propto \frac{\rho_{contact}}{\text{area}} + \frac{\rho_{sheet}}{4} \cdot \frac{\text{width}}{\text{length}}$$

$$I_{\text{max, space-charge-limit}} \propto \text{area} / (\text{thickness})^2$$

$$\Delta T \propto \frac{\text{power}}{\text{length}} \times \log\left(\frac{\text{length}}{\text{width}}\right)$$

PIN photodiode



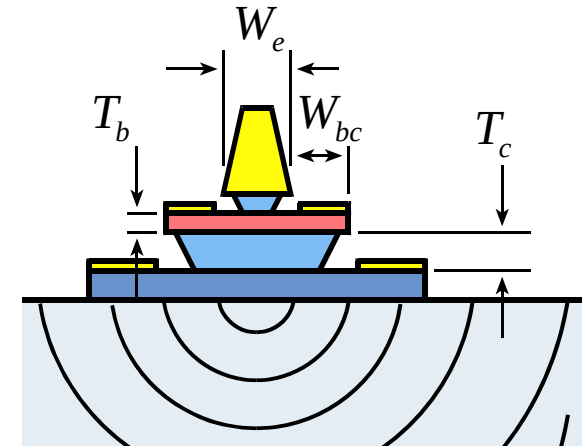
To double bandwidth,

reduce thicknesses 2:1 Improve contacts 4:1

reduce width 4:1, keep constant length

increase current density 4:1

Bipolar Transistor Scaling Laws



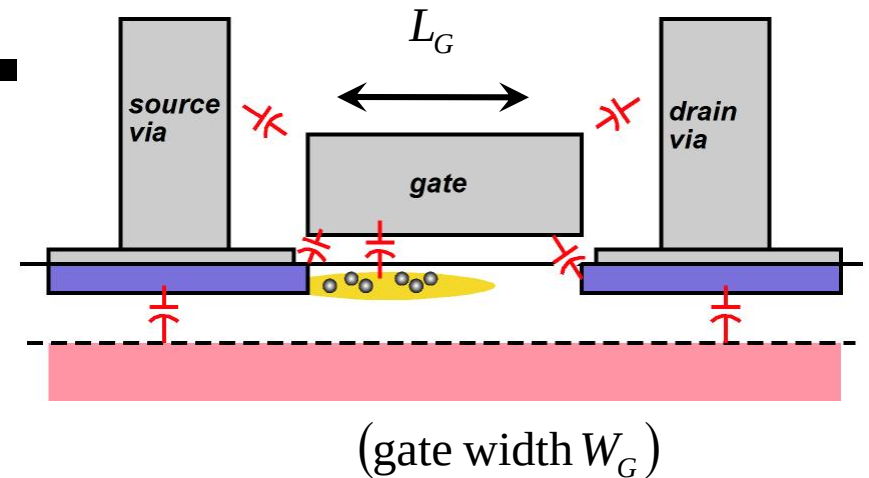
Changes required to double transistor bandwidth:

(emitter length L_E)

parameter	change
collector depletion layer thickness	decrease 2:1
base thickness	decrease 1.414:1
emitter junction width	decrease 4:1
collector junction width	decrease 4:1
emitter contact resistance	decrease 4:1
current density	increase 4:1
base contact resistivity	decrease 4:1

Linewidths scale as the inverse square of bandwidth because thermal constraints dominate.

FET Scaling Laws



Changes required to double transistor bandwidth:

parameter	change
gate length	decrease 2:1
gate dielectric capacitance density	increase 2:1
gate dielectric equivalent thickness	decrease 2:1
channel electron density	increase 2:1
source & drain contact resistance	decrease 4:1
current density (mA/ μm)	increase 2:1

Linewidths scale as the inverse of bandwidth because fringing capacitance does not scale.

THz & nm Transistors: it's all about the interfaces

*Metal-semiconductor interfaces (Ohmic contacts):
very low resistivity*

*Dielectric-semiconductor interfaces (Gate dielectrics):
very high capacitance density*

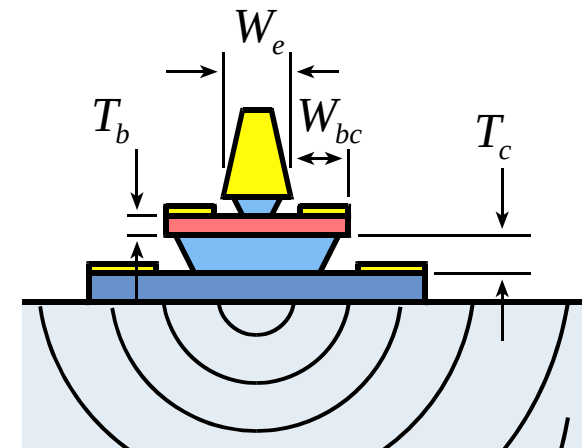
Transistor & IC thermal resistivity.



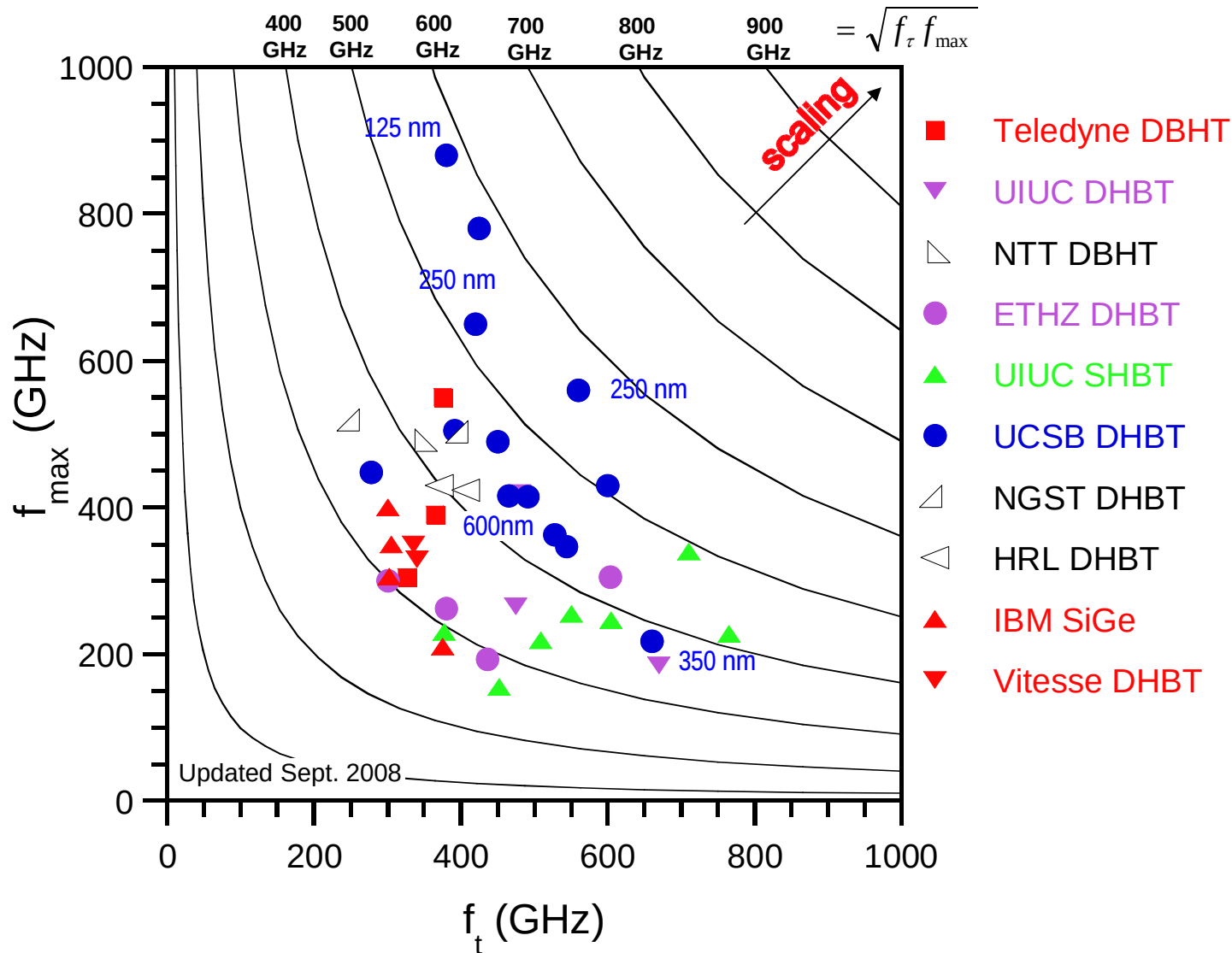
THz Bipolar Transistors

InP Bipolar Transistor Scaling Roadmap

	industry	university →industry	university 2007-9	appears feasible	maybe
emitter	512 16	256 8	128 4	64 2	32 nm width 1 $\Omega \cdot \mu\text{m}^2$ access ρ
base	300 20	175 10	120 5	60 2.5	30 nm contact width, 1.25 $\Omega \cdot \mu\text{m}^2$ contact ρ
collector	150 4.5 4.9	106 9 4	75 18 3.3	53 36 2.75	37.5 nm thick, 72 $\text{mA}/\mu\text{m}^2$ current density 2-2.5 V, breakdown
f_τ	370	520	730	1000	1400 GHz
f_{max}	490	850	1300	2000	2800 GHz
power amplifiers	245	430	660	1000	1400 GHz
digital 2:1 divider	150	240	330	480	660 GHz



InP DHBTs: September 2008



popular metrics :

f_τ or $f_{\max}$ alone

$(f_\tau + f_{\max})/2$

$\sqrt{f_\tau f_{\max}}$

$(1/f_\tau + 1/f_{\max})^{-1}$

much better metrics :

power amplifiers :

PAE, associated gain,
mW/ μm

low noise amplifiers :

$F_{\min}$, associated gain,

digital :

f_{clock} , hence

$(C_{cb} \Delta V / I_c)$,

$(R_{ex} I_c / \Delta V)$,

$(R_{bb} I_c / \Delta V)$,

$(\tau_b + \tau_c)$

Ohmic Contacts Good Enough for 3 THz Transistors

64 nm (2.0 THz) HBT needs $\sim 2 \Omega \cdot \mu\text{m}^2$ contact resistivities

32 nm (2.8 THz) HBT needs $\sim 1 \Omega \cdot \mu\text{m}^2$

Contacts to N-InGaAs*:

<i>Mo</i>	<i>MBE in-situ</i>	<i>0.3 (+/- 0.3) $\Omega \cdot \mu\text{m}^2$</i>
<i>TiW</i>	<i>ex-situ</i>	<i>~ 1 to $2 \Omega \cdot \mu\text{m}^2$</i>

Contacts to P-InGaAs:

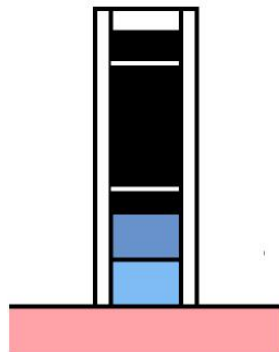
<i>Mo</i>	<i>MBE in-situ</i>	<i>below $2.5 \Omega \cdot \mu\text{m}^2$</i>
<i>Pd/...</i>	<i>ex-situ</i>	<i>0.36 (+/- 0.3) $\Omega \cdot \mu\text{m}^2$</i>

**measured emitter resistance remains higher than that of contacts.*

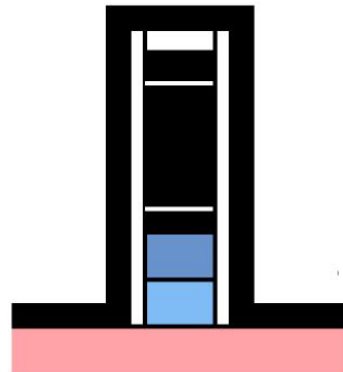
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THz HBTs: MOSFET-like Processes for 64, 32 nm Nodes

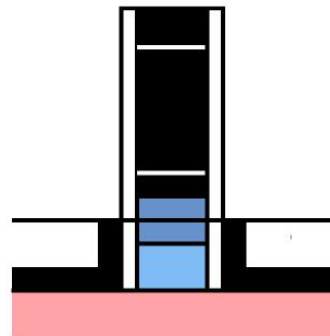
emitter



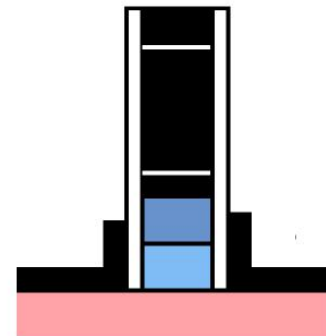
metal



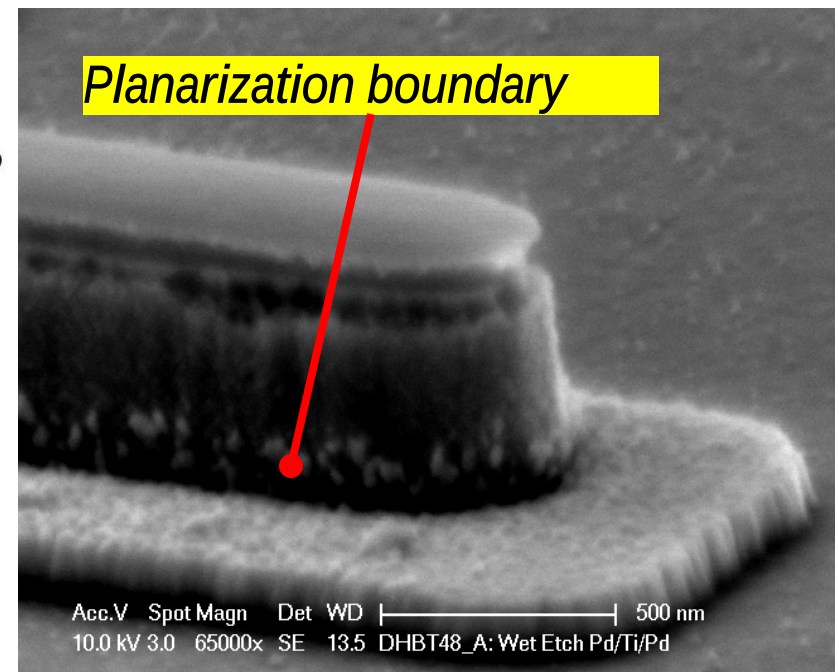
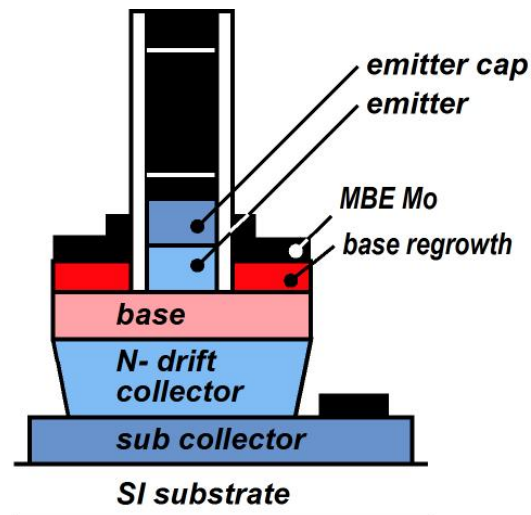
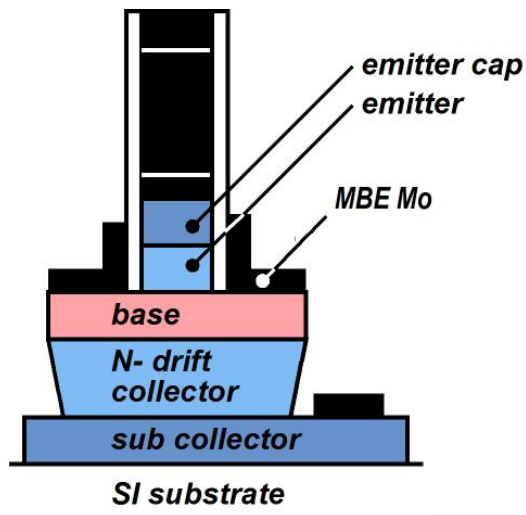
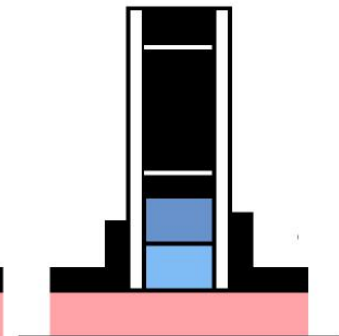
planarize



etch

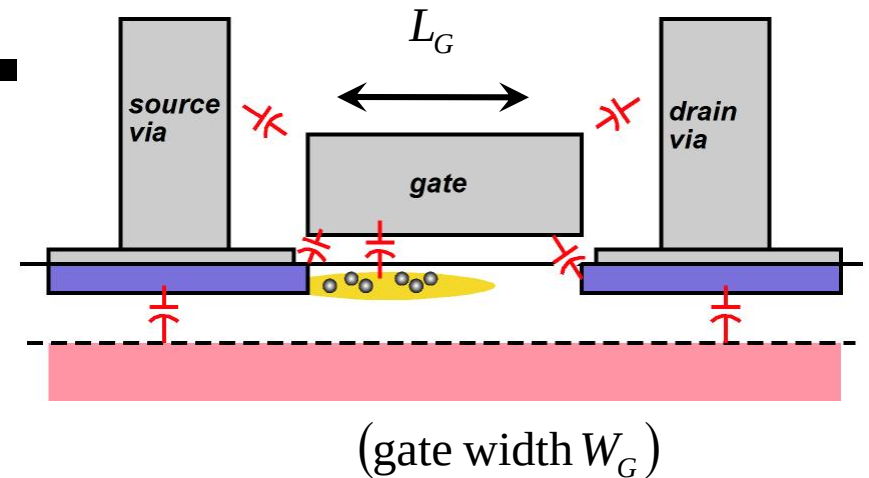


pattern



nm MOSFETs

FET Scaling Laws



Changes required to double transistor bandwidth:

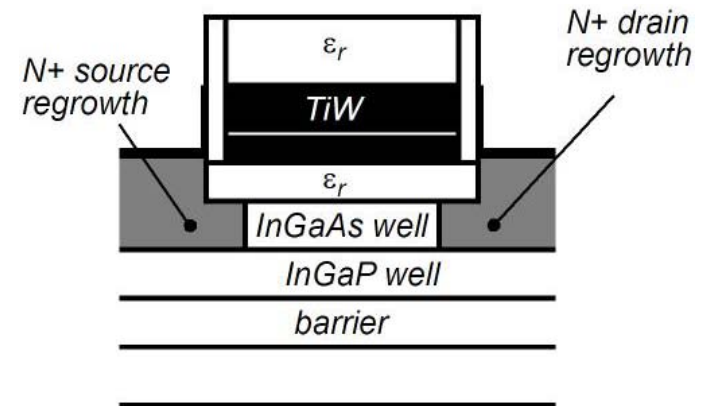
parameter	change
gate length	decrease 2:1
gate dielectric capacitance density	increase 2:1
gate dielectric equivalent thickness	decrease 2:1
channel electron density	increase 2:1
source & drain contact resistance	decrease 4:1
current density (mA/ μm)	increase 2:1

What do we do if gate dielectric cannot be further scaled ?

III-V MOSFETs for VLSI

What is it ?

MOSFET with an InGaAs channel



Why do it ?

low electron effective mass $\rightarrow$ higher electron velocity

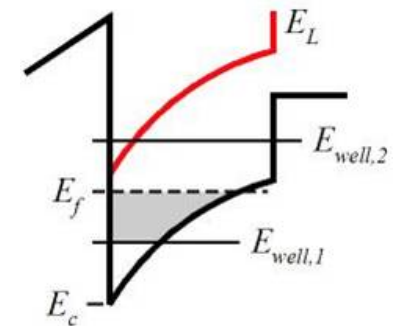
more current, less charge at a given insulator thickness & gate length

very low access resistance

What are the problems ?

low electron effective mass $\rightarrow$ constraints on scaling !

must grow high-K on InGaAs, must grow InGaAs on Si

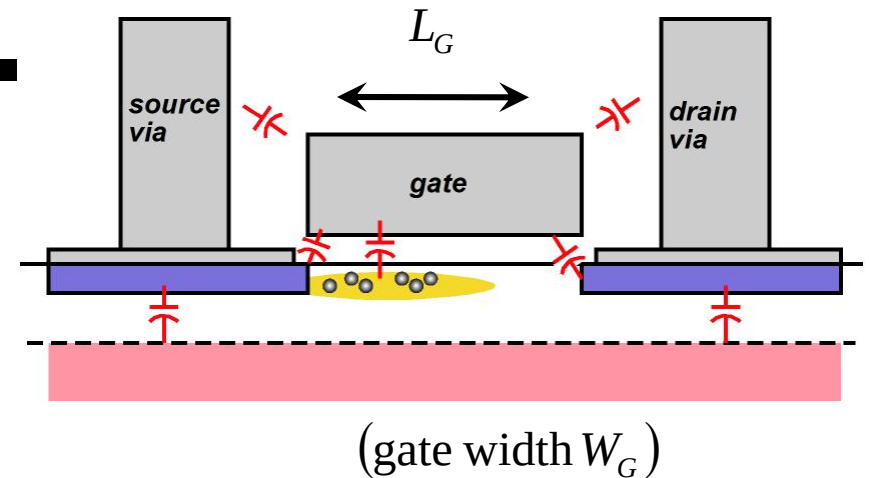


Synopsis

III-V MOSFET might win... if Si gate dielectric cannot scale below 0.5 nm

THz Field-Effect Transistors (THz HEMTs)

FET Scaling Laws



Changes required to double transistor bandwidth:

parameter	change
gate length	decrease 2:1
gate dielectric capacitance density	increase 2:1
gate dielectric equivalent thickness	decrease 2:1
channel electron density	increase 2:1
source & drain contact resistance	decrease 4:1
current density (mA/ μm)	increase 2:1

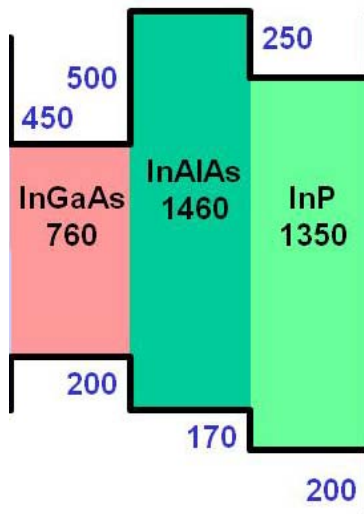
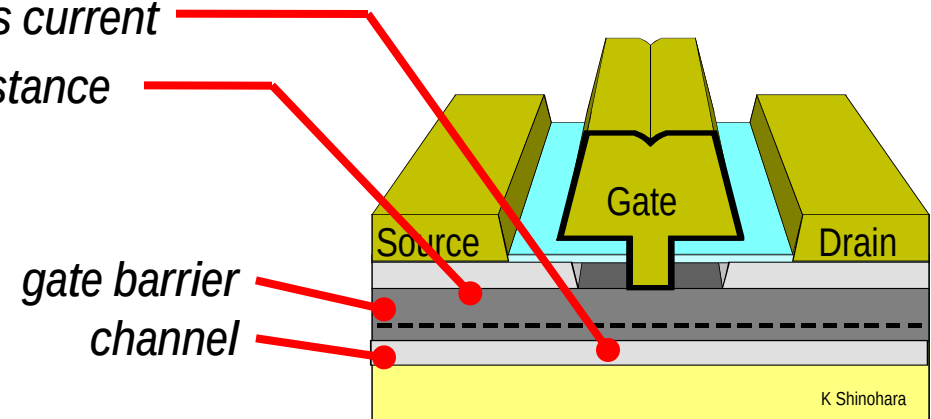
***InGaAs HEMTs are best for mm-wave low-noise receivers...
...but there are difficulties in improving them further.***

Why HEMTs are Hard to Improve

1st challenge with HEMTs: reducing access resistance

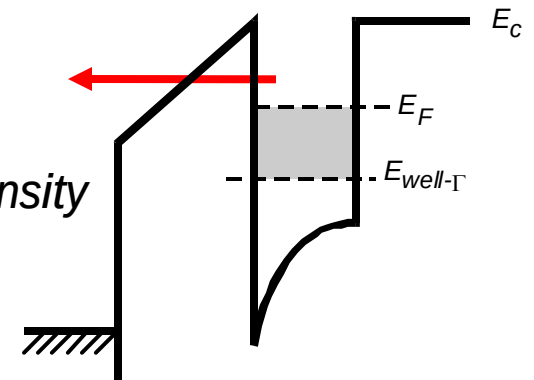
low electron density under gate recess → limits current

gate barrier lies under S/D contacts → resistance



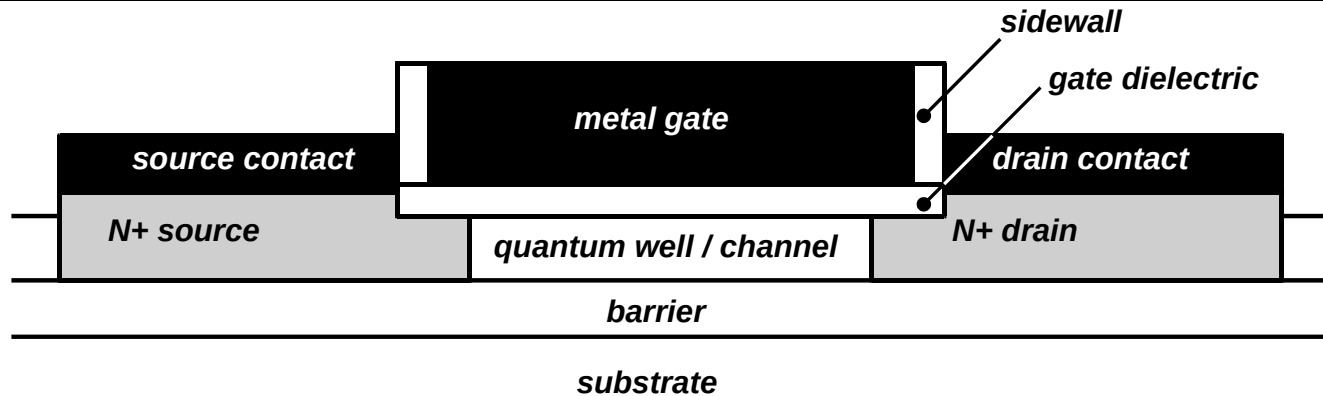
*2nd challenge with HEMTs:
low gate barrier*

*high tunneling currents with thin barrier
high emission currents with high electron density*



III-V MOSFETs do not face these scaling challenges

InGaAs MOSFETs as THz Low-Noise Amplifiers



Why ?

Much lower access resistance in S/D regions

Higher gate barrier → higher feasible electron density in channel

Higher gate barrier → gate dielectric can be made thinner

Estimated Performance (?)

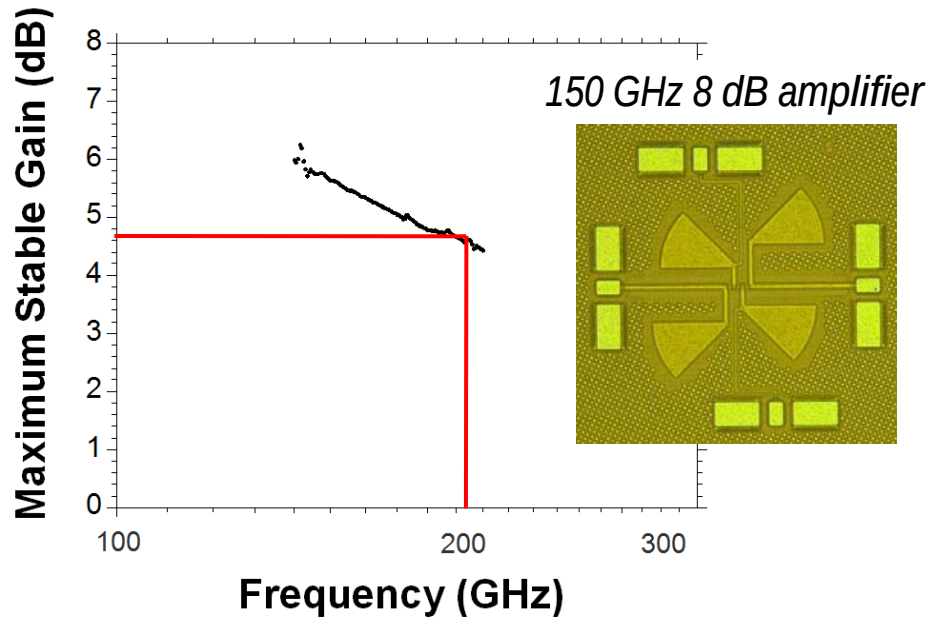
2 THz cutoff frequencies at 32 nm gate length

VSLI for mm-wave & sub-mm-wave systems

Billions of 700-GHz Transistors → Imaging & Arrays

65 nm CMOS: ~5 dB gain @ 200 GHz

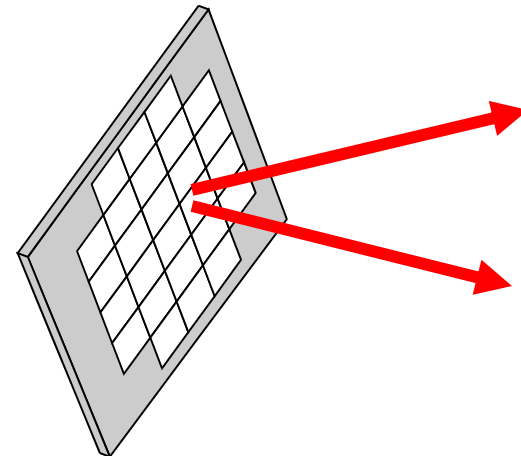
22 nm will be much faster yet.



What can you do with a few billion 700-GHz transistors ?

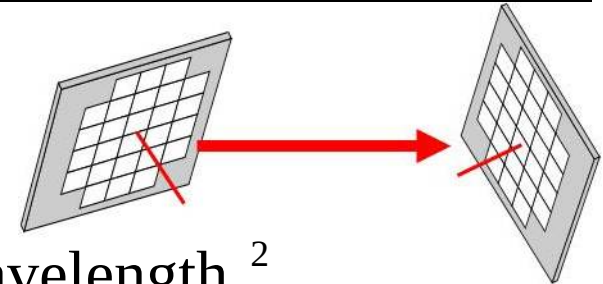
Build Transmitter / Receiver Arrays

*100's or 1000's of transmitters or receivers
...on < 1 cm² IC area
...operating at 100-500 GHz.*



Billions of 700-GHz Transistors → Imaging & Arrays

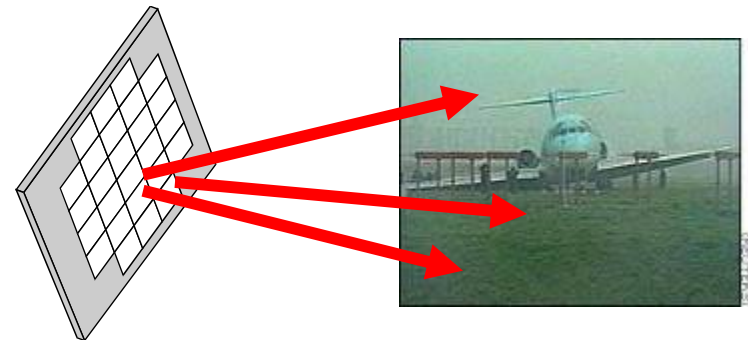
Arrays for point-point radio links:



$$\text{bit rate} \cdot \text{distance}^2 \propto (\# \text{ array elements})^2 \cdot \text{wavelength}^2$$

Arrays for (sub)-mm-wave imaging :

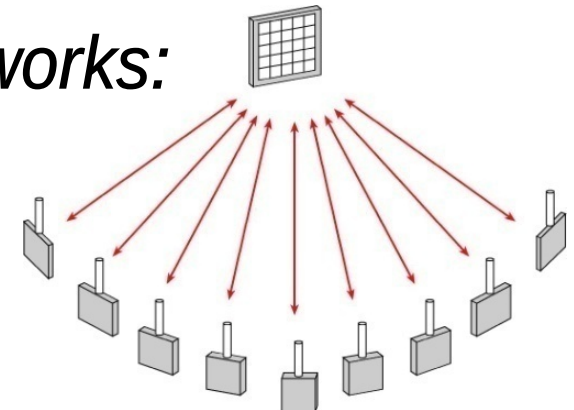
resolvable pixels = # array elements



Arrays for Spatial-Division-Multiplexing Networks:

independent beams = # array elements

$$\leq \frac{4 \cdot \text{array area}}{\text{wavelength}^2}$$



It's a great time to be working on electronics !

Device scaling (Moore's Law) is not yet over.

*Challenges in scaling:
contacts, dielectrics, heat*

*Multi-THz transistors:
for systems at very high frequencies
for better performance at moderate frequencies*

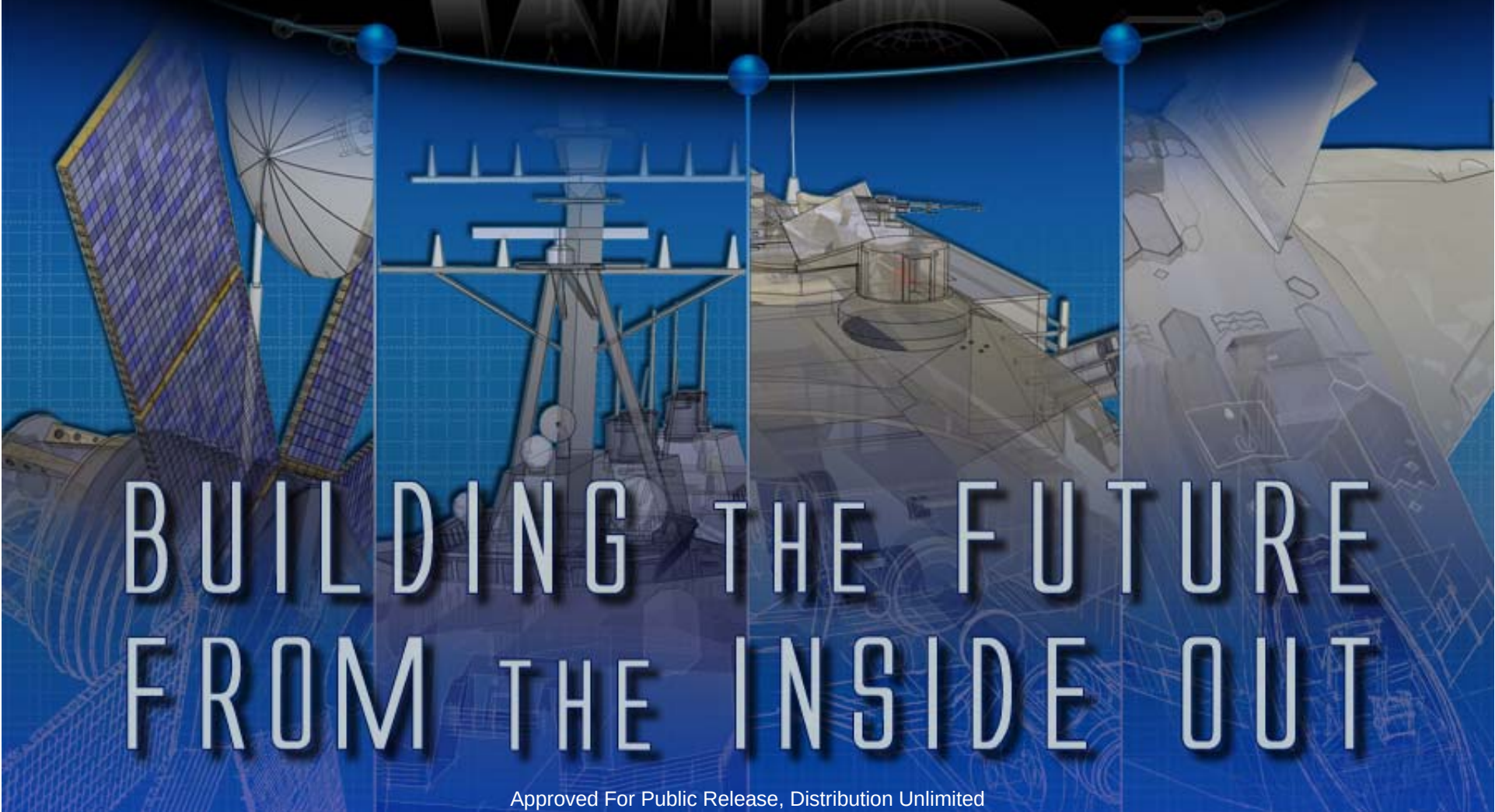
*Vast #s of THz transistors
complex systems
new applications.... imaging, radio, and more*

MICROSYSTEMS TECHNOLOGY OFFICE

MTD SYMPOSIUM

The logo for the Microsystems Technology Office (MTO) Symposium. It features the letters 'MTD' in a large, bold, metallic font. The 'D' is stylized with a globe in the center, and the word 'DARPA' is written across it. Circuit traces extend from the 'M' and 'D'. Below 'MTD' is the word 'SYMPOSIUM' in a smaller, white, sans-serif font. The entire logo is set against a dark background with a reflection effect below it.

BUILDING THE FUTURE
FROM THE INSIDE OUT

The background of the poster is a collage of various technological and infrastructure elements. On the left, there's a large satellite dish and a solar panel array. In the center, a complex antenna structure is visible. On the right, there's a large, modern building with a glass facade. The entire background is set against a blue gradient with a grid pattern. A thin blue line with three blue spheres runs horizontally across the middle of the image, passing through the collage.

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