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An Ultra Low Power 180-degree, 1-bit phase shifter using MOSFETS

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Abstract: *An ultra low power 180-degree , 1-bit phase shifter has been designed using Agilent's Advanced Design Software (ADS) co-simulation. Silicon-on-Insulator (SOI). MOSFETs were used as the switching elements because of their low current draw and low capacitance. A 1-bit 0, 180-degree phase shift has been realized with only two MOSFETs, simplifying manufacture and decreasing power.*

Keywords: phase shifter, microstrip, silicon-on-insulator (SOI), MOSFET switch.

I. Introduction

A phase shifter switchable between 0 and 180 degree is useful for many applications, especially phase modulators for BPSK modulation. Low power is desired to minimize size, weight and space of systems that require batteries and long persistence. Design of switched transmission line phase shifters usually requires two single-pole, double-throw (SPDT) switches. SPDT switches can be realized in a wide variety of ways, using FET, diode, or MEM (micro-electro-mechanical) switches. GaAs MESFETs, HEMTs, P-HEMTs or P-I-N diodes have been used to realize phase shifters [3.], but suffer from high current draw and depletion-mode behavior, requiring negative voltages or DC biasing of the transmission lines to turn off. MEM switches either require high voltages to actuate or are difficult to integrate. Although reflection-type phase shifters using hybrid couplers and two switching elements have been reported, this type was discarded after insertion loss of designs using this architecture was found to be too high. Single switch type transmission line phase shifters can also be designed, but are limited to phase angles of smaller than 45 degrees [3.]. MOSFETs are the ideal choice for low-power designs because they do not draw any DC current through their gate, and the only power used is CV^2f. Limitations of MOSFETs for this application are the capacitance of the MOS structure, its relatively high resistance, and its limited power handling capability. This paper describes a switched line phase shifter using only two MOSFETs to realize an ultra low power, bi-directional, 1-bit, 180- degree phase shifter.

II. Phase Shifter Design

The design is shown schematically in Figure 1. The conventional switched line configuration can be reduced to a single switch topology as shown in Figure 1 for the special case of a 180-degree phase shift. Ideally. a reflective SPDT switch will present an open circuit to the port. If the line length is a multiple of a half wavelength, the open circuit will transform to an open circuit at the junction on the right hand side of the circuit in Figure 1. However, a non-ideal reflective SPDT switch will have near-unity, off-port reflection coefficient magnitude, and also non-zero phase. The line length is adjusted to compensate so that the phase difference between the two paths is a multiple of a half-wavelength. For a SPDT switch, only two MOSFETs are necessary (Figure 2).

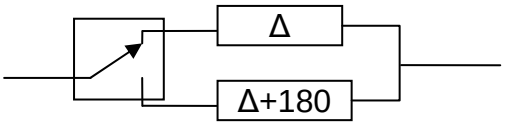

Figure 1: Schematic of a two transistor, 1-bit, 180-degree phase shifter.

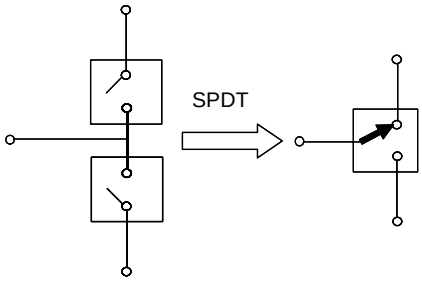

Figure 2: Schematic diagram showing how two individual switches make up a SPDT switch.

Using microstrip construction and Dupont's Pyralux 9121 as a substrate, Agilent's Advanced Design System (ADS) was used to simulate transmission line characteristics using Momentum, and co-simulated with measured MOSFET characteristics taken using on-wafer measurements with an 8510C and Cascade microprobe station.

A. SOI MOSFET Characteristics

SOI MOSFETs have reduced parasitics from a bulk process. RF functions are then readily realized in SOI, which has excellent isolation properties due to the total isolation of silicon islands from one another. This enables integration of digital circuitry and RF on the same die, enabling more system-on-a-chip applications.

SANDIA National Lab's radiation-hardened, five-level metal, 0.35-um process was used to produce the MOSFETs used in this design. The width of the transistors was 200 microns, and their length was 0.5 microns. These dimensions were chosen to provide a good trade-off of capacitance (isolation) and resistance (insertion loss) for the switching element at the design frequency of 8 GHz. The transistor also has a body contact using a T-gate structure to allow the device to be used in a transmission line series configuration without requiring biasing of the transmission lines. Figure 3 shows measured data of S21 for the Sandia FET. At 8 Ghz, an insertion loss at a gate voltage of 3 volts is 2 dB, and it's isolation is 7.4 dB. These numbers include pad parasitics, and with a higher resistivity substrate, can be improved upon.

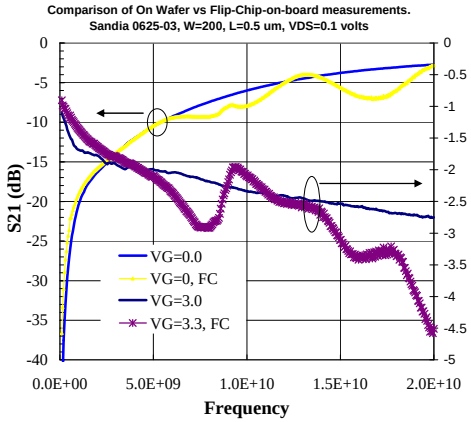

Figure 3: Measured S21 vs. frequency of 200- x 0.5-um MOSFET. On-wafer and flip-chip onboard measurements.

B. Flip-Chip Onboard Process

To introduce minimal packaging parasitics to the MOSFETs, a flip-chip on board technique was developed that avoids inductance introduced by relatively long bond wires, and keeps the rest of the design compact in area. The MOSFETs are diced out into 1- x 1-mm die, and gold stud-bumps are attached to the source, drain, gate, and body pads. The die is placed onto the PCB traces directly with conductive epoxy (Figure 4). Measured characteristics of the flip-chipped die are shown in Figure 3 showing slight changes from on-wafer measurements, but still with acceptable RF characteristics.

Figure 4: Side view of gold stud bumps attached to the die pads (left). Flip-chipped MOSFET die on printed circuit board (right).

C. Phase Shifter Simulation

Using the measured on-wafer MOSFET characteristics, Momentum and ADS were used to perform a co-simulation. Matching to 50 ohms was accomplished through a ¼-wavelength impedance transformation in microstrip. Figure 5 (left) shows the layout and ports in Momentum. Ports 1 and 2 are "single" ports, while ports 3 through 6 are "internal" ports and serve as the connections to the flip-chipped transistors. Figure 5 (right) shows the MOSFET measured data components placed on the internal ports for switches in the "off" (VG = 0 volts) and "on" (VG = 3 volts) states. Table 1 summarizes the design specifications and the simulated results.

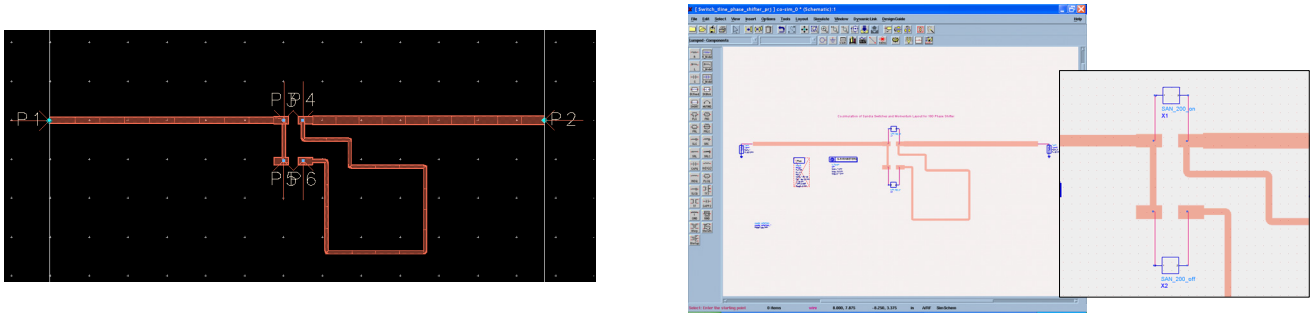

Figure 5: Left: Momentum layout of phase shifter with internal ports where the MOSFET die are positioned. Right: ADS co-simulation environment showing a Momentum "look-alike" layout component and the attached MOSFET S-parameter components.

Table 1. Specifications and simulated results.

	Specification	Simulated Results
Frequency	8 GHz	8 GHz
Insertion Loss	< 5 dB	4.1, 5.5 dB
Phase Shift	Steps 0°and 180°	Delta= 182.5°
VSWR, 50 Ohm	< 1.5:1 input and output	1.47 :1
Control	0,+3.3V	0, +3.3V

III. Phase Shifter Measurements:

Figure 7 shows the constructed phase shifter with two MOSFET die using the flip-chip technique described above. Two control lines and two ground lines are visible in the photograph, coming in from the top and bottom. The ground lines contact the body of the SOI MOSFET through a "T-gate" body tie. This simplifies the construction of the phase shifter since no DC biasing of the transmission lines is necessary. A single sided board is all that is necessary for the phase shifter construction using Dupont's Pyralux 9121 bonded onto FR4 as a substrate.

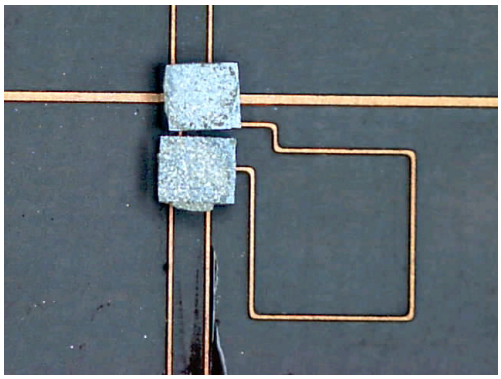

Figure 7: 180-degree phase shifter.

Figure 8 shows the measured and simulated return loss from both ports for the 0 and 180 states. Figure 9 shows the measured and simulated phase differences between the two states. As can be seen, the simulations for return loss do not match that closely with measurements while the phase difference is within 2 degrees at the center (design) frequency. Reasons for the disparity are possible variations in the MOSFET characteristics from the measured on-wafer MOSFETs and the MOSFETs flip-chipped onto the phase shifter, interactions of the control lines that were not included in the co-simulation, or the flip-chip parasitics. However, for proof-of-concept, the measured results show that a 1-bit, 180-degree phase shifter has been realized, and that simulation is close to describing the observed behavior.

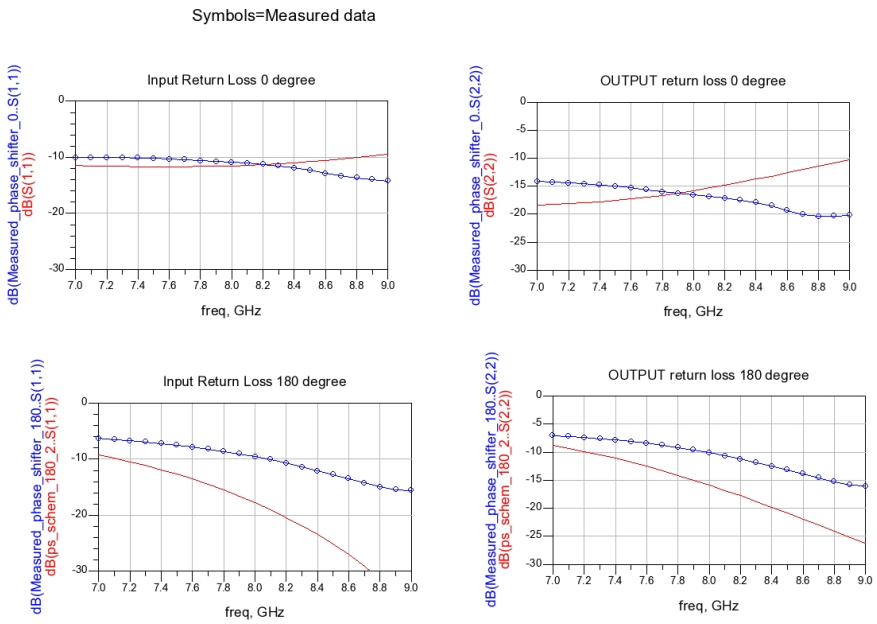

Figure 8: Measured and simulate input and output Return Loss for 0- and 180-degree states of the phase shifter.

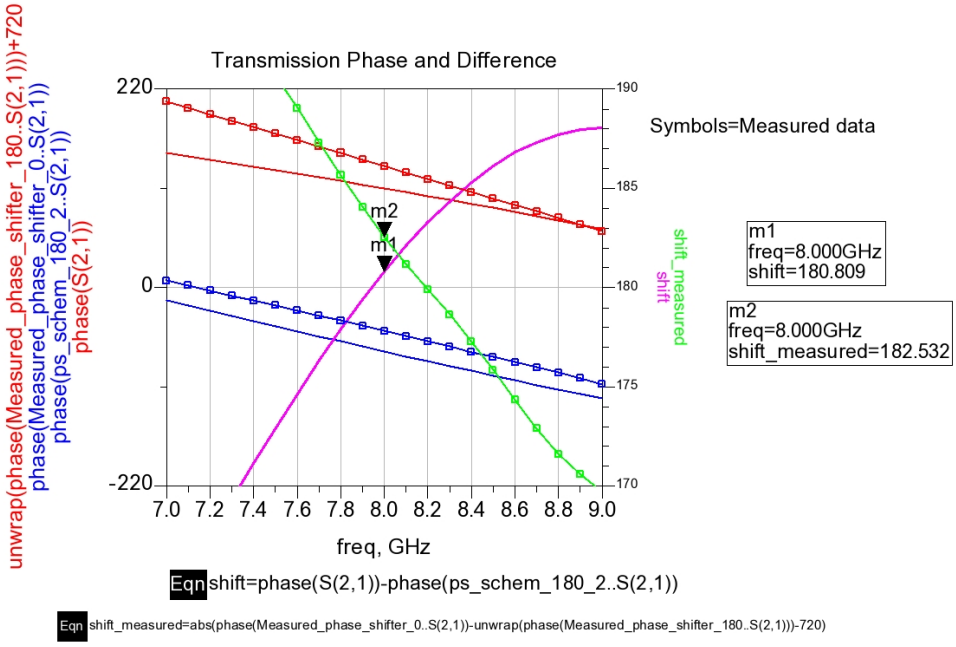

Figure 9: Measured and simulated Phase and Phase Difference of the 1-bit phase shifter.

IV. Coplanar waveguide (CPW) to microstrip transition:

To test the phase shifter, a coplanar waveguide to microstrip transition was necessary. A tapered transition from GSG probes to microstrip was designed to minimize reflections. An exponential taper is one method to improve a transition from one impedance to another [2.], but since exponential curves are difficult to implement in most layout tools, a radial arc was used instead (Figure 11). Via through-holes are used to stitch the grounds to the backplane ground all along the CPW transition to obtain good grounding.

An improved layout was made using ideas presented in [4.]. To improve the transition, vias were added in the y direction, and the ground spacing was kept constant for a longer distance before tapering. A picture of the initial and re-designed launch is shown in Figure 12. Measured reflection for both layouts is shown in Figure 13. The improved layout has reduced reflections by 5 to 10 dB from 8 to 20Ghz.

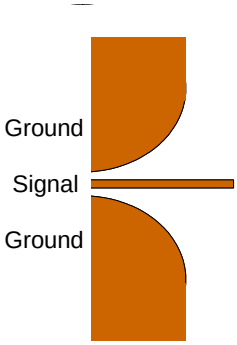

Figure 10: Layout of Ground-Signal-Ground (GSG) to microstrip launch

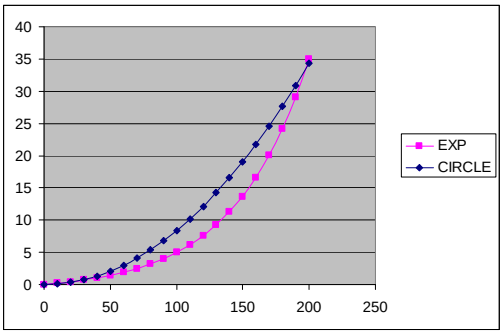

Figure 11: Comparison of radial and exponential tapering for CPW to microstrip transition. Units are in Mils.

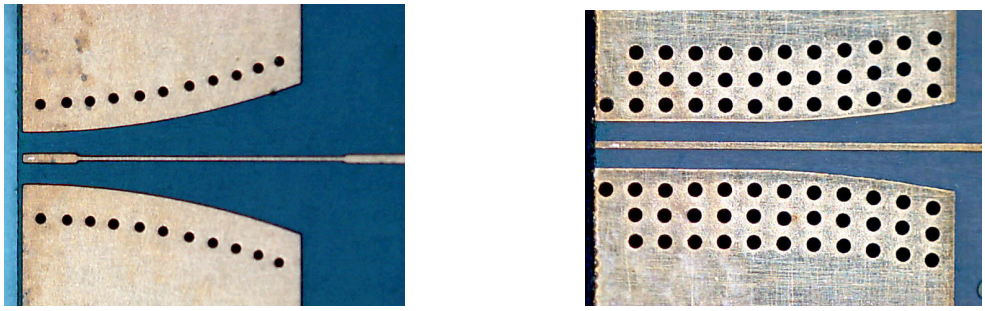

Figure 12: Left: Photograph of first attempt at GSG to microstrip launch. Right: Photograph of improved layout.

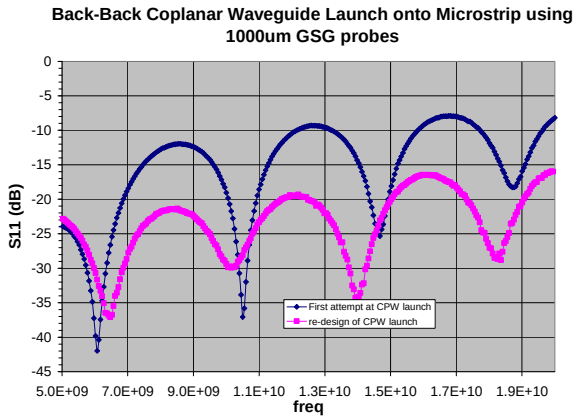

Figure 13: S11 vs. frequency for initial and improved GSG to microstrip launch.

V. Conclusion

A 0- and 180-degree phase shifter has been realized with only two SOI MOSFETs and microstrip transmission lines. The phase shifter is designed on a standard thin film PCB material. Performance can be improved by optimizing the switches length and width to improve insertion loss at the expense of isolation. The small size enables the phase shifter to fit in between patch antenna elements. The technique is useful for small, low-power, and low-profile devices.

A CPW to microstrip launch has also been designed and fabricated in the same PCB material to create a low return loss transition between GSG micro probes and the device under test.

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Mission Area: Microelectronics

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