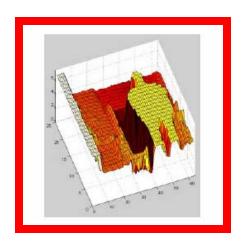
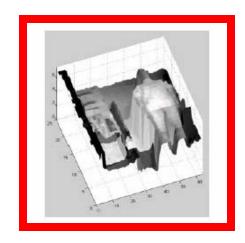
ORTHOGONALLY MODULATED CMOS READOUT INTEGRATED CIRCUIT FOR IMAGING APPLICATIONS





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Electrical and Computer Engineering Department

University of Delaware



December 13, 2004

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ORTHOGONALLY MODULATED CMOS READOUT INTEGRATED CIRCUIT FOR IMAGING APPLICATIONS



- Introduction and motivation
- Contribution Phase I: Proof of principle
 Orthogonal encoding readout system description
 Prototype system design and verification
 Conclusions
- Contribution Phase II: Improving the system performance

Readout cell improvements

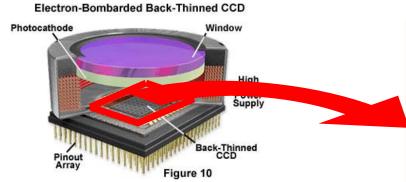
Transimpedance amplifier integration

Conclusion and brainstorm on further improvements



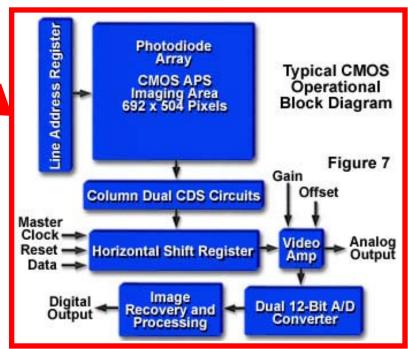


Read Out Integrated Circuit ROIC



ROIC may include:

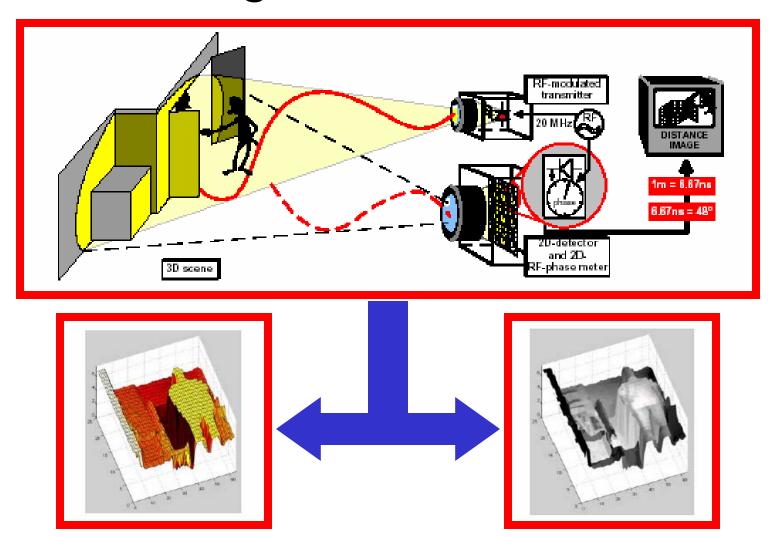
Amplifier electronics
Control signal generators
Analog-Digital Conversion
On-chip Digital Signal Processing





Distance information: a time of flight measurement

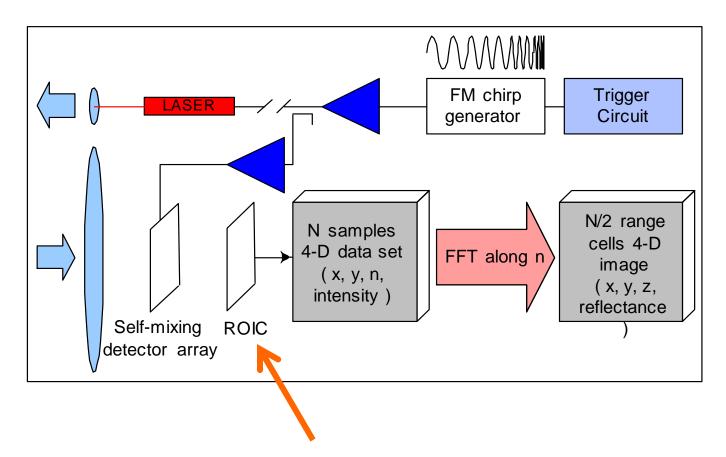








FM/CW LADAR system



Motivation: Readout Integrated Circuit ROIC for active/passive imaging systems





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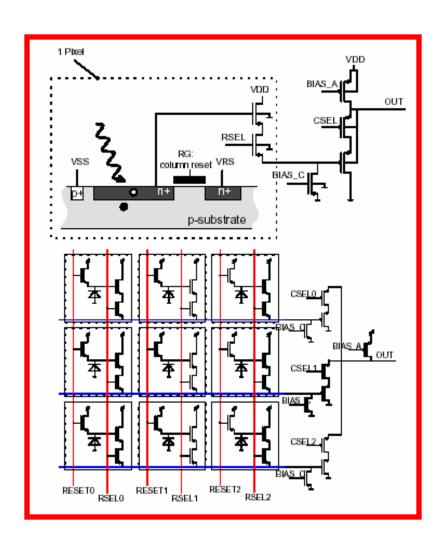
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ROIC conventional architecture





Time Domain Multiple Access

Control signals access every readout cell in a time scheduled manner, sampling the voltage signals and transferring them to the readout bus.

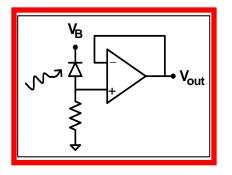
It requires faster electronics for bigger photodetector arrays.

Each readout cell must be capable of storing the required charge, which becomes a problem for big array sizes (1024x1024).

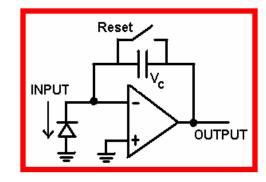


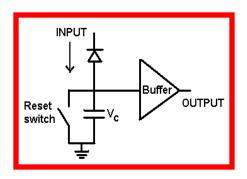
Read Out Cell Architectures



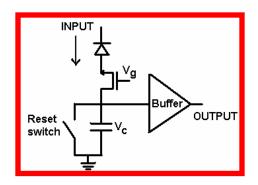


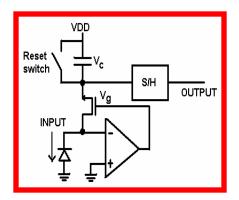
From Direct Injection to Capacitive TransImpedance Amplifier







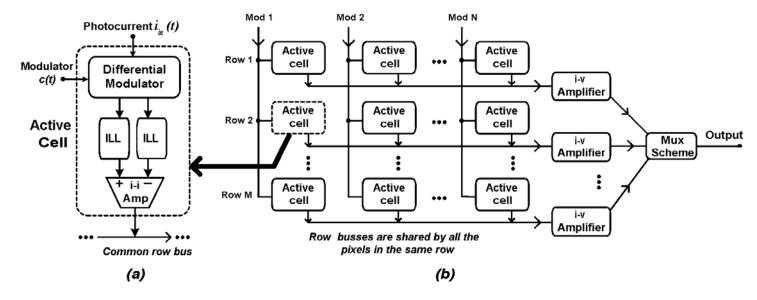






ROIC proposed architecture





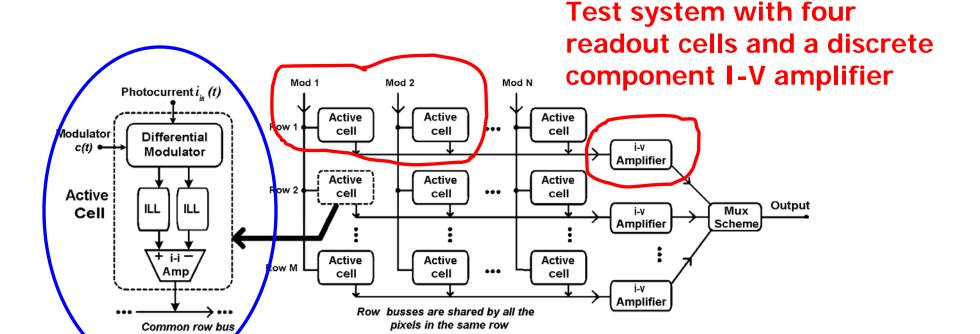
Orthogonal encoding ROIC

- Each column is multiplied by a unique code, and the multiplied signals are summed in the row common bus
- Codes are chosen to minimize cross talk
- Current-to-voltage amplifier per row
- Multiplexer scheme to generate single data stream



Orthogonal Encoding ROIC First Phase Design Tasks





(b)

Design of the Active Readout Cell

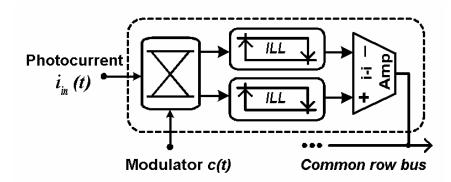
(a)

To design and fabricate a test chip for a proof of principle of the active 2D readout technique.



Active Readout Cell: Design Requirements





Readout cell for orthogonal encoding

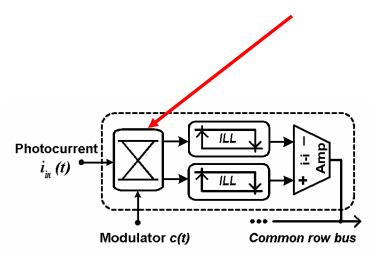
Multiplies the input current by the code Provides detector virtual ground Couples the detector impedance to the bus Reduces charge injection noise



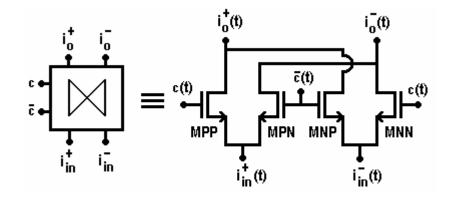
Active Readout Cell: Implementation



Differential code multiplier



Readout cell for orthogonal encoding



$$i_{o}^{+}(t) = i_{in}^{+}(t) \cdot c(t) + n_{c} + i_{in}^{-}(t) \cdot \overline{c}(t) + n_{\overline{c}},$$

$$i_{o}^{-}(t) = i_{in}^{+}(t) \cdot \overline{c}(t) + n_{\overline{c}} + i_{in}^{-}(t) \cdot c(t) + n_{c},$$

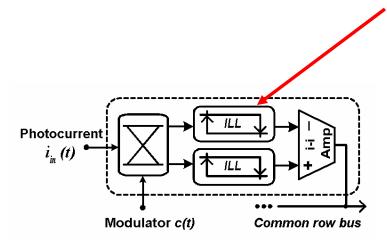
Differential output current $i_{od}(t) = i_o^+(t) - i_o^-(t) = [i_{in}^+(t) - i_{in}^-(t)] \cdot [c(t) - \overline{c}(t)],$

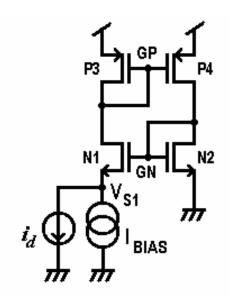


Active Readout Cell



Current Locked Loop ILL





Characteristics

Detector virtual ground

$$\frac{v_{g1}}{v_{s1}}\Big|_{low\ freq.} = \frac{-g_1g_4}{g_2g_3 - g_1g_4} = \frac{-\gamma}{1 - \gamma}, \text{ with } \gamma = \frac{g_1g_4}{g_2g_3}$$

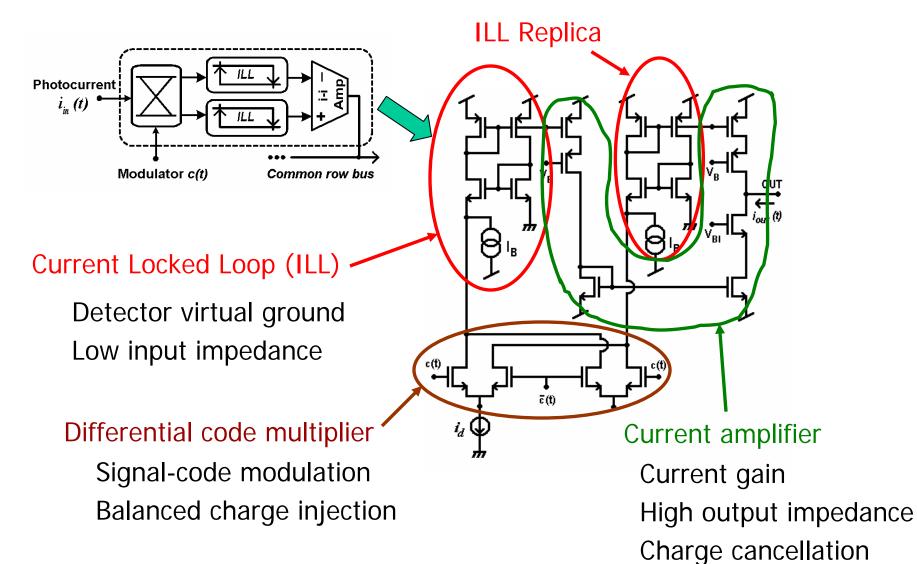
Low input impedance

$$Z_{in}\big|_{low\ freq.} = \frac{1}{g_1}(1-\gamma)$$



Active Readout Cell

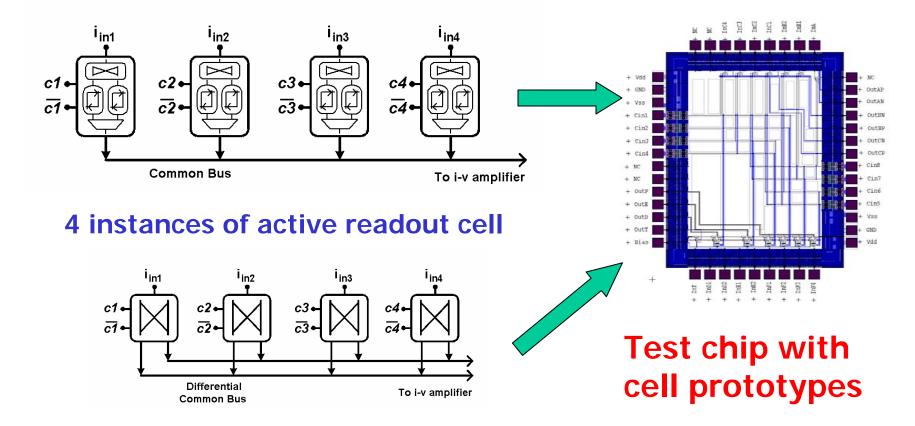






Test chip implementation



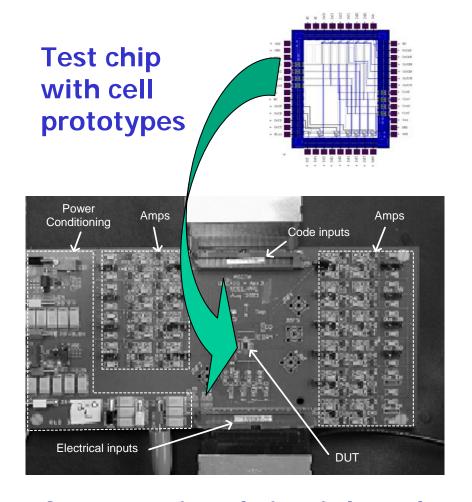


4 instances of cell with input modulator only



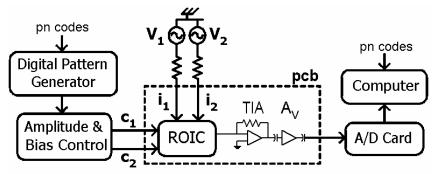
Prototype system testing





Custom printed circuit board for electro-optical testing

ROIC electrical verification set up



Code signals generated and conditioned externally

Voltage sources + Resistors emulate electrical current inputs

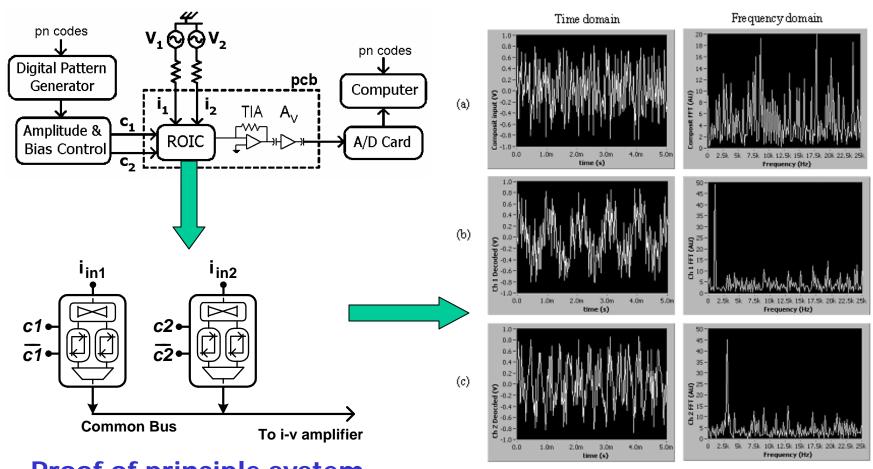
High-gain off-chip transimpedance amplifiers on the pcb

Data is acquired and processed in the computer



Verification Results





Proof of principle system with 2 encoding cells

Test results



Prototyping phase conclusion



Satisfactory results with the 2 encoding cells experiment confirm validity of the orthogonal encoding scheme for readout circuits

Applicability extends to passive imaging systems

Depending on the system conditions, the orthogonal encoding architecture is advantageous with respect to the conventional time-multiplexed scheme

Integrating the transimpedance amplifiers with improved versions of readout cells should enhance noise performance of the overall system



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Readout cell improvements

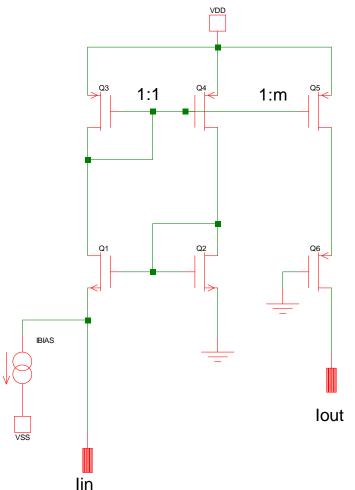
Transimpedance amplifier integration

Conclusion and brainstorm on further improvements





ILL current gain and noise performance



$$\overline{i_{Q3}^2} = 4kT\gamma g_3$$

$$\overline{i_{Q3}^{2}} = 4kT\gamma g_{3}$$

$$\overline{i_{out}^{2}} = 4kT\gamma g_{5} \left(1 + \frac{g_{5}}{g_{3}}\right) = 4kT\gamma g_{3}m(1+m)$$

Input referred noise

$$\overline{i_{ieq}^2} = \frac{\overline{i_{out}^2}}{m^2} = 4kT\gamma g_3 \frac{(1+m)}{m}.$$

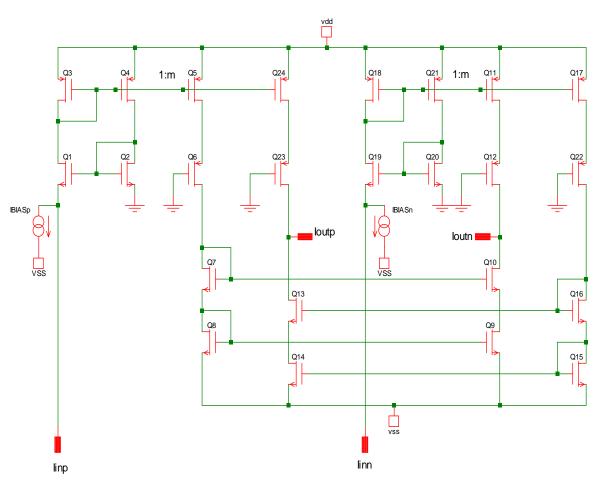
Minimize g_3

Maximize current gain *m*





Fully differential architecture



Additional current mirror for complementary output

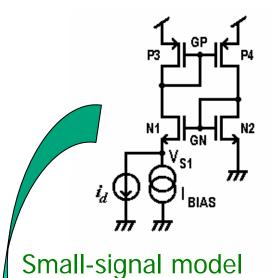
Improved charge injection cancellation and offset

Noise from cascode mirrors is minimized





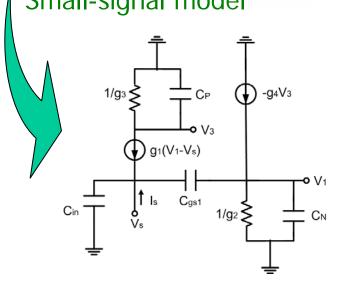
Input impedance engineering

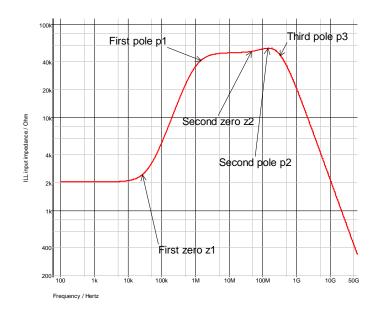


From small-signal model, solve for Z_{in}

$$Z_{in} = \frac{V_s(s)}{I_s(s)} = \left(\frac{1}{sC_{in}}\right) / \frac{(g_3 + sC_P)(g_2 + s(C_{gs1} + C_N)) - g_1g_4}{(g_1 + sC_{gs1})(g_3 + sC_P)(g_2 + sC_N)}$$

Input impedance without C_{in}



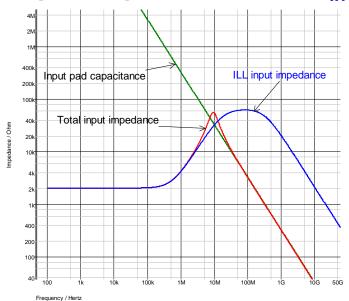






Input impedance engineering (cont'd)

Input impedance with C_{in}



ILL pole-zero analysis

$$z_{1} = \frac{K_{z} - C_{gs1}g_{3} - C_{N}g_{3} - C_{P}g_{2}}{2C_{P}(C_{gs1} + C_{N})}$$

$$z_{2} = \frac{-K_{z} - C_{gs1}g_{3} - C_{N}g_{3} - C_{P}g_{2}}{2C_{P}(C_{gs1} + C_{N})}$$

$$p_1 = -\frac{g_3}{C_P}$$

$$p_2 = -\frac{g_2}{C_N}$$

$$p_3 = -\frac{g_1}{C_{gs1}}$$

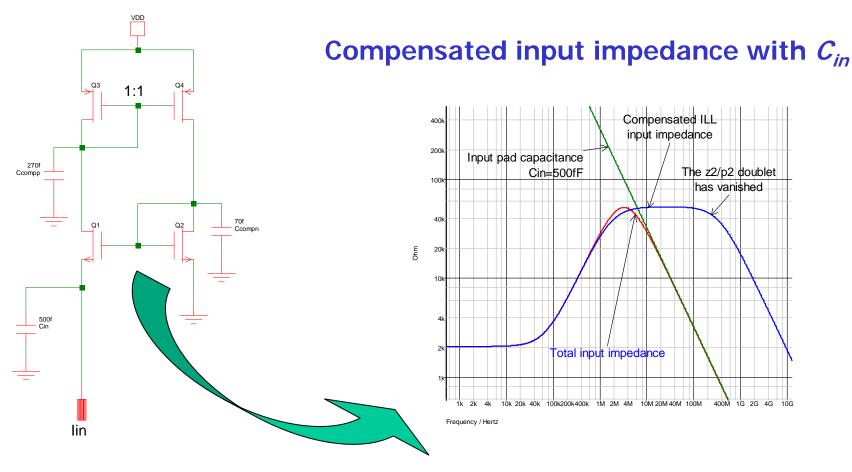
$$\mathbf{K}_{Z} = \sqrt{C_{gs1}^{2}g_{3}^{2} + 2C_{gs1}(C_{N}g_{3}^{2} + C_{P}(2g_{1}g_{4} - g_{2}g_{3})) + C_{N}^{2}g_{3}^{2} + 2C_{N}C_{P}(2g_{1}g_{4} - g_{2}g_{3}) + C_{P}^{2}g_{2}^{2}}$$

 C_P controls p_1 and z_1 , but also moves z_2 to the left C_N moves p_2 close to z_2 , canceling its effect p_3 determines overall gain-bandwidth





Input impedance engineering (cont'd)



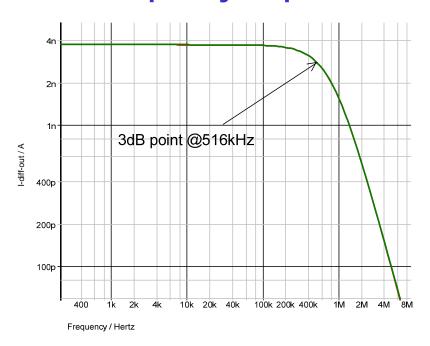
 $C_P = 270 \text{fF}$ and $C_N = 70 \text{fF}$ compensate the input impedance for $C_{in} = 500 \text{fF}$



Improved Active Readout Cell Performance

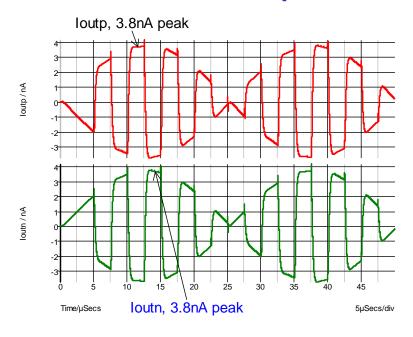


Frequency response



Designed for 500kHz code bandwidth (16 cells)

Transient response



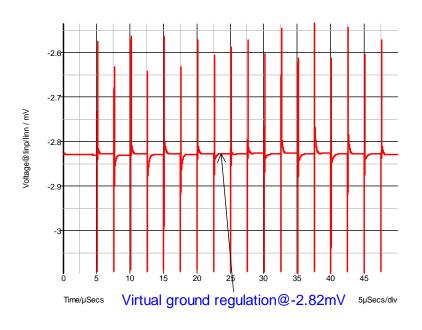
Current gain of 3.8A/A



Improved Active Readout Cell Performance

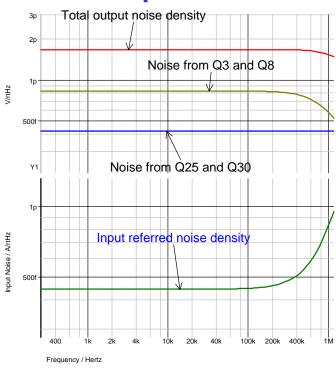


Virtual ground regulation



Between -3.1mV and -2.6mV

Noise performance



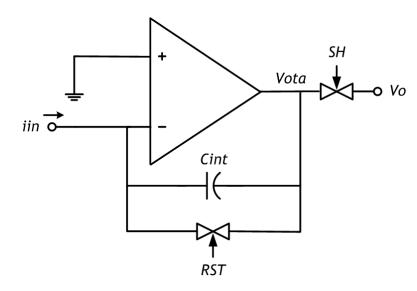
Input referred noise 400fA/rtHz



Transimpedance amplifier implementation

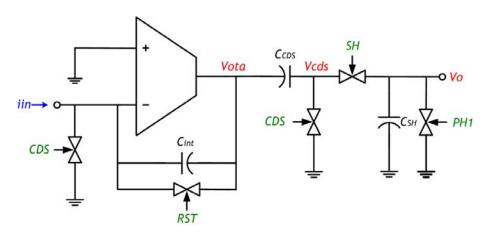


Capacitive TIA (CTIA)



RST switch injects charge and produces sampling (kT/C) noise

CTIA with correlated double sampling (cds)



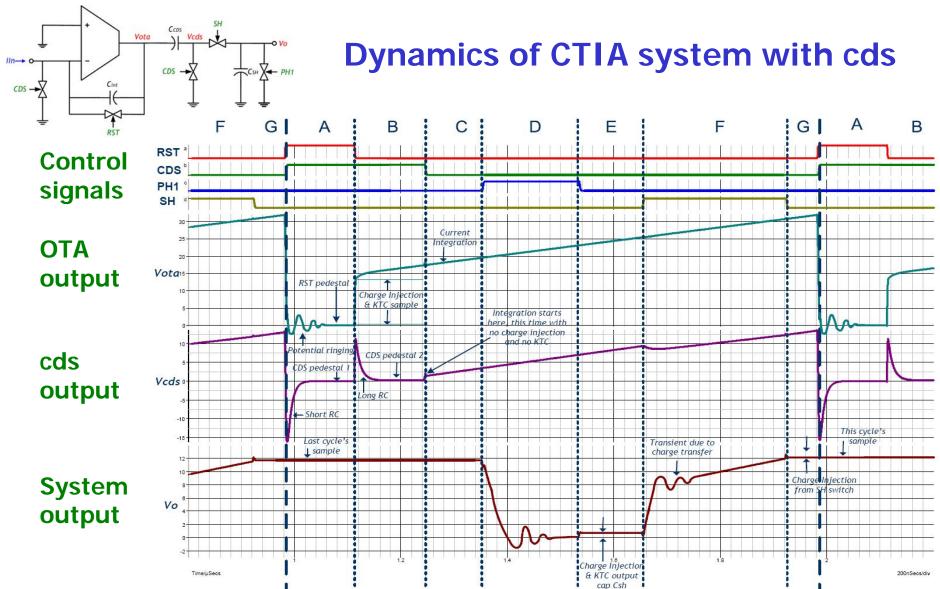
CDS structure removes sampling noise

SH capacitor produces voltage divider



CTIA system-level implementation



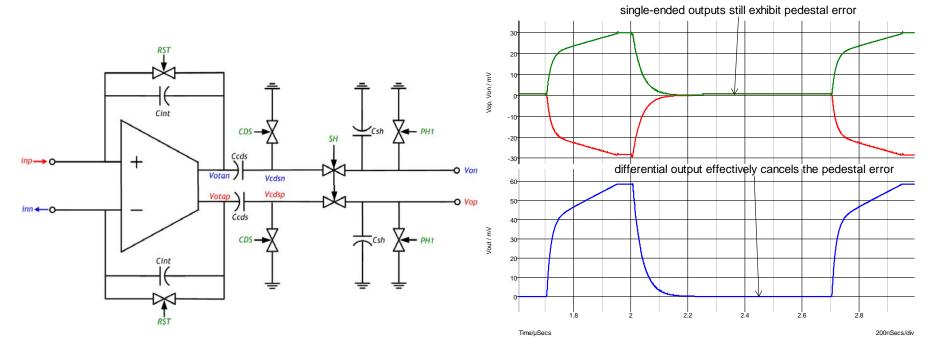




CTIA system-level implementation



Advantages of fully differential CTIA system



Fully differential CTIA system

Transient response of

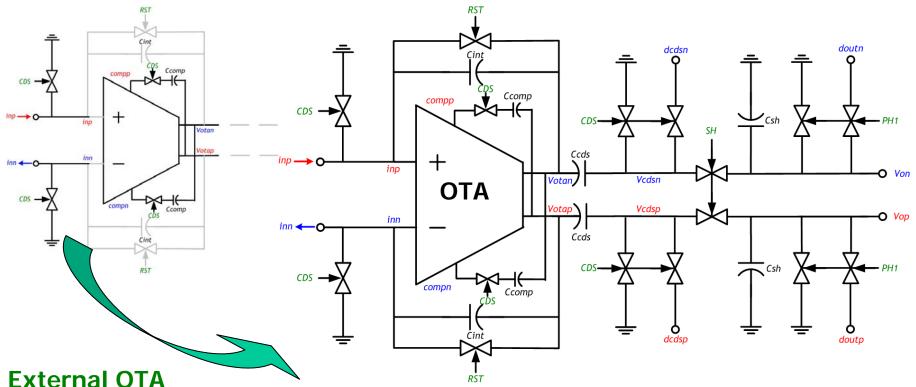
Single-ended vs. Differential output



CTIA system-level implementation



External OTA compensation and sizing of switches and capacitors



External OTA compensation

Input stabilization switches

 $C_{CDS} = 5pF$, $C_{SH} = 1pF$, $C_{comp} = 3pF$, $C_{int} = 50fF$

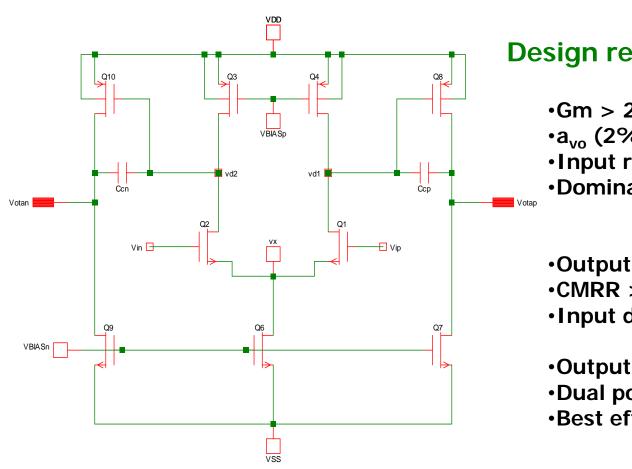
Switches designed for worst-case scenario $R_{\text{SW}}\!\sim\!1\text{k}\Omega$



OTA circuit-level implementation



2-stage Miller compensated OTA, design requirements



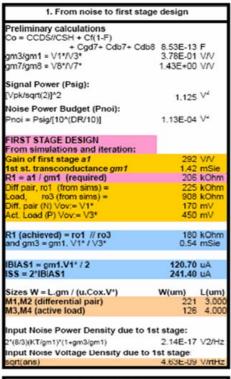
Design requirements

- •Gm > 250mSie
- •a_{vo} (2% settling accuracy) > 40k
- •Input referred noise < 5nV/rtHz</p>
- Dominant pole and non-dominant pole more than three decades apart
- Output common-mode < 10mV
- \cdot CMRR > 60dB
- Input differential capacitance not to exceed 15pF
- Output swing of 2.4Vpk-pk
- Dual power supplies of ±2.5V
- Best effort on power consumption and layout area





ccuracy:= E			
Vstep		2.00% 5.00E-08 40.00	sec dB V/V V
Initial d	esign knobs		
Cs) Cp) (assumed) DS cap) cap) t (Vpk-pk) ¹		1.50E-11 5.00E-12 1.00E-12 3.00 0.80	F
Cf+Cp)		1.33E-03 7.51E+02	V/V V/V
ture itor parameters	1.38E-23 300 1.60E-19 NMOS 2.46E-15 2.01E-16	PMOS 2.38E-15 2.61E-16	\$#% K C F/um^2
	cop Gain:= c = Vstep = VSD= -VSS Initial d ck (Cf) (Cs) (Cs) (Cs) (Cs) (Cs) (Cs) (Cs) (Cs	Initial design knobs (Cs) (Cs) (Cs) (Cs) (Cs) (Cs) (Cs) (C	Note



2. Static accuracy im	plications	
Static error:= E_st E_st = E * St.en%	1.600%	
a0 (minimum)		
a0 = 1 / (F.E_st) a0 (dB)	46.94 33.43	k dB
Gain of second stage, a2 (mi	nimum)	
a2=a0 / a1	160.74	W
3. Dynamic Accu	ıracy	
Dynamic error:= E_dyn		
E_dyn = E - E_st	0.400%	
Slewing (N/A for CTIA)		
Slew time (t_slew)	0.00E+00	sec
SR_ext = (B-1).IBIAS / Co		V/us
SR_int = IBIAS / C		V/us
SR_ext = SR_int		
then IBIAS-slew:		
(DeltaVod/2)*C / t_slew	_	A
B(2nd:1st BIAS ratio) = 1 + Co	C	
Linear		
Linear time:= t_lin = ts-t_slew	5.00E-08	sec
Linear accuracy:= E_lin		
E_lin = E_dyn (NO SLEW)	0.400%	
minimum OTA's transcondu		
$Gm_s = -(Co/F)*[In(E_lin)/T_lin]$		
or desired Gm	4.00E-01	
Gm = max(Gm_s, desired Gm	4.00E-01	Sie
Then IBIAS becomes		
THOU IDING DOCUMES		

-		
Requirements for second stage (minimum)	
a2 (minimum)	160.74	
gm8 = Gm / a1 (minimum)	1.37E-03	Sie
R2 = a2 / gm8 (minimum)	1.17E+05	Ohn
SECOND STAGE DESIGN		
From simulations and iteration:		
Gain of second stage a2	150	VN
2nd st. transconduct.gm8	3.60E-04	Sie
R2 = a2 / gm8 (required)	4.17E+05	
Com. src. ro8 (from sims) =	1.48E+05	
Load CS, ro7 (from sims) =	2.89E+05	
Com src. (P) Vov:= V8* (from sims) Load CS (N) Vov:= V7* (from sims)		
Load CS (N) Vov:= V/* (from sims)	3.11E-01	V
R2 (achieved) = ro7 // ro8	9.79E+04	
and gm7 = gm8. V8* / V7*	5.15E-04	
1014 00 (1) 0 1/01 (0	A AFF AL	
IBIAS2 (in paper) = gm8.V8* / 2 IBIAS2 (from sims)	3.05E-04 2.50E-04	
Company of the Compan	ZIOOL OT	
Sizes W = L.gm / (u.Cox.V*)	W(um)	
M8,M10 (common source)	8.56E+01	
M7,M9 (active loads)	7.29E+01	5.00
Input Noise Power Density due to	2nd stage	:
(1/a1)(8/3)(KT/gm8)(1+gm7/gm8)		

3. From total Gm and a2 to second stage design

4. Tweaking in th	e simulato	r
important values so far		
gm1		mSie
R1	205.63	
gm8	0.36	mSie
R2	97.88	kOhm
O Initial transistor sizes	W(um)	L(um)
	221	3.0
M3,M4 (active load)	126	4.0
M8 (common source)	86	4.0
M1,M2 (differential pair) M3,M4 (active load) M8 (common source) M7 (2nd stage bias)	73	
Sizes after tweaking in sim	w	- 1
M1,M2 (differential pair)	200	3.000
M3.M4 (active load)	100	4.000
M8 (common source)	100	
M7 (2nd stage bias)	80	5.000
and for CMFB amplifier (fre	om sims)	
M14,M14a,M15,M15a (diff p		
M16, M17 (act. Load)	80	5.000
M18 (diff pair bias)	100	4.000

M16, M17 (act. Load) M18 (diff pair blas)	5.075 6.3	5.075 4.025
Yielding transistor sizes of	w	L
M1,M2 (differential pair)	198.8	2.975
M3,M4 (active load)	100.8	4.025
M8 (common source)	100.8	4.025
M7 (2nd stage bias)	81.2	5.075
and for CMFB amplifier		
M14, M14a, M15, M15a (diff pair)	9.8	0.875
M16, M17 (act. Load)	81.2	5.075
1140 (diff nois black	400.0	4.005

5. LAYOUT sizes

12.425

5.075

6.3 4.02

6.3 4.02

M1,M2 (differential pair)

13,M4 (active load)

7 (2nd stage bias)

8 (common source)

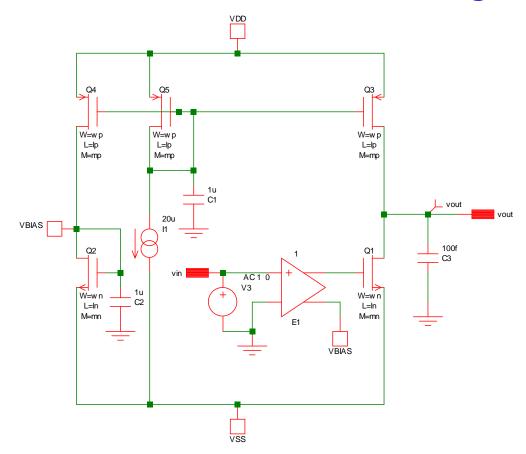
1	6. Rough verification	
55	Col = Col_factor.W Cgs = (2/3)W.L.Cox + Col Cgd = Col	
9 6 6 6	Cgs1,2 Cgd1,2 Cgs8 Cgd8	1.02E-12 F 4.02E-14 F 6.61E-13 F 2.61E-14 F
	Compensation cap C Check for consistency, hope Cp-new = Cgs1+Cgd1.(1+a1)	
6 6 6 6	Frequency response fd = 1/ (2 pi.R1 (gm8.R2.(C+Cgd8)+ fnd = gm8/(2 pi.Co) att = 20.log(fnd/fd)	####### kHz 255.50 MHz

	SPECS	
COLOR CODES	KNOBS	
	PARTIAL VALS	
	FINAL VALUES	





First and second stage design strategy



Circuit for design of amplification stage

Transistor models from vendor are used to optimize the design of a single stage of amplification with active loading

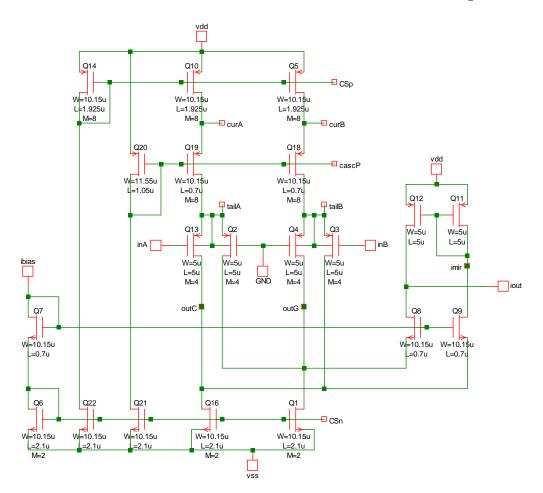
Bias conditions are replicated, and noise from biasing strategy is properly filtered out

Design results are back-annotated in work sheet





Common-Mode amplifier design



Q13 and Q3 compute common-mode voltage from the OTA output and "compare" it to the desired value (GND)

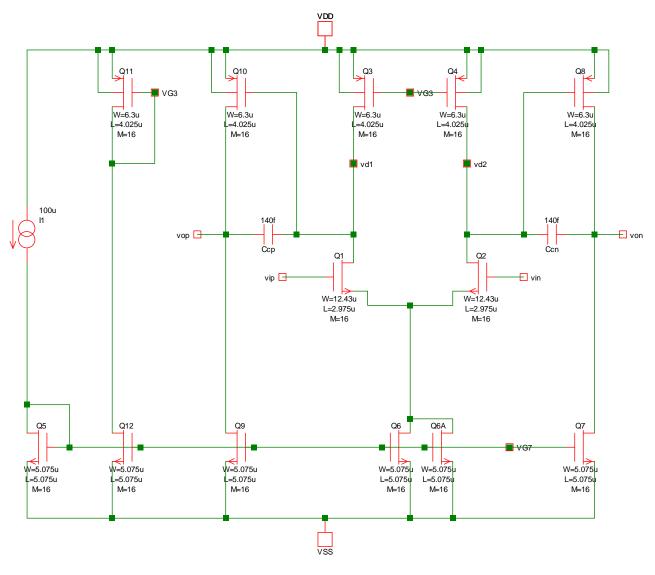
The amplifier produces a current output that regulates the common-mode voltage in the differential amplifier

Common-mode amplifier circuit





Final schematic for differential OTA

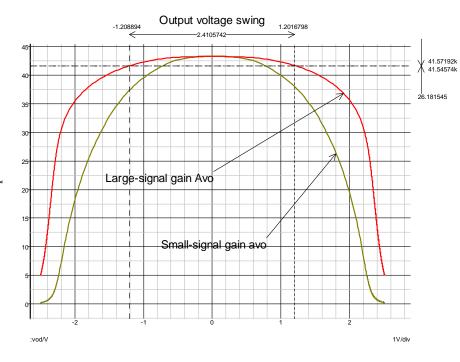




OTA Performance



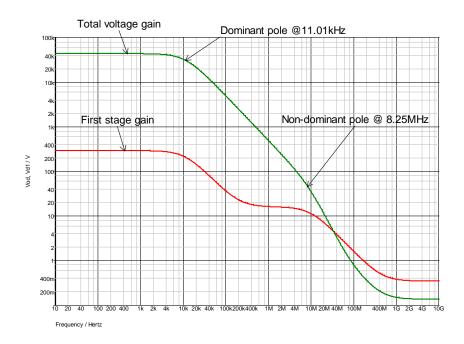
Open-loop gain



Open-loop gain exceeds 40,000 for the operation

range (2.4Vpk-pk)

Frequency response



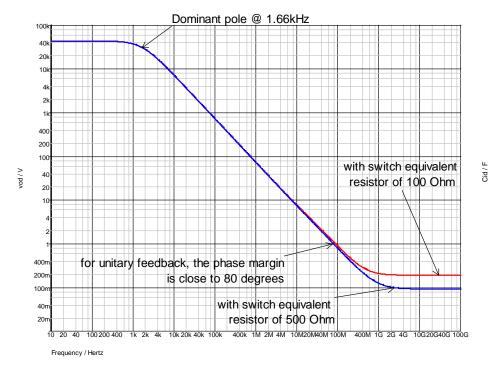
Dominant and non-dominant pole about three decade apart



OTA Performance



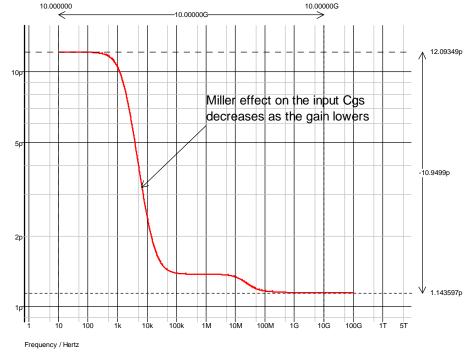
Frequency response with external compensation



External compensation of 3pF yields phase margin of about 80 degrees

Compensation switch optimally sized for zero-nulling

Input differential capacitance



Cin ~ 12pF at low frequencies

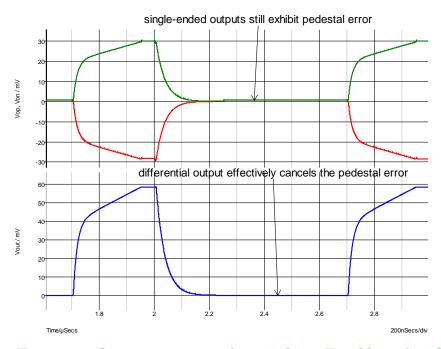
Decays for high frequencies because of absence of Miller effect



OTA Performance



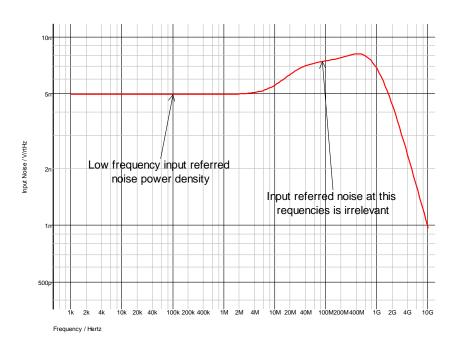
Transient response with external compensation



External compensation of 3pF effectively reduces differential transient ringing

CMFB amplifier is also compensated (1pF) to reduce common-mode voltage transient ringing

Input referred noise density



Low frequency input referred noise around 5nV/rtHz

High frequency noise density is not relevant in this case

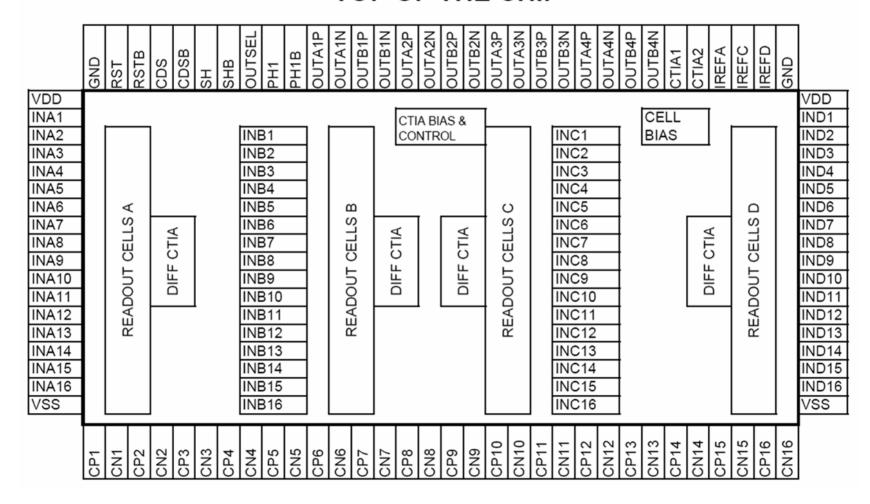


Second generation ROIC



Four 1x16 arrays + Fully differential CTIA

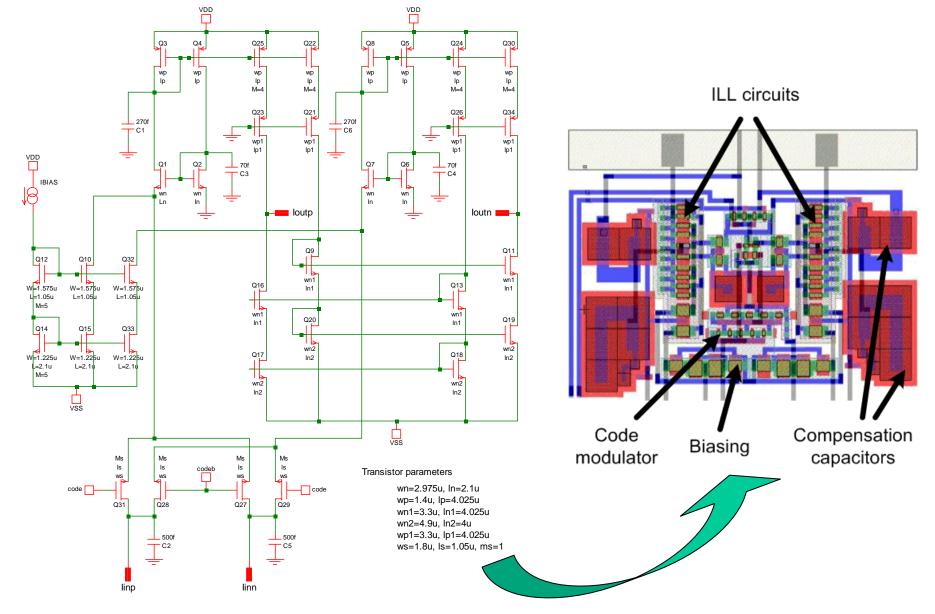
TOP OF THE CHIP





Readout cell physical design



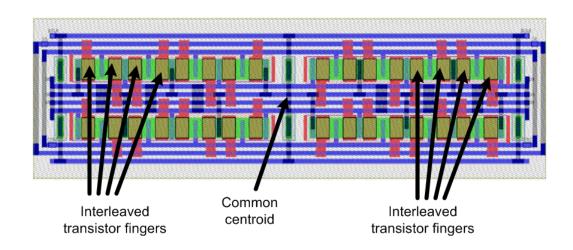




CTIA physical design

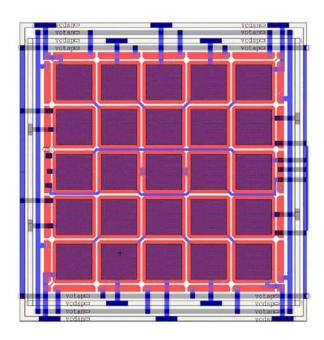


Matching transistors and capacitors



All differential pairs are designed with multi-finger, common-centroid structure

The differential OTA is divided into differential pair sections



Four-capacitor layout using common-centroid techniques

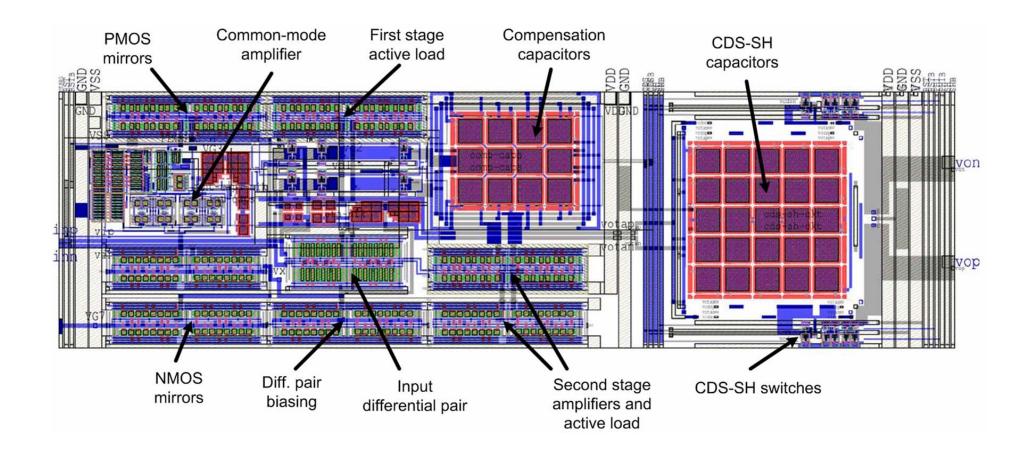
Dummy cap in the middle shorted to ground



ROIC physical design



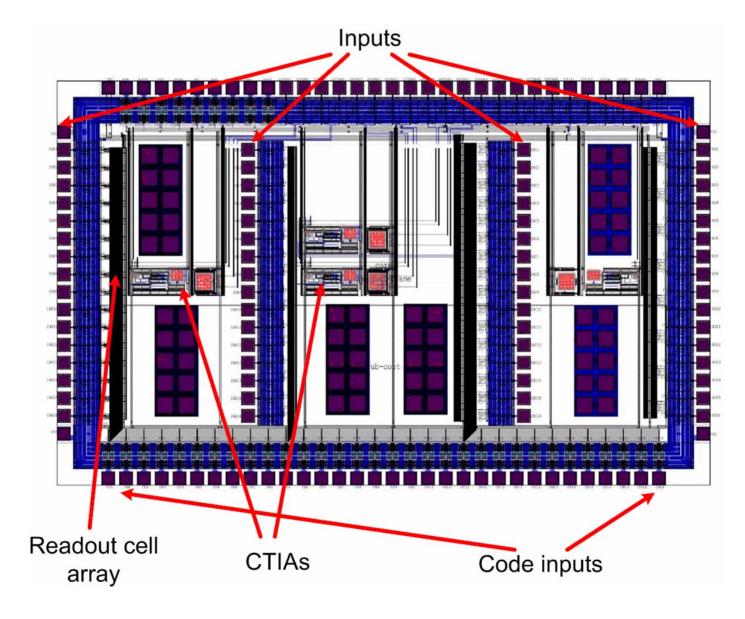
Fully differential CTIA amplifier





ROIC physical design









- Introduction and motivation
- Contribution Phase I: Proof of principle
 Orthogonal encoding readout system description
 Prototype system design and verification
 Conclusions
- Contribution Phase II: Improving the system performance

Readout cell improvements

Transimpedance amplifier integration

 Conclusion and brainstorm on further improvements

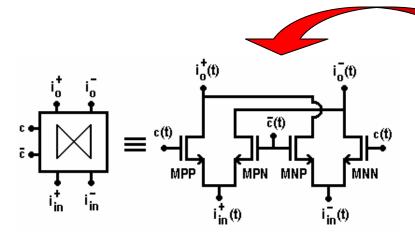


Conclusion



Satisfactory results with the prototype experiment confirm validity of the orthogonal encoding scheme for readout circuits

Expect system performance improvement with the design optimization of the readout cell and the integration of the fully differential CTIA



$$i_{o}^{+}(t) = i_{in}^{+}(t) \cdot c(t) + n_{c} + i_{in}^{-}(t) \cdot \overline{c}(t) + n_{\overline{c}},$$

$$i_{o}^{-}(t) = i_{in}^{+}(t) \cdot \overline{c}(t) + n_{\overline{c}} + i_{in}^{-}(t) \cdot c(t) + n_{c},$$

$$i_{od}(t) = i_o^+(t) - i_o^-(t) = [i_{in}^+(t) - i_{in}^-(t)] \cdot [c(t) - \overline{c}(t)],$$

The readout cell with the codemodulator only is an outstanding candidate for highly-scalable imaging systems. Its characteristics: only four transistors, zero noise, no power consumption, no band width limitations.

Further improvement is accomplished if differential photodetector devices are used

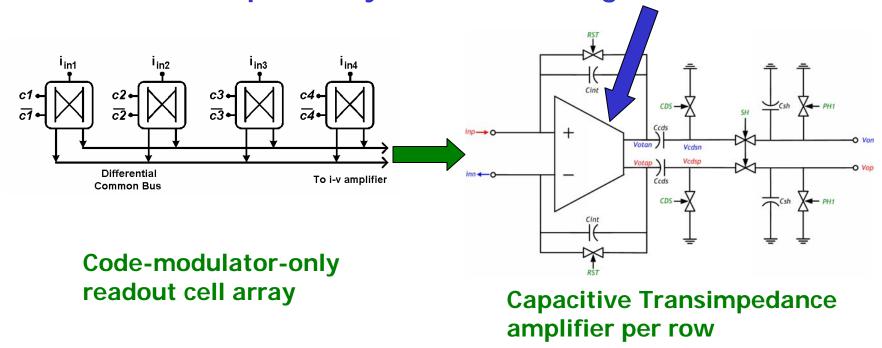


Conclusion (cont'd)



Take advantage of switched nature of the system to cancel charge injection peaks from readout cells.

With code-modulator-only cells the system becomes highlyscalable but the noise performance of the OTA amplifier needs to be improved by one order of magnitude

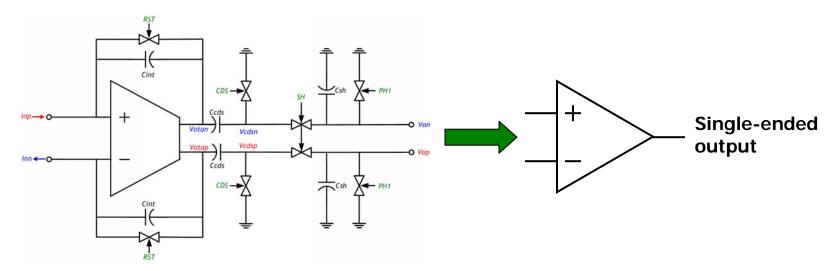




Conclusion (cont'd)



Integrating an amplifier to perform differential to singleended conversion inside the chip would improve the system performance (pedestal voltages and vestigial voltage spikes would be cancelled inside the integrated circuit)



Capacitive Transimpedance amplifier per row

Differential amplifier per row



Acknowledgements



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