

Abstract

NATH, JAYESH. Design and Characterization of Frequency Agile RF and Microwave Devices using Ferroelectrics. (Under the direction of Dr. Michael B. Steer).

A methodology for the optimized design of tunable distributed resonators is introduced and verified. This technique enables maximum tuning with minimum degradation in quality (Q) factor. The concept of a network transformation factor and a new figure-of-merit for tunable resonators is introduced and applied to experimental data. The figure-of-merit quantifies the trade-off between tunability and Q factor for a given tuning ratio of the variable reactance device. As such, it can be extended to the design of filters, phase shifters, antennas, matching networks and other frequency-agile devices where resonant elements are used. Varactors utilizing Barium Strontium Titanate (BST) thin-film were designed and fabricated in integrated form and also in discrete form as standard 0603 components. High frequency characterization and modeling of BST varactors is described. A novel characterization technique for the intrinsic loss extraction of symmetrical two-port networks was developed and verified experimentally. Both integrated and discrete BST thin-film varactors were used to design, fabricate and characterize frequency-agile circuits. Tunable bandpass and bandstop filters and matching networks are described. A dual-mode, narrowband microstrip patch antenna with independently tunable modes was developed and characterized. Tuning and nonlinear characterization results are presented. Investigation for the use of BST thin-film varactors for voltage-controlled oscillators and phase shifters are also presented. Design parameters, fabrication issues, and processing challenges are discussed.

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**Design and Characterization of Frequency Agile RF and Microwave
Devices using Ferroelectrics**

by

Jayesh Nath

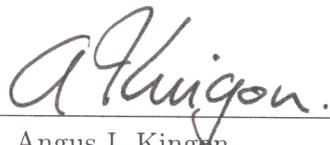
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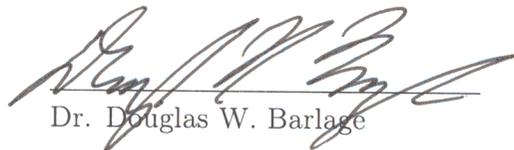
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Chair of Advisory Committee



Dr. Douglas W. Barlage

To my mom for her love and understanding and to my father for his patience and
support ...

“ We shall not cease from exploration. And the end of all our exploring will be to arrive where we started and know the place for the first time. ”

T. S. Eliot, *Little Gidding*

...

Biography

Jayesh Nath received the B.E. degree (with honors) in electronics and communication engineering from the Birla Institute of Technology-Mesra, Ranchi, India in June 2001 and joined the Ph.D. program in electrical and computer engineering at North Carolina State University, Raleigh, North Carolina in August 2001.

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Mr. Nath is a student member of the Automatic RF Techniques Group (ARFTG), International Microelectronics and Packaging Society (IMAPS), IEEE Microwave Theory and Techniques Society (MTT-S), IEEE Circuits and Systems Society (CAS), European Microwave Association (EuMA), and the IEEE Components, Packaging and Manufacturing Technology Society (CPMT). He likes reading, HAM radio activities, and astronomy.

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Chapter 1

Motivation, Contributions and Dissertation Overview

1.1 Introduction

This chapter deals with the motivation for this work, original contributions and publications resulting from the original contributions. First the basics of frequency-agile systems and the need for such systems will be reviewed. Various enabling technologies such as mechanical varactors, MEMS, semiconductor varactors and BST varactors will be described and compared. In the light of the need for frequency-agile systems, the characteristics of BST varactor and its application to system design will be described. The motivation for this work and the objectives of the research work will also be introduced. A list of original contributions and publications will also be presented. Finally, an overview of the dissertation will be described.

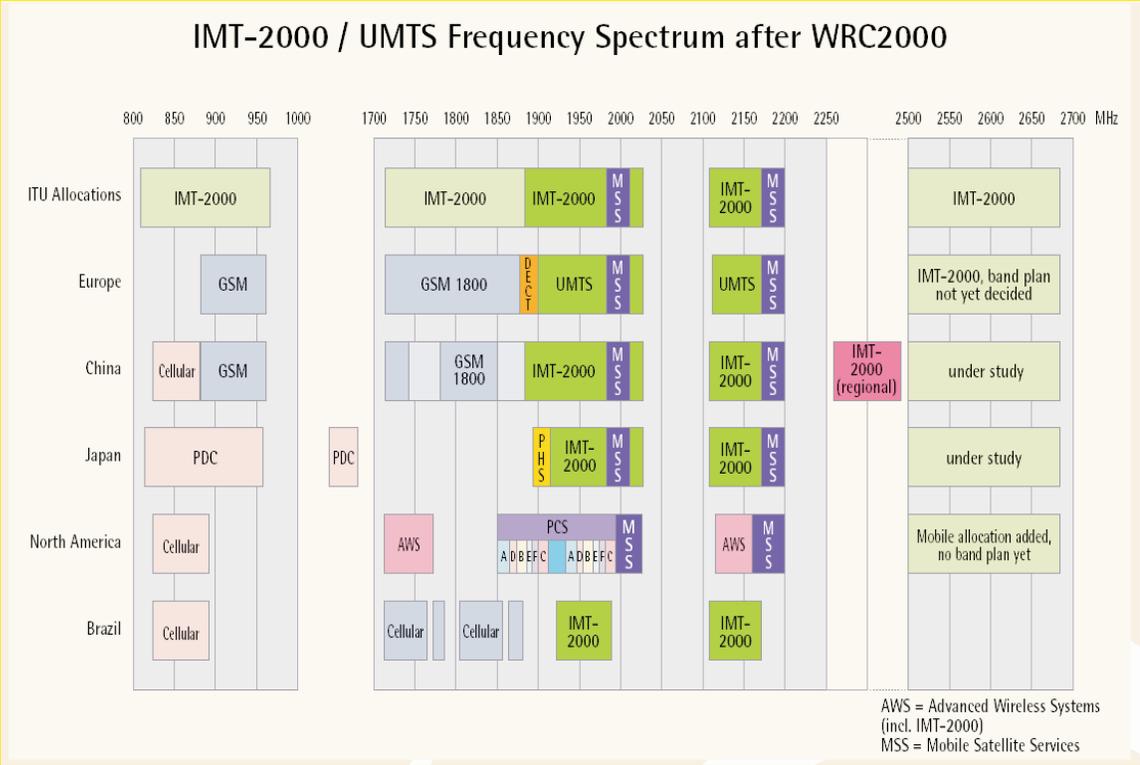


Figure 1.1: Crowding of electromagnetic spectrum. Credit: World Radiocommunication Conference (WRC) 2000

1.2 Frequency agile radio frequency systems

With the proliferation (see Figures 1.1 and 1.2) of wireless systems and standards over the past few decades the need for frequency-agile hardware has increased considerably. Since different parts of the world tend to have different frequency standards, the need for devices operating on different standards and also over different frequency bands within each standard is increasing quickly. It is estimated that as of late 2005 well over 2.0 billion people around the world used a wireless device and millions more are joining the growing network each day. Though GSM has over 75% market share, there are eight other major standards. Sometimes, the same standard is implemented at different frequency bands in different regions of a country or in different countries. GSM, for instance, operates in the 800, 900, 1800, and 1900 MHz bands, necessitating the need for a multi-frequency wireless device.

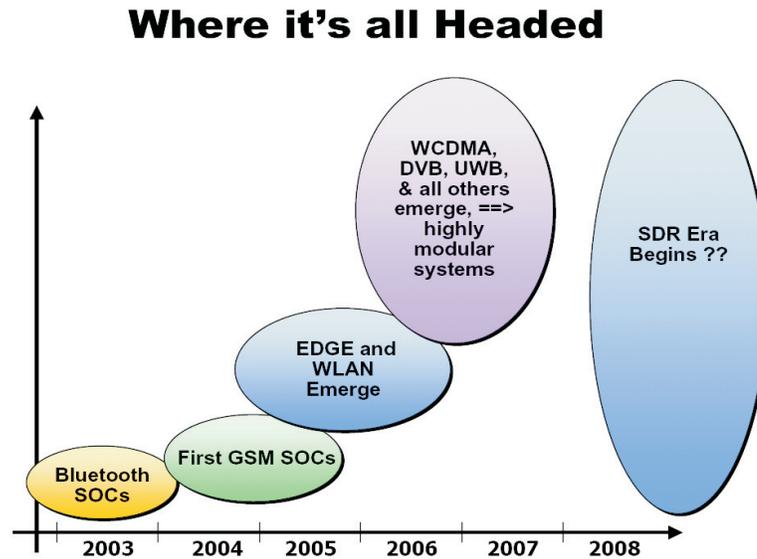


Figure 1.2: Proliferation of wireless standards. Credit: Texas Instruments, Inc.

Traditionally, frequency agility has been achieved by replicating hardware components for different frequency bands. Quad-band phones covering all four GSM frequencies are a standard now. However, this increases both the board space and cost. There is a great need for a single hardware unit to operate across different frequency bands and seamlessly switch between heterogeneous standards [1, 2]. The need is echoed by the military and satellite markets as well. DARPA (Defense Advanced Research Project Agency) has funded a program called the Joint Tactical Radio System (JTRS) [3] which hopes to achieve the ultimate frequency agility by integrating modular, scalable, multi-band, multi-mode hardware devices that can be upgraded in software and is interoperable through the internationally endorsed open Software Communications Architecture (SCA). Reuse, scalability, and field upgrades are the key advantages from a military perspective, among others. Similarly, in the field of satellite communication it is not uncommon to find multiple-frequency transponders on the same communication spacecraft serving different markets and varied needs. This not only allows judicious use of spectrum resources but also lowers the cost of satellite based communication systems since the payload cost is shared. Further

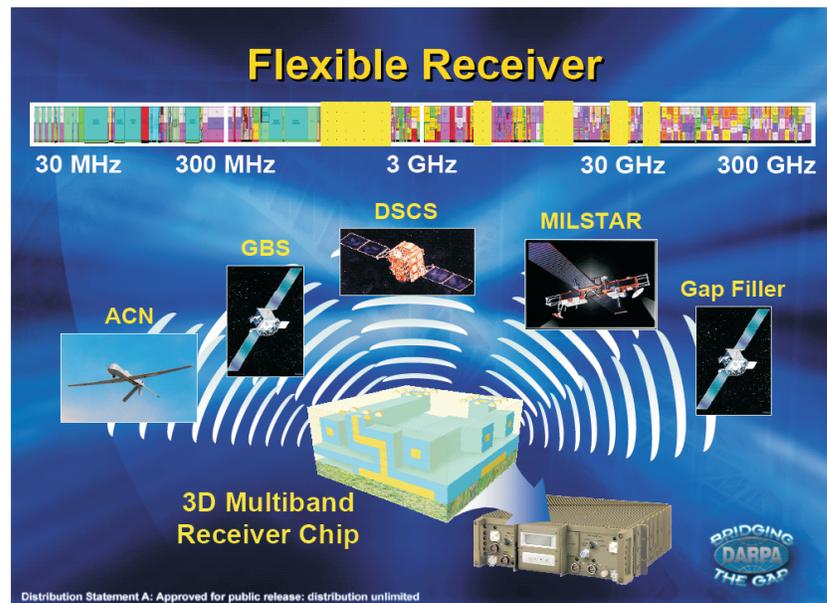


Figure 1.3: Need for frequency-agile transceivers. Credit: DARPA

reduction in payload weight by using frequency-agile transponders is highly desirable.

1.2.1 Techniques for achieving frequency agility

Frequency agility can be achieved in either the digital or the analog domain or a combination of both. In most practical systems a reasonable compromise is made. Typically analog frequency-agile systems offer higher dynamic range at a higher cost while achieving frequency agility in the digital domain is usually accomplished in software at a marginal cost, though at the expense of reduced dynamic range. For the purposes of this dissertation, discussions of frequency agility will refer to analog frequency agility unless otherwise noted. Figure 1.3 shows a frequency-agile receiver operating from 30 MHz to 300 GHz as envisioned by DARPA. DARPA has funded many projects that aim to develop technologies which will provide frequency agility in a modular multi-band 3D chip. Various commercial applications are also being developed, such as the one from Maxim Integrated Inc., shown in Figure 1.4. A

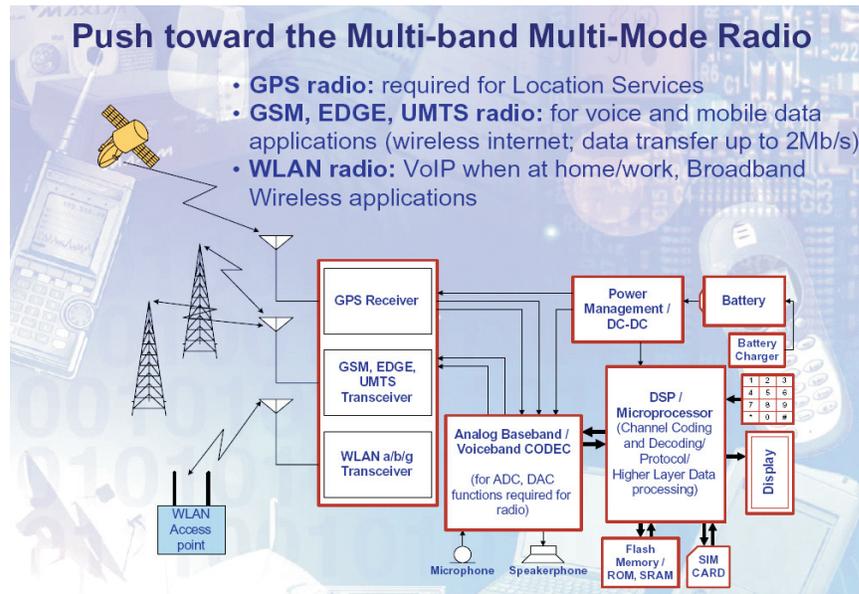


Figure 1.4: Typical Multi-band, Multi-mode radio. Credit: Maxim Integrated Products Inc.

single-chip [4] provides multi-functionality in terms of services offered to the end-user. The demand for a single product which offers cellular, WLAN and location based services has witnessed tremendous growth in recent years.

Analog components such as filters, matching networks, phase shifters, power amplifiers [5], duplexers and antennas need to be frequency-agile in a multi-band, multi-standard communication system, see Figure 1.5. From a physical point of view, changing either the inductance or the capacitance will accomplish frequency agility. This is because all frequency selective devices comprise of unit structures which are resonant systems and the resonant frequency of any system can be reduced to an equivalent capacitance and inductance.

Various techniques for changing either the inductance or the capacitance is illustrated pictorially in Figure 1.6. In general, methods of changing the capacitance are much more practical than those for changing the inductance. This is especially true at higher frequency where an integrated variable reactance element is highly desirable. Details of the various tuning methods and enabling technologies is discussed in the next section.

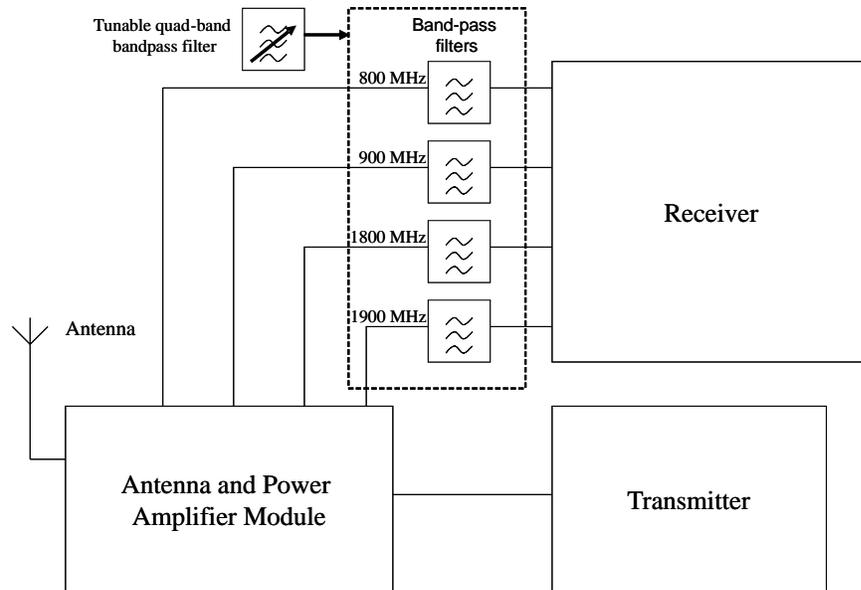


Figure 1.5: Block diagram of a quad-band wireless transceiver using four fixed frequency filters, a single frequency-agile filter can potentially replace four parts.

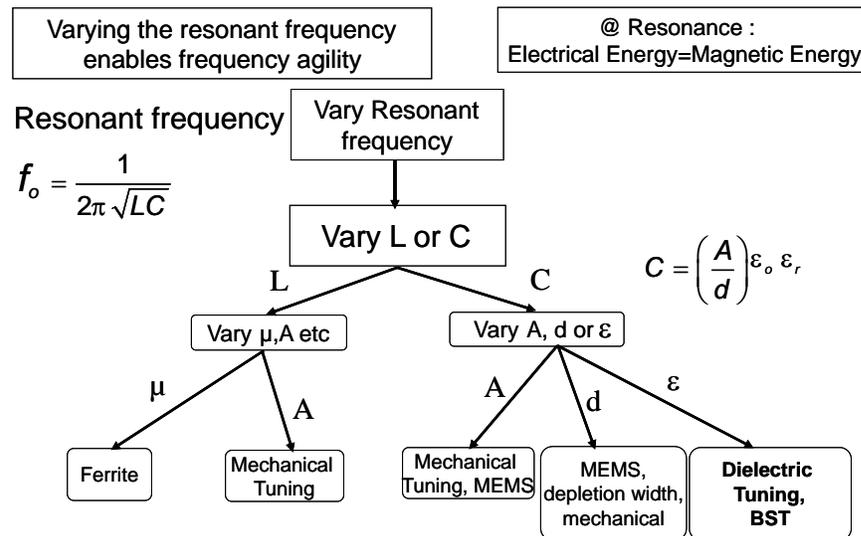


Figure 1.6: Techniques for achieving frequency agility.

1.2.2 Enabling technologies

Various technologies have been used for frequency-agile devices. Ferrites and ferrimagnetic components, YIG (yttrium iron garnet), semiconductor varactors and PIN diodes, mechanical varactors, microelectromechanical(MEMS) [6], varactors, and ferroelectric varactors are the most commonly used technologies. The choice of technology depends on the application, system specification, cost, integration with other technologies and reliability, among others. Usually two or more of these technologies may be required to work in a complementary manner to achieve the required system performance.

Ferrites and ferrimagnetic components have been used for many years for fabricating tunable filter and phase shifters. Ferrimagnetic materials exhibit magnetic anisotropy upon application of a DC magnetic bias field. This field aligns the magnetic dipole moments in the material to produce a nonzero net magnetic moment and causes the dipoles to precess at a frequency controlled by the strength of the bias field. The interaction with the applied microwave signal can also be controlled by adjusting the strength of the bias field [7]. Ferrite materials exhibit a typical hysteresis curve and are usually operated in saturation where losses are lower. One of the popular design for a ferrite phase shifter is the remnant nonreciprocal phase shifter using a ferrite toroid in a rectangular waveguide. It provides a digital phase shift and allows noncontinuous bias current operation. Current pulses of different polarity only need to be applied when switching states. The same design can be modified to operate in the continuous bias current mode as an analog phase shifter. Nonreciprocal faraday rotation phase shifters are also used [7].

A ferrite based phase shifter has the advantages of low cost, and large power handling capability. However, they are slow (switching time in the microsecond range), and bulky, and are discrete components which do not offer ease of monolithic integration with the rest of the system.

MEMS or microelectromechanical systems have been used for various application since the 1970s. They are essentially miniature incarnations of mechanical switches fabricated at the micron scale using conventional photolithography tech-

niques. MEMS have been used as temperature and pressure sensors, accelerometers, gas chromatographs, and other sensing devices. In early 1990s Larson [8] was the first to demonstrate a MEMS switch and a varactor at microwave frequencies. Since then RF MEMS have been extensively developed by both companies and universities. MEMS- based varactors and switches have been used to construct tunable filters, phase shifters and matching networks. MEMS switches have been used as low loss RF switches in multi-band communication devices to replace GaAs, MOS or PIN diode based switches. They offer small size and have a low insertion loss advantage over the competition. Broadly speaking, MEMS can be divided into four broad categories [9]:

- RF MEMS switches, varactors, inductors, and transmission lines.
- Micromachined high Q resonator, filters, and antennas.
- RF micromachined resonators that use mechanical vibration of small beams. High Q resonator at low frequencies have been used as reference clock sources.
- FBAR (Film Bulk Acoustic Resonators) using acoustical vibrations to achieve very high Q (> 2000) resonators. Agilent has pioneered its use in low loss, compact filters and duplexers for mobile handsets.

MEMS devices also offer low power operation and high linearity. Due to the low thermal budget involved in MEMS processing, they can be added as a last step process in CMOS, GaAs, SiGe and other popular process technologies. Despite all the advantages, the widespread use of MEMS has been impeded by the high cost of packaging and by reliability issues. MEMS-based devices typically require hermetic packaging and this significantly increases the cost over solid-state devices. An associated problem is that of reliability and lifetime testing. Many systems, especially military systems require lifetimes of over 30 years and most of the MEMS devices currently available do not meet such requirements. Another important limitation of MEMS-based devices is that of slow switching speed. Typically the switching speed is in the range of a few microseconds. Though it is quite sufficient for an application

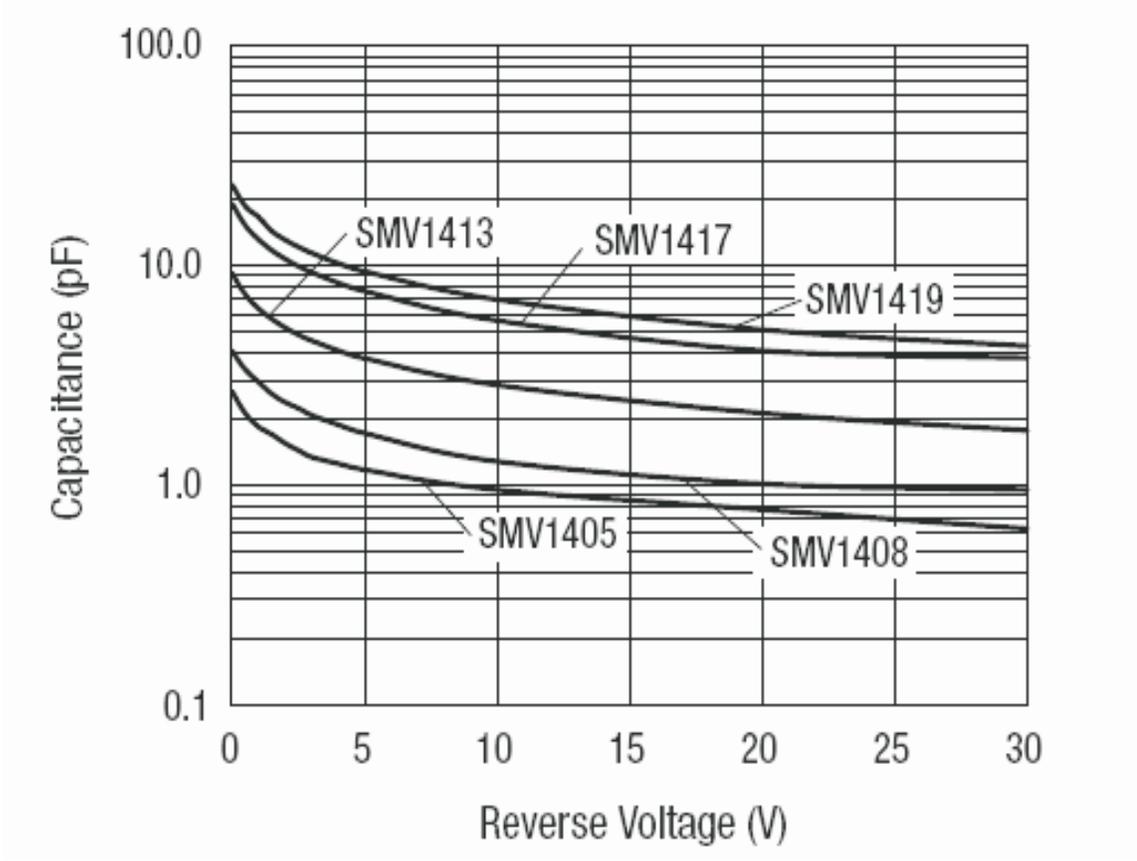


Figure 1.7: C-V curve from Skyworks, Inc. [10] for silicon abrupt varactor diodes.

such as switching in cell phones, it proves to be a limitation on the system performance in phased array radar system where tracking a target in real time is of primary concern. Overall, MEMS-based devices have tremendous potential for frequency-agile devices if packaging and reliability problems are solved.

Semiconductor varactors have been used in frequency-agile devices in both discrete and integrated form for over five decades. Operation is based on the principle of change in the depletion width when a reverse bias is applied to a PN junction diode. The depletion width can be thought of as the distance between the two plates of an equivalent parallel plate capacitor. The depletion width increases with increasing reverse bias and hence the capacitance decreases with bias, see Figure 1.7.

Semiconductor diodes [10] have a significant advantage in terms of tuning range

and tuning ratios as large as 15:1 for under 20 V bias are easily available for hyperabrupt diodes. Of course, such high tuning comes at a price of poor linearity and lower Q . The linearity can be controlled to an extent by properly tweaking the manufacturing process to yield the desired C-V curve. Semiconductor varactors have Q factor in the range of 20–60 up to 10 GHz. Beyond that, the Q factor degrades dramatically. GaAs varactors offer higher Q factors than their silicon counterparts but they have a higher flicker noise due to increased mobility. Various frequency-agile devices such as tunable filters, matching networks, phase shifters, and antennas have been reported using semiconductor varactors. It is also the varactor of choice for most integrated and on-chip VCOs.

Mechanical varactors [11] have been used since the early days of radio for channel selection at the RF front-end. Even today one can find motorized and microprocessor controlled mechanical varactors used in tunable filter banks and other frequency-agile devices. They offer high power handling capability and extremely low insertion loss. However, their large size and weight prevents their use in all but very specialized applications.

Ferroelectric varactors utilize the fact that the dielectric constant is a function of the applied electric field [12]. They are generally used in the paraelectric phase above the Curie temperature (T_c) where hysteresis is absent and losses are lower. Barium Strontium Titanate (BST) is the most popular of the perovskite-type ferroelectric materials used as dielectric for fabricating tunable capacitors. BST offers low loss, high tunability and integration with other technologies. BST varactors, both in parallel plate and interdigital form, have been used to demonstrate tunable phase shifters, filters, matching networks and delay lines. They offer higher Q in the gigahertz range compared to a semiconductor varactor [16]. Though at the expense of higher tuning voltage, but not higher power, BST varactors offer better linearity performance than semiconductor varactors. In the construction of voltage controlled oscillator they potentially offer a lower $1/f$ noise device, though this needs to be investigated further.

Recently, Park *et al.* [13] reported a non-ferroelectric tunable material, Bismuth Zinc Niobate (BZN) as a microwave dielectric. It has cubic pyrochlore structure and a

Table 1.1: Comparison of competing technologies.

Parameter	Mechanical Varactor	Semiconductor Varactor	Ferroelectrics (BST)	MEMS Varactor
Tunability	Excellent (20:1)	Very good (15:1)	Good (3:1)	Very good (10:1)
Q factor	Excellent (500–1000) (@ 1–5 GHz)	Good (10–20) (@ 20 GHz)	Very Good (30–50) (@ 20 GHz)	Excellent (150–200) (@ 20 GHz)
Integration	Difficult	Very Good	Very Good	Very good
Packaging	Standard	Standard	Standard	Hermetic
Cost	High	Low	Low	Moderate
Linearity	Excellent (> 60 dBm)	Moderate (15–25 dBm)	Very Good (30–55 dBm)	Excellent (> 65 dBm)
Size & weight	Large	Small	Small	Small
Reliability	Very Good	Excellent	Very good	Good
Maturity	Mature	Mature	Developing	Developing

permittivity in the range of 170–200. Its low loss ($\tan \delta = 0.0005$) and high tunability (55%) are the main attractions compared to ferroelectrics. They reported Q factor of over 200 at 20 GHz and low leakage current and high field strength compared to thin-film BST varactors. This is a very promising material and could become a viable technology for frequency-agile systems.

1.2.3 Comparison of competing technologies

Various technologies mentioned in the previous section have particular strengths and weaknesses. Depending on the particular systems requirements, the most suitable technology from a cost, ease of integration and reliability point of view is chosen. It is conceivable that in certain implementations two or more technologies might be employed for system design. For example, in phased array radar systems azimuth scanning is usually implemented using mechanical rotors while elevation scanning is implemented using electronic phase shifters. Similarly, in multi-standard, multi-band wireless devices, MEMS switches could be used at the front end for selecting the appropriate filter while a semiconductor varactor can be used in a fully-integrated

digital oscillator. A comparison of various competing technologies in light of parameters typically considered in system design is shown in Table 1.1.

1.3 Original contributions

Several contributions were made as a part of this dissertation work. A technique for the design of optimized resonators and a figure-of-merit enabling the trade-off between tunability and Q factor was introduced and verified. Furthermore, a technique for calculating the intrinsic loss in symmetrical two-port network is also introduced and verified. A BST thin-film and metallization process was co-developed and optimized. Frequency agile devices using the BST process were designed, fabricated and characterized. A discrete BST thin-film varactor technology was also developed and employed to demonstrate frequency-agile bandstop and bandpass filters on FR4 board in the range of 1–4 GHz. A novel dual-mode antenna with independently tunable modes was designed and characterized. A list of original contributions is given below. Appropriate sections in the dissertation are indicated against each original contribution that is claimed.

1. Co-development of thin-film BST and metallization process (Chapter 3, Section 3.3)
2. Process optimization for high Q BST varactors (Chapter 3, Section 3.3)
3. Characterization of BST varactors (Chapter 3, Sections 3.3 and 3.4)
4. Resonator design for optimized tuning and quality factor (Chapter 4, Sections 4.2.2, 4.2.3, 4.2.4, and 4.2.5)
5. Intrinsic loss extraction technique (Chapter 4, Sections 4.3.2, 4.3.3, and 4.3.4)
6. Integrated tunable bandpass filter on alumina and sapphire (Chapter 5)
7. Development of discrete BST varactor technology (Chapter 6, Section 6.1)

8. Discrete tunable bandstop filters (Chapter 6, Section 6.3)
9. Discrete tunable bandpass filter (Chapter 6, Section 6.4)
10. Tunable matching network (Chapter 7, Section 7.2)
11. Narrowband tunable antenna (Chapter 7, Section 7.3)
12. Co-development of BST thin-film based VCO and master oscillator power amplifier (Appendix A, B)
13. Development of co-planar T resonator based permittivity characterization technique (Appendix C)
14. Co-development of BST interdigital varactor loaded line phase shifter (Appendix D)

1.4 Publications

This section details a list of technical publications and patents generated as a part of this research work. Publications in progress have been listed separately. Six journal and ten refereed conference papers have been published while seven other papers are in progress for a total of twenty three publications. One provisional patent has also been filed.

List of papers:

- **Publications:**

1. **J. Nath**, W. M. Fathelbab, P.G. Lam, D. Ghosh, Seymen Aygun, Kevin G. Gard, J.-P. Maria, A. I. Kingon, and M. B. Steer, “Discrete Barium Strontium Titanate (BST) Thin-Film Interdigital Varactors on Alumina: Design, Fabrication, Characterization, and Applications,” Accepted for publication in 2006 *IEEE MTT-S Int. Microwave Symp.* , Jun. 2006.

2. **J. Nath**, D. Ghosh, J.-P. Maria, A. I. Kingon, W. Fathelbab, P. D. Franzon, and M. B. Steer, "An electronically-tunable microstrip bandpass filter using thin-film barium strontium titanate (BST) varactors," *IEEE Trans. on Microw. Theory and Tech.*, vol. 53, no.9, pp. 2707–2712, Sep. 2005.
3. **J. Nath**, D. Ghosh, W. Fathelbab, J.-P. Maria, A. I. Kingon, P.D. Franzon, and M. B. Steer, "A tunable combline bandpass filter using barium strontium titanate interdigital varactors on an alumina substrate," in 2005 *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 595–598, Jun. 2005.
4. M. Buff, **J. Nath**, and M. B. Steer, "Origin of half-wavelength errors in microwave measurements using the thru-line calibration family," Under review.
5. F.P. Hart, S.R. Luniya, **J. Nath**, D. Ghosh, A. Victor, J.-P. Maria, and M.B. Steer, "Discrete-Time filter synthesis and implementation in a circuit simulator," Accepted for publication in *Int. J. on RF and Microwave Computer Aided Eng.*
6. A. Victor, **J. Nath**, D. Ghosh, S. Aygun, W. Nagy, J.-P. Maria, A. I. Kingon, and M. B. Steer, "Voltage controlled GaN-on-Si HFET master oscillator power amplifier using ferroelectric varactors," Submitted to 36th *Eur. Microwave Conf.*, Under Review.
7. A. Victor, **J. Nath**, D. Ghosh, B. Boyette, J.-P. Maria, M. B. Steer, A. I. Kingon, and G. T. Stauf, "Noise characteristics of an oscillator with a barium strontium titanate (BST) varactor," Accepted for publication in *IEE Proc. Microwaves, Antennas & Prop.*.
8. D. Ghosh, **J. Nath**, J.-P. Maria, M. B. Steer, and A. I. Kingon, "High Q (Ba, Sr)TiO₃ interdigitated capacitors fabricated on low cost polycrystalline alumina substrates with copper metallization," in *Proc. Amer. Ceram. Soc. Conf.*, pp. 125–132, Jan. 2005.
9. **J. Nath**, D. Ghosh, J.-P. Maria, M. B. Steer, and A. I. Kingon, "A tunable combline bandpass filter using thin-film barium strontium titanate (BST),"

- in *Proc. Asia-Pacific Microwave Conf.*, New Delhi, India, Dec. 2004, pp. 939–940.
10. **J. Nath**, D. Ghosh, J.-P. Maria, M. B. Steer, A. I. Kingon, and G. T. Stauf, “Microwave properties of BST thin-film interdigital capacitors on low cost alumina substrates,” in *Proc. 34th Eur. Microwave Conf.*, Amsterdam, Netherlands, Oct. 2004, pp. 1497–1500.
 11. A Victor, **J. Nath**, D. Ghosh, B. Boyette, J.-P. Maria, M. B. Steer, A. I. Kingon, and G. T. Stauf, “A voltage controlled oscillator using barium strontium titanate (BST) thin-film varactor,” in *Proc. Radio and Wireless Conf.*, Atlanta, Georgia, Sep. 2004, pp. 91–94.
 12. W. Y. Liu, J. Suryanarayanan, **J. Nath**, S. Mohammadi, L. P. B. Katehi, and M. B. Steer, “Toroidal inductor for radio frequency integrated circuits,” *IEEE Trans. on Microw. Theory and Tech.*, vol. 52, no. 2, pp. 646-654, Feb. 2004.
 13. D. Ghosh, B. J. Laughlin, **J. Nath**, A. I. Kingon, M. B. Steer, and J.-P. Maria, “Tunable high Q interdigitated (Ba, Sr)TiO₃ capacitors fabricated on low cost substrates with copper metallization,” *Thin Solid Films.*, vol. 496, no. 2, pp. 669-673, Feb. 2006.
 14. T. Kim, **J. Nath**, J. Wilson, S. Mick, P. Franzon, M. B. Steer, and A. I. Kingon, “A high K nanocomposite for high density chip-to-package interconnections,” in *Proc. Mater. Res. Soc. Fall Symp.*, Boston, MA, Dec. 2004, pp. G5.9.1–G5.9.6.
 15. **J. Nath**, and M. B. Steer, “A straight forward method of characterizing the intrinsic insertion loss characteristics of symmetrical two ports,” in *Proc. 62nd Automatic RF Tech. Group Conf.*, Boulder, Colorado, Dec. 2003, pp. 233–238.
 16. J. Suryanarayanan, W. Y. Liu, **J. Nath**, B. N. Johnson, S. Mohammadi, L. P. B. Katehi, and M. B. Steer, “Toroidal inductors for integrated radio frequency and microwave circuits,” in 2003 *IEEE MTT-S Int. Microwave*

Symp. Dig. , Jun. 2003, vol. 1, pp. A93–A96.

• **In preparation:**

1. **J. Nath**, D. Ghosh, J.-P. Maria, A. I. Kingon, and M. B. Steer, “Design of optimized resonators : Tunability and Q factor trade-off,” In Preparation.
2. **J. Nath**, D. Ghosh, J.-P. Maria, A. I. Kingon, W. Fathelbab, K. G. Gard, and M. B. Steer, “A frequency agile bandpass filter using thin-film barium strontium titanate (BST) interdigital varactors on alumina,” In Preparation.
3. **J. Nath**, D. Ghosh, J.-P. Maria, A. I. Kingon, W. Fathelbab, K. G. Gard, and M. B. Steer, “A tunable bandstop filter on FR4 substrate using discrete thin-film BST varactors ,” In Preparation.
4. **J. Nath**, D. Ghosh, J.-P. Maria, A. I. Kingon, W. Fathelbab, K. G. Gard, and M. B. Steer, “Tunable matching network using BST thin-film interdigital varactors on Alumina,” In Preparation.
5. **J. Nath**, D. Ghosh, J.-P. Maria, A. I. Kingon, W. Fathelbab, K. G. Gard, and M. B. Steer, “A dual-mode narrowband tunable microstrip patch antenna using ferroelectric varactors ,” In Preparation.
6. D. Ghosh, **J. Nath**, M. B. Steer, A. I. Kingon, and J.-P. Maria, “High density, low loss metal-insulator-metal (MIM) capacitors using ZrO_2 thin-films for RF applications,” In preparation.
7. D. Ghosh, **J. Nath**, S. Aygun, W. Fathelbab, A. I. Kingon, M. B. Steer, and J.-P. Maria, “An electronically tunable microwave bandpass filter using ferroelectric Barium Strontium Titanate (BST) thin-films on low cost polycrystalline alumina substrate and base metal electrodes,” In preparation.

Invention disclosure:

1. A. I. Kingon, A. Mortazawi, J.-P. Maria, M. B. Steer, and **J. Nath**, “Novel frequency-tunable antennae for wireless devices employing varactors integrated with the radiating metallization and a co-fabrication method for the same, ” Oct. 2004, NCSU Invention Disclosure No. 05-007. Provisional patent application in progress.

1.5 Dissertation overview

This dissertation presents work done on the design and characterization of BST (Barium Strontium Titanate) based thin-film frequency-agile radio frequency devices.

BST has a field-dependent permittivity and can be used as a dielectric in voltage tunable capacitors or varactors. Chapter 2 reviews the fundamentals of BST varactor technology and presents a survey of the BST-based frequency-agile devices reported in the literature.

Chapter 3 introduces the BST varactor technology and details the choice of various capacitor configurations. Substrate issues, metallization and other processing details are also discussed. BST varactor characterization results for MOCVD and sputtered BST thin-film on alumina are presented. Interdigital capacitors were fabricated yielding capacitors in the sub-picofarad range and tunable by voltages up to 120 V. Low frequency intrinsic Q of over 100 were obtained. This reduced to an external Q of 17 at 26 GHz mainly due to the series resistance introduced at the electrodes. The maximum dielectric tunability was found to be about 1.65:1 (40%) for an applied field of 300 kV/cm at a bias of 120 V. Results are also presented for BST varactors deposited on alumina substrate using RF magnetron sputtering and metallization using a thermally evaporated copper. Q factor in the range of 28–30 was obtained for 0.2–0.6 pF capacitors at 26.5 GHz.

Chapter 4 introduces a technique for optimized resonator design. Experimental verification of the technique and trade-off with tunability and Q factor is also discussed. The concept of network transformation factor and a new figure-of-merit for characterizing tunable resonators is introduced and applied to the experimental re-

sults. A method of characterizing the intrinsic loss characteristics of a symmetrical two-port network using a two tier calibration procedure is also introduced. Mathematical development and experimental verification is presented. A first tier calibration to device fixturing ports results in symmetry. The second tier calibration uses a single through line. The resulting characterization is equivalent to the transmission factor of the network with ideal input and output matching networks. This has the effect of putting two ideal matching networks at the input and output of the network. A microstrip bandpass filter measurement and characterization using this technique is presented. The results are compared with de-embedded characterization obtained using the TRL (Thru-Reflect-Line) calibration procedure.

In Chapter 5 a third-order tunable combline bandpass filter using integrated thin-film BST varactors on sapphire and alumina substrate is presented. The center frequency of the filter on sapphire varied from 2.44 GHz to 2.88 GHz (16% tuning) upon the application of 180 V tuning voltage. The insertion loss of the filter was 8.3 dB at zero bias and 6.7 dB at 180 V bias. The return loss was better than 17 dB at all bias voltages. The effect of metallization on insertion loss is reported and non-linear characterization using a two-tone setup is also presented. The zero bias insertion was reduced from 8.3 dB for 0.5 μm sputtered copper metallization to 5.1 dB for 1 μm evaporated copper metallization. The IIP3 of the filter was found to be +41 dBm.

The effect of vias and bond wire on insertion loss is reported and non-linear characterization using a two-tone setup and a digitally modulated signal is also presented. For filters on alumina the high bias insertion was reduced from 6.6 dB for filters with wire-bonds and epoxy grounding to 4.5 dB for filters with on-chip probe pads with ground vias. The center frequency of the filter varied from 1.6 GHz to 2.0 GHz (25% tuning) upon the application of 200 V tuning voltage. The reduced loss was due to the elimination of wire-bonds and “ground wrapping”. The IIP3 of the filter was found to be +38 dBm. Using a digitally modulated signal the ACPR was found to be better than -55 dBc for up to +26 dBm of input power.

In Chapter 6 discrete BST varactor technology is introduced and temperature characterization is described. Tunable bandstop filters at 1 and 3 GHz using two different topologies on FR4 substrate are presented. Frequency tunability up to 20%

was obtained with tuning voltages up to 130 V. A second-order bandpass filter at 2 GHz with 22% tuning with the application of 130 V is also described. The insertion loss decreased from 4.9 dB at high bias state to 2.9 dB at 130 V. The power consumption was $< 0.7 \mu\text{W}$. Nonlinear characterization showed an IIP3 of +32 dBm and an ACPR of better than -50 dBc up to +26 dBm of input power.

In Chapter 7 the design and characterization of a semi-lumped tunable matching network and a narrowband dual-mode tunable antenna with independently tunable mode is also presented. A tuning range of over 400 MHz from 2.9 GHz to 3.3 GHz was obtained with a return loss better than 23 dB for the tunable matching network. The maximum tuning voltage was 200 V.

Two tunable antennas were designed, one with a BST MIM varactor on copper foil and the other with discrete BST Interdigital (IDC) varactors. For the first antenna, the zero bias frequency was 628.5 MHz and the return loss was 6.33 dB. The resonant frequency tuned to 653.2 MHz upon application of 40 V bias but the return loss deteriorated to 2.66 dB. The observed tuning range was 4%. The antenna with the discrete BST IDC varactor showed 8% tuning with 120 V. The return loss was better than 13 dB over the tuning range. Gain of 2 dB was obtained for the tunable transverse mode, while the gain of the non-tunable mode was 6 dB at 2.4 GHz. Radiation pattern of the antenna is also presented.

Finally, in Chapter 8 the dissertation draws to a close with conclusions and implications of the research work and recommendations for future work.

Application of BST varactors to other frequency-agile components, a voltage controlled oscillator (VCO), a master oscillator power amplifier (MOPA), and a tunable phase shifter are also presented in the Appendix A, B, and D respectively. The frequency of oscillation using a BST MIM varactor varied from 34.8 MHz to 44.5 MHz (28% tuning) upon application of 7 V tuning voltage. The VCO gain was 1.38 MHz/V and the 2nd harmonic was over 23 dB below the fundamental throughout the tuning range. A master oscillator power amplifier using discrete BST IDC varactor and GaN-on-Si transistor showed flat power output of 1.6 W over the tuning range at 1.6 GHz. Phase noise of -81 dBc/Hz at 10 kHz offset was recorded. A loaded line phase shifter using BST interdigital varactor was characterized at 10 GHz and showed phase

shift of 17 deg/dB. Also in Appendix C, a new technique for characterizing frequency dependent permittivity of thin-film dielectric using a multi-layer CPW T-resonator is presented and experimentally verified.

1.6 Conclusion

In this chapter the motivation for this work and the need for frequency-agile systems was discussed. Various technologies for frequency-agile systems were discussed and compared. A list of original contribution and publications was also presented. Finally, an overview of the dissertation was described. The next chapter presents a survey of the literature on BST growth and characterization. Literature on frequency-agile devices using BST varactors will also be discussed.

Chapter 2

Literature Review

2.1 Introduction

In this chapter the fundamentals of dielectric tuning in ferroelectrics and their growth and characterization techniques will be discussed. A survey of BST thin-film varactor based frequency-agile devices reported in the literature will also be presented.

2.2 Ferroelectrics and applications for tunable devices

Ferroelectrics are a class of polar materials that exhibit spontaneous polarization (see Figure 2.1) under the influence of an external applied electric field [14]. Ferroelectrics also show a peak in permittivity at the transition temperature, see Figure 2.2. The phenomenon of ferroelectricity has been known to the Europeans since the 15th century. Rochelle salt has been used for the past 275 years for its mild purgative medicinal properties. It was discovered in La Rochelle, France in 1655 by Elie

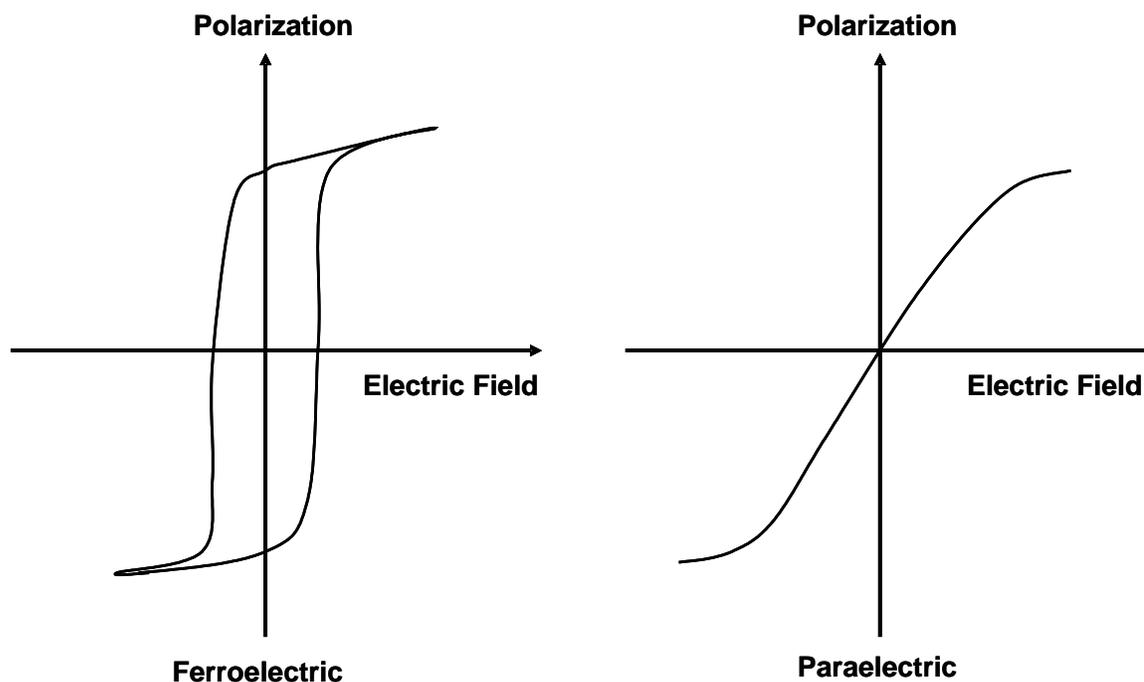


Figure 2.1: Polarization versus electric field.

Seignette who was an apothecary. The salt is sodium potassium tartrate tetrahydrate. However, it is unstable against dehydration and is a difficult material to work with for reliable electrical connections. It is also complex structurally. Ferroelectricity was “rediscovered” in the United States in 1923 when Joseph Valasek was analyzing Rochelle salt [15]. He was the first to establish the analogy between the magnetic properties of ferromagnetics and the dielectric properties of Rochelle salt and hence the name *ferroelectrics*. He also demonstrated the hysteretic nature of the polarization and its marked dependence on temperature.

These difficulties were largely overcome when Busch and Scherer reported the occurrence of ferroelectricity in potassium dihydrogen phosphate (KDP) and the isostructural dihydrogen arsenate. This was followed by the discovery of Barium Titanate (BaTiO_3) in the 1940s. BaTiO_3 belongs to the family of ceramic perovskite (named after a Russian mineralogist named Perovskiy) dielectrics. BaTiO_3 is the prototype of many oxide based ferroelectric perovskites which are characterized by the chemical

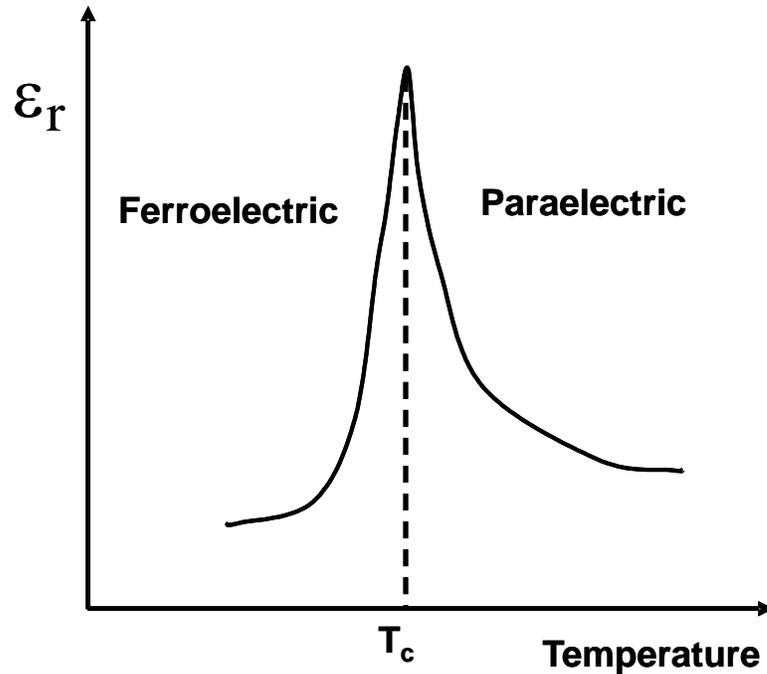


Figure 2.2: Permittivity versus temperature.

formulae ABO_3 , where A and B are cations. Ferroelectric materials have permanent electric dipoles and therefore exhibit spontaneous polarization. Among the 32 crystal classes, 11 of them have a center of symmetry and hence cannot exhibit ferroelectricity. Of the remaining 21 crystal classes, only 10 exhibit spontaneous polarization and can be classified as ferroelectrics. The classification of ferroelectrics based on symmetry is shown in Figure 2.3.

Over the past few decades $BaTiO_3$ has been extensively employed in transducers, capacitors and thermal detectors. R. B. Gary demonstrated the first working transducer using barium titanate in 1945 [15]. It was not long until lead zirconate:lead titanate (PZT) was developed for use in transducer applications in 1950s. Barium titanate, however, remained the candidate of choice for high density, multi-layered capacitors due to its high dielectric constant and ease of manufacturing.

It was recognized early on that ferroelectrics could be used in microwave applications. However, there has been a renewed interest in application of ferroelectrics for

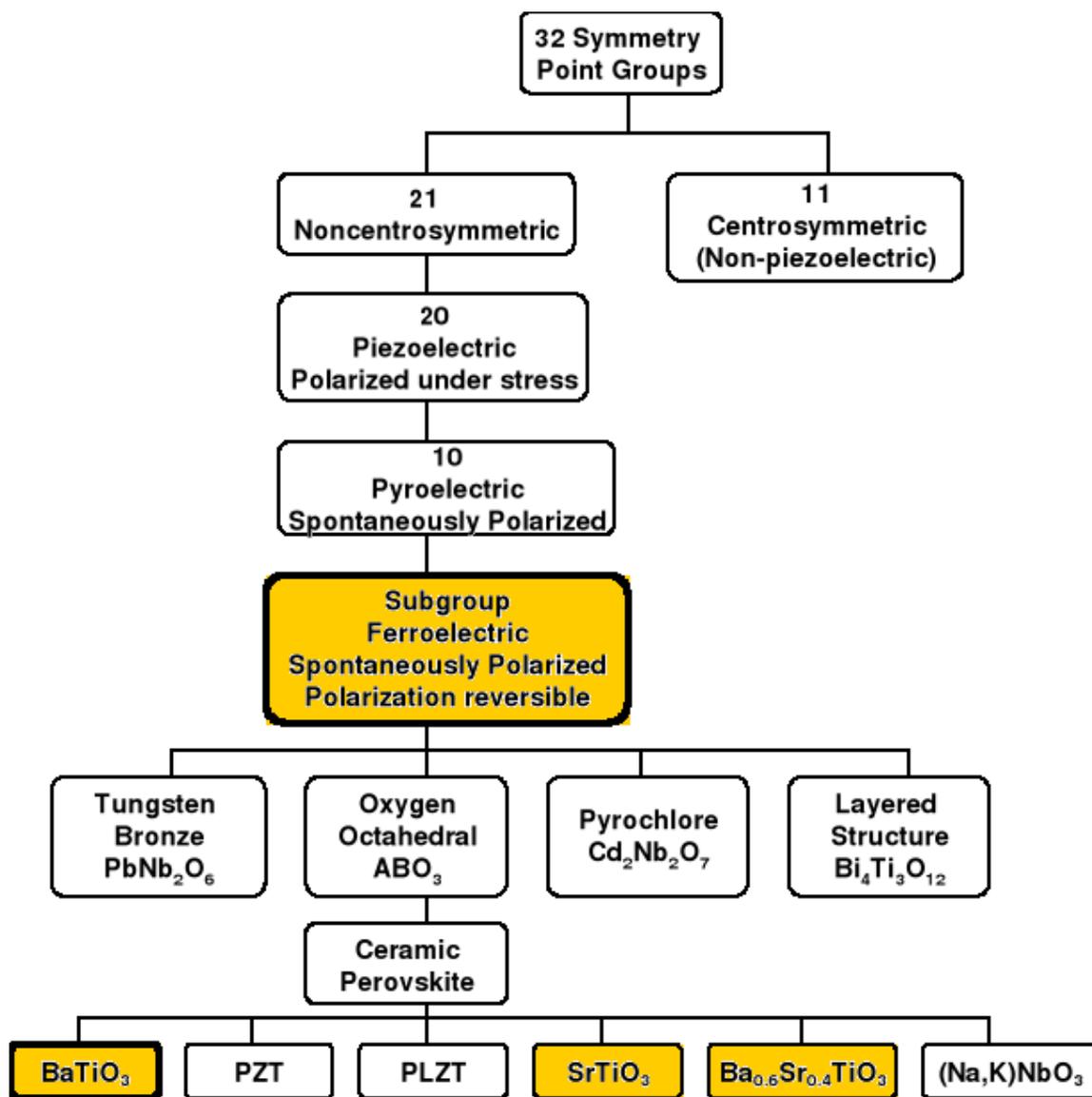


Figure 2.3: Interrelationship of piezoelectrics and subgroups on the basis of symmetry [12].

tunable microwave devices in the past decade. This is in large part due to advances in thin-film growth techniques and the ability to integrate ferroelectrics with semiconductor and ceramic technologies and thereby affording economy of scale. Integration with other technologies leads to miniaturization and also lower cost. Both thin-film and thick-film ferroelectric technology has been developed. Thin-film processes are those where the film thickness is $< 1 \mu\text{m}$ while processes resulting in film thicknesses $> 1 \mu\text{m}$ are considered thick-film processes. Both processes utilize the fact that application of an external bias leads to rearrangement of the microscopic dipoles in the material causing a change in the dielectric constant of the material (see Figure 2.5). It is to be noted that most ferroelectrics are used in their paraelectric phase, i.e above the Curie Temperature (T_c). It is well established that the absence of domain walls in the paraelectric phase results in lower loss tangent compared to the ferroelectric phase, thereby rendering the material in the paraelectric phase more suitable for microwave applications [16]. Despite this technical distinction, ferroelectrics used in the paraelectric phase for tunable microwave devices are still referred to as ferroelectric materials. A typical frequency response curve of a dielectric material is shown in Figure 2.4. This curve shows a general trend. The exact ranges of frequency where permittivity is non-dispersive with frequency is dependent on the material properties, growth techniques, and interfacial properties. For thin-film BST, permittivity has been shown to be flat with frequencies up to 50 GHz.

Ferroelectrics have been used as tunable dielectrics to fabricate varactors of both parallel plate and interdigital form. The most common ferroelectric used for tunable microwave devices is Barium Strontium Titanate (BST). It has a Curie temperature in the range of $-30 \text{ }^\circ\text{C}$ to $+10 \text{ }^\circ\text{C}$ depending on the stoichiometry of the film and deposition conditions. BST thin-film varactors have been used to demonstrate a wide variety of tunable microwave devices. Loaded-line phase shifters, low-pass and reflection type phase shifters, tunable planar filters, tunable matching networks, tunable antennas, and voltage controlled oscillators (VCO) using BST varactor as the tuning element have been successfully demonstrated. In the next section the characteristics of thin-film and thick-film BST will be discussed and potential applications will be highlighted.

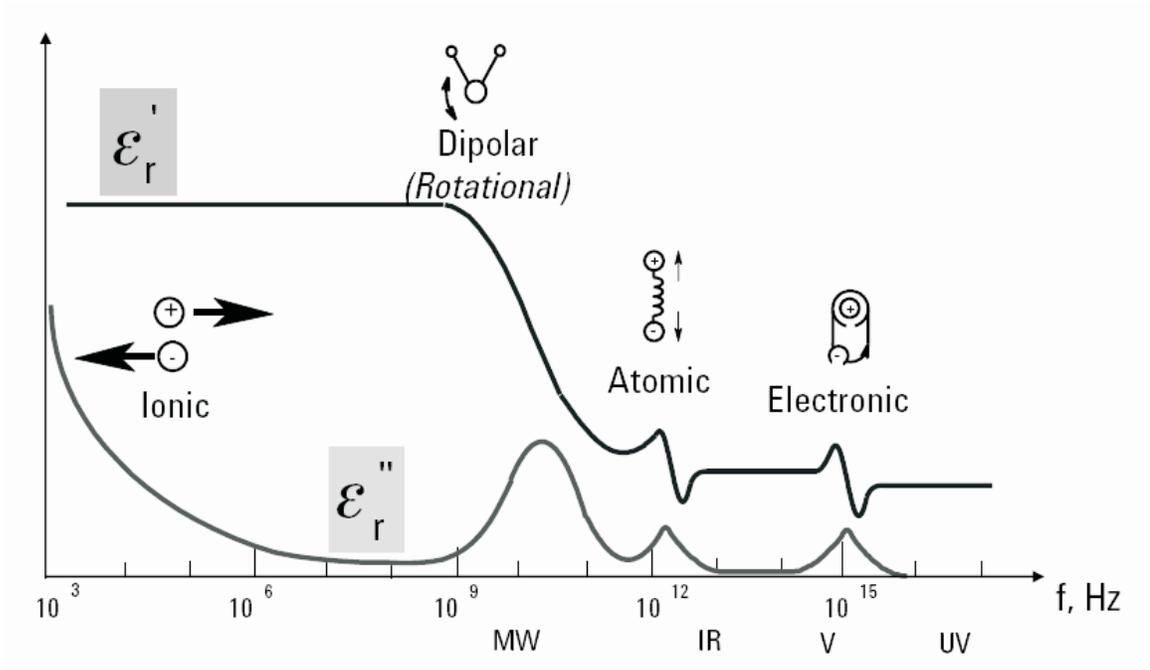


Figure 2.4: Frequency response of dielectric mechanisms [17], MW: Microwave, IR: Infra-red, V: Visible, UV: Ultra-violet

2.3 Bulk, thick-film, and thin-film BST

Thin-film processes are those where the resultant film thickness is $< 1 \mu\text{m}$ while processes resulting in film thicknesses greater than $> 1 \mu\text{m}$ are considered thick-film processes. A solid mass of ferroelectric single crystals will be considered as bulk BST in this work. The thickness of bulk BST is usually in the $500\text{--}2000 \mu\text{m}$ range. Bulk ferroelectrics are useful in substantial size reduction of microwave devices due to their high dielectric constant ($500\text{--}2000$). When used as substrates or as dielectric filling in transmission lines the linear dimensions becomes inversely related to the square root of the dielectric constant, thereby enabling a size reduction of a factor of $10\text{--}20$ corresponding to the dielectric constant range of approximately $100\text{--}400$. Bulk ferroelectrics can also be used in lens antennas for beam steering applications. One of the biggest drawbacks of bulk BST is that very high tuning voltages ($400\text{--}2000 \text{V}$) are typically required to achieve a usable tuning range. This limits their use in all but very specialized applications where the availability of high voltages is not of

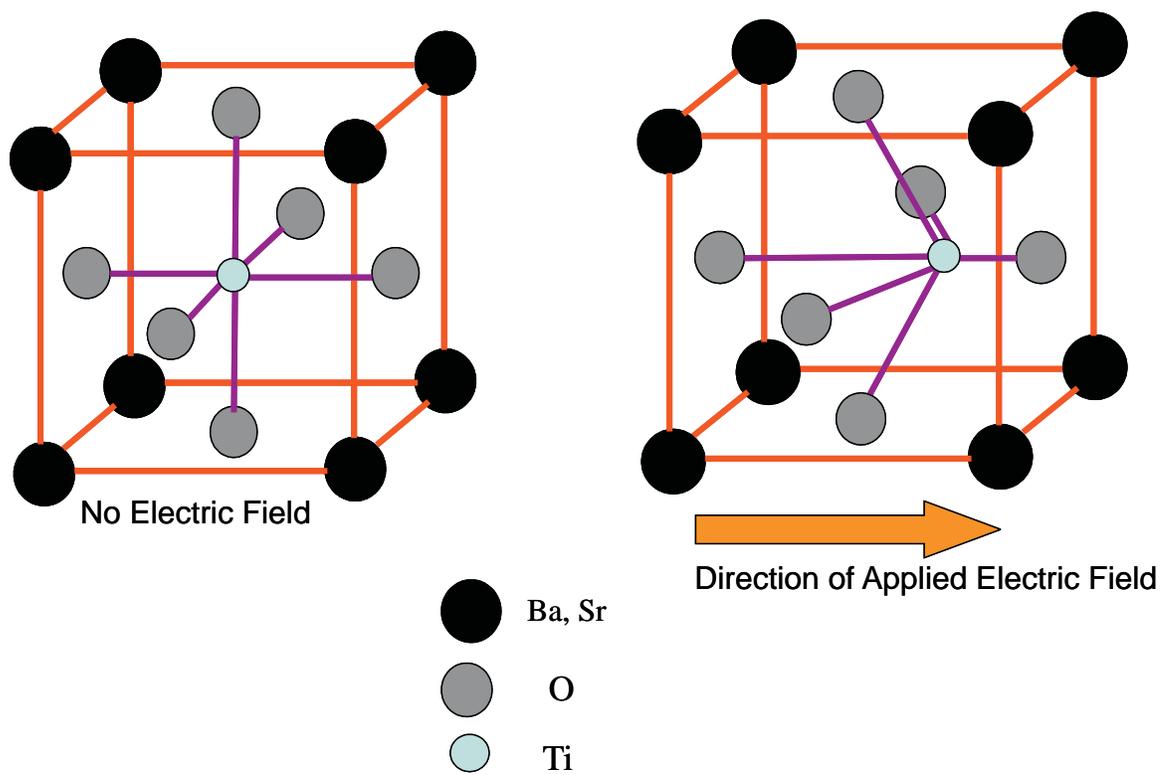


Figure 2.5: Rearrangement of unit cell in response to external electric field.

primary concern. As will be pointed out later, bulk BST typically exhibits lower loss tangent values than thin-film BST.

Thick-film BST is a considerably more practical form of BST requiring substantially lower tuning voltages and has been developed using screen-printing technology. It also affords integration with Low-Temperature Co-fired Ceramic (LTCC). Thickness usually ranges from 2–30 μm and tuning voltages in the range of 100–400 V have been achieved. Tunable filters, phase shifters and matching networks have been demonstrated using this technology. Hu *et al.* [18] demonstrated a reflection type phase shifter at 2.2–2.6 GHz with an average differential phase shift of 48° and insertion loss of 2.4 dB. The figure-of-merit (FOM) was 54 deg/dB at 2 GHz. The tuning voltage was 100 V. They used a 25 μm thick BST layer and 8 μm thick silver paste for the transmission line. Though the FOM is lower than that reported for thin-film phase shifters, the results look very promising. Jackoby *et al.* [19] has summarized the results for thick-film BST on alumina using a low-cost screen printing process and subsequent pressing and sintering. They reported loss tangent and permittivity in the range of 0.01 and 450 respectively at zero bias. The tunability was more than 60% for 20 V/ μm of applied field. They also reported a phase shifter with a 28 deg/dB FOM for a maximum field strength of 100 kV/cm. Other researchers have also reported tunable filters and matching networks using BST thick-film. The material showed a strong frequency dispersion and the dielectric quality factor was reported as 11 at room temperature and 10 GHz. The results, though promising, are not as good as that obtained with thin-film BST. The most important difference is that thin-film BST has been shown to have non-dispersive behavior up to 40 GHz. Furthermore, the tunability is lower than that of thin-film. This is in large part due to the fact that only a thin upper layer of the BST film is tunable. The rest of the layer is equivalent to a non-tunable capacitor in parallel with the tunable upper layer. This results in lower overall tuning range.

BST thin-film is very attractive for tunable microwave devices due to the low tuning voltages required, typically between 2 and 200 V, depending on the thin-film composition, film thickness, and capacitor configuration. Even though the dielectric loss is one order of magnitude lower than that of bulk BST, the lower tuning volt-

age and other integration benefits make thin-film BST a viable candidate. It can be produced using standard photolithographic process and could potentially be low cost. Typically substrates such as MgO, LaAlO₃, Sapphire and Alumina are used to grow BST-thin-film. Important considerations include good lattice matching with the substrate since the interfacial strain has been shown to affect the electrical properties of the BST thin-film. Silicon substrates, though a very attractive alternative, do not provide a good lattice matching and hence electrical properties are inferior. However a buffer layer provides a potential solution to this problem.

York *et al.* [20, 21] have demonstrated loaded-line phase shifters on sapphire and quartz substrates. Using a parallel plate capacitor configuration and less than 20 V tuning voltage they reported figures-of-merit of 93 deg/dB and 87 deg/dB at 6.3 and 8.5 GHz respectively.

2.4 Methods of growing BST thin-film

BST thin-film is grown by a wide variety of methods each with their own advantages. The method of choice is usually determined by the application, cost and system parameters. Broadly speaking, they can be divided into three main categories :

1. Physical Vapor Deposition (PVD)—this includes RF sputtering, molecular beam epitaxy (MBE) and pulsed laser deposition (PLD).
2. Chemical solution deposition (CSD)—this includes sol-gel and metal-organic decomposition.
3. Chemical Vapor Deposition (CVD)—this includes metalorganic chemical vapor deposition (MOCVD), and atomic layer deposition. (ALD)

Some of the preferred methods of growing BST thin-films will now be discussed. Chemical Solution Deposition (CSD) methods such as sol-gel are widely used for growing high quality BST thin-film at low cost and with good composition control.

It does not require vacuum infrastructure. The sol-gel method consists of a sequence of methods. First a stable dispersion (sol) of particles less than $0.1 \mu\text{m}$ in diameter is formed in a liquid from organic or inorganic precursors [22]. In the next step a gel is formed based on a change in concentration, aging, change in pH value of the liquid, or addition of a suitable electrolyte and three-dimensional bonding occurs. The remaining liquid is evaporated from the gel by heating or freeze-drying. Finally, the dehydrated gel is converted into powder by increasing the temperature. Van Keuls *et al.* [23] have demonstrated a phase shifter using CSD deposited BST thin-film on LaAlO_3 . The device had an insertion loss of 6.5 dB and a FOM of 40.9 deg/dB at 14.2 GHz. Various groups have also used this process for integrating BST with LTCC technology.

In the Pulsed Laser Deposition (PLD) technique a high-energy pulsed laser beam is focused on the surface of a target at an angle such that the substrate can sit directly in front of the target. The interaction of the pulsed laser ablates the material and produces a plume of material that is subsequently deposited on the substrate. The PLD method affords a very fast rate of deposition and the deposition temperature is also low. This can be beneficial in processes with limited thermal budgets. Bellotti *et al.* [24] reported a tunability of 65% for a bias field of 70 kV/cm and a quality factor of 4 at 20 GHz. Heteroepitaxial BST thin-film was deposited on $\text{LaAlO}_3/\text{MgO}$ using PLD. The paper also reports the effects of strain on tunability. Bubb *et al.* [25] also reported a high quality BST thin-film on MgO. A Q factor of 600 was reported at 6 GHz with tunability of 12%.

MOCVD is a widely used method for BST deposition. It is based upon a chemical reaction of chemicals called metalorganic precursors in a vapor phase. The metalorganic precursors are transported into the reactor chamber using a carrier gas. High temperature in the chamber decomposes the precursors and the liberated atoms recombine forming a compound. It offers many advantages including: large area growth, conformal deposition, excellent composition control, and uniformity. Tombak *et al.* [26] have also reported parallel plate metal-insulator-metal (MIM) varactors on silicon using MOCVD BST. They reported varactors using both platinum (Pt) and tungsten (W) electrodes on standard silicon substrates.

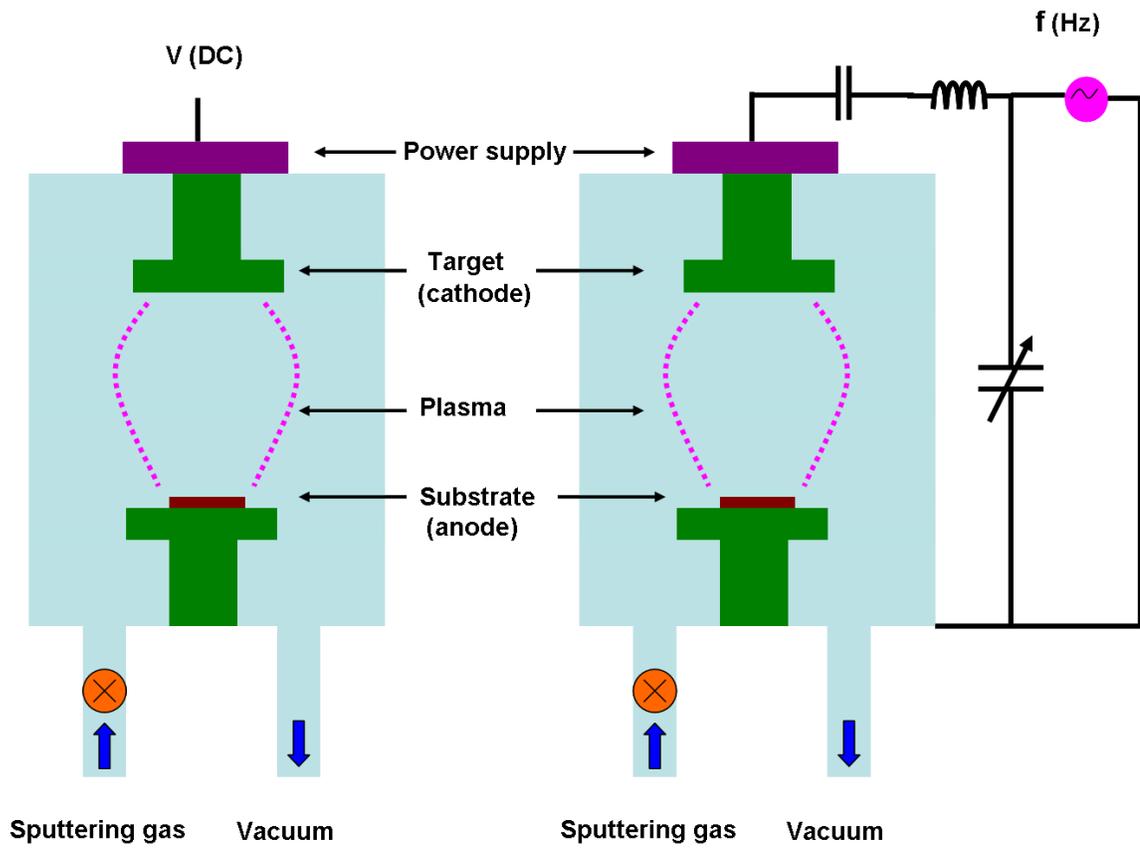


Figure 2.6: Schematic of DC and RF sputtering chamber.

Courtesy of Dr. Jon-Paul Maria

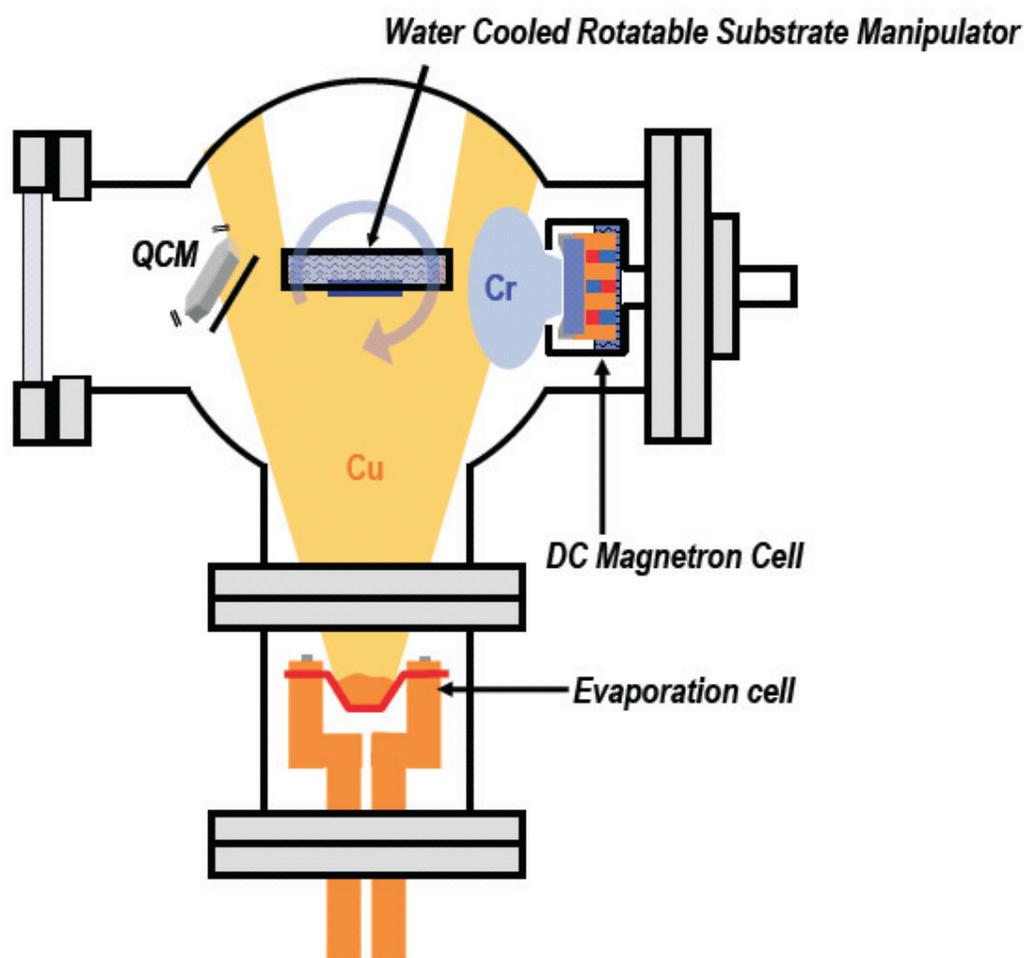


Figure 2.7: Schematic of a dual evaporation and RF sputtering chamber.

Courtesy of Dr. Jon-Paul Maria

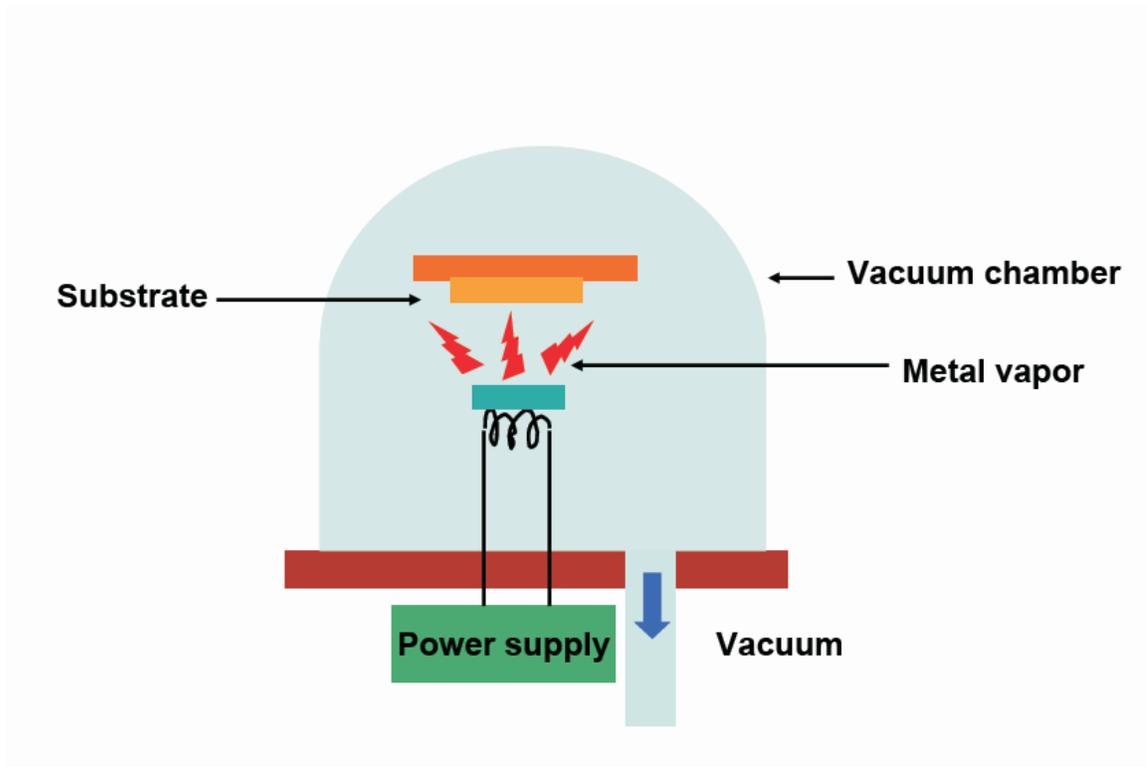


Figure 2.8: Schematic of an evaporation chamber [27].

RF sputtering is by far the most commonly used method for BST thin-film growth. Various groups have reported varactors and devices using this versatile technique. It is a physical vapor deposition process which involves removal of material from a solid cathode [28]. The cathode is bombarded by positive ions emitted from a rare gas discharge. The ions with high kinetic energy displace or sputter atoms from the material. The sputtered atoms then get deposited on the substrate. Sputtering is usually done either in a DC chamber or RF chamber. In the former a DC current is used to create a discharge while in the latter process RF energy, usually at 13.56 MHz, is used to create the plasma discharge. DC sputtering is mostly used for metal and other conductive oxides. RF sputtering is employed for dielectrics and other non-conducting materials. The RF cycle is necessary to remove the charge build up on the non-conductive target. RF sputtering chambers also need a matching network that impedance matches the chamber to the RF source for optimum transfer of energy to the target. Both DC and RF sputtering techniques can employ either diode or magnetron as sputter source. The diode source offers the following advantages:

- Cheap and very simple.
- Available in large production sizes.
- Uniform plasma is created between anode and cathode, this leads to uniform consumption of the sputter target.

The disadvantages of a diode source are as follows:

- Inefficient use of electrons to maintain the plasma.
- Electrons can cause substrate damage.
- Low deposition rates.

Magnetron sputter sources use a magnetic field to control the motion of electrons. This is accomplished by placing a permanent magnet behind the target. The advantages offered by a magnetron source are following:

- Reduction in substrate bombardment.
- Increased deposition rate.
- High efficiency due to increased plasma density.

The disadvantages of a magnetron source are following:

- Source is complex and hence more expensive.
- Uneven consumption of the sputter target due to localization of plasma in a ring around the center of the target.

Despite the added cost and complexity of a magnetron sputter chamber the advantages are quite compelling that they warrant widespread use. The quality and the properties of BST thin-film deposited by sputtering technique is dependent on numerous parameters such as substrate temperature, partial pressure of oxygen, total sputtering pressure, RF power and composition of the target, and the ratio of the partial pressure of Ar and O₂.

Padmini *et al.* [29] have investigated the effect of texturing on the tunability of BST films. They concluded that <100> textured BST thin-film shows good tunability under optimized conditions. They optimized the deposition conditions such that the film was predominantly <100>. It was noted that a biaxial tension in the film results in the polar axis of the material orienting itself along the substrate surface and this results in increased tunability.

Xu *et al.* [30] studied the effect of substrate and post deposition anneal on the properties of sputtered BST film on MgO and LaAlO₃. They reported better tunability on MgO compared to LaAlO₃ due to tensile stress in the former. Tunability was also improved by post deposition anneal in air at 900 °C for 5 hours. The tunability obtained was 22% for 100 kV/cm (10 V/μm) and a loss tangent of 0.0023 at 1 MHz and room temperature.

2.5 Characterization of BST thin-film

BST thin-film is typically characterized for electrical and physical properties. The method of choice for physical characterization are following:

- **X-Ray Diffraction(XRD)** — characterize the texture/orientation of the BST film.
- **Atomic Force Microscopy (AFM)** — evaluate surface roughness and morphology of the BST film.
- **Scanning Electron Microscopy (SEM)** — characterize thickness and surface of the film.
- **Profilometry** — measure film thickness.

Electrical characterization involves the following:

- **LCR Meter** — Capacitance and loss tangent versus voltage and frequency. Usually accurate up to 10 MHz.
- **Impedance Analyzer** — Capacitance and loss tangent versus voltage and frequency. Usually accurate up to 3 GHz, measurement range overlaps with LCR meter.
- **Electrometer, DC parameter Analyzer** — Leakage current versus voltage and time. Also reliability measurement.
- **Hot-Cold Stage** – Capacitance and loss tangent versus temperature.
- **Vector Network Analyzer** — Model extraction and impedance data up to 50 GHz.
- **Signal Generators and Spectrum Analyzer** — Nonlinear characterization and modeling.

The common methods used for the electrical characterization of BST thin-film will now be discussed. The BST thin-film to be characterized is measured as such or embedded in a circuit in the form of a varactor or a tuning element. Capacitance and loss tangent is then extracted from the measured data. The accuracy of characterization technique depends on the frequency range of interest. The frequency range determines whether the fixturing and other peripheral effects can be ignored without compromising the accuracy of the measurement. For instance a simple parallel RC model may work very well at few tens of MHz but the same model would results in erroneous results if fixturing effects are not properly accounted for and calibrated out of the measured data. Also at higher frequencies a distributed model may be required to accurately extract the capacitance and loss tangent data. In general, the higher the frequency of measurement the greater is the effort involved in the measurement and the accuracy degrades with increasing frequency range.

Certain techniques such as the resonant cavity method are well suited for thick-film/bulk BST and yield very accurate result at one frequency point even at microwave frequencies. Thin-film BST is typically much more difficult to characterize than thick-film/bulk BST. One of the simplest characterization techniques is the one using lumped element capacitors; either in parallel plate or interdigital configuration. LCR meters and Impedance Analyzers employ a RF I-V test method in which a current is forced through the capacitor under test and the voltage drop across it is measured. Some LCR meters also use bridge balancing technique similar in principle to the classic Wheatstone bridge. Both methods yield complex impedance and capacitance and loss tangent data is extracted using either a parallel or series RC model. LCR meters generally do not require additional calibration structure and they are accurate to up to 10 MHz. Impedance Analyzers such as the Agilent 4991A use additional calibration to extend the test frequency to 3 GHz. Open, short and $50\ \Omega$ load are the typical calibration structures used for removing test fixture parasitics. Impedance analyzer also provide one-port reflection data which can be directly used in a circuit simulator for model fitting. Network Analyzers typically measure one-port reflection data using ratio of reflected to incident power. The measured S-parameters can be converted into impedance or Z-parameter using Equation (2.1).

$$Z_{in} = Z_o \frac{1 + S_{11}}{1 - S_{11}} \quad (2.1)$$

where Z_o is usually 50Ω .

Extraction of capacitance using a network analyzer is usually more accurate than extraction of loss tangent data. This is because the loss measured is the total loss in the device and the separation of metallic losses from dielectric loss becomes very difficult at high frequencies. At RF frequencies the metal loss begins to dominate the total loss in the device under test and this increases the uncertainty in the extraction of the dielectric loss. Accuracy is typically increased by using additional calibration structures to remove the effect of parasitics and accurately calculate metallic loss. The total device quality factor can be conveniently calculated using the network analyzer. Equation (2.2) can be used to extract Q factor from the measured complex reflection coefficient once it has been converted to Z-parameter using Equation (2.1).

$$Q = \frac{|Im(Z_{in})|}{|Re(Z_{in})|} \quad (2.2)$$

Alternatively in terms of one-port S parameter:

$$Q = \frac{|2(Im(S_{11}))|}{|1 - (Im(S_{11}))^2 - (Re(S_{11}))^2|} \quad (2.3)$$

It can be seen from Equation (2.3) that the Q factor is highly sensitive to errors in the measurement of the complex reflection coefficient. Figures 2.9 and 2.10 show the results of the sensitivity analysis of Q factor in terms of the error in the imaginary and real part of the complex reflection coefficient respectively. The plots were generated for a Q factor of 34 with 0.97 and 0.05 as the imaginary and real part of S_{11} respectively. It is evident from the plots that the error in Q factor is very sensitive to errors in the imaginary part of the reflection coefficient. Hence, extreme care must be exercised while measuring Q factor with a network analyzer. It can similarly be shown that the sensitivity of Q factor with an RF I-V method is considerably better.

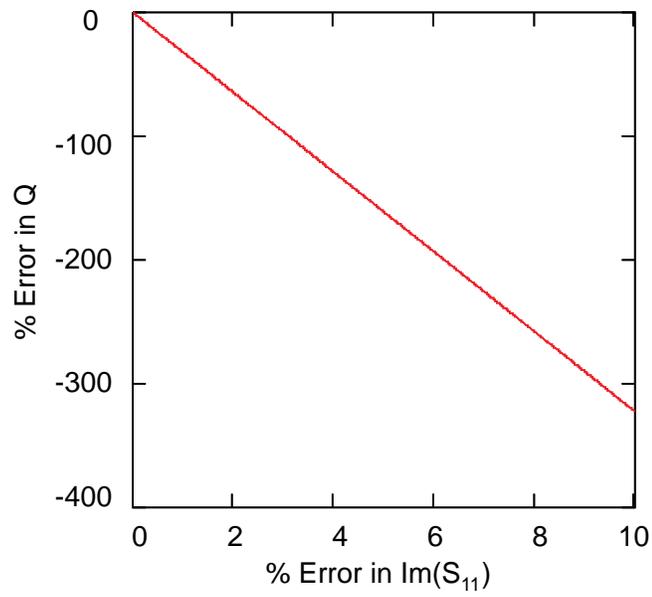


Figure 2.9: Q factor error versus error in $\text{Im}(S_{11})$.

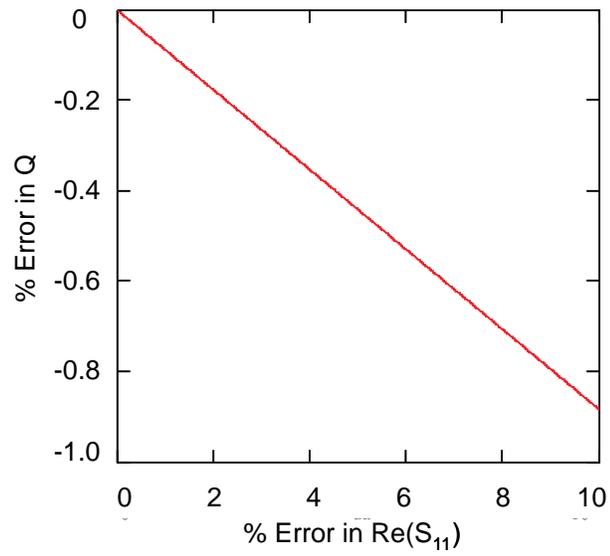


Figure 2.10: Q factor error versus error in $\text{Re}(S_{11})$.

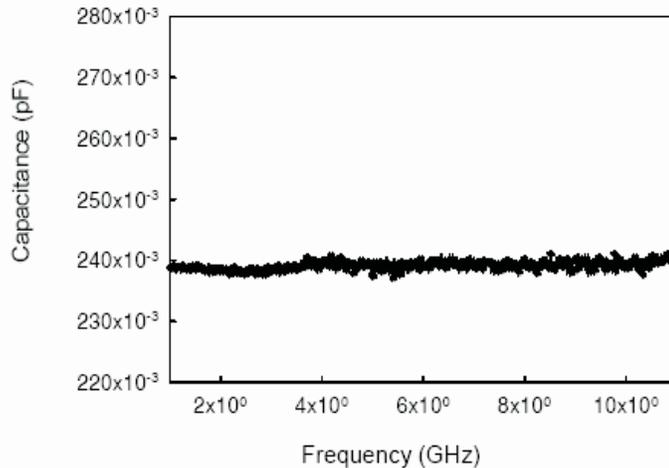


Figure 2.11: Capacitance versus frequency of a BST capacitor (after Zhu *et al.* [32]).

Jin [31] has demonstrated that in a two-port measurement configuration the accuracy in parameter extraction is increased. Experimental results using Jin's work was reported by Zhu *et al.* [32]. They used three structures, namely the capacitor under test embedded in a transmission line and two other through lines to remove the effect of transmission lines in which the capacitor was embedded. Explicit formulae for capacitance and loss tangent in terms of measured parameters was reported. The BST film thickness was 200 nm deposited using PLD. Tunability of 2.4:1 at 15 V bias and a loss tangent of less than 0.012 up to 10 GHz was reported. The extracted capacitance value showed little dispersion with frequency, see Figure 2.11. However, the loss tangent value varied by over 70% between 1 and 12 GHz, see Figure 2.12.

Other two port parameter extraction techniques using the network analyzer include measurement of co-planar transmission line, planar resonators and coupled line. Formulae derived using conformal mapping technique are then used to extract permittivity and loss tangent data from the measured S parameters. There have been some reports in the literature regarding this extraction technique but there seems to be some disagreement over the dispersion properties of the dielectric constant and the loss tangent of the BST film. Lue *et al.* [33] have reported such a technique using a combination of Thru-Reflect-Line (TRL) and conformal mapping technique.

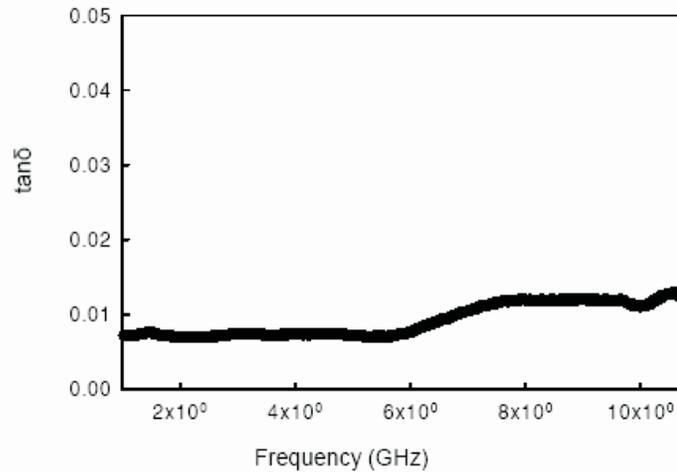


Figure 2.12: Loss tangent versus frequency of BST thin-film (after Zhu *et al.* [32]).

The extracted loss tangent data reported by them shows considerable dispersion at frequencies below 5 GHz. This can be seen in Figure 2.13.

2.6 BST-based tunable filters

Tunable filters using thick film, thin-film and bulk BST have been reported in the literature. Various university groups have reported BST thin-film based filters. There are at least four companies that are pursuing the commercialization of this technology for tunable applications. They are:

1. Paratek Inc., USA [34, 38].
2. Agile Materials and Technologies Inc., USA [35].
3. nGimat Inc., USA [36].
4. Gennum Corporation, Canada [37].

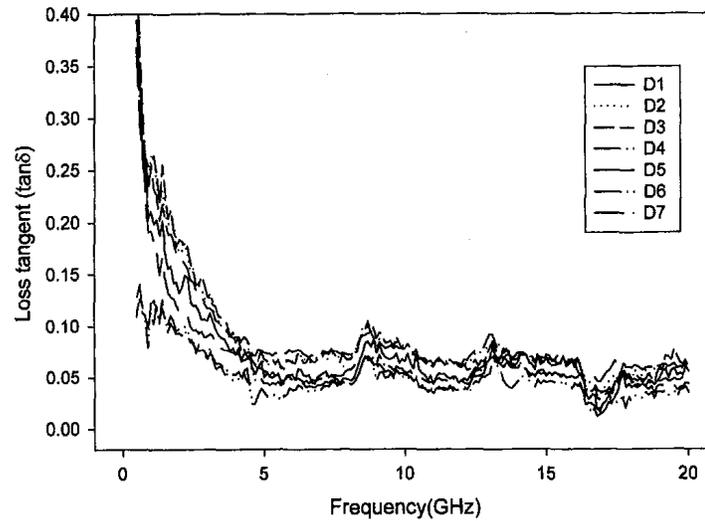


Figure 2.13: Calculated loss tangent versus frequency of BST thin-film. D1, D2, D3, etc. represent different samples with varying permittivity, for details see Lue *et al.* [33].

Apart from the four companies mentioned above, other large corporations such as Samsung, Nokia, Rockwell Scientific, Matsuhita and others are also pursuing or supporting their own internal research and development programs in this area.

Planar filters using either a single layer or multiple layer configuration are commonly used. A combination of lumped and distributed approach is usually employed. Filters using a single layer BST and metal use a interdigital or a gap capacitor configuration while those employing a single layer BST and two or more levels of metal use a parallel plate configuration. In the single layer configuration tuning is sometimes also achieved by applying bias voltage across the substrate/BST thin-film stack up. Though this technique is attractive from a fabrication and analysis point of view, the bias voltage required to achieve reasonable tuning tends to be prohibitive for almost all but the very specialized systems. Configurations where bias is applied locally through the BST is more promising in terms of realizability and integration with other systems.

Kozyrev *et al.* [39] reported a 20 GHz tunable filter using BST thick-film gap capacitors on MgO with silver electrodes. They reported a 3:1 change in capacitance

at 20 GHz with loss tangents in the range of 0.1–0.05 with 0–400 V bias. The sintered thickness of BST was 5 μm . The filter was based on a symmetrical finline topology in a rectangular waveguide. A 9% (1.8 GHz at 20 GHz nominal center frequency) tuning of the center frequency was obtained with maximum insertion loss of 3.5 dB and a 3 dB bandwidth of 3.5%. This is one of the first tunable filter reported using BST thick-film technology at room temperature.

Findikoglu *et al.* [40] described a 3-pole tunable bandpass filter on LaAlO_3 using a Strontium Titanate (1.2 μm) and YBCO thin-film combination to reduce conductor losses. The filter had a bandwidth of less than 2% and tuned more than 15% at 4 K and 76 K. The center frequency was at 2.3–2.4 GHz and the insertion loss was in the range of 16–30 dB at zero bias and improved to 3–6 dB at bias voltages over 100 V. One of the drawbacks of the filter was the relatively high insertion loss despite the additional cost associated with cryogenic cooling.

Eriksson *et al.* [41] reported a two-pole bandpass filter based on YBCO and plated single crystal KTO disk resonators. The filter operated at 0.9 GHz with a 1.5% bandwidth at 77 K. With 500 V bias, 5% tuning range was obtained. The insertion loss ranged from 1.6–4.7 dB over the tuning range. This result was comparable with commercially available tunable filter of similar characteristics.

Subramanyam *et al.* [42] reported a K-band microstrip bandpass filter using a thin-film HTS/Ferroelectric/Dielectric multi-layer configuration. They used a thin-film of YBCO/STO on LaAlO_3 dielectric substrates. The STO layer was 0.3 μm thick while the HTS was 0.35 μm thick. The two pole filter was centered at 19 GHz with a 7% measured bandwidth. The passband of the filter showed considerable distortion. At 77 K the minimum insertion loss was 3.3 dB and a tuning range of 9% at 17.4 GHz with ± 500 V bias was reported. The same filter was investigated at 24 K and a demonstrated a slightly degraded insertion loss of 4.4 dB at zero bias. However, the tunability improved to 14% with ± 400 V. A comparative filter with the HTS thin-film but measured at 77 K showed considerably higher loss of 6 dB. The same group also reported a two-pole filter [43] on MgO using pulse laser ablated 0.35 μm BST thin-film and gold multi-layer configuration. The filter demonstrated a rather low tunability of 3% with ± 100 V bias at room temperature. The 3-dB bandwidth

was 500 MHz at 17.2 GHz and insertion loss ranged from 8.1 dB at the zero bias state to 5.3 dB at the high bias state.

Roy *et al.* [44] reported a tunable filter at VHF frequencies using bulk ferroelectrics. The filter showed a tuning range of 1.75:1 with 200 V bias. The insertion loss at 77 MHz was approximately 2 dB and increased to 7 dB at 137 MHz. The authors reported that these losses were corrected for conductor loss but the exact methodology was not described. It is expected that the actual losses would be much higher than the reported values.

Vendik *et al.* [45] reported a 3-pole tunable filter using BST film at room temperature. Tunable capacitors were formed by a 10 μm gap in the microstrip line. The insertion loss was 15 dB at zero bias and at the center frequency of 4.4 GHz. The loss improved to 7 dB at the high bias state of 150 V at 4.65 GHz. The tuning range was 5.7%. The loss tangent values for the BST film ranged from 0.044 to 0.017 at the zero and high bias states respectively.

Tombak *et al.* [46] have reported tunable lowpass and bandpass filters in the VHF range using parallel plate BST thin-film capacitors and 0–6 V tuning voltage. The tuning voltage is considerably lower than the high bias voltages required for filters using planar or interdigitated capacitors. This feature lends itself to easy integration with many systems where higher bias voltages are not available. The authors used MIM capacitors fabricated on silicon using a MOCVD BST thin-film process and Pt electrodes. The capacitors were subsequently singulated from the wafer and used in discrete form. They reported both a third and fifth order lowpass filter. The fifth order lowpass filter had an insertion loss of 2 dB and a tunability of 40% (120–170 MHz) with the application of 0–9 V DC bias. The IIP3 of the filter was +22 dBm at zero bias voltage. IIP3 or input IP3 (third-order intercept point) is defined as the extrapolated input power level of a single tone for which the output power of the third-order intermodulation products equals that of the single-tone linear fundamental output power. The third-order filter had an insertion loss of 0.8 dB and a 30% (120–170 MHz) tuning range. The IIP3 at zero bias was +24 dBm. The bandpass filter showed a tunability of 57% (176–276 MHz) with 0–6 V bias. The passband insertion loss was 3 dB and the IIP3 was measured to be +19 dBm.

Noren *et al.* [47] also reported a two-pole bandpass filter with 35% center frequency tuning from 910 to 1230 MHz for a 50% reduction in capacitance. The insertion loss was in the range of 6–7 dB over the tuning range. As means of alleviating the insertion loss they also presented a technique of shunting the tunable capacitor with a high Q ceramic resonator to improve the Q factor at cost of reduced tuning range. A 7% tuning range for a 50% reduction in capacitance was reported. Q factor ranged from 135–217 over the tuning range.

Rahman *et al.* [48] have reported a 3-pole tunable combline bandpass filter using BST thin-film and LTCC technology. The filter was targeted at the commercial cellphone market. The filter tuned from 1656 MHz to 1983 MHz with an average insertion loss of 4.3 dB. The tuning voltage requirements were not indicated in the paper.

Overall, a wide variety of BST based tunable filter have been reported in the literature. In general MIM based filters have lower tuning voltage requirement than planar capacitors at the expense of reduced linearity. Planar capacitor based filters tend to have higher power handling capabilities. Most filters have been reported on single crystal substrates and at cryogenic temperatures. In the next section BST-based tunable phase shifters will be reviewed.

2.7 BST-based tunable phase shifter

A phase shifter is a device that will provide a variable insertion phase in a microwave signal path without changing the physical path length [49]. Phase shifters are used in many different applications. Some of the most important ones are in phased array radars, synthetic aperture radars, diversity combining schemes, and adaptive antenna configurations. Phase shifters can be broadly classified into the following categories:

1. Digital
2. Loaded line

3. Reflection type
4. Switched line
5. Low-pass/High-pass

Digital, Switched line, and Low-pass/High-pass phase shifter typically use switches and are more suitable for applications requiring discrete values of phase shift. The loaded line and the reflection type phase shifters lend themselves to analog phase shifter design where a variable reactance element can be employed to achieve continuous phase tuning. In this section only these two types of phase shifters will be discussed and a survey of BST thin-film based phase shifters reported using these topologies will be presented.

Nagra *et al.* [50] expanded on the work by Rodwell *et al.* [51] and reported optimization techniques for loaded line phase shifters. They reported a 0–360 degree phase shift at 20 GHz with 4.2 dB of insertion loss. Liu *et al.* [21] reported a BST thin-film phase shifter loaded with interdigital varactors on a sapphire substrate. With a 1 μm gap (separation between two electrodes, see Section 3.2 for details) in IDC, differential phase shift of 110° at 20 GHz was reported. The insertion loss was 3.4 dB, resulting in a 32 deg/dB FOM (figure-of-merit). The tuning voltage was 100 V. Acikel *et al.* [20] also reported a phase shifter in the Ku/Ka band using parallel plate and IDC varactors on sapphire and glass substrates. The parallel plate version showed a phase shift of 180° with 4 dB of insertion loss at 30 GHz. The tuning voltage was 30 V. The IDC version showed a tuning of 460 degrees at 8 GHz with 8.8 dB of loss. Both circuits showed a promising FOM of 60 deg/dB at 10 GHz. Sullivan *et al.* [52] recently reported an adaptive duplexer using the BST phase shifter developed by the UCSB (University of California Santa Barbara) group. They employed a single-path feedforward technique to achieve over 20 dB improvement in isolation over a 2 MHz bandwidth.

Kim *et al.* [53] have reported reflection-type phase shifters using BST interdigital varactors on sapphire using the CCVD (chemical combustion vapor deposition technique) and copper metallization. The circuit consisted of a Lange coupler with

a series LC termination. By changing the capacitance, the phase of the reflection coefficient is changed and phase shifting through the network is achieved. The phase shifter operated in the 1.9–2.5 GHz range with a phase shift of over 90° and better than 2 dB of insertion loss. A maximum figure of merit of 72 deg/dB was achieved at 2GHz. They also reported IIP3 of +32 dBm and +41.9 dBm for 0 and 60 V bias respectively. The same group has also reported a phase shifter using an all-pass network consisting only of lumped elements and a size of less than 2.2 mm X 2.6 mm at 2.4 GHz [54]. The phase shifter provides for over 121 degrees of phase shift with a maximum insertion loss of 3.75 dB from 2.4–2.5 GHz. The figure of merits of both single and double section phase shifters was over 65 deg/dB from 2.4 to 2.5 GHz.

In a subsequent publication [55] they also reported a temperature optimized device with the figure of merit of 62.5 deg/dB ± 2.5 deg/dB from 10 °C to 75 °C. The temperature variation of the phase shift was held to less than 4° over 10 °C to -50 °C . They investigated different ratios of Ba/Sr and (Ba+Sr)/Ti for minimizing the temperature variation and found that a Ba/Sr ratio of 1.2 : 1 and (Ba+Sr)/Ti ratio of 0.8 : 1 yielded a C_{\max}/C_{\min} variation of 1.17. As an application of the phase shifter the group demonstrated a ferroelectric smart antenna system for WLAN where the antenna automatically adjusts to the interference null by dynamically changing the phase shift in the beam forming network [56].

Kuylentierna *et al.* [57, 58] have reported true-time delay lines using BST thin-film parallel plate varactors on high resistivity silicon. They used laser ablation process and gold metallization in a coplanar strip loaded line configuration for circuit fabrication. The absolute group delay was reported to be 70 ps at room temperature and tunable by up to 20% under 20 V bias voltage. The insertion loss was less than 3.5 dB at 20 GHz. At a much cooler temperature of 145 K the group delay increased to 100 ps and the tunability to 50% under similar bias conditions. At 7 GHz, the insertion loss was 3 dB, resulting in a figure of merit of 0.03 dB/ps and 50 ps/mm. The leakage current at room temperature was less than 0.1 μ A.

Romanofsky *et al.* [59] have also reported phase shifter for phased array and reflectarray applications. A linear array at 23.675 GHz using 16 ferroelectric phase shifters on a 1 cm \times 0.75 cm MgO substrate was reported. 36° of scan

angle was achieved. The authors also reported phase shifter using CCVD and PLD methods on LaAlO_3 and Sapphire respectively. The figure of merit was reported as 50 deg/dB and 18 deg/dB for the PLD and CCVD films respectively at 20 GHz [60].

Lee *et al.* [61] have reported a 10 GHz phase shifter using BST IDC varactors on MgO. Phase shift of 153° was obtained at 10 GHz with 11.6 dB of loss. Relatively high tuning was obtained using only 40 V bias. This was accomplished by inserting a seed layer of thin BaTiO_3 (BT) with a lattice parameter intermediate between those of BST thin-film and MgO. This relieves the lattice mismatch stress in the BST thin-film and improves its dielectric properties. A large capacitance tuning of 78% with 133 kV/cm and loss tangent in the range of 0.024 and 0.01 between 0 and 40 V bias was reported. The same group has also reported a PLD BST thin-film deposited on MgO which was used to fabricate a loaded line phase shifter using interdigital varactors. The phase shift was reported to be 179° with an insertion loss of 5.6 dB at zero bias at 20 GHz. At the high end of the bias range (200 V) the insertion loss decreased to 2.1 dB. The figure of merit was 32 deg/dB.

A silicon based phase shifter using high resistivity silicon substrates and TiO_2 buffer layer was reported by K.-B. Kim *et al.* [62]. They used a PLD technique for depositing $0.5 \mu\text{m}$ BST thin-film. Phase shift of 98° at 50 V and 17 GHz was reported. The figure of merit was 10.5 deg/dB at 17 GHz. Though the FOM is quite low it is a promising technology that will lead to monolithic integration. This has the potential of greatly reducing cost and also improving reliability.

Ryu *et al.* [63] have reported a tunable phase shifter on MgO using PLD deposited BST thin-film. The film thickness was 400 nm and 60/40 composition of Ba/Sr was used. They used RF-ion milling to remove BST from the substrate except for areas in which the interdigital fingers were located. They measured a 179° phase shift at 20 GHz with maximum insertion loss of 5.6 dB. A FOM of 32 deg/dB was achieved.

BST-based phase shifters have the potential of reducing the cost of phased-array systems while providing a figure-of-merit which is comparable to or better than that of semiconductor or ferrite- based phase shifters. Potential size and weight reduction are also important features.

2.8 BST-based oscillators

VCOs are perhaps the most ubiquitous element in all communication systems, wired or wireless. In a wireless system the quality of the communication link is determined in large part by the characteristics of the VCO. A reversed bias semiconductor junction is typically used as the tuning capacitor in a VCO, wherein the applied voltage changes the depletion width and hence the tuning capacitance. The figure of merit of the VCO is primarily determined by the quality of the capacitor used and the RF voltage that can be applied across the capacitor. The varactor must operate in the reversed bias region to avoid forward conduction and excess shot noise. Thus there is a limit to the RF voltage swing that can be impressed upon the capacitor and this imposes an inherent limitation on the lowest achievable phase noise in the VCO. This is in sharp contrast to the BST varactor which can handle high RF voltage swings since there is no equivalent of a forward biased junction as in the case of a conventional semiconductor varactor. Now, the Q factor of a semiconductor varactor increases with increasing bias. Thus, while increased resonator Q is desirable, the increased RF voltage peak plus DC tuning voltage risks forward biasing the semiconductor junction. This is known as the junction bias effect and is minimized by using an array of back-to-back varactors. The BST varactor does not suffer this consequence. Thus a BST-based VCO is expected to offer better performance than a semiconductor based VCO in terms of harmonic performance and phase noise, especially $1/f$ noise. However, there are very few reports of BST thin-film based VCO in the open literature. Some of them are discussed below.

Paratek Inc. markets tunable oscillators based on BST varactors and they also hold several US patents [64] in that area. They have however not reported any data in the open literature. Recently Xu *et al.* [65] have also used BST thin-film varactor as decoupling elements in high-power on chip GaN (Gallium Nitride) VCOs due to their high capacitance density. This enables high values decoupling capacitors to be integrated on-chip.

2.9 BST-based tunable antennas and matching networks

Reconfigurable antennas are very useful in multi-functional and multi-band wireless communication devices. They also find use in electronic surveillance, countermeasures and other defense applications. The properties of these antennas can be adapted in real time to achieve selectivity in frequency, bandwidth, polarization and gain. Compared to broadband antennas, tunable antennas offer certain significant advantages. They have a small footprint and have similar radiation pattern and gain for all frequencies of operation. They offer judicious use of the electromagnetic spectrum and their frequency selectivity is useful for reducing co-site interference and jamming. Furthermore, a reconfigurable narrowband antenna can also enable low power transceivers by potentially eliminating the losses in duplexers.

Tunable antennas have been typically fabricated by loading a microstrip patch antenna with varactors [68]. Tuning can either be voltage controlled or optically controlled. Since the antenna is reactively loaded, the resonant frequency of the antenna can be changed by changing the reactance. All of these implementations use discrete components such as PIN diodes, varactor diodes or switches to vary the resonant frequency.

Tunable matching networks are required for multi-band devices using a single antenna. Even for single-band devices the antenna impedance varies over time due to human and environmental capacitive effects. A dynamically tunable matching network will optimize the power transfer for varying usage conditions. The design of efficient Power Amplifiers (PA) is essential for reducing the power consumption and hence increasing battery life and potentially reducing the size of the wireless device. The PA in a multi-band, multi-standard phone must operate efficiently across different frequency bands. The two most common circuit configurations used are multiple PAs optimized for each band and selected using switches and single broadband PA with tunable matching network either by using switches or varactors. Considerable work has been done in the area of MEMS-based tunable matching networks using either

MEMS switches or varactors. Though MEMS is a very promising technology; it still has very stringent packaging requirements and consequently higher cost. Reliability is also a concern. Semiconductor varactor-based tunable matching networks have been implemented by many researchers but they suffer from poor linearity performance.

Chen *et al.* [66] recently reported a BST thin-film parallel plate varactor based tunable matching network at 900 and 450 MHz on sapphire. The impedance transformer network was capable of transforming a 50Ω impedance to range of values between 13–29 Ohm at 900 MHz. Using a slightly modified network, antenna matching was obtained over 425–490 MHz with approximately 1.5 dB of insertion loss. A narrowband matching with less than 0.6 dB of loss was also reported.

Scheele *et al.* [67] have also reported an impedance matching network using discrete BST interdigital varactor fabricated on alumina using a screen printing process. They reported an insertion loss of 1.15 dB for 50Ω source and load impedances. The tuning range was from approximately 1880 MHz to 2000 MHz (6.4%) for 100 V bias. They also reported nonlinear characterization of the matching network at different power levels. IIP3 of +46.5 dBm and +52.8 dBm at +26 dBm and +33 dBm average input power was reported. Applications include real-time antenna impedance matching. However, it should be noted that the tuning range is far too low for many applications and could only be used for trimming the desired response to compensate for manufacturing tolerances.

2.10 Conclusion

A summary of BST tuning mechanisms and techniques for characterizing BST thin-film was presented. Fundamental concepts were also reviewed. A survey of frequency-agile devices using thick-film, thin-film and bulk BST was also presented. A range of devices fabricated on various substrates using optimized deposition techniques have been described. Most authors have used expensive single crystalline substrates for BST thin-film fabrication as it is usually believed that epitaxial growth of BST thin-film on such substrates results in improved electrical properties. However,

such substrates are also not widely available in large sizes. Typically polycrystalline alumina is the most commonly used substrate in the microwave industry. There is need for a BST process that allows integration with other existing passive technologies on alumina. This would result in lower cost and also promote increased usage. Another challenge with BST-based devices has been achieving thick metallization to reduce conductor losses, especially in the range of 1–10 GHz. Most BST processes require a high temperature anneal to fully crystallize the BST thin-film and increase grain size. This is essential for obtaining high quality BST thin-film [27]. The thermal budget restricts the choice of metallization to noble metals which can be processed at high temperatures, typically in the range of 600–1200 °C, required for an optimized BST thin-film process. The conductivity of noble metals is usually 2–6 times lower than that of good conductors such as copper and silver. This further aggravates the lithographic and processing challenges as thicker metal films are required to meet the thickness requirement of three skin depths for reducing conductor losses to a minimum. If copper could be used, the lithographic challenge could be rendered more tractable.

In the next chapter BST thin-film varactor technology on polycrystalline alumina using copper metallization will be introduced and processing issues, substrate and metallization choice will be discussed. Techniques for microwave characterization of BST varactor will be introduced and measured results will also be presented.

Chapter 3

BST Varactor Technology

3.1 Introduction

Barium Strontium Titanate ($\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$ or BST) is an attractive candidate material for tunable microwave devices as it has a high dielectric constant of about 300–500 for thin-films, large field-dependent permittivity, and relatively low dissipation losses. The voltage dependent permittivity of BST enables the fabrication of frequency-agile components such as tunable filters [48], delay lines [57, 58], and phase shifters [21, 20]. Tunability and loss are traded off in processing and for most microwave applications practical tuning range of 2:1 can be achieved with material loss tangents of the order of 0.005. BST thin-film was described as an enabling technology for frequency-agile systems in Chapter 1. In Chapter 2 various devices reported in the literature using BST thin-film varactors are described. Methods for growth and characterization of BST thin-film were also presented.

In this chapter different capacitor configurations and the effect of metallization on Q factor will be discussed. Substrate choice and optimization of BST thin-film for maximum tuning and low-loss will also be discussed. The fabrication of interdigital varactors using $0.3\ \mu\text{m}$ MOCVD thin-film BST and also $0.6\ \mu\text{m}$ sputtered BST thin-

film will be described. Both processes used polycrystalline alumina substrate for varactor fabrication. Electrical characterization is presented up to 26 GHz. Electrode thicknesses of 0.1 μm , 0.5 μm , and 1.0 μm were considered and intrinsic Q factor of more than 100 was obtained. Intrinsic Q factor is defined as the inverse of the material loss tangent. The Q factor measured at low frequencies is the intrinsic Q factor since the dominant loss mechanism is energy dissipation in the material. At higher frequencies, the measured Q factor is the external Q and is dominated by the external series resistance of the capacitor. A new model was developed to relate the external and intrinsic Q factors and identify the sources of loss and so guide circuit development [69]. IDC varactors were also compared with MIM varactors and a parametric evaluation was also carried out. Results of capacitance variation with frequency, finger spacing and number of fingers are also reported. Frequency dispersion of capacitance is also evaluated.

3.2 Capacitor structures: parallel plate and inter-digital configurations

Microwave applications require capacitances in the sub-picofarad (< 1 pF) range and preferably with 3 μm lithography InterDigital Capacitors (IDCs). This is because MIM (metal-insulator-metal) capacitors have a very high capacitance density due to the high dielectric constant of BST thin-films. Hence, to achieve sub-picofarad capacitance, MIM capacitors require either sub-micron lithography or series connection of capacitors, both of which require expensive multi-layer photolithography. The IDC varactor lends itself to single-layer processing and higher Q values. Various parameters defining the IDC varactor are shown in Figure 3.1. A schematic of both the MIM and the IDC is shown pictorially in Figure 3.2. The MIM capacitors offer the following advantages:

- Lower tuning voltages, usually in the range of 5–30 V.

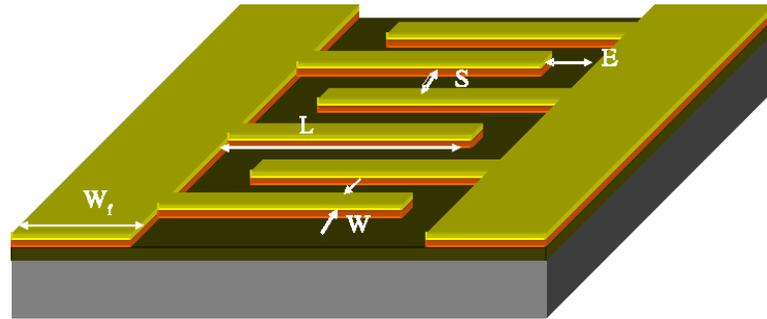


Figure 3.1: Representative 3D layout of the BST interdigital varactor, L = finger length, S = finger spacing, E = finger end gap, W = width of the fingers, and W_f = width of feed-line.

- Very high capacitance density, in the $10\text{--}40 \text{ fF}/\mu\text{m}^2$ range.

Its disadvantages are as follows:

- Lower power handling capability compared to interdigital capacitors.
- Poor linearity.
- Two or more layer lithography and micron level lithography for $< 0.2 \text{ pF}$ capacitors is required.
- Growth of thick bottom electrode required for high Q capacitors can be challenging.

Interdigital capacitors lend themselves to the design of $< 0.2 \text{ pF}$ capacitors quite naturally. Since the total capacitance is the sum of gap capacitances between the fingers, all that is required to reduce the value of the capacitors is to make the gaps larger or to reduce the length. Of course, making the gap larger entails an increase in the tuning voltage which is usually not desired so capacitance is usually adjusted by changing the finger length or the number of fingers. The following are the advantages of the interdigital capacitors:

- High power handling capability [70].
- Better linearity [71], usually 15 to 20 dB higher than MIM varactors.

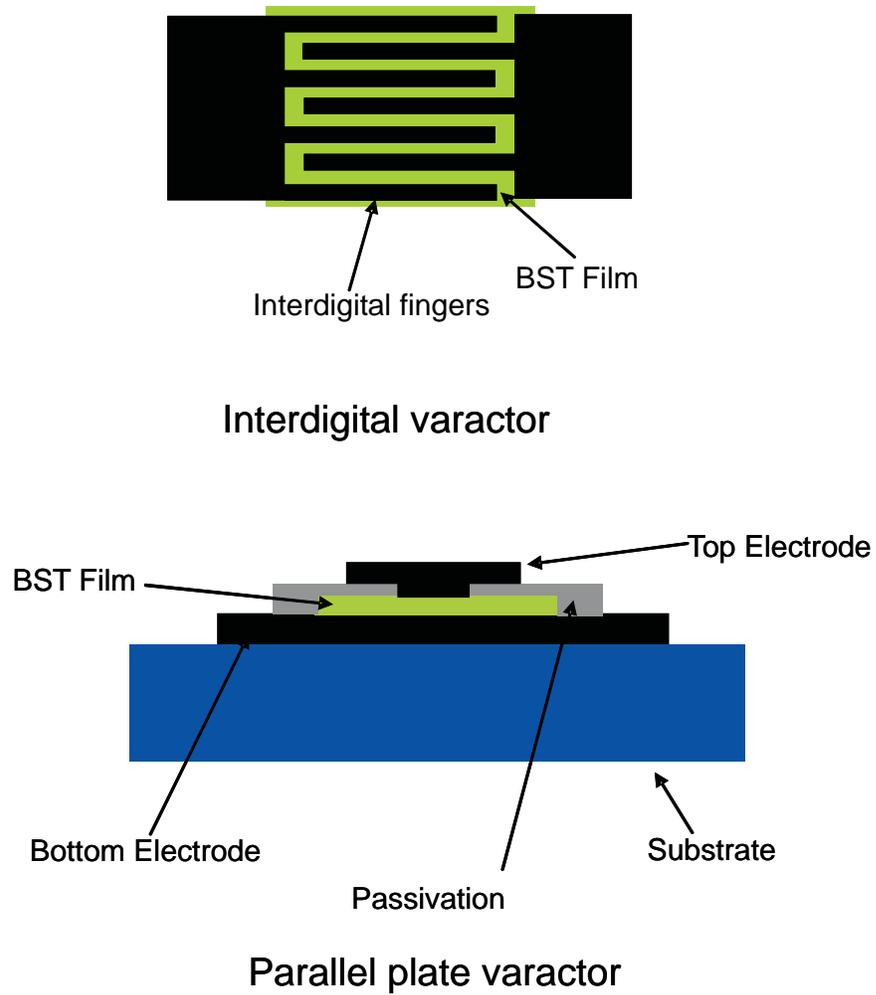


Figure 3.2: Interdigital and parallel plate BST varactors.

- Simple and inexpensive single layer lithography.
- Thickness of metal is only limited by the aspect ratio issues in processing.

The IDC varactors does have its own share of disadvantages as noted below:

- Tuning voltages are considerably higher, in the range of 75–400 V depending on the configuration and the type of BST thin-film.
- Low capacitance density compared to the MIM configuration.
- Difficult to analyze analytically, usually empirical formulae and some electromagnetic simulation is required.

The choice of MIM or IDC varactor depends on the specific application and other system requirements. Since both MIM and IDC varactors draw very little current (1–10 nA) [72] the usage is largely determined by the availability of tuning voltage and linearity requirements. In portable applications where space and cost is of utmost concern, MIM capacitors should be preferred. In fixed applications such as WLAN node or wireless base stations where availability of high voltages and space is not of great consequence and higher linearity is required, IDC is the configuration of choice.

3.3 Substrate choice and metallization

The substrates generally chosen for BST-based varactors have been sapphire [21, 20], magnesium oxide (MgO) [73], lanthanum aluminium oxide (LaAlO₃) [74], strontium titanate (SrTiO₃), and SiO₂/Silicon due to the ease with which high quality BST thin-films that can be grown epitaxially at high temperatures on such single crystalline substrates. These substrates are costly and are generally not readily available in large sizes and processing is expensive. Silicon is one possible alternative substrate but conventional low-resistivity silicon has poor microwave and millimeter wave properties and so-called high resistivity silicon substrate loses its resistivity when processed at the high temperatures (600–1200 °C) required for the fabrication

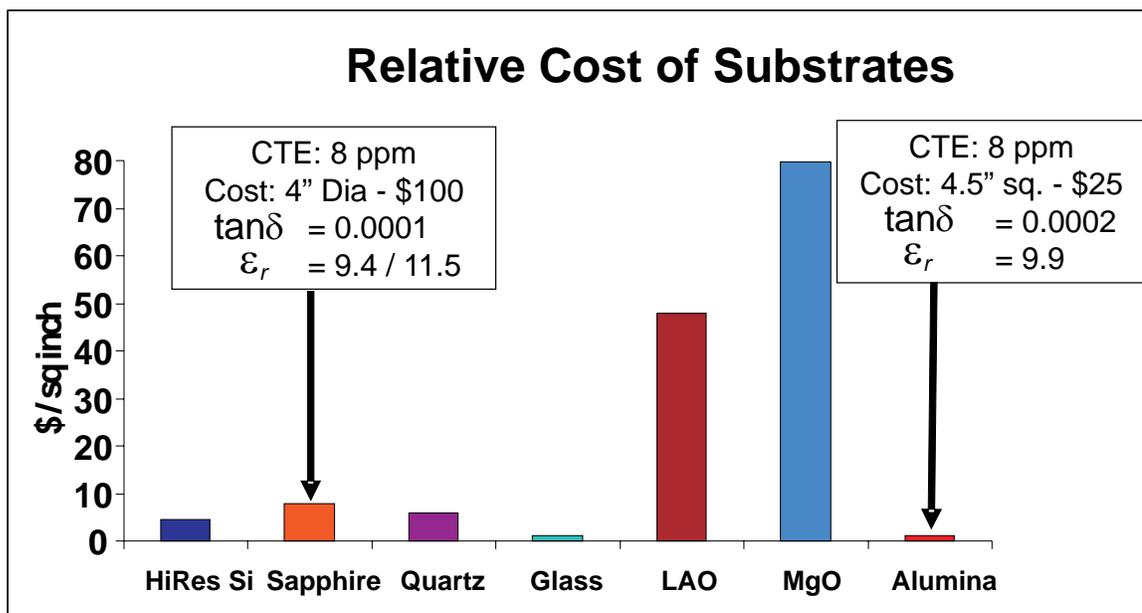


Figure 3.3: Cost comparison of different substrates, CTE: Coefficient of thermal expansion.

of high quality BST films. However, research is being carried out in adapting BST processing to develop devices requiring lower thermal budget [58]. Alumina is a well known low-cost substrate and has been used in the microwave industry for decades. It is low loss, readily available, and is compatible with most existing fabrication processes. Due to its low cost, availability from multiple vendors, and widespread use in the microwave industry a BST thin-film process was developed on polycrystalline alumina substrate. A cost comparison of alumina with other candidate substrates is shown in Figure 3.3. In particular it should be noted that both alumina and sapphire have similar properties in terms of CTE (coefficient of thermal expansion), permittivity and loss tangent. However, the per unit area cost of alumina is about one-fourth that of sapphire. Moreover, alumina is easier to machine than sapphire. It should be noted that the chemical form of both alumina and sapphire is the same, Al_2O_3 . Delpart *et al.* [75] have reported BST film of $1.8 \mu\text{m}$ thickness on alumina. Loss tangent values were in the range of 0.04–0.06, resulting in maximum Q 's of about 16.

High-quality BST capacitors on low cost polycrystalline alumina substrates using



Figure 3.4: MOCVD chamber at ATMI, Inc.

copper metallization and single step processing was developed and characterized. Both MOCVD and sputtering techniques were used. The MOCVD was used for BST thin-film deposition in co-operation with the Materials Science and Engineering (MSE) department at NC State University and ATMI Inc (see Figure 3.4). The sputtering technique was developed in-house by the MSE department at NC State University (see Figure 3.5). The quality of the BST thin-film is a function of the processing conditions such as temperature, film thickness, and thus film integrity, substrate nucleation and other processing conditions [76]. These, particularly the processing temperature, impose limits on the types and thicknesses of metals that can be used and structures that can be realized. Thus development of BST-based varactors is a trade-off of many factors.

The metal organic chemical vapor deposition (MOCVD) process at ATMI [77] was used to grow $0.3 \mu\text{m}$ $(\text{Ba}_{0.5}\text{Sr}_{0.5})\text{TiO}_3$ (known as BST-0.5) thin-films on $635 \mu\text{m}$ -thick 99.6% polished ($<2 \mu\text{in}$ surface roughness) alumina substrates (Intertec Southwest Inc., Tucson, AZ). The MOCVD process provides excellent composition

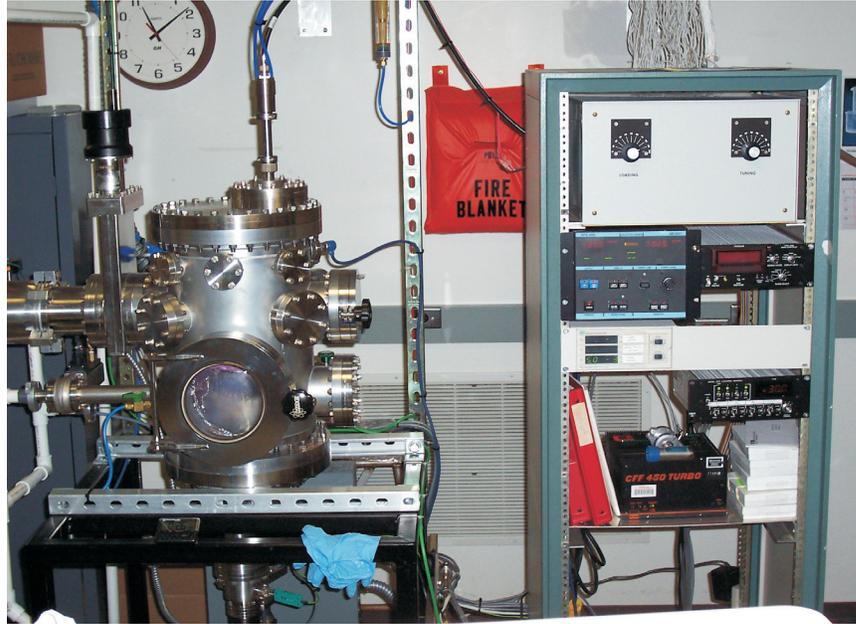


Figure 3.5: BST sputtering chamber at NC State University.

control, good area coverage and conformal coating and hence was used for fabrication of the BST thin-films. Film deposition was done at 640 °C in the MOCVD chamber. A bilayer lift-off process was used for fabrication of the IDCs. Microchem LOR 5A resist was used in conjunction with Shipley 1813 positive imaging resist to produce a thick bilayer stack. Bilayer process was chosen since it involves only benign chemicals which do not harm the BST thin-film. After a standard photolithography technique the sample was further metallized. Details of the fabrication include a thin 0.03 μm adhesion layer of chromium (Cr) deposited by magnetron sputtering at room temperature; this was followed by sputtering of copper (0.1–0.5 μm) which was chosen as the top electrode metal since it provides high conductivity and is also low cost.

A radio frequency magnetron sputtering technique was also used in the MSE department at NC State University to deposit thin-film $(\text{Ba}_{0.75}\text{Sr}_{0.25})\text{TiO}_3$ (known as BST-0.75) on polished ($<1 \mu\text{in}$ surface roughness) polycrystalline alumina substrates (from Coorstek, Golden, Colorado) [27]. The BST composition was chosen for optimum balance between dielectric tunability and loss tangent. The substrates ranged

in size from 0.5 inch square to 2 inch square and 635 μm in thickness. Sputtering was done off axis at an angle of 30° in an argon/oxygen mixture ($\text{Ar}:\text{O}_2 = 5:1$) to obtain optimal stoichiometry and uniform film thickness. However, the gun normal pointed at the center of the substrate despite the 30° incident angle. A 4 inch diameter stoichiometric ceramic BST target (Super Conductor Materials Inc., NY) was used and sputtering pressure of 10 mtorr was maintained. Deposition temperature was maintained at 300°C . Deposition was done for 60 min to obtain 0.6 μm thick BST film. After deposition the film was annealed at 900°C in air for 20 hours to obtain fully dense and crystalline BST thin-film on alumina substrate. The process was optimized for tunability and for low leakage current, see Figure 3.6. The leakage current is shown as the actual current and is not normalized per unit area as is the usual practice with leakage current data reported for MIM varactors. The leakage current at a bias field of 100 kV/cm was measured as 1.39×10^{-10} A. The calculation of area through which leakage current flows in an IDC is not as straightforward as that for a MIM varactor. However, the approximate area was calculated using the total IDC surface area as found to be 1.3×10^{-4} cm^2 . The leakage current density was calculated as 1.0×10^{-6} A/ cm^2 at a bias field of 100 kV/cm. This is comparable to the best results published in the literature for high quality BST thin-film [27]. Standard photolithography and a metal lift-off process was developed and used to define the fingers of the interdigital varactor and the feed electrodes. A lift-off process was used since it utilizes benign chemicals which do not harm the BST. This is in contrast to an etch back process where potentially harmful acids are used. Positive imaging photoresist Shipley 1813 and Microchem LOR 5A was used to deposit a thick bilayer photoresist stack for lift-off. After standard UV (ultra-violet) exposure and development of the photoresist the sample was ready for metallization.

Metallization is an important consideration for obtaining high Q BST varactors. Ideally, one would like to have the metallization with highest conductivity and maximum possible thickness allowed by the lithography process. The skin depth versus frequency for various metals is shown in Figure 3.7. In order to minimize loss, metal thickness of three skin depth is required. However, in the case of BST thin-film process metallization choice is guided by its interaction with the BST thin-film layer and

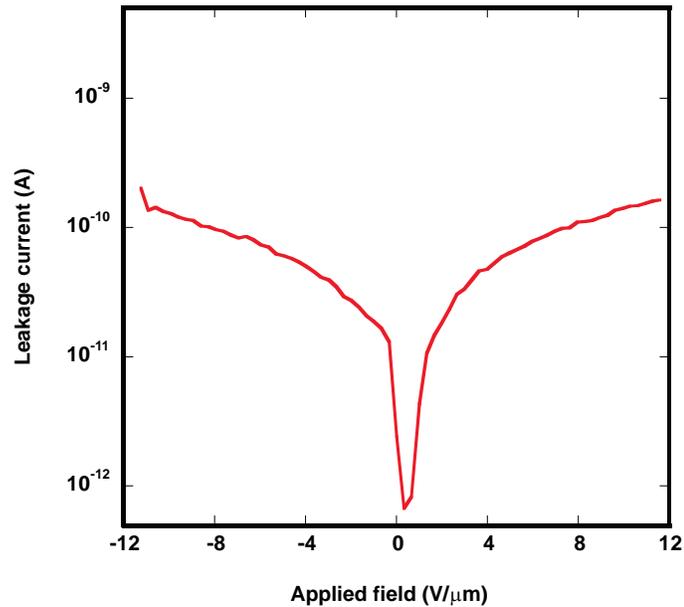


Figure 3.6: Measured leakage current data with bias. Finger length, $L = 1000 \mu\text{m}$, Width, $W = 10 \mu\text{m}$, Spacing, $S = 10 \mu\text{m}$.

other processing issues. Typically, noble metals such as Pt, Au, or Ir have been used as electrodes in thin-film oxide based devices because they are in most cases non-reactive upon contact with oxides and their large work functions provide Schottky contacts. However, due to the high resistance values of Pt and Ir, electrode thicknesses of several microns are necessary to achieve an acceptably low ESR (Equivalent Series Resistance) of the device. The use of thick electrodes involves difficult patterning issues from a manufacturing point of view. One of the issues is achieving high aspect ratio — closely spaced fingers with thick metallization. One key development in the microelectronics industry has been the use of copper in interconnects since it offers higher conductivity and improved electromigration performance. However, limited work has been reported in the area of using copper as an electrode material for thin-film oxide-based devices due to its inherently poor adhesive property and its tendency to oxidize [78]. Despite this copper was chosen as the top electrode metal in our work since it provides the highest conductivity (see Table 3.1) of any base metal. Technology was developed in the MSE department at NC State University to enable copper to be deposited on BST without the associated oxidation problems.

Table 3.1: Conductivity data for common metals [7].

Material	Conductivity (10^7 S/m) @ 20 °C
Silver	6.173
Copper	5.813
Gold	4.098
Chromium	3.846
Aluminium	3.816
Tungsten	1.825
Nickel	1.449
Platinum	0.952
Titanium	0.175

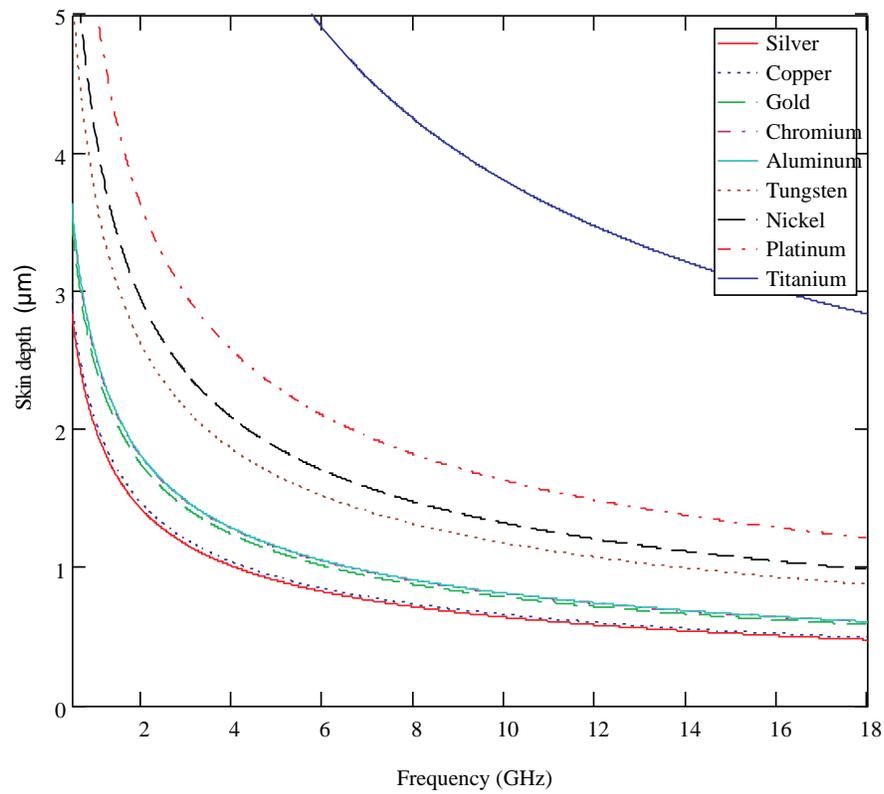


Figure 3.7: Skin depth versus frequency for various metals.

The choice of adhesion layer is an important consideration in the process flow. Usually metals with a high conductivity value have poor adhesion properties to dielectrics. So, less conductive metals or oxides of metals are used as an adhesion layer between the metal and the dielectric. Typical adhesion layers are Chromium (Cr), Titanium (Ti), Titanium-Tungsten (Ti-W), and Iridium Oxide (IrO_2). The adhesion layer should be reasonably conductive and should be able to provide sufficient adhesion with minimum thickness. The problem of adhesion was addressed by using a metallic adhesion layer. This also provided barrier to oxidation. Cr is a good choice which meets these requirements. Ti-W is also commonly used. Ti requires specially processing since both the adhesion layer and the metal must be deposited *in situ*. This is because of the tendency of Ti to form an oxide in ambient environment.

Chrome (Cr) was selected as the adhesion layer of choice for reasons mentioned above. First a thin layer of chromium ($0.03 \mu\text{m}$) was sputtered on top of the BST film and this was followed by deposition of $0.5\text{--}1.0 \mu\text{m}$ copper, either by sputtering or by thermal evaporation. Finally, lift-off was done in Microchem Remover PG solution to define the interdigital fingers. A series of IDCs were fabricated in this manner and characterized using an impedance analyzer. Finally lift-off was completed in a Microchem Remover PG solution. A representative layout of the IDC capacitor is shown in Figure 3.8.

3.4 BST varactor modeling

Microwave characterization on two sets of IDCs with different metal thicknesses was performed in a one-port configuration using a HP 8510C Vector Network Analyzer. Standard one-port Open-Short-Load (OSL) calibration was performed using a $100 \mu\text{m}$ pitch ground-signal (GS) probe and a calibration substrate from GGB Industries [79] (see Figure 3.9). Capacitor measurements were done for different number of fingers and also for varying width and spacing of the fingers. The data presented here is for the IDCs with smallest finger spacing since this results in maximum electric field in the BST and hence the largest tuning range. The dimensions of the IDCs for

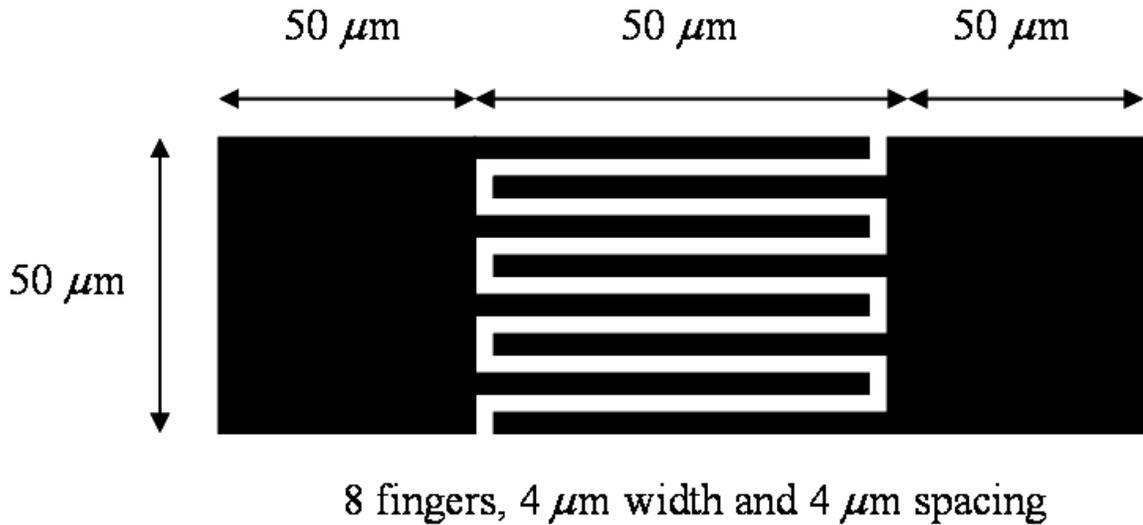


Figure 3.8: Representative layout of the BST interdigital varactor.

each of the two sets are as follows: $W = 4.0 \mu\text{m}$, $S = 4.0 \mu\text{m}$, no. of fingers, $N = 6, 8, 10$, length of fingers, $L = 50 \mu\text{m}$. The contact pad size was $50 \mu\text{m}$. Bias was applied to the IDCs using a DC Source/Monitor (HP4142B) and a high voltage bias tee from Picosecond Pulse Labs. A current-limiting resistor network was also used to prevent excess current through the bias tee and the network analyzer port in the event of a capacitor shorting out due to the application of high bias voltages. Usually this is not much of a problem since the capacitors usually become open circuited in the event of breakdown but it is essential to prevent the bias tee from excessive current if the breakdown event were to turn out to be a short circuit instead.

The reflection data was measured at different voltages up to 120 V. It was found that capacitor breakdown occurred at about 130 V due to air breakdown. High voltages could be applied if a passivation layer was used as the dielectric breakdown of the BST film was very high. At bias voltages below breakdown the DC insulation resistance was found to be of the order of $10 \text{ G}\Omega$. This was verified independently using a DC current measurement setup.

It was found that the extracted series resistance obtained was quite high for the

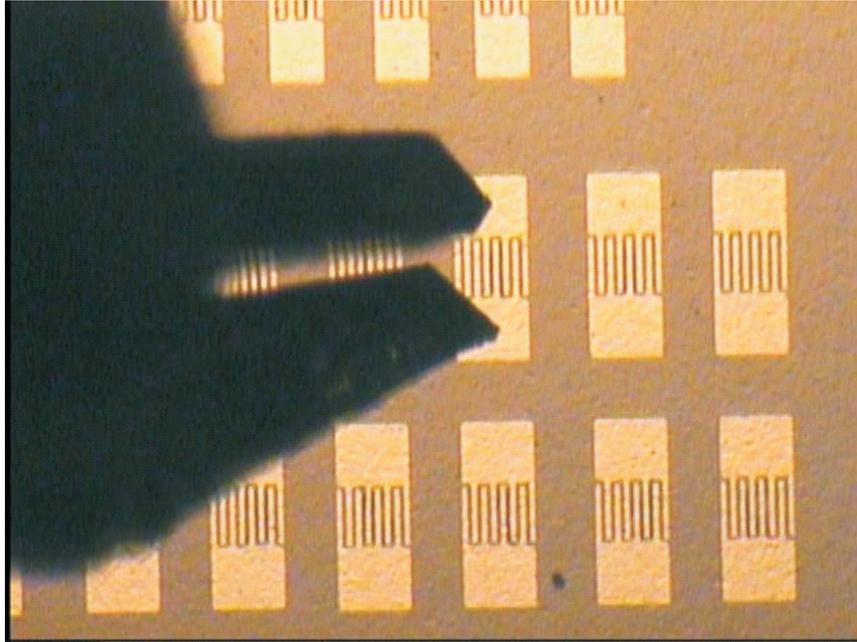


Figure 3.9: BST interdigital capacitor under test.

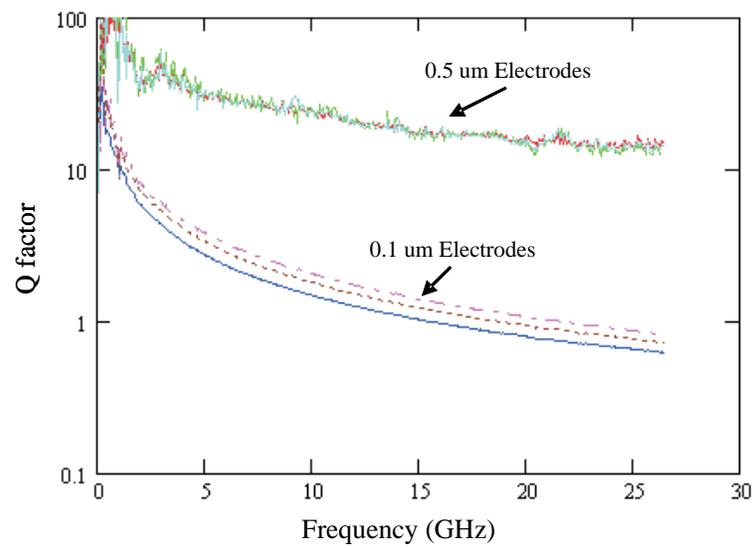


Figure 3.10: Q factor of the BST interdigital capacitor for different capacitors in the range of 0.15–0.25 pF.

capacitors with 0.1 μm of metal, in the range of 15–20 Ω , depending on the number of fingers. The values for 0.5 μm of metal were found to be in the range of 1.5–2 Ω . These values are quite different from those obtained using simple calculations based on DC resistance and the physical dimensions of the IDC contact pads. Such calculations are based on the assumption that the current distribution in the electrodes is uniform. This is a reasonable assumption up to 26 GHz for the 0.1 μm electrode and up to 10 GHz for the 0.5 μm electrode. At these frequencies the thickness is much smaller than the skin depth and hence the current distribution can be considered constant in the cross-section. To investigate this discrepancy further the quality of the sputtered copper was evaluated using a sheet resistance method using the four-point probe technique. It was found that the resistivity of the sputtered copper film was substantially higher than that of copper base metal. The resistivity was higher by a factor of as much as 50–60 times that of copper base metal. This explains why such high resistance values for series resistance were extracted. The impact of this on external Q factor for two different electrode thicknesses is shown in Figure 3.10.

In Figure 3.10 the total device Q factor was calculated using Equation (3.1).

$$Q = \frac{|Im(Z_{in})|}{|Re(Z_{in})|} \quad (3.1)$$

It can be seen that using thicker metallization can improve the Q factor by as much as an order of magnitude. In the microwave region the Q factor is primarily limited by the series conductor losses and hence it is disadvantageous to use BST-based capacitors as discrete components. In the discrete form the advantages of having a high quality BST thin-film is systematically undermined by the series resistance resulting from the contact to the capacitor. Thus the solution is to use BST varactors in an integrated fashion. As seen in Figure 3.10 the Q factor for the capacitor with 0.5 μm of metal is 17 at 26 GHz while that of the capacitor with 0.1 μm of metal is about 1 at the same frequency. It should be noted that these values are comparable to or better than that reported in the literature for similar IDC structures. These results have been obtained despite the fact that the copper deposition process is not well

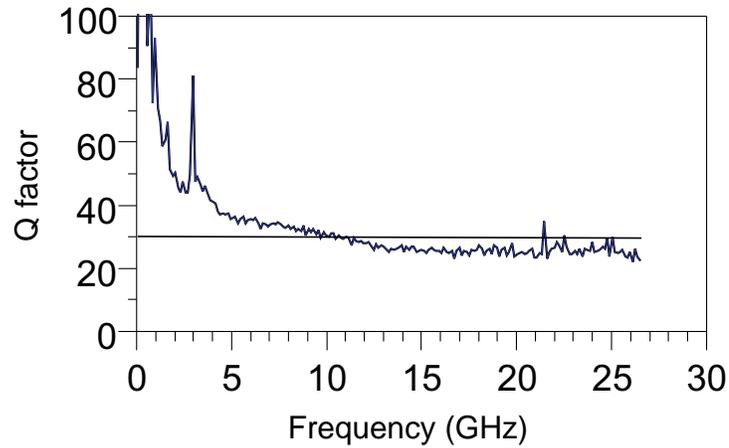


Figure 3.11: Measured Q factor for BST varactor (0.4 pF) with evaporated copper.

optimized. The low frequency Q factor data shows values in the range of 100–250. This clearly indicates that the quality of the BST thin-film is quite good and the Q factor is primarily limited by the metallic losses in the GHz range. A comparison of the sputtered copper with evaporated copper shows that for the same thickness the conductivity of evaporated copper is much higher. Measured Q factor in the range of 30 at 26 GHz for a 0.4 pF capacitor with 0.5 μm of evaporated copper is shown in Figure 3.11.

The tunability was calculated by fitting a model to the measured data across various bias voltages. Unlike the simple parallel RC model widely used in the literature it was found that a good fit was obtained only if the series resistance and the series inductance was taken into account. This is particularly true at higher frequencies when the effect of such parasitic elements is most significant.

From the reflection data the model of Figure 3.12 was extracted using fits of both external Q and reflection data. This proved to be the most reliable way of extracting the model of the device with very high intrinsic Q of the BST. In the process of fitting the parameters to the measured reflection data, it was found that the same response

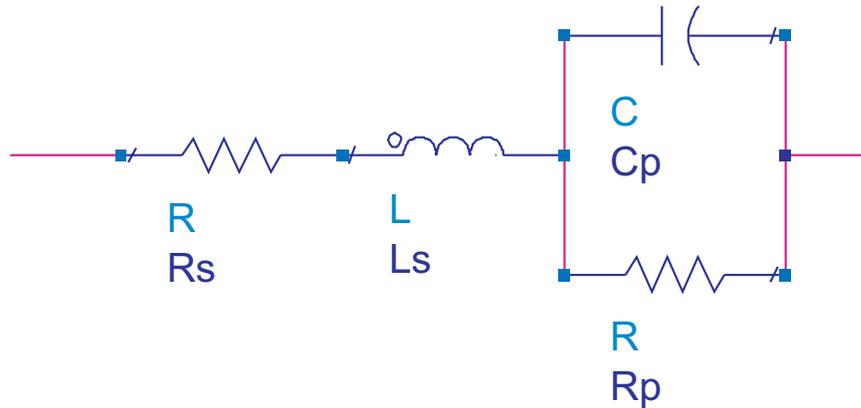


Figure 3.12: Equivalent circuit model of the BST interdigital capacitor.

could be obtained using different networks resulting in vastly different values of the extracted capacitance. This problem is due to the inherent inaccuracy of extracting loss from a reflection coefficient that is very close to unity in magnitude. This difficulty was resolved by simultaneously fitting the model to both reflection data and Q values. As shown in Figure 3.13 the agreement between measured and simulated values is quite good. The plot is shown for a capacitor with eight fingers. Though for the sake of clarity the comparison is shown only for zero-bias, the model holds equally well at all bias voltages.

Comparison of the measured and modeled Q is shown in Figure 3.14. All element values in the model were assumed to be independent of frequency. The typical peaking behavior of the Q factor with frequency is evident in the plot. The peak occurs where the contribution due to metallic losses begins to overtake the losses due to dielectric dissipation in the BST film, since the former is directly proportional to frequency while the latter is inversely related to frequency. The measurement uncertainties correspond to high intrinsic Q of the capacitors. However the frequency of the peak of the external Q is most critical in determining the intrinsic Q rather than the absolute value of the Q at the peak. From this the intrinsic Q of the BST capacitor, without the parasitic series resistance was determined to be in the range of 100 to 250.

Tunability of the IDC with electrode thickness of $0.1 \mu\text{m}$ was found to be about

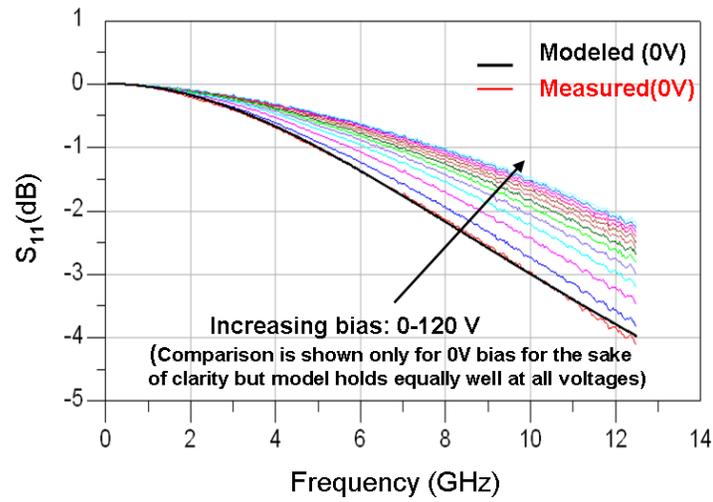


Figure 3.13: Measured reflection (S_{11}) data for BST interdigital capacitor for bias voltages up to 120 V. Comparison with model is shown only for zero bias.

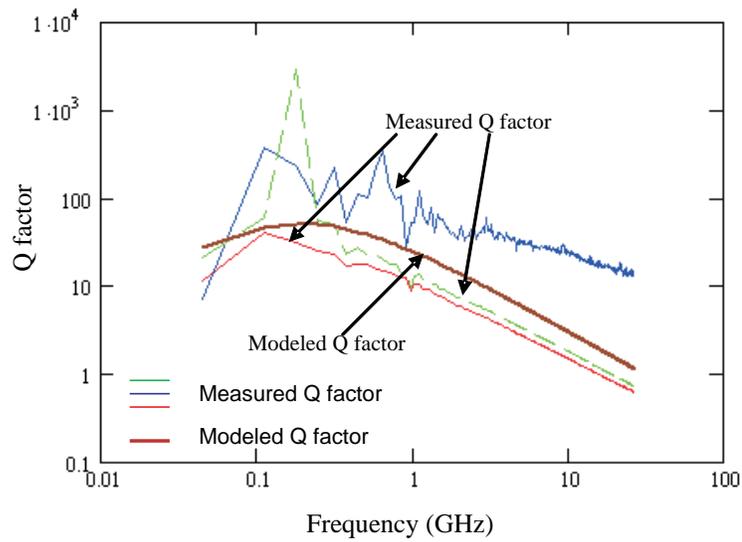


Figure 3.14: Comparison of measured and modelled Q factor.

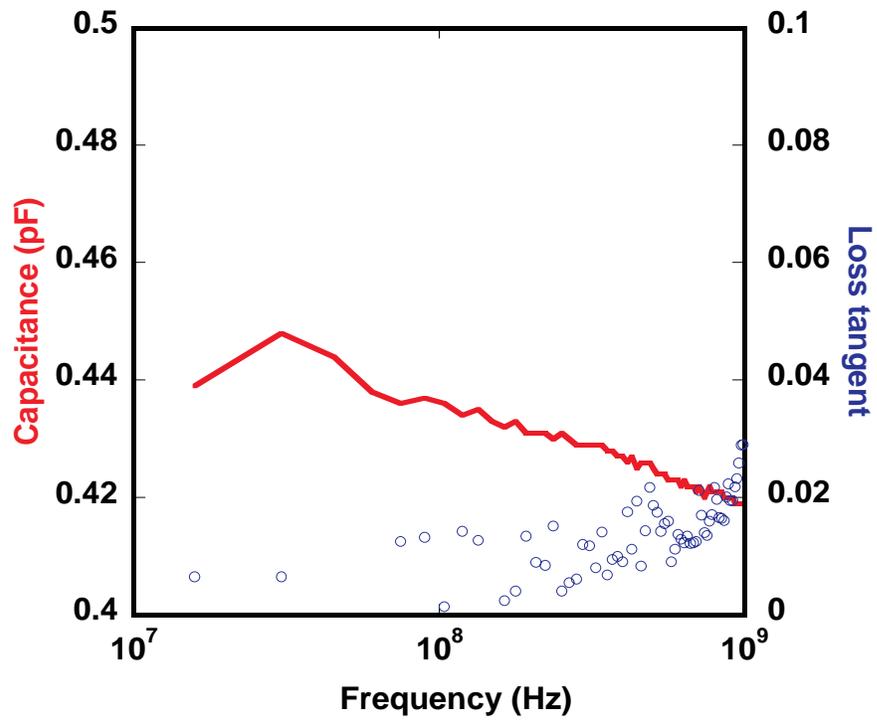


Figure 3.15: Measured frequency dependence of capacitance and loss tangent, solid line represents capacitance and open circles represent loss tangent.

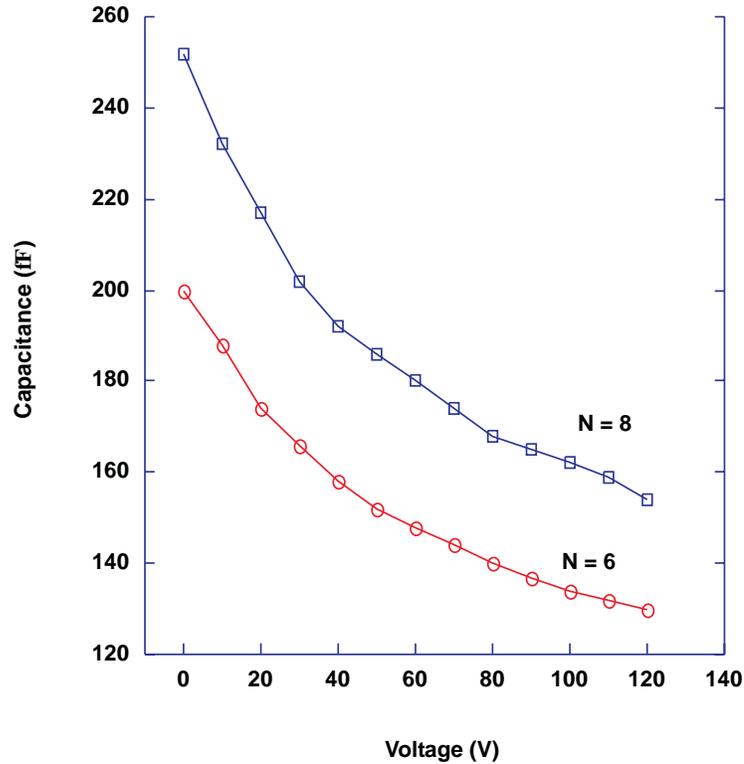


Figure 3.16: Extracted capacitance versus voltage for $N = 6, 8$.

35% at a bias voltage of 120 V, for the 6 finger capacitor the capacitance decreased from 200 fF to 130 fF. For the 8 finger IDCs the capacitance decreased from 252 fF to 154 fF for a 40% tuning or 1.64:1 tuning ratio at 120 V. It should be noted that although Q measurements at zero-bias could be performed up to a frequency of 26.5 GHz, the reflection data for different bias voltages was recorded only up to a frequency of 12 GHz. This is due to the upper frequency limit of the high voltage bias tee that was used. Capacitance versus voltage for six and eight finger IDC is plotted in Figure 3.16. Using formulae published by Gevorgian [80], permittivity versus voltage was also extracted (Figure 3.17) and shows a trend similar that of capacitance versus voltage.

The frequency dependence of capacitance was also investigated using a E4991A Agilent Impedance Analyzer (1 MHz to 3 GHz). The result is shown in Figure

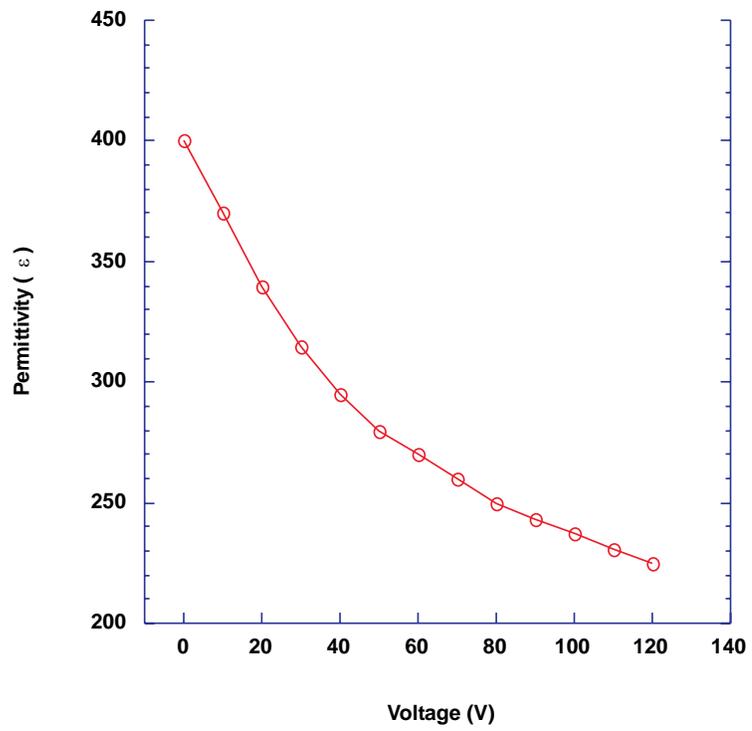


Figure 3.17: Extracted permittivity versus voltage.

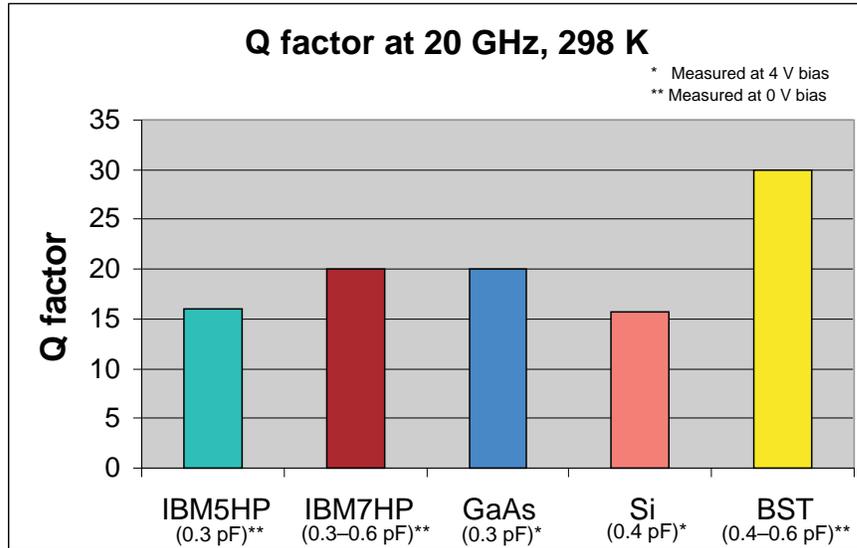


Figure 3.18: Comparison of BST IDC Q factor with commercially available semiconductor varactor.

3.15. As can be noted from the plot, there is very little frequency dispersion in the capacitance up to 1 GHz. The loss tangent data shows considerable dispersion throughout the measurement range. This is due to the fact that the instrument assumes a simple series or parallel RC model for the extraction of loss tangent and capacitance. Note that the tunability data is expected to be independent of frequency.

Comparison of Q factor of BST IDC varactor with commercially available semiconductor varactor at 20 GHz is shown in Figure 3.18. It can be seen that the BST varactor is superior to the state-of-the-art semiconductor varactors in terms of Q factor. At higher frequencies the advantage in terms of Q is more pronounced. The BST IDC varactor is also compared with data reported by other research groups, see Table 3.2. The Q factor and tunability obtained is comparable to or better than similar results on expensive single crystal substrates such as sapphire, MgO, and LAO.

Table 3.2: Comparison of BST IDC Varactor

Author	Capacitance (pF)	Q factor	Tunability	Substrate
Y.K.Yoon <i>et al.</i> , G. Tech (2003)	0.78	18.0 @ 2.5 GHz	20.5 % @ 30 V (250 kV/cm)	Sapphire
Y.K.Yoon <i>et al.</i> , G. Tech (2003)	0.52	21.5 @ 1.0 GHz	54.0 % @ 30 V (150 kV/cm)	Sapphire
R. A. York <i>et al.</i> , UCSB (2000)	7.0	20.0 @ 26.0 GHz	46.0 % @ 90 V (450 kV/cm)	Sapphire
Delpart <i>et al.</i> , (2005)	1.0	< 14.0 @ 6.0 GHz	15.0 % @ 35 V (35 kV/cm)	Alumina
S. E. Moon <i>et al.</i> , (2003)	0.4	21.0 @ 9.0 GHz	43.0 % @ 40 V (133 kV/cm)	MgO
Y. L. Cheng <i>et al.</i> , (2003)	1.5	–	26.0 % @ 40 V (200 kV/cm)	LAO
J. Nath <i>et al.</i> , (2004-2005)	0.4	28.0 @ 26.0 GHz	41.0 % @ 35 V (97.5 kV/cm)	Alumina

3.5 Comparison with MIM varactors and parametric investigation

A set of capacitors was also fabricated to investigate the dependence of capacitance on various parameters such as finger spacing and number of fingers. The results are shown in Figures 3.19 and 3.20 respectively. As expected, the capacitance scales with increasing number of fingers or reduced spacing. This trend agrees with that predicted by analytic formulae published in the literature [80]. Either method of scaling could be used to obtain the required capacitance values.

The tunability of interdigital capacitors with finger spacing (see Figure 3.21) was compared with published data for BST MIM varactors. It is interesting to note that the rate of decrease of tunability is also a function of the finger spacing. When the finger spacing was increased beyond 6 μm the tunability decreased rather slowly with further increase in finger spacing. This behavior can be explained by considering the fact that beyond a certain finger spacing most of the field lines between adjacent

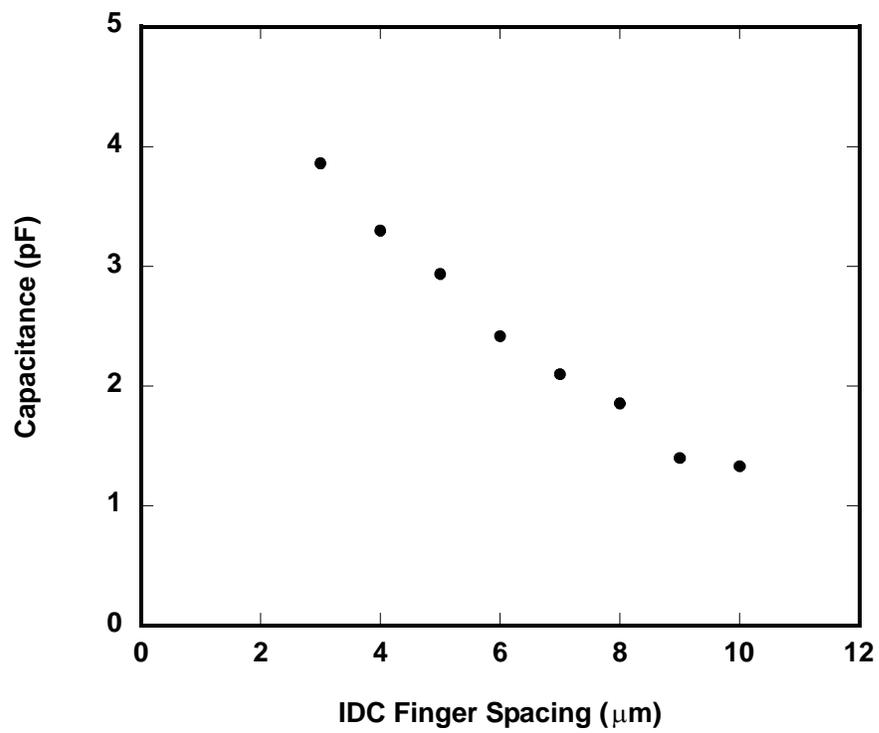


Figure 3.19: Capacitance dependence on finger spacing, data at 0 V and 1 MHz. Finger length, $L = 1000 \mu\text{m}$, Number of fingers, $N = 10$. Width is equal to spacing.

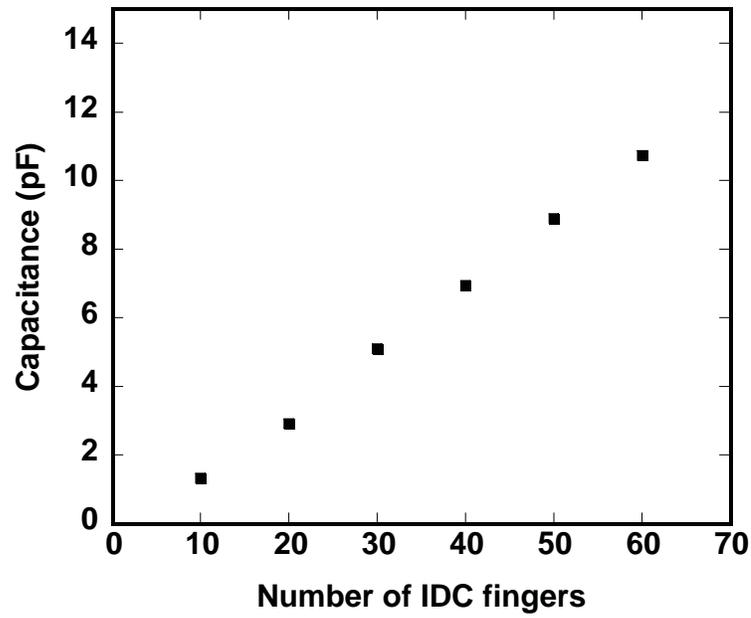


Figure 3.20: Capacitance dependence on number of fingers, data at 0 V and 1 MHz. Finger length, $L = 1000 \mu\text{m}$, Width, $W = 10 \mu\text{m}$, Spacing, $S = 10 \mu\text{m}$.

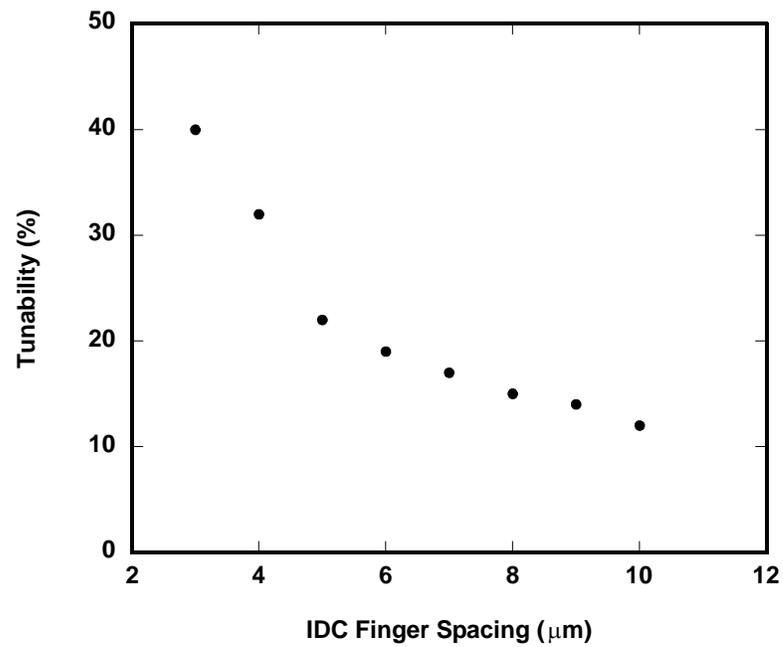


Figure 3.21: Tunability dependence on finger spacing, data at with 35 V bias and 1 MHz.

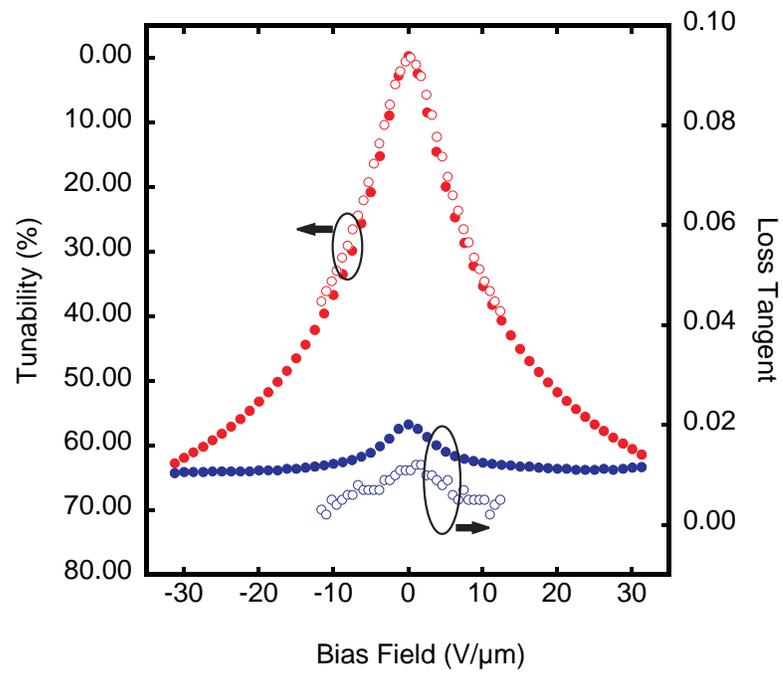


Figure 3.22: Comparison of IDC tunability with published data on MIM varactors, data at with 35 V bias and 1 MHz; open circles represent IDC data, solid circles represent MIM data

fingers are already in the air above the fingers. Increasing the finger spacing further does not reduce the tunability significantly. However, this qualitative reasoning has not been confirmed by simulation or analytic techniques. It is usually believed that an MIM capacitor is more tunable than an IDC varactor. While that is true in terms of absolute tuning voltage required, it has been demonstrated (see Figure 3.22) that on an electric field basis, an IDC on polycrystalline alumina substrate is just as tunable [113]. In fact, it has a lower loss tangent than the corresponding MIM varactor for the same tunability. The data compares MIM varactors on copper foil and IDC varactors on alumina. Both capacitor configurations were implemented using the same BST process in order to have a fair comparison.

3.6 Conclusion

In this chapter various configuration of capacitors were discussed. Each configuration has its own advantage depending on the particular application. Choice of substrates and metal electrodes for optimum BST varactor performance were also discussed. Results from the characterization of both MOCVD and sputtered BST thin-film on polycrystalline alumina were presented. Tunability of up to 1.64:1 was reported with Q factor up to 30 at 26 GHz for a $0.5 \mu\text{m}$ evaporated copper metallization. This is comparable to results reported in the literature by other groups but on expensive single crystalline substrates. It is expected that with thicker electrodes the external Q factor would be significantly higher. The effect on Q factor was quite dramatic with change in electrode thickness. It should be possible to obtain higher tunability by using smaller finger spacing to increase the applied electric field and also by using a passivation layer over the electrodes for applying higher voltages.

BST technology on alumina with copper metallization was demonstrated to be a very viable technology for frequency-agile systems. In the next chapter design techniques for optimized design of tunable resonator for high tuning range without any significant compromise in Q factor values will be introduced. The concept of network transformation factor (τ_{NTF}) and a new figure-of-merit (K_τ) will also be

described. Also, a novel characterization technique for the extraction of intrinsic loss in symmetrical two-port networks will be introduced and verified.

Chapter 4

Design of Tunable Resonators

4.1 Introduction

This chapter introduces the optimized design of distributed tunable resonators. In frequency-agile systems the goal is to achieve the maximum frequency agility for a given tuning ratio of the element or device that is being used for tuning. This must be accomplished without sacrificing the Q factor of the devices. The theory is presented and results demonstrate an optimized tunable resonator design. The concept of network transformation factor (τ_{NTF}) is introduced to quantify the tunability of different networks using the same tuning element. Tuning frequency and Q factor data will be presented. Furthermore, a figure-of-merit (K_τ) is defined for a tunable resonator in terms of the Q factor and the network transformation factor. This enables the design trade-off between tunability and Q factor to be made in accordance with the system requirements. This technique will be contrasted with figure-of-merit, or Commutation Quality Factor (CQF) introduced by Vendik *et al.* [81, 82]. An intrinsic loss extraction technique is introduced for symmetrical two port networks. This enables the physical loss in the device to be determined so as to guide technology development.

4.2 Optimized resonator design

4.2.1 Introduction

The goal of any frequency-agile system is to operate with maximum selectivity and tunability while simultaneously achieving minimum insertion loss. Selectivity is the property of a communication system that allows it to select the desired channel while rejecting other channels. The higher the selectivity the better the system performance. Tunability allows the system to cover multiple frequency bands. Insertion loss is the attenuation that a signal suffers while passing through frequency selective devices in a communication system. The insertion loss for a filter, phase shifter, matching network and other components are largely determined by the Quality factor or the Q factor of the elements comprising the resonator. Q is a measure of the effectiveness of the resonator to store energy in a network with minimum loss. The higher the Q factor the lower the losses in the resonator. In the limit of no loss, a resonator approaches an ideal system of energy oscillation that sustains itself without any external driving force once an impulse is initially applied to the system. The Q factor is defined as the ratio of the average energy stored to energy dissipated per cycle, see Equation (4.1).

$$Q = \omega \left(\frac{\text{Average energy stored}}{\text{Energy dissipated per second}} \right) \quad (4.1)$$

The smaller the energy dissipation the larger the Q factor. It should be noted that it is the relative amount of energy dissipated that determines the Q factor. Therefore, if either the volume fraction in which the energy is stored is increased or the volume fraction in which energy is dissipated is decreased, the Q factor will increase. The Q factor for series RLC and parallel RLC resonance is given by Equations (4.2) and (4.3) respectively.

$$Q_{\text{series}} = \frac{\omega L}{R} = \frac{1}{\omega RC} \quad (4.2)$$

$$Q_{\text{parallel}} = \frac{R}{\omega L} = \omega RC \quad (4.3)$$

It is seen from the above equations that in a lumped element resonant system the Q factor is largely determined by the equivalent series resistance in the series case and by the equivalent parallel resistance in the parallel case. In most practical implementation the resistance is determined by the inductor. Typical implementation of inductors include a coil wound SMT inductor or an on-chip inductor. In either case Q factors of 20–50 in the range of 1–5 GHz is typical [83]. Capacitors on the other hand have a slightly better Q factor in the range of 60–100 in the same frequency range. The overall Q factor is therefore dominated by the inductor. There have been various attempts to increase the Q factor of inductors, especially those on-chip. Among a variety of techniques, micromachined inductors and meshed ground plane techniques to reduce eddy current losses have been explored by various researchers to reduce the loss. However, despite the advancements, the Q factor remains < 100 for all implementations. Integrated inductors are used for on-chip circuits despite their limitations due to ease of integration with other circuitry and small size. However, for applications where high selectivity and low insertion loss is desired one must turn to distributed resonators for realizing higher Q factor. Moreover as the frequency of operation increases the length of a resonator required for resonance also decreases, making them a more attractive method of realizing higher Q .

A distributed resonator is typically realized [7] by a quarter-wave or half-wave transmission line terminated in either an open-circuit or a short-circuit. Implementations include microstrip, stripline, suspended stripline, waveguide, co-axial line, inverted microstrip and other transmission line topologies. The energy in a distributed resonator is stored in the distributed bulk of the material and the volume is much larger than in the case of a lumped element implementation. Q factor values range from 150 for a microstrip implementation to over 1000 for co-axial and suspended stripline implementations. Frequency agility can be obtained by loading the transmission line resonators with a tunable reactive element such as a varactor. The high

Q factor of transmission line resonators offers the possibility of achieving an overall Q factor for the resonator and varactor combination which is higher than that of the varactor alone. This can be expected since a large part of the energy is stored in the bulk of the resonator and the volume fraction occupied by the capacitor is comparatively smaller. Overall, this has the effect of raising the Q factor above that of the individual varactor alone. This concept can be used to great advantage in the design of a tunable resonator, as will be shown in later sections. A distributed resonator forms the basis of many frequency selective elements including filters and so this work leads to the design of minimum loss tunable distributed filters. It also allows the trade-off between tunability and Q factor for a given specification. The total Q factor in any resonant system is given by the parallel combination of the conductor, dielectric and radiation Q factors, see Equation (4.4). For most systems, except for those at very high frequencies, the radiation Q factor is much larger than the conductor and dielectric Q factors and the overall Q is limited by those two sources, see Equation (4.5).

$$\frac{1}{Q_{\text{total}}} = \frac{1}{Q_{\text{cond}}} + \frac{1}{Q_{\text{diel}}} + \frac{1}{Q_{\text{rad}}} \quad (4.4)$$

$$\frac{1}{Q_{\text{total}}} \cong \frac{1}{Q_{\text{cond}}} + \frac{1}{Q_{\text{diel}}} \quad (4.5)$$

The dielectric and conductor Q factor can be found by calculating the energy stored and energy dissipated in a given volume. For a system consisting of separate regions with different dielectric and conductor properties, the total Q factor can be calculated from the sum of partial Q factors in each region using Equation (4.6). From a knowledge of the electric field and magnetic fields, the conductor and dielectric Q factors in each subregion, i , can be readily calculated using Equations (4.7) and (4.8) respectively.

$$Q = \frac{1}{\sum_{i=1}^N \frac{1}{Q_{\text{diel}(i)}} + \sum_{i=1}^N \frac{1}{Q_{\text{cond}(i)}}} \quad (4.6)$$

$$Q_{\text{diel}(i)} = \frac{\omega \left(\frac{\varepsilon_i}{2} \iiint_{v_i} |E_i|^2 dv \right)}{\frac{\omega \varepsilon_i \tan \delta_i}{2} \iiint_{v_i} |E_i|^2 dv} \quad (4.7)$$

$$Q_{\text{cond}(i)} = \frac{\omega \left(\frac{\varepsilon_i}{2} \iiint_{v_i} |E_i|^2 dv \right)}{\frac{R_{s(i)}}{2} \iint_{S_i} |H_{t(i)}|^2 ds} \quad (4.8)$$

For the case of a resonator consisting of two regions ($i = 2$), Equation (4.6) can be simplified and expanded to yield the total dielectric Q factor, see Equation (4.9). Similarly the total conductor Q factor and hence the total Q factor of the system can be calculated using Equations (4.10) and (4.11) respectively.

$$Q_{\text{diel}(i=2)} = \frac{\omega \left[\left(\frac{\varepsilon_1}{2} \iiint_{v_1} |E_1|^2 dv \right) + \left(\frac{\varepsilon_2}{2} \iiint_{v_2} |E_2|^2 dv \right) \right]}{\frac{\omega \varepsilon_1 \tan \delta_1}{2} \iiint_{v_1} |E_1|^2 dv + \frac{\omega \varepsilon_2 \tan \delta_2}{2} \iiint_{v_2} |E_2|^2 dv} \quad (4.9)$$

$$Q_{\text{cond}(i=2)} = \frac{\omega \left[\left(\frac{\varepsilon_1}{2} \iiint_{v_1} |E_1|^2 dv \right) + \left(\frac{\varepsilon_2}{2} \iiint_{v_2} |E_2|^2 dv \right) \right]}{\frac{R_{s(1)}}{2} \iint_{S_1} |H_{t(1)}|^2 ds + \frac{R_{s(2)}}{2} \iint_{S_2} |H_{t(2)}|^2 ds} \quad (4.10)$$

$$Q_{\text{total}(i=2)} = \left(\frac{1}{Q_{\text{diel}(i=2)}} + \frac{1}{Q_{\text{cond}(i=2)}} \right)^{-1} \quad (4.11)$$

The motivation for the investigation into the design of optimal resonators was to achieve the maximum tunability for a given change in capacitance without significantly reducing the Q factor. The above equations clearly demonstrate that if the volume fraction occupied by the lossy tuning element is minimized with respect to the bulk of the resonator where the large part of the energy is stored, the overall Q factor could possibly be raised above that of the individual tuning element while simultaneously achieving improved frequency tuning. This is essential for BST thin-film varactor since it usually has a limited tuning range (2:1) and a material quality factor (inverse of material loss tangent) of 100–150. There is also a trade-off between loss and tunability in the material itself. This follows directly from the Kramers-Kronig

relationship between the real and imaginary part of the complex permittivity. In general, the higher the tunability, the higher the loss tangent and vice-versa. The goal, therefore, was to develop a technique for attaining maximum tuning of a resonator using distributed elements. In the following section the network transformation factor is introduced and a figure-of-merit is defined which enables evaluation of resonators with different Q factors and tunability.

4.2.2 Network transformation factor and tunability

The effect of the network in which a tuning element is embedded and how it transforms the tunability of the element into the resultant tunability of the overall network will now be discussed. For a first order system consisting of a lumped element inductor and a capacitor forming a parallel resonant network (see Figure 4.1), the change of resonant frequency is directly related to the square root of the capacitance ratio. This network yields the maximum frequency tuning that can be achieved. For a 2:1 tuning ratio, a $\sqrt{2}$:1 tuning ratio of resonant frequency is obtained and so on. In this configuration the Q factor of the parallel resonant circuit is limited by the Q factor of the individual elements. In most practical cases, this means that the Q will be inductor limited, as discussed in the previous section.

Many practical circuits such as filters, phase-shifters, matching networks, etc, are therefore built using high Q resonant elements such as short-circuited or open-circuited transmission lines. In order to achieve frequency agility, transmission line resonant elements are loaded/embedded with one or more tuning elements such as a variable capacitor. Though the Q factor of the transmission line and varactor combination is usually higher than that of the varactor alone, the frequency tuning ratio is generally lower than that of the maximum that can be achieved using a lumped element parallel resonator. The exact trade-off between the overall Q and the frequency tuning ratio is dependent on the network itself and several common network topologies were investigated to evaluate the network transformation factor. Four different networks have been evaluated and they will be referred to as Type A, Type B, Type C, and Type D. These networks were selected because they represent

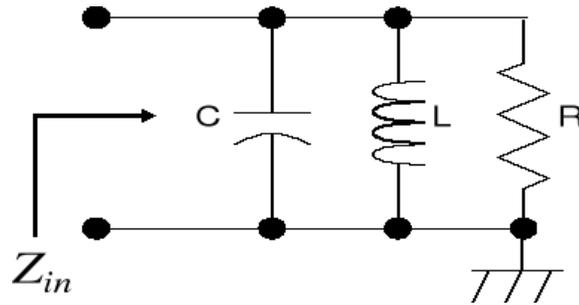


Figure 4.1: Parallel lumped element resonator

the most common topologies used in the design of frequency-agile networks. Each of these represent a unique case of energy distribution and placement of the tuning element such that an optimum trade-off between tunability and Q factor is obtained. Each of these networks also have subnetwork topologies where a reduction in line length might lead to increased tuning. For instance the transmission line length for the Type A network can be made vanishingly small and the tunability would then approach that of parallel lumped element resonators. However, the Q factor would then be limited by that of the capacitor or the inductor, whichever is lower.

We focus on four different network types as described below:

- Type A – Capacitor in parallel with shorted transmission line (Figure 4.2(a))
- Type B – Capacitor in parallel with open-circuited transmission line (Figure 4.2(b))
- Type C – Capacitor in parallel with transmission line with series capacitor loading at the end (Figure 4.2(c))
- Type D – Capacitor in series with the transmission line at the shorted end (Figure 4.2(d))

The frequency tuning ratio, i.e, ratio of the change in resonant frequency from one state to another, obtained for different capacitance ratio was investigated for each of these topologies. The aim was to achieve parallel resonance, i.e input impedance of

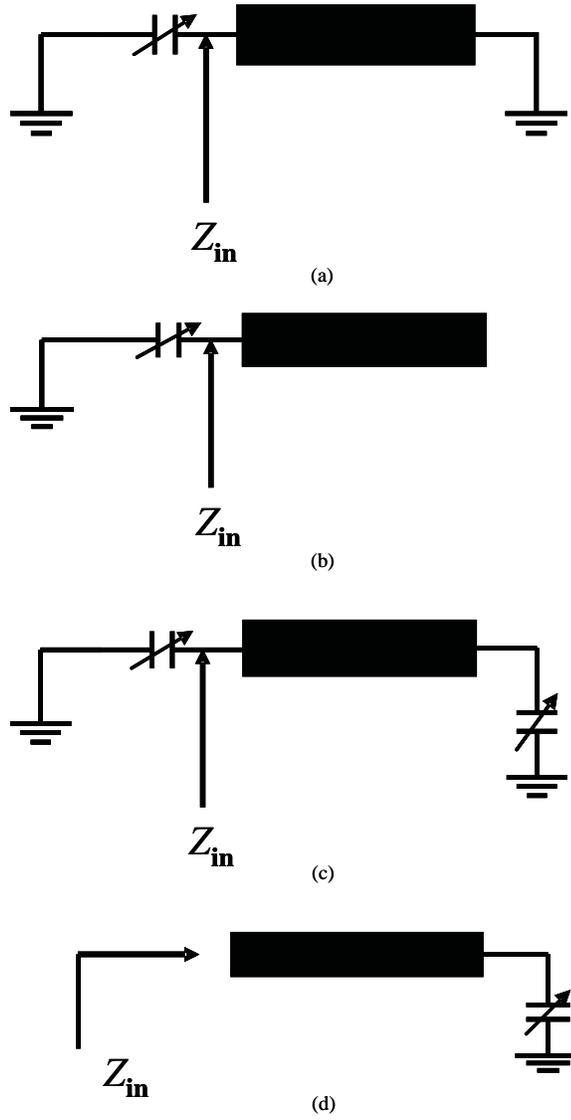


Figure 4.2: Various tunable network topologies, (a) Type A; (b) Type B; (c) Type C; (d) Type D.

Table 4.1: Tuning Characteristics (Type A)

Capacitance Tuning Ratio(η)	Frequency(f_1) State 1 (MHz)	Frequency (f_2) State 2 (MHz)	Frequency Tuning Ratio (f_2/f_1)
1.0 : 1	1194	–	1.0
1.5 : 1	1194	1358	1.137
2.0 : 1	1194	1466	1.228
4.0 : 1	1194	1684	1.410
8.0 : 1	1194	1831	1.534

very high value (open-circuit point on the Smith Chart). For the sake of comparison, a parallel lumped element resonator (see Figure 4.1) is also investigated under similar tuning conditions. All simulations were carried out in the microwave circuit simulator from Agilent, Advanced Design Systems (ADS). The resonator frequency in each case was determined by evaluating the zero crossing of the phase versus frequency curve. Q factor was determined using the 3-dB method and employing high impedance (500 k Ω) ports in the simulation setup which is mathematically equivalent to a weakly coupled two-port resonator. Q factor was then determined as the ratio of the center frequency to the 3-dB bandwidth of the resonator. The error in the extraction of Q factor was $< \pm 3\%$. Capacitor Q factor of 20 and 40 was considered. In both cases the transmission line Q was > 200 . For the lumped element case, the inductor Q factor was assumed to be equal to the capacitor Q factor, i.e. equal to 20 and 40 respectively. The results are shown in Table 4.1 and 4.2, Table 4.3 and 4.4, Table 4.5 and 4.6, Table 4.7 and 4.8, and Table 4.9 and 4.10 for Type A, Type B, Type C, Type D networks, and the parallel lumped element resonator respectively. It can be clearly seen that different network topologies have a different frequency tuning range for the same capacitance tuning ratio. A comparative summary of tuning ratio for various network topologies is shown in Table 4.11.

The Type C network with two tunable capacitors at either end of the resonator has the most tuning range. A comparative plot of the frequency tuning range for different network topologies, including the lumped element resonator, for a range of capacitance tuning ratios is shown in Figure 4.3.

Table 4.2: Figure-of-Merit (FOM) (Type A)

Capacitance Tuning Ratio(η)	Q Factor (Capacitor $Q = 20$)	Q Factor (Capacitor $Q = 40$)	Figure of Merit ($K_{\tau 20}$)	Figure of Merit ($K_{\tau 40}$)
1.0 : 1	25.96	49.75	0	0
1.5 : 1	29.52	50.23	4.044	6.881
2.0 : 1	34.90	61.04	7.957	13.917
4.0 : 1	49.53	84.20	20.307	34.522
8.0 : 1	73.24	114.44	39.110	61.110

Table 4.3: Tuning Characteristics (Type B)

Capacitance Tuning Ratio(η)	Frequency(f_1) State 1 (MHz)	Frequency (f_2) State 2 (MHz)	Frequency Tuning Ratio (f_2/f_1)
1.0 : 1	1194	–	1.0
1.5 : 1	1194	1268	1.062
2.0 : 1	1194	1313	1.100
4.0 : 1	1194	1397	1.170
8.0 : 1	1194	1445	1.210

Table 4.4: Figure-of-Merit (FOM) (Type B)

Capacitance Tuning Ratio(η)	Q Factor (Capacitor $Q = 20$)	Q Factor (Capacitor $Q = 40$)	Figure of Merit ($K_{\tau 20}$)	Figure of Merit ($K_{\tau 40}$)
1.0 : 1	49.75	85.28	0	0
1.5 : 1	55.13	90.57	3.418	5.615
2.0 : 1	62.52	101.00	6.252	10.100
4.0 : 1	87.31	126.90	14.843	21.573
8.0 : 1	120.42	144.50	25.288	30.345

Table 4.5: Tuning Characteristics (Type C)

Capacitance Tuning Ratio(η)	Frequency(f_1) State 1 (MHz)	Frequency (f_2) State 2 (MHz)	Frequency Tuning Ratio (f_2/f_1)
1.0 : 1	1836	–	1.0
1.5 : 1	1836	2153	1.172
2.0 : 1	1836	2381	1.296
4.0 : 1	1836	2915	1.589
8.0 : 1	1836	3346	1.822

Table 4.6: Figure-of-Merit (FOM) (Type C)

Capacitance Tuning Ratio(η)	Q Factor (Capacitor $Q = 20$)	Q Factor (Capacitor $Q = 40$)	Figure of Merit ($K_{\tau 20}$)	Figure of Merit ($K_{\tau 40}$)
1.0 : 1	23.54	44.78	0	0
1.5 : 1	25.63	47.84	4.408	8.228
2.0 : 1	27.68	51.76	8.193	15.320
4.0 : 1	36.44	64.77	21.463	38.149
8.0 : 1	53.11	90.43	43.656	74.333

Table 4.7: Tuning Characteristics (Type D)

Capacitance Tuning Ratio(η)	Frequency(f_1) State 1 (MHz)	Frequency (f_2) State 2 (MHz)	Frequency Tuning Ratio (f_2/f_1)
1.0 : 1	2689	–	1.0
1.5 : 1	2689	2889	1.074
2.0 : 1	2689	3036	1.129
4.0 : 1	2689	3379	1.256
8.0 : 1	2689	3640	1.354

Table 4.8: Figure-of-Merit (FOM) (Type D)

Capacitance Tuning Ratio(η)	Q Factor (Capacitor $Q = 20$)	Q Factor (Capacitor $Q = 40$)	Figure of Merit ($K_{\tau 20}$)	Figure of Merit ($K_{\tau 40}$)
1.0 : 1	48.89	84.03	0	0
1.5 : 1	48.15	82.54	3.563	6.107
2.0 : 1	48.19	84.33	6.216	10.878
4.0 : 1	59.28	96.57	15.175	24.722
8.0 : 1	82.73	121.33	29.28	42.950

Table 4.9: Tuning Characteristics (Lumped Element Resonator)

Capacitance Tuning Ratio(η)	Frequency(f_1) State 1 (MHz)	Frequency (f_2) State 2 (MHz)	Frequency Tuning Ratio (f_2/f_1)
1.0 : 1	1194	–	1.0
1.5 : 1	1194	1464	1.225
2.0 : 1	1194	1688	1.414
4.0 : 1	1194	2388	2.000
8.0 : 1	1194	3376	2.828

Table 4.10: Figure-of-Merit (FOM) (Lumped Element Resonator)

Capacitance Tuning Ratio(η)	Q Factor (Capacitor, Inductor $Q = 20$)	Q Factor (Capacitor, Inductor $Q = 40$)	Figure of Merit ($K_{\tau 20}$)	Figure of Merit ($K_{\tau 40}$)
1.0 : 1	10.0	20.0	0	0
1.5 : 1	10.0	20.0	2.25	4.5
2.0 : 1	10.0	20.0	4.14	8.28
4.0 : 1	10.0	20.0	10.0	20.0
8.0 : 1	10.0	20.0	18.28	36.56

Table 4.11: Comparison of frequency tuning ratio for various network topologies for different capacitance tuning ratios

Capacitance Tuning Ratio(η)	Type A (f_2/f_1)	Type B (f_2/f_1)	Type C (f_2/f_1)	Type D (f_2/f_1)	Lumped Element Resonator (f_2/f_1)
1.5 : 1	1.137	1.062	1.172	1.074	1.225
2.0 : 1	1.228	1.100	1.296	1.129	1.414
4.0 : 1	1.410	1.170	1.589	1.256	2.000
8.0 : 1	1.534	1.210	1.822	1.354	2.828

It is worth noting that in each case the maximum tuning of the resonator for a given capacitance ratio is less than that obtained from the parallel LC resonant circuit. Also, the higher the tuning the lower the Q factor of the capacitor and transmission line combination for a given Q factor of the capacitor. This is due to the network transformation factor for different topologies. The network transformation factor (τ_{NTF}) is defined as the ratio of the frequency tuning ratio of the resonator to the maximum tuning ratio obtained from a parallel LC resonator for a given capacitance ratio. Some definitions are given below:

- η = capacitance tuning ratio
- τ_{NTF} = network transformation factor
- f_1 = resonant frequency in state 1
- f_2 = resonant frequency in state 2
- $F_r = f_2/f_1$ = resonator frequency tuning ratio
- $F_m = \sqrt{\eta}$ = maximum frequency tuning ratio

$$\tau_{\text{NTF}} = \frac{F_r}{F_m} = \frac{F_r}{\sqrt{\eta}} \quad (4.12)$$

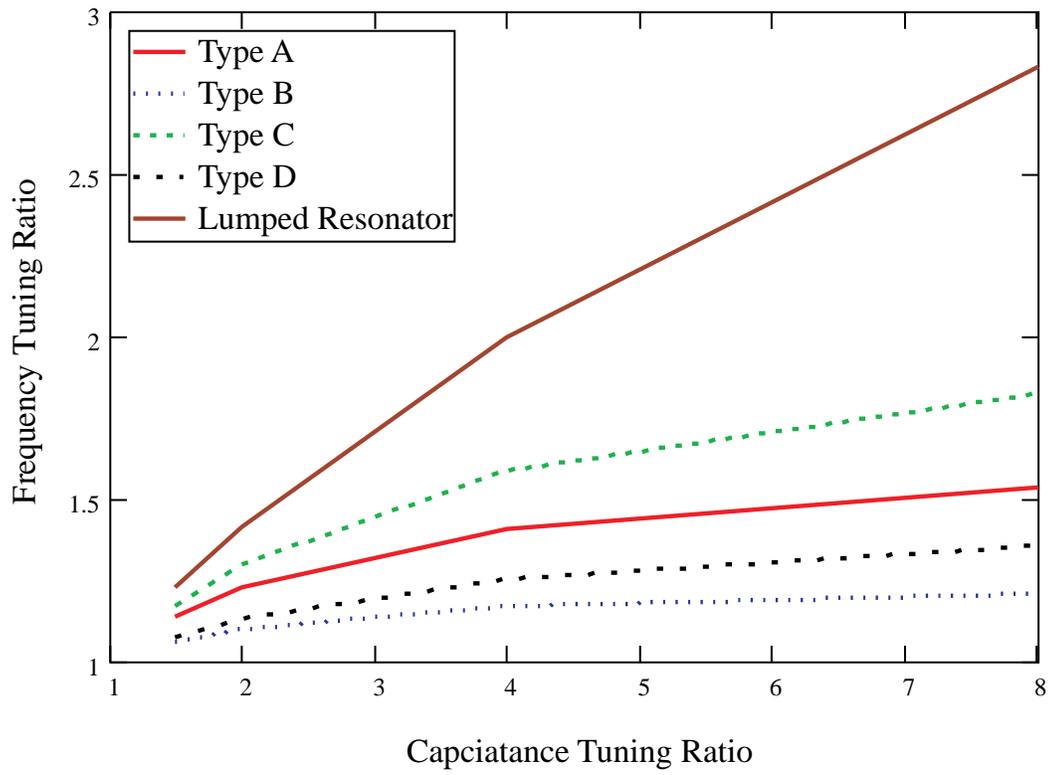


Figure 4.3: Frequency tuning ratio for various network topologies and capacitance ratios.

The largest value of τ_{NTF} is 1 and the higher the value the more tunable the particular network topology is. The parallel LC network has a value of $\tau = 1$. The smallest value of τ_{NTF} is $1/\sqrt{\eta}$. However, the higher the τ_{NTF} , the lower the overall Q factor. Thus, the network transformation factor is a measure of the suitability of a given topology for frequency-agile devices. Depending on the system tuning and loss requirements, trade-offs can be made based on the network transformation factor.

A figure-of-merit, K_τ , will be defined in terms of the Q factor and the network transformation factor. The definition is given below:

$$K_\tau = Q(\sqrt{\eta}\tau - 1) \quad (4.13)$$

For a given capacitance ratio η it is obvious that a higher τ_{NTF} is desired for achieving a higher K_τ . Now, τ_{NTF} is a measure of tunability that can be achieved for a given network topology. The figure-of-merit, K_τ , therefore, is a measure of the trade-off between tunability and Q factor. The higher the number, the better the design.

A comparison of the various network topologies with the lumped element resonator in terms of FOM (K_τ) is shown in Figures 4.4 and 4.5 for a capacitor Q factor of 20 and 40 respectively. In both cases the transmission line Q factor was > 200 . For the lumped element case, the inductor Q factor was assumed to be equal to the capacitor Q factor, i.e. equal to 20 and 40 respectively for Figures 4.4 and 4.5. Type C network represents the best compromise between tunability and Q factor since it has the highest FOM for the two values of the Q factor of the varactor considered here. It is worth noting that FOM of the lumped element resonator is the lowest among all cases considered here. Even though the parallel lumped element resonator represents the best choice of network topology in terms of tuning characteristics (see Figure 4.3), it does not represent an optimal design in terms of the trade-off between tunability and loss. The Q factor of the parallel lumped element resonator is always less than half of the individual Q factor of the capacitor and inductor, i.e., less than 10 and 20 respectively for the two cases considered here. On the other hand, distributed network topologies offer an increase in the overall Q factor at the price of reduced tunability.

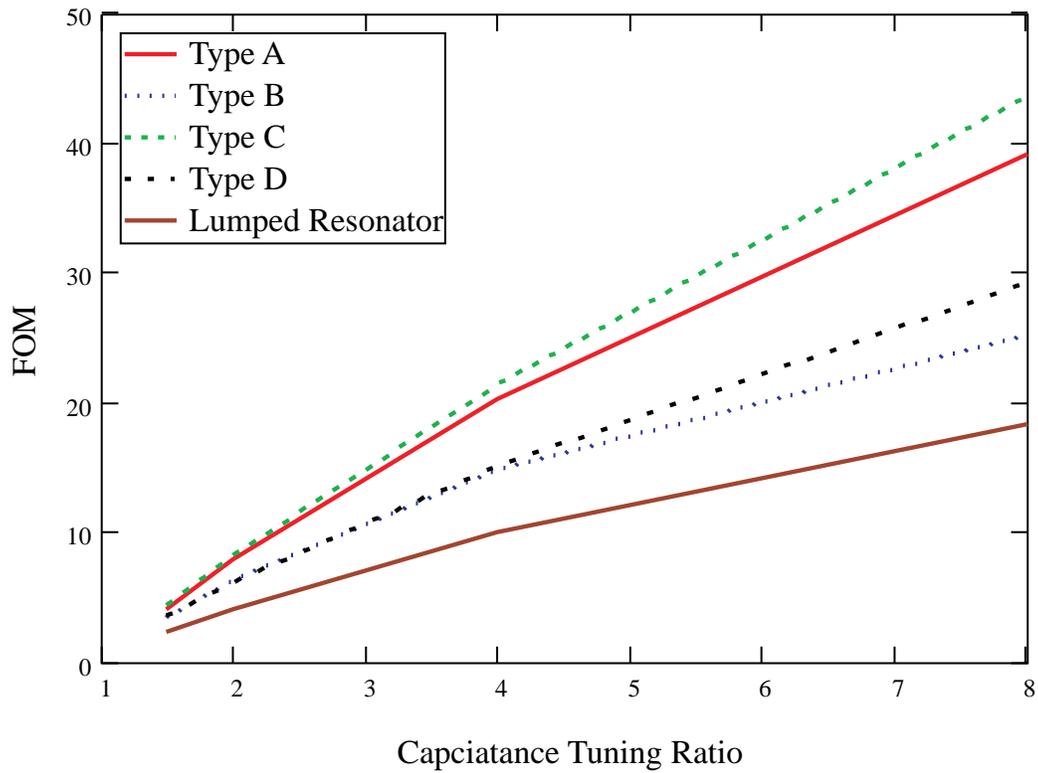


Figure 4.4: FOM for various network topologies versus capacitance tuning ratio, Q factor for varactor for all topologies and fixed value inductor in the lumped element resonator case assumed to be was 20, Q of transmission line resonator was > 200

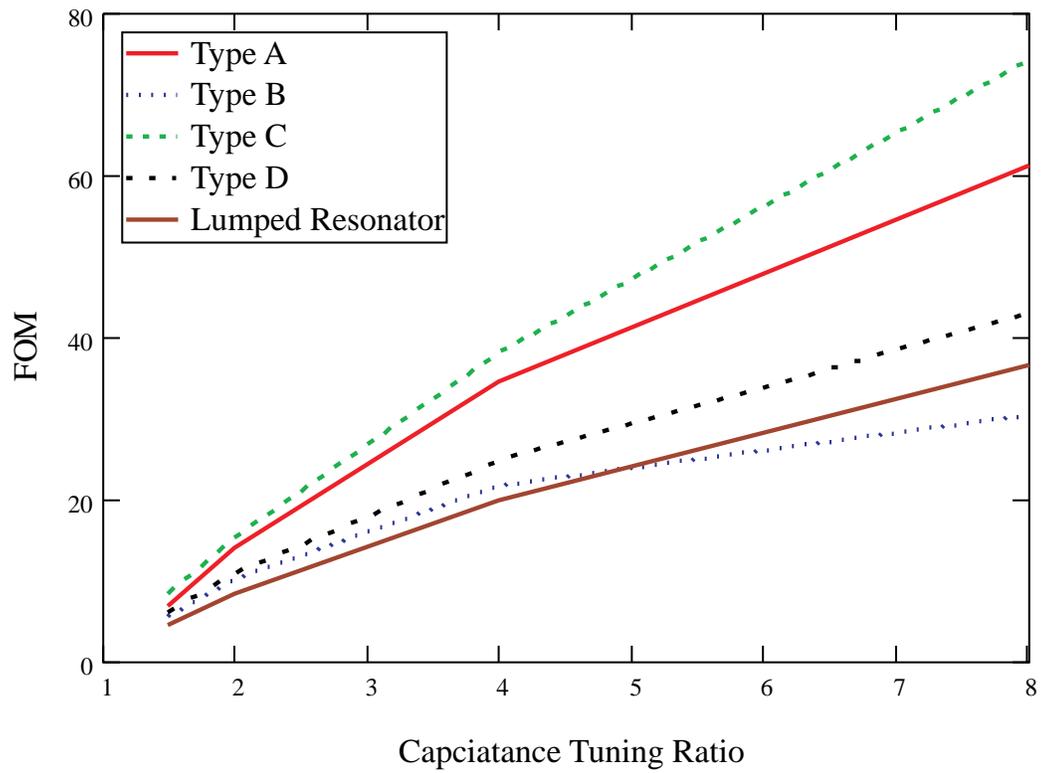


Figure 4.5: FOM for various network topologies versus capacitance tuning ratio, Q factor for varactor for all topologies and fixed value inductor in the lumped element resonator case assumed to be was 40, Q of transmission line resonator was > 200

Overall, distributed resonators provide more flexibility in terms of trade-off between loss and tunability, thus providing a larger design space.

The following section describes the technique for a single distributed resonator loaded with a capacitor in series along its length (Type D). The objective was twofold. The first was to determine the optimum capacitance for a given position along the line and the second was to determine the optimum position along the line for a given optimum capacitance. The two are complementary, as will be shown later.

4.2.3 Quarter-wave varactor loaded resonator

A short-circuited quarter-wave transmission line behaves like a parallel lumped element resonator at a frequency where its electrical length is 90° . The resonator can be made tunable in many ways including loading it with a varactor at the shorted end will as be discussed (see Figure 4.6). The series varactor has the effect of increasing the resonant frequency for a given physical length. This is because the capacitor adds negative electrical length to the transmission line and hence the resonant frequency must increase in order for the line to look electrically longer. The frequency at which this occurs is the new resonant frequency and the effective electrical length of the transmission line and the varactor combination becomes 90° and parallel resonance is restored. This is shown pictorially in Figure 4.7. The curve has been plotted for a 2.0 cm long line on FR4 substrate with a relative dielectric constant of 4.6. The line has been loaded by a 2.0 pF capacitor at the end. The total electrical length of the line and the capacitor combination is plotted. The two curves are for the two states of the tunable capacitor when it is changed from 2.0 pF to 1.0 pF. The intersection of the 90° line with the two curves gives the resonant frequency of the loaded resonator at two capacitor states, in this case 2.60 GHz and 2.94 GHz.

In this particular case the resonator frequency changed from 2.60 to 2.94 GHz as the capacitance changed from 2.0 to 1.0 pF. The frequency shift obtained from other values of nominal capacitance while keeping the tuning ratio, η ($\eta = 2$ in this case) fixed is listed in Table 4.12. As can be seen, the shift in frequency peaks for a nominal capacitance value of 2.0 pF for this particular case (see Figure 4.8).



Figure 4.6: Series capacitor loaded transmission line resonator

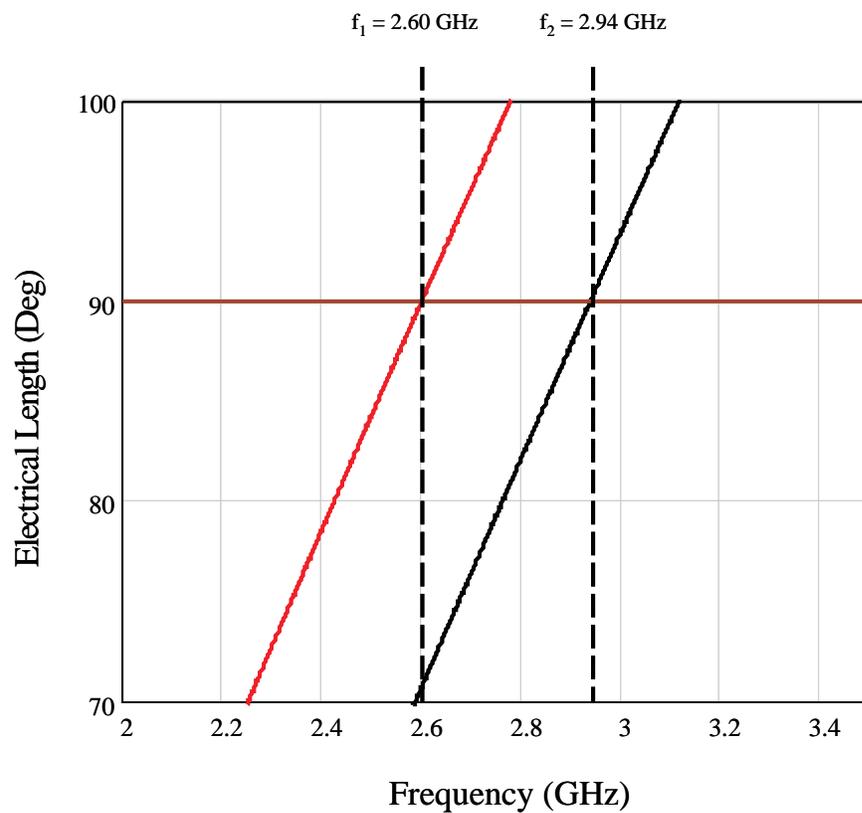
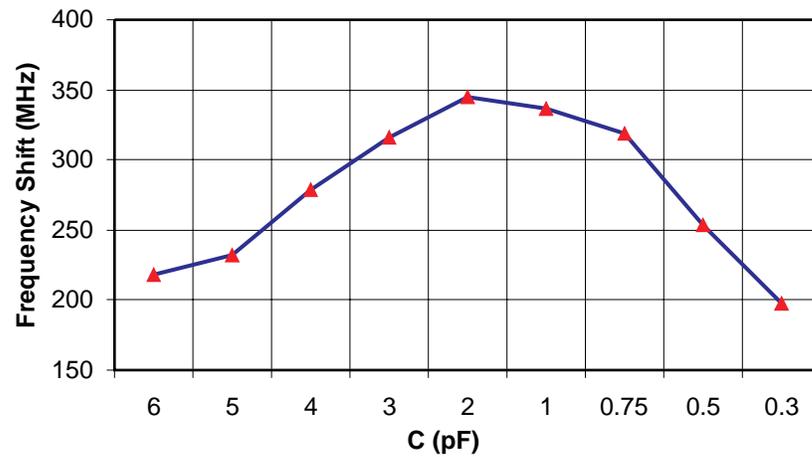


Figure 4.7: Total electrical length versus frequency for a capacitively loaded line resonator of length 2 cm on FR4, resonator frequency changed from 2.60 to 2.94 GHz as the capacitance changed from 2.0 to 1.0 pF, two lines are for capacitance value of 2.0 pF (left) and 1.0 pF (right)

Table 4.12: Frequency shift versus capacitance range

No.	Tuning Range	Frequency Shift(MHz)	Center Frequency (MHz)	% Tuning
1	6.0–3.0	218	2214	9.85
2	5.0–2.5	232	2268	10.23
3	4.0–2.0	279	2326	12.00
4	3.0–1.5	316	2428	13.00
5	2.0–1.0	339	2600	13.03
6	1.73–0.865	345	2667	12.93
7	1.0–0.5	337	2939	11.46
8	0.75–0.37	319	3074	10.37
9	0.50–0.25	254	3271	7.76
10	0.30–0.15	198	3471	5.70

Figure 4.8: Frequency shift versus capacitance (for $\eta = 2$).

This peaking behavior of the shift in resonant frequency can be understood from the fact that on a Smith Chart the change in electrical length for a fixed capacitance ratio is dependent on the nominal value of the capacitance. For instance, for a 2:1 capacitance change, a corresponding reactance change near the open-circuit position from say 100Ω to 200Ω results in a much smaller change in electrical length than the one resulting from 0.5Ω to 1.0Ω reactance change in the center of the Smith Chart. This suggests the possibility of finding an optimum value of capacitance for which the change in electrical length is maximum. This will now be investigated using standard differentiation techniques.

The phase angle of the reflection coefficient of a transmission line for a lossless capacitive load is given by:

$$\theta_{1c} = \tan^{-1} \left(\frac{1}{2\pi f C_o Z_o} \right) \quad (4.14)$$

Here Z_o is the characteristic impedance of the transmission line, C_o is the loading capacitance, f is the frequency of operation, and θ_{1c} , θ_{2c} , and $\Delta\theta$ are in radians.

If the capacitance tuning ratio is η , the capacitance in the biased state becomes C_o/η and the phase angle of the reflection coefficient becomes:

$$\theta_{2c} = \tan^{-1} \left(\frac{\eta}{2\pi f C_o Z_o} \right) \quad (4.15)$$

The change in phase angle is given by:

$$\Delta\theta = \theta_{2c} - \theta_{1c} = \tan^{-1} \left(\frac{\eta}{2\pi f C_o Z_o} \right) - \tan^{-1} \left(\frac{1}{2\pi f C_o Z_o} \right) \quad (4.16)$$

Now let:

$$k = \left(\frac{1}{2\pi f C_o Z_o} \right) \quad (4.17)$$

Here k is a variable defined in terms of the characteristic impedance, loading capacitance, and the frequency of operation.

Using Equation (4.17) above, Equation (4.16) becomes:

$$\Delta\theta(k) = \tan^{-1} (\eta k) - \tan^{-1} (k) \quad (4.18)$$

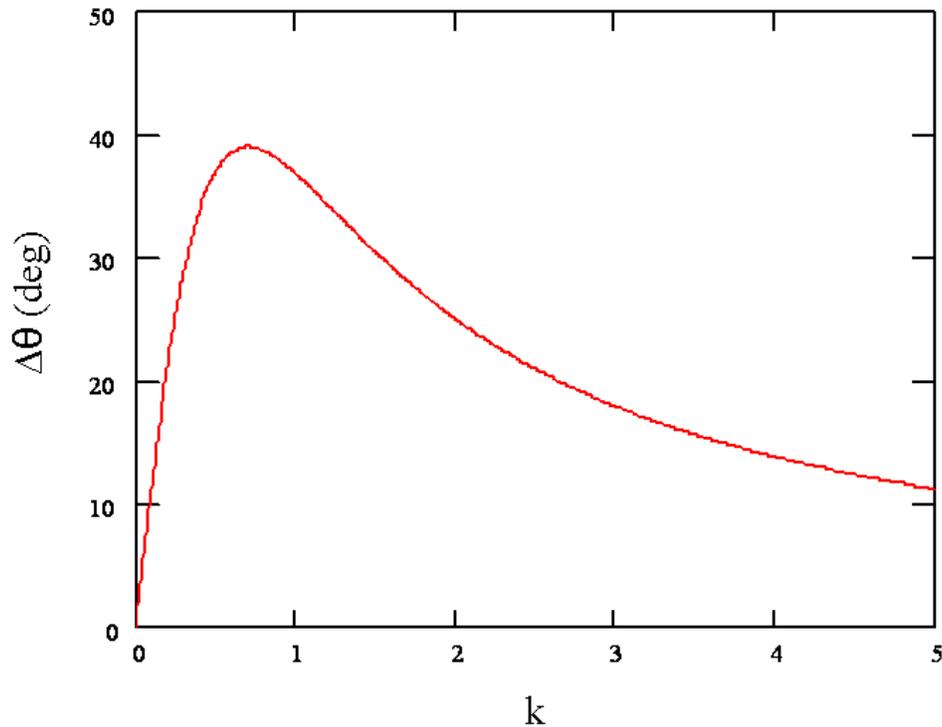


Figure 4.9: Phase change versus k for $\eta = 2$, and $Z_o = 50 \Omega$

By differentiating Equation (4.18) with respect to the variable k and equating the derivative to zero that the maximum value of $\Delta\theta$ occurs when the following condition is satisfied:

$$k = \frac{1}{\sqrt{\eta}} \quad (4.19)$$

The plot of phase change versus k for $\eta = 2$, and $Z_o = 50 \Omega$ is shown in Figure 4.9.

Equation (4.19) above is the key to designing tunable resonators with maximum tuning for a given capacitance ratio. All parameters required for the design can be deduced from this important result. The technique will now be described. The maximum phase change as a function of the capacitance tuning ratio is plotted in

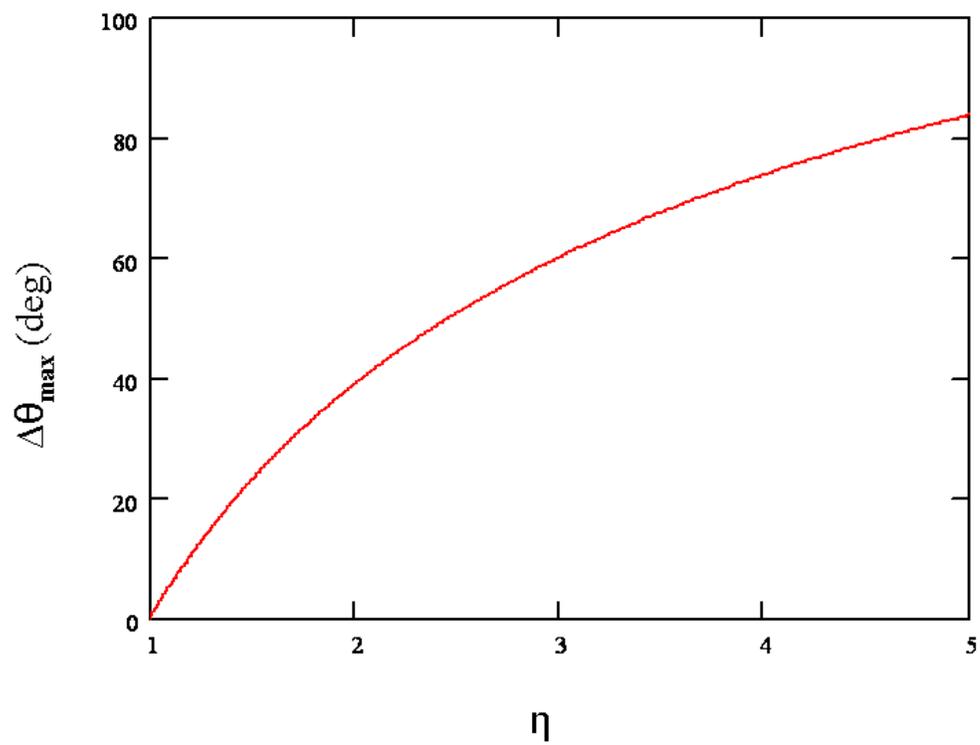


Figure 4.10: Maximum phase change of input reflection coefficient for a capacitively loaded resonator for a given capacitance tuning ratio.

Figure 4.10.

For the purposes of further discussion, it should be noted that for $\eta = 2$, the maximum phase change can be calculated using Equation 4.16 and was found to be 38.942° when the normalized reactance of the capacitor is 0.707 and changes to 1.414, for a 2:1 capacitance change. A 2:1 capacitance change is considered here since this is what is achieved with a BST varactor optimized to have a loss tangent of 0.01 and so a maximum Q factor of 100. This is readily seen from the Smith Chart as well. An expanded view of the Smith Chart highlighting this is shown in Figure 4.11 below. Using a protractor this can indeed be verified to be true.

The procedure for obtaining maximum tuning is outlined below. It consists of the following steps:

1. First select the desired resonant frequency
2. Next look up the optimum capacitance value using the chart (Figure 4.12)
3. Now adjust the physical length of the resonator such that its nominal resonant frequency coincides with the desired resonant frequency chosen in step 1 above.
4. The % tuning thus obtained will be the maximum for the given change in capacitance ratio.

Step 2 above requires a little more explanation. Since the equations governing the resonant frequency are transcendental equations they cannot be solved in an explicit manner. A graphical solution must be obtained. This is shown in Figure 4.13. The intersection points of the two phase lines for the capacitors with that of the phase line for the resonator gives the resonant frequency at each of the two states of the capacitor.

4.2.4 Optimum loading position for a tunable resonator

The result obtained above is a fundamental result and shows the limit of maximum tuning that can be attained for the given topology. The next step is to find if there

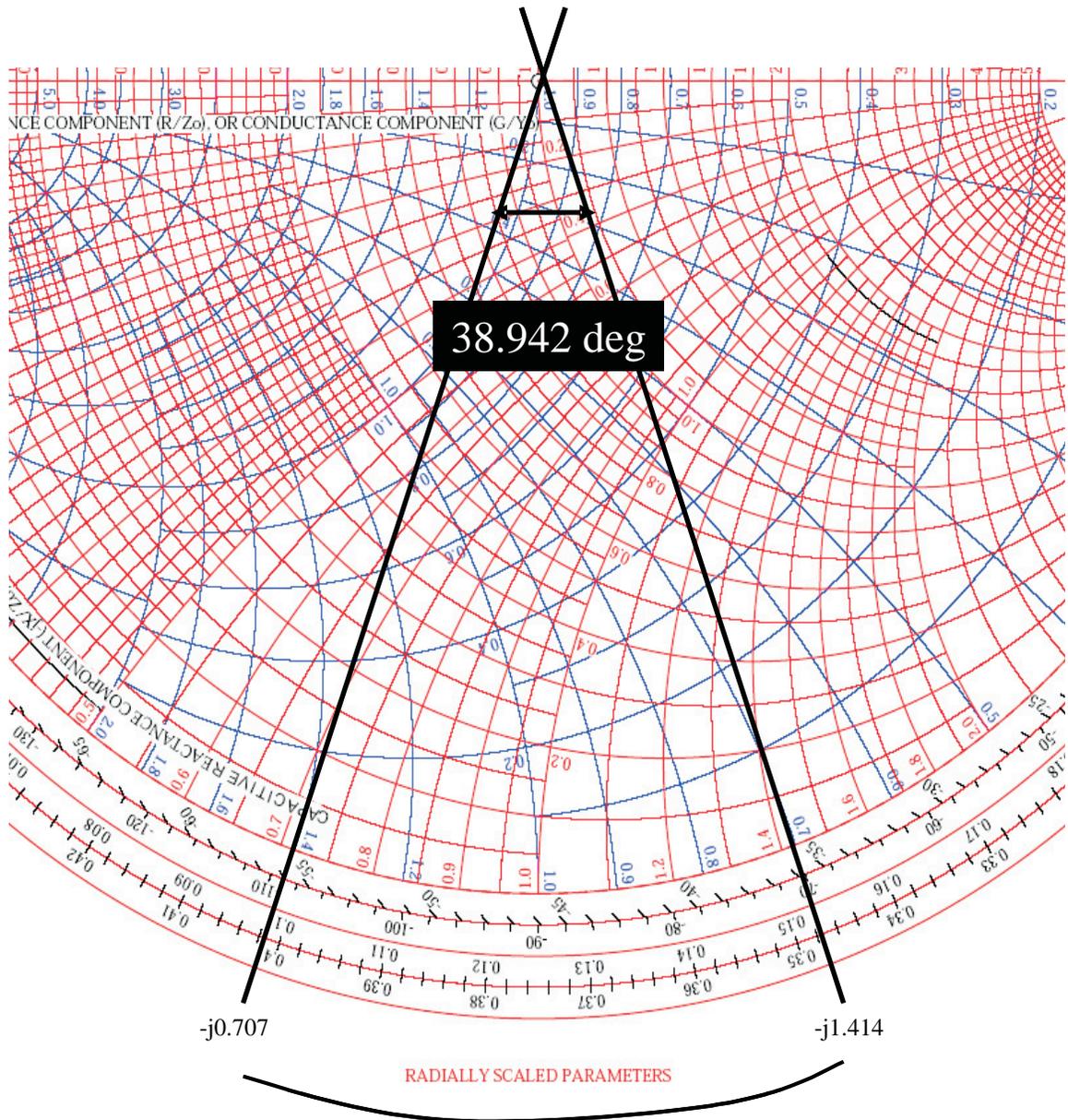


Figure 4.11: Maximum phase change of reflection coefficient for a capacitive load on an expanded view of the smith chart that can be achieved for with a 2:1 capacitance change.

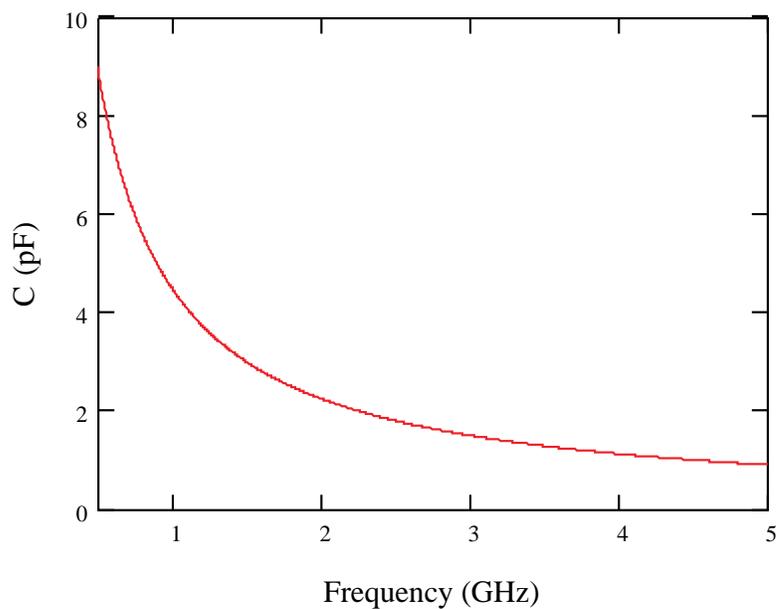


Figure 4.12: Optimum capacitance value for maximum tuning for $\eta = 2$, and $Z_o = 50\Omega$.

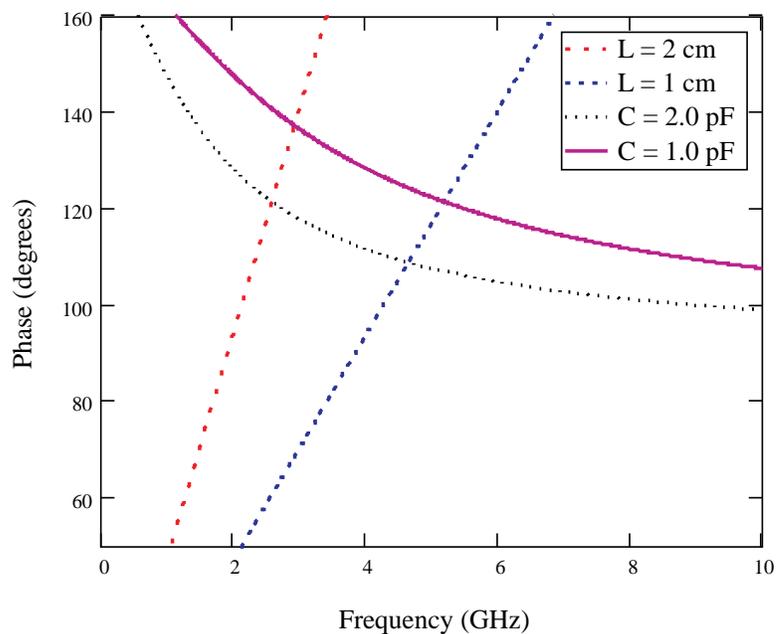


Figure 4.13: Graphical solution of resonant frequency for a capacitively loaded line, intersection of phase curves for the transmission line and the reflection coefficient phase of the capacitive load gives the resonant frequency of the capacitively loaded resonator.

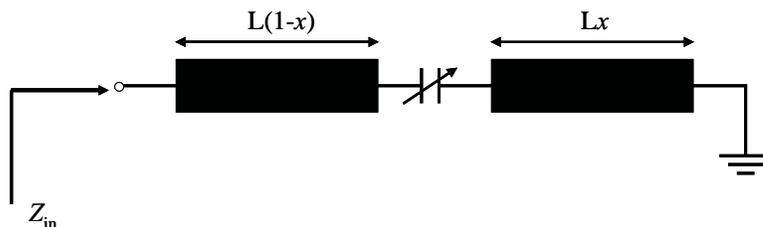


Figure 4.14: Resonator loaded with a varactor at position x ($0 \leq x \leq 1$) from the shorted end, total length is L .

is any optimum loading position along the length of the line for which the tuning is optimized. This question will be addressed now. The split resonator with the series capacitive loading at a position x along the line is shown in Figure 4.14. The frequency shift for different values of x with the constraint that $0 \leq x \leq 1$ was investigated.

It was found that just as there is an optimum value of loading capacitor there is an optimum position along the line for maximum tunability. The results for varying x from 0 to 1 is shown in Figure 4.15. It is observed that for $x = 0.3$ the tuning is maximum. It should be noted that the optimized condition found in the previous section was used for generating this result, all other parameters are the same as before.

The shift in resonant frequency as a function of x was also calculated numerically and the results, both in terms of absolute shift in frequency as well as % shift in frequency, are shown in Figures 4.16 and 4.17 respectively. It can be seen that both the absolute and % shift in tuning peaks at a values of $x = 0.3$ as perviously indicated. The peaking behavior is again due to the fundamental results obtained in the pervious section and can be seen intuitively on a Smith Chart.

Thus, the technique of designing resonators with optimal tuning is two fold: first find the value of the optimum capacitor and the line length for the desired resonant frequency and then place the capacitor at the optimum position along the length of the line. The experimental verification of tuning and Q factor trade-off for two different network topologies loaded with similar tuning elements will be presented in the next section. This procedure is quite general and can be repeated for other network types such as those previously discussed.

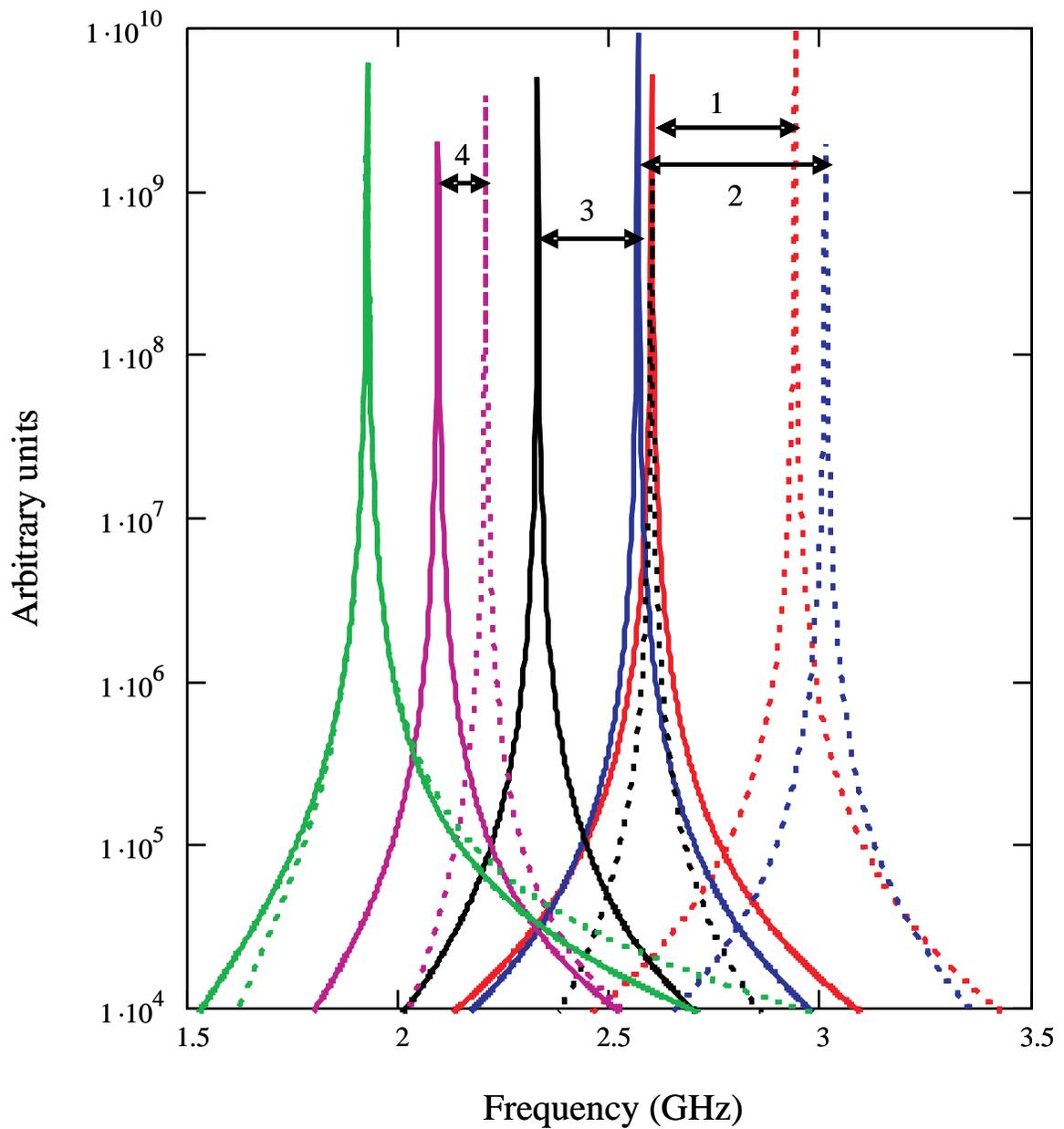


Figure 4.15: Shift in resonant frequency for various values of x ; 1($x = 0.0$); 2($x = 0.3$); 3($x = 0.5$); 4($x = 0.7$); solid lines, $C = 2.0$ pF; broken lines, $C = 1.0$ pF, corresponding to $\eta = 2$.

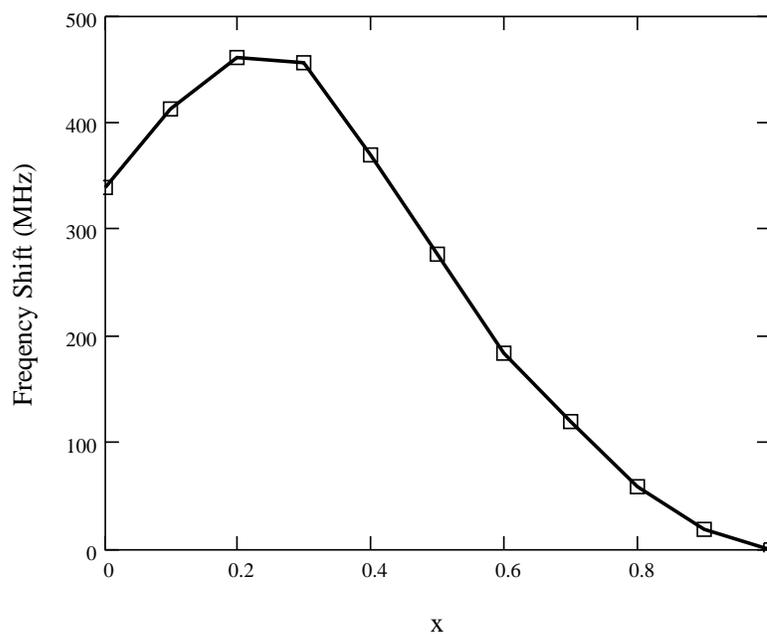


Figure 4.16: Shift in resonant frequency as function of x for $\eta = 2$ and center frequency corresponding to the curves in Figure 4.15.

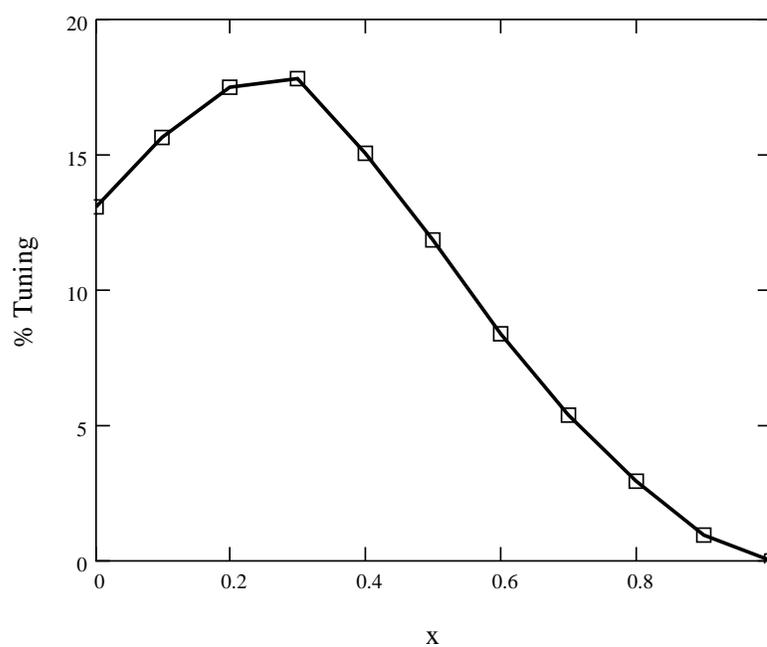


Figure 4.17: Percentage shift in resonant frequency as function of x for $\eta = 2$ and center frequency corresponding to the curves in Figure 4.15.

Table 4.13: Resonator design parameters

Parameter	Value
Material	FR4
Dielectric Constant	4.6
Loss Tangent	0.016
Height	62 mil
Metal thickness	34 μm
Resonator length	2.0 cm
Resonator impedance	50 Ω
Resonator line width	2.9 mm
Coupling Gap	800 μm
Loading parameter (x)	0.3
Varactor	Skyworks 1232-079
Varactor tuning range	6:1

4.2.5 Experimental verification of optimal tuning

Two resonators were designed and characterized in order to verify the principles introduced in the previous section. In the first design the resonator was loaded with a capacitor at the end of the line while in the second design the resonator was loaded at a position $x = 0.3$ along the length of the line. The parameters common to both design are given in Table 4.13.

The design was implemented and verified using a circuit-EM co-simulation in ADS. The layout of two different design is shown in Figures 4.18 and 4.20 respectively. Design I is for case where the resonator is loaded at the end of the line, while Design II is the case where the resonator is loaded at an optimum position along the length of the line. The photographs of the two resonator designs are shown in Figures 4.19 and 4.21 for $x = 0.3$.

The resonators were weakly coupled to the input and output port so that the loaded and unloaded Q factor would be equal. This aids in the extraction of unloaded Q and also renders fabrication easier. The bias was applied to the resonators using a short circuited quarter wave line of high characteristic impedance. At one end of the bias line a 100 pF (rated to 50 V) decoupling capacitor was attached. This provided an RF short while simultaneously providing for a DC open, enabling bias voltage to

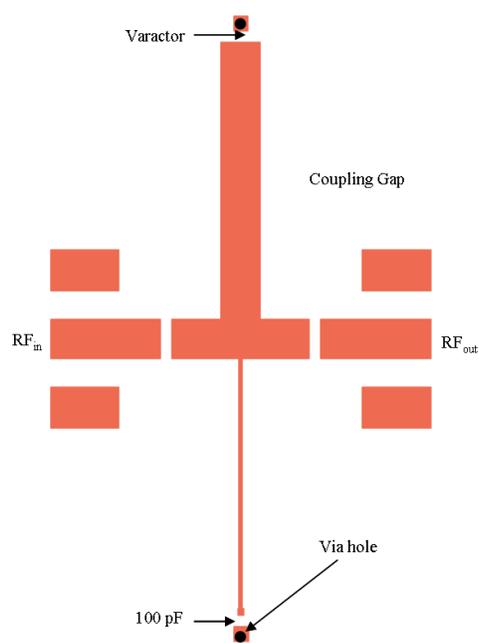


Figure 4.18: Resonator layout: Design I.

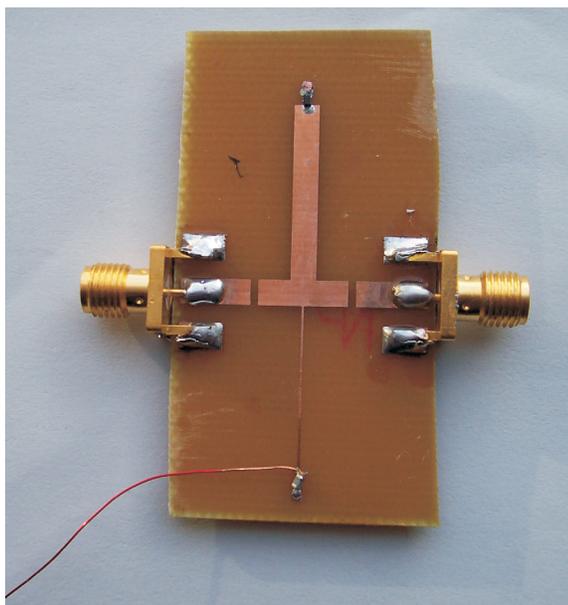


Figure 4.19: Fabricated resonator: Design I.

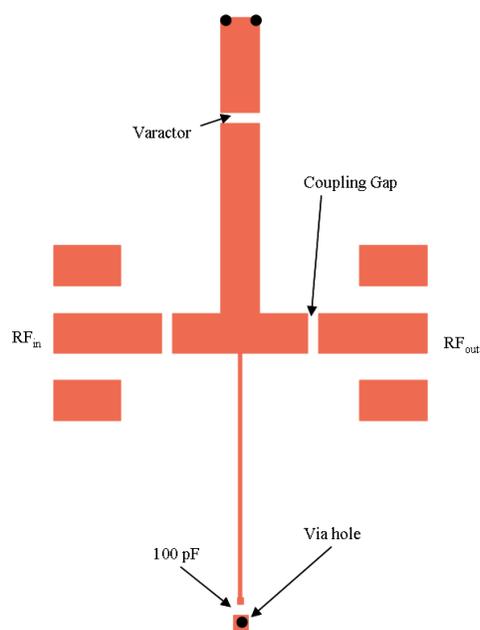


Figure 4.20: Resonator layout: Design II.

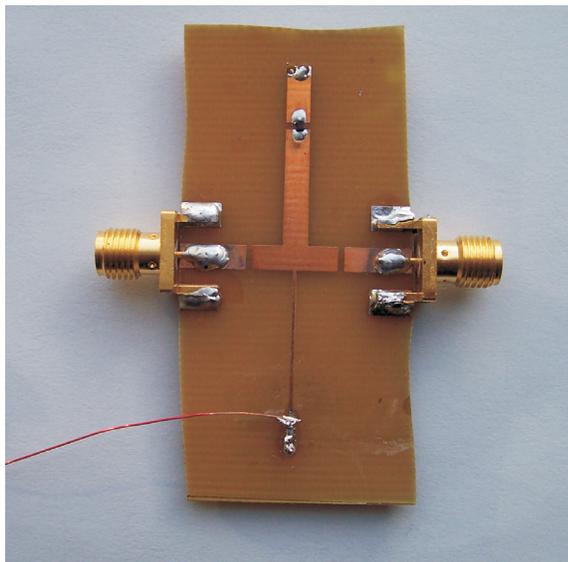


Figure 4.21: Fabricated resonator: Design II.

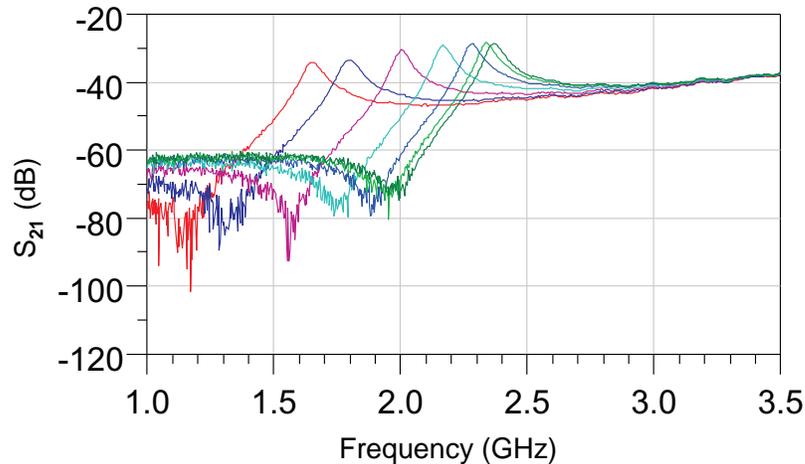


Figure 4.22: Measured S_{21} for Design I, increasing bias (decreasing capacitance) from left to right, 0 V, 1 V, 3 V, 5 V, 8 V, 11 V, and 15 V.

be applied at this point. The input and output port connections were made using edge-launch SMA connectors. The FR4 board was fabricated using an in-house PCB process. SMT components were attached using solder paste. All measurements were made on a HP 8510C vector network analyzer with a full two-port calibration from 1.0 to 3.5 GHz. The results are shown in Figures 4.22 and 4.23 for the end-loaded and the split resonator respectively.

The S-parameter data was recorded with varying bias and post-processing was done in MathCAD[®]. The results show a marked difference in tuning between the two designs, as was expected from the analysis presented in the previous section. The tuning data with bias is shown in Figure 4.24 and the rate change with bias is shown in Figure 4.25. It can be clearly seen that the design with the split resonator has more tuning range than the one with the capacitor loaded at the end. Also the rate change of frequency with bias is greater for the split resonator design, as would be expected. The Q factor data with bias was extracted using the 3 dB method and is plotted in Figure 4.26. Due to the weak couplings used at the input and output

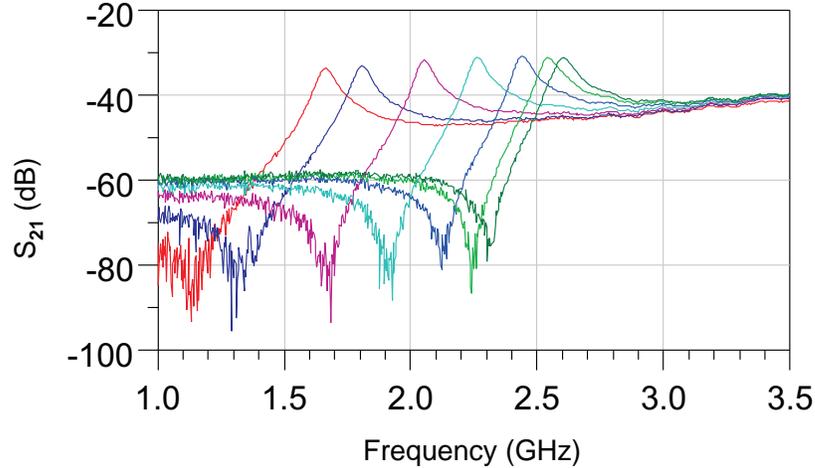


Figure 4.23: Measured S_{21} for Design II, increasing bias (decreasing capacitance) from left to right, 0 V, 1 V, 3 V, 5 V, 8 V, 11 V, and 15 V.

ports, the loaded and unloaded Q factors are the same to within $\pm 3\%$ over the same voltage tuning range. It can be seen that the Q factor for the split resonator (Design II) design is slightly lower than for the resonator with loading at the end (Design I). This is especially true at the higher end of the bias range. This point will be explained later when the trade-off between Q factor and tunability will be discussed. It will be shown that a slight deterioration in Q factor results in substantial gain in tuning and in most situations this would be an acceptable or rather a desired trade-off.

Before analyzing the tuning data for the two resonators, it is essential to digress in order to calculate the capacitance tuning range and other parameters at the frequency of interest. This is essential since the analysis will be based on the capacitance values and the tuning range at the frequencies of interest while the Skyworks datasheet only provides data at 50 MHz (as is the case with almost all varactor manufacturers). This is presented in the next section. Hence the varactor must be characterized at those frequencies before resonator tuning data is analyzed further.

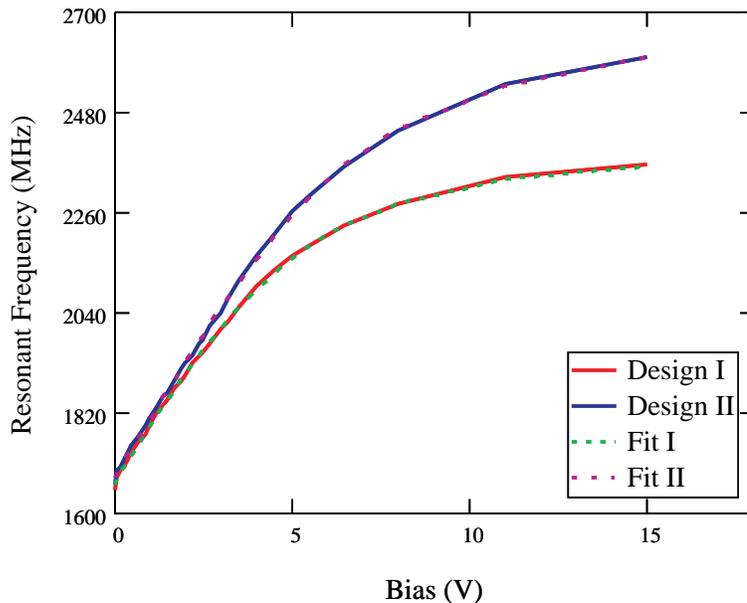


Figure 4.24: Measured resonant frequency tuning with bias.

4.2.6 Parameter extraction of varactor diode at RF frequencies

A methodology for extraction of the varactor model at RF frequencies will be presented. The capacitance, series resistance and hence the Q factor is expected to be different at 1–3 GHz, compared to the data available at 50 MHz.

The varactor was characterized using a transform method introduced in [84]. Using this technique the impedance of the varactor under test is transformed from the edge of the Smith[®] Chart to the center over a narrow range of frequencies. This improves the accuracy of the model extraction substantially. In a one-port reflection type measurement, the error in phase of S_{11} at the edge of the Smith[®] Chart degrades the accuracy of the method. In the transform method this is avoided since the varactor is matched to 50Ω . This is accomplished by loading the varactor at the end of the transmission line shorted at both ends and appropriately tapping along the length of the line for the input port. This is shown in the layout in Figure 4.27.

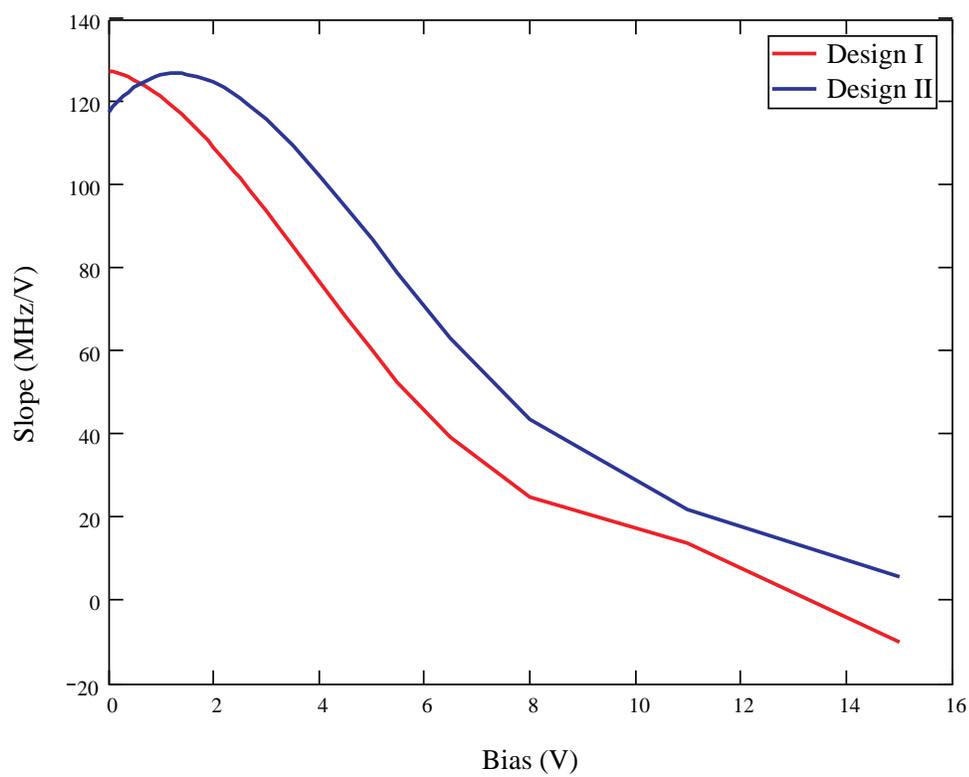


Figure 4.25: Measured rate change of resonant frequency with bias.

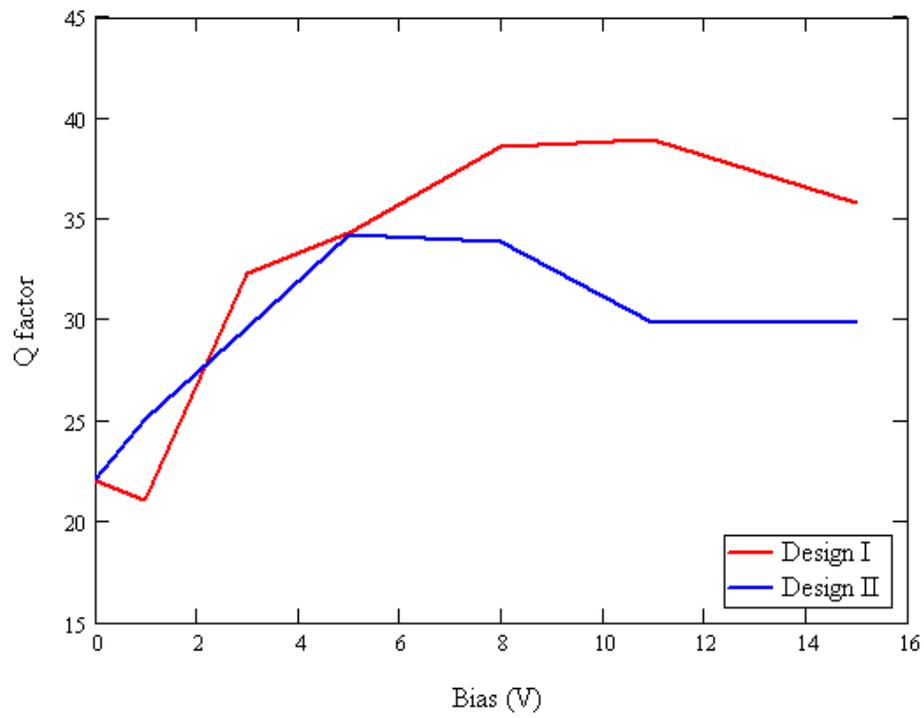


Figure 4.26: Measured Q factor with bias.

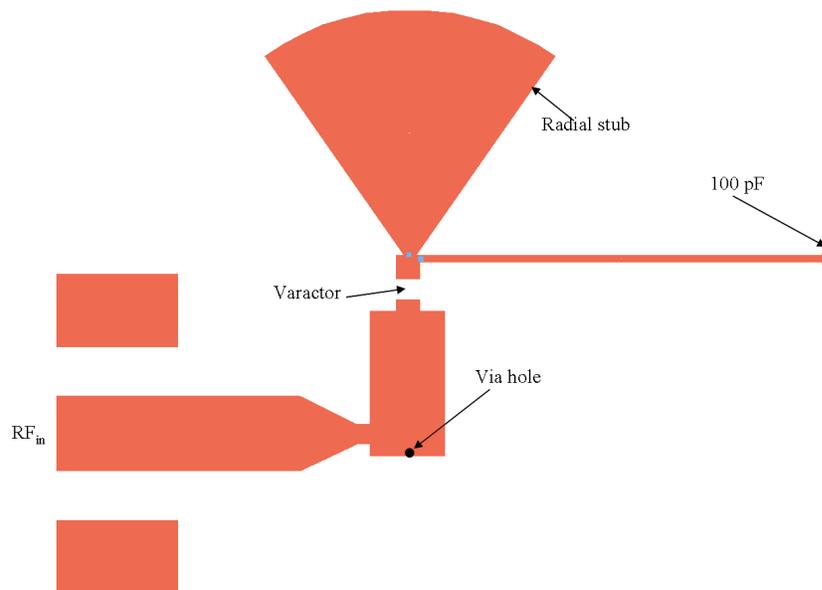


Figure 4.27: Layout for varactor parameter extraction circuit.

The fabricated fixture with the diode mounted on it is shown in Figure 4.28.

The radial stub and the high impedance quarter-wave line at the end of the varactor provide an RF short while providing a floating DC node for application of bias. The design was implemented in ADS using a circuit-EM co-simulation method for improved accuracy. The one-port reflection data was measured over a 1.5–3.5 GHz frequency range and the bias was swept from 0 to 15 V in appropriate steps. The tuning data is shown in Figure 4.29 and it can be seen that the matching for all bias voltages is better than 7 dB. This is sufficient to extract an accurate model. The data post-processing was done in ADS and a series RLC model was fitted to the measured data over the bias and frequency range. Again, circuit-EM co-simulation was used for increased accuracy. An physical line length of 7 mm in PTFE (Polytetrafluoroethylene) dielectric was added at the input port in the model to account for the fact that reference plane of the VNA calibration was not at the edge of the FR4 board but at the end of the return cable 3.5 mm connector on the VNA where calibration was performed. This corresponds to an electrical delay of 24° at 2 GHz. The value of

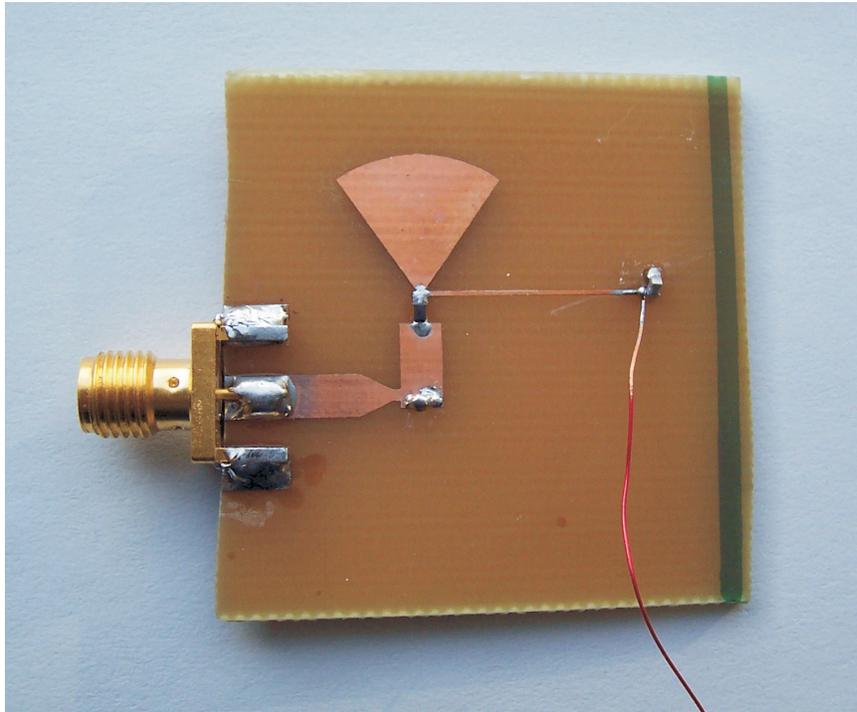


Figure 4.28: Fabricated test fixture for diode characterization.

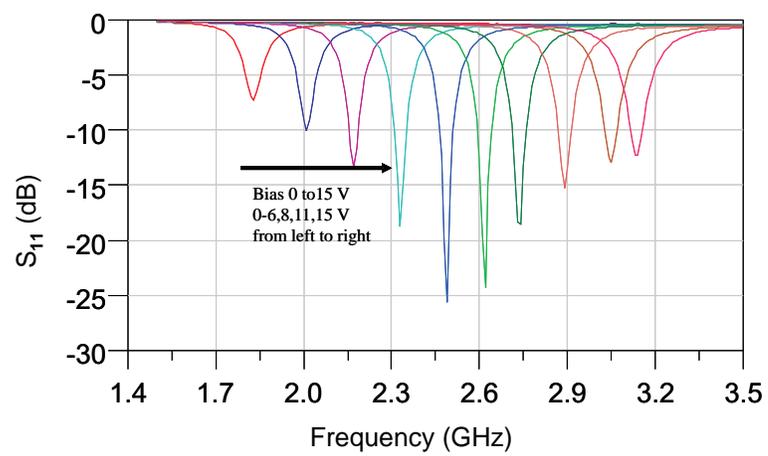


Figure 4.29: Measured S_{11} data versus bias for the varactor.

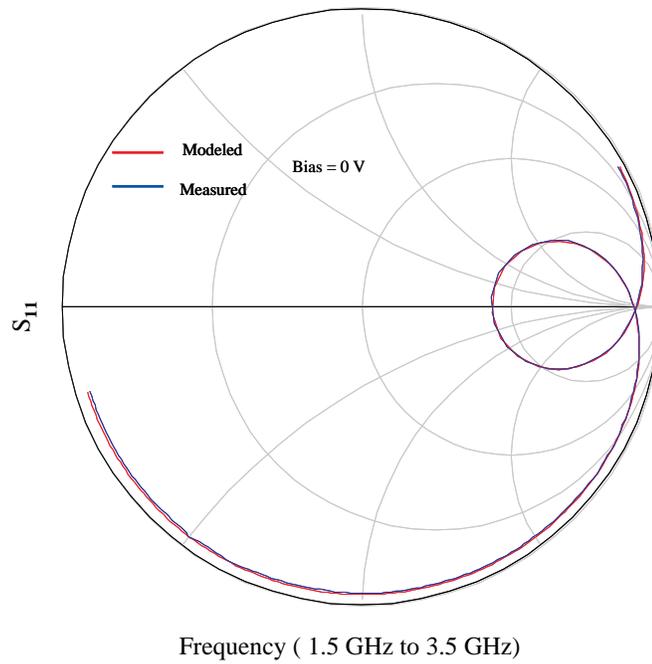


Figure 4.30: Fit of S_{11} on a Smith Chart at 0 V bias.

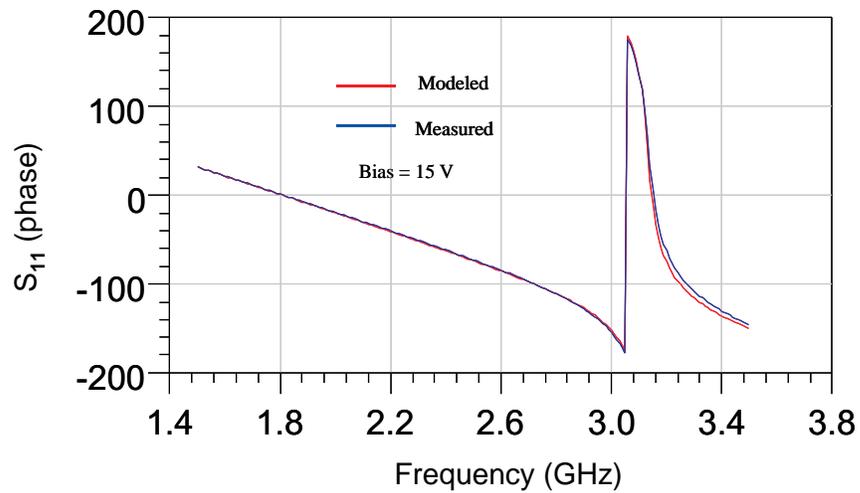


Figure 4.31: Fit of $S_{11}(\text{phase})$ with model at 15 V.

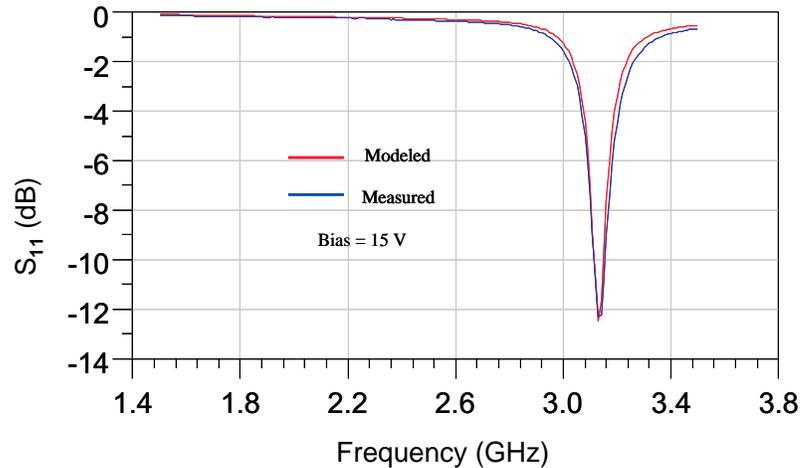


Figure 4.32: Fit of S_{11} (dB) with model at 15 V.

parasitic inductance used was 0.7 nH as found in the manufacturer's data sheet for a SC-79 package. The fit between modelled and measured data is shown in Figure 4.30 for 0 V bias and in Figures 4.31 and 4.32 for 15 V bias. It can be seen that the fit is excellent, over both magnitude and phase over the range of bias voltages. Only the two extremes of the bias range is shown for clarity but the model work equally well at all bias points. The extracted capacitance as function of bias is shown in Figure 4.33.

The zero-bias capacitance is 3.9 pF and it decreased to 0.55 pF at 15 V. This is slightly smaller than the 4.15 pF and 0.72 pF quoted on the manufacturer datasheet at 50 MHz. Considering the tolerances in the manufacturing process this is a reasonable range. The series resistance was similarly extracted and the result is shown in Figure 4.34. The zero-bias resistance is 2.1 Ω and is considerably higher than the 1.5 Ω quoted by the manufacturer at zero bias and 50 MHz. The resistance decreased to 1.1 Ω at 15 V bias. The extracted value of capacitance and series resistance was then used to calculate the Q factor as a function of bias at 2 GHz and the results are shown in Figure 4.35. Exponential fit of C_v using a standard semiconductor varactor model and also a dual exponential model was carried out. It was found that the dual exponential fit (Equation (4.20)) has much better accuracy over the bias range than

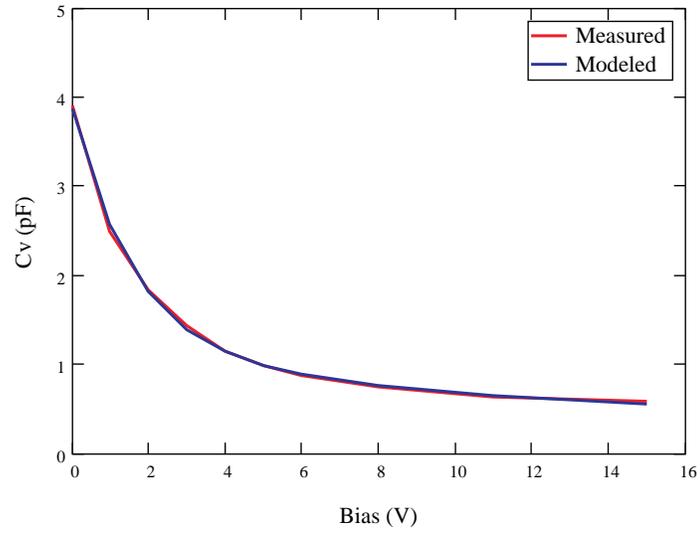


Figure 4.33: Extracted capacitance (C_v) versus bias.

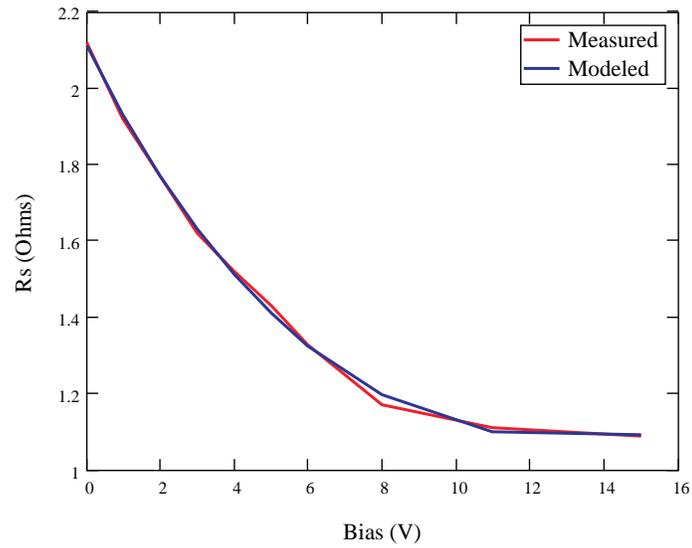


Figure 4.34: Extracted series resistance (R_s) versus bias.

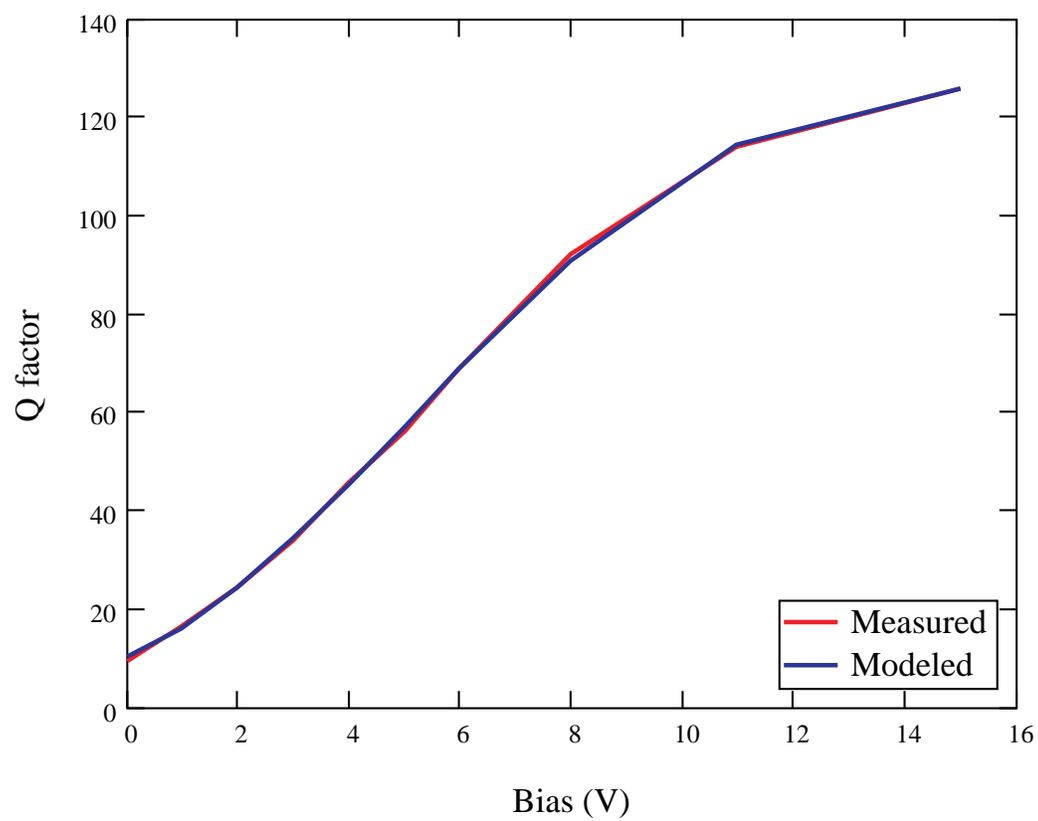


Figure 4.35: Extracted Q factor versus bias at 2 GHz.

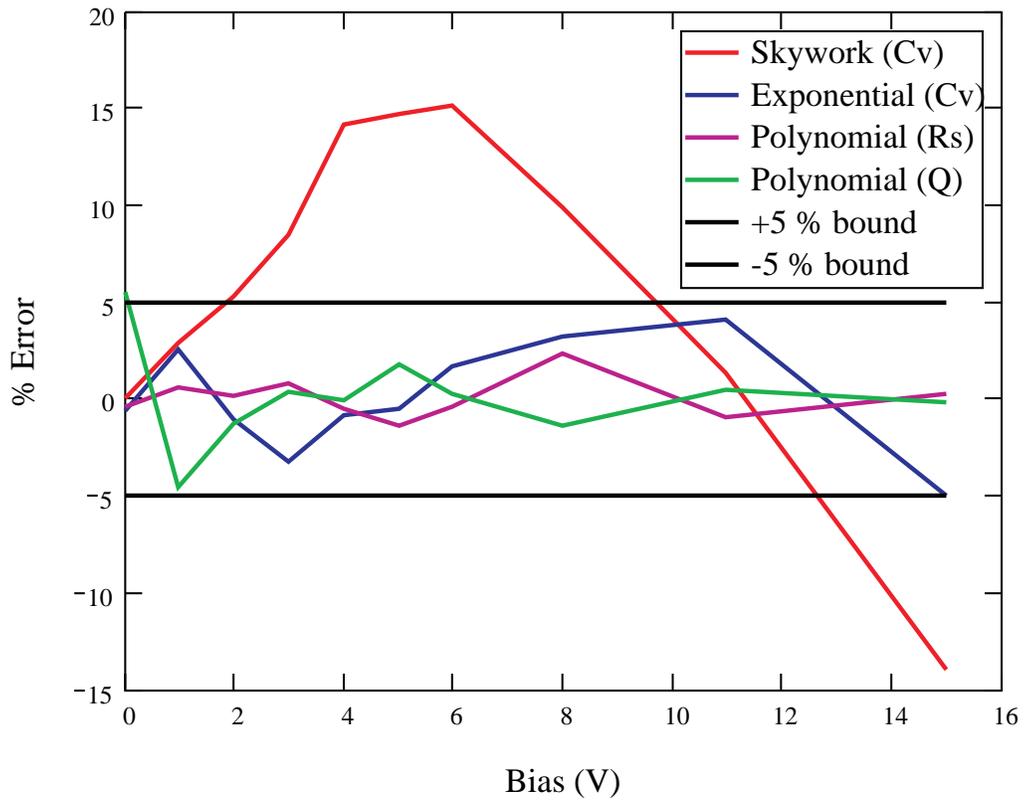


Figure 4.36: Percentage error for the model for C_v , R_s , and Q factor.

the standard model (Equation (4.21)). Though the former does not have any physical meaning, it will suffice since only interpolated capacitance values at bias points other than those measured are required. The error is shown in Figure 4.36 and it can be seen that the dual exponential model has less than $\pm 5\%$ error over the bias range compared to over 15% error for the standard model at the low and high end of the bias range.

$$C_{\text{exp}}(V) = 2.844e^{-0.5921V} + 1.034e^{-0.04202V} \quad (4.20)$$

$$C_{\text{skyworks}}(V) = \frac{3.9}{\left(1 + \frac{V}{1.7}\right)^{0.9}} \quad (4.21)$$

$$R_s(V) = 2.112 - 0.1919V + 0.01137V^2 - 0.0002105V^3 + 2.311(10^{-7})V^4 \quad (4.22)$$

$$Q(V) = 10.15 + 4.099V + 1.731V^2 - 0.1504V^3 + 0.003402V^4 \quad (4.23)$$

Polynomial curve fits for the extracted series resistance (R_s) and Q factor (Q) were also obtained using the curve fitting routine in Matlab®. The error for the 4th order polynomial fit for R_s (Equation (4.22)) and Q (Equation (4.23)) is shown in Figure 4.36. As for the fit of capacitance, the error is less than $\pm 5\%$ over the bias range. The analysis of the tuning data using the extracted capacitor parameters will be presented in the following section.

4.2.7 Results and discussion

A summary of tuning data is listed in Tables 4.14 and 4.15 shows the center frequency and tuning range for different capacitance range for the two designs. The percentage change in resonant frequency for different capacitance changes is also listed in Table 4.16. Frequency shift for the two different designs for various capacitance

Table 4.14: Summary of resonator tuning data (Center frequency versus capacitance)

Capacitance (pF)	Center Frequency (MHz) Design I (end-loaded)	Center Frequency(MHz) Design II (split-resonator)
3.89	1650	1661
3.55	1692	1702
3.40	1702	1714
3.13	1732	1747
2.66	1770	1792
2.22	1837	1856
2.00	1872	1890
1.72	1927	1942
1.50	1970	2010
1.33	2017	2070
1.14	2097	2164
0.98	2162	2261
0.85	2230	2362
0.66	2335	2539
0.55	2365	2599

Table 4.15: Summary of resonator tuning data (absolute frequency shift)

Capacitance Range(pF)	η	Frequency Shift(MHz) Design I (end-loaded)	Frequency Shift(MHz) Design II (split-resonator)
3.89–0.55	7.07:1	715	938
3.4–1.7	2.0:1	225	228
3.13–1.5	2.09:1	238	263
2.66–1.33	2.0:1	247	278
2.0–1.0	2.0:1	290	371
1.33–0.66	2.0:1	318	469
1.14–0.55	2.07:1	268	435
0.85–0.55	1.54:1	135	237
0.85–0.66	1.29:1	105	177

Table 4.16: Summary of resonator tuning data (% frequency shift)

No.	Capacitance Range(pF)	Frequency Shift(MHz) Design I (end-loaded)	Frequency Shift(MHz) Design II (split-resonator)
1	3.89–0.55	43.33	56.47
2	3.4–1.7	13.22	13.30
3	3.13–1.5	13.74	15.05
4	2.66–1.33	13.95	15.51
5	2.0–1.0	15.49	19.63
6	1.33–0.66	15.76	22.65
7	1.14–0.55	12.78	20.10
8	0.85–0.55	6.05	10.03
9	0.85–0.66	4.70	7.49

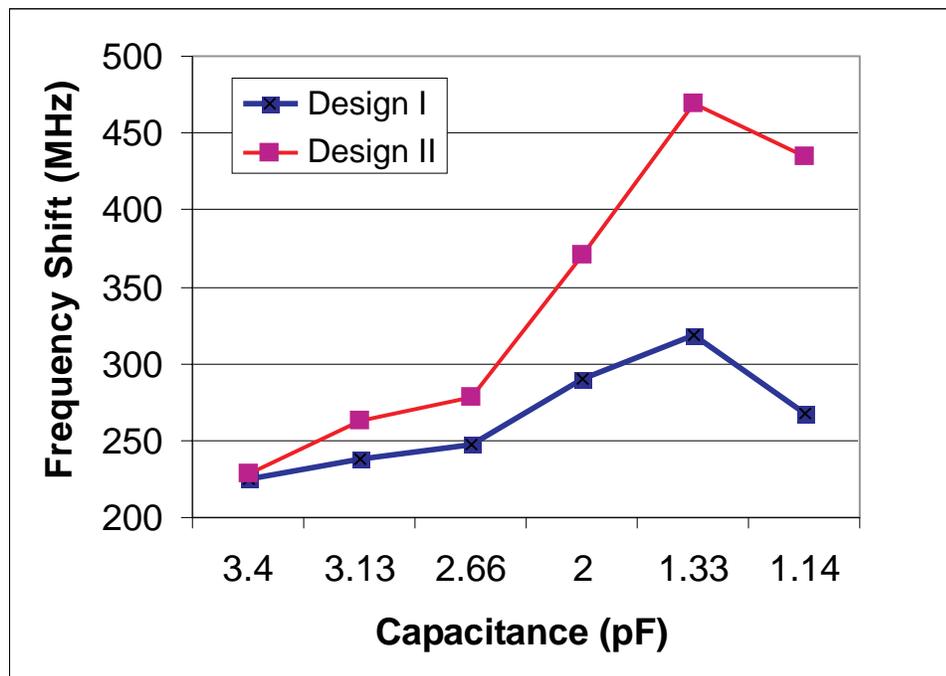


Figure 4.37: Frequency shift for Design I and II as a function of capacitance.

values is shown in Figure 4.37. Some interesting trends can be observed in light of the theory presented in the previous sections:

- For each type of design the shift in resonant frequency is a function of the nominal capacitance for a fixed capacitance ratio $\eta=2$. There is also an optimum value of capacitance. In our case this happens when the capacitance changes from 1.33 pF–0.66 pF.
- The split resonator design offers more tuning than the end-loaded resonator for the optimum capacitor loading (in this case 1.33 pF). The tuning is 47.5% or 151 MHz more in the case of the split resonator (see No. 6 in Table 4.15).
- Over the complete tuning range, the end-loaded resonator tunes 718 MHz while the split resonator tunes 938 MHz (see No. 1 in Table 4.15). This is 220 MHz or 30% more tuning for the same bias range.
- Over a 1.55:1 change in capacitance from 0.85–0.55 pF the change in resonant frequency for the end-loaded design is 135 MHz while it is 237 MHz for the split-resonator design (see No. 8 in Table 4.15). This is a substantial increase of 75% more tuning for the same capacitance range.
- Over a slightly smaller tuning range of 1.29:1 from 0.85–0.66 pF the change in resonant frequency for the end-loaded design is 105 MHz while it is 177 MHz for the split-resonator design (see No. 9 in Table 4.15). This is still a substantial increase of 68.6% more tuning for the same capacitance range.
- The increased tunability come a price of lower Q factor (see Figure 4.26). The split resonator has a lower Q factor over a portion of the tuning range. The worst case situation occurs at 11 V bias where the Q factor for the end-loaded resonator is 39 while that for the split resonator is 30. Thus the Q factor of the end-loaded resonator is 30% higher at best. At the expense of slight reduction in Q factor substantial gain in tunability is obtained and depending on the capacitance range the increased tuning can be as high as 75% more.

Overall, the trade-off with Q factor results in substantially higher tunability and is a worthwhile compromise to make in the design of frequency-agile systems. The network transformation factor for Type I and Type II resonator designs will now be calculated. If tuning of the two topologies for capacitance change between 1.33 pF and 0.66 pF is considered, the network transformation factor for the two topologies can be found as follows:

$$\tau_{\text{NTF},1} = \frac{F_{r1}}{F_m} = \frac{\frac{2335}{2017}}{\sqrt{2}} = \frac{1.1576}{1.414} = 0.8186 \quad (4.24)$$

$$\tau_{\text{NTF},2} = \frac{F_{r2}}{F_m} = \frac{\frac{2539}{2070}}{\sqrt{2}} = \frac{1.2265}{1.414} = 0.8674 \quad (4.25)$$

Hence the network transformation factor of the Type II resonator is more than that of Type I resonator. However, as expected, the Q factor of Type II design is 30 at 11 V bias while the Q for Type I design is 39 at same bias voltage. Thus the maximum difference Q factor between the two resonator and hence represents the worst case scenario in terms of loss. To evaluate the overall usefulness of the two resonator designs their figure-of-merit as defined in the previous sections will now be evaluated.

$$K_{\tau_1} = Q(\sqrt{\eta}\tau_{\text{NTF},1} - 1) = 39(\sqrt{2}(0.8186) - 1) = 6.15 \quad (4.26)$$

$$K_{\tau_2} = Q(\sqrt{\eta}\tau_{\text{NTF},2} - 1) = 30(\sqrt{2}(0.8674) - 1) = 6.80 \quad (4.27)$$

It is seen that even though Type I resonator has 30% higher Q factor than Type II resonator, the figure-of-merit, K_{τ} , of the latter is higher than that of the former. Hence, the Type II resonator design is a better choice for the design of frequency-agile circuits. The new figure-of-merit introduced enables a straightforward evaluation of the inherent trade-off between tunability and Q factor of frequency-agile resonators. This is expected to be a useful tool in the design and evaluation of circuits and systems employing tunable elements. It should be noted that the figure-of-merit

applies equally well for all technologies as the definition is independent of the tuning mechanism. In the next section the experimental tuning data previously reported will be compared with another figure-of-merit referred to as the commutation quality factor (CQF).

4.2.8 Commutation Quality Factor (CQF) comparison

Vendik et al. have expanded on the pioneering work done by Kawakami on the figure of merit of a two state one-port network. Kawakami showed that a figure of merit can be defined for such a network and it is invariant under a lossless reciprocal transformation. Vendik defines the Commutation Quality Factor or CQF as the ratio of the input impedances of a lossless reciprocal two-port terminated in the impedance pair Z_1 and Z_2 , provided the imaginary part of both input impedances are zero. They have also demonstrated its invariance with respect to a lossless reciprocal transformation. The applicability of the CQF does not depend on the physical nature of the device and hence it can be applied to a wide variety of switchable or tunable microwave devices. Here the CQF as it applies to a semiconductor varactor and a ferroelectric varactor will be considered. The figure-of-merit for a tunable resonator as defined by Vendik in terms of CQF will now be discussed. The definitions of CQF for a ferroelectric and a semiconductor varactors is given by Equations (4.28) and (4.29) respectively [81].

$$K_{\text{ferro}} = \frac{(n - 1)^2}{n \times \tan \delta_1 \times \tan \delta_2} \quad (4.28)$$

$$K_{\text{Semi}} = \frac{\left(\frac{C_1}{C_2} - 1\right)^2}{(\omega C_1)^2 \times r_1 \times r_2} \quad (4.29)$$

For the ferroelectric varactor, n (which is equal to the η used in this work) is the tunability ratio given by C_1/C_2 and $\tan \delta_1$, $\tan \delta_2$ are the loss tangents in two states. In the case of a semiconductor varactor C_1 and C_2 are the two states of the tunable capacitor and r_1 , r_2 are the equivalent series resistance for the capacitor in two states.

This simplification is valid only when the parallel resistance of the varactor is of a very large value. The exact equations can be found in [81]. Vendik quotes 5000 and 10000 as the typical values for the CQF of the ferroelectric and the semiconductor varactors respectively. In our case the CQF of the Skyworks varactor, calculated at 2 GHz for a 1.33–0.66 pF change in capacitance was found to 2050.

In subsequent publications [82], Vendik defined the figure-of-merit of a tunable resonator using the CQF as a parameter, see Equation (4.30).

$$F = \frac{f_1 - f_2}{\Delta f} = 0.5\sqrt{K} \quad (4.30)$$

Here f_1 and f_2 are the resonant frequencies in two states. It is not clear from their published work as to what the exact definition of Δf is. They only mention that it is the pass-band width of the resonator. They have not reported any other work in which this figure-of-merit has been used explicitly or compared with measured data. It should also be pointed out that Vendik's work assumed a lumped element resonator while a distributed resonator has been discussed in this dissertation. For the sake of discussion the 1-dB and the 3-dB bandwidths of the resonators was used. The maximum shift in tuning is now given by $22.5\Delta f$. The value of K for the varactor used in our experiment was 2050. The 3-dB bandwidth of our resonator is in the range of 65–75 MHz. Using the lower value a maximum predicted frequency shift of 1462.5 MHz for a 1.33–0.66 pF change in capacitance was obtained. Clearly such a large frequency shift was not obtained. Frequency shift of 318 MHz in the case of an end-loaded resonator and a 469 MHz shift in the case of the split resonator was obtained. The typical 1-dB bandwidth of our resonator was found to be 30 MHz and this predicts a frequency shift of 675 MHz. This was also higher than the maximum frequency shift that was obtained. The CQF and the figure-of-merit introduced by Vendik does give an idea of the maximum tuning that case be attained for a given varactor and resonator system, in large part, by the virtue of the fact that it considers a one-port lossless transformation. While the limit itself is useful, there still is a requirement for a technique to design distributed resonators with optimized

tuning. This was introduced in the previous section.

4.2.9 Summary

Design techniques for choosing optimum capacitance and line lengths for end-loaded resonator which results in maximum tuning for a given capacitance ratio was presented. Further improvement in tunability can be obtained by optimally splitting the resonator and loading it with the varactor at an optimal distance from the shorted end. Design techniques for the same have also been presented. A network transformation factor (τ_{NTF}) was introduced to evaluate the frequency tuning ratio obtained from different tunable resonator networks with the same capacitance tuning ratio of the resonator. A figure-of-merit (K_{τ}) that helps guide the tunability and Q factor trade-off in the design of frequency-agile networks was also introduced in terms of the network transformation factor and the Q factor. Finally, the design and characterization of tunable resonators based on these two novel design ideas and a proof-of-concept was presented. A much higher tuning range was obtained at the expense of slight degradation in Q factor. This technique is expected to be very useful in the design of optimal frequency-agile circuits. In the next section a novel characterization technique for extracting the intrinsic insertion loss of symmetrical two-port networks will be introduced and verified.

4.3 Intrinsic Loss Extraction Technique

4.3.1 Introduction

In the evaluation of new microwave technologies it is desirable to obtain the intrinsic loss of devices, or as it will be referred to here, the DUT. The intrinsic loss of a two-port DUT is defined here as the insertion loss of the DUT with ideal lossless matching networks at each of the ports of the DUT. Thus all of the power delivered to Port 1 of the combined network either is delivered to the external Port 2

or it is dissipated in the DUT. This represents the lowest insertion loss of the device. Most importantly it enables technologies to be evaluated and their ultimate system impact to be determined prior to full subsystem design involving matching network realization. In the next section a procedure for determining the intrinsic loss of a symmetrical DUT is presented. The procedure, termed Intrinsic Loss Extraction (ILE) calibration, is a two-tier calibration scheme and relies on symmetrical fixturing so that the fixtures plus the symmetrical device is also a symmetrical network. The first tier of calibration, using standard SOLT calibration for example, calibrates the system to the planes of the fixtures. The second tier utilizes a through connection of the fixtures only. The measurement of the DUT plus fixtures directly leads to the intrinsic loss. The intrinsic loss is also compared here to the S-parameters of the device referred to the characteristic impedance of the line standard used in a full TRL calibration. The characteristic impedance of this line standard, particularly in new technologies cannot be estimated but this too is a measure of the fundamental characteristics of the device.

The evaluation of characteristic impedance is not feasible in certain cases due to insufficient knowledge of the material parameters or lack of analytic formula for a given structure. This is especially true in the case of a BST (Barium Strontium Titanate) device where the permittivity of the thin-film depends on the deposition temperature, pressure and also the annealing conditions. It has been mentioned in the literature that BST (Barium Strontium Titanate) thin-film microwave device needs to be well characterized [33, 85]. A TRL-based algorithm has been used by Lue [33]. It has also been pointed out in the past by Hoer [86, 87] that the TRL technique could be used to measure non-50 Ω devices in a 50 Ω environment. Using a more generalized mathematical theory it was shown in [88] that TRL inherently accounts for any differences in the characteristic impedance between the measurement system and the device under test.

The standard TRL technique [89, 90] was modified in order to mathematically obtain the true transmission characteristics of the device using only one line standard. The only requirement is that the characteristic impedance of the line standard being used should be the same as the device to be characterized. This can be done even

without knowing the characteristic impedance of the device under test and hence can be very useful for BST thin-film based devices and other new technologies.

4.3.2 Theory

The procedure for doing this is as follows: A first tier calibration using standard SOLT technique or any other calibration method is done. (In our case a 3.5 mm SOLT was performed). With reference to Figure 4.38, the thru line standard is measured, so that the measured cascade transfer parameters are:

$$[R_t] = [R_a][R_{Ta}][R_b][R_{Tb}] \quad (4.31)$$

$$[R_t] = [R_{Na}][R_{Nb}] \quad (4.32)$$

Here $[R]$ is the transfer matrix of the two port and the subscripts a, Ta, b, Tb refers to the transfer matrices of the error box and the impedance matching matrices at port 1 and 2 respectively. The transfer matrices with subscripts Na and Nb refer to the cascading of the error box and the impedance matching matrices at each port. The transfer matrix with subscript t corresponds to that measured for the thru line. The transfer matrix and the scattering matrix are related as follows:

$$[R] = \begin{bmatrix} \frac{-(S_{11}S_{22}-S_{12}S_{21})}{S_{21}} & \frac{S_{11}}{S_{21}} \\ \frac{-S_{22}}{S_{21}} & \frac{1}{S_{21}} \end{bmatrix} \quad (4.33)$$

Lastly the device under test is measured:

$$[R_{Dm}] = [R_a][R_{Ta}][R_D][R_b][R_{Tb}] \quad (4.34)$$

$$[R_{Dm}] = [R_{Na}][R_D][R_{Nb}] \quad (4.35)$$

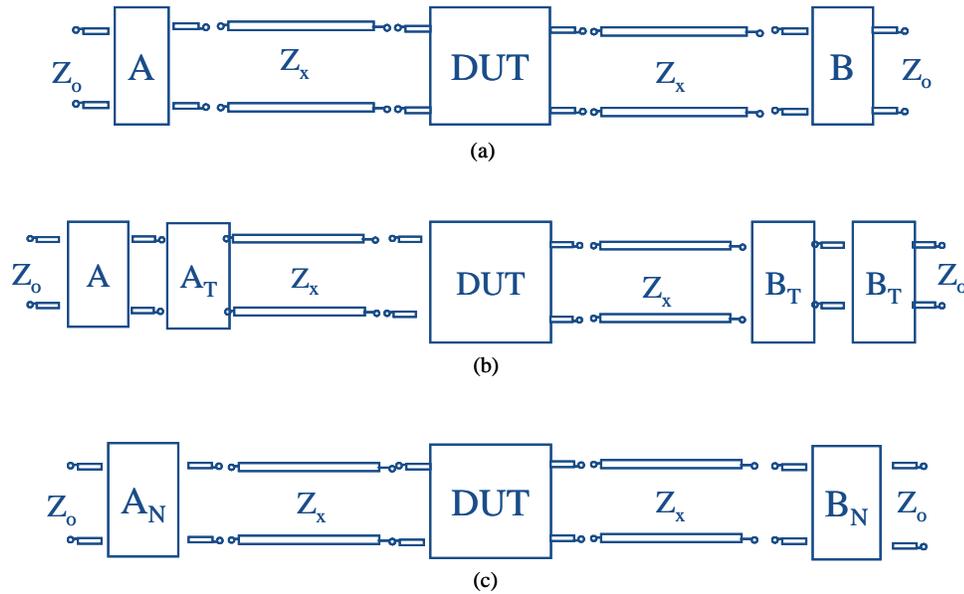


Figure 4.38: Through calibration procedure: (a) a device embedded in an unknown system; (b) introduction of matching networks to convert between Z_o and Z_x and (c) impedance networks and error boxes lumped together at the two ports.

Here the subscripts Dm and D refer to the transfer matrix of the device measured and the actual transfer matrix of the device with no reflection at its ports. Next it is assumed that:

$$[R_D] = \begin{pmatrix} 0 & S_{21,DUT} \\ S_{21,DUT} & 0 \end{pmatrix} \quad (4.36)$$

This is mathematically equivalent to having ideal impedance transforming networks at the input and output port of the device under test. It was further assumed that the device under test is symmetrical. Hereafter, the solution follows the algorithm outlined in [89, 90] and yields the value of $S_{21,DUT}$. This is the true insertion characteristics of the device with no reflections at its ports. This procedure is outlined in Figure 4.38.

4.3.3 Design and implementation

As a proof of concept an edge-coupled microstrip bandpass filter (Figure 4.39(a)) on a Gilam 2032 board with 75Ω input and output impedance was fabricated and measured on a HP 8510 C Network Analyzer. The filter was designed using the SFILTER synthesis tool from Eagleware and the EM simulation was done in Momentum ADS. The filter was de-embedded using the TRL algorithm. TRL standards namely a 75Ω through, 75Ω line and an open were also fabricated on the same substrate (Figure 4.39(b)). The actual length of the through was used to properly position the reference plane. The filter and the thru line were also measured after a first tier 3.5 mm SOLT (short-open-load-thru) calibration.

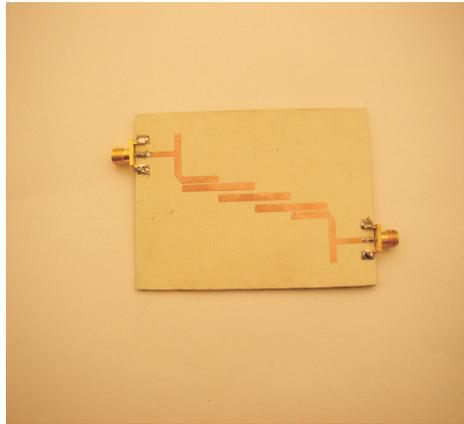
4.3.4 Measured results

The measured data for the filter and the through line after a first tier calibration were processed off-line using the steps outlined above to obtain the intrinsic transmission characteristics of the device. A full TRL calibration was also implemented on the HP 8510C system. The results are compared in Figure 4.40.

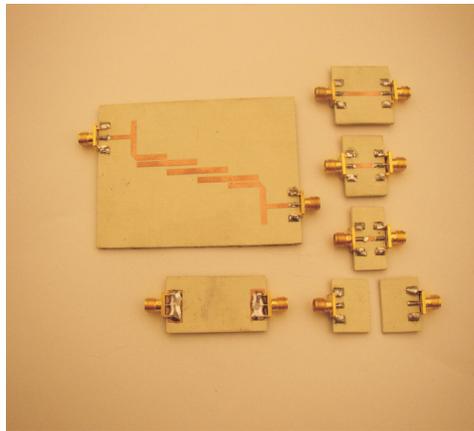
The intrinsic loss of a device determined using the ILE procedure determines the transmission loss solely due to the device. The results can be interpreted as follows. The ideal matching networks effectively placed at Port 1 of the DUT serves to deliver all of the power inserted at the external Port 1. This power is either dissipated in the DUT or it emerges at the external Port 2. The loss plotted in Figure 4.40 is the loss in the DUT alone and is the best that can be achieved. An expanded plot is shown in Figure 4.41. This can be contrasted to an alternative measure of device loss:

$$|S_{11}|^2 + |S_{21}|^2$$

which is shown in Figure 4.42. Here the S-parameters are obtained using conventional TRL calibration and the device S-parameters are referred to the characteristic impedance of the line standard. The impedance transforming network inherent in the TRL deembedding procedure is not a matching network. Thus power that enters the



(a)



(b)

Figure 4.39: Experimental fixtures: (a) $75\ \Omega$ bandpass filter; (b) TRL/characterization kit

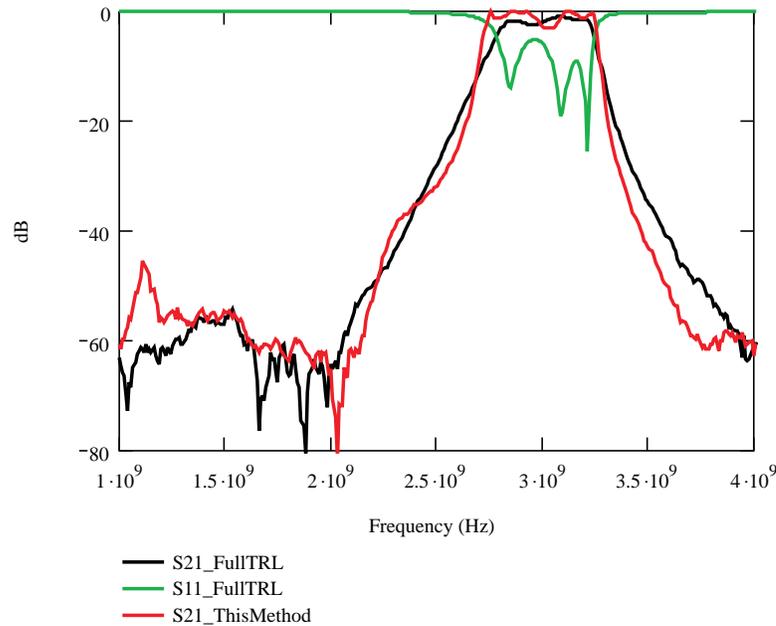


Figure 4.40: Comparison of symmetrical filter characteristics using a full TRL algorithm and the method outlined in this work.

external Port 1 is delivered to the load but power reflecting from the internal Port 1 reflects from the fixture and enters the device again.

A further observation can be made about these results. The filter tested here is a fifth-order filter so that there are five resonators with the resonant frequencies approximately uniformly spaced in the passband of the filter. At resonance there is higher loss than at other frequencies as currents and fields peak leading to higher losses such as I^2R losses. This can clearly be seen in Figure 4.41 where the intrinsic loss between resonances reduces to virtually zero. The association of losses with resonance cannot be observed using the standard S-parameter extraction. A magnitude only plot of the loss parameter is shown in Figure 4.43.

4.3.5 Summary

A simple and straightforward method of characterizing the intrinsic insertion loss characteristics of a symmetrical two port network has been presented. As way of

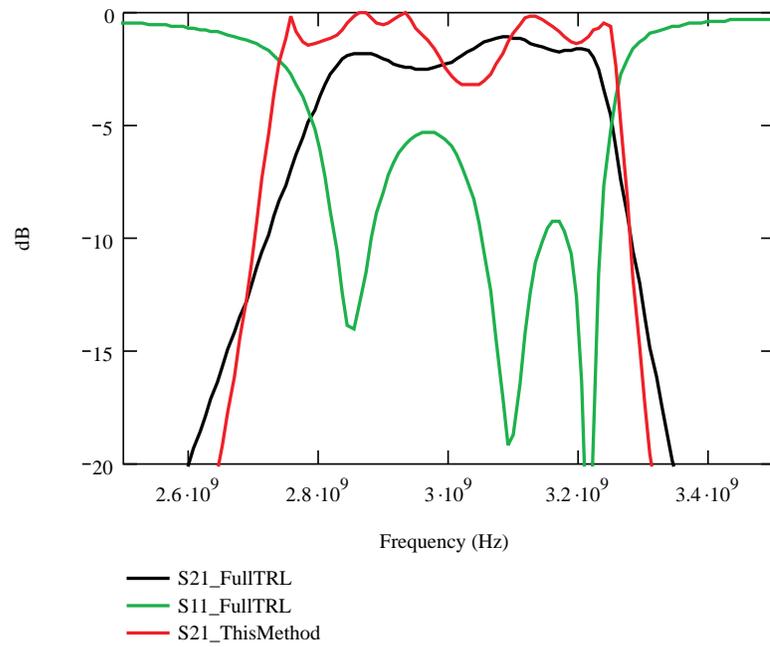


Figure 4.41: Comparison of symmetrical filter characteristics using a full TRL algorithm and the method outlined in this work, zoom-in plot

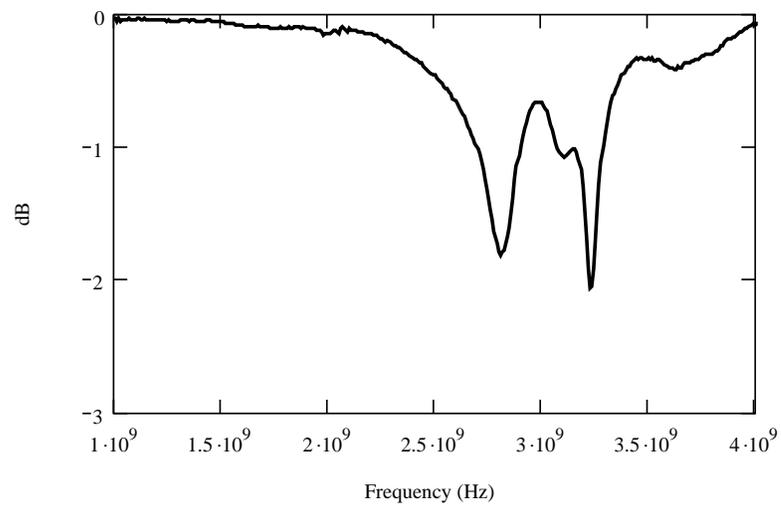


Figure 4.42: Plot of loss parameter (in dB) obtained from TRL.

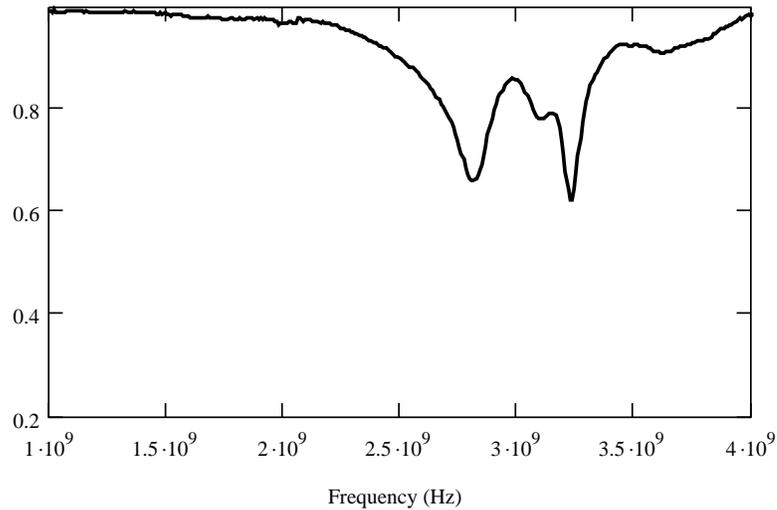


Figure 4.43: Plot of loss parameter (magnitude) obtained from TRL.

demonstration a symmetrical filter was measured and characterized using this technique. This technique enables a straightforward method of characterizing the intrinsic loss of symmetrical two port networks. This is very useful at the technology development stage or for materials and systems with unknown characteristics. The technique could also be extended to a general or asymmetric networks if additional measurements are made.

4.4 Conclusion

This chapter presented two novel techniques for the design of tunable resonators with optimized frequency shift and a acceptable trade-off between Q factor and tuning. Design equation and curves were presented. A network transformation factor (τ_{NTF}) was introduced and a figure-of-merit (K_{τ}) that helps guide the tunability and Q factor trade-off in the design of frequency-agile networks was also introduced in terms of the network transformation factor and Q factor. Experimental verification using a semiconductor varactor and microstrip resonators on FR4 substrate were also described. A novel characterization technique for extraction of intrinsic loss in sym-

metrical two-port networks was also presented. In the following chapter frequency-agile RF filters using integrated BST thin-film interdigital varactors on sapphire and alumina will be presented.

Chapter 5

Tunable Filter using Integrated BST Thin-Film Varactors

5.1 Introduction

Tunable filters have been widely investigated for multi-functional, multi-band RF and microwave devices. The use of tunable filters leads to greater functionality, better channel selectivity, reduced size and weight since the same hardware can be employed at multiple bands. Over the years many technologies have been considered as potential candidates for the implementation of tunable filters and other frequency-agile components. Mechanically tunable filters using plungers or mechanical varactors have been used for many decades [91, 92, 93, 94]. However, they are usually bulky and have slow tuning speed. Even though they offer large power handling capability and are low loss, the size and weight constraints limit their application to very specific systems. More recently a microscopic incarnation of the mechanically tunable filters have been investigated in the form of MEMS (microelectromechanical system) [95] varactor based tunable filters. MEMS based filters [96, 97] are very attractive from a

small size and low insertion loss perspective. However, they have stringent packaging requirements and usually suffer from reliability issues. Furthermore their tuning speed (usually of the order of microseconds) and power handling capabilities are limited. Another varactor technology that has been used for tunable filters is the reverse biased semiconductor varactor. Semiconductor varactor [98, 99] based tunable filter have been implemented by many researchers but they usually have high insertion loss and poor linearity performance. This is mainly due to their low Q factor above a few GHz.

The use of BST thin-film varactor for tunable filters [40, 100, 42, 101, 102] has been discussed in Chapter 2. The properties of BST thin-film interdigital varactor was previously described in Chapter 3. BST is a scalable low-cost material which can be fabricated using standard manufacturing processes and also offers the ease of integration with a variety of substrates. The packaging requirements for BST devices are also compatible with those of existing systems and devices. Furthermore BST varactors can reliably handle high power [70] and also offer switching speed in the nano-second range. BST varactor based tunable filters reported in the literature have been typically designed with discrete varactors. These realizations utilized parallel-plate varactors and yielded insertion loss in the range of 4–7 dB [26, 46, 47] with a center frequency of 1–2 GHz. Not much work has been done in the area of BST thin-film interdigital varactor based tunable filters at room temperature. In this chapter a room temperature implementation of a BST thin-film interdigital varactor based third-order tunable combline bandpass filter will be presented. A single layer lithography on sapphire and alumina and copper metallization has been used. The fabrication and design details, measurement results and nonlinear characterization of the filters are also discussed.

5.2 Tunable bandpass filter on sapphire

5.2.1 Introduction

Measured data for two filters are presented, one with $0.5\ \mu\text{m}$ of sputtered copper (F1) and one with $1\ \mu\text{m}$ of evaporated copper (F2). The filter F1 is centered at 2.6 GHz, has a tuning range of 16 %, and has an insertion loss between 6.7 dB and 8.3 dB across the range. The filter F2 had similar center frequency and tuning range but showed much lower insertion loss. The zero bias loss was 5.1 dB and this reduced to 3.3 dB at high bias. This is made possible using low-loss BST material in a gap capacitor topology to obtain appropriate capacitance values. These filters require tuning voltages in the range of 100–200 V compared to filters with parallel-plate designs requiring a voltage tuning of 0–30 V.

5.2.2 Filter fabrication

Various techniques that have been used so far for BST thin-film fabrication are RF sputtering, metal organic chemical vapor deposition (MOCVD), pulsed laser deposition (PLD), and sol gel processing. Single crystalline sapphire was used as a substrate for deposition of BST thin-film by RF sputtering. Sapphire has attractive microwave properties such as low loss tangent ($\tan\delta = 0.0001$) at microwave frequencies and high dielectric strength. The coefficient of thermal expansion (CTE ~ 8.4 ppm) of sapphire is very close to that of BST (CTE ~ 9 ppm) and hence high temperature annealing is possible without cracking the BST thin-films. In Chapter 3 the factors that need to be considered while selecting the metallization scheme were discussed. Noble metals such as Pt, Au, or Ir have been typically used as electrodes in thin-film oxide based devices because they are in most cases non-reactive upon contact with oxides and their large work functions provide Schottky contacts. However due to the high resistance values of Pt and Ir, multiple micron layer electrode thicknesses are necessary for achieving acceptable low ESR (Equivalent Series Resistance) of the device. Instead, copper was chosen as the top electrode metal in our work since it

is easily available, provides the highest conductivity of any base metal and can be etched by standard techniques. A step by step process flow for the fabrication process is shown in Figure 5.1.

A radio frequency magnetron sputtering technique was used to deposit thin-film $\text{Ba}_{0.75}\text{Sr}_{0.25}\text{TiO}_3$ on polished single crystalline c-plane sapphire substrates (Commercial Crystal Labs. Inc, FL). A BST composition of 75/25 ratio of Ba/Sr was chosen for optimum balance between dielectric tunability and loss tangent. The substrates were 10 mm x 10 mm in size and 500 μm in thickness. Sputtering was done off axis at an angle of 30° in an argon/oxygen mixture ($\text{Ar}:\text{O}_2 = 5:1$) to obtain optimal stoichiometry and uniform film thickness. However the gun normal pointed at the center of the substrate despite the 30 degree incident angle. A 4 inch diameter stoichiometric ceramic BST target (Super Conductor Materials Inc., NY) was used and sputtering pressure of 10 mtorr was maintained. Deposition temperature was maintained at 300 $^\circ\text{C}$. Deposition was done for 60 minutes to obtain 0.6 μm thick BST film. After deposition the film was annealed at 900 $^\circ\text{C}$ in air for 20 hours to obtain fully dense and crystalline BST thin-film on sapphire substrate. Standard photolithography and metal lift-off process was used to define the fingers of the interdigital varactor and the feed electrodes. A lift-off process was used since it utilizes benign chemicals which do not harm the BST. This is in contrast to an etch-back process where potentially harmful acids are used. Positive imaging photoresist Shipley 1813 and Microchem LOR 5A was used to deposit a thick bilayer photoresist stack for lift-off. After standard UV exposure and development of the photoresist the sample was ready for metallization. First a thin layer of chromium (0.03 μm) was sputtered and this followed by deposition of 0.5–1.0 μm copper, either by sputtering or by thermal evaporation. Finally, lift-off was done in Microchem Remover PG solution to define the interdigital fingers. A series of interdigital capacitors (see Figure 5.2) were fabricated in this manner and characterized using an impedance analyzer.

A representative tuning curve of the BST varactor is shown in Figure 5.3. The varactor shows a 12% tuning with an applied bias of 35 V at 1 MHz. The finger spacing was 5 μm and hence a tuning field of 70 kV/cm across adjacent fingers. This of course assumes that the total applied field goes through the BST but in reality

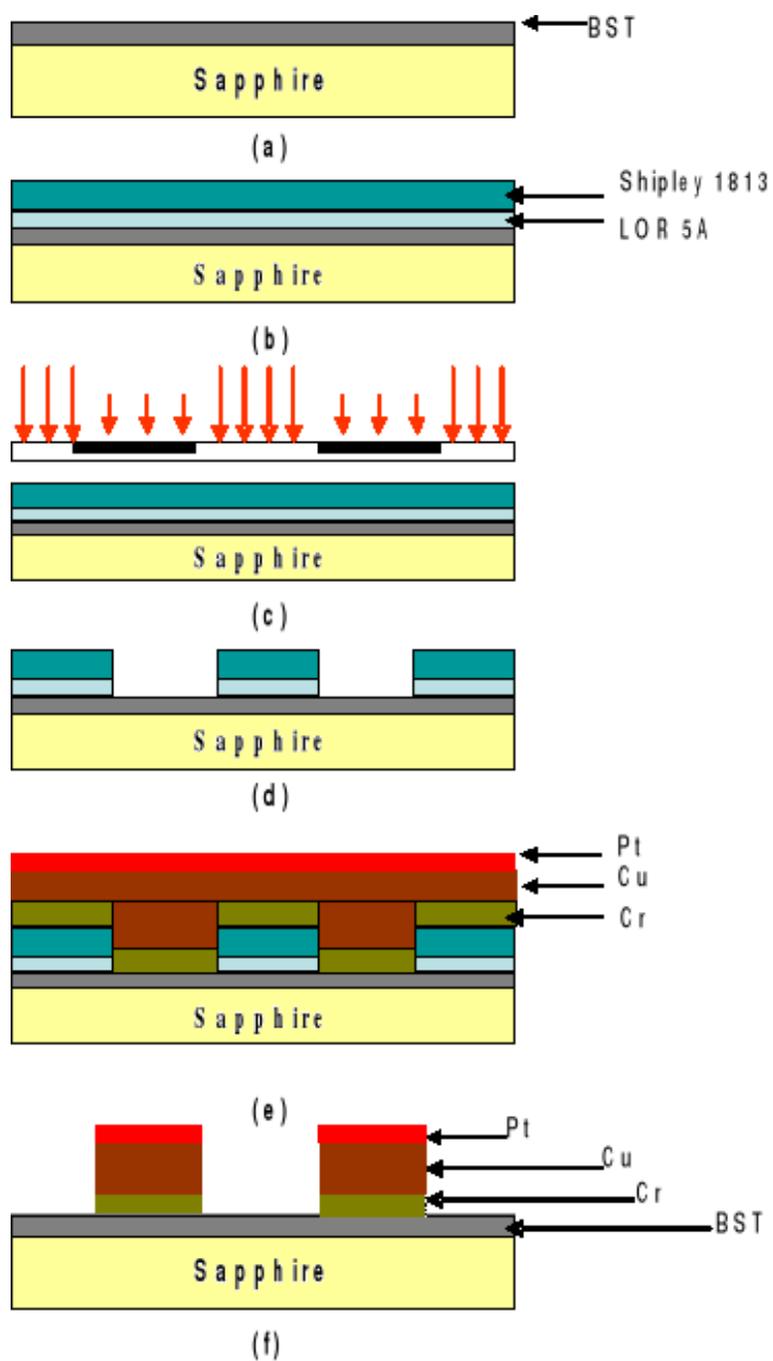


Figure 5.1: Process flow for BST interdigital varactor fabrication (a) deposition of BST thin-film by sputtering. (b) positive imaging resist and lift-off resist deposition. (c) UV exposure. (d) resist development (e) Cr and Cu deposition. (f) patterning of top-metal by lift-off.

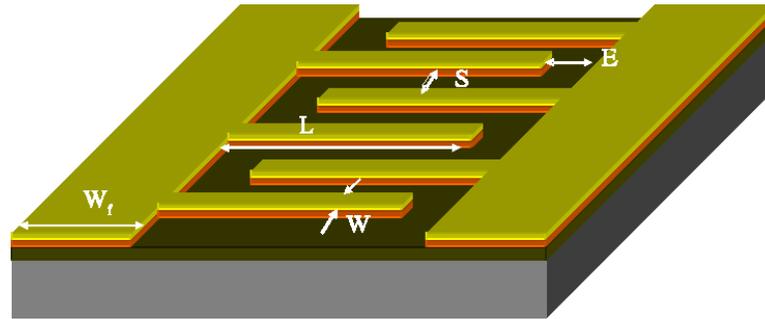


Figure 5.2: Schematic of the BST interdigital varactor.

some of the electric field is in air. Hence this is a worst case calculation and gives a fair idea of the tunability of the BST film. The Q factor of varactor was found to be 100 at zero volt bias and this increased to a value of 250 at 35 V bias, all at 1 MHz.

The BST interdigital varactors (IDCs) were used to design tunable combline band-pass filters (see Figure 5.4). A 3rd order topology was chosen and the effect of changing the loading capacitors was analyzed.

5.2.3 Filter design

The initial filter synthesis was done using the MFilter tool in GENESYS [103] suite offered by Eagleware. After the initial synthesis, the filter parameters, namely the width, length, spacing and the loading capacitance were optimized to meet the specifications. The initial synthesis yielded loading capacitance values with less than 5% difference. Since it is difficult to maintain such precise tolerances in capacitance values, it was decided that all loading tolerances be made equal so that any tolerance would simply result in the shift of the frequency of operation and not affect the filter characteristics drastically. This is much easier from a fabrication point of view. One of the requirements of the design was to make the final design exactly fit a 10 mm x 10 mm piece of c -plane sapphire substrate. This is necessary since a “ground-wrapping” technique was used for making ground connections at the end of the resonators and the loading capacitors. Such a process enabled us to fabricate the filter using a single-step

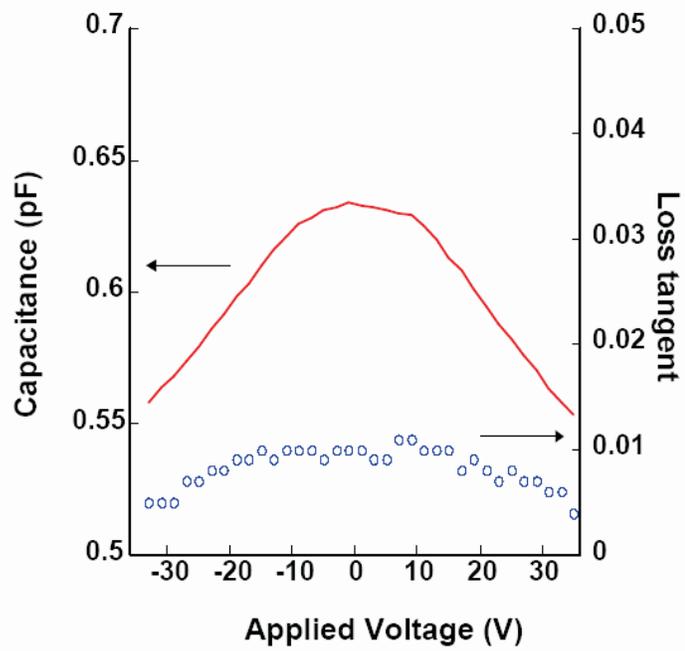


Figure 5.3: A representative tuning curve of the BST interdigital varactor ($W = 5 \mu\text{m}$, $S = 5 \mu\text{m}$, $E = 5 \mu\text{m}$, $L = 200 \mu\text{m}$, $W_f = 50 \mu\text{m}$, No. of fingers = 12) at 1 MHz.

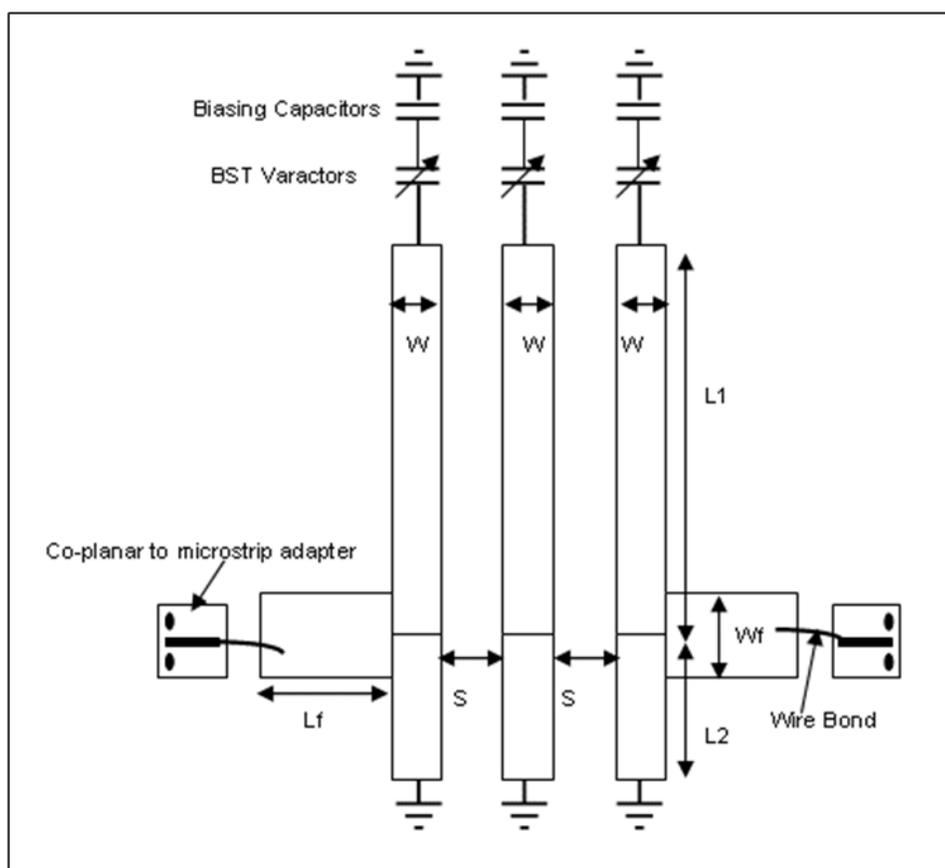


Figure 5.4: Schematic of the tunable combline bandpass filter.

and inexpensive lithography process with no vias. Therefore, the design was tweaked and optimized so that the end of the filter (including the biasing network) touched the edge of the substrate. The filter parameters were found to be as follows: $W = 235 \mu\text{m}$, $S = 235 \mu\text{m}$, $L_1 = 4500 \mu\text{m}$, $L_2 = 3000 \mu\text{m}$, $L_f = 4377.5 \mu\text{m}$, and $W_f = 430 \mu\text{m}$.

The filter had a center frequency of 2.4 GHz with a 3 dB bandwidth of 500 MHz. The nominal electrical length of the resonators was 58° at the center frequency and the impedance was 69Ω . The biasing network consisting of three 1.0 nF DC blocking capacitors rated to 200 V were added to the design in series with the tuning capacitors. These capacitors provided DC contact points for applying bias to the BST varactors while at the same time presenting short to the RF signal. The capacitance values were found to be 0.6 pF for the required length and the frequency of operation. Using a combination of formulae available in the literature [80] for calculating the capacitance of the multi-layered IDCs and our own prior work on BST-based IDC varactors [69], the length, $L = 200 \mu\text{m}$, width, $W = 5 \mu\text{m}$, spacing, $S = 5 \mu\text{m}$ and the number of fingers, $N = 12$ for the IDCs was determined. An empirical formula derived using measurement data for different capacitor configurations perviously discussed in Chapter 3 was used in conjunction with the analytic formula derived by Gevorgian *et al.* [80] using a conformal mapping technique.

After the design, fabrication was undertaken using the process flow described in the previous section. Additional steps were required to deposit metal on the back side of the sapphire substrate for grounding. This was done in a manner similar to the metallization on the top. First a thin layer of Cr ($0.03 \mu\text{m}$) was deposited by sputtering, followed by $1 \mu\text{m}$ of copper, deposited using either by sputtering or thermal evaporator. Filters using both sputtered and evaporated copper metallization will be described in this chapter. It will be shown that evaporated copper has almost twice the conductivity of sputtered copper even when using optimized sputtering conditions. A thin capping layer of Pt ($0.03 \mu\text{m}$) was deposited on the top to prevent the ambient oxidation of copper and also to improve the wire bonding of the gold wire to the feed lines. The final stack up of the layers is shown in Figure 5.5. The filter was then conveniently assembled on a Rogers high frequency laminate using conductive

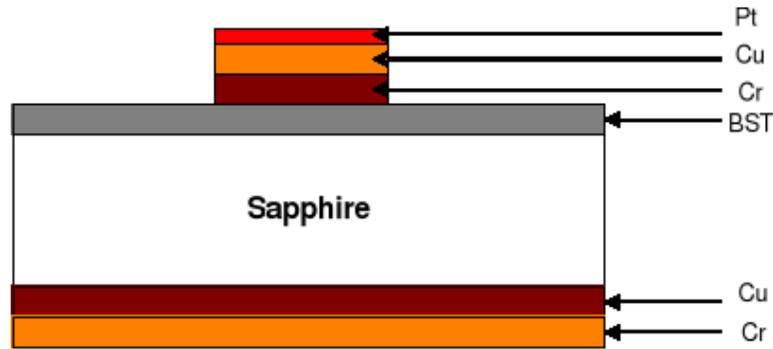


Figure 5.5: Layer stack-up of the bandpass filter.

epoxy which also served as the common ground plane. The biasing capacitors were then attached to the biasing network and the ground connections were made by using conductive epoxy and wrapping it over the edge of the substrate.

The input and output of the filter was then connected to J Micro Technologies [104] CPW-to-Microstrip adapter using gold wire bonds (Figure 5.6). This enables the use of air co-planar probes for the measurement and characterization of the filter. The assembled bandpass filter is shown in Figure 5.7(a). At each stage of assembly the integrity of the contacts was carefully monitored.

Two bandpass filters (F1 and F2) using different metallization techniques were fabricated. The first filter (F1) was fabricated using $0.5 \mu\text{m}$ of sputtered copper [105]. The second filter (F2) was fabricated using $1.0 \mu\text{m}$ of evaporated copper [72]. It was found that the resistivity of copper using the sputtering method was two times higher than that of base metal and this contributed significantly to the insertion loss of the filter. Hence, it decided that evaporated copper which was optimized to have approximately 1.2 times the resistivity of base metal should be used. Furthermore, the thickness was increased from $0.5 \mu\text{m}$ to $1.0 \mu\text{m}$ and this resulted in a considerable reduction in the insertion loss of the filter. The results are presented in the next section.

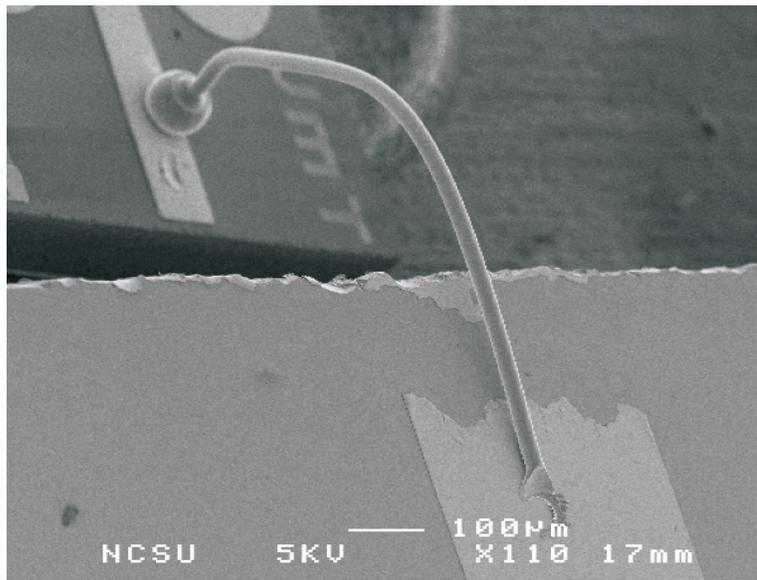
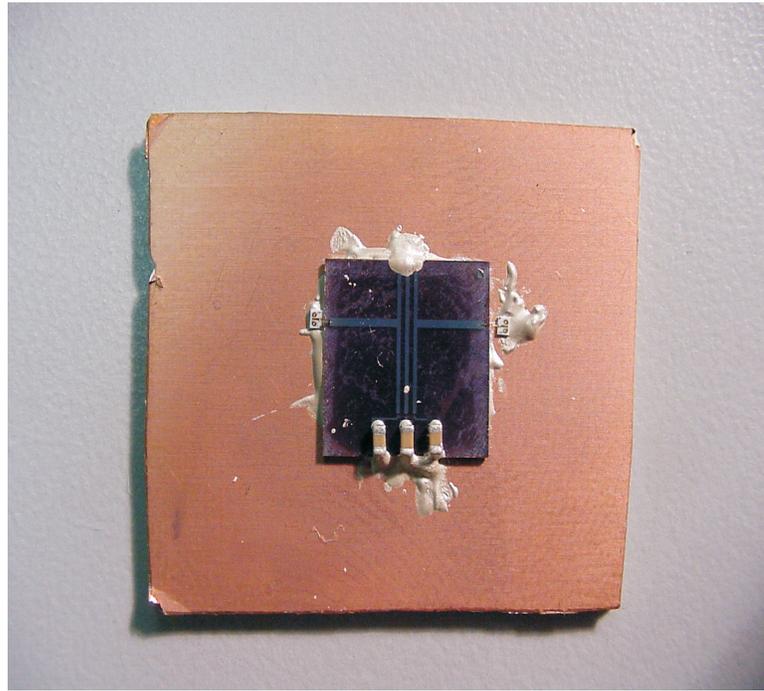


Figure 5.6: SEM photograph of wire-bond to the CPW-to-Microstrip adapter.

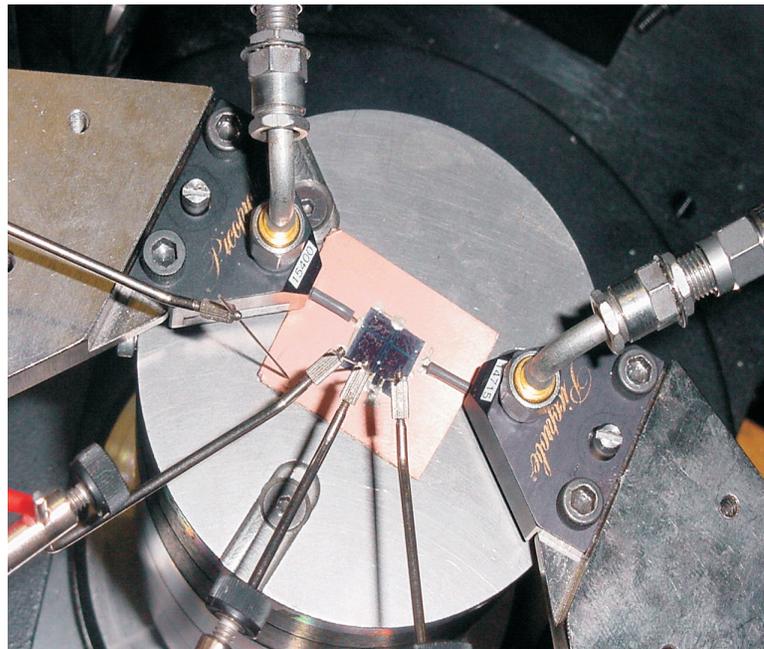
5.2.4 Measured results

The filters were measured on a HP 8510C network analyzer using a Cascade Microtech [106] Model 42 Microwave R&D probe station. A $150\ \mu\text{m}$ GSG (ground-signal-ground) probe from GGB Industries was used for measurement. A two port LRM (line-reflect-match) calibration was performed using a CS-5 calibration substrate and appropriate calibration coefficients. The reference plane was established at the end of the probe tips. It should be noted that the Coplanar-to-Microstrip probes were not de-embedded from the measurements. This does not introduce any appreciable error and the additional losses are minimal and expected to be in the range of 0.2 dB. The bias was applied using DC probes and a HP 4142 B parameter analyzer (see Figure 5.7(b)). The bias was varied up to 180 V and the S-parameter was recorded at each bias point. The insertion loss and the return loss of the filter F1 are presented in Figures 5.8 and 5.9 respectively.

The filter was centered at 2.44 GHz and had a zero bias insertion loss of 8.3 dB. The center frequency was tuned by 16% to 2.88 GHz by the application of 180 V bias. The insertion loss at the high bias state decreased to 6.7 dB. This was due to



(a)



(b)

Figure 5.7: Combline bandpass filter: (a) assembled bandpass filter; and (b) filter under test.

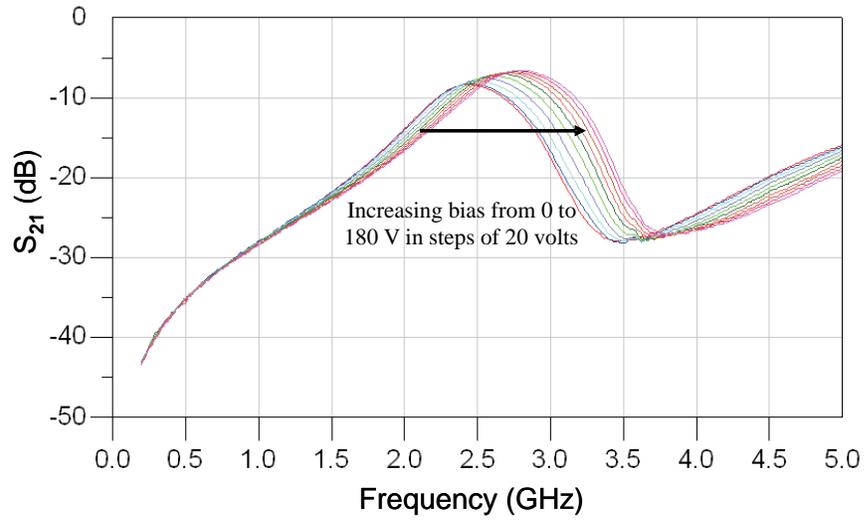


Figure 5.8: S_{21} versus bias for filter F1.

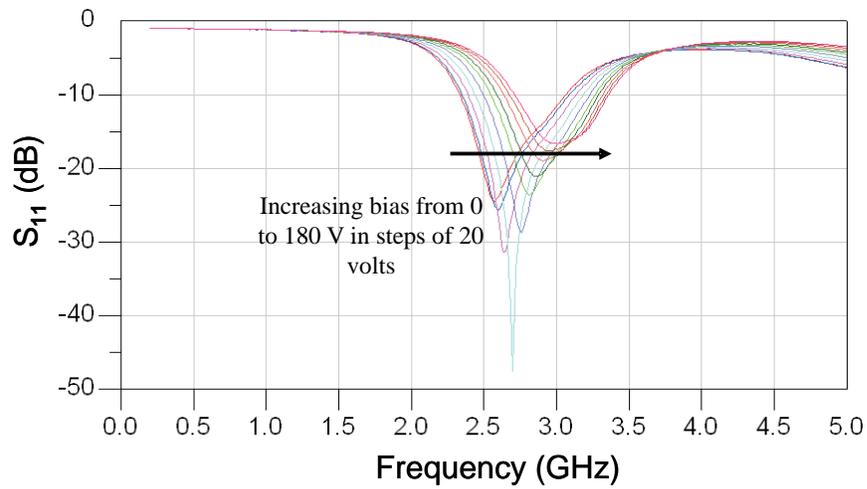


Figure 5.9: S_{11} versus bias for filter F1.

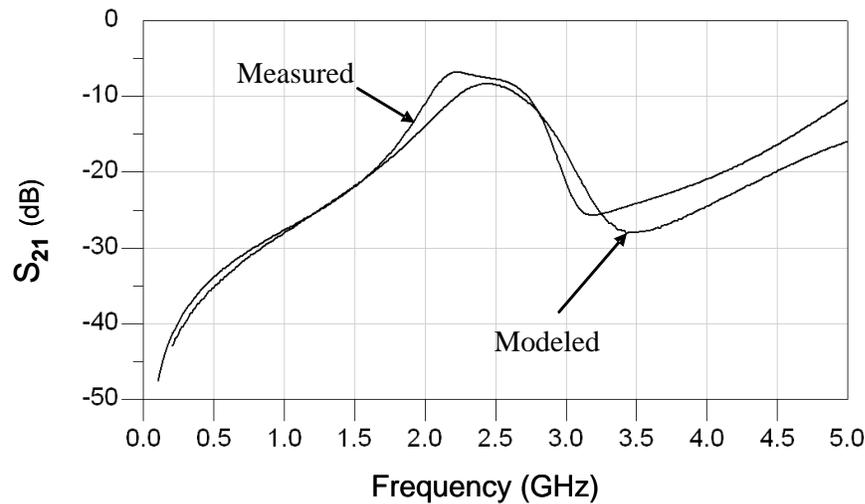


Figure 5.10: Comparison of measured and simulated S_{21} at zero bias for filter F1.

the higher Q factor of the BST interdigital varactors at high bias voltages (see Figure 5.3). The return loss was better than 17 dB at all bias voltages. A comparison of the measured and simulated insertion loss plot at zero bias is presented in Figure 5.10.

The measured data closely agrees with the simulated results in ADS [107] and the slight discrepancy the high end of the frequency range can be attributed to unaccounted parasitic inductances and capacitances. The model used for comparison includes the effect of parasitic resistances due to the use of conductive epoxy for grounding and also the lower conductivity of sputtered copper. The parasitic values were obtained from DC resistance measurements and the conductivity of copper was obtained from four point probe measurements. The rather high insertion loss of the filter F1 is primarily due limited thickness of the metal and also due to the higher resistivity of sputtered copper. The skin depth of copper at the frequency of operation of the filter is $1.34 \mu\text{m}$ and hence there is considerable room for improvement in the insertion loss.

Towards that end, the filter F2 was fabricated with $1.0 \mu\text{m}$ of copper. To further improve the insertion loss a new filter F2 was fabricated using evaporated copper which has much lower resistivity than sputtered copper. The measured insertion loss

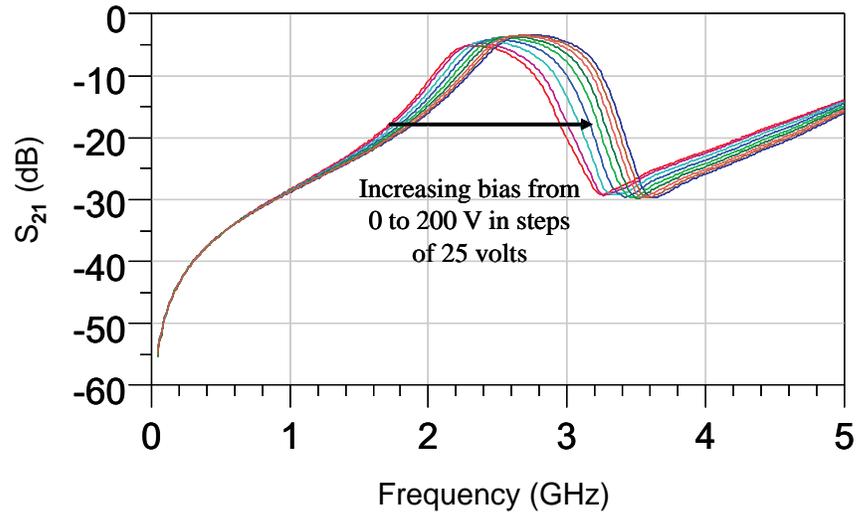


Figure 5.11: S_{21} versus bias for filter F2.

and return loss results for filter F2 are presented in Figures 5.11 and 5.12 respectively. A comparison of measured and modelled data at the high and low end of the bias range is shown in Figure 5.13

The filter F2 was also centered at 2.44 GHz with a minimum zero bias insertion loss of 5.1 dB. This is an improvement of over 3 dB compared to filter F1. Clearly the metal thickness and the resistivity have a tremendous impact on the insertion loss of the filter. The filter was tuned to 2.88 GHz (16% tuning) by the application of 200 V bias and the minimum insertion loss further reduced to 3.3 dB. This was in part due to improved matching and also in part due to higher Q factor of the BST varactors at high bias voltages. The return loss was better than 13 dB for all bias voltages. This result demonstrates the potential of BST thin-film interdigital varactor technology for tunable filter applications. It should be noted that the metal thickness is still less than the skin depth at the frequency of operation and hence there is more room for improvement. The use of a via process and elimination of wirebonds at the input and output of the filter should enable further reduction in the insertion loss. Such a filter is described in the next section. The current drawn by the BST varactor with bias was also recorded to estimate the total power consumption in the filter. The data is

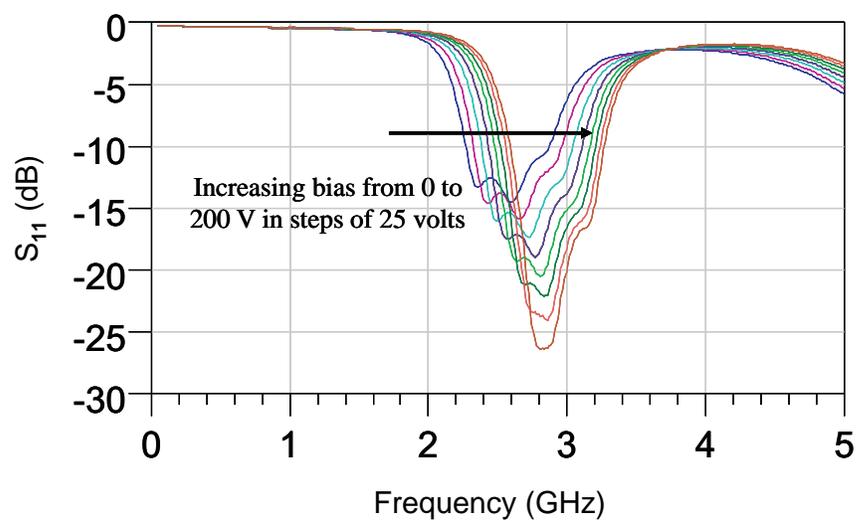
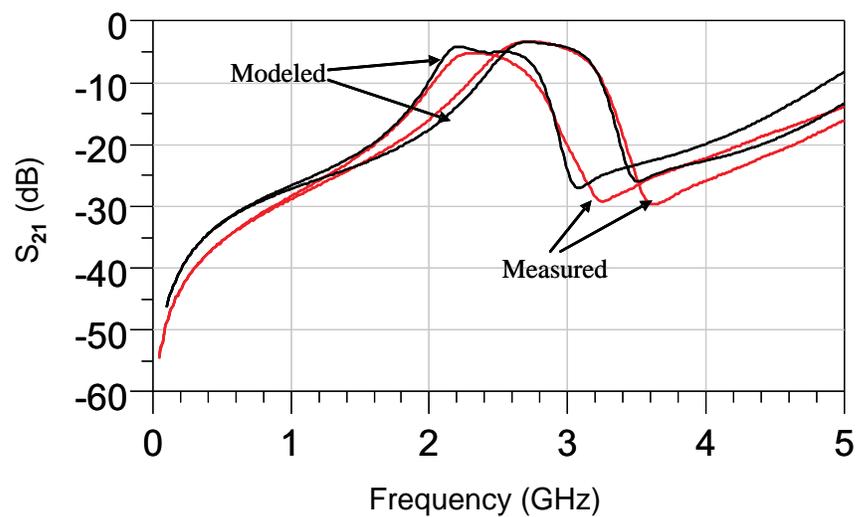
Figure 5.12: S_{11} versus bias for filter F2.

Figure 5.13: Comparison of measured and modelled data at zero bias.

Table 5.1: Total leakage current for the filter versus bias voltage

Bias(V)	Current(nA)
25	22.68
75	48.87
125	66.20
175	67.54

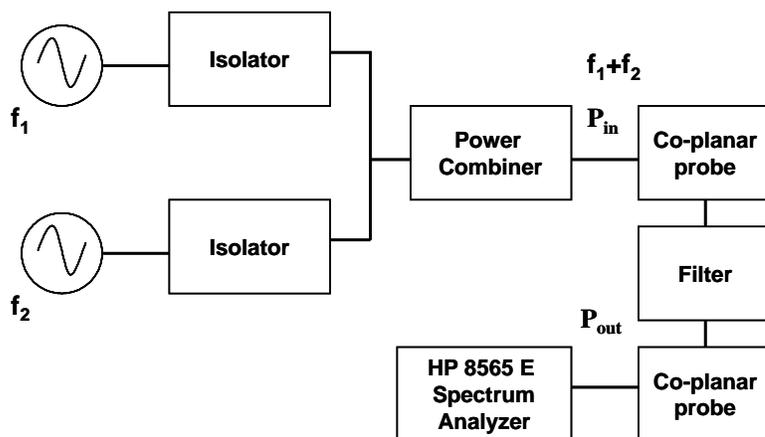


Figure 5.14: Experimental setup for intermodulation measurements.

shown in Table 5.1. The current recorded was the total DC current for the all three BST capacitors and hence total DC power dissipated in the filter was approximately $12 \mu\text{W}$ over the tuning range.

The tunable filters were also characterized for their linearity performance using a two-tone intermodulation test. For transmitter application the intermodulation generated by the non-linearity of the filter should be suppressed to allow the use of high power signals [108]. The third-order intermodulation (IM3) distortion is of great concern since it can potentially produce spurious signals within the pass band of the filters and can have an adverse effect on system performance [109]. A widely used measure of non-linearity is the third-order intercept point (IIP3), which is defined as the input power at which the output power of the fundamental tone and the IM3 products are equal.

The experimental setup for measuring the IIP3 is shown in Figure 5.14. Two tones

separated by 10 MHz were used for the intermodulation test. The two tones were centered at 2.35 GHz and 2.36 GHz respectively. Isolators were used in both paths to prevent the reflection of signals back to the signal generators which could potentially create additional distortion products. First the intermodulation product of the setup was measured and the input attenuation on the spectrum analyzer was set to 30 dB so that the IM3 products created by the setup are negligible and near the noise floor of the analyzer. This prevents the intermodulation products generated by the setup from impacting the intermodulation measurement of the device under test. The signal strength of the sources was adjusted to equalize the input power of the two tones at the input of the filter. This was necessary since the amplitude response of the isolator and the power combiner was not constant with frequency. The output power of the fundamental tones and the IM3 products was recorded using a spectrum analyzer as the input power was swept from -7.7 dBm to + 6.3 dBm. The input power was swept in steps of 2 dBm and the output power of the fundamental tone increased by the same amount. The output power of the IM3 products increased by three times or 6 dBm for every 2 dBm increase in the input power. This clearly follows the expected 1:1 and 3:1 slope for the fundamental tone and the IM3 products respectively (see Figure 5.15). The measured data was then extrapolated using a straight line fit for the extraction of IIP3. The IIP3 of the filter was found to be +41 dBm. The IIP3 value of the tunable filter is comparable to or better than the IIP3 performance of commercially available tunable bandpass filters based on semiconductor varactor diodes.

5.2.5 Summary

A room temperature tunable combline bandpass filter using a BST thin-film interdigital varactor and a new metallization scheme has been presented. The new bandpass filter achieved 16% tunability upon the application of 200 V bias. The insertion loss of the filter was reduced from 8.3 dB to 5.1 dB at zero bias and from 6.7 dB to 3.3 dB at high bias state by using thicker metallization and evaporated copper. Intermodulation test of the filter showed an IIP3 of +41 dBm. The tuning

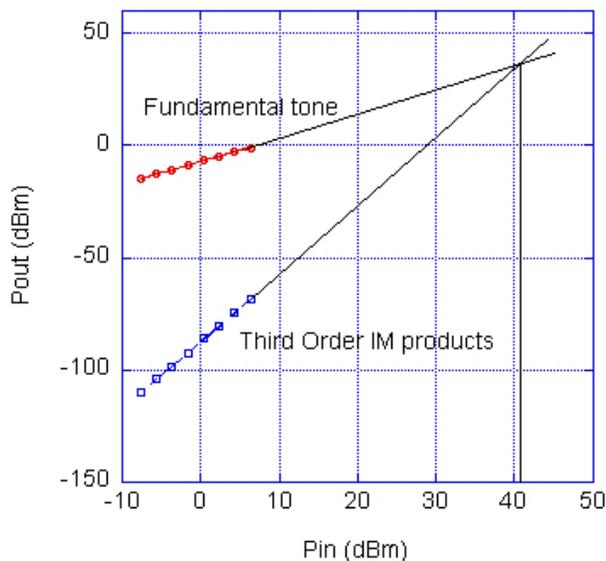


Figure 5.15: Measured intermodulation data for the tunable filter F2.

characteristics, insertion loss and the IIP3 of the filter can be further improved by process and design optimization. For instance, the use of vias and integration of the filter in a package or on a chip with other components will eliminate the wire bonds and further improve the insertion loss. These results are very encouraging and it is expected that BST thin-film will be widely used in the design of tunable microwave filters and other frequency-agile devices. In the next section an integrated bandpass filter on alumina will be presented.

5.3 Tunable bandpass filter on alumina

5.3.1 Introduction

BST-based tunable filters have been typically fabricated on single crystal substrates since high quality BST films can be epitaxially grown on such substrates at high temperatures. However, they are expensive and not widely used in the mi-

crowave industry. The objective, therefore, was to develop a low-cost tunable filter using a single-step fabrication process. A room temperature implementation of a voltage-tunable planar combline filter using thin-film BST interdigital varactor on polycrystalline alumina and copper metallization was developed. The advantages of alumina have been discussed in Chapter 3. In the previous chapter a tunable bandpass filter was presented on sapphire. In this chapter similar tunable filter design and characterization will be presented on alumina and their properties would be compared.

5.3.2 Tunable filter design

Tunable filters using BST thin-film varactors can be implemented in various topologies. There are essentially two choices for each topology: a lumped element circuit or a distributed implementation. A distributed approach was taken in the implementation of BST varactor based bandpass filter in LTCC technology [48]. This can be contrasted with the lumped element approach where the BST thin-film varactor is used in discrete form and wire bonded to other lumped components [46], or co-fabricated with inductors. The latter implementation is usually limited by the low Q factor of the inductors available in an integrated manufacturing process or in SMT form. However, it should be mentioned, that the lumped element approach offers a size advantage at the low microwave frequencies since the resonator length at such frequencies is of the order of a few centimeters. A distributed element approach was chosen for the work presented here since it allows the integration of the BST varactor in the circuit in the same fabrication step; this improves the Q factor by minimizing the series resistance. A third-order combline bandpass filter was designed with a center frequency of 1.75 GHz and a 3 dB passband equal to 20% of the center frequency. The filter was designed using the MFilter synthesis tool in the GENESYS suite from Eagleware. The initial design was then tweaked and optimized for manufacturability. The capacitive loadings at the end of the resonators were changed to be equal since a tolerance of the order of a few tens of femtofarads is difficult to achieve. Furthermore, all widths and spacing were made equal and this resulted in a physically symmetrical

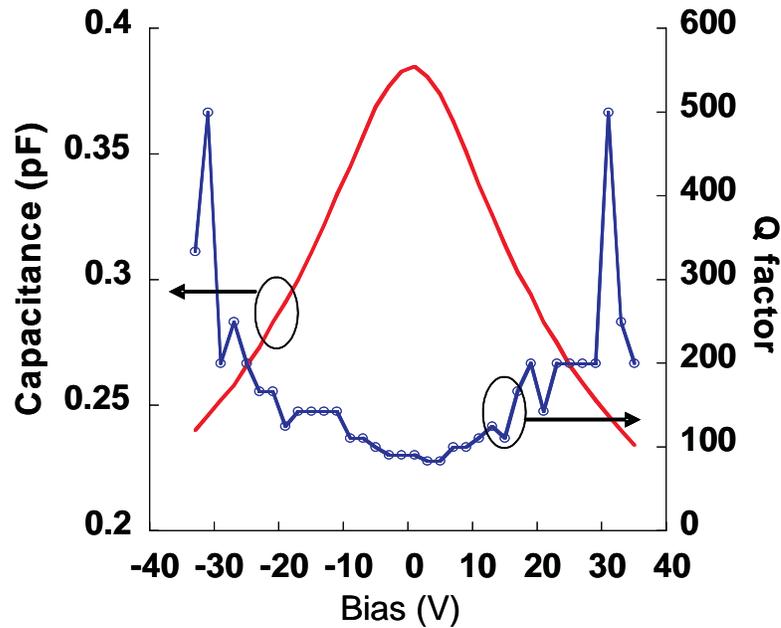


Figure 5.16: Representative tuning curve for thin-film BST interdigital varactor on polycrystalline alumina at 1 MHz.

filter. The nominal electrical length of the resonator was 57° at the center frequency and the characteristic impedance was 52.2Ω . A tapped design was used for the input and output feed and the impedance of the feed lines was 50Ω . The schematic of the optimized filter is shown in Figure 5.17, the nominal BST loading capacitor was found to be 1.26 pF for the desired response. The fingers of the BST interdigital varactor had a length of $200 \mu\text{m}$ and width of $5 \mu\text{m}$. The spacing of the fingers was $5 \mu\text{m}$ and the number of fingers was 24. Formulae for calculating the capacitance of multi-layered thin-film interdigital capacitors can be found in [80].

The filter parameters were found to be as follows: $W = 550 \mu\text{m}$, $S = 450 \mu\text{m}$, $L_1 = 5900 \mu\text{m}$, $L_2 = 4600 \mu\text{m}$, $W_f = 600 \mu\text{m}$, and $L_f = 5225 \mu\text{m}$. At the end of each BST varactor a 1 nF DC blocking capacitor with a rating of 200 V was attached. This served as the bias point for the BST varactors while providing a RF ground path for the high frequency signal. Parasitic resistances and inductances were also modelled in the design phase and filter parameters were adjusted to achieve the desired filter response. The layout of the filter was done in ADS (Advanced Design System).

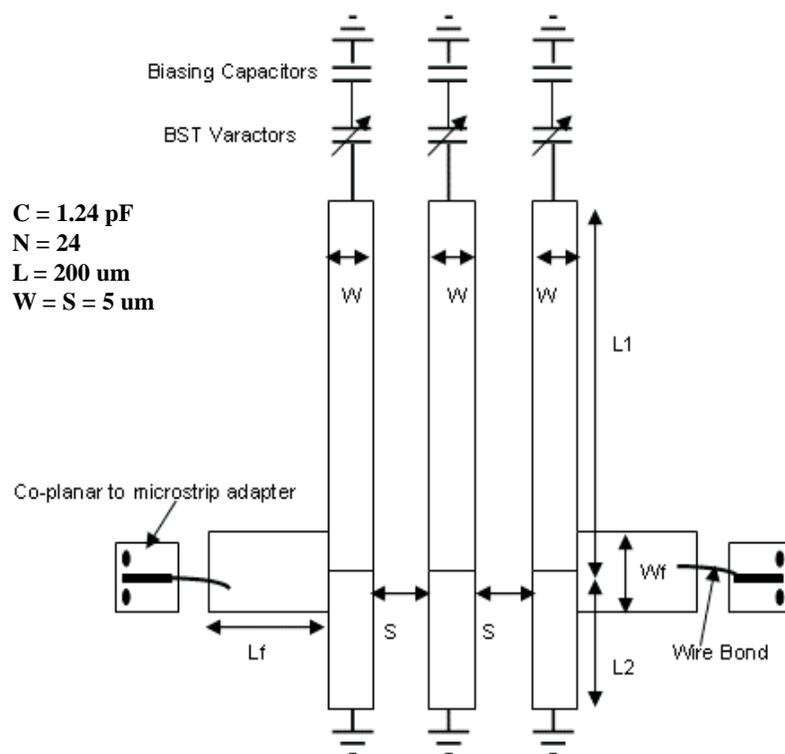


Figure 5.17: Schematic of the bandpass filter.

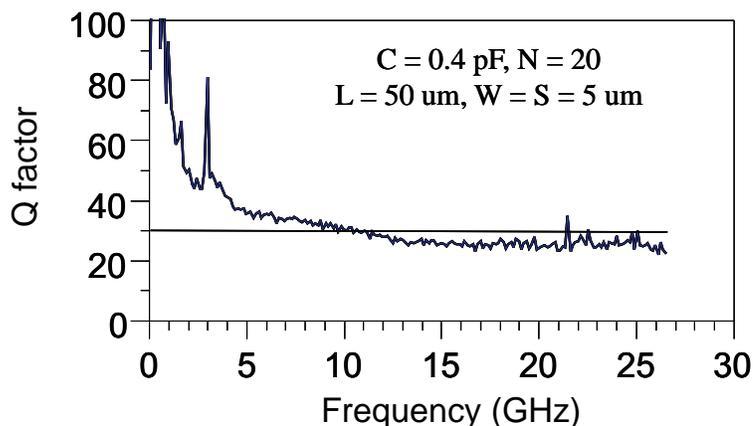


Figure 5.18: Q factor of varactor versus Frequency.

5.3.3 Filter Implementation

Polycrystalline alumina (Al_2O_3) was chosen as the substrate for fabrication of the BST varactors and tunable filters. The objective was to evaluate the suitability of alumina as substrate for BST-based tunable filter and compare it with the characteristics of a similar filter fabricated on sapphire. The advantages of alumina was discussed in Chapter 3. It is an excellent substrate for frequency-agile devices since it exhibits low loss tangent (0.0002) in the microwave range. Furthermore, the coefficient of thermal expansion of alumina ($\text{CTE} \sim 9$ ppm) is closely matched to BST and hence high temperature processing is possible without cracking the BST thin-films.

A representative tuning curve of the BST thin-film interdigital varactor on alumina is shown in Figure 5.16. A 1.7:1 (40%) tuning ratio is achieved for a varactor with $3 \mu\text{m}$ finger spacing and 35 V bias. This corresponds to a 120 kV/cm tuning field and is one of best results to date for BST varactors on any substrate. The Q factor data with frequency is shown in Figure 5.18. At frequencies < 5 GHz uncertainty in Q factor is large, this results in the large excursions in the data shown in Figure 5.18. At lower frequencies the Q factor of the varactor is in the range of 75–100 and the uncertainty in Q is higher for high Q values (see section 2.5). SEM (scanning electron microscopy) photographs of the interdigital varactor is shown in Figures 5.19 and 5.20.

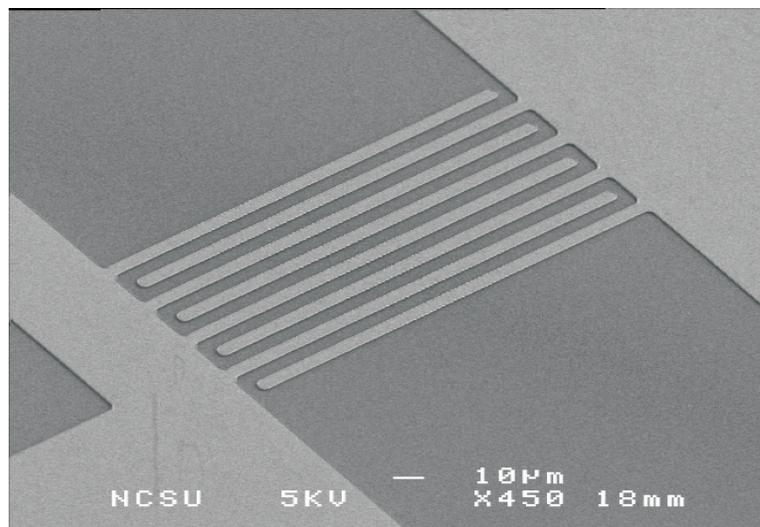


Figure 5.19: SEM photograph of interdigital varactor (450X).

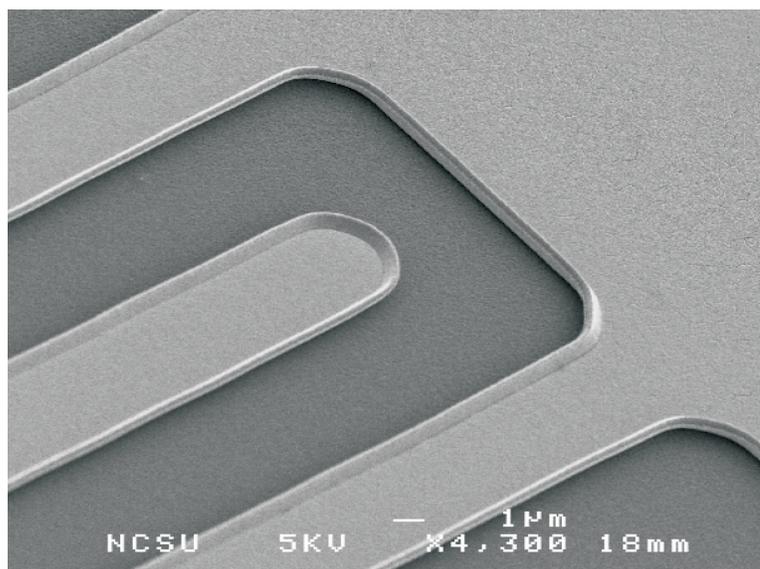


Figure 5.20: SEM photograph of interdigital varactor (4300X).

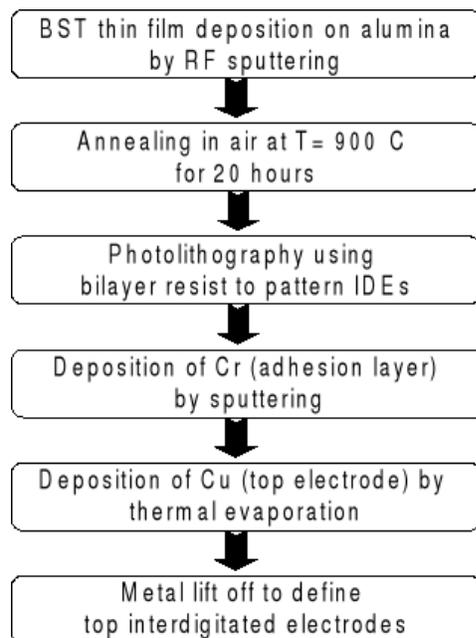


Figure 5.21: Process flowchart for sputtered BST thin-film fabrication process with copper metallization.

Radio frequency magnetron sputtering was used to deposit 600 nm of thin-film $\text{Ba}_{0.75}\text{Sr}_{0.25}\text{TiO}_3$ on 14 mm x 14 mm and 635 μm thick, one side polished alumina substrate. The deposition temperature was maintained at 300 °C. A sputtering gas mixture of oxygen and argon and 10 mtorr total pressure was used for depositing the BST thin-films. After deposition the films were annealed in air to obtain fully crystalline films. The details of the modeling and characterization of BST thin-film interdigital varactors on alumina has been described in Chapter 3.

A standard photolithography and metal lift-off technique was used for defining the filter pattern on the BST/alumina substrate. A bilayer technique using multiple layers of lift-off resist and positive imaging photoresist was used to make a thick photoresist stack on the samples. After exposure and development of the photoresist, the sample was metallized. A thin layer of Cr (0.02 μm) was deposited first by magnetron sputtering followed by 1 μm of Cu deposited by thermal evaporation. Cu was chosen as the top electrode metal in this work since it provides the highest conductivity of any base metal and it is inexpensive compared to noble metal electrodes (e.g. Au

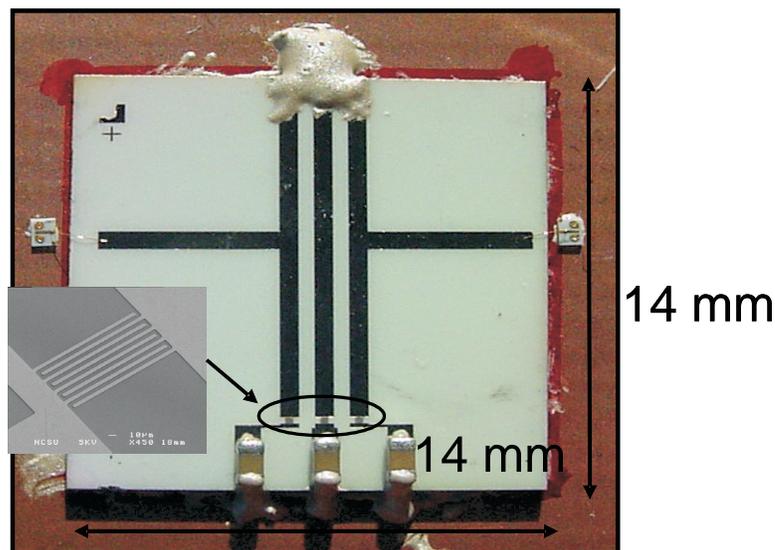


Figure 5.22: Assembled bandpass filter on an alumina substrate with integrated BST varactors shown in inset.

and Pt) which have been used in most oxide-based microwave devices to date. The advantages of copper metallization has been discussed in detail in Chapter 3. Finally a capping layer of Pt ($0.03 \mu\text{m}$) was deposited on top of the Cu layer. This prevented ambient oxidation of copper. Metal lift-off was then performed to define the complete filter structure. The backside of the alumina substrate was metallized using Cr ($0.02 \mu\text{m}$) and Cu ($1 \mu\text{m}$), this acts as the ground plane. The step-by-step process flow can be found in Figure 5.21. After fabrication, the filter was attached using conductive epoxy to a high-frequency laminate, see Figure 5.22. The metallized board served as the common ground plane for the filter and the J-micro CPW-to-Microstrip adapters used for input and output connections.

The copper surface of the board serves as the common ground plane. Since a “via” process was not used, the ground connections at the end of the resonators were made by “ground-wrapping” using conductive epoxy. The additional resistance in the range of $0.7\text{--}1 \Omega$ for each ground connection introduced by this grounding technique has been included in the simulation. The input and output connections to the filter was made using J-Micro CPW-to-Microstrip adaptors and wire-bonds, see Figure 5.23.

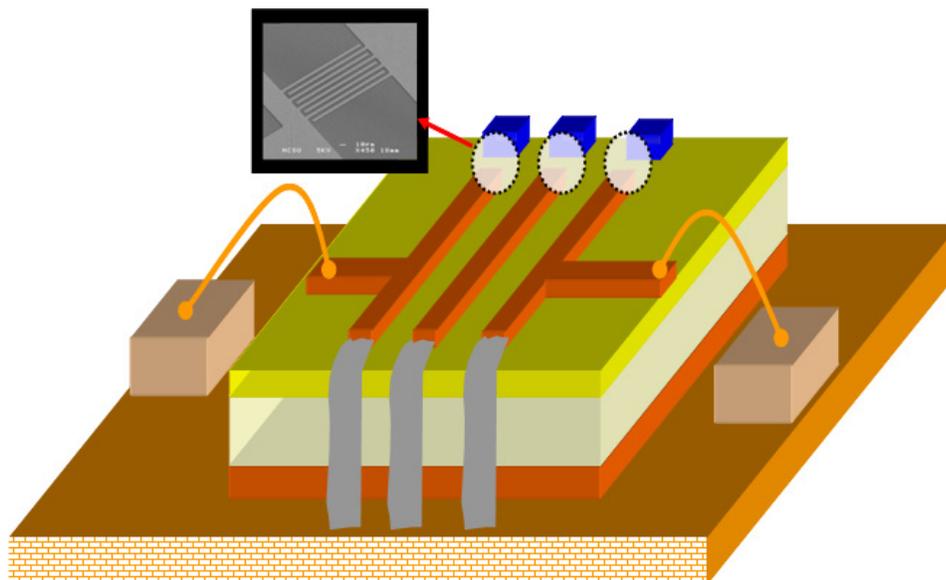


Figure 5.23: Schematic of the filter with epoxy ground wrapping and wirebonds at input and output.

5.3.4 Measured results

The filter was measured (see Figure 5.24) on a HP 8510C Network Analyzer using a $150\ \mu\text{m}$ pitch GSG (ground-signal-ground) probe from GGB Industries. An LRM calibration was performed using the CS-5 calibration substrate from GGB Industries.

The zero-bias response can be seen in Figure 5.25 and the filter is centered at 1.6 GHz with an insertion loss of 6.6 dB. This downward shift in the center frequency can be explained by a slight increase in the resonator length due to the use of epoxy for “ground-wrapping”. The overall mask dimensions of the filter was 13 mm x 13 mm. The filter was fabricated on a 14 mm x 14 mm substrate and this leads to an extension of the line length by approximately $1000\ \mu\text{m}$. This explains the downward shift in the center frequency compared to a designed value of 1.75 GHz. The BST varactors at the end of the resonators were measured to be 1.16 pF at 1 MHz. A comparison of the measured and simulated zero bias filter response including these effects is shown in Figure 5.25 and the agreement is quite good. The slight discrepancy at higher frequency can be attributed to unaccounted parasitics in the simulation.

The BST varactors had a zero bias Q factor of about 20 in the range of 1–2 GHz.

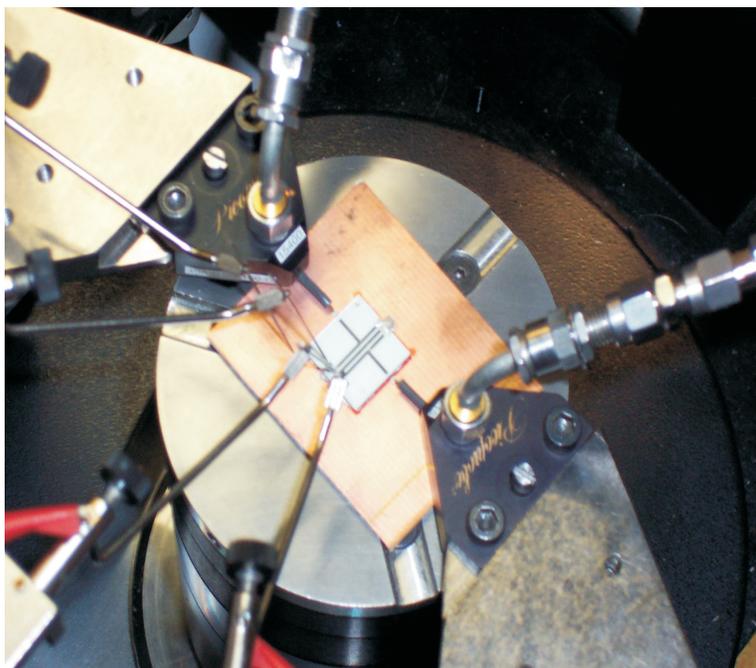


Figure 5.24: Filter under test.

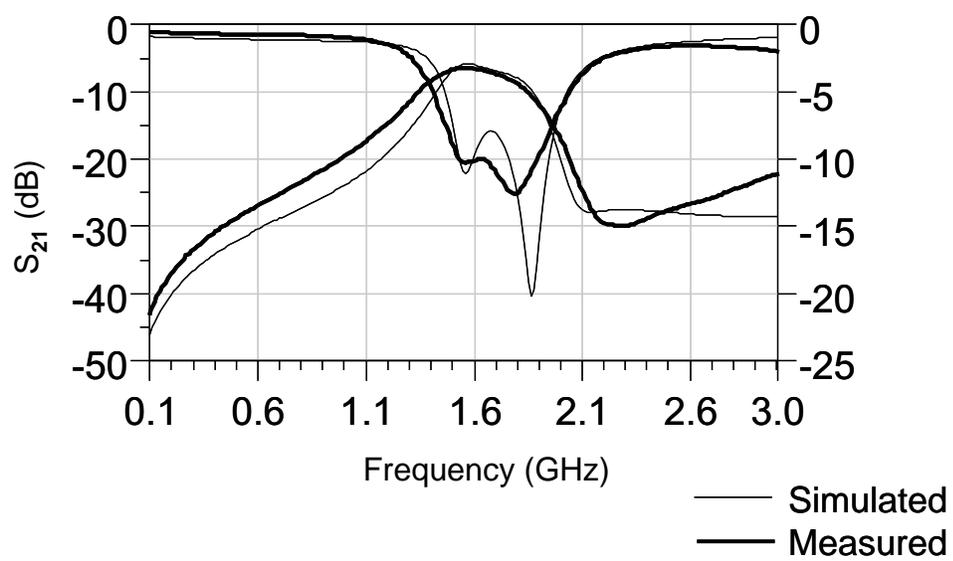


Figure 5.25: Comparison of the measured and simulated filter at zero bias.

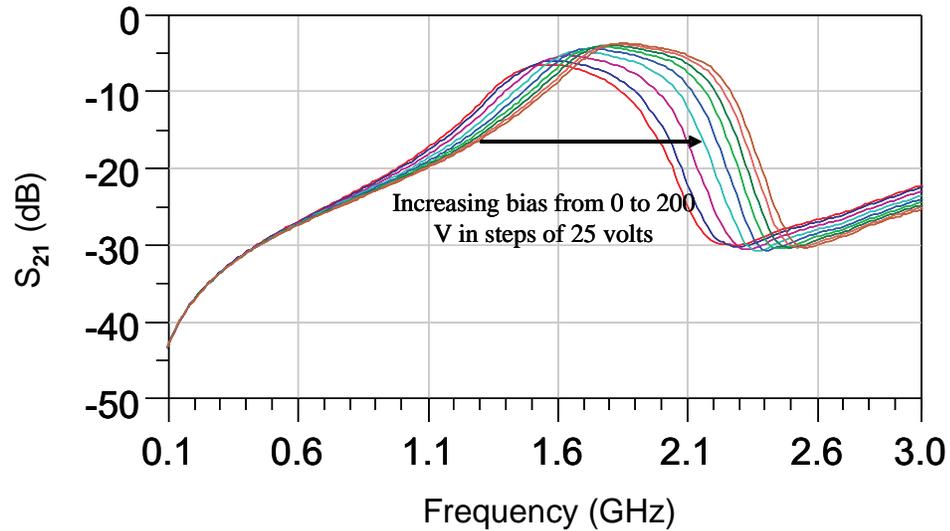


Figure 5.26: Measured S_{21} of the filter with applied bias.

The varactors were biased using DC probes at one end of the DC blocking capacitors. All varactors were tuned in tandem. The DC bias was varied from 0 V to 200 V in steps of 25 V and the S-parameter data was recorded at each bias point. From a comparison of measured and modelled data the BST varactor tuning was found to be 2:1 (50%) for 200 V bias. The center frequency of the filter tuned from 1.6 GHz at zero bias to 2 GHz at 200 V bias, see Figure 5.26. The frequency tuning achieved was 25% and the filter is capable of covering the GPS and the GSM bands at 1800 and 1900 MHz. In an improved fabrication process where the parasitics are eliminated, the tuning range of the filter would be further increased. The mid-band insertion loss was 6.6 dB at zero bias and this decreased to 4.3 dB at 200 V bias. The decrease in insertion loss with increasing bias is in part due to the increased Q factor of the BST varactors with bias (see Figure 5.16) and also in part due to improved matching that results with change in capacitance (see Figure 5.27). A summary of the filter tuning results can be found in Table 5.2.

The tuning was achieved by an electric field of 300 kV/cm. The BST interdigital varactors were designed with a finger width and spacing of 5 μm but a slight overdevelopment of the liftoff resist lead to an increase in the finger spacing by 1.5–2.0 μm .

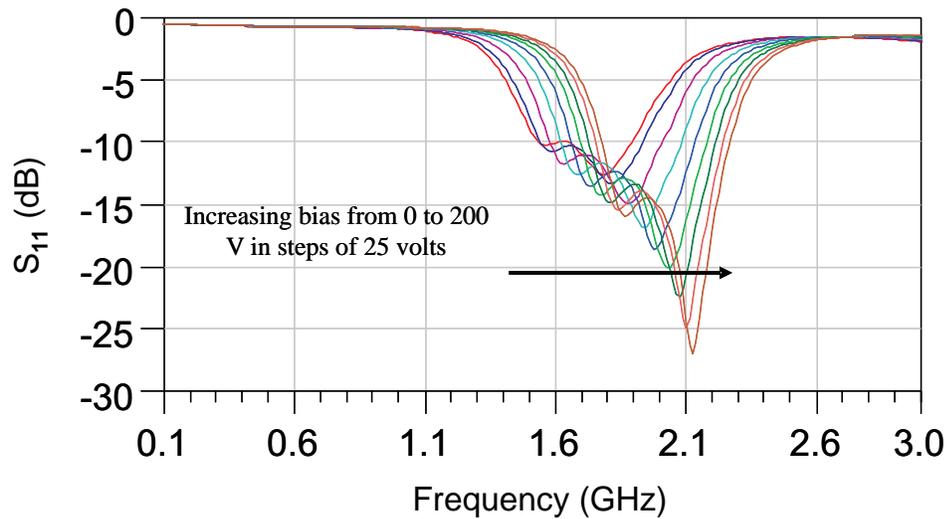


Figure 5.27: Measured S_{11} of the filter with applied bias.

It should be noted that the tuning voltage can be reduced by decreasing the finger spacing and simulation results show that with $3 \mu\text{m}$ spacing, similar tuning can be achieved by voltages less than 100 V. In Chapter 6 a tunable bandpass filter on FR4 with 22% center frequency tuning at 130 V bias will be presented.

5.3.5 Effect of metallization, vias and wire bond

Though tuning voltages are rather high compared to parallel plate BST varactors, a major advantage is the simple and inexpensive fabrication process. It should also be noted that such high voltages can be readily achieved in non-portable devices using DC to DC converters at low cost. In comparison with commercially available fixed frequency bandpass filters at similar frequencies the BST filters have an additional loss of about 2.5–3.5 dB. However, this situation can be straightforwardly remedied by using a “via” process and a thicker metallization. The “via” process would reduce the parasitic resistance at the end of the resonator and simulation results show that it would reduce the insertion loss by approximately 1–1.5 dB. The effective metal thickness used in our process was about $0.8 \mu\text{m}$ (physical thickness was $1 \mu\text{m}$) since

Table 5.2: Summary of filter results

Bias(V)	Center Frequency (GHz)	Insertion Loss (dB)	Return Loss (dB)
0	1.60	6.55	10.00
25	1.64	6.13	10.30
50	1.74	5.80	11.00
75	1.80	5.33	12.00
100	1.84	4.90	12.35
125	1.89	4.70	12.94
150	1.92	4.45	13.40
175	1.95	4.37	13.90
200	2.00	4.30	14.70

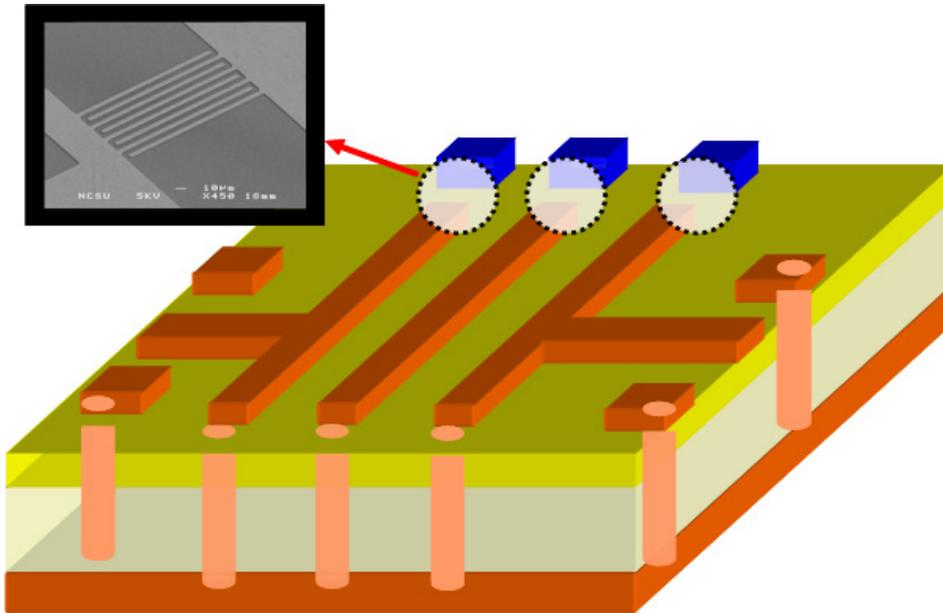


Figure 5.28: Schematic of the filter with vias and on-chip probe pads.

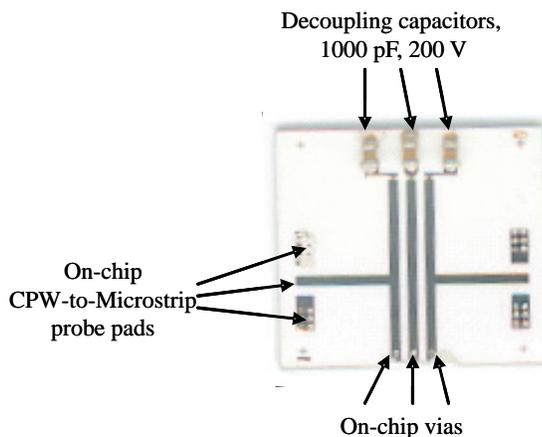


Figure 5.29: Fabricated tunable filter with vias and on-chip probe pads.

the conductivity of evaporated copper was approximately 80% of the base metal conductivity. The skin depth of copper is $1.65 \mu\text{m}$ at 1.6 GHz and hence the insertion loss can be considerably reduced by increasing the metal thickness. Furthermore, the wire bond and the CPW-to-Microstrip adapters at the input and output introduce an additional 0.5–0.7 dB of loss. In an integrated process they would be eliminated leading to further improvement in insertion loss. A new via-process was developed to eliminate the need for epoxy “ground-wrapping” (Figure 5.23). Furthermore the wirebonds at the input and output was also eliminated and “on-chip” probe pads were used as shown in Figure 5.28. The fabricated filter using this new process is shown in Figure 5.29. A 2.1 dB improvement in insertion loss was obtained, in line with the reduction in loss predicted by simulation. The integrated on-chip filter with vias and probe pads showed a zero bias insertion loss of 4.5 dB and the loss decreased to 3.5 dB at 125 V bias. Tuning was found to be 10% from 1937 MHz to 2133 MHz. Return loss was better than 9 dB over the tuning range. The measured insertion loss and return loss of the on-chip filter with vias can be found in Figures 5.30 and 5.31 respectively. The tuning data is limited to 125 V since the BST varactor broke down at that bias voltage.

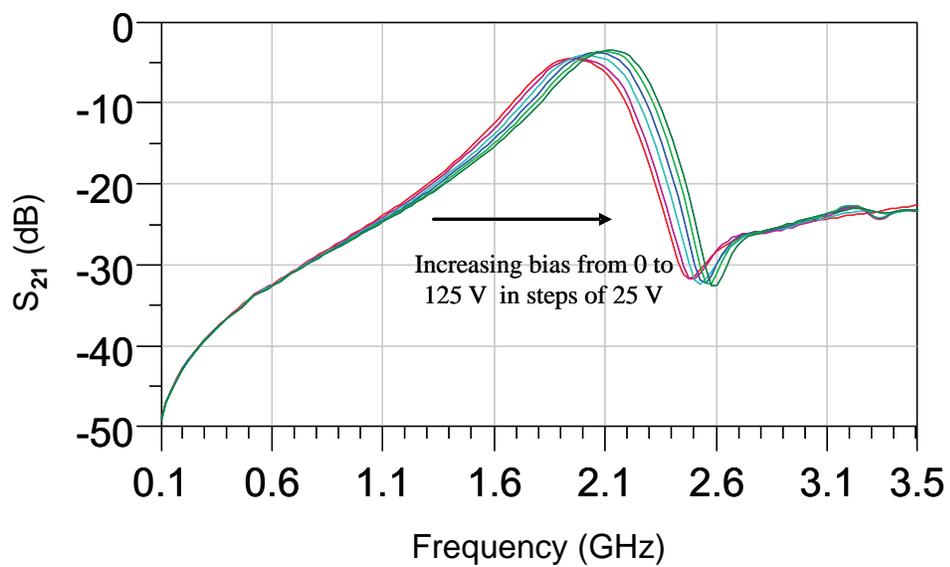


Figure 5.30: Measured S_{21} of the on-chip filter with applied bias.

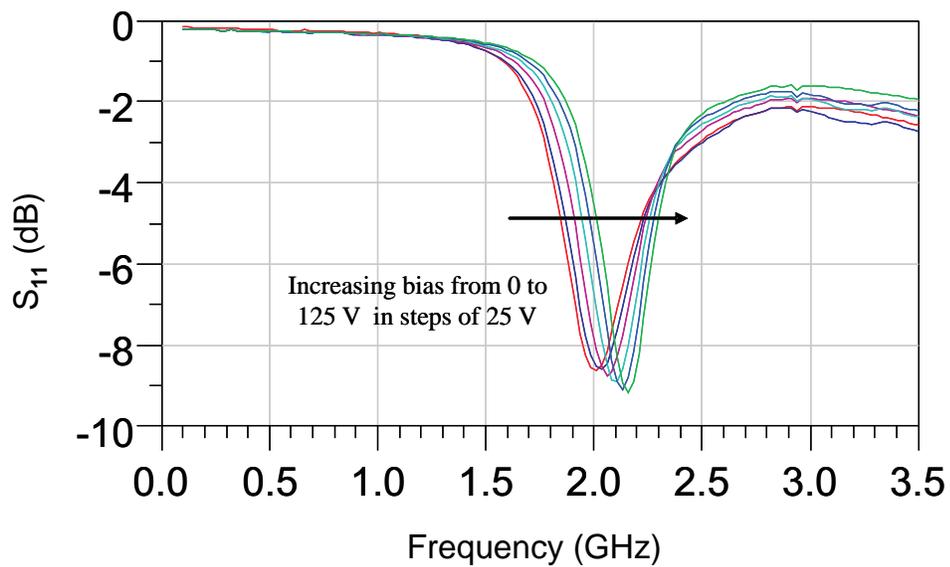


Figure 5.31: Measured S_{11} of the on-chip filter with applied bias.

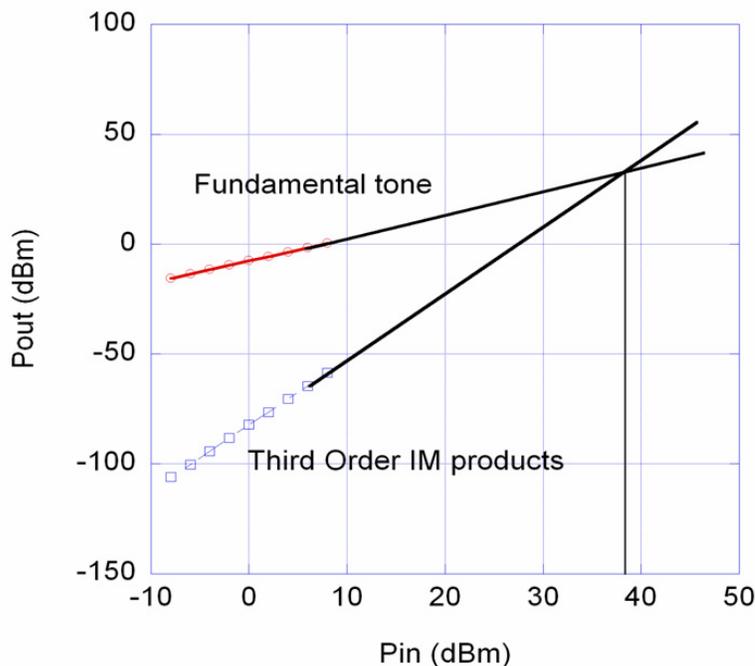


Figure 5.32: Two-tone characterization results for the filter.

5.3.6 Non-linear characterization

The tunable filter was also characterized for nonlinearities. The filter is expected to be nonlinear since the C-V curve of the BST varactor is nonlinear. First a two tone test was carried out using the test setup shown earlier. The two tones (1.60 GHz and 1.61 GHz) were centered in the passband of the filter and the output power of the fundamental tones and the third order intermodulation product was recorded as the input power was swept. The IIP3 was found to be +38 dBm (Figure 5.32). It was ensured that the test setup does not contribute to any non-linearity.

The filter was also characterized for its response to a digitally modulated signal. A CDMA 2000 pilot signal was used for the test. To increase the output power of the signal obtained from the Agilent signal generator a highly linear power amplifier from RFMD [110], RF3805, was used. It has an IIP3 of $> +50$ dBm and it was ensured that the ACPR of the test setup was at least 10 dBc better than that of the filter at all test conditions. The measurement setup is shown in Figure 5.33. The

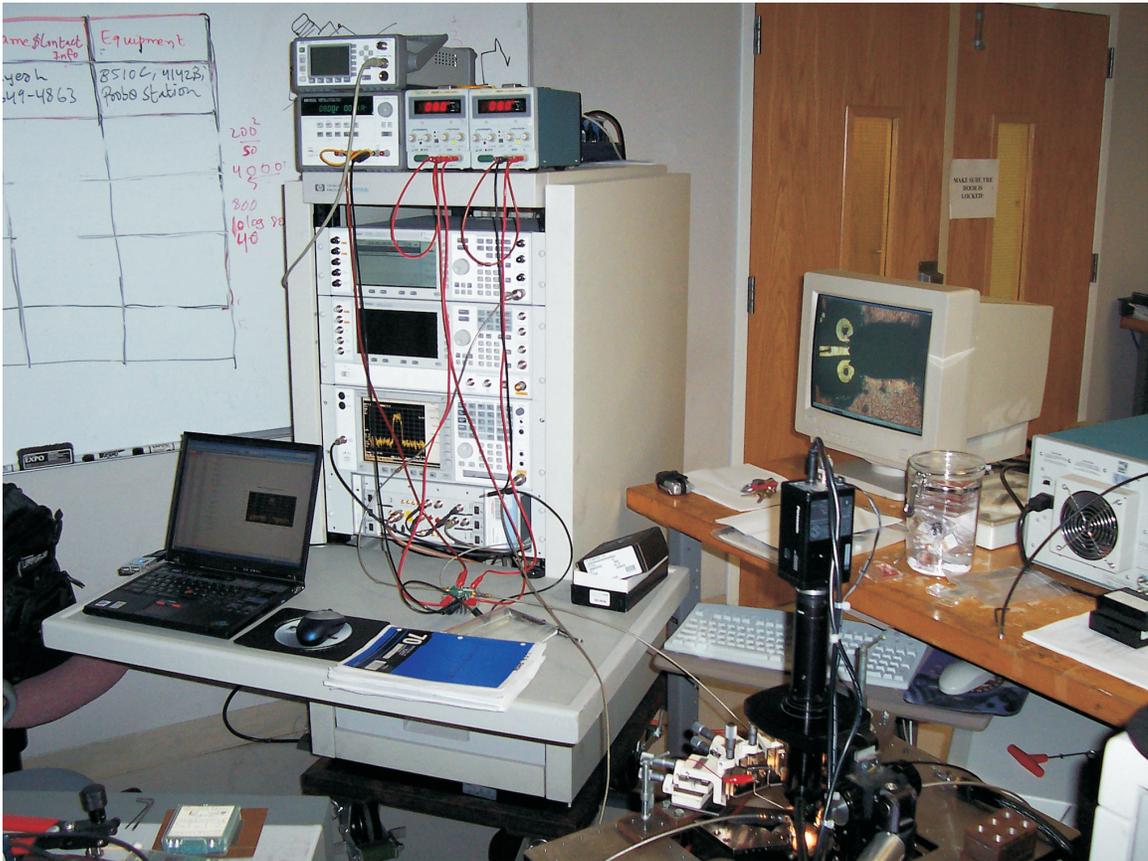


Figure 5.33: ACPR measurement setup.

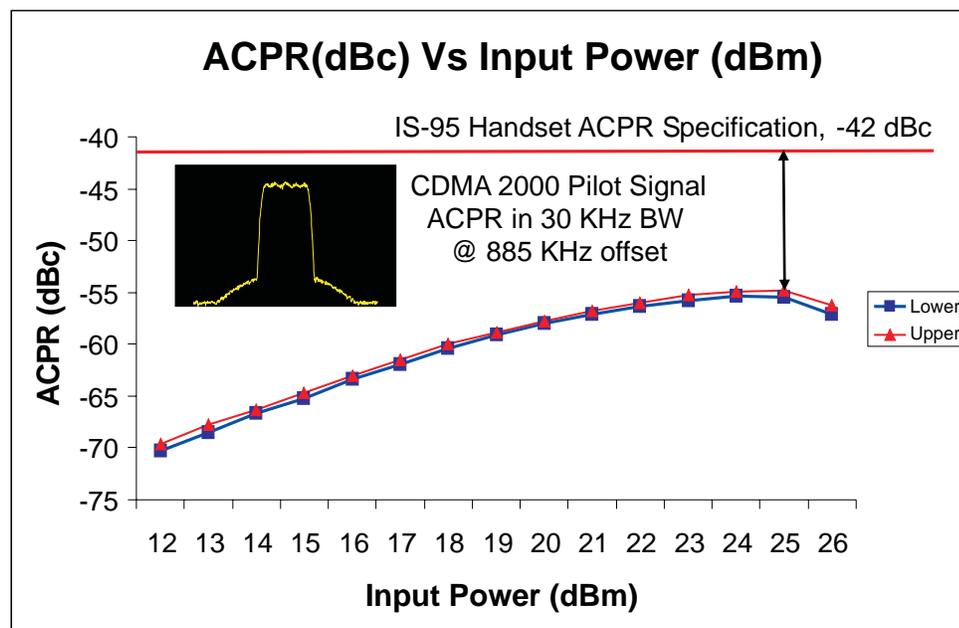


Figure 5.34: ACPR results for the filter, the inset shows a representative spectrum for a CDMA 2000 signal.

ACPR (adjacent channel power ratio) was measured using a built in measurement personality in the Agilent PSA. As shown in Figure 5.34 the ACPR is better than -55 dBc up to + 26 dBm of input power. This compares favorably with the IS-95 handset ACPR specification of -42 dBc. It should be noted that both IIP3 and ACPR values are worst case values since the measurements were taken at zero bias. These parameters are expected to improve with bias as the device operates in the region of the C-V curve that has a smaller slope.

5.3.7 Summary

A tunable combline filter based on thin-film BST interdigital varactors and with a center frequency of 1.6 GHz was demonstrated. The filter was fabricated on a standard polycrystalline alumina substrate using copper metallization. The measured filter results closely matched the simulation results when all parasitic elements were accounted for. The zero-bias insertion loss of the filter was 6.6 dB and this decreased

to 4.3 dB at 200 V bias. The tuning was found to be 25% for an applied electric field of 300 kV/cm. The filter was found to be fairly linear with IIP3 and ACPR values of +38 dBm and -55 dBc respectively. The integrated on-chip filter with vias and probe pads showed a zero bias insertion of 4.5 dB and decreased to 3.5 dB at 125 V bias. Tuning was found to be 10% from 1937 MHz to 2133 MHz.

5.4 Filter performance and figure-of-merit

In Chapter 4 the concept of network transformation factor was formulated and a new figure-of-merit (FOM) was introduced to quantify the trade-off between Q factor and tunability. It was shown that different networks transform the tunability of the varactor in a manner which is inversely related to the total Q factor of the network. The exact relationship is dependent on the network topology, this is quantified by the network transformation factor, τ_{NTF} . The FOM was formulated in terms of τ_{NTF} and the Q factor. It enables comparison of different networks and the Q factor and tunability trade-off. Results were presented for two networks of Type D (see section 4.2.2). The tunable filters described in the previous chapter belongs to the classic combline topology or Type A network previously discussed. The filters results will now be quantified in terms of τ_{NTF} , FOM, and Q . The definition of Q factor is slightly different from that of a single resonator since new variables such as coupling factor with adjacent resonators and fractional bandwidth must be taken into account. The modified definition will be presented below. Before discussing the filter tuning results, the tuning and Q factor trade-off for a single combline (Type A) resonator will be discussed. This network topology is the building block for the tunable filters described in pervious sections.

As previously noted, the tuning for Type A networks can be increased by shortening the length of the transmission line, though at the expense of reduced Q . To keep the resonant frequency constant, the capacitance value must be increased. In practical situations this usually means that the Q factor of the capacitor will be lower. The effect on total Q factor of the resonator and capacitor combination is

therefore two-fold: first the total energy stored in the transmission line is reduced since the physical length has been shortened, and second the Q factor of the varactor is also reduced due to increased capacitance value. For the sake of further discussion it will be assumed that the Q factor of the capacitor is constant regardless of the value of the capacitance. This represents an optimistic situation and will suffice for instructive purposes. It will be shown that even in this situation the total Q factor is considerably reduced as the tuning increases.

In the limit of shortening the length of the transmission line, the frequency response of Type A network asymptotically approaches that of the a parallel inductor and capacitor combination. The resonant frequency tuning ratio (f_r) correspondingly approaches the maximum limit (f_m) of $\sqrt{\eta}$, where η is the capacitance tuning ratio of the varactor. As the length is shortened the transmission line approximates an inductor and the total Q is dominated by the Q factor of the capacitor or the inductor, whichever is lower. Two different lengths of shorted combline resonator on alumina (635 μm thick, $\epsilon_r = 10$) was considered, the first resonator was 0.1 cm long and the second one was 1.2 cm. Both resonators were loaded with appropriate capacitance value so that the nominal resonant frequency was the same, in this case 1626 MHz. The capacitance tuning ratio in both case was 2:1 ($\eta = 2$). The Q factor of the varactor was assumed to be 10 and independent of frequency. The length of the shorted resonator on alumina was 1.785 cm for resonance at 1626 MHz without the capacitive loading. The unloaded Q factor without the capacitor was 200 at 1626 MHz. Copper metallization with a thickness of 5 μm was used for Q factor calculations.

For the resonator of length 0.1 cm, a capacitive loading of 22.2 pF was required to achieve resonance at 1626 MHz. The nominal Q factor of the network was 9.62. When capacitance was reduced to 11.1 pF, the resonant frequency shifted to 2291 MHz and the Q factor increased to 9.8. The frequency tuning ratio (f_r) was 1.409 and the network transformation factor, τ_{NTF} was found to be 0.996. This shows that the tunability is close to the maximum achievable limit of 1.0 ($\tau_{\text{NTF},\text{max}}$). The Q factor of the network is however limited by that of the capacitor and is always < 10 . The FOM was calculated as 4.008.

For the resonator of length 1.2 cm, a capacitive loading of 1.1 pF was required

to achieve resonance at 1626 MHz. The nominal Q factor of the network was 16.0. When capacitance was reduced to 0.55 pF, the resonant frequency shifted to 1923 MHz and the Q factor increased to 23.1. The frequency tuning ratio (f_r) was 1.183 and the network transformation factor, τ_{NTF} was found to be 0.836. The tunability in this case is considerably lower than the maximum achievable limit of 1.0. The Q factor of the network is however more than twice that of the varactor alone. The FOM was calculated as 4.22. Thus, though the first network offers considerably more tuning than the second one, the FOM for the second network is slightly higher. This means that the second resonator design with the longer transmission line and reduced tuning provides a better overall trade-off between Q factor and tunability. The two cases discussed above demonstrate the inherent trade-off between tunability and Q factor for a tunable resonator. The usefulness of the network transformation factor and the FOM in quantifying the trade-off is also evident. The filter tuning results will now be analyzed in terms of τ_{NTF} and FOM.

The tuning data for the third-order combline filter on alumina and sapphire will be used for the following discussion. Cohn [111] described a formula (see Equation (5.1)) which quantifies the effect of dissipation on the insertion loss of a bandpass filter.

$$\text{IL} = 4.343 \sum_{i=1}^N \frac{\Omega_c}{(\text{FBW})(Q_{ui})} g_i \text{ dB} \quad (5.1)$$

Here IL is the insertion loss of the filter in dB, FBW is the fractional bandwidth of the filter, Q_{ui} is the unloaded Q of the i^{th} combline resonator corresponding to g_i and calculated at the center frequency of the filter, N is the order of the lowpass prototype, Ω_c is the cutoff frequency of the lowpass prototype and g_i is the lowpass prototype element value.

If the unloaded Q of the resonators are equal and $\Omega_c = 1$, Equation (5.1) can be simplified to yield the Q_u , the unloaded Q of the resonator, see Equation (5.2).

$$Q_u = \frac{4.343}{(\text{IL})(\text{FBW})} \sum_{i=1}^N g_i \quad (5.2)$$

$$Q_u = \frac{13.9}{(\text{IL})(\text{FBW})} \quad (5.3)$$

To a good approximation the sum of g_i 's for a third-order filter is equal to 3.2 for a tchebychev lowpass prototype with 0.1 dB of ripple, Equation 5.2 can be further simplified to Equation 5.3. For the combline filter on alumina (see section 5.3.4), $\text{FBW} = 0.2$, and $\text{IL} = 4.3$. Using Equation 5.3, the unloaded Q of a single resonator in the combline filter was found to be 16.16. The frequency tuning ratio (f_r) of the filter was perviously found (see section 5.3.4) to be 1.25, hence, $\tau_{\text{NTF}} = 0.884$ and the FOM (K_τ) of the filter was calculated to be 4.04. It is readily seen that the FOM of the filter is approximately equal to the FOM of the tunable resonators discussed earlier. This demonstrate that the filter design represents a good trade-off between Q factor and tunability.

The tunable filter on sapphire can be analyzed in a similar manner. The $\text{FBW} = 0.2$, and $\text{IL} = 3.3$ for the third-order filter on sapphire (see section 5.2.4). Using Equation 5.3, the unloaded Q of a single resonator in the combline filter was found to be 21.06. The frequency tuning ratio (f_r) of the filter was perviously found (see section 5.2.4) to be 1.18, hence, $\tau_{\text{NTF}} = 0.835$ and the FOM (K_τ) of the filter was calculated to be 3.80.

It was perviously observed that the filter on alumina offers higher tuning than the filter on sapphire at the cost of higher insertion loss. However, the FOM for the filter on alumina is higher than that of the filter on sapphire and hence represents a better design trade-off. The FOM (K_τ) and τ_{NTF} are two important parameters that allow the comparison of tunable filter with different characteristics. Using the network transformation factor and the FOM, different filter topologies and fabrication technologies can be contrasted in a unified manner.

5.5 Conclusion

In this chapter frequency-agile filters on sapphire and alumina substrates using integrated BST thin-film varactors at room temperature were presented. This is the first demonstration of a tunable bandpass filter on alumina at room temperature and using copper metallization reported in the literature. While sapphire substrate is single crystalline and hence expensive, alumina is polycrystalline and is widely available at low cost. When proper integration techniques were used, the tunable filter on alumina exhibited a lower loss than the filter on sapphire. The tuning characteristics and nonlinear behavior were also similar. The two filters were compared using the network transformation factor τ_{NTF} and the figure-of-merit (K_{τ}) for tunable resonator formulated in Chapter 4. It was found that the bandpass filter on alumina has a higher figure of merit than a similar filter on sapphire, representing optimized design and a better design trade-off between Q factor and tunability. It is expected that the BST thin-film interdigital varactor on polycrystalline alumina and copper metallization will be a competitive technology and a cost-effective solution for the next generation of multi-band and multi-standard devices for both commercial and military applications.

In the next chapter the advantages of discrete BST thin-film varactor technology will be described and tunable filters based on this technology will be presented.

Chapter 6

Tunable Filters using Discrete BST Thin-Film Varactors

6.1 Introduction

In the previous chapter the focus was on BST thin-film interdigital varactors on sapphire and alumina and tunable filters monolithically integrated with BST varactors were reported. These filters had insertion loss in the 3–7 dB [72, 105, 112] range over the full tuning range. A significant contribution to the total insertion loss was identified as skin effect loss in transmission lines used for the filter structure. This is especially significant in the frequency range of 1–6 GHz where the lithographic challenge is fabricating interdigital fingers that are 3–5 μm (three skin depths) thick and spaced 3–4 μm apart.

One solution to this problem is to fabricate discrete BST thin-film interdigital varactors and subsequently integrate them in a hybrid manner on a microwave laminate. This enables the transmission lines comprising the filter to be considerably thicker than three skin depths at the frequencies of interest and simultaneously affording a

simple and inexpensive integration with BST thin-film varactors. This solution compares favorably with the one where a masking process is employed to increase the metal thickness for the transmission lines in the circuit to a thickness greater than that used for the fingers in the interdigital varactors. This masking process is essential for avoiding aspect ratio problems during photolithography and lift-off. The discrete BST varactor technology also enables rapid integration of BST with other technologies. For instance, filters or other frequency-agile devices could be fabricated using a standard PCB or a thick-film process and discrete BST varactors could be attached as a last step. This affords integration of heterogeneous technologies in straightforward manner and is also low-cost.

In this chapter discrete BST thin-film interdigital capacitors on alumina will be described. The capacitors were fabricated on a 1 inch square tile of alumina comprising approximately 150 capacitors of 0603 (60 mils X 30 mils) footprint. Singulation was done using a diamond saw. Electrical and thermal characterization of the BST varactors in discrete form will be presented in this chapter. As an application band-stop and bandpass filters on a FR4 board using the discrete varactors were fabricated and characterized. Tuning data and nonlinear characterization of the filter is also presented.

6.2 Design of discrete BST varactors on alumina

Polycrystalline alumina (Al_2O_3) was chosen as the substrate for fabrication of BST varactors. The advantages of alumina has been previously discussed in Chapter 3. Thin-films of $\text{Ba}_{0.60}\text{Sr}_{0.40}\text{TiO}_3$ were deposited on double side polished alumina substrate (Cooresstek, Golden, Colorado.) using a radio frequency magnetron sputtering technique. Deposition time of 60 minutes resulted in a film thickness of $0.6 \mu\text{m}$. Post deposition anneal was done ex-situ in air at $900 \text{ }^\circ\text{C}$ for 20 hours to fully crystallize and densify the BST films [113]. Detailed deposition conditions have been described in Chapter 3. An array of discrete IDCs was patterned on the BST/alumina substrate by a photolithographic lift-off technique, see Figure 6.1.

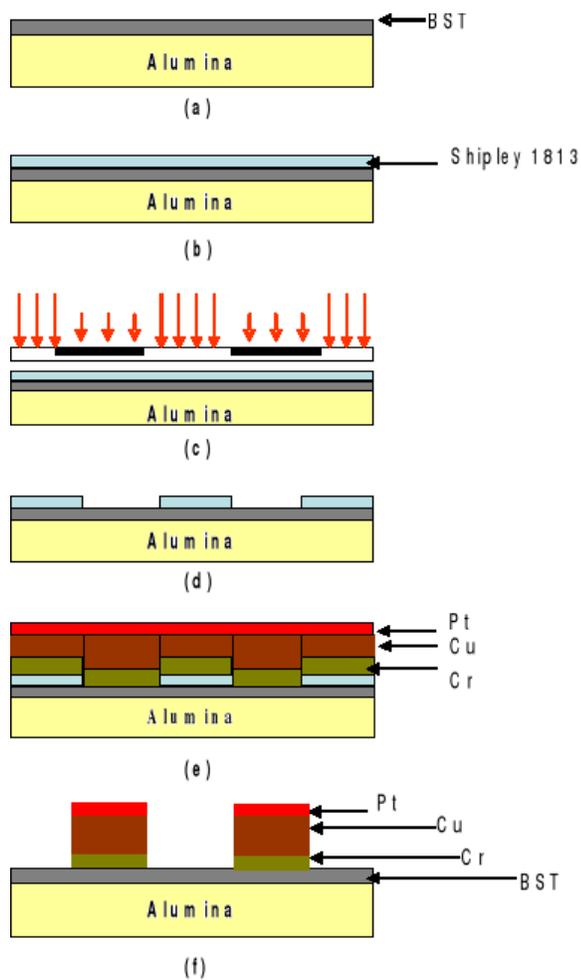


Figure 6.1: Modified process flow for narrow gap discrete IDC varactors.

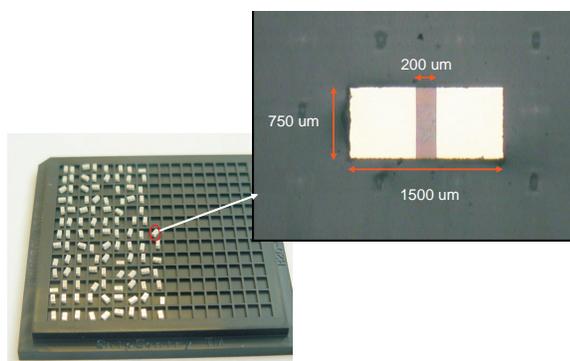


Figure 6.2: Diced 0603 BST varactor in carrier.

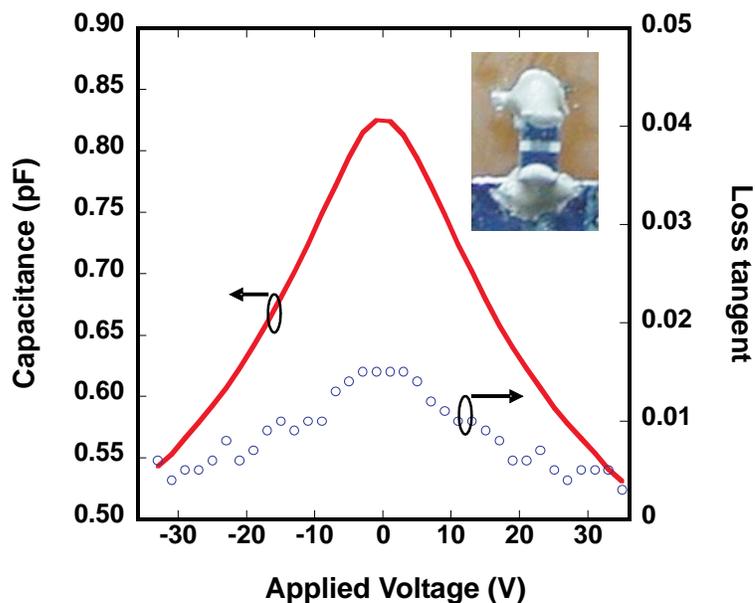


Figure 6.3: Representative tuning curve for discrete (0603) thin-film BST interdigital varactor on polycrystalline alumina at 1 MHz.

A modified lift-off technique using positive imaging photoresist Shipley 1813 was developed and used in this work. After the photoresist patterns were prepared, a two-layer metallization stack was deposited. Initially, a thin layer of Cr ($0.02 \mu\text{m}$) was deposited. This acts as an adhesion layer. Subsequently, $0.5 \mu\text{m}$ of Cu was deposited by thermal evaporation without breaking vacuum in a dual deposition chamber. Finally a capping layer of Pt ($0.03 \mu\text{m}$) was deposited on top of the Cu layer. This was done to prevent ambient oxidation of copper. To complete the IDC fabrication, metal lift-off was done in Microchem PG remover at 60°C . The fingers of the BST interdigital varactor had a length of $195 \mu\text{m}$ and width of $10 \mu\text{m}$. The finger spacing was $3 \mu\text{m}$ and the number of fingers was 16. The discrete BST varactors were subsequently diced (Figure 6.2) and characterized.

Capacitance and the loss tangent data after dicing is the same as that measured before the dicing process. A tunability of 1.5:1 or 33% was recorded for 35 V bias (116 kV/cm). The loss tangent at zero bias was 0.015 and this decreased by a factor of three to 0.005 at 35 V bias, see Figure 6.3. Formulae for calculating the capacitance of multi-layered thin-film interdigital capacitors can be found in [80]. The variation of

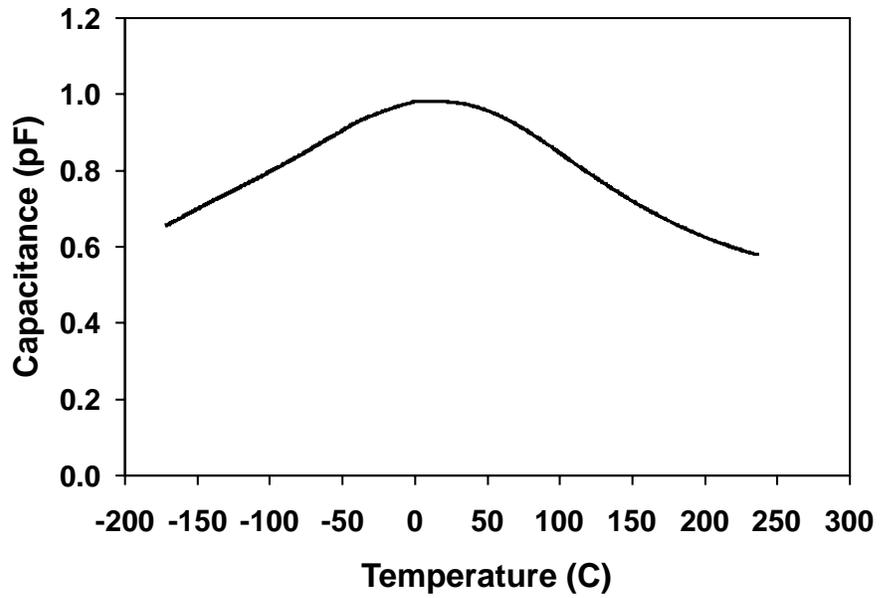


Figure 6.4: Temperature variation of the diced BST varactor.

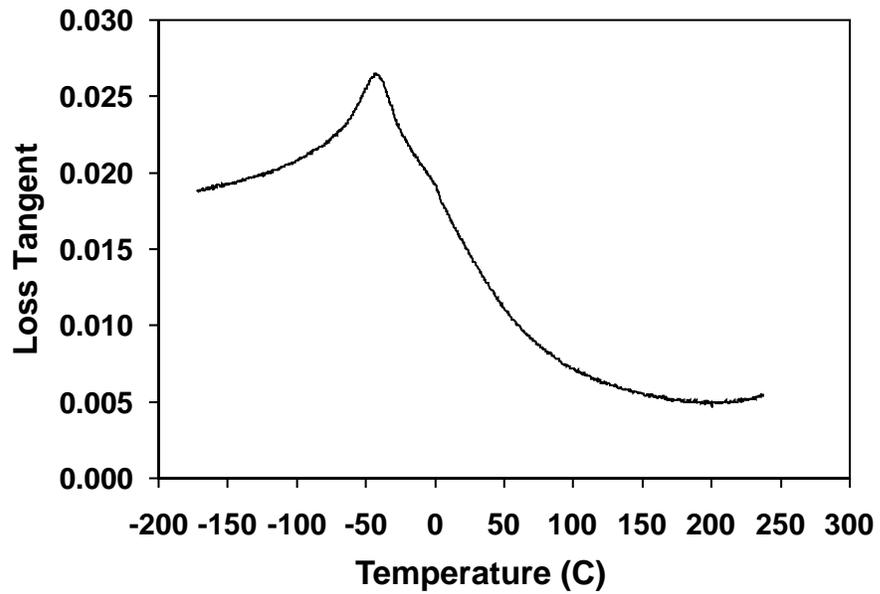


Figure 6.5: Loss tangent variation of the diced BST varactor.

capacitance and loss tangent over a wide temperature range from $-170\text{ }^{\circ}\text{C}$ to $+230\text{ }^{\circ}\text{C}$ was measured. As shown in Figures 6.4 and 6.5, the curves show a typical ferroelectric to paraelectric transition at around $+3\text{ }^{\circ}\text{C}$. This is expected for a 60/40 composition of the BST target used for this work. Upon approach to T_c (Curie temperature) during cooling, the loss tangent increases, heralding the onset of the ferroelectric phase. In the next section tunable bandstop filter on FR4 substrate using discrete IDC varactors will be described.

6.3 Tunable bandstop filter on FR4

6.3.1 Introduction

Bandstop filters are widely used for improving the selectivity and sensitivity of communication systems [114, 115, 116]. Such filters help mitigate the receiver interference problems in dense wireless environments. The use of tunable filters leads to greater functionality, better channel selectivity, reduced size and weight since the same hardware can be employed at multiple bands. With the proliferation of wireless systems and use of new frequency spectrum for newer standards and protocols, receiver desensitization due to interference has morphed into a pressing problem. Mechanical, cavity, and YIG filters have been employed for many years for achieving frequency-agile bandstop filters. These filters are both bulky and large in size, precluding their use in most but the very specialized and niche applications where weight, size and cost are not of great concern. Furthermore, tuning speed is critical in many applications. Both YIG and mechanically tuned filters have slow tuning speed. The tuning speed of YIG filter is in the milliseconds range and also requires tuning current in the $m\text{A}$ range. It does however provide extremely sharp rejection. Tunable bandstop filters using varactor diodes and pin diodes have also been investigated in the literature. Such products are also available commercially. Recently, compact bandstop filter designs on standard PCB substrates have been introduced [117, 118, 119, 120]. A frequency-agile bandstop filter using BST thin-film as reported in [121]. A novel

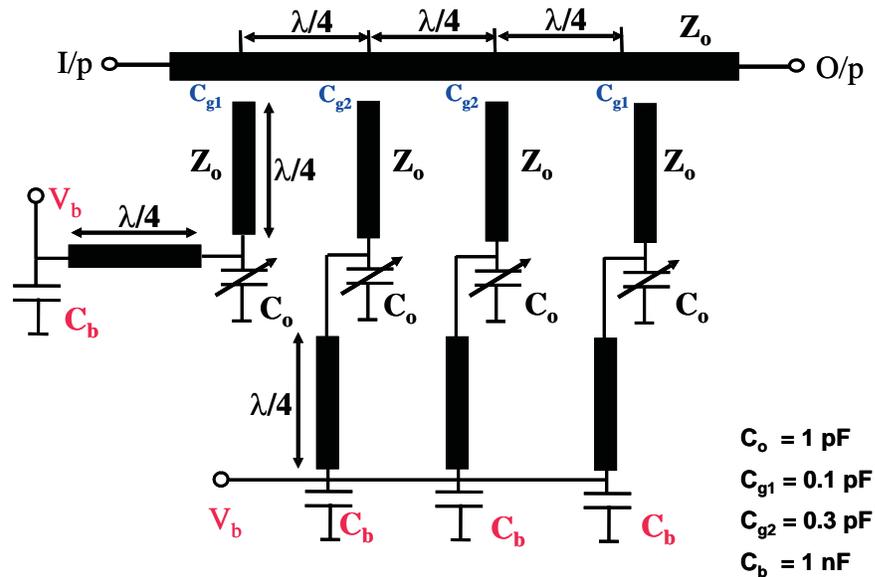


Figure 6.6: Schematic of the capacitively coupled narrowband bandstop filter.

bandstop filter with sharp rejection skirts was reported in [122]. Bandstop filters on commercial silicon substrates have also been reported [123]. Two configurations of bandstop filters were designed and characterized using BST thin-film IDC varactors in discrete form.

6.3.2 Design and implementation of bandstop filters

Bandstop filters were designed using the standard methodology given in [124]. A fourth-order capacitively coupled [125] filter and a third-order directly coupled [126] filter, with narrow and moderate bandwidths respectively were designed. The capacitively coupled filter required extra biasing circuitry consisting of short-circuited quarter-wave transmission line of high impedance. On the other hand, the directly coupled filter afforded ease of tuning without an extra bias circuit since bias could be applied at either ports. The circuit for the capacitively coupled filter is shown in Figure 6.6 and the assembled bandstop filter is shown in Figure 6.7.

The circuit for the directly coupled filter is shown in Figure 6.8 and the assembled

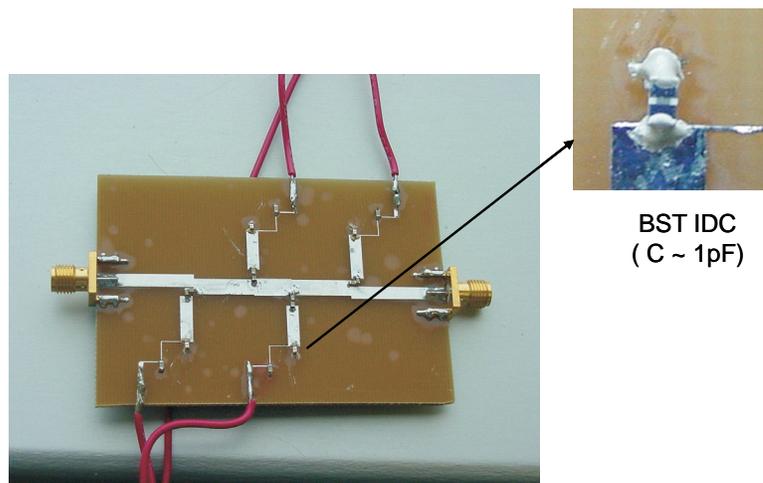


Figure 6.7: Assembled bandstop filter (capacitively coupled).

bandstop filter is shown in Figure 6.9. Both circuits were fabricated on a FR4 substrate with a dielectric thickness of 62 mils, dielectric constant of 4.6, loss tangent of 0.016 and 34 μm copper thickness. The patterns were etched using a standard PCB process.

6.3.3 Measured results and discussion

The filters were measured on a HP 8510C vector network analyzer after a full two-port calibration. The capacitively coupled filter was designed to operate in the range of 3.5–4.0 GHz. Four such filters were fabricated with the nominal value of the BST tuning capacitor as 1.0 pF. The results for three of them are shown below and are labelled as F1, F3, and F4. The filter F2 in this series did not work due to a capacitor short that was discovered after assembly. The filter F1 tuned from 3.69 GHz to 3.9 GHz with the application of 90 V bias. The BST varactor broke down at higher bias voltages. The depth of the notch was 16.0 dB at zero bias and increased to 19.5 dB at 90 V bias, see Figure 6.10. The increase in the depth of the notch is in part due to higher Q factor of the BST varactor at high bias voltages. The insertion loss in passband was < 2 dB.

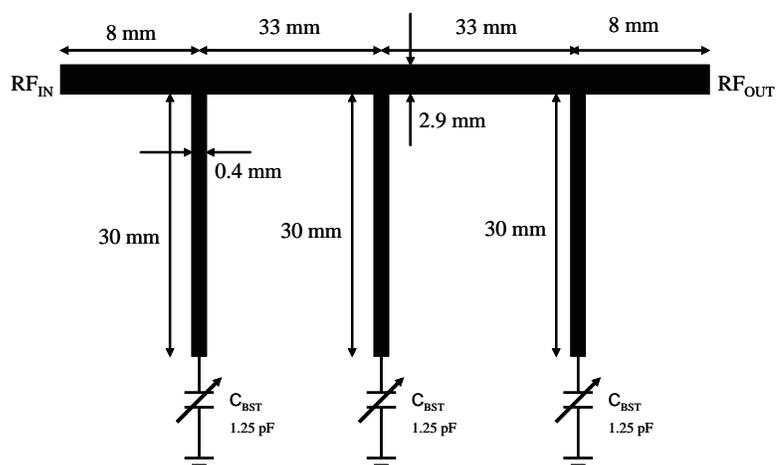


Figure 6.8: Schematic of the direct coupled narrowband bandstop filter.

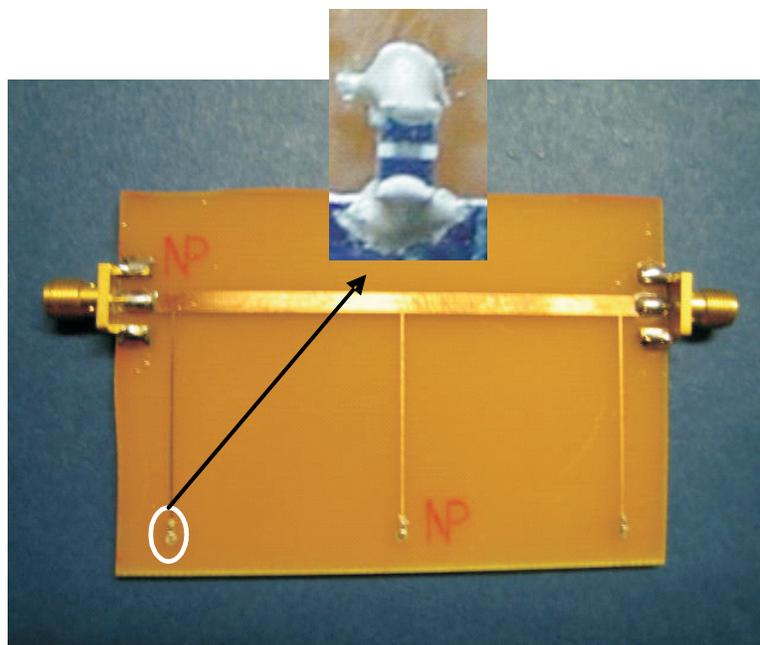


Figure 6.9: Assembled bandstop filter (direct coupled).

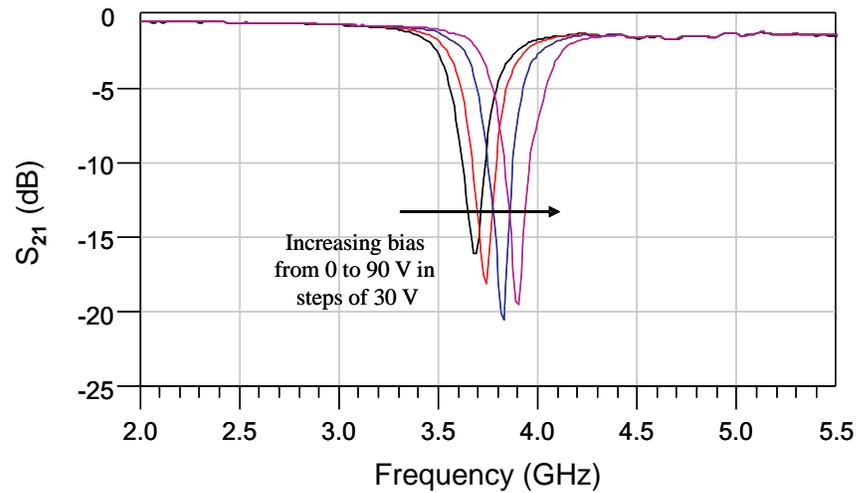


Figure 6.10: Measured S_{21} for capacitively coupled bandstop filter (F1), increasing bias from left to right.

The filter F3 tuned from 3.68 GHz to 3.86 GHz with 75 V bias. The depth of the notch at zero bias was 21.7 dB, about 5 dB more than the filter F1. The notch increased to 26.3 dB at 75 V bias, Figure 6.11. The tuning range, therefore was 4.9%.

The filter F4 showed the maximum tuning in the series. It tuned from 3.65 GHz to 3.99 GHz with 140 V bias, see Figure 6.12. The depth of the notch at zero bias was 18.0 dB but degraded to 12.0 dB as one of the BST varactor got open-circuited with higher bias voltages. The full tuning range was 9.5%. However, when tuning is considered only for bias voltages where all four BST varactors were functional, the tuning was 7.8% with 100 V bias and the depth of the notch was 26.9 dB. Overall, the results are quite promising in terms of tuning and may be increased further by optimally designing the filter and also reducing the gap size in the IDC varactors for higher tunability.

The third-order directly coupled filter consists of half-wave stubs shorted at one end. At the frequency of interest they provide attenuation poles, thus resulting in bandstop behavior. The 3-dB bandwidth of the filter was in the range of 40–50%. The filter lends itself naturally to biasing. The nominal value of BST varactors was 1.25 pF. The measured transmission and reflection data is shown in Figures 6.13 and 6.15 respectively. The tuning range was from 850 MHz to 1050 MHz with 140 V bias.

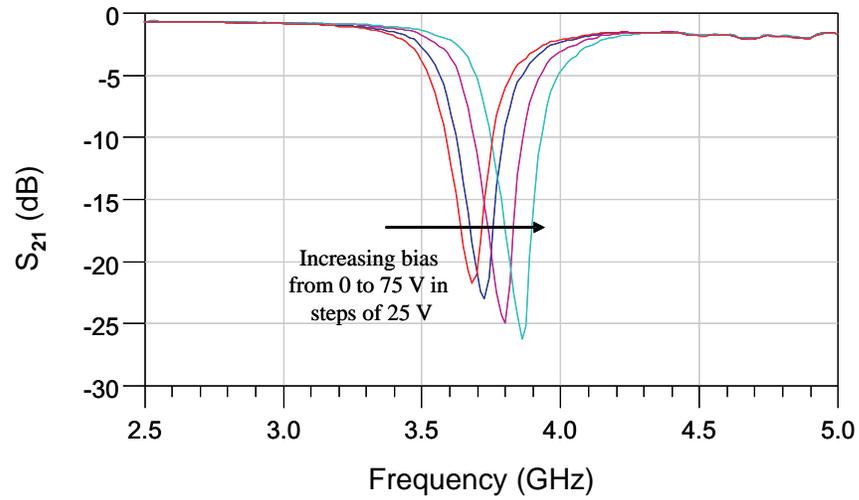


Figure 6.11: Measured S_{21} for capacitively coupled bandstop filter (F3), increasing bias from left to right.

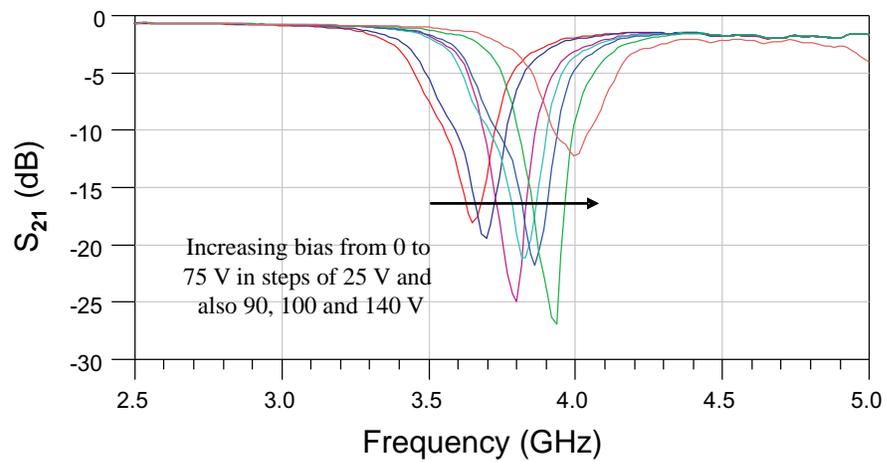


Figure 6.12: Measured S_{21} for capacitively coupled bandstop filter (F4), increasing bias from left to right.

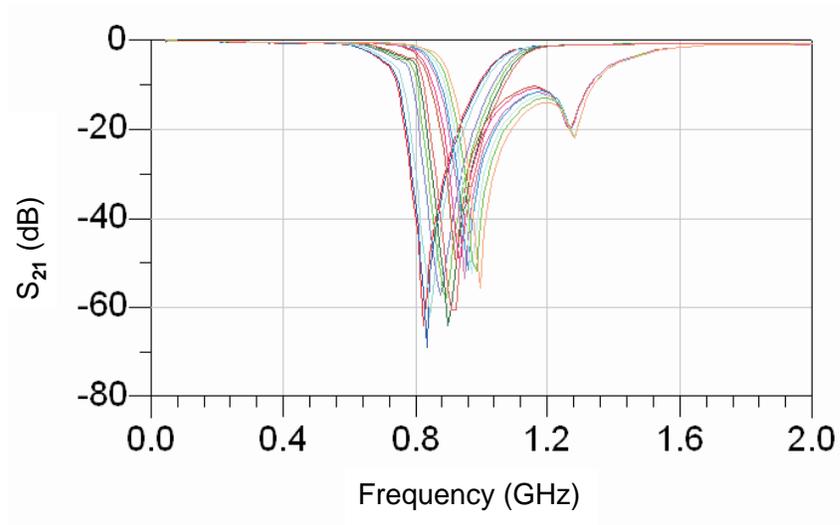


Figure 6.13: Measured S_{21} tuning data for direct coupled bandstop filter (F5) up to 140 V bias, increasing bias from left to right.

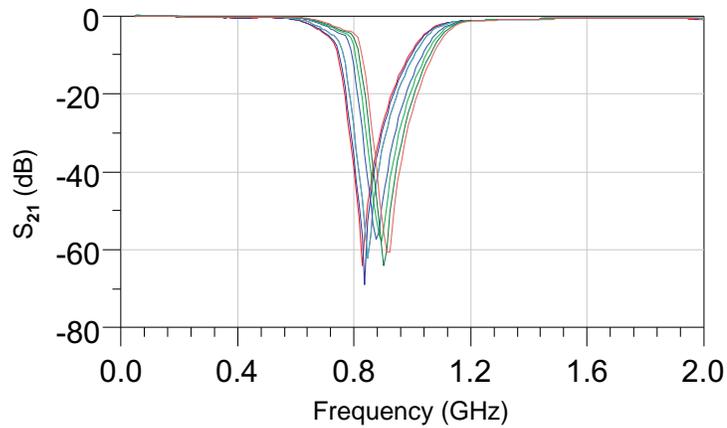


Figure 6.14: Measured S_{21} tuning data for direct coupled bandstop filter (F5) up to 50 V, increasing bias from left to right.

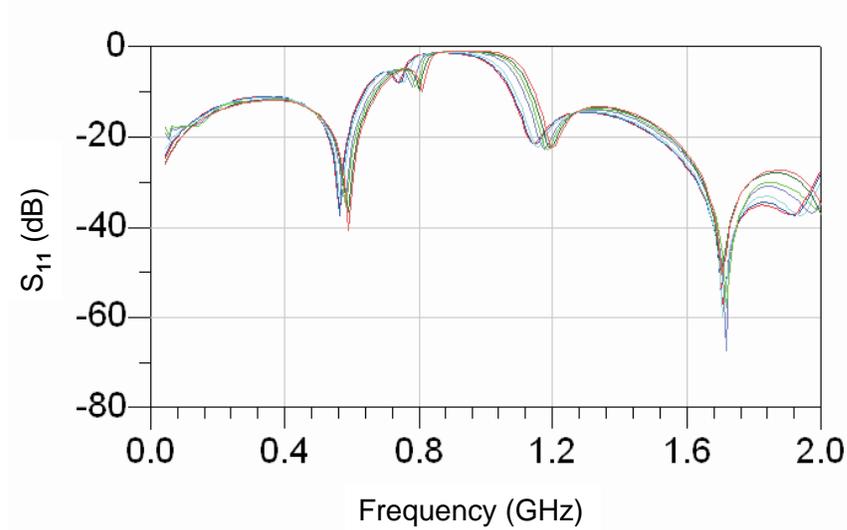


Figure 6.15: Measured S_{11} tuning data for direct coupled bandstop filter (F5) up to 50 V, increasing bias from left to right.

At the higher end of the bias range the one of the BST varactor got open-circuited. The full bias range showed a 22.5% tuning while the tuning range was 12.5% for 50 V with all varactors functional, see Figure 6.14. The insertion loss in the passband was < 1 dB. It must be noted that a higher tuning range comes at a price of wider 3-dB bandwidth of the filter compared to the capacitively coupled bandstop filter.

6.3.4 Summary

Thin Film barium strontium titanate (BST) varactors in discrete form have been used to design tunable bandstop filters. Two topologies have been implemented, a 3rd order filter using directly coupled varactor loaded stubs and a 4th order filter using capacitively coupled varactor loaded stubs. The filters were fabricated on a 62 mil thick FR-4 substrate and the BST varactors were fabricated on a polycrystalline alumina substrate ($\epsilon_r = 10.0$, $\tan\delta = 0.0001$) using sputtered BST film and copper metallization ($0.5 \mu\text{m}$) and subsequently diced to obtain discrete varactor with a standard 0603 footprint. The directly coupled and the capacitively coupled filters tuned in the range of 850–1050 MHz and 3.5–4.0 GHz respectively with application

of up to 140 V bias. It is expected that further design optimization and improved BST discrete varactor technology would lead to better tuning results and more reliable varactor performance. In the next section a bandpass filter on FR4 substrate and its tuning and nonlinear characterization will be presented.

6.4 Tunable bandpass filter on FR4

6.4.1 Introduction

Discrete Barium Strontium Titanate (BST) thin-film capacitors in industry standard 0603 footprint have been used to design a 2nd-order tunable combline bandpass filter on FR4 substrate. The filter showed a center frequency tuning of 22% from 2.14 GHz to 2.61 GHz upon application of 130 V (433 kV/cm) bias. The zero-bias insertion loss was 4.9 dB which decreased to 2.9 dB at the high bias state. The return loss was better than 11 dB over the tuning range. Nonlinear characterization of the filter using two-tone test and a digitally-modulated CDMA 2000 signal showed an IIP3 of +32 dBm and an ACPR of better than -50 dBc up to +26 dBm of input power, respectively.

6.4.2 Design and fabrication

A 2nd-order filter was designed based on a lowpass lumped element prototype with inverters. From the lowpass prototype an initial estimate of the inter-resonator couplings was first determined. The filter was constructed on an FR4 board with a substrate thickness of 62 mil (1.57 mm), dielectric constant of 4.6 and loss tangent of 0.016. With the knowledge of the coupling coefficients the electrical prototype was then converted to a physical layout using ADS [107]. Upon simulation, the resulting values of the loading capacitors were found to be 0.7 pF each. The nominal electrical length of the resonators was 45 degrees at the center frequency of the filter. The discrete BST varactors were attached at the end of the resonators using conductive

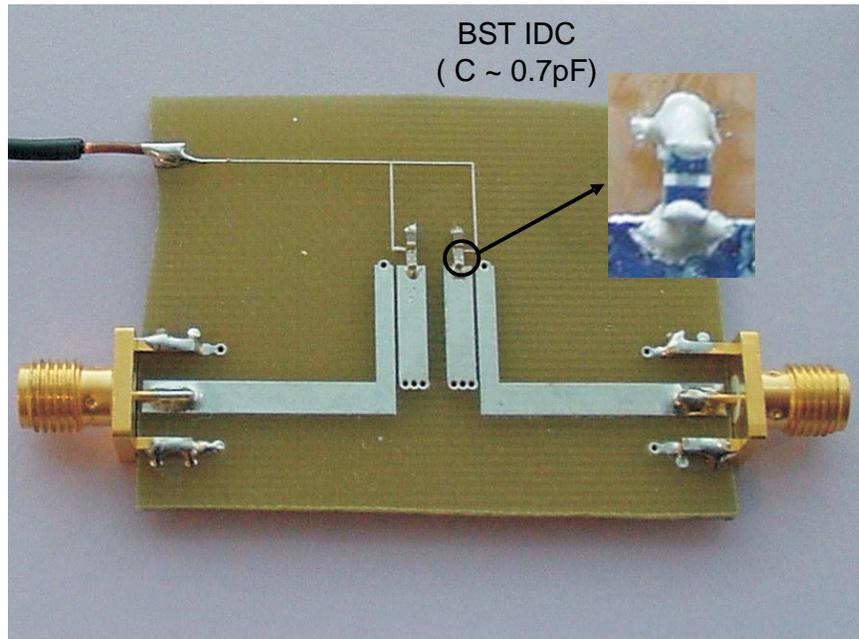


Figure 6.16: Assembled bandpass filter on FR4.

epoxy. The biasing circuitry consists of two discrete capacitors of high value (1 nF) and rated to 200 V. This ensures an RF short while providing a node for DC tuning. High impedance tuning lines were then connected to a DC power supply. The assembled bandpass filter is shown in Figure 6.16.

6.4.3 Measurement and characterization

The filter was measured on a HP 8510C vector network analyzer and bias was varied from 0 to 130 V using a HP 4142B DC source. The tuning response of the filter is shown in Figure 6.17. The zero bias insertion loss was 4.9 dB and the filter was centered at 2.14 GHz. At the high end of the tuning range, the center frequency moved to 2.61 GHz and the insertion loss improved to 2.9 dB. This is in part due to higher Q factor of the BST varactors with increasing bias and also due to better matching at lower capacitance values, see Figure 6.18. The Q factor of the BST varactors was estimated using a comparison of the measured and modelled data and

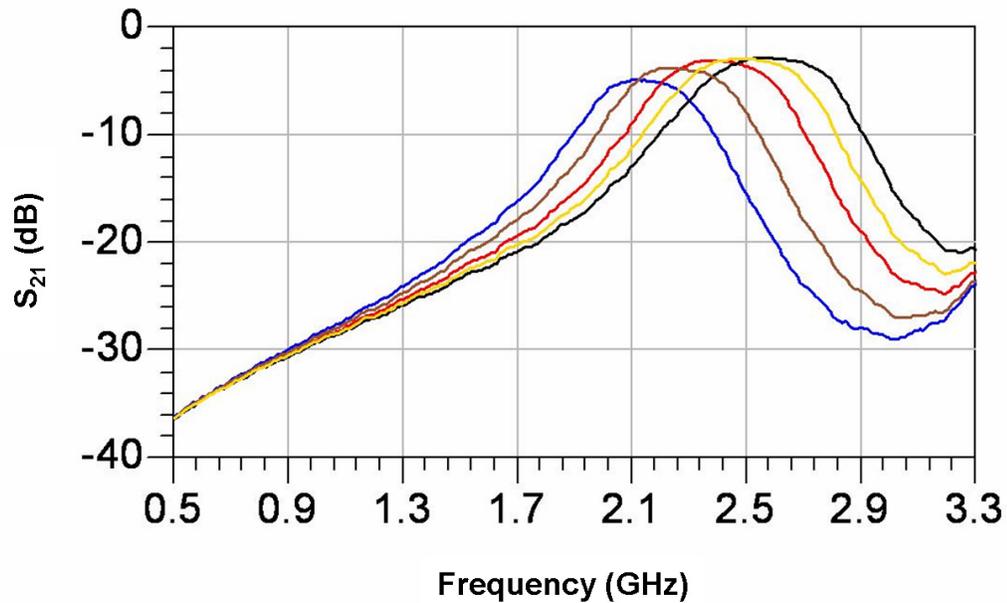


Figure 6.17: Measured S_{21} of the filter with applied bias; 0 V, 30 V, 60 V, 90 V, and 130 V bias from left to right.

was found to be approximately 20 in the operating range. The return loss of the filter was better than 11 dB over the entire tuning range. A comparison of the measured and modelled data at zero-bias is shown in Figure 6.19. The model holds equally well at other bias voltages. There is a slight deterioration in the upper passband due to the parasitics associated with the bias circuitry.

A summary of filter tuning data is shown in Table 6.1. The DC current was recorded at each bias point. The worst case total DC power consumption is $< 0.7 \mu\text{W}$. This compares very favorably with semiconductor varactor diodes where the power consumption is of the order of tens of microwatts.

6.4.4 Nonlinear characterization

As is evident from Figure 6.3, the BST varactor is nonlinear. The nonlinear characterization was done at 0 V bias which represents the worst case operating condition. The nonlinear characterization of the filter using a two-tone test and also

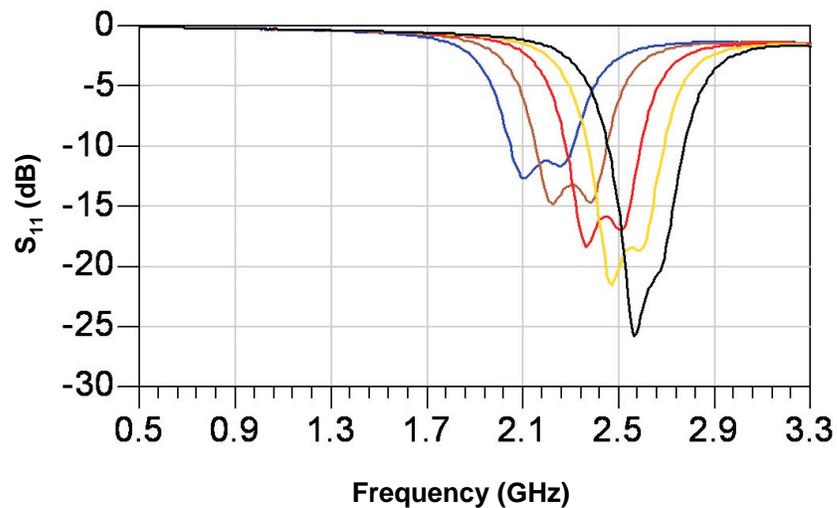


Figure 6.18: Measured S_{11} versus bias; 0 V, 30 V, 60 V, 90 V, and 130 V bias from left to right.

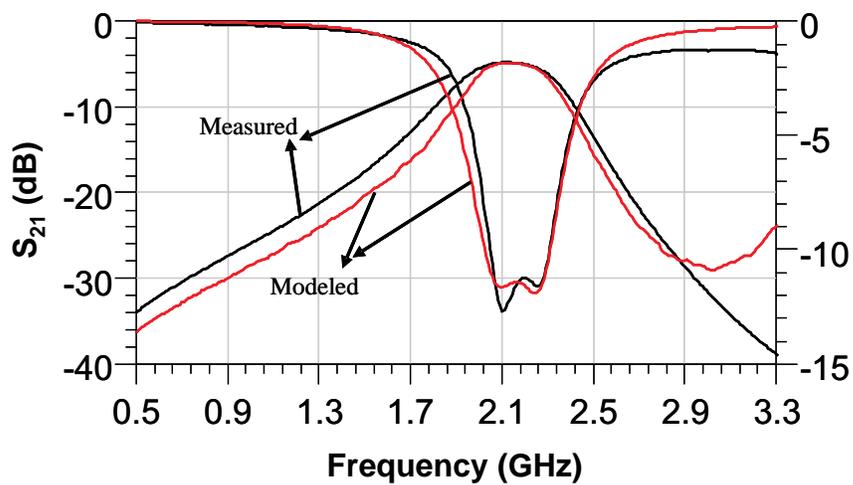


Figure 6.19: Comparison of measured and modelled data at zero bias.

Table 6.1: Summary of bandpass filter tuning

Bias Voltage (V)	Center Frequency (GHz)	Insertion Loss (dB)	Return Loss (dB)	DC Current (nA)
0	2.14	4.93	11.2	–
20	2.22	4.23	12.3	1.5
40	2.32	3.56	14.1	3.4
60	2.40	3.10	15.1	3.7
80	2.48	3.01	17.6	5.1
100	2.53	2.89	19.3	5.4
120	2.58	2.89	20.0	5.6
130	2.61	2.92	21.8	4.5

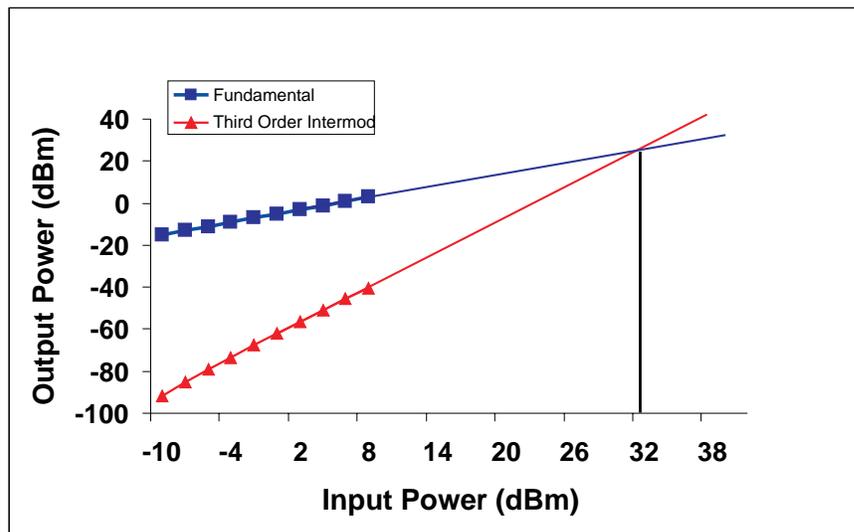


Figure 6.20: Two-tone intermodulation measurement of the filter at 0 V.

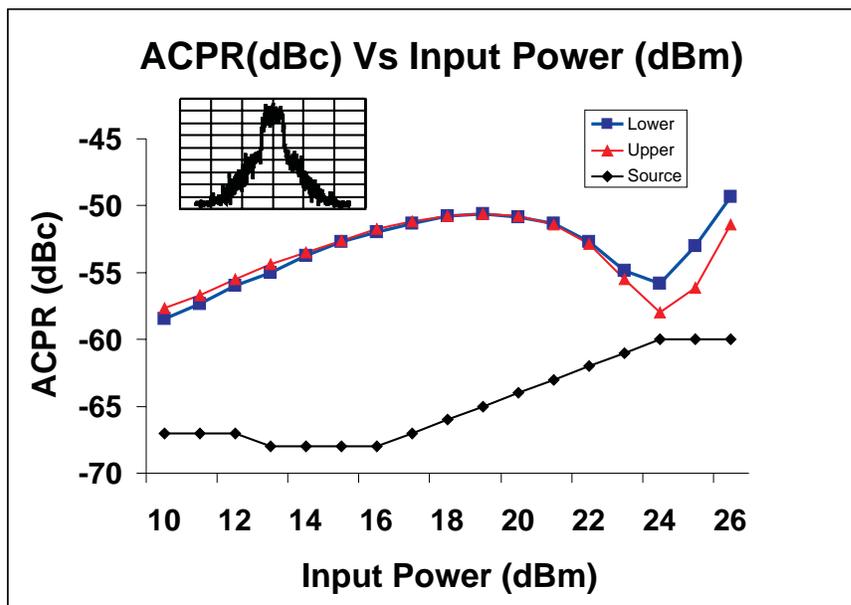


Figure 6.21: Adjacent Channel Power Ratio (ACPR) of the filter for a CDMA 2000 signal at 0 V. The source ACPR is that of the setup alone without the filter, for accurate measurement source ACPR must be 10 dBc below the ACPR of the device under test.

a digitally-modulated signal was carried out. The input power of the two tones was swept up to +8 dBm and the output power level of the tones and the intermodulation products was recorded. An IIP3 of +32 dBm was found from extrapolation, see Figure 6.20.

The filter was also characterized using a CDMA 2000 pilot signal with power levels up to +26 dBm. The ACPR was measured in a 30 kHz bandwidth at an offset of 750 kHz from the center frequency of 2.14 GHz. The ACPR was found to be better than -50 dBc, see Figure 6.21. The ACPR results are consistent with the measured IIP3 up to +18 dBm input power where higher order nonlinearity starts to cancel the third order component resulting in a distortion notch around +25 dBm input power. The 4:1 ACPR slope of the distortion characteristic after the notch is indicative of a fifth order nonlinearity; although, there is 3-dB of asymmetry implying that a baseband even order interaction term is present.

6.4.5 Filter performance and figure-of-merit

The performance of the tunable bandpass filter using discrete BST varactors will be evaluated in terms of the network transformation factor and the FOM. The filter tuned from 2.14 GHz to 2.61 GHz, resulting in 22% tuning of the center frequency. The FBW = 0.10, and IL = 2.9 for the second-order filter. To a good approximation the sum of g_i 's for a second-order filter is equal to 1.465 for a tchebychev lowpass prototype with 0.1 dB of ripple and Equation (5.3) can be modified to yield Equation (6.1).

$$Q_u = \frac{6.36}{(\text{IL})(\text{FBW})} \quad (6.1)$$

The unloaded Q of a single resonator in the combline filter was found to be 21.93. The frequency tuning ratio (f_r) of the filter was perviously found to be 1.22, hence, $\tau_{\text{NTF}} = 0.863$ and the FOM (K_τ) of the filter was calculated to be 4.82. The FOM of the filter is greater than the FOM of the tunable filters using integrated BST thin-film varactors on alumina and sapphire discussed earlier. It should be noted that the FOM does not take into account the shape factor and linearity of the filters. A more comprehensive figure-or-merit using those parameters is required for fair comparison. However, the FOM is a useful parameter for comparing filters with similar shape factor and linearity but designed using different network topologies and fabricated using different technologies.

6.4.6 Summary

A second-order tunable combline bandpass filter on FR4 substrate was presented. The center frequency tuning was found to be 22% for an applied electric field of 433 kV/cm (130 V bias). Nonlinear characterization of the filter showed an IIP3 of +32 dBm and an ACPR of better than -50 dBc for input power up to +26 dBm.

Table 6.2: Comparison of Tunable BST Filters

Author	Frequency/ Filter Order	Insertion Loss/IP3	Tunability @ Bias	Temp./ Substrate
Tombak <i>et al.</i> , NCSU (2001)	176–276 MHz/ Third-order	3.0 dB/ +19 dBm	57.0 % @ 6 V	298 K Si, discrete
Noren, (2004)	910–1230 MHz Second-order	6–7 dB	35.0%	298 K Discrete
Rahman <i>et al.</i> , Paratek (2004)	1656–1983 MHz Thrid-order	4.5 dB	19.7 %	298 K LTCC
Vendik <i>et al.</i> , (2003)	4400 MHz Third-order	7–15 dB	5.7 % @ 150 V	298 K MgO
Eriksson <i>et al.</i> , (2004)	900 MHz Second-order	1.6–4.7 dB	5.0 % 500 V	77 K KTO
Nath <i>et al.</i> , NCSU (2005)	2440-2880 MHz Third-order	3.3–5.1 dB +41 dBm	18.0% @ 200 V	298 K Sapphire
Nath <i>et al.</i> , NCSU (2005)	1600-2000 MHz Third-order	6.6–4.3 dB +38 dBm	25.0% @ 200 V	298 K Alumina
Nath <i>et al.</i> , NCSU (2006)	2140-2610 MHz Second-order	2.9–4.9 dB +32 dBm GHz	22.0 % @ 130 V	298 K Alumina,FR4

6.5 Conclusion

Discrete thin-film varactors in standard 0603 footprint have been designed, fabricated and characterized. Temperature characterization showed optimized performance at room temperature and acceptable performance over a range of temperatures from -170 °C to $+230$ °C. As an application, bandstop and bandpass filters on low-cost FR4 substrate were designed and characterized. The bandstop filter showed tuning up to 22% for the directly coupled filter and up to 9.5% for the capacitively coupled filter. The bandpass filter showed tuning of up to 22% with 2.9 dB of insertion loss with 130 V bias. Nonlinear characterization demonstrated that the filters have sufficient linearity to be used in frequency-agile front-ends. It is expected that the discrete BST thin-film interdigital varactor technology will prove to be a viable candidate for frequency-agile devices in the range of 1–6 GHz where it is advantageous to have thick transmission lines and the parasitics associated with the discrete varactor assembly can be tolerated. Finally, a comparison of tunable filter data pre-

sented in the previous chapters is compared with tunable filter data reported by other research groups on various substrates, see Table 6.2. BST tunable filters on sapphire, alumina, and FR4 substrate show tuning and loss characteristics comparable to or better than those reported by other researchers. Tunable filter on FR4 substrate has the highest tunability and lowest loss for any room temperature BST varactor based tunable filter reported till date in the literature. In the next chapter a tunable matching network and a dual-mode multi-band tunable patch antenna with independently tunable modes will be described.

Chapter 7

Tunable Matching Network and Dual-Mode Patch Antenna

7.1 Introduction

In this chapter a tunable matching network on alumina that matches a range of impedances from 10–30 Ω over a wide range of frequencies will be described. A dual-band tunable antenna is also introduced and characterized experimentally. The antenna has two orthogonal modes and both modes can be tuned independently. The two modes radiate in different directions. This allows wider frequency coverage, higher selectivity and larger coverage footprint.

7.2 Tunable matching network

7.2.1 Introduction

The widespread use of wireless communication devices necessitates the need for multi-band, multi-standard and multi-functional devices. Frequency agile components are required for such multi-functional systems. They need to be low cost, small size and light weight without compromising system performance. Various enabling technologies such as semiconductor, MEMS (microelectromechanical systems) and ferroelectric thin-film varactors have been explored for such tunable front ends.

With increasing functionality being added to portable wireless devices the power consumption and battery life is more important than ever before. The design of efficient power amplifiers (PA) is essential to reducing the power consumption and hence increasing the battery life and potentially reducing the size of the wireless device. The PA in a multi-band, multi-standard phone must operate efficiently across different frequency bands [127, 128, 129]. The two most common circuit configurations used are multiple power amplifiers optimized for each band and selected using switches and single broadband PA with tunable matching network either by using switches or varactors. Considerable work has been done in the area of MEMS based tunable matching networks using either MEMS switches or varactors [130, 131, 132, 133]. Though MEMS is a very promising technology; it still has very stringent packaging requirements and consequently higher cost. Reliability is also a concern. Semiconductor varactor based tunable matching networks [134, 135, 136] have been implemented by many researchers but they suffer from poor linearity performance.

Recently, a BST thin-film parallel plate varactor based tunable matching network at 900 MHz was demonstrated on sapphire [66]. The impedance transformer network was capable of transforming a 50Ω impedance to range of values between 13–29 Ω . In this chapter will present the design and characterization of tunable matching network using BST thin-film interdigital varactors on polycrystalline alumina substrate.

7.2.2 Design and implementation

The most convenient matching network designs are in the form of double or triple stub tuners [137]. They afford wide impedance coverage on the Smith Chart and also ease of fabrication. The latter is able to match any impedance on the Smith chart to a given reference impedance. Such impedance matching networks have been reported in the literature using MEMS and semiconductor varactors. There has been no report of a BST thin-film varactor based tunable matching network using stub tuners. The goal of this work was to demonstrate such a network. A matching network that transforms low output impedances of power amplifiers, typically in the range of 5–10 Ω , to 50 Ω reference impedance over a wider range of frequencies was designed. A double stub topology was chosen and design the implemented using the methodology outlined in [137, 7]. Shorted stubs were used and were loaded with BST varactors at one end to provide the match over the designed frequency range. The design was the optimized using the microwave circuit simulator, Agilent ADS 2004A. The simulation showed that impedances in the range of 5–30 Ω range could be matched to a 50 Ω reference impedance over a 400–500 MHz bandwidth at a center frequency of around 2–3 GHz.

The design was further optimized for maximum return loss at each frequency of operation and for manufacturability. It is noted that two BST varactors have important but different functions regarding the operation of the circuit. The varactor C_{b1} controls the shift in frequency while the varactor C_{b2} help optimize the return loss at each frequency of operation. Though a change in C_{b2} also changes the frequency of operation, the impedance change responsible for the bulk of the frequency shift is that of C_{b1} . The circuit parameters are shown in Figure 7.2. The fabrication of the matching network closely follows the process flow outlined in the previous section. A representative tuning curve of the BST varactor is shown in Figure 7.1. The varactor shows a 15% tuning (for 5 μm finger spacing) with an applied field of 35 V at 1 MHz. Loss tangent was 0.013 at 0 V and decreased to 0.007 at 35 V. The surface mount biasing capacitors, inductors, and the resistor were also attached using conductive epoxy. The matching network was conveniently assembled on a

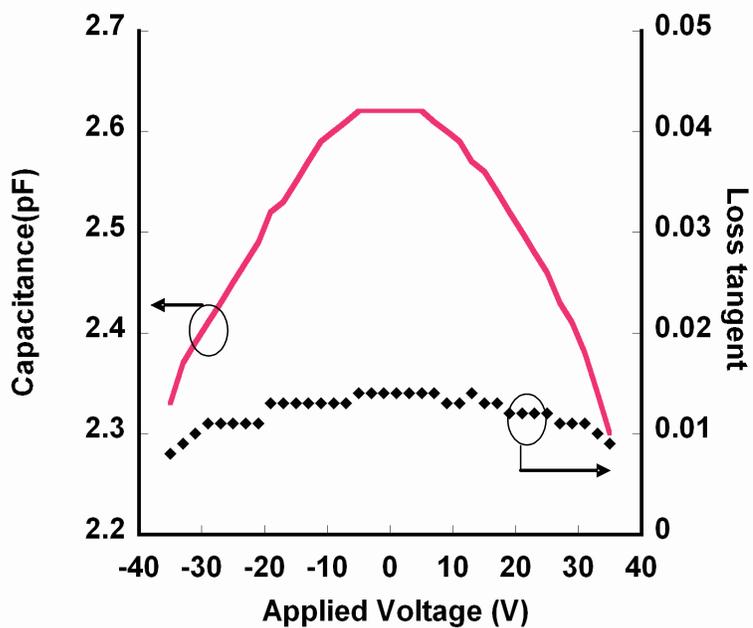


Figure 7.1: Representative tuning curve of the BST varactor.

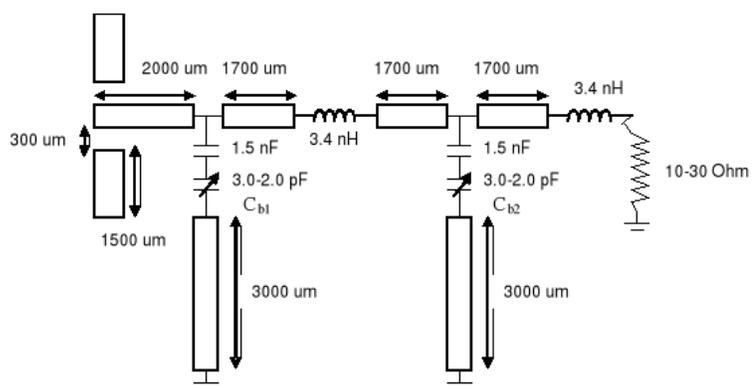


Figure 7.2: Schematic of the tunable matching network.

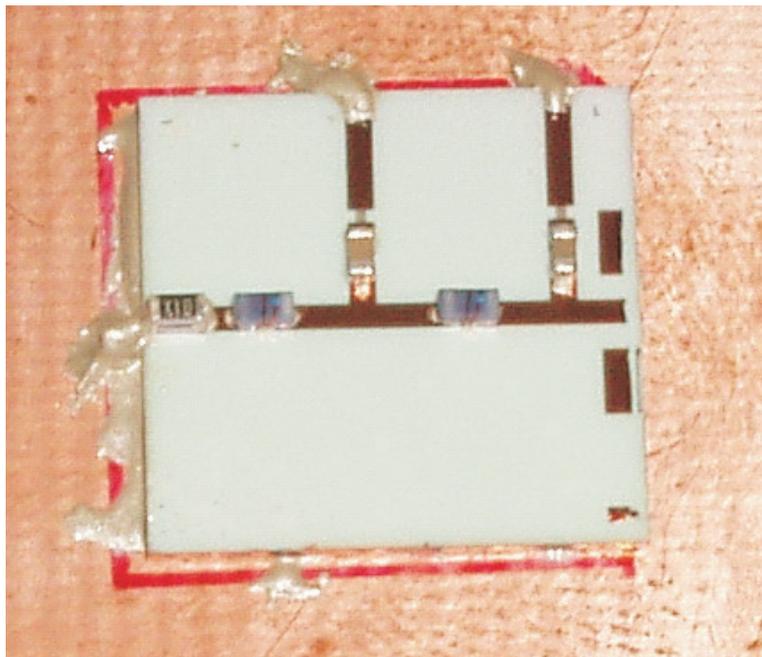


Figure 7.3: Assembled matching network.

high frequency laminate also using conductive epoxy. Since vias were not used, the edge of the two stubs was “ground-wrapped” over the edge to complete the electrical connection to the common ground plane. The assembled matching network is shown in Figure 7.3.

7.2.3 Measurement and results

A HP 8510C network analyzer and a 1250 μm pitch ground-signal-ground (GSG) probe from GGB Industries was used to characterize the matching network. One port open-short-load (OSL) calibration was performed using the CS-10 calibration substrate. HP 4142B was used to apply bias to the two BST varactors for tuning the matching network. Bias was applied using DC needle probes. The matching network under test is shown in Figure 7.4.

Measured tuning results for the tunable matching network under bias up to 200 V are shown in Figures 7.5 and 7.6. The matching network operates with better than

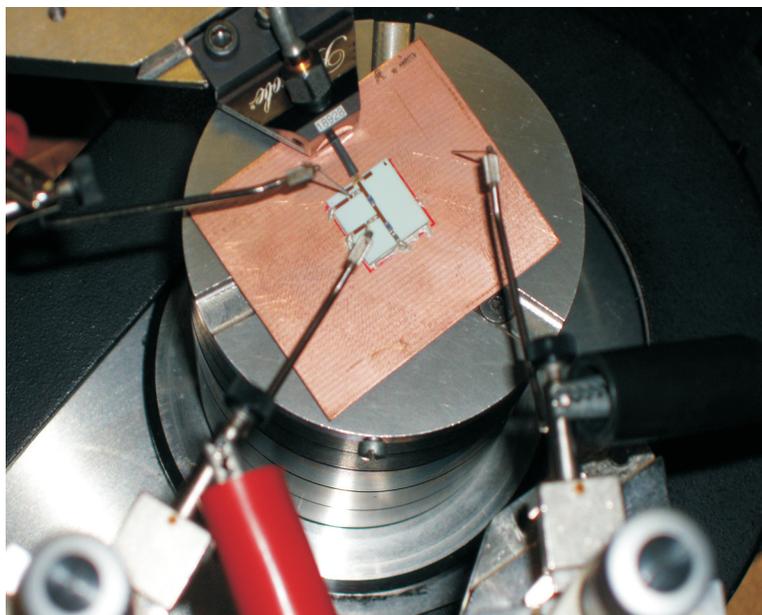


Figure 7.4: Matching network under test.

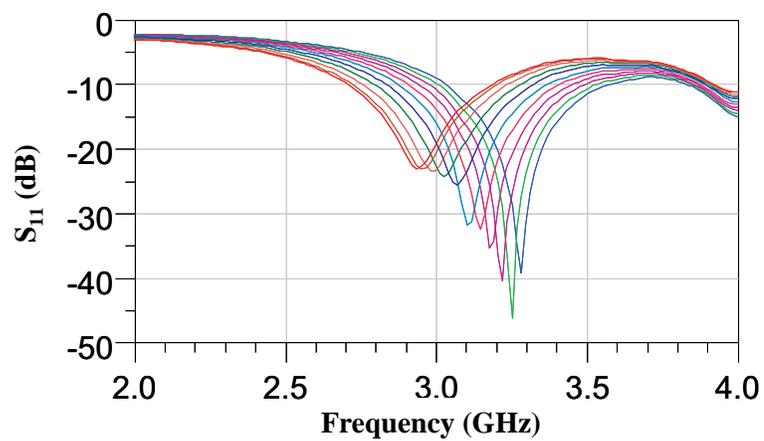


Figure 7.5: Measured S_{11} versus bias.

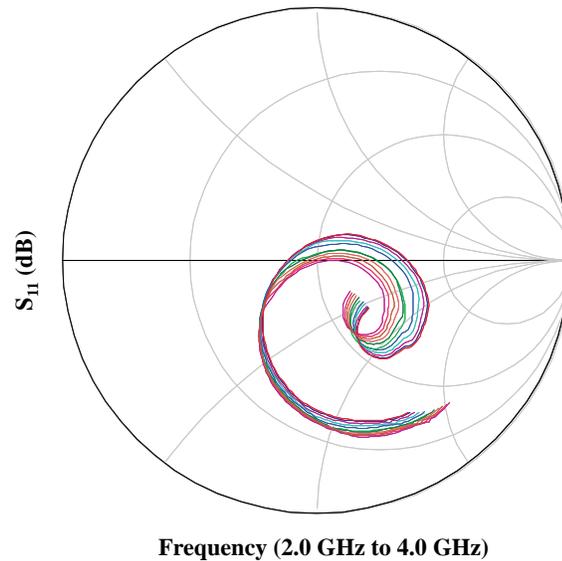


Figure 7.6: Measured S_{11} versus bias on a Smith[®] Chart.

23 dB of return loss over a 400 MHz bandwidth from 2.9 to 3.3 GHz. It was able to transform a 10Ω impedance to a 50Ω impedance over a wide range of frequencies.

7.2.4 Summary

A double-stub matching network using BST varactors that can transform low impedance values to a 50Ω environment with over 23 dB of matching and a wide range of frequencies was presented. This would enable efficient matching of a power amplifier with a low output impedance to antennas over a band of frequencies. For an extended tuning range this work could be extended to a triple stub tuner. In the next section a novel tunable antenna with two independently tunable modes of operation will be presented.

7.3 Dual-mode narrowband tunable antenna

7.3.1 Introduction

Reconfigurable antennas are very useful in multi-functional and multi-band wireless communication devices. They also find use in electronic surveillance, countermeasures and other defense applications. The properties of these antennas can be adapted in real time to achieve selectivity in frequency, bandwidth, polarization and gain. Compared to broadband antennas, tunable antennas offer certain distinct advantages. They have a small footprint and have similar radiation pattern and gain for all frequencies of operation. They offer judicious use of the electromagnetic spectrum and their frequency selectivity is useful for reducing co-site interference and jamming. Furthermore a reconfigurable narrowband antenna can also enable low power transceivers by potentially eliminating the losses in the duplexer. An alternative to a reconfigurable antennas is a multi-frequency or broadband antenna. Many techniques for the design for broadband antennas have been reported in literature [139, 140, 141]. While broadband or multi-band antennas do cover a range for frequencies, they are inherently less selective than fixed frequency antennas. This degrades the selectivity at the front- end. Thus a narrowband tunable antenna is the ideal solution and offers the best of both worlds in terms of selectivity and frequency coverage.

In the past tunable antennas have been fabricated by loading a microstrip patch antenna with varactors. The tuning can either be voltage controlled or optically controlled. Since the antenna is reactively loaded, the resonant frequency of the antenna can be changed by changing the reactance. These implementations use discrete components such as PIN diodes, varactor diodes or switches to vary the resonant frequency. These methods introduce additional manufacturing steps, increasing cost and component count while at the same time reducing reliability. It is desirable to have a process that allows the fabrication of reconfigurable antennas in a monolithic fashion.

A reconfigurable antenna with integrated varactors and a radiating metallic patch was designed and characterized. The antenna covers the 3.1–3.4 GHz band and can

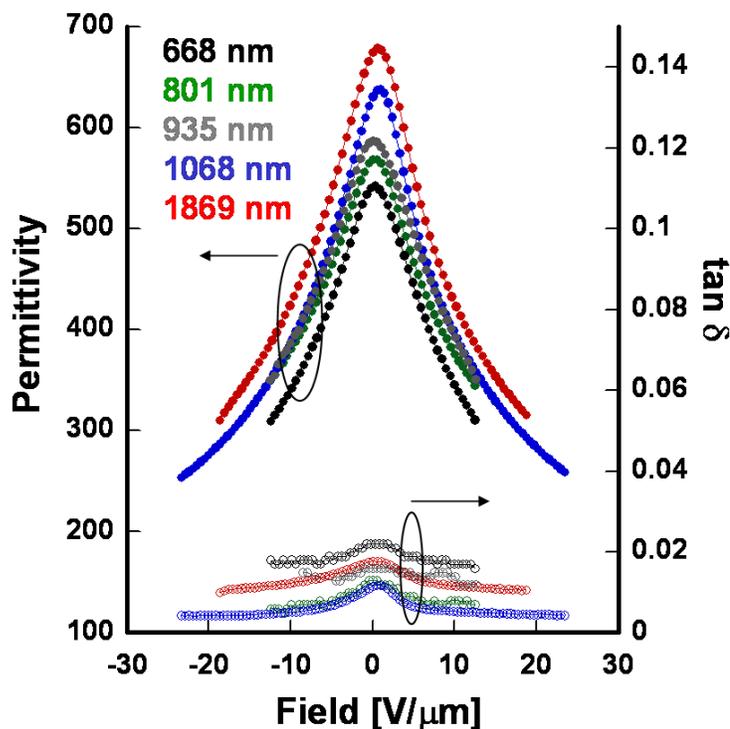


Figure 7.7: C-V curve for BST MIM varactor on Copper foil (1/2 oz.) for various thicknesses.

be continuously tuned over the entire frequency range. The radiation pattern and gain of the tunable antenna is also presented.

7.3.2 Materials and fabrication

BST interdigital varactors on alumina has been previously used to fabricate frequency-agile devices. This chapter will present BST MIM varactors on copper foil which were used to fabricate a tunable antenna. Typical C-V curve for BST MIM varactors on industry standard copper foil is shown in Figure 7.7.

BST has been known to form Schottky barriers with the electrodes and this leads to leakage current, thereby increasing losses. Also the interface between BST and metal affects the loss tangent of the thin-film and often high temperature (600–800 °C) annealing is required to obtain low loss dielectric films. This high temperature

processing requirement precludes the use of a variety of metals and other substrates and is too restrictive from a process view point. Various researchers have attempted to solve this thick metallization problem by using electrodes of noble metals (Pt, W etc) and oxides of Iridium. The usefulness of this approach is debatable as electrode thicknesses of more than 1–2 μm are difficult to achieve in practice and the conductivities of these electrodes are about 5–10 times lower than that of Cu, Ag etc. Hence it is highly desirable to have a process that allows low temperature steps and thick electrodes. Such a process has been developed and it is now possible to fabricate BST thin-film on copper foil as thick as 20–30 μm and does not require a high temperature anneal [138]. The BST on Cu foil can then be patterned as desired and the combination can then be laminated onto a substrate of choice to yield the required antenna circuitry. In order to promote adhesion and improve reliability an in-house capability to grow copper foil of the order of 10–20 μm was developed and these will be referred to as “ultra-foils” due to their smooth surface compared to off-the-shelf copper foil. Typical C-V results for BST thin-film on ultra-foil is shown in Figure 7.8.

7.3.3 Design and implementation

A tunable microstrip patch antenna was designed and tested as a proof of concept. The tunable antenna was designed using analytic microstrip antenna design formulae available in the literature [142, 143, 144] and the design was verified using Sonnet [145], a 3D planar electromagnetic simulator, and HFSS [146]. Standard design methodology published in the literature was used to design a co-axial line-fed microstrip patch antenna [147, 148]. This design represents a departure from the design methodology commonly used for tunable antennas in the literature. Most researchers use the radiating patch of the antenna to attach the varactors. The non-radiating edge of the antenna was used instead. This excites an additional mode (transverse mode) which can be tuned independently of the fundamental mode corresponding to the length of the antenna. This methodology offers greater design flexibility and wider frequency coverage. The antenna could also be loaded at both the radiating and the non-radiating edges, resulting in two independently tunable modes. This new

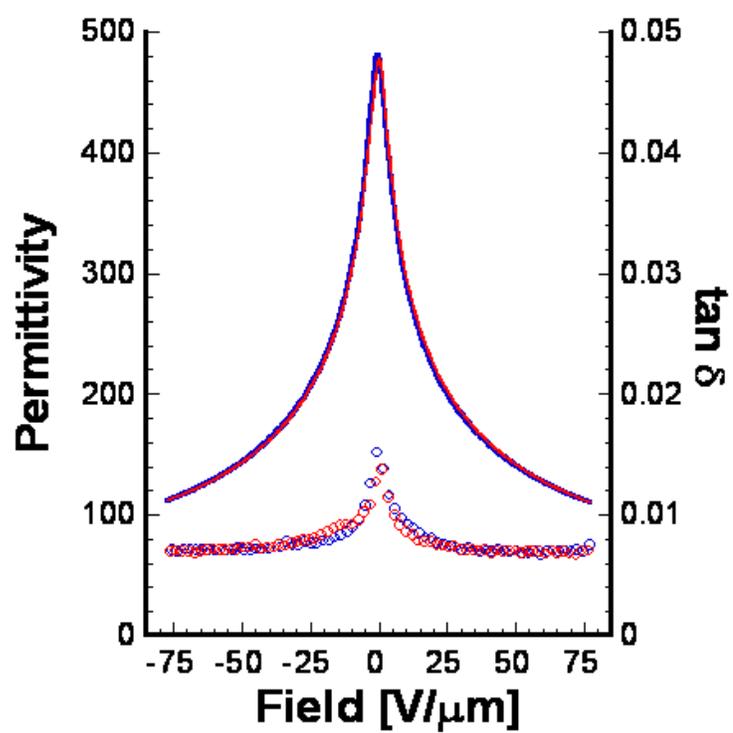


Figure 7.8: C-V data from a shadow masked Pt MIM structure on a 450 nm BST film deposited on a Zn treated ultra-foil substrate, solid line: permittivity, open circles: loss tangent.

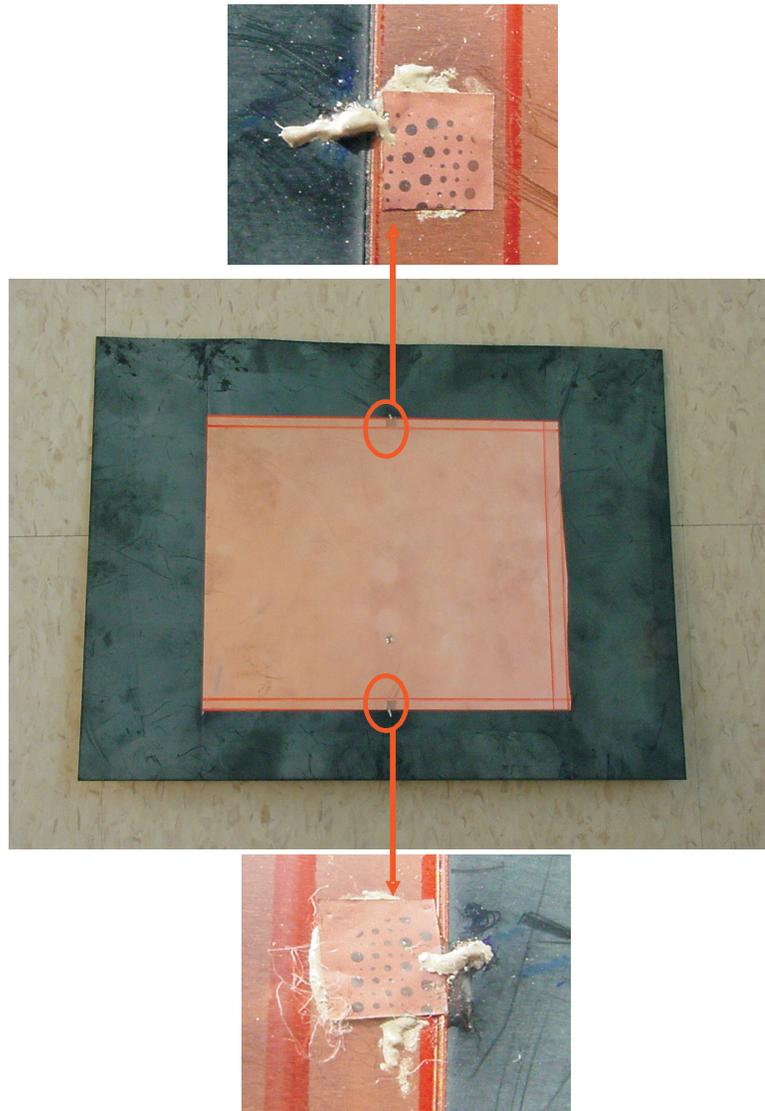


Figure 7.9: Assembled tunable patch antenna using BST MIM varactor on copper foil.

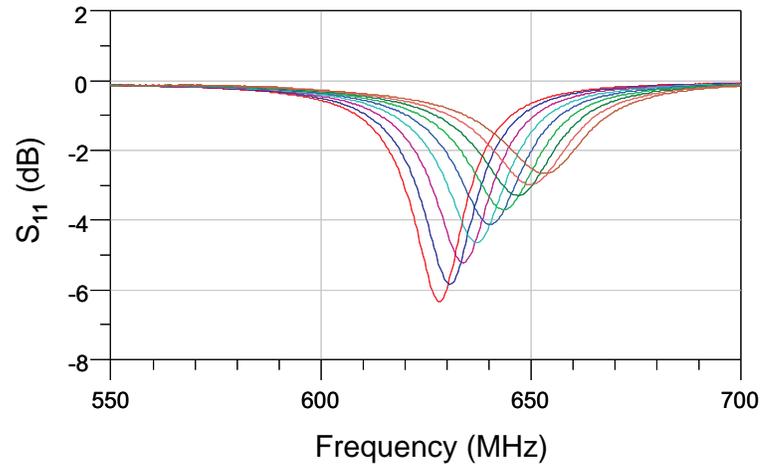


Figure 7.10: Measured S_{11} for patch antenna using BST MIM varactor on copper foil. Increasing bias from left to right, 0 to 40 V in steps of 5 V.

antenna design concept was verified using Sonnet®, both modes were found to be independent of each other. The gain of the transverse mode is slight lower than that of the fundamental mode but still high enough to be of practical use. Two antenna designs were implemented, one with BST MIM varactors on the radiating edge and one with discrete BST IDC varactors on the non-radiating edge.

The antenna with BST MIM varactor loaded on the radiating edge of the patch will be described now. A low dielectric constant patch ($\epsilon_r=2.6$) was used to improve gain and efficiency. The antennas dimension at $f = 680$ MHz was found to be $L = 15$ cm, $W = 18$ cm. The distance of the feed from the center was $L/6$. The return loss of the antenna was measured on a HP 8510C Network Analyzer and the resonant frequency was found to vary from 628.5 MHz to 653.2 MHz with 40 V bias (Figure 7.10). The return loss was 6.4 dB at zero bias and degraded to 2.66 dB at 40 V bias. It is believed that the poor performance of the antenna was due to the integration method employed. As seen in Figure 7.9 epoxy attachment method was used and it introduced additional parasitics which degraded the antenna performance. This issue was addressed in a subsequent design in which discrete BST varactor were used.

The BST IDC loaded antenna has an instantaneous bandwidth of less than 1% and can be continuously tuned over a 240 MHz bandwidth. The bandwidth is small

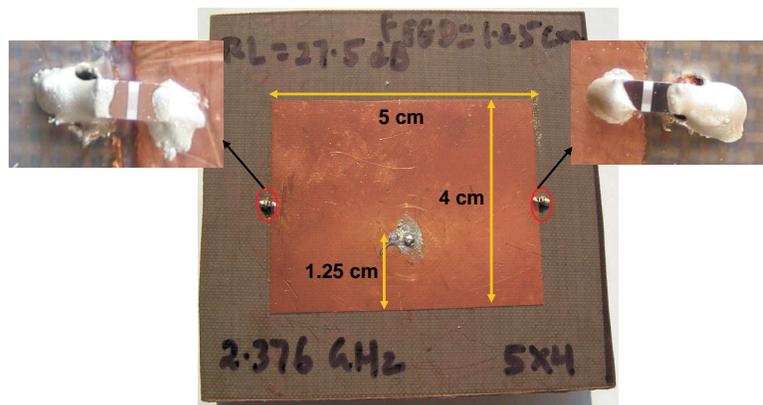


Figure 7.11: Assembled tunable patch antenna loaded with BST IDC varactor on alumina.

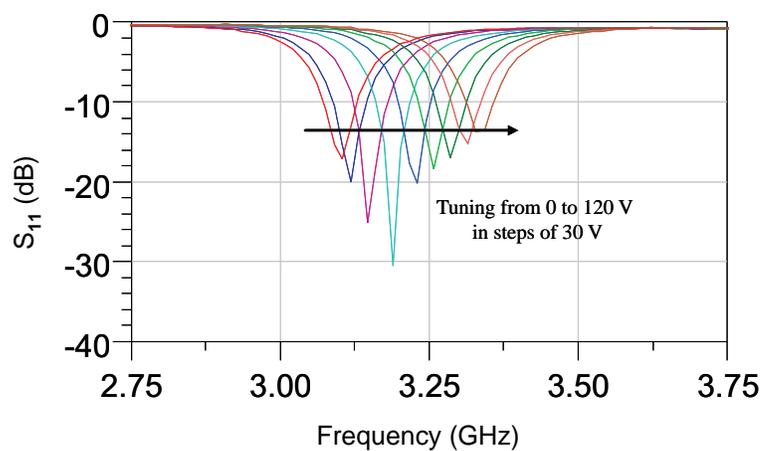


Figure 7.12: Measured S_{11} for patch antenna loaded with discrete BST IDC varactor on alumina; expanded frequency range.

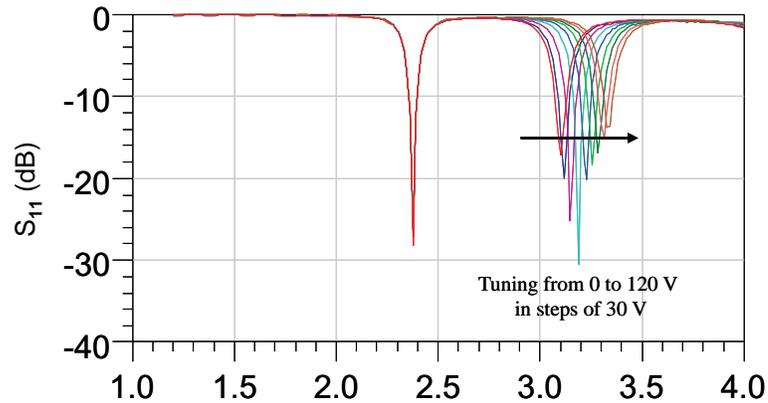


Figure 7.13: Measured S_{11} for patch antenna loaded with discrete BST IDC varactor on alumina, the non-tunable mode at 2.4 GHz and the transverse tunable mode (3.1–3.4 GHz) can be clearly seen.

since it is well-known that microstrip patch antennas are narrowband radiators. This feature is desirable for providing interference rejection at the front-end of a receiver. The antenna was designed for a fundamental radiation mode at 2.4 GHz and an additional transverse mode at 3.1 GHz. The antenna was loaded with varactors at the non-radiating edge in order to tune the transverse mode only. The antennas dimension at $f = 2.4$ GHz was found to be $L = 4$ cm, $W = 5$ cm. The distance of the feed from the center was 0.75 cm. The fabricated antenna is shown in Figure 7.11. The antenna return loss was measured using a network analyzer and it showed a return loss of greater than 13 dB for all bias voltages. The design closely matched the EM simulation to within 1 dB. The slight discrepancy was due to the fact that the inductance and capacitance associated with the coaxial feed was not taken into account in the EM simulation. The zero bias frequency was 3140 MHz and it tuned to 3380 MHz with 120 V bias. The observed tuning range was 7.7%, and the absolute tuning bandwidth was 240 MHz, see Figure 7.12. The frequency response of the antenna showing both the fixed frequency mode and the tunable mode is shown in Figure 7.13

A semiconductor varactor loaded antenna was also designed to demonstrate the full range of the transverse tunable mode. The varactors were attached to the non-radiating edge of the antenna as in the case of the BST varactor loaded antenna

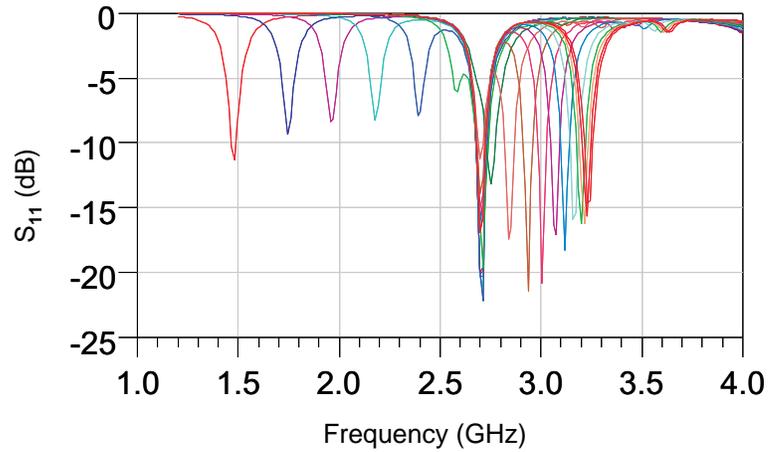


Figure 7.14: Measured S_{11} for patch antenna loaded with semiconductor varactor, full tuning range

discussed earlier. Measured results are shown in Figures 7.14 and 7.15. The tunable mode is located at 1.5 GHz for zero bias and the non-tunable mode is located at 2.7 GHz. With increasing bias, the capacitance decreases and hence the resonant frequency of the tunable mode goes up. The tunable mode crosses the fixed frequency mode and moves beyond it at high end of the bias range without affecting the fixed frequency mode (Figure 7.15).

7.3.4 Gain and radiation pattern

Due to the lack of an anechoic chamber, the gain and radiation pattern of the antenna was measured in free space (lab environment). The antenna test setup is shown in Figure 7.16. It consists of a reference antenna with a known gain and a automated turn table that enables data to be recorded in azimuth and elevation. A vector network analyzer and Fris's transmission formula is used to calculate the gain. Radiation pattern is plotted using post-processing routines in Matlab[®]. A conventional microstrip patch was measured to verify the accuracy of the setup and results were close to the expected gain from analytic calculations and EM simulation.

The measured gain and amplitude plot for the BST interdigital varactor loaded tunable antenna is shown in Figures 7.17 and 7.18 respectively. The gain of the

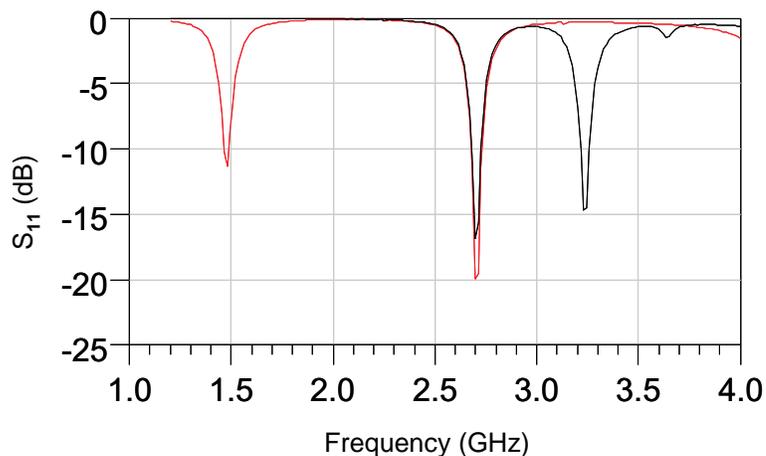


Figure 7.15: Measured S_{11} for patch antenna loaded with semiconductor varactor at zero bias and 14.5 V bias, the non-tunable mode is located at 2.7 GHz and the tunable mode tunes from 1.5 GHz to 3.25 GHz

antennas is approximately 2 dBi. Though gain is 3–4 dBi lower than that predicted by electromagnetic simulation, the mode is clearly a radiating mode. It is believed the lower measured gain is due to reflections from metal cabinets in the direction of maximum gain.

7.3.5 Summary

Narrowband antennas can provide a certain degree of selectivity upfront before the signal reaches the RF/Analog front end. By a judicious choice of the IF frequency and receiver architecture the antennas can augment the image rejection provided on-chip by as much as 20–30 dB. This is particularly true in case of hybrid receiver architecture which combines the benefits of heterodyne (superior performance) and homodyne (greater integration) receiver architectures. In this case the LO emissions are out of band and is suppressed by the selectivity of the antenna, further more the image frequency is positioned such that the antennas and the pre-select filter provide adequate image rejection. This eliminates the need for a separate image reject filter, saving cost and board space and leading to greater integration. Enabling technologies for such narrowband antenna and experimental results have been presented. It is



Figure 7.16: Measurement setup for antenna characterization.

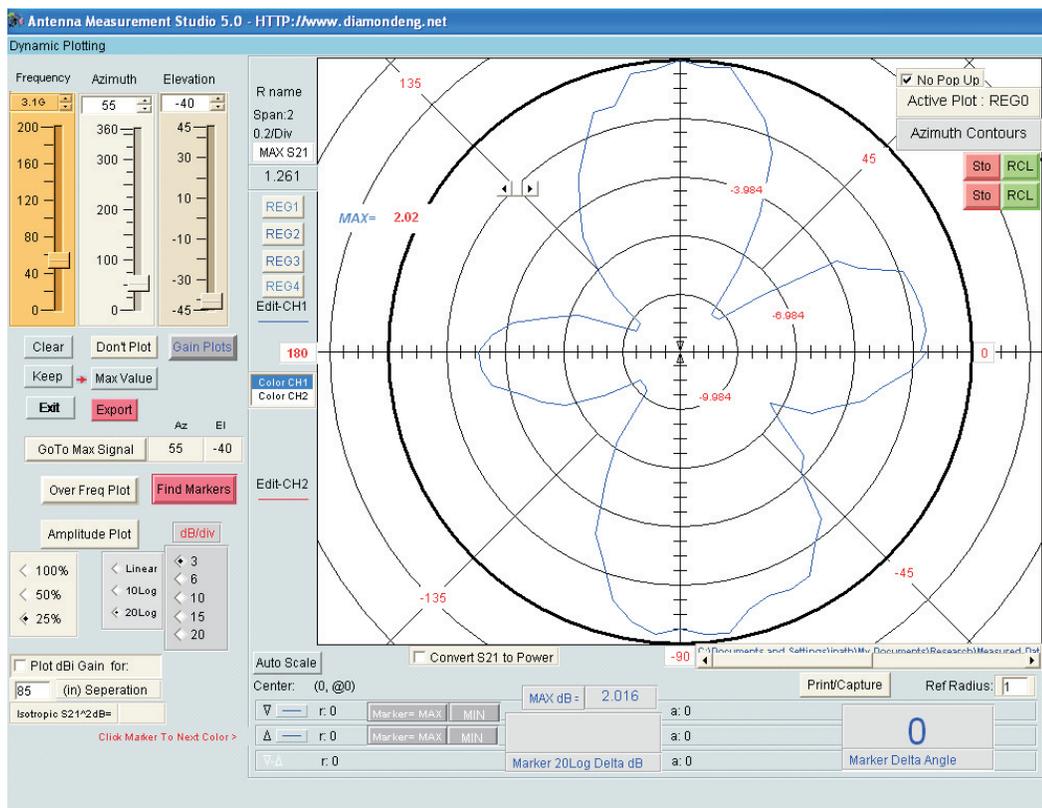


Figure 7.17: Gain of the tunable antenna, 2 dBi at 3.1 GHz

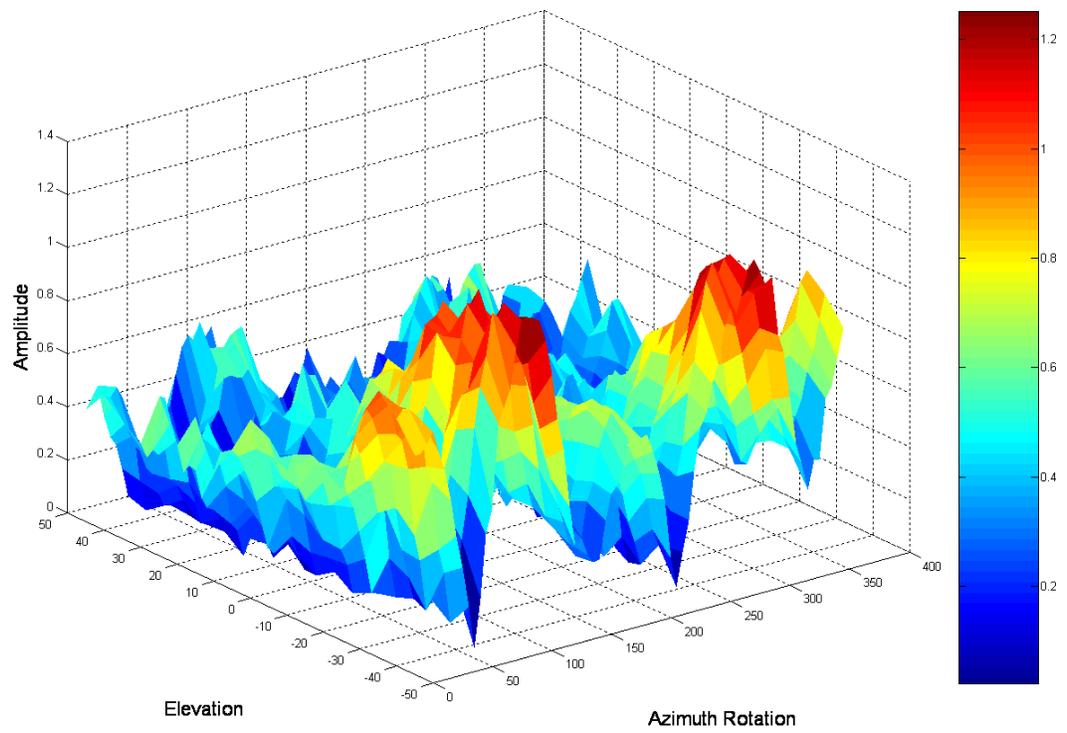


Figure 7.18: Amplitude plot of the tunable antenna at 3.1 GHz, two distinct lobes are evident in the plot corresponding to the polar gain plot.

expected to be a viable solution for highly selective narrow-band antennas.

7.4 Conclusion

A tunable matching network was presented. It provides matching of low output impedance power amplifier to antennas, thus enabling efficient power transfer. The matching network was demonstrated on alumina and a 400 MHz operational bandwidth with over 23 dB of matching was demonstrated. A narrow-band reconfigurable antenna was also presented. Over 240 MHz of tuning bandwidth was demonstrated with good return loss over the tuning range. The instantaneous bandwidth of $< 1\%$ provides high selectivity at the front-end.

A narrow band reconfigurable antenna has numerous applications in multi-band, multi-functional communication systems. With increasing functionality being added to communication devices and a plethora of wireless standards in use, multi-band operation is a must for today's antennas. It is not uncommon to find quad-band transceivers in today's "world phone" interfaced to quad-band antennas. Such antennas have been available on the market for a long time but they have certain inherent limitations. They do not have good matching characteristics over different frequency bands. While cost effective, another limitation of multi-band antennas is their detuning when held in proximity to the body. It is common to observe resonance shifts completely out of band with some embedded cellular handset antennas. When additional multi-band operation is required, the multi-band antenna ceases to work an effective electromagnetic transducer. The solution to this problem is to have narrow band reconfigurable antennas which dynamically tune their frequency of operation to provide a truly intelligent RF front-end. Such a narrow-band antenna maintains its characteristics (gain, return loss, directivity etc.) over the entire frequency of operation, enabling a better communication link. A reactively loaded patch can also be used for polarization diversity. This is possible by changing the capacitance which then changes the polarization of the radiated waves. Polarization diversity is particularly useful for increasing the capacity of wireless communication networks. This is

possible since it can boost the C/I ratio and hence increase capacity. By the same token the antenna can also be used for TDMA and frequency hopping applications.

In the final chapter the implications of the research work presented in this dissertation will be discussed and directions for future work will also be presented.

Chapter 8

Conclusion and Future Work

8.1 Summary of research and original contributions

This dissertation investigated the tuning of distributed resonators using lumped varactors. Fundamental results on the trade-off between tunability and Q factor in resonant systems were formulated. The concept of a network transformation factor (τ_{NTF}) was introduced. It enables the evaluation of different network topologies in terms of the maximum achievable tunability, thus guiding circuit and system development. A figure-of-merit (K_{τ}) was also formulated to quantify the trade-off between Q and tunability. These parameters enable the design of optimized frequency-agile systems. Two different resonator designs were characterized to illustrate the concepts introduced. Tunable filters and antennas have also been designed with tunability close to the maximum achievable limit.

It has been demonstrated that even with limited tuning ratio (2:1 or less) of the varactor, substantial tuning range can be achieved for frequency-agile resonators utilizing such a varactor. In addition, the overall Q of the resonator does not degrade

significantly. For 2:1 tuning ratio of the capacitor, the optimized resonator design showed 22% frequency tuning and a Q factor of 30. Though the Q of the resonator design with lower tuning was higher by 30%, the optimized design achieved 75% more tuning. Overall, the optimized design had a better FOM. The total Q factor of the transmission line and varactor combination was found to be more than that of the varactor alone. Such an increase in Q was achieved by judiciously placing the capacitor so that its contribution to the total loss is minimal while at the same time its reactance change determines tuning. The concepts introduced here can be utilized for judiciously choosing tuning elements and network topology for optimized system performance. In particular, a ferroelectric varactor with limited tuning and Q in the range of 50–100 could be used to load a high Q ceramic of suspended stripline resonator to achieve a total overall Q factor in the range of 200–400 while simultaneously achieving significant tuning range.

An intrinsic loss extraction technique was introduced which enables technology development by facilitating the material loss parameters to be determined in a simple and straightforward manner. This is accomplished by forcing ideal lossless impedance matching at the input and output ports. The transmission factor calculated using this method includes only the physical loss in the device itself. This represents the minimum insertion loss that can be achieved for a given technology. A $75\ \Omega$ fifth-order filter was characterized to illustrate the concept and the methodology of intrinsic loss extraction technique. Applications include determination of intrinsic loss in materials whose dielectric properties are as yet unknown or difficult to determine otherwise.

A significant part of this research work also focused on the characterization and optimization of a BST thin-film process on polycrystalline alumina using copper metallization. Introduction of a thin layer of chromium as a low loss adhesion layer between alumina and BST thin-film and the optimization of copper metallization process for achieving low series resistance of BST varactors have been instrumental in the design of BST-based frequency-agile systems. Q factor and tunability of BST IDC varactors on alumina were comparable to or better than results published in the literature for both IDC and MIM configurations fabricated on more expensive single crystalline substrates. For a 0.4 pF capacitor, Q factor of 30 at 26 GHz was obtained.

A varactor tuning ratio of 1.7:1 was obtained with 35 V bias or 115 kV/cm bias field. Use of alumina opens up the possibility of monolithic integration of BST-based devices with other microwave circuits fabricated on alumina.

One of the most fruitful contributions was the design and implementation of discrete BST varactors on alumina. This allows the design of frequency-agile systems using heterogenous technologies but assembled in a homogeneous fashion. As a result, the lithographic challenge of fabricating varactors with high-aspect ratio metallization was solved in a novel way. This also allows system design to be modular thus leading to rapid integration of various technologies. It is envisioned that discrete BST varactor would be useful in VCOs, filters, phase shifters, matching networks and antennas up to 10 GHz.

Using both integrated and discrete BST varactor technology frequency-agile band-pass filters were designed and implemented. The filters on alumina and FR4 substrate were the first ones reported using BST varactor technology on alumina and using copper metallization. The insertion loss (2.9 dB on FR4 and 3.5 dB on alumina) achieved is also the lowest reported till date. Center frequency tuning of 25% was obtained for 2:1 varactor tuning, demonstrating optimized design. Nonlinear characterization of the filters demonstrated their suitability for use in frequency-agile systems. IIP3 in the range of 32–41 dBm and ACPR in the range of -50 dBc to -55 dBc for +26 dBm of input power was obtained. A tunable matching network and a narrowband dual-mode tunable antenna using BST varactors was introduced. The tunable antenna has two independently tunable modes with different radiation patterns. This could be used to an advantage in smart antenna systems. The tunable antenna can also cover multiple frequency bands and provide real-time selectivity at the front-end of a transceiver.

The BST thin-film varactor technology has tremendous potential in both integrated and discrete form as an enabling technology for frequency-agile systems. Each implementation has its own particular advantages. It is also possible that the BST process could also be used in post-fabrication filter tuning and temperature compensation. To further enhance the usefulness of BST varactors a solder-bump process development is recommended. This would result in further improvement of BST

varactor Q thus affording improved system performance. Such concepts and other suggestions for future research work will be discussed in the next section.

8.2 Future research

Novel design concepts for optimized resonator tuning, a BST thin-film process and frequency-agile devices using both integrated and discrete BST varactor technology were presented in this dissertation. Techniques and processes formulated as a part of this research work have opened new avenues for further exploration. The Q factor for integrated BST varactor at 26 GHz was reported as 30 and that for a discrete BST varactor in the range of 2–6 GHz is between 15–20. Various methods for improving the Q factor were investigated and the most important recommendation is the development of a solder bump process that would allow a more controlled varactor attachment than the conductive epoxy process that was used for this work. The possibility of achieving high aspect ratio metallization for BST IDCs using a DRIE (Deep Reactive Ion Etch) process should also be investigated. Another area of development would be novel circuits using the concepts of network transformation factor and the trade-off of Q factor with tunability discussed in Chapter 4. Investigation of BST varactor contribution to $1/f$ noise in a VCO should also be considered an area of further development. The following work is envisioned in future using the techniques and material technology introduced in this dissertation:

- Optimized filters, phase shifters and matching networks using the design technique presented in Chapter 4. This would enable maximum tuning without a significant compromise in the Q factor. The limited tunability of BST varactor (usually 2:1) would be put to maximum use.
- Tunable filters on low loss high frequency microwave laminate using discrete IDC varactors. It has been estimated that discrete IDC varactors can be used up to a frequency of 8–10 GHz beyond which the parasitic effect would begin to dominate and using an integrated BST thin-film varactor becomes essential.

- Development of solder/indium bumping technique for achieving low resistance connections to discrete IDCs. Silver epoxy is currently used for attaching the IDCs to the board. Though this is acceptable in the range of 1–3 GHz, a better interconnection method is highly desirable at higher frequencies.
- Integrated VCOs and phase shifters using BST thin-film varactor on alumina would demonstrate the advantages of the BST varactor compared to semiconductor varactors at higher frequencies. Investigation of $1/f$ noise in a VCO circuit employing a BST varactor is also recommended.
- Integrated tunable antennas using BST thin-film MIM varactor on copper foil. This would enable low-cost antenna development for mass production. In addition, phased arrays or reflectarrays could also be demonstrated.
- BST varactor can also be used in a tunable linearizer for reducing distortion in nonlinear power amplifiers.
- Recently tunable left-handed materials and circuits have been designed using semiconductor varactors. In particular, a leaky wave scanning antenna and a reduced size phase shifter have been reported. Such circuits could be designed with BST varactors and should be expected to have better performance in terms of linearity and power consumption.

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Appendices

Appendix A

Voltage Controlled Oscillator using MIM BST Varactor

A.1 Introduction

VCOs are perhaps the most ubiquitous element in all communication systems, wired or wireless. In a wireless system the quality of the communication link is determined in large part by the characteristics of the VCO [149, 150]. A reversed bias semiconductor junction is typically used as the tuning capacitor in a VCO, wherein the applied voltage changes the depletion width and hence the tuning capacitance. The figure of merit of the VCO is primarily determined by the quality of the capacitor used and the RF voltage that can be applied across the capacitor [151]. The varactor must operate in the reversed bias region to avoid forward conduction and excess shot noise. Thus there is a limit to the RF voltage swing that can be impressed upon the capacitor and this imposes an inherent limitation on the lowest achievable phase noise in the VCO [152]. This is in sharp contrast to the BST varactor which can handle high RF voltage swings since there is no equivalent of a forward biased junction as in the

case of a conventional semiconductor varactor. Now, the Q factor of a semiconductor varactor increases with increasing bias. Thus, while increased resonator Q is desirable, the increased RF voltage peak plus DC tuning voltage risks forward biasing the semiconductor junction. This is known as the junction bias effect and is minimized by using an array of back-to-back varactors. The BST varactor does not suffer this consequence. BST-based varactors are passive devices and have significantly different properties compared to semiconductor varactors. The capacitance tuning mechanism in a BST varactor is in sharp contrast to that of a semiconductor varactor, the former being a spontaneous polarization effect whereas the latter is a variable space charge depletion effect. The characteristics of these two types of varactors can be expected to be different in terms of tuning voltage, tuning linearity, breakdown voltage and noise effects. The semiconductor varactor has been used extensively as a tuning element in voltage controlled oscillators (VCOs).

Due to the fundamentally different tuning mechanism in the BST thin-film varactor, a single BST varactor-based VCO will have markedly different spectral characteristics. In particular there is no limitation on the voltage swing; hence the spectral purity can be traded off with power consumption. It also has a symmetrical tuning curve and can be operated in either the bipolar or unipolar mode. Furthermore it should have better noise characteristics than a semiconductor varactor, particularly in terms of lower $1/f$ noise and shot noise. Finally, the well-behaved capacitance-voltage curve of the BST varactor lends itself to lower Q and therefore more robust Phase Locked Loop designs [153]. The prospects of substituting a semiconductor varactor with a BST thin-film varactor for improving the overall spectral characteristics of a VCO is evaluated. A voltage tunable oscillator using a BST thin-film varactor was designed and characterized. The frequency of oscillation varied from 34.8 MHz to 44.5 MHz (28% tuning) upon application of 7 V tuning voltage. The VCO gain was 1.38 MHz/V and the 2nd harmonic was over 23 dBc below the fundamental throughout the tuning range. The work presented in Appendix A and B was performed in collaboration with Alan Victor. He was responsible for circuit design and implementation, results presented here are due to the joint work carried out with him.

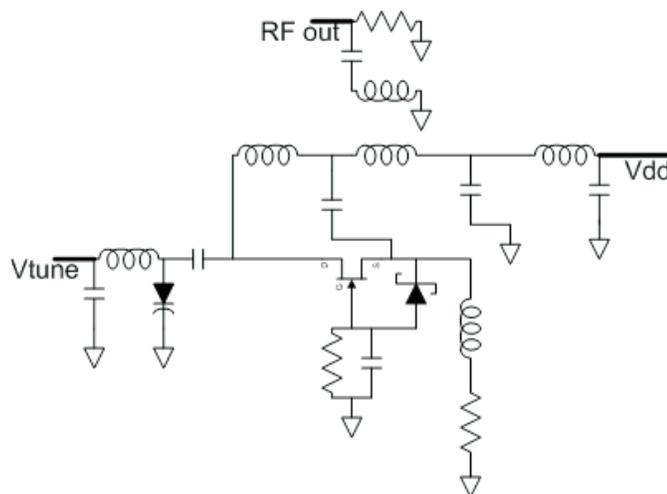


Figure A.1: Circuit diagram of the VCO.

A.2 Design and fabrication

A 35–45 MHz range VCO was designed and characterized with both a semiconductor varactor and a BST varactor. The VCO was used as a test vehicle and the only element changed was the varactor so that any performance differences could be attributed to the devices themselves. The circuit diagram for the VCO is shown in Figure A.1.

The VCO resonator is designed to maximize the unloaded Q with tuning. When the resonator is embedded in a feedback loop of an active device the loaded Q is set to maximize Signal-to-Noise Ratio (SNR). A toroid inductor was selected to maximize the unloaded Q and maintain a convenient form for feedback adjustment. A tapped feedback Hartley oscillator configuration was used. A combination of components determines the resonator and VCO operating frequency. A Mathcad[®] routine enabled a minimum resonator inductance and varactor coupling capacitance to be determined. These component values are determined as a function of the varactor minimum capacitance, the varactor-tuning ratio, the desired VCO tuning range, and the total fixed parasitic resonator and active device capacitance. The varactor coupling capacitance and resultant unloaded Q associated with the BST or semiconductor varactor

network is held constant to facilitate performance comparison. In the final VCO design the coupling capacitance to the varactor in the resonator tank was adjusted to either improve phase noise or adjust oscillator-tuning sensitivity. The semiconductor varactor used had a nominal Q of 30 at 1-volt bias.

The BST varactor was fabricated using a metal organic chemical vapor deposition (MOCVD) [77] process achieving a nominal Q of 32 with no bias. The BST thin-film was deposited on Si/SiO₂/Pt and had platinum (Pt) top electrodes which were patterned using the standard image reversal process. The MOCVD process provides excellent composition control, good area coverage and conformal coating and hence was used for fabrication of the BST thin-film. Two BST capacitors were connected in series; this was done to obtain low value BST varactors since the thin-film has very high permittivity ($\epsilon_r \sim 300$). The capacitors were diced from the wafer and attached to a 7-pin ceramic DIP (Dual-Inline-Package) carrier. The two top electrodes were then wire bonded to the gold pads. The zero-bias value of the BST varactor used in this work was found to be 200 pF and had a 3:1 tuning ratio from 1 to 12 V bias. The core of the VCO used an n-Channel JFET (Model U 310 from Vishay Siliconix). The VCO was then assembled using discrete components on an FR4 board, see Figure A.2.

A.3 Measured results and discussion

The C-V curves of the BST and semiconductor varactors were measured on an analyzer at 10 MHz for bias voltages up to 9 V. It can be seen from the C-V curves, Figure A.3, that the semiconductor varactor has greater non-linearity than the BST varactor. The VCO was tested using an Agilent E4445A PSA Series Spectrum Analyzer. The wide-band spectrum and frequency tuning was measured at different tuning voltages. In Figure A.4 it can be seen that the BST varactor has a more linear tuning curve than does the semiconductor varactor and also has a lower VCO gain. This should allow a more robust PLL (Phase Locked Loop) design compared to a semiconductor varactor VCO. The BST varactor VCO also has much better 2nd

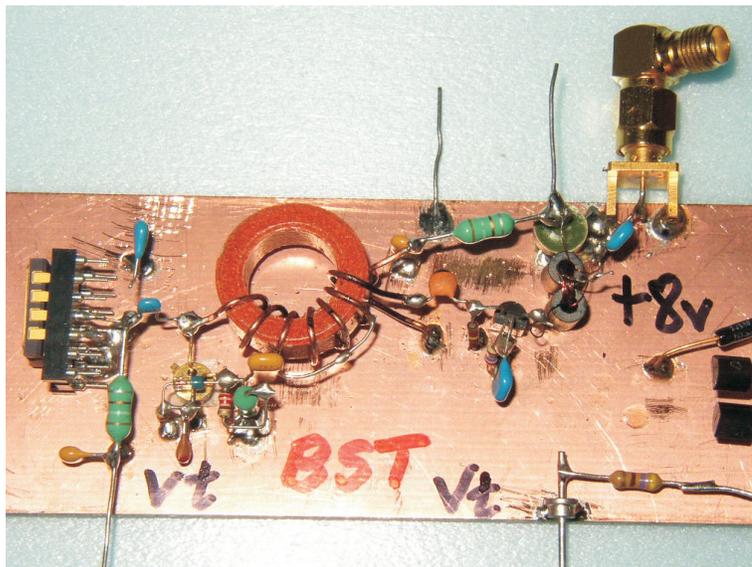


Figure A.2: Assembled BST varactor VCO.

harmonic performance compared to the semiconductor varactor. It can be seen in Figure A.5 that the 2nd harmonic for the BST varactor VCO is well under 23 dBc over the entire tuning range whereas the semiconductor varactor degrades to -18.0 dBc at high bias voltages. This is because the single varactor is subject to forward bias on peak value of the RF swing while the BST varactor is quite insensitive to it. The change in slope of the 2nd harmonic curve for the BST varactor at different bias voltages can be attributed to the fact that over certain regions of the C-V curve the BST is more non-linear than in other regions. Hence nonlinearity, or conversely the approximation to a linear small signal model, is voltage dependent (see Figure A.3).

The superior performance of the BST varactor is clearly shown in Figure A.6. It presents the broadband spectrum of the two VCOs at high bias voltages at one extreme of the frequency tuning range. This also corresponds to noise at one end of the voltage swing. This plot presents the broadband noise and it can be seen that the noise generated with the semiconductor varactor is much higher than that with the BST varactor.

With the semiconductor varactor, one extreme of the RF voltage swing results in

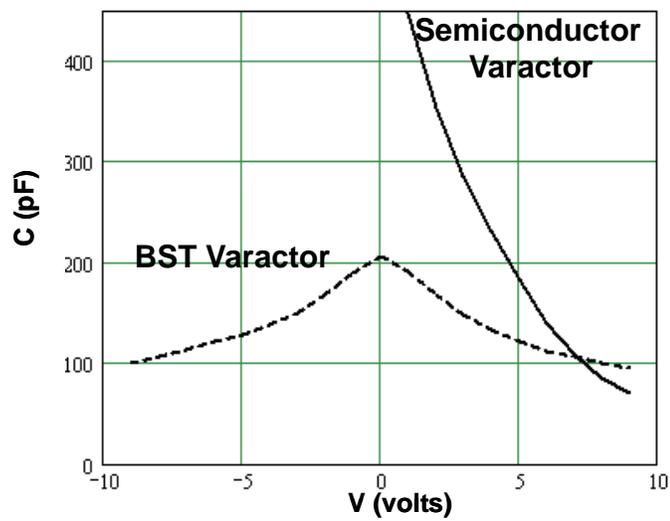


Figure A.3: C-V curves for BST and semiconductor varactor.

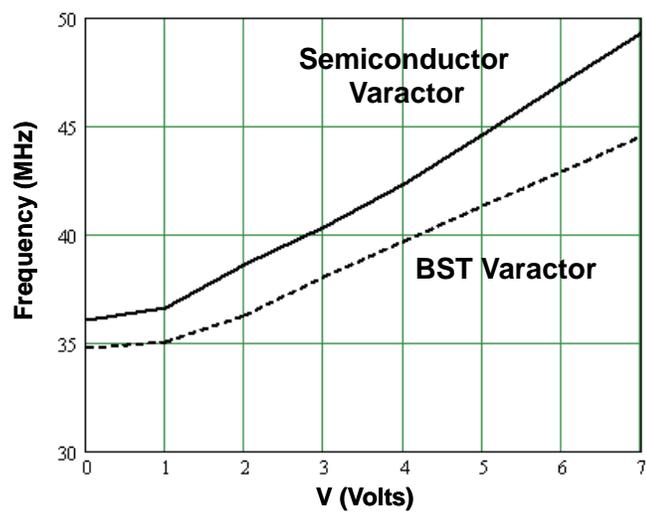


Figure A.4: Tuning curves for BST and semiconductor varactor.

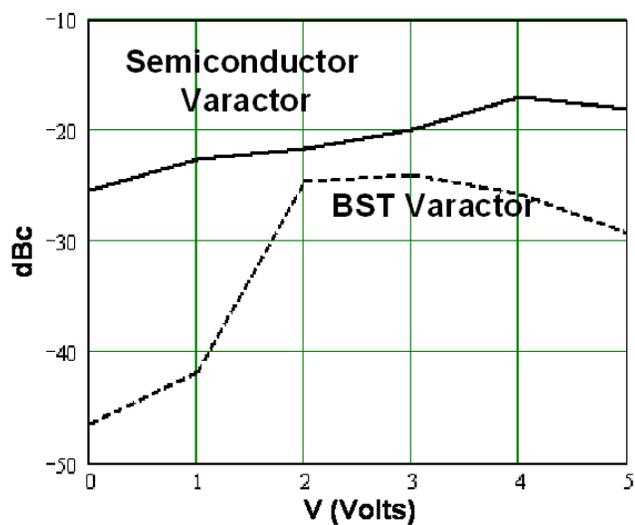


Figure A.5: 2^{nd} Harmonic versus bias for BST and semiconductor varactor.

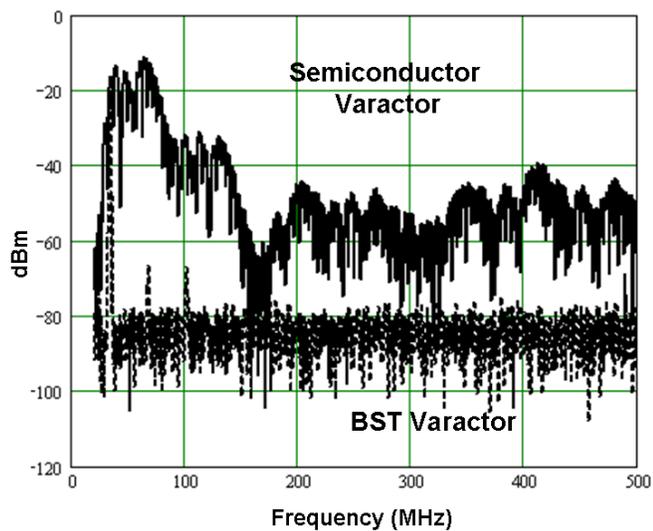


Figure A.6: Wide-band spectra for BST and semiconductor varactors at high bias voltage (6V).

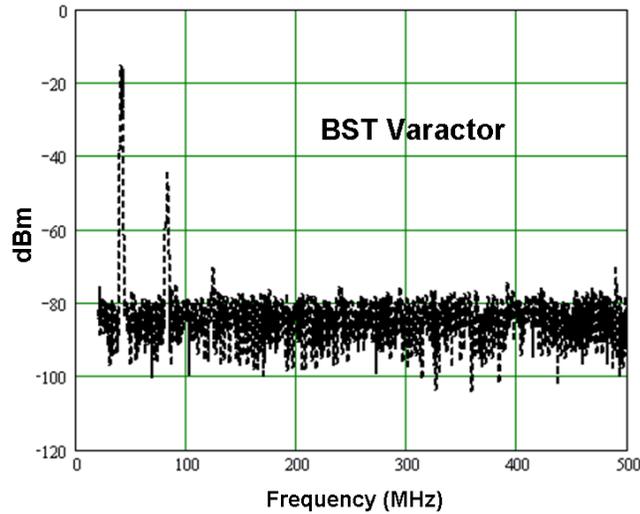


Figure A.7: Wide-band spectra for BST varactor VCO.

mild forward conduction with shot noise generation. Thus the improvement in VCO spectral performance demonstrated in Figure A.6 can be attributed to the absence of varactor junction forward bias effect in BST varactors. Note that the Q factor of the BST varactor is 45, less than that of the semiconductor varactor which has a Q factor of 77. At increased bias voltages, the increase in varactor and resonator Q permits a higher peak RF resonator voltage. The semiconductor varactor tends to get slightly forward biased over the RF swing leading to a significant degradation in the spectrum where as the BST varactor does not suffer from such problems. This fact can be used advantageously for improving the phase noise of the oscillator by trading it with higher voltage swings across the tuning capacitor [154]. An improved phase noise can significantly decrease the BER, relax the specification on the power amplifier, and also address the problem of reciprocal mixing. Furthermore it also reduces the interference in adjacent channels [155, 156].

As discussed earlier, the favorable C-V curve of a BST varactor also allows greater suppression of the second harmonic and up conversion of noise from baseband. This is shown in Figures A.7 and A.8. The wide-band spectral plot is shown for 5 V bias. It is seen that the BST varactor VCO has almost 11 dB more 2nd harmonic rejection

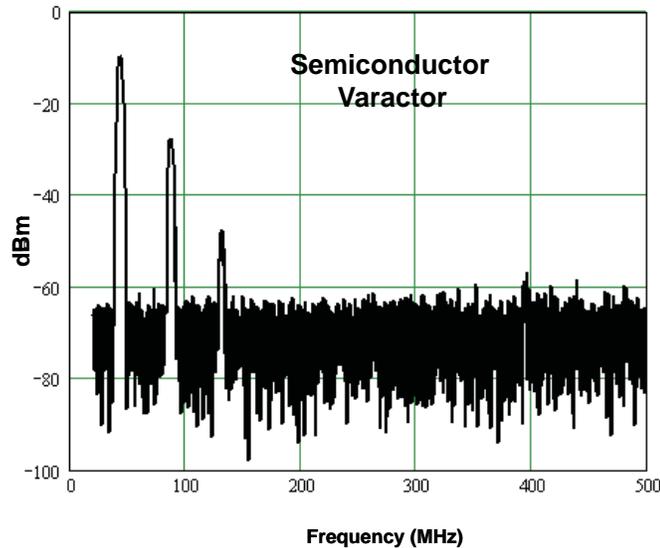


Figure A.8: Wide-band spectra for semiconductor varactor VCO.

than the semiconductor varactor. This is very important in both transmit and receive chains and allows much greater receiver sensitivity than otherwise possible. This also mitigates the problem of the unwanted power located at the harmonics from falling into the desired channel upon mixing during the frequency conversion process [157]. In addition, the lower second order distortion reduces baseband up-conversion effects and self-biasing.

A.4 Conclusion

A Voltage Controlled Oscillator (VCO) utilizing a BST thin-film varactor was designed and characterized. The sideband spectral characteristics of the VCO are promising and harmonic rejection was significantly better than that for the VCO using a semiconductor varactor. Due to the absence of a semiconductor junction the BST VCO also tolerates higher RF swings and offers more design flexibility. The lower K_{vco} of the BST VCO renders the phase noise less sensitive to the noise and jitter injected or coupled from other circuitry. Thus it also lends itself to on-chip VCO

designs. Overall the BST varactor based VCO seems to be a very strong candidate for high performance VCOs.

Appendix B

GaN-on-Si VCO using Discrete BST Interdigital Varactor

B.1 Introduction

The relatively high gate-to-drain breakdown voltages of a Gallium Nitride (GaN) Heterostructure Field Effect Transistor (HFET) enables the design of oscillators with high RF voltage swings [158, 159, 160, 161, 162, 163]. To take advantage of this in a voltage controlled oscillator (VCO) the tunable reactive element must have a high breakdown voltage so that high phase noise performance can be obtained through increased reactive energy storage in the tank circuit. A GaN HFET is combined here with a thin-film Barium Strontium Titanate (BST)-based varactor in an interdigitated capacitor structure affording large RF swings of up to 200 V peak-to-peak. This enables a tunable Master Oscillator Power Amplifier (MOPA) that in a transmitter obviates the need for a mixer and power amplifier.

A 1.6 GHz high power Master Oscillator Power Amplifier with a GaN-on-Si heterostructure field effect transistor (HFET) will be introduced. The voltage-controlled

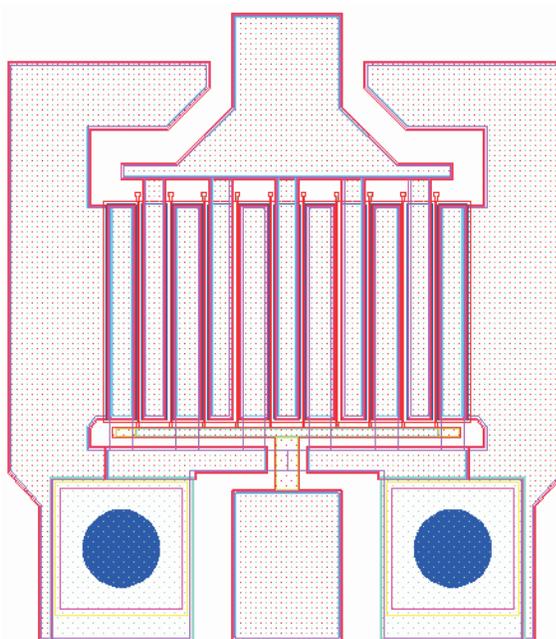


Figure B.1: The 2 mm gate periphery GaN HFET consists of 10 gate fingers $0.7 \mu\text{m}$ long and $200 \mu\text{m}$ wide with a $30 \mu\text{m}$ gate pitch and contains two backside source vias.

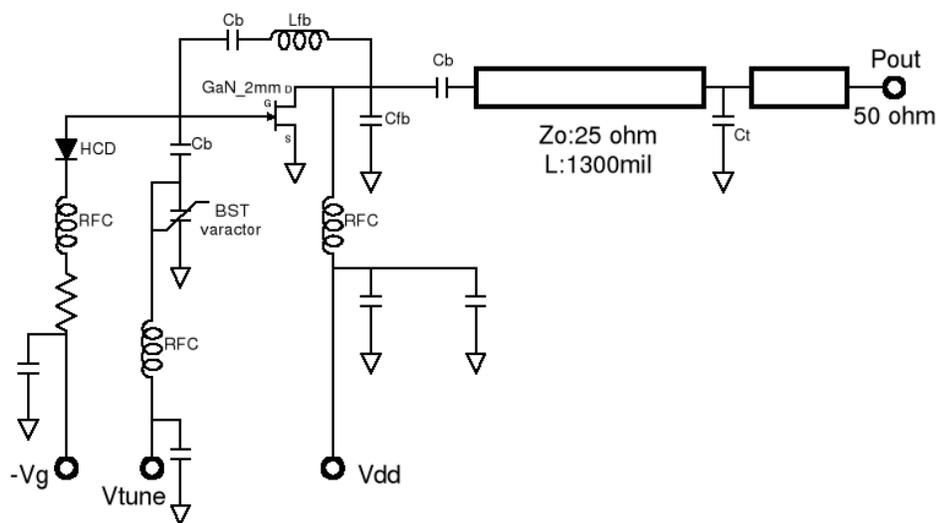


Figure B.2: GaN HFET-BST oscillator with gate-drain feedback network and output load matching network operates in a grounded source configuration.

oscillator used a thin-film barium strontium titanate (BST) interdigital varactor as the tuning element. The surface-mount varactor was fabricated using sputtered BST film and copper metallization on alumina. An output power of 1.6 W (32 dBm) was obtained with a DC conversion efficiency of 25.5%. Flat tuning sensitivity of 500 kHz/V, 49 MHz linear frequency tuning, and power flatness of better than 0.5 dBm were obtained with 0–100 V tuning voltage. The maximum oscillator phase noise was -81.4 dBc/Hz at 100 kHz offset.

B.2 Device technology and oscillator design

The AlGaIn/GaN HFET was grown by MOCVD on a 100 mm diameter, 150 μm thick, $\langle 111 \rangle$ Si substrate (GaN-on-Si HFET) [159]. The device had a 2 mm gate periphery consisting of 10 gate fingers each of which was 0.7 μm long and 200 μm wide. A 30 μm gate pitch separated adjacent fingers and there were two backside source vias, see Figure B.1. The device had 130 V breakdown and an I_{dss} of 900 mA. At 2.0 GHz and 28 V drain bias the device presents input and output impedances of and respectively, and has an available output power of better than 5.0 W. The HFET was attached into a thermally conductive CuW single-ended ceramic package using an AuSi eutectic process that grounded the source vias to the package. The device is unconditionally stable, with a K factor of 1.2 at the design frequency.

The VCO circuit is shown in Figure B.2 where feedback, through, and appropriate load reflection coefficient, Γ_L , yield stable oscillation [164] with a negative real input conductance and an inductive susceptance at the gate terminal. In conjunction with the BST varactor this forms the tunable resonator at the gate. The varactor is tightly coupled to the gate terminal through a series blocking capacitor. Tight coupling is difficult to implement with alternative junction varactors due to the risk of junction forward bias [165]. Decoupling of the varactor results in increased loaded resonator Q but at the expense of reduced tuning range [166]. A series Schottky diode permits soft start of the oscillator. The V_{tune} terminal provides varactor control and is low-frequency decoupled. The fabricated VCO is shown in Figure B.3 where the device is

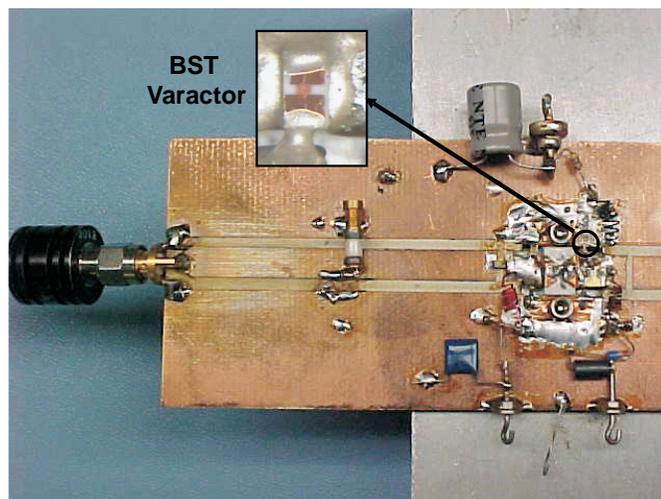


Figure B.3: Assembled GaN-on-Si MOPA with the BST varactor.

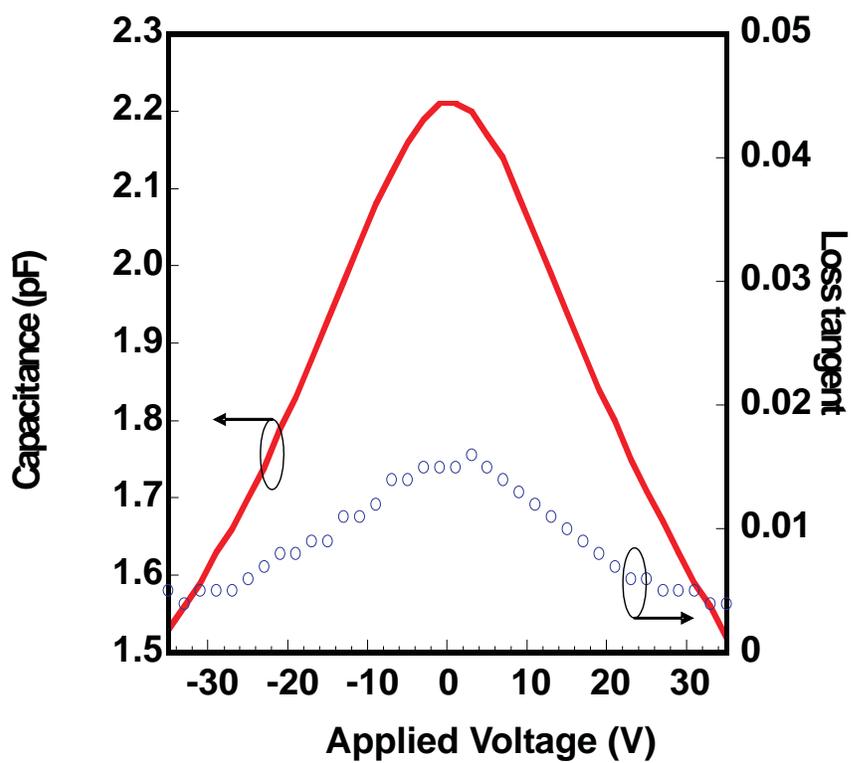


Figure B.4: Representative tuning curve of the BST interdigital varactor at 1 MHz.

directly mounted on a heat-sink through a slot in the circuit board. Additional networks provide bias control and RF decoupling. The RF chokes and bypass capacitors had self-resonant frequencies above 6 GHz.

B.3 Fabrication of BST interdigital varactor

BST is a ferroelectric which in its paraelectric phase is a dielectric with an electric field-dependent permittivity. Here it is used to form interdigitated capacitors in standard surface mount 0603 form. A $0.6\ \mu\text{m}$ $\text{Ba}_{0.60}\text{Sr}_{0.40}\text{TiO}_3$ thin-film was deposited on a polished alumina substrate using a radio frequency magnetron sputtering technique [113], details can be found in Chapter 6. An array of discrete IDCs with finger width and spacing and finger length was fabricated using a two-layer metallization (20 nm of Cr and 500 nm of Cu) process and a photolithographic metal lift-off technique. The varactor tuning and loss curve is shown in Figure B.4 and breakdown voltage exceeded 100 V.

B.4 Experimental results

The oscillator has a nominal frequency of 1629 MHz and a power output of 1.6 W (32 dBm) and the power flatness across the tuning range was better than 0.5 dBm, see Figure B.5. The total DC efficiency was 25.5% over the entire tuning range at a drain voltage of 28 V. The corner frequency (where an oscillator with a small loaded Q transitions from a 30 dB/decade slope to 20 dB/decade) is at 3 MHz. Phase noise degradation over the tuning range was found to be small. At 0 V varactor bias the noise at 100 kHz offset degraded by 3 dBc/Hz compared to that at high bias voltages. The phase noise was -81.4 dBc/Hz at 100 kHz offset, see Figure B.6. From 0 V to 100 V the oscillator tuning gain was nearly constant at approximately 500 kHz/volt resulting in near linear frequency tuning, see Figure B.7.

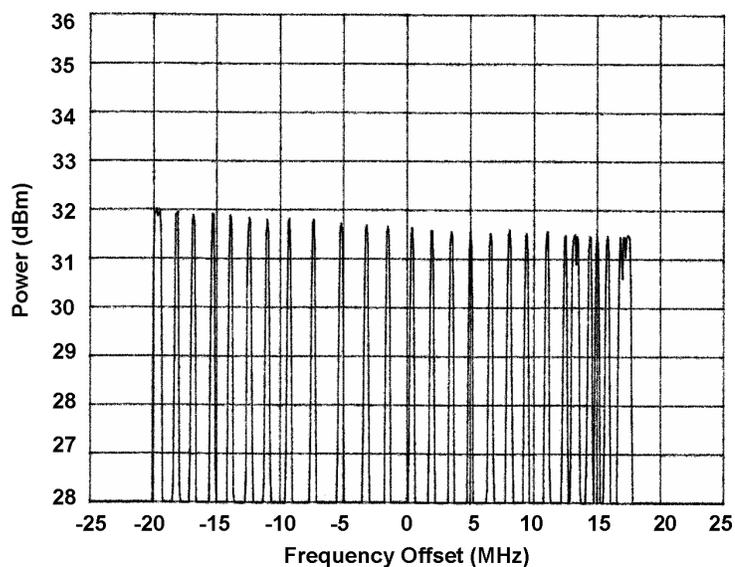


Figure B.5: Power flatness plot of the VCO as the tuning voltage was varied in steps from 0 to 70 V, center frequency is at 1649 MHz.

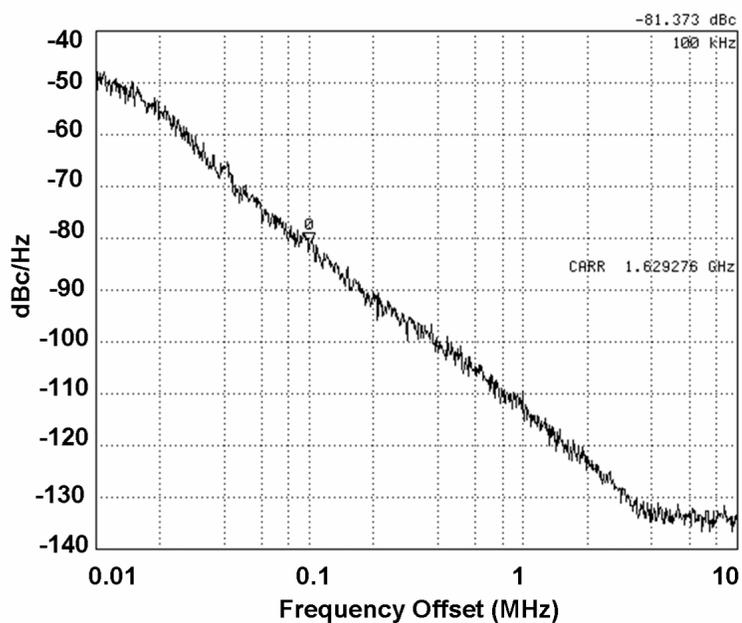


Figure B.6: Phase Noise (-81.4 dBc/Hz @ 100 kHz offset) plot of the GaN-on-Si VCO.

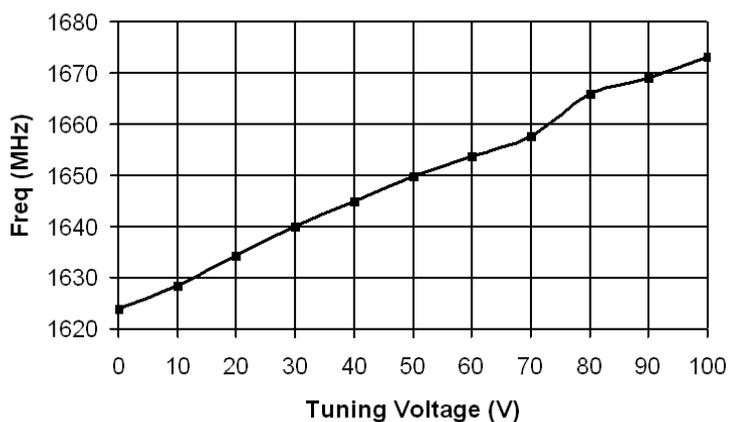


Figure B.7: Oscillator tuning curve.

B.5 Conclusion

A MOPA with a GaN-on-Si oscillator and a BST varactor was presented as a voltage-tunable, high-power microwave-frequency oscillator. A simple topology demonstrated efficiency of 25.5% at 1.6 W (32 dBm) output power with nearly linear tuning and flat output power (< 0.5 dBm deviation). No spurious oscillation modes were observed. The MOPA can be incorporated in a phase locked loop for further phase-noise reduction.

Appendix C

Co-planar T-resonator based Permittivity Extraction Technique

C.1 Introduction

AC-coupled interconnects (ACCI) is a very exciting technology for achieving high-density chip-to-package interconnects while simultaneously providing a simple, mechanically robust interface. The technology combines the stress-relieving “underfill” layer with the dielectric medium for capacitive coupling. For good AC coupling, it is desirable for the underfill material to have a permittivity around 20 at operating frequencies. However, there is a lack of microwave frequency data for high permittivity ceramic-polymer composite systems in the literature. The development and microwave frequency characterization of high K nanocomposite underfill was undertaken.

Increasing chip functionality demands a high density interconnect technology. One of the most commonly used interconnect technology uses a direct, contacting path for every input/output connection. This limits achievable connect density in pin and ball

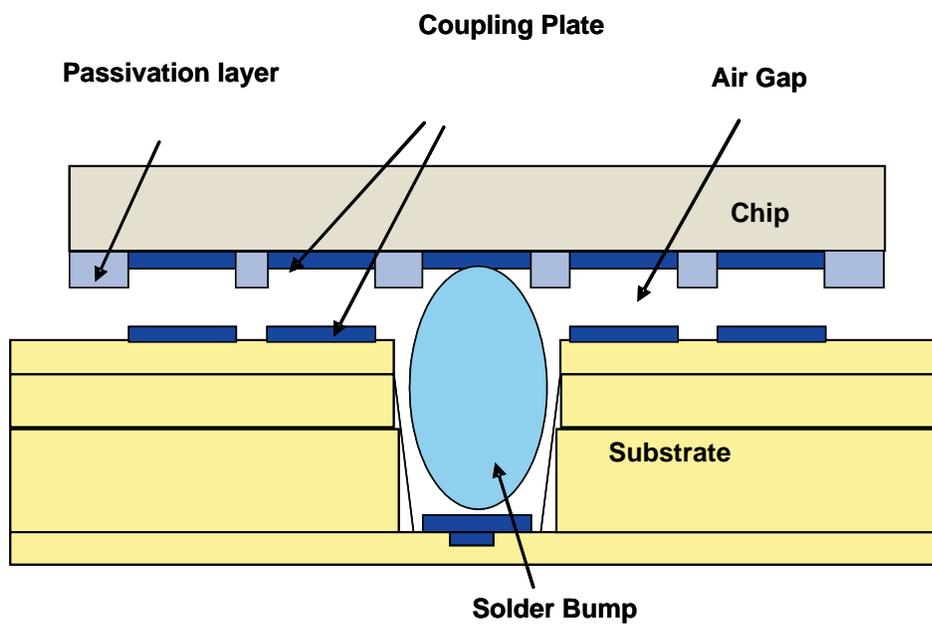


Figure C.1: Schematic of AC coupled interconnect technology components.

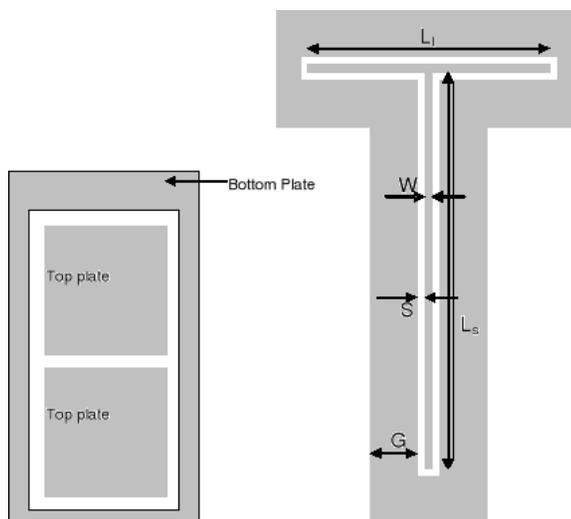


Figure C.2: Schematic of floating plate capacitor (left) and CPW T-resonator structure (right).

grid arrays and thermal mismatch stresses create rework and compliance problems in very high-density solder bump arrays. AC-coupled interconnects is a very promising technology for achieving high-density interconnects while simultaneously providing a simple mechanical interface [167, 168]. In this technology buried solder bumps enable DC power and ground connections, and capacitors spaced across the same surface serves as the capacitively coupled interconnect for high frequency signals (see Figure C.1).

Most implementations of the AC-coupled interconnect concept requires that the chip and the substrate be brought into very close proximity (1–2 μm) to achieve the required capacitance for effective coupling due to the limited permittivity of dielectrics used (air, $\epsilon_{r(\text{air})} = 1$ or SiO_2 , $\epsilon_{r(\text{SiO}_2)} = 3.9$). This requirement poses significant manufacturing and integration challenges due to tolerance issues associated with such small dimensions. The stringent tolerance can be considerably relaxed by replacing the underfill material with a higher permittivity material. Hence there is a need for a high permittivity material that can achieve higher capacitance densities and thereby relax the proximity requirements between the chip and the substrate. Such a material can also provide stress relief by acting as an underfill material and thus improve the overall reliability of the interconnects. In this work a BaTiO_3 -epoxy nanocomposite has been developed and its high frequency characterization has been presented. Photodefinable epoxy was used as polymer matrix for its balanced properties and potential for thick film patterning. BaTiO_3 nano-sized powder was used for modifying the dielectric properties of the underfill. Dielectric properties were evaluated with ceramic loading and curing temperature. The dielectric properties were measured from 45 MHz up to 26.5 GHz to evaluate its suitability for use in high density, high frequency interconnects.

C.2 Experimental details

BaTiO_3 (BT-9, 200 nm, Cabot) nano-powders and commercially available photodefinable epoxy (Probelec 7081, Hunstman) were selected for underfill composition.

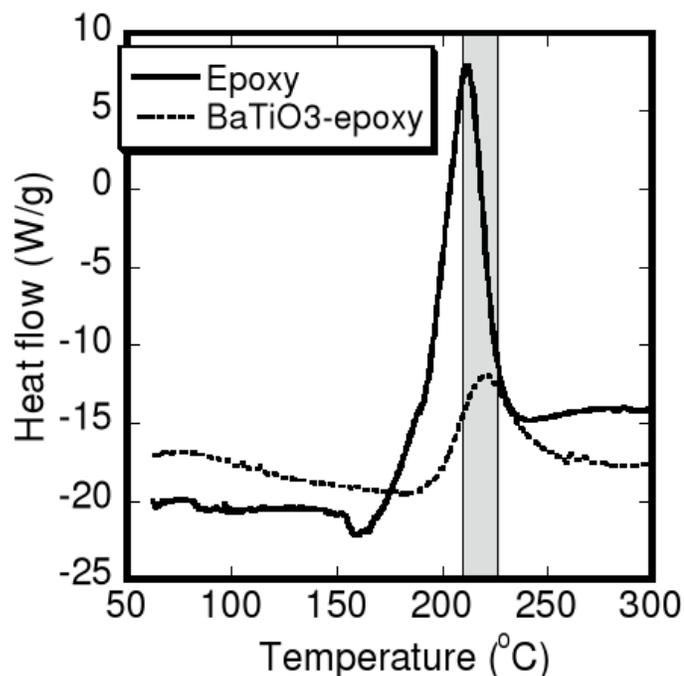


Figure C.3: Curing behavior of composite and epoxy polymer by DSC.

Photodefinable epoxy was selected due to their potential for underfill pattern formation. Ceramic powders, solvent (PGMEA) and dispersing agent (BYK 9010) were mixed in required proportion and blended using a ball mill for 20 hours. The required amount of epoxy was then added and ball milled for another 5 hours to ensure homogeneity. The suspension was spun-on for 20–40 seconds at 1200–2000 rpm on platinized Si or polished alumina substrates (> 99.6%, 50 nm surface finish, ISI Inc). Curing was done for 60 minutes, ranging from 150 °C to 240 °C. For high frequency dielectric measurements two different structures were used.

A floating capacitor structure where the bottom electrode consists of a blanket layer of metal and top electrodes were patterned in the form of squares (Figure C.2). This leads to two series connected capacitor and affords easy access for measurements using planar probes. The floating capacitors were measured at frequencies from 1 kHz to 26.5 GHz. A HP 4192A Impedance Analyzer was used up to 10 MHz, an Agilent 4199A Impedance Analyzer was used up to 3 GHz, and finally a HP 8510C

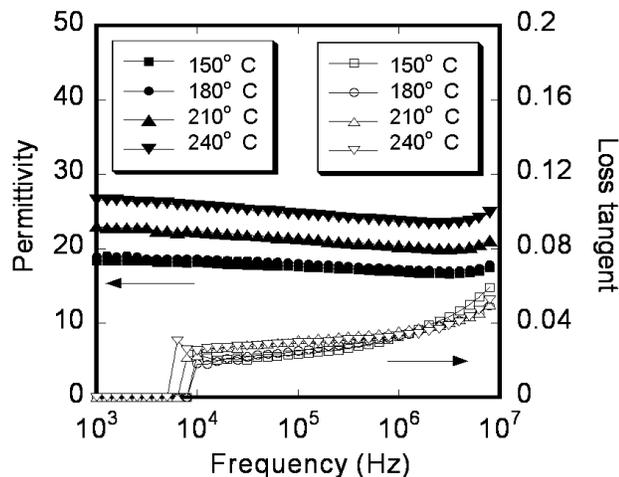


Figure C.4: Low frequency dielectric properties of BaTiO₃-epoxy composite films with cure temperature.

network analyzer was used up to 26.5 GHz. The capacitance, and hence the permittivity data was extracted from all measurements and Q factor was calculated up to 26.5 GHz. However the loss tangent values are reported only up to 3GHz since the loss tangent extraction is more difficult at higher frequencies. This is due to the fact that the metal loss dominates above a few GHz and the dielectric loss becomes too small a value to extract.

The second structure employed was a CPW T-resonator structure, see Figure C.2. This consists of a CPW line loaded with a stub in the middle. The length of the stub determines the frequency of resonance, and the effective dielectric constant can be deduced from the measured resonant frequency points. The use of a T-resonator structure for extraction of dielectric permittivity has been reported in the literature [169] and the application for a CPW T-resonator structure was first introduced by Paterson [170]. A modified version of this technique in which the effective permittivity of the resonator structure is determined with and without the nanocomposite under test was formulated. This enables us to extract the frequency dependent permittivity of the nanocomposite by using a partial capacitance method [171, 172]. Since

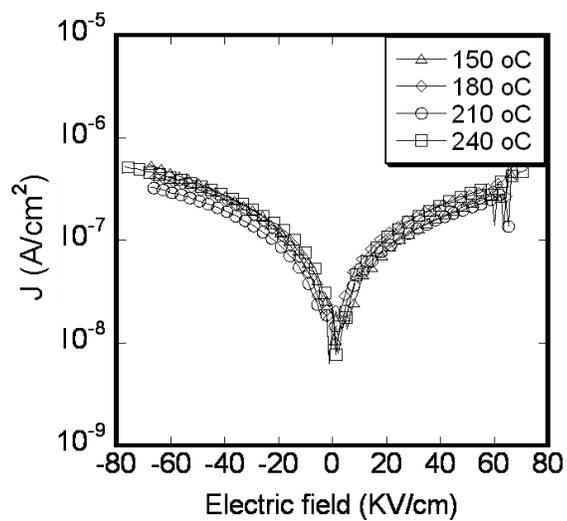


Figure C.5: Measured leakage current with electric field.

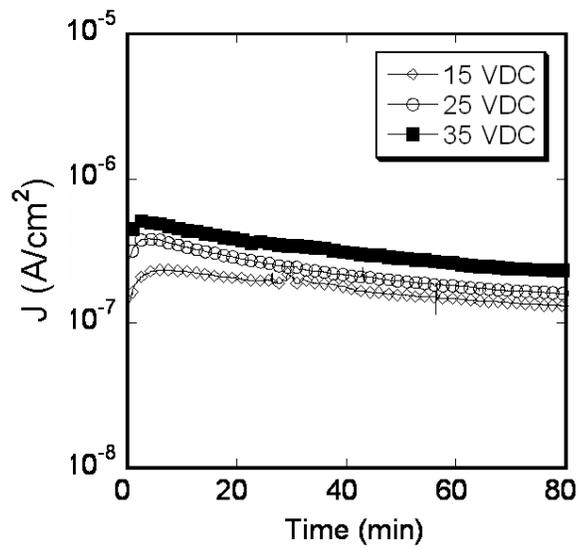


Figure C.6: Measured leakage current with time.

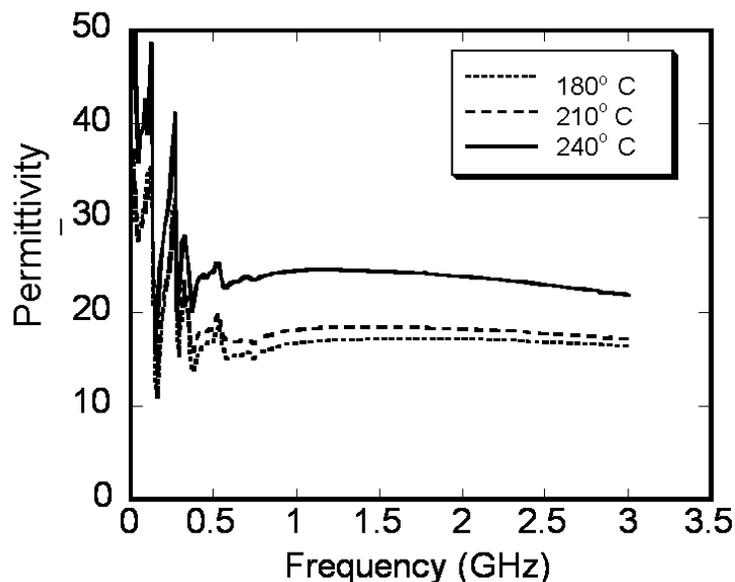


Figure C.7: Permittivity of BaTiO₃-epoxy thick film versus frequency and temperature for floating plate structure.

the frequency dependent permittivity of the both bare alumina and the alumina / nanocomposite stack up is known, the frequency dependent permittivity of nanocomposite can be extracted using standard multi-layered CPW formulae [171, 172]. A program was written in MathCAD® [173] to implement the extraction of the permittivity from the measured data. The CPW T-resonator was designed with a center conductor width, $W = 100 \mu\text{m}$, spacing, $S = 50 \mu\text{m}$, ground plane width, $G = 450 \mu\text{m}$, length of stub, $L_s = 6500 \mu\text{m}$ and line length of CPW, $L_1 = 2500 \mu\text{m}$.

C.3 Results and discussion

Thermal stress-relieving underfill usually undergo an elevated temperature 'reflow' step associated with (or subsequent to) solder bump bonding. Therefore the polymer curing conditions must be compatible with the solder process limits. DSC plot for

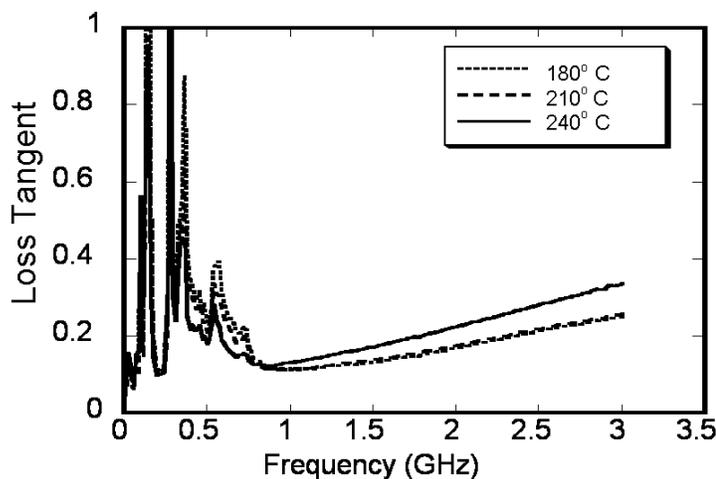


Figure C.8: Loss tangent of BaTiO₃-epoxy thick film versus frequency and temperature for floating plate structure.

epoxy and composite materials are shown in Figure C.3. Epoxy and composite show maximum exothermic reaction around 200–220 °C, which suggests potential compatibility of this composite with the eutectic solder bump process [174]. The shift in the maximum peak position might be due to the difference in heat capacity in the constituent materials. The T_g (glass transition temperature) for both materials were found to be 110 °C (not shown here), which is slightly below than most of commercial capillary flow underfill (130 °C) [175]. Further T_g modulation for better stress relief would be realized by modification of the polymer composition.

It is important to optimize the ceramic loading in composite films as the ceramic loading is directly related to the permittivity. There are a number of models and experimental reports on the dielectric properties of ceramic-polymer composites. As studied by other groups [176], Jaysundere and Smith model [177], which assumes the spherical particles in a homogeneous matrix, fits experimental data well up to 60 vol% BaTiO₃ loading. From our experimental work, model calculations, and device simulation requirements, 30 vol% loading was selected for further study. Figure C.4 shows the low frequency dielectric properties of BaTiO₃-epoxy composite thick films

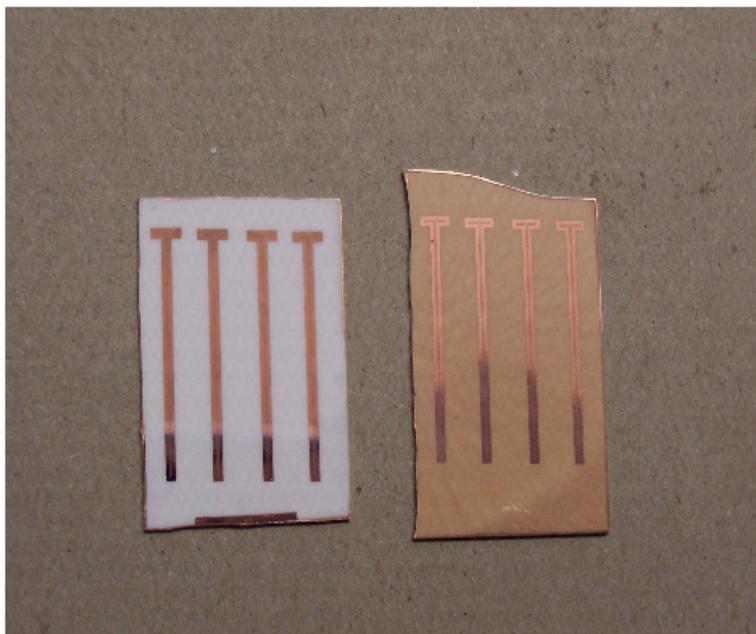


Figure C.9: Fabricated CPW T-resonator structures on bare alumina (left) and with BaTiO₃-epoxy thick film on alumina (right).

on platinized Si. As the curing temperature increases up to 240 °C, permittivity also increases. This might be due to the enhanced connectivity between BaTiO₃ particles and epoxy matrix, but it is not clear at this moment. Dielectric loss did not show a significant variation with curing temperature. The slight decrease in permittivity at higher frequency (close to 1 MHz) might be due to the smaller contribution of polarization at higher frequencies. For the materials to be used for electronic application, reliability would be one of the important parameters to be optimized. Figure C.5 shows the leakage current density versus field of composite thick films cured from 150–240 °C. Regardless of cure temperature, all of the composite thick films showed similar leakage current densities ($\sim 10^{-8}$ A/cm² at zero bias), which is comparable to, or better than, previously reported composite films [178, 179]. Figure C.6 shows typical leakage current density versus time at high dc bias voltage. There is no evidence of time dependent dielectric breakdown or resistance degradation. This is encouraging for reliable service operation.

Figures C.7 and C.8 show the dielectric response of BaTiO₃-epoxy thick films

Table C.1: Extracted frequency dependent permittivity of Alumina.

Frequency (GHz)	Permittivity of Al_2O_3
5.071	9.38
14.83	10.0

Table C.2: Extracted frequency dependent permittivity of BST nanocomposite.

Frequency (GHz)	Permittivity of BaTiO_3 epoxy nanocomposite
4.906	16.2
14.33	17.5

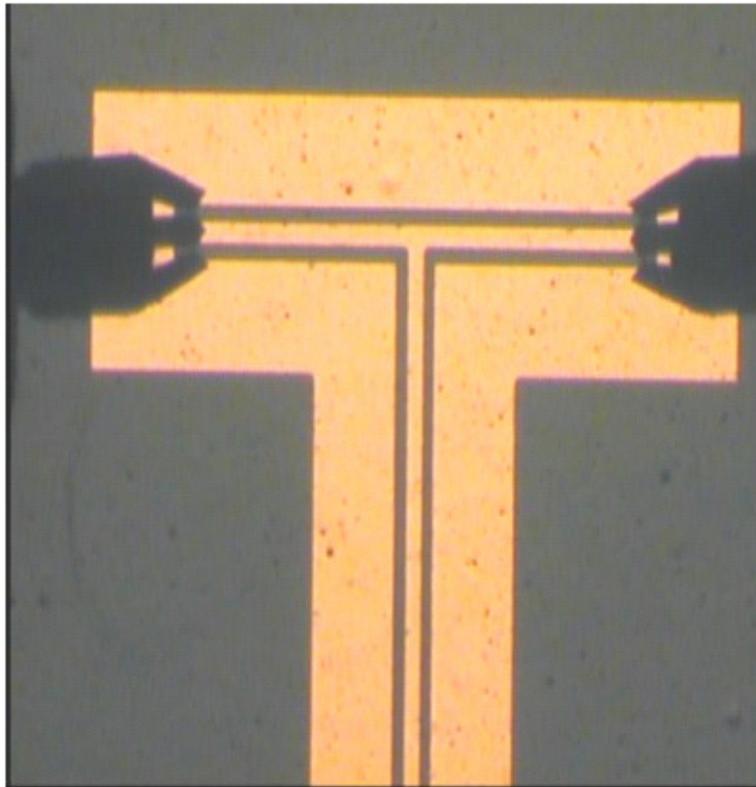


Figure C.10: CPW T-resonator under test.

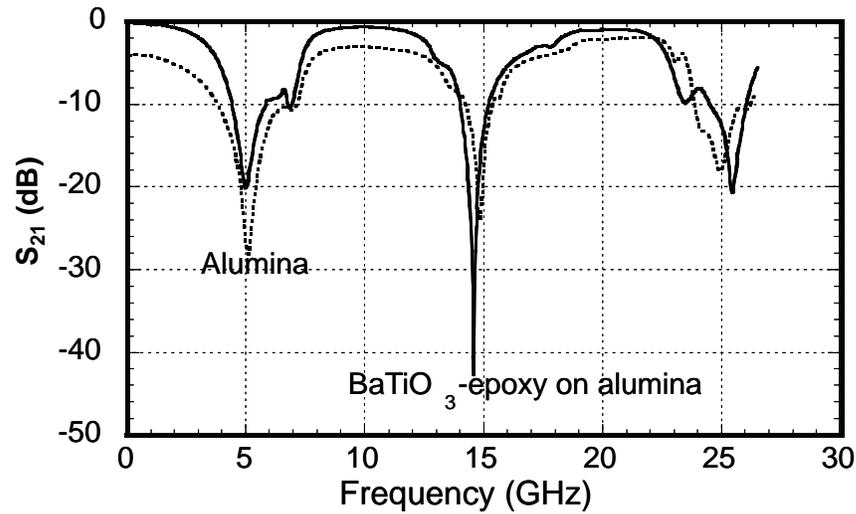


Figure C.11: S_{21} versus frequency for CPW T-resonator.

with floating capacitor structure on platinized Si up to 3 GHz. Although there is noise up to ~ 0.7 GHz from the resonance between dielectrics and analyzer, there is a good correlation between data across the different frequency regimes obtained from different instruments. Above 1 GHz, capacitance (and permittivity) was found to be stable. The loss tangent increased up to ~ 0.3 at 3 GHz. The total Q factor including the metal losses was calculated and was found to be 2 at 26.5 GHz (not shown here). This high dielectric loss might be mostly from the epoxy resin around GHz regime. However, it should be noted that other factors could contribute to the observed dielectric loss. BaTiO_3 ceramics has been shown to have dielectric relaxation in the low GHz region.

Dielectric relaxation of epoxy resin depends on the curing agent, polymerization/cross-linking reaction, reaction temperature etc. For ceramic-polymer composite, other factors like particle size of BaTiO_3 , porosity of composite, might complicate the interpretation. Though the losses might seem high, this would be still acceptable for chip operation. System level calculations were carried out to show that such additional losses can be compensated for in a digital system by the use of additional compensating circuitry with very little overhead. The fabricated CPW T-resonator

structures are shown in Figure C.9. The CPW-T resonator structure under test on a probe station is shown in Figure C.10 and S_{21} plot with frequency is shown in Figure C.11 for composite thick films cured at 210 °C with a stub length of 6500 μm . Due to the limited length of the stub, only three data points are obtained out of which two can be used for extraction of permittivity. Above 20 GHz multimoding occurs due to the discontinuity at the T-junction, and wire bonds [170] or air bridges are required to extend the frequency range. Another method of increasing the number of data points would be to increase the stub length. As can be seen in Table C.1 the frequency dependent permittivity of alumina was experimentally instead of assuming it to be 10 (supplied by the manufacturer at 1 MHz). These values were then used to extract the permittivity values of the nanocomposite, which leads to improved accuracy. Overall it can be concluded that the permittivity of the nanocomposite is relatively flat with frequency and is in the range of 16–18 (Table C.2).

C.4 Conclusion

BaTiO₃-epoxy nanocomposite thick films were prepared and evaluated for potential use in ACCI (AC-Coupled Interconnect) application. For 30 vol % BaTiO₃ loaded epoxy composite, dielectric properties were measured using different capacitor/transmission line structures. Permittivity of underfill was flat with frequency and for the composite cured at 210 °C, permittivity of ~ 18 was measured up to 14 GHz. Permittivity of composites could be modulated by changing the ceramic loading and cure temperatures. Dielectric relaxations for the composites were observed above 1 GHz up to 3 GHz. Dielectric loss was calculated from Q factor and maximum loss was ~ 0.3 at 3 GHz. In summary, the BaTiO₃-epoxy nanocomposite seems to be a very promising candidate for underfill material in ACCI (AC-Coupled Interconnect) for next generation interconnects in multi-gigabit systems.

Appendix D

Phase-Shifter using BST

Interdigital Varactor

D.1 Introduction

The the advantages of BST-based loaded line phase shifters has been discussed in Chapter 2. A loaded line phase shifter on polycrystalline alumina using copper metallization was designed and characterized.

D.2 Design and Fabrication

Phase shifter was designed using the loaded line methodology presented in [50]. BST thin-film process described in Chapter 3 was used. The transmission line was loaded with IDC varactors on either side. The schematic of the phase shifter and a photograph of fabricated phase shifter is shown in Figures D.1 and D.2 respectively.

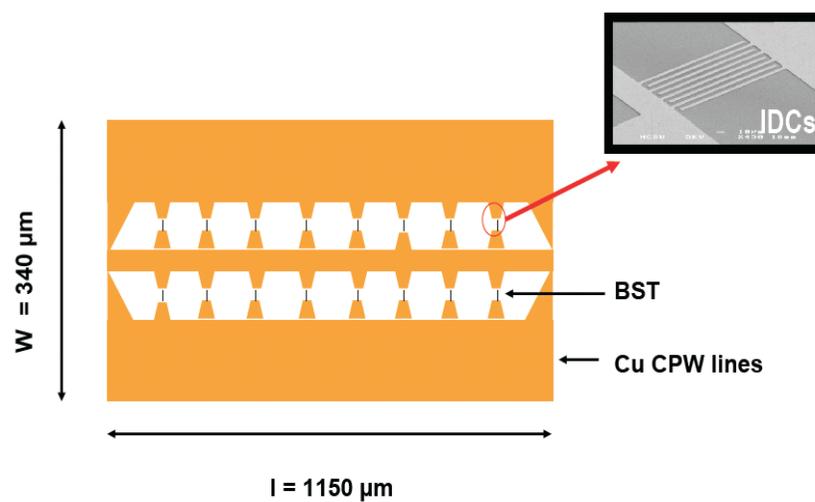


Figure D.1: Schematic of the loaded-line phase shifter

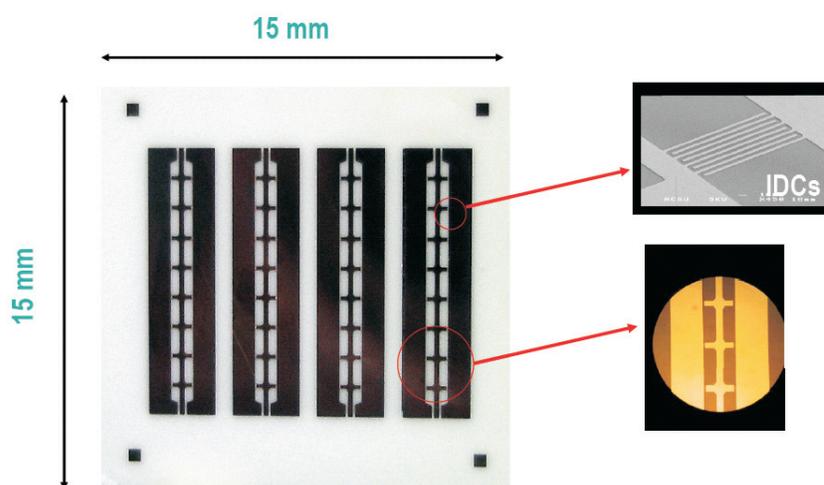


Figure D.2: Fabricated loaded-line phase shifter

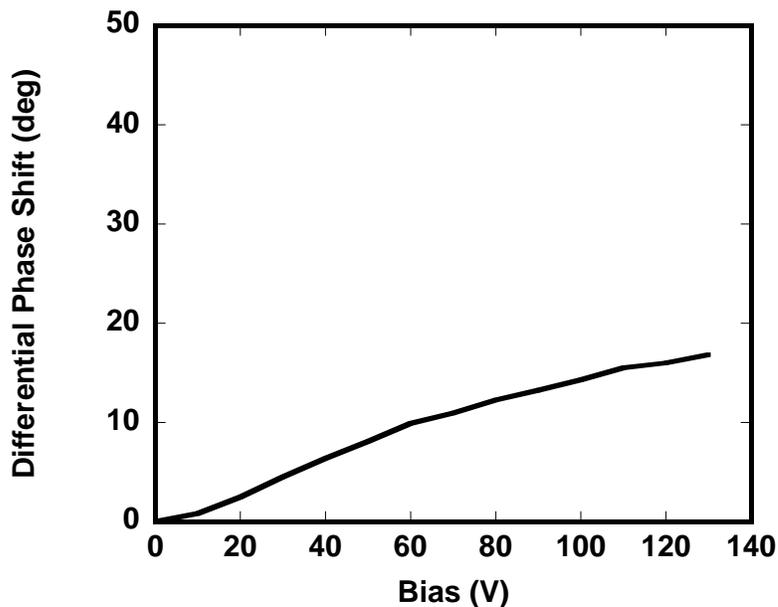


Figure D.3: Measured differential phase shift versus bias.

D.3 Measured Results

The phase shifter was measured on a HP8510 C vector network analyzer. A two-port LRM calibration was performed using a calibration substrate from Cascade Microtech. A 200 μm pitch GSG probe was used for measurements. Bias was applied using a high voltage bias tee from Picosecond Pulse Labs. The IDC varactors broke down beyond 130 V bias. The maximum phase shift obtained at 10 GHz was 18° (Figure D.3) and the maximum insertion loss was 1.1 dB (Figure D.4). The figure-of-merit was calculated to be 16.4 deg/dB.

With applied bias the insertion loss at 10 GHz decreases to 0.7 dB, see Figure D.5. The return loss at zero bias was better than 20 dB (Figure D.6) over the frequency range.

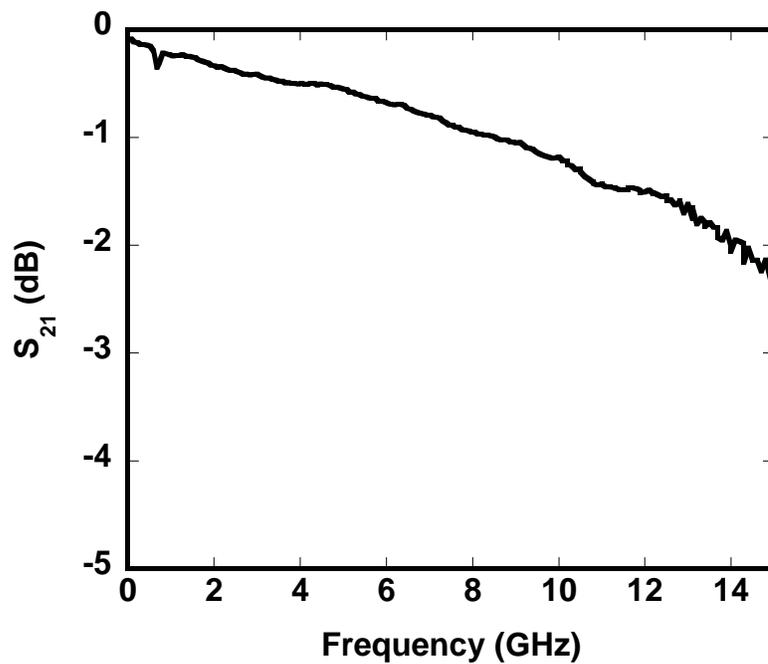


Figure D.4: Measured S_{21} versus frequency at zero-bias.

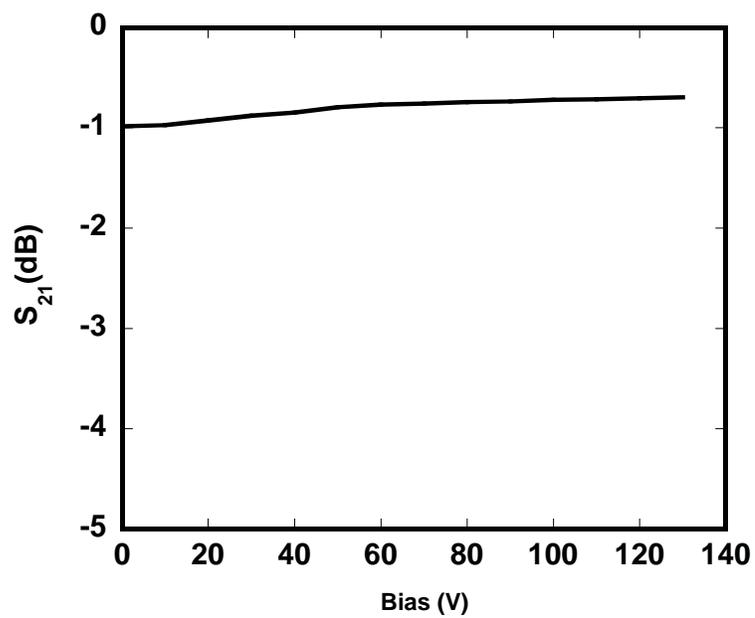


Figure D.5: Measured S_{21} versus bias at 10 GHz.

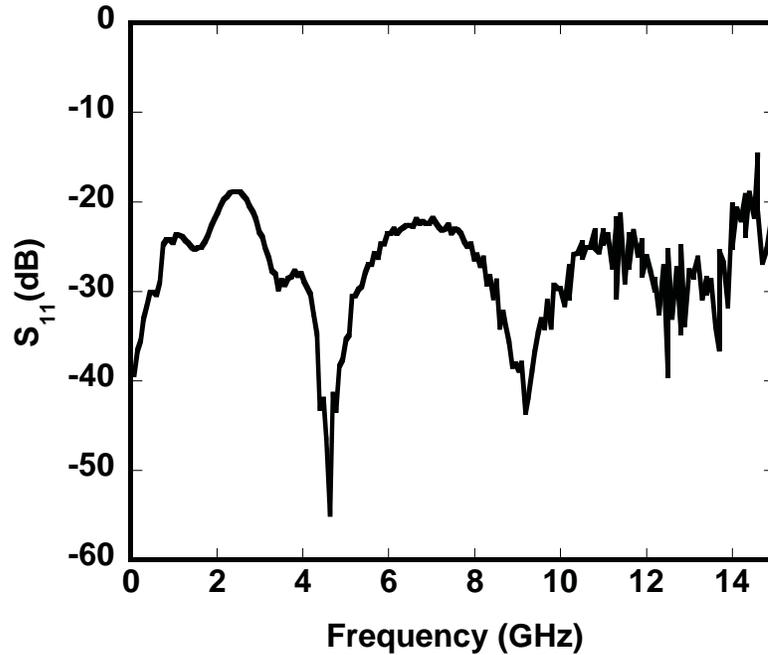


Figure D.6: Measured S_{11} versus frequency at zero-bias.

D.4 Conclusion

The FOM of the BST IDC varactor loaded phase shifter was 16.4 dB/deg at 10 GHz. Though this is much lower than that reported for BST MIM varactor based phase shifters, there is considerable room for improvement. First, the design could be optimized to yield a larger phase shift for the same capacitance tuning ratio. Second, the IDC tunability could be improved. The IDC gap spacing was 6–6.5 μm and for a 130 V bias this corresponds to an applied field of 200 kV/cm. In comparison to MIM varactor based designs the applied field is lower by a factor of 3–4. By either increasing the applied field or by designing a smaller gap spacing in the IDCs, the phase shift and hence the FOM can be improved substantially.