Progress and Planned Future Directions in Optical Processing and Communications

DARPA/MTO Microsystems Technology Symposium

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Standard Form 298 (Rev. 8-98)
Prescribed by ANSI Std Z39-18

Technology Push and Integration Trends

ⓐ Transistor

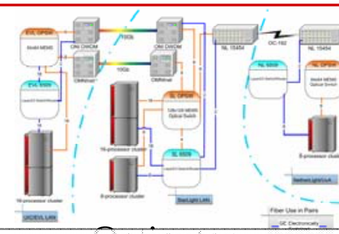
ⓑ Million to Billion transistor integration

ⓒ Heterojunction Laser, Optical Waveguides, Integrated & Silicon Photonics

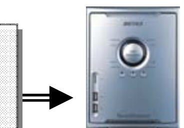
ⓓ Heterojun
Integrated

ⓔ Vertical M
Storage

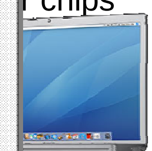
NEC earth simulator



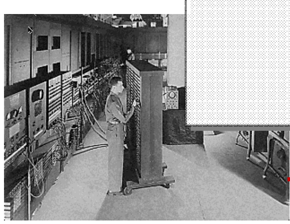
Cisco CRS-1 (92 Tbps
- 40 Racks

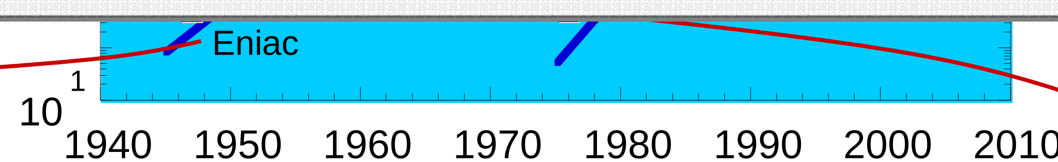


Systems
ers on-chip
for chip-to-
processor
r chips



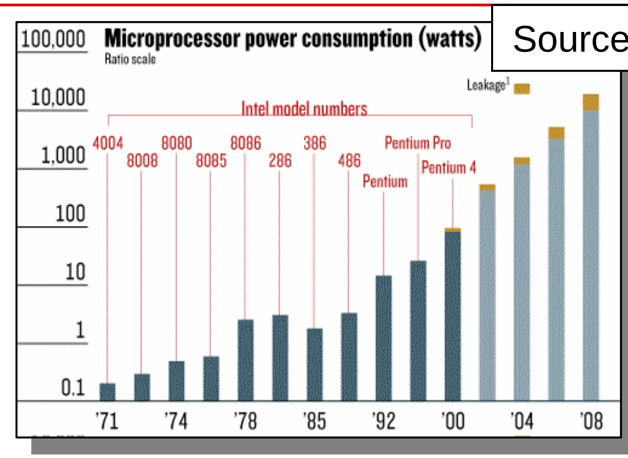
Approximately every 10 years we see the results of basic technology research reduce systems from lab size to the desktop size. This trend enables vast new applications that cannot be fully forecast.



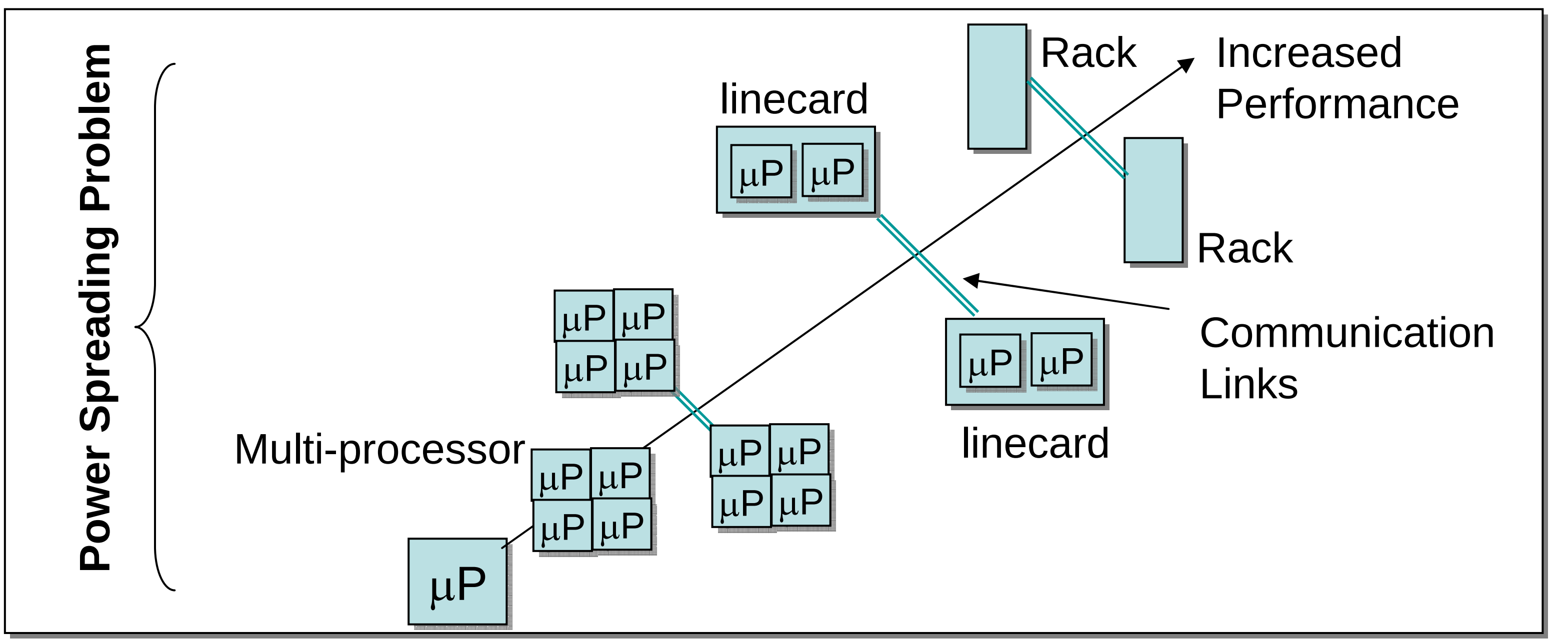


Power and Size: The Next Frontier

- *Decreased transistor size, 2x transistors on chip every 18 months, increased frequency*
- *Leakage current is huge problem, chips (hence systems) become power constrained*
- *New transistor technologies aim to decrease leakage current but requires new processing infrastructure. Costly to roll over to new foundries from current.*
- *Moving to multi-processor cores to keep up performance without increasing speed*



Source: Intel



Technical Contributors

CSWDM

Integrated Optical Wavelength Converters and Routers for Robust Wavelength-Agile Analog/ Digital Optical Networks

UCSB: M. Masanovic, V. Lal, J. Summers, H. -F Chou, E. Skogen, J. S. Barton M. Sysak, D. J. Blumenthal, J. E. Bowers, L. A. Coldren, N. Dagli, E. Hu

DoD-N

LASOR: A Label Switched Optical Router

Cisco Systems: D. Civello, G. Epps

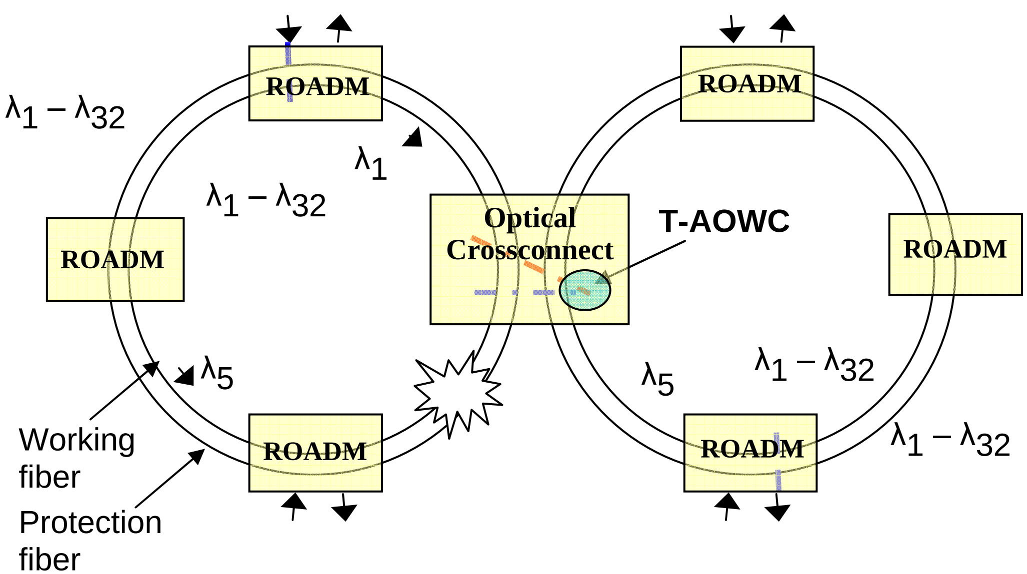
JDSUniphase: C. Coldren, G. Fish

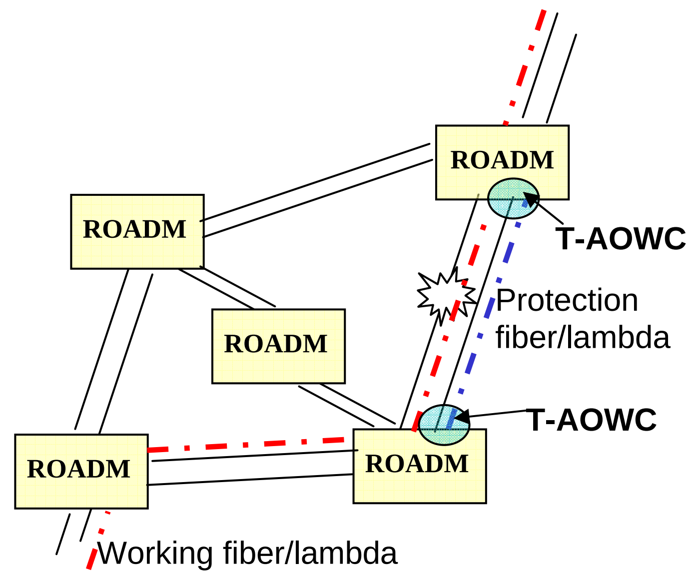
Stanford University: N. Beheshti, Y. Ganjali, N. McKeown

UCSB: B. Koch, M. Chun, L. Garza, M. Mashanovitch, J. Barton, T. Berg, J. Mack, H. Poulsen, S. Nicholes, E. Burmeister, H. Park, M. Dummer, A. Tauke-Pedretti, B. Stamenic, D. J. Blumenthal, J. E. Bowers, L. A. Coldren

CSWDM- Motivation and Applications

- Monolithically integrate widely tunable digital and analog wavelength conversion from any input λ to any output λ
- Make tunable wavelength converters inexpensive to use
- Eliminate off-chip high speed electrical for WC and regeneration
- Analog operation to 20GHz
- Integrate signal quality monitoring
- Push limits of on-chip component and function density

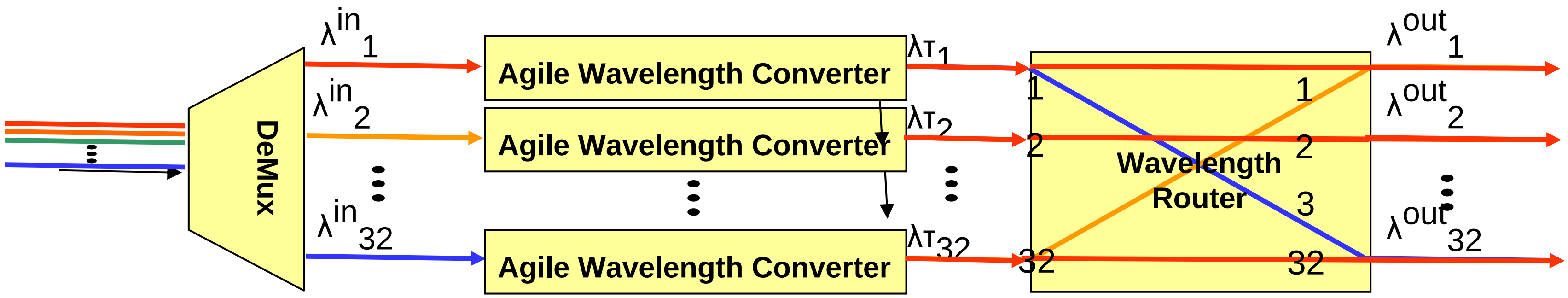




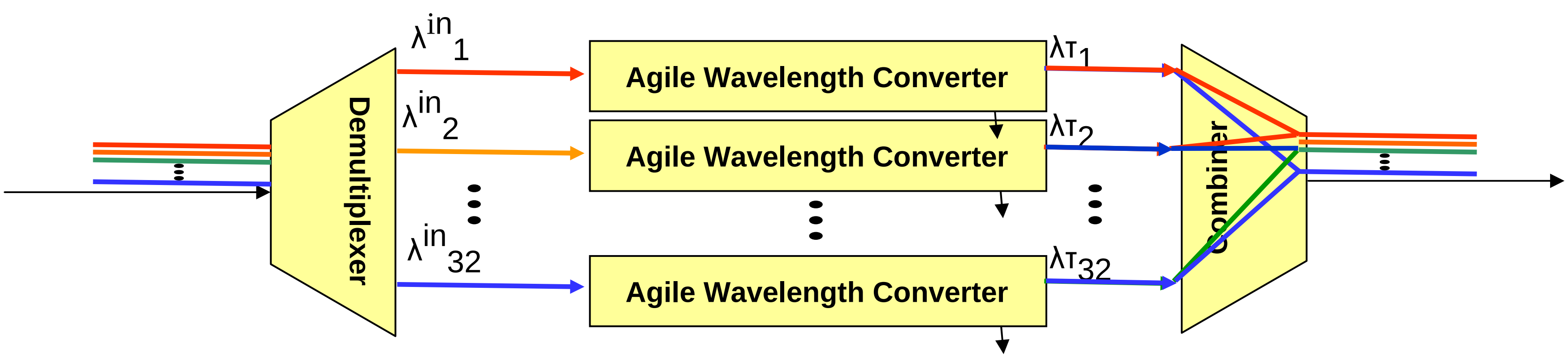
CS-WDM

All-Optical Switching on-Chip for DoD Applications

Wavelength/Space Switch



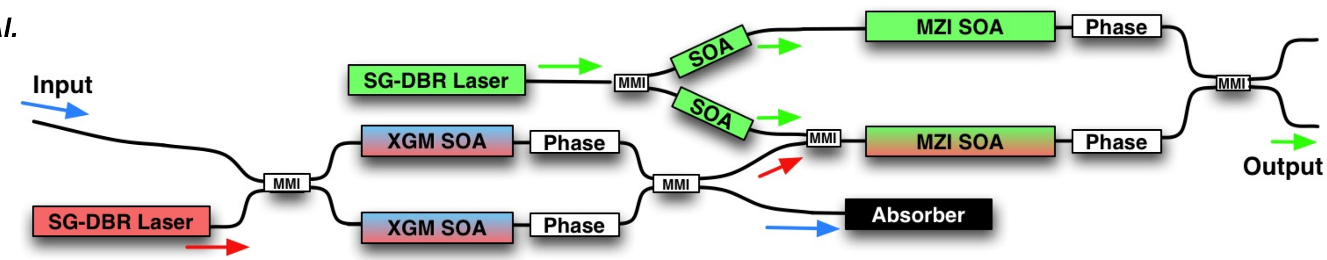
Wavelength Interchanger

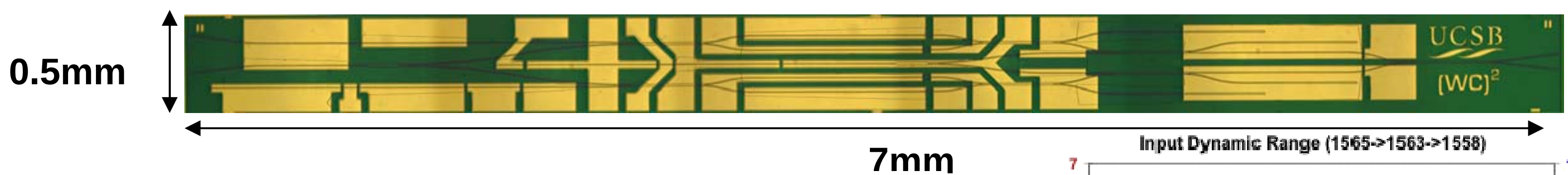


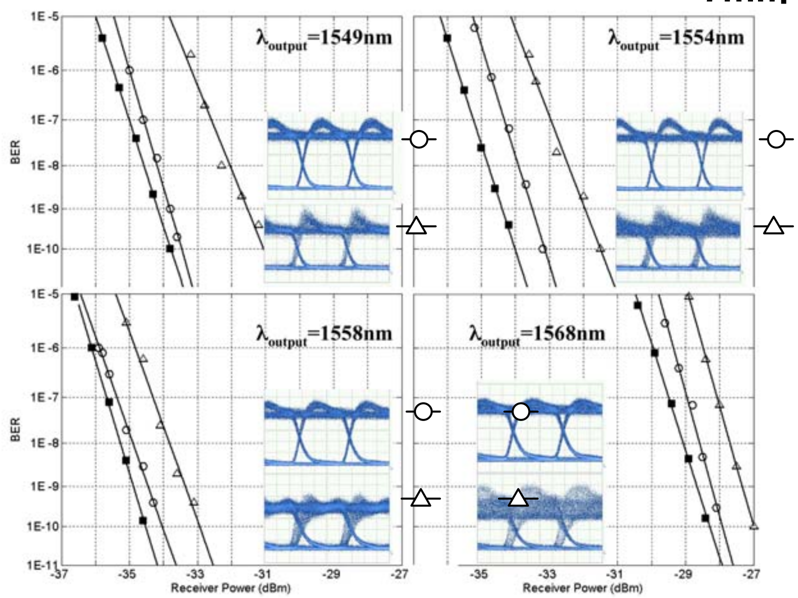
CS-WDM

2-Stage Tunable Wavelength Converters

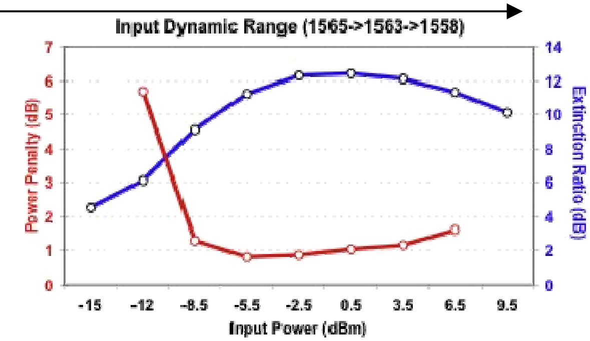
J. Summers, et. Al.

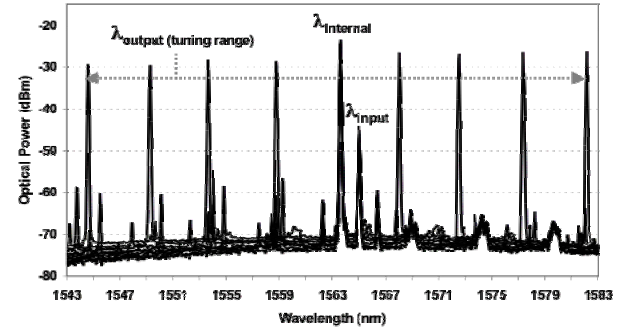






- Back-to-Back
- $\lambda_{input} \neq \lambda_{output}$
- $\lambda_{input} = \lambda_{output}$

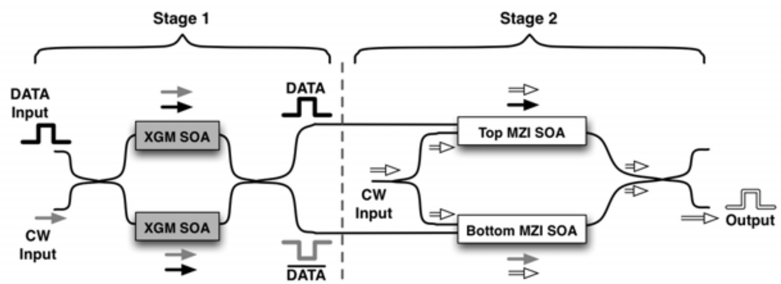


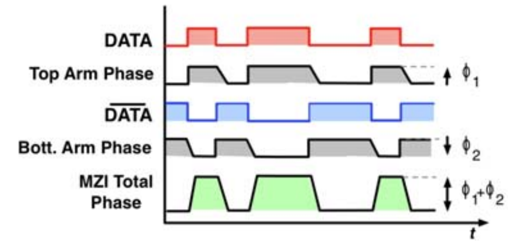


CS-WDM

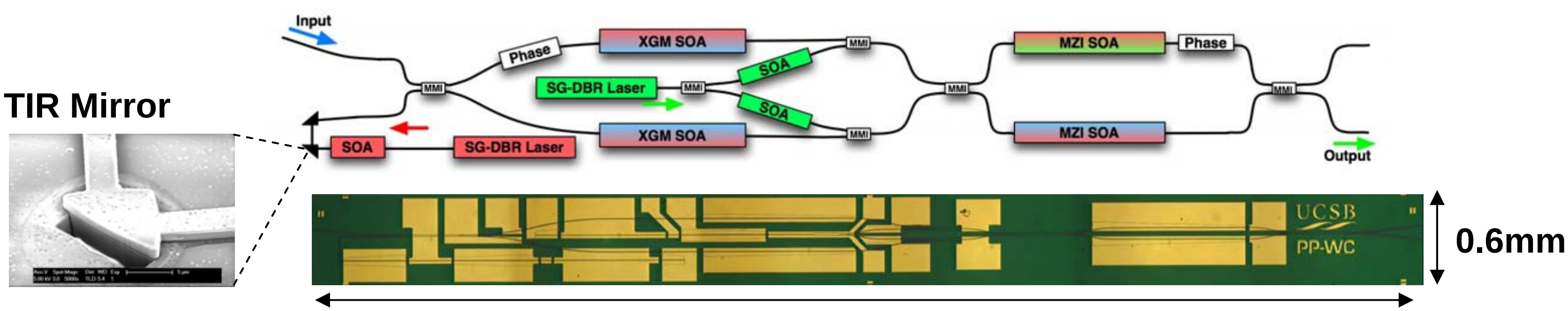
All-Optical Push-Pull Wavelength Converters

J. Summers, et. Al.



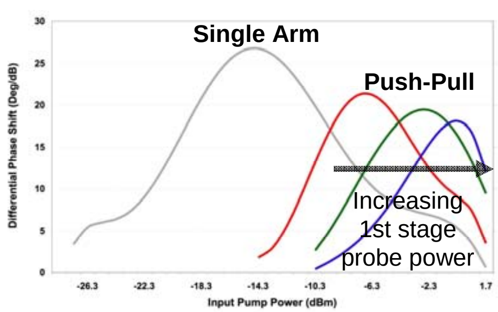


TIR Mirror

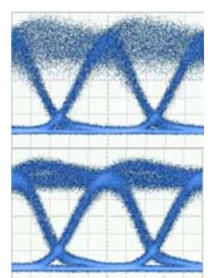


7mm

Phase Measurements



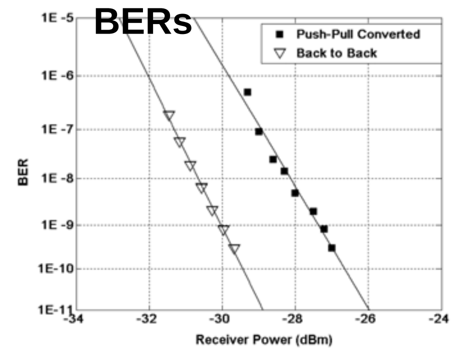
Eye Diagrams



Single Arm
-large phase swing
-poor noise (noise floor)

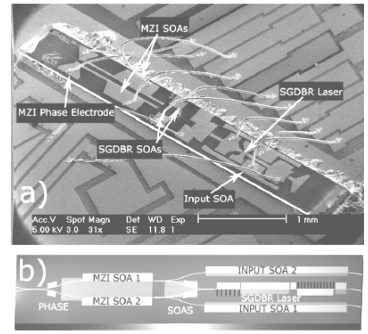
Push-Pull
-full π phase swing
-improved noise

BERs

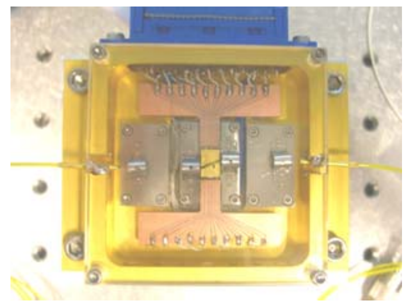


CS-WDM
Materials-Device-Function-System

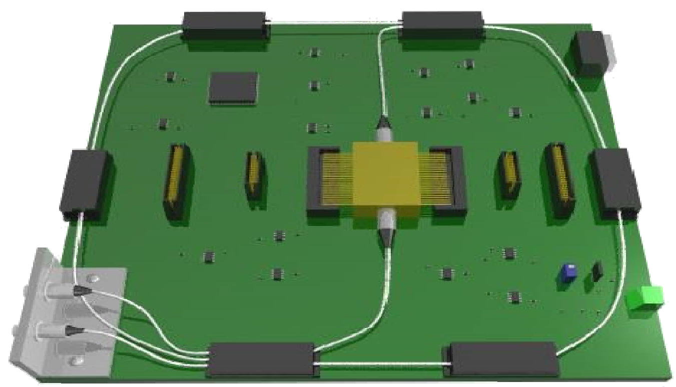
- 1^{st} generation: Feb. '04
  - Chip-on-carrier 2.5Gbs wavelength tunable all-optical wavelength converters sent to MIT-LL.



- 2^{nd} generation: Aug. '05
  - Packaged 2.5Gbps T-AOWCs sent to MIT-LL.

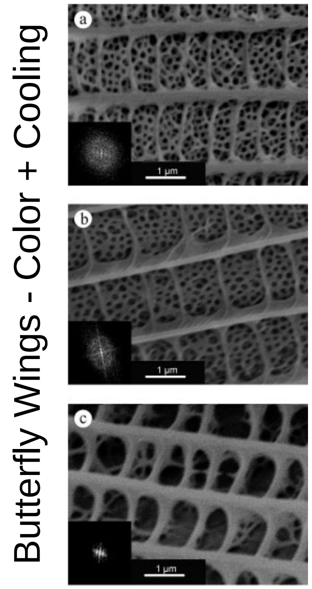


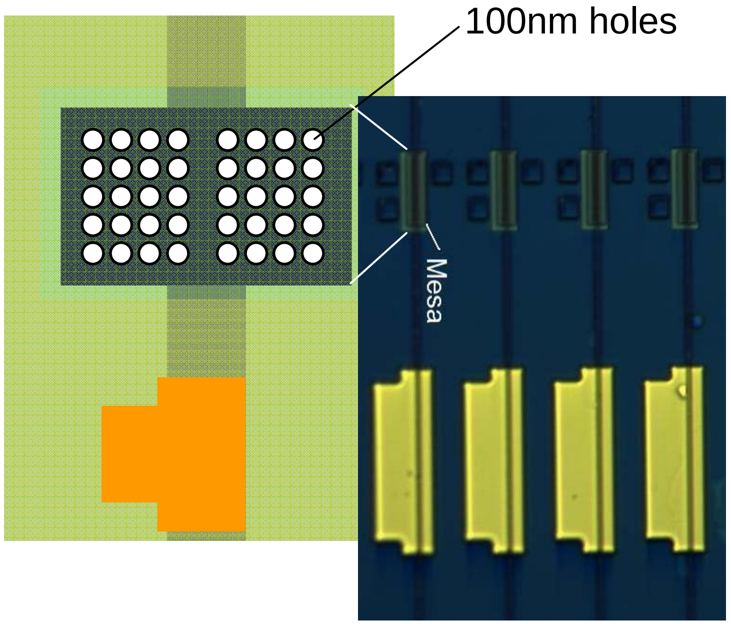
- 3^{rd} generation: Dec. '05 - Jan. '06
  - (4) x T-AOWCs packaged and integrated on control circuit boards installed on in-flight demo.



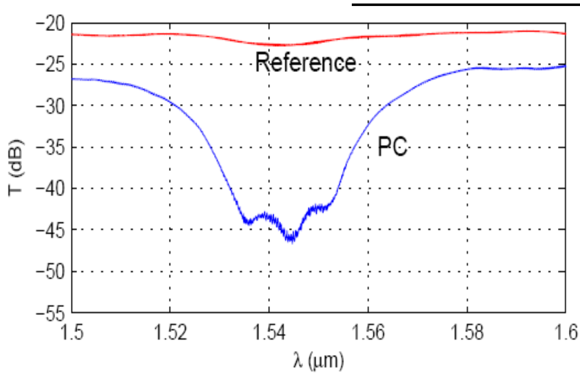
CS-WDM

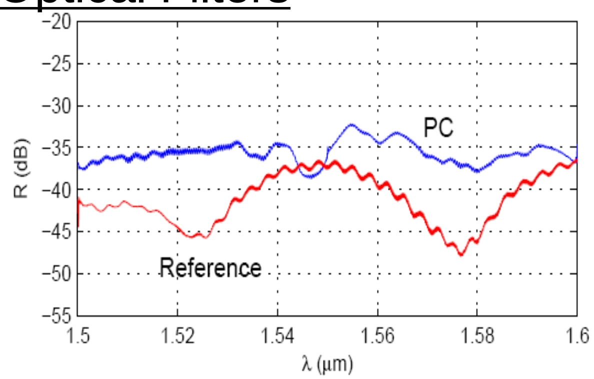
Manipulating Light with Photonic Crystals





Ultra-Short Optical Filters





L=30μm

M. Davanço, A. Xing, J. Raring, E. L. Hu, and D.J. Blumenthal" "Broadband Photonic Crystal Passive Filters for Monolithically Integrated InP Photonic Integrated Circuits," Submitted to OFC 2006.

LASOR

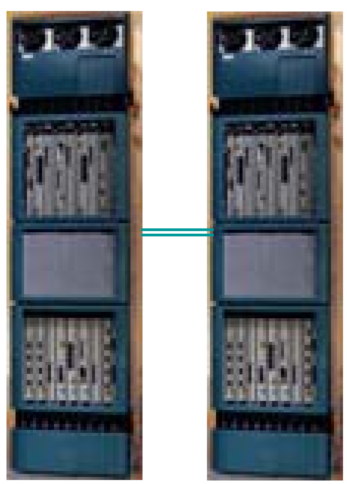
DoD-N

Were Does Integrated Photonics Fit into the Picture?

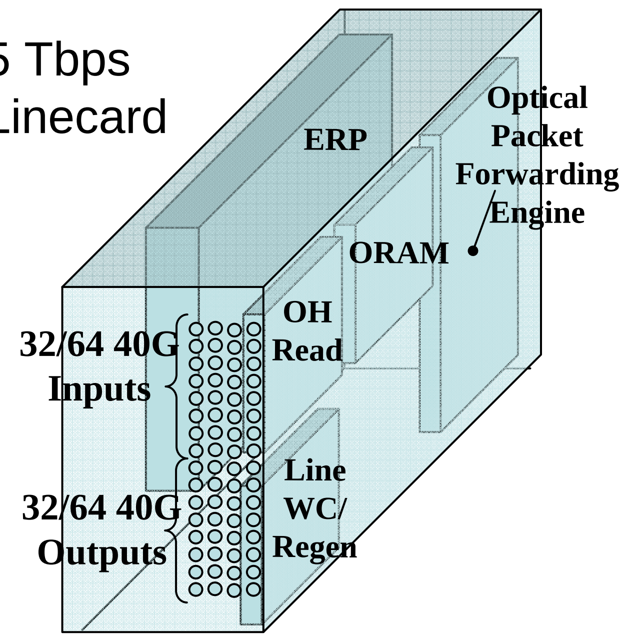
Process and switch photons around to reduce power → Integrate Photonic Functions onto a Chip to reduce size → Photonic Integrated Circuits (PICs) still at 1960s of Electronics → Research in:
- Physics
- Materials
- Devices and PICs
- Processing
- Architectures

- DARPA MTO DOD-N Program - LASOR (Haney, Shah)
  - UCSB: Blumenthal, Bowers, Coldren
  - Stanford: McKeown
  - Cisco
  - JDSU

Rack Rack

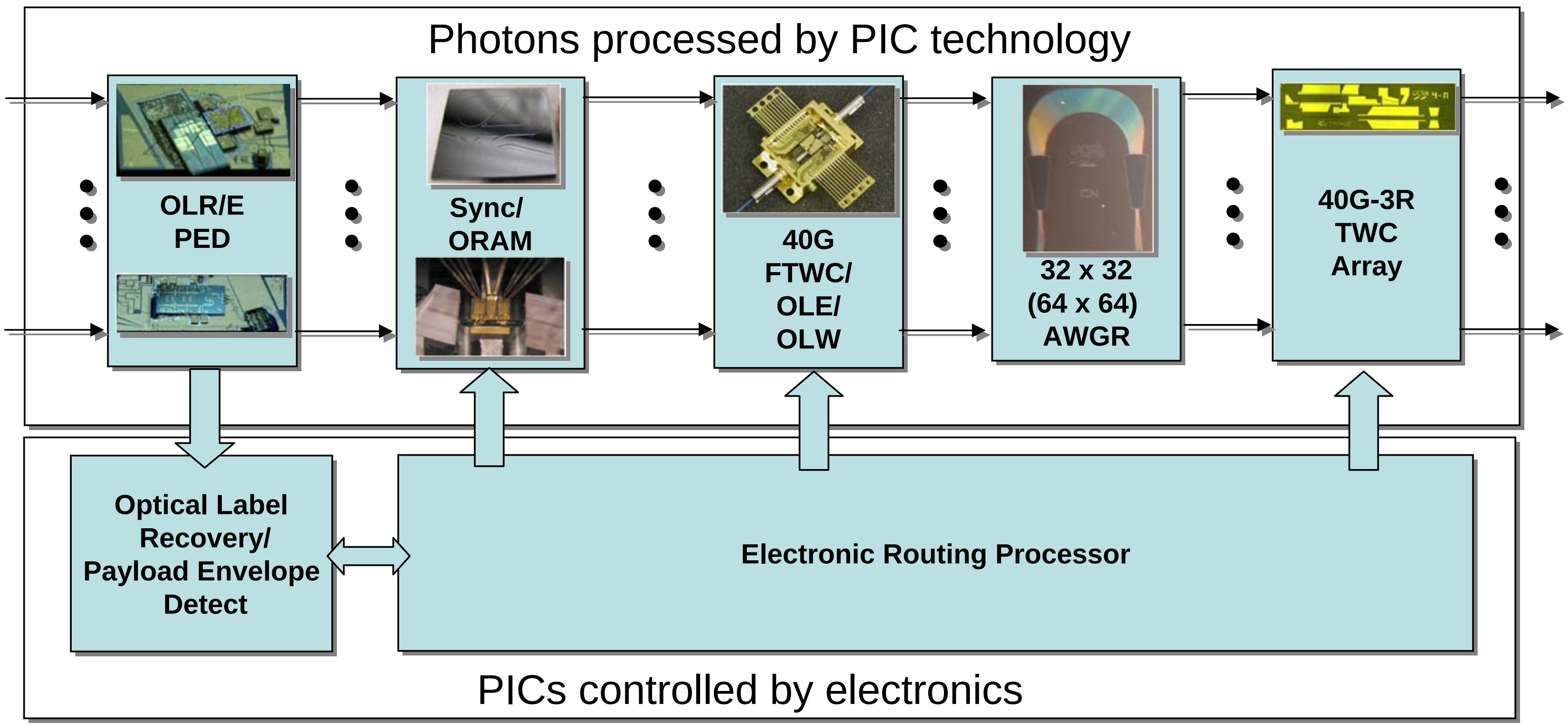


Today's Technology



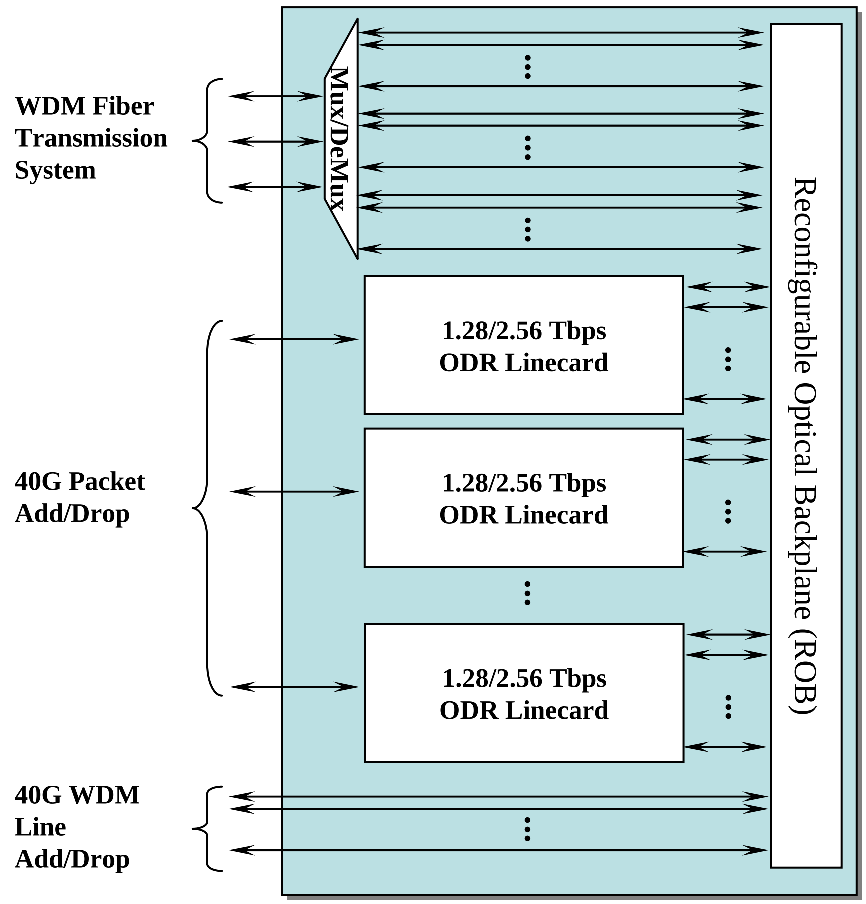
LASOR Optical Packet Router Linecard

Pushing envelope on density and functionality of InP and Silicon Photonics

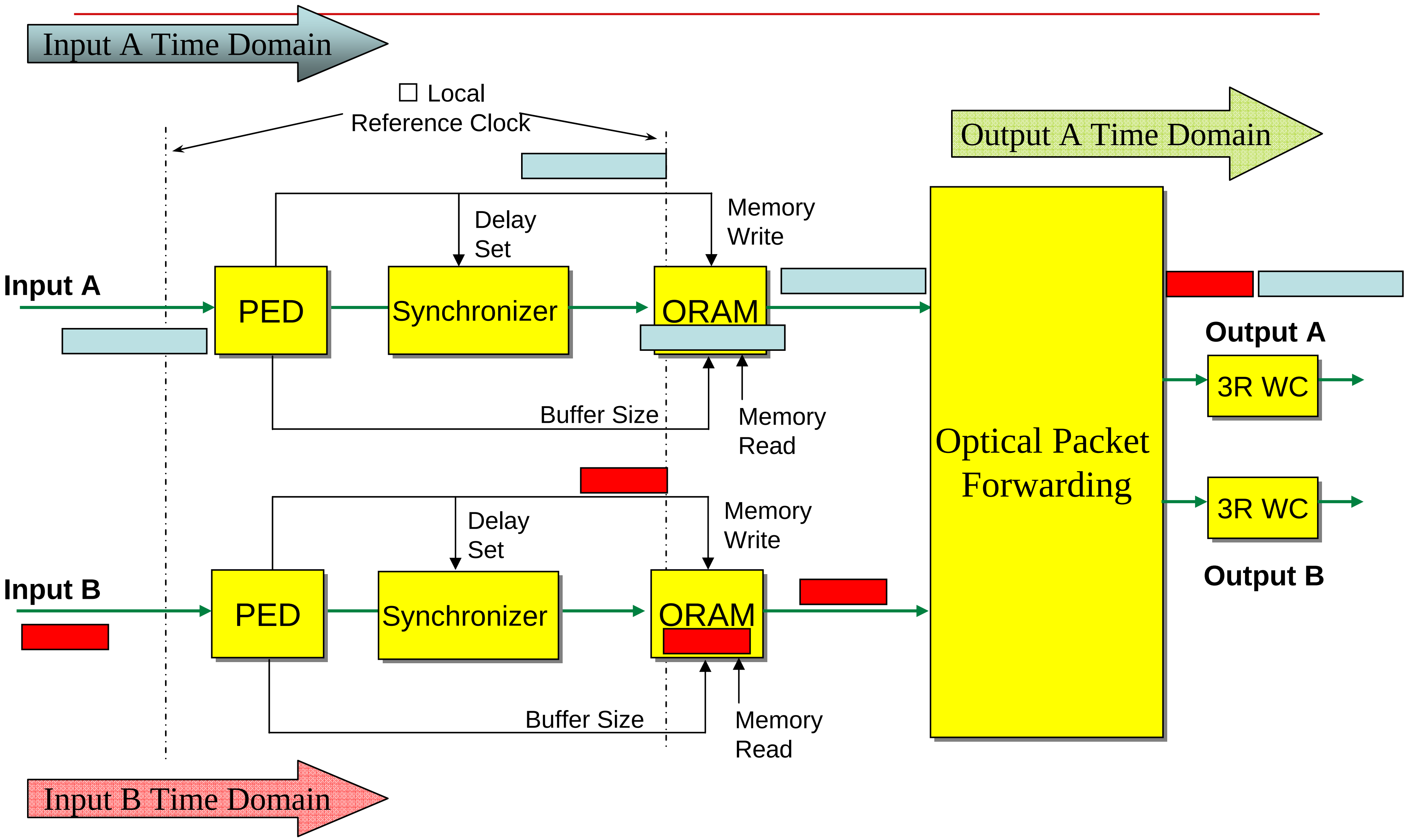


100 Tbps Optical Routing Node

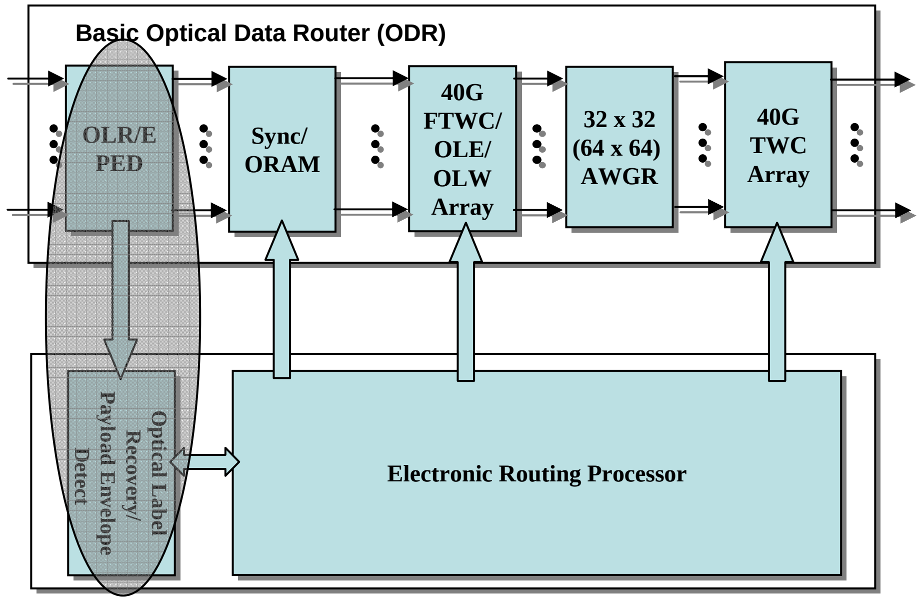
- Linecards connected to WDM transmission system and local ports via ROB
- Optical express paths added to linecard
- ISP traffic engineering applied to realize 100 Tbps capacity
- Supports multiple architectures
  - Multistage
  - Distributed
  - Balanced
- Support any ratio of express WDM traffic, optically packet routed traffic, and added/dropped traffic
- Modular capacity growth of WDM on a link-by-link basis



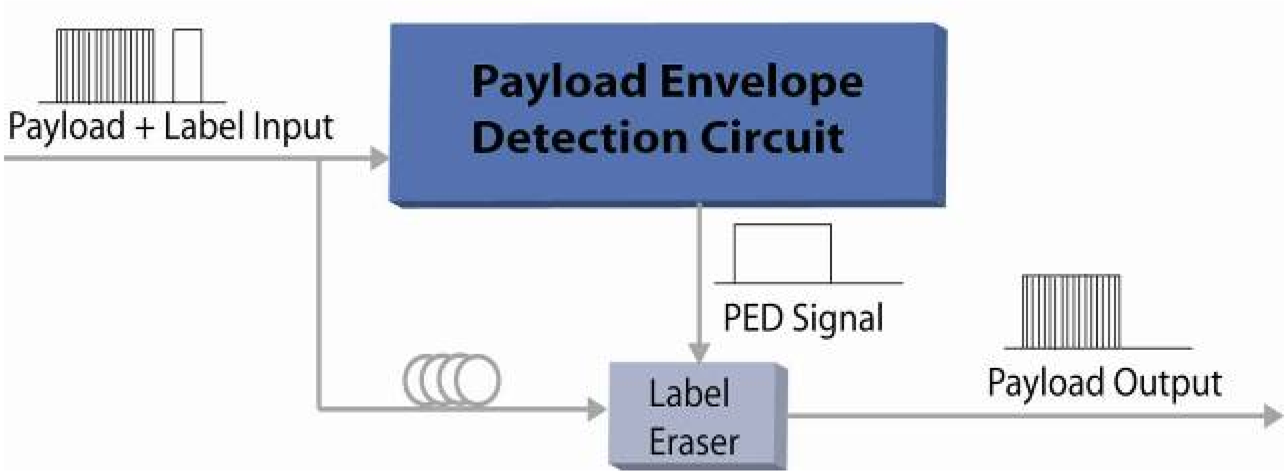
Optically Buffered ODR



Optical Header Recovery and Payload Envelope Detect

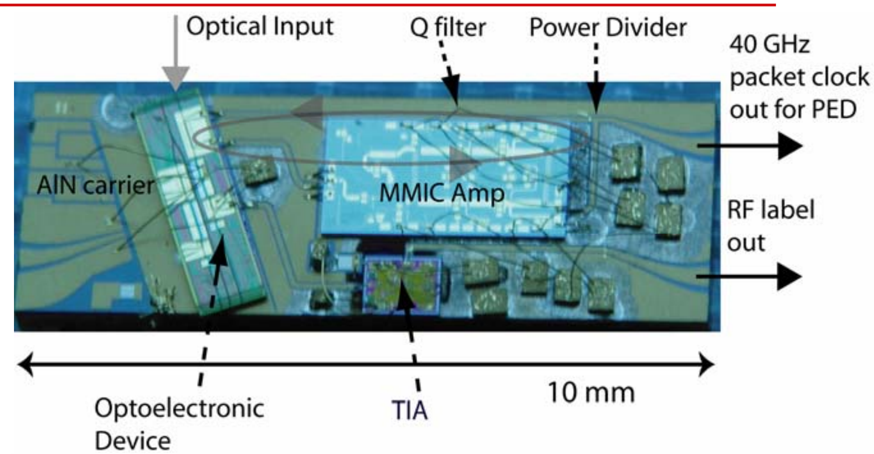


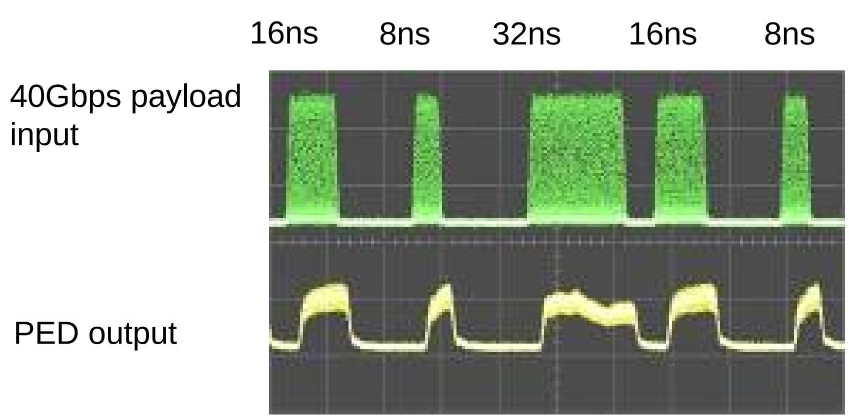
Payload Envelope Detection (PED)

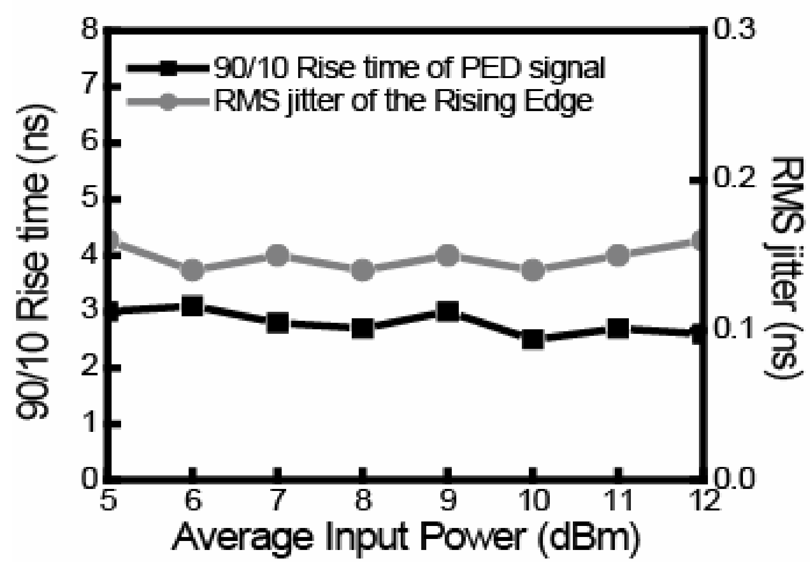


Phase 1 Hybrid PED

- **Hybrid Integrated Optoelectronic Payload Envelope Detection (PED) device**
  - variable length PED signals generated
  - 3ns rise/fall time
  - 150 ps RMS jitter
  - ~7 dB input power dynamic range
  - Removed and inserted labels using this PED signal with <1dB power penalty

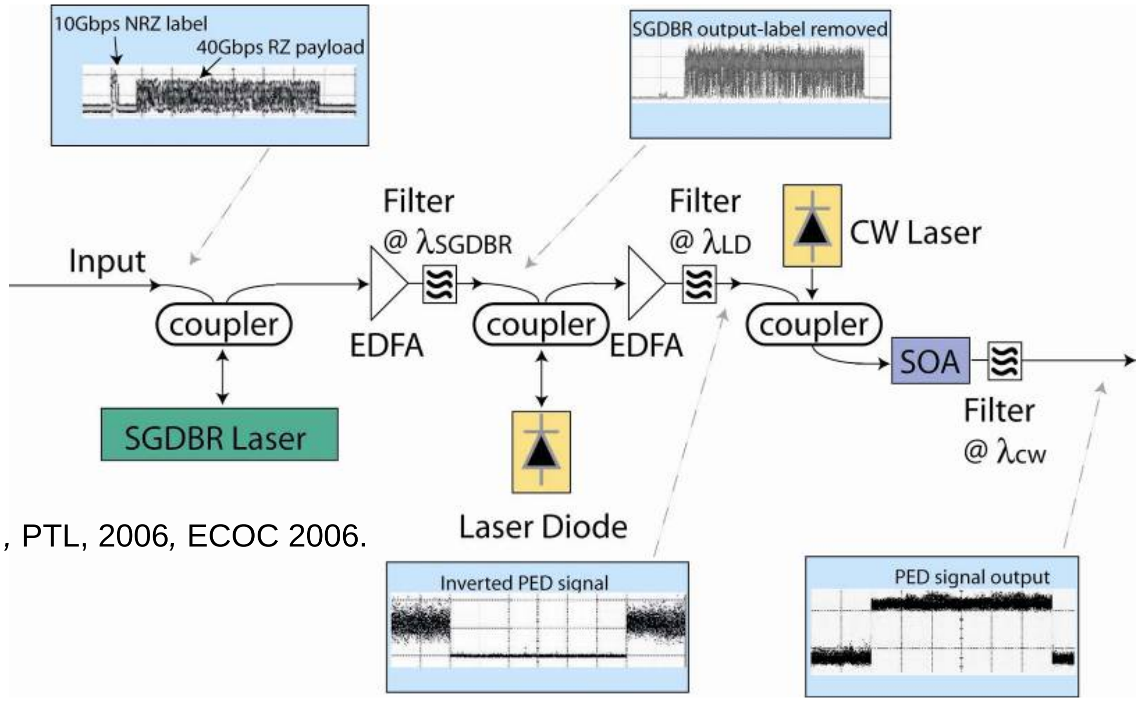






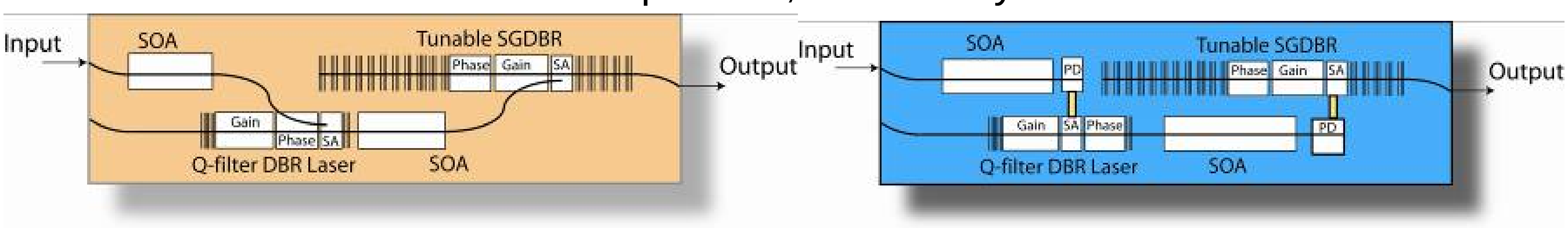
Ref: Koch *et al.*, OFC 2006, JLT, 2006, *Optics Express,* 2006.

Phase II - All-Optical PED



Ref: Koch *et al.,* PTL, 2006, ECOC 2006.

Integrated all-optical PED: Compact, single component, low power consumption, Less expensive, low latency

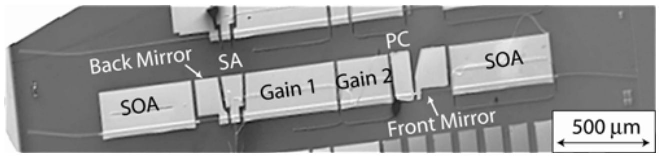


All-Optical 3R Regeneration

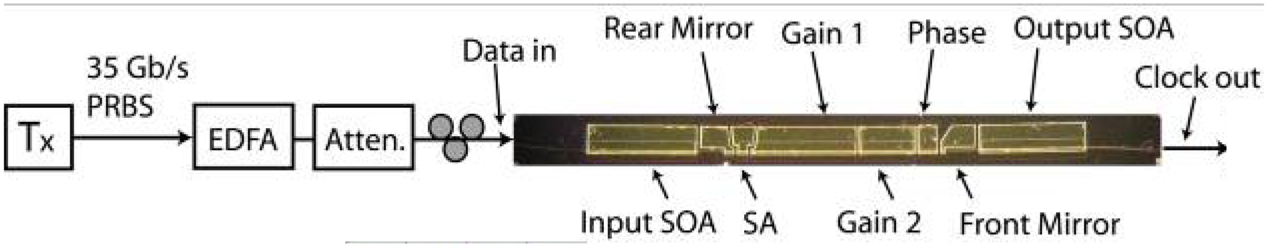
- Goals
  - Precisely determine the repetition rate
  - Very high quality pulse reshaping and re-timing
  - integrated all-optical 3R regenerator

- Approach
  - Integrated Mode Locked Lasers with optical gates
  - Short, transform limited pulses
  - Very high extinction ratios
  - High output powers possible
  - Integrate MLLs with other components

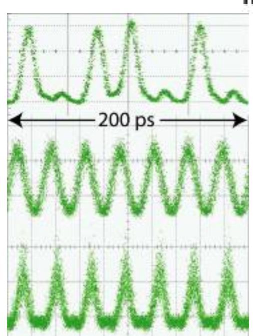
40 GHz InP MLL



Clock Recovery with tunable output pulsewidth



Ref: Koch et al. OFC 2007

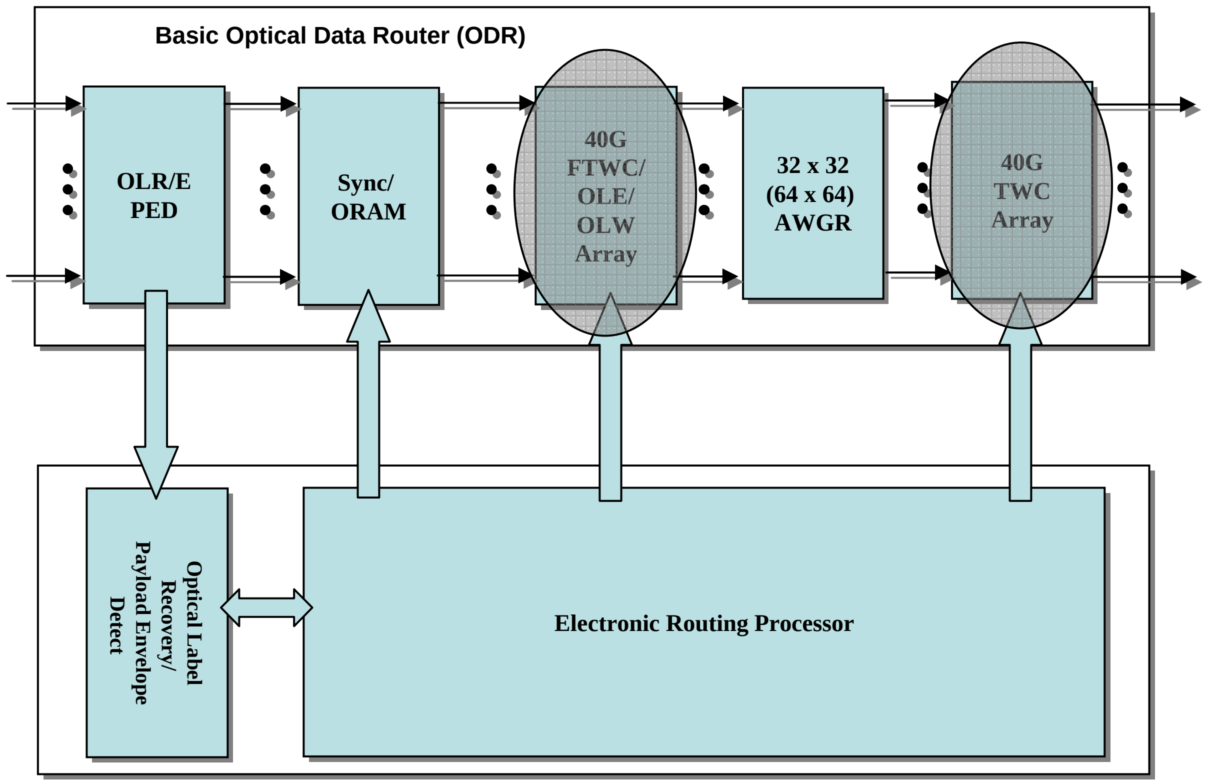


Data input

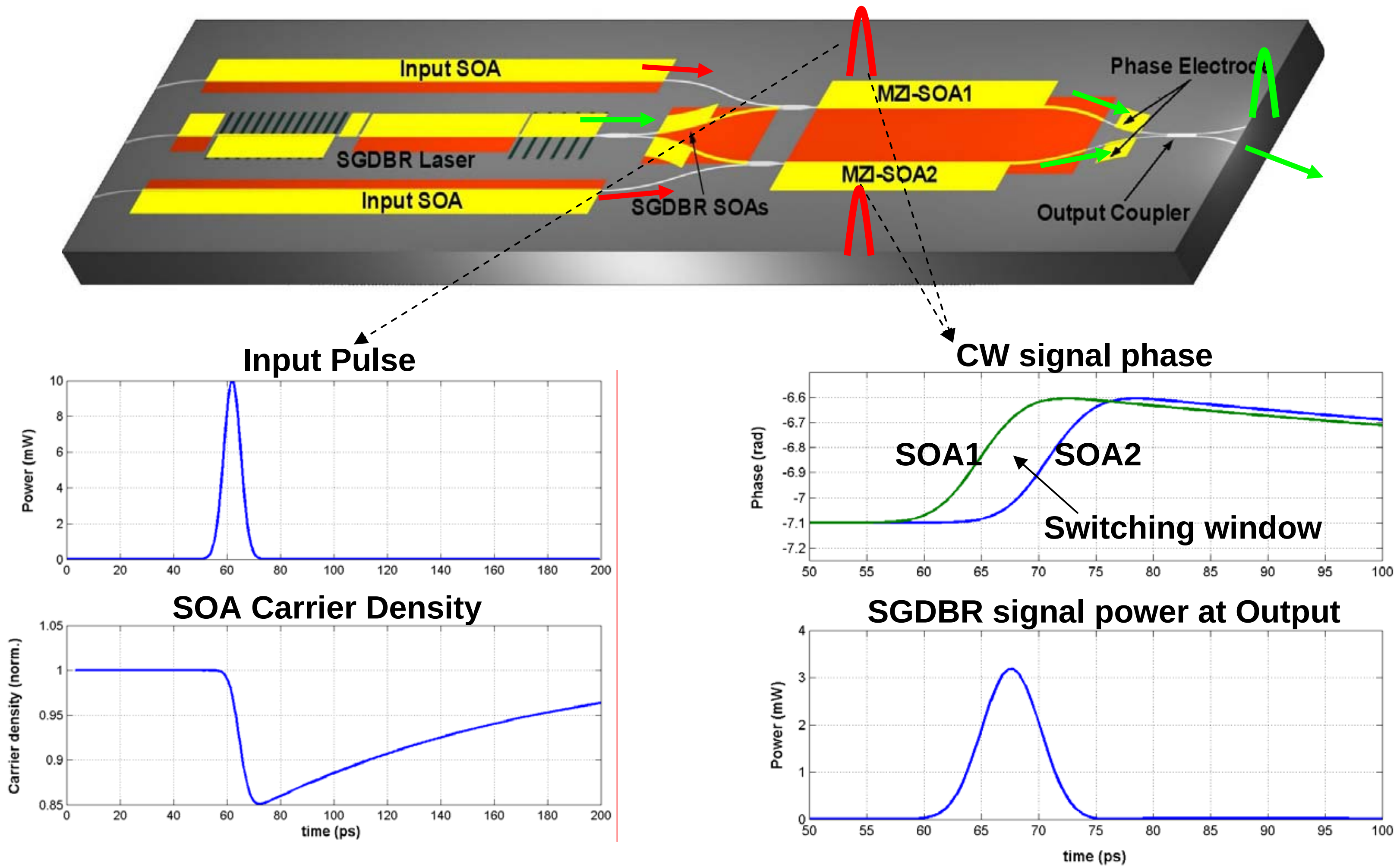
Clock output

Clock output under different bias conditions

40Gbps Wavelength Converter Technology



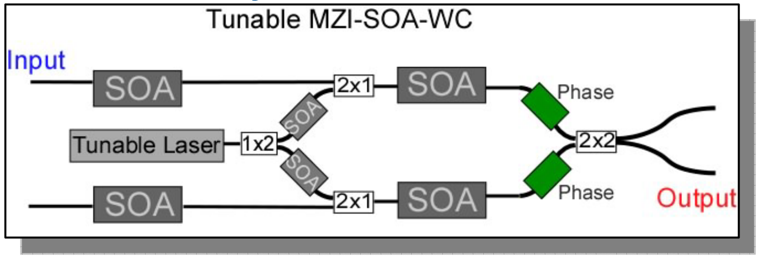
40Gbps Packet WC: Operating Principle



40Gbps Monolithic Widely-Tunable Differential Wavelength Converters

Gen. 1 : External Delay

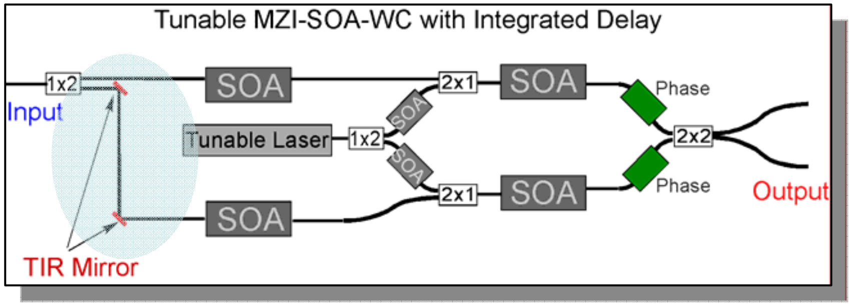
Chip Area = 2.5mm²



V. Lal, M. L. Mašanović, J. A. Summers, L. A. Coldren, and D. J. Blumenthal, "40Gbps Operation of an Offset Quantum Well Active Region Based Widely Tunable All-Optical Wavelength Converter,"Optical Fiber Communication Conference, Anaheim, California, 2005.

Gen. 2 : Integrated Input Differential Delay

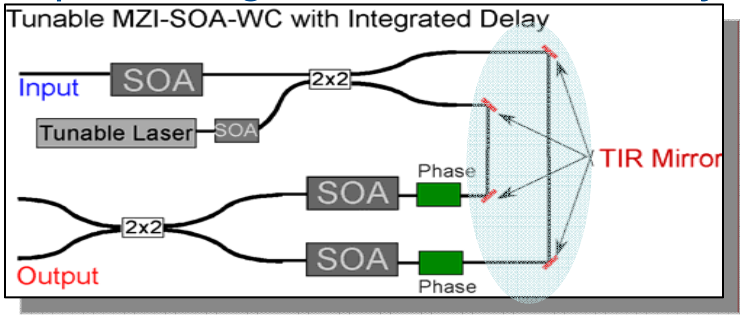
Chip Area = 3.8mm²



J. A. Summers, V. Lal, M. L. Mašanović, L. A. Coldren, and D. J. Blumenthal, "Widely-Tunable All-Optical Wavelength Converter Monolithically Integrated with a Total Internal Reflection Corner Mirror Delay Line for 40Gbps RZ Operation," Integrated Photonics Research and Applications (IPRA '05), Paper IMC5, San Diego, California, April 11-13, 2005.

Gen. 3 : Compact Integrated Balanced Delay

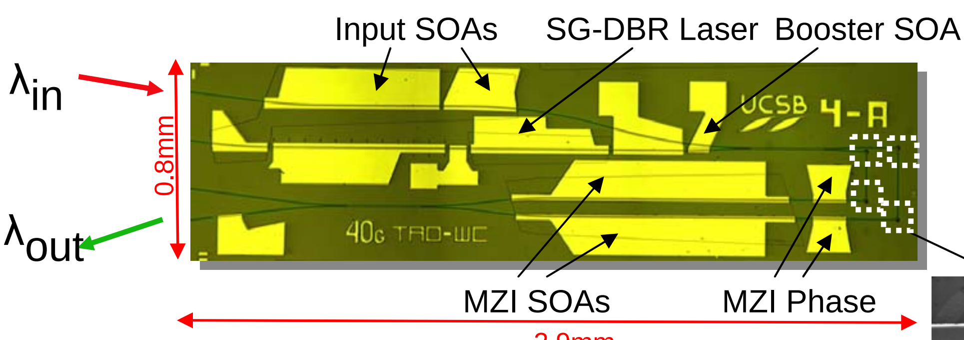
Chip Area = 2.4mm²

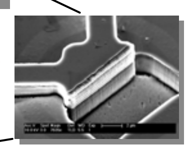


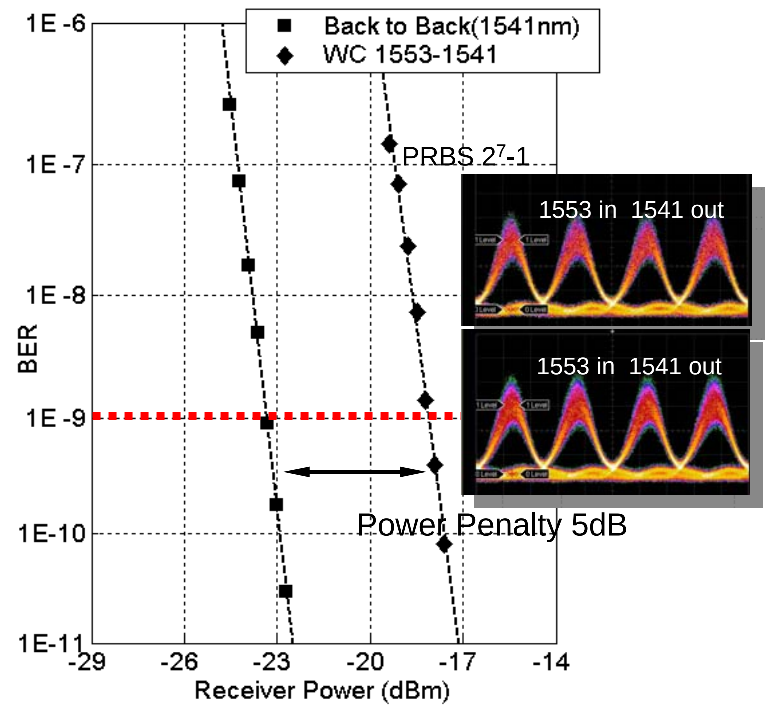
V. Lal, J. A. Summers, M. L. Masanovic, L. A. Coldren, and D. J. Blumenthal, "Novel Compact InP-based Monolithic Widely Tunable Differential Mach-Zehnder Interferometer Wavelength Converter for 40Gbps Operation," Indium Phosphide and Related Materials, Opto-I (IPRM '05), Glasgow, Scotland, May 8-12.

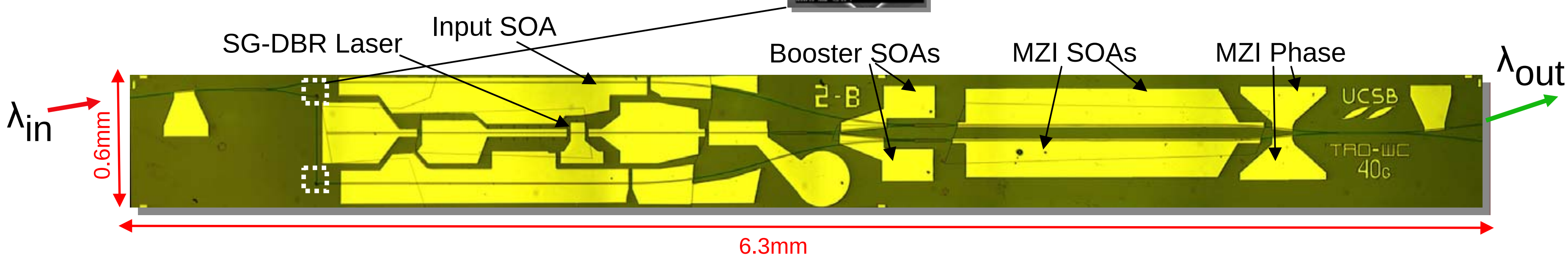
40G Tunable Wavelength Converters with Integrated Delay

- World's First Monolithic Integrated 40G Tunable All-Optical WC
- On-chip delay lines using TIR mirrors for RZ operation
- Optical preamplifiers
- Optical power splitters and combiners
- Mach-Zehnder interferometer optical wavelength converter
- Tunable laser
- Laser booster optical amplifier



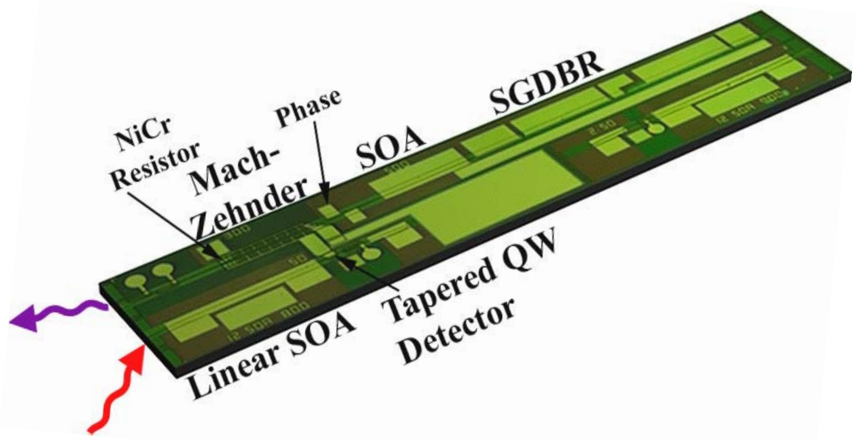




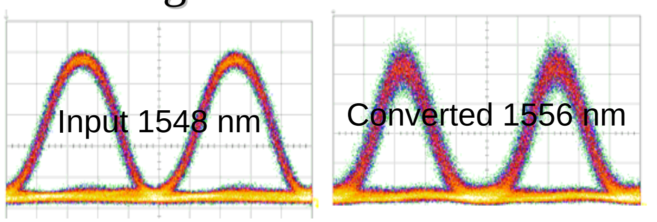


Field-based Monolithic Wavelength Converters

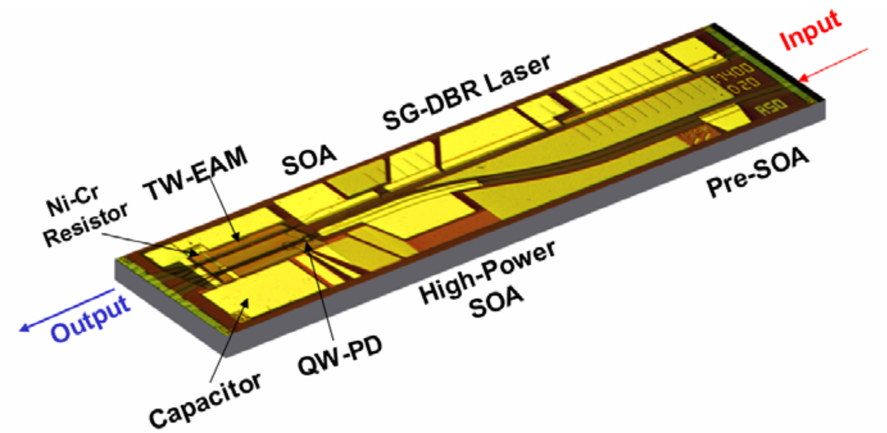
Mach-Zehnder



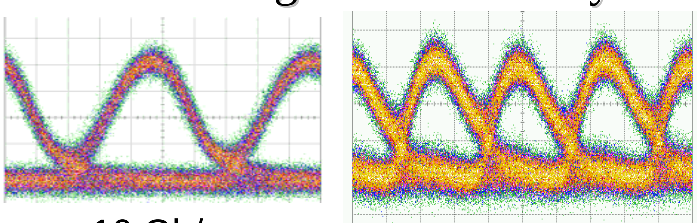
Wavelength Conversion at 10 Gb/s



Electro-Absorption



Wavelength Converted Eyes



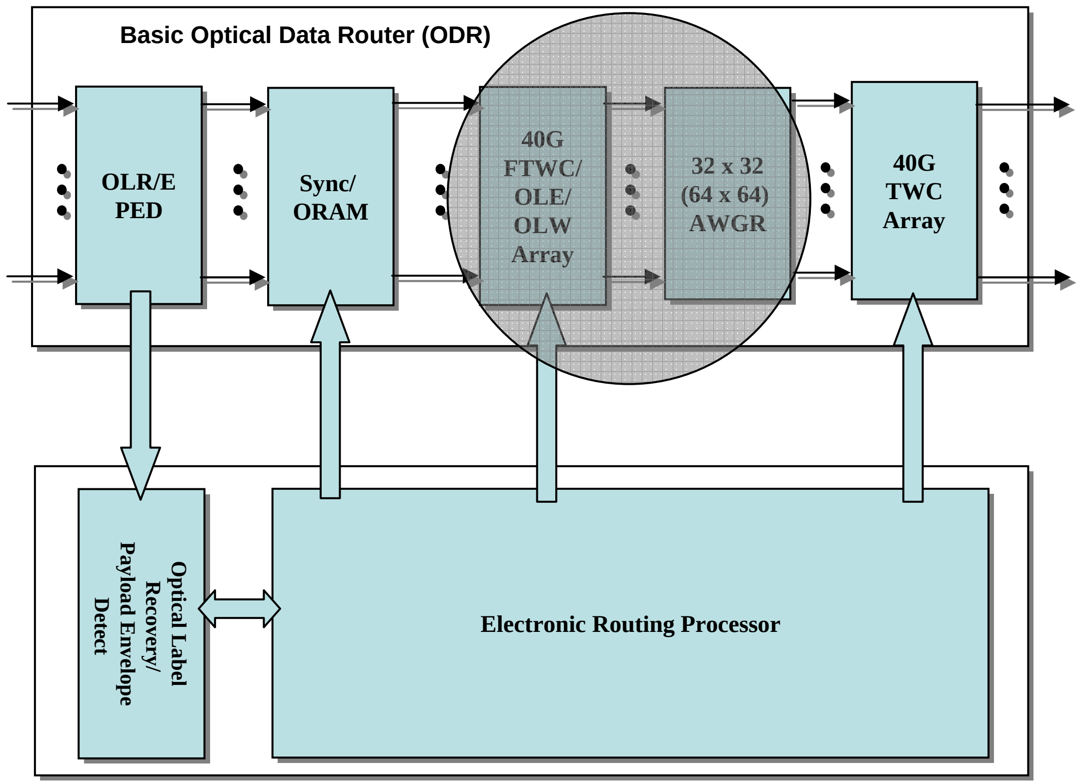
10 Gb/s

20 Gb/s

- Integrated RF interconnections and terminations
- Bandwidth greater than 20 GHz
  - Frequency response limited by QW detectors

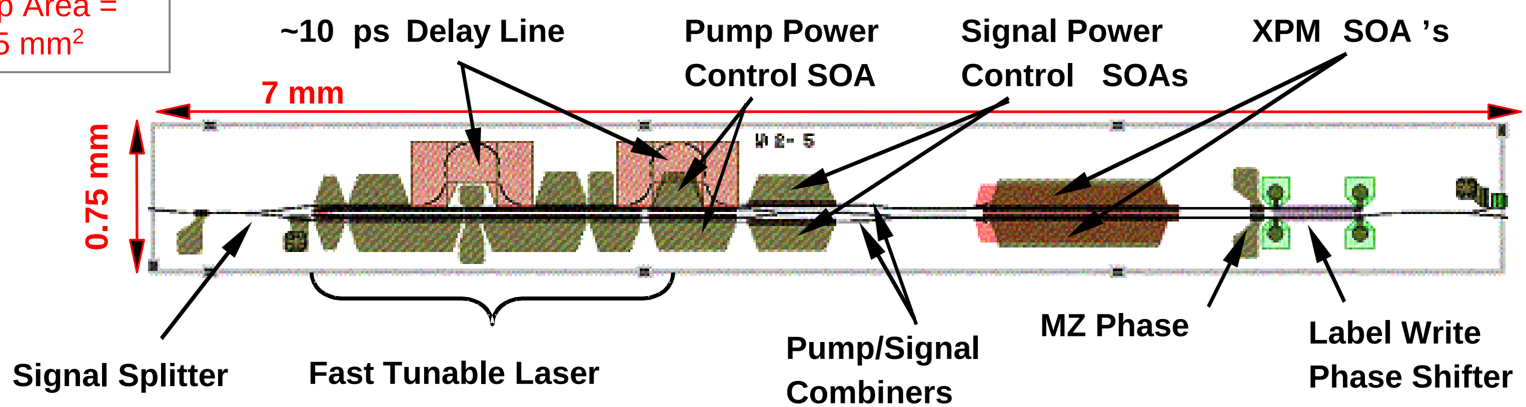
A. Tauke-Pedretti, J. Barton, L. JohanssonM. Dummer, M. Sysak, J. Raring, L. Coldren

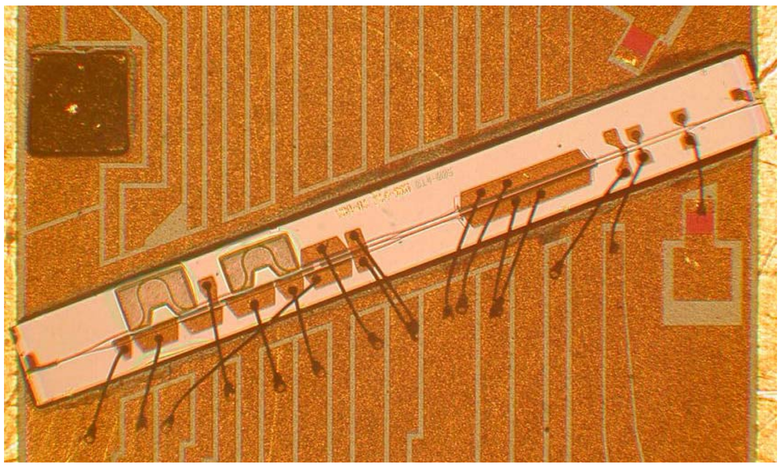
Packet Forwarding

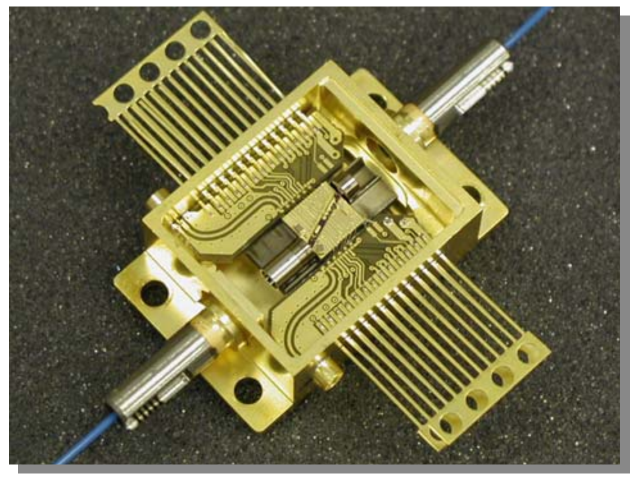


PFC Chip and Module

Chip Area = 5.25 mm^2

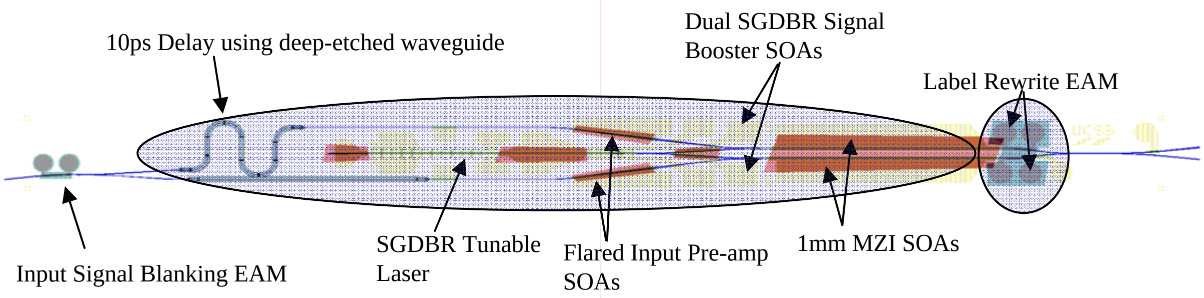


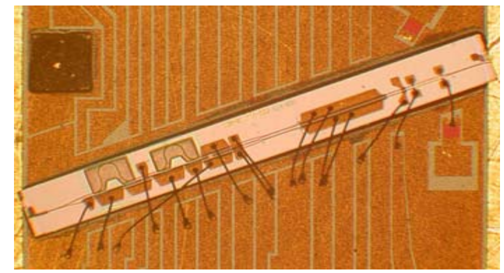




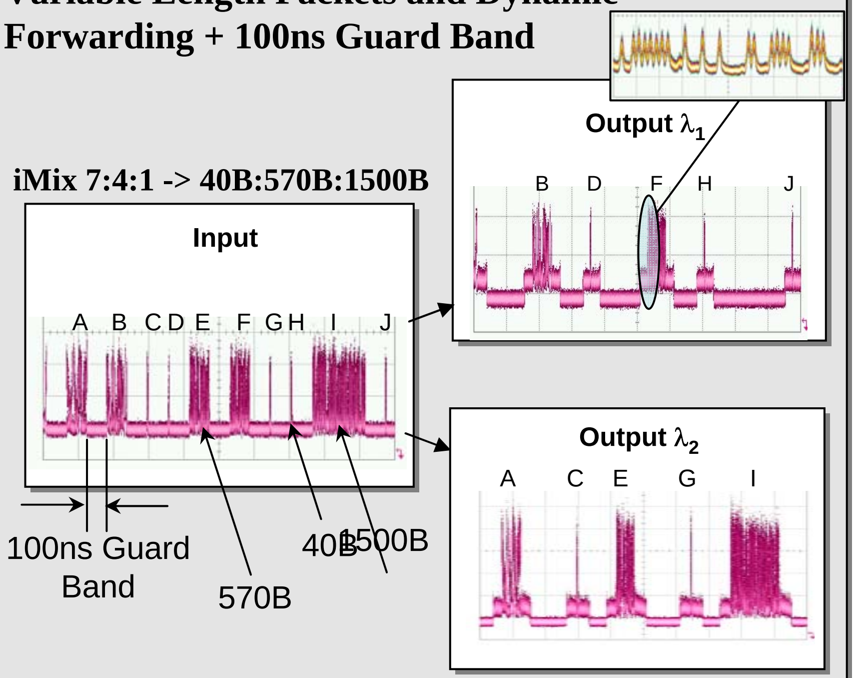
"Monolithic Widely Tunable Optical Packet Forwarding Chip in InP for All-Optical Label Switching with 40 Gbps Payloads and 10 Gbps Labels," V. Lal, M. Mašanović, D. Wolfson, G. Fish, C. Coldren, and D. J. Blumenthal, Accepted for presentation as Postdeadline Paper, ECOC 2005 Glasgow, Scotland.

PFC Packet λ-Conversion and OH Re-Write

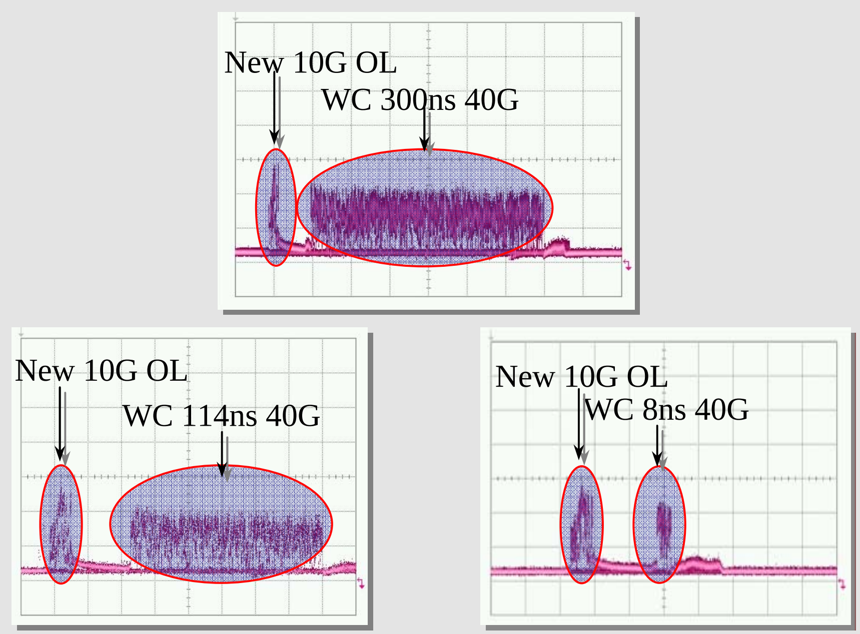




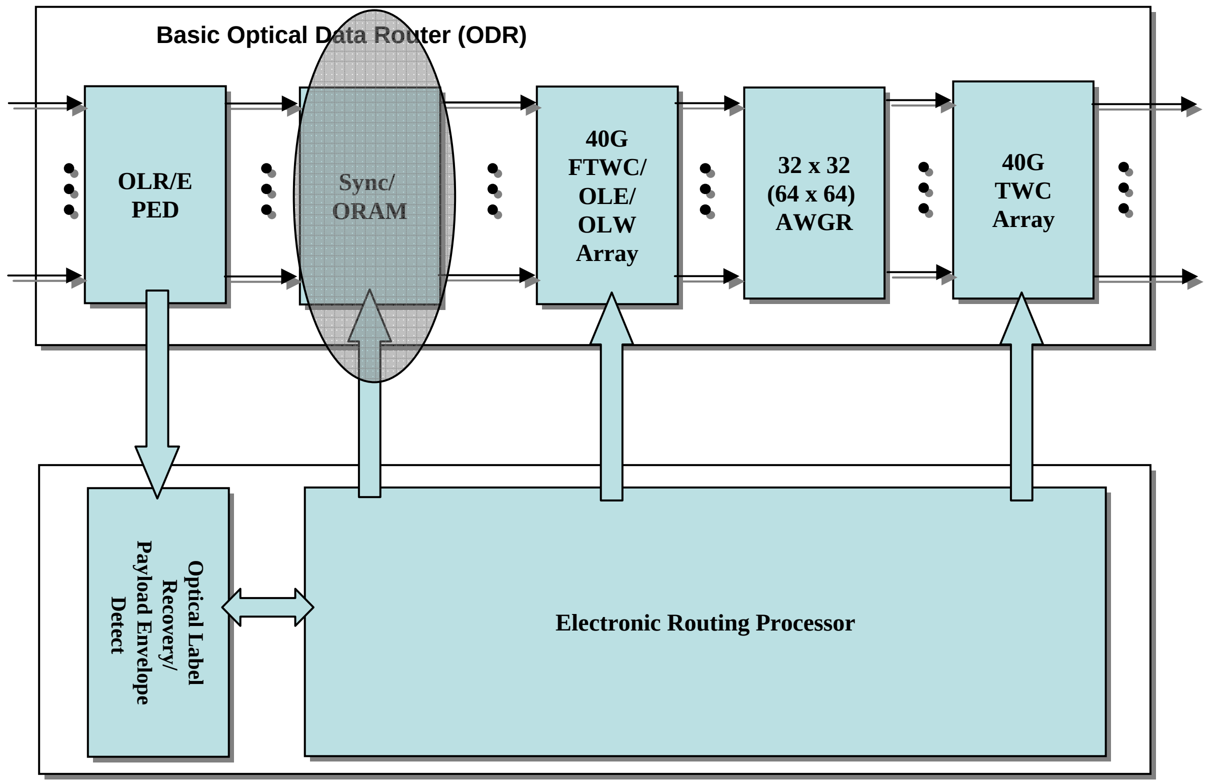
Variable Length Packets and Dynamic Forwarding + 100ns Guard Band



10G Optical Header Re-Write

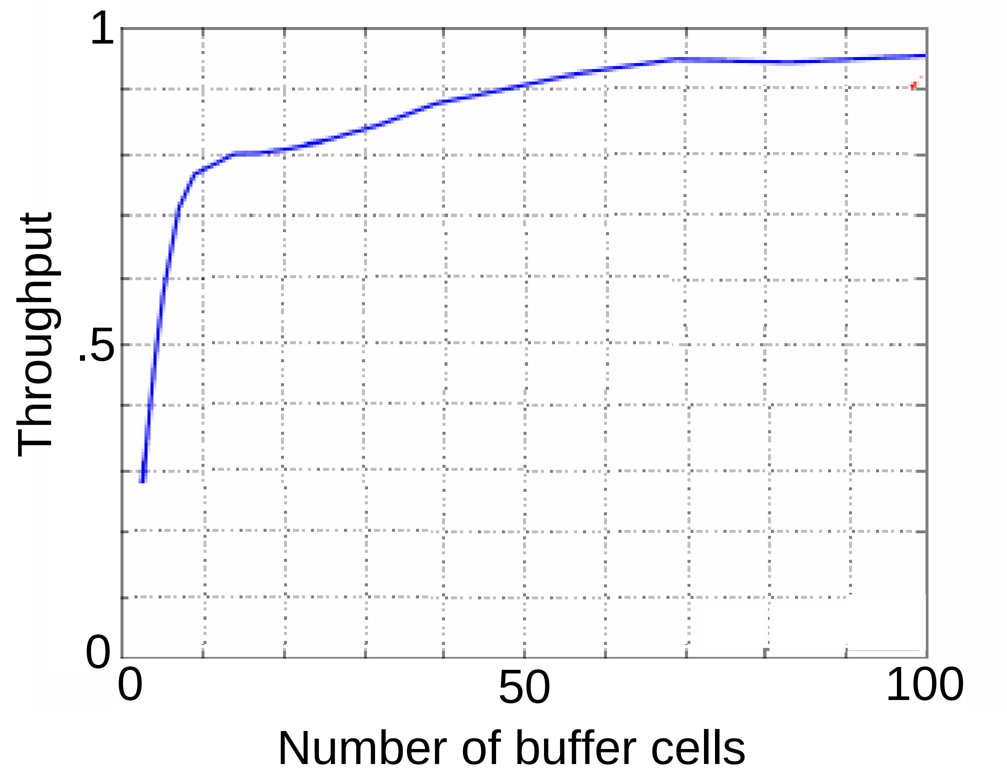


Synchronizers and Buffers



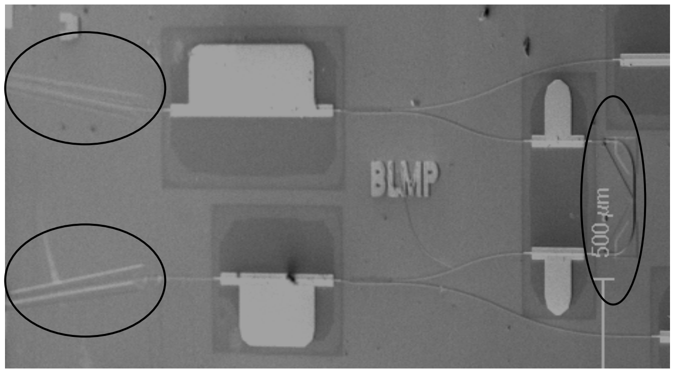
Small Buffer Performance

- Optical routers will receive access flows at much lower bandwidths than backbone links
  -> naturally spaces packets
- Small numbers of buffers make a large difference.
- Only 20-50 buffers are needed (assuming customer is willing to sacrifice 25% of link capacity)
- Studies were performed by Professor McKeown's group (Enachescu et al ACM/SIGCOMM 2005)

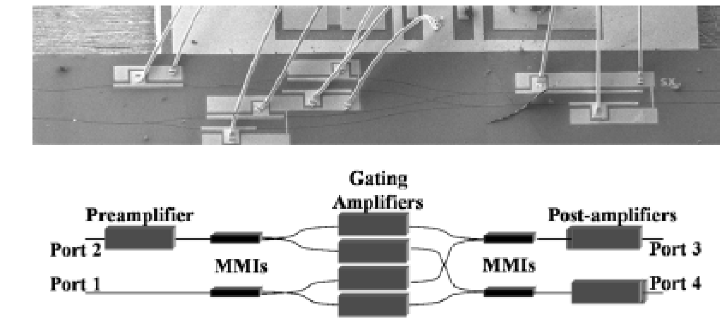


*Output-queued router. An increase of **60%** in throughput is achieved with <**15** buffers.*

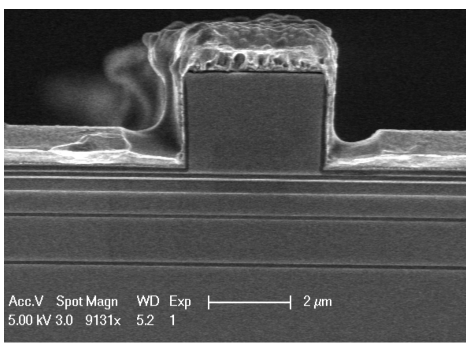
Hybrid Recircualating Packet Buffers



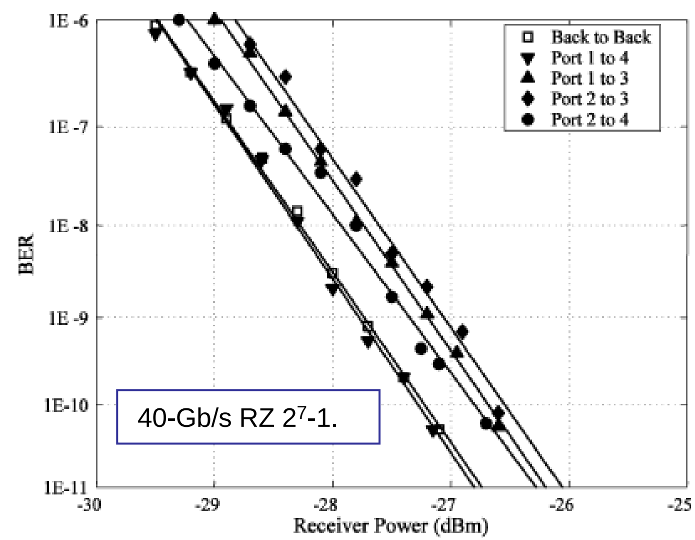
Input and output of a buffer showing spot size converters (left) and 90˚ bends (right).



Fabricated SOA gate matrix switch wirebonded to an aluminum nitride submount.

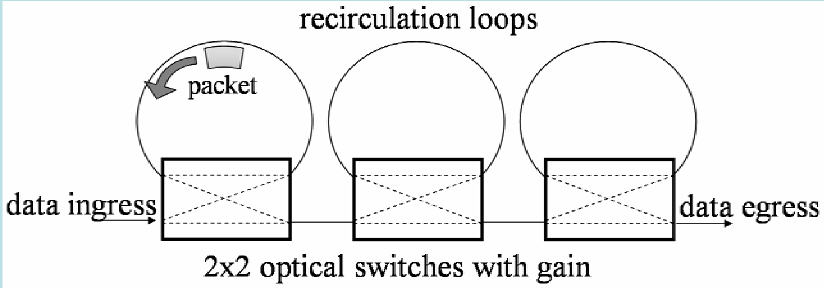


Epitaxial layers, including lower two 1.2 Q layers for spot size conversion.



Optical Buffer (ORAM)

- Recirculating buffers for on-chip, integrated optical packet buffer with dynamic control of storage time and random read.



- Hybrid buffers are designed to combine the fast switching available with InGaAsP-based photonic chips and the low propagation loss available with silica waveguides.

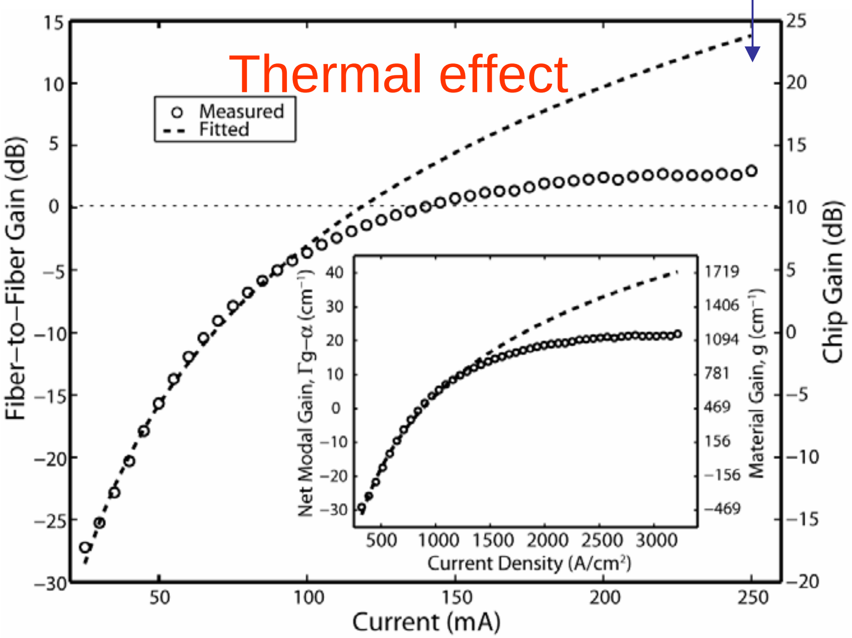
  - Silica waveguides have been designed and fabricated. Testing shows loss of less than 0.02 dB/cm.
  - Recent device fabrication shows good results on improved design features such as spot size converters and 90° bends, however out-sourced material regrowth created contamination which limited performance.
  - InGaAsP gate matrix switches were designed, fabricated, and tested. Error-free performance was shown with negligible power penalty. [Burmeister, *Photon. Technol. Lett*., vol. 18, no. 1, 2006].

LASOR

Integrated optical buffer-silicon evanescent amplifier

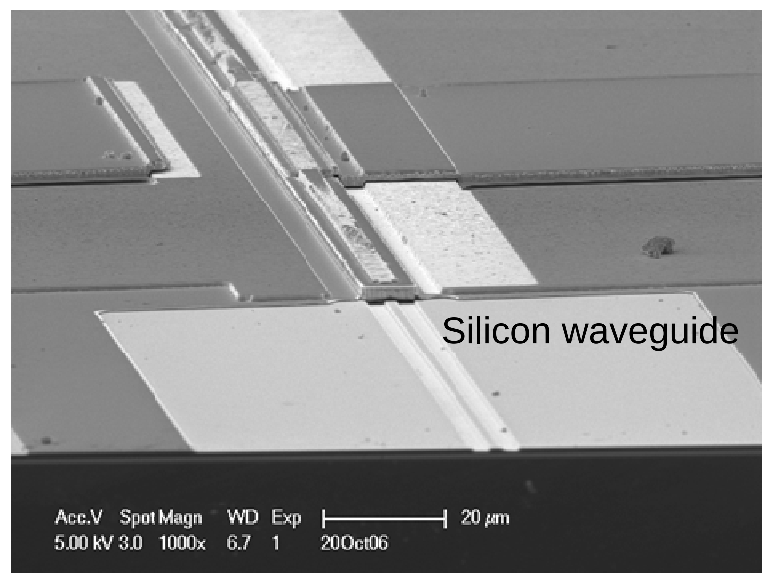
- **Long Term Goal:** Demonstrate fully integrated optical packet buffer.
- **Short Term Goals:** 1) Demonstrate 10 passes around loo . 2) Demonstrate gain based switch architecture.

- **1st generation results**
  - Maximum fiber to fiber gain: 3 dB
  - Estimated chip gain of 13 dB
  - Thermally limited by heat generation due to high series resistance



- **2nd generation Objectives**
  - Maximum gain > 20 dB
  - Silicon Input/Output waveguide for integration with silicon delay lines

- **Current status**
  - Fabrication is finished.
  - Gain ripple because of reflections at the junction of silicon and III-V section
  - Better transition design needed such as tapers on III-V side.



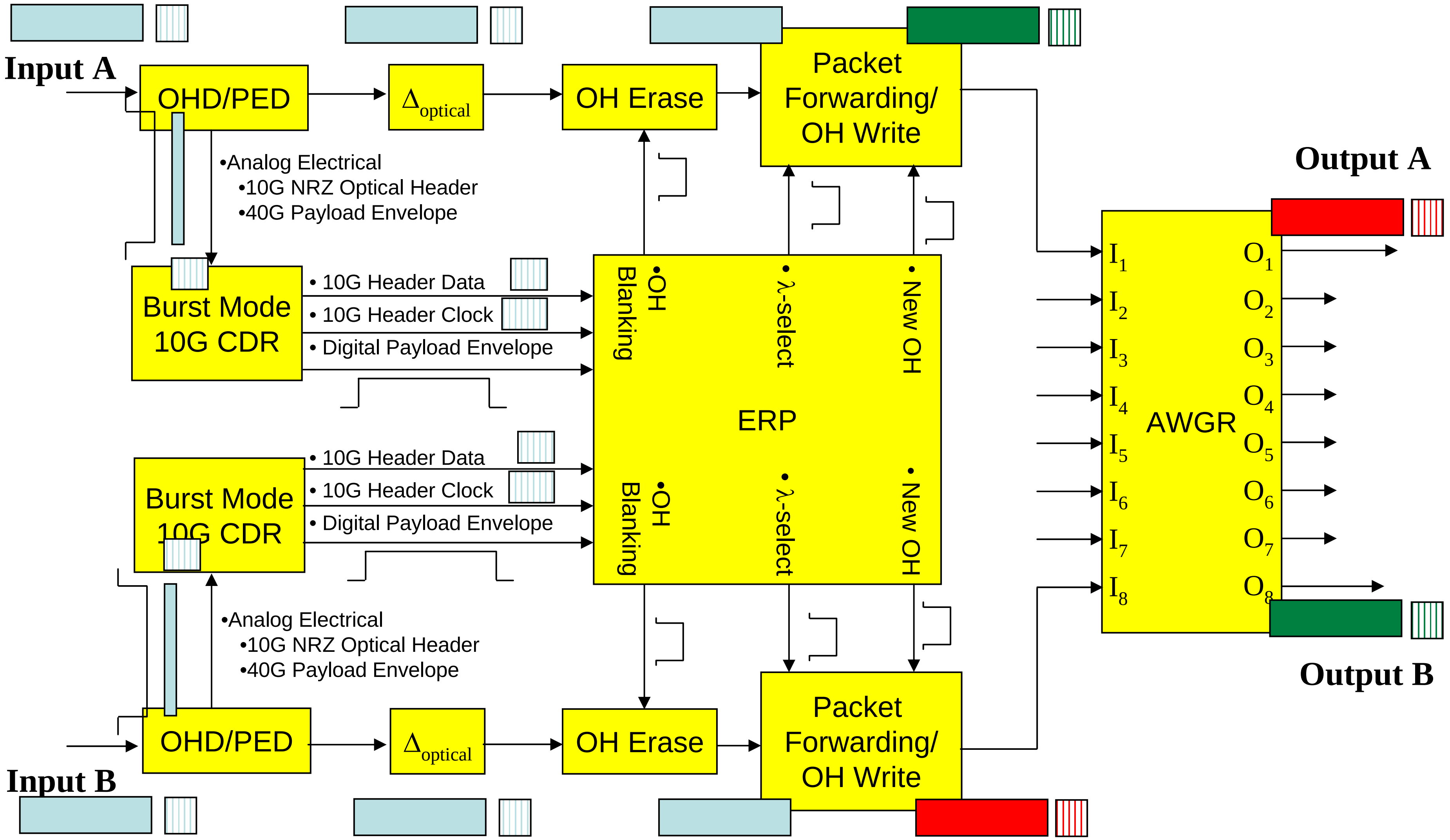
Chip Level 2x2 Optically Buffered ODR

Movie File

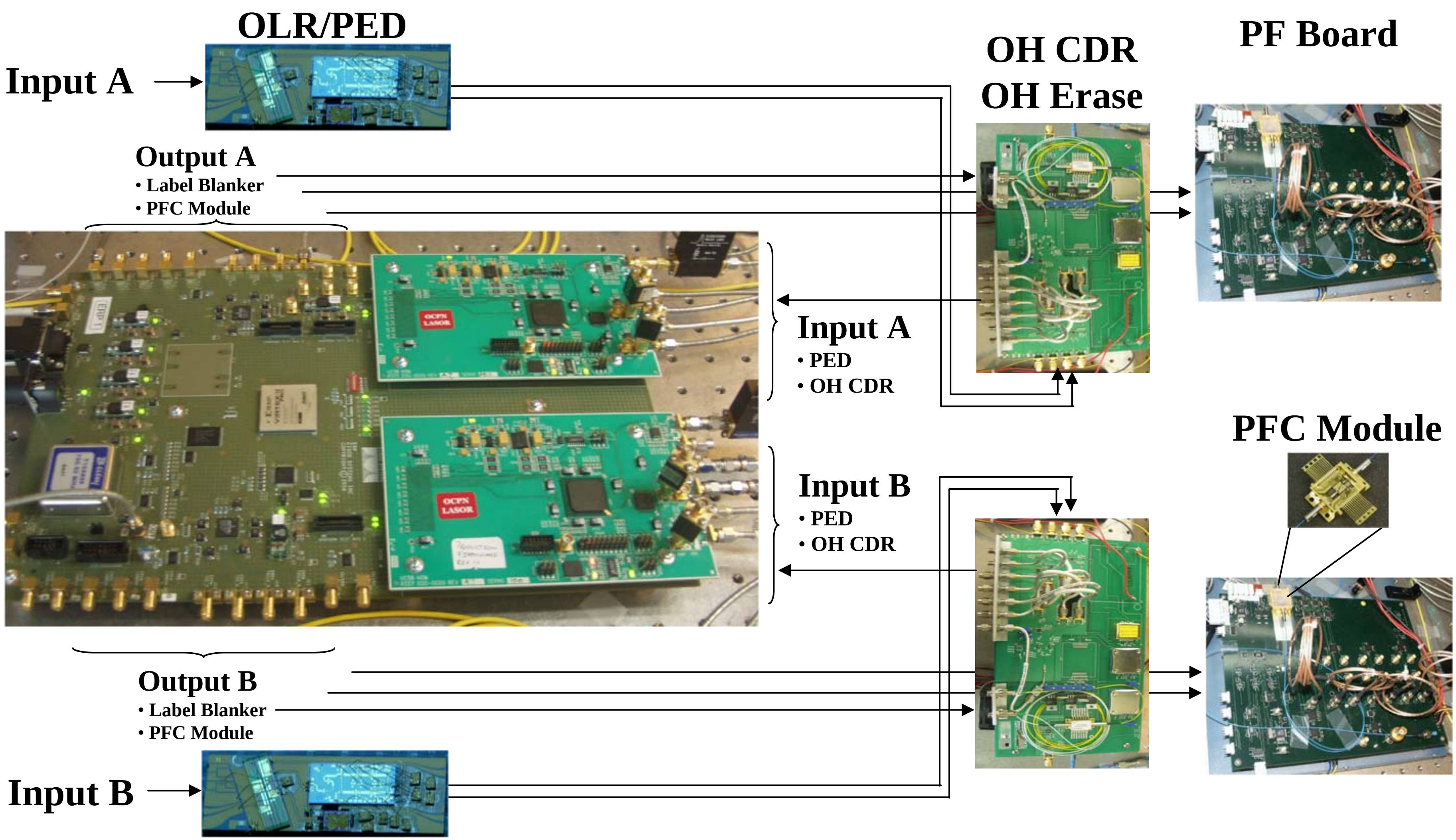
LASOR

System Demonstrations

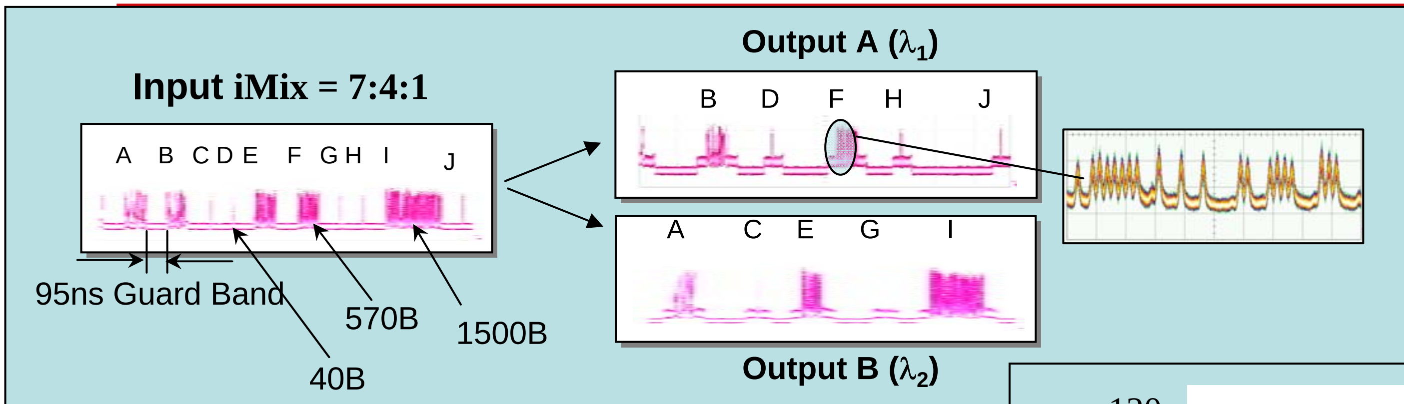
2x2 ODR Functional Diagram



Electronic Control



Layer-2/3 Results: Payload Throughput



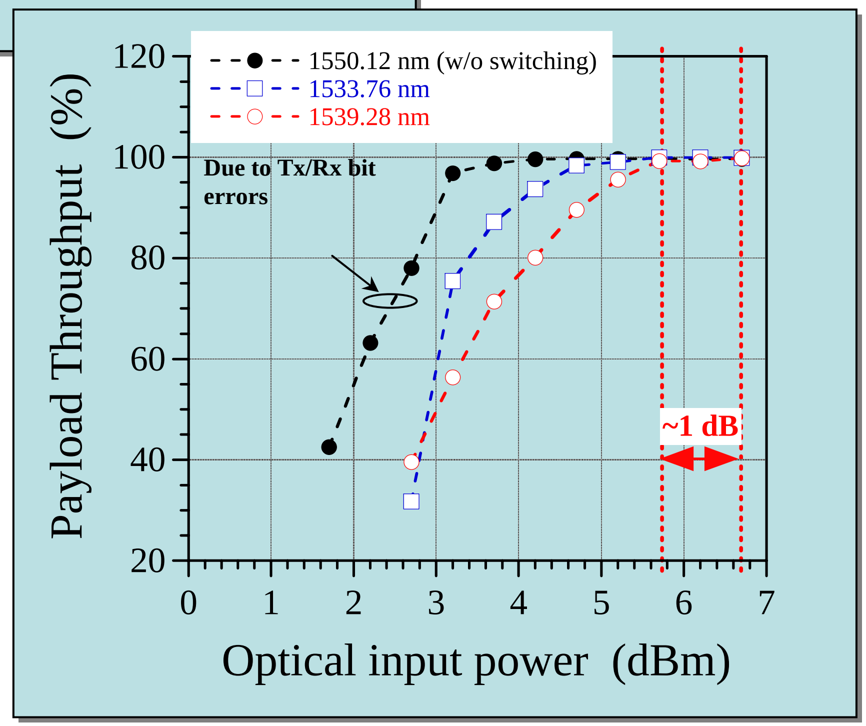
Stream#316 - Output of WC, switching, 30 runs (I), 1533.76nm.txt - Notepad

File Edit Format View Help

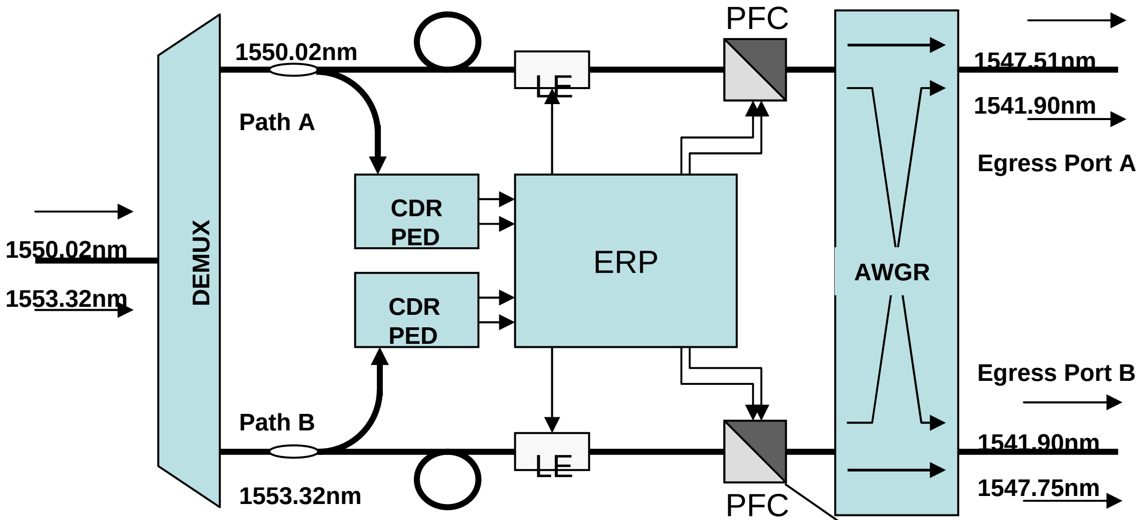
```
Data set used:         Stream#316
Stream points:         433152
Number of EA blocks:   10
Number of packets in data set:      60
Max packets that can be captured:  181

Optimum delay        0
Optimum threshold  -800
```

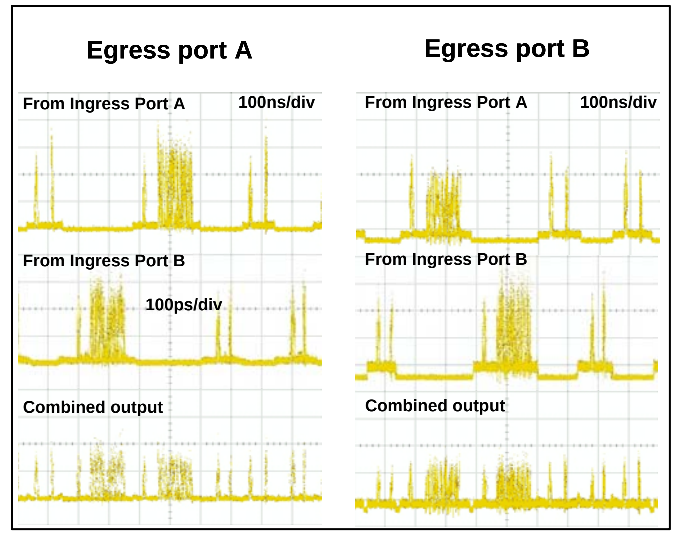
Run	OPI count	Payload ID	Seq. errors	Throughput
1	181		0	100.00 %
2	181		0	100.00 %
3	181		0	100.00 %
4	181		2	100.00 %
5	181		4	100.00 %
6	181		2	100.00 %
7	180		3	99.45 %
8	181		2	100.00 %
9	181		2	100.00 %
10	181		0	100.00 %
11	181		0	100.00 %
12	181		4	100.00 %
13	180		7	99.45 %
14	181		4	100.00 %
15	180		3	99.45 %
16	181		4	100.00 %
17	181		0	100.00 %
18	181		0	100.00 %
19	181		0	100.00 %
20	181		2	100.00 %
21	181		2	100.00 %
22	181		0	100.00 %
23	181		0	100.00 %
24	181		0	100.00 %
25	181		0	100.00 %
26	181		2	100.00 %
27	181		0	100.00 %
28	181		0	100.00 %
29	181		0	100.00 %
30	181		0	100.00 %

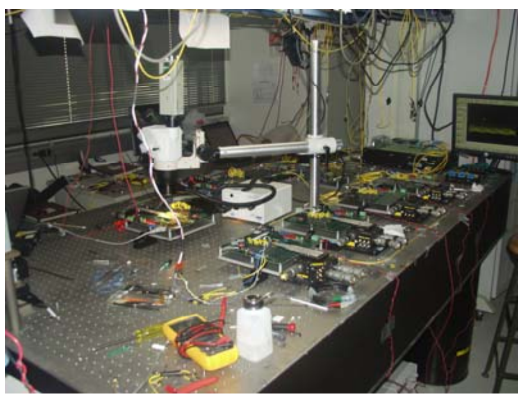
Average Throughput = 99.94 %

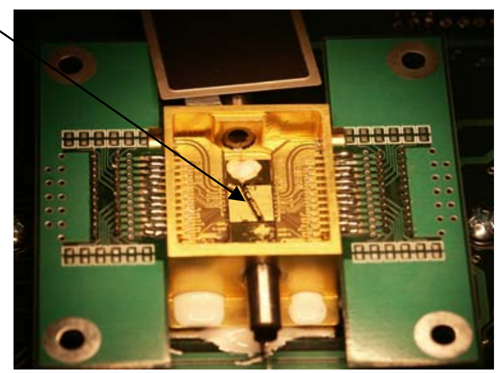


2x2 ODR Demonstration









H. Poulsen, W. Donat, V. Lal, M. Mashanovitch, G.Epps, D. Civello, C. Coldren, G. Fish, D. Blumenthal, "Demonstration of Simultaneous Multiplexing/Demultiplexing Operation of an All-Optical 2x2 Packet Switch with Asynchronous Variable-length Optically Labeled 40Gbps Packets," Accepted for presentation at ECOC 2006.

CSWDM and LASOR Building Blocks

- Monolithic dynamic wavelength converters
  - Regenerative, cascadable, input-output isolation
  - Two stage - internal wavelengths or wavebands
  - Internal wavelength optimized signal processing and memories
- Dynamic data (packet) storage cells
- Dynamic data (packet) synchronization cells
- Data envelope detectors
- All-optical clock and data recovery elements
- Switches and gain blocks
- Optical carrier filters
- Optical data filters

Future Directions

- Advance 2-stage wavelength converters with intermediate signal processing stages
- Ultra low-loss waveguides
- Phonon engineering for heat removal
- Integrated coherent wavelength converters
- Integration of FPGA electronics + digtial/analog + photonics
- All-optical FPGAs made with programmable optical cells
- New composite material systems that are engineered for optimum optical performance + thermal properties + integration with Si electronics