AIR FORCE OFFICE OF SCIENTIFIC RESEARCH

DTIC Data

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Research Title: "WAFER CLEANING AND PRE-BONDING MODULE FOR WAFER BONDING"

Type Submission: ~~New Work Effort~~ Final Report

Inst. Control Number: FA9550-05-1-0391DEF

Institution: THE REGENTS OF THE UNIVERSITY OF CALIFORNIA

Primary Investigator: Dr. Umesh Mishra

Invention Ind: none

Project/Task: 2305B / X

Program Manager: Dr. Gerald L. Witt

Objective:

This instrumentation grant stems from a DURIP 2005 proposal that was highly ranked but was not awarded due to limitation of funds. The semiconducting processing equipment hereby provided will add an important research capability to a team at UCSB that has numerous AFOSR and other DoD research projects.

Approach:

The equipment to be supported in for wafer clleaning and pre-bonding processing treatments. After the sample preparations provided by this equipment, experimental epitaxial layers will be bonded to suitable substrates. These substrates will provide electrical and other physical properties not available from same-type substrates.

Progress:

Year: 2007 **Month:** 12 **Final**

The EVG 810 system was delivered to UCSB and installed in the new Engineering Sciences cleanroom. The machine was inspected and checked out to insure that it met the designed specifications for bond strength. A number of silicon wafers were bonded with and without activation. As designed, the silicon wafers bonded with an energy of approximately 1.5 J/m2 when activated versus 0.4 J/m2 without activation. The bulk fracture strength of silicon is approximately 2.5 J/m2.

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14. ABSTRACT

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Wafer Cleaning and Pre-Bonding Module for Wafer Bonding

FA9550-05-1-0391

Final Performance Report

Summary

A DURIP grant was issued for the proeurement of a plasma aetivations system. The purpose of the system is to improve the quality of bond for direet semieonduetor wafer bonding by inereasing the bond strength while allowing a lower bonding temperature. An EV Group 810 system was acquired, and has improved the bonding proeess by allowing reduetions in temperature from 550°C to 350°C for III-Vs and allowed the bonding of silieon to gallium nitride.

Background

Many semieonduetor material systems are ineompatible with eaeh other. Some eannot be grown together through heteroepitaxy due to excessive lattiee mismatch, while for others, the proeess eonditions neeessary to produee deviees on one would destroy the other. Semieonduetor wafer bonding is one solution to both these issues. Bonding allows for the two material systems to be grown separately, then integrated post-growth and either pre- or post-proeessing. Where a lattiee mismateh would eause severe dislocations onee grown past the eritieal thiekness, bonded epilayers do not suffer this

problem; the threading dislocations do not propagate post-bond are replaced by misfits at the interface.

Bonded material systems allow for the 'perfect storm' of semiconductor devices: combining a very high-speed electron injector with a high-breakdrown collector. A bonded-FET design was proposed, combining a InGaAs/InAlAs FET for the device source and channel with a GaN drain.

A DURIP grant was issued for the procurement of a plasma activation system. By specially preparing and 'activating' the surface of the two materials to be joined, the bond strength can be increased without having to resort to higher bonding temperatures. An EV Group 810 system was ordered to fulfill the grant.

Results

The EVG 810 system was delivered to UCSB and installed in the new Engineering Sciences cleanroom. The machine was inspected and checked out to insure that it met the designed specifications for bond strength. A number of silicon wafers were bonded with and without activation. As designed, the silicon wafers bonded with an energy of approximately 1.5 J/m^2 when activated versus 0.4 J/m^2 without activation. The bulk fracture strength of silicon is approximately 2.5 J/m^2.

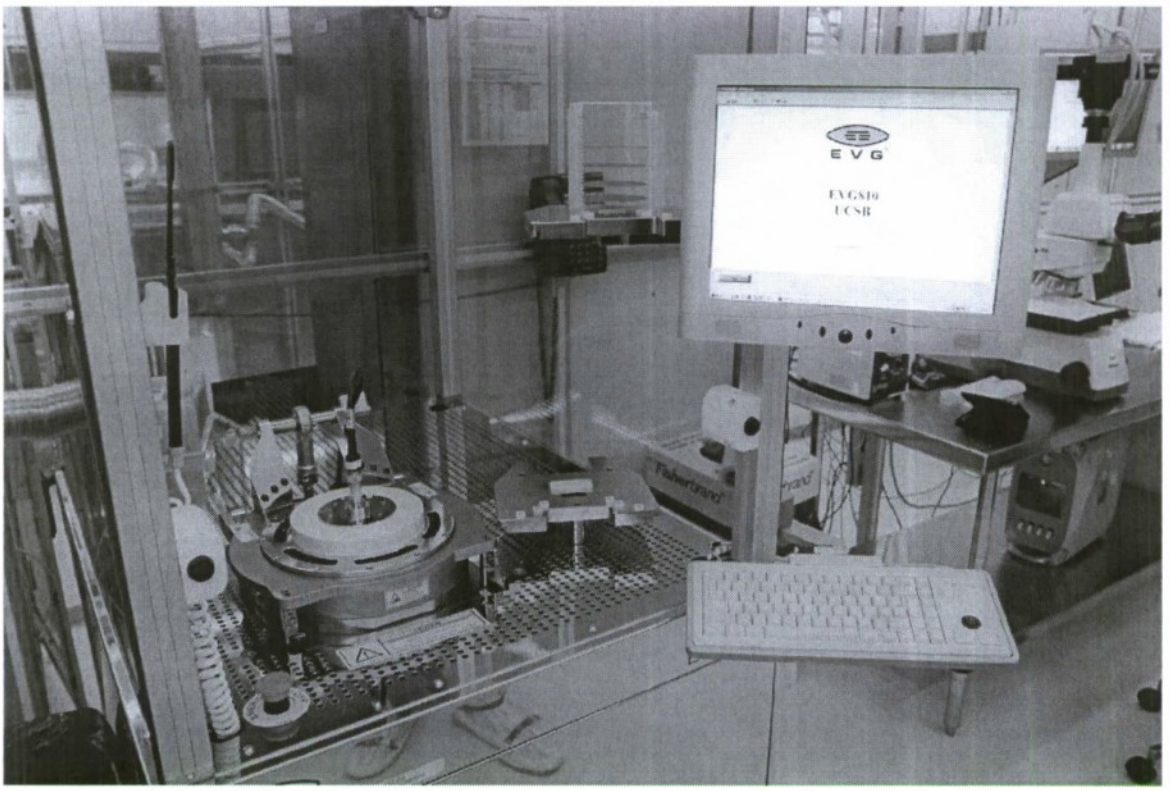


Figure 1 - The EVG 810 plasma activation system. Activation chamber is located on the left side, wit h Windows-based control computer adjacent. RF power supplies are located in the cabinet below.

When applied to the bonding of compound semiconductors, specifically III-arsenide to gallium nitride materials, the standard process emerged with a reduced bond temperature of 350-400°C, from a previous range of 550-700°C. This is particularly of importance in any indium based semiconductors, where the volatility of indium at high temperatures can affect the material parameters post-bond. Additionally, the EVG activation system has allowed the bonding of silicon to gallium nitride in similar temperature ranges, where it was unable to bond at all previously.

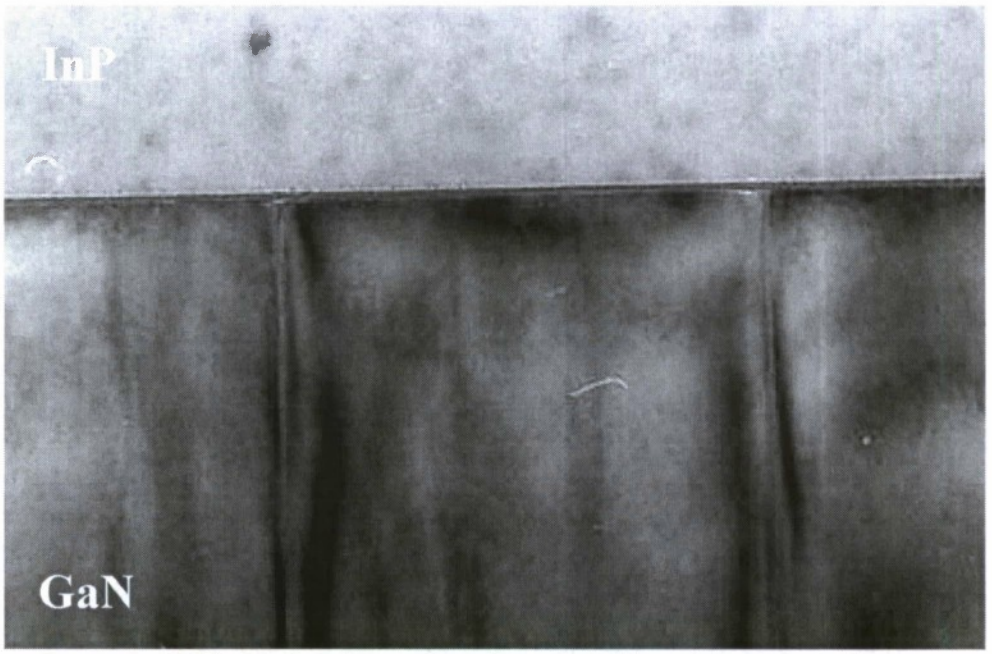


Figure 2 - TEM of InP-GaN interface. Note that dislocations in the GaN do not propagate into the bonded material on top.

The current bonding process, as developed at UCSB for the bonding of III-arsenides to gallium nitride, consists of the following major steps:

1. Cleaving and general preparation of samples.
2. Acetone and isopropanol solvent cleans to remove organics.
3. Megasonic water clean to remove particles.
4. O2 descum to remove last of organics.
5. HF dip to strip any native oxide.
6. EVG 810 plasma activation to treat surface prior to contact.
7. Contact and bonding.

Bonds of up to 1/4 of 2" wafers have been achieved, with nothing larger attempted due to prohibitive material cost and negligible return.

Initial devices have been produced using an InGaAs/InAlAs MESFET along with a GaN MESFET collector structure. Initial data shows the modulation of current in the InGaAs channel.

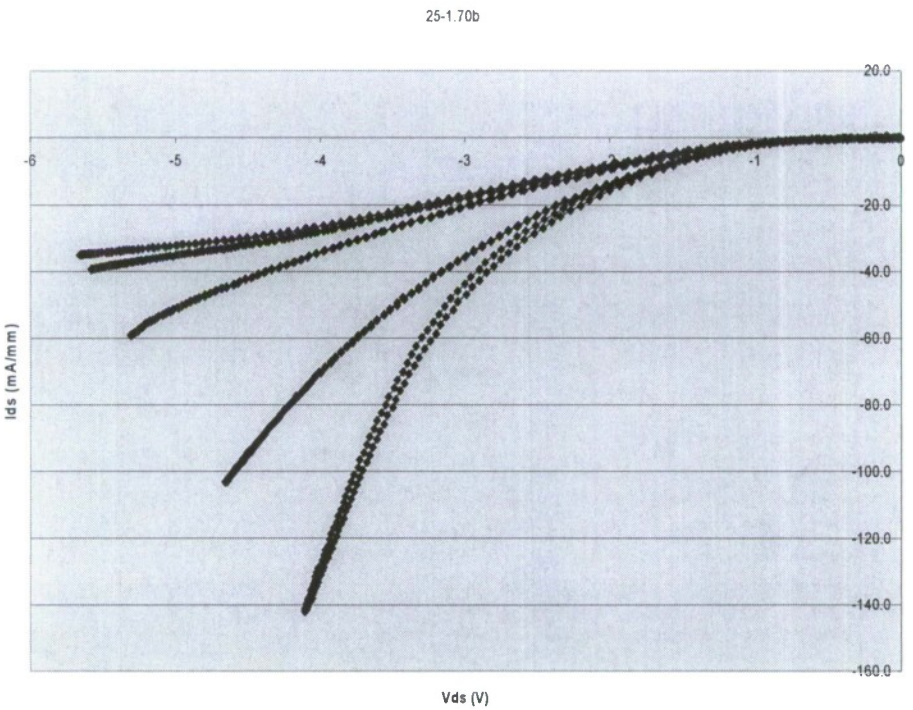


Figure 3 - DC Current in Bonded FET device.

Future work will improve injection from source to drain by better matching the conduction bands as well as improved process conditions in bonding.

Conclusion

As stated, the purchase and use of the EVG 810 plasma activation system has allowed for a simple plasma activation process, reduced the bonding temperature, and provided results in the form of bonds not achievable prior to its use. The gains from the use of the system will continue as the recipes used in the machine are developed and evolve to best suit the materials in use.

Wafer Bonding for Microwave and Power Electronics

FA9550-06-1-0089

Annual Performance Report

Summary

Several advances were made in the construction of bonded III-arsenide to gallium nitride devices. A mask-set containing several device experiments was designed and initial results for these devices were obtained. A first attempt at bonding silicon to GaN was made successfully.

Background

Many semiconductor material systems are incompatible with each other. Some cannot be grown together through heteroepitaxy due to excessive lattice mismatch, while for others, the process conditions necessary to produce devices on one would destroy the other. Semiconductor wafer bonding is one solution to both these issues. Bonding allows for the two material systems to be grown separately, then integrated post-growth and either pre- or post-processing. Where a lattice mismatch would cause severe dislocations once grown past the critical thickness, bonded epilayers do not suffer this problem; the threading dislocations do not propagate post-bond are replaced by misfits at

the interface. Bonded material systems allow for the 'perfect storm' of semiconductor devices: combining a very high-speed electron injector with a high-breakdrown collector.

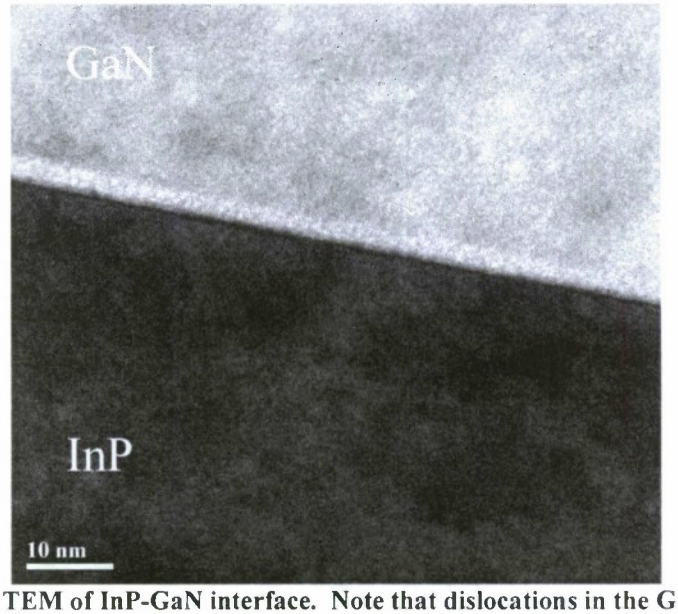


Figure 1 - TEM of InP-GaN interface. Note that dislocations in the GaN do not propagate into the bonded material on top.

A bonded-FET design was proposed, combining an InGaAs/InAlAs FET for the device source and channel with a GaN drain. We proposed a device design leveraging the benefits of the two materials in an attempt to produce a high speed, high power device. The device structure appears as follows (not to scale):

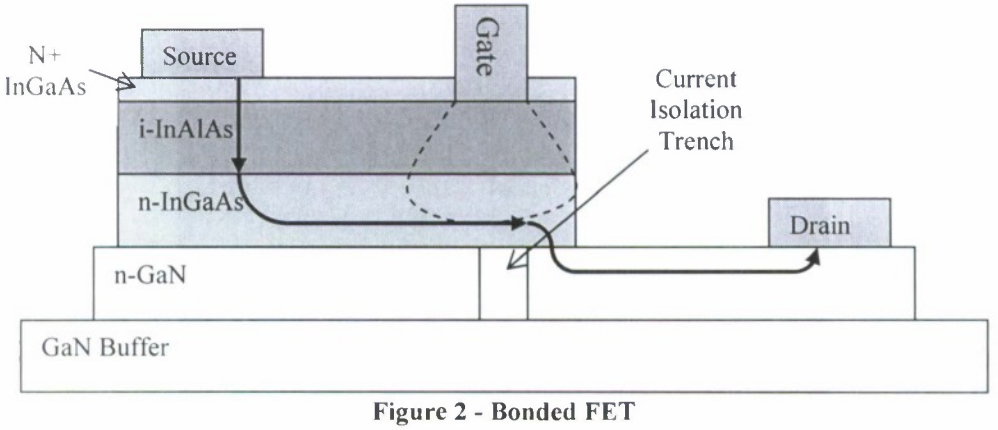


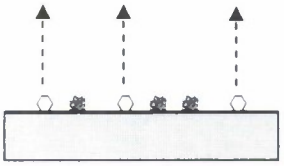
Figure 2 - Bonded FET

The current is injected from the source into the InGaAs, and forced through the gate-controlled area of the InGaAs by physically removing the current path from the GaN prior to bonding.

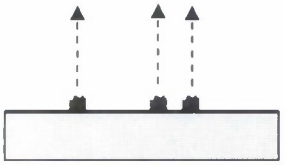
Results

A DURIP grant allowed the purchase of an EVG 810 plasma activation system, which helps prepare the bonding surface and improve bond strength. Consequently, the standard process emerged with a reduced bond temperature of 350-400°C, from a previous range of 550-700°C. This is particularly of importance in any indium based semiconductors, where the volatility of indium at high temperatures can affect the material parameters post-bond. Additionally, the EVG activation system has allowed the bonding of silicon to gallium nitride in similar temperature ranges, where it was unable to bond at all previously. The cleaning and bonding process now consists of the following steps:

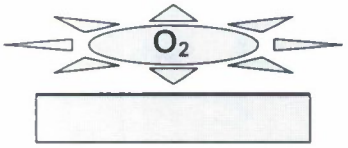
1. Organics Clean



2. Megasonic Clean

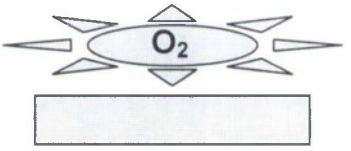


3. O2 Ash

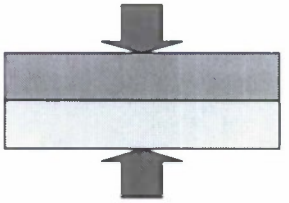


4. HF Dip

5. Plasma Activation



6. Joining & Bonding



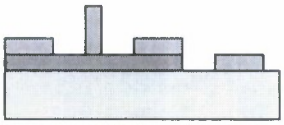
7. Substrate Removal	8. Device Processing
	

Table 1- Bonding Process Steps

A mask-set was designed to include numerous experiments to maximize the amount of data to be gathered from a given sample. The included devices and experiments in the mask are:

- 1, 2: Optical (0.7μ) gates and optical (0.5μ) trenches. Varied gate-edge to trench spacing and overlap.
- 3: Optical gates with E-beam trenches.
- 4: Ebeam gates with optical trenches.
- 5: Ebeam gates and trenches.
- 6: FatFETs and five TLMs. TLMs can be used to extract all contact resistances and bonded-interface resistances.
- 7: Hall pattern and Schottky diodes.
- 8: On-die RF calibration.
- 9: Optical alignment marks and verniers.

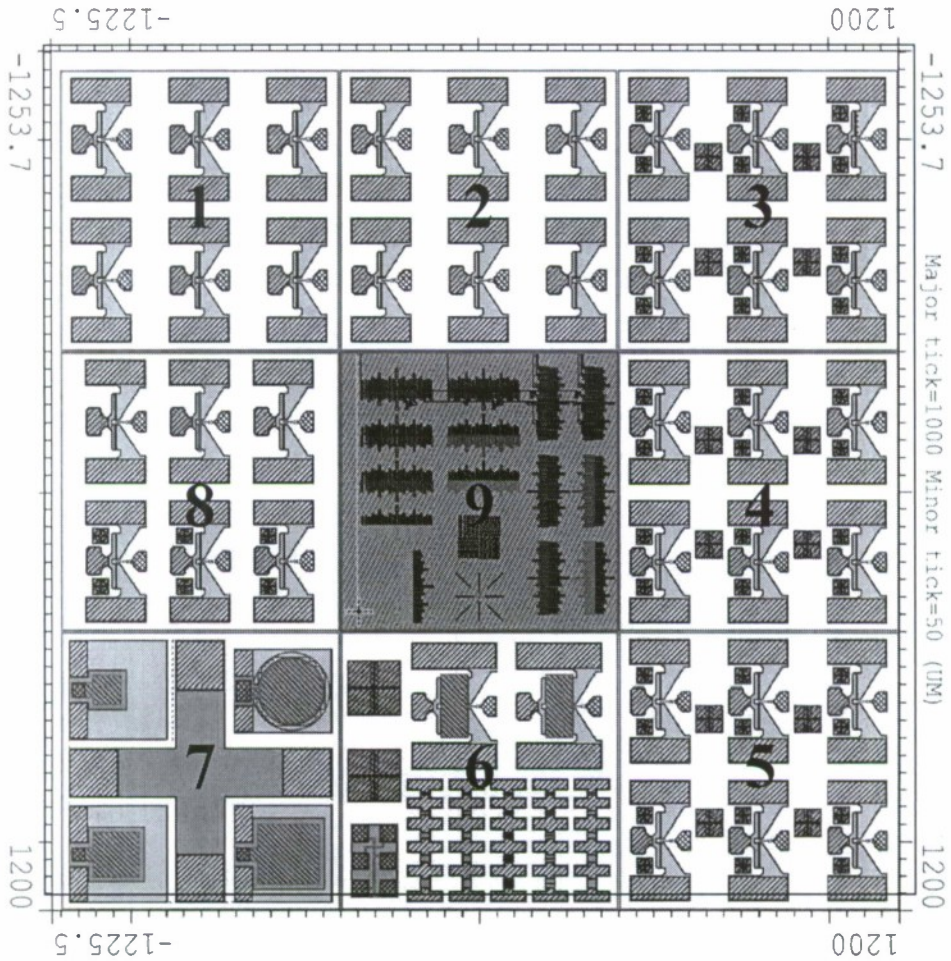
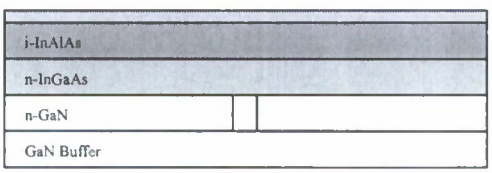


Figure 3 - Mask layout for Bonded FETs. 5 device experiments, TLMs & Fat FETs, Hall & Diodes, and on-die calibration.

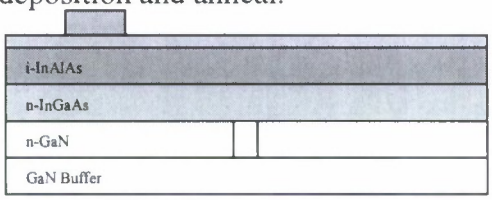
The process flow for the construction of the devices is as follows:

1. Etch current isolation channels and alignment marks into GaN.

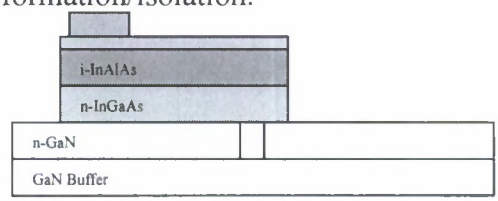
2. Bond materials and remove the substrate.



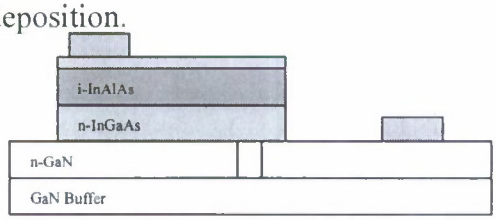
3. Source ohmic deposition and anneal.



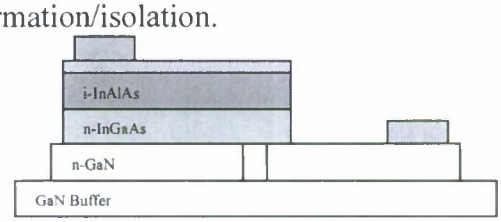
4. InGaAs mesa formation/isolation.



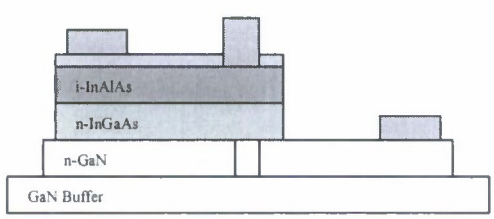
5. Drain ohmic deposition.



6. GaN mesa formation/isolation.



7. Gate deposition.



Initial devices have been produced using an InGaAs/InAlAs MESFET along with a GaN MESFET collector structure. Initial data shows the modulation of current in the InGaAs channel.

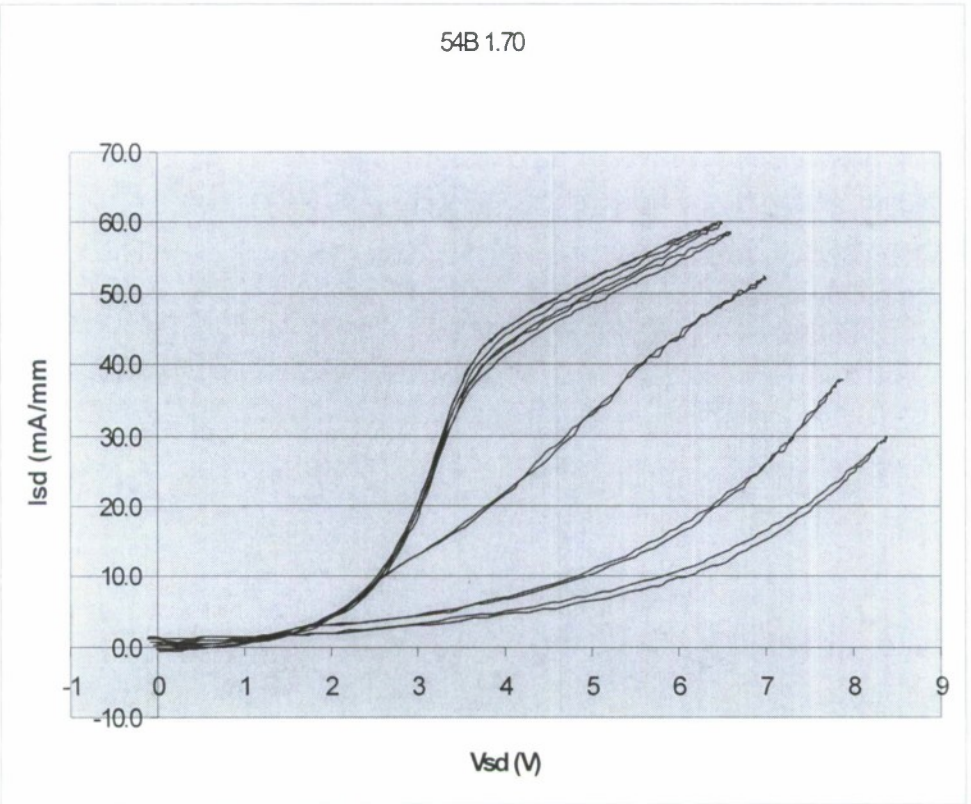


Figure 4 - DC Current in Bonded FET device.

Future work will improve injection from source to drain by better matching the conduction bands as well as improved process conditions in bonding.

Conclusion

Significant progress has been made in the realm of wafer bonding. The first devices for InGaAs/InAlAs-GaN bonding have been produced, and the initial Si-GaN bonding shows strong promise. The EVG 810 activation tool obtained with a DURIP grant has helped improve the bonding process.