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Time-Reversal Based Range Extension Technique for Ultra-wideband (UWB) Sensors and Applications in Tactical Communications and Networking

Technical Report (Quarterly)

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14. ABSTRACT

This technical report (quarterly) details the work for Office of Naval Research (ONR) by Tennessee Tech. The goal of this project—jointly funded by ONR, NSF, and ARO—is to build a general purpose testbed with time reversal capability at the transmitter side. The envisioned application is for UWB sensors and tactical communications in RF harsh environments where multipath is rich and can be exploited through the use of time reversal. In the past three months our focus has been on improving the transmitter baseband and making use of full functions of the D/A. Our next work items include improvement of the time acquisition to support transmission over longer distance. We are designing a new synchronization head, and will implement and test the function on the FPGA based platform. We will soon have a improved version of time reversal system over the air, and some field tests at extended range are expected in early 2009. For technology transfer, the evolution of this testbed toward a multi-GHz wideband cognitive radio is promising.

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Executive Summary

This technical report (quarterly) details the work for Office of Naval Research (ONR) by Tennessee Tech. The goal of this project—jointly funded by ONR, NSF, and ARO—is to build a general purpose testbed with time reversal capability at the transmitter side. The envisioned application is for UWB sensors and tactical communications in RF harsh environments where multipath is rich and can be exploited through the use of time reversal.

In the past three months our focus has been on improving the transmitter baseband and making use of full functions of the D/A.

Our next work items include improvement of the time acquisition to support transmission over longer distance. We are designing a new synchronization head, and will implement and test the function on the FPGA based platform.

We will soon have a improved version of time reversal system over the air, and some field tests at extended range are expected in early 2009.

For technology transfer, the evolution of this testbed toward a multi-GHz wideband cognitive radio is promising.

Contents

Part I

Test-bed

Chapter 1

Project Overview

This is the last report in the second year of the three-year projeet. The system demonstration was made in as early as May 2009. The current effort is to find out the praetieal limit for range extension by optimizing waveforms (sec Chaptcr 4) for lowcr data rate.

In the past thrce months our focus has been on improving the transmitter baseband and making use of full functions of thc D/A.

Our next work items includc improvemcnt of thc time acquisition to support transmission over longer distancc. Wc are designing a new synchronization head, and will implement and test the function on the FPGA based platform.

We will soon have a improved version of time reversal system over the air, and some field tests at extended rangc are cxpected in early 2009.

Sincc UWB waveform detection requires multi-GHz sampling rate, A/D converter (ADC) is the bottleneck for thc time rcversal system concept. For the current version, only energy dctection is used to avoid the multi-GHz ADC. Fortunately, a revolutionary technology called compressed sensing has just appeared. Chapter 5 investigates this problem.

Let us give an output for the last year—year 2009—of this project. The objective is twofold. First, we must demonstratc the system using a waveform that is optimal in the sense of range extension. Low date rate in the order of 10 $kbps$ is the range we will focus on.

Second, technology transfer should be pursued. In particular, the evolution of this testbed toward a multi-GHz wide-band cognitive radio is promising. The rational is as follows. Multi-GHz wideband spectrum sensing is inevitable for a convergence of three different technology areas: cognitive radio network, cognitive radar and cognitive anti-jamming systems. The state-of-the-art system has a bandwidth of 100 MHz. Our Lab, however, has demonstrated the system of more than 900 MHz. This initiative is being funded by NSF MRI (Major Research Instrument Initiative). This effort is especially significant to promote this convergence.

Chapter 2

Special Consideration for Burst Mode Communications

As part of effort to ensure a simple receiver structure, burst mode transmission has been adopted in the test-bed. There is not an always-connected link between the transmitter and receiver. A link is established between them only when a burst of data with control preamble is transmitted. Challenges in burst mode communications are obvious: automatic gain control (AGC) and synchronization have to be achieved in a very short time without having prior knowledge about the received signal level and timing. In addition, multipath effect and frequency selective fading make link establishment more difficult.

2.1 AGC and Thresholding

AGC is a common function in communication systems. An typical AGC circuit is a feedback loop implemented in analog format or digital format (actually mixed analog-digital format). The AGC performance can be characterized by dynamic range, response time and tracking accuracy. Note that the response time and the tracking accuracy are two conflicting parameters due to the behavior of the feedback loop and the nature of signal strength measurement. Digital AGC is getting popular thanks to fast evolution of semiconductor technology following the Moore's law, and double-loop AGC is usually used for better performance. One of the key element in AGC is a variable-gain amplifier (VGA). Major parameters of a VGA include dynamic range and bandwidth. Most VGAs on the market have very limited bandwidths and are not suitable for UWB applications. A typical technique to achieve a wide-band VGA with large dynamic range is to combine a large-range variable attenuator and a wide-band amplifier. This solution has been consided for future test-bed development.

To study the behavior of digital AGC, a Matlab/Simulink based simulation has been conducted. Shown here is the simulated system configuration including major elements VGA, peak detector, control logic and algorithm (not shown). The key parameters are as follows: 5-bit ADC, 64-level VGA with 1-dB step, and update rate 1/800 GHz = 1.25 MHz. This system setting leads to a fast response to a signal strength jump–a response delay of one update period at 10-dB SNR.

There are some other issue associated with AGC, such as the impact of the ADC's soft limits (ceiling and floor) on the AGC performance and thus on the overall system performance. Compensation for the ADC's soft limits may

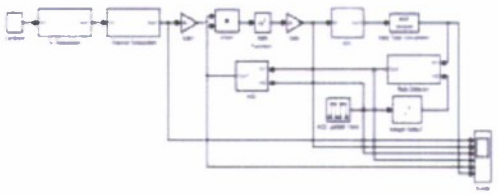

Figure 2.1: AGC simulation configuration

need to be considered in designing the AGC algorithm.

2.2 Fast Time Acquisition

A three-stage bust mode acquisition technique has been design and implemented in the test-bed. These stages include detection of frame-of-arrival, chip synchronization and frame synchronization. In addition to synchronization function, signal strength can be estimated in the first stage, so that proper thresholds can be set for making hard decision. After obtaining chip timing in the chip synchronization and producing hard decision, the received binary sequence is used in the frame synchronization stage, which contributes very little to hardware complexity.

The overall synchronization performance, represented by receiver operation characteristic (ROC), is significantly affected by the first stage. For a simple threshold-based frame-of-arrival detection, the ROC is sensitive to the initial threshold. Unfortunately, at the beginning of the synchronization procedure the AGC has not been ready and no threshold adjustment can be made, thus the preselected threshold has to be used, even though it may not be appropriate.

Our next work items will include improving the frame-of-arrival detection by reducing its sensitivity to the signal strength and noise level. By reducing this sensitivity, the impact of AGC on the synchronization ROC also decreases. Possible solutions can be sequential detection or quickest detection. The challenges would be in deriving a likelihood metric for unknown channel impulse response, and implementing the algorithm at acceptable complexity level.

Chapter 3

Implementation

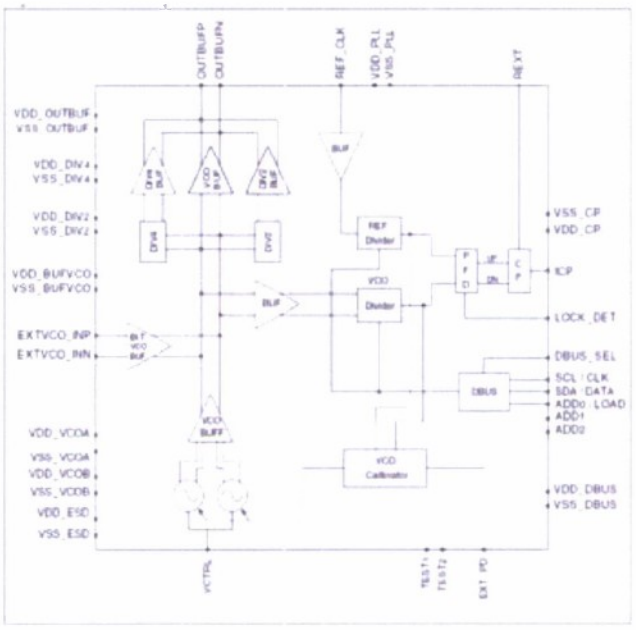

Figure 3.1: Block diagram of STW81101 RF synthesizer with VCOs.

3.1 Local Oscillator Evaluation Board STW81101-EVB4G by STMicroelectronics

In wideband systems such as the UWB cognitive radio system, proper LO signal generation is the most challenging issue in RF front-end because it must cover a wide frequency range and consume very little power in doing it, as well as switch its frequency at a very fast speed.

After carefully selection, we finally choose STMicroelectronics STW81101 as our next local oscillator,which enables the fast switch of the center frequency for the test-bed transmission.

The STMicroelectronics STW81101 is an integrated RF synthesizer with voltage controlled oscillators (VCOs). Showing high performance,high integration, low power, and multi-band performances, STW81101 is a low-cost one-chip alternative to discrete PLL and VCO solutions. The STW81101 includes an integer-N frequency synthesizer and two fully integrated VCOs featuring low phase-noise performance and a noise floor of -155 dBc/Hz. The combination of wide frequency range VCOs (using centerfrequency calibration over 32 sub-bands) and multiple output options (direct output, divided by 2, or divided by 4) allows coverage of the 825 MHz-1100 MHz, 1650 MHz-2200 MHz and 3300 MHz-4400 MHz bands.

The STW81101 is designed with STMicroelectronics advanced 0.35 m SiGe process.

Figure 3.1 shows the separate blocks that, when integrated, form an Integer-N PLL frequency synthesizer. The STW81101 consists of two internal low-noise VCOs with buffer blocks, a divider by 2, a divider by 4, a low-noise PFD (phase frequency detector), a precise charge pump, a 10-bit programmable reference divider, two programmable counters and a programmable dual modulus prescaler. The 5-bit A-counter and 12-bit B-counter, in conjunction with the dual modulus prescaler P/P+1 (16/17 or 19/20), implement an N integer divider, where N = B*P +A. The division ratio of both reference and VCO dividers is controlled through the selected digital interface (I2C bus or SPI), Beside, we can control the device by FPGA using I2C or SPI protocol.

The STW81101 features three different alternately selectable bands: direct output (3.3 to 4.4 GHz), divided by 2 (1.65 to 2.2 GHz) and divided by 4 (850 to 1100 MHz). Three evaluation boards are available depending on the output matching network optimal frequency range:(1) EVB1G (single output - 1 GHz - output divider by 4).(2) EVB2G (single output - 2 GHz - output divider by 2). (3) EVB4G (single output - 4 GHz - direct output). The board photo of EVB4G for STW81101 is shown as Figure 3.2. The direct output PFD frequency spurs is shown as Figure 3.3.

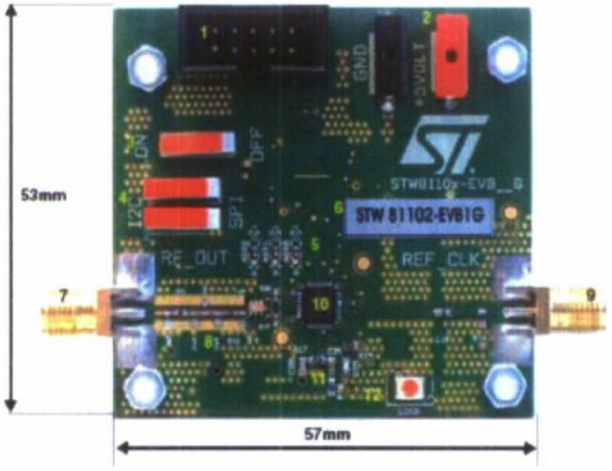

Figure 3.2: STW81101-EVB4G

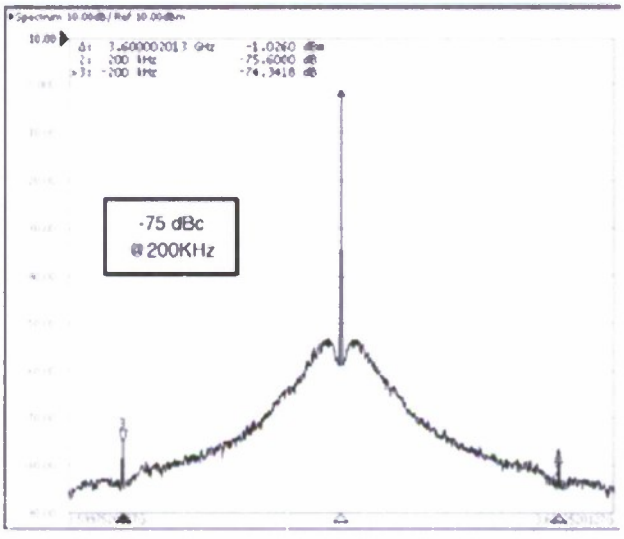

Figure 3.3: STW81101 direct output PFD frequency spurs.

To achieve a suitable power level, a good matching network is necessary to adapt the output stage to a 50 Ω load. Moreover, since most commercial RF components have single-ended input and output terminations, a differential to single-ended conversion may be required. A topology that permits the board a broadband matching as well as balanced to unbalanced conversion, is shown in Figure 3.4. For differential to single conversion, the 50 to 100 Ω

Johanson balun is recommended

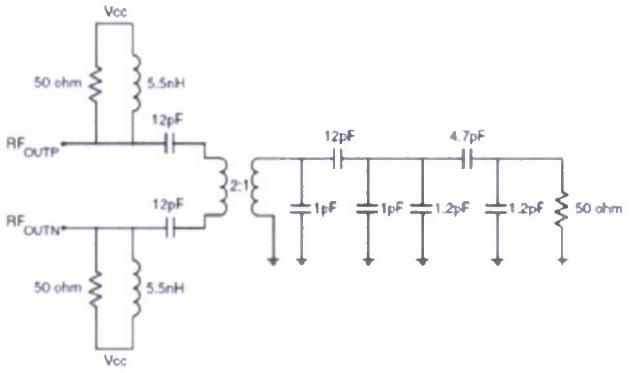

Figure 3.4: Evaluation board (EVB4G) matching network.

The selection of the digital interface type is done by the proper hardware connection of the pin DBUS_SEL (0 V for I2C bus, 3.3 V for SPI). All devices operate with a power supply of 3.3 V and can be powered down when not in use.

For I2C configuration, Data is transmitted from microprocessor to the STW81101 through the 2-wire (SDA and SCL) I2C bus interface. The STW81101 is always a slave device. The I2C bus protocol defines any device that sends data on the bus as a transmitter, and any device that reads the data as a receiver. The device controlling the data transfer is the master, and the others are slaves. The master always initiates the transfer and provides the serial clock for synchronization. Figure 3.5 shows the waveform data that was transmitted to STW81101 IC.

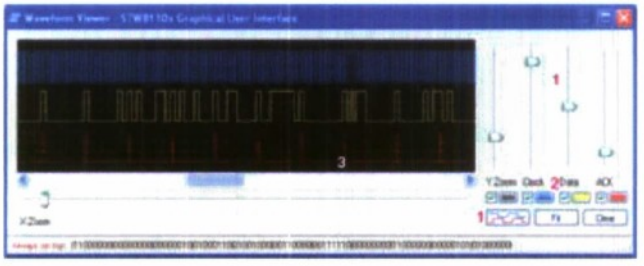

Figure 3.5: waveform view of the data be transmitted to the STW81101 IC.

The STW81101 IC also can be programmed by means of a high-speed serial-to-parallel interface with write option only. The 3-wire bus can be clocked at a frequency as high as 100 MHz to allow fast programming of the registers containing the data for RF IC configuration. The chip is programmed through serial words with a full length of 26 bits. The first 2 MSBs represent the address of the registers, and the 24 LSBs represent the value of the registers. Each data bit is stored in the internal shift register on the rising edge of the CLOCK signal. The outputs of the selected register are sent to the device on the rising edge of the LOAD signal.

3.2 High Speed FPGA-DAC Interface

The sampling rate of our 2nd generation testbed reaches 500 Msps with 2-bit resolution. This is below the capability of the Fujitsu DAC, which supports 1 Gsps sampling rate with 14-bit resolution. As discussed in the previous report, this limited performance is due to the interface between FPGA evaluation board (EB) and DAC development kit (DK). Since the FPGA EB is not designed for high-speed connection, there are few synchronized pins when data rate is over 500 Mbps. To increase the sampling rate and resolution of the DAC, we found a new FPGA EB, ML550, which is designed for high-speed data transmission. Here we will introduce ML550 and the connection between it and DAC DK.

3.2.1 Virtex-5 ML550 Networking Interfaces Platform

The ML550 Networking Interfaces Platform has an XC5VLX50T-FFG1136 FPGA on chip. The key features are:

- 64M x 8 DDR SDRAM memory
- Eight clock sources: - 200 MHz, 250 MHz, 133 MHz, and 33 MHz on-board oscillators - Two ICS8442 clock synthesizer devices
- One USB "B" port
- One 64 x 128 pixel LCD
- A System ACE CompactFlash (CF) Configuration Controller that allows storing Six Samtec LVDS connectors (a total of 53 differential input and 53 differential output
- Onboard power regulators with 5% output margin test capabilities, in 2.5% Power monitor connector for detailed current measurements on Vccint, Vccaux, and Vcco supplies

The clock and interfacing components on ML550 are very powerful. The differential SMA clock inputs are connected to the global clock inputs of the FPGA. An onboard 200-MHz oscillator calibrates the I/O delay, and an onboard 250-MHz oscillator is provided for general use. The two ICS8442 clock synthesizer devices output differential LVDS clocks in the 31.25 MHz to 700 MHz range, which can drive LVDS data rate up to 1.4 Gbps. The ML550 provides 53 pairs of transmit signals and 53 pairs of receive LVDS signals. These signals are distributed across three Samtec QSE-DP connectors for transmitting and another three connectors for receiving. The number of LVDS output and the speed of the LVDS data rate can maximize the DAC's capability to dual channel 14-bit 1 Gsps output.

Fujitsu and Xilinx developed an application to drive the DAC DK with ML550. An interface adapter is built by Fujitsu (Fig. 3.6). This adapter can be directly plugged onto the DAC DK 0.1" pitch header. Two SAMTEC EQCD high-speed ribbon cables are used to connect the adapter and ML550. The complete interface setup is illustrated in Fig. 3.7. The ribbon cable supports data rate up to 2.84 Gbps.

Fujitsu and Xilinx provided an application note to verify this setup with MB86065. An experiment was tested to show that this setup can drive single-port 14-bit 1.3 Gsps data into DAC. In our application however, we need to verify its ability to drive dual-port 14-bit 1 Gsps data. Now the ML550 board is available but the ribbon cables are still on the way. We will test this setup when the cables arrive.

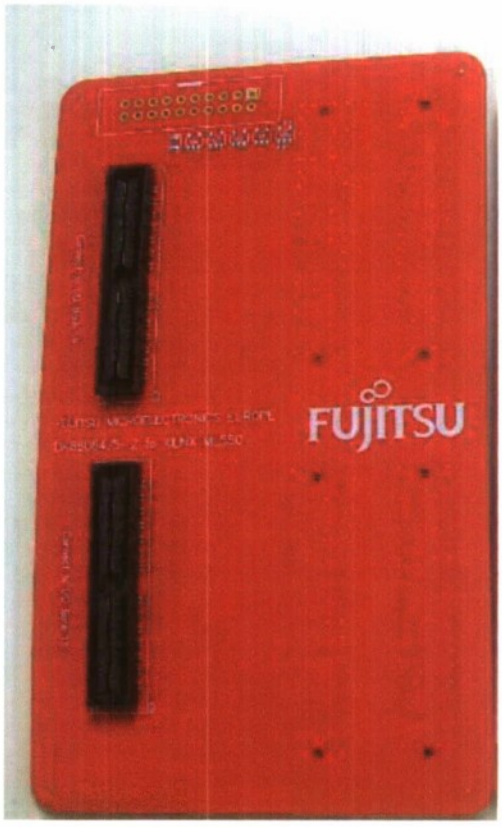

Figure 3.6: Passive interface adapter

Figure 3.7: Interface setup connecting ML550 and Fujitsu DAC DK

Chapter 4

Waveform-level Precoding with Simple Energy Detector Receiver for Wideband Communication

4.1 Introduction

Recent advances in miniaturization, low-power electronics and wireless communications, stimulated by increasing demands for automation in home and industrial areas, have triggered tremendous interests in the wireless sensor network (WSN) research, development and deployment. Designing WSNs is a big challenge due to tough constraints and conditions posed by specific applications and environments. Examples of these constraints and conditions include power consumption, node simplicity, node cost, low signal leakage and non-line-of-sight propagation, severe multipath, etc.

Mainly due to potentially low implementation complexity, suboptimal reception strategies, such as transmitted reference (TR) [1–8] and its variants [9–13] as well as energy (or square law) detector [14–17], have received increasing attention for complexity and cost constrained wideband applications. These suboptimal schemes are of low-complexity in the sense that no channel estimation is required and they are less sensitive to timing error. Of course, their performances are poor comparing to those of the optimal receivers.

One philosophy to use simple receivers without sacrificing overall performance is to shift part of receiver side functions to the transmitter side, i.e., add preprocessing at the transmitter to compensate performance loss, which is meaningful for a centralized network where one powerful central station communicates with a large number of nodes. In particular, high-bandwidth waveform level precoding is feasible as giga-Hertz sampling rate becomes practical. Real-time arbitrary waveform precoding provides a new platform for ultimate performance optimization using channel information. Depending upon the channel information, each pair of transmitter and receiver in the system chooses a transmitted waveform that is optimal in some sense. An example of waveform precoding is time reversal pre-filtering at the transmitter to focus the signal in time at the receiver [18–25], where the transmitted waveform is simply a time-reversed version of the channel impulse response (CIR). In such a system the receivers can be very simple, because they do not need special means (like a RAKE combiner) to capture dispersed energy over time, and even equalizers may not be necessary.

Waveform precoding can take into account both receive signal-to-noise ratio (SNR) and inter-symbol-interference (ISI). A common shortcoming is that the mentioned simple receivers are not able to work with typical linear equalization techniques, thus they are not suitable for applications when ISI exists apparently. Unlike linear receiver, the equivalent discrete channels of some suboptimal schemes behave nonlinearly, where an equivalent discrete-time channel has data input at one end and it outputs decision statistic plus noise at the other end [17, 25–27]. The decision statistic contains a desired signal and a nonlinear ISI component that cannot be well handled by normal linear equalization techniques. This fact suggests the use of some waveform-level channel shortening techniques.

In addition, in a rich multipath environment waveform precoding combined with multiple transmitter antennas can focus signal into a spot spatially. This spatial focusing feature can enable spatial division multiple access (SDMA) or enhance physical-layer security without consuming additional radio resources [22, 28, 29].

In this paper, a radio system combining waveform precoding and simple energy detector receiver is considered. Both on-off keying (OOK) and pulse position modulation (PPM) can be adopted as modulation schemes. The receiver uses an integrator to accumulate signal energy. For better performance the signal can be weighted prior to integration and there must be a best weighting function depending on the signal waveform and the noise level [30–34]. In fact, implementation of weighting function is not of low complexity and this contradicts the philosophy of low-complexity receiver design. A relatively simpler weighting method is a gating function which is equivalent to the use of a proper integration interval [17, 25, 35, 36]. A practical implementation of a smart integrator is to control the integrator's on-duration. Denoted by R_b the symbol rate and consider a received symbol waveform with most of the energy

concentrated in an interval T_I. If $T_I < T_b = 1/R_b$, then integrating over the interval T_I outperforms integrating over the interval T_b, since both gather almost the same amount of signal energy but the latter gathers more noise.

This paper tries to answer a fundamental question: given the transmission bandwidth and CIR, what are the best transmitted waveform and the best integration window size? Unlike performance evaluation of a linear receiver, analyzing an energy detector receiver is relative difficult. Park's model is adopted as an approximate analytical tool to formulate the equivalent SNR. Waveform optimization can be conducted based on this equivalent SNR. However, for arbitrary CIR to find a continuous time closed-form optimal solution is not feasible. Instead, a numerical approach using matrix operation is adopted. This work is to be tested on a real-time wideband radio test-bed. To obtain meaningful and convincing results, measured channel data is used to process numerical results.

The rest of the paper is organized as follows. The system is described in Section II. Theoretical analysis is presented in Section III. In Section IV, channel sounding are discussed. Numerical results are provided in Section V, followed by some remarks given in Section VI.

4.2 System Description

We limit our discussion to a single-user scenario. Assume the channel remains static during a data burst (say $100\mu s$ [8]) and CIR is available at the transmitter. How CIR is obtained is not a task of this paper. An ideal low-pass filter with one-sided bandwidth W is placed at the receiver's front-end.

The transmitted signal with OOK modulation is

$$s(t) = \sum_{j=-\infty}^{\infty} d_j p(t - jT_b), \tag{4.1}$$

where T_b is the symbol duration, $p(t)$ is the transmitted symbol waveform defined over $[0, T_p]$, and $d_j \in \{0, 1\}$ is j-th transmitted bit. Without loss of generality, assume the minimal propagation delay is equal to zero. The energy of $p(t)$ is normalized and defined as E_b,

$$\int_0^{T_p} p^2(t)\, dt = 1 \tag{4.2}$$

The received noise-polluted signal at the output of the receiver front-end filter is

$$\begin{aligned} r(t) &= h(t) \otimes s(t) + n(t) \\ &= \sum_{j=-\infty}^{\infty} d_j x(t - jT_b) + n(t), \end{aligned} \tag{4.3}$$

where $h(t), t \in [0, T_h]$ is the multipath impulse response that takes into account the effect of the RF front-end including the transceiver antennas. "$\otimes$" denotes convolution operation. $n(t)$ is a low-pass additive zero-mean Gaussian noise with one-sided bandwidth W and one-sided power spectral density N_0, and $x(t)$ is the received noiseless symbol-"1" waveform defined as

$$x(t) = h(t) \otimes p(t). \tag{4.4}$$

We further assume that $T_b \geq T_h + T_p \stackrel{\text{def}}{=} T_x$, i.e. no existence of ISI.

Figure 4.1: Energy-detector recciver.

An cnergy detector receiver performs squaring operation, integration over a given time window T_I, and threshold decision. Corresponding to the time index k, the k-th decision variable at the output of the integrator is given by

$$z_k = \int_{kT_b+T_{I0}}^{kT_b+T_{I0}+T_I} r^2(t)dt \tag{4.5}$$

$$= \int_{kT_b+T_{I0}}^{kT_b+T_{I0}+T_I} (d_k x(t-kT_b)+n(t))^2 dt \tag{4.6}$$

whcre T_{I0} is the starting time of integration for each symbol and $0 \le T_{I0} < T_{I0}+T_I \le T_x \le T_b$.

4.3 Waveform Design

4.3.1 Equivalent SNR

Analyzing an energy detector receiver as shown in Figure 4.1 is not as easy as analyzing linear receiver. The decision statistic z_k can bc approximated as a chi-square or a non-central chi-square random variable, with $2TW$ degrees of freedom [37,38]. A number of approximating models have been proposed to evaluate the performancc of receiver operating characteristic (RCO) [39]. When $2TW$ is large, the chi-square or a non-central chi-square pdfs asymptotically become Gaussian by the central limit theorem. In this case, the required receive SNR and decision threshold can be determined, given the probability of false alarm P_f and the probability of detection P_d [39]. With thc notation used in this paper, the rcceived SNR before the square law is expressed as,

$$d_I = \frac{\int_{T_{I0}}^{T_{I0}+T_I} x^2(t)\,dt}{T_I W N_0} \tag{4.7}$$

The ROC formulas based on Gaussian approximation can be extended to handle arbitrary value of $2TW$ by introducing an empirical loss function $C(d_I)$ [40,41], with its general form

$$C(d_I) = \frac{b+d_I}{d_I}, \tag{4.8}$$

wherc a and b are constants. In the following formula, the loss function links the received SNR and an equivalent SNR which provides thc same dctection performance when applied to a coherent receiver,

$$\mathrm{SNR}_{\mathrm{eq}} = \frac{aT_I W d_I}{C(d_I)} \tag{4.9}$$

$$= \frac{aT_I W d_I^2}{b+d_I} \tag{4.10}$$

$$= \frac{2\left(\int_{T_{I0}}^{T_{I0}+T_I} x^2(t)\,dt\right)^2}{2.3T_I W N_0^2 + N_0 \int_{T_{I0}}^{T_{I0}+T_I} x^2(t)\,dt} \tag{4.11}$$

The equivalent SNR $\mathrm{SNR}_{\mathrm{eq}}$ is used as a performance indicator in this paper. The parameters a and b take 2 and 2.3, respectively, the same as Park's selection in [40].

4.3.2 Waveform Optimization

In order to get the better performance, the equivalent SNR $\mathrm{SNR}_{\mathrm{eq}}$ should be maximized. Define,

$$E_I = \int_{T_{I0}}^{T_{I0}+T_I} x^2(t)\,dt \tag{4.12}$$

For given T_I and W, $\mathrm{SNR}_{\mathrm{eq}}$ is the increasing function of E_I. So the maximization of $\mathrm{SNR}_{\mathrm{eq}}$ in Equation 4.9 is equvalent to the maximization of E_I in Equation 4.12.

So the optimization problem is shown below,

$$\begin{array}{l} \max \int_{T_{I0}}^{T_{I0}+T_I} x^2(t)\,dt \\ s.t. \int_0^{T_p} p^2(t)\,dt = 1 \end{array} \tag{4.13}$$

In order to solve the optimization problem 4.13, $p(t)$, $h(t)$ and $x(t)$ will be uniformly sampled and the count-part of the optimization problem 4.13 in the digital domain will be solved. Assume the sampling period is T_s. $T_p/T_s = N_p$, $T_h/T_s = N_h$ and $T_x/T_s = N_x$. So $N_x = N_p + N_h$.

$p(t)$, $h(t)$ and $x(t)$ are represented by $p_i, i = 0, 1, \ldots, N_p$, $h_i, i = 0, 1, \ldots, N_h$ and $x_i, i = 0, 1, \ldots, N_x$ respectively, where,

$$p_i = p(it_s) \tag{4.14}$$

$$h_i = h(it_s) \tag{4.15}$$

$$x_i = x(it_s) \tag{4.16}$$

So the count-part of Equation 4.4 in the digital domain is shown as,

$$x_i = p_i * h_i \tag{4.17}$$

$$= \sum_{j=0}^{N_p} p_j h_{i-j} \tag{4.18}$$

Define,

$$\mathbf{p} = [p_0\ p_1\ \cdots\ p_{N_p}]^T \tag{4.19}$$

and

$$\mathbf{x} = [x_0\ x_1\ \cdots\ x_{N_x}]^T \tag{4.20}$$

Construct channel matrix $\mathbf{H}_{(N_x+1)\times(N_p+1)}$,

$$(\mathbf{H})_{i,j} = \begin{cases} h_{i-j}, 0 \le i-j \le N_h \\ 0, \quad else \end{cases} \tag{4.21}$$

where $(\bullet)_{i,j}$ denotes the entry in the i-th row and j-th column of the matrix.

Thus the matrix expression of Equation 4.17 is,

$$\mathbf{x} = \mathbf{H}\mathbf{p} \tag{4.22}$$

and the constraint in the optimization problem 4.13 can be expressed as,

$$\|\mathbf{p}\|_2^2 T_s = 1 \tag{4.23}$$

where "$\|\bullet\|_2$" denotes the norm-2 of the vector.

Meanwhile assume $T_I/T_s = N_I$ and $T_{I0}/T_s = N_{I0}$, so the valid entries in $\mathbf{x}$ for integration constitute $\mathbf{x}_I$ as,

$$\mathbf{x}_I = [x_{N_{I0}}\ x_{N_{I0}+1}\ \cdots\ x_{N_{I0}+N_I}]^T \tag{4.24}$$

and E_I in Equation 4.12 can be equivalently shown as,

$$E_I = \|\mathbf{x}_I\|_2^2 T_s \tag{4.25}$$

Similar to Equation 4.22, $\mathbf{x}_I$ can be obtained by,

$$\mathbf{x}_I = \mathbf{H}_I\mathbf{p} \tag{4.26}$$

where $(\mathbf{H}_I)_{i,j} = (\mathbf{H})_{N_{I0}+i,j}$ and $i = 1, 2, \ldots, N_I + 1$ as well as $j = 1, 2, \ldots, N_p + 1$.

So the count-part of the optimization problem 4.13 in the digital domain can be expressed as,

$$\begin{array}{l} \max \|E_I\|_2^2 \\ s.t.\ \|\mathbf{p}\|_2^2 T_s = 1 \end{array} \tag{4.27}$$

This optimization problem can be solved by Lagrange Multiplier method. Define objective function as,

$$J = \|E_I\|_2^2 + \lambda\left(1 - \|\mathbf{p}\|_2^2 T_s\right) \tag{4.28}$$

$$= \|\mathbf{H}_I\mathbf{p}\|_2^2 T_s + \lambda\left(1 - \|\mathbf{p}\|_2^2 T_s\right) \tag{4.29}$$

where λ is Lagrange Multiplier. From $\frac{\partial J}{\partial \mathbf{p}} = 0$, it is obtained that,

$$\mathbf{H}_I^T\mathbf{H}_I\mathbf{p} = \lambda\mathbf{p} \tag{4.30}$$

So the optimal solution $\mathbf{p}^*$ is the eigen-vector corresponding to the maximum eigen-value in eigen-function 4.30 and $\mathbf{p}^*$ satisfies Equation 4.23. Furthermore, E_I^* will be obtained.

4.4 Channel Sounding

The time domain channel sounding is employed to get $h(t)$. This kind of channel sounding consists of a pulse generator, a signal generator, a low noise amplifier (LNA), a transmitter antenna and a receiver antenna, and a digital sampling oscilloscope (DSO). Figure 4.2 shows the setup of the time domain channel sounding. The signal

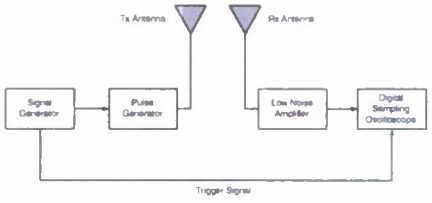

Figure 4.2: The setup of the time domain channel sounding.

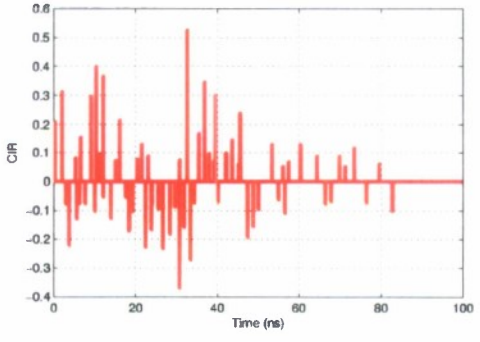

Figure 4.3: CIR.

generator, the pulse generator and the transmitter antenna constitute the transmitter part and DSO along with the receiver antenna and LNA constitutes the receiver part. The signal generator is used to trigger the pulse generator and the pulse generator generates the pulse that is transmitted through the channel. On the receiver side the signal is amplified by LNA and then displayed and recorded on DSO. A triggering signal from the signal generator is also used to synchronize DSO to record the data of the received signal. The tapped-delay-line model of CIR will be estimated using "CLEAN", a matching pursuit algorithm based on the recorded data from DSO and the noiseless waveform template of the transmitted pulse. Raised-cosine filter is used in this paper to emulate the RF front-end filter including the transceiver antennas, so $h(t)$ can be obtained by convolving CIR and the raised-cosine filter with bandwidth W.

4.5 Numerical Results

Figure 4.3 shows CIR under investigation in this paper and the energy of $h(t)$ is normalized. $W = 1GHz$. $T_s = 0.025ns$, $T_h = 100ns$, $T_p = 100ns$ and $T_{I0} + \frac{T_I}{2} = 100ns$. If the optimal waveform $\mathbf{p}^*$is transmitted, $E_I^*(T_I)$ and $\mathrm{SNR}_{\mathrm{eq}}^*(T_I)$ will be obtained. If the transmitted waveform is time reversed $h(t)$, $E_I^{\mathrm{TIR}}(T_I)$ and $\mathrm{SNR}_{\mathrm{eq}}^{\mathrm{TIR}}(T_I)$ will be obtained. Figure 4.4 shows $\mathrm{SNR}_{\mathrm{eq}}^*(T_I)$ and Figure 4.5 shows $\mathrm{SNR}_{\mathrm{eq}}^{\mathrm{TIR}}(T_I)$. For the relatively low E_b/N_0 region, the optimal T_I is less than $5ns$ seen from Figure 4.4 and Figure 4.5. Increasing T_I will introduce more noise and the performance will degrade. For the relatively high E_b/N_0 region, we can choose the proper T_I such that the larger T_I can not bring the obvious increase of $\mathrm{SNR}_{\mathrm{eq}}$.

Let's define two gains to quantify the performance of optimal waveform using time reversal as benchmark. One is an energy gain,

$$G_e(T_I) = \frac{E_I^*(T_I)}{E_I^{\mathrm{TIR}}(T_I)} \tag{4.31}$$

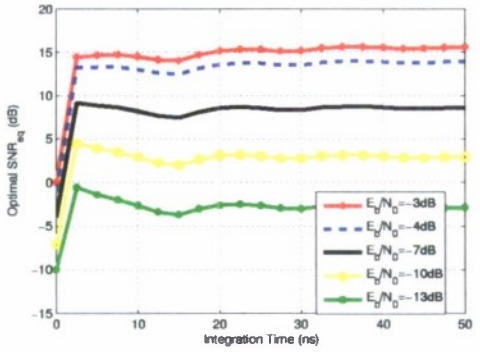

Figure 4.4: $\mathrm{SNR}_{\mathrm{eq}}^{*}(T_I)$.

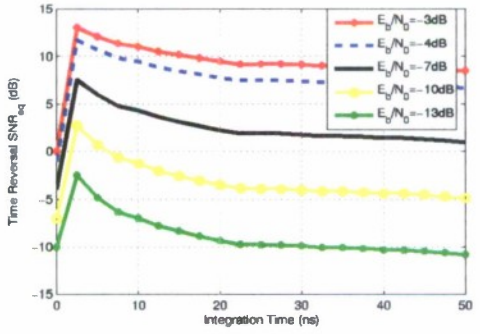

Figure 4.5: $\mathrm{SNR}_{\mathrm{eq}}^{\mathrm{TIR}}(T_I)$.

and the other is an $\mathrm{SNR}_{\mathrm{eq}}$ gain,

$$G_{\mathrm{SNR}_{\mathrm{eq}}}(T_I) = \frac{\mathrm{SNR}_{\mathrm{eq}}^{*}(T_I)}{\mathrm{SNR}_{\mathrm{eq}}^{\mathrm{TIR}}(T_I)} \tag{4.32}$$

Figure 4.6 and Figure 4.7 show the energy gain and $\mathrm{SNR}_{\mathrm{eq}}$ gain respectively. When $T_I \to 0$, the energy gain and the $\mathrm{SNR}_{\mathrm{eq}}$ gain approach 1. In this kind of situation, the optimal waveform is the time reversed $h(t)$. So, from peak detection's point of view, time reversal is the optimal waveform-level precoding. However, when T_I increases, the optimal waveform can bring obvious performance enhancement not only for the energy gain but also for the $\mathrm{SNR}_{\mathrm{eq}}$ gain.

Define,

$$T_I^{*} = \arg\max_{T_I} \mathrm{SNR}_{\mathrm{eq}}^{\mathrm{TIR}}(T_I) \tag{4.33}$$

If $\mathrm{SNR}_{\mathrm{eq}}^{\mathrm{TIR}}(T_I^{*})$ is used as the benchmark, then the other $\mathrm{SNR}_{\mathrm{eq}}$ gain is defined as,

$$G_{\mathrm{SNR}_{\mathrm{eq}}}^{*}(T_I) = \frac{\mathrm{SNR}_{\mathrm{eq}}^{*}(T_I)}{\mathrm{SNR}_{\mathrm{eq}}^{\mathrm{TIR}}(T_I^{*})} \tag{4.34}$$

Figure 4.8 shows $G_{\mathrm{SNR}_{\mathrm{eq}}}^{*}(T_I)$. In the relatively high E_b/N_0 region, the performance of optimal waveform can be improved by a few decibels over the time reversal scheme with optimal integration window when T_I for optimal waveform is larger than a certain threshold. While if E_b/N_0 is relatively low, the optimal T_I for optimal waveform is still needed to get the better performance.

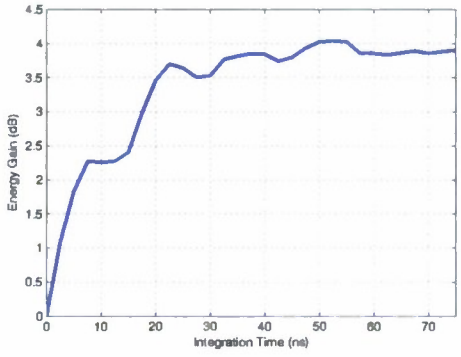

Figure 4.6: Energy gain.

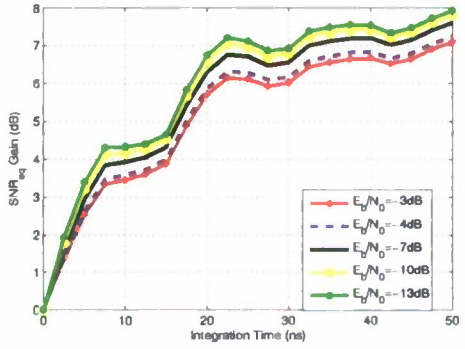

Figure 4.7: SNR_{eq} gain.

4.6 Conclusion

Wideband waveform-level precoding with energy detector receiver has been studied. This work is a part of our effort in searching for simple-receiver solutions with enhanced performance. Thanks to the empirical loss function, elegant analytical frame has been established, enabling derivation of closed-form optimization results. Numerical results show that performance can be improved by a few decibels over the time reversal scheme with optimal integration window, meaning that time reversal is not the best waveform-level precoding for energy detector receiver. This research suggests that waveform-level precoding can significantly extend the communication range without consuming extra transmitted power. The results of this paper will be verified on the real-time wideband radio test-bed.

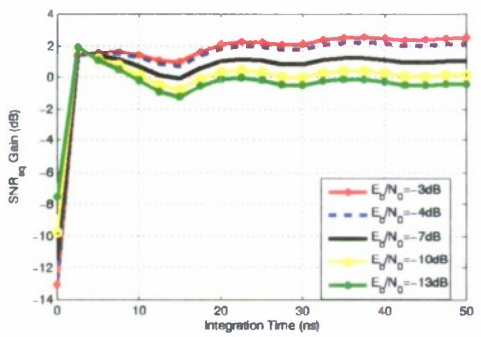

Figure 4.8: $\mathrm{SNR}_{\mathrm{eq}}$ gain using $\mathrm{SNR}_{\mathrm{eq}}^{\mathrm{TIR}}(T_I^*)$ as the benchmark.

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Chapter 5

A Compressed Sensing Based Ultra-Wideband Communication System

Sampling is the bottleneck for ultra-wideband (UWB) communication. Our major contribution is to exploit the channel itself as part of compressed sensing, through waveform-based pre-coding at the transmitter. We also have demonstrated a UWB system baseband bandwidth (5 GHz) that would, if with the conventional sampling technology, take decades for the industry to reach. The concept has been demonstrated, through simulations, using real-world measurements. Realistic channel estimation is also considered.

5.1 Introduction

Ultra-wideband (UWB) [1–4] represents a new paradigm in wireless communication. The unprecedented radio bandwidth provides advantages such as immunity from flat fading. Two primary challenges exist: (1) how to collect energy over the rich multipath components; (2) extremely high sampling rate analog to digital conversion (A/D). Time reversal [5] provides a promising solution to the first problem [6]. In particular, the concept of time reversal has recently demonstrated in a real-time hardware test-bed [7, 8]. At the heart of time reversal, the channel itself is exploited as a part of the transceiver. This idea makes sense since when few movements exist, the channel is time-invariant and reciprocal [9]. In principle, most of the processing at the receiver can be moved to the transmitter—where energy consumption and computation are sufficient for many advanced algorithms.

A natural question arises: Can we move the hardware complexity of the receiver to the transmitter side and reduce the sampling rate of A/D? We are motivated to use standard converters at the level of 125 Msps—for which excellent high dynamic range commercial solutions are available. Fortunately compressed sensing (CS) [10, 11] is a natural framework for our purpose.

CS has been used to UWB communications [12–16]. Our major contribution is to exploit the channel itself as part of compressed sensing, through waveform-based pre-coding at the transmitter. Only one low-rate A/D is used at the receiver. We also have demonstrated (Fig. 5.2) a UWB system covering the 3 GHz – 8 GHz frequency band that would, if with the conventional sampling technology, take decades for the industry to reach.

This paper is organized as follows. Section 5.2 introduces the CS theory background and extends CS concept to a

continuous time filter based architecture. Section 5.3 describes the proposed CS based UWB system together with a CS based channel estimation method. Section 5.4 shows the simulation results and section 5.5 gives the conclusions.

5.2 Compressed Sensing for Communications

5.2.1 Compressed sensing background

Reference [17] gives a most succinct highlight of the CS principles and will be followed here for a flavor of this elegant theory. Consider the problem of reconstructing an $N \times 1$ signal vector x. Suppose the basis $\Psi = [\psi_1, ..., \psi_N]$ provides a K-sparse representation of x, where $K << N$; that is

$$x = \sum_{n=0}^{N-1} \psi_n \theta_n = \sum_{l=1}^{K} \psi_{n_l} \theta_{n_l} \tag{5.1}$$

Here x is a linear combination of K vector chosen from Ψ; $\{n_l\}$ are the indices of those vectors; $\{\theta_{n_l}\}$ are the coefficients. Alternatively, we can write in matrix notation

$$x = \Psi\theta, \tag{5.2}$$

where $\theta = [\theta_0, \theta_1, ..., \theta_{N-1}]^T$. In CS, x can be reconstructed successfully from M measurements and $M << N$. The measurement vector y is done by projecting x over another basis Φ which is incoherent with Ψ, i.e. $y = \Phi\Psi\theta$. The reconstruction problem becomes an $l_1 - norm$ optimization problem:

$$\hat{\theta} = \arg\min ||\theta||_1 \quad s.t. \quad y = \Phi\Psi\theta. \tag{5.3}$$

This problem can be solved by linear programming techniques like basis pursuit (BP) or greedy algorithms such as matching pursuit (MP) and orthogonal matching pursuit (OMP).

When applying CS theory to communications, the sampling rate can be reduced to sub-Nyquist rate. In [18] and [15] a serial and a parallel system structure were proposed, respectively. Sampling rate can be reduced to less than 20% of Nyquist rate. However, they were designed for signals that are sparse in frequency domain. In this paper we propose a serial system structure which is suitable for pulse-based UWB communications, which is sparse in time domain. The analog-to-information converter (AIC) structure in [18] is not suitable for UWB communications. 3 – 8 GHz UWB signal is considered as an example in describing the reasons:

- The pseudo noise (PN) chip rate requirement for PN sequence makes it difficult for UWB signals, which must be at least twice the maximum signal frequency. For example, a 3 – 8 GHz UWB signal needs at least 16 GHz chip rate.
- The multiplier, which can be a mixer, supporting such high bandwidth for 3 – 8 GHz UWB signal is difficult to implement.
- The system is time-variant. Each measurement is the product of a streaming signal and a changing PN sequence. This requires a huge amount of storage space and complex computation.

In this paper, a simple architecture that is suitable for UWB signals is proposed using a finite impulse response (FIR) filter-based architecture.

5.2.2 Filter-based compressed sensing

Random filter based CS system for discrete time signals was proposed in [19]. This idea can be extended to continuous time signals. We use $*$ to denote the convolution process in a linear time-invariant (LTI) system. Assume that there is an analog signal $x(t), t \in [0, T_x']$ which is K-sparse over some basis Ψ:

$$x(t) = \sum_{n=0}^{N-1} \Psi_n(t)\,\theta_n = \Psi(t)\,\theta, \tag{5.4}$$

where

$$\Psi(t) = [\Psi_0(t), \Psi_1(t), ..., \Psi_{N-1}(t)], \tag{5.5}$$

$$\theta = [\theta_0, \theta_1, ..., \theta_{N-1}]^T. \tag{5.6}$$

Note that there are only K non-zeros in θ. $x(t)$ is then fed into a length-L FIR filter $h(t)$:

$$h(t) = \sum_{i=0}^{L-1} h_i \delta(t - iT_h'), \tag{5.7}$$

where T_h' is the time delay between each filter tap.

The output $y(t) = h(t) * x(t)$ is then uniformly sampled with sampling period T_s'. T_s' follows the relation $T_s'/T_h = q$, where q is a positive integer. M samples are collected so that $M \cdot T_s' = \lfloor L \cdot T_h + T_x' \rfloor$, where $(L \cdot T_h + T_x')$ is the duration of $y(t)$.

Now we have the down-sampled output signal $y(mT_s'), m = 1, 2, ..., M-1$:

$$\begin{aligned} y(mT_s') &= h(mT_s') * x(mT_s') \\ &= \int_0^{T_y} h(mT_s - \tau)\, x(\tau)\, d\tau \\ &= \int_0^{T_y} \left[\sum_{i=0}^{L-1} h_i \delta(mT_s - iT_h - \tau)\right] x(\tau)\, d\tau \\ &= \sum_{i=0}^{L-1} h_i x(mT_s - iT_h) \\ &= \Phi x, \end{aligned} \tag{5.8}$$

where Φ is a $quasi - Toeplitz$ matrix and

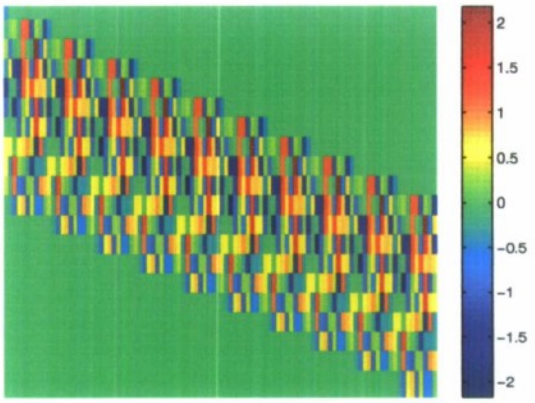

Figure 5.1: An example of $quasi-Toeplitz$ matrix. Each row is a shifted copy of the row above.

$$x = [x(0), x(T_h), ..., x((M-1)qT_h)]^T = \Psi\theta, \tag{5.9}$$

$$\Psi = [\Psi(0), \Psi(T_h), ..., \Psi((M-1)qT_h)]^T. \tag{5.10}$$

A $quasi-Toeplitz$ matrix has such property: each row of Φ has L non-zero entries and each row is a copy of the row above, shifted right by q places, as shown in Fig. 5.1.

Let $y_m = y(mT_s)$, we have

$$y = [y_0, y_1, ..., y_{M-1}]^T. \tag{5.11}$$

Combining Equations 5.4, 5.5, 5.6, 5.8, 5.9, 5.10 and 5.11, we have:

$$y = \Phi\Psi\theta = \Theta\theta \tag{5.12}$$

Now the problem becomes recovering $N \times 1$ vector θ from the $M \times 1$ measurement vector y, which is exactly the same as the problem posed in Equation 5.3. The number of measuremcnts for successful recovery depends on the sparsity K, duration of the analog signal T_x, filter length L and the incoherence between Φ and Ψ. Numerical results in Section 5.3 show that when $x(t)$ is sparse and $h(t)$ is a PN sequence, θ can be reconstructed successfully with a reduced sampling rate, requiring only $M << N$ measurements. Note that measurement y is a projection from x via an FIR filter. We use this feature to design our proposed system.

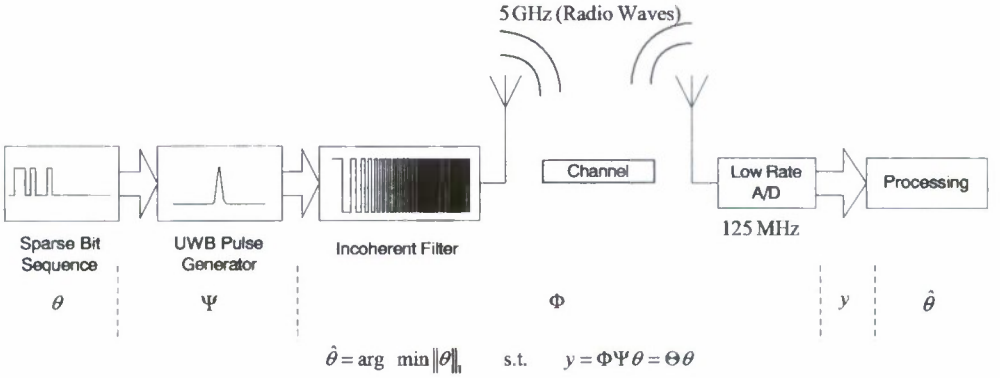

Figure 5.2: The system architecture of the proposed CS based UWB system. The communication problem of recovering the transmitted information can be modeled as a CS problem.

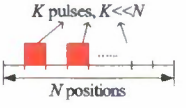

Figure 5.3: The structure of the transmitted symbol. This symbol is K-sparse. There are K pulses in N positions and $K << N$.

5.3 Compressed Sensing Based UWB Communication System

5.3.1 Communication system architecture

With the knowledge of Section 5.2.1 and Section 5.2.2, we propose a CS-based UWB communication system which is able to reduce the sampling rate to 1.25% of Nyquist rate. The system architecture is illustrated in Fig. 5.2. A UWB signal is transmitted by feeding a sparse bit sequence through a UWB pulse generator and an pre-coding filter. Then, the received signal is directly sampled after the channel, using a low-rate A/D and then processed by a recovery algorithm. Φ is the projection matrix consisting of the pre-coding filter and the channel. It can be noticed that channel itslef is part of the projection matrix in CS, so the receiver is very simple, with only one low-rate A/D to collect measurement samples. Our simulation in Section 5.4 shows that 3 – 8 GHz UWB signals can be successfully recovered by a 125 Msps A/D.

K-pulse position modulation (PPM) is used to modulate sparse bit sequence. Each PPM symbol is K-sparse: there are N positions and only $K << N$ pulses in each symbol, as illustrated in Fig. 5.3. The output of the UWB pulse generator can be written using the notations in Equation 5.4 and 5.5, with $\Psi_n(t) = p(t - nT_p)$, where $p(t)$ is the function of the UWB pulse and T_p is the period of the pulse. Pre-coding filter and channel are modeled as FIR filters, with combined impulse response $h(t) = f(t) * c(t)$, where $f(t)$ and $c(t)$ are the impulse response for the pre-coding filter and the channel, respectively. Here $h(t)$ is equivalent to the $h(t)$ in Equation 5.7. The received signal $y(t) = h(t) * x(t)$ is then uniformly sampled by an A/D with sampling period T_s. Similar to Equation 5.8 and 5.11, the down-sampled measurements form the $M \times 1$ vector $y = \Phi\Psi\theta = \Theta\theta$, where Φ is a $quasi - Toeplitz$ matrix. Now, the communication problem becomes a problem of estimating $\hat{\theta}$ from $M << N$ measurements, which is again identical to the problem described as Equation 5.3.

Figure 5.4: Block diagram of channel estimation

Figure 5.5: An equivalent block diagram of channel estimation

The success of recovery relies on the sparsity K and the incoherence between Ψ and Φ. Sparsity is easily met by controlling the transmitted sequence. In our simulation, $K = 1$, which means that there is only one pulse in PPM symbol. The incoherence property can be met by proper selection of the pre-coding filter $f(t)$. Simulation results show that if $f(t)$ is a PN sequence whose chip rate is equal to the bandwidth of the UWB pulse $p(t)$, θ can be successfully recovered using recovery algorithms. So far the discussion is in baseband. If the transmitted UWB is passband, then up-conversion is applied after the pre-coding filter. PN chip rate and the receiver structure remain the same. No down-conversion is required at the receiver. For example, as will be shown in the simulation, a 3 – 8 GHz UWB pulse requires a 5 GHz PN chip rate, which is the same as the signal bandwidth, not the Nyquist rate of the maximum signal frequency, as required by the AIC system. A/D at the receiver directly samples the received signal, without doing down-conversion.

The number of measurements M and sampling rate are related and determined by the length of the combined filter $h(t)$. If $h(t)$ is long, the received signal is "spread out" in the time domain, therefore sufficient measurements can be made under a lower sampling rate.

5.3.2 Channel estimation

After down-sampling, y is processed at the receiver with Θ using BP. In constructing Θ, $f(t)$, $c(t)$ and $\Psi(t)$ are required. $f(t)$ and $\Psi(t)$ are fixed and can be considered as prior knowledge at the receiver. The channel, $c(t)$, however, needs to be estimated. A CS based channel estimation method is proposed. A 3 – 8 GHz channel can be estimated by a 500 Msps A/D.

Similar to Equation 5.7, the UWB channel can be modeled as:

$$c(t) = \sum_{i=0}^{L-1} c_i \delta(t - i l_h) \tag{5.13}$$

The channel estimation block diagram is illustrated in Fig. 5.4. A UWB probing pulse $p(t) * f(t)$ is transmitted to "probe" the channel, where $p(t)$ is a UWB pulse and $f(t)$ is a PN sequence. At the receiver, sub-Nyquist rate A/D collects M uniform measurements. This process can be represented as $y = D \downarrow (c(t) * f(t) * p(t))$, where $D \downarrow$ denotes a down-sampling factor of $\lfloor N/M \rfloor$ and y denotes the measurement vector. Since the system is LTI, an alternative block diagram can be drawn as Fig. 5.5. Then, $y = D \downarrow ((f(t) * p(t)) * c(t))$. In matrix notation, $y = \Theta c$, where Θ is a $quasi - Toeplitz$ matrix derived from $f(t) * p(t)$ and $c = [c_0, c_1, ..., c_{L-1}]^T$. The channel estimation problem is to get $\hat{c}$ from measurements y, which is identical to the CS problem described in Equation 5.3.

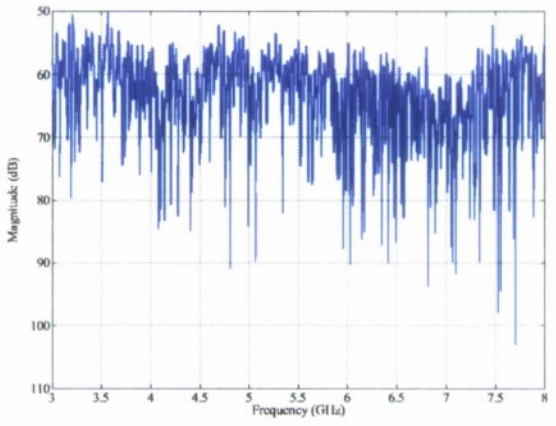

Figure 5.6: Frequency domain data from VNA measurement.

Successful recovery requires c to be sparse and the incoherent property of measurement matrix Θ [11]. Indoor UWB channel is sparse and PN sequence structured Θ has the incoherent property. PN chip rate should be the same as the bandwidth of the channel under estimation. We use simulation to show the estimation result.

First, we need to set up the real channel $c(t)$ as the estimation target. Vector network analyzer (VNA) is used to get the real indoor channel coefficient c. 3 – 8 GHz channel is measured by VNA with 1 MHz frequency step and 128 averages. c is derived from CLEAN algorithm using a rectangular window in frequency domain. The VNA result and the relative time domain channel $c(t)$ are depicted in Fig. 5.6 and Fig. 5.7. $c(t)$ has about 50 non-zero entries in c. PN chip rate is 5 GHz and length of $f(t)$ is 1 μs. Baseband Gaussian UWB pulse $p(t)$ has 5 GHz bandwidth. Since the measured channel is in passband, up-conversion is applied after the PN filter. At the receiver, 500 Msps A/D is used to get measurements. BP is then used to get the estimated vector $\hat{c}$ with the knowledge of $f(t)$, $p(t)$ and y only. Additive white Gaussian noise (AWGN) is added at the received samples as $y = \Theta c + w$, where w is the noise vector. Basis pursuit denoising (BPDN) is used to solve the recovery problem with noise. Fig. 5.8 (a) shows the estimation result and Fig. 5.8 (b) shows the zoomed in result. It can be seen that though $\hat{c}$ is a little noisy, all major paths in $\hat{c}$ perfectly match to c. Only the amplitudes are slightly different.

We will use c as "perfect estimation" to form the measurement matrix Φ and the noisy $\hat{c}$ as "imperfect estimation" to form the measurement matrix $\hat{\Phi}$ in the CS-based UWB communication system symbol error rate simulation. Interestingly, though imperfect estimation is noisy, the symbol error rate is similar to perfect estimation.

5.4 Simulation Results

Since UWB channel is stable when few movements exist in the indoor environment, we assume that channel is time-invariant during the channel estimation and communication process.

In the simulation, each symbol has only one pulse in 256 candidate positions, containing 8 bits information. This is a special case of the PPM symbol illustrated in Fig. 5.3, with $K = 1$. More pulses can be used to increase the information per symbol. Since the purpose of the paper is to recover θ, not maximizing the data rate, the case when $K > 1$ is not simulated. The UWB pulse generator produces a 5 GHz bandwidth Gaussian pulse. The pre-

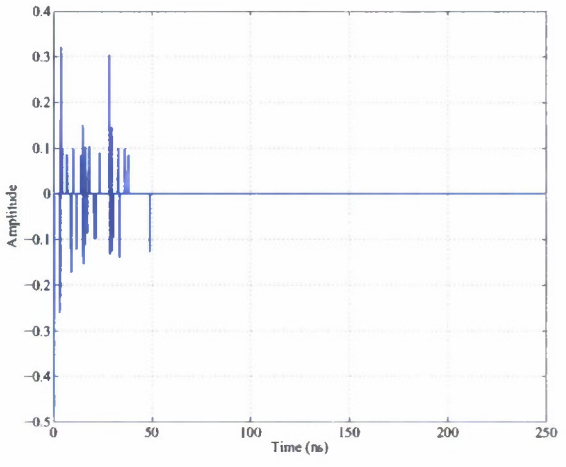

Figure 5.7: Time domain channel derived from VNA measurement. The sparsity of this channel is 50.

coding filter is a PN sequence with 128 ns duration and 5 GHz chip rate. Then the signal is modulated with a 5.5 GHz sinusoidal, up-converting to the 3 – 8 GHz frequency band. Measured channel $c(t)$ in 5.7 is used. Due to the delay spread of the channel and the length of PN sequence, the received signal y(t) is spread out over 256 ns. A 256 ns guard period is added between symbols to avoid intersymbol interference (ISI). At the receiver, perfect synchronization is assumed. 125 Msps, 250 Msps and 500 Msps sampling rates are simulated to evaluate the symbol error rate VS SNR per symbol performance. Since measurements are made in a 512 ns period, the relating numbers of measurements M for 125 Msps, 250 Msps and 500 Msps are 64, 128 and 256, respectively. BPDN provided by [20] is used as the reconstruction algorithm. The position with maximum amplitude in $\hat{\theta}$ is compared with the position in θ. If two positions are exactly the same, the symbol is considered as reconstructed successfully. 20000 simulations were performed for each SNR plot.

Fig. 5.9 shows the reconstruction result under 125 Msps sampling rate without any additive noise. $\hat{\theta}$ reconstructed from perfect/imperfect channel profile is compared with original θ. From Fig. 5.9, we can see that $\hat{\theta}$ from imperfect channel profile is a bit more noisy. However, the position of maximum amplitude is exactly the same as the one in θ. Therefore, the transmitted symbol is recovered successfully. After 20000 simulations, no errors can be found.

Fig. 5.10 shows the results under AWGN. Perfect/imperfect channel estimation and 125 Msps/250 Msps/500 Msps sampling rate are simulated. We can see that higher sampling rate provides better symbol error rate performance. This is because more measurements are collected under higher sampling rate. It is also noticed that under same sampling rate, the symbol error rate of perfect channel estimation and imperfect channel estimation have almost no difference. From the 500 Msps sampling rate curve, we can see that the symbol error rate is 0 when SNR is over -6 dB, in 20000 simulations.

Many interesting topics are raised after the simulation. Does the measurement matrix Φ and Ψ satisfy the incoherence property in theory? What is the relationship for sampling rate, SNR and symbol error rate? Why the imperfect channel estimation shows similar performance with perfect channel estimation? How to achieve synchronization with the system? Further effort needs to be done to explain these questions.

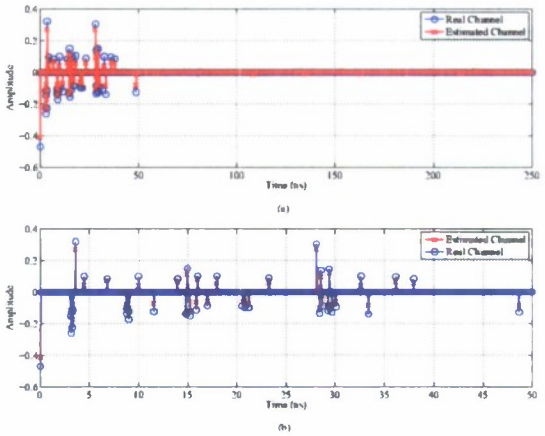

Figure 5.8: (a) Channel estimation result. (b) Zoomed in version of the result.

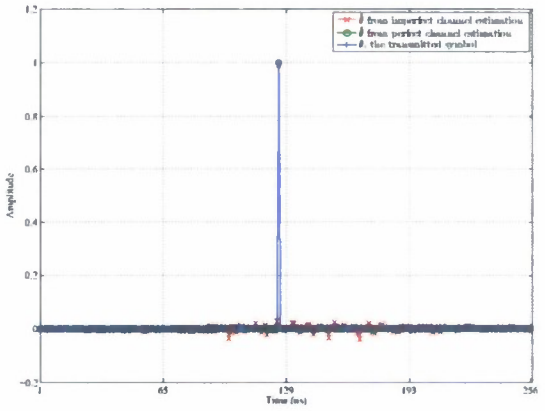

Figure 5.9: Recovery of $\hat{\theta}$ using 125 Msps A/D, perfect/imperfect channel estimation. No noise is added.

5.5 Conclusions

Our proposed approach is to exploit the projection matrix with channel itself and a waveform-based pre-coding at the transmitter. Taking the channel as part of CS results in a very simple receiver design, with only one low-rate A/D. The pre-coding is implemented in a natural way using an FIR filter. The concept has been demonstrated, through simulations, using real-world measurements. Realistic channel estimation is also considered. The philosophy is to trade computation complexity for hardware complexity, and move receiver complexity to the transmitter.

This work is just the beginning of the pre-coded CS. Future work includes reduction of algorithm complexity. BP and OMP are two families of algorithms for applications like imaging and sensing. Much quicker algorithms are required for real-time applications such as UWB communications. Deterministic CS [21] will be considered in the context of UWB channel.

Traditional pre-coding optimizes the system in the digital domain. The waveform-based pre-coding optimizes the

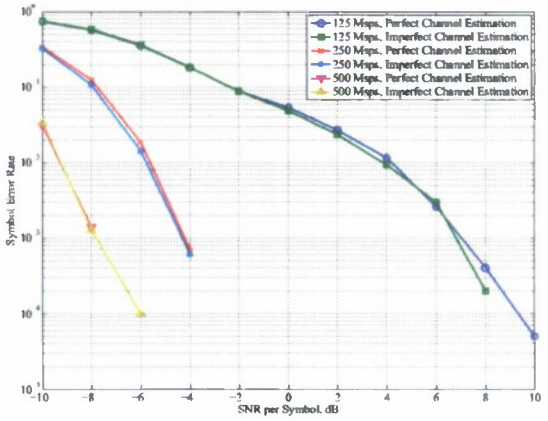

Figure 5.10: Simulation results of symbol error rate vs SNR per symbol at the receiver.

transceiver in both mixed signal and digital domain. CS provides a natural framework. The minimum complexity can be the optimization criterion. It may be more natural to combine waveform-based pre-coding with sampling innovation [22], since pre-coding can be used to reduce the degrees of freedom—thus the sampling rate.

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Part II

Appendix

Chapter 6

The Second Generation Time-Reversal Test-bed Reference Manual. Rev. 0.1

6.1 Overall Introduction

A general purpose Time-Reversal UWB transceiver test-bed for communication and ranging was developed. The main goal is to implement a pair of transmitter and receiver to verify our Time-Reversal conceptual-proof schemes. The design is based on energy (square law) detection reception technology. On April 14, 2008,we demonstrated the very first time reversal UWB radio in our lab. The major parameters of the test-bed under test are as follows.

- bandwidth: 800 MHz
- center frequency: 4 GHz
- chip rate: 25 Mc/s
- bit rate: 6.25 Mb/s
- propagation channel: indoor NLOS, 5 m

Pulse based signaling and transmitter-side processing are adopted as system design guideline. Although direct pulse (carrier less) transmission can largely reduce complexity of transmitter RF front-end, it is not a good choice for multi-purpose radio testbed mainly because of its inflexibility. As a matter of fact, a modulated pulse is not only easy to generate but also more flexible: the center frequency is determined by a local oscillator and the spectral shape is governed by the baseband pulse. Conceptual testbed architecture is shown in Figure 6.1. Following an FIR filter (embedded in the FPGA), the digital-to-analog converter (DAC) outputs desired analog waveforms. The simple-receiver philosophy is reflected in this testbed with on/off keying (OOK) and diode based non-coherent detector at the receiver. At the receiver, demodulation is done in digital domain, so that algorithms and parameters can be

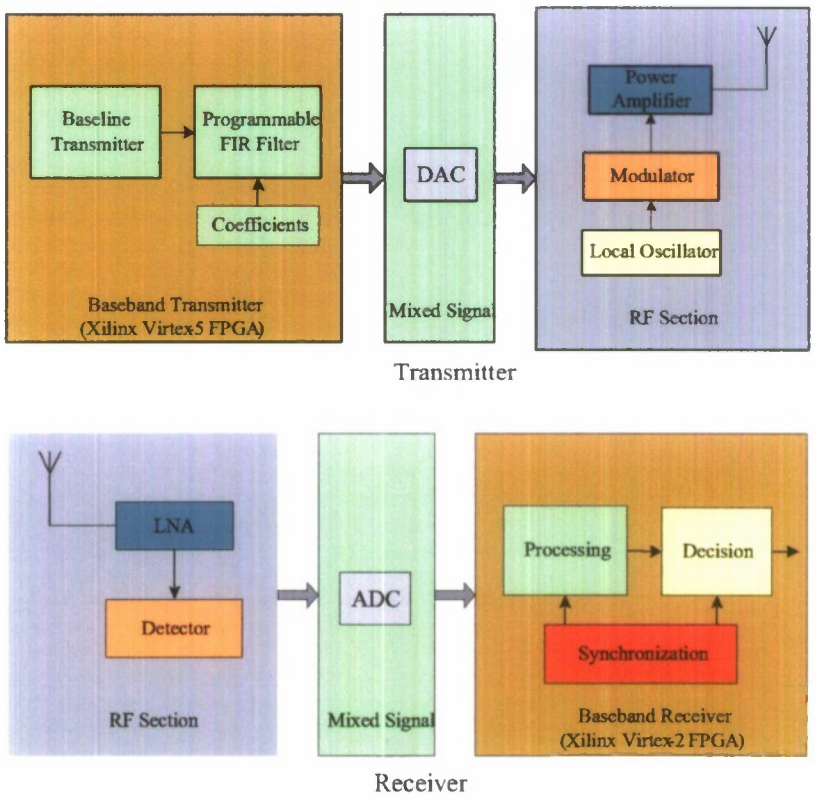

Figure 6.1: Overall testbed architecture.

adjusted easily. Of course, the analog-to-digital converter (ADC) is power hungry and it may be replaced by some substitute circuits in commercialized products in the future.

Noticeable temporal focusing has been seen and successful data transmission has been experimentally demonstrated in this some how harsh environment. Encouraged by this historical demonstration, we will continue the project toward next goalssystem improvement and double transmission distance, To achieve these in one year, there will be a body of challenging jobs including transplanting the receiver back-end from the Virtex-2 platform to the Virtex-5 platform, increase of the prefilter length, and solving the dynamic range problem, etc. At current stage, the receiver back-end is powered by Virtex-5 platform and we are modifiying the system to double transmission distance.

6.2 Transmitter setup and configuration

At the testbeds transmitter side,there are mainly five parts: Xilinx Virtex-5 LXT Prototype Platform, Fujitsu DK86064 DAC Evaluation Kit, TRF3703-15 Quadrature Modulator Evaluation Module, PSA4000A Local Oscillator Evaluation Board and Mini-Circuits ZVE-8G Amplifier.Transmitter Architecture is shown as Figure 6.2. Baseband signals from DAC are converted to passband signal by modulator and then be sent to the amplifier, the output signal of amplifier goes to the antenna and then be transmitted through the air. major components and modules for transmitter side are listed in Table 6.1.

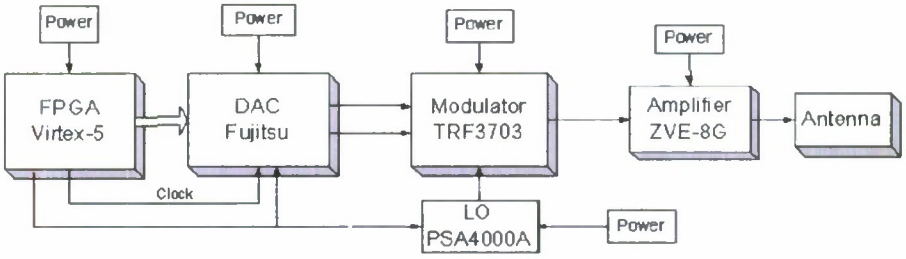

Figure 6.2: The architecture of test-be transmitter

Table 6.1: A list of Selected Components/Modules for Transmitter

FPGA back-end	Virtex-5 LXT	Xinlix	65nm/1.0V core/550MHz/17,280 slices/680 User I/Os
DAC	MB86064	Fujitsu	Dual 14-bits 1GSa/s
Local oscillator	PSA4000A	Z-communications	Center frequency 4.0 GHz
Modulator (up-converter)	TRF3703-15	Texas Instruments	Direct quadrature modulator 400 MHz to 4 GHz
Amplifier	ZVE-8G	Mini-circuits	Wideband(2 to 8 GHz)/ low noise(4 dB typ)/35dB gain

6.2.1 Power Level

- FPGA-Virtex 5 board: 5V- 6A;
- DAC board: 1.8V- 0.26A; 3.3V- 0.10A;

- Modulator: 5V-0.05A; 5V- 0.21A;
- Local Oscillator: 6.1V- 0.12V;
- Power Amplifier: 12V- 0.87A;

6.2.2 Connection

1 Modulator (TRF3703-15)

1) Connect output (To DSO, Amplifier, or antenna, or spectral analyzer)

2) Power on (5V, ¡205mA)

3) Connect input from Local Oscillator and DAC

2 Amplifier (2VE-8G)

1) Connect output (To antenna)

2) Power on (12V, 0.87A)

3) Connect input from Modulator

3 Local Oscillator

1) Connect output (To Modulator)

2) Power on (6.1V, 0.12A)

3) Configure it to work at 4.0GHz

4 FPGA+DAC

1) Connect output

2) Power on (DAC, 1.8V, .16A; 3.3V, 0.08A)

2) Start

6.2.3 Disconnection

1) DAC+FPGA stop, Power off

2) Local Oscillator Power off, Configuration device power off

3) Modulator Power off

4) Amplifier input disconnect, then power off.

FPGA configuration

There are two configuration files used in the transmitter FPGA, one is when the waveform is 4 ns pulse waveform, the other one is when the waveform is is time reversed channel impulse response. the first bit files is xxx1, the second bit files is xxx2.

Note that current FPGA cannot download MCS file to Prom for some reason.

If the waveform is 4 ns pulse, the functionalities in FPGA is shown in Figure 6.3. Figure 6.4 shows the results observed from ChipScope. If the waveform is time reversed channel impulse response, the functionalities in FPGA is shown in Figure 6.5. Figure 6.6 shows the results observed from ChipScope.

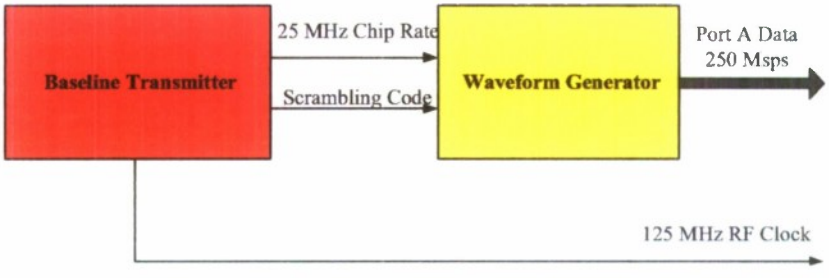

Figure 6.3: The functionalities in Virtex-5 FPGA if 4 ns pulse is generated.

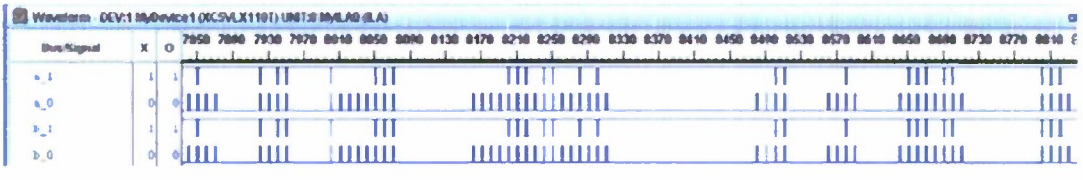

Figure 6.4: The results observed from ChipScope if 4 ns pulse is generated.

Discrete-time waveform is generated by the waveform generator module in FPGA based on chip value, scrambling code and the pre-loaded waveform template. Figure 6.7 shows the implementation of the waveform generator module. The discrete-time waveform is then fed to the DAC via the high-speed connection buses. Because of the limitation of the high-speed connection, only 2 bits are used to represent the continuous waveform in the digital domain. Owing to the introduction of scrambling code, the ternary quantization of the continuous waveform is implemented in FPGA.

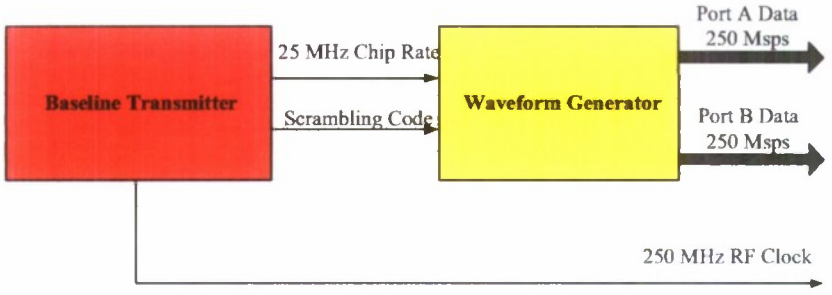

Figure 6.5: The functionalities in Virtex-5 FPGA if time reversed channel impulse response is generated.

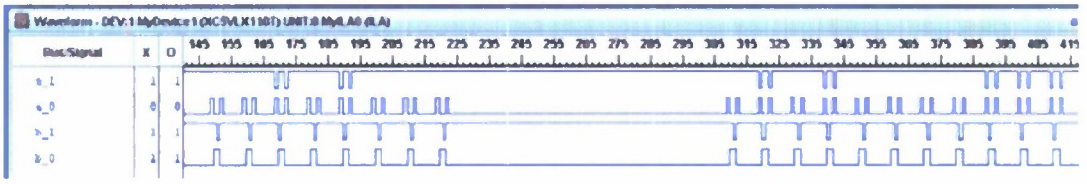

Figure 6.6: The results observed from ChipScope if time reversed channel impulse response is generated.

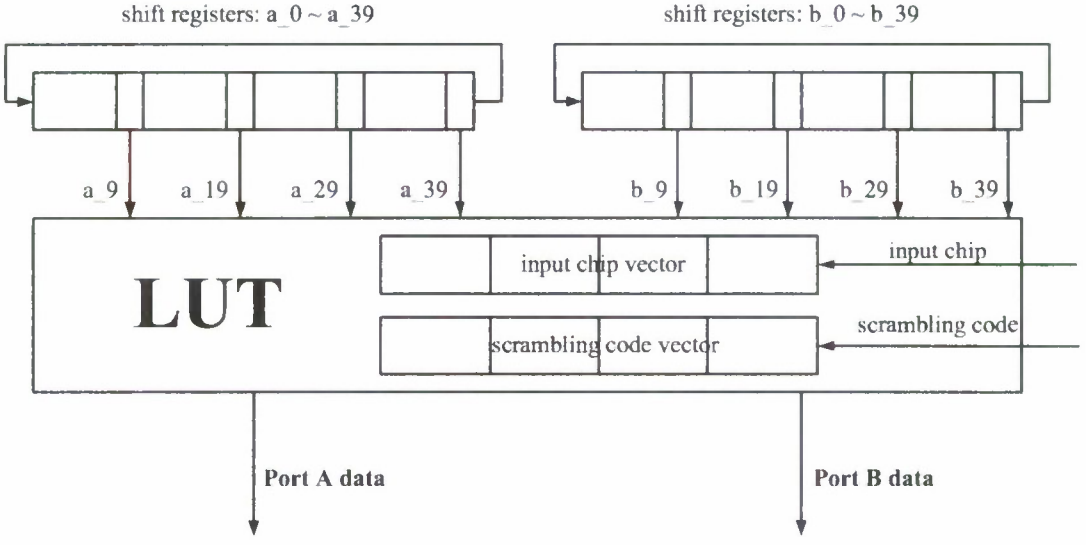

Figure 6.7: The implementation of the waveform generator module.

6.2.4 DAC configuration

The two different transmitted waveform two different DAC configurations. For pulse-based waveform, The interface is shown as Figure 6.8.as we can see there is no interleave within DAC. For time reversal waveform, The interface is shown as Figure 6.9. As we can see input A and input B are interleave in DAC.

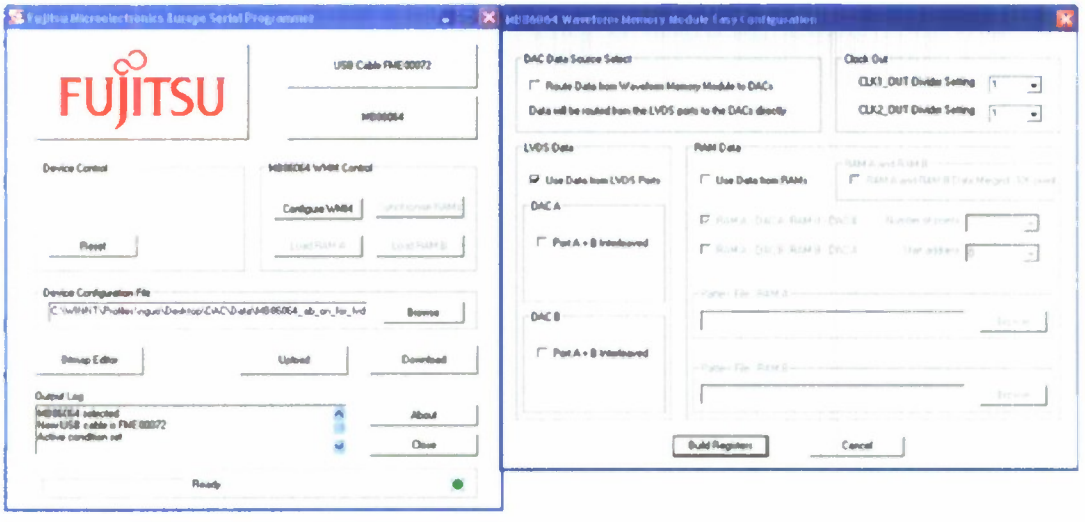

Figure 6.8: DAC configuration when 4 ns pulse is transmitted.

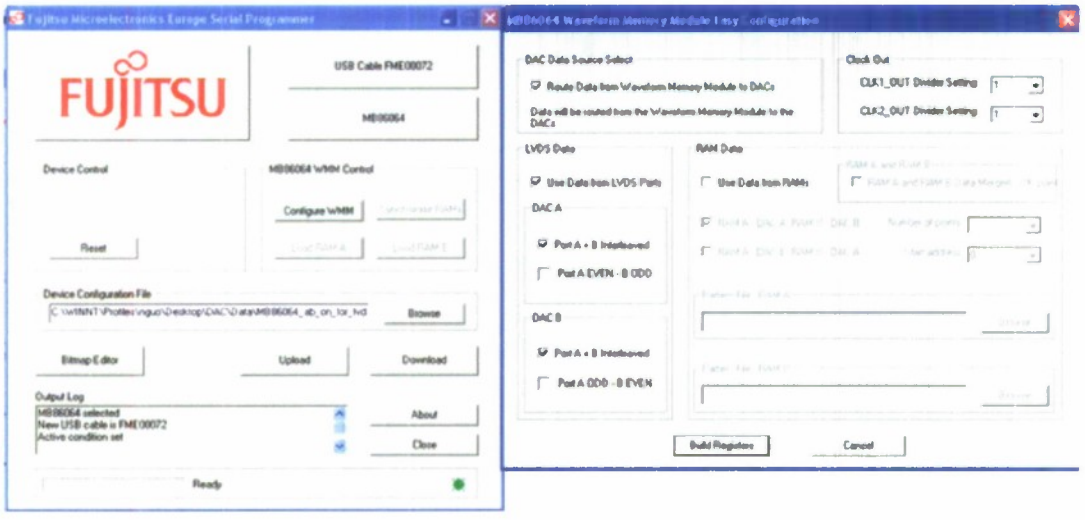

Figure 6.9: DAC configuration when time reversed channel impulse response is generated.

Note that the files to be downloaded to DAC are the same: MB86064_ab_on_for_lvds_data.txt.

6.2.5 DAC and FPGA connection

The picture of the baseband arbitrary waveform generator is shown in Figure 6.10. As we can see, data and clock signal are fed to DAC board from FPGA hoard through Intronix probing cable and SMA cable respectively. According to our measurement results, this probing cable can actually support sampling at 1 GHz. Note that when only DAC A port or B port is used, the other port should be properly terminated.

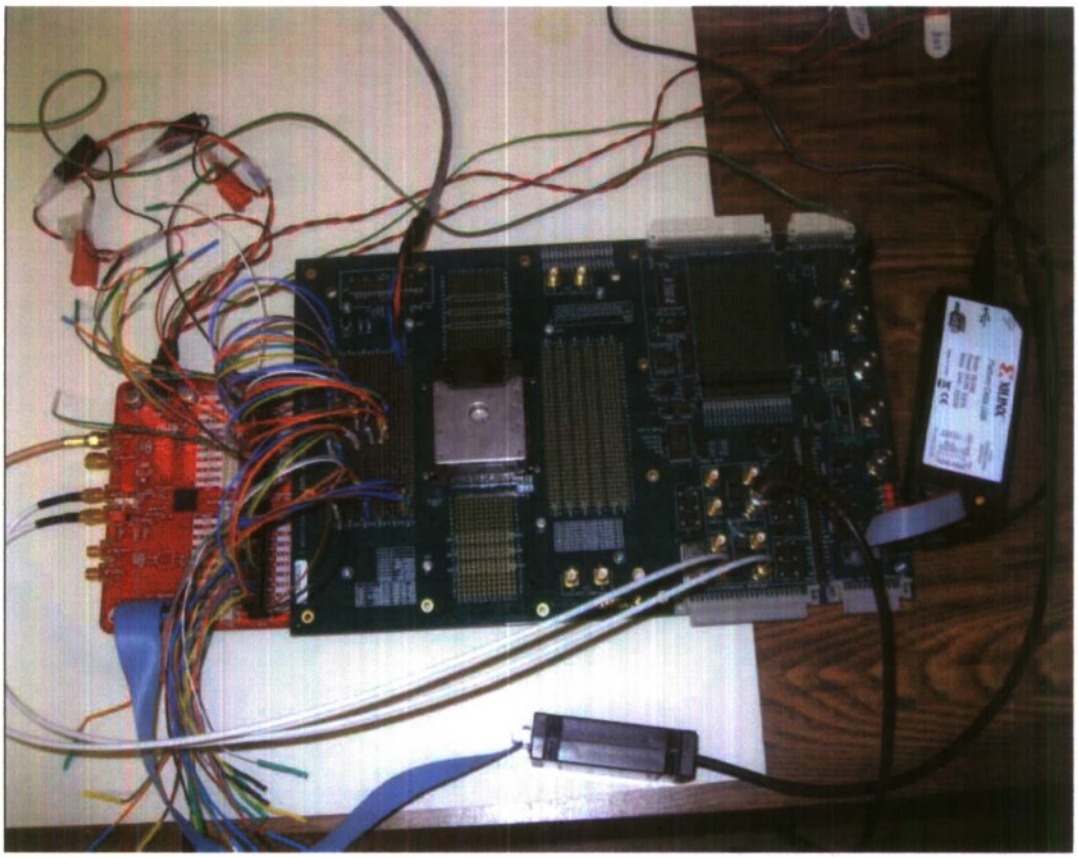

Figure 6.10: The picture of the baseband arbitrary waveform generator in the transmitter side.

According to thc connection limitations between FPGA and DAC board, the DAC requires the FPGA to providc two channels running at 2-bit resolution with 250 MHz sampling rate and one 250 MHz clock signal. The final pin assignment of the DAC and the FPGA is shown in Table 6.2.

6.2.6 Transmitter RF Front-End

We mainly rely on off-the-shelf products in our test-bed's RF development.The test-bed's transmitter RF front-cnds can be shown as Figure 6.11.

Local Oscillator PSA4000A is used to generated 4.0GHz frequency for modulator, it is configured by FPGA board through an SPI port. whenever the FPGA board is powered on, the Local Oscillator is configured automatically to

Table 6.2: Pin assignment.

Port Name	FPGA Pin #	DAC Pin #
waveform_data_a_p <0>	T28	A8
waveform_data_a_n <0>	T29	X_A8
waveform_data_a_p <1>	W31	A9
waveform_data_a_n <1>	Y31	X_A9
waveform_data_a_p <2>	V28	A10
waveform_data_a_n <2>	V27	X_A10
waveform_data_a_p <3>	Y27	A11
waveform_data_a_n <3>	W27	X_A11
waveform_data_a_p <4>	V30	A12
waveform_data_a_n <4>	W30	X_A12
waveform_data_a_p <5>	U27	A13
waveform_data_a_n <5>	U28	X_A13
waveform_data_a_p <6>	AB31	A14
waveform_data_a_n <6>	AA31	X_A14
waveform_data_b_p <0>	T31	B8
waveform_data_b_n <0>	R31	X_B8
waveform_data_b_p <1>	P34	B9
waveform_data_b_n <1>	N34	X_B9
waveform_data_b_p <2>	A30	B10
waveform_data_b_n <2>	B30	X_B10
waveform_data_b_p <3>	N33	B11
waveform_data_b_n <3>	M33	X_B11
waveform_data_b_p <4>	C34	B12
waveform_data_b_n <4>	D34	X_B12
waveform_data_b_p <5>	F31	B13
waveform_data_b_n <5>	E31	X_B13
waveform_data_b_p <6>	B25	B14
waveform_data_b_n <6>	C25	X_B14

work at 4.0 GHz. As the RF picture shows, there is a DB9 cable which connect the Local Oscillator and FPGA.

SPI module pins assignment in FPGA is as shown in Table 6.3.

Quadrature modulator TRF3703-15 is used to convert complex modulated signals from baseband directly up to RF.there are two inputs for modulator, one is the 4.0GHz clock signal from Local oscillator and the other one is the transmitted waveform signal for DAC board.

However,Both the DACs output and modulators baseband input are differential type. RF transformer based AC coupling is used to bridge the DAC and modulator as shown in Figure 6.12. The advantage of using transformers is that they isolate the DC connection between the two devices but still provide wide bandwidth. The 82-ohm and 36-ohm resistors accommodate about 50 ohm input impedance and common mode voltage about 1.5 V required by the modulator.

ZVE-8G by Mini-circuits is a power amplifier operating from 2-8 GHz with +30 dB gain and a 1 dB compression

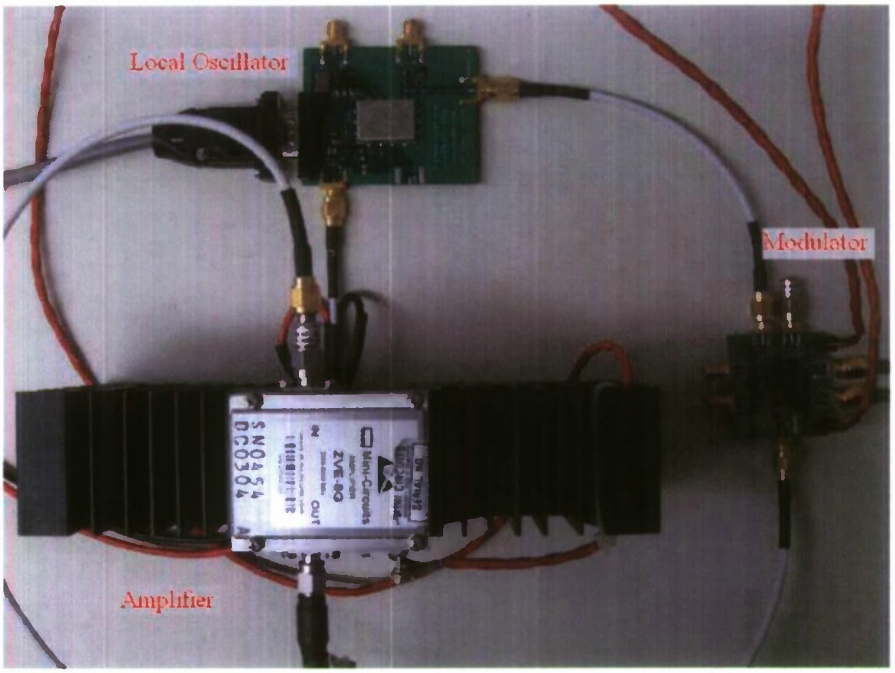

Figure 6.11: The picture of transmitter RF front-ends.

point of 30 dBm. The unit requires a single 12 V 1.2 A supply.

6.3 Receiver setup and configuration

The receiver design is based on energy (square law) detection reception technology, the architecture is shown as Figure 6.13 and the actual picture is as shown as Figure 6.14. The MAX108, an 8 bits,1.5 GHz flash ADC, is employed to convert the analog signal into digital signal in the baseband. the digital back-end is powered by newly transplanting Virtex-5 LXT development board.

6.3.1 Power Level

- RF board: +5V; Provided by FPGA board;
- Low noise amplifier: +15V;
- ADC board: +3.3V Digital ; +5V,-5V Digital; +5V Analog;

Table 6.3: Pin assignment.

Port Name	FPGA Pin #
sclk	AP25
mosi	AN25
le	AM25
led_show_lo	G33

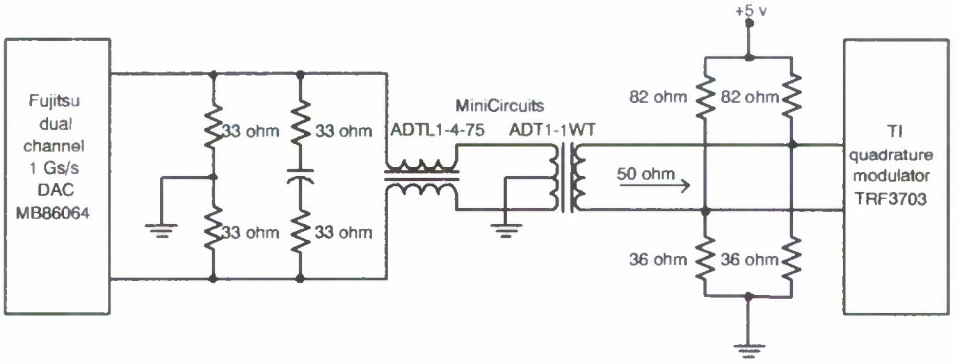

Figure 6.12: Coupling between DAC and modulator

- FPGA board: +5V, 6A;

The ADC power connection is as Figure 6.15 shows.

6.3.2 FPGA configuration

For Virtex-5 FPGA in the receiver side,there is one configuration file to be download to the prom of the Virtex-5 FPGA board. The pins assignment can be shown as Fig. 6.16, the pin E13 is the output signal, which is the final output result after demodulation. this signal can be monitored directly by equipment.

The receiver FPGA has the ability to set variable threshold, there are two push buttons PB3 and PB4 used to increase or decrease the value of the threshold, and 4 leds will shows the corresponding status. the push buttons and leds are as shown in Figure 6.14.The setting is as the Table 6.4 shows when pushing PB3 or PB4 button.

6.3.3 Connection between FPGA board and ADC board

As the pictures, the FPGA board and the ADC board are connected together through 50 SMA cables, with a ADC/FPGA interface board which is plugged into the Samtec connector on FPGA board, the interface solution can support signals with frequency of up to several GHz.

A 4-layer PCB board is designed and fabricated to have 50 Ω characteristic impedance for each trace. As shown in Fig. 6.17, for each pair of LVPECL signals, the traces are designed to have same length such that the positive and

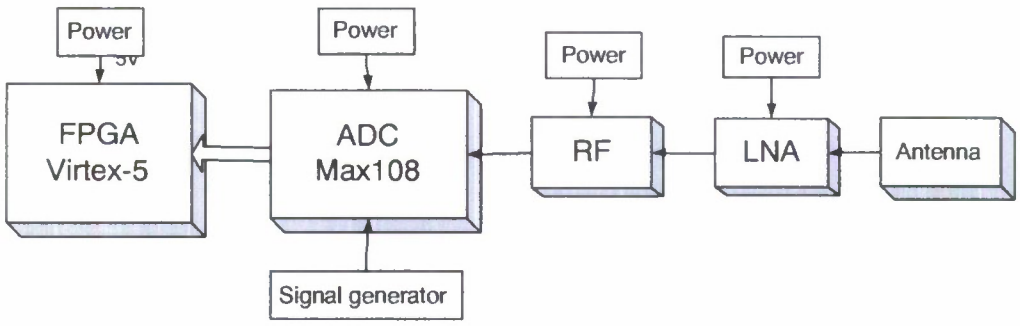

Figure 6.13: The architecture of the Test-bed receiver

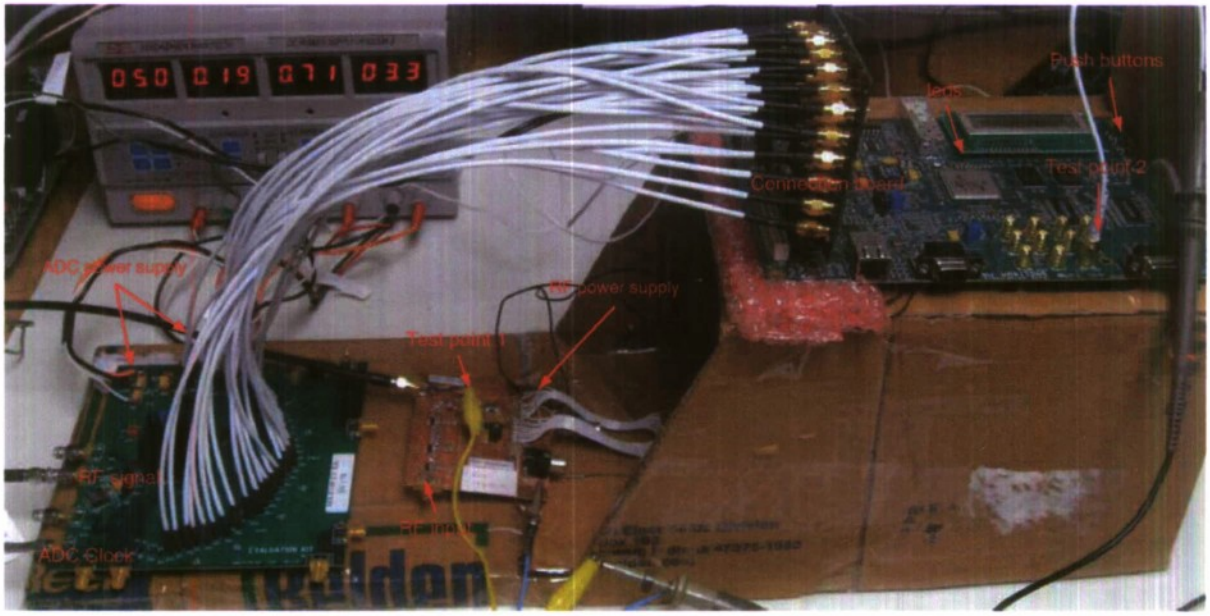

Figure 6.14: The picture of the Test-bed receiver

negative signals experience same delay.

6.4 System Test

There are two test points in the receiver side,as shown in Figure 6.14, Test point 1 is detector output, the output of the RF signal to be sampled by ADC. Test point 2 is the final demodulated signal, named as "'data out"' in FPGA, both the two signals are monitored by DPO. Besides, in order to observe the demodulated signal, a reference signal from the transmitter is necessary.

System test is required to performed in a typical non-line-of-sight (NLOS) environment. As out previous test shows, transmitter and receiver are located in compartment A and compartment B in Figure 6.18 and Figure 6.19. There are wood and metal shelves, desks and chairs, computers and electronic equipments in both compartments. Figure

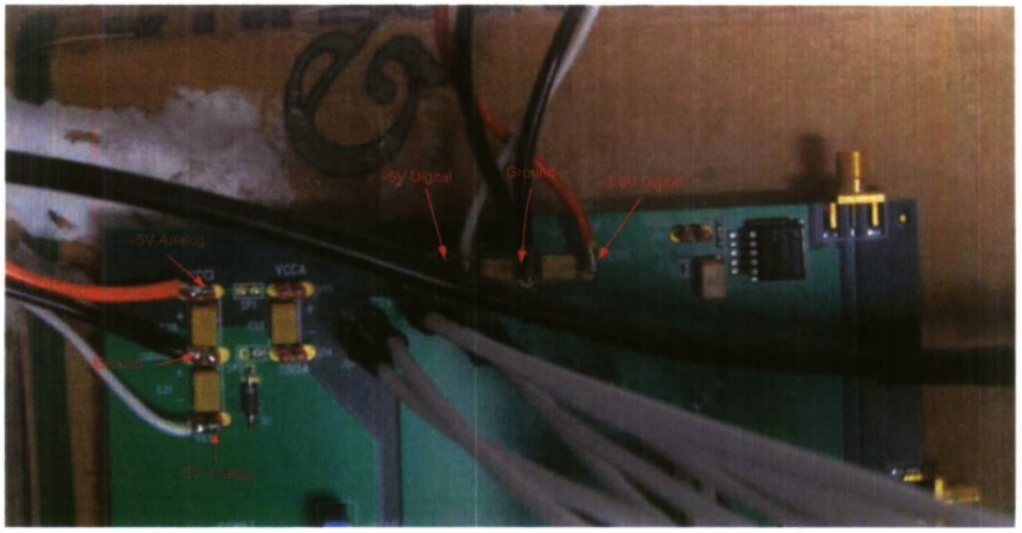

Figure 6.15: The power supply of ADC board

6.20 shows the layout of the office and the positions of the antennas. The transmit and receive antennas are NLOS. Multipaths can be obtained.

We first prepare the baseband time reversal waveform from the measurement, during the measurement, no people is inside the office. Since the channel is tend to change after measurement, we try to maintain the positions of all the furnitures and equipments.

The transmitted time reversal waveform captured by DPO at the transmitter side is shown in Figure 6.21. Figure 6.22 is the spectrum of the modulated time reversal waveform captured by Spectrum Analyzer. The center frequency is 4 GHz and the 10 dB bandwidth is about 800 MHz.

For single-pulse based waveform is as shown in Figure 6.23. The spectrum of the modulated waveform is shown in Figure 6.24. The center frequency is 4 GHz and the 10 dB bandwidth is about 400 MHz.

Figure 6.25 shows the system test result using time reversal waveform. The first trace is the transmitted waveform. The second trace is the detector output. The third trace is the bit stream. In the first trace, we can see that it is a zoom-out version of Figure 6.21. Distinguishable pulses can be observed in the second trace. In the third trace, we can clearly figure out the values of the bit stream. It is exactly the same as what is transmitted.

Figure 6.26 shows the system test result using the single-pulse waveform without time reversal. We can see undistinguishable pulses due to the multipaths. The third trace is flat. It means that the bit stream from FPGA decision is always '1'. Hence we can say that the system is not working.

Here we give a close-up to the second trace of the time reversal waveform test result, shown in Figure 6.27. The first trace is the transmitted waveform. The second trace is the received waveform after detector. The third trace is the bit clock running at 6.25 MHz. Time focusing property can be observed by comparing the first trace and the second trace. At the transmitter side, each chip period has four pulses. While at the receiver side, after the channel, each chip period has only one pulse. Four pulses arrive at the same position in time axis after propagating through the channel. Pulses between chips are clearly separated. Some sidelobes can be observed, because we use 2-bit ternary

INPUT

CONNECTOR	Pins	Signals		Pins	Signals
	E18	board_clk			
	AD14	rst_sw			
FX2-IO1	D9	REFCLKP	FX2-IO19	C6	RXN_data_P[0]
FX2-IO2	D10	REFCLKN	FX2-IO20	C7	RXP_data_P[0]
FX2-IO3	F8	RXN_data_A[0]	FX2-IO21	B7	RXN_data_P[1]
FX2-IO4	F7	RXP_data_A[0]	FX2-IO22	A7	RXP_data_P[1]
FX2-IO5	G9	RXN_data_A[1]	FX2-IO23	G7	RXN_data_P[2]
FX2-IO6	F9	RXP_data_A[1]	FX2-IO24	H7	RXP_data_P[2]
FX2-IO7	J8	RXN_data_A[2]	FX2-IO25	A5	RXN_data_P[3]
FX2-IO8	H8	RXP_data_A[2]	FX2-IO26	B6	RXP_data_P[3]
FX2-IO9	A8	RXN_data_A[3]	FX2-IO27	A10	RXN_data_P[4]
FX2-IO10	A9	RXP_data_A[3]	FX2-IO28	B10	RXP_data_P[4]
FX2-IO11	E7	RXN_data_A[4]	FX2-IO29	A3	RXN_data_P[5]
FX2-IO12	E8	RXP_data_A[4]	FX2-IO30	A4	RXP_data_P[5]
FX2-IO13	C8	RXN_data_A[5]	FX2-IO31	A12	RXN_data_P[6]
FX2-IO14	B9	RXP_data_A[5]	FX2-IO32	B11	RXP_data_P[6]
FX2-IO15	D6	RXN_data_A[6]	FX2-IO33	B5	RXN_data_P[7]
FX2-IO16	E6	RXP_data_A[6]	FX2-IO34	B4	RXP_data_P[7]
FX2-IO17	D8	RXN_data_A[7]			
FX2-IO18	C9	RXP_data_A[7]			

OUTPUT

GTP		
EXTERNAL GTP CLOCK		
GCLK0(J10)	E13	data_out

Figure 6.16: New pins assignment in the receiver FPGA

quantization and there are only four pulses in each chip. However, from Figure 6.27, we can claim that, to the best of our knowledge, the time focusing property of time reversal is verified by our test-bed for the first time.

Table 6.4: Pin assignment.

Leds status	Threshold value
0000	1/2
0001	1/4
0010	1/8
0011	1/16
0100	1/32
0101	1/2
0110	1/2
0111	1/2
1000	1/2
1001	1/2
1010	1/2
1011	1/2
1100	1/2
1101	1/2
1110	1/2
1111	1/2

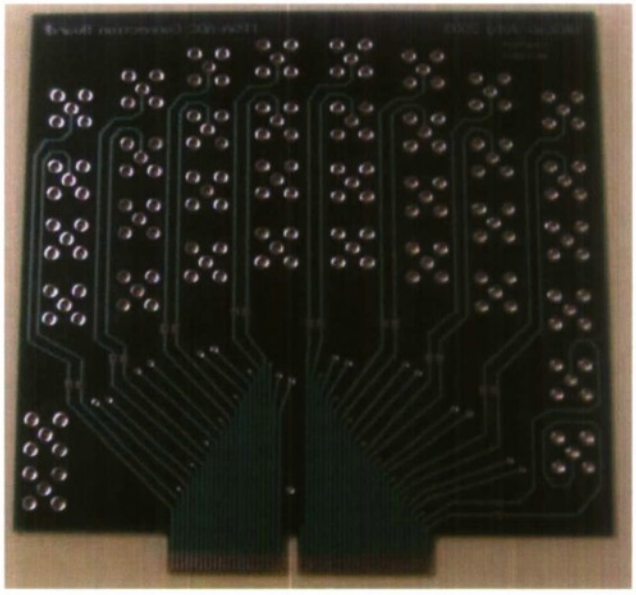

Figure 6.17: The connection board between ADC board and FPGA board

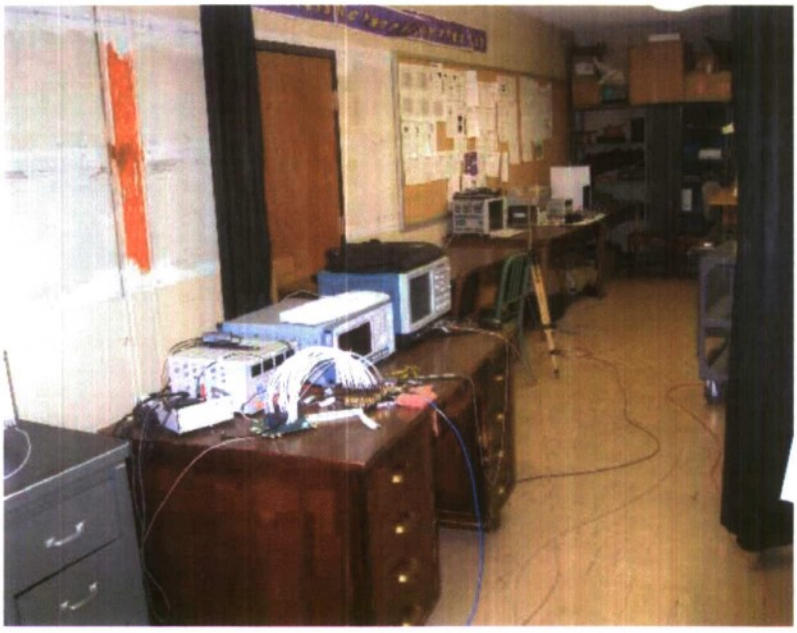

Figure 6.18: Room 400, compartment A.

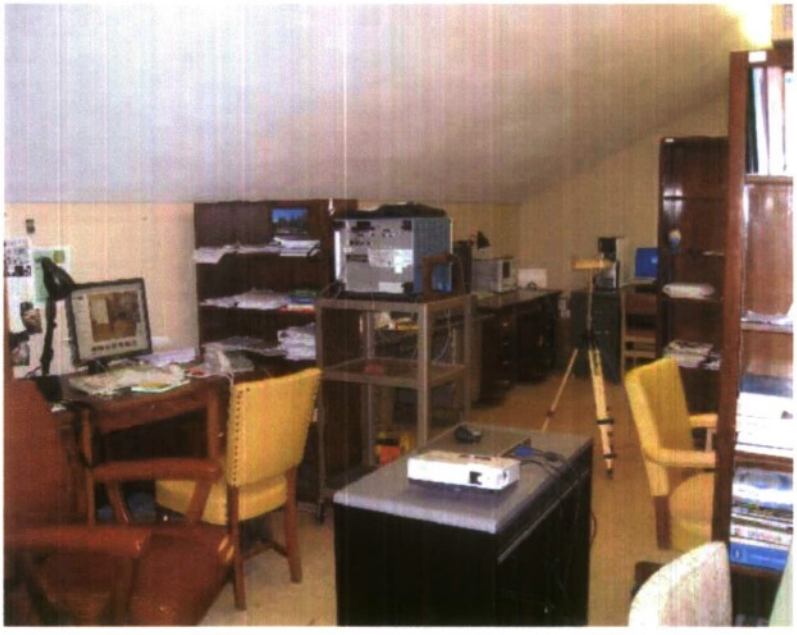

Figure 6.19: Room 400, compartment B.

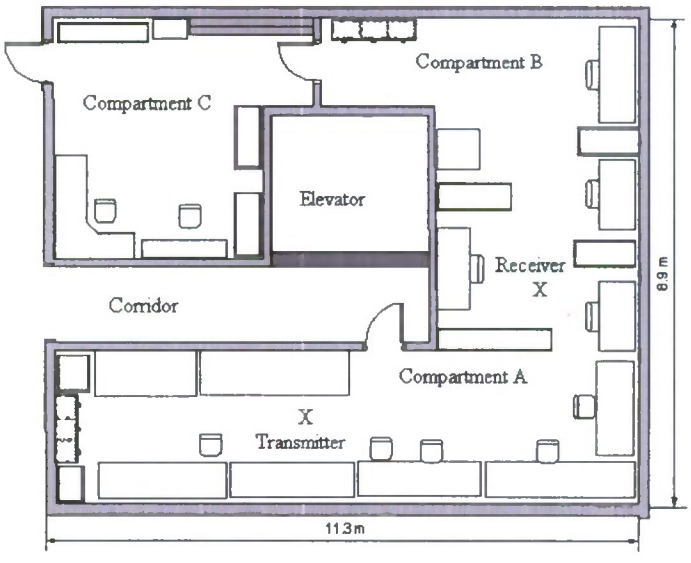

Figure 6.20: Room 400, layout.

Figure 6.21: Baseband time reversal waveform with scrambling.

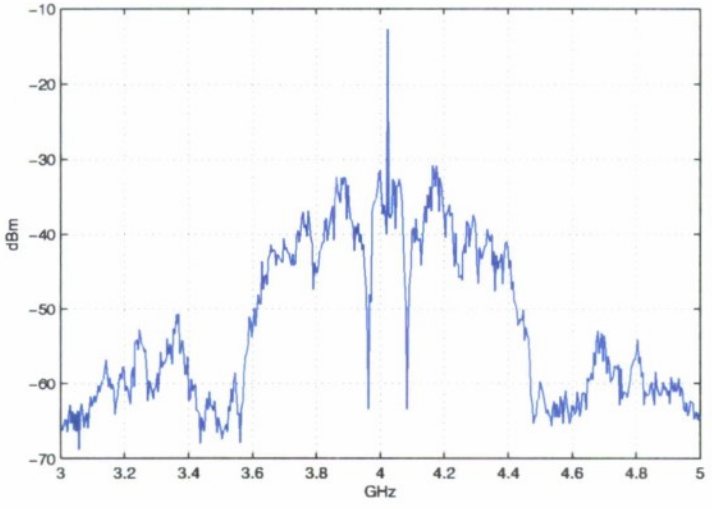

Figure 6.22: Spectrum of time reversal waveform after modulation.

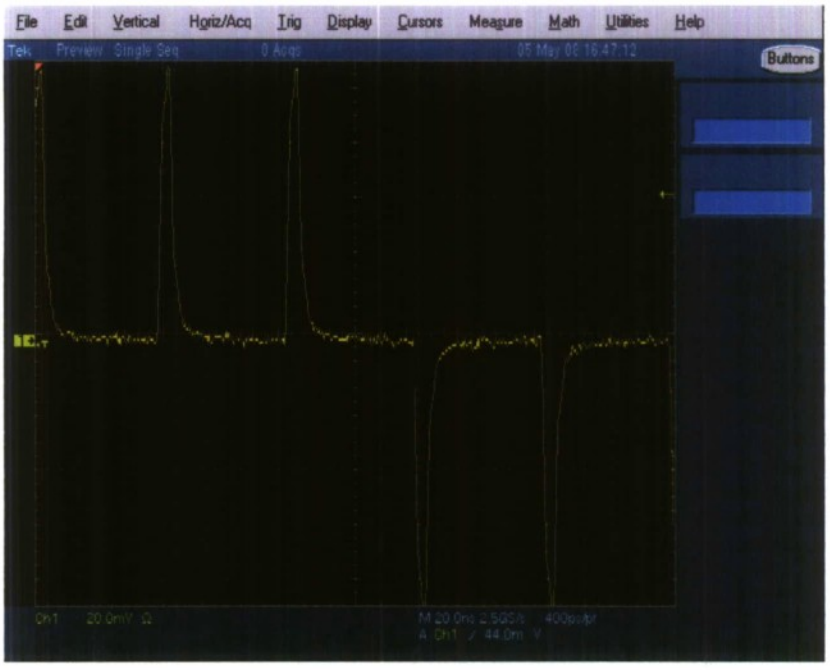

Figure 6.23: Baseband single-pulse waveform with scrambling.

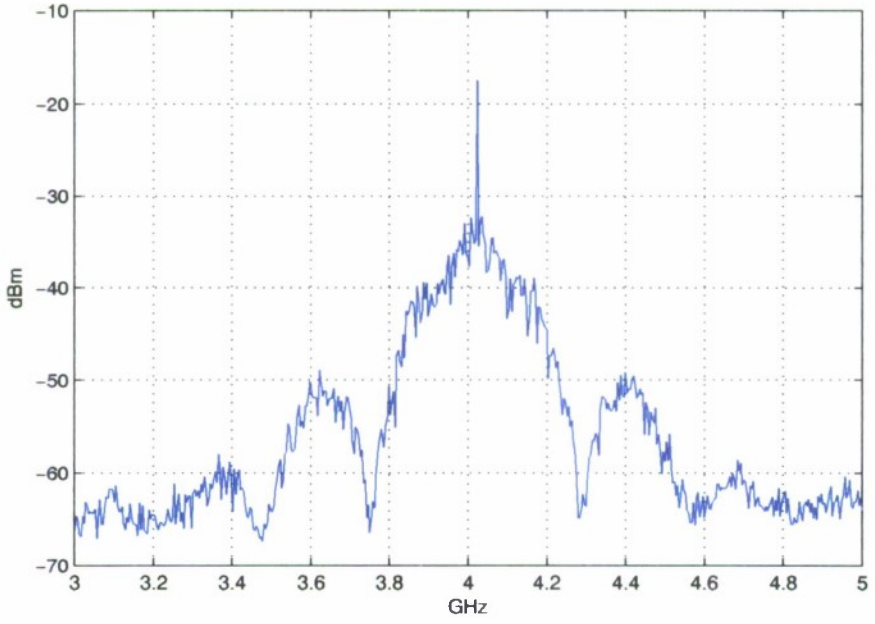

Figure 6.24: Spectrum of single-pulse waveform after modulation.

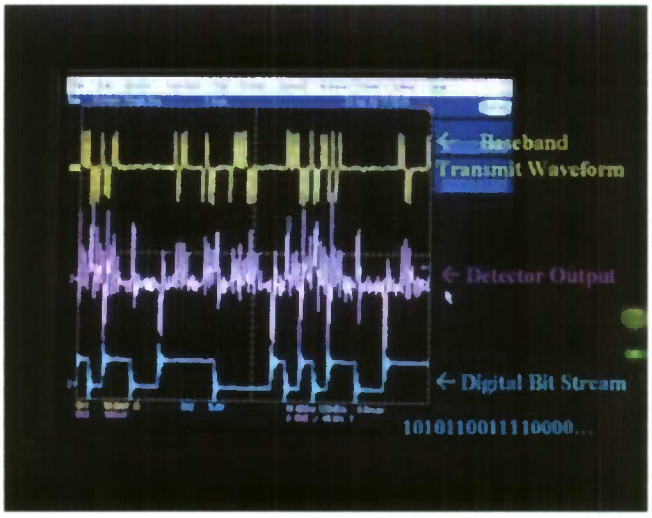

Figure 6.25: Time reversal waveform, system test result.

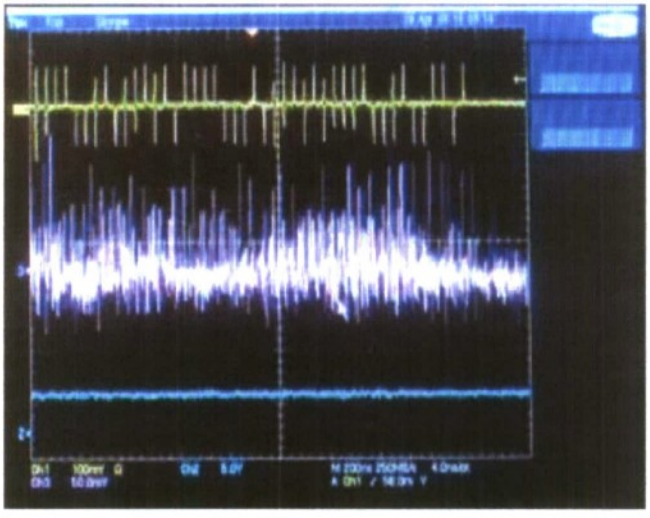

Figure 6.26: Single-pulse waveform, system test result.

Figure 6.27: Time focusing property of time reversal.