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14. ABSTRACT

Although single-electron devices have many advantages over conventional electronic devices and are therefore expected to have important applications for military, space, and commercial use, many fabrication challenges associated with nanoscale geometrical control have limited their implementation for practical use. The aim of this project was to create new single-electron device architecture and its associated fabrication techniques to realize single-electron device fabrication on a large scale, thereby enabling their implementation for practical applications. We demonstrated 1) chip-level fabrication of single-electron transistors, 2) that they can be fabricated in completely parallel processing, with each device individually addressable, 3) clear I-V characteristics of Coulomb blockade/staircase and Coulomb oscillations, and 4) that they can operate at room temperature. These results show that fabrication of integrated systems of room-temperature single-electron devices is now possible, paving a pathway toward practical use of single-electron devices.

15. SUBJECT TERMS

Single-electron transistors, nanoelectronic devices, CMOS-compatible fabrication, room-temperature operation, large-scale fabrication, nanoparticles

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ONR Final Report:

Fabrication of Single Electron Devices within the Framework of CMOS Technology

(Grant No: N00014-05-1-0030)

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I. Introduction and Background

Single-electron devices in which the transport and storage of single electrons are systematically controlled hold great promise for future electronic devices and sensors for military, space, and commercial use. Their advantages over the conventional devices include ultra-low power consumption, scalability to the sub-nanometer regime, and extremely high charge sensitivity. These capabilities can produce a variety of devices that could play critical roles in providing NAVY's technical needs. The devices operating at ultra-low power consumption and with high-packing density could be utilized, for example, for long-endurance UAVs, remote communications, remote monitoring, and devices for missiles, aircrafts, and submarines.

Although the technical merits of single-electron devices are clear, their implementation to practical use has been limited. This is because their fabrication requires nanoscale geometrical arrangement of device components (i.e., source/drain electrodes, and Coulomb islands), which has been difficult to achieve on a large scale, limiting the single-electron device fabrication only a few units at a time. Until now, the nanoscale geometrical control has been carried out using techniques such as e-beam lithography/angle deposition, nanoscale oxidation, electromigration, electrodeposition, and scanning tunneling microscopy. However, these techniques are not suitable for large-scale processing, restricting their implementation in practical devices.

This project aimed to create new single-electron device architecture and its associated processes that would enable single-electron device fabrication in complete parallel processing. CMOS-compatibility in the processes and materials was in the core of this project, which had the single-electron devices defined using photolithography, making each device unit individually addressable and connected to the macroscopic world using usual CMOS interconnection technology. The central goal of this project was to demonstrate that individually addressable single-electron transistors can be fabricated on a large scale and that they operate at room temperature. The success of this project would pave the way toward practical realization of single-electron devices that could support NAVY's critical technology needs as well as commercial electronic devices for everyday use.

II. Summary of Accomplishments

In this project, we created new single-electron device architecture that made large-scale fabrication of single-electron devices possible. Their fabrication processes were developed within the framework of CMOS fabrication technology. We demonstrated the functioning of the fabricated devices by showing the Coulomb blockades, Coulomb staircases, and Coulomb oscillations. These devices were individually addressable and operated at room temperature. These accomplishments are described below in more detail.

II.A. Design of New Single-Electron Device Architecture

Single-electron devices require the arrangement of device components (i.e., Coulomb islands, source, drain, and gate electrodes) on a nanometer scale. Having a device structure that satisfies the nanometer scale geometrical requirements and at the same time enables the fabrication in complete parallel processing over a large area was a key objective for this project. We created a new single-electron device architecture that satisfies these requirements.

Figure 1 shows the schematic of the new single-electron device architecture. There are three key aspects of this architecture that enable large-scale fabrication of single-electron devices. First, separation of the source and drain electrodes is defined by the thickness of the intervening dielectric film. This enables accurate control of source-drain separation because the thickness of the film h can be controlled with sub-nanometer scale precision using film deposition techniques such as plasma-enhanced chemical vapor deposition (PECVD) and atomic-layer deposition (ALD). Second, the drain, dielectric layer, and source (the elevated portion in Fig. 1) are vertically self-aligned. This self-alignment allows the integrity of the source-drain separation to be maintained along the periphery of source/drain electrodes, which is achieved without regards to the shape of the drain electrode. Third, the Coulomb island is positioned on the exposed sidewall of the dielectric layer, which allows taking the lateral dimension L arbitrarily since single-electron transport occurs only in the region at the edge of drain/dielectric/source stack (the region in the dashed box in Fig.1). The liberty of choosing lateral dimension L makes it possible to use photolithography and other associated techniques that are compatible

with current CMOS technology, enabling single-electron device fabrication in complete parallel processing.

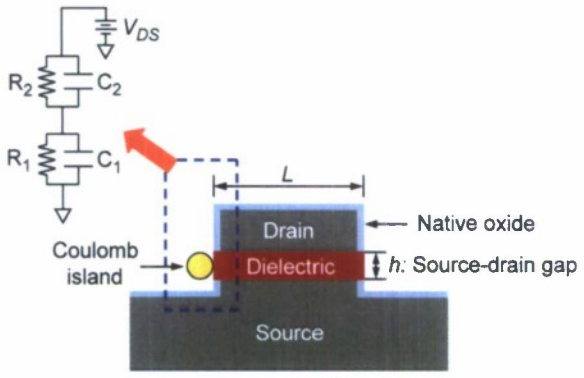

Figure 1. A new architecture for single-electron devices.[1] The source and drain electrodes are vertically separated and self-aligned so that their separation *h* can be precisely defined by controlling the thickness of the inserted dielectric film. The lateral dimension *L* can be arbitrarily chosen since the electron tunneling occurs via the Coulomb island positioned at the sidewall of the exposed dielectric film. Inset: an equivalent circuit for the single-electron transport occurring in the dashed box.

II.B. Establishment of Fabrication Techniques

II.B.1. Key Process Steps

The new single-electron device structure was fabricated based on CMOS fabrication technology. Figure 2 shows the key process steps of our single-electron device fabrication. On silicon substrate, isolation oxide was thermally grown to electrically isolate individual devices from others. Source electrodes were made by depositing Cr film using an e-beam evaporator or thermal evaporator. Then, PECVD silicon oxide (thickness: 10-20 nm) was deposited on top of the source electrode. Drain electrode was defined using photolithography, Cr deposition, and lift-off, Fig. 2(a). Drain/dielectric/source stack was then made using reactive ion etching (RIE) with the drain electrode utilized as a hard mask, therefore leading to the *self-aligned* drain/dielectric/source stack, Fig. 2(b). Nanoparticles (Coulomb islands) were attached on the sidewall of the exposed dielectric film (PECVD silicon oxide) by forming self-assembled monolayers (SAMs) on the substrate, followed by immersion of the wafer into

10- or 20- nm Au colloids, Fig. 2(c). Figure 3 is an SEM image showing nanoparticle attachment on the exposed sidewall of the PECVD oxide layer that was sandwiched between source and drain electrodes.

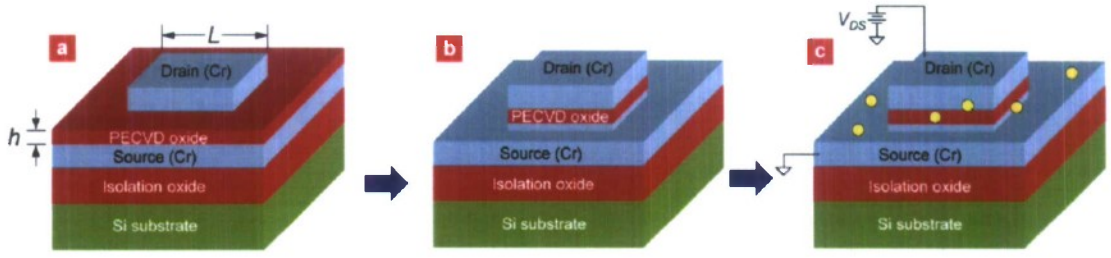

Figure 2. Schematic of the key process steps.[1] (a) Definition of drain electrode using photolithography, Cr deposition, and lift-off. (b) Formation of self-aligned drain/dielectric/source stack using RIE. The drain electrode is used as a hard mask, leading to self-alignment of drain/dielectric/source. (c) Attachment of Coulomb islands (nanoparticles) on the exposed sidewall of PECVD oxide.

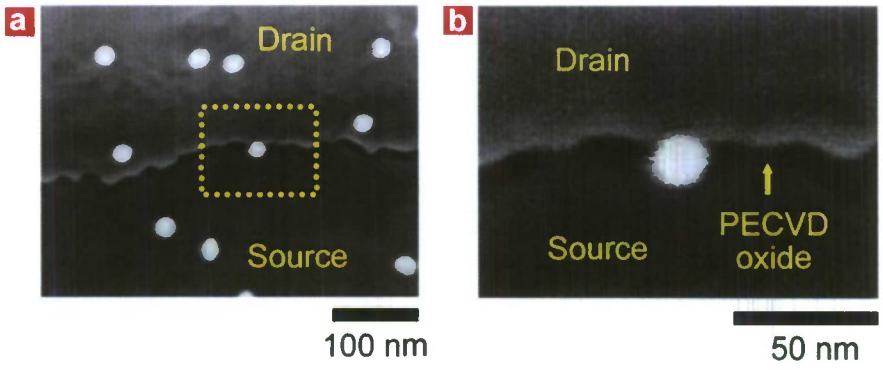

Figure 3. Attachment of Coulomb islands on the PECVD oxide sidewall.[1] (a) The ~20 nm Au nanoparticles (bright dots) are attached on the sidewall of the PECVD oxide layer. The PECVD oxide appears as a dark line between the source and drain electrodes. (b) A magnified image of the dotted box in (a). Due to tilting (30° from vertical) of the SEM sample stage during imaging, the thickness of the PECVD oxide layer appears about two times (1/sin30°) smaller.

Many of the process techniques involved in the fabrication in Fig. 2 were newly developed. For example, the deposition process for PECVD silicon oxide was carefully designed to obtain supreme quality of the dielectric layer; the breakdown electric field of our PECVD silicon oxide is ~3 MV/cm, very close to that of a thermally grown silicon dioxide, ~5 MV/cm. Another example is the development of nanoparticle attachment techniques. This involved developing a procedure for formation of SAMs, attraction of charged nanoparticles onto the SAMs, and removal of the SAMs molecules by UV ozone after nanoparticle attachment.

Materials in our single-electron devices were also carefully chosen. For example, we used Cr as source and drain electrodes because Cr forms native oxide and importantly the tunneling resistance of the chromium native oxide is very low (barrier height of chromium oxide (0.06 eV) is ~30 times lower than that of aluminum oxide (1.6-2.5 eV)). The low tunneling barrier of chromium oxide allowed larger separation between the Coulomb island and source/drain electrodes, therefore reduced junction capacitances, making room-temperature operation possible.

II.B.2. Process Flow for Fabrication of Single-Electron Devices

We accomplished chip-level fabrication of single-electron devices that operate at room temperature. Figure 4 shows the process flow for two-terminal single-electron devices. We employed four photomask steps to simultaneously fabricate a large number of single-electron devices on a silicon wafer. In the first photomask step, the source electrodes were defined on top of the isolation oxide, Fig. 4(a) (only one device unit is displayed for clarity). In the second mask step, Fig. 4(b), each single-electron device structure was constructed on top of every source electrode using the procedure described in Fig. 2. In the third mask step, Fig. 4(c), the wafer was passivated with silicon dioxide, followed by making vias for each device unit. In the fourth mask step, Fig. 4(d), bond pads were defined using photolithography, followed by Au deposition and lift-off, which connected the bond pads to the source/drain electrodes through vias. Figure 4(e) shows a photograph of an actual fabricated chip mounted on a chip carrier.

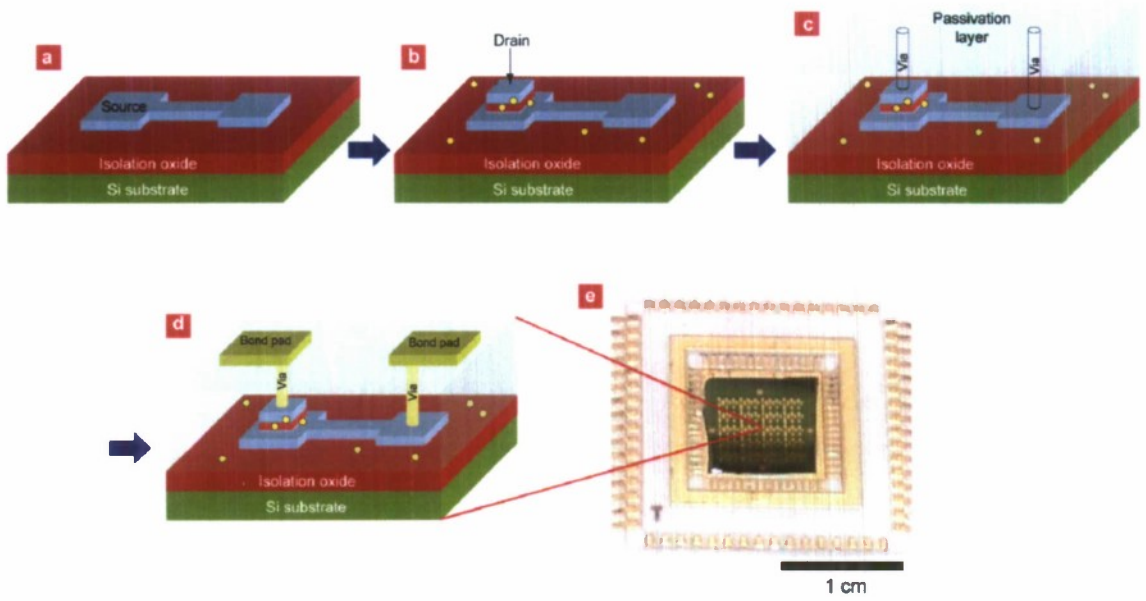

Figure 4. Process Flow.[1] (Only one device unit is displayed for clarity; schematic is not to scale.) (a) First mask step: the source electrodes (Cr) were made on top of the isolation oxide using photolithography, Cr deposition, and lift-off. (b) Second mask step: using the second photomask and using the procedure shown in Fig. 2, each single-electron device was fabricated on top of every source electrode. (c) Third mask step: the wafer was passivated by silicon dioxide, followed by formation of vias using photolithography (third photomask) and RIE of the passivation layer. (d) Fourth mask step: defining the bond pads using photolithography (fourth photomask), followed by deposition of Au and lift-off, leading to electrical connection between source/drain electrodes and bond pads. (e) A photograph of a fabricated chip mounted on a chip carrier.

Importantly, we also fabricated single-electron transistors by adding gate electrodes to our single-electron device architecture. This was done by adding gate electrodes that encompass PECVD oxide sidewall, Fig. 5. This was carried out by inserting additional mask step before making vias and bond pads. The gate electrodes were created using photolithography and other CMOS-compatible processes, and every gate was individually addressable.

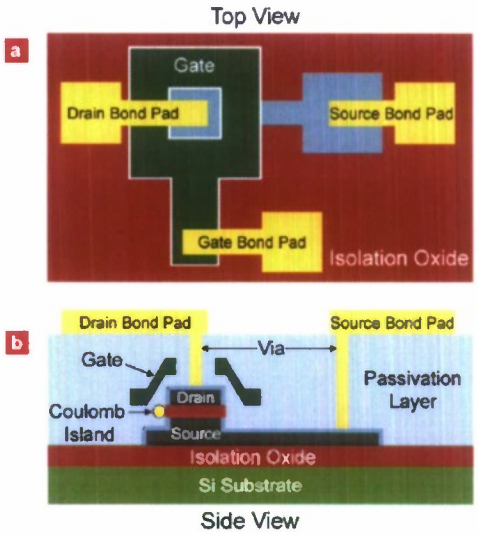

Figure 5. Schematic of single-electron transistor.[1] (Only one device unit is displayed for clarity; schematic is not to scale.) Individually addressable gate electrodes were created using photolithography, surrounding PECVD oxide sidewall. (a) Top view. (b) Side view.

II.C. Demonstration of the Functioning of Single-Electron Devices

We show the functioning of our single-electron devices by demonstrating Coulomb blockades, Coulomb staircases, and Coulomb oscillations. Importantly, we demonstrate that the new single-electron devices operate at room-temperature, a critical requirement for practical implementation of single-electron devices.

II.C.1. Demonstration of Coulomb Staircases

A definitive proof for the single-electron tunneling in the fabricated devices is the Coulomb staircase, where each step corresponds to addition/subtraction of a single electron into/from the Coulomb island. Figure 6(a) and 6(b) demonstrate clear Coulomb staircases for fabricated devices whose Coulomb islands were ~10 nm and ~20nm Au nanoparticles, respectively. Figure 6(a) displays Coulomb staircases at room temperature. The voltage intervals between the adjacent arrows are very periodic (arrows indicate the points where the current changes abruptly). The high degree of periodicity can be seen more clearly from the high linearity of the arrow positions displayed in the inset of Fig. 6(a). The voltage interval ΔV_{DS} is measured to be 46±3 mV. The energy required to

add/subtract one electron to/from the Coulomb island is therefore ~50 meV (~$e\Delta V_{DS}$), which is about two times larger than the room-temperature thermal energy, ~25 meV.

Figure 6(b) shows another example of the Coulomb staircase, which was measured from a chip fabricated using ~20 nm Au colloid. The voltage interval ΔV_{DS} of the staircase is very periodic, as evidenced by the high linearity of the arrow positions, inset of Fig. 6(b). The voltage interval ΔV_{DS} is measured to be 20±2 mV, about two times lower than that for devices made with ~10 nm Au nanoparticles, 46±3 mV (Fig. 6(a)). This inverse proportionality of the voltage interval with Coulomb island size is in agreement with the linear dependence of the self-capacitances of Coulomb islands with their diameters.

We also calculated the I-V characteristics of the Coulomb staircase using the orthodox theory of single-electron tunneling. The red line in Fig. 6(b) displays the simulated I-V characteristics, which is in very good agreement with the experimental data.

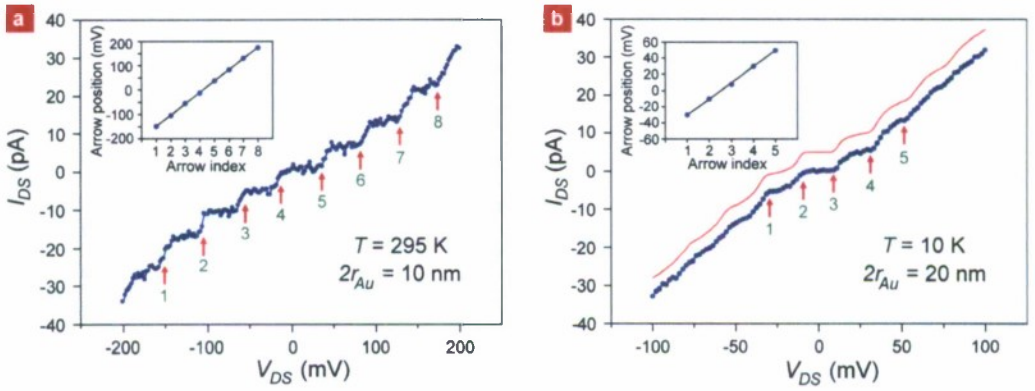

Figure 6. I-V characteristics demonstrating Coulomb staircase behavior.[1] (a) A Coulomb staircase measured at room temperature, from a chip fabricated using ~10 nm Au colloid. Each arrow indicates the point where the current changes abruptly. (b) A Coulomb staircase measured at 10K, from a chip fabricated using ~20 nm Au colloid. The blue dots: measured data; the red line: I-V characteristics calculated using orthodox theory for the equivalent circuit in Fig. 1. The simulated I-V is shifted vertically by 5 pA for clarity. The simulation parameters: C_1 = 7.30 aF, C_2 = 0.88 aF, R_1 = 2.05 GΩ, R_2 = 0.40 GΩ, and Q_0 (background charge) = 0.05e.

II.C.2. Demonstration of Coulomb Blockades

The Coulomb staircases demonstrated above were observed for asymmetric tunneling junctions ($R_1C_1 >> R_2C_2$). We also demonstrated Coulomb blockade without Coulomb staircase for symmetric junctions ($R_1C_1 \approx R_2C_2$). Figure 7(a) displays Coulomb blockade at temperatures ranging from 10K to 315K. The Coulomb blockade is clearly seen at 10K, and with thermal smearing out, up to room temperature. This measured Coulomb blockade is in good agreement with the simulation obtained using the orthodox theory, Fig. 7(b).

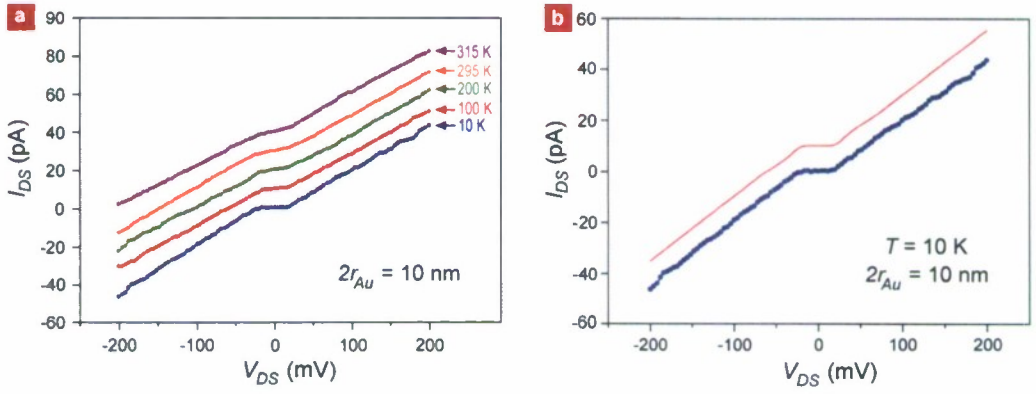

Figure 7. I-V characteristics of Coulomb blockade behavior.[1] (a) Demonstration of Coulomb blockade at different temperatures, 10K-315K, from a chip fabricated using ~10 nm Au colloid. (b) Comparison of measured Coulomb blockade I-V characteristics (blue dots) with simulated I-V (red line). The simulated I-V is shifted vertically by 10 pA for clarity. The simulation parameters: $C_1 = 3.5$ aF, $C_2 = 3.4$ aF, $R_1 = 1.8$ GΩ, $R_2 = 2.1$ GΩ, and $Q_0 = 0.07e$.

II.C.3. Demonstration of Coulomb Oscillations

We also demonstrated the functioning of fabricated single-electron transistors by demonstrating the Coulomb oscillations, i.e., the periodic modulations of source-drain current I_{DS} as a function of gate voltage V_G. This was demonstrated at room temperature (red dots) as well as at 10K (blue dots), Fig. 8. The Coulomb peaks were very periodic, with $\Delta V_G = 205$ mV, which corresponds to a gate capacitance C_G of ~0.78 aF.

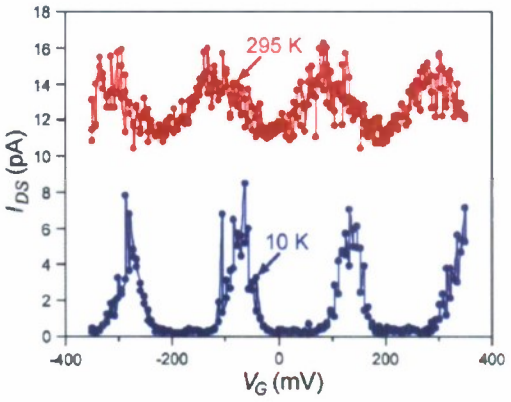

Figure 8. Demonstration of Coulomb oscillations.[1] From a chip fabricated using ~10 nm Au colloid. V_{DS} = 10 mV.

We also demonstrated the gate effect in the functioning of the fabricated single-electron transistors by observing the Coulomb staircase behaviors at different gate biases. Figure 9(a) displays a clear change of Coulomb staircase characteristics when the gate voltage V_G was applied (blue dots: V_G = 0V; red dots: V_G = 0.25V). These behaviors were also in excellent agreement with the simulations, which are shown in Fig. 9(b) and 9(c).

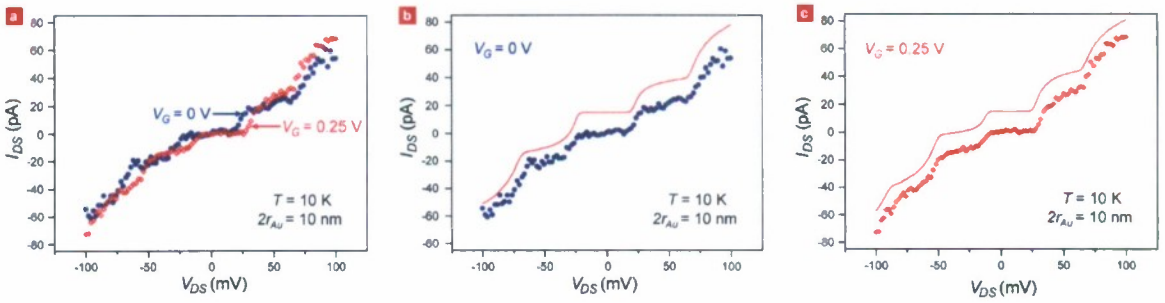

Figure 9. Effect of gate bias in the single-electron transistor.[1] From a chip fabricated using ~10 nm Au colloid. (a) The change of Coulomb staircase characteristics with gate bias is shown. Blue dots: V_G = 0V; Red dots: V_G = 0.25V. (b) Comparison of measurement with simulation for V_G = 0V. The simulation parameters: V_G = 0V, C_1 = 3.4 aF, C_2 = 0.24 aF, C_G = 0.78 aF, R_1 = 0.79 GΩ, R_2 = 0.19 GΩ, and Q_0 = 0.05e. (C) Comparison of measurement with simulation for V_G = 0.25V. The simulation parameters: V_G = 0.25V, C_1 = 3.4 aF, C_2 = 0.24 aF, C_G = 0.78 aF, R_1 = 0.79 GΩ, R_2 = 0.19 GΩ, and Q_0 = 0.05e.

II.C.4. Device to Device Variations

Our approach made it possible to fabricate single-electron transistors in large numbers in parallel processing. It would be interesting and important to see how much variations in the device characteristics exist among those devices. Figure 10 displays the interval of the Coulomb peaks ΔV_G (the periodicity of the Coulomb oscillations) from ten different device units, measured at room temperature. The standard variation of ΔV_G is only ~10% (17 mV) of the average value (183 mV). We expect that optimizations of the fabrication processes should reduce the scatter even further.

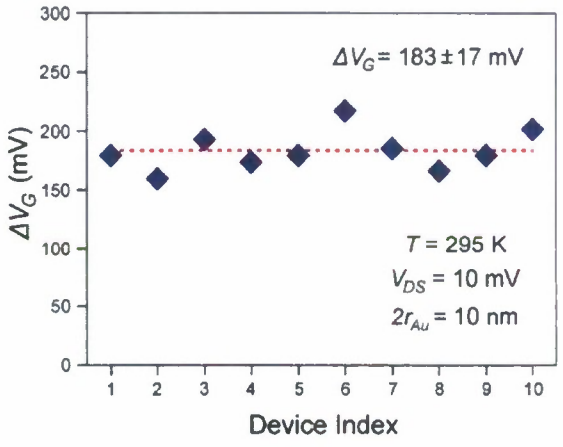

Figure 10. Device to device variations for Coulomb interval ΔV_G.[1] Measured at room temperature, from ten different device units. The measured ΔV_G is 183 ± 17 mV; the standard deviation corresponds to only ~10% of the average. The red dotted line indicates the average value of ΔV_G, 183 mV.

II.D. Controlled Placement of Coulomb Islands

In the single-electron device fabrication described above, attachment of nanoparticles on the PECVD oxide sidewall was carried out randomly. Although this simplified the device fabrication and was sufficient to demonstrate parallel fabrication of arrays of room-temperature single-electron transistors, it produced a success rate (criteria: Coulomb oscillations at room temperature) of only about 1%. To control the placement of nanoparticles (Coulomb islands) with nanoscale precision, we developed new concepts for placing nanoparticles and demonstrated their effectiveness on nanoparticle placement on a large scale. Below we describe the major outcomes of these approaches.

II.D.1. Electrostatic Funneling

In our new approach named "Electrostatic Funneling", charged nanoparticles in a colloid are guided by an electrostatic energy gradient and placed on targeted locations with nanoscale precision. Figure 11(a) and 11(b) show the concept of the electrostatic funneling with a one-dimension guiding structure as an example. Here a surface pattern of alternating lines is functionalized with positively and negatively charged self-assembled monolayers (SAMs). When immersed into a Au colloid (Au nanoparticles: negatively charged), the electrostatic interaction between the substrate and nanoparticles results in the interaction free energy shown in Fig. 11(a). The nanoparticles are guided along the free energy gradient onto a low-energy site, a center of a positively charged line, Fig. 11(a) and (b).

The important benefits of this approach are 1) the dimension of the guiding structure (such as the width "W" in Fig. 11(a) and (b)) is on the order of 100 nm, so that they can be defined on a wafer scale, using photolithography and other CMOS-compatible processes, and 2) at the same time, nanometer-scale placement precision can be achieved since the nanoparticles are guided (funneled) onto low energy positions. The above two allow large-scale nanoparticle placement with nanoscale precision.

We demonstrated the concept of the electrostatic funneling using ~20 nm Au nanoparticles and one-dimensional guiding structure with line width of ~100 nm. Figure 11(c) is an SEM image demonstrating the effectiveness of the electrostatic funneling concept. The placement precision (the average deviation of the nanoparticles from the

center of the line) was measured to be ~6 nm. Importantly, this precision placement was carried out over the entire wafer piece in parallel processing.

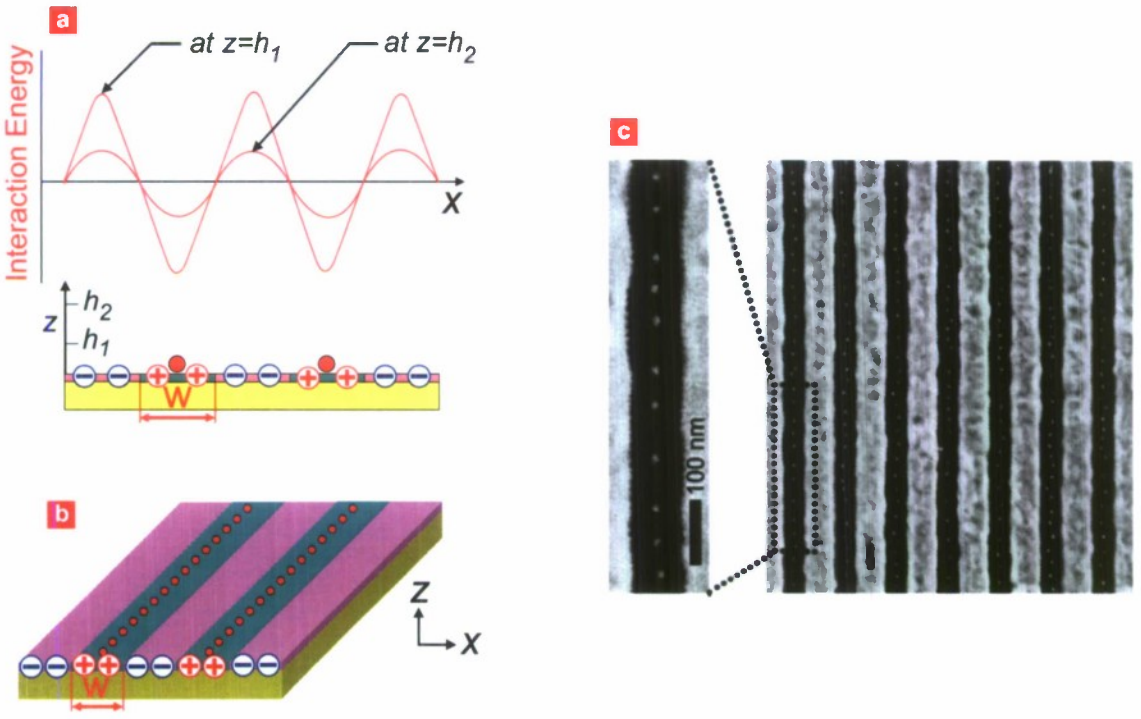

Figure 11. "Electrostatic Funneling" for precise nanoparticle placement on a large scale.[2] (a)-(b) The schematic of the electrostatic funneling concept. (c) An SEM image demonstrating the effectiveness of the electrostatic funneling concept. Bright dots: ~20 nm Au nanoparticles. The placement precision was measured to be ~6 nm.

II.D.2. Nanoparticle Placement in the New Single-Electron Device Structure

The electrostatic funneling method does not need to be restricted to planar geometries, but can be applied to any geometry as long as an appropriate electrostatic funneling structure can be formed. As a first step to utilize the electrostatic funneling for precise placement of Coulomb islands for our single-electron device structure, we demonstrated the controlled placement of nanoparticles on the exposed sidewalls of silicon oxide having varying thicknesses, Fig. 12. Figure 12(b)-(d) are SEM images demonstrating placement of nanoparticles with size of ~200, ~80, and ~50 nm,

respectively. We note that the nanoparticles were placed along the *centers* of the exposed oxide sidewalls via electrostatic funneling.

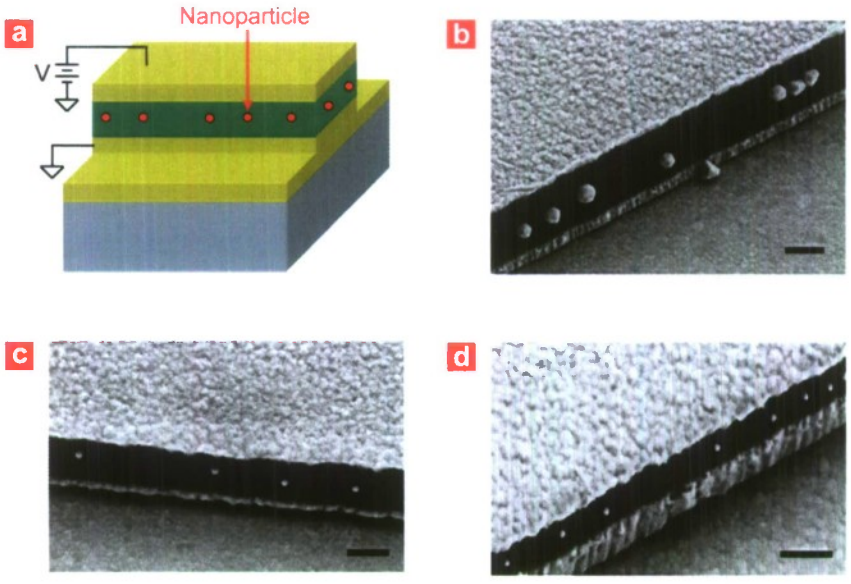

Figure 12. Controlled nanoparticle placement on the exposed oxide sidewall.[2] (a) Schematic of the sample geometry. (b)-(d) SEM images demonstrating controlled nanoparticle placement on the exposed oxide sidewalls. The diameter of Au nanoparticles was ~200, ~80, and ~50 nm for (b), (c), and (d), respectively. Scale bars: 400 nm.

II.D.3. Single-Particle Placement

The ultimate control in the placement of nanoparticles would be the capability of manipulating and positioning them at the single-nanoparticle level, i.e., assigning just one single-nanoparticle to a specific substrate position. We developed such technique, named "Single-Particle Placement (SPP)", in which exactly one nanoparticle is electrostatically guided and placed onto each target location in a self-limiting way. Figure 13(a)-(b) illustrate the concept of SPP. First, the substrate surface is functionalized with positively and negatively charged SAMs that form an electrostatic guiding structure, the electrostatic funnel. When immersed in a nanoparticle colloid, a nanoparticle is guided and placed at a target position, the circle center in Fig. 13(a). Once a nanoparticle occupies the circle, it alters the electrostatic potential landscape in such a way that the approach of other nanoparticles to the substrate surface is prohibited, resulting in self-limiting SPP, Fig. 13(b). Figure 14 demonstrates the effectiveness of SPP. Out of 100 circles, 97 circles contained exactly one Au nanoparticle. This single-particle level placement may play an effective role for the fabrication of single-electron devices and many other nanoscale devices and sensors.

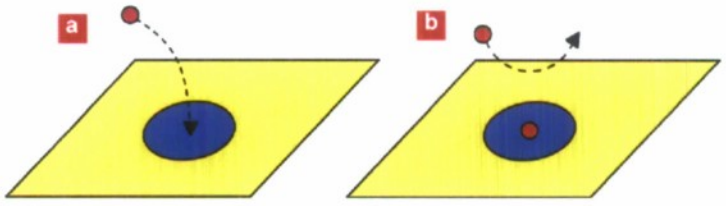

Figure 13. Single-particle placement (SPP).[3] (a) A nanoparticle in a colloid is electrostatically guided onto a circle center. (b) Once a nanoparticle occupies a circle, the approach of other nanoparticles is prohibited. Inside the circle: positively charged; outside the circle: negatively charged; and nanoparticle: negatively charged.

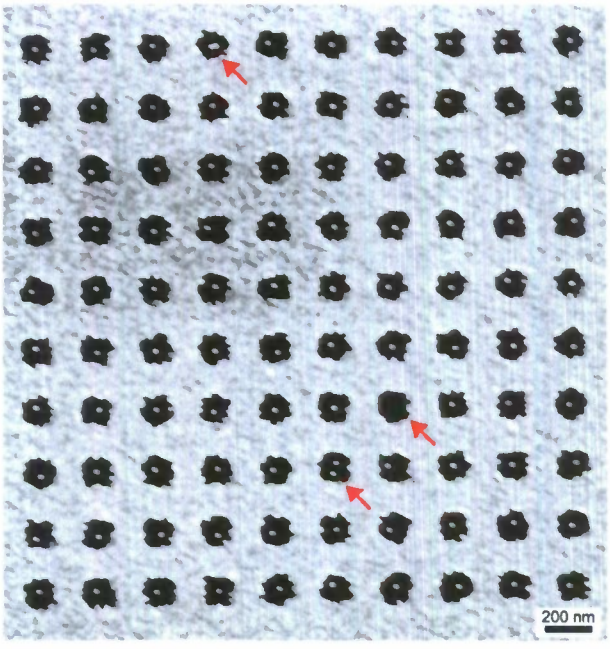

Figure 14. SEM image demonstration the SPP.[3] Bright dots: ~20 nm Au nanoparticles; dark circular patterns: silicon oxide; bright area: Au surface. The arrows indicate the defects.

II.E. Impact and Future Work

This project accomplished the following:

- Demonstrated that single-electron devices can be fabricated on a large scale in complete parallel processing.
- Each device unit can be individually addressed.
- Demonstrated the functioning of the fabricated single-electron devices; clear Coulomb blockades, Coulomb staircases, and Coulomb oscillations.
- The devices operate at room temperature.

The above results indicate that we have made an important step toward practical fabrication of room-temperature single-electron devices for everyday use. The CMOS-compatible fabrication procedure promises realization of integrated systems of single-electron devices or hybrid systems composed of single-electron devices and CMOS devices. These capabilities have established firm technical foundations for fabricating integrated single-electron memory systems as well as single-electron logics, which we will pursue for years to come. The other important step we are going to make is to

implement the controlled nanoparticle placement techniques (section II.D.) into our single-electron device fabrication. This will make sure that the nanoparticles are selectively and accurately positioned on the exposed sidewall, appreciably increasing the yield for the single-electron device fabrication.

References

1. Ray, V., Subramanian, R., Bhadrachalam, P., Ma, L. C., Kim, C. U. & Koh, S. J. CMOS-compatible fabrication of room-temperature single-electron devices. *Nat. Nanotechnol.* 3, 603-608 (2008).
2. Ma, L.-C., Subramanian, R., Huang, H.-W., Ray, V., Kim, C.-U. & Koh, S. J. Electrostatic funneling for precise nanoparticle placement: A route to wafer-scale integration. *Nano Lett.* 7, 439-445 (2007).
3. Huang, H. W., Bhadrachalam, P., Ray, V. & Koh, S. J. Single-particle placement via self-limiting electrostatic gating. *Appl. Phys. Lett.* 93, 073110 (2008).

III. Publications/Presentations/Awards

III.A. Publications/Patent

1. V. Ray, R. Subramanian, P. Bhadrachalam, L.-C. Ma, C.-U. Kim, and S.J. Koh, "CMOS-compatible fabrication of room-temperature single-electron devices", *Nature Nanotechnology*, Vol. 3, p.603-608, 2008 (**Highlighted by MRS in MRS home page, MRS *Materials News*, MRS *Materials360*; Highlighted on *NSF News*; Highlighted by *NanotechWeb, Nanowerk, TRN, AZ nanotechnology, Betterhumans, World Gold Council, SILObreaker, EDN, High Technology Exchange***)
2. H.-W. Huang, P. Bhadrachalam, V. Ray, and S.J. Koh, "Single-particle placement via self-limiting electrostatic gating", *Applied Physics Letters*, Vol. 93, p.073110, 2008 (**Highlighted by MRS in *Materials360;* August 2008**)
3. **(Invited)** S.J. Koh, "Strategies for Controlled Placement of Nanoscale Building Blocks", *Nanoscale Research Letters*, Vol. 2, p.519-545, 2007
4. **(Invited)** S.J. Koh, "Controlled Placement of Nanoscale Building Blocks: Toward Large-Scale Fabrication of Nanoscale Devices", *JOM*, Vol. 59, p.22-28, 2007
5. L.-C. Ma, R. Subramanian, H.-W. Huang, V. Ray, C.-U. Kim, and S.J. Koh, "Electrostatic Funneling for Precise Nanoparticle Placement: A Route to Wafer-Scale Integration ", *Nano Letters*, Vol. 7, p.439-445, 2007 (**Highlighted by MRS in *eMatters;* January 2007**)
6. S.J. Koh, C.-U. Kim, L.-C. Ma, R. Subramanian, "Positioning of Nanoparticles and Fabrication of Single Electron Devices", U.S. Patent #: US7465953B1, 12/16/2008

III.B. Presentations

1. **(Invited)** S.J. Koh, "Large-scale fabrication of single electron devices utilizing colloidal nanoparticles", Particles 2008, Orlando, Florida, May 2008
2. V. Ray, R. Subramanian, P. Bhadrachalam, S.J. Koh, "CMOS based fabrication of single electron devices on a large scale", 2008 APS March Meeting, New Orleans, Louisiana, March 2008
3. H.-W. Huang, V. Ray, S.J. Koh, "Large-Scale Placement of Single Nanoparticles with Nanoscale Precision", TMS Annual Meeting, New Orleans, Louisiana, March 2008 (**1st place for the Best Student Paper Award in Nanomaterials, TMS2008)**
4. V. Ray, R. Subramanian, P. Bhadrachalam, S.J. Koh, "Large-Scale Fabrication of Single Electron Devices", TMS Annual Meeting, New Orleans, Louisiana, March 2008 (**1st place for the Best Student Paper Award in Nanomaterials, TMS2008)**
5. S.J. Koh, "Controlled Placement of Nanoparticles for Integrated Systems of Nanoscale Devices and Sensors", PRICM-6, Jeju, Korea, November 2007
6. **(Invited)** S.J. Koh, "Large-Scale and Precise Nanoparticle Placement via Electrostatic Funneling", Particles 2007, Toronto, Ontario, Canada, August 2007
7. V. Ray, H.-W. Huang, R. Subramanian, L.-C. Ma, C.-U. Kim, S.J. Koh, "Precise Nanoparticle Placement via Electrostatic Funneling", Materials Research Society Spring Meeting, San Francisco, California, April 2007
8. **(Invited)** S.J. Koh, "Electrostatic Funneling Scheme for Wafer-Scale Fabrication of Nanoscale Devices", TMS Annual Meeting, Orlando, Florida, February 2007
9. S.J. Koh, "From Adatom Interactions to the Manipulation of Atom Clusters", Gert Ehrlich Symposium on Surface Science, Urbana, Illinois, May 2006
10. L.-C. Ma, R. Subramanian, H.-W. Huang, V. Ray, N. Basit, C.-U. Kim, S.J. Koh, "Wafer-Level Positioning of Nanoparticles using CMOS Technology and Wet Chemistry", Materials Research Society Spring Meeting, San Francisco, California, April 2006
11. **(Invited)** S.J. Koh, "Controlled Positioning of Nanoparticles in a Wafer-Level", TMS Annual Meeting, San Antonio, Texas, March 2006
12. L.-C. Ma, R. Subramanian, H.-W. Huang, V. Ray, C.-U. Kim, S.J. Koh, "Fabrication of One-Dimensional Assemblies of Nanoparticles in a Wafer Scale", JSPS-UNT Joint

Symposium On Nanoscale Materials For Optoelectronics and Biotechnology, University of North Texas, Denton, Texas, February 2006

III.C. Awards

1. Seong Jin Koh: National Science Foundation CAREER Award (2005)
2. Vishva Ray (the PI's graduate student): 1st place for the Best Student Paper Award in Nanomaterials, TMS 2008 International Conference, New Orleans, Louisiana, March 2008
3. Hong-Wen Huang (the PI's graduate student): 1st place for the Best Student Paper Award in Nanomaterials, TMS 2008 International Conference, New Orleans, Louisiana, March 2008