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Attorney Docket No. 79479

FIELD PROGRAMMABLE GATE ARRAY BASED GLOBAL COMMUNICATION CHANNEL FOR DIGITAL SIGNAL PROCESSOR CHIPS

STATEMENT OF GOVERNMENT INTEREST

BACKGROUND OF THE PRESENT INVENTION

(1) Field of the Invention

The present invention relates to a method for networking, and a network of, digital signal processors via at least one field programmable gate array.

(2) Description of the Prior Art

With reference to FIG. 1, there is illustrated a typical network of digital signal processors (DSP) known in the art whereby a host DSP 11 is configured and programmed to globally broadcast data to a multitude of non-host DSPs 15. Each non-host DSP 15 is linked to the host DSP 11 by a connection between at least one communication port 17 located on the host DSP 11 and at least one communication port 17 on each non-host DSP 15. Typically, such lines of communication are bidirectional. Connecting a host DSP 11 to a multitude of non-host DSPs 15 in the manner illustrated often times requires a complex and costly

patchwork of cables and connectors. Quite often, the data to be transmitted from the host DSP 11 to each of the plurality of non-host DSPs 15 is identical. In order to receive the data broadcast from the host DSP 11, each non-host DSP 15 must be physically connected via its communication port or ports 17 to a communication port or ports 17 on the host DSP 11. This requirement reduces the number of non-host DSPs 15 which may receive the data from the host DSP 11 to a number no greater than the number of communication port 17 located on the host DSP 11. In addition to this restrictive requirement, the software which is executed by the host DSP 11 in order to broadcast data to each of the non-host DSPs 15 must be executed for each non-host DSP 15 connected to host DSP 11. This requirement mandates the repetitive execution of software which is identical for each non-host DSP 15 receiving the data communicated by host DSP 11.

What is therefore needed is a method of networking a host DSP 11 with a plurality of non-host DSPs 15 which is neither limited by the number of communication ports 17 located on the host DSP 11, nor requiring the identical, repetitive execution of software running on the host DSP 11.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a method for networking, and a network of, digital signal processors (DSP) via at least one field programmable gate array so as to enable the simultaneous broadcast of data from a DSP to a plurality of DSPs.

In accordance with the present invention, an apparatus comprising a host digital signal processor (DSP), at least one field programmable gate array (FPGA) in communication with the host DSP for receiving a digital signal from the host DSP, and at least one non-host DSP in communication with the at least one FPGA for receiving the digital signal.

In further accordance with the present invention, a method for connecting digital signal processors comprises the steps of providing a host digital signal processor (DSP), providing at least one field programmable gate array (FPGA) in communication with the host DSP for receiving a digital signal from the host DSP, and providing at least one non-host DSP in communication with the at least one FPGA for receiving the digital signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram of a network of digital signal processors (DSPs) known in the art;

FIG. 2 is a diagram of a network of a host DSP in communication with a plurality of non-host DSPs via a field programmable gate array (FPGA) according to the present invention; and

FIG. 3 is a diagram of an embodiment of the present invention incorporating a plurality of slave/host DSPs.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

It is therefore an aspect of the present invention to provide a method for configuring a host digital signal processor

(DSP) 11 in communication with a plurality of non-host DSPs 15 wherein the number of non-host DSPs 15 receiving data broadcast from the host DSP 11 may be greater than the number of communication ports 17 located upon host DSP 11. Furthermore, the method of the present invention does not require each non-host DSP 15 to be physically connected to host DSP 11. This is achieved by interposing a field programmable gate array (FPGA) between the host DSP 11 and the non-host DSPs 15. The FPGA 13 serves to receive the broadcast data from the host DSP 11, to buffer the data so received, and to handle the communication and dissemination of the buffered broadcast data to a plurality of non-host DSPs 15. In a preferred embodiment, host DSP 11 is located within a host computer 33, preferably an IBM PC compatible computer.

With reference to FIG. 2, there is illustrated in detail a preferred embodiment of the present invention. Host DSP 11 is in communication with FPGA 13 via connection 19 which connects a communication port 17 located on host DSP 11 to a communication port 17 located on FPGA 13. Connection 19 therefore provides bidirectional communication between host DSP 11 and FPGA 13. FPGA 13 has a plurality of additional communication ports 17 which are utilized to communicate with a multitude of additional non-host DSPs 15. FPGA 13 communicates with each non-host DSP 15 via a connection 19 which connects a single communication port 17 located on FPGA 13 to a single communication port 17 located on a non-host DSP 15. In this manner, bidirectional communication is enabled between each non-host DSP 15 and the FPGA 13.

In operation, host DSP 11 communicates a single stream of data to FPGA 13 via a connection 19. It is a property of FPGAs that they may be dynamically programmed to execute software instructions. FPGA 13 is therefore programmed to buffer the stream of data received by the host DSP 11 and to transmit the received and buffered data out via the plurality of communication ports 17 in communication with non-host DSPs 15. In addition to transmitting the buffered data, the FPGA 13 is preferably programmed to perform any and all initialization and data synchronization activities required to facilitate the communication of buffered data between the FPGA 13 and each and every non-host DSP 15. Such communication may be either synchronous or asynchronous. FPGA 13 is preferably constructed so as to comprise an internal memory capable of storing, retrieving, and returning upon request, digital data.

In an alternative embodiment of the present invention, FPGA 13 may be in communication with an external storage device 21 wherein the data broadcast by host DSP 11 to FPGA 13 may be buffered and stored in external storage device 21, and retrieved by FPGA 13 as required for broadcast to the non-host DSPs 15. External storage device 21 may be any device known in the art capable of storing and retrieving digital data. In addition to communicating with non-host DSPs 15, FPGA 13 may similarly communicate with a peripheral device 23 via a communication port 17 located upon FPGA 13 and connected to the peripheral device 23 by a connection 19.

With reference to FIG. 3, there is illustrated an

alternative embodiment of the present invention. As noted above with reference to FIG. 2, non-host DSPs 15 receive data broadcast by host DSP 11 via FPGA 13. In such a configuration, non-host DSPs 15 are referred to as operating in a "slave" modality with respect to the operation of the host DSP 11. However, it is certainly possible that one or more non-host DSPs 15 may, in turn, act as a host DSP to one or more external devices. As illustrated in FIG. 3, slave/host DSPs 31, 31' operate in such a manner. There need be no physical difference between the composition of slave/host DSPs 31, 31' and non-host DSPs 15 as previously described. Rather, the designation of slave/host DSPs 31 by a unique reference number serve merely to differentiate the operative roll of slave/host DSPs 31 as opposed to that of non-host DSPs 15. Slave/host DSP 31 is connected via a connection 19 to a non-host DSP 15. Likewise, slave/host DSP 31' is connected to an FPGA 13 via a connection 19 extending between a communication port 17 located on slave/host DSP 31 and a communication port 17 located on FPGA 13. It is evident that, in this manner, the status of each non-host DSP 15 receiving data broadcast from a host DSP 11 may be altered to that of a host DSP 11 thus earning the designation slave/host DSP 31.

It is apparent that there has been provided in accordance with the present invention a field programmable gate array based global communication channel for digital signal processor chips which fully satisfies the objects, means, and advantages set forth hereinbefore. While the present invention has been described in the context of specific embodiments thereof, other

alternatives, modifications, and variations will become apparent to those skilled in the art having read the foregoing description. Accordingly, it is intended to embrace those alternatives, modifications, and variations as fall within the broad scope of the appended claims.

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ABSTRACT OF THE DISCLOSURE

An apparatus comprising a host digital signal processor (DSP), at least one field programmable gate array (FPGA) in communication with the host DSP for receiving a digital signal from the host DSP, and at least one non-host DSP in communication with the at least one FPGA for receiving the digital signal.

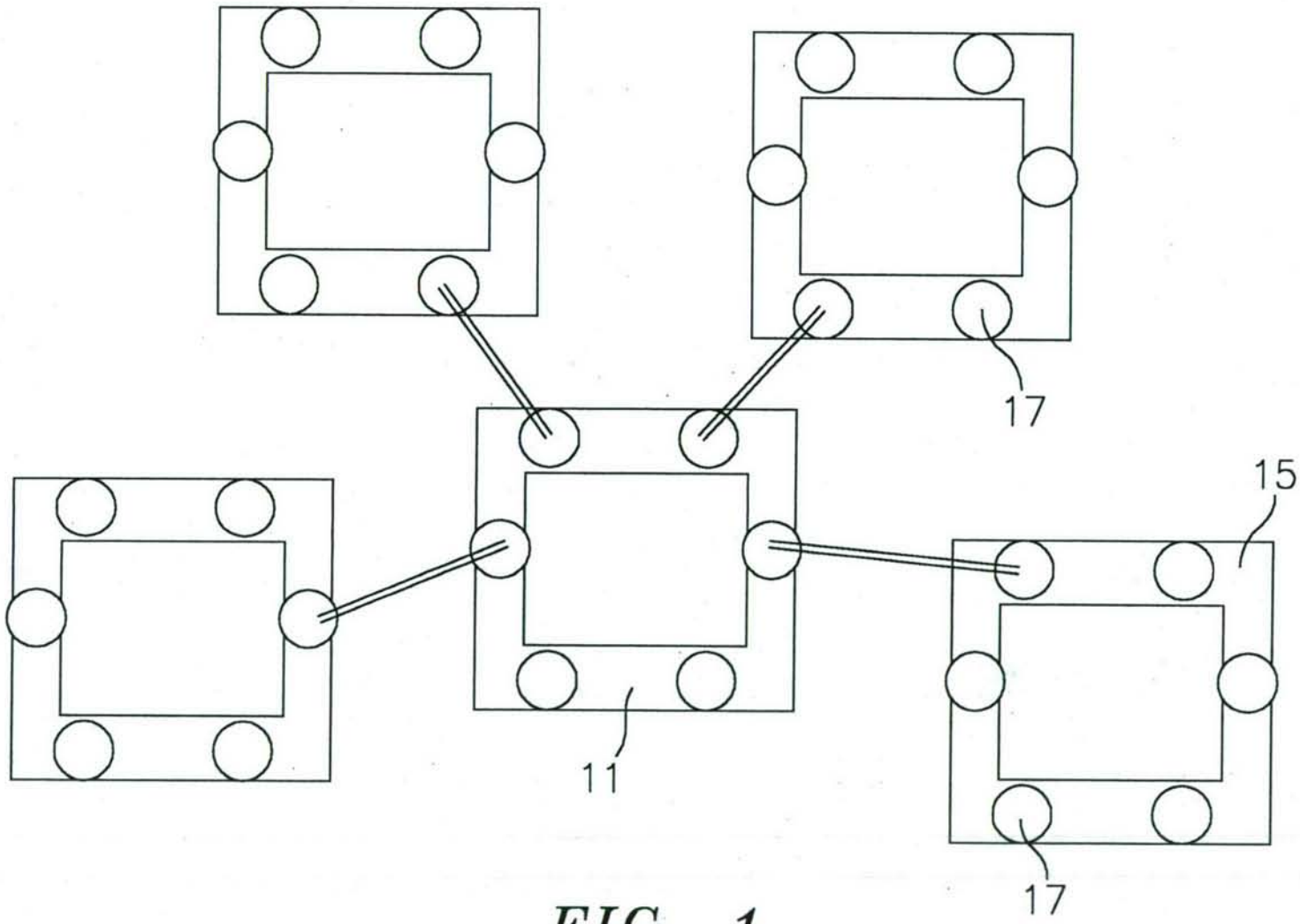

FIG. 1
(PRIOR ART)

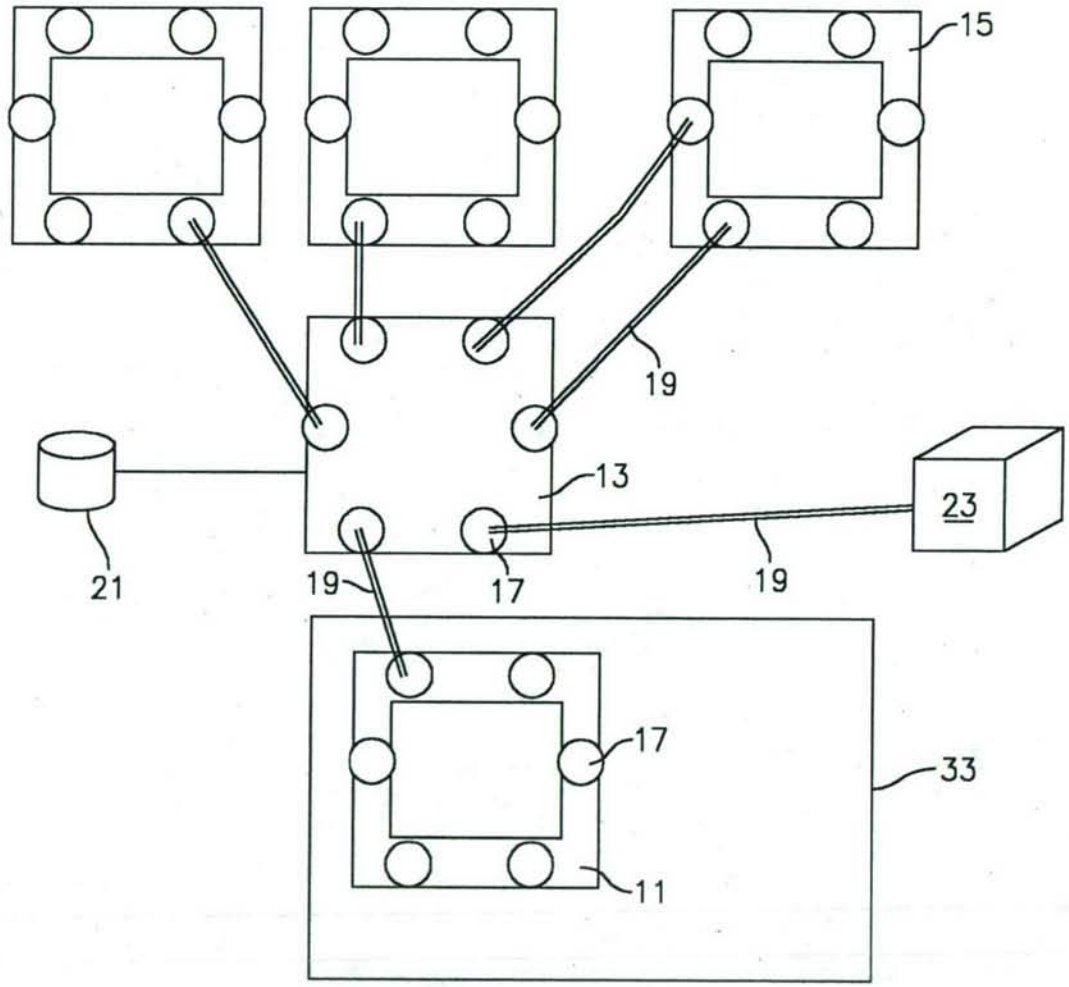

FIG. 2

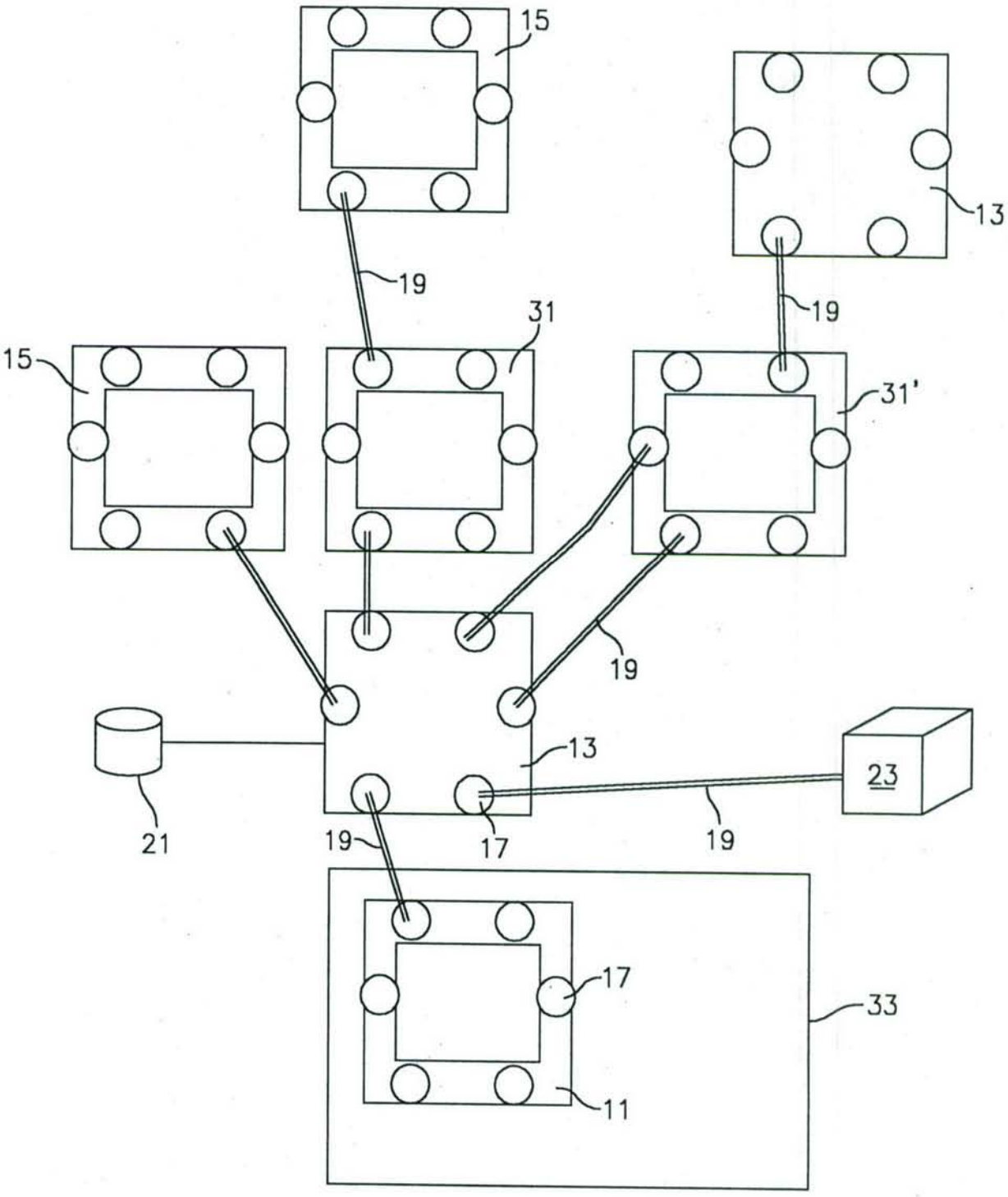

FIG. 3