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**GEORGIA TECH GT-VIAG
VLSI DESIGN VERIFICATION DOCUMENT**

VLSI DEVELOPMENT REPORT
REPORT NO. VDR-0142-90-009
MARCH 11, 1991

**GUIDANCE, NAVIGATION AND CONTROL
DIGITAL EMULATION TECHNOLOGY LABORATORY**

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COMPUTER ENGINEERING RESEARCH LABORATORY

Georgia Institute of Technology
Atlanta, Georgia 30332-0540

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MARCH 11, 1991

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GEORGIA TECH GT-VIAG VLSI DESIGN VERIFICATION DOCUMENT

INTRODUCTION

There are eleven (11) Georgia Tech VLSI designs (see Table 1) in the AHAT Program. Each of these designs has been produced by Georgia Tech using the Genesil Silicon Compiler. Each design has passed the design verification process at Silicon Compiler Systems / Mentor Graphics and each has been fabricated in a bulk CMOS process (fabrication of certain chips was not complete when this document was released). Each of the Georgia Tech designs listed in Table 1 is being delivered to USASDC and to the Harris Corporation for conversion and fabrication in a rad-hard process. The program under which this work is done is AHAT (Advanced Hardened Avionics Technology). This document includes design information for the Georgia Tech instruction address generation chip, GT-VIAG.

Table 1. Georgia Tech Chip Set for AHAT

Design	DV Passed	Tape Delivered	Fabricated	Tested
GT-VFPU/1A	1/17/89	8/3/90	5/19/89	4/4/90
GT-VNUC				
GT-VTF				
GT-VTHR	12/11/90	2/15/91	3/1/91	
GT-VCLS	1/26/90	7/12/90	7/13/90	
GT-VCTR	2/8/90	7/12/90	7/13/90	
GT-VIAG	3/8/91	3/11/91		
GT-VDAG	2/22/91	2/25/91		
GT-VSNI	1/17/89	5/23/90	4/14/89	4/4/90
GT-VSM8	1/17/89	6/8/90	5/6/89	4/4/90
GT-VSF	9/12/89	7/19/90	7/13/90	

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GT-VIAG : Instruction Address Generation Chip

1. Design Verification Checklist

The DV checklist attached in Appendix A.

2. Functional Description

This section describes briefly the function of the chip and the modules at core level.

2.1. Module boot_mod

Functional Description

The “boot rom” code that contains the instructions that are executed when IAG is in a bootstrap mode is actually implemented in a PLA named “boot_pla”. There is additional hardware that checks for the boot pattern whenever the instruction address (Pc) is zero. If the special pattern is not detected, the chip enters a bootstrap mode that enables it to load instruction and data memory from I/O device 3.

2.2. Module inst_mod

Functional Description

This module serves two main purposes. First, all instructions are funneled through this module, so that boot instructions can be substituted during the booting process. (I/O instructions are multiplexed in io_mod.) This also permits halting the instruction pipeline under certain circumstances using the “guard” signal. Second, another datapath contains the instruction registers. These are used to sample a single word of instruction memory or to write out a single word of instruction memory. This supports bootstrap loading, for example, by loading the registers from the network and then writing out the word after all the data has been received. Extra hardware controls the reading and writing process (so that, for example, an instruction that is sampled is not executed).

2.3. Module intr_mod

Functional Description

This module maintains the interrupt vector table, detects and prioritizes interrupt conditions, and determines whether and which interrupt to execute. The interrupt vector table is a RAM block, and it contains a single 26-bit destination address for each of the 16 possible interrupt conditions. The interrupt detection logic includes disabled and non-disabled interrupt registers and an “interrupt enable” flag that enables maskable interrupts. The “valid_intr_mod” takes into account the priority of the interrupt currently being serviced. If a higher priority interrupt occurs, it pushes the current interrupt onto its own internal hardware stack. All interrupt stack operations can only use the hardware stack.

2.4. Module io_mod

Functional Description

This module controls the input and output operations of the chipset. It identifies which I/O device should be active, whether the unit is in an input or output mode, and checks to make sure the I/O

device has completed the indicated operation. Besides much glue logic, it contains four separate modules to control synchronous and asynchronous input and output. These modules include PLA-based state machines to control handshaking.

2.5. Module `lcntr_mod`

Functional Description

This module contains the special-purpose loop counter and hardware to load, store, increment, and test it for zero. It can be loaded and stored directly or by using the "Begin Loop" and "End Loop" instructions. If the counter is non-zero when a "Begin Loop" is executed, the current loop counter value is pushed onto the stack. This supports nested loops.

2.6. Module `pc_gen_mod`

This module controls the Pc. It also contains the pc register, "BPP" control hardware, and the hardware stack and associated support.

Many modules are used to determine the next Pc. There are various kinds of branch conditions which can come from a wide variety of sources. (See the programming specification for more details.) Two modules, `brpend_ctrl` and `flush_ctrl`, detect and create a "flush" condition, which occurs when the wrong condition was chosen for a conditional branch. One module, "bradr_pla" accepts the raw instruction inputs and interrupt condition to determine the source of the next address. "pc_ndp_mod" uses this information to control the multiplexers, and it keeps track of the flush destination and can increment the Pc. The pc register is used for "external" branches and for instruction reading and writing. It contains an "autoincrement" to support writing to adjacent memory locations. The "BPP" hardware supports the BPP opcode by maintaining the BPP register and controlling whether the chip is in the BPP mode. Finally, additional hardware supports the hardware stack by controlling the source of the push, containing the necessary 32 deep by 27 bit wide RAM, and maintaining the stack pointer.

2.7. Module `pc_st_mod`

This module multiplexes the "pc_gen_mod" read out bus ("br_adr") with the loop counter. This is needed because loop counter instructions are part of so-called "pc_ld" and "pc_st" instructions.

2.8. Module `r_out_mod`

Functional Description

This module contains several multiplexers which control which part of the chip is being read out over the data (RF) bus. The control logic controls the selection.

2.9. Module `rf_din_mod`

Functional Description

This module controls the "f_r_1" bus, which is used for loading registers. It can drive the bus with the R bus one cycle before, the F bus one or two cycles before, or the value "0". The latter is used at reset to simultaneously reset most registers. The selection is based on the booting signal and the operand dependency checking signals. (See the documentation for DAG for a description of these.)

2.10. Module `status_mod`

Functional Description

This module checks for kernel instructions being executed in the user mode, maintains and flags any error conditions that occur, and contains a special-purpose status register that can be loaded with either error information or interrupt servicing information.

2.11. Module task_ptr_mod

Functional Description

This module contains the “task pointer” and “task pointer limit” registers. These are used when IAG is in the “user” mode to define an allowable range of instruction addresses. The task pointer is added in to every instruction address while in the user mode. (This adder is in pc_gen_mod.) Additional logic in this module controls whether the chip is in user or kernel mode.

2.12. Module timer_mod

Functional Description

This module contains two “timers”, which are actually 16-bit counters. There are registers that control the starting value of the two count-up counters. A carry-out from either timer is flagged as an interrupt.

2.13. Instruction decoder modules (5 random logic blocks)

Functional Description

There are five random logic blocks that carry out some of the instruction decoding. (Some additional decoding is performed by the individual modules listed above.) The five modules are pc_maj_dec, MISC_dec, LD_dec, ST_dec, and inst_en. The first four are somewhat hierarchical, in that one signal from one enables the next.

3. Signal Descriptions

3.1. Inputs

A description of the inputs and outputs to the IAG are described below. All signals are active high except those that start with “N_”.

Name	Timing	From	Purpose
ALU_flag	SB(t)	ALU	Undesignated ALU flag.
Carry	SB(t)	ALU	Carry flag from the ALU.
Clk	N/A	Ext.	Provides clocking control to the chip.
DAG_error	VB(t)	DAG	Indicates that an error has occurred at the GT-VIAG chip.
DAV[3:1]	VB(t)	I/O	Input device ready for I/O devices 1 to 3
IAG_test[1:0]	VB(t)	Ext.	Test pins that manually control “freeze” and “guard” modes on IAG to permit non-destructive state readout
Inst_rdy	VB(t)	Inst. Mem.	Instruction ready line. If this line is low, the next instruction executed will be a nop. (That is, the instruction will be disregarded.)

Intr[8:0]	VB(t)	Ext.	9 external interrupt signals.
N_reset	VB(t)	Ext.	Active low external reset line for the GT-VIAG chip.
Pixel_clk	VB(t)	Ext.	Clock for SP chips—used as data input for IAG to compute Ios signal which controls SP I/O
RFI[3:1]	VA(t)	I/O	Output device ready for I/O devices 1 to 3
R_eq_f_1	VB(t)	DAG	Status for R_adr[25:0] equals to F_adr_1[25:0]
R_eq_f_2	VB(t)	DAG	Status for R_adr[25:0] equals to F_adr_2[25:0]
Sign	SB(t)	ALU	Sign flag from the ALU.
Status[4:0]	VB(t)	Ext.	Five external status lines that can be used as branch conditions.
S_eq_f_1	VB(t)	DAG	Status for S_adr[25:0] equals to F_adr_1[25:0]
S_eq_f_2	VB(t)	DAG	Status for S_adr[25:0] equals to F_adr_2[25:0]
Zero	SB(t)	ALU	Zero flag from the ALU.

3.2. Outputs

The primary destination is listed below. All signals are active high except those that start with “N_”.

Name	Timing	To	Purpose
ALU_opcode[7:0]	SB(t)	ALU	Opcodes to control the operation of the ALU.
Booting	SB(t)	DAG	Indicates GT-EP chipset has entered a bootstrap mode.
DAG_R_en	SB(t)	DAG	R-bus enable line for the GT-VDAG chip.
Flush	VB(t)	EP	Indicates that a wrong execution path has been taken and that all pipeline registers need to be flushed.
Freeze	VB(t)	EP	Indicates that instruction execution is temporarily suspended.
Guard	VB(t)	DAG	Halts loading of new instructions into instruction pipe.
Ids_eq_ods_1/2	SB(t)	DAG	Compares current Ids[3:0] with Ods[3:0] from one and two cycles ago. Used for operand dependency checking on GT-VDAG.
Ids_freeze	SB(t)	DAG	Indicates an input operation has blocked.
Ids_sel	WB(t)	ALU,I/O	Active high signal indicating that the GT-VIAG I/O is in the input mode. This signal is the inverse of the Ods_sel signal.
Inst_en	SB(t)	DAG	Activates output drivers on instruction lines on GT-VDAG chip; used to load instruction memory.
Inst_rd	SB(t)	DAG	Instruct the GT-VDAG chip to read the value on the instruction data bus into its instruction registers.
Ios	SB(t)	I/O	SP I/O interface control signal that prevents two asynchronous I/O events from happening in one Pixel_clk phase.

Kernel_mode	SB(t)	DAG	Indicates that instruction execution is currently in kernel mode.
Ncs[3:1]	W(t)	I/O	Active low chip selects for I/O devices 1 to 3.
N_cs_pha	VA(t)	Inst. Mem.	Chip select for the instruction memory that is accessed on PHASE_A.
N_cs_phb	VB(t)	Inst. Mem.	Chip select for the instruction memory that is accessed on PHASE_B.
N_inst_wr	VA(t)	Inst. Mem.	Write signal line for the instruction memory.
N_read[1]	VB(t)	I/O	Active low read signal for device 1.
N_reset_out	SB(t)	EP	Reset signal that includes hard reset and soft reset.
N_write[1]	VA(t)	I/O	Active low write signal for device 1.
Ods_freeze	SB(t)	DAG	Indicates an output operation has blocked.
Ods_ids[3:0]	W(t)	I/O	Multiplexed input and output device select lines.
Ods_sel	WA(t)	I/O	Active high signal indicating that the GT-VIAG I/O is in the output mode.
Pc[25:0]	SA(t)	Inst. Mem.	Program counter used to fetch the next instruction fields.
Read[3:2]	VB(t)	I/O	Active high read signals for devices 2 and 3.
Valid_intr_pulse	SB(t)	DAG	Instruct the GT-VDAG chip to cancel the execution of the current instruction because an interrupt has occurred.
Write[3:2]	VA(t)	I/O	Active high write signals for devices 2 and 3.

3.3. Bidirectional

Name	Timing	From/To	Purpose
Dr	W(t)	I/O	This signal stands for the active low device ready status line. If no I/O device is being accessed, IAG drives the line high.
Inst[45:0]	VB(t)/SA(t)	Inst. Mem.	Bi-directional instruction fields.
RF[31:0]	VB(t)/VB(t)	I/O,EP	Bidirectional data bus used to funnel information in and out of the GT-VIAG chip.

Table 3.1 Pin Summary Table

4. Final Notes

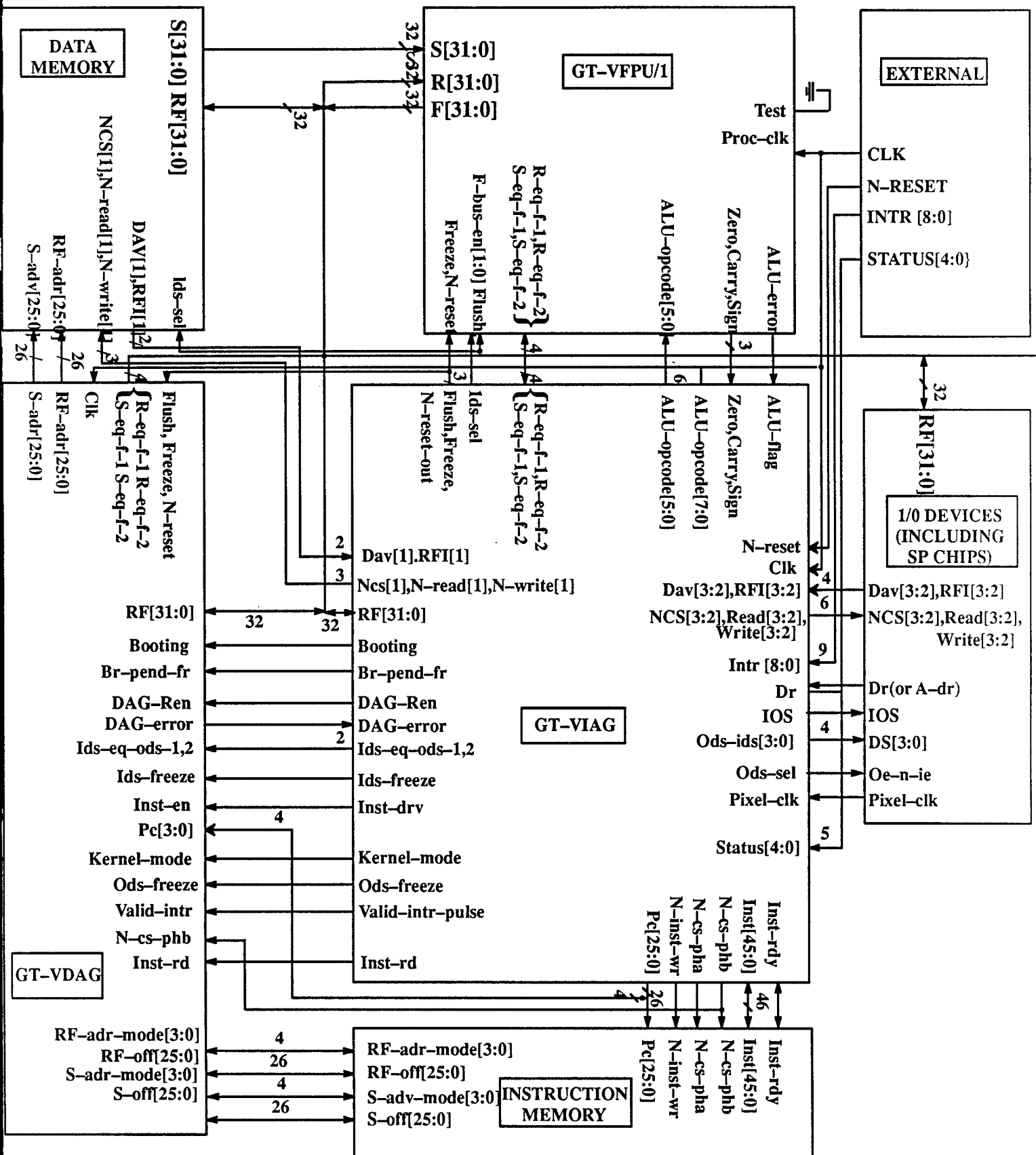
The chip required minor modifications during DV. There were two reasons for this. First, the chip power and ground router was not behaving properly, and so some of the rails needed widening. Second, the "bradr_pla" found in pc_gen_mod grew significantly larger because Mentor Graphics

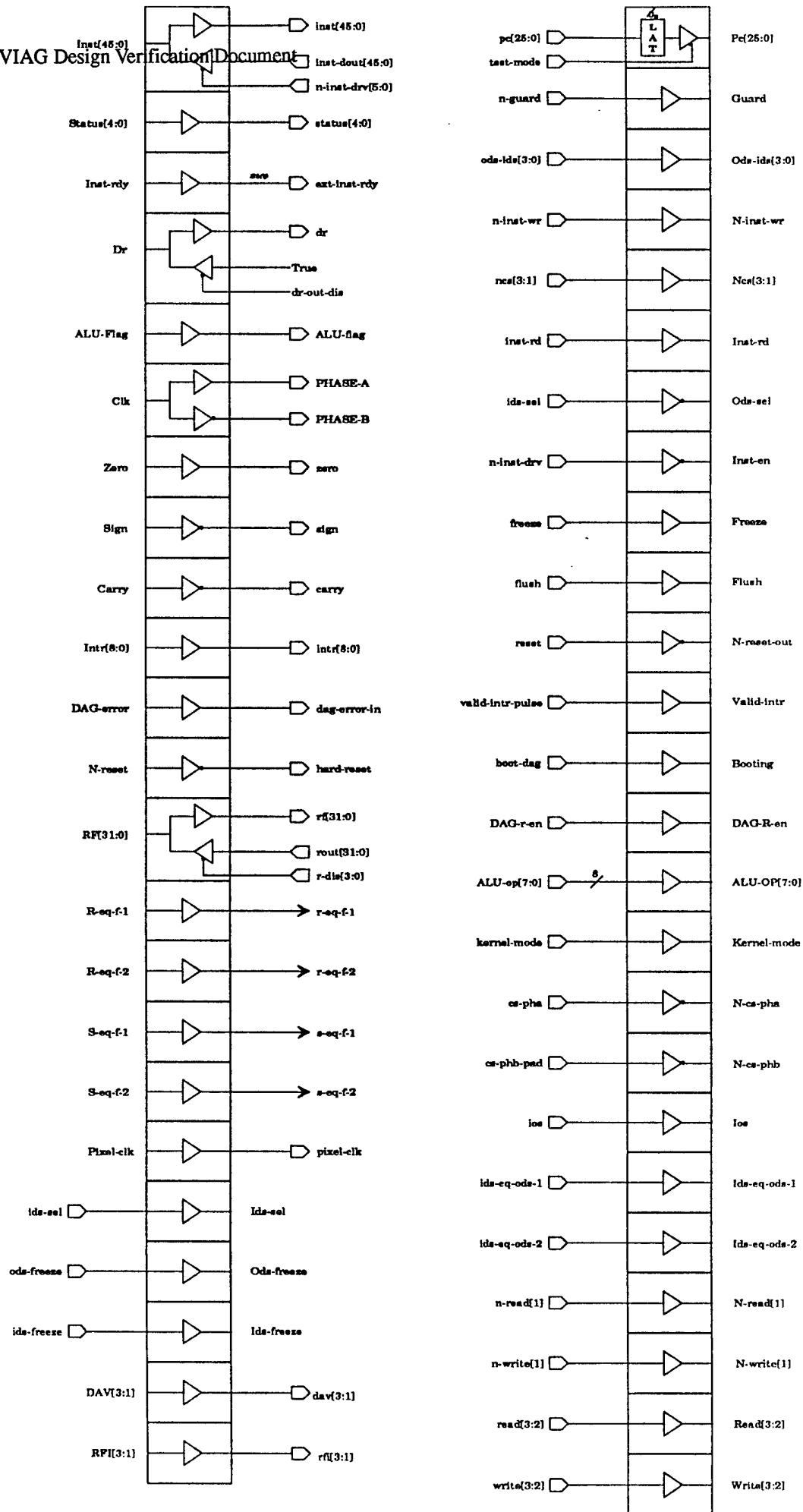
was using a later release of their logic compiler software. This had a direct impact on chip size. The power and ground rail problem was fixed and the logic compiler blocks were set to optimize slightly differently. The final chip size is 411 mils by 427 mils, and the cycle time (75 degrees C, 5.0V, Typical) is 91.8 ns.

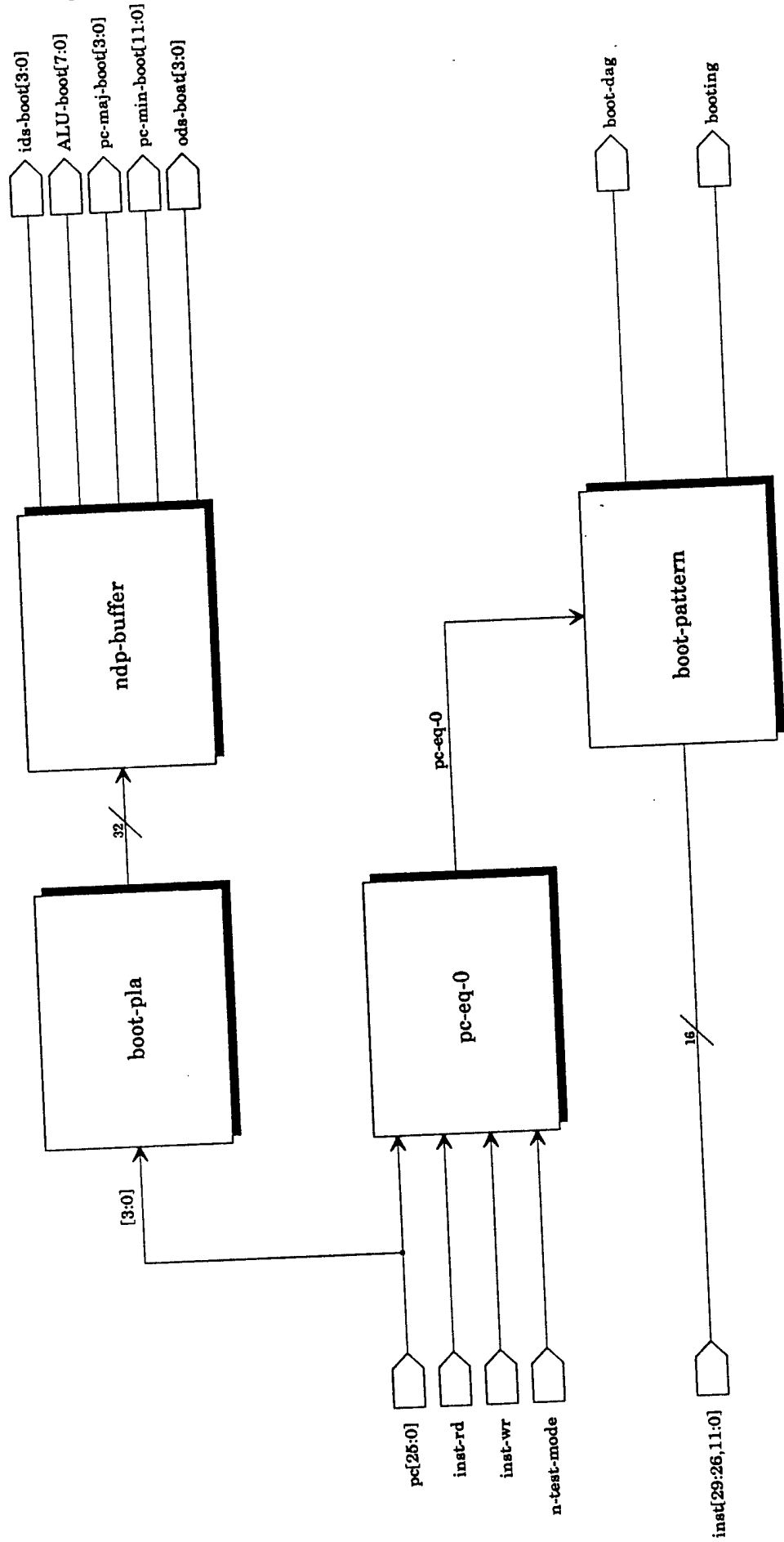
NOTE: Instructions for recovering the DV database from the tape should be enclosed with the tape itself.

5. Block Diagrams and Schematics

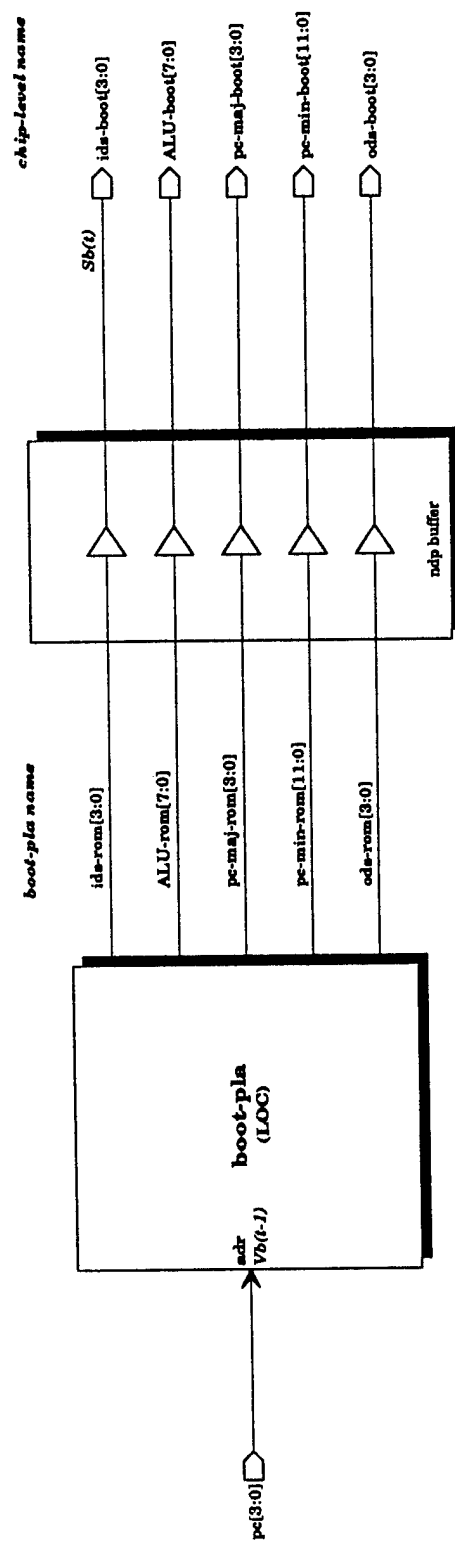
The following is a series of schematics that describe the hardware of GT-VIAG and its part in the EP chipset. This section begins with a diagram of how GT-VIAG and GT-VDAG fit together in a complete system.





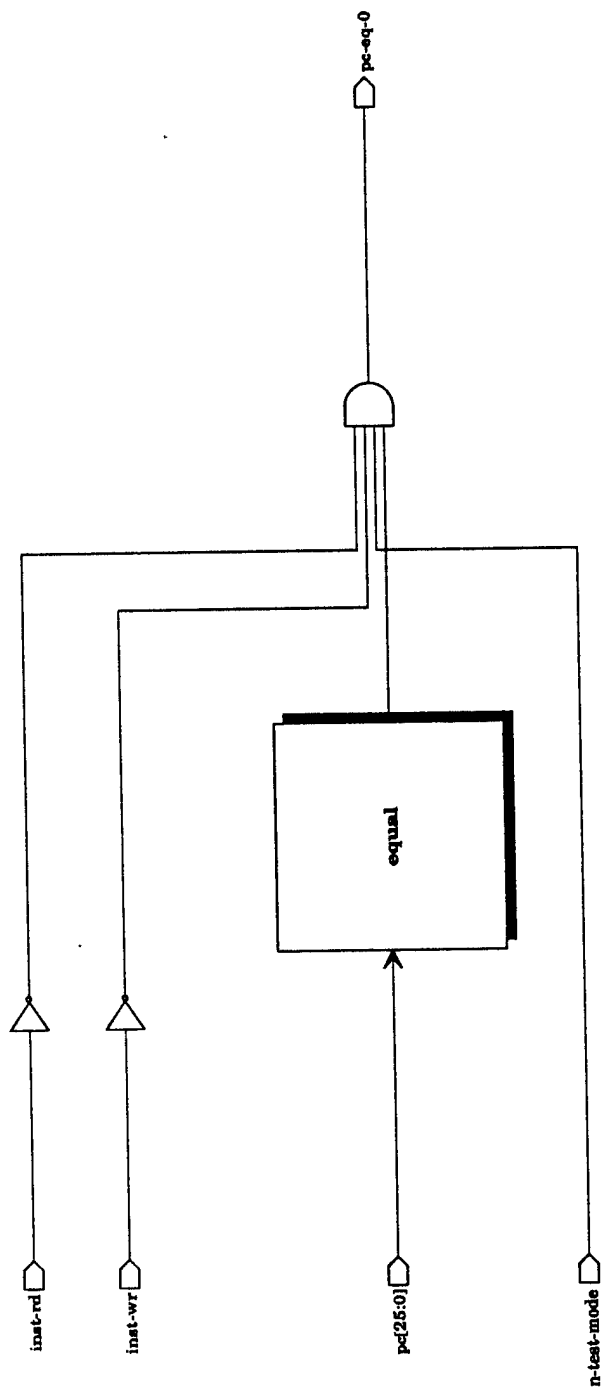


boot-mod

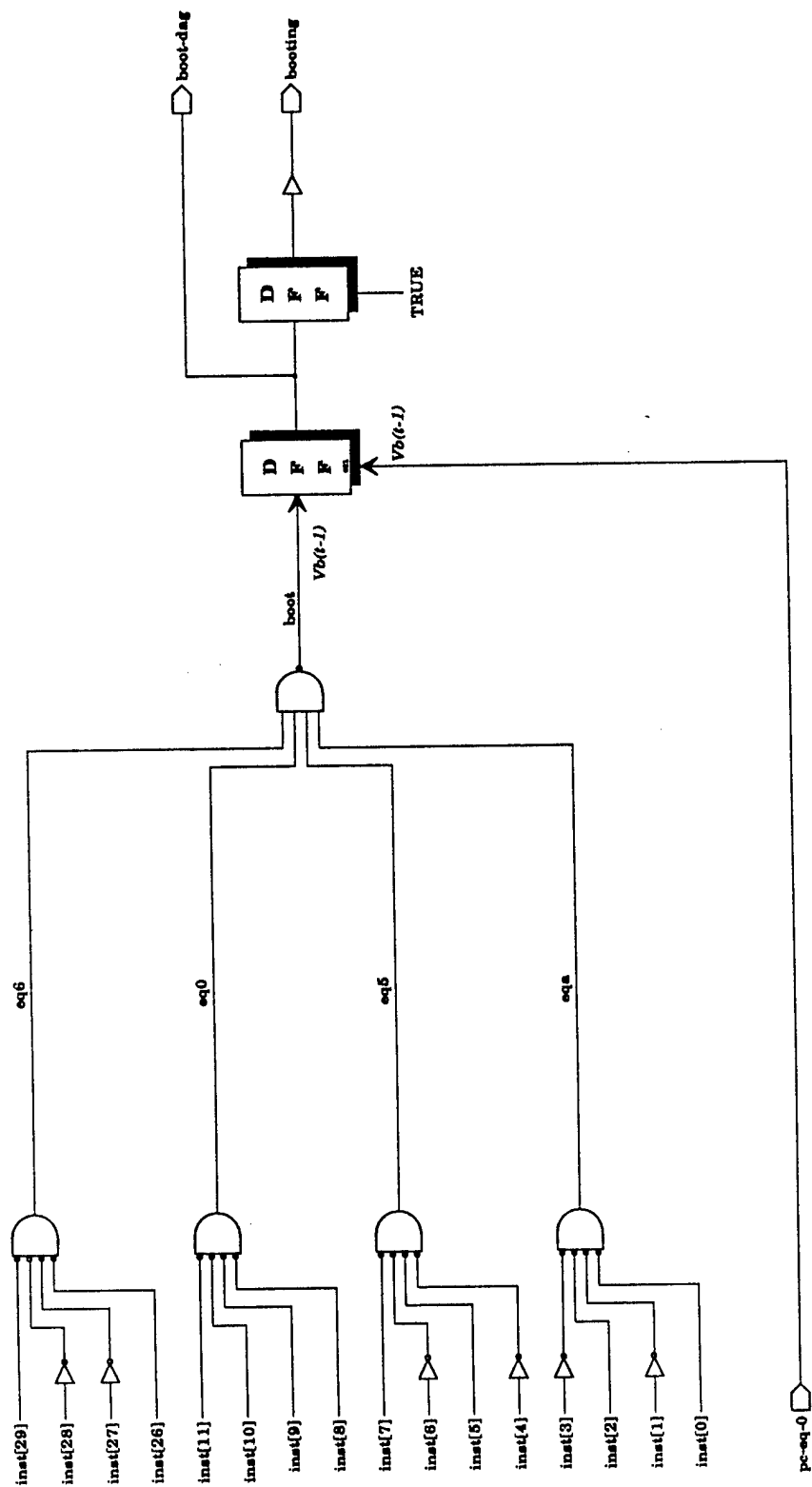


boot-pla

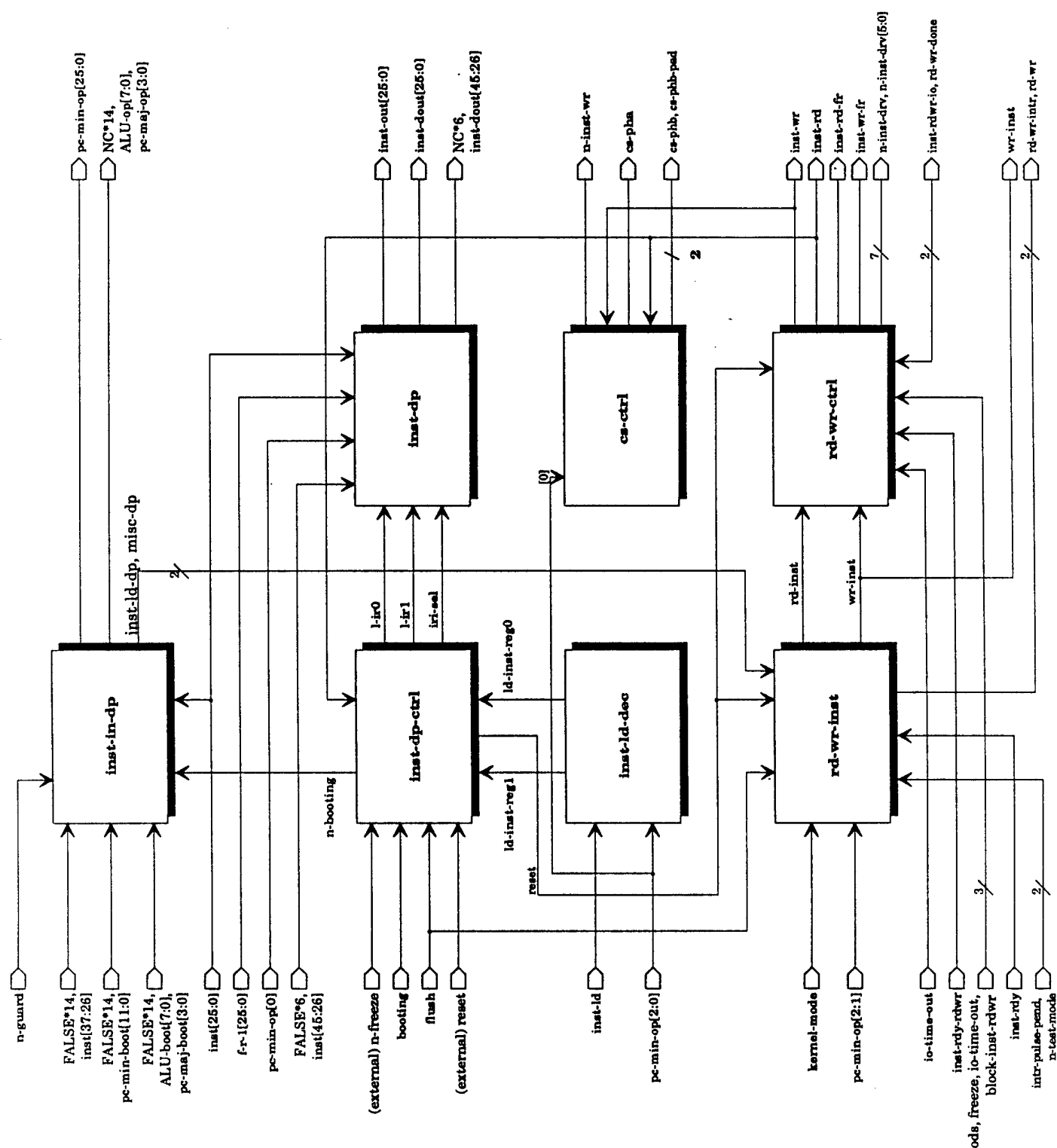
\\gt-viag\pc-eq-0.drw



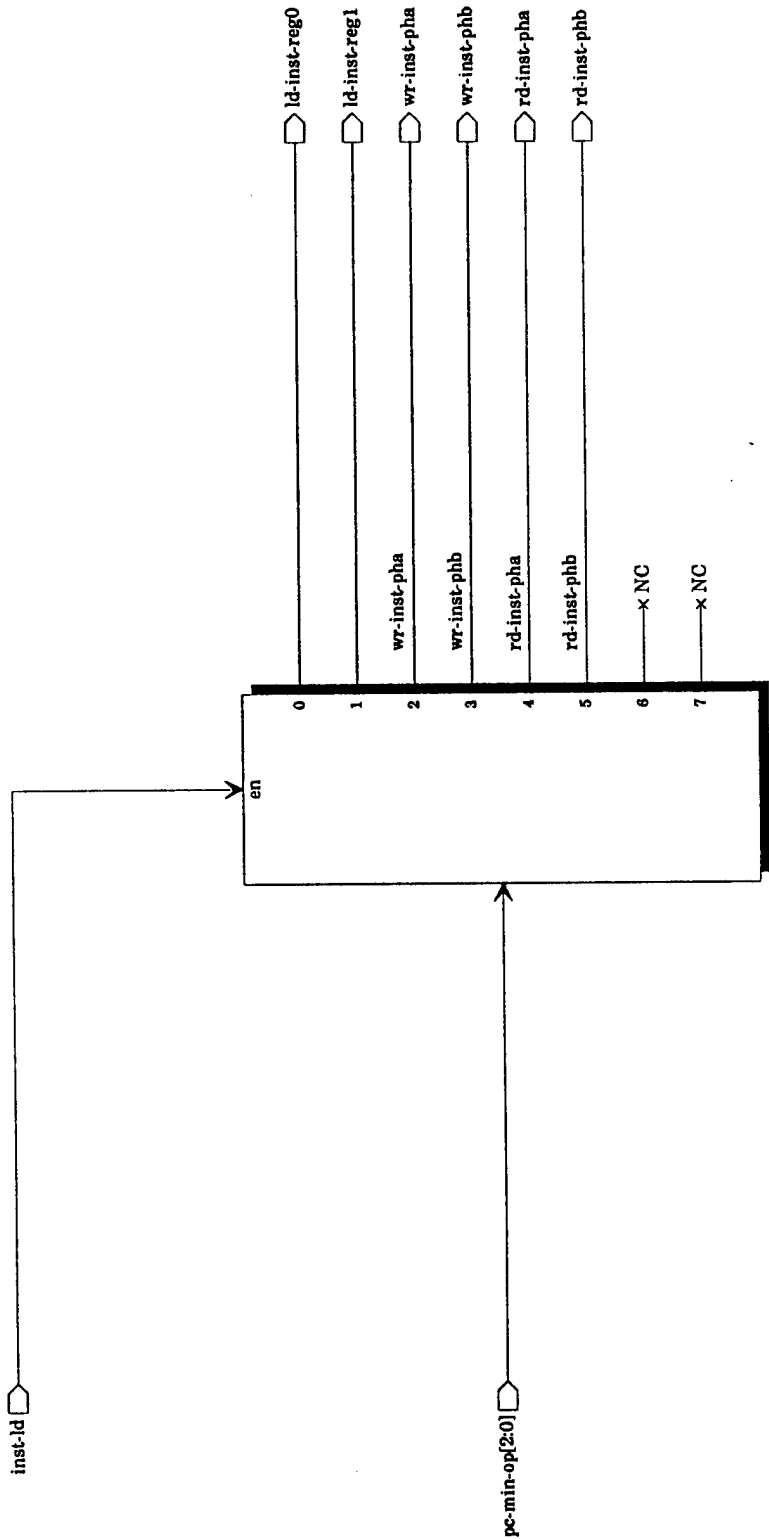
pc-eq-0



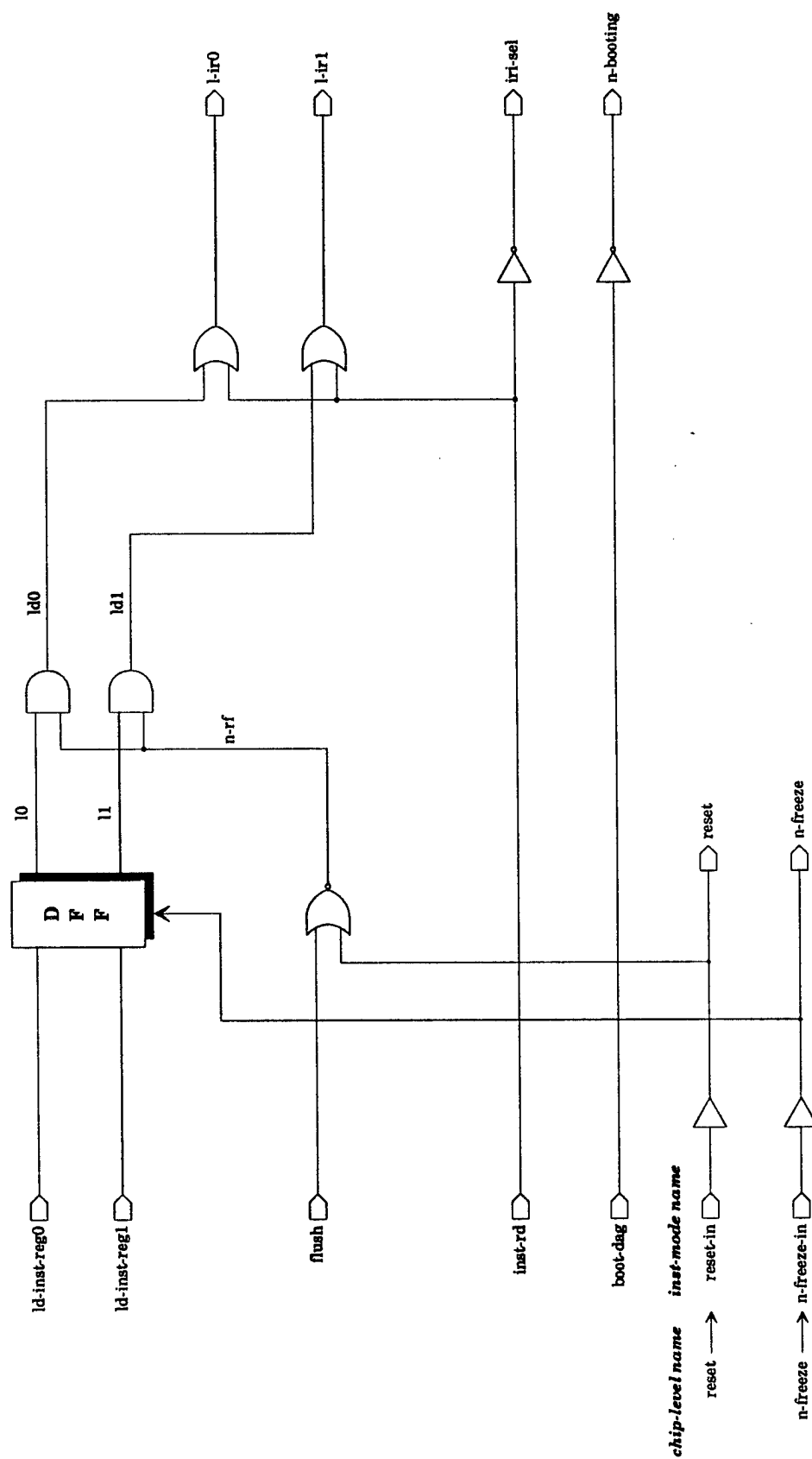
boot-pattern

**inst-mod**

C:\Program Files\Internet Explorer\iexplore.exe

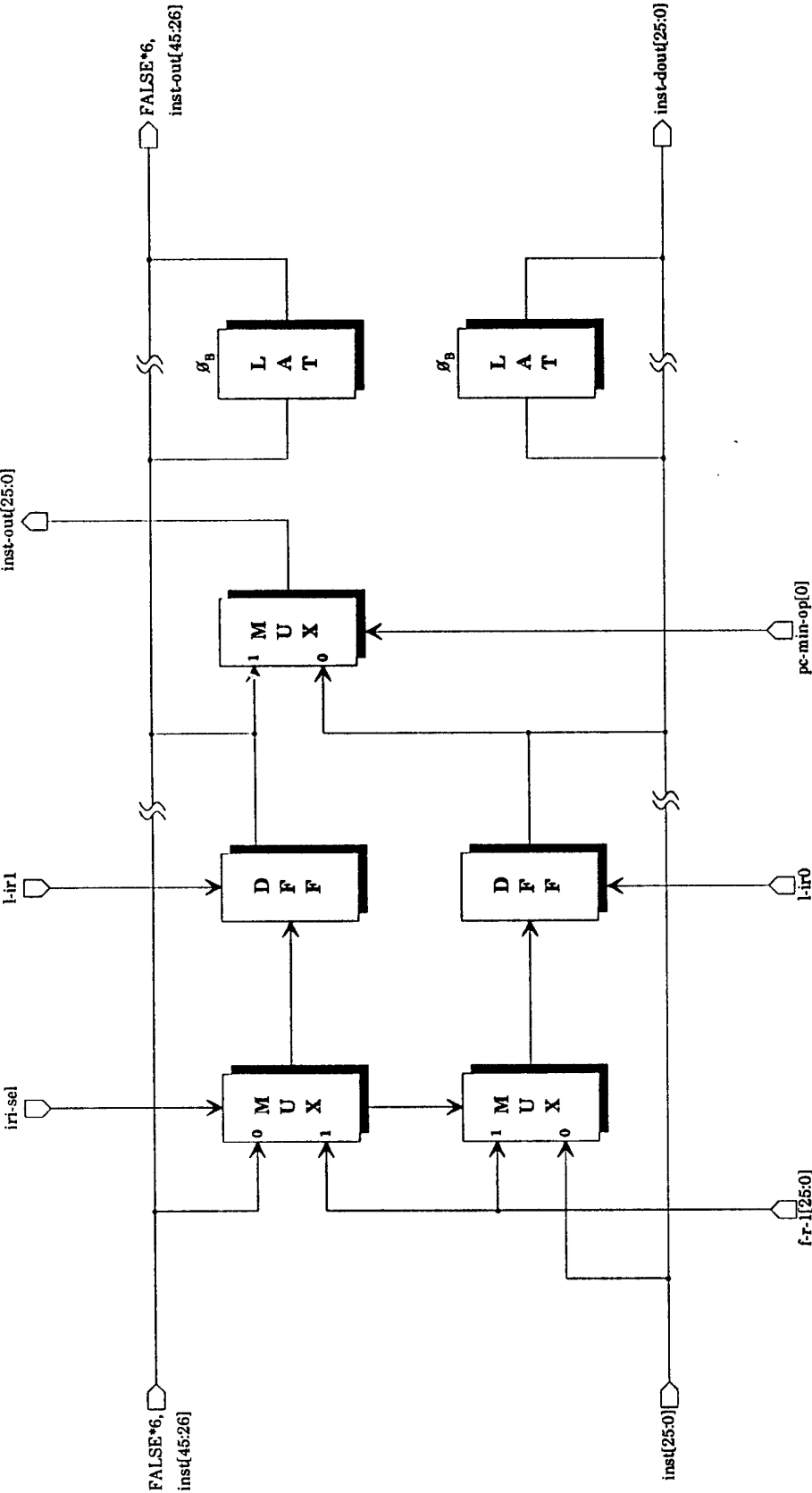


inst-ld-dec

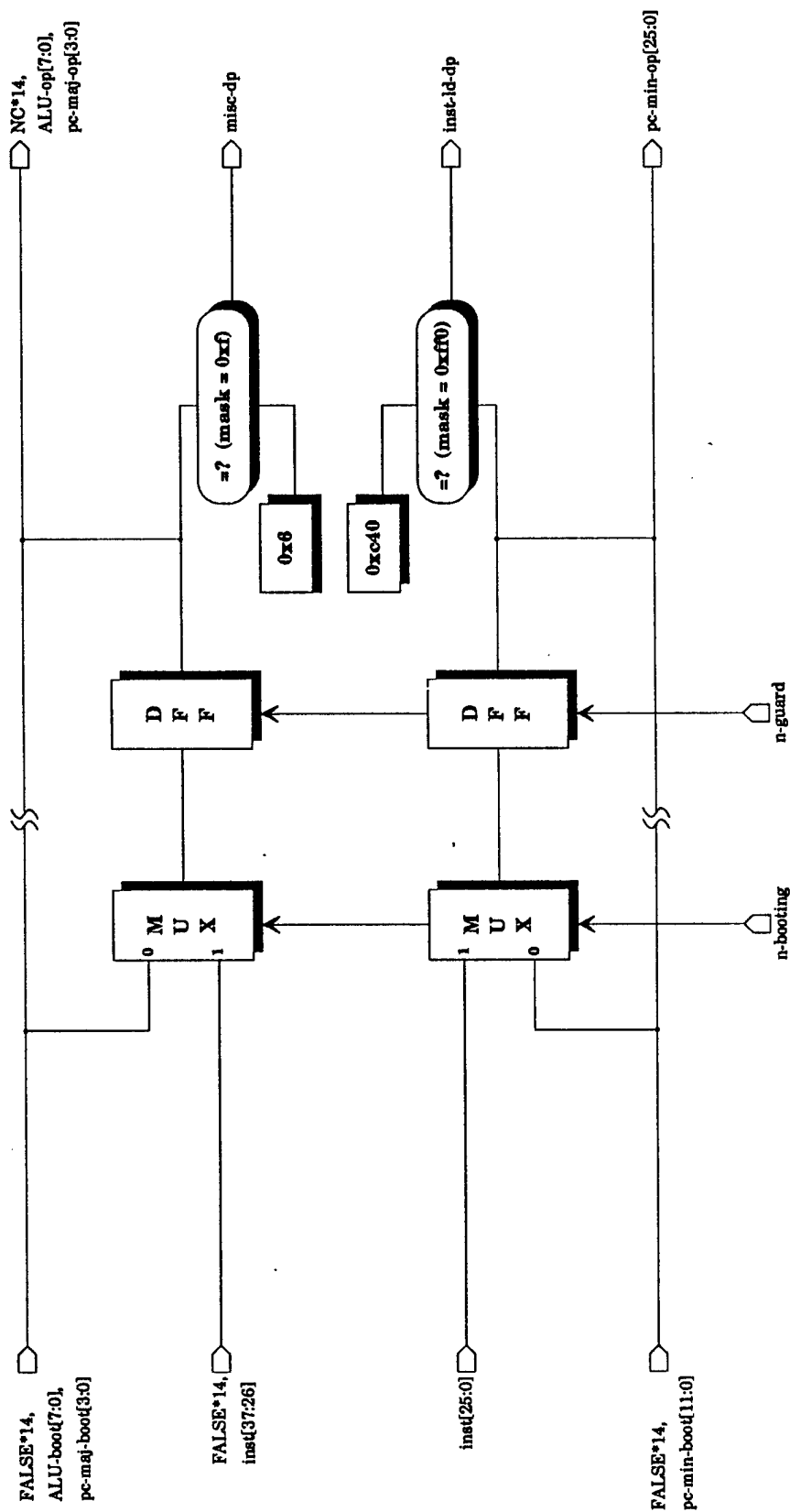


inst-mod
inst-dp-ctrl

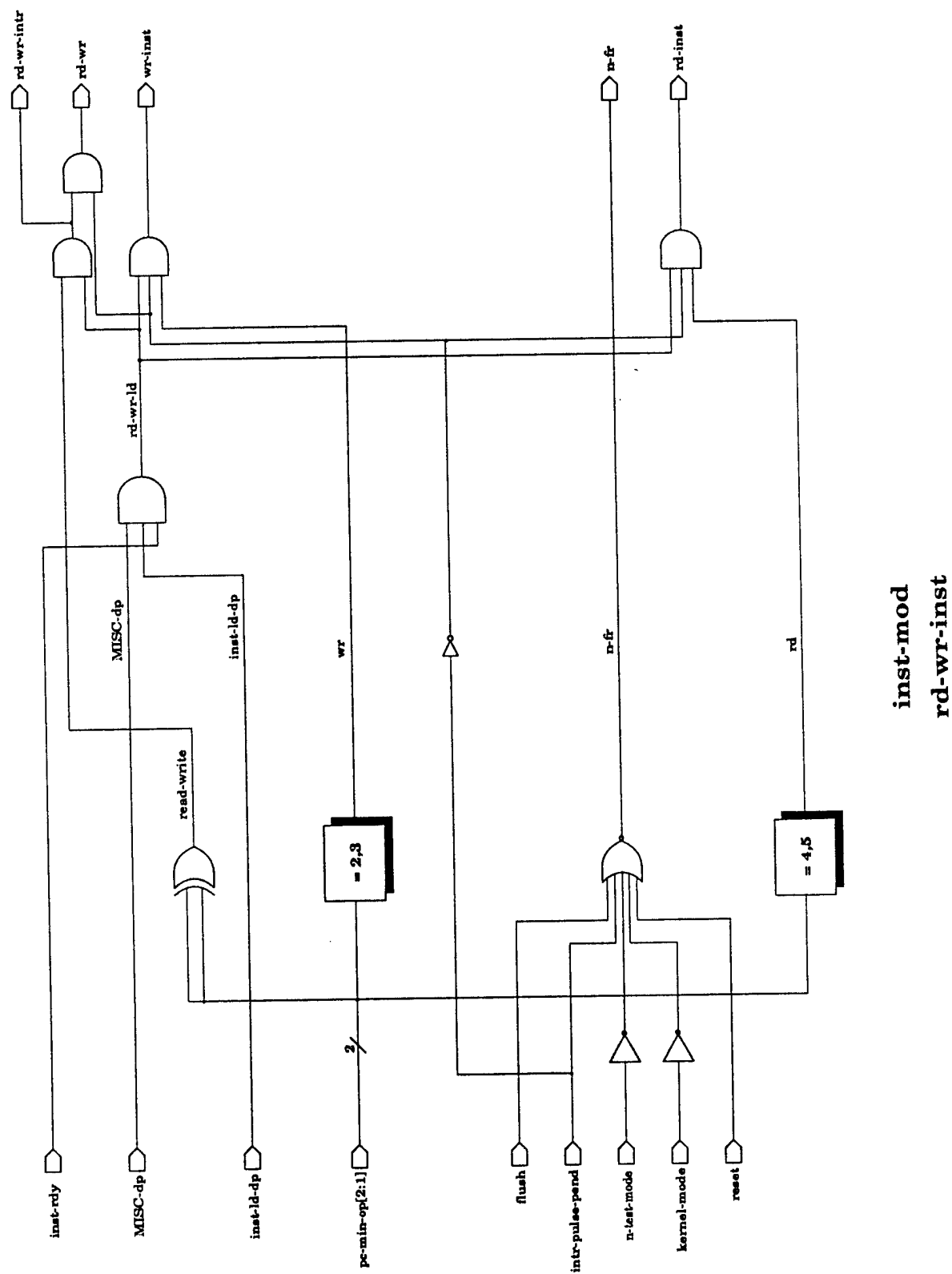
v:\gt-viag\inst-dp.drw

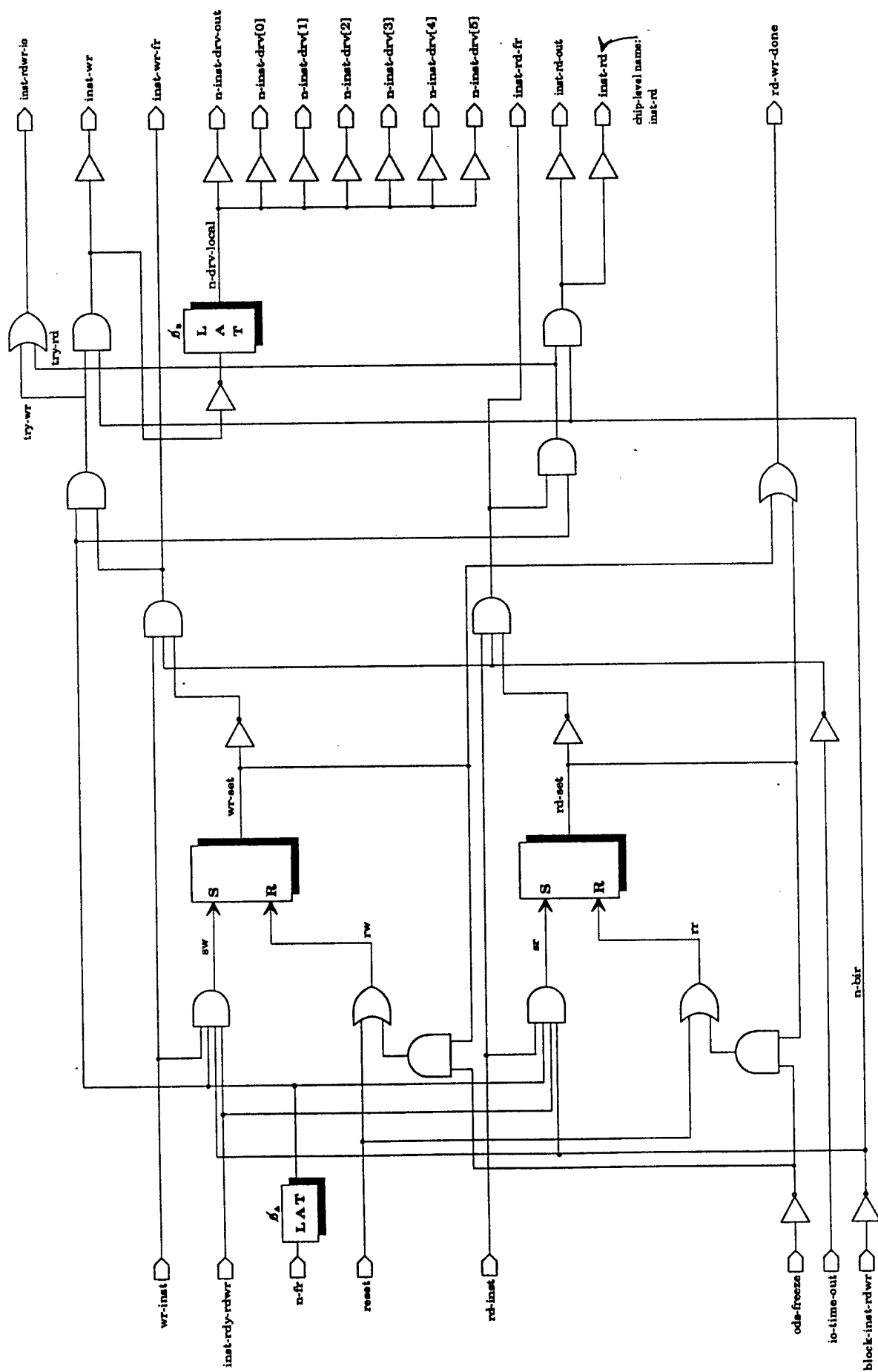


inst-dp

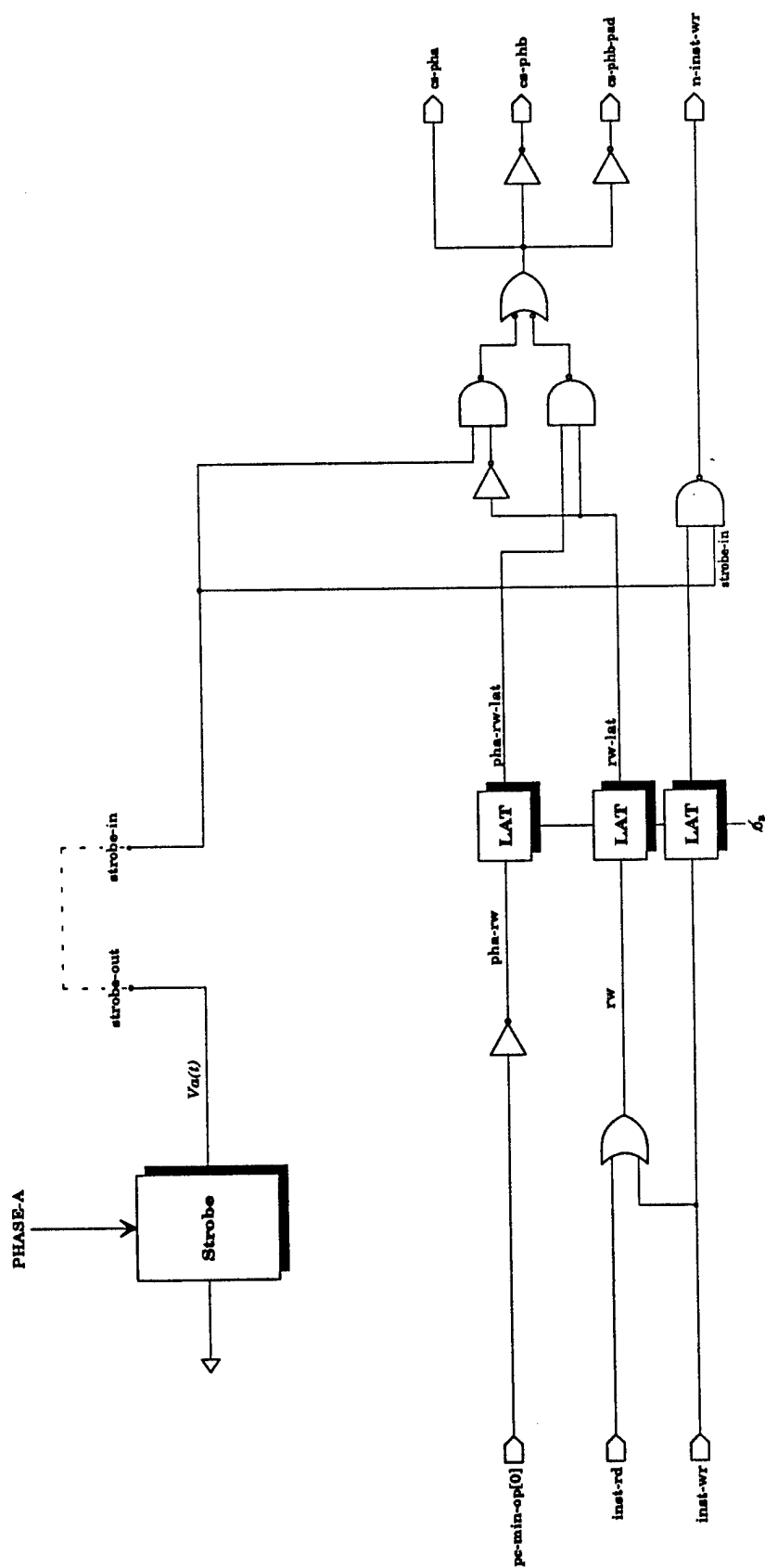


inst-in-dp

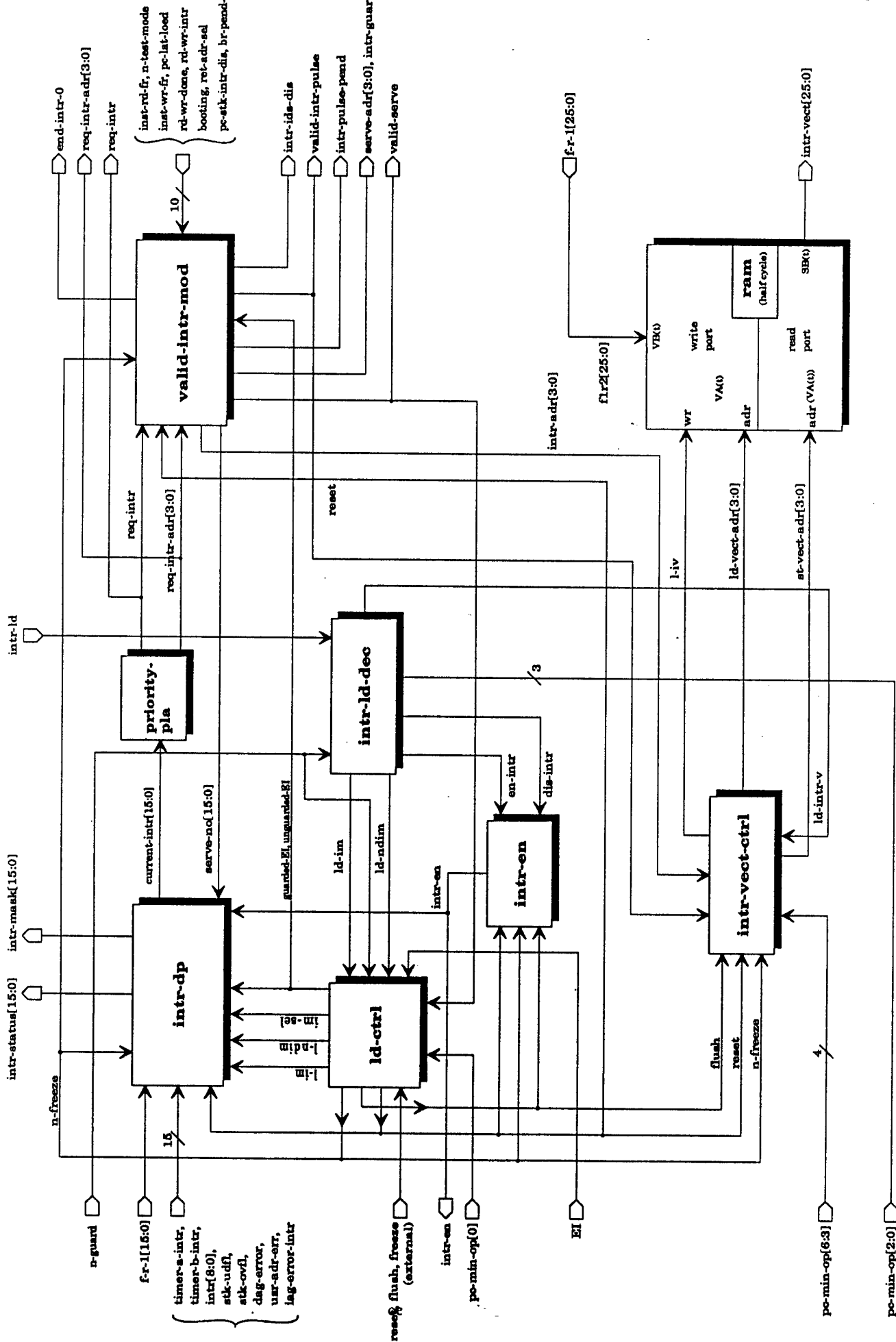


inst-mod
rd-wr-ctrl

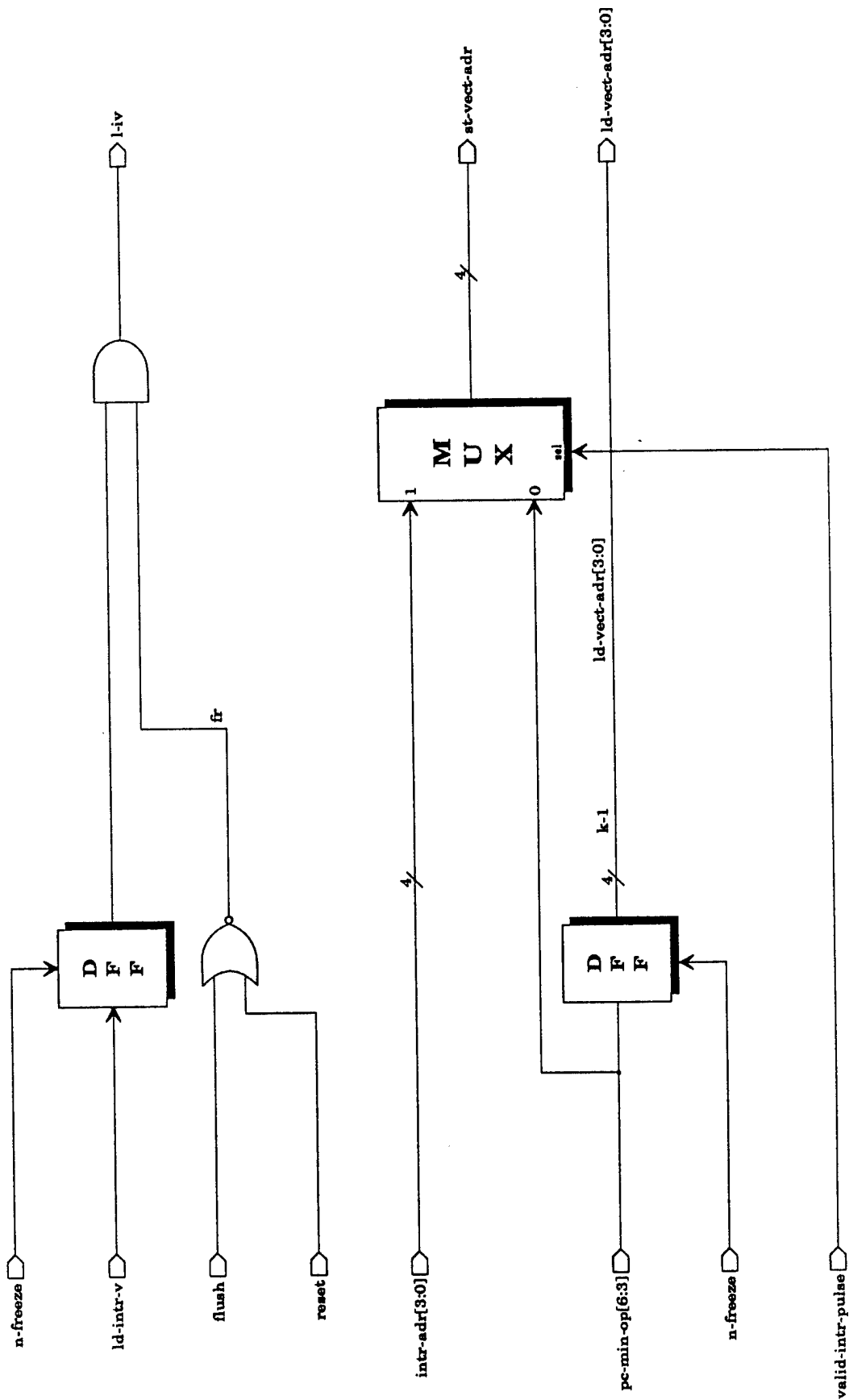
v:\ge-viag\rdw\etel.drw



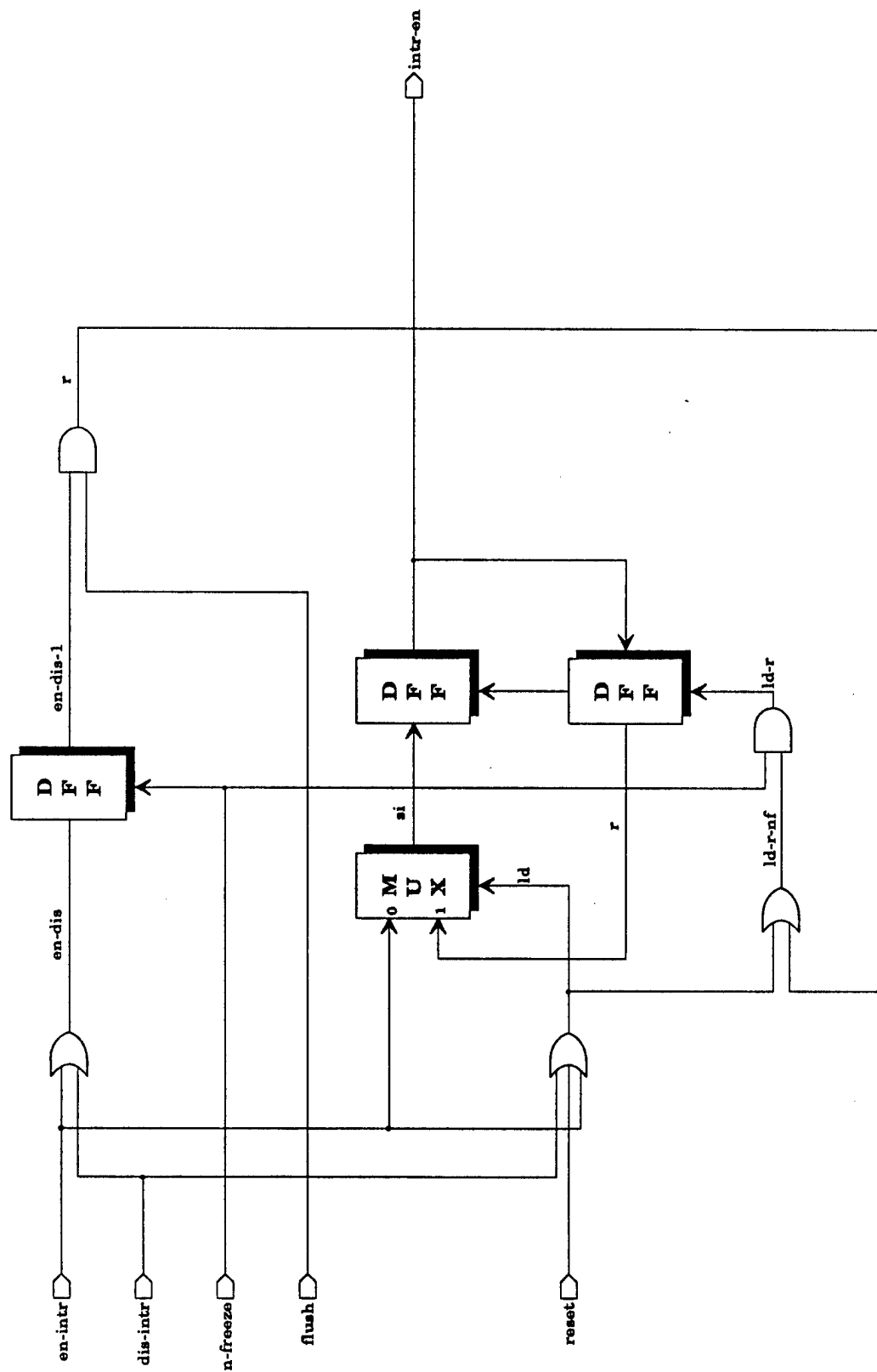
cs-ctrl

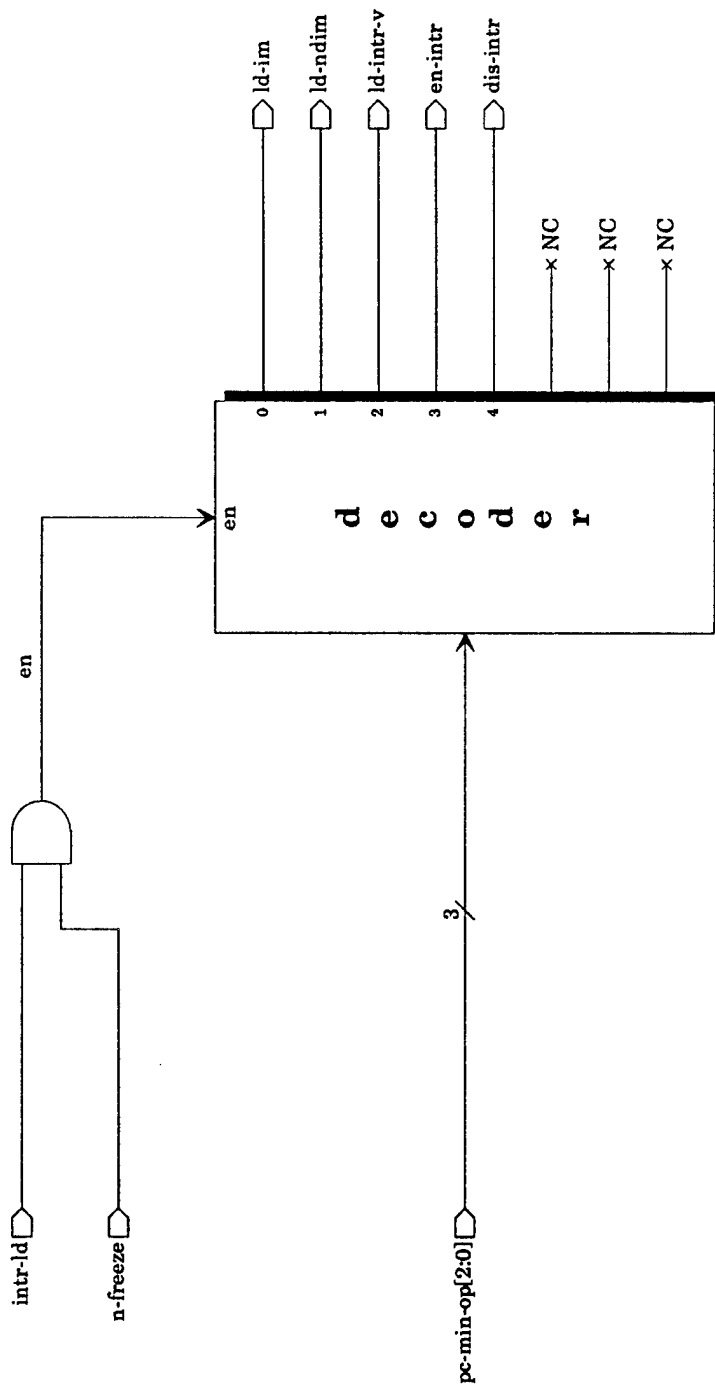


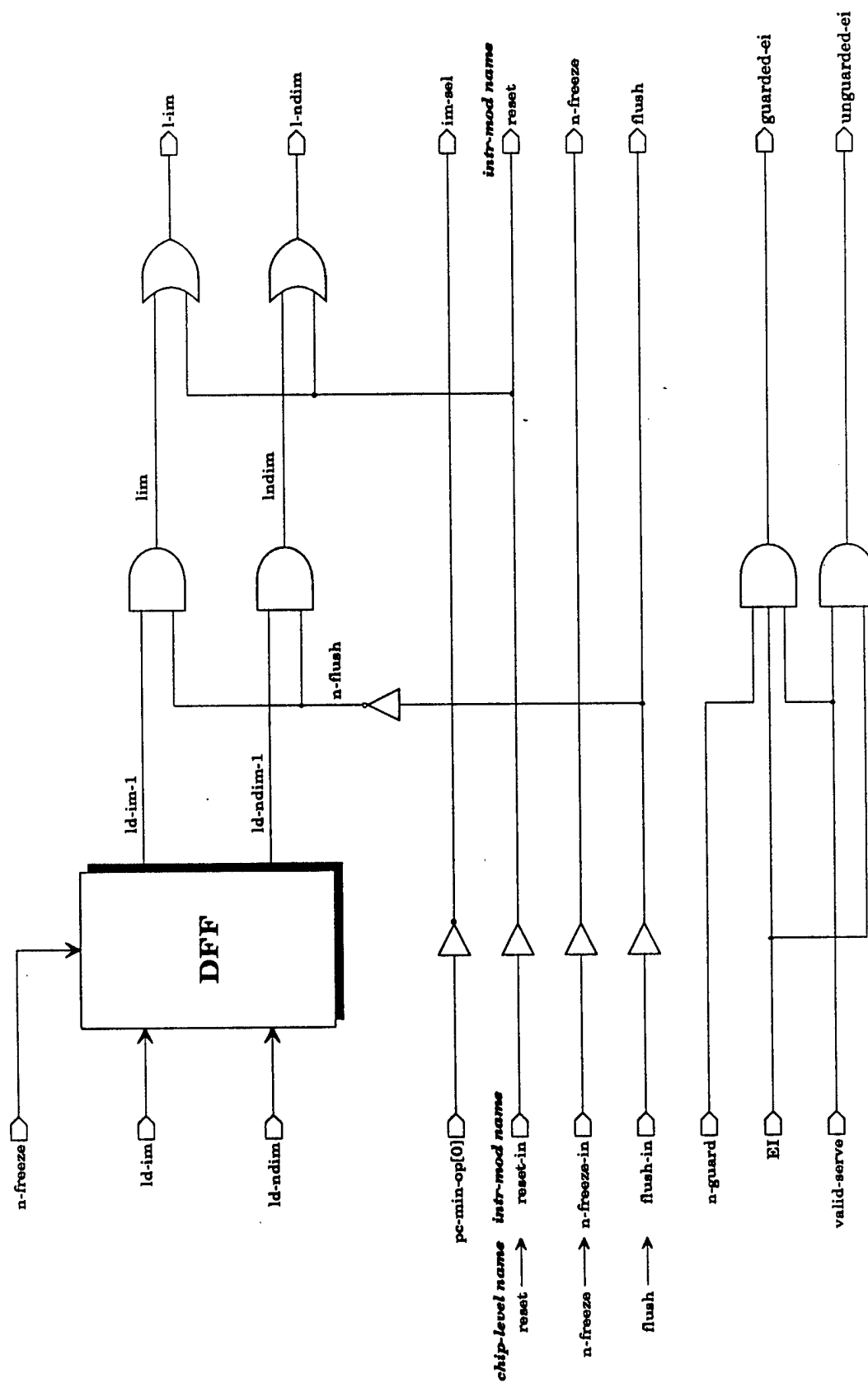
intr-mod



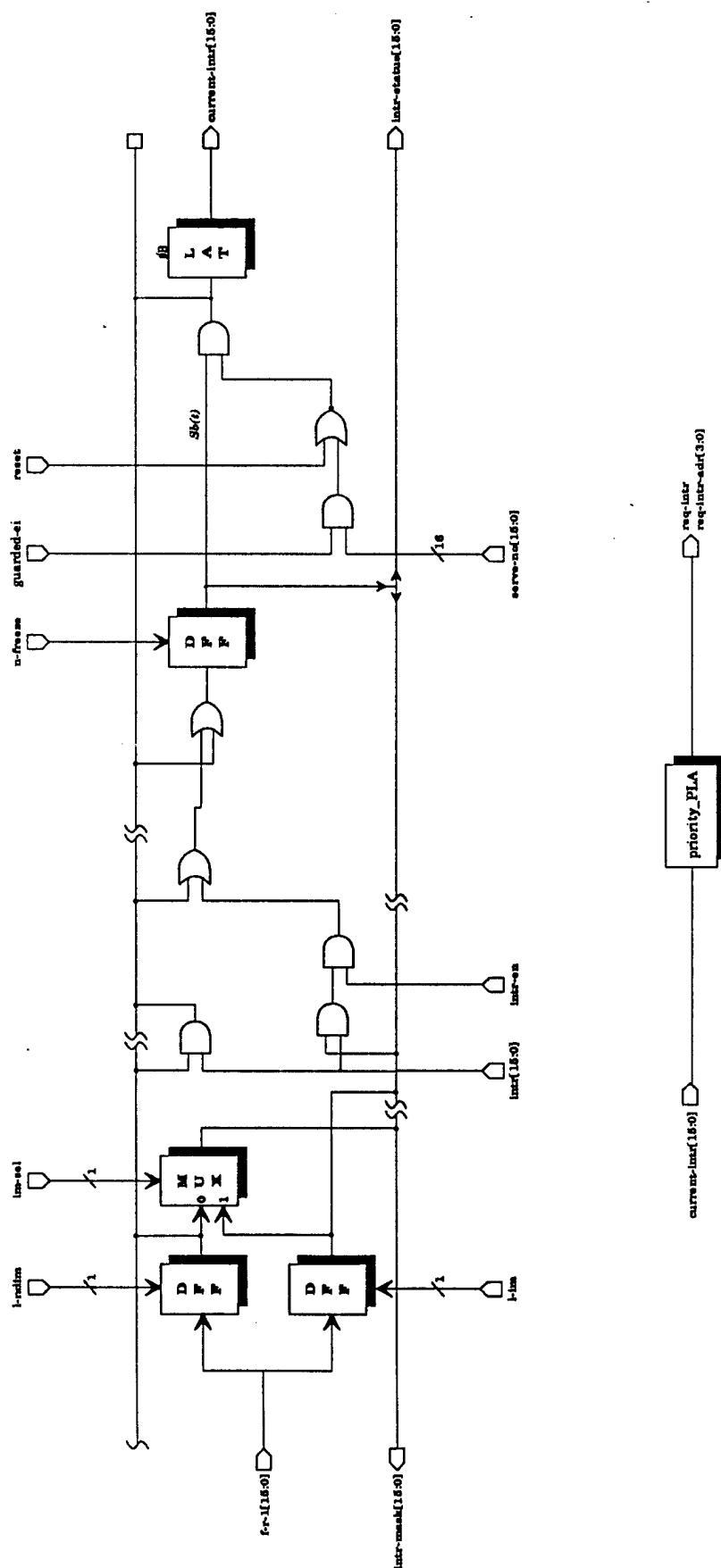
intr-vect-ctrl

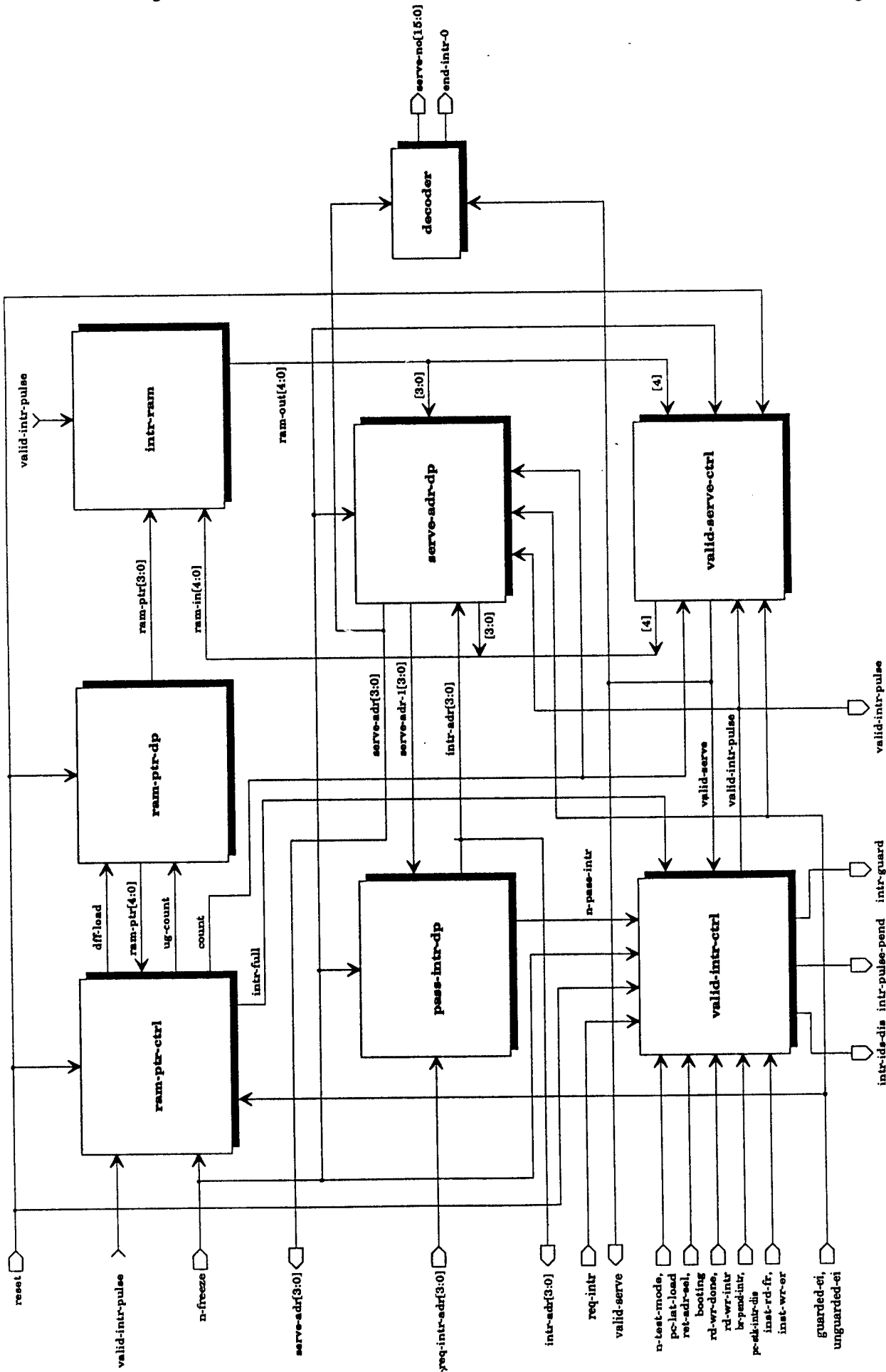
**intr-en**

**intr-lid-dec**

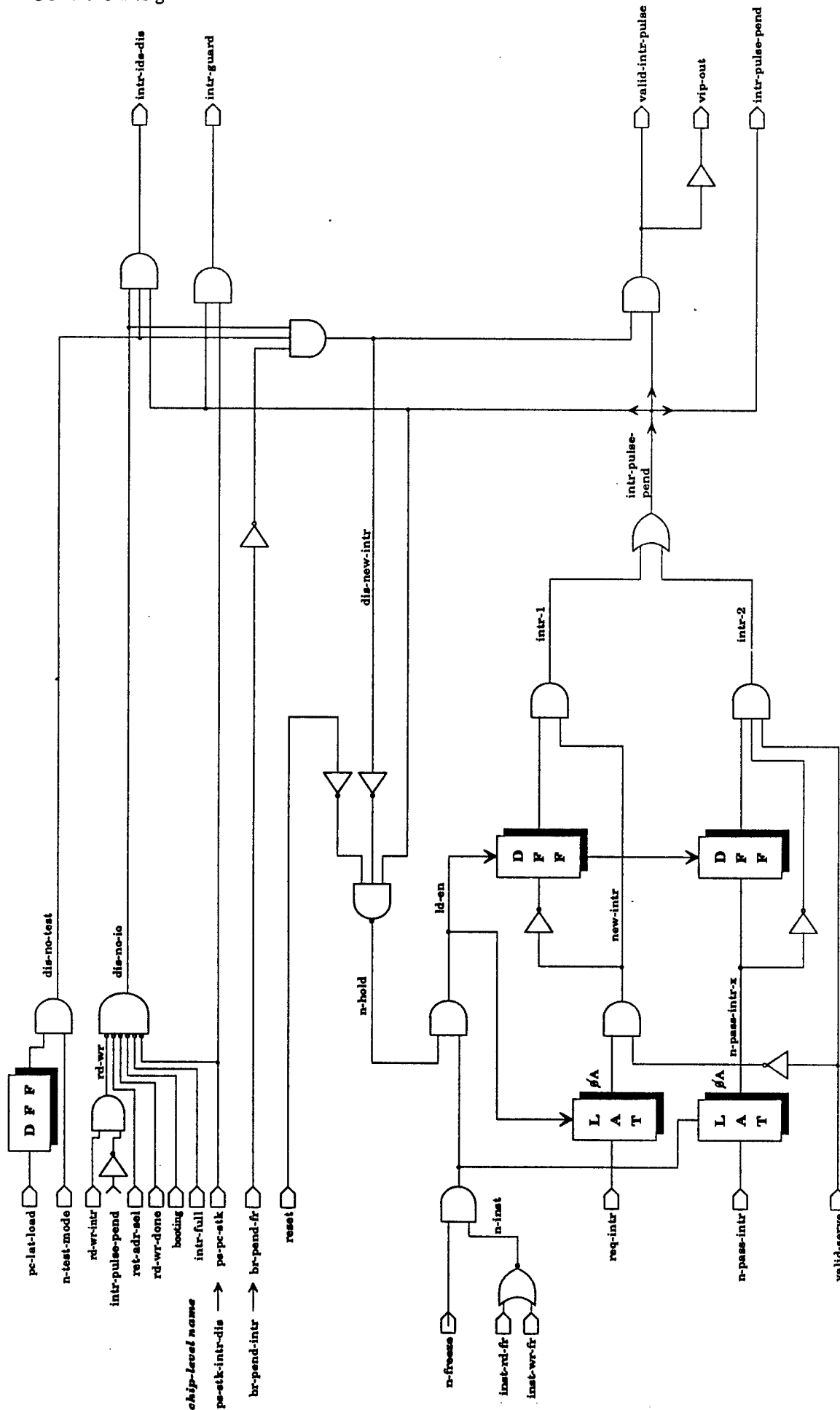


intr-mod
ld-ctrl

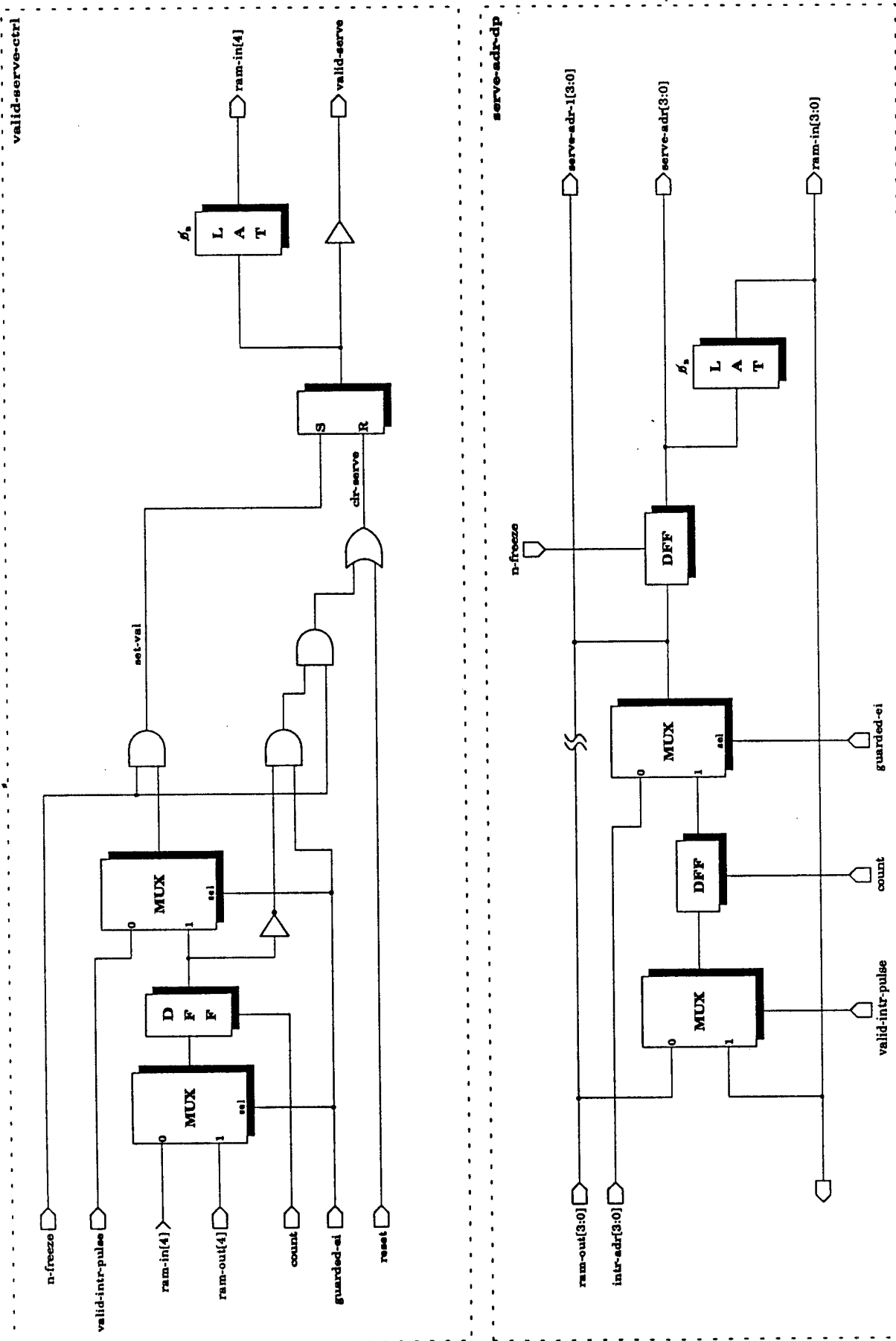
**intr-dp**



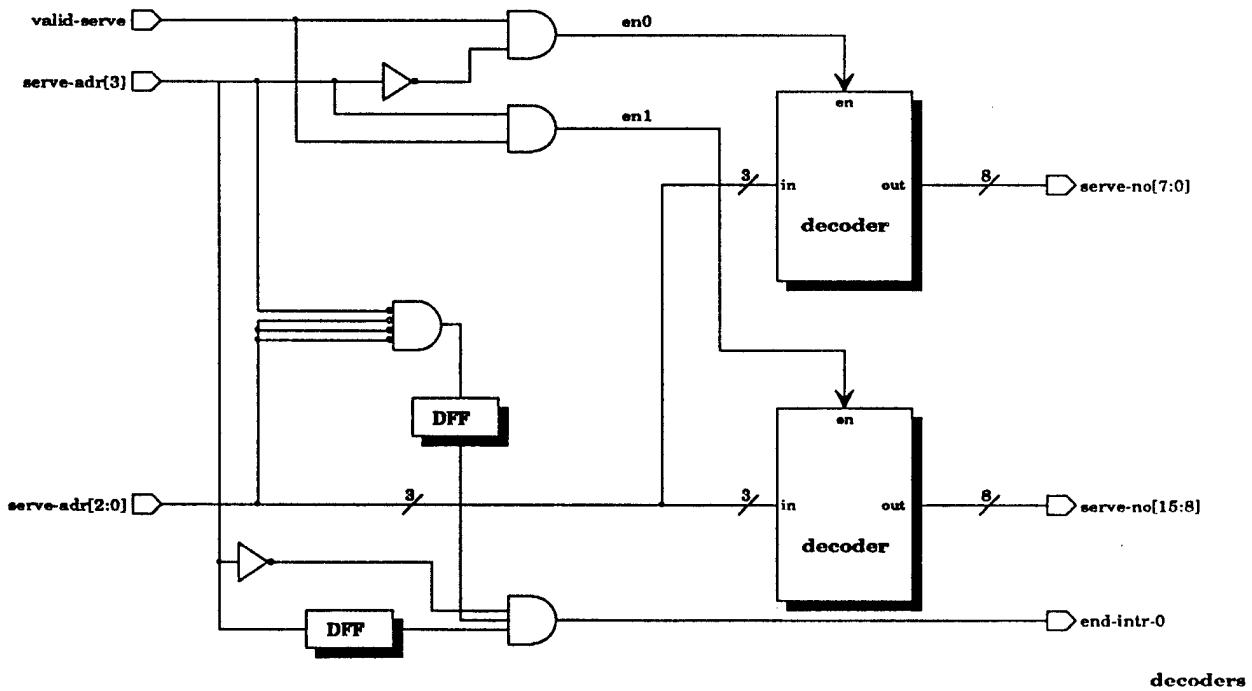
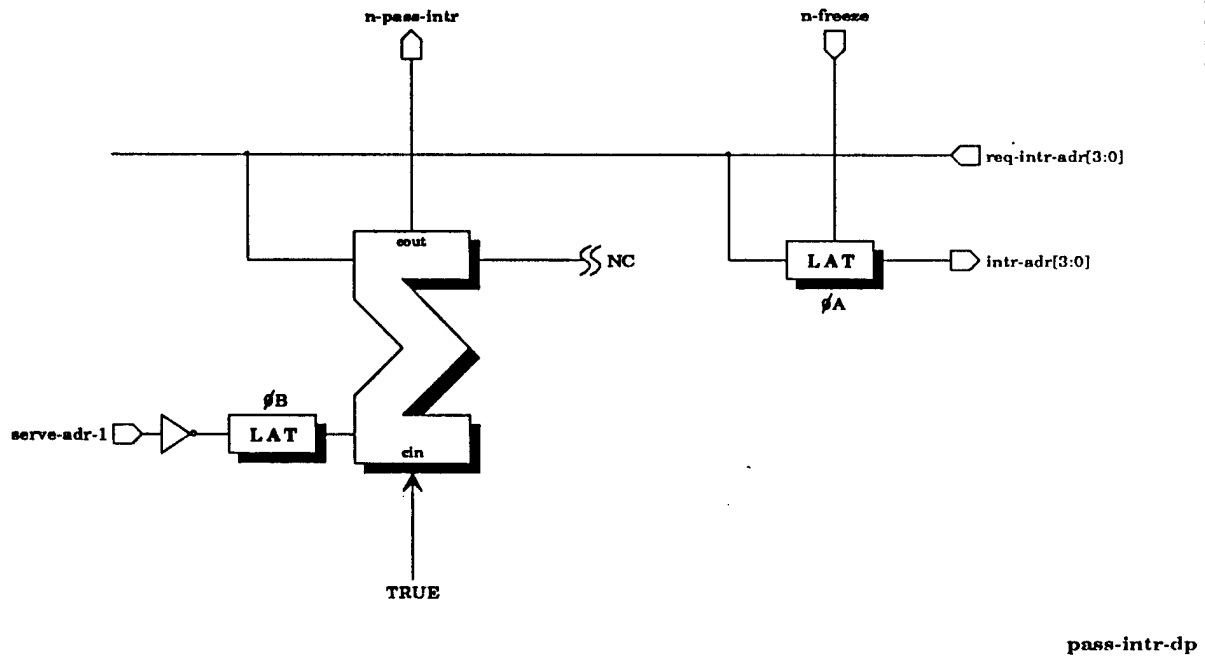
valid-intr-mod



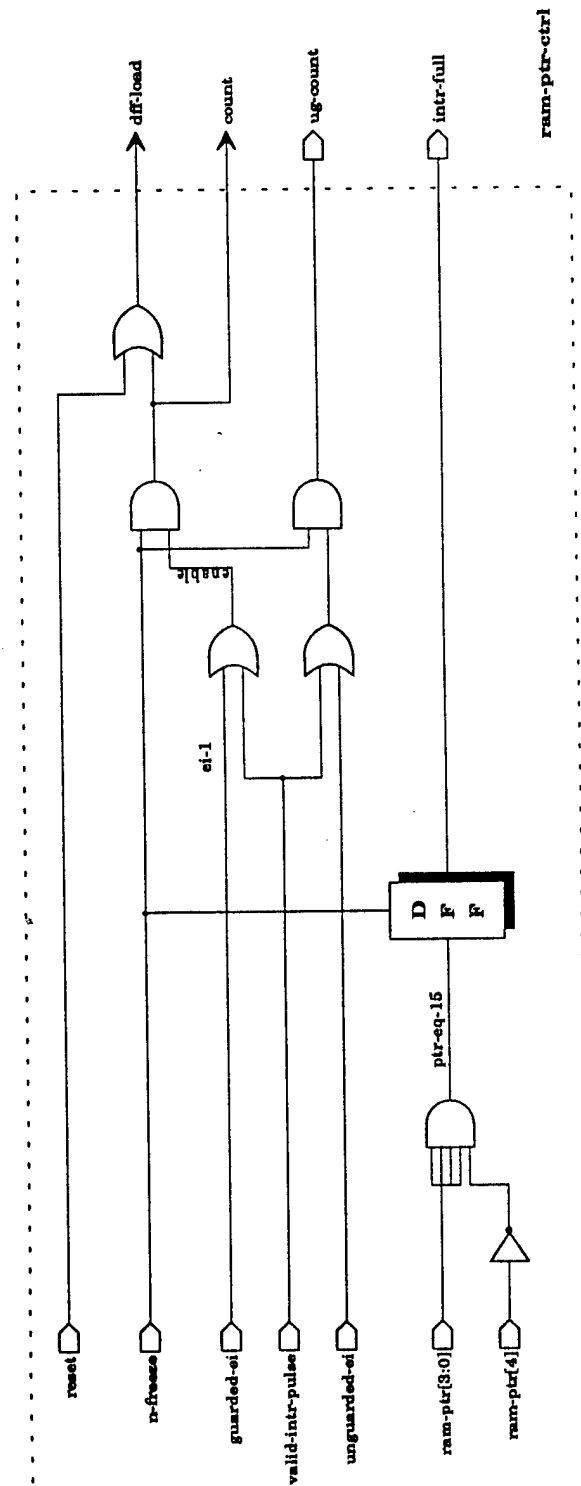
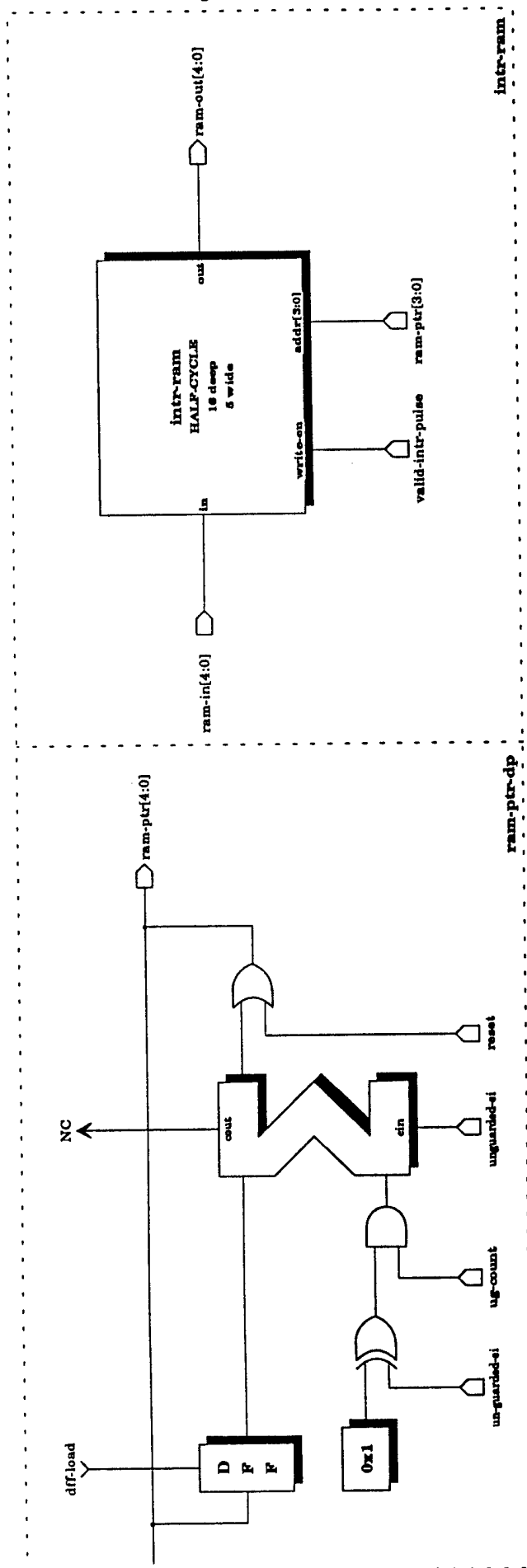
NOTE: "valid-intr-pulse" is used inside intr-mod
 "vip-out" is connected to "valid-intr-pulse"
 at the chip level



valid-serve-ctrl
serve-addr-dp

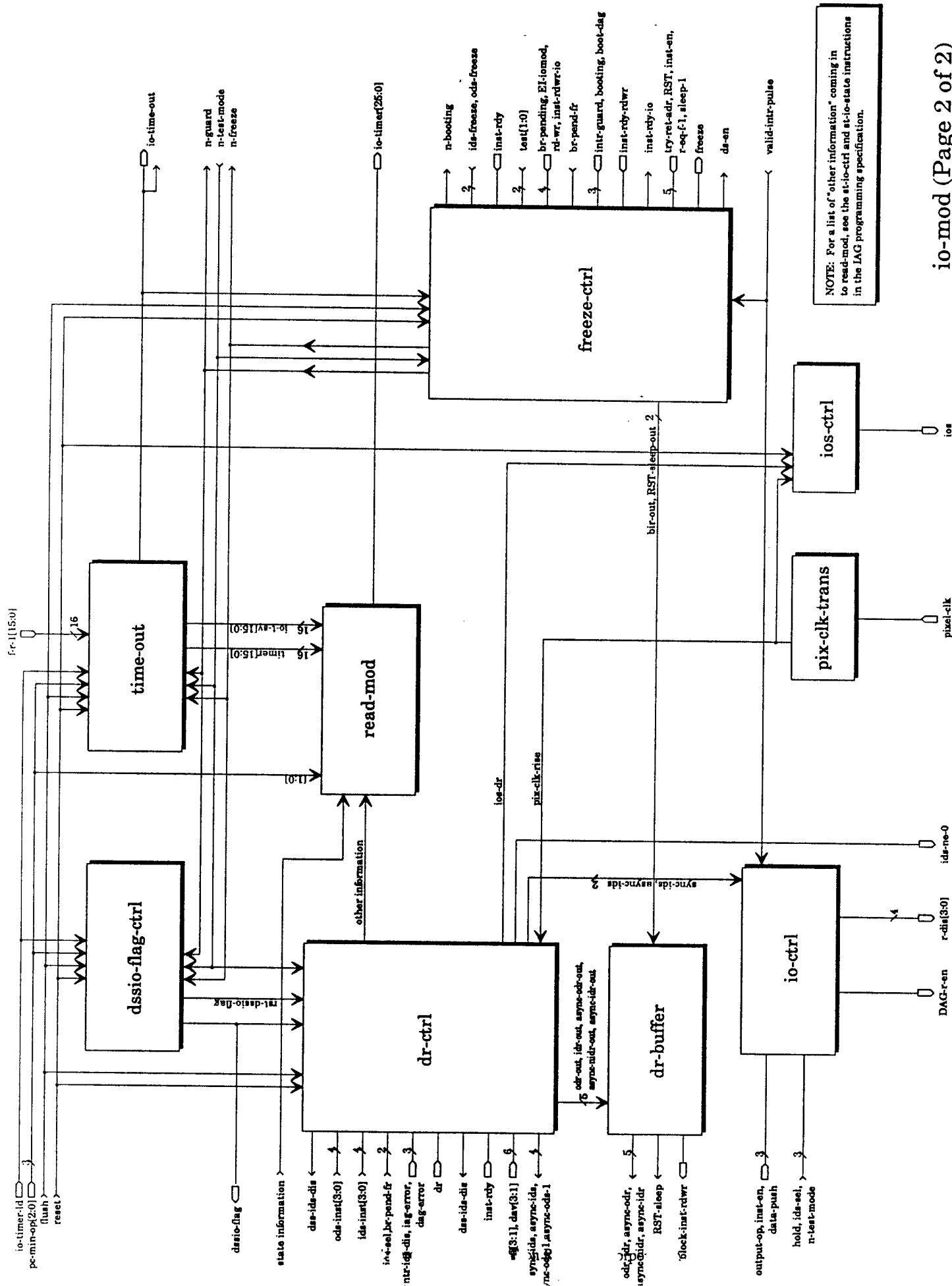


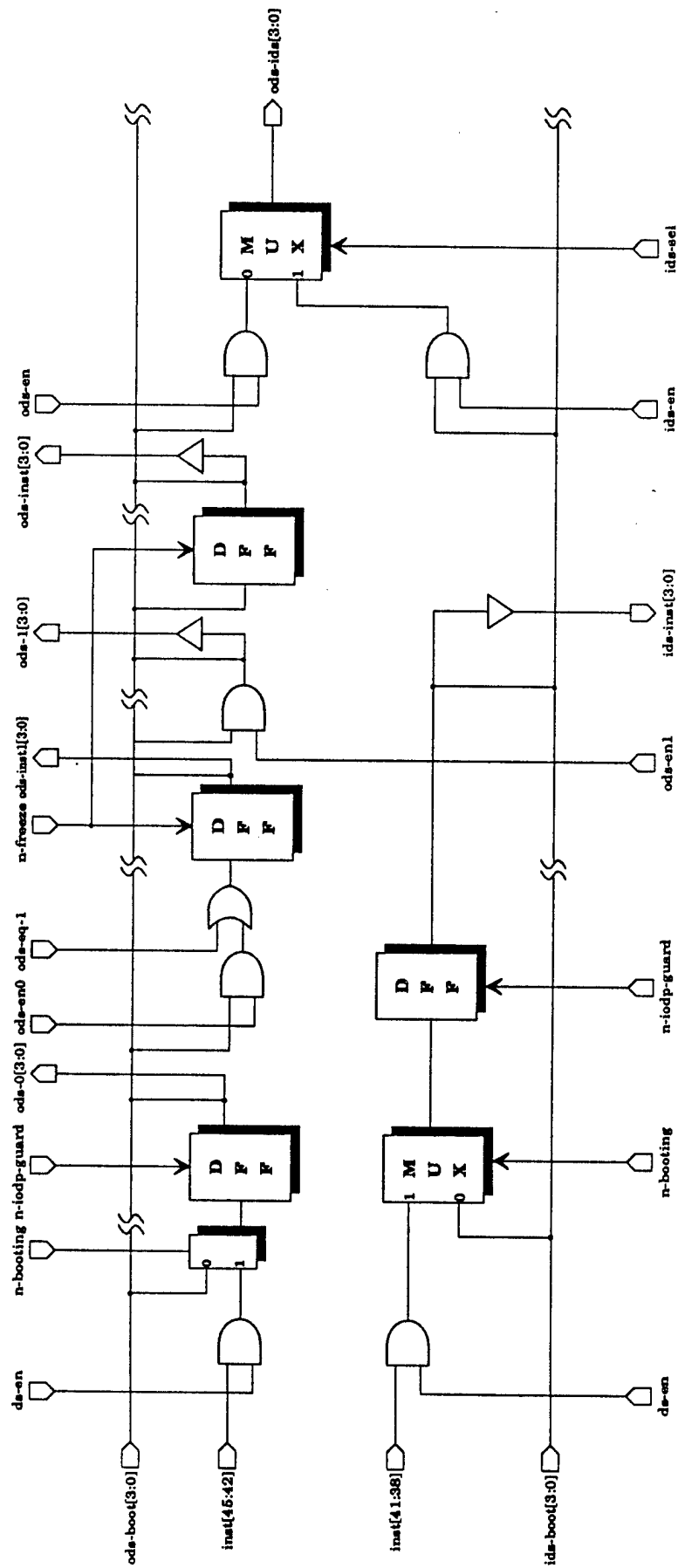
**pass-intr-dp
decoders**



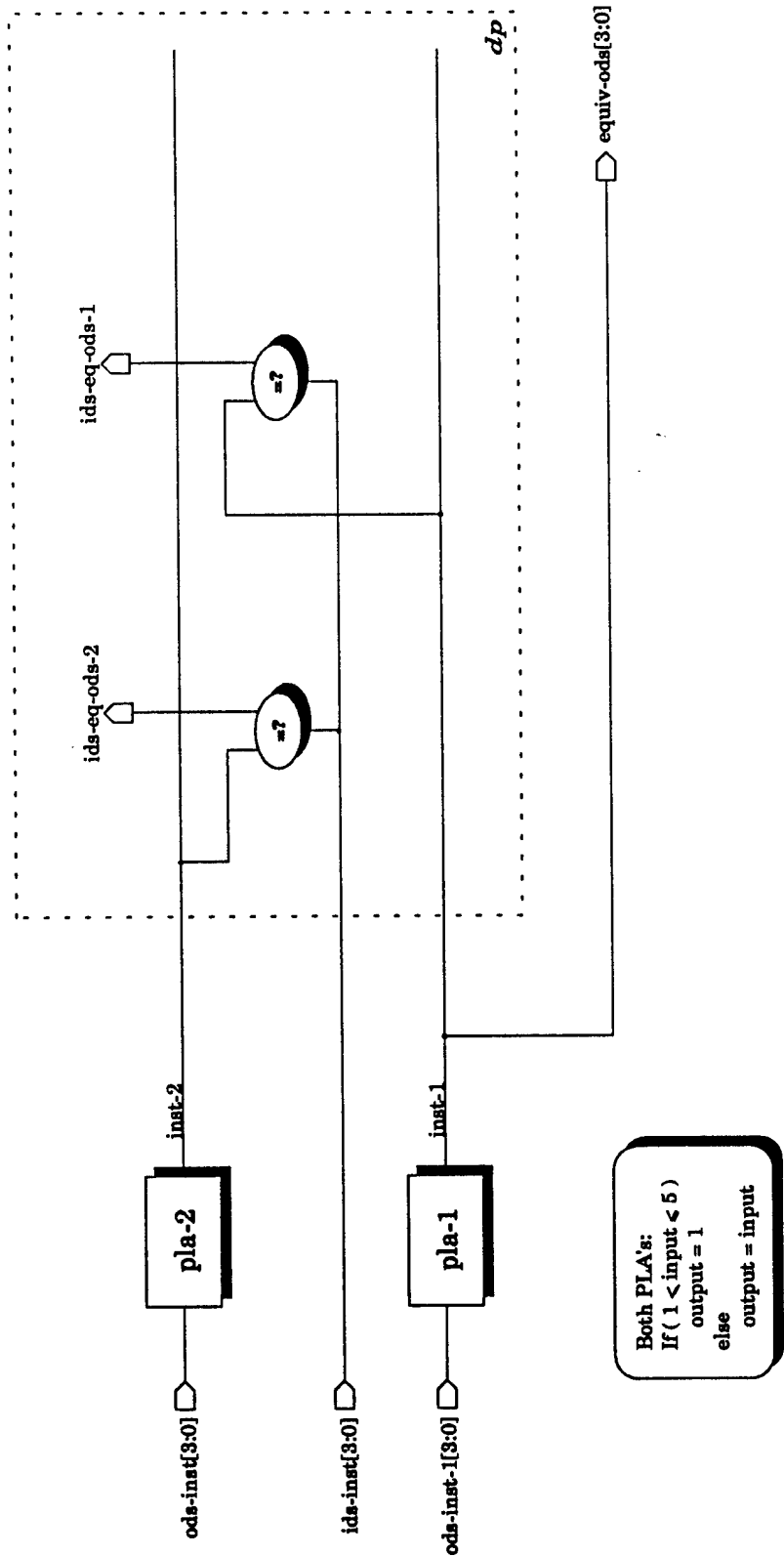
ram-ptr-dp







io-mod
io-dp



ds-dep-check-mod

```

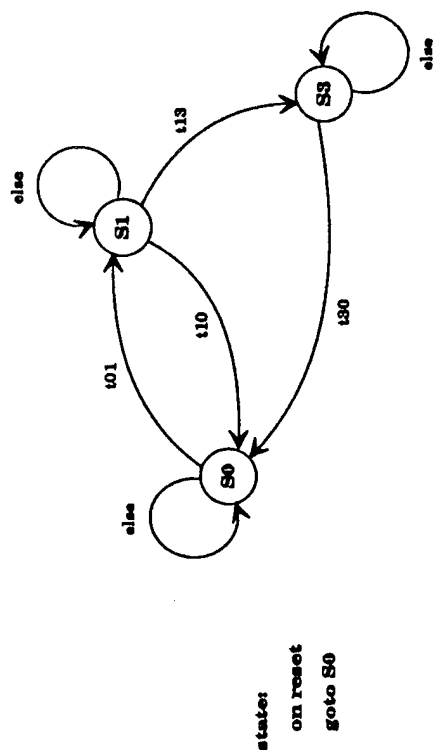
ods-en0      = ~BALU * ~flush * ~reset-1 * ~reset * ~valid-intr-pulse * n-guard
ods-en1      = ~flush * ~reset-1
ods-en       = ~async-ods-dis * ~sync-ods-dis * ~reset-1
ids-en       = ~async-ids-dis * ~sync-ids-dis * ~reset * ~flush * ~ds-ids-dis * ~reset1
dr-out-dis   = ods-ids[0] + ods-ids[1] + (ao * a1 * ao * a0) + (a1 * a1 * a1 * a0)
ods-freeze-in = sync-ods-fr + async-ods-fr
ids-freeze-in = sync-ids-fr + async-ids-fr
br-pend-fr   = (ids-inst[3] + ids-inst[2] + ids-inst[1]) * br-pending
              (reset-1 = Z' reset)
br-pend-intr = (ids-inst[3] + ids-inst[2] + ids-inst[1]) * BALU . 1
ods-eq-1     = BALU * ~flush * ~reset * ~reset-1 * ~booting * n-guard

```

Note: "ai - a1,0" is the state of async-ids-ctrl
 "ao - a1,0" is the state of async-ods-ctrl

io-mod
 ds-ctrl

Input: idr , $sync-ids$, $dag-error$, $valid-intr-pulse$, $io-time-out$, $ids-inst[3:2]$,
 $br-pending$, $inst-rdy$, $ids-sel$, $flush$, $inst-rd-fr$, $inst-wr-fr$, $lag-error$



state:

on reset

goto S0

Output:

ctrl: $sync-ids-dis = sync-ids * \neg flush * \neg idr-en + S2 + S3 + br-pend-fr$
 $sync-ids-fr = active-ids * idr-en * ids-sel * \neg idr + S1 * \neg idr-rdy + S3 * \neg valid-intr-pulse$

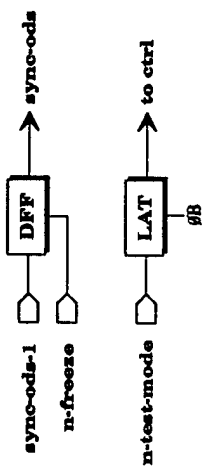
ctrl: $idr-en = \neg dag-error * \neg lag-error * \neg flush * \neg Z \neg reset * \neg inst-rd-fr * \neg inst-wr-fr * \neg Z \neg inst-rdy * \neg RST \neg sleep$
 $\neg (intr-ids-dis * \neg br-pend-fr) * \neg test-mode$
 $ids-rdy = idr * idr-en * ids-sel$
 $active-ids = sync-ids * \neg flush * ids-sel * \neg br-pend-fr$

transition:

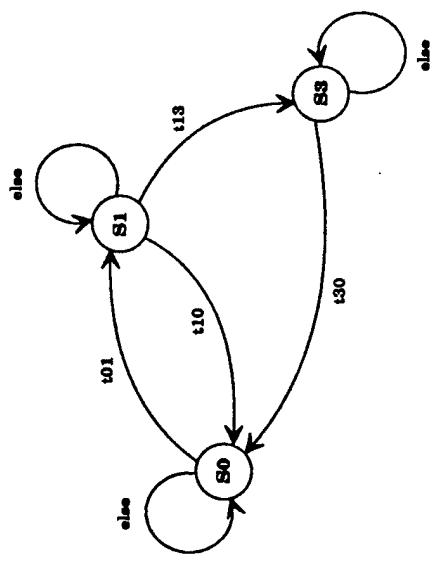
t01 = $(active-ids * \neg idr-rdy * idr-en * ids-sel) * \neg test-mode$
t10 = $ids-rdy * \neg test-mode$
t13 = $(\neg idr-rdy * io-time-out) * \neg test-mode$
t30 = $(valid-intr-pulse) * \neg test-mode$

io-mod
 sync-ids-ctrl

Input: odr, sync-ods, dag-error, lag-error, valid-intr-pulse, io-time-out,
inst-rdy, ids-sel, flush, inst-rd-fr, inst-wr-fr, prepare-intr



ctrl:
$$\begin{aligned} \text{odr-en} &= Z' (-\text{dag-error-in} * -\text{lag-error-x} * \\ &\quad -\text{reset} * \text{inst-rdy}) * -S2 * -\text{test-mode} \\ \text{ods-rdy} &= \text{odr} * \text{odr-en} * -Z' \text{ids-sel} \\ \text{active-ods} &= \text{sync-ods} * -(\text{ids-sel} * Z' \text{ids-sel}) \end{aligned}$$



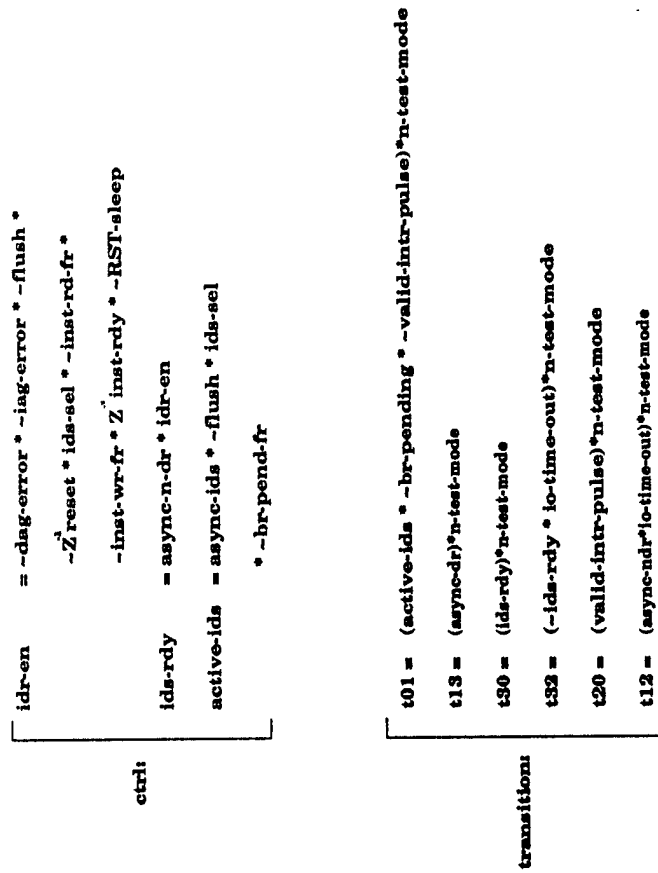
state:
on reset
goto S0

transition:
$$\begin{aligned} t01 &= (\text{active-ods} * -\text{ods-rdy} * \text{odr-en} * -Z' \text{ids-sel}) * \text{n-test-mode} \\ t10 &= (\text{ods-rdy}) * \text{n-test-mode} \\ t13 &= (-\text{ods-rdy} * \text{io-time-out}) * \text{n-test-mode} \\ t30 &= (\text{valid-intr-pulse}) * \text{n-test-mode} \end{aligned}$$

Output:

ctrl:
$$\begin{aligned} \text{sync-ods-dis} &= \text{sync-ods} * -\text{odr-en} + S2 + S3 \\ \text{sync-ods-fr} &= \text{active-ods} * \text{odr-en} * -Z' \text{ids-sel} * -\text{odr} * S0 + S1 * -\text{ods-rdy} + S3 * -\text{valid-intr-pulse} \end{aligned}$$

io-mod
sync-ods-ctrl



Input: idr, sync-ids, dag-error, lag-error, valid-intr-pulse, io-time-out,
inst-rdy, ids-sel, flush, inst-rd-fr, inst-wr-fr

Output:

ctrl:

```

async-ids-dis = S0 * async-ods * ~flush + S2 + br-pend-fr + s3
sample-int    = active-ids*async-dr*n-test-mode
hold-in       = active-ids*s3 * n-test-mode
async-ids-fr  = active-ids * S0 * ~valid-intr-pulse + S1 + S3 * ~ids-rdy + S2 * ~valid-intr-pulse
  
```

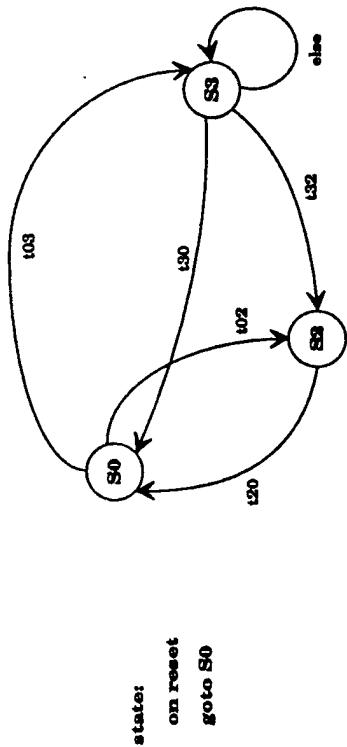
io-mod
async-ids-ctrl

ctrl:

odr-en = Z¹ (-dag-error-in * -lag-error-x *
-reset * inst-rdy) * Z¹ ids-sel
ods-rdy = async-dr * odr-en
active-ods = async-ods * -ids-sel

transition:

t03 = (active-ods * async-idr * odr-en) * n-test-mode
t30 = (-ods-rdy) * n-test-mode
t32 = (ods-rdy * io-time-out) * n-test-mode
t20 = (valid-intr-pulse) * n-test-mode
t02 = (-ods-rdy * io-time-out * active-ods) * n-test-mode



Input: odr, async-ods, dag-error, lag-error, valid-intr-pulse, io-time-out,
inst-rdy, ids-sel, flush, inst-rd-fr, inst-wr-fr, prepare-intr

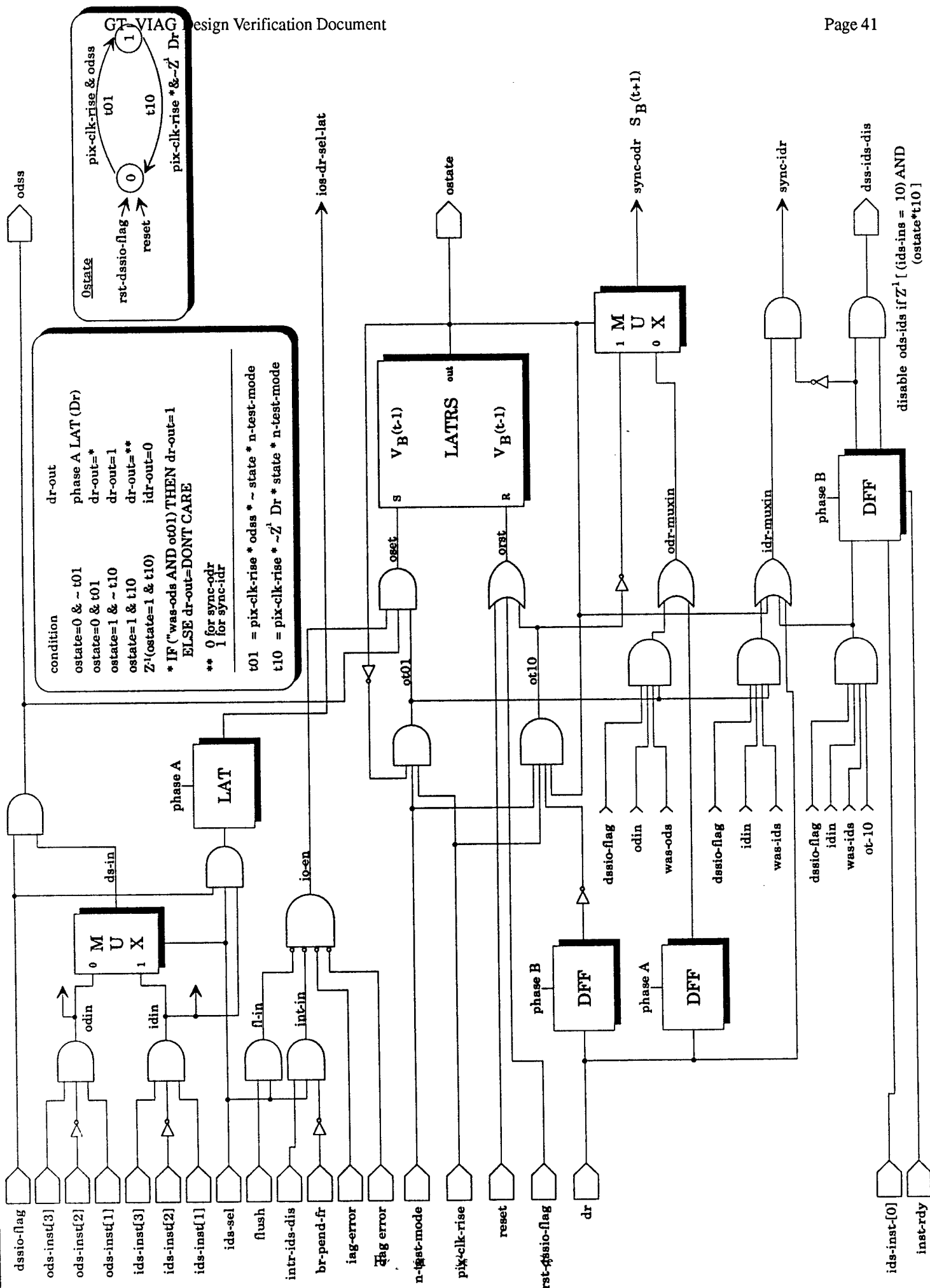


Output:

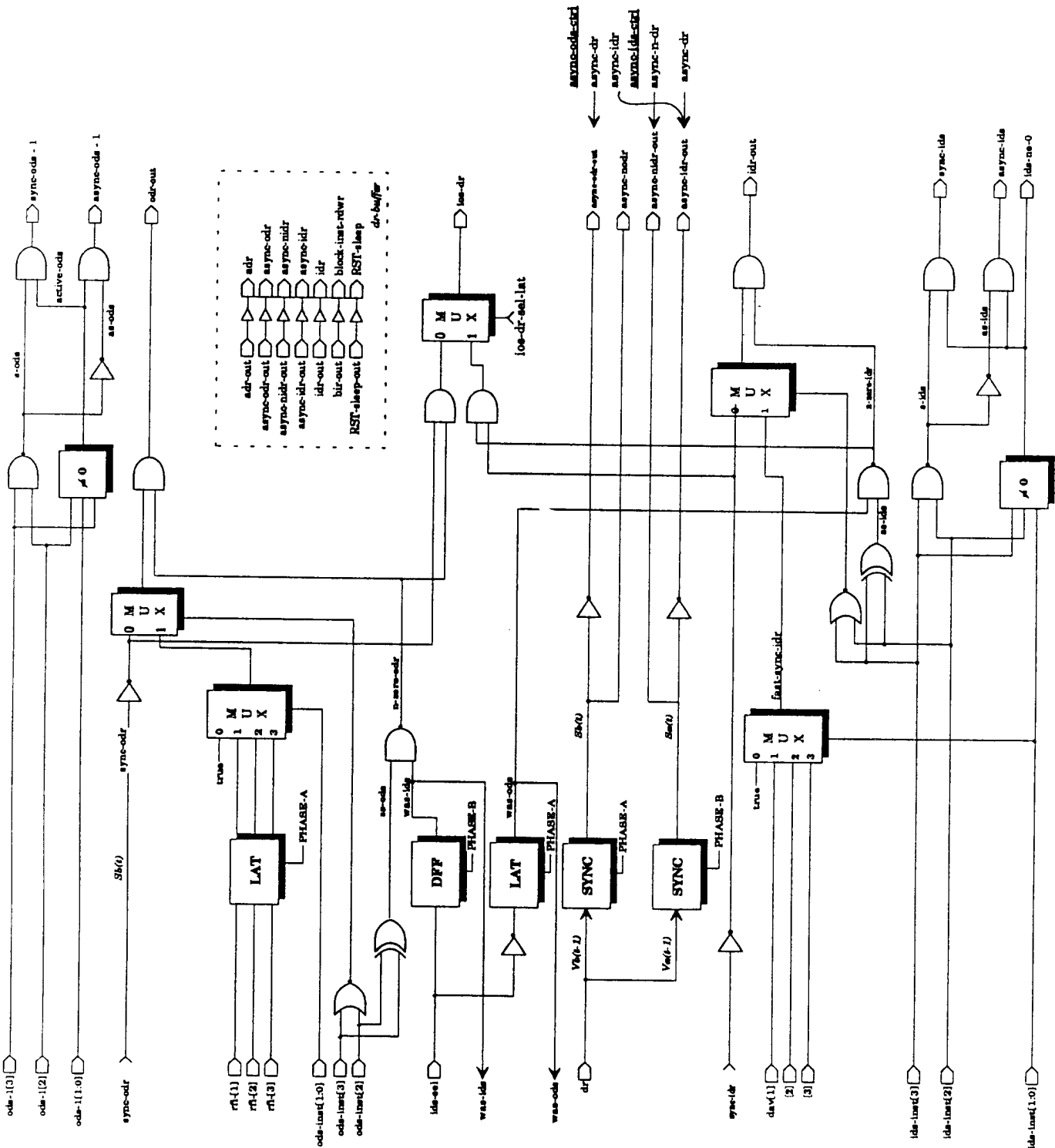
ctrl:

async-ods-dis = S2 + S3
async-ods-fr = active-ods * S0 + S3 * ods-rdy + S2 * -valid-intr-pulse

io-mod
async-ods-ctrl

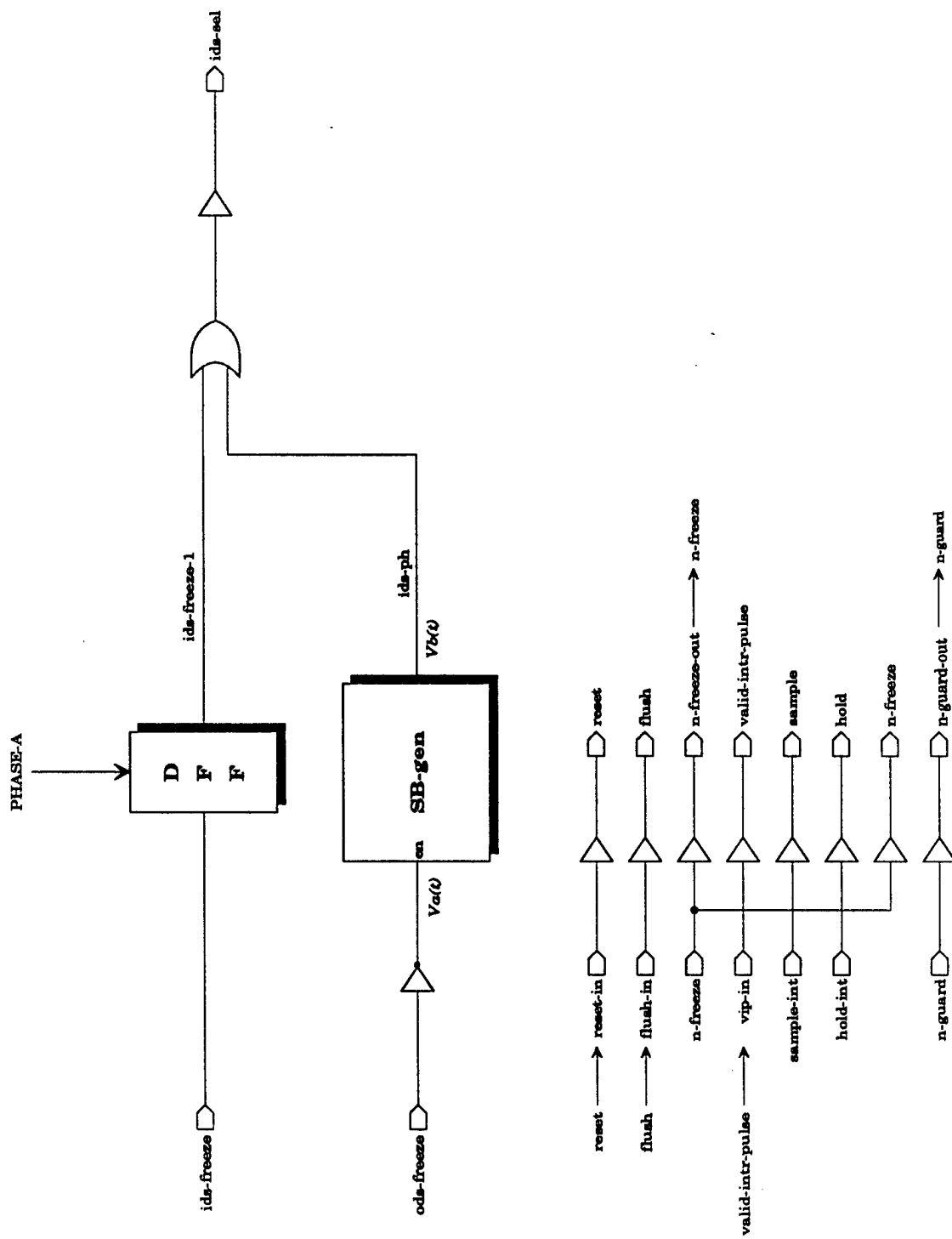


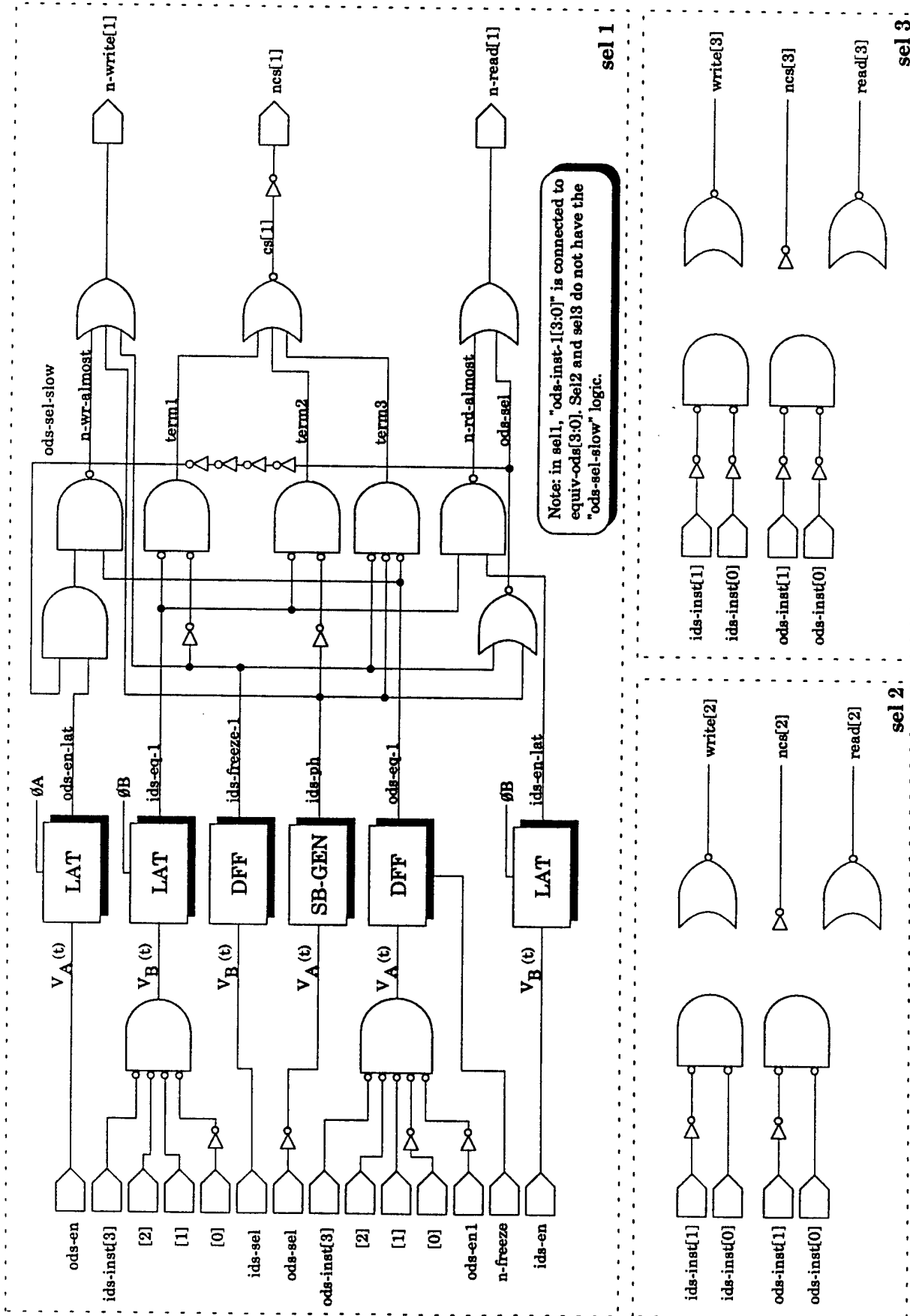
dr-ctrl (page 1 of 2)



dr-ctrl
(page 2 of 2)

WAGE VOUCHER SYSTEM



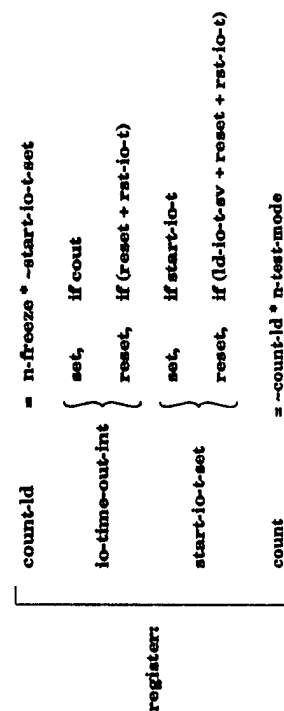
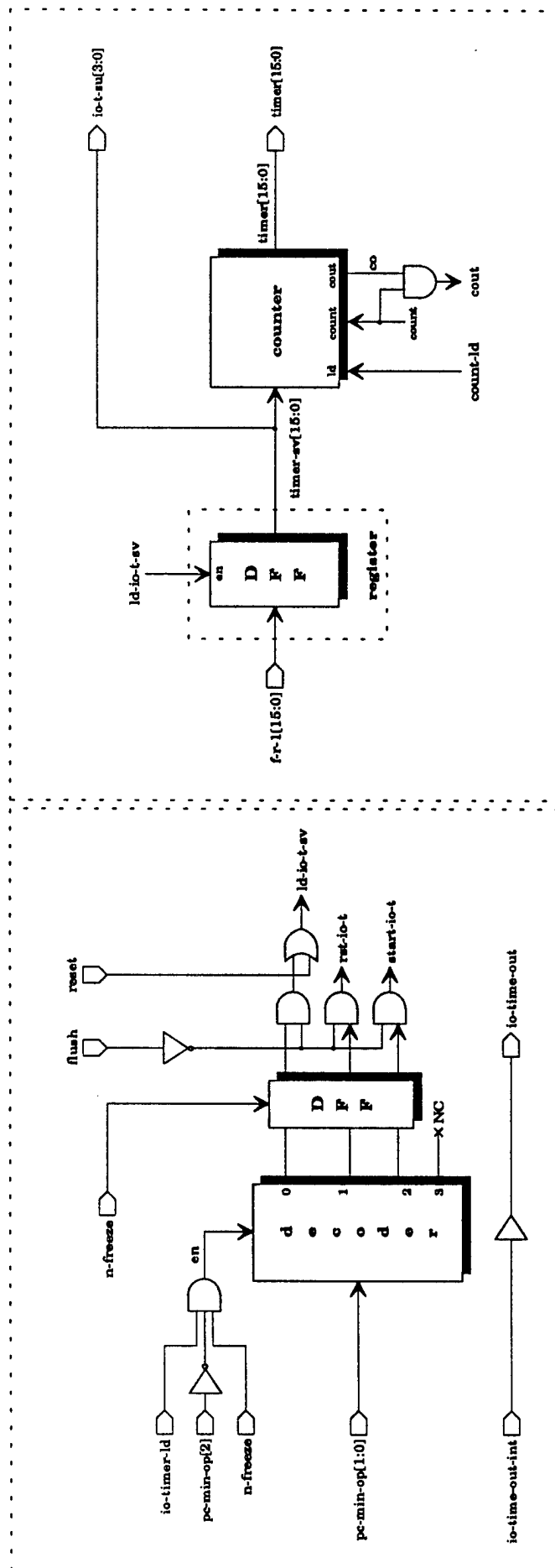


iomod

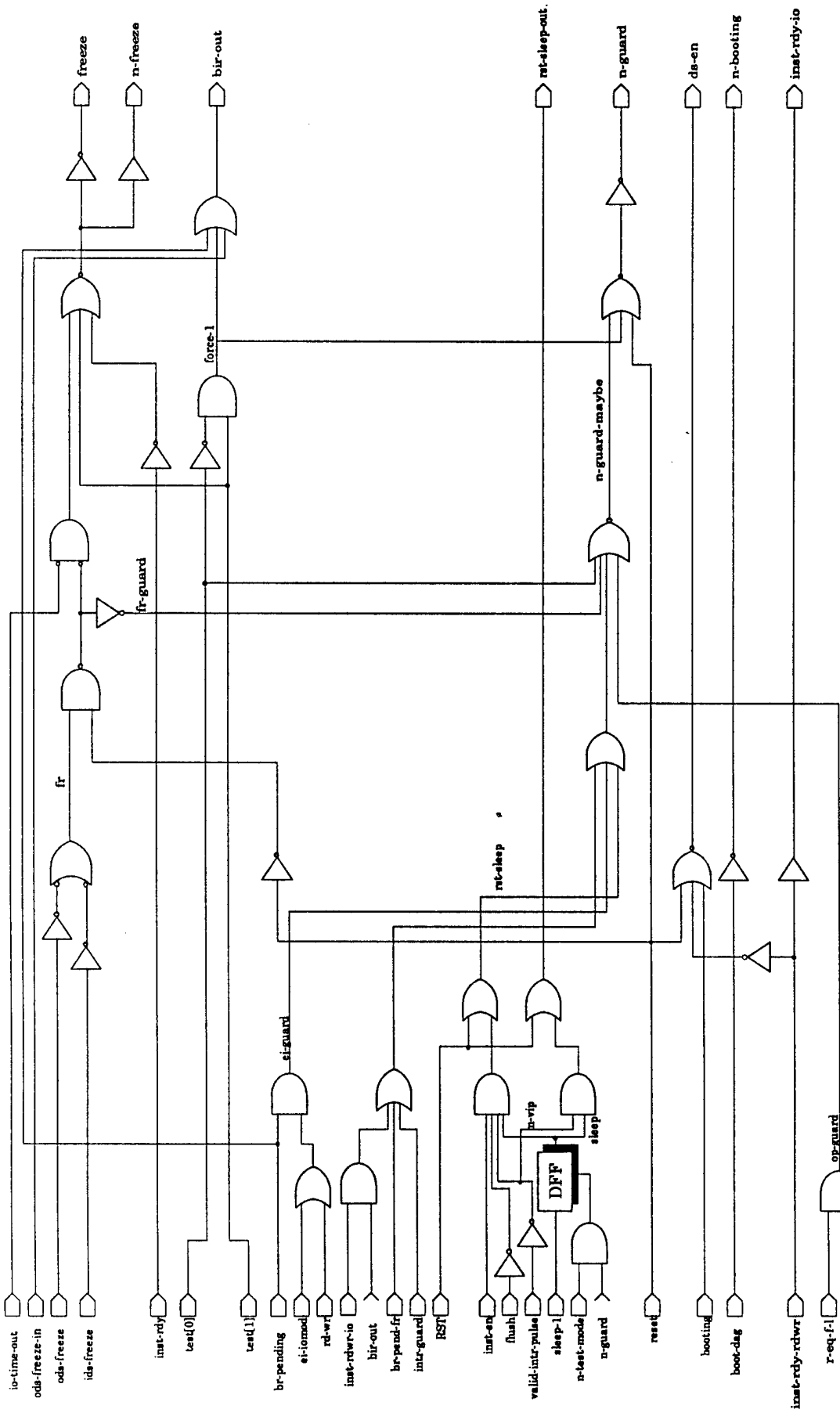
sel1,sel2,sel3

input: io-timer-ld, reset, so-intr-dis, si-intr-dis, so-intr-dis, n-freeze, n-valld-intr, f-r-1[15:0], pc-min-op[0]

output: io-timer[15:0], io-time-out



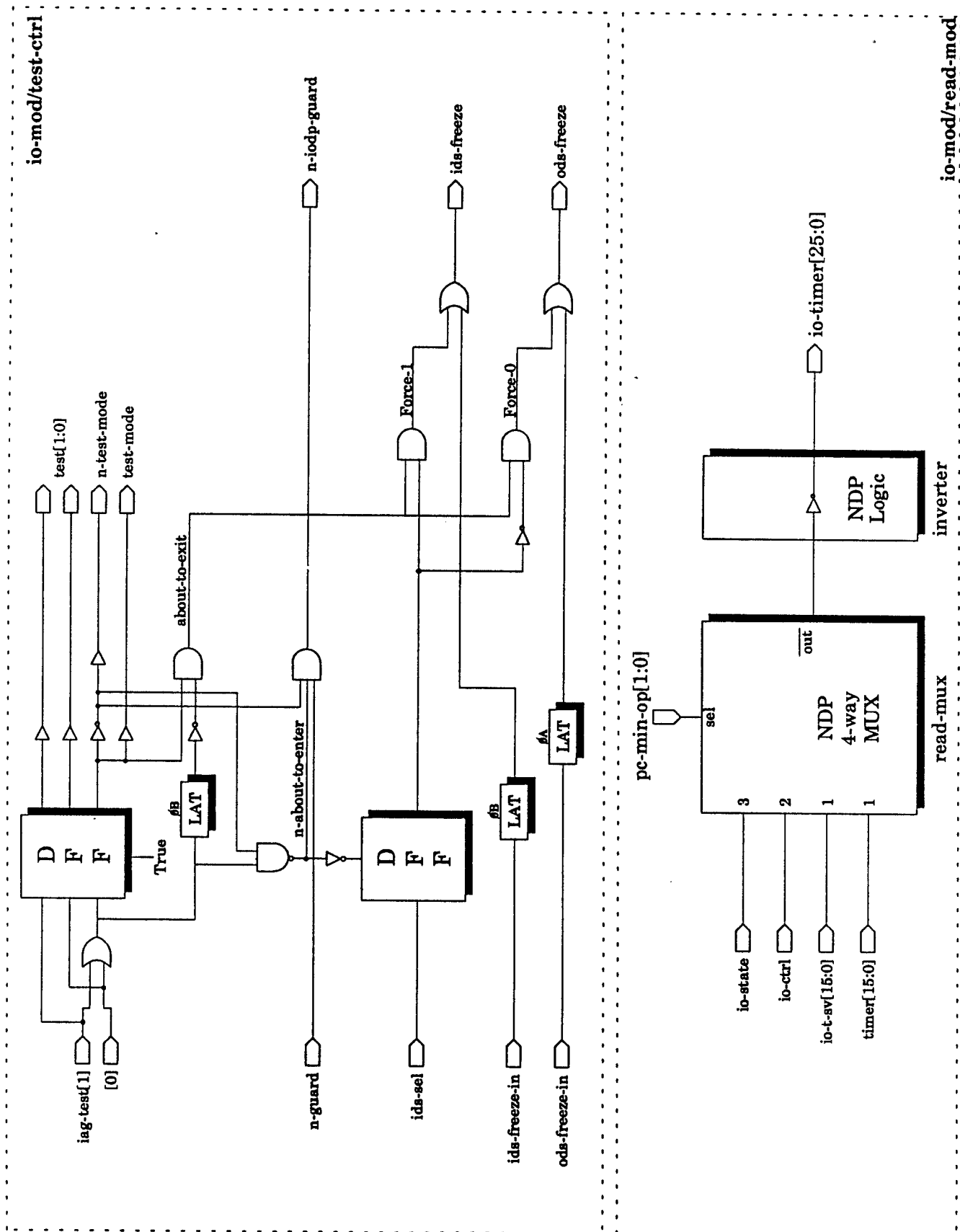
time-out

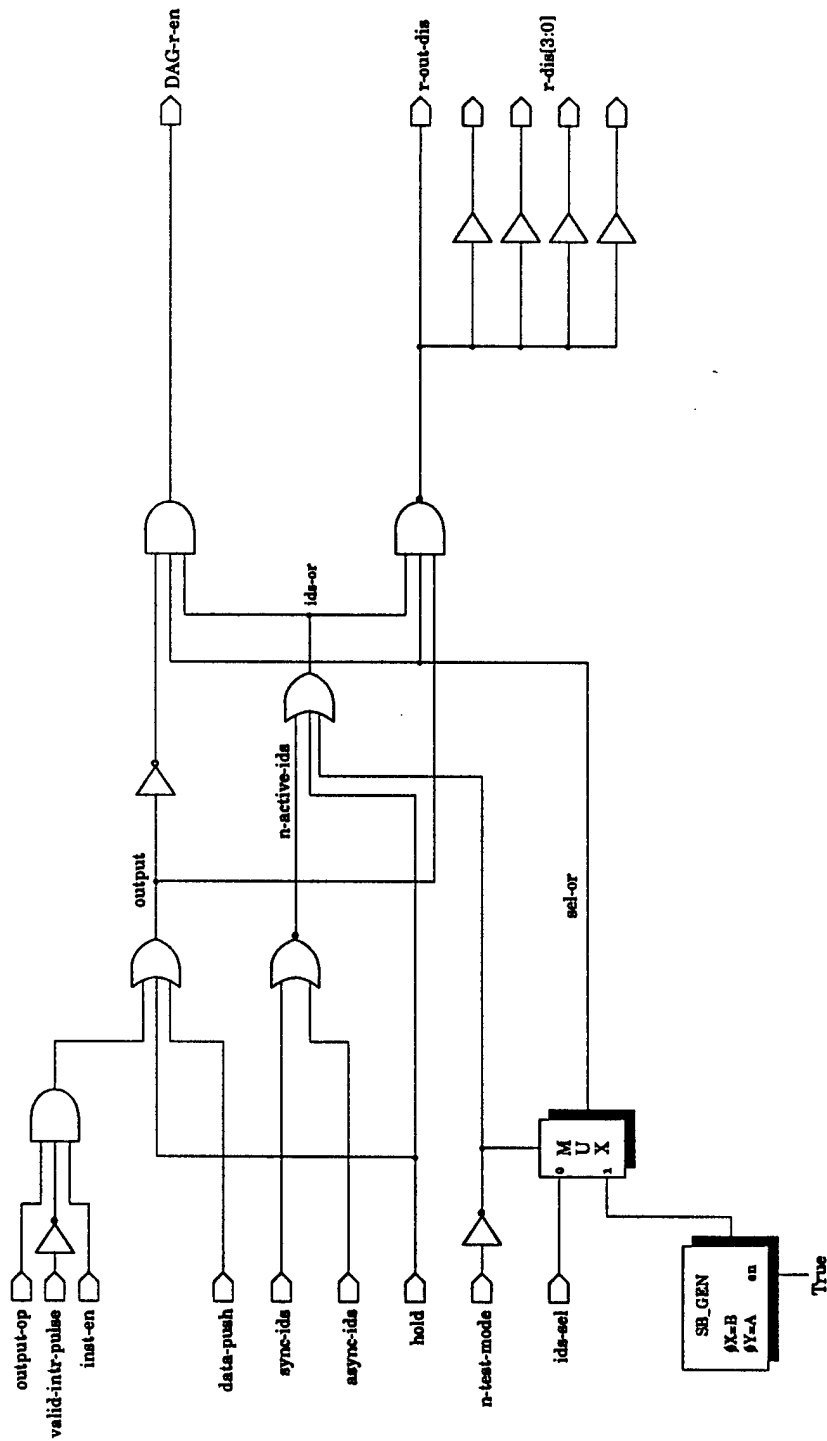


NOTE:
sync-ids-ctrl
sync-ods-ctrl
asyn-ids-ctrl
asyn-ods-ctrl
all use "Inst-rdy-io"
At the io-mod level, the netlist connects
"Inst-rdy-io" to their "Inst-rdy" input.

TEST	As is	Freeze	Guard
00	-	-	-
01	1	1	-
10	1	1	0
11	1	1	1

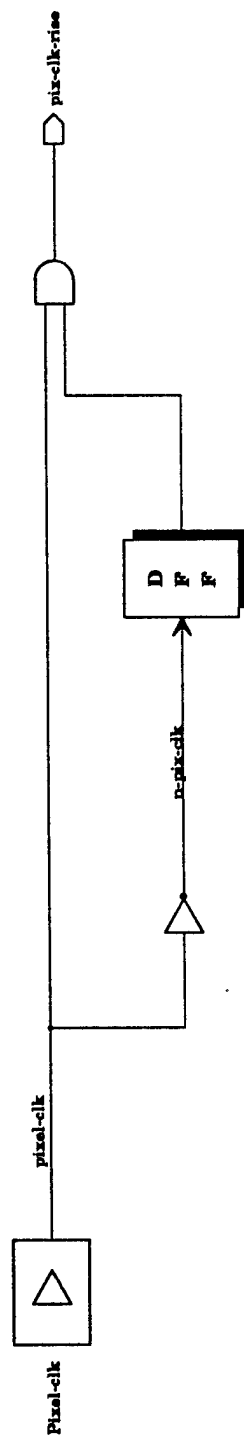
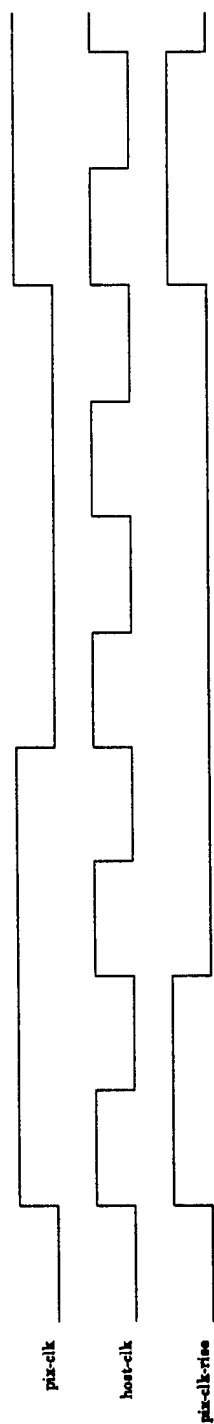
io-mod
freeze-ctrl



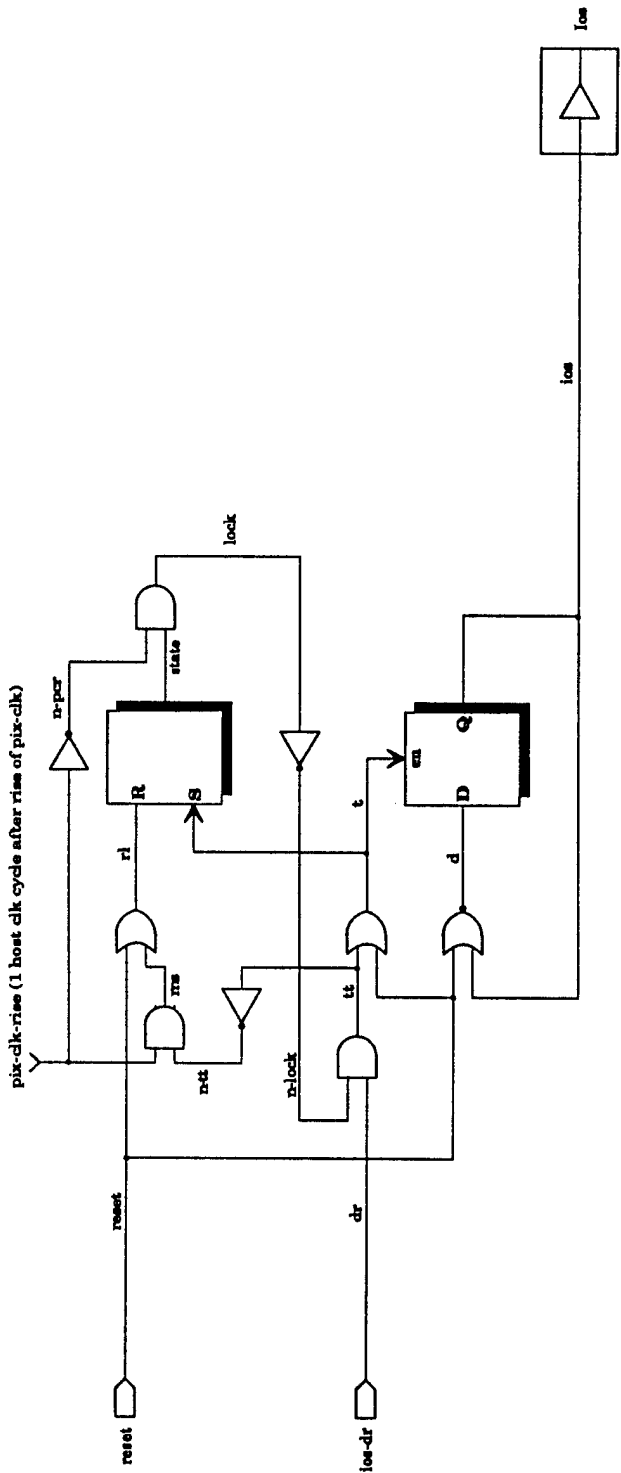


io-ctrl

1



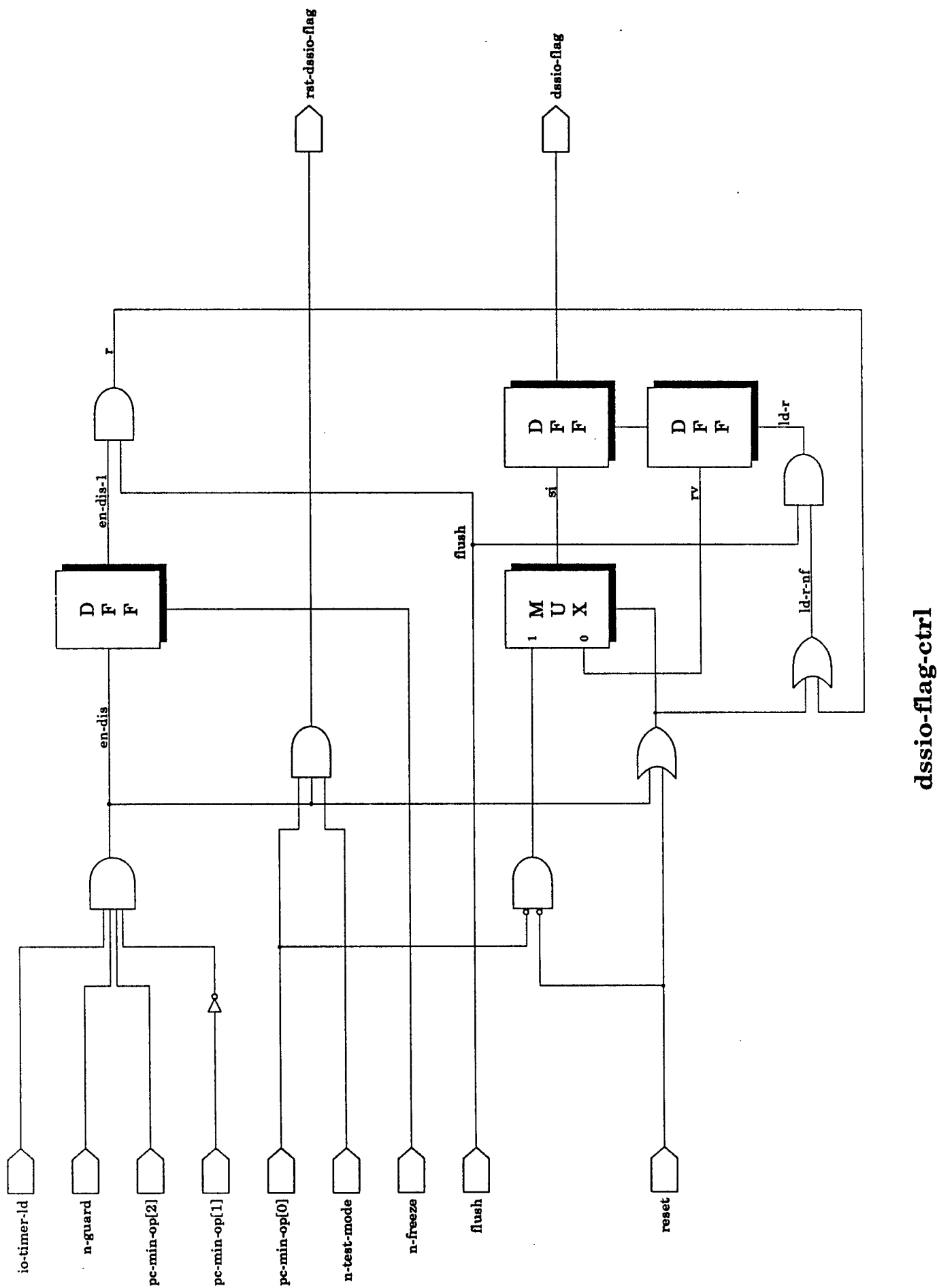
pix-clk-trans

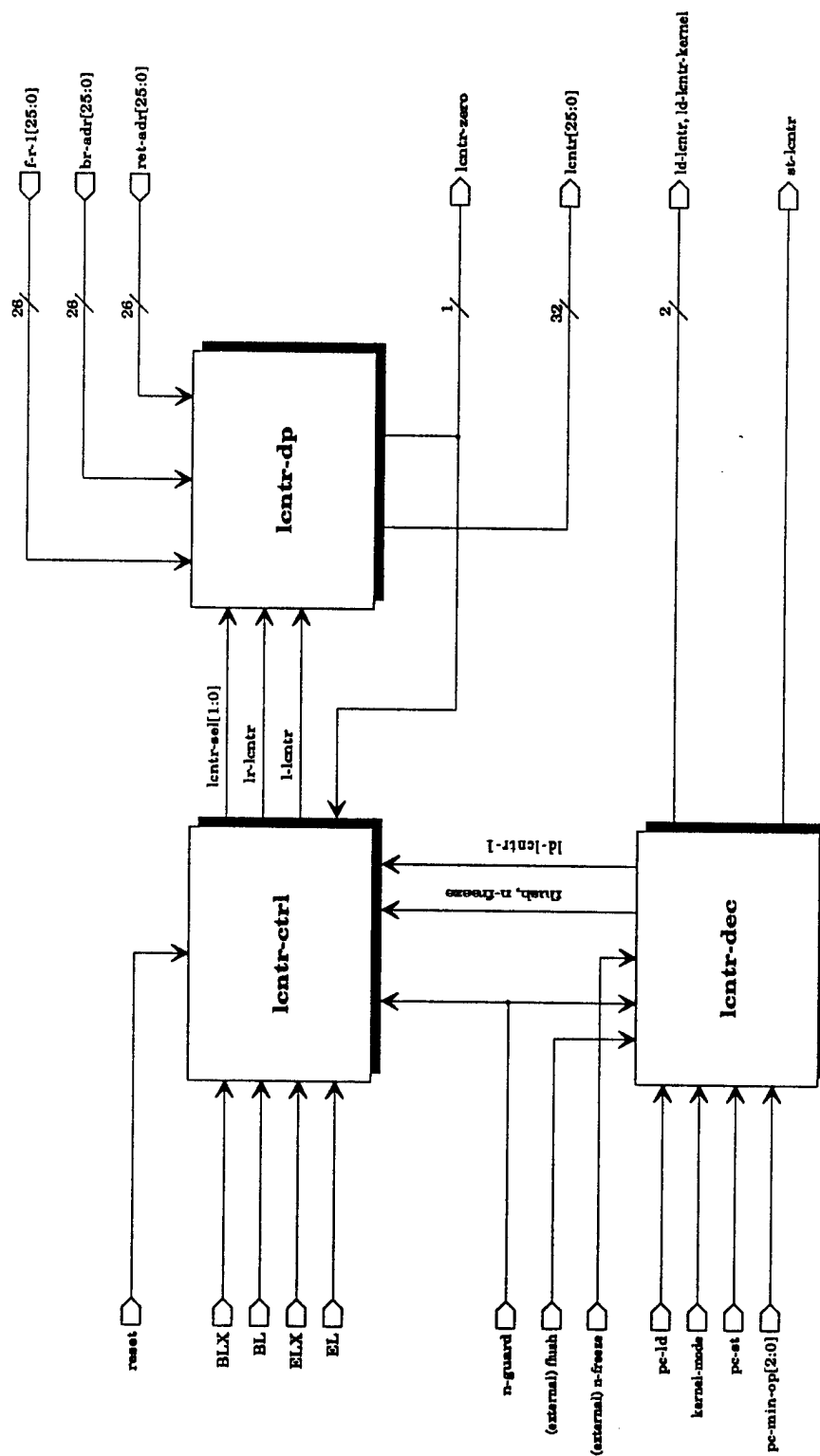


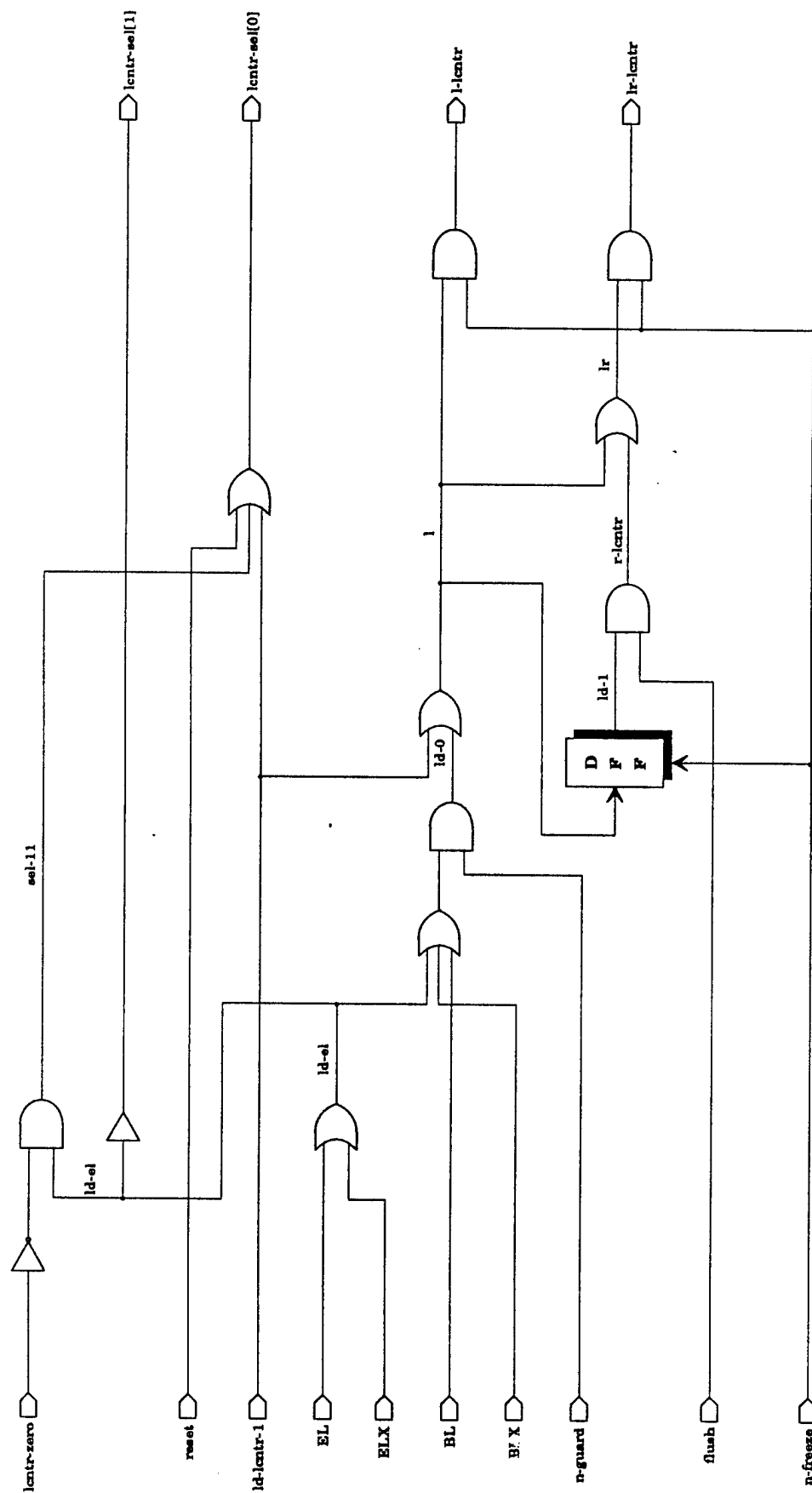
Transition : 1. OK if pix-el-clk 'sinco the last change of state
2. state changes on valid Dr

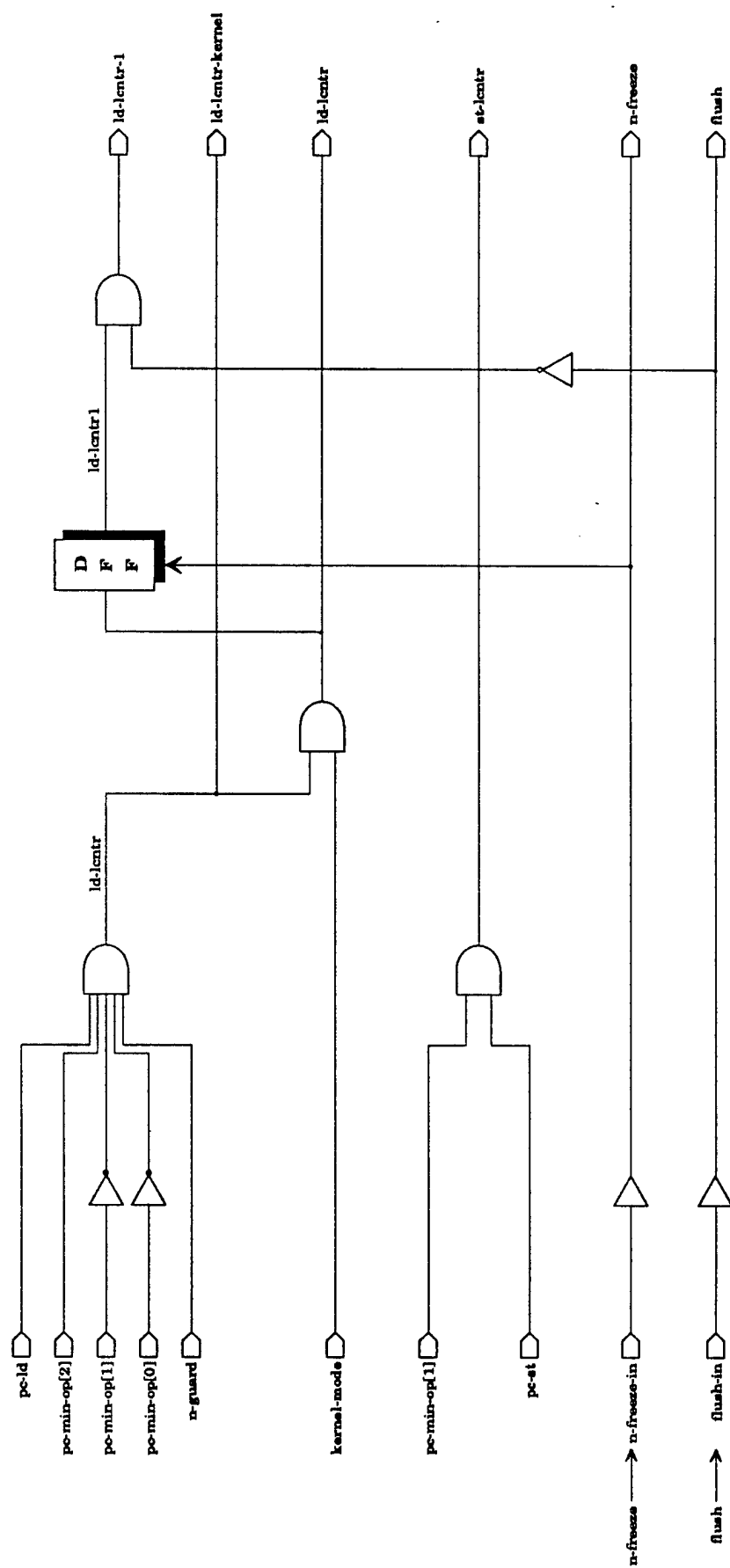


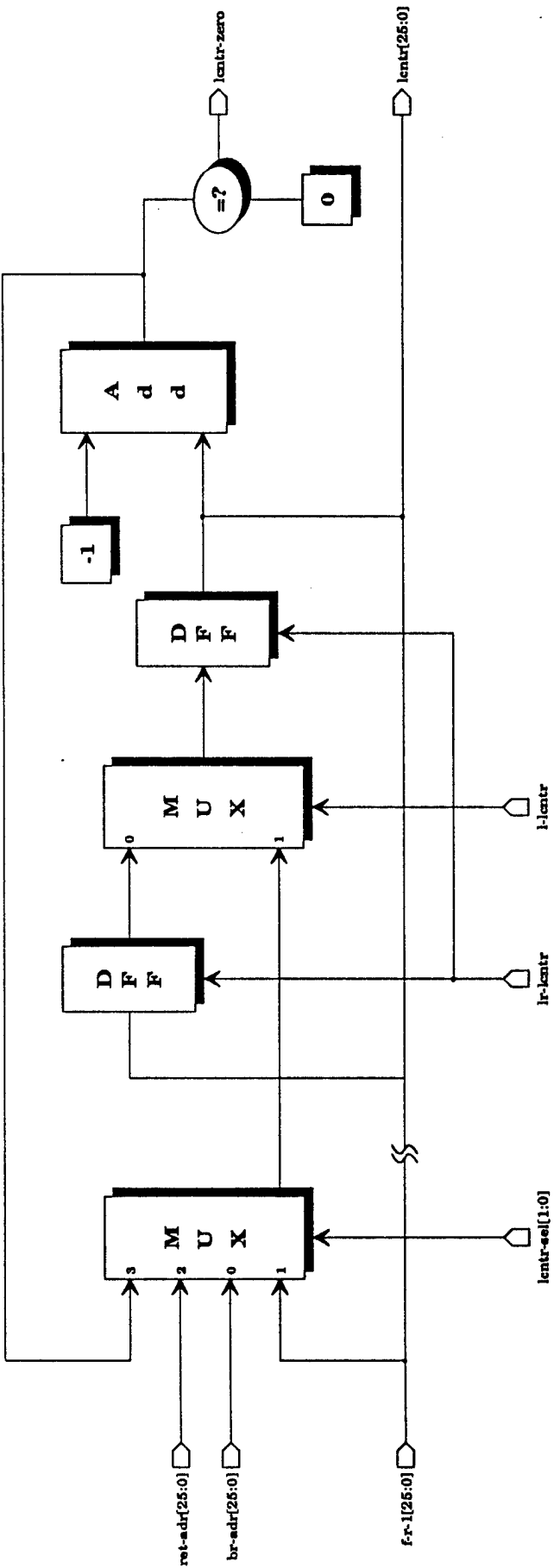
ios-ctrl





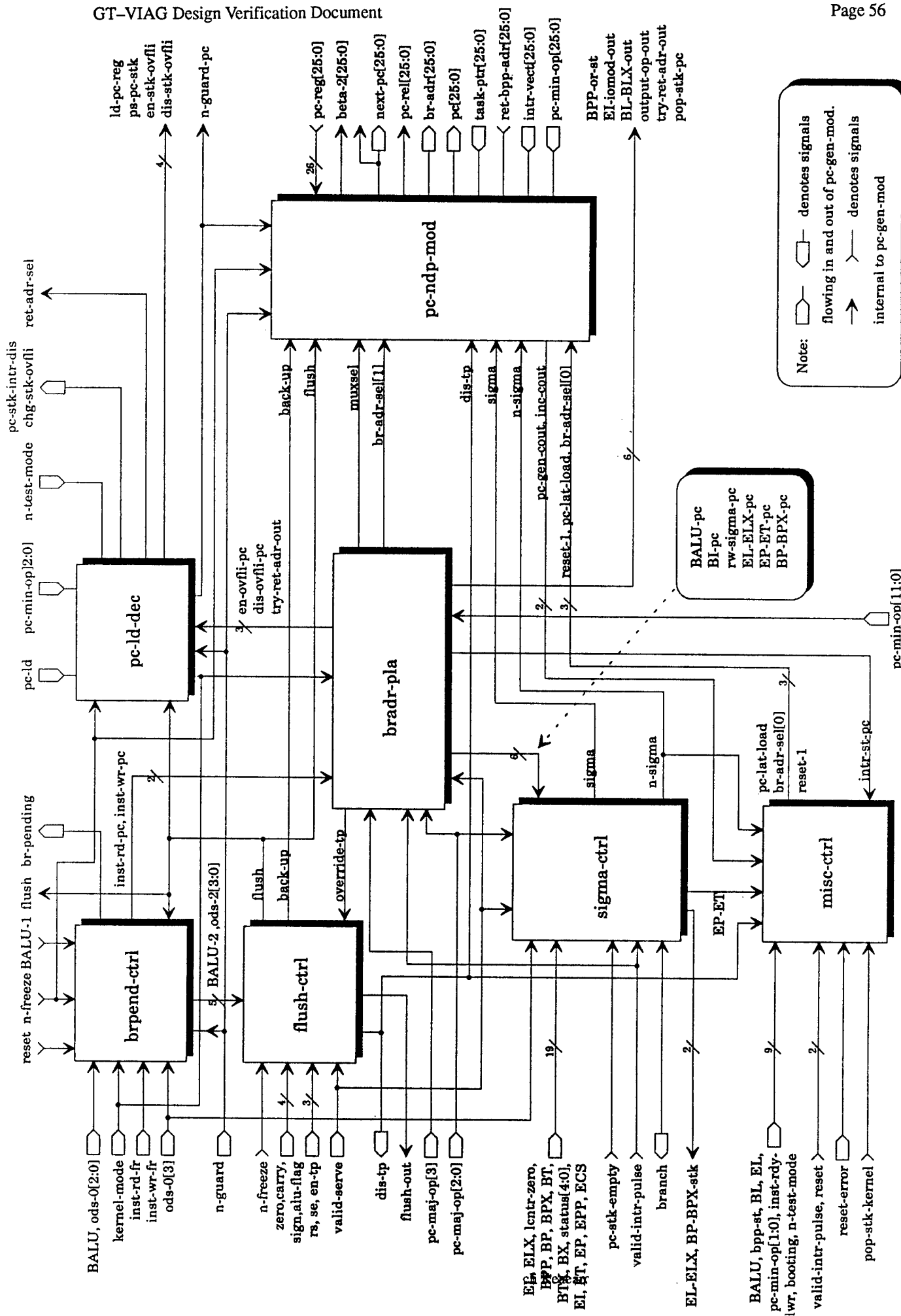
**lentr-ctrl**

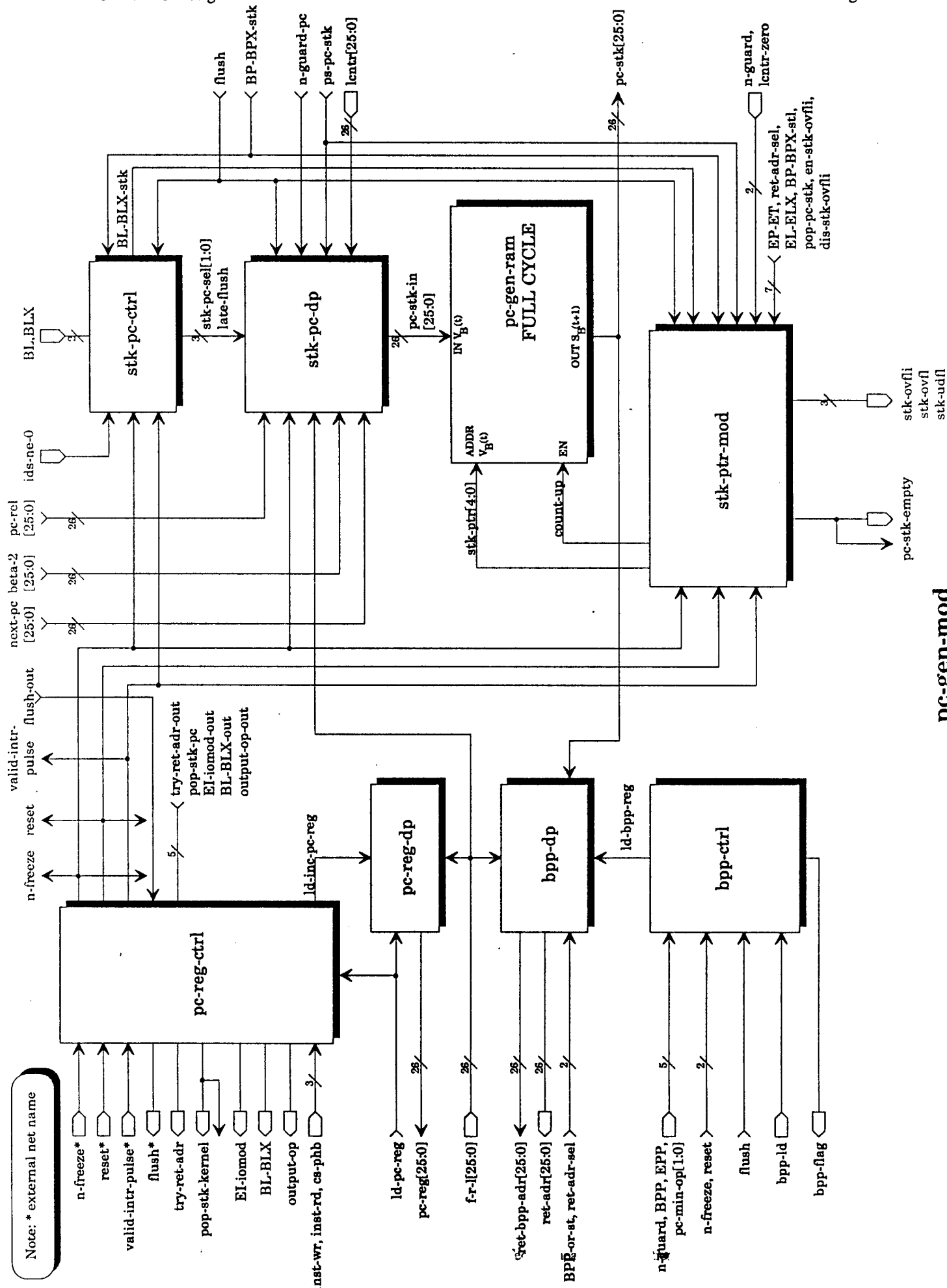
**lentr-dec**

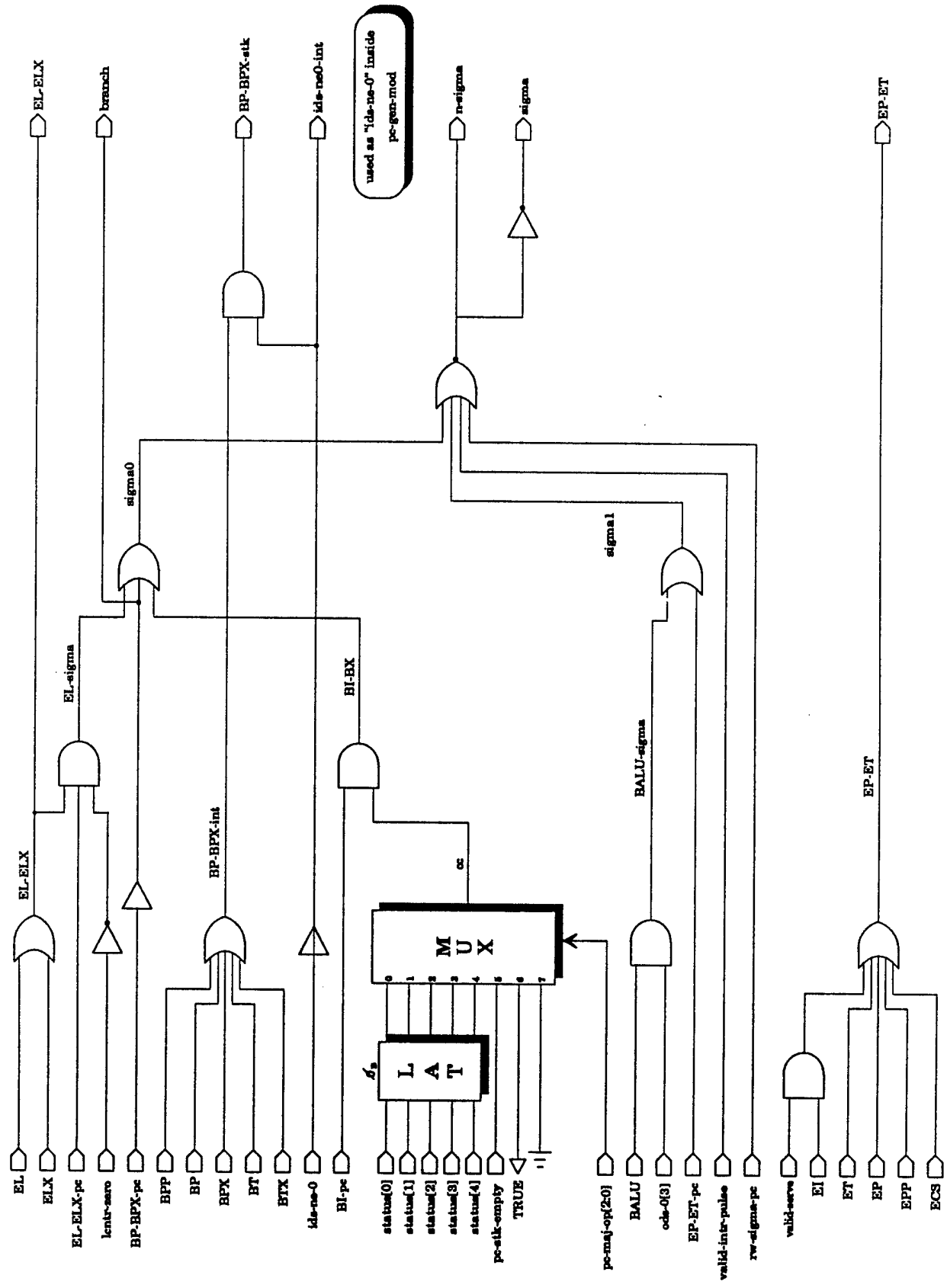


lentr-sel	condition
0 0	BL, BLX
0 1	ld-lentr-1, reset
1 0	(EL/ELX)^(lentr-zero)
1 1	(EL/ELX)^(not lentr-zero)

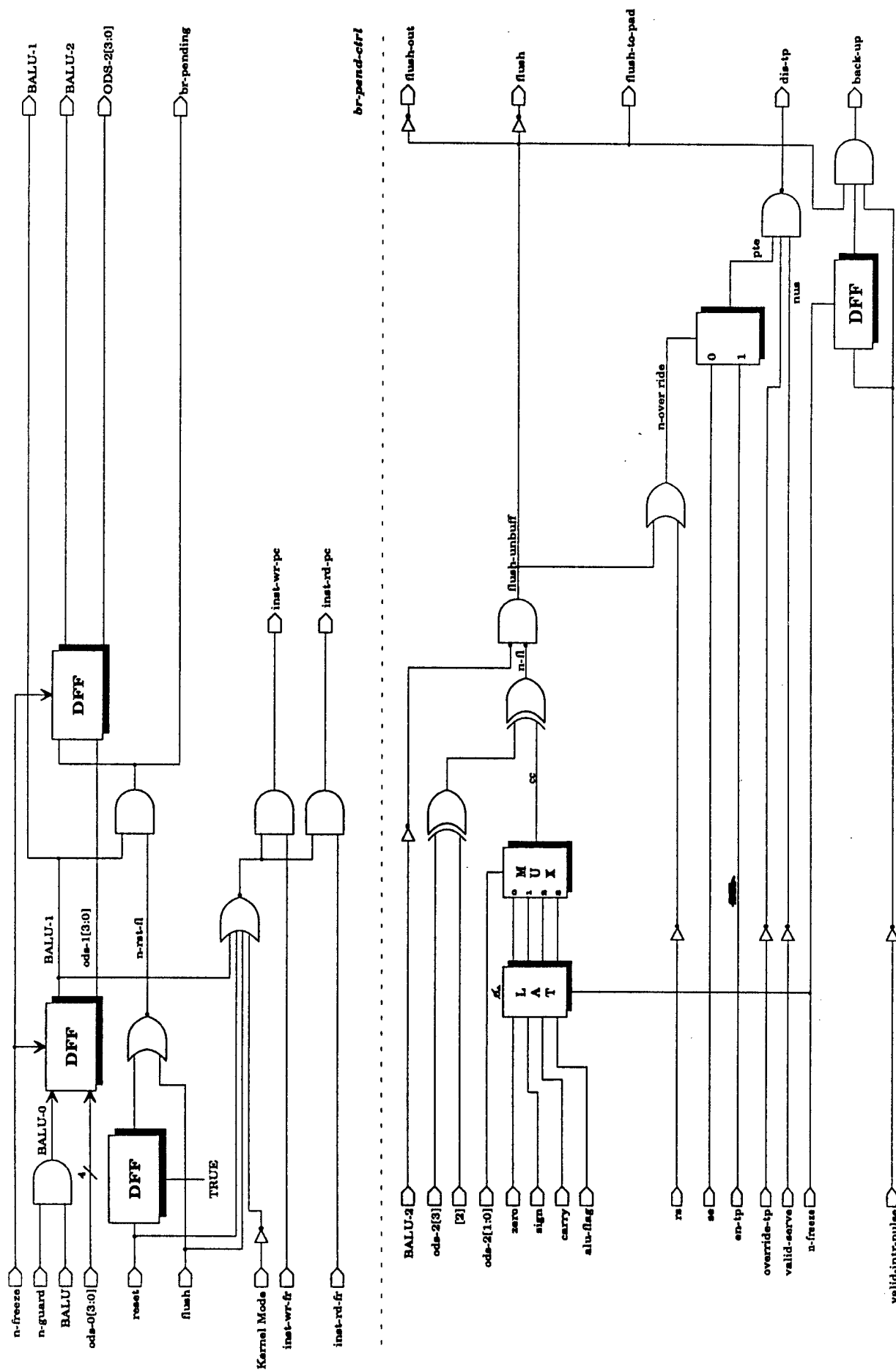
lentr-dp

pc-gen-mod
(page 1 of 2)

pc-gen-mod
(page 2 of 2)

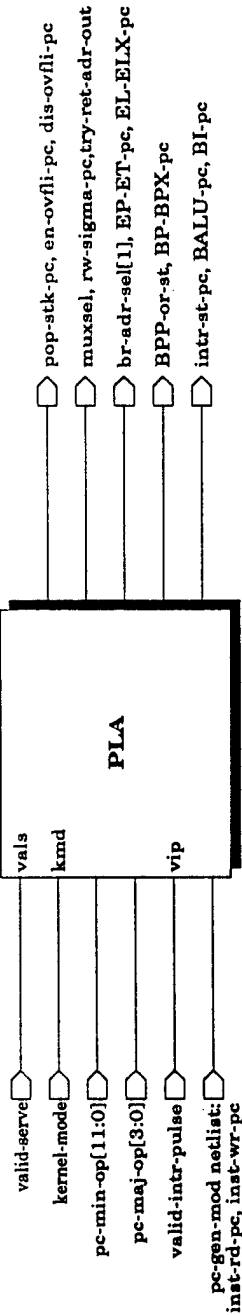


sigma-ctrl



NOTE: "Truest" is used inside pc-gen-mode
 "flush-out" is used in the rest of the chip

pc-gen-mod
 flush-ctrl

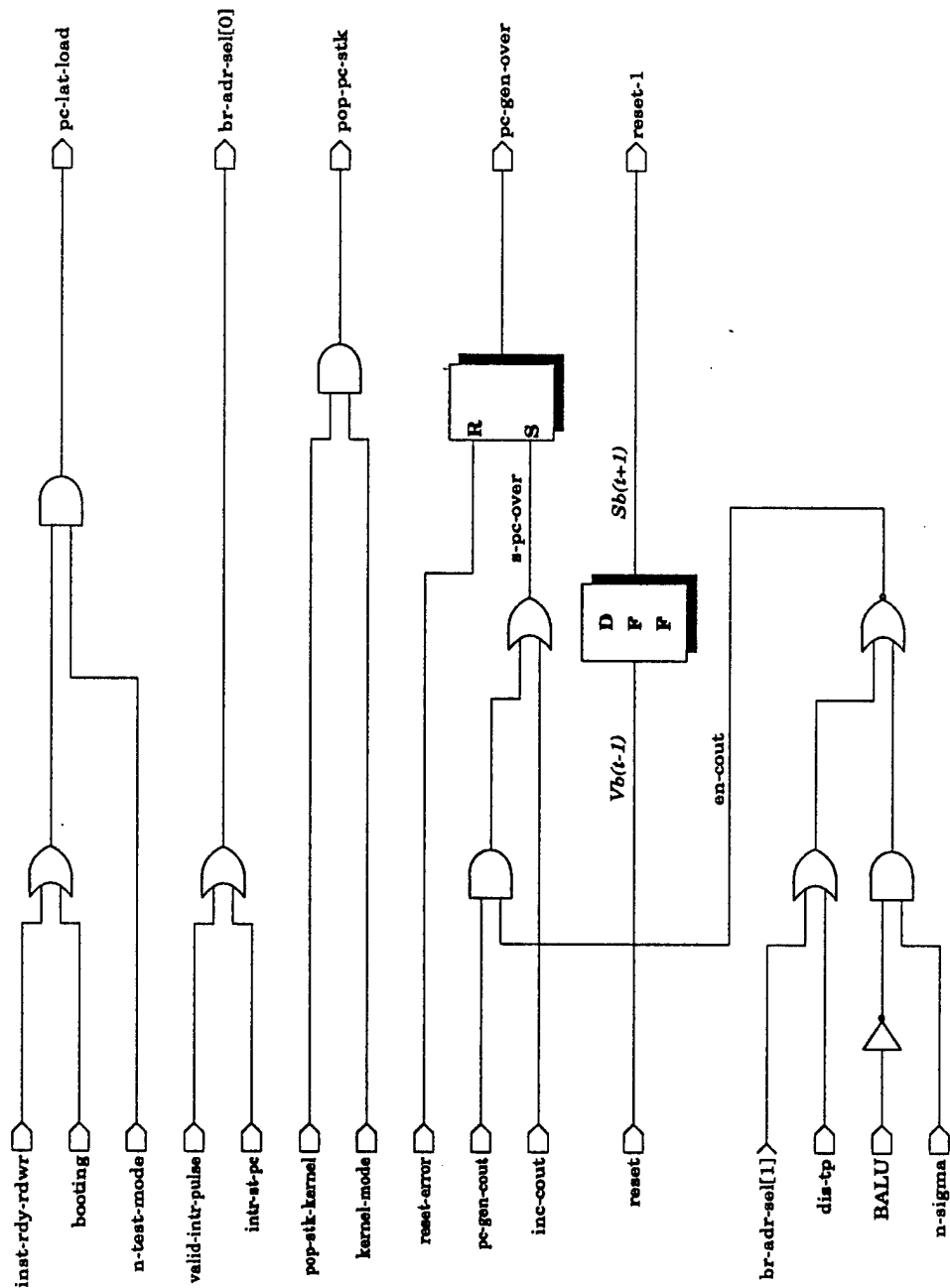


CONDITIONS

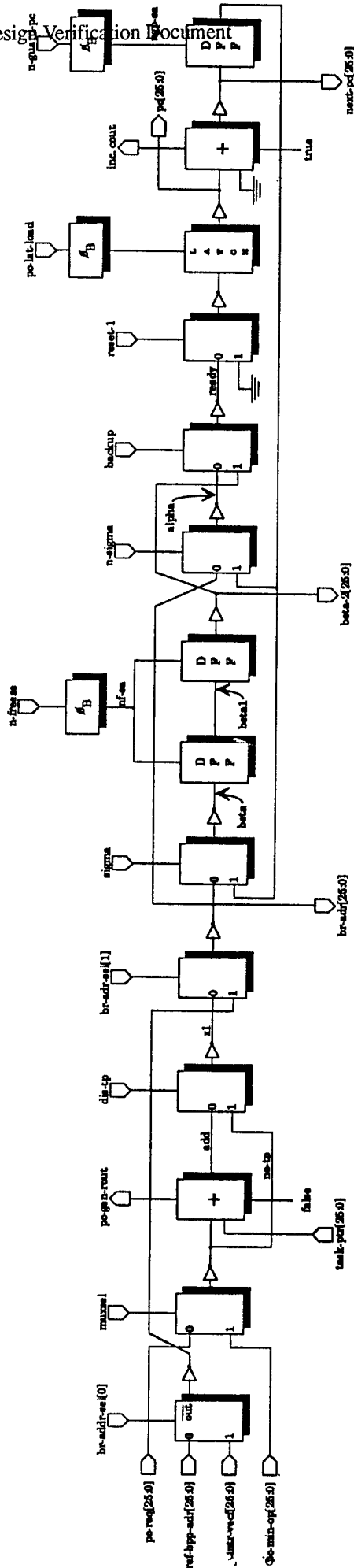
(Notice that these are the same as generated by the decoders, but without inst-en and valid-intr-pulse)
(underlined names are AND'ed with "kernel-mode")

br-adr-sel[1]		mux-sel		intr-st-pc		BPP-or-st		EL-ELX-pc	
condition	value	condition	value	condition	value	condition	value	condition	value
pop-pc-stk	1	BX	0	intr-st	1	BPP	1	EL	1
EL*valid-serve		BPX		else	0	hpp-st	1	ELX	1
ET		BTX				else	0	else	0
EP		BLX							
EPP		ELX							
ECS	1	rd-inst	0						
intr-st		wr-inst							
BPP									
hpp-st									
valid-intr-pulse									
BX	0	BL	1						
BPX		BI							
BTX		BALU							
BLX		BP							
ELX		BT							
inst-rd	0	EL	1						
inst-wr									
BL									
BI									
BALU									
BP	1		0						
BT									
EL									

bradr-pla



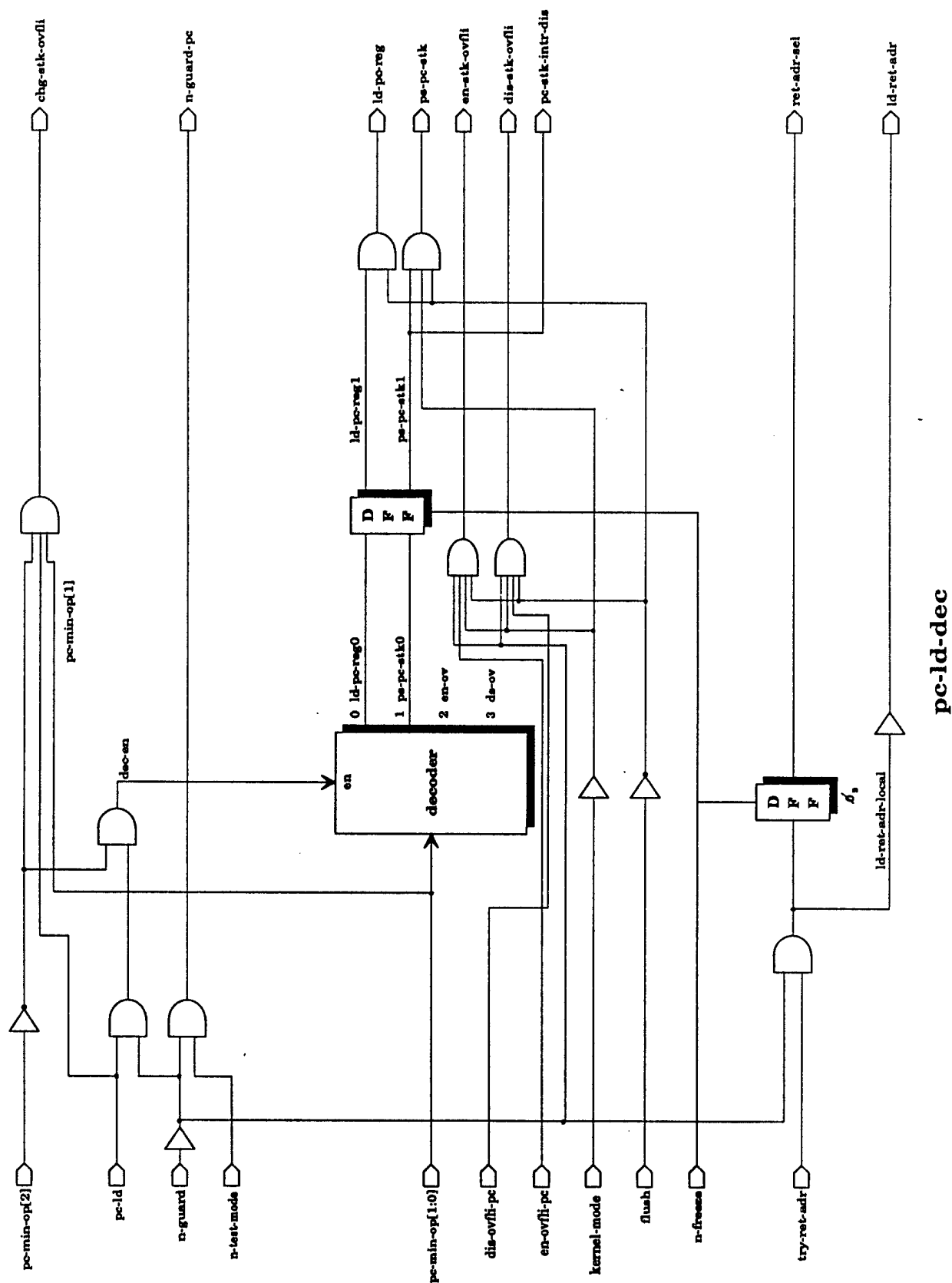
misc-ctrl

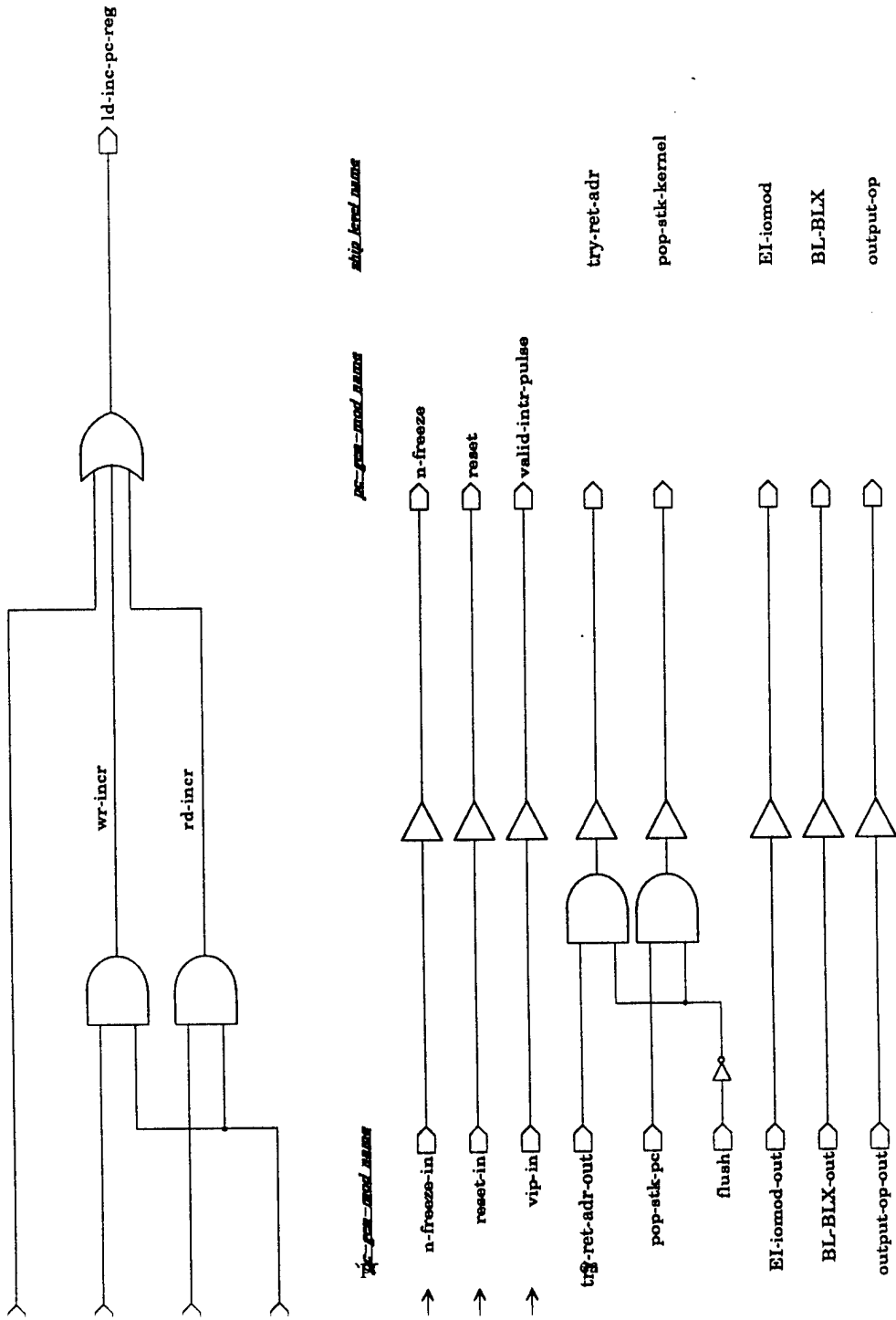


br-adr-sel	condition
0 0	BX v BPX v BTX v BLX v ELX v inst-wr v inst-rd
0 1	BIVBALU v BPVBT v EL v BL
1 0	EP-ETV ECS v pop-pc-stk v EI
1 1	valid-intr-pulse v intr-st v BPP v bpp-st

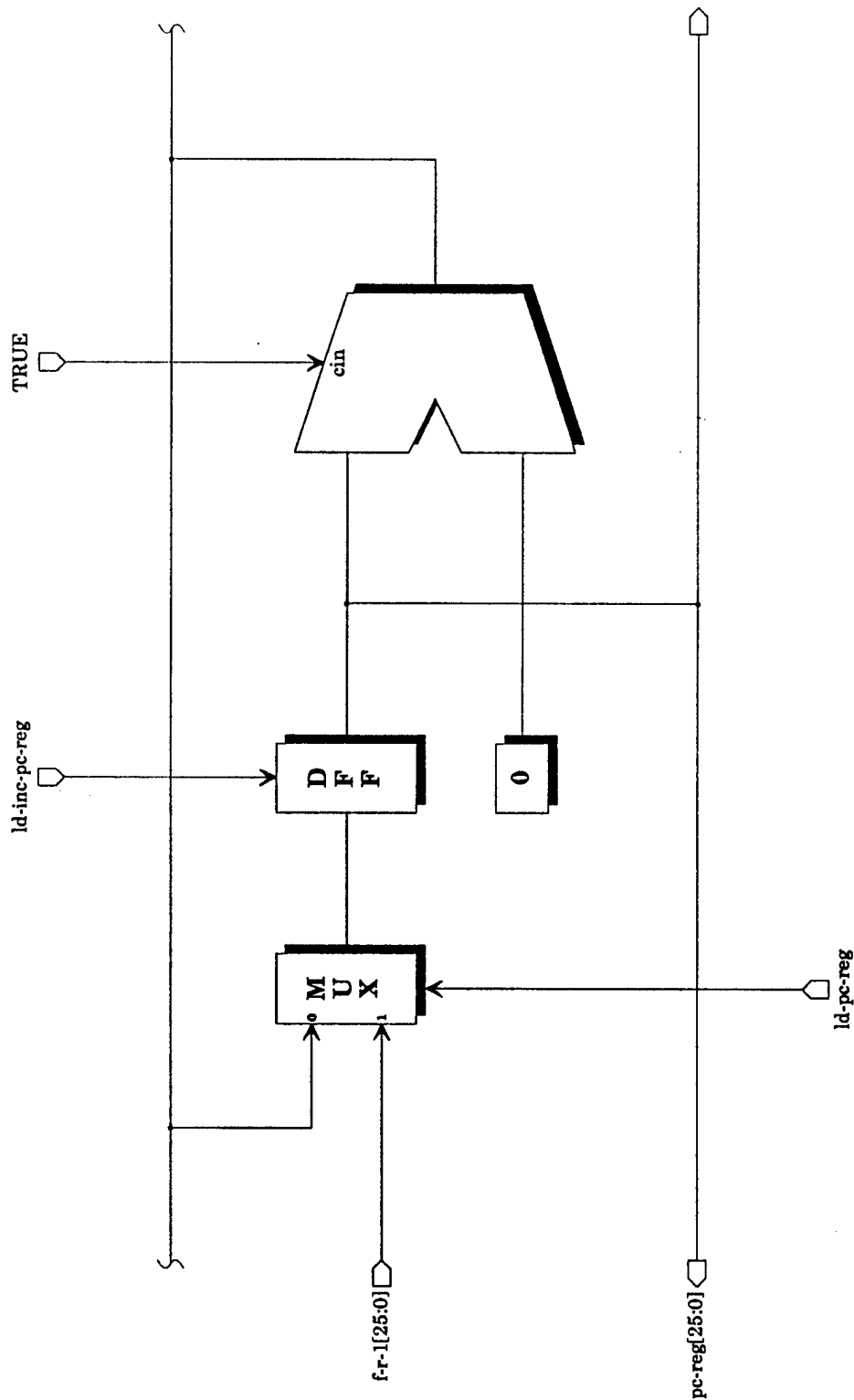
conditions for bradr-pla

pc-ndp-mod

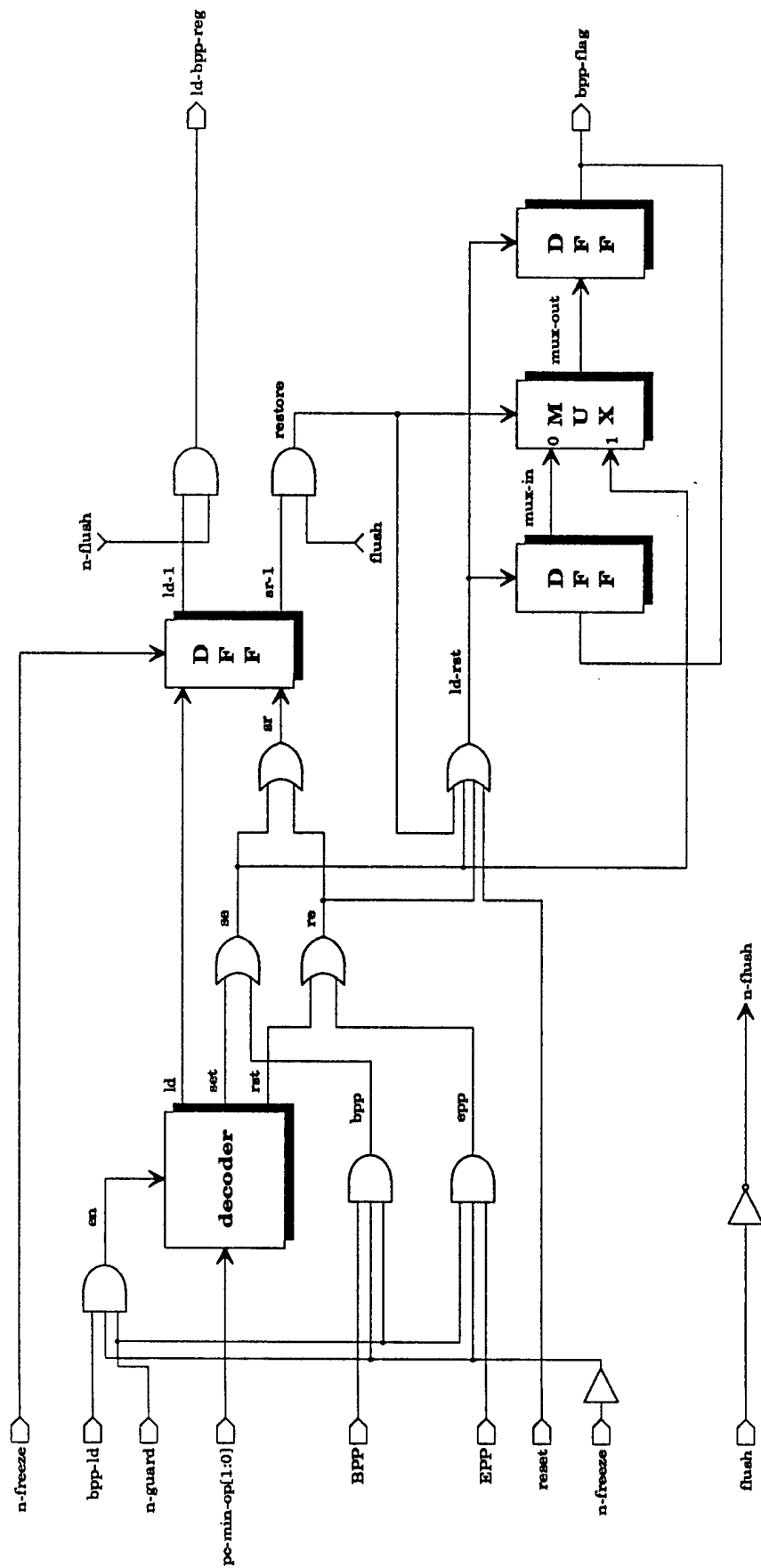


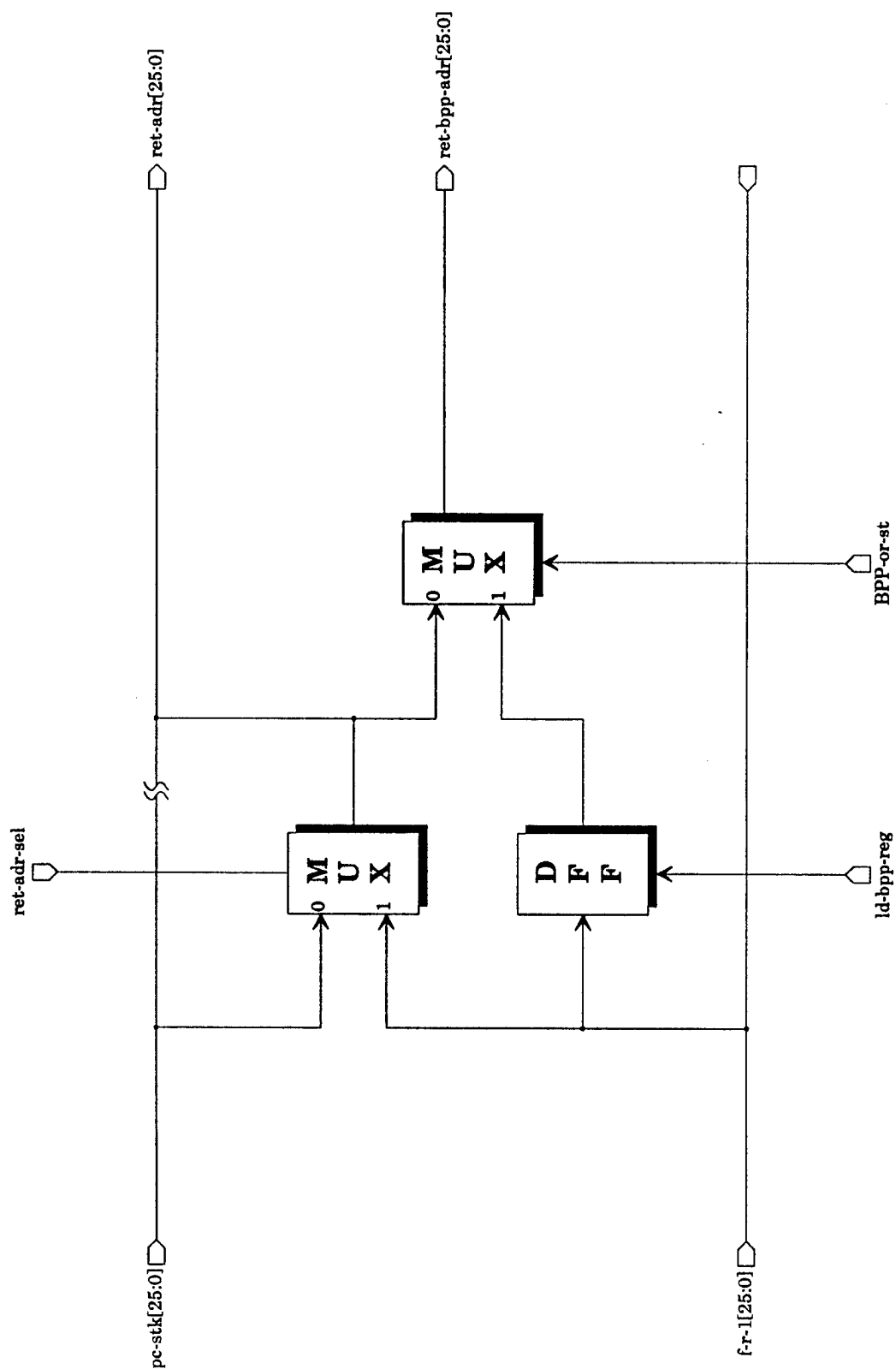


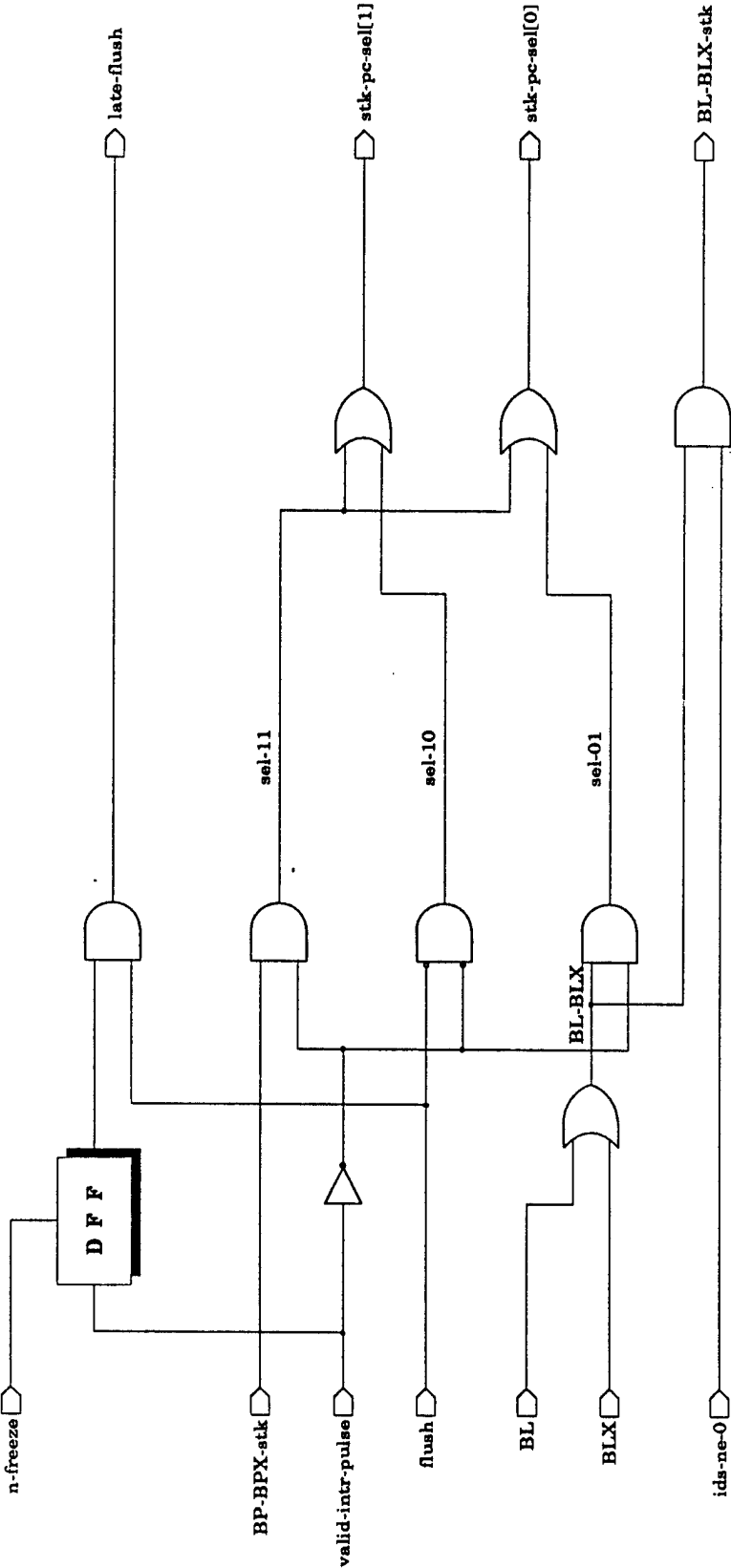
pc-gen-mod
pc-reg-ctrl



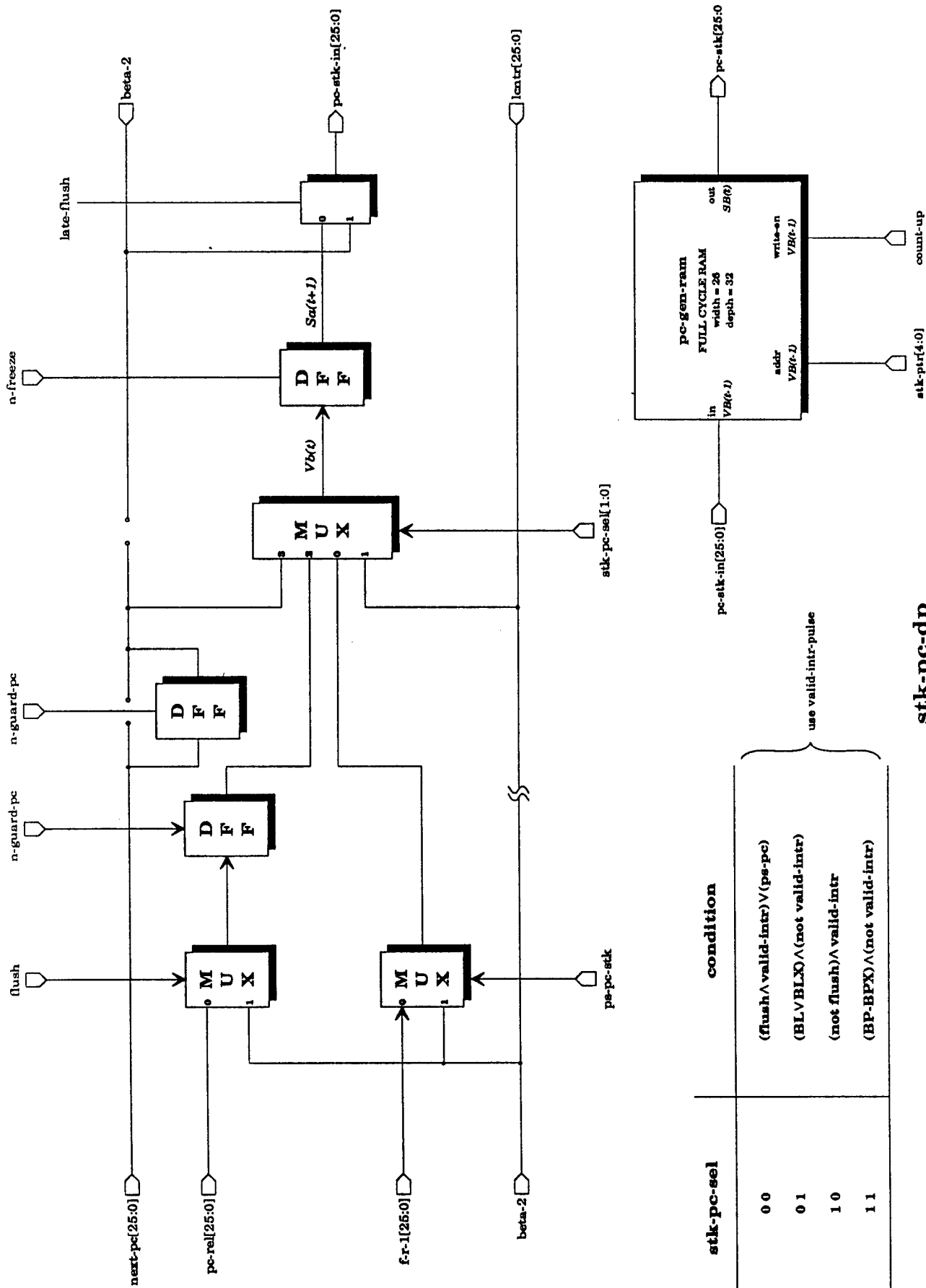
pc-reg-dp

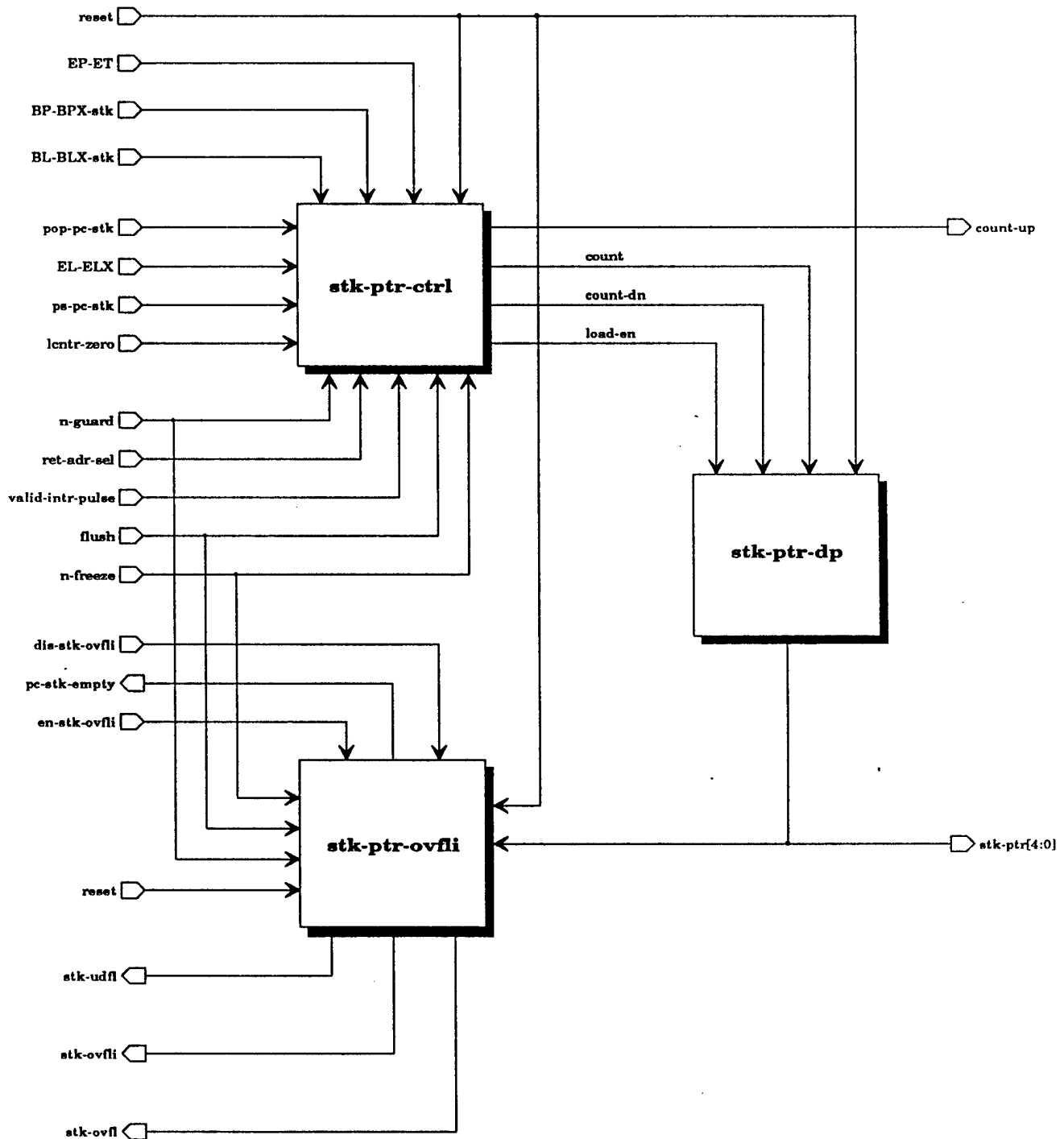
**bpp-ctrl**

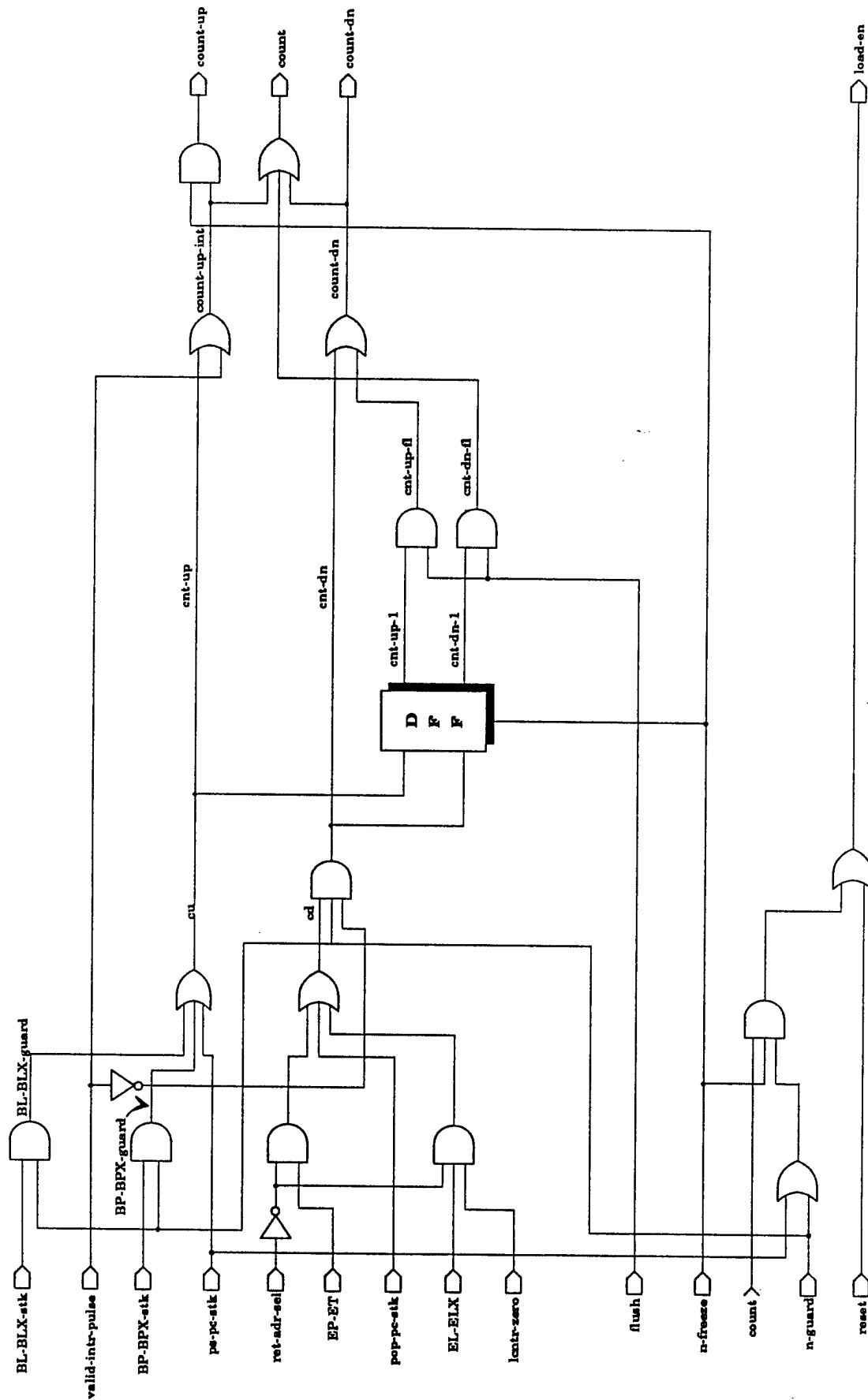
**bpp-dp**



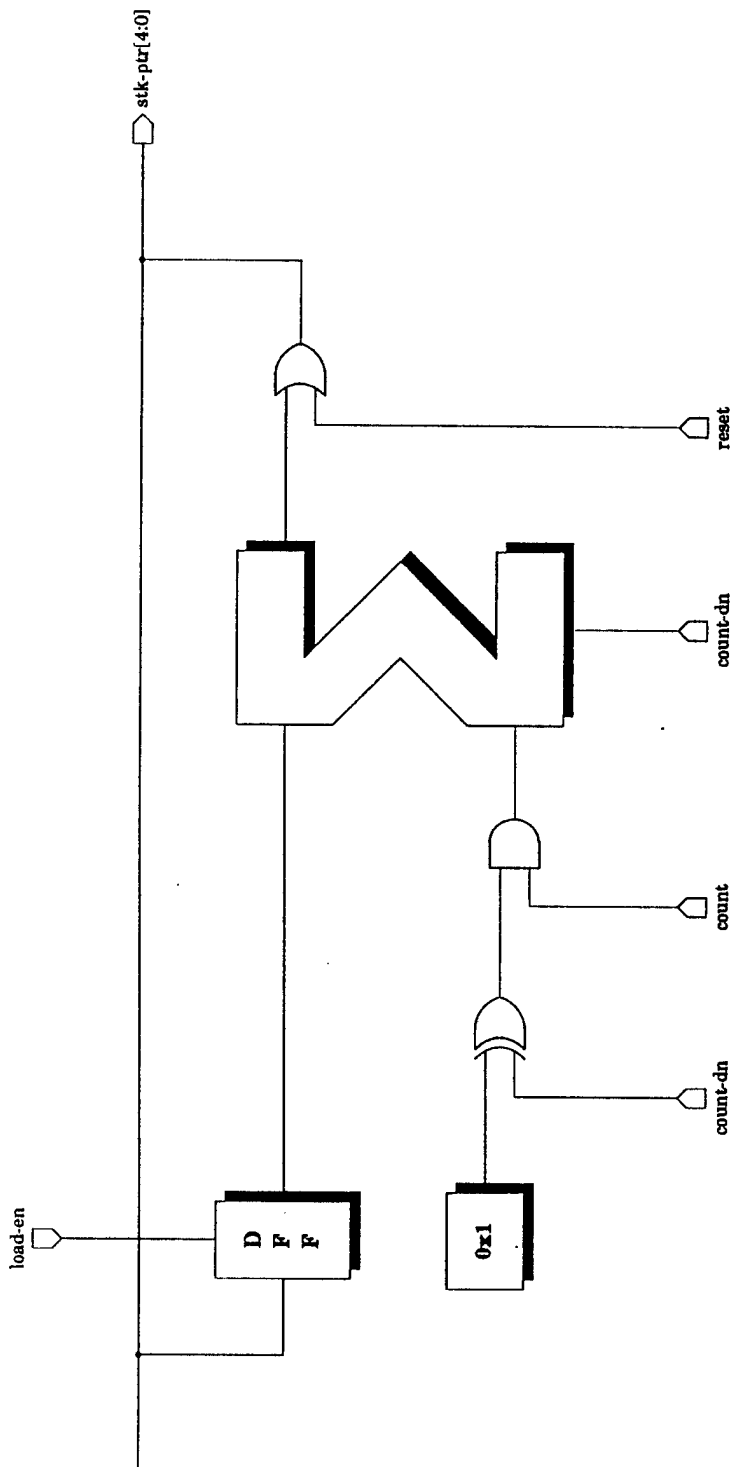
stk-pc-ctrl

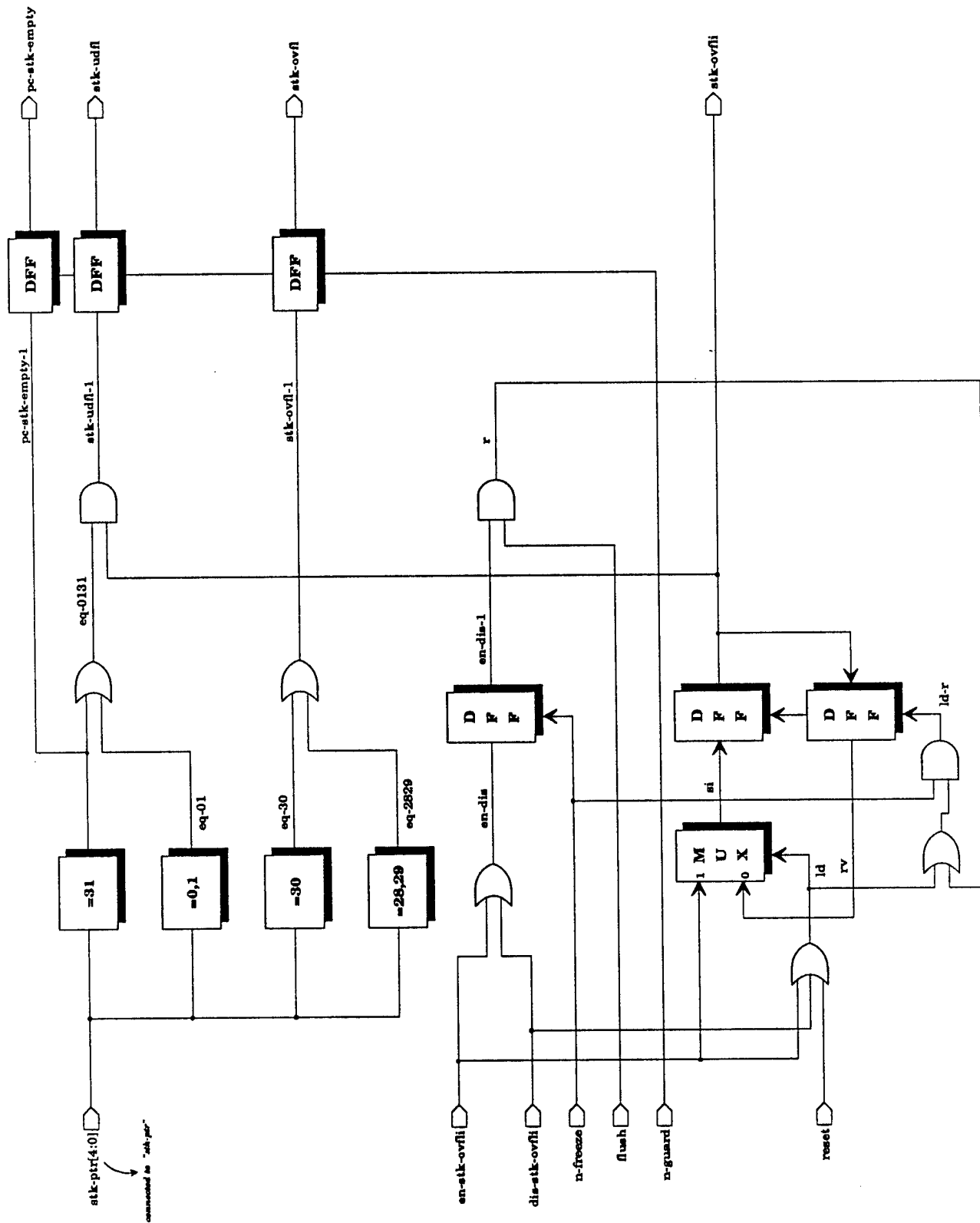


**stk-ptr-mod**

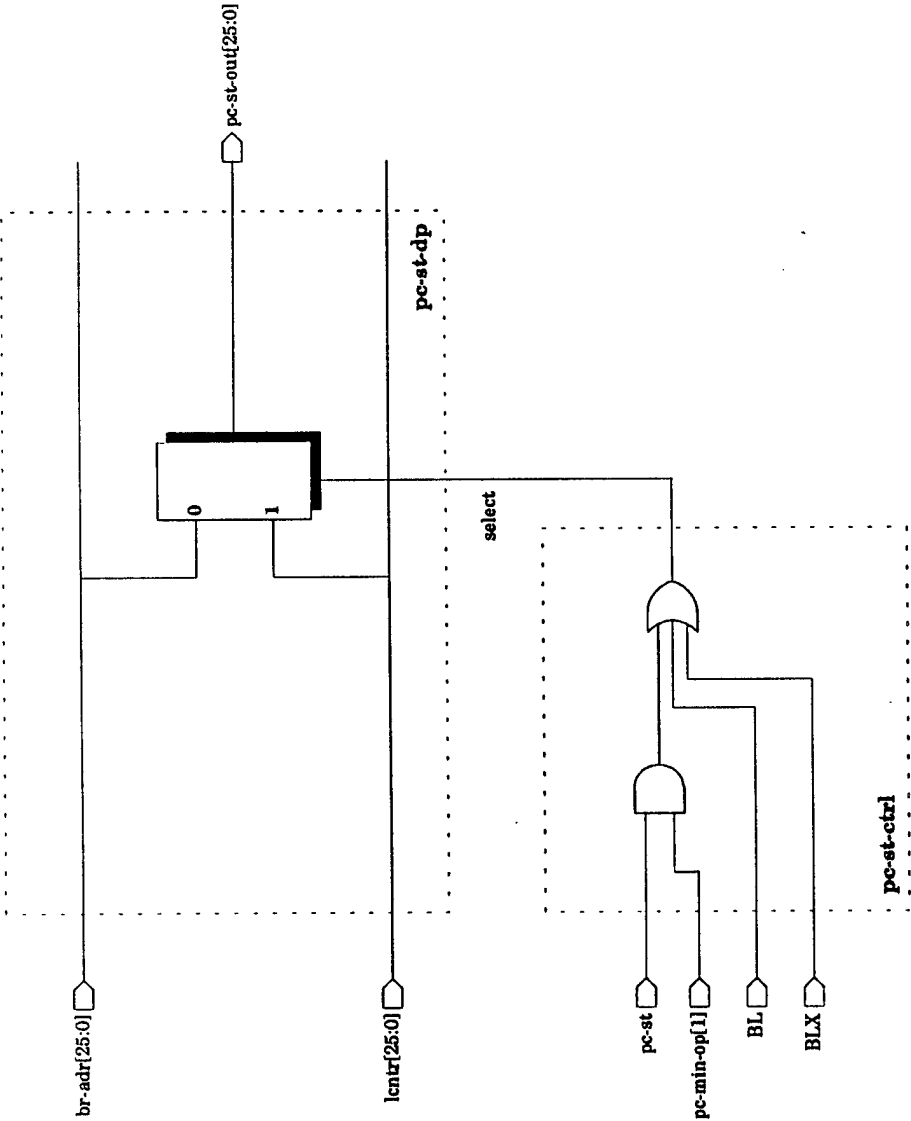


stk-ptr-ctrl

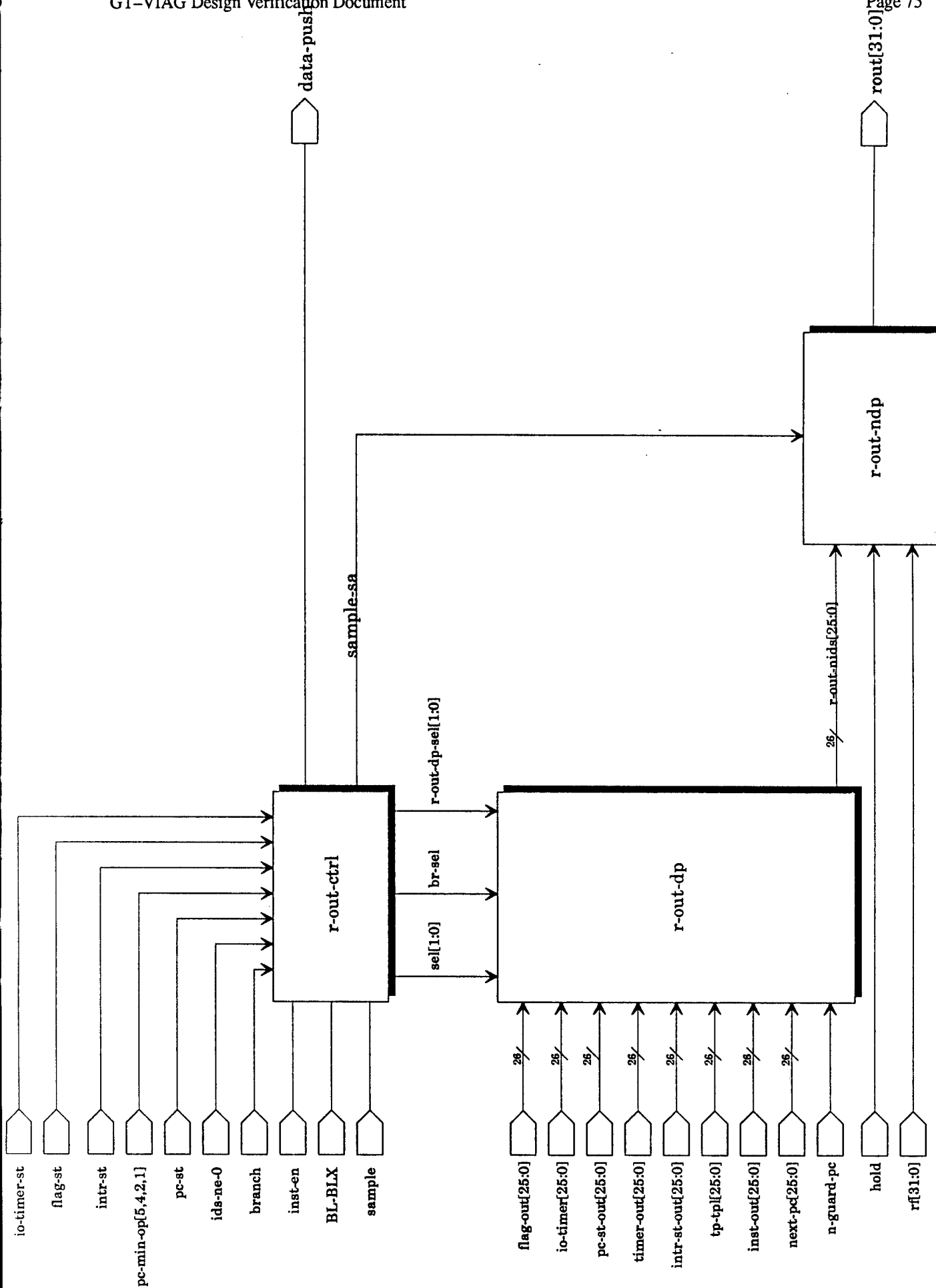
**stk-ptr-dp**

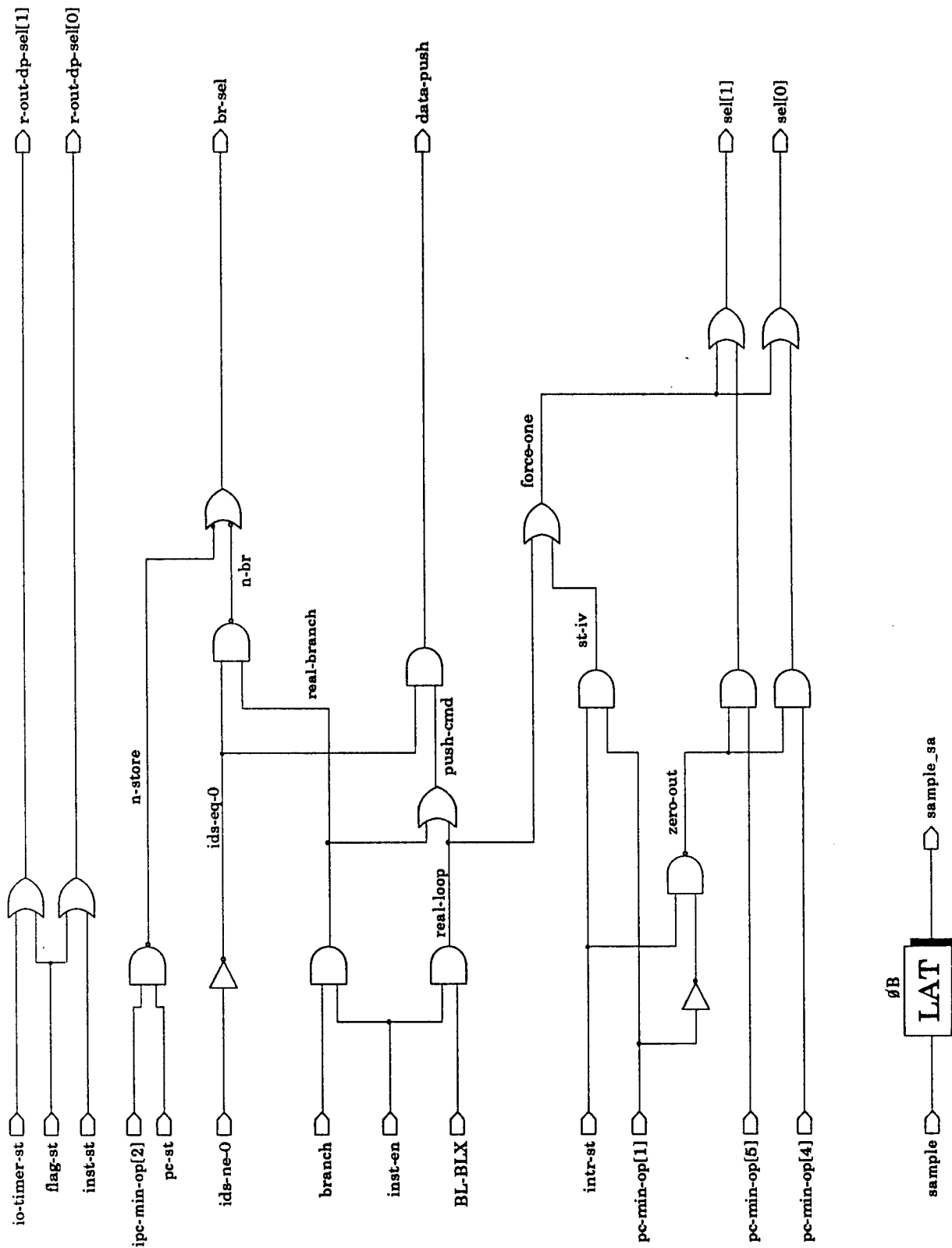


pc-gen-mod
stk-ptr-mod
stk-ptr-ovfli

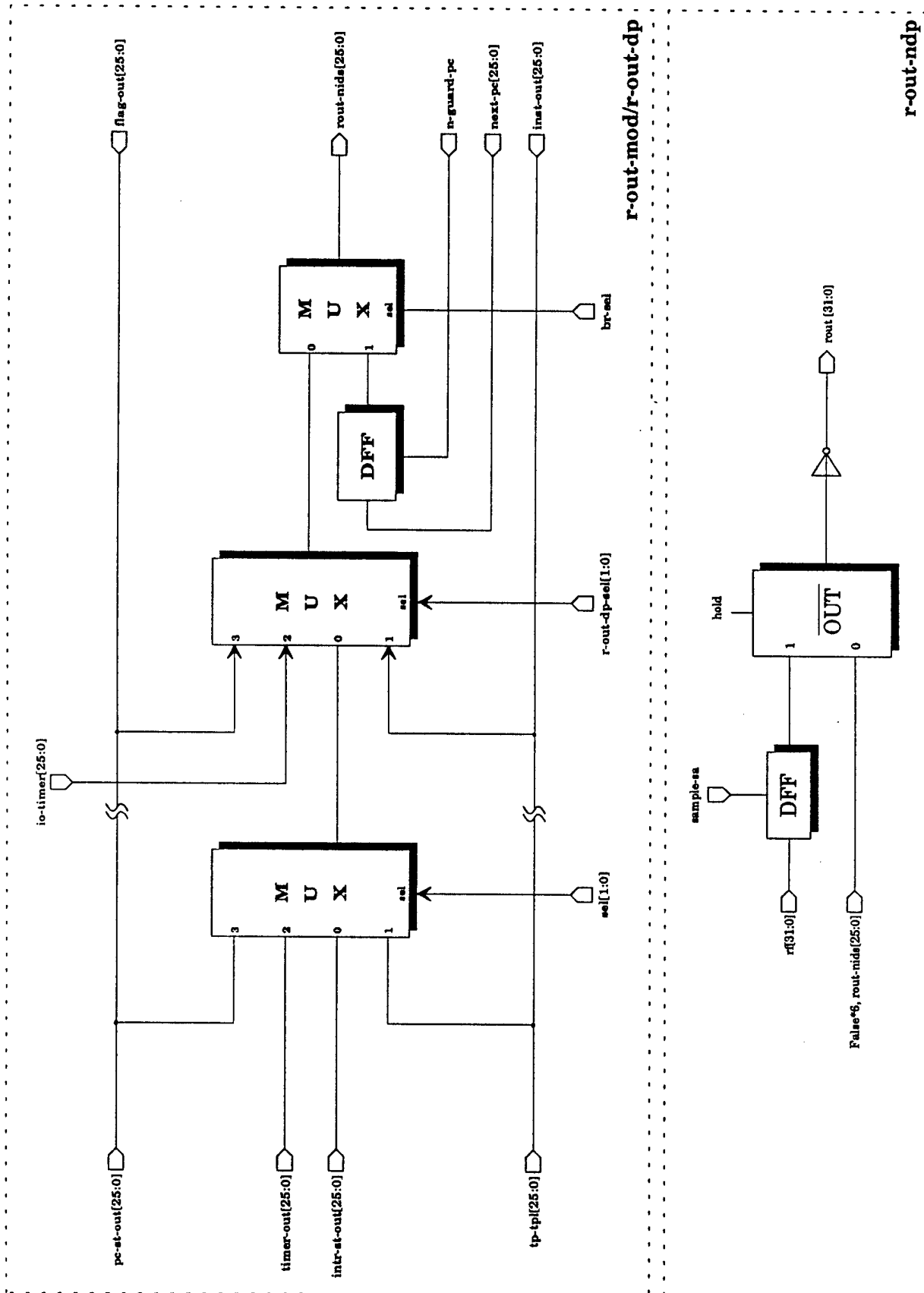


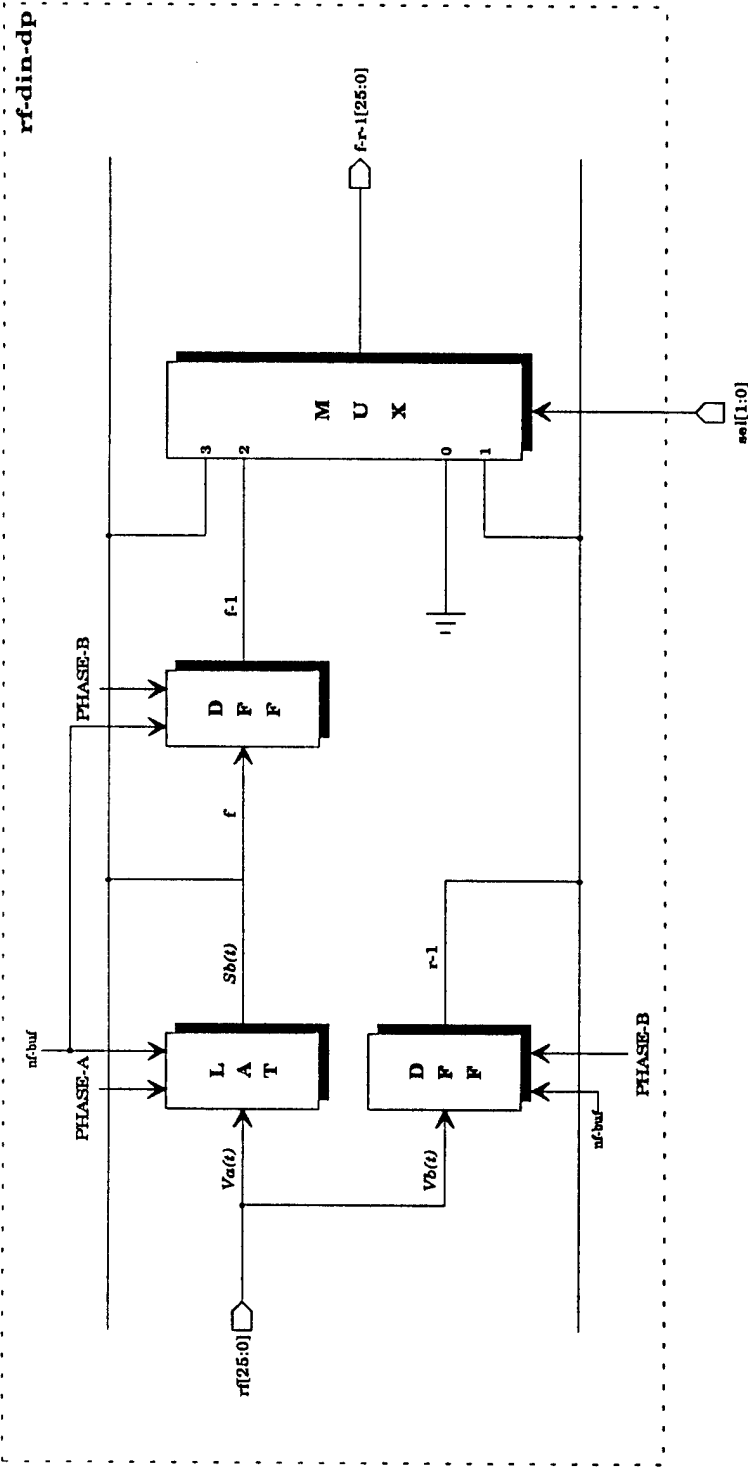
pc-st-mod



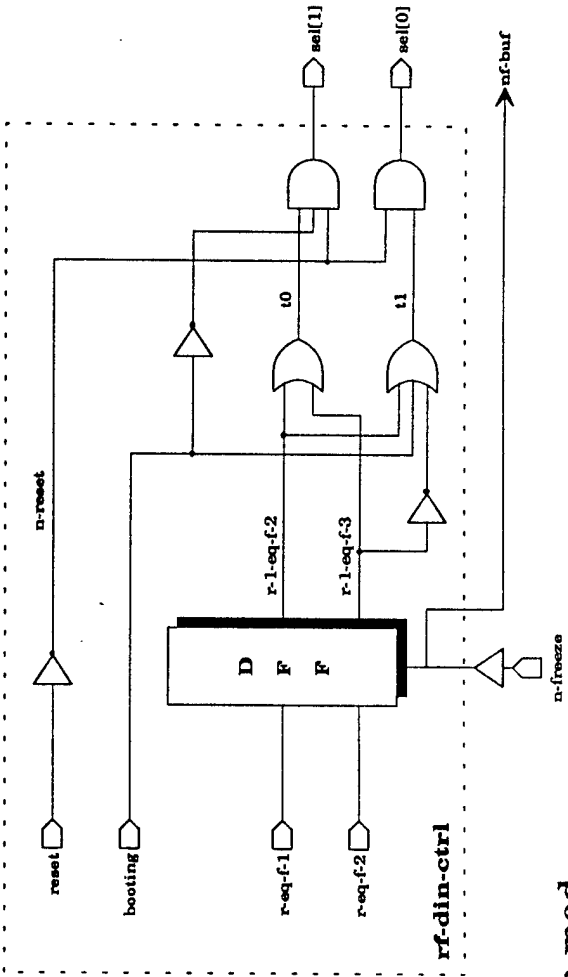


r-out-mod/r-out-ctrl

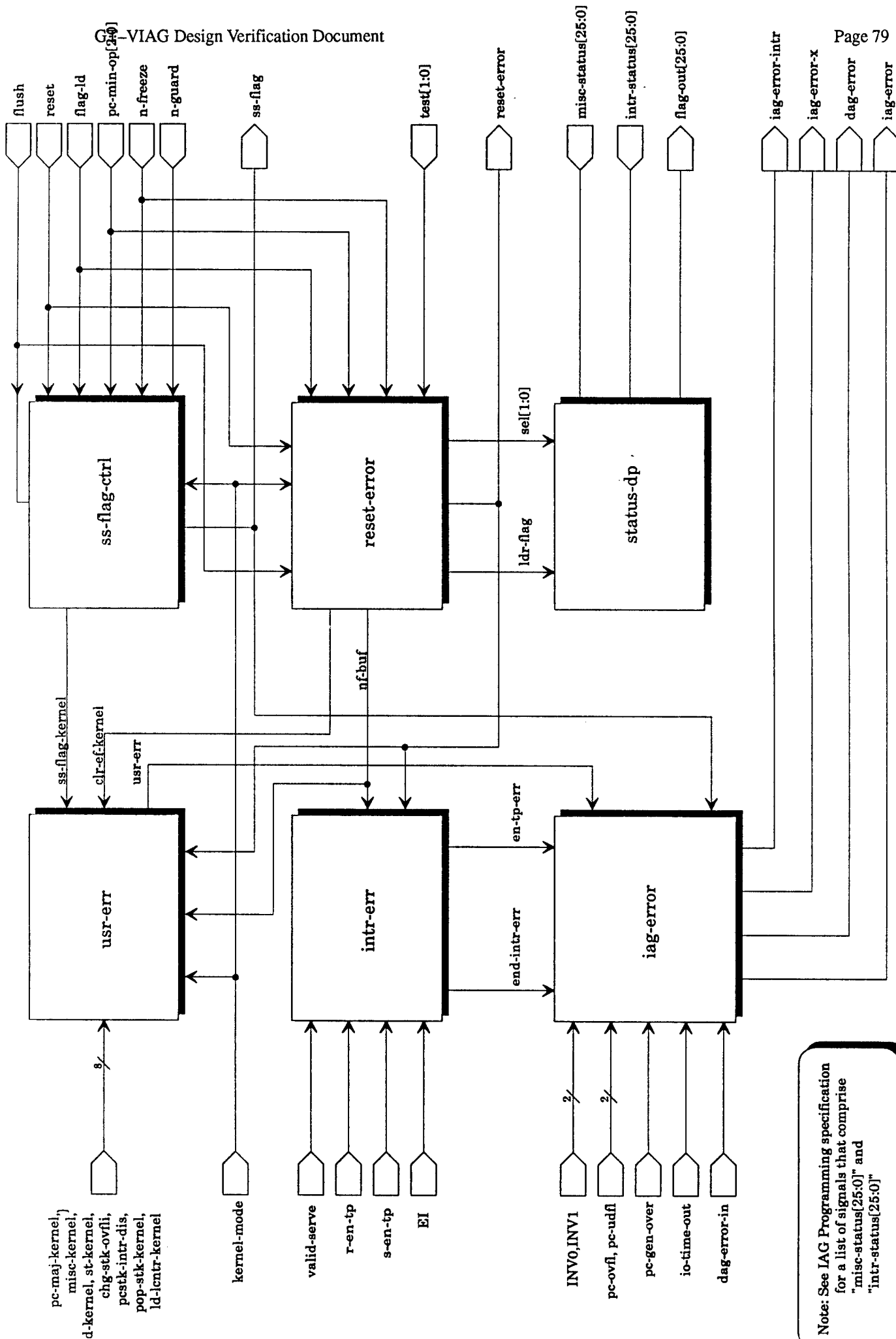




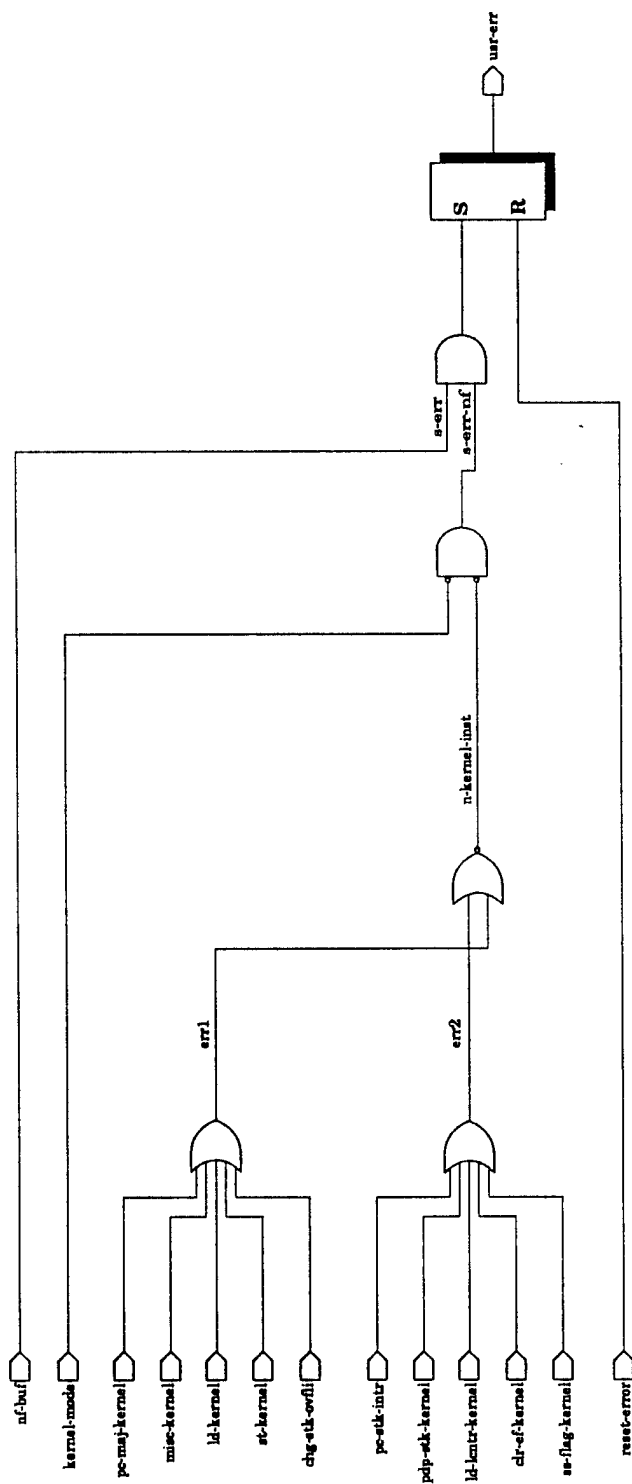
reset	$Z^{-1} r-eq-f-1$	$Z^{-1} r-eq-f-2$	$f-r-1$	$sel[1:0]$
0	0	0	$r-1$	0 1
0	0	1	$f-1$	1 0
0	1	0	f	1 1
0	1	1	f	1 1
1	X	X	0	0 0

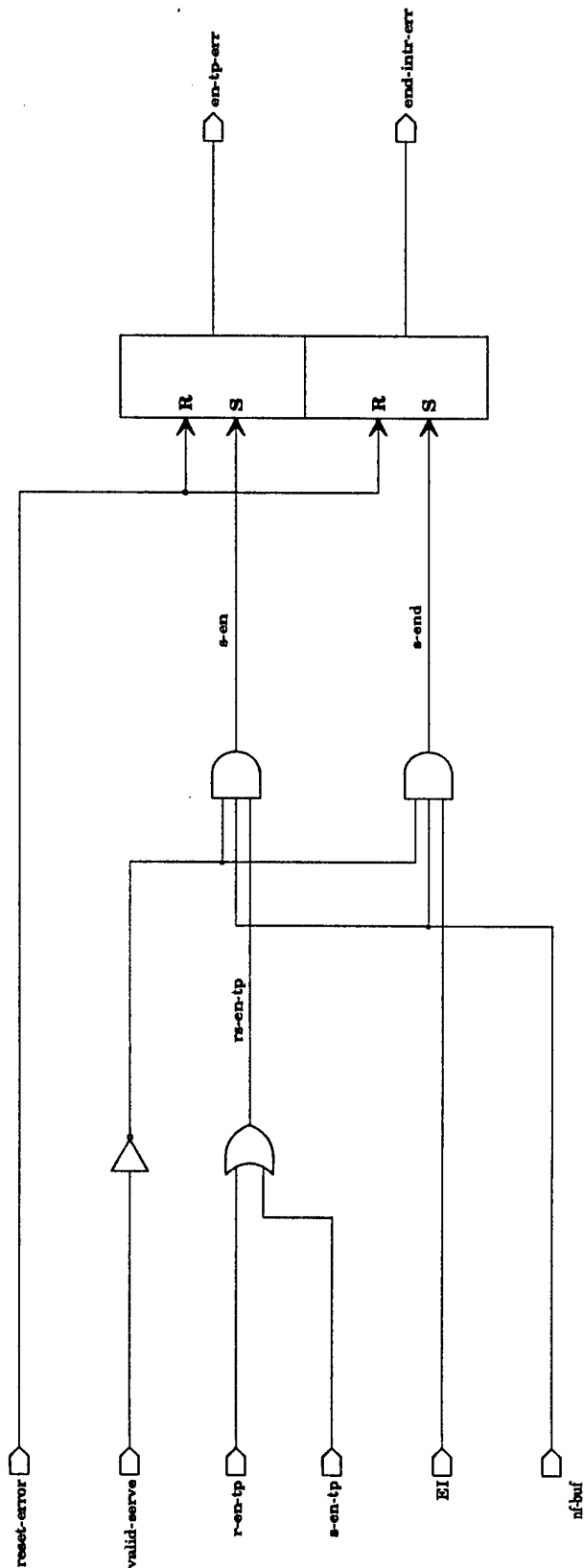


rf-din-mod

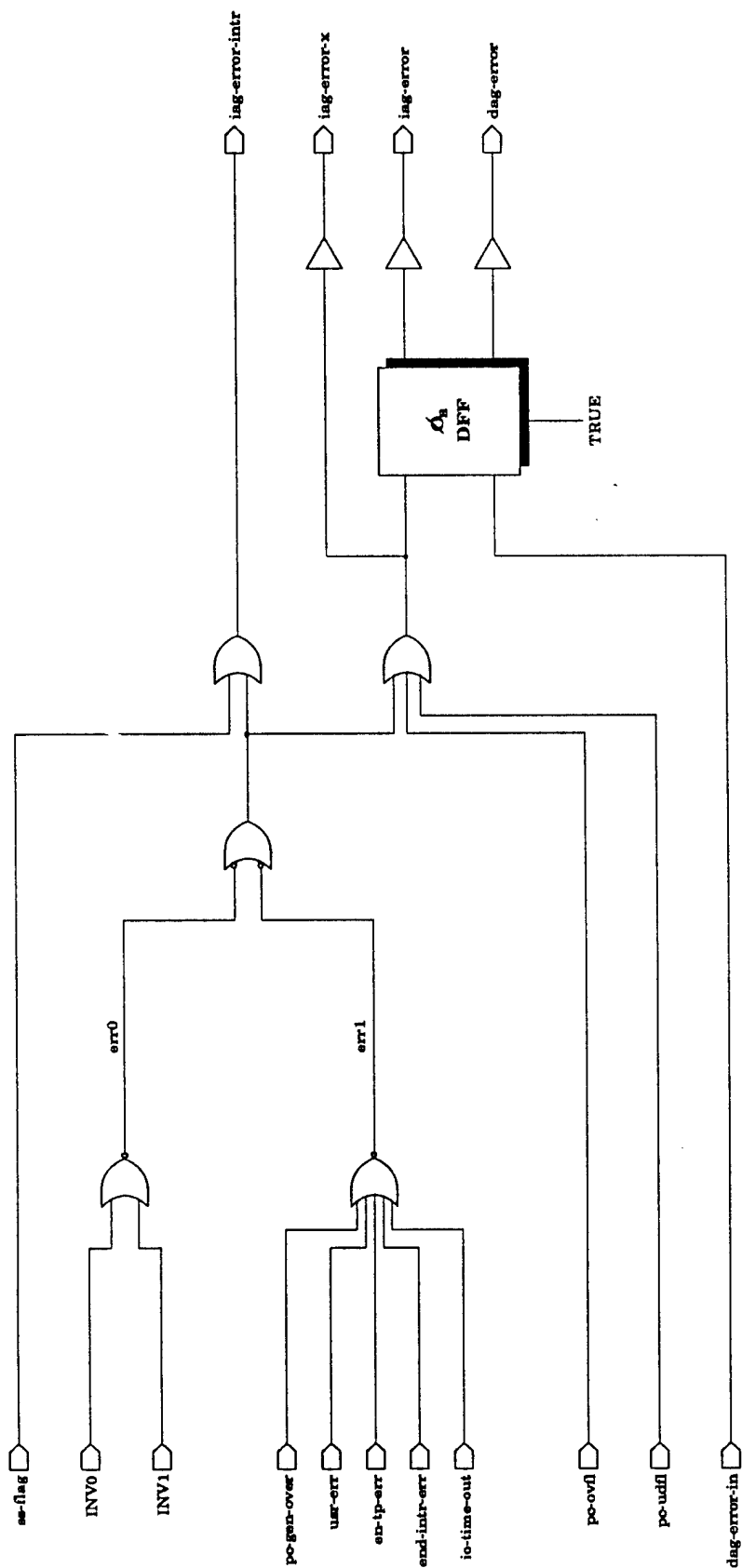


status-mod

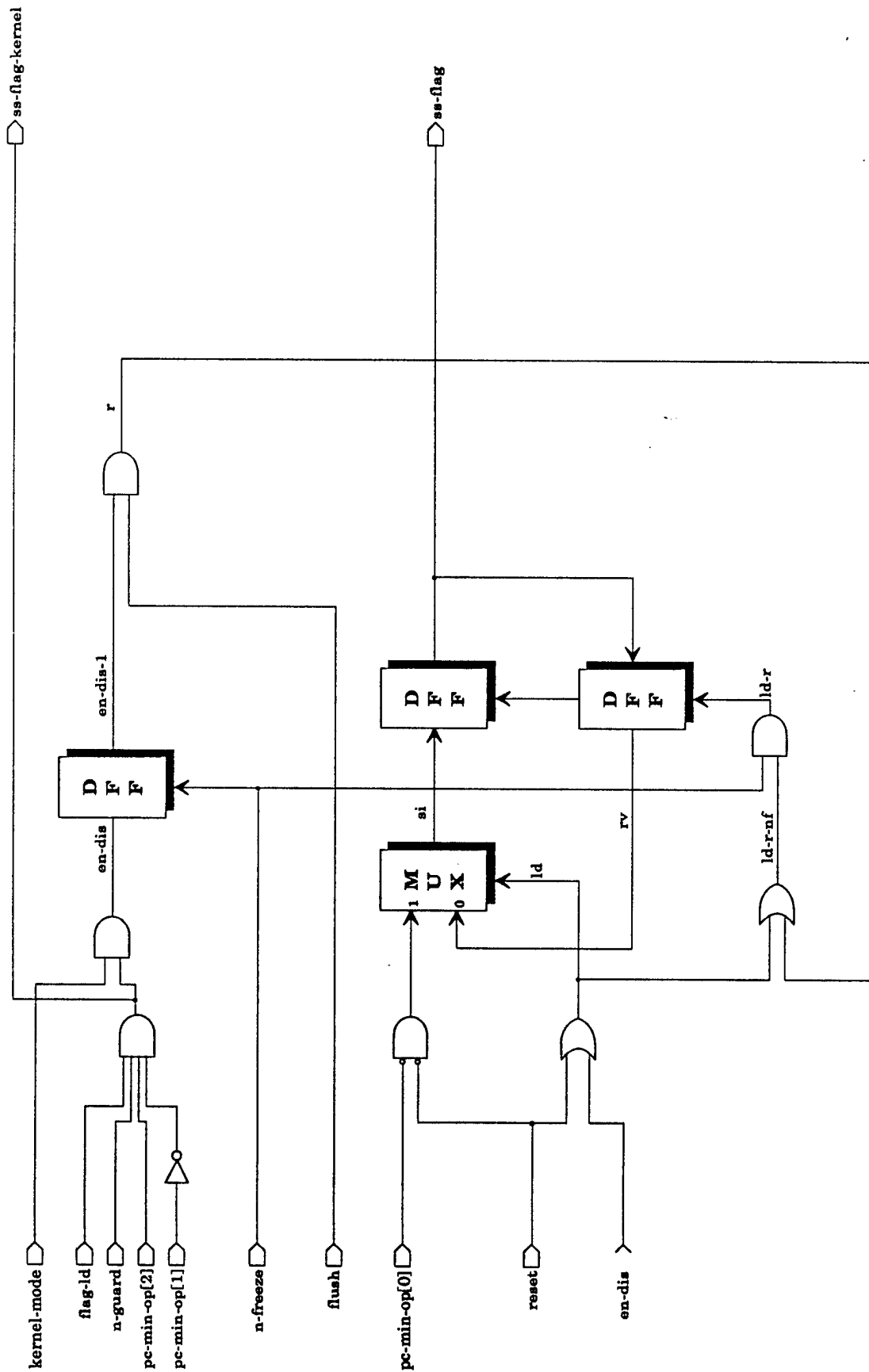
**usr-err**



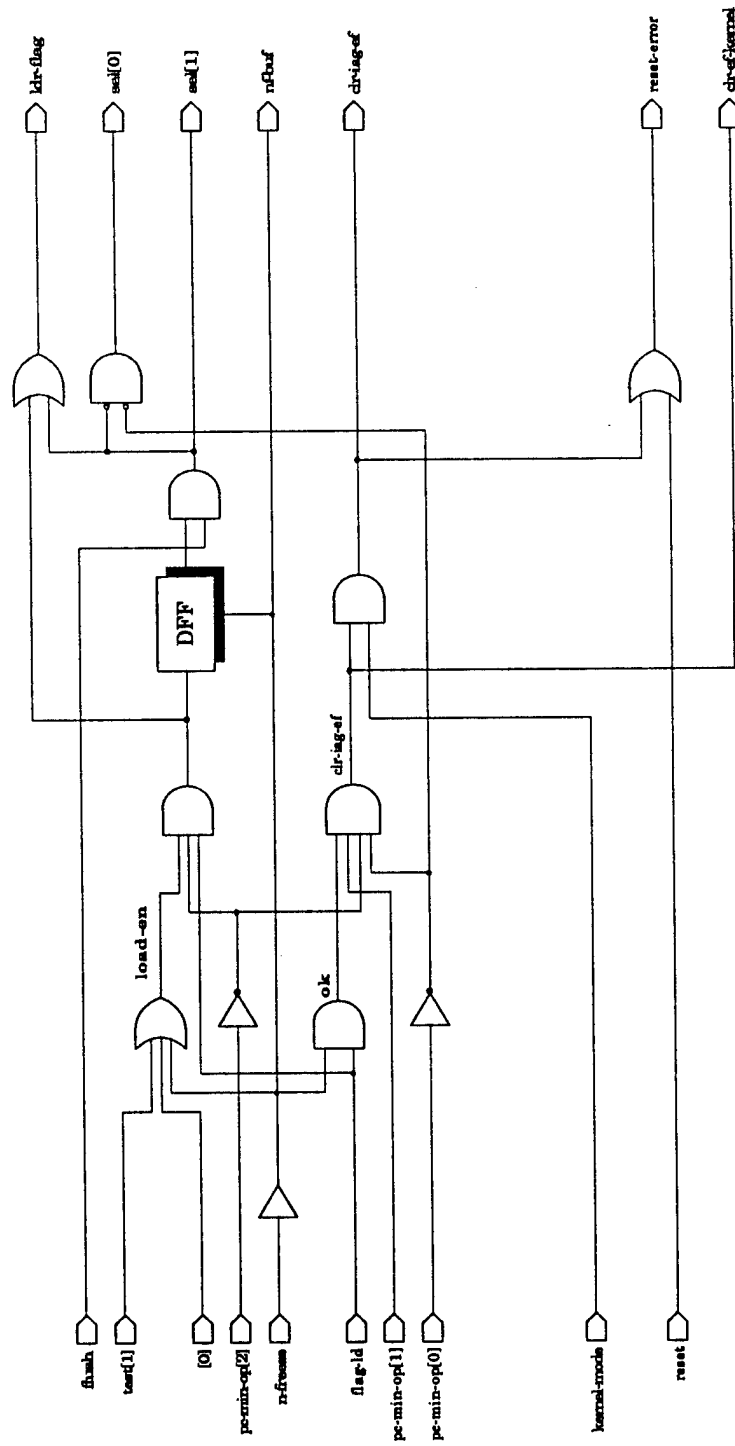
intr-err



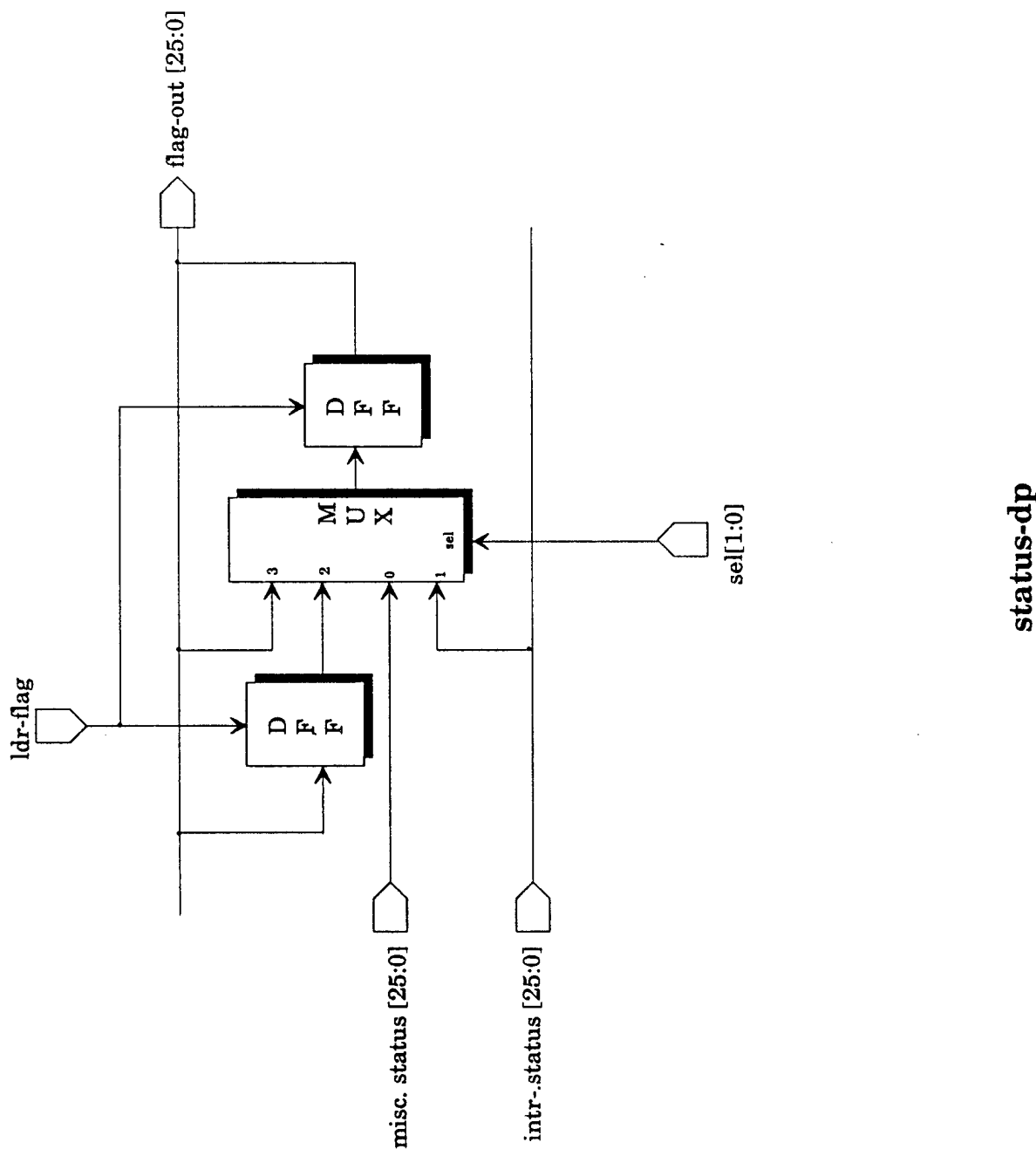
status-mod
iag-error

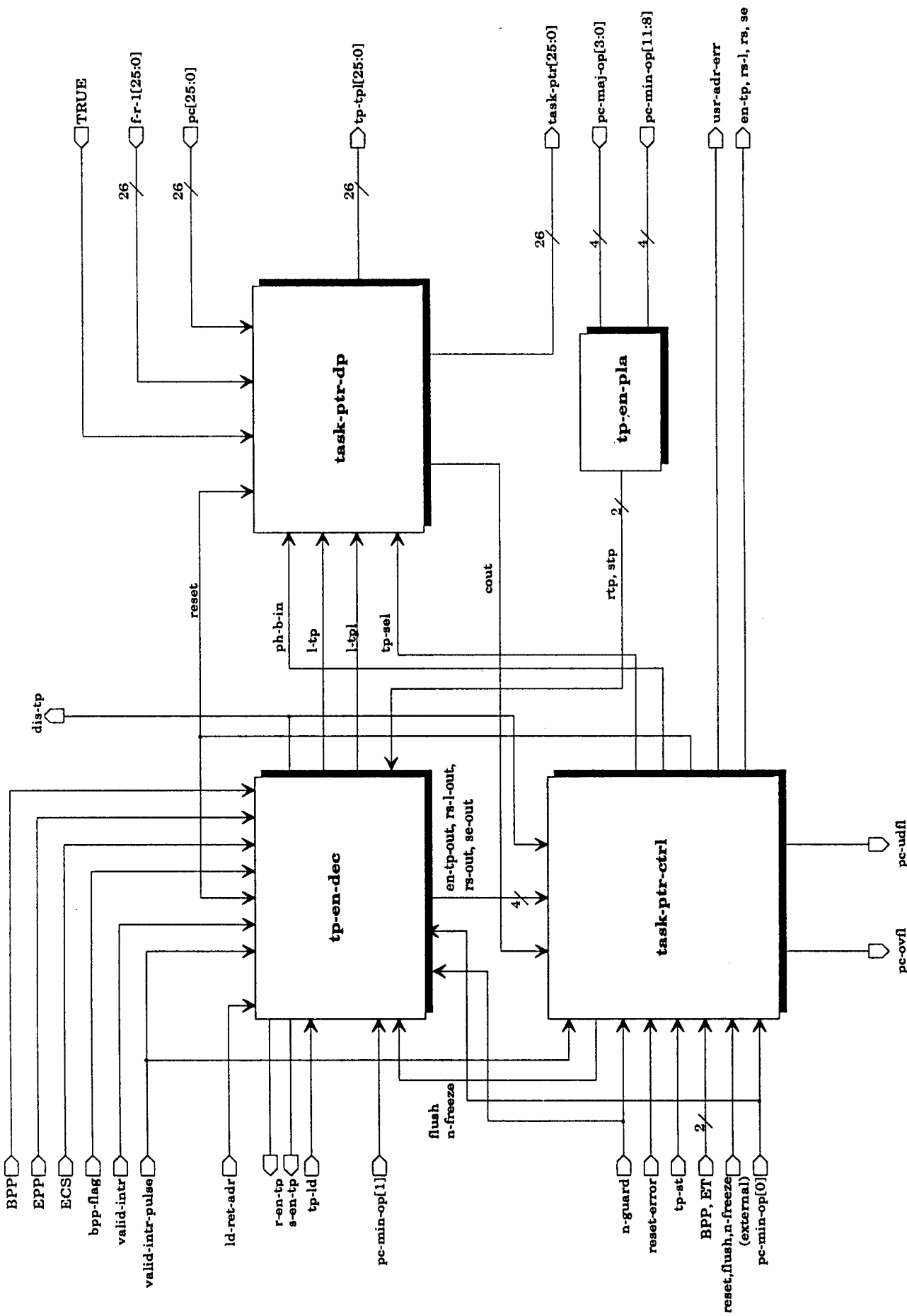


status-mod
ss-flag-ctrl

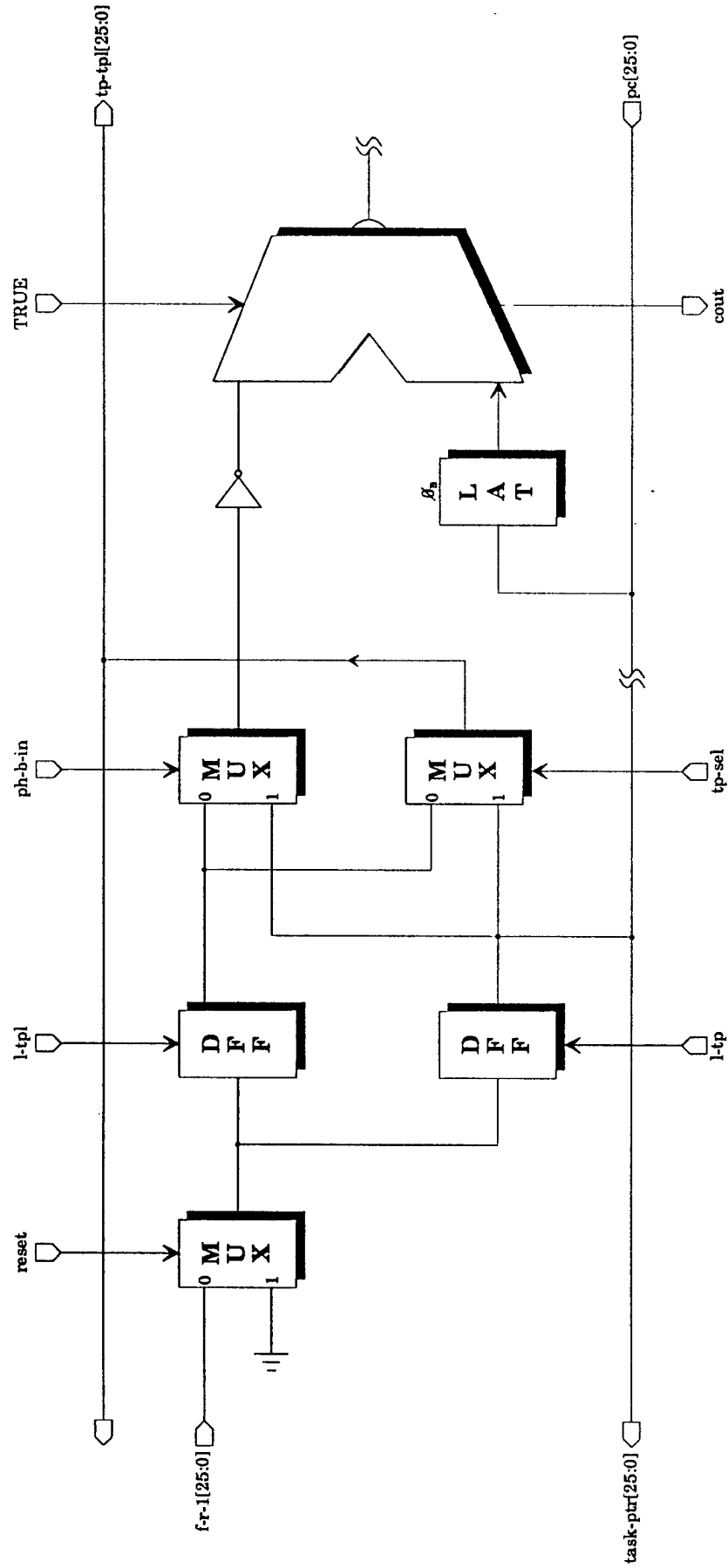


status-mod / reset-error

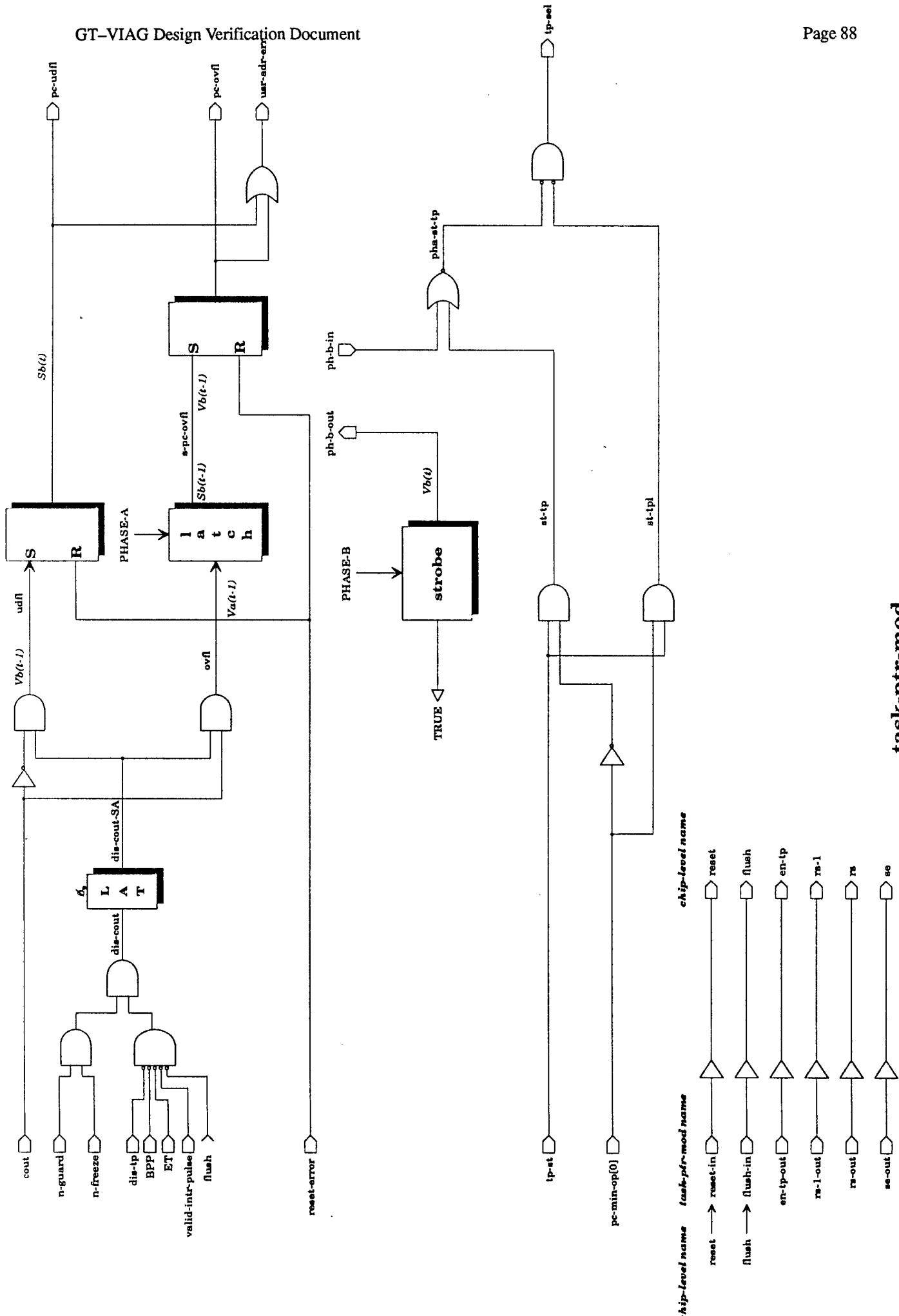




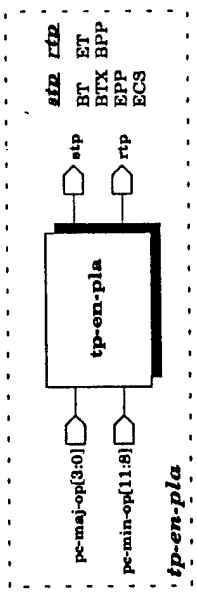
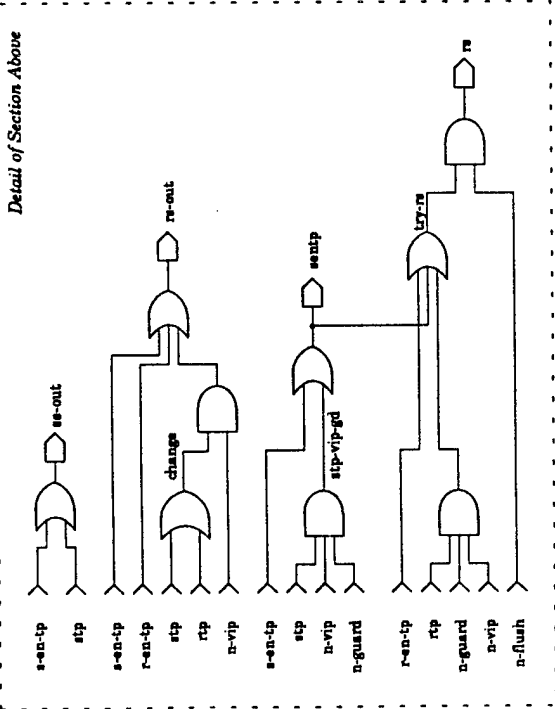
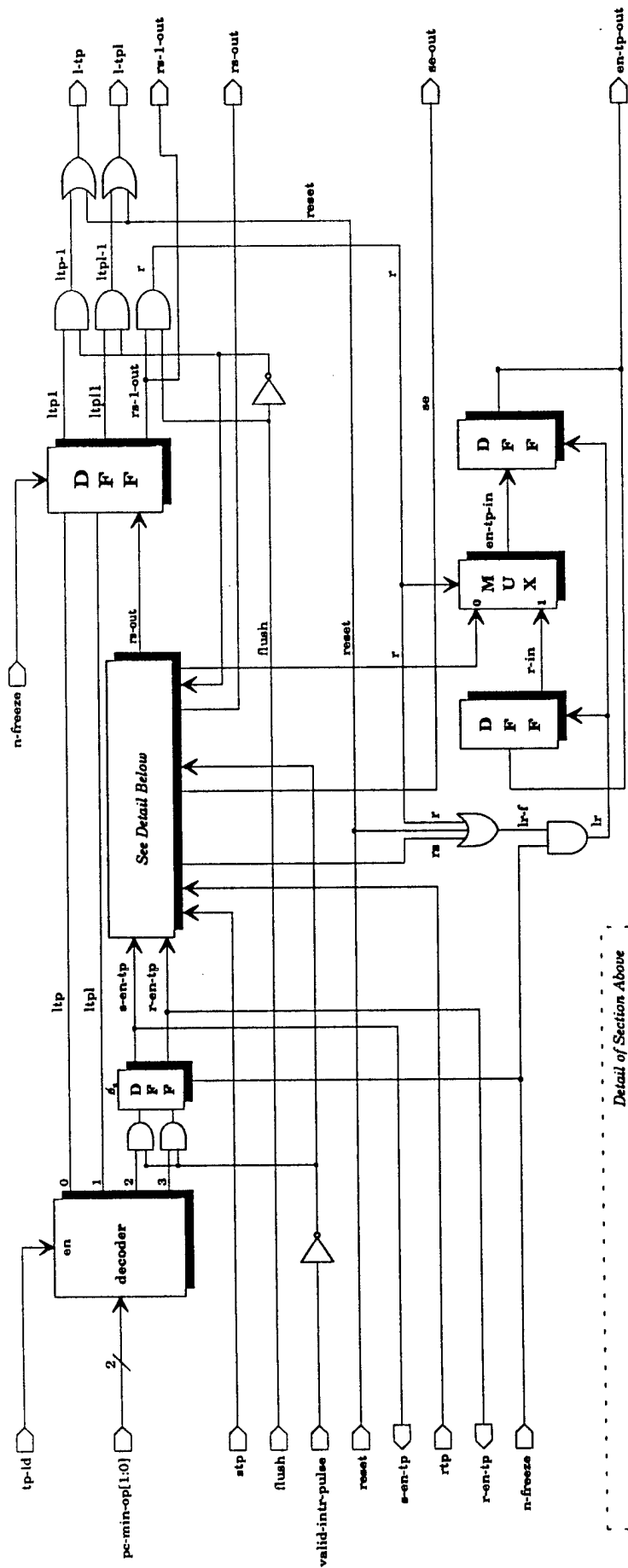
Y:\GT-VIAG\TAS\TMD.DRW



task-ptr-mod
task-ptr-dp

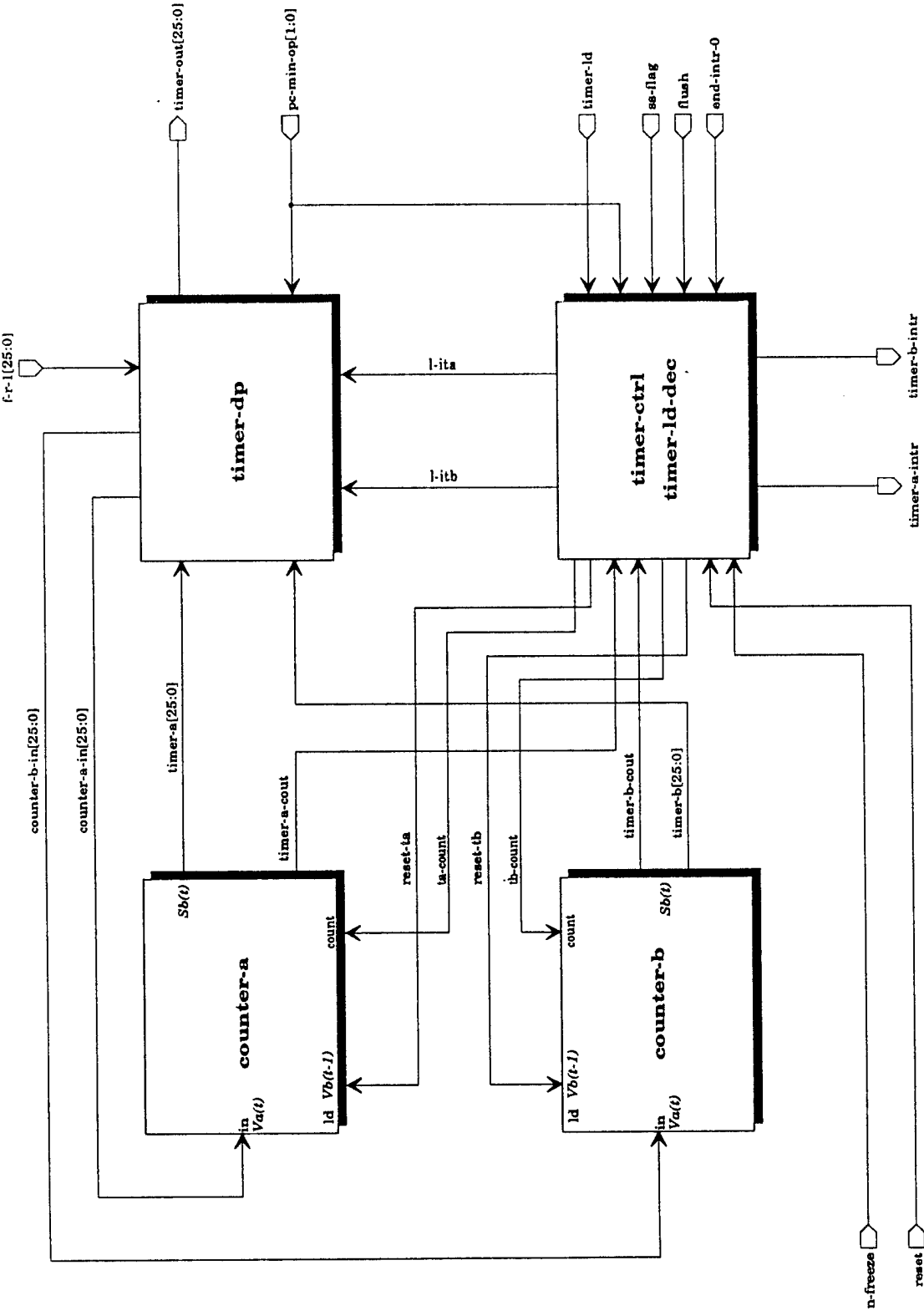


task-ptr-mod
task-ptr-ctrl

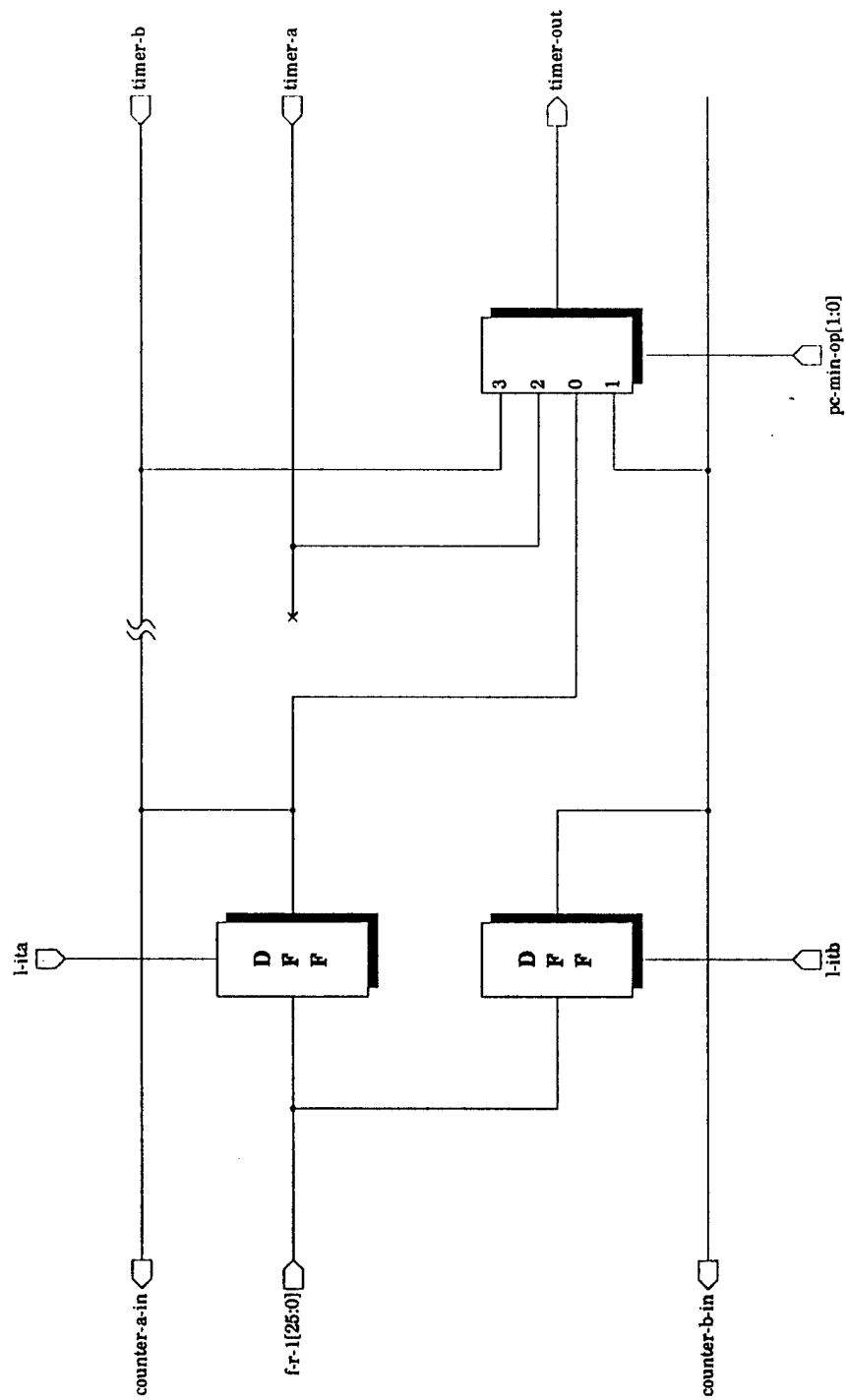


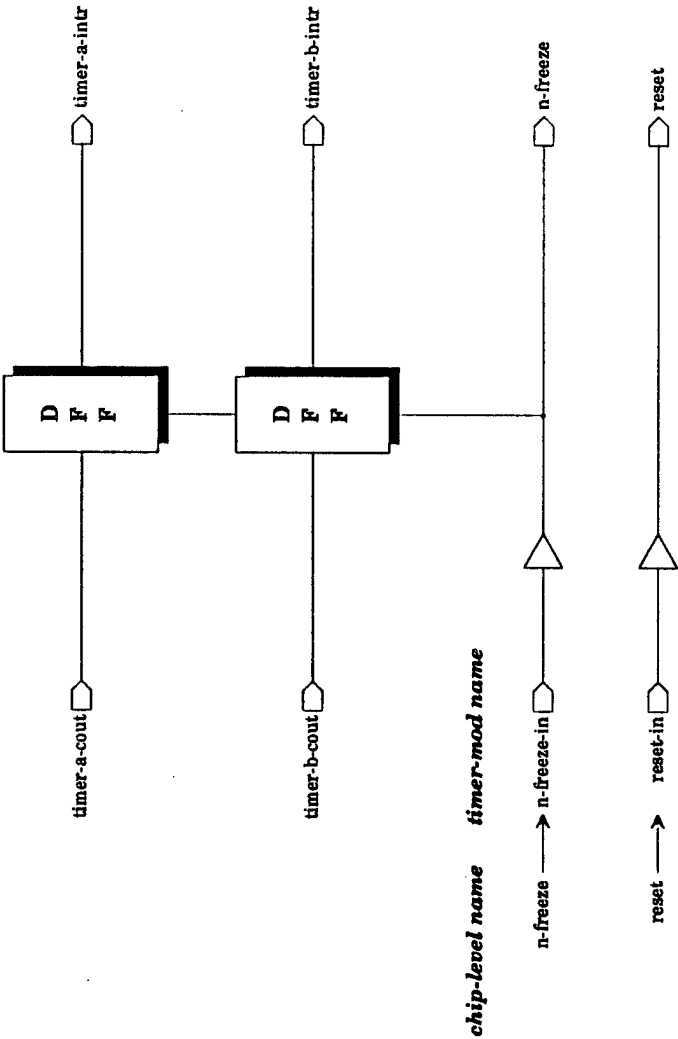
tp-en-dec

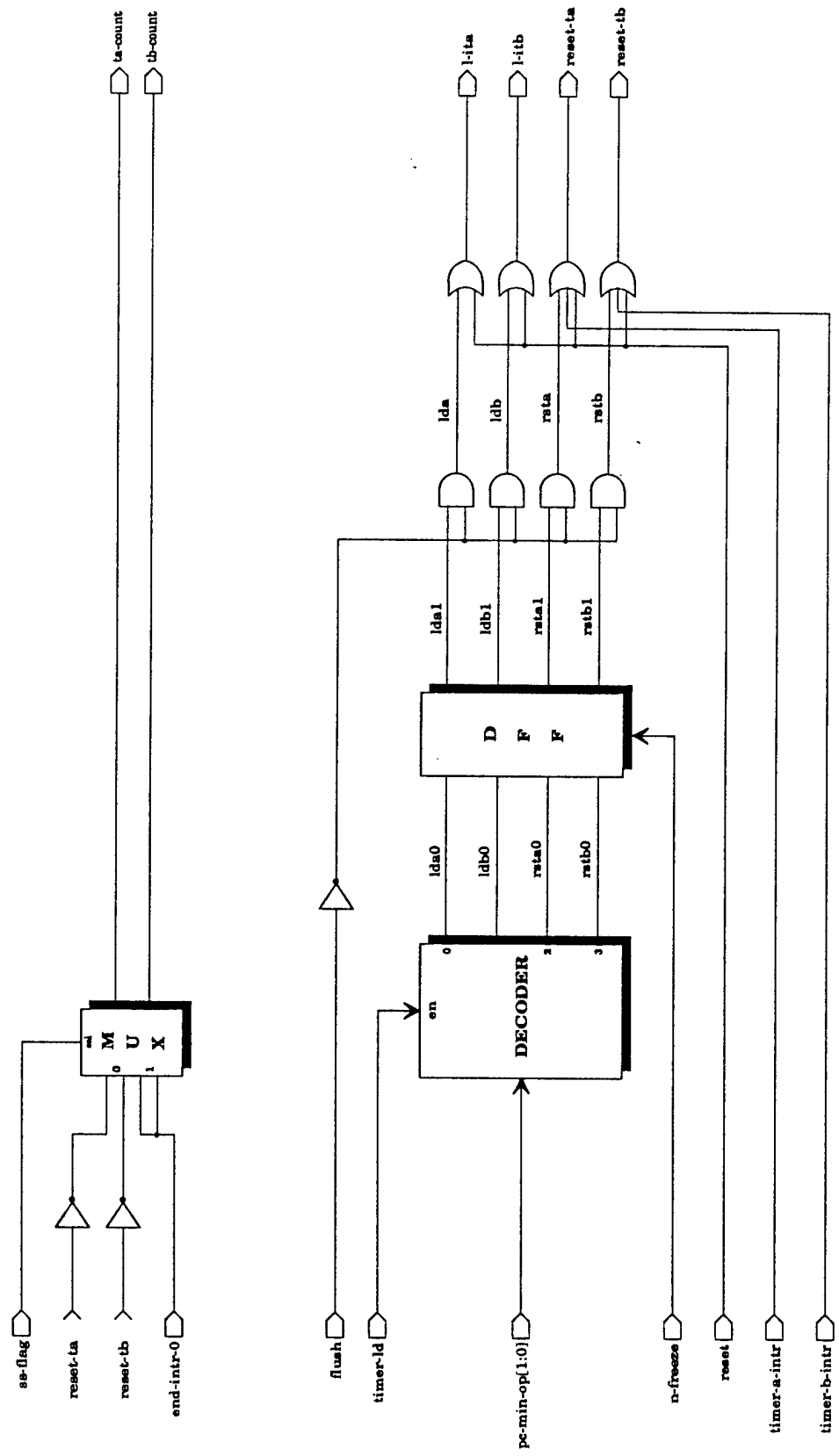
V:\GT-VIAG\TIMER-MDDR



timer-mod

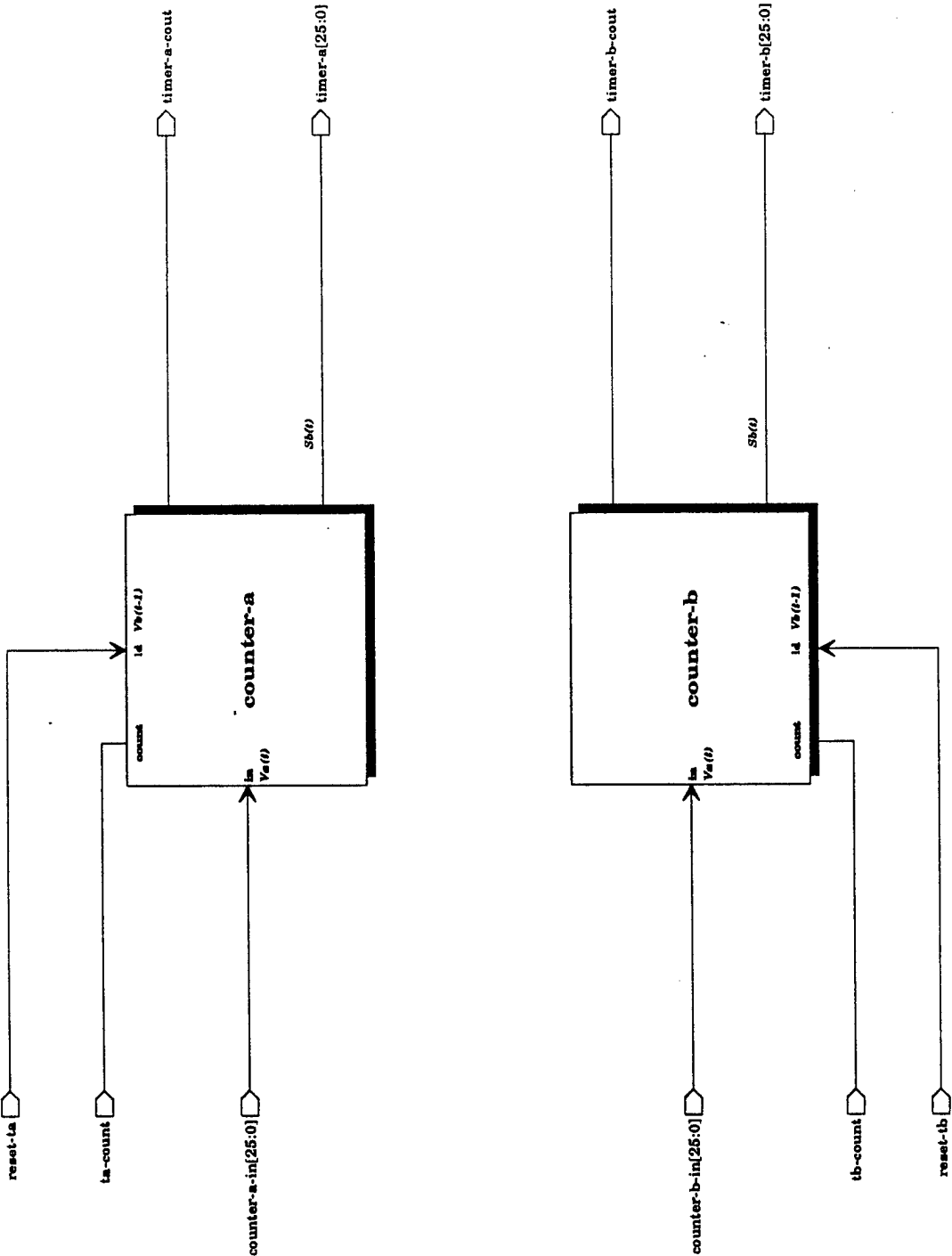
**timer-dp**



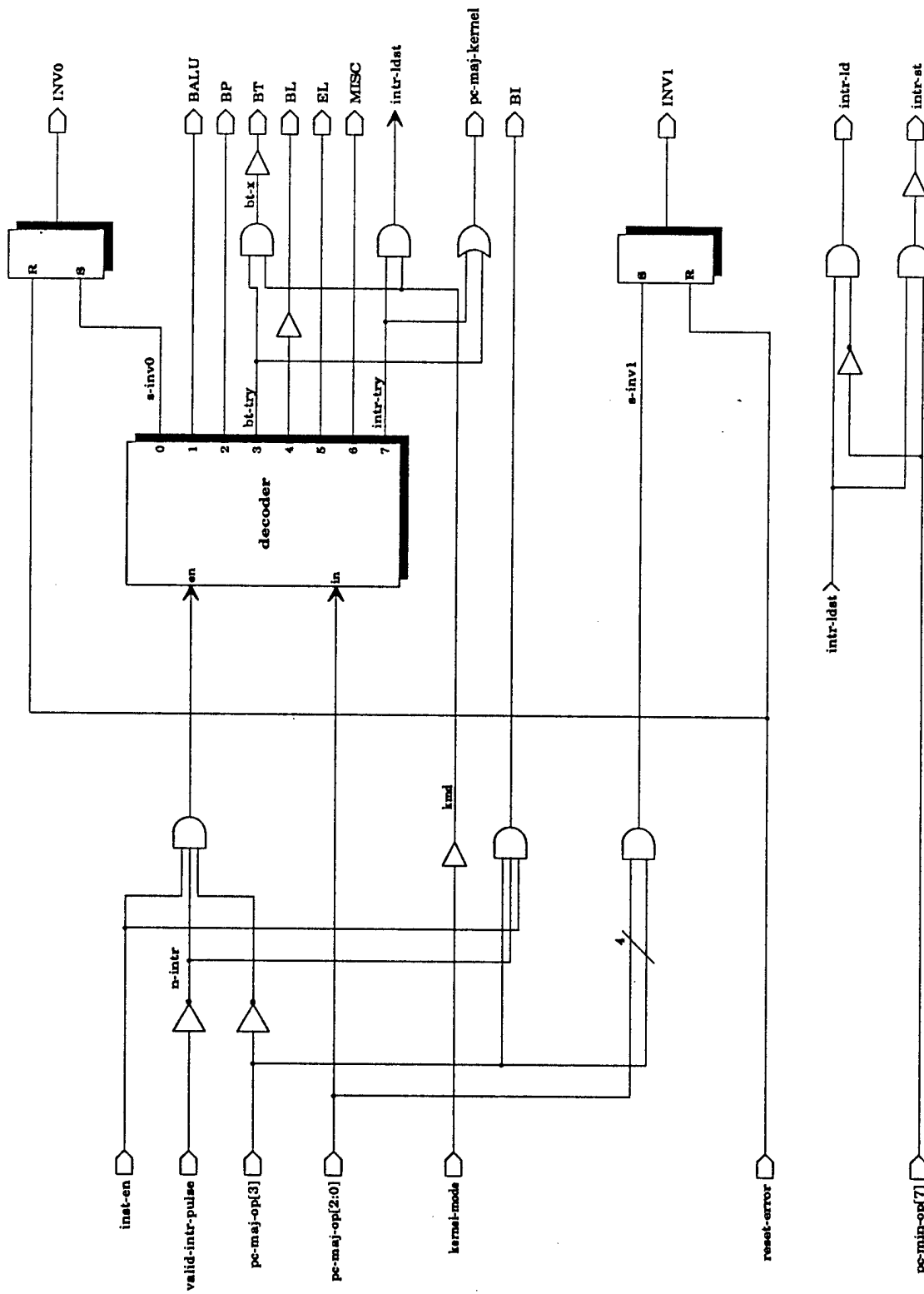


timer-ld-dec

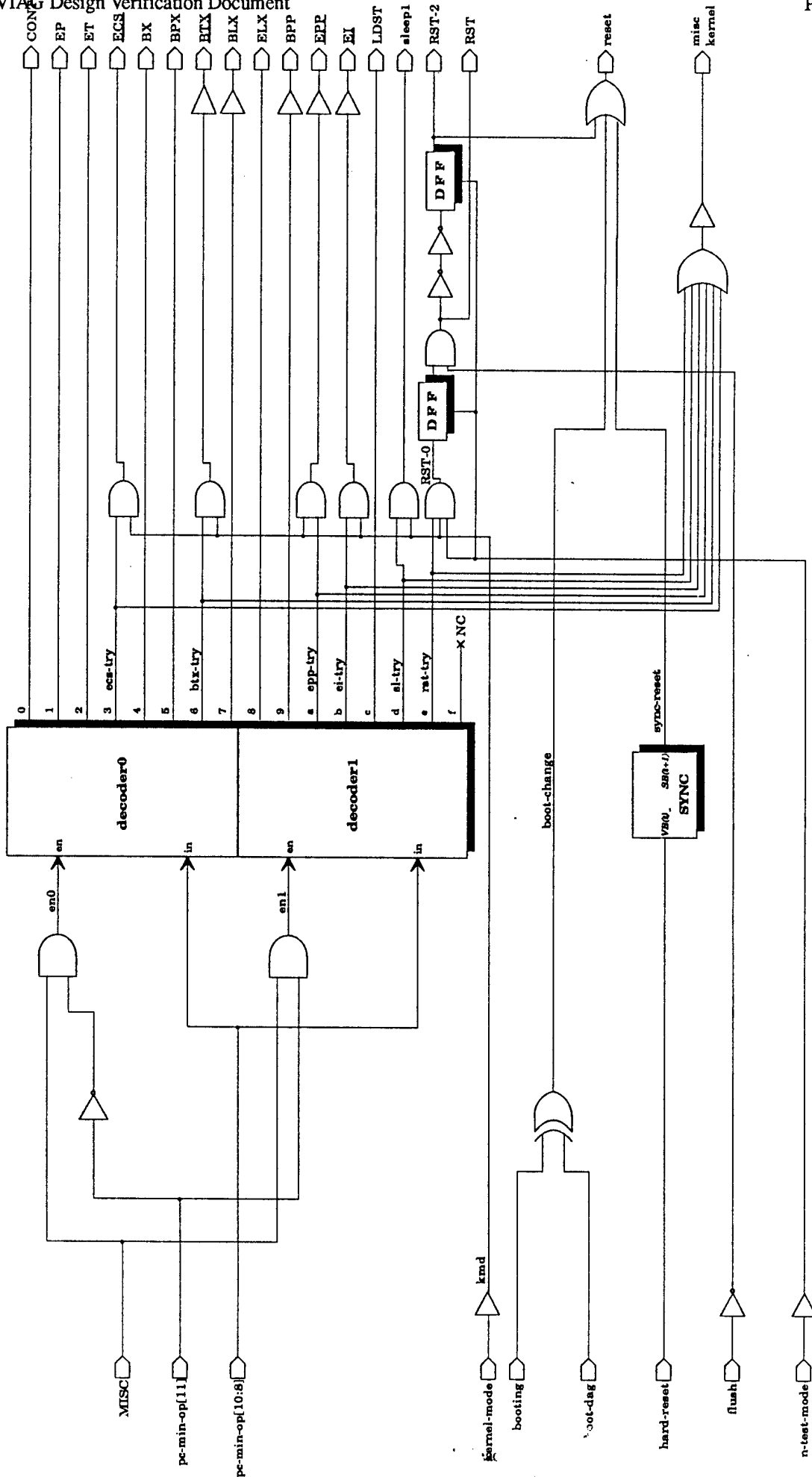
V:\GT-VIAG\CONTACTS.DRW



counter-a & counter-b

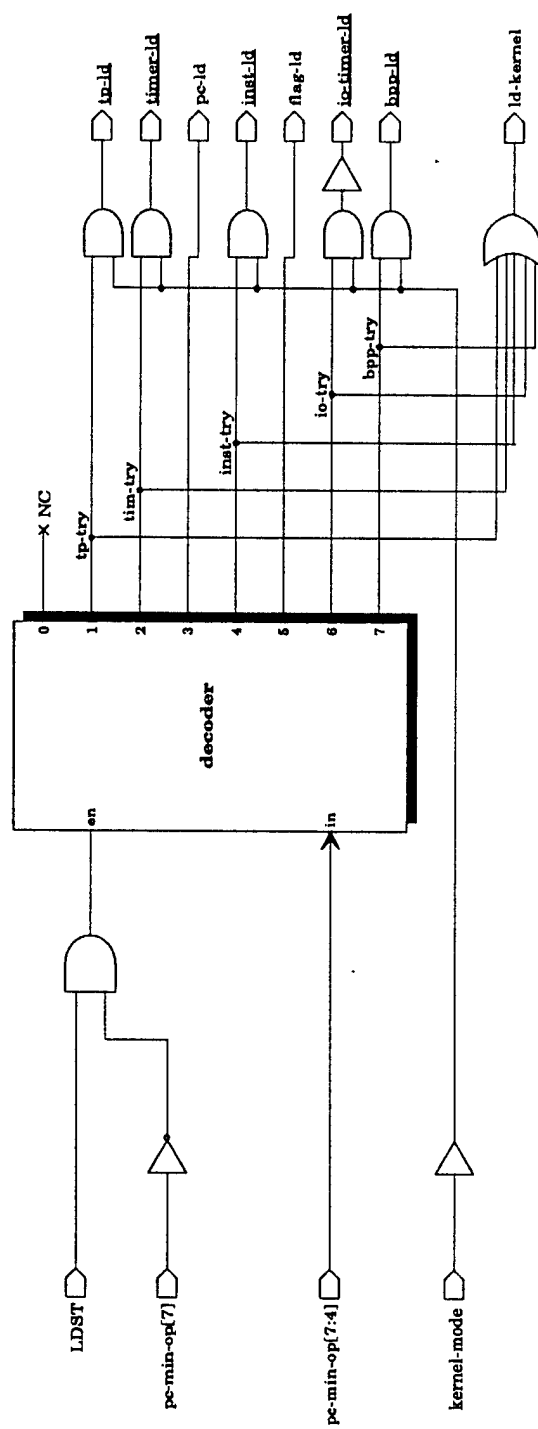


pc-maj-dec

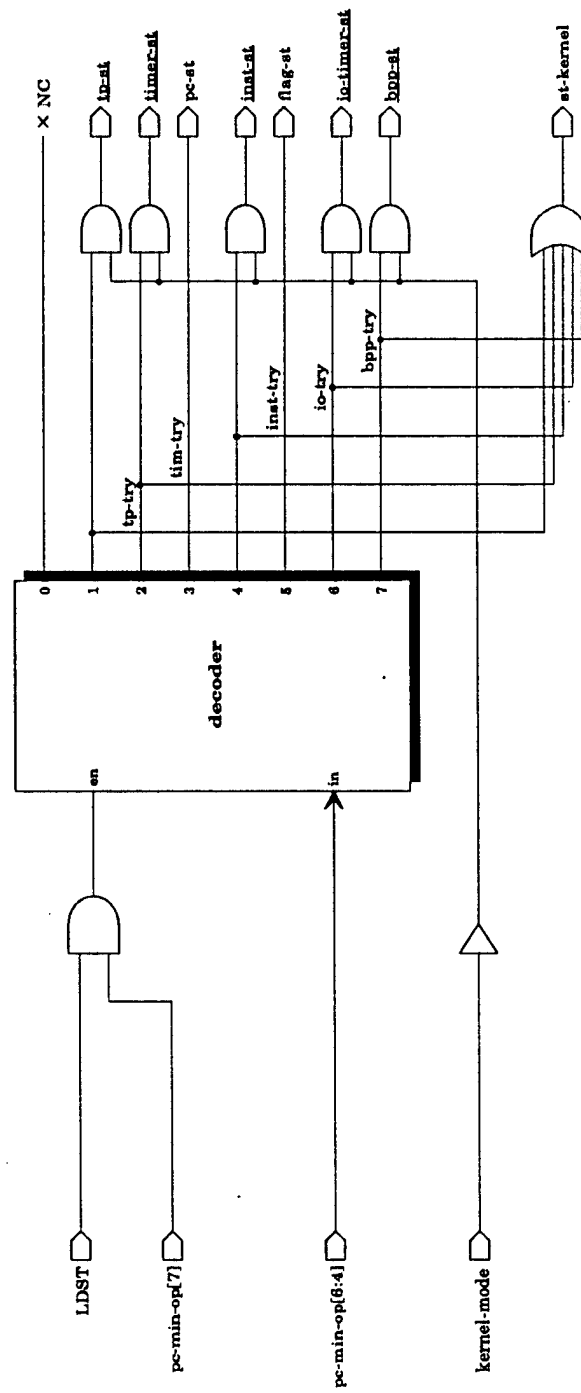


MISC-dec

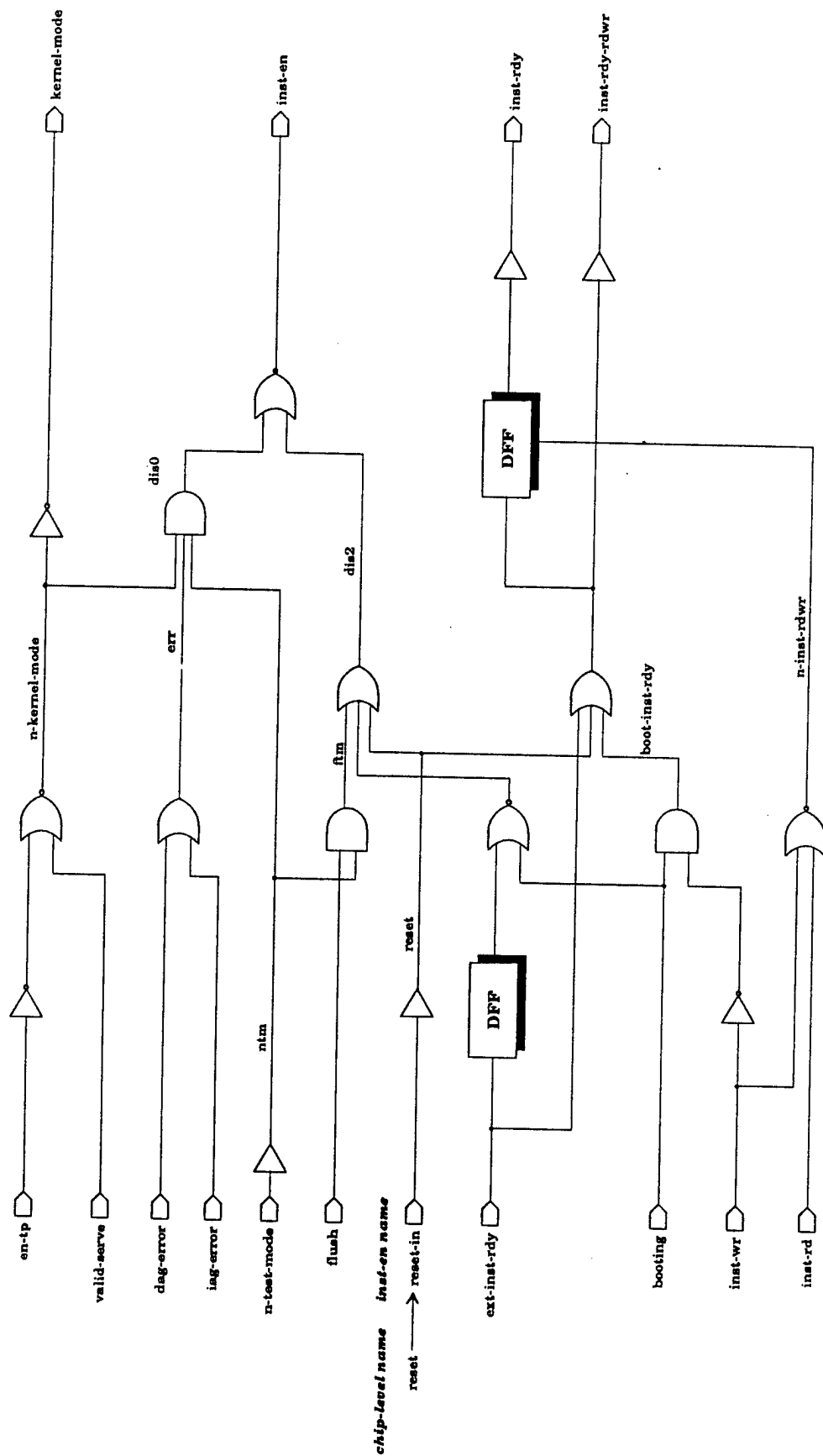
v:\gt-viag\misc-dec.dwg



LD-dec



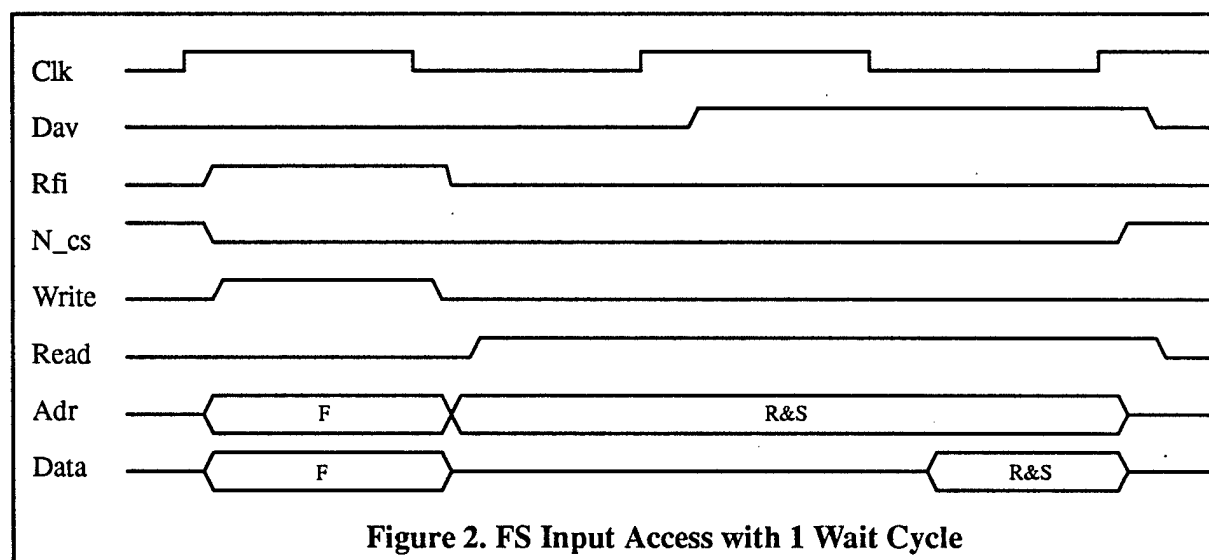
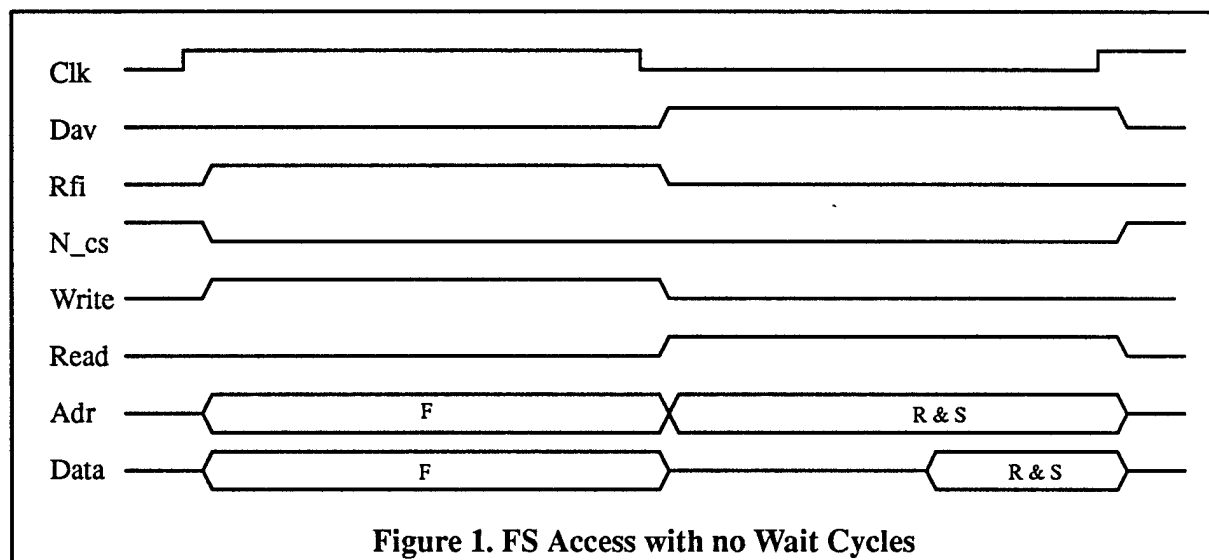
ST-dec

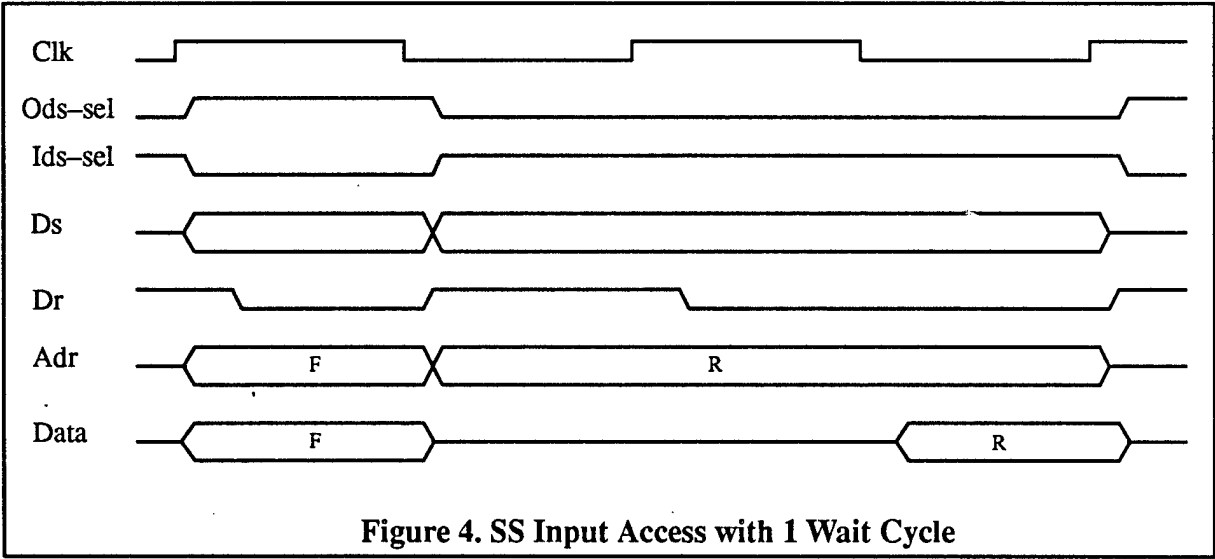
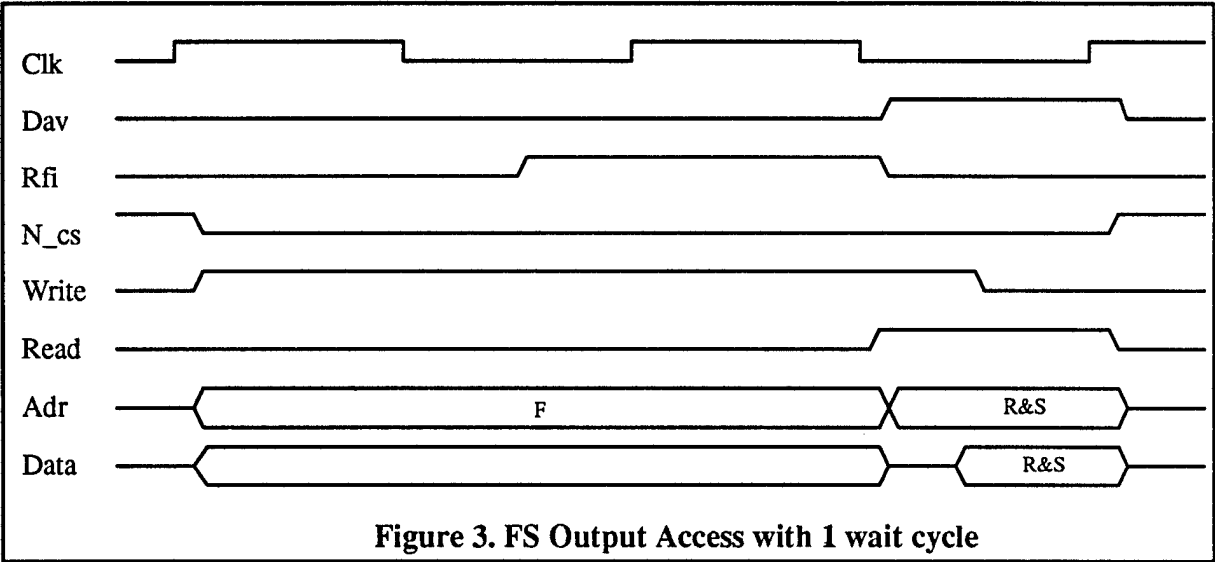
**inst-en**

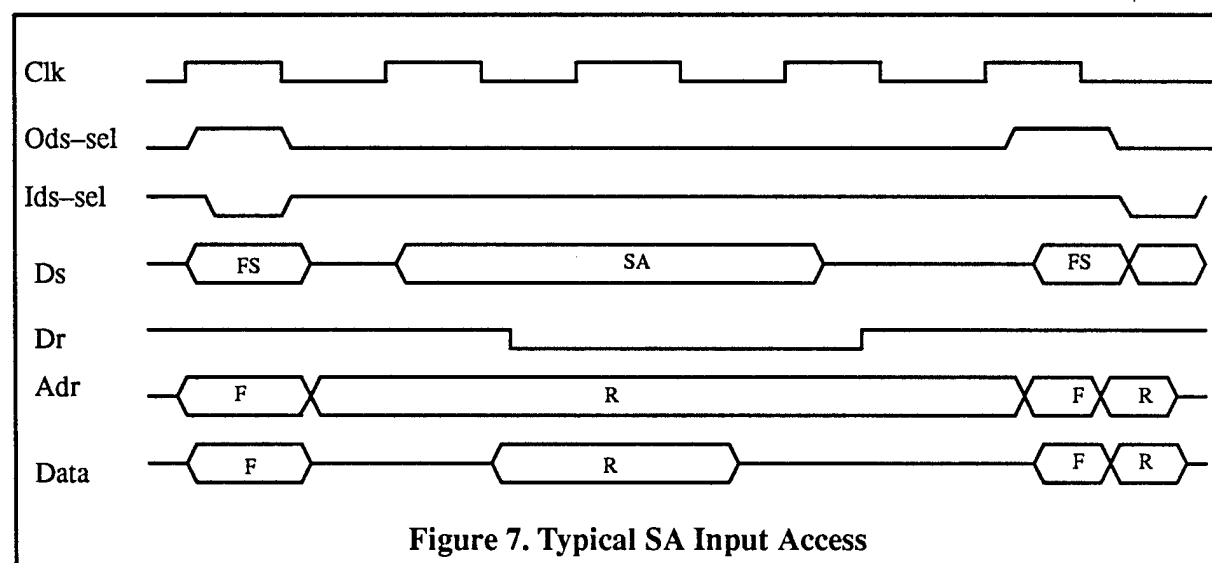
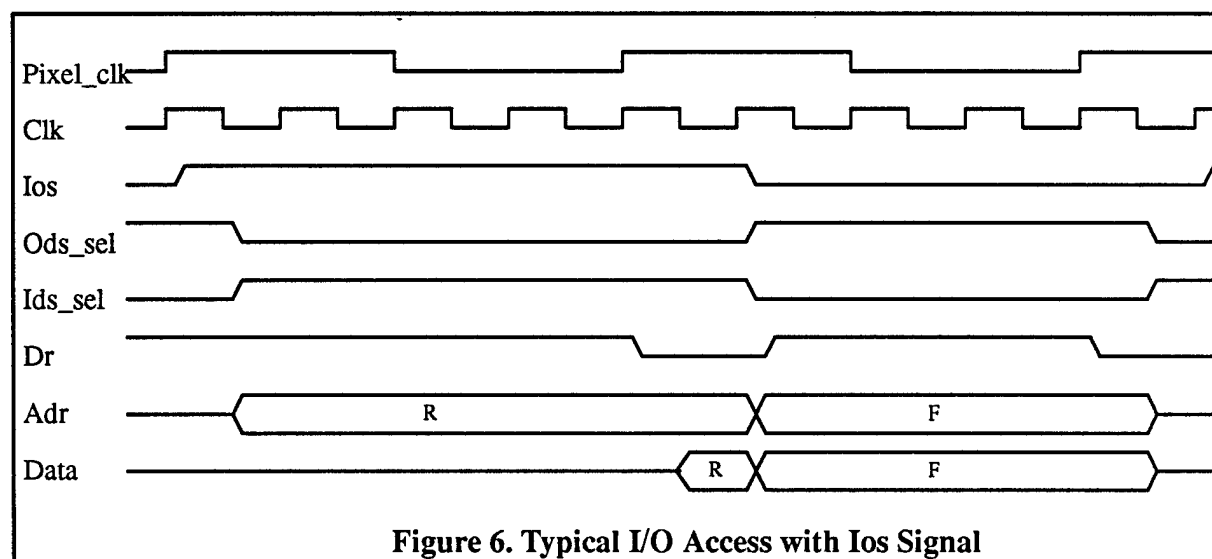
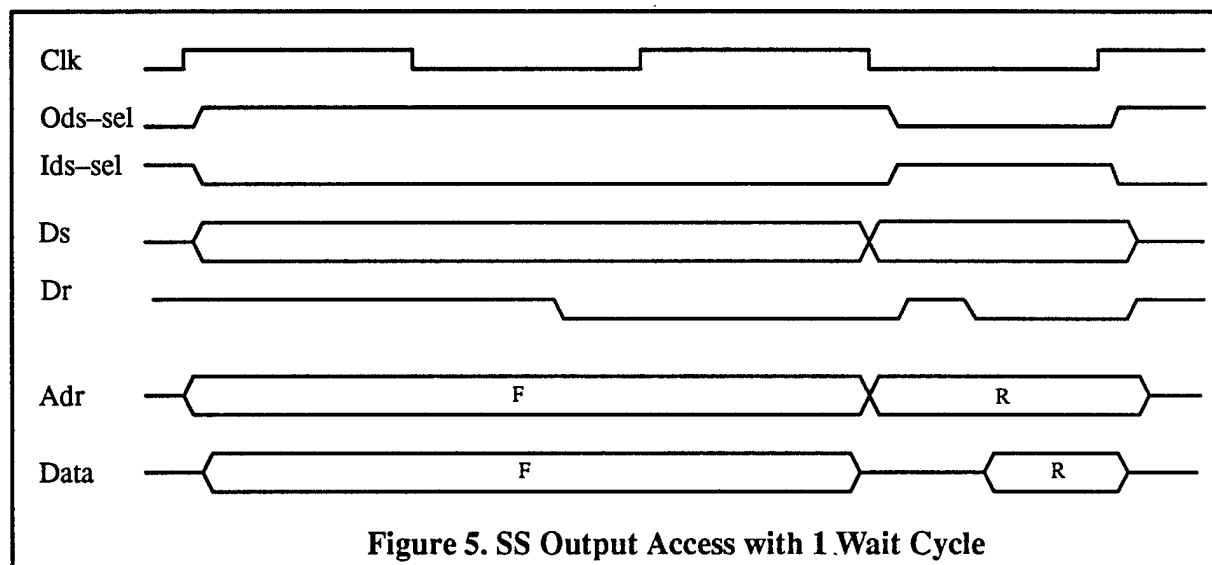
6. Timing Diagrams

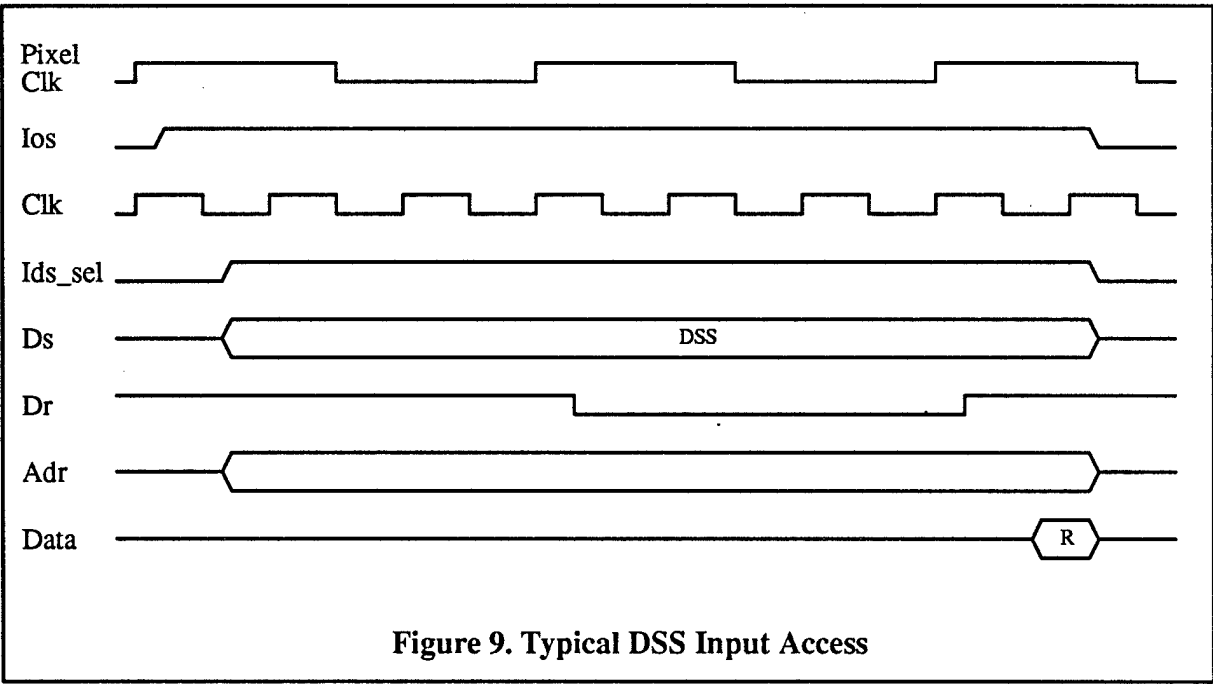
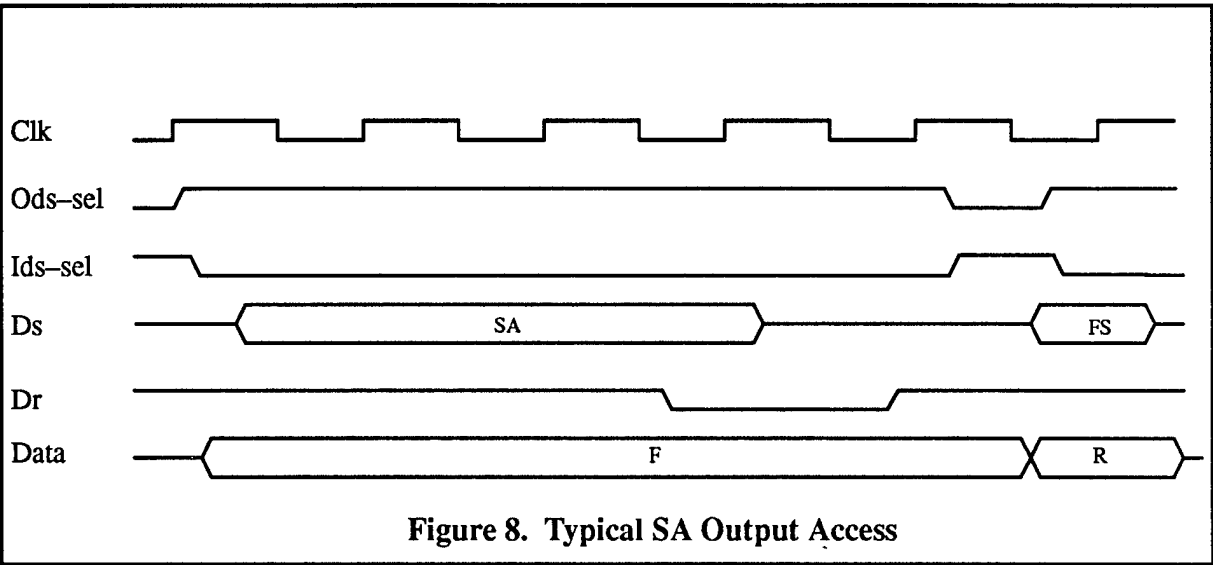
The following are timing diagrams of the various types of I/O that the GT-EP chipset supports. A more complete description of the interface can be found in the GT-EP I/O Interface Specification.

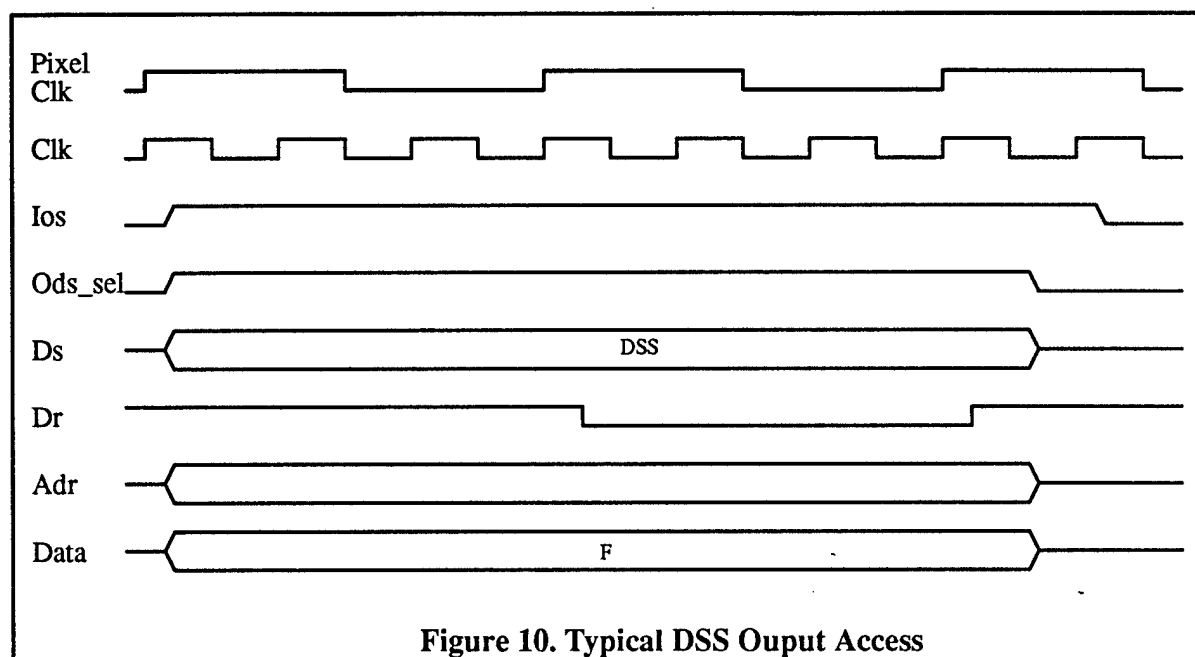
a











7. Pin Description

Pin#	Loc.	Signal Name	Abbrev.	Pad Type	Strength	Timing
1	B1	FALSE	FALSE	VSS CORE		
2	C4	Inst[12]	Inst_12	DATA IO	DRVSPEED1,NORM	
3	C2	TRUE	TRUE	VDD EDGE		
4	C3	Inst[13]	Inst_13	DATA IO	DRVSPEED1,NORM	
5	C1	FALSE	FALSE	VSS CORE		
6	D4	Inst[14]	Inst_14	DATA IO	DRVSPEED1,NORM	
7	D2					
8	D3	Inst[15]	Inst_15	DATA IO	DRVSPEED1,NORM	
9	F4	Inst[16]	Inst_16	DATA IO	DRVSPEED1,NORM	
10	G4	Inst[17]	Inst_17	DATA IO	DRVSPEED1,NORM	
11	D1	Inst[18]	Inst_18	DATA IO	DRVSPEED1,NORM	
12	E4	Inst[19]	Inst_19	DATA IO	DRVSPEED1,NORM	
13	E1	Inst[20]	Inst_20	DATA IO	DRVSPEED1,NORM	
14	E3	Inst[21]	Inst_21	DATA IO	DRVSPEED1,NORM	
15	F2	Inst[22]	Inst_22	DATA IO	DRVSPEED1,NORM	
16	E2	Inst[23]	Inst_23	DATA IO	DRVSPEED1,NORM	
17	F1	FALSE	FALSE	VSS EDGE		
18	F3	Inst[24]	Inst_24	DATA IO	DRVSPEED1,NORM	
19	G1	Inst[25]	Inst_25	DATA IO	DRVSPEED1,NORM	
20	G3	FALSE	FALSE	VSS CORE		
21	H2	Inst[26]	Inst_26	DATA IO	DRVSPEED1,NORM	
22	G2	Inst[27]	Inst_27	DATA IO	DRVSPEED1,NORM	
23	H1	TRUE	TRUE	VDD EDGE		
24	H4	Inst[28]	Inst_28	DATA IO	DRVSPEED1,NORM	
25	J1	Inst[29]	Inst_29	DATA IO	DRVSPEED1,NORM	
26	H3	Inst[31]	Inst_31	DATA IO	DRVSPEED1,NORM	
27	J2	Inst[30]	Inst_30	DATA IO	DRVSPEED1,NORM	
28	H5	Inst[32]	Inst_32	DATA IO	DRVSPEED1,NORM	
29	J5	Inst[33]	Inst_33	DATA IO	DRVSPEED1,NORM	
30	K1	Inst[34]	Inst_34	DATA IO	DRVSPEED1,NORM	
31	J4	Inst[35]	Inst_35	DATA IO	DRVSPEED1,NORM	
32	K2	FALSE	FALSE	VSS CORE		
33	J3	Inst[36]	Inst_36	DATA IO	DRVSPEED1,NORM	
34	L1	FALSE	FALSE	VSS EDGE		
35	K3	Inst[37]	Inst_37	DATA IO	DRVSPEED1,NORM	
36	M1	Status[3]	Status_3	DATA IN	NORMAL	
37	K4	Status[4]	Status_4	DATA IN	NORMAL	
38	N1	Inst[40]	Inst_40	DATA IO	DRVSPEED1,NORM	
39	K5	Inst[38]	Inst_38	DATA IO	DRVSPEED1,NORM	
40	M2	Inst[39]	Inst_39	DATA IO	DRVSPEED1,NORM	
41	L3	Pixel_clk	Pxl_clk	DATA IN	NORMAL	
42	P1	Ios	Ios	DATA OUT	DRVSPEED1	
43	L2	N_write[1]	Nwrt_1	DATA OUT	DRVSPEED1	
44	R1	Ncs[2]	Ncs_2	DATA OUT	DRVSPEED1	
45	M3	Read[2]	Read_2	DATA OUT	DRVSPEED1	
46	M4	Write[2]	Write_2	DATA OUT	DRVSPEED1	
47	L4	Ncs[3]	Ncs_3	DATA OUT	DRVSPEED1	
48	P2	Read[3]	Read_3	DATA OUT	DRVSPEED1	

49	N2	Write[3]	Write_3	DATA OUT	DRVSPEED1
50	T1				
51	N3	Ids_freeze	Ids_frz	DATA OUT	DRVSPEED1
52	R2	Ods_freeze	Ods_frz	DATA OUT	DRVSPEED1
53	N4	RFI[2]	RFI_2	DATA IN	NORMAL
54	U1	RFI[3]	RFI_3	DATA IN	NORMAL
55	P3	IAG_test[1]	IAG_tst1	DATA IN	NORMAL
56	T2	RFI[1]	RFI_1	DATA IN	NORMAL
57	T3	IAG_test[0]	IAG_tst0	DATA IN	NORMAL
58	P4	TRUE	TRUE	VDD CORNER	
59	U2	DAV[2]	DAV_2	DATA IN	NORMAL
60	R3	DAV[1]	DAV_1	DATA IN	NORMAL
61	U3	N_read[1]	Nread_1	DATA OUT	DRVSPEED1
62	T4	DAV[3]	DAV_3	DATA IN	NORMAL
63	U4				
64	P5	Ncs[1]	Ncs_1	DATA OUT	DRVSPEED1
65	P6	Ids_sel	Ids_sel	DATA OUT	DRVSPEED1
66	N7	Inst[41]	Inst_41	DATA IO	DRVSPEED1
67	T5	Pc[0]	Pc_0	DATA OUT	DRVSPEED3
68	R4	Pc[2]	Pc_2	DATA OUT	DRVSPEED3
69	U5	FALSE	FALSE	VSS EDGE	
70	R5	TRUE	TRUE	VDD EDGE	
71	T6	Pc[1]	Pc_1	DATA OUT	DRVSPEED3
72	R6	Pc[3]	Pc_3	DATA OUT	DRVSPEED3
73	U6	Pc[4]	Pc_4	DATA OUT	DRVSPEED3
74	P7	Pc[5]	Pc_5	DATA OUT	DRVSPEED3
75	U7	Pc[6]	Pc_6	DATA OUT	DRVSPEED3
76	R7	Pc[7]	Pc_7	DATA OUT	DRVSPEED3
77	T8	Pc[8]	Pc_8	DATA OUT	DRVSPEED3
78	T7	Pc[9]	Pc_9	DATA OUT	DRVSPEED3
79	U8	FALSE	FALSE	VSS EDGE	
80	P8	TRUE	TRUE	VDD EDGE	
81	U9	Pc[10]	Pc_10	DATA OUT	DRVSPEED3
82	R8	Pc[11]	Pc_11	DATA OUT	DRVSPEED3
83	T9	Pc[12]	Pc_12	DATA OUT	DRVSPEED3
84	N8	Pc[13]	Pc_13	DATA OUT	DRVSPEED3
85	N9	TRUE	TRUE	CLOCK VDD	
86	U10	FALSE	FALSE	CLOCK VSS	
87	P9	Clk	Clk	CLOCK	
88	T10	Pc[14]	Pc_14	DATA OUT	DRVSPEED3
89	R9	TRUE	TRUE	VDD EDGE	
90	U11	Pc[15]	Pc_15	DATA OUT	DRVSPEED3
91	R10	Pc[16]	Pc_16	DATA OUT	DRVSPEED3
92	U12	Pc[17]	Pc_17	DATA OUT	DRVSPEED3
93	N10	Pc[18]	Pc_18	DATA OUT	DRVSPEED3
94	T12	Pc[19]	Pc_19	DATA OUT	DRVSPEED3
95	P10	FALSE	FALSE	VSS EDGE	
96	U13	Pc[20]	Pc_20	DATA OUT	DRVSPEED3
97	T11	Pc[21]	Pc_21	DATA OUT	DRVSPEED3
98	T13	Pc[23]	Pc_23	DATA OUT	DRVSPEED3
99	R11	Pc[24]	Pc_24	DATA OUT	DRVSPEED3

100	U14	TRUE	TRUE	VDD EDGE	
101	P11	Pc[22]	Pc_22	DATA OUT	DRVSPEED3
102	U15	Pc[25]	Pc_25	DATA OUT	DRVSPEED3
103	N11	Intr[0]	Intr_0	DATA IN	NORMAL
104	P12	Intr[1]	Intr_1	DATA IN	NORMAL
105	R12	Intr[2]	Intr_2	DATA IN	NORMAL
106	T15				
107	R13	Intr[4]	Intr_4	DATA IN	NORMAL
108	U16	Intr[3]	Intr_3	DATA IN	NORMAL
109	T14	Intr[6]	Intr_6	DATA IN	NORMAL
110	U17	Intr[5]	Intr_5	DATA IN	NORMAL
111	P13	Intr[8]	Intr_8	DATA IN	NORMAL
112	T16	Intr[7]	Intr_7	DATA IN	NORMAL
113	T17	Ods_sel	Ods_sel	DATA OUT	DRVSPEED1
114	R14	FALSE	FALSE	VSS CORNER	
115	R16	Ids_eq_ods_2	Ids_eq_ods2	DATA OUT	DRVSPEED1
116	R15	Guard	Guard	DATA OUT	DRVSPEED1
117	R17	Dr	Dr	DATA IO	DRVSPEED3,NORM
118	P14	Ids_eq_ods_1	Ids_eq_ods1	DATA OUT	DRVSPEED1
119	P16				
120	P15	TRUE	TRUE	VDD CORE	
121	P17	TRUE	TRUE	VDD EDGE	
122	L14	Ods_ids[3]	Oids_3	DATA OUT	DRVSPEED1
123	M14	Ods_ids[2]	Oids_2	DATA OUT	DRVSPEED1
124	N14	Ods_ids[1]	Oids_1	DATA OUT	DRVSPEED1
125	N17	FALSE	FALSE	VSS EDGE	
126	N15	Ods_ids[0]	Oids_0	DATA OUT	DRVSPEED1
127	M16	RF[0]	RF_0	DATA IO	DRVSPEED1,NORM
128	N16	RF[1]	RF_1	DATA IO	DRVSPEED1,NORM
129	M17	RF[2]	RF_2	DATA IO	DRVSPEED1,NORM
130	M15	RF[3]	RF_3	DATA IO	DRVSPEED1,NORM
131	L17	RF[4]	RF_4	DATA IO	DRVSPEED1,NORM
132	L15	RF[5]	RF_5	DATA IO	DRVSPEED1,NORM
133	K16	RF[6]	RF_6	DATA IO	DRVSPEED1,NORM
134	L16	RF[7]	RF_7	DATA IO	DRVSPEED1,NORM
135	K17	TRUE	TRUE	VDD CORE	
136	K14	RF[9]	RF_9	DATA IO	DRVSPEED1,NORM
137	J17	RF[8]	RF_8	DATA IO	DRVSPEED1,NORM
138	K15	TRUE	TRUE	VDD EDGE	
139	J16	RF[10]	RF_10	DATA IO	DRVSPEED1,NORM
140	K13	FALSE	FALSE	VSS EDGE	
141	J13	RF[11]	RF_11	DATA IO	DRVSPEED1,NORM
142	H17	RF[12]	RF_12	DATA IO	DRVSPEED1,NORM
143	J14	RF[13]	RF_13	DATA IO	DRVSPEED1,NORM
144	H16	Zero	Zero	DATA IN	NORMAL
145	J15	Sign	Sign	DATA IN	NORMAL
146	G17	Carry	Carry	DATA IN	NORMAL
147	H15	Flush	Flush	DATA OUT	DRVSPEED1
148	F17	ALU_Flag	ALU_Flag	DATA IN	NORMAL
149	H14	RF[14]	RF_14	DATA IO	DRVSPEED1,NORM
150	F14	RF[16]	RF_16	DATA IO	DRVSPEED1,NORM

151	H13	RF[17]	RF_17	DATA IO	DRVSPEED1,NORM
152	F16	RF[19]	RF_19	DATA IO	DRVSPEED1,NORM
153	G15	RF[15]	RF_15	DATA IO	DRVSPEED1,NORM
154	D17	TRUE	TRUE	VDD CORE	
155	G16	RF[18]	RF_18	DATA IO	DRVSPEED1,NORM
156	C17	Inst[43]	Inst_43	DATA IO	DRVSPEED1,NORM
157	F15	RF[20]	RF_20	DATA IO	DRVSPEED1,NORM
158	D16	RF[21]	RF_21	DATA IO	DRVSPEED1,NORM
159	G14	Inst[42]	Inst_42	DATA IO	DRVSPEED1,NORM
160	F14				
161	E16	TRUE	TRUE	VDD EDGE	
162	B17	RF[22]	RF_22	DATA IO	DRVSPEED1,NORM
163	E15	FALSE	FALSE	VSS EDGE	
164	C16	ALU_opcode[7]	ALUOp_7	DATA OUT	DRVSPEED1
165	E14	ALU_opcode[6]	ALUOp_6	DATA OUT	DRVSPEED1
166	A17	RF[23]	RF_23	DATA IO	DRVSPEED1,NORM
167	D15	TRUE	TRUE	VDD CORE	
168	B16	RF[24]	RF_24	DATA IO	DRVSPEED1,NORM
169	B15	RF[25]	RF_25	DATA IO	DRVSPEED1,NORM
170	D14	TRUE	TRUE	VDD CORNER	
171	A16	ALU_opcode[0]	ALUOp_0	DATA OUT	DRVSPEED1
172	C15	ALU_opcode[1]	ALUOp_1	DATA OUT	DRVSPEED1
173	A15	ALU_opcode[3]	ALUOp_3	DATA OUT	DRVSPEED1
174	B14	ALU_opcode[4]	ALUOp_4	DATA OUT	DRVSPEED1
175	A14				
176	D13	ALU_opcode[5]	ALUOp_5	DATA OUT	DRVSPEED1
177	D12	Inst[44]	Inst_44	DATA IO	DRVSPEED1,NORM
178	E11	Inst[45]	Inst_45	DATA IO	DRVSPEED1,NORM
179	B13	RF[26]	RF_26	DATA IO	DRVSPEED1,NORM
180	C14	RF[27]	RF_27	DATA IO	DRVSPEED1,NORM
181	A13	ALU_opcode[2]	ALUOp_2	DATA OUT	DRVSPEED1
182	C13	RF[28]	RF_28	DATA IO	DRVSPEED1,NORM
183	B12	RF[29]	RF_29	DATA IO	DRVSPEED1,NORM
184	C12	RF[30]	RF_30	DATA IO	DRVSPEED1,NORM
185	A12	RF[31]	RF_31	DATA IO	DRVSPEED1,NORM
186	D11	Valid_intr_pulse	Vintr_p	DATA OUT	DRVSPEED1
187	A11	TRUE	TRUE	VDD EDGE	
188	C11	FALSE	FALSE	VSS EDGE	
189	B10	Inst_rdy	Inst_rdy	DATA IN	NORMAL
190	B11	DAG_error	DAG_err	DATA IN	NORMAL
191	A10	N_reset	N_reset	DATA IN	NORMAL
192	D10	R_eq_f_1	Reqf_1	DATA IN	NORMAL
193	A9	Inst_rd	Inst_rd	DATA OUT	DRVSPEED1
194	C10	Freeze	Freeze	DATA OUT	DRVSPEED1
195	B9	N_inst_wr	Ninst_wr	DATA OUT	DRVSPEED1
196	E10	Status[0]	Status_0	DATA IN	NORMAL
197	E9	Kernel_mode	Krnl_md	DATA OUT	DRVSPEED1
198	A8	TRUE	TRUE	VDD EDGE	
199	D9	Status[1]	Status_1	DATA IN	NORMAL
200	B8	N_reset_out	Nrst_out	DATA OUT	DRVSPEED1
201	C9	Inst_en	Inst_en	DATA OUT	DRVSPEED1

202	A7	DAG_R_en	DAG_R_en	DATA OUT	DRVSPEED1
203	C8	N_cs_pha	Ncs_pha	DATA OUT	DRVSPEED1
204	A6	N_cs_phb	Ncs_phb	DATA OUT	DRVSPEED1
205	E8	R_eq_f_2	Reqf_2	DATA IN	NORMAL
206	B6	S_eq_f_1	Seqf_1	DATA IN	NORMAL
207	D8	S_eq_f_2	Seqf_2	DATA IN	NORMAL
208	A5	Booting	Booting	DATA OUT	DRVSPEED1
209	B7	Inst[0]	Inst_0	DATA IO	DRVSPEED1,NORM
210	B5	Inst[1]	Inst_1	DATA IO	DRVSPEED1,NORM
211	C7	FALSE	FALSE	VSS EDGE	
212	A4	Status[2]	Status_2	DATA IN	NORMAL
213	D7	Inst[2]	Inst_2	DATA IO	DRVSPEED1,NORM
214	D6	Inst[3]	Inst_3	DATA IO	DRVSPEED1,NORM
215	E7	Inst[4]	Inst_4	DATA IO	DRVSPEED1,NORM
216	A3				
217	C6	Inst[6]	Inst_6	DATA IO	DRVSPEED1,NORM
218	B3	Inst[5]	Inst_5	DATA IO	DRVSPEED1,NORM
219	C5	Inst[7]	Inst_7	DATA IO	DRVSPEED1,NORM
220	A2	FALSE	FALSE	VSS EDGE	
221	B4	Inst[9]	Inst_9	DATA IO	DRVSPEED1,NORM
222	A1	Inst[8]	Inst_8	DATA IO	DRVSPEED1,NORM
223	D5	Inst[11]	Inst_11	DATA IO	DRVSPEED1,NORM
224	B2	Inst[10]	Inst_10	DATA IO	DRVSPEED1,NORM

8. Key Parameters

```

) Key Parameters for Chip /tmp_mnt/net/yoda/mta/iag/iag/gt_vic/iag
) =====
)
) TIME = Mon Feb  4 15:02:45 1991
)
) ROUTE_VERSION = 8.00
) HEIGHT = 426.5 MILS
)   ( = 10833.1 u )
) WIDTH = 417.4 MILS
)   ( = 10601.9 u )
) ROUTED = 1 (0=NO,1=YES)
) TOTAL_WIRE_LENGTH = 1972764 MILS
)   ( = 50108205. u )
) CORE_AREA = 140707.9 SQUARE_MILS
)   ( = 90779114.4 u2 )
) PADRING_AREA = 37329.1 SQUARE_MILS
)   ( = 24083243. u2 )
) PAD_AREA = 33988.2 SQUARE_MILS
)   ( = 21927827. u2 )
) ROUTE_AREA = 103308.9 SQUARE_MILS
)   ( = 66650770.1 u2 )
) PERCENT_ROUTING_OF_CORE = 73 %
) PERCENT_ROUTING_OF_CHIP = 58 %
) PERCENT_CORE_OF_CHIP = 79 %
) PERCENT_PADRING_OF_CHIP = 20 %
) PERCENT_PAD_OF_PADRING = 91 %

```

```
)
) NETLIST_VERSION = 2.0
) NETLIST_EXISTS = 1 (0=NO,1=YES)
)
) PHASE_A_TIME = 42.6 NANOSECONDS
) PHASE_B_TIME = 46.3 NANOSECONDS
) SYMMETRIC_TIME = 92.6 NANOSECONDS
) NUMBER_OF_TRANSISTORS = 65190
) Key Parameters (set 124) Modified
) POWER DISSIPATION = 1180.46 MILLIWATTS @5V_10MHZ
)
)
) ROUTE_ESTIMATE_LVL = 0
) FLAT_ROUTE = 0 (0=NO,1=YES)
) TECHNOLOGY_NAME = CMOS-1
) PACKAGE_SPECIFIED = 1 (0=NO,1=YES)
) PACKAGE_NAME = CPGA224f2
) FABLINE_NAME = HP2_CN10B
) COMPILER_TYPE = GCX
)
) FLOORPLAN_VERSION = 8.0
) BOND_PAD_CNT = 216
) HEIGHT_ESTIMATE = 354.27 MILS
)   ( = 8998.457 u )
) WIDTH_ESTIMATE = 399.68 MILS
)   ( = 10151.87 u )
) FUSED = 1 (0=NO,1=YES)
) FUSION_REQUIRED = 1 (0=NO,1=YES)
) PINOUT = 1 (0=NO,1=YES)
) PINOUT_REQUIRED = 1 (0=NO,1=YES)
) PLACED = 1 (0=NO,1=YES)
) PLACEMENT_REQUIRED = 1 (0=NO,1=YES)
)
)
) DOWN_BONDS_ALLOWED = 1 (0=NO,1=YES)
) PKG_PIN_COUNT = 224
) PKG_WELL_HEIGHT = 480.00 MILS
)   ( = 12192.00 u )
) PKG_WELL_WIDTH = 480.00 MILS
)   ( = 12192.00 u )
) AREA = 178021.1 SQUARE_MILS
)   ( = 114852090. u2 )
) OBJECT_TYPE = Chip
) AREA_PER_TRANSISTOR = 2.730804 SQUARE_MILS
)   ( = 1761.80552 u2 )
) PHYSICAL_IMPLEMENTATIONS_EXIST = 0 (0=NO,1=YES)
) CHECKPOINTS_EXIST = 0 (0=NO,1=YES)
) CAN_SET_FABLINE = 1 (0=NO,1=YES)
)
) Key Parameter Listing Complete
```

9. PADRING.033

OUTPUT RINGS REPORT Version 1

Noise contribution:(ma/nh) Speed0: 2.50 Speed1: 5.00 Speed2: 8.33 Speed3: 16.66

Limits: Maximum noise level: 100. Unacceptable level: 150

Combined power pads do not supply clean power to the core.

Their use is discouraged

Ring under analysis: VDD

PAD NAME	EDGE	SPEED	DRIVE	PAD TYPE	SUPPLY	COMMENT

WARNING: pc_pad[13]	NORTH	3	CMOS	0		EXCESSIVE NOISE LEVEL
pc_pad[12]	NORTH	3	CMOS	1		OK
pc_pad[11]	NORTH	3	CMOS	1		OK
pc_pad[10]	NORTH	3	CMOS	1		OK
edge_vdd[8]	NORTH		POWER			
pc_pad[9]	NORTH	3	CMOS	1		OK
pc_pad[8]	NORTH	3	CMOS	1		OK
pc_pad[7]	NORTH	3	CMOS	1		OK
WARNING: pc_pad[6]	NORTH	3	CMOS	0		EXCESSIVE NOISE LEVEL
WARNING: pc_pad[5]	NORTH	3	CMOS	0		EXCESSIVE NOISE LEVEL
pc_pad[4]	NORTH	3	CMOS	1		OK
pc_pad[3]	NORTH	3	CMOS	1		OK
pc_pad[1]	NORTH	3	CMOS	2		OK
edge_vdd[2]	NORTH		POWER			
pc_pad[2]	NORTH	3	CMOS	2		OK
pc_pad[0]	NORTH	3	CMOS	2		OK
inst5_pad[1]	NORTH	1	CMOS	2		OK
ids_sel_pad	NORTH	1	CMOS	2		OK
dev1_pads[0]	NORTH	1	CMOS	2		OK
dev1_pads[1]	NORTH	1	CMOS	1		OK
corner_vdd[0]	NORTH		POWER			
io_freeze_pad[1]	EAST	1	CMOS	1		OK
io_freeze_pad[0]	EAST	1	CMOS	1		OK
dev3_pads[2]	EAST	1	CMOS	1		OK
dev3_pads[1]	EAST	1	CMOS	1		OK
dev3_pads[0]	EAST	1	CMOS	1		OK
dev2_pads[2]	EAST	1	CMOS	1		OK
WARNING: dev2_pads[1]	EAST	1	CMOS	0		EXCESSIVE NOISE LEVEL
WARNING: dev2_pads[0]	EAST	1	CMOS	0		EXCESSIVE NOISE LEVEL
WARNING: dev1_pads[2]	EAST	1	CMOS	0		EXCESSIVE NOISE LEVEL
WARNING: ios_pad	EAST	1	CMOS	0		EXCESSIVE NOISE LEVEL
WARNING: inst4_pad[7]	EAST	1	CMOS	0		EXCESSIVE NOISE LEVEL
WARNING: inst4_pad[6]	EAST	1	CMOS	0		EXCESSIVE NOISE LEVEL
WARNING: inst5_pad[0]	EAST	1	CMOS	0		EXCESSIVE NOISE LEVEL

inst4_pad[5]	EAST	1	CMOS	1	OK
inst4_pad[4]	EAST	1	CMOS	1	OK
inst4_pad[3]	EAST	1	CMOS	1	OK
inst4_pad[2]	EAST	1	CMOS	1	OK
inst4_pad[1]	EAST	1	CMOS	1	OK
inst4_pad[0]	EAST	1	CMOS	1	OK
inst3_pad[6]	EAST	1	CMOS	1	OK
inst3_pad[7]	EAST	1	CMOS	1	OK
inst3_pad[5]	EAST	1	CMOS	1	OK
inst3_pad[4]	EAST	1	CMOS	1	OK
edge_vdd[1]	EAST		POWER		
inst3_pad[3]	EAST	1	CMOS	1	OK
inst3_pad[2]	EAST	1	CMOS	1	OK
inst3_pad[1]	EAST	1	CMOS	1	OK
inst3_pad[0]	EAST	1	CMOS	1	OK
inst2_pad[7]	EAST	1	CMOS	2	OK
inst2_pad[6]	EAST	1	CMOS	2	OK
inst2_pad[5]	EAST	1	CMOS	2	OK
inst2_pad[4]	EAST	1	CMOS	2	OK
inst2_pad[3]	EAST	1	CMOS	2	OK
inst2_pad[2]	EAST	1	CMOS	2	OK
inst2_pad[1]	EAST	1	CMOS	1	OK
inst2_pad[0]	EAST	1	CMOS	1	OK
inst1_pad[7]	EAST	1	CMOS	1	OK
inst1_pad[6]	EAST	1	CMOS	1	OK
edge_vdd[0]	EAST		POWER		
inst1_pad[5]	EAST	1	CMOS	1	OK
inst1_pad[4]	EAST	1	CMOS	1	OK
inst1_pad[3]	SOUTH	1	CMOS	1	OK
inst1_pad[2]	SOUTH	1	CMOS	1	OK
inst1_pad[1]	SOUTH	1	CMOS	1	OK
inst1_pad[0]	SOUTH	1	CMOS	1	OK
inst0_pad[7]	SOUTH	1	CMOS	1	OK
inst0_pad[6]	SOUTH	1	CMOS	1	OK
inst0_pad[5]	SOUTH	1	CMOS	1	OK
inst0_pad[4]	SOUTH	1	CMOS	1	OK
inst0_pad[3]	SOUTH	1	CMOS	1	OK
inst0_pad[2]	SOUTH	1	CMOS	1	OK
inst0_pad[1]	SOUTH	1	CMOS	1	OK
inst0_pad[0]	SOUTH	1	CMOS	1	OK
boot_pad	SOUTH	1	CMOS	2	OK
csb_pad	SOUTH	1	CMOS	2	OK
csa_pad	SOUTH	1	CMOS	2	OK
dag_r_en_pad	SOUTH	1	CMOS	2	OK
inst_drv_pad	SOUTH	1	CMOS	2	OK
reset_out_pad	SOUTH	1	CMOS	2	OK
edge_vdd[7]	SOUTH		POWER		
kernel_mode_pad	SOUTH	1	CMOS	2	OK
n_inst_wr_pad	SOUTH	1	CMOS	2	OK
freeze_pad	SOUTH	1	CMOS	2	OK
inst_rd_pad	SOUTH	1	CMOS	2	OK
edge_vdd[6]	SOUTH		POWER		
valid_intr_pad	SOUTH	1	CMOS	2	OK

fr3_pad[7]	SOUTH	1	CMOS	2	OK
fr3_pad[6]	SOUTH	1	CMOS	2	OK
fr3_pad[5]	SOUTH	1	CMOS	2	OK
fr3_pad[4]	SOUTH	1	CMOS	2	OK
alu_op_pad[2]	SOUTH	1	CMOS	2	OK
fr3_pad[3]	SOUTH	1	CMOS	2	OK
fr3_pad[2]	SOUTH	1	CMOS	2	OK
inst5_pad[5]	SOUTH	1	CMOS	2	OK
inst5_pad[4]	SOUTH	1	CMOS	2	OK
alu_op_pad[5]	SOUTH	1	CMOS	2	OK
alu_op_pad[3]	SOUTH	1	CMOS	2	OK
alu_op_pad[4]	SOUTH	1	CMOS	2	OK
alu_op_pad[0]	SOUTH	1	CMOS	2	OK
alu_op_pad[1]	SOUTH	1	CMOS	2	OK
fr3_pad[1]	SOUTH	1	CMOS	2	OK
corner_vdd[1]	SOUTH		POWER		
fr3_pad[0]	WEST	1	CMOS	2	OK
alu_op_pad[6]	WEST	1	CMOS	2	OK
fr2_pad[7]	WEST	1	CMOS	2	OK
alu_op_pad[7]	WEST	1	CMOS	2	OK
edge_vdd[5]	WEST		POWER		
fr2_pad[6]	WEST	1	CMOS	2	OK
inst5_pad[2]	WEST	1	CMOS	2	OK
fr2_pad[5]	WEST	1	CMOS	2	OK
fr2_pad[4]	WEST	1	CMOS	2	OK
inst5_pad[3]	WEST	1	CMOS	2	OK
fr2_pad[2]	WEST	1	CMOS	2	OK
fr1_pad[7]	WEST	1	CMOS	2	OK
fr2_pad[3]	WEST	1	CMOS	2	OK
fr2_pad[1]	WEST	1	CMOS	2	OK
fr2_pad[0]	WEST	1	CMOS	2	OK
fr1_pad[6]	WEST	1	CMOS	1	OK
flush_pad	WEST	1	CMOS	1	OK
fr1_pad[5]	WEST	1	CMOS	1	OK
fr1_pad[4]	WEST	1	CMOS	1	OK
fr1_pad[3]	WEST	1	CMOS	1	OK
fr1_pad[2]	WEST	1	CMOS	1	OK
edge_vdd[4]	WEST		POWER		
fr1_pad[0]	WEST	1	CMOS	1	OK
fr1_pad[1]	WEST	1	CMOS	1	OK
fr0_pad[7]	WEST	1	CMOS	1	OK
fr0_pad[6]	WEST	1	CMOS	1	OK
fr0_pad[5]	WEST	1	CMOS	1	OK
fr0_pad[4]	WEST	1	CMOS	2	OK
fr0_pad[3]	WEST	1	CMOS	2	OK
fr0_pad[2]	WEST	1	CMOS	2	OK
fr0_pad[1]	WEST	1	CMOS	2	OK
fr0_pad[0]	WEST	1	CMOS	2	OK
ods_ids_pad[0]	WEST	1	CMOS	1	OK
ods_ids_pad[1]	WEST	1	CMOS	1	OK
ods_ids_pad[2]	WEST	1	CMOS	1	OK
ods_ids_pad[3]	WEST	1	CMOS	1	OK
edge_vdd[10]	WEST		POWER		

dr_pad	WEST	3	CMOS	1	OK
ideqod_pad[0]	WEST	1	CMOS	1	OK
ideqod_pad[1]	WEST	1	CMOS	2	OK
guard_pad	WEST	1	CMOS	2	OK
ods_sel_pad	WEST	1	CMOS	2	OK
pc_pad[25]	NORTH	3	CMOS	2	OK
pc_pad[22]	NORTH	3	CMOS	1	OK
edge_vdd[3]	NORTH		POWER		
pc_pad[24]	NORTH	3	CMOS	1	OK
pc_pad[23]	NORTH	3	CMOS	1	OK
pc_pad[21]	NORTH	3	CMOS	1	OK
WARNING: pc_pad[20]	NORTH	3	CMOS	0	EXCESSIVE NOISE LEVEL
pc_pad[19]	NORTH	3	CMOS	1	OK
pc_pad[18]	NORTH	3	CMOS	1	OK
pc_pad[17]	NORTH	3	CMOS	1	OK
pc_pad[16]	NORTH	3	CMOS	1	OK
pc_pad[15]	NORTH	3	CMOS	1	OK
edge_vdd[9]	NORTH		POWER		
pc_pad[14]	NORTH	3	CMOS	1	OK

This ring has 2 more VDD pads than it needs
 Ring under analysis: VSS

PAD NAME	EDGE	SPEED	DRIVE	PAD TYPE	SUPPLY	COMMENT

WARNING: pc_pad[13]	NORTH	3	CMOS	0		EXCESSIVE NOISE LEVEL
pc_pad[12]	NORTH	3	CMOS	1	OK	
pc_pad[11]	NORTH	3	CMOS	1	OK	
pc_pad[10]	NORTH	3	CMOS	1	OK	
edge_vss[10]	NORTH		POWER			
pc_pad[9]	NORTH	3	CMOS	1	OK	
pc_pad[8]	NORTH	3	CMOS	1	OK	
pc_pad[7]	NORTH	3	CMOS	1	OK	
WARNING: pc_pad[6]	NORTH	3	CMOS	0		EXCESSIVE NOISE LEVEL
WARNING: pc_pad[5]	NORTH	3	CMOS	0		EXCESSIVE NOISE LEVEL
pc_pad[4]	NORTH	3	CMOS	1	OK	
pc_pad[3]	NORTH	3	CMOS	1	OK	
pc_pad[1]	NORTH	3	CMOS	1	OK	
edge_vss[9]	NORTH		POWER			
pc_pad[2]	NORTH	3	CMOS	1	OK	
pc_pad[0]	NORTH	3	CMOS	1	OK	
inst5_pad[1]	NORTH	1	CMOS	1	OK	
ids_sel_pad	NORTH	1	CMOS	1	OK	
dev1_pads[0]	NORTH	1	CMOS	1	OK	
WARNING: dev1_pads[1]	NORTH	1	CMOS	0		EXCESSIVE NOISE LEVEL
WARNING: io_freeze_pad[1]	EAST	1	CMOS	0		EXCESSIVE NOISE LEVEL
WARNING: io_freeze_pad[0]	EAST	1	CMOS	0		EXCESSIVE NOISE LEVEL

```

WARNING: dev3_pads[2]    EAST    1    CMOS    0    EXCESSIVE NOISE LEVEL
WARNING: dev3_pads[1]    EAST    1    CMOS    0    EXCESSIVE NOISE LEVEL

dev3_pads[0]    EAST    1    CMOS    1    OK
dev2_pads[2]    EAST    1    CMOS    1    OK
dev2_pads[1]    EAST    1    CMOS    1    OK
dev2_pads[0]    EAST    1    CMOS    1    OK
dev1_pads[2]    EAST    1    CMOS    1    OK
ios_pad        EAST    1    CMOS    1    OK
inst4_pad[7]    EAST    1    CMOS    1    OK
inst4_pad[6]    EAST    1    CMOS    1    OK
inst5_pad[0]    EAST    1    CMOS    1    OK
inst4_pad[5]    EAST    1    CMOS    1    OK
edge_vss[8]     EAST          POWER
inst4_pad[4]    EAST    1    CMOS    1    OK
inst4_pad[3]    EAST    1    CMOS    1    OK
inst4_pad[2]    EAST    1    CMOS    1    OK
inst4_pad[1]    EAST    1    CMOS    2    OK
inst4_pad[0]    EAST    1    CMOS    2    OK
inst3_pad[6]    EAST    1    CMOS    2    OK
inst3_pad[7]    EAST    1    CMOS    2    OK
inst3_pad[5]    EAST    1    CMOS    2    OK
inst3_pad[4]    EAST    1    CMOS    2    OK
inst3_pad[3]    EAST    1    CMOS    2    OK
inst3_pad[2]    EAST    1    CMOS    1    OK
inst3_pad[1]    EAST    1    CMOS    1    OK
inst3_pad[0]    EAST    1    CMOS    1    OK
edge_vss[7]     EAST          POWER
inst2_pad[7]    EAST    1    CMOS    1    OK
inst2_pad[6]    EAST    1    CMOS    1    OK
inst2_pad[5]    EAST    1    CMOS    1    OK
inst2_pad[4]    EAST    1    CMOS    1    OK
inst2_pad[3]    EAST    1    CMOS    1    OK
inst2_pad[2]    EAST    1    CMOS    1    OK
inst2_pad[1]    EAST    1    CMOS    1    OK
inst2_pad[0]    EAST    1    CMOS    2    OK
inst1_pad[7]    EAST    1    CMOS    2    OK
inst1_pad[6]    EAST    1    CMOS    2    OK
inst1_pad[5]    EAST    1    CMOS    1    OK
inst1_pad[4]    EAST    1    CMOS    1    OK

inst1_pad[3]    SOUTH    1    CMOS    2    OK
inst1_pad[2]    SOUTH    1    CMOS    2    OK
inst1_pad[1]    SOUTH    1    CMOS    2    OK
inst1_pad[0]    SOUTH    1    CMOS    2    OK
inst0_pad[7]    SOUTH    1    CMOS    2    OK
edge_vss[0]     SOUTH          POWER
inst0_pad[6]    SOUTH    1    CMOS    2    OK
inst0_pad[5]    SOUTH    1    CMOS    2    OK
inst0_pad[4]    SOUTH    1    CMOS    2    OK
inst0_pad[3]    SOUTH    1    CMOS    2    OK
inst0_pad[2]    SOUTH    1    CMOS    2    OK
edge_vss[6]     SOUTH          POWER
inst0_pad[1]    SOUTH    1    CMOS    2    OK
inst0_pad[0]    SOUTH    1    CMOS    2    OK

```

boot_pad	SOUTH	1	CMOS	3	OK
csb_pad	SOUTH	1	CMOS	3	OK
csa_pad	SOUTH	1	CMOS	3	OK
dag_r_en_pad	SOUTH	1	CMOS	2	OK
inst_drv_pad	SOUTH	1	CMOS	2	OK
reset_out_pad	SOUTH	1	CMOS	2	OK
kernel_mode_pad	SOUTH	1	CMOS	2	OK
n_inst_wr_pad	SOUTH	1	CMOS	2	OK
freeze_pad	SOUTH	1	CMOS	1	OK
inst_rd_pad	SOUTH	1	CMOS	1	OK
edge_vss[5]	SOUTH		POWER		
valid_intr_pad	SOUTH	1	CMOS	1	OK
fr3_pad[7]	SOUTH	1	CMOS	1	OK
fr3_pad[6]	SOUTH	1	CMOS	1	OK
fr3_pad[5]	SOUTH	1	CMOS	1	OK
fr3_pad[4]	SOUTH	1	CMOS	1	OK
alu_op_pad[2]	SOUTH	1	CMOS	1	OK
fr3_pad[3]	SOUTH	1	CMOS	1	OK
fr3_pad[2]	SOUTH	1	CMOS	1	OK
inst5_pad[5]	SOUTH	1	CMOS	1	OK
inst5_pad[4]	SOUTH	1	CMOS	2	OK
alu_op_pad[5]	SOUTH	1	CMOS	1	OK
alu_op_pad[3]	SOUTH	1	CMOS	1	OK
alu_op_pad[4]	SOUTH	1	CMOS	1	OK
alu_op_pad[0]	SOUTH	1	CMOS	1	OK
alu_op_pad[1]	SOUTH	1	CMOS	1	OK
fr3_pad[1]	SOUTH	1	CMOS	1	OK
fr3_pad[0]	WEST	1	CMOS	1	OK
alu_op_pad[6]	WEST	1	CMOS	1	OK
fr2_pad[7]	WEST	1	CMOS	1	OK
edge_vss[4]	WEST		POWER		
alu_op_pad[7]	WEST	1	CMOS	1	OK
fr2_pad[6]	WEST	1	CMOS	1	OK
inst5_pad[2]	WEST	1	CMOS	1	OK
fr2_pad[5]	WEST	1	CMOS	1	OK
fr2_pad[4]	WEST	1	CMOS	1	OK
inst5_pad[3]	WEST	1	CMOS	1	OK
fr2_pad[2]	WEST	1	CMOS	2	OK
fr1_pad[7]	WEST	1	CMOS	2	OK
fr2_pad[3]	WEST	1	CMOS	2	OK
fr2_pad[1]	WEST	1	CMOS	2	OK
fr2_pad[0]	WEST	1	CMOS	1	OK
fr1_pad[6]	WEST	1	CMOS	1	OK
flush_pad	WEST	1	CMOS	1	OK
fr1_pad[5]	WEST	1	CMOS	1	OK
fr1_pad[4]	WEST	1	CMOS	1	OK
fr1_pad[3]	WEST	1	CMOS	1	OK
edge_vss[3]	WEST		POWER		
fr1_pad[2]	WEST	1	CMOS	1	OK
fr1_pad[0]	WEST	1	CMOS	1	OK
fr1_pad[1]	WEST	1	CMOS	1	OK
fr0_pad[7]	WEST	1	CMOS	2	OK
fr0_pad[6]	WEST	1	CMOS	2	OK

fr0_pad[5]	WEST	1	CMOS	2	OK
fr0_pad[4]	WEST	1	CMOS	2	OK
fr0_pad[3]	WEST	1	CMOS	2	OK
fr0_pad[2]	WEST	1	CMOS	2	OK
fr0_pad[1]	WEST	1	CMOS	2	OK
fr0_pad[0]	WEST	1	CMOS	1	OK
ods_ids_pad[0]	WEST	1	CMOS	1	OK
edge_vss[2]	WEST		POWER		
ods_ids_pad[1]	WEST	1	CMOS	1	OK
ods_ids_pad[2]	WEST	1	CMOS	1	OK
ods_ids_pad[3]	WEST	1	CMOS	1	OK
dr_pad	WEST	3	CMOS	1	OK
ideqod_pad[0]	WEST	1	CMOS	2	OK
ideqod_pad[1]	WEST	1	CMOS	2	OK
guard_pad	WEST	1	CMOS	2	OK
ods_sel_pad	WEST	1	CMOS	2	OK
corner_vss[0]	WEST		POWER		
pc_pad[25]	NORTH	3	CMOS	1	OK
pc_pad[22]	NORTH	3	CMOS	1	OK
pc_pad[24]	NORTH	3	CMOS	1	OK
pc_pad[23]	NORTH	3	CMOS	2	OK
pc_pad[21]	NORTH	3	CMOS	1	OK
pc_pad[20]	NORTH	3	CMOS	1	OK
edge_vss[1]	NORTH		POWER		
pc_pad[19]	NORTH	3	CMOS	1	OK
pc_pad[18]	NORTH	3	CMOS	1	OK
pc_pad[17]	NORTH	3	CMOS	1	OK

WARNING: pc_pad[16] NORTH 3 CMOS 0 EXCESSIVE NOISE LEVEL

WARNING: pc_pad[15] NORTH 3 CMOS 0 EXCESSIVE NOISE LEVEL

WARNING: pc_pad[14] NORTH 3 CMOS 0 EXCESSIVE NOISE LEVEL

This ring has 1 more VSS pad than it needs

Noise Level can be reduced by adding more ring power pads
or using slower speed output pads.

10. Power Dissipation

```
) Total power consumption (5.5V, 0 DegC 50pf/out_pad):
)   DC:          114.84mW [114.84(core)+0.00(ring)]
)   AC@10MHz:   1089.71mW [413.59(core)+676.12(ring)]
```

11. Simulation Setup Files

11.1. designinit.080

```
func designinit {
    toggle /Clk 0 ' (0 5 10)
    tag /Clk step both
```

```
tag /Clk cycle falling
}
```

12. Timing Setup Files

12.1. basic.040

```
LABEL Input constraints from other chips
HOLDTIME_MARGIN 2.00
SELECT_EXT_CLOCK Clk
INPUT DAG_error 1 0 19.80 0.00 0.00 0.00
INPUT ALU_Flag 1 0 21.50 0.00 0.00 0.00
INPUT Carry 1 0 21.50 0.00 0.00 0.00
INPUT R_eq_f_1 1 0 58.30 0.00 8.30 0.00
INPUT R_eq_f_2 1 0 58.30 0.00 8.30 0.00
INPUT S_eq_f_1 1 0 57.90 0.00 7.90 0.00
INPUT S_eq_f_2 1 0 57.90 0.00 7.90 0.00
INPUT R_eq_f_1 0 1 8.30 0.00 0.00 0.00
INPUT R_eq_f_2 0 1 8.30 0.00 0.00 0.00
INPUT S_eq_f_1 0 1 7.90 0.00 0.00 0.00
INPUT S_eq_f_2 0 1 7.90 0.00 0.00 0.00
INPUT Sign 1 0 21.50 0.00 0.00 0.00
INPUT Zero 1 0 21.50 0.00 0.00 0.00
INPUT RF[0] 1 0 40.50 0.00 0.00 0.00
INPUT RF[1] 1 0 40.50 0.00 0.00 0.00
INPUT RF[2] 1 0 40.50 0.00 0.00 0.00
INPUT RF[3] 1 0 40.50 0.00 0.00 0.00
INPUT RF[4] 1 0 40.50 0.00 0.00 0.00
INPUT RF[5] 1 0 40.50 0.00 0.00 0.00
INPUT RF[6] 1 0 40.50 0.00 0.00 0.00
INPUT RF[7] 1 0 40.50 0.00 0.00 0.00
INPUT RF[8] 1 0 40.50 0.00 0.00 0.00
INPUT RF[9] 1 0 40.50 0.00 0.00 0.00
INPUT RF[10] 1 0 40.50 0.00 0.00 0.00
INPUT RF[11] 1 0 40.50 0.00 0.00 0.00
INPUT RF[12] 1 0 40.50 0.00 0.00 0.00
INPUT RF[13] 1 0 40.50 0.00 0.00 0.00
INPUT RF[14] 1 0 40.50 0.00 0.00 0.00
INPUT RF[15] 1 0 40.50 0.00 0.00 0.00
INPUT RF[16] 1 0 40.50 0.00 0.00 0.00
INPUT RF[17] 1 0 40.50 0.00 0.00 0.00
INPUT RF[18] 1 0 40.50 0.00 0.00 0.00
INPUT RF[19] 1 0 40.50 0.00 0.00 0.00
INPUT RF[20] 1 0 40.50 0.00 0.00 0.00
INPUT RF[21] 1 0 40.50 0.00 0.00 0.00
INPUT RF[22] 1 0 40.50 0.00 0.00 0.00
INPUT RF[23] 1 0 40.50 0.00 0.00 0.00
INPUT RF[24] 1 0 40.50 0.00 0.00 0.00
INPUT RF[25] 1 0 40.50 0.00 0.00 0.00
INPUT RF[26] 1 0 40.50 0.00 0.00 0.00
INPUT RF[27] 1 0 40.50 0.00 0.00 0.00
INPUT RF[28] 1 0 40.50 0.00 0.00 0.00
```

```
INPUT RF[29] 1 0 40.50 0.00 0.00 0.00
INPUT RF[30] 1 0 40.50 0.00 0.00 0.00
INPUT RF[31] 1 0 40.50 0.00 0.00 0.00
INPUT RF[0] 0 1 43.60 0.00 0.00 0.00
INPUT RF[1] 0 1 43.60 0.00 0.00 0.00
INPUT RF[2] 0 1 43.60 0.00 0.00 0.00
INPUT RF[3] 0 1 43.60 0.00 0.00 0.00
INPUT RF[4] 0 1 43.60 0.00 0.00 0.00
INPUT RF[5] 0 1 43.60 0.00 0.00 0.00
INPUT RF[6] 0 1 43.60 0.00 0.00 0.00
INPUT RF[7] 0 1 43.60 0.00 0.00 0.00
INPUT RF[8] 0 1 43.60 0.00 0.00 0.00
INPUT RF[9] 0 1 43.60 0.00 0.00 0.00
INPUT RF[10] 0 1 43.60 0.00 0.00 0.00
INPUT RF[11] 0 1 43.60 0.00 0.00 0.00
INPUT RF[12] 0 1 43.60 0.00 0.00 0.00
INPUT RF[13] 0 1 43.60 0.00 0.00 0.00
INPUT RF[14] 0 1 43.60 0.00 0.00 0.00
INPUT RF[15] 0 1 43.60 0.00 0.00 0.00
INPUT RF[16] 0 1 43.60 0.00 0.00 0.00
INPUT RF[17] 0 1 43.60 0.00 0.00 0.00
INPUT RF[18] 0 1 43.60 0.00 0.00 0.00
INPUT RF[19] 0 1 43.60 0.00 0.00 0.00
INPUT RF[20] 0 1 43.60 0.00 0.00 0.00
INPUT RF[21] 0 1 43.60 0.00 0.00 0.00
INPUT RF[22] 0 1 43.60 0.00 0.00 0.00
INPUT RF[23] 0 1 43.60 0.00 0.00 0.00
INPUT RF[24] 0 1 43.60 0.00 0.00 0.00
INPUT RF[25] 0 1 43.60 0.00 0.00 0.00
INPUT RF[26] 0 1 43.60 0.00 0.00 0.00
INPUT RF[27] 0 1 43.60 0.00 0.00 0.00
INPUT RF[28] 0 1 43.60 0.00 0.00 0.00
INPUT RF[29] 0 1 43.60 0.00 0.00 0.00
INPUT RF[30] 0 1 43.60 0.00 0.00 0.00
INPUT RF[31] 0 1 43.60 0.00 0.00 0.00
IGNORE_PATH fr0_pad[0]/rout fr0_pad[0]/rf
IGNORE_PATH fr0_pad[1]/rout fr0_pad[1]/rf
IGNORE_PATH fr0_pad[2]/rout fr0_pad[2]/rf
IGNORE_PATH fr0_pad[3]/rout fr0_pad[3]/rf
IGNORE_PATH fr0_pad[4]/rout fr0_pad[4]/rf
IGNORE_PATH fr0_pad[5]/rout fr0_pad[5]/rf
IGNORE_PATH fr0_pad[6]/rout fr0_pad[6]/rf
IGNORE_PATH fr0_pad[7]/rout fr0_pad[7]/rf
IGNORE_PATH fr1_pad[0]/rout fr1_pad[0]/rf
IGNORE_PATH fr1_pad[1]/rout fr1_pad[1]/rf
IGNORE_PATH fr1_pad[2]/rout fr1_pad[2]/rf
IGNORE_PATH fr1_pad[3]/rout fr1_pad[3]/rf
IGNORE_PATH fr1_pad[4]/rout fr1_pad[4]/rf
IGNORE_PATH fr1_pad[5]/rout fr1_pad[5]/rf
IGNORE_PATH fr1_pad[6]/rout fr1_pad[6]/rf
IGNORE_PATH fr1_pad[7]/rout fr1_pad[7]/rf
IGNORE_PATH fr2_pad[0]/rout fr2_pad[0]/rf
IGNORE_PATH fr2_pad[1]/rout fr2_pad[1]/rf
IGNORE_PATH fr2_pad[2]/rout fr2_pad[2]/rf
```

```
IGNORE_PATH fr2_pad[3]/rout fr2_pad[3]/rf
IGNORE_PATH fr2_pad[4]/rout fr2_pad[4]/rf
IGNORE_PATH fr2_pad[5]/rout fr2_pad[5]/rf
IGNORE_PATH fr2_pad[6]/rout fr2_pad[6]/rf
IGNORE_PATH fr2_pad[7]/rout fr2_pad[7]/rf
IGNORE_PATH fr3_pad[0]/rout fr3_pad[0]/rf
IGNORE_PATH fr3_pad[1]/rout fr3_pad[1]/rf
IGNORE_PATH fr3_pad[2]/rout fr3_pad[2]/rf
IGNORE_PATH fr0_pad[0]/r_out_dis fr0_pad[0]/rf
IGNORE_PATH fr0_pad[1]/r_out_dis fr0_pad[1]/rf
IGNORE_PATH fr0_pad[2]/r_out_dis fr0_pad[2]/rf
IGNORE_PATH fr0_pad[3]/r_out_dis fr0_pad[3]/rf
IGNORE_PATH fr0_pad[4]/r_out_dis fr0_pad[4]/rf
IGNORE_PATH fr0_pad[5]/r_out_dis fr0_pad[5]/rf
IGNORE_PATH fr0_pad[6]/r_out_dis fr0_pad[6]/rf
IGNORE_PATH fr0_pad[7]/r_out_dis fr0_pad[7]/rf
IGNORE_PATH fr1_pad[0]/r_out_dis fr1_pad[0]/rf
IGNORE_PATH fr1_pad[1]/r_out_dis fr1_pad[1]/rf
IGNORE_PATH fr1_pad[2]/r_out_dis fr1_pad[2]/rf
IGNORE_PATH fr1_pad[3]/r_out_dis fr1_pad[3]/rf
IGNORE_PATH fr1_pad[4]/r_out_dis fr1_pad[4]/rf
IGNORE_PATH fr1_pad[5]/r_out_dis fr1_pad[5]/rf
IGNORE_PATH fr1_pad[6]/r_out_dis fr1_pad[6]/rf
IGNORE_PATH fr1_pad[7]/r_out_dis fr1_pad[7]/rf
IGNORE_PATH fr2_pad[0]/r_out_dis fr2_pad[0]/rf
IGNORE_PATH fr2_pad[1]/r_out_dis fr2_pad[1]/rf
IGNORE_PATH fr2_pad[2]/r_out_dis fr2_pad[2]/rf
IGNORE_PATH fr2_pad[3]/r_out_dis fr2_pad[3]/rf
IGNORE_PATH fr2_pad[4]/r_out_dis fr2_pad[4]/rf
IGNORE_PATH fr2_pad[5]/r_out_dis fr2_pad[5]/rf
IGNORE_PATH fr2_pad[6]/r_out_dis fr2_pad[6]/rf
IGNORE_PATH fr2_pad[7]/r_out_dis fr2_pad[7]/rf
IGNORE_PATH fr3_pad[0]/r_out_dis fr3_pad[0]/rf
IGNORE_PATH fr3_pad[1]/r_out_dis fr3_pad[1]/rf
IGNORE_PATH fr3_pad[2]/r_out_dis fr3_pad[2]/rf
IGNORE_PATH inst0_pad[0]/inst_dout inst0_pad[0]/inst
IGNORE_PATH inst0_pad[1]/inst_dout inst0_pad[1]/inst
IGNORE_PATH inst0_pad[2]/inst_dout inst0_pad[2]/inst
IGNORE_PATH inst0_pad[3]/inst_dout inst0_pad[3]/inst
IGNORE_PATH inst0_pad[4]/inst_dout inst0_pad[4]/inst
IGNORE_PATH inst0_pad[5]/inst_dout inst0_pad[5]/inst
IGNORE_PATH inst0_pad[6]/inst_dout inst0_pad[6]/inst
IGNORE_PATH inst0_pad[7]/inst_dout inst0_pad[7]/inst
IGNORE_PATH inst1_pad[0]/inst_dout inst1_pad[0]/inst
IGNORE_PATH inst1_pad[1]/inst_dout inst1_pad[1]/inst
IGNORE_PATH inst1_pad[2]/inst_dout inst1_pad[2]/inst
IGNORE_PATH inst1_pad[3]/inst_dout inst1_pad[3]/inst
IGNORE_PATH inst1_pad[4]/inst_dout inst1_pad[4]/inst
IGNORE_PATH inst1_pad[5]/inst_dout inst1_pad[5]/inst
IGNORE_PATH inst1_pad[6]/inst_dout inst1_pad[6]/inst
IGNORE_PATH inst1_pad[7]/inst_dout inst1_pad[7]/inst
IGNORE_PATH inst2_pad[0]/inst_dout inst2_pad[0]/inst
IGNORE_PATH inst2_pad[1]/inst_dout inst2_pad[1]/inst
IGNORE_PATH inst2_pad[2]/inst_dout inst2_pad[2]/inst
```

```
IGNORE_PATH inst2_pad[3]/inst_dout inst2_pad[3]/inst
IGNORE_PATH inst2_pad[4]/inst_dout inst2_pad[4]/inst
IGNORE_PATH inst2_pad[5]/inst_dout inst2_pad[5]/inst
IGNORE_PATH inst2_pad[6]/inst_dout inst2_pad[6]/inst
IGNORE_PATH inst2_pad[7]/inst_dout inst2_pad[7]/inst
IGNORE_PATH inst3_pad[0]/inst_dout inst3_pad[0]/inst
IGNORE_PATH inst3_pad[1]/inst_dout inst3_pad[1]/inst
IGNORE_PATH inst3_pad[2]/inst_dout inst3_pad[2]/inst
IGNORE_PATH inst3_pad[3]/inst_dout inst3_pad[3]/inst
IGNORE_PATH inst3_pad[4]/inst_dout inst3_pad[4]/inst
IGNORE_PATH inst3_pad[5]/inst_dout inst3_pad[5]/inst
IGNORE_PATH inst3_pad[6]/inst_dout inst3_pad[6]/inst
IGNORE_PATH inst3_pad[7]/inst_dout inst3_pad[7]/inst
IGNORE_PATH inst4_pad[0]/inst_dout inst4_pad[0]/inst
IGNORE_PATH inst4_pad[1]/inst_dout inst4_pad[1]/inst
IGNORE_PATH inst4_pad[2]/inst_dout inst4_pad[2]/inst
IGNORE_PATH inst4_pad[3]/inst_dout inst4_pad[3]/inst
IGNORE_PATH inst4_pad[4]/inst_dout inst4_pad[4]/inst
IGNORE_PATH inst4_pad[5]/inst_dout inst4_pad[5]/inst
IGNORE_PATH inst4_pad[6]/inst_dout inst4_pad[6]/inst
IGNORE_PATH inst4_pad[7]/inst_dout inst4_pad[7]/inst
IGNORE_PATH inst5_pad[0]/inst_dout inst5_pad[0]/inst
IGNORE_PATH inst5_pad[1]/inst_dout inst5_pad[1]/inst
IGNORE_PATH inst5_pad[2]/inst_dout inst5_pad[2]/inst
IGNORE_PATH inst5_pad[3]/inst_dout inst5_pad[3]/inst
IGNORE_PATH inst5_pad[4]/inst_dout inst5_pad[4]/inst
IGNORE_PATH inst5_pad[5]/inst_dout inst5_pad[5]/inst
IGNORE_PATH dr_pad/dr_out_dis dr_pad/dr
IGNORE_PATH fr0_pad[0]/rf pc_gen_mod/bpp_dp/f_r_1[0]
IGNORE_PATH fr0_pad[1]/rf pc_gen_mod/bpp_dp/f_r_1[1]
IGNORE_PATH fr0_pad[2]/rf pc_gen_mod/bpp_dp/f_r_1[2]
IGNORE_PATH fr0_pad[3]/rf pc_gen_mod/bpp_dp/f_r_1[3]
IGNORE_PATH fr0_pad[4]/rf pc_gen_mod/bpp_dp/f_r_1[4]
IGNORE_PATH fr0_pad[5]/rf pc_gen_mod/bpp_dp/f_r_1[5]
IGNORE_PATH fr0_pad[6]/rf pc_gen_mod/bpp_dp/f_r_1[6]
IGNORE_PATH fr0_pad[7]/rf pc_gen_mod/bpp_dp/f_r_1[7]
IGNORE_PATH fr1_pad[0]/rf pc_gen_mod/bpp_dp/f_r_1[8]
IGNORE_PATH fr1_pad[1]/rf pc_gen_mod/bpp_dp/f_r_1[9]
IGNORE_PATH fr1_pad[2]/rf pc_gen_mod/bpp_dp/f_r_1[10]
IGNORE_PATH fr1_pad[3]/rf pc_gen_mod/bpp_dp/f_r_1[11]
IGNORE_PATH fr1_pad[4]/rf pc_gen_mod/bpp_dp/f_r_1[12]
IGNORE_PATH fr1_pad[5]/rf pc_gen_mod/bpp_dp/f_r_1[13]
IGNORE_PATH fr1_pad[6]/rf pc_gen_mod/bpp_dp/f_r_1[14]
IGNORE_PATH fr1_pad[7]/rf pc_gen_mod/bpp_dp/f_r_1[15]
IGNORE_PATH fr2_pad[0]/rf pc_gen_mod/bpp_dp/f_r_1[16]
IGNORE_PATH fr2_pad[1]/rf pc_gen_mod/bpp_dp/f_r_1[17]
IGNORE_PATH fr2_pad[2]/rf pc_gen_mod/bpp_dp/f_r_1[18]
IGNORE_PATH fr2_pad[3]/rf pc_gen_mod/bpp_dp/f_r_1[19]
IGNORE_PATH fr2_pad[4]/rf pc_gen_mod/bpp_dp/f_r_1[20]
IGNORE_PATH fr2_pad[5]/rf pc_gen_mod/bpp_dp/f_r_1[21]
IGNORE_PATH fr2_pad[6]/rf pc_gen_mod/bpp_dp/f_r_1[22]
IGNORE_PATH fr2_pad[7]/rf pc_gen_mod/bpp_dp/f_r_1[23]
IGNORE_PATH fr3_pad[0]/rf pc_gen_mod/bpp_dp/f_r_1[24]
IGNORE_PATH fr3_pad[1]/rf pc_gen_mod/bpp_dp/f_r_1[25]
```

12.2. baseline.040

LABEL 75 deg C, 5.0 Volts

TEMP_VOLT 75 5.00

12.3. room.040

LABEL 67 deg C, 5.0 Volts

TEMP_VOLT 67 5.00

12.4. worst.040

LABEL 117 deg C, 4.5 Volts

TEMP_VOLT 117 4.50

13. Timing Reports**13.1. TYPICAL, 75 deg C, 5.0 V**

Genesil Version v8.0.2 -- Mon Feb 4 10:42:49 1991

Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/iag

Timing Analyzer

CLOCK REPORT MODE

Fabline: HP2_CN10B

Corner: TYPICAL

Junction Temperature: 75 deg C

Voltage: 5.00v

External Clock: Clk

Included setup files:

#0 basic

(Input constraints from other chip>

#1 baseline

(75 deg C, 5.0 Volts)

CLOCK TIMES (minimum)

Phase 1 High: 42.6 ns

Phase 2 High: 46.3 ns

Cycle (from Ph1): 87.4 ns

Cycle (from Ph2): 90.8 ns

Minimum Cycle Time: 90.8 ns

Symmetric Cycle Time: 92.6 ns

CLOCK WORST CASE PATHS

Minimum Phase 1 high time is 42.6 ns set by:

** Clock delay: 1.6ns (44.2-42.6)

Node	Cumulative Delay	Transition
io_mod/sell/(internal)	44.2	rise
io_mod/sell/ods_eq_1_before	43.3	fall
io_mod/sell/n_ods_en1	41.9	rise
io_mod/sell/ods_en1	40.8	fall
io_mod/ds_ctrl/ods_en1	40.8	fall
io_mod/ds_ctrl/ods_en1'	36.3	fall

io_mod/ds_ctrl/flush	36.0	rise
io_mod/ids_sel/flush	36.0	rise
io_mod/ids_sel/flush'	35.2	rise
io_mod/ids_sel/flush_in	34.6	rise
<_gen_mod/flush_ctrl/flush_out	34.6	rise
<gen_mod/flush_ctrl/flush_out'	29.5	rise
<mod/flush_ctrl/GB.LP.NNZ5fN11	29.3	fall
<mod/flush_ctrl/GB.LP.NNZ5fN21	28.2	rise
<mod/flush_ctrl/GB.LP.NNZ5fN22	27.7	fall
<_mod/flush_ctrl/GB.LP.NNZ5fN2	27.0	rise
<_mod/flush_ctrl/GB.LP.NNZ5fN6	26.1	fall
<LP.NNalustatZ2eoutZ5fxZ5bZ2Z5d	25.6	rise
pc_gen_mod/flush_ctrl/sign	24.5	rise
sign_pad/sign	24.5	rise
sign_pad/sign'	23.6	rise
Sign	21.5	rise

Minimum Phase 2 high time is 46.3 ns set by:

** Clock delay: 2.1ns (48.4-46.3)

Node	Cumulative Delay	Transition
<_din_mod/rf_din_dp/(internal)	48.4	fall
rf_din_mod/rf_din_dp/rf[1]	47.6	rise
fr0_pad[1]/rf	47.6	rise
fr0_pad[1]/rf'	45.6	rise
RF[1]	43.6	rise

Minimum cycle time (from Ph1) is 87.4 ns set by:

** Clock delay: 2.1ns (89.4-87.4)

Node	Cumulative Delay	Transition
<atus_mod/status_dp/(internal)	89.4	fall
status_mod/status_dp/371	88.9	fall
<_mod/status_dp/INTER3_ST1[19]	88.6	rise
<mod/status_dp/intr_status[19]	87.5	rise
</priority_pla/req_intr_adr[2]	87.5	rise
<priority_pla/req_intr_adr[2]'	80.9	rise
<d/priority_pla/GB.LP.NNZ5fN13	80.6	fall
<d/priority_pla/GB.LP.NNZ5fN11	80.3	rise
<d/priority_pla/GB.LP.NNZ5fN41	80.1	fall
<d/priority_pla/GB.LP.NNZ5fN30	79.5	rise
<d/priority_pla/GB.LP.NNZ5fN32	78.5	rise
<d/priority_pla/GB.LP.NNZ5fN25	77.5	fall
<priority_pla/current_intr[14]	77.3	rise
<_mod/intr_dp/current_intr[14]	77.3	rise
<mod/intr_dp/current_intr[14]'	77.2	rise
<_mod/intr_dp/phb_lat_VAL1[14]	76.5	rise
*intr_mod/intr_dp/(internal)	75.4	fall
intr_mod/intr_dp/guarded_ei	71.6	fall
intr_mod/ld_ctrl/guarded_ei	71.6	fall
intr_mod/ld_ctrl/guarded_ei'	70.9	fall
intr_mod/ld_ctrl/n_guard	69.8	fall
io_mod/ids_sel/n_guard_out	69.8	fall
io_mod/ids_sel/n_guard_out'	67.2	fall
io_mod/ids_sel/n_guard	66.6	fall

io_mod/freeze_ctrl/n_guard	66.6	fall
io_mod/freeze_ctrl/n_guard'	66.3	fall
<od/freeze_ctrl/GB.LP.NNZ5fN14	66.1	rise
<od/freeze_ctrl/GB.LP.NNZ5fN34	65.1	fall
<od/freeze_ctrl/GB.LP.NNZ5fN36	64.7	rise
<od/freeze_ctrl/GB.LP.NNZ5fN31	63.9	fall
io_mod/freeze_ctrl/r_eq_f_1	63.7	rise
reqfl_pad/r_eq_f_1	63.6	rise
reqfl_pad/r_eq_f_1'	60.4	rise
R_eq_f_1	58.3	rise

Minimum cycle time (from Ph2) is 90.8 ns set by:

 ** Clock delay: 4.2ns (95.0-90.8)

Node	Cumulative Delay	Transition
<_gen_mod/stk_pc_dp/(internal)	95.0	fall
<gen_mod/stk_pc_dp/next_pc[24]	94.8	rise
<_ndp_mod/next_pc_buff/OUT[24]	94.8	rise
<ndp_mod/next_pc_buff/OUT[24]'	90.5	rise
<c_ndp_mod/next_pc_buff/IN[24]	89.8	rise
<ndp_mod/next_pc_adder/OUT[24]	89.8	rise
<dp_mod/next_pc_adder/OUT[24]'	89.7	rise
<ndp_mod/next_pc_adder/IN1[16]	81.8	fall
<od/pc_ndp_mod/pc_buff/OUT[16]	81.8	fall
<d/pc_ndp_mod/pc_buff/OUT[16]'	78.8	fall
<mod/pc_ndp_mod/pc_buff/IN[16]	78.2	fall
<d/pc_ndp_mod/pc_latch/OUT[16]	78.2	fall
</pc_ndp_mod/pc_latch/OUT[16]'	78.0	fall
<od/pc_ndp_mod/pc_latch/IN[16]	76.7	fall
<d/pc_ndp_mod/pc_unlat/OUT[16]	76.7	fall
</pc_ndp_mod/pc_unlat/OUT[16]'	76.6	fall
<od/pc_ndp_mod/pc_unlat/IN[16]	76.4	rise
<pc_ndp_mod/n_pc_unlat/OUT[16]	76.4	rise
<c_ndp_mod/n_pc_unlat/OUT[16]'	76.3	rise
<pc_ndp_mod/n_pc_unlat/IN1[16]	75.9	fall
<_mod/pc_ndp_mod/ready/OUT[16]	75.9	fall
<mod/pc_ndp_mod/ready/OUT[16]'	75.8	fall
<n_mod/pc_ndp_mod/ready/IN[16]	75.6	rise
<od/pc_ndp_mod/n_ready/OUT[16]	75.6	rise
<d/pc_ndp_mod/n_ready/OUT[16]'	75.4	rise
<od/pc_ndp_mod/n_ready/IN1[16]	75.0	fall
<_mod/pc_ndp_mod/alpha/OUT[16]	75.0	fall
<mod/pc_ndp_mod/alpha/OUT[16]'	75.0	fall
<n_mod/pc_ndp_mod/alpha/IN[16]	74.7	rise
<od/pc_ndp_mod/n_alpha/OUT[16]	74.7	rise
<d/pc_ndp_mod/n_alpha/OUT[16]'	74.6	rise
<od/pc_ndp_mod/n_alpha/IN1[16]	74.2	fall
<mod/pc_ndp_mod/br_adr/OUT[16]	74.2	fall
<od/pc_ndp_mod/br_adr/OUT[16]'	71.2	fall
<_mod/pc_ndp_mod/br_adr/IN[16]	71.0	rise
<d/pc_ndp_mod/n_br_adr/OUT[16]	71.0	rise
</pc_ndp_mod/n_br_adr/OUT[16]'	70.9	rise
<d/pc_ndp_mod/n_br_adr/IN2[16]	70.5	fall
<d/pc_ndp_mod/absolute/OUT[16]	70.5	fall

</pc_ndp_mod/absolute/OUT[16]'	70.2	fall
<od/pc_ndp_mod/absolute/IN[16]	70.0	rise
<pc_ndp_mod/n_absolute/OUT[16]	70.0	rise
<c_ndp_mod/n_absolute/OUT[16]'	69.8	rise
<pc_ndp_mod/n_absolute/IN2[16]	69.4	fall
intr_mod/ram/intr_vect[16]	69.4	fall
intr_mod/ram/intr_vect[16]'	69.2	fall
intr_mod/ram/st_vect_adr[2]	63.7	rise
<intr_vect_ctrl/st_vect_adr[2]	63.7	rise
<ntr_vect_ctrl/st_vect_adr[2]'	60.8	rise
</intr_vect_ctrl/GB.LP.NNZ5fN2	60.5	fall
<tr_vect_ctrl/valid_intr_pulse	60.1	rise
<r_mod/valid_intr_ctrl/vip_out	60.1	rise
<_mod/valid_intr_ctrl/vip_out'	55.5	rise
<alid_intr_ctrl/GB.LP.NNZ5fN21	55.3	fall
<alid_intr_ctrl/GB.LP.NNZ5fN11	54.3	rise
<valid_intr_ctrl/GB.LP.NNZ5fN7	53.7	fall
<valid_intr_ctrl/GB.LP.NNZ5fN0	53.4	rise
<valid_intr_ctrl/GB.LP.NNZ5fN6	52.6	fall
<valid_intr_ctrl/GB.LP.NNZ5fN3	52.3	rise
<alid_intr_ctrl/GB.LP.NNZ5fN10	51.1	rise
<P.NNnpassint22eout25fx25b025d	50.1	fall
*</valid_intr_ctrl/n_pass_intr	48.4	fall
<_mod/pass_intr_dp/n_pass_intr	48.4	fall
<mod/pass_intr_dp/n_pass_intr'	48.2	fall
</pass_intr_dp/req_intr_adr[0]	43.8	rise
</priority_pla/req_intr_adr[0]	43.8	rise
<priority_pla/req_intr_adr[0]'	37.3	rise
<od/priority_pla/GB.LP.NNZ5fN1	37.2	fall
<d/priority_pla/GB.LP.NNZ5fN36	36.8	rise
<d/priority_pla/GB.LP.NNZ5fN47	36.1	fall
<d/priority_pla/GB.LP.NNZ5fN51	35.9	rise
<d/priority_pla/GB.LP.NNZ5fN40	35.1	fall
<d/priority_pla/GB.LP.NNZ5fN12	34.7	rise
<d/priority_pla/GB.LP.NNZ5fN14	33.4	rise
</priority_pla/current_intr[4]	31.6	fall
<r_mod/intr_dp/current_intr[4]	31.6	fall
<_mod/intr_dp/current_intr[4]'	31.5	fall
<r_mod/intr_dp/phb_lat_VAL1[4]	30.7	fall
intr_mod/intr_dp/guarded_ei	26.1	rise
intr_mod/ld_ctrl/guarded_ei	26.1	rise
intr_mod/ld_ctrl/guarded_ei'	25.2	rise
intr_mod/ld_ctrl/n_guard	24.5	rise
io_mod/ids_sel/n_guard_out	24.5	rise
io_mod/ids_sel/n_guard_out'	21.7	rise
io_mod/ids_sel/n_guard	21.1	rise
io_mod/freeze_ctrl/n_guard	21.1	rise
io_mod/freeze_ctrl/n_guard'	20.5	rise
<od/freeze_ctrl/GB.LP.NNZ5fN14	20.3	fall
<od/freeze_ctrl/GB.LP.NNZ5fN34	19.9	rise
<mod/freeze_ctrl/GB.LP.NNZ5fN2	19.4	fall
<mod/freeze_ctrl/GB.LP.NNZ5fN6	19.1	rise
<mod/freeze_ctrl/GB.LP.NNZ5fN9	18.2	rise
io_mod/freeze_ctrl/ids_freeze	17.4	fall

io_mod/test_ctrl/ids_freeze	17.4	fall
io_mod/test_ctrl/ids_freeze'	16.6	fall
io_mod/test_ctrl/ids_fr_lat	15.9	fall
io_mod/test_ctrl/ids_freeze_in	14.4	fall
io_mod/ds_ctrl/ids_freeze_in	14.4	fall
io_mod/ds_ctrl/ids_freeze_in'	14.4	fall
io_mod/ds_ctrl/async_ids_fr	13.4	fall
<d/async_ids_ctrl/async_ids_fr	13.4	fall
</async_ids_ctrl/async_ids_fr'	13.2	fall
<async_ids_ctrl/GB.LP.NNZ5fN27	13.0	rise
<async_ids_ctrl/GB.LP.NNZ5fN15	11.8	fall
<async_ids_ctrl/GB.LP.NNZ5fN18	11.5	rise
<async_ids_ctrl/GB.LP.NNZ5fN28	10.8	fall
</async_ids_ctrl/GB.LP.NNZ5fN6	9.8	rise
<async_ids_ctrl/GB.LP.NNZ5fN12	9.3	fall
io_mod/async_ids_ctrl/ids_sel	9.0	rise
io_mod/ids_sel/ids_sel	9.0	rise
io_mod/ids_sel/ids_sel'	7.3	rise
io_mod/ids_sel/ids_sel_buf	6.7	rise
io_mod/ids_sel/ids_sel_buf'	6.6	rise
io_mod/ids_sel/ids_ph_in	5.4	rise
io_mod/ids_sel/ids_ph_out	5.4	rise
io_mod/ids_sel/ids_ph_out'	5.3	rise
io_mod/ids_sel/PHASE_B	4.2	rise
clk_pad/PHASE_B	4.2	rise
Clk	0.0	fall

Genesil Version v8.0.2 -- Mon Feb 4 10:43:23 1991

Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/iag

Timing Analyzer

OUTPUT DELAY MODE

Fabline: HP2_CN10B

Corner: TYPICAL

Junction Temperature: 75 deg C

Voltage: 5.00v

External Clock: Clk

Included setup files:

#0 basic (Input constraints from other chip)
 #1 baseline (75 deg C, 5.0 Volts)

OUTPUT DELAYS (ns)

Output	Ph1(r) Delay		Ph2(r) Delay		Loading(pf)	
	Min	Max	Min	Max		
ALU_opcode[0]	13.0	14.6	---	---	50.00	PATH
ALU_opcode[1]	13.0	14.6	---	---	50.00	PATH
ALU_opcode[2]	12.8	14.5	---	---	50.00	PATH
ALU_opcode[3]	12.8	14.4	---	---	50.00	PATH
ALU_opcode[4]	12.8	14.5	---	---	50.00	PATH
ALU_opcode[5]	12.8	14.4	---	---	50.00	PATH
ALU_opcode[6]	12.8	14.5	---	---	50.00	PATH
ALU_opcode[7]	12.8	14.5	---	---	50.00	PATH
Booting	13.1	14.8	---	---	50.00	PATH
DAG_R_en	15.5	57.8	17.6	26.8	50.00	PATH
Dr	20.5	60.4	25.2	27.6	50.00	PATH

Flush	13.5	36.4	---	---	50.00	PATH
Freeze	16.4	45.3	17.5	27.9	50.00	PATH
Guard	16.9	74.7	17.8	30.9	50.00	PATH
Ids_eq_ods_1	18.2	20.3	---	---	50.00	PATH
Ids_eq_ods_2	18.7	21.0	---	---	50.00	PATH
Ids_freeze	13.5	16.9	11.5	23.0	50.00	PATH
Ids_sel	12.1	15.8	13.2	13.2	50.00	PATH
Inst[0]	---	---	11.4	14.5	50.00	PATH
Inst[10]	---	---	11.9	14.4	50.00	PATH
Inst[11]	---	---	11.9	14.4	50.00	PATH
Inst[12]	---	---	11.9	14.4	50.00	PATH
Inst[13]	---	---	11.8	14.4	50.00	PATH
Inst[14]	---	---	11.8	14.4	50.00	PATH
Inst[15]	---	---	11.7	14.4	50.00	PATH
Inst[16]	---	---	11.8	14.4	50.00	PATH
Inst[17]	---	---	11.8	14.4	50.00	PATH
Inst[18]	---	---	11.8	14.4	50.00	PATH
Inst[19]	---	---	11.8	14.4	50.00	PATH
Inst[1]	---	---	11.5	14.5	50.00	PATH
Inst[20]	---	---	11.8	14.4	50.00	PATH
Inst[21]	---	---	11.9	14.4	50.00	PATH
Inst[22]	---	---	11.9	14.4	50.00	PATH
Inst[23]	---	---	11.9	14.4	50.00	PATH
Inst[24]	---	---	11.7	14.5	50.00	PATH
Inst[25]	---	---	11.6	14.5	50.00	PATH
Inst[26]	---	---	11.8	14.5	50.00	PATH
Inst[27]	---	---	11.9	14.5	50.00	PATH
Inst[28]	---	---	12.0	14.5	50.00	PATH
Inst[29]	---	---	12.0	14.5	50.00	PATH
Inst[2]	---	---	11.6	14.5	50.00	PATH
Inst[30]	---	---	12.1	14.5	50.00	PATH
Inst[31]	---	---	12.1	14.5	50.00	PATH
Inst[32]	---	---	12.0	14.5	50.00	PATH
Inst[33]	---	---	12.1	14.5	50.00	PATH
Inst[34]	---	---	12.1	14.5	50.00	PATH
Inst[35]	---	---	12.1	14.5	50.00	PATH
Inst[36]	---	---	12.2	14.5	50.00	PATH
Inst[37]	---	---	12.2	14.5	50.00	PATH
Inst[38]	---	---	12.3	14.5	50.00	PATH
Inst[39]	---	---	12.3	14.5	50.00	PATH
Inst[3]	---	---	11.6	14.5	50.00	PATH
Inst[40]	---	---	12.3	15.7	50.00	PATH
Inst[41]	---	---	12.5	15.7	50.00	PATH
Inst[42]	---	---	12.0	15.7	50.00	PATH
Inst[43]	---	---	12.0	15.7	50.00	PATH
Inst[44]	---	---	11.7	15.7	50.00	PATH
Inst[45]	---	---	11.7	15.7	50.00	PATH
Inst[4]	---	---	12.2	14.5	50.00	PATH
Inst[5]	---	---	12.2	14.5	50.00	PATH
Inst[6]	---	---	12.1	14.5	50.00	PATH
Inst[7]	---	---	12.0	14.5	50.00	PATH
Inst[8]	---	---	12.0	14.4	50.00	PATH
Inst[9]	---	---	12.0	14.4	50.00	PATH
Inst_en	---	---	13.0	13.2	50.00	PATH

Inst_rd	13.7	49.3	---	---	50.00	PATH
Ios	12.3	13.7	---	---	50.00	PATH
Kernel_mode	21.1	26.3	---	---	50.00	PATH
N_cs_pha	13.9	13.9	8.9	13.5	50.00	PATH
N_cs_phb	13.1	13.1	10.9	13.9	50.00	PATH
N_inst_wr	12.6	12.6	8.2	8.2	50.00	PATH
N_read[1]	12.5	16.7	14.7	16.0	50.00	PATH
N_reset_out	15.4	23.3	---	---	50.00	PATH
N_write[1]	11.0	24.8	12.4	18.5	50.00	PATH
Ncs[1]	10.1	15.4	11.8	14.2	50.00	PATH
Ncs[2]	10.6	15.9	12.2	14.6	50.00	PATH
Ncs[3]	10.7	16.0	12.3	14.7	50.00	PATH
Ods_freeze	13.8	40.7	15.9	16.9	50.00	PATH
Ods_ids[0]	15.6	55.2	17.6	21.4	50.00	PATH
Ods_ids[1]	15.5	55.1	17.5	21.3	50.00	PATH
Ods_ids[2]	15.6	55.2	17.7	21.4	50.00	PATH
Ods_ids[3]	15.6	55.2	17.7	21.4	50.00	PATH
Ods_sel	11.5	16.2	15.3	15.3	50.00	PATH
Pc[0]	---	---	9.5	12.2	50.00	PATH
Pc[10]	---	---	9.5	12.2	50.00	PATH
Pc[11]	---	---	9.5	12.2	50.00	PATH
Pc[12]	---	---	9.5	12.2	50.00	PATH
Pc[13]	---	---	9.5	12.2	50.00	PATH
Pc[14]	---	---	9.5	12.2	50.00	PATH
Pc[15]	---	---	9.5	12.2	50.00	PATH
Pc[16]	---	---	9.5	12.2	50.00	PATH
Pc[17]	---	---	9.5	12.2	50.00	PATH
Pc[18]	---	---	9.5	12.2	50.00	PATH
Pc[19]	---	---	9.5	12.2	50.00	PATH
Pc[1]	---	---	9.5	12.2	50.00	PATH
Pc[20]	---	---	9.5	12.2	50.00	PATH
Pc[21]	---	---	9.5	12.2	50.00	PATH
Pc[22]	---	---	9.5	12.2	50.00	PATH
Pc[23]	---	---	9.5	12.2	50.00	PATH
Pc[24]	---	---	9.5	12.2	50.00	PATH
Pc[25]	---	---	9.5	12.2	50.00	PATH
Pc[2]	---	---	9.5	12.2	50.00	PATH
Pc[3]	---	---	9.5	12.2	50.00	PATH
Pc[4]	---	---	9.5	12.2	50.00	PATH
Pc[5]	---	---	9.5	12.2	50.00	PATH
Pc[6]	---	---	9.5	12.2	50.00	PATH
Pc[7]	---	---	9.5	12.2	50.00	PATH
Pc[8]	---	---	9.5	12.2	50.00	PATH
Pc[9]	---	---	9.5	12.2	50.00	PATH
RF[0]	14.8	78.1	16.3	25.8	50.00	PATH
RF[10]	14.1	77.7	16.9	30.6	50.00	PATH
RF[11]	14.0	77.6	16.9	26.7	50.00	PATH
RF[12]	14.0	77.6	16.9	25.6	50.00	PATH
RF[13]	13.9	77.6	16.9	25.7	50.00	PATH
RF[14]	13.8	77.5	16.9	26.8	50.00	PATH
RF[15]	14.0	77.6	16.9	25.6	50.00	PATH
RF[16]	14.1	87.0	15.4	41.8	50.00	PATH
RF[17]	14.1	77.7	15.4	27.7	50.00	PATH
RF[18]	13.8	77.5	15.4	29.3	50.00	PATH

RF[19]	13.9	77.6	15.4	27.9	50.00	PATH
RF[1]	14.7	78.1	16.3	25.8	50.00	PATH
RF[20]	14.4	78.0	15.4	25.6	50.00	PATH
RF[21]	14.0	77.7	15.4	25.3	50.00	PATH
RF[22]	13.8	77.6	15.4	40.5	50.00	PATH
RF[23]	13.6	77.4	15.4	25.1	50.00	PATH
RF[24]	13.3	77.2	16.2	24.9	50.00	PATH
RF[25]	13.5	77.4	16.2	26.9	50.00	PATH
RF[26]	13.1	55.9	16.2	24.9	50.00	PATH
RF[27]	13.1	55.9	16.2	24.9	50.00	PATH
RF[28]	12.8	55.9	16.2	24.9	50.00	PATH
RF[29]	12.8	55.9	16.2	24.9	50.00	PATH
RF[2]	14.7	78.0	16.3	25.7	50.00	PATH
RF[30]	12.7	55.9	16.2	24.9	50.00	PATH
RF[31]	12.6	55.9	16.2	24.9	50.00	PATH
RF[3]	14.6	78.0	16.3	25.7	50.00	PATH
RF[4]	14.5	78.0	16.3	25.6	50.00	PATH
RF[5]	14.5	77.9	16.3	25.6	50.00	PATH
RF[6]	14.4	77.9	16.3	25.6	50.00	PATH
RF[7]	14.4	77.9	16.3	25.6	50.00	PATH
RF[8]	14.2	77.8	16.9	30.4	50.00	PATH
RF[9]	14.3	77.8	16.9	28.2	50.00	PATH
Read[2]	18.2	21.7	17.8	20.9	50.00	PATH
Read[3]	20.5	24.1	19.9	23.2	50.00	PATH
Valid_intr_pulse	17.1	30.1	---	---	50.00	PATH
Write[2]	11.3	24.5	14.1	14.8	50.00	PATH
Write[3]	11.3	24.5	14.1	14.8	50.00	PATH

Genesil Version v8.0.2 -- Mon Feb 4 11:14:00 1991

Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/iag Timing Analyzer

SETUP AND HOLD MODE

Fabline: HP2_CN10B Corner: TYPICAL

Junction Temperature: 75 deg C Voltage: 5.00v

External Clock: Clk

Included setup files:

#0 basic (Input constraints from other chip>

#1 baseline (75 deg C, 5.0 Volts)

INPUT SETUP AND HOLD TIMES (ns)

Input	Setup Time		Hold Time		
	Ph1(f)	Ph2(f)	Ph1(f)	Ph2(f)	
ALU_Flag	22.2	3.4	0.1	-2.4	PATH
Carry	21.8	3.4	0.1	-2.4	PATH
DAG_error	---	5.7	---	-2.9	PATH
DAV[1]	---	39.8	---	-7.0	PATH
DAV[2]	---	40.2	---	-7.1	PATH
DAV[3]	---	40.4	---	-7.4	PATH
Dr	19.9	41.8	-2.2	-1.6	PATH
IAG_test[0]	---	37.2	---	-0.3	PATH
IAG_test[1]	---	37.2	---	-0.4	PATH
Inst[0]	---	4.0	---	-2.5	PATH
Inst[10]	---	4.7	---	-2.9	PATH

Inst[11]	---	4.5	---	-2.9	PATH
Inst[12]	---	3.6	---	-2.3	PATH
Inst[13]	---	3.5	---	-2.3	PATH
Inst[14]	---	3.3	---	-2.1	PATH
Inst[15]	---	3.3	---	-2.0	PATH
Inst[16]	---	3.3	---	-2.1	PATH
Inst[17]	---	3.3	---	-2.1	PATH
Inst[18]	---	3.4	---	-2.1	PATH
Inst[19]	---	3.4	---	-2.2	PATH
Inst[1]	---	4.2	---	-2.6	PATH
Inst[20]	---	3.4	---	-2.2	PATH
Inst[21]	---	3.5	---	-2.2	PATH
Inst[22]	---	3.4	---	-2.2	PATH
Inst[23]	---	3.3	---	-2.0	PATH
Inst[24]	---	3.2	---	-1.9	PATH
Inst[25]	---	3.2	---	-1.9	PATH
Inst[26]	---	4.5	---	-2.5	PATH
Inst[27]	---	4.9	---	-2.7	PATH
Inst[28]	---	5.3	---	-2.9	PATH
Inst[29]	---	4.7	---	-2.9	PATH
Inst[2]	---	4.6	---	-3.1	PATH
Inst[30]	---	3.1	---	-1.9	PATH
Inst[31]	---	3.4	---	-2.2	PATH
Inst[32]	---	3.1	---	-1.9	PATH
Inst[33]	---	3.1	---	-1.9	PATH
Inst[34]	---	3.1	---	-1.9	PATH
Inst[35]	---	3.1	---	-1.9	PATH
Inst[36]	---	3.1	---	-1.9	PATH
Inst[37]	---	3.8	---	-2.7	PATH
Inst[38]	---	4.7	---	-2.6	PATH
Inst[39]	---	4.8	---	-2.7	PATH
Inst[3]	---	4.8	---	-3.2	PATH
Inst[40]	---	4.9	---	-2.8	PATH
Inst[41]	---	4.8	---	-2.7	PATH
Inst[42]	---	5.5	---	-3.5	PATH
Inst[43]	---	5.4	---	-3.5	PATH
Inst[44]	---	5.3	---	-3.3	PATH
Inst[45]	---	5.3	---	-3.3	PATH
Inst[4]	---	5.0	---	-3.1	PATH
Inst[5]	---	4.4	---	-3.1	PATH
Inst[6]	---	5.1	---	-3.1	PATH
Inst[7]	---	4.4	---	-3.0	PATH
Inst[8]	---	4.6	---	-3.0	PATH
Inst[9]	---	4.5	---	-2.9	PATH
Inst_rdy	---	13.5	---	-0.4	PATH
Intr[0]	---	5.8	---	-4.2	PATH
Intr[1]	---	5.8	---	-4.3	PATH
Intr[2]	---	5.8	---	-4.3	PATH
Intr[3]	---	5.8	---	-4.3	PATH
Intr[4]	---	5.8	---	-4.3	PATH
Intr[5]	---	5.9	---	-4.4	PATH
Intr[6]	---	5.9	---	-4.4	PATH
Intr[7]	---	5.9	---	-4.4	PATH
Intr[8]	---	5.4	---	-3.8	PATH

N_reset	-1.4	---	2.7	---	PATH
Pixel_clk	20.9	43.3	-10.1	-1.1	PATH
RFI[1]	19.5	---	-0.9	---	PATH
RFI[2]	19.4	---	-1.0	---	PATH
RFI[3]	19.5	---	-0.8	---	PATH
RF[0]	1.1	2.2	-0.4	-0.2	PATH
RF[10]	1.3	2.3	-0.5	-0.4	PATH
RF[11]	1.2	2.3	-0.5	-0.3	PATH
RF[12]	1.2	2.3	-0.5	-0.3	PATH
RF[13]	1.5	2.6	-0.7	-0.6	PATH
RF[14]	1.2	2.3	-0.4	-0.3	PATH
RF[15]	1.2	2.3	-0.5	-0.3	PATH
RF[16]	1.3	2.4	-0.6	-0.4	PATH
RF[17]	1.3	2.4	-0.5	-0.4	PATH
RF[18]	1.1	2.2	-0.4	-0.2	PATH
RF[19]	1.3	2.3	-0.5	-0.4	PATH
RF[1]	2.0	3.1	-1.3	-1.1	PATH
RF[20]	1.1	2.2	-0.3	-0.2	PATH
RF[21]	1.2	2.3	-0.4	-0.3	PATH
RF[22]	1.3	2.3	-0.5	-0.3	PATH
RF[23]	1.4	2.5	-0.6	-0.5	PATH
RF[24]	1.4	2.5	-0.6	-0.5	PATH
RF[25]	1.6	2.6	-0.8	-0.7	PATH
RF[26]	---	0.6	---	0.2	PATH
RF[27]	---	0.6	---	0.2	PATH
RF[28]	---	0.5	---	0.3	PATH
RF[29]	---	0.4	---	0.3	PATH
RF[2]	1.2	2.2	-0.4	-0.3	PATH
RF[30]	---	0.4	---	0.4	PATH
RF[31]	---	0.3	---	0.4	PATH
RF[3]	1.2	2.3	-0.4	-0.3	PATH
RF[4]	1.2	2.3	-0.4	-0.3	PATH
RF[5]	1.9	3.0	-1.2	-1.1	PATH
RF[6]	1.2	2.3	-0.5	-0.3	PATH
RF[7]	1.2	2.3	-0.5	-0.3	PATH
RF[8]	1.3	2.3	-0.5	-0.4	PATH
RF[9]	1.6	2.7	-0.8	-0.7	PATH
R_eq_f_1	---	30.8	---	-3.5	PATH
R_eq_f_2	---	3.7	---	-1.6	PATH
S_eq_f_1	---	3.6	---	-2.6	PATH
S_eq_f_2	---	3.6	---	-2.6	PATH
Sign	22.3	3.3	0.2	-2.3	PATH
Status[0]	15.2	---	-1.9	---	PATH
Status[1]	15.2	---	-1.9	---	PATH
Status[2]	16.2	---	-2.9	---	PATH
Status[3]	15.0	---	-1.5	---	PATH
Status[4]	14.7	---	-1.5	---	PATH
Zero	21.9	3.3	0.2	-2.3	PATH

Genesil Version v8.0.2 -- Mon Feb 4 11:18:30 1991

Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/iag

Timing Analyzer

PATH DELAY MODE

Fabline: HP2_CN10B

Corner: TYPICAL

Junction Temperature: 75 deg C

Voltage: 5.00v

External Clock: Clk

Included setup files:

#0 basic (Input constraints from other chip>

#1 baseline (75 deg C, 5.0 Volts)

		PATH DELAY (ns)			
Source Object	Connector	(Ph1) Min	Max		
Dest. Object	Connector	(Ph2) Min	Max		
clk_pad_____	PHASE_A_____	4.8	11.0		
io_mod/sell_____	ods_en_____	9.6	11.5	PATH	
io_mod/sell_____	ods_en_____	---	---		
*CURRENT*_____	Ncs[1]_____	---	---	PATH	
clk_pad_____	PHASE_A_____	4.4	4.9		
io_mod/sell_____	ods_inst[3]_____	---	---	PATH	
io_mod/sell_____	ods_inst[3]_____	---	---		
*CURRENT*_____	Ncs[1]_____	---	---	PATH	
clk_pad_____	PHASE_A_____	4.8	11.0		
io_mod/sell_____	ods_en_____	9.6	11.5	PATH	
io_mod/sell_____	ods_en_____	8.4	9.3		
*CURRENT*_____	N_write[1]_____	---	---	PATH	
clk_pad_____	PHASE_A_____	4.4	4.9		
io_mod/sell_____	ods_inst[3]_____	---	---	PATH	
io_mod/sell_____	ods_inst[3]_____	---	---		
*CURRENT*_____	N_write[1]_____	---	---	PATH	
io_mod/io_dp_____	ods_en_____	8.4	9.8		
*CURRENT*_____	Ods_ids[2]_____	8.4	9.8	PATH	
io_mod/io_dp_____	ids_sel_____	8.7	10.9		
*CURRENT*_____	Ods_ids[2]_____	8.7	10.9	PATH	
io_mod/io_dp_____	dff1_VAL1[2]_____	9.2	10.6		
*CURRENT*_____	Ods_ids[2]_____	9.2	10.6	PATH	

>

```

*****
          Genesil Version v8.0.2 -- Mon Feb  4 11:18:36 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/iag          Timing Analyzer
*****
NODE DELAY MODE
-----
Fabline: HP2_CN10B          Corner: TYPICAL
Junction Temperature:75 deg C      Voltage:5.00v
External Clock: Clk
Included setup files:
#0 basic          (Input constraints from other chip>
#1 baseline       (75 deg C, 5.0 Volts)
-----

```

NODE DELAYS (ns)

Object	Connector	Ph1(r) Delay Min Max	Ph2(r) Delay Min Max	
io_mod/io_dp__	ods_en__	9.3 15.5	11.2 13.1	PATH
io_mod/io_dp__	ids_sel__	6.5 10.2	9.0 9.0	PATH
io_mod/io_dp__	dff1_VAL1[2]__	6.5 6.9	--- ---	PATH

>

```

*****
          Genesil Version v8.0.2 -- Mon Feb  4 11:18:50 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/iag          Timing Analyzer
*****
VIOLATION MODE
-----
Fabline: HP2_CN10B          Corner: TYPICAL
Junction Temperature:75 deg C      Voltage:5.00v
External Clock: Clk
Included setup files:
#0 basic          (Input constraints from other chip>
#1 baseline       (75 deg C, 5.0 Volts)
-----

```

NO VIOLATIONS

Hold time check margin: 2.0ns

13.2. GUARANTEED, Room T, 5.0V

```

*****
          Genesil Version v8.0.2 -- Mon Feb  4 11:37:55 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/iag          Timing Analyzer
*****
VIOLATION MODE
-----
Fabline: HP2_CN10B          Corner: TYPICAL

```

```

Junction Temperature:67 deg C      Voltage:5.00v
External Clock: Clk
Included setup files:
#0 basic          (Input constraints from other chip>
#1 room          (67 deg C, 5.0 Volts)

```

NO VIOLATIONS

Hold time check margin: 2.0ns

Genesil Version v8.0.2 -- Mon Feb 4 12:08:59 1991

Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/iag Timing Analyzer

CLOCK REPORT MODE

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Fabline: HP2_CN10B          Corner: GUARANTEED
Junction Temperature:67 deg C      Voltage:5.00v
External Clock: Clk
Included setup files:
#0 basic          (Input constraints from other chip>
#1 room          (67 deg C, 5.0 Volts)

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CLOCK TIMES (minimum)

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Phase 1 High: 73.9 ns      Phase 2 High: 69.2 ns
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Cycle (from Ph1): 122.5 ns      Cycle (from Ph2): 143.9 ns
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Minimum Cycle Time: 143.9 ns      Symmetric Cycle Time: 147.8 ns
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CLOCK WORST CASE PATHS

Minimum Phase 1 high time is 73.9 ns set by:

** Clock delay: 4.5ns (78.4-73.9)

Node	Cumulative Delay	Transition
<c_ndp_mod/pc_latch/(internal)	78.4	fall
<od/pc_ndp_mod/pc_latch/IN[23]	77.4	rise
<d/pc_ndp_mod/pc_unlat/OUT[23]	77.4	rise
</pc_ndp_mod/pc_unlat/OUT[23]'	77.3	rise
<od/pc_ndp_mod/pc_unlat/IN[23]	77.0	fall
<pc_ndp_mod/n_pc_unlat/OUT[23]	77.0	fall
<c_ndp_mod/n_pc_unlat/OUT[23]'	76.9	fall
<pc_ndp_mod/n_pc_unlat/IN1[23]	76.3	rise
<_mod/pc_ndp_mod/ready/OUT[23]	76.3	rise
<mod/pc_ndp_mod/ready/OUT[23]'	76.2	rise
<n_mod/pc_ndp_mod/ready/IN[23]	75.9	fall
<od/pc_ndp_mod/n_ready/OUT[23]	75.9	fall
<d/pc_ndp_mod/n_ready/OUT[23]'	75.8	fall
<od/pc_ndp_mod/n_ready/IN1[23]	75.3	rise
<_mod/pc_ndp_mod/alpha/OUT[23]	75.3	rise
<mod/pc_ndp_mod/alpha/OUT[23]'	75.2	rise
<n_mod/pc_ndp_mod/alpha/IN[23]	74.8	fall
<od/pc_ndp_mod/n_alpha/OUT[23]	74.8	fall
<d/pc_ndp_mod/n_alpha/OUT[23]'	74.8	fall
<od/pc_ndp_mod/n_alpha/IN1[23]	74.2	rise

<mod/pc_ndp_mod/br_adr/OUT[23]	74.2	rise
<od/pc_ndp_mod/br_adr/OUT[23]'	67.3	rise
<_mod/pc_ndp_mod/br_adr/IN[23]	67.0	fall
<d/pc_ndp_mod/n_br_adr/OUT[23]	67.0	fall
</pc_ndp_mod/n_br_adr/OUT[23]'	66.9	fall
<d/pc_ndp_mod/n_br_adr/IN2[23]	66.4	rise
<d/pc_ndp_mod/absolute/OUT[23]	66.4	rise
</pc_ndp_mod/absolute/OUT[23]'	65.8	rise
<od/pc_ndp_mod/absolute/IN[23]	65.5	fall
<pc_ndp_mod/n_absolute/OUT[23]	65.5	fall
<c_ndp_mod/n_absolute/OUT[23]'	65.4	fall
<pc_ndp_mod/n_absolute/IN2[23]	64.9	rise
intr_mod/ram/intr_vect[23]	64.8	rise
intr_mod/ram/intr_vect[23]'	64.2	rise
intr_mod/ram/st_vect_adr[2]	49.5	rise
<intr_vect_ctrl/st_vect_adr[2]	49.4	rise
<ntr_vect_ctrl/st_vect_adr[2]'	44.6	rise
</intr_vect_ctrl/GB.LP.NN25fN2	44.2	fall
<tr_vect_ctrl/valid_intr_pulse	43.7	rise
<r_mod/valid_intr_ctrl/vip_out	42.3	rise
<_mod/valid_intr_ctrl/vip_out'	34.7	rise
<alid_intr_ctrl/GB.LP.NN25fN21	34.5	fall
<alid_intr_ctrl/GB.LP.NN25fN11	33.1	rise
<valid_intr_ctrl/GB.LP.NN25fN7	32.1	fall
<valid_intr_ctrl/GB.LP.NN25fN0	31.7	rise
<valid_intr_ctrl/GB.LP.NN25fN6	30.3	fall
<valid_intr_ctrl/GB.LP.NN25fN3	29.9	rise
<od/valid_intr_ctrl/rd_wr_intr	29.1	fall
inst_mod/rd_wr_inst/rd_wr_intr	28.1	fall
<st_mod/rd_wr_inst/rd_wr_intr'	25.2	fall
inst_mod/rd_wr_inst/read_write	24.1	fall
<t_mod/rd_wr_inst/pc_min_op[1]	21.8	rise
<t_mod/inst_in_dp/pc_min_op[1]	21.5	rise
<_mod/inst_in_dp/pc_min_op[1]'	12.4	rise
<st_mod/inst_in_dp/dff_VAL2[1]	11.2	rise
inst_mod/inst_in_dp/PHASE_A	7.7	rise
clk_pad/PHASE_A	6.8	rise
Clk	0.0	rise

Minimum Phase 2 high time is 69.2 ns set by:

** Clock delay: 4.4ns (73.7-69.2)

Node	Cumulative Delay	Transition
<atus_mod/status_dp/(internal)	73.7	fall
<_mod/status_dp/INTER3_ST1[20]	72.4	rise
<mod/status_dp/intr_status[20]	70.6	rise
</priority_pla/req_intr_adr[3]	70.2	rise
<priority_pla/req_intr_adr[3]'	59.6	rise
<d/priority_pla/GB.LP.NN25fN36	58.6	rise
<d/priority_pla/GB.LP.NN25fN47	57.6	fall
<d/priority_pla/GB.LP.NN25fN51	57.3	rise
<d/priority_pla/GB.LP.NN25fN40	56.0	fall
<d/priority_pla/GB.LP.NN25fN12	55.5	rise
<d/priority_pla/GB.LP.NN25fN14	53.4	rise

</priority_pla/current_intr[4]	50.6	fall
<r_mod/intr_dp/current_intr[4]	50.6	fall
<_mod/intr_dp/current_intr[4]'	50.5	fall
<r_mod/intr_dp/phb_lat_VAL1[4]	49.3	fall
intr_mod/intr_dp/guarded_ei	42.3	rise
intr_mod/ld_ctrl/guarded_ei	42.3	rise
intr_mod/ld_ctrl/guarded_ei'	40.9	rise
intr_mod/ld_ctrl/n_guard	39.9	rise
io_mod/ids_sel/n_guard_out	38.5	rise
io_mod/ids_sel/n_guard_out'	33.9	rise
io_mod/ids_sel/n_guard	33.1	rise
io_mod/freeze_ctrl/n_guard	33.1	rise
io_mod/freeze_ctrl/n_guard'	32.0	rise
<od/freeze_ctrl/GB.LP.NNZ5fN14	31.8	fall
<od/freeze_ctrl/GB.LP.NNZ5fN34	31.1	rise
<mod/freeze_ctrl/GB.LP.NNZ5fN2	30.3	fall
<mod/freeze_ctrl/GB.LP.NNZ5fN6	29.9	rise
<mod/freeze_ctrl/GB.LP.NNZ5fN9	28.5	rise
io_mod/freeze_ctrl/ids_freeze	27.4	fall
io_mod/test_ctrl/ids_freeze	27.3	fall
io_mod/test_ctrl/ids_freeze'	26.0	fall
io_mod/test_ctrl/ids_fr_lat	24.9	fall
io_mod/test_ctrl/ids_fr_lat'	24.9	fall
io_mod/test_ctrl/ids_freeze_in	22.6	fall
io_mod/ds_ctrl/ids_freeze_in	22.6	fall
io_mod/ds_ctrl/ids_freeze_in'	22.6	fall
io_mod/ds_ctrl/async_ids_fr	21.2	fall
<d/async_ids_ctrl/async_ids_fr	21.2	fall
</async_ids_ctrl/async_ids_fr'	20.8	fall
<async_ids_ctrl/GB.LP.NNZ5fN27	20.5	rise
<async_ids_ctrl/GB.LP.NNZ5fN15	18.8	fall
<async_ids_ctrl/GB.LP.NNZ5fN18	18.3	rise
<async_ids_ctrl/GB.LP.NNZ5fN28	17.2	fall
</async_ids_ctrl/GB.LP.NNZ5fN6	15.6	rise
<async_ids_ctrl/GB.LP.NNZ5fN12	14.9	fall
io_mod/async_ids_ctrl/ids_sel	14.4	rise
io_mod/ids_sel/ids_sel	14.3	rise
io_mod/ids_sel/ids_sel'	11.6	rise
io_mod/ids_sel/ids_sel_buf	10.7	rise
io_mod/ids_sel/ids_sel_buf'	10.5	rise
io_mod/ids_sel/ids_ph_in	8.7	rise
io_mod/ids_sel/ids_ph_out	8.7	rise
io_mod/ids_sel/ids_ph_out'	8.6	rise
io_mod/ids_sel/PHASE_B	7.0	rise
clk_pad/PHASE_B	6.4	rise
Clk	0.0	fall

Minimum cycle time (from Ph1) is 122.5 ns set by:

** Clock delay: 4.4ns (126.9-122.5)

Node	Cumulative Delay	Transition
<atus_mod/status_dp/(internal)	126.9	fall
status_mod/status_dp/389	126.0	fall
<_mod/status_dp/INTER3_ST1[20]	125.7	rise

<mod/status_dp/intr_status[20]	123.8	rise
</priority_pla/req_intr_adr[3]	123.5	rise
<priority_pla/req_intr_adr[3]'	112.9	rise
<d/priority_pla/GB.LP.NNZ5fN36	111.8	rise
<d/priority_pla/GB.LP.NNZ5fN47	110.9	fall
<d/priority_pla/GB.LP.NNZ5fN51	110.5	rise
<d/priority_pla/GB.LP.NNZ5fN40	109.3	fall
<d/priority_pla/GB.LP.NNZ5fN12	108.7	rise
<d/priority_pla/GB.LP.NNZ5fN14	106.7	rise
</priority_pla/current_intr[4]	103.9	fall
<r_mod/intr_dp/current_intr[4]	103.8	fall
<_mod/intr_dp/current_intr[4]'	103.8	fall
<r_mod/intr_dp/phb_lat_VAL1[4]	102.5	fall
intr_mod/intr_dp/guarded_ei	95.6	rise
intr_mod/ld_ctrl/guarded_ei	95.6	rise
intr_mod/ld_ctrl/guarded_ei'	94.1	rise
intr_mod/ld_ctrl/n_guard	93.2	rise
io_mod/ids_sel/n_guard_out	91.7	rise
io_mod/ids_sel/n_guard_out'	87.2	rise
io_mod/ids_sel/n_guard	86.3	rise
io_mod/freeze_ctrl/n_guard	86.3	rise
io_mod/freeze_ctrl/n_guard'	85.3	rise
<od/freeze_ctrl/GB.LP.NNZ5fN14	85.0	fall
<od/freeze_ctrl/GB.LP.NNZ5fN34	84.4	rise
<mod/freeze_ctrl/GB.LP.NNZ5fN2	83.6	fall
<mod/freeze_ctrl/GB.LP.NNZ5fN6	83.1	rise
<mod/freeze_ctrl/GB.LP.NNZ5fN9	81.7	rise
io_mod/freeze_ctrl/ids_freeze	80.6	fall
io_mod/test_ctrl/ids_freeze	80.6	fall
io_mod/test_ctrl/ids_freeze'	79.3	fall
io_mod/test_ctrl/ids_fr_lat	78.2	fall
io_mod/test_ctrl/ids_fr_lat'	78.1	fall
io_mod/test_ctrl/ids_freeze_in	75.9	fall
io_mod/ds_ctrl/ids_freeze_in	75.9	fall
io_mod/ds_ctrl/ids_freeze_in'	75.8	fall
io_mod/ds_ctrl/async_ids_fr	74.4	fall
<d/async_ids_ctrl/async_ids_fr	74.4	fall
</async_ids_ctrl/async_ids_fr'	74.1	fall
<async_ids_ctrl/GB.LP.NNZ5fN27	73.8	rise
<async_ids_ctrl/GB.LP.NNZ5fN15	72.0	fall
<async_ids_ctrl/GB.LP.NNZ5fN18	71.6	rise
<async_ids_ctrl/GB.LP.NNZ5fN28	70.4	fall
</async_ids_ctrl/GB.LP.NNZ5fN6	68.9	rise
<async_ids_ctrl/GB.LP.NNZ5fN12	68.1	fall
io_mod/async_ids_ctrl/ids_sel	67.7	rise
io_mod/ids_sel/ids_sel	67.5	rise
io_mod/ids_sel/ids_sel'	64.8	rise
io_mod/ids_sel/ids_sel_buf	63.9	rise
io_mod/ids_sel/ids_sel_buf'	63.7	rise
io_mod/ids_sel/ids_ph_in	62.0	rise
io_mod/ids_sel/ids_ph_out	62.0	rise
io_mod/ids_sel/ids_ph_out'	61.8	rise
*io_mod/ids_sel/(internal)	60.3	fall
io_mod/ids_sel/n_ods_freeze	58.0	rise

io_mod/ids_sel/ods_freeze	57.4	fall
io_mod/test_ctrl/ods_freeze	57.3	fall
io_mod/test_ctrl/ods_freeze'	53.8	fall
io_mod/test_ctrl/ods_fr_lat	52.7	fall
io_mod/test_ctrl/ods_freeze_in	50.4	fall
io_mod/ds_ctrl/ods_freeze_in	50.4	fall
io_mod/ds_ctrl/ods_freeze_in'	49.8	fall
io_mod/ds_ctrl/async_ods_fr	48.4	fall
<d/async_ods_ctrl/async_ods_fr	48.4	fall
</async_ods_ctrl/async_ods_fr'	48.1	fall
<async_ods_ctrl/GB.LP.NNZ5fN30	47.8	rise
</async_ods_ctrl/GB.LP.NNZ5fN1	45.6	fall
<ync_ods_ctrl/valid_intr_pulse	45.1	rise
<_mod/ids_sel/valid_intr_pulse	45.1	rise
<mod/ids_sel/valid_intr_pulse'	44.1	rise
io_mod/ids_sel/vip_in	43.3	rise
<r_mod/valid_intr_ctrl/vip_out	42.3	rise
<_mod/valid_intr_ctrl/vip_out'	34.7	rise
<alid_intr_ctrl/GB.LP.NNZ5fN21	34.5	fall
<alid_intr_ctrl/GB.LP.NNZ5fN11	33.1	rise
<valid_intr_ctrl/GB.LP.NNZ5fN7	32.1	fall
<valid_intr_ctrl/GB.LP.NNZ5fN0	31.7	rise
<valid_intr_ctrl/GB.LP.NNZ5fN6	30.3	fall
<valid_intr_ctrl/GB.LP.NNZ5fN3	29.9	rise
<od/valid_intr_ctrl/rd_wr_intr	29.1	fall
inst_mod/rd_wr_inst/rd_wr_intr	28.1	fall
<st_mod/rd_wr_inst/rd_wr_intr'	25.2	fall
inst_mod/rd_wr_inst/read_write	24.1	fall
<t_mod/rd_wr_inst/pc_min_op[1]	21.8	rise
<t_mod/inst_in_dp/pc_min_op[1]	21.5	rise
<_mod/inst_in_dp/pc_min_op[1]'	12.4	rise
<st_mod/inst_in_dp/dfv_VAL2[1]	11.2	rise
inst_mod/inst_in_dp/PHASE_A	7.7	rise
clk_pad/PHASE_A	6.8	rise
Clk	0.0	rise

Minimum cycle time (from Ph2) is 143.9 ns set by:

 ** Clock delay: 7.5ns (151.4-143.9)

Node	Cumulative Delay	Transition
<_gen_mod/stk_pc_dp/(internal)	151.4	fall
<gen_mod/stk_pc_dp/next_pc[24]	151.1	rise
<_ndp_mod/next_pc_buff/OUT[24]	150.9	rise
<ndp_mod/next_pc_buff/OUT[24]'	143.8	rise
<c_ndp_mod/next_pc_buff/IN[24]	142.8	rise
<ndp_mod/next_pc_adder/OUT[24]	142.8	rise
<dp_mod/next_pc_adder/OUT[24]'	142.7	rise
<_ndp_mod/next_pc_adder/IN1[1]	132.6	rise
<mod/pc_ndp_mod/pc_buff/OUT[1]	132.6	rise
<od/pc_ndp_mod/pc_buff/OUT[1]'	124.2	rise
<_mod/pc_ndp_mod/pc_buff/IN[1]	123.4	rise
<od/pc_ndp_mod/pc_latch/OUT[1]	123.4	rise
<d/pc_ndp_mod/pc_latch/OUT[1]'	123.1	rise
<mod/pc_ndp_mod/pc_latch/IN[1]	121.7	rise

<od/pc_ndp_mod/pc_unlat/OUT[1]	121.7	rise
<d/pc_ndp_mod/pc_unlat/OUT[1]'	121.6	rise
<mod/pc_ndp_mod/pc_unlat/IN[1]	121.3	fall
</pc_ndp_mod/n_pc_unlat/OUT[1]	121.3	fall
<pc_ndp_mod/n_pc_unlat/OUT[1]'	121.3	fall
</pc_ndp_mod/n_pc_unlat/IN1[1]	120.7	rise
<n_mod/pc_ndp_mod/ready/OUT[1]	120.7	rise
<_mod/pc_ndp_mod/ready/OUT[1]'	120.6	rise
<en_mod/pc_ndp_mod/ready/IN[1]	120.3	fall
<mod/pc_ndp_mod/n_ready/OUT[1]	120.3	fall
<od/pc_ndp_mod/n_ready/OUT[1]'	120.2	fall
<mod/pc_ndp_mod/n_ready/IN1[1]	119.7	rise
<n_mod/pc_ndp_mod/alpha/OUT[1]	119.7	rise
<_mod/pc_ndp_mod/alpha/OUT[1]'	119.5	rise
<en_mod/pc_ndp_mod/alpha/IN[1]	119.2	fall
<mod/pc_ndp_mod/n_alpha/OUT[1]	119.2	fall
<od/pc_ndp_mod/n_alpha/OUT[1]'	119.2	fall
<mod/pc_ndp_mod/n_alpha/IN1[1]	118.6	rise
<_mod/pc_ndp_mod/br_adr/OUT[1]	118.6	rise
<mod/pc_ndp_mod/br_adr/OUT[1]'	112.4	rise
<n_mod/pc_ndp_mod/br_adr/IN[1]	112.1	fall
<od/pc_ndp_mod/n_br_adr/OUT[1]	112.1	fall
<d/pc_ndp_mod/n_br_adr/OUT[1]'	112.0	fall
<od/pc_ndp_mod/n_br_adr/IN1[1]	111.4	rise
<_gen_mod/pc_ndp_mod/x1/OUT[1]	111.4	rise
<gen_mod/pc_ndp_mod/x1/OUT[1]'	111.3	rise
pc_gen_mod/pc_ndp_mod/x1/IN[1]	111.0	fall
<en_mod/pc_ndp_mod/n_x1/OUT[1]	111.0	fall
<n_mod/pc_ndp_mod/n_x1/OUT[1]'	110.9	fall
<en_mod/pc_ndp_mod/n_x1/SEL[0]	109.0	rise
pc_gen_mod/flush_ctrl/dis_tp	108.5	rise
pc_gen_mod/flush_ctrl/dis_tp'	105.9	rise
<_mod/flush_ctrl/GB.LP.NNZ5fN5	105.6	fall
<mod/flush_ctrl/GB.LP.NNZ5fN10	104.8	rise
<mod/flush_ctrl/GB.LP.NNZ5fN20	104.2	fall
<mod/flush_ctrl/GB.LP.NNZ5fN12	103.8	rise
pc_gen_mod/flush_ctrl/rs	103.0	fall
task_ptr_mod/task_ptr_ctrl/rs	102.2	fall
task_ptr_mod/task_ptr_ctrl/rs'	101.0	fall
<_ptr_mod/task_ptr_ctrl/rs_out	100.1	fall
task_ptr_mod/tp_en_dec/rs_out	100.1	fall
task_ptr_mod/tp_en_dec/rs_out'	99.0	fall
<r_mod/tp_en_dec/GB.LP.NNZ5fN3	98.6	rise
<n_dec/GB.LP.NNin222eINZ5b0Z5d	98.0	fall
<od/tp_en_dec/valid_intr_pulse	97.5	rise
<r_mod/valid_intr_ctrl/vip_out	95.1	rise
<_mod/valid_intr_ctrl/vip_out'	87.5	rise
<alid_intr_ctrl/GB.LP.NNZ5fN21	87.3	fall
<alid_intr_ctrl/GB.LP.NNZ5fN11	85.9	rise
<valid_intr_ctrl/GB.LP.NNZ5fN7	84.9	fall
<valid_intr_ctrl/GB.LP.NNZ5fN0	84.5	rise
<valid_intr_ctrl/GB.LP.NNZ5fN6	83.1	fall
<valid_intr_ctrl/GB.LP.NNZ5fN3	82.7	rise
<alid_intr_ctrl/GB.LP.NNZ5fN10	81.0	rise

<P.NNnpassintZ2eoutZ5fxZ5b0Z5d	79.5	fall
*</valid_intr_ctrl/n_pass_intr	77.0	fall
<_mod/pass_intr_dp/n_pass_intr	77.0	fall
<mod/pass_intr_dp/n_pass_intr'	76.6	fall
</pass_intr_dp/req_intr_adr[0]	70.0	rise
</priority_pla/req_intr_adr[0]	69.9	rise
<priority_pla/req_intr_adr[0]'	59.4	rise
<od/priority_pla/GB.LP.NN25fn1	59.1	fall
<d/priority_pla/GB.LP.NN25fn36	58.6	rise
<d/priority_pla/GB.LP.NN25fn47	57.6	fall
<d/priority_pla/GB.LP.NN25fn51	57.3	rise
<d/priority_pla/GB.LP.NN25fn40	56.0	fall
<d/priority_pla/GB.LP.NN25fn12	55.5	rise
<d/priority_pla/GB.LP.NN25fn14	53.4	rise
</priority_pla/current_intr[4]	50.6	fall
<r_mod/intr_dp/current_intr[4]	50.6	fall
<_mod/intr_dp/current_intr[4]'	50.5	fall
<r_mod/intr_dp/phb_lat_VAL1[4]	49.3	fall
intr_mod/intr_dp/guarded_ei	42.3	rise
intr_mod/ld_ctrl/guarded_ei	42.3	rise
intr_mod/ld_ctrl/guarded_ei'	40.9	rise
intr_mod/ld_ctrl/n_guard	39.9	rise
io_mod/ids_sel/n_guard_out	38.5	rise
io_mod/ids_sel/n_guard_out'	33.9	rise
io_mod/ids_sel/n_guard	33.1	rise
io_mod/freeze_ctrl/n_guard	33.1	rise
io_mod/freeze_ctrl/n_guard'	32.0	rise
<od/freeze_ctrl/GB.LP.NN25fn14	31.8	fall
<od/freeze_ctrl/GB.LP.NN25fn34	31.1	rise
<mod/freeze_ctrl/GB.LP.NN25fn2	30.3	fall
<mod/freeze_ctrl/GB.LP.NN25fn6	29.9	rise
<mod/freeze_ctrl/GB.LP.NN25fn9	28.5	rise
io_mod/freeze_ctrl/ids_freeze	27.4	fall
io_mod/test_ctrl/ids_freeze	27.3	fall
io_mod/test_ctrl/ids_freeze'	26.0	fall
io_mod/test_ctrl/ids_fr_lat	24.9	fall
io_mod/test_ctrl/ids_fr_lat'	24.9	fall
io_mod/test_ctrl/ids_freeze_in	22.6	fall
io_mod/ds_ctrl/ids_freeze_in	22.6	fall
io_mod/ds_ctrl/ids_freeze_in'	22.6	fall
io_mod/ds_ctrl/async_ids_fr	21.2	fall
<d/async_ids_ctrl/async_ids_fr	21.2	fall
</async_ids_ctrl/async_ids_fr'	20.8	fall
<async_ids_ctrl/GB.LP.NN25fn27	20.5	rise
<async_ids_ctrl/GB.LP.NN25fn15	18.8	fall
<async_ids_ctrl/GB.LP.NN25fn18	18.3	rise
<async_ids_ctrl/GB.LP.NN25fn28	17.2	fall
</async_ids_ctrl/GB.LP.NN25fn6	15.6	rise
<async_ids_ctrl/GB.LP.NN25fn12	14.9	fall
io_mod/async_ids_ctrl/ids_sel	14.4	rise
io_mod/ids_sel/ids_sel	14.3	rise
io_mod/ids_sel/ids_sel'	11.6	rise
io_mod/ids_sel/ids_sel_buf	10.7	rise
io_mod/ids_sel/ids_sel_buf'	10.5	rise

io_mod/ids_sel/ids_ph_in	8.7	rise
io_mod/ids_sel/ids_ph_out	8.7	rise
io_mod/ids_sel/ids_ph_out'	8.6	rise
io_mod/ids_sel/PHASE_B	7.0	rise
clk_pad/PHASE_B	6.4	rise
Clk	0.0	fall

Genesil Version v8.0.2 -- Mon Feb 4 12:09:28 1991

Chip: /tmp_mnt/net/yoda/mta/iag/iag/gt_vic/iag Timing Analyzer

OUTPUT DELAY MODE

Fabline: HP2_CN10B Corner: GUARANTEED

Junction Temperature: 67 deg C Voltage: 5.00v

External Clock: Clk

Included setup files:

#0 basic	(Input constraints from other chip>
#1 room	(67 deg C, 5.0 Volts)

Output	OUTPUT DELAYS (ns)				Loading(pf)			
	Ph1(r) Delay		Ph2(r) Delay					
	Min	Max	Min	Max				
ALU_opcode[0]	20.0	21.7	---	---	50.00	PATH		
ALU_opcode[1]	20.1	21.8	---	---	50.00	PATH		
ALU_opcode[2]	19.6	21.4	---	---	50.00	PATH		
ALU_opcode[3]	19.7	21.5	---	---	50.00	PATH		
ALU_opcode[4]	19.8	21.5	---	---	50.00	PATH		
ALU_opcode[5]	19.7	21.5	---	---	50.00	PATH		
ALU_opcode[6]	19.8	21.6	---	---	50.00	PATH		
ALU_opcode[7]	19.8	21.6	---	---	50.00	PATH		
Booting	20.7	22.5	---	---	50.00	PATH		
DAG_R_en	24.0	79.7	28.1	41.6	50.00	PATH		
Dr	31.8	84.2	39.6	42.8	50.00	PATH		
Flush	19.1	42.4	---	---	50.00	PATH		
Freeze	26.0	72.6	27.3	42.9	50.00	PATH		
Guard	28.5	88.2	31.1	49.9	50.00	PATH		
Ids_eq_ods_1	27.3	31.4	---	---	50.00	PATH		
Ids_eq_ods_2	28.2	31.9	---	---	50.00	PATH		
Ids_freeze	19.8	24.2	17.2	34.2	50.00	PATH		
Ids_sel	17.3	22.5	19.6	19.6	50.00	PATH		
Inst[0]	---	---	17.9	22.1	50.00	PATH		
Inst[10]	---	---	19.1	21.7	50.00	PATH		
Inst[11]	---	---	19.0	21.7	50.00	PATH		
Inst[12]	---	---	19.0	21.7	50.00	PATH		
Inst[13]	---	---	18.9	21.7	50.00	PATH		
Inst[14]	---	---	18.7	21.7	50.00	PATH		
Inst[15]	---	---	18.6	21.7	50.00	PATH		
Inst[16]	---	---	18.7	21.7	50.00	PATH		
Inst[17]	---	---	18.8	21.7	50.00	PATH		
Inst[18]	---	---	18.8	21.7	50.00	PATH		
Inst[19]	---	---	18.8	21.7	50.00	PATH		
Inst[1]	---	---	17.9	22.1	50.00	PATH		
Inst[20]	---	---	18.8	21.7	50.00	PATH		

Inst [21]	---	---	18.9	21.7	50.00	PATH
Inst [22]	---	---	19.0	21.7	50.00	PATH
Inst [23]	---	---	19.1	21.7	50.00	PATH
Inst [24]	---	---	18.3	22.0	50.00	PATH
Inst [25]	---	---	18.2	22.0	50.00	PATH
Inst [26]	---	---	18.9	22.0	50.00	PATH
Inst [27]	---	---	18.9	22.0	50.00	PATH
Inst [28]	---	---	19.0	22.0	50.00	PATH
Inst [29]	---	---	19.0	22.0	50.00	PATH
Inst [2]	---	---	18.1	22.1	50.00	PATH
Inst [30]	---	---	19.3	22.0	50.00	PATH
Inst [31]	---	---	19.3	22.0	50.00	PATH
Inst [32]	---	---	19.2	22.2	50.00	PATH
Inst [33]	---	---	19.2	22.3	50.00	PATH
Inst [34]	---	---	19.3	22.3	50.00	PATH
Inst [35]	---	---	19.3	22.3	50.00	PATH
Inst [36]	---	---	19.4	22.3	50.00	PATH
Inst [37]	---	---	19.5	22.3	50.00	PATH
Inst [38]	---	---	19.8	22.3	50.00	PATH
Inst [39]	---	---	19.9	22.3	50.00	PATH
Inst [3]	---	---	18.1	22.1	50.00	PATH
Inst [40]	---	---	19.7	24.7	50.00	PATH
Inst [41]	---	---	20.3	24.8	50.00	PATH
Inst [42]	---	---	19.2	24.2	50.00	PATH
Inst [43]	---	---	19.1	24.2	50.00	PATH
Inst [44]	---	---	18.4	24.3	50.00	PATH
Inst [45]	---	---	18.3	24.3	50.00	PATH
Inst [4]	---	---	19.7	22.1	50.00	PATH
Inst [5]	---	---	19.6	22.0	50.00	PATH
Inst [6]	---	---	19.4	22.0	50.00	PATH
Inst [7]	---	---	19.3	22.0	50.00	PATH
Inst [8]	---	---	19.2	21.7	50.00	PATH
Inst [9]	---	---	19.2	21.7	50.00	PATH
Inst_en	---	---	19.6	19.8	50.00	PATH
Inst_rd	21.0	72.4	---	---	50.00	PATH
Ios	18.1	19.5	---	---	50.00	PATH
Kernel_mode	33.2	40.9	---	---	50.00	PATH
N_cs pha	20.2	20.2	13.3	20.2	50.00	PATH
N_cs phb	19.6	19.6	15.7	20.9	50.00	PATH
N_inst_wr	18.2	18.2	12.4	12.4	50.00	PATH
N_read[1]	18.8	24.1	22.2	23.3	50.00	PATH
N_reset_out	23.1	35.4	---	---	50.00	PATH
N_write[1]	15.8	37.1	18.5	27.6	50.00	PATH
Ncs[1]	14.7	21.8	17.4	20.4	50.00	PATH
Ncs[2]	15.6	22.7	18.1	21.1	50.00	PATH
Ncs[3]	15.9	23.0	18.5	21.4	50.00	PATH
Ods_freeze	20.5	64.2	23.2	24.7	50.00	PATH
Ods_ids[0]	24.0	76.2	27.6	33.6	50.00	PATH
Ods_ids[1]	23.7	75.9	27.3	33.3	50.00	PATH
Ods_ids[2]	23.9	76.2	27.5	33.5	50.00	PATH
Ods_ids[3]	23.9	76.2	27.5	33.5	50.00	PATH
Ods_sel	17.7	24.1	23.1	23.1	50.00	PATH
Pc[0]	---	---	13.7	17.2	50.00	PATH
Pc[10]	---	---	13.4	16.9	50.00	PATH

Pc[11]	---	---	13.4	16.9	50.00	PATH
Pc[12]	---	---	13.3	16.8	50.00	PATH
Pc[13]	---	---	13.3	16.8	50.00	PATH
Pc[14]	---	---	13.5	17.0	50.00	PATH
Pc[15]	---	---	13.6	17.1	50.00	PATH
Pc[16]	---	---	13.6	17.1	50.00	PATH
Pc[17]	---	---	13.7	17.2	50.00	PATH
Pc[18]	---	---	13.7	17.2	50.00	PATH
Pc[19]	---	---	13.7	17.2	50.00	PATH
Pc[1]	---	---	13.7	17.2	50.00	PATH
Pc[20]	---	---	13.8	17.3	50.00	PATH
Pc[21]	---	---	13.9	17.4	50.00	PATH
Pc[22]	---	---	13.9	17.4	50.00	PATH
Pc[23]	---	---	13.9	17.4	50.00	PATH
Pc[24]	---	---	13.9	17.4	50.00	PATH
Pc[25]	---	---	13.9	17.4	50.00	PATH
Pc[2]	---	---	13.7	17.2	50.00	PATH
Pc[3]	---	---	13.7	17.2	50.00	PATH
Pc[4]	---	---	13.7	17.2	50.00	PATH
Pc[5]	---	---	13.7	17.2	50.00	PATH
Pc[6]	---	---	13.7	17.1	50.00	PATH
Pc[7]	---	---	13.6	17.1	50.00	PATH
Pc[8]	---	---	13.6	17.1	50.00	PATH
Pc[9]	---	---	13.6	17.1	50.00	PATH
RF[0]	22.8	109.9	25.5	39.7	50.00	PATH
RF[10]	21.6	109.1	26.9	47.1	50.00	PATH
RF[11]	21.4	109.0	26.9	42.0	50.00	PATH
RF[12]	21.4	108.9	26.9	40.1	50.00	PATH
RF[13]	21.3	108.9	26.9	40.1	50.00	PATH
RF[14]	21.0	108.9	26.9	40.7	50.00	PATH
RF[15]	21.5	109.3	26.9	40.2	50.00	PATH
RF[16]	21.8	109.5	25.0	65.4	50.00	PATH
RF[17]	21.6	109.4	25.0	43.7	50.00	PATH
RF[18]	21.1	109.0	25.0	46.2	50.00	PATH
RF[19]	21.4	109.3	25.0	43.9	50.00	PATH
RF[1]	22.7	109.8	25.5	39.6	50.00	PATH
RF[20]	22.4	110.1	25.0	39.5	50.00	PATH
RF[21]	21.6	109.4	25.0	38.9	50.00	PATH
RF[22]	21.2	109.2	25.0	63.2	50.00	PATH
RF[23]	20.7	108.9	25.1	38.4	50.00	PATH
RF[24]	20.2	108.5	27.1	40.4	50.00	PATH
RF[25]	20.5	108.8	27.1	42.1	50.00	PATH
RF[26]	19.8	78.4	27.1	40.3	50.00	PATH
RF[27]	19.7	78.4	27.1	40.3	50.00	PATH
RF[28]	19.3	78.4	27.0	40.3	50.00	PATH
RF[29]	19.2	78.3	27.0	40.3	50.00	PATH
RF[2]	22.7	109.7	25.5	39.6	50.00	PATH
RF[30]	19.1	78.3	27.0	40.3	50.00	PATH
RF[31]	19.0	78.3	27.0	40.3	50.00	PATH
RF[3]	22.6	109.6	25.6	39.5	50.00	PATH
RF[4]	22.4	109.5	25.6	39.4	50.00	PATH
RF[5]	22.3	109.5	25.6	39.3	50.00	PATH
RF[6]	22.3	109.4	25.6	39.3	50.00	PATH
RF[7]	22.2	109.4	25.6	39.2	50.00	PATH

RF[8]	21.8	109.2	26.8	46.4	50.00	PATH
RF[9]	21.9	109.3	26.8	43.7	50.00	PATH
Read[2]	27.5	32.6	27.7	31.6	50.00	PATH
Read[3]	31.6	36.8	31.4	35.7	50.00	PATH
Valid_intr_pulse	27.4	50.2	---	---	50.00	PATH
Write[2]	17.1	37.6	20.3	21.5	50.00	PATH
Write[3]	17.2	37.6	20.4	21.6	50.00	PATH

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Chip: /tmp_mnt/net/yoda/mta/iag/iag/gt_vic/iag

Timing Analyzer

SETUP AND HOLD MODE

Fabline: HP2_CN10B

Corner: GUARANTEED

Junction Temperature: 67 deg C

Voltage: 5.00v

External Clock: Clk

Included setup files:

#0 basic

(Input constraints from other chip>

#1 room

(67 deg C, 5.0 Volts)

INPUT SETUP AND HOLD TIMES (ns)

Input	Setup Time		Hold Time		
	Ph1(f)	Ph2(f)	Ph1(f)	Ph2(f)	
ALU_Flag	34.5	3.7	0.6	-2.5	PATH
Carry	34.0	3.7	0.6	-2.6	PATH
DAG_error	---	9.7	---	-4.2	PATH
DAV[1]	---	62.3	---	-10.0	PATH
DAV[2]	---	62.9	---	-9.9	PATH
DAV[3]	---	63.2	---	-10.4	PATH
Dr	31.0	65.8	-3.6	-2.6	PATH
IAG_test[0]	---	58.4	---	0.2	PATH
IAG_test[1]	---	58.3	---	0.1	PATH
Inst[0]	---	4.8	---	-2.6	PATH
Inst[10]	---	6.2	---	-3.5	PATH
Inst[11]	---	6.0	---	-3.5	PATH
Inst[12]	---	4.0	---	-2.4	PATH
Inst[13]	---	3.8	---	-2.2	PATH
Inst[14]	---	3.5	---	-1.9	PATH
Inst[15]	---	3.5	---	-1.8	PATH
Inst[16]	---	3.5	---	-1.9	PATH
Inst[17]	---	3.5	---	-1.9	PATH
Inst[18]	---	3.6	---	-2.0	PATH
Inst[19]	---	3.7	---	-2.1	PATH
Inst[1]	---	5.0	---	-2.7	PATH
Inst[20]	---	3.7	---	-2.1	PATH
Inst[21]	---	3.8	---	-2.2	PATH
Inst[22]	---	3.7	---	-2.1	PATH
Inst[23]	---	3.4	---	-1.8	PATH
Inst[24]	---	3.3	---	-1.7	PATH
Inst[25]	---	3.3	---	-1.7	PATH
Inst[26]	---	5.9	---	-2.9	PATH
Inst[27]	---	6.2	---	-3.0	PATH
Inst[28]	---	6.9	---	-3.4	PATH
Inst[29]	---	6.3	---	-3.4	PATH

Inst[2]	---	6.1	---	-3.9	PATH
Inst[30]	---	3.3	---	-1.8	PATH
Inst[31]	---	3.6	---	-2.2	PATH
Inst[32]	---	3.3	---	-1.8	PATH
Inst[33]	---	3.3	---	-1.8	PATH
Inst[34]	---	3.3	---	-1.8	PATH
Inst[35]	---	3.3	---	-1.8	PATH
Inst[36]	---	3.3	---	-1.8	PATH
Inst[37]	---	4.6	---	-3.2	PATH
Inst[38]	---	6.5	---	-2.8	PATH
Inst[39]	---	6.6	---	-3.0	PATH
Inst[3]	---	6.3	---	-3.9	PATH
Inst[40]	---	6.8	---	-3.1	PATH
Inst[41]	---	6.5	---	-3.1	PATH
Inst[42]	---	8.3	---	-4.6	PATH
Inst[43]	---	8.2	---	-4.5	PATH
Inst[44]	---	8.0	---	-4.2	PATH
Inst[45]	---	7.9	---	-4.2	PATH
Inst[4]	---	6.6	---	-3.9	PATH
Inst[5]	---	5.9	---	-3.8	PATH
Inst[6]	---	6.7	---	-3.8	PATH
Inst[7]	---	5.9	---	-3.7	PATH
Inst[8]	---	6.1	---	-3.5	PATH
Inst[9]	---	5.9	---	-3.5	PATH
Inst_rdy	---	21.6	---	0.8	PATH
Intr[0]	---	8.1	---	-6.1	PATH
Intr[1]	---	8.1	---	-6.1	PATH
Intr[2]	---	8.2	---	-6.2	PATH
Intr[3]	---	8.2	---	-6.2	PATH
Intr[4]	---	8.2	---	-6.2	PATH
Intr[5]	---	8.3	---	-6.3	PATH
Intr[6]	---	8.4	---	-6.3	PATH
Intr[7]	---	8.4	---	-6.4	PATH
Intr[8]	---	7.6	---	-5.6	PATH
N_reset	-3.7	---	5.5	---	PATH
Pixel_clk	32.2	67.5	-14.9	-1.4	PATH
RFI[1]	29.4	---	-1.2	---	PATH
RFI[2]	29.3	---	-1.3	---	PATH
RFI[3]	29.3	---	-1.0	---	PATH
RF[0]	1.1	2.2	-0.2	0.5	PATH
RF[10]	1.2	2.3	-0.3	0.3	PATH
RF[11]	1.2	2.3	-0.3	0.4	PATH
RF[12]	1.1	2.2	-0.2	0.4	PATH
RF[13]	1.5	2.6	-0.7	0.0	PATH
RF[14]	1.0	2.1	-0.1	0.6	PATH
RF[15]	1.0	2.1	-0.1	0.6	PATH
RF[16]	1.2	2.2	-0.3	0.4	PATH
RF[17]	1.1	2.2	-0.2	0.4	PATH
RF[18]	0.9	1.9	0.1	0.7	PATH
RF[19]	1.1	2.1	-0.2	0.5	PATH
RF[1]	2.6	3.7	-1.8	-1.1	PATH
RF[20]	0.8	1.9	0.1	0.8	PATH
RF[21]	0.9	2.0	0.0	0.7	PATH
RF[22]	1.1	2.2	-0.2	0.5	PATH

RF[23]	1.3	2.4	-0.5	0.3	PATH
RF[24]	1.4	2.4	-0.5	0.2	PATH
RF[25]	1.7	2.8	-0.9	-0.1	PATH
RF[26]	---	-0.5	---	1.4	PATH
RF[27]	---	-0.5	---	1.5	PATH
RF[28]	---	-0.8	---	1.7	PATH
RF[29]	---	-0.8	---	1.8	PATH
RF[2]	1.2	2.2	-0.2	0.5	PATH
RF[30]	---	-0.9	---	1.8	PATH
RF[31]	---	-1.0	---	1.9	PATH
RF[3]	1.2	2.2	-0.2	0.5	PATH
RF[4]	1.2	2.3	-0.2	0.4	PATH
RF[5]	2.5	3.6	-1.7	-1.0	PATH
RF[6]	1.2	2.3	-0.3	0.4	PATH
RF[7]	1.2	2.3	-0.3	0.4	PATH
RF[8]	1.2	2.3	-0.3	0.4	PATH
RF[9]	1.7	2.8	-0.9	-0.2	PATH
R_eq_f_1	---	50.4	---	-5.1	PATH
R_eq_f_2	---	4.6	---	-1.7	PATH
S_eq_f_1	---	4.2	---	-3.1	PATH
S_eq_f_2	---	4.3	---	-3.2	PATH
Sign	34.6	3.6	0.7	-2.4	PATH
Status[0]	22.9	---	-2.8	---	PATH
Status[1]	22.8	---	-2.8	---	PATH
Status[2]	25.1	---	-4.9	---	PATH
Status[3]	22.3	---	-2.1	---	PATH
Status[4]	21.8	---	-2.1	---	PATH
Zero	34.1	3.6	0.8	-2.4	PATH

Genesil Version v8.0.2 -- Mon Feb 4 12:14:13 1991

Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/iag

Timing Analyzer

PATH DELAY MODE

Fabline: HP2_CN10B

Corner: GUARANTEED

Junction Temperature: 67 deg C

Voltage: 5.00v

External Clock: Clk

Included setup files:

#0 basic

(Input constraints from other chip>

#1 room

(67 deg C, 5.0 Volts)

PATH DELAY (ns)

Source Object	Connector	(Ph1) Min	Max	
Dest. Object	Connector	(Ph2) Min	Max	
clk_pad_____	PHASE_A_____	7.7	17.5	
io_mod/sell_____	ods_en_____	15.1	18.6	PATH
io_mod/sell_____	ods_en_____	---	---	
*CURRENT*_____	Ncs[1]_____	---	---	PATH
clk_pad_____	PHASE_A_____	7.2	7.7	

io_mod/sell_____	ods_inst[3]_____	---	---	PATH
io_mod/sell_____	ods_inst[3]_____	---	---	
*CURRENT*_____	Ncs[1]_____	---	---	PATH
clk_pad_____	PHASE_A_____	7.7	17.5	
io_mod/sell_____	ods_en_____	15.1	18.6	PATH
io_mod/sell_____	ods_en_____	12.0	12.8	
*CURRENT*_____	N_write[1]_____	---	---	PATH
clk_pad_____	PHASE_A_____	7.2	7.7	
io_mod/sell_____	ods_inst[3]_____	---	---	PATH
io_mod/sell_____	ods_inst[3]_____	---	---	
*CURRENT*_____	N_write[1]_____	---	---	PATH
io_mod/io_dp_____	ods_en_____	12.5	14.0	
*CURRENT*_____	Ods_ids[2]_____	12.5	14.0	PATH
io_mod/io_dp_____	ids_sel_____	13.0	15.7	
*CURRENT*_____	Ods_ids[2]_____	13.0	15.7	PATH
io_mod/io_dp_____	dff1_VAL1[2]_____	13.7	15.2	
*CURRENT*_____	Ods_ids[2]_____	13.7	15.2	PATH
> _____	_____			

Genesil Version v8.0.2 -- Mon Feb 4 12:14:17 1991

Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/iag Timing Analyzer

NODE DELAY MODE

Fabline: HP2_CN10B

Corner: GUARANTEED

Junction Temperature: 67 deg C

Voltage: 5.00v

External Clock: Clk

Included setup files:

#0 basic

(Input constraints from other chip>

#1 room

(67 deg C, 5.0 Volts)

NODE DELAYS (ns)

Object	Connector	Ph1(r) Delay	Ph2(r) Delay
		Min Max	Min Max

```

io_mod/io_dp__ ods_en_____ 14.5  24.3   17.5  21.0 PATH
io_mod/io_dp__ ids_sel_____ 10.7  15.9   14.5  14.5 PATH
io_mod/io_dp__ dff1_VAL1[2]_ 10.2  10.7   ---   ---  PATH
>
*****
Genesil Versior v8.0.2 -- Mon Feb  4 12:14:29 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/iag          Timing Analyzer
*****
VIOLATION MODE
-----
Fabline: HP2_CN10B                      Corner: GUARANTEED
Junction Temperature:67 deg C           Voltage:5.00v
External Clock: Clk
Included setup files:
#0 basic                               (Input constraints from other chip>
#1 room                               (67 deg C, 5.0 Volts)
-----
NO VIOLATIONS
Hold time check margin: 2.0ns

```

13.3. GUARANTEED, Max T, Min V

```

*****
Genesil Version v8.0.2 -- Mon Feb  4 12:15:26 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/iag          Timing Analyzer
*****
CLOCK REPORT MODE
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Fabline: HP2_CN10B                      Corner: GUARANTEED
Junction Temperature:117 deg C           Voltage:4.50v
External Clock: Clk
Included setup files:
#0 basic                               (Input constraints from other chip>
#1 worst                               (117 deg C, 4.5 Volts)
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CLOCK TIMES (minimum)
Phase 1 High:    91.9   ns           Phase 2 High:    85.8   ns
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Cycle (from Ph1): 152.0   ns           Cycle (from Ph2): 178.5   ns
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Minimum Cycle Time: 178.5   ns           Symmetric Cycle Time: 183.8   ns
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CLOCK WORST CASE PATHS
Minimum Phase 1 high time is  91.9   ns set by:
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** Clock delay: 5.6ns (97.5-91.9)
Node                               Cumulative Delay      Transition
<c_ndp_mod/pc_latch/(internal)     97.5                   fall

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<od/pc_ndp_mod/pc_latch/IN[23]	96.3	rise
<d/pc_ndp_mod/pc_unlat/OUT[23]	96.3	rise
</pc_ndp_mod/pc_unlat/OUT[23]'	96.1	rise
<od/pc_ndp_mod/pc_unlat/IN[23]	95.7	fall
<pc_ndp_mod/n_pc_unlat/OUT[23]	95.7	fall
<c_ndp_mod/n_pc_unlat/OUT[23]'	95.7	fall
<pc_ndp_mod/n_pc_unlat/IN1[23]	95.0	rise
<_mod/pc_ndp_mod/ready/OUT[23]	95.0	rise
<mod/pc_ndp_mod/ready/OUT[23]'	94.8	rise
<n_mod/pc_ndp_mod/ready/IN[23]	94.5	fall
<od/pc_ndp_mod/n_ready/OUT[23]	94.5	fall
<d/pc_ndp_mod/n_ready/OUT[23]'	94.4	fall
<od/pc_ndp_mod/n_ready/IN1[23]	93.7	rise
<_mod/pc_ndp_mod/alpha/OUT[23]	93.7	rise
<mod/pc_ndp_mod/alpha/OUT[23]'	93.5	rise
<n_mod/pc_ndp_mod/alpha/IN[23]	93.2	fall
<od/pc_ndp_mod/n_alpha/OUT[23]	93.2	fall
<d/pc_ndp_mod/n_alpha/OUT[23]'	93.1	fall
<od/pc_ndp_mod/n_alpha/IN1[23]	92.4	rise
<mod/pc_ndp_mod/br_adr/OUT[23]	92.4	rise
<od/pc_ndp_mod/br_adr/OUT[23]'	83.7	rise
<_mod/pc_ndp_mod/br_adr/IN[23]	83.3	fall
<d/pc_ndp_mod/n_br_adr/OUT[23]	83.3	fall
</pc_ndp_mod/n_br_adr/OUT[23]'	83.2	fall
<d/pc_ndp_mod/n_br_adr/IN2[23]	82.5	rise
<d/pc_ndp_mod/absolute/OUT[23]	82.5	rise
</pc_ndp_mod/absolute/OUT[23]'	81.8	rise
<od/pc_ndp_mod/absolute/IN[23]	81.5	fall
<pc_ndp_mod/n_absolute/OUT[23]	81.5	fall
<c_ndp_mod/n_absolute/OUT[23]'	81.4	fall
<pc_ndp_mod/n_absolute/IN2[23]	80.7	rise
intr_mod/ram/intr_vect[23]	80.7	rise
intr_mod/ram/intr_vect[23]'	79.9	rise
intr_mod/ram/st_vect_adr[2]	61.5	rise
<intr_vect_ctrl/st_vect_adr[2]	61.5	rise
<ntr_vect_ctrl/st_vect_adr[2]'	55.5	rise
</intr_vect_ctrl/GB.LP.NNZ5fN2	55.0	fall
<tr_vect_ctrl/valid_intr_pulse	54.4	rise
<r_mod/valid_intr_ctrl/vip_out	52.6	rise
<_mod/valid_intr_ctrl/vip_out'	43.1	rise
<alid_intr_ctrl/GB.LP.NNZ5fN21	42.8	fall
<alid_intr_ctrl/GB.LP.NNZ5fN11	41.1	rise
<valid_intr_ctrl/GB.LP.NNZ5fN7	39.9	fall
<valid_intr_ctrl/GB.LP.NNZ5fN0	39.4	rise
<valid_intr_ctrl/GB.LP.NNZ5fN6	37.7	fall
<valid_intr_ctrl/GB.LP.NNZ5fN3	37.2	rise
<od/valid_intr_ctrl/rd_wr_intr	36.2	fall
inst_mod/rd_wr_inst/rd_wr_intr	35.0	fall
<st_mod/rd_wr_inst/rd_wr_intr'	31.3	fall
inst_mod/rd_wr_inst/read_write	29.9	fall
<t_mod/rd_wr_inst/pc_min_op[1]	27.1	rise
<t_mod/inst_in_dp/pc_min_op[1]	26.7	rise
<_mod/inst_in_dp/pc_min_op[1]'	15.3	rise
<st_mod/inst_in_dp/dff_VAL2[1]	13.9	rise

inst_mod/inst_in_dp/PHASE_A	9.5	rise
clk_pad/PHASE_A	8.5	rise
Clk	0.0	rise

Minimum Phase 2 high time is 85.8 ns set by:

 ** Clock delay: 5.5ns (91.4-85.8)

Node	Cumulative Delay	Transition
<atus_mod/status_dp/(internal)	91.4	fall
<_mod/status_dp/INTER3_ST1[20]	89.9	rise
<mod/status_dp/intr_status[20]	87.6	rise
</priority_pla/req_intr_adr[3]	87.1	rise
<priority_pla/req_intr_adr[3]'	73.9	rise
<d/priority_pla/GB.LP.NNZ5fn36	72.6	rise
<d/priority_pla/GB.LP.NNZ5fn47	71.4	fall
<d/priority_pla/GB.LP.NNZ5fn51	71.0	rise
<d/priority_pla/GB.LP.NNZ5fn40	69.4	fall
<d/priority_pla/GB.LP.NNZ5fn12	68.7	rise
<d/priority_pla/GB.LP.NNZ5fn14	66.2	rise
</priority_pla/current_intr[4]	62.7	fall
<r_mod/intr_dp/current_intr[4]	62.6	fall
<_mod/intr_dp/current_intr[4]'	62.6	fall
<r_mod/intr_dp/phb_lat_VAL1[4]	61.0	fall
intr_mod/intr_dp/guarded_ei	52.5	rise
intr_mod/ld_ctrl/guarded_ei	52.5	rise
intr_mod/ld_ctrl/guarded_ei'	50.7	rise
intr_mod/ld_ctrl/n_guard	49.5	rise
io_mod/ids_sel/n_guard_out	47.7	rise
io_mod/ids_sel/n_guard_out'	42.0	rise
io_mod/ids_sel/n_guard	41.0	rise
io_mod/freeze_ctrl/n_guard	40.9	rise
io_mod/freeze_ctrl/n_guard'	39.6	rise
<od/freeze_ctrl/GB.LP.NNZ5fn14	39.3	fall
<od/freeze_ctrl/GB.LP.NNZ5fn34	38.6	rise
<mod/freeze_ctrl/GB.LP.NNZ5fn2	37.5	fall
<mod/freeze_ctrl/GB.LP.NNZ5fn6	37.0	rise
<mod/freeze_ctrl/GB.LP.NNZ5fn9	35.3	rise
io_mod/freeze_ctrl/ids_freeze	33.9	fall
io_mod/test_ctrl/ids_freeze	33.8	fall
io_mod/test_ctrl/ids_freeze'	32.2	fall
io_mod/test_ctrl/ids_fr_lat	30.9	fall
io_mod/test_ctrl/ids_fr_lat'	30.8	fall
io_mod/test_ctrl/ids_freeze_in	28.0	fall
io_mod/ds_ctrl/ids_freeze_in	28.0	fall
io_mod/ds_ctrl/ids_freeze_in'	28.0	fall
io_mod/ds_ctrl/async_ids_fr	26.2	fall
<d/async_ids_ctrl/async_ids_fr	26.2	fall
</async_ids_ctrl/async_ids_fr'	25.8	fall
<async_ids_ctrl/GB.LP.NNZ5fn27	25.4	rise
<async_ids_ctrl/GB.LP.NNZ5fn15	23.3	fall
<async_ids_ctrl/GB.LP.NNZ5fn18	22.7	rise
<async_ids_ctrl/GB.LP.NNZ5fn28	21.2	fall
</async_ids_ctrl/GB.LP.NNZ5fn6	19.4	rise
<async_ids_ctrl/GB.LP.NNZ5fn12	18.4	fall

io_mod/async_ids_ctrl/ids_sel	17.9	rise
io_mod/ids_sel/ids_sel	17.7	rise
io_mod/ids_sel/ids_sel'	14.3	rise
io_mod/ids_sel/ids_sel_buf	13.3	rise
io_mod/ids_sel/ids_sel_buf'	13.0	rise
io_mod/ids_sel/ids_ph_in	10.8	rise
io_mod/ids_sel/ids_ph_out	10.8	rise
io_mod/ids_sel/ids_ph_out'	10.7	rise
io_mod/ids_sel/PHASE_B	8.7	rise
clk_pad/PHASE_B	8.0	rise
Clk	0.0	fall

Minimum cycle time (from Ph1) is 152.0 ns set by:

 ** Clock delay: 5.5ns (157.5-152.0)

Node	Cumulative Delay	Transition
<atus_mod/status_dp/(internal)	157.5	fall
status_mod/status_dp/389	156.5	fall
<_mod/status_dp/INTER3_ST1[20]	156.0	rise
<mod/status_dp/intr_status[20]	153.8	rise
</priority_pla/req_intr_adr[3]	153.3	rise
<priority_pla/req_intr_adr[3]'	140.1	rise
<d/priority_pla/GB.LP.NN25fN36	138.8	rise
<d/priority_pla/GB.LP.NN25fN47	137.6	fall
<d/priority_pla/GB.LP.NN25fN51	137.1	rise
<d/priority_pla/GB.LP.NN25fN40	135.6	fall
<d/priority_pla/GB.LP.NN25fN12	134.9	rise
<d/priority_pla/GB.LP.NN25fN14	132.4	rise
</priority_pla/current_intr[4]	128.8	fall
<r_mod/intr_dp/current_intr[4]	128.8	fall
<_mod/intr_dp/current_intr[4]'	128.7	fall
<r_mod/intr_dp/phb_lat_VAL1[4]	127.2	fall
intr_mod/intr_dp/guarded_ei	118.7	rise
intr_mod/ld_ctrl/guarded_ei	118.7	rise
intr_mod/ld_ctrl/guarded_ei'	116.9	rise
intr_mod/ld_ctrl/n_guard	115.7	rise
io_mod/ids_sel/n_guard_out	113.9	rise
io_mod/ids_sel/n_guard_out'	108.2	rise
io_mod/ids_sel/n_guard	107.1	rise
io_mod/freeze_ctrl/n_guard	107.1	rise
io_mod/freeze_ctrl/n_guard'	105.8	rise
<od/freeze_ctrl/GB.LP.NN25fN14	105.5	fall
<od/freeze_ctrl/GB.LP.NN25fN34	104.7	rise
<mod/freeze_ctrl/GB.LP.NN25fN2	103.7	fall
<mod/freeze_ctrl/GB.LP.NN25fN6	103.2	rise
<mod/freeze_ctrl/GB.LP.NN25fN9	101.5	rise
io_mod/freeze_ctrl/ids_freeze	100.1	fall
io_mod/test_ctrl/ids_freeze	100.0	fall
io_mod/test_ctrl/ids_freeze'	98.4	fall
io_mod/test_ctrl/ids_fr_lat	97.0	fall
io_mod/test_ctrl/ids_fr_lat'	97.0	fall
io_mod/test_ctrl/ids_freeze_in	94.2	fall
io_mod/ds_ctrl/ids_freeze_in	94.2	fall
io_mod/ds_ctrl/ids_freeze_in'	94.1	fall

io_mod/ds_ctrl/async_ids_fr	92.4	fall
<d/async_ids_ctrl/async_ids_fr	92.4	fall
</async_ids_ctrl/async_ids_fr'	91.9	fall
<async_ids_ctrl/GB.LP.NN25fN27	91.6	rise
<async_ids_ctrl/GB.LP.NN25fN15	89.4	fall
<async_ids_ctrl/GB.LP.NN25fN18	88.9	rise
<async_ids_ctrl/GB.LP.NN25fN28	87.4	fall
</async_ids_ctrl/GB.LP.NN25fN6	85.6	rise
<async_ids_ctrl/GB.LP.NN25fN12	84.6	fall
io_mod/async_ids_ctrl/ids_sel	84.1	rise
io_mod/ids_sel/ids_sel	83.9	rise
io_mod/ids_sel/ids_sel'	80.5	rise
io_mod/ids_sel/ids_sel_buf	79.4	rise
io_mod/ids_sel/ids_sel_buf'	79.2	rise
io_mod/ids_sel/ids_ph_in	77.0	rise
io_mod/ids_sel/ids_ph_out	77.0	rise
io_mod/ids_sel/ids_ph_out'	76.9	rise
*io_mod/ids_sel/(internal)	75.0	fall
io_mod/ids_sel/n_ods_freeze	72.1	rise
io_mod/ids_sel/ods_freeze	71.3	fall
io_mod/test_ctrl/ods_freeze	71.3	fall
io_mod/test_ctrl/ods_freeze'	66.8	fall
io_mod/test_ctrl/ods_fr_lat	65.5	fall
io_mod/test_ctrl/ods_freeze_in	62.7	fall
io_mod/ds_ctrl/ods_freeze_in	62.7	fall
io_mod/ds_ctrl/ods_freeze_in'	62.0	fall
io_mod/ds_ctrl/async_ods_fr	60.2	fall
<d/async_ods_ctrl/async_ods_fr	60.2	fall
</async_ods_ctrl/async_ods_fr'	59.9	fall
<async_ods_ctrl/GB.LP.NN25fN30	59.5	rise
</async_ods_ctrl/GB.LP.NN25fN1	56.6	fall
<ync_ods_ctrl/valid_intr_pulse	56.1	rise
<_mod/ids_sel/valid_intr_pulse	56.1	rise
<mod/ids_sel/valid_intr_pulse'	54.9	rise
io_mod/ids_sel/vip_in	53.8	rise
<r_mod/valid_intr_ctrl/vip_out	52.6	rise
<_mod/valid_intr_ctrl/vip_out'	43.1	rise
<alid_intr_ctrl/GB.LP.NN25fN21	42.8	fall
<alid_intr_ctrl/GB.LP.NN25fN11	41.1	rise
<valid_intr_ctrl/GB.LP.NN25fN7	39.9	fall
<valid_intr_ctrl/GB.LP.NN25fN0	39.4	rise
<valid_intr_ctrl/GB.LP.NN25fN6	37.7	fall
<valid_intr_ctrl/GB.LP.NN25fN3	37.2	rise
<od/valid_intr_ctrl/rd_wr_intr	36.2	fall
inst_mod/rd_wr_inst/rd_wr_intr	35.0	fall
<st_mod/rd_wr_inst/rd_wr_intr'	31.3	fall
inst_mod/rd_wr_inst/read_write	29.9	fall
<t_mod/rd_wr_inst/pc_min_op[1]	27.1	rise
<t_mod/inst_in_dp/pc_min_op[1]	26.7	rise
<_mod/inst_in_dp/pc_min_op[1]'	15.3	rise
<st_mod/inst_in_dp/dff_VAL2[1]	13.9	rise
inst_mod/inst_in_dp/PHASE_A	9.5	rise
clk_pad/PHASE_A	8.5	rise
Clk	0.0	rise

Minimum cycle time (from Ph2) is 178.5 ns set by:

 ** Clock delay: 9.3ns (187.8-178.5)

Node	Cumulative Delay	Transition
<_gen_mod/stk_pc_dp/(internal)	187.8	fall
<gen_mod/stk_pc_dp/next_pc[24]	187.4	rise
<_ndp_mod/next_pc_buff/OUT[24]	187.2	rise
<ndp_mod/next_pc_buff/OUT[24]'	178.4	rise
<c_ndp_mod/next_pc_buff/IN[24]	177.0	rise
<ndp_mod/next_pc_adder/OUT[24]	177.0	rise
<dp_mod/next_pc_adder/OUT[24]'	176.9	rise
<_ndp_mod/next_pc_adder/IN1[1]	164.7	rise
<mod/pc_ndp_mod/pc_buff/OUT[1]	164.7	rise
<od/pc_ndp_mod/pc_buff/OUT[1]'	154.2	rise
<_mod/pc_ndp_mod/pc_buff/IN[1]	153.1	rise
<od/pc_ndp_mod/pc_latch/OUT[1]	153.1	rise
<d/pc_ndp_mod/pc_latch/OUT[1]'	152.8	rise
<mod/pc_ndp_mod/pc_latch/IN[1]	151.1	rise
<od/pc_ndp_mod/pc_unlat/OUT[1]	151.1	rise
<d/pc_ndp_mod/pc_unlat/OUT[1]'	151.0	rise
<mod/pc_ndp_mod/pc_unlat/IN[1]	150.6	fall
</pc_ndp_mod/n_pc_unlat/OUT[1]	150.6	fall
<pc_ndp_mod/n_pc_unlat/OUT[1]'	150.5	fall
</pc_ndp_mod/n_pc_unlat/IN1[1]	149.8	rise
<n_mod/pc_ndp_mod/ready/OUT[1]	149.8	rise
<_mod/pc_ndp_mod/ready/OUT[1]'	149.7	rise
<en_mod/pc_ndp_mod/ready/IN[1]	149.3	fall
<mod/pc_ndp_mod/n_ready/OUT[1]	149.3	fall
<od/pc_ndp_mod/n_ready/OUT[1]'	149.2	fall
<mod/pc_ndp_mod/n_ready/IN1[1]	148.5	rise
<n_mod/pc_ndp_mod/alpha/OUT[1]	148.5	rise
<_mod/pc_ndp_mod/alpha/OUT[1]'	148.4	rise
<en_mod/pc_ndp_mod/alpha/IN[1]	148.0	fall
<mod/pc_ndp_mod/n_alpha/OUT[1]	148.0	fall
<od/pc_ndp_mod/n_alpha/OUT[1]'	147.9	fall
<mod/pc_ndp_mod/n_alpha/IN1[1]	147.2	rise
<_mod/pc_ndp_mod/br_adr/OUT[1]	147.2	rise
<mod/pc_ndp_mod/br_adr/OUT[1]'	139.4	rise
<n_mod/pc_ndp_mod/br_adr/IN[1]	139.0	fall
<od/pc_ndp_mod/n_br_adr/OUT[1]	139.0	fall
<d/pc_ndp_mod/n_br_adr/OUT[1]'	139.0	fall
<od/pc_ndp_mod/n_br_adr/IN1[1]	138.3	rise
<_gen_mod/pc_ndp_mod/x1/OUT[1]	138.3	rise
<gen_mod/pc_ndp_mod/x1/OUT[1]'	138.1	rise
pc_gen_mod/pc_ndp_mod/x1/IN[1]	137.7	fall
<en_mod/pc_ndp_mod/n_x1/OUT[1]	137.7	fall
<n_mod/pc_ndp_mod/n_x1/OUT[1]'	137.7	fall
<en_mod/pc_ndp_mod/n_x1/SEL[0]	135.3	rise
pc_gen_mod/flush_ctrl/dis_tp	134.6	rise
pc_gen_mod/flush_ctrl/dis_tp'	131.4	rise
<_mod/flush_ctrl/GB.LP.NNZ5fN5	131.0	fall
<mod/flush_ctrl/GB.LP.NNZ5fN10	130.1	rise
<mod/flush_ctrl/GB.LP.NNZ5fN20	129.4	fall
<mod/flush_ctrl/GB.LP.NNZ5fN12	128.9	rise

pc_gen_mod/flush_ctrl/rs	127.8	fall
task_ptr_mod/task_ptr_ctrl/rs	126.9	fall
task_ptr_mod/task_ptr_ctrl/rs'	125.3	fall
<_ptr_mod/task_ptr_ctrl/rs_out	124.2	fall
task_ptr_mod/tp_en_dec/rs_out	124.2	fall
task_ptr_mod/tp_en_dec/rs_out'	122.8	fall
<r_mod/tp_en_dec/GB.LP.NNZ5fN3	122.3	rise
<n_dec/GB.LP.NNin2Z2eINZ5b0Z5d	121.5	fall
<od/tp_en_dec/valid_intr_pulse	121.1	rise
<r_mod/valid_intr_ctrl/vip_out	118.0	rise
<_mod/valid_intr_ctrl/vip_out'	108.5	rise
<alid_intr_ctrl/GB.LP.NNZ5fN21	108.2	fall
<alid_intr_ctrl/GB.LP.NNZ5fN11	106.5	rise
<valid_intr_ctrl/GB.LP.NNZ5fN7	105.3	fall
<valid_intr_ctrl/GB.LP.NNZ5fN0	104.7	rise
<valid_intr_ctrl/GB.LP.NNZ5fN6	103.1	fall
<valid_intr_ctrl/GB.LP.NNZ5fN3	102.5	rise
<alid_intr_ctrl/GB.LP.NNZ5fN10	100.5	rise
<P.NNnpassintZ2eoutZ5fxZ5b0Z5d	98.6	fall
*</valid_intr_ctrl/n_pass_intr	95.5	fall
<_mod/pass_intr_dp/n_pass_intr	95.5	fall
<mod/pass_intr_dp/n_pass_intr'	95.0	fall
</pass_intr_dp/req_intr_adr[0]	86.9	rise
</priority_pla/req_intr_adr[0]	86.8	rise
<priority_pla/req_intr_adr[0]'	73.6	rise
<od/priority_pla/GB.LP.NNZ5fN1	73.2	fall
<d/priority_pla/GB.LP.NNZ5fN36	72.6	rise
<d/priority_pla/GB.LP.NNZ5fN47	71.4	fall
<d/priority_pla/GB.LP.NNZ5fN51	71.0	rise
<d/priority_pla/GB.LP.NNZ5fN40	69.4	fall
<d/priority_pla/GB.LP.NNZ5fN12	68.7	rise
<d/priority_pla/GB.LP.NNZ5fN14	66.2	rise
</priority_pla/current_intr[4]	62.7	fall
<r_mod/intr_dp/current_intr[4]	62.6	fall
<_mod/intr_dp/current_intr[4]'	62.6	fall
<r_mod/intr_dp/phb_lat_VAL1[4]	61.0	fall
intr_mod/intr_dp/guarded_ei	52.5	rise
intr_mod/ld_ctrl/guarded_ei	52.5	rise
intr_mod/ld_ctrl/guarded_ei'	50.7	rise
intr_mod/ld_ctrl/n_guard	49.5	rise
io_mod/ids_sel/n_guard_out	47.7	rise
io_mod/ids_sel/n_guard_out'	42.0	rise
io_mod/ids_sel/n_guard	41.0	rise
io_mod/freeze_ctrl/n_guard	40.9	rise
io_mod/freeze_ctrl/n_guard'	39.6	rise
<od/freeze_ctrl/GB.LP.NNZ5fN14	39.3	fall
<od/freeze_ctrl/GB.LP.NNZ5fN34	38.6	rise
<mod/freeze_ctrl/GB.LP.NNZ5fN2	37.5	fall
<mod/freeze_ctrl/GB.LP.NNZ5fN6	37.0	rise
<mod/freeze_ctrl/GB.LP.NNZ5fN9	35.3	rise
io_mod/freeze_ctrl/ids_freeze	33.9	fall
io_mod/test_ctrl/ids_freeze	33.8	fall
io_mod/test_ctrl/ids_freeze'	32.2	fall
io_mod/test_ctrl/ids_fr_lat	30.9	fall

io_mod/test_ctrl/ids_fr_lat'	30.8	fall
io_mod/test_ctrl/ids_freeze_in	28.0	fall
io_mod/ds_ctrl/ids_freeze_in	28.0	fall
io_mod/ds_ctrl/ids_freeze_in'	28.0	fall
io_mod/ds_ctrl/async_ids_fr	26.2	fall
<d/async_ids_ctrl/async_ids_fr	26.2	fall
</async_ids_ctrl/async_ids_fr'	25.8	fall
<async_ids_ctrl/GB.LP.NNZ5fN27	25.4	rise
<async_ids_ctrl/GB.LP.NNZ5fN15	23.3	fall
<async_ids_ctrl/GB.LP.NNZ5fN18	22.7	rise
<async_ids_ctrl/GB.LP.NNZ5fN28	21.2	fall
</async_ids_ctrl/GB.LP.NNZ5fN6	19.4	rise
<async_ids_ctrl/GB.LP.NNZ5fN12	18.4	fall
io_mod/async_ids_ctrl/ids_sel	17.9	rise
io_mod/ids_sel/ids_sel	17.7	rise
io_mod/ids_sel/ids_sel'	14.3	rise
io_mod/ids_sel/ids_sel_buf	13.3	rise
io_mod/ids_sel/ids_sel_buf'	13.0	rise
io_mod/ids_sel/ids_ph_in	10.8	rise
io_mod/ids_sel/ids_ph_out	10.8	rise
io_mod/ids_sel/ids_ph_out'	10.7	rise
io_mod/ids_sel/PHASE_B	8.7	rise
clk_pad/PHASE_B	8.6	rise
Clk	0.0	fall

Genesil Version v8.0.2 -- Mon Feb 4 12:15:29 1991

Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/iag Timing Analyzer

OUTPUT DELAY MODE

Fabline: HP2_CN10B Corner: GUARANTEED

Junction Temperature: 117 deg C Voltage: 4.50v

External Clock: Clk

Included setup files:

#0 basic (Input constraints from other chip>
 #1 worst (117 deg C, 4.5 Volts)

OUTPUT DELAYS (ns)

Output	Ph1(r) Delay	Ph2(r) Delay	Loading(pf)
	Min Max	Min Max	
ALU_opcode[0]	24.8 27.0	--- ---	50.00 PATH
ALU_opcode[1]	24.9 27.1	--- ---	50.00 PATH
ALU_opcode[2]	24.3 26.6	--- ---	50.00 PATH
ALU_opcode[3]	24.4 26.7	--- ---	50.00 PATH
ALU_opcode[4]	24.5 26.8	--- ---	50.00 PATH
ALU_opcode[5]	24.4 26.7	--- ---	50.00 PATH
ALU_opcode[6]	24.6 26.8	--- ---	50.00 PATH
ALU_opcode[7]	24.6 26.8	--- ---	50.00 PATH
Booting	25.7 28.0	--- ---	50.00 PATH
DAG_R_en	29.9 93.9	35.0 51.8	50.00 PATH
Dr	39.6 99.3	49.2 53.3	50.00 PATH
Flush	23.7 47.4	--- ---	50.00 PATH
Freeze	32.3 90.3	33.9 53.2	50.00 PATH

Guard	35.5	99.0	38.7	61.9	50.00	PATH
Ids_eq_ods_1	33.9	39.1	---	---	50.00	PATH
Ids_eq_ods_2	35.0	39.6	---	---	50.00	PATH
Ids_freeze	24.5	30.0	21.4	42.4	50.00	PATH
Ids_sel	21.6	28.0	24.4	24.4	50.00	PATH
Inst[0]	---	---	22.2	27.5	50.00	PATH
Inst[10]	---	---	23.8	27.1	50.00	PATH
Inst[11]	---	---	23.7	27.1	50.00	PATH
Inst[12]	---	---	23.7	27.0	50.00	PATH
Inst[13]	---	---	23.5	27.0	50.00	PATH
Inst[14]	---	---	23.3	27.0	50.00	PATH
Inst[15]	---	---	23.2	27.0	50.00	PATH
Inst[16]	---	---	23.3	27.0	50.00	PATH
Inst[17]	---	---	23.4	27.0	50.00	PATH
Inst[18]	---	---	23.4	27.0	50.00	PATH
Inst[19]	---	---	23.5	27.0	50.00	PATH
Inst[1]	---	---	22.3	27.5	50.00	PATH
Inst[20]	---	---	23.4	27.0	50.00	PATH
Inst[21]	---	---	23.6	27.0	50.00	PATH
Inst[22]	---	---	23.7	27.0	50.00	PATH
Inst[23]	---	---	23.8	27.0	50.00	PATH
Inst[24]	---	---	22.8	27.4	50.00	PATH
Inst[25]	---	---	22.7	27.4	50.00	PATH
Inst[26]	---	---	23.5	27.4	50.00	PATH
Inst[27]	---	---	23.5	27.4	50.00	PATH
Inst[28]	---	---	23.6	27.4	50.00	PATH
Inst[29]	---	---	23.7	27.4	50.00	PATH
Inst[2]	---	---	22.5	27.5	50.00	PATH
Inst[30]	---	---	24.1	27.4	50.00	PATH
Inst[31]	---	---	24.0	27.4	50.00	PATH
Inst[32]	---	---	23.9	27.7	50.00	PATH
Inst[33]	---	---	23.9	27.7	50.00	PATH
Inst[34]	---	---	24.0	27.7	50.00	PATH
Inst[35]	---	---	24.1	27.7	50.00	PATH
Inst[36]	---	---	24.2	27.8	50.00	PATH
Inst[37]	---	---	24.3	27.8	50.00	PATH
Inst[38]	---	---	24.6	27.8	50.00	PATH
Inst[39]	---	---	24.7	27.8	50.00	PATH
Inst[3]	---	---	22.6	27.5	50.00	PATH
Inst[40]	---	---	24.5	30.8	50.00	PATH
Inst[41]	---	---	25.3	31.0	50.00	PATH
Inst[42]	---	---	23.9	30.2	50.00	PATH
Inst[43]	---	---	23.7	30.2	50.00	PATH
Inst[44]	---	---	22.8	30.3	50.00	PATH
Inst[45]	---	---	22.8	30.3	50.00	PATH
Inst[4]	---	---	24.5	27.5	50.00	PATH
Inst[5]	---	---	24.4	27.5	50.00	PATH
Inst[6]	---	---	24.2	27.5	50.00	PATH
Inst[7]	---	---	24.0	27.4	50.00	PATH
Inst[8]	---	---	23.9	27.1	50.00	PATH
Inst[9]	---	---	23.9	27.1	50.00	PATH
Inst_en	---	---	24.3	24.7	50.00	PATH
Inst_rd	26.1	90.1	---	---	50.00	PATH
Ios	22.4	24.2	---	---	50.00	PATH

Kernel_mode	41.4	50.9	---	---	50.00	PATH
N_cs_pha	25.1	25.1	16.6	25.1	50.00	PATH
N_cs_phb	24.3	24.3	19.6	25.9	50.00	PATH
N_inst_wr	22.7	22.7	15.4	15.4	50.00	PATH
N_read[1]	23.5	30.0	27.5	29.0	50.00	PATH
N_reset_out	28.8	44.1	---	---	50.00	PATH
N_write[1]	19.7	46.1	23.0	34.2	50.00	PATH
Ncs[1]	18.3	27.1	21.5	25.3	50.00	PATH
Ncs[2]	19.4	28.1	22.5	26.2	50.00	PATH
Ncs[3]	19.8	28.5	23.0	26.6	50.00	PATH
Ods_freeze	25.5	79.8	28.8	30.7	50.00	PATH
Ods_ids[0]	29.7	91.1	34.2	41.7	50.00	PATH
Ods_ids[1]	29.3	90.8	33.8	41.3	50.00	PATH
Ods_ids[2]	29.6	91.1	34.2	41.7	50.00	PATH
Ods_ids[3]	29.6	91.1	34.2	41.7	50.00	PATH
Ods_sel	22.1	29.9	28.6	28.6	50.00	PATH
Pc[0]	---	---	17.1	21.4	50.00	PATH
Pc[10]	---	---	16.7	21.0	50.00	PATH
Pc[11]	---	---	16.7	20.9	50.00	PATH
Pc[12]	---	---	16.6	20.9	50.00	PATH
Pc[13]	---	---	16.5	20.8	50.00	PATH
Pc[14]	---	---	16.8	21.1	50.00	PATH
Pc[15]	---	---	16.9	21.2	50.00	PATH
Pc[16]	---	---	17.0	21.2	50.00	PATH
Pc[17]	---	---	17.0	21.3	50.00	PATH
Pc[18]	---	---	17.1	21.3	50.00	PATH
Pc[19]	---	---	17.1	21.4	50.00	PATH
Pc[1]	---	---	17.1	21.3	50.00	PATH
Pc[20]	---	---	17.2	21.5	50.00	PATH
Pc[21]	---	---	17.3	21.5	50.00	PATH
Pc[22]	---	---	17.4	21.6	50.00	PATH
Pc[23]	---	---	17.3	21.6	50.00	PATH
Pc[24]	---	---	17.3	21.6	50.00	PATH
Pc[25]	---	---	17.4	21.6	50.00	PATH
Pc[2]	---	---	17.1	21.4	50.00	PATH
Pc[3]	---	---	17.0	21.3	50.00	PATH
Pc[4]	---	---	17.0	21.3	50.00	PATH
Pc[5]	---	---	17.0	21.3	50.00	PATH
Pc[6]	---	---	17.0	21.3	50.00	PATH
Pc[7]	---	---	17.0	21.2	50.00	PATH
Pc[8]	---	---	17.0	21.2	50.00	PATH
Pc[9]	---	---	16.9	21.2	50.00	PATH
RF[0]	28.4	131.2	31.7	49.3	50.00	PATH
RF[10]	26.9	130.2	33.4	58.5	50.00	PATH
RF[11]	26.7	130.1	33.4	52.1	50.00	PATH
RF[12]	26.6	130.1	33.4	49.9	50.00	PATH
RF[13]	26.5	130.0	33.4	49.9	50.00	PATH
RF[14]	26.2	130.0	33.4	50.5	50.00	PATH
RF[15]	26.7	130.5	33.5	49.9	50.00	PATH
RF[16]	27.1	130.8	31.1	81.2	50.00	PATH
RF[17]	26.9	130.7	31.1	54.3	50.00	PATH
RF[18]	26.2	130.2	31.1	57.4	50.00	PATH
RF[19]	26.6	130.5	31.1	54.5	50.00	PATH
RF[1]	28.3	131.1	31.7	49.2	50.00	PATH

RF[20]	27.8	131.5	31.1	49.0	50.00	PATH
RF[21]	26.8	130.7	31.1	48.2	50.00	PATH
RF[22]	26.3	130.3	31.1	78.3	50.00	PATH
RF[23]	25.7	130.0	31.1	47.6	50.00	PATH
RF[24]	25.1	129.5	33.7	50.2	50.00	PATH
RF[25]	25.5	132.6	33.7	52.2	50.00	PATH
RF[26]	24.6	92.2	33.6	50.1	50.00	PATH
RF[27]	24.5	92.2	33.6	50.1	50.00	PATH
RF[28]	24.0	92.2	33.6	50.1	50.00	PATH
RF[29]	23.9	92.2	33.6	50.0	50.00	PATH
RF[2]	28.2	131.0	31.8	49.1	50.00	PATH
RF[30]	23.7	92.1	33.6	50.0	50.00	PATH
RF[31]	23.6	92.1	33.6	50.0	50.00	PATH
RF[3]	28.1	130.9	31.8	49.0	50.00	PATH
RF[4]	27.9	130.8	31.8	48.9	50.00	PATH
RF[5]	27.8	130.7	31.8	48.8	50.00	PATH
RF[6]	27.7	130.7	31.8	48.7	50.00	PATH
RF[7]	27.6	130.6	31.8	48.7	50.00	PATH
RF[8]	27.2	130.4	33.4	57.6	50.00	PATH
RF[9]	27.3	130.5	33.4	54.3	50.00	PATH
Read[2]	34.3	40.7	34.5	39.3	50.00	PATH
Read[3]	39.5	45.9	39.2	44.6	50.00	PATH
Valid_intr_pulse	34.1	62.5	---	---	50.00	PATH
Write[2]	21.4	46.7	25.2	26.7	50.00	PATH
Write[3]	21.5	46.8	25.4	26.9	50.00	PATH

Genesil Version v8.0.2 -- Mon Feb 4 12:19:35 1991

Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/iag

Timing Analyzer

SETUP AND HOLD MODE

Fabline: HP2_CN10B

Corner: GUARANTEED

Junction Temperature:117 deg C

Voltage:4.50v

External Clock: Clk

Included setup files:

#0 basic

(Input constraints from other chip>

#1 worst

(117 deg C, 4.5 Volts)

INPUT SETUP AND HOLD TIMES (ns)

Input	Setup Time		Hold Time		
	Ph1(f)	Ph2(f)	Ph1(f)	Ph2(f)	
ALU_Flag	42.9	4.6	0.8	-3.0	PATH
Carry	42.2	4.6	0.8	-3.1	PATH
DAG_error	---	12.1	---	-5.2	PATH
DAV[1]	---	77.2	---	-12.3	PATH
DAV[2]	---	77.9	---	-12.3	PATH
DAV[3]	---	78.3	---	-12.9	PATH
Dr	38.4	81.6	-4.4	-3.2	PATH
IAG_test[0]	---	72.4	---	0.4	PATH
IAG_test[1]	---	72.3	---	0.2	PATH
Inst[0]	---	5.9	---	-3.1	PATH
Inst[10]	---	7.6	---	-4.3	PATH
Inst[11]	---	7.3	---	-4.3	PATH
Inst[12]	---	4.9	---	-2.9	PATH

Inst[13]	---	4.7	---	-2.7	PATH
Inst[14]	---	4.4	---	-2.3	PATH
Inst[15]	---	4.3	---	-2.2	PATH
Inst[16]	---	4.3	---	-2.2	PATH
Inst[17]	---	4.4	---	-2.3	PATH
Inst[18]	---	4.4	---	-2.3	PATH
Inst[19]	---	4.5	---	-2.5	PATH
Inst[1]	---	6.2	---	-3.3	PATH
Inst[20]	---	4.6	---	-2.5	PATH
Inst[21]	---	4.6	---	-2.6	PATH
Inst[22]	---	4.6	---	-2.5	PATH
Inst[23]	---	4.2	---	-2.1	PATH
Inst[24]	---	4.1	---	-2.0	PATH
Inst[25]	---	4.1	---	-2.0	PATH
Inst[26]	---	7.2	---	-3.5	PATH
Inst[27]	---	7.6	---	-3.6	PATH
Inst[28]	---	8.6	---	-4.2	PATH
Inst[29]	---	7.7	---	-4.1	PATH
Inst[2]	---	7.5	---	-4.7	PATH
Inst[30]	---	4.0	---	-2.1	PATH
Inst[31]	---	4.5	---	-2.6	PATH
Inst[32]	---	4.0	---	-2.1	PATH
Inst[33]	---	4.0	---	-2.1	PATH
Inst[34]	---	4.0	---	-2.1	PATH
Inst[35]	---	4.0	---	-2.1	PATH
Inst[36]	---	4.0	---	-2.1	PATH
Inst[37]	---	5.6	---	-3.8	PATH
Inst[38]	---	8.0	---	-3.4	PATH
Inst[39]	---	8.2	---	-3.6	PATH
Inst[3]	---	7.8	---	-4.8	PATH
Inst[40]	---	8.4	---	-3.8	PATH
Inst[41]	---	8.1	---	-3.7	PATH
Inst[42]	---	10.3	---	-5.6	PATH
Inst[43]	---	10.2	---	-5.5	PATH
Inst[44]	---	9.9	---	-5.2	PATH
Inst[45]	---	9.8	---	-5.1	PATH
Inst[4]	---	8.2	---	-4.7	PATH
Inst[5]	---	7.2	---	-4.6	PATH
Inst[6]	---	8.3	---	-4.7	PATH
Inst[7]	---	7.2	---	-4.5	PATH
Inst[8]	---	7.5	---	-4.3	PATH
Inst[9]	---	7.2	---	-4.3	PATH
Inst_rdy	---	26.9	---	1.1	PATH
Intr[0]	---	9.9	---	-7.5	PATH
Intr[1]	---	10.0	---	-7.5	PATH
Intr[2]	---	10.1	---	-7.6	PATH
Intr[3]	---	10.1	---	-7.6	PATH
Intr[4]	---	10.2	---	-7.7	PATH
Intr[5]	---	10.2	---	-7.7	PATH
Intr[6]	---	10.3	---	-7.8	PATH
Intr[7]	---	10.4	---	-7.9	PATH
Intr[8]	---	9.4	---	-6.8	PATH
N_reset	-4.6	---	6.9	---	PATH
Pixel_clk	39.9	83.7	-18.5	-1.7	PATH

RFI[1]	36.5	---	-1.4	---	PATH
RFI[2]	36.3	---	-1.6	---	PATH
RFI[3]	36.4	---	-1.2	---	PATH
RF[0]	1.4	2.8	-0.2	0.7	PATH
RF[10]	1.6	2.9	-0.3	0.5	PATH
RF[11]	1.5	2.8	-0.3	0.5	PATH
RF[12]	1.4	2.8	-0.2	0.6	PATH
RF[13]	1.9	3.2	-0.8	0.1	PATH
RF[14]	1.3	2.6	-0.1	0.8	PATH
RF[15]	1.3	2.6	-0.1	0.7	PATH
RF[16]	1.5	2.8	-0.3	0.5	PATH
RF[17]	1.4	2.7	-0.2	0.6	PATH
RF[18]	1.1	2.4	0.1	1.0	PATH
RF[19]	1.3	2.7	-0.1	0.7	PATH
RF[1]	3.3	4.6	-2.2	-1.4	PATH
RF[20]	1.0	2.3	0.2	1.1	PATH
RF[21]	1.1	2.5	0.1	0.9	PATH
RF[22]	1.4	2.7	-0.2	0.7	PATH
RF[23]	1.7	3.0	-0.5	0.4	PATH
RF[24]	1.7	3.0	-0.6	0.3	PATH
RF[25]	2.2	3.5	-1.0	-0.1	PATH
RF[26]	---	-0.6	---	1.8	PATH
RF[27]	---	-0.7	---	1.9	PATH
RF[28]	---	-0.9	---	2.1	PATH
RF[29]	---	-1.0	---	2.2	PATH
RF[2]	1.5	2.8	-0.2	0.6	PATH
RF[30]	---	-1.1	---	2.3	PATH
RF[31]	---	-1.2	---	2.4	PATH
RF[3]	1.5	2.8	-0.2	0.6	PATH
RF[4]	1.5	2.8	-0.2	0.6	PATH
RF[5]	3.1	4.5	-2.1	-1.2	PATH
RF[6]	1.5	2.9	-0.3	0.5	PATH
RF[7]	1.6	2.9	-0.3	0.5	PATH
RF[8]	1.5	2.8	-0.3	0.5	PATH
RF[9]	2.2	3.5	-1.0	-0.2	PATH
R_eq_f_1	---	62.7	---	-6.4	PATH
R_eq_f_2	---	5.7	---	-2.1	PATH
S_eq_f_1	---	5.2	---	-3.7	PATH
S_eq_f_2	---	5.3	---	-3.9	PATH
Sign	43.1	4.4	1.0	-2.9	PATH
Status[0]	28.3	---	-3.5	---	PATH
Status[1]	28.3	---	-3.5	---	PATH
Status[2]	31.1	---	-6.1	---	PATH
Status[3]	27.7	---	-2.6	---	PATH
Status[4]	27.1	---	-2.5	---	PATH
Zero	42.4	4.4	1.0	-2.8	PATH

Genesil Version v8.0.2 -- Mon Feb 4 12:20:05 1991

Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/iag Timing Analyzer

PATH DELAY MODE

Fabline: HP2_CN10B

Corner: GUARANTEED

Junction Temperature:117 deg C

Voltage:4.50v

External Clock: Clk

Included setup files:

```
#0 basic          (Input constraints from other chip>
#1 worst          (117 deg C, 4.5 Volts)
```

		PATH DELAY (ns)			
Source Object	Connector	(Ph1) Min	Max		
Dest. Object	Connector	(Ph2) Min	Max		
clk_pad_____	PHASE_A_____	9.5	21.7		
io_mod/sell_____	ods_en_____	18.8	23.1	PATH	
io_mod/sell_____	ods_en_____	---	---		
*CURRENT*_____	Ncs[1]_____	---	---	PATH	
clk_pad_____	PHASE_A_____	8.8	9.5		
io_mod/sell_____	ods_inst[3]_____	---	---	PATH	
io_mod/sell_____	ods_inst[3]_____	---	---		
*CURRENT*_____	Ncs[1]_____	---	---	PATH	
clk_pad_____	PHASE_A_____	9.5	21.7		
io_mod/sell_____	ods_en_____	18.8	23.1	PATH	
io_mod/sell_____	ods_en_____	14.9	15.9		
*CURRENT*_____	N_write[1]_____	---	---	PATH	
clk_pad_____	PHASE_A_____	8.8	9.5		
io_mod/sell_____	ods_inst[3]_____	---	---	PATH	
io_mod/sell_____	ods_inst[3]_____	---	---		
*CURRENT*_____	N_write[1]_____	---	---	PATH	
io_mod/io_dp_____	ods_en_____	15.6	17.4		
*CURRENT*_____	Ods_ids[2]_____	15.6	17.4	PATH	
io_mod/io_dp_____	ids_sel_____	16.2	19.5		
*CURRENT*_____	Ods_ids[2]_____	16.2	19.5	PATH	
io_mod/io_dp_____	dff1_VAL1[2]_____	17.0	18.9		
*CURRENT*_____	Ods_ids[2]_____	17.0	18.9	PATH	
> _____	_____				

```
*****
Genesil Version v8.0.2 -- Mon Feb  4 12:20:09 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/iag          Timing Analyzer
*****
```

NODE DELAY MODE

```
-----
Fabline: HP2_CN10B                      Corner: GUARANTEED
Junction Temperature:117 deg C          Voltage:4.50v
External Clock: Clk
Included setup files:
#0 basic                                (Input constraints from other chip>
#1 worst                                (117 deg C, 4.5 Volts)
-----
```

NODE DELAYS (ns)

Object	Connector	Ph1(r) Delay Min	Ph1(r) Delay Max	Ph2(r) Delay Min	Ph2(r) Delay Max	
io_mod/io_dp__	ods_en__	18.0	30.1	21.7	26.1	PATH
io_mod/io_dp__	ids_sel__	13.3	19.7	18.0	18.0	PATH
io_mod/io_dp__	dff1_VAL1[2]_	12.6	13.2	---	---	PATH

>

```
*****
Genesil Version v8.0.2 -- Mon Feb  4 12:20:18 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/iag          Timing Analyzer
*****
VIOLATION MODE
-----
```

```
Fabline: HP2_CN10B                      Corner: GUARANTEED
Junction Temperature:117 deg C          Voltage:4.50v
External Clock: Clk
Included setup files:
#0 basic                                (Input constraints from other chip>
#1 worst                                (117 deg C, 4.5 Volts)
-----
```

NO VIOLATIONS

Hold time check margin: 2.0ns

DV CHECKLIST

1. DV CONTROL NUMBER : _____

2. CUSTOMER INFORMATION

Customer Name : Georgia Tech / CERL Chip Name : GT-VIAG

Address : 400 Tenth Street FAX : (404) 894-3120

CRB Room 377

Atlanta, GA 30332-0540

Project Manager : Dr. C. O. Alford Phone : (404) 894-2505

Design Engineer : Dr. Wei Siong Tan Phone : (404) 894-2508

Samuel H. Russ Phone : (404) 894-7472

Test Engineer : Joseph I. Chamdani Phone : (404) 894-2527

3. SERVICES INFORMATION

xx Design Verification Service only. PO # _____

_____ Prototype Service and Design Verification. PO # _____

_____ 1.8% Maintenance

_____ SCS Test _____ Foundry Test _____ Customer Test

When DV is complete, send verified physical database tape to

Customer Y N Silicon Vendor Y N

4. DV CONTACT : Ying Chow Phone : (408) 371-2900

7.7. Test Pad (PM Pad) is included? Y N (Required for PS)

7.8. Power Pad : VDD: Core 4 VSS: Core 4
 Ring 13 Ring 12

NP protection for nwell pad? Y N

TTL output pads or N Protection for inputs? Y N
 If yes, have you received silicon vendor approval? Y N

Error in PADRING.033 (PADRING.DRC)? Y N Hardcopy attached? Y N

ESD requirements _____ Approved by SCS? Y N

8. ELECTRICAL INFORMATION

8.1. Chip Frequency Specified in netlist : 10.0 MHz Target frequency : 10.0 MHz
 8.2. Power Dissipation: GENESIL = 1.18 W at 10 MHz Spec = 1.0 W at 10.0 MHz
 8.3. Operating Voltage: from 4.5 Volts to 5.5 Volts

9. SIMULATION

9.1. Number of Clocking Regimes : 1

	Clock Pad Name	DIV/NO DIV	Ext Clock Name	Int PHASE A/PHASE B Name
1.	<u>clock pad</u>	<u>NO DIV</u>	<u>Clk</u>	<u>PHASE A / PHASE B</u>
2.	_____	_____	_____	_____
3.	_____	_____	_____	_____
4.	_____	_____	_____	_____
5.	_____	_____	_____	_____

9.2. Simulation Setup Files:

Name : designinit.080 Listings attached : Yes

Description : Sets up Clk and tags for cycles and steps.

Affected Tests : Required for simulation with .089's, not needed for traceobj output.

Name : _____ Listings attached : _____

Description : _____

Affected Tests : _____

Name : _____ Listings attached : _____

Description : _____

Affected Tests : _____

Name : _____ Listings attached : _____

Description : _____

Affected Tests : _____

9.3. Test Vector Set:

Total No. of Vectors : 29,734

NOTE : Test vectors written one phase per vector have a maximum test frequency on the IMS Tester of 10 MHz.

Test vectors written one cycle per vector have a maximum test frequency on the IMS Tester of 20 MHz.

1. Name : add_trace.083 No of vectors : 3494Description : Tests all adders.Portions of Chip Tested : VariousPass with GFL model? xxPass with GSL model? xxUse for PS testing? Y NPass Fight Test? xx2. Name : boot_trace.083 No of vectors : 108Description : Tests bootstrap mode.Portions of Chip Tested : Various.Pass with GFL model? xxPass with GSL model? xxUse for PS testing? Y NPass Fight Test? xx3. Name : branch_trace.083 No of vectors : 546Description : Tests branching modes and opcodes.Portions of Chip Tested : pc_gen_modPass with GFL model? xxPass with GSL model? xxUse for PS testing? Y NPass Fight Test? xx4. Name : dp_trace.083 No of vectors : 2704Description : Tests logic contained in parallel datapaths on-chip.Portions of Chip Tested : Various.Pass with GFL model? xxPass with GSL model? xxUse for PS testing? Y NPass Fight Test? xx5. Name : dssio_trace.083 No of vectors : 1616Description : Tests DSS I/O mode.

Portions of Chip Tested : io mod

Pass with GFL model? xx

Pass with GSL model? xx

Pass Fight Test? xx

Use for PS testing? Y N

6. Name : flush trace.083 No of vectors : 1710

Description : Tests flush signal.

Portions of Chip Tested : pc gen mod, etc.

Pass with GFL model? xx

Pass with GSL model? xx

Pass Fight Test? xx

Use for PS testing? Y N

7. Name : freeze trace.083 No of vectors : 1132

Description : Tests freeze signal.

Portions of Chip Tested : io mod, etc.

Pass with GFL model? xx

Pass with GSL model? xx

Pass Fight Test? xx

Use for PS testing? Y N

8. Name : grd trace.083 No of vectors : 1322

Description : Tests guard signal.

Portions of Chip Tested : io mod, etc.

Pass with GFL model? xx

Pass with GSL model? xx

Pass Fight Test? xx

Use for PS testing? Y N

9. Name : iag test trace.083 No of vectors : 2220

Description : Tests IAG's special test mode.

Portions of Chip Tested : Various.

Pass with GFL model? xx

Pass with GSL model? xx

Pass Fight Test? xx

Use for PS testing? Y N

10.Name : inst_rdy_trace.083 No of vectors : 498
Description : Tests behavior of chip in its interaction with the inst_rdy signal.

Portions of Chip Tested : inst_en, various

Pass with GFL model? xx
Pass with GSL model? xx Use for PS testing? Y N
Pass Fight Test? xx

11.Name : intr_trace.083 No of vectors : 480
Description : Tests interrupts.

Portions of Chip Tested : intr_mod, etc.

Pass with GFL model? xx
Pass with GSL model? xx Use for PS testing? Y N
Pass Fight Test? xx

12.Name : io_intr_trace.083 No of vectors : 694
Description : Tests interruption of I/O operations.

Portions of Chip Tested : io_mod, intr_mod

Pass with GFL model? xx
Pass with GSL model? xx Use for PS testing? Y N
Pass Fight Test? xx

13.Name : io_trace.083 No of vectors : 268
Description : Tests I/O

Portions of Chip Tested : io_mod

Pass with GFL model? xx
Pass with GSL model? xx Use for PS testing? Y N
Pass Fight Test? xx

14.Name : ios_trace.083 No of vectors : 202
Description : Tests generation of Ios signal.

Portions of Chip Tested : io_mod/ios_ctrl

Pass with GFL model? xx
Pass with GSL model? xx Use for PS testing? Y N
Pass Fight Test? xx

15.Name : iosat_trace.083 No of vectors : 3833
Description : Generated by performing a traceobj of the GT-EP chipset.

Portions of Chip Tested : Various

Pass with GFL model? xx
Pass with GSL model? xx Use for PS testing? Y N
Pass Fight Test? xx

16.Name : kernel_trace.083 No of vectors : 1070
Description : Tests to confirm kernel instructions are not executed in user mode.

Portions of Chip Tested : Various

Pass with GFL model? xx
Pass with GSL model? xx Use for PS testing? Y N
Pass Fight Test? xx

17.Name : ldst_trace.083 No of vectors : 308
Description : Tests load and store instructions.

Portions of Chip Tested : Various

Pass with GFL model? xx
Pass with GSL model? xx Use for PS testing? Y N
Pass Fight Test? xx

18.Name : reg_test_trace.083 No of vectors : 1158
Description : Loads all registers with test patterns.

Portions of Chip Tested : Various.

Pass with GFL model? xx
Pass with GSL model? xx Use for PS testing? Y N
Pass Fight Test? xx

19.Name : sort4_trace.083 No of vectors : 4517
Description : Generated by performing a traceobj of the GT-EP chipset.

1.	_____	Y N
2.	_____	Y N
3.	_____	Y N
4.	_____	Y N
5.	_____	Y N
6.	_____	Y N
7.	_____	Y N
8.	_____	Y N
9.	_____	Y N

10. TIMING ANALYSIS

10.1. System Environment

Temperature Coefficient: 35 Degrees C / Watt (theta JA)
 Operating Temp : from 0⁰ C (min) to 75⁰ C (max)
 Operating Voltage : from 4.5 V (min) to 5.5 V (max)
 room junction temp = $25 + (\text{theta JA} * \text{Power}) = \underline{67}$ degrees C
 maximum junction temp = maximum ambient temp + (theta JA * Power) = 117 degrees C

10.2. Reports (Include the following reports)

(required for PS)* guaranteed corner 5.0V room junc temp	(required for PS)* guaranteed corner min operating V max junction temp	typical corner min operating V max junction temp
Cycle : <u>xx</u>	Cycle : <u>xx</u>	Cycle : <u> </u>
Setup/Hold : <u>xx</u>	Setup/Hold : <u>xx</u>	Setup/Hold : <u> </u>
Output Delay : <u>xx</u>	Output Delay : <u>xx</u>	Output Delay : <u> </u>
Violation : <u>xx</u>	Violation : <u>xx</u>	Violation : <u> </u>

10.3. Timing Setup Files:

Name : basic.040 Listings attached : Yes
 Temperature : Voltage :
 Description : Ouput delays from other chips are specified, as well as IGNORE PATH.
To be used for analysis at all temperatures, voltages, and corners.

Name : baseline.040 Listings attached : Yes
 Temperature : 75 Voltage : 5.0
 Description : For TYPICAL analysis.

Name : room.040 Listings attached : Yes
 Temperature : 67 Voltage : 5.0
 Description : For room temp, 5 V, GUARANTEED analysis

Name : worst.040 Listings attached : Yes
 Temperature : 117 Voltage : 4.5
 Description : For max, temp, 4.5V, GUARANTEED analysis

10.4. Critical Boundary Conditions:

List critical paths here or annotate the timing report.
Attach additional pages if needed.

Clock Name :	<u>Clk</u>			
	report	limit (+/-5%)	report	limit (+/-5%)
1. Phase 1 High	<u>42.6 ns</u>	<u>50 ns</u>	<u> </u>	<u> </u>
2. Phase 2 High	<u>46.3 ns</u>	<u>50 ns</u>	<u> </u>	<u> </u>
3. Symmetric Cycle	<u>92.6 ns</u>	<u>100 ns</u>	<u> </u>	<u> </u>
4. Minimum Cycle	<u>90.8 ns</u>	<u>100 ns</u>	<u> </u>	<u> </u>

Outputs

	Signal Name	load (pF)	delay	limit
1.	<u>Flush</u>	<u>50</u>	<u>36.4</u>	<u>37.9</u>
2.	<u>Freeze</u>	<u>50</u>	<u>27.9</u>	<u>38.3</u>
3.	<u>Guard</u>	<u>50</u>	<u>30.9</u>	<u>32.7</u>
4.	<u>Ids eq ods 1</u>	<u>50</u>	<u>20.3</u>	<u>42.8</u>
5.	<u>Ids eq ods 2</u>	<u>50</u>	<u>21.0</u>	<u>42.6</u>
6.	<u>Ids freeze</u>	<u>50</u>	<u>23.0</u>	<u>47.4</u>
7.	<u>Ods freeze</u>	<u>50</u>	<u>40.7</u>	<u>47.4</u>
8.	<u>Pc[25:0]</u>	<u>50</u>	<u>12.2</u>	<u>15.0</u>
9.	<u>RF[31:0]</u>	<u>50</u>	<u>40.5</u>	<u>40.0</u>
10.	<u> </u>	<u> </u>	<u> </u>	<u> </u>
11.	<u> </u>	<u> </u>	<u> </u>	<u> </u>
12.	<u> </u>	<u> </u>	<u> </u>	<u> </u>

Inputs

	Signal Name	setup report / limit	hold report / limit
1.	<u>RF[31:0] — PHASE A</u>	<u>2.0 / 5.0</u>	<u>-0.3 / 0.0</u>
2.	<u> — PHASE B</u>	<u>3.1 / 5.0</u>	<u>0.2 / 0.0</u>
3.	<u> </u>	<u>/</u>	<u>/</u>
4.	<u> </u>	<u>/</u>	<u>/</u>
5.	<u> </u>	<u>/</u>	<u>/</u>
6.	<u> </u>	<u>/</u>	<u>/</u>
7.	<u> </u>	<u>/</u>	<u>/</u>
8.	<u> </u>	<u>/</u>	<u>/</u>
9.	<u> </u>	<u>/</u>	<u>/</u>

10.5. Hold Time Violations : none (At 2.0 nsec.)

11. DC CHARACTERISTICS

PARAMETERS	DESCRIPTION	CONDITIONS 0 to 70	CONDITIONS -55 to +125	MIN	MAX
DATA PAD INPUT ONLY					
VIH	Input High Voltage			2.0V	
VIL	Input Low Voltage				0.8V
IIL	Input Leakage	VSS<Vin<VDD	VSS<Vin<VDD	-10uA	10uA
CIN	Input Capacitance				6.0pf
DATA PAD OUTPUT ONLY					
VOH	Output High Voltage	VDD= 4.5V IOH=-2.2	VDD= 4.5V IOH=-2mA	2.4V	
VOL	Output Low Voltage	VDD= 4.5V IOL= 6mA	VDD= 4.5V IOL= 5mA		0.4V
IOZ	Output Leakage current(high Z)	VSS<Vout<VDD	VSS<Vout<VDD	-10uA	10uA
COUT	Output Capacitance				7.0pf
DATA PAD INPUT/OUTPUT					
VOH	Output High Voltage	VDD= 4.5V IOH=-2.2	VDD= 4.5V IOH=-2mA	2.4V	
VOL	Output Low Voltage	VDD= 4.5V IOL= 6mA	VDD= 4.5V IOL= 5mA		0.4V
VIH	Input High Voltage			2.0V	
VIL	Input Low Voltage				0.8V
IOZ	Output leakage current (high Z)	VSS<Vout<VDD	VSS<Vout<VDD	-10uA	10uA
CIO	Input/Output Capacitance				7.0pf
CLOCK PAD					
VIH	Input High Voltage			3.9V	
VIL	Input Low Voltage				0.6V
IIL	Input Leakage	VSS<Vin<VDD	VSS<Vin<VDD	-10uA	10uA
CIN	Input Capacitance				15pf

NOTE: All parameters at a supply voltage of VDD = 5V (+/- 10%).

12. CUSTOMER COMMENTS**Pre-Verification Comments**

1. tnet reports some "undriven nets". These are correct, and do not represent an actual error.
2. Genesil's Pading CCC flags bond angle, bond length, and wire crossing problems. A copy of the bonding diagram has been sent to HP for approval.

Post-Verification Comments

1. Power and ground routing forced extensive re-routing of the entire chip. The placement of core power and ground pins confused the router and made the route larger.
2. Die Size is now approximately 411 by 427 mils.
3. Genesil flagged bonding angle, length, and wire crossing problems. HP as checked the bonding and found it acceptable for prototype purposes.
4. pc gen mod/bradr pla grew enormously when re-compiled. Steps were taken to get it back to original size since the size increase affected the entire die size.

13. CUSTOMER APPROVAL

The undersigned understands that if any design changes are initiated by the Customer subsequent to this sign-off, the Customer is liable for any charges imposed by Silicon Compiler Systems as agreed to in either the Design Verification Terms & Conditions or the Prototype Services Terms & Conditions. In addition, such changes require the DV process to be started from the beginning, which results in extended DV schedules.

Customer Approval : _____ Date ____/____/____
Title : _____

14. SCS APPROVAL**Pre-Verification Comments**

SCS Approval : _____ Date ____/____/____
Regional Field Application Consultant

SCS Approval : _____ Date ____/____/____
Technical Support Team Leader