Final Report
Period Covered: 1 August 99 – 14 December 00

AASERT – 97 BMDO
Utilizing ISE-TCAD Software to Simulate Power MOSFET Devices Operating at Cryogenic Temperatures

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Grant No. F49620-97-1-0475
UCF Account number 16-26-511

April 13, 2001

REPORT DOCUMENTATION PAGE

AFRL-SR-BL-TR-01-

0337

1. AGENCY USE ONLY *(Leave blank)*

2. REPORT DATE

3. REPORT TYPE AND DATES COVERED
FINAL 15 JUN 97 TO 14 DEC 00

4. TITLE AND SUBTITLE
AASERT-97-BMDO UTILIZING ISE-TCAD SOFTWARE TO STIMULATE POWER MOSFET DEVICES OPERATING AT CRYOGENIC TERPERATURES

5. FUNDING NUMBERS
61103D
3484/TS

6. AUTHOR(S)
PROFESSOR CHOW

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
UNIV OF CENTRAL FLORIDA

8. PERFORMING ORGANIZATION REPORT NUMBER
F49620-97-1-0475

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
AIR FORCE OF SCIENTIFIC RESEARCH
801 NORTH RANDOLPH ST RM732
ARLINGTON, VA 22203-1977

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES
APPROVED FOR PUBLIC RELEASE, DISTRIBUTION UNLIMITED

12a. DISTRIBUTION AVAILABILITY STATEMENT

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

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14. SUBJECT TERMS

15. NUMBER OF PAGES

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

Utilizing ISE-TCAD Software to Simulate Power MOSFET Devices Operating at Cryogenic Temperatures

Research activities of AASERT-funded students

1. Robert Mauriello
2. Anabel Marcos

During the duration of the grant, Robert Mauriello completed his MS degree. Two papers are published (reprints attached). A copy of his MS thesis is also attached. Robert started working on his Ph.D. dissertation in 2000 but had to accept full time employment due to financial reasons. His Ph.D. study is on hold.

Robert Mauriello is now working for Motorola in Phoenix, Arizona. Anabel Marcos is continuing where Robert left off. Anabel is currently supported under an AFRL contract.

Both Anabel and Robert are U.S. citizens.

SIMULATION OF POWER MOSFET UNDER CRYOGENIC CONDITIONS

Robert Joseph Mauriello

ABSTRACT

There has been research in the past on electronics operation at cryogenic temperature, however here we present research by the use of simulation tools for the study power MOSFETs operating at cryogenic temperatures. Bt the use Integrated Systems Engineering Technical computer Aided Design software (ISE-TCAD), power MOSFETs were modeled and simulated under room temperature (300 K) and also Liquid Nitrogen Temperature (77 K). Power MOSFETs make an almost ideal candidate for operating at cryogenic conditions because of their high switching speeds, large breakdown voltage, and increase performance in on resistance.

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1 INTRODUCTION

Silicon power MOSFETs are important semiconductor devices used in a variety of high frequency power switching applications. These include power converters, telecommunication systems, lighting applications and medical electronics [1]. Power MOSFETs are also an integral part of high power silicon devices because of high input impedance, low forward voltage drop, and high switching speeds. In addition, advanced microwave applications utilize cryogenic systems for improved immunity to noise [2].

Over the last several years, low temperature studies on power MOSFETs have concluded that these devices make a very suitable choice for cryogenic conditions. Operating power

MOSFETs at cryogenic temperatures will lower the overall resistance of the device, as well as increase both electron mobility and the transconductance of the device [3].

The present work explores the operating characteristics of a power MOSFET under cryogenic conditions. The computer-generated model of the device was simulated using the semiconductor device modeling and simulation package from Integrated System Engineering (ISE) TCAD. Simulations of the device were performed for a range of parameter extraction results, and a comparison was performed of the simulated device at room temperature (300 K) and liquid nitrogen temperature (77 K).

Section 2 discusses the MOSFET concept and provides a brief comparison of the power MOSFET to that of the conventional MOSFET. Section 3 introduces the ISE-TCAD software and the physical models used in its simulation and analysis. The programs incorporated into TCAD are then explained and a summary of the overall device is developed. Section 4 is arranged into three parts in that it first utilizes the modeling equations and analyzes the important parameters at 300 K and at 77 K. We then simulate the base model of the power MOSFET under a variety of conditions, and present the tests performed for the power MOSFET at 300 K and 77 K. Then, we change the doping concentrations of key regions of the power MOSFET and compare the characteristics of each device to the base model.

Section 5 includes an attempt to design and fabricate the power MOSFET using the Class 100 clean room facility at the University of Central Florida. It describes the processes used, concentration distribution profiles, and a discussion on why the DMOS did not perform as expected. An ion implantation is currently carried out to fabricate the MOSFET.

2 POWER MOSFET PHYSICAL AND OPERATING CHARACTERISTICS

For power applications, the current handling capabilities of a conventional (lateral) MOSFET will not suffice. Therefore, the development of the power MOSFET was introduced to combat the situations of high current flow and power dissipation.

2.1 Physical Construction of the Power MOSFET

In contrast to the lateral MOSFET, a single diffused source and drain device, the power MOSFET (referred to as DMOS) is a double diffused device with the source and gate on the top of the substrate and the drain arranged on the backside of the substrate. Three distinct regions of the DMOS exist, the lightly doped n^- epitaxial layer, the p-type body region and the more heavily doped n^+ source region as shown in Figure 2.1. Vertical current flow is vital in a power device in order to utilize the silicon effectively and to reduce the device internal resistance to drain current flow [4]. Power devices require large drain and source areas to handle the current and power dissipation. Although first generation power MOSFETs utilized lateral technology, a high channel resistance resulted due to a long channel that was necessary in this type of construction. Modern power devices utilize vertical current flow, and thereby minimizing channel length considerations, an inherently low resistance is achieved.

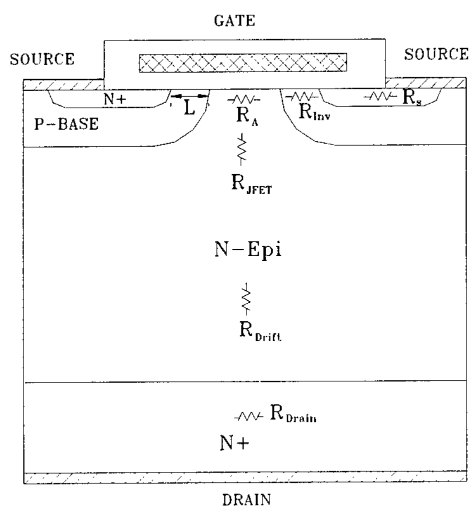

Figure 2.1 Cross-section of Power MOSFET Showing Resistance of Each Section

As previously mentioned, the DMOS is a double diffused process forming the p-type body region and n^+ source regions. In the DMOS, the distance between the highly doped source regions and the body regions, as shown in Figure 2.1, determine the channel length of the device.

2.2 Operation of the Power MOSFET

The basic operation of the DMOS is similar in some ways, but very different in others, to that of the lateral MOSFET. Like the lateral MOSFET, the power MOSFET is a voltage-controlled device whose output current can be controlled using very low gate drive voltage levels. The conductance of a semiconductor depends on the number and mobility of free carriers. Applying an electric field perpendicular to the current flow can modulate the number of free carriers, which directly affects the conductance. The voltage applied through a thin dielectric plate creates the electric field. This concept, which is the basic principle of operation of the Field Effect Transistor (FET), was proposed and patented in the 1920s and 1930s by Lilienfeld in the United States and Heil in England [5]. Forward current flow occurs for positive gate bias voltage of sufficient magnitude to create an inversion layer at the surface of the p-base region under the gate electrode. This inversion layer connects the n^+ source region to the n drift layer and provides a continuous path for the flow of electrons from the source to the drain, with the conventional current flow from the drain to the source. In the p-base region, the flow of electrons is lateral across the channel and vertical across the n^- drift region. This resultant channel is short as designated by the channel length (L) in Figure 2.1. Current is then conducted by the electrons from the source through the p-type body region (channel) into the epitaxial (n^-) region and downward into to drain of the DMOS. One concept the reader should notice is that the depletion region between the epitaxial (n^-) region and the p-type body region extends into the lightly doped epitaxial layer and does not spread into the channel, as does a conventional MOSFET. As a result, even with a short channel length, the breakdown voltage of the DMOS can be very high [6].

The DMOS's ability for large current handling capabilities is largely dependent upon the electron mobility of the device and the associated velocity saturation of charged carriers. When the DMOS is exposed to large gate voltages in power applications, a large electric field is created perpendicular to the channel length. The velocity of the charged carriers in turn obtains an upper limit of about 5×10^6 cm/s (electrons). This will result in a constant transconductance in the velocity saturation region of the drain current vs. gate voltage curve [7].

Power MOSFETs can be switched off by reducing the gate bias voltage to zero, that is, by externally shorting the gate electrode to the source electrode. When the gate voltage is removed, the electrons are no longer attracted to the channel and that breaks the conductive path from drain to source. This switching from on-state to off-state takes place rapidly without any delay from minority carrier storage and recombination that are experienced in bipolar devices. This turn-off time is controlled by the rate of removal of the charge on the gate electrode because this charge determines the conductivity of the channel.

There are parasitic n^+-p-n-n^+ bipolar transistors associated with the power MOSFET structure. This parasitic bipolar transistor is kept inactive by shorting the p-base region to the n^+ source regions to the source metal contact. The resistance between the p-base region between the shorts can become large and any lateral current flow in the p-base, due to capacitive currents can lead to forward biasing of the n^+/p junction at locations remote from the shorts. These currents can arise from the large time rate of change of voltage on the drain at high frequencies. Forward biasing of the n^+/p junction activates the parasitic bipolar transistor and leads to the initiation of minority carrier transport. This not only can slow down the switching of the power MOSFET but also can lead to second breakdown. Due to the high time rate of change of voltage in the high frequency applications, it is common practice to form the short in every cell and minimize the length of the n^+ source region from the edge of the channel to the short [8].

A conductive path is created across the p-base region underneath the gate by applying a positive voltage at the gate electrode for an n-channel device. The total resistance between the source and drain limits the current flow. This resistance consists of many components, which determines the on-state voltage drop when the device is carrying current. Figure 2.2 presents one half of the DMOS structure (due to symmetry), with different components of the total on-resistance shown. The resistance of the n^+ source ($R_n{}^+$) and substrate (R_{SUB}) regions is negligible for high voltage power MOSFETs that have high drift region resistance [9]. The channel resistance (R_{Inv}) and accumulation layer resistance (R_A) is determined by the conductivity of the thin surface layer induced by the gate bias. These are functions of the charge in the surface layer and the electron mobility near the surface. The drift layer contributes two components to the total on-resistance. The portion of the drift region that comes to the upper surface between the cells contributes a resistance (R_{JFET}) that is enhanced at higher drain voltages due to the pinch-off action of depletion layers extending from adjacent p-base regions. The main body of the drift region contributes a large series resistance (R_D) especially for high voltage devices. The on-resistance of a power MOSFET is the total resistance between the source and drain terminals when the device is turned on. The on-resistance determines the maximum current rating of the device. The power dissipation in the DMOS during current conduction is given by:

$$P = I_D^2 R_{ON} \tag{2.1}$$

This expression is based upon the assumption that the power MOSFET is operated in the linear region at a relatively small drain bias during current conduction. The total on-resistance of the power MOSFET is determined by all the resistive components where [8]:

$$R_{ON} = R_{n^+} + R_{Inv} + R_A + R_{JFET} + R_D + R_{SUB} \tag{2.2}$$

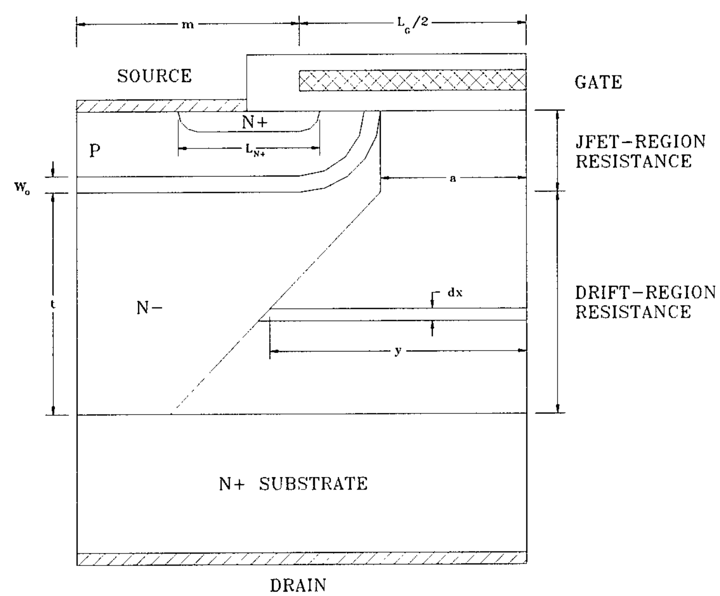

Figure 2.2 Cross Section of DMOS showing Design Dimensions

Resistance Due to the Source Diffusion

Figure 2.2 is the DMOS structure cross section, however, here the author has labeled some important physical parameters that are used in the determination of the above mentioned resistance associated with the DMOS. The commonly accepted model of specific source resistance is:

$$R_{n^+,sp} = \frac{1}{2}\rho_{Sn^+}L_{n^+}(L_G + 2m) \tag{2.3}$$

Referring to Figure 2.2, the term 2m is the cell diffusion window and L_G is the length of the gate electrode between the each adjacent cells, L_{n+} is the length of the n^+ source region, ρ_{Sn+} is the sheet resistance of the n^+ diffusion. Also, $(L_G + 2m)$ is the cell repeat spacing and specific on resistance normalizes the resistance to cm^{-2} [8].

Resistance due to the Inversion Channel

The specific on resistance that is due to the inversion channel is given by [8]:

$$R_{Inv,sp} = \frac{L_{ch}(L_G + 2m)}{2\mu_n C_{ox}(V_G - V_{th})} \tag{2.4}$$

Here, L_{ch} is the channel length of the device, μ_{nInv} is the inversion region electron mobility, C_{ox} is the oxide capacitance due to the oxide thickness, V_G is the applied gate voltage and V_{th} is the threshold voltage of the device.

Resistance due to Accumulation Layer

Assuming linear cell geometry, the accumulation layer resistance is given by [8]:

$$R_A = \frac{K(L_G - 2x_p)(L_G + 2m)}{2\mu_{nA}C_{ox}(V_G - V_{th})} \tag{2.5}$$

This resistance accounts for the current spreading from the channel into the JFET region and is dependent upon the charge in the accumulation layer and the mobility for free carriers at the accumulated surface. The term μ_{nA} is the accumulation region mobility, x_p is depth of the base region diffusion and the factor K accounts for the two dimensional nature of the current flow from the channel into the JFET region via the accumulation layer.

Resistance due to the JFET Region

The resistance of the drift region between the p-base diffusions is referred to as the JFET resistance because the current flow resembles that of a junction field effect transistor with the p-base regions acting as the gate regions. Here the JFET region resistance is given by [8]:

$$R_{JFET} = \frac{\rho_D (L_G + 2m)(x_p + W_o)}{L_G - 2x_p - 2W_o} \qquad (2.6)$$

Here the term W_o is the depletion layer extension as seen in Figure 2.2 and can be a significant fraction of the gate length L_G. Increasing the gate length can solve this problem, however, this can lead to poor channel density and a reduced cell breakdown voltage.

Resistance due to the Drift Region

In the drift region, the specific resistance is given by [8]:

$$R_{D,sp} = \frac{\rho_D (L_G + 2m)}{2} \ln\left(\frac{L_G + 2m}{L_G - 2x_p - 2W_o}\right) + \rho_D (t - m - x_p - W_o) \qquad (2.7)$$

where ρ_D is the drift region resistivity . Current spreads into the drift region from the JFET region as shown in Figure 2.2. One model to explain the current spreading in the drift region is based on the cross-section of the term a where:

$$a = L_G - 2x_p \quad (2.8)$$

With this in mind, the cross-section for the current flow then increases with the depth through the drift region.

The doping concentration of the epitaxial drain region affects the on-resistance of the power MOSFET. The heavier the doping concentration, the smaller the on-resistance becomes. Smaller on-resistance is favored for many switching applications, however, breakdown voltage is sacrificed. Breakdown voltage is also dependent upon epitaxial concentration. For an abrupt junction with doping concentration N, on the lightly doped side, the breakdown voltage of the device is given by:

$$V_{BD} = 5.34 \cdot 10^{13} N^{\frac{-3}{4}} \quad (2.9)$$

where V_{BD} is the breakdown voltage of the device for a plane junction and N is the doping concentration in cm^{-3} [10].

Although the junction between the p-type body and n^- epitaxial layer is not planer, the breakdown voltage approaches that of the plane junction. In the forward blocking state, the depletion layer of both ends of the p-body expands into the epitaxial layer beneath the gate oxide and overlap.

Low doping concentrations in the epitaxial layer must be low to maintain high breakdown voltage. However, low doping results in a low current density capability for a given electric field and is likely not to support high levels of channel current due to carrier drift velocity saturation.

Ideal Specific On-Resistance

In the ideal case where the resistance of the n^+ source, n^+ substrate, inversion channel region, accumulation region and the JFET region are negligible, the specific on-resistance of the power MOSFET will then be determined by the drift region alone. In addition, if it is assumed that the current flows uniformly through the drift region without current spreading effects, the resistance of the drift region is referred to as the ideal specific on-resistance for the power MOSFET. For n-channel devices ideal specific on-resistance is:

$$R_{on,sp} = \frac{W_D}{q\mu_n N_D} \tag{2.10}$$

where W_D is the width of the drift region conduction, and μ_n is the bulk electron mobility.

2.3 Threshold Voltage

The minimum gate voltage that is required to induce a channel is called the threshold voltage. It is an important design parameter for power MOSFETs. If it is large, a high gate bias voltage will be needed to turn on the power MOSFET. This might cause problems with the design of the gate drive circuitry. It is also very important that the threshold voltage not be too low. Due to the existence of trapped charges in the gate oxide, it is possible for the threshold voltage to be negative for n-channel power MOSFETs. This is an unacceptable condition because a conductive channel will now exist at zero gate bias voltage, i.e., the device will exhibit normally-on characteristics. Even if the threshold voltage is above zero for an n-channel power MOSFET, its value should not be too low because the device can then be inadvertently triggered into conduction. This can occur either by noise signals at the gate terminal or by the gate voltage being pulled up during high speed switching operations. Typical power MOSFET threshold voltages are designed to range between 2 and 3 volts. Threshold voltage can be expressed by:

$$V_{th} = \phi_{ms} - \frac{Q_i + Q_d}{C_{ox}} + 2\phi_f \tag{2.11}$$

ϕ_{ms} = work-function of the metal minus the work-function of the semiconductor.

Q_i = the total trapped charges that are associated to the gate oxide material.

C_{ox} = Capacitance due to the oxide layer.

Q_d = Electric charge relating the doping concentration to the depletion width.

ϕ_f = Fermi energy of the N-type region at the surface.

In general strong inversion (ϕ_s) occurs when the applied voltage causes the energy band of the semiconductor to bend by $2\phi_f$ where ϕ_f is the Fermi energy of the n-region at the surface (See Figure 2.3).

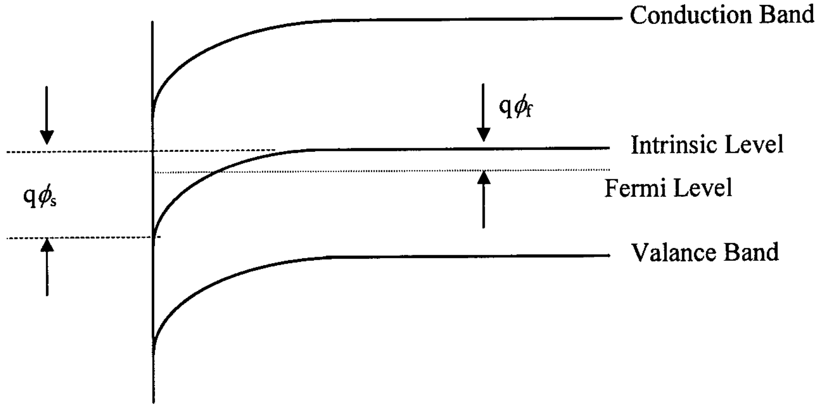

Figure 2.3 Band Gap at the Silicon-Silicon Oxide Interface Showing Inversion State

2.4 Power MOSFET Transconductance

Another very important factor that determines the power MOSFETs operating characteristics is the transconductance of the device. The transconductance is defined as:

$$g_m = \left[\frac{\Delta I_d}{\Delta V_g}\right]_{V_{DS}} \tag{2.12}$$

where $\Delta V_{GS}=V_{G3}-V_{G2}$. Another way to analyze this is recalling that drain current in the saturated region is:

$$I_{DS} = \frac{\mu_{ns} C_{ox} Z}{2L}\left(V_g - V_{th}\right)^2 \tag{2.13}$$

and differentiating this with respect to V_g yields:

$$g_m = \mu_{ns} C_{ox} \frac{Z}{L} \left(V_g - V_{th} \right) \quad (2.14)$$

A large transconductance is desirable to obtain a high current handling capability with low gate drive voltage, and for achieving high frequency response. In the saturated region, the output characteristics are controlled by the gate induced channel characteristics. The transconductance is, therefore determined by the design of the channel and gate structure.

3 INTRODUCTION TO ISE-TCAD AND MODELING EQUATIONS

The major focus of this thesis is the simulation and parameter extraction of the Power MOSFET (DMOS). The DMOS was designed and operational simulations were performed using the Technical Computer Aided Design software developed by Integrated Systems Engineering AG (ISE-TCAD). This is a popular semiconductor process, device and circuit simulator used by many major companies in the semiconductor industry. The latest version of ISE-TCAD, version 4.0, incorporates a graphical interface as well as having the ability to edit using a text editor. Both process and device simulations are sequenced in the operational window by utilizing drag and drop icons.

The ISE-TCAD software is a combination of many individual programs, which the user defines, in a particular order. Because ISE-TCAD has so many applications and uses, this discussion will only consider those programs used to design and simulate the operation of the DMOS.

3.1 ISE-TCAD Introduction

At the heart of ISE-TCAD is the main the TOOL FLOW EDITOR. The tool flow is in the windows operating environment, GENESISe and is the area of ISE-TCAD where all Process, Grid, Device and Visualization Tools are located. Generally speaking, any device simulation performed should be kept in the above order.

The first tool used in this simulation is the Grid Editor MDRAW-ISE. MDRAW-ISE is used for two-dimensional grid generation, mesh generation, impurity concentration information and refinement parameters supplied by the designer. MDRAW-ISE provides two major environments: the Boundary Editor and the Doping Editor. If the process simulator is used prior to the grid generation, then all of MDRAW's input parameters are automatically incorporated as a result of masks utilized and the process defined.

The Boundary Editor is a program composed by the user to define the physical dimensions of the semiconductor device to be simulated. These parameters include oxide layers, contacts, and the type of substrate used. Dimensions, in units of microns, are used in a coordinate system starting at a reference point of (0,0) to depict the physical characteristics of the device. In this file the user can assign virtually any commonly used substrate material such as silicon, polysilicon, or gallium arsenide, and any oxide layer such as silicon dioxide or silicon nitride.

Also within MDRAW-ISE is the Doping Editor that is a program used to characterize the profiles of impurity distribution including concentrations, boundaries, and type of impurity used. The Doping Editor can also incorporate Gaussian profiles, error function profiles, constant function profiles, and lateral diffusion. The user can assign dose, standard deviations, and junction depth, to more accurately depict real life conditions of diffusion. Also within this program, the user can define an optional refinement area to be analyzed under tighter dimensions. An example of this is the case of a MOSFET where the channel length is typically a few angstroms thick.

The next phase of the simulation is the operational simulation tool DESSIS-ISE. DESSIS-ISE is used for multidimensional Electro-thermal mixed-mode device and circuit simulation for semiconductor devices. Incorporated into DESSIS-ISE (which is a text editor) is DESSIN-ISE. DESSIN-ISE is the graphical interface for DESSIS-ISE, which consists of eight sections: Electrode, Thermode, File, Interface Conditions, Physics, Plotting, Math and Solve Parameters. Of these, the main emphasis is on the last five listed.

The Interface Conditions section is used to characterize interface charge conditions and recombination velocity. This is an optional section used for the insulation-substrate boundary of a device.

The Physics section is used to describe physical models to be used in the simulation. Here we describe mobility modeling, incorporating such things as doping dependence, high field saturation, and electric fields. The user can also incorporate oxide charge, carrier to carrier scattering, and methods of recombination (including Shockley-Reed-Hall-recombination, Auger recombination, and avalanche generation). Here the user also assigns one of the following keywords: "temperature", "thermodynamic" or "hydrodynamic", which will be used in the DESSIS-ISE program.

The Plotting section is used to designate the variables that are to be solved for in the DESSIS-ISE program and can be observed visually by PICASSO. Virtually, any variable conceived by semiconductor analysis can be observed including conduction current, hole and electron current/density, lattice temperature, electron and hole mobility, lattice temperature, electron and hole Joule temperature.

The Math section is used to specify the numerical methods in order to solve Poisson's equation, Electron equation and Hole equation. The user specifies the number of Newtonian iterations that are to be used to solve the above equations until the error between the iterations (default is 10^{-3}) is achieved.

The Solve section is used to specify what equations DESSIS-ISE is to solve and the method of solving. It is also used to describe a transient voltage condition or a quasi-stationary (ramping) voltage condition applied to a specified contact. For instance, transient and quasi-stationary conditions can be evaluated using a MOSFET device where the user can supply a constant gate voltage and vary the drain voltage to a specified value.

Finally, incorporated into the simulation is the graphical output programs used for parameter evaluation. For viewing the simulation results, INSPECT-ISE and PICASSO-ISE are used. INSPECT-ISE is a tool to display and analyze operational and transient outputs. PICASSO-ISE displays either two or three-dimensional semiconductor devices with color iso-bars showing the distribution of many parameters mentioned previously such as current density, mobility, Electro-static potential and temperature.

3.2 Modeling Equations of DESSIS-ISE

The DESSIS-ISE program is used to perform simulations based on Drift-diffusion, Thermodynamic and Hydrodynamic transport models. DESSIS-ISE will solve Poisson's equation, Electron current continuity equation and Hole current continuity equation, using the fully coupled Newtonian method until the specified accuracy has been achieved.

Transport Equations

DESSIS-ISE can be utilized to solve a variety of transport conditions. The three models used are drift-diffusion, thermodynamic and hydrodynamic. The Drift-Diffusion mode of simulation is used for isothermal simulation with stationary transport. The Thermodynamic model compensates for self-heating effects of the device. These two simulation models are suitable for devices with long active regions. The Hydrodynamic mode accounts for device self-heating and non-stationary transport effects. Devices with small active regions are suitable for this type of simulation. In this simulation, the Drift-Diffusion transport model was used. In the Drift-Diffusion model, Poisson's equation is

$$\nabla \bullet \varepsilon \nabla \psi = -q\,(p - n + N^{+}_{D} - N^{-}_{A}) \qquad (3.1)$$

Where ε is the electric permitivity of silicon, q is the elementary electronic charge, n and p are the electron and hole densities, and N_D^+ and N_A^- are the number of ionized donors and acceptors, respectively. The electron and hole continuity equations are as follows:

$$\nabla \bullet J_n = qR + q(\partial n/\partial t) \qquad (3.2)$$

$$-\nabla \bullet J_p = qR + q(\partial p/\partial t) \qquad (3.3)$$

Where R is the net electron-hole recombination rate and J_n and J_p are the electron and hole current densities given by:

$$J_n = -nq\mu_n(\nabla\phi_n) \qquad (3.4)$$

$$J_p = -pq\mu_p(\nabla\phi_p) \qquad (3.5)$$

Where ϕ_n and ϕ_p are electron and hole quasi-Fermi potentials. Also, μ_n and μ_p are the electron and hole mobilities. Using the Boltzman statistics,

$$n = n_{i,eff} e^{\frac{-q(\phi_n - \Psi)}{kT}} \qquad (3.6)$$

$$p = n_{i,eff} e^{\frac{-q(\phi_p - \Psi)}{kT}} \qquad (3.7)$$

where ϕ_n and ϕ_p are the n-side and p-side Fermi potentials, respectively, $n_{i,eff}$ is the effective intrinsic density, k is Boltzman constant, T is the temperature in Kelvin, and ψ is the electrostatic potential.

In addition to using the standard Drift-Diffusion model, DESSIS-ISE can also account for self heating effects by the use of the Thermodynamic model. In this model, once the electrostatic potential and the electron and hole densities have been found, the amount of heat generated within the device is also determined. This model takes into account electro-thermal effects under the assumption that the charge carriers are in thermal equilibrium with the lattice. Using this model, DESSIS-ISE can evaluate electron and hole Joule heat, recombination heat, and Thomson heat. As a result, equations (3.4) and (3.5) will be modified to:

$$J_n = -nq\mu_n (\nabla\phi_n + P_n\nabla T) \qquad (3.8)$$

$$J_p = -pq\mu_p (\nabla\phi_p + P_p\nabla T) \qquad (3.9)$$

Where P_n and P_p are the electrons and holes thermoelectric powers. DESSIS-ISE uses a default temperature of 300 Kelvin. However, in the Physics Section of DESSIS-ISE, a uniform lattice temperature can be incorporated.

The Hydrodynamic model utilizes the gradient of the carrier temperatures as an additional driving force for currents. This is useful for small active area devices such as submicron MOSFETs.

After DESSIS-ISE has solved Poisson's equation, electron current continuity equation and Hole current continuity equation, a print-out will be generated by the program to show electron, conduction and hole currents over a specified range of voltages. Once the DESSIS-ISE and MDRAW programs have been completed, the user can then execute PICASSO-ISE. PICASSO-ISE is an interactive visualization tool that utilizes the data from DESSIS-ISE and M-Draw to develop high quality pictures of the simulated semiconductor device.

Band Gap and Band Gap Narrowing Model

For intrinsic Silicon, the band gap of the material is expressed as:

$$E_g(T) = E_g(0K) - \frac{\alpha T^2}{T + \beta} \tag{3.10}$$

Where $\alpha = 4.73 \cdot 10^{-4} \frac{eV}{K}$ and $\beta = 436K$. Included in this is a choice for the model used for Band Gap at 0 Kelvin. These models will be discussed further in the next section.

Based on physical measurements of the quantity $\mu_n n_i^2$ in n-p-n transistors with different base doping concentrations and a one-dimensional model for the collector current, so called "apparent band gap narrowing" models have been suggested by Slotboom and de Graaff for p-type materials where [11]:

$$\Delta E_g(N_A) = E_{BGN}\left[\ln\left(\frac{N_A}{N_{REF}}\right) + \sqrt{\left(\ln\left(\frac{N_A}{N_{REF}}\right)\right)^2 + 0.5}\right] eV \tag{3.11}$$

Where $E_{BGN} = 0.009eV$ and $N_{REF} = 10^{17}$ cm^{-3}, and N_A is the acceptor concentration.

Effective Intrinsic Density Model

The intrinsic carrier density of undoped silicon is given by [12]:

$$n_i(T) = \sqrt{N_c(T)N_v(T)e^{-\frac{E_g(T)}{2kT}}} \tag{3.12}$$

Here, the Effective Densities of States $N_c(T)$ and $N_v(T)$ are:

$$N_c(T) = \frac{2}{h^3}\left(2\pi m_e^* kT\right)^{\frac{3}{2}} \tag{3.13}$$

$$N_v(T) = \frac{2}{h^3}\left(2\pi m_h^* kT\right)^{\frac{3}{2}} \tag{3.14}$$

Here m_e^* and m_h^* are the effective electron and hole mass respectively and h is Planck's constant.

Incomplete Ionization

In silicon, all dopants are usually ionized at room temperature because the impurity levels are sufficiently shallow. In the case of cryogenic conditions, donor and acceptor levels of boron and phosphorus are relatively deep compared to the thermal energy kT/q at room temperature. Therefore, incomplete ionization of the impurity atoms occur, which is given by:

$$N_D^+ = \frac{N_D}{1 + g_c \exp\left(\frac{E_{fn} - E_D}{kT}\right)} \tag{3.15}$$

$$N_A^- = \frac{N_A}{1+\frac{1}{g_v}\exp\left(\frac{E_A - E_{fp}}{kT}\right)} \qquad (3.16)$$

here, the donor and acceptor impurity level must be taken into account in Poisson's equation. The donor and acceptor levels are given by:

$$E_D = E_{D_o} - \alpha N_i^{\frac{1}{3}} \qquad (3.17)$$

$$E_A = E_{A_o} - \alpha N_i^{\frac{1}{3}} \qquad (3.18)$$

where E_D and E_A are the donor and acceptor impurity energy levels, respectively. Refer to Appendix 1 for the constants used in the above equations.

Mobility Models

In DESSIS-ISE, mobility is modeled in modular components. The high field mobility is a function of the low field mobility and a driving force. The low field mobility is dependent on three groups of other mobilites: bulk mobility (μ_b), surface contributions (μ_{sr}) and contributions made by carrier to carrier scattering (μ_{eh}) where:

$$\frac{1}{\mu_{low}} = \frac{1}{\mu_b} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_{eh}} \qquad (3.19)$$

The bulk mobility model is a temperature dependent constant where:

$$\mu_{const} = \mu_L \left(\frac{T}{300}\right)^{-\zeta} \qquad (3.20)$$

Here μ_L is the lattice mobility and is equal to, μ_L=1417 cm^2/Vsec and ζ=2.5 for electrons and μ_L=470.5 cm^2/Vs and ζ=2.2 for holes [13]. Mobility is also dependent on the doping of the material and is adversely effected by heavily doped materials. Impurity scattering is well described by the bulk mobility model of Masetti, et al. [14], which extends the Caughey-Thomas expression [15] to the heavy doping range where:

$$\mu_{dop} = \mu_{\min 1} e^{-\frac{P_c}{N_i}} + \frac{\mu_{const} - \mu_{\min 2}}{1+\left(\frac{N_i}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1+\left(\frac{C_s}{N_i}\right)^{\beta}} \tag{3.21}$$

Refer to Appendix 1 for a complete listing of the constants used above. This model can be used in the concentration range 10^{13} to 4×10^{21} cm^{-3}.

Surface contributions are also taken into account when modeled because mobility degrades at interfaces, like in the MOSFET channels, and is accounted for in the Lombardi, et al, model [16]. This model combines surface phonon scattering and surface roughness scattering ("sr") with the bulk mobility ("b") from equation 3.15

$$\mu_{ac} = \frac{B}{F_{\perp}} + \frac{C\left(\frac{N_i}{N_o}\right)^{\lambda}}{F_{\perp}^{\frac{1}{3}}\left(\frac{T}{T_o}\right)} \tag{3.22}$$

$$\mu_{sr} = \frac{\delta}{F_{\perp}^{2}} \tag{3.23}$$

Here, μ_{ac} and μ_{sr} are functions of total doping concentration, N_i and $F_{\perp}$ are components of the electric field normal to the silicon-silicon oxide interface. Again, all parameters are found in Appendix 1.

When the drift-diffusion model is used, velocity saturation is modeled in DESSIS-ISE according to Canali, et al. [17]. This model originates from the Caughey-Thomas model [15], but has temperature dependent parameters where:

$$\mu(F) = \frac{\mu_{low}}{\left[1+\left(\frac{\mu_{low}F}{v_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}} \tag{3.24}$$

The parameters are listed in Appendix 1. The driving force (F) describing the high field velocity saturation can be the parallel component of the electric field or the gradient of the quasi-Fermi level. β and v_{sat} are defined as:

$$\beta = \beta_o \left(\frac{T}{T_o} \right)^{\beta_{\exp}} \tag{3.25}$$

$$v_{sat} = v_{sat,o} \left(\frac{T}{T_o} \right)^{-v_{sat,\exp}} \tag{3.26}$$

For the constants used in this model refer to Appendix 1.

These are the majority of temperature dependent terms that are accounted for in the ISE-TCAD software. Each of these models can be incorporated into the simulations by designating the appropriate key words in the DESSIS-ISE portion of the program.

4 POWER MOSFET SIMULATIONS AT ROOM AND CRYOGENIC TEMPERATURES

This section consists of two parts. Firstly, it analyzes some important operating parameters of power MOSFETs when exposed to cryogenic conditions; and second, it utilizes ISE-TCAD software to run simulations on a power MOSFET operating at room temperature (300K) and cryogenic temperature (77K) with these conditions taken into account. Section 4.1 utilizes the equations set forth by ISE-TCAD software as described in Section 3 and simulations are performed on the equations to determine the validity of the equations and to gain an understanding of what happens to these parameters under cryogenic conditions. Section 4.2 then uses ISE-TCAD software to run simulations on a basic model using ISE-TCAD in order to solve for a variety of results. Section 4.3 then changes both epi-layer concentration and base concentration for an analysis of operating characteristics and compares these to the basic model.

There are many advantages to operating electronics at cryogenic conditions such as an increase of electron mobility and as a result, a decrease in on-resistance and increase in transconductance. However, some disadvantages include an increase in threshold voltage and decrease in breakdown voltage. Simulations were conducted to determine the change incorporated with these parameters as well as an attempt to optimize the device at 77 K.

For both the physical parameter evaluation and the operating analysis, a base line DMOS was developed based on the parameters set forth by the ISE-TCAD model that is supplied with their software. Figure 4.1 is a cross section of the device using MDRAW-ISE. The channel length of the device is 2 μm and a gate oxide thickness of 700 Angstroms. The epi-layer is lightly doped Phosphorous (n^-), doped at $2x10^{14}$ cm^{-3} and the background bulk material is highly doped Phosphorous (n^+), doped at $1x10^{19}$ cm^{-3} and is 5 μm thick. Diffused into the epi-layer are two Boron ion-implanted (p) base regions displaying a gaussian profile with a lateral diffusion coefficient of 0.8, surface concentration at $5x10^{16}$ cm^{-3} and a junction depth of 2 μm. Diffused within the two Boron wells are two highly doped phosphorous wells (n^+) with surface concentration of $1x10^{19}$ cm^{-3}, a junction depth of 0.6 μm with a junction concentration of $4x10^{18}$ cm^{-3}. As defined in Section 2, the channel length of the device is the distance between the n^+ source region and the p base region where inversion occurs. In this instance, the channel length is 2 μm. The cross section of colors throughout each region is an indication of total impurity concentration with red indicating the concentration of n type material to blue indicating the concentration of p type material per the pallet in the bottom right hand corner of the cross section. As explained in Section 2, M-DRAW is that part of ISE-TCAD used to define each of the regions including doping profile. See Appendix 2 for the M-DRAW-ISE command file used to generate this device.

4.1 Cryogenic Conditions on Parameters of the DMOS

In this section, we will analyze the modeling equations that ISE-TCAD uses to perform the simulations of devices. Here we study five important physical properties of the power MOSFET, and how these are affected by cryogenic conditions. These properties include Band Gap and Band Gap Narrowing Effects, Intrinsic Carrier Concentration, Ionized Impurity concentration, electron mobility, and threshold voltage.

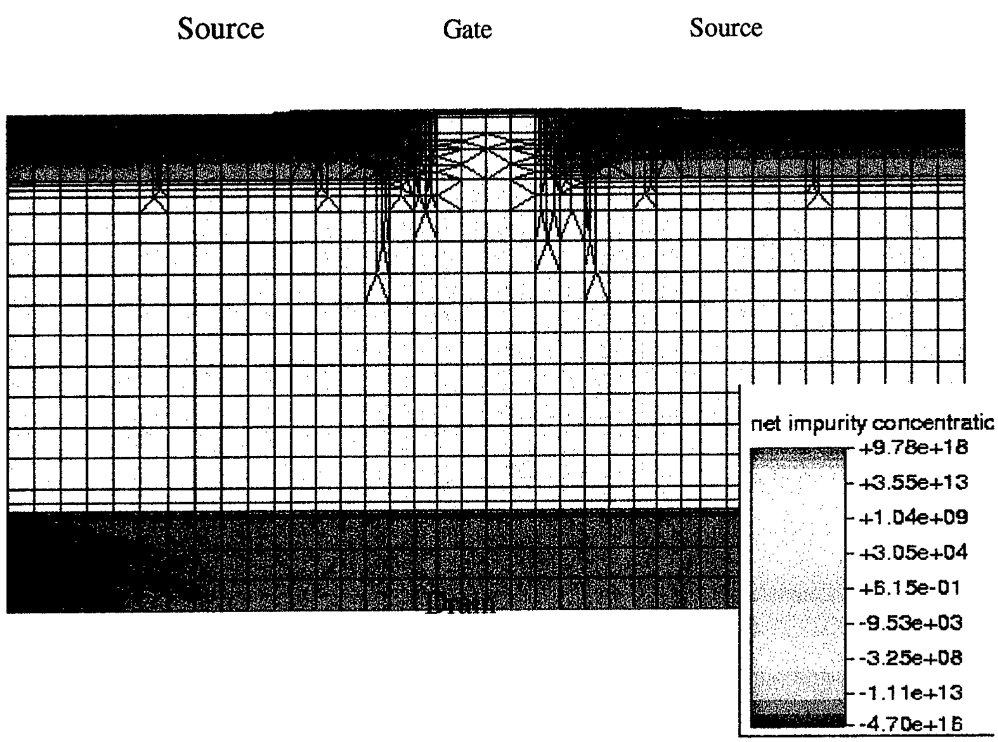

Figure 4.1 Cross Section of the DMOS Using MDRAW-ISE

Cryogenic Effects on Band Gap and Band Gap Narrowing

The models that are used to compare the effects of LNT are the band gap model, the Intrinsic Carrier Concentration model, the Incomplete Ionization model and the Mobility model as discussed in Section 3. In this section, we will show how the above parameters change with temperature for the device described above.

The band gap model, as discussed in Section 3, is dependent upon temperature, as shown in Figure 4.2. This figure is a graphical representation of how band gap changes as temperature is reduced per equations 3.10 and 3.11. It also represents the comparison of the band gap of intrinsic silicon to silicon doped with concentrations of the three major regions of the DMOS, meaning the drift region, base region, and source region. Band gap shifts from 1.095 eV to 1.036 eV for all concentrations except $1x10^{19}$ cm^{-3}, which is the highly doped source region. For a concentration of $1x10^{19}$ cm^{-3}, band gap shifts from an initial value of 1.012 eV at 300 K to 1.053 eV at 77 K. At such a high doping concentration, the on set of degeneracy and the narrowing of the band gap are related to the now concentration depended density of state function. Meanwhile, the band gap narrowing on the other lighter doping concentrations are not affected by band gap narrowing.

Cryogenic Effects on Intrinsic Carrier Concentration

In the absence of a dopant, the resistivity is controlled by the creation of electrons and holes in the conduction and valence band due to the thermal generation process, which allows the transfer of electrons from the valence band into the conduction band. This process produces both a free electron and a free hole, which can take part in current conduction [18]. The density of these intrinsically created carriers is dependent upon the density of states in the conduction (N_C) band and valence band (N_V) as referred to in equation 3.12 where N_C and N_V are defined per equations 3.13 and 3.14, respectively. Figure 4.3 shows how intrinsic carrier concentration changes as the material is exposed to cryogenic conditions for each of the three regions of the DMOS. There is very little difference between all regions except that of the source concentration at $1x10^{19}cm^{-3}$. Referring back to equation 3.12:

$$n_i(T) = \sqrt{N_c(T)N_v(T)}e^{-\frac{E_g(T)}{2kT}} \qquad (4.1)$$

Here, intrinsic concentration is proportional to the band gap and temperature. When heavily doped, the intrinsic concentration is displaying the effects of band gap narrowing as discussed,

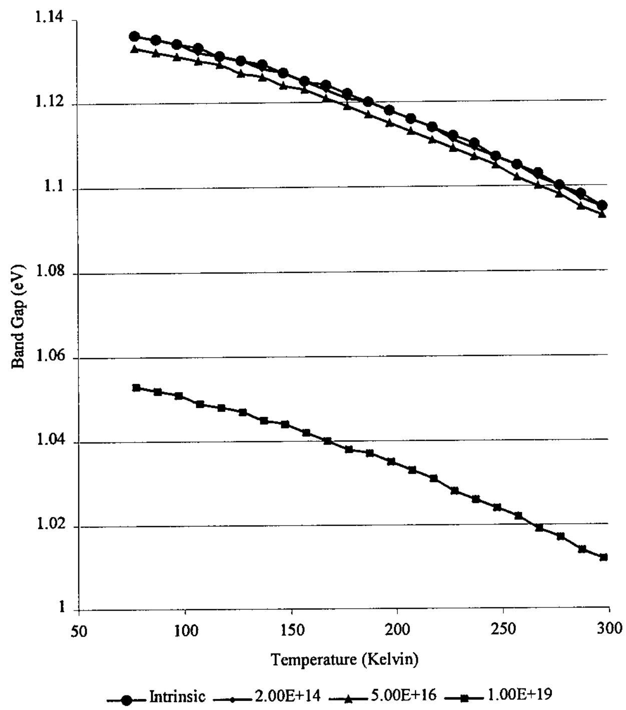

Figure 4.2 Plot of Band Gap and Band Gap Narrowing Effects at Different

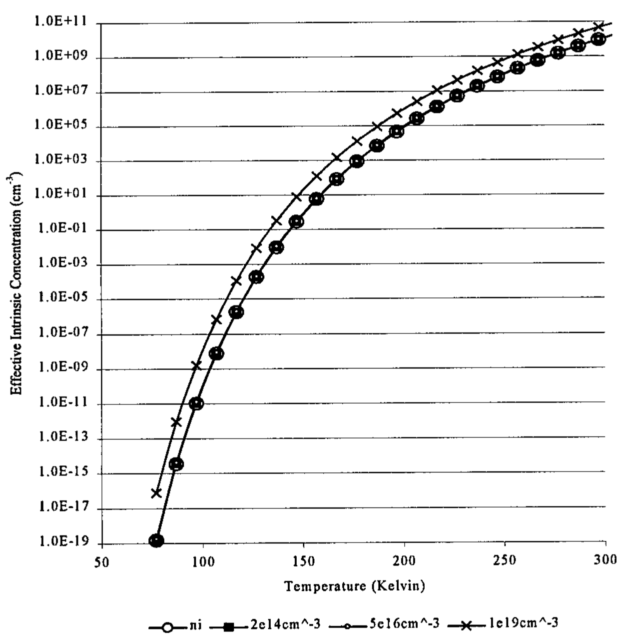

Figure 4.3 Plot of Effective Intrinsic Concentration v. Temperature

Hence, its curve has been shifted up slightly. It would then follow that since the overall effect of intrinsic carrier concentration is, that as the temperature of the lattice decreases so does the intrinsically created carriers due to thermal generation. But in the case where the dopant is of a high concentration, the effective band gap decreases; therefore, there exists a greater chance for electrons and holes to become thermally generated.

Cryogenic Effects on Ionized Impurity Concentrations

Low temperature operation of silicon devices is also dependent upon the number of charge carriers in neutral and depletion regions. The number of carriers in the neutral region is one factor that determines the on-resistance of the device, while the number of ionized donors in the depletion region determines the breakdown voltage of the device [19].

At low temperatures, there is a reduction in the amount of ionized acceptor and donor charge carriers in the bulk silicon. This phenomenon is referred to as carrier freeze-out. The concentration of non-ionized donors in an n-type material is given by

$$N_{Non-Ion} = \frac{N_D}{1+\frac{1}{2}\exp(\frac{E_{fn}-E_D}{KT})} \tag{4.2}$$

Where N_D is the total impurity concentration, E_{fn} is the electron Fermi level and E_D is the effective impurity donor level. The total ionized donor concentration in the neutral region is derived using the charge neutrality condition in a purely n-type material:

$$N_i = N_C\left[\frac{\sqrt{1+8\exp[\frac{E_C-E_D}{KT}]\frac{N_D}{N_C}}-1}{4\exp\left(\frac{E_C-E_D}{KT}\right)}\right] \tag{4.3}$$

In Figure 4.4, the total ratio of ionized donors to that of total available donors is plotted versus temperature. Here, we see again that all three regions of doping are plotted versus temperature. Included in this plot is a concentration of $1\text{x}10^{18}\text{cm}^{-3}$ which is used for dopant dependent clarification. Notice that at $1x10^{19}cm^{-3}$, the ratio of ionized donors takes on a completely different profile than that at $1x10^{18}cm^{-3}$. In the first three plots, the characteristics of ionized impurity concentration vs. temperature take on basically the same shape. It is worth noting that according to this carrier freeze-out formulation for phosphorus in silicon doped at $5x10^{16}cm^{-3}$,

although 90% of donors are ionized at 150 K, only 20% remain ionized at 77 K. Thus, the on-resistance of the power MOSFET operating at LNT is not related by the formulation that at room temperature 100% ionization of donors occur. Making the statement "Incomplete Ionization" compensates for this in the Physics Section of the DESSIS-ISE file.

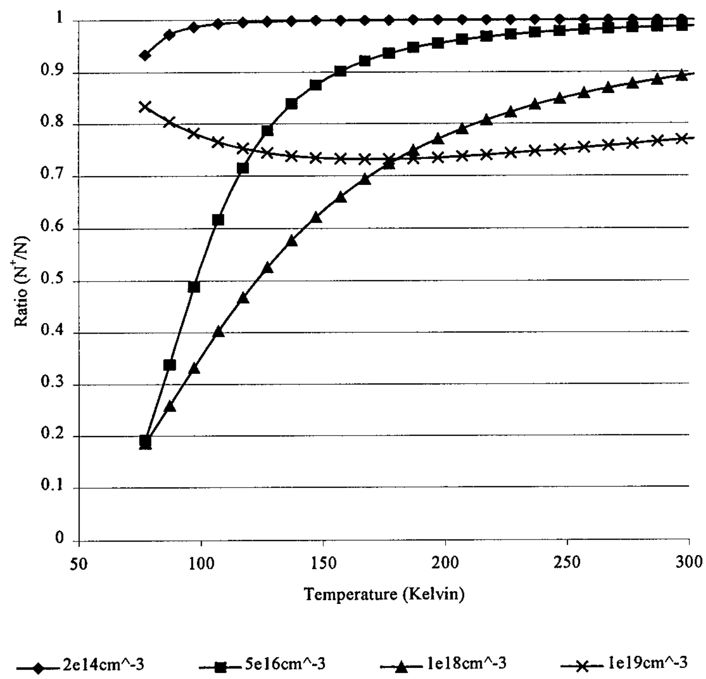

Figure 4.4 Plot of the Ratio of Ionized Donors to Total Available Donors versus Temperature

Cryogenics Effects of Mobility

In general terms, the mobility is the ease of the electrons (or holes) to drift through the material. The mobility can be defined as the average particle drift velocity per unit electric field [20]. Where:

$$\mu_n = -\frac{\langle v_x \rangle}{\vec{E}} \tag{4.4}$$

where E is the electric field and v_x is the average drift velocity through the lattice.

Two basic types of scattering mechanisms that influence mobility through a lattice structure are impurity scattering and lattice scattering (phonon scattering). The first is impurity scattering where, as thermal energy of the impurities decreases, ionized impurity scattering increases due to the lower carrier thermal velocity. The other is the decrease in lattice scattering (or phonon scattering) as the temperature decreases. The net effect on mobility depends on which of the two scattering effects are dominant. Lattice scattering dominates when temperature in the lattice is greater than 50 K; carriers through a crystal lattice are scattered by the vibration of the lattice structure. In this temperature range mobility is proportional to $T^{-3/2}$. As temperature decreases, mobility will increase. As a result, semiconductor devices such as MOSFETs will have a greater mobility at cryogenic temperatures as compared to room temperature.

Hill and other researchers reported the effect of negative temperature dependence on mobility [21]. The drift region mobility was found to decrease below 50 K, which accounts for the increase of on-resistance, and may be attributed to localized electron traps where the electric field is insufficient to ionize the trapped carriers. From this study, a comparison was performed to evaluate the relative importance of the component of the devices resistance. Mazzoni indicates that the n-drift resistance is by far the most important component at 300 K, while at temperatures below 77 K, the enchantment area and JFET area resistance tends to become more important [22]. This resistance is proportional to the semiconductor resistivity and so is also inversely proportional to mobility and has similar temperature characteristics.

In Section 3, we discussed the equations used by ISE-TCAD in the modeling of mobility in silicon. Figure 4.5 is a plot of bulk mobility as a function of temperature based on the dopant dependent mobility model, presented in equation 3.16. Included in this graph is that of the heavy doping model as presented in equation 3.17. Dopant types have been taken into account for the different regions of the DMOS per Appendix 2. The results plotted in Figure 4.5, however, do not compensate for the high electric field effects of the inversion channel and also the silicon/silicon oxide roughness compensation, as presented in Section 3. For all simulations using ISE-TCAD, these compensations were taken into account.

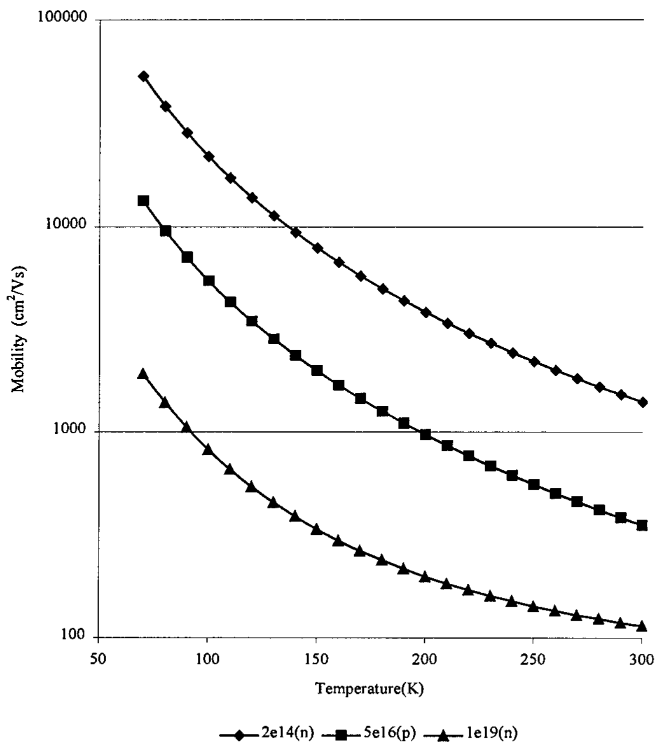

Figure 4.5 Plot of Doping Dependent Mobility vs. Temperature at each Dopant Region

In order to show the overall effect of temperature's relation to mobility, refer to Figure 4.6, which is a plot of the dopant concentration dependent mobility as a function of dopant concentration for both n and p type material at 77K and 300K.

As discussed in Section 2, the total on-resistance is:

$$R_{on} = R_{n^+} + R_{ch} + R_a + R_j + R_D + R_s \tag{4.5}$$

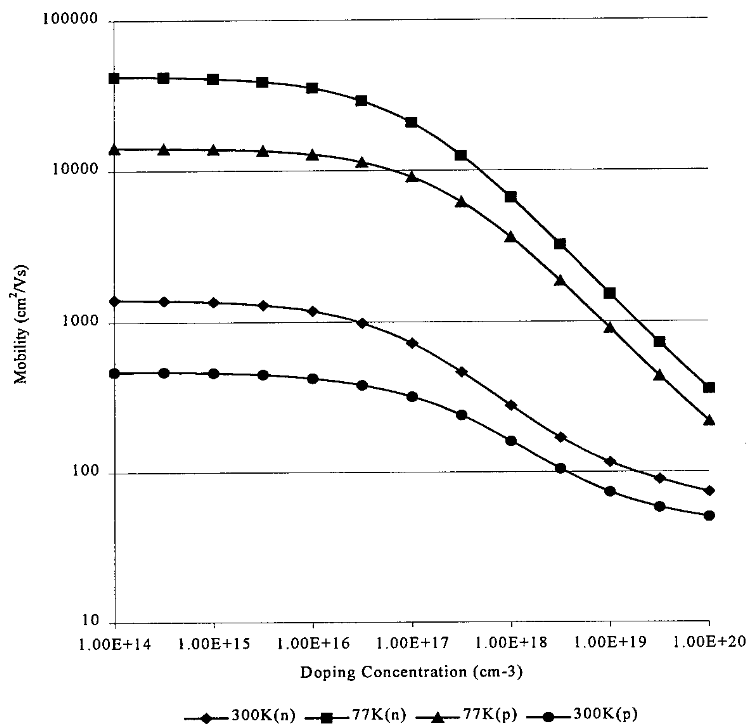

Figure 4.6 Plot of Dopant Dependant Mobility vs. Dopant Concentration at 77K and 300K for both n and p Type Dopant

and associated with each of these regions of resistance is the associated mobility. For a specific device, the mobility associated with the body inversion under the drain is that the inversion layer mobility can be modeled as:

$$\mu_{ns}(T) = C_1\left(\frac{T}{300}\right)^{-1.26} \tag{4.6}$$

Where T is the lattice temperature and C_1 is some constant associated with a particular device for curve fitting purpose [23]. After the current flows through the inversion layer, it passes through the accumulation layer that is directly under the gate into the epi-layer of the device. Therefore, the accumulation layer mobility can be modeled with the following expression:

$$\mu_{nA} = C_2\left(\frac{T}{300}\right)^{-0.81} \tag{4.7}$$

Here C_2 is some constant associated with the particular device for curve fitting [24].

The bulk mobility (μ_{nB}) term is constant in both the JFET resistance and the drain resistance and has been measured by Jacoboni, et al. [25], based on his results:

$$\mu_{nB} = C_3\left(\frac{T}{300}\right)^{-2.42} \quad \text{for T} \geq \text{ 200 K,} \tag{4.8}$$

$$\mu_{nB} = C_4\left(\frac{T}{200}\right)^{-2.00} \quad \text{for 77 K} \leq \text{T} \geq \text{200 K} \tag{4.9}$$

Based on Singh and Baliga [26], the values of C_1-C_4 are 357,757,1350 and 3601, respectively. Figure 4.7 is a plot of the mobility of each region as a function of temperature. In this example, bulk mobility has the greatest mobility throughout the whole range in temperatures, ranging from 1400 cm^2/Vs at 300 K and obtaining almost 25000 cm^2/Vs at LNT. This explanation is for a specific device where the data was taken and the mobility was fitted for that device. Here, it is used as an extra example of mobility variations with temperature, where each coefficient is used for curve fitting purposes.

Specific on Resistance Comparisons

The specific on resistance as from equation 2.10 says:

$$R_{on,sp} = \frac{W_D}{q\mu_n N_D} \tag{4.10}$$

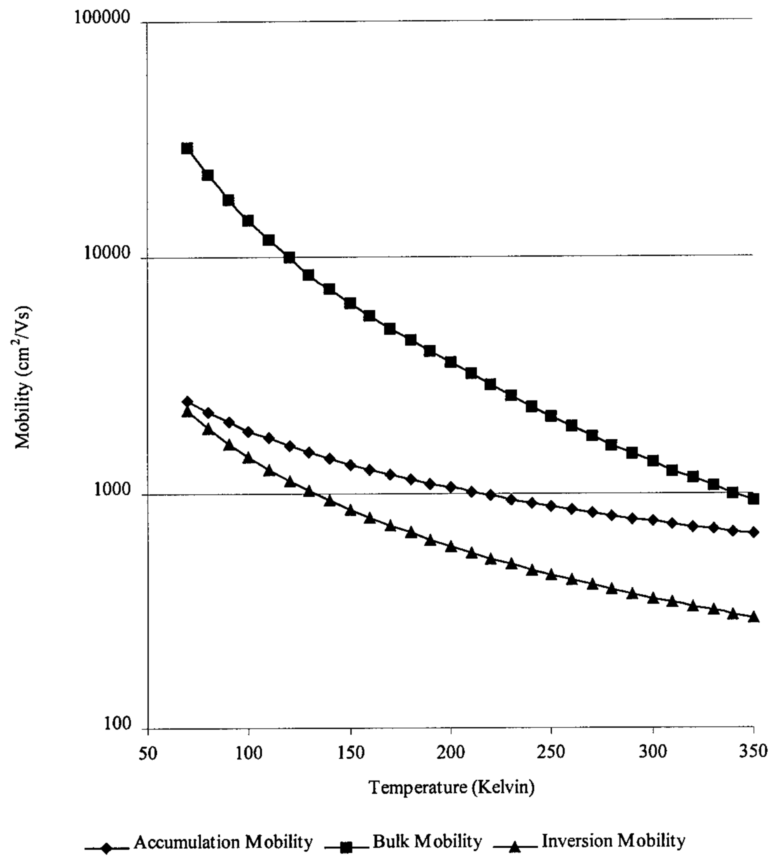

Figure 4.7 Plot of Three Region of DMOS Mobility versus Temperature

Here W_D is the drain width and assumes that the majority of the on resistance of the device is due to drift resistance (R_D). Substituting into equation 4.8 in terms of critical electric field, the specific on resistance now becomes:

$$R_{on,sp} = \frac{4BV^2}{\varepsilon_s E_c^{\ 3} \mu_{nB}} \qquad (4.11)$$

Here, BV is the designed breakdown voltage of the device and E_c is the critical electric for the device. Figure 4.8 is a plot of specific on resistance vs. temperature at breakdown voltage of 1000V, 700V and 500V. As temperature decreases, on resistance is improved because it is

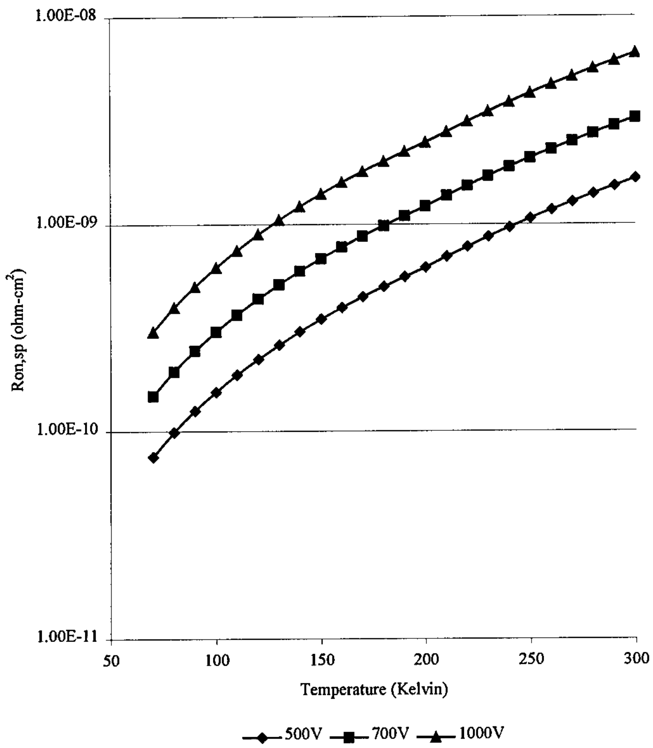

Figure 4.8 Plot of Specific on Resistance vs. Temperature

mainly determined by the temperature dependent bulk mobility associated with the drain region on resistance [27]. Figure 4.9 is a plot of specific on resistance vs. breakdown voltage for 300K and 77K. From this and the preceding graphs, it is assumed that the drift region mobility is in the order of $1\text{x}10^{14}$ cm^{-3} to $1\text{x}10^{16}$ cm^{-3} to model the mobility solely as temperature dependent and not dependent upon dopant concentration. Referring back to Figure 4.6, this assumption is valid for the range of drift concentration required. Here, we show that specific on resistance decreases as breakdown voltage decreases, however breakdown voltage is inversely dependent upon drain region concentration. From the two graphs, you see that there is a trade off between low on resistance and high breakdown voltage as related to the epi-layer dopant concentration. In general, for power devices, the higher breakdown voltage is desired especially when the device is required to block large reverse biased voltages. However, in either case, on resistance decreases drastically when the device is exposed to cryogenic conditions.

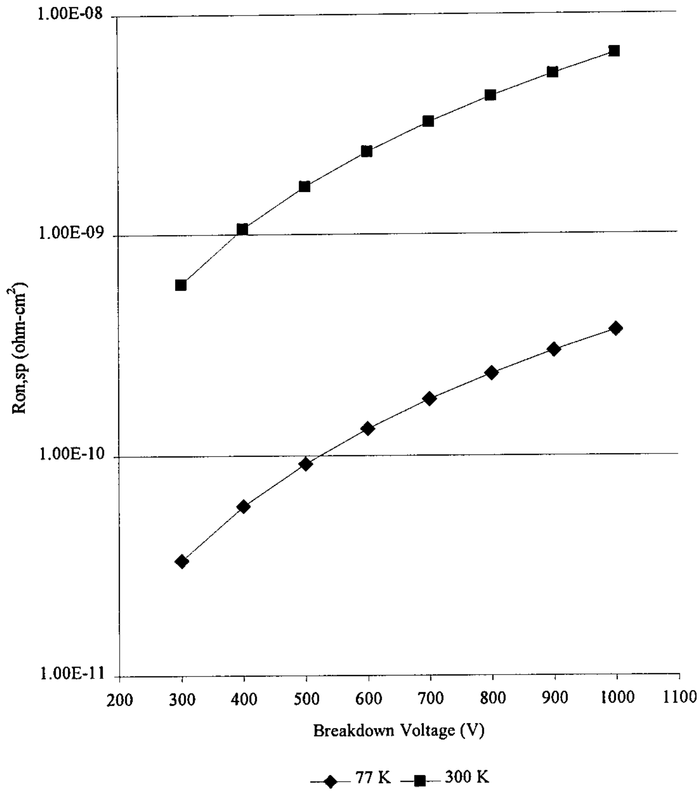

Figure 4.9 Plot of Specific On Resistance vs. Breakdown Voltage at 77K and 300K

4.2 ISE-TCAD Simulations at Room and Cryogenic Temperatures of Basic Power MOSFET Model

As discussed at the beginning of this Chapter, this section will primarily involve the simulation of the power MOSFET using ISE-TCAD as the primary means of simulation and graphical results. The scope of this section is to determine more specifically, the operating characteristics of the device using the results from INSPECT-ISE and PICASSO-ISE. Refer to Appendix 2 for the MDRAW-ISE command file used in the dopant profile and physical dimensions of this base line DMOS.

Threshold Voltage of the Device at Room and Cryogenic Temperatures

As the temperature of the device decreases, the threshold voltage will shift to a higher voltage. This is mainly due to a large decrease in intrinsic carrier concentration from 300K to 77K. A low intrinsic carrier concentration increases the band bending in the p-base region, which needs to be compensated for by a higher gate voltage for the inversion layer to occur. The impurity atoms in the p-base region remain almost completely ionized in the presence of the large electric field, so that the threshold voltage is determined by the total acceptor concentration even at low temperatures in spite of the freeze out effects [28]. To demonstrate this, applying a very small drain voltage (0.1V) simulated the device for threshold voltage measurements. The gate voltage was ramped from 0V to 3V and the output drain current was monitored. Figure 4.10 is a plot of the square root of drain current vs. applied gate voltage. According to these results, the

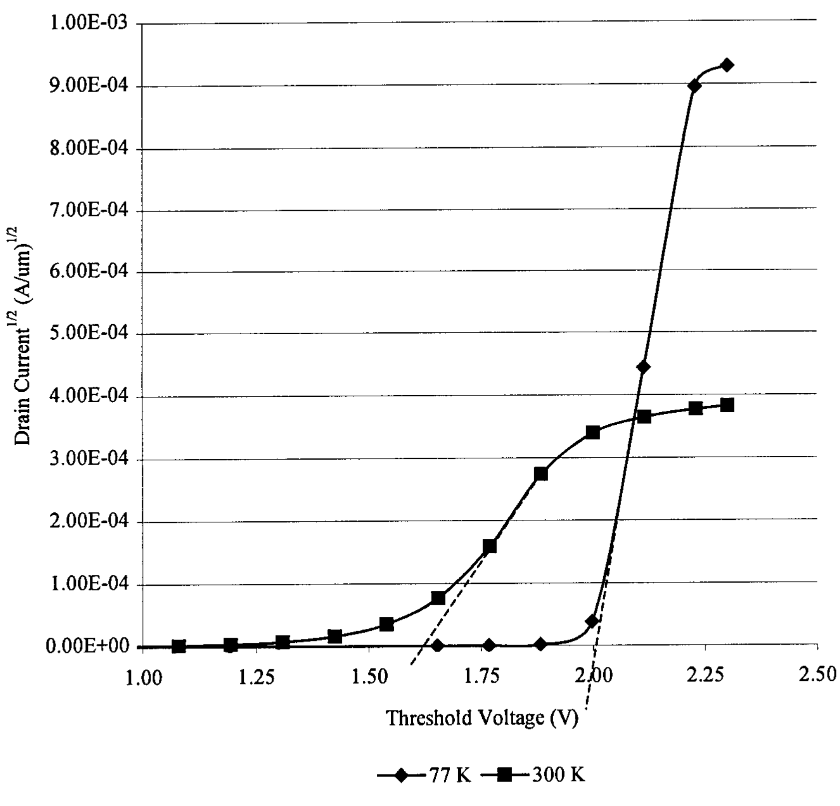

Figure 4.10 Plot of Threshold Voltage at 77K and 300K

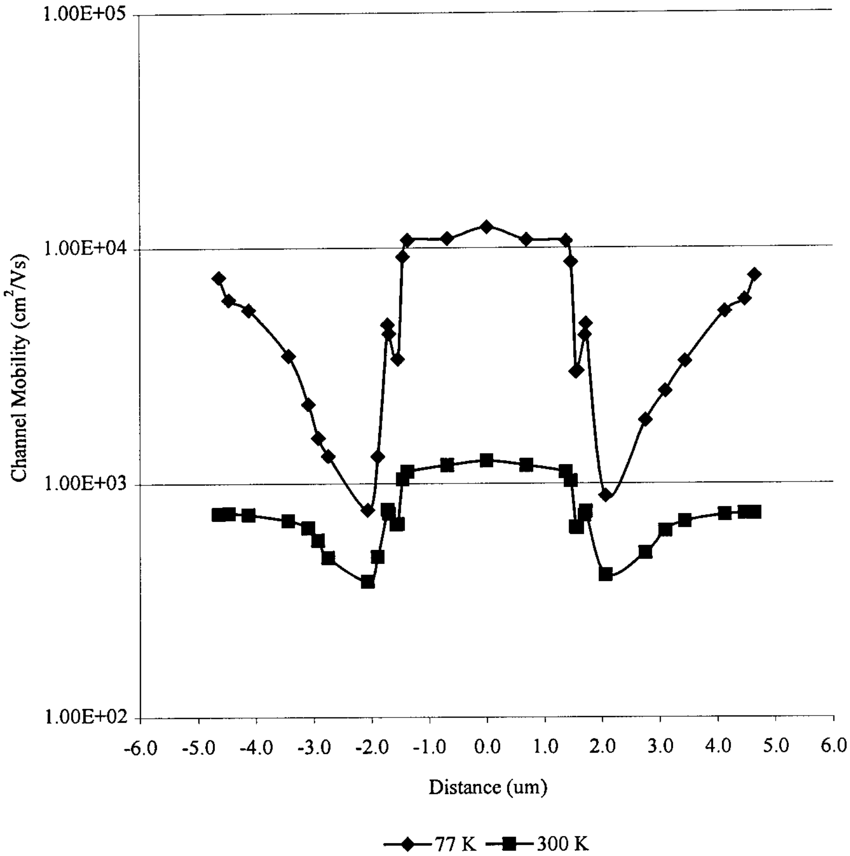

Figure 4.11 Plot of Electron Mobility Across the Gate at 77 K and 300 K

threshold voltage of the device at 300 K is 1.6 V, where at 77 K, the threshold voltage shifts up slightly to 2.0 V. To understand the mechanics of what is happening under the base region, Figure 4.11 is a plot of electron mobility directly under the surface and across the oxide along the x-axis. Here, you can see that electron mobility has increased by a factor of 10. This graph also demonstrates the decrease in mobility through the inversion channel. The units in the x-axis are in microns and correspond to the scale in reference to Figure 4.13.

Drain Current Characteristics of the Device Including Specific On Resistance Measurements

Here, the operating characteristics of the device are simulated in order to gain an understanding of what happens to the current vs. voltage profile, the breakdown voltage profile and the electron current density. Figure 4.12 is a plot of drain current vs. drain voltage at a gate voltage of 3 V for both 77 K and 300 K. Recalling that drain current is dependent on the drift region mobility, drift region mobility increases as temperature decreases as explained in Figure 4.7 and this plot is a direct result. Saturated drain current increases from 7.6×10^{-6} Amp/μm to 2.6×10^{-5} Amp/μm. This corresponds to drain current increasing by a factor of 3.4 at 77 K compared to that at 300 K.

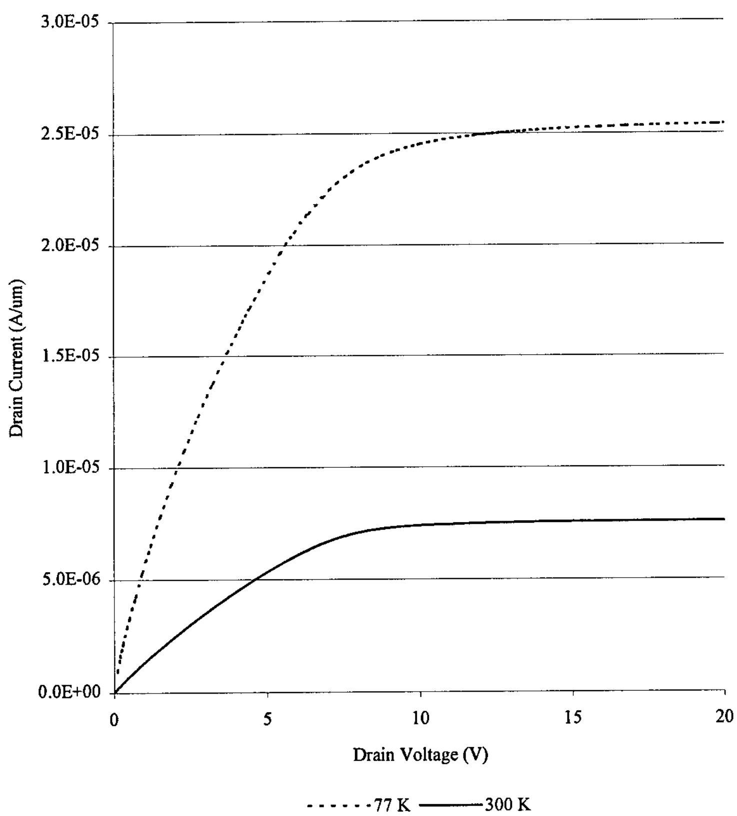

Figure 4.12 Plot of Drain Voltage vs. Drain Current at V_G=3V at 77 K and 300 K

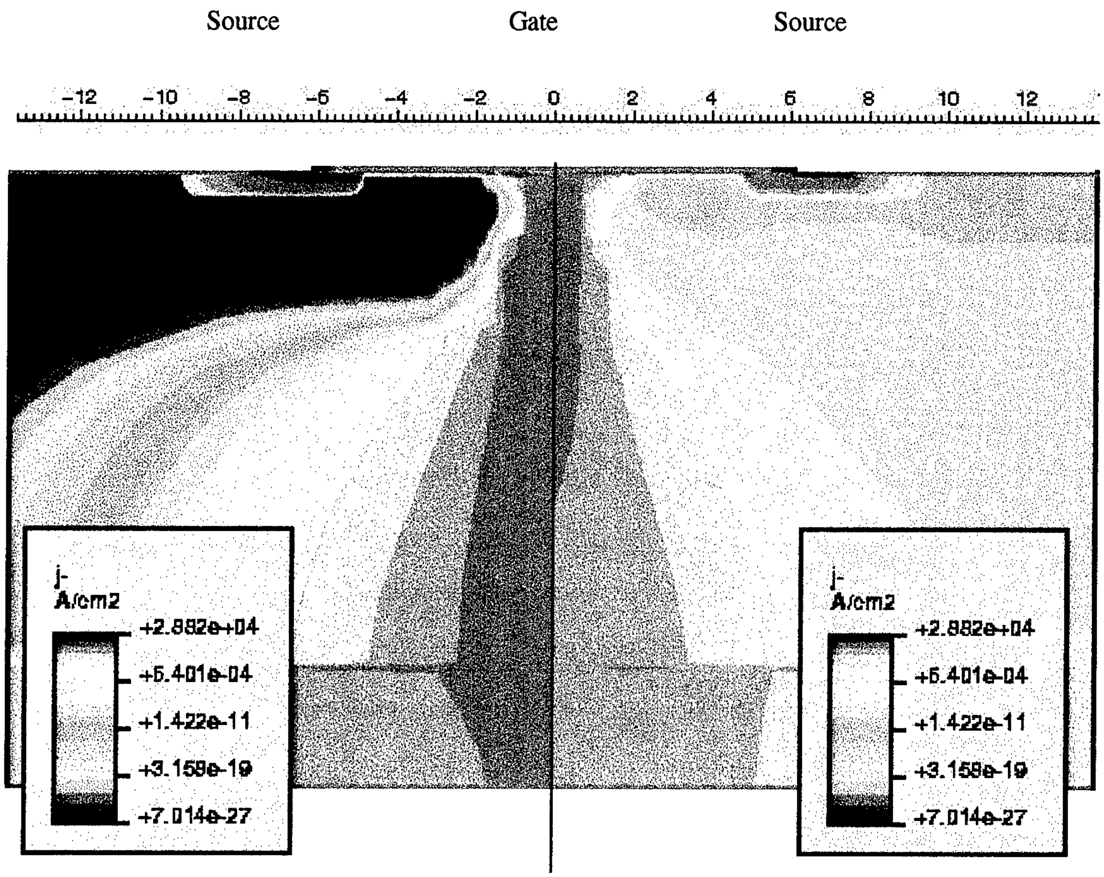

Figure 4.13 Cross Section Showing Electron Current Density at 77 K and 300 K

Figure 4.13 is a PICCASO-ISE cross section of the device at 77 K and 300 K. Here the concentrations are shown on equal scale for clarification. The left half is the device showing electron current density at 77 K, while the right half is the device with electron current density at 300 K. In both instances, the device is in a full state at 20 V at the drain and 3 V on the gate. Here, you can see the effects of current spreading in the drift region and the availability of free holes on the outer edges of the depletion region. At 77 K, the maximum current density is concentrated all the way through the drift region into the drain, where as, at 300 K the density is not as concentrated as it barely extends down the drift region half way. In order to gain a better understanding of what is happening to current density in the drift region, refer to Figure 4.14. This is a plot of electron current density for the two temperatures as a function of position in the x-axis, taken at the mid point of the drift region. Current density for both instances reaches a maximum in the center of the drift conduction channel, however, at 77 K, a maximum value of

1150 A/cm^2 is obtained where at 300 K it reaches a maximum of 420 A/cm^2. This corresponds to a 3x increase of conduction current when operated at 77 K. Also, notice that although current density increases at 77 K, the overall width of the current density channel in the drift region has not changed.

From the previous section, it has been stated that specific on resistance is proportional to drift region width and inversely proportional to drift region mobility and concentration. From Figure 4.12 the calculated specific on resistance corresponds to a factor of 3x increase in specific on resistance at 77 K compared to that at 300 K. Figure 4.15 is a plot of drift region mobility taken at the same position as current density from the previous plot. Recalling that drift region mobility is inversely proportional to on resistance, this plot demonstrates the drastic improvement in bulk (drift) region mobility as a function of temperature across the length of the device. In this region, bulk mobility increases from about 450 cm^2/Vs at 300 K to over 1200 cm^2/Vs at 77 K.

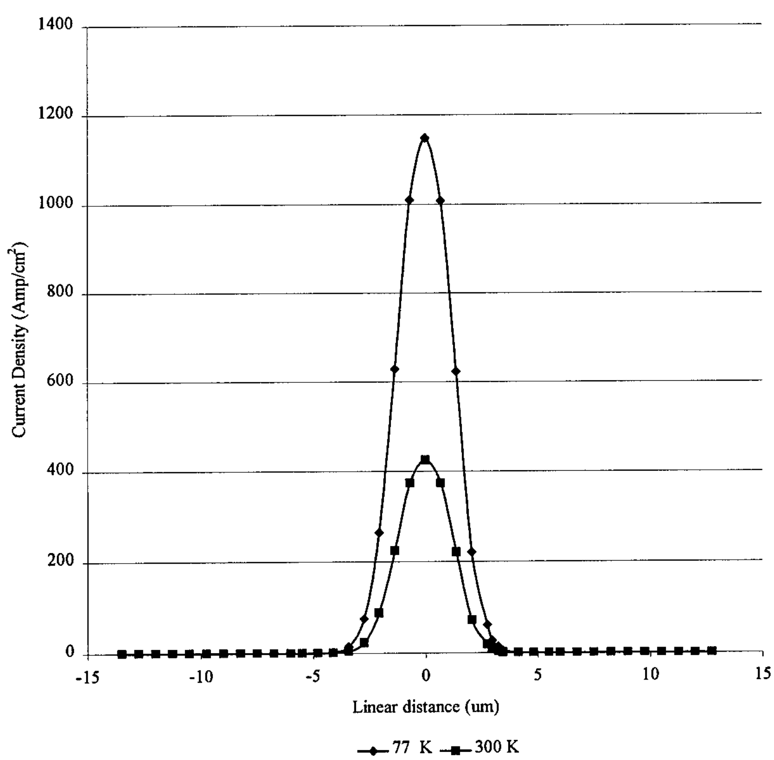

Figure 4.14 Plot of Electron Current Density Along the X-Axis

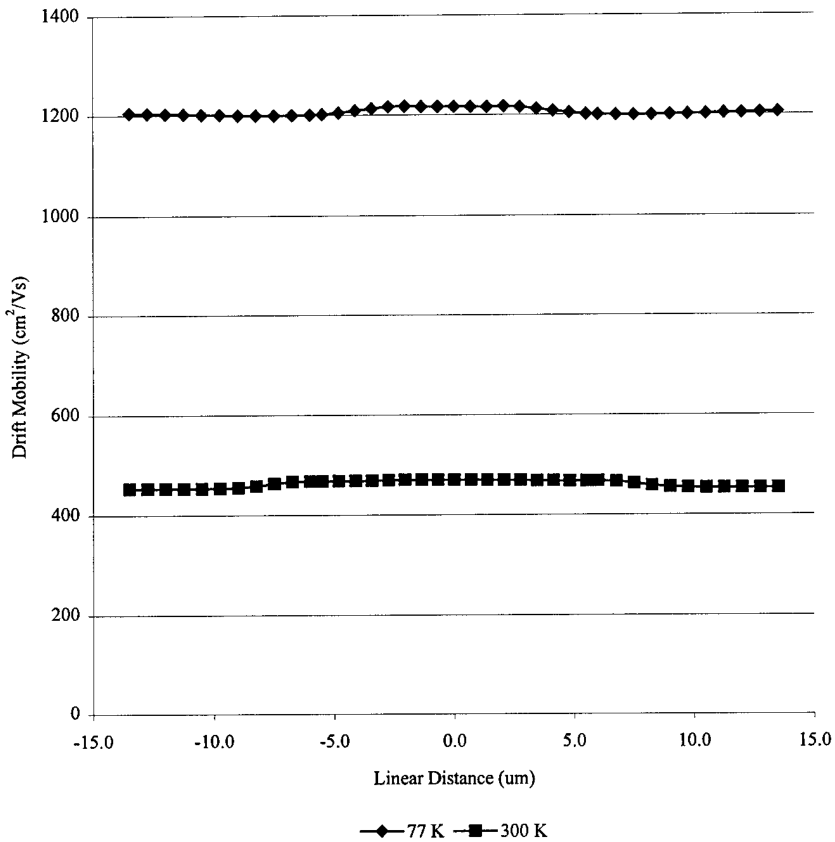

Figure 4.15 Plot of Drift Region Mobility across the Device

Transconductance at Cryogenic Temperatures

For the determination of the transconductance of the device, the following plots were generated. Figure 4.16 is the drain current vs. drain voltage plot at 77 K and 300 K with an applied gate voltage of 3V and 4V as per the graph. Combining the two temperature ranges clarifies the magnitude of increase in the transconductance of the device at 77 K vice 300 K. At 77 the normalized transconductance is 4.3×10^{-5} A/Vμm while at 300 K the normalized transconductance is only 1.55×10^{-5} A/Vμm. In this instance, the gain in transconductance corresponds to about an increase of almost three times.

Breakdown Voltage at Cryogenic Temperatures

As previously discussed, one of the drawbacks in operation at cryogenic temperatures is the slight reduction in breakdown voltage. This is realized by understanding that the mean free path of carriers at LNT increases giving them more energy for a given electric filed prior to collision resulting in a reduced avalanche breakdown voltage [29]. Figure 4.17 is a plot of drain current vs. drain voltage at both 77 K and 300 K showing the decreased breakdown voltage effects at LNT. Breakdown voltage of the device is about 208 V at 300 K as compared to 195 V at 77 K. This corresponds to about a 6% decrease in breakdown voltage when operated at LNT.

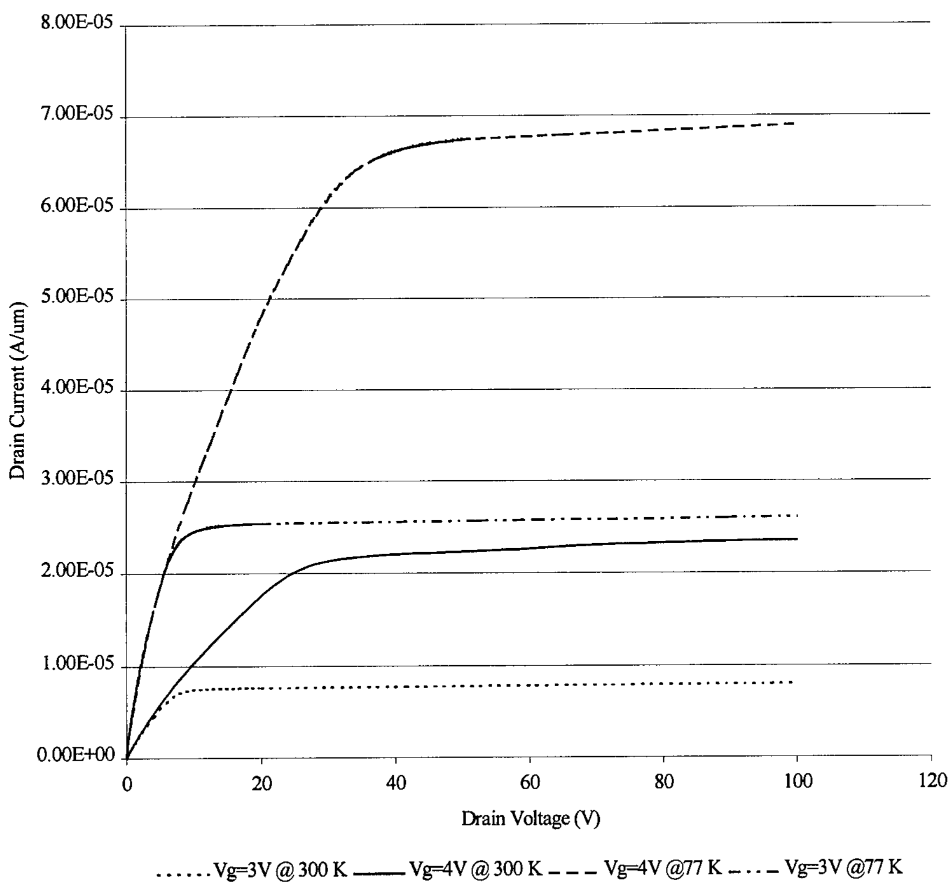

Figure 4.16 Plot of Drain Current vs. Drain Voltage at 3V and 4V for 77 K and 300 K

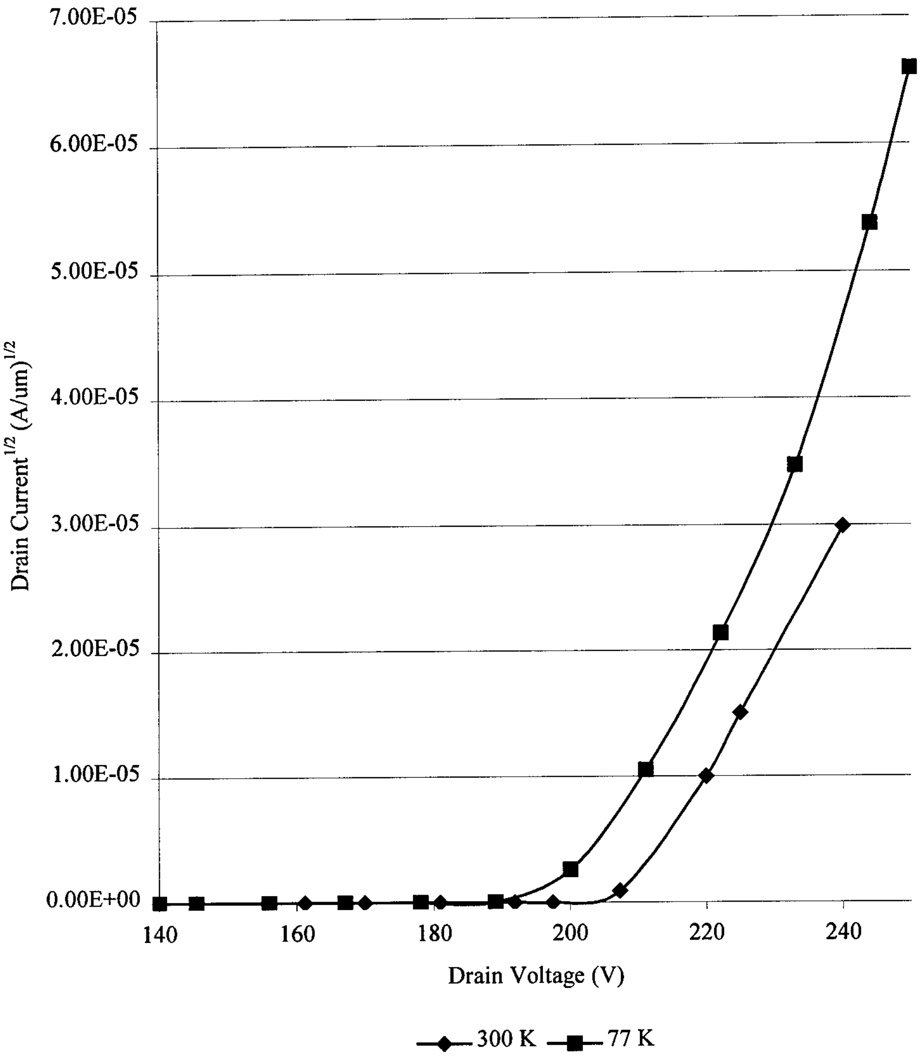

Figure 4.17 Plot of Drain Current vs. Drain Voltage for Breakdown Voltage Comparison

4.3 Doping Changes and a Comparative Analysis on Operating Parameters

In this section, the doping concentrations of both the epi-layer and p-base regions are changed to study the effects of a variety of parameters. Section 1 will study the effects of changing the epi-layer concentration from the base model of 2×10^{14} cm^{-3} doped phosphorous to 3×10^{14} cm^{-3} and then to 4×10^{14} cm^{-3}. Here, topics of interest are the current versus voltage curves at 77 K including specific on resistance and breakdown voltage analysis. Section 2 will then study the effects of changing the p-base region concentration from the base model of $5x10^{16}$ cm^{-3} to $7x10^{16}$ cm^{-3} and $9x10^{16}$ cm^{-3} doped boron. In this section, topics of interest are threshold voltage comparisons, inversion layer mobility changes, and drain current versus drain voltage comparisons.

Effects of Varying Epi-Layer Concentration at 77 K

As discussed in section 4.1, there is a trade off in operating characteristics between low on resistance and high breakdown voltage. Figure 4.18 is a plot of drain current versus drain voltage for an epi-layer concentration of $2x10^{14}$ cm^{-3}, $3x10^{14}$ cm^{-3} , and $4x10^{14}$ cm^{-3}. The obvious observation that should be made is the increase in the on resistance with the higher epi-layer doping concentrations, as discussed in section 4.1. This can be accounted for by recalling equation 4.10 where the specific on resistance is inversely proportional to epi-layer concentration. Another view that can be generated for further analysis is Figure 4.19. This figure is a PICASSO-ISE plot of the electron current density at 77 K with an epi-layer of $2x10^{14}$ cm^{-3} on the left and side and an epi-layer of $4x10^{14}$ cm^{-3} on the right hand side. Here, as concentration increases, the current density of the device will increase slightly, leading to a lower on resistance. As briefly mentioned before, as doping level of the epi-layer is increased, the specific on resistance of the device will decrease, however, breakdown voltage decreases as a result. Figure 4.20 is a plot of drain current versus drain voltage at the given epi-layer concentrations to show the effects of doping on breakdown voltage. These simulations were performed at 77 K and show that breakdown voltage of the device decreases from the original 195 V to 185 V at $3x10^{14}$ cm^{-3} and, finally, to 179 V at $4x10^{14}$ cm^{-3}.

Effects of Varying Base Layer Concentration at 77 K

This section compares the simulated results of the power MOSFET operating at 77 K by changing the doping concentration of the p-base region. Topics of interest are the drain current versus drain voltage curves, the threshold voltage analysis and the mobility of the electrons at silicon-silicon oxide interface.

The doping concentration of p-base region plays an important role in the overall conduction and turn on of the power MOSFET. Figure 4.21 is the drain current versus drain voltage plot of the DMOS at 77 K when base region doping changes from the original $5x10^{16}$ cm^{-3} to $7x10^{16}$ cm^{-3} and then to $9x10^{16}$ cm^{-3}. Drain current reduces substantially as base region concentration increases. From this plot, comparing the original base region doping concentration to that of $9x10^{16}$ cm^{-3}, drain current decreases from $2.54x10^{-6}$ A/μm to $1.14x10^{-6}$ A/μm, a 95% decrease.

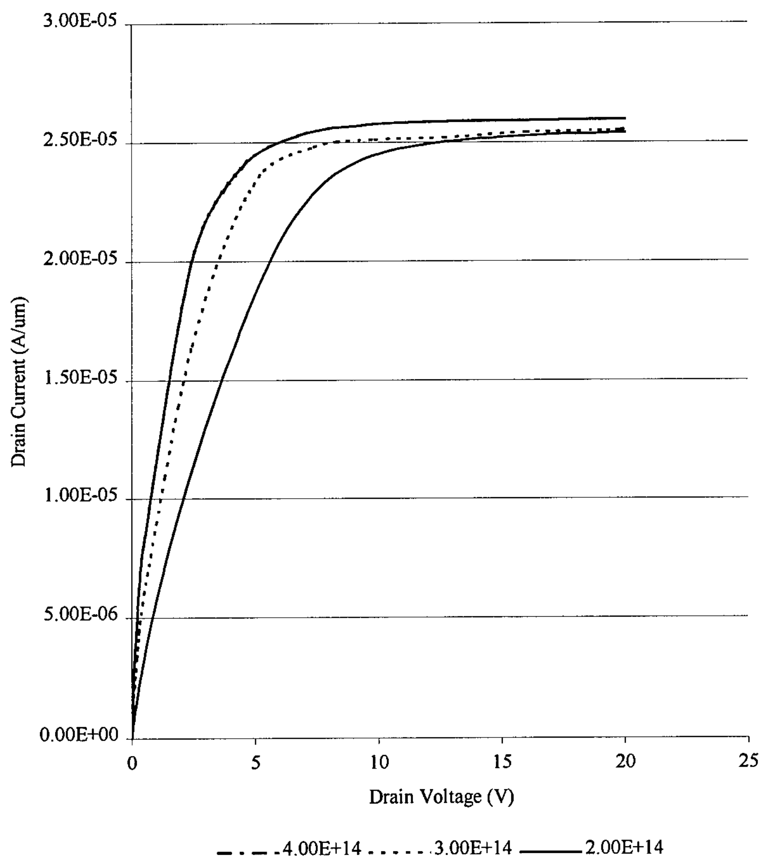

Figure 4.18 Plot of Drain Voltage vs. Drain Current at 77K with Varying Epi-Layer

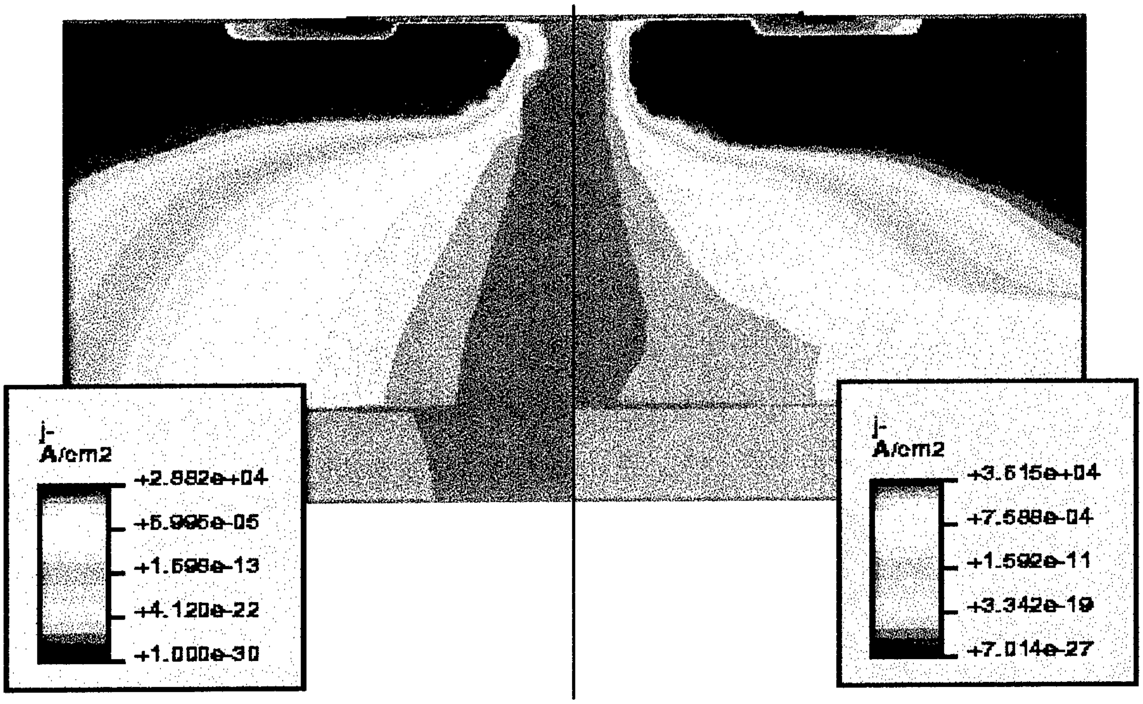

Figure 4.19 Cross Section of Device at 77K Showing Increased Current Density

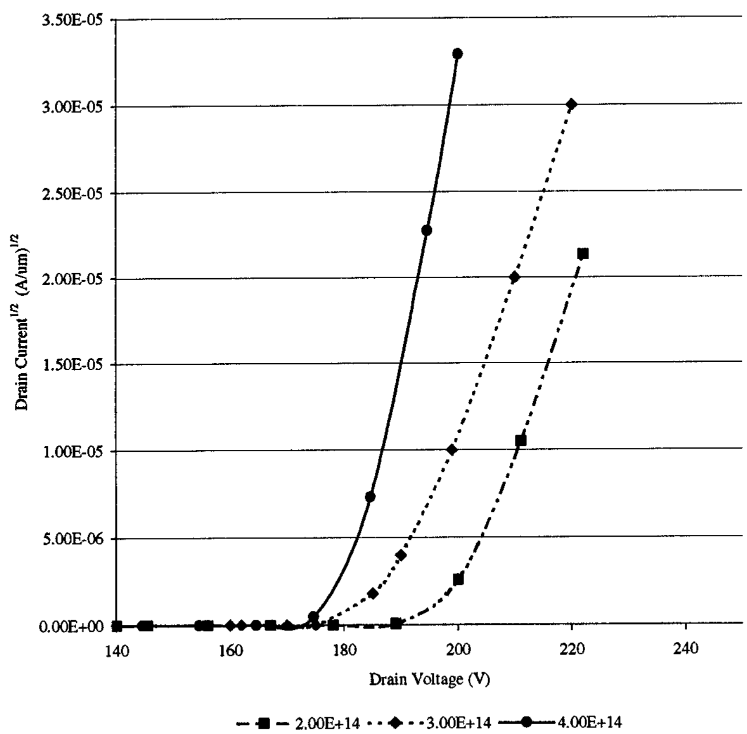

Figure 4.20 Plot of Breakdown Voltage by Varying Epi-Layer Concentration

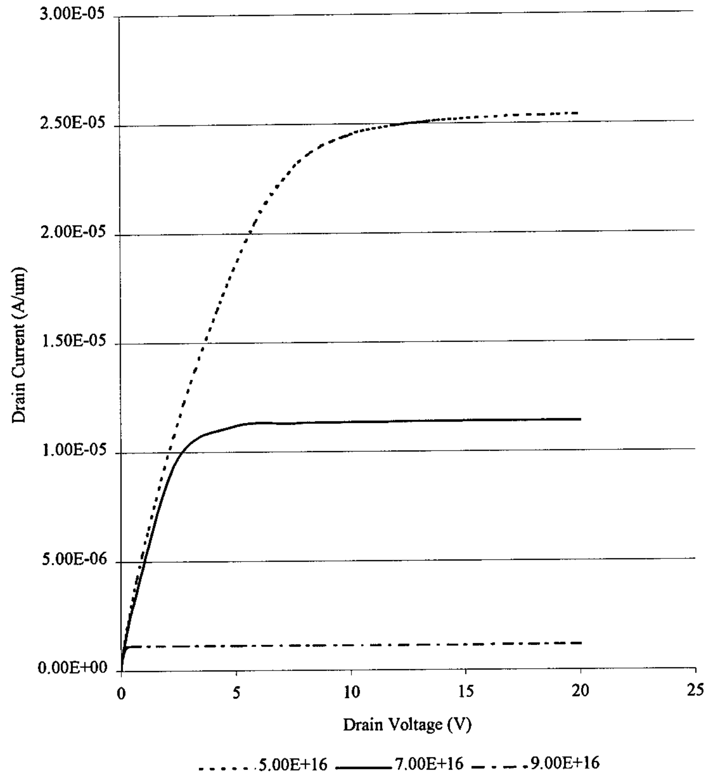

Figure 4.21 Plot of Drain Current vs. Drain Voltage by Varying Base Concentration

To gain a better understanding of why this occurs, it is important to compare the threshold voltage of the device under these conditions. Figure 4.22 is a plot of gate voltage versus the square root drain current simulated at 77 K. Increasing the base region concentration will result in an increase in threshold voltage. From the graph, threshold voltage increases from 2.0 V to 2.3 V and finally to 2.7 V. This is realized when p-type material is required to go under strong inversion conditions, as discussed in Section 3. The requirement for the condition of strong inversion to occur is higher for higher doping concentrations.

Another parameter that should be analyzed is the current density through the inversion channel. Figure 4.23 is a plot of electron current density through the channel region. At a base concentration of $5x10^{16}$ cm^{-3}, current density is $2.14x10^4$ A/cm^2, while at $5x10^{16}$ cm^{-3}, current density is $9.63x10^3$ A/cm^2 and at $7x10^{16}$ cm^{-3}, the current density is only 963 A/cm^2. This corresponds to a decrease in current density along the channel by 95%.

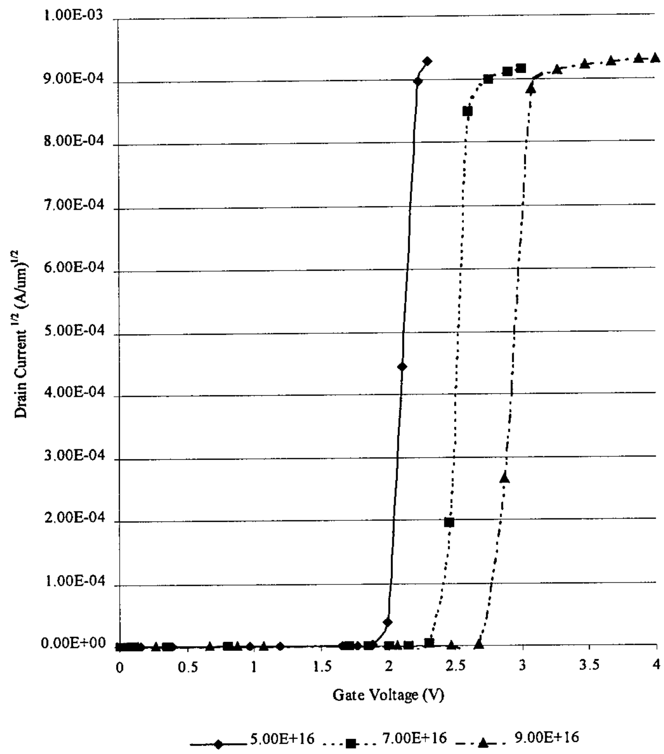

Figure 4.22 Plot of Threshold Voltage by Varying Base Concentration

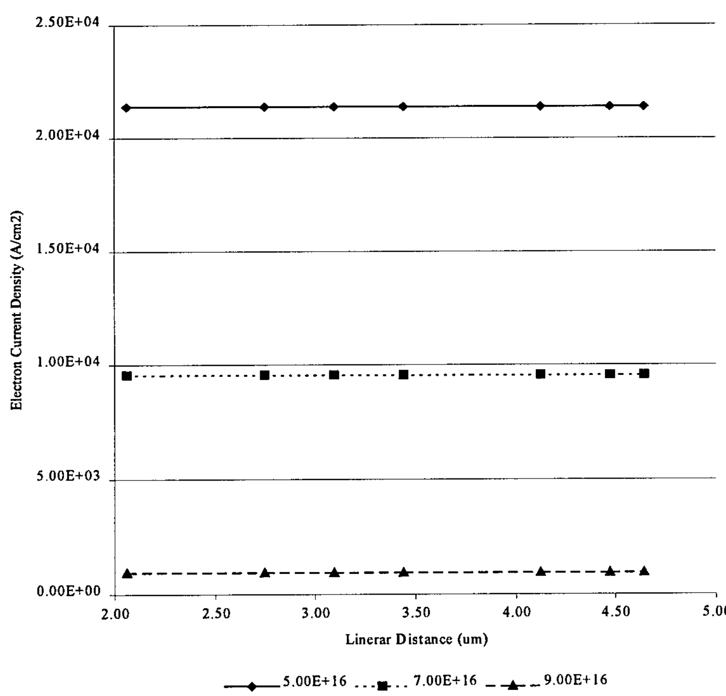

Figure 4.23 Plot of Electron Current Density across the Inversion Channel

5 POWER MOSFET FABRICATION AND DESIGN CONSIDERATIONS

Section 5 is devoted to explaining the processes involved in terms of the fabrication of the power MOSFET. Although an operating power MOSFET did not result from this effort, valuable information was gained in the understanding of important design considerations. Included in this chapter is the summary of the mask layers, processes used, and resultant diffusion profiles. Also included, is a discussion on why the device did not operate and suggested corrective actions needed for further study.

It is the opinion of the author that there is a strong need to fabricate the power MOSFET and perform operating tests on the device in order to accurately verify the validity of the models used in the simulation of the device. Although commercial power MOSFETs are readily available, and many key operating parameters are given in their vendor supplied technical specifications, the general public for patent confidentiality does not easily obtain many other key physical parameters. These parameters include gate oxide thickness, dopant concentrations and profiles, gate surface area and number of die per package. As a result of these ambiguities, it was then determined to fabricate a power MOSFET here at the University of Central Florida's class 100 clean room.

5.1 Fabrication of the Mask Levels

Based on the cross section of the device presented in Figure 2.1, it was determined that there was a need for four levels of masking in order to produce the DMOS. Mask level one was to be used to open the window in the thermally deposited silicon oxide in preparation for the boron diffusion used for the p-base regions. Mask level two was to be used to open the window in the thermally deposited silicon oxide in preparation for the phosphorous diffusion used for the n^+ source regions. Mask level three would be used to open the contact windows for the aluminum metalization, and mask level four would be used for metal stripping to form the source and gate contacts.

The design of the four layers of masking was performed using Auto-Cad. The masks were drawn originally on a 10x scale, then sent to a photo-reduction facility in order to produce a

10x reduction of each mask on an individual transparency. With the use of these transparencies, photolithography and thermal diffusion techniques were then utilized to fabricate the Power MOSFET. Figure 5.1 is the overhead view of each mask layer that was used in the fabrication of the device; all dimensions are in units of microns. The masks also include the fabrication of the n and p type resistors. The extra components in the mask will allow for easy measurements and characterization of the diffused materials in order to more accurately describe the parameters, such as doping concentrations, oxide thickness and metalization integrity of the device. The device has an inversion channel length of 50 μm, with large pads on the source and gate for easy access.

5.2 Processing the Power MOSFET

As described earlier, the power MOSFET was fabricated in the clean room at the University of Central Florida. Source and body diffusions were done thermally using Diffusion Furnaces. Although a complete procedure is provided in Appendix 3, an outline of the procedure is provided below.

The wafer of choice was a $2x10^{14}$ cm^{-3} n-type epi-layer with a thickness of 3.5 μm on a n^+ silicon substrate. The wafer was cleaned and prepared per Appendix 3, and was then allowed growing a thermal oxide of 4000 Å at 1100° C for 45 minutes. Negative Photo-resist was then spun for 30 seconds and a soft bake was performed for 3 minutes. Using a Carl Suiss mask aligner, the wafer was exposed for 20 seconds using UV light. The photo-resist was then developed for 2 minutes and inspected. Upon inspection, the wafers were then etched in a buffered oxide etch solution for 13 minutes. A predeposition of boron was then performed using boron doped wafers at 950° for 5 minutes. Next, a borosilicate etch was performed for 10 minutes, followed by a drive in at 1100° C for 1 hour and 30 minutes. This drive-in of the boron allowed for a new oxide growth of 4500 Å. The resultant oxide for the boron drive-in is the gate oxide needed for inversion to occur. However, this oxide was too thick for proper gate inversion action to occur, so a buffered oxide etch was performed for 8 minutes to reduce the oxide layer to about 2500 Å. A similar procedure (refer to Appendix 3) was performed for the second mask level, as above, and a contact window was then opened using the third mask level.

Aluminum was deposited on the front side of the wafer and mask four was then utilized using positive photo-resist. Excess Aluminum was removed using a 10:1 mixture of hydrofluoric acid to distilled water. Aluminum was then deposited on the backside of the wafer to form the drain contact.

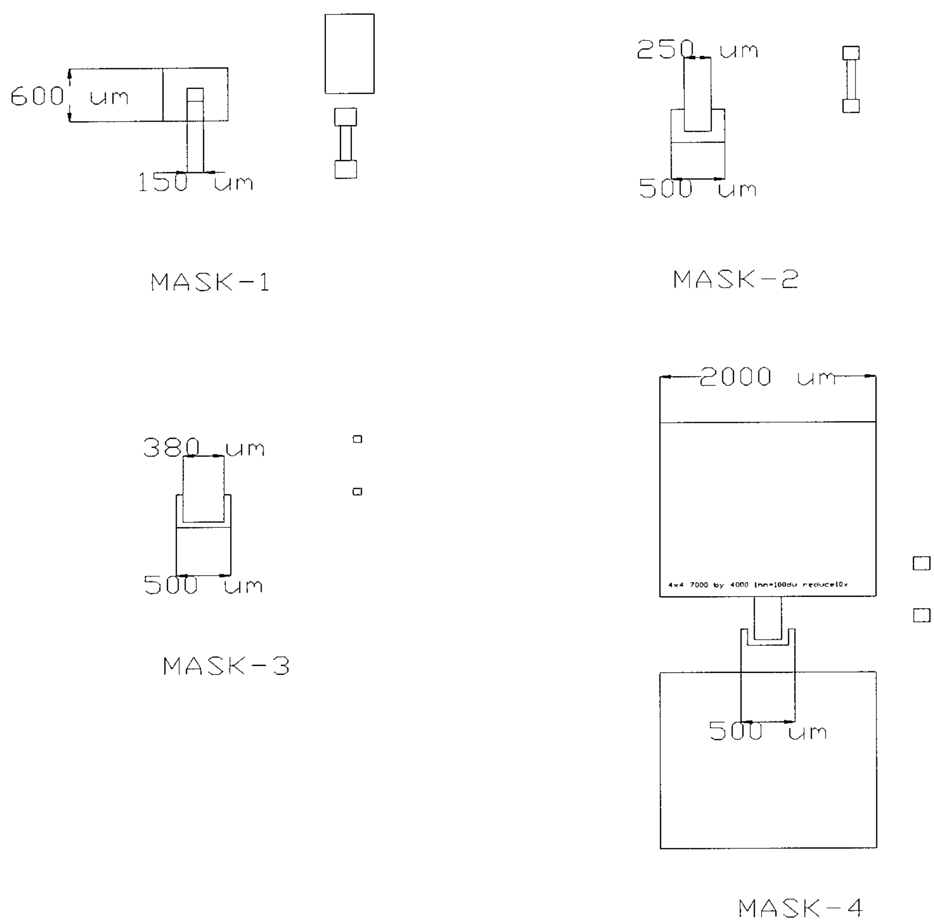

Figure 5.1 Overhead of Power MOSFET Mask Configuration

5.3 Diffusion Profile of the Base and Source Regions

In order to diffuse the Boron and the Phosphorous into the Silicon epi-layer, some considerations were taken into account in not to punch through the epi-layer. The n-type epi-layer was 3.5 μm thick with a concentration of 2×10^{14} cm^{-3}. Therefore, it was safe to diffuse the p-type boron approximately 2.0-2.5 μm deep. With this in mind, and assuming the surface solubility of boron, pre-deposited at 950°C, is 1.1×10^{20} cm^{-3},

$$N_{Boron@PRE} = N_{SurfaceSol}\left(1 - erf\left(\frac{x}{2\sqrt{D_1 t_1}}\right)\right) \tag{5.1}$$

D_1 is the diffusion coefficient for Boron, and t_1 is time of pre-deposition. Refer to Appendix 3 for the values used in this analysis. After the pre-deposition and the borosilicate etch was preformed, the drive-in of the boron was performed at 1100°C for 1 ½ hour. Here, the dose required for drive-in was 1.74×10^{14} cm^{-2}, where the dose (Q) is:

$$Q = 2N_{SolidSol}\sqrt{\frac{D_1 t_1}{\pi}} \tag{5.2}$$

The drive-in profile then, takes on a Gaussian profile and the concentration (N_{Boron}) is:

$$N_{Boron} = \frac{Q}{\sqrt{D_2 t_2 \pi}} \exp\left[-\left(\frac{x}{2\sqrt{D_2 t_2}}\right)^2\right] \tag{5.3}$$

Where D_2 is the Diffusion coefficient of drive-in, t_2 is the time of drive-in, and Q is dose from above. Again, refer to Appendix 3 for the values used. Figure 5.2 is the plot of the diffusion profile for this particular diffusion. For clarity, the pre-deposition profile is also plotted against the diffusion profile. The resulting profile gives a final surface concentration of 2.44×10^{18} cm^{-3} at a junction depth in the epi-layer of 2.4 μm.

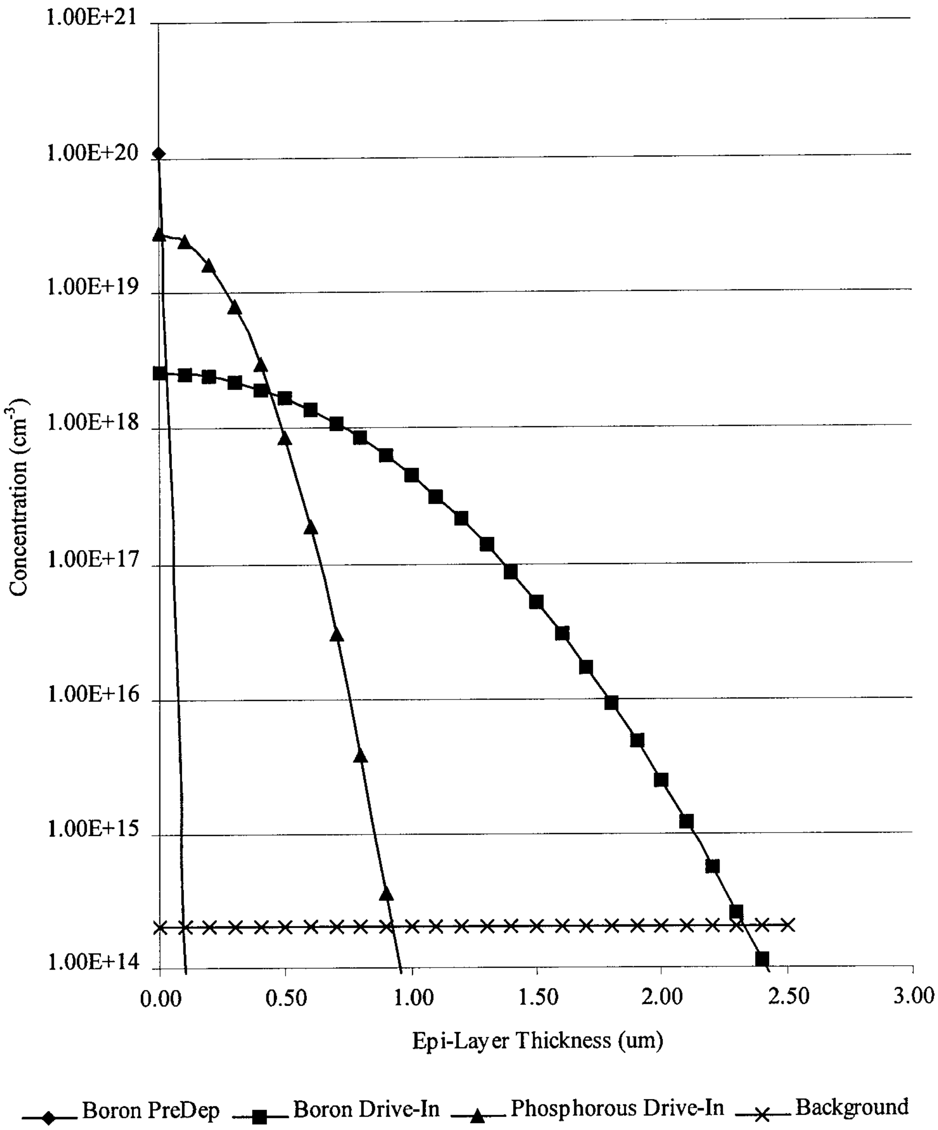

Figure 5.2 Plot of Diffusion Profiles

Following this, the source diffusion was then performed with the specific times, t_3 and t_4, and temperatures listed in Appendix 3. Figure 5.2 also shows the source distribution.

5.4 In-Operability of the Fabricated Device

Following the fabrication of the device, the next phase of the process was to test the finished product. Testing was to be performed at both room temperature and at 77 K. However, during the initial testing of the device for operability, the device operated completely independent of gate voltage and displayed a linear current versus voltage curve on the curve tracer, and it was assumed that the device was fabricated incorrectly. Through many revisions of the procedure and mask dimensions, the resultant device still did not operate as a MOSFET but rather as a resistor.

Up to this point, all simulations of the device were performed using the model presented previously. Through the use of ISE-TCAD, the device was simulated and did show the characteristics as displayed during testing. It also showed that the highly doped n-epi / p-base reverse biased junction was breaking down at very low voltages. This is due to large differences in doping concentration between the two junctions, causing an avalanche to occur. The junction was at $2.8x10^{18}$ cm^{-3} on the surface on the base diffusion and $2x10^{14}$ cm^{-3} associated with the epi-layer. The solution seemed to be lowering surface concentration of the base diffusion.

5.5 Corrective Actions for Fabrication

Lowering the surface concentration of the base diffusion can potentially be accomplished by two means. One of these means, and the most promising, is the use of ion implantation. As seen within this study, the p-base region plays a very important role on current handling capabilities, threshold and breakdown voltage. The operating characteristics change drastically with just a small change in doping concentrations. Ion implantation can used to diffuse the base region to obtain a surface concentration of $5x10^{16}$ cm^{-3}. Prior to ion implantation, a detailed analysis of dose and junction depth requirements is needed.

The other possible option to obtain low surface concentration is the use of a spin-on dopant. Spin-on dopants can be obtained for a variety of concentrations, however, there are some drawbacks using this method including an excess time to drive for such a deep well. The reasonable choice seems to be the use of ion implantation, lowering the surface concentration of the p-base region.

6 CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

It has been established that MOSFETs operate significantly better at cryogenic temperature compared to room temperature. This report examines both the operational and physical aspects of the MOSFET under cryogenic condition. We studied not only mathematical models but also operational analysis by the use of ISE-TCAD simulation tools.

A variety of tests were performed on the device including current vs. voltage, threshold voltage and breakdown voltage measurements. Included in this, are both one and two-dimensional current density and mobility measurements in different regions of the MOSFET. It has been shown that for the particular device, channel mobility increases by 10x, current density and electron mobility in the drift region increases by 3x. However, some of the disadvantages include a threshold voltage of approximately 21% higher, and a breakdown voltage decrease by 6% when device is operated at 77K.

Another interesting outcome of this study is the realization of a trade off between low on resistance and high breakdown voltage. Major areas of interest within the power MOSFET are the epi-layer and base regions. As epi-layer concentration increased, on resistance decreased (but no gain in transconductance), and breakdown voltage decreased. Likewise, when the base region concentration increased, threshold voltage increased and current density decreased substantially.

The next logical step is to successfully fabricate an operational device and incorporate the physical characteristics into ISE-TCAD for full testing verification of the models used thus far. Another aspect of research is to include thermal properties of the power MOSFET under cryogenic conditions. From here, we can go beyond the device simulation and testing cryogenic circuits.

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