002088

JPRS-ESA-84-040

5 November 1984

DISTRIBUTION STATEMENT A
Approved for public release;
Distribution Unlimited

East Europe Report

SCIENCE & TECHNOLOGY

CZECHOSLOVAKIA:

SYSTEM OF SMALL ELECTRONIC COMPUTERS

19980501 024

DTIC QUALITY INSPECTED 3

FBIS FOREIGN BROADCAST INFORMATION SERVICE

REPRODUCED BY
NATIONAL TECHNICAL
INFORMATION SERVICE
U.S. DEPARTMENT OF COMMERCE
SPRINGFIELD, VA. 22161

5
256
A12

NOTE

JPRS publications contain information primarily from foreign newspapers, periodicals and books, but also from news agency transmissions and broadcasts. Materials from foreign-language sources are translated; those from English-language sources are transcribed or reprinted, with the original phrasing and other characteristics retained.

Headlines, editorial reports, and material enclosed in brackets [] are supplied by JPRS. Processing indicators such as [Text] or [Excerpt] in the first line of each item, or following the last line of a brief, indicate how the original information was processed. Where no processing indicator is given, the information was summarized or extracted.

Unfamiliar names rendered phonetically or transliterated are enclosed in parentheses. Words or names preceded by a question mark and enclosed in parentheses were not clear in the original but have been supplied as appropriate in context. Other unattributed parenthetical notes within the body of an item originate with the source. Times within items are as given by source.

The contents of this publication in no way represent the policies, views or attitudes of the U.S. Government.

PROCUREMENT OF PUBLICATIONS

JPRS publications may be ordered from the National Technical Information Service, Springfield, Virginia 22161. In ordering, it is recommended that the JPRS number, title, date and author, if applicable, of publication be cited.

Current JPRS publications are announced in Government Reports Announcements issued semi-monthly by the National Technical Information Service, and are listed in the Monthly Catalog of U.S. Government Publications issued by the Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402.

Correspondence pertaining to matters other than procurement may be addressed to Joint Publications Research Service, 1000 North Glebe Road, Arlington, Virginia 22201.

JPRS-ESA-84-040

5 November 1984

EAST EUROPE REPORT

SCIENCE & TECHNOLOGY

CZECHOSLOVAKIA: SYSTEM OF SMALL ELECTRONIC COMPUTERS

Prague VYBER INFORMACI Z ORGANIZACNI A VYPOCETNI TECHNIKY in Czech 1982 pp 1-207

CONTENTS

Preface (3)..... 2

1. Introduction (3)..... 4

1.1 Structure of this publication (10)..... 4
1.2 SMEP Program (11)..... 5
1.3 System of markings (11)..... 6

2. 16-bit Systems (13)..... 7

2.1 Hardware systems (13)..... 7

2.1.1 Basic Configurations (16)..... 12
SM 3-20 Minicomputer..... 12
SM 4-20 Minicomputer..... 15
SM 52/11 Minicomputer..... 20
SM 50/50 Microcomputer System..... 25
PPPD 1 Acquisition System with SM 3-20..... 31
PPPD 1 Acquisition System with SM 50/50..... 31
PPPD 2 Acquisition System with SM 4-20..... 33
ISAP 1 Graphic System with SM 4-20..... 34
IMS 2 Measuring System with SM 50/50..... 36

2.1.2 Disk Memories (35)..... 37
5 MB-CM 5400, CM 5403..... 37
10 MB-CM 5410..... 38
29 MB-CM 5405..... 39
Memory with CM 5605 Floppy Disk..... 39

2.1.3 Tape Memories (40) 42
CM 5300, CM 5300.01, IZOT 5003 42
CM 5302, CM 5003 42

2.1.4 Peripheral Units Using Paper (42) 45
CM 6204 Tape Reader/Perforator 45
CM 6208 Tape Reader/Perforator 46
EC 6112 Punch Card Reader 46

2.1.5 Printers (45) 47
CM 6301 Dot Printer 48
CM 6313 Line Printer 48

2.1.6 Graphic Systems (47) 50
CM 7405 Graphic Terminal 50
GVM 01 Graphic Monitor 53
Digigraf 1712 Drawing System 54
Digigraf 1208 Drawing System 55
Digitizer 1208 Reading System 55
BAK 5T Coordinate Graph Plotter 55
CM 6303 Dot Printer/Graphic Output 56

2.1.7 Terminals, Data Transmission Systems and Connecting Units (52) 57
CM 7202 Display Terminal 57
CM 1601 Display Terminal 60
Semigraphic Terminal 61
CM 7108 Terminal with Printer 62

ASAD CM 6002 Asynchronous Adapter 64
QASAD CM 8512 Quadruple Adapter 66
AMU CM 8511 Asynchronous Multiplex 66
SAD CM 8506 Synchronous Adapter 70
SAD B SM 1207 Synchronous Adapter 71
SAD D SM 1208 Synchronous Adapter 72
CM 8105 Zero Modem 72

MDS 200 Modem 73
MDS 1200 Modem 73
KOMPRO Communication Processor 74

PAD 8 CM 6001 Parallel Adapter 75
PAD 12 SM 0706 Parallel Adapter 75
PAD 16 SM 0708 Parallel Adapter 75

2.1.8 Interface Units (67) 76
LJSP CM 9205 Laboratory Unit 76
IMS 2 CM 0102 Connecting Unit 78
CM 9004 Connecting Unit for DASIO 600 79
CAMAC Frame Control Unit 80

2.1.9 Structural and Systemic Elements (71)..... 81
CM 0101 Systemic Unit..... 81
SM 2016 Connecting Plate..... 81
CM 4103 Common Busbar Repeater..... 82
Expansion Grid..... 83
Casing..... 83
Casing with Expansion Rack..... 83

2.2 Software (73)..... 84

2.2.1 Operating Systems (73)..... 84
LOS..... 84
FOBOS 1..... 85
FOBOS 2..... 85
DIAMS 1..... 86
DIAMS 2..... 88
DOS RVR 1..... 89
DOS RV 2..... 90
MOS RV 2..... 91
--RSZ..... 92
--DTS..... 92
--SORT..... 93
--MTD..... 94
--Text Processor..... 94
--Set of Programs for Scientific and Tech. Calculations... 94

2.2.2 Programming Systems (81)..... 95
PPPD 1..... 95
GOLEM..... 100
MARKAB (PPPD 2)..... 100
VU BASIC..... 101
VYUKA..... 102

2.2.3 Telecommunication Software (87)..... 104
Emulation Routines..... 104
SYRPOS 1--Computer Networks..... 105

2.2.4 Software for Graphics (94)..... 114
SM GRAF..... 115
GFS..... 116
MINIG..... 116

2.2.5 Programming Languages (98)..... 118
Macroassembler..... 118
BASIC..... 119
BASIC PLUS..... 120
BASIC PLUS 2..... 121
FORTRAN IV..... 121
FORTRAN IV PLUS..... 121
COBOL..... 123
FOCAL..... 124
MUMPS..... 124

2.2.6 Testing Monitors (102) 125
TMOS 1 125
TMOS 2 125

3. Imported 16-bit Systems (103) 125

3.1 SM 4-10 (103) 125
3.2 INDEPENDENT (104) 126

4. 8-bit Systems (112) 135

4.1 Hardware (112) 136

4.1.1 SM 50/40 Cassette (115) 138
4.1.2 SM 2138 Single Plate Microcomputer (116) 139
4.1.3 Memories (117) 141
SM 0440 16 KB Dynamic RAM 141
SM 0441 16 KB with Reserve 142
SM 0442 64 KB Dynamic RAM/EPROM 143
SM 0449 16 KB EPROM 144

4.1.4 Input/Output Units (121) 145
SM 1350 (LLM) Multiplex 145
SM 1352 Analog-Digital Converter (ADC) 147
SM 1353 8-bit Analog Outputs (A08) 149
SM 1354 12-bit Analog Outputs (A012) 151
SM 1355 48 Discrete Inputs/Outputs (DIO) 152
SM 1356 Counter Inputs (CI) 153
SM 1357 Interruption Inputs (II) 155
SM 1358 Pulse Output (PO) 156
SM 1360 Multiplex (HLM) 157
SM 2165 Parallel Input/Output-72 Lines TTL (MPAPV) 159
SM 2170 Mathematical Module 160

4.1.5 Control Units for Peripheral Equipment (133) 161
SM 2150 Four Serial Channels (MPASV) 161
Control Unit for Floppy Disk Memory 161
SM 2143 Nonstandard Interface Module 163

4.1.6 Power Supply Units (135) 163
A Basic Power Supply Unit 163
B Power Supply Unit 164
C Power Supply Unit 164
D Power Supply Unit 165

4.1.7 Structural Elements (137) 165
Cassette 165
Ranging Box 166

4.1.8 Developmental Micromputer Systems (MVS) (138)..... 166
MVS I Perforated Tape..... 167
MVS II Disk-Oriented..... 169
Basic Unit..... 169
MVE Developmental Emulator..... 170
FM 1501 A/M Perforated Tape Reader..... 172
DT 105 S Perforated Tape Punch..... 173
CONSUL C 2111 Dot Printer..... 173
PGM 08 Memory Programmer..... 174
Floppy Disk Memory..... 175

4.1.9 SM 50/40 Microcomputer (145)..... 176
Basic Microcomputer Configuration..... 177
Programmable Terminal..... 178
System for Text Processing..... 179

4.1.10 SM 53/10 Distributed System (148)..... 180
TOP Terminal of Process Operator..... 181
TSP Interface Terminal..... 181
Terminals Connection Cable..... 183
SM 1341 Communication Module..... 184
Structural Design..... 184

4.1.11 SM 53/20 Distributed System (152)..... 185

4.1.12 VUVT Training Microcomputer (152)..... 185

4.2 Software (154)..... 187

4.2.1 DOS MVS (154)..... 187
Macroassembler..... 191
PL/M 80..... 192
BASIC 80..... 192
PASCAL 80..... 192
FORTRAN 80..... 192

4.2.2 LOS VMS (158)..... 193
4.2.3 Real Time Execution (158)..... 193
4.2.4 MUOS (161)..... 196
4.2.5 MIKROS (161)..... 197
DATOS Program for Operation with Sets..... 199
DYNAMIT Sorting Program..... 199
FORTRAN M..... 200
P/BASIC..... 200
G/BASIC..... 200
K/BASIC..... 201
COBOL 80..... 201
TEXT 01..... 202

4.2.6 Basic Software for SM 53/10 (165)..... 202

4.2.7 MODUS (166) 203
Continuous Technological Processes 205
Discrete Technological Processes 208

4.2.8 Cross-Programming Systems (170) 209

5. Operational and Installation Conditions (171) 210

5.1 Operational and Installation Conditions for Minicomputers (171). 210
5.2 Operational Conditions for Microcomputers (172) 212

6. Documentation and Literature (174) 213

6.1 16-bit Systems (174) 213
6.2 8-bit Systems (179) 218
6.3 Instructional Documentation (181) 219
6.4 Outline of Monographs (183) 221

7. Training (185) 223

7.1 Courses for Managerial Personnel and Organizers (188) 228
7.2 Courses for Programmers (188) 229
7.3 Courses for System Programmers (189) 229
7.4 Courses for Operators (189) 229
7.5 Courses for Technicians (189) 230

8. Planning and Technical Assistance (193) 230

8.1 Note on Planning Remote Data Processing Systems (193) 231

9. Technical Services (195) 232

10. Availability (198) 236

10.1 Hardware (198) 236

10.1.1 16-bit Systems (198) 236
10.1.2 8-bit Systems (200) 238

10.2 Software (201) 240
10.3 Documentation (202) 241
10.4 Imported Systems (202) 241

11. Order Justification and Information (203) 241

11.1 Budgeting of Computer Technology (203) 241
11.2 Ordering, Directory (206) 245
11.3 Deliveries (206) 245
11.4 Warranties (206) 246

11.4.1 Hardware (206) 246
11.4.2 Basic Software (207) 246

11.5 Information, Directory (207) 246

12. References (207) 247

SYSTEM OF SMALL ELECTRONIC COMPUTERS

Prague VYBER INFORMACI Z ORGANIZACNI A VYPOCETNI TECHNIKY in Czech 1982
pp 1-207

[Special issue of VYBER INFORMACI Z ORGANIZACNI A VYPOCETNI TECHNIKY devoted to a monograph by Eng Vaclav Vojtech, et al.: "Outline of the SMEP System of Small Electronic Computers"]

[Text] Selection of Information From Organization and Computer Technology

OUTLINE OF THE SYSTEM OF SMEP SMALL ELECTRONIC COMPUTERS

Eng Vaclav Vojtech, et al.

Published by

National Technical Service Organization

NOTO

Sectoral Information Center

Office Machines fiduciary concern enterprise, Prague

Members of the team of authors:

Eng Jan Cip, CSc
Eng Jaroslav Dvorak
Eng Rudolf Hofmeister
Eng Milan Kukacka
Ludmila Kustkova
Eng Jan Mirvald
Eng Ivan Peceny
Eng Josef Saidl
Eng Zdenek Vokac

Reviewed by

Eng Milan Gabik, Research Institute for Computer Technology, Zilina
Eng Eduard Glut, Computer Technology Enterprises, Namestovo

Preface

The system of small electronic computers designated by the abbreviation SMEP was adopted in the CSSR as a prospective program for computer technology in the area of minicomputers and microcomputers. After the planned termination of previously introduced production of other types of minicomputers, SMEP will represent the key source for meeting the needs of the national economy with computer technology of this type.

Thus, SMEP is justifiably the center of attention of wide strata of the professional public as the system with which most users of computer technology will come directly or indirectly into contact in the nearest future.

The duration of domestic production of computers can already be counted in decades. If we consider the preceding many years of tradition in the production and application of perforated tape or punch-card-oriented computer systems, it can be asserted without exaggeration that computer technology forms an integral and organic part of most economic, technical, scientific, administrative and other activities in the CSSR. The concept of development, production and utilization of the SMEP system represents a qualitatively new level in the history of Czechoslovak production of computer technology, because never have we encountered in the past a program of such breadth and complexity as the SMEP program. Its modular concept, variability, and the extent of hardware and software form a basis for wide potential applications of SMEP.

The extant practice of producing integrated computer systems led to a simplified approach on the part of both suppliers and users. The SMEP concept confronted both parties with an entirely new situation in which many things no longer apply and in which many things have to be built from the ground up.

The usual initial difficulties attendant to the introduction of every new computer technology program are due in the case of SMEP specifically to its extent.

A source of misunderstanding and the cause of many complications is the low level of familiarization with the basic principles of the system's composition and function and inadequately based on distorted information of a commercial nature.

While the special issue of VYBER now in your hands cannot close all the gaps in information about SMEP, the authors hope that it will help to eliminate some difficulties. We intend to keep updating the information we are now publishing and offer it to you again in the form of revised reissues. For that reason we solicit your comments, advice and criticism as contributions to an improved version of the next issue expanded by additional information. Send your comments to: Office Machines [Kancelarske stroje], odbor obchodni politiky [marketing policy department], 12 Melantrichova Street, 111 90 Prague 1.

The authors

NOTE:

At the time the authors were proofreading this issue it could be stated that some information appearing in this special issue of VYBER had already been updated. Particularly gratifying is the fact that Office Machines has prepared detailed information for users of all types of the described products and, moreover, that project documentation and information for ordering have already been disseminated. This information is available through the network of representatives of the marketing sector in Prague who are stationed at individual outlets of Office Machines. The names and addresses of these representatives appear in the directory part of this publication.

1. Introduction

1.1 Structure of This Publication

After an outline of the structure of the entire publication, the first chapter stresses the SMEP program as the international program of the CEMA countries and the manner of its implementation in the CSSR within individual chronological stages. The chapter includes a description of the utilized designation of SMEP hardware.

The second chapter is devoted to 16-bit SMEP systems made in the CSSR that operate on the principle of a common busbar (i.e., SM 3-20, SM 4-20, SM 52/11 and SM 50/50). The first part of this chapter is devoted to hardware, including both computer configurations and expanding peripheral devices as well as structural and systemic elements. The second part is devoted to software for those systems. The selection of the described hardware and software was made in order to describe devices that are available in the current year or should be available in 1984-85 at the very latest. This chapter merely enumerates the individual systems; their specific availability is dealt with in chapter 10.

The third chapter is devoted to systematically compatible 16-bit systems which, contrary to those dealt with in the preceding passage, come from imports. These include the Soviet SM 4-10 minicomputer and the Romanian INDEPENDENT minicomputer of the 100 series.

The fourth chapter deals with 8-bit SMEP systems operating on the principle of the systemic busbar I 41 developed in VUVT [Research Institute for Computer Technology] in Zilina and produced by the AVT [Computer Technology Enterprises] in Banska Bystrica. These include SM 50/40 cassettes, MVS I and MVS II developmental systems, the SM 50/40 microcomputer, the SM 53/10 and SM 53/20 systems and the VUVT training microcomputer. Here, too, the second part of the chapter describes the software for these systems and cross-programming for 8-bit systems.

The fifth chapter summarizes the findings on operational and installation conditions for the computer technology dealt with in the previous chapters.

The sixth chapter offers information about documentation for SMEP computers. It mentions the documentation accompanying the hardware and lists the individual titles of user program documentation. The chapter further provides a list of literature offered exclusively to participants in training courses offered by the training section of Office Machines. In conclusion, it offers an outline of monographs from various events staged by VTS [Scientific and Technical Society], DT [House of Technology], etc., which deal with SMEP problems.

The seventh chapter deals with training and offers guidance for the selection of courses for managerial personnel, programmers, operators and technicians, including training curricula of Office Machines for any given period of the year.

The eighth chapter mentions planning services and technical assistance provided for users. A part of the chapter is formed by a note about planning systems for remote data processing, reporting of requirements for communications, modems, etc.

The ninth chapter offers information about technical services, i.e., installation, and also deals briefly with the complementation of computer systems.

The tenth chapter outlines the envisioned availability of the described computer systems in individual years.

The eleventh chapter deals with the procedures for requesting computer hardware and software and provides individual addresses that can be used for inquiries, orders, etc. The chapter also describes the manner of deliveries and the warranties offered for hardware and software.

In conclusion, a list of references used in the compilation of this publication is provided.

1.2 SMEP Program

Worldwide development shows that the most dynamic progress within the field of computer technology is going on in the sphere of minicomputers and microcomputers, as they suitably complement large all-purpose computer systems and, of themselves, facilitate the effective automation of management and control in various branches of the national economy, in data processing, etc.

The establishment of the SMEP uniform system of small electronic computers, similarly to the establishment of the JSEP program [Uniform System of Electronic Computers] for large computer systems, was decided upon by the 12th Plenum of the Intergovernmental Committee for CEMA Cooperation in the area of computer technology in 1974.

The key objective of the SMEP program was to provide individual CEMA member countries with a tool for management and control that would provide for the highest possible degree of inheritability of software, hardware, a uniform concept and compatible organizational, methodological and operational principles and standards.

The SMEP program is administered by the SMEP Board of Chief Designers (RHK SMEP) and is participated in by Bulgaria, Hungary, Cuba, Poland, Romania, USSR and CSSR.

The individual participating countries avail themselves of bilateral and multilateral international scientific and technological cooperation. The highest control organ of the SMEP program in the CSSR is the SMEP Chief Designer (HK SMEP). The organ responsible for the development of the SMEP program in the CSSR is the ZAVT [Automation and Computer Technology Enterprises] concern under the jurisdiction of FMEP [Federal Ministry of Electrotechnical Industry]. Within this concern, the key R&D facility and coordinator of many state projects relevant to SMEP is the VUVT in Zilina. The key

producers of SMEP hardware are the ZVT [Computer Technology Plants] concern enterprise in Banska Bystrica and ZVT in Namestovo. Coordinators and participants in state projects in the area of software generation are the fiduciary concern organizations Office Machines and Datasystem, which also function as marketing and servicing organizations for the CSR and SSR. In addition to these organizations, the development of the SMEP program is participated in by dozens of additional organizations from various sectors of the national economy.

From the chronological viewpoint, dealing with the SMEP program is divided into individual stages tied to the solution of individual state-sponsored projects. The SMEP I stage progressed in our country with regard to research, development and the production of prototypes of individual implementational outputs of the state project between the years 1977 and 1980. Production start-up in the SMEP I stage began in 1979, and it can be assumed that products developed in SMEP I will be on the market by 1983.

The R&D aspect of the SMEP II stage falls between the years 1979-1983. The first products from the SMEP II stage will be introduced on the market by Office Machines as early as 1983.

The R&D aspect of the SMEP III stage is planned for 1983-1988.

1.3 System of Markings

Various sources do not always use uniform markings for SMEP hardware that are in keeping with SMEP nomenclature. This publication, in keeping with the recommendation of the office of HK SMEP for the CSSR and with production documentation, uses the following markings:

1) Individual modules and indivisible units such as processors, memories, terminals, etc., which have successfully passed international tests are designated by the symbol CM and a four-digit number, in which the first two digits refer in closer detail to the type of system.

Examples:

CM 2301--processor of the SM 3-20 minicomputer,
CM 2401--processor of the SM 4-20 minicomputer,
CM 2402--processor of the INDEPENDENT 100 minicomputer,
CM 6301--the Robotron 1156 dot printer,
CM C1C1 [sic; should be 0101]--systemic unit, basic structural element.

2) Basic configurations of computers, base systems, etc., generated on the basis of the marketing capacity of a given country are designated by the symbol SM and a combination of digits.

Examples:

SM 3-20--minicomputer of the SMEP I series from the CSSR,
SM 50/40-1--minicomputer system of the SMEP II series from the CSSR.

3) Individual printed circuit plates and partial items bear the designation SM and a four-digit number.

Examples:

SM 2016--extension plate of common busbar,
SM 2138--single-plate minicomputer of the SM 50/40 system,
SM 1355--module of discrete inputs/outputs of the SM 50/40 system.

However, some devices bear more designations of SMEP nomenclature. For example, the ASAD asynchronous adapter on the SM 1201 printed circuit plate underwent international tests under the designation CM 6002, while the SM 50/50 minicomputer system bears the international designation CM 1628. Other devices bear only the designation CM, e.g., the CM 0101 systemic unit, and others merely SM, e.g., the 16-bit parallel adapter PAD 16-SM 0708. Finally, some hardware connected to SMEP bears only a designation of JSEP nomenclature (the EC 6112 punch card reader, some graphic peripheral systems) or bear no designation in SMEP nomenclature (power sources, some structural elements).

It also ought to be pointed out that designation by SMEP nomenclature is not an unequivocal identification of a product; for example, the CM 8511 multiplex comes in seven variants, designation of the CM 7202 display terminal does not specify what type of cable is called for in local, remote or long-distance connection via a modem, the CM 6313 linear printer can designate two basic types of printers with a varying output. Thus, it is advisable that, in the interest of uniform specification of SMEP devices (e.g., in placing orders), use be made of the data listed in the remaining part of this publication until a catalogue of SMEP marketing organizations is published.

2. 16-bit Systems

2.1 Hardware

The series of 16-bit minicomputers and macrocomputers of SMEP is formed by the members of the SMEP I and SMEP II developmental series as follows:

SMEP I:	SMEP II:
--SM 3-20	--SM 52/11
--SM 4-20	--SM 50/50

These computers come in the so-called basic configurations or in configurations oriented toward the needs of users in specific areas. This involves:

--PPPD 1 system for multikeyboard data acquisition for up to 8 work points,
--MARKAB (PPPD 2) system for multikeyboard data acquisition for 32 work points,
--ISAP 1 interactive graphic system,
--IMS 2 integrated measuring system.

Both types of configurations can be further expanded by available hardware and software.

Many of the above-mentioned minicomputers share identical basic properties and an identical structural layout. Differences between individual computers and their potential applications are given, on the one hand, by the differences and capacities of the processors of the individual computers, selection of peripheral units in the computer layout, i.e., the computer's configuration, and on the other by the selection of software.

Systemic Structure

Figure 1 shows the systemic structure of 16-bit computers SMEP with a common busbar (SZ).

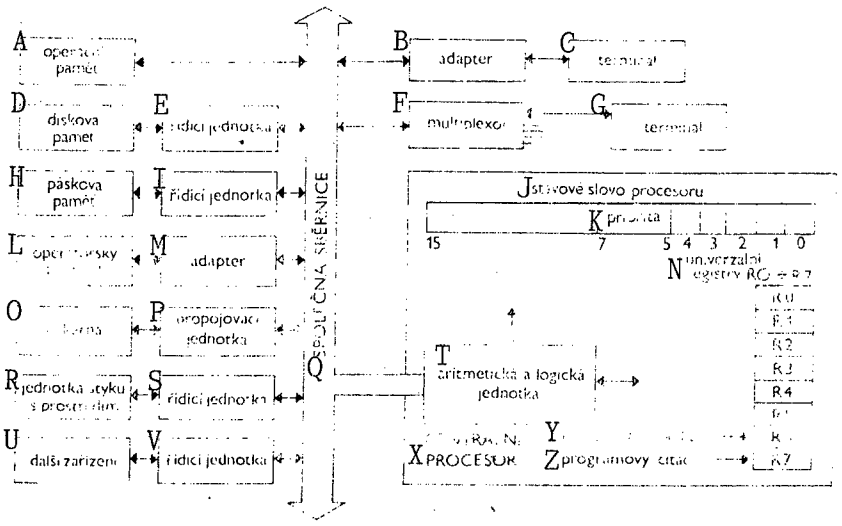


Figure 1. Basic systemic structure of 16-bit SMEP systems

Key:

A) working memory storage
B) adapter
C) terminal
D) disk memory
E) control unit
F) multiplex
G) terminal
H) tape memory
I) control unit
J) processor state word
K) priority
L) operator's terminal
M) adapter
N) multipurpose registers
O) printer
P) interconnecting unit
Q) common busbar
R) interface unit
S) control unit
T) arithmetic and logic unit
U) additional units
V) control unit
X) central processor
Y) storage indicator
Z) program counter

Individual modules of the system (processor, memories, terminal, etc.) are uniformly connected to a common busbar by circuits providing interface between the common busbar and the modules proper. In external memories this coupling is provided by the requisite control units, in peripheral units and terminals by adapters and interconnection units. The system for connecting individual modules to the computer is described subsequently for each individual device.

Structural Layout and Common Busbar

The structural layout of 16-bit SMEP computers makes uses of the addressing principle in which the working memory storage is addressed from address zero, while data registers of input/output systems and registers indicating the state of those systems are located in the addressing space of the last, i.e., the highest 4K memory words.

This space of the highest 4K memory words is reserved for the operation of the computer itself and cannot be used, e.g., for entering programs. With regard to physical implementation, the highest 4K words of the computer's working memory storage are blocked, i.e., unused, and the corresponding data and state registers of all devices are located in individual adapters or control units of peripheral systems.

The form of communication is identical for all systems. An identical set of instructions is used for communication with the working memory storage and with peripheral units, and data on a random address of the common busbar is processed identically, whether it is data in the working memory storage or data in the data register of a peripheral system.

The common busbar contains 51 two-way and 5 one-way conductors, including address, data and control lines. All modules of the system are permanently connected to the busbar by their address inputs and, depending on the control signals of the busbar, they react to their own addresses (see Figure 2).

The common busbar makes it possible to address the working memory storage and registers of auxiliary systems up to 128K words in words or syllables (1 word = 2 syllables). Information is transmitted in 8-bit syllables or 16-bit words. The system of transmission along the busbar is asynchronous, using the query-answer system. This mode permits a very flexible use of the busbar, depending on the internal operating cycles of individual modules.

The busbar is assigned for transmission to the requesting modules by the processor on the basis of priority selection.

In so-called processorless transmission, the processor does not participate in the data transmission (e.g., during the transmission of data between the working memory storage and the disk memory) and can perform other functions.

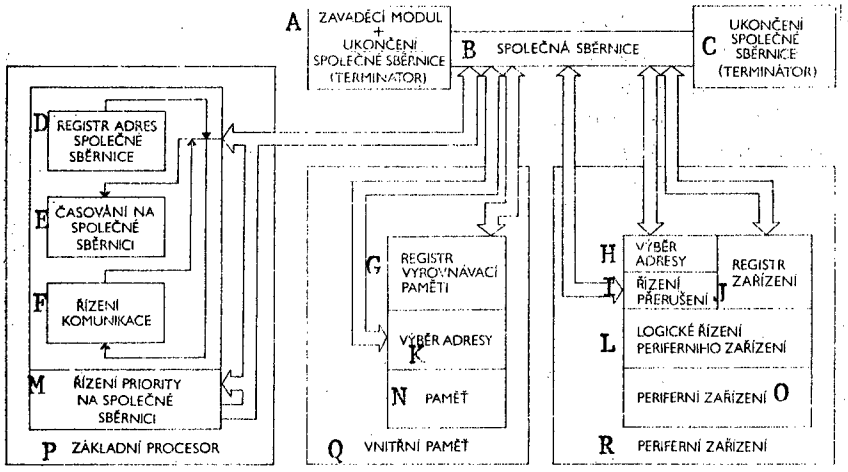


Figure 2. Coupling to common busbar

Key:

A) introductory module and common busbar terminator
B) common busbar
C) common busbar terminator
D) register of busbar addresses
E) timing on common busbar
F) communication control
G) register of buffer memory
H) address selection
I) interruption control
J) system register
K) address selection
L) logic control of peripheral units
M) priority control on common busbar
N) memory
O) peripheral equipment
P) basic processor
Q) internal memory
R) peripheral equipment

Mechanical Concept

The basis of the mechanical concept of SMEP systems is formed by:

--CM 0101 systemic unit,
--printed circuit plates,
--19-inch grid of height 7 U (1 U = 44 mm),
--housing of 19-inch width.

The systemic unit is an integral mechanical unit formed by a small frame holding 96 direct contacting connectors connected into a matrix plate. Interconnection of connector outputs is provided by printed circuits of the matrix plate, and also by wrapped joints. Leads from the systemic unit are made by cable with a connector. The CM 0101 basic systemic unit has four positions for the insertion of printed circuit plates.

The individual printed circuit plates are of the following dimensions:

--one-third plate (single connector)	140 x 240 mm
--two-thirds plate (double connector)	280 x 240 mm
--three-thirds plate (triple connector)	420 x 240 mm

Note: The structural arrangement of the SM 50/50 microcomputer system is partially different and permits the use of plates up to a maximum of the two-thirds size.

The 7U grid is an independent structural unit with built-in power sources and a ventilation unit, into which can be built six CM 0101 systemic units. The grid is suspended in the SMEP housing by means of extendable and collapsible telescopic units. The mechanical concept can be seen in Figure 3; individual elements are described in closer detail in chapter 2.1.9.

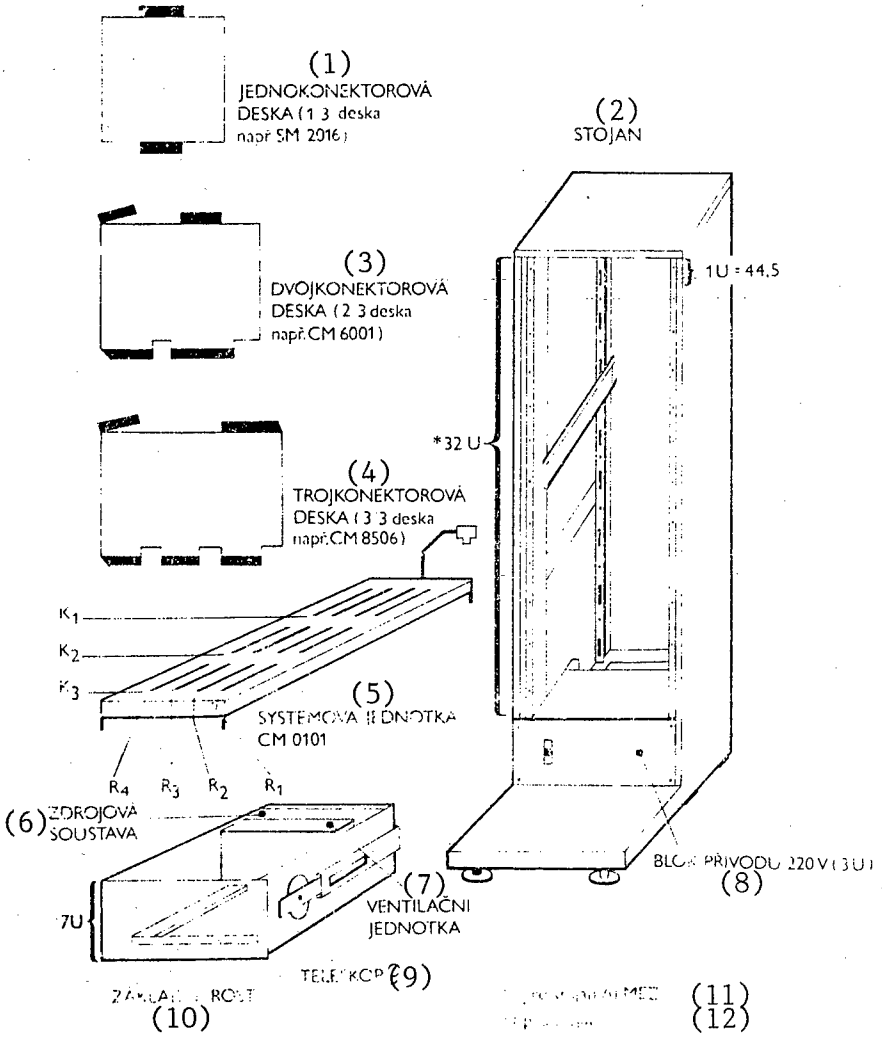


Figure 3. Mechanical concept of SMEP

Key:

1. single connector plate (1/3 plate, e.g., SM 2016)
2. housing
3. double-connector plate (2/3 plate, e.g., CM 6001)
4. triple-connector plate (3/3 plate, e.g., CM 8506)
5. CM 0101 systemic unit
6. power supply system
7. ventilation unit
8. 220 V (3U) power feed block
9. telescoping unit
10. basic grid
11. 37 U for ALMEZ housing
12. 33 U for Fe housing

Systemic Concept

Mechanical elements permit a modular arrangement and, for the systemic viewpoint, easy expansion of the system. This configuration is limited on the one hand by software and on the other by the systemic possibilities. The latter are given by the fact that the common busbar can have a maximum length of 13 m, making it possible to connect to it modules with a total number of 20 systemic loads. In the case of the individual modules that are connected to the common busbar and are described in the subsequent text, the specification "number of loads on common busbar" is given in technical data.

In case a system with a higher number of systemic loads than the mentioned 20 is to be connected to the common busbar, it is possible to expand the number of systemic loads by additional 19 with the aid of the CM 4103 common busbar repeater or, in other words, electrically to extend the length of the common busbar.

2.1.1 Basic Configurations

The subsequent text lists the configurations of computers and user-oriented configurations that will be offered by Office Machines in 1983, depending on production and imports (see also chapter 11).

SM 3-20 Minicomputer

The SM 3-20 minicomputer was developed as the first model of the SMEP I series intended for scientific and technological calculations, acquisition and preprocessing of data, applications in physical laboratories, metrological centers, automation of scientific experiments, control of laboratory experiments, applications in education, agriculture, medicine, etc.

Linkage to other SMEP systems is provided by mutually transferable memory media (magnetic disks, magnetic tapes, floppy disks, perforated tape) and standardized interface for long-distance data transmission (synchronous and asynchronous).

The SYRPOS program system under the MOS RV V2 or DOS RV V2 operating system makes it possible to form computer networks under SM 4-20 or SM 52/11 control.

Linkage to JSEP systems is provided by mutually transferable memory media (magnetic tapes, floppy magnetic disks), or it can be provided by a standardized interface for long-distance data transmission. The emulation routines EC 8514 and EC 7920 now in preparation will facilitate cooperation between SM 3-20 and JSEP in batch or interactive mode.

Basic Characteristics of the SM 3-20 (CM 2301) Processor

The CM 2301 processor provides for control and assignment of the common busbar to individual peripheral systems, performs arithmetic and logic operations and decodes instructions. It operates with parallel transmission of information with 16-bit words or with 8-bit syllables. The CM 2301 processor is further characterized by:

--microprogram control,
--storage-oriented data processing,
--single or double operand instructions,
--direct access to memory,
--four-level multiple interruption mode,
--vectored interruption,
--protection against power outages and automatic new start-up,
--asynchronous contact with other modules of the system.

The SM 3-20 minicomputer is equipped with the NMOS SM 0401 semiconductor memory with a capacity of 32K words and a memory cycle of less than 500 ns.

The grid of the processor of the SM 3-20 minicomputer is shown in Figure 4.

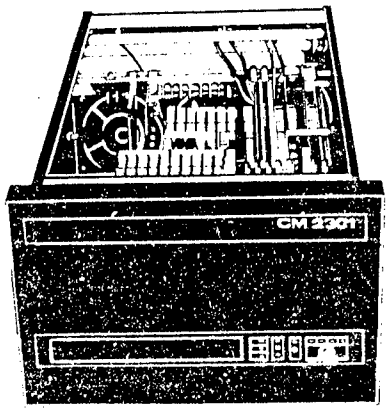


Figure 4. Grid of processor of the SM 3-20 minicomputer

The CM 2301 permits direct addressing of memory with a capacity of 32K words, whereby individual words or syllables can be addressed individually. The set of instructions processed by this processor is called the basic instructional set SMEP.

The processor contains a control unit, an arithmetic and logic unit, control of common busbar, an interruption system, protection circuits against power outages, a simple control panel to which can be added an introductory module and a busbar terminator module.

Technical specifications:

speed of R-R type operations	300,000 op/s
capacity of addressable memory	32K words
maximum user memory capacity	28K words
number of instructions	76
number of address modes	12
instruction addressing	0, 1, 2

Basic Configuration of the SM 3-20 Minicomputer (Figure 5);

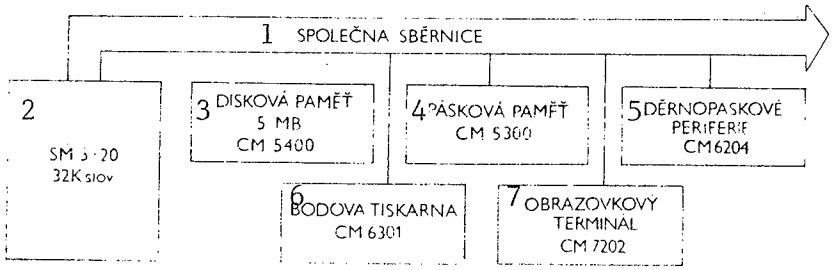


Figure 5. Basic configuration of SM 3-20

Key:
1. common busbar
2. SM 3-20 32K words
3. CM 5400 disk memory 5MB
4. CM 5300 tape memory
5. CM 6204 perforated tape periphery
6. CM 6301 dot printer
7. CM 7202 display terminal

--module of the CM 2301 processor with the SM 0451/B semiconductor memory with 32K capacity, SM 0203 introducing module, SM 0205 timer, CM 5105 control unit of cassette disk memories facilitating connection of up to four CM 5400 disk units (IZOT 1370--Bulgaria) or CM 5403 (KDP 721--Zbrojovka enterprise), a control unit for tape memories making it possible to connect up to four CM 5300 type tape memories, CM 5300.01 or CM 5302 (Bulgaria), the CM 6002 asynchronous adapter for the CM 7202 type display terminal (operator's terminal) and the CM 6001 parallel adapter for connection of a point printer and the SM 2014 terminator module;

--CM 5400 basic cassette disk unit with fixed or exchangeable disk with overall 5 MB capacity;

--CM 5300.01 basic tape unit of an equivalent with a standard 9-ft magnetic tape, recording density 32 bit/mm (800 bpi), NRZI type recording, total capacity 10 MB;

--CM 7202 alphanumeric display terminal with keyboard, display tube capacity 1920 symbols (24 lines x 80 symbols), transmission speed in operator's terminal function maximum 2400 bit/s, serial IRPS interface;

--CM 6301 dot printer (Robotron 1156--GDR), printing speed 100 symbols/s, 132 symbols per line, parallel IRPR interface;

--the module CM 6204 (SPTP/3--Poland) punch-card reader/puncher, reading speed 500 symbols/s, punching speed 50 symbols/s, including the CM 6001 parallel adapter located in the processor grid or, alternatively, replacing the CM 6204 module by the XM 5605 memory module with floppy disk containing a control unit and two CONSUL or MOMFLEX (Hungary) disk units, total capacity 512 KB;

--basic and extension SMEP casing, grids, power sources, cables, accessories. Standard equipment supplied with the SM 3-20 minicomputer is the FOBOS operating system with languages Macroassembler, FORTRAN IV and BASIC.

SM 4-20 Minicomputer

The SM 4-20 minicomputer is the most efficient model of the SMEP I series. It is intended, e.g., for control of R&D experiments, metrological centers, for mass data processing, for control of continuous and discontinuous technological processes, for formation of management information systems, data banks, control of computer networks, etc.

The SM 4-20 has full upward compatibility with the SM 3-20 minicomputer, but offers some advantages over the latter:

--an expanded set of instructions,
--higher input/output transmissivity of information,
--a wider range of applications due to larger capacity of working memory storage of 128K words and more efficient operating systems.

Linkage to other SMEP systems is provided by mutually transferable memory media (magnetic tapes, magnetic disks, floppy disks) and a standardized interface for long-distance data transmission (synchronous and asynchronous). The SYRPOS 1 program system under the DOS RV V2 operating system facilitates the formation of computer networks with 16-bit SMEP computers.

Linkage to JSEP systems is provided by mutually transferable memory media (magnetic tapes, floppy magnetic disks), or a standardized interface for long-distance data transmission. The EC 8514 and EC 7920 emulation routines now under preparation will permit cooperation between SM 4-20-JSEP in batch or interactive mode.

Basic Characteristics of SM 4-20 (CM 2401) Processor

The CM 2401 processor provides for the control and assignment of common busbar to individual peripheral systems, performs arithmetic and logic operations and decodes instructions.

The basic properties of the CM 2401 processor coincide with those of the CM 2301 processor. In a wider context the CM 2401 processor may include:

--the processor proper,
--an introductory module,
--common busbar terminator module,
--operator's panel,
--simple and programmable timer,
--processor of floating decimal point (Figure 6).

These modules are mutually interconnected by means of their common busbar, except the processor of the floating decimal point, which is connected directly to the processor proper.

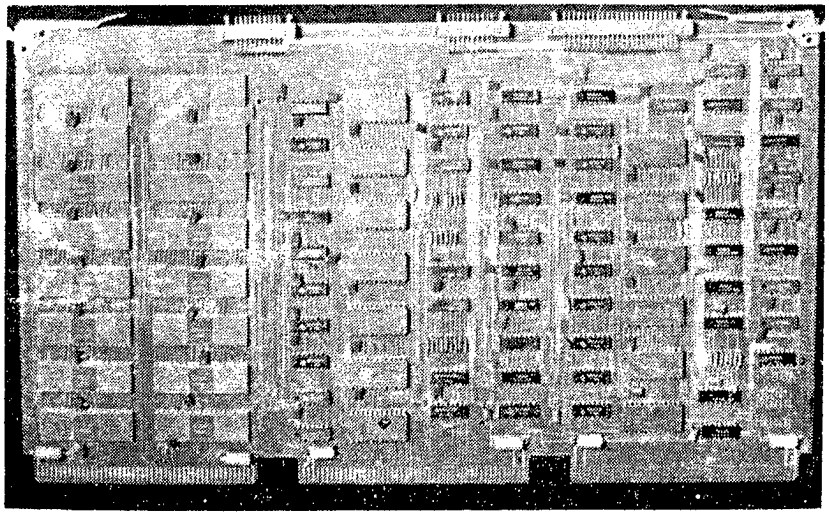


Figure 6. Processor of floating decimal point for SM 4-20

The CM 2401 processor permits addressing the 124K capacity memory by words or by syllables.

The set of instructions is formed by:

--basic set of instructions SMEP (i.e., same as the SM 3-20),

--expanded set of instructions (i.e., e.g., multiplication, division, shift, logic and systemic instructions),

--set of instructions for the decimal floating point processor.

Technical specifications:

speed of R-R type operations	420,000 op/s
capacity of addressable memory	128K words
maximum user memory capacity	124K words
number of instructions	84
number of instructions in floating decimal point	45
number of address modes	12

The SM 4-20 minicomputer comes equipped with a self-correcting NMOS CM 3511 semiconductor memory with a capacity of 128K words and memory cycle of 850 ns and access time of 550 ns. The memory facilitates self-correction of a single error and by indication of a double error during transmission (Figure 7).

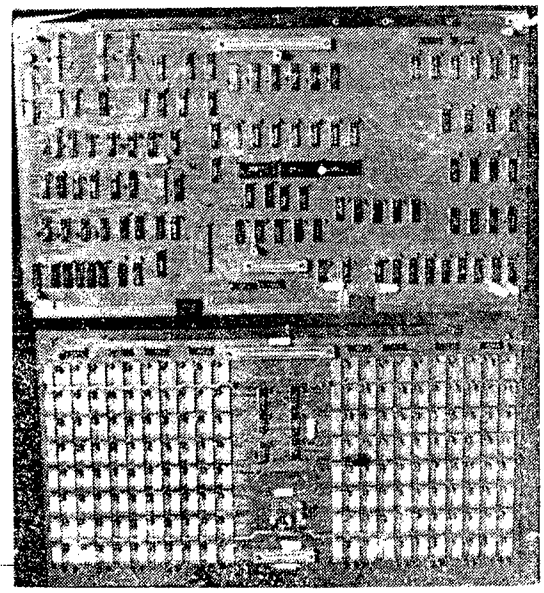
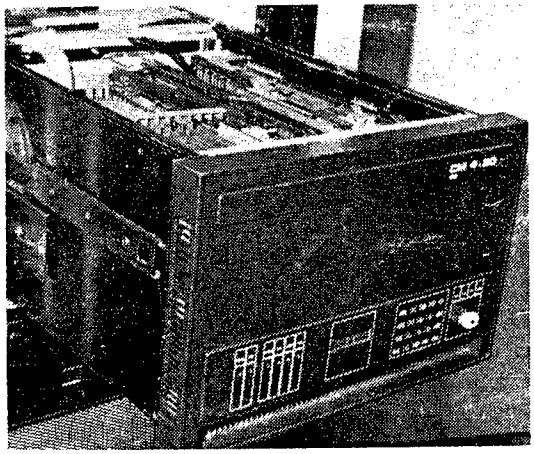


Figure 7. Disassembled NMOS technology CM 3511 memory of 128K words (256K syllables) capacity for computers SM 4-20 and SM 52/11

It is planned to expand the CM 2401 processor in the future with a programmer's panel (Figure 8) which offers many testing and tuning opportunities. Its operation is controlled by its own 8-bit microprocessor.

Figure 8. CM 2401 processor with programmer's panel



Basic Configuration of the SM 4-20 Minicomputer (Figure 9):

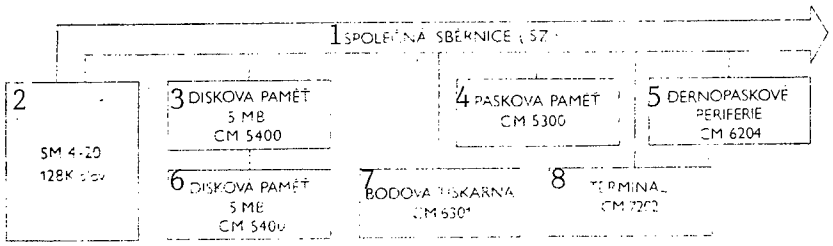


Figure 9. Basic configuration of SM 4-20

Key:

1. common busbar (SZ)
2. SM 4-20 128K words
3. CM 5400 disk memory with 5 MB
4. CM 5300 tape memory
5. CM 6204 perforated tape peripheries
6. CM 5400 disk memory with 5 MB capacity
7. CM 6301 dot printer
8. CM 7202 terminal

--Module of the CM 2401 processor with CM 3511 semiconductor 128K memory, SM 0203 introductory module, SM 0205 simple timer, SM 0204-CM 2001 programmable timer, SM 4220 processor for floating decimal point, CM 5105 control unit of cassette disk memories facilitating the connection of up to four CM 5400 (IZOT 1370--Bulgaria) or CM 5403 (KDP 721--Zbrojovka) disk units or their combination, control unit of magnetic tape memories facilitating the connection of up to four CM 5300.01 tape units or their equivalents CM 5302 and CM 5303, the CM 6002 asynchronous adapter for the CM 7202 display terminal (operator's terminal) and the CM 6001 parallel adapter for connection of a dot printer, the SM 2014 terminator module;

--two CM 5400 disk units (basic and expanding), each unit having a fixed and exchangeable disk of a total capacity of 5 MB;

--CM 5300.01 basic tape unit or equivalent with a standard 9 ft magnetic tape, recording density 32 bit/mm (800 bpi), NRZI recording mode, total capacity 10 MB;

--CM 7202 alphanumeric display terminal, display tube capacity 1920 symbols (24 lines x 80 symbols), transmission speed in operator's terminal function maximum 2400 bit/s, IRPS serial interface;

--CM 6301 (Robotron 1156--GDR) dot printer, printing speed 100 symbols/s, 132 symbols per line, IRPR parallel interface;

--CM 6204 (SPTP/3--Poland) module reader/perforator of perforated tape, reading speed 500 symbols/s, perforating speed 50 symbols/s with the requisite CM 6001 parallel adapter located in the processor grid or, alternatively, instead of the CM 6204 module, the CM 5605 module of memory with floppy disk containing a control unit and two disk units with a total capacity of 512 KB;

--basic and expansion SMEP casing, grids, power sources, cables, accessories.

Figure 10. Basic and expansion casing of the SM 4-20 minicomputer

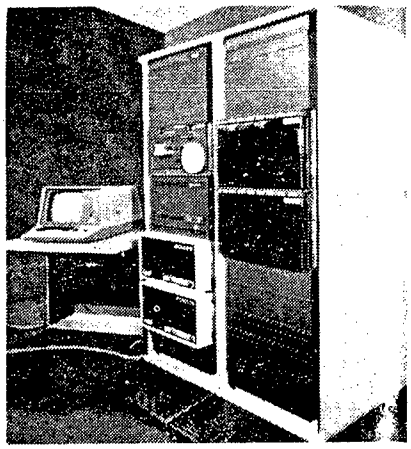


Figure 11. Basic configuration of the SM 4-20 minicomputer with one expansion tape memory (without dot printer)

Standard equipment delivered with the SM 4-20 minicomputer includes the DOS RV V2 operating system with the languages Macroassembler, FORTRAN IV, BASIC, FORTRAN IV PLUS and BASIC PLUS 2.

CM 3103 Ferritic Working Memory Storage

Semiconductor memories that are supplied as standard equipment with the basic configurations of the SM 3-20 and SM 4-20 computers require permanent power feed in order for the information stored in them to be retained even in case of a power outage. That is why computers equipped with semiconductor memory come equipped for such a case with a battery power source which will provide power for the memory for at least 2 hours, thus permitting the retention of information.

On the other hand, ferritic memories operate on a principle that facilitates the permanent storage of information that cannot become lost even after a long time,which offers advantage or is necessary in many applications. For that reason, ferritic memories continue to be used despite their larger dimensions and higher power input.

Available as an option for the SM 3-20 minicomputer is a ferritic memory with a 32K-word capacity and the following specifications:

total capacity	32K words
access time	⩽ 400 ns
memory cycle	⩽ 1000 ns
number of loads on common busbar	1
structural design	independent 7U grid
power feed/input	220 V/250 VA
weight	37 kg

Also available for SM 4-20 minicomputers is a 64K-word capacity memory with the following specifications:

total capacity	64K words
access time	⩽ 400 ns
memory cycle	⩽ 1000 ns
number of loads on common busbar	2
structural design	independent 7U grid
power feed/input	200 V/350 VA
weight	45 kg

SM 52/11 Minicomputer

The SM 52/11 minicomputer is an efficient computer system of the SMEP II series. It is suitable for:

--high-performance applications in real time,

--multiuser systems and multipurpose applications with time sharing.

The SM 52/11 minicomputer has bottom to top program compatibility with the SMEP series of 16-bit computers, i.e., SM 3-20, SM 50/50 and SM 4-20. It differs from the mentioned types primarily by:

--user-oriented microprogramming,
--expanded set of instructions,
--higher transmissivity,
--higher speed,
--system for monitoring of errors.

Linkage to other SMEP systems is provided by mutually transferable memory media (magnetic tapes, magnetic disks, floppy disks) and a standardized interface for long-distance data transmission (synchronous and asynchronous). The SYRPOS 1 program system under the DOS RV V2 operating system permits the formation of computer networks based on SMEP minicomputers.

Linkage to JSEP systems is provided by mutually transferable memory media (magnetic tapes, floppy magnetic disks), or can be provided by a standardized interface for long-distance data transmission. The EC 8514 and EC 7920 emulation routines now in preparation will permit collaboration between SM 52/11 and JSEP in batch or interactive mode.

The basic feature of the SM 52/11 minicomputer design is again a common busbar; the devices connected to it communicate on the query-answer principle, whereby one system controls the operation of the common busbar in the function of a master and the other carries out requirements in the function of a slave. Conflicting situations are resolved on the basis of priorities. The processor is connected to the common busbar between the working memory storage and the input/output system, thus providing for the requisite switching off of the CACHE memory (see below) in contact between the input/output system and the working memory storage.

Figure 12 shows the block layout of the SM 52/11 minicomputer.

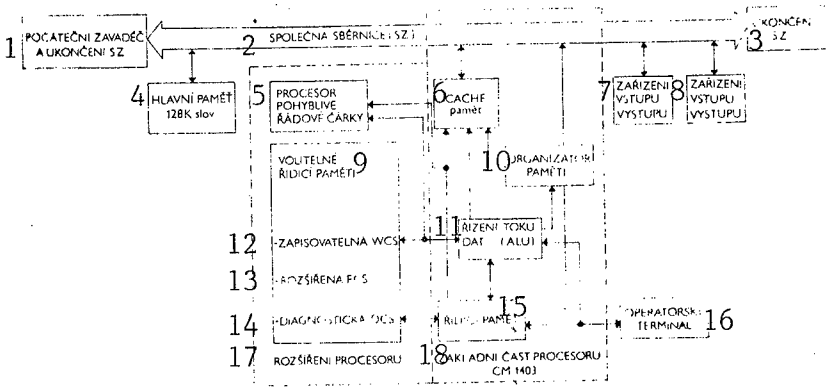


Figure 12. Block layout of the SM 52/11 minicomputer

Key:

1. initiator and common busbar terminator
2. common busbar (SZ)
3. SZ terminator
4. main memory 128K
5. floating decimal point processor
6. CACHE memory
7. input/output system
8. input/output system
9. selectable control memories
10. memory organizer
11. data flow control (ALU)
12. recordable WCS
13. expanded ECS
14. DCS diagnostics
15. control memory
16. operator's terminal
17. processor expansion
18. CM 1403 basic processor part

CM 1403 Processor of the SM 52/11 Minicomputer

The CM 1403 processor contains the following basic blocks:

--microprogram control unit,
--arithmetic unit,
--circuits for internal arithmetic with floating decimal point,
--CACHE memory with 2048-syllable capacity (1 syllable = 8 bits),
--memory organizer,
--common busbar control,
--interruption system,
--protective circuits against power outage,

--circuits for monitoring process errors,
--programmer panel.

The arithmetic and control unit permits the use of 132 instructions which include instructions for multiplication, division, 32- and 64-bit arithmetic with floating decimal point and user-oriented microprogramming and servicing instructions. The basic set of instructions is identical with the SM 3-20 set of instructions. The expanding set of instructions, compatible with the SM 4-20 minicomputer set of instructions, controls arithmetic operations with fixed decimal point and multiple shifts or cycles. The floating decimal point processor is compatible with SM 4-20 and operates sequentially with simple or doubled accuracy.

The CACHE memory accelerates processor access to data and instructions stored in the memory. Thanks to this arrangement, the resultant cycle of the main memory does not exceed 550 ns. A copy of preselected parts of the main memory can extend to 2080 bytes. In addition to speed, use of the CACHE memory offers the advantage of limited use of the common busbar, thus creating room for mutual transmissions between input/output systems and memory.

The programmer's panel forms a part of the processor and makes the work of the system operator and of the technician easier. It makes it possible to work with the processor's registers and with memory cells of the entire main memory even while the computer is in operation. Standard functions make it possible to initiate the program of the introductory module directly or start up an optional diagnostic module.

The memory organizer makes it possible to expand a 16-bit physical address into an 18-bit virtual address and thus expand the address space from 32K to 128K words and in multiple-user and multipurpose applications provides for the protection and transferability of programs.

The processor can operate in two modes:

--privileged, allowing performance of the entire set of instructions;

--user-oriented, where the program is protected against performing instructions that could cause a modification of the control program or use of memory space assigned by a privileged program or another user.

The interrupting system operates with four basic priority levels. The system uses a storage where in case of program interruption the processor stores important program information which will permit automatic return to the same point in the program under conditions that existed prior to interruption.

The core of circuits for monitoring errors is formed by a set of registers. At the occurrence of an error, the information stored in them facilitates their expedient pinpointing and analysis. If an error occurs in the CACHE memory, in the floating decimal point processor or in user control memory, these modules can be disconnected. The system can continue to operate, but, of course, at a limited speed of carrying out of instructions.

Protection against power outage becomes operational as soon as voltage in the mains network drops below 190 V. The program run is interrupted and within 2 ms the program attending the outage memorizes the data contained in the registers and the states of peripheral units. When voltage is restored, the interrupting vector is used to start up the program of voltage restoration and the state which existed prior to the outage is restored. In some extreme caes the introducing module can be used for a repeated start-up of the system. The basic processor can be expanded by the following optional modules (see the block diagram).

The external processor for floating decimal point FPP (32- and 64-bit format) is in asynchronous operation with the basic processor, where it is connected to its inner busbar. FPP accelerates the operation of the internal processor of the floating decimal point. Arithmetic computations are carried out in parallel at high speed, thus considerably increasing the system's output in processing instructions involving the floating decimal point. It is used with great advantage particularly in complicated scientific and technical calculations. It has at its disposal six internal 64-bit registers.

The set of instructions for internal arithmetic for the floating decimal point is identical with the set of instructions for the optional processor of the floating decimal point.

In the CM 1403 is available a part of the address space of the processor's control memory that can be used by the user. For the basic system are reserved 2.5K words of address space. The remaining 1.5K words can be used for three optional microprogram modules which offer a high degree of flexibility and the potential for expansion of microprogram control.

The RAM-type SM 0211-3 recordable control memory with the requisite software--referred to as WCS--has a 1024-word capacity and is used for generating user microprograms, including their tuning. The control word width is 48 bits + 3 parity bits.

The ROM-type SM 0211-1 expanded control memory--referred to as ECS--has a 1.5K-word capacity and control word width of 48 bits and can be used for the permanent storage of user microprograms generated and tuned on, e.g., WCS. These microprograms can be used only for reading.

The ROM-type SM 0211-2 diagnostic control memory--referred to as DCS--has a maximum 2K-word capacity and control word width of 55 bits. It actually involves a technical application of the ECS module. It is used for microprogram testing of the basic processor and for localization of errors to the level of the plate module, a group of integrated circuits and in the DCS memory proper. It is a standard part of the processor.

The CM 1403 processor is structurally located in the standard 19-inch SMEP grid and is formed by six three-connector SMEP plates, two atypical plates for the programmer's panel and systemic units. In the processor grid is also located a memory, and a four-plate processor for arithmetic with a floating decimal point; into one position is inserted one of the optinal modules DCS, ECS or WCS, and three positions are reserved for the interface module, the simple timer and the introductory module.

The CM 1403 processor comes equipped with a self-correcting CM 3511 memory with 128K-word capacity. Thanks to the use of the rapid CACHE memory, the memory cycle is shortened to less than 550 ns. The described processor does not make it possible to expand internal memory beyond the 128K-word capacity.

Technical specifications of the processor proper:

speed of carrying out R-R type operations	1,800,000 op/s
control word width	48 bits
number of internal registers	92
number of instructions	139
control memory capacity	4K words
number of address modes	12
number of registers for all-purpose application	8
CACHE memory capacity	1K words
number of loads on common busbar	1
processor grid weight	up to 70 kg

Set of Instructions:

--basic set of SMEP instructions (same as SM 3-20 or SM 50/50 in basic version 32K words);

--EIS expanded set of instructions (same as SM 4-20, or SM 50/50 with 128K word memory);

--set of instructions for arithmetic with floating decimal point (same as SM 4-20);

--instructions for user microprogramming;

--servicing instructions.

Basic Configuration of the SM 52/11 Minicomputer (Figure 13):

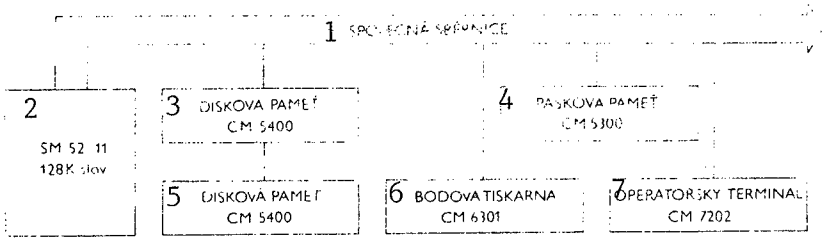


Figure 13. Basic configuration of SM 52/11

Key:
1. common busbar
2. SM 52/11 128K words
3. CM 5400 disk memory
4. CM 5300 tape memory
5. CM 5400 disk memory
6. CM 6301 dot printer
7. CM 7202 operator's terminal

--The module of the SM 52/11's processor with CM 3511 semiconductor memory with 128K-word capacity, introductory module, SM 0205 simple timer, SM 0204 programmable timer, SM 0211-2 diagnostic control memory, control unit of CM 5105 cassette disk memories allowing connection of up to four CM 5400 (IZOT 1370--Bulgaria) or CM 5403 (KDP 721--Zbrojovka) disk units or their combination, control unit of magnetic tape memories allowing connection of up to four CM 5302 tape units or their variant, CM 6002 asynchronous adapter for the CM 7202 display terminal (operator's terminal) and the CM 6001 parallel adapter for connection of a point printer, SM 2014 terminator module;

--power supply grid with programmer's panel 7U high;

--two CM 5400 disk units (basic and expansion unit), each unit with a fixed and exchangeable disk with a total capacity of 5 MB;

--basic CM 5302 tape unit with standard 9 ft magnetic tape, recording density 32 bit/mm (800 bpi), NRZI recording, maximum reel diameter 267 mm;

--CM 7202 alphanumeric display terminal, display tube capacity 1920 symbols (24 lines x 80 symbols), transmission speed in operator's terminal function max. 2400 bit/s, IRPS serial interface;

--CM 6301 (Robotron 1156--GDR) dot printer, printing speed 100 symbols/s, 132 symbols per line, IRPR parallel interface;

--basic and expansion SMEP casing, grids, power sources, cables, accessories.

Additional SMEP expansion modules can be connected to the SM 52/11 minicomputer. The standard equipment delivered with the SM 52/11 minicomputer includes the DOS RV V2 operating system with languages Macroassembler, FORTRAN IV, BASIC, FORTRAN IV PLUS and BASIC PLUS 2.

SM 50/50 Microcomputer System

The variant of the SM 50/50 16-bit computer developed in the CSSR operates on the principle of a common busbar, providing its full compatibility with the SM 3-20, SM 4-20 and SM 52/11 systems.

The SM 50/50 microcomputer is suited for, e.g.,

--acquisition and preprocessing of data,

--use as an office computer,

--formation of computer and terminal networks,

--control of processes.

It is a modular system which in the subsequently described variants that are currently in preparation makes it possible to use not only modules developed specially for the SM 50/50, but also modules that are already currently available within the SMEP program.

CM 1628 Processor for SM 50/50

The CM 1628 processor is a microprogrammable processor on a 2/3 SMEP plate bearing the designation SM 0252. The set of instructions is identical with that of the SM 3-20 minicomputer.

The CM 1628 processor will be provided in the next stage with the following optional systems:

--memory organizer with CACHE memory facilitating expansion of the address space from 32K words to 128K words,

--SM 0255 plate, the programmer's panel.

The optional modules come on plates with conforming dimensions and are connected with the processor's plate by couplings in the upper part of the plates.

A part of the CM 1628 processor is the terminator module of the common busbar:

--SM 2014 for grid variant (same as for SM 3-20, SM 4-20 and SM 52/11),

--SM 2037 for the cassette variant.

The cassette and terminal variants must at the same time use the "combined module" mentioned below and, for the grid variant, the "initial lead-in" + "simple asynchronous adapter" or "combined module."

The processor itself is designed on the basis of microprocessor sections.

From the functional viewpoint it can be divided into the following blocks:

--arithmetic logic unit,

--microprogram control unit,

--common busbar control,

--interrupting system,

--circuits for protection against power outages.

The arithmetic logic unit ALU with circuits formed by microprocessor sections providing the requisite functions consists further of a PSW register (16-bit state word) and an internal address decoder. The microprocessor section is a 4-bit arithmetic logic unit with a 16x4 bit fast RAM memory, a register for multiplication and division operations and control, multiplex and decoding circuits. These four sections are arranged and connected in cascade for the formation of 16-bit words. The PSW register provides for the storage of information about the sign bits of preceding operations, indication of requests for interruption, recording of priorities, and data about the preceding and current mode. Four bits of the state word remain unused in reserve. According

to the applied mode, the role of the internal address decoder is to provide transmission from/to the PSW register and internal registers in microprocessor section or transmissions between registers and registers of auxiliary systems connected to the common busbar.

The microprogram control unit facilitates the decoding of instructions, their implementation and, in case of need, microinstructional branching. It consists of a simple 16-bit IR register into which every instruction is stored for the time needed for carrying it out so that the instructions decoder correctly takes over the control signals for the computation of operands and the computation itself. Subprograms can contain types of instructions within the system's own set of instructions. Other instructions must be adapted to the systemic properties of the processor. The control unit further contains a control microprogram RMP memory and a microinstruction register. The control microprogram memory consists of PROM-type memories of 512-word capacity, whereby each word is 56 bits long, determining within cycles the operation of the arithmetic and logic part and of transmission and decision-making circuits. One part of the control word determines the subsequent address of the program, another part facilitates the modification of formed addresses by means of microprogram branching.

The priority interrupting system has four levels, and selection progresses in sequence with the priority level of the request for interruption, depending on the distance of the device connected to the common busbar from the processor. The processor differentiates and services all external, internal and instructional interruptions.

The circuit for protection against power outages interrupts the program when a voltage drop occurs in the network and within 2 ms stores the contents of registers into memory storage. When voltage is restored, so is the state of the system prior to the outage.

A part of the processor is also formed by a generator of clock cycles which generates two types of clock pulses:

--short pulses with a period of 180 ns,

--long pulses with a period of 280 ns.

Technical specifications:

word length	16 bits
direct addressing	32K words
potential expansion of addressing	up to 128K words
number of registers for general use	8
data processing format	8 or 16 bits
addressing modes	12
number of instructions	84
speed of carrying out of R-R operations	415,000 op/s
number of loads on common busbar	1
weight	up to 0.4 kg
feed voltage/max. consumption	+ 5V/7A

Other Modules of the SM 50/50 System

The 64K Word Dynamic RAM Memory With Parity Control

Is designed primarily for SM 50/50 microcomputer systems, but can also be used in the SM 52/11 and SM 4-20 systems. As long as memory capacity is modified to 32K words, it can be used even for the SM 3-20. Its 2/3 SMEP plate is inserted into the grid and is fed power by its system. Word length is 16 + 2 control bits; each syllable of this parity memory is thus controlled by one bit.

The functioning of parity circuits is controlled by the program accessible memory register. Operating modes are: word reading, word entry and syllable entry.

Technical specifications:

word length	16 + 2 bits
access time	< 500 ns
memory cycle	< 600 ns
operating modes	word reading word entry syllable entry
number of loads on common busbar	1
maximum plate capacity	64K words
addressing potential	0-128K words
memory elements	MHB 4116
weight	up to 0.7 kg
feed voltage	+ 5 V + 12 V in reserve
maximum power input	17 W

The 16K Word Dynamic RAM and 12K Word EPROM Memory

is designed exclusively for the SM 50/50 system. It is also contained on a 2/3 plate inserted into the grid containing the power supply. It is connected to the common busbar as an independent functional block. The independent RAM part facilitates the entry and reading of information, while the EPROM part is designed only for the reading of information.

With regard to the parity circuits and the state register, the RAM part is designed similarly to the NOMS 64K semiconductor working memory storage. Information in the EPROM part is not protected by parity bits. Properties of the RAM part coincide with those of the NMOS 64K byte semiconductor working memory storage.

Technical specifications:

RAM part:

word length	16 + 2 bits
control	parity
maximum plate capacity	16K words

EPROM part:

word length	16 bits
memory plate module capacity	4K words
maximum plate capacity	12K words
access time	550 ns
memory cycle	600 ns
number of loads on common busbar	1

Memory Organizer with CACHE Memory

This single-plate module allows expanded addressing of memory up to 128K words and makes contact between processor and memory more efficient to the point where the system's output increases by approximately one-half.

As in the SM 52/11 system, the CACHE memory is a very fast semiconductor memory of small capacity used on the second level of the memory system which does not expand potential capacity, but keeps copies of information from the first level and substantially accelerates the processor's access to memory.

The system with CACHE memory takes advantage of the fact that occurrence of reading operations amounts to 85 to 90 percent and occurrence of entry operations is only 15 to 10 percent, and that programs contain repetitive sequences of instructions that have to be performed several times. In communication with memory the processor anticipates in reading primarily data from CACHE memory and only if it fails to obtain them does it take them from the working memory storage and store them simultaneously in the CACHE memory. During entry, the data are recorded in both memories. Thus, in the worst case, during a second reading from the same memory cell the processor can read data from the CACHE memory. Since the CACHE memory is several times smaller than the working memory storage, the mapping mechanism assigning cells to both the CACHE and working memory operates so as to store in the CACHE memory entire cyclically repetitive sections of characteristic sequences of instructions processed by the given system. Therefore, the overall efficiency of processing also depends on the manner of operation with this memory (cyclic sections, repeat sequences of instructions, etc.). Three registers are available for program control and for diagnostics.

The CACHE memory of the SM 50/50 system has a capacity of 1K 27-bit words, one of its cells reflecting up to 128 various cells of the working memory storage. The structural design places this memory on a 2/3 plate shared with the memory organizer.

The memory organizer is functionally and systemically identical with the memory organizer of the SM 4-20. In multiprogram systems with working memory storage capacity in excess of 32K words it provides for controlled access and protection of memory and reserving of data segments. It operates in privileged mode

(performing the entire set of instructions) or in user mode (blocks the program against carrying out a certain type of instructions or against the user of memory space allocated to other programs).

Technical specifications:

CACHE memory:

capacity	1K word
word length	27 bits (16 data bits 7 associative sign bits 4 service bits)
access time	80 ns
access mode	associative address
information control	by parity

Memory organizer:

address space	virtual 16 bits physical 18 bits
operation modes	user, systemic
transfer: number of pages	16 (8 for each mode)
page length	32 to 4098K words
number of loads on common busbar	1
weight	up to 0.4 kg
feed voltage/maximum consumption	5 V/8 A

It will be possible to expand the SM 50/50 system by the following modules:

--CM 8512 quadruple asynchronous series adapter (QUASAD) for the connection of a maximum of four input/output systems with the current loop interface (20 or 40 mA) or with the interface CCITT V.24 (closer description offered below);

--single-plate combined module combining the functions of a lead-in module, simple timer and asynchronous ASAD series adapter for contact with operator's terminal;

--any random SMEP expansion module with connection to the common busbar (parallel or series adapter, interface units, etc.).

Additional modules for the SM 50/50 will be readied for production, e.g.:

--discrete inputs/outputs module,
--analog inputs/outputs module,
--control units for CM 5113 cassette disk memory,
--control unit for tape memory.

These modules will be compatible with the other 16-bit systems.

Configuration of the SM 50/50 Microcomputer System

The basic structural variant of the SM 50/50 system is a programmable terminal. The basic programmable terminal unit is built into the display terminal and contains the logic control of the terminal itself, a processor of the SM 50/50 microcomputer with a 32K word memory, a series adapter for long-distance data and supplementary modules.

The SM 50/50 microcomputer will be supplied with the FOBOS operating system.

Also based on the programmable SM 50/50's terminal is the configuration of the PPPD 1 acquisition system based on the SM 50/50, and the IMS 2 measuring system based on the SM 50/50.

In addition to the SM 50/50 programmable terminal variant, in the next stage will be made available an SM 50/50 variant in a 7U high grid suitable, e.g., for building into a casing.

PPPD 1 Acquisition System with SM 3-20

The basic hardware configuration (Figure 14) of the system for acquisition, preparation and preprocessing of data consists of:

--the SM 3-20 minicomputer in basic configuration,

--1 to 7 CM 7202 type expansion display terminals with series interface.

Key:
1. SM 3-20 32K words
2. CM 5300.01 tape memory
3. CM 5400 disk memory
4. CM 6301 dot printer
5. CM 6204 perforated tape peripheries
6. common busbar
7. CM 7202 display terminal

Figure 14. Basic configuration of PPPD 1 with SM 3-20

The program system designed for this configuration is the PPPD 1 V 02.C UNIVERSAL, the description and functional potential of which are described in the chapter on "Software."

PPPD 1 Acquisition System with SM 50/50

The basic hardware configuration of the system for the acquisition, preparation and preprocessing of data (Figure 15) is based on the programmable terminal, the basic unit of which is built into a display terminal and will consist in the first stage of the following:

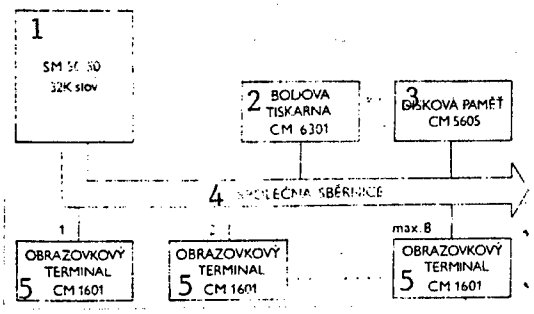


Figure 15. Basic configuration of PPPD 1 with SM 50/50

Key:
1. SM 50/50 32K words
2. CM 6301 dot printer
3. CM 5605 disk memory
4. common busbar
5. CM 1601 display terminal

--plate of display terminal logic;

--combined module plate including the lead-in module, series interface for the operator's terminal and a simple timer. The lead-in module contains memories with fixed programs of lead-in programs from various media, tests of internal diagnostics and a program emulating the function of the computer panel on the terminal;

--plate of SM 50/50 processor;

--plate of RAM semiconductor memory of 28K words. Use is made of one-half of a 64K-word RAM memory with the proviso that the last 4K words are blocked for the system;

--one to two plates of the QASAD 4-channel asynchronous adapter facilitating the use of IRPS interface up to 500 m or a modem interface according to CCITT V.24 designated as S 2. Two plates facilitate the interconnection of seven additional terminals; the remaining eighth connection can be used for direct connection of the SM 50/50 system with a computer on a hierarchically higher level (e.g., SM 4-20);

--CM 6001-PAD 8 parallel adapter for connection of the CM 6301 dot printer;

--plate for memory with flexible disk interconnection, permitting the connection of the disk memory control unit in the CM 5605 unit with two disk units with a capacity of 256K bytes each to the basic SM 50/50 unit without common busbar leadout.

The acquisition system's basic unit is supplemented by:

--floppy disk memory (2 disk units),

--1 to 7 expansion CM 1601 display terminals.

The PPPD 1 V 03 program system (see chapter on "Software") is planned for the acquisition system based on the SM 50/50 with a flexible disk memory.

The basic unit of the PPPD 1 system built into a display terminal with the CM 5605 disk memory in a desk-top variant is shown in Figure 16.

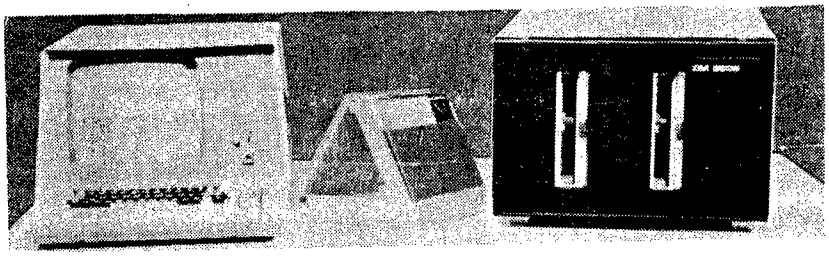


Figure 16. Basic unit of the PPPD 1 system on the basis of SM 50/50 with the CM 5606 disk memory

MARKAB (PPPD 2) Acquisition System with SM 4-20

The MARKAB (PPPD 2) is designed for 16-bit SMEP minicomputers with memory up to 128K words (Figure 17).

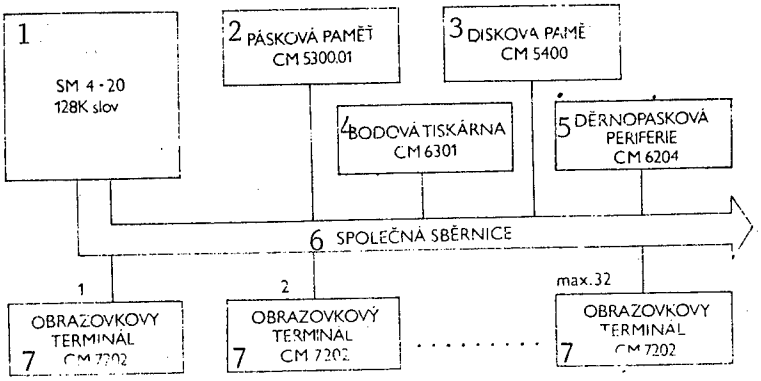


Figure 17. Basic configuration of MARKRAB [sic] (PPPD 2) with SM 4-20

Key:
1. SM 4-20 128K words
2. CM 5300.01 tape memory
3. CM 5400 disk memory
4. CM 6301 dot printer
5. CM 6204 perforated tape periphery
6. common busbar
7. CM 7202 display terminal

The hardware configuration is formed by:

--the basic configuration of the minicomputer with internal memory of 128K words, a disk memory and the CM 8511 multiplex with a number of connections corresponding to the number of installed terminals (the multiplex can be replaced by the CM 6002 asynchronous adapters, the number of which corresponds to the number of installed terminals);

--expansion serial display terminals up to a maximum number of 32.

The software designed for this acquisition system is MARKAB (original work designation PPPD 2).

ISAP 1 Graphic System with SM 4-20

The interactive system for automated design ISAP is a set of hardware and software for the automation of design and planning operations.

Hardware configuration (Figure 18):

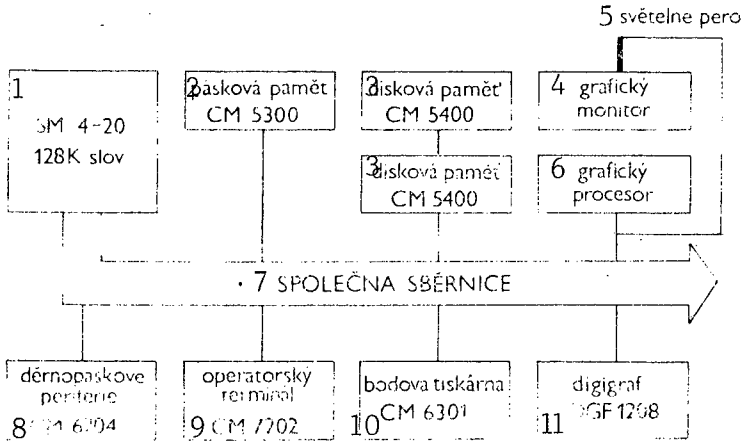


Figure 18. Basic configuration of ISAP 1

Key:

1. SM 4-20 128K words
2. CM 5300 tape memory
3. CM 5400 disk memory
4. graphic monitor
5. light pen
6. graphic processor
7. common busbar
8. CM 6204 perforated tape peripheries
9. CM 7202 operator's terminal
10. CM 6301 dot printer
11. DGF 1208 digigraf

1. Casing:

--basic grid containing the CM 2401 processor with CM 3511 semiconductor memory with 128K-word capacity, the SM 0203 lead-in module, the SM 0205 simple timer, the CM 2001 programmable timer, processor for floating decimal point, control unit for CM 5105 disk memories allowing connection of up to four CM 5400 (Bulgaria) or CM 5403 (Zbrojovka) disk units or their combination, adapters for connection of peripheral devices and the SM 2014 terminator module;

--CM 5400 basic disk unit with insertion of cassette disk from above with a fixed and exchangeable disk of 5 MB capacity;

--CM 5400 expansion disk unit;

--CM 5605 floppy disk memory module containing a control unit and two MOMFLEX or CONSUL disk units with a total capacity of 512 KB or, in another variant, CM 6204 or CM 6208 perforated tape reader/puncher module.

2. Casing:

--basic grid containing a processor of the CM 2301 graphic terminal of the GVM 01 graphic vector monitor with a 16K-word memory, adapters for the connection of peripheral devices;

--expansion grid containing the tape memory control unit making it possible to connect up to four tape units (CM 5300.01, CM 5302 or CM 5303 or their combination) and adapters for the connection of peripheral devices;

--CM 5302 basic tape unit (or equivalent) with standard 9 ft magnetic tape, recording density 32 bit/mm (800 bpi) in NRZI mode;

--CM 5302 tape unit (or equivalent).

Independent devices:

--CM 7202 display terminal with IRPS serial interface in the function of operator's terminal;

--CONSUL C 2111 dot printer with graphic mode, i.e., modification which permits point printing of various graphic information;

--GVM 01 graphic vector monitor with light pen;

--CM 6313 (VIDEOTRON VT 27090) line printer with printing speed of 900 lines/m;

--Digigraf 1208 drafting system--imaging part of the EC 7907 complex;

--Digitizer 1208 read-off system--input part of the EC 7907 complex;

--operator's panel-tablet, an auxiliary interactive device for the selection of one of eight functions in cooperation with the graphic monitor.

The ISAP 1 system can be further expanded by other available hardware with interface used in SMEP.

The basic software supplied with the ISAP 1 system includes:

--DCS RV V2 operating system,

--SM GRAF set of graphic programs,

--GFS set of graphic programs.

This basic software can be supplemented by MINIG software and by functional software according to individual applications.

IMS 2 Measuring System with SM 50/50

The configuration of the SM 50/50 system for control of the IMS 2 measuring systems is similar to that of the PPPD 1 system.

The basic SM 50/50 module built into the display terminal contains the following plates (Figure 19):

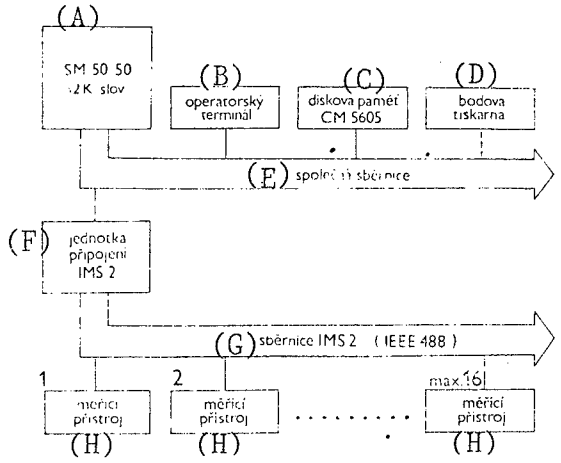


Figure 19. Basic configuration of IMS 2 with SM 50/50

Key:
A. SM 50/50 32K words
B. operator's terminal
C. CM 5605 disk memory
D. dot printer
E. common busbar
F. IMS 2 connecting unit
G. IMS 2 busbar (IEEE 488)
H. measuring instrument

--logic plate of display terminal,

--combined module plate,

--SM 50/50's processor plate,

--32K-word memory formed by plate of 64K-word RAM memory,

--reserve for connecting either a dot printer or the DIGIBAK plotter,

--interconnecting plate for floppy disk memory,

--first plate of the IMS 2 interconnecting unit,

--second plate of the IMS 2 interconnecting unit.

The IMS 2 interconnecting unit is designed on two 2/3 SMEP plates, of which one is connected to the common busbar and the second to the IMS 2 busbar, both being mutually interconnected. It permits transmission speed of up to 250 KB/s and connection of up to 15 measuring instruments by cable not exceeding 4 m in length (a close description of the IMS 2 unit appears elsewhere).

The language devised for programming IMS 2 is IMS-BASIC S, which is an expansion of the BASIC language and is stored in the library under the title IBASS.

2.1.2 Disk Memories

External memories with magnetic disk media can be divided into several groups:

--Cassette disk memories with 5 MB capacity (these disk memories are delivered routinely in basic configurations of SMEP minicomputers, and also as expansion modules), or of double capacity of 10 MB.

CM 5400, CM 5403 Cassette 5 MB Disk Memories

Cassette disk memories serve for recording, storage and reading of larger volumes of data. Information is stored on a 12-sector magnetic disk in a type EC 5269.01 (IZOT 5269, IBM 5440) cassette with insertion from top or in a type BASF 631 (IBM 2315) cassette with frontal insertion.

A cassette disk memory configuration is formed by:

--CM 5105 control unit,

--disk units proper:

CM 5400 (Bulgaria) with insertion from top, or
CM 5403 (KDP 721, KDP 723--Zbrojovka) with frontal insertion.

The CM 5105 control unit provides for the connection of the memory units to the common busbar and their control, i.e., remembering a given command, requested addresses, blocks and state reports generated in the performance of an operation. During data transmission between the computer's working memory storage and individual disk memories the control unit checks the number of words being transmitted, generates the sector address, coding of the recorded signal and performs data selection with control of the read signal.

The program operation of the disk memory is organized on the common busbar via seven program registers with transmission of data blocks between the working memory storage and the control unit.

The control unit is located in the grid of the central processor, where it takes up the space of two systemic units. The control unit is connected by cable to the first unit of the disk memory. In case another expansion memory unit is being added, the terminating member is taken out of the first disk memory unit and in its place is inserted the cable connector of the expansion (second) disk; this terminating member is placed into the expansion disk.

In adherence to the rules for connections it is possible to connect a maximum of four CM 5400, CM 5403 units or their combination to one CM 5105 control unit.

The memory unit itself (Figure 20) contains one fixed and one exchangeable disk. The disk surface is divided into 204 addressable tracks (4 being reserve tracks), which are divided into 12 addressable sectors with fixed length of 256 words of 16 bits each, i.e., 512 bytes. The entire unit has a 5M-byte capacity with median access time of approximately 50 ns.

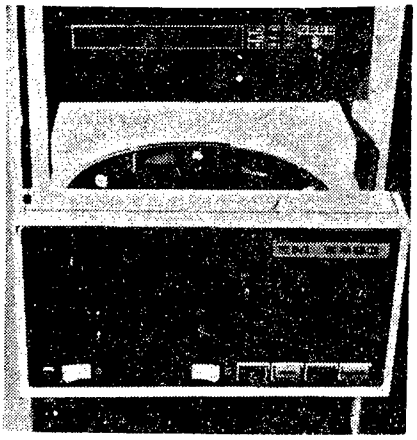


Figure 20. CM 5400 disk unit

Technical specifications for disk units appear in Table 1.

Table 1. Specifications for CM 5400 and CM 5403 cassette disk memory units

Specification	CM 5400	CM 5403 KDP 721	CM 5403 KDP 723
Overall capacity (MB)	5		
Recording type	Double frequency-DF		
Max. data transmission speed (Mbit/s)	2.5		
Max. recording density (bit/mm)	87		
Number of oper. surfaces on disk	2		
Number of sectors	12		
Revolution speed (rpm)	2400		
Number of tracks	200+4	200+3	
Median access time (ms)	50	45	
Module height in casing	6 U	13 U	7 U
Feed voltage	220 V/50 Hz		
Power input	350	350	

The variant of the CM 5403 KDP 723 disk memory now in preparation differs from the CM 5403 KDP 721 in that the KDP 721 type is structurally formed by two grids; it contains the disk unit proper and a power source of a total height of 13 U; the KDP 723 type has the power source built into the grid of the disk unit itself and its total height is 7 U.

CM 5410 10 MB Disk Memory

The CM 5410 (Bulgaria) disk memory is an innovated variant of the CM 5400 cassette disk memory of 5 MB capacity with a double density of recording (i.e., 408 tracks are used instead of 204) and, consequently, also a double capacity of 10 MB.

All other specifications coincide with those of the CM 5400 disk memory. The CM 5113 control unit that is being developed is necessary for connecting these memories and has systemic specifications identical to those of the CM 5105 control unit, making it possible to connect up to four 10M-byte and 5M-byte disk units.

CM 5405 29 MB Disk Memory

The CM 5405 large-capacity disk memory (variant IZOT 5061--Bulgaria) serves for storing a large volume of data with direct access. The disk memory is formed by a control unit (which makes it possible to connect up to eight disk units of the EC 5061.C type) and two basic disk units.

The memory medium is formed by the EC 5261-01 20-surface disk pack. The control unit has 12 registers accessible by program. Data are recorded with double frequency with 2200 bpi density. It has 10 sectors, each with 256 words.

The control unit with power sources structurally forms independent grids. These grids are placed into a casing which is a part of this disk subsystem. In the casing there is free space of 15 U for building in additional SMEP expansion modules. The disk unit is an independent device (Figure 21) which is connected to the control unit by cable.

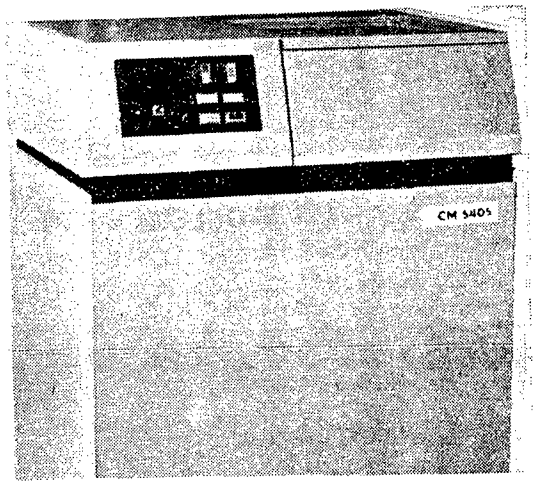


Figure 21. CM 5405 29M byte disk unit

Technical specifications:

Type of medium	29M byte disk pack
Type of recording	NRZI with double density
Median access time	50 ms
Power feed	3x380/220 V
Disk unit power input	1.5 kVA
Disk unit dimensions	610x775x975 mm
Disk unit weight	180 kg

CM 5605 Floppy Disk Memory

External floppy disk memory is a peripheral system facilitating recording, storage and readout of information on a magnetic medium--a floppy disk. The carrier with the recording layer is in an envelope made of plastic with openings for the head, for the hub of the rotary spindle and for a fixed index mark. The inner packing of the disk is lined with a fibrous material which

cleans the disk's surface. Data are recorded on one side of the disk, which is divided into 77 tracks with 26 sectors of 128 byte each. The disk is standardized in accordance with ISO TC 97/SC-11.

The CM 5605 floppy disk memory is an independent structural module in 16-bit SMEP minicomputers which is placed into a SMEP casing and contains:

--a control unit with interface for connection to the common busbar, the so-called interconnection plate (Figure 22),

--2 disk units,

--a grid including a ventilation unit and power supply sources.

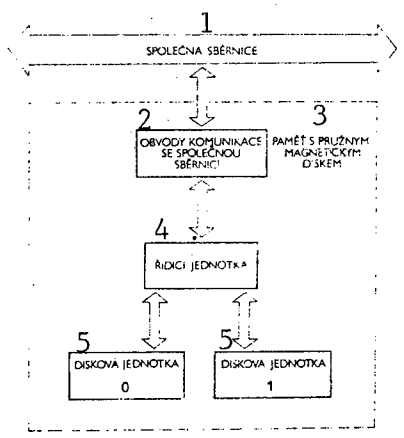


Figure 22. Systemic design of a floppy magnetic disk memory

Key:
1. common busbar
2. circuits for communication with common busbar
3. floppy magnetic disk memory
4. control unit
5. disk unit

The control unit provides for communication with the common busbar of the computer, control of movement of the reading/recording head, selection of the addressed space, generation of format in data recording, control of read data and assessment of error states. A part of the control unit is a micro-program memory with 256 byte capacity and a buffer memory with a capacity of 128 bytes per sector.

The program operation of floppy disk memory occurs through two registers.

The control unit facilitates the connection of two disk units.

The CM 5606 was supplied in the past with CONSUL C 7112.5, and MOMFLEX MF 3200 floppy disk units. Currently, the MF 6400 and C 7113 are supplied. Technical specifications for both units appear in Table 2.

Table 2. Technical specifications for floppy disk memories with CONSUL and MOMFLEX memory units

Specifications	C 7112.5	MF 3200
Memory's format capacity (KB)	2x256	
Number of working surfaces	1	
Number of tracks on floppy disk	77	
Number of sectors per track	26	
Number of symbols per sector	128	
Recording density (bit/mm)	128	
Speed of revolutions (rpm)	360±2%	
Type of recording	DF	
Motion period by 1 track (ms)	10	
Motion arrest period (ms)	25	
Head contact period (ms)	40	
Median access time (ms)	500	
Speed of data transmission (kbit/s)	250	
Module height	7 U	
Power supply	220 V + 10%, -15%/50Hz	
Power input (VA)	350	
Weight (kg)	44	40

The floppy disk memory is mechanically built into a 7 U high grid (Figure 23). The grid can be placed into any casing of computers SM 3-20, SM 4-20, SM 52/11. A design variant of the CM 5605 for the SM 50/50 will be intended for desk-top use.

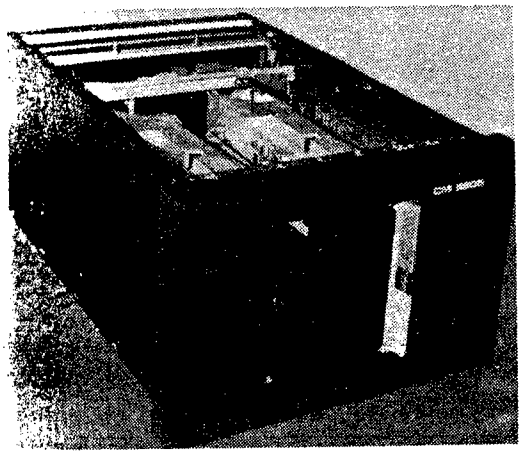


Figure 23. CM 5605 floppy magnetic disk memory with CONSUL mechanisms

The floppy disk memory puts one load on the common busbar.

The memory can be connected to the system in two ways: either the SM 0602 interconnection plate is placed into a free systemic unit and connected by a cable that comes with the accessories to the systemic unit which forms part of the floppy disk memory, or the interface plate remains in the systemic unit of the floppy disk memory and the control unit is connected directly to the common busbar by cables that come with the accessories.

Note: A floppy disk memory with selectable single or double recording density is currently under development.

2.1.3 Tape Memories

Magnetic tape memory is an external memory with successive selection. Information is recorded on 8 tracks (8 information + 1 parity bit) of a standard magnetic tape 12.8 mm (½ inch) wide with density of 32 bit/mm (800 bpi) by the NRZI recording system.

Tape memory configuration is formed by:

--a control unit,

--a distribution panel for connecting a maximum of four tape memory units,

--the so-called small tape memory units proper, types CM 5300 (see Figure 24), CM 5300.01 or the older type IZOT 5003 and the so-called large units, types CM 5302 (Figure 25) and CM 5303, all Bulgarian products.

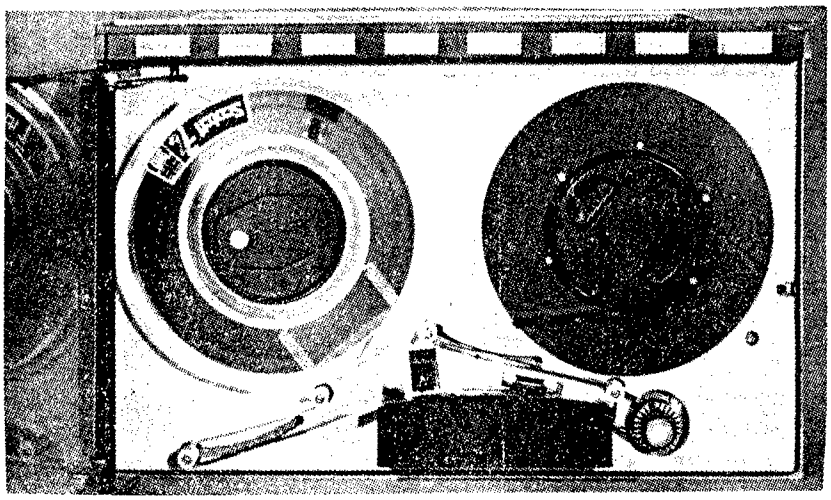


Figure 24. CM 5300 tape unit

Figure 25. CM 5302 tape unit

The control unit provides for retention in memory of assigned command, transmission address of data, length of the transmitted block and status reports generated during implementation of the command. After decoding the command the control unit provides for selection of the requested unit, control of tape advance, generation of block format during recording as well as decoding of data during reading with simultaneous transmission of data between the working memory storage and the buffer memory of the control unit.

Information is stored on the tape in blocks, whereby several blocks can be delineated by a set mark. Block search is facilitated by the interblock gap which precedes every block. The correctness of the recorded information is controlled by generating a longitudinal parity bit LRC for each symbol and cyclical control CRC after every block. The organization of recording on tape at this level meets ISO R 1863 and CSN [Czechoslovak State Norm] 36 94 64 recommendations.

The program operation of the control unit via the common busbar is organized via six program registers.

The control unit takes up structurally one whole systemic unit and contains two 2/3 and two 3/3 plates. The standard location of this systemic unit is in the grid of the expansion casing.

The control unit of tape memories puts one load on the common busbar, regardless of how many memory units are connected to the control unit. The control unit is connected by cables that belong among its accessories to the distribution panel.

The distribution panel contains for the connection of each tape unit one pair of connectors for units of the type starting with CM 53. and two separate pairs of connectors for units IZOT 5003, meaning that it is possible to connect to the distribution panel any random combination of tape units up to four, but only up to two of that number can be units of the IZOT 5003 type.

In the casing--in which is located the grid with the tape memory control unit--at least one tape memory unit must be located, because the distribution panel for the connection of other tape memory units is located in the back part of the casing directly behind this first memory unit.

Basic data on magnetic tape memory units are shown in Table 3.

Table 3. Technical specifications for tape memories

Specifications	IZOT 5303	CM 5300	CM 5300.01	CM 5302	CM 5303
Reel diameters (mm)		216		264	
Total reel capacity (MB)		10		20	
Speed of data transmission kB/s)		10		20	36
Operational tape advance speed (m/s)		0.32		0.64	1.14
Start-stop duration (ms)		20±2		15±1	8.3±0.6
Rewind speed (m/s)		1.5		2.5	2.7
Number of tracks			8		
Recording density (bit/mm)			32		
Recording system			NRZI		
Entry format			ISO/R-1863-1971		
Power feed			220 V + 10%, -15%/50 Hz ± 1 Hz		
Maximum power input (VA)	359	250	250	650	750
Dimensions: height (mm)		211 (7 U)			621
width (mm)		482			482
depth (mm)		450			540
Weight		35			60

Note: Work is currently under way to develop the domestic MMP 45 tape memory comparable to the CM 5303 with selectable density of 32 or 64 bits/mm and to develop a new control unit for recording NR 21 and PE.

2.1.4 Peripheral Units Using Paper

The peripheral systems using paper media--those that constitute standard equipment of SMEP minicomputers in basic configurations or as an expansion system--include:

--CM 6204 reader/puncher module of perforated tape SPTP/3 (Poland),
--CM 6208 reader/puncher module of perforated tape CONSUL,
--EC 6112 punch card reader with control unit.

These systems are subsequently described in closer detail. In addition to these subsequently described systems, from the technical viewpoint it is possible to connect to the common busbar any additional systems using paper media only with a standard interface via a corresponding adapter (e.g., FS 1501 independent perforated tape reader with parallel interface adapted to IRPR interface via the CM 6001 parallel adapter).

CM 6204 Perforated Tape Reader/Puncher SPTP/3 (Poland)

This combined module serves for the input and output of perforated tape in SMEP computers. The module contains a perforated tape reader, DT 105 perforated tape puncher and electronic equipment. The device uses an IRPR interface and must be connected to the common busbar via the CM 6001 parallel adapter, which is placed in a systemic unit in the processor grid.

The module of the CM 6204 reader/punchers structurally forms an independent grid and is placed into a SMEP casing (see Figure 26).

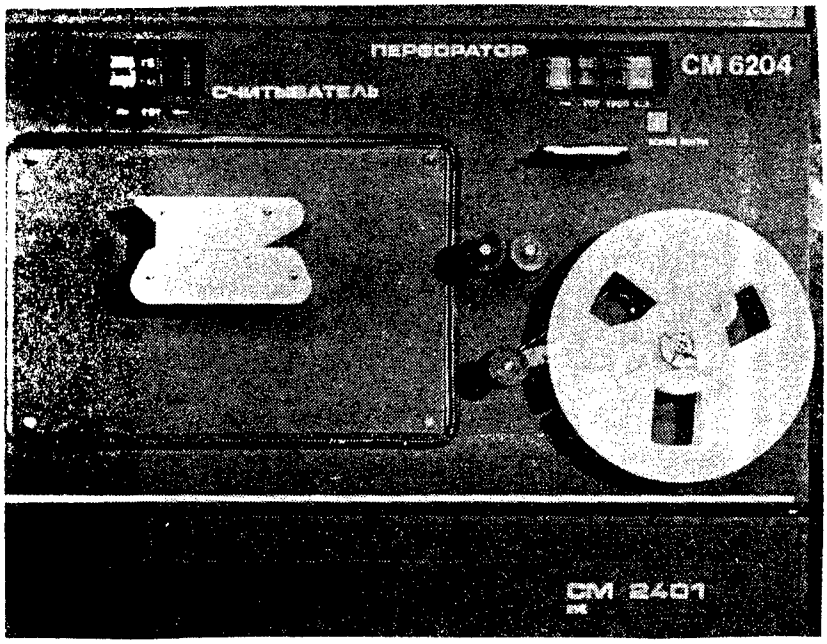


Figure 26. Module of the CM 6204 perforated tape reader/puncher in casing of the SM 4-20 minicomputer

[Russian inscriptions in photo: left = reader, center = perforator]

Technical specifications:

Type of medium	5- or 8-track perforated tape
Perforating speed	50 symbols/s
Reading speed	150/300 symbols/s
(depending on type of reader)	500/100 symbols/s
	1000/200 symbols/s
Number of connections to common busbar	1
Dimensions for building into casing	height 6 U
Weight	42 kg
Power feed/power input	220 v/350 VA

CONSUL CM 6208 Perforated Tape Reader/Perforator

The CM 6208 carries out the same functions as the CM 6204, with the following most essential differences:

--it is a domestic product used as CONSUL 333.3 perforator and CONSUL 337.201/A reader,

--the grid the device is built into is 7 U high in SMEP casing.

Technical specifications:

Reading:

Type of medium	8-track perforated tape
Reading speed	300 symbols/s

Perforation:

Type of medium	5- or 8-track perforated tape
Perforating speed	55 symbols/s
Number of connections to common busbar	1
Building-in dimensions	height 7 U
Weight	42 kg
Power feed/power input	220 V/500 VA

EC 6112 Perforated Card Reader Set

The Aritma 2050-EC 6112 perforated card reader with the SM 0706 control unit facilitates the reading of information recorded on standard and nonstandard punch cards and its transmission into 16-bit SMEP computers.

The input medium can be an 80- or 90-column punch card, or an abbreviated card.

The SM 0706 control unit (actually a PAD 12 parallel adapter) contains an input channel which provides for the transmission of data from the reader into the computer and circuits which provide for communication with the card reader and with the common busbar of the computer.

The control facilitates the connection of readers type EC 6112 (11, 21, 31, 41, 52, 71); the connection of another type of reader is accomplished by a different selection of couplers and substitution of the reader's adapting resistors.

The program operation of the system is provided with the aid of three registers. The EC 6112 is structurally an independent desktop unit (see Figure 27); the SM 0706 control unit is a 2/3 plate which is placed at random into any free systemic unit position. A part of the set is formed by the reader, desk, PAD 12 and interconnecting cables:

Technical specifications:

Type of medium	80- or 90-column punch cards
Data flow width	12 bits
Type of transmission	parallel, asynchronous
Number of addressable registers	3
Number of loads on common busbar	1
Maximum cable length	5m
Reader dimensions	560x430x340
Reader weight	39 kg
Power feed/power input	220 V/200 VA

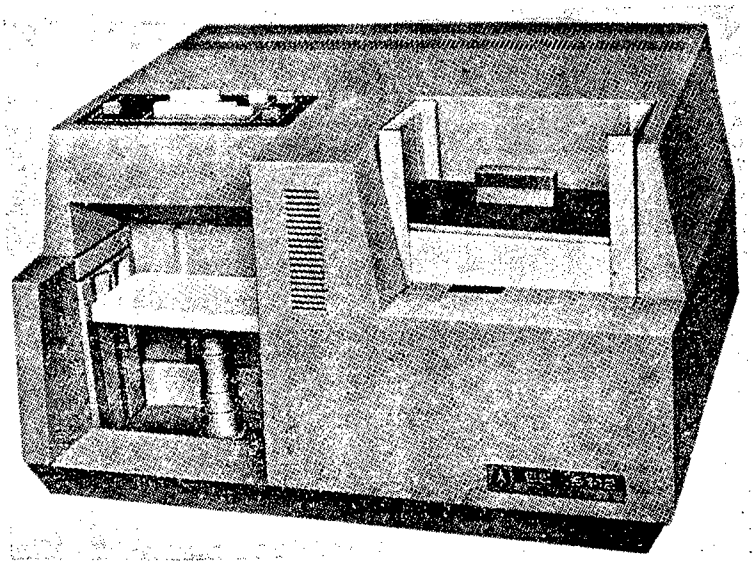


Figure 27. EC 6112 punch card reader

2.1.5 Printers

A printer is an output device facilitating the imaging or printout of information.

The subsequent text describes:

--CM 6301--Robotron 1156 (GDR) dot printer,
--CM 6313--Videoton 27090 or 27060 (Hungary) line printer.

No attention is paid in this part to the CM 6302 (DZM 180--Poland) dot printer, which does not constitute standard equipment of the mentioned types of SMEP minicomputers, nor is any mention made of the CM 6303 (CONSUL C 2111) dot printer, which is currently not being supplied and is described among developmental systems in the chapter on 8-bit systems. The specifications of the CM 6303 printer correspond to those of the printer used in the terminal with print CM 7108. A variant of the CM 6303 printer with graphic output is mentioned in the section on "Graphic Systems."

CM 6303 Robotron 1156 (GDR) Dot Printer (Figure 28)

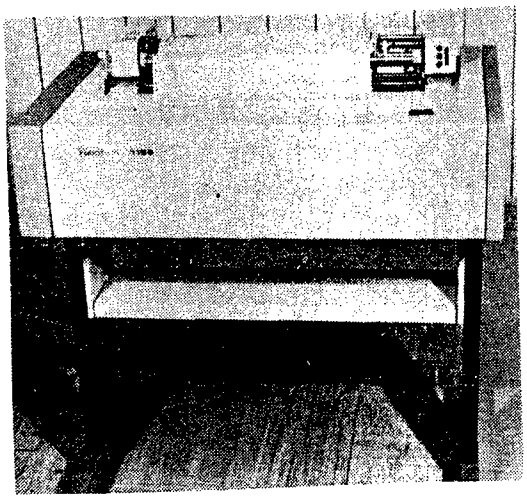


Figure 28. CM 6301--Robotron 1156 dot printer

The dot printer provides a medium rate of information output from the computer. It is usually used as a systemic printer of a computer or as a printer for printing the contents of the CM 7202 display terminal (hard-copy).

Technical specifications:

Printing speed	100 symbols/s 30 symb/s in start/stop mode
Printing width	max. 132 symb/line
Set of symbols	64 symbols (Latin alphabet)
Symbol imaging	5x7 matrix
Symbol height	2.5 to 2.7 mm
Symbol width	1.7 to 1.9 mm
Symbol spacing	2.54 mm
Line spacing	4.23 (5.08) mm
Print direction	forward and reverse
Number of copies	1 + 5
Number of loads on common busbar:	
in systemic printer function	1
in hard-copy function	0

Power supply from network	220 V + 10% - 15%
Maximum power input	250 VA
Weight	max. 45 kg
Dimensions	977x500x250 mm

The CM 6301 uses a parallel interface and in the function of a systemic printer it must be connected to the computer via the CM 6001 parallel adapter over a maximum distance of 15 m.

In hard-copy function the CM 6301 is directly connected to the CM 7202 terminal. The "PRINT" mode of the CM 7202 terminal will be shown in Figure 41.

CM 6313 Videoton VT 170 90 (Hungary) Line Printer

The CM 6313 line printer makes it possible to print out a large number of output sets from a computer and thus finds application in, e.g., mass data processing (Figure 29).

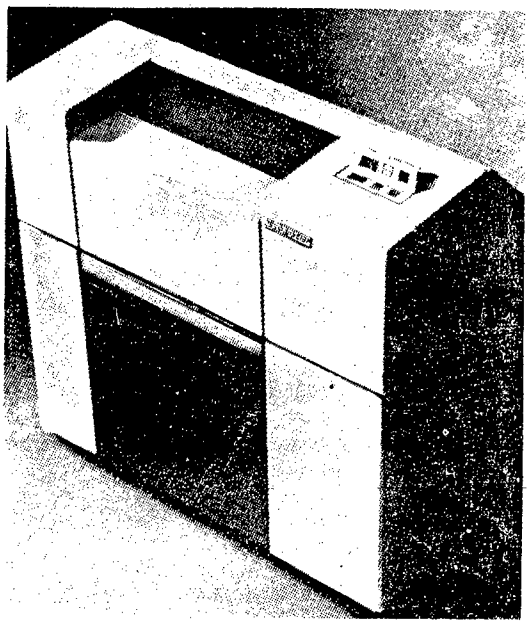


Figure 29. CM 6313 line printer

Technical specifications:

Printing speed VT 270 90	900 lines/min
VT 270 90 (older type)	650 lines/min
Number of symbols per line	136
Max. symbol width	1.65 mm
Max. symbol height	2.4 mm
Set of symbols	64 (Latin alphabet)
Number of copies	1 + 5
Number of loads on common busbar	1
Voltage feed from network	220 V + 10% - 15%

Current consumption from network	6 A
Max. power input	1.5 kVA
Weight	max. 200 kg
Dimensions	1000x600x1050 mm

Note: Preparations are being made for delivery of the VT 230 00 printer with a printing speed of 300 lines/min.

The line printer is an independent device and is connected to the system via the CAM 6001 parallel adapter by cable with maximum length of 15 m.

2.1.6 Graphic Systems

Graphic systems include various devices serving for the input and output of graphic information. From the systemic viewpoint these devices can be connected to SMEP minicomputers by the requisite adapters, but some of them form a part of graphic complexes (ISAP 1).

The subsequent part describes:

--CM 7405 graphic terminal,
--GVM 01 graphic vector monitor,
--Digigraf 1712 drafting system,
--Digigraf 1208 drafting system,
--Digitizer 1208 read-off system,
--BAK ST coordinate plotter,
--CM 6303/graphic output dot printer with graphic mode of operation.

CM 7405 Graphic Terminal

This graphic vector terminal is an interactive input/output device in SMEP systems calling for the graphic processing of information, e.g., in design, planning and other areas. The terminal also allows the processing of alphanumeric data and modification of graphic information by means of a light pen (see Figure 31) and functional keyboard.

It is also possible to connect drafting equipment to the device to make a permanent copy.

The graphic terminal consists of the following key parts (see Figures 30 and 31):

--processor of terminal with memory,
--graphic processor,
--GVM-01 graphic monitor with light pen,
--keyboard or display terminal or terminal with printout.

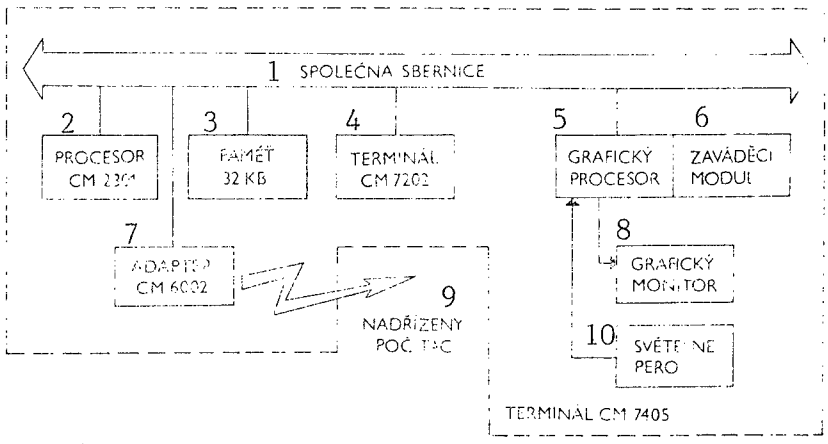


Figure 30. CM 7405 terminal

Key:

1. common busbar
2. CM 2301 processor
3. 32 KB memory
4. CM 7202 terminal
5. graphic processor
6. graphic processor
7. CM 6002 adapter
8. graphic monitor
9. hierarchically higher computer
10. light pen

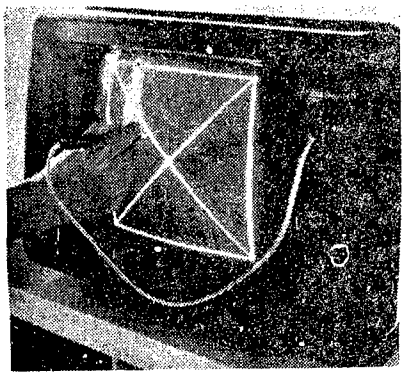


Figure 31. GVM01 graphic monitor with light pen (or first part of the CM 7405 graphic terminal)

The CM 7405 terminal processor is based in the CM 2301 processor (of the SM 3 20 minicomputer), internal memory has a 32K byte capacity.

The graphic processor provides linkage with the CM 2301 processor through the common busbar, communication with the CM 2301 processor and conversion of data for the graphic monitor. The graphic processor is structurally located in a grid with the CM 2301 processor. Its individual plates (three 3/3 and one 2/3) are located in a special systemic unit which takes up six positions. A lead-in module forms a part of the graphic processor.

The GVM-01 graphic monitor provides for the imaging of generated vectors and alphanumeric symbols on the display and also provides connection between the processor and the light pen.

The graphic terminal is connected long-distance or locally via an asynchronous adapter to a hierarchically higher SM 4-20 or SM 52/11 computer (see Figure 30).

The communication lead-in module provides direct connection of the keyboard or display terminal with the hierarchically higher computer and introduction of programs from the latter into the working memory storage of the graphic terminal.

The program operation of the mentioned system is provided by the operating systems DOS RV V2 or FOBOS 1 or 2 in cooperation with the expanding program product SM GRAF working with the language FORTRAN IV or FORTRAN IV PLUS.

A maximum of eight CM 7405 terminals can be connected to SM 4-20 or SM 52/11 type minicomputers.

Figure 32. Operator's terminal and processor (second part of the CM 7405 graphic terminal)

Technical specifications:

Image format	235/235 mm
Imaging mode	vector, point, symbol
Type of imaging	vector with info restoration
Type of imaged vectors	given by program
Flicker and scan synchronization	given by program
Duration of symbol depiction	max. 26 μs
Duration of vector depiction	max. 204.6 μs
Time for random shift of beam	max. 20 μs
Max. inaccuracy of drawing	1 raster unit
Max. inaccuracy in connecting 2 vectors	max. 1.5 mm (whole display)
Geometric drawing	max. 2 percent
Raster	1024x1024 points
Imaging point diameter	0.5 mm
Number of brightness levels	8
Number of various imaging symbols	127
Symbol dimensions	6x8 points (3x4 mm)
Set of symbols	KOI 7 and 31 special symbols
Number of lines (selectable)	39 (42)

Number of symbols per line (selectable)	73 (85)
Type of script	italics (incline 75°)
Symbol generator	RPROM memory
Control symbols	CR, LF, BS, SI, SO
Weight	250 kg
Feed voltage	220 V/50 Hz
Monitor power input	max. 400 VA

GVM 01 Graphic Vector Monitor

The GVM 01 graphic vector monitor with a light pen is an independent interactive graphic input/output device (used, e.g., in the CM 7405 graphic terminal). However, this monitor can be used as an independent interactive imaging module as a vector imaging unit connected to a SMEP minicomputer, e.g., SM 4-20 (see Figure 33).

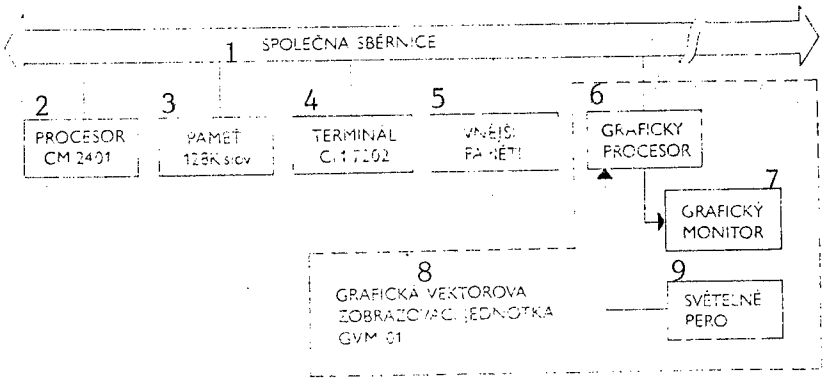


Figure 33. Graphic vector imaging unit connected to SM 4-20 minicomputer

Key:
1. common busbar
2. CM 2401 processor
3. 128K-word memory
4. CM 7202 terminal
5. external memories
6. graphic processor
7. graphic monitor
8. GVM 01 graphic vector imaging unit
9. light pen

In this case the graphic imaging unit uses the systemic sources of the computer (external magnetic memories, operator's terminal, etc.).

The graphic vector monitor is structurally and electrically an independent desk-type unit. Technical specifications for the monitor are listed sub the CM 7405 terminal.

The graphic vector monitor forms a part of the ISAP 1 interactive graphic system. The GVM 01 can be supplemented by an operator's panel-tablet, an auxiliary interactive device making it possible to select by pushbutton one of eight functions, e.g., in the selection of the "menu" in cooperation with

the display. It can be connected to a computer by means of a modified PAD 8-CM 6001 adapter.

Digigraf 1712 Drawing System

The Digigraf 1712 is a programmable system (Figure 34) serving for drawing plans, line drawings, graphs, substrates produced by engraving, piercing, cutting and exposure to light of the corresponding media, i.e., cartographic paper, drafting paper, tracing paper, engraving foil, scaling foil, metallized paper and photosensitive paper.

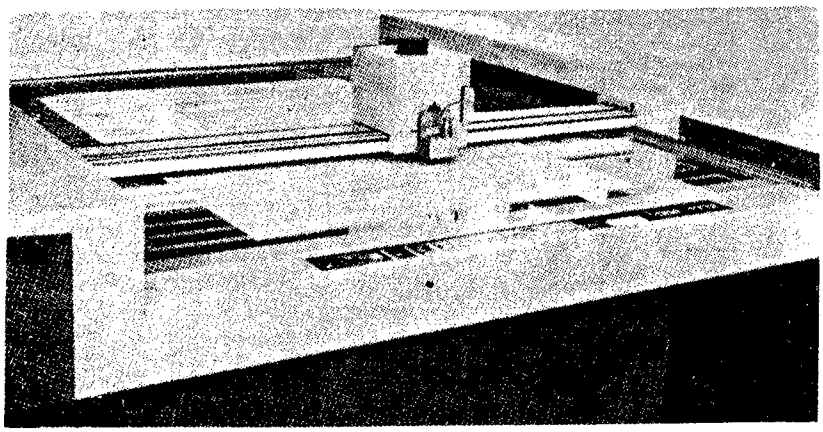


Figure 34. Digigraf 1712 drafting system

These operations are carried out by means of the so-called technological heads with imaging specifications (speed, acceleration) selectable by program.

Electrostatic holding is used for the media on which drawing or other operations are performed.

The Digigraf 1712 comes equipped in its basic variant with a combined double stylus drawing head with ballpoint or tubular pens.

The system is controlled by a microprocessor and all electronic equipment is built into the pedestal. The table is equipped with dynamic servomotors for motion in perpendicular X and Y axes. The operator's panel for controlling the table is located at the edge of the horizontal drawing area.

Technical specifications:

Size of drawing area	1672x1180 mm
Basic step size	0.01 mm
Max. speed	350 mm/s
Acceleration	selectable 0.05 to 5 m/s^2
Dimensions	2300x2210x1200 mm
Weight	700 kg
Power feed/power input	220 V/1300 VA

The Digigraf drafting system forms a part of the ISAP 1 interactive graphic system.

Digigraf 1208 Drawing System

The Digigraf 1208 is a programmable drafting system with properties analogous to those of the Digigraf 1712, except that the 1208 type is structurally smaller and has a smaller drawing area.

The system is connected to the common busbar of SMEP minicomputers by means of the PAD 16 parallel adapter.

Technical specifications:

Size of drawing area	1189x841 mm
Basic step size	0.01 mm
Max. speed	400 mm/s
Acceleration	selectable 0.05 to 5 m/s^2
Dimensions (wxdxh)	1700x1800x 1200 mm
Weight	550 kg
Power feed/power input	220 V/1300 VA

Digitizer 1208 Read-off System

The Digitizer 1208 semiautomatic coordinates reader is used for reading the coordinates of points from a flat substrate, primarily maps, plans, drawings, etc. In on-line operation it is connected to SMEP computers with a common busbar by means of the PAD 16 parallel adapter. In off-line operation it can work with a tape memory or with a perforated tape puncher.

BAK 5T Coordinate Plotter

The BAK 5T operates on the analog principle and is connected to SMEP minicomputers via, e.g., the DIGIBAK 512 digitalization system.

This complex is connected to the common busbar by means of the PAD 16-SM 0708 parallel adapter.

The BAK 5T planar coordinate plotter (Figure 35) is an output device serving for the automated plotting of functions y = f(x) in a rectangular coordinate system. The plotter provides for electrostatic paper holding, plotting by a ballpoint or tubular pen, selection from eight types of plotting lines, various types of imaging of graphs, diagrams, progressions, etc., into a random format of maximum size A3.

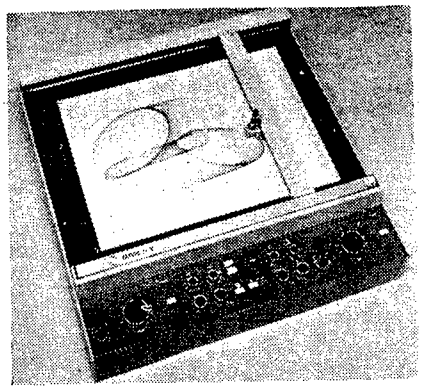


Figure 35. BAK 5T coordinate plotter

Technical specifications:

Size of drawing area	380x280 mm
Static accuracy	±0.2 percent
Plotting hysteresis	<0.3 mm
Max. speed	800 mm/s
Dimensions (w x h x d)	530x165x530 mm
Weight	22 kg
Power feed/power input	220 V/100 VA

CM 6303/Graphic Output Dot Printer

Modification of the CM 6303 (CONSUL 2111) dot printer with JSEP interface produced a system which provides a two-color output (black and red). The system is suited, e.g., for the ISAP 1 interactive graphic system and provides:

--drawing of logic diagrams,
--drawing of stencils for deposition of printed circuits on plates,
--plotting of metallic joints and printed circuits, etc.

A sample of graphic output from this printer is shown in Figure 36.

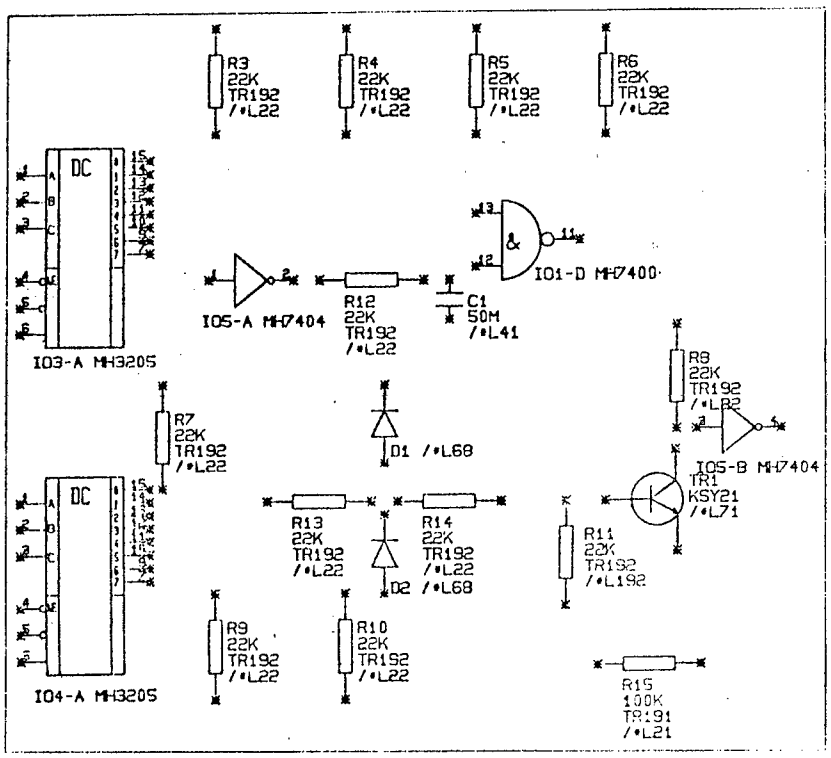


Figure 36. Sample of output from the CM 6303 printer with graphic output

The printer can be used for drawings up to a maximum width of 340 mm. The time required for making an A 3 format drawing (420x297 mm) is approximately 3.5 min.

The properties of the printer in printing routine alphanumeric symbols remain unchanged and correspond to the data specified for the terminal with CM 7108 print.

2.1.7 Terminals, Data Transmission Systems and Connecting Units

The subsequent text describes terminals and other hardware that can serve for communication of users with 16-bit SMEP systems with a common busbar.

The following hardware is involved:

--CM 7202 alphanumeric display terminal,
--CM 1601 simple alphanumeric display terminal,
--a semigraphic display terminal,
--CM 7405 graphic terminal (description appears in the chapter "Graphic Systems"),
--terminal with CM 7108 print,
--ASAD CM 6002 asynchronous adapter,
--QASAD CM 8512 quadruple asynchronous adapter,
--AMU CM 8511 synchronous multiplex,
--SAD CM 8506 all-purpose synchronous adapter,
--SAD B SM 1207 synchronous adapter,
--SAD D SM 1208 synchronous adapter,
--CM 8105 zero modem,
--MDS 200 modem,
--MDS 1200 modem,
--KOMPRO communication processor,
--PAD 8 CM 6001 parallel adapter,
--PAD 12 SM 0706 parallel adapter,
--PAD 16 SM 0708 parallel adapter.

All the developed systems have been found compatible by the Czechoslovak Communications Administration and can be connected into the Czechoslovak telecommunications network.

In the passage on "Planning" appears a comment on planning long-distance data processing systems using the Czechoslovak telecommunications network.

CM 7202 Display Terminal

This alphanumeric display terminal facilitates communication between user and system. The CM 7202 terminal is a compact device with keyboard for data input and a monitor as its output system (see Figure 37).

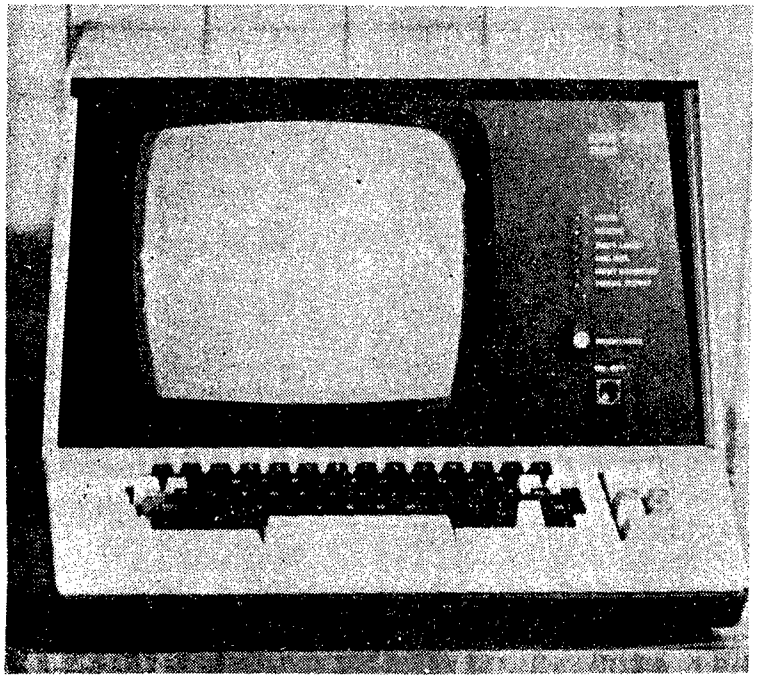


Figure 37. CM 7202 display terminal

There are two CM 7202 variants depending on the type of interface:

--CM 7202 IRPR with IRPR parallel interface, permitting local connection of the terminal to the system up to a distance of 15 m, designated as CM 7202/P;

--CM 7202 IRPS with a serial interface permitting connection via the IRPS voltage loop up to a distance of 500 m or via interface V.24 CCITT and a modem with no distance limitation, designated as CM 7202/S.

Transmission takes place in 7-bit transmission code KOI 7 (ASCII).

The terminal facilitates operation in several modes:

--local mode (Figure 38) is used for the preparation and editing of data on the display (in memory), whereby no communication with the computer occurs;

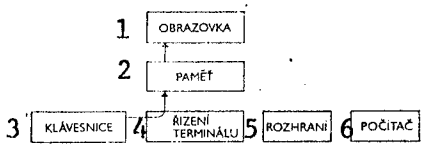


Figure 38. Local mode of operation

Key:
1. display
2. memory
3. keyboard
4. terminal control
5. interface
6. computer

--long-distance symbol mode, whereby data are transmitted from the keyboard into the computer by individual symbols and after receiving are sent back into the terminal's memory and are displayed on the display tube; this involves duplex operation on line with the computer (Figure 39);

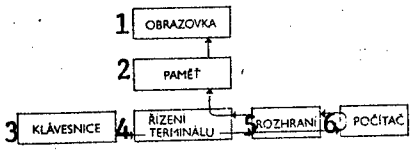


Figure 39. Long-distance duplex symbol mode of operation

Key:
1. display
2. memory
3. keyboard
4. terminal control
5. interface
6. computer

--long-distance block mode (Figure 40), in which a block of data from the display, prepared, e.g., in the local mode, is transferred into the computer as one unit (maximum 1920 symbols);

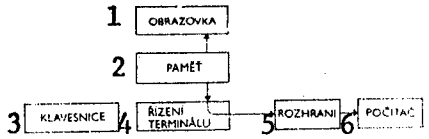


Figure 40. Long-distance block mode

Key:
1. display
2. memory
3. keyboard
4. terminal control
5. interface
6. computer

--print mode (Figure 41), in which data from the display are printed out on the connected printer for hard copy; it is possible to print out information prepared either in local (from keyboard) or long-distance mode (from computer), but during printout operation is not possible in some other mode, i.e., communication between operator and computer is interrupted.

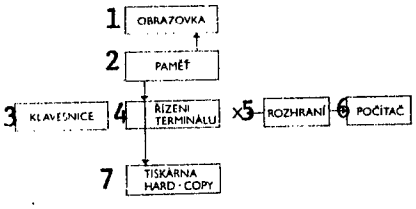


Figure 41. Print mode

Key:
1. display
2. memory
3. keyboard
4. terminal control
5. interface
6. computer
7. printer (hard-copy)

Note: Communication between terminal and computer is interrupted in this mode.

This keyboard permits the entry of alphanumeric and digital information and performance of various operations in both local and long-distance mode. The terminal currently does not have a physically separated numerical keyboard; in case of need (e.g., in data acquisition systems), this keyboard is integrated in the field of an alphanumeric keyboard and its program operation is similar to that of comparable foreign products. Production of a separate numerical keyboard is in preparation for 1983.

Technical specifications:

Maximum number of imaged symbols	1920
Imaging format	24 lines w/80 symbols each
Set of imageable symbols	96
Symbol imaging	5x7 dot matrix
Number of keys	67
CM 7202/S terminal transmission speed	100 - 9600 bit/s
CM 7202/S transmission speed in the function of a computer's operator's terminal	max. 2400 bit/s
CM 7202/P terminal transmission speed	150 kB/s
Feed voltage	220 V/50 Hz
Max. power input	160 VA
Dimensions	800x480x350 mm
Weight	30 kg

Note:

Innovated variants of the CM 7202 terminal under development bear the following designations:

--CM 7202.M1-A--alphanumeric version,
--CM 7202.M1-G--semigraphic version,
--CM 7202.M1-T--text processing version

Thus, the CM 7202 terminal described herein will be replaced in the future by the CM 7202.M1-A terminal.

CM 1601 Display Terminal

The CM 1601 display terminal is a simplified alphanumeric terminal derived from the CM 7202 type. The simplification consists in reduced capacity of internal memory and, consequently, the number of displayable symbols is also lower. The entire logic part of terminal control is contained on a single plate with printed circuits. The set of control symbols is also limited in comparison to the CM 7202.

The terminal uses a serial interface IRPS voltage loop or CCITT V.24 and can operate in local mode and in long-distance symbol mode (see Figures 38 and 39).

The CM 1601 terminal's technical specifications are similar to those of the CM 7202 terminal and, as such, it is suitable for application as an expanding input/output system for minicomputers or microcomputers using either IRPS-voltage loop or V.24 CCITT interface. The CM 1601 does not permit the connection of a hard-copy printer.

Technical specifications (differing from CM 7202):

Number of lines (selectable)	16 (12)
Number of symbols per line (selectable)	64 (40)
Set of displayable symbols	64
Capacity of image memory	1K byte
Power input	160 VA

Semigraphic Terminal

The semigraphic terminal is a display terminal offering the imaging of graphs, its design being based on the CM 7202 terminal.

Its possibilities in the area of processing alphanumeric information approximate those of the CM 7202 terminal. However, the semigraphic terminal offers the additional possibility of displaying in a raster of 512 horizontal and 236 vertical points two independent, separately controlled graphs as well as various other graphic symbols, e.g., arrows, indices, signs of mathematical operations. This considerably expands the possibilities for application of this terminal, e.g., for monitoring of histograms, progress of periodic processes, monitoring, simulation, drawing of various layouts, tables and diagrams.

The terminal makes it possible to display any random combination of graphics and text. Individual instructions for controlling the system's operation are given from the keyboard, either by individual keys or by their combinations.

The semigraphic terminal is connected via a serial interface voltage loop IRPS or V.24 CCITT with a transmission speed of 100-9600 bit/s in full duplex.

Technical specifications:

Interface	IRPS, V.24 CCITT
Transmission speed in full duplex	100, 200, 300, 600, 1200, 2400, 4800 or 9800 bit/s
Display:	
Size	205x130 mm
Display of alphanumeric information:	
Number of lines	24
Number of symbols per line	80
Set of symbols	96 symbols KOI 7 31 control and graphic symbols
Special functions	shift by one line down shift by one line up ring, erasure, tabulator, courser control

Format of symbol display	7x7 dot matrix
Display of graphic information:	
Resolving power	512 horizontal + 236 vertical points
Graphs or histograms	two functions variable x each individually controlled
Network of coordinates	512 vertical and 236 horizontal lines, each individually controlled
Other properties	individual blanking and light up of all graphic functions, graph erasure
Special functions:	
Hold screen mode	permits interruption of data transmission and holding information on the screen for further study
Terminal identification	in receiving control symbol ESC Z the terminal responds ESC E
Mechanical and electrical data:	
Dimensions	800x480x350 mm
Weight	28 kg
Power supply	220 V/50 Hz

Note:

The described semigraphic terminal will take the form of the CM 7202.M1-G display terminal (see note following the description of the CM 7202 display terminal).

CM 7108 Terminal with Printer

The CM 7108 terminal, consisting of the CONSUL C 2113 dot printer and the CONSUL C 259.11 keyboard, is designed for local or long-distance connection to a computer by parallel or serial interface (Figure 42).

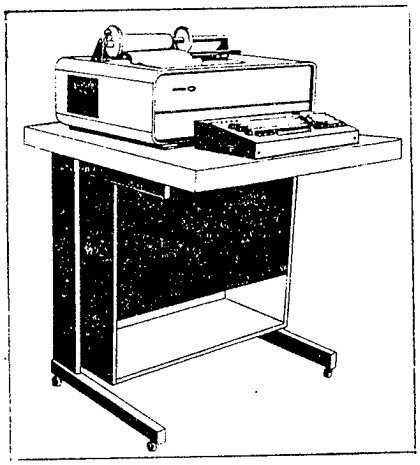


Figure 42. CM 7108.70 terminal (VUVT)

Variants of the terminal:

--CM 7108.43 parallel interface IRPR,
--CM 7108.61 serial interface V.24 CCITT,
--CM 7108.63 serial interface-voltage loop.

This terminal can be used in lieu of the basic operator's terminal, e.g., when there is a need for keeping a log of the system's operation, or it can be used as an expansion terminal (in the serial variant) up to a distance of 500 m from the computer.

Structurally, the terminal consists of a desk with electronic equipment, a printing mechanism and an alphanumeric keyboard.

Technical specifications:

Transmission speed	selectable 100, 200, 300 Bd
Type of transmission	parallel serial asynchronous
Mode of operation	duplex
Protection against errors	even parity odd parity without parity control
Set of symbols	96
Number of symbols per line	132
Data format	7 or 8 information bits parity bit 1 or 2 stop bits
Printing speed	max. 20 symbols/s
Paper format	roll, folded paper
Power feed from network	220 V + 10 percent - 15 percent
Max. power input	620 VA
Weight	max. 90 kg
Dimensions	800x800x750

CM 6002 Asynchronous Adapter

The CM 6002 is a single-line asynchronous adapter which facilitates the connection of a device in half or full duplex. This device can be a series asynchronous terminal or some other SMEP computer with a CM 6002 adapter.

This asynchronous adapter offers the choice of one of two interfaces:

--interface IRPS-voltage loop 20 mA (40 mA),
--V.24 CCITT interface.

This asynchronous adapter is very flexible and makes it possible to select many functions through couplings; speed can be selected from 100 to 9600 bit/s; the type of parity protection is also selectable--even parity, odd parity or without parity; length of the stop bit of the transmitted symbol can be 1, 1.5 or 2 bits.

The ASAD-CM 6002 is structurally designed on one 2/3 plate with the designation SM 1201 (see Figure 43). IRPS interface allows for the connection of peripheral equipment up to 500 m by means of a spiral quad wire as shown in Figure 44a, with the proviso that the d-c resistance of no loop may exceed 100Ω. Local connection via IRPS interface can be seen in Figure 44b.

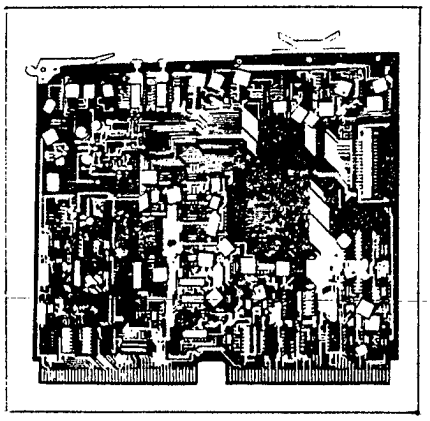


Figure 43. ASAD-CM 6002 asynchronous adapter

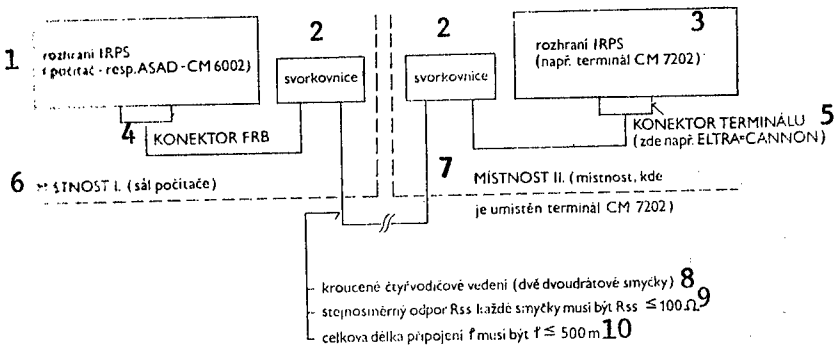


Figure 44a. Potential long-distance connection of CM 6002 via IRPS interface

Key:
1. IRPS interface (computer or ASAD CM 6002)
2. terminal block
3. IRPS interface (e.g., CM 7202 terminal)
4. FRB connector
5. terminal connector (here, e.g., ELTRA=CANNON)
6. room 1 (computer location)
7. room 2 (location of CM 7202 terminal
8. twisted four-conductor line (two 2-wire loops)
9. D-c resistance R_{ss} of each loop must be $R_{ss} \leqq 100\Omega$
10. total length of connection f must be $f \leqq 500$ m

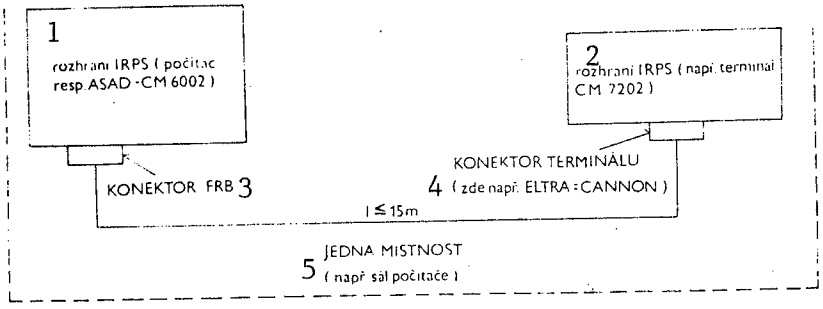


Figure 44b. Potential local connection of CM 6002 via IRPS interface

Key:
1. IRPS interface (computer or ASAD CM 6002)
2. IRPS interface (e.g., CM 7202 terminal)
3. FRB connector
4. terminal connector (here, e.g., ELTRA=CANNON)
5. one room (e.g., computer room)

Whenever more systems with serial interface are to be connected, it is better to use the CM 8511/IRPS asynchronous multiplex.

Technical specifications:

Type of transmission	asynchronous start/stop
Number of information bits	5, 6, 7 or 8
Length of stop element	1, 1.5, 2 bits
Transmission protection	even parity odd parity without parity
Max. transmission speed	9600 bits
Mode of operation	half duplex full duplex
Interface	IRPS-20 mA (40 mA), V.24 CCITT
Number of loads on common busbar	1

QASAD CM 8512 Quadruple Asynchronous Adapter

The CM 8512 provides for connection of four serial asynchronous devices with the IRPS or V.24 CCITT interface on a common busbar.

The CM 8512 offers for each of four lines functions similar to those of the ASAD-CM 6002 asynchronous adapter. The difference consists in the fact that these functions are selectable in the case of the ASAD asynchronous adapter by couplings, and in case of the QASAD quadruple adapter they can be selected by the program. However, the number of IRPS or V.24 outputs must be specified at the time the system is ordered.

The CM 8512 is structurally formed by one 2/3 plate and a distribution panel to which are connected individual IRPS lines via a terminal block and V.24 via a connector.

Technical specifications:

Number of independent channels	4
Type of transmission	asynchronous start-stop
Number of information bits	5, 6, 7 or 8
Length of stop element	1 or 2 bits
Transmission protection	even parity odd parity without parity
Transmission speed	50-19,200 bit/s selectable for each channel
Mode of operation	full duplex
Interface	IRPS-voltage loop 20 mA V.24 CCITT
Number of loads on common busbar	

AMU CM 8511 Asynchronous Multiplex

The CM 8511 is a program-controlled asynchronous multiplex which makes it possible to connect up to 8 or even up to 16 asynchronous series lines to a common busbar.

The key significance of its application is constituted by two facts:

--in view of the principle on which the CM 8511 multiplex operates (control of terminals, buffer memory, etc.), its use offers a more efficient operation of the computer than is the case in connecting the same number of terminals via individual single-line ASAD asynchronous adapters;

--with the use of a larger number of terminals the use of a single multiplex appears more economically preferable and reliable than use of independent asynchronous adapters.

The CM 8511 makes it possible to use two types of serial asynchronous interface, i.e., IRPS-voltage loop and V.24 CCITT in the following combinations:

--AMU A 8 channels with V.24 CCITT interface,
--AMU B expansion of AMU A to 16 channels V.24 CCITT,
--AMU C with IRPS interface,
--AMU D expansion of AMU C to 16 channels IRPS,
--AMU E 16 channels with V.24 CCITT interface,
--AMU F 16 channels with IRPS interface,
--AMU G 16 channels: 8 channels V.24 CCITT and 8 channels IRPS.

The multiplex is modular with eight line modules. Its structural makeup is as follows:

A part of the multiplex is always:

--a special systemic unit for four plate positions into which can be inserted plates constituting a random variant of the multiplex A-G which is placed into the basic or an expansion grid;

--a distribution panel allowing for connection of eight lines V.24 by ELTRA connectors or eight IRPS lines via terminal block; it is placed into the rear part of the computer casing.

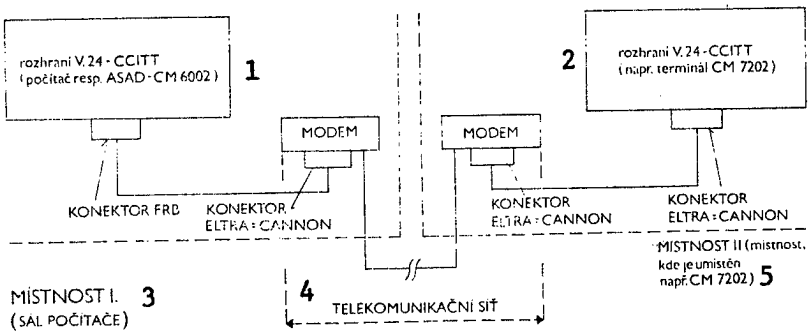


Figure 45. Potential long-distance connection of CM 6002 via V.24 CCITT interface

Key:
1. V.24 CCITT interface (computer or ASAD CM 6002)
2. V.24 CCITT interface (e.g., CM 7202 terminal)
3. room 1 (computer location
4. telecommunication network
5. room 2 (location of, e.g., CM 7202)

Depending on the type of multiplex (for 8 or 16 lines, for IRPS or V.24 interface) it is equipped with the corresponding plates and accessories.

More than one multiplex can be connected to a computer, theoretically up to 128 lines.

Figures 46 and 47 show an example of multiplex application.

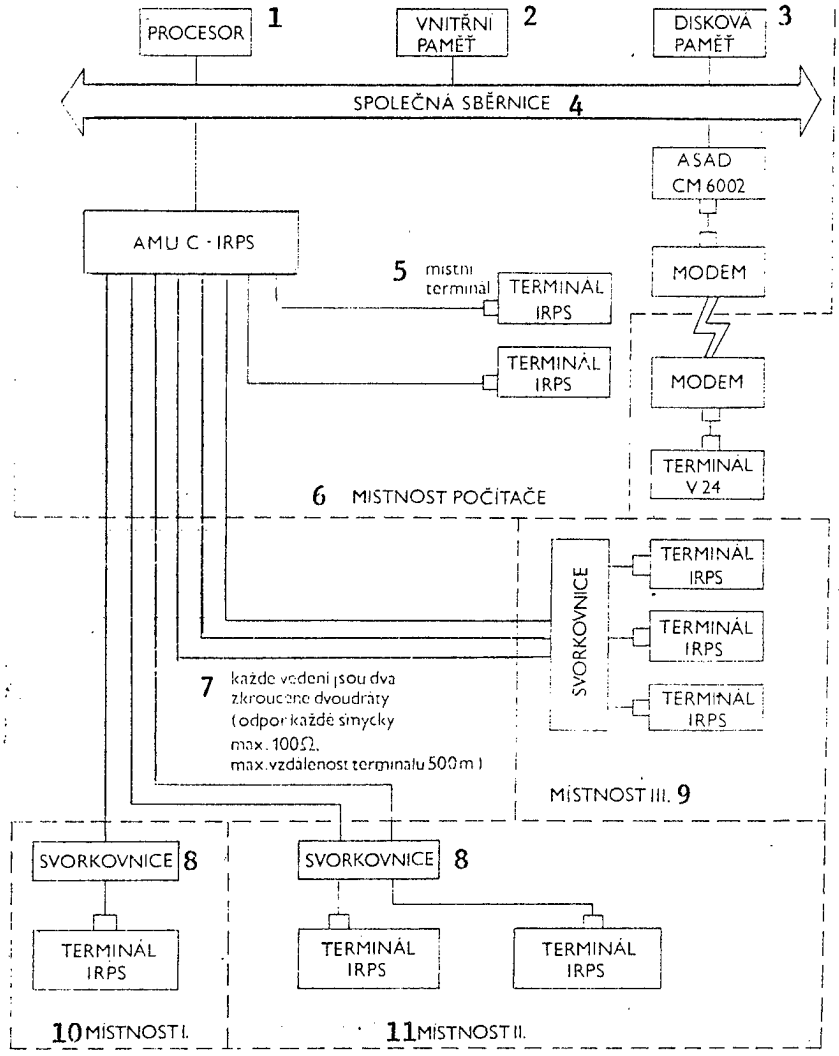


Figure 46. Example of multiplex application with IRPS interface

Key:

1. processor
2. internal memory
3. disk memory
4. common busbar
5. local terminal
6. computer location
7. each line is a pair of twisted twin wires (resistance of each loop is max. 100 Ω, max. distance of terminal is 500 m)
8. terminal block
9. room 3
10. room 1
11. room 2

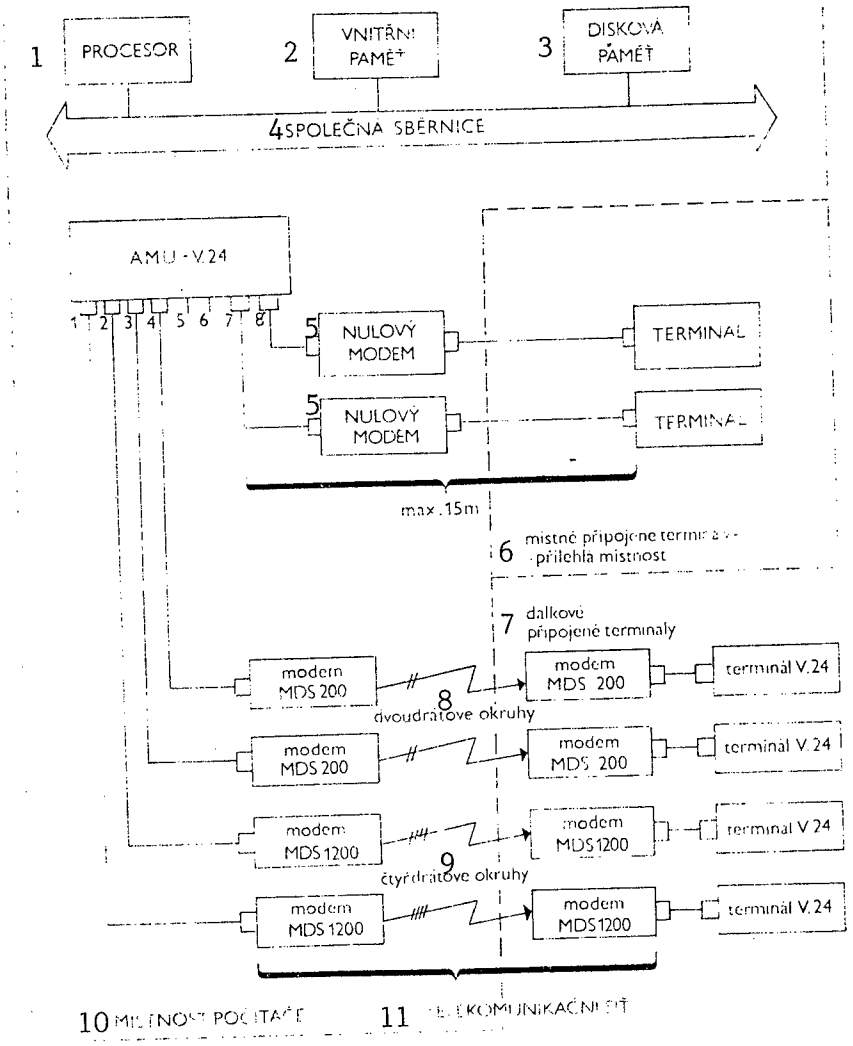


Figure 47. Example of multiplex application with V.24 CCITT interface

Key:

1. processor
2. internal memory
3. disk memory
4. common busbar
5. zero modem
6. locally connected terminals in adjacent room
7. long-distance connection terminals
8. twin-wire circuits
9. four-wire circuits
10. computer location
11. telecommunication network

If a user requires a multiplex with V.24 interface for long-distance connection of terminals via modems and, further, needs to connect a terminal locally up to 15 m, then it is possible--in case of free capacity of the multiplex with V.24 interface--to use the CM 8105 zero modem described in the next part (see Figure 47).

Technical specifications:

Number of channels	8 or 16
Transmission speed	50-9600 bit/s selected by program separately for each channel
Transmission mode	full duplex

Date format:

Starting element	1 bit
Information field	5, 6, 7 or 8 bits
Parity bit	1 bit or without parity
Stop element	1 or 2 bits (program selected)
Parity control	even, odd or no parity (program selected)

Number of loads on common busbar:

AMU A, B, C, D	1
AMU E, F, G	2

SAD CM 8506 All-purpose Synchronous Adapter

The CM 8506 synchronous adapter is a single-line adapter with selectable properties for serial synchronous transmission using procedures SDLC, HDLC, DDCMP and--with supplementary software--also procedure BSC.

It provides for reliable transmission between two SMEP computers, and also--by means of the EC 7920 emulator under the DOS RV V2 operating system (see chapter on "Software")--connection between SMEP-JSEP computers on the basis of the BSC program procedure.

The CM 8506 comprises circuits necessary for cooperation with a synchronous modem. Connection to a synchronous adapter can be currently accomplished by a corresponding variant of the Czechoslovak MDS 1200 modem. The adapter's interface meets CCITT recommendations. The SAD-CM 8506 is structurally designed on a single 3/3 plate (Figure 48), which is inserted into the systemic unit located in the basic or expansion grid. In view of its design, the SAD can be used in all 16-bit systems with a common busbar, except the SM 50/50.

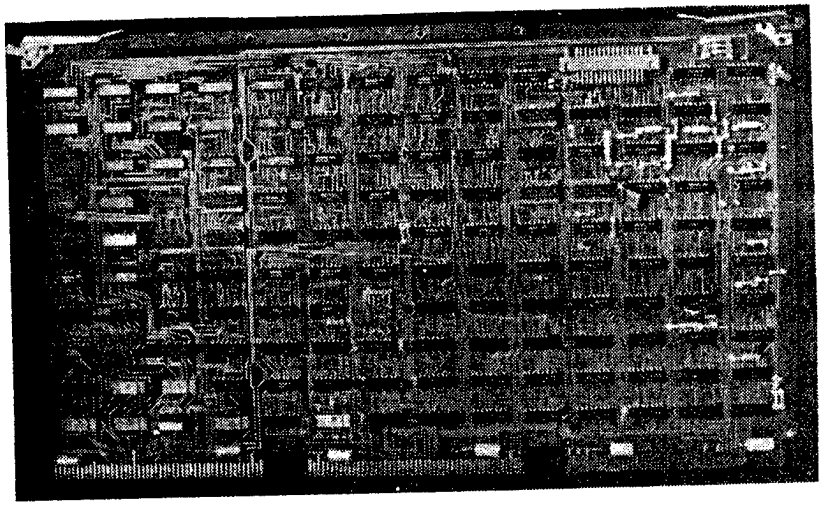


Figure 48. SAD - CM 8506 synchronous adapter

Technical specifications:

Number of independent channels	1
Type of transmission	series synchronous
S2 interface on modem side	acc. to V.24 and V.28 CCITT recommendations
Max. speed of data transmission	9600 bit/s
Operating mode	full duplex half duplex
Number of information bits	8

Safegaurds against transmission errors:

Procedure DDCMP, BSC	CRC 16 cyclic code
procedure HDLC, SDLC	CRC CCITT cylic code
Number of loads on common busbar	1

SAD B Synchronous Adapter with Procedure BSC-SM 1207

The SAD B synchronous adapter is a single-line series synchronous adapter for connecting a SMEP computer to a hierarchically higher JSEP computer (which uses the BSC procedure) and operating under its control.

In that case the SMEP computer operates under the DOS RV V2 operating system, under which also runs the EC 7920 emulation program that permits operation in dialogue mode, or EC 8514 permitting batch mode operation with a JSEP computer. (Closer details in chapter on "Software.")

The SAD B was developed on one 2/3 plate, which makes it possible to build it into all 16-bit SMEP systems with a common busbar.

Technical specifications:

Number of independent channels	1
Type of transmission	series synchronous
Number of information bits	7 or 8
Transmission procedure	BSC
Transmission mode	half duplex

Transmission safeguards:

--with use of ASCII alphabet	VRC/LRC 8 parity
--with use of EBCDIC alphabet	CRC 16 cyclic code
Number of loads on common busbar	1

SAD D Synchronous Adapter with Procedure DDCMP-SM 1208

The SAD D is a single-line series synchronous adapter facilitating mutual interconnection of SMEP minicomputers in a computer network in accordance with the SMEP network layer architecture when the physical contact layer uses the DDCMP communication procedure (see chapter on "Software").

The SAD D was developed on one 2/3 plate, which makes it possible to be built into any 16-bit SMEP system with a common busbar.

Technical specifications:

Number of independent channels	1
Type of transmission	series synchronous
Number of information bits	8
Alphabet used	ASCII
Transmission safeguard	CRC 15 cyclic code
Operating mode	duplex haf-duplex
Max. transmission speed	9600 bit/s
Number of loads on common busbar	1

CM 8105 Zero Modem

The zero modem is a supplementary device which makes it possible to connect a terminal without a standard modem to the series asynchronous V.24 CCITT interface up to a distance of 15 meters.

Use of the zero modem makes sense in cases when there is a free capacity in an asynchronous multiplex with the V.24 interface and there is a need for connecting another terminal at short range. Then, instead of using a new multiplex or a series adapter with IRPS interface, it is possible to use the zero modem (see Figure 47).

The zero modem is structurally formed by a small box with two connectors, and for connection to a terminal and to a computer requires two cables with the requisite connectors at both ends.

In a general office setting, in administrative buildings, etc., the device can be connected over distances considerably longer than 15 m (up to hundreds of meters); however, the user must verify these possibilities himself with a view to the intensity of interference at the point of installation. The distance of 15 meters specified by the supplier is based on the most adverse interference conditions.

Technical specifications:

Number of independent channels	1
Interface used	V.24 CCITT
Operating mode	half-duplex full fuplex
Max. transmission speed	48K bit/s

MDS 200 Modem

The MDS is a device which facilitates the transmission of data along telephone lines by low-level frequency modulated signal. It is designed for the asynchronous transmission of data. On a twin-wire line it makes it possible to transmit information simultaneously in both directions (full duplex) independently, because transmitter and receiver operate on frequency divided and equivalent channels.

The connection to a public commutated network is accomplished by means of a telephone set connected to a modem, which can also be used as a regular telephone set when no data is being transmitted.

The modem can also be used on noncommutated (fixed) telephone connections. Here, too, a service connection can be made by an MB telephone set fed from the modem.

The modem is intended for the connection of terminals with printers. However, since it needs only a twin-wire line and offers full duplex operation, it is often also used for connecting the CM 7202 display terminals.

Technical specifications:

Max. transmission speed	200 bit/s
Type of modulation	dual frequency

Marketing of MDS 200 modems is provided exclusively by the communications administration.

MDS 1200 Modem

The MDS 1200 is a signal converter designed for interconnecting remote terminals and computers with V.24 CCITT interface at a speed of 600 or 1200 bit/s via telephone line.

In its basic configuration the MDS 1200 permits half-duplex asynchronous operation on a twin-wire commutated or leased line.

Supplemented with a four-wire unit, its area of application is expanded to four-wire leased lines in full duplex mode with simultaneous contact by telephone. Such a four-wire line is called for in, e.g., duplex operation of the CM 7202 display terminal. Thus, the advantage offered by higher operational speed (in comparison with the MDS 200) is negated by the requirement for two 4-wire lines (i.e., double that needed for transmission by the MDS 200).

With the use of a synchronization unit the MDS 1200 modem permits operation in synchronous mode.

Technical specifications:

Modulation rate of main channel	1200 Bd or 600 Bd selectable
Modulation rate of reverse channel	75 bd
Type of modulation	frequency

Marketing of MDS 1200 modems is provided exclusively by the communications administration.

KOMPRO Communication Processor

The currently developed KOMPRO is an auxiliary communication processor which is connected to a common busbar and controls the operation of synchronous or asynchronous communication modules, i.e., ASAD, QASAD, SAD adapters and multiplexes. It operates in parallel with the operation of the computer's main processor and takes over several communication functions for it.

KOMPRO has its own RAM type control memory in which are stored control programs that can be fed from the main processor.

Technical specifications:

Length of microinstruction	16 bits
Capacity of registering memory	16 bytes
Capacity of RAM control memory	1K words
Size of data word	8 bits
Capacity of data memory	1K words
Size of state registers	8 bytes
Size of data registers	16 bits
Number of data registers	2
Size of NPR address	18 bits
NPR data transmission	1 byte 1 word or multiple
CSR transmission	1 word or multiple
Interval of programmable timer	50 µs
Cooperation with memory	DMA two-way
Number of controlled asynchronous lines	max. 48
Number of controlled synchronous lines	max. 16
Number of loads on common busbar	1
Number of KOMPRO in one SMEP system	max. 16

PAD 8 CM 6001 Parallel Adapter

This is an all-purpose interconnecting unit for the connection of input and output systems with IRPR interface to a common busbar (one input and one output channel). It find application with, e.g., perforated tape readers/punchers, dot and line printers with parallel interface. It is structurally designed on a 2/3 plate SM 0701, is placed into the grid and is connected with the requisite device by cables not exceeding 15 m in length.

Technical specifications:

Number of loads on common busbar	1
Number of bits transmitted in parallel	8
Number of programmable registers	4
Max. transmission speed	300K byte/s
Power feed/consumption	+5 V/1.5 A
Weight	0.5 kg

PAD 12 SM 0706 Parallel Adapter

This interconnecting unit is used as a control unit for connection of the EC 6112 card reader (see description thereunder).

Technical specifications:

Number of loads on common busbar	1
Number of bits transmitted in parallel	12
Number of programmable registers	2
Power feed/consumption	+5 V/1.8 A
Weight	0.7 kg

PAD 16 SM 0708 Parallel Adapter

This is an all-purpose interconnecting unit for the connection of mainly graphic systems with IRPR interface, e.g., DIGIBAK 5T, DIGIGRAF, DIGITIZER. Its structural design is again the same, i.e., on a 2/3 plate placed into the grid and connected with the requisite device by cables not exceeding 15 m in length.

The PAD 16 parallel adapter has one input and one output channel.

Technical specifications:

Number of loads on common busbar	1
Number of bits transmitted in parallel	16
Number of programmable registers	3
Power feed/consumption	+5 V/2 A
Weight	0.5 kg

2.1.8 Units for Interfacing With the Environment

Another area envisioned for application of 16-bit minicomputers is the automation of processes, production, scientific experiments and laboratory operations.

Application in these areas will be found by hardware for interfacing with the environment. This includes:

--CM 9205--LJSP laboratory unit for interfacing with the environment,
--CM 0102--IMS 2 connecting unit,
--CM 9004--connecting unit for DASIO 600,
--control unit (under preparation) for the CAMAC frame.

CM 9205 LJSP Laboratory Unit for Interfacing With the Environment

The LJSP is a compact analog subsystem for operation in real time. It is suitable for the automation of laboratory operations, scientific and technical experiments.

The system contains a 12-bit analog digital converter, a sampling amplifier, a 16-channel analog multiplex, two 12-bit digital analog converters, a crystal-controlled clock and control of the imaging system for the sampling circuit.

The analog digital converter samples data at a given frequency and provides for their retention in digital form for further processing. The multiplex can be expanded by an external multiplex. The sampling amplifier provides for accurate conversion even at rapidly changing signals by keeping the input voltage constant until the conversion is completed. The digital analog converter can be made to operate at random as 12-bit or 10-bit in bipolar or unipolar mode. Circuits for control of the imaging system make it possible to display data in a field format containing a maximum of 4096x4096 points. The mentioned converter can be used also for controlling an X-Y plotter (e.g., BAK 5T).

The programmable clock offers the possibility of selecting several precision measuring methods and counting of time intervals.

The real time clock operates on the priority level BR 6 and the block of analog outputs on level BR 4. Program operation is provided by means of eight registers. The LJSP unit uses three interrupting vectors.

Structurally the LJSP unit is placed into a systemic unit in the basic or expansion grid and is formed by two 2/3 plates, complementary wafers, cables and a distribution panel to which conductors from the medium are attached by screws (see Figure 49).

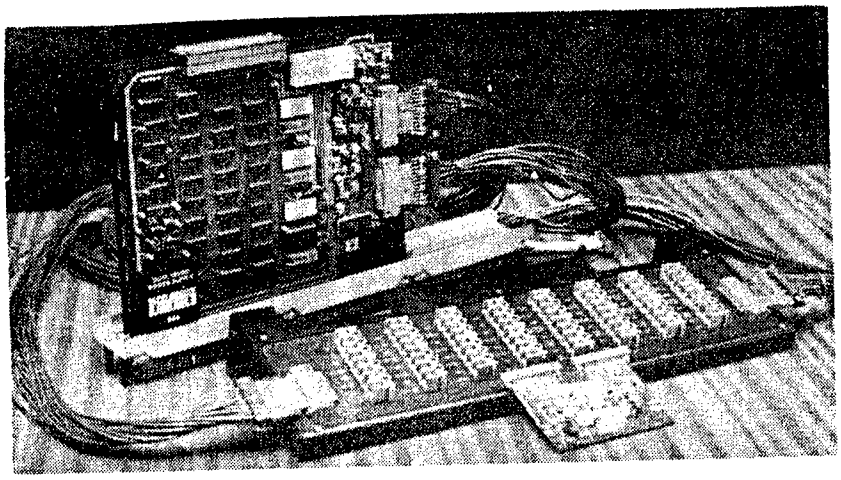


Figure 49. CM 9205 laboratory unit for contact with media

Technical specifications:

Analog digital converter: (selectable by coupler)	
Input voltage range	0 - 5 V 0 to 10 V ± 2.5 V ± 5 V
Resolution power	10 or 12 bits (selectable)
Accuracy at 20°C	max. ± 0.1 percent for 10 bits max. ± 0.05 percent for 12 bits
Linearity	½ LSB
Conversion time	22-23 µs
Number of input channels	16
Stabilization time (sampling multiplex)	8 µs (at 5 V cycle) with precision < ½ LSB
Digital analog converter:	
Number of converters	2
Voltage range	- 5 V to ± 5 V - 0.5 V to ± 0.5 V
Resolution power	10 or 12 bits selectable
Accuracy at 20°C	± 0.1 perc. in 10 V range for 10 bits ± 0.04 perc. in 10 V r. for 12 bits ± 2 percent at 1 V range
Input impedance	50 Ω
Loading capacity	1 M /100 pF

Programmable clock:

Frequencies	
--from crystal generator	1000; 100; 10; 1; 0.1 kHz
--from external logic input	
--from additive frequency input	
Operating mode	individual repetitive
Range of counters	8 bits
Range of presetting register	8 bits
Clock accuracy	± 0.005 percent
Signal level for external and additive input	TTL

Common LJSP specifications:

Number of connections to common busbar	1
Weight (w/o distribution panel)	approx. 1 kg
Power feed/consumption	5 V/4 A

IMS 2-CM 0102 Connecting Unit

The IMS 2 connecting unit is an integrated measuring system designed for automatic control of measuring instruments with built-in interface IMS 2 (IEEE 488, HP IB) connected to 16-bit computers with common busbar.

The IMS 2 interface is of the busbar type; its basic transmission unit is 1 byte. The busbar transmits three types of information: data, information for control of transmission of information and information for control of interface. Program operation is provided by means of four registers.

Up to 15 instruments or devices with IMS 2 interface can be connected to the IMS 2 busbar (see Figure 50).

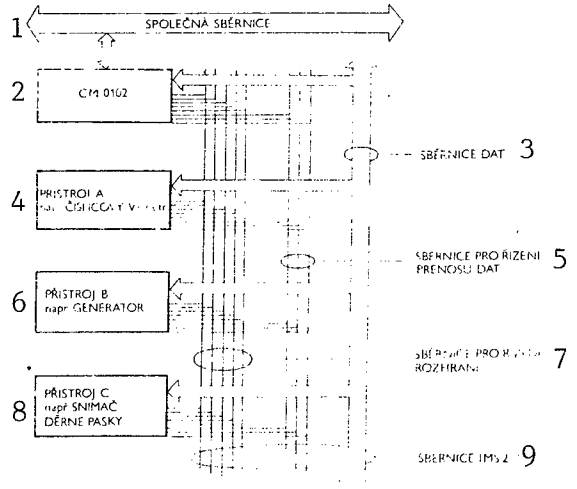


Figure 50. Connection of instruments to IMS 2 busbar

Key:
1. common busbar
2. CM 0102
3. data busbar
4. device A, e.g., digital V-meter
5. busbar for data transmission control
6. device B, e.g., generator
7. busbar for interface control
8. device C, e.g., perforated tape reader
9. IMS 2 busbar

The CM 0102 is structurally formed by two 2/3 plates and a connecting wafer and the requisite cables. The two above-mentioned plates are inserted into any adjacent positions in the systemic unit (see Figure 51).

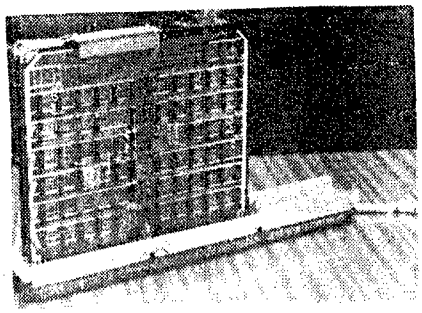


Figure 51. IMS 2-CM 0102 connecting unit

Programming of the IMS 2 unit is provided by the BASIC programming language expanded by instructions CMD, IFC, REN, LOC, FORMAT, OUTPUT, INPUT, WAIT.

Technical specifications:

Transmission speed	max. 250 kbyte/s
Interrupting level	selectable
Number of loads on common busbar	1

Interface functions carried out in accordance with IEEE:

TL--transmitter
LI--receiver
AH1--correspondence receiver
SH1--source of correspondence
SR1--request for service
C 1, 2, 3, 4, 5--control.

CM 9004 Connecting Unit for DASIO 600

The connecting unit for DASIO 600 makes it possible to connect input and output modules of the DASIO 600 system to the common busbar of 16-bit SMEP systems and thus provide contact with technological processes.

The assembly of input and output modules for digital control of DASIO 600 (DASIO 600=CM 9101) is designed for direct connection of control computers with the controlled technological object; its production and marketing is provided by METRA Blansko.

DASIO 600 can use two input/output channels for connection with a computer--one for channel address transmission, the second for transmission of data for the requisite channel. With respect to operating mode, both DASIO 600 and the CM 9004 connecting unit operate in one of following modes:

--address mode, used on the DASIO 600 side for program control of a combination of input and output modules other than binary modification modules;

--cyclic start-up mode for modifying input modules of DASIO 600. The structural design of the CM 9004 connecting unit calls for three 2/3 plates SM 1300, SM 1301 and SM 1302, whereby the required variant always consists of two 2/3 plates with accessories;

--the address mode (designation A) includes:

- --SM 1300 plate,
- --SM 1301 plate,
- --cable, connecting wafer;

--the cyclical continuous mode DMA (designation B) includes:

- --SM 1300 plate,
- --SM 1301 plate,
- --cable, connecting wafer;

--the cyclic start-up mode (designation C) includes:

- --SM 1300 plate,
- --SM 1302 plate,
- --cable, connecting wafer;

whereby configurations A and B differ only in the use of varying circuits on plates and the type of cable used.

The two requisite plates of the CM 9004 variant are placed into two adjacent positions of a systemic unit in the basic or expansion grid, interconnected by the connecting wafer and by cable connected to the DASIO 600 periphery.

Programming of the CM 9004 control unit is provided by a service program under the FOBOS 1, FOBOS 2 and DOS RV V2 operating systems.

Control Unit of the CAMAC Frame

CAMAC is a modular system for the acquisition and processing of data designed originally for the automation of scientific experiments in nuclear engineering and currently also used in the sphere of scientific experiments and control of technological processes. It is designed for connection to 16-bit SMEP computers.

The CAMAC frame control unit will be designed on two plates, the SM 1310 and SM 1321, designed for building into the standard CAMAC unit (SV-022 Polon).

The control unit is fed + 5 V from the CAMAC frame, connection to the common busbar is done by cable.

Technical specifications:

Number of loads on common busbar	1
Power feed/consumption	+ 5 V/max. 4.5 A
Weight	1.5 kg

2.1.9 Structural and Systemic Elements

The passage devoted to the mechanical concept of 16-bit systems with common busbar offered a brief description of the individual elements used in the construction of SMEP systems.

Some of these elements are available individually, which offers users the possibility of expanding their computer configurations in keeping with the availability of individual elements.

Below we offer a description of the following elements:

--CM 0101 systemic unit,
--SM 2016 interconnecting plate,
--CM 4103 common busbar repeater,
--expansion grid,
--casing,
--casing with expansion grid.

CM 0101 Systemic Unit

The systemic unit is described in the section on the mechanical concept of SMEP (see Figures 3 and 52). The basic configurations of minicomputers (SM 3-20, SM 4-20, SM 52/11) always contain at least two free systemic units used for expansion. The concept UBM, universal interconnection block, which can be encountered in this connection, is actually the CM 0101 systemic unit.

Note: In addition to the CM 0101 basic systemic unit--which has all-purpose applications and is used in most systems--use is also made of specialized systemic units; such a specialized systemic unit forms a part of, e.g., the CM 8511 multiplex. These specialized systemic units can be intended for more than four positions, e.g., a part of the CM 5105 control unit of cassette disk memories is a specialized systemic unit for eight positions, i.e., double that of the CM 0101.

SM 2016 Interconnecting Plate for Systemic Units

Every systemic unit connected to the common busbar circuit must use all the K3 positions (see Figure 52). In cases where a position is not taken up by a plate, all such positions of a systemic unit must be taken up by the SM 2016 interconnecting 1/3 plates. Such a situation can occur, e.g., when the existing configuration of a computer is expanded by one systemic unit and into it is built, e.g., a twin-plate unit for contact with the environment and two positions remain free. For the system to function, both positions must be taken up (actually involving interconnection of the common busbar signals "BUS NPG" and "BUS BG 4-7") either by unused plates, e.g., parallel or series adapters, or by the just-mentioned SM 2016 interconnecting plates.

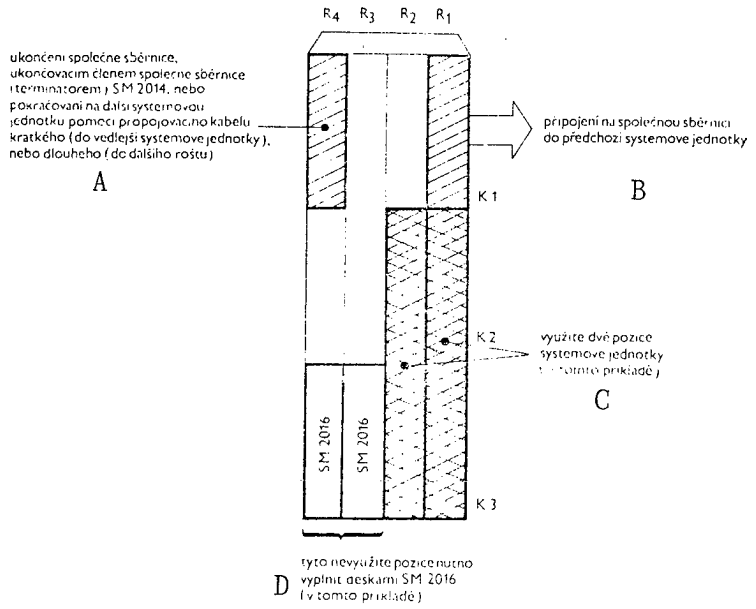


Figure 52. Sample of SM 2-16 extension plate application

Key:

A. termination of common busbar by the SM 2014 common busbar terminator or continuation to another systemic unit by means of a short interconnection cable (to an adjacent systemic unit) or by a long cable (to another grid)
B. connection to the common busbar into the preceding systemic unit
C. two used-up positions of a systemic unit (in this example)
D. these unused positions must be taken up by SM 2016 plates (in this example)

CM 4103 Common Busbar Repeater

The total number of loads on a common busbar is limited to 20. In case this number become exhausted, use is made of the CM 4103 common busbar repeater, which restores the common busbar signals and provides for expansion by an additional 19 loads. In view of the fact that the common busbar is also limited in length, when using the repeater the common busbar can be extended by an additional 7 meters.

The repeater is structurally designed on two 1/3 plates connected by cable. A repeater with a short cable is intended for the connection of two adjacent systemic units in one grid.

Technical specifications:

Lag behind repeater	[figure illegible]
Number of loads on common busbar	1

Expansion Grid

The expansion grid is a mechanically independent structural unit 7U high which is intended for building into a SMEP casing (see Figure 3).

In addition to mechanical parts, it contains a ventilation unit, power sources for the requisite dc voltage dimensioned for maximal load on the grid, a 220 V feed block, two free systemic units, cable for connection with the basic grid and a short cable for interconnecting adjacent systemic units.

The expansion grid has a reserve free position for four additional CM 0101 systemic units.

Casing

An expansion casing is a 19-inch SMEP casing used for building in expansion modules for which there is inadequate room in existing casings or where it is intended to provide a reserve for additional expansions. Examples of modules that can be built into the casing are:

--floppy disk memory (CM 5605),
--expansion units of tape memories (CM 5300.01, CM 5302, CM 5303),
--expansion units of disk memories (CM 5400, CM 5403).

A part of the casing is a power feed block and cable, a ventilation system and panels for covering unused space. The total height of the casing that can be used for building in of modules is 32 U (U = 44.5 mm) in the case of the ALMEZ casing, or 33 U in the case of the OCEL steel casing.

Most expansion modules are suspended in the casing on telescoping supports (disk memories, floppy disk memories, perforated tape peripheries, IZOT 5003 and CM 5300 tape memories). Tape memories are suspended on rotary mounts or attached directly to the front side of the casing.

Technical specifications:

Power feed for casing	220 V/50 Hz
Max. power input per casing	2420 VA
Weight of ALMEZ casing	115 kg
Weight of FE casing	90 kg

Casing With Expansion Grid

A casing with an expansion grid represents a combination of the expansion grid and casing described above.

2.2 Software

The second part of the chapter dealing with 16-bit systems with a common busbar is devoted to software for these systems and is divided into the following sections:

--operating systems,
--program systems,
--telecommunication software,
--graphic software,
--programming languages,
--testing monitors.

2.2.1 Operating Systems

The following part describes the following operating systems:

--LOS,
--FOBOS 1,
--FOBOS 2,
--DIAMS 1,
--DIAMS 2,
--DOS RVR 1,
--DOS RV V2,
--MOS RV V2.

This part further contains a description of expansion software operating under the DOS RV V2 operating system:

--RSZ,
--DTS,
--SORT,
--MTD,
--text processor,
--set of programs for VTV.

LOS

The LOS perforated tape operating system is of the lowest order among the many operating systems for 16-bit SMEP systems.

The individual programs of this operating system are located on perforated tapes and in case of need are introduced into the working memory storage.

Languages: Assembler, BASIC and FOCAL.

The use of the LOS operating system comes under consideration in case of other than disk configurations of computers with a common busbar.

FOBOS 1

FOBOS 1 is a single-user, disk-oriented operating system for the interactive development of programs and for applications in real time. It contains a single-task monitor for a twin-task monitor of the foreground/background type in which the foreground with higher priority operates with a real time task and the background carries out program development or processes a batch task.

FOBOS 1 is suited for mass data processing, scientific and technical calculations, mathematical and economic computations, processing of various tasks in real time.

The advantage offered by this operating system is its processing speed and simple operation. The following languages can work under this operating system: Macroassembler, FORTRAN IV, BASIC and FOCAL.

Typical hardware configuration:

--SM 3-20 minicomputer in basic configuration.

FOBOS 2

The FOBOS 2 operating system represents in comparison to the FOBOS 1 operating system a higher improved version. Some of the properties of the FOBOS 2 operating system are derived from those of FOBOS 1, others represent significant changes and expansions. The objective of these changes is to achieve higher efficiency of operation.

The FOBOS 2 operating system, just as the FOBOS 1, facilitates operation in a single program mode when only one program is processed, or in a multiprogram mode when the means of the computer system are divided between two programs. From the user's viewpoint the working memory storage is divided into two parts; a foreground sector and a background sector, whereby processor time is assigned in successive steps to both programs. The foreground program has a higher priority than the background program. These two modes can be used on computers with memory of up to 32K words.

However, the FOBOS 2 operating system makes it possible to use the multiprogram mode even for a memory with a capacity exceeding 32K words. By means of a monitor for expanded memory (XM) it uses memory pagination and in so doing permits the use of memories of up to 128K words.

Other expansions of the FOBOS 2 operating system include new service programs and expansion of the possibilities of existing service programs.

The FOBOS 2 operating system includes the following key programs:

--three types of mutually compatible monitors--single angle, double angle (foreground and background), and an MX monitor for operation in a system with expanded memory;

--translators and compilers:

--Macroassembler,
--FORTRAN IV,
--BASIC,
--BASIC S for IMS 2 measuring systems,
--COBOL;

--text editor;

--service programs (interpreter of chain instructions, program for operation with peripheries, an extraction program, program for extraction from libraries, communication program, librarian, program for operation with sets, programs for batch processing, a tuning program, etc.).

Thus, the basic difference in comparison to the FOBOS 1 operating system is constituted by the fact that it facilitates multiprogramming in configurations with operating memory storage in excess of 32K words.

The FOBOS 2 operating system can operate with the basic configuration of any SMEP computer with a common busbar.

DIAMS 1

The DIAMS 1 is an interactive, multiuser data base operating system. Its possibilities are given primarily by the properties of the programming language MUMPS, which it uses. MUMPS is a higher programming language oriented toward operation with chains and facilitates such text operations as, e.g., determination of the contents of a certain part of text, connecting or dividing of text. DIAMS frees the user from the necessity to program peripheral equipment and structuring of the data base in the traditional sense.

The MUMPS language is interpretive, i.e., each user instruction is carried out directly with the generation of an intermediate code. This does away with operations connected with translating, compiling and program start-up as in, e.g., the Macroassembler language.

The programmer can concentrate on the logic arrangement of his data base and the generation of logic required for data processing. The user makes symbolic reference to all data, whereby the data are stored by the operating system in the memory hierarchically and arranged into tree-type structures. Physical and logic assignment of memory for a tree-type structured data base is provided for by the operating system, the programmer defines merely the requisite relations between these data. The data base thus generated can be made accessible to all users of the system or to all users of a certain user class.

The operating system is permanently present in the working memory storage and, depending on type of generation, takes up 11-40K words. The remainder of the working memory storage can be divided into user sectors and into buffer memories of the operating system. Terminals and individual user sectors are not permanently assigned. The division of memory into user sectors is automatic. The standard size of a user sector is 2-2.5K words. This value

can be changed in the course of generation in a range of 128 to 4096 words. In user registration into the operating system the assignment of the requisite sector to the user is entirely automatic. There can be a maximum of 16 such sectors.

In each user sector is a single user program together with locally defined data and the requisite systemic information. The user program runs for the allotted time and control is then transferred to deal with the next task of highest priority.

With the use of a computer that has a 128K memory, the operating system can accommodate 16 to 40 users simultaneously. With a computer having a memory of up to 32K simultaneous operation can be provided for approximately four users.

The DIAMS 1 operating system consists of the following basic modules:

--executive--controls time allocation and multiprogramming in the system on the basis of a system of priorities;

--monitor of input/output systems--monitor operation of the terminal and of peripheral systems and processes interruptions;

--MUMPS language interpreter--provides for direct performance of instructions and displays error reports on the terminal;

--data base control program--provides for physical and logic control of the data base.

Data stored on a disk in tree-type structures are called global data and are formed into global variables (junctions).

Global variable junctions of the same name form global fields of the mentioned hierarchical tree-type structure. Contrary to local data--which are defined only in the user sector and are only temporary--global parameters are permanent and can be used by other user programs.

The set of service programs belonging to the operating system is divided into two groups:

--systemic service programs, which can be used only by the system programmer and serves for control and maintenance of the operating system;

--library service programs that can be used by all users, e.g., printout of programs directory, copying of programs, etc.

The operating system provides protection for systemic and user sets. This protection is implemented by means of an indentification number and a user's or programmer's password. The user can operate with all sets of his class, the programmer can change sets, generate new sets, etc.

DIAMS 1 operates with the following types of data:

--chain--max. sequence 132 ASCII symbols;

--a number with a fixed decimal point or two decimal points in a range from 214 74836.47 to 214 74836.47 or a number with a floating decimal point of 4-word length, approximately in a range of -10^{-38} to 10^{+38} (precision for 17 decimal points).

Minimal hardware configuration: SM 3-20 minicomputer in basic configuration,
SM 4-20 minicomputer in basic configuration,
(min. with 1 disk memory).

Expansion modules: max. 16 display terminals connected via ASAD-CM 6002,
max. three CM 8511 multiplexes each with 16 lines with terminals, e.g., CM 7202,
max. 4 disk memories,
max. 4 tape memories.

DIAMS 2

The DIAMS 2 is an integrated system, including an operating system with a built-in data base control system and its own interpretive programming language DSM (Digital Standard MUMPS).

The operating system is suited for the development of a modular, easily modified system for data bank control and for processing large volumes of text data with a higher number of simultaneously participating users operating in interactive mode.

DIAMS 2 offers users the possibility for easy generation and modification of programs written in the DSM language and the means for generating a data base that is accessible and modifiable. The system monitors the users' access to the system on the basis of a multilevel, dynamically specified protective plan.

The key differences in comparison to the DIAMS 1 operating system can be summarized by the following points:

--the language is a complete implementation of the standardized version of ANSI MUPS (X. 11. 1 - 1977) with expanded Z region,

--a new self-optimizing structure of global sets with chain indices,

--potential for the formation of a distributed data base,

--recording of information about operation on tape-log,

--temporary storage of printing set on tape,

--expanded set of systemic and library programs,

--modified version of the system for the generation and maintenance of reserve copies.

Time sharing and multiprogramming in the dynamic assignment of user sectors is provided for by the executive system. Multilevel cyclic planning with a varying priority of tasks in line provides for the maximum utilization of the central unit. Initially, the task is incorporated into the waiting line with the highest priority and once it reaches the head of the line it is transferred into the line of running routines. Contrary to the DIAMS 1 operating system, the time interval assigned to routines is constant and does not depend on the priority of a given waiting line. Nevertheless, in view of the employed system of cyclical change in priority (preempting), the response time is shorter.

Contrary to static structures used in, e.g., COBOL and PL/1, sets in the DIAMS 2 system are maintained as dynamic self-optimizing B trees with variable length of recording (up to 256 symbols). Data base control is from the systemic viewpoint more complicated than in DIAMS 1 but, on the other hand, offers the user the advantage of simpler devising of global structures and elimination of potential entry of an ineffective data structure.

The interpreter of the standardized DSM language makes possible additional applications in cooperation with other modules of the operating system, e.g., interprocessor communication, parallel running of programs or mutual communication between active processes.

The DIAMS 2 operating system is suited for the SM 4-20 or SM 52/11 computers and can accommodate approximately 16-40 users.

DOS RVR 1

The DOS RVR 1 is an operating system with time sharing for a maximum of 24 independent users. It is suited for work in conversation mode as well as for processing data in batches.

The user has at his disposal all the systemic resources and the manner of dynamic planning of processor time, with the sharing of inner and disk memories, constantly provides for high efficiency of processing of tasks.

The operating system's monitoring program provides for the efficient functioning of the entire system through constant dynamic control of processor time use, and operatively assigns the processor, sector of working memory storage, sets and peripheral equipment to tasks which are next in line to provide for the computer's handling of maximum volumes of data. The system automatically and dynamically assigns to each task one of 255 priority levels for processing.

The DOS RVR 1 offers to its users all the requisite resources for generation and processing of data sets. Handling of sets can be controlled either directly from the user's terminal or by the user program. Data sets can be in sequential systems or in systems with direct access. Data sets in systems with direct access can be used by several users simultaneously.

The system provides full protection for data sets. Each user can specify for his sets the degree of confidentiality.

The basic language of this operating system is BASIC PLUS. A part of this language is formed not only by means for computation but also control instructions and other means that make it possible to use the BASIC PLUS interpreter to control the operation of the entire computer system. It is envisioned to incorporate into the DOS RVR 1 operating system a compiler of the programming languages FORTRAN IV and COBOL.

DOS RV V2

The DOS RV V2 is a multiprogram, event-controlled real-time operating system. It comes in two basic variants, given by the size of internal memory of the computer used:

--mapped version for computers with memory up to 128K words, which offers full functioning; it is suited for approximately 8-15 users, depending on the mode of operation and the manner in which the system's services are utilized;

--unmapped version for minicomputers with memory up to 32K words, which offers somewhat limited possibilities and is suitable for approximately three users.

The operating system in its mapped version makes it possible to process or combine real-time tasks of high priority with a necessarily fast response to external events involving less urgent but considerably voluminous tasks in multiprogram mode with time sharing. The manner of assignment of memory, overlapping of program segments, fast cooperation with external disk memory, the dynamic compression of memory as well as the system of priorities provide for high efficiency in processing of tasks. The system is protected against misuse by unauthorized persons, individual sets also being protected.

The operating system includes the following software components:

--control programs: execution,
monitor for communication with user,
programs for control of peripheral units,
system for operation with sets;

--service and auxiliary programs, making it possible to generate, tune, modify and correct programs, undertake conversion of sets, provide printouts of the contents of sets, verification of sets, etc.;

--multipurpose protection programs, which offer protection for individual users, i.e., access rights to sets and systems.

During a power outage the system provides for automatic new start-up and continued operation. Among the advantages offered by this operating system is its potential for parallel operation in various problem areas with the use of all the languages it has at its disposal. This means that it is possible

to carry out in parallel, e.g., data acquisition, scientific and technical calculations and tuning of programs, and all of this in various languages.

The following languages can operate under this operating system: Macroassembler, FORTRAN IV, FORTRAN IV PLUS, COBOL, BASIC, BASIC PLUS 2.

This operating system also supports the following purpose-oriented software:

--RSZ system: a system for operation with recording-oriented data sets organized by sequence, relation or indexing;

--SORT: program for sorting of recording-oriented sets;

--SYRPOS 1: a system for controlling computer and terminal networks based on SMEP minicomputers providing for communication among computers and terminals, remote processing and control of tasks, handling of sets and access to remote sets, etc.;

--SM GRAF: a set of programs in FORTRAN language for the CM 7405 graphic terminal;

--MTD: a set of programs making it possible to turn out a magnetic tape in the standard format of other computers (JSEP, IBM, SIEMENS etc.);

--text processor;

--set of programs for scientific and technical calculations.

The mentioned languages and expansion software will be described in closer detail later.

Typical hardware configuration:

--SM 4-20, SM 52/11 or SM 50/50 minicomputer with 128K-word memory in basic configuration, expanded by terminals of the unit for contact with the environment or other peripheral units.

MOS RV V2

The MOS RV V2 is a small multiprogram operating system for operation in real time with residential operation in the working memory and providing merely for carrying out of tasks.

The MOS RV V2 operating system is fully compatible with the subset of the DOS RV V2 operating system; programs operating under MOS RV V2 operate without any changes under DOS RV V2.

The MOS RV V2 is intended for 16-bit SMEP minicomputers with a common busbar and no external memory. Development of programs and generation of the system is done on a host system under the DOS RV V2 operating system. Tasks can be written in Macroassembler, FORTRAN IV or FORTRAN IV PLUS, translated and combined on the host system.

The MOS RV V2 will find application in diskless versions of computers with a common busbar, in computer networks, etc.

Expansion software working under the DOS RV V2 operating system:

1) RSZ:

The RSZ system is a group of programs intended for operation with sets under the DOS RV V2 operating system. At the time of task combination these programs are combined with user programs and thus form a connecting line between the user task and the data structure of the medium. RSZ in combination with the DOS RV V2 is an efficient and flexible system for storage, selection and modification of data in sets.

RSZ generates for sets three types of organization:

--sequential,
--relational,
--indexing.

A set's organization determines the manner of selection and storage of data in the set. These techniques are known as access modes to sets:

--sequential access,
--random access,
--access by means of addresses of entries.

After the generation of a set by means of RSZ, the user program can work with data in the sets.

The RSZ system uses a number of service programs:

--program for generation of reserve copies of data sets on disk or tape,

--program for transfer of recordings between two RSZ by sets of random organization or format of recording,

--program for display of information about data and the structure of data in the reserve copy sets,

--an optimization program, etc.

2) DTS:

The DTS is a dialogue system for direct, expedient and simple operation with sets generated by means of the RSZ system, the presence of which is required during operation under the DOS RV V2 operating system. Operation with this system offers analogous possibilities, such as operation on the basis of applicational user programs, yet it is shorter and more efficient than the generation of new source programs that has to be followed up by translation and combining the program into a task that can be run.

This dialogue system operates as an interpreter.

DTS functions:

--selection of groups of recordings according to instructions,
--sorting of a selected group of recordings according to specified criteria,
--defining of a certain recording for further processing,
--changing of value in a specified field of a selected recording,
--erasure of recording,
--performance of a certain sequence of instructions for all or selected recordings in the set.

The sequence of instructions that are often used in operation with the inquiry system can be retained for further use in an indirect command set and make repeated use of them in case of need. The DTS makes it possible to use the entire set of arithmetic operations (sum, difference, product, share, negation) and statistical operations (sum, average, minimum, maximum).

One of the instruction of the DTS is the instruction HELP, which displays all DTS instructions to include a guide to their use.

3) SORT:

SORT is a program that, according to recording codes and sorting selection, makes it possible to sort any random data set generated with the aid of RSZ.

SORT provides for four basic types of sorting:

--sorting of entries--a sorted set is generated out of an input set by transfer of entire entries;

--sorting of indicators--a table of individual entry indicators is generated from the input set, which is then sorted and, through a new run through the input set, a sorted input set is formed;

--generation of an address set--the input set is not sorted, there occurs merely the formation of a sorted set of addresses in the desired sequence which can be used for reading entries from the input set;

--generation of a set of indices--a set of addresses is generated just as in the preceding sorting procedure that contains in addition the values of codes by which the address set is sorted.

This sorting program provides for the section from a large number of sorting codes depending on varying user needs.

SORT operates exclusively under the DOS RV V2 operating system.

4) MTD:

The MTD is a service program which on a SMEP minicomputer under control of the DOS RV V2 operating system facilitates the reading of a standard magnetic tape made by computers, JSEP, SMEP, IBM, ICL, Siemens, Univac, PDP, etc., and also makes it possible to come up on a SMEP minicomputer with a tape that can be processed in the above-mentioned computers.

Thus, the basic MTD function is the transfer of data from magnetic tape of the basically used formats onto a disk or from a disk to a magnetic tape of ANSI format, format without set indication readable on JSEP type systems, or onto a tape with nonstandard recording.

MTD also makes possible the transfer of data from disk to disk, printout from disk or tape, display of these data on a display terminal and recording of data from the terminal on disk or tape.

MTD changes the code from EBCDIC to ASCII and vice versa and facilitates changes in blockage of recording. The records can be of fixed or variable length with block length ranging between 14 to 2048 syllables. Length of records can be selected in a range of 4 to 512 syllables.

Typical hardware configuration:

--SM 3-20, SM 4-20, SM 52/11 minicomputer in basic configuration with magnetic cassette tape memory formed by the following units:

--CM 5300,
--CM 5300.01,
--CM 5302,
--CM 5303.

5) Text Processor:

The program unit Text Processor operates with text sets generated by editing programs under the DOS RV V2 operating system and carries out their final formatting (evening of lines, graphic format, printing of headings, lower/upper case conversions, pagination, numbering of chapters, etc.). The program is controlled by directives specified in the source text. Output can occur through any of the computer's outputs (terminal, printer, perforator, disk set).

Typical hardware configuration:

--basic configuration of the SM 4-20 or SM 52/11 computer.

The installation of the text processor calls for a contiguous space for 58 free blocks on a disk medium.

6) Set of Programs for Scientific and Technical Calculations:

The set of scientific and technical programs for scientific and technical calculations is formed by more than 100 programs in the FORTRAN IV language

and makes it possible to carry out various mathematical, technical, statistical and other calculations. The programs are independent of inputs/outputs and are available in source form.

Algorithms for individual programs were selected on the basis of the following criteria:

--minimum demands on memory,
--unambiguity of implementation,
--speed of calculations.

This set of programs can be roughly divided into the following areas:

--operations with matrixes,
--operations with polynomials,
--special functions (gamma, Bessel, integrals),
--nonlinear equations,
--Fourier analysis,
--standard differential equations,
--random numbers,
--statistics.

2.2.2 Programming Systems

The following are among the software systems described in this section:

--PPPD 1,
--GOLEM,
--VYUKA,
--MARKAB (PPPD 2),
--VU BASIC.

PPPD 1

The program system PPPD 1 V02.C UNIVERSAL is an acquisition, multikeyboard system of up to eight terminals facilitating the acquisition and preprocessing of data.

The function of operators in the system and data control is controlled by forms. Forms for specific applications are generated by the user through definition of the parameters.

The PPPD 1 system operates under the host monitor of the FOBOS 1 operating system.

The PPPD 1 set of programs consists of the following components:

--monitor of the operating system,
--program for operation with sets,
--service programs of inputs/outputs,

--program for control of parallel operation of terminals,
--supervisor programs,
--automatic recordkeeping programs,
--programs for generation, printout and editing of forms,
--programs for guidance of operators (during preparation, control, updating and editing of data),
--programs for preprocessing of data (programs for combining batches on a disk, sorting generator, simple print generator, transcription to magnetic tape, offering the possibility of selection, combining of batches on a magnetic tape, functions addition, subtraction and multiplication with a fixed decimal point).

The type of each entry (word in a sentence) is defined by the user in a corresponding form. The PPPD 1 V02.C UNIVERSAL provides for selection among the following types of entry:

C--integer with a sign,
J--numerical chain without sign (insignificant zeroes remain),
K--same as J, additionally controlled on control number,
F--number with a decimal part and a sign (of the format type),
T--alphabetical chain,
A--alphanumeric chain.

The length of entries in the standard version is as follows:

C	15
J	24
K	24
F	15
T	24
A	24

In the standard version of the system sentence length is 20 words.

Length can be changed in the program. The size of a batch can be selected and is determined according to the number of symbols in the sentence.

The number of batches stored simultaneously on a cassette disk is given by the disk's capacity, which is 4800 blocks (1 block=512 symbols). The system itself needs 400 blocks. At operators' output of 10,000 strikes an hour and at work on 8 terminals, the data placed on the disk will come from approximately 3 work shifts.

Data can be controlled and updated during preparation according to the type of recording, according to the dimension of the recording (after reaching the maximum dimension in accordance to format the carrier stops moving), according to control number for type K entries and according to the number of decimal points for F type entries (possibility for automatic insertion of a decimal point and zeroes behind decimal point).

For nonobligatory entries the system automatically supplements the defined dimension chain according to the form (standard spacing). Automated duplication of entries is provided by the key LF and that of the entire block of entries by the key CR. Automatic filling in of decimals (including the decimal point) is provided by F type entries.

Any symbol can serve as a filler symbol for entries. Supplementing by filler symbols does not occur during the insertion of an entry, but is done as needed by independent selection in the mode of the system's supervisor. Filler symbols during printing are spaces (in cases where entries are not supplemented by other symbols).

The type of entry is sequential. The system permits operation with virtual sets which, however, are more demanding on the disk's capacity. The user is provided in the system by tools for their use.

Control copies of data batches can be printed on a linear printer or on a terminal. It is possible to print entire sentences, or selected words from sentences in the selected sequence. During printing it is also possible to print control numbers and serial numbers of sentences.

The PPPD 1 facilitates the combining of batches into final sets directly on the disk and their sorting according to the selected sorting criteria. Combining of batches into final sets can also be done from disk to magnetic tape. During the transcription of data onto magnetic tape, it is possible to transform the data according to the selected table.

Sorting is done with the use of three types of sorting generators in accordance with a random number of sorting criteria. After the completion of sorting there occurs an automatic transfer to the state that preceded sorting. One type of sorting calls for the interruption of operation on all other terminals and transfer under the communications monitor. The remaining two types operate directly within the PPPD 1 system.

The transcription of data onto magnetic tape is made possible by a program which facilitates decoding into any random code (for JSEP, TESLA, etc.), entry of selected words from sentences in the determined sequence, combining of batches into a single set, etc. On a magnetic tape the number and size of sets is limited only the tape's length of 1,200 feet.

Printout from the magnetic tape of data that has already been decoded and entered in accordance with the conventions for JSEP computers (or other types of computers) can be done in accordance with a decoded table either on the terminal or through the printer.

The programming languages used in writing all-purpose applicational programs are VU BASIC, Macroassembler, FORTRAN IV. The PPPD 1 system is an open system, meaning that users can generate their own program modules by which they expand the system's possibilities in case it does not fully cover its needs by programs that are supplied as standard equipment.

The PPPD system includes batches, sets and forms generated by other systems.

Protection for the system and data sets is provided by an access procedure and password control after each entry into the system's supervisor mode. The password also specifies for operators the types of operations they can perform in the system. Another form of protection is automatic control of used-up space on a disk.

The system's automated recordkeeping keeps track of form, batches and data sets, of operators' performance, size of batches, number of errors in batches and their arrangement, etc. This recordkeeping also precludes the operation of one operator from being affected by that of another.

Automatic control of used-up space on a disk automatically closes a generated batch, thereby limiting losses of entered data. A printout of data about the space available on a disk facilitates the planning of operations during a shift.

By corrections in a batch in the PPPD 1 V02.C UNIVERSAL system we understand corrections of entries after completion of sentence, retrieval of sentences in a finished batch by the sentence's mask or index, corrections during control by repeat entry, and corrections during optical control. Additional sentences can be placed into batches at random points, words can be corrected in sentences, or sentences can be eliminated from the batch.

Control of batches (in all forms) is arranged so that the operators control only entries (words) specified in the form for control. Other entries progress further without control.

Segmenting a set into smaller batches facilitates parallel operation on one system.

Selective batch correction makes it possible to select a sentence according to its mask or index; the sentence becomes displayed on the terminal. With regard to this sentence, the operator can decide that:

--the sentence is valid and operation continues,
--the sentence is to be deleted,
--some words in the sentence will be corrected and operation continues,
--new sentences will be inserted behind the sentence and operation continues,
--operation ends.

Control by control numbers makes it possible to control prepared data by totals of magnitude data, e.g., per document and per batch.

Performance of operators can be printed out in outline from the automatic recordkeeping system even in the course of operation.

Output of data onto a magnetic tape takes a form which makes it possible to process the prepared and preprocessed data on other computers (JSEP, SMEP, TESLA, IBM etc,), the so-called transport data--off-line mode.

Typical hardware configuration:

--SM 3-20 minicomputer in basic configuration with CM 7202 expansion display terminals of up to eight units.

The V03 version of the PPPD 1 system now under preparation for the SM 50/50 computers with a 32K memory capacity and with a floppy disk memory is also intended for the acquisition, preparation and preprocessing of data from a maximum of eight terminals.

Organization of operations in working with data is as follows:

--system start-up from a floppy disk,
--generation of statistical and record keeping sets on the disk,
--preparation of data in ASCII code,
--transcription of data from ASCII code onto an empty disk into EBCDIC code.

With the use of suitable hardware and software it is possible to precess prepared data.

PPPD 1 V03 software will include:

--a set of all-purpose application programs,
--program for operation with peripheries,
--program for control of parallel operation of terminals with the programming system,
--control programs--monitor and service programs of peripheries.

The set of all-purpose application programs is controlled by the supervisor, which provides for the following operational modes:

--preparation of data according to forms,
--generation of forms,
--generation of statistical set of batches,
--printout of recordkeeping and statistics,
--generation of recordkeeping of forms,
--control and correction of data batches,
--control copy of data batches,
--combining of batches into sets,
--sorting of data sets,
--transcription of data from ASCII code into EBCDIC code,
--decoding into another code,
--editing of batches,
--preparation of source programs in Assembler and IN FORTRAN.

Preparation under the PPPD 1 V03 system has a multiple backup:

--access to the system is allowed only to authorized operators (code + password),

--the system contains a control part providing mutual protection for data batches and individual operator terminals,

--the password controls whether a given operator is allowed to operate in the selected mode.

GOLEM

The GOLEM V3.2 system is an integrated set of programs for the acquisition, preparation and preprocessing of data capable of working with up to eight (six) terminals. It uses the monitor of the FOBOS 1 operating system. It uses the direct access method for gaining access to data in disk memories. The result of the system's operation are sets whose structure is suitable for processing on various computer systems such as JSEP, IBM, SIEMENS, etc.

The GOLEM system uses the GUBAS programming language, which is based on a synthesis of the BASIC language and is specially adapted for GOLEM. It differs from the BASIC language mainly by the shortening of instructions to two letters.

A variant of the GOLEM system is the 4.1 version, which operates under control of the DOS RV V2 operating system. A batch generated under the GOLEM V 4.1 system can be directly processed by the program of the DOS RV V2 operating system. The 4.1 version is programmed exclusively in the Macroassembler language, which provides for fast response, particularly with a large number of terminals.

In addition to the 4.1 version, work is also in progress on the 8.0 version, which uses the DIAMS operating system.

MARKAB (PPPD 2)

MARKAB is the designation of a system designed for the acquisition, preparation and preprocessing of data, with former work designation PPPD 2.

The MARKAB system, identified in closer detail as MARKAB [sic], consists of two key components:

--the host operating system DOS RV V2,
--a subsystem for the acquisition, preparation and preprocessing of data.

The programming language used in devising the MARKAB system was BASIC PLUS.

Operation in the system is controlled by the system's supervisor, which logically connects individual operator stations to the system. The system supervisor further controls the output process of prepared data into the output set for a magnetic tape, a disk or to the printer. Data on magnetic tape are in a form suitable for final processing on hierarchically higher computers, e.g., JSEP, IBM, Siemens, or the generated output sets can be processed by the computer itself.

The work of the data preparation operator is controlled in the MARKAB system by formats. Input control formats and input formats are used in the process of data input. The input control format controls the input of data in the global sense (which input formats are to be used, which fields are to be duplicated, which are to be expanded, etc.). The input format specifies each entry in detail, including its control, length, method of verification, supplementing, etc.

The operator can generate input batches, can verify data, retrieve, interrupt operation and resume it, it can close a batch and display the state of data preparation.

The MARKAB system supervisor has at its disposal modes for copying formats, generating formats, compiling formats into a library, operating with terminals, codes, passwords by displaying the state of work of individual operators, the state of libraries. The system's supervisor also provides for the generation of output batches with the aid of output control and output formats.

Typical hardware configuration:

--SM 4-20 or SM 52/11 minicomputer in basic configuration with expansion display terminals (max. 32) and other peripheries (e.g., line printer, large-capacity disk memory).

VU BASIC

BASIC for more users--multiuser BASIC (VU BASIC)--is a system containing its own operating system with components of the FOBOS 1 operating system and a dialogue language of the BASIC type, which facilitates simultaneous operation with up to eight users.

In comparison to the standard BASIC language, the multiuser BASIC contains some additional instructions, and other instructions are used in a different form. The differences are constituted either by the needs of the multiuser type of operation (connecting of the user to the system by means of an identification and a password, protection of sets against intentional or accidental damage or destruction by another user, assignment of peripheral units, etc.), or by expansion of possibilities (new instructions, keys, functions, etc.).

An important role in the operation of the VU BASIC system is played by the so-called system supervisor, which assigns to users their identification and password, provides for operation of the entire system, assigns to individual users sectors of the memory, etc.

VU BASIC can be operated as a single task in the system with a single-task monitor or, with a twin-task monitor, it can operate both in the foreground and background.

VU BASIC can operate in two basic modes--either with the use of the instruction HELLO or without it.

When operating with the instruction HELLO, operation with sets is limited by the access rights of individual users, and each user is assigned an identification and a password by the system's supervisor.

When operating without the instruction HELLO, all users are privileged and have access to all sets.

The distribution medium contains:

--programs in a form capable of start-up,
--source programs in BASIC for the system's operation,
--relative modules for the generation of various variants of multiuser BASIC,
--source programs in Macroassembler required for connecting user functions in Macroassembler.

The multiuser BASIC in the form capable of start-up comes in two variants:

--MUBAS.SAV, for operation in single- or twin-task monitor,

--MUBAS.REL, for operation in the foreground.

Both variants have an overlapping structure and all properties are selectable.

From among the supplied relative modules the system's supervisor can assemble various variants of multiuser BASIC. Multiuser BASIC does not facilitate the specification of systems by means of logic names and the processing of multireel sets on tape memory. In start-up of the VU BASIC set the systemic programs must be in place in the system. After start-up the system supervisor must determine in the initial dialogue the characteristics and properties of the required method of operation. A connection program makes it possible to connect to the system user programs in Macroassembler. VU BASIC makes it possible to form sequential and virtual sets on disk memory, on tape memory only sequential, whereby only one set can be open on each unit. The protection of generated sets is determined by their class (public, group, private). The processing of a set is divided into four types (start-up, reading, updating, complete processing).

Typical hardware configuration:

--SM 3-20 or SM 50/50 minicomputer with 32K-word memory in basic configuration with the requisite number of expansion terminals (maximum of eight).

VYUKA

The VYUKA V01.A system for the automation of instructional processes was developed on the basis of the multiuser version of the BASIC-VU BASIC language.

Up to eight students-users can operate in a dialogue mode in the system, who can select a certain subject for study and verification of knowledge in the form of a test.

The system consists of:

a) programs for defining the curriculum, the progress of instruction, asking of questions, analysis and updating of sets;

b) sets of segments of the program designed to guide the student during operation in the system of programmed instruction, asking of questions, analysis of answers, printing of explanations and making an entry about the student's performance for the user of the instructor;

c) programs for printout of the record of students' performance.

The instructor defines in the program sub point a):

--initial information,
--questions,
--answers (serial number of question, evaluation, text of answer, key direction of continuation and the number of the subsequent question); evaluation uses three grades:

1--correct,
2--partially correct,
3--incorrect.

The answer is formed by a text chain with 9 maximum length of 72 symbols.

The system makes it possible to select instruction in the form of tests in 10 subjects (scientific disciplines, topics, etc.). During the instruction process a set providing information about the student's progress is compiled in the program sub point b).

It includes the following data:

--the student's registration number,
--text of the question,
--text of the answer,
--evaluation (S-- correct, CS-- partially correct, N-- incorrect),
--abbreviation, if explanation was used.

Sub point c) in the program the instructor can control any set with information about the progress of a student's work.

Prior to starting operation with the system on terminals (numbering 1 to 8), the system engineer dialogue must be undertaken.

The system for automation of the teaching process comes with a generated VUBAS.SAC set for a single-task monitor. Modules in objective configuration are not supplied with the system. These modules are available upon user request.

Typical hardware configuration:

--SM 3-20 or SM 50/50 minicomputer with 32K-word memory in basic configuration with up to eight expansion terminals.

A hierarchically higher version of the VYUKA instructional system contains many improvements that find practical application in the process of instruction (e.g., classification using five grades).

2.2.3 Telecommunication Software

There are two basic approaches to devising systems for remote data processing with SMEP minicomputers--the formation of nonhomogeneous systems in which heterogeneous systems--e.g., SMEP and JSEP--are interconnected in the so-called emulation mode on the basis of compatible communication interfaces and routines and, further, the formation of homogeneous systems where systemically compatible SMEP units form a uniform computer network called SYRPOS.

Emulation Routines

Emulation routines make it possible to interconnect SMEP minicomputers with a host JSEP computer or an equivalent computer by means of the EC 7921 interactive routine or the EC 8514 batch routine.

The EC 7921 interactive routine is software for SMEP minicomputers operating under the DOS RV VA operating system (see Figure 53), which enables the minicomputer user to communicate with the host JSEP computer. Herein the JSEP computer views the thus connected SMEP system as an EC 7921-type periphery, so that no extensive changes need to be made in the large computer's basic software.

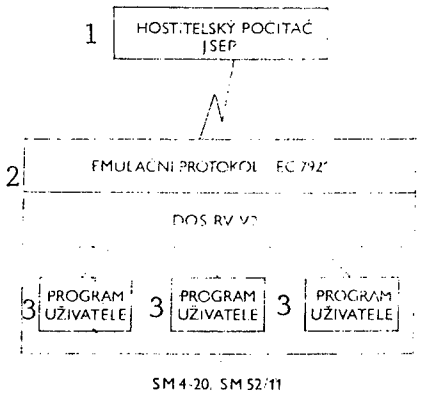


Figure 53. Structure of EC 7921 emulation routine

Key:
1. host computer
2. emulation routine
3. user's program

The user program can form a transmission channel between the SMEP computer and the host JSEP computer and avail itself of all the services of the DOS RV V2 operating system. In so doing it can make use of all the technical resources of the host computer, e.g., disk memory; of advantage is the fact that communication can be initiated by the user program.

All operations connected with this communication, including temporary storage of print sets on a disk, formatting, etc., are provided by the emulation program. The emulation program can serve up to six independent synchronous lines with the BSC routine.

The EC 8514 batch emulation routine is software for SMEP minicomputers, operating under the DOS RV V2 operating system, enabling the minicomputer user to generate data sets with the aid of service programs of the DOS RV V2 operating system and transfer these sets by a simple instruction either to the host computer (see Figure 54) or to another SMEP minicomputer, which also operates under the DOS RV V2 operating system with EC 8514 emulator.

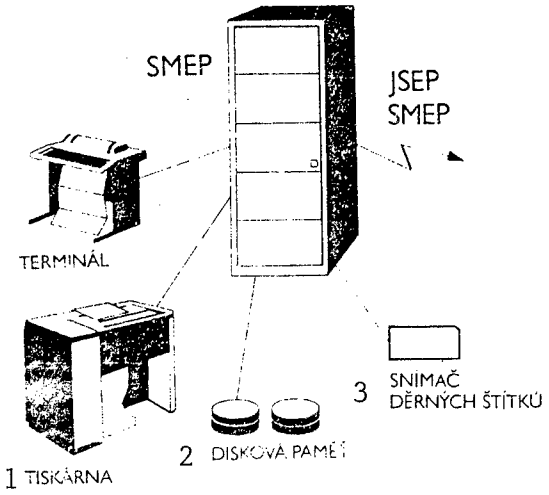


Figure 54. Diagram of connection with the aid of the EC 8514 routine

Key:
1. printer
2. disk memory
3. punch card reader

The received data can be printed on a line printer or entered as a set in the format given by the DOS RV V2 operating system.

The transmitted data can have the form of either 80 symbol entries in a block up to 400 symbols in length during transmission to the host JSEP computer, or 132 symbol entries in a block to other remote SMEP systems.

Up to three data sets which are to be transmitted can be specified by a single instruction for transmission. The routine even keeps simple statistics on the errors occurring in the transmission.

SYRPOS 1

The SYRPOS 1 is a system for the control of computer networks formed on the basis of SMEP minicomputers with the requisite hardware operating under the control of the DOS RV V2 operating system and its variants (MOS RV V2, unmapped version DOS RV V2).

The following computers come under consideration in the formation of computer networks:

--in the function of central computers:

--SM 4-20,
--SM 52/11,
--SM 50/50 with 128K-word memory;

--in the function of satellite computers:

--SM 3-20,
--SM 50/50 with 32K words memory.

A computer network is formed by at least two centers, i.e., at least two SMEP systems with the requisite software.

A center is formed by:

--a computer,
--peripheral system and terminals connected to it,
--software.

The general topology of a SYRPOS 1 network is shown in Figure 55.

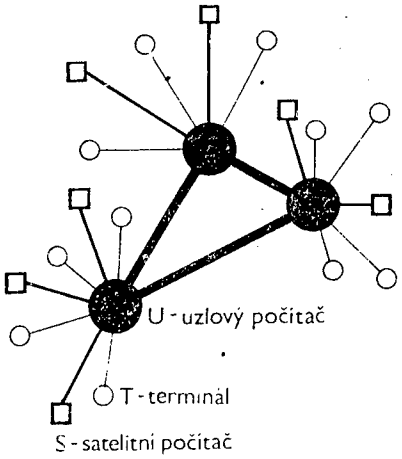


Figure 55. General topology of a SYRPOS system

Key:
U) central computer
S) satellite computer

Users of such a SYRPOS network can use the following functions:

--communication with other terminals--the user of a terminal can transmit messages from one terminal to another located in the network's center, which can be local or be located at a random distance, and can also communicate in dialogue form with any other terminal;

--handling of sets--the user of the terminal can transfer sets from one center of the terminal to another center. It is possible to transfer a set of instructions to another center and carry it out there or, conversely, transfer a set of instructions from a remote to a local center and carry it out there;

--communication between tasks--tasks written in the Macroassembler and FORTRAN IV languages in various centers of the network can exchange data and message via a common communication sphere of the memory of one of the computers;

--access to remote sets and their processing--the user can open, close, copy and read sets stored at any center of the network as long as he has authorized access to the given remote center. Unneeded sets can be erased by the user;

--access to network's hardware--the user of the terminal can use hardware connected to any center of the network;

--remote control of tasks--tasks installed in various centers of the network can be controlled from any given center. It is possible to arrange for the immediate execution of a program, prepare a program for later timed execution or for periodic execution, and also to interrupt the execution of a program.

Moreover, with the use of SMEP minicomputers with 32K-word memory, i.e., SM 3-20 or SM 50/50, it is also possible to use the following functions:

--remote introduction of the MOS RV V2 operating system into a satellite computer--it will adjust the MOS RV V2 with service programs of the host DOS RV V2 and the SYRPOS system into a final form and by a certain procedure connected with the activation of ROM memory in the remote system it introduces the outline of the MOS RV V2 operating system into the memory of the remote computer. After completion of introduction, the thus generated MOS RV V2 activates itself and is capable of operating in the network;

--remote instruction of user tasks tuned on the host system. With the aid of the host and satellite lead-in unit it is possible to introduce into the memory of the satellite computer tasks which were tuned by a hierarchically higher system for the subordinate system.

The systems within the network are protected against unauthorized entry and against accidental erasure of data by an effective protective system. Access to sets in remote centers of the computer network is possible only if the user becomes an authorized participant in the network and in the remote center. To become one he needs permission from the system in the remote center, and prior to the first operation the system makes an inquiry in the block of information related to protection of sets (identification code, password, billing account number).

Concept of SMEP Network Layout

SMEP network layout is a set of rules and conventions including many communication procedures on the basis of which it is possible to device a computer network of a certain topology. The SYRPOS 1 software set which puts this concept into practice can be divided into several strata:

--the user stratum, i.e., dialogue stratum, on which the user generates his data and communications with the network. This stratum is constituted by the DAP routine or by the user's program;

--the logic link stratum at the level of providing network services is formed by the NSP routine, also called the logic connection routine;

--the physical link stratum is formed by the DDCMP routine, which controls a physical serial link (synchronous and asynchronous) by a full or half duplex on two-point connections;

--the hardware control stratum provides for the reception and transmission of individual bits. It performs control of peripheral system and of all communication hardware, including adapters, modems and connectors.

Figure 56 shows the flow of data through the system via individual strata. From the viewpoint of any random stratum the transmission block in a certain stratum is called a message.

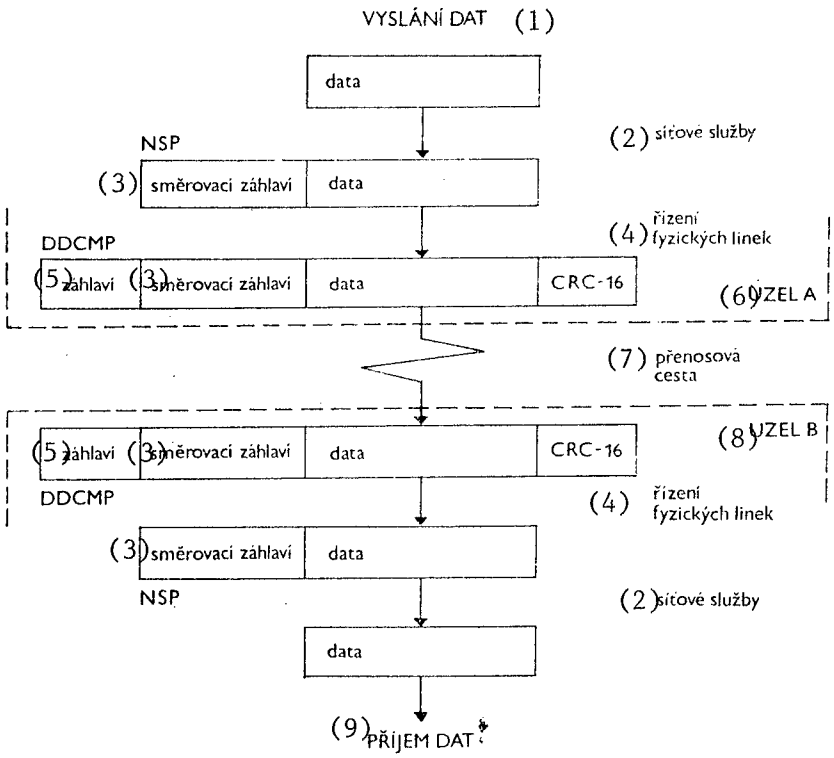


Figure 56. Progress of message from transmitting to receiving center

Key:
1. data transmission
2. network services
3. routing heading
4. control of physical lines
5. heading
6. center A
7. transmission route
8. center B
9. data reception

The subsequent text will be devoted to a more detailed description of the individual routines which make the individual strata work.

DCMP Routine

The task of this routine is to provide for the errorless transmission of data between two adjacent centers; this involves the detection and correction of errors, sequencing of messages and control of the line itself.

Routine's functions:

--generation of a framework providing for correct formation of symbols from 8-bit combinations;

--control of proper sequence and completeness of data during transmission through a network channel subject to interference;

--providing against errors by cyclic code of the 16th order (CR-16);

--effective transmission of a random sequence of bytes in a data field (transparency of data) whereby information in the length of a data field is listed in the message heading (which makes DDCMP different from other procedures, e.g., BSC, SDLC). For this reason this procedure is sometimes not grouped with symbol-oriented procedures such as BSC, where data transparency is provided by the symbol DLE, or with bit-oriented procedures such as SDLC, where transparency is provided by insertion of one bit "0" into the relevant sequence and is called a routine with byte count;

--operation independent of the type of transmission, synchronous, asynchronous at interface with hardware;

--control of a two-point connection operating in full or half duplex;

--synchronization during establishment of connection and during transmission.

It should be realized that the routine itself does not provide for the routing of messages in the network, nor does it care in what physical manner the messages are transmitted and received. These operations are provided for by adjacent strata.

The routine itself provides for communication between stations in duplex mode where operation progresses in both directions simultaneously, or half duplex mode where the direction of transmission changes alternately, both on a two-point or a multipoint connection. Each of these modes has its own precise procedure for cooperation.

Between two centers, one of which at a given moment controls and the other of which is controlled, it is possible to transmit either numbered or unnumbered data messages by which control information is transmitted.

In practice, the transmission occurs so that the controlling station transmits numbered data messages. The controlled station can respond either by another numbered message (which contains information about correctly received previous messages) or a controlling unnumbered message of the types ACK or NAK. To speed up communication, this affirmative or negative confirmation of reception can relate to more received messages.

The messages also carry the requisite information for routing in the network (addresses, etc.) and for control of the requisite hardware.

The routine differentiates between numbered and unnumbered messages. The format of a numbered message is shown in Figure 57.

Figure 58 shows the format of an unnumbered message. These messages transmit control information, data about the state of the transmission and information about requests for retransmission of a certain message.

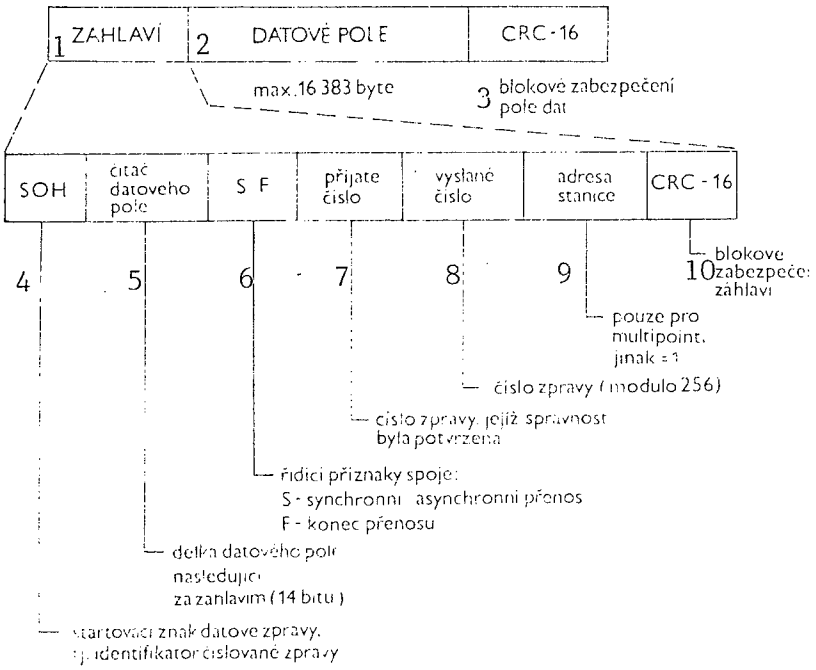


Figure 57. Format of a numbered message

Key:
1. heading
2. data field
3. data field blocking
4. SOH/starting symbol of data message, i.e., numbered message identifier
5. data field counter/length of data field following headline (14 bits)
6. S/F/control signs for link, S = synchronous/asynchronous transmission
   F = end of transmission
7. received number/number of message with confirmed correctness
8. transmitted number/number of message (modulo 256)
9. station address/only for multipoint, otherwise = 1
10. CRC-16/blocking of heading

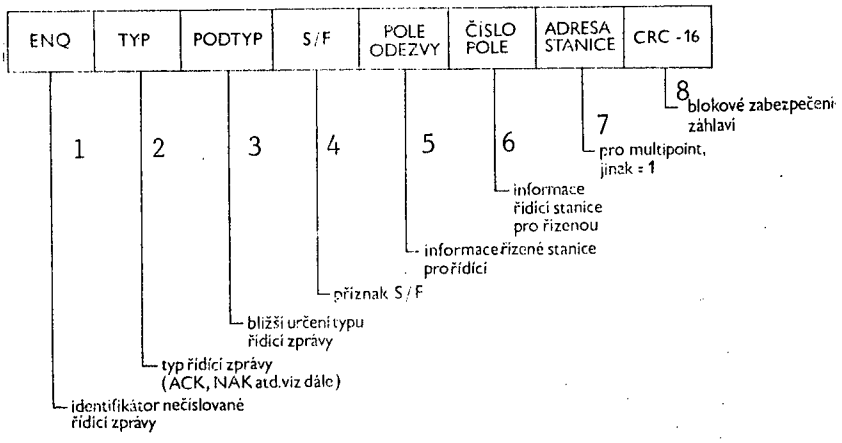


Figure 58. Format of unnumbered message

Key:
1. ENQ/identifier of unnumbered control message
2. TYPE/type of control message (ACK, NAK, see below)
3. SUBTYPE/closer specification of control message type
4. S/F/sign S/F (see sub 6. in Fig. 57)
5. response field/information of controlled station for controlling station
6. field number/information of controlling station for controlled station
7. station address/for multipoint only, otherwise = 1
8. CRC-16/blocking of heading

Selected types of unnumbered messages:

--ACK--message confirming positive reception of a numbered message. It contains the same information as the field called "received number" in the numbered message, i.e., giving number of the message the correctness of which was confirmed;

--NAK--message announcing erroneous reception is used to have the controlled station transmit to the controlling station information about the detection of error in the received message. The cause of the error is coded in the field subtype. Otherwise, an NAK message carries information analogous to an ACK message, i.e., in addition to the mentioned last erroneous messages it confirms the positive reception of previous messages. Reception of NAK in the controlling station usually causes retransmission of the relevant message; only in cases where NAK is generated as a response to noise in the communication channel (that were assessed as message) is NAK ignored in the controlling station;

--REP--response to a message number is used by the controlling station to obtain from the controlled station or from the data channel information about the state of a message bearing a certain number. It is used in cases when no response is received from the controlled station after the transmission of a data message. The response to REP is ACK or NAK, depending on the outcome of the transmission of a message bearing a certain number;

--STRT--start of message is used for establishing initial contact and synchronization between stations operating with the DDCMP procedure; it is intended for cooperation with the message STACK described below;

--STACK--affirmative answer to start of message. STACK is a response to STRT, when the station has completed the initial phase of establishing contact. Just as STRT, STACK contains the relevant numbers of transmitted and received messages. Response to STACK can be a data message, ACK or REP.

NSP Routine

The NSP procedure provides in SMEP a layout for logic connection between tasks or users. It refers only to logic links, not to physical links. This means that several logic links can work in one physical field. A prerequisite for this is the generation of an errorless physical data link (generated by means of DDCMP, a physical field and hardware). NSP performs services for the DAP routine or for the users for control and maintenance of the network.

Functions of the NSP routine:

--functions on dialogue level:

--establishment of logic link for conversation,
--transmission of data along logic link,
--reception of data from logic link,
--control of interruption system at logic link level,
--cancelling of logic link;

--link control functions:

--multiplexing of logic links at physical link level,
--control of logic links' operation;

--functions providing supervision over network:

--detects outages of centers or links in the network and provides supervision over routing between individual centers;

--functions for network maintenance:

--maintains error reporting system.

The format of these messages is analogous--the opening provides identification whether it involves a message transmitting data or control information for the network and, further, routing an NSP routine headline containing various pieces of information about the sender and receiver of the message and about the message itself.

A communication network can have many characteristics depending on its physical links, the capacity of buffer units in the network's centers, the routing strategy, and routing technique. NSP supports three levels of communication networks:

--the lowest level offers sequential delivery of messages from transmitter to receiver and vice versa for a two-point link and uses unnumbered logic links;

--the medium level offers sequential delivery of messages, uses numbered logic links and sequential confirmation of reception;

--the highest level offers delivery of messages between transmitting and receiving stations which are not sequential, uses numbered logic links and nonsequential confirmation of reception. It is used for systems with packet switching.

DAP Routine

The DAP routine is a procedure for the user stratum. It is made up by a format independent of the equipment and is designed for the exchange of data between sets and systems of input/output. It also makes it possible to meet the demands of a user program requesting services from a remote program on another computer.

Functions of the DAP routine:

--retrieval of set on input system,
--entry of set into output system,
--transmission of set between two centers,
--providing maintenance of sets (erasure, redesignation),
--transmission of data in various codes and formats,
--protection of sets against unauthorized users,
--remote control of input/output systems (e.g., rewinding of magnetic tape),
--control of horizontal and vertical format in various systems,
--checking errorless functioning of local and remote peripheries,
--providing for multiple transmission of control or data messages via a single logic link.

All messages of the DAP routine coincide in structure, which consists of identification data of DAP procedure, type of DAP message, channel number, length of message and the message itself.

Instructions from a user operating at this level of the routine are divided into three groups:

--basic instructions--generate communication routes and transmit data along them;

--instructions for sharing of sets--enable computers to transmit data to another computer or request them from another computer, from its set or input/output system controlled by another computer;

--instructions for control of program--enable one computer to start up or stop running programs on another system in the network.

Examples of instructions (data which follow instruction):

--CONNECT--establishment of connection (with someone),
--SEND--transmission of data (where),
--RECEIVE--reception of data (wherefrom),
--DISCONNECT--termination of connection (with someone),
--OPEN--opening of a set (where and which),
--GET--transfer of data into our buffer memory (wherefrom),
--PUT--transfer of data from our buffer memory (whereto),
--CLOSE--closing of set (which) and cancellation of link,
--DELETE--cancellation of set (which),
--RUN--start-up of program (which and where),
--ABORT--termination of a running program (which and where).

2.2.4 Software for Graphics

Software for the ISAP 1 interactive graphic system, described in the section on basic configurations in 16-bit systems, with the SM 4-20 minicomputer can be formed by:

--DOS RV V2 or FOBOS 1 operating system,
--SM GRAF set of graphic subprograms for operation of graphic vector monitor,
--GFS graphic functional software for operation of the DIGIGRAF drafting system,
--MINIG software,
--applicational software for a certain sphere of problems, e.g.:

- --ISAN 1 interactive system for design of printed circuits (sample design is shown in Figure 59),
- --system for planning apartment interiors,
- --system for structural design of parts of electric machinery,
- --system for design of distributors,
- --system for drafting cross and longitudinal sections and straight line design,
- --system for design of framed structures.

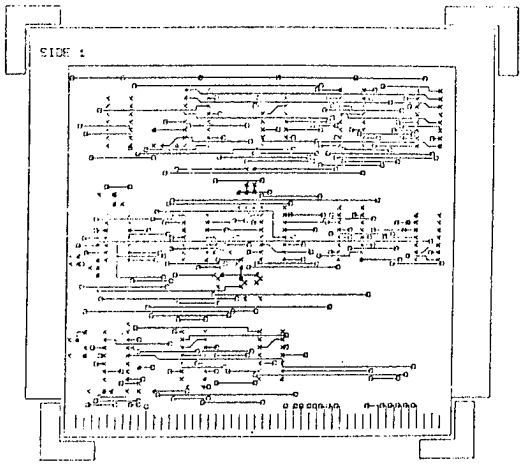


Figure 59. Printed circuit design (output from ISAN 1)

There follows a detailed description of basic parts of software, i.e.:

--SM GRAF,
--GFS,
--MINIG.

SM GRAF

SM GRAF is a set of programs for processing graphic information for the CM 7405 graphic terminal or the GVM 01 graphic monitor connected to computers of the SMEP series. From this set is formed a library of graphic subprograms that can be called by a program in FORTRAN. The library of graphic subprograms can be generated under the FOBOS or DOS RV V2 operating system.

Images are drawn by graphic programs on the screen of the terminal. The simplest graphic elements, the so-called atoms, are points, line segments and symbols. The location of atoms is usually relative to the immediate position of the beam, but it is also possible to image the so-called absolute point, the coordinates of which are absolute in relation to the screen.

Line segments can be imaged in four ways: solid line, line consisting of short or long dashes and a dot and dash line. All atoms can be imaged in eight brightness levels. All atoms can flash.

Symbols can be divided into two groups:

--routine set of symbols in code KOI 7, which has its printable image on the printer;

--a set of 31 special symbols, mathematical symbols, letters of the Greek alphabet, etc. Transition to this set of symbols is achieved by introducing the transfer code ahead of the normally printable symbols.

All symbols can be imaged normally or in italics.

Atoms can be combined into images, images can be arranged hierarchically. Images are marked by an index. An image with an index represents a figure. Figures can be used to perform operations such as cancellation, extinction, new imaging, insertion of atoms, cancellation of atoms, copying, etc.

A high degree of interaction with a graphic terminal is facilitated by a light pen, which can be used to select preprogrammed graphic operations. The light pen can also be used for modifying images. Input of graphic functions can also be performed from the keyboard.

The SM GRAF software can be used under the FOBOS operating system, in which case the graphic terminal operates as an independent system, or under the DOS RV V2 operating system, when the graphic terminal can operate either independently or as a satellite system of the host computers SM 4-20 or SM 52/11.

Some SM GRAF sets are written in FORTRAN IV and some in Macroassembler, so that libraries of graphic subprograms can be generated under the FOBOS as well as DOS RV V2 operating systems. FORTRAN IV or FORTRAN IV PLUS language compiler must be incorporated under the operating system.

GFS

GFS is general software providing for the operation of the digigraf graphic drafting system. GFS (graphic functional software) was developed in Office Machines for the JSEP I, JSEP II and ADT 4500 computers, and implementation for SMEP computers was carried out by Datasystem.

GFS represents a set of library subprograms, the major part of which is written in FORTRAN and part in Assembler.

The set of these subprograms can be divided into a group of organizational subprograms and a group of executive subprograms.

Organizational subprograms provide for:

--introductory initiation,
--selection of output,
--determination of the drawing's scale,
--rotation of axes of the system of coordinates,
--definition of the technological head,
--determination of the type of pen,
--selection of the type of line,
--marking of specified points by selected symbols,
--closing of the drafting set.

Executive subprograms provide for:

--connection of points by line segments,
--imaging of the drawing's boundary limits,
--imaging of a closed polygon,
--crosshatching of a closed n-polygon,
--imaging of axes, curves, circles, arcs, interpolation curves,
--imaging of text chains,
--marking points by selected markings, etc.

MINIG

MINIG is a set of programs intended for ISAP interactive graphic systems with the SM 4-20 computer. MINIG operates under control of the DOS RV V2 operating system and its concept is such that it is relatively independent of the graphic input and output systems employed. With the use of graphic output systems only, part of MINIG can be used for passive graphics; with the use of graphic and output systems (i.e., an extra graphic terminal or monitor equipped with a light pen), it is possible to implement interactive graphics. The characteristic feature of MINIG is the separation of the process of generating images from the process of their depiction.

MINIG makes it possible to:

--generate images in the form of data, the so-called sets of graphic instructions stored in general form on a disk not designed for a specific graphic output system;

--generate libraries of various graphic images (e.g., standardized structural elements, diagram markings) and their incorporation into higher combinations (drawings);

--use the once-generated images in a different scale, different position, etc.;

--draw images on various graphic systems;

--interactively operate with individual images;

--use passive graphics for individual graphic peripheral systems.

Figure 60 indicates the process of imaging in conventional passive graphics and Figure 61 shows the process of imaging by means of MINIG. While conventional passive graphics is characterized by direct control of graphic peripheries by means of the operating system, the MINIG program system always uses indirect output on graphic peripheries through service programs. This means that the generation of an image description in the form of a set of graphic instructions on disk memories occurs first, and then it is imaged by means of MINIG service programs on some graphic periphery.

Use of the graphic process in interactive graphics is shown in Figure 62.

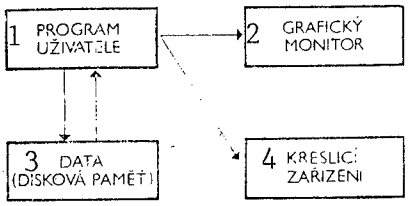


Figure 60. Conventional passive graphics

Key:
1. user program
2. graphic monitor
3. data (disk memory)
4. drafting system

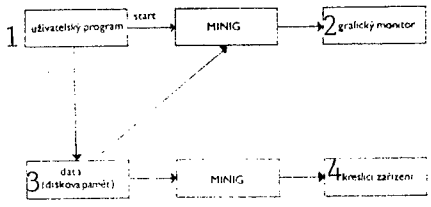


Figure 61. MINIG passive graphics

Key:
1. user program
2. graphic monitor
3. data (disk memory)
4. drafting system

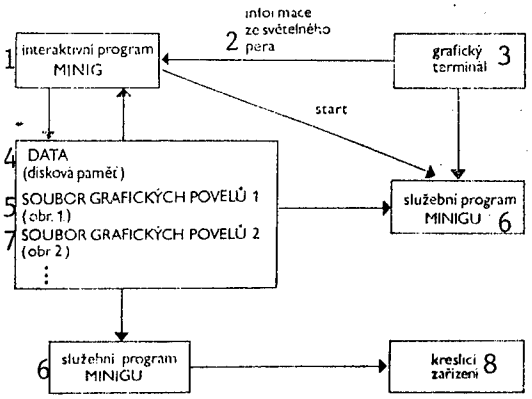


Figure 62. MINIG interactive graphics

Key:
1. MINIG interactive program
2. information from light pen
3. graphic terminal
4. data (disk memory)
5. set of graphic instructions 1 (image 1)
6. MINIG service program
7. set of graphic instructions 2 (image 2)
8. drafting system

In this arrangement the user program is replaced by a program for interactive graphic operation that uses a graphic monitor light pen. The MINIG service program serves for drafting as in passive graphics. After completion of graphic operations, the resultant images or sets of graphic instructions are stored in external memory and can be drafted by a drafting system.

MINIG consists of three main parts:

--system for image generation,
--library of graphic subprograms,
--service programs.

2.2.5 Programming Languages

The following text offers a more detailed description of the programming languages forming part of the operating systems of 16-bit SMEP computers:

--Macroassembler,
--BASIC,
--BASIC PLUS,
--BASIC PLUS 2,
--FORTRAN IV,
--FORTRAN IV PLUS,
--COBOL,
--FOCAL,
--MUMPS.

In addition to the described languages, preparations are being made for a PASCAL and ADA compiler.

Macroassembler

Macroassembler is an effective multipurpose basic programming tool. Macroassembler translates a source program in two runs.

Macroassembler translator is implemented in operating systems FOBOS 1 and FOBOS 2, DOS RV V2, DOS RVR.

The important features of this language are:

--control of program run and of Macroassembler language functions,
--specification of systems and titles of sets for input and output sets,
--printout of errors on a specified output system,
--alphabetically arranged format printout of a table of symbols,
--potential for generation of transferable modules,
--potential for using global symbols declared for connection of relative modules,
--instructions for conditional translation,
--instructions for dividing a program into sections,
--instructions for repetition of orders,
--macroinstructions defined by user,
--extensive amount of systemic macroinstructions,
--effective means for printout, e.g., printout of cross references.

Macroassembler facilitates the use of a library of macroinstructions. The system includes a library of systemic macroinstructions, and the user can generate his own library of user macroinstructions and combine both libraries for use.

Macroassembler incorporated under the DOS RV V2 operating system uses, moreover, certain expansions, e.g., an indirect set of instructions for control of the translation process or wider use of global symbols.

Macroassembler under the FOBOS operating system (MACRO translator) requires at least 12K bytes of internal memory. Macroassembler requiring 8K-word memory (ASEMBL translator) can be used with certain limitations.

In the DOS RVR operating system Macroassembler is incorporated under an optional translator of FORTRAN IV.

Under the DOS RV V2 operating system, Macroassembler requires a 14K-word memory; an 8K-word Macroassembler can be generated with certain limitations.

BASIC

BASIC is a conversation language for one user which can be learned with relative ease. It uses simple English words and abbreviations, known mathematical symbols, and thanks to fast response makes the generation, tuning and running of programs expedient.

The BASIC processor is designed as an incremental translator-interpreter which transforms source instructions of the language into a compact code and stores them directly in the memory. After issuing the instruction RUN, this internal code is interpreted and processed as a program. By using the instruction LIST or SAVE, this internal code can be translated back into the original symbol format. The source program can be processed either by instructions, whereby each instruction is immediately carried out, or as a whole. Direct processing by instructions is used for the tuning and generation of programs, and the computer can be used in this manner as a calculator.

BASIC processes two types of sets: sequential and virtual. Sequential sets are symbol sets of chains of symbols or numerical data approached sequentially. Virtual sets behave as ordinary fields, and consist of chains of symbols or numerical elements; access to them occurs by means of indices. Then the virtual set behaves as if it were residential in the memory.

For connection with special functions or functions generated by the user there is the instruction CALL, which makes it possible to call up a function by means of a name and transfer of arguments. Functions can be generated as subprograms, which the user enters in Macroassembler. There is also a set of functions for processing graphic tasks that can be called up by means of the instruction CALL.

The BASIC language is implemented under the following operating systems:

--LOS,
--FOBOS 1,
--FOBOS 2,
--DOS RV V2,
--MOS RV V2.

A description of the multiuser BASIC language, the so-called VU BASIC, which forms an independent program system, was presented in the preceding section.

BASIC PLUS

The BASIC PLUS language is a superstructure of the basic BASIC language. In comparison to BASIC, it considerably expands the possibilities for all-round application, particularly in the area of data processing. In it are introduced modifiers conditioning the implementation of instructions; new instructions and many instructions are expanded.

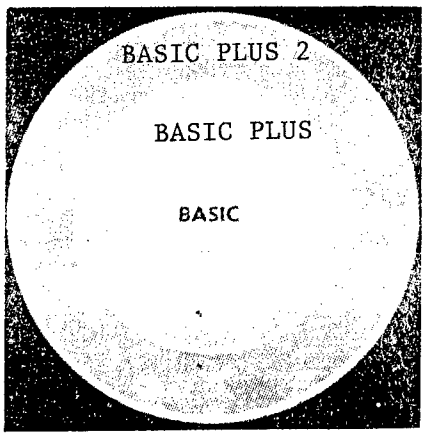


Figure 63. BASIC type languages

BASIC PLUS permits the processing of chains of symbols and data with a fixed decimal point. In addition to processing input and output data piece by piece, it is also possible to process by entries. Another difference in comparison to BASIC is the reinforcement of the conversational nature of the language.

BASIC PLUS makes it possible to use algebraic functions for addition, subtraction, multiplication, transposition and inversion of matrices, operators of Boolean functions.

BASIC PLUS is the basic programming language in the DOS RVR 1 operating system. Some control instructions of BASIC PLUS serve at the same time as systemic instructions of this operating system.

BASIC PLUS 2

BASIC PLUS 2 is the fundamental BASIC or BASIC PLUS with expanded potential for processing of chains, i.e., alphabetical data, and the possibility for processing of data sets within the capabilities of the RSZ system.

BASIC PLUS 2 implemented under the DOS RV V2 operating system includes expansions in the following areas:

--virtual field,
--sets of input/output entries,
--operation with chains,
--operation with matrices,
--variables with long identifiers,
--structure IF ... THEN ... ELSE,
--program for processing of errors,
--modification of instructions,
--functions defined by the user,
--multiple instruction lines,
--multiple line instructions.

The compiler of the BASIC PLUS 2 language under the DOS RV V2 operating system requires for its operation the RSZ system, in the area of hardware a processor with a floating decimal point and in internal memory a user sector with a minimum capacity of 24K words.

FORTRAN IV and FORTRAN IV PLUS

The FORTRAN programming language is intended primarily for the solution of scientific, technical, mathematical and economic calculations. In processing sets with a simple structure, it can also be used for the solution of some simpler problems on the boundary of mass data processing and scientific and technical calculations.

The FORTRAN language is based on the standard ANSI X 3.9-1966 and is available in two variants:

--FORTRAN IV, incorporated into most SMEP operating systems;
--FORTRAN IV PLUS, which is an expanded version of the preceding language and is incorporated only under the DOS RV V2 operating system.

User programs written in FORTRAN IV can be processed without modification by the FORTRAN IV PLUS compiler. Compilers of both variants of the language are of the optimizing type, whereby the FORTRAN IV PLUS compiler carries out a considerably larger measure of optimization.

In addition to compilers, the FORTRAN IV system includes a library of standard subprograms in FORTRAN and a library of service programs.

In comparison to the standard ANSI, FORTRAN IV includes many significant expansions, particularly:

--index expressions can contain a random arithmetic expression;

--fields can have up to seven dimensions;

--instead of Hollerith constants, apostrophic chains can be used in the FORMAT instruction;

--in description DATA it is possible to use both Hollerith and apostrophic literals;

--it is admissible to use mixed expressions, including complex and byte;

--each instruction can contain a commentary separated from the instruction by an exclamation point;

--instructions marked by the letter D in the first column are carried out only during sorting; otherwise they are considered to be comments;

--the instructions READ and WRITE can contain the parameter END=, signalling a jump in the program when the end of a set is identified; in addition, they can contain the parameter ERR=, signalling a jump in the program when an error is identified during data input/output;

--in the output list of instructions WRITE, TYPE and PRINT, any expression can figure as an element;

--random expressions can appear in parameters of the cycle DO and the switch GO TO;

--step value in instructions of the cycle DO can be negative;

--in the switch aligned to GO TO a list of signals can be omitted;

--input and output data can use a random format;

--input/output instructions have been expanded by additional instructions;

--logic operations, operation with bits and masking can be performed on integers;

--the specifying instructions LOGICAL 1 or BYTE make it possible to store small integers and symbol data with maximum economy of memory; this makes it possible to mask and arithmetically process symbol data;

--the specification IMPLICIT makes it possible to redefine implicit types of variables, etc.

The FORTRAN IV language is implemented under the following operation systems:

--FOBOS 1,
--FOBOS 2,
--DOS RV V2,
--DOS RVR.

The second variant, FORTRAN IV PLUS, contains the following expansions in comparison to FORTRAN IV:

--the instruction ENTRY, which can be used in subprograms and functions for determining multiple input points;

--the instruction PARAMETR, intended for defining symbolic names for constants;

--defining of lower and upper limits of fields that can be entered during declaration of fields; the lower limit can be negative, zero or positive;

--data of the type INTEGER*4, with 31 accuracy bits, and data of the type INTEGER*2, whereby both types of data can be used in the same program;

--declaration of INTEGER-type logical and data without explicit specification of length;

--expanded possibilities for use of instructions READ and WRITE;

--the instruction INCLUDE, which incorporates source text in FORTRAN IV from another set into program in FORTRAN IV PLUS.

Thus, the key differences between the compilers of both variants consist in the fact that FORTRAN IV PLUS

--offers expanded potential,
--generates a highly optimized code,
--requires a processor with a floating decimal point.

A program translated by the FORTRAN IV PLUS compiler performs typical scientific and technical calculations two to three times faster than a program translated by the FORTRAN IV compiler with the same hardware configuration.

The FORTRAN IV PLUS compiler is implemented under the DOS RV V2 operating system.

COBOL

The COBOL programming language implemented under the DOS RV V2 operating system is a subset of the full specification of the COBOL language and corresponds to the Standard ANSI X 3.23-1974.

It contains all standard instructions required for operation with data sets which can be sequential, relative and index-type (with which a COBOL program

operates via RSZ), and instructions for operation with elementary data items and operation with chains are also implemented.

COBOL of the SMEP system does not contain an internal sorting instruction, nor the instruction ENTER. These functions are provided by the sorting program SORT and potential combination of target-oriented programs via the service program MERGE and connecting program TKB. However, the sorting of entire recordings cannot be performed by the user directly in his COBOL program via a library.

Programs in COBOL can be combined with programs written separately in Macro-assembler, FORTRAN IV, FORTRAN IV PLUS and BASIC PLUS 2. The COBOL compiler in the DOS RV V2 system also includes three service programs:

--program for generation of input configurations, which generates a COBOL program from a specified set;

--program for changing the format of the source program into punch card format;

--program for generation of a full set of overlap MERGE.

The COBOL program also requires for its operation under the DOS RV V2 operating system the RSZ system, and places relatively high demands on the size of a computer's internal memory and on operating space on disk media for operating sets (during translation the compiler requires up to 512 free operating blocks).

The COBOL programming language is also implemented under the FOBOS 2 operating system. This compiler provides these additional functions:

--REPGEN for printouts,
--REFORM formatting program,
--COSORT sorting program.

FOCAL

The FOCAL programming language is used for various computations in real time, e.g., for numerical mathematics, statistical analysis. FOCAL is an interpreter that facilitates operation in interactive dialogue mode or in program mode. It provides for the processing of input analog quantities, and discrete input/output quantities, and facilitates cooperation with graphic peripheries or measuring systems.

FOCAL is implemented under the FOBOS operating system and requires an 8K-byte memory. This programming language has not found wide application and is usually replaced by BASIC.

MUMPS

MUMPS is a special language intended exclusively for work with the DIAMS operating system. It is suited for work with text chains and is similar to BASIC; just as BASIC does, it operates on the interpretive principle.

However, in comparison to BASIC, MUMPS is more efficient and affords faster access to data. Programs in MUMPS are substantially shorter than in BASIC.

2.2.6 Testing Monitors

TMOS 1

TMOS 1 is a testing operating system for SMEP computers. It includes a set of diagnostic programs for SMEP hardware and is used exclusively for testing and diagnostic purposes.

TMOS consists of two basic parts: service programs, including a monitor, and a set of testing programs.

The testing operating system in the basic variant designated TMOS is supplied automatically with deliveries of computer systems.

TMOS 2

TMOS 2 is a newly prepared variant of the testing operating system and, in comparison to the TMOS 1 version, also contains interaction tests.

3. Imported 16-bit Systems

Among the 16-bit systems imported into the CSSR belong the following minicomputers:

--SM 4-10,
--INDEPENDENT 1-100.

3.1 SM 4-10 Minicomputer

Users in the CSSR were provided in 1978 with the first so-called basic configuration of Soviet-made 16-bit SM 3-10 computers with 32K-word ferrite memory, which were followed in 1979 by deliveries of the follow-up type SM 4-10 minicomputer with 128K-word memory.

In the developmental series of processors of SMEP minicomputers the domestic SM 3-20 and SM 4-20 constitute a developmentally higher level than that of the SM 3-10 and SM 4-10 systems. For example, with regard to the structural differences of these computers, in a comparison of the processors from the viewpoint of plates and volume the ratio is approximately 1:4.

An advantage offered by the SM 4-10 systems is their peripheral equipment. It can be said that the "interesting" hardware (tape memory, multiplex, disk memory 29 MB) appeared in import deliveries on an average a year earlier than from domestic production.

The set of instructions of the processor of the SM 4-10 minicomputer includes:

--basic set of SMEP instructions,
--expansion set of instructions.

The SM 4-10 does not have a special processor of a floating decimal point and, thus, it does not have a set of instructions for a floating decimal point (as does the SM 4-20).

To provide an idea of the speed of comparable computers, Tables 4 and 5 present a comparison of speed according to the MM 019-78 test. This methodology specifies a different type of computation for the SM 3- and SM 4-type computers, thus the differences between the two tables are small.

Table 4. Comparison of the speed of SM 3-type computers

Type of computer	Number of operations/s
PDP 11/04	129,000
PDP 11/05	116,000
SM 3-10	100,000
SM 3-20	124,000

Table 5. Comparison of the speed of SM 4-type computers

Type of computer	Number of operations/s
PDP 11/34	130,000
PDP 11/40	165,000
SM 4/10	145,000
SM 4/20	148,000

The SM 4-10 minicomputer comes with the multiprogram OS RV operating system, second version, comparable to the domestic DOS RV V2 operating system. With this operating system it is possible to obtain modules for mass data processing:

--FOBRIN variation of DTS (see chapter on "Software"),
--SORT,
--COBOL compiler, etc.

A complete set of hardware and programmer documentation in Russian is supplied with the SM 4-10.

3.2 INDEPENDENT 1-100 Minicomputer

Office Machines has been marketing the INDEPENDENT 1-100 minicomputer from Romania in the CSSR since 1982.

The processor of this computer underwent international SMEP tests in 1978 and was included in that program under the designation CM 2402. Peripheral units supplied with this system are in most cases products made under license which are not included in SMEP nomenclature.

The processor of this minicomputer is comparable to the processor of the SM 4-10 computer or to the CM 2401 processor of the SM 4-20 computer, with the proviso that the CM 2401 is technologically on a higher level and has an additional processor of floating decimal point.

Preparations are being made to replace imports of the I-100 computer by the I-102F computer, the processor of which is comparable to the CM 1403 processor of the SM 52/11 minicomputer.

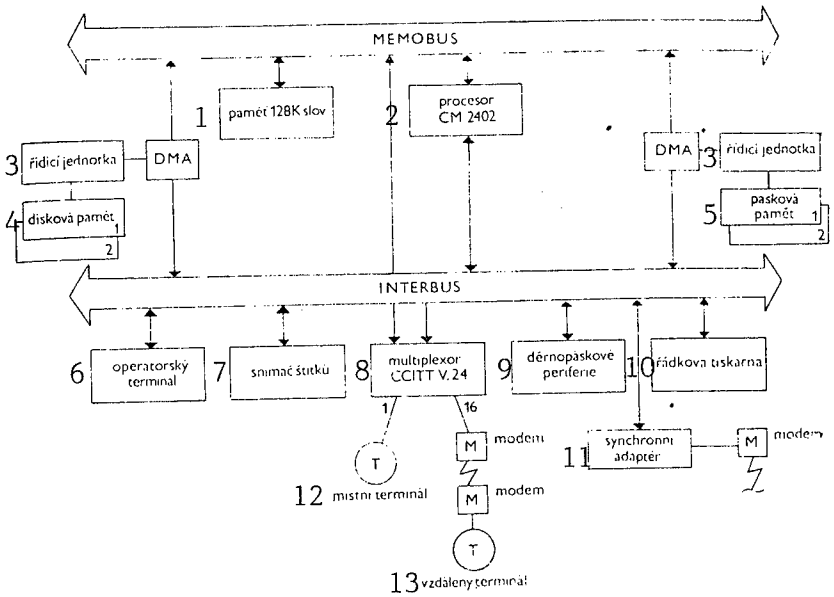
Minicomputer's Characteristics

The INDEPENDENT I-100 is an all-purpose word-oriented 16-bit computer with wide areas of application. Thanks to the flexibility and modular concept of its high-performance hardware (large-capacity disk memory, tape memory with large reels, line printer, multiplex) and software, it can be applied in areas such as:

--scientific and technical applications,
--mass data processing,
--statistical computations,
--applications in real time,
--control of technological processes,
--remote data processing,
--formation of computer and terminal networks.

The I-100 is technologically based on TTL (SSI and MSI) logic integrated circuits and MOS-LSI on 4-layer printed circuits.

The basic layout of the system is shown in Figure 64.



Key:
1. 128K-word memory
2. EM 2402 processor
3. control unit
4. disk memory
5. tape memory
6. operator's terminal
7. punch card reader
8. CCITT V.24 multiplex
9. perforated tape periphery
10. line printer
11. synchronous adapter
12. local terminal
13. remote terminal

Figure 64. Wiring of the INDEPENDENT I-100 minicomputer

CM 2402 Processor

The CM 2402 processor, consisting of a control unit, an arithmetic-logic unit, memory organizer, microprogram memory and emulator of instructions, interconnects two systemic busbars INTERBUS and MEMOBUS.

INTERBUS is the computer's internal busbar, which provides for dialogue between the basic unit and individual peripheral systems.

MEMOBUS is a simplified version of INTERBUS, using the same operating code. It provides connection between the basic unit and memory and, further, between memory and the systems for direct access into DMA memory, which can be, e.g., a disk memory or a tape memory. The basic unit organizes the exchange of information in the system and, further, performs a set of system-internal instructions. This internal set of instructions is processed with the aid of microprogram memory of 2K-word capacity and a decoding emulator of instructions so that the set of the computer's instructions is identical to the set of instructions of computers of the SMEP series.

The block of expanded addressing makes it possible to address a memory of up to 128K words. It also administers protected pages of memory, their control, dynamic placement in memory, etc.

The DMA system for direct access to memory facilitates the direct transmission of data between the internal memory and the requisite system without the participation of the processor. As soon as the central processor receives through INTERBUS the requisite information for DMA data transmission, logic disconnection of DMA from INTERBUS transfers control of data transmission between peripheral systems and memory to MEMOBUS.

The total capacity of its internal semiconductor memory is 128K words. It is formed by four blocks with 32K words each.

Its programmable real time clock generates time pulses with frequencies of 50 Hz, 10 kHz and 100 kHz.

The system's operator terminal is addressed as a normal periphery. The operator can control the operation of the processor, address the main memory or the expanded microprogram memory, the system's registers, registers of the state of programs, etc. The terminal is formed by a dot printer with keyboard, control unit and a clock.

Other systemic properties of this processor are identical with processors of this series, e.g., those of SM 4-10, SM 4-20.

Aside from floating decimal point instructions, the basic instructional set of the I-100 computer coincides with that of the SM 4-10 and SM 4-20 computer. However, the difference is in instructions for the floating decimal point. The SM 4-10 and I-100 systems have a set of basic emulated instructions for the floating decimal point that corresponds to the set of instructions of the domestic SM 50/50 microcomputer with 128K-word memory. On the other

hand, the SM 4-20 minicomputer, equipped with a special floating decimal point processor, facilitates hardware-performed performance of arithmetic and logic operations using arithmetic in the floating decimal point. These operations, when needed, must be carried out in the I-100 or SM 4-10 systems by the program.

Tape Memory

This system consists of a unit for direct access to memory, a control unit which makes it possible to connect up to four magnetic tape units and two memory units (see Figure 65).

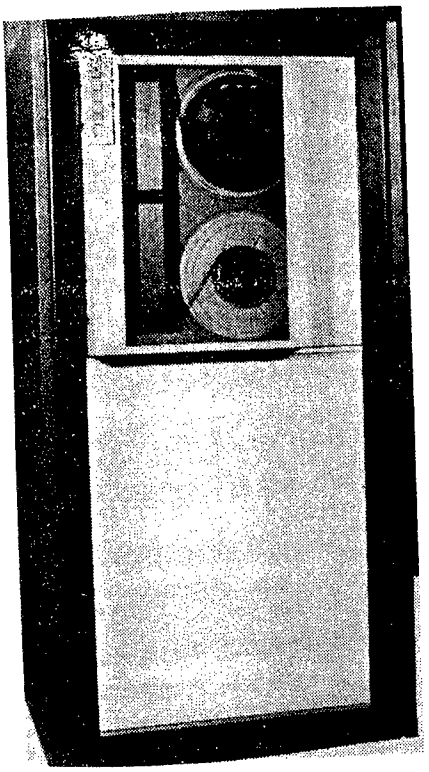


Figure 65. Casing with tape memory

Technical specifications:

type of tape	standard 9 track
recording density	switchable 800/1600 bpi
tape length	max. 2400 ft
reading speed	37.5 ips
type of recording	PE for 1600 bpi density NRZI for 800 bpi density
transmission speed	30 or 60 KB/s
power feed	220 V/50 Hz
power input	1500 VA

RCD 9742 Large-Capacity Disk Memory (Figure 66)

This system consists of a unit for direct access to memory, a control unit making it possible to connect a maximum of four disk memory units with a capacity of 58 MB each. A part of the subsystem consists of two disk memory units.

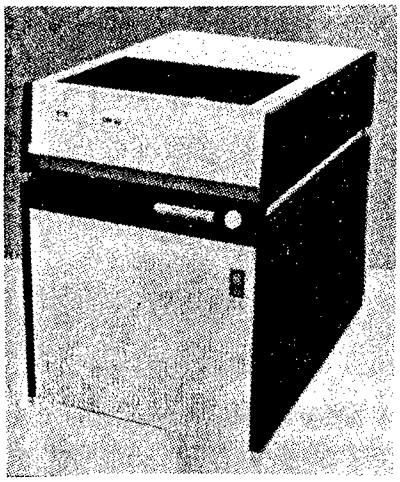


Figure 66. RCD 9742 disk memory with 58 M byte

Technical specifications:

number of sectors	12
transmission speed	312 KB/s
speed of disk rotation	2400 rps
average access time	37 ms
average retrieval time	10 ms
total capacity	58 MB formatted capacity
dimensions	698x953x711 mm
weight	280 kg
power feed/power input	220 V/max. 380 VA

CDC 9226 Card Reader

It consists of a reader of standard 80-column cards with the requisite control unit (see Figure 67).

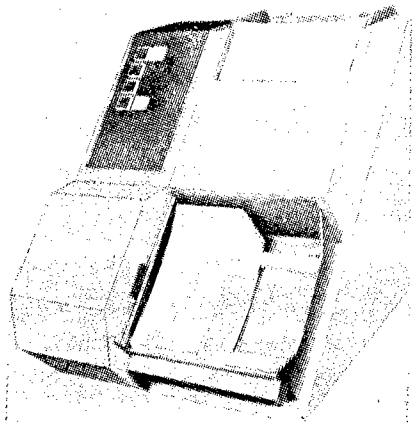


Figure 67. CDC 9226 card reader

Technical specifications:

reading speed	600 cards/min
type of reading	photoelectric
capacity of input/output	1000/1000 cards
card feeder	440x360x540 mm
dimensions	25 kg
weight	220 V/250 VA
power feed/power input	

Punch Card Reader/Puncher Module

It consists of a punch card reader/puncher with a control unit.

Technical specifications:

carrier medium	8-track paper punch card
reading speed	300 symbols/s
punching speed	75 symbols/s
power feed/power input	220 V/300 VA

RCD 9389 Line Printer

The RCD 9389 line printer (Figure 68) operates on the principle of the symbol band. The line printer configuration includes a control unit.

Figure 68. RCD 9389 line printer

Technical specifications:

printing speed	900 lines/min
number of symbols per line	132
set of symbols	64 standard ASCII symbols
number of copies	1 to 6

line density	6 to 8 lines/inch
density of print in line	10 symbols/inch
dimensions	863x876x1220 mm
weight	159 kg
power feed/power input	220 V/1400 VA

Asynchronous Adapter

This is a serial asynchronous single-line adapter for connection with an asynchronous system, e.g., a terminal or a computer, either through a modem at unlimited distance or in local mode through a current loop up to 500 m long.

Technical specifications:

transmission speed	50 to 9600 bit/sec
symbol format	5 to 8 bits
length of stop bit	1; 1.5; 2 bits
interface	CCITT V.24 IRPS current loop
transmission protection	parity or without parity
type of transmission	full or half duplex

Asynchronous Multiplex

This is a system with DMA direct access into memory for connecting a maximum of 16 lines. Its output is in interruption mode after symbol. Separate timing is generated separately for each line from a common crystal oscillator, which makes it possible to select the speed of each line by the program. Two FIFO-type 64-symbol buffer memories serve for data recording.

Technical specifications:

transmission speed	50 to 9600 bit/s
symbol format	5 to 8 bit
stop bit length	1 or 1.5 bit for 5-bit symbol 1 or 2 bits for 6 to 8-bit symbol
interface	CCITT V.24
transmission control	parity or without parity

Synchronous Adapter

This single-line series synchronous adapter provides linkage between the computer proper and a serial synchronous line. It is suited for providing linkage with another synchronous system, e.g., a remote concentrator, another SMEP or JSEP computer with the proper procedure.

Technical specifications:

transmission speed	600 to 9600 bit/sec
transmission procedure	SDLC, HDLC BSC, DDCMP
type of transmission	full or half duplex
interface	CCITT V.24 with full modem control

DAF 2010 Display Terminal

It is connected to the I-100 minicomputer via an asynchronous multiplex or via a synchronous adapter (see Figure 69).

Technical specifications:

screen capacity	1920 symbols (24x80)
symbol imaging	5x7 point matrix
imagining modes	normal (white symbols on dark backgr.) inverse (dark symbols on white backgr.)
number of displayable symbols	96 standard ASCII
number of keys	101 in three fields: functional, numerical and alphanumeric
interface	CCITT V.24
max. connection distance	unlimited long-distance via modem, local under worst interference conditions 15 m
potential for printer connection (hard copy)	via CCITT V.24 interface
operating mode	symbol, line, page

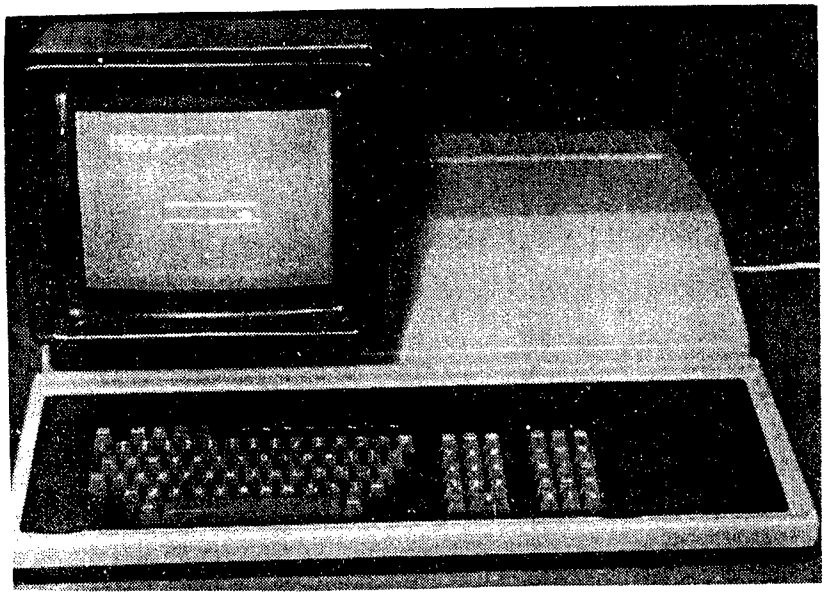


Figure 69. DAF 2010 display terminal

The display terminal can operate with punctuation marks, symbols for tabulation and control symbols. With the aid of the requisite hardware it can be used for some semigraphic functions.

Centronix Terminal With Printer

This serial asynchronous terminal with printer operates on the principle of a dot printer with keyboard. This terminal can be used as an operator terminal of the I-100 computer.

Technical specifications:

printing speed	60 symbols/s
number of symbols per line	132
set of symbols	64 standard ASCII symbols
type of control	microprogram
interface	IRPS - current loop CCITT V.24
max. connecting distance	up to 500 m via current loop, via CCITT V.24 same as DAF 2010

Basic configuration of I-100 hardware:

--basic unit including:

   --CM 2402 processor,
   --control panel,
   --expansion module,
   --power supply control,
   --real time clock,
   --microprogram PROM memory of 2K-word capacity,
   --RAM memory block of 32K words,
   --RAM expansion memory block 32K (3 units),
--operator's terminal with control unit,
--card reader with control unit,
--line printer with control unit,
--perforated tape reader/puncher with control unit,
--disk memory subsystem 58 MB
  (control unit + 58 MB disk unit + 1 disk bundle),
--expansion disk unit 58 MB + 1 disk bundle,
--DMA unit for tape memory,
--subsystem tape memory 800/1600 bpi, control unit + 1 memory unit + medium,
--expansion tape unit 800/1600 bpi including medium,
--DAF 2010 display terminal with cables for local and remote connection (10 pcs),
--asynchronous multiplex for 16 lines CCITT V.24,
--synchronous adapter,
--desk, casings, power sources, accessories, expendables.

Software

With the I-100 computer comes a set of software products bearing the designation MININET/MINOS V.1.0, comprised of the following items:

--MINOS V.2.1 operating system similar to out DOS RV V2 operating system;
--MININET software facilitating the formation of terminal and computer networks in simple as well as in extensive configurations, analogous to SYRPOS 1;

--translators, interpreters, service programs and libraries:

--Macroassembler,
--FORTRAN IV,
--COBOL,
--BASIC,
--SORT,
--library of programs for mathematical computations,
--MINOS/TEST residential operating system for testing hardware.

The MINOS operating system facilitates operation of the following translators:

--FORTRAN IV. V. 2. 52,
--FORTRAN IV PLUS V.3.0,
--COBOL V.4.1, including SORT V.2.0 and RMS-11K V. 1. 8,
--BASIC PLUS 2,
--PASCAL.

Ducumentation

With the INDEPENDENT system comes a set of technical and programmer documentation numbering 50 volumes, both sets in English.

4. 8-Bit Systems

Eight-bit SMEP microcomputers are supplied in the CSSR under the basic designation SM 50/40-1. The assembly of SM 50/40 microcomputer modules is based on a single plate microcomputer built on the basis of the MHB 8080 microprocessor, and contains a whole series of additional modules. Individual variants of 8-bit microcomputers, including software, are described in the subsequent text.

The 8-bit microcomputer system can find application in many areas of the national economy, e.g.:

--mechanical engineering--control of machinery, conveyer belts, control of rolling mill lines, automatic dosing machines;

--commerce--automatic dispensing machines, scales, cash registers, systems for data input using sensors with a decimal point code;

--transportation--control of transportation systems, intersections, trackage, autoblocks, dashboard systems;

--administration--systems for processing of text information, multikeyboard data acquisition systems, office computers;

--health care--automated analyzers, monitoring of patients in intensive care units;

--computer technology--desktop computers with distributed intelligence, local networks, programmable terminals.

4.1 Hardware

Hardware of microcomputer systems based on the SM 50/40 modular assembly can be divided into four basic categories:

--SM 50/40 cassette assembly, consisting of individual modules including the single-plate microcomputer itself, structural elements and power sources. From these components and software for operation in real time it is possible to generate variants for the control of machinery, control of processes, control of systems, i.e., variants for building into final products of another manufacturer, sometimes also referred to as OEM variants (see Figure 70).

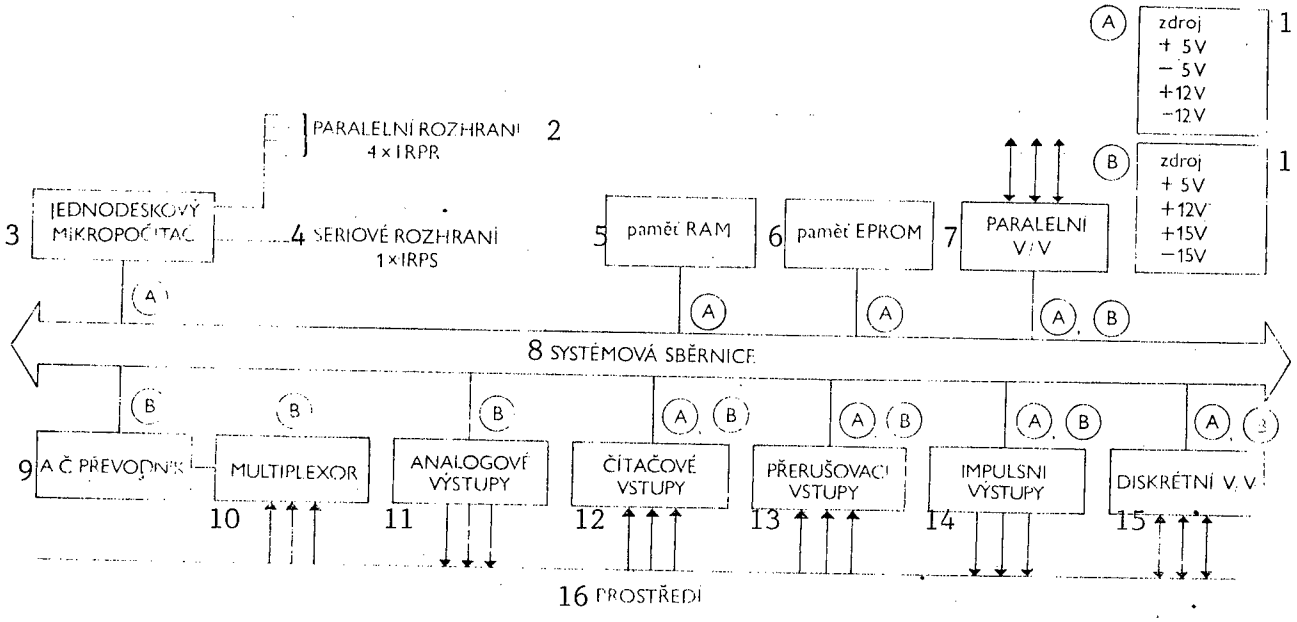


Figure 70. SMH 50/40 cassette wiring

Key:

1. power source
2. parallel interface
3. single-plate microcomputer
4. serial interface
5. RAM memory
6. EPROM memory
7. parallel input/outputs
8. systemic busbar
9. analog/digital converter
10. multiplex
11. analog outputs
12. counter inputs
13. disconnecting inputs
14. pulse outputs
15. discrete inputs/outputs
16. environment

--Developmental systems for the generation of software for microcomputer systems based on the SM 50/40 modular assembly (see Figure 71).

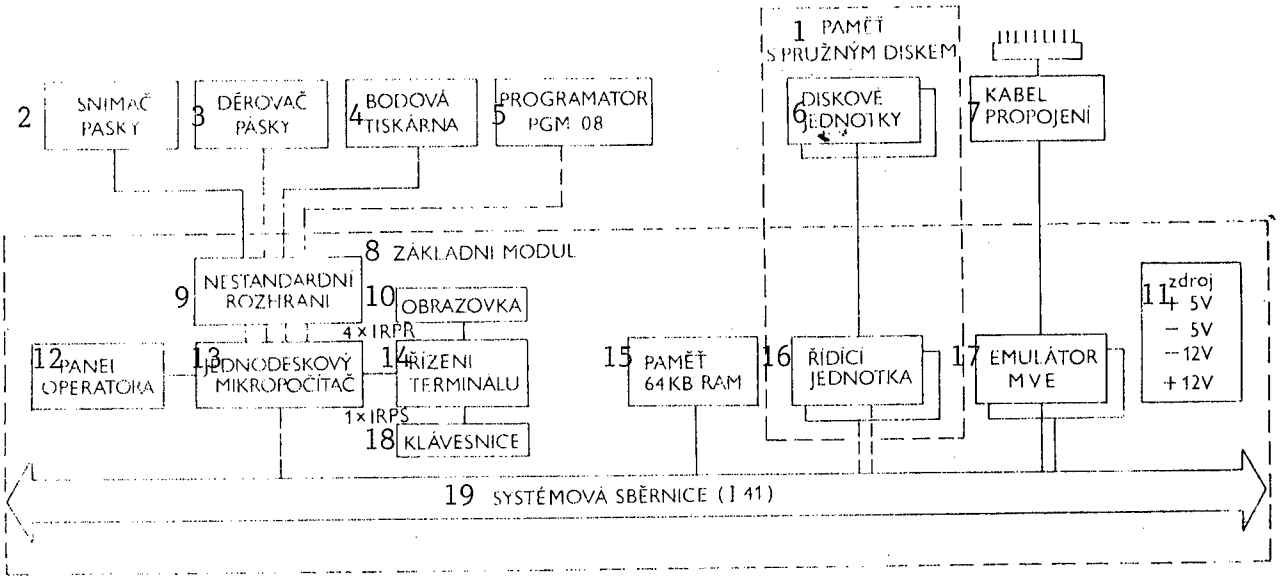


Figure 71. MVS developmental system layout

Key:

1. floppy disk memory
2. tape reader
3. tape perforator
4. dot printer
5. PGM 08 programmer
6. disk units
7. interconnecting cable
8. basic module
9. nonstandard interface
10. screen
11. power source
12. operator's panel
13. single-plate microcomputer
14. terminal control
15. 64 KB RAM memory
16. control unit
17. MVE emulator
18. keyboard
19. systemic busbar

--SM 50/40 microcomputers which are conceptually based on the SM 50/50 modular assembly, their configuration sharing many common features with, e.g., developmental systems, but basic and applicational software and the area of application are different. This involves the category known as desktop and personal computers, office computers, programmable terminals, etc.

--SM 53/10 and SM 53/20 distributed systems are based on the SM 50/40 modular assembly; in cooperation with terminals for contact with the environment and terminals of process operators, it facilitates the monitoring or control of complex technological processes.

--The VUVT training microcomputer constitutes in its own way a different, yet no less important independent category. It is designed for teaching computer technology, for hobby activities, for polytechnical training. A part of the

microcomputer is formed by a set of additive systems--training aids suitably and methodically selected to permit experimentation in various areas--measuring, regulation and, in discrete control, writing, tuning and start-up of programs, etc.

The application of this aid is enhanced by a handbook which contains instructions, descriptions and examples intended for beginning as well as advanced students of computer technology.

4.1.1 SM 50/40 Cassette

The SM 50/40 cassette represents a complex of hardware and software. The hardware is formed by a system of plates-modules, containing a single-plate microcomputer, expansion memories, input/output units, control units for peripheral equipment, structural elements and power sources. The plates can be used to devise in modular fashion single-computer (in the simplest case single-plate) or multicomputer microprocessor systems of the most varied configurations.

The basis of this modular assembly is formed by a single-plate microcomputer designed on the basis of the MHB 8080 microprocessor. It facilitates systemic operation in a mode with several processors, the so-called MULTIMASTER mode. Another module, a mathematical module, operates in parallel with the control processor and speeds up arithmetic computations.

Other expansion modules of this modular assembly make it possible to expand systemic ROM and RAM memories, expand the number of digital inputs and outputs, the connection of analog inputs and outputs and connection of peripheral equipment.

The key application of independent cassettes is envisioned as OEM products, meaning that these systems will form a part of systems manufactured by other final producers.

From the structural viewpoint the design of all plates is identical, with dimensions of the so-called 2/3 SMEP plates. The plates have two layers and measure 280x240 mm.

On the inner side of the plate, i.e., toward the interior of the cassette into which it is inserted, there are two direct 96-contact ELTRA 803 or TE Jihlava connectors, by which the modules are connected to the systemic busbar of the SM 50/40 system, along which occur all communications among individual modules.

The busbar is precisely defined from the functional, electric and structural viewpoints and all systems connected to it strictly comply with these principles. This busbar is functionally and electrically compatible with the MULTIBUS busbar.

On the opposite side of the plate are connectors serving to connect external environmental media (also with the aid of a ranging box) or peripheral units.

Some plates make possible applications of various types, thanks to exchangeable memory elements and other modifications that can be selected by the program and various interconnections.

The SM 50/40 modular assembly is an open system which will be gradually supplemented by additional modules. Development and documentation completed by the end of 1982 includes the following modules:

SM 2138 Single-Plate Microcomputer

Memories:

--SM 0440 dynamic RAM memory 16K byte,
--SM 0441 RAM CMOS 16K byte memory with backup,
--SM 0442 combined 64K byte RAM and 16K byte EPROM memory,
--SM 0449 EPROM memory 16K byte;

Input/output units:

--SM 1350 multiplex of low-level analog signals,
--SM 1352 analog digital converter,
--SM 1353 9-bit analog outputs,
--SM 1354 12-bit analog outputs,
--SM 1355 48 discrete inputs/outputs,
--SM 1356 counter pulse inputs for 16 lines,
--SM 1357 disconnecting inputs,
--SM 1358 pulse outputs,
--SM 1360 multiplex of high-level analog signals,
--SM 2170 mathematicl module,
--SM 2165 parallel input/output-72 TTL lines;

Control units of peripheral systems:

--SM 2150 4 series asynchronous channels,
--SM 2151 + SM 2154 control unit for floppy disk memory,
--SM 2143 + SM 2158 module of nonstandard parallel interfaces;

Power supply sources:

Source A--voltage ±5 V, ± 12 V,
Source B--voltage + 5 V, + 12 V, ± 15 V,
Source C--voltage ± 5 V, + 12 V,
Source D--voltage + 5 V, ± 12 V, + 18 V;

Structural elements:

--cassette
--ranging box.

There follows a detailed description of the individual modules of the SM 50/40 modular assembly.

4.1.2 SM 2138 Single-Plate Microcomputer

This single-plate microcomputer is the basic module of SM 50/40. It contains the following functional blocks:

--its own 8-bit parallel processor based on MHB 8080 facilitating the addressing of up to 64KB memory,
--block for ccntrol of systemic busbar I 41,
--block of 2 KB static RMA memory,
--block of 4KB EPROM memory,
--block of IRPS serial interface or S2 for one peripheral unit,
--block of parallel interface (48 TTL lines) for 4 input/output units, IRPR interface,
--block of program timer,
--block of disconnection control.

The MHB 8080 microprocessor has at its disposal 76 basic instructions 1, 2 or 3 bytes long facilitating 3 ways of addressing the operand. The set of instructions is divided into transmission, arithemtic, logic, branching instructions and, finally, instructions in storage, input/output and control. The time for performance of one instruction ranges between 2 to 8.5 μs (with clock frequency 2 MHz).

Individual SM 50/40-1 modules are mutually interconnected by a systemic busbar (I 41) which is compatible with the busbar of the SBC 80/20 microcomputer. It is formed by a set of lines which are divided according to function into:

--16 one-way address lines,
--8 two-way data lines,
--8 disconnecting level lines,
--14 control signal lines,
--auxiliary signal lines,
--reserve lines.

The lines are physically located in two 96-contact connectors K1 and K2. Through the main connector K2 run address lines, data lines, disconnecting signal lines and control signal lines. Through the auxiliary K1 connector run power feed lines and auxiliary signal lines.

This busbar facilitates the cooperation of individual modules in the mode MASTER-SLAVE. The control module MASTER excites address lines and control signal lines and controls contact on systemic busbar. The subordinate SLAVE module cannot control the systemic busbar.

The number of simultaneously connected control modules is limited to three. The basic priority disconnecting system is eight-level, vectored and programmable.

The terminal version of the SM 2138T microcomputer does not use a programmable disconnection control unit.

Technical specifications:

data busbar	8 bits
address busbar	16 bits
max. addressable memory capacity	64K byte
data format	8 bits
number of basic instructions	78
speed of instruction performance	2 to 8.5 µs
residential RAM memory capacity	2K byte
residential EPROM memory capacity	4K byte
number of disconnecting levels	8
interface	systemic busbar (I 41)
potential connection of IRPR peripheries	4 data channels
of IRPS or S2 (V.24 CCITT) peripheries	1 data channel
max. number of connectable inputs/outputs	256
input and output signal level	TTL, V.24, current loop, 20 mA - IRPS
max. external dimensions	295x245x15 mm
weight	max. 1 kg
feed voltage/max. consumption	+ 5 V/4.7 A + 12 V/0.3 A - 5 V/0.2 A - 12 V/0.2 A
feed voltage tolerance	± 4 percent

4.1.3 Memories

SM 0440 Dynamic 16K Byte RAM Memory

The SM 0440 independent functional block contains a semiconductor memory suited for use as the basic working memory storage of systems based on the SM 50/40 modular assembly. The plate can be addressed through internal couplers in capacity ranges of 0-16K, 16K-32K, 32K-48K, 48K-64K, and in this manner it is possible to build a memory of up to 64 KB capacity from SM 0440 modules.

Contact with other modules of the SM 50/40 modular assembly is via the systemic busbar (I 41). The memory uses dynamic memory elements, the contents of which are renewed at an interval of maximally 2 ms. Memory control is designed so that during the cyclic renewal of request for reading or entry it always automatically waits until the operation is completed. Similarly, a request for renewal waits until the ongoing cycle of reading or storage is completed.

From the functional viewpoint the memory can be divided into the following parts:

--block of address decoder of memory blocks,
--selection of 16 KB module,
--memory control,
--16Kx8-bit memory matrix,
--register of input/output data.

Technical specifications:

memory capacity	16 KB
word length	8 bits
addressing potential	0-64K in step 16K
access time	< 420 ns
memory cycle for reading	<< 640 ns
memory cycle for recording	< 640 ns
memory cycle in regeneration of info	< 640 ns
connection to the system	via systemic busbar (I 41)
max. external dimensions of module	295x245x15 mm
weight	< 1 kg
feed voltage/max. consumption	+ 5 V/1.5 A - 5 V/0.02 A + 12 V/0.35 A
feed voltage tolerance	± 4 percent

SM 0441 C, N, A 16 KB C MOS RAM Memory With Battery Reserve

The semiconductor working memory storage 16 KB C MOS RAM is an independent functional block for use in microcomputer systems based on SM 50/40 in the following variants:

memory 16 KB C MOS	SM 0441/C
memory 16 KB N MOS	SM 0441/N
memory 16 KB N MOS/C MOS	SM 0441/A

The static memory elements of the memory field of the 16 KB N MOS memory are N MOS MHB 2101 A, those of C MOS memory are MHB 1902 A elements.

The memory field of the N MOS/C MOS memory has a combination of these elements in the requisite modules with 4 KB each. The C MOS static memory elements are fed in backup mode from a source of backup voltage located on the SM 0441 plate, thus providing for the protection of information against loss in case of power outage in the grid.

Technical specifications:

plate dimensions	280x240x15 mm
weight	up to 0.7 kg

Plate SM 0441/C--Memory 16K byte C MOS RAM:

max. memory capacity	16 KB
word length	8 bits
addressing potential	in range 0-64K in step 16K in range 16K in step 4K
blocking of random module	4K
access time	950 ns
memory cycle	1.1 µs

operating modes	reading recording backup
length of data protection by backup during power outage	minim. 100 hrs
feed voltage/max. consumption	+ 5 V/0.7 A + 12 V/0.12 A

Plate SM 0441/N--Memory 16K byte N MOS RAM:

max. memory capacity	16 KB
word length	8 bits
addressing potential	in range 0-64K in step 16K in range 16K in step 4K
random module blocking	4K
access time	460 ns
memory cycle	560 ns
operating modes	reading recording
feed voltage/max. consumption	+ 5 V/4.5 A

Plate SM 0441/A--Memory 16K byte N MOS/C MOS RAM:

max. memory capacity	16 KB
word length	8 bits
memory addressing potential	in range 0-16K in step 16K in range 16K in step 4K
random module blocking	4K
access time for N MOS	460 ns
access time for C MOS	950 ns
memory cycle	1.1 µs
operating mode	reading recording backup of memory C MOS
length of data protection by backup during power outage	minim. 100 hrs
configuration	feed voltage/max. consumption
4 KB N MOS + 12 KB C MOS	+ 5 V/1.7 A + 12 V/0.12 A
8 KB N MOS + 8 KB C MOS	+ 5 V/2.6 A + 12 V/0.12 A
12 KB N MOS + 4 KB C MOS	+ 5 V/3.5 A + 12 V/0.12 A

SM 0442 A, B 64K Byte RAM and 16K Byte EPROM Memory

This semiconductor working memory storage forms an independent functional block of 64 KB RAM memory (read/record) of 16 KB EPROM memory (read only, with possibility for electronic programming of memory in the PGM 08 programmer of the MVS developmental system). It is intended for systems based on SM 50/40.

The RAM memory field with module 16K can be addressed by internal couplings up to a capacity of 64K on plate and EPROM memory field with module 16K at random in address space 0-64K in capacity range 16K at random in step 1K.

The memory field of RAM memory has N MOS memory elements with dynamic information storage (MHB 4116 or equivalent), the memory field of the EPROM memory has EPROM-type memory elements (12708 or equivalent).

In use of the 16 KB EPROM memory, the 16 KB capacity of RAM memory need not be used in the same address position, whereby the overall usable capacity of the SM 0442 module is maximally 64 KB.

Technical specifications:

capacity of RAM memory	up to 64 KB
capacity of EPROM memory	up to 16 KB
word length	8 bits
access time of RAM memory	$\leq$ 420 ns
access time of EPROM memory	$\leq$ 550 ns
reading cycle length of RAM	$\leq$ 590 ns
recording cycle length of RAM	$\leq$ 590 ns
info regeneration cycle length	$\leq$ 590 ns
cycle length of EPROM memory	$\leq$ 650 ns
max. external dimensions of module	280x240x15 mm
weight	up to 1 kg

Variant SM 0442/A:

selectable memory ranges	48 KB RAM + 16 KB EPROM 32 KB RAM + 16 KB EPROM 16 KB RAM + 16 KB EPROM
feed voltage/max. consumption	+ 5 V/1.3 A - 5 V/0.45 A + 12 V/0.55 A

Variant SM 0442/B:

selectable memory range	64 KB RAM 48 KB RAM 32 KB RAM 16 KB RAM
feed voltage/max. consumption	+ 5 V/1.1 A - 5 V/0.01 A + 12 V/0.25 A

SM 0449 16K Byte EPROM Memory

Programmable semiconductor memory of 16 KB capacity serves for the storage and reading of information during power outage. The fixed recording of memory contents is done by individual memory chips on a special device, e.g., PGM 08.

Technical specifications:

memory capacity	16K byte
word length	8 bits
access time	< 550 ns
reading cycle length	< 650 ns
connection with system	systemic busbar (I 41)
max. external dimensions of module	295x245x15 mm
weight	up to 1 kg
power feed	+ 5 V/1.4 A + 12 V/1.1 A - 5 V/0.85 A
power feed tolerance	± 4 percent

4.1.4 Input/Output Units

SM 1350 Low-Level Multiplex (LLM) of Analog Signals

The LLM module is a contactless semiconductor switch operating on the principle of a memory condensor. It contains 16 differential input channels with two pairs of switching transistors by which the input signal is fed to an amplifier. The differential amplifier is located in a thermostat to reduce thermal dependence on ambient temperature. The module is intended for connecting recorded low-level voltage signals (up to 100 mV--e.g., from thermocouples, current signals 5 mA, 10 mA and measuring by means of resistance sensors--resistance transmitters) to an analog converter. The SM 1350 module, or several SM 1350 and SM 1360 modules, form together with the SM 1352 module a functional unit. All control signals of the LLM module are generated by control circuits of the SM 1352 module--analog-to-digital converter. It has no direct connection to the busbar.

On the plate are located control circuits, an address decoder, an address multiplex and a differential amplifier. The user can place terminator resistors for current signals or current sources for resistance sensors on the plate.

The SM 1350 plate is connected to the SM 1352 control plate via the busbar of an analog subsystem by insertion into a random position in the grid or cassette which has a source with the requisite voltage.

The recommended types of ranging strips and cables are shown in Table 6.

Table 6. Types of ranging strips and cables for SM 1350 (LLM)

Signal	Ranging strip in system SM 50/40	SM 53/10	Cable
Voltage - U	1 X SM 1375	1 X SM 1380	8 XF 641 151
Current - I	1 X SM 1375	1 X SM 1380	8 XF 641 151
Current - I	1 X SM 1376	2 X SM 1380	8 XF 641 150
	2 X SM 1375	2 X SM 1381	8 XF 641 151
Resistance - R	2 X SM 1375	2 X SM 1375	8 XF 641 150
Current - I and resistance - R	2 X SM 1376	2 X SM 1380	8 XF 641 150

Technical specifications:

number of inputs on module	16
character of input signals	differential voltage
ranges	0-10 mV ± 10 mV
	0-20 mV ± 20 mV
	0-50 mV ± 50 mV
	0-100 mV ± 100 mV

Basic measuring error (from entire range):

in ranges	0-10 mV	± 10 mV	± 0.4 percent
	0-20 mV	± 20 mV	± 0.4 percent
	0-50 mV	± 50 mV	± 0.2 percent
	0-100 mV	± 100 mV	± 0.2 percent

measuring time	200 µs
suppression of two-phase interference	100 dB/0-50 Hz
suppression of normal interference	60 dB/0-50 Hz
input resistance	50 MΩ
selectable circuits on module for power feed to resistance sensors	power sources
	0.25 mA
	0.333 mA
	0.5 mA
selectable circuits in ranging part	resistance sensors for current signals
	5 mA
	10 mA
	20 mA
dimensions	280x240x15
weight	up to 0.5 kg
feed voltage	+ 5 V
	+ 15 V
	- 15 V
feed voltage tolerance	± 5 percent

Note: Specifications apply in connection with the SM 1352 module.

SM 1352 Analog-to-Digital Converter (ADC)

This ADC module forms with the multiplex of analog signals the input block for analog signals. It serves for the conversion of analog signals in the form of direct current or voltage into digital form and their introduction into the computer. The block is suited for direct control of production processes in industry and for laboratory purposes.

The ADC can work with a system based on the SM 50/40 modular assembly via the I 41 systemic busbar as a memory sector or an input/output device. It is connected with the multiplex by reserved conductors of the busbar of the analog subsystem. The ADC module contains a central analog-to-digital converter, registers and control circuits required for controlling the operation of the block of analog inputs.

From the functional viewpoint the module can be divided in closer detail into the following parts: address decoder, disconnection circuits, data transmission circuits, control and state register, gain register and multiplex address register, last address register, a comparator, five-input digital multiplex with eight bits each, a programmable amplifier, a sampling amplifier, an analog-to-digital converter, its control and control of the gating circuit as well as a testing source.

Structural design:

The module is designed as a standard 2/3 SMEP plate measuring 280x240 mm. It is connected via K1 and K2 connectors to the I 41 systemic busbar, where the feed voltage of + 15 V, - 15 V is also fed. Control signals for multiplexes are led out via the K1 connector to the reserved conductors of the busbar of the analog subsystem. On the opposite side of the module is a coaxial connector for feeding of testing voltage.

Technical specifications:

range of input controls (ranges controllable by program)	± 5 V, A = 1 0 to +5 V, A = 1 ± 2.5 V, A = 2 0 to + 2.5 V, A = 2 ± 1 V, A = 5 0 to + 1 V, A = 5 ± 0.5 V, A = 10 0 to 0.5 V, A = 10

--nominal static characteristics of conversions:

400 bit/1 V in range ± 5 V
800 bit/1 V in range 0 to +5 V
800 bit/1 V in range ± 2.5 V
1000 bit/1 V in range 0 to +2.5 V
2000 bit/1 V in range ± 1 V
4000 bit/1 V in range 0 to + 1 V
4000 bit/1 V in range ± 0.5 V
8000 bit/1 V in range 0 to + 0.5 V

--output data code:

--supplementary binary code on bipolar ranges
(+ 5 V, ± 2.5 V, ± 1 V, ± 0.5 V)
--direct binary code on monopolar ranges
(0 to + 5 V, 0 to + 2.5 V, 0 to + 1 V, 0 to + 0.5 V)

--number of output code orders

--nominal weight per unit of the least order of output code:

in range ± 5 V	2.5 mV
in range 0 to + 5 V	1.25 mV
in range ± 2.5 V	1.25 mV
in range 0 to + 2.5 V	0.625 mV
in range ± 1 V	0.5 mV
in range 0 to + 1 V	0.25 mV
in range ± 0.5 V	0.25 mV
in range 0 to + 0.5 V	0.125 mV

--characteristics of measuring errors at normal conditions according to NM MPV after VT 28-80 (20°C ± 2°C)

bipolar ranges:

permissible value of constant of basic error	γsd = ± 0.1 percent
permissible value of variable of basic error	δd = ± 0.1 percent

monopolar ranges:

permissible value of constant of basic error	γsd = ± 0.05 percent
permissible value of variable of basic error	δd = 0.05 percent

Errors are expressed in percentages of range.

--supplementary error from temperature change (Δt - 10°C)

at bipolar ranges
error constant $\gamma t, d$ = ± 0.05 percent
error variable $\delta t, d$ < 20 percent δd

at monopolar ranges:

error constant $\gamma t, d$ = ± 0.025 percent
error variable $\delta t, d$ = < 20 percent δd

--supplementary error from changes in humidity:

in relative humidity range of 40-80 percent at 30°C:
error constant $\gamma v, d$ < 20 percent $\gamma s, d$
error variable $\delta v, d$ < 20 percent δd

in relative humidity range of 80-90 percent at 30°C:

at bipolar ranges:

error constant γv, d = ± 0.05 percent
error variable δv, d = 0.05 percent

at bipolar [sic] ranges:

error constant γv, d = ± 0.025 percent
error variable δv, d = ± 0.05 percent

--supplementary error from vibrations (frequency and amplitude of vibrations according to NM MPK after VT 22-79):

at bipolar ranges:

error constant γvbd = ± 0.025 percent
error variable δvbd = ± 0.025 percent

at monopolar ranges:

error constant γvbd = ± 0.012 percent
error variable δvbd = ± 0.012 percent

--length of analog-to-digital conversion	tp = 30 µs ± 5 percent
--input current	I. inp. ≦ ± 10 nA at t ≦ 25°C I. inp. ≦ ± 150 nA at t = 55°C
module dimensions	280x240x18 mm
weight	0.5 kg
connectors	2 polar on plate (WK 180 48) 1 coaxial connector TX 611 1500
feed voltage/max. consumption	+ 5 V/1.8 A + 15 V/0.1 A - 15 V/0.05 A
feed voltage tolerance	- 15 V/0.05 A ± 4 percent

SM 1353 8-Bit Analog Outputs (A08)

The SM 1353-A08 module forms the output module of the contact with environment of the SM 50/40 microcomputer system and is suited for the control of production processes, for the display of digital information on the screen of an oscilloscope or some other display device. The A08 configuration includes eight 8-bit digital-to-analog converters and circuits for connection with the I 41 systemic busbar of the SM 50/40 system. The individual converters are designed for the conversion of data from the microcomputer to an analog output magnitude. The analog output signal can come from current or voltage

output. The A08 can cooperate with a system based on the SM 50/40 as a memory sector or as a peripheral unit. From the functional viewpoint we can differentiate between the following parts of the A08:

--address decoder,
--analytical circuit,
--data receiver,
--data register,
--D/A converter,
--voltage amplifier,
--current amplifier,
--INITL receiver,
--source of reference voltage.

Technical specifications:

number of inputs on module	8
data format	8 bits
data format at monopolar range	direct binary
data format at bipolar ranges	binary supplementary
format of output signal/load (selectable by coupling)	
voltage ranges	0 to 5 V/1 kΩ to ∞
	- 5 to + 5 V/1 kΩ to ∞
	0 to 10 V/2 kΩ to ∞
	- 10 to 10 V/2 kΩ to ∞
current ranges	0 to 5 mA/0 to 2 kΩ
	- 5 to + 5 mA/0 to 2 kΩ
	0 to 10 mA/0 to 1 kΩ
	- 10 to + 10 mA/0 to 1 kΩ
	0 to 20 mA/0 to 500 Ω
	- 20 to + 20 mA/0 to 500 Ω
galvanic separation of outputs	none
precision class	0.5 percent
conversion time	< 50 μs to 90 percent value with maximum ohmic load
output impedance	1 Ω
SM 1353 plate dimensions	280x240x16 mm
weight	up to 1 kg
outputs from plate into the system	standard via K1, K2 connectors
outputs from plate into ranging module	via P1 connector
feed voltage/max. consumption	+ 5 V/1.5 A
	+ 15 V/0.4 A
	- 15 V/0.3 A
feed voltage tolerance	± percent

Accessories:

8XF 641 150 interconnecting cable I	1 pc

SM 1354 12-Bit Analog Outputs (A012)

The SM 1354-A012 module forms a module for contact with environment for the SM 50/40 microcomputer system.

The A012 is intended for the conversion of data from a microcomputer to an analog output magnitude. It is suited for the direct control of production processes, for the imaging of digital data on display devices. The analog output signal can be taken from a voltage or current output.

The A012 configuration includes

--four 12-bit digital analog converters,
--circuits for connection with busbar of the SM 50/40 microcomputer.

Technical specifications:

number of outputs on the module	4
data form	12 bits
data form in monopolar range	direct binary
data form in bipolar range	binary complementary
type of output signal/load (selectable by coupler)	
voltage ranges	0 to 5 V/1 kΩ to ∞ - 5 V to + 5 V/1 kΩ to ∞ 0 to 10 V/2 kΩ to ∞ - 10 V to + 10 V/2 kΩ to ∞
current ranges	0 to 5 mA/0 to 2 kΩ - 5 to + 5 mA/0 to 2 kΩ 0 to 10 mA/0 to 1 kΩ - 10 to + 10 mA/0 to 1 kΩ 0 to 20 mA/0 to 500 Ω - 20 to + 20 mA/0 to 500 Ω
galvanic separation of inputs	none
precision class	0.1 percent
conversion time	< 50 µs up to 90 percent value at max. ohmic load
input impedance	1 Ω
plate dimensions	280x240x16 mm
weight	up to 1 kg
connectors	K1, K2 direct to busbar P1 (ELTRA 803) for cable to ranging module
feed voltage/max. consumption	+ 5 V/1.5 A + 15 V/0.25 A - 15 V/0.2 A
feed voltage tolerance	± 4 percent

Accessories:

8 XF 641 151 interconnecting cable II.

SM 1355A-F 48 Discrete Inputs/Outputs (DIO)

The SM 1355 plate of discrete, optically inculated, i.e., galvanically separated, 48 digital input/outputs in several variants provides for input/-output of signal and discrete controlled process into a system based on SM 50/40.

The DIO communicates with the processor under a program using program interruptions. The basic address of the DIO module, i.e., address of connection to systemic interface [sic] I 41 and the module's disconnecting level, are selected by wire couplings. The selection of the DIO module's basic address can be done in the memory and input/output of the SM 50/40 microcomputer system.

From the functional viewpoint the DIO module can be divided into the following parts:

--block of address selection in busbar and control logic,
--block of interruption logic,
--programmable interface circuits,
--block of galvanic separation.

The DIO module makes it possible to change the configuration of inputs/outputs and also the level of the input signal. For that reason the module comes in six basic variants:

SM 1355 A	32 inputs with level + 24 V 16 outputs
SM 1355 B	24 inputs with level - 24 V 24 outputs
SM 1355 C	28 inputs with level + 24 V 20 outputs
SM 1355 D	32 inputs with level + 48 V 16 outputs
SM 1355 E	24 inputs with level + 48 V 24 outputs
SM 1355 F	28 inputs with level + 48 V 20 outputs

Accessories:

96-pole connector	WK 180 48	1 pc

The DIO module with the listed combinations also includes the following:

32 inputs/16 outputs	8XF 642 019 testing connector	1 pc
24 inputs/24 outputs	8XF 642 020 testing connector	1 pc
28 inputs/20 outputs	8XF 642 021 testing connector	1 pc

Technical specifications:

input signal level:

for log 0	0 to 4.8 V or 0 to 9.6 V
for log 1	+ 24 V ± 20 percent or + 48 V ± 20 percent
max. current consumed by 1 input at log 1:	nominal 10 mA, max. 17 mA
insulation resistance of each input	100 MΩ/500 V
insulation voltage between inputs	235 V
insulation resistance of outputs	100 MΩ/500 V
load capacity of outputs	24 V/0.2 A
insulation voltage between outputs	235 V
max. dimensions of module	295x245x15 mm
weight	up to 1 kg
connector used	96 direct contact
feed voltage/max. consumption	+ 5 V/1 A
feed voltage tolerance	± 4 percent

SM 1356 A, B 16-Line Counter Inputs (CI)

The counter input module is intended for the processing of pulse signals in which the information carrier is the number of frequency of pulses from a controlled process in a microprocessor system based on the SM 50/40 modular assembly.

The SM 1356 module contains 16 input lines which are galvanically separated from the microcomputer system. Sixteen counters operate with a width of 16 bits.

The CI module facilitates:

--scanning of the state of counters,
--generation of a request for interruption after counting the requisite number of pulses,
--program -selected mode of any given computer.

The CI module can be addressed either as a memory cell or as an input/output device of a microcomputer system.

The CI module's counters can operate in the following modes:

--Mode A--reading of input pulse signals from zero till the 16-bit counter is filled, subsequent request for interruption, scanning of the counter's state. After read-off of the state of the counter it is set back to zero, i.e., it starts reading the input pulse signals from zero.

--Mode B--reading of input pulse signals from zero till the 16-bit counter is filled, subsequent request for interruption, scanning of the counter's state. After read-off of the state of the counter it is not set back to zero and continues counting input pulses from the read-off state.

--Mode C--reading of input pulse signals from a preset value (counter state), request for interruption during read-off of the present number of input pulse signals. Scanning of the counter's state, not causing resetting of the counter to zero. After request of interruption the counter must be preset to a new value.

--Mode D--reading of input pulse signals from a preset value (counter state) with recurring setting of the counter, request for interruption after reading the set number of input pulse signals. Scanning of the state of the counter, not causing it to be reset to zero.

Selection of the requisite mode of operation is done by the program.

Electric voltage levels corresponding to logic signals can be divided into three regions within OV-Vcc:

--region corresponding to log "0,"
--region corresponding to log "1,"
--region of forbidden levels.

Only leading descending pulse edges can appear in the region of forbidden levels.

Permissible region log "0" for signals of TTL level:

--input signals: 0 to 0.8 V,
--output signals: 0 to 0.45 V.

Permissible region log "1" for signals of TTL level:

--input signals: 2.0 to 5.5 V,
--output signals: 2.4 to 5.5 V.

The transition time of the leading and descending edge of pulses is approximately 10 ns.

Permissible region log "0" of signals from controlled process:

--0 V to 4.8 V for input signal level of + 24 V,
--0 V to 9.6 V for input signal level of + 48 V.

Permissible region log "1" of sianals from controlled process:

--+ 24 V ± 20 percent,
--+ 48 V ± 20 percent.

Module variants:

variants of plate A	log "1" + 24 V ± 20 percent log "0" 0 V to 4.8 V
variants of plate B	log "1" + 48 V ± 20 percent log "0" 0 V to 9.6 V.

Technical specifications:

counter capacity	16 bits
input signal level:	
for log "0"	0 to 4.8 V or 0 to 9.6 V
for log "1"	+ 24 V ± 20 percent or + 48 V ± 20 percent
insulation resistance of each input	100 MΩ/500 V
insulation voltage between inputs	235 V
number of inputs	16
max. frequency of input signal	2.5 kHz
plate dimensions	280x240x15 mm
weight	up to 1 kg
connector	96-contact, direct
type of cable for interconnection of input signals by ranging	8XF 641 151
feed voltage/max. consumption	5 V/3.5 A
voltage tolerance	± 4 percent

SM 1357 A, B Interruption Inputs (II)

The interruption inputs module is a plate which contains 31 + 1 optically insulated input lines and circuits for the control of interruption. The module is meant for processing and priority (asynchronous) analysis of input interruption signals from the environment into the microcomputer, whereby these signals call for immediate processing and response by the microcomputer.

The module contains:

--circuits for connection to the common busbar (I 41),
--input circuits,
--registers,
--multiplexes,
--input counter,
--programmable interruption controller based on 8259,
--a microprogrammable unit.

Those circuits provide for the following functions:

--activation of interruption on the basis of an input signal,

--programmable mode selection,
--reading the state of inputs at any random moment,
--reading the interruption vector which corresponds to the interrupting input signal in which there occurred a change of state and was given priority selection for interruption,
--masking of interruption,
--galvanic separation of input signals.

The characteristic of input/output signals corresponds to the counter inputs module CI plate SM 1356 A, B.

Technical specifications:

number of interrupted signals	32 (one of them for diagnostics)
level of interrupted signals	
log "0" module A	0 V to 4.8 V
log "0" module B	0 V to 9.6 V
log "1" module A	24 V ± 20 percent
log "1" module B	48 V ± 20 percent
insulation resistance of galvanic separation of inputs (each input)	100 MΩ/500 V
max. frequency of interrupting input signals	2.5 kHz
plate dimensions	280x240x15 mm
weight	up to 1 kg
feed voltage/max. consumption	+ 5 V/2.5 A
voltage tolerance	± 4 percent

SM 1358 8-Line Pulse Output (PO)

The pulse outputs module is an additive module for the microprocessor system based on SM 50/40 designed for control of analog regulators, DOC stations and stepping motors. It generates pulse signals with program-selected number and width of pulses and a signal standing for an expansion sign, and signals "MORE" or "LESS" that occur frequently in analog regulators designed for cooperation with a computer. The SM 1392-4 output modules can give the output the following character:

--transistor exciter without galvanic separation of TS,
--transistor exciter with galvanic separation of GO, GOZ,
--current output PV,
--TTL level.

One module has eight independent channels. From the functional viewpoint the module can be divided into: address decoder, data receiver, data register with counter, circuits controlling connection with the busbar, circuit for output state analysis, an optional adaption module, INITL receiver.

It is connected to the busbar by connectors K1 and K2. The type of output signal selected by a coupling is fed to the selected substitutable output module. Output modules are connected to the basic SM 1358 plate by one screw

and wire leads. Output signals from output modules are fed to the P1 output connector on the opposite side the K1 and K2 connectors.

Technical specifications:

number of output pulses	8
input data format	8 bit + sign bit in direct code
type of output signal (acc. to the used output module)	TTL
transistor exciter with open collector without galvanic separation	24 V/200 mA (TS)
transistor exciter with open collector with galvanic separation	24 V/200 mA (GO, GOZ)
current pulse	5 mA to + 5 mA (PV)
kind of output signal	0 to 255 with sign
number of pulses	0 to 255
number of pulses MORE, LESS	0 to 255 T with sign
pulse length	0 to 255 T
pulse length of MORE, LESS	
current, width-modulated pulse	+ 5 mA inactive 0
with the meaning MORE	5 mA
with the meaning LESS	1 Hz to 100 kHz derived from 9.2164 MHz frequency
time base frequency	potential connection of external time base at TTL level
plate dimensions	280x240 mm
weight	up to 1 kg
feed voltage/max. consumption	+ 5 V/3 A
feed voltage tolerance	± 4 percent

SM 1360 A, B Multiplex of High-Level Analog Signals (HLM)

This module is intended for connecting scanned voltage signals to an analog digital converter (ADC). The SM 1360 is actually a contactless semiconductor switch which contains 32 differential input channels by which the input signal is connected to an amplifier.

The addressed input channel is connected by analog multiplexes to a differential amplifier with transmission A=1, which changes input differential voltage into output asymmetric voltage.

The HLM can have an SM 1390 C and SM 1390 D current terminator, which serves for the conversion of current signals to voltage signals.

The plate contains the following blocks:

--control circuits,
--address decoder,
--analog multiplex,

--differential amplifier,
--power source for multiplex.

The HLM module is designed as a 2/3 SMEP plate bearing the designation SM 1360 A or SM 1360 B, depending on the type of multiplex. The module, or several types of modules SM 1360, SM 1350 form with the SM 1352 module an independent functional unit. All control signals of the HLM module are generated by control circuits of the SM 1352 module A/D converter; it has no direct connection to the I 41 busbar.

The plate contains three 96-contact direct connectors. Connectors K1 and K2 connect the module for power feed (+ 15 V, - 15 V) from the I 41 systemic busbar and to the SM 1352 module. Connector P1 connects analog signals from the environment to the multiplex plate.

Signals from the environment are connected to ranging strips and then via cables to the P1 connector of the HLM module. Depending on the type of signal, the following types of ranging strips and cables must be selected from Table 7.

Table 7. Types of ranging strips and cables for the SM 1369 (HLM)

Signal	Ranging strip in system		Cable
	SM 50/40	SM 53/10	
Voltage - U	2 X SM 1375	2 X SM 1380	8 XF 641 150
Current - I small system	2 X SM 1375	2 X SM 1380	8 XF 641 150
Current - I large system	2 X SM 1376	4 X SM 1381	8 XF 641 150
Voltage with filtering current - I	2 X SM 1376	4 X SM 1381	8 XF 641 150
Voltage with filtering current - I	2 X SM 1376	2 X SM 1381 1 X SM 1380	8 XF 641 150

A maximum of 8 HLM modules can be connected to one A/D converter. The HLM module has a maximum of 32 input channels.

The analog multiplex contains elements of the MAE 08B type (SM 1360 A plate) or the K 590 KH1 type (the SM 1360 B plate). Outputs of multiplexes are led to the differential amplifier with LF 356 elements.

Technical specifications:

number of inputs	32
character of input signals	differential voltage
ranges	0 to + 0.5 V ± 0.5 V
	0 to + 1 V ± 1 V
	0 to 2.5 V ± 2.5 V
	0 to 5 V ± 5 V

basic measuring error:

at unipolar ranges	≦ 0.005 percent of range
at bipolar ranges	≦ 0.1 percent of range
measuring time	50 µs
suppression of two-phase interference	≦ 60 dB in 0 to 50 Hz band
input resistance	≦ 50 MΩ
plate dimensions	280x240x18 mm
type of connector	96-contact, direct
feed voltage/max. consumption	+ 15 V/0.1 A - 15 V/0.05 A + 5 V/0.4 A
feed voltage tolerance	± 4 percent

SM 1390-1, 1396 Auxiliary Circuits for Signal Modification

Auxiliary circuits for signal modification are structurally separate independent modules that are connected to analog or ranging modules. They include the following modules:

--SM 1390 A-D resistance quadripole,
--SM 1391 RC quadripole-filter,
--SM 1396 A-C power supply sources.

Circuits SM 1390 and SM 1391 are located only on ranging module plates.

Circuits SM 1396 are always located on the SM 1350 low-level analog inputs module.

SM 2165 72-Line TTL (MPAPV) Parallel Inputs/Outputs

The SM 2165 module is an expansion module of the SM 50/40 system facilitating connection of devices with parallel interface.

The SM 2165 is divided into the following blocks:

--block of data busbar receivers and transmitters,
--address decoder block,
--control block,
--interrupting block,
--interface block for connecting of parallel systems.

The interface block for connection of peripheral devices is formed by three 8255 programmable circuits. Each circuit contains 24 parallel input/output lines divided into 3 channels with 8 lines each.

The module makes it possible to program 72 TTL level lines according to need, e.g.:

--one input channel,
--one output channel,
--one two-way channel.

Each of these varying modes calls for a different terminator circuit:

--resistance dividers for input channels,
--transmission exciter for output channels,
--two-way exciter for two-way transmission.

The terminator circuits of these transmission channels are inserted into the base of plates, making their replacement easy.

Technical specifications:

number of channels	6 + 3
data flow width	8 bits
plate dimensions	280x240x15 mm
weight	max. 1 kg
connectors	K1, K2 direct connector to systemic busbar 96-contact connector for connection of peripheral equipment

SM 2170 Mathematical Module

This mathematical module is intended for speeding up operations in the SM 50/40 system for applications which process large volumes of arithmetical computations with fixed and floating decimal point. This module operates in parallel with operation of the SM 2138 single-plate microcomputer.

Technical specifications:

length of argument	32 bits
argument w/floating decimal point:	
information	23 bits
exponent	8 bits
sign	1 bit
argument w/fixed decimal point:	
positive number	32 bits
number with random sign	31 + 1 bit
positive [sic] number	16 bits
operations	addition subtraction multiplication division extraction of root raising to a power
number of operational registers	16
average time for performance of instr.	70 μs

typical durations:

multiplication w/fixed decimal point	15 µs
root extraction w/floating dec. pt	205 µs
feed voltage/max. consumption	+ 5 V/6 A

4.1.5 Control Units for Peripheral Equipment

SM 2150 Four-Serial Asynchronous Channels (MPA SV)

The module of programmable adapters with serial interface is intended for connection of additive devices with serial interface to the SM 50/40 microcomputer system. The module makes it possible to connect four additive devices with IRPS or S2 (V.24 CCITT) interface. The module is programmable and facilitates two-way data transmission between the microcomputer system and an additive device at speeds of 50 to 9600 bit/s.

Accessories:

--MPASV interconnecting cable	8 XF 641 146	1 pc
--MPASV testing cable	8 XF 641 145	1 pc
--MPASV testing coupling	8 XF 642 018	1 pc
--SM 1215 plate	8 XF 052 095	1 pc

Technical specifications:

interface for connection to SM 50/40	systemic busbar (I 41)
interface for additive devices	IRPS (current loop) S2 (V.24 CCITT)
number of connectable input/output systems	4
type of operation	asynchronous
transmission speeds	50, 100, 200, 300, 600, 1200, 2400, 4800, 9600 bit/s
number of information bits	5 to 8 (selected by program)
number of stop bits	1; 1.5; 2 (program-selected)
plate dimensions	280x240x15 mm
weight	0.5 kg
connector for connecting of peripheries	96-contact, direct
feed voltage/max. consumption	+ 5 V/3 A + 12 V/0.5 A - 12 V/0.5 A
feed tolerance	± 4 percent

SM 2151, SM 2152 Control Unit for Floppy Disk Memory

The control unit for a floppy magnetic disk memory makes it possible to connect this memory to the SM 50/40 microcomputer system through its systemic busbar (I 41). The incorporation of this unit into the system is shown in Figure 72.

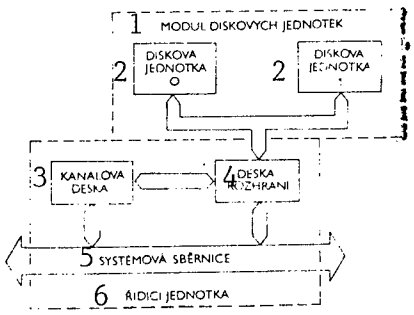


Figure 72. Floppy Disk Memory Wiring

Key:
1. disk unit module
2. disk unit
3. channel plate
4. interface plate
5. systemic busbar
6. control unit

The control unit consists of two plates:

--SM 2151 channel plate,
--SM 2152 interface plate.

The SM 2151 channel plate represents the basic module.

It receives, decodes, and responds to channel instructions from the SM 2138 central processor, facilitates the transmission of data, monitors the state of the disk unit and error conditions. These indicative bits are organized into the final byte that can be read by the central processor. Control functions of the channel plate and interface plate are provided for by an 8-bit microprocessor composed of elements of the 3000 series.

The channel plate consists of the following functional blocks:

--block of channel instructions,
--microprocessor control unit (MCU) block,
--microprogram memory block,
--block of the chief progressive element (CPE),
--block of data and clock shift registers (SR),
--data control block.

The SM 2152 interface plate provides communication between disk units and the I 41 systemic busbar. Under microprogram control from the channel plate the interface plate generates signals which control the movement of headings. The interface plate receives data read from the disk, interprets certain synchronizing bit samples, controls the correctness of data by using a control polynomial and transfers the data to the channel plate. During the recording operation the interface plate transmits at the required time data and clock bits to a selected disk unit. It also generates two bytes of cyclical control code, which are added behind the data and serve for control of correct data reading.

When the disk control unit requires access to the working memory storage, the interface unit requests and maintains the systemic busbar as a "master" and generates a suitable instruction in the memory.

When the SM 2138 central processor transmits a channel instruction into a disk memory, the channel plate confirms it in accordance with the relevant procedure for operation on the systemic busbar.

The interface plate can be divided into the following functional blocks:

--disk unit control block,
--serial data and clock bit synchronizing block,
--generator of recording pulses,
--CRC block for backup control generation,
--busbar control block.

Technical specifications:

number of control unit modules (plates)	2
dimensions of modules	295x245x15 mm
interface	systemic busbar (I 41)
feed voltage/max. consumption	+ 5 V/3 A
feed tolerance	± 4 percent

SM 2143 Nonstandard Interface Module

The nonstandard interface module is intended for connecting peripheral units with a parallel interface that is different from the standard IRPR interface, e.g.:

--FS 1501 A/M perforated tape reader,
--DT 105 S perforated tape punch,
--CONSUL C 2111 point printer,
--eventually also the PGM 08 programmer,

to the basic SM 2138 module. This interconnection can be made either by means of the 7 CK 895 056 (FS 1501, DT 105 S, C 2111) cable or by the SM 2158 (PGM 08--part MVS I and MVS II) wafer, and thus the nonstandard peripheries plate must be placed into the grid in a position adjacent to the basic module. The nonstandard interface module structurally takes up one position.

Technical specifications:

interface used	parallel
max. dimensions of module	295x245x15 mm
weight	< 1 kg
feed voltage/max. consumption	+ 5 V/0.3 A + 12 V/0.05 A
feed tolerance	± 4 percent

4.1.6 Power Supply Sources

Basic Power Supply Source A (± 5 V, ± 12 V)

The basic network power supply source A is intended for all types of microcomputer systems based on the SM 50/40 cassette. The basis of the source is formed by the SM 4072/A plate. The module is provided with a metallic cover. Source A takes up two positions in the cassette.

Technical specifications:

SM 4072/A plate dimensions	280x240x38 mm
max. external dimensions of source	310x255x45 mm
weight	approx. 3.5 kg
[power feed]	220 V + 10 percent - 15 percent
frequency	50 Hz ± 1 Hz
max. consumption	230 VA
output voltage/max. current	+ 5 V ± 0.1 V/10 A - 5 V ± 0.1 V/1 A + 12 V ± 0.15 V/2 A - 12 V ± 0.15 V/1 A

Power Supply Source B (+ 5 V, + 12 V, ± 15 V)

The network power supply source B is intended to be supplementary for modules for connection with the environment of microcomputer systems built on the basis of the SM 50/40 cassette. The basis of the source is formed by the SM 4072/B plate. The module is provided with a metallic cover. Source B takes up two positions in the cassette.

Technical specifications:

SM 4072/B plate dimensions	280x240x38 mm
max. external dimensions of source	310x255x45 mm
network power feed	220 V + 10 percent - 15 percent
weight	approx. 2.5 kg
frequency	50 Hz ± 1 Hz
max. power input of source	230 VA
output voltage/max. current	+ 5 V ± 0.1 V/10 A + 12 V ± 0.15 V/1 A + 15 V ± 0.15 V/1 A
[max. power output]	95 W

Power Supply Source C (± 5 V, + 12 V)

The network power supply source C is intended to be supplementary for the MVS 80 developmental microcomputer system built on the basis of the SM 50/40 cassette. The basis of the source is formed by the SM 4072/C plate. The module is provided with a metallic cover. Source C takes up two positions in the cassette.

Technical specifications:

SM 4072/C plate dimensions	280x240x38 mm
max. external dimensions of source	310x255x45 mm
weight	approx. 2.5 kg
network power feed	220 V + 10 percent - 15 percent

frequency	50 Hz ± 1 Hz
max. power input of source	230 VA
output voltage/max. current	+ 5 V ± 0.1 V/16 A - 5 V ± 0.1 V/1 A + 12 V ± 0.15 V/1 A
max. power output	95 W

Power Supply Source D (+ 5 V, ± 12 V, + 18 V)

The network power supply source D is intended as supplementary for microcomputer systems built on the basis of the SM 50/40 cassette. Its basis is formed by the SM 4072/D plate. The module is provided with a metallic cover. Source D takes up two positions in the cassette.

Technical specifications:

SM 4072/D plate dimensions	280x240x38 mm
max. external dimensions of source	310x255x45 mm
weight	approx. 2.5 kg
network power feed	220 V + 10 percent - 15 percent
frequency	50 Hz ± 1 Hz
max. power input of source	230 VA
output voltage	+ 5 V ± 0.1 V/10 A + 12 V ± 0.15 V/1 A - 12 V ± 0.15 V/1 A + 18 V ± 0.15 V/1 A
max. power output	95 W

4.1.7 Structural Elements

Cassette

A cassette is the basic structural element of the SM 50/40 modular assembly.

The cassette consists of:

--the mechanical cassette itself,
--SM 2141 matrix plate with positions for 5 modules (plates) + 2 modules for a power supply source,
--a ventilator.

The basic configuration for OEM purposes is formed by the so-called cassette of variant A, supplemented by power source A, a simple control panel and network power feed (SM 0250) and the basic module of the SM 2138 single-plate microcomputer. The cassette in this configuration has four spare positions for expansion modules.

The matrix desk is terminated by a connector through which it is possible to connect to cassette A yet one more expansion cassette supplemented by a suitable power supply source and thus devise an expanded configuration. In the latter case the cassettes form one mechanical unit.

The cassette A or combined cassettes can be mechanically suspended in the built-in system by means of M 4 screws. The spacing of these suspension openings is shown in Figures 73 and 74.

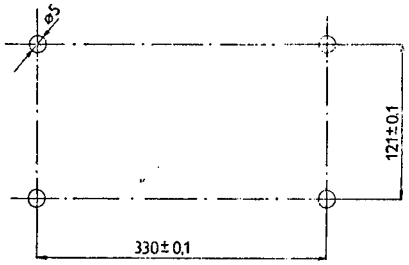


Figure 73. Spacing of suspension openings of a single cassette

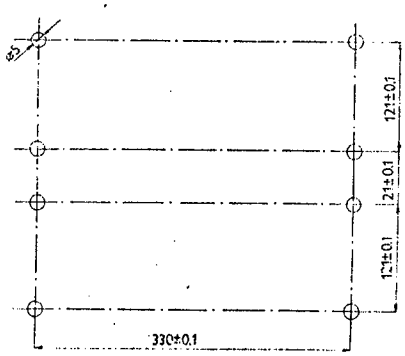


Figure 74. Spacing of suspension openings for two combined cassettes

The designation of the cassettes (e.g., cassette A) is derived from the type of the used source (in this case source A).

Technical specifications:

max. number of combined cassettes	2
cassette dimensions	452x151.5x308 mm
weight	up to 10 kg

Ranging Box

The ranging box is a supplementary element of the SM 50/40 cassette used for the interconnection of cables from the environment, i.e., from individual sensing action elements, with cables of the individual modules of units for contact with the environment.

Technical specifications:

ranging box dimensions	452x284x120 mm

4.1.8 MVS Developmental Systems

Microcomputer developmental systems [MVS] represent the basic hardware for the generation of software for systems based on SM 50/40 modular assembly of 8-bit microcomputers. With the use of other means they facilitate the verification of the correct and required functioning of the developed user systems

connected with a controlled user object and, further, programming of EPROM-type memories.

Basic configurations:

Depending on hardware configuration, we differentiate between two basic MVS configurations:

--MVS I developmental system in perforated tape version,
--developmental system equipped with external memory with floppy magnetic disk, the so-called MVS II disk-oriented version.

Both variants of these systems are described in detail below.

MVS I Perforated Tape Oriented Developmental System

The microcomputer developmental system in the MVS I perforated tape version is intended for the generation of software for SMEP systems based on the MHB 8080 microprocessor. The MVS I configuration includes:

--The basic MVS unit, consisting of terminal with keyboard, operator control panel located next to terminal, power source, and a grid for eight plates-modules. The grid is composed of the following modules:

  --SM 2138 single-plate microcomputer,
  --terminal control module,
  --SM 0442 64 K byte RAM memory,
  --MVE 80 developmental emulator and accessories that take up two positions since they are designed on two plates,
  --SM 2143 nonstandard interface module for connection of perforated tape reader, perforated tape punch and printer,
--FS 1501 A/M perforated tape reader,
--DT 105 S perforated tape punch,
--CONSUL C 2111 dot printer,
--PGM 08 programmer of EPROM memory,
--three work desks, accompanying documentation, connecting cables and accessories.

Peripheral units are connected to the rear connector panel of the basic unit containing 6 connectors with 25 Cannon-type contacts each. Figure 75 shows the systemic structure of the MVS I developmental system in the perforated tape version and Figure 76 shows the layout of MVS blocks.

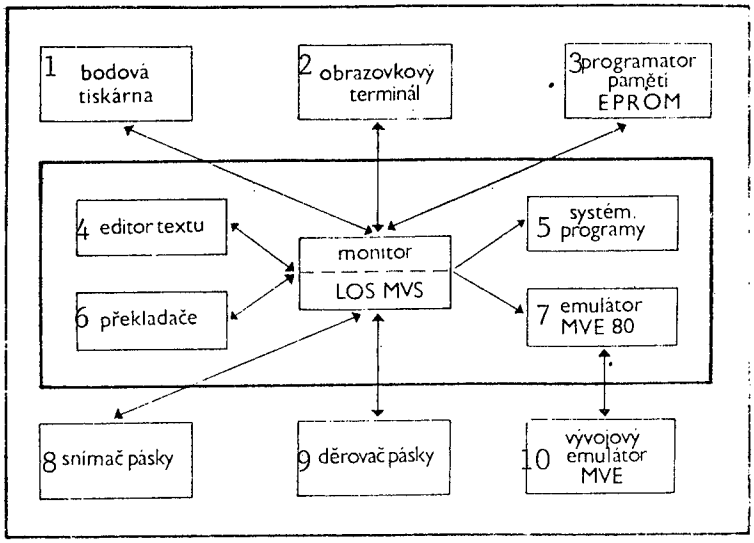


Figure 75. Systemic structure of MVS I in perforated tape version

Key:
1. dot printer
2. display terminal
3. EPROM memory programmer
4. text editor
5. systemic programs
6. translators
7. emulator
8. tape reader
9. tape perforator
10. developmental emulator

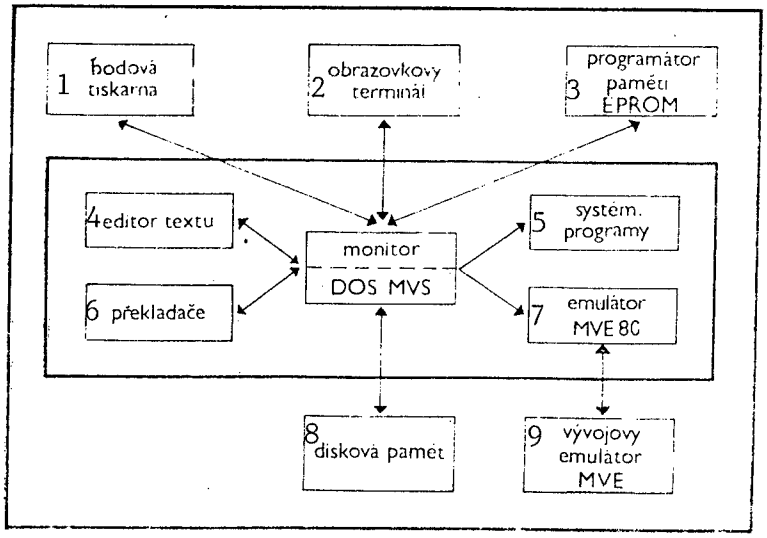


Figure 76. Systemic structure of MVS II in disk-oriented version

Key:
1. dot printer
2. display terminal
3. EPROM memory programmer
4. text editor
5. systemic programs
6. translators
7. emulator
8. disk memory
9. developmental emulator

MVS II Disk-Oriented Developmental System

The MVS II disk-oriented microcomputer developmental system with external memory on a floppy magnetic disk is intended for the generation of software and for the application of SMEP systems based on the MHB 8080 microprocessor. The configuration of hardware is conducive to the use of disk-oriented operating systems, and higher programming languages, and expands the potential for using these systems.

MVS II configuration includes:

--the basic MVS unit analogous to that of the MVS I system and containing:

  --SM 2138 single-plate microcomputer,
  --terminal control module,
  --SM 0442/B 64KB RAM memory,
  --MVE developmental emulator formed by two plates and accessories,
  --control unit of floppy disk memory designed on two plates,
  --SM 2143 nonstandard interface module for connection of perforated tape reader and printer,

--external memory with a floppy magnetic disk,
--FS 1501 A/M perforated tape reader,
--CONSUL C 2111 dot printer,
--PGM 08 EPROM memory programmer,
--four work desks, accompanying documentation, connecting cables and accessories.

The connection of peripheral equipment coincides with that used in the MVS I system. The systemic structure of the MVS II developmental system can be seen in Figure 76.

Individual Modules of Developmental Systems

The modules of developmental systems include, on the one hand, the individual modules of the SM 50/40 cassette modular assembly described in detail in the preceding part and, on the other hand, modules and individual devices listed in the configuration of developmental systems MVS I and MVS II. A more detailed description of these devices follows.

Basic Unit

The basic unit of SMEP microcomputer systems, i.e., developmental systems for the SM 50/40, microcomputers based on the 50 40, as in the SM 50/50, is formed by a modified display terminal. In the mechanical part of this terminal is a built-in grid for incorporation of eight 2/3 SMEP plates, operator control panel, a terminal control module and power sources.

Technical specifications:

effective screen area	200x120 mm
number of lines (optional)	16 (or 12)
number of symbols per line (optional)	64 (or 40)

Edit functions: carrier shift in four directions
carrier shift to start of image
carrier shift to beginning of line
tabulation, shift of information one line up

type of symbol generation	5x7 point raster
number of idsplayable symbols	64
interface used	serial IRPS
transmission speed used	9600 bit/s
dimensions	800x480x350 mm
weight with empty grid	up to 35 kg
power feed	220 V/50 Hz
max. power input	485 VA

The operator's panel is a functional complement of the basic unit. Its basis is formed by the SM 2149 plate attached to the front part of the terminal and connected by a connector to the internal systemic busbar (I 41) and with the SM 2138 module.

The panel's control elements allow the system's operator to perform initiation, introduce the basic lead-in program, manually set interruption at eight levels. Its indication elements indicate the states RUN and HALT and interruption levels RST 0-RST 7.

The terminal control module provides for the performance of all logic functions of the keyboard and screen of the basic unit. It is structurally designed on one plate and takes up one position in the grid of the basic unit.

MVE Microcomputer Developmental Emulator

MVE is one of the additive devices of the MVS microcomputer development system that makes efforts connected with design of microcomputer systems based on SM 50/40 easier and faster.

To operate with the emulator, it is connected by cable to the system being developed so that it actually replaces its microprocessor. The prototype system has at its disposal all systemic MVS resources (memory, peripheries) and diagnostic resources of the emulator. It can also be used for tuning programs, if the system is still not equipped with the requisite hardware. The emulator consists of two basic modules:

--SM 2135 processor module,
--SM 2134 monitoring module,

and also contains a connecting wafer which provides for the transmission of signals between the emulator and the system being developed.

Each module is structurally formed by one plate, meaning that MVE takes up two positions in the grid of the basic unit. The emulator communicates with the developmental system via the I 41 systemic busbar, emulator modules communicate among themselves via the emulator's internal busbar and are connected to the system being developed via the user busbar. From the MVS viewpoint the emulator is one of the input/output systems. Communication occurs via the control block with a 256 byte RAM memory in MVS.

The SM 2135 processor module forms a part of the MVE emulator. From the functional viewpoint it can be divided into the following parts:

--clock generator block with internal frequency of 2.048 MHz,
--MHB 8080 microprocessor block--carrying out either the user's or its own control program,
--address mapping block making it possible to "borrow" from the MVS its memory and peripheral equipment on behalf of the system being developed,
--MVS busbar control block,
--block of MVS busbar exciters and receivers,
--user busbar control block,
--emulation control block,
--state interruption register,
--timer.

The SM 2134 monitoring module can be divided from functional viewpoint into the following blocks:

--clock monitoring block,
--instructions decoder,
--instruction register and state register--they are the emulator's peripheries which facilitate communication with MVS,
--selection of interruption level,
--8080 state word register,
--multiplex,
--256 byte RAM memory,
--1K byte ROM memory,
--control pulse generator,
--address generator,
--emulation interruption logic,
--comparator,
--comparator's control register,
--interruption cause register.

The emulator can operate at full speed in real time or in a step-by-step mode. The emulator monitors the development of conditions for stopping emulation:

--occurrence of a specified address,
--occurrence of a signal defined by the user,
--user program remains inactive for one-quarter of a second,
--attempt to violate protected region,
--interruption from front panel via INT 4.

The emulator has 44 memory machine cycles.

Technical specifications:

SM 2135 plate

plate dimensions	280x240x15 mm
weight	up to 0.6 kg
feed voltage/max. consumption	+ 5 V/3.5 A + 12 V/150 mA - 5 V/1 mA

SM 2134 plate

plate dimensions	280x240x15 mm
weight	0.5 kg
feed voltage/max. consumption	+ 5 V/3.2 A - 5 V/50 mA + 12 V/100 mA

The SM 2154 connecting wafer is part of the equipment of the cable connecting the MVE emulator with the user system. It forms with the requisite conductors a small base that is inserted into the base of the MHB 8080 microprocessor in the user developmental system. The plate's only circuit is fed from the user source.

The SM 2146 MVE cable plate is part of the cable connecting the MVE emulator with the user system.

The operation of the MVE module is controlled by the MVE 80 program under the DOS MVS or LOS MVS operating system.

FS 1501 A/M Perforated Tape Reader

An independent input device is used for the input of perforated tape. The device forms a structurally independent unit designed for desktop use. The device is terminated by a parallel interface differing from IRPR (JSEP). Thus, it is connected to the system by means of the SM 2143 nonstandard interface module.

Technical specifications:

reading speed	1500 symbols/s
reading principle	photoelectric
tape width	5 to 8 tracks
dimensions	420x223x205 mm
weight	18 kg
power feed	220 V/50 Hz
power input	230 VA

In addition to the accessories supplied by manufacturer of peripheral equipment it comes with:

8XF 641 158 cable for reader	1 pc
8XF 641 155 cable of FS 1501 reader	1 pc

DT 105 S Perforated Tape Punch

The DOT 105 S is an output device used for output of data on perforated tape. It structurally forms an independent unit intended for desktop use. The device is terminated by a parallel interface differing from the IRPR (JSEP). Thus, it is connected to the system by means of the SM 2143 nonstandard interface module.

Technical specifications:

reading [sic] speed	50 symbols/s
tape width	5 to 8 tracks
dimensions	415x330x250 mm
weight	20 kg
power feed	220 V/50 Hz
power input	200 VA

Accessories:

In addition to the accessories supplied by manufacturer of peripheral systems, it comes with:

8XF 641 131 cable for perforator	1 pc
8XF 641 156 cable of DT 105S perforator	1 pc

CONSUL C 2111 Dot Printer

The CONSUL C 2111 dot printer is a serial printer used for the output of alphanumeric information from the system.

The dot printer is structurally designed as an independent unit for desktop use.

The device is terminated by a parallel JSEP interface differing from IRPR. Thus it is connected to the system by the SM 2143 nonstandard interface module.

Technical specifications:

max. printing speed	15 symbols/s
number of symbols (Latin alphabet)	64
imaging format	7x9 symbols [sic]
printing width	132 symbols
dimensions	700x543x950 mm
weight	47 kg
power feed	220 V/50 Hz
power input	450 VA

Accessories:

In addition to accessories provided by peripheral equipment manufacturer, it comes with:

EC 7181 mosaic cable	8XF 641 157	1 pc
cable for mosaic [printer]	8XF 641 159	1 pc

PGM 08 Programmer of EPROM Memory

The EPROM memory programmer is a device of MVS microcomputer developmental systems which makes it possible to

--store the contents of MVS memory in EPROM memory,
--store the contents of RAM memory in MVS memory,
--program direct or inverse data.

The entire programming process on the programmer is controlled by software. It can operate with memories of the types I 8708, 2708, MH 74188, MH 74S2871. The time for programming the I 8708 memory type takes approximately 140 seconds.

The programmer is an independent device for desktop use and is connected to MVS via the IRPR parallel interface.

The basis of PGM 08 is formed by a plate of the SM 2156 program module and a power sources module located in a box and a cable for connection to MVS that is a part of its configuration.

Technical specifications:

SM 2156 plate:

dimensions	280x240x13 mm
weight	350 g
feed voltage/max. consumption	+ 5 V/1.2 A + 12 V/0.2 A + 27 V/0.3 A - 5 V/0.15 A

PGM 08 programmer:

box type	WK 127 03
box dimensions	480x90x338 mm
weight	up to 6 kg
power feed	220 V/50 Hz
max. consumption	40 VA

Accessories:

PZ cable	8XF 641 131	1 pc
network cord		1 pc

Floppy Disk Memory

Floppy disk memory facilitates the recording of data on a disk, retrieval and reading of information.

The memory consists of a control unit and an independent grid with disk units. The control unit is formed by two plates:

--channel plate ,
--interface plate (see Figure 77)

which are placed into the basic unit.

Technical specifications:

format capacity of memory	2x256K byte
format capacity of track	3 326 byte
format capacity of sector	128 byte
number of tracks	77
recording format	ISO TC 97/DSC 11
type of entry	DF
transmission speed	250k bit/s
average access time	370 ms
number of revolutions	360 rpm
dimensions	493x723x344 mm
weight	max. 40 kg
power feed	220 V + 10 percent - 15 percent 50 Hz ± 1 Hz
power input	max. 350 VA

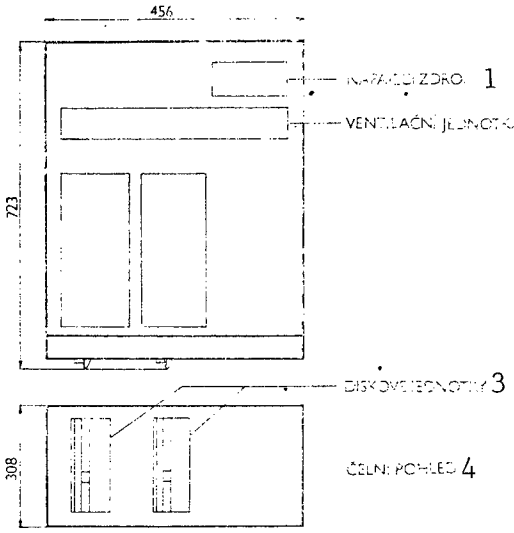


Figure 77. Dimensions of floppy disk memory (grid with CONSUL disk units)

Key:
1. power supply source
2. ventilation unit
3. disk units
4. front view

It is described in closer detail in the section on the SM 50/40 Cassette Modular System. The independent 19-inch grid contains two disk units (type CONSUL 7113, MOMFLEX MF 3200 or MF 6400 with the requisite electronics for reading, recording and control), a ventilation unit, a terminal box, power supply source and a distribution block (see Figure 77).

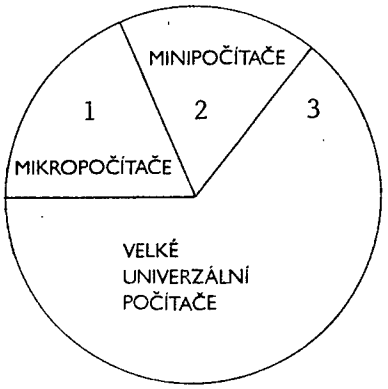
Accessories:

In addition to accessories supplied by the disk units producer, it comes with:

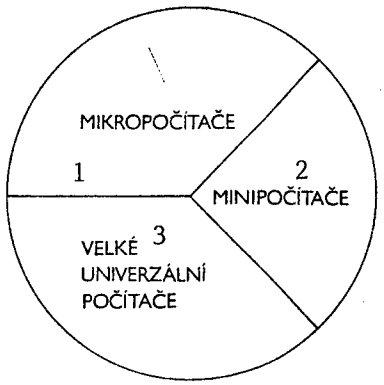
network cord	1 pc
PZ cable 8XF 641 131	2 pcs
RJ cable 8XF 641 139	1 pc

4.1.9 SM 50/40 Microcomputer

Eight-bit systems have found worldwide application in the area of data processing as microcomputers, office and desktop computers. At the present time microcomputers have gained a strong position in this sphere and are constantly expanding it. To offer an idea of the share of individual computer categories in data processing, Figure 78 provides worldwide statistics on its development expressed in turnover. The diagrams show the large number of microcomputer systems of all types that are in use as their price is lower by many times than that of large all-purpose computers.



1980: 100 percent of worldwide turnover



1985: 210 [sic] percent of worldwide turnover

Figure 78. Envisioned sales of computers for data processing divided by categories

Key:
1. microcomputers
2. minicomputers
3. large all-purpose computers

Office Machines will also start delivering these systems. It is envisioned to provide the SM 50/40 microcomputers in the initial stage in the following variants:

--basic microcomputer configuration for use as a so-called desktop or office computer,
--program terminal (terminal station),
--system for text processing.

From the viewpoint of hardware configuration it involves no basic changes; configuration of these systems is similar to that of developmental systems and is also based on the 50/40 modular system.

However, the software used by these systems is different. It includes new operating and programming systems, additional translators and user-oriented programs. Their detailed description is offered in the following sections.

Basic Configuration of the SM 50/40 Microcomputer

The basic configuration of SM 50/40 microcomputer (Figure 79) can be used for the automation of office operations, acquisition of data, processing of smaller agendas from the area of mass data processing, scientific and technical calculations, economic and statistical computations, etc. In its systemic concept this computation device is again based on the SM 50/40 modular assembly and its configuration includes:

--basic unit with a terminal and a built-in operator's panel with modules:

  --SM 3128 single-plate microcomputer,
  --SM 0442/B 64K byte RAM memory,
  --SM 2143 nonstandard interface module,

--CONSUL C 2111 (CONSUL C 2113) dot printer,
--FS 1501 A/M perforated tape reader,
--floppy magnetic disk memory,
--three desks and accessories.

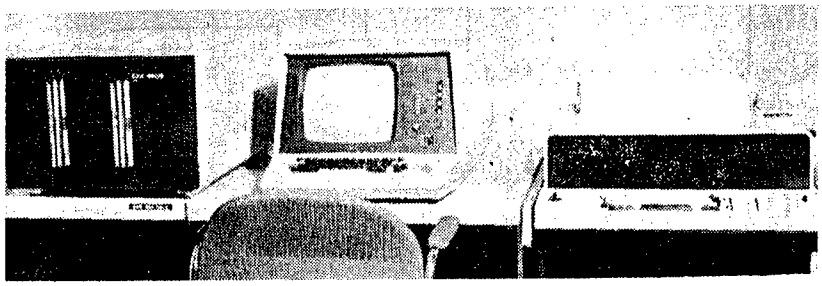


Figure 79. Basic configuration of SM 50/40 microcomputer

The MIKROS operating system with the relevant languages and libraries of subprograms are intended primarily for this microcomputer. The computer can also use the DOS MVS and MUOS operating system.

Programmable Terminal

The programmable terminal, sometimes also referred to as a terminal station, is a terminal device intended for both independent operation and interactive contact between operator and a hierarchically higher computer system. It can be used for the acquisition and preprocessing of data in the processing of production or administrative agenda, as a terminal for reservations, as an office terminal, countertop or business terminal. The control station makes it possible to connect three additional terminals, a memory with floppy disks and a printer (see Figure 80).

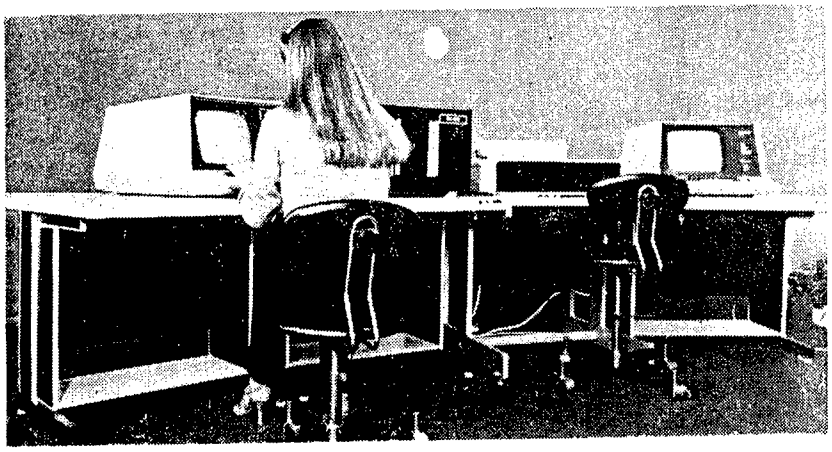


Figure 80. Programmable terminal workstation

The configuration of the programmable terminal coincides with configuration of the microcomputer, supplemented by the SM 2140 serial adapters module and the requisite expansion display terminals, so that it is formed as follows:

--basic unit with display terminal and operator's panel and modules:

- --SM 2138 single-plate microcomputer,
- --SM 0442/B 64K byte RAM memory,
- --SM 2150 [sic] serial adapters module,

--max. three CM 1601, CM 7202 expansion display terminals with IRPS, S2 interface,
--floppy disk memory,
--dot printer,
--three desks and accessories.

The described variant has in reserve one serial channel (IRPS or V.24 CCITT), e.g., for connection to a hierarchically higher computer, and three parallel channels with IRPR interface.

The MUOS operating system is intended for the programmable terminal. It is envisioned to supplement this operating system as well as communication software for communication with a hierarchically higher SMEP or JSEP computer and the relevant functional software for any given application, e.g., data acquisition.

System for Text Processing

One of the variants of the SM 50/40 microcomputer supplemented by additional hardware and software is the system for text processing.

The system for text processing is a device which with its keyboard--with key distribution corresponding to the distribution of keys on a normal typewriter in Czech or Slovak--makes it possible to generate routine texts such as letters, documentation, directories, lists, indices, etc., in Czech or Slovak with upper case and lower case letters and diacritical marks. These generated texts can be stored in floppy disk memory and, according to need, selected parts of the text can be displayed on the screen for correcting errors, substitutions, copying and supplementing random parts of the text. The stored text can be printed out on a printer in random format with various graphic modifications, offsets, paragraphs, new pages, etc.

The system for text processing is based on the SM 50/40 microcomputer and comprises the following:

--basic microcomputer unit built into a display terminal and containing:

  --SM 2138 single-plate microcomputer,
  --SM 0442 64K byte RAM/EPROM memory,
  --semigraphic module,

  --keyboard with key distribution corresponding to distribution of keys on a typewriter in Czech or Slovak,

--floppy disk memory,
--printer with contour printout (i.e., print corresponding to that of a typewriter), or an electric typewriter.

A variant of the text processing system configuration is shown in Figure 81. The text processing system operates with the TEXT 01 set of programs which provides for the requisite functions. TEXT 01 operates under the MIKROS operating system.

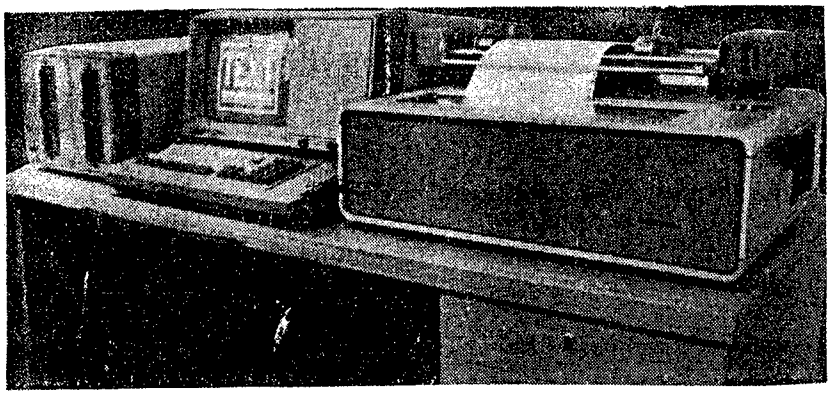


Figure 81. System for processing of texts with a dot printer

4.1.10 SM 53/10 Distributed Computer System

Systems for the control of technological processes are usually divided hierarchically into several control levels. A technological process usually consists of a series of partial, relatively independent processes. All functions for the automation of partial processes, such as regulation, guidance and control, are performed by the automation system at the lowest hierarchical level, i.e., the process level. On a higher hierarchical level, the so-called coordinative level (see Figure 82) there occurs coordination and control of larger parts of the process, consisting of several parts of the process. At this level computations of some balancing quantities and logic control are usually performed.

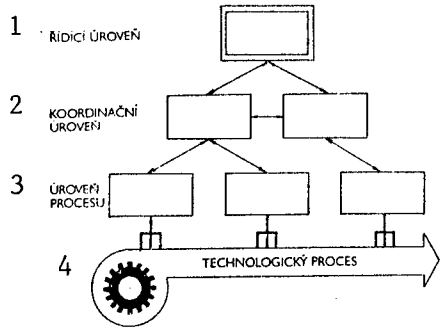


Figure 82. Structure of a hierarchical system for control of technological processes

Key:
1. control level
2. coordinative level
3. process level
4. technological process

Functions at the very top of an entire technological process, i.e., functions connected with analysis, optimization, processing of balancing quantities, economizing with energy and raw materials, etc., can be dealt with at the highest hierarchical level of control.

The hierarchical arrangement of the control system offers several advantages. Key advantages consist in cutting down on response time by the control system to an event in the process in comparison to centralized control, lowering of costs for interconnecting individual sensors and action elements of the

technological process with elements of the control system through the performance of initial processing of information at the lowest hierarchical level, the partial process level. No less advantageous is the improved reliability of the entire system thanks to its horizontal and vertical distribution into subsystems. The breakdown of a random partial process affects only a part of the entire process and the functioning of the entire system, though limited, remains preserved.

The SM 53/10 system constitutes a specific implementation of a distributed computer system for the control of technological processes. It is made up of functionally and structurally independent terminals connected in series into a single complex (Figure 83).

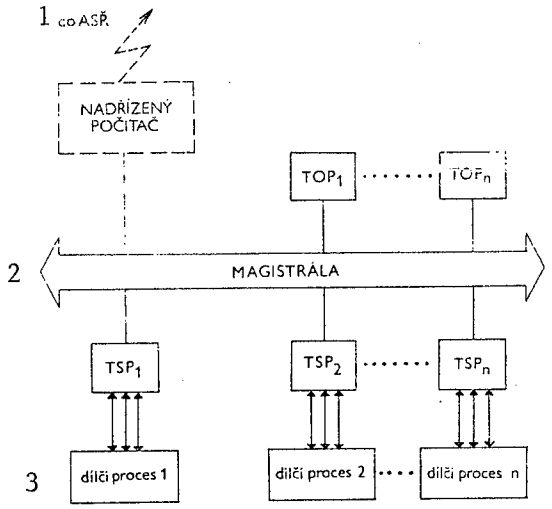


Figure 83. Structure of the SM 53/10 system

Key:
1. to automated control system
2. in series connection
3. partial process

Terminals are formed on the basis of SM 50/40 and are divided according to function into:

--TOP terminal of the process operator,
--TSP terminal for contact with environment.

A hierarchically higher level can make use of the SM 4-20, and SM 52/11 computers that are also connected in series.

The TOP process operator's terminal facilitates communication between the operator and the SM 53/10 system.

The operator can:

--monitor data from a selected place,
--check the state of closed control loops of any TSP terminal for contact with the environment,
--change the parameters and algorithms of these loops,
--monitor the state of the process on a displayed diagram,

--determine technological limits for control of individual input variables from the process,
--change data processing algorithms for input variables of the SM 53/10 system,
--monitor the trend in changes of individual process magnitudes, etc.

The terminal consists of the SM 50/40 microcomputer equipped with SM 50/40 modules, a semigraphic monitor, technological keyboard, floppy disk memory, a dot printer and a communication module.

The TSP terminal for contact with the environment provides communication with the technological process, i.e., it collects data from the process, preprocesses them and with the aid of action elements provides for eventual regulation or control.

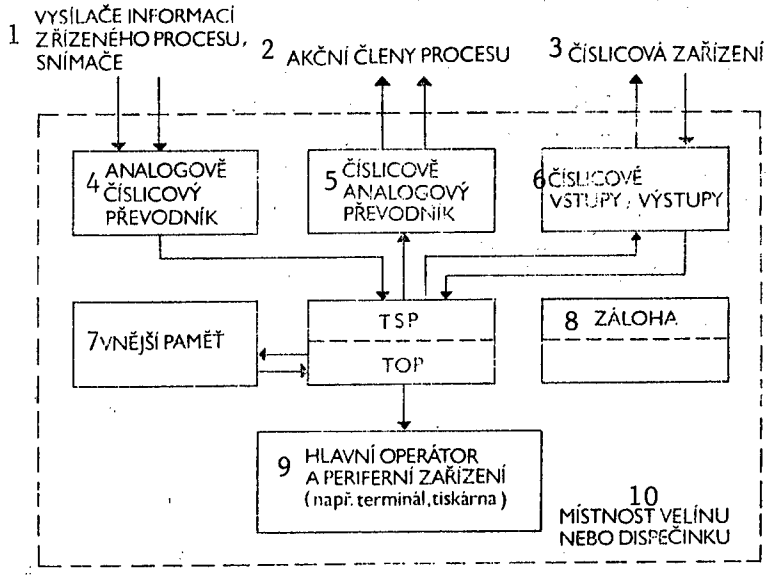


Figure 85. Example of a simple configuration of a centralized control system

Key:
1. transmitters of information from controlled process, sensors
2. action elements of process
3. digital systems
4. A/D converter
5. D/A converter
6. digital inputs/outputs
7. external memory
8. reserve
9. main operator and peripheral equipment (e.g., terminal, printer)
10. control room or dispatching room

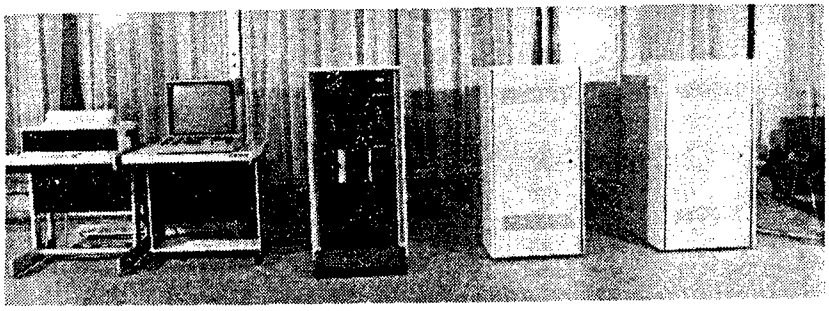


Figure 86. Configuration of the SM 53/10 system (1xTOP and 2xTSP)

The TSP terminal for contact with environment is formed by simple SM 50/40 modules described in the relevant section, supplemented by a communication module which is described below.

The general configuration of the terminal is as follows:

--SM 2136 (variant 1) single-plate microcomputer,
--SM 1344 diagnostic module with interruption system,
--any suitable memory module,
--selectable modules of units for contact with the environment,
--communication module for connection to SM 1341 serial connection of SM 53/10,
--terminal box with distributor, power source and ventilation,
--ranging box for connection of cables (distribution block).

The terminal for contact with the environment is an operatorless terminal which communicates with other parts of the SM 53/10 system via its in-series connection and is not equipped with peripheral systems.

In-Series Long-Distance Line

The in-series connection of the SM 53/10 system is formed by a coaxial cable to which individual terminals are connected and which provides for the transmission of information between individual terminals. Its interface is designated ILPS.

Up to 63 terminals can be connected to this long-distance line at its overall length of 1.5 km and at a data transmission speed of 47 KB/s. Terminals are galvanically separated from the line.

From the viewpoint of transmission control along the line the terminals are divided into three groups:

--central station, a selected TOP terminal which controls the assignment of the long-distance line to a requesting terminal, carries out cyclical queries into the state of terminals and supervises the line;

--control station that, if requested, can take over control of the line and establish connection with any random station;

--subordinate station that participates in transmission on the basis of a request from the control station (or from the central station), but cannot initiate transmission by itself.

The transmission procedure generally consists of two phases. An active station sends out a message on the basis of which the addressed station sends a response. The basic message format appears in Figure 84. Depending on the contents of the control field, the data part of the message transmits the requested data, provides responses to received data, etc. Safeguarding of the message is formed by CRC 16 CCITT cyclic code.

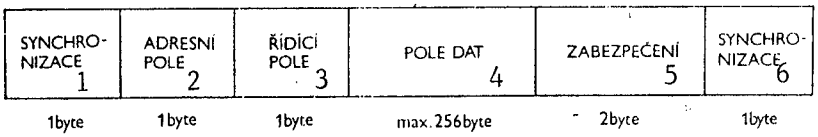


Figure 84. Basic message format (variant of HDLC routine)

Key:
1. synchronization
2. address field
3. control field
4. data field
5. safeguard
6. synchronization

This transmission procedure provides for the exchange of errorless messages among terminals and handling of emergency states during transmission.

The minimal SM 53/10 configuration is formed by one TSP terminal for contact with the environment and one TOP terminal of the process operator.

SM 1341 Communication Module

The communication module provides for communication among individual terminals of the SM 53/10 system as well between SM 53/10 and the hierarchically higher SM 4-20, SM 52/11 computers. Every terminal and computer connected to the long-distance line must be equipped with it.

Technical specifications:

type of transmission	series, synchronous
transmission routine	HDLC variant
transmission speed	47 KB/s
type of safeguard	CRC 16 cyclic code
structural design	2/3 plate

Structural Design

The TOP terminal of the process operator appears in the accompanying photograph. It consists of a casing, a desk, a monitor and a keyboard. The TSP terminal for contact with environment is formed by an independent box (Figure [87]).

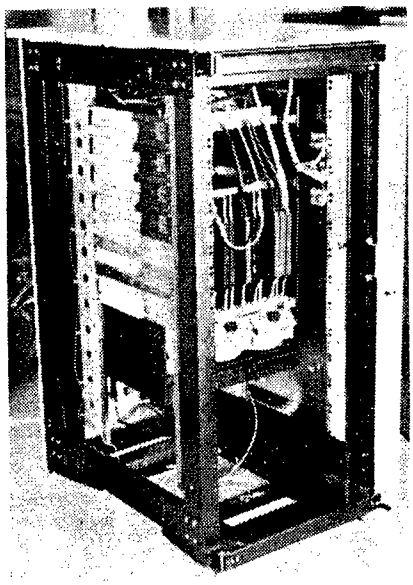


Figure 87. TSP terminal for contact with environment of the SM 53/10 system

The casing contains a grid for 16 modules of the SM 50/40 modular assembly and communication modules, up to two ranging panels (in the case of the TSP terminal) that make it possible to connect 14 ranging strips each of which contains up to nine 4-way terminal strips, connectors for the connection of cables and various auxiliary modules (e.g., terminator elements), a ventilation unit, 220 V distribution block and accessories.

Technical specifications:

Casing dimensions	800x800x1200 mm

The basic software for the SM 53/10 system is described in the relevant section together with the application-oriented MODUS system suitable for a distributed information or control system based on SM 53/10.

4.1.11 SM 53/20 Distributed System

The SM 53/20 system with distributed intelligence is another variant of the currently prepared applications of the SM 50/40 system supplemented by additional hardware (SM 1342 twin-access memory, communication processor based on 50/40, asynchronous adapter facilitating communication in more directions) and special software. Contrary to the SM 53/10, this involves a radial system where the connection of terminals is not tied to a connecting line of limited length, but occurs by serial asynchronous transmission with the use of modems.

4.1.12 VUVT Training Microcomputer

The training microcomputer is an experimental computer for theoretical and practical instruction in microcomputer technology for the TESLA MHB 8080-type circuit that can also be used as a portable microcomputer for small-scale testing and control.

The microcomputer is located in a portable attache case (see Figure 88). Its basis is formed by the microcomputer's base plate measuring 420x260 mm and including:

--MHB 8080 microprocessor with supporting circuits,
--keyboard with 24 elements,
--8-space 7-segment display,
--1K byte PROM memory with monitor,
--1K byte RAM user memory,
--input/output circuits--72 lines,
--three 16-bit timers,
--digital-to-analog and analog-to-digital converter,
--4-vector interruption logic,
--V.24 CCITT interface,
--converter for external memory formed by a conventional cassette tape recorder.

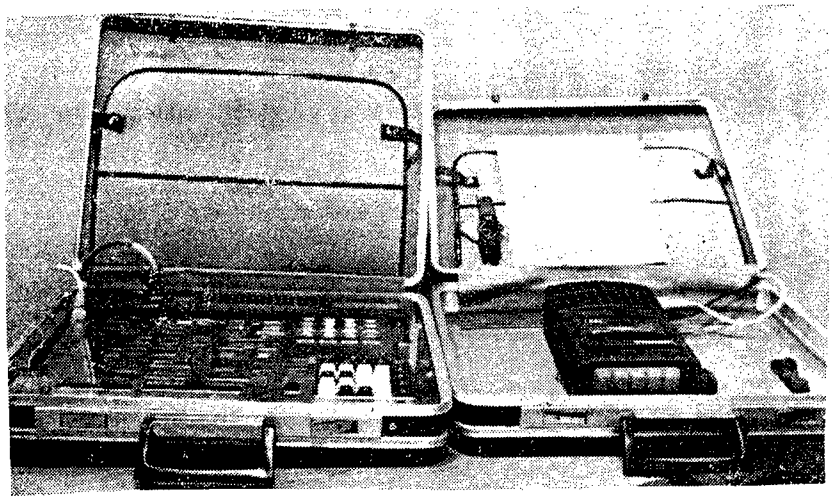


Figure 88. VUVT training microcomputer (overall view)

The microcomputer is ready for expansion by the following circuits:

--1K byte RAM user memory,
--3K byte EPROM memory,
--interface with 20 or 40 mA current loop.

A great many devices can be connected to the microcomputer from accessories (miniature motor with sensor of revolutions, duplicator, thermistor temperature sensor) as well as from other expansion modules, e.g., the CM 1601 or CM 7202 terminals.

The training microcomputer makes it possible to compile programs, load data into the microcomputer, control the correct functioning of compiled programs, examine the relation between hardware and software and use it as a basis for proposing user systems.

A part of the training computer is a library of programs stored on a cassette and handbooks of the microcomputer system.

A detailed view of the training microcomputer is shown in Figure 89.

The microcomputer's technical specifications are given by the MHB 8080 microprocessor and, as such, are identical with the specifications listed in the description of the SM 2138 microcomputer.

Additional technical specifications:

attache case dimensions	465x365x125 mm
weight	7 kg
power feed	220 V/50 Hz
max. power input	75 VA

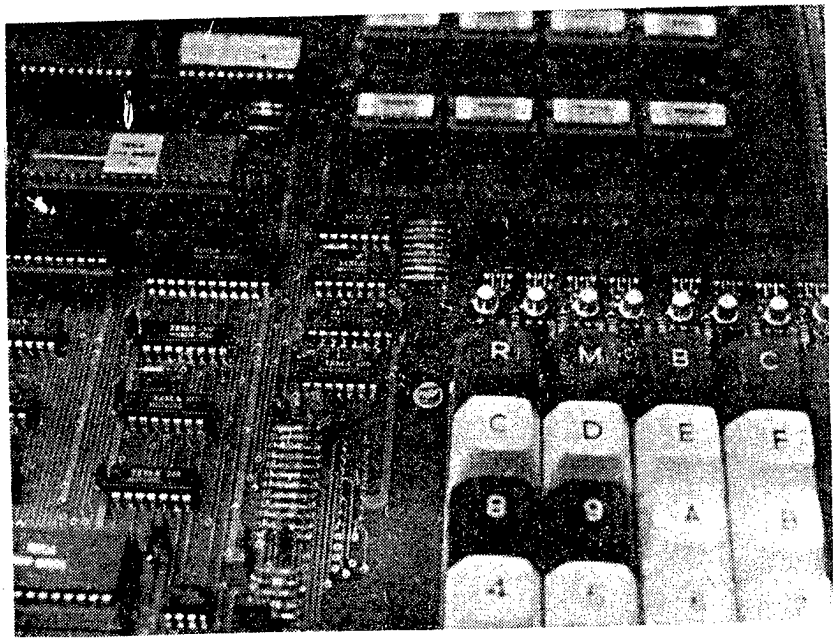


Figure 89. Close-up view of the plate of the VUVT training computer

4.2 Software

4.2.1 DOS MVS

DOS MVS is a disk-type operating program and is used for the generation of programs in the MVS II developmental system.

The key function of DOS MVS is the control of systemic resources of MVS and control of sets stored on floppy disks.

The operating system is divided into a monitor and the operating system itself.

The monitor is a residential program with an extent of approximately 2 KB, is stored in EPROM memory and provides for the performance of the basic functions of the operating system. Part of the monitor consists of service programs for input/output devices of the developmental system, including operator's terminals.

The monitor further provides for:

--display and modification of contents of memory and registers of the single-plate microcomputer,
--input/output of user program,
--printout of user program,
--pacing the user program, setting stops in the program,
--editing of program in machine code stored in memory,
--shifting of memory sectors.

The monitor also contains a number of additional subprograms designed to make the user's work easier. Communication with the monitor occurs by means of the operator terminal.

Part of the operating system itself is permanently stored in the working memory storage (residential part), while other programs are fed into the working memory storage from a disk memory in case of need.

The basic DOS MVS instructions include:

--FORMAT: initiates a new floppy disk for use in the system, also facilitates copying of sets;

--DEBUG: introduces a designated program from disk memory into internal memory and transfers control to the monitor for tuning or start-up of program;

--SUMBIT: provides for the performance of a set of instructions stored in disk memory;

--DIR: directory--provides information about the name, size and other characteristics of a selected set on a disk;

--COPY: provides for copying of sets and transmission of sets among individual peripheral systems;

--DELETE: makes room on floppy disk for another set;

--RENAME: renames sets stored on disk;

--ATTRIB: provides for marking of sets with various indicators, e.g., protection against entry;

--HEXOBJ and OBJHEX: provide for conversion between hexadecimal form and objective form of DOS MVS.

The DOS MVS operating system also includes the following programs and programming languages:

--LIB,
--LINK,
--LOCATE,
--MVE 80,
--control program for programmer,
--editor,
--EDIT 80,
--arithmetic library,
--Macroassembler,
--PL/M 80,
--BASIC 80,
--FORTRAN 80,
--PASCAL 80.

LIB--Librarian

Librarian LIB provides for the generation and maintenance of systemic and user programs and subprograms; library modules can be used as input modules for connecting programs.

The LIB program uses the following instructions:

CREATE--generation of librarian for set LIST--listing of library modules, ADD--incorporation of module in library EXIT--return from LIB program, DELETE--cancellation of module in library.

LINK--Connecting Program

The LINK connecting program makes it possible to connect various modules into one resultant transferable module. Individual modules can be generated in varying languages. This means in practice that the entire system of programs can be generated in modular form and individual modules can be programmed in different languages, e.g., control structures in PL/M 80 and arithmetics in FORTRAN 80. Each module can then be individually translated, tuned and only in the end is the resultant program generated (see Figure 90).

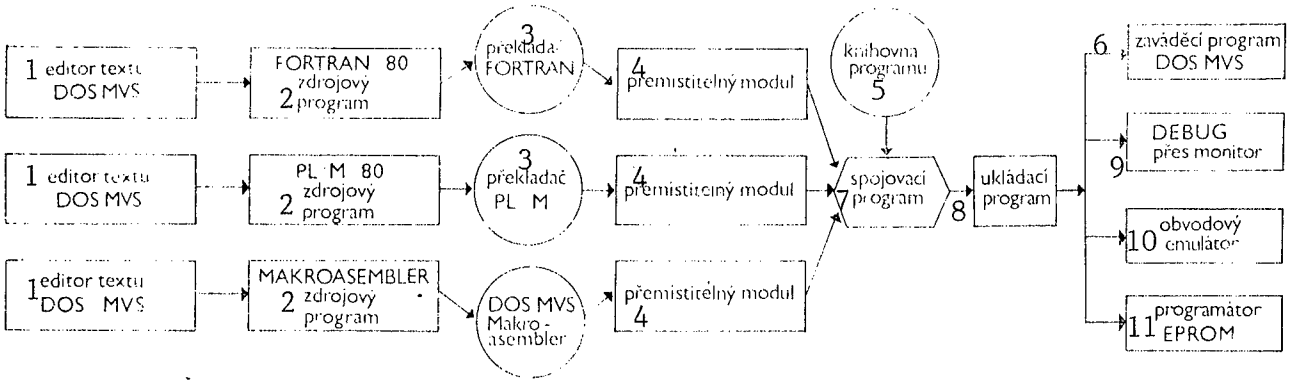


Figure 90. Diagram showing development of programs under DOS MVS

Key:

1. text editor
2. source program
3. translator
4. transferable module
5. program library
6. lead-in program
7. connecting program
8. storage program
9. via monitor
10. circuit emulator
11. programmer

LOCATE--Storage Program

The LOCATE storage program transforms a transferable output module into a target module in absolute configuration, which can be started up and run.

Individual segments of the module can be hereby located under various memory addresses, e.g., performance code into EPROM memory, data and storage into RAM memory.

MVE 80

The MVE 80 control program for emulator is a piece of software controlling the functioning of the MVE emulator. It allows the prototype system being developed to make use of all hardware and software systemic resources of MVS and also facilitates its diagnosis. The prototype software can be stored in MVS working memory storage and can be run as if it were located in the prototype system. The emulator makes it possible to generate software for systems which have not been technically completed as yet. Emulation can progress in real time or in step-by-step mode. It can be stopped at any time, determine the state of the prototype and, eventually, operation can be resumed.

The MVE 80 makes it possible to display and also change many of the system properties--state of registers, contents of memory, contents of recorder, state of inputs/outputs, etc. In addition, it can provide information about the duration of emulation, the address of the last emulated instruction, the last 44 emulated machine cycles, immediate depth of subprogram address, symbolic names and their values in table of symbols.

The ME 80 has its own system of error reports.

Control Program for Programmer

This program controls the operation of the peripheral system--PGM 08 programmer--and, depending on user needs, facilitates the programming of EPROM memory.

Editor

The text editor offers the possibility of simple editing at line level, i.e., input, output and handling of text. The text editor makes it possible for a program to be entered from a keyboard, perforated tape reader, floppy disk memory or be put out to display, printer, perforated tape punch or floppy disk memory.

Editor instructions makes it possible to:

--introduce a text set from the input/output system into the memory,
--setting of an editing mark in the text at any random position,
--insertion of texts into sets,
--deletion of a chain of symbols from text,
--retrieval of a set of symbols,
--substitution of one chain by another, etc.

Editor instructions can be assigned independently or they can be combined into chains of instructions.

EDIT 80

EDIT 80 is a screen-oriented text editor with editing in screen or instruction mode; it permits insertion, shifting, erasure and other modification of texts in a simple manner. EDIT 80 permits operation in screen or instruction mode.

In screen mode it is possible to display an ASCII set, move the carrier at random to any symbol in the text and carry out the insertion or erasure of text.

In instruction mode instructions can be used to shift or copy text and parts of words as well as operation with sets on a floppy disk.

Arithmetic library

The ARITM library contains a whole series of programs facilitating arithmetical computations with a floating decimal point.

Macroassembler

Macroassembler is a program which receives the source text of a program written in a symbolic language and in two runs generates the requisite machine code. A translator version under DOS MVS generates a transferable program which can be segmented and individual modules can be combined to form an absolute targeted code. Macroassembler with the use of MAKRO FILE facilitates the extensive use of stored text segments and control of translation.

PL/M 80

PL/M 80 is a higher programming language of the PASCAL type offering the possibility of operation in real time. It is based on the PL/1 language.

BASIC 80

BASIC 80 is an expanded version of the standard BASIC language. In comparison to the standard version it contains a number of systemic instructions facilitating interactive operation and instructions for tuning of programs, for line-level editing, etc.

It permits the formation of sequential data sets containing numbers or chains of maximum length of 255 symbols.

PASCAL 80

PASCAL 80 is an expanded version of the standard PASCAL language. The PASCAL 80 system consists of an interpretive system and a compiler. The PASCAL 80 compiler translates a source program into a pseudocode which is interpreted and run by the interpretive system. The printout of the source program, including error reports, is carried out during translation.

A text editor is used for the generation of a source program.

Programs in PASCAL 80 can be segmented (overlap procedures), which allows very extensive programs to be run.

PASCAL 80 includes effective means for monitoring programs, monitoring their selected parts, interruption at a random point, etc.

FORTRAN 80

The FORTRAN 80 translator translates the source code of FORTRAN into machine code. It translates FORTRAN program units into tranferable target modules for use on 8-bit SM 50/40 systems and can generate target code modules, printout of source and translated code and printout of cross references.

The translator works under the DOS MVS operating system. Target modules generated by the translator can work under DOS MVS or in ERC real time execution.

The translator comes equipped with a set of transferable library modules which are supplemented by systems operating in real time, including arithmetic with floating decimal point, with mathematical functions input/output with sequential or direct access (with or without formatting) and elementary interaction with the DOS MVS operating system or ERC.

Operations with floating decimal point can be performed by subprograms either by means of the mathematical module or by subprograms that form part of the translator.

The DOS MVS operating system can be used with the MVS II developmental system.

4.2.2 LOS MVS

The perforated tape version of the LOS MVS operating system for the MVS I developmental system performs the same functions as DOS MVS. In view of the limited hardware possibilities of the MVS II developmental systems, the possibilities offered by LOS MVS are more limited than DOS MVS.

Nevertheless, even LOS MVS offers a possibility for generation of software for the SM 50/40 systems.

The LOS MVA operating system includes the following parts:

--monitor,
--Macroassembler,
--text editor,
--BASIC 80 language interpreter,
--control program for emulator,
--control program for programmer.

4.2.3 Real Time Execution

ERC real time execution modules and programming language modules form the basis for setting up microcomputer systems based on the SM 50/40 (SM 53/10) modular assembly that operate in real time. Specific software for a certain application made up of ERC library modules is called Real Time System (SRC).

Figure 91 shows the developmental diagram of the origin of the Real Time System. The system's parameters are selected during communication. The output of a connected program can be located in PROM memory or can be introduced by a lead-in program into RAM memory.

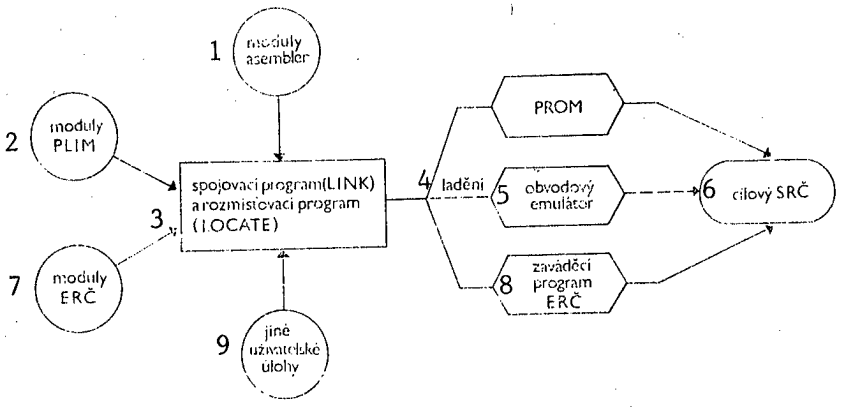


Figure 91. Developmental diagram of SRC

Key:
1. assembler modules
2. PLIM modules
3. LINK and LOCATE programs
4. tuning
5. circuit emulator
6. target SRC
7. ERC modules
8. ERC lead-in program
9. other user tasks

Real time execution permits the simultaneous running of several independent tasks (multitasking) on the basis of priorities, interruption, organizes communication between tasks and communication between microcomputer and external environment.

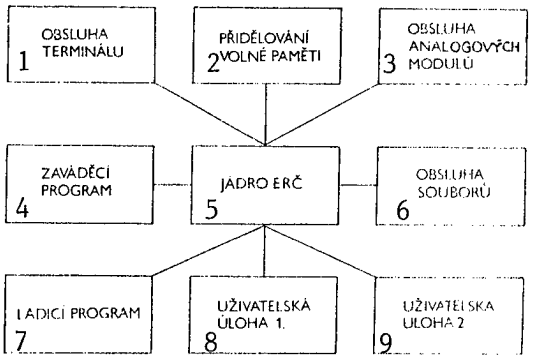


Figure 92. ERC configuration

Key:
1. terminal operator
2. free memory allocation
3. analog modules operator
4. lead-in program
5. ERC core
6. set operator
7. tuning program
8. user task 1
9. user task 2

The core requires approximately 2K byte of ROM memory and permits the devising of a real-time system even with the processor module; it provides for the following functions: system initiation, control and synchronization of tasks, system timing, exchange of system information.

Systemic tasks include:

--terminal operation facilitates communication of the operator with the system;

--set operation simplifies operation with sets on a flexible disk in real time without interruption of other systemic functions; these sets are compatible with those generated under DOS MVS;

--lead-in program serves to feed application programs into the memory of the running system;

--the tuning program for tuning in real time can cooperate with the MVE emulator.

The allocation of free memory makes the user's work with the system easier.

The operation of analog modules-inputs and outputs provides for the following functions:

--repeated input from one channel,
--input from successive channels with constant gain,
--input from successive channels with variable gain,
--input from selected channels,
--input via selected channels.

The read data are recorded in a sector predetermined by the user.

The systemic tasks can be supplemented by user tasks. Individual tasks in the system communicate with the ERC core by calling the systemic directives of the core by the instruction CALL that perform individual functions of the core. Communication between tasks occurs with the aid of the mechanism MESSAGE--BOX. A special case of BOXES are INTERRUPTION BOXES into which are fed MESSAGES and interruptions. Tasks running under ERC control have a priority (0-255) assigned to the user.

The user can utilize in his programs ERC instructions which provide for basic functions of the system. Individual instructions can be written in PL/M 80, Macroassembler, FORTRAN 80 and BASIC 80.

ERC also includes testing and diagnostic programs for verification of correct functioning of the system and its diagnostics.

Requirements on the size of memory are shown in Table 8.

Table 8. Requirements on ERC modules' memory extent

1 Přibližné požadavky na paměť v bytech								
2 modul	3 jádro	obsluha terminálu min. 4	obsluha terminálu max. 5	přidělování volné paměti 6	7 obsluha souborů	8 obsluha disku	obsluha analogových modulů 9	zaváděcí program 10
PROM	2K	600	3K	1K	5,5K	700	800	600
RAM	250	120	950	250	1,6K	100	50	900

Key:
1. approximate requirements on memory in bytes
2. module
3. core
4. terminal operation min.
5. terminal operation max.
6. free memory allocation
7. set operation
8. disk operation
9. analog modules operation
10. lead-in program

A specific user SRC is generated from the ERC on the MVS II developmental system under control by DOS MVS, and on the operator's terminal of TOP process in the SM 53/10 system with basic software for SM 53/10.

4.2.4 MUOS

The MUOS operating system is a flexible, multiuser disk operating system designed for programmable terminal operation. This operating system makes it possible to transfer any random program in machine code to a user task or to a transferable task that services several users.

The operating system includes a text editor, the TL higher programming language, Macroassembler, program for operation with disks and user programs. It has at its disposal means for generating reentry programs that can be used by several users simultaneously.

Up to seven input/output systems-terminals can work for MUOS with the use of input and output interruptions. Six uninterruptable systems can be connected simultaneously, as can up to eight external memory units with a floppy disk. The users can have access either all to one disk or individually to different disks.

With the use of the so-called overlap function more than one task can be run on one terminal. All tasks are located in the memory so that the number of possible tasks depends on the size of memory in the system and on the extent of individual tasks.

Real-time clocks have the highest interruption priority and are the source for planning all tasks. Tasks have the same priority, time is allocated cyclically with the use of the ROUND-ROBIN system.

The following programs are implemented under the operating system:

--TEXTED: a text editor serving for writing programs in TL language, assembler programs, documentation of ASCII sets. TEXTED can be used by several users simultaneously;

--ASSEMBL: a two-run Macroassembler translator; in the first run is generated a table of signals and in the second run the target module;

--FILLES: a set of programs for operation with floppy disks which provides for the following functions: directory printout, erasure of sets, renaming, printout of the number of free sectors, etc.

Under the operating system there also work a number of subprograms that provide for the printout of ASCII sets, printing of a translated assembler program, connecting of transferable programs, copying of disks, copying of sets on one disk or onto another disk, etc.

The MUOS operating system requires for its functioning an SM 50/40 microcomputer with external disk memory, which can be expanded by a maximum of three serial terminals.

TL Programming Language

The higher programming language TL (Terminal Language) can be used under the MUOS operating system. It resembles the programming language BASIC and with its block structure corresponds to the ALGOL language.

The language's arithmetic allows work with precision of up to 55 digits. The language makes it possible to operate with sets, carry out arithmetic and logic operations, operation with chains, operation with various functions with up to 255 dimension matrices, etc.

For its functioning it requires the SM 50/40 microcomputer equipped with the MUOS operating system.

4.2.5 MIKROS

The MIKROS operating system is functionally compatible with the CP/M operating system in 2.2, which is currently the most widely used operating system for microcomputers worldwide.

MIKROS is a single-user disk-oriented operating system which is characterized by

--simplicity,
--general and all-purpose applicability,
--independence of hardware.

It takes up approximately 6K bytes of internal RAM memory and is modular, whereby linkage to hardware is concentrated in one module, which can be easily modified.

It offers a wide scale of services which cover the usual needs of user tasks. In view of the modular structure of the operating system's core, the assortment of these services can be expanded in accordance with the user's needs.

The operating system can be divided into four parts:

--BIOS input/output module, which forms an interface between the system and hardware. It includes basic control input/output programs for standard peripheral units:

  --floppy disk,
  --keyboard and screen,
  --printer,
  --tape perforator and reader;

--BDOS basic module of the operating system's core, which provides for systemic calls and operation with sets on disk;

--CCP interpreter of instructions, which interprets and performs instructions fed into the operating system from the terminal's keyboard;

--TPA operating spheres for nonresidential parts of MIKROS and user programs.

The set control system under MIKROS makes it possible to serve up to 16 external disk memories with a maximum capacity of 8M bytes each.

Each of the disk sets can be marked "systemic" or "protected against entry."

Among the residential functions of the operating system are:

--DIR--information about sets on disk,
--TYPE--display of called set on screen,
--REN--renaming of set,
--ERA--erasure of set,
--SAVE--storage of data from operation on a disk under an assigned name.

Nonresidential functions of the operating system provide the following programs:

--ED--text editor facilitating the generation of sets and changes in sets,
--PIP--conversion program for printout on screen and through printer, copying of sets, connecting of sets, etc.,
--STAT--information about free space on disk, about sets, about individual data and also about assignment of logic names to physical systems,
--LOAD--introduction of program into memory,
--DUMP--hexadecimal display of set on screen,
--SLAP--testing and tuning of programs,
--SUBMIT--performance of instructions and sets of instructions,
--LINK 80--connecting and lead-in program,
--LIB 80--library control.

Other nonresidential functions of the MIKROS operating system can be provided by the following supplementary software:

--DATOS--set of programs for automation of adminisrative operations,
--DYNAMIT--multipurpose sorting program.

The following translators are implemented under the operating system:

--MASH--Macroassembler for the generation of programs in symbolic language,
--FORTRAN M,
--P/BASIC,
--G/BASIC,
--K/BASIC,
--COBOL 80.

Also available is a library of basic statistical methods and a numeric library in the P/BASIC language.

The MIKROS operating system can be used on the SM 50/40 computer or the MVS II developmental system.

DATOS

DATOS is a set of programs for processing of data and texts into random forms.

DATOS is intended for work under the MIKROS v 2.2 operating system. It forms a retrieval, modification and updating system for data sets.

Properties of the DATOS set of programs:

--program service takes the form of reports and instructions fed via keyboard and displayed on a screen terminal;

--generated data sets comply with the conventions of the programming languages FORTRAN, COBOL, BASIC;

--input data for processing can be formatted at random;

--input data can be verified. The program makes it possible to permit the entry only of data that conform to a set requirements (masks, setting of obligatory chains, etc.);

--it is possible to search for a selected entry (sentence) in several ways and to edit the retrieved entry at random (insertion, erasure, modification of symbols, etc.)--all the functions of a standard text editor;

--it makes it possible to preset a mask for input data (prescribed format); this function offers advantage to operators by limiting of errors;

--it makes possible user protection of sets stored on a disk, meaning that access to sets is protected by user identification.

Typical hardware configuration:

SM 50/40 microcomputer or MVS II developmental system.

DYNAMIT

DYNAMIT is intended for work under the MIKROS operating system, see 2.2. It performs sorting, arrangement of sets, formatting conversions of all kinds of sets for use in programs written in BASIC, FORTRAN, and COBOL as well as operation with text sets.

Properties of the DYNAMIT program:

--sorts and combines up to 32 sets into a single input set with dynamic use of disk memory depending on the size of working memory storage;

--sets can contain data in ASCII, BCD and/or binary code;

--it processes logic entries up to 4096 symbols long;

--sets can contain data with fixed (given) length, of varying length, limited by a control symbol as well as entries for processing by a program in COBOL;

--it is possible to specify key fields containing up to 32 keys, each with symbols indicating the type of data;

--key data can be ASCII chains, ASCII numerals, BCD (for COBOL condensed decadic form) or binary.

Typical hardware configuration:

SM 50/40 microcomputer or MVS II developmental system.

FORTRAN-M

FORTRAN-M is a translator designed to work under the MIKROS operating system. It translates source-type programs in FORTRAN into a format with transferable pages, at the same time compiling the translation procedure.

Input sets for the translator are located in a floppy disk memory. The translator is supplemented by a library of programs which facilitate the use of formating functions, standard transformation functions and input/output operations.

Typical hardware configuration:

SM 50/40 microcomputer or MVS II developmental system.

P/BASIC

P/BASIC is an expanded version of the standard BASIC language. The expansion involves the processing of text information and processing of data while controlling processes in real time. In comparison to the standard version, the P/BASIC includes a number of systemic instructions that make interactive use of the language easier, and it is also equipped for program tuning.

P/BASIC makes it possible to read and modify any point in the memory, input and output from individual input/output units, manipulation with bits, time delay of programs, interruption of programs, and makes it possible to call from its program a program in Macroassembler.

G/BASIC

G/BASIC is an expanded version of the BASIC language with graphic instructions now in preparation. The language will be used for the operation of a semi-graphic terminal or a drafting system.

The graphic instructions of the language can be divided into groups of instructions for drafting and writing.

Instructions for drafting make it possible to:

--determine the starting point of a system of coordinates,
--plot x and y axes anywhere on the drafting area or on the screen,
--plot points in relation to the selected starting point of coordinates.

Instructions for writing permit the use of the screen for standard display of symbols transmitted from keyboards.

K/BASIC

This compilable version of the BASIC language, i.e., K/BASIC, implemented under the MIKROS operating system brings--in addition to the advantageous properties shared by the preceding variants of the BASIC language, such as simple mnemotechnics, operation with chains and easy formatting of outputs, etc.--some expansions:

--identifiers 31 symbols long,
--nonobligatory numbering of lines,
--multi-instruction lines and multiline instructions,
--cycle with logic condition (WMIIE...WEND),
--printout of cross references,
--computation of numerical and chain variables and the so-called integral variables,
--multiline functions with transfer of parameters defined by the user,
--potential for storage of whole-line input chains,
--formatting of printout.

K/BASIC is suited for computations of an economic, scientific and technical character, for operation with text chains, etc., because it combines the advantages of speed of compiled programs and simple generation of programs.

K/BASIC includes two modules:

--compilation module,
--interpreting program.

Source text generation is done with an editor. The generated source program is translated by a compiler and starts up the interpreting program.

K/BASIC permits operation with sets on a floppy disk with sequential or random access; the compiler makes it possible to connect programs from other sets in BASIC. The range of K/BASIC language application is enhanced by its systemic instructions.

COBOL 80

The COBOL 80 compiler reads the source program written in COBOL 80 and generates a transferable version of the program and the translation procedure.

COBOL 80 is based on ANSI COBOL 1974; in comparison with the latter standard, some of its modules are not implemented at all, some only at a lower level. However, it does have some additional expansions, such as, e.g., interactive operation.

TEXT 01

The program-equipped TEXT 01 facilitates the processing of text information.

TEXT 01 works under the control of the MIKROS operating system.

The software services individual input/output systems and also contains a module for cooperation with the user and its own text processor. The latter makes it possible to select one of four basic modes of operation:

--entry--serves for making entries into a previously generated text, generation of new text, change of name, change of password. It permits graphic modification of text--beginning of paragraph, accentuation of text, page ending, return to offset, return to beginning, skipping, pagination, deleting lines, etc.;

--printout--serves for the selection and printout of text on a printer, including selection of graphic format (number of letters per line, number of lines per page);

--catalogue--serves for display of data about stored text;

--erase--serves for elimination of certain parts of text.

The mode for cooperation with the user is set automatically at the system's start of operation, or after completion of one of the four basic modes. Individual sets are protected by a password against misuse by an unauthorized person.

4.2.6 Basic Software for SM 53/10

The basic software includes sytems for the support of TSP terminals for contact with the environment and for the support of operator's terminals in the TOP process. In view of the character of the SM 53/10 system, it contains a set of programs which provide for mutual communication among these program products.

Software for the support of the operator terminal in the TOP process makes it possible to:

--tune applicationally oriented software,
--generate the requisite variant of an information or control system,
--control the process itself.

In view of the TSP terminal configuration, TOP terminals perform the tuning of software designed for TSP.

The ERC real-time execution is used in the operation of the TSP terminals for contact with the environment. ERC provides the requisite services for the operation of the individual modules and units for contact with the environment; a more detailed description was offered in the preceding section.

Software for communication provides linkage between individual terminals, i.e.:

--TOP in the function of a central station supervising control of a long-distance line; it operates in a cyclic mode of call signs in which it inquires into the state of other terminals. It processes this information and assigns control functions to selected terminals which it provides with messages, and also provides for the transmission of emergency information in the system;

--TOP in the function of a control station, whereby it can obtain data prepared by a subordinate terminal and can transmit data to the subordinate terminal;

--TSP as a subordinate station prepares messages or sets of messages for the control terminal whereby a system of priorities provides for the transmission of important messages ahead of data messages.

4.2.7 MODUS

MODUS (Microcomputer-Oriented Distributed User System) is software for the generation and operation of specific application software of information or control systems.

It is designed for the SM 53/10 microcomputer distributed system.

The MODUS system has a modular assembly structure, the basic elements of which are formed by program modules of two types:

--systemic,
--applicational.

Systemic modules are independent of application. They control in a standard manner the transmission of information between individual TSP and TOP of a distributed network and between the computer system and a technological process. Applicational modules are modules devised to meet the specific needs of control systems of a certain category of technological processes. While MODUS does prescribe a precise form for applicational modules, their thematic content is determined by the user. The contents of modules are selected so as to meet as best as possible the needs of the user in a given area of application, particularly with regard to their degree of complexity.

As modules are formed by one or more elementary algorithms, whereby the modules can form entire control networks, the applicational module is designed to perform certain characteristics groups of elementary functions with repetitive occurrence in control of technological processes of a given class.

It stands to reason that the requirements of functions built into the module can show significant differences for varying technological processes. From the viewpoint of the area of application, there occurs the generation of sets of applicationally-oriented modules.

The software configuration of a specific TSP terminal is then determined by:

--the selection of a set of modules,
--defining admissible types of magnitudes and, thus, also the possible information linkages in the network.

Thus, with the use of all-purpose software, it becomes possible to devise applicational software "made to order" for the given control system.

The MODUS system is formed in principle by:

--defining functions and,
--interpretive functions,

whereby the latter two are accessible by key selection only to the level of:

--systemic engineer, or
--process operator.

Resources at the level of the system engineer include:

--the system engineer's language oriented toward the technological process. With the aid of a semigraphic monitor and TOP keyboard it makes it possible to define in a conversational manner the selected strategy of monitoring and control of a technological process. It facilitates the generation and connection of control networks (defining of modules, their linkages, specifications).

In this mode the MODUS system feeds various forms onto the screen, and by filling them out the process of defining the system is implemented. At the same time, the system controls the admissibility of responses, adherence to certain limitations, mutual linkages to previous responses, etc. Values of the filled-out data are fed into the input lines of the screen and are controlled prior to being transferred to the requisite part of the form. The operator is informed of any detected error.

--system engineer's language oriented toward process operation. It facilitates the conversational defining of images required by the operator, routines, emergency reports and operator functions. Operator images are used, e.g., for operator communication with the system during its operation and are composed of two parts:

--static background,
--dynamic foreground.

Static background is formed by printout from the keyboard onto the screen. It is possible to use both alphanumeric and graphic symbols. The background

of the image is then formed by a permanent display of, e.g., tables, diagrams representing key technological junction points, etc. At the same time, a selection of points for displaying the actual values of certain magnitudes is made. These magnitudes are defined during the generation of foreground in the next implementation step.

The resources at operator's level include:

--Operator functions:

--call-up of image on screen,
--output of routine,
--copy of image from screen to printer,
--changing the value of a called up magnitude in the image,
--setting of logic value by functional key,
--acknowledging of alarm,
--printout of archive set from disk through the printer;

--Automatic functions of the system:

--entry of information about alarm into the archive set,
--entry about operator's course of action into the archive set,
--printout of archive set when sector on disk in filled to capacity;

--Functions activated by defined states of magnitudes:

--illumination of optical signalization with eventual acoustic signalization,
--flickering of displayed magnitude when reaching emergency state,
--image call-up,
--procedure output;

--Functions actuated in dependence on time:

--output of frequency procedures (e.g., related to work shifts).

Thus, the microcomputer-oriented distributed user system MODUS simplifies operations in the generation of a control system. The generation of a MODUS version for a given class of technological processes--meaning primarily the generation of the requisite applicational modules--practically eliminates the need for programming, which is replaced by a conversational definition of the type of control and operation of the system and by a definition of operator's resources (images, routines, functions of keys and alarms).

In this way the MODUS system approximates the thinking process of technicians working in the sphere of automation who are used to combining control systems from individual control mechanisms and similar means of automation.

Continuous Technological Processes

Continuous technological processes constitute a traditional area for all-purpose programming systems. Among others, the following modules were devised for synthesis of control of such processes:

--SNIM module for standard initial processing of analog magnitudes. This module performs the following functions:

--linearization,
--conversion to technical unit,
--filtration,
--testing of technological limits,
--testing of trends;

--REG 1 module for standard dynamic control (numerical version of PID controller, including various modifications and specializations). The module performs the following functions:

--bilateral limitation of requested value (clamping),
--limiting the rate of change of requested value (ramping),
--computation of the manipulated variable (the control algorithm itself),
--testing of the absolute value of a control deviation.

The module facilitates the impactless coupling and cascading of control loops.

--REG 2 module for standard static control (ratio control, differential control and other nondynamic control algorithms). The module performs functions analogous to that of the REG 1 module and has similar properties;

--VYST module for computer control of CM and CMA stations of a certain type. The module performs the following functions:

--bilateral limitation of the requested setting of an action element,
--computation of deviation in the setting of an action element in CM or CMA station units,
--bilateral limitation on the rate of change in the position of an action element,
--conversion of the permissible change in the position of an action element to signals required by CM or CMA stations.

Figure 93 presents an example of a technological process involving the mixing of liquids. Figure 94 shows the diagram of a control network for simple cascade control. In addition to the above-listed applicational modules, the control network makes use of the following systemic modules:

--VSPO (INput FIeld [in Czech]) module for transmission of information into the given network of a given terminal (in the example in Figure 94 it serves to call up requested values by the operator);

--VYPO (OUtput FIeld [in Czech]) for transmission of information from the given network of a given terminal (in the example shown in Figure 94 it serves for monitoring of controlled and even other magnitudes by the operator);

--AVST module for analog inputs;

--AVYS module for analog outputs.

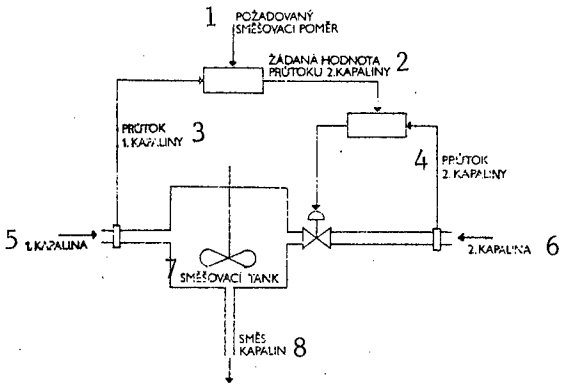


Figure 93. Mixing of two liquids in a given ratio

Key:
1. required mixing ratio
2. required flux value for 2d liquid
3. flux of 1st liquid
4. flux of 2nd liquid
5. 1st liquid
6. 2nd liquid
7. mixing tank
8. liquid mixture

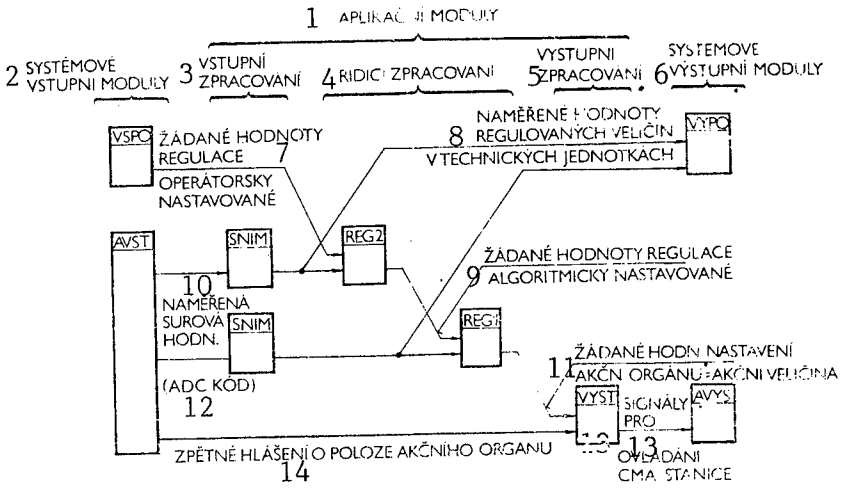


Figure 94. Diagram of control network with cascade control

Key:
1. applicational modules
2. system input modules
3. input processing
4. control processing
5. output processing
6. system output modules
7. requested control values set operator
8. measured values of controlled magnitudes in technical units
9. requested control values set by algorithms
10. measured raw value
11. requested value of action element setting=manipulated variable
12. ADC code
13. signal for CMA station control
14. feedback report about position of action element

Let us point out that Figure 94 shows merely a rough outline of a control network. The numbers of inputs and outputs of individual blocks, just as the numbers of information linkages between blocks, are actually much higher.

The SNIM, REG 1, REG 2 and VYST applicational modules are comprehensive in nature: each of them performs a characteristic sequence of functions repeatedly encountered in the monitoring and control of continuous technological processes. However, these multifunctional modules can be alternatively replaced by a greater number of simpler unifunctional modules. This will make the equivalent control networks more complex. It is up to the user to determine the suitability of one or another set of applicational modules for the synthesis of his control system.

Discrete Technological Processes

As was the case with continuous processes, versions of the MODUS system can be set up for discrete processes or for cases where the system provides for both continuous and discrete control.

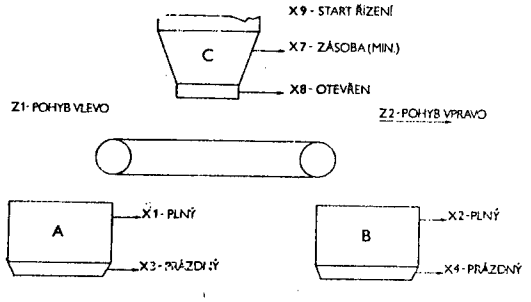
Discrete control can use:

--logic functions (combination),
--sequential functions (generating sequences of logic signals with memorizing of internal states).

In this way it is possible to define systems that provide certain sequences of process signals during start-up or stopping of technological units, control of discrete technological processes, or that use sequential control within the system for the activation and deactivation of control networks.

To offer an example of discrete control, let us use a technological unit with storage tanks, outlined in Figure 95, and its control network, shown in Figure 96.

The system automatically refills storage tanks A and B from storage tank C by controlling the direction of the conveyor's motion.



Key:
X9: Start of control
X7: Supply (min.)
X8: Open
Z1: Move to left
Z2: Move to right
X1: Full
X2: Full
X3: Empty
X4: Empty

Figure 95. Control of storage tanks

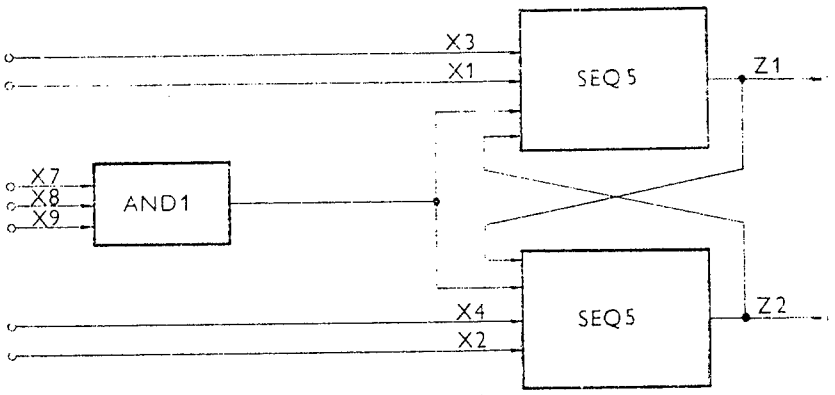


Figure 96. Control network for storage tanks (without systemic blocks)

Key:

X9: Start of control	Z1: Move to left	X2: Full
X7: Supply (min.)	Z2: Move to right	X3: Empty
X8: Open	X1: Full	X4: Empty

4.2.8 Cross-Programming Systems

Cross-programming systems are designed for operation on SM 3-20, SM 4-20 and other minicomputers. Under control of the FOBOS operating system they make it possible to develop software for the SM 50/40 microcomputer. They consist of:

--Macroassembler,
--simulator,
--retranslator.

A standard editor of a minicomputer can be used for the generation of programs. Macroassembler is a program written in FORTRAN IV.

During the tuning of programs the simulator permits:

--input of data in linear or hexadecimal form with selection of computer address;

--input of data from keyboard of terminals, perforated tape, disk memory;

--start of simulation from random address;

--stopping of simulation on a random address, printing out of data about the state of the program, scanning and changing the contents of memory cells and of indicative registers;

--storage or cancellation of program sectors with automatic address substitution of the simulated program;

--storage of program in a disk or tape memory.

The retranslator permits the dumping of the program to a terminal or to a printer.

5. Operational and Installation Conditions

The subsequent text offers a detailed description of the operating and installation conditions for minicomputer systems SM 3-20, SM 4-20, SM 52/11 and derived types (PPPD-1 and others).

Installation conditions for microcomputer systems must comply with analogous valid regulations. Part 5.2 deals with operational conditions for these systems.

5.1 Operational and Installation Conditions for Minicomputers

Structural Considerations

The basic configuration of SM 3-20, SM 4-20 or SM 52/11 computer systems calls for an area of approximately 20-25 m^2. For expansion systems, such as printers, large capacity disks, additional casings, etc., provisions must be made for additional space commensurate with the number and type of such systems. The ceiling height must conform to valid hygienic regulations, i.e., 2.70 m in spaces with air conditioning and an area up to 100 m^2.

The required standardized load on the floor must be determined on the basis of the configuration of the computer and its proposed distribution (a rule of thumb value is on the order of approximately 3-6 kN/m^2). It is recommended that the room be provided with a double floor made of nometallic boards, or metal boards coated with an insulating material that prevents the formation of static electricity. In cases where a double floor is not considered, provision must be made for simple cable bedding and grounding; the type of the floor covering used must exclude the possibility of the formation of static electricity. The floor itself must be properly grounded.

The walls and ceiling of the room must have a dust-free, easily cleaned surface. Noise attenuation linings for walls are not necessary and where small spaces are involved they are not very effective. However, acoustic ceiling design in combination with lighting can be helpful.

Electric Installation

Electric installation must comply with valid standards. The power supply system is 3 X 380/220 V, 50 Hz, whereby the power feed for the computer system must be independent.

The distributor must be fed independently from the main distributor of the facility or from a transformer station to prevent interference in a pulse-type network from induction-type appliances. Protection is provided by zeroing. An independent grounding conductor must have resistance $\leq 4\ \Omega$.

The entire computer system, including peripheral equipment, must be connected to the same phase of the power distribution network, except large-capacity disk memories, which require three-phase feed. In expanding the system by remote peripheral equipment, the latter can be connected to another distribution phase.

The computer system is capable of operation during feed voltage changes from +10 percent to -15 percent of nominal voltage and nominal frequency tolerance of +1 to -1 Hz. From the viewpoint of illumination design, computer rooms belong to category III, with high demands on lighting. The practically verified and recommended illumination value for operation with windows is 650 Lx, in windowless operation 850 Lx.

It is imperative that all electric appliances installed in the room (computer, socket and light distribution and air conditioning) be disconnectable by a manual emergency push-button directly in the room as well as along emergency escape routes.

Air conditioning

Operational and normal climatic conditions are prescribed for the operation of SMEP computers by their producer from the viewpoint of requirements on ambient atmosphere.

Operational climatic conditions:

air temperature	+5°C to +40°C
relative air humidity	40-90 percent at 30°C
atmospheric pressure	84-107 kPa
air pollution (dust nuisance)	max. 1 mg/m^3 at particle size of 3.10^6 m

Improved reliability of the system can be expected under normal climatic conditions.

Normal climatic conditions:

air temperature	20°C ± 5°C
relative air humidity	65 ± 15 percent
atmospheric pressure	84-107 kPa
air pollution (dust nuisance)	max. 1 mg/m^3 at particle size of 3.10^6 m

However, of essence is the fact that in view of the prescribed conditions regarding air pollution, air conditioning is absolutely necessary if operational or normal climatic conditions are to be maintained.

The permissible concentration of aggressive substances in the air is:

sulfur trioxide (SO_3)	max. 20 mg/m^3
sulfur dioxide (SO_2)	max. 2 mg/m^3
ozone (O_3)	max. 0.2 mg/m^3
hydrogen monosulfide (H_2S)	max. 20 mg/m^3

Safety and Hygiene of Work

From the viewpoint of noise pollution and vibrations, their respective levels at points of permanent operation must not exceed the values stipulated by decree of the Ministry of Health. Spaces for the operation of computer systems must meet all hygienic requirements on operational environment and other recommendations.

Fire Prevention

Spaces containing installed SMEP computers must meet from the viewpoint of fire prevention the standard regarding the fire safety of structures and all attendant standards. The requisite fire prevention inspectorate must be consulted about a system for electric fire signalization. The most suitable manual fire extinguishers are foam-type.

5.2 Operational Conditions for Microcomputers

The SM 50/40 and derived types of microcomputer systems (programmable terminal, TOP in the SM 53/10 system, etc.) with external floppy disk memory can be operated under the below specified conditions:

Operational conditions:

air temperature	+5°C to +40°C
relative air humidity without dew formation at 30°C	40 to 90 percent
temperature gradient	10°C/hour
atmospheric pressure	84 to 107 kPa
admissible dust nuisance	max. 1 mg/m^3
size of dust particles	max. 3.10^6 m
operating position of modules	horizontal, vertical
mechanical impact resistance	max. 1 g
admissible concentration of aggressive substances	SO_3 max. 20 mg/m^3
	O_3 max. 0.2 mg/m^3
	H_2S max. 20 mg/m^3

Permissible frequency vibrations of microcomputer modules in operation is up to 25 Hz, with maximum amplitude of 0.1 mm throughout the entire frequency range.

Normal conditions:

air temperature	+20°C ± 5°C
relative air humidity	65 ± 15 percent
atmospheric air pressure	84-107 kPa
admissible dust nuisance	max. 1 mg/m^3
size of dust particles	max. 3.10^6 m

For SM 50/40 cassettes and also for some other derived products which are not equipped with an external floppy disk memory identical operating conditions apply, with the proviso that admissible dust nuisance is 10 mg/m^3 without any limitation on the size of dust particles.

6. Documentation and Literature

A part of each delivery of a SMEP computer system, SMEP expansion module or any software is a complete set of the requisite documentation, as required by the concluded economic agreement. The extent of original technical documentation supplied with individual computers is so large that a listing of individual items would exceed the scope of this publication. To offer an idea--original technical documentation for the SM 4-20 computer is formed by 5 books of A3 format with about 1,000 pages, or for the SM 52/11 by 12 A3 format books with approximately 2,500 pages.

Thus, the following text offers only lists of publications issued as sets for user program documentation accompanying deliveries of SMEP computers, a list of training documentation issued about SMEP by the educational division of Office Machines and a list of monographs issued on the occasion of CSVTS colloquia dealing with these problems.

All sublists contain ahead of the publication's title the publisher's index number, after the title the serial number of the edition, the publisher, the year of publication, the format and the number of pages. [The title of publications written in Slovak is preceded by an asterisk.]

6.1 16-bit Systems

Outline of documentation not related to a specific operating system

Index number	Title	Published by	Format	No of pages
-	SMEP Dictionary	UVT TESLA 1978	A5	68
-	Basic instructions and programming methods	1. UVT TESLA 1978	A5	164
MINI S 036-1	Basic instructions and programming methods	2. KS OSTRAVA 1980	A4	162
-	SMEP--general description of system	UVT TESLA	A5	176
-	Assembler--language description	1. UVT TESLA	A5	128
MINI S 071-1	Assembler--language description	2. KS OSTRAVA 1981	A4	128
-	BASIC--language description	UVT TESLA 1979	A5	116
-	FOCAL--language description	UVT TESLA 1979	A5	92

Index number	Title	Published by	Format	No of pages
-	COBOL--language description (basic modules)	TESLA PROMES 1979	A5	136
-	COBOL--language description (functional modules)	TESLA PROMES 1980	A5	124
-	FORTRAN--language description	1. TESLA PROMES 1979	A5	128
MINI S 04401	[No title given]	2. KS Ostrava 1981	A4	128
-	SM 3/5M 4 hardware and software	1. UVT TESLA 1978	A5	144
-	SM 3 and SM 4 hardware and software	2. UAVT 1979	A4	144
-	SMEP computers	ZP CSVTS KS Prague 1981	A4	98
DOCUMENTATION FOR THE LOS OPERATING SYSTEM				
-	Perforated tape operating system 1st and 2nd volume	UVT TESLA 1977	A4	504
-	Description of operating system and programming	UVT TESLA 1978	A5	120
-	Service programs	UVT TESLA 1978	A5	112
DOCUMENTATION FOR THE FOBOS 1 OPERATING SYSTEM				
-	Description of operating system	1. UVT TESLA 1979	A5	128
MINI S 033-1	Description of operating system	2. KS Ostrava 1981	A4	130
-	Service programs	1. UVT TESLA 1978	A5	180
MINI S 03801	Service programs	2. KS Ostrava	A4	188
-	SYSLIB library of systemic subprograms	UVT TESLA 1978	A4	140
-	Systemic macroinstructions	UVT TESLA 1978	A4	164
-	Set of subprograms for floating decimal point	1. UVT TESLA 1978	A4	52
MINI S 041-1	Set of subprograms for floating decimal point	2. KS Ostrava 1981	A4	52
-	Operating system reports	1. UVT TESLA 1978	A5	154
MINI S 040-1	Operating system reports	2. KS Ostrava 1981	A4	152
-	Auxiliary programs	1. UVT TESLA 1978	A5	160
MINI S 039-1	Auxiliary programs	2. KS Ostrava 1981	A4	166
	Assembler--programmer's handbook	1. UVT TESLA 1978	A5	60

Index number	Title	Published by	Format	No of pages
MINI S 042-1	Assembler--programmer's handbook	2. KS Ostrava	A4	62
	FORTRAN--programmer's handbook	1. UVT TESLA 1978	A4	70
MINI S 044-1	FORTRAN--programmer's handbook	2. KS Ostrava 1980	A4	72
-	BASIC--programmer's handbook	1. UVT TESLA 1978	A4	108
MINI S 043-1	BASIC--programmer's handbook	2. KS Ostrava 1981	A4	114
-	Operating system generation	1. TESLA PROMES 1979	A5	92
MINI S 034-1	Operating system generation	2. KS Ostrava 1981	A4	94
MINI S 035	Control program and its use	1. TESLA PROMES 1979	A5	132
-	Control program and its use	2. KS Ostrava 1980	A4	134
-	VU BASIC	TESLAPROMES 1980	A4	164
MINI S 061-1	SM GRAF user's handbook	KS Ostrava 1981	A4	214
MINI SF 087-1	COBOL--user's handbook	KS Ostrava 1982	A4	127
OUTLINE OF DOCUMENTATION FOR THE DIAMS 1 OPERATING SYSTEM				
-	DIAMS--language description	TESLA PROMES 1979	A4	123
-	DIAMS--user's handbook	TESLA PROMES 1979	A4	243
M624 S 001-1	Programmer's handbook	Datasystem 1980	A4	158
M624 S 002-1	System programmer's handbook	Datasystem 1980	A4	138
M624 S 003-1	MUMPS--language handbook	Datasystem 1980	A4	127
OUTLINE OF DOCUMENTATION FOR DIAMS 2 OPERATING SYSTEM				
MINI S 081-1	System programmer's handbook	Datasystem 1982	A4	
DOCUMENTATION FOR THE VYUKA OPERATING SYSTEM				
MINI S 029-1	V01 program instruction	KS Ostrava 1981	A4	28
MINI S 030-1	*System engineer's handbook	KS Ostrava 1981	A4	64
MINI S 031-1	*System engineer's handbook. Use of assembler routines	KS Ostrava 1981	A4	26
MINI S 060-1	*Control tasks of basic V01 system of programmed instruction	KS Ostrava 1981	A4	28

Index number	Title	Published by	Format	No of pages
DOCUMENTATION FOR PPPD-1				
M693 A 001-1	*User's handbook	KS Ostrava 1980	A4	68
M693 A 002-1	*System engineer's tasks	KS Ostrava 1980	A4	28
MINI A 003-1	*Control tasks	KS Ostrava 1980	A4	43
MINI A 004-1	*Operation in supervision mode HELP	KS Ostrava 1981	A4	28
DOCUMENTATION FOR FOBOS 2 OPERATING SYSTEM				
-	Basic functions of OS	TESLA PROMES 1980	A5	168
-	Systemic macroinstructions	TESLA PROMES 1980	A5	190
-	FORTRAN Programmer's handbook (expansion for DOS RVR and FOBOS 2)	TESLA PROMES 1980	A4	160
-	BASIC--language description	UVT TESLA 1979	A5	116
-	Assembler--language description	UVT TESLA 1978	A5	128
MINI S 036-1	Basic instructions and programming methods	2. KS Ostrava 1980	A4	162
MINI S 044-1	FORTRAN--language description	2. KS Ostrava 1981	A4	130
MINI S 020-1	FORTRAN--programmer's handbook	2. KS Ostrava	A4	72
MINI S 021-1	Service programs	TESLA ELTOS 1982	A4	148
MINI S 023-1	BASIC--programmer's handbook	in preparation		
MINI S 024-1	Assembler, commo program librarian, system library	TESLA PROMES + KS Ostrava 1982	A4	165
MINI S 025-1	Auxiliary programs	TESLA PROMES 1980	A4	160
MINI S 026-1	System programmer's handbook	TESLA + KS 1982	A4	160
MINI S 027-1	OS messages	TESLA ELTOS + KS Ostrava 1982	A4	180
MINI S 028-1	OS generation	TESLA + KS 1982	A4	186
DOCUMENTATION FOR DOS RVR 1 OPERATING SYSTEM				
-	FORTRAN programmer's handbook (Expansion for DOS RVR and FOBOS 2)	TESLA PROMES 1980	A4	160
MINI S 047-1	BASIC PLUS--programmer's handbook	KS Ostrava + TESLA PROMES 1981	A4	102
MINI S 050-1	Basic OS functions	KS Ostrava + TESLA PROMES 1981	A4	176
MINI S 053-1	OS controller's handbook	KS Ostrava + TESLA ELTOS 1982	A4	148
MINI S 054-1	BASIC PLUS--language description	KS Ostrava + TESLA ELTOS 1982	A4	140

Index number	Title	Published by	Format	No of pages
MINI S 055-1	Special programming methods	KS Ostrava + TESLA ELTOS 1982	A4	166
MINI S 056-1	Operating system generation	KS Ostrava + TESLA ELTOS 1982	A4	155
DOCUMENTATION FOR MARKAB [sic] SYSTEM				
MINI S 102-1	MARKAB 1450 user's handbook	KS Ostrava 1982	A4	63
DOCUMENTATION FOR DOS RV V2 OPERATING SYSTEM				
M621 S 001-1	*Drivers	Datasystem 1980	A4	85
M621 S 002-1	*DBG tuning program	Datasystem 1980	A4	75
M621 S 003-1	*FORTRAN--language description	Datasystem 1980	A4	184
M621 S 004-1	*Processor description	Datasystem 1980	A4	165
M621 S 005-1	*FORTRAN IV--user's handbook	Datasystem 1980	A4	110
M621 S 006-1	*Operator's handbook	Datasystem 1980	A4	224
M621 S 007-1	*Service programs I	Datasystem 1980	A4	146
M621 S 008-1	*Communication program I	Datasystem 1980	A4	86
M621 S 009-1	*Macroassembler	Datasystem 1980	A4	166
MINI S 010-1	*Dictionary	Datasystem 1980	A4	42
MINI S 011-1	*PRESRV copying system	Datasystem 1980	A4	32
MINI S 012-1	*Introduction to system	Datasystem 1980	A4	48
MINI S 013-1	*Execute mode	Datasystem 1980	A4	180
MINI S 014-1	*Set of subprograms for scientific and technical calculations	Datasystem 1980	A4	105
MINI S 015-1	*Pocket handbook	Datasystem 1980	A4	44
MINI S 037-1	*FORTRAN IV PLUS user's handbook	Datasystem 1980	A4	144
MINI S 046-1	*Beginner's handbook	Datasystem 1980	A4	56
MINI S 058-1	*BASIC PLUS 2 user's handbook	Datasystem 1981	A4	154
MINI S 051-1	*Systemic subprograms handbook	Datasystem 1981	A4	135
MINI S 052-1	*Input/output operations	Datasystem 1981	A4	360

Index number	Title	Published by	Format	No of pages
MINI S 061-1	*SM GRAF user's handbook	KS Ostrava 1981	A4	214
MINI S 070-1	BASIC PLUS 2 language description	Datasystem 1981	A4	347
MINI S 086-1	*DOS RV V2 inquiry system DTS	DS Bratislava 1982	A4	100
MINI S 083-1	*DOS RV V2 introduction to RSZ	DS Bratislava 1982	A4	50
MINI S 032-1	*System for control of computer networks. User's handbook	KS Ostrava 1980	A4	24
MINI S 059-1	*System for control of computer networks System programmer's handbook	KS Ostrava 1980	A4	58
MINI S 078-1	*System for control of computer networks Programmer's handbook	Datasystem Bratislava 1982	A4	175
MINI A 011-1	Text processor. User's handbook	KS Ostrava 1982	A4	36

6.2 8-bit Systems

DOCUMENTATION FOR DOS MVS (LOS MVS) OPERATING SYSTEM

M708 T 001-1	*DOS MVS Macroassembler SM 50/40-1 Preliminary user's handbook	KS Ostrava 1980	A4	106
MINI S 048-1	*DOS MVS Macroassembler SM 50/40-1 Operator's handbook	KS Ostrava 1981	A4	32
MINI S 045-1	DOS MVS Macroassembler SM 50/40-1	Datasystem	A4	87
MINI S 019-1	*User's handbook--text editor (MVS)	Datasystem	A4	40
MINI S 049-1	*DOS MVS-PL/M 80 programmer's handbook	KS Ostrava 1 1981	A4	154
MINI S 066-1	MONITOR SM 50/40-1 operator's handbook	Datasystem	A4	24
MINI S 067 1	MVS-MONITOR operator's handbook	Datasystem	A4	28
MINI S	*DOS MVS-PL/M 80 operator's handbook		A4	
MINI S 068-1	*SM 50/40-1 arithmetic library for floating decimal point	Datasystem 1981	A4	50
MINI S 065-1	MVE 80 microcomputer developmental emulator. Operator's handbook	Datasystem	A4	79
MINI S 062-1	Cross-programming equipment of SM 50/40-1 microcomputer. User's handbook	KS Ostrava	A4	92
MINI S 063-1	MONITOR SM 50/40-1	KS Ostrava 1981	A4	74
MINI S 064-1	MONITOR MVS	KS Ostrava 1981	A4	80
MINI S 069-1	*DOS MVS-PL/M 80 operator's handbook	KS Ostrava 1981	A4	51
MINI S 075-1	*MVS--screen-oriented text editor EDIT 80. User's handbook	KS Ostrava 1981	A4	56

Index number	Title	Published by	Format	No of pages
MINI S 076-1	MVS-FORTRAN 80 programmer's handbook	KS Ostrava 1982	A4	166
MINI S 090-1	*DOS MVS FORTRAN 80 operator's handbook	KS Ostrava 1982	A4	153
MINI S 072-1	*DOS MVS user's handbook	DS Bratislava 1981	A4	70
MINI S 091-1	*PASCAL 80 user's handbook	KS Ostrava 1982	A4	83
MINI S 098-1	DOS MVS BASIC 80 programmer's handbook	KS Ostrava 1982	A4	121
DOCUMENTATION FOR MUOS OPERATING SYSTEM				
MINI S 079-1	*TL preliminary user's handbook	Datasystem 1982	A4	81
MINI S 080-1	*MUOS operator's handbook	Datasystem 1982	A4	69
DOCUMENTATION FOR MIKROS OPERATING SYSTEM				
MINI S 077-1	*MIKROS K/BASIC user's handbook	KS Ostrava 1981	A4	122
MINI S 088-1	MIKROS programmer's handbook	KS Ostrava	A4	42
MINI S 089-1	*MIKROS user's handbook	KS Ostrava 1982	A4	110
M019 T 001-1	P/BASIC preliminary user's handbook	KS Ostrava 1980	A4	116
MINI S 101-1	MIKROS COBOL 80 programmer's handbook	KS Ostrava 1982	A4	251
MINI S 103-1	FORTRAN-M language description and user's handbook		A4	126
MINI A 010-1	DATOS user's handbook		A4	150
MINI A 009-1	DYNAMIT operator's and programmer's handbook		A4	92
DOCUMENTATION FOR REAL TIME EXECUTION				
MINI S 097-1	*ERC user's handbook	Datasystem Bratislava 1982	A4	426
6.3 Instructional Documentation				
8000 T 168-1	SMEP I hardware & software description	1. KS Prague 1980	A4	262
8000 T 168-2	SMEP I hardware & software description	2. KS Prague 1981	A5	228
8000 T 180-1	Handbook for operation of SM 3-10 and	KS Prague 1980	A5	444
8000 T 185-1	DOS RV operating system	KS Prague 1981	A4	40
8000 T 191-1	DARO SOEMTRON 1156 alphanumeric series printer	KS Prague 1981	A4	180

Index number	Title	Published by	Format	No of pages
8000 T 198-1	SMEP assembler	KS Prague 1982	A5	264
8000 T 199-1	DOS/SMEP user's handbook	KS Prague 1981	A4	51
8000 T 211-1	Common busbar and input/output control	KS Prague 1981	A4	66
8000 T 212-2	OS-RV SMEP operating system	KS Prague 1981	A4	226
8000 T 213-1	RAFOS/SMEP operating system	KS Prague 1981	A5	52
8000 T 214-1	FORTRAN/SMEP programming system	KS Prague 1982	A4	257
8000 T 219-1	Dictionary defining basic SMEP terms	KS Prague	A4	42
8000 T 226-1	*PPPD programming means based on SMEP computers and practical examples	KS Prague 1981	A4	148
8000 T 227-1	CM 5400 cassette disk memory	KS Prague 1982	A4	184
8000 T 229-1	Collection of examples in Fortran SMEP	KS Prague 1981	A5	127
8000 T 233-1	KDP CM 5400 operating instructions	KS Prague 1982	A4	84
8000 T 234	KDP CM 5400-drawings	KS Prague 1982	A3	36
8000 T 235	SM 3-20 processor	KS Prague 1982	A4	160
8000 T 237-1	Collection of examples in BASIC language	KS Prague	A4	58
8000 T 238-1	Testing and diagnostic SMEP programming	KS Prague	A4	190
8000 T 254-1	DOS RV/SMEP controllers generation	KS Prague 1982	A5	200
8000 T 255-1	DOS RVRV/SMEP operating system Auxiliary programs II	KS Prague 1982	A5	100
8000 T 265-1	Collection of examples in VU BASIC language	KS Prague 1982	A4	27
8000 T 267-2	Basic characteristics of ADA language	KS Prague 1982	A4	50
8000 T 268-1	SMEP PPPD 1 V02 C universal Instructional handbook	KS Prague	A4	139
8000 T 275-1	FDT/SMEP tuning program	KS Prague 1982	A5	48
8000 T 279-1	Structured programming--programmer's handbook	KS Prague 1982	A5	28
8000 T 280-1	Structured programming--collection of solved examples	KS Prague 1982	A5	147
8000 T 281-1	DOS RV generation in unmapped version	KS Prague 1982	A5	122
8000 T 285-1	ADA programming language	KS Prague 1982	A5	448

Index number	Title	Published by	Format	No of pages
-	COBOL in DOS RV collected examples	KS Prague 1982	A5	112
028-865	TKB Task Builder PIP program for operation with sets	KS Prague 1980	A4	15
029-865	RSX-11M system pocket handbook	KS Prague 1981	A5	21
031-800	DOS/SMEP operating system. Examples of practical applications	KS Prague 1981	A4	43
-	ODT SMEO program description	KS Prague 1981	A5	18

6.4 Outline of Monographs Published as Part of CSVTS Nationwide Colloquia

SMEP computers (monograph from seminar SMEP 78)			
1st Volume	DT Prague 1978	A5	204
2nd Volume	DT Prague 1978	A4	122
FOBOS/SMEP Operating System (monograph from seminar SMEP 79), 1st Volume	DT Prague 1979	A5	352 + appen d.
2 Volume	DT Prague 1980	A5	352 + correc.
SM 3/SM 4 Operating System for Real-Time Operation (monograph from seminar SMEP 79)	DT Prague 1979	A4	10
SMEP Computers ex Moscow Exposition "JSEP and SMEP and Their Applications" (monograph from seminar SMEP 79)	DT Prague 1979	A4	6
Making SMEP I Software Available in CSSR (monograph from seminar SMEP 79)	DT Prague	A4	9
SMEP and ASVT Hierarchical Systems Applications (monograph from seminar SMEP 80)	DT Prague 1980	A5	174
Monograph from 3rd seminar "Applications of SMEP Minicomputer Systems," Strbske Pleso 1980	Datasystem EF SVST, CSVTS Bratislava 1980	A4	257
*Monograph from Conference SMEP '80	DT Bratislava	A5	180
SMEP (monograph from seminar SMEP 81 Bratislava)	DT Bratislava 1981	A5	244
Research, production and applications of SMEP mini-computers (monograph from seminar SMEP 81 Prague)	DT Prague 1981	A5	230
Computer Course in SM 3-20 and SM 4-20 in Trojanovice 1981	ZP CSVTS KS 1981	A4	139
Mini-Mikro '81 Spring Course (MUOS, TEXT 01)	ZP CSVTS at VUVT Zilina 1981	A4	139
Mini-Mikro '81 Spring Course (PPPD-1 VO2B, VU BASIC)	ZP CSVTS at VUVT Zilina 1981	A5	132

Monograph from Introductory Course on SM 50/40-1 Microcomputers	ZP CSVTS at KS Ostrava 1981	A5	50
Monograph from 4th Seminar "Applications of SMEP Microcomputer Systems" Strebske Pleso 1982	Datasystem, EF SVST Bratislava 1982	A4	312
Minicomputers-Microcomputers (monograph from seminar Minicomputers and Microcomputers 82)	DT Prague 1982	A5	218
MIKROS Compendium of Lectures	ZP CSVTS at VUVT Zilina 1982		
Real-Time Execution for SM 50/40, Parts I + II	ZP CSVTS at VUVT Zilina 1982	A5	230
		A5	104
SMEP '82 (monograph from seminar SMEP 82 Prague)	DT Prague 1982	A5	248
MARKAB 3350 (PPPD 2)	ZP CSVTS at VUVT Zilina 1982	A5	162
Spring Courses Mini-Mikro (compendium of lecture on VUVT training microcomputer)	ZP CSVTS at VUVT Zilina 1982	A5	116
	ZP CSVTS at KS Ostrava 1982		63

[Key to abbreviations:

CSVTS = Czechoslovak Scientific and Technical Society
DT = House of Technology
EF = School of Electrotechnical Engineering
KS = Office Machines
SVST = Slovak Institute of Technology
VUVT = Research Institute for Computer Technology
ZP = Enterprise branch]

7. Training

The educational division of Office Machines has been conducting since 1979--as part of services connected with deliveries of SMEP minicomputer technology--specialized courses oriented toward the training of its own and user specialists in the use of SM 3 and SM 4 minicomputers. The concept of the specialized training is modular and has been gradually expanded and improved, and has been offered to users in connection with potential marketing of the relevant products. A total of 170 courses were held in 3 school years (till June 1982), and were attended by 3,513 students seeking preparation for their position as technician, programmer or operator of SMEP minicomputers.

The training program in the area of programming and operation of SMEP computer systems for the 1982-83 school year was based on the experience of its organizers gained through the implementation of a modular system of courses categorized according to the job orientation of personnel in computer centers--Table 9.

Table 9. Outline of training in school year 1982-1983

Course number	Course title	Job	Duration in weeks	Practice
810	Technology of structured programming	P	2	yes
851	Operation of SM 3-10 computers	O (P)	2	yes
852	Operation of SM 3-20 computers	O (P)	2	yes
853	Operation of SM 4-10 computers	O (P)	2	yes
854	Operation of SM 4-20 computers	O (P)	2	yes
860	SMEP I computers and their software	P,O,M	1	yes
861	SM 3/SM 4 design and instruct. network Assembler	P	2	yes
862	LOS operating system	P (O)	2	yes
863	LOS operating system	P (O)	2	yes
864	FOBOS operating system	P (O)	2	yes
865	DOS RV V2 operating system	P (O)	3	yes
866	DIAMS operating system	P (O)	2	yes
867	DOS RVR operating system	P (O)	2	yes
874	System programming FOBOS	P	2	yes
875	System programming DOS RV 2	P	2	yes
881	Programming language FORTRAN IV	P	2	yes
882	Programming language COBOL	P	3	yes
883	Programming language BASIC	P	1	yes
887	ADA software	P	2	no
889	VU BASIC operating system	P	1	yes
897	OS RV operating system	P (O)	3	yes
898	VYUKA operating system	P,M	1	yes
899	PPPD 1 system	P,M	1	yes
901	Basic SMEP course	T	1	yes
913	SM 3-10 processor	T	2	yes
914	SM 4-10 processor	T	8	yes
915	SM 3-10, SM 4-10 peripheries	T	8 (5)	yes

917	CM 7205 (VT 340) display unit	T	2	yes
923	SM 3-20 processor	T	6 (8)	yes
924	SM 4-20 processor	T	7	yes
925	SM 3-20, SM 4-20 peripheries	T	7	yes
926	SM 3-20, SM 4-20 testing	T	3	yes
927	CM 7202 display terminal	T	2	yes
928	CM 3103 ferritic working memory storage	T	1	
929	Optional peripheries for SM 3-20, SM 4-20	T	1	
960	5400 cassette disk memory	T	2	yes
962	CM 5403 cassette disk memory	T	2	yes
964	CM 5605 floppy disk memory	T	2	yes
970	CM 5300 tape memory	T	2	yes
971	Tape memory control unit	T	2	yes
980	CM 6204 perforated tape subsystem	T	1	yes
981	CM 6208 perforated tape subsystem	T	1	yes
982	EC 6112 card reader with control unit for SMEP	T	2	yes
985	Dot printer	T	2	yes
986	CM 7108 terminal with printer	T	3	yes
987	CM 6301 dot printer	T	2	yes
988	CM 6313 line printer	T	2	yes
-	New SM 4-10 peripheries	T	9	yes
890	SMEP II hardware and software	P,M	1	
905	Basic course in microcomputer systems	T	3	
940	Basic modules of SM 50/40 system	T	4	yes
941	SM 50/40 developmental system	T		yes
946	Testing of SM 50/40 system	T	2	yes

Sub Job: P--programmer
O--operator
M--managerial personnel (organizer)
T--technician

The training of specialists is centrally organized in Office Machines by the education division of the parent enterprise in Prague. Within its framework of activities this division provides in full for the preparation of personnel needed by customers as well as the enterprises' own cadre of specialists.

SMEP customers receive direct notifications of the ever-expanding services offered in the area of specialized training; together with the negotiation of an economic contract and delivery they are offered courses for technicians, operators and programmers. However, it cannot be said that the personnel of customer organizations are being sent to take the individual courses in the logical sequence recommended by their organizers, despite the fact that the entire modular concept of the system of courses with thoroughly established linkage calls for such an approach.

The selection of a suitable cycle of instruction must be based on a model schedule of the sequence of courses, with request from the educational division for Office Machines forms for obligatory scheduling (for participation of

each student separately for each course) to assure incorporation into the prepared individual qualification plan. The obligatory scheduling of courses must include the function performed by the person sent to attend the courses. That person will attest by his signature in the schedule that he had been informed of the progression of instruction and the required qualifications stated in the offer. Failure to meet the conditions for acceptance can detrimentally affect the participant's progress.

The courses are held in leased boarding facilities on the premises of Merkur in Havirov, and in Plzen, in Karlovy Vary (with housing) and in extension form (without housing or board) in Prague, i.e., places where the students can be invited to practical tuning and instruction with the use of a computer.

The continuing endeavor of SMEP instruction organizers is to provide the course participants with all needed and helpful documentation as well as an optimum amount of computer time and practical instruction.

Recommended Sequence of Courses for Targeted Jobs

The educational division of Office Machines offers SMEP courses in the following groups:

--courses for key personnel and organizers,
--courses for programmers and operators (group 8)--see Figure 97,
--courses for technicians (group 9) see Figures 98 and 99.

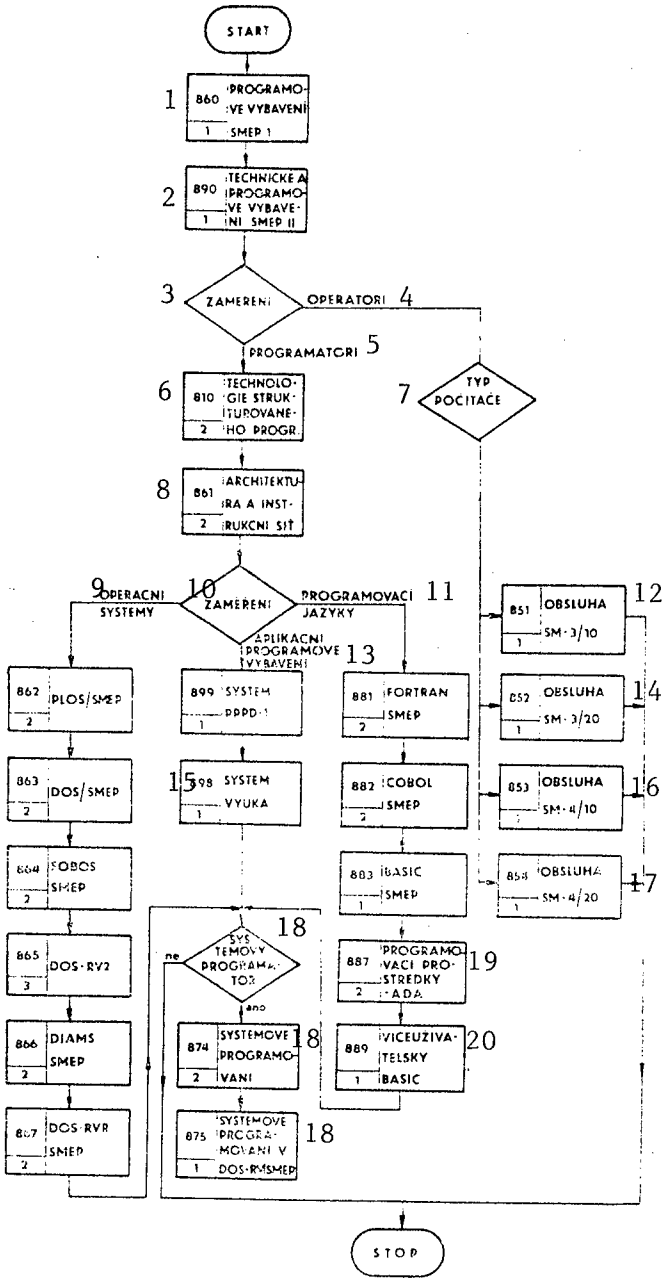


Figure 97. Training of programmers

Key:

1. software
2. hardware
3. orientation
4. operators
5. programmers
6. technology if structured programming
7. type of computer
8. design and instr. network
9. operating systems
10. orientation
11. programming languages
12. SM 3/10 operation
13. applicational software
14. SM 3/20 operation
15. VYUKA system
16. SM 4/10 operation
17. SM 4/20 operation
18. system programming
19. ADA software
20. multiuser BASIC

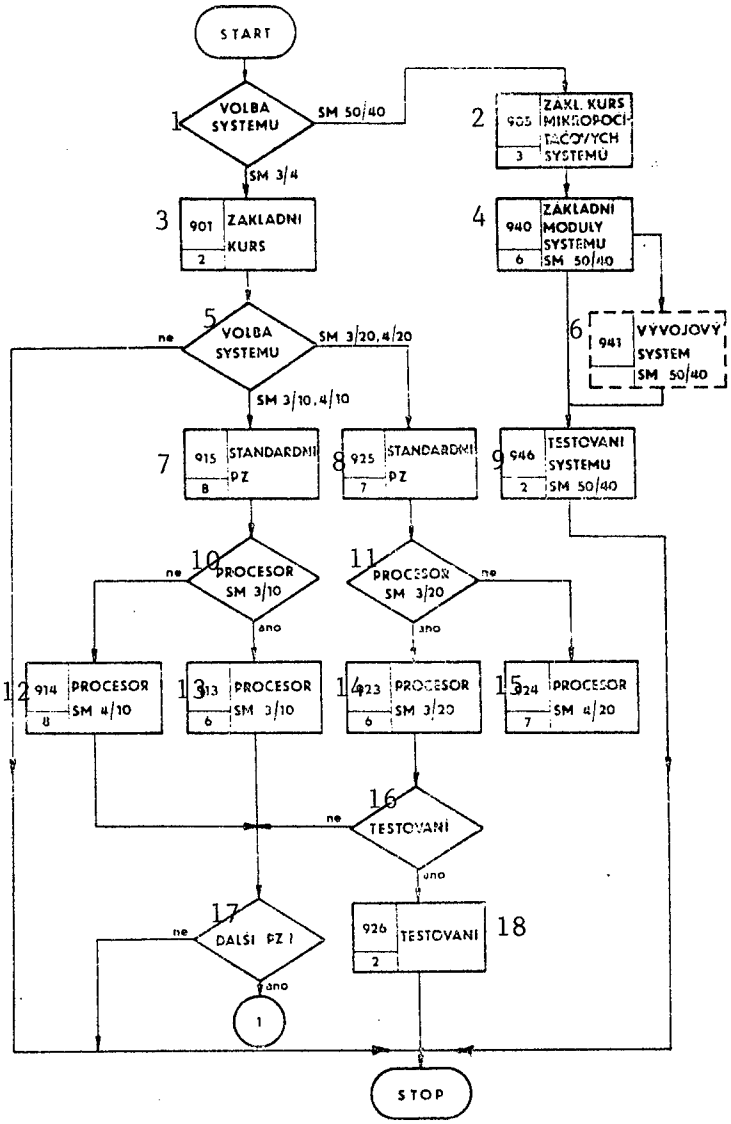


Figure 98. Training of technicians (Part 1)

Key:

1. system selection
2. basic microcomputer system course
3. basic course
4. basic modules of SM 50/40 system
5. system selection
5. SM 50/40 developmental system
7. standard peripheries
8. standard peripheries
9. SM 50/40 system testing
10. SM 3/10 processor
11. SM 3/20 processor
12. SM 4/10 processor
13. SM 3/10 processor
14. SM 3/20 processor
15. SM 4/20 processor
16. testing
17. additional peripheries
18. testing

ne = no; ano = yes

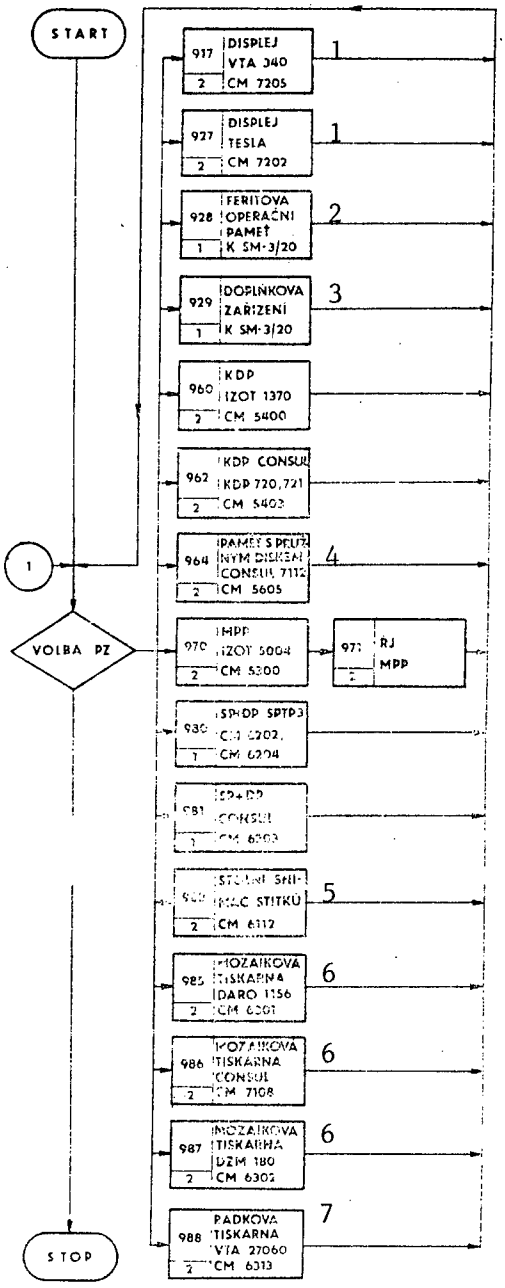


Figure 99. Training of technicians (Part 2)

Key:
1. display
2. ferritic working memory
3. peripheries for SM 3/20
4. floppy disk memory
5. CM 6112 desktop card reader
6. mosaic printer
7. line printer

An outline of courses for both groups appears in Table 9. The group number coincides with the first digit of course number.

7.1 Courses for Managerial Personnel and Organizers

Courses for key personnel and/or organizers--who from an analytical viewpoint oversee the practical application of SMEP computers--are for the most part

provided on the basis of individual agreements as extracurricular courses with their own individual curricula. Nevertheless, even the standardly offered training contains a number of courses suitable for such personnel. This involves specifically the introductory course 860 and applicational program courses (problem-oriented configurations, i.e., courses starting with the digits 89).

7.2 Courses for Programmers

The programming courses included in group 8 are not differentiated from the viewpoint of the SMEP computers used. They form subgroups of courses

--introductory courses (courses 860, 861, 810),
--programming languages (courses 881-889),
--operating systems for programming (courses 874 and 875),
--applicational program courses (so far courses 897 and 899).

Selected variants of the sequence of courses should respect the listed sequence and the student should first complete introductory courses, then courses for the selected programming languages, then courses on operating systems and only then courses dealing with applicational software.

All courses are gradually updated in keeping with the transfer of additional program products to Office Machines from the relevant organizations. The subgroup of user-oriented programs will be successively supplemented by additional problem-oriented configurations.

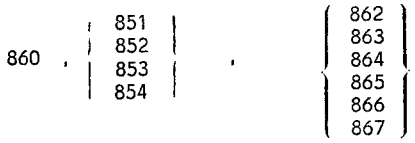
Depending on the personnel staffing of SMEP computer centers, it is often expedient to send programmers--after completion of at least two initial courses (860, 861)--to courses for operators.

7.3 Courses for System Programmers

A system programmer should acquire through course participation at least minimal knowledge in the scope of courses 860, 861, 883-889, 874 and/or 875. These courses, supplemented by a selected course in a language and operating system as well as a relevant course for operators (851-854), together with the imperative personal practice (temporary duty assignment) with a computer, are the prerequisite for developing the talents and capabilities that a system programmer should possess (generation of control systems, resolution of complaints, providing consultation to user programmers, contact with the central library of NOTO [national organization of technical services] programs, etc.).

7.4 Courses for Operators

If the center equipped with a SMEP computer has a manning slot for an operator (which by far is not always the case), it is recommended that he complete courses from group 8:



From the offered courses for operational control (851-854) and operating systems (862-867) are selected relevant courses, depending on the type of computer and operating system used in the center.

7.5 Courses for Technicians

Courses for SMEP technicians are concentrated in group 9 and form the following subgroups (see also Figures 98 and 99):

90--basic courses independent of any given type of computer,
91--processors and peripheries of systems SM 3-10 and 40-10,
92--processors and peripheries for computers of domestic production, testing system,
94--courses on SM 50/40 microcomputer systems,
96--courses on disk memories,
97--courses on magnetic tape memories,
98--courses on individual peripheral systems, terminals, input/output systems, etc.

The individual study plan of personnel trained to perform the job of technician should include in logical sequence first the relevant basic course, then, depending on orientation, a course dealing with the appropriate processor or a course on the relevant set of peripheral systems. Here the mutual sequence of courses in subgroups 91, 92, 94, 96, 97 and 98 is irrelevant.

The outline of the plans of instruction as presented in the text includes courses conducted by the educational division of Office Machines and, moreover, it assumes that the user is starting the training of personnel with a sufficient time lead prior to delivery so as to avail himself of the opportunity of reconciling the logical sequence of courses with the data scheduled for their presentation. This outline does not include additional sources of information, such as:

--study of literature and documentation,
--use of temporary duty assignment in a "seasoned" computer center of some other organization,
--seminars staged by CSVTS, SAK [Society for Applied Cybernetics] and other organizations,
--courses conducted by Datasystem, VUVT, ZVT and other organizations,
--courses offered in sectoral training facilities,
--courses abroad.

These additionally listed opportunities can add depth to preparation or cut down on the total time needed to prepare personnel to operate SMEP computers.

8. Planning and Technical Assistance

Technical assistance and/or planning on the basis of placed orders is provided for the preparation of facilities from the viewpoint of operational conditions for minicomputers by units of the computer centers planning division of Office Machines in individual regions (Prague, Plzen, Hradec Kralove, Brno, Ostrava and Teplice). These services are offered contingent on available capacity and involve:

--assessment and/or proposed design for implementation,
--proposed distribution of a minicomputer system,
--air conditioning,
--power supply for air conditioning, including controls,
--electric fire alarm,
--technological interior design.

These activities are provided specifically by the following planning centers:

Location	Code	Street address, representative	Telephone
Prague 1	111 90	Narodni trida 19 Otto Sebor	26 71 41-4
Plzen	304 35	Karlova 40 Eng Svatopluk Perina	22 50 55
Hradec Kralove	501 95	Spitalska 183 Jiri Horak	25 846
Brno	601 12	Veveri 102 Eng Ivan Hlavon	59 654
Ostrava	701 00	Zivicna 1 Eng Jaroslav Stebel	23 17 60 23 26 14
Teplice	415 23	Gottwaldova 19	61 21-3

8.1 Note on Planning Remote Data Processing Systems Using CSSR Telecommunications Network

Data transmission services in the Czechoslovak telecommunications network--until publication of the "Data Transmission Regulations" now in preparation--are subject to the provisions of the telephone and telegraph regulations and attendant statutes. These provisions are binding for users and must be respected in the planning, implementation and operation of remote data processing systems which use the facilities of the uniform telecommunications network (JTS) for the transmission of data. Detailed information about the possibilities and conditions for providing data services and fees for these services are available from organs of the communications administration. It is imperative that planners of remote data processing system consult these organs; here are some implementable proposed solutions.

Consultation in preparatory planning stage is offered:

--for users on Prague territory by the International and Long-Distance Telephone and Telegraph Exchange (MTTU Prague), operational/marketing unit;

--in individual regions by the Regional Directorates of Communications;

--for systems reaching into several CSR regions by the Central Directorate of Communications Prague, telecommunications division;

--for systems encompassing the country's entire territory by the Federal Ministry of Communications, telecommunications department;

--consultations in technically demanding cases and problems of a conceptual nature by the Research Institute for Communications Prague, data transmission group.

The MDS 200 and MDS 1200 modems of Czechoslovak production--after connection to the telecommunication circuits of the communications administration and introduction into operation--are incorporated into ITS as systems of the Communications Administration, which then are loaned to the user and maintained for a specified remuneration. The means for procurement of these systems are provided by the user.

The specified types of modems are supplied to users exclusively by the Czechoslovak Communications Administration. In view of delivery and planning deadlines the users must submit their binding requests to the relevant organization of the Communications Administration, at the latest by the end of October preceding the years of delivery by 2 years.

In cases where the listed modems are not operated in the JTS, they remain the user's property. Modems not supplied by the communications administration are procured by the users themselves. However, the only types that can be operated in JTS are those for which certification and approval for connection to JTS were issued. These systems remain the user's property and he then provides for their operation and maintenance.

Any systems owned by the user (i.e., data transmission terminals and/or modems or other signal converters) can be connected to JTS circuits (i.e., digital circuits with modems of the Communications Administration or analog circuits) only with the consent of the Communications Administration.

Permission for connection and operation is granted only for systems approved (homologized) by the Communications Administration.

9. Technical Services

Technical services for SMEP systems are organized in all plants of Office Machines, for the most part in the form of SMEP Technical Services and Technical Service for Office Equipment. These sections provide basic services, i.e., systems setup (installation) and repair.

The actual performance of services for customers is conducted on a decentralized basis within the territorial jurisdiction of Office Machines plants in the CSR, including subsidiary operations.

Centralized control and coordination is provided by the establishment of key brand-oriented centers which deal with problems of logistical backup as well as by functions of central control and methodical units in the parent plant in Prague. The inevitability of centralized control of services is coming to the fore primarily in connection with the introduction of concern-type management and centralization of commercial services.

The basic objective for the development of SMEP-oriented services is meeting the needs of customers, i.e., improving the quality of these services and their performance for the widest possible circle of users. This means a transition from an extensive form of services, performed mostly "in the field," to intensive, industrial forms. This involves first of all transfer of most services (including preparatory activities) to technical service centers, i.e., to units of technical preparation of production, laboratories, workshops and specialized facilities. This makes it possible to make use of specialized technical equipment, including complex automated diagnostic systems for recurrent repairs of customers' computer technology. This also makes it possible to attain a great increase in labor productivity than is the case "in the field," and in so doing also meet to a much greater extent than before the demands of users on the quality, extent, expediency and price of services, and also the economic effectiveness of services, not only on the scale of the service organization but from the viewpoint of society as a whole.

An important resource in the area outside of capital allocations that will promote industrial forms of repair are the means expended on technical progress. It is envisioned, as part of dealing with the sectoral project for technical progress, to develop the requisite hardware and especially software for diagnostics which is not supplied by producers, and work is continuing in dealing with practical problems connected with utilization of technological systems (e.g., spaces, capacities, repair technology, safety). From this viewpoint, dealing with the projects in individual stages of their resolution and implementation accrues to Office Machines. The basic requirement herein is the typicality of a solution and its potential use by other organizations in the CSSR.

An integral part of the wide application of minicomputers and microcomputers is also the preparation of cadres, which takes the specific form of introducing new viable methods of instruction, including program instruction with a computer.

The actual performance of services calls for a corresponding system of management that has at its disposal all the requisite information for operational, tactical and strategic management. The demands placed on such a system of management can be met only by an automated information subsystem.

Returning at this point to the actual performance of services "in the field," i.e., on customers' premises, it can be said that basic services are currently being provided, i.e., setup and repair of SMEP systems. From the viewpoint of volume and importance of performed services, the focal point is the servicing of domestically produced computers. The provision of services for imported computers has its own specific aspects.

The setup of SMEP computers progresses in three phases:

--preinstallation preparations,
--actual activation,
--turning over into operation.

At the stage of preinstallation preparations the objective of the supplying organization is providing the future user with a maximum of information not only on the technological systems and its potential applications, but also on the requisite operational and technical measures that must be taken into consideration in the preparation of spaces for a computer. Smooth follow-up of computer delivery by its installation is inevitably tied to initiative on the part of users in the preparation of spaces (to which is tied the granting of warranty).

The actual activation of domestic SMEP computers is carried out by personnel of Office Machines. In the case of imported system this is done, as a rule, especially in the initial period, by foreign specialists on the basis of a contract concluded between the foreign supplier and Office Machines.

Endeavors are being made to create in the near future conditions that would make it possible for technical service units to be able to set up SMEP computers supplied from abroad that would favorably affect the comprehensiveness and effectiveness of services both from the viewpoint of the service organization and from the viewpoint of the national economy.

Launching into operation includes turning over hardware and software to the customer on the basis of the stipulated transfer and acceptance specifications. Acceptance tests are attended by responsible representatives of the supplier and of the customer.

Launching of a computer into operation is followed up by the phase of providing guaranteed as well as post-warranty repairs. The optimum organization of these repairs calls for a suitable pattern of technical services for a given stage of development of services. The determination of such a model of technical services for SMEP computers is based on the following criteria:

--design specifications and key technical and functional properties of SMEP systems (complexity, modular structure, the used technology of production and elementary basis, potentials of a diagnostic system, etc.);

--expected and attained levels of reliability parameters, i.e., trouble-free operation, ease of repair, expedient availability and the resultant operational efficiency;

--capacity and organizational possibilities of Office Machines (manpower, materiel, transportation and communication) and the relevant qualitative level of the logistical backup formed by storage facilities, laboratories, workshops and specialized facilities;

--economic effectiveness of the proposed form of services at a given stage from the viewpoint of society as a whole.

The service organization's ultimate goal is to provide full guaranteed and post-warranty services for domestic SMEP computers in the form of comprehensive technical care throughout the CSR. Herein the optimum solution appears to be the utilization of a model of technical service without the constant

presence of a technician at the computer, which has at its prerequisite the provision of all indispensable material and technical resources in the field as well as in the center while organizing repairs by the substitution method. It is expected that the customer will provide qualified operators who will not only be intermediaries for communication between man and machine, but will also provide competent information about any breakdown to the technical service center. Such timely and comprehensive information is of decisive importance in optimizing the time for restoring the system's functioning. It is this area in particular that points up the importance of the new forms of personnel training of the service organization as well as of the customer.

From the long-term viewpoint comprehensive technical care represents a qualitatively higher form of activity which the service organization could implement in the nearest future as soon as the indispensable conditions have been created, the so-called completing of the assortment of modules and turning out of complete systems.

Completing the assortment of modules means filling in the gaps which occurred in the linkage production-user sphere in connection with a shortage of peripheral equipment. Completing the assortment of modules calls at the present time for becoming proficient in the technology used for carrying out required modifications of peripheral equipment so as to make possible the implementation of the so-called direct deliveries of peripheral equipment for the expansion of basic configurations of already delivered SMEP computers in the required quality and functional reliability.

The turning out of a complete system represents a qualitatively higher level of services offered to users. This could be viewed as a higher form of delivery, wherein the supplying organization turns over a computer system as a complete unit that includes software for data computers as well as for computers incorporated into production control or technological processes. From this it follows that it will involve deliveries of nonstandard configurations "made to measure" for the user, depending on his needs.

The turning out of complete systems can be seen as an opportunity for the continued development of Office Machines in the area of mini- and microcomputer technology, a qualitatively higher level of offered services and the key task from the viewpoint of the need of both the national economy and of users.

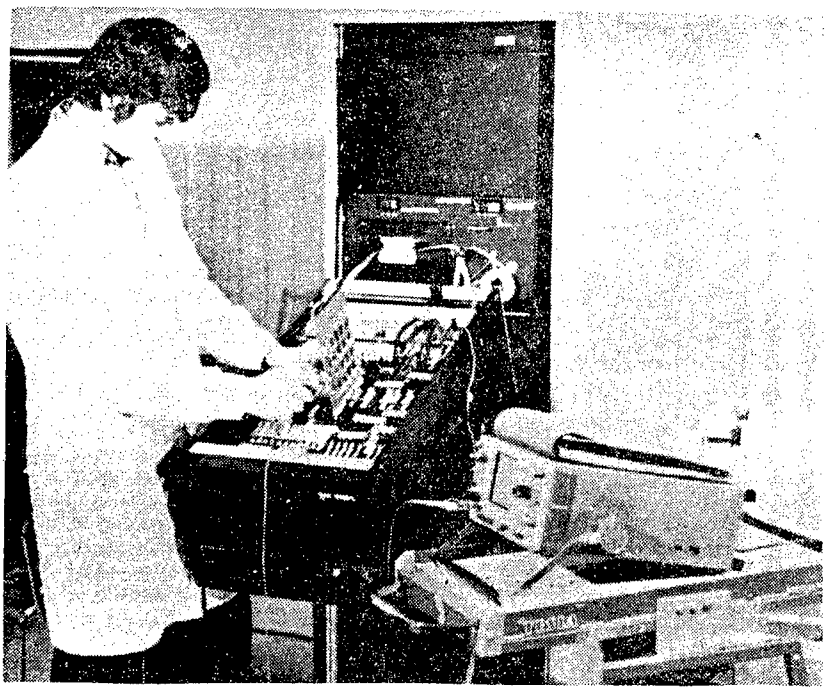


Figure 100. The utilized design of SMEP systems makes technical care easier

10. Availability

The following test will outline the state of availability of individual hardware, software and documentation. This chapter attempts to provide answers to the questions of "what" will be available "when." The questions of "how" to obtain individual products and "where" to order them and "where" to obtain information are answered by the subsequent chapter. In view of the fact that the closing deadline for this publication came at a time when Office Machines had not yet concluded economic contracts for 1983 deliveries, the subsequently listed data are of a merely informative nature.

10.1 Hardware

10.1.1 16-Bit Systems

The basic configurations of minicomputers that already were in production in 1982 (SM 3-20 since 1980, SM 4-20 since 1981) are listed in this publication in configurations in which they were standardly delivered in 1982, which also are the initial configurations for 1983.

The SM 52/11 minicomputer and the SM 50/50 microcomputer are to be produced as of 1983 and it is envisioned that initially, i.e., in 1983, they will be delivered in the basic configurations listed in section 2.1.1.

A change in comparison to 1982 can occur in the configuration of the ISAP 1 interactive graphic system, where it is envisioned to supplement it by large-capacity 29 MB disks and additional graphic systems directly in the basic configuration.

In the subsequent text is listed the assumed availability of individual hardware, with the provision that a number of measures had been taken for meeting the market demand in the area of computer technology.

Nevertheless, it ought to be realized--and practice shows this ever more clearly--that blaming failures in the use of computer technology on a shortage of peripheral equipment is too superficial. Many users do not base their demands for delivery of complete systems, and for supplementing them beyond the scope of the delivered standard configurations of minicomputers, on their actual processing needs, but rather on the volume of investment resources which they managed to obtain for the procurement of computer technology that must be spent, on the basis of their mistaken idea that computer technology will eliminate shortcomings in the management of organizations, on the basis of wishing to have the largest computer center, etc. Everybody who has had at least some experience with computer technology konws that from the technical viewpoint it is not difficult to justify even the most exaggerated demand.

Experience with many successfully applied SM 3-20 and/or SM-24 computers shows that with a responsible and knowledgable approach to use of computers these computers are not only adequate for many applications, but also that many of the possibilities they offer often remain unused. It stands to reason that the lack of a conceptual approach to the use of a computer, the endeavor to show at any cost as early as possible that "it works," causes data processing to be ineffective, time-consuming and then the easiest way out really is blaming the computer.

This state of affairs is borne out by cases of many organizations that as late as the time of the computer's installation have no proper concept of its application.

It cannot be asserted that the SM 3-20 minicomputer could replace the EC 1021 computer, but if we compare for the sake of interest some of the features of the SM 3-20 computer with those of the EC 1021 computer, we come to the surprising conclusion that many specifications for both computers are comparable (size of working memory storage, speed of carrying out instructions, capacity of disk units, etc.), but that some specifications are in favor of the SM 3-20 minicomputer (substantially simpler and more efficiently working specialized operating systems, a more effective set of instructions, particularly for input/output operations). And, despite all this, at the time the EC 1021 computer was being produced and introduced nobody thought that the computer was unusable, as many users think of the SM 3-20 today.

According to information from technical press, it is known that in foreign countries a great number of computers with varying output capacity are available. There are minicomputers with internal 16 Mbyte memory, with disk memories of up to 600 MB and other top features. At the same time, however, it is not always pointed out that the computer selected as the average European computer for 1981 was the DEC company's PDP 11/34 minicomputer with a large-capacity disk memory. And, for the sake of illustration, the catalogue of the basic configurations of this company's computers also offers the basic configuration of the PDP 11/34 with 64 K-word internal memory and one 5 MB capacity disk for 1983.

Understandably, many applications require large systems, large memories, many peripheral units; however, there is a need to consider whether developmental stages in the introduction of computer technology can be skipped without long-term experience with simple applications, e.g., data acquisition, and to demand hardware for the immediate control of complicated complexes in economic production units and plants, preferably as early as tomorrow, with everything operating in interactive mode and in real time.

In 1982 there were available, and it can be expected that a certain number of units will also be available in 1983, the following peripheral systems:

--CM 5400 and CM 5403 5 BM cassette disk memory,
--CM 5605 floppy disk memory,
--CM 5300.01, O. K. small tape memory,
--CM 6204 and/or CM 6208 perforated tape reader/puncher,
--CM 6112 punch card reader with control unit (PAD 12),
--CM 6301 dot printer,
--CM 6313 dot printer in a very limited number of units,
--graphic systems as part of ISAP 1 graphic complexes,
--CM 7202 series and/or parallel terminals,
--CM 7108 parallel terminal with printer,
--ASAD CM 6002 asynchronous adapter,
--PAD 8 CM 6001 parallel adapter,
--PAD 16 SM 0706 parallel adapter,
--SAD CM 8506 synchronous adapter,
--CM 8105 zero modem,
--LJSP CM 9205 laboratory unit for contact with environment,
--IMS 2 CM 0102 interface unit,
--CM 9004 (three variants) interface unit for DASIO 600,
--CM 0101 systemic unit,
--CM 4103 common busbar repeater,
--expansion grid,
--casing,
--casing with expansion grid.

In 1983 these systems will be expanded by:

--CM 5405 large-capacity 29 B disk memory,
--CM 8302 large tape memory,
--CM 1601 display terminal,
--AMU CM 8511/C asynchronous multiplex,
--SM 2016 extension plate.

It can be expected that the additional systems described in the preceding chapters will become available in 1984 and 1985.

10.1.2 8-Bit Systems

Deliveries of the SM 50/40 system are to commence through Office Machines in 1983 in the configurations specified below:

--Basic configuration of cassette A containing:

--SM 2138 single-plate microcomputer,
--SM 0440 16K byte dynamic RAM memory,
--SM 0449 16K byte EPROM memory,
--SM 1355/B module of 48 discrete, optically insulated 24 V inputs/outputs in a 24 inputs/24 outputs combination,
--power supply source A,
--the cassette's own mechanism;

--MVS 1 developmental system in configuration:

--basic unit with display terminal with a built in operator's panel and modules:

--SM 2138 single-plate microcomputer,
--SM 0442/B 64K byte RAM memory,
--SM 2143 nonstandard interface module,
--MVE developmental simulator,

--CONSUL C 2111 dot printer,
--FS 1501 A/M perforated tape reader,
--DT 105 S perforated tape punch,
--PGM 08 EPROM memory programmer,
--3 desks with accessories;

--configuration of cassette A and cassette B containing:

--SM 2138 single-plate microcomputer,
--SM 0442/A 48K byte RAM memory + 16K byte EPROM memory,
--SM 1335/B module of 48 discrete, optically insulated 24 V input/outputs in combination of 24 inputs/24 outputs,
--power supply source A,
--A cassette's own mechanism,
--SM 1353 module of 8 analog 8-bit outputs,
--SM 1354 module of 4 analog 12-bit outputs,
--power supply source B,
--B cassette's own mechanism;

--ranging box;

MVS II developmental system in configuration:

--basic units with operator's terminal and built-in operators panel and modules:

--SM 2138 single-plate microcomputer,
--SM 0442/B 64K byte RAM memory,
--SM 2143 nonstandard interface module,
--MVE developmental simulator,

--CONSUL C 2111 dot printer,
--FS 1501 A/M perforated tape reader,
--flexible magnetic disk memory,
--PGM 08 EPROM memory programmer,
--4 desks with accessories;

--selected configuration of the SM 53/10 system.

It is envisaged that individual modules of the SM 50/40 modular assembly will be freely available from 1984 and, further, that in 1984-1985 will become available the SM 50/40 microcomputer, programmable terminal, text processing system, the SM 5320 system....

The VUVT training microcomputer is supplied exclusively through VUVT Zilina.

10.2 Software

In 1983 it will become possible to acquire software for 16-bit computers listed in the outline of operating and programming systems, software for graphic systems and individual programming languages. Software for 8-bit microcomputer is available.

In addition to this software, preparations are underway in Office Machines to start marketing additional software generated through cooperation with researchers, intraplant R&D projects and as part of work on solution of the state task.

The APV applicational software generated in task P04 119 214 covers specifically the following problem areas:

User service programs expanding the basic software of SMEP I minicomputers by conversion programs with logic functions, a general print and program generator, operation with tables in memory, library of adjustable programs, transfer of data between DIAMS and DOS RV operating systems, updating and other programs.

APV for the preparation and preprocessing of data covers the area of preparation, preprocessing and transmission of data on the basis of hardware CONSUL, SM 3, SM 4, SM 50/40 and SM 50/50.

Selected tasks in the system for automated management of small organizations are dealt with through automated processing of the subsystems on the SM 4 and/or SM 52/11 computer listed below:

--Technical preparation of production,
--Operational production control,
--Logistics,
--Capital assets,
--Marketing management,
--Economic information,
--Personnel and wages,
--Energy management,
--Management of upgraded forms of supply.

The solution of this partial task is divided into two stages. The first stage--which ends in 1983--will provide for the autonomous processing of the above-listed subsystems on SMEP computers. In the second stage--which ends in 1984--the JSEP multi-level automated system of management will be worked out in closer detail.

APV for SMEP I, SMEP II mathematical, economic, statistical, scientific and technical calculations represents a set of programs for the processing of tasks and calculations from the area of mathematics, statistics, economy, science and technical calculations.

APV for data transmission between SMEP-SMEP, SMEP-JSEP stands for interconnection of computers SMEP I-JSEP, SMEP I-SMEP I, SMEP II-JSEP and SMEP II-SMEP I, and the establishment of a transmission route between two computer systems utilizing the existing telecommunications network and working out of testing methods.

APV for computer graphics for equipping graphic complexes is intended to automate design operations and operations of a technological nature with the use of SMEP I and/or SMEP II computers.

APV for the management of large commercially-oriented units is for the automation of recordkeeping and information operations connected with the circulation of goods as well as improved efficiency and effectiveness of procurement, storage and sales operations.

APV for the food industry is to control production in food processing enterprises with direct deliveries including the areas of marketing, personnel, supply, transportation and actual production.

10.3 Documentation

With the exception of a few titles that are either being printed or are currently sold out, all documentation listed in the relevant chapter is available.

10.4 Imported Systems

Office Machines will continue to mediate deliveries of SM 4-10 minicomputers from the USSR and INDEPENDENT from Romania in 1983.

11. Order Justification and Information

11.1 Budgeting of Computer Technology

--budgeted,
--other.

a) Budgeted computer systems are requisitioned in 1983 in accordance with "Instruction No 1/83 of the deputy minister of commerce," published by FMEP under index no 500/40/83, which includes:

1. The following computer systems are subjects for the balancing of needs at the ministerial department level (central balance "U")--balanced at FMEP:

EC 1011--producer Hungary,
EC 1027--producer CSSR,
EC 1032--producer Poland,
EC 1045--producer USSR,
EC 1055--producer GDR.

The following are subjects for the balancing of needs at the medium level of management (enterprise balance + V):

EC 1026--producer CSSR,
SM 4--producer CSSR + USSR,
SM 52-11--producer CSSR.

2. In view of the nature of computer technology and the complexity of preparation for application, the process of balancing needs is divided into 3 years.

The basis for balancing out the needs at both levels are the specifications of the balance of needs for computer systems for the year 1983 issued by FMEP under index no 510/250/82 on 13 December 1982, specifically the part for the years 1984 and 1985.

The result will be a projection of the need for computer systems for the year 1984, an updated outlook of the projection for 1985 and a projection outlook for 1986 conforming to new requirements.

3. The basic documentation justifying the reason for the selection of the type of computer, and its configuration, and attesting to the completion of preparations, is a properly filled out "Outline of Preparations for Use of Computer" (hereafter "Outline"), issued by FMEP under index no 500/43/80.

For requisitioning JSEP computers the "Outline" is filled out in full; for SMEP computers only pages 1, 2, 6, 12, are filled out, including approval by a central authority (ministerial department)--see page 12 of "Outline."

4. Procedure for requisitioning computer systems budgeted at middle management level (enterprise balance--"V"):

4.1 The customer organization makes its requirements known to the relevant NOTO organization depending on the location where the computer is to be installed, i.e., in:

--CSR: Office Machines fiduciary concern organization, trade policy department, # 15 ulice 28. rijna, ZIP code 111 90 Prague 1, telephone no. 26 39 06, 26 10 70.

--SSR: Datasystem fiduciary concern organization, department of marketing and complementing of computer systems, # 4 Stefanicova, Bratislava, ZIP code 815 69, telephone no. 432 70,

in the course of preparation of the implementation plan proposal for 1984, but no later than 30 May 1983, as follows:

4.1.1 Requisitions for delivery of computers in 1984 and 1985 are submitted by users in accordance with the projected outlook which forms a part of the specifications of the projected needs for 1983. If the "Outline" has already been included in the plan preparations and discussed with the NOTO organization, the requisition is submitted in the form of a letter which will contain--in addition to basic data about the requisition (user, economic production unit, ministerial department, registration number DOV, type of computer, requested year of delivery)--only data regarding the meeting of the planned deadlines of preparations, their specification, changes and supplementing with reference to the relevant points of the "Outline." The "Outline" need be submitted only in case of substantial changes or with extraordinary new requirements.

4.1.2 Requisitions for the delivery of computers in 1986 are submitted on the "Outline" (single copy), including approval by central authority.

4.2 Supply-demand negotiations for the delivery of computers in 1984 through 1986 are conducted by the relevant NOTO organization with the objective of striking a balance between the resources at its disposal in individual types of computers and the demands of customers, or it may propose to customers a substantial solution in cases where demand exceeds potential supply in individual types. A record will be made of the negotiations in accordance with paragraph 12 of Decree No 48/80 of the SBIRKA ZAKONU, which in case of possible disputes will contain proposals for their resolution and will be turned over to customer organizations for comment by 30 June 1983.

4.3 By 20 July 1983 both NOTO organizations submit a summary of requirements and proposed distribution of computers for the years 1984 through 1986, together with records of negotiation of supply-demand relations and proposals for resolution of any disputes to the relevant general management of Automation and Computer Technology Plants (GR ZAVT).

4.4 In accordance with paragraph 12, section 6 of Decree No 48/80 of the SBIRKA ZAKONU, the GR ZAVT will conduct at its level a comprehensive negotiation with the objective of resolving any disputes in the supply-demand relations no later than 14 days prior to the deadline for submission of the implementation plan proposal for 1984 to central authorities, will compile the balance and carry out its specification.

Notification of determined allocations will be done through FMEP to central organizations of customers together with a specification of the JSEP systems, balance "U"; see point 5.5.

5. Procedure for requisitioning computer systems budgeted at ministerial department level (central balance--"U"):

5.1 Customer organizations make their requirements known via their middle level of management through central authorities (ministerial departments) directly to the balancing point at FMEP as follows:

5.1.1 Requisitions for delivery of computers in 1984 and 1985 are submitted in keeping with the projected outlook which forms part of FMEP balance specifications for 1983. Customers listed in the projected outlook will confirm the acceptance of their requisition for delivery through their middle management level to their central authority in the form of a letter.

The "Outline" will be submitted only in cases of extraordinary new requirements not listed in the projected outlook balance.

5.1.2 Requisitions for delivery of computers in 1986 are submitted on the "Outline."

5.2 Central authorities submit to FMEP no later than 30 June 1983 a list of requirements for their sector, specifically:

5.2.1 In the form of a letter in which they confirm accepted requisitions for delivery listed in the projected outlook for 1984 and 1985 which forms part of the FMEP balance specifications for 1983, together with confirmation by relevant units of the central authority about investment backup of the requisition.

5.2.2 Requisitions for the delivery of computers in 1986 and extraordinary new requirements on deliveries in 1984 and 1985, i.e., not listed in the projected balance of needs, are submitted in triplicate on the "Outline" form.

5.3 New requirements ("Outline") are turned over by FMEP immediately upon submission, no later than 10 July 1983, for comment to FMTIR [Federal Ministry for Technological and Investment Development]. FMTIR makes and successively turns over to FMEP, no later than 20 August 1983, comments on the new requirements from the viewpoint of their effectiveness.

In the interest of smooth processing, central authorities are advised to hold preliminary discussions with FMTIR about new requirements for the delivery of centrally budgeted computers (balance U) already during the preparation of the plan before 30 June 1983.

5.4 Interdepartmental negotiation of supply-demand relations is carried out no later than 14 days prior to the deadline for submission of the economic implementation plan proposal for 1984.

5.5 FMEP compiles a balance and sends its specifications to the central organizations of customers in accordance with paragraph 14, section 2 of Decree No 48/80 of the SBIRKA ZAKONU.

b) Other SMEP computer technology systems are divided at the GR ZAVT level:

--ISAP systems and computers of the ADT series are balanced and allocated to users through GR ZAVT at the recommendation of the NOTO organization;

--systems of the SM 50/40, SM 50/50, SM 53/10 series are not subject to balancing, and distribution to users is carried out by the NOTO organization in cooperation with GR ZAVT.

c) The requisite information from the area of budgeting computer technology can be obtained at Office Machines in Plzen, Hradec Kralove, Brno, Ostrava and Teplice from representatives of business sectors whose addresses are listed in chapter 11.

d) The procedure for requisitioning computer systems in 1984 for the years 1985-87 will be updated by FMEP in the course of the first quarter of 1984.

11.2 Ordering, Directory

The procedure for ordering hardware, budgeted or not, was specified in the preceding section.

Orders for hardware and its basic software (including imported systems 4-10 and INDEPENDENT of the I 100 series) are taken exclusively at the following address:

Office Machines, fiduciary concern enterprise
Sector of OSVS--SMEP marketing
Husitska 36
1190 Prague 3

Orders for additional SMEP software, including documentation, are handled by sectors of systemic engineering of the territorially applicable Office Machines plants:

Prague 3	111 90	Husitska 11
Plzen	304 35	Uslavska 2
Hradec Kralove	501 95	Labska 1364
Brno	601 12	Veveri 102
Ostrava 1	701 00	Vystavni 14
Teplice	415 23	Gottwaldova 19

Orders for individual shipments of SMEP programming documentation are handled at the following address:

Office Machines, fiduciary concern enterprise
Sector of systemic engineering
Vystavni 14
701 00 Ostrava 1.

11.3 Deliveries

Deliveries of SM 3-20, SM 4-20, SM 52/11, SM 4-10, INDEPENDENT of the 100 series, MVS I and II, SM 53/10 computers and other systems are for the most part handled under the provisions of paragraph 165 of the economic codex in the context of Law No 37/71 of the SBIRKA ZAKONU. An economic contract

for delivery of a computer includes delivery of the basic configuration of the computer, expansion hardware type 403, basic software and attendant introductory services.

Part of the economic contract for delivery is a contract concluded for providing operations and services in connection with setting up the computer and training of customer's personnel.

The extent and composition of the basic software is stipulated in the economic contract for computer delivery. Basic software is turned over to the customer no later than the day of computer startup, user program documentation supplementing basic software is turned over in a single copy within 60 days of the conclusion of the economic contract for computer delivery.

11.4 Warranties

11.4.1 Hardware

The warranty period for a basic computer configuration is 12 months from start-up, not to exceed 15 months from completion of delivery.

The warranty period for expansion hardware type 403 is always specified in the appropriate section of the economic contract for delivery. One of the conditions for honoring the warranty on the part of the supplier is keeping prescribed records about the operation and technical state of the supplied products on the part of the user (technical log).

The customer provides his own storage of replacement parts for post-warranty repairs in a period preceding by 13 months the required year for delivery of replacement parts.

11.4.2 Basic Software

The customer has the right to advance his claims relevant to responsibility for defects in the basic software, constituted by operating systems and the relevant user program documentation, in the form of a claim conforming to the valid Claims Regulations for Basic Software within the service life of the computer.

The right to claim errors applies only to program components of the last valid version turned over to the customer as a matter of record.

11.5 Information

Business-related information about SMEP systems is offered by the following representatives of the business sector at individual plants of Office Machines:

Prague 3	130 00	Husitska 36 Department OSVS-SMEP	27 43 51-6
Plzen	304 35	Guldenerova 9 Comrade Eng Pavel Stauber	464 03
Hradec Kralove	591 95	Resslova 935	313 21/007
Brno	601 12	Veveri 102 Comrade Miroslav Kuchta	507 07
Ostrava	701 00	Gottwaldova 203 Comrade Eng Ladislav Nemec	570 41/003
Teplice	415 23	Gottwaldova 19 Comrade Eng Stanislav Mikulu	61 21-3

12. References

--promotional literature of VUVT, ZVT, Datasystem, TESLA, Office Machines, Aritma, VUES [Research Institute for Electric Machinery], ZPA, METRA, VUMS;

--promotional literature of DEC, Intel, Siemens, Digital Research, Electronum, Izotimpex, Videoton, Robotron, Mera-Elzab, MOM;

--VYBER INFORMACI Z ORGANIZACNI A VYPOCETNI TECHNIKY, Volumes 1981, 1982, Office Machines, Prague.

Use was also made of the literature and documentation listed in chapter 6.

8204
CSO: 8112/1501

END