# SEMICONDUCTOR PACKAGING

## A DoD Dual Use Technology Assessment

### Final Report

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# Executive Summary

*This assessment concludes that commercial capabilities for single-chip semiconductor packaging are sufficient to assure affordable access to meet military needs, and no action is required by the Department of Defense (DoD). Driven by markets in telecommunications, computers, consumer electronics, and automotive systems, the integrated circuit (IC) packaging industry is able to provide the mainstream packaging technology required by the DoD. Although predominantly offshore, IC assemblers and equipment suppliers are highly competitive and diversified. Packaging materials suppliers are concentrated in Japan, but there has been no indication that access to materials will be limited or denied.*

*Commercial capabilities, that meet DoD requirements for high performance multi-chip modules (MCM) and other leading-edge semiconductor packages, are neither affordable nor sufficient. DoD/ ARPA's (Advanced Research Project Agency) advanced packaging program is improving United States (U.S.) industry capability and affordability in this crucial packaging area and this support should be continued. Access by DoD to U.S. industry capability is assured, but the DoD needs to work with industry to assure that cost-effective dual-use MCM manufacturing technologies are available for military use.*

*Increased use of plastic encapsulated semiconductors in military systems should be accelerated, but not indiscriminately. Near and long-term failure mechanisms in extreme environments for plastic packaged devices must be well characterized and understood. A physics-of-failure approach should be adopted to determine root causes of semiconductor packaging related failures.*

*Continued DoD research and development (R&D) investments in advanced packaging materials and more cost-effective manufacturing technologies will help assure that future advances in military packaging technology will be available and affordable in meeting military needs.*

U.S. national security demands that United States military forces have guaranteed, cost-effective access to the world's best technology. In their *Future Warfighting Capabilities* plan, the Joint Staff and Joint Requirements Oversight Council identified high performance electronics and semiconductor packaging as a high priority to

accomplish future mission requirements.[1] Under its dual-use strategy, the DoD will increasingly rely on commercial semiconductor packaging components and technologies to meet defense needs.[2]

Today, the defense share of the total worldwide integrated circuit (IC) market is about 2 %. Although the DoD remains an important customer for certain IC suppliers, it has lost much of its historical market power and influence in dealing with industry.

This assessment focuses on semiconductor packaging, commonly referred to as first-level packaging. Semiconductor packaging is the science and art of establishing interconnections and a suitable environment for integrated circuit chips. Both single-chip and multi-chip assemblies are addressed. The primary materials in a semiconductor package are plastic molding encapsulants, ceramics, and metals.

As the DoD moves toward greater acceptance and utilization of commercial IC packages, it must deal with the fact that most IC packaging and assembly plants, and equipment and materials suppliers are located offshore, primarily in Japan and other countries in the Far East. However, there is no indication at this time that this creates a vulnerability for the DoD. These capabilities should continue to be available to U.S. military suppliers.

The DoD has traditionally relied on hermetically sealed, ceramic semiconductor packages. In contrast, well over 90% of commercial ICs are encapsulated in plastic. However, high performance commercial ICs (microprocessors and Application Specific Integrated Circuits (ASICs)) are generally packaged in ceramics due to performance requirements and high thermal dissipation.

As the DoD moves toward increased insertion of plastic packages into its electronic systems, it must be assured that the required protection and reliability are provided against the range of storage and operating environments imposed on modern military systems.

In summary, to assure that national security requirements are maintained under a dual-use strategy, the DoD must be assured of:

- Ready access to leading-edge industrial technology developments that parallel current military requirements and ultimately enable new military capability.
- Affordable, readily available, and on-going access to commercial technology and manufacturing capability (foreign and domestic).
- A healthy, reliable, accessible semiconductor packaging manufacturing infrastructure (materials and equipment).

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[1] *Defense Science and Technology Strategy, Director, Defense Research and Engineering*, Department of Defense, September 1994.

[2] *Dual Use Technology: A Defense Strategy for Affordable, Leading-Edge Technology*, Department of Defense, February 1995.

Access to Leading-Edge Technology. Increasingly, the commercial semiconductor packaging industry is being driven by demands for higher input/output (I/O) pin count, higher chip density, and improved performance. Package configurations are moving toward small-outline, single-chip surface mount technologies of all types— low to medium performance multi-chip modules; and direct chip attach (chip on board) and three-dimensional packaging.

Driven by semiconductor packaging requirements for high performance consumer electronics, telecommunications, automotive electronics, microprocessors for computers, and application specific ICs (ASICS), the majority of commercial semiconductor packaging technology is consistent with current and future military requirements. Industry use of high pin-count ball grid arrays, tape automated bonding, quad flat pack, and a variety of other small outline, surface mount packages serves the majority of military markets.

It is not clear, however, that industry will be able to supply military demands for high performance multi-chip modules (MCMs) and related high density packaging technology. Driven by cost-performance trade-offs, industry does not yet have sufficient motivation to invest in the technology and manufacturing infrastructure required to use high performance MCMs in commercial packaging lines. To assure that military requirements for performance and cost are met, DoD R&D and manufacturing technology investments in MCMs should be continued. This issue has been clearly recognized and is being addressed by ARPA's Packaging Program and by the Technology Reinvestment Project (TRP).

This assessment also recommends continued DoD investment in advanced package substrate materials and computer design tools. Advances in these areas can improve semiconductor performance, often at reduced cost. DoD funds should be invested in partnership with U.S. industry to encourage commercial adoption of the required packaging capabilities.

Plastic or ceramic. Due to historical demand for high reliability, DoD military semiconductor packaging has primarily used ceramic rather than plastic materials with stringent testing and qualification procedures. This resulted in establishment of military specific vendors and manufacturing lines and the associated high procurement costs. In effect a niche market was created and perpetuated serving the DoD.

For direct military packages, ceramic is used almost exclusively (over 90%). However, under the DoD's Qualified Manufacturers List (QML) and its emphasis on best commercial practices, plastic encapsulated ICs are increasingly finding their way into military systems.

Most military merchant vendors support increased insertion of commercial plastic packages into military systems, but the reasons do not always have to do with reduced cost. It is not clear, under the Qualified Manufacturers List (QML), that the use of plastic encapsulated ICs will, in fact, result in significant cost savings, given the costs of

assured quality control, reliability, supplier responsiveness, traceability, obsolescence control, and supplier selection. Beyond cost, however, insertion of plastic packages into military systems allows for a broader product portfolio and more rapid access and integration of leading-edge ICs into military systems. Many ICs are available only in plastic.

The insertion of plastic packaged ICs into military systems should be accelerated, but should not be done indiscriminately. Test data shows that plastic encapsulated ICs, under most conditions, are as reliable as ceramic. However, there are legitimate concerns for long-storage life and extreme temperature and humidity environments. Failure rates for plastic encapsulated microcircuits (PEMs) vary widely from supplier to supplier. It is apparent that they could be readily used in many non-critical, relatively benign military applications. At the opposite extreme, where the ICs must perform at extreme temperature and humidity conditions and cycles, or where assured operation after long-term storage (up to 20 years) is important (missiles and other armaments), military vendors are reluctant to move away from the proven reliability of ceramic packages.

The move toward plastic should be made with a thorough knowledge of the technical trade-offs and the other issues listed above. Additional work needs to be done on the use of Highly Accelerated Stress Testing (HAST). Near and long-term failure modes must be well characterized and understood. A physics-of-failure approach should be widely adopted by the DoD to determine root causes of semiconductor packaging failures and to establish a scientific basis for evaluating new materials, structures, and packaging materials. Ongoing work at Department of Energy (DoE) defense laboratories, Department of Commerce's (DoC) National Institute of Standards and Technology (NIST), and universities should be leveraged to help develop this understanding.

The Multi-Use Manufacturing Work Panel of the Industry Task Force for Affordability is working with the military IC manufacturing industry on accelerating the use of commercial integrated circuits in military systems. The task force is directly addressing many of the issues discussed above, and may provide a mechanism to systematically address the insertion of commercial ICs into military systems.

Semiconductor Packaging Infrastructure. Worldwide IC packaging and assembly is highly competitive and primarily concentrated in Thailand, Hong Kong, Korea, Taiwan, and Japan. Whether foreign or U.S. owned, military lines on overseas semiconductor IC packaging and assembly plants are routinely QML certified. Driven by lower costs and existing infrastructure, off-shore assembly will continue for many current and future military semiconductor packages. U.S. military vendors rely on these foreign assembly plants and there are no indications that U.S. access would be denied in the future.

Leading-edge military package types, driven by finer input/output (I/O) pitch and higher precision, increasingly require fully automated assembly and inspection techniques. With this, the advantages of lower-cost, off-shore labor becomes less a

deciding factor in assembly plant location. Consequently, U.S. assemblers may be able to recapture part of this market. It is encouraging that at least one U.S. company, by focusing on high precision automated packaging, has recently become profitable while in direct competition with off-shore IC assemblers. In addition to competitive costs, on-shore packaging benefits U.S. IC manufacturers by providing shorter inventory turn times and avoids the transport back and forth between Asia, which can affect reliability.

Semiconductor packaging equipment is supported by a dozen or more competitors around the globe. The markets are competitive and geographically diversified. U.S. producers account for about a third of the market.

The world supply of semiconductor packaging materials is far more concentrated both economically and geographically. Japanese firms dominate the supply of both ceramic packages and plastic encapsulation resins. Kyocera alone supplies about two-thirds of U.S. consumption of ceramics for IC packaging. While other suppliers compete with Kyocera, U.S. and other nation's chip manufacturers have preferred to take advantage of the quality and service they receive from Kyocera. Kyocera has established a plant in the U.S. There is no indication that DoD IC suppliers would be denied access to these capabilities in the future. Further confidence is added by the existence of IBM's extensive ceramics packaging capability, which is now serving merchant markets.

Concerns have been expressed over Sumitomo Chemical's dominance of the plastic resin market. As with Kyocera, alternative suppliers are available, but Sumitomo's high quality product and service has given them a dominant market position. In the summer of 1993, a fire destroyed a major Sumitomo production facility in Ebino, Japan. Initial fears of an impending shortage of epoxy encapsulation resins were short lived and by the beginning of 1994, there was and continues to be a glut of these resins on the market with both Sumitomo Chemical and Nippon Kayaku bringing new capacity on-line and customers learning to increase their utilization efficiency.

Conclusions. At present, IC assemblers, equipment suppliers, and materials suppliers are mostly off-shore, but do not have the incentive or market leverage needed to threaten the withholding of supplies in order to gain financial or political advantage. Nor is there reason to believe DoD IC manufacturers will lose access to most leading packaging technologies. However, these dependencies should be regularly monitored to assure that economic and political conditions do not affect DoD access and create vulnerabilities.

Commercial availability of advanced MCMs is nearing the point where it can support many military demands for high performance semiconductor packages at affordable costs. ARPA programs in MCM packaging and the Technology Reinvestment Project (TRP) focus area on Low Cost Electronic Packaging are contributing significantly to the development of a U.S. based MCM manufacturing capability available to the DoD and should be strongly supported.

Our conclusions are summarized in Table 1 for a variety of critical military packaging technologies and packaging infrastructure. A list of possible DoD options for each of the technology and assembly areas is included. Issues related insertion of commercially available, single-chip packages into military systems will be addressed in an upcoming DoD study on the Insertion of Commercial Integrated Circuits into Military Systems.

Affordable manufacturing for MCMs and related flip-chip and direct chip attach are being addressed by current ARPA R&D and manufacturing technology investments, including the TRP. Support for this program is critical to assuring future, affordable DoD access to commercial, high performance MCMs.

Electromagnetic interference (EMI) resistant packaging is achieved by both IC design and packaging. The small packaging dimensions in MCMs can improve EMI resistance. In addition, EMI resistance is achieved by enclosing the entire IC package in a metal enclosure, generally a system unique, higher-level packaging concern.

Finally, continued DoD R&D investments in advanced packaging materials, computer aided design tools, and more cost-effective manufacturing technologies will help assure that future packaging technologies will be available and affordable for meeting military needs.

Table 1

**Relation of DoD Technology Investment to State of Dual Use Technology and Industrial Capabilities for Semiconductor Packaging**

| Packaging Technology | State of Technology | | | | | Possible Policy Options | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Military Unique | Access assured and commercial capabilities alone will be sufficient | Access is assured but DoD needs affordability in high-end technologies | Access is assured but DoD needs to ensure commercial suppliers can supply leading edge technology | DoD needs assured access to technology and industrial capabilities | R&D Investment | Develop and deploy new manufacturing technologies | Transition defense technology to commercial applications | Insertion of Commercial Technology |
| MCM C, D, L | | | X | X | | X | X | | X |
| 3-D MCM | | | | X | | X | X | | |
| Flip chip and Direct Chip Attach | | | X | X | | X | X | | X |
| Miniature QFP | | X | | | | | | | X |
| Grid Arrays (BGA, PGA) | | X | | | | | | | X |
| EMI resistant packaging | | X | | | | | | | |
| Radiation resistant packaging | X | X | | | | | | | |
| TAB | | X | | | | | | | X |
| **Assembly Infrastructure** | | | | | | | | | |
| Assembly | | X | | | | | X(MCM) | | |
| Packaging materials | | X | | | | | | | |
| Packaging equipment | | X | | | | | X(MCM) | | |
| New substrates | | | | X | | X | | | |
| Computer Aided Packaging Design | | | | | X | X | | X | |

# Chapter I
# Military Requirements And Semiconductor Packaging

## A. The Importance of Semiconductor Packaging

Electronics has been, and continues to be one of the fastest moving technology areas relevant to modern war fighting and conflict prevention. In their Future Warfighting Capabilities plan, the Joint Staff and Joint Requirements Oversight Council (September 1994) identified high performance electronics and semiconductor packaging as a high priority to accomplish future mission requirements. Similarly, the Department of Defense Advisory Group on Electron Devices in its deliberations on technologies of strategic importance to the military departments identified electronics packaging and interconnect technology to be of paramount importance to future military systems.[1]

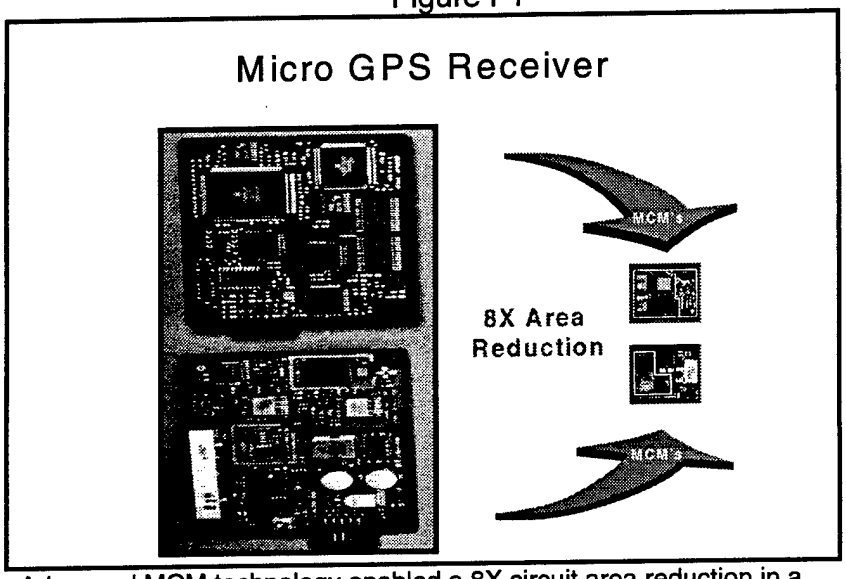
High performance electronic systems that sustain the technological leadership of U.S. military are undergirded by the key enabling technologies of semiconductor devices and packaging. Increasingly, advanced semiconductor packaging is the key enabler for smaller, lighter, lower power, more reliable, higher performance and ultimately lower cost electronic systems. Advances in electronics enable the production of new generations of weapons that provide unprecedented capabilities in land-sea-air warfare. Computational tools using advances in electronic hardware enable the rapid simulation and design of affordable future weapon. High speed processors and high density electronic packages are required for advanced $C^3I$. New ultra-compact, highly efficient microwave and millimeter-wave modules enable new concepts in unmanned airborne vehicle (UAV) radars, electronic decoys, and phased-array systems that improve our ability to defend against stealth platforms, and improve weapon accuracy in land, sea, and air encounters. In semiconductors, in general, and semiconductor packaging in particular, the DoD must be assured of early, affordable access to new semiconductor device and packaging technologies and production capabilities that are responsive to its needs when systems are under development, when they are being fielded, and when they are needed in increasing numbers for times of conflict.

Along with the standard military requirements that include reliable operation in severe environments (temperature, humidity, and EMI) and ruggedness, new systems will demand increased processing speed, reduced size and weight, and low power operation. Advanced semiconductor packaging is essential to continue increased military semiconductor device performance to enable proliferation of portable systems, wireless data communications, and other needed future defense capabilities. The dramatic impact of advanced semiconductor packaging in military systems is illustrated

[1] *Special Technology Area Review On Electronic Packaging*, Report of the Department of Defense Advisory Group on Electron Devices, Office of the Under Secretary of Defense for Acquisition, Washington, DC 20301-3140, July 1993.

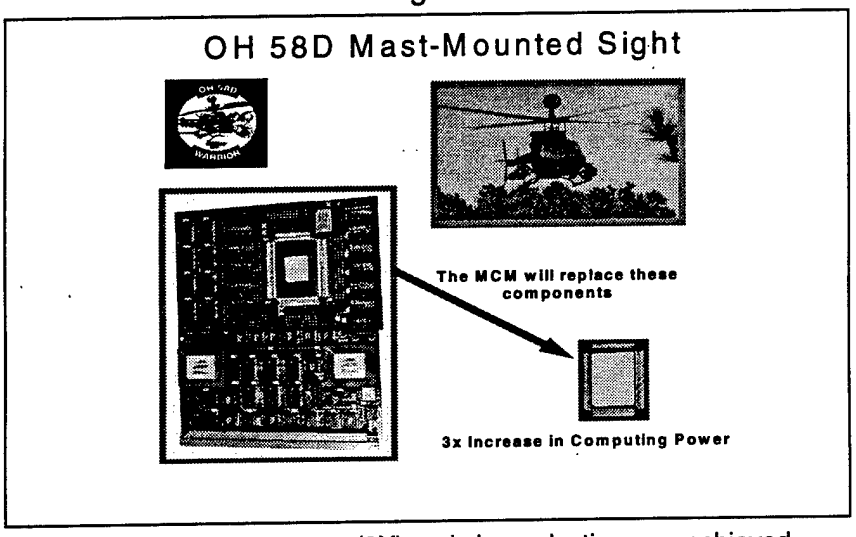
in Figures I-1 and 2. In these systems, the use multi-chip-modules (MCMs) allowed for much higher clock speed; more than doubled reliability; significantly increased system density while decreasing size, and weight; and demonstrated the rapid transition from system design to insertion.

Figure I-1




Advanced MCM technology enabled a 8X circuit area reduction in a military hand-held global positioning sensor (GPS) unit without sacrificing performance.

Figure I-2




Increased computing power (3X) and size reduction was achieved by using MCM technology in an OH 58D helicopter mask mounted signal processor unit.

## B. Focus of Assessment

This assessment of semiconductor packaging addresses military semiconductor packaging requirements, summarizes the status of the packaging industry, and issues related to meeting national security needs. To ensure that national security requirements are maintained under a dual use strategy, the DoD must be assured of:

- Ready access to leading-edge industrial technology developments that parallel current requirements and ultimately enable new military capabilities.
- Affordable, readily available, and on-going access to commercial technology and manufacturing capability (foreign and domestic).
- A healthy, reliable, accessible semiconductor packaging manufacturing infrastructure (materials and equipment).

This assessment focuses on the enclosures protecting the individual IC chips or dice, generally referred to as first level semiconductor packaging. The assembly of a complete system generally involves several levels of packaging. Subsequent levels of packaging provide interconnections among the IC modules including printed circuit boards (PCBs), card cages, backplanes and cabling.

For semiconductor packaging, DoD must address the following issues:

- Abandoning, to some degree, its long-standing reliance on hermetically sealed IC packaging to increase use of commercial semiconductor packages.
- Adoption of commercially acceptable qualification procedures and reliability standards.
- Assurance that current and projected dependence on foreign packaging companies, material suppliers, and equipment vendors provides the required quality, are dependable, and provide timely access.
- Assurance that industry's R&D and advanced manufacturing capabilities are sufficient to meet emerging military requirements.

This assessment is being conducted as a part of an ongoing dual use technology and industrial assessment of semiconductor capabilities by the Office of the Assistant Secretary of Defense (Economic Security). This assessment integrates and builds upon a number of recently completed and ongoing activities, including:

- Interagency Specialists Group on Electronic Packaging Government/Industry Report on Packaging Roadmaps and Strategies (ongoing).
- Department of Defense study on Insertion of Commercial ICs into Military Applications (in process).
- DoD Assessment of Semiconductor Devices and Manufacturing (in process).
- Japan Technology Evaluation Center Assessment of Packaging Technology in Japan (in process).

- U.S. Department of Commerce's National Institute of Standards and Technology Report on the Metrology and Data for Microelectronic Packaging and Interconnection Workshop (May 1994).
- U.S. Army Missile Command's Study of the Use of Plastic Encapsulated Microcircuits Versus Hermetically Sealed Microcircuits For Meeting Missile System Mission Critical Reliability Requirements (June 1994).
- The National Economic Council and National Security Council Interagency's Assessment of the Competitiveness of the Electronics Packaging Industries in the United States (March 1994).
- DoD Microcircuit Planning Group's Final Report on the Commercialization Status and Progress Report for Implementing the Defense Science Board Recommendations on Microelectronics (October 1993).
- The Department of Defense Advisory Group on Electron Devices Special Technology Area Review on Electronics Packaging Technology (July 1993).
- The Department of Defense Advisory Group on Electron Devices Special Technology Area Review on Microwave Packaging Technology (February 1993).

This report provides interim findings on the status of the semiconductor packaging industry and issues related to meeting national security needs. Since the Interagency Specialists Group on Electronic Packaging is an on-going activity, and other aspects of the overall semiconductor assessment are still in process, this report provides an interim perspective on the status, issues, program and policies. In particular, policy and program measures intended to foster greater use of plastic encapsulated microcircuits in military applications will be included in an assessment of the insertion of commercial integrated circuit technologies now being completed.

# Chapter II
# Semiconductor Packaging Technology

## A. Introduction

Semiconductor[1] packaging, commonly referred to as "first-level packaging,"[2] is the science and art of establishing interconnections and a suitable operating environment for integrated circuits. This assessment focuses on the technology and processes involved in packaging an integrated circuit (IC) efficiently, reliably, and affordably.

The typical microelectronics package is designed to provide the following structures and functions:

- Signal distribution: Connections for signals to and from the silicon chip.
- Power distribution: Connections for providing electrical power to the chip.
- Thermal management: A means of removing the heat generated by the ICs so that they stay within an allowable temperature range.
- Circuit protection: A structure to support and protect the chip from moisture, electromagnetic spectrum radiation, temperature, and mechanical vibration and shock.

Plastic, ceramic and metal materials are the primary materials that go into the fabrication of semiconductor packages.

## B. Background

The Joint Electronic Design Engineering Council for Semiconductor Packages (JEDEC) now lists well over 1000 registered outlines of packages ranging from 4-pin dual-in-line packages (DIP) to 400-pin Quad-Flat Packs. Some common semiconductor packages in use today are shown in Figure II-1.

For many years, beginning in the 1960s, the dual-in-line (DIP) package was the dominant IC package type, both in ceramic and plastic. The development of DIP was undertaken largely for the United States government, primarily for avionics and satellites. The DIP package, both plastic and ceramic, has been the mainstay of integrated circuit packaging for many years and will remain in high-volume production for years to come. However a number of factors began to work against the DIP.

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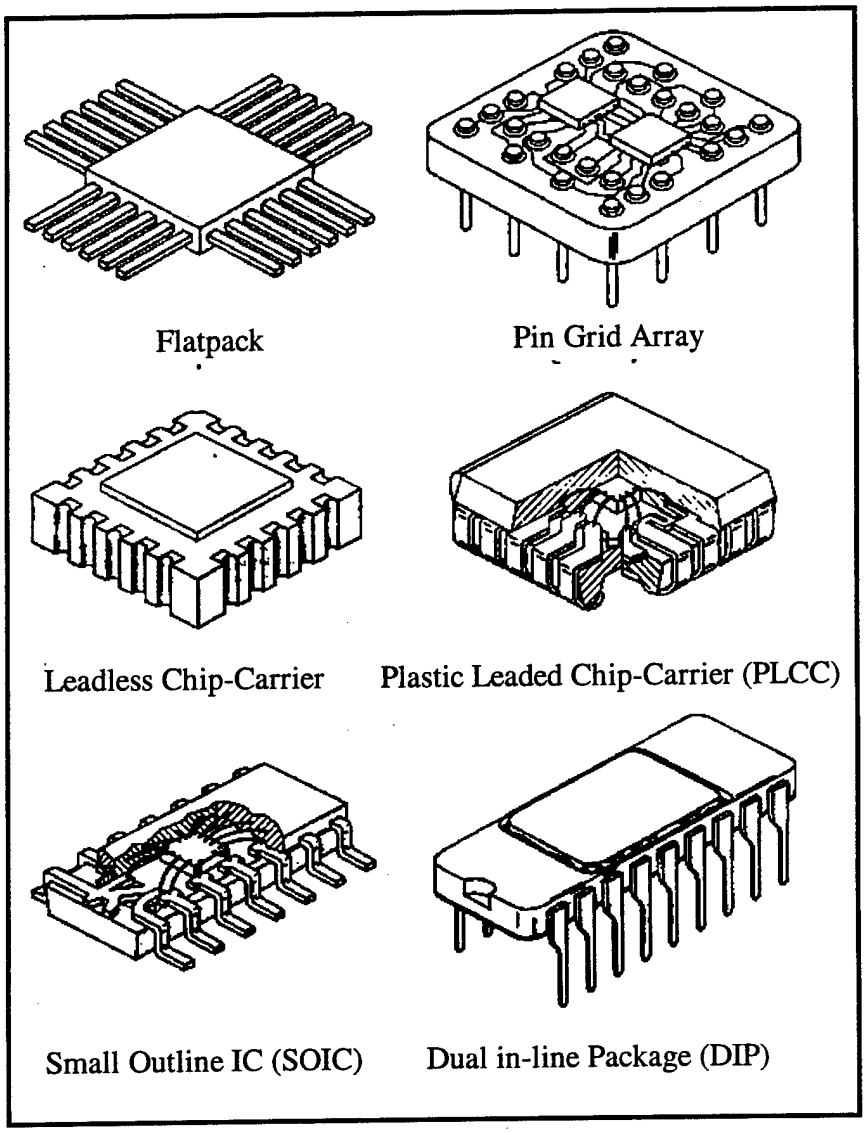
[1] Semiconductor and microelectronics are used synonymously in this assessment. An integrated circuit is a specific type of microelectronics device containing both passive and active components. Today's ICs can contain up to several million transistors on a single silicon chip.

[2] Second-level packaging is the attachment of the substrate onto the circuit card and third-level packaging is the attachment of the circuit card into higher levels of the system.

One was the development of very large scale ICs (VLSICs) and ultra large scale ICs (ULSICs), both high input/output (I/O) pin-count devices.

To accommodate VLSICs and ULSICs the DIP became very large and the associated speed reduction due to increased signal propagation time created performance problems. In addition, the opening of the consumer electronics market required more power in a smaller package.

Figure II-1
**Semiconductor Packages**

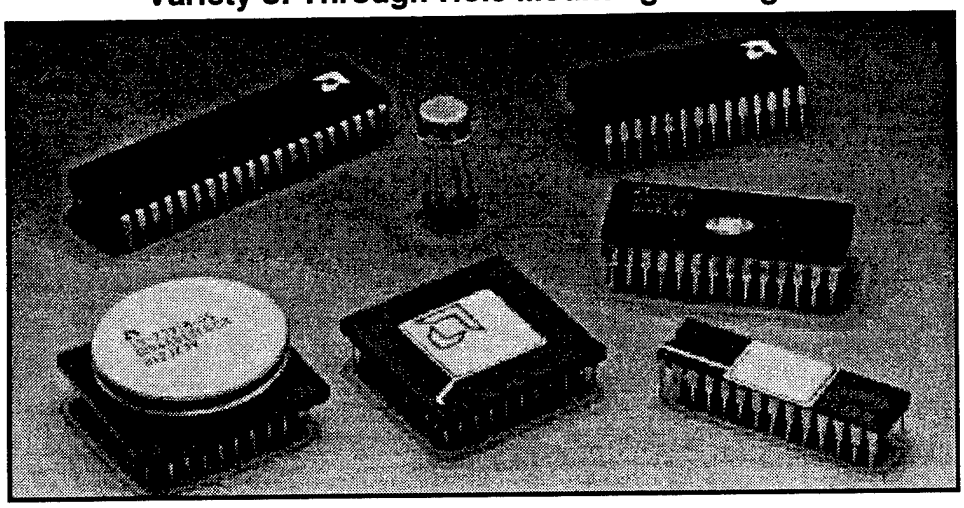



Source: *Principles of Electronic Packaging*, McGraw-Hill Book Company

Two solutions to these problems were the pin-grid-array (PGA) and surface-mount packages. Figure II-2 depicts a variety of through hole mounting packages, both DIPs and PGAs.

Figure II-2

**Variety of Through-Hole Mounting Packages**



Source: Integrated Circuit Engineering Corporation

PGA packages are currently available with several hundred leads and can readily dissipate large amounts of heat. The PGA is a through-hole type IC package with rigid pins protruding from the bottom of the package. The ceramic PGA, first developed and used in volume by IBM, is the dominant version of this package type, however plastic PGAs are also available. Although popular for high pin-count applications, the PGA has several inherent disadvantages:

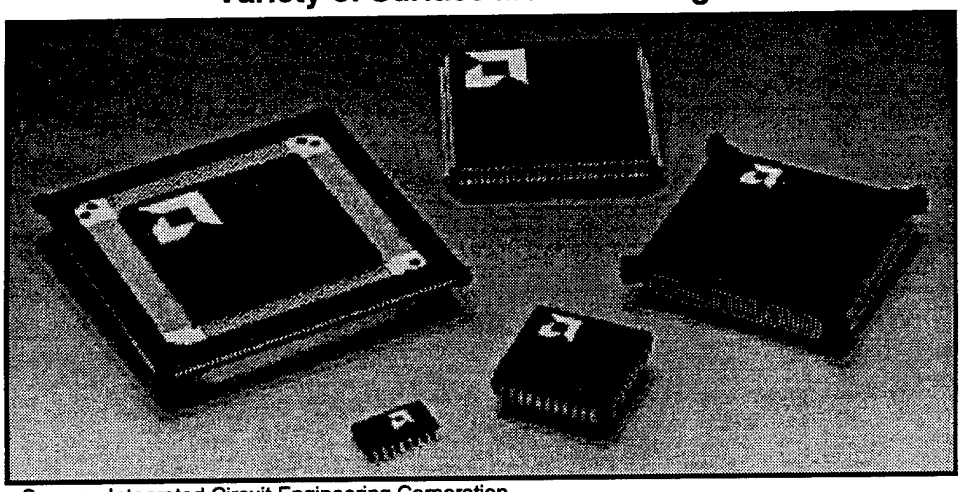
- The PGA package can consume a large amount of printed circuit board (PCB) area.
- The layout of the PCB interconnections becomes increasingly difficult as the number of PGA package pins increases.
- If the PGA is soldered directly to the PCB, it is virtually impossible to remove, especially for higher-pin-count versions, without damaging the PCB.
- The ceramic PGA is one of the most expensive IC packages and is driven by the cost of the ceramic substrate, fabrication, and by the number of pins. Plug-in sockets are available for ceramic PGAs.

Surface-mount technology (SMT), similar to the PGA, allows for I/O pin counts in the 100's while maintaining high speed performance. The early SMT packages included the small-outline IC (SOIC) and the leaded-and leadless chip-carrier. To mount either a DIP or a PGA package, a hole must be drilled in the printed circuit board for each package pin. The surface-mount-package, however, eliminates the need for these

holes, permits high pin counts, and its smaller size is suitable for high speed performance.

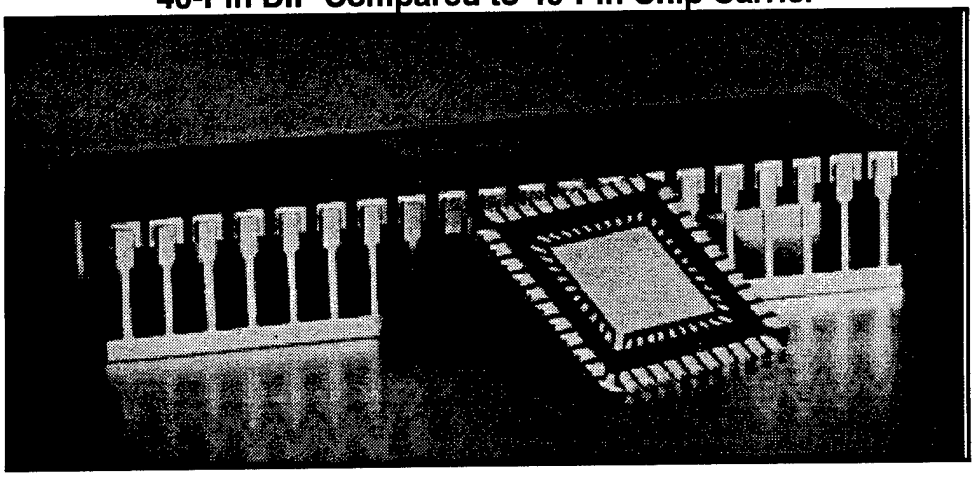
Surface mount packages developed in the late 1970s and 1980s included small outline (SO) packages; leadless and leaded chip-carrier; and quad-flat pack. SMTs are available in both plastic and ceramic versions depending on the application. Once again, the development of many of the SMTs were motivated by U.S. military demand for high I/O density and high performance. As with DIPs, most of the SMTs are now widely accepted by commercial industry. Figure II-3 shows a variety of surface mount packages, while Figure II-4 illustrates the dramatic packaging density improvement with surface mount technology.

Figure II-3
**Variety of Surface Mount Packages**



Source: Integrated Circuit Engineering Corporation

Figure II-4
**40-Pin DIP Compared to 40-Pin Chip Carrier**



In the 1990s, new packaging technologies are being developed to meet the requirements of increasing I/O density and high-speed performance. These technologies include ball grid arrays (BGA), area array TAB, chip-on-board (COB), and 2-D and 3-D multi-chip modules (MCMs), and wafer-scale integration.

In most of the above packaging configurations, the IC chip is attached to a substrate that contains a conducting structure for external power and signal connections. The substrate also serves to transfer heat from the chip. In a ceramic package, the chip is mounted on a ceramic substrate on which the conductors are deposited by thick-film technology, often in multi-layers. In plastic packaging the chip is mounted on a metal leadframe and the chip and leadframe are encapsulated in plastic by injection molding.

The IC chip is attached to the conducting structure in several ways. For both ceramic and plastic packages, the most popular is wire-bonding where the chip is attached to the conductor terminals with very small wires from contacts on the chip to the substrate conductors. Flip-chip, another method of attachment, uses an array of small solder balls over the surface of the chip to both physically attach the chip to the substrate and make the required electrical connection. IBM was an early pioneer in flip-chip technology with their controlled-collapse chip connection (C4) process. As an example of the connection density achievable by flip-chip, Fujitsu recently introduced a flip-chip interconnection (bump interconnection) that will allow connection pitches as small as 0.12 mm (4.8 mil), with I/O counts from 300 to 600 on areas of 200 $mm^2$ to 500 $mm^2$.

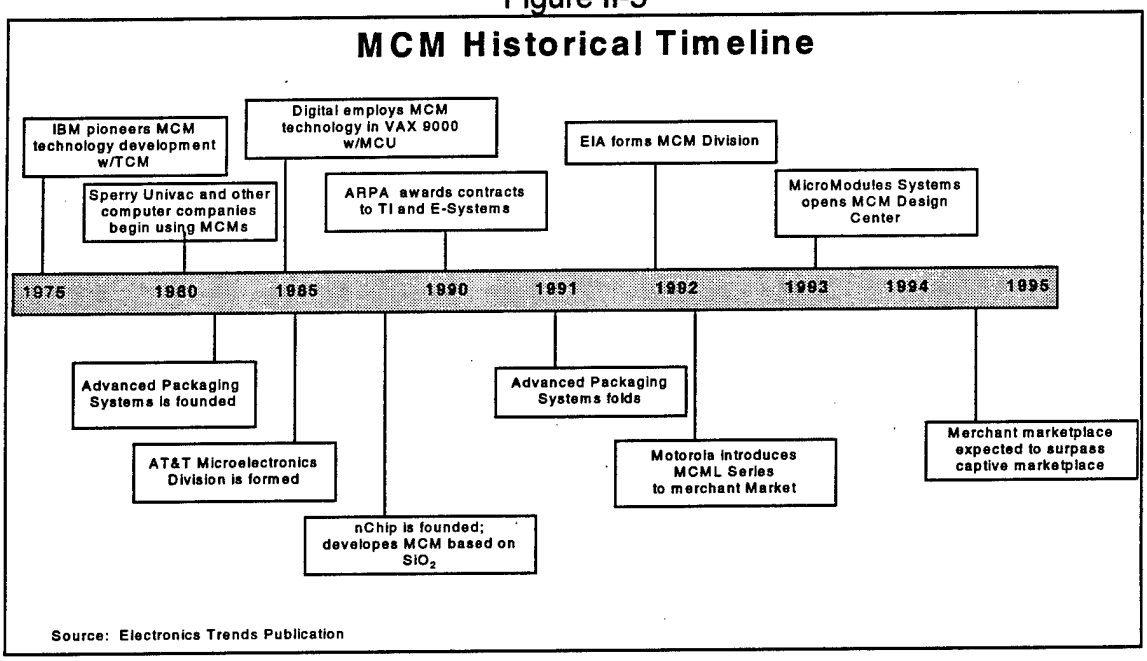
A packaging technique receiving considerable attention in the 1990s is the multichip-module (MCMs). Many large computer, telecommunications, and aerospace manufacturers are using, working on, or considering designs that include MCMs. The term multi-chip module has been used for at least 25 years. The definition of an MCM varies widely ranging from a number of single chip modules mounted on printed wiring boards to modules using multi-layer substrates of cofired ceramic with thin film conductive layers on top.

The rapid growth in interest is due in part to the advances in IC capabilities which require a new packaging strategy to effectively employ the potential cost performance of these devices. A second reason is the long-standing research and development efforts of the leading vertically integrated innovators in the U.S., such as IBM, AT&T, DEC, Honeywell, and Rockwell, as well as the merchant vendor innovators, such as Raychem, Polycon, Texas Instruments Micro Module Systems, and n-CHIP. These firms, often with the support of DoD, have developed new technological solutions to packaging challenges. Through their pioneering efforts, stimulated in part by strong competition from Japan, high density MCMs are now penetrating the U.S. merchant world. Figure II-5 outlines the development of the MCM beginning with IBM's introduction in 1975, to introduction of MCM technology into the merchant market.

The one common element to all MCMs is form factor. An MCM is a highly functional module that looks like either a large single-chip package or a small printed circuit card. It has three general features:[3]

- Offers better performance density per unit cost than conventional single chip packages on printed circuit boards.
- Is a unit of exchange between vendors and customers with a clean interface and looks like a single chip module package or a printed circuit board.
- Is often an intermediate step, until a single chip solution is available, that reduces the time to market for a new product.

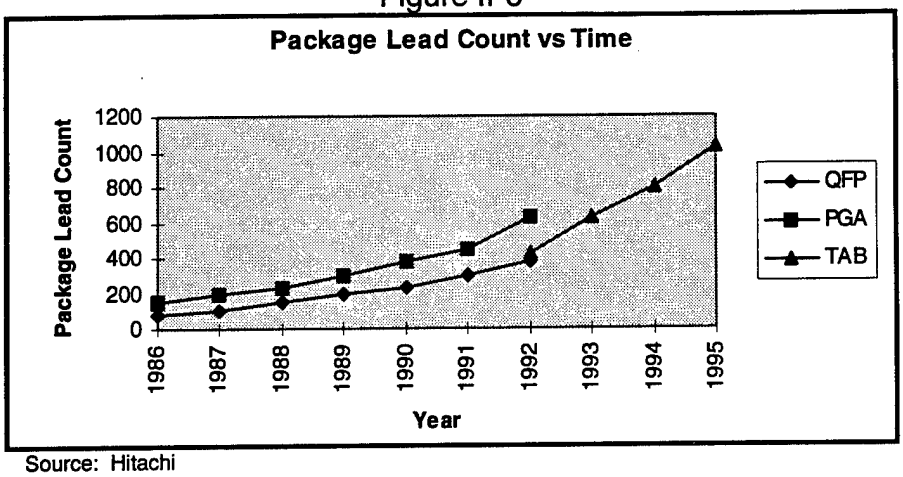
Figure II-5




With increasing pin-counts, and the increasing use of multi-chip modules, there has been more interest in the use of tape-automated-bonding (TAB). TAB is basically a leadframe that is deposited onto a film carrier. Some of TAB's benefits include being able to test and burn-in bare chips, to simultaneously bond up to 1000 leads, small lead pitch, and its compatibility with very thin packages. Most of TAB's problems come from the high entry cost, the expense of applying gold bumps to the die, and the difficulty of reworking TAB devices. Bumping a wafer for TAB is not an easy process. Figure II-6 illustrates that TAB packages allows for packages with up to 1000 I/O leads.

[3] Eric Bogatin, *High Performance Packaging Solutions,* Integrated Circuit Engineering Corp., 1991.

Figure II-6




Source: Hitachi

## C. Plastic Packages

Many applications use plastic encapsulated microcircuit (PEMs) packages due to their small size and low cost. They are generally one-half to one-tenth the cost of comparable ceramic or metal packages. In 1993, approximately 98% of all integrated circuits were packaged in plastic. Plastic packages are usually constructed by injecting a molding compound into a form that already contains the semiconductor device attached to a metal leadframe. Molded plastic packages are non-hermetic and maybe vulnerable to moisture related failures. A typical plastic package assembly flow along with associated percentage manufacturing costs, as shown in Figure II-7, starts with separation of individual ICs from the processed wafer and proceeds through final packaging and shipping. Wire bonding and molding account for nearly 50% of the cost.

However, the protection of ICs from degradation caused by the presence of moisture at high temperature has been the subject of intense study during the past twenty years or so. A large body of Highly Accelerated Stress Testing (HAST) and field-use data indicate that newly developed materials and techniques can provide excellent protection against moisture induced damage and allow PEMs to compete favorably with hermetically sealed ceramic and metal packages. Plastic package integrity has been progressively improved through better materials, increased purity of the molding material, higher-quality device passivation,[4] improved leadframe designs, continual design iteration, and manufacturers' quality procedures.

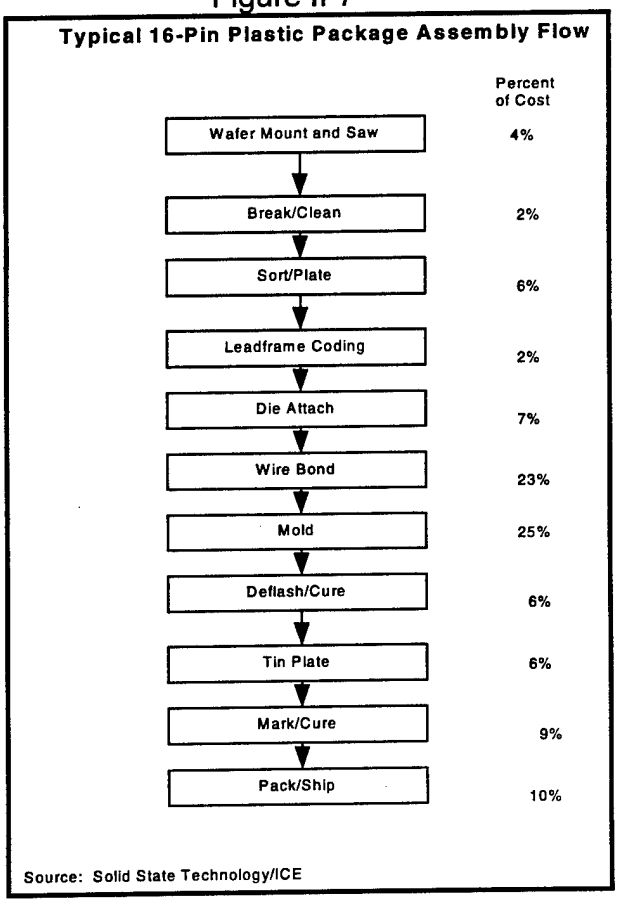
However, before plastic packages can be widely used in critical, high reliability military applications, it will be necessary to develop standardized and uniform test techniques for evaluating the protective properties of coatings. The decision to use or not to use plastic packages in military hardware must be based on the specified

[4] Dr. Sorin Witzman at Northern Telecom reports that moisture associated failures occur only if the passivation layer is broken due to an initial manufacturing defect or after field delamination and thermal cycling. In the absence of defective parts, moisture had no effect on field reliability. Private communication, July 1995.

operating environment, storage conditions, storage user-period, user reliability conditions, and the availability of reliability data. ICs that operate continuously in a controlled environment are excellent choices for plastic packages. The heat generated during operation tends to keep the package drier and prevents much of the absorption of moisture. Applications where power and temperature are cycled cause the IC to breathe-in moisture on each cooling cycle and then tends to drive the moisture outward during the next heating cycle. This can lead to device failure.

One of the predominant failure modes in plastic packages is corrosion of metal pads and other chip metallurgy. The potential for corrosion failures results from the combination of chemicals that may be outgassed internal to the package and the moisture that permeated the plastic package. This moisture can combine on the chip and/or lead bond surfaces with ionic species that may be present in the package from numerous sources. Most IC failures are chemical in nature and are influenced by temperature. Another failure mechanism in plastic packages (and to a lesser degree in ceramic) is interconnection wire breaks and bond fractures due to temperature cycling, and materials with dissimilar thermal coefficients of expansion.

Figure II-7



However demonstrated performance, approaching that of hermetically sealed packages, along with the benefits of lower material costs, less complex fabrication, and reduced testing are driving the movement toward wide acceptance of plastic packages in both commercial and military markets.

## D. Ceramic Packages

Applications requiring hermeticity, extremely high thermal dissipation, or operation in extremely harsh environments use ceramic packages. Examples include defense and space systems, leading edge microprocessors, and some industrial electronics. Ceramic packages are generally manufactured by a merchant supplier, who provides the completed packages to the semiconductor manufacturer or contract assembler for incorporation of the IC and final sealing. Ceramic packages simplify device reliability since the package does not come into contact with the active surface of the device and, when hermetically sealed, is completely impervious to moisture, air, and ionic contaminants that can harm the IC. The materials used in ceramic packages also offer a higher degree of thermal conductivity as compared to plastic packages,[5] making them useful when the IC dissipates more than a few watts or is used in a high temperature environment.

Ceramic package product categories:

- Crystal oscillator carriers: multi-layer, surface mounted products used to package oscillating crystals in timing devices, computer applications, and fuses for military munitions.

- Ceramic packages incorporating ceramic components joined with glass (frit) or epoxy seals include:
  - CERDIP (ceramic dual-inline package) - each package includes both a top and bottom member.
  - CERQUAD - like a CERDIP, but with flat leads on all four sides.
  - CERPACK - single layer, surface mount flat package including both a top and bottom member, with flat leads exiting parallel to the seating plane from the frit glass on two opposite sides.

- Multi-layer ceramic packages include:
  - MCM-C
  - Ball grid array
  - Pin grid array
  - Ceramic quad flat pack

[5] With an embedded heat spreader and thermally conductive epoxy, the heat dissipation of a plastic package can be excellent.

The manufacturing process for ceramic IC packages is outlined below:

1. A powder (usually aluminum oxide) is combined with a binder, a plasticizer and solvents in a ball mill. The resulting slurry is formed into long strips of "green tape" whose thickness is in thousandths of an inch.
2. The flexible tape is spool fed to either a manual or computerized punching machine, which punches vias (electrical path), tooling holes, cavities for the IC, and registration holes. Holes in the tape are coated so that they can be filled with a conductive (tungsten or molybdenum-based) paste for electrical connections.
3. A metallization pattern is placed on the tape, in a process similar to silk-screening, using a standard thick film screen printer. For multi-layer cofired ceramic packages, constituent tape layers will then be laminated together by pressing between heated platens. The part's final shape may be cut after lamination.
4. The lamination layers are next fired ("sintered") at an elevated temperature. Following firing, nickel plating is applied, to create a wettable surface, to facilitate adhesion of items, which will be subsequently brazed to the fired surface.
5. Leads, I/O pins, and/or seal rings are brazed onto the fired parts. After brazing, a protective nickel layer and a final corrosion-resistant conductive gold layer are applied to the product surface. This is followed by final inspection and testing.
6. Die attach.
7. Wire bond.
8. Lid seal.

## E. Metal Packages

Metal packages are primarily used for discrete transistors and small ICs, requiring only a few leads. Military hybrids and some high frequency applications also use metal packages, as they provide electromagnetic shielding for the device. The complexity of passing leads through the conducting metal body of the package without shorting makes extendibility to higher lead counts difficult.

## F. Multi-Chip Approaches

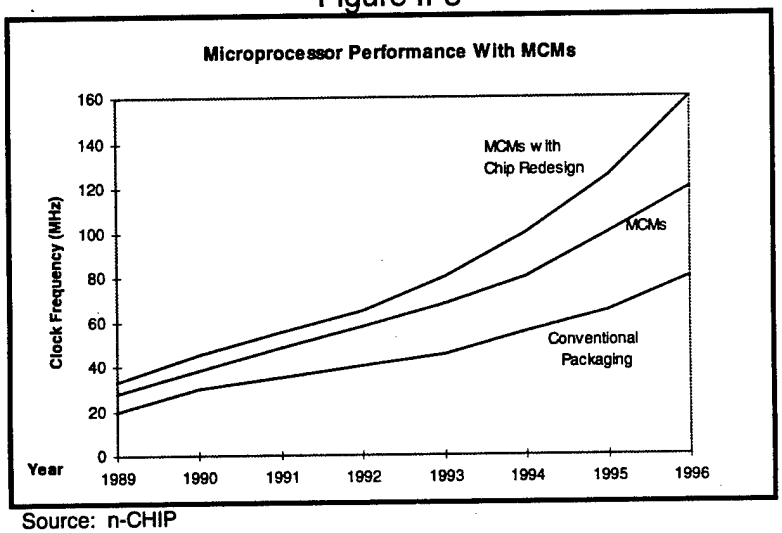
Semiconductor packages mainly house a single IC. However, most circuits consist of multiple ICs in single chip modules (SCMs) interconnected on a printed wiring board (PWB). Two alternatives to interconnecting a number of ICs on a PWB are chip-on-board (COB) and multi-chip modules (MCM). In MCMs, groups of bare die are interconnected within each module using some form of high density wiring substrate prior to assembly onto a PWB. In chip-on-board, the "bare" chips are directly attached to a PWB, eliminating the first-level packaging altogether. Both approaches yield

substantial gains in system performance, reliability, and compactness. Improved system performance for MCMs primarily results from faster circuit speed (clock frequency) due to reduced propagation time delay, Figure II-8.

Three approaches evolving from different technology bases are being used to implement MCMs. Laminated MCMs (MCM-L), an extension of PWB technology, use a multilayer laminate to perform the interconnection function. MCMs-L are the least expensive multichip substrate and represents the least expensive route to improved performance. A laminated MCM-L is generally not repairable.

Ceramic MCMs (MCM-C) are multichip modules, utilizing the thick-film technology generally associated with hybrid circuit fabrication on ceramic substrates or multilayer ceramic packages. MCMs-C are used in moderation in high performance (>100 MHz) applications. An MCM-C is a cofired ceramic, hermetic substrate, pioneered in the 1980s and used extensively in military/aerospace environments, supercomputers, and in medical electronics. Its ability, to support vias through the ceramic, makes the technology good for modules that have pin grid array (PGA) interfaces with printed wiring boards.

Figure II-8




Source: n-CHIP

MCMs-D are multichip modules in which, at a minimum, the signal lines are created by the deposition (D) of thin-film metal and dielectric materials in multilayer structures. MCMs-D are used for high-performance (>100 MHz) applications. In an MCM-D, the substrate is based on an interconnection pattern, formed by sequentially deposited dielectrics and conductors on a base substrate, typically by thin-film processes. This is the highest density and performance approach but also the most expensive of the MCM approaches. Whereas, MCMs-L cost from $1 to $3 per square inch, the MCM-D costs in the neighborhood of $20-plus per square inch. For a specified functionality, however, MCM-D may require a much smaller substrate area than an MCM-L. Figure II-9

summarizes the major problems associated with MCMs. Figure II-10 depicts the substrate cost vs. wiring density for the three MCM types.

Figure II-9

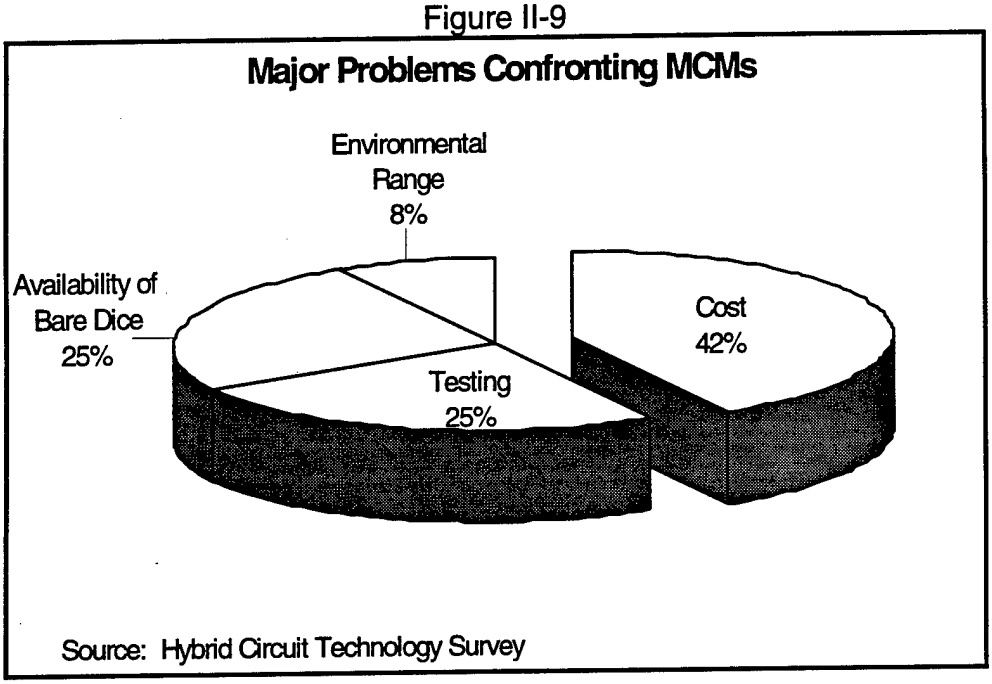
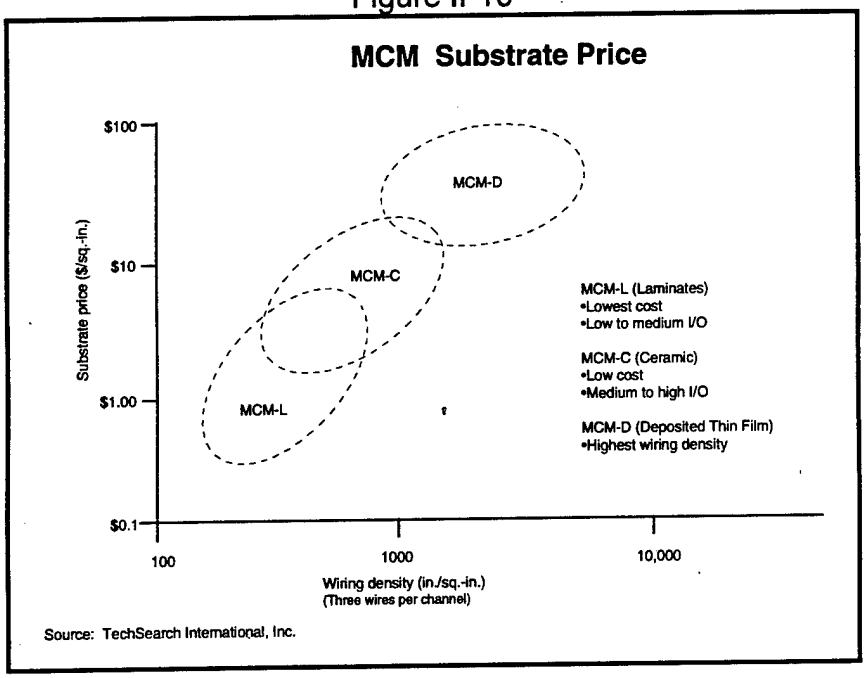


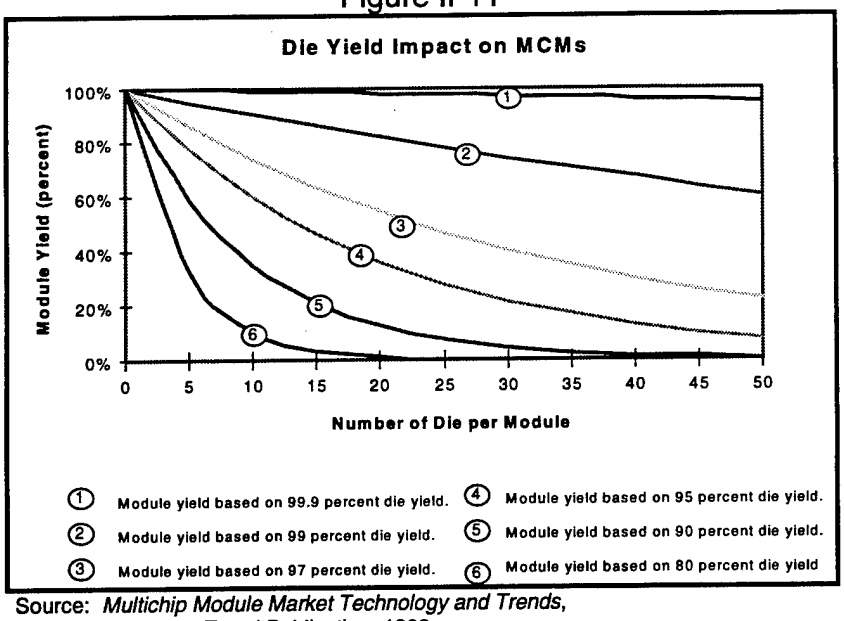

Figure II-10




A significant factor for MCMs is the lack of an IC manufacturer infrastructure in place to fully test, successfully deliver, and warrant bare IC chips. The known-good-die

(KGD) issue is an essential ingredient to establishing an MCM infrastructure. Many semiconductor suppliers are reluctant to sell bare chips. Figure II-11 shows the importance of high-yielding good die in an advanced MCM.

Figure II-11




Source: *Multichip Module Market Technology and Trends*, Electronic Trend Publication, 1993

Several industry-led consortiums have been formed to help spur development of MCMs, several of which are funded by the Technology Reinvestment Project. The MCM-L consortium led by Sheldal is a vertically integrated consortium whose objective is to develop very fine-line laminate technology for MCM-Ls. The MCM-D consortium includes Hughes Aircraft, Boeing, MicroModule Systems, n-Chip, Sandia, and SEMI. It is primarily focused on equipment development for large area (e.g., 24"x12"), low-cost substrate panels for MCMs-D. An MCM-C consortium, that includes Alcoa and Coors, is nearly finalized.

## G. Summary

Semiconductor packaging encompasses a wide range of technology streams, including materials, mechanical processes, and electrical. The primary trade-offs in semiconductor packaging include cost, size and weight, functionality and performance, quality and reliability, and energy consumption. In many cases, miniaturization will continue to drive the development of semiconductor packaging technologies. Semiconductor packaging roadmaps indicate advances in component-mounting density and semiconductor packaging materials.

Technical developments in packaging are targeted to the ultimate goal of "package-less" systems, i.e., bare chip-on-board and wafer-level integration. However, due to its low cost and established infrastructure, single chip packaging will likely dominate the market in terms of volume well into the future.[6] The use of ball grid array, MCM-L and MCM-D and packages using flip-chip technology will increase through the end of this century. Advances in "chip-scale" packaging, with the package approaching the size of the chip, are leading to further miniaturization of IC packages.

[6] "Has the Packaging Revolution Finally Run Out of Steam?," *Semiconductor International,* Feb. 1995.

# Chapter III
# Semiconductor Packaging For Military Markets

*A strong and growing dependency exists between our national defense capability and the semiconductor industry.*[1] *Semiconductor packaging is increasingly crucial to the performance of military electronic systems and strongly impacts system cost.*

## A. Impact of Semiconductor Packaging on Performance and Cost in DoD Systems

Semiconductor packaging technology for DoD electronic systems are best understood in the context of emerging military requirements. Broadly stated, new military electronic systems will be smaller, lighter, smarter, more mobile, lower cost, faster, more data intensive, and more tightly coupled to human senses. To a large extent, future warfighting capabilities will depend on advances in:

- Communications
- Intelligence gathering, analysis, and distribution
- Precision strike
- Platform, vehicle, and weapon control
- Battlefield situational awareness
- Command and control
- Sensor data processing
- Human interface

To a large extent, these capabilities are enabled by advanced semiconductor packaging technology. Packaging can increase integrated circuit density by 10-100X, improve system performance by 2-10X, reduce power consumption by 10-30%, increase reliability by 10-100X and allow for multiple analog and digital technologies in a single module.[2] Along with greatly improved performance, advanced semiconductor packaging can reduce the cost of military electronics.

Trends in semiconductor packaging for the military include:

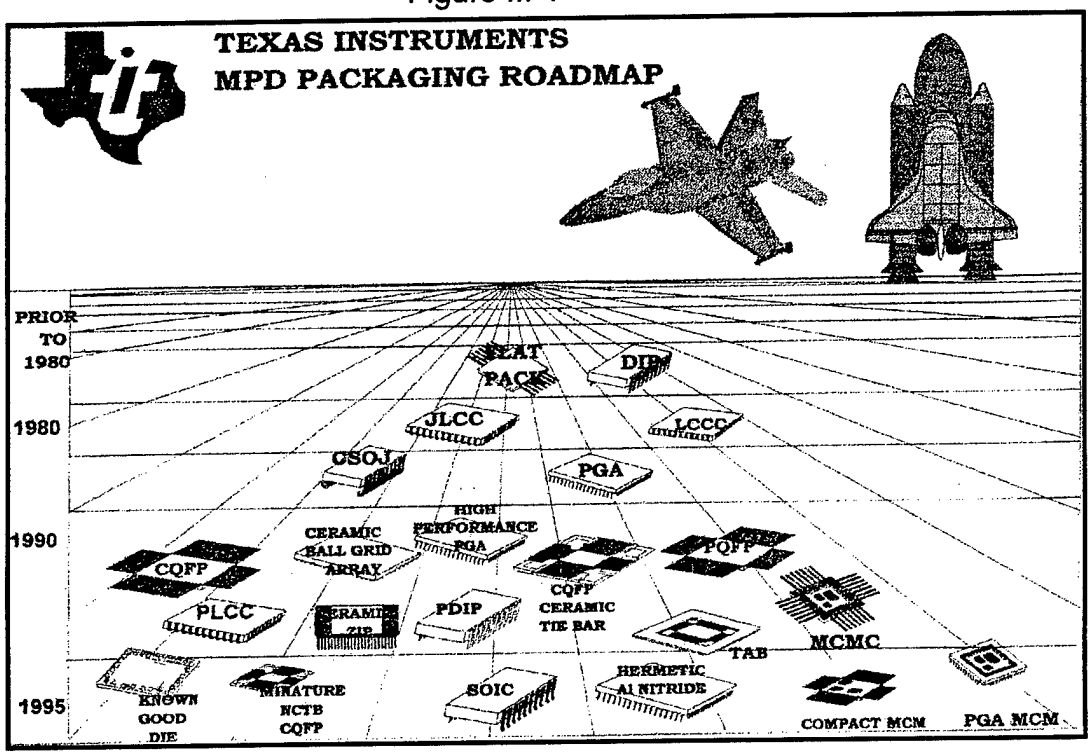
- greatly reduced use or elimination of single-chip packaging
- increased movement toward area array I/O board connections
- high density interconnections to match I/O density

[1] *Special Technology Area Review on Electronics Packaging*, Report of Department of Defense Advisory Group on Electron Devices, July 1993.
[2] "Electronic Packaging and Interconnect Strategy," Nicholas J. Naclerio, ARPA Electronic Packaging and Interconnect Conference, Feb. 1995.

Fortunately for the DoD, many of the packaging technologies being developed and used by industry for the emerging information age overlap new military semiconductor packaging requirements. Military IC packaging has progressed from low density, limited performance IC packages prior to 1980, to the present proliferation of high pin count, high performance surface mount technologies, TAB, and MCMs. In the future it is expected that these technologies will be further refined, high performance MCMs will be used increasingly, and direct chip attachment to the circuit board will increase.

Figure III-1 depicts the migration in military IC packaging from low density, limited performance IC packages prior to 1980, to the present proliferation of high pin count, high performance surface mount technologies, TAB, and MCMs. In future years, these technologies will be further refined, high performance MCMs will find increased use, and direct chip attachment to the circuit board will increase.

Figure III-1




Source: Military Products Division, Texas Instruments

Electronics represents over 40% of the procurement cost of many military systems and increasingly, semiconductor packaging is a major cost-driver. The vast majority of military ICs (>90%) contain die (bare chips) that are identical to those used in commercial applications, or that are commercially manufactured application specific integrated circuits (ASICs) similar to those made for commercial customers. Therefore, while the cost of the die for commercial and military ICs is generally equivalent, the

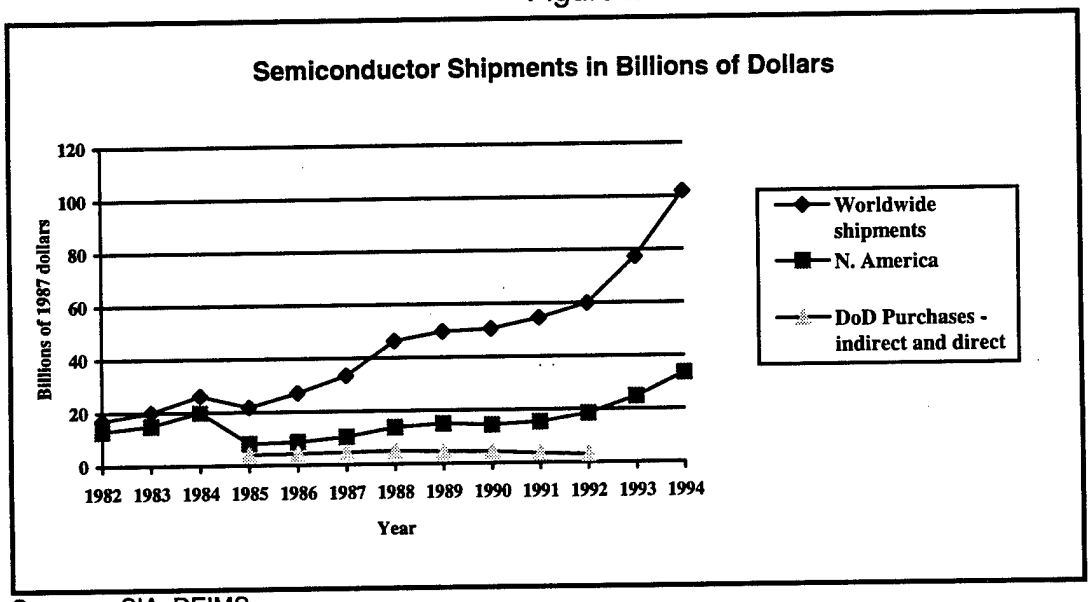
unique packaging and assembly, extensive testing, and qualification processes contribute to large (5 to 10x) cost differences between military and commercial ICs.

## B. DoD Market

*The defense share of total IC market purchases is small, exerts minimal influence in industry, and is dominated by ceramic packages*

As shown in Figure III-2, the defense share of total market purchases of semiconductors has been small and declining over time. With relatively constant military purchases, the DoD's market share is shrinking due to the rapid increase in commercial market sales. Currently the defense share is estimated at about 2%. DoD's entire annual demand for ICs of about $1.2 billion is far less the global demand for Intel's 486 microprocessor chip.[3] When compared to total worldwide IC merchant usage, Figure III-3, the total military share is only about 5%.[4]

Figure III-2

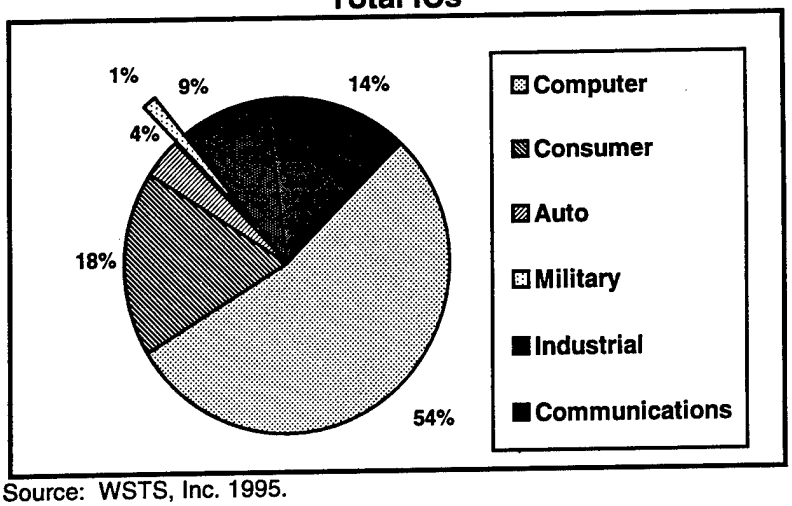



Sources: SIA, DEIMS

[3] "Acquisition Reform and Moving to the Best Commercial Practices: A Look at the Microelectronics Industry," B. A. Kausal, Briefing, Sept. 6, 1994. Mr. Kausal was the chairman of the Commercial Acquisition Streamlining Team (CAST) for the microelectronics industry.

[4] *Status 1993: A report on the Integrated Circuit Industry*, Integrated Circuit Engineering (ICE) Corporation, 1993.

Figure III-3
**World Semiconductor Trade Statistics**
**1994 Annual End Use Survey**
**Total ICs**



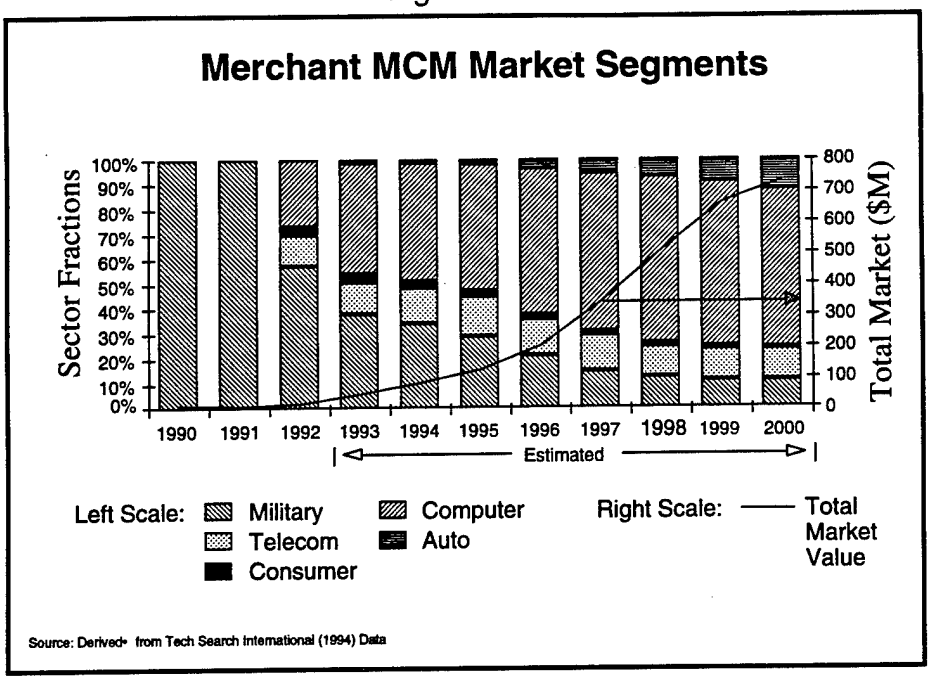

Source: WSTS, Inc. 1995.

Although DoD has critical needs for semiconductors and remains an important customer for certain IC suppliers, it has lost market power and influence in dealing with industry. Two leading defense suppliers, Motorola and Advanced Micro Devices (AMD), recently announced that they will stop producing MILSPEC devices.[5] The top five remaining military suppliers are: Harris Semiconductor, National Semiconductor, Analog Devices, Texas Instruments, and Intel. Their combined sales in 1993 were $630 million. Although not yet tabulated, sales for 1994 are expected to be about the same.[6]

For MCMs, the military market share is shrinking due to increasing commercial demand for MCMs of all types (Figure III-4). The military segment of MCM applications was the main driver for the technology in the late 1980s and continues to support many of the manufacturers. In 1992, military applications accounted for 55% of merchant MCM revenues (Figure III-4). Though the military MCM market is declining in terms of percentage of total revenues it should increase in terms of actual revenues. The military applications segment is expected to account for about 20% of total 1996 MCM revenues, or $40 million. It should decrease to less than 10% by year 2000, but military MCM purchases are projected to increase to about $70 million.

[5] "Motorola and AMD Exit Military," Rayner, C. P., *Military and Aerospace Electronics*, Vol. 5, No. 13, Dec. 1994. For discussion of MILSPEC see next section of this chapter.
[6] ICE, 1995.

Figure III-4




## C. Current DoD Practices

*Due to an emphasis on high reliability, DoD military semiconductor packaging was primarily implemented in ceramics and subjected to stringent testing and qualification procedures. This resulted in establishment of military specific vendors and manufacturing lines and in high costs per unit.*

DoD was an initial driving force in the early development of ICs. The first significant use of these devices came in 1962, when Texas Instruments (TI) was awarded a contract to design and build integrated circuits for the improved Minuteman missile system. Additional demands followed from the NASA Apollo Program, and the U.S. government sponsored development of large, high-performance main frame computers. DoD and NASA demands dominated the IC market during the early and mid-1960s, accounting for about 70% of sales. DoD was also a path breaker in establishing standards and tests for IC reliability.

Throughout the 1960s and 1970s, MILSPEC was the hallmark of top quality in the military and commercial markets. Manufacture of ICs in the 1960s and 1970s was more of an art form than a science, so the quality control methods that emerged relied heavily on tests and screening of finished components. To assure MILSPEC reliability, hermetically sealed IC packages became the standard. At that time, manufacturing processes were not well understood and thus were inadequately controlled. Therefore, 100% percent testing was required to assure required reliability.

Even with substantial gains in process know-how, and with manufacturing processes under much greater control, DoD continued until recently to rely on long-standing "high-reliability" specifications, standards, end-of-line testing and screening, and expensive packages (ceramic). In effect DoD has created and perpetuated a niche industry serving DoD alone. Today over 90% of commercial ICs (units) are packaged in plastic, while over 95% of DoD ICs are packaged in ceramics.[7] Due to differences in suppliers, packaging, and quality assurance requirements, military ICs cost from five to eight times the cost of standard commercial-industrial devices (Figure III-5).

In 1989, DoD took a major step toward establishing a framework for quality assurance designed to be more compatible with commercial semiconductor packages by adopting the Qualified Manufacturer List (QML).[8] With QML, a manufacturing line, with its attendant quality control process, is audited and qualified, instead of qualifying each semiconductor device individually. Any parts built on a QML approved line are considered qualified. The QML approach incorporates an industry technical review board and statistical quality controls with Defense Electronic Supply Center (DESC) oversight.

Since QML allows for the deletion of non-value-added processes, it is considered to be a performance-based specification. That is, rigid screening requirements are not mandated by QML--only the ability of a QML device to meet the requirements for military applications. As such, the onus for product quality and reliability is placed with the semiconductor supplier and is not relegated to a rigid cookbook of mandatory tests and screens. Under QML, off-shore assembly and packaging is permitted and many military semiconductor suppliers extensively use off-shore facilities. Over 90% of ceramic packages used in defense are produced off-shore.[9]

While a thorough examination of the progress and impact of changing electronics qualification methods and standards is outside the scope of this assessment, it is apparent that by adopting QML the DoD is increasingly moving toward the adoption of commercial packaging qualification procedures.

DESC is making significant progress in getting IC producers to adopt QML certification. As of June 1994, DESC had about 71 microprocessors and over 6000 other types of ICs that met QML. Part of the success lies with the program having the full endorsement of most of the major semiconductor manufacturers. QML reduces government and OEM quality audits of IC manufacturers, and emphasizes process control and flexible testing, i.e., best industry practices.

---

[7] David R. Graham, Herschel Kanter, Michael Pecht, Steven Yencho, "A Dual-Use Strategy for Microcircuit Packaging," Alexandria, VA: Institute for Defense Analyses, IDA Paper P-3060, Feb. 14,1995.

[8] For a more complete discussion of DoD quality control procedures, including QML, Standard Military Drawings (SMD), Qualified Parts Lists (QPL), and MIL-STDs, see "A Dual Use Strategy for Microcircuit Packaging," IDA Paper P-3060, Feb. 14, 1995.

[9] *The Effect Of Imports Of Ceramic Semiconductor Packages On The National Security: An Investigation Conducted Under Section 232 of the Trade Expansion Act of 1962*, PB 93-192441, U.S. Department of Commerce, August 1993.

Figure III-5
**Electronic Packaging Characteristics by Market Segment**

| Market Segment | Operating Range | Packaging Type | Testing Required | Sources and Cost Ratio (relative to consumer) |
|---|---|---|---|---|
| **Military (MILSPEC)** | **-55$^0$ to +125$^0$ C** | **Hermetic** | **MIL-STD 833**<br>**• Full temperature testing**<br>**• Quality assurance testing**<br>**• Baselines controlled** | **Die - U.S.**<br>**Package - Global**<br>**Cost Ratio:**<br>**5X to 10 X** |
| **Military (QML)** | **-55$^0$ to +125$^0$ C** | **Hermetic and plastic** | **Qualified Manufacturers List (QML)** | **Die - Global**<br>**Package - Global**<br>**Cost Ratio: 5X - 7X** |
| Commercial - High reliability | -55$^0$ to +125$^0$ C | Hermetic or plastic | End -of-line testing is optimized - emphasis on statistical process control | Global<br>Cost Ratios:<br>Hermetic: 2X to 3X<br>Plastic: 1.8X to 2.5X |
| Commercial - Industrial | -40$^0$ to +85$^0$ C (variable) | Hermetic or plastic | Emphasis on statistical process control<br>Minimal quality assurance testing | Global<br>Cost Ratios:<br>Hermetic: 1.5X to 2X<br>Plastic: 1.2X to 1.5X |
| Commercial - Consumer | 0$^0$ to 70$^0$ C | Plastic or hermetic | Emphasis on statistical process control<br>Minimal quality assurance testing (at 25$^0$ C) | Global<br>Cost Ratio:<br>Plastic: 1X |

Source: DoD Microcircuit Planning Group, Commercial Status

While recognizing this progress, some argue that QML does not go far enough and that continuing test requirements carried over from MIL-STD-883 still imposed on QML

production lines directly impact semiconductor packaging.[10] One view is that "QML still demands that the IC supplier support a military organization in addition to its commercial organization....While liberalizing QML is a move in the right direction, maintaining separate military lines is no longer justifiable."[11] In sum, the military specification system continues to evolve and there is disagreement over the extent to which commercial packages should be incorporated into military applications. While the QML process has distinct advantages over previous quality assurance methods, its success will depend critically on how it is implemented.

## D. Trends

*Semiconductor packaging in military systems will increasingly use commercial semiconductor packages. MILSPEC criteria will give way to commercially-accepted, processed-based reliability data. Driven in part by ARPA, high-performance, low-cost MCM technology should increasingly find its way into commercial and military systems.*

The ability to field weapons systems that meet new requirements, that can be upgraded to meet future operational requirements, and that have affordable life-cycle costs, depends largely on our ability to adapt or exploit commercial electronics. Because the DoD will be required to achieve required performance at an affordable cost, the semiconductor packaging used in military systems will be driven by technologies and techniques largely developed and used in industry. This is supported by Secretary of Defense Perry's vision for simplification of the way the Pentagon buys military systems.[12] As part of the mandate, the Secretary directed the military Services "to use performance and commercial specifications and standards instead of military specifications and standards, unless no practical alternative exists to meet user needs." Continuing pressure to move beyond QML to certification and adoption of industry IC reliability standards will pave the way to broader use of commercial packaging technology.

Driven by steady advances in industry, military semiconductor packaging will increasingly move toward surface mount, area array packages, MCMs of all types, and direct-chip-attachment techniques and wafer-level integration. Much of this will use plastic encapsulants. Cost-performance tradeoffs will drive the selection of packaging technology.

As previously stated, ceramic packages have been the technology of choice for military applications. However, a growing body of evidence presented in both industry literature and scientific journals indicates that the principal failure mechanisms of plastic

[10] Graham, et. al.,*Op. Cit.*
[11] Edward Hakim, Carl Rust, Wisty Olsson, "Beyond the Qualified Manufacturers Line,". Annual Reliability and Maintainability Symposium, January 1995.
[12] Secretary of Defense William Perry, "Acquisition Reform: A Mandate for Change," February 24, 1994.

encapsulated microcircuits have been successfully controlled.[13] This is due to improvements in materials, design, and manufacturing. Plastic encapsulated microcircuits (PEMs) are now generally as reliable, on average, as ceramic packaged circuits over a wide range of environments, with the possible exceptions of highly corrosive (high humidity, high temperature) and long-term storage.[14] For example, the failure rate of plastic packages has decreased from about 100 per $10^6$ device-hours in 1978 to about 0.05 per $10^6$ device-hours in 1990.[15] Further, studies comparing plastic encapsulated devices with hermetic devices show that they are approximately equal in reliability in harsh environments, with plastic having higher reliability in some cases.[16] However, there is considerable controversy, not so much whether plastic packaging should be used in military systems, but to what extent, in what applications, and how to qualify them.

It is evident that PEMs can be successfully used for many military systems and should result in significant cost savings. The implementation of DoD acquisition reform measures will likely accelerate the use of plastic packages in future military systems. Many applications can achieve the benefits of PEMs under most environmental conditions. However, it is not clear that plastic encapsulated microcircuits (PEMs) should be used for all DoD applications. Examples include electronics continuously exposed to high-humidity, high-temperature environments. Reliability data remains scarce regarding long-term storage of military electronics and a reliable cost study comparing PEM vs. hermetic IC cost has not been done. There is a diversity of views throughout the military and industry over the use of PEMs versus ceramic packages.[17]

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[13] Papers on this subject include: Brizoux, M. et al., "Plastic Encapsulated ICs in Military Equipment Reliability Prediction Modeling," *Quality and Reliability Engineering International,* Vol. 8 (1992) pp. 195-211; Condra, L. and Pecht, M. "Commercial Microcircuit Options in Military Avionics Systems Demand Reliability," *Defense Electronics,* (August 1991) pp. 43-47; Condra, L., O'Rear, S. Freedman, T., Flancia, L., Pecht, M., and Barker, D., "Comparison of Plastic and Hermetic Microcircuits Under Temperature-Humidity Bias," *IEEE Trans. Comp. Hybrids Manufacturing Tech*nology, 15,5 (October 1992), 640-650; Crook, D. L., "Evolution of VLSI Reliability Engineering," *Proc. 1990 International Reliability Physics Symposium,* (March 1990) pp. 2-11; and Watson, G. F., "Plastic-Packaged ICs in Military Equipment." *IEEE Spectrum* (Feb. 1991).

[14] *Proceedings of the Case Studies Symposium on the Successful Use of Commercial Integrated Circuits (IC) in Military Systems, Vol. II,* Sponsored by the Industry Task Force on Affordability, Alexandria, VA, June 13-15, 1994.

[15] Watson, *Op. Cit.*

[16] A study done by Rockwell-Collins compared plastic mounted devices against ceramic packaged devices in a 3532 hour temperature cycling test. The parts were cycled every 4 hours between -40 and $+85^0$ C. in 85% relative humidity with 5 v. dc bias --- a test designed to simulate a worst-case avionics environment. The failure rate for plastic devices was 1.6% per $10^6$ hours; the rate for ceramics was 6.1% per $10^6$ device hours.

[17] For two opposing viewpoints, see "Why the DoD Will Use Plastic Encapsulated Microcircuits," *Military and Aerospace Electronics,* Sept. 20, 1993. Edward Hakim, Chief, Component Reliability Branch, Army Research Branch, Fort Monmouth, NJ, and "Why the DoD Should Be Wary of Plastic Encapsulated Microcircuits," Noel E. Donlin, *Military and Aerospace Electronics,* Jan. 1994.

Multichip modules (MCM) are growing in importance for both commercial and defense applications. Military applications, such as radar, electronic warfare, communications, and smart munitions all require microwave or millimeter wave electronics that will increasingly rely on MCM packaging. The market for MCMs is divided into segments ranging from high performance, high cost packaging (MCM-C and MCM-D) to more moderate performance, lower cost packaging (MCM-L). Military demand for MCMs is generally driven by high performance, high packaging density, and high reliability. The modules will find increased usage in high performance, portable military electronic systems where size and weight are at a premium.

Currently the primary barriers to wide acceptance of MCMs by industry are:

- Availability/Yield
- Cost
- Assembly/Test
- Die Availability
- Reliability

To assure long-term DoD access to commercial MCM technology that meets demanding military requirements and is affordable, ARPA is making MCM technology, design, and manufacturing a high priority in their Electronic Packaging and Interconnect program. ARPA's investments in MCMs includes development of new substrates for improved heat dissipation, higher speed, and reduced manufacturing costs. Working closely with industry, they are developing flexible design tools and manufacturing process that reduce the cost of MCM modules.

ARPA accomplishments to date include: development of several new or improved substrate technologies; establishment of merchant MCM foundries for meeting DoD needs at IBM, Motorola, and n-CHIP; several new computer-based MCM design tools and design kits; bare-die test and standards at major IC vendors; significant standard package cost reduction; and demonstrated rapid turn around time from design to tested MCMs.

DoD is jointly funding two MCM consortiums--one for each MCM-L and MCM-D technologies--with industry providing the remaining funding. The common goal is to reduce manufacturing costs while improving performance and reducing size of MCMs to the point where DoD needs are addressed through dual use manufacturers.

Although hurdles such as high prices and lack of standards have stifled acceptance of MCMs in the past, use of the technology, in large part due to ARPA's efforts, should, for the near term, grow in areas such as smart munitions and satellites. The capability of MCMs to interconnect large numbers of chips in one-tenth the area of conventional approaches will have substantial positive impact on the cost and performance of weapons systems.

# Chapter IV
# Semiconductor Packaging For Commercial Markets

*Historically, IC packaging has not been a high priority for the semiconductor industry. In part, this resulted from the fact that sophisticated packaging methods were seen as secondary to the need to improve both IC performance and production yields. Now, however, packaging technology is increasingly seen as a limiting factor to semiconductor performance. Demands for more I/O, higher performance, faster speed, and better thermal management are placing a new emphasis on packaging. Some semiconductor manufacturers now view packaging as a key element of product differentiation.*

This section summarizes the technology and application drivers and trends for commercial semiconductor packaging, including multi-chip modules, and three related categories of packaging infrastructure: [1] enterprises that test and package chips; [2] suppliers of the bonding, molding, pressing, trimming, finishing, inspection and other equipment used in semiconductor packaging; and [3] material suppliers.

## A. Semiconductor Packaging Industry Drivers and Trends

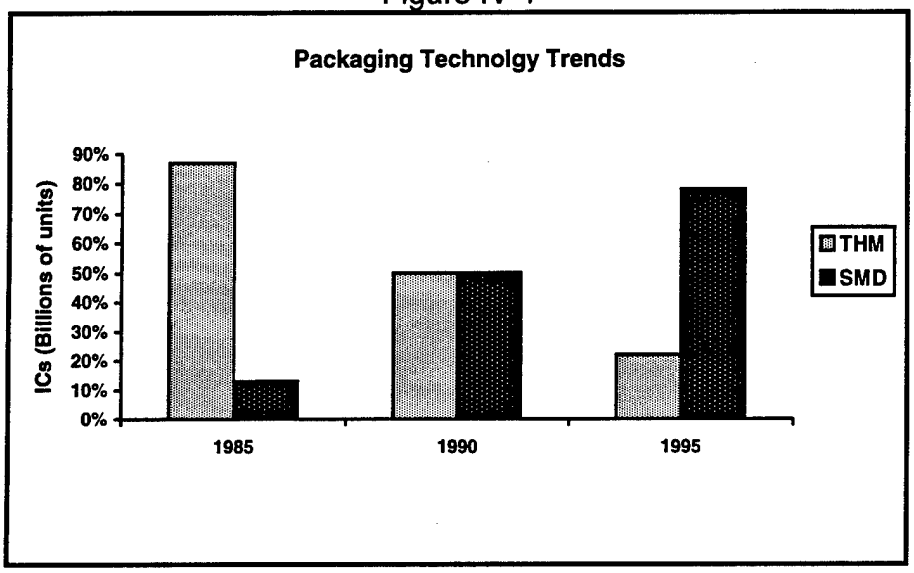
*For future semiconductor products, the need is for semiconductor packages that are smaller, thinner, lighter, and cheaper. The trend is toward high pin count, area array surface mount technologies, and direct chip attach technologies. Use of MCMs is increasing.*

There are two distinct sectors of the semiconductor packaging market--one driven by size and cost reduction, and the other by performance enhancement. The two are currently following different technology paths, but their long-term trends should converge.

For future semiconductor products, the need is for semiconductor packages that are smaller, thinner, lighter, and cheaper. These products include integrated circuits for such applications as memory cards, consumer electronics, and portable telecommunications. These applications are now primarily implemented in single-chip, plastic packages. According to the Semiconductor Industry Association's (SIA's) 15 year technology roadmap for packaging, these applications are likely to migrate to smaller, thinner plastic packages, chip-on-board (COB), and simple multi-chip modules (MCMs). To minimize board or MCM area, flip-chip processes increasingly will be used. This eliminates area or height that would have been taken up by the package or leads and reduces the amount of packaging materials consumed.

The semiconductor industry has been steadily moving toward surface mount devices (SMD), away from through-hole mounting (THM) (Figure IV-1). This movement is changing the packaging industry and successful packaging equipment vendors are taking advantage of this growing market by manufacturing equipment flexible enough for easy changeover for THD to surface mount and from one SMD configuration to another.[1]

Figure IV-1




Source: VLSI Research Inc.

At the high performance end of the product spectrum are microprocessors and Application Specific Integrated Circuits (ASICs), which require higher clock speeds, increased lead counts, and greater power dissipation. To meet the requirements of these important, high margin products, the package must provide shorter, more controlled electrical paths, more conductive thermal paths, and far more interconnects between ICs. The Ball Grid Array (BGA) package, offering higher assembly yield, shorter electrical paths and requiring less board area, will likely be used for many of these applications. The SIA roadmap predicts a migration to flip-chip, and high performance MCMs throughout the remainder of the decade.

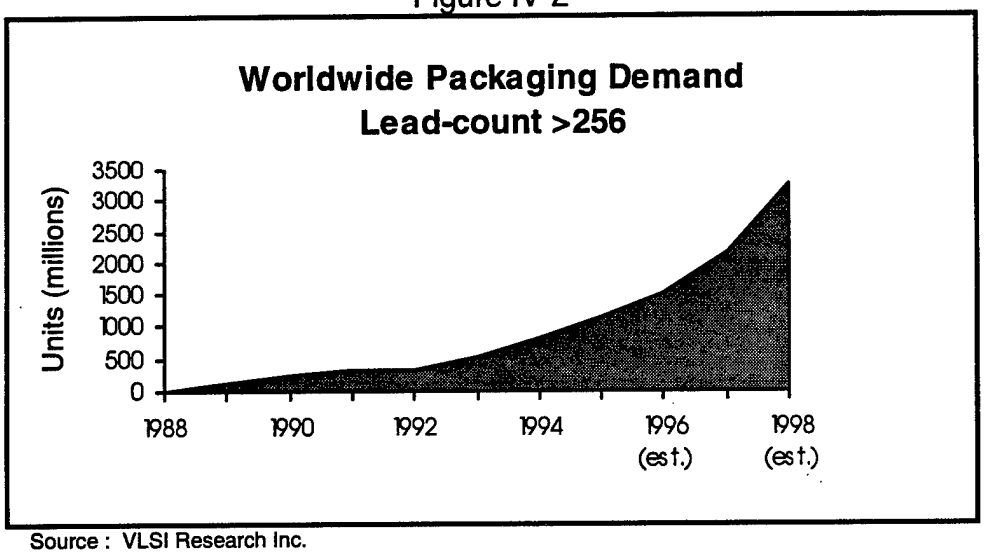
Data and projections clearly indicate significant movement toward higher lead-count semiconductor packages (Figure IV-2).[2] Although in terms of units, small lead count (<60) devices[3] still dominate the market by more than two orders of magnitude, the highest growth rate is for the high-lead count packages. Projections for 1998 show market share for packages with lead counts of 256 or greater will be about 2%, up from

[1] VLSI Research, 1992.
[2] Ibid.
[3] In 1993, 2-4 lead-count packages led at 101.4 billion units; 17 - 24 lead-count devices were second at 13.5 billion units. Packages with > 256 lead-count was last at 519 million units. By dollar value, high leadcount packages account for more than 70% of revenues.

0.3% in 1993. This reflects the increased demand for higher density, higher performance semiconductor devices.

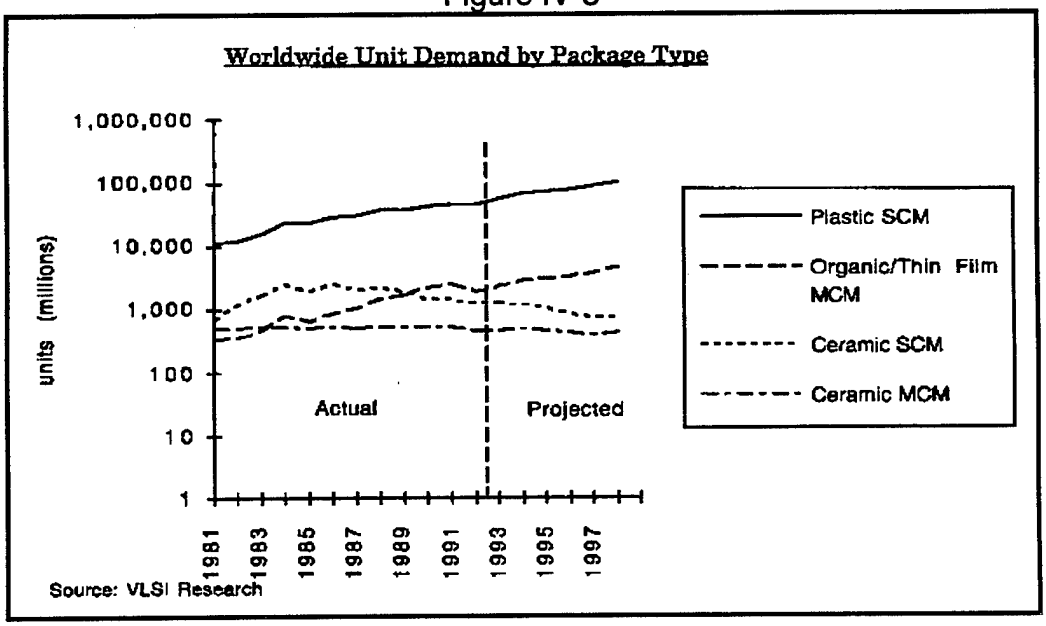
In terms of actual and projected units, Figure IV-3 shows the worldwide unit demand for plastic and ceramic single chip modules (SCM), and for organic/thin film (MCM-L) and ceramic (MCM-C) multichip modules. Due to their low cost, steady growth is anticipated for plastic SCMs and MCM-Ls. The decline in unit volume for ceramic packages is primarily due to the decline in demand for ceramic DIPs (CERDIPS), the simplest pressed ceramic packages used for certain types of memories and simple military ICs.

Figure IV-2




Source : VLSI Research Inc.

Figure IV-3



The loss in sales revenue from CERDIP packages is offset by increased sales of ceramic pin grid arrays (CPGAs), a much more expensive type of multi-layer ceramic package used for microprocessors and ASICs. CERDIP production facilities are generally not convertible to CPGA production, which requires a multi-layer ceramic process.4

In summary, the worldwide packaging/assembly market is moving toward:[5]

- Increasing lead count of microprocessor and logic devices
- Thinner packages for memory devices
- Tighter lead-pitch (spacing) to reduce footprint or to move from perimeter to area array packages
- Multi-layer plastic high performance packages
- Growing use of ball grid arrays
- Increasing use of low-cost MCMs
- Chip size packages

## B. Semiconductor Packaging Infrastructure

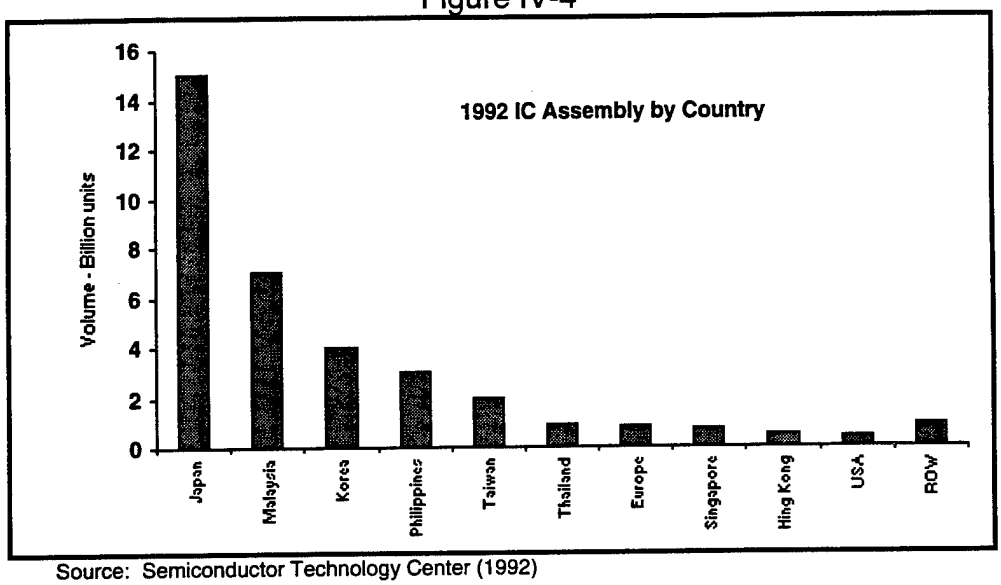
*Seventy-nine percent of assembly by U.S. manufacturers is performed offshore by a mix of captive and contract assembly houses. The breadth and diversity of firms competing in the packaging market indicates that it is a highly-competitive market, both for simple, high volume packaging, and for more advanced, high density packaging. The equipment market is especially competitive and geographically diverse. Packaging materials supply, especially for plastic packages, is primarily concentrated in Japan.*

Semiconductor packaging is done by semiconductor manufacturers or their contract assemblers. In the case of plastic packages, this means purchasing molding compound and leadframes, attaching the integrated circuit (IC) to the leadframe, molding and sealing the package around the IC and leadframe, finishing and marking the IC, and package inspection. In the case of ceramic packages, metal packages, or MCMs; components must be bought and assembled. Large systems companies may also specify and/or purchase single chip or multi-chip packages (MCMs), especially when the MCM will incorporate die from multiple users.

To reduce costs most semiconductor manufacturers have relocated their package assembly operations to low labor-cost regions, particularly in Asia (Figure IV-4). According to SEMATECH, 79% of assembly operations by U.S. manufacturers are located offshore by a mix of captive and contract assembly houses.

[4] "Enhancing the Competitiveness of U.S. Electronic Packaging Industries," Nicholas Naclerio, National Economic Council, March 1994.
[5] "Packaging and Assembly Market Trends," Subash Khadpe, SEMI Industry Strategy Symposium, January 1993.

Figure IV-4




Source: Semiconductor Technology Center (1992)

IC Packaging Companies - Table IV-1 identifies the twenty-one leading commercial packaging companies (listed alphabetically).[6] Three of these firms are headquartered in the United States, but most semiconductor packaging firms are located in Asia, including Japan, Korea, Philippines, Hong Kong, Taiwan, and Thailand. Three of the companies offering BGA packaging are American-owned. The breadth and diversity of firms competing in the packaging market indicates that this is a highly-competitive market, both for simple high volume packaging, as well as for more advanced, high density packaging.

Semiconductor Packaging Equipment - The semiconductor packaging equipment market is the largest single segment of the assembly equipment market. Overall it accounts for about 5% of the total semiconductor equipment market, a figure that has remained relatively constant during the past decade.[7] The packaging equipment market is made up of vendors selling processes and equipment used to encase and label dice in their protective cases, protect the dice from the environment, and inspect the package for proper functionality. Packaging equipment can be further segmented into three submarkets, with the following revenues in 1992:

- Molding and Sealing $296 million
- Finish and Marking $116 million
- Package Inspection $41.6 million

[6] *The Worldwide IC Packaging Foundry Market,* Electronic Trend Publications, 1994. The survey does not include leading defense packaging suppliers, because the list is from a market survey aimed at the commercial marketplace. Hence it understates packaging capabilities offered by U. S. companies.
[7] VLSI Research, op cit.

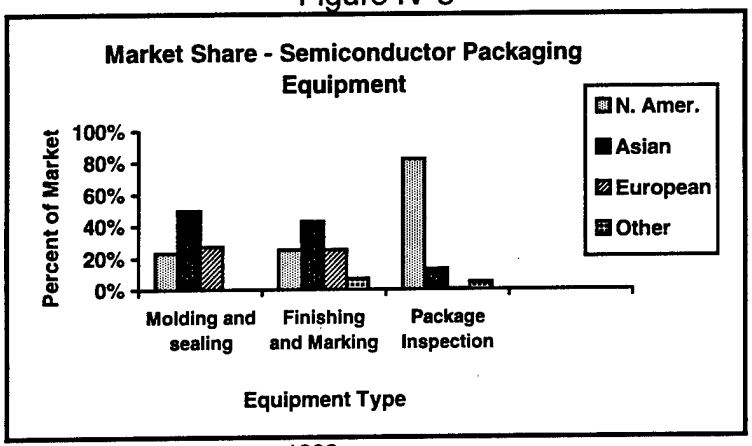
The market share distribution for each of these submarkets by region is shown in Figure IV-5.

Table IV-1

| Leading Packaging Companies Worldwide | | | | |
|---|---|---|---|---|
| Company | Home Nationality | Offerings of Leading Technologies | | |
| | | Ball Grid Array | Fine Pitch Wire Bond | MCMs |
| Accurel | U.S. | | | X |
| Amkor/Anam | Korea | X | | X |
| ASAT | Hong Kong | X | X | X |
| ASE | Taiwan | | | |
| Dyn-Sem | Philippines | | | |
| EM2/Hanna | Thailand | | | X |
| Hestia | U.S. | X | X | X |
| Hyundai | Korea | | X | |
| IBM | U.S. | X | X | X |
| Kyocera | Japan | X | | X |
| Matsushita | Japan | | | X |
| MicroModule Systems | U.S. | X | | X |
| Mitsui High-tec | Japan | | X | X |
| NTK | Japan | X | X | X |
| Pacific Semiconductors | Philippines | X | | X |
| Shinko | Japan | X | X | X |
| Siliconware Precision Industries | Taiwan | | | X |
| S-MOS Systems/Seiko Epson | Japan | | | X |
| Sumitomo Metals | Japan | | | |
| Swire | Hong Kong | | | X |
| Texas Instruments | U.S. | | | X |

Source: Electronic Trends, 1994

Figure IV-5




Source: VLSI Research Inc. 1992

As Table IV-2 shows, in every equipment category, the leading seller accounts for less than a third of total sales. The top four sellers in each of these areas combine for about 60% to about 75% of the market. There are several smaller competitors in each category. U.S. vendors account for a third or less of the sales in every category, except inspection equipment, an area dominated by U.S. firms.

Table IV-2

**Market Structure of Packaging Equipment Suppliers**

| Equipment Type | Market Share (Percent of sales) | | Market share of N. American Companies (percent of sales) |
|---|---|---|---|
| | Top Vendor | Top four vendors | |
| Molding Equipment | 20 | 60 | 31 |
| Presses | 29 | 76 | 15 |
| Die and Molds | 21 | 69 | 15 |
| Finishing | 26 | 58 | 25 |
| Inspection | 22 | 62 | 82 |

Source: VLSI Research Inc. *1992 Survey of the Packaging Equipment Industry*

The top ten semiconductor packaging equipment companies in 1993 are listed in Table IV-3.

Table IV-3

**Top 10 Semiconductor Packaging Equipment Companies - 1993**

| Company | Country | Key Products |
|---|---|---|
| Apic Yamada | Japan | Auto Molds/Trim & Form |
| ASM Pacific Technology | Europe | Die/Wire Bonders; Molding/Trim and Form |
| Disco Corp. | Japan | Dicing/Mounting/Backgrinding |
| Fico | Netherlands | Molding/Trim and Form |
| Kaijo Corp. | Japan | Wire/TAB/Die Bonders; Saws |
| Kulicke & Soffa (K&S) | U.S. | Wire/TAB/Die Bonders; Saws |
| NEC Electronics | Japan | Molding/Trim & Form, Marking |
| NEC Nichiden Machinery | Japan | Die Bonders & Custom Equipment |
| Shinkawa | Japan | Wire/TAB/Die Bonders |
| Towa Corp. | Japan | Auto Molds/Trim and Form |

Source: Semiconductor Technology Center

Semiconductor Packaging Materials - The supply of packaging materials is heavily concentrated in a few firms and geographically dominated by Japanese producers. The industry structure for semiconductor packaging differs substantially according to the type of packaging technology. For plastic IC chip packaging, the actual formation of the packaged IC is usually done by the semiconductor manufacturer, or by a contract assembler, as part of an IC assembly and test operation in which IC wafers are diced into individual chips, tested at the chip level, assembled into molded packages, then inspected and tested as a packaged IC. The main elements of a plastic package are a metal leadframe, which is stamped or etched by the supplier into a particular pattern for each IC type, bonding wire used to attach the die to the leadframe, and an epoxy resin molding compound.

For the ceramic packaged ICs, the semiconductor manufacturer or assembler usually procures packages as components from a firm specializing in making these components, and then uses these components in the final assembly process. Thus, for ceramic packages, the supply base consists of vendors of components, and for plastic packages, the supply base consists predominantly of vendors who supply materials and equipment for forming the package.

The top ten semiconductor packaging materials companies in 1993 are listed in Table IV-4. The merchant markets for leadframes, plastic molding compounds, and bonding wire are dominated by Japanese suppliers. No U.S. companies were included.

The top molding compound suppliers are Sumitomo Bakelite, and Nitto Denko, Japanese firms with production facilities in Japan and other parts of Southeast Asia.[8] Two Japanese firms, Nippon Kayaku and Sumitomo Chemical, supply 80 percent of the epoxy resin used in the molding compounds for forming plastic IC packages.[9] The top five suppliers of leadframes used in plastic packages are Japanese companies that manufacture all of their product in Asia. Individual sales (estimated 1994) for these companies range from $400 million for Shinko Electric to $210 million for Sumitomo/Possehl. In total, Japanese firms comprise 85 percent of the world's leadframe supply. The U.S.-based suppliers' market share for leadframes today is about 15 percent, up from 11 percent in 1989. For bonding materials, Japanese firms comprise 85% of the world's supply (1992), up from 66% in 1989. During the same interval, sales of U.S.-based products fell from 32% to 15%.

Japanese firms also dominate the production of ceramic packages. In 1992, Kyocera, NTK, Shinko and Sumitomo together supplied approximately 92% of the world-wide merchant market, with Kyocera alone providing over 58%. Ceramic packages for high performance microprocessors, ASICs, and other information-intensive applications, including U.S. military systems, are generally made by Japan's Kyocera Corp., which commands 70% of the world market. Suppliers of

[8] *Status 1993: A Report on the Integrated Circuit Industry*, Integrated Circuit Engineering Corporation, 1993, p. 1-18.
[9] SEMATECH, based on Rose Associate data, 1993.

ceramic packages in the U.S. include Alcoa, Coors, and Diacon. Kyocera also has production facilities in the U.S.

Table IV-4
**Top 10 Semiconductor Packaging Materials Companies 1993**

| Company | Country | Key Products |
|---|---|---|
| Dai Nippon Printing | Japan | Leadframes |
| Kyocera Corp. | Japan | Packages and Substrates |
| Mitsui High-Tec | Japan | Leadframes |
| Nitto Denko | Japan | Molding/Encapsulation, Wafer Mounting Tape |
| NTK Technical Ceramics | Japan | Packages and Substrates |
| Shinko Electric | Japan | Leadframes and Packages |
| Sumitomo Bakelite | Japan | Molding and Encapsulation |
| Sumitomo Metal Mining | Japan | Leadframes, Wire & TAB Tape |
| Tanaka Denshi Kogyo | Japan | Wire, Ribbons and Preforms |
| Toppan Printing | Japan | Leadframes |

Source Semiconductor Technology Center

In addition, a number of integrated Japanese electronics firms produce ceramic packages, mostly for their own consumption. These include NEC, Hitachi, Matsushita, Oki, and Toshiba. By contrast, only IBM in the U.S. has in-house ceramic package production capabilities, and now offers some of their ceramic packages for sale on the open market.

Actual and forecasted worldwide semiconductor packaging materials and equipment volume and value are shown in Tables IV-5 and IV-6. These data indicate growth in all areas except for ceramic direct-in-line packages (CERDIP) and headers.

## C. Current State of the U.S. Packaging Industry

*The U.S. is far behind in the low-cost plastic packaging market, but maintains leadership in high performance packaging.*

The relocation of many semiconductor packaging and assembly operations to low labor-cost regions, particularly in Asia, and the rapid increase in Japan's consumer semiconductor market have contributed to the loss of market share by U.S. packaging equipment and materials suppliers. Between 1984 and 1992, U.S. assembly and packaging equipment market share fell from 39% to 31%.

However, there is reason to believe that this situation may change. IC assembly is no longer as labor intensive, because some of the most popular IC packages today are high lead count, surface mount types that are only assembled using automated equipment. By focusing on these package types and fully automated assembly, at least one U.S. company, Integrated Packaging Assembly Corp. (IPAC), started in 1994, expects to turn a profit in the first quarter of 1995 and more than quadruple its 1994 sales. In addition to assembly cost, IC manufacturers benefit from shorter inventory turn times and improved delivery by avoiding the transport back and forth between Asia.

The relatively low priority placed on packaging in the U.S., in part, reflects the markets, U.S. semiconductor companies have targeted. The majority of ICs produced by U.S. semiconductor companies go into the computer, telecommunications, and automotive markets. In those sectors, form factor has not been a primary product differentiator, and for most products packaging was not a major limiting factor in performance. On the other hand, Japanese semiconductor companies are much more closely tied to the consumer electronics marketplace where cost, size, and weight are the primary drivers. As a result, these producers lead in compact low-cost packaging.

Table IV-5

**Worldwide Packaging Materials Forecast**
(millions of dollars)

| | Actual | Forecast | | |
|---|---|---|---|---|
| | 1994 | 1995 | 1996 | 1997 |
| Leadframes | 2660 | 2900 | 3172 | 3520 |
| Ceramic packages metallized | 1150 | 1325 | 1350 | 1400 |
| Encapsulation resins | 748 | 792 | 877 | 973 |
| Bonding wire | 417 | 455 | 496 | 536 |
| Seal lids with preforms | 120 | 130 | 125 | 125 |
| Die attach materials | 115 | 120 | 126 | 132 |
| CERDIP | 105 | 101 | 94 | 88 |
| Header and cans | 90 | 88 | 86 | 84 |
| Hybrid materials | 330 | 340 | 350 | 360 |
| Other | 210 | 220 | 230 | 240 |
| Total | 5945 | 6471 | 6906 | 7458 |
| Percent growth | 21 | 8.8 | 6.7 | 8.0 |

Source: Rose Associates

At the very high end, where packaging limits performance, the U.S. has maintained technology leadership, though the majority of production is within captive suppliers, mainly IBM.[10] This captive production is important since it supports substantial

[10] IBM is a large producer of complex ceramic packaged modules and has shifted from a captive producer to selling into the merchant market.

technical and industrial capabilities. However, by taking advantage of its assembly, equipment, and materials infrastructure, Japanese companies are well positioned to compete successfully with the U.S. firms in high performance packaging.

Table IV-6

**Worldwide Packaging Materials Forecast**
(units)

| | Actual | Forecast | | |
|---|---|---|---|---|
| | 1994 | 1995 | 1996 | 1997 |
| Leadframes (M) | 90,000 | 92,000 | 94,000 | 96,000 |
| Ceramic packages metallized (M) | 78 | 92 | 97 | 102 |
| Encapsulation resins (M pounds) | 189 | 200 | 211 | 222 |
| CERDIP (M bases and lids) | 500 | 460 | 415 | 375 |
| Bonding wire (M feet) | 7800 | 8500 | 9300 | 10,100 |
| Headers | 800 | 780 | 760 | 740 |
| Die attach materials (K pounds) | 165 | 175 | 183 | 190 |

Source: Rose Associates

Changes in end-product markets mean new requirements for semiconductor packages. The evolution of the computer and telecommunications industries toward portable, hand-held products means that size and weight will become increasingly important. Increases in semiconductor device performance mean that packaging will likely become a performance limiter for common desktop computers. The combination of these trends means that electronic packaging will increasingly become a product differentiator for mainstream devices produced by U.S. semiconductor companies.

## D. Multi-Chip Modules

Multi-chip modules (MCMs) are a key enabler for electronic systems requiring high speed and high density. MCMs allow individual ICs to be placed very close together in a single package, either plastic or ceramic. They can employ wire bonding techniques, TAB, and direct attach flip chip techniques. MCMs can be surface mounted to circuit boards (e.g., BGA) or can use PGA techniques. As such, they use much of the assembly technology as for single-chip ICs. However, a single substrate with multiple die presents far more complexity in die attach adhesives and placement, wirebonding pattern recognition, and bonding replacement. Materials issues in MCMs are at least as complex.

The current and future MCM markets include personal computers, workstations, high definition television (HDTV), mainframe and supercomputers, telecommunications, automotive, and military systems. End-of-decade market size estimates vary by an order of magnitude from $800 million to $8 billion. Table IV-7 shows figures on MCM

demand, merchant and captive combined, by types of application. To date, MCMs have been used extensively in the military/aerospace and high-end computer markets. The mainstream commercial IC industry is now beginning to explore the use of MCMs as well.

Since the growth of the MCM market will depend on their affordability in those applications having the greatest potential for mass production, MCM vendors are striving for greater production efficiency in high-volume manufacturing. However, the ability to attract the financing required to develop and employ volume production techniques requires demonstrated confidence in the emergence of these markets. As an emerging technology competing against existing and developing alternatives, MCM producers face financial and management challenges, as much as, technical issues.

Table IV-7

**World MCM Application Revenue ($M) Forecasts**

**(Captive & Merchant)**

| Applications | 1992 | 1994 | 1996 | CAGR(%) |
|---|---|---|---|---|
| Computer | 196 | 258 | 445 | 22.8% |
| Military | 64 | 85 | 132 | 19.6% |
| Telecomm | 22 | 40 | 100 | 45.4% |
| Other | 18 | 29 | 73 | 43.1% |

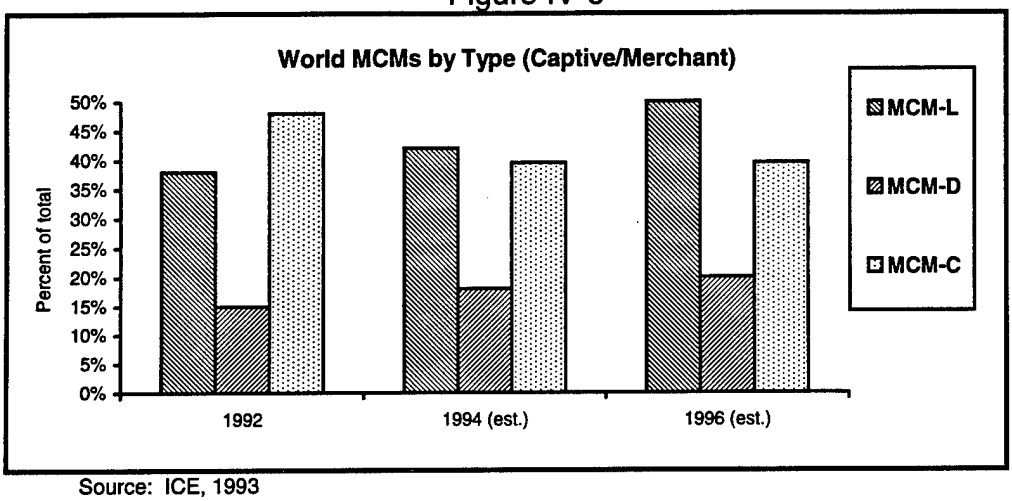
Source: ICE

The three main substrate interconnect technologies, MCM-L, MCM-C, and MCM-D, have contrasting growth projections. Laminate-based MCMs (MCM-L) accounted for 37% of MCMs sold in 1992. By 1996, MCMs-L are projected to comprise 50% of the MCM market. MCM-C, now 50% of the total MCM market is projected to decline to under 30% by 1996. MCM-D sales, now 15% of the market, are projected to reach 20% by 1996, as their pricing becomes more competitive (Figure IV-6). However, to achieve the projected growth, MCM-D will require significant reduction in cost and manufacturing complexity while the reliability of MCM-L must be improved. At present, the MCM-C market is growing at nearly 20% per year.

MCM production today is about evenly divided between U.S. and Japanese producers, with Europe's current market share of about 5% expected to grow to about 11% by 1996. This roughly equal division of the market between U.S. and Japanese firms is expected to persist over the next several years. The major change now anticipated is from captive MCM production to merchant vendors

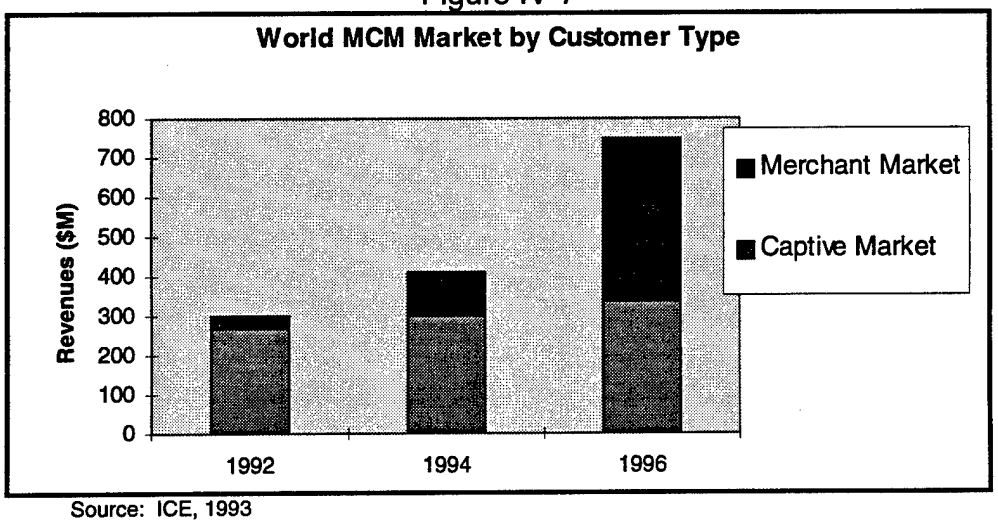
(Figure IV-7). Technological change may create an opportunity for new players to enter the merchant packaging market, and current captive producers are increasingly looking to the merchant market as a source of revenues. Table IV-8 is a compilation of companies that produce MCMs.

Figure IV-6




Source: ICE, 1993

Figure IV-7




Source: ICE, 1993

Table IV-8

| MCM Manufacturers | | | |
|---|---|---|---|
| **Vendor** | **Location** | **Vendor** | **Location** |
| ACX Technologies | United States | IST | United States |
| ArcSys Inc. | United States | Kyocera | Japan |
| AT&T | United States | LSI Logic | United States |
| Boeing | United States | MCC | United States |
| British Telecom | Europe | MCNC | United States |
| Bull | Europe | MicroModule Systems | United States |
| Carborundum/BP | United States | Motorola | United States |
| Chip Supply | United States | nCHIP | United States |
| CNET | Europe | NEC | Japan |
| Cray | United States | NTK | Japan |
| Crosscheck | United States | NTT | Japan |
| Dassault Electronique | Europe | Quadrant | United States |
| DEC/MicroModule Systems | United States | Rockwell | United States |
| Dow Chemical/Polycom | United States | Shinko Electric Industries | Japan |
| Fujitsu | Japan | Siemens | Europe |
| General Electric | United States | Silicon Connections | United States |
| GEC-MRC | Europe | SMI | Japan |
| Harris | United States | S-MOS Systems (Seiko Epson) | Japan |
| Hestia Technologies, Inc. | United States | Sumitomo Metal & Mining | Japan |
| Hewlett-Packard | United States | Tektronix | United States |
| Honeywell | Japan | Texas Instruments | United States |
| Hughes | United States | Thorn-EMI | Europe |
| Ibiden | Japan | Toshiba | Japan |
| IBM | United States | Unisys | United States |
| IMI | United States | VLSI Technology | United States |
| Integrated System Assemblies | United States | W.R. Grace | United States |
| Intergraph | United States | Z-Systems | United States |
| Irvine Sensors | United States | | |

Source: Dataquest Inc. and Electronic Trend Publications

## E. Evaluation of U.S. and Japanese Electronic Packaging Technology

Results from a recent government sponsored evaluation of electronic packaging technology and manufacturing in Japan found the Japanese ahead in 11 of 15 manufacturing areas, parity in one (wire bond), and a U.S. lead in three (MCM-D, flip-chip assembly, and design) (Table IV-9).

Table IV-9

**Packaging Technology Assessment - U.S. vs. Japan**

| | Technology | Volume Mfg. |
|---|---|---|
| Single Chip Modules | | |
| Plastic | Japan | Japan |
| Ceramic | U.S. | Japan |
| Multi-Chip Modules | | |
| Thin Film (MCM-D) | U.S. | U.S. |
| Ceramic (MCM-C) | U.S. (High performance) | Japan (Low cost) |
| Laminate (MCM-L) | Japan | Japan |
| Chip-on-board (COB), Chip-on-glass (COG) | Japan | Japan |
| Chip Assembly | | |
| Flip-chip | U.S. | U.S. |
| TAB | Japan | Japan |
| Wire bond | Parity | Parity |
| Package assembly (Process, tools, density) | Japan | Japan |
| Passives, Components | Japan | Japan |
| Printed wiring board | Japan | Japan |
| Flex circuits | Japan | Japan |
| Connectors | Japan | Japan |
| Design | U.S. | U.S. |

Source: Japanese Technology Evaluation Center (JTEC), 1993

# Chapter V
# U.S. Government Semiconductor Packaging Programs

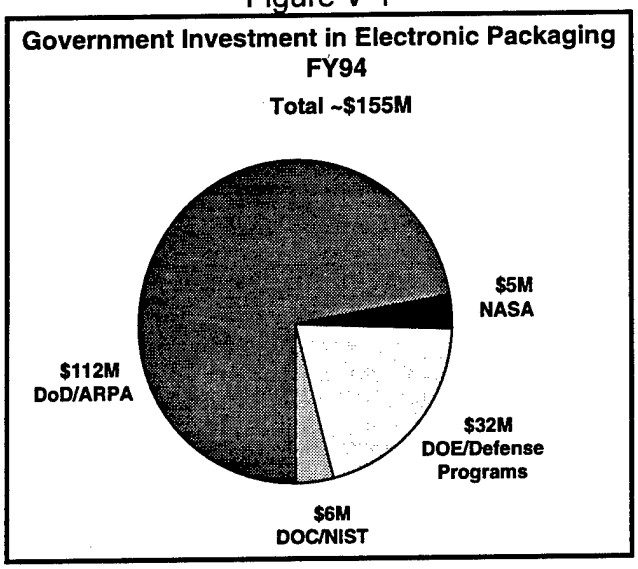
Because of the importance of semiconductor packaging technologies for military and commercial systems, Secretary of Defense Perry and Secretary of Commerce Brown announced in March 1994, an action plan for electronic packaging technology. This plan builds upon ongoing federal programs, the DoD's efforts to foster dual-use technologies that strengthen U.S. national security by strengthening critical elements of the national industrial base, and previous Department of Commerce recommendations regarding the ceramic packaging industry. The elements of the action plan for packaging are summarized below:

- An Interagency Specialists' Group is to be established and chaired by the Advanced Research Projects Agency (ARPA), to work with industry to develop set of national R&D priorities and a technical roadmap that will lead to U.S. leadership in electronic packaging. The group held its first meeting on November 1994, to develop a national packaging roadmap and strategy that is consistent with national security requirements.
- The DoD is working with the semiconductor industry to expand the SEMATECH consortium's electronic packaging programs to address a broader range of nearer-term packaging priorities.
- The DoD is expanding the supplier qualification program, established by SEMATECH, to address all areas of electronic packaging critical to the DoD and the semiconductor industry.
- Through the Technology Reinvestment Project (TRP), the DoD is funding a new $30-40 million Defense-led program, focusing on developing low cost, high performance electronic packaging technology that meets long-term military needs by supporting industrial R&D in key areas. Because the program is cost-shared with industry, this should stimulate at least $60 to $80 million in new technology investments.
- The DoD, DoC, and DoE are supporting ongoing federal R&D programs that maintain U.S. leadership in high performance packaging technologies, and in critical support infrastructure such as design and reliability testing. Support for basic materials and process R&D, which are essential for long-term technology leadership, are also being continued.
- The DoD will continue to work with industry to eliminate any artificial barriers between the defense and commercial markets. This will assure that U.S. vendors have maximum access to the defense markets and R&D, and will allow the DoD and other government customers to take advantage of the economies of scale and increased efficiency provided by commercial markets.

In FY94, the U.S. government spent over $150 million in packaging-related R&D. Approximately, three quarters goes directly to the U.S. industry through contracts, grants and other agreements. The remainder is spent in government laboratories on

programs that usually involve industry collaboration. Approximately 85% of these funds go towards projects that are dual use in nature, and directly aid the capabilities of the domestic infrastructure. Many of the projects involve cooperative activities and are cost-shared with industry. Figure V-1 shows the breakdown of the FY94 funds by agency.

Figure V-1




These programs target packaging approaches that include single-chip modules, MCMs, and printed circuit boards, as well as, a range of support technologies such as design tools, assembly equipment, testing, reliability, metrology, and advanced materials. The support technologies, which are generally independent of packaging approach and materials approach, make up over 40% of the federal investment. Projects range from basic research through application demonstrations in military and commercial systems.

Of the 60% of federal R&D that is invested in specific packaging approaches, roughly two thirds is directed towards performance-driven applications. Examples include critical military functions, such as automatic target recognition, command and control and precision strike, as well as, important dual-use applications including high performance computing, high speed networking, and automatic test equipment. Technologies under development include thin-film MCMs, optical interconnects, 3-D packaging schemes, microwave packaging, and new materials and systems for thermal management. Also, under development are new packaging technologies aimed at compact, lightweight, low cost solutions for military applications, such as personal navigation, wireless communications, and hand-held computing. These technologies include low cost laminates, mixed signal packaging, and adhesive flip-chip. The objective in the majority of these programs is to develop healthy domestic suppliers who can satisfy defense needs along with high commercial leverage.

## A. DoD/ARPA

ARPA's semiconductor packaging strategy is:

1. Support establishment of a strong domestic (dual use) merchant infrastructure to assure that U.S. national security needs are met.
2. Exploit packaging technology discontinuity (movement from single chip to multi chip).
3. Focus on leveraging end-product markets where the U.S. has a strong presence (computers, telecommunications, automotive, and aerospace).
4. Re-establish U.S. leadership in defense critical, high value-added packaging technologies.

The ARPA program is made up of two major elements: a core packaging program and the Technology Reinvestment Project (TRP) focus area. Government TRP funding is matched by industry. The TRP packaging focus has its largest investment in the industry-led muti-chip module consortia.

ARPA core packaging program investments include:

- Area I/O, Flip Chip Infrastructure
- Test Cost Reduction
- System Design With First Pass Success
- Concurrent Chip/Package/System Design Optimization
- MCM/COB Substrate Technology
- New Packaging/System Paradigms
- Next Generation Materials Systems
- Cost-effective Mixed Signal Modules

A significant addition to ARPA's base program is contained in the Technology Reinvestment Project (TRP). The mission of the TRP is to increase the DoD's access to affordable, leading edge technology by leveraging commercial know-how, investments, and markets for military use.[1] TRP projects are selected and designed: (1) to obtain access to emerging commercial technology by using the commercial world's drive and ability to quickly develop and apply it; and (2) to assure defense access to existing technologies at the lowest possible cost. Each TRP projects is selected on its technical merit, defense relevance, and strength of the proposing industry team.

The TRP packaging projects, objectives, and funding levels are listed in Table V-1. In all cases, industry funding is (by statute) at least equal to government funding. The project objectives all target low cost, leading edge semiconductor packaging where the aim is to move the commercial, dual use market forward.

[1] Actions in the Congress which reduce TRP funding may severely weaken DoD's strategy to help build an industry base in high performance semiconductor packaging. As discussed in Chapter 3, DoD access to advanced commercial packaging technology is critical to meet DoD's future warfighting requirements. It is very likely that defense will lose assured access to important capabilities unless U.S. industry invests in achieving a strong market position in high performance semiconductor packaging. The goal of the TRP is to strengthen defense access to these critical capabilities.

Table V-1

## Technology Reinvestment Project: Low Cost Electronic Packaging

| Title | Goal | Total Project Cost ($M) |
|---|---|---|
| **1993 Awards** | | |
| Technology to Produce High-Performance, Low-Cost Interconnections for Flip-Chip Attachment | ...produce an order-of-magnitude improvement in manufacturing labor hours over current solder-based systems. | $5.7<br>(36 mos.) |
| The MCM Consortium -<br><br>The Path to a Globally Competitive MCM Industry in the U.S. | ...lower manufacturing costs while improving performance and reducing size of MCMs.<br><br>... reduce cost of MCMs to the point where DoD needs are addressed through the U.S. commercial supply base. | $40<br>(24 mos.) |
| **1994 Awards in Low Cost Electronic Packaging Focus Area** | | |
| Low Cost Packaging Technology for Automotive Electronics | ...to develop compact, reliable, low-cost packaging to meet the harsh environmental requirements of military/aerospace and of under-the-hood automotive applications<br><br>... applying applicable commercially driven technology dramatically reduce cost relative to current DoD packaging approaches. | $12.6<br>(24 mos.) |
| Low Cost Flip Chip | ...develop solder bumping capability, test and handling processes and hardware, substrates optimized for flip-chip interconnect, surface mount compatible board assembly processes, and industry standard design rules for area array and peripheral bumped chips.<br><br>... application demonstrations are chips for portable wireless military communications, missile guidance electronics, and a modem for satellite communications. | $20.5<br>(24 mos.) |
| Competitive Low Cost Packaging for Wireless Communications in a Global Grid | ...develop new ceramic packaging {that will} reduce costs for many RF electronic applications by reducing component count and assembly costs.<br><br>... project includes a number of application demonstrations of direct interest to DoD | $8.0<br>(24 mos.) |
| Lost Cost Packaging Based on Area Bonding Adhesives with X, Y, and Z Axis Conductivity | ...develop and qualify several new low-cost packaging approaches utilizing conductive epoxy adhesives that offer lower cost, solder-free joining. | $1.6<br>(24 mos.) |
| Pad Printer | ...develop a dramatically improved printing technology [that] will allow thick-film hybrids and ceramic multi-chip modules to be manufactured with reduced size and cost.<br><br>... these MCMs are particularly important for a range of military platforms, weapons, and other systems subjected to harsh environments | $2.2<br>(24 mos.) |
| Low Cost Plastic Packaging | ...revolutionize plastic packaging technology and create a domestic infrastructure [allowing] an ever increasing number of high-performance military and commercial ICs [to] shift to plastic for a substantial cost reduction | $20<br>(24 mos.) |
| Technology and Production Acceleration of Low Cost, Aluminum Nitride Electronic Packaging | ...enable the production of low-cost ceramic packages which support the very large, high power, high pin-count, area-array chips forecasted by the semiconductor industry for leading-edge microprocessor and application-specific integrated circuits.<br><br>... product evaluation provided by military end-user team | $9.8<br>(24 mos.) |
| Low Cost Electronic Packaging Through Systems Approach to Ball Grid Array Package Assembly | ...develop a lower cost and more environmentally friendly approach to assembling ball grid array packages [which] are expected to become predominant in high pin count devices used in both military and commercial applications | $.0.42<br>(10 mos.) |
| Low Cost, High Density, Sequential Build PWB Manufacturing Technology | ... develop and demonstrate a high volume manufacturing process for high-density printed wiring boards capable of a 50% cost reduction relative to current t processes. | $6.9<br>(24 mos.) |

Sources: Advanced Research Projects Agency, TRP Project Summary; TRP Focus Competition on Low Cost Electronic Packaging

ARPA is also working with SEMATECH and the Semiconductor Equipment and Materials Industry (SEMI) to establish a Standardized Supplier Qualification Assessment (SSQA) and a Technology Assessment Protocol (TAP) for ceramic package suppliers. The adoption of these methodologies by the SEMATECH membership will greatly reduce the effort required by companies who wish to become qualified to supply multiple U.S. semiconductor companies with packaging materials. One supplier audit has already been completed and a second is being initiated.

## B. Department of Energy (DoE)

The majority of DoE's packaging investments are in Defense Programs (DP) and support DP's mission to assure the viability, safety, and security of the nations nuclear weapon's stockpile. High performance, compact, highly reliable electronics are a critical element of modern nuclear weapons. Semiconductor electronics play a vital role in weapon timing and firing, safety, delivery, targeting, as well as, the monitoring of weapon performance and long-term degradation.

To achieve its objectives, DP has developed a broad-based competency in electronics packaging with the associated infrastructure in facilities and technologies. Its capabilities cover the spectrum from fundamental research to prototyping and evaluation. DP's annual investment in activities related to electronic packaging is approximately $32M and is enabled by laboratory facilities worth over $100M.

Driving the DoE packaging infrastructure and competency are special shapes, weight and volume constraints, elevated operating temperature, severe mechanical vibration and shock, and long-life (approximately 30 years) with ultra-reliability. As with most DoD mission critical electronic systems, packaging is the enabling technology for the operation of all electronic components.

Although all of the DP laboratories are engaged in packaging R&D, Sandia National Laboratory, due to its design and production oversight responsibility in nuclear weapon electronics, has the majority. However, important programs at Oak Ridge (e.g., packaging materials) and at Lawrence Livermore National Laboratory (e.g., 3-D interconnects) take advantage of the unique expertise available at those laboratories.

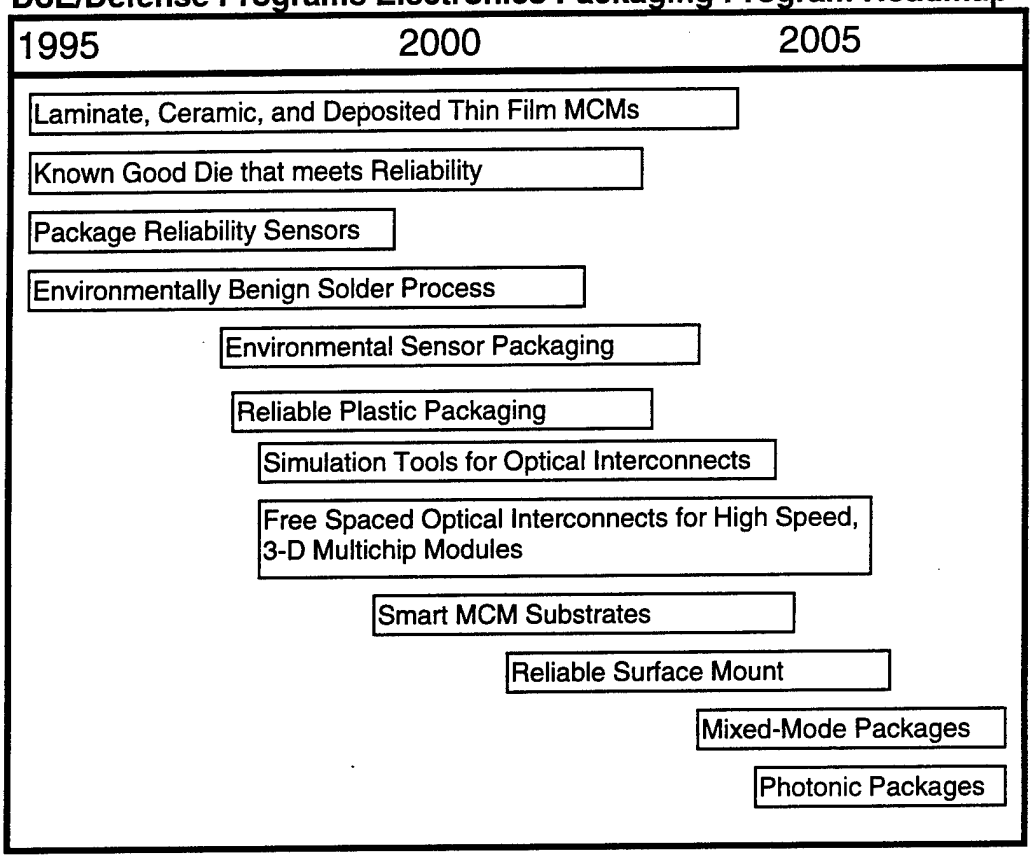
Defense Programs packaging program includes the following technology areas, representing efforts in research, development, and weapons deployment:

- Package prototyping: single chip, multi-chip, hybrid microcircuits, printed circuit boards, and photonics
- Computer modeling: thermal, mechanical, and electromechanical
- Design tools: test, auto-layout, design rule checker
- Failure analysis and reliability
- Multi-chip modules: deposited thin-film, ceramic, and laminate
- Materials analysis and synthesis
- Assembly R&D
- Qualification

- Test chips and smart substrates
- Three-dimensional packaging
- Mixed-mode packaging
- Known Good Die (KGD)
- Optoelectronic packaging and interconnects
- Flat panel display packaging

Figure V-2, the Defense Programs Packaging Roadmap, emphasizes reliability, modeling, and movement toward surface mount technology in the nuclear weapons program.

Figure V-2
**DoE/Defense Programs Electronics Packaging Program Roadmap**




In addition to direct mission-related work, Defense Programs conducts packaging-related R&D in partnership with other federal agencies under work-for-others agreements. These include developing packaging test methodologies and materials for the DoD Reliability without Hermeticity(RwoH) program, advanced packaging for a miniaturized DoD synthetic aperture radar and multi-processor computer (SANDAC), high reliability packaging assembly monitoring, and secure multichip module design and manufacture for several Federal customers.

The DP Laboratories actively engage in cost-shared partnerships with industry. Similar to DoD's dual-use strategy, these interactions help assure that Defense Programs nuclear weapon's laboratories have ready access to industry leading-edge

technology and talent, and that industry will be able to help meet future DP semiconductor packaging requirements.

## C. Department of Commerce/NIST

A third major government-sponsored effort in electronic packaging is in DoC's National Institute of Science and Technology (NIST). NIST's program in electronic packaging is embedded in Laboratory Programs and the Advanced Technology Program (ATP) for a total of about $30M. The ATP portion ($24M) is matched with over $26M in private funding.

The Laboratory Program includes characterization, metrology, and processing related to curing rates of plastics, metal films, moisture, adhesion properties, solderability, and gases.

Important, up-coming project areas include moisture effects in electronic packaging resins, mechanics of thin layers, integrated design, manufacturing, and reliability tools for solder interconnects, and thermomechanical reliability of interfaces.

Advanced Technology Program (ATP). NIST's ATP program supports cost-shared (with industry), pre-competitive R&D projects in four areas related to semiconductor packaging:

- Printed wiring board interconnects.
- Flip-chip monolithic microwave IC (MMIC) manufacturing.
- Solder jet technologies.
- Conducting polymers.
- Interconnects for ultra-low dielectric constant, high performance materials.

## D. NASA

Semiconductor packaging in NASA is focused on:

- System engineering.
- Advanced surface mount technologies.
- Multi chip modules.
- Three dimensional packaging structures.
- Monolithic microwave integrated circuits (MMIC).
- Low cost packaging and chip-on-board (COB).
- Electro-optical packaging.
- System demonstrations.

Reliability is crucial for NASA and, consequently, adoption of physics of failure techniques, reliability modeling, and establishment of appropriate test requirements for space environments are high priority elements in NASA packaging programs. As for the DoD, NASA's packaging roadmap emphasizes the insertion of direct-chip-attach, ball grid array, and MCM-D and 3-D packaging structures within the next five years.

## E. Conclusions

Although DoD has the bulk of government semiconductor packaging programs, the DoE, NIST, and NASA programs add important elements. DoE's packaging program for nuclear weapons stresses reliability analysis, known-good-die, advanced MCM substrates and interconnect, and computer simulation tools. In addition, it is supported by extensive, modern laboratory capabilities. NIST's Laboratory Programs stress complex metrology related to semiconductor packaging and can provide important understanding of failure modes in plastic and other packaging configurations. NASA's knowledge base and models of physics-of-failure can benefit proposed DoD changes in reliability assessment methods. Each of these government programs supports important developments which help further the DoD's dual-use strategy in high performance semiconductor packaging.

The Interagency Packaging Specialists Group provides a mechanism to coordinate and maximize the contributions of the government agencies. Beyond developing a set of national R&D electronic packaging priorities and technical roadmap, the group could serve as focal point for information exchange, and development and coordination of interagency projects that lead toward establishing a dual-use semiconductor packaging U.S. industry infrastructure and reliability standards.

# Chapter VI
# Maintaining Assured Access To Semiconductor Packaging Capabilities That Meet Military Needs

*Progress in commercial semiconductor packaging supports most current and near-term military requirements. However, emerging DoD requirements for high-speed processors, application specific ICs, and high-density, low-power and portable electronics require additional technical and industrial manufacturing capabilities.*

*Currently well over 90% of commercial packages are encapsulated in plastic and the movement toward plastic is increasing as new materials with improved properties are developed. The DoD is increasingly moving toward plastic packages and this should continue where it is clear that needed system reliability and performance are not compromised. Work should be accelerated and coordinated to assure that the performance of plastic encapsulants in military systems is thoroughly understood and characterized. Modeling of the physics of failure should increasingly be used to redirect the selection of packaging materials and if possible, predict long-term material and IC failure.*

*There is currently no reason to believe that the DoD will lose access to leading edge, packaging assembly, equipment, or materials suppliers. However, over the longer-term, it is not clear that the existing efforts and base of packaging and assembly companies will be willing or able to meet new military requirements for high performance MCMs and other high density packaging. This issue is clearly recognized, and is being addressed by ARPA's Packaging Program which will enable DoD to use commercial capabilities that meet DoD requirements.*

## A. Technology Drivers

Increasingly, the commercial semiconductor packaging industry is being driven by demands for higher pin (I/O) count and density and higher performance. Package configurations are moving toward small-outline, single-chip surface mount technologies of all types; [1] multi-chip modules; and direct chip attach (chip on board). Depending on the application, most of these package configurations can be either plastic encapsulated or in hermetically-sealed ceramic. Packaging is now a limiting factor in IC performance and many semiconductor manufacturers view packaging as a source of strategic differentiation. Packaging directly determines the maximum clock rates for microprocessors, the size and weight of portable electronics, and heat dissipation.

[1] BGA, PGA, QFP, Chip carrier.

In most areas, progress in commercial semiconductor packaging technology supports current and near-term military requirements. Increasingly industry is using high pin-count ball grid arrays, TAB, quad flat pack, and a variety of other small outline surface mount packages in military equipment.

However, emerging military demands require increased emphasis on high chip density, highly reliable semiconductor packaging that enables microprocessors and ASICS to operate from 100 megahertz to several gigahertz. MCM technology leads the way to achieving this level of performance. MCMs that achieve this performance are not now readily available or affordable from industry and it is not likely that industry alone will be achieve this combination of performance and low cost. The primary impediments to this are manufacturing practice and experience with demanding products for which current demand is low and the development of infrastructure capabilities that are beyond the direct interest of individual MCM firms. Therefore a primary goal for the DoD is to achieve the required performance at lower cost. To do so, continued DoD R&D matched with industry support will be needed to accelerate development of the technologies, materials, and manufacturing techniques that assure availability of needed industrial capability.

Enabling technologies for this class of MCMs include higher heat dissipation substrates, flip-chip mounting techniques, known good die, new testing approaches, low dielectric materials for high frequency operation, and computer simulation and design tools.

## B. Plastic and Ceramic Packaging

Well over 90% of commercial packages are plastic and the trend toward plastic is increasing. High performance commercial ICs (microprocessors and ASICs) are generally packaged in ceramic but even for these applications, the use of plastic is increasing. Ceramic packaging capability is strong in the U.S. and world-wide. For directly purchased military ICs, ceramic packages are used almost exclusively (over 90%). Commercial practices, and plastic encapsulated ICs are increasingly finding their way into military systems.

Most military merchant vendors support increased insertion of commercial plastic packages into military systems, for reasons that do not always have to do with reduced cost. It is not clear, under QML, that plastic encapsulated ICs would, in every case, result in significant cost savings, given that additional costs to assure quality control, required reliability, assured supplier responsiveness, traceability, obsolescence control, and supplier selection may be incurred. Beyond cost, however, insertion of plastic packages into military systems allows for a broader product portfolio and more rapid access to leading-edge packaging technologies. Table VI-1 lists and compares the potential advantages and disadvantages of commercial and QML certified plastic and ceramic packages.

The insertion of plastic packaged ICs into military systems has both pros and cons and is highly dependent on the environmental operating conditions. Test data shows that with newer resins and pre-coat techniques, plastic encapsulated ICs, under most conditions, are as reliable as ceramic. However, concerns remain about IC failure after long-storage life and extreme temperature and humidity fluctuations. Failure rates for PEMs vary widely from supplier to supplier. It is apparent that commercial ICs could be readily used in many of DoD's non-critical, non-extreme environmental conditions applications. These include many computer systems, communications systems, command and control, and high speed sensor data processing applications. At the opposite extreme where the ICs must perform at extreme temperature and humidity conditions and cycles, or where assured operation after long-term storage (up to 20 year) is important (missiles and other armaments), military vendors would be reluctant to move away from the proven reliability of ceramic packages.

Table VI-1

**Comparison of Package Options**

| | Commercial Plastic | QML Plastic | QML Ceramic |
|---|---|---|---|
| Initial price | Lowest | Mid range | Highest |
| Temperature range | Typical 0 - 70$^0$ F | -55 TO 125$^0$ F<br>As required | -55 TO 125$^0$ F<br>As required |
| Test Program | Commercial data sheet | SMD[2] | SMD |
| Long term reliability | Good | Good | Best |
| Supplier responsiveness | Dependent on revenue | High | High |
| Storage/Processing | Some additional requirements | Some additional requirements | As current |
| Product portfolio | Best | Weak to good | Good |
| Time to market | Best | Good | Good |
| Obsolescence control | Minimal | Best | Best |
| Traceability | Minimal | Best | Best |
| Other contractor requirements | Not available | As Required | As required |
| Supplier certification | By user | DESC | DESC |
| Supplier selection | Critical | Less important | Less important |

Source: Texas Instruments

In June, 1994, the Industry Task Force on Affordability hosted a symposium on The Successful Use Of Commercial ICs In Military Systems where successful uses of commercial ICs were presented for a broad class of DoD applications, from image

[2] The Standard Military Drawing (SMD) was created in the 1980s to militarize the documentation on non-Qualified Parts List (QPL) grade devices. SMD parts are tested in accordance with MIL-STD-883, and part drawings and data are maintained centrally by DoD, rather than being left with the device manufacturer. Electrical specifications are controlled by DoD drawings, as in the QPL devices, but all of the other extensive certification and qualification associated with QPL is not necessary. Because production line certification is not required, off shore assembly and packaging is permitted. The theory behind SMD is that establishing standardized performance characteristics for ICs can help encourage multiple sources for a given device and reduce risk of designing with a manufacturer's unique specification. The SMD system currently defines over 85% of military-use ICs, according to the SIA.

processing to smart munitions. These systems operated in a broad range of environments including space, ship-board, extremely cold environments in the Arctic, dropped into the ocean, and aircraft installations. In many cases the motivation for using commercial parts was to obtain functionality not readily obtainable through procurement of MIL-SPEC components. This project is scheduled to more fully validate the case study results, do more specific assessments of potential benefits and savings from commercial IC applications, and propose experiments and demonstrations to identify the full extent of commercial IC applications, risk, and savings/benefits.

Current and forecast trends that enhance the confidence and mitigate risk in the area of commercial ICs in military systems include:

- Increasing availability of industrial grade and automotive components with extended temperature range and severe environmental requirements through substantial characterization similar to MIL-STD-883.
- Demand by the portable and hand-held communications marketplace to provide lower power devices with small outline, high pin count plastic packages.

The move from ceramic to plastic should be done with a thorough knowledge of the technical trade-offs, and the other issues listed above. Additional work needs to be done into the use of Highly Accelerated Stress Testing (HAST) for temperature and humidity acceleration and extrapolation to long-term reliability. In addition to HAST, a physics of failure approach should be increasingly used to redirect the selection of packaging material selection and to set targets for the material science research community. As material properties and models for creep and fatigue become better characterized, it may be possible to predict the long-term behavior of plastic packages.

Reliability assessments of military electronics has traditionally been based on empirical failure-rate models developed from curve fits of field-failure data. In the U.S. Army, electronic packaging decisions have been controlled by U.S. Mil-Hdbk-217 for the past 30 years. Mil-Hdbk-217 relies on failure data which are sparse until well after a new technology is mature. This approach discourages innovative and cost effective electronics packaging materials, structures, and technologies. Crucial failure details not addressed by Mil-Hdbk-217 include:

- failure site
- failure mechanism
- electrical load and environment history
- materials
- geometries

This methodology does not give the designer or manufacturer insight into, or control over, the actual causes of failure since cause-and-effect relationships are not captured. "Physics of failure" is an approach for the development of reliable products that uses knowledge of root cause failure processes to prevent product failures through robust design and manufacturing approaches. The physics of failure approach incorporates reliability into the design process by establishing a scientific basis for evaluating new

materials, structures, and packaging technologies. Generic failure models are used by physics of failure that are as effective for new materials as they are for existing designs.

In 1992, the Headquarters of the Army Materiel Command (AMC) authorized the Electronic Equipment Physics of Failure Project to facilitate a transition from MIL-Hdbk-217 to a more scientific, physics of failure approach to electronic packaging. The U.S. Army Materiel Systems Analysis Activity (AMSAA) was directed to lead this effort for the Army, with support from the University of Maryland Electronic Packaging Research Center. Moving from a empirical-based reliability determination (e.g., Mil-Hdbk-217) to a physics of failure approach will help ensure that the DoD is taking advantage of the best packaging technologies and materials, that root-causes of failure mechanisms are understood and remedied, and that the best practices of industry are represented. Continued development and implementation of the physics of failure approach should be encouraged. The DoE national weapons laboratories and NIST are dealing with similar packaging issues and should work in close collaboration with DoD physics of failure programs.

## C. Semiconductor IC Assembly

Worldwide IC packaging and assembly is highly competitive and, with the exception of a few U.S. companies, is concentrated primarily in Japan, Thailand, Korea, Hong Kong, and the Philippines. U.S. military vendors have relied on these foreign assembly plants for years and there are no indications that U.S. access to these facilities would be denied in the future. Whether foreign or U.S. owned, military lines on overseas semiconductor IC packaging and assembly plants are routinely QML certified by DESC.

Driven by lower costs and existing infrastructure, off-shore assembly will continue for many current and future military semiconductor packages. However, for the new class of high performance MCMs discussed earlier, it may be possible to establish a domestic manufacturing capability and supporting infrastructure that can provide faster and more accessible support for DoD semiconductor packaging needs well into the future. Success will depend on programs such as ARPA's MCM packaging effort in reducing the manufacturing cost of high performance MCMs, the development of commercial markets that demand this performance, and U.S. industry initiatives to compete in this market.

## D. Packaging Equipment

Packaging equipment falls into five major categories with a dozen or more competitors from around the globe. The markets are competitive and geographically diversified. U.S.-based vendors dominate the market in one of the categories, inspection equipment, with TI as the leading seller. U.S. sellers account for a third or

less of the markets in every category except for inspection equipment. These markets are highly diversified, both in terms of vendors and their geographical base; access to packaging equipment is unlikely to be denied to any producer.

However as market demand for new packaging technologies increases, new opportunities may exist which can be exploited by U.S. entrants into the semiconductor packaging equipment industry. As in the assembly industry, this would improve the quality of assured DoD access to this part of the packaging infrastructure.

## E. Packaging Materials

Historically and currently, DoD relies on a largely foreign supply of semiconductor packaging materials. The supply of semiconductor packaging materials is far more concentrated, both industrially and geographically. The supply of both ceramic packages and plastic encapsulation resins is highly concentrated in a handful of Japanese firms. Kyocera alone supplies about two-thirds of merchant U.S. ceramic package consumption. Many other suppliers compete with Kyocera, but U.S. and foreign chip manufacturers have preferred to take advantage of the prices, quality and service they have received from Kyocera. In the course of investigating the national security consequences of dependence on imports of ceramic IC packages, the DoC found:

> ...ceramic semiconductor packages are not being imported into the U.S. in quantities and under such circumstances as to threaten or impair U.S. national security. Although current conditions in the ceramic package industry did not present an immediate threat to national security, improving the capabilities of the domestic ceramic package industry is desirable for both economic and national security reasons.[4]

Similar concerns have been expressed over Sumitomo Chemical's dominance of the plastic resin market. As with Kyocera, there are alternative suppliers available, but Sumitomo's high quality product, service, and pricing have given them a dominant market position. In the summer of 1993, a fire destroyed a major Sumitomo production facility in Ebino, Japan. Initial fears of an impending shortage of epoxy encapsulation resins were short lived and by the beginning of 1994, these resins were available on the market in ample supply, with both Sumitomo Chemical and Nippon Kayaku bringing new capacity on-line, and customers learning to increase their efficiency of utilization.

[4] *The Effect Of Imports Of Ceramic Semiconductor Packages On The National Security: An Investigation Conducted Under Section 232 of the Trade Expansion Act of 1962*, PB 93-192441, U.S. Department of Commerce, August 1993.

This incident points out that for high-demand materials:

1. Alternate industry resources can be quickly converted to meet demand
2. Substitute materials and suppliers become available
3. Technical and industrial know-how can be marshaled to circumvent a potentially major shortage
4. The timeframe needed to compensate for the material shortage can be short

Foreign technology and manufacturing leadership in plastic and ceramic single chip packaging technology should continue to meet DoD industrial and technology requirements into the future. In ceramics, existing U.S. and foreign technology and manufacturing capability will satisfy DoD requirements.

It is instructive to contrast the DoD vulnerabilities in semiconductor packaging with flat panel displays. In 1994, the DoD concluded that it must have early, assured, and affordable access to the most advanced display technology, and that it currently lacks such access.[5] In response to that conclusion, the DoD Flat Panel Display Initiative was implemented. Table VI-2 compares the findings of the flat panel display industry dual use assessment with that of the ceramic package industry.

Table VI-2
**DoD Dual Use Access - Ceramic Packaging Compared to Flat Panel Displays**

| Issue | Ceramic SCM Packaging | Flat Panel Displays |
|---|---|---|
| Vendor concentration | Dominated by Japanese and other Far East vendors. One vendor supplying over 70% of high performance semiconductor packages | Dominated by small number of offshore vendors with over 50% of supply from one vendor |
| Willingness to work with the DoD | Yes, even to the extent that the major ceramic supplier established a U.S. facility | No. Major vendor explicitly informed DoD of corporate policy not to deal with DoD. |
| Domestic capabilities in case of emergency | Yes. For ceramic packages, captive producer quickly able to supply U.S. military needs. Widespread availability of assembly equipment, materials, and technical know-how. | No. Little production capability |
| Willingness of foreign government to guarantee free export to DoD | Yes, written assurance | No |

[5] Building U.S. Capabilities in Flat Panel Displays, The Flat Panel Display Task Force Final Report, Department of Defense, October 1994.

## F. Conclusions

At present, IC assemblers, equipment, and materials suppliers (mostly off-shore) do not appear to have either the incentive or the market leverage needed to threaten to withhold supplies from DoD suppliers in order to gain financial or political advantage. Although semiconductor packaging materials supply is highly concentrated in Japanese vendors, U.S. companies can readily buy state of the art materials from Japanese suppliers. For ceramics, U.S. suppliers are competitive.

Leading-edge military package types, driven by finer pitch and higher precision, increasingly require fully automated assembly and inspection techniques. With this, the advantage of lower-cost, off shore labor becomes less of a deciding factor in assembly location and U.S. assemblers may be able to recapture part of this market. In reality, military semiconductor suppliers will continue to make packaging technology decisions based on required performance and cost tradeoffs and they have ready access to leading industry technology and practices.

An exception to this is in high performance MCM technology and manufacture. Industrial manufacturing infrastructure for advanced MCMs is not at the point where it can support increasing military demands for high performance semiconductor packages at affordable costs without DoD support. Many military electronics capabilities can be enhanced by MCM packaging. The advantages include lower cost, increased portability, reduced design to insertion cycle, and improved reliability. Although commercial use of MCMs is increasing, it is primarily in the lower performance MCM-L area.

The DoD/ARPA Advanced Electronics Packaging Program is directly addressing this issue by investing in support for development of MCM design and manufacturing technologies that can significantly reduce cost and increase acceptance and use by industry. A significant element of DoD's advanced packaging program is contained in the Technology Reinvestment Project. Continued support by DoD of MCM packaging can contribute significantly to the development of a dual use, U.S-based MCM manufacturing capability and infrastructure that will assure that future military needs in advanced, high performance packages can be met in an affordable fashion.

Beyond MCMs, the development of advanced packaging substrate materials processing technology and better understood assembly processes can result in even higher performance semiconductor devices. Potential advantages include improved thermal dissipation, higher temperature operation, higher clock speed, and increased packaging density. DoD R&D investments in these areas should be continued. Another high payoff area is the development of computer-aided packaging design codes that include complete thermal, mechanical, and electrical analysis (including electromagnetic interference) capabilities. The ability to predict performance and potential failures a priori can result in a much more efficient, lower cost, reduced turn-around packaging design processes. These areas require relatively modest DoD investments and can result in significant military and commercial payoff.

Under current and expected future circumstances, no vulnerabilities to meeting Defense needs have been identified in the supply chain for semiconductor packaging. Given the dependence on foreign supply, however, DoD access to semiconductor packaging materials, and to a lesser degree, assembly and equipment, should be monitored.

The focus of this assessment is assured access to critical military semiconductor packaging technologies, manufacturing and assembly operations, and supporting infrastructure. Table VI-3 summarizes our conclusions. It also lists possible DoD options for each of the technology and manufacturing areas. To meet DoD future needs, this assessment recommends continued R&D investment and joint industry-DoD development of new manufacturing technologies for MCMs and the related technologies of flip chip and direct chip attach. Development of new materials and computer aided design tools should be continued and expanded. Commercial technologies and capabilities exist for many military requirements and should be inserted into military systems as long as system reliability and performance are not compromised. This includes the accelerated, but judicious, use of plastic packaged ICs.

Table VI-3

**Relation of DoD Technology Investment to State of Dual Use Technology and Industrial Capabilities for Semiconductor Packaging**

| Packaging Technology | State of Technology | | | | | Possible Policy Options | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Military Unique | Access assured and commercial capabilities alone will be sufficient | Access is assured but DoD needs affordability in high-end technologies | Access is assured but DoD needs to ensure commercial suppliers can supply leading edge technology | DoD needs assured access to technology and industrial capabilities | R&D Investment | Develop and deploy new manufacturing technologies | Transition defense technology to commercial applications | Insertion of Commercial Technology |
| MCM C,D,L | | | X | X | | X | X | | X |
| 3-D MCM | | | | X | | X | X | | |
| Flip chip and Direct Chip Attach | | | X | X | | X | X | | X |
| Miniature QFP | | X | | | | | | | X |
| Grid Arrays (BGA, PGA) | | X | | | | | | | X |
| EMI resistant packaging | | X | | | | | | | |
| Radiation resistant packaging | X | X | | | | | | | |
| TAB | | X | | | | | | | X |
| **Assembly Infrastructure** | | | | - | | | | | |
| Assembly | | X | | | | | X(MCM) | | |
| Packaging materials | | X | | | | | | | |
| Packaging equipment | | X | | | | | X(MCM) | | |
| New substrates | | | | X | | X | | | |
| Computer Aided Packaging Design | | | | | X | X | | X | |

# APPENDIX A

## Glossary Of Terms

| | |
|---|---|
| AMC | Army Materiel Command |
| AMSAA | Army Materiel Systems Analysis Activity |
| ARPA | Advanced Research Projects Agency |
| ASIC | Application Specific Integrated Circuits |
| BGA | Ball Grid Array |
| $C^3I$ | Command, Control, Communication, And Intelligence |
| C4 | Controlled-Collapse Chip Connection |
| CAST | Commercial Acquisition Streamlining Team |
| CERDIP | Ceramic Dual-Inline Package |
| COB | Chip-On-Board |
| COG | Chip-On-Glass |
| CPGA | Ceramic Pin Grid Array |
| CQFP | Ceramic Quad-Flat Pack |
| DEIMS | Defense Economic Impact Modeling System |
| DESC | Defense Electronics Supply Center |
| DIP | Dual-In-Line Package |
| EIA | Electronics Industry Association |
| EMI | Electromagnetic Interference |
| GPS | Global Positioning Sensor |
| HAST | Highly Accelerated Stress Testing |
| HDTV | High Definition Television |
| IC | Integrated Circuit |
| ICE | Integrated Circuit Engineering Corporation |
| IDA | Institute For Defense Analyses |
| JEDEC | Joint Electronic Design Engineering Council |
| JTEC | Japanese Technology Evaluation Center |
| KGD | Known-Good-Die |
| LCCC | Leadless Ceramic Chip Carrier |
| MCM | Multi-Chip Modules |
| MCM-C | Ceramic Multichip Modules |
| MCM-D | Multi-Chip Modules - Deposited Thin Film |
| MCM-L | Laminated Multi-Chip Modules |

# Glossary of Terms (continued)

| | |
|---|---|
| Mil-Hdbk | Military Handbook |
| MIL-STD | Military Standard |
| MILSPEC | Military Specification |
| MMIC | Monolithic Microwave Integrated Circuit |
| NIST | National Institute Of Standards And Technology |
| OEM | Original Equipment Manufacturer |
| PCB | Printed Circuit Board |
| PDIP | Plastic Dual-In-Line Package |
| PEM | Plastic Encapsulated Microcircuit |
| PGA | Pin Grid Array |
| PLCC | Plastic Leaded Chip-Carrier |
| PQFP | Plastic Quad Flat Pack |
| PWB | Printed Wiring Board |
| QFP | Quad Flat Pack |
| QML | Qualified Manufacturers List |
| QPL | Qualified Parts List |
| SCM | Single Chip Module |
| SEMI | Semiconductor Equipment And Materials International |
| SIA | Semiconductor Industry Association |
| SMD | Standard Microcircuit Drawing |
| SMD | Surface-Mount Device |
| SMT | Surface-Mount Technology |
| SOIC | Small -Outline Integrated Circuit |
| SSQA | Standardized Supplier Qualification Assessment |
| TAB | Tape-Automated-Bonding |
| TAP | Technology Assessment Protocol |
| THM | Through-Hole Mounting |
| TRP | Technology Reinvestment Project |
| UAV | Unmanned Airborne Vehicle |
| ULSIC | Ultra Large Scale Integrated Circuit |
| VLSIC | Very Large Scale Integrated Circuit |