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Selective Etching of Silicon for Selective Area Epitaxial Growth

by Donna J. Advena and John H. Dinan

ARL-TR-983

April 1996

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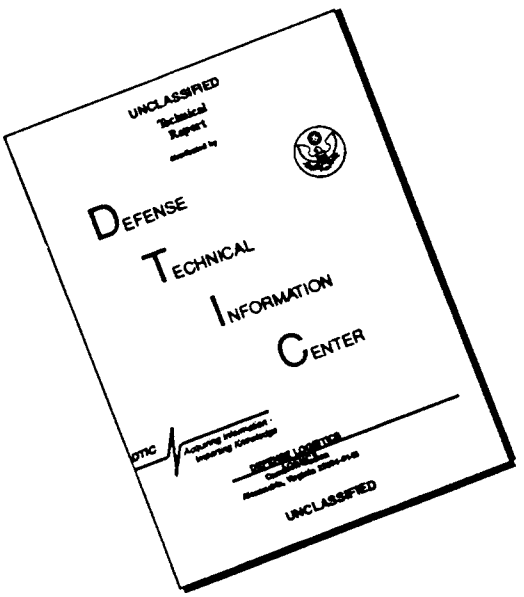

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ARMY RESEARCH LABORATORY

Selective Etching of Silicon for Selective Area Epitaxial Growth

by

Donna J. Advena
U.S. ARMY RESEARCH LABORATORY
John H. Dinan
U.S. ARMY CECOM NIGHT VISION AND ELECTRONIC SENSORS DIRECTORATE

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
U.S. Army Research Laboratory
Attn: AMSRL-SE-ED
10235 Burbeck Rd, Suite 110
Fort Belvoir, VA 22060-5838

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U.S. Army Research Laboratory
Attn: AMSRL-SE-ED
10235 Burbeck Rd, Suite 110
Fort Belvoir, VA 22060-5838

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Executive Summary

The work summarized in this report was performed under a Technology Program Annex in support of the Night Vision and Electronic Sensors Directorate. This work will result in the development of a monolithic infrared detector, thus increasing the performance and decreasing the cost of infrared detector arrays.

A process was established to enable the epitaxial growth of HgCdTe infrared material in recesses formed in a silicon wafer. Reactive ion plasma etching was chosen to etch undercut cantilevers with smooth floors in silicon. With a thermal oxide used as the mask, process parameters were optimized at a power of 100 W, pressure of 200 mtorr, and a sulfur hexafluoride gas flow rate of 18 standard cubic centimeters per minute (sccm). The etch rate of a 1×1 cm silicon piece with an array of 50-μm square holes and 100-μm spacing was 32,230 Å/min; this etch rate was 147 times faster than that of thermal oxide.

1. Introduction

Mercury cadmium telluride infrared detector arrays are costly because of the material growth methods and fabrication procedures necessary to process the nonstandard size detector material. Selective area epitaxial growth of this detector material is a process that can reduce defect densities [1–3] and allow for growth directly on silicon, leading to a monolithic technology and significantly reduced fabrication costs. For epitaxial material to be grown in selected areas on a wafer, the starting wafer must have undercut recesses with a smooth, single crystalline floor. The goals of this work are to (1) produce an undercut profile in 15 μm of silicon, and (2) leave a smooth silicon floor in the recesses. The undercut profile is necessary to prevent sidewall growth of the epitaxial material, and the smooth floor is necessary to accommodate high-quality epitaxial growth. Figure 1 illustrates two possible configurations that would allow for growth in recesses. To achieve the desired edge profile and wafer surface, we investigated both wet and dry etching. We used thermal oxide and photoresist as masks to determine which would best serve as the masking material. We also optimized process conditions to obtain high etch-rate selectivity between the silicon and masking layer and to minimize damage to the surface of the silicon.

2. Wet Etching (100) Silicon

We investigated several chemical etchants to determine which, if any, would produce the desired edge profile and surface morphology on the silicon wafer. The starting wafer was (100) silicon with a top layer of either thermal oxide (silicon dioxide) or silicon monoxide. The oxide was patterned with AZ 1350 JSF striation free photoresist and etched in a buffered oxide etch (BOE) consisting of 1 part hydrofluoric acid to 10 parts ammonium fluoride. Several different chemical mixtures were used to etch the silicon. Table 1 is a summary of etchant recipes and their result [4–7].

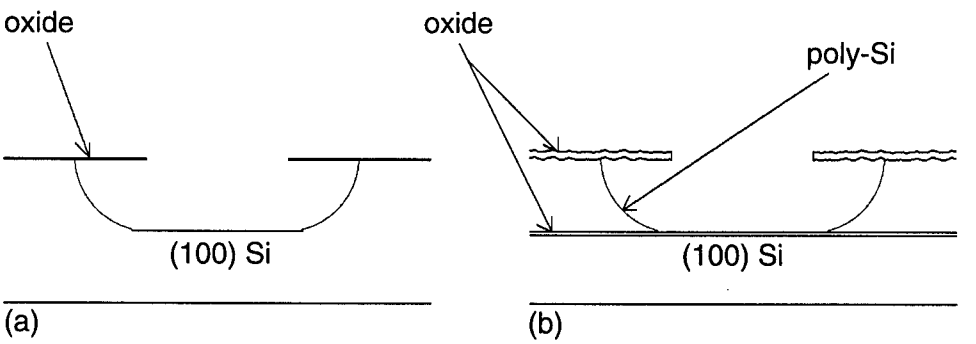

Figure 1. Two possible configurations that would allow for selective epitaxial growth in recesses. (a) Oxide masks recess, which is formed directly in single crystalline silicon. (b) Top oxide masks poly-Si recess. Bottom oxide layer protects single crystalline silicon and is removed before growth.

Table 1. Results of wet etching silicon.

Etchant	Ref.	Masking layer	Comments
50 mL H_2O 15 g KOH 15 mL isopropanol	4	0.2-μm SiO	Etchant heated to 70 °C; anisotropic profile; angled sidewall underneath cantilever; **rough surface**.
1000 mL H_2O 100 g NH_4F 2 mL H_2O_2 (30%)	5	0.2-μm SiO	Room temperature; **no significant etching**; sample was left in solution 5.0 minutes.
8% HF 75% HNO_3 17% CH_3COOH	6	0.2-μm SiO	**Mask etched**; smooth floor; nonuniform in areas where SiO was removed.
1 HF 3 HNO_3 10 CH_3COOH	7	0.2-μm SiO	Insignificant etching of Si; **mask etched** slowly.
5 mL HF (49%) 93 mL HNO_3 (70%) 48 mL H_2O	4	0.2-μm SiO	Fresh etchant at 30 °C; **mask etched**; smooth floor; bubbly and grainy in areas where SiO was removed. The same etchant cooled to room temperature had slower etch rate, and Si looked grainy. With same etchant a day old and at 25 °C, no etching took place.
5 mL HF (49%) 93 mL HNO_3 (70%) 48 mL H_2O	4	0.1-μm SiO_2	Fresh etchant at 30 °C; **mask etched**.

Significant results in bold.

The etch rate of silicon in the KOH/H_2O/isopropanol mixture was highly dependent on the temperature of the etchant solution. Rates ranged from 0.23 μm/min at 60 °C to 1.1 μm/min at 80 °C. The etched surface was also extremely rough. The $H_2O/NH_4F/H_2O_2$ solution did not etch the silicon, and two of the three $HF/HNO_3/CH_3COOH$ solutions and the $HF/HNO_3/H_2O$ solution attacked the masking layer. Because all wet etchants significantly roughened the wafer surface and did not always produce the undercut cantilevers needed for growth, reactive ion plasma etching was investigated.

3. Dry Etching (100) Silicon

The dry etch system used for this study was a Plasma-Therm Batchtop reactive ion etcher with a 20 ft^3/min rotary vane pump and throttle valve controller. The Batchtop was powered by a 13.56-MHz rf generator and had a parallel-plate configuration with an automatic matching network. Parameters that were varied included etch gas, flow rate, power, pressure, and etch time. The bias voltage, which is a result of other etching parameters, was also recorded. The wafers were (100) silicon patterned with photoresist or thermal oxide.

3.1 Photoresist Mask

The first set of experiments used a combination of CF_4 and O_2 gases and was carried out on silicon wafers patterned with AZ 1350 JSF photoresist. Table 2 shows selectivity and etch rates of silicon and photoresist versus rf power level. While the etch rates of both the silicon and photoresist increased with increasing power, selectivity did not dramatically change. The O_2 content was then varied from 8 to 25 percent while the other parameters were kept constant. Figure 2 illustrates how the selectivity between the silicon and photoresist varied with O_2 content. A maximum selectivity of two was obtained when the O_2 content of the etch gas was 16 percent. A selectivity of two was insufficient to etch 15 µm of silicon, because the photoresist is typically 2 µm thick. The etching of silicon using thermal oxide as the masking layer was then investigated.

Table 2. Etch rates and selectivity of silicon patterned with photoresist at varying power levels.

Power (W)	Si etch rate (Å/min)	Resist etch rate (Å/min)	Selectivity (Si/resist)	Dc bias voltage (V)
100	320	450	0.71	240
125	560	880	0.63	290
200	1260	2110	0.60	390

Other etch parameters: pressure = 200 mtorr, O_2 content = 8% in CF_4, and total gas flow = 20 sccm. Pattern of 100-µm open lines with 200-µm spaces.

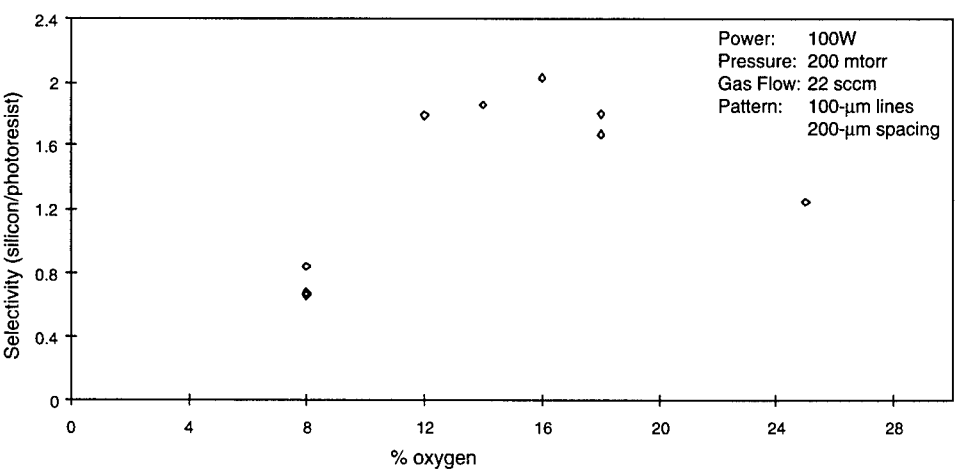

Figure 2. Etch rate selectivity (silicon/photoresist) versus percentage of oxygen content in CF_4.

3.2 Thermal Oxide Mask

The wafers were (100) silicon with an 1100-Å thermal oxide masking layer. The etching conditions were the same as before: power = 100 W, pressure = 200 mtorr, total gas flow = 22 sccm, bias voltage = 240 V, and a pattern of 100-μm lines with 200-μm spaces. A maximum selectivity of 22 was obtained at 14-percent oxygen, as shown in figure 3. However, the surface of the silicon was unacceptably roughened under these etching conditions. The gas was then switched to very-large-scale integration (VLSI) grade SF_6 with the other parameters as follows: pressure = 200 mtorr, power = 100 W, SF_6 flow rate = 18 sccm, and bias voltage = 12 V. With the new etch gas, the selectivity increased to 70. The edge profile was similar to that obtained with the CF_4/O_2 mixture, but the surface morphology of the silicon was significantly improved as compared to the previous procedure. The improved surface morphology was probably due to the drop in bias voltage, which resulted in less ion bombardment at the surface of the silicon.

During this study, it was found that pattern size dramatically affected etch rates. A 3-in. silicon wafer was patterned with square holes of three sizes: 50, 100, and 500 μm. Table 3 shows how the etch rate increased with decreasing hole size. Since the thermal oxide etch rate did not change much, selectivity increased for decreasing hole size. Table 4 lists etch rates and selectivity for a second set of etching parameters. A selectivity as high as 600 was established for a square hole, 50 μm on a side, with the following parameters: power = 100 W, pressure = 300 mtorr, SF_6 gas flow = 15 sccm, and O_2 gas flow = 1.7 sccm. However, the addition of oxygen made the surface rough, and the sidewalls appeared to extend out more from underneath the cantilever compared to samples etched at 200-mtorr pressure and no oxygen.

Table 5 documents how pressure changes affected selectivity. The selectivity starts to increase with increasing pressure, but drops off dramatically between 300 and 500 mtorr. The effect of an oxygen plasma clean before the sulfur hexafluoride etch is also demonstrated in this table. The oxygen

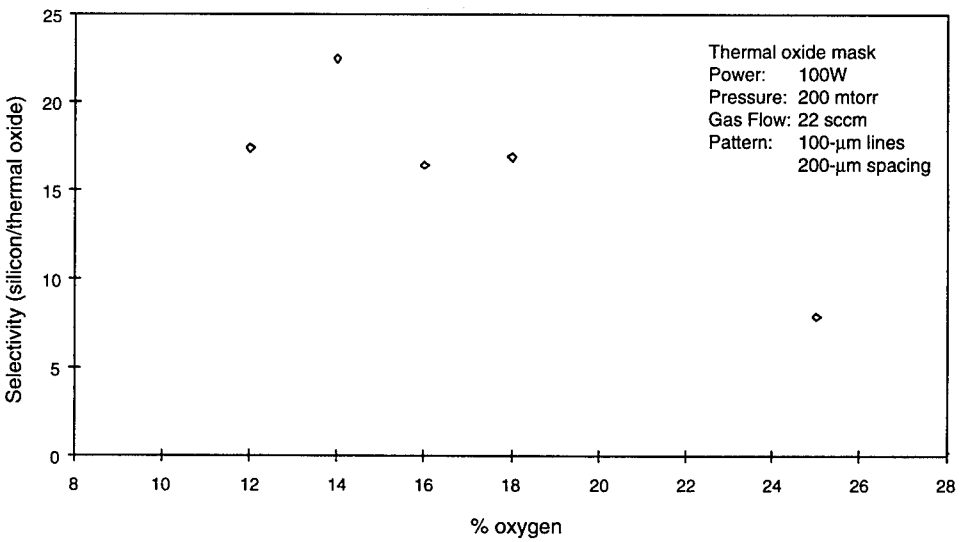

Figure 3. Etch rate selectivity (silicon/thermal oxide) versus percentage of oxygen content in CF_4.

Table 3. Effect of hole size on etch rates and selectivity.

Hole size (100-μm spacing)	Silicon area/ total area	Si etch rate (Å/min)	Oxide etch rate (Å/min)	Selectivity (Si/oxide)
500 × 500 μm	0.69	8,000	115	70
100 × 100 μm	0.25	19,500	145	134
50 × 50 μm	0.11	22,300	145	154

Etching parameters: power = 100 W, pressure = 200 mtorr, and SF_6 flow rate = 15 sccm.

Table 4. Effect of hole size on etch rates and selectivity for different pressure and flow rate.

Hole size (100-μm spacing)	Silicon area/ total area	Si etch rate (Å/min)	Oxide etch rate (Å/min)	Selectivity (Si/oxide)
500 × 500 μm	0.69	9,050	45	200
100 × 100 μm	0.25	22,700	75	300
50 × 50 μm	0.11	27,400	45	600

Etching parameters: power = 100 W, pressure = 300 mtorr, total gas flow rate = 16.7 sccm (10% O_2 in SF_6).

Table 5. Effect of pressure change on etch rates and selectivity.

Pressure (mtorr)	Si etch rate (Å/min)	Oxide etch rate (Å/min)	Selectivity (Si/oxide)
200	15,880	170	93
300	8,440	50	169
300 (with O_2 preclean)	10,070	130	77
500	520	70	7.4

Etch parameters: power = 100 W, SF_6 flow rate = 15 sccm, and 200 × 200 μm open squares with 100-μm spacing.

preclean increased the silicon and oxide etch rates, but decreased the selectivity.

The next batch of substrates were (100) Si with 13,500 Å of thermal oxide as the masking layer. The thicker oxide allowed for longer etch times and deeper etching into the silicon. A scanning electron micrograph of an etched sample is shown in figure 4. The angled profile of the oxide layer was due to lithography problems during the BOE etch of the oxide layer, and was not a result of plasma etching. The tapered oxide mask could also account for the bottom surface near the edge of the hole appearing rounded instead of flat.

The effect of flow rate on selectivity and surface morphology was investigated next. The flow rate of the SF_6 gas was varied from 10 to 30 sccm, as shown in table 6. The oxide etch rate was fairly constant, while the silicon etch rate increased with an increase in flow rate, peaking at 20 sccm and then dropping off. The dc bias voltage did not change with changes in the flow rate of the gas, remaining at 15 V. While the flow rates between 15 and 25 sccm produced fairly smooth surfaces, rates above and below that window created grainy, rough surfaces.

In additional experiments, we added argon to the SF_6 for a total flow rate of 15 sccm to determine its effect on the etch rates and selectivity. At

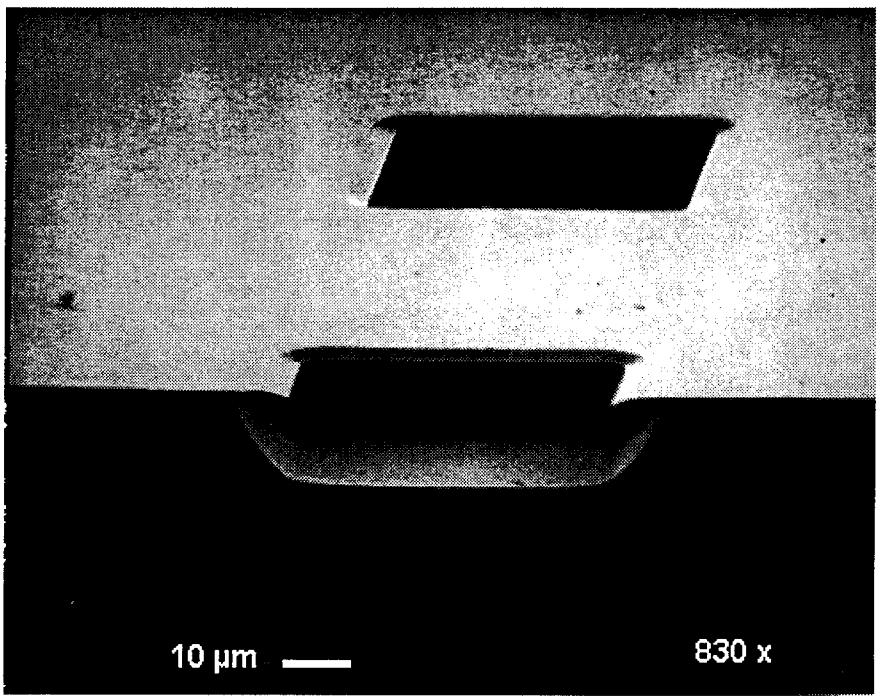

Figure 4. SEM photograph of plasma-etched recess in (100) Si. Etch parameters: power = 100 W, pressure = 200 mtorr, SF_6 flow rate = 18 sccm.

Table 6. Effect of SF_6 flow rate on etch rates and selectivity.

Flow rate (sccm)	Si etch rate (Å/min)	Oxide etch rate (Å/min)	Selectivity (Si/oxide)
10	29,160	250	117
15	29,820	240	124
18	32,230	220	147
20	33,180	220	151
25	30,840	240	129
30	27,440	250	110

Etch parameters: power = 100 W, pressure = 200 mtorr, and pattern of 50 × 50 µm holes.

2-percent Ar, the bias voltage and selectivity remained the same (15 V and 124, respectively). With 25-percent Ar, the bias voltage increased slightly to 20 V, and the selectivity decreased slightly to 112. The resulting silicon surface exhibited rougher morphology in both cases.

Most samples were etched with the substrate "as is"; that is, no attempt was made to clean the surface before the plasma etch. After the oxide was patterned, the photoresist was removed by the samples being rinsed in acetone, then methanol, and dried with nitrogen. However, we precleaned a few samples in various ways to see if this could improve the fairly smooth surface. A preclean etch with sulfuric acid:hydrogen peroxide, 4:1, resulted in an extremely rough surface and a lower silicon etch rate. Precleaning samples in acetone with an ultrasonic cleaner and rinsing with methanol also roughened the surface. An oxygen plasma preclean was also investigated, and it too had a negative impact on the smoothness of the surface. All attempts to preclean the wafers resulted in etched surfaces with rougher surface morphologies.

The parameters for etching silicon to obtain a high selectivity over oxide and a smooth floor were optimized at 100-W power, 200-mtorr pressure, and 18-sccm flow rate of SF_6 gas. Although the recessed floors were fairly smooth, the goal was to have a recessed floor as smooth as the original surface. Therefore, etching was examined on an oxide/poly-Si/oxide/Si wafer. The goal was to plasma etch through the poly-Si with the top oxide used as the mask, and leave enough oxide on the bottom to protect the underlying single crystalline silicon. The bottom oxide could then be etched before epitaxial growth.

4. Dry Etching Recesses in Poly-Silicon

In the following experiments, the wafers had a configuration as shown in figure 1(b), with a top oxide layer 1 μm thick, 15 μm of poly-Si, and a bottom oxide layer 1000 Å thick. The top oxide was patterned with photoresist and etched in BOE. The photoresist was then removed, leaving the top oxide layer to serve as the mask for the poly-silicon. The etch parameters were pressure = 200 mtorr, power = 100 W, SF_6 flow rate = 18 sccm, and bias voltage = 12 V. The etch was stopped to leave 300 to 600 Å of oxide at the bottom of the recess. Therefore, the remaining oxide could be etched in BOE just before growth of the epitaxial layer. The dry etch resulted in an undercut profile with an overhanging oxide cantilever, an excellent candidate wafer for selective area epitaxial growth. The scanning electron micrograph in figure 5 shows the undercut profile in the polysilicon and the overhanging oxide cantilever.

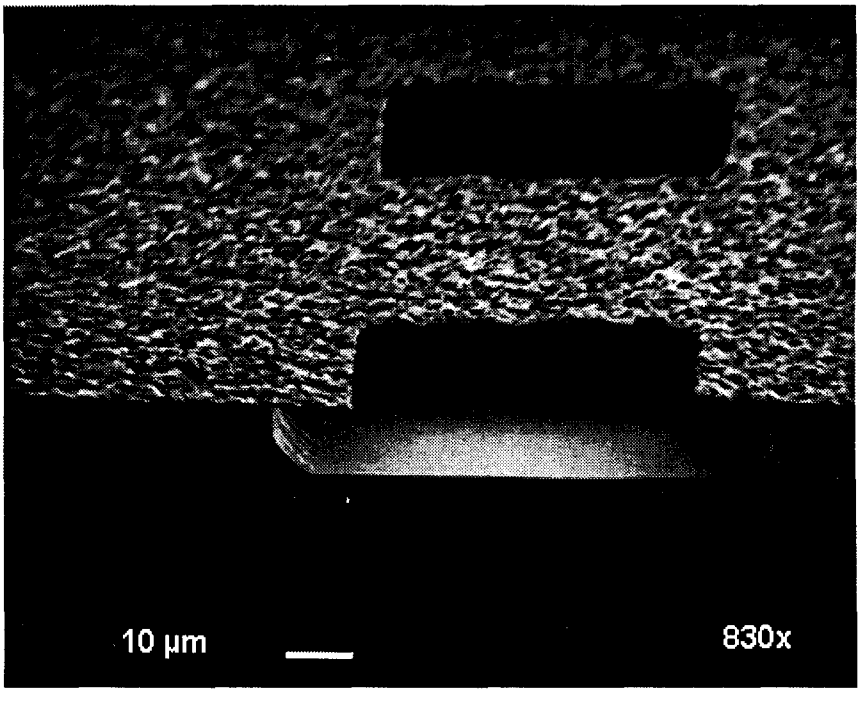

Figure 5. SEM photograph of plasma-etched poly-Si with oxide mask. Etch parameters: power = 100 W, pressure = 200 mtorr, and SF_6 flow rate = 18 sccm.

5. Conclusions

In this study, a process was established to enable the epitaxial growth of HgCdTe in recesses formed in a silicon wafer. Reactive ion plasma etching was chosen as the method to etch undercut cantilevers with smooth floors in silicon. The method resulted in high selectivity, etching silicon many times faster than thermal oxide. Selectivity was dependent on the hole size of the pattern. The optimized parameters that produced the highest selectivity and the smoothest floor in silicon were power = 100 W, pressure = 200 mtorr, and SF_6 gas flow rate = 18 sccm. Plasma etching produced the undercut cantilevers necessary to prevent sidewall growth of epitaxial material, and left a smooth oxide protective layer while the substrate awaited growth.

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