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A UNIVERSAL SMART WEAPON MICROPROCESSOR

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This report recommends a microprocessor suitable for use in all future smart weapons. To select such a microprocessor, a general knowledge of smart weapons is presented first. For a further understanding of smart weapons, the operation of a specific system, STAFF, is described. The specifications of the desired universal microprocessor are then enumerated. The currently available microprocessors are studied, compiled, and compared. Texas Instruments' TMS320C80 is recommended as the universal microprocessor for future smart weapons.

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INTRODUCTION

The objective of this report is to recommend a microprocessor suitable for use in any smart guided weapon that might be developed in the future. The reason such a microprocessor is needed is that each of the microprocessors presently used in a smart weapon becomes quite outdated by the time the weapon has reached the production stage. A microprocessor is required that is more powerful, that can do multiprocessing, and that has greater memory so it can handle additional future input and output requirements.

Microprocessors are classified into complex instruction set computer (CISC) and reduced instruction set computer (RISC) types. The latest type of microprocessor, which is especially applicable to smart weapons, is the digital signal processor (DSP). The DSPs resemble the original computers that were designed for solving mathematical problems, such as ballistic firing tables. Digital signal processors are available in CISC and RISC versions.

This report will recommend a particular DSP as the universal smart weapon microprocessor. The DSP derives its special abilities from its various multiplicities. It may have two external buses, two buses to external memory, multiple communications ports, two accesses per cycle, and two pipeline systems. These characteristics allow the DSP to perform at a rate of millions of floating point operations per second (MFLOPS). The disadvantage of a DSP is that it has certain programming difficulties because of its architecture.

In order to select the desired microprocessor a good understanding of its functioning in a smart weapon system is required. First, a generalized system will be presented that will show what every smart weapon system must have. From this generalization, additional future mechanical and electronic functions will be hypothesized, and consequently, the additional operations that the microprocessor must perform.

The smart target activated fire and forget (STAFF) system has been selected as an example of what could be done to improve upon present smart weapon systems used by the U.S. Army. The STAFF system, which is presently under development, will first be considered functionally. The microprocessor system will then be presented, and each of the sections will be explained. The physical layout of the microprocessor will be descibed, and its electronic functions will be presented using block diagrams. The basic specifications of the required microprocessor will then be enumerated. Its architecture, types of processing, and memory requirement will be explained.

The speed of a microprocessor is measured in MFLOPS. In order to select the required microprocessor, a MFLOPS spec must be determined. The MFLOPS of each section of the STAFF system will be presented. The MFLOPS spec for the required microprocesor will then be set to a value that must exceed the worse case value of the

STAFF system. Although the specs of the required microprocessor have 22 items, the most important ones are speed, memory and versatility. A search of six domestic companies was made. Their specs were compared, and a microprocessor was selected that met the above mentioned specs, and was also cost effective.

ELEMENTS OF A SMART WEAPON SYSTEM

Figure 1 shows the basic components of a typical smart weapon system signal processor. After the weapon is aimed and fired in the direction of a target, it continuously receives either thermal, radar or other types of signals from the ground. This information is converted to digital form by an analog to digital converter. This must be done since the system microprocessor is digital. The information is then conditioned. It undergoes spectral processing which modifies it so that targets can be discriminated. Finally, the microprocessor generates signals that either cause the weapon to turn towards the target, to fire a lethal mechanism at the target, or to detonate the weapon if no target is detected.

More specifically, the microprocessor controls a number of signals almost simultaneously. Smart weapons are equipped with either radar, infrared, electromagnetic, acoustic, magnetic or other types of sensors. These sensors detect objects that may or may not be targets. The signals from these objects are fed to the microprocessor which processes them in order to discriminate between targets and non-targets. During flight, some types of smart weapons use a reference that produces signals to indicate the orientation of the weapon with respect to ground. On verifying a target, if the weapon is guided, the microprocessor sends signals to the weapon's control surfaces which turn the weapon so that it strikes the target. In some weapon systems, the final function of the microprocessor is to determine the best time to detonate the warhead.

In order to select a microprocessor for a universal smart weapon processor, one must foresee what additional signals a microprocessor might have to process in a future smart weapon. There may be new sensor inputs and additional outputs for new mechanical functions. A universal microprocessor for future smart weapons, then, must have a capacity for handling several more input and output signals than present microprocessors do.

SMART TARGET ACTIVATED FIRE AND FORGET (STAFF) SYSTEM

ARDEC, in conjunction with Alliant Techsystems Inc., has been developing the STAFF smart weapon for a number of years. In order to obtain a better understanding of how a microprocessor functions in a particular smart weapon system, the operation of the STAFF system will be presented next.

Figure 2 shows a cross-section of a STAFF round, indicating all of the mechanical and electronic components. Figure 3 shows the STAFF electronics. In firing the STAFF round, the operator first sets the range switch on the STAFF after the range-to-target is estimated or determined electronically. The range switch is used to inhibit the functioning of the round until it is in the vicinity of the target, thus preventing the incidence of false alarms. The operator then loads the round into the tank gun. Through his sighting telescope, he aims at an imaginary basket above the target and then launches the weapon.

As shown by figure 4, the downward looking radar searches for the ground, and then the microprocessor sends signals that keep the forward looking radar pointed at the ground. It does this by receiving information from the rate sensor and then giving torque commands to the electromechanical roll control system (EMRCS).

At the beginning of the weapon flight, the forward looking radar is activated and looks for the target, as shown in figure 5. When the target is detected, the microprocessor will continuously process signals from the radar to determine if it is in fact the desired target. When the target is verified, the microprocessor will send signals to the weapon fins to roll the weapon and point the warhead at the target.

The microprocessor will then send signals to eject the warhead cover and arm the weapon. The downward looking radar, that has been pointed at the ground directly below the weapon from the beginning of the flight, will then give signals to the microprocessor which will decide the best time to fire the munition. Finally, the microprocessor will emit a signal to fire the explosively formed penetrator when the weapon is near the target. This scenario is shown in figure 6.

STAFF ELECTRONICS

In order to understand what the capabilities of a smart weapon microprocessor are and what is expected from it in a future weapon system, the electronics of the STAFF system are described next in more detail.

The electronics consists of integrated circuits (IC) mounted on five flex or printed circuit boards (PCBs). Figure 7 shows PCBs 3 and 4, which contain the bulk of the electronics. Electrically programmable read only memory (EPROM) holds the weapon program. The system microprocessor is the Texas Instruments SMJ320C30 (C30). It stores and retrieves information from the static random access memory (SRAM) while executing various parts of the program. In order to perform the specialized high-speed functions required by the system processor, and to comply with the system's rigorous form and fit requirements, Alliant Techsystems had to design four application specific

integrated circuits (ASIC): designated 3.1, 4.1, 4.2, and E.1. ASIC 3.1 does timing and control, ASIC 4.1 performs spectral processing, two ASIC 4.2s perform down-conversision and filtering, and ASIC E.1 performs data-linking.

Figure 8 shows the block diagram of the STAFF system processor C30. Printed circuit boards 1 and 2 contain the power supply circuitry . Printed circuit board 3 contains the C30 and ASIC 3 .1. Printed circuit board 4 contains two ASIC 4 .1 and ASIC 4 . 2 . Printed circuit board 5 contains the analog-to-digital (A/D) converter and multiplexer.

On launching the weapon, the thermal battery is activated and the power conditioning unit applies power to the electronic system. The A/D converter then begins to receive signals from the forward and downward looking radars. These analog signals are conditioned and then converted to digital form in preparation for digital signal processing.

The output of the A/D converter is connected to the signal conditioning board (PCB 4), where the data enters ASIC 4.2. There it is filtered by a finite impulse response (FIR) filter (fig. 9). These data are then transmitted to two 4.1 ASICs for spectral processing. Figure 10 shows a block diagram of the elements involved in the processing. The processing is performed in conjunction with the C30, using a fast Fouriertransform (FFT).

Printed circuit board 3 contains the C30, the SRAM data memory, and the timing and control ASIC 3.1. During manufacture of the weapon, the system program is permanently burned into the EPROMs on PCB 4. As the microproccessor processes data, it places the data in, or removes it from, the SRAM. The integrated circuit, ASIC 3.1, coordinates all the computing processes of the system processor. Figure 11 shows these timing and control functions. Note that the system has four different clocks. Also note that in the operation of the C30, ten different functions are multi-plexed. The signals handled by the system processor can be classified either as inputs, outputs, or two-way. The only signal that is two-way is the data-link, which gives the range of the target either through the fire control system or the range switch. The signals inputted to the system processor are those of the sensors, while those that are outputted are those for firing, motion and electronic control, and telemetry.

SPECIFICATIONS OF THE UNIVERSAL MICROPROCESSOR

Having now seen the processing that the microprocessor must perform in a smart weapon system, the general specifications of a universal microprocessor can now be set down. The most important spec is speed, or the number of operations that a

microprocessor can perform per unit time. This report recommends a CISC DSP as the universal microprocessor. The following characteristics give it its speed:

- Harvard architecture, which has dual program and data access
- Either sequential-staging or parallel-processing versions of multiprocessing
- Iterative algorithmic processing performed by a highspeed multiplyand-accumulate
- Iteration control that gives extremely efficient matrix manipulation
- Floating point operation, which eliminates the need of a program for scaling intermediate results.

Another specification for the required microprocessor is that it have as much memory as possible without sacrificing any other important specification. Since in a universal smart weapon microprocessor the number and operation of future functions is not known, as much on-chip memory as possible must be provided. Newer DSPs have memory for instructions and data that ranges from 16 megabytes (MB) to 4 gigabytes (GB).

The versatility of a particular DSP is its ability to handle various operations simultaneously. The DSP that will be recommended in this report has this ability, since it has a number of DSPs in one package. The versatility of the recommended DSP is also its ability to be adapted to other future smart weapons with minimum reconfiguration.

SPEED OF THE UNIVERSAL MICROPROCESSOR

The universal microprocessor must be capable of operating at a speed that is at least as fast as the fastest processing component plus any other system processor components operating at the same time, in order to keep up with the incoming information. The speeds of DSPs range from 20 to 100 MFLOPS. In order to see how much speed is needed in smart weapon electronics, the speeds generated in the STAFF system will be presented.

The STAFF system processor operates in four modes: search and track, discrimination, fuzing, and vertical sensing. Figure 12 shows the signal processing for the search and track, and discrimination modes; while figure 13 shows that of the fuzing, and vertical sensing modes. Both figures can be divided into three sections. On the left the A/D operations, in the center the ASIC 4.2 weighted sum operation, and on the right the ASIC 4.1 window weight, FFT, and sample presum operations.

Table 1 shows the MFLOPS of each of the ASICs for each mode. The worse case is 39.6 MFLOPS. In the design of a new smart weapon, then, the system microprocessor must be able to handle information with at least a 40 MFLOPS rate. The MFLOPS in Table 1 are maximum numbers based on continuous operation. To get exact figures requires a detailed analysis of this report.

The maximum speed of typical smart weapons such as PGMM, SADARM and WAM are 24,1 and 10 MFLOPS respectively. Selection of a universal microprocessor operating at 50 MFLOPS should sufficiently handle all future smart weapon system microprocessor requirements. Each DSP of the microprocessor that this report will recommend is rated at 100 MFLOPS, twice the speed of current systems.

SELECTION OF THE UNIVERSAL MICROPROCESSOR

A typical CISC DSP operates at 25 MFLOPS, while that of a RISC DSP operates at 50 MFLOPS. While RISC DSPs have a faster instruction cycle, they generally lack the hardware to perform the real-time digital signal processing that CISC DSPs can perform. In the design of a smart weapon processor, then, a study must be made to determine which of its processors can be of the CISC type and which of the RISC type.

To determine the most suitable microprocessor for future smart weapon systems, the DSPs of the following domestic companies were investigated: American Telephone and Telegraph (ATT), Analog Devices (AD), Intel, Motorola (MOT), National Semiconductor (NS), and Texas Instruments (TI). Table 2 shows the parameters of the DSPs studied. Of the DSPs with one DSP per package, the TI TMS320C40 (designated as the TI C40 on Table 2) has the best overall characteristics.

In the last several years, several manufacturers have developed rnultiprocessors (mPs); ICs with more than one DSP per package. In our mP selection, then, it must be decided whether to use several DSPs or one mP in our system processor design. Referring to figure 8 again, microprocessors C30 and ASICs 4.1 and 4.2 could be four individual DSPs or they could all be contained in one mP. Two of the ASICs perform spectral processing and one does FIR filter processing. These functions will not change in any future smart weapon; therefore, they can be contained in one package.

Use of individual DSPs in a system has a number of advantages. A CISC or RISC type DSP can be selected for a particular function, whereas in an mP all the DSPs necessarily are the same. Another advantage of using individual DSPs is that after design, if some unexpected change must be made, the redesign is much easier to accomplish, both electronically and mechanically.

Using one mP rather than a number of DSPs also has a number of advantages. The mP that will be recommended has five DSPs and a SRAM. The four processing

functions and the SRAM can be contained in one IC, thereby eliminating four ICs that are in the STAFF system processor. Another advantage of a mP is increased reliability. DSPs have from 100 to over 300 external connections. In a mP many of these connections are internal, so that the number of solder connections needed is greatly reduced .

The reduction in the number of ICs when a mP is used results in a financial gain. The cost of the mP that will be recommended will be less than the four DSPs and the SRAM that it will replace in a typical system that presently exists, resulting in a cost saving .

The large cost savings realized, however, is through the elimination of the ASIC development costs when a mP is used. In a new smart weapon system processor using the proposed mP, the master processor (MP) would be the system microprocessor; one DSP would execute FIR filtering, two DSPS would accomplish spectral processing, and the SRAM would hold the data. Furthermore, once the universal smart weapon processor has been designed, its modification for use in other future smart weapons will result in much lower design costs.

The microprocessor recommended for use in future smart weapons is the TI 32-bit TMS320C80 mP. Figure 14 is a block diagram of this microprocessor. It integrates four DSPs; a RISC MP; a SRAM crossbar memory, a memory containing a network of crossed wires that can be variously interconnected; and memory and video controllers. The five DSPs execute independently and concurrently. A crossbar connects the DSPs with 25 2 KB blocks of SRAM, The SRAM provides RAM and cache memory for each DSP. The function of the cache memory is to hold data needed only temporarily. Any DSP can access any of 16 SRAM blocks. The peak crossbar bandwidth is 4.2 GB/sec. Memory-mapped control registers handle both the transfer and video controllers.

The mP has high DSP throughput, each DSP executing from its own crossbar instruction cache memory. The memory of each DSP is 2 KB, while that of the master processor is 4 KB. The MP also has a 4 KB data cache. The DSPs perform operations with single cycle execution.

Each DSP has a 64-bit instruction word for controlling the data unit and each of two independent address units. Each address unit has a 32-bit data path to the crossbar.

The MP has an integrated 64-bit floating point unit (FPU) that shares a common register file with integer processing. The FPU supports vector processing with built-in vector operations and four accumulators. Vector instructions can start a multiply, add, and load or store every cycle, which results in a peak performance of 100 MFLOPS. The whole mP has the capability of two billion operations per second.

There are three other specs that the required microprocessor must meet regardless of the one chosen. They are the specs for operating voltage, operating temperature, and packaging. The required microprocessor must operate in the 3.0 to 5.5 volt range to be compatible with the other ICs in the system processor. The STAFF system microprocessor operates over the mil spec temperature range of -55 to 125 deg. C. This requirement is excessive, since the weapon itself only has to be operable over the temperature range of -32 to 49 deg. C. Establishing the latter temperature range for the required microprocessor will reduce its cost appreciably. Lastly, the microprocessor must be housed in a ceramic pin grid array package in order for it to be able to withstand the gun firing forces.

To complete the perspective on the choice of the required microprocessor, several other factors must be considered. One is the use of the C high level programming language. In the evolution of microprocessors, operating systems based on C were developed. This led to the development of C compilers and development tools based on C. The programs, then, for microprocessor systems are usually written in C. Therefore, when developing microprocessor systems, the C language cannot be avoided. Since most engineers are familiar with C, and since it is easier to work with than other languages, it should be adopted by the whole electronics industry for microprocessor work. Since Ada is the Department of Defense mandatory programming language, an Ada use waiver must be obtained at the start of any microprocessor project.

CONCLUSIONS

The TI TMS320C80, containing five digital signal processors (DSPs) in one package, a maximum speed of 100 MFLOPS per DSP, and a 50 KB data memory, is proposed for use as the universal smart weapon system microprocessor. Use of this microprocessor will result in less component, development and redesign costs compared with a design using one DSP per package. The system processor will be more reliable because of the great decrease in the number of solder connections, since one microprocessor replaces a number of individual DSPs.

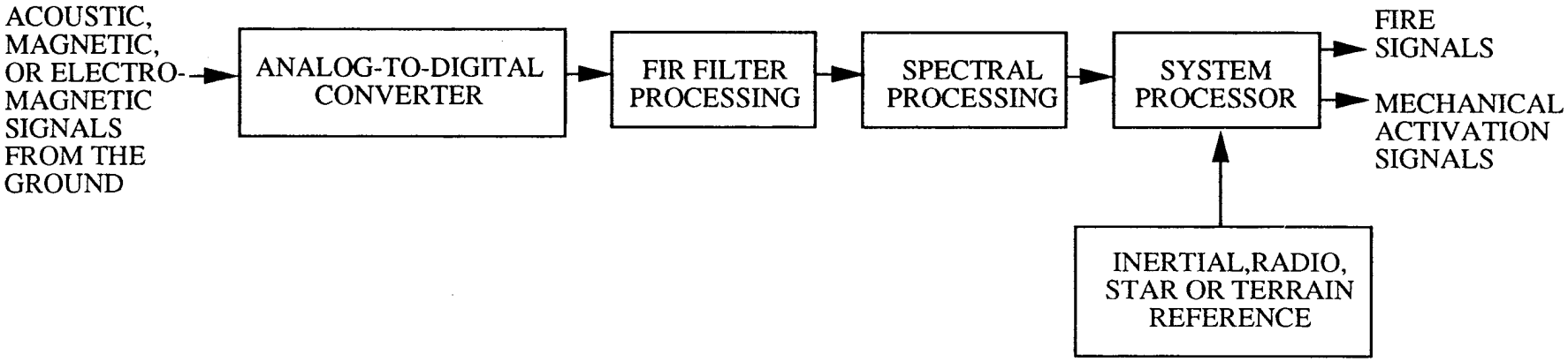


Figure 1
Basic elements of a smart weapon signal processor

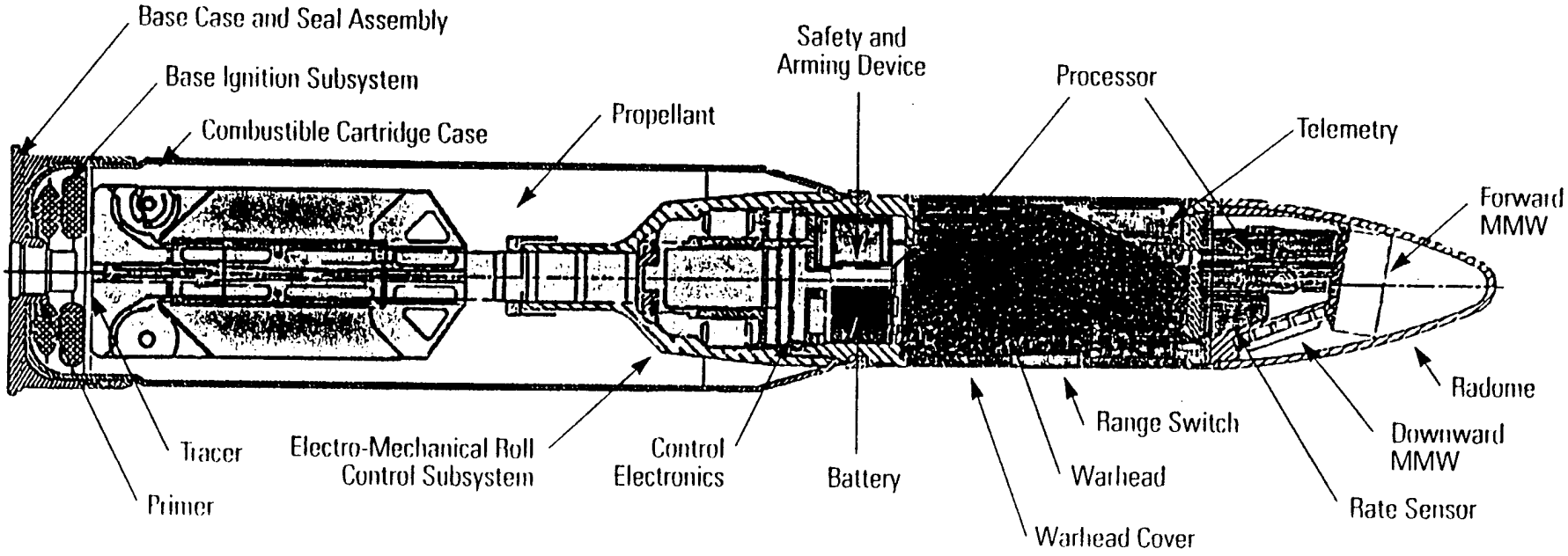


Figure 2
STAFF round

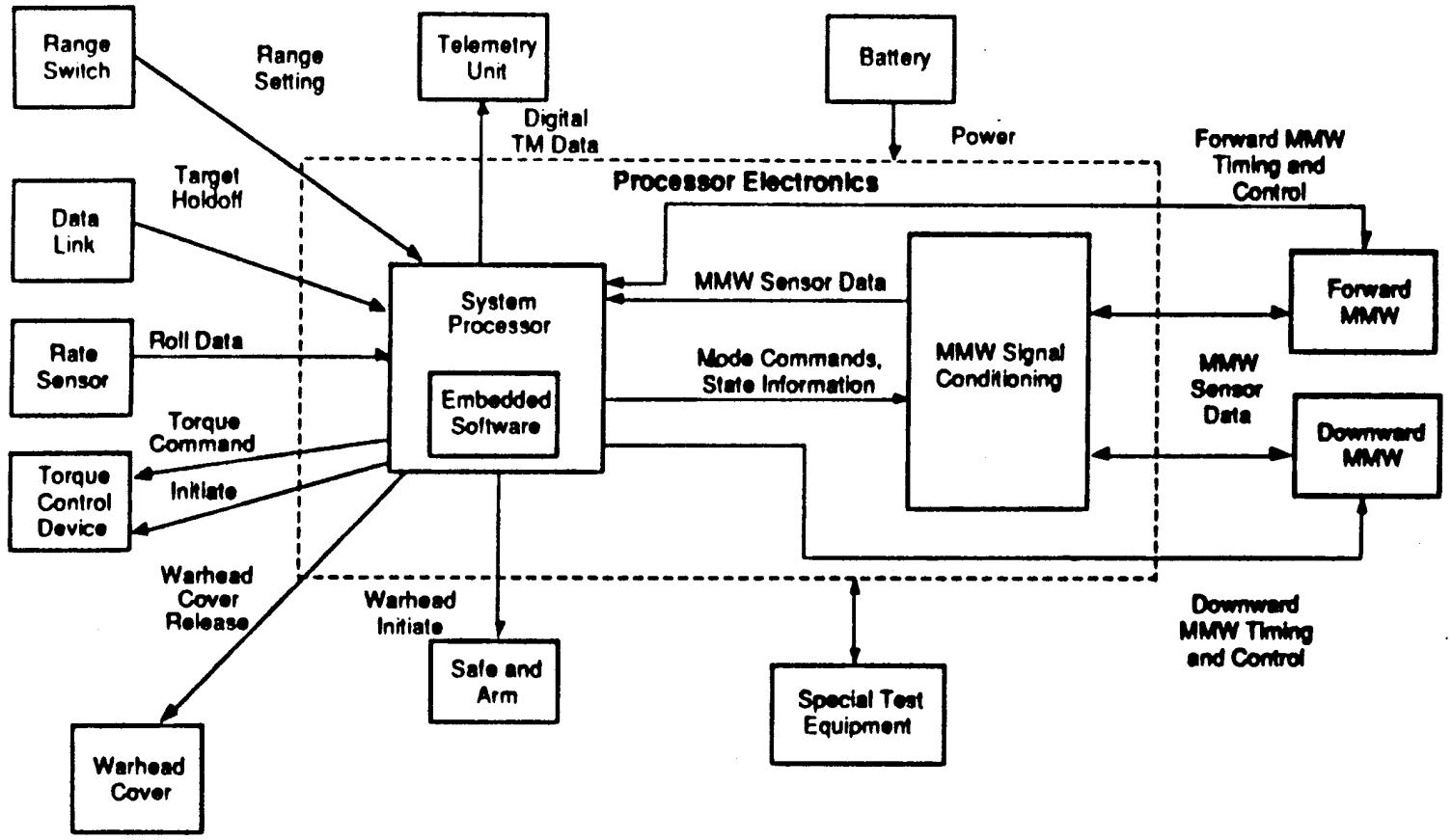


Figure 3
STAFF electronics

Down Looking Sensor looks for the ground.

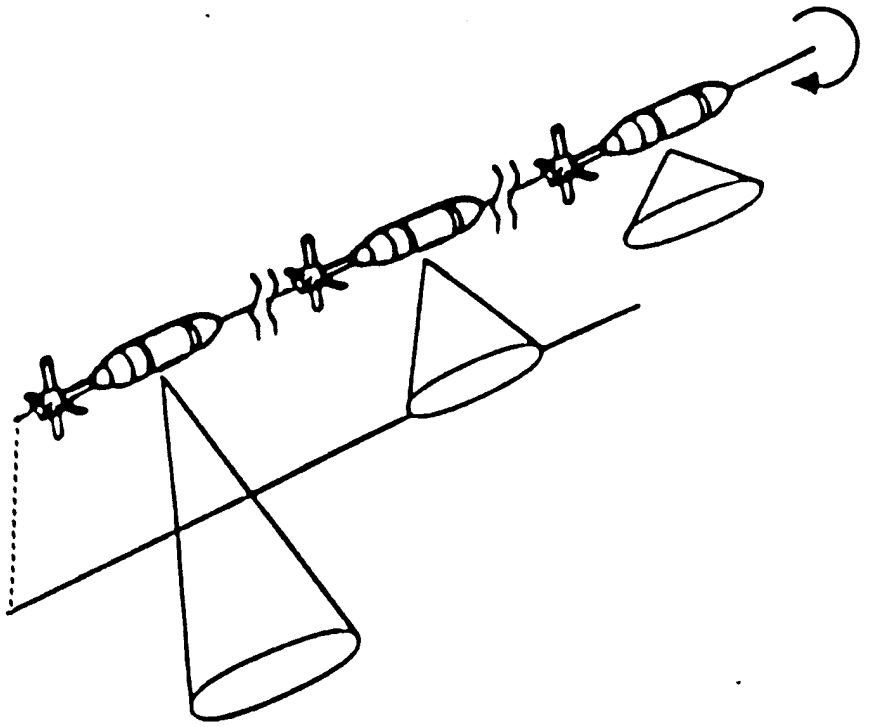


Figure 4
Downward looking radar

Forward Looking Sensor looks for the target.

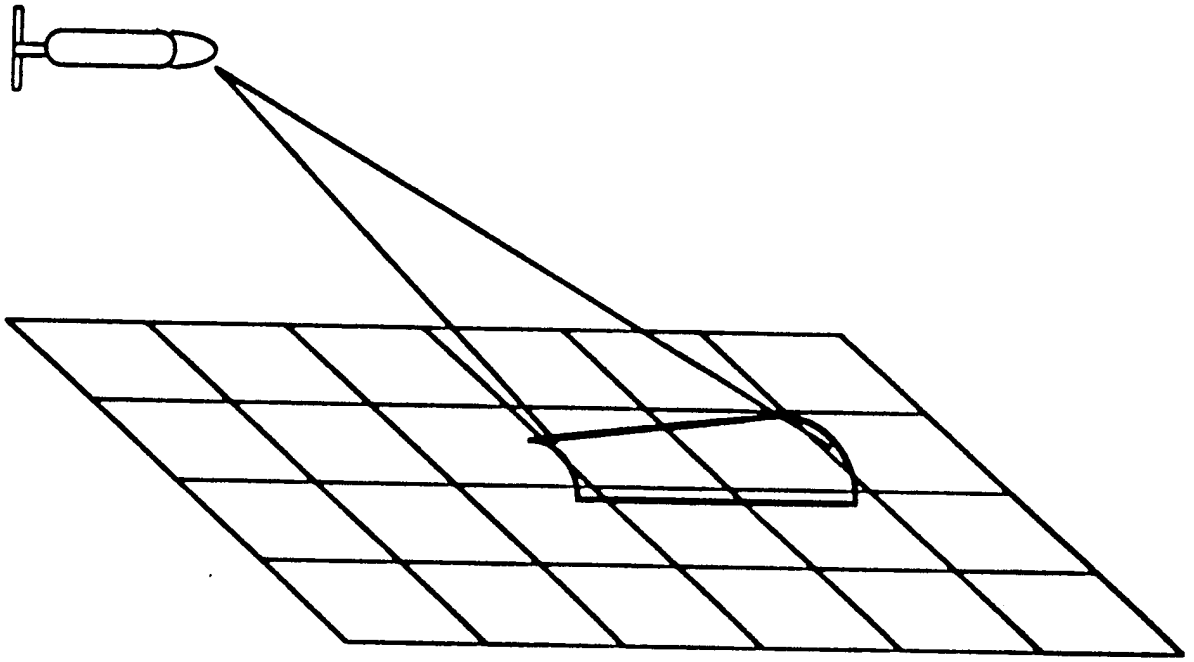
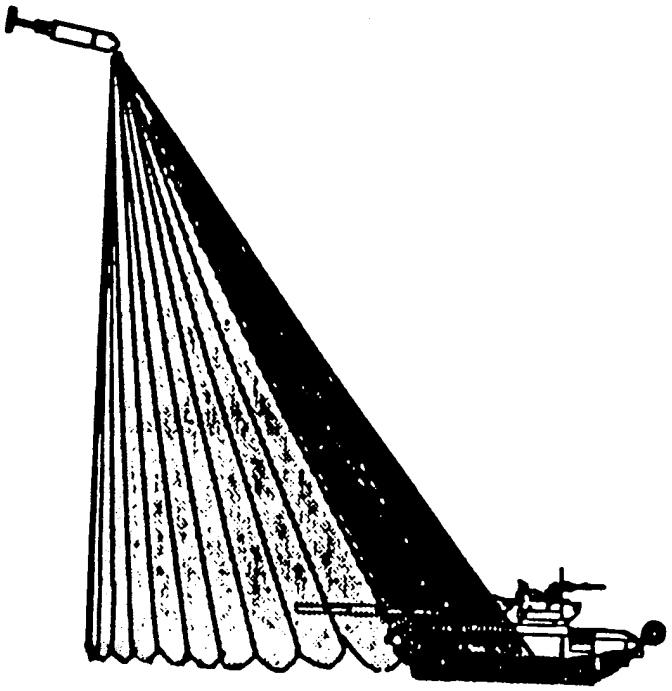


Figure 5
Forward looking radar

Down Looking Sensor will look down at the target and determine the best time to fire the warhead.



Fire Warhead

Figure 6
Warhead firing

BOARD 3/4 LAYOUT

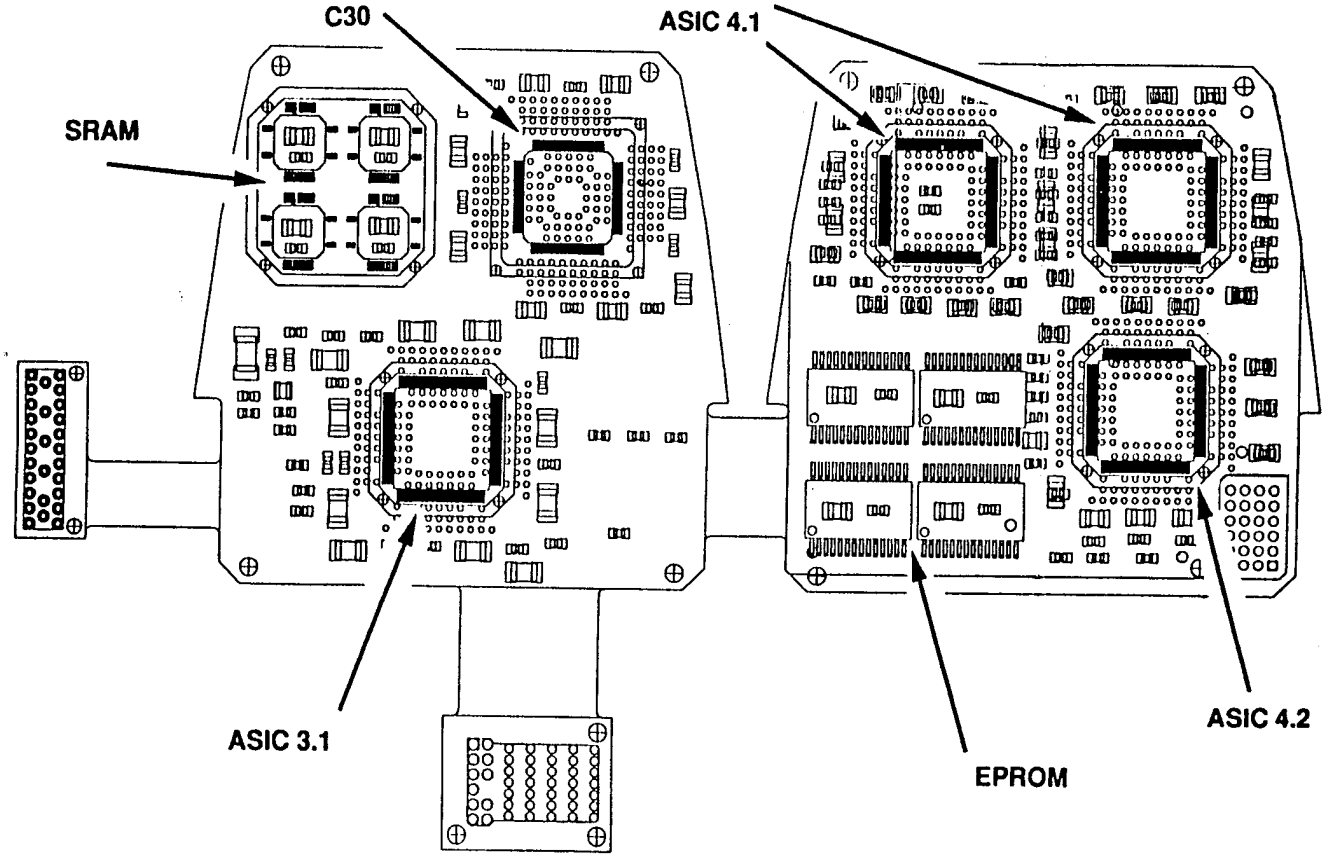


Figure 7
STAFF electronics layout

PROCESSOR

Processor Hardware Block Diagram

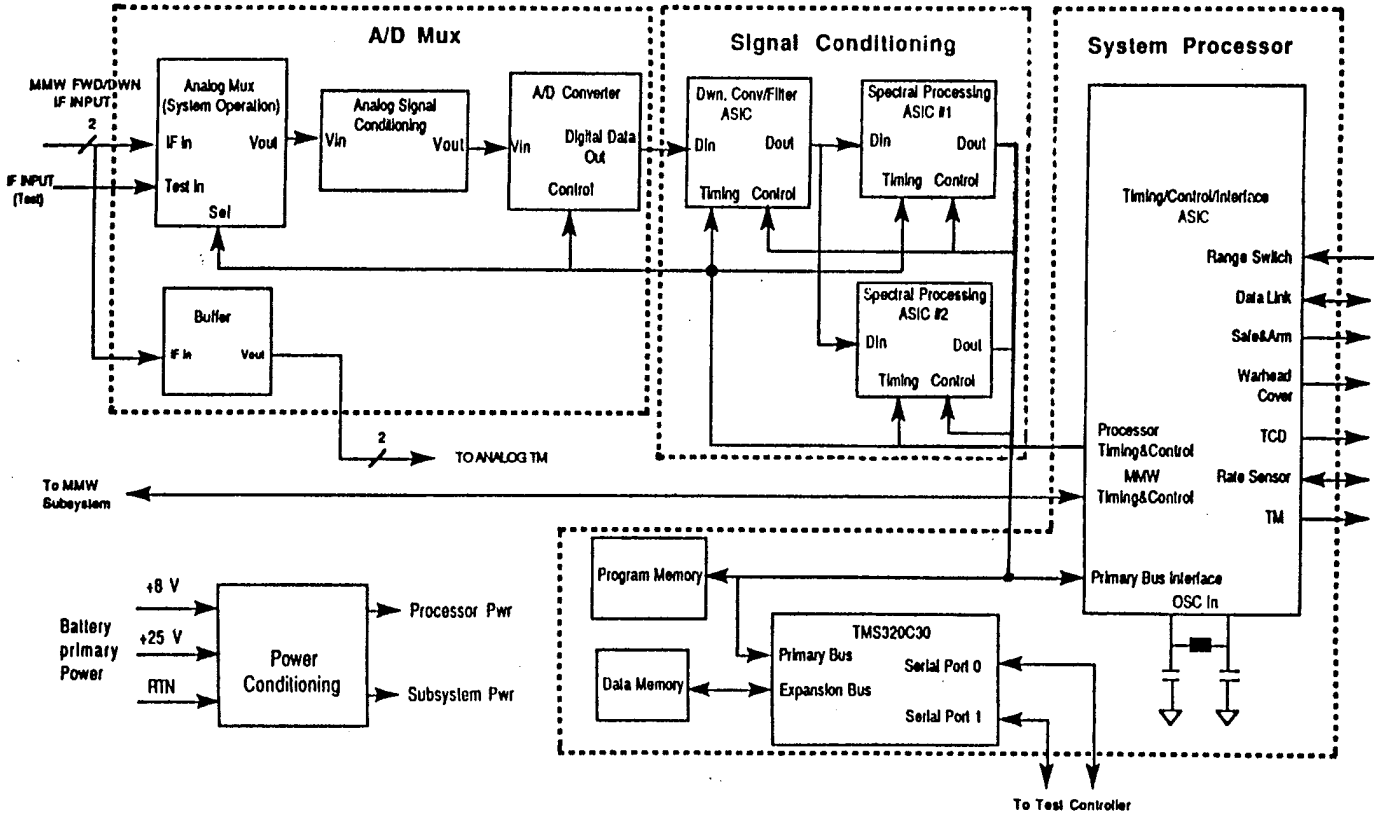


Figure 8
STAFF system processor

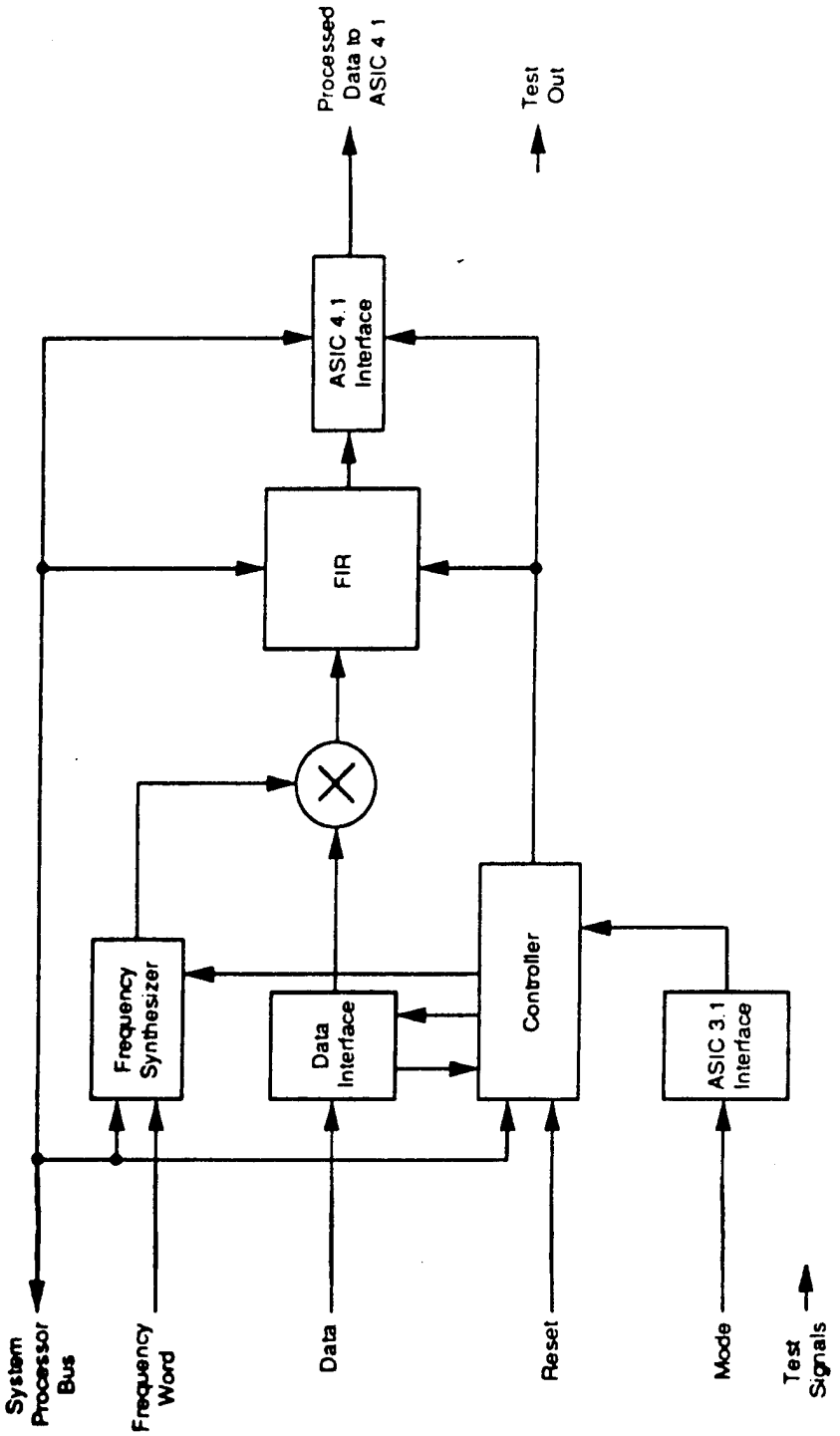


Figure 9
ASIC 4.2

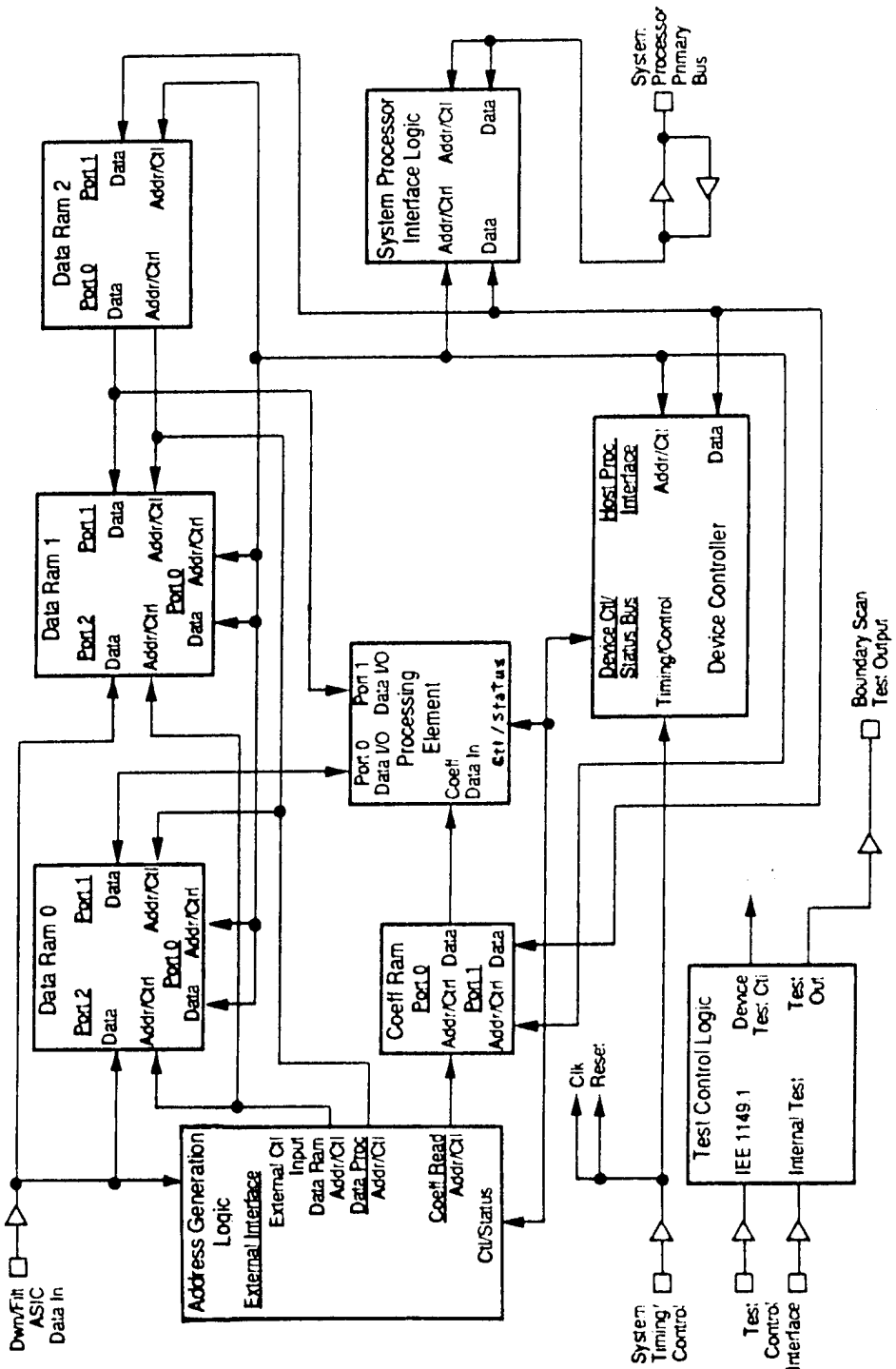


Figure 10
ASIC 4.1

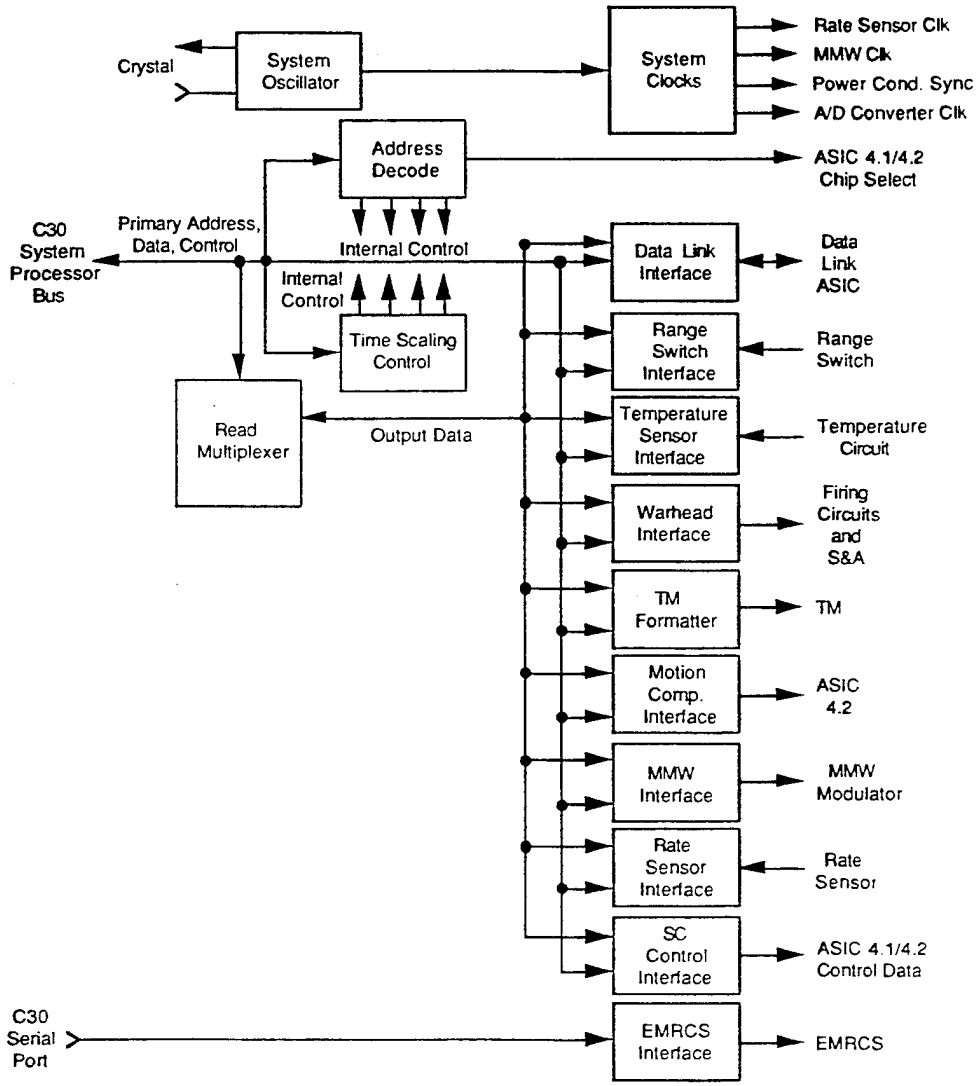


Figure 11
ASIC 3.1

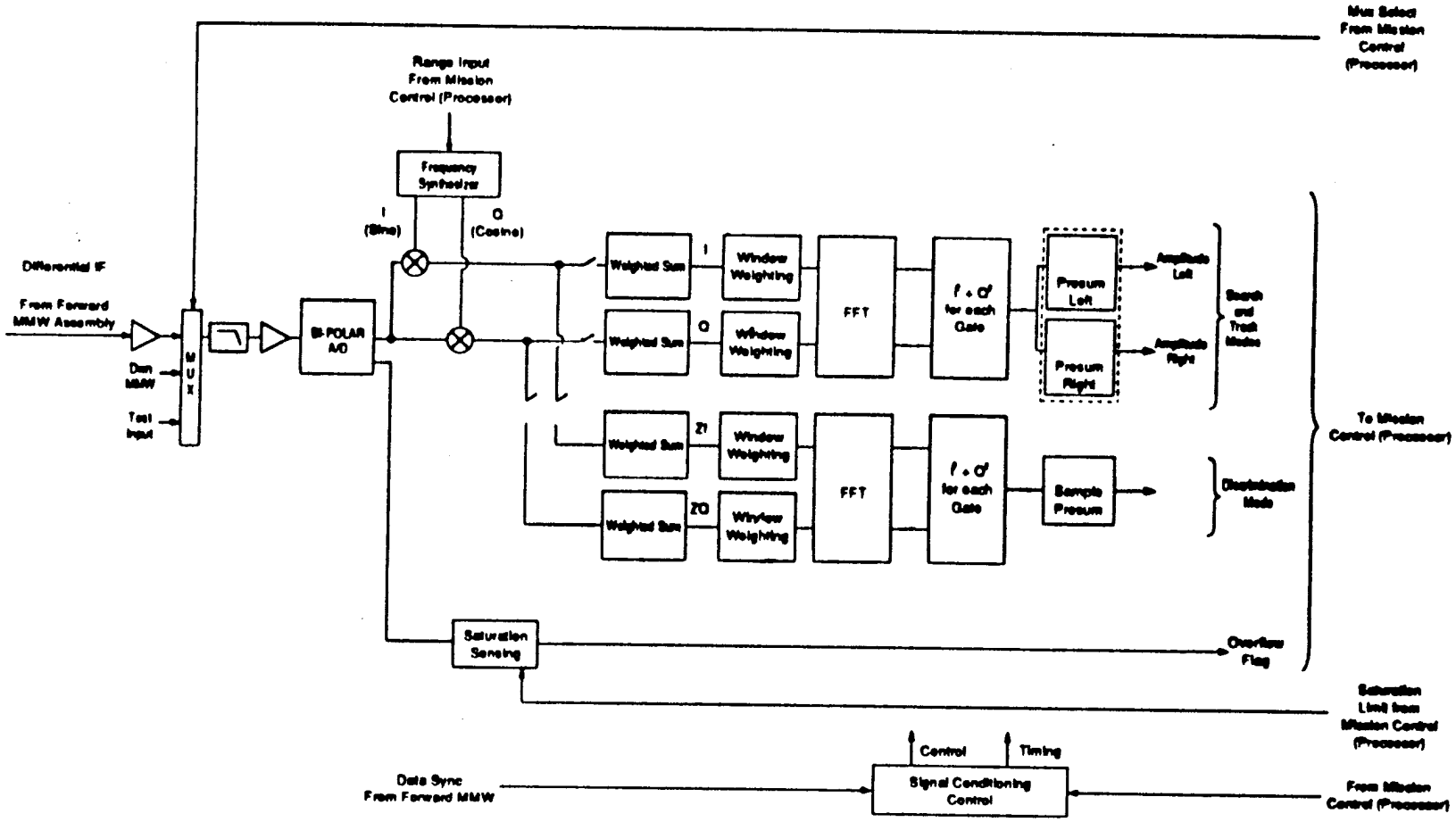


Figure 12
Search and track, and discrimination modes processing

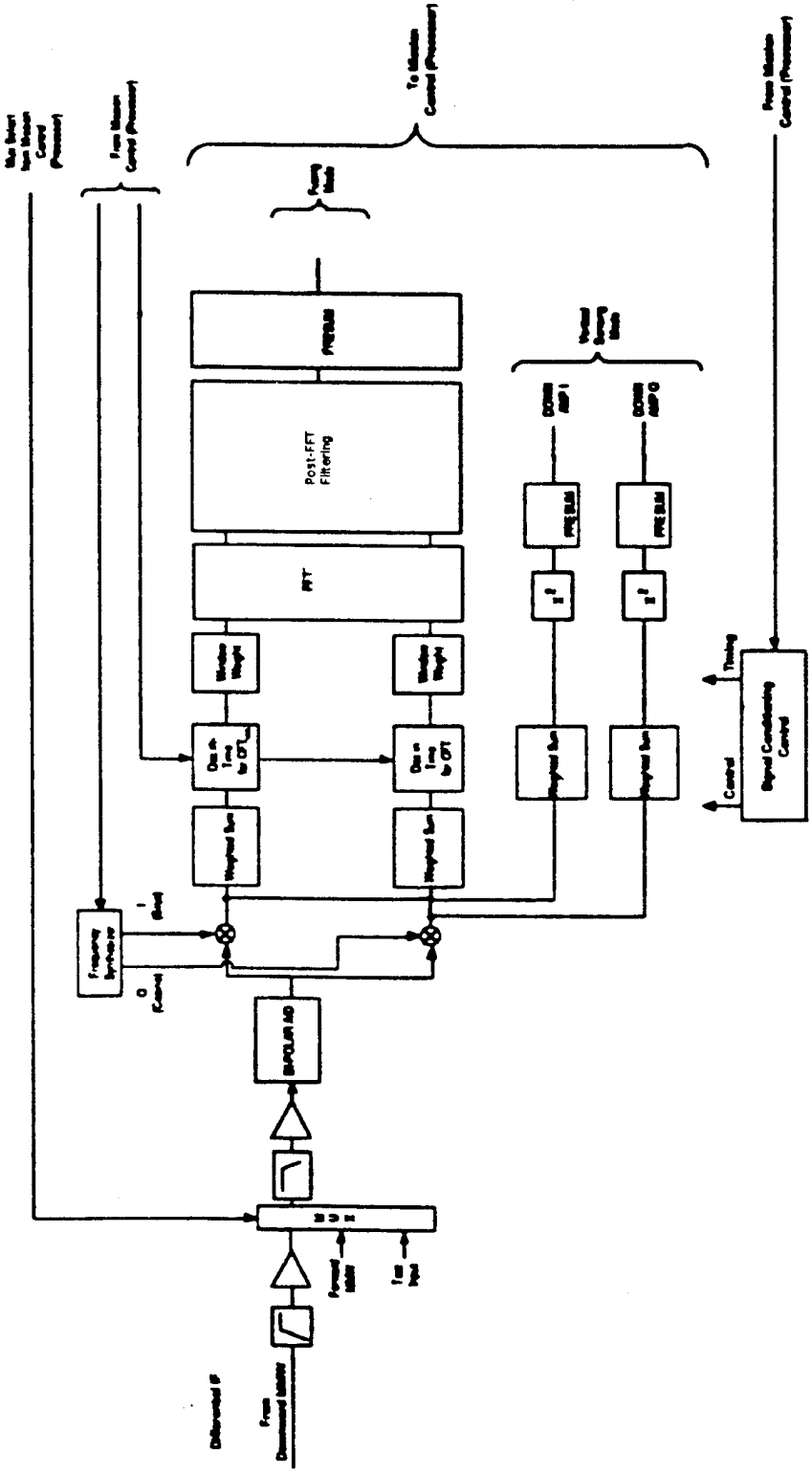


Figure 13
Fuzing and vertical sensing modes processing

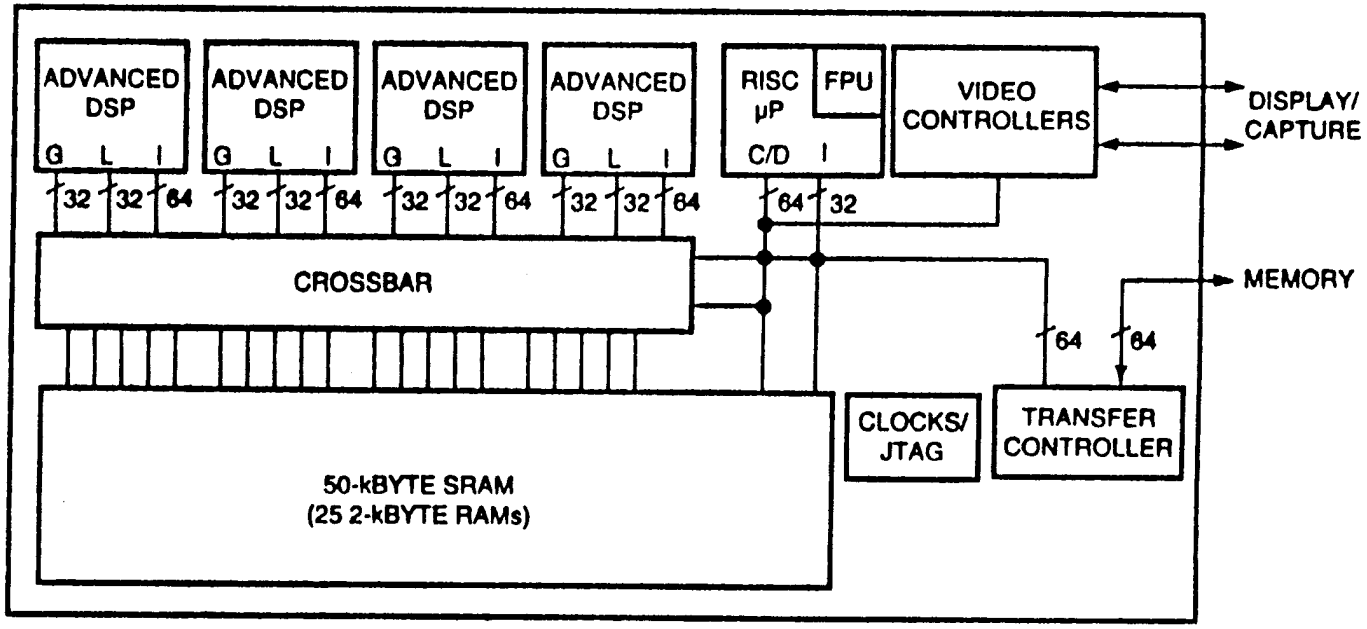


Figure 14
Texas Instruments TMS320C80 multiprocessor

Table 1
MFLOPS for ASICS 3 .1, 4 . 1 and 4 . 2

	ASIC No.		
Mode	3.1	4.1	4.2
Search & Track	12.1	9.6	38.8
Discrimination	11.2	5.3	39.4
Fuzing	11.0	4.5	39.6
Vertical Sensing	10.1	1.0	39.5

Table 2
DSP parameter comparison

	TI C30	TI C40	ATT DSP320	AD 21020	MOT 96002	ATT 3210	INTEL i860	NS SF680	TI C80
Clock speed (MHz)	33	50	40	25	40	67	50	50	50
Instruction cycle (ns)	60	40	80	40	50	60	20	20	20
MAC cycle (ns)	50	40	80	40	50	60	20	20	20
Accumulator size (bits)	40	40	40	80	96	40	64	64	64
FP formats (bits)	32,40	32,40	32	40	32,44	32	32,40	32,40	32
Registers (no)	28	34	26	12	34	26	48	32	207
RAM memory (KB)	2-1	2-4	1	0	2-4	2-4	16	1	25-2
ROM memory (KB)	4	0	2	0	1	0	0	0	0
Program memory (KB)	.256	.512	3-2	0	4	0	16	4	25-2
External buses (no)	2	2	1	2	2	1	1	1	2
Internal buses (no)	4	5	1	2	8	1	1	1	2
Off-chip fetch (no cy)	1	.5	.5	1	1	.5	2	2	1
Pipelined MAC (no cy)	1	1	2	1	1	2	2	2	1
Max parallel oper (no)	7	11	7	7	10	9	7	4	15
Instructions (no)	135	135	90	63	133	63	98	58	
Floating pt div (ns)	1560	360	880	300	300	660	300	620	
Interrupt res (no inst)	3	4	3	3	6	3	24	16	
1024-point FFT (ms)	3	1.025	2.9	.77	1.047	1.9	.76	1.025	
Interrupts (no)	4	4	6	5	3	6	1	15	4
DMA channels (no)	1	6	3	0	2	2	0	2	5
Serial ports (no)	2	0	1	0	0	1	1	1	0
Parallel ports (no)	0	0	1	0	0	1	0	0	0

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