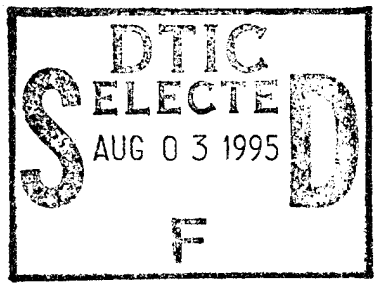
Complementary 2-D MESFET for Low Power Electronics

Interim Report # 4

Air Force SBIR Phase I
Contract Number: F33615-95-C-1679

July 31, 1995



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(AirForce SBIR Contract F33615-95-C-1679)

Phase I Interim Report #4

As detailed in the Phase I proposal, the project has four major tasks. These are 1) assessment of the p-channel 2-D MESFET device fabrication, 2) development of a p-channel 2-D MESFET model and implementation of the model into AIM-SPICE, 3) circuit simulations of complementary 2-D MESFET circuits using AIM-SPICE and comparison with conventional circuits, and, 4) analysis of manufacturability and technology insertion issues. This report summarizes progress in each task area through 28 JUL 95.

Task 1: Assessment of p-Channel Device Fabrication

The assessment of the p-channel 2-D MESFET device fabrication is underway. Heterostructure modeling of a prospective AlGaAs/InGaAs/GaAs structure was completed and an order was placed for growth of the wafer. The wafer is scheduled to be delivered in mid-August. Fabrication of p-channel devices fabrication will begin in August/September.

Task 2: Development of p-Channel 2-D MESFET Model

The preliminary p-channel 2-D MESFET model has been implemented into AIM-Spice and is presently being used to simulate discrete p-channel 2-D MESFET *I-V* characteristics as well as complementary 2-D MESFET logic circuits (see below). The p-channel device model uses a lower Schottky barrier height (typically 0.6V) compared with that of the n-channel device (typically 0.8 V). Also, the hole mobility has been set to 1000 cm^2/Vs, consistent with the observed trend of enhanced electron mobility in the n-channel devices.

Task 3: Complementary 2-D MESFET Circuit Simulations

Circuit simulations of complementary 2-D MESFET circuits are underway. In Fig. 1, we show the dc transfer characteristics of the complementary 2-D MESFET inverter at room temperature using the n- and p-channel device models implemented in AIM-Spice. The simulations predict excellent low power switching behavior including a noise margin of 0.23 V and voltage gain of 10 at a supply voltage of V_{DD}= 0.6 V. While the use of this low V_{DD} value leads to good dc switching behavior, it may be necessary to increase the supply voltage in order to achieve high speed performance. We are looking at ways to reduce the p-channel leakage current and thereby permit higher supply voltages, if that should prove necessary. Power-delay simulations of all of these circuits are underway.

Task 4: Manufacturability and Technology Insertion Issues

This task will be summarized in the Final Report.

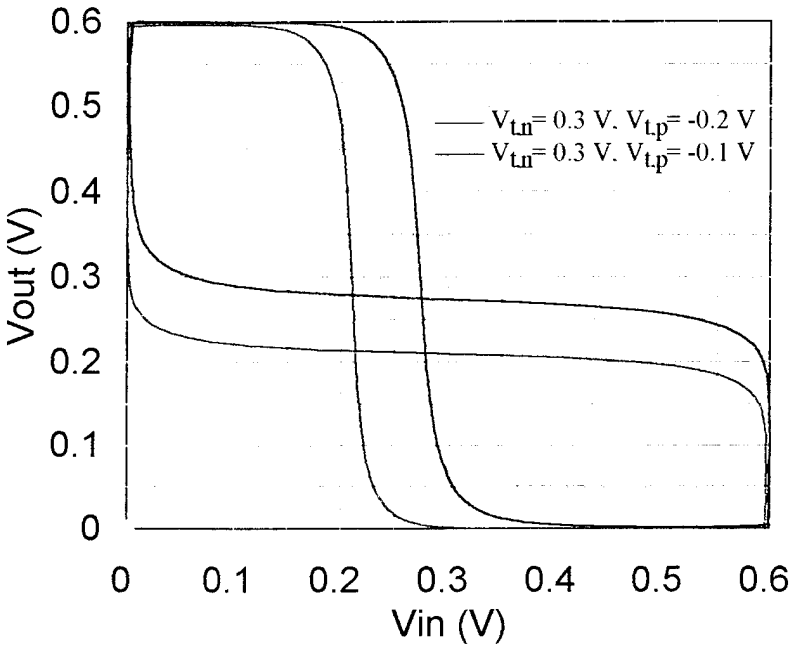

Fig. 1. Complementary 2-D MESFET DC inverter characteristics for two different p-channel threshold voltages at V_{DD} = 0.6 V. Both inverters have noise margins of above 0.2 V and voltage gains of about 10.

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