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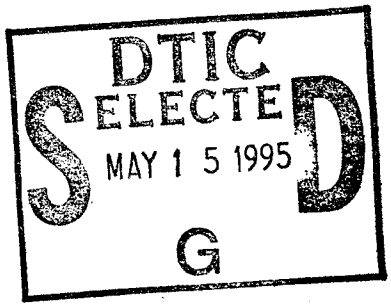
OPTICAL INTERCONNECTS FOR 3D COMPUTER ARCHITECTURES

Franz Haas, Capt, USAF; David A. Honey, Major, USAF; Harold F. Bare, LtCol, USAF



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13. ABSTRACT (Maximum 200 words)

This report details a novel approach for integrating optical interconnects into Air Force computer systems to increase system performance. Computer systems from the average personal desktop models to specialized supercomputers are limited in performance by the electronic wiring used to transport information between processing circuitry. Using light instead of electronics to transport information inside a computer can greatly increase overall system operating speed. A modular optical interconnect architecture was designed and demonstrated which is applicable for use in a variety of computer architectures (multichip module or wafer scale integration). The interconnect scheme uses a diffractive optic to image an array of light emitting diodes (LEDs) on one board to a corresponding array of photodetectors on a second board. This optical solution can replace 16 electronic wires running between the two boards.

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ABSTRACT

Computer systems from specialized supercomputers to the average personal desktop models are limited in performance by the electronic wiring used to transport information between processing circuitry. The processing "speed limit" inside a chip is much faster (greater than 100MHz) than the corresponding data rates capable for chip-to-chip communications (typically less than 60MHz). The limitation is a factor of the impedance of long electronic wires. Information pathways can be broken into two groups, those that connect computer chips on a single board (in-plane) and those that connect chips on separate computer boards (plane-to-plane). This segregation of interconnect types is important because radically different technologies are being applied to address each issue.

In-plane interconnect speeds are greatly increased by a shift to smaller computer boards called multichip modules (MCMs). The reduced distance between processing chips and the use of fine wires in the interconnects create an extremely fast interconnect technology. A complete computer system, however, would require a number of MCMs with communication pathways connecting each module. Electronic wiring is currently used for this plane-to-plane interconnect. Due to the long distances and thick wires needed for mechanical stability, the electronic solutions do not meet the speed and manufacturability requirements that are desired in this new computer package. The use of light as the transmission medium in the plane-to-plane interconnect application looks promising because there are no impedance limited data rates associated with optical interconnects.

This report details the accomplishments of the first year of effort of RL/OCPB's in-house commitment to develop optical interconnects for Air Force computer systems. A modular architecture was designed and demonstrated which is applicable for use in a variety of board technologies (multichip module or wafer scale integration). The interconnect scheme uses a diffractive optic to image an array of light emitting diodes (LEDs) on one board to a corresponding array of photodetectors on a second board. This optical solution can replace 16 electronic wires running between the two boards. The following report details the architecture, component design and testing as well as system integration and performance.

ACKNOWLEDGEMENTS

The diffractive optic design and fabrication was conducted predominantly by Dave Mikolas of Cornell University. A more complete description of the diffractive optic research can be found in the Rome Laboratory Final Technical Reports RL-TR-93-116, "Free space vertical optical interconnect using reflective binary optic focusing gratings and arrays of LEDs and photodetectors" by H. Craighead, D. Mikolas, F. Haas, D. Honey, and H. Bare; and RL-TR-93-167, "Development of a vertical optical interconnect" by D. Mikolas, and H. Craighead.

The light emitting diodes (LEDs) described in this report were designed and fabricated by Harold Bare and David Honey. The photodetector arrays were designed and fabricated by Franz Haas. All devices were fabricated using the cleanroom facilities at the National Nanofabrication Facility located at Cornell University by the above mentioned researchers. All device testing and system integration was performed at the Rome Laboratory Photonics Center.

OPTICAL INTERCONNECTS FOR 3D COMPUTER ARCHITECTURES

I. INTRODUCTION

This work is in response to current and future intra-computer data transmission needs. Present computer operating speeds are limited primarily by chip-to-chip and board-to-board communication rates.[1] The goal of this in-house effort was to develop the technologies for a high data rate computer bus to alleviate this bottleneck. To achieve this goal we have identified the current interconnect limitations, determined an appropriate computer platform to apply a high speed interconnect, designed a new bussing scheme which would alleviate the current interconnect limitations, and we have demonstrated this scheme.

Discussions with RL/OCTS personnel who are involved in high performance computer development for specific Air Force needs lead to the following conclusions: 1. the limitation of electronic on-board and board-to-board communication rates is primarily due to the high parasitic capacitances of long, thick wires or metalization runs, 2. board-to-board electronic interconnects are also limited in packing density and total number of interconnects, 3. in specific architectures requiring massive numbers of interconnects, the main limitation with electronic interconnect solutions is power drain, 4. the on-board chip-to-chip data transmission rate limitations has been partially alleviated by the advent of the multi chip module (MCM) as a replacement of the computer board.

The computer platform chosen for our interconnect demonstration was a multi-layer MCM structure. MCMs are currently being used throughout the DoD due to their high reliability, durability under extreme environmental conditions, and their small size.[2] The commercial world is also migrating to the MCM platform for its high speed, low power drain, and potential for low life cycle costs.[3] A few multilayer MCM designs have been implemented to date.[4] We anticipate more military and commercial applications will require a stacked MCM architecture for a high level of processing power in a small and durable package. Our interconnect research is focused on providing the following functionalities to a stacked MCM package: 1. a high data rate board-to-board communication bus, 2. a small footprint per channel through the use of source and detector arrays and micro-optics, 3. a modular component design capable of easy insertion into a variety of MCM packages, and 4. ease of fabrication of all components through the use of standard substrates and standard processing techniques.

Optical interconnects were chosen as an alternative to traditional electronic interconnects due to the potential for extremely high (>1GHz/channel)[5] data rates. Photons traveling through free space or waveguides (i.e. fibers or lithographically defined polymer

waveguides) do not experience the impedance that is present in electronic interconnects. This means that the interconnect medium is no longer the limiting data rate bottleneck. Optical sources and detectors can be modulated at high data rates, they can be arranged in arrays for parallel bussing schemes, and have varying degrees of integrateability with traditional electronics. Most optical interconnect schemes are facilitated by the move to MCMs because of the potential for placing specialized optical source die (typically GaAs) right next to a traditional silicon processing die.

II. THE ARCHITECTURE

The optical bus under development consists of arrays of optical sources on one MCM transmitting 16 channels in parallel to an array of photodetectors on a second MCM (see Fig. 1). Consistent with current and expected computer development, all active components (circuits requiring power, ground and electronic signal) are placed on the top side of the MCMs. In order to transmit light from the top of one MCM to the top of a second MCM, a hole is made in the second MCM. A single diffractive optic element (DOE) placed above this hole reflects, redirects, and focuses the light from the optical sources to the photodetectors. This type of interconnect is called "freespace" because no waveguide is used to control the light propagation.

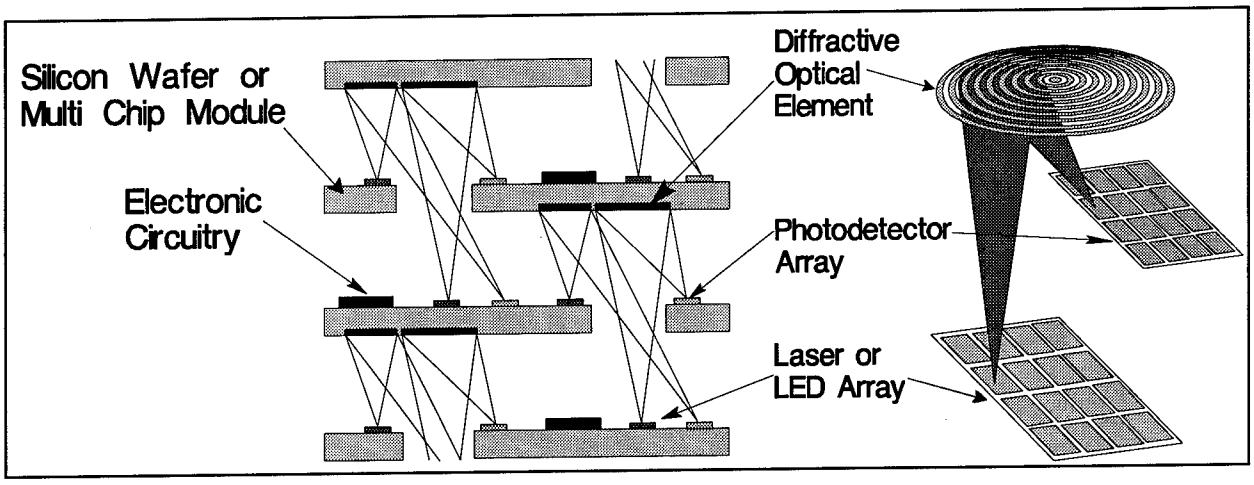


Figure 1. A plane-to-plane 16 channel optical interconnect using a diffractive optic element (DOE) to focus and redirect the light from an array of light emitting diodes (LEDs) to an array of photodetectors.

Given the freespace nature of this interconnect and the need for accurate placement of the three components (source array, detector array, and DOE), a level of alignment tolerance was engineered into the architecture. By making larger detectors, the "target" that the source image must hit is greater giving a greater tolerance to initial component placement errors or image drift due to environmental changes. The individual sources and detectors should be spaced to accommodate the required "target" size. One-thousandth of an inch (or 1.0mil = 25.0microns) of misalignment tolerance in the X and Y axis of the image on the photodetector was chosen as a realistic tolerance given the capabilities of standard die placement machines. The DOE is optimized for focusing light from the center of the source array to the center of the detector array. As source/detector pairs are located farther from the center of the arrays, the imaging of the DOE deteriorates contributing to optical crosstalk. The target area and imaging ability of the DOE therefore limits the possible number of channels per array. 16 channels (see component design sections for device sizes and spacings) were found to be within the focusing capabilities of the 1.1mm diameter lens designed for the demonstration.

Each component of this interconnect, the LED arrays, photodetector arrays, and the DOE were fabricated at the National Nanofabrication Facility (NNF) at Cornell University by Rome Laboratory engineers and Cornell staff under an ES&E contract with the Photonics Center. The NNF is a National Science Foundation funded "Open Learning Laboratory". Devices were tested and integrated into a demonstration system at the Rome Laboratory Photonics Center. Device design, fabrication, testing and integration details follow in this report.

III. THE COMPONENTS:

III. A. DIFFRACTIVE OPTICS

As the name implies, diffractive optics use the physical property of diffraction to control the propagation of light through or the reflection of light off the lens. The "diffractive structures" of a DOE are mathematically defined to perform a certain lensing function. In the architecture presented here, the function is to focus light from an array of light sources on one computer board (MCM) to an array of detectors on a second computer board. The location of the source and detector arrays relative to the center of the diffractive optic and the LED wavelength were variables in the lens calculation formula. The image of the source incident on the detector is demagnified by a factor of 0.5.

The DOE designed, fabricated, tested and integrated into our demonstration was a four level, off-axis, reflective diffractive optic shown in Fig 2. The diffractive pattern was etched in Si using two masking steps. Si wafers are inexpensive and silicon processing is very well understood. We were able to design and fabricate a 1.1mm diameter, reflective, diffractive optic device that performed a complex function at much lower costs and in

shorter time than we could procure a traditional reflective mirror (assuming that it was possible to fabricate a bulk optical device of this size with such a complex focusing functionality).

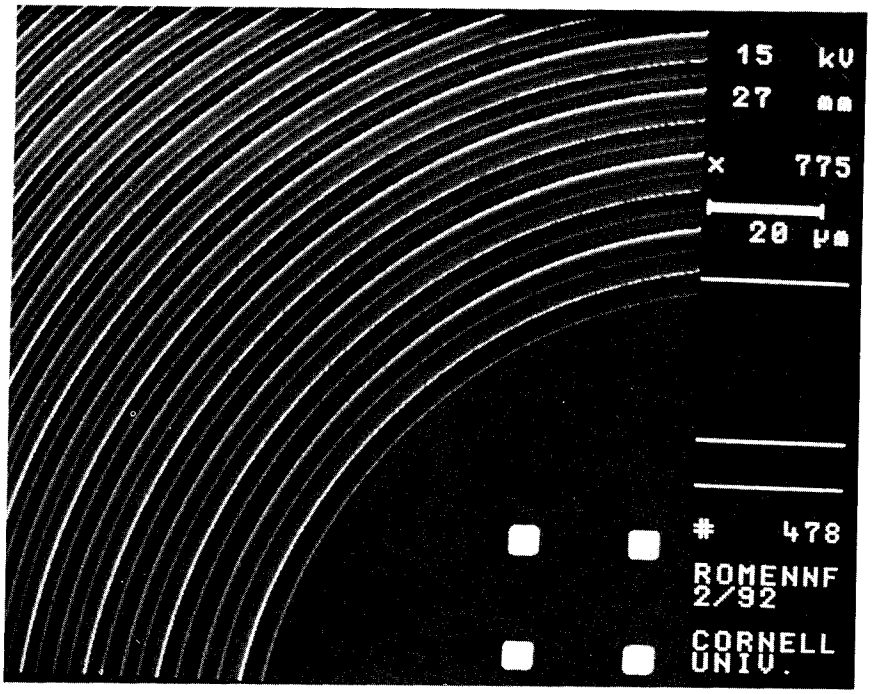


Figure 2. Scanning electron micrograph of 4-level focusing diffractive optic elements.

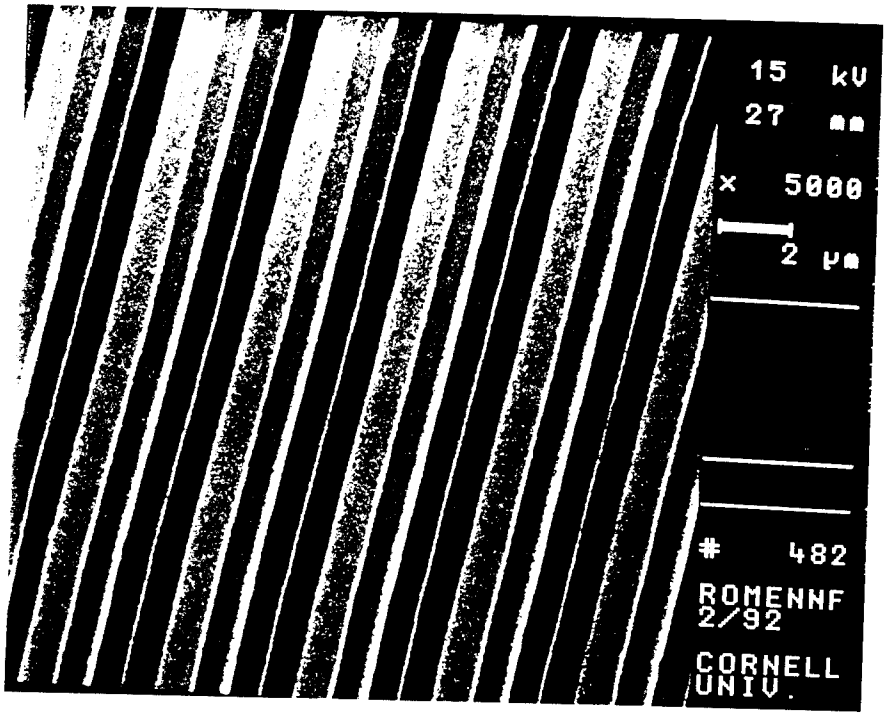
III. A. i. DESIGN

To understand the principles behind the design of focusing DOE's, it is helpful to first look at linear gratings (see Figure 3.a.). A beam of monochromatic light incident on the linear grating will be diffracted into a number of beams of light called "orders" each at a certain angle from the incident angle (see Figure 3.b.). The angle of diffracting orders is defined by the grating equation:[6]

$$a \sin \theta_m = m\lambda$$

Here a is the period of the diffractive structures, θ_m is the angle of diffraction of the mth order, and λ is the wavelength of light. In our architecture, the optical interconnect is established using the first diffracted order. By varying the period of the linear grating we can change the direction that each order diffracts off the grating. We can optimize the amount of light in the first order by varying the diffractive structure pattern.

a)



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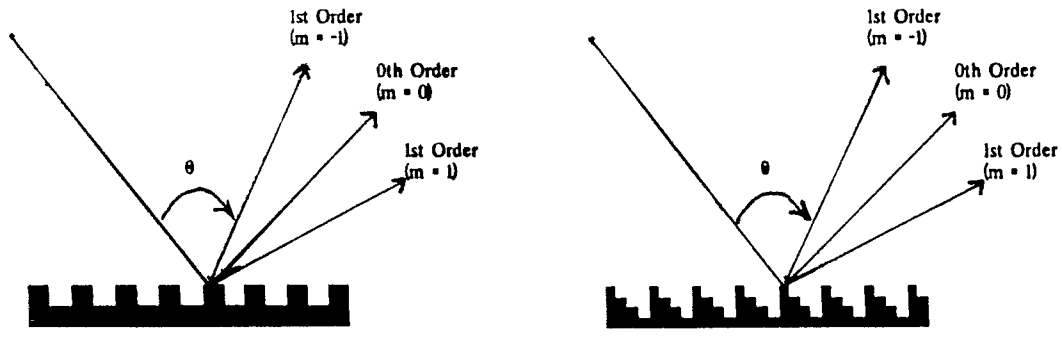


2 Level DOE

4 Level DOE

Figure 3. a) SEM of a linear diffraction grating, and b) the diffracted "orders" off the linear grating.

Figure 2 shows a focusing DOE. To understand how this lens operates, look at a small section of the DOE and notice the comparison with the linear grating. The focusing DOE can be thought of as a locus of adjacent linear gratings with a variable period that gets smaller as the diffractive structures go farther from the center of the lens. Mathematically, each curve of the lens represents a line of equal phase for light traveling from a source at a known location to a detector at another known position. At every fractional (as defined by the DOE designer) change in the phase of the reflected (or transmitted) light, a new curve is defined. The more fractional steps used to define the lens, the closer the DOE approximates a blazed lens with a continuous slope. As shown in Figure 4, the more steps in the diffractive pattern, the greater the "efficiency" (the percentage of light in the first order at the design wavelength) of the grating.

$$E = [\sin(\pi/2^m) / (\pi/2^m)]^2$$

# of Masks (m)	# of Steps	Efficiency (E)
1	2	41%
2	4	81%
3	8	95%
4	16	99%

Figure 4. The relationship between number of steps in a diffraction pattern and theoretical diffraction efficiency.[7]

The DOEs used in our demonstration were defined using a software package called FREDD (Fresnel Diffractive Device) which was written by Dirk Brown of Cornell University with adjustments by Dave Mikolas.[8] This program is hosted on a Macintosh computer and defines the continuous phase patterns of a DOE given the placement of a source and detector in three dimensions relative to the center of the DOE, the wavelength of light used, reflective or transmissive operation, the number of phase "rings", and the number of sides to the elemental fractured cell of the curved diffractive structures (more sides gives a more accurate approximation of the ideal lens at a cost of longer computational and e-beam exposure time). The data from the FREDD program was transferred to the Cambridge e-Beam lithography control computers for exposure of the DOE design onto Si wafers coated with e-Beam resist.

III. A. ii. FABRICATION

Four level off-axis reflective DOE's were fabricated in silicon (Si). Photo and e-beam lithography were compared as methods of defining the diffractive structures. Photolithography is an industry standard due to its low cost and quick turn around times. E-beam lithography, though much more expensive, offers the capability to define very small structures across a large area with a high degree of alignment accuracy. In both cases, reactive ion etching (RIE) was used to etch the diffractive patterns into the Si substrate.

III. A. ii. a. PHOTOLITHOGRAPHY

The photolithography process entails the fabrication of a mask or reticle which is placed in a projection exposure system which transfers the pattern on the mask to a resist coated substrate. To generate the mask, a resist coated chrome-on-quartz mask blank was exposed with a 10X enlargement of the DOE pattern using a GCA MANN 3600 Pattern Generator. The mask was developed for 60sec in a 1:1 solution of MF-312 and deionized H_2O. The chrome was etched for 70-80sec in standard chrome etchant (ascetic acid). The remaining resist left on the mask was etched for 5min in an O_2 atmosphere in a Plasmatherm-72 RIE.

Three inch Si wafers were prepared for the photolithography exposure by an initial primer of 20%HMDS in PGMEA. The primer coated wafers sat for 10sec before being spun dry at a rate of 3000rpm for 30sec. KTI 895i (16.5cs) photoresist was applied and spun at 35000rpm until dry giving a 1.3μm thickness. The wafers were subjected to a 60sec hot plate post bake at 90°C. A GCA MANN DSW 4800 10:1 Stepper was used to expose the prepared wafers. Exposure times varied from 1.2 to 1.5sec depending on the mask and the exposure tests taken before the final exposure. The wafers were then developed in KTI 945 for 90 to 120sec. The pattern of the DOE in the photoresist was transferred to the substrate using a Plasmatherm-72 Reactive Ion Etcher. The Si was etched to a depth of 160nm in 2.4min in a CF_4 atmosphere (29.4sccm) with 175W of applied RF and a bias of 450V at 40mTorr.

III. A. ii. b. E-BEAM LITHOGRAPHY

In e-beam lithography there is no intermediate exposure mask. The pattern is written directly onto a resist coated Si wafer by a focused electron beam under computer control. This process takes much more time than the bulk exposure process of photolithography especially when many structures across a large area need to be exposed. However, the extremely small structures that the e-beam can resolve and the precise alignment control of the e-beam itself coupled with extensive calibration and substrate alignment techniques makes this process superior for defining high performance DOE's.

One of the challenges in DOE fabrication is generating extremely small structures in close proximity to each other. E-beam lithography has been successfully used in the commercial world to define sub-micron transistor gate metalization masks, but these devices are typically isolated from other e-beam exposures by relatively large distances. The e-beam itself has a Gaussian power profile. When two e-beam exposures are close to each other, the Gaussian tails overlap causing an overexposure and subsequent "blooming" of the final structures (see Figure 5). As the diffractive features get smaller towards the outside of the lens, this blooming error will increase resulting in a lower diffraction efficiency and increased optical crosstalk.

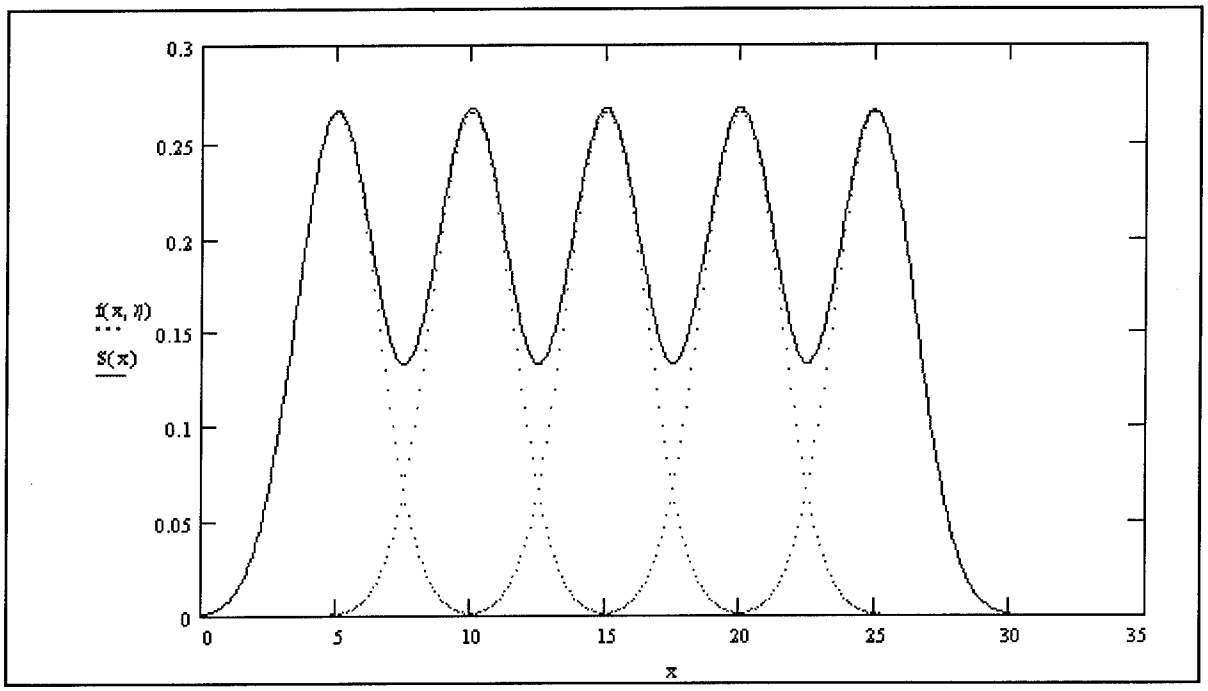


Figure 5. Overlapping e-beam gaussian exposures. The solid line represents the net exposure recorded in the e-beam resist.

Empirical e-beam dose (the level of electron current supplied to the substrate) versus resist exposure tests for a range of device sizes and periods were conducted. This data will be used in future DOE designs to optimize the diffraction efficiency. This data can be used to either modify the original CAD design to take into account the over-exposure as a function of structure size and period or as a guide for varying the e-Beam current dose during exposure.

Choosing a suitable mask "system" became another technical challenge when etching small features with small periods. Due to the Gaussian nature of the power distribution of the e-Beam, the resist is exposed with a Gaussian profile. To obtain an accurate design

represented in the mask for small structures with small periods, the mask must be thin or the exposure areas will overlap. A two-mask process was used to transfer the pattern from the initial PMMA (polymethel-methacrylate) e-beam resist mask to a second mask used to transfer the pattern to the Si substrate.

The fabrication of submicron structures with submicron placement tolerances across a 1mmX1mm square area requires a well designed alignment strategy. The Cambridge e-beam alignment and calibration tools were used in conjunction with multiple well placed and well designed alignment marks on the Si substrate. Four micron square, 500Å thick gold alignment marks were used on top of a 50Å chrome adhesion layer.

A more in-depth discussion of the fabrication of DOE's can be found in the Rome Lab Final Technical Report RL-TR-93-167 by David Mikolas and Harold Craighead of Cornell University.

III. A. iii. TESTING

A functional capability test was conducted to insure that the DOE would focus a 4X4 array of 50 X 50μm sources to an array of matched photodetectors as required by our architecture depicted in Figure 1. An optically flat glass plate coated with metal (Cr) was coated with resist, exposed, developed, and etched to open a 4X4 array of 50μmX50μm windows. An expanded HeNe (632nm) light beam passing through these holes replicated the array of LED emitters that were used in the final demonstration. When the mask was placed at the proper location relative to the center of the DOE, the images of the simulated LEDs were clearly focused at the point in space where the photodetector array would be placed. This was a dramatic demonstration of the functional capability of the DOE. Arrays of apertures with dimensions as small as 10μm were included on the mask and were clearly imaged by the DOE.

The test described above determined the functionality of the DOE but not a conclusive diffraction efficiency. In our continuation of this in-house effort we will establish a means of measuring the diffraction efficiency of small diameter (1mm) DOE lenses. The completed interconnect is the true "efficiency" test for the DOE - the ratio of light emitted from the LEDs to the amount of light imaged onto the corresponding photodetectors. This data will be included in the next In-House Final Report.

III. B. LED ARRAY

Four by four arrays of independently addressable light emitting diodes (LEDs) were designed and fabricated to provide sources for a multichannel board-to-board optical interconnect. LEDs were chosen as an alternative to the more recent technology of vertical cavity surface emitting lasers (VCSELs). Although a surface emitting laser is much faster (GHz vs MHz), and has a monochromatic and more powerful emission spectrum (mW vs

μW) than a homojunction surface emitting LED, operation of the LED is well understood and fabrication involves standard semiconductor materials and processing techniques. LEDs provide low cost, easily fabricated light sources which can be arranged in two-dimension arrays.

The LEDs are GaAsP homojunction diodes designed to emit visible light at 655nm. Visible light emission, ease of fabrication, and flexible device geometries were the key design parameters. Emission in the visible spectrum was important for ease of system alignment. The 655nm center wavelength also allowed for testing of the DOE with a common 630nm HeNe laser. The simple design also contributed to the >98% device yield. Figure 6 shows an individual LED and an array of 16 LEDs.

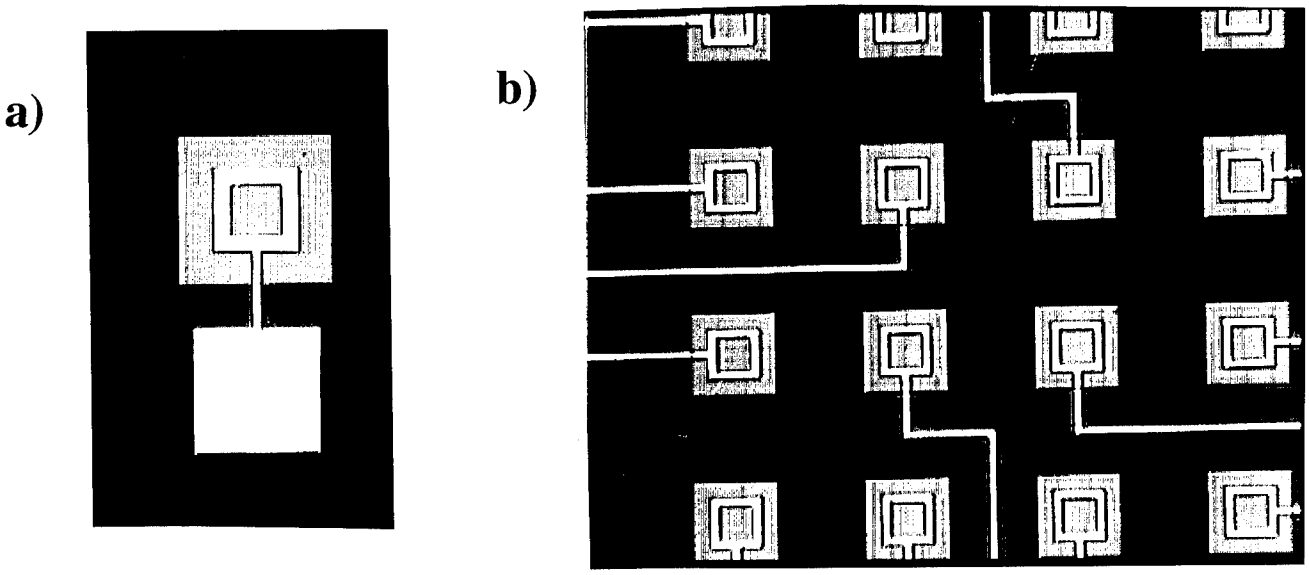


Figure 6 a) individual GaAsP LEDs and, b) an array of 16 50 X 50μm LEDs.

III. B. i. DESIGN

An LED is a forward biased pn junction that emits light through the process of radiative recombination.[9] Typical LEDs have a forward voltage drop of 1.5 to 2.5V and draw 5 to 20mA.[10] The wavelength of the emitted light can be calculated from the bandgap of the substrate by the following equation:

$$\lambda = hc/Eg$$

where λ is the emitted wavelength, h is Planck's constant (4.135×10^{-15}eVs), c is the speed of light ($3X10^{8}$m/s), and Eg is the bandgap of the substrate.[11]

The LED substrate design is composed of a GaAs substrate with a 15μm intermediate graded epitaxial layer of $GaAs_{(1-x)}P_{(x)}$:Te (where x varied from 0.0 to 0.3) and a 15μm top epitaxial layer of $GaAs_{0.7}P_{0.3}$:Te. The LED active area (region of electron-hole pair recombination and light emission) is defined by the pn-junction formed by the Te n-doped epitaxial layer and by regions of Zn p-doping. Metalization contacts annealed to the n and p regions form contacts used to bring current to the device. The Te concentration for both epitaxial growths was $0.5\text{-}3.0X10^{17}$ cm^{-3}.

Figure 7 is a computer aided design (CAD) of the LED chip layout. An array of 16 LEDs lies in each corner of the chip. All LEDs were placed on 200μm centers to match the 100μm centers of the photodetectors after the LED image is reduced by a factor of 0.5. Each array has a different active area and/or metalization pattern. Device sizes were 50 X 50μm, 100 X 100μm, and 180 X 180μm. Variations in metalization patterns were fabricated to determine the best means of adequately distributing current to the devices while limiting the amount of light that is blocked. Metalization patterns varied from a simple 5 or 10μm metal bar to three concentric 5μm wide, square rings centered in the device active area. A number of test patterns and devices are shown in the center of the chip CAD drawing.

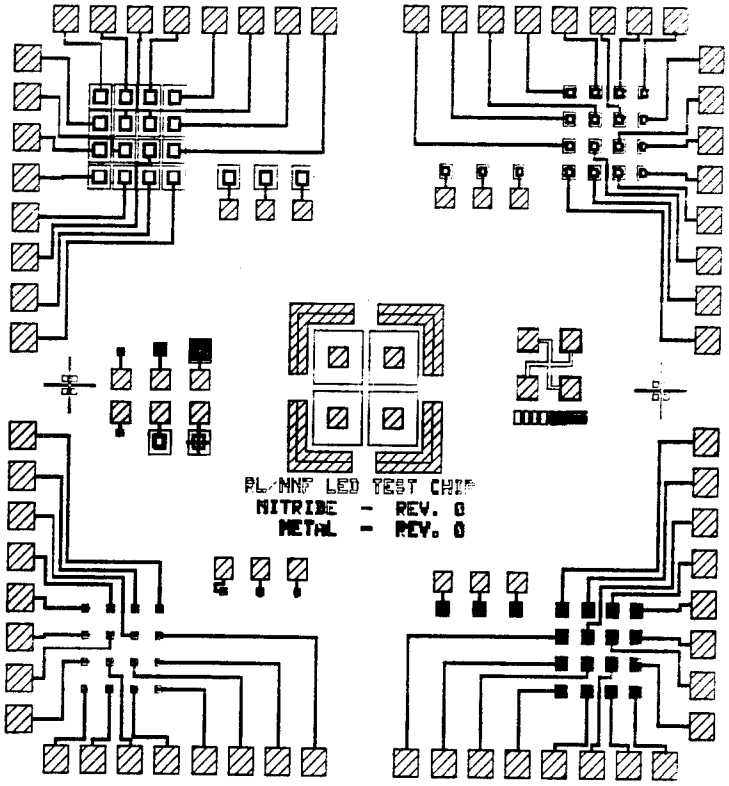


Figure 7. CAD layout of LED chip.

III. B. ii. FABRICATION

LEDs were fabricated from commercially available n-type epitaxial GaAsP on GaAs substrates. The first processing step consisted of depositing a layer of thermally grown silicon nitride. Photolithography and wet chemical etching was used to open "windows" in the silicon nitride exposing the GaAsP surface. Zn was then diffused into these window regions forming the LED active areas. A second photolithography step was then used to define the Al p-type metalization contacts. The Al contacts were annealed using two techniques described below. Next, the complete backside of the LED chip was metalized with Au-Ge to form the n-type contact and a final anneal was performed.

Rapid thermal annealing (RTA) and conventional furnace annealing were compared as techniques for developing good ohmic contacts to the p and n-type regions. Figure 8 shows the output intensity as a function of drive current for LEDs subjected to both RTA and conventional annealing techniques. Conventionally annealed devices demonstrated a higher light output as well as a more consistent performance in current-voltage and radiance-current characteristics. The RTA process is a relatively intense and sudden thermal cycle resulting in a sharp temperature gradient, and hence a nonuniform anneal condition across the wafer surface which may have contributed to the degraded performance of these devices.

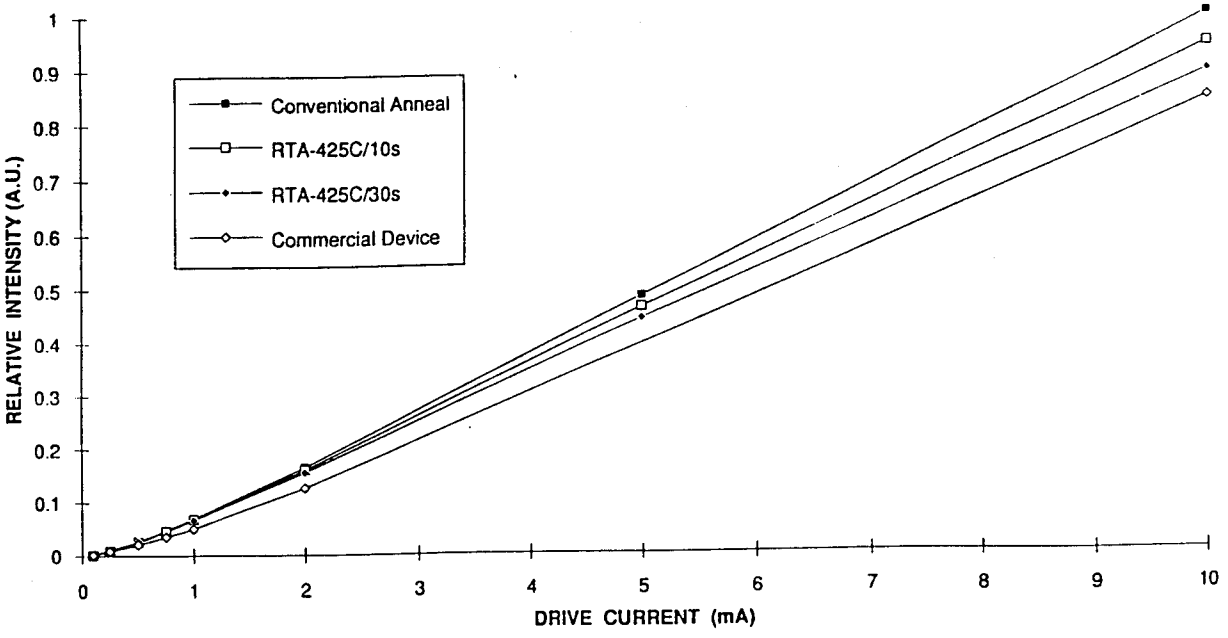


Figure 8. Relative intensity-current measurements for LED's fabricated with conventional two-step furnace anneal cycle, and two single rapid thermal anneal cycles: 425°C/10s and 425°C/30s, as well as commercially available devices.

III. B. iii. TESTING

The LEDs were evaluated electrically and radiometrically. Current-voltage measurements were made with a Hewlett-Packard 4145A Semiconductor Parameter Analyzer. A Newport 835 Optical Power Meter with an 818L Silicon Photosensor was used to monitor the LED optical power output as the device current was varied by the HP analyzer. The output spectrum of the GaAsP material was measured using an Anritsu MS9001B1 Optical Spectrum Analyzer.

In studying the effect of electrode geometry on the optical power output, no apparent difference in optical output level was observed among the various electrode patterns. Evidently, all electrode patterns examined were able to adequately distribute the electric field within a given junction area, thereby producing a similar optical output level. Upon examining the effect of junction area on optical output level, only small changes were observed for the three junction areas investigated. For example, the optical output level varied only a few tenths of a microwatt between the smallest (50 X 50μm) and the largest (180 X 180μm) junction areas at a drive current of 10mA. Hence, since electrode size and junction area did not significantly affect device performance at the desired drive current level, the smallest junction area LED (50 X 50μm) was selected to facilitate component alignment in the demonstrating interconnect scheme.

At a drive current of 10mA, the voltage drops across the elements of an array of 50 X 50μm LEDs varied from 1.87 to 1.99V while the radiance varied from 0.202 to 0.219W/cm^2-sr. Such variation is normal and acceptable for developing source arrays for optical interconnect schemes. Device uniformity is further demonstrated by the compilation of the 16 drive current vs applied voltage and radiance vs drive current plots (Figure 9.a.) for devices in a single array. Figure 9.b. shows that the radiance level transverses three orders of magnitude as the drive current is varied from 0.1 to 20mA. This large range clearly enhances the potential for a device to be effectively modulated. The optical spectrum output from the LEDs is shown in Figure 10. The spectrum has a center wavelength of 655nm with a half-power bandwidth of approximately 20nm.

Despite low light outputs, this simple source was suitable for demonstrating a novel optical interconnect architecture. These results prove the usefulness of simple, visible, surface-emitting LED arrays. Devices were quickly fabricated with the required active area size and device-to-device spacings. An abundant supply of robust light sources were at hand for insertion in a variety of optical interconnect schemes. This quick fabrication turnaround and high level of device dependability would not be possible with costly and complex vertical cavity surface emitting laser arrays.

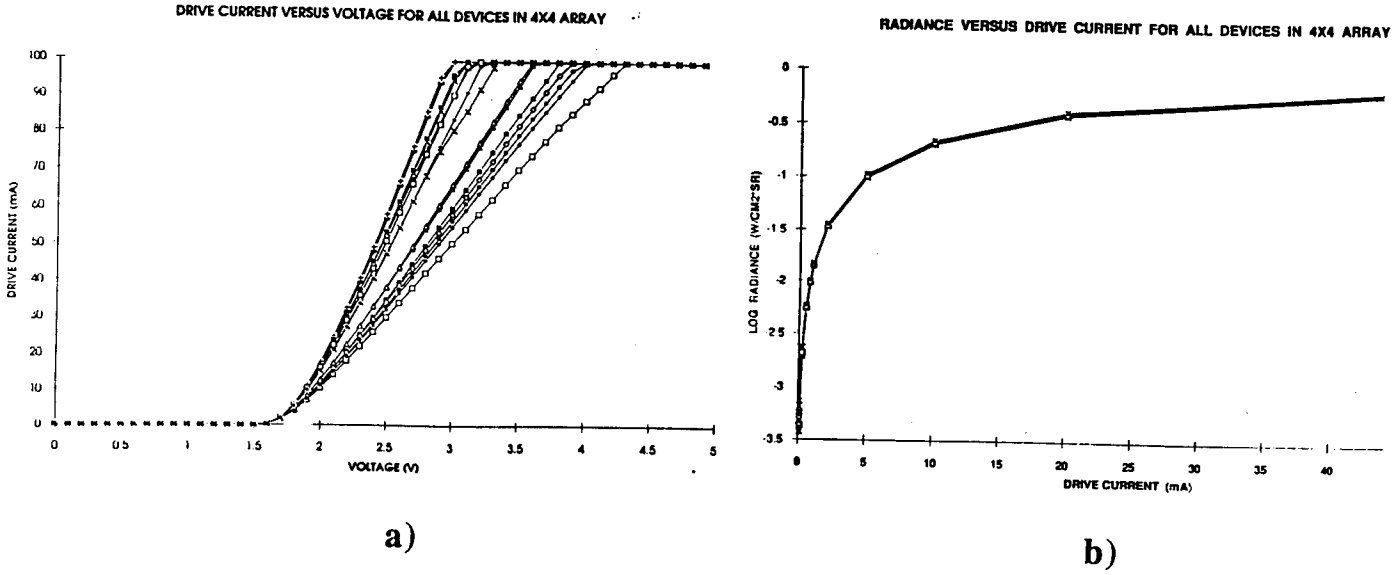


Figure 9. Uniformity of GaAsP LED's (junction area 50 X 50μm) in a 4X4 array - each symbol represents a separate device in the array: a) current-voltage measurements with 100mA compliance limit and b) radiance-current measurements.

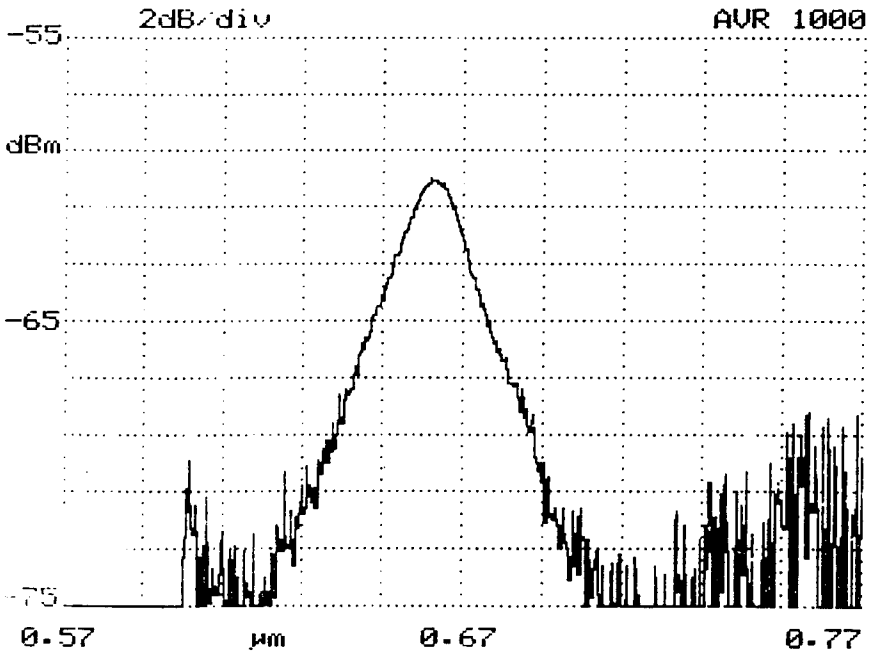
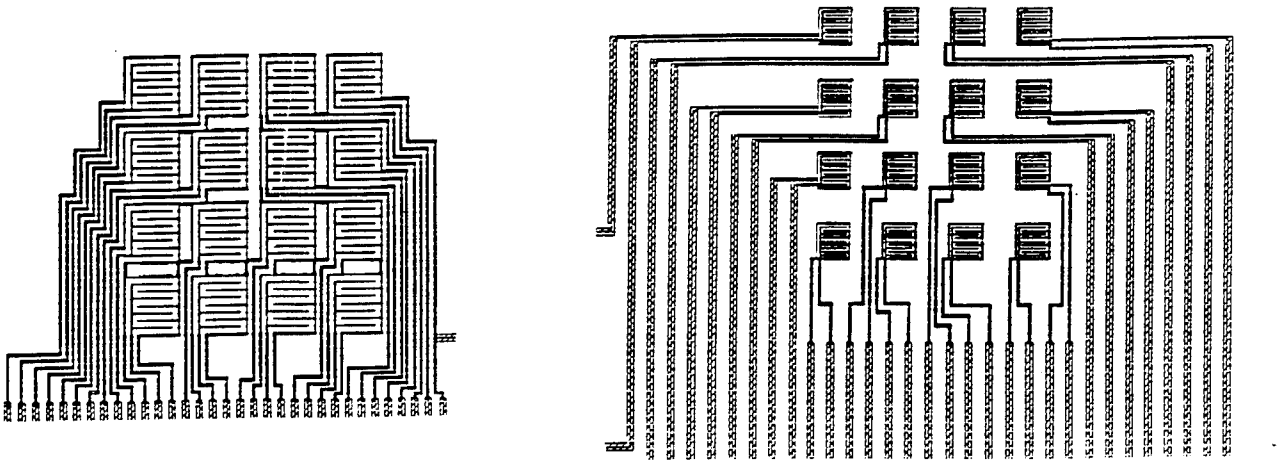


Figure 10. Optical spectrum output for an LED at 100mA.

III. C. PHOTODETECTOR ARRAY

The photodetector arrays were designed to adhere to the project goals of ease of component fabrication, the use of standard fabrication processes and materials, and robustness of design. They are metal-semiconductor-metal (MSM) photodetectors on silicon (Si) substrates. MSMs have been the focus of much recent research due to their high speed operation on both Si and GaAs.[12] Si was chosen in our application because of it's good responsivity in the visible spectrum and because it is the standard substrate for electronic circuits. The MSM design is very flexible and can easily be used in 2D monolithic photodetector arrays.

The detectors consist of interdigitated (see Figure 11) electrodes biased from0Vto 10V on a semiconductor substrate. The metal-semiconductor interface forms a Schottky rectifying contact. The two electrodes as a system form back to back Schottky contacts where one contact is forward biased and the other is reverse biased. The semiconductor area between the electrodes is depleted of free carriers due to the applied bias. A photon incident on the semiconductor will induce an electron hole pair which will be attracted to and collected by the positive and negative electrodes producing the detector's "photocurrent". Different electrode metals and metalization patterns were analyzed for optimum detector sensitivity and reduction of electrical crosstalk.



a) Shared ground layout.

b) Each detector has its own signal and ground line.

Figure 11. Metal-semiconductor-metal photodetectors in 2 array configurations.

III. C. i. DESIGN

The detectors were designed to be responsive to low levels of 655nm light, to minimize optical crosstalk from light hitting the substrate outside of the detector active area, to be easily fabricated, and to be arranged in a 4X4 array. Design parameters were substrate material, metalization geometries (most importantly electrode width and spacing), electrical isolation material and thicknesses, and choice of electrode metal.

In designing MSM photodetectors it is important to know how much light will be absorbed and converted to current within the collection depth of the biased electrodes. We can determine the amount of light absorbed vs distance into the substrate by using the following exponential relationship:

$$I_A(x) = I_{os}\,(1 - e^{(-\alpha x)})$$

where $I_A(x)$ is the amount of light absorbed in x microns of substrate given an intensity of light (I_{os}) just inside the material's surface. α is the absorption coefficient for a certain material and wavelength of incident light. The absorption coefficient for Si with incident light of 655nm is approximately $3x10^3$ cm^{-1}.[13] A plot of the intensity of light vs depth for Si and 655nm light is shown in Figure 12. The photo-generated free carrier collection depth can be approximated to the digit spacing length (5μm for the left array and 10μm for the right array). As can be seen in the absorption plot, nearly 100% absorption will take place within 1μm of the substrate surface. Therefore, for both arrays we can assume a total collection of all generated free carriers.

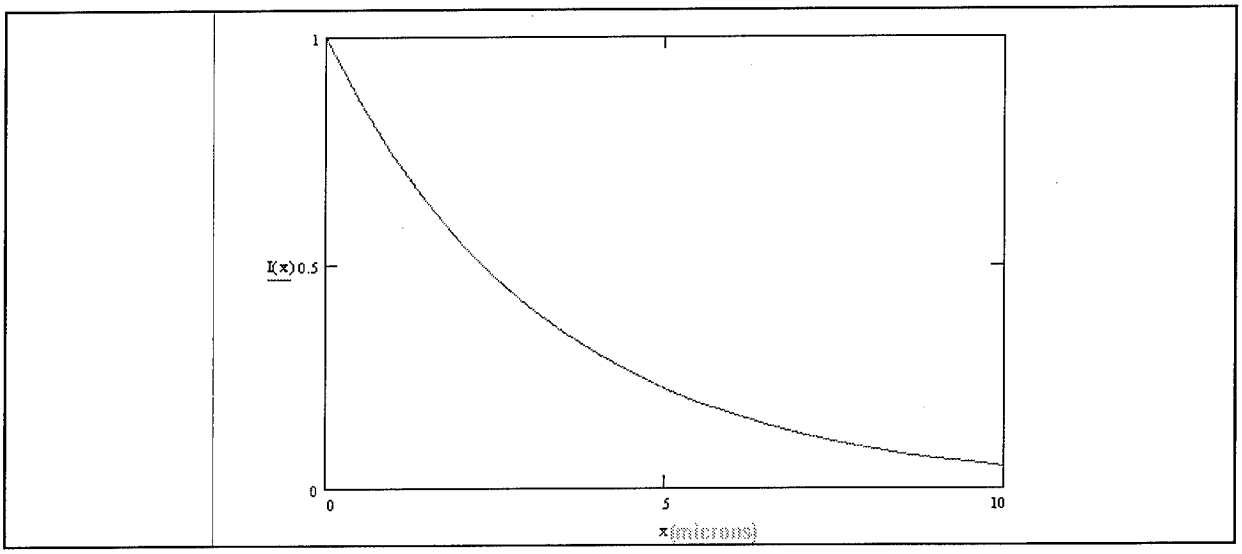


Figure 12. Intensity at a depth x of an arbitrary intensity of "1" just under Si surface for 655nm light.

Two metalization patterns were tested for the 4X4 array of detectors. The main differences between the arrays were digit spacing and the use of a common ground in the right array vs using a separate ground for each detector in the left array. The two configurations are shown in Figure 11. In this generation of the detector array our goal was to establish a low frequency optical interconnect between computer boards using a simple emitter/detector pair and a DOE, hence no consideration was given for high speed data transmission (>50MHz) such as coplanar waveguiding. The details of the two array configurations are given in Table 1. There is a difference in active areas because the individual ground leads of the left array needed more space.

Array	**Left**	**Right**
Digit width	1μm	1μm
Digit spacing	5μm	10μm
Total digit length	595μm	790μm
Total digit contact area	595μm^2	790μm^2
Window dimensions	59 X 59μm	87 X 87μm
Active area	3136μm^2	7225μm^2
% metalized	0.19	0.11
Theoretical efficiency	46%	55%

Table 1 Design details of the two detector arrays.

An approximation of the efficiency of the MSM photodetectors is given by:

$$\text{Efficiency} = Y_m Y_t Y_c (1-e^{-\alpha x})$$

where Y_m is the fraction of light hitting the Si surface (ie not hitting the metal electrodes), Y_t is the fraction of light that is transmitted into the Si substrate (1 - reflection), and Y_c is the incident photon to freed electron/hole pair ratio. The exponential factor in parentheses represents the fraction of light that is absorbed within the collection region of the semiconductor (ie. not transmitted through and therefore contributing to photo-generated photodetector current). For the 59 X 59μm detectors, the theoretical efficiency using the above loss mechanisms is 46% while the 87 X 87μm detectors have a theoretical efficiency of 55%. The larger detectors will obviously collect more light if the image is blurred, but will also collect more optical crosstalk. The larger spacings between electrodes aide in device efficiency, but increase device response time.

Aluminum (Al) and gold (Au) metalizations were used on both n and p-type Si wafers. The different metal/semiconductor combinations produce different device operating characteristics. Figure 13 graphically represents the energy profile of the MSM detector under a range of operating modes. Device performance is dictated by the metal-to-semiconductor barrier height. The barrier height is dependant on the work function of the

metal used and the substrate doping level and type. A larger barrier height results in a smaller dark current which is critical for low light level operation of these devices.

Silicon dioxide (SiO_2) was used to electrically isolate the metalization leads connecting the photodetector electrodes to the die bonding pads. Without this isolation layer between metal runs and the semiconductor substrate, the entire metalization pattern on the die would act as a photodetector by collecting photo-generated charges outside of the photodetector active area. This would greatly increase optical crosstalk and decrease device signal to noise ratio (SNR).

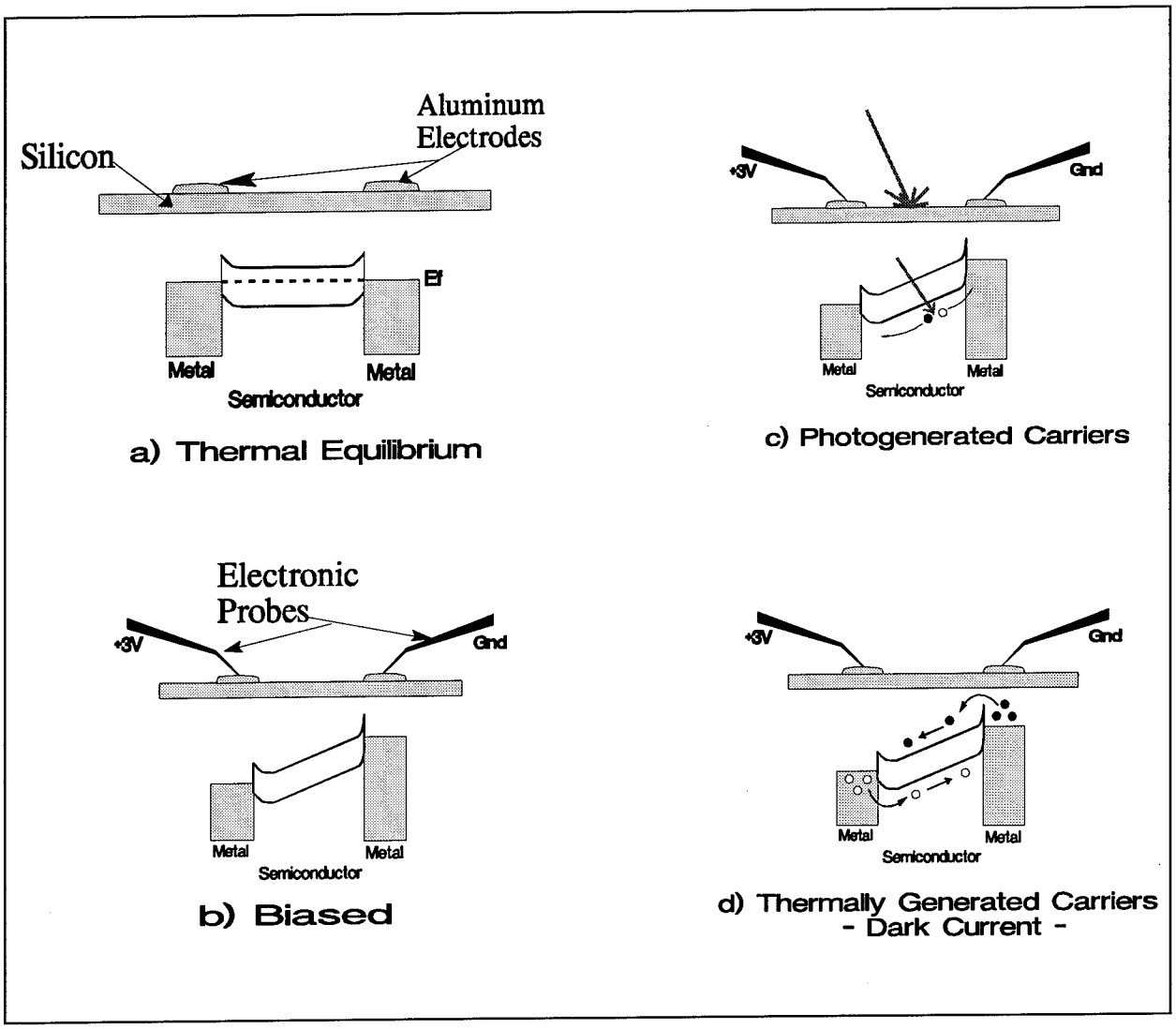


Figure 13. The energy diagram of metal-semiconductor-metal photodetectors under 4 operating modes: a) unbiased, no illumination, b) biased with no illumination, c) biased and illuminated, and d) biased with no illumination.

III. C. ii. FABRICATION

The MSM photodetectors were fabricated using standard photolithography and lift-off techniques. Two masks were used in conjunction with a 10 to 1 projection photolithography stepper. SiO_2 was first grown as an isolation layer on the standard, high resistivity (>10Ωcm) n and p-type Si substrates. Alignment marks and "windows" for the photodetector active areas were etched through the SiO_2 to the Si substrate. The electrodes were then defined using liftoff and metal deposited by evaporation. The detailed processing steps follow.

SiO_2 was deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD). Two thicknesses of SiO_2 (1000Å and 2000Å) were grown on both n and p-type Si wafers. Those four wafers were then liquid primed with HMDS-EGMEA (spun at 3000rpm for 30sec after a 10sec settling time) to prepare them for application of photoresist. Shipley 1400-27 photoresist was spun onto all wafers at 4000rpm for 30sec. The wafers were then subjected to a 60sec postbake at 90°C on a hotplate. One p-type wafer (with 1000Å SiO_2) was used for a photolithography exposure test to establish the proper exposure time. The optimum exposure time of 0.7sec was used on a 10 to 1 photolithography projection stepper. After exposure the wafers were developed for 1min in a 1:1 mixture of MF312 and de-ionized H_2O. The wafers were then placed in a 6:1 solution of water and HF (BOE or buffered oxide etch) to etch the active area windows and alignment marks. The photoresist remaining on the wafers (acting as the etch mask) was removed by an acetone bath.

Liftoff was used to define the 1μm digit width of the detector electrodes. The liftoff process is a technique that can create small (<1μm) structures with good repeatability once the process is calibrated. Figure 14 outlines the technique in pictorial form. The basis of the technique is to manipulate the photoresist in a way that produces an undercut profile. When metal is evaporated onto the photoresist covered substrate, gaps are left between the metal on the exposed substrate and the metal deposited on the photoresist. When soaked in acetone, the photoresist is dissolved "lifting off" the unwanted metal and leaving the metal evaporated on the exposed Si.

The wafers were primed, spun with photoresist, and postbaked using the same formula described in the SiO_2 widow etching process. An exposure test was run to establish the exposure time for the metalization mask. A number of ~10μm diameter "blisters" were apparent in test patterns subjected to long exposure times. Thermally grown SiO_2 wafers were then subjected to the same test to determine if the blisters were due to nonuniformities associated with the PECVD SiO_2 growth process. The thermally grown SiO_2 exhibited the same blistering effects. 1.5sec was chosen as the exposure time and resulted in few blisters. To establish the "undercut" resist profile the photoresist was "reversed" by baking the wafers for 80min in an ammonia (NH_3) atmosphere and then

placing them under an UV light for 1min. The resist was developed in 1:1 M312:H_2O solution for 30sec.

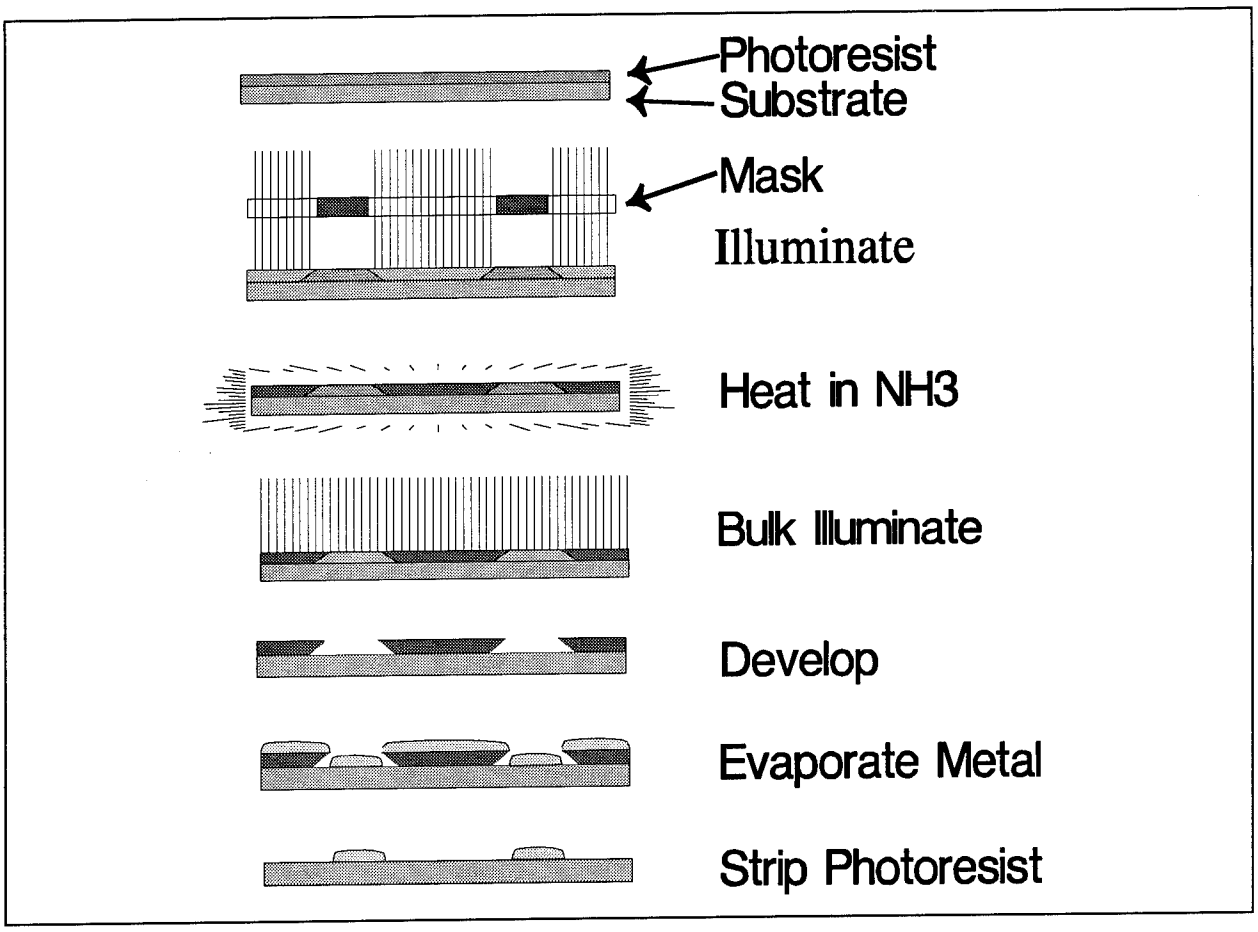


Figure 14. The "lift-off" procedure for depositing metal electrodes on a substrate.

The wafers were dipped for 1-2sec in the 6:1 buffered HF solution to etch away any native oxide that had grown in the active area and to hydrogen-terminate the Si surface limiting further oxide growth. 150nm of Au was evaporated on n and p-type wafers and 150nm of Al was evaporated on a p-type wafer. All wafers were soaked in acetone for 1hr, 15min and were subjected to 10sec of ultrasound to assist in the liftoff process.

III. C. iii. TESTING

Standard I/V, dark current, and responsivity tests were conducted for the different semiconductor types and electrode metals. The main test device used as a voltage source and for current measurements was an Anritsu 4145B Semiconductor Parameter Analyzer.

Responsivity tests were conducted by launching a HeNe laser beam (628nm) into a 9μm core fiber. The free end of the optical fiber was cleaved and attached to a micrometer and placed perpendicular to and directly over the detector under test. The fiber was placed such that the light output would underfill the photodetector active area. Neutral density filters were placed in front of the HeNe laser to establish a range of known optical power levels delivered to the photodetector. Dark current measurements were taken at a range of bias currents with all room lights and the HeNe laser turned off.

The performance of the detectors was measured using the proximity coupling of the fiber with an output of 500μW of 628nm HeNe light. At an electrode bias of 5V, 150μA of current flowed. The dark currents for the Al on p-type Si was 1μA for a 5V bias and 0.1μA for Au on n-type Si at the same bias. These dark current levels are high relative to the expected optical signal from an LED in the final demonstration. To improve the system SNR the detector will have to have a lower dark current, a higher responsivity, the light source will have to be stronger, and/or the DOE will have to have a greater diffraction efficiency.

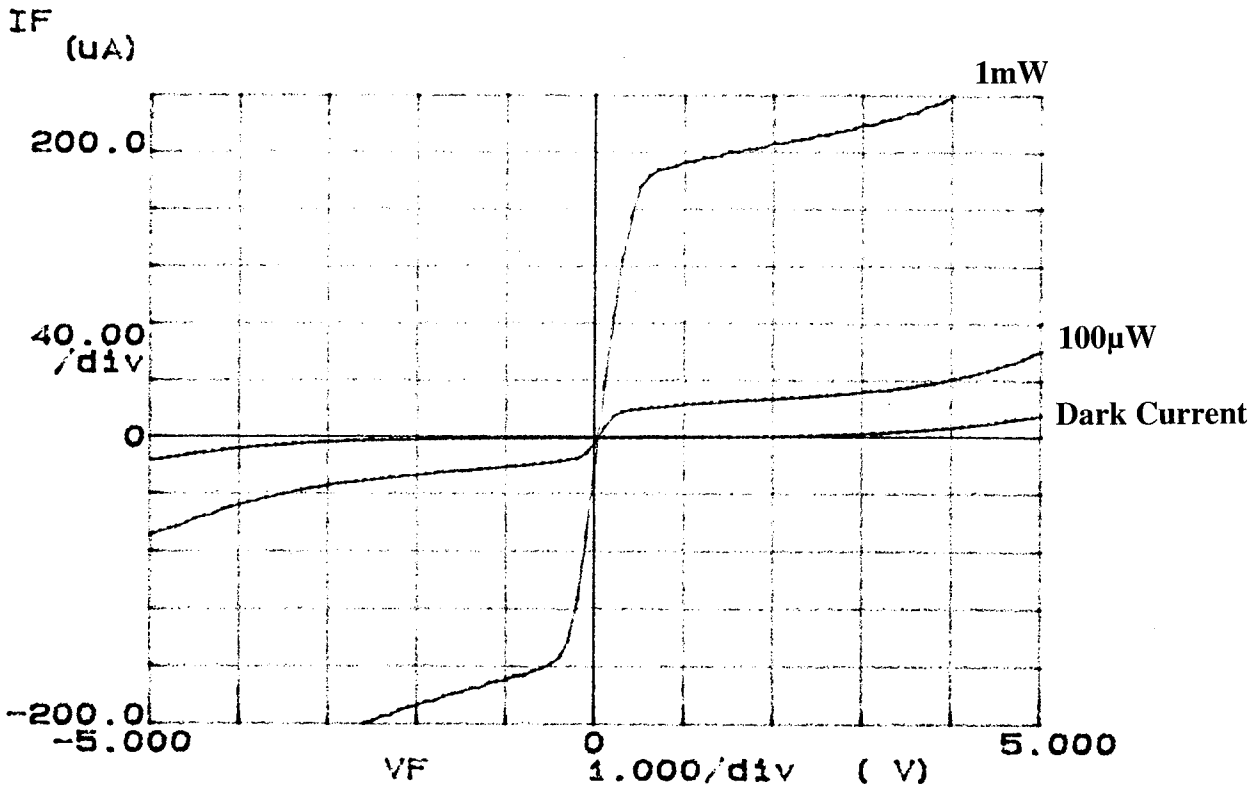


Figure 15. I/V curves of an MSM photodetector with Al metalization on an n-type Si wafer. The bottom curve shows the device dark current. The middle and top curves show the induced photocurrent with 100μW and 1mW of 780μm light incident on the detector.

IV. SYSTEM INTEGRATION

Pretested LED and photodetector die were epoxied and wirebonded to pc-boards. The pc-boards were designed to match the bonding pad layout of each die and to be as thin (1/16 in) as possible while still offering sufficient mechanical stability. The DOE die containing a two and a four level lens was glued to a glass microscope slide. The slide was etched with a grid pattern to assist in aligning the "upside down" DOE to the other two die.

Micrometers were used with a high power (1000X) microscope to perform the system alignment. First the LED die was centered in the highest power microscope objective's field of view. The die was then moved to the right a distance of 1500μm. The microscope was raised (using a calibrated micrometer) 3mm. The photodetector die was brought into focus and centered in the microscope's field of view using the XYZ stage attached to the pc-board. The microscope was again raised 3mm and the front edge of the DOE was brought into focus and centered by manipulating micrometers controlling the microscope slide holding the DOE die. The microscope was then focused on the photodetector array (the microscope can see "around" the DOE due to the NA of it's lower power objectives). Once power was applied to the LED's, their images, focused by the DOE were clearly visible on the photodetectors. Alignment time was approximately 15 minutes.

V. TESTING

Testing of the demonstration multi-channel optical interconnect consisted of assembling and aligning the three components within the built-in tolerance of +/- 1mil in the X and Yaxis. The microscope was used to observe the focusing ability of the DOE for the given die to die spacings. The main objective of this demonstration was a success; the DOE performed as expected. The LED images were clearly focused on the photodetectors. However, the optical signal reaching the photodetectors was too low to register above the detector dark current noise level. The amount of light incident on the active area of each detector is <10μW. Given the 0.3A/W responsivity of the detectors at a 3V bias, 10μW would generate 3μA of electrical signal. This upper limit of the output current is in the range of the 1μA and 0.1μA dark currents of the Al on p-type Si and Au on n-type Si respectively.

VI. RESULTS/CONCLUSION

Several conclusions can be drawn from this research. The first and most striking is that diffractive optics can be designed, fabricated, and aligned for use in a board to board intra-computer optical interconnects. DOE's can be designed with pc-based software packages,

fabricated with standard sub-micron fabrication tools (e-beam lithography), and can be used in a great range of monochromatic beam steering/focusing applications. The second conclusion is that simple source and detector arrays can be fabricated with a large degree of flexibility of layout and sizing. These devices are useful as a very low cost DOE test system or as components in a <50MHz/channel multichannel optical interconnect. A final conclusion that can be drawn from this work is that more research is needed in our source and detector designs. The light output from the LED's were limited due to the lossy nature of the GaAsP visible LED's. Future work in optical interconnects by our group will either utilize a more efficient light source (with a greater light output) and/or a detector with a lower dark current.

The components detailed in this report and the future generations of these components will enable computer architects to develop computer systems which are not limited in processing speed due to the chip-to-chip and board-to-board interconnect speed. Diffractive optics can be used for complex routing schemes interconnecting multiple processors and memory systems. With optical communications, the data rates that are possible offer a "transparent" interconnect pathway or a means of limiting pinouts through the use of multiplexing techniques. Real estate can further be conserved by "beaming" information directly to the input regions of a die instead of terminating all input/output bonding pads at the limited die border. Multichip modules are an ideal vehicle for the optical interconnect technology. The high speed optical transmitter and receiver die can be placed adjacent to the processing and memory die thereby limiting signal travel delays. For board to board interconnects the substrate must be transparent or it must be possible to fabricate an opening or optical "via" through it. This research will continue in the further development of the source, detector, and diffractive optic components with a multichannel, GHz/channel, MCM-to-MCM optical interconnect as the final goal.

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