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Defect Reduction and Back Channel Degradation in SIMOX

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Technical Report

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13. ABSTRACT *(Maximum 200 words)*

Because of potential back channel leakage problems and parasitic bipolar effects in silicon-on-insulator (SOI) metal-oxide-semiconductor (MOS) devices, especially n-channel MOS devices which must operate in an ionizing radiation environment, it is desirable to produce SIMOX wafers which have a layer of poor quality silicon near the Si/buried SiO_2 interface. Also, for device fabrication these wafers must have low defect, high quality silicon near the wafer surface.

In this program we have demonstrated, for the first time, that by Ge implantation and solid phase epitaxy regrowth, the surface region of the Si top layer of the SIMOX wafer is improved and the region adjacent to the buried SiO_2 is degraded. N-MOSFETs with and without Ge implantation, were fabricated on SIMOX and Si wafers. Our results show that Ge implantation into SIMOX significantly reduced off-state leakage and parasitic bipolar effects. In addition, gate-induced drain leakage of n-MOSFETs was greatly suppressed and the source-to-drain breakdown voltage was improved.

All devices were irradiated with 100 krad x-ray at RADC. Our measurements show that for devices fabricated on SIMOX with Ge implantation the off-state leakage current was up to 1000 times less than for devices fabricated on SIMOX without Ge implantation.

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PREFACE

We are very grateful to Dr. Les Palkuti for his continued support and encouragement of this work. We would also like to thank LCDR L. Cohn for his support of this program. We are indebted to many individuals from Spire and other institutions for the success of this program. These people include, but are not limited to: Dr. Walter Shedd for his fruitful discussions and advice and for providing us with irradiation facilities; to Dr. J. Chung and H. F. Wei at MIT for device fabrication and testing; to Dr. Kevin Jones and his students at the University of Florida for their XTEM experiments; and to Mr. Bobby Buchanan who was the program manager throughout most of this program.

CONVERSION TABLE

Conversion factors for U. S. Customary to metric (SI) units of measurement

MULTIPLY → BY → TO GET
TO GET ← BY ← DIVIDE

angstrom	1.000 000 X E -10	meters (m)
atmosphere (normal)	1.013 25 X E +2	kilo pascal (kPa)
bar	1.000 000 X E +2	kilo pascal (kPa)
barn	1.000 000 X E -28	meter^2 (m^2)
British thermal unit (thermochemical)	1.054 350 X E +3	joule (J)
calorie (thermochemical)	4.184 000	joule (J)
cal (thermochemical)/cm^2	4.184 000 X E -2	mega joule/m^2 (MJ/m^2)
curie	3.700 000 X E +1	*giga becquerel (GBq)
degree (angle)	1.745 329 X E -2	radian (rad)
degree Fahrenheit	$T_K = (T\,°F + 459.67)/1.8$	degree kelvin (K)
electron volt	1.602 19 X E -19	joule (J)
erg	1.000 000 X E -7	joule (J)
erg/second	1.000 000 X E -7	watt (W)
foot	3.048 000 X E -1	meter (m)
foot-pound-force	1.355 818	joule (J)
gallon (U.S. liquid)	3.785 412 X E -3	meter^3 (m^3)
inch	2.540 000 X E -2	meter (m)
jerk	1.000 000 X E +9	joule (J)
joule/kilogram (J/kg) (radiation dose absorbed)	1.000 000	Gray (Gy)
kilotons	4.183	terajoules
kip (1000 lbf)	4.448 222 X E +3	newton (N)
kip/inch^2 (ksi)	6.894 757 X E +3	kilo pascal (kPa)
ktap	1.000 000 X E +2	newton-second/m^2 (N-s/m^2)
micron	1.000 000 X E -6	meter (m)
mil	2.540 000 X E -5	meter (m)
mile (international)	1.609 344 X E +3	meter (m)
ounce	2.834 952 X E -2	kilogram (kg)
pound-force (lbs avoirdupois)	4.448 222	newton (N)
pound-force inch	1.129 848 X E -1	newton/meter (N · m)
pound-force/inch	1.751 268 X E +2	newton-meter (N/m)
pound-force/foot^2	4.788 026 X E -2	kilo pascal (kPa)
pound-force/inch^2 (psi)	6.894 757	kilo pascal (kPa)
pound-mass (lbm avoirdupois)	4.535 924 X E -1	kilogram (kg)
pound-mass-foot^2 (moment of inertia)	4.214 011 X E -2	kilogram-meter^2 (kg·m^2)
pound-mass-foot^3	1.601 846 X E +1	kilogram/meter^3 (kg/m^3)
rad (radiation dose absorbed)	1.000 000 X E -2	**Gray (Gy)
roentgen	2.579 760 X E -4	coulomb/kilogram (C/kg)
shake	1.000 000 X E -8	second (s)
slug	1.459 390 X E +1	kilogram (kg)
torr (mm Hg, 0° C)	1.333 22 X E -1	kilo pascal (kPa)

*The becquerel (Bq) is the SI unit of radioactivity; 1 Bq = 1 event/s.
**The Gray (Gy) is the SI unit of absorbed radiation.

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FIGURES (Continued)

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SECTION 1

INTRODUCTION

1.1 OBJECTIVE.

The main objectives of this program were to investigate the possibilities of implanting Ge into the silicon top layer of Separation by IMplantation of OXygen (SIMOX) wafers a) to reduce defect density in the surface silicon (the device region) and b) to degrade the quality of silicon near the Si/SiO_2 interface in order to decrease the back-channel leakage current and minimize parasitic bipolar effects.

We also evaluated the effect of a damaged back channel on device performance by fabricating test structures. SIMOX substrates would be implanted with Ge using an optimized process and then sent to an integrated circuits production facility (subcontract) to be run through a device processing line. Several circuits have been fabricated on the substrates, and their electrical characteristics would be evaluated before and after exposure to ionizing radiation.

1.2 BACKGROUND.

The fabrication of silicon-on-insulator (SOI) material with the SIMOX process has gained increasing importance in the fabrication of radiation hard devices. However, one of the obstacles to the more widespread use of SIMOX material is the high density of dislocations in the silicon top layer. Standard SIMOX wafers typically have a silicon surface layer about 1500Å thick and a buried layer about 4000Å thick. The interfaces are generally smooth and sharp, but there are some silicon islands in the buried oxide layer. The density of defects in this material has typically been observed at a level of about 10^8 to 10^{10} dislocations/cm^2.[1,2,3]

Potential back-channel leakage problems in SOI metal-oxide-semiconductor (MOS) devices, especially in n-channel MOS devices which must operate in an ionizing radiation environment, make it desirable to produce SIMOX wafers which have a layer of poor quality silicon near the Si/buried SiO_2 interface. At the same time, these wafers must have low defect, high quality silicon near the wafer surface for device fabrication.

We have demonstrated that with Ge ion implantation and solid phase epitaxy regrowth, the surface region of the silicon top layer of the SIMOX wafer is improved and the region adjacent to the buried SiO_2 is degraded. These results have been observed by Rutherford backscattering spectroscopy (RBS)/channeling, cross-sectional transmission electron microscopy (XTEM), and plan-view TEM (PTEM).

1.2.1 Improving the Crystalline Quality of SOI Material by Implantation.

It has been demonstrated[4] that the crystalline quality of the silicon layer grown on sapphire substrates (SOS) by chemical vapor deposition (CVD) can be improved by implantation of silicon ions and subsequent thermal annealing. Only amorphization and solid phase epitaxy regrowth are necessary to improve the crystalline quality of the silicon because defects in SOS material are planar (twins and stacking faults).[5] Conversely, the threading dislocation defects in the SIMOX material are linear and align along the (110) direction.[1] Therefore, partial amorphization of the silicon top layer is necessary but not sufficient to reduce the density of defects in SIMOX since the threading dislocations will regrow with the Si during solid phase epitaxy.

Threading dislocations are terminated by interfaces which, in SIMOX material, normally are at the buried layer and the wafer surface. Epitaxially-grown layers produced by CVD may also exhibit interface termination if the new layer is sufficiently strained relative to the substrate.[6] We anticipated that Ge implantation would not only produce an amorphized silicon layer (similar to Si implantation but with a lower dose) but would also create a strained layer because of the larger lattice constant of silicon alloyed with germanium as opposed to that of pure silicon. Thus, the strained layer would create an artificial interface and stop the propagation of threading dislocations during solid phase epitaxy regrowth.

Recently, substantial progress has been made in reducing threading dislocation density by using multiple implantation processes.[7,8,9,10,11] Although a Ge implantation process can reduce the density of threading dislocations that reach the surface. Figure 1-1 shows a cross section of a SIMOX wafer implanted with Ge at a dose of 5×10^{14} Ge^+/cm^2 at 150 keV and then annealed for 0.5 hour at 850°C in N_2. Figure 1-2 shows a plan-view TEM of the silicon top layer of the same sample; note the presence of several threading dislocation defects and dislocation loops. Figure 1-3 shows a plan-view TEM of only the surface region of the silicon top layer after the lower part of the sample was thinned; note that no threading dislocation defects can be seen in the Ge-implanted region. However, perhaps more importantly, Ge implantation creates a degraded region near the Si/buried SiO_2 interface which may be advantageous for radiation-hard device applications.

We have studied the effect of Ge implantation into the Si top layer of SIMOX material, followed by solid phase epitaxy regrowth, on reducing the density of threading dislocations that reach the surface. RBS/channeling work on Ge-implanted wafers proves that Ge occupies substitutional sites in Si. Details of this work may be found in the Phase I Final Report, contract # DNA001-88-C-0195, entitled "Defect Reduction in SIMOX Wafers." Figure 1-4 illustrates the angular scans for three different crystalline axes of a si sample implanted with 1×10^{15} Ge^+/cm^2 at 100 keV and annealed for 0.5 hour at 850°C. For these axes, the minimum yield, X_{min}, is quite similar and indicates that, as expected, the Ge dopant atoms are located on lattice sites in the Si.

Although the preliminary Ge doses used appeared too low to produce the desired strain, we did observe a reduction in threading dislocation density (see Figures 1-1, 1-2, and 1-3) which indicated that mechanism(s) other than a strained layer were responsible for the decrease. We believe that the defect density reduction is related to the creation of numerous point defects during Ge implantation and/or to end-of-range damage in the form of dislocation loops near the Si/buried SiO_2 interface which may pin down the dislocations during solid phase epitaxy regrowth.

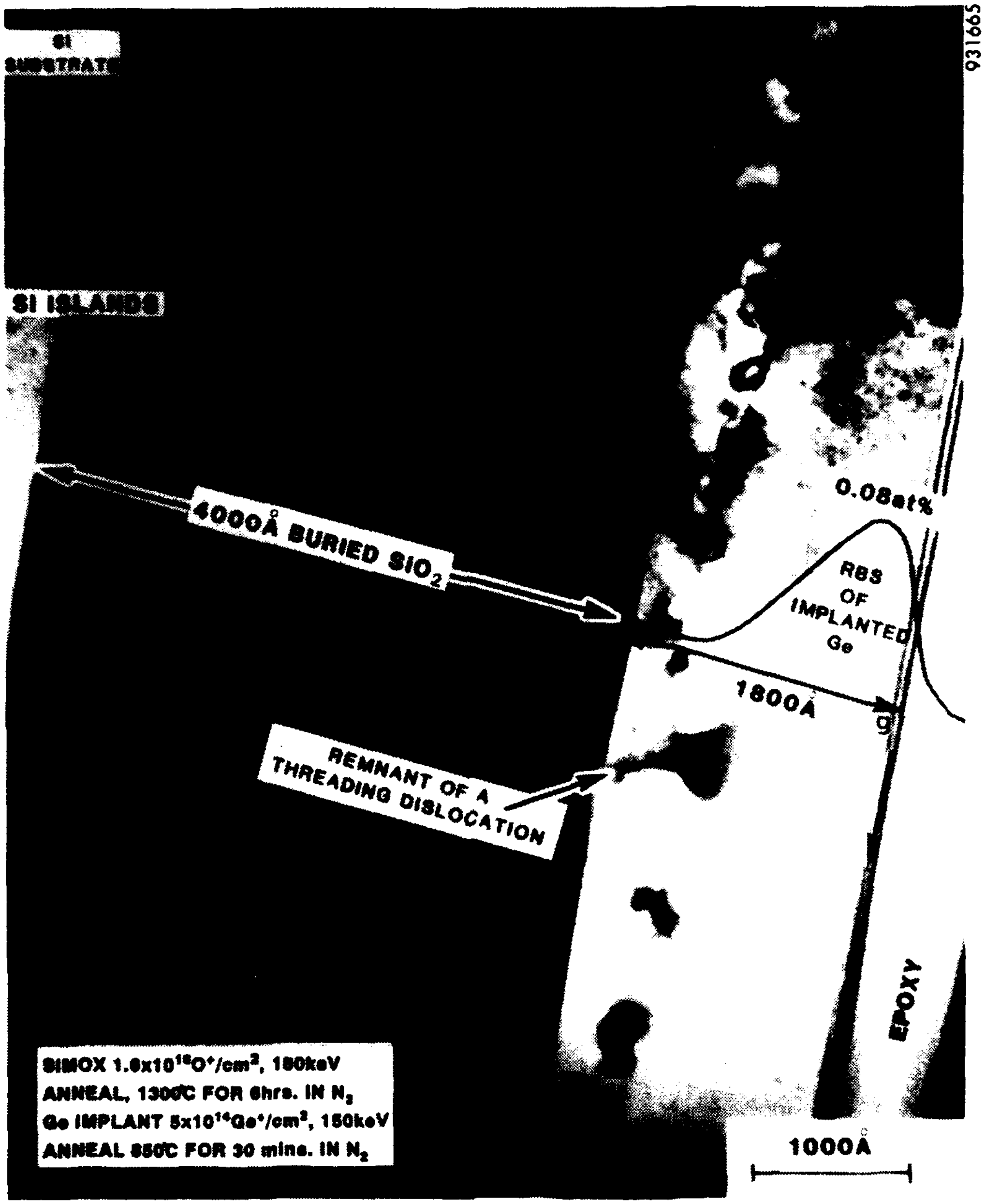


Figure 1-1. *Cross section of SIMOX wafer implanted with Ge at dose of 5×10^{14} Ge^+/cm^2 at 150 keV and then annealed for 0.5 hour at 850°C in N_2.*

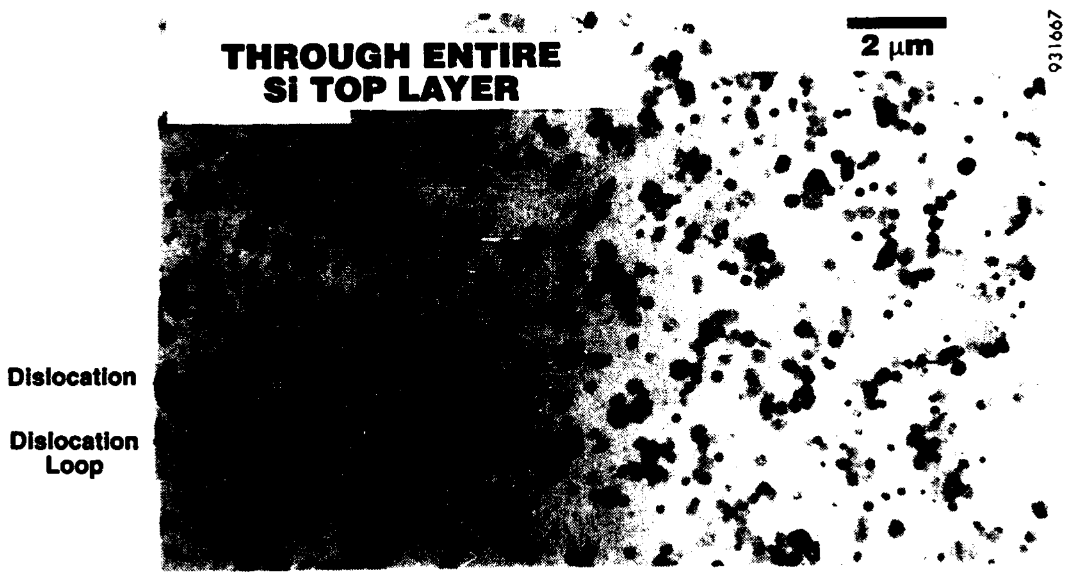


Figure 1-2. *Plan-view TEM of the silicon top layer.*

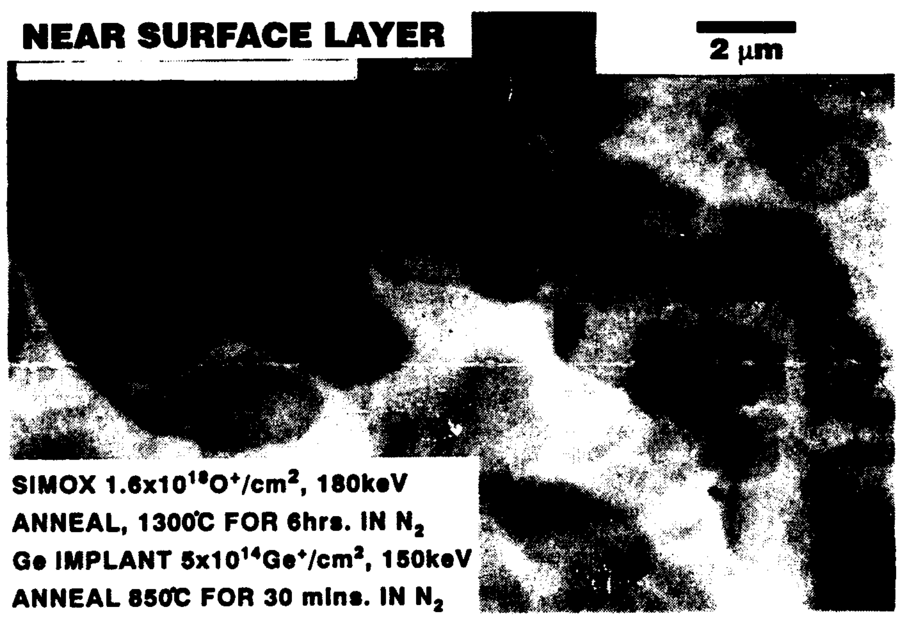


Figure 1-3. *Plan-view TEM of only the surface region of the silicon top layer.*

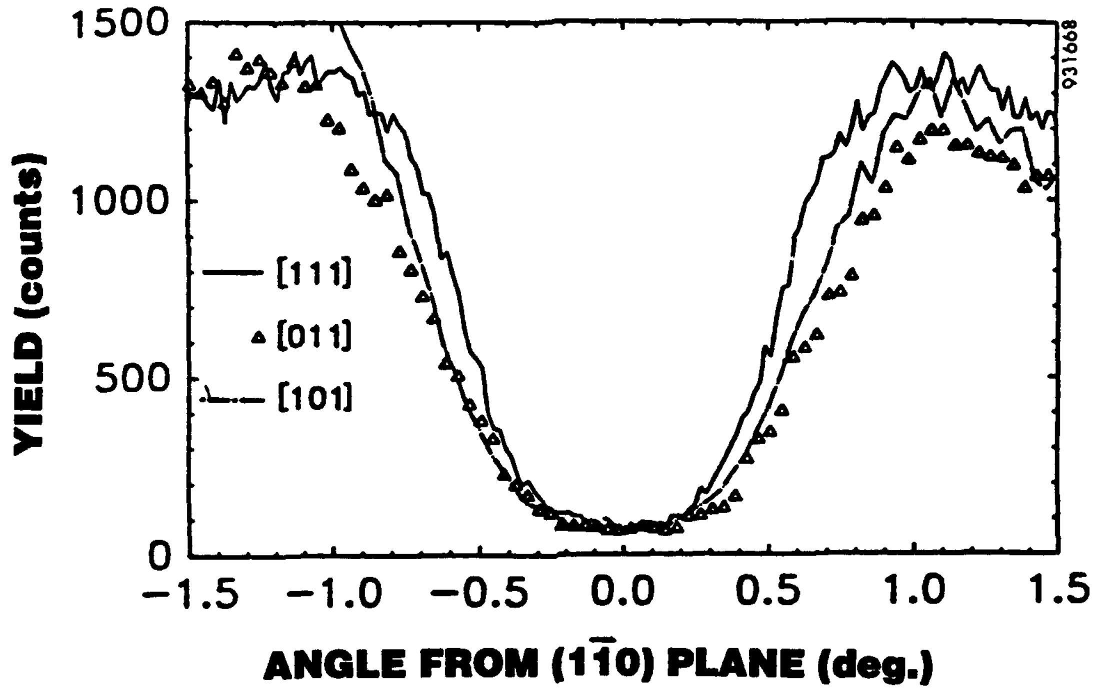


Figure 1-4. *Angular scans for three different crystalline axes of the silicon sample implanted with 1x10^{15} Ge^{+}/cm^{2} at 100 keV and annealed for 0.5 hour at 850°C. These scans indicate that germanium is substitutional.*

However, we observed that much higher strain levels (produced, in this case, by the growth of a Ge-doped epitaxial layer) do indeed deflect many threading dislocations away from the surface. Figure 1-5 is an XTEM of such a sample and clearly shows the reduction of the density of defects which reach the surface by the deflection of some of the dislocations away from the surface and back towards the SiO_2 interface. One aspect of Phase II was to use much higher doses of implanted Ge to investigate fully the effect of a sufficiently strained layer in combination with the other mechanisms responsible for reducing defect density.

During the period of Phase I and Phase II of this work, other processes have been developed by Spire and others such as multiple oxygen implantation which appear more effective on defect reduction of SIMOX material.[7-11] Therefore, in this program, we have emphasized creating degradation regions near the SiO_2 interface which are considered advantageous for radiation hard device applications. A variety of ways[12] exist for reducing "back-channeling" in metal-oxide-semiconductor (MOS) devices fabricated in SIMOX, but Ge implantation is more practical and achieves both a higher quality surface Si region and a degraded Si region near the Si/buried SiO_2 interface with one low dose, room temperature implantation.

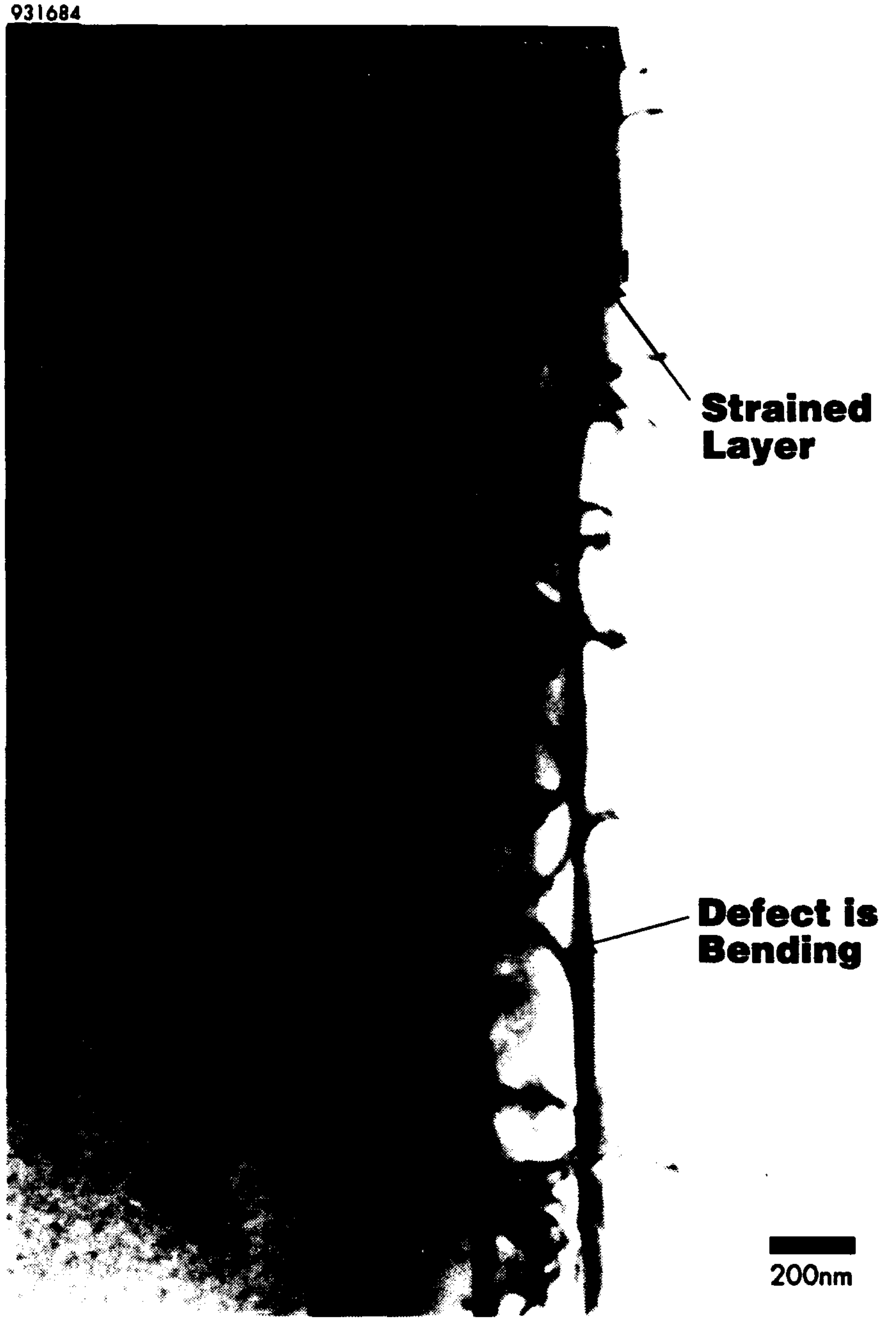


Figure 1-5. *Standard SIMOX wafer on which was epitaxially grown a pure Si layer followed by a Ge-doped Si layer (about 6% Ge) followed by a pure Si layer. This preliminary result clearly demonstrated that by creating a sufficiently strained layer we can deflect threading dislocation defects away from the surface.*

1.2.2 Back-Channel Leakage.

An MOS device fabricated in SOI material may have an unwanted parasitic MOS device at the silicon/buried insulator interface after exposure to ionizing radiation.[12,13,14] The passage of ionizing radiation through an insulator such as SiO_2 generates free electrons and holes. The electrons are more mobile and are swept out of the oxide, and the holes tend to be trapped near the silicon interface.[15,16] The trapped positive charge induces a negative charge in the silicon at the insulator interface, which can cause a change in the electrical characteristics of component MOS devices and can create inversion layers in p-type silicon (Figure 1-6).[13] If the inversion layer connects n-type regions of different potentials, a parasitic NMOS can be turned on by ionizing radiation, creating a permanent leakage path (Figure 1-6).

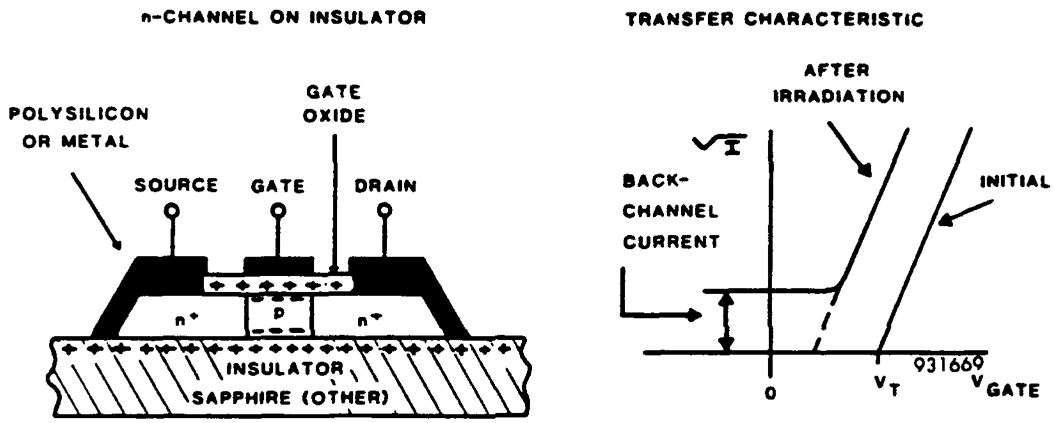


Figure 1-6. *Cross section of NMOS transistor on insulating substrate illustrating the trapped positive charge-induced parasitic back-channel and its effect on transfer characteristics.*[13]

Therefore, we need a silicon top layer which consists of a high quality layer at the surface for device fabrication, adjacent to a damaged layer. The high quality silicon surface layer is used for device fabrication, and the damaged silicon layer, because of reduced mobility, decreases the back-channel current.

Phase II work emphasized the radiation hardening of SIMOX material by reducing mobility in the interface region through degradation, thereby decreasing back-channel leakage current induced by ionizing radiation. Figure 1-7 illustrates another XTEM result of a standard SIMOX wafer Ge-implanted at 80 keV with a higher dose of 1×10^{16} Ge^+/cm^2. Figure 1-7 shows that no threading dislocations occur in the surface region and that a continuous damaged layer with a thickness of about 200 to 400Å has appeared near the Si/SiO_2 interface. The hardening of SIMOX material by the degradation of the Si/SiO_2 interface would be investigated primarily with Ge implanted into SIMOX, with subsequent solid phase epitaxy regrowth.

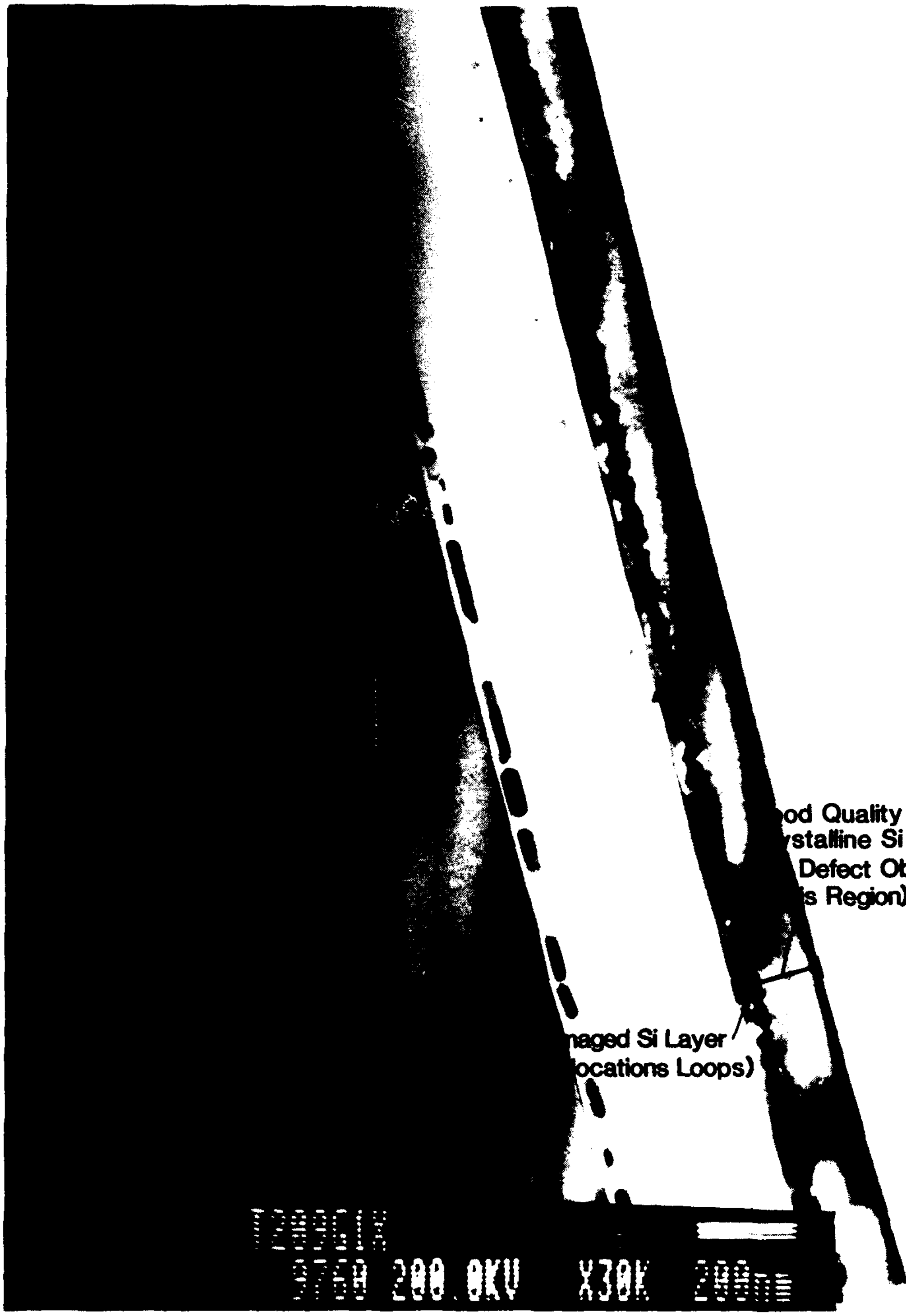


Figure 1-7. *XTEM of a SIMOX sample implanted with a dose of 1 x 10^{16} Ge^+/cm^2 at 80 keV and annealed for 0.5 hours at 850°C. Note the absence of threading dislocations in the surface Si region and the damaged layer near the Si/SiO_2 interface.*

SECTION 2

EXPERIMENTAL PROCEDURES AND DISCUSSION OF RESULTS

Throughout the Phase II program, we prepared a large number of SIMOX wafers for both materials analysis and device fabrication. These wafers were implanted with germanium under various conditions in order to optimize the parameters for producing SIMOX wafers with reduced defect density near the surface (device region) and a degraded back-channel region for improved radiation hardness and lower bipolar parasitic effects. Tables 2-1 and 2-2 summarize the list of wafers and Ge implantation. Figures 2-1 through 2-6 are representative optical reflectance and RBS data which were used to study the layer structure and composition of these wafers.

2.1 EFFECTS OF Ge IMPLANTATION ENERGY.

In Phase II, we studied the effects of Ge implantation energy on defect formation in the back-channel region of the Si top layer in SIMOX wafers. To reduce the back-channel leakage, the implantation energy must be adjusted so that the end-of-range damage is close to the Si/SiO_2 interface. However, our results indicated that a minimum distance between the amorphous/crystalline (α/c) and Si/SiO_2 interfaces must be maintained to ensure the formation of dislocation loops resulting from Ge implantation. If the projected depth of the end-of-range damage, as determined by implantation energy, is less than this critical distance, dislocation loop formation may be reduced. Therefore, optimizing the implantation energy and controlling the location of end-of-range damage are greatly significant.

We implanted Ge with a dose of 1×10^{15} Ge^+/cm^2 at 100 keV into both a bulk silicon and a SIMOX wafer with a Si superficial layer about 1700Å thick. The samples were then annealed at 850°C for 0.5 hours in nitrogen. Figures 2-7a and 2-7b show the XTEM results of the Ge-implanted SIMOX and bulk Si samples, respectively. The end-of-range damage (dislocation loops) can be clearly seen in Figure 2-7b. Fewer dislocation loops can be seen in the SIMOX sample as compared to the bulk Si sample. Comparison with the plan-view TEM obtained from these samples (Figures 2-7c and 2-7d) clearly indicates the creation of fewer dislocation loops in SIMOX material than in bulk Si. Dislocation loop densities were about 8×10^9 cm^{-2} in SIMOX and 1.85×10^{10} cm^{-2} in bulk Si.

Fewer dislocation loops may appear in SIMOX as compared to bulk Si because of the distance of the bulk Si dislocation loops from the surface (Figures 2-7a and 2-7b) which, in SIMOX wafers, corresponds nearly to the location of the Si/SiO_2 interface. Dislocation loops are believed to originate from Si interstitials. Based on our results, if the distance between α/c and Si/SiO_2 interfaces in Ge-implanted SIMOX is less than a critical value, the Si/SiO_2 acts as a sink for Si interstitials, resulting in fewer dislocation loops.

To confirm the above notion, we implanted a SIMOX wafer with a Ge dose of 2×10^{15} Ge^+/cm^2 at 80 keV and compared it to a bulk Si sample implanted with the same dose, but at 100 keV. Figures 2-8a and 2-8b show the PTEM results of these samples. The dislocation loop densities for both samples appear comparable; 2.5×10^{10} cm^{-2} for bulk Si and 1.85×10^{15} cm^{-2} for SIMOX.

Table 2-1. *List of Ge^+-implanted SIMOX wafers for materials research.*

Wafer	Dose (Ge^+/cm^2)	Energy (keV)	Anneal
#SOI3A	1E16	190	0.5 hrs at 850°C in N_2
#T240	1E16	190	0.5 hrs at 850°C in N_2
#T241	1E16	190	0.5 hrs at 850°C in N_2
SiCTL-A	1E15	100	0.5 hrs at 850°C in N_2
SIMOX-1	1E15	100	0.5 hrs at 850°C in N_2
SIMOX-2	2E15	80	0.5 hrs at 850°C in N_2
SIMOX-3	1E16	80	0.5 hrs at 850°C in N_2
SIMOX-4	2E16	80	0.5 hrs at 850°C in N_2
SIMOX-5	2E16	40	0.5 hrs at 850°C in N_2
SiCTL-B	2E16	40	0.5 hrs at 850°C in N_2
#T469B	1E15	80	2 hrs. at 850°C in N_2
#T469D	1E15	110	2 hrs. at 850°C in N_2
MULT-A	2E15	160	0.5 hr. at 850°C in N_2
802B	2E15	100	0.5 hr. at 850°C in N_2
802C	2E15	80	0.5 hr. at 850°C in N_2
802D	3E15	40	0.5 hr. at 850°C in N_2 1 hr. at 1000°C in N_2
802E	3E15	120	0.5 hr. at 850°C in N_2 1 hr. at 1000°C in N_2
802F	3E15	160	0.5 hr. at 850°C in N_2 1 hr. at 1000°C in N_2
#P1047 (p-type)	1E16	160	1 hr at 1000°C in N_2
#1047GE			1 hr. at 1000°C in Ar
#N1043 (n-type)	1E16	160	1 hr. at 1000°C in N_2
#1043GE			1 hr. at 1000°C in N_2
NAS-3	1E16	160	1 hr. at 1000°C in Ar

Table 2-2. *List of Ge^{+}-implanted SIMOX wafers for device research.*

Wafer	First Half		Second Half		Anneal/N_2 (0.5 hr.)
	Dose (Ge^{+}/cm^2)	Energy (keV)	Dose (Ge^{+}/cm^2)	Energy (keV)	
#SOI-1*	0	--	1E15	150	850°C
#SOI-2*	5E15	120	5E15	150	850°C
#SOI-3*	0	--	1E16	150	850°C
#SOI-4**	0	--	1E15	150	850°C
#SOI-5**	1E15	120	1E15	150	950°C
#SOI-6**	5E15	120	5E15	150	850°C
#SOI-7**	5E15	120	5E15	120	850°C
#SOI-8**	0	--	5E15	120	950°C
#SOI-9**	0	--	5E15	150	950°C
#SOI-10**	0	--	1E16	150	850°C
#SOI-11**	1E16	120	1E16	150	950°C
#SOI-12	0	--	0	--	--
#IBIS-1*	0	--	5E15	150	850°C
#IBIS-2**	0	--	5E15	150	950°C
#IBIS-3**	0	--	1E16	150	850°C
#IBIS-4**	5E15	150	1E15	150	850°C
#BULK-1*	0	--	5E15	150	850°C
#BULK-2**	0	--	5E15	150	850°C
#BULK-3**	0	--	5E15	150	950°C
#BULK-4**	1E16	150	1E15	150	950°C

* Ge implant before LOCOS ** Ge implant after LOCOS

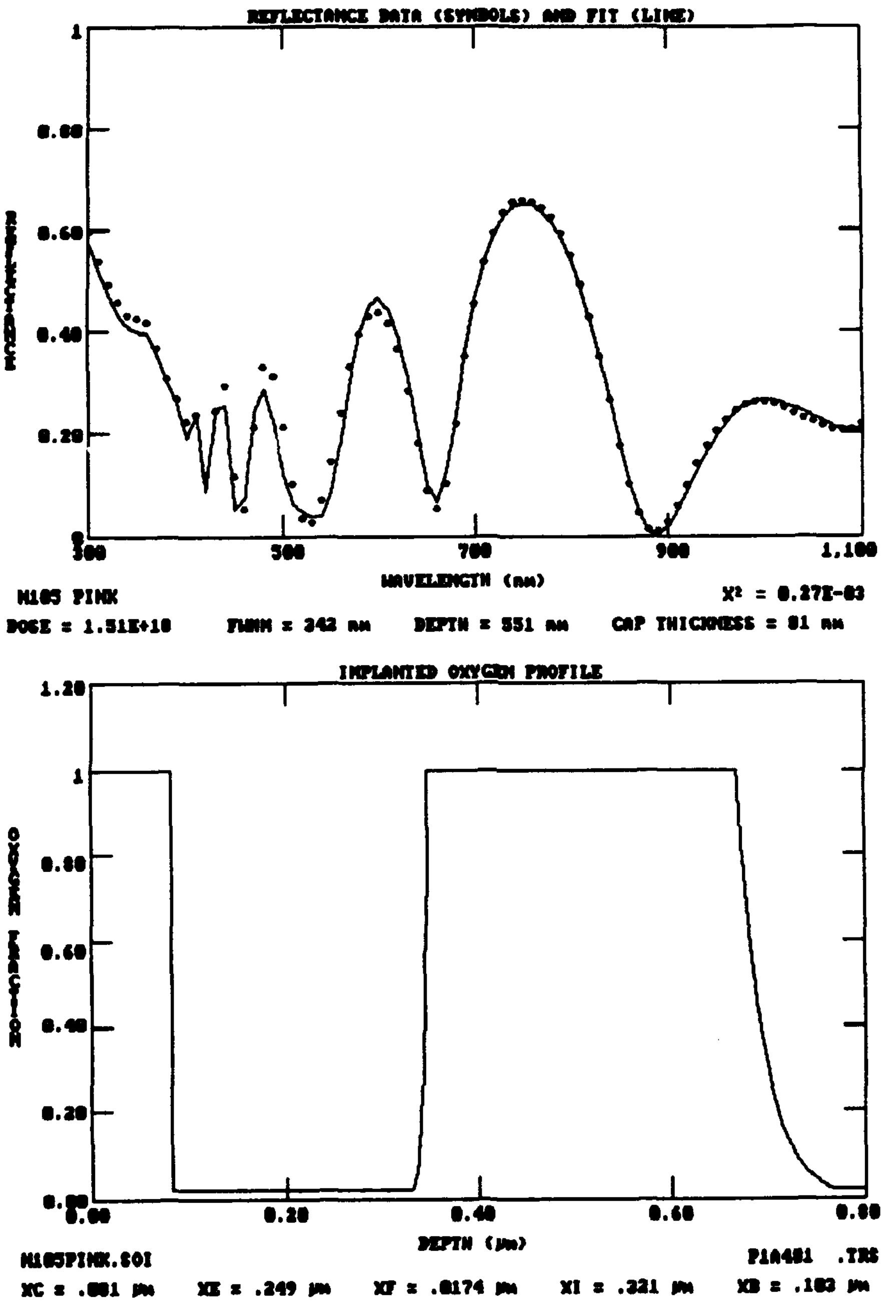


Figure 2-1. *Optical reflectance data with fit and analysis for standard SIMOX wafer #N105 indicating a silicon top layer about 2490Å thick and a buried oxide layer about 3210Å thick.*

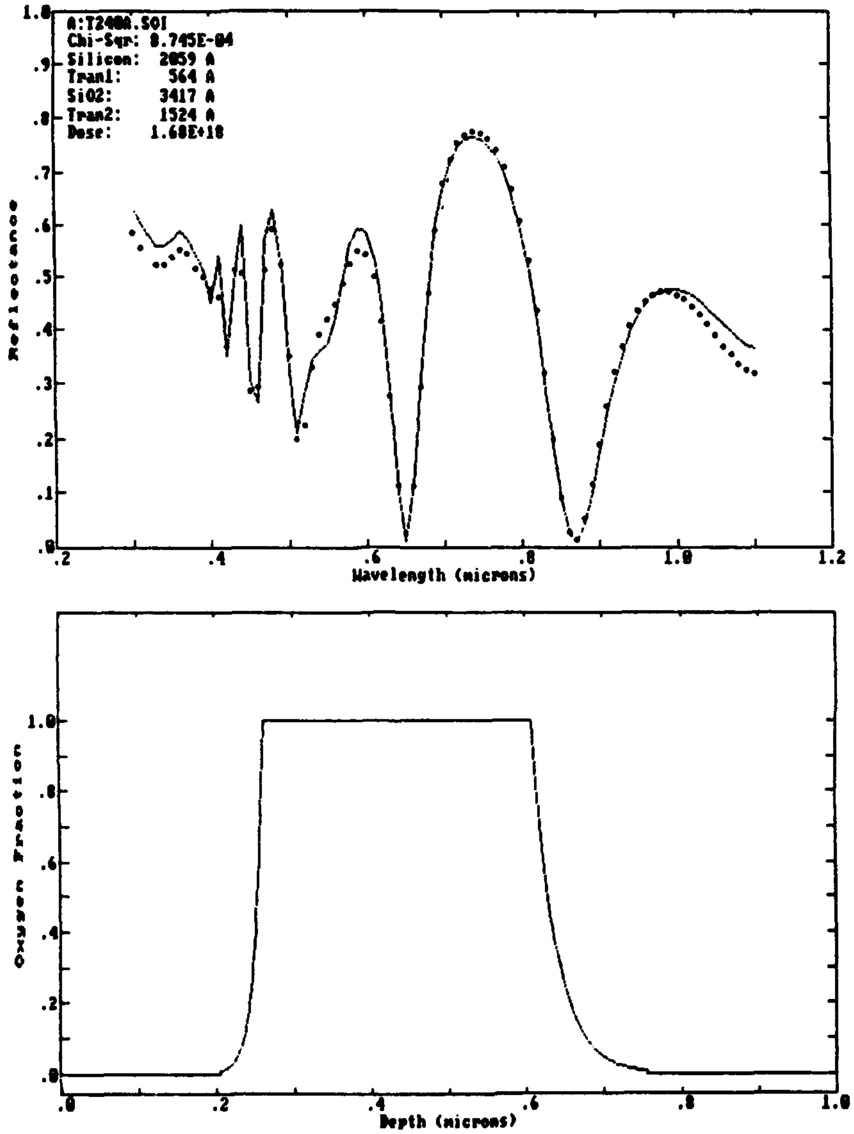


Figure 2-2. *Optical reflectance data with fit and analysis for standard SIMOX wafer #T240 indicating a silicon top layer about 2060Å thick and a buried oxide layer about 3420Å thick.*

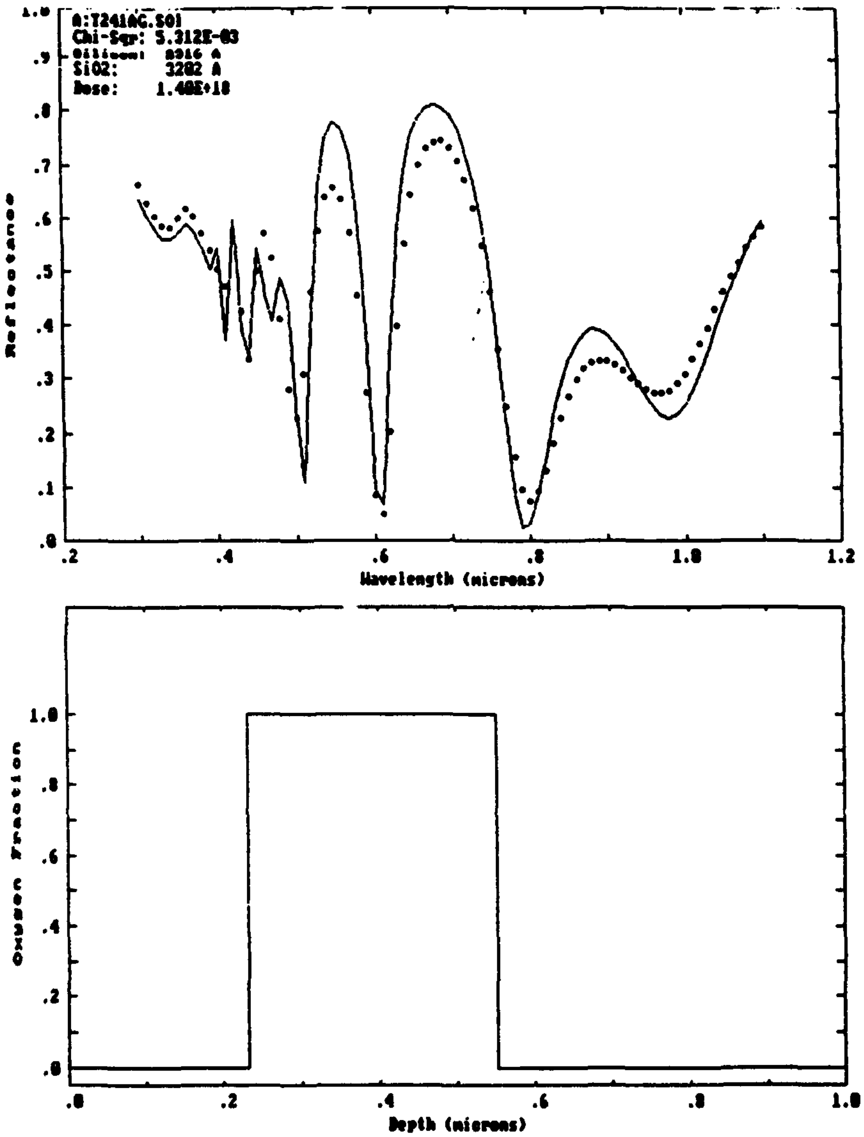


Figure 2-3. *Optical reflectance data with fit and analysis for standard SIMOX wafer #T241 indicating a silicon top layer about 2200Å thick and a buried oxide layer about 3200Å thick.*

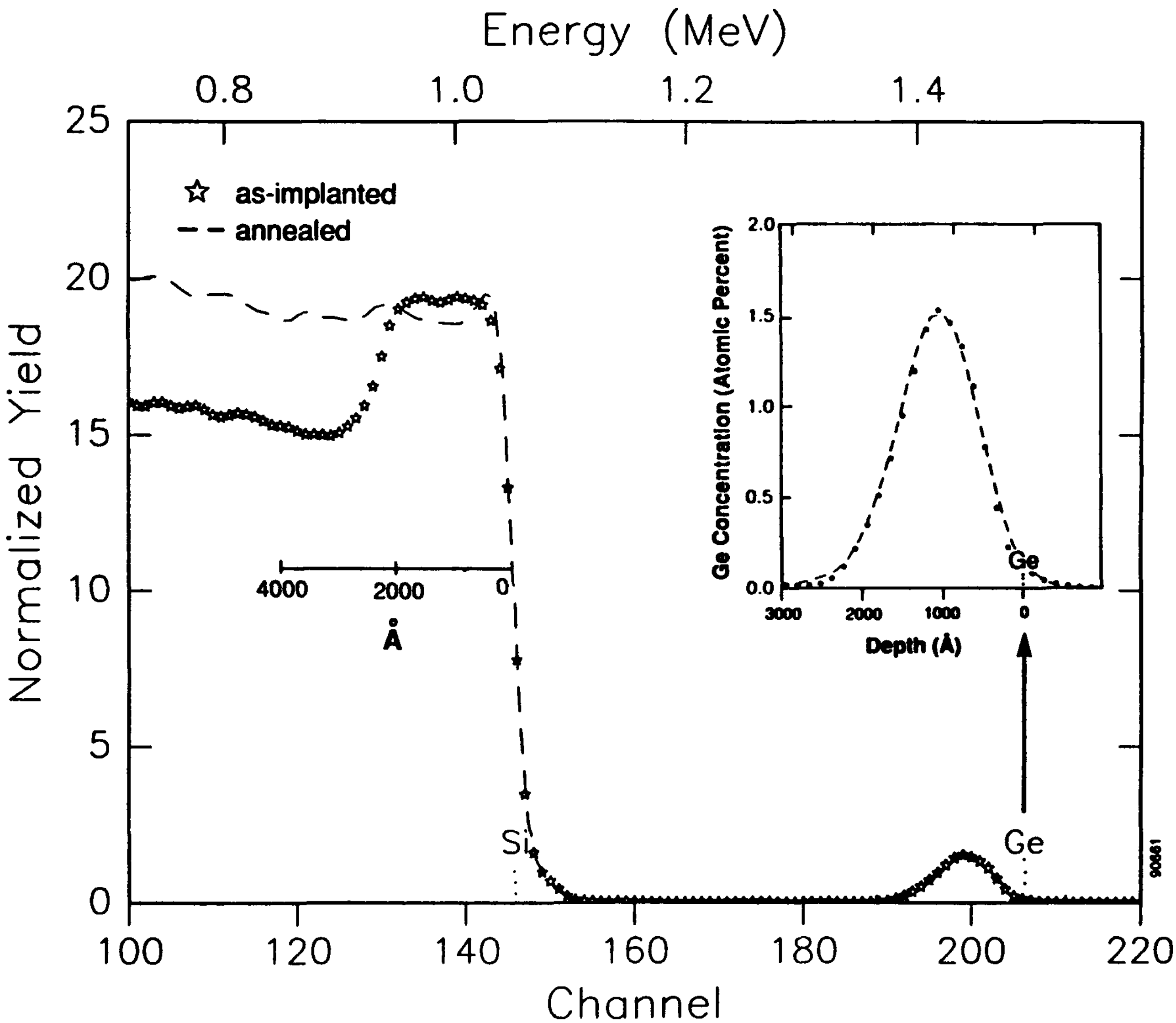


Figure 2-4. *RBS results for Si control sample #CTL1 implanted with a Ge dose of 1 x 10^{16} Ge^{+}/cm^{2} at 190 keV before and after annealing for 0.5 hour at 850°C in N_2. No redistribution of Ge resulting from annealing can be observed.*

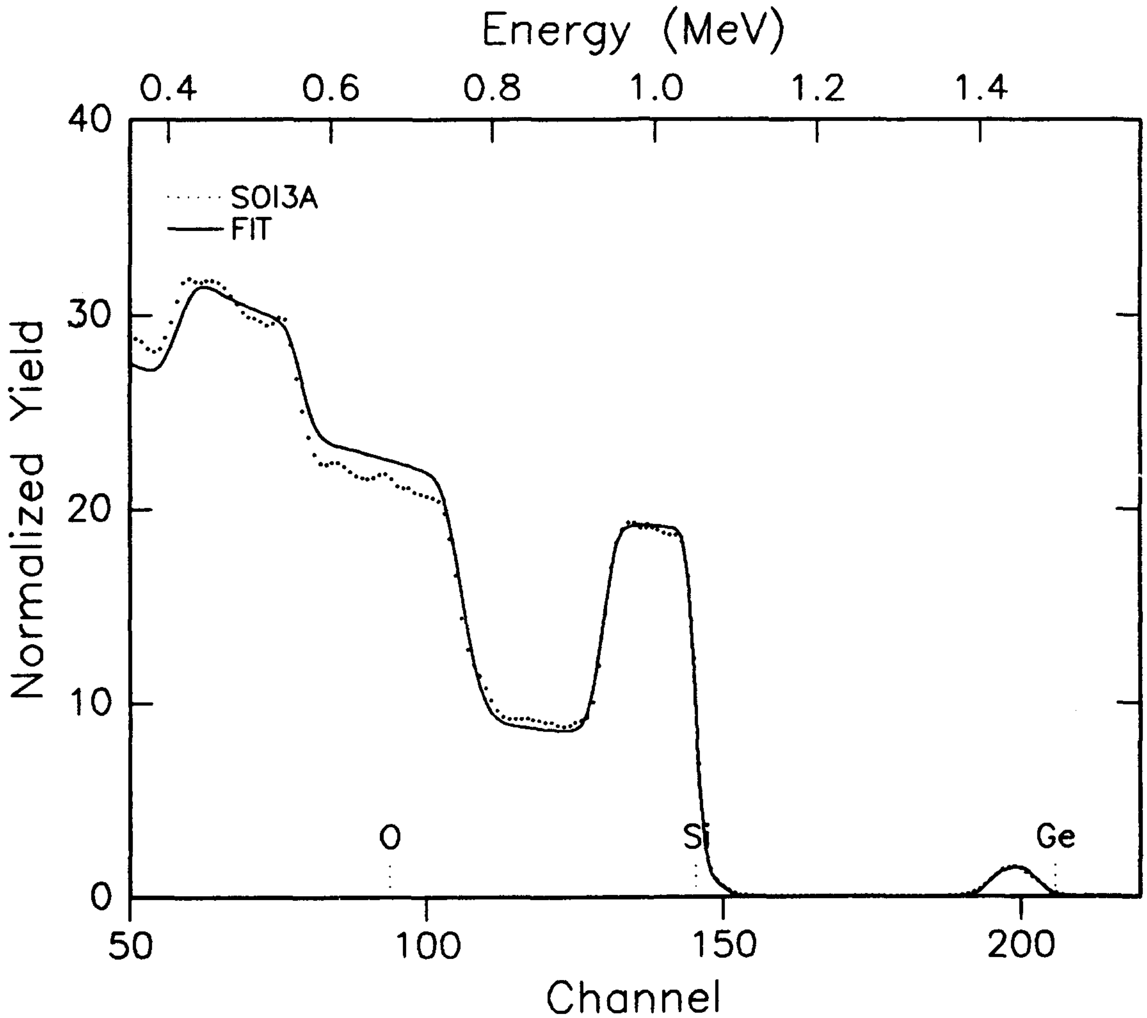


Figure 2-5. *RUMP code fit to RBS results for SIMOX sample #SOI3A (a piece of #N105) implanted with a dose of 1 x 10^{16} Ge^{+}/cm^{2} at 190 keV and annealed for 0.5 hours at 850°C in N_2. Results show a Si-Ge layer about 1240Å thick with Ge concentration of 1.54 atomic percent, 400Å below the surface. Total Si top layer thickness is about 2450Å which is in agreement with optical reflectance results.*

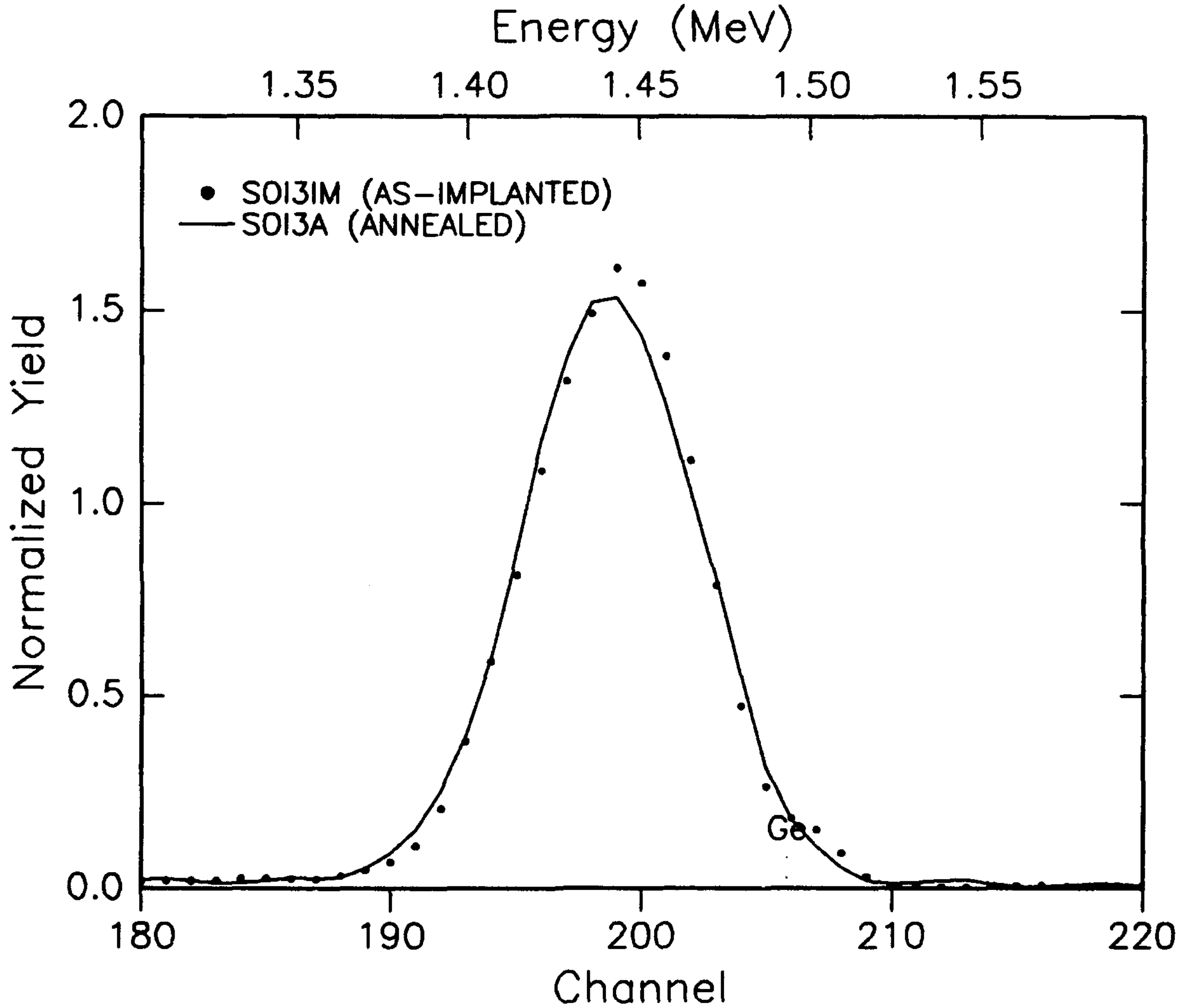


Figure 2-6. *RBS spectra of the Ge profile in as-implanted and annealed pieces of SIMOX sample (#SOI3) implanted with a dose of 1 x 10^{16} Ge^{+}/cm^{2} at 190 keV. As in the control Si sample shown in Figure 2-1, no significant redistribution of Ge resulting from annealing can be observed.*

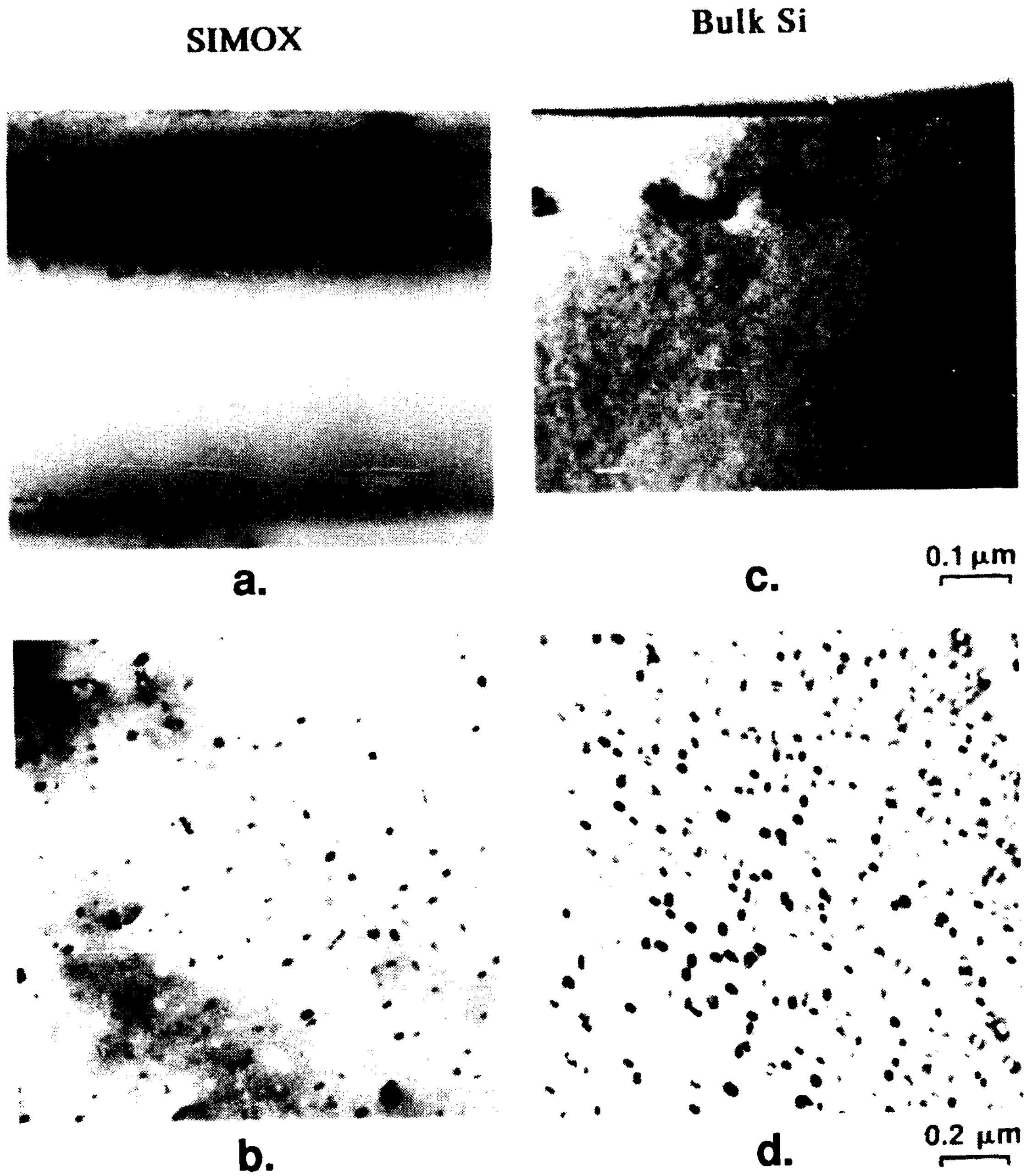


Figure 2-7. *Cross-sectional and plan-view TEMs show effect of Si/SiO_2 interface on dislocation loop formation. a) XTEM of SIMOX sample implanted with $1x10^{15}$ Ge^{+}/cm^2 at 100 keV and annealed for 0.5 hour at 850°C in N_2. b) XTEM of bulk Si sample implanted with Ge and annealed under above conditions. c) and d) Plan-view TEMs of samples in a and b, respectively. The fewer dislocation loops in SIMOX as compared to bulk Si may be explained by distance of dislocation loops from surface, which, in SIMOX wafers, closely corresponds to location of Si/SiO_2 interface.*

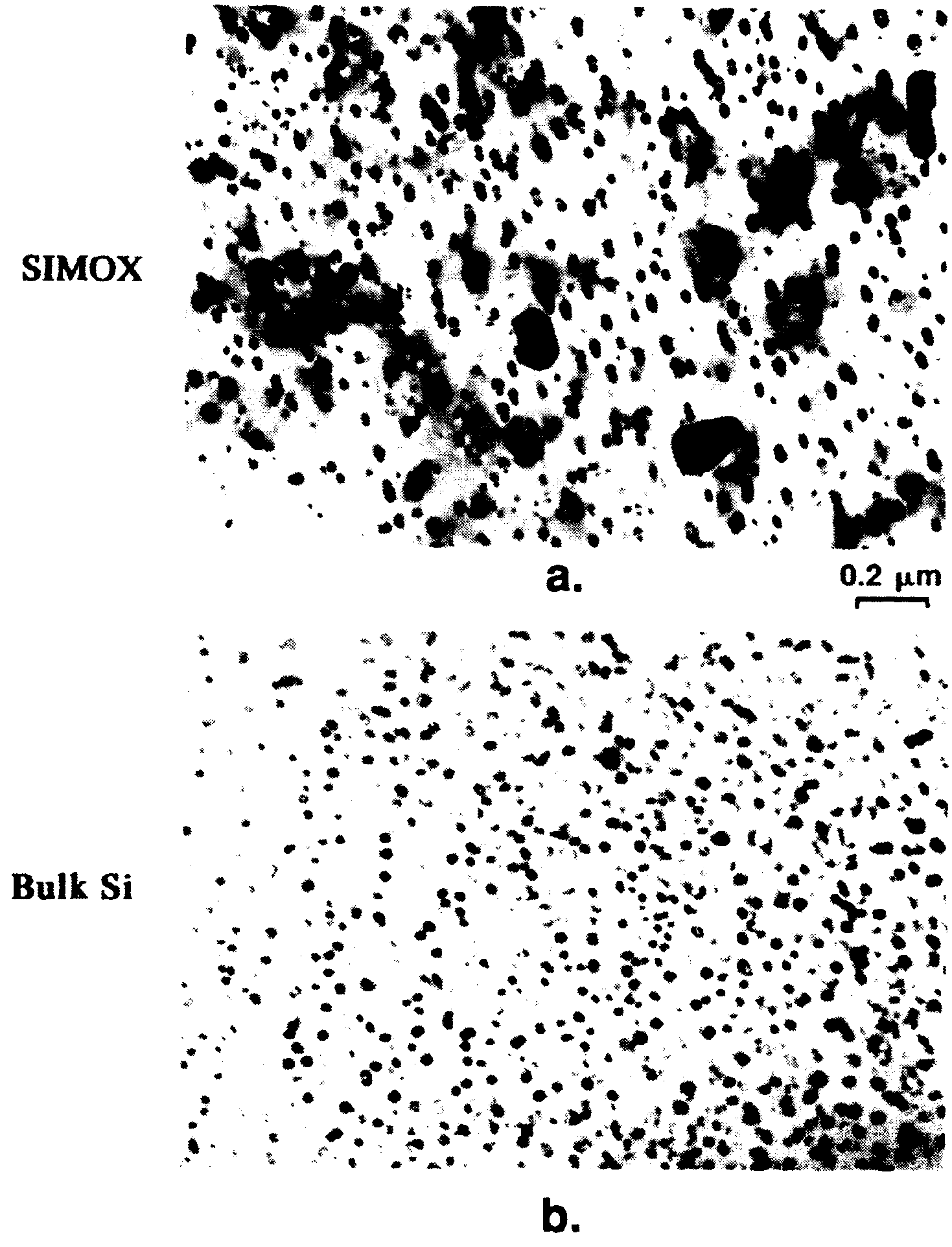


Figure 2-8. *Plan-view TEM results from a) SIMOX sample implanted with a dose of $2x10^{15}$ Ge^{+}/cm^{2} at 80 keV and b) bulk silicon sample implanted with the same Ge dose but at 100 keV. When, by lowering the implantation energy, the α/c interface in SIMOX wafers moves away from the Si/SiO_2 interfaces, the dislocation loop density becomes comparable to that in bulk Si.*

These results indicate that the creation of the dislocation loops strongly depends on the location of the α/c interface relative to the buried oxide layer. If Ge implantation into SIMOX is carried out so that the α/c interface is closer to the buried oxide interface than the critical distance, fewer dislocation loops will be created.

2.2 EFFECTS OF Ge IMPLANTATION DOSE.

Following the study of the effect of Ge implantation energy, we studied the effect of Ge implantation dose on the formation of a degraded back-channel region in SIMOX structures. We implanted several SIMOX samples with various Ge doses at 80 keV and annealed them for 30 minutes at 850°C in nitrogen. These samples were studied by PTEM and XTEM to characterize the defect formation in the back-channel region as a function of Ge implantation dose. Some samples were also produced by implanting Ge at 40 keV.

Figure 2-9a shows the dislocation loops produced by end-of-range damage resulting from implanting a SIMOX sample with a Ge dose of 2 x 10^{15} Ge^+/cm^2 at 80 keV. As the Ge dose increases to 1 x 10^{16} Ge^+/cm^2, the dislocation loop density increases significantly (Figure 2-9b). Figure 2-9c illustrates that if the Ge dose is further increased to 2 x 10^{16} Ge^+/cm^2, no individual dislocation loops are observed. In the latter sample, the dislocation loops appear to overlap and form a network of defects. These results can also be seen in Figures 2-10a and 2-10b which depict XTEM micrographs from the SIMOX samples implanted with Ge doses of 2 x 10^{15} and 2 x 10^{16} Ge^+/cm^2, respectively. Only individual dislocation loops can be seen in the sample with 2 x 10^{15} Ge^+/cm^2, while defects in the sample implanted with 2 x 10^{16} Ge^+/cm^2 appear extended and continuous.

The defect structure resulting from end-of-range damage in the SIMOX sample implanted at 80 keV with 2 x 10^{16} Ge^+/cm^2 may have been partially influenced by the Si/SiO_2 interface. When comparing PTEMs from this sample and those from a Si control sample implanted under the same conditions, we saw slightly different defect structures (Figures 2-11a and 2-11b). Also, threading dislocations in SIMOX wafers may possibly play a role in structuring the end-of-range damage. However, this effect is not fully understood.

Conversely, PTEM results from a SIMOX sample and a Si control wafer implanted under identical conditions with a dose of 2 x 10^{16} Ge^+/cm^2 at an implantation energy of 40 keV show no difference in the structure of end-of-range damage (Figure 2-11c and 2-11d). As shown in these figures, only individual dislocation loops can be observed in both the SIMOX and the Si samples.

We also studied the relationship between the dislocation loop defect density and the Ge implantation dose and energy. The effect of the damaged layer formed by Ge implantation must be related to the electrical properties of the back-channel region. One of the best approaches for investigating the back-channel region in SIMOX is by using back-gate MOSFET structures. However, we also attempted to study various electrical properties of Ge-implanted samples using simpler test structures and several characterization techniques such as spreading resistance and C-V measurements.

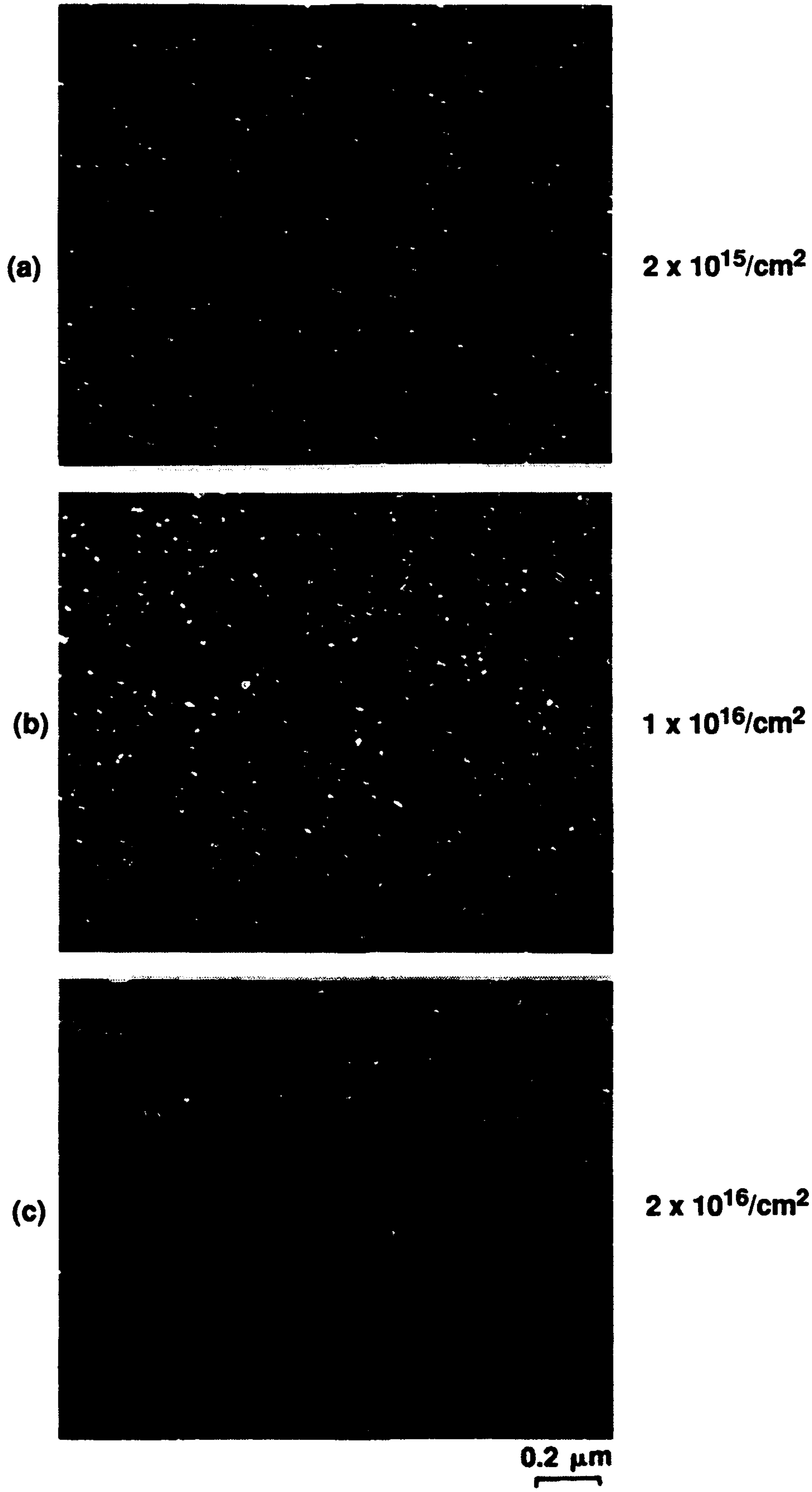


Figure 2-9. *PTEM micrographs of SIMOX samples implanted with Ge at 80 keV with doses of a) 2 x 10^{15} Ge^+/cm^2, b) 1 x 10^{16} Ge^+/cm^2, and c) 2 x 10^{16} Ge^+/cm^2.*

80 keV
(a) $2 \times 10^{15}/cm^2$

80 keV
(b) $2 \times 10^{16}/cm^2$

Figure 2-10. *XTEM micrographs of SIMOX samples implanted with Ge at 80 keV with doses of a) 2×10^{15} Ge^+/cm^2 and b) 2×10^{16} Ge^+/cm^2.*

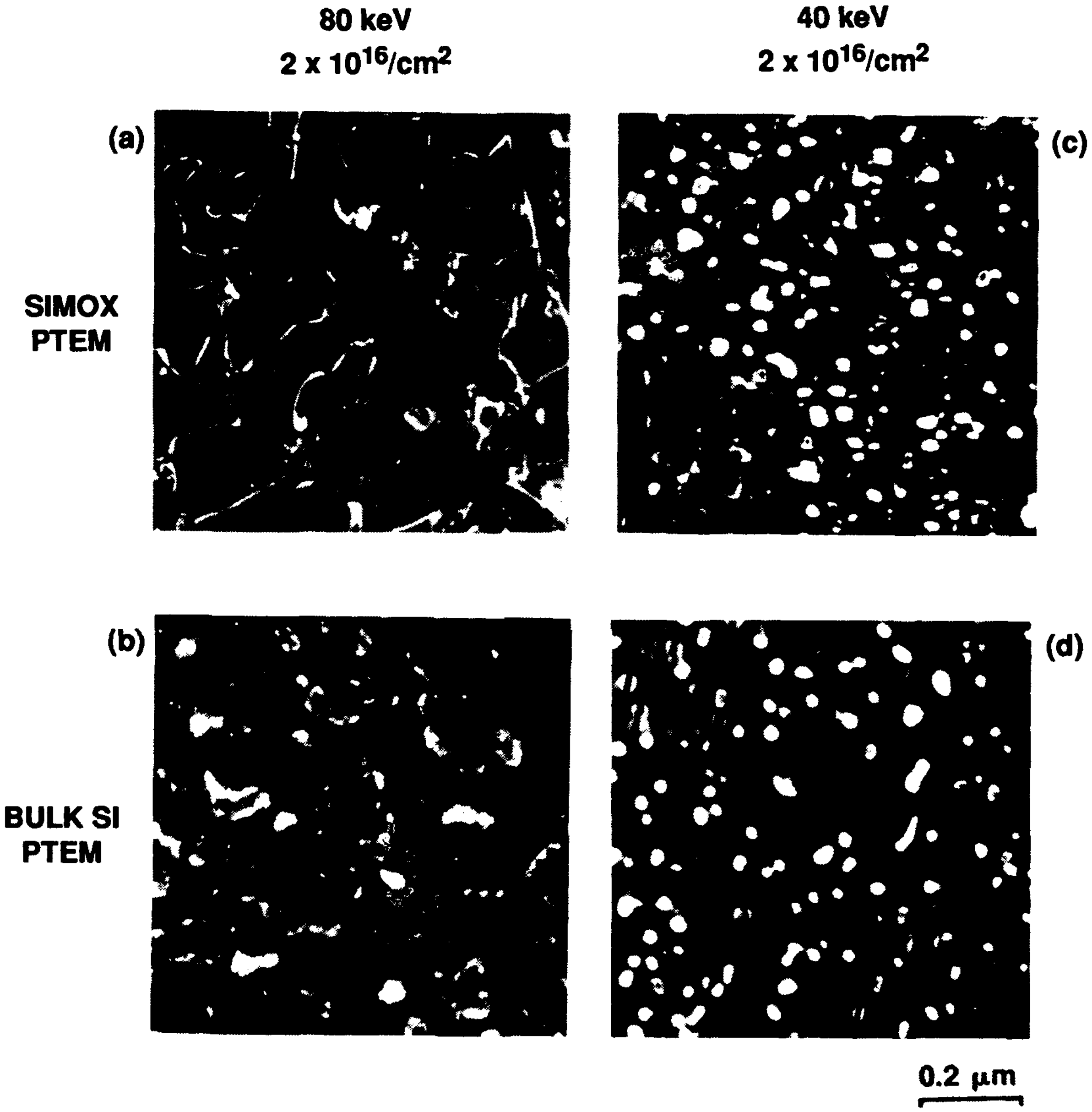


Figure 2-11. *PTEM results for samples implanted with 2×10^{16} Ge^{+}/cm^{2}; a) SIMOX sample implanted at 80 keV, b) Si sample implanted at 80 keV, c) SIMOX sample implanted at 40 keV, and d) Si sample implanted at 40 keV.*

2.3 EFFECTS OF HAZE.

One objective of this program has been to study and compare the effects of Ge implantation on the degradation of the back-channel region in SIMOX wafers produced at Spire and other companies in the US and overseas. We used multiple-implant SIMOX wafers from a commercial vendor to verify that back-channel degradation by Ge-implantation applies universally to all SIMOX wafers.

As noted above, we studied the layer structure of the wafers using optical reflectance and Rutherford backscattering spectroscopy (RBS). The results showed SIMOX wafers with Si top layers about 1800Å thick and buried oxide layers about 4500Å thick. We implanted a piece from one of these wafers with a dose of 2 x 10^{15} Ge^+/cm^2 at 160 keV and annealed the sample at 850°C for 30 minutes in N_2.

After Ge implantation, we studied the layer and crystalline structure of this sample using RBS and XTEM. The RBS results shown in Figure 2-12 indicated that after Ge implantation and annealing a Si:Ge layer about 1160Å thick, with a peak Ge concentration of about 0.5 at.%, formed close to the wafer surface. The results also suggested that the end-of-range damage, as determined by the penetration depth of Ge ions, should be about 500Å from the upper Si/SiO_2 interface.

Figure 2-13 is an XTEM micrograph of the multiple-implant SIMOX sample after Ge implantation and annealing. The buried oxide layer appears of very good quality and is continuous with no Si islands, but the Si top layer does not have good crystallinity and seems either amorphous or poly-crystalline. These results were inconsistent with our established results for Ge implantation into single-implant SIMOX wafers with similar layer thicknesses (as determined by optical reflectance and RBS). We repeated the XTEM analysis of the sample, with the same results. We speculated that the results related to the degree of "haze" on the commercial multiple-implant wafers. Before Ge implantation, we had noticed a considerable amount of haze on the wafer surfaces and, therefore, studied the surface morphology using an optical microscope. Figure 2-14 compares the optical micrographs (1000x magnification) from the surface of the commercial multiple-implant SIMOX wafer with those from a similar non-Ge-implanted wafer produced at Spire.

We discussed our findings with technical personnel from the SIMOX vendor. They indicated that the upper Si/SiO_2 interface in their multiple-implant wafers is generally wavy, and that this waviness produces haze at the wafer surface. After further discussion, we attempted to find an explanation for the resulting amorphous/poly-crystalline Si top layer after Ge implantation and annealing.

One possible explanation is that the waviness at the upper Si/SiO_2 interface plays an important role in the solid phase epitaxy (SPE) regrowth of the Si top layer. Figures 2-15a and 2-15b show schematics of two SIMOX structures, one with a smooth upper Si/SiO_2 interface and the other with a wavy interface, implanted with Ge under identical conditions. If Ge implantation amorphizes the Si layer as indicated in the figures, problems will arise during SPE regrowth of the sample with the wavy interface. Since only pockets of single-crystal Si remain after Ge implantation, rather than a continuous layer, these regions can only recrystallize the

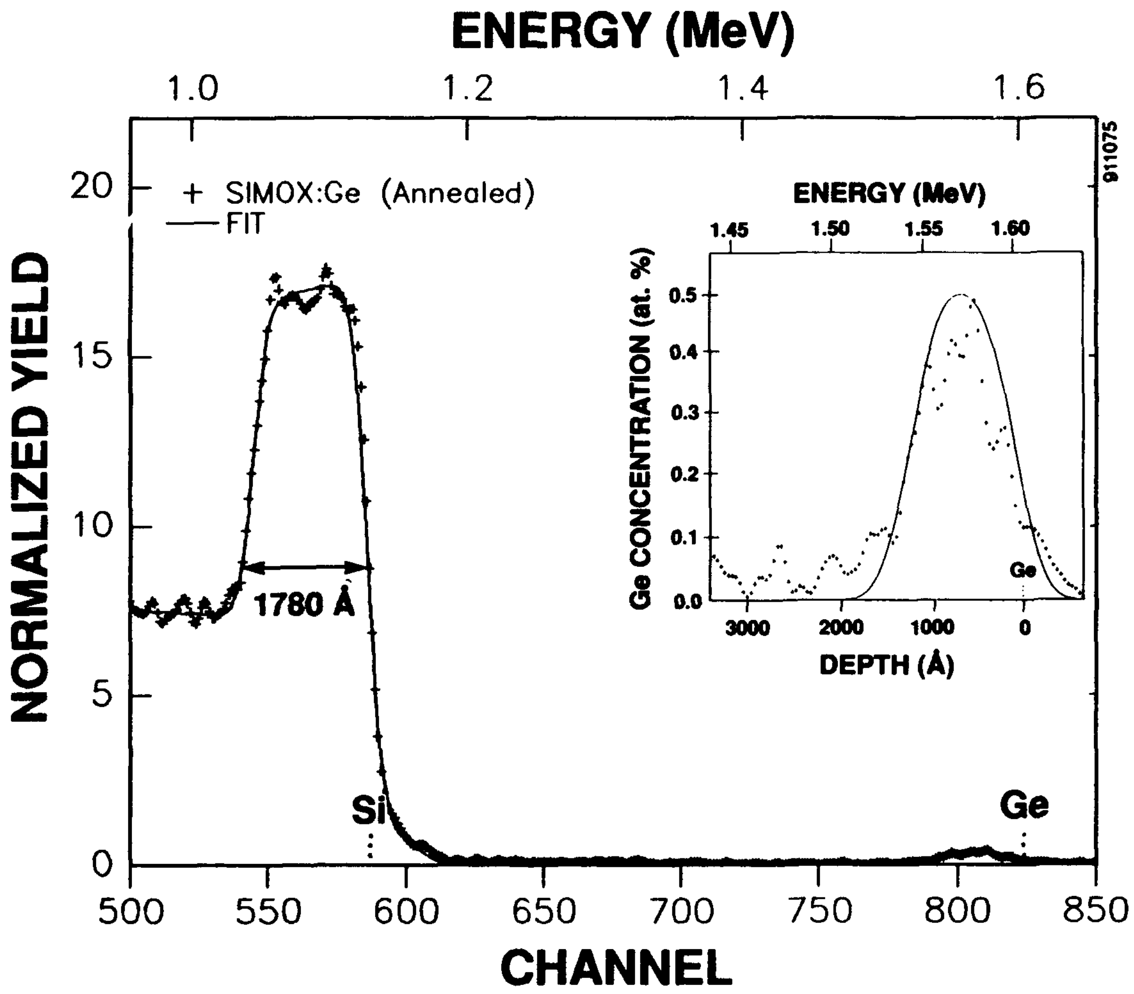


Figure 2-12. *RBS result for a commercial multiple-implant SIMOX sample both Ge-implanted and annealed. A fit to data indicates a Si:Ge layer about 1160Å thick with a peak Ge concentration of 0.5 at.%, formed about 100Å from the surface and 520Å from the upper Si/SiO$_2$ interface.*

Figure 2-13. *XTEM micrograph of a commercial multiple-implant SIMOX wafer both Ge-implanted and annealed. The buried SiO_2 layer is continuous and of good quality, but the Si top layer appears amorphous or poly-crystalline.*

(a)

(b)

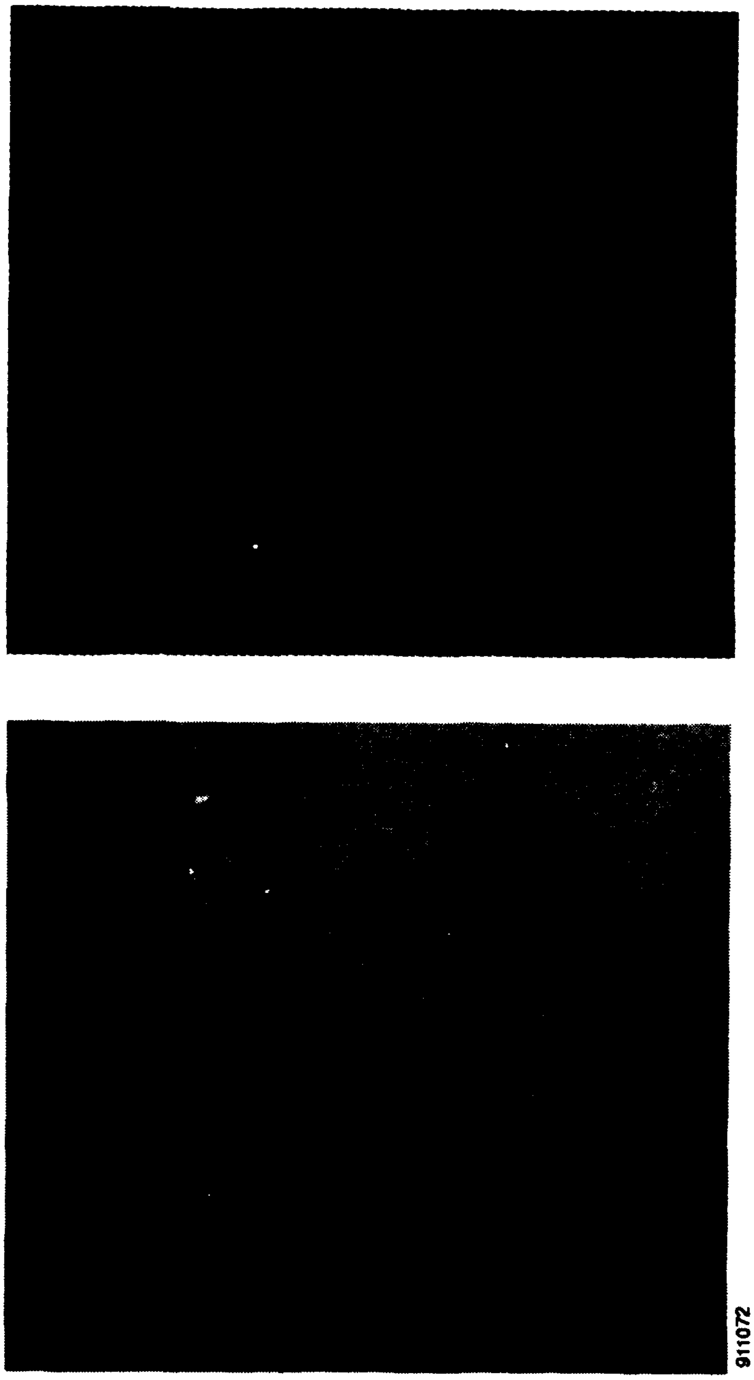


Figure 2-14. *Comparison of the optical micrographs (1000x magnification) from surface of a) commercial multiple-implant SIMOX and b) multiple-implant SIMOX wafer produced at Spire. The surface of the commercial multiple-implant wafer appears to be relatively hazy and rough.*

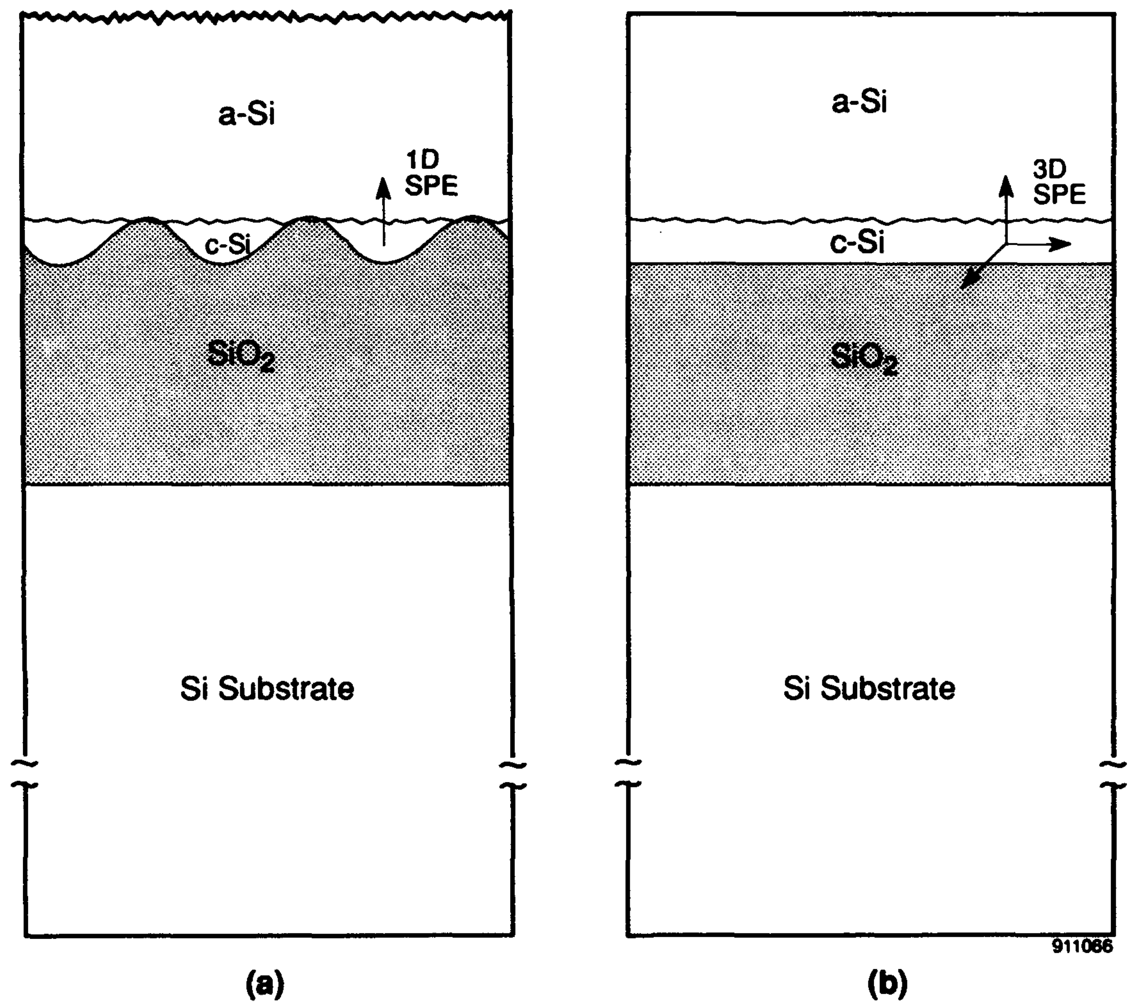


Figure 2-15. *Cross-sectional schematics of Ge-implanted SIMOX wafers with a) wavy upper Si/SiO_2 interface and b) smooth upper Si/SiO_2 interface. Only vertical (1D) recrystallization may be possible in sample a, but the adjacent Si in sample b can recrystallize in all directions (3D).*

adjacent Si vertically. Lateral recrystallization will be inhibited by the surrounding SiO_2 walls. In fact, the scientists from the SIMOX vendor agreed with this hypothesis and further hypothesized that, due to the strain present in these pockets, even the vertically-recrystallized Si may not have the same orientation as the original Si. On the other hand, the sample with a smooth interface and a continuous single-crystal layer (seed) remaining after Ge implantation can recrystallize the adjacent Si in three dimensions, resulting in a single-crystal Si top layer. Thus, a lower Ge implantation energy should be used for multiple-implant SIMOX wafers with wavy upper Si/SiO_2 interfaces rather than for standard SIMOX wafers with similar layer thicknesses.

SECTION 3

ELECTRICAL CHARACTERIZATION

3.1 C-V MEASUREMENTS.

During Phase II, we made several simple test structures and used various techniques to evaluate the effects of Ge implantation on the electrical properties of the back-channel region.

We fabricated several simple test capacitors on p-type SIMOX wafers, with and without Ge implantation, for C-V measurements. These capacitors were formed by a) evaporating aluminum on the p-type SIMOX samples; b) masking and isolating device regions using photolithography; c) removing excess Al; d) selectively etching off the Si top layer using an ethylene-diamine-based mixture, and finally, e) evaporating Al to the back side of the wafer. Figure 3-1 shows a schematic of these test structures. We used a Model 565 MSI Electronics C-V Meter connected to a Hewlett-Packard Model 85B computer and operated at 1 MHz to measure the C-V characteristics.

Figure 3-2 compares the high frequency C-V characteristics for a) p-type standard SIMOX sample without Ge implantation (#T469E), b) a piece of the same SIMOX wafer with 1×10^{15} Ge^+/cm^2 implanted at 80 keV (#T469B), and c) another piece of the same wafer with 1×10^{15} Ge^+/cm^2 implanted at 110 keV (#T469D). The standard single-implant SIMOX wafer (#T469) was produced at Spire by implanting a four-inch p-type Si(100) substrate with an oxygen dose of 1.6×10^{16} O^+/cm^2 at 160 keV followed by annealing for six hours at 1300°C in nitrogen. The Ge-implanted samples were annealed for two hours at 850°C in nitrogen. As shown in Figure 3-2, Ge implantation appears to shift the C-V curve toward the more positive voltage region. In addition, as the implantation energy increases from 80 to 110 keV, a larger positive shift in the C-V curve occurs. These results may be due to the charge-trapping behavior of the defects formed by Ge implantation near the Si/SiO_2 interface.

For more conclusive C-V measurements, we also fabricated new test capacitors with an n-type Si top layer and n-type Si substrate (N-on-N structure) after preparing single-implant SIMOX wafers with n-type substrates. To form the n-type Si top layer, we implanted pieces of the wafer with a dose of 6×10^{14} As^+/cm^2 at 110 keV. The samples were then annealed for 30 minutes at 900°C in N_2 to activate the dopants and remove the implantation damage. We then implanted the Si top layer with a dose of 2×10^{15} Ge^+/cm^2 at 100 keV and annealed the samples for 30 minutes at 850°C in N_2. RBS analyses and results from a surface morphology study of these wafers showed relatively good quality material with the desired layer structure. A fit to the RBS data, shown in Figure 3-3, indicates a Si top layer about 2200Å thick and a buried SiO_2 layer about 3550Å thick.

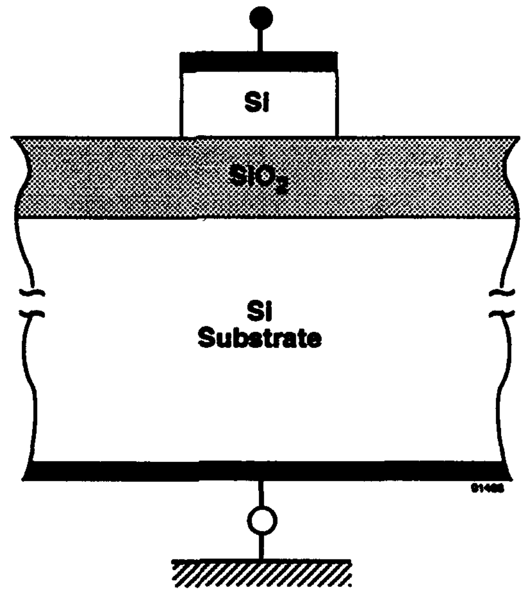


Figure 3-1. *Schematic of test structures used for C-V measurements.*

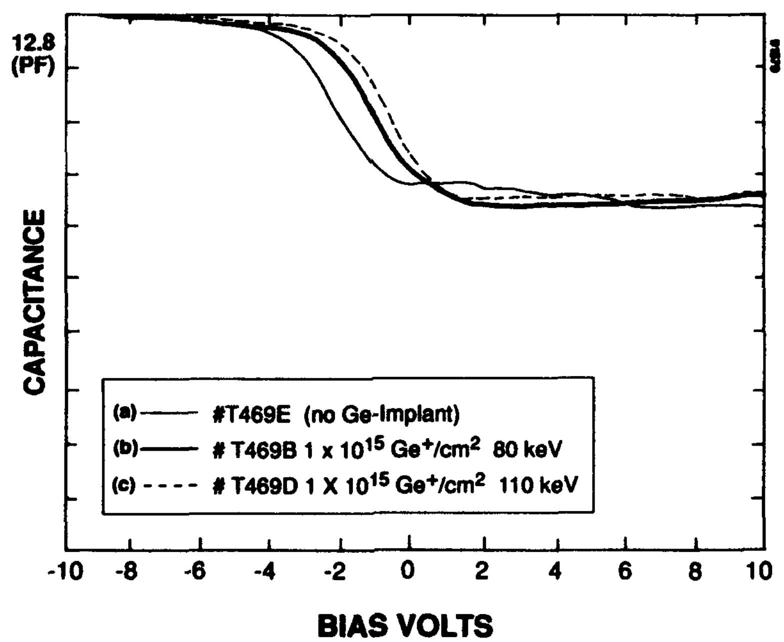


Figure 3-2. *High frequency C-V curves for SIMOX samples a) with no Ge implant (#T469E), b) with 1 x 10^{15} Ge^+/cm^2 implanted at 80 keV (#T469B), and c) with 1 x 10^{15} Ge^+/cm^2 implanted at 110 keV (#T469D). All samples are pieces of the same SIMOX wafer (#T469).*

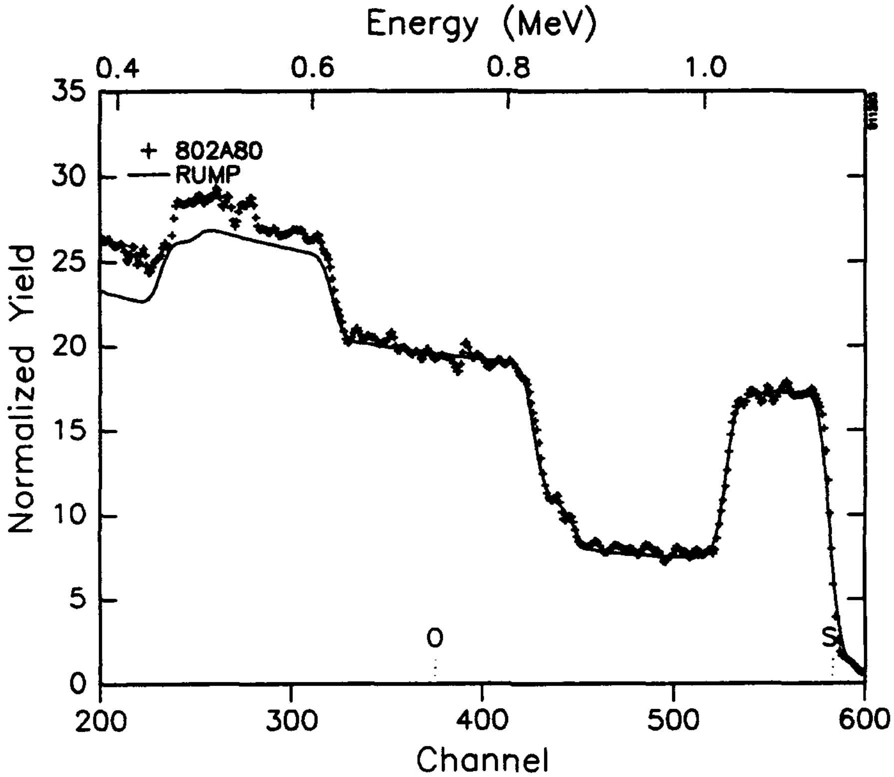


Figure 3-3. *RBS results of the single-implant, n-type standard SIMOX wafer used for C-V characterization. A fit to the RBS results indicates a Si top layer about 2200Å thick and a buried SiO_2 layer about 3550Å thick.*

We fabricated test capacitors on SIMOX samples implanted with As^+ and Ge^+ as well as on samples without any such implantations. To fabricate these devices, we deposited Al onto the samples using an electron-beam evaporator and then photolithographically-masked isolated regions of the samples using a photomask (see Figure 3-4) provided by Dr. Frank Sinclair of Eaton Corporation, Beverly, MA. We then removed the excess Si (regions not masked with Al) using an ethylene-diamine-based preferential etchant at 100°C to form isolated Si top layer regions with Al contacts.

We studied the capacitance-voltage (C-V) characteristics of the devices using a Materials Development Model SCM/16 Semiconductor Measurement System. This system is equipped with a Boonton Model 72C capacitance meter, an MDC model RM-1600 computer, and an MSI Electronics Model WF-2 probe station. For C-V measurements, we first swept the voltage across each capacitor from -100V to +100V and then retraced it by sweeping the bias from +100 to -100 volts.

Figure 3-5 shows the C-V characteristics of capacitors fabricated on SIMOX wafers without As^+ and Ge^+ implantation. The results indicate that the Si substrate is indeed n-type material, but that the Si top layer appears to be p-type. Conversely, the C-V characteristics of devices fabricated on samples implanted with both As^+ and Ge^+ (as shown in Figure 3-6) suggest that the Si top layer has converted to a lightly doped n-type material. In both C-V curves, an unusually large stretch-out exists between the depletion regions of the Si top layer and the Si substrate.

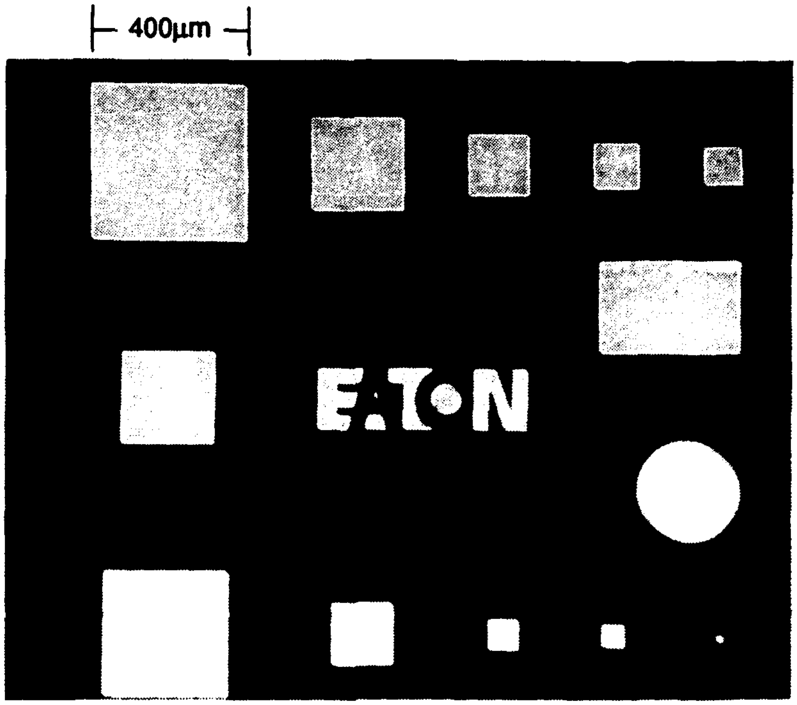


Figure 3-4. *The photomask pattern used for fabricating SIMOX capacitors. The photomask was provided by Dr. Frank Sinclair of Eaton Corporation, Beverly, MA.*

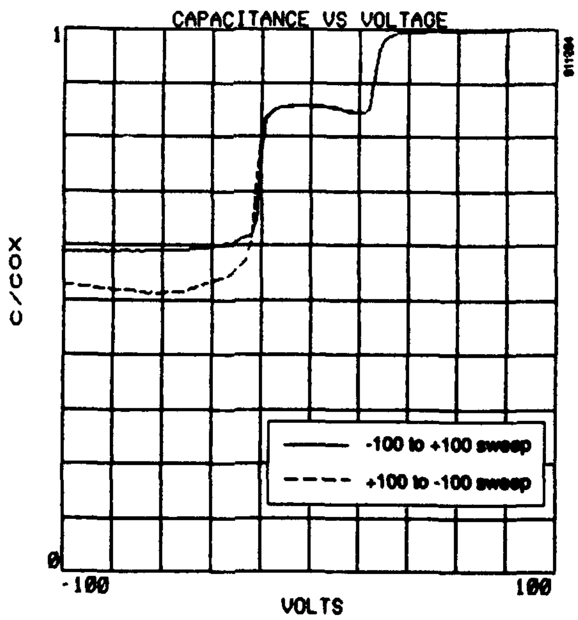


Figure 3-5. *C-V characteristics for as-fabricated SIMOX capacitors without As and Ge implantations. Results indicate an n-type Si substrate and a p-type Si top layer. The stretch-out in the C-V curve suggests process-induced ionizing radiation effects.*

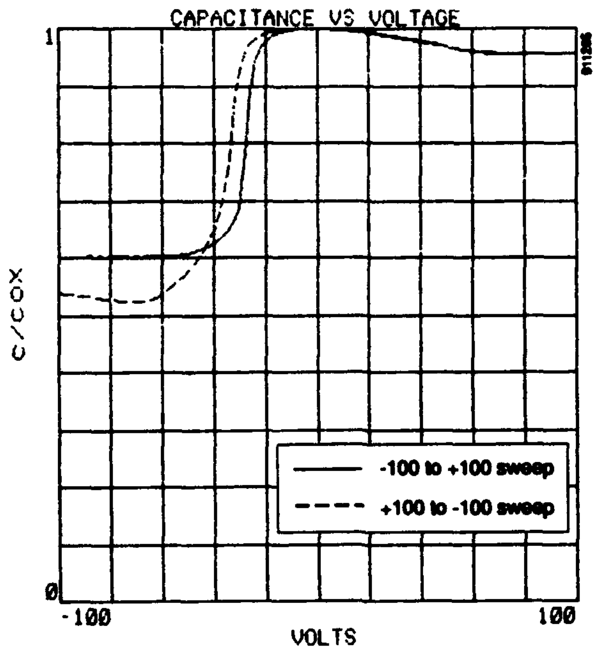


Figure 3-6. *C-V characteristics for as-fabricated SIMOX capacitors implanted with both As and Ge. The results indicate an n-type Si substrate and a lightly doped n-type Si top layer. These results also suggest that the capacitors were irradiated during the fabrication process.*

Since the stretch-out may have resulted from irradiation of the samples by the electron-beam during Al evaporation, we annealed the samples for periods of up to eight hours at an average temperature of about 225°C to remove the irradiation damage.

Figures 3-7 and 3-8 show the C-V characteristics of the same devices used for the measurements in Figures 3-5 and 3-6, respectively, after annealing for eight hours at an average temperature of about 225°C. As shown, annealing results in a significant reduction in the stretch-out of the C-V curves.

By comparing the results shown in Figures 3-5 and 3-7 to the results shown in Figures 3-6 and 3-8, we see that the C-V curve of devices with both As^+ and Ge^+ implants shifts when the direction of the sweeping bias changes, while the C-V curves of devices without As^+ and Ge^+ implants remain relatively stable.

In general, the C-V analyses were not very helpful for quantitatively evaluating the effect of Ge implantation on the electrical properties in the back-channel region of SIMOX wafers. Therefore, we focused our remaining efforts on more suitable characterization techniques.

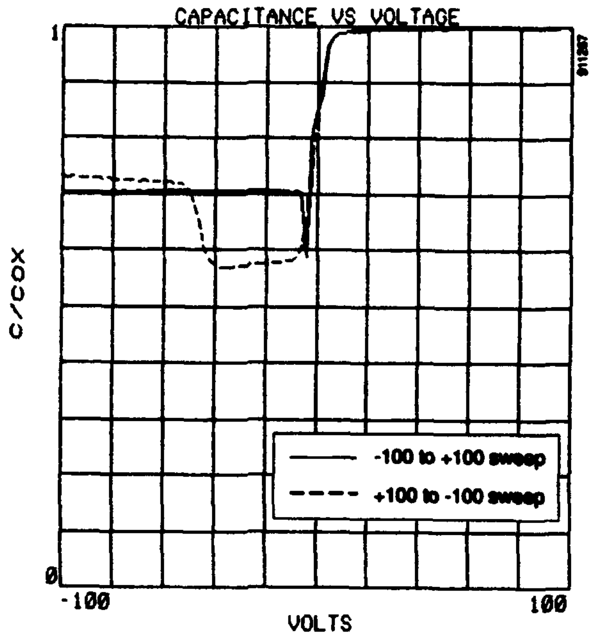


Figure 3-7. *C-V characteristics for capacitors of Figure 3-5 after annealing for eight hours at an average temperature of about 225°C. Annealing resulted in a significant reduction in the C-V curve stretch-out.*

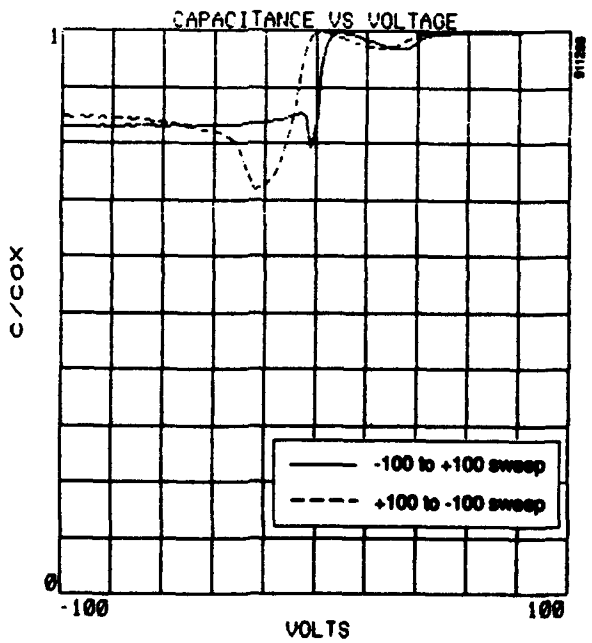


Figure 3-8. *C-V characteristics for capacitors of Figure 3-6 after annealing for eight hours at an average temperature of about 225°C. Again, annealing resulted in a significant reduction in the C-V curve stretch-out.*

3.2 POINT-CONTACT MOS TEST.

We used the point-contact MOS transistor (PCMOST) method to study the electrical properties of Ge-implanted samples in order to characterize and compare their current-voltage (I-V) characteristics with those from unimplanted samples.

We used a standard single-implant SIMOX wafer produced by implanting an oxygen dose of 1.8 x 10^{18} O^+/cm^2 at 200 keV followed by annealing at 1300°C for six hours. Rutherford backscattering spectroscopy (RBS) results for this sample indicated a Si top layer about 2200Å thick and a buried oxide layer about 3550Å thick. We also used a multiple-implant SIMOX wafer with a Si top layer of about 1800Å thick and a buried oxide layer about 4500Å thick.

We then implanted pieces of the above SIMOX wafers with a dose of 2 x 10^{15} Ge^+/cm^2 at 80 keV and annealed them for 30 minutes at 850°C in N_2. These implanted and unimplanted SIMOX pieces were then used for test device fabrication to evaluate the effect of Ge implantation on the electrical properties of the back-channel region. The devices used in this study were fabricated by first thermally evaporating Al on the samples through a shadow mask and then selectively etching off, in a preferential Al etchant (ethylene-diamine-based), the excess Si top layer regions not covered with Al down to the buried oxide layer. Finally, we removed the Al from the remaining isolated Si top layer regions using a phosphoric-acid based mixture.

To perform the PCMOST measurements, two probes were pressure-contacted onto the Si top layer at a distance of about 0.5 mm from each other. A third contact was made to the Si substrate on the back side of the sample. Figure 3-9 shows a diagram of the PCMOST system used at Spire. We used a Hewlett-Packard Model 6113A DC power supply to provide a constant bias to the drain, while a Hewlett-Packard Model 6216B power supply provided the back-gate bias. The current at the source was then measured as a function of the gate bias using a Keithley Model 485A picoammeter. In this study, we applied a 1 volt bias to the drain and varied the gate voltage from -30V to +30V.

We measured the I-V characteristics of several test devices on each sample. The I-V curves obtained from different devices on SIMOX samples without Ge implantation behaved very similarly and resembled a "gull wing" with a minimum current at zero bias (V_G = 0V). Conversely, we recorded two distinct I-V behaviors from devices fabricated on SIMOX wafers with Ge implantation.

Figures 3-10a and 3-10b compare the I-V characteristics of devices fabricated on standard SIMOX samples with and without Ge implantation. As shown, both I-V curves have a minimum current at V_G = 0V, but the leakage current in the device with Ge implantation is generally smaller than that of the unimplanted device, particularly for positive V_G region. Although the I-V curve of the Ge-implanted device still has the "gull wing" shape, the minimum leakage current occurs at V_G = -5V instead of at V_G = 0V.

We obtained similar results for devices fabricated on multiple-implant SIMOX samples with and without Ge implantation. Figures 3-11a and 3-11b compare the I-V curves of a device fabricated on multiple-implant SIMOX without Ge implantation with those from two different devices with Ge implantation. Our results showed that the amount of leakage current in devices

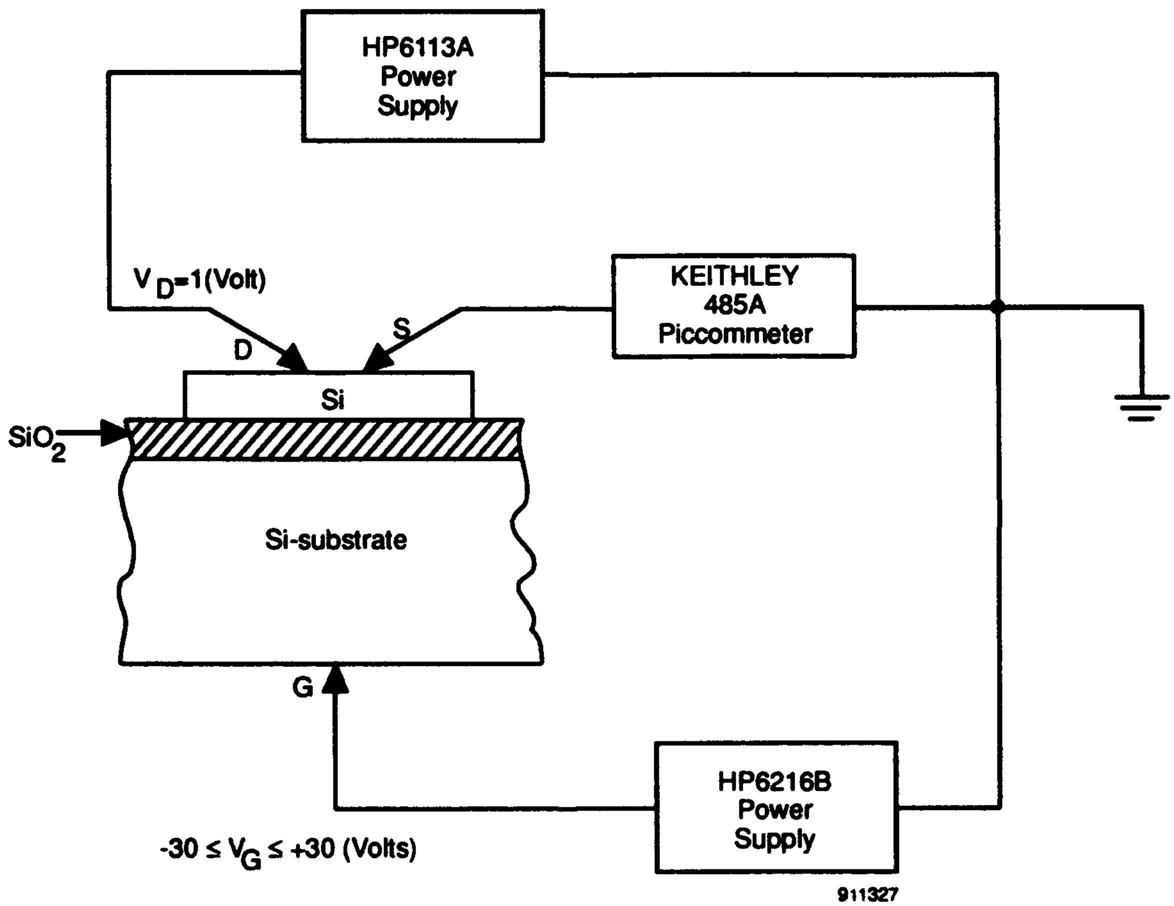


Figure 3-9. *Schematic diagram of the point-contact MOS transistor (PCMOST) measurement system used to study the electrical characteristics of the back-channel region in SIMOX wafers.*

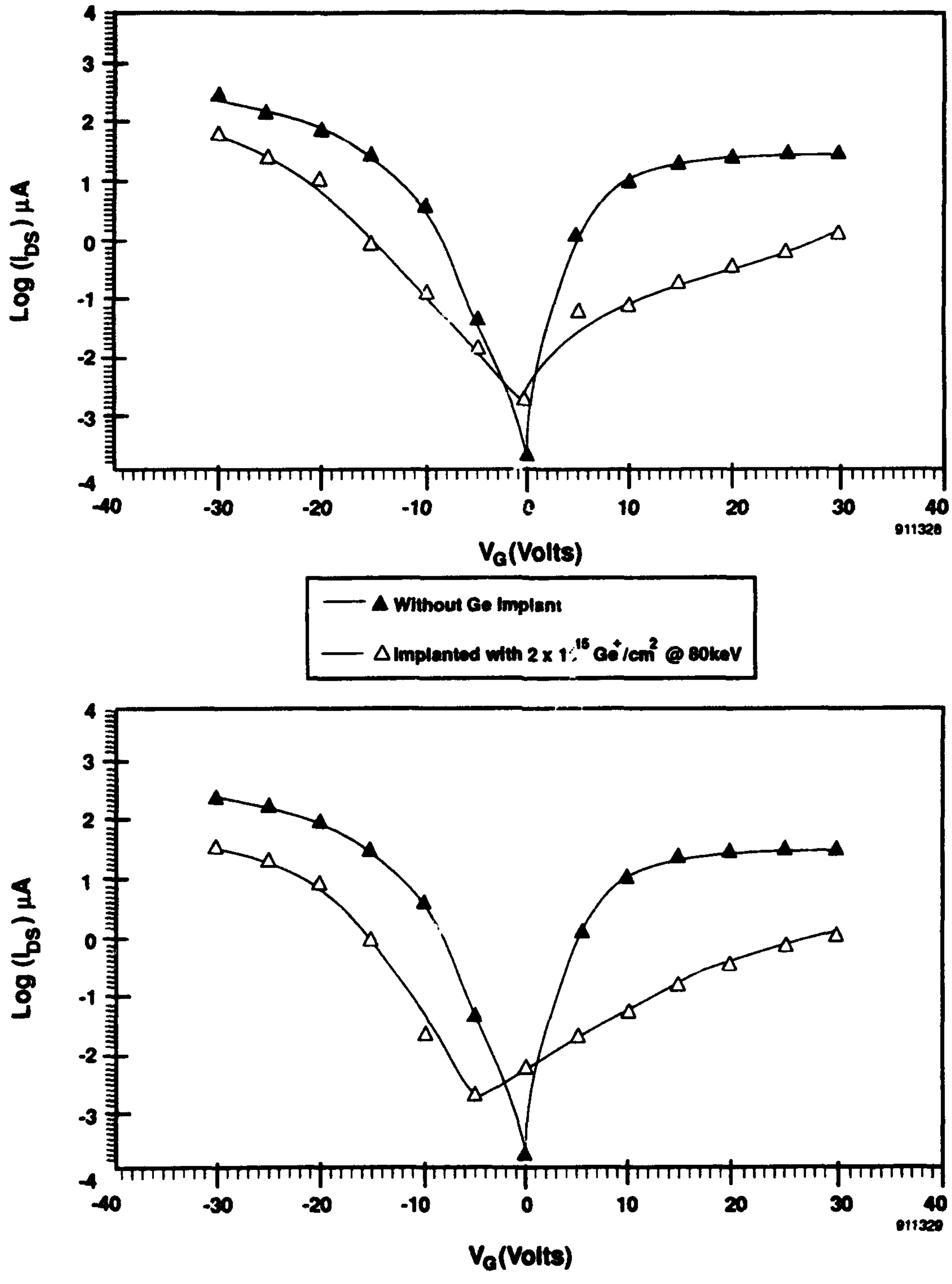


Figure 3-10. *Comparison of the I-V curves of a standard SIMOX PCMOST device without Ge implantation and two different devices from a sample with Ge implantation. The leakage current in Ge-implanted devices is generally smaller than that in non-Ge-implanted devices.*

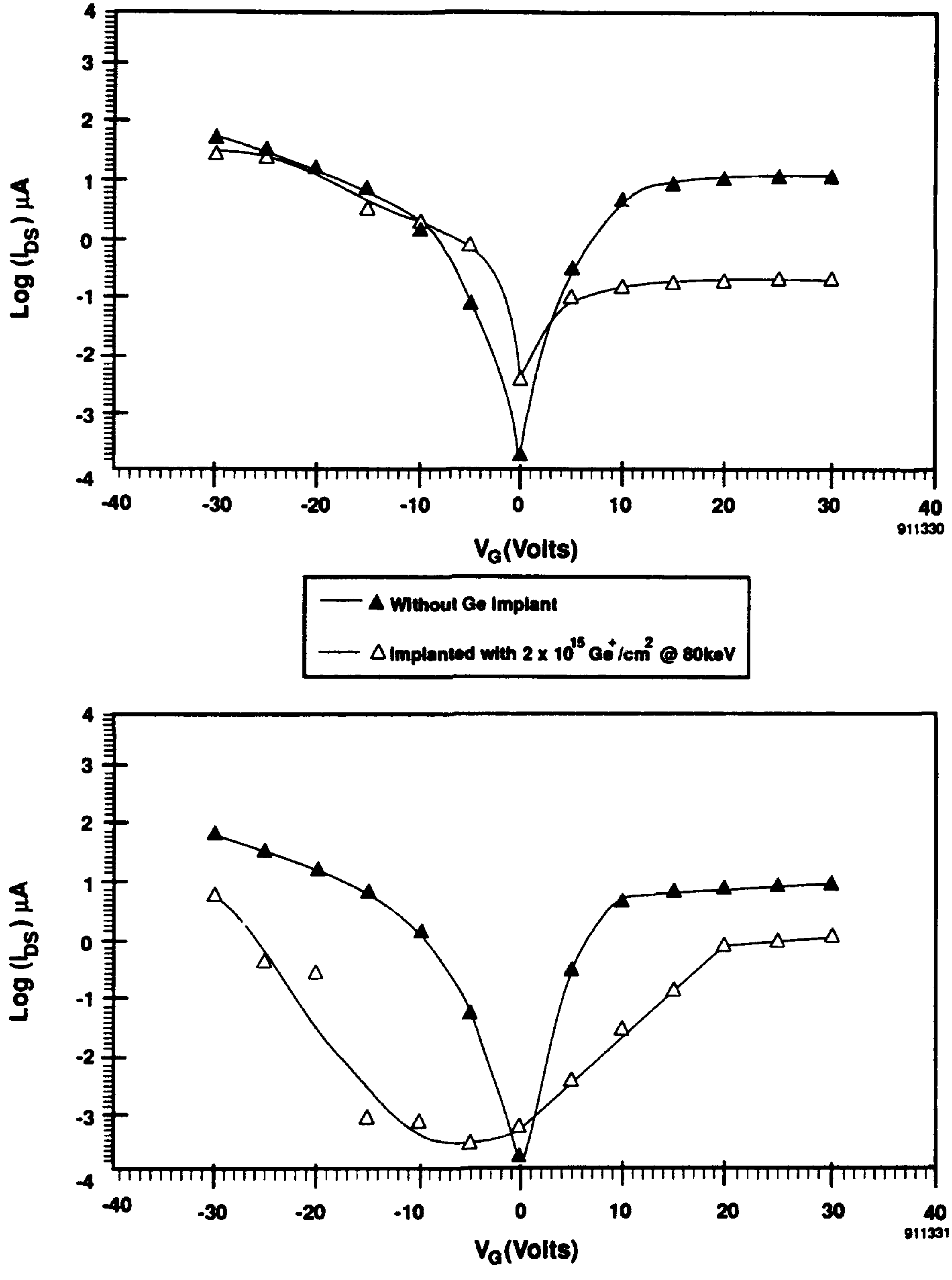


Figure 3-11. *Comparison of the I-V curves of a multiple-implant SIMOX PCMOST device without Ge implantation and two different devices from a sample with Ge implantation. Again, the leakage current in Ge-implanted devices is generally smaller than that in non-Ge-implanted devices.*

with Ge implantation is generally smaller than that for devices without Ge. This supports the concept that Ge implantation can be used effectively for degrading the back-channel region in SIMOX wafers.

3.2.1 Improved Point-Contact MOS Transistor.

The preliminary results of our work in the previous section demonstrated the feasibility of studying the back-channel region using PCMOST. However, the measurement system required various improvements before quantitative data could be recorded. For example, the current-voltage characteristics were to be recorded and plotted continuously using a computer-controlled procedure rather than by measuring drain-to-source current (I_{DS}) at discrete incremental points of applied gate voltage. In addition, the updated system was to enable bipolar sweeping of the voltage.

We concentrated on two directions: 1) improving the PCMOST measurement system and 2) Ge-implanting several standard SIMOX wafers using different implantation conditions as well as fabricating test structures on both Ge-implanted and untreated SIMOX wafers for PCMOST measurements. The layer structures of selected Ge-implanted samples were studied by XTEM.

Figure 3-12 is the schematic of the improved PCMOST measurement system. In this system, a Kepco bipolar operational power supply enables DC voltage sweeping in the range from -20V to +20V, and, vice versa, across the back-gate of the SIMOX test structures. The constant bias of about 1V between the drain and source (V_D) of the PCMOST is provided by an HP6113A DC power supply. Drain-to-source current and the back-gate voltage (V_G) are monitored with a Keithley 485 auto-ranging picoammeter and a Keithley 195A digital multimeter. As shown in the figure, the test equipment and procedures are computer-controlled through IEEE 488 bus lines.

We implanted germanium into three standard SIMOX samples (all from one wafer) with a dose of 3 x 10^{15} Ge^+/cm^2 at energies of 40, 120, and 160 keV. The three samples were then annealed for 30 minutes at 850°C in N_2.

To fabricate the PCMOST test structures, we photolithographically masked the surfaces of the above Ge-implanted samples and a SIMOX sample from the same original wafer but without Ge-implantation. Aluminum was then thermally evaporated onto the samples, and the excess was removed using a lift-off process. The remaining Al masked square regions had a surface area of about 0.25 mm.^{2} Using a preferential etchant, the unmasked Si top layer regions were etched off to expose the buried SiO_2. Finally, all the remaining Al was etched off to create isolated square Si top layer regions for PCMOST measurements (see Figure 3-12).

Figure 3-13 shows the I-V characteristics from a test device on the standard single-implant SIMOX sample without Ge implantation. The solid I-V curve is recorded when V_G is swept from negative to positive voltages, followed by the dashed curve which indicates the I-V behavior when the voltage is swept in the reverse direction. As shown, both curves appear similar with a small current minimum at a V_G value near 0V. However, when a small bias is applied to the back-gate, a large current flows in the back-channel region with a rate (slope of the linear region on the curve) of about 3 decade/V.

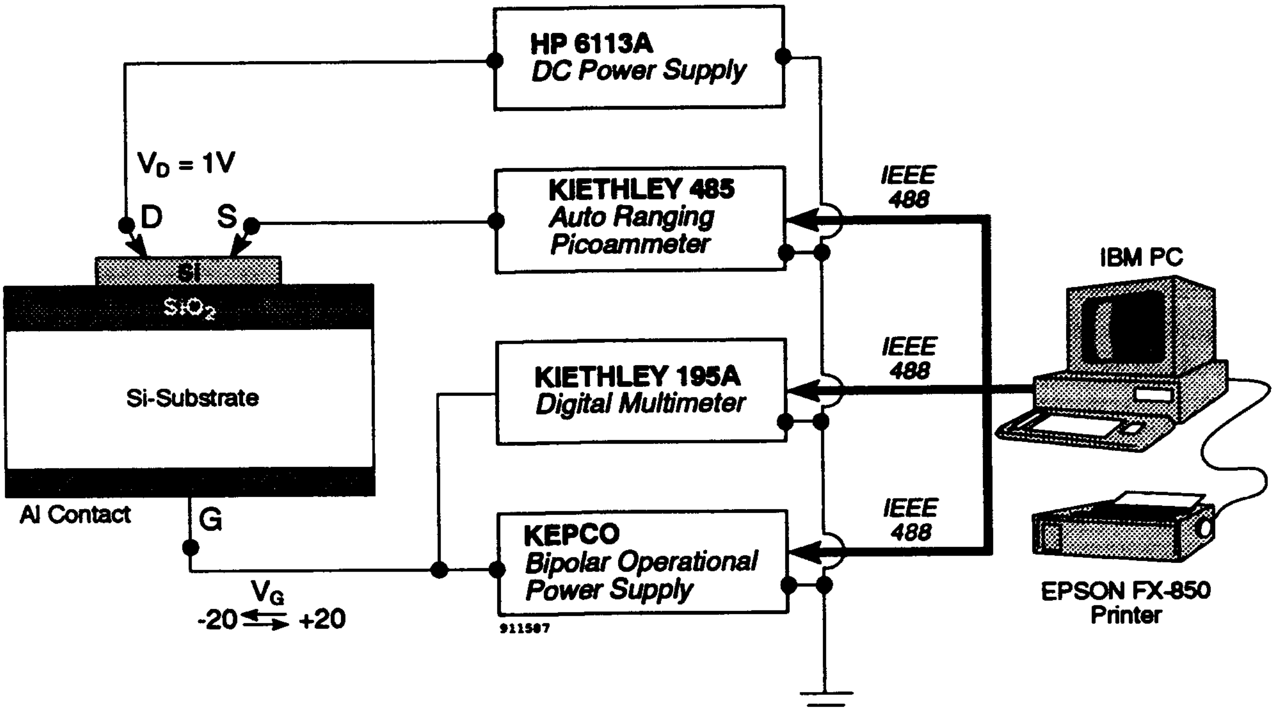


Figure 3-12. *Schematic of the improved point-contact MOS transistor measurement system.*

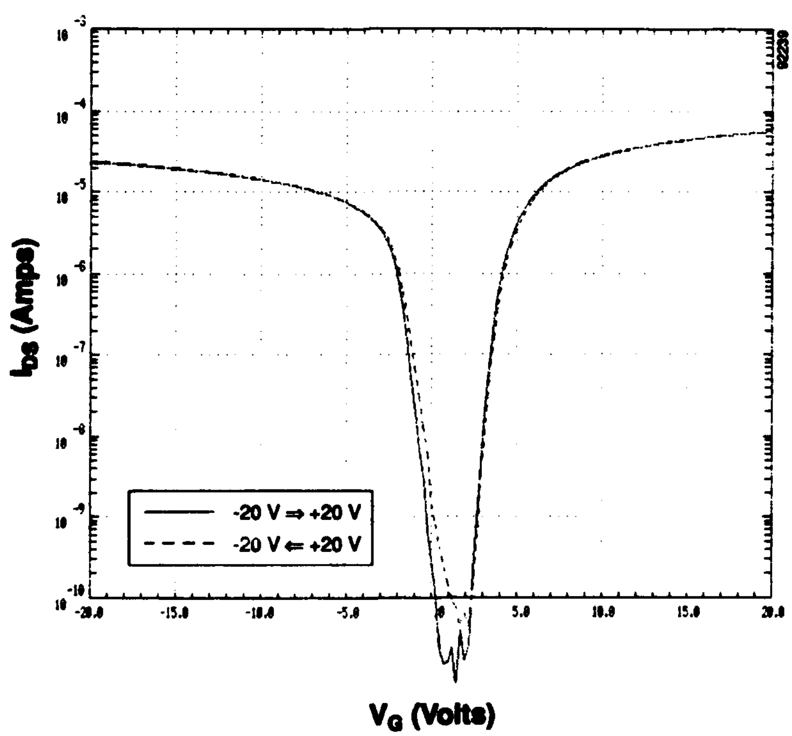


Figure 3-13. *Current-voltage characteristics from a PCMOST structure fabricated on a standard SIMOX sample without Ge implantation.*

Figures 3-14a, 3-15a, and 3-16a show the I-V characteristics of the samples implanted with a Ge dose of 3 x 10^{15} Ge^{+}/cm^{2} at 40, 120, and 160 keV, respectively, and annealed for 30 minutes at 850°C. As shown, several differences exist between these I-V curves and the ones obtained from the sample without Ge implantation. One obvious difference is that when the gate voltage sweep shifts direction, the I-V curve shifts toward the negative voltages. When we discussed these results with Dr. H. Hughes from the Naval Research Laboratories, he speculated that the shift may have resulted from the residual implantation damage caused inadequate post-implantation annealing. He suggested that annealing the samples at a temperature of 1000°C for one hour might eliminate the shift between I-V curves. Therefore, we followed Dr. Hughes advice and tested the I-V characteristics of the reannealed samples. The results of this work will be discussed in the next section.

From the linear regions of the I-V curves shown in Figures 3-14a, 3-15a, and 3-16a, one can also discern that the flow of current in the back-channel region increases at a much slower rate (about 0.75 decade/V) than that measured in Figure 3-13 for the sample without Ge implantation. Significantly, this result may indicate that Ge implantation actually does result in the degradation of the back-channel region, thus inhibiting current leakage channel formation in the back interface.

The I-V curves of the Ge-implanted and non-Ge-implanted samples differ again in that the I_{DS} value at V_G=0 is lower for the sample without Ge than for the Ge-implanted sample. Implanting Ge into the Si top layer and then annealing the wafer may have improved the quality of the Si near the surface layer, enhancing the carrier life-time and, thus, forming a current path near the surface between the source and drain. We have discussed earlier that adequate Ge implantation into the Si top layer of SIMOX wafers may result in bending the threading dislocation defects and stopping their propagation to the surface layer.

3.2.2 Effect of Annealing on PCMOST Characteristics.

As mentioned above, we annealed the Ge-implanted samples for one hour further at 1000°C in N_2 and again measured their PCMOST characteristics. Figures 3-14b, 3-15b, and 3-16b show I-V characteristics of these samples after the second annealing, clearly indicating that the second annealing eliminated the shift between the individual I-V curves (solid and dashed curves) in each sample. However, after the second annealing, a significant change in the location of the minimum I_{DS} appears to occur, shifting to large positive voltage regions. We speculate that some impurities may have contaminated the Si top layer during the second annealing process, thus causing the shift in I-V curves. The large leakage current at V_G = 0 may also be caused by further improvements in the quality of the Si surface layer. As shown, the rate at which the current increases as a function of the applied gate voltage becomes even slower after the second annealing, making it more difficult to control the current path from the back-channel region.

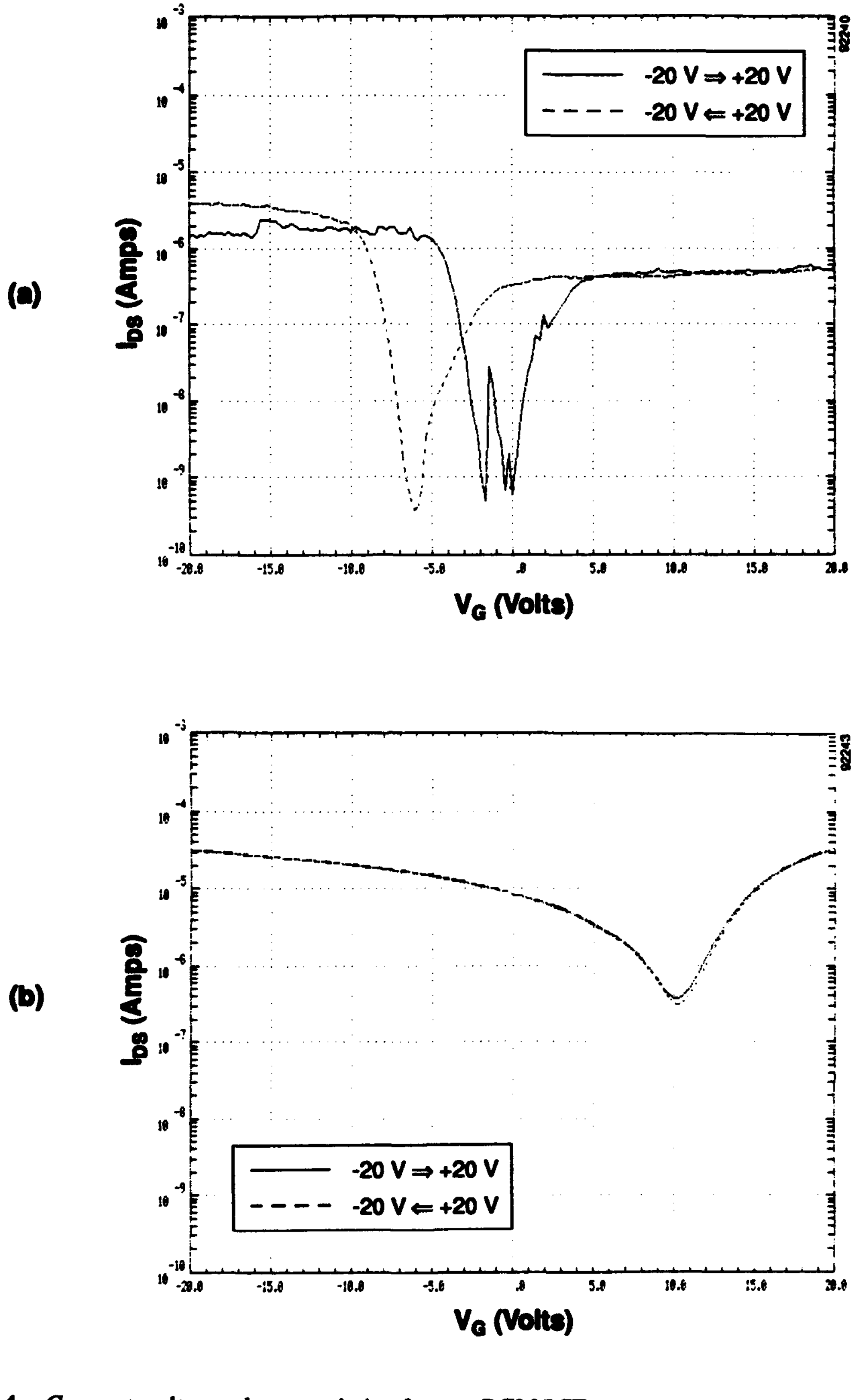


Figure 3-14. *Current-voltage characteristics from a PCMOST structure fabricated on standard SIMOX samples implanted with a dose of $3x10^{15}$ Ge^+/cm^2 at 40 keV and annealed for a) 30 minutes at 850°C in N_2 and b) 30 minutes at 850°C followed by one hour at 1000°C in N_2.*

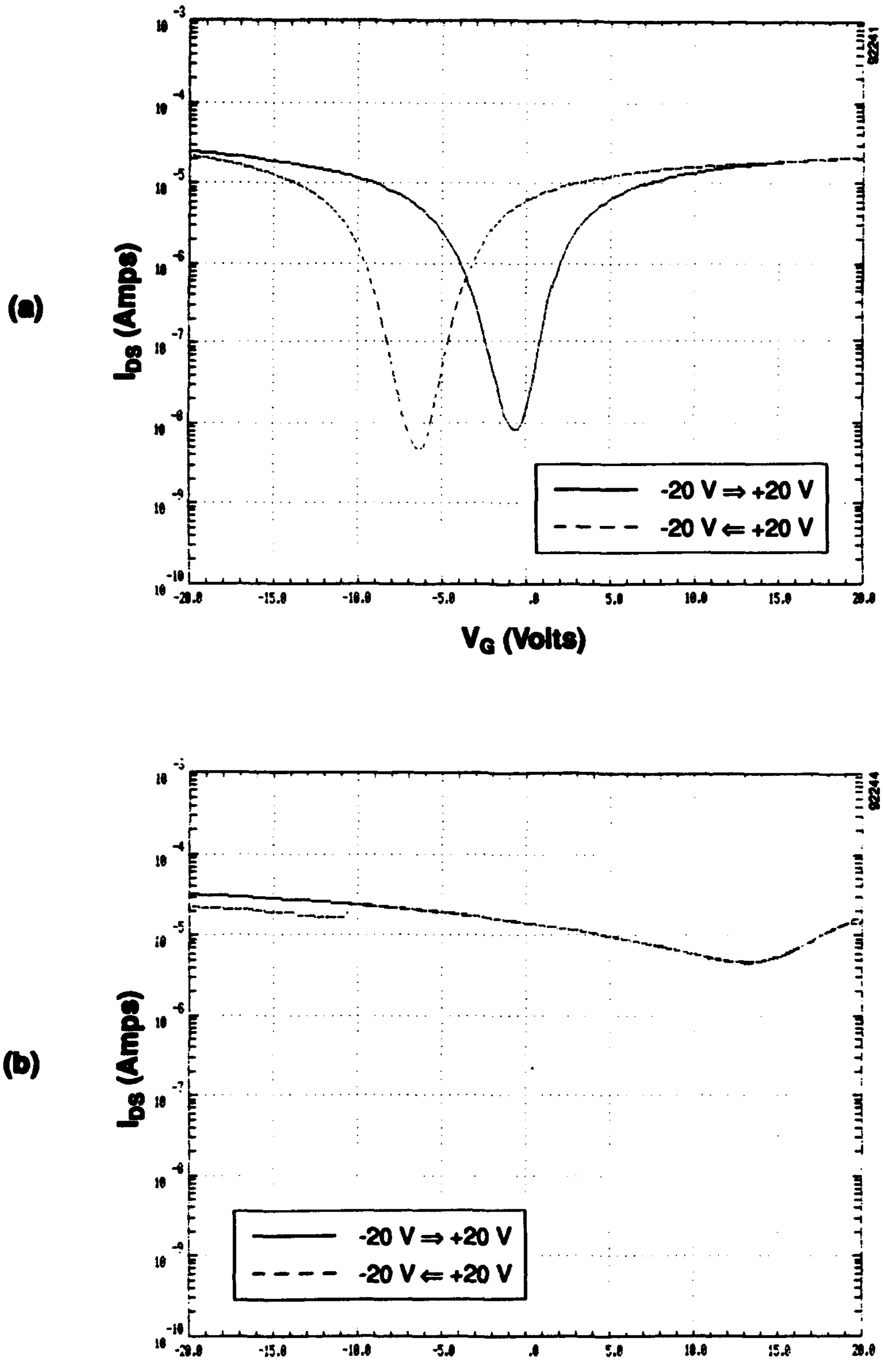
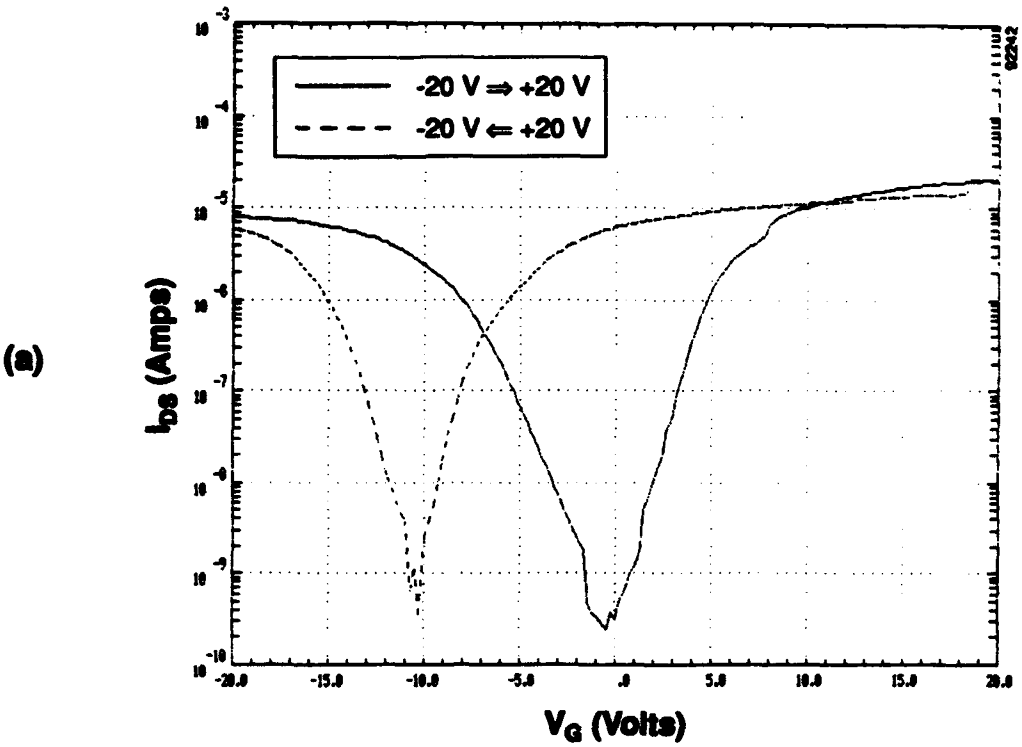


Figure 3-15. *Current-voltage characteristics from a PCMOST structure fabricated on standard SIMOX samples implanted with a dose of 3 x 10^{15} Ge^{+}/cm^{2} at 120 keV and annealed for a) 30 minutes at 850°C in N_2 and b) 30 minutes at 850°C followed by one hour at 1000°C in N_2.*



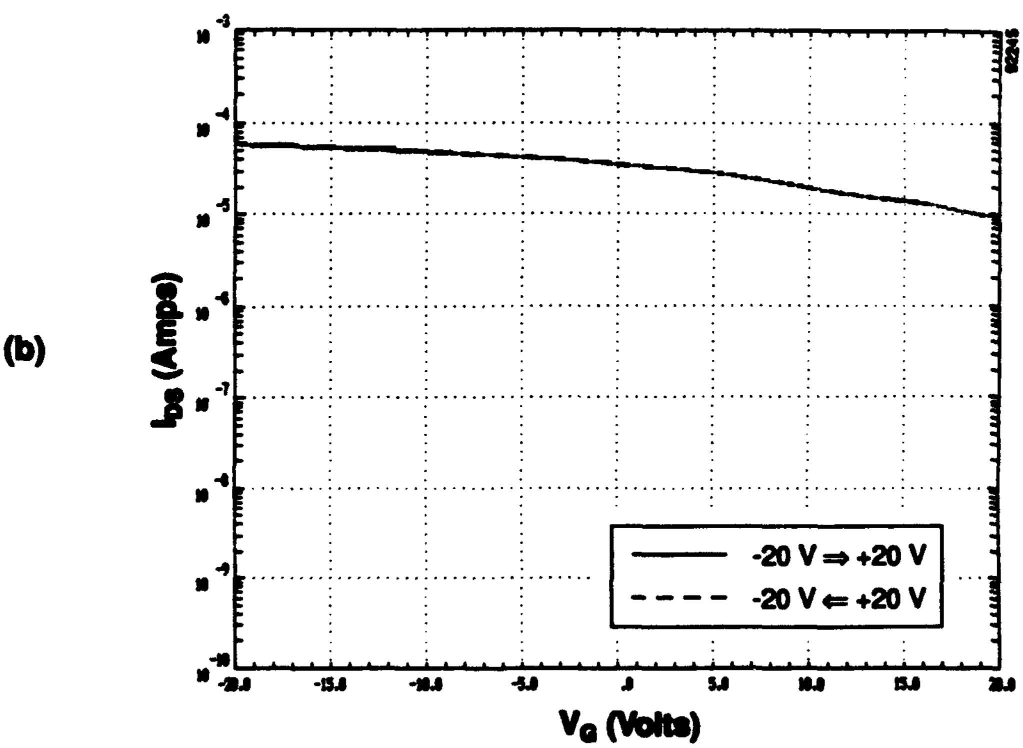


Figure 3-16. *Current-voltage characteristics from a PCMOST structure fabricated on standard SIMOX samples implanted with a dose of $3x10^{15}$ Ge^{+}/cm^{2} at 160 keV and annealed for a) 30 minutes at 850°C in N_2 and b) 30 minutes at 850°C followed by one hour at 1000°C in N_2.*

We implanted additional SIMOX wafers with Ge, fabricated new test structures, and continued to measure PCMOST characteristics to understand better the effects of Ge implantation on the electrical properties of the Si top layer, especially close to the SiO_2 interface region.

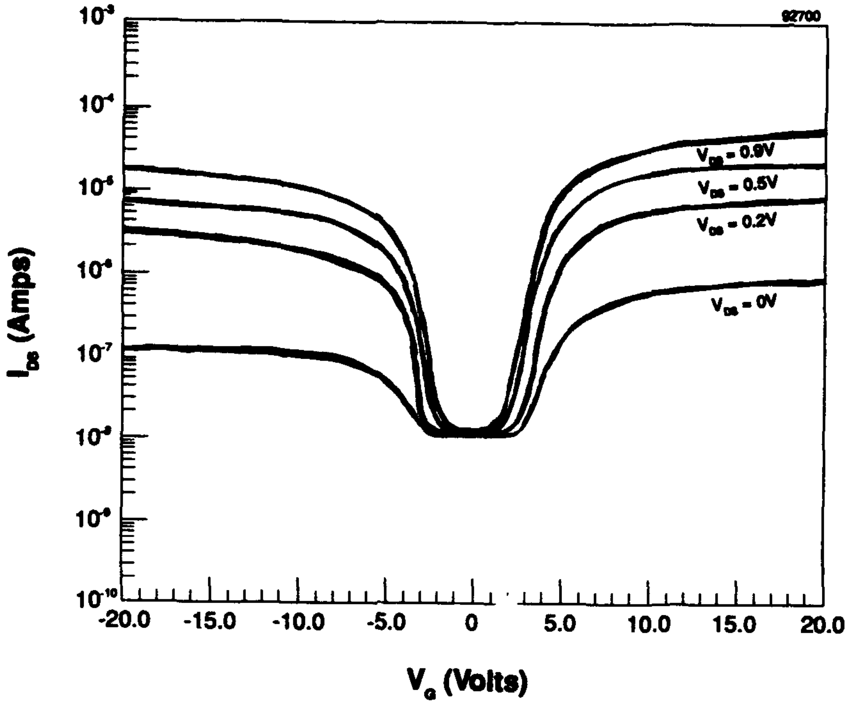
We implanted Ge into samples from two standard SIMOX wafers (#P1047, a p-type <100> wafer and #N1043, an n-type <100> wafer) with a dose of 1 x 10^{16} Ge^+/cm^2 at 160 keV. Both implanted samples were then annealed at 1000°C for one hour. However, one sample (#1043GE) was annealed in N_2 ambient, while the other (#1047GE) was annealed in Ar ambient with about 0.5% O_2 gas flowing.

To fabricate test structures on Ge-implanted samples (#1043GE and #1047GE) and non-Ge-implanted samples (#1043 and #1047), we deposited 5000Å of SiO_2 (instead of Al) onto the surface layer for masking in the EDP silicon etchant. We patterned the samples photolithographically and then placed them in buffer HF solution to remove the oxide from non-device regions and expose the Si. The samples were then etched in EDP solution to remove the Si and expose the buried SiO_2 layer. Finally, the oxide layer covering the isolated Si top layer islands was removed in buffer HF.

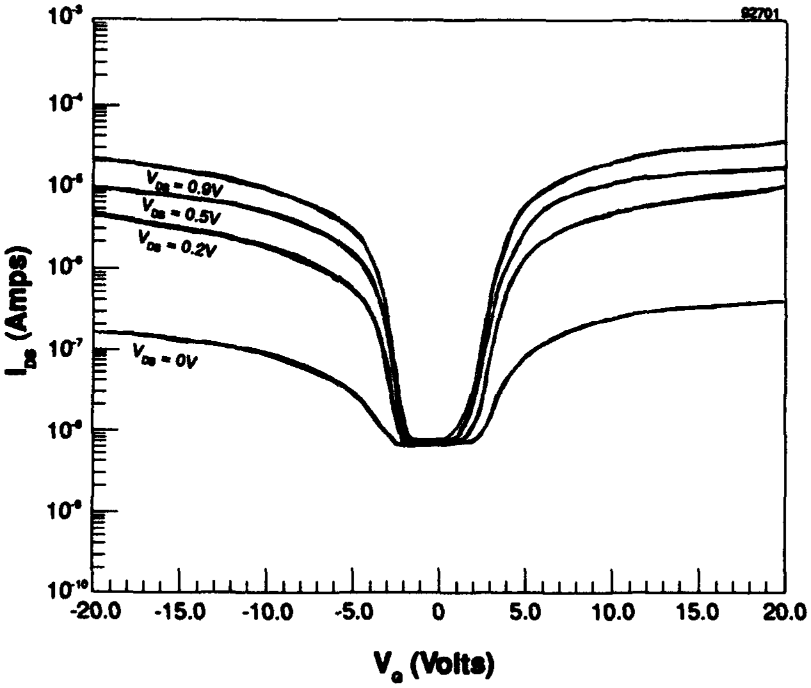
Using our improved PCMOST measurement system, we measured the dependence of drain current I_{DS} on gate voltage V_G, where the Si substrate serves as a gate contact and V_{DS} was taken as an adjustable parameter. Figure 3-17a and 3-178b shows representative PCMOST results obtained from devices fabricated on SIMOX samples without Ge implantation, with V_{DS} adjusted to 0, 0.2, 0.5, and 0.9V. Figure 3-18a and 3-18b, conversely, shows the PCMOST results from Ge-implanted devices with Ar and N_2 anneal ambient, respectively. Despite the difference in annealing ambient, results from the Ge-implanted structures appear similar; however, they reveal several important differences when compared with results for non-Ge-implanted SIMOX structures (Figure 3-17a and 3-17b).

As shown in Figure 3-18a and 3-18b, the I-V curves measured at V_{DS} values above zero (0.2, 0.5 and 0.9V) for Ge-implanted samples typically indicated a minimum I_{DS} at V_G values near 10V and the current leakage increase with the applied V_{DS} for all V_G biases. In the SIMOX samples without Ge implantation (Figure 3-17a and 3-17b), a minimum I_{DS} of about 10 nA occurs at V_G values near zero, regardless of the applied V_{DS} value (though current leakage increases with V_{DS} for other V_G biases).

We observed a most interesting difference in the magnitude of the drain current when comparing devices without and with Ge implantation under zero bias applied between the source and drain (V_{DS} = 0V). The drain current under zero bias can only originate from the gate bias supply through the implanted SiO_2 layer. This very significant accomplishment implies that the parasitic gate leakage current was reduced by more than an order of magnitude due to the Ge implantation. The Ge seems to form a high resistivity region in the Si/SiO_2 interface region, blocking the gate leakage current flow.

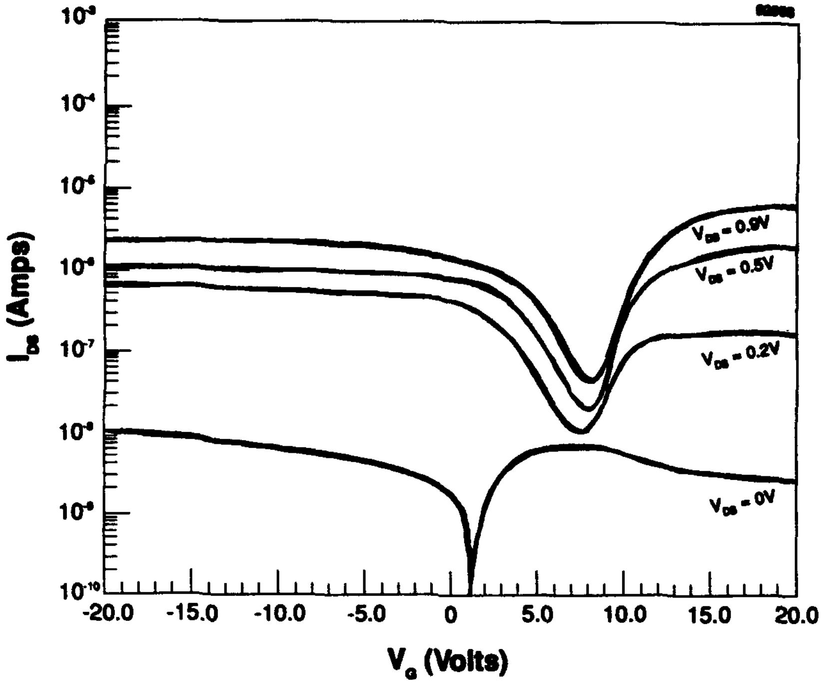


A

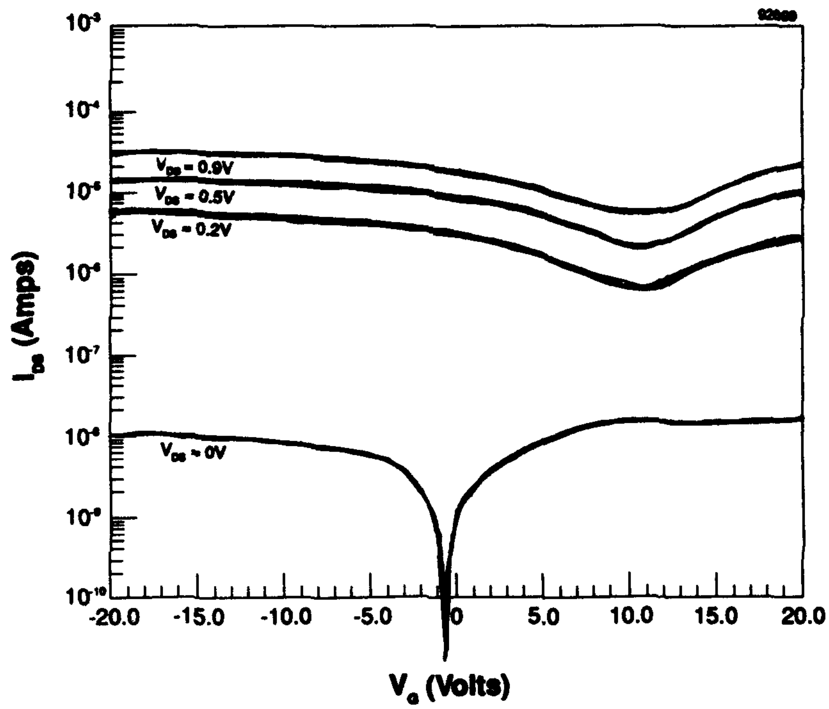


B

Figure 3-17. *PCMOST characteristics of structures fabricated on standard SIMOX samples without Ge implantation: a) sample #1047 and b) sample #1043.*



A



B

Figure 3-18. *PCMOST characteristics of structures fabricated on standard SIMOX samples implanted with a dose of $1x10^{16}$ Ge^{+}/cm^{2} at 160 keV and annealed for one hour at 1000°C in a) argon (sample #1047GE) and b) nitrogen (sample #1043GE).*

Also, Ge implantation seems to create a depletion mode FET. Results shown in Figure 3-18a and 3-18b demonstrates that a hole current can flow between the source and drain even without a gate bias, indicating the presence of an accumulation channel. When the gate bias becomes increasingly positive, this hole current decreases and, in fact, will vanish at gate voltages over +10V. At strong positive biases, electrons accumulate and I_{DS} increases, thus demonstrating a back-channel depletion-mode FET. When measuring the Hall effect in the top Si layer as a function of gate bias, if the mobile carriers change from holes to electrons as V_G exceeds +10V, Hall voltage polarity should be reversed. Furthermore, the measurement provides magnitudes of both electron and hole mobilities, confirming that Ge can improve the crystalline quality of the Si top surface film.

SECTION 4

SUBCONTRACT AGREEMENTS FOR DEVICE FABRICATION

4.1 QUICK TURNAROUND MOSFET DEVICES.

Though we initiated arrangements for a subcontract with Massachusetts Institute of Technology (MIT) Lincoln Laboratories, Lexington MA, for device and circuit processing, no agreement was finalized. However, we did collaborate briefly with Dr. Pramod C. Karulkar to study the effect of Ge implantation on back-channel degradation in SIMOX wafers.

We implanted a three-inch standard SIMOX wafer with a Ge dose of 1×10^{16} Ge^+/cm^2 at 160 keV and annealed it at 1000°C in Ar for one hour, along with another SIMOX wafer without Ge implantation from the same lot. Dr. Karulkar used both wafers for test device fabrication and testing; his preliminary results follow.

The test devices were very simple, quick turnaround MOSFETs fabricated only on small areas of the SIMOX wafers to allow further processing steps and the future use of such wafers. Figure 4-1 shows a schematic for the quick turnaround test MOSFETS. To fabricate these test devices, they patterned the SIMOX wafers and etched the Si mesa. They then applied a photoresist layer as an implantation mask. To form the source and drain, boron was implanted with a dose of 2×10^{15} B^+/cm^2 at 30 keV into the wafers through windows in the photoresist. Finally, the photoresist was removed, and the wafers were annealed for 30 minutes at 900°C. The buried SiO_2 functions as the back-gate oxide and the substrate as the back-gate electrode in this device. During electrical characterization, probes were pressure-contacted to the source, drain, and back gate. No metallization or doping of the channel region was performed.

The C-V measurements of these simple devices seemed to indicate good MOSFET characteristics. Figure 4-2 (a and b) compares the I_D-V_{DS} curves, and Figure 4-3 (a and b) compares the I_D-V_B curves of the two types of devices. The carrier mobilities in the devices' inversion layers (both with and without Ge implantation) appear identical with values of 160 to 200 cm^2/V-S. The kink effect related to the floating body can be observed in the I-V results, especially those from the SIMOX devices without Ge implantation.

4.2 SUBCONTRACT WITH DEVICE PROCESSING INSTITUTION.

Under Dr. Karulkar's direction, MIT Lincoln Laboratory would have fabricated and tested several devices and circuits to evaluate the effect of Ge implantation in reducing back-channel leakage in SIMOX structures. Unfortunately, Lincoln Laboratory was unable to finalize the agreement because of its Air Force contract which prevents it from directly competing with industry or from functioning as a subcontractor on any government contract.

We arranged a subcontract agreement with Prof. James E. Chung of the Dept. of Electrical Engineering and Computer Science at MIT. Under Professor James Chung's supervision, the MIT group would fabricate and test a number of devices and circuits on SIMOX wafers, provided by Spire, in order to determine the effectiveness of Ge implantation for reducing back-channel leakage in NMOS SIMOX devices and for improving radiation hardness.

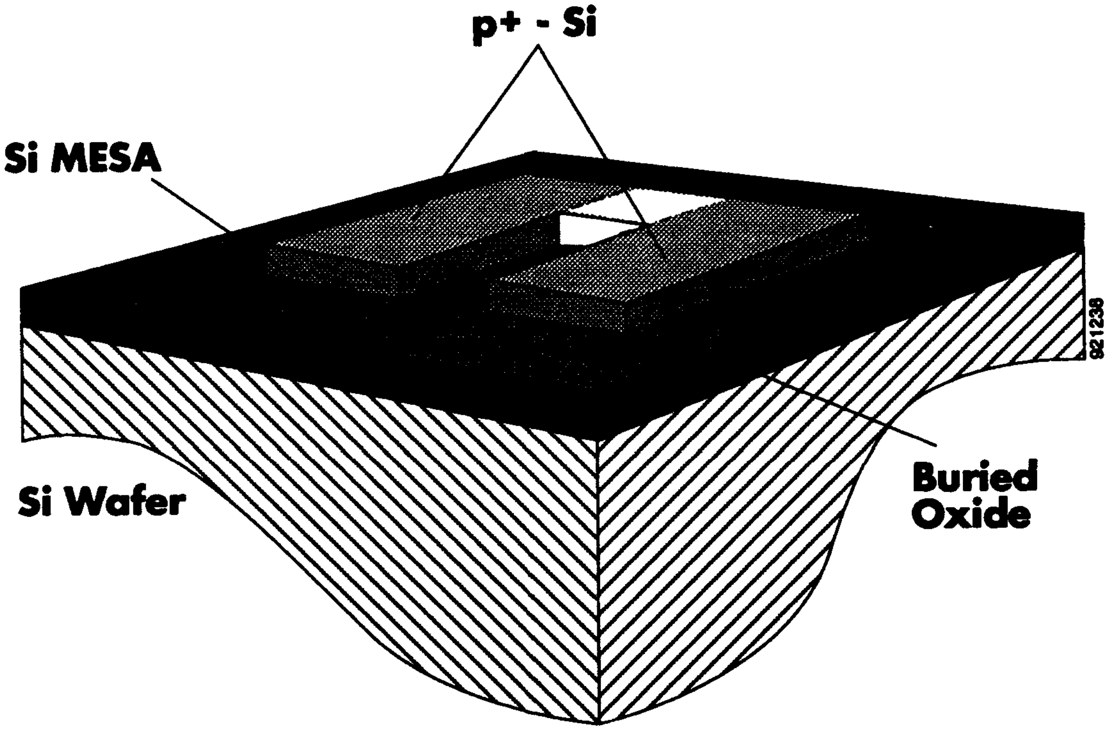


Figure 4-1. *Schematic of the quick turnaround MOSFETs fabricated on SIMOX wafers.*

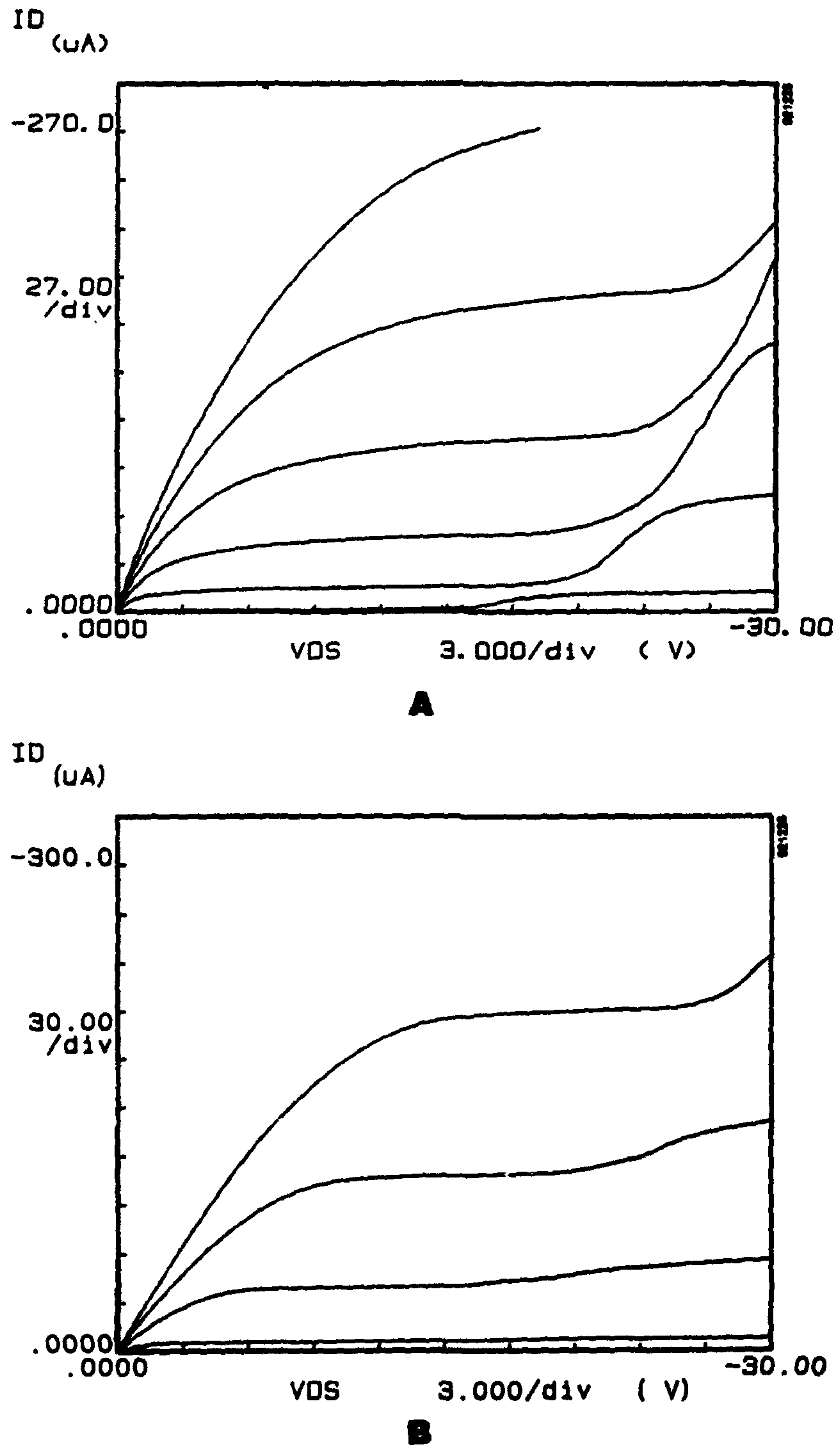


Figure 4-2. *I_D vs. V_{DS} characteristics from quick turnaround devices fabricated on a) SIMOX without Ge implantation and b) SIMOX with Ge implantation.*

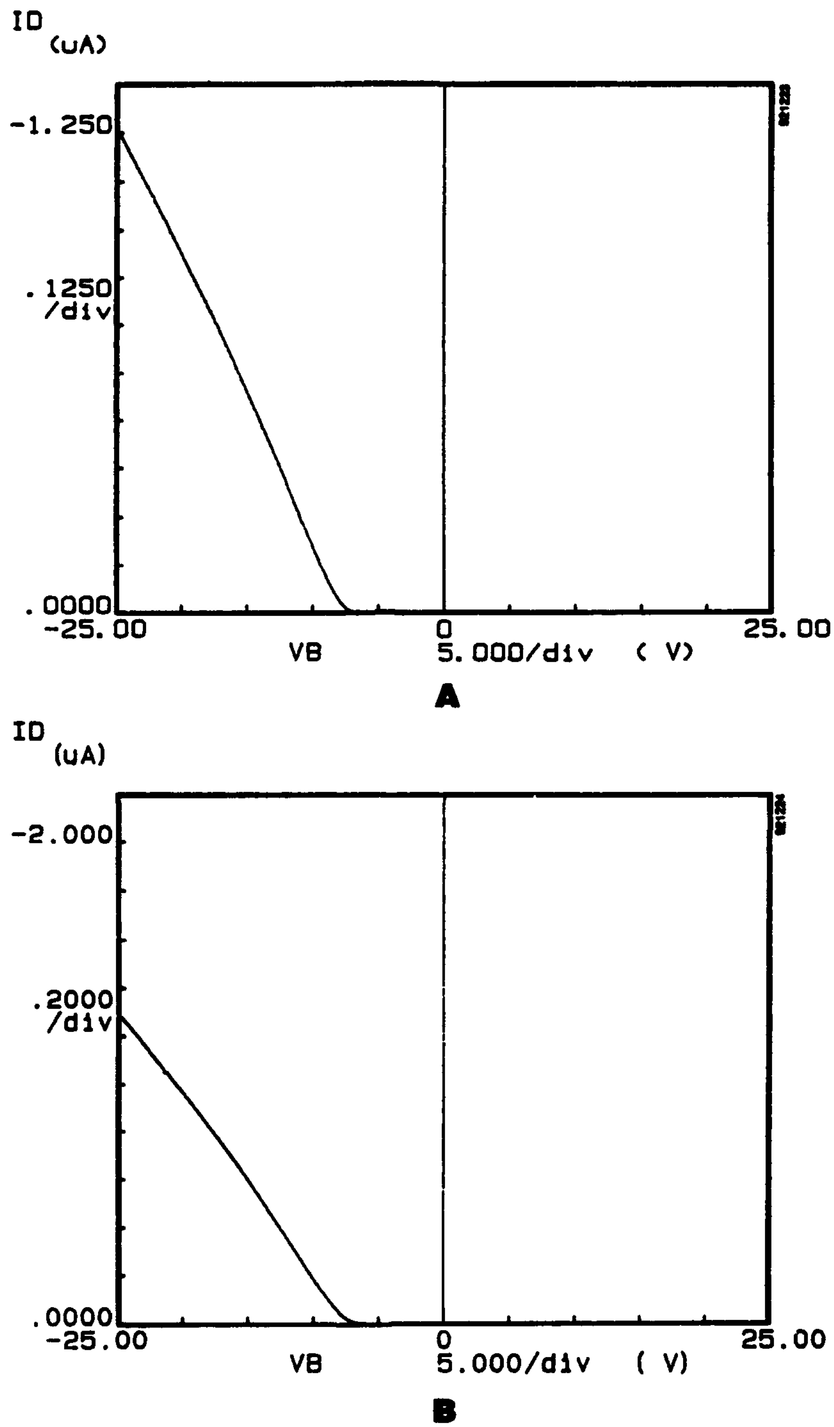


Figure 4-3. *I_D vs. V_B characteristics from quick turnaround devices fabricated on a) SIMOX without Ge implantation and b) SIMOX with Ge implantation.*

SECTION 5

DEVICE FABRICATION

This section includes five pages of information listing the SIMOX and bulk Si samples, as well as the process flow for fabricating Phase II devices at MIT. Below are additional details and explanations of the fabrication steps provided by MIT.

5.1 PREPARATION OF SIMOX WAFERS.

To demonstrate the universality of Ge implantation for improving the performance and radiation hardness of SIMOX devices and circuits, we purchased several four-inch standard single-implant SIMOX wafers from IBIS Corporation and SOITEC USA. All wafers were Ge-implanted at Spire and sent to MIT for device fabrication.

5.2 PROCESS FLOW.

We worked with MIT to generate an appropriate process flow for device fabrication on the above-described wafers. Devices and circuits were fabricated under identical conditions on different non-implanted and Ge-implanted wafers. Results from characterizing and comparing these devices and circuits aided in evaluating the Ge implantation process as a method for 65 reducing back-channel leakage and improving device performance.

Samples were implanted with Ge^+ and annealed under optimum conditions determined by previous studies. In most samples, only half of each wafer was implanted with Ge^+ while the other half was masked during implantation. By fabricating and testing identical devices over each entire wafer surface, we could evaluate the effect of Ge implantation on device performance without risking possible non-uniformities among different sample structures.

We divided the wafers into two groups, the first composed of five wafers and the second of 15. Processing these two sets of wafers differed: the first group was initially implanted with Ge, annealed, and, finally, isolated using the LOCalized Oxidation of Silicon (LOCOS) process, while the second group was first isolated using LOCOS and then received Ge implantation.

Ge was implanted into the device active regions before the gate oxidation step. A fractional-factorial Ge implantation matrix of nine elements, in terms of implant energy, dose, and top Si recrystallization-annealing temperature, was implemented in the device fabrication process in order to optimize the Ge-implant technology. The Ge implant energies used were 120 keV and 150 keV; Ge^+ doses were 10^{15}, 5×10^{15}, and 10^{16} /cm^{-2}; and recrystallization annealing temperatures were at 850°C and 950°C. The matrix elements of 120 keV and annealing temperature of 850°C for all three doses were not included. The total time of recrystallization-annealing, which was performed immediately after the Ge implant, was 30 minutes.

The major thermal cycle after LOCOS consisted of the gate oxidation and source/drain drive-in steps for a total of 70 minutes at 900°C. As substitutional dopants in Si, Ge showed no evidence of redistribution at 850°C.[17] However, at 900°C or higher, the as-implanted Ge profile may have been broadened.

Thus in Phase II, Non-LDD, n-MOSFETs were fabricated on SIMOX wafers, along with bulk control devices. The gate oxide thickness was 120Å, the top silicon thickness was 2000Å, and the buried oxide thickness was 3850Å. The channel doping had three splits: Boron 1.5×10^{15} cm^{-3} (fully depleted), BF_2 7×10^{16} cm^{-3} (partially depleted), and BF_2 $2.1 \times {}^{17}cm^{-3}$ (partially depleted). Devices with body-contacts (H-gate) and edge-less gates were also fabricated.

We measured the layer thicknesses of a wafer from each SIMOX group using Spire's non-destructive optical reflectance analysis. Figures 5-1 and 5-2 show the optical reflectance results from regions near the edge and at the center, respectively, of the SOITEC SIMOX wafer. These results indicate an average Si top layer thickness of about 2095Å and a buried oxide layer thickness of about 3700Å. Figures 5-3 and 5-4 show the optical results measured from regions near and at the center, respectively, of the IBIS wafer. These results indicate an average Si top layer thickness of about 2190Å and a buried oxide layer thickness of about 3800Å. The results shown in Figures 5-1 through 5-4 agree with the layer thicknesses measured at SOITEC (Si=2056Å, SiO_2=3985Å) and IBIS (Si=2190Å, SiO_2=3866Å). The values for layer thickness are useful for determining the appropriate Ge implantation energy to create back-channel defects.

To: PTC
Subject: SIMOX NMOSFET with Ge-implantation process traveler
From: Hua-Fang Wei
Date: December 18, 1992

The purpose of this run is to build Ge-implanted NMOSFETs using SIMOX SOI wafers, with non-fully depleted and fully depleted operation modes. Some starting SOI wafers received Ge implantation in the top Si film. Some starting SOI wafers without Ge-implant will be Ge-implanted after LOCOS is formed. Ge implant will be preformed at SPIRE (only Ge is implanted and only Si substrate is used in that implanter). Ge implantation recrystallization annealing will be done at ICL.

According to previous SiGe work, tube A7 can be used for LTO, B5 for anneal, and B7 for sintering, all after SiGe deposition.

The top target Si thickness is designed to be thickest possible so as to minimize the interaction between the Ge-implant-damaged region and the top channel. Non-fully depleted mode is achieved by channel implant with Boron.

Three Ge-implantation-related process variables are considered in the design of experiment. There are:
Ge implantation dose (D1=1E15 cm^-2, D2=5E15, D3=1E16),
Ge implantation energy (E1 = 150 keV , E2=E1-30 KeV),
After Ge implantation recrystallization annealing temperature (T1=850 C, T2=950 C).
Previous studies indicate D2 and T1 are more favored.
Notation "V" means virgin, or no Ge is implanted, which serves as controller.
Most single wafers have pairs of samples on them in terms of half wafer (divided by '||' sign).
SOI-Wafer # is SOI wafer from Soytech, Ibis # is SOI wafer from IBIS. This run can also compare wafers from different companies.

Experiment Matrix:
(1) Ge implantation before device process:
SOI-Wafer 1: V||D1/E1/T1
SOI-Wafer 2: D2/E2/T1||D2/E1/T1
SOI-Wafer 3: V||D3/E1/T1
Ibis 1, and bulk-wafer 1: V||D2/E1/T1

(2) Ge implantation after LOCOS:
SOI-Wafer 4: V||D1/E1/T1
SOI-Wafer 5: D1/E2/T2||D1/E1/T2
SOI-Wafer 6: D2/E2/T1||D2/E1/T1
Bulk-wafer 2: V||D2/E1/T1
SOI-Wafer 7: D2/E2/T1
SOI-Wafer 8: V||D2/E2/T2
SOI-Wafer 9, Ibis 2, and bulk-wafer 3: V||D2/E1/T2
SOI-Wafer 10 and Ibis 3: V||D3/E1/T1
SOI-Wafer 11: D3/E2/T2||D3/E1/T2
Bulk-wafer 4: D3/E1/T2||D1/E1/T2
Ibis 4: D2/E1/T1||D1/E1/T1

(3) No Ge implantation at all
SOI-Wafer 12: V and no T1/T2

Note: All virgin half wafers (no Ge implantation) also receive the after Ge implantation annealling the other half wafers receive.
SOI-Wafer 7 is the duplication since the combination of D2 and T1 are important.
A full factorial experiment of D, E, and T will yield 12 total. In the design above the combinations of D1/E2/T1 and D3/E2/T1 are not included.

SIX MASK NMOSFET PROCESS FOR 0.5 MICRON CHANNEL LENGTH SOI DEVICES

LOT # __spire__ LOT OWNER _Hua-Fang Wei_

RESISTIVITY __10-20_ ohm-cm TOTAL NUMBER OF WAFERS:16 simoxs,4 bulks,13 dummies

STARTING SIMOX SOI WAFER: P-Si(2245 A)/SiO2(3794 A)/P-Si (Boron doped,2.5E14 cm^-3)
STARTING BULK WAFER: P SUBSTRATE (Boron doped, 2.5E14 cm^-3)

* indicates a step which needs to be modified from the NMOS baseline opset

```
STEP #     STEP DESCRIPTION                     STATUS
------     ----------------                     ------

1          Ge implantation for 4 wafers (done at SPIRE)

2          Recrystallization anneal             Number wafers ________
           850 C, 30 min, B5              Opset start ________
           recipe needs to be created           Opset finish ________

3*         Stress Relief Oxide                  Number wafers ________
           dsro220.set (recipe 230/A1)          Opset start ________
           (950C, 38.75min in DryO2             Opset finish ________
            950C, 30min in N2)
           Dummy #1 in for SRO monitoring, out
           Dummies #2,3 in; dummy #4 in, out

4            LPCVD Silicon Nitride              Number wafers ________
           dnit1.5k.set (recipe 410/A5)         Opset start ________
           (800C, 2hr)                    Opset finish ________
           Dummies #2,3 for Nitride monitoring,out

5          Active Area Pattern                  Number wafers ________
           phfieldsor.set                       Opset start ________
           (Mask: SOI CD                        Opset finish ________
            Job: ICL CWR1)

6          Nitride Plasma Etch                  Number wafers ________
           plnit1.5k.set                        Opset start ________
           Dummy #2 in, for etch monitoring, out      Opset finish ________

7          P-Field Implant (p-bulk)             Number wafers ________
           ipfieldlsu.set                       Opset start ________
           (Boron, 3E13, 25 keV)                Opset finish ________
           dummy #4 and its twin in, out

8          Resist Ash                     Number wafers ________
           ash.set                        Opset start ________
                                          Opset finish ________

9*         Field Oxide                          Number wafers ________
           (fox+SRO:t1 A SiO2)
           t1=11 0%(2245/.45)
           t1 is measured from dummy #4
           dsfox.set (recipe 114/B1 or B2)            Opset start ________
           (950C, 30min in DryO2                Opset finish ________
            950C, time min in WetO2             time is so decided to yield t1 A
```

SiO2
950C, 30min in DryO2
950C, 30min in N2)
Dummy #4 in for fox monitoring, out

10 Nitride Wet Etch Number wafers ______
wnit1.5k.set Opset start ______
Dummy #3 in for etch monitoring, out Opset finish ______

11 Stress Relief Oxide Wet Etch Number wafers ______
wsro220.set Opset start ______
Opset finish ______
Dummy #1 in for SRO etch monitoring, out

12* Dummy Gate Oxide Growth Number wafers ______
dgate120.set (recipe 112/A2) Opset start ______
(900C, 25min in DryO2 Opset finish ______
900C, 25min in N2)
Dummy #5 in for oxide monitoring, out
Dummies #6 & #7 in, out

****************(repeat 13,14,15 for implant splits)************************

13* Channel Implant Pattern Number wafers ______
phchannel.set Opset start ______
(Mask: no mask Opset finish ______
Job: LSU,4 for HI vt)
LSU,9 for MED vt)
Decide channel implant dose now using known dummy oxide thickness and SUPREM, so as to have non-fully depleted mode for higher dose implants, lower dose implant and intrinsic are fully depleted modes.

14* Channel Implant Number wafers ______
ipvtlsu.set Opset start ______
(BF2, 40keV, 3E12 for HI vt) Opset finish ______
(BF2, 40keV, 1E12 for MED vt)
(no implants for low vt)
Dummies #6 & #7 in, out

15 Resist Ash Number wafers ______
ash.set Opset start ______
Opset finish ______

****************(repeat 13,14,15 for implant splits)******************

16 Dummy Gate Wet Etch Number wafers ______
wgate120.set Opset start ______
Dummy #5 in for etch monitoring, out Opset finish ______
Dummies #6 & #7 in

17* Gate Oxide Number wafers ______
dgate109.set (recipe 112/A2) Opset start ______
(900C, 25min in DryO2 Opset finish ______
900C, 25min in N2)
Dummies #6 & #7 out
Dummies #8 & #9 in for oxide monitoring
Dummy #10 in, out

18* LPCVD Polysilicon Number wafers ______
poly3k.set (recipe 428/A6) Opset start ______
(625C) Opset finish ______
Dummies #8 & #9 for poly monitoring, out
Dummy #11 in, out

19	Poly Gate Pattern phpoly1su.set (Mask: SOI CP Job: ICL CD1)	Number wafers ______ Opset start ______ Opset finish ______
20	Plasma Poly Etch plpoly3k.set Dummy #8 in for etch monitoring, out	Number wafers ______ Opset start ______ Opset finish ______
21	Resist Ash ash.set	Number wafers ______ Opset start ______ Opset finish ______
22	N+ Poly/S/D Pattern phn+1su.set (Mask: SOI CN+ Job: ICL CP1)	Number wafers ______ Opset start ______ Opset finish ______
23*	Poly And S/D Implant inpsdhao.set (As: 25kev,4e15) Dummies #10 & #11 in, out	Number wafers ______ Opset start ______ Opset finish ______
24	Resist Ash ash.set	Number wafers ______ Opset start ______ Opset finish ______
25	P+ Poly/S/D Pattern pp+1su.set (Mask: SOI CP+ Job: ICL CD1)	Number wafers ______ Opset start ______ Opset finish ______
26*	P+ Sub Contact Implant innsd1su.set (BF2: 25kev,4e15) Dummy #9 in, out	Number wafers ______ Opset start ______ Opset finish ______
27	Resist Ash ash.set	Number wafers ______ Opset start ______ Opset finish ______
28*	Poly And S/D Diffusion ddrivehao.set (recipe 113/B5) (900C, 15min in Dry O2) (900C, 5 min in N2) Dummies #6,#7,#9,#10 & #11 in,out Dummy #10 for oxide increase (beyond gate oxide) monitoring	Number wafers ______ Opset start ______ Opset finish ______
29*	LTO Deposition dlto4k.set (recipe 437/A7, 400C) Dummies #12 &#13 in for LTO monitoring	Number wafers ______ Opset start ______ Opset finish ______
30	LTO densification dann.set (recipe 806/B5) (950C, 30min in N2) Dummies #12 & #13 out Dummies #6,#7,#9,#10 & #11 in,out	Number wafers ______ Opset start ______ Opset finish ______
31	Resist Coat phcoat.set	Number wafers ______ Opset start ______ Opset finish ______
32	Backside LTO Wet Etch	Number wafers ______

	wlto4k.set	Opset start ________
		Opset finish ________
	Dummies #6 & #7 in for channel doping monitoring, out	
	Dummy #9 in for P + sub contact doping monitoring, out	
	Dummy #10 in for S/D doping monitoring, out	
	Dummy #11 in for poly doping monitoring, out	
33	Backside Poly Plasma Etch	Number wafers ________
	plpoly3k.set	Opset start ________
	(CCL4, 45sec/8sec)	Opset finish ________
34	Backside Oxide Wet Etch	Number wafers ________
	wox5k.set	Opset start ________
		Opset finish ________
35	Resist Ash	Number wafers ________
	ash.set	Opset start ________
		Opset finish ________
36	Contact Pattern	Number wafers ________
	phconthao.set	Opset start ________
	(Mask: SOI CC	Opset finish ________
	Job: ICL CP1)	
37	LTO Plasma Etch	Number wafers ________
	pllto4k.set	Opset start ________
	(CF4)	Opset finish ________
	Dummies #12 & #13 in for etch monitoring	
38	LTO Wet Etch	Number wafers ________
	wlto4k.set	Opset start ________
		Opset finish ________
	Dummies #12 & #13 for etch monitoring, out	
39	Resist Ash	Number wafers ________
	ash.set	Opset start ________
		Opset finish ________
40	Metal Deposition (Al)	Number wafers ________
	cvclugc.set	Opset start ________
	(Use Varian.set)	Opset finish ________
	Dummy #14 in for metal monitoring, out	
41	Metal Pattern	Number wafers ________
	phmetlsu.set	Opset start ________
	(Mask: SOI CM1	Opset finish ________
	Job: ICL CC)	
42	Metal Plasma Etch	Number wafers ________
	plmetal.set	Opset start ________
		Opset finish ________
43	Resist Ash	Number wafers ________
	ash.set	Opset start ________
		Opset finish ________
44	Sinter Metal	Number wafers ________
	dsinter.set (recipe 710/B8)	Opset start ________
	(400C, 40min in H2+N2)	Opset finish ________

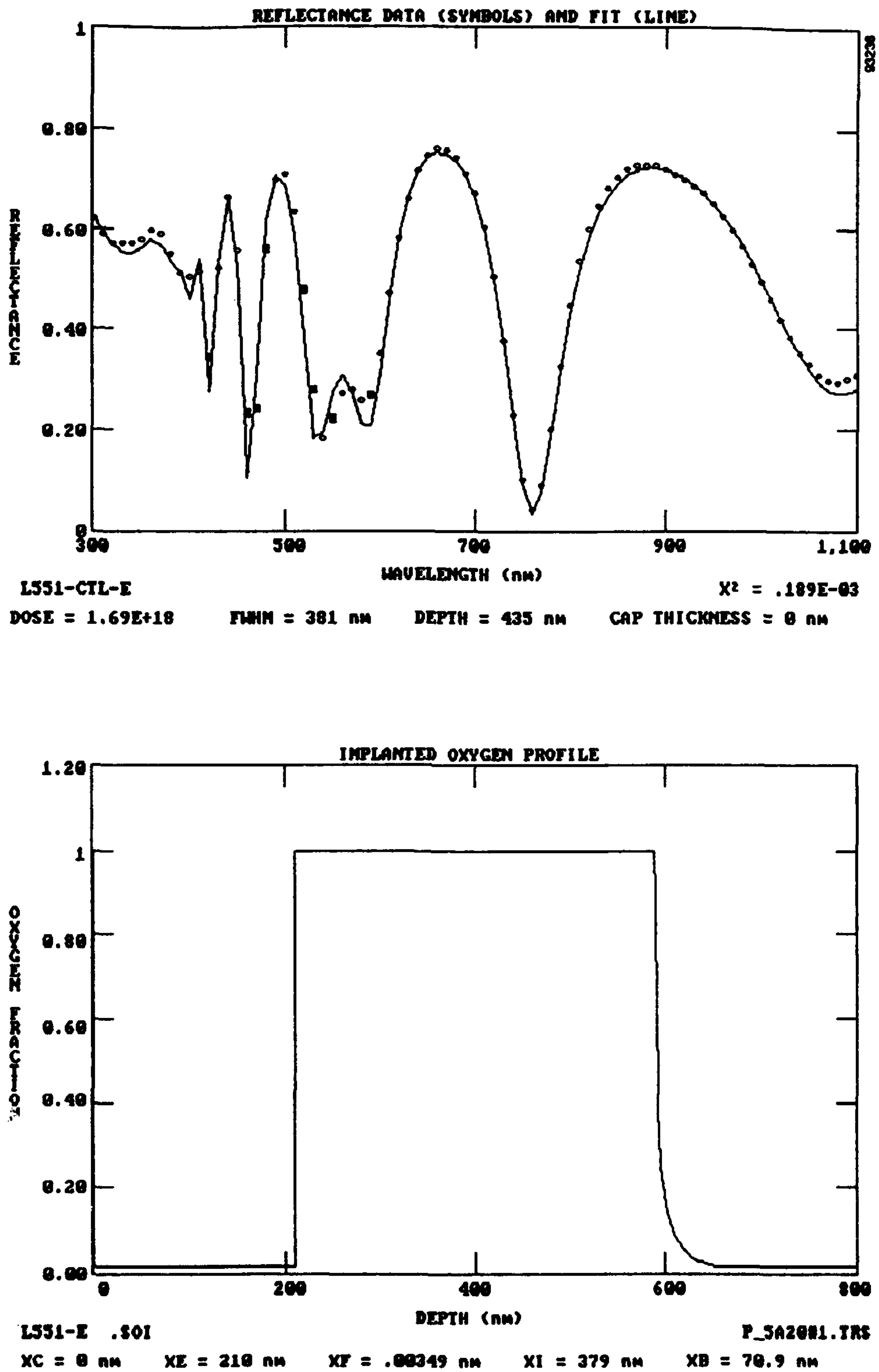
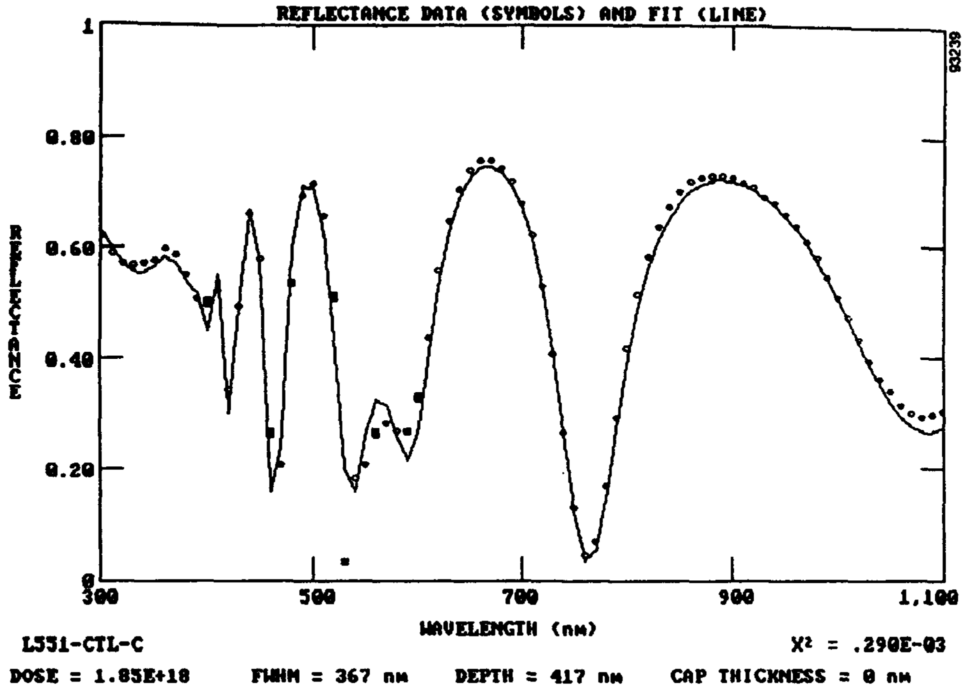


Figure 5-1. *Optical reflectance results measured on the region near edge of a SOITEC SIMOX wafer indicating a Si top layer 2100Å thick and a buried SiO_2 layer 3790Å thick.*



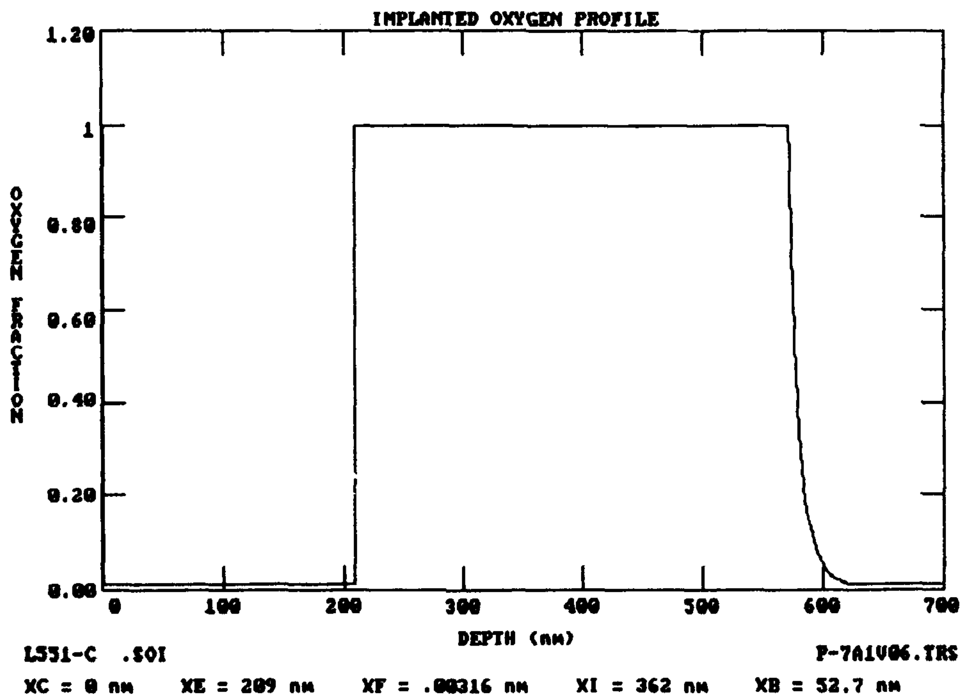


Figure 5-2. *Optical reflectance results measured at the center region of a SOITEC SIMOX wafer indicating an Si top layer 2090Å thick and a buried SiO_2 layer 3620Å thick.*

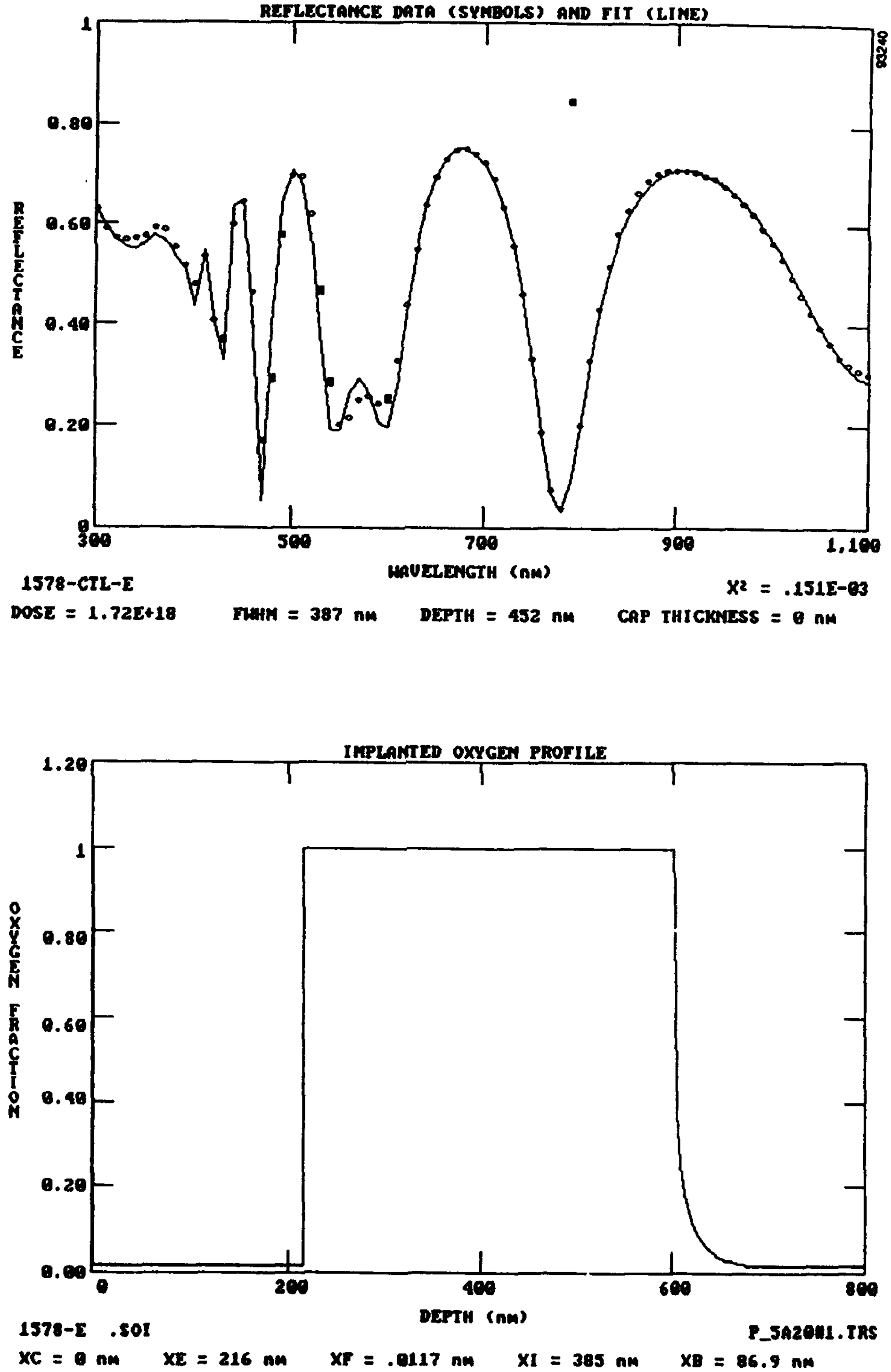


Figure 5-3. *Optical reflectance results measured on the region near edge of an IBIS SIMOX wafer indicating a Si top layer 2160Å thick and a buried SiO_2 layer 3850Å thick.*

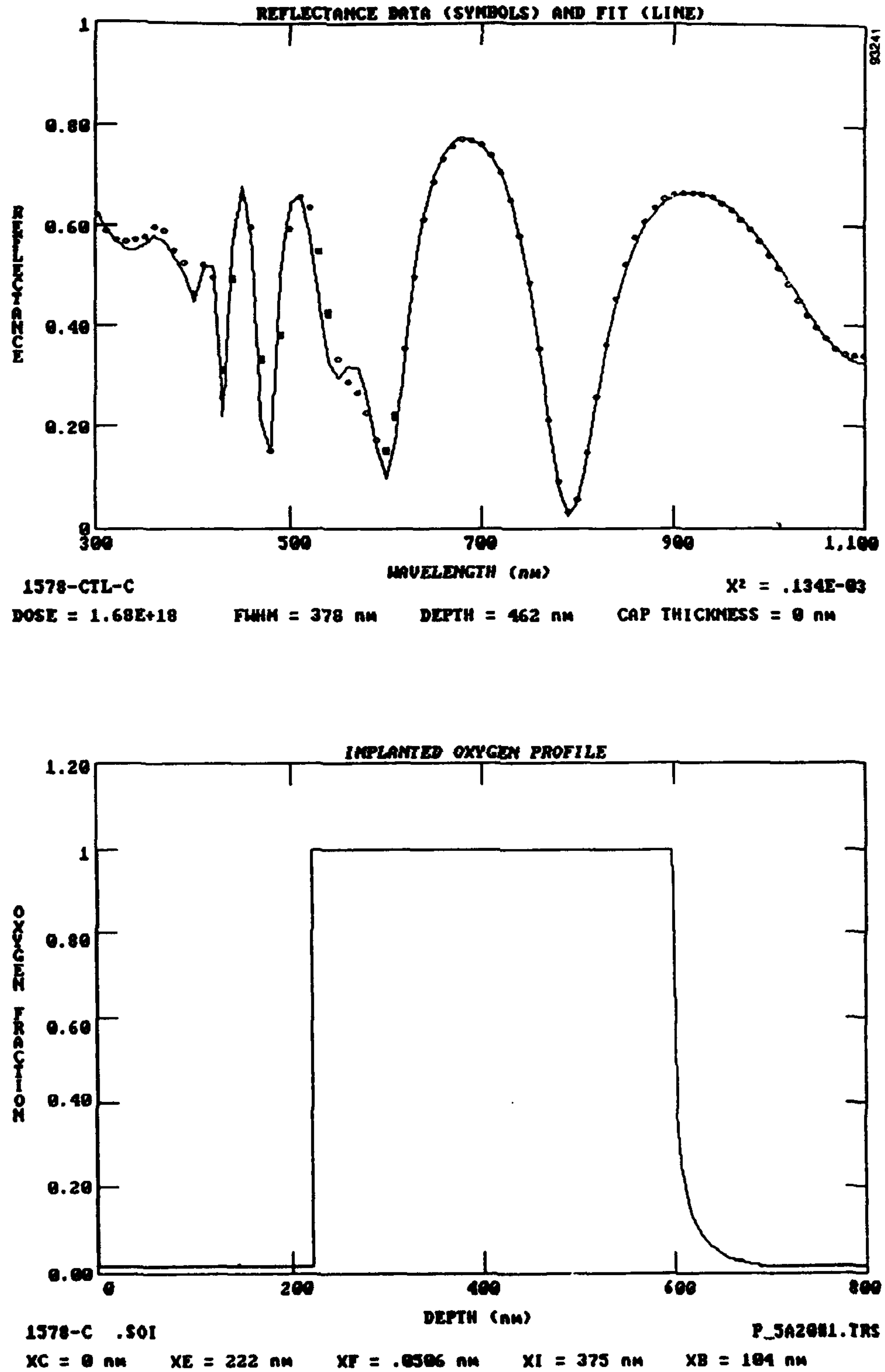


Figure 5-4. *Optical reflectance results measured at the center region of a SOITEC SIMOX wafer indicating an Si top layer 2200Å thick and a buried SiO_2 layer 3750Å thick.*

SECTION 6

DEVICE CHARACTERIZATIONS AND RESULTS

The material provided in this section was provided to Spire by the subcontractor (Department of Electrical Engineering and Computer Science at Massachusetts Institute of Technology, Cambridge, Massachusetts) under the supervision of Professor James Chung.

As indicated previously, SOI n-MOSFETs suffer from parasitic bipolar effects such as low break-down voltage,[18] amplification of GIDL (gate-induced-drain-leakage),[19] and back-channel off-state leakage which are caused by trapped positive charges in the buried oxide. These charges may originate from factors such device processing, hot-carrier degradation, and/or exposure to radiation-intensive environments.[18] Previous work has demonstrated the use of the DSFET (dual source SOI MOSFET) structure to eliminate the effects of the parasitic BJT.[20]

In this program, we have demonstrated a simple and well-controlled technique of channel defect engineering based on implanting Ge into SOI device channels to degrade the minority carrier lifetime killer and thus reduce the parasitic bipolar effect and improve the source-to-drain breakdown voltage. Furthermore, we have shown that Ge implantation creates Si structural defects in the back interface region which reduces the back channel off-state leakage and improves the radiation hardness of the device.

The success of the Ge-implantation technique requires that defect states be introduced at the back Si-SiO_2 interface without degrading the front channel Si quality. Figure 6-1 shows an XTEM micrograph of a SIMOX wafer implanted with a dose of 5×10^{15} Ge^+/cm^2 at 120 keV and annealed for 30 minutes at 850°C to form end-of-range damage dislocation loops near the buried SiO_2 interface while retaining a high quality Si layer near the surface for device fabrication.[21] The superimposed RBS profile of the implanted Ge in the Figure indicates the Ge dopant distribution from the front to back interface.

The following subsections summarize the work performed and results obtained by the MIT group for the Phase II devices before and after exposure to ionizing radiation. The radiation experiments were performed at the Rome Air Development Center, Hanscom Air Force Base, Massachusetts, with the permission and under the supervision of Dr. Walter Shedd.

6.1 PRE-IRRADIATION EXPERIMENTS AND RESULTS.

6.1.1 Improvement of Breakdown Voltage by Ge Implantation.

Our results indicate that due to the recombination centers introduced by the Ge dopants and defect states, all parasitic bipolar effects in SOI MOSFETs are reduced in the Ge-implanted devices. Figure 6-2 shows the suppression of bipolar gain in H-gate devices with the Ge-implant. The body is boron doped at 1.5×10^{15} cm^{-3} and the body tie serves as the base contact. Both front and back gates are biased at -2 V to insure that both interfaces are in accumulation mode and the field-effect component in I_c is eliminated.[22]

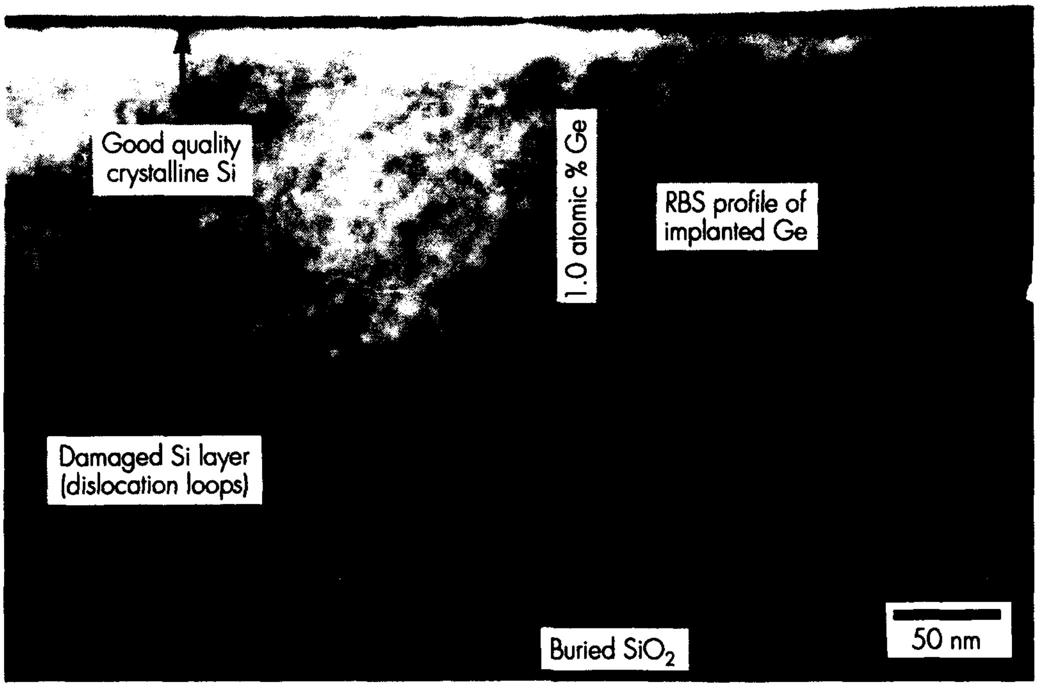


Figure 6-1. *XTEM micrograph and RBS profile of Ge in SIMOX wafer implanted with a dose of 5 x 10^{15} Ge^{+}/cm^{2} at 120 keV and annealed for 30 minutes at 850°C.*

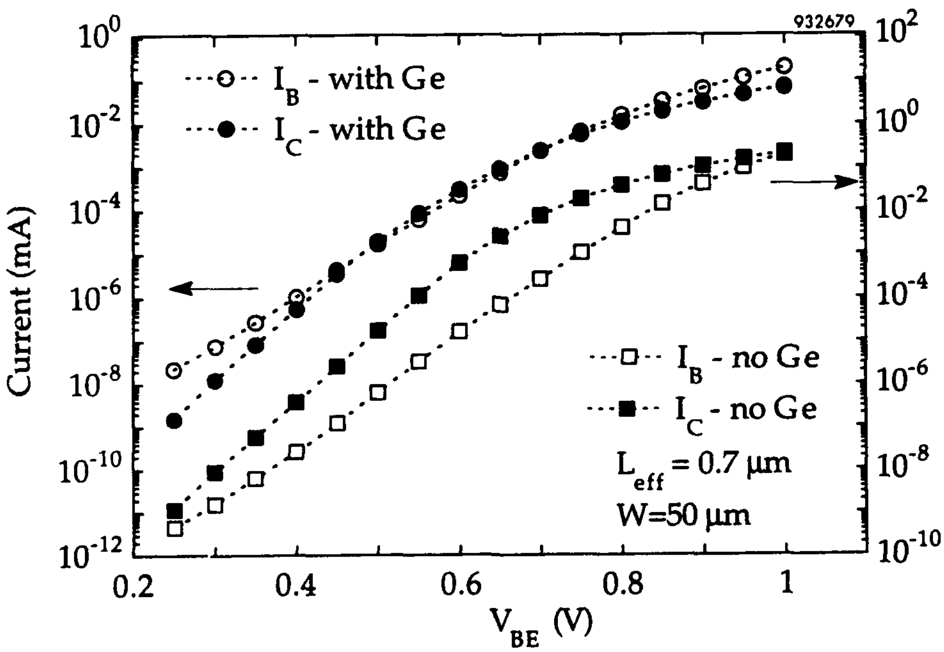


Figure 6-2. *Gummel plots for lateral SIMOX NPN BJTs (H-gate structures) with and without Ge-implant, $V_{GS,f} = V_{GS,b}$ = -2 volts. The Ge was implanted with a dose of $5x10^{15}$ Ge^{+}/cm^{2} implantation at 120 keV and the samples were annealed at 950°C for 30 minutes.*

As shown in Figure 6-3, the breakdown voltage is improved in the Ge implanted SIMOX devices compared with the ones without the Ge-implant. The source to drain breakdown voltage for SOI devices is defined at 2 mS output conductance and $V_{GS,f} = V_{T,f}$ while back gate is grounded. For bulk devices, the breakdown voltage definition remains the same except $V_{GS,f} = V_{T,f} + 2V$.

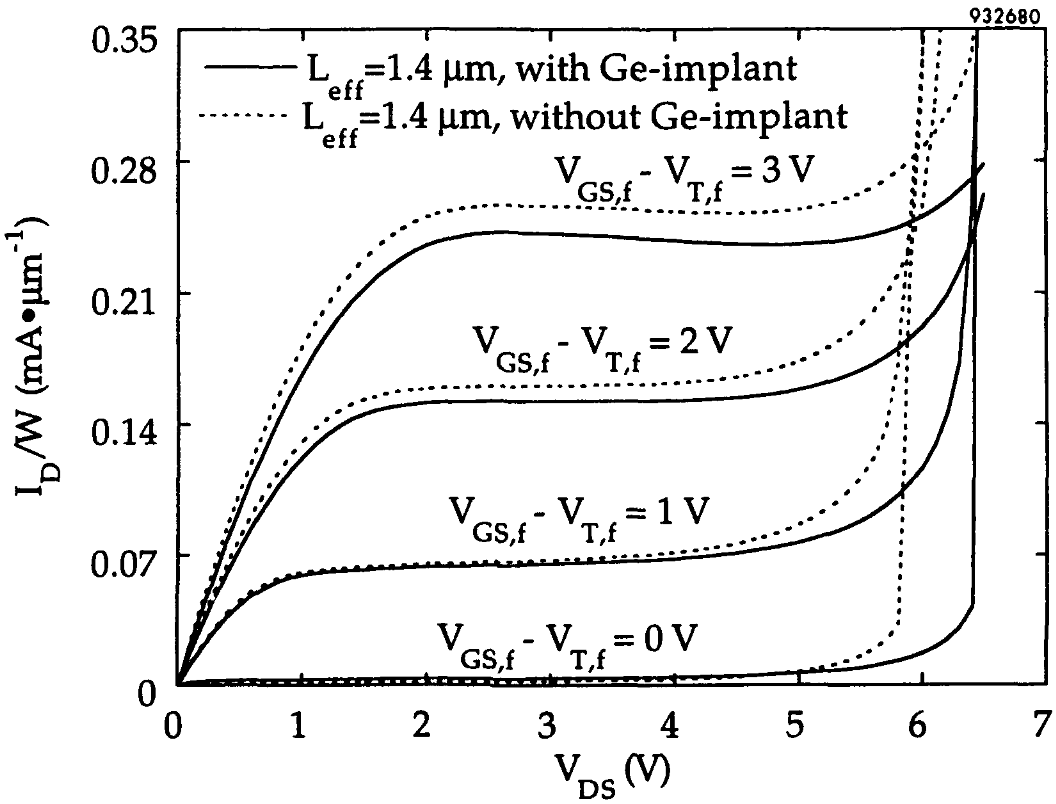


Figure 6-3. *Breakdown voltage improvement in SIMOX SOI n-MOSFETs due to Ge implantation ($5x10^{15}$ Ge^{+}/cm^{2} at 150 keV, annealed at 950°C), $V_{GS,b}$ = 0 volts.*

The channel-length-dependent improvement in breakdown voltages of both SOI devices and bulk controls is shown in Figures 6-4 and 6-5, respectively. Given the same reduction in the electron diffusion length, the amount of breakdown voltage improvement increases with increasing L_{eff}, as expected from open-base bipolar breakdown theory. For L_{eff} less than 0.5 µm, punch-through rather than bipolar breakdown dominates in bulk devices, as seen in Figure 6-5. The improvement in breakdown voltage with different Ge-implant technologies is shown in Figure 6-6, which indicates an optimal Ge-implant condition of 5 x 10^{15} cm^{-2} at 120 keV, annealed at 950°C.

Our studies show that GIDL is also suppressed in SOI devices with the Ge-implant, as shown in Figure 6-7. This improvement results because the gate-to-drain overlap area is smaller due to retarded arsenic diffusion in the Ge-implanted Si. The parasitic bipolar effect in GIDL is reduced because of the lower bipolar gain of Ge-implanted samples.

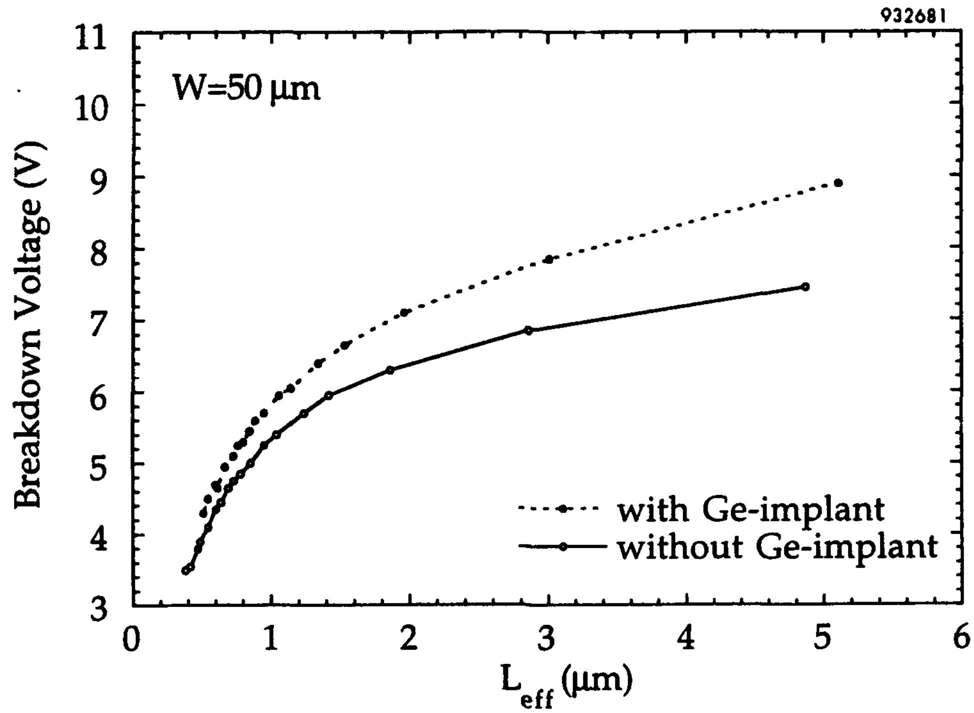


Figure 6-4. *Channel length-dependent breakdown voltage improvement in SIMOX SOI n-MOSFETs due to Ge implantation with a dose of 5 x 10^{15} Ge^{+}/cm^{2} at 120 keV and annealing at 950°C.*

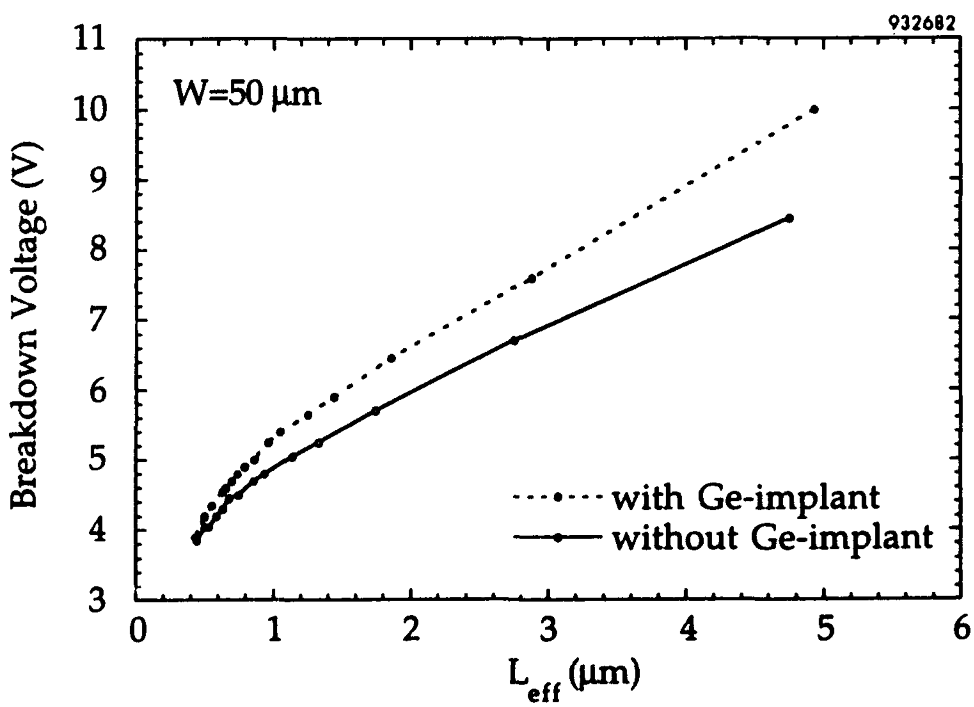


Figure 6-5. *Channel length-dependent breakdown voltage improvement in bulk n-MOSFETs due to Ge implantation with a dose of 5 x 10^{15} Ge^{+}/cm^{2} at 150 keV and annealing at 950°C.*

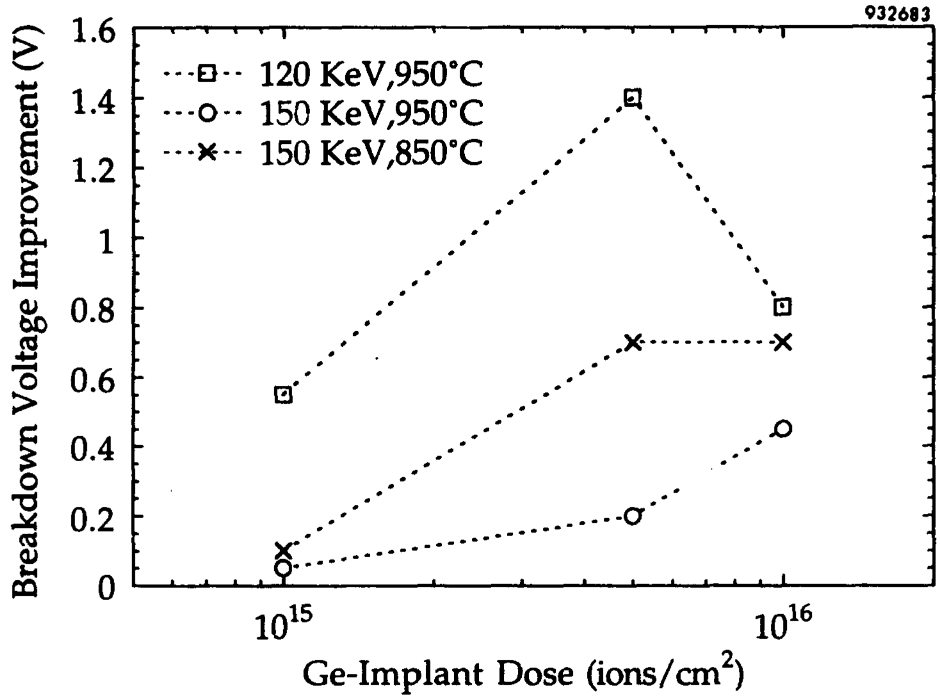


Figure 6-6. *Breakdown voltage improvement in SIMOX n-MOSFETs implanted with Ge and annealed under different conditions.*

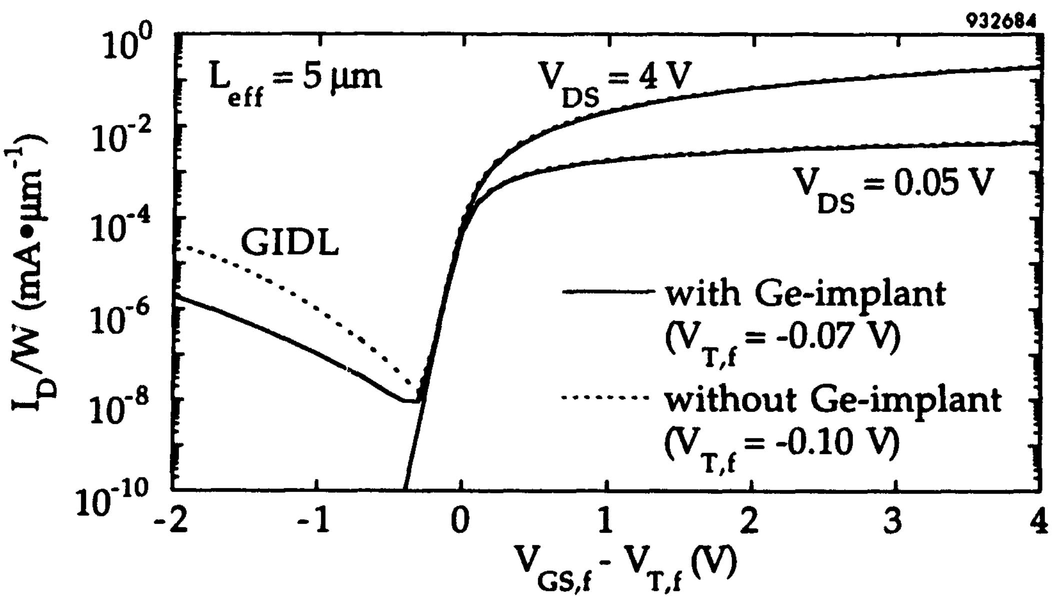


Figure 6-7. *Comparison of front channel performance in samples with and without Ge implantation (5 x 10^{15} Ge^{+}/cm^2 at 120 keV, ann. at 950°C, with $V_{GS,b}$ = 0 V).*

6.1.2 Off-State Leakage Improvement by Ge Implantation.

The defect states introduced at the back Si=SiO_2 interface region by Si structural defects and possible migrated Ge dopants can pin the Fermi level in the back interface region, as illustrated in Figure 6-8. For partially-depleted devices, positive back gate bias or trapped holes in the buried oxide can be initially supported by space charge formed by the ionized defect states. Further increase in the back bias or the amount of trapped holes will eventually cause band bending and back-channel inversion. As a result, the back-channel threshold-voltage (when the front-channel is biased in accumulation) is increased. For both partially- and fully-depleted devices with the Ge-implant, suppressed bipolar effects from impact ionization and reduced back channel mobility from Si-structural defects and Ge-related scattering also contribu'e to the overall reduction of back-channel leakage current. Indeed, the off-state leakage current is substantially suppressed, as shown in Figure 6-9. For fully-depleted devices, however, back-channel V_T remains unchanged because the body effect does not change with doping, including the Ge-implantation.[2]

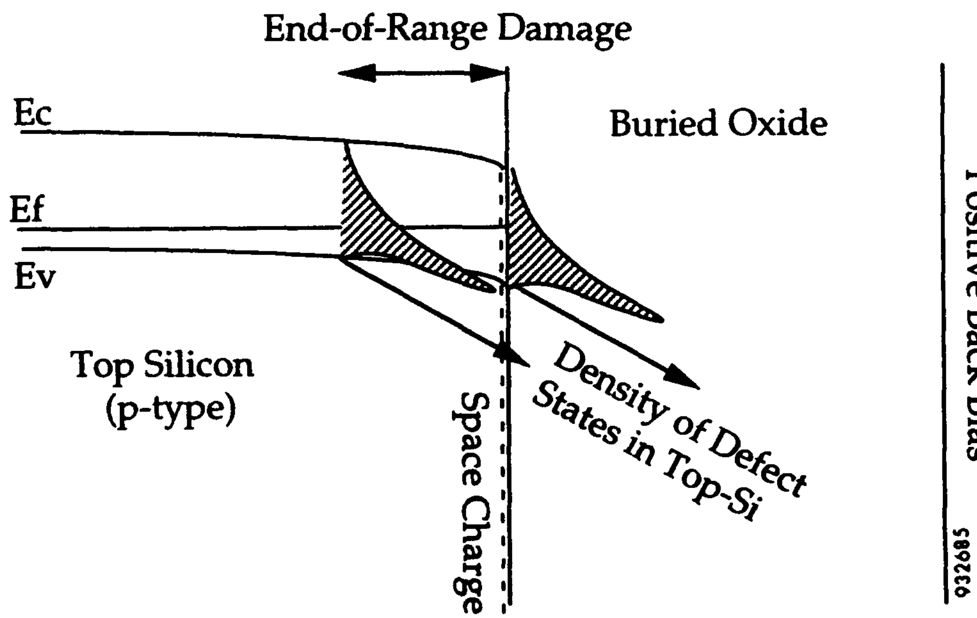


Figure 6-8. *Energy band diagram illustrating the back interface Fermi level pining in SIMOX SOI structures.*

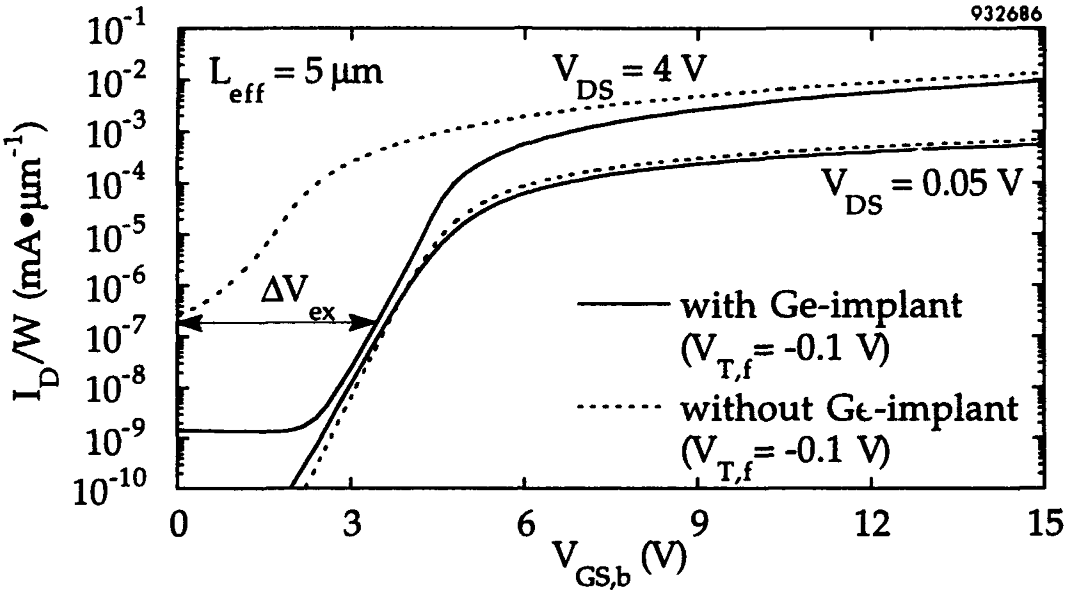


Figure 6-9. *Back channel leakage reduction in SIMOX devices due to Ge implantation ($5x10^{15}$ Ge^+/cm^2 at 120 keV, annealed at 950°C, $V_{GS,f}$).*

Also indicated in Figure 6-9, compared with non-implanted SOI devices, devices with Ge-implantation can sustain an extra back bias ($V_{ex}\Delta$) beyond the zero back bias condition. This extra back bias can be viewed to represent the total extra positive charge sustainable by the device due to trapped holes in the buried oxide. Shown in Figure 6-10, is ΔV_{ex} for different Ge-implant technologies. To achieve the largest ΔV_{ex}, an optimal Ge-implant condition of 5 x 10^{15} Ge^+/cm^2 dose at 120 keV annealed at 950°C is necessary. Notice this optimal Ge-implant condition is the same as that required for the greatest breakdown voltage improvement shown in Figure 6-6. The similar bell-shaped trend in both Figure 6-10 and Figure 6-6 indicates the important role played by the Si defect states created during the Ge-implant. A lower implant energy results in a larger volume of Si defects between the Ge-implant end-of-range and the buried oxide because the threading dislocations are terminated at the strain-induced interfaces (SiGe/Si and Si/SiO_2). A smaller thermal cycle, using lower recrystallization temperatures will retain more Si defect structures. All these effects are observable in Figures 6-6 and 6-10.

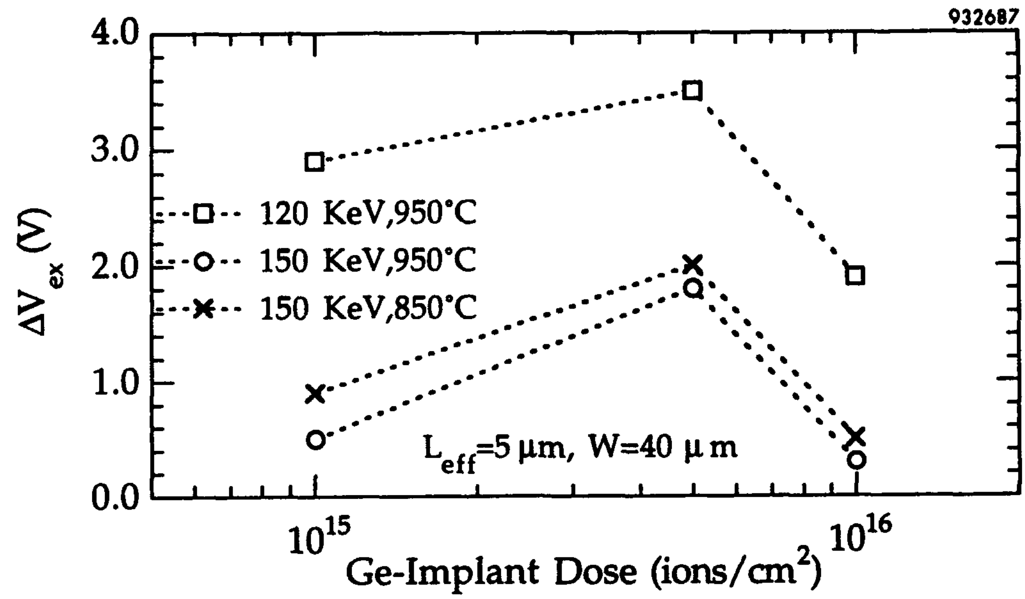


Figure 6-10. *Extra back bias levels resulting from Ge⁺ implantation with different dose, energy, and annealing temperature (V_{GSf} = -0.8V).*

6.1.3 Further Evaluation of the Ge-Implant Technology.

It is important that the Ge-implant-induced damage in the channel does not change the body effect of the front threshold voltage. As seen in Figure 6-11, the front threshold voltage with back bias remains unchanged by the Ge-implant for fully-depleted SOI devices. The front channel subthreshold slope also remains the same in SOI devices with the Ge-implant compared with the non-implanted ones, as shown in Figure 6-7.

Finally, it is also important that the optimal Ge-implant technology does not significantly degrade the front-channel current-drive. Shown in Figure 6-12 are the extreme cases of SOI front-channel μ_{eff} (effective mobility) degradation due to the Ge-implant, compared with μ_{eff} in a corresponding bulk n-MOSFET without the Ge-implant. The mobility was measured using a procedure in which the channel normal field E_{eff} is compensated with a non-zero field at the back interface for SOI devices.[23] Front-channel low- and high-field mobility degradation are shown in Figures 6-13 and 6-14, respectively, for different Ge-implant technologies. Low-field mobility is observed to be more sensitive to the particular Ge-implant conditions indicating that impurity (Ge) scattering is the major cause for μ_{eff} degradation. Indeed, this point is consistent with the overall μ_{eff} degradation trend observed in Figures 6-13 and 6-14. Higher Ge doses, lower implant energies (with resulting shorter projection ranges), and higher annealing temperatures (which broaden the Ge profile) result in more Ge dopants near the front-channel thus produce more μ_{eff} degradation in the front channel.

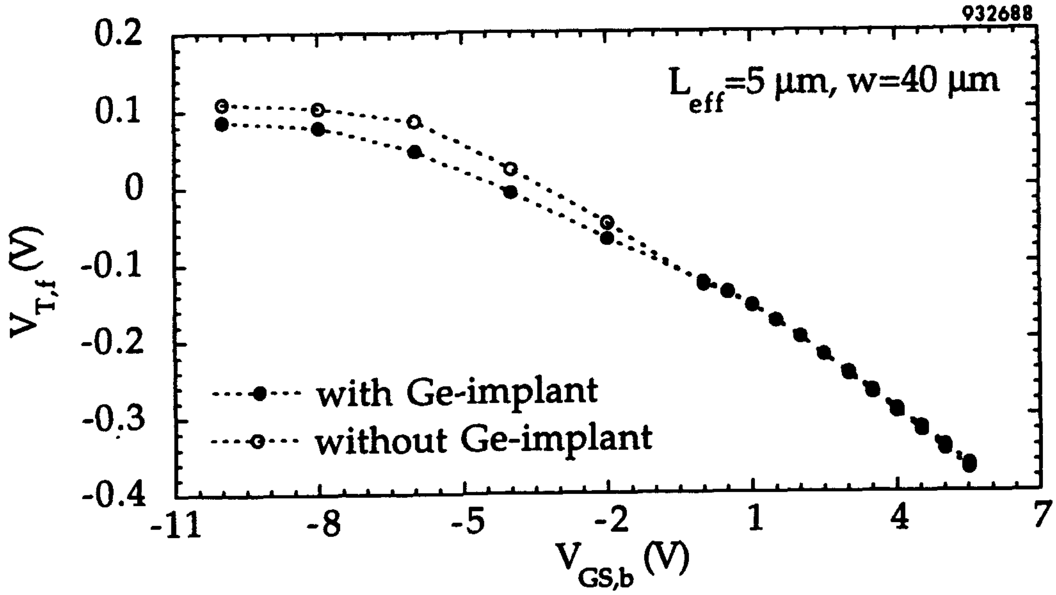


Figure 6-11. *Impact of Ge-implantation (5x10[15] Ge+/cm² at 150 keV and annealed at 950°C on front channel threshold voltage ($V_{T,f}$) body effect in SIMOX devices.*

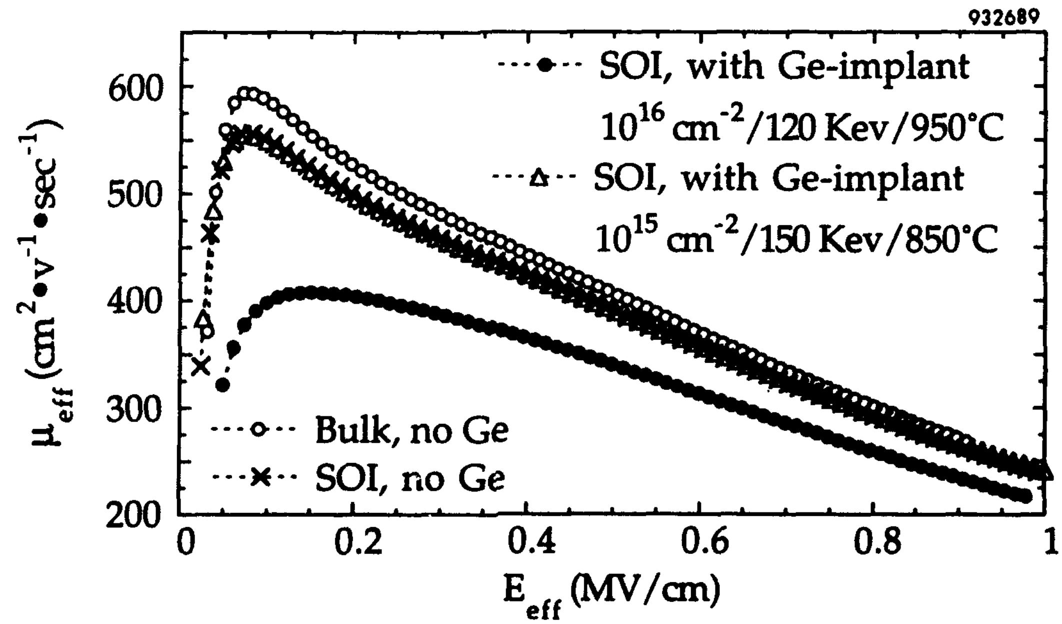


Figure 6-12. *Extreme degradation cases of front-channel μ_{eff} versus channel effective normal field due to Ge-implant.*

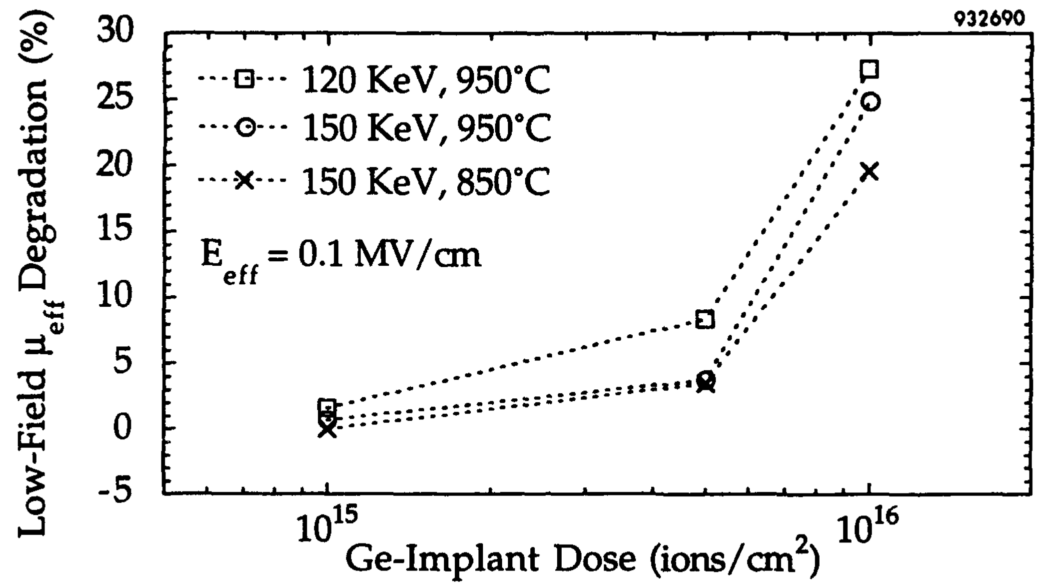


Figure 6-13. *Front-channel low-field mobility degradation resulting from Ge implantation into SIMOX and annealing at different conditions.*

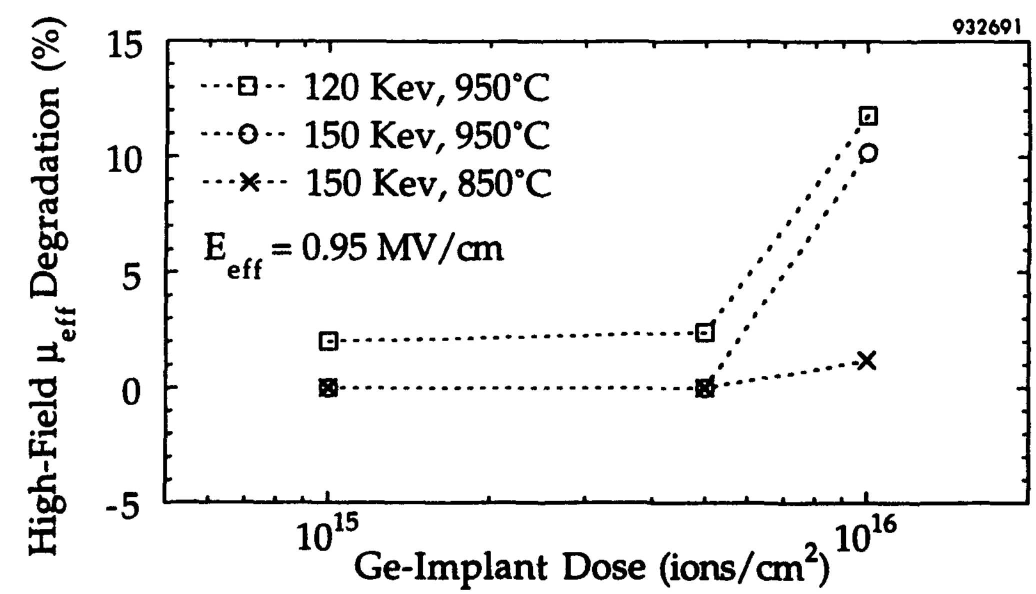


Figure 6-14. *Front-channel high-field mobility degradation resulting from Ge implantation into SIMOX and annealing at different conditions.*

6.2 POST-IRRADIATION EXPERIMENTS AND RESULTS.

6.2.1 Results from Testing Fully-Depleted Edge-Less Devices.

As discussed in Sections 6.1.2 and 6.1.3, the body effect remains unchanged for fully-depleted devices. Therefore after radiation, the shift of back-channel threshold voltage is the same for Ge-implanted SOI devices and non-implanted ones. However, the reduced bipolar effect and back-channel mobility degradation effect in off-state leakage can still be observed after irradiation. Figures 6-15a and 6-15b show the pre-irradiation back-channel subthreshold characteristics for Ge-implanted and non-implanted fully-depleted SIMOX devices. Both devices have a back-channel V_T value of about 3V (germanium implantation has little influence on the body effect). Figures 6-16a and 6-16b show the post-irradiation (100 Krad) changes of back threshold voltage and off-state leakage. As seen, the amount of back-channel V_T shift is the same for both Ge-implanted and non-implanted devices because the same amount of holes are trapped in buried oxide and device regions. But, the off-state leakage at V_{DS} = 4V is almost three orders of magnitude less at $V_{sub} = V_{T,b}$, for Ge-implanted devices. Notice the large shift in $V_{T,b}$ resulting from the 4V bias on back gate during irradiation which pushes the trapped holes to the back interface.

6.2.2 Results from Partially-Depleted Edge-Less Devices.

For partially-depleted devices, the Ge-implanted SIMOX devices always showed higher back-channel V_T due to the back-interface Fermi level pinning effect discussed in Section 6.1.2. This effect still exists after the irradiation. Pre-irradiation subthreshold characteristics for partially-depleted Ge-implanted and non-implanted SIMOX devices are shown in Figures 6-17a and Figure 6-17b. The starting $V_{T,b}$ values for Ge-implanted and non-implanted devices were 3.3V, and 2.4V , respectively. After 170 Krad X-ray irradiation, a 4V shift in $V_{T,b}$ was observed in both devices, thus preserving the higher $V_{T,b}$ value for the Ge-implanted device. Off-state leakage reduction effect is also retained after the irradiation for Ge-implanted devices, as shown in Figure 6-18. The back gate bias was 0V during radiation, so trapped holes in the buried oxide were not concentrated at the back interface region, resulting in a much smaller shift in $V_{T,b}$ compared with the shift described in Section 6.2.1.

6.3 SUMMARY OF RESULTS.

In conclusion, we have demonstrated channel defect engineering in SIMOX SOI and bulk Si devices using Ge-implantation in order to suppress parasitic bipolar effects and to reduce off-state leakage, and have discussed the physical mechanisms involved in this simple and well-controlled technique.

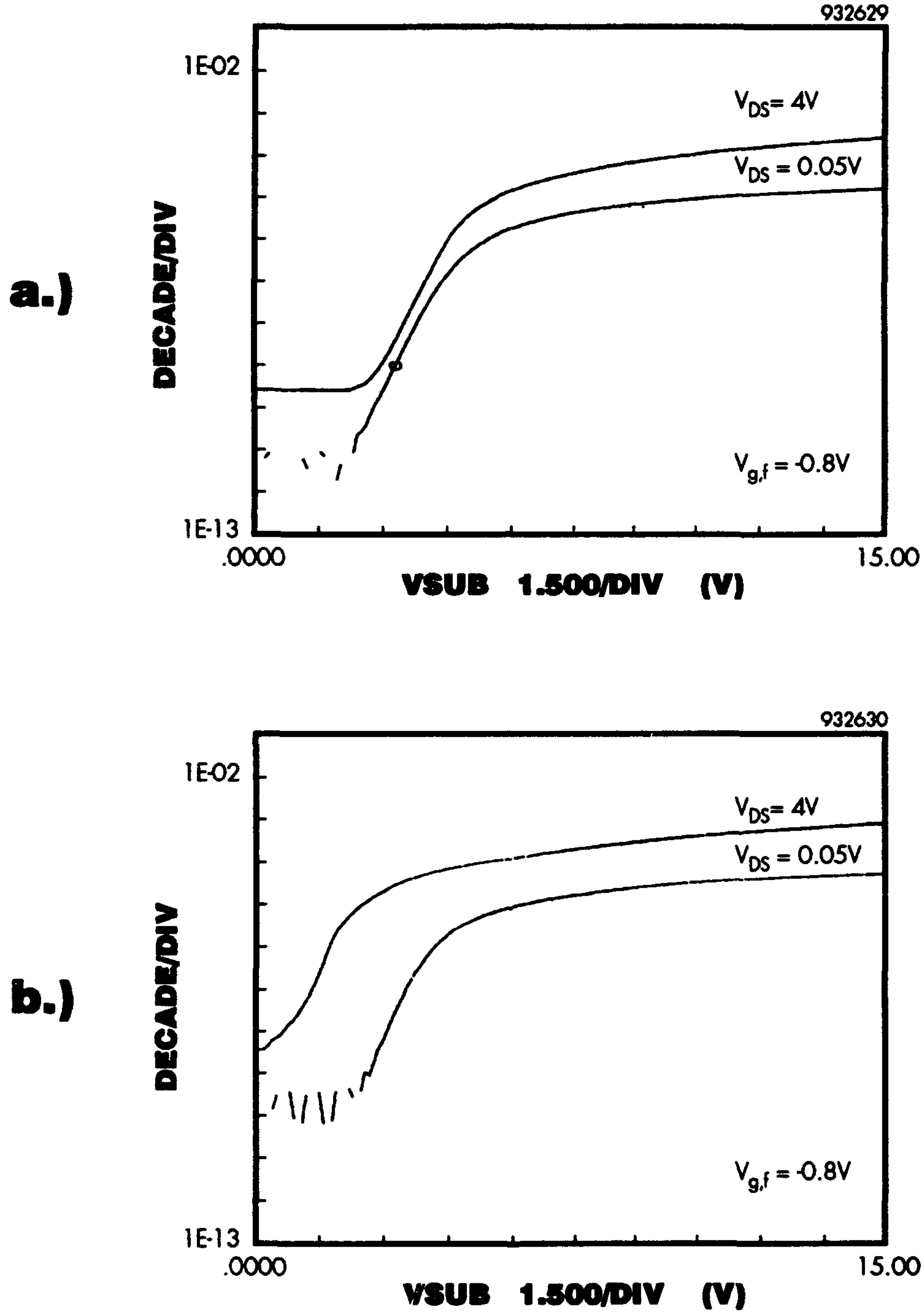


Figure 6-15. *Comparison of pre-irradiation subthreshold characteristics of fully-depleted SIMOX devices a) with, and b) without the Ge implantation (L_{eff}=5 µm and W=40µm).*

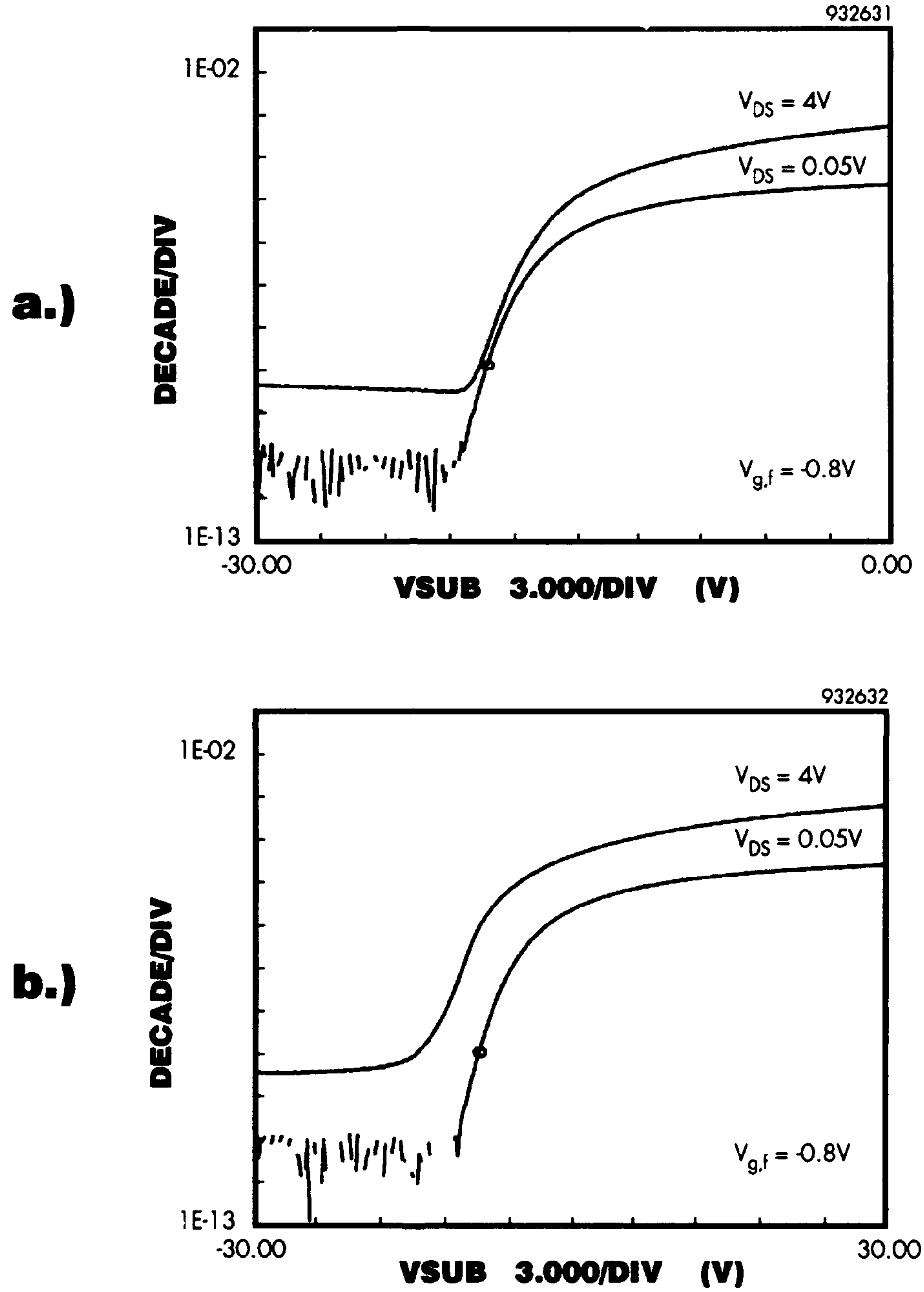
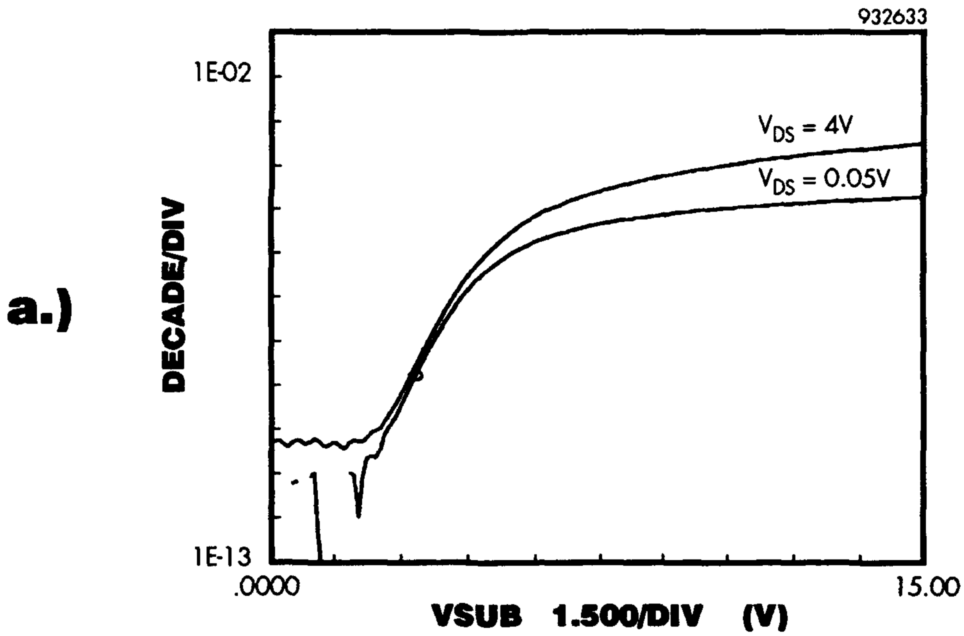


Figure 6-16. *Comparison of post-irradiation, 100 Krads (Si), back-channel V_T vs. leakage current plots for fully-depleted SIMOX devices a) with, and b) without Ge implantation ($V_{G,f}$=-0.8V, V_{sub}, or $V_{G,b}$=4V during irradiation).*



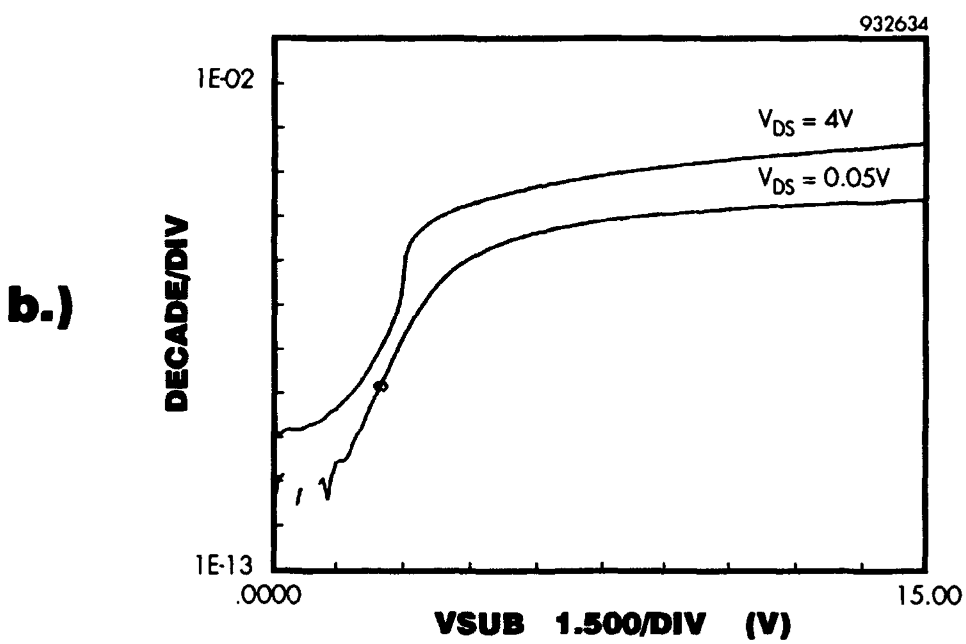
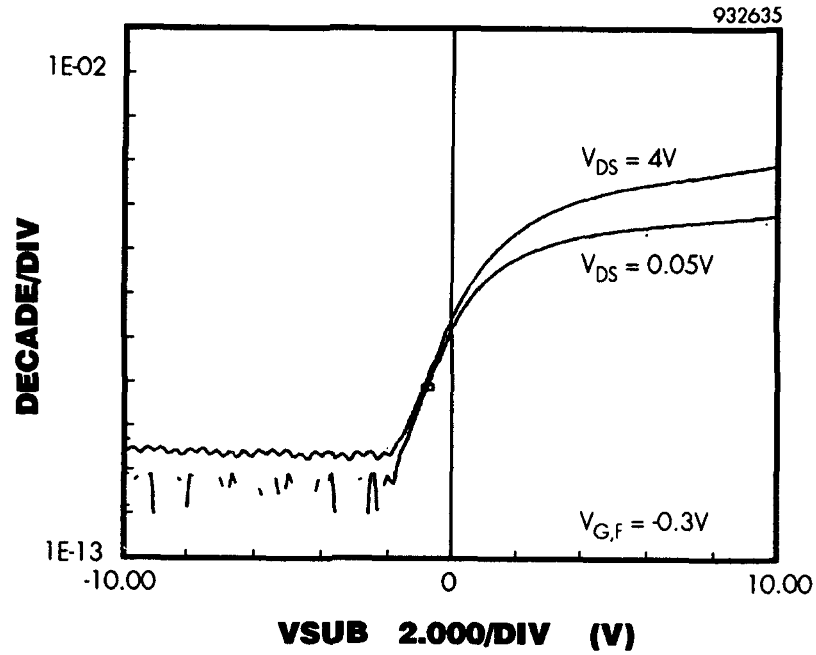


Figure 6-17. *Comparison of pre-irradiation subthreshold characteristics of partially-depleted SIMOX devices a) with, and b) without the Ge implantation (L_{eff}=5 µm, and W= 40 µm).*

a.)



b.)

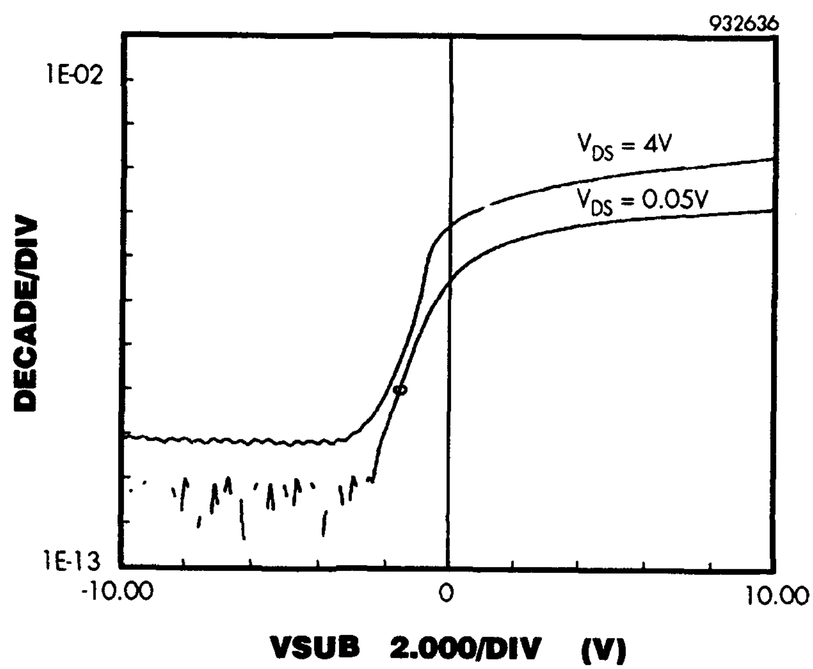


Figure 6-18. *Comparison of post-irradiation, 170 Krads (Si), back-channel V_T vs. leakage current plots for partially-depleted SIMOX devices a) with, and b) without Ge implantation ($V_{G,f}$=-0.3V, V_{sub}=0V during irradiation).*

SECTION 7

CONCLUSIONS

In this program we demonstrated the improvement of the crystalline quality of the Si top layer and the degradation of Si at the Si/buried SiO_2 interface for SIMOX wafers implanted with Ge. Improving the crystalline quality of the surface region is essential for high performance device fabrication. In addition, degradation of the Si/buried SiO_2 interface region significantly reduces back channel leakage current in devices exposed to ionizing radiation.

In order to demonstrate applications of Ge-implantation into SIMOX, we have fabricated n-MOSFET devices on SIMOX and Si, with and without Ge implantation. No degradation in device performance was observed for devices fabricated on SIMOX substrates implanted with Ge, as compared to substrates without Ge implantation. Our results clearly indicate that off-state leakage and parasitic bipolar effects were reduced in the Ge-implanted SIMOX substrates. Electrical testing was also performed before and after irradiation of devices at 100 krad X-ray at RADC. Our electrical testing after irradiation shows that off-state leakage current for devices fabricated on SIMOX with Ge implantation was about 1000 times less than that for devices fabricated on SIMOX without Ge implantation. Lastly, our results indicate that Ge implantation into SIMOX resulted in the suppression of the gate-induced drain leakage of n-MOSFETs and the the source-to-drain voltage was significa ly improved.

SECTION 8

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