RAPID AND ACCURATE TIMING SIMULATION OF RADIATION-HARDENED DIGITAL MICROELECTRONICS USING VHDL

DISSERTATION

Charles P. Brothers, Jr., Captain, USAF

AFIT/DS/ENG/94-01

DEPARTMENT OF THE AIR FORCE
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Wright-Patterson Air Force Base, Ohio

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Charles P. Brothers, Jr.

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Abstract

This dissertation presents the development of a fast, accurate, timing simulation capability based on VHSIC Hardware Description Language (VHDL) without the use of back annotation of timing delay information. This VHDL-based timing simulator is intended for use with radiation-hardened microelectronic circuits in simulating timing of circuit operation in pre-radiation, post-radiation (1 Mrad(Si) total dose), and ionizing dose radiation environments. Development of the timing models used in the VHDL timing simulator are presented. The implementation of the timing models are incorporated into a VHDL library composed of basic logic gates, latches, and flip-flops. Simulations of complex circuits were run in SPICE and VHDL to assess the timing accuracy and simulation run time of the VHDL-based timing simulator versus SPICE. Results of the simulations are presented. Final evaluation of the simulator included testing of a microprocessor control unit. In all cases, the VHDL-based simulation ran over two orders of magnitude faster than the equivalent SPICE simulation. In the pre- and post-radiation environment, accuracy estimates are usually within five percent and never exceed 12 percent. Worst-case timing estimate errors increase above 15 percent for dose rates above 1.0×10^{11} rads(Si) per second. This VHDL-based timing simulator represents an improvement over SPICE in the ability to quickly simulate complex circuits while sacrificing some accuracy.

RAPID AND ACCURATE TIMING SIMULATION OF RADIATION-HARDENED DIGITAL MICROELECTRONICS USING VHDL

I. Introduction

1.1 Introduction

This document presents a research effort to develop a method of accurately simulating the operation and timing performance of radiation-hardened microelectronic circuits in a rapid fashion using VHSIC Hardware Description Language (VHDL). Chapter I introduces important background information, and includes the purpose statement and research approach. This chapter concludes with an overview of the dissertation.

1.2 Background

Microelectronic circuits are affected by most forms of radiation including prompt gamma and x-ray or ionizing radiation, neutron radiation, and alpha radiation. Evaluated incident radiation includes dose rates and total dose absorbed. When exposed to high radiation dose rates, microelectronic circuits experience parameter changes and permanent damage. Some of the parameter changes anneal with time after the radiation source is removed causing potential circuit operation shifts for days after the initial exposure [1].

In many cases, depending on the microelectronic circuit design, the damage induced by radiation does not cause the circuit to malfunction or degrade below specification levels.

Throughout this document, all radiation values are given in terms of the rad, where one rad equals 100 ergs of radiation deposited per gram of material [1]. The most common dose level will be one million rads into silicon (1 Mrad(Si)). Total dose refers to the dose absorbed from ionizing radiation.

Parametric and performance simulations of radiation-hardened microelectronic circuits are time-consuming and difficult, especially for complex circuits. Currently, designers rely on SPICE-based simulators to predict the operation and timing performance of radiation-hardened microelectronic circuits. In an effort to improve the simulation capability of radiation-hardened microelectronic circuits, several researchers are developing fast circuit simulators [2, 3]. In every case, each simulator suffers from limitations in operating performance or capability.

Current microelectronic circuit simulations rely on specially modified versions of SPICE to estimate post-radiation parameter and performance changes. With complex integrated circuits, SPICE simulations require time intensive CPU resources. Creating fast circuit simulators that provide a relatively accurate picture of the response of an integrated circuit to radiation exposure allows simulation of microelectronic circuits with larger numbers of transistors. Being able to efficiently simulate these circuits which are constructed for applications where radiation hardness is required, such as electronics used in space or subject to nuclear weapons effects, becomes practical using fast microelectronic circuit simulators.

The major limitation of SPICE-based simulators is the computer processing time required to simulate the operation of a complex microelectronic circuit. The discreet time differential equations used by SPICE require many iterations to simulate the operation of a circuit through a single logic state transition. When a circuit is composed of many thousands of transistors, simulating the circuit can consume days. The advantage of SPICE is its accuracy in simulating circuit performance.

To improve on the simulation speed of SPICE requires a simulator to use simpler and/or fewer equation iterations for simulation of a microelectronic circuit. The task of making computer use more efficient and faster in simulation turn-around time has been accomplished by developing switch-based simulators. Switch-based simulators treat transistors as switches, where only state transitions need be calculated, speeding-up the simulation process. A refinement of the switch-based simulator concept is based on VHDL, a standardized simulation environment that simulates microelectronic circuits as either behavioral or structural constructs at the switch or logic-block level.

SPICE-based microelectronic circuit simulators, the current standard, are used by most circuit designers when designing radiation hardened circuits. Simulators other than SPICE have been developed for special applications. These include a switch-level timing simulator, PARA, tied to particular technology libraries, and one simulator developed by LSI Logic that uses VHDL libraries with pre- and post-radiation timing data [2, 3].

For this research effort VHDL, operating under Synopsys, was chosen since it provides the capability for reasonable accuracy, a quick running simulation environment, and is the DoD standard hardware description language [4]. Other options could have been chosen, including developing a new simulator, but VHDL provides an adequate

environment for executing the models developed in this research and is IEEE Standard 1076 [5]. Simulation of radiation-hardened microelectronic circuits can be greatly improved with the use of VHDL-based simulators. SPICE-based simulators are accurate, but are slow in simulating the operation of complex circuits. Improved simulation capability of radiation-hardened microelectronic circuits can be realized through VHDL circuit simulators, which currently suffer some limitations in timing accuracy and ability to simulate circuit behavior for varying radiation environments. Improved fast simulation capability and increased timing accuracy by using the VHDL simulator with the necessary models and libraries for radiation-hardened microelectronic circuits improves the ability of circuit designers to develop complex radiation-hardened microelectronic circuits in a timely manner.

A limited VHDL radiation-hardened microelectronics simulator is under development at a company, LSI Logic, containing block-level pre- and post-radiation (1 Mrad(Si) total dose) timing data for their particular radiation-hardened circuit designs [3]. Simulation of each circuit is accomplished by running the VHDL code using the pre-radiation library and checking performance of the circuit against design specifications. After the pre-radiation circuit design is acceptable, the VHDL code is rerun using the post-radiation library data to check the performance of the circuit. All timing simulations are based on the performance of gate array microelectronic circuit blocks designed by LSI Logic.

VHDL-based simulation methods are being developed for non-radiation-hardened applications to increase the timing accuracy of VHDL. Methods of increasing timing accuracy include back annotation of timing delays, multi-level logic schemes and

insertion of delay nodes between logic gates. The value of these efforts is to reduce simulation time by over two orders of magnitude while sacrificing less than 15 percent in timing accuracy.

The VHDL-based simulator can be used by microelectronic circuit designers to incorporate the effects of a radiation environment into a simulation, thus incorporating the effects of radiation on circuit performance. The use of the VHDL-based simulator complements SPICE, allowing designers to spend less time simulating circuit operation and timing performance during the development of radiation-hardened microelectronic circuits than is possible when SPICE is used exclusively for circuit simulation.

1.3 Problem Statement

The purpose of this research is to develop simple generic models that provide rapid and accurate timing estimates for simulating radiation-hardened microelectronic circuits using a VHDL-based simulator. A realistic goal is for the VHDL-based simulator to run at least two orders of magnitude faster than SPICE while maintaining timing accuracy to within 15 percent of the values obtained using SPICE. Demonstration of the models is accomplished by developing VHDL compatible libraries and then demonstrating the model operation using the VHDL-based logic simulator. Validation of the models and subsequent libraries is accomplished by running simulations and comparing the results with data obtained from results of running radiation-inclusive models in SPICE simulations. The vendor validated the radiation-inclusive SPICE models by comparing results with fabricated test articles.

1.4 Approach

Developing a method of simulating microelectronic circuit operation and providing accurate timing estimates required several steps to be completed. First, the sources of time delays were determined. These included the intrinsic logic-block delays, fanout induced delays, differences in sub-circuit output slew rate, and delay effects of a radiation-inclusive environment. Second, models that accurately estimate the timing delays were developed. Third, the models were incorporated into VHDL useable libraries providing a simulation environment. Fourth, simple microelectronic circuits were tested to validate the operation and accuracy of the models using the VHDL-based simulation. Finally, the VHDL-based simulator was tested and validated with larger circuits (over 2800 transistors) to demonstrate the timing accuracy and the faster performance against the baseline SPICE performance.

1.4.1 Determining Time Delay Source. The sources of the time delay in the operation of the microelectronics were determined. Every digital microelectronic circuit takes some amount of time, after an input stimulus changes, to switch from one output state to another. This switching delay time is predicated on several factors including but not limited to: intrinsic logic-block delays, fanout-load induced delays, circuit slew-rate, radiation-environment, temperature, and supply-voltage.

This research held many of the potential variables, including temperature and supply-voltage, constant. Variables evaluated are the intrinsic logic-block delays, fanout-load induced delays, circuit slew-rate, and radiation environment. Time delay information was collected for each primitive logic gate by running SPICE simulations with various

output loads connected to the logic gate under test. Every primitive logic circuit was simulated to determine the internal intrinsic time delay of the circuit. The change in time delays were then measured for fanout-loads of 27 to 270 femtofarads, representing fan-out loading of one to ten gates. Circuit slew-rate time delay effects were also incorporated into the fanout time delay measurements. All simulations were conducted for the pre-radiation environment, 1 Mrad(Si) total dose environment, and various levels of radiation dose rates. The resulting changes in the microelectronic circuit timing delay were recorded for each simulation run.

1.4.2 Model Development. The second step consisted of developing the models. After the timing delays for each logic gate were determined, models were developed that accurately represented the associated timing delays. Measurements from the SPICE simulations, for each primitive logic gate, were used to provide delay time information in developing the models. The basic timing model used consists of two element types, a resistor and capacitor. The drive capability of a logic gate is represented as a drive resistance. The fanout-induced and the gate intrinsic time delay components are represented by capacitance values. Additionally, gate leakage, when applicable, is represented as a load resistance. The logic gate state transition time delay is calculated by summing the capacitances and load resistances separately and then using the product of the drive resistance against the load capacitance and resistance to calculate the delay time information.

Accounting for radiation environment induced time delay changes was accomplished by adjusting the values of the drive resistance and load capacitances.

Provisions for adjusting the gate input load capacitance and resistance also exist. If the MOS transistor input gate leakage had been significant for the technology implemented (Texas Instruments, SIMOX) it would have been observed during the SPICE simulation runs. Subsequently, the model calculations would have reflected these changes. The model structure developed for this research allows for gate leakage resistance and load capacitance values to be adjusted in response to a radiation environment should a fabrication technology require it.

The values for the load capacitance, drive resistance, and intrinsic time delay capacitance of the model variables were determined empirically, using SPICE measurements, for each logic-block switching condition. The load capacitance for the gate inputs was extrapolated from measurements obtained from SPICE. Time delay information was then collected, using SPICE, for both output high-to-low and low-to-high transitions with load fanout values set from one gate to ten gates. Using this data, the drive resistance values were then calculated. Finally, the intrinsic delay time of each gate was measured and the intrinsic delay time load capacitance values were calculated.

1.4.3 VHDL Code Development. VHDL code was developed which executes the models (complete with variables) that run under a VHDL environment for accurate simulation of desired microelectronic circuits. The code is designed to run efficiently in VHDL; independent sections of each logic gate were divided into processes (subroutines). The individual processes within each logic gate are then only invoked as necessary, keeping overall program run time to a minimum.

VHDL code was developed to run the radiation-inclusive environment time delay models. The necessary functions needed to implement the model were parsed into blocks. The blocks included the Boolean logic function, the radiation effects procedure, and the time delay calculation. The Boolean logic function simply implemented the functional operation of the logic gate. The radiation effects procedure is used to adjust values of the drive resistance and the intrinsic time delay load capacitance, as necessary to account for the effects of the simulated radiation environment. The time delay calculation procedure inputs all the adjusted drive and load parameters and calculates the transition time delay of the logic gate.

One important feature of the VHDL code is the requirement to feed back the load values from the load gates to the driving logic gate. The feedback is accomplished through the VHDL logic gate ports. When the driving logic gate output is connected to more than one other load gate input, a special construct, called the WIRE, is required to combine the input load parameters of these gates and feed the sum of the load values back to the driving gate.

The WIRE provides two functions. First, the WIRE inputs the load capacitance and resistance from the driven stage logic gates and sends the sum of the values to the driving logic gate. Second, logic transition information is sent from the driving logic cell to the driven gates after the calculated time delay.

1.4.4 Initial Model Validation. The operation and accuracy of the VHDL implemented models needed to be determined. Initially, the VHDL code was used in the simulation of small microelectronic circuits to validate the function and timing accuracy

of the models when compared to SPICE simulations of the same circuit. By evaluating operation of the VHDL code on small, simple, microelectronic circuits, the focus remained on insuring the correct operation of the timing models within the VHDL code.

Initial model function and transition delay time calculations were accomplished on each of the individual logic gates. Since the VHDL model parameter values were obtained directiy using SPICE, the VHDL results agreed to within one percent for all measurements made. After the individual gates were tested, a four-bit ripple-carry full adder was designed and tested in VHDL and compared with the results obtained from SPICE.

1.4.5 Model and Simulator Testing. After initial tests were completed, the operation of the VHDL code was validated. To demonstrate the models would work for a large cross section of microelectronic circuit designs, it was necessary to expand the library set to the final size of 15 gates. The complete set of models was incorporated into the final library. The library of gates was then validated with three different circuits, including a relatively complex circuit consisting of the control unit for a 16-bit microprocessor. Results were compiled for all the radiation-inclusive model VHDL tests and compared with the results obtained using SPICE. Additionally, the circuits were simulated in standard library VHDL to show the accuracy increase, and slower run time obtained by using the radiation-inclusive VHDL model.

1.5 Overview

This document is organized into a total of seven chapters. This chapter provided an introduction to the research. Chapter II summarizes the effects of radiation on microelectronic circuits. Radiation effects are divided into three sections: ionizing total-dose radiation, neutron irradiation, and dose rate effects. Ionizing radiation includes but is not limited to: gamma, x-ray, and secondary emissions from alpha and beta radiation.

Chapter III presents a summary of current microelectronic circuit simulators. These simulators include; SPICE-based, switch-level, and hybrid simulators. SPICE-based simulators are both conventional SPICE using radiation-inclusive models and dedicated radiation-inclusive SPICE. Switch-level simulators treat transistors or logic-blocks as discrete event switches. The hybrid simulators contain a mix of other types of simulators, with one part of the simulator using one type of technique and another part using a different simulation technique.

Chapter IV documents the development of the simulation models and the VHDL library. Development of the simulation models using simple mathematical models to calculate the timing performance of digital microelectronic circuits is presented. The logic for choosing VHDL to run the timing simulation of the models in simulating the operation of the microelectronics and the development of the VHDL library are presented.

Chapter V details the test plan or method of testing and validating the simulation models and VHDL library. This chapter contains the procedures, methods of data collection, circuits tested, and the benchmarks, for both SPICE and a standard implementation of VHDL.

Chapter VI presents the results of the testing methodology in Chapter V. Timing accuracy and run time performance are presented for the microelectronic circuits tested. Error sources uncovered during testing are also documented. This chapter discusses the useability, strengths, and weaknesses of the simulator models and implementation.

Chapter VII contains the conclusions and recommendations for further research. This chapter reviews the useability of the simulator models and implementation. Finally, recommendations are made that outline possible directions for further research using the findings of this research.

II. Effects of Radiation on Microelectronics

2.1 Introduction

Radiation has several effects on microelectronic circuits which can be split into several categories, to include: ionizing radiation, neutron radiation, and the dose rate of radiation. Each category of radiation has a different effect on electronic circuits and is presented separately. Ionizing radiation primarily effects the insulating oxide in metal-oxide-semiconductor field effect transistors (MOSFETs) and neutron radiation effects mostly the channel region of MOSFETs. Finally, radiation dose rates affect MOS circuits through several mechanisms including: photocurrent generation, trapped-hole generation, trapped-hole annealing, and increased channel conductivity, all of which are time dependent. In MOSFET microelectronic circuits, the principal problem is the effect of ionizing radiation in the gate silicon dioxide (SiO_2) insulator.

2.2 Ionizing Radiation

2.2.1 Physical Effects of Ionizing Radiation on MOSFETs. Ionizing radiation includes but is not limited to, gamma, x-ray, and secondary emissions from alpha and beta radiation. The time dependent effects of a prompt ionizing radiation event impinging on a MOSFET is shown in Figure 1, with the pre-radiation condition of the gate oxide being shown in Figure 1(a). The principal ionizing radiation damage mechanism in MOSFETs is due to the creation of electron-hole pairs in the gate SiO_2 insulator during exposure to radiation, as shown in Figure 1(b). When the initial irradiation occurs, electron-hole pairs

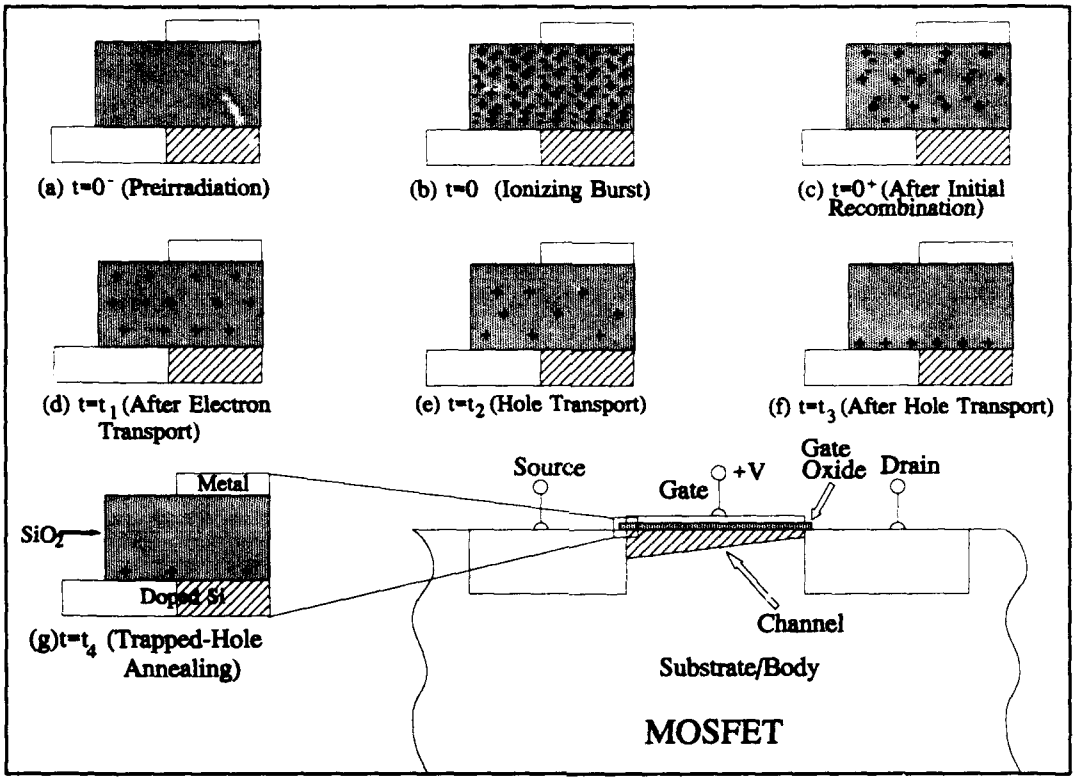

Figure 1. MOSFET Displaying Radiation Induced Hole Trapping.

are generated so they are evenly distributed through the SiO_2. Many of the electron-hole pairs recombine within a few ten thousandths of a second, as shown in Figure 1(c). After the initial recombination, the remaining free electrons are swept out of the insulator material, in a few thousandths of a second, by the electric field in the gate insulator, leaving only trapped-holes, as shown in Figure 1(d) [6, 7]. The holes have a much lower mobility than the electrons and move very slowly in the SiO_2 material. The presence of only holes, which have a positive charge, in the gate oxide causes a negative shift in the MOSFET threshold voltage. When exposed to an electric field, the holes slowly migrate toward the most negative potential within the insulator material. When the most negative potential is the channel, the holes migrate toward the insulator-channel interface as is shown in Figure 1(e, f), increasing the threshold voltage shift from the

initial value. Finally, much more slowly, continuing in some cases for years, the trapped-holes are annealed out of the SiO_2, as shown in Figure 1(g), causing the threshold voltage to shift back toward the initial pre-radiation value [8].

When the most negative potential is the gate and the most positive potential is the channel, as typically occurs in a p-channel MOSFET, the holes migrate toward the insulator-gate interface causing the shift in the threshold voltage to decrease from the initial voltage shift, resulting in a smaller, long term shift. This is the primary reason that a p-channel metal-oxide-semiconductor (PMOS) FET threshold voltage is much less affected by hole trapping than a n-channel metal-oxide-semiconductor (NMOS) FET threshold voltage in digital complementary metal-oxide-semiconductor (CMOS) circuits.

One additional phenomena that is observed at total dose levels above 1×10^5 rads(Si) is the creation of interface states generated by breaking bonds at the SiO_2-channel interface [7]. The interface states leave a negative charge at the boundary of the gate oxide and the FET channel and thus affect the threshold voltage.

2.2.2 Parameter Changes Due to Ionizing Radiation. The most significant property affected in MOS transistors by ionizing radiation is the shift in threshold voltage, primarily due to the trapped-holes in the SiO_2 gate insulator [1]. At high total dose levels, interface states leave a negative charge offsetting the effect of the trapped holes in the SiO_2. The net effect of the trapped holes and the interface states to the threshold voltage for NMOS FETs is to negatively shift the threshold voltage at low dose levels and positively shift the threshold voltage at high dose levels, as shown in Figure 2. For PMOS FETs, the threshold voltage is shifted negatively at all dose levels, due to the

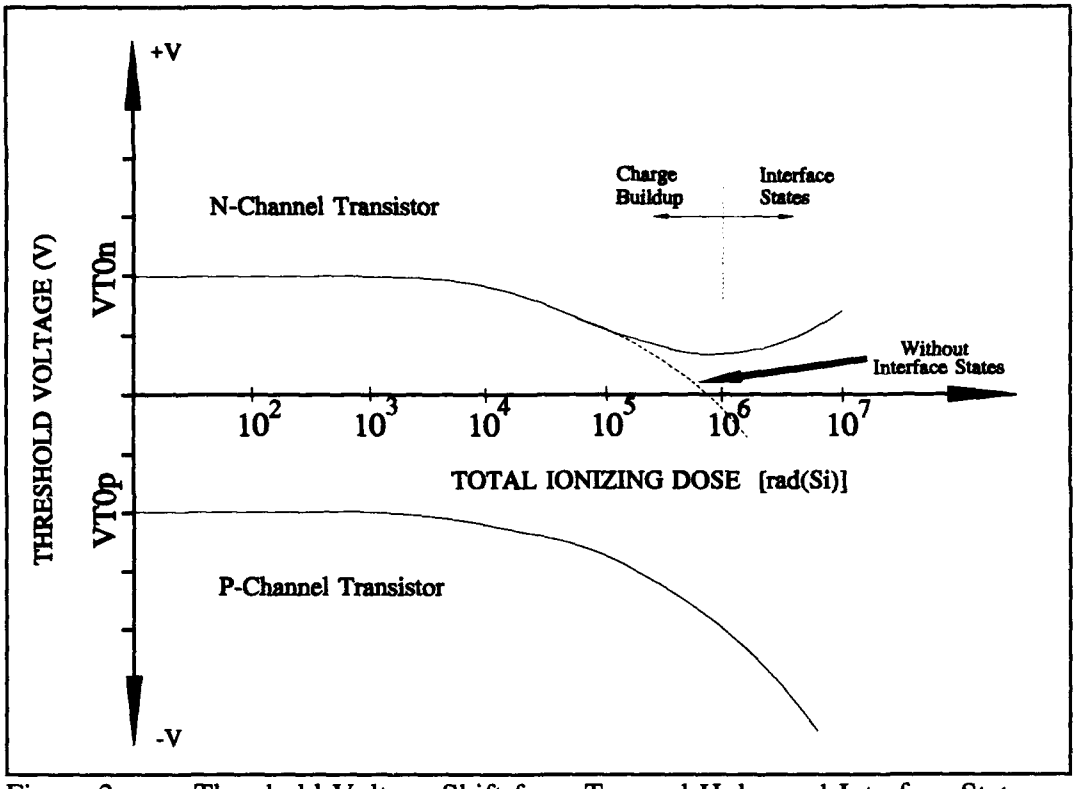

Figure 2. Threshold Voltage Shift from Trapped Holes and Interface States.

trapped holes and interface states working together. Designing CMOS circuits to survive high levels of ionizing radiation must incorporate gate oxide fabricated as thin as possible in order to minimize the number of trapped holes generated during irradiation. The shifts in threshold voltage that do occur must be accounted for in the circuit modeling effort.

2.3 Neutron Irradiation

2.3.1 Physical Effects of Neutron Irradiation. Neutron irradiation damages silicon crystalline structure, creating defects in the material that act as traps for the carriers, effectively removing majority carriers from the semiconductor material. MOSFET devices are less affected by dislocation damage, caused by neutron irradiation, than are bipolar devices. The dislocation damage in the semiconductor material is caused

when neutrons passing through break bonds in the semiconductor crystalline structure and knock atomic bonds out of position. The greatest change noted in MOS transistors is a change in channel conduction. In n-channel MOS transistors, neutrons cause a decrease in effective hole density in the p-substrate [7]. In p-channel MOS transistors, neutrons cause a decrease in effective electron density in the n-substrate. In both the n-channel and p-channel MOSFETs, conduction is reduced by exposure to neutron irradiation.

Dislocation damage also occurs in the insulating oxide (SiO_2) layers throughout microelectronic circuits. This damage is not limited to the gate oxide but also includes the oxide layers used to insulate various power and signal lines from each other. The damage to the insulator can increase current leakage through the insulator material.

2.3.2 Parameter Changes Due to Neutron Irradiation. By removing the carriers, neutron irradiation causes an increase in the resistance of the semiconductor material. In MOSFETs, the channel resistance is increased due to majority carrier removal in the channel [1]. Polysilicon traces also experience an increase in resistance due to carrier removal caused by the neutron irradiation. A further artifact of the dislocation damage and resultant majority carrier removal is higher levels of minority carriers in the channel. The increased minority carrier level lowers the gate voltage necessary to invert the channel, shifting the threshold voltage closer to zero and making it easier to turn the transistor on. In both p-channel and n-channel MOS transistors, neutron irradiation makes it easier to turn on the transistor and decreases the drive capability of the transistor while it is on. Decreased drive is caused by the decreased

majority carrier mobility and increased leakage at each node, while the increased node leakage also makes it easier to turn the transistors on.

Not only is the MOSFET drive capability reduced, the increased polysilicon trace resistance serves to further decrease the effective drive capability of the circuit. Finally, the effect of the dislocation damage is observed in the insulating oxide layers. An increase in leakage current is observed between adjacent circuit elements and traces due to lattice disruptions in the oxide material.

The design of circuits hardened to survive neutron irradiation must incorporate several factors. CMOS circuits designed to survive a high neutron fluence must be designed with a fanout margin that takes into consideration the effect of the neutron irradiation. Transistor size must be increased to account for increased drive required to account for insulator leakage and resistive losses in the polysilicon traces. Transient switching current requirements must be increased since the transistors turn on more easily after exposure to neutron irradiation. So, during a logic transition both the PMOS and NMOS transistors will be more strongly turned on. The microelectronic circuit power supply lines must be sized to account for the increased transistor size, switching current load from the transistors, and circuit insulator leakage.

2.4 Dose Rate Effects

2.4.1 Physical Effects of Dose Rate on MOSFETs. Radiation dose rate affects microelectronic circuits in several ways; photocurrent generation, trapped-hole generation, trapped-hole annealing, increased channel conductivity, and interface state build-up. When radiation passes through silicon, bonds are disrupted, dislocating electrons.

Differing effects are observed depending on whether the dislocation occurred within the bulk material, junction, or oxide layer.

Photocurrent generation is caused by the generation of electron-hole pairs in the PN junction of a diode. The radiation-induced photocurrent flows in the reverse direction within the diode junction. This photocurrent is observed within MOSFET devices in the diode junctions, including those found between the source, drain, and channel-to-bulk material. Additionally, during irradiation, electron-hole pairs are generated in the oxide layer creating an oxide leakage current as the electrons vacate the oxide layer This can be significant if the dose rate is high [9].

After initial hole generation, some of the holes recombine with electrons while the rest slowly migrate to an oxide interface. Then, at a much slower rate, the holes anneal out of the oxide layer, with the complete process occurring over 20 years or more. All effects, except the hole annealing, occur within a few seconds after the radiation exposure. Additionally, during radiation exposure, electron-hole pairs are created in MOS transistor channels, increasing the channel conductivity during the radiation event. Interface states are created at the gate insulator and channel interface, by radiation, upsetting the interface bonds. These interface states create a negative charge at the gate-to-channel interface.

2.4.2 Parameter Changes Due to Dose Rate. Photocurrent generation is a significant concern, not only in conventional diodes and bipolar transistors, but also in MOSFET devices. Photocurrents can become significant, requiring the microelectronic circuit power supply lines to deliver large amounts of current just to sink the radiation generated photocurrents. In most MOS devices, the active elements are fabricated on

bulk silicon material that forms a reverse-biased PN junction for electrical isolation. When exposed to ionizing radiation, the reverse-biased PN junction, from the active MOS device to the bulk material (body/substrate) of the circuit, generates an electrical current. This photocurrent can be eliminated by fabricating and electrically isolating the active devices on an insulator material such as silicon-on-sapphire (SOS) or silicon-on-insulator (SOI) where the insulator is usually SiO_2.

In NMOS transistors, trapped holes cause a negative shift, while interface states cause a positive shift in threshold voltage. At some dose rate, the accumulation of trapped-holes balance the effects interface states at the oxide-to-channel interface, and at the gate-oxide-to-channel interface, and results in lowering the overall shift in threshold voltage. In Figure 3, at a dose rate below one rad(Si) per second and greater, interface states begin to dominate the threshold voltage shift of an n-channel MOSFET, since trapped holes anneal out of the gate oxide faster than they accumulate [8]. Once the rate of trapped-hole accumulation exceeds the rate of annealing, the trapped holes dominate the shift in threshold voltage and cause a net negative shift in threshold voltage. The exact dose rate, where each phenomena is dominant, depends upon the fabrication technology used.

When a circuit experiences a prompt radiation event, MOS transistors will experience an initial negative shift in threshold voltage that will then change with respect to time as the trapped holes anneal out of the gate oxide, as shown in Figure 4. If the interface states did not exit, the threshold voltage would eventually return to its initial value as the trapped holes annealed.

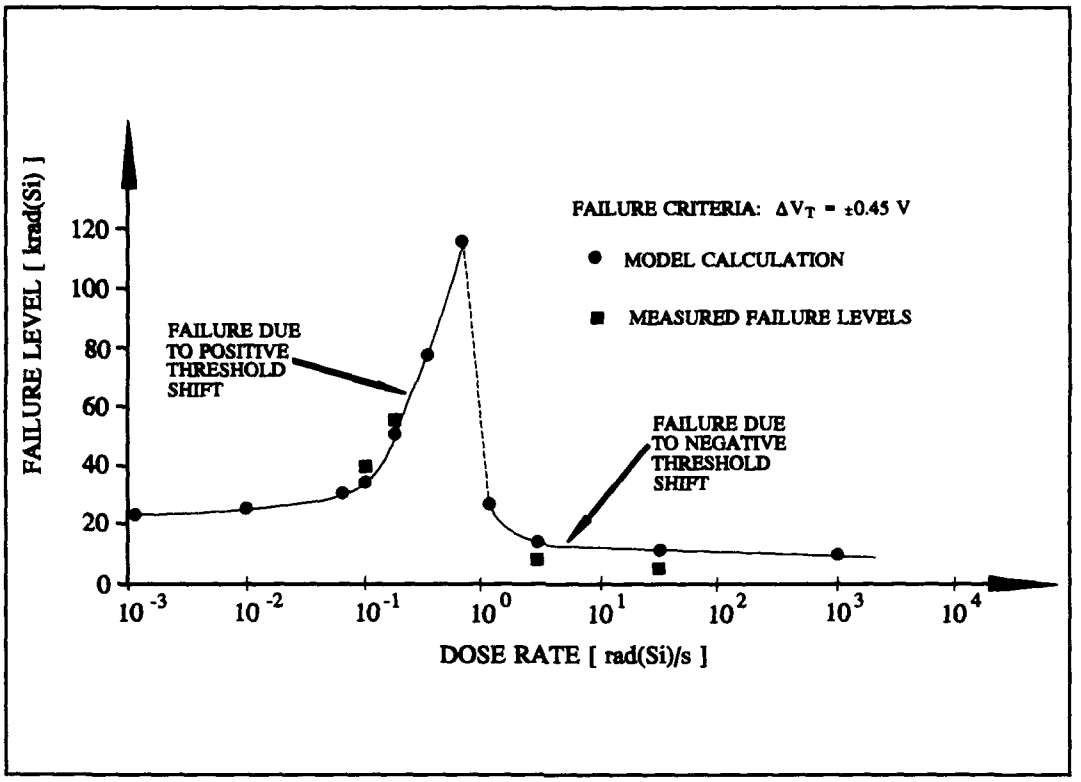

Figure 3. Threshold Voltage Driven Failure versus Ionizing Dose Rate [8].

The rebound of the threshold voltage is due to the interface states which leave a negative charge at the gate-to-channel interface, effectively shifting the threshold voltage by a positive potential [1]. Some argument exists as to whether interface states are created at the time of the prompt radiation event as shown in the top curve of Figure 4, or whether the interface states buildup over time after exposure to the prompt radiation event. In the prompt interface state buildup model, all the interface states are generated during the prompt radiation event. Alternatively, in the time dependent buildup model, interface state buildup begins after the prompt radiation event has occurred and the buildup completes thousands of seconds later. In either case, the transistor threshold voltage shifts initially negative after the prompt event, recovers to the original threshold voltage after some period of time, and then rebounds to a positive threshold voltage shift.

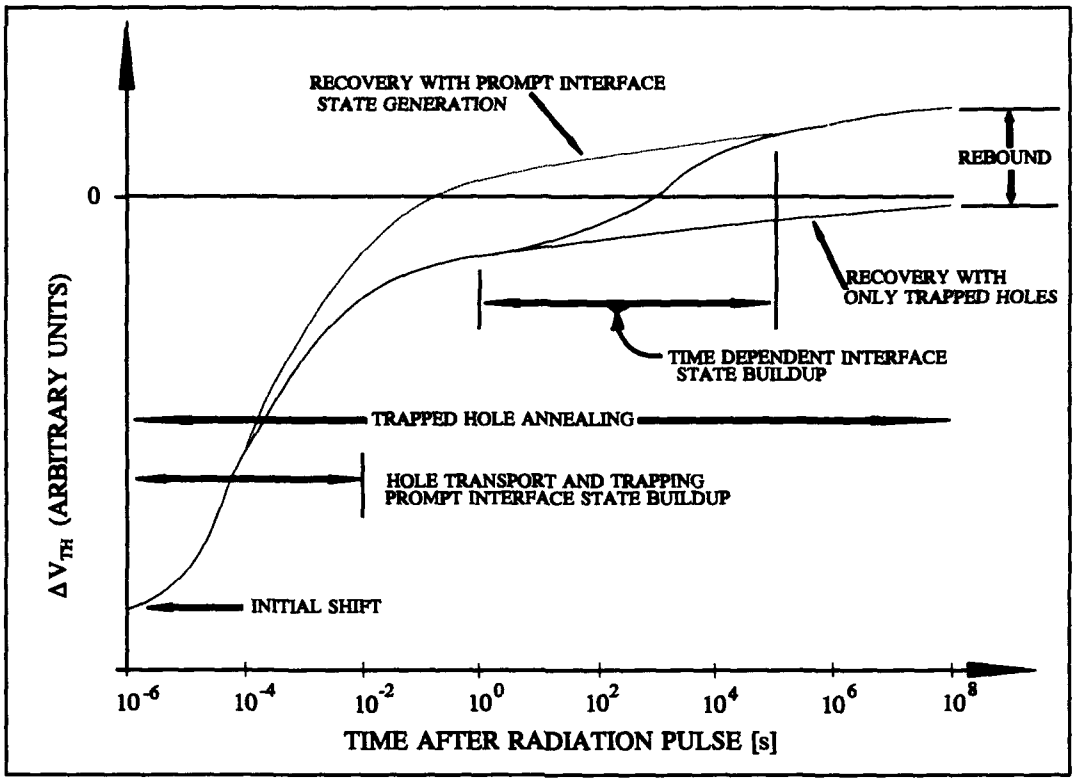

Figure 4. Threshold Voltage Shift due to Single Pulse of Radiation.

2.5 *Summary*

Ionizing, neutron, and the dose rate irradiation have different effects on MOS microelectronic circuits. Ionizing radiation affects the insulating oxide in MOSFETs, causing shifts in threshold voltage. Neutron radiation affects the channel region of a MOSFET, increasing channel resistance and slightly shifting the threshold voltage. Finally, radiation dose rates affect MOS circuits through several mechanisms: photocurrent generation, trapped-hole generation, and trapped-hole annealing. These collectively increase channel conductivity and shift the threshold voltage. All the dose rate effects are time dependent and eventually anneal to stable values. In MOSFET microelectronic circuits, the principal radiation concern is ionizing radiation effects on the threshold voltage.

III. Summary of Current Simulators

3.1 Introduction

Several types of microelectronic circuit simulators available or in development have the potential for evaluating the impact of radiation on microelectronic circuit operation. These simulators include SPICE, PARA, VHDL, MHDL, and AnaVHDL based simulators. SPICE-type circuit simulators, including the equations frequently used, will be discussed. Equations discussed include the Ebers-Moll equations for diodes and the Schichman-Hodges equations for MOSFET circuits. Basic switch-level simulators will be discussed second, with the primary discussion focusing on PARA, a simulator being developed at Vanderbilt University. Next, event driven simulators will be discussed, with the emphasis on various modifications to VHDL. A quick examination of MHDL, an analog simulator, will be included. Finally, a hybrid simulator, AnaVHDL, that combines capabilities of SPICE and VHDL will be presented.

3.2 SPICE-Type Simulators

Several specialized SPICE-type circuit simulators have been modified to include radiation effects in the circuit models, and are used to model the effects of radiation on electronic circuits. SYSCAP, a specialized SPICE-type of circuit simulator that models the effects of radiation on electronic circuits, is owned and used by Rockwell International [1]. Another simulator is RADSPICE which is used by SAIC and is co-owned with Meta Software [1].

The SPICE-type simulators use modified mathematical models to accurately simulate the effects of radiation on microelectronic circuits. Most SPICE-type simulators for radiation-hardened bipolar transistors use modified and expanded Ebers-Moll or Gummel-Poon equation models to include the effects of radiation on the circuits [10]. Many MOSFET SPICE models are available for simulating various MOS technologies; one common model is the Schichman-Hodges model [11]. Unfortunately, radiation-inclusive SPICE-type simulation requires more computer processing time, increasing the amount of time required to simulate a given circuit over non-radiation inclusive SPICE simulations.

An example of a radiation-inclusive large-signal diode used in SPICE is shown in Figure 5 and described by the diode current equation:

$$i_D(t) = \frac{V_D(t)}{R_{DL}} - i_{ppD}(t) + i_{DI}(t) + T_D\frac{d[i_{DI}(t)]}{dt} - \alpha_1 i_{jI}(t) + C_D(t)\frac{d[V_D(t)]}{dt} \qquad (1)$$

where:

$$i_{DI}(t) = I_S\left[\exp\left(\frac{V_D(t)}{M_D\theta}\right) - 1\right], \quad \theta = \frac{kT}{q}$$

$$C_D(t) = \frac{C_{DO}}{(1 - V_D(t)/V_{DBI})^{1/2}} \qquad (2)$$

C_{D0}	-	zero voltage capacitance
I_s	-	reverse saturation current
M_D	-	diode constant, $1<M_D<2$
T_D	-	diode time constant
V_{DBI}	-	built-in diode voltage
α_1	-	current transfer coefficient

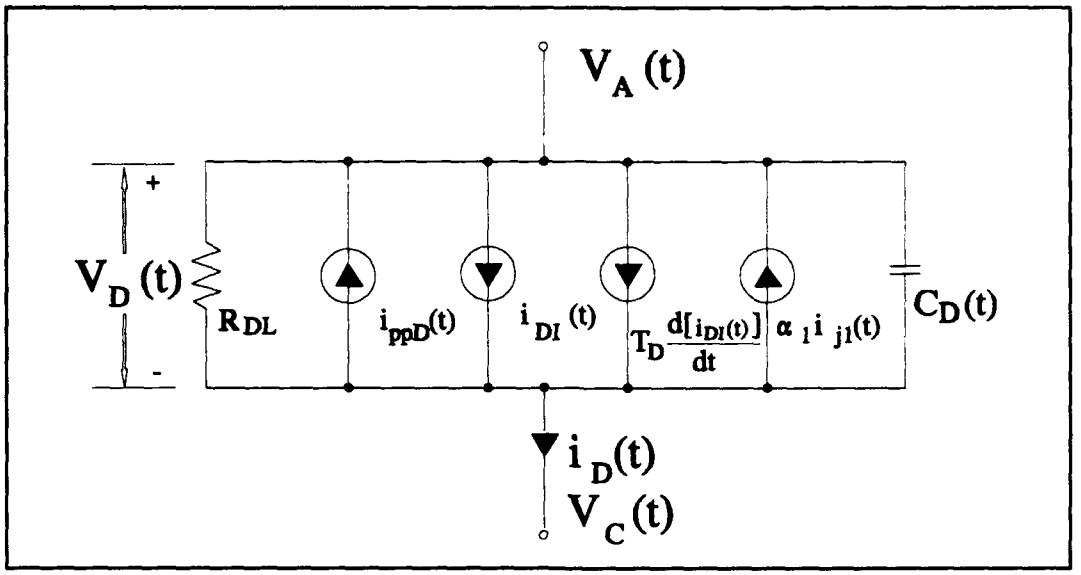

Figure 5. Radiation-inclusive Ebers-Moll Large-signal Diode [1].

The diode primary photocurrent is given by $i_{ppD}(t)$, radiation-induced leakage resistance is included in R_{DL}, radiation-induced parasitic element is given by $\alpha_1 i_{j1}(t)$, and the change in effective capacitance is seen in $C_D(t)$ [1, 12].

A typical radiation-inclusive field effect transistor model in SPICE uses the model shown in Figure 6. The definitions include subscripts for source (*s*), gate (*g*), drain (*d*), and body or substrate (*b*):

R_{gs}, R_{gd}	-	Surface Leakage Resistance
R_s, R_d	-	Dynamic DC Channel Resistance
C_{gs}, C_{gd}	-	Gate Metal/Poly and Source-Drain Diffusion Overlap Capacitance
C_C,	-	Channel to Gate Capacitance
C_B	-	Channel to Body Capacitance
D_{sb}, D_{db}	-	Built-in Source and Drain to Body Diode Junctions
I_s, I_D	-	Source and Drain Radiation-Induced Current Generators

All the listed variables can be affected by exposure to radiation. However, the greatest impact comes from the change to the current sources (I_s, I_D) caused by the change

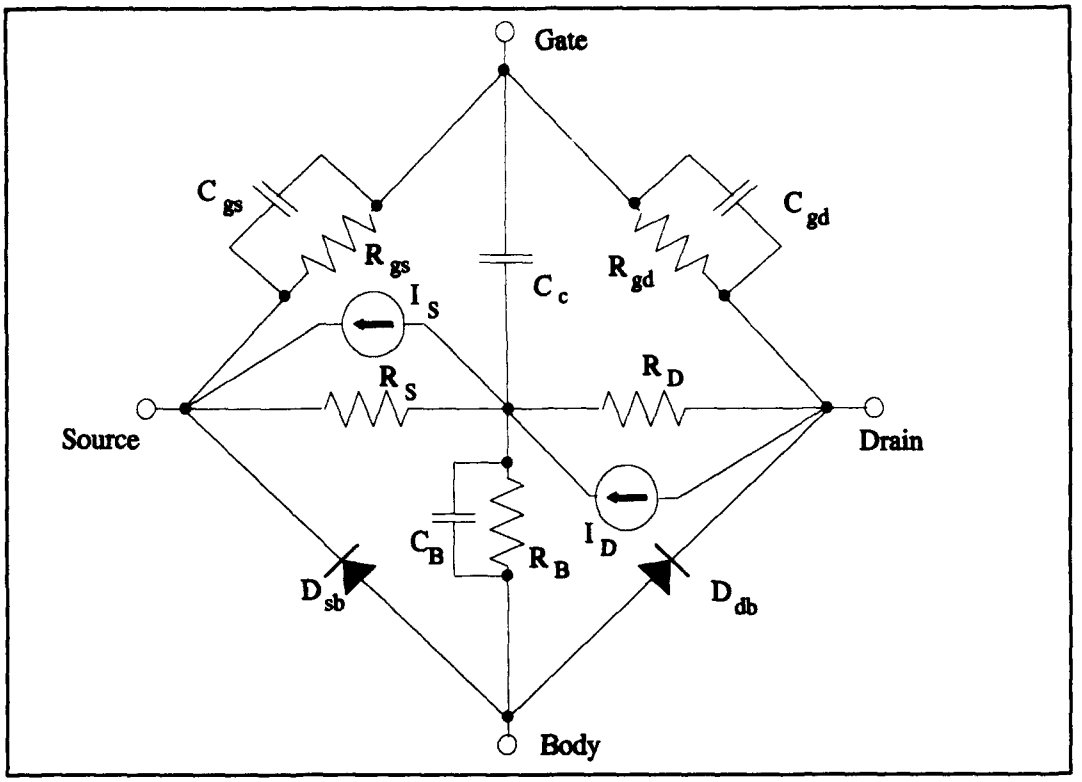

Figure 6. Radiation-inclusive Field Effect Transistor [1].

in the transconductance, effectively shifting the threshold voltage of the MOSFET [1]. When the threshold voltage is shifted, digital circuits may no longer switch states and analog gain curves will change. The indicated diodes D_{sb} and D_{db} also behave like the large-signal diode, shown in Figure 5, where ionizing radiation will induce photocurrents if the MOSFET is not insulated from the bulk material (body).

When the microelectronics are primarily CMOS, other SPICE models, including the Schichman-Hodges model, can be used to simulate circuit operation. In this research, the baseline SPICE simulations were conducted using a Texas Instruments proprietary model based on a modified Schichman-Hodges model. As such, it is important to briefly examine the Schichman-Hodges model as used in CMOS simulation of SPICE

circuits [11]. The primary equation in the Schichman-Hodges model is the current drain-to-source (I_{ds}) equation. I_{ds} is shown in Equation 3 as:

Cutoff Region, $v_{gs} \leq v_{th}$

$$I_{ds} = 0.0$$

Linear Region, $v_{ds} < v_{gs} - v_{th}$, $v_{gs} > v_{th}$

$$I_{ds} = KP \times \frac{W_{eff}}{L_{eff}} \times (1 + \lambda \times v_{ds}) \times \left(v_{gs} - v_{th} - \frac{v_{ds}}{2} \right) \times v_{ds} \tag{3}$$

Saturation Region, $v_{ds} \geq v_{gs} - v_{th}$, $v_{gs} > v_{th}$

$$I_{ds} = \frac{KP}{2} \times \frac{W_{eff}}{L_{eff}} \times (1 + \lambda \times v_{ds}) \times (v_{gs} - v_{th})^2$$

where:

KP	-	Intrinsic Transconductance Parameter
W_{eff}	-	Channel Width, Effective
L_{eff}	-	Channel Length, Effective
λ	-	Channel-Length Modulation
v_{ds}	-	Drain-to-Source Voltage
v_{gs}	-	Gate-to-Source Voltage
v_{th}	-	Threshold Voltage

The primary effect on I_{ds} is the decrease in KP and a shift in v_{th}, as discussed earlier, when the total ionizing dose is increased. The other parameters of the equation are relatively unaffected. W_{eff} and L_{eff} are physical parameters defined by the size of the device and the doping of the silicon. The channel-length modulation factor, λ, is dependent on the doping concentrations of the transistor. The voltages v_{ds} and v_{gs} are the

operating voltages of the device. The threshold voltage, v_{th}, is dependent on the transistor design and the radiation dose observed.

These highly-specialized models, running in SPICE simulators, are accurate in simulating the effects of radiation on microelectronics because the detailed parameter changes are well modeled. The limitation of SPICE comes from the large amount of computing time required to simulate the operation of a circuit. In the interest of designing more complex circuits, other circuit simulators are being developed that require less computing effort.

3.3 Switch-Level Simulators

Switch-level simulators include timing simulators that treat electronic circuits as gates or switches and assign timing delays associated to each gate. Switch-level simulators trade timing accuracy for simulation speed, allowing complex circuits to be quickly simulated. Circuits can be simulated for pre- and post-radiation circuit timing by creating gate-level timing databases for all of the gates both pre- and post-radiation. Alternatively, circuit timing delays may be simulated by creating equations or look-up tables that model circuit delays based on the radiation environment to which the circuit is exposed.

One example of a switch-level simulator is PARA, a program developed at Vanderbilt University [2, 13]. As a simulator, PARA is quite complex in evaluating a microelectronic circuit for power supply-related failures, static failures, and dynamic failures. The worst-case operating parameters for the circuit are assumed and generated for testing. Power supply-related failures are determined by calculating the static current

requirements of the circuit and radiation-induced leakage current. The induced leakage current calculations assume that the outputs of 50% of the logic gates are logic high and the rest of the outputs are logic low. More accurate calculations could be made at the cost of simulation time by determining the actual state of the logic gates during irradiation. In Very Large Scale Integration (VLSI) designs, it is impractical to actually predetermine the gate states for the power supply-related leakage currents. The leakage currents are higher in gates that are logic high during radiation exposure, so the total microelectronic circuit leakage current is calculated by PARA using the average of the two leakage currents. All the currents are summed, the results are reported, and, if the total current is within specifications, the test continues. Otherwise, the test is halted.

Assuming the microelectronic circuit passes the PARA power supply-related test, the circuit is then analyzed for potential static failure modes. PARA evaluates all circuit elements for potential stuck-at faults. Potential nodes for stuck-at-0 faults are identified by evaluating the ratio of n-path leakage current to minimum p-path conductance, as seen in Figure 7. If the n-path leakage to p-path conductance exceeds a programmed value, the node is identified as a potential static stuck-at-0 fault. Stuck-at-1 faults are analyzed in a similar manner. If the p-path leakage approaches the minimum n-path conductance, the node being evaluated is identified as a potential stuck-at-1 fault.

When all the static faults are identified, the designer then modifies current sinking and sourcing to design specifications. After all power supply and static tests are passed, PARA conducts the dynamic failure mode test. Dynamic failures are identified by the increased node-to-node delay incurred by decreased node current drive capability caused by decreased carrier mobility and increased leakage currents at each node. PARA uses

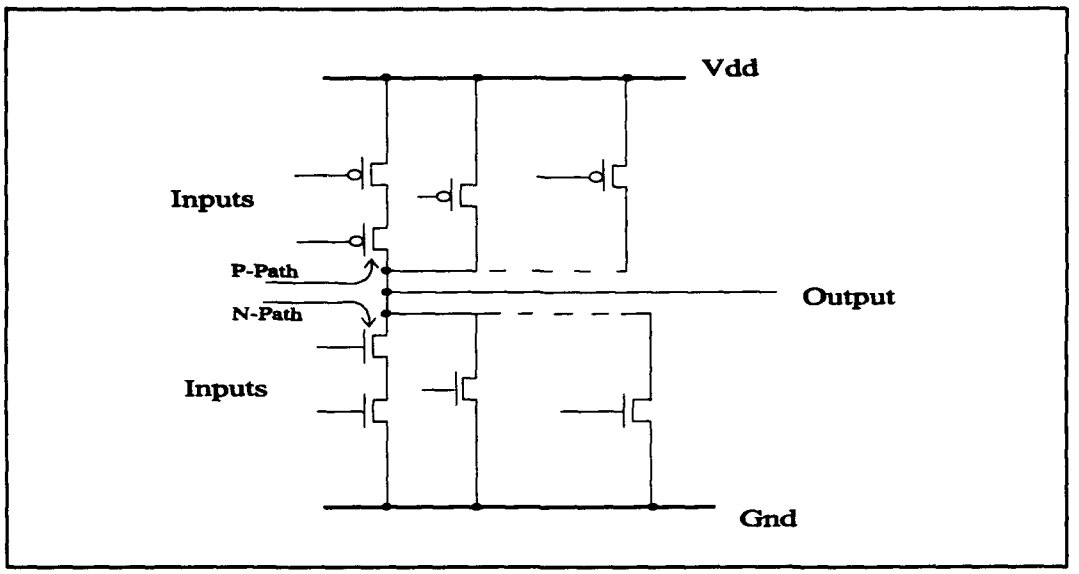

Figure 7. MOS Microelectronic Circuit Showing N-path and P-path Currents.

simple resistor-capacitor (RC) delay calculations at the switch-level of the MOS circuitry to estimate the increased delay time at each node.

To increase the efficiency of the dynamic failure testing, PARA identifies the post-irradiation input vector that results in the worst-case path delay from an input node to an output node. PARA reports the path delays and devices in each path to the designer for verification. To insure complete coverage of all circuit parameters, PARA calculates the effect of irradiating the circuit for all possible combinations of operating conditions. Independently, each input is set low during irradiation, then tested for both low-to-high and high-to-low transitions, and then reset to high and again tested for both low-to-high and high-to-low transitions. This stepping procedure is repeated until all input signals are passed from the inputs to the output nodes. After completion of the tests, the worst-case paths are reported to the designer. Designers can use PARA to make iterative and incremental changes to meet specifications in the design of radiation-hardened microelectronic circuits.

Several test circuits were processed through PARA and the results were validated using SPICE. Test circuits included a chain of twelve inverters connected in series, an 8-bit full adder, a 4-bit carry look-ahead adder, and a 128-bit static random access memory (SRAM) column. In every case, PARA was able to identify the failure mode or correctly model the worst-case delay.

PARA is not without its limitations. By using node-level exhaustive input condition analysis of the microelectronic circuits, PARA simulation speeds do not improve over SPICE simulation speeds as circuits become large [13]. Tests of PARA reported speed improvements over SPICE for the small circuits, but reported slower run times for the large circuits tested.

Correctable inefficiencies in the matrix manipulation algorithm were identified as the cause for the poor large circuit performance. Using efficient algorithms for processing the matrices, such as those used in SPICE, would allow PARA to simulate circuits faster than SPICE even on large circuits [13]. The slow run time to test large circuits currently makes PARA unsuitable for VLSI circuit analysis and simulation. Other simulators are necessary to test and accurately simulate complex microelectronic circuits.

3.4 VHDL-Based Simulators

VHDL-based simulators have the advantage of being written in a language that is mature and accepted by the Department of Defense (DoD) and the Institute of Electrical and Electronics Engineers (IEEE) under standard 1076 for use in design and development of microelectronic circuits [5]. Several vendors, including Synopsys and Vantage, have developed design systems around VHDL. None of these design

environments include the incorporation of radiation effects into their system designs. One company, LSI Logic, is taking the first step in incorporating radiation effects into a VHDL environment [3].

LSI Logic has designed a library of electronic logic circuits based on radiation hardened gate-arrays that have been analyzed for timing performance both pre- and post-radiation. The timing data is placed in two VHDL libraries, both pre- and post-radiation exposure, for each logic circuit that LSI Logic makes, allowing the user to design custom circuits using their library and simulate the circuit for timing performance.

The limitation of the LSI Logic approach is that the block-level design is limited to a library set of circuits based on gate-array design. The timing data is provided for the microelectronic circuit blocks before radiation exposure and after exposure to 1 Mrad(Si) total dose [3]. Unfortunately, the timing delays associated with each block are only recorded for two separate exposure levels, zero dose and 1 Mrad total dose. While this method is useful for LSI Logic's application, the overall usefulness is limited in more generalized applications.

Extensive research is being conducted in using VHDL as an accurate timing simulator in the non-radiation inclusive environment. Several methods of providing accurate methods of timing simulations are being researched. The method most used for accurate timing estimation is back-annotation of timing delays in circuit sections [14]. Back-annotation of timing delays involves the collection of timing delay information on blocks of circuits and then entering the delay information into the VHDL code representing the circuit. The collection of timing delay information may be accomplished by one of two methods. The circuit may be simulated by an accurate timing simulator

such as a SPICE-based simulator or the circuit may actually be fabricated and the delay information can then be measured. The use of a SPICE-based simulator is the most common method of collecting timing information for circuit blocks. Back-annotated VHDL code is then used to simulate the operation and timing performance of much larger circuits, ones that are difficult to simulate using SPICE due to the long, CPU-intensive, simulation run times.

Back-annotation is not ideal, and suffers from one potentially serious error source. If the design of a circuit is such that a major portion of the timing delay occurs at the circuit-block interface, timing estimates can easily lose accuracy. Back-annotation methods can accurately model only the timing characteristics within a circuit block. The timing delays at the boundary of the circuit block are not normally modeled. Effects of circuit drive and fanout loading to include parasitic line loads require special efforts to be modeled accurately.

One correction to the potential loss of accuracy in back-annotated timing models is to insert timing delay blocks in between circuit blocks to account for timing delays due to different capabilities in circuit drive and effects of fanout and wire loading [15]. The individual block delay time can be either estimated or determined by SPICE simulation of the circuit boundary elements. In either case, the fanout load must be known in order to provide accurate timing estimates.

The other approach to increasing the accuracy of timing estimation uses multi-valued logic to simulate the actual operation of a circuit. In this approach, there exists not only the logic '0' and logic '1' values, but also logic values that represent intermediate voltage values. The drive capability, load capacitance, and intermediate

voltage values are used to estimate the time delay as a logic state transition occurs [16]. Load capacitance is input in this simulation scheme via generic declarations, and non-default values must be manually inserted before simulation run time. Thus, the load capacitance must be back-annotated if timing accuracy is necessary. This provides an accurate method of simulating the slew rate of various logic circuits for varying fanout loads. Reported accuracy for this method agrees with baseline results to within 5 percent for the circuits tested [16]. This approach yields good accuracy at the cost of several complex calculations per transition.

3.5 MHDL Simulator

Microwave Hardware Description Language (MHDL) is in development as an outgrowth of VHDL, which was discussed in the preceding section. MHDL is a simulation environment for the operation of solid state microwave circuits and transfer functions [17].

The computer code is similar in structure to VHDL. MHDL requires attributes, variables, and signals all to be declared in a fashion similar to VHDL. Logic gate inputs and outputs are defined as connectors, while the use of external package attributes are commanded with the term "inherits" instead of the VHDL term "use". Different terms aside, the structure of the two simulation languages are similar.

As in VHDL, both behavioral and structural circuit descriptions are allowed. Unlike VHDL, many variable types are predefined, such as frequency, force, length, mass, phase, power, time, unit multipliers, and voltage. Additionally, MHDL may be used to simulate transfer functions using mathematical formulas in the complex domain [17].

Other mathematical capabilities of MHDL include incorporation of spreadsheet design tools to facilitate prototyping of complex designs.

While MHDL has interesting prospects, it is still early in development with the Language Reference Manual (LRM) being revised and modified on a frequent basis. After maturity, MHDL has the potential to be a tool for the design of radiation-hardened electronics. Developers and users of VHDL could possibly benefit by the incorporation of the mathematical functions and tools contained in MHDL.

3.6 Hybrid Simulators

Under development, for generic microelectronic circuit simulation, are a class of simulators that combine more than one type of simulation method in order to simulate the operation of a circuit. This may be accomplished to provide greater accuracy or fidelity in a subsection of a circuit without incurring the penalty of simulating the entire circuit with a high fidelity circuit simulator such as SPICE. Alternatively, one type of simulator may be used for the simulation of analog circuitry while the other simulator may be used for digital circuitry.

One example of a hybrid simulator is Analog VHDL (AnaVHDL), in development at the University of Cincinnati [18]. AnaVHDL combines the capabilities of SPICE and VHDL into a single simulator system in an attempt to gain the benefits offered by each type of simulator. AnaVHDL uses a slightly modified SPICE deck and the SPICE differential equations to simulate sections of a circuits that are analog or require high fidelity. The remainder of the circuit being simulated uses normal VHDL to simulate digital circuit operation.

The VHDL portion of AnaVHDL operates like any other VHDL simulator providing logic state and basic delay time information. The SPICE portion of AnaVHDL is written in VHDL but simulates the DC and transient operation of a circuit using SPICE algorithms. While AnaVHDL provides some benefit over conventional SPICE simulators, the computational-intensive SPICE algorithms limit potential speedup. Potential radiation-inclusive applications for AnaVHDL include using the analog portions of the simulator to simulate the critical timing paths of a microelectronic circuit. In this case, AnaVHDL would simply run existing SPICE models in the critical portions of a circuit.

3.7 Summary

Three major classes of circuit simulators are available or in development for evaluating radiation-hardened circuits. SPICE-based simulators are the most accurate and widely available for designing radiation-hardened microelectronic circuits. The need for faster circuit simulators has led to the development of switch-level simulators that execute faster than SPICE. These simulators must provide both accurate circuit function and timing estimates. Finally, in an attempt to combine the potential benefits of SPICE and switch-level simulators, hybrid simulators are being developed.

More work is needed in the development of circuit simulators that operate quickly, allowing circuit designers to design and simulate complex circuits in a timely manner. Using VHDL is a potential candidate, since VHDL design systems already exist complete with accepted standards. Only library model generation and delay time calculation are required to implement the capability of modeling microelectronic circuits both before and after exposure to radiation.

IV. Model and Simulator Library Development

4.1 Introduction

This chapter outlines the decision process used in choosing a simulator, followed by the development of the models representing the operation and time delay characteristics of the microelectronic circuits. A simulator library needed to be developed that would accurately and efficiently implement the models after the models were developed.

Section 4.2 outlines the selection of a fast simulator for implementing the timing models. Section 4.3 discusses the development of the models and the resulting equations. Section 4.4 describes the development of the simulator library necessary to implement the timing models.

4.2 Simulator Selection

In the last chapter, several different types of circuit simulators were discussed, each with advantages and disadvantages. For this research, a simulator was needed that would run efficiently, using the least amount of CPU processing time, while still providing accurate circuit timing estimates. Node-analysis based simulators, such as SPICE and PARA, become slow in simulating the operation of circuits with more than a few hundred transistors. The slow run time of node-analysis based simulators is due the nature of matrix processing. As the number of nonlinear devices (n) increases, the number of calculations required to process the nonlinear devices increases by n^m where

$1 \leq m \leq 2$ [19]. Algorithms have been developed to improve the processing of sparse matrices, containing many zeros off the diagonal, but the number of calculations required to process a matrix of nonlinear devices still increases by a factor greater than n^1 [20].

A fast simulator, using the lowest amount of computer processing, requires choosing an event-driven simulator, since node-driven simulators waste time processing equations on static nodes. Furthermore, in order to ensure fast run times, the simulator chosen should use just a few simple equations in calculating the event response for each affected node in a circuit. Analog event-based simulators, such as MHDL, require many calculations to process each event. Multi-valued-logic event-base simulators are more efficient than pure analog simulators but many calculations are still required to process each event.

Hybrid simulators present a compromise between the types of simulators, gaining some of the benefits and costs of each simulator incorporated into the hybrid. If short simulation run time is desired, the circuit simulator should remain completely event-driven and use as few calculations as possible to achieve the desired results.

In this research, a VHDL-based simulator was chosen since it is an event driven simulator. Another option would have been to develop a new simulator; however, the effort required to develop a new simulator was outside the scope of this research. To use VHDL, special models have to be developed and implemented in VHDL code, in order to obtain the required timing accuracy while minimizing simulation run time.

4.3 *Model Development*

The goals for development of the timing models are fast execution speed and accurate timing estimates for a large cross section of circuit designs. Three primary factors were the focus of the development of the models. First, the load parameters of each input were considered and modeled. Second, the drive capability of each device was modeled. Finally, the intrinsic delay of each gate was modeled.

The goals required the models to be simple yet accurate. The models must account for various types of logic circuits, including the output drive capability and load each logic gate output must be able to drive. Finally, the timing models must incorporate the capability to account for radiation effects, to include total ionizing dose and ionizing dose rates.

4.3.1 Load and Drive Determination. Every useful digital logic gate contains at least one input and at least one output. Several factors must be considered when developing timing models for these logic gates. First, every input has an associated load capacitance and may also have some input leakage resistance in the radiation-inclusive environment. Second, every logic gate has an intrinsic time delay that must be accounted for in the gate delay time estimation. Third, each output has a drive capability which may be thought of in terms of a drive resistance capability.

Input loads were determined first. While the capacitance of MOSFET gates vary, depending on input voltage, an equivalent average may be determined by comparing the results of delay time measurements obtained for a state transition for both a dynamic input and a fixed capacitive load. Values for the input load capacitance were determined,

by using SPICE, to measure the delay time for a logic gate to change state when connected to the input of a load gate and also when connected to a fixed-value capacitor. The different values of fixed capacitors were selected until the logic gate state transition time delays were within one percent of the value obtained from the dynamic load provided by an actual gate input. The timing accuracy limit was determined by rounding the extrapolated value obtained from SPICE to the nearest base unit value for capacitance used in this research, 1 fF. These measurements, using SPICE, were repeated for several gates. The load capacitance for an input composed of one PMOS (L = 0.8 μm, W = 12.0 μm) and one NMOS (L = 0.8 μm, W = 6.8 μm) transistor in the Texas Instruments, gate-array, SIMOX process, was measured to be 27 fF. Complex logic gates such as the exclusive-OR (XOR) have more than one CMOS transistor pair per input, and as such, have a higher capacitance load on each input. The XOR gate has two input CMOS transistor pairs per input and thus the load capacitance is 54 fF at each gate input.

Next, the pull-up and pull-down drive capability was determined. In this model development, the output pull-up and pull-down drive capability was evaluated independently, since the values of the pull-up and pull-down varied by factors of two to three (based on initial SPICE simulation of the Texas Instruments, SIMOX gate-array, inverter and NAND gates). The next task required selecting a simple model, capable of accurate timing estimates. Simulators discussed earlier, such as PARA and the multi-valued VHDL, use the product of drive resistance and the sum of load capacitances to determine the propagation delay time of a logic gate [13, 16, 21].

In this model, the drive capability is represented as an equivalent resistance parameter and is determined by measuring the logic propagation delay time for various

loads connected to the output. The load capacitances are known constants that are determined beforehand. The pull-up and pull-down propagation delay times are represented by the simple equations:

$$t_{pLH}=R_{pull-up}\times\sum_{i=1}^{n} C_i\ ,\quad t_{pHL}=R_{pull-down}\times\sum_{i=1}^{n} C_i \tag{4}$$

where:

t_{pLH}	-	Propagation Delay Time, Output Going Low-to-High
t_{pHL}	-	Propagation Delay Time, Output Going High-to-Low
$R_{pull-up}$	-	Effective Pull-Up Drive Resistance
$R_{pull-down}$	-	Effective Pull-Down Drive Resistance
C_i	-	Capacitance of the i^{th} Load

Since pull-up and pull-down propagation delay times are considered separately, independent values for $R_{pull-up}$ and $R_{pull-down}$ must be developed.

$R(i)_{pull-up}$ and $R(i)_{pull-down}$ were calculated by measuring the different pull-up and pull-down propagation delay times when a logic gate output was connected to differing numbers of inverter loads in configurations representing fanouts from zero to ten. The change in the pull-up and pull-down propagation delay time, as measured in SPICE, was compared for each of the ten different fanout loads to the calculated pull-up and pull-down propagation delay time using the equations:

$$R(i)_{pull-up}=\left(\frac{(t(i)_{pLH}-t(i-1)_{pLH})}{C_{load}}\right),\quad R(i)_{pull-down}=\left(\frac{(t(i)_{pHL}-t(i-1)_{pHL})}{C_{load}}\right) \tag{5}$$

where:

$R(i)_{pull-up}$	-	Effective Incremental Pull-Up Drive Resistance
$R(i)_{pull-down}$	-	Effective Incremental Pull-Down Drive Resistance

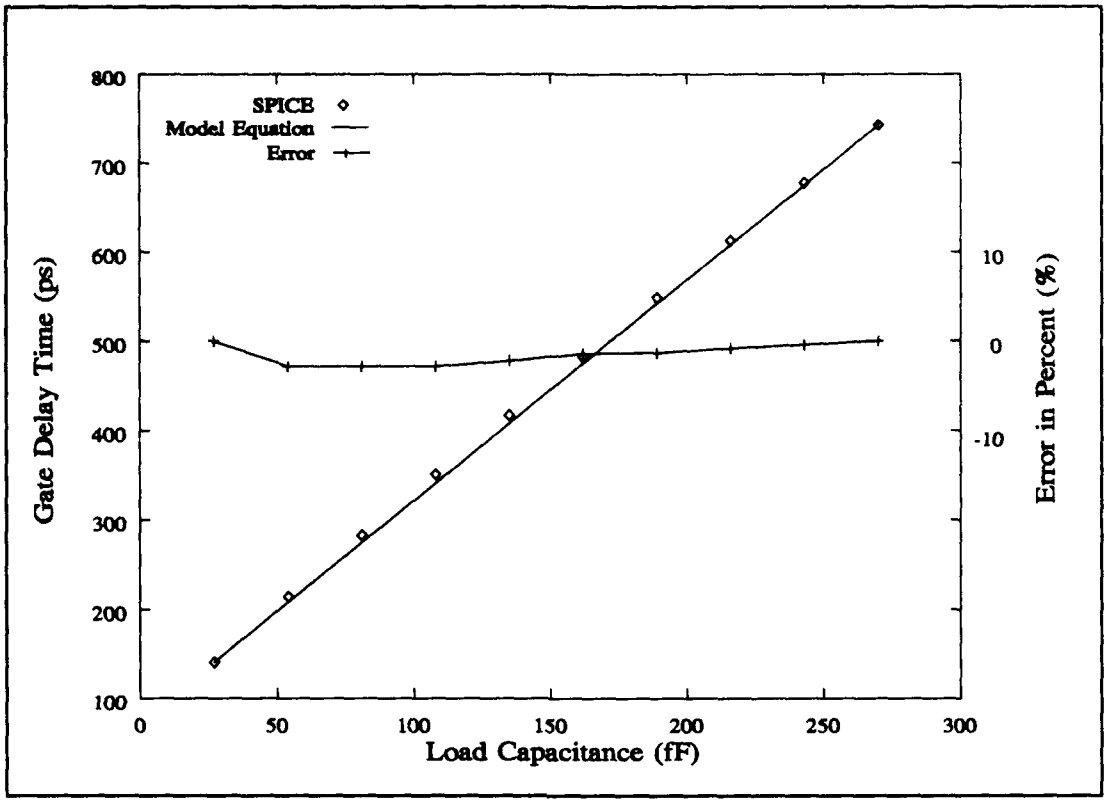

Figure 8. Pull-Up Fanout Modeling Error, Two-Input NAND Gate.

$t(i)_{pLH}$	-	Propagation Delay Time, Output Going Low-to-High, Fanout = i
$t(i)_{pHL}$	-	Propagation Delay Time, Output Going High-to-Low, Fanout = i
C_{load}	-	Load Capacitance = 27 fF

The incremental output resistances $R(i)_{pull\text{-}up}$ and $R(i)_{pull\text{-}down}$ were observed to be within three percent of being a constant value. Assuming a constant value, $R_{pull\text{-}up}$ and $R_{pull\text{-}down}$ were calculated using the equations:

$$R_{pull\text{-}up}=\left(\frac{(t(10)_{pLH}-t(1)_{pLH})}{10\times C_{load}}\right),\quad R_{pull\text{-}down}=\left(\frac{(t(10)_{pHL}-t(1)_{pHL})}{10\times C_{load}}\right) \tag{6}$$

Evaluation of the model results for the two-input NAND gate is shown in Figure 8, with the diamond points representing the measured values obtained using SPICE. The solid line represents the values calculated from the model equations and the error is shown with the line containing the vertical tick-marks and uses the scale on the

right side of the graph. Note that the error is less than three percent for all load values from 27 to 270 fF.

One special consideration, in determining the drive resistance, was the necessary allocation of rise and fall time compensation to be embedded into the drive resistance value. Rise and fall time compensation is required because the propagation delay time of a logic gate is dependent upon the rise and fall time of the input drive signal, as shown in Figure 9. The two-input NAND gate fall time shows the high-to-low fall time for a NAND gate with its output connected to five gate inputs, as shown in Figure 10. In Figure 9, the inverter after NAND shows the output fall time for the inverter being fed a signal from the two-input NAND gate. The inverter in the chain displays the fall time for an inverter embedded in a chain of inverters, with each feeding exactly one inverter. Note the inverter being fed a signal by the NAND gate has a slower fall time than the inverter embedded in the chain of inverters.

Rise and fall time compensation is accomplished by measuring the propagation delay time of a gate after passing its output through an inverter, as shown in Figure 10. The fanout loads are composed of inverters connected in parallel. The propagation delay time of a single fanout inverter is then subtracted from the total propagation delay time. The resulting rise and fall propagation delay times are then assigned to $t(i)_{pLH}$ and $t(i)_{pHL}$, respectively. This method of determining the delay through a gate, feeding a fanout greater than one, allows for accurate overall timing estimates by compensating for the greater than normal propagation gate delay times in a load gate caused by the slow rise and fall times of the driving gate.

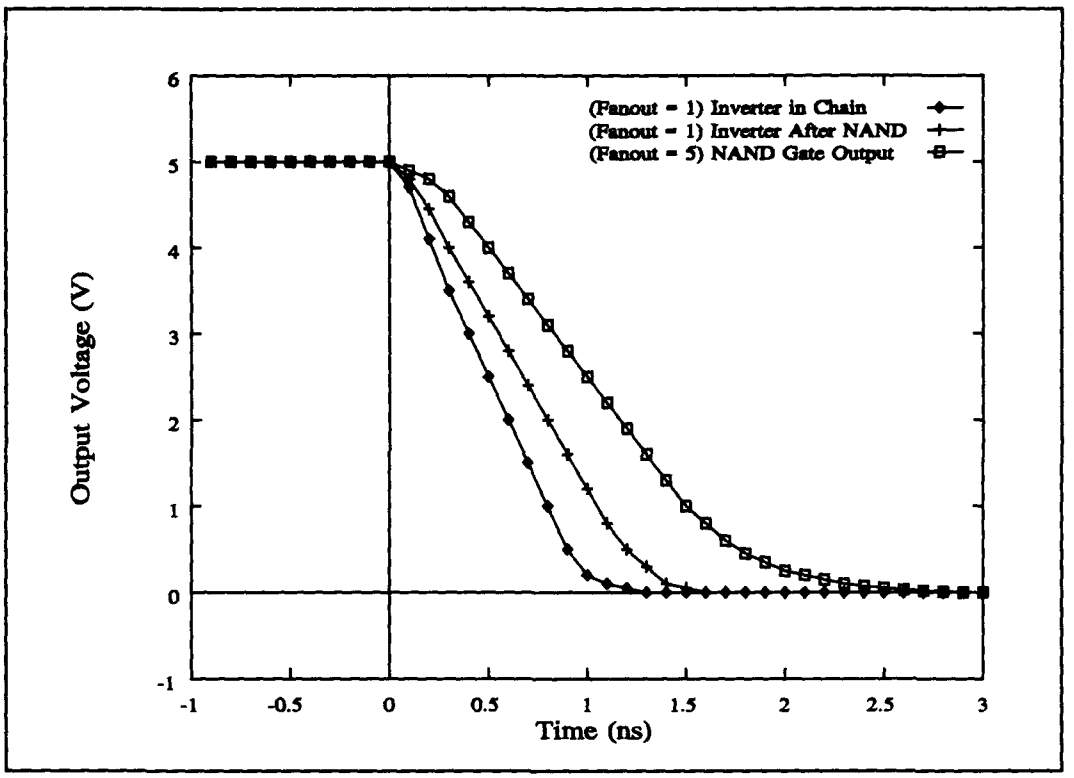

Figure 9. Fall Times for NAND Gate with Inverters and Chained Inverters.

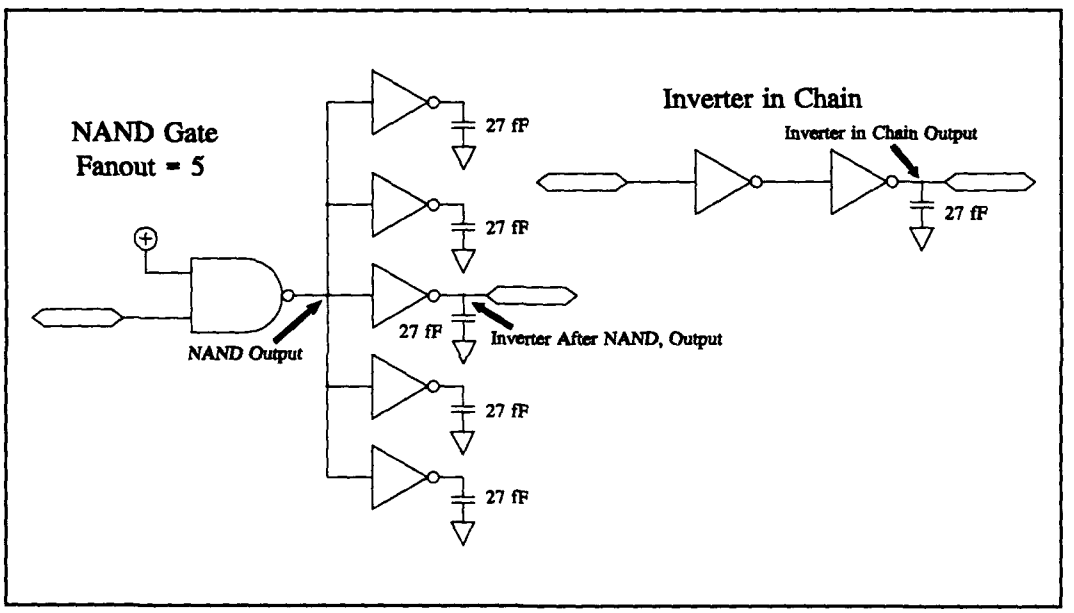

Figure 10. A NAND Gate Loaded with Five Inverters and an Inverter Chain.

The pull-up and pull-down drive resistance terms are easy to calculate once the measurement circuits are setup for each of the logic gates. The drive resistance values

in conjunction with the load capacitance combine to makeup two of the three terms required to model the total propagation delay time of a logic gate. The last parameter, the logic gate internal intrinsic delay time, needs to be calculated last. The total delay time of a logic gate is given by the equation:

$$t_{tLH}=t_{pLH}+t_{intLH}\ ,\quad t_{tHL}=t_{pHL}+t_{intHL} \tag{7}$$

where:

t_{tLH}	-	Total Gate Delay Time, Output Going Low-to-High
t_{tHL}	-	Total Gate Delay Time, Output Going High-to-Low
t_{intLH}	-	Internal Intrinsic Gate Delay Time, Output Going Low-to-High
t_{intHL}	-	Internal Intrinsic Gate Delay Time, Output Going High-to-Low

The last parameter determined in the pre-radiation time delay model was the intrinsic delay of the logic gate. Since each gate already has a pull-up and pull-down resistive drive capability, the intrinsic delay was represented by a capacitance value. This capacitance would be summed along with all the load capacitors and then multiplied by the pull-up or pull-down drive resistance value to determine the overall logic gate time delay as shown in the equations:

$$t_{tLH}=R_{pull-up}\times\left(\left(\sum_{i=1}^{n}C_i\right)+C_{pull-up-int}\right),\quad t_{tHL}=R_{pull-down}\times\left(\left(\sum_{i=1}^{n}C_i\right)+C_{pull-down-int}\right) \tag{8}$$

where:

$C_{pull-up-int}$	-	Internal Intrinsic Pull-Up Capacitance
$C_{pull-down-int}$	-	Internal Intrinsic Pull-Down Capacitance

The determination of each logic gate intrinsic delay time capacitance was accomplished by making a delay time measurement, in SPICE, of the logic gate total time

delay connected to a nominal fanout load of 27 fF. The intrinsic delay time capacitances were determined by the equations:

$$C_{pull-up-int} = \left(\frac{t_{tLH}}{R_{pull-up}} \right) - C_{load}, \quad C_{pull-down-int} = \left(\frac{t_{tHL}}{R_{pull-down}} \right) - C_{load} \tag{9}$$

The radiation-inclusive model VHDL descriptions as developed to this point may be implementated as a non-radiation environment timing simulator. The radiation-inclusive parameter variables and the radiation effects procedure calls are not incorporated in the generic declarations of the VHDL descriptions, simplifying the descriptions for use as a non-radiation environment timing simulator. VHDL model descriptions based on the models developed to this point allows designers to adapt the models for use in circuit design when radiation effects are not a concern, while retaining the timing accuracy of the radiation-inclusive VHDL models. Simulation run time will be faster than the complete radiation-inclusive VHDL models but still slower than base VHDL.

4.3.2 Radiation Effects. The effect of radiation, both total dose and dose rate, must be accounted for in the timing models of the logic circuits. First, total ionizing dose was considered with the level being fixed at the 1 Mrad(Si) level due to limitations in the radiation-inclusive SPICE models available. Second, dose rate was modeled with the dose rate varied from 1×10^{9} to 2×10^{12} rads(Si) per second. Initial testing was conducted for dose rates ranging from 1×10^{8} to 1×10^{14} rads(Si) per second. The lowest dose rate where a change was observed in timing performance of any gate was 1×10^{9} rads(Si) per second. The highest dose rate where the combinational logic gates still operated was 2×10^{12} rads(Si) per second.

The total ionizing dose radiation-inclusive SPICE models included only data for the 1 Mrad(Si) dose level. Thus, the models developed include only this level of total dose modeling. SPICE simulations were rerun for all the tests described in Section 4.3.1 and the net effect on the logic gates was to increase the effective drive resistance and intrinsic delay time, while the input load values remained constant. The effective delta drive resistance was calculated for each logic gate using the equations:

$$\Delta R_{pull\text{-}up\text{-}p} = \left(\frac{(\Delta t(10)_{pLH} - \Delta t(1)_{pLH})}{10 \times C_{load}} \right) - R_{pull\text{-}up}$$
$$\Delta R_{pull\text{-}down\text{-}p} = \left(\frac{(\Delta t(10)_{pHL} - \Delta t(1)_{pHL})}{10 \times C_{load}} \right) - R_{pull\text{-}down} \quad (10)$$

where:

$\Delta R_{pull\text{-}up\text{-}p}$	-	Delta Pull-up Drive Resistance, Post-Rad
$\Delta t(10)_{pLH}$	-	Propagation Delay Time Rise, Post-Rad, Fanout = 10
$\Delta t(1)_{pLH}$	-	Propagation Delay Time Rise, Post-Rad, Fanout = 1
$\Delta R_{pull\text{-}down\text{-}p}$	-	Delta Pull-down Drive Resistance, Post-Rad
$\Delta t(10)_{pHL}$	-	Propagation Delay Time Fall, Post-Rad, Fanout = 10
$\Delta t(1)_{pHL}$	-	Propagation Delay Time Fall, Post-Rad, Fanout = 1

Thus, the pull-up drive resistance used in calculating timing delays for the total dose environment is the sum of $\Delta R_{pull\text{-}up\text{-}p}$ and $R_{pull\text{-}up}$.

The next step was to calculate the model values for the intrinsic time delay capacitance. The effective delta capacitance was calculated for all the logic gates using the equations:

$$\Delta C_{pull\text{-}up\text{-}int\text{-}p} = \left(\frac{\Delta t_{tLH}}{\Delta R_{pull\text{-}up\text{-}p} + R_{pull\text{-}up}} \right) - \left(C_{load} - C_{pull\text{-}up\text{-}int} \right)$$

$$\Delta C_{pull\text{-}down\text{-}int\text{-}p} = \left(\frac{\Delta t_{tHL}}{\Delta R_{pull\text{-}down\text{-}p} + R_{pull\text{-}down}} \right) - \left(C_{load} - C_{pull\text{-}down\text{-}int} \right) \quad (11)$$

where:

$\Delta C_{pull\text{-}up\text{-}int\text{-}p}$ - Delta Intrinsic Delay Rise Capacitance, Post-Rad

$\Delta C_{pull\text{-}down\text{-}int\text{-}p}$ - Delta Intrinsic Delay Fall Capacitance, Post-Rad

The intrinsic time delay for every logic gate measured increased; however, in some cases $\Delta C_{rise\text{-}p}$ and $\Delta C_{fall\text{-}p}$ decreased because the magnitude of change in the drive resistance was greater than the change in the intrinsic time delays. With values established for the total dose environment, it was then necessary to develop models for the dose rate radiation environment.

The dose rate environment was modeled for a large range of radiation dose rates, from 1×10^{9} to 2×10^{12} rads(Si) per second. The radiation-inclusive SPICE models were examined and the input gates of the MOS transistors were found to be unaffected. As such, the only parameters of the time delay model affected would be the drive resistance and the intrinsic time delay capacitance.

The first task in modeling the logic gate timing delay characteristics was to collect performance data for several different dose rates within the range from 1×10^{8} to 1×10^{14} rads(Si) per second. Initial testing was conducted for dose rates of 1×10^{8}, 2×10^{8}, 5×10^{8}, 1×10^{9}, ... 1×10^{14} rads(Si) per second. The lowest dose rate where a change of 0.1 percent or greater was observed in timing performance of any gate was 1×10^{9} rads(Si) per second. The highest radiation dose rate where the combinational logic gates still operated was 2×10^{12} rads(Si) per second.

The next task was to determine what equations would adequately model the changes in the drive resistance and intrinsic delay capacitance over the specified range. A least-squares curve fitting program was used to fit various equations to the results of the SPICE simulations [22]. Keeping in focus the requirement to keep the timing models fast yet accurate, a polynomial equation was chosen as the equation to be used in the modeling process. A least-squares analysis of a quadratic equation, modeling the changes in timing performance when compared to SPICE simulations at dose rates of 1×10^{9}, 2×10^{9}, 5×10^{9}, 1×10^{10}, ... 2×10^{12} rads(Si) per second, yielded less than one percent error. Reducing the measured dose rate values to 1×10^{9}, 1×10^{10}, 1×10^{11}, 1×10^{12}, and 2×10^{12} rads(Si) per second yielded the similar results with the error remaining below one percent.

Based on the modeling results, data collection for the rest of the circuits was accomplished for the dose rates of 1×10^{9}, 1×10^{10}, 1×10^{11}, 1×10^{12}, and 2×10^{12} rads(Si) per second. The coefficients of the quadratic equation were determined by a least-squares fit for each parameter in the model (drive resistance and intrinsic time delay load capacitance). The equations representing the model parameters for the pull-up or the rising state transition are expressed by the equation:

$$R_{pull\text{-}up\text{-}dr}=R_{pull\text{-}up}+D_R\times R_{pull\text{-}up\text{-}dr\text{-}b}+D_R^2\times R_{pull\text{-}up\text{-}dr\text{-}a}$$
$$C_{pull\text{-}up\text{-}dr}=C_{pull\text{-}up}+D_R\times C_{pull\text{-}up\text{-}dr\text{-}b}+D_R^2\times C_{pull\text{-}up\text{-}dr\text{-}a} \qquad (12)$$

where:

$R_{pull\text{-}up\text{-}dr}$	-	Pull-up Drive Resistance, Dose Rate Inclusive
D_R	-	Dose Rate
$R_{pull\text{-}up\text{-}dr\text{-}b,a}$	-	Delay Time Rise Coefficients, Quadratic Terms "b" and "a"

$C_{pull\text{-}up\text{-}dr}$ - Rise Capacitance, Dose Rate Inclusive

$C_{pull\text{-}up\text{-}dr\text{-}b,a}$ - Delay Time Rise Coefficients, Quadratic Terms "b" and "a"

The equations representing the model parameters for the pull-down or the falling state transition are expressed using similar equations, where pull-up and rise are replaced with pull-down and fall, respectively.

4.3.3 Model Determination Procedures Summary. This section detailed the development and selection of the models used in calculating timing delays for the logic gates in both the pre-radiation and radiation-inclusive environment. SPICE simulations of each logic gate were the source of the data used to develop the models. The process for determining the model variables was accomplished in a 13-step process as outlined in Figure 11. Once the model variables were determined, the models were implemented in a simulator. The implementation of the models into the VHDL simulator is detailed in the next section.

4.4 VHDL Library Development

Development of a VHDL library was intended to facilitate the implementation of a radiation-inclusive VHDL modeling scheme. The initial library development used model parameters for the time delay measurements, both pre- and post- radiation exposure. Load parameters and circuit drive capability used values that were determined by running SPICE simulations and implementing the models developed in the previous section. The initial library of VHDL gates was intended to demonstrate the concept of using VHDL for radiation-inclusive modeling while using a reduced set of logic gates.

1. Determine the load capacitance of the inverter input, one PMOS and one NMOS transistor.
2. Calculate the pull-up drive resistance.
3. Calculate the pull-down drive resistance.
4. Calculate the intrinsic time delay pull-up load capacitance.
5. Calculate the intrinsic time delay pull-down load capacitance.
6. Calculate the post-rad total dose pull-up drive resistance.
7. Calculate the post-rad total dose pull-down drive resistance.
8. Calculate the post-rad total dose intrinsic time delay pull-up load capacitance.
9. Calculate the post-rad total dose intrinsic time delay pull-down load capacitance.
10. Calculate the equation terms for the dose rate pull-up drive resistance.
11. Calculate the equation terms for the dose rate pull-down drive resistance.
12. Calculate the equation terms for the dose rate intrinsic time delay pull-up load capacitance.
13. Calculate the equation terms for the dose rate intrinsic time delay pull-down load capacitance.

Figure 11. Model Variable Computation Process.

The initial VHDL library contained a simple set of logic gates. These included an inverter (IV110), two-input NAND (NA210), three-input NAND (NA310), and a special WIRE cell to propagate signals and information between logic gates. The WIRE cell is necessary in order to back-propagate logic gate and wire load information to the driving circuit when the driving gate fanout is greater than one. In order to back-propagate the driven load to the driving gate, the WIRE cell must back-propagate the sum of all the loads connected to the driving logic gate in order to facilitate logic state propagation delay time calculation.

Incorporating radiation-induced timing changes required drive capability parameter changes to facilitate accurate timing estimates. Radiation effects show up in the models in the form of changed effective drive capability, load resistance, and load capacitance.

4.4.1 VHDL Gate Design. The gate design was accomplished in a fashion that models the operation of a physical VLSI gate in logic operation and timing. The logic operation is accomplished by using Boolean equations that simulate the logic function of

the gates. Timing estimates were empirically derived from SPICE simulations using equations incorporating the effects of changes in loading and radiation environment.

All logic gates contain resistance and capacitance parameters used in determining the time delay of the gate, as shown in Figure 12. The inputs of each logic gate contain load resistance parameter values that represent the equivalent load of the gate. The load resistance, at the input of the logic gate, represents gate leakage if measurable. The capacitance at the gate input represents the input MOS gate capacitance used in determining the load seen by the driving logic gate.

The drive resistance value shown in Figure 12 represents the drive pull-up capability of the logic gate. The capacitance at the output of the gate is used in conjunction with the pull-up drive resistance to calculate the logic gate intrinsic low-to-high time delay.

The pull-up drive resistance value is modified by the radiation-inclusive models to account for exposure to radiation and compensate for changes in drive capability. The capacitance at the output of the logic gate is adjusted after exposure to radiation to account for changes in the logic gates intrinsic time. The model variables are incorporated into the logic gates in the form of generic declarations at the beginning of the VHDL code for each logic gates. The VHDL pseudo-code describing the operation of the two-input NAND gate is contained in Figure 13. The first section of the code establishes the generic declarations. All the timing model values for resistance and capacitance in the pre-radiation, post-radiation, and dose rate inclusive environment are declared within the generic declarations. Next, the port declarations are made, including the logic signal ports and the ports used for passing load values to the logic gate.

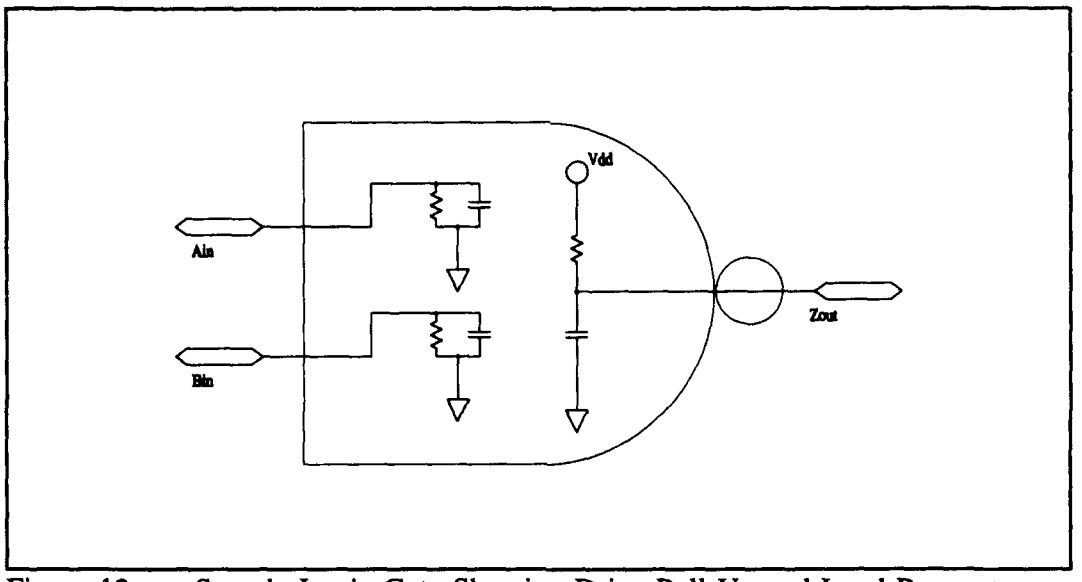

Figure 12. Sample Logic Gate Showing Drive Pull-Up and Load Parameters.

The body of the code has two processes. The first process is used to calculate the effect of the simulated radiation environment on the logic gate resistance and capacitance values. The second process actually defines operation of the logic gate. In this process, the procedure call that determines the logic gate time delay is accomplished and any glitch conditions are reported. A glitch is when an input to a given logic gate is stimulated while the gate is currently undergoing a logic state transistion due to an earlier input stimulation.

The complete VHDL code for two-input NAND gate is contained in Appendix A. The VHDL code in Appendix A contains calls to the three radiation specific procedures used in determining the changes in drive resistance, load capacitance, and gate time delay. These three radiation specific procedures are contained in Appendix B.

The WIRE cell back-propagates the effective resistive and capacitive load information to the driving gate when the fanout is greater than one. The WIRE cell sums the parallel resistances and capacitances and feeds the equivalent load resistance and

```
entity for NA210
  generic declarations for
        pull-up and pull-down resistance and intrinsic capacitance
              Pre-rad
              Post-Rad
              Dose Rate Quadratic Coefficients
        input load resistance and capacitance
  port connections
    radiation_dose        in  dose_record
    A                     in  std_ulogic
    A_load                out signal_load
    B                     in  std_ulogic
    B_load                out signal_load
    Z                     out std_ulogic
    Z_load                in signal_load
end NA210 entity declaration

architecture for NA210
begin
 process (changes to radiation_dose)
  begin
        calculate effect of radiation on
        drive resistance and intrinsic delay capacitance
  end
 process (changes to input A or B)
  begin
   if input A changes then
        calculate radiation inclusive time delay
        if glitch occurs then
            report
        end if
        update time for time delay
   end if
   if input B changes then
        calculate radiation inclusive time delay
        if glitch occurs then
            report
        end if
        update time for time delay
   end if
   update output Z
  end process
end architecture
```

Figure 13. Two-Input NAND Gate (NA210) Algorithm.

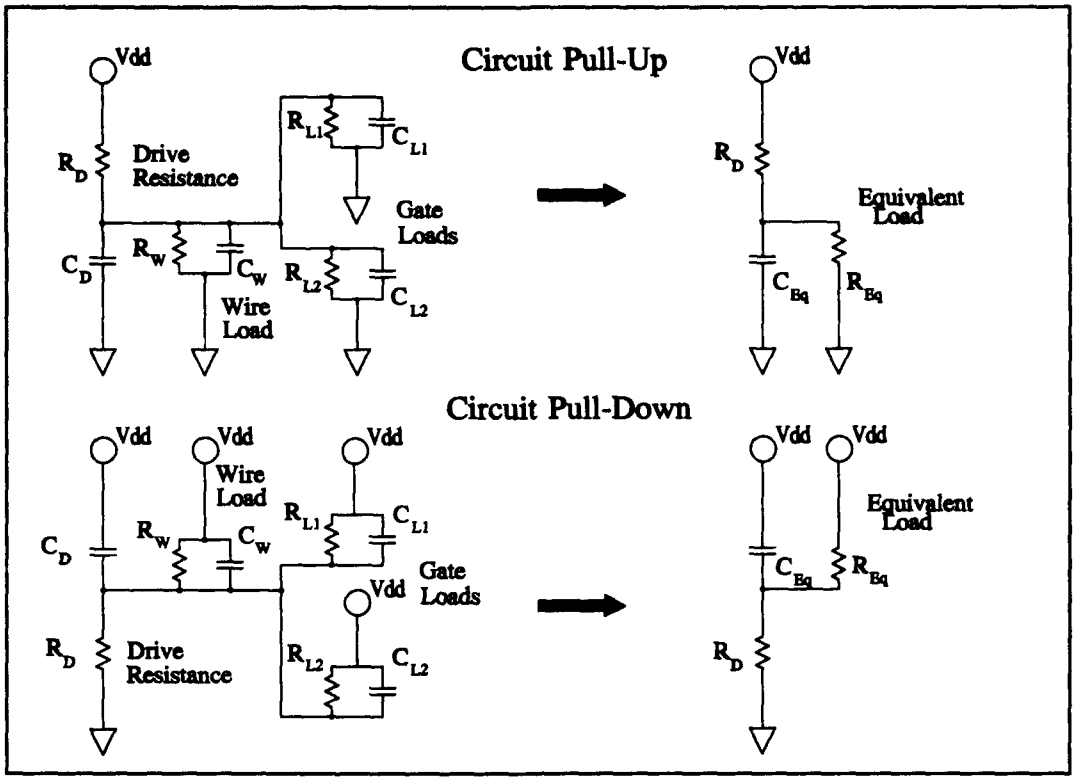

Figure 14. Equivalent Load Schematic For Delay Time Calculation.

capacitance to the driving gate, as shown in Figure 14, where C_{eq} and R_{eq} are defined by the equations:

$$C_{eq}=C_D+C_W+C_{L1}+C_{L2}$$

$$R_{eq}=\frac{1}{\frac{1}{R_W}+\frac{1}{R_{L1}}+\frac{1}{R_{L2}}} \tag{13}$$

The WIRE cell can also be used when the fanout is equal to one. This allows the designer to insert wire capacitance for large wires when this becomes a factor in the circuit performance. The algorithm describing the operation of the WIRE cell is outlined in Figure 15. The complete VHDL code for the WIRE cell is contained in Appendix C.

```
entity WIRE is
  generic declarations for
        number of output connections
        wire resistance and capacitance
  port connections
    radiation_dose      in  dose_record
    A                   in  std_ulogic
    A_load              out signal_load
    Z                   out std_ulogic
    Z_load              in  load_array (number of output connections)
end WIRE entity declaration

architecture for WIRE
begin
   process (change to input A or Z_load)
   begin
      sum load resistances and capacitances
      update output Z
   end process
end architecture
```

Figure 15. WIRE Cell Algorithm.

4.4.2 Design of Sample Circuit. The initial sample circuit was chosen to exercise the sample gates and require a fairly long ripple path, from the first bit input to the last output through a circuit. A chain of full-adders was chosen to meet these requirements. The full-adder design chosen for the initial sample circuit is shown in Figure 16. A ripple-carry adder was chosen since it provides the required ripple path need to exercise the simulator. The particular ripple-carry design was chosen because it contains all three of the initial library logic gate elements and requires use of the *WIRE* cell. The *WIRE* cell is required to operate for fanouts of two and four. Additionally, the *WIRE* cell is required to operate across two different levels of VHDL code when several full-adders are combined into a multi-bit adder.

The ripple-carry four-bit adder was selected because a chain of four full-adders is sufficient to test the VHDL library, complete with the three logic gates and the *WIRE*

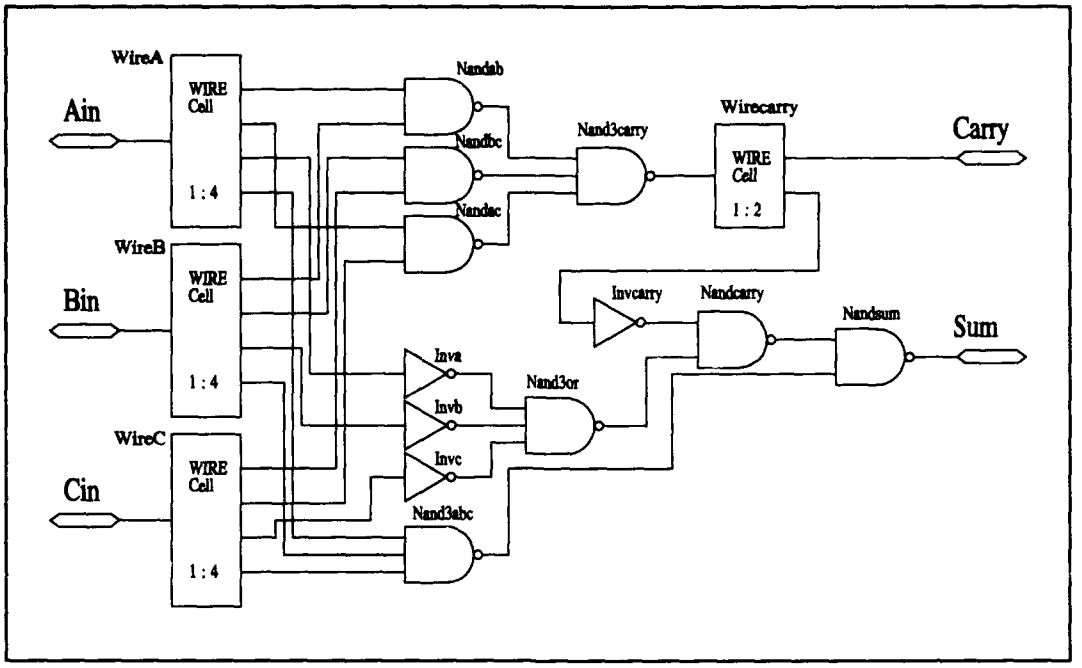

Figure 16. Ripple-Carry Full-Adder Logic Diagram.

cell. The schematic for the four-bit adder is shown in Figure 17. The *WIRE* cell is required to be used at two different levels and connected to other *WIRE* cells insuring that the full function of the cell is tested. The complete logic gate listing for the four-bit full-adder and number of gates and cells used is shown in Table 1.

Table 1. Four-Bit Full-Adder, VHDL Cell Library Gates Used

Cell Name	Function	Number of Gates
IV110	Inverter	16
NA210	2-Input NAND Gate	20
NA310	3-Input NAND Gate	12
	Total	48
WIRE	Wiring Cell	16

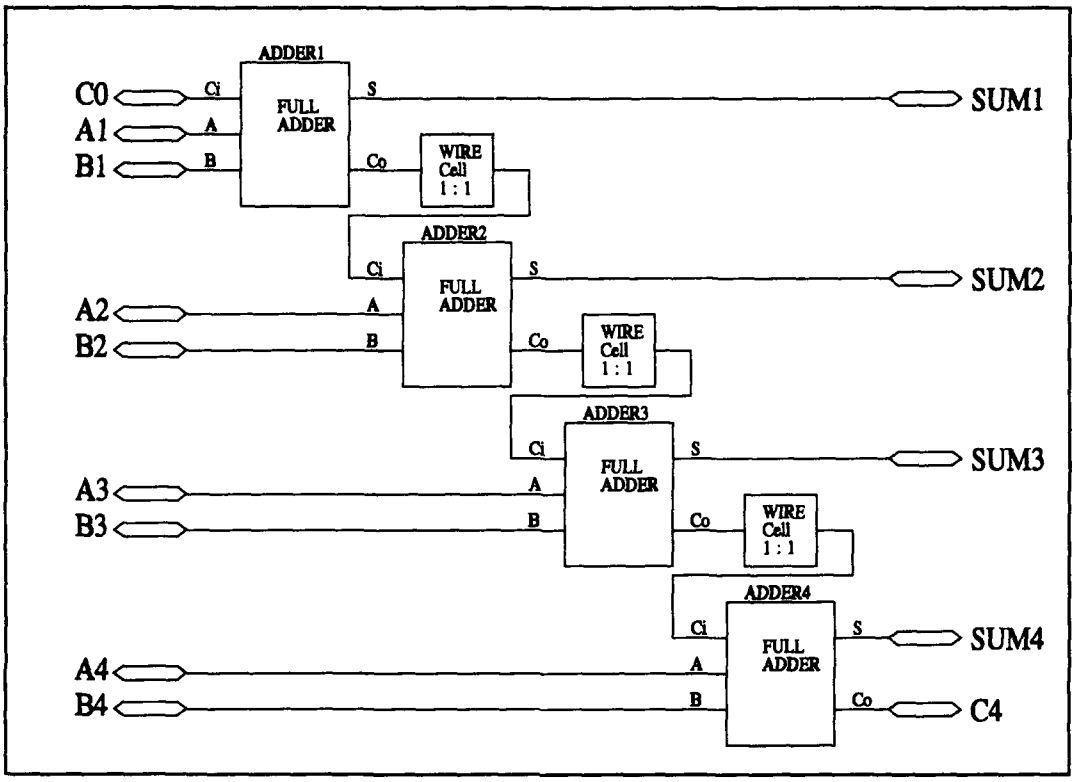

Figure 17. Four-Bit Ripple Carry Adder Block Diagram with WIRE Cell.

A prime consideration in the design of the VHDL gates and their implementation is the accurate estimation of timing delays. One way to accurately estimate timing delays is to evaluate the drive capability of a gate and the load the gate must drive to determine the time required for the gate output logic state to change. In this implementation, the load of every cell driven by a gate is summed and back-propagated to the output of the driving gate as shown in Figure 18. The VHDL code for the one-bit full adder is shown in Appendix D. The forward signal paths for the logic states and the feedback load information are observed in the logic and *WIRE* cell port declarations.

The design and operating characteristics of radiation-hardened logic gates are easily understood and the drive capability is easily measured. This allowed the initial testing to be limited to a small number of gates in developing the VHDL library. In the

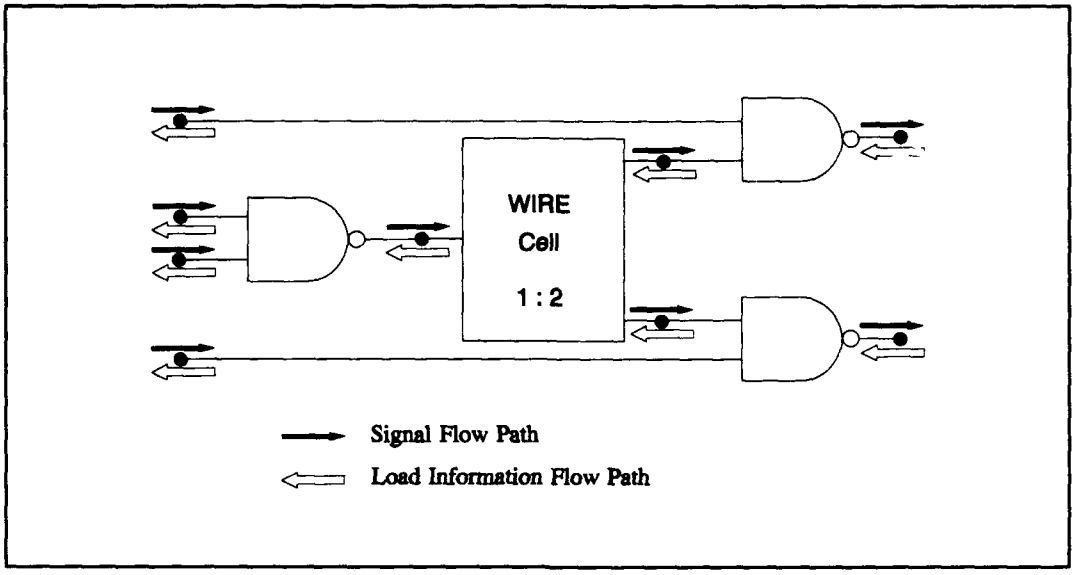

Figure 18. Logic Diagram Showing WIRE Cell and Signal Flow Paths.

initial testing, only three combinational logic gates were evaluated and tested. By keeping the library size small, effort was concentrated on the operation and timing accuracy of the models developed in the previous section. Test signal selection was also important since the four-bit full-adder has nine inputs yielding a total of 4608 single input state transitions possible, as shown by the equation:

$$T_n = 2^{n-1} \times n \times 2$$
$$T_9 = 2^8 \times 9 \times 2 = 4068 \ , \quad when \ n=9 \tag{14}$$

where T_n is the number of input state transitions. The first term, 2^{n-1}, is the number of states of the inputs not currently changing state. The second term, n, is the number of different positions the input that is changing state can occupy. The last term, 2, represents the number of transistions an input signal can accomplish, that is, high-to-low and low-to-high.

The number of possible input state transitions is defined by the product of the number of logic states for *n-1* bits, number of bits (*n*), and the low-to-high and high-to-low state transitions. Many of these transitions are redundant, from a timing point of view, due to the repetitive nature of the four-bit adder circuit. Thus, 18 different input state transition signals were chosen to determine the timing characteristics of the four-bit adder. These signals are listed in Table 2. Input signals were chosen at each adder stage to exercise each of the full-adder sum outputs. The input *B1* was selected to ripple a signal all the way through the circuit, exercising each sum and the four-bit adder fourth-bit carry out (*C4*).

4.4.3 Testing. Testing the gates consisted of using a four-bit ripple carry adder comprised of the basic logic gates listed above to evaluate timing delay estimation. First, test runs were accomplished before exposure to radiation and the results were recorded. Second, total ionizing dose was set to 1 Mrad(Si) and the simulation run was repeated. Third, several values of dose-rate were input and run through the radiation-inclusive VHDL model simulator. The results were compared with the values obtained when the circuit was simulated using SPICE. In the pre-radiation and the 1 Mrad(Si) total dose radiation environment, timing accuracy of the VHDL simulator agreed with the SPICE values to within 5 percent for all the time delay measurements collected. The dose rate radiation environment was also tested.

At low dose rates, the VHDL simulation and the SPICE simulation values do not change from the pre-radiation values since timing is unaffected at low dose rates. For higher dose rates, the VHDL simulator results agreed with the SPICE results to within 5

Table 2. Four-Bit Full-Adder, Measured Signal Transitions

NAME	Input	Transition	Out	Transition
A1rS1r	A1	rise	SUM1	rise
B1rS1f	B1	rise	SUM1	fall
B1fS1r	B1	fall	SUM1	rise
A1fS1f	A1	fall	SUM1	fall
A2rS2r	A2	rise	SUM2	rise
B1rS2f	B1	rise	SUM2	fall
B1fS2r	B1	fall	SUM2	rise
A2fS2f	A2	fall	SUM2	fall
A3rS3r	A3	rise	SUM3	rise
B1rS3f	B1	rise	SUM3	fall
B1fS3r	B1	fall	SUM3	rise
A3fS3f	A3	fall	SUM3	fall
A4rS4r	A4	rise	SUM4	rise
B1rS4f	B1	rise	SUM4	fall
B1fS4r	B1	fall	SUM4	rise
A4fS4f	A4	fall	SUM4	fall
B1rC4r	B1	rise	C4	rise
B1fC4f	B1	fall	C4	fall

percent, until the high dose rates (greater the 1×10^{10} rads(Si) per second) caused large photocurrent generation, resulting in logic gate output transistors being unable to sink the photocurrents. When the radiation dose rate is increased above 1×10^{10} rads(Si) per second, photocurrent generation increases to the point to where the CMOS logic gates are unable to pull the output voltages to the rail voltage values.

At the dose rate of 1×10^{11} rads(Si) per second, worst-case accuracy degraded to 6 percent. At 1×10^{12} rads(Si) per second, worst-case accuracy further degraded to just

under 17 percent. At the highest dose rate, 2×10^{12} rads(Si) per second, worst case accuracy degrades to over 28 percent.

4.4.4 Expansion of Capability. Calculation of the effects of radiation on a VLSI circuit are accomplished at the individual logic gate level. Recognizing that identical gates should have the same response to radiation regardless of location in the die, single models were developed for each logic gate. Furthermore, for digital circuits, given that all transistors on a die are fabricated simultaneously, it should follow that changes in drive capability and changes in load characteristics should behave in a similar manner for all transistors fabricated on a single die.

Therefore, expansion to the final VHDL logic gate library incorporated in this research is a straight forward process. Table 3 lists the gates contained in the final VHDL library. The model variables, for each of the gates in the VHDL library, were all obtained using process outlined in Section 4.1. The variables were then input into the VHDL code for each logic gate listed in Table 3.

4.5 Summary

In this chapter, the development and implementation of the models and VHDL library were presented. Each part of the model development was detailed to include the model variables: gate input capacitance, gate input resistance, drive pull-up and pull-down resistance values, and intrinsic time delay pull-up and pull-down capacitance values. These models may also be used without the radiation-inc[illegible]e parameters for accurate timing simulation of microelectronic circuits where radiation is not a concern. Each

Table 3. Final VHDL Cell Library

Cell Name	Function
AN210	2-Input AND Gate
AN310	3-Input AND Gate
BU130	Buffer, 3X Drive
DTB10	D Flip-Flop with Preset and Clear
EN210	2-Input Exclusive NOR Gate
EX210	2-Input Exclusive OR Gate
IV110	Inverter
IV211	Gated Inverter
LAH10	D Latch
NA210	2-Input NAND Gate
NA310	3-Input NAND Gate
NO210	2-Input NOR Gate
NO310	3-Input NOR Gate
OR210	2-Input OR Gate
OR310	3-Input OR Gate

model variable had to be det d for all the radiation environments: pre-radiation, post-radiation, and radiation dose rate.

After the model variables were determined for each of the logic gates, the variables were incorporated into the VHDL logic gates. Tests were conducted on three basic logic gates; an inverter, two-input NAND, and three-input NAND. Additionally, a special *WIRE* cell was generated and tested. All the gates worked as expected and the timing errors were 5 percent or less, except when the radiation dose rates exceeded 1×10^{10} rads(Si) per second.

Based on the results obtained from the initial testing of the three logic gates and the similarities of all CMOS logic gates in a single fabrication process, the modeling

process outlined in Figure 11 was implemented and translated into VHDL for the remaining logic gates listed in Table 3. The next chapter describes the test plan used to test the complete VHDL library developed for this research.

V. *Simulator Test Procedures*

5.1 Introduction

This chapter describes the simulator test plan in detail. First, the goals of the testing are presented. Second, the test circuit selections, including circuit descriptions, are presented. Third, the testing procedures are discussed, including an overview of the parameters measured and data recorded. Fourth, the simulation tools used and data collection methods are discussed. Finally, data reduction procedures are described.

5.2 Validation of Goals

The goal of this research was to produce radiation-inclusive models that would simulate microelectronic circuits providing timing accuracy within 15 percent of what SPICE provides. Additionally, the models developed in this research need to simulate at least two orders of magnitude faster than SPICE simulations.

Tests of the models, incorporated into VHDL descriptions, were conducted in order to validate timing accuracy, run time performance, and logic operation of the radiation-inclusive models developed for this research. The initial simulations, described in Chapter 4 using the four-bit adder, indicated the models operated as envisioned for the first three logic gates and the WIRE interconnect cell. The next step was to insure the models could be used to evaluate many different types of circuits, incorporating additional logic gates and state memory cells, and simulate correctly providing accurate timing delay information.

Scaling of circuit complexity needed to be validated for the simulator. While circuit simulation speed in standard VHDL scales well with increasing circuit complexity, this capability needed to be confirmed for the radiation-inclusive models as implemented in VHDL. Thus, tests were developed to validate the timing accuracy, simulator run time, and functional operation for logic circuits of varying complexity.

The performance of the radiation-inclusive VHDL models was compared to two other simulators, SPICE and standard VHDL models. SPICE provided the performance baseline since the data obtained from SPICE is accurate and traceable to physically constructed microelectronic circuits at Texas Instruments [23]. The radiation-inclusive model VHDL was the test simulator and all of the measurements recorded were compared against the measurement values obtained using SPICE. Finally, standard model VHDL simulations were run to provide a comparison of the capability of the standard model VHDL against the results obtained using the radiation-inclusive VHDL model, both for timing accuracy and simulation run time. Even though functional operation should be the same for both the standard and radiation-inclusive model VHDL simulations, correct functional operation of both models was verified during simulation.

Preference was given to selecting microelectronic circuits that incorporate as many of the logic gates listed in Section 4.3.4 as possible. Data was collected for each circuit tested, confirming the functional operation, logic propagation delay timing information, and simulation run time for the various logic gates as simulated by each of the three simulators.

5.3 *Test Circuit Description*

Microelectronic circuits were selected to implement the testing goals. The specific selection of the microelectronic circuits required balancing the goals of obtaining valid test data indicating the timing accuracy against the necessary simulation run time. Every logic gate and memory circuit was tested for functional as well as timing accuracy, at the gate level, in VHDL after the models were implemented. Testing of functional operation was conducted in order to insure the modeling process, as outlined in the previous chapter, had been run correctly.

In addition to the tests conducted for each logic gate, a total of four circuits were selected and simulated. The four-bit adder, described in Chapter 4, represented the least complex circuit and has the lowest total transistor count of the four circuits. The other three circuits tested included a binary coded decimal (BCD) to seven-segment converter, microwave oven controller, and a 16-bit microprocessor control unit.

5.3.1 BCD to Seven-Segment Converter. The second logic circuit chosen was a BCD to seven-segment converter as shown in Figure 19. This implementation of the converter was not intended to be the fastest or the smallest implementation of the circuit. Instead, this circuit was designed to use several of the logic gates implemented in the radiation-inclusive model VHDL library which were not used in the four-bit adder circuit, while providing reasonable size and timing performance. Table 4 contains a complete listing of gates used in the converter circuit.

The converter gate count is slightly lower than the four-bit adder gate count. The total gate count for the BCD to seven-segment converter is 37 while the adder logic gate

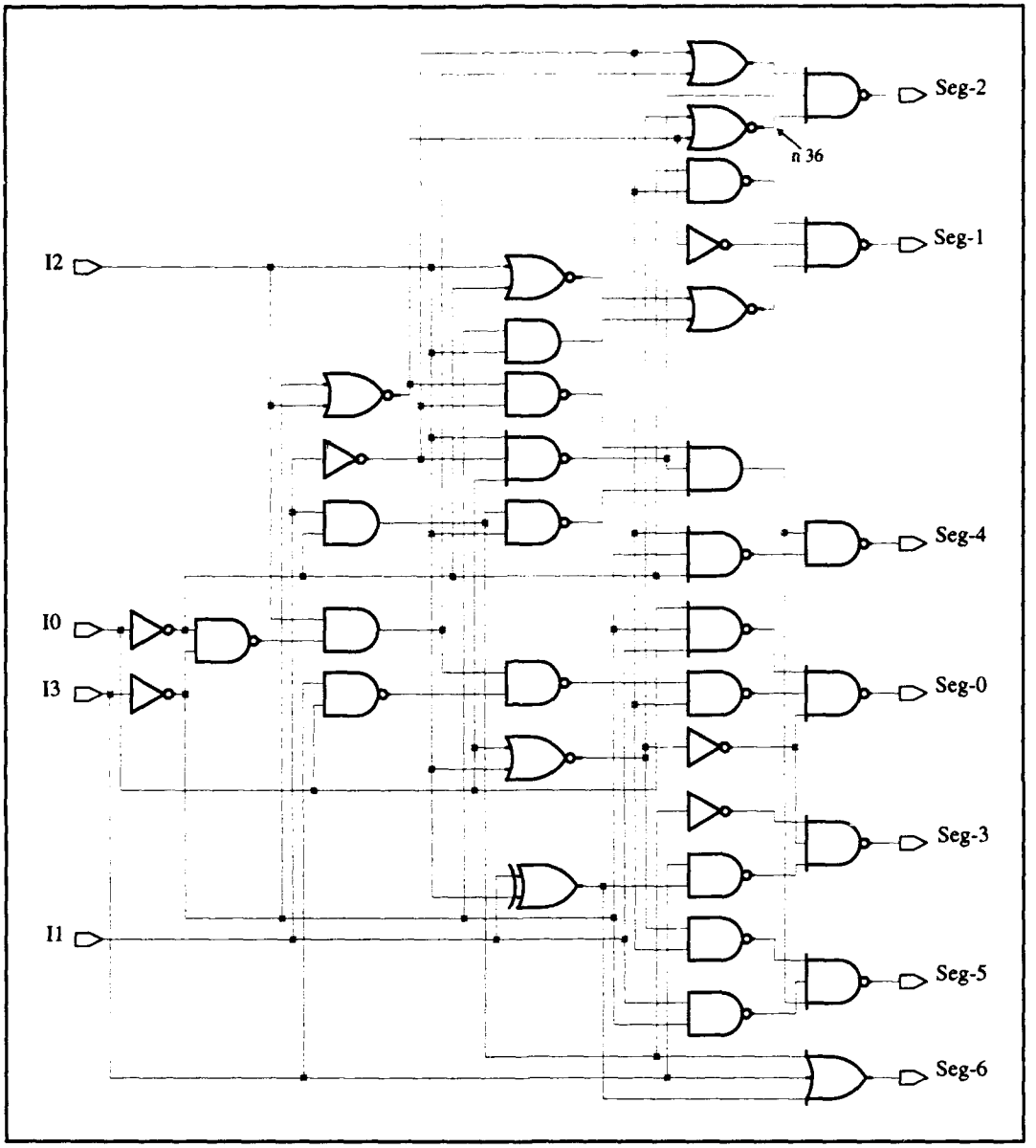

Figure 19. Binary Coded Decimal to Seven-Segment Converter Schematic.

count is 48. However, there is no repetition of sub-circuits in the BCD to seven-segment converter, while the adder is constructed of four repeated full-adder blocks. Additionally, the BCD to seven-segment converter has a higher total transistor count; 222 transistors versus 184 transistors in the four-bit full-adder circuit. The range of fanout loads in the BCD to seven-segment converter is one to eight with the average fanout load calculated at 1.87 (51.8 fF). The average fanout load value was obtained by counting all the gates

Table 4. BCD to Seven-Segment Converter, VHDL Cell Library Gates Used

Gate Name	Function	Number of Gates
AN210	2-Input AND Gate	3
AN310	3-Input AND Gate	1
EX210	2-Input Exclusive OR Gate	1
IV110	Inverter	6
NA210	2-Input NAND Gate	11
NA310	3-Input NAND Gate	8
NO210	2-Input NOR Gate	5
OR210	2-Input OR Gate	1
OR310	3-Input OR Gate	1
	Total	37
WIRE	Wiring Cell	15

and the load inputs, with the circuit final outputs given a fanout load of one. The capacitance value takes into account the load input capacitance values for all the logic gates, including the XOR gate which has a loading of 54 fF at each input.

Four inputs were used for the binary coded decimal signal lines. With four inputs, a completely combinational logic circuit containing 64 different possible logic transitions could be observed and measured, as calculated by Equation (14), Section 4.4.2. It was not necessary to measure the time delay of every input-to-output logic value change; observation of the circuit in Figure 19 permitted the selection of a representative sample of signals that were evaluated and measured. Signal transitions were selected by choosing several signal propagation paths which vary in number of gates, fanout of the gates, and logic function of the gates through which a signal propagates.

As a result of careful examination, 24 input-to-output transition signals were selected to determine the ability of the radiation-inclusive model VHDL simulator to provide accurate timing information. The input-to-output transition signals selected are shown in Table 5. The selected signals include signals that propagate through only one gate (*e.g.*, Input 3 to Output 6) and signals that propagate through as many as five logic gates (*e.g.*, Input 0 to Output 6).

5.3.2 State Machine Control Unit. The first two circuits contained exclusively combinational logic gates. The third circuit, a state machine control unit in the form of microwave oven control unit (Figure 20), was selected because it contained two types of state memory cells the, D flip-flop (DTB10) and D latch (LAH10). Additionally, this circuit incorporated the tri-state output inverter (IV211) to allow disconnection of the output drive signals. The circuit designed is a sample state machine to control the operation of a microwave oven. It was designed by writing a behavioral VHDL description and then synthesizing a structural circuit using the Synopsys Design Analyzer, version 3.0b [4].

The circuit, as designed, contains 446 transistors organized into 67 gates, as listed in Table 6. The range of fanout loads in the oven controller is from one to nine, with an average fanout load calculated to be 1.88 (51 fF).

The microwave oven controller circuit contains six inputs representing the input programming functions of the oven. With six inputs, a combinational logic circuit would have 384 possible single bit logic transitions that could occur; however, the oven controller contains several conditional control provisions, such as the *reset* which

Table 5. BCD to Seven-Segment Converter, Measured Signal Transitions

NAME	Input	Transition	Output	Transition
I0rO2r	I0	rise	Seg-2	rise
I0rO3r	I0	rise	Seg-3	rise
I0rO4r	I0	rise	Seg-4	rise
I0rO5r	I0	rise	Seg-5	rise
I0fO2f	I0	fall	Seg-2	fall
I0fO3f	I0	fall	Seg-3	fall
I0fO4f	I0	fall	Seg-4	fall
I0fO5f	I0	fall	Seg-5	fall
I1rO0f	I1	rise	Seg-0	fall
I1rO2f	I1	rise	Seg-2	fall
I1rO3f	I1	rise	Seg-3	fall
I1rO5f	I1	rise	Seg-5	fall
I1rO1f	I1	rise	Seg-1	fall
I1rO4f	I1	rise	Seg-4	fall
I1rO6r	I1	rise	Seg-6	rise
I1fO1r	I1	fall	Seg-1	rise
I1fO4r	I1	fall	Seg-4	rise
I1fO6f	I1	fall	Seg-6	fall
I2rO2f	I2	rise	Seg-2	fall
I2rO3f	I2	rise	Seg-3	fall
I2fO2r	I2	fall	Seg-2	rise
I2fO3r	I2	fall	Seg-3	rise
I3rO6r	I3	rise	Seg-6	rise
I3fO6f	I3	fall	Seg-6	fall

overrides all other inputs, and limits the output state transitions possible based on the input signal choices. Signal transitions measured for the oven were primarily a function of the output transitions triggered by the system clock (*clk*) since the clock determines all

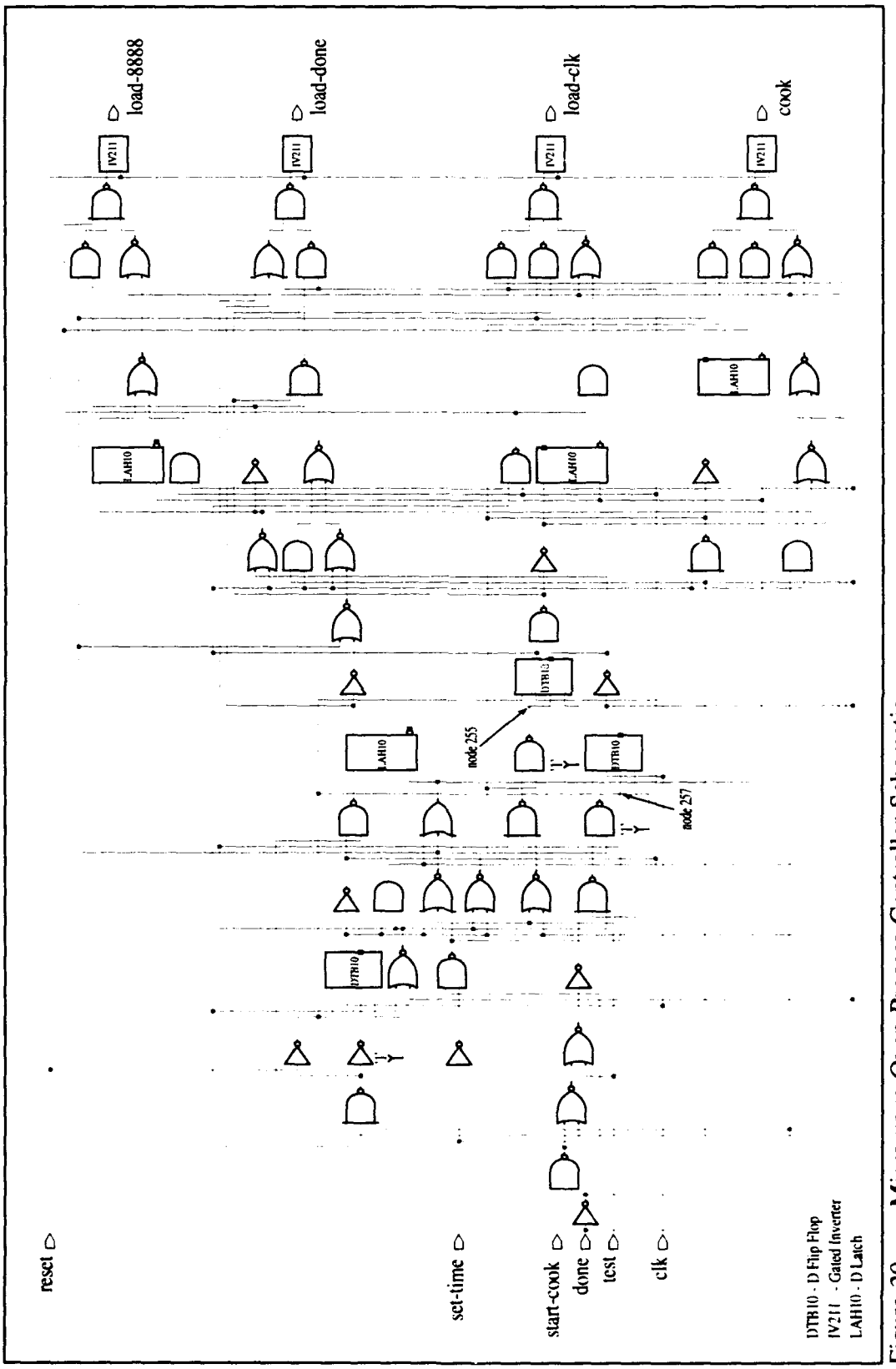

Figure 20. Microwave Oven Process Controller Schematic.

Table 6. Microwave Oven Controller, VHDL Cell Library Gates Used

Gate Name	Function	Number of Gates
AN210	2-Input AND Gate	5
DTB10	D Flip-Flop	3
IV110	Inverter	11
IV211	Gated Inverter	4
LAH10	D Latch	4
NA210	2-Input NAND Gate	14
NA310	3-Input NAND Gate	8
NO210	2-Input NOR Gate	14
NO310	3-Input NOR Gate	2
OR310	3-Input OR Gate	2
	Total	67
WIRE	Wiring Cell	26

output logic transition times. This is the result of the output values being set with the flip-flops and latches. Furthermore, the *reset* input overrides all other inputs and disables all outputs. The signal transitions that were selected for observation were primarily chosen to observe the propagation delay times from the flip-flops and latches to the output. The actual signal transitions observed and measured are shown in Table 7. All input signals listed are primary circuit inputs. The first eight output transitions measured are circuit outputs, and the last four output transitions measured are internal nodes indicated in Figure 20.

5.3.3 16-Bit Microprocessor Control Unit. The final circuit was selected to provide a more complex circuit containing a much larger number of logic gates than the previous three circuits. The large number of logic gates, in different combinations,

Table 7. Microwave Oven Controller, Measured Signal Transitions

NAME	Input	Transition	Output	Transition
clk88r	clock	rise	load-8888	rise
clk88f	clock	rise	load-8888	fall
clkckr	clock	rise	load-clk	rise
clkckf	clock	rise	load-clk	fall
clkcoor	clock	rise	cook	rise
dnrcoof	done	rise	cook	fall
dnrlddr	done	rise	load-done	rise
clklddf	clock	rise	load-done	fall
cook255r	cook	rise	node 255	rise
done255f	done	rise	node 255	fall
cook257r	done	rise	node 257	rise
done257f	done	rise	node 257	fall

allowed testing to confirm the flexibility and accuracy of the radiation-inclusive VHDL models. Simulation run time versus logic gate count confirmed the efficiency in scaling of the radiation-inclusive VHDL model simulator runs versus SPICE.

The 16-bit microprocessor circuit chosen was designed using a state timing table developed as part of a class project [24]. The microprocessor circuit was designed for and controlled the operation of a 16-bit single-chip microprocessor. The original behavioral description was implemented using a state timing table. For this research, the state timing table was synthesized into structural VHDL using the Synopsys Design Analyzer, version 3.0b [4]. The logic gates used to implement the 16-bit microprocessor are listed in Table 8. The structural VHDL was simulated for function and the results agreed with the data presented in the class project report.

Table 8. Microprocessor Control Unit, VHDL Cell Library Gates Used

Cell Name	Function	Number of Gates
AN210	2-Input AND Gate	50
AN310	3-Input AND Gate	4
DTB10	D Flip-Flop	7
IV110	Inverter	77
NA210	2-Input NAND Gate	105
NA310	3-Input NAND Gate	48
NO210	2-Input NOR Gate	103
NO310	3-Input NOR Gate	51
OR210	2-Input OR Gate	67
OR310	3-Input OR Gate	24
	Total	536
WIRE	Wiring Cell	61

As shown in Table 8, the 16-bit microprocessor control unit, as implemented, is constructed of 536 logic gates and incorporates 61 *WIRE* cells. The 536 logic gates use 2864 transistors, representing a circuit that contains roughly one order of magnitude more circuit elements than the previous circuits tested for this research. The fanout loads in the 16-bit microprocessor control unit range from one to ten equivalent input loads, with the average fanout load calculated to be 1.96 (53 fF).

Signals were selected for monitoring the various state propagation delay times for various outputs of the control unit. The large circuit size limited the input stimulus that could be tested in a reasonable amount of time. For the purpose of this research, it was reasonable to select several output signals that are timed off the clock signal driving the D flip-flops. SPICE simulation of the microprocessor power-up reset cycle, representing

the first 400 ns of operation, required several hours of simulation time for a single pass running on a Sun Microsystems SPARCstation II computer system.

The signals monitored and measured are output signals that change logic state during the first 400 ns of the control unit power-up reset cycle. These signals are listed in Table 9. These signal logic values are controlled and the output transitions driven by unique combinations of the six D flip-flops which are cycled by the system clock. Thus, the output signal transitions are driven by various logic signal paths through the microprocessor control unit circuitry.

5.4 Simulation Procedures

Every circuit selected was simulated in the same fashion to produce uniformity and comparability of the resulting data. First, an input data set was selected to execute the operation of the circuits. Simulation of timing accuracy was accomplished by first selecting an input-to-output signal data set for each microelectronic circuit. The input signals were then programmed as stimuli for each simulator run. Second, each circuit was simulated in SPICE and in the radiation-inclusive model VHDL for several different radiation environments. Third, all the circuits were simulated using the base VHDL with the radiation-inclusive model VHDL in the pre-radiation environment. Output signal time delay information was measured during or after each of the three simulator run times.

The base VHDL, used as a comparisons for this research, used the same functional descriptions as the radiation-inclusive model VHDL. The only difference between the two VHDL simulations was the method of calculating the time delay information for each gate. While the radiation-inclusive model VHDL used the load values in calculating the

Table 9. 16-Bit Microprocessor Control Unit, Measured Signal Transitions

NAME	Input	Transition	Output	Transition
60iplf	clock	60ns rise	ipl	fall
60ipmuxf	clock	60ns rise	ipmux	fall
60DTRf	clock	60ns rise	DTR	fall
60ALU2r	clock	60ns rise	ALU2	rise
60BIPr	clock	60ns rise	BIP	rise
60ALEr	clock	60ns rise	ALE	rise
100ALU2f	clock	100ns rise	ALU2	fall
100BIPf	clock	100ns rise	BIP	fall
100ALEf	clock	100ns rise	ALE	fall
100RDBRf	clock	100ns rise	RDBR	fall
180irlf	clock	180ns rise	irl	fall
180DTRr	clock	180ns rise	DTR	rise
180ALU3r	clock	180ns rise	ALU3	rise
220iplr	clock	220ns rise	ipl	rise
220ALU3f	clock	220ns rise	ALU3	fall
260iplf	clock	260ns rise	ipl	fall
260ipmuxf	clock	260ns rise	ipmux	fall
260DTRf	clock	260ns rise	DTR	fall
260ALU3r	clock	260ns rise	ALU3	rise
260ALU1r	clock	260ns rise	ALU1	rise
260ALU0r	clock	260ns rise	ALU0	rise
260BIPr	clock	260ns rise	BIP	rise
340ir2lr	clock	340ns rise	ir2l	rise
380ir2lf	clock	380ns rise	ir2l	fall

time delay through each gate, the base VHDL used a constant load value for the delay time calculation. The base VHDL gate descriptions were constructed with conventional time delay values for the logic transitions. To insure that reasonable values for the time

delays were used, each gate was modeled with a fanout load of 54 fF. A capacitance of 54 fF represents an equivalent fanout load of two inverter inputs connected to a gate output. This value was chosen since it is within seven percent of the average fanout reported for each of the circuits tested. By choosing this load value and modeling actual gates, an accurate assessment of the base VHDL timing performance was possible.

5.5 Data Collection Procedures

Simulation of the microelectronic circuits is of little use unless valid data is collected. Valid data collection was necessary for proper evaluation of the simulator performance. The same data needed to be collected for each of the three simulators; SPICE, radiation-inclusive model VHDL, and base VHDL. Tables 5, 7, and 9 in Section 5.3 list the logic value transition signals collected. Additionally, the run time for each simulator was recorded.

All SPICE signal timing data was collected directly using the measure function available in HSPICE, version H92b [11]. Simulator run time data was collected from the simulation run time log file. Data was collected from both VHDL simulations, running under the Synopsys VHDL Debugger, version 3.0b, using the Waveform Viewer program to manually record timing data into ASCII data files [25]. VHDL run time information was collected using a stopwatch since the simulations were run within a Synopsys graphical interface program, preventing easy access to the computer system run time collection utilities.

The choice of running the SPICE simulations using HSPICE and VHDL simulations using the Synopsys VHDL Debugger was intentional. HSPICE compiles the

SPICE deck and runs the simulations using compiled computer code. The Synopsys VHDL Debugger, using the Waveform Viewer program, runs VHDL descriptions in an interpreted mode. The advantage of this choice was SPICE, the CPU intensive simulator, was running efficiently using compiled computer code while the "fast" event driven simulator, VHDL, was running in a slower interpreted mode. Thus, the reported run time speed-up values are conservative and even better simulation speed-up ratios should be possible.

All VHDL based simulations were run in the interpreted mode. The only differences in the run times between the base VHDL and the radiation-inclusive VHDL models are the additional time required to determine the radiation-inclusive delay time parameters. These parameters included the radiation-inclusive drive and load, resistance and capacitance, and the delay time calculations executed during simulation run time. The radiation-inclusive VHDL simulations always run slower than the base VHDL simulations due to the additional time delay data calculated during simulation run time.

5.6 Data Reduction Procedures

Raw test data is difficult to analyze and use without modification. The data from each test was collected and combined to present a clear picture of the results. SPICE data provides the baseline for the timing accuracy testing and, as a result, was used as the reference for all error calculations.

To insure a minimum of data entry errors, automated data measurement recording was employed for all SPICE measurements. All VHDL timing measurements were manually recorded to ASCII data files and then checked to insure accurate recording of

the data. All error calculations were accomplished using FORTRAN programs to insure accuracy and reduce the possibility of errors created by manual data entry and calculation.

Three data summary listings were produced for each of the four circuits tested in this research, as shown in Appendices E through H. Within each of these four appendices, the first tabular listing contains the radiation-inclusive model VHDL and SPICE values for the pre-radiation and 1 Mrad(Si) total dose results. The second tabular listing contains the values for the dose rate results. The third tabular listing contains the results for the standard VHDL timing accuracy results.

Data presented on the timing accuracy of the radiation-inclusive model VHDL and the standard model VHDL were compared directly with the results obtained using SPICE. The timing errors were recorded in percentages and the SPICE value is used as the reference value for the calculations.

5.7 Summary

This chapter described the test circuits selected to validate the simulator models in the radiation-inclusive model VHDL. The simulator test plan was described, indicating the simulators used, listing the signal transitions measured, and specifying the radiation environment parameters selected. The goals of the testing were presented, estimating the simulation speed-up and timing accuracy performance expected. The test circuit selections, including circuit descriptions, were presented. The testing procedures were outlined, including an overview of the parameters measured and data recorded. The simulation tools used and data collection methods were listed and the data reduction

procedures were described. The next chapter details the test results obtained in this research.

VI. Results and Analysis

6.1 Introduction

This chapter details the results of the simulation runs using base-VHDL, radiation-inclusive model VHDL, and SPICE for the four circuits tested. For all circuits tested, timing error summaries are presented for the pre-radiation, 1 Mrad(Si) total dose, and various dose rates ranging up to 2×10^{12} rads(Si) per second. First, the results are discussed for the combinational logic circuits: the four-bit full-adder and the BCD to seven-segment converter circuit. Next, the measurement results for the circuits containing the flip-flops, the microwave oven controller and 16-bit microprocessor control unit, are described. The chapter concludes with a discussion of the time delay calculation error sources for the radiation-inclusive model VHDL simulator.

6.2 Simulation Data Presentation

The overall results of simulating each circuit are presented, showing the run time and timing errors observed for base-VHDL, radiation-inclusive model VHDL, and SPICE simulations for each of the four circuits. The percent error for each signal transistion is:

$$e(i)=\left(\frac{t(i)_{VHDL}-t(i)_{SPICE}}{t(i)_{SPICE}}\right)\times 100\% \qquad (15)$$

where:

$t(i)_{SPICE}$ - SPICE Time Delay of the i^{th} Signal Transition

$t(i)_{VHDL}$ - VHDL Time Delay of the i^{th} Signal Transition

The mean of the absolute value of the timing error for each logic signal state transition time delay was calculated using the equation:

$$\mu = \frac{1}{n} \times \sum_{i=1}^{n} |e(i)| \tag{16}$$

where:

μ	-	Mean Percentage of the VHDL Absolute Value of Timing Estimate Error
n	-	Number of Signal Transitions Measured in Each Circuit

The standard deviation of the timing error absolute values was also calculated for each circuit using the equation:

$$\sigma = \sqrt{\frac{1}{(n-1)} \sum_{i=1}^{n} [|e(i)| - \mu]^2} \tag{17}$$

where σ is the standard deviation. After the calculations were accomplished for a given circuit, the results were plotted showing the relative timing accuracy performance versus run time for each simulator. An ideal simulator would have both a zero percent timing error and zero run time.

Results are shown for each of the four circuits simulated. The timing error versus run time is shown for both the pre-radiation and 1 Mrad total dose radiation-inclusive VHDL model. The radiation-inclusive VHDL model timing accuracy results are presented for several different radiation dose rates ranging from 1×10^9 to 2×10^{12} rads(Si) per second.

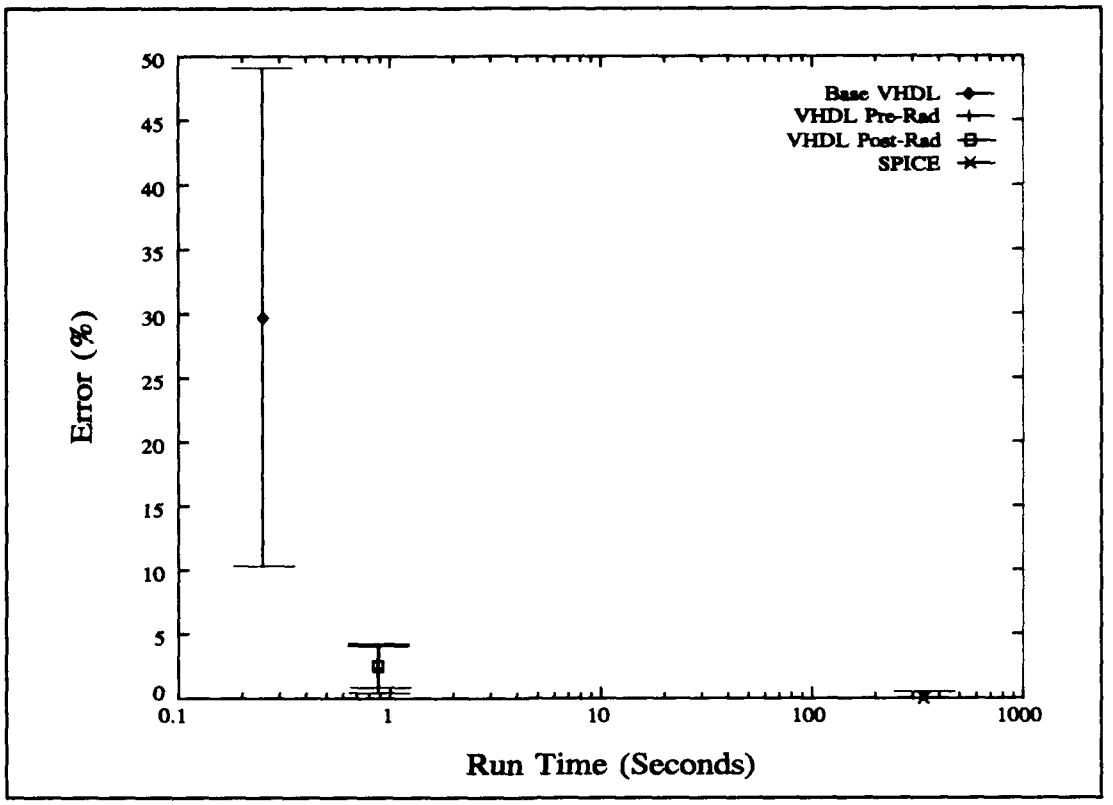

Figure 21. Four-Bit Full-Adder, Simulation Timing Errors.

6.2.1 Four-Bit Full-Adder. The four-bit adder was designed and tested during the initial model and VHDL library development, as described in Chapter 4. The 18 different time delay transition signals are listed in Chapter 4, Table 2. All the VHDL timing measurements were referenced against the measurements obtained by using SPICE, the baseline. Timing error and standard deviation were calculated using Equations (16) and (17).

The mean and standard deviation for the 18 different time delay signals of the four-bit full-adder for each case are shown in Figure 21. The detailed measurement values and error calculation results are found in Appendix E. Each simulator run time is represented using a logarithmic scale on the x-axis, while the timing accuracy data is shown using a linear scale on the y-axis. All simulation run times shown for the base

VHDL, radiation-inclusive model VHDL, and SPICE are the average run time for a single simulation. Both the pre-radiation and 1 Mrad(Si) total dose results are shown for the radiation-inclusive VHDL model.

The SPICE results, located in the lower right corner, show the SPICE run time and indicate the SPICE run-to-run differences of the propagation delays observed during testing. The SPICE values varied by about 0.5 percent on different simulation runs when the circuit node locations in the simulation matrix were changed.

The two overlaying data bars, at 0.9 seconds, are both the pre- and post-radiation inclusive model VHDL simulation. Mean error values are 2.3 percent and 2.5 percent respectively. The error bars show the standard deviation of the absolute value of the timing error. The standard deviation values for pre- and post-radiation inclusive model VHDL simulation runs are 1.8 percent and 1.7 percent respectively. Plotted at two seconds run time is the base VHDL simulator run timing error data. The absolute value of the timing error was 29.7 percent and the standard deviation was 19.4 percent.

Timing accuracy results of the VHDL simulations are presented in Figure 22 for the four-bit full-adder when exposed to a radiation dose rate environment ranging from 1×10^{9} to 2×10^{12} rads(Si) per second. Timing accuracy remains close to that of the pre- and post-radiation dose environments for dose rates up to 1×10^{10} rads(Si) per second. As dose rates increase above 1×10^{10} rads(Si) per second, timing accuracy deteriorates until by 2×10^{12} rads(Si) per second the mean timing error has increased to nearly 20 percent. The primary source of timing error in the radiation-inclusive model VHDL is the inability of the various logic gates to pull the output voltages all the way to the rail voltages. This source of timing error will be discussed in Section 6.3.5.

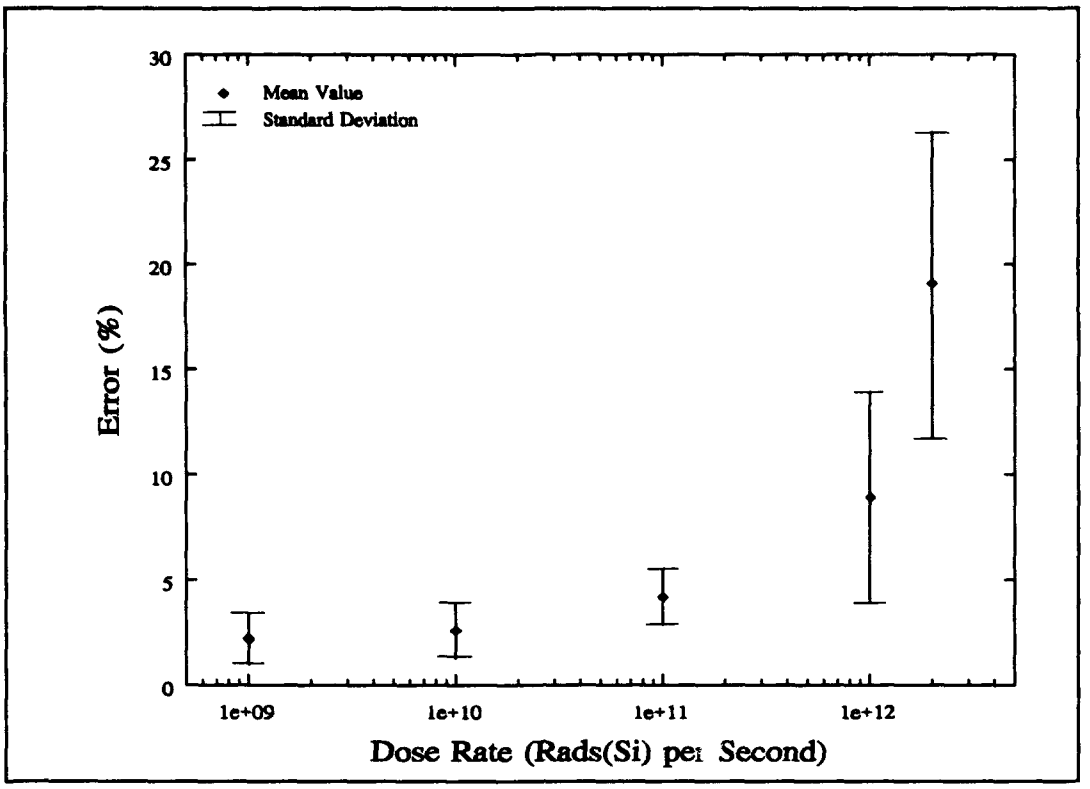

Figure 22. Four-Bit Full-Adder Dose Rate Timing Accuracy.

Simulation of the four-bit adder using the radiation inclusive model VHDL demonstrated a dramatic improvement in timing accuracy calculation over the base-VHDL results, but with a run time penalty. The radiation-inclusive model VHDL ran two to three times slower than the base-VHDL. Because the four-bit adder contained only three different logic gates, additional testing was required with more complex circuits.

6.2.2 BCD to Seven-Segment Converter. The second combinational logic circuit tested was the BCD to seven-segment converter circuit. This circuit is a more diverse and complex circuit than the four-bit full-adder. Testing the radiation-inclusive model VHDL simulator required additional data collection to accurately characterize timing accuracy. A total of 24 different time delay signal transitions were recorded.

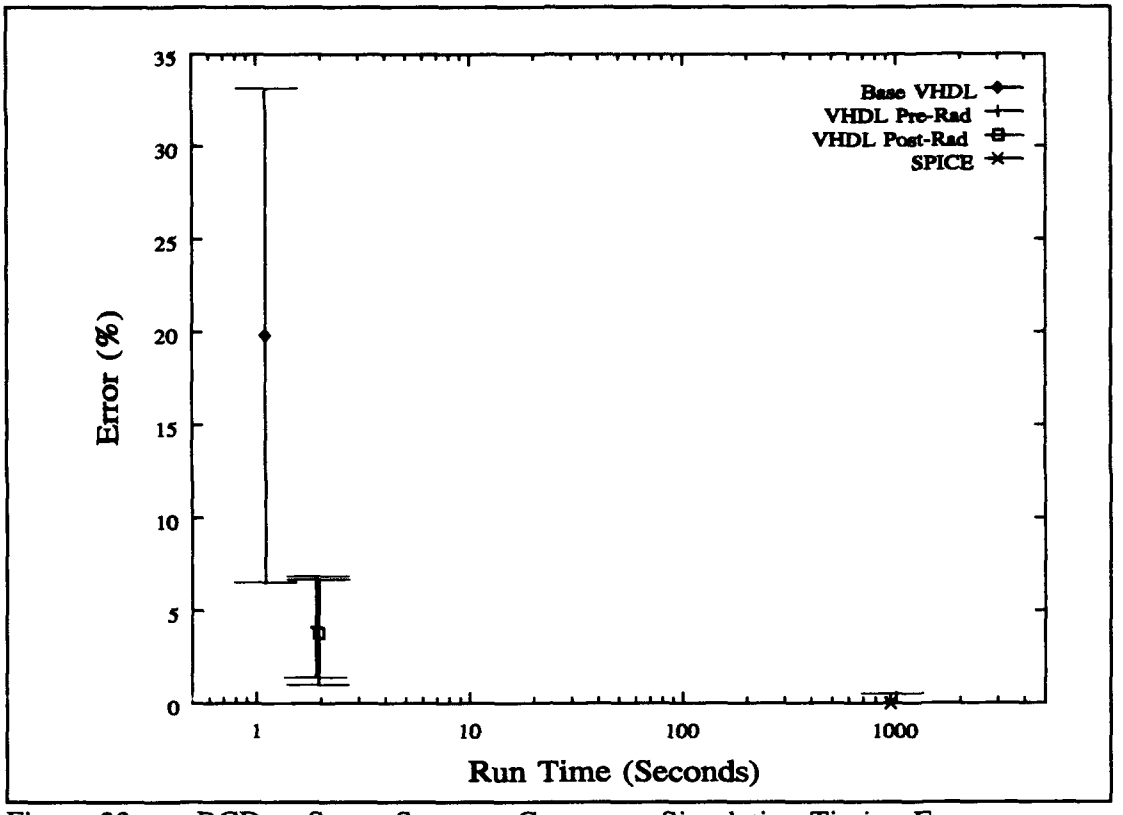

Figure 23. BCD to Seven-Segment Converter, Simulation Timing Errors.

The detailed measurement values and error calculation results are found in Appendix F. The summary results of the time delay error measurements are shown in Figure 23. The simulation run times for each simulator were considerably longer than the run times observed for the adder circuit. Each SPICE simulation took an average of 940 seconds to run, radiation-inclusive VHDL simulation took 2.5 seconds to run, and base-VHDL simulation ran in 1.1 seconds. The mean of the absolute time delay error for the pre-radiation VHDL simulation was 4.1 percent while the error for the post-radiation VHDL simulation was 3.8 percent. The standard deviation for the pre- and post-radiation VHDL data was 2.7 and 2.8 percent respectively.

The base-VHDL error results are also shown in Figure 23, at 1.1 seconds run time. The mean of the absolute error for the base-VHDL simulation run is 19.8 percent with

a standard deviation of 13.3 percent. As with the adder circuit, the SPICE simulation timing results varied less than one percent run-to-run.

Timing accuracy results are presented in Figure 24 for simulation of the BCD to seven-segment converter when exposed to a radiation dose rate environment ranging from 1×10^{9} to 2×10^{12} rads(Si) per second. Timing accuracy remains close to that of the pre- and post-radiation dose environments for dose rates up to 1×10^{11} rads(Si) per second. As dose rates increase above 1×10^{11} rads(Si) per second, timing accuracy deteriorates until by 2×10^{12} rads(Si) per second the mean timing error had increased to over 25 percent. Timing accuracy of the radiation-inclusive model VHDL compared favorably with the SPICE results. The mean error remained below five percent for all radiation environments until the dose rate exceeded 1×10^{11} rads(Si) per second.

The four-bit full-adder and BCD to seven-segment converter circuits were composed entirely of combinational logic gates. The next circuit tested, the microwave oven controller, incorporated state devices, flip-flops and latches, in the design.

6.2.3 Microwave Oven Controller. The microwave oven controller circuit added two different state machine devices and the tri-state inverter to the testing, the first complex circuit tested with state machine logic devices. The radiation-inclusive model VHDL simulator timing error and standard deviation were calculated using Equations (16) and (17). A total of 12 different time delay signal transitions were recorded.

The detailed measurement values and error calculation results are found in Appendix G. The absolute value of the mean and standard deviation of the time delay error measurements are shown in Figure 25. The simulation run times for each simulator

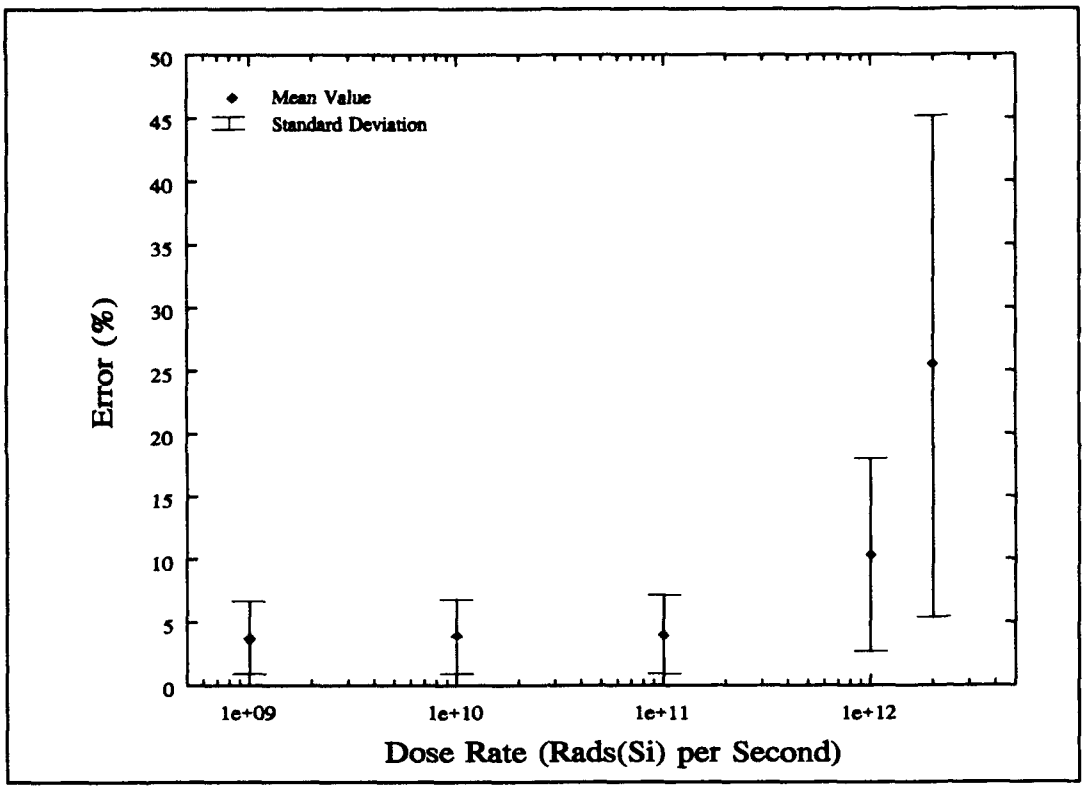

Figure 24. BCD to Seven-Segment Converter Dose Rate Timing Accuracy.

were considerably longer than the run times observed for either of the previous circuits because of the circuit complexity. Each SPICE simulation pass took 10,800 seconds to run, radiation-inclusive VHDL simulation took 5 seconds to run, and each base-VHDL simulation ran in 1.8 seconds. The mean of the absolute time delay error for the pre-radiation VHDL simulation was 3.0 percent while the error for the post-radiation VHDL simulation was 3.2 percent. The standard deviation for the pre- and post-radiation VHDL data was 3.0 and 2.9 percent respectively.

The base-VHDL error results are shown in Figure 25, at 1.8 seconds run time. The mean of the absolute error for the base-VHDL simulation run was 13.5 percent with a standard deviation of 7.2 percent. As with the previous two circuits, the SPICE simulation run-to-run timing results varied less than one percent.

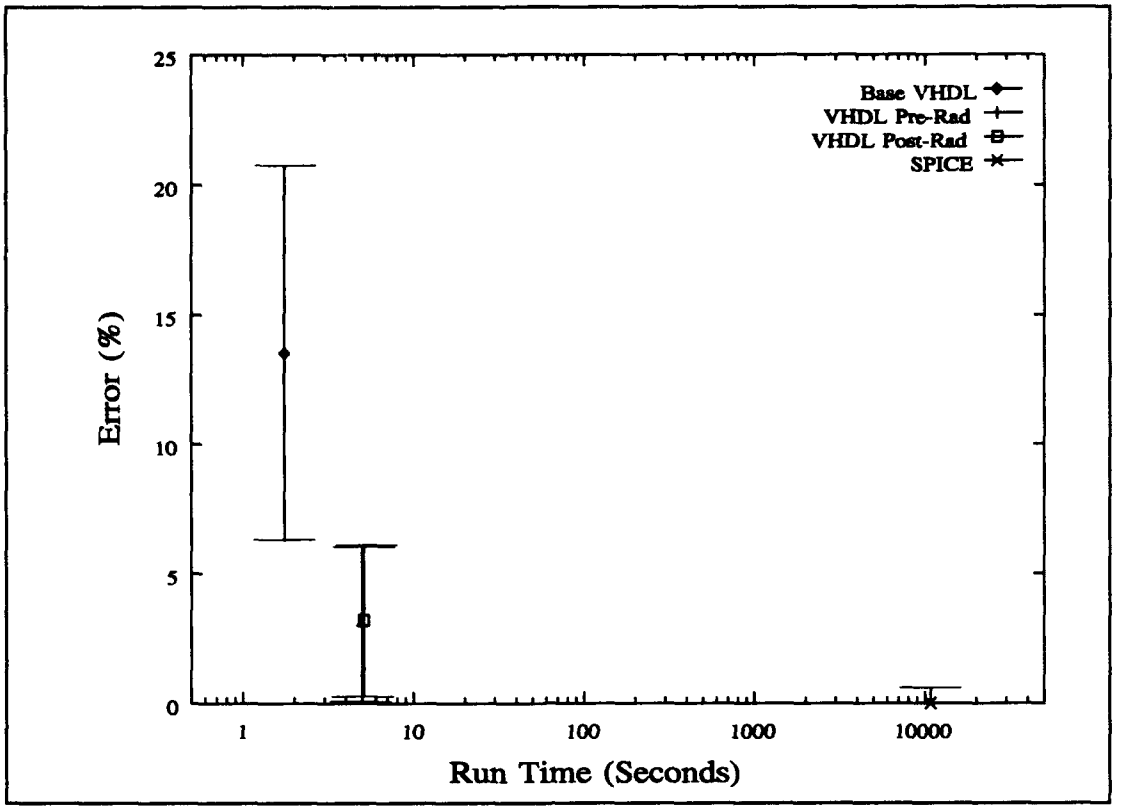

Figure 25. Microwave Oven Controller, Simulation Timing Errors.

Timing accuracy results are presented in Figure 26 for simulation of the microwave oven controller when exposed to a radiation dose rate environment ranging from 1×10^{9} to 1×10^{12} rads(Si) per second. Timing accuracy remains close to that of the pre- and post-radiation dose environments for dose rates up to 1×10^{11} rads(Si) per second. For the dose rate of 1×10^{12} rads(Si) per second, the mean timing error increased to almost 10 percent. At dose rates of 2×10^{12} rads(Si) per second and greater the flip-flops no longer changed state and no meaningful timing data was collected.

Accuracy of the radiation-inclusive model VHDL compared favorably with the results obtained from SPICE, with the mean error remaining under 4 percent for all the radiation environments tested except for dose rates over 1×10^{11} rads(Si) per second. Although more complex than the BCD to seven-segment converter, the radiation-inclusive

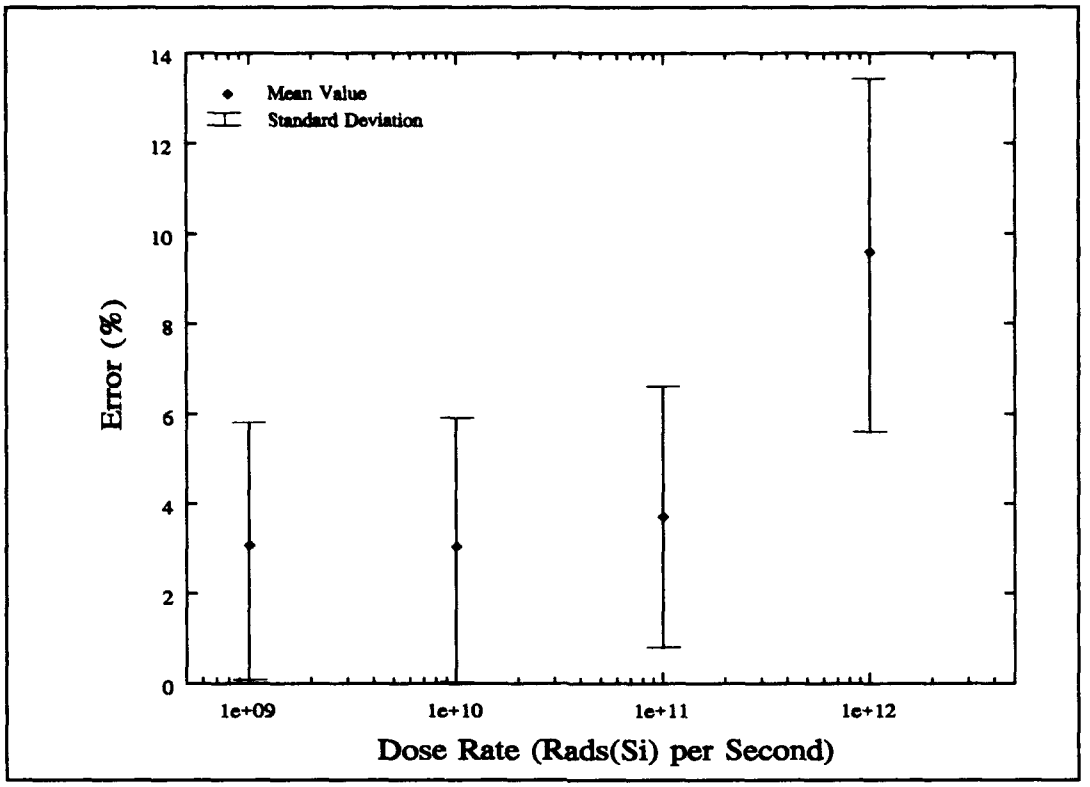

Figure 26. Microwave Oven Controller Dose Rate Timing Accuracy.

model VHDL simulations of the microwave oven controller were more accurate, primarily due to the greater use of two-input logic gates and inverters.

6.2.4 16-Bit Microprocessor Control Unit. The final and most complex circuit tested in this research effort was a 16-bit microprocessor control unit. The radiation-inclusive model VHDL simulator timing error and standard deviation were calculated using the same method as the previous three circuits. A total of 24 different time delay signal transitions were recorded.

The detailed measurement values and error calculation results are found in Appendix H. The absolute value of the mean and standard deviation of the time delay error measurements are shown in Figure 27. The simulation run times for each simulator

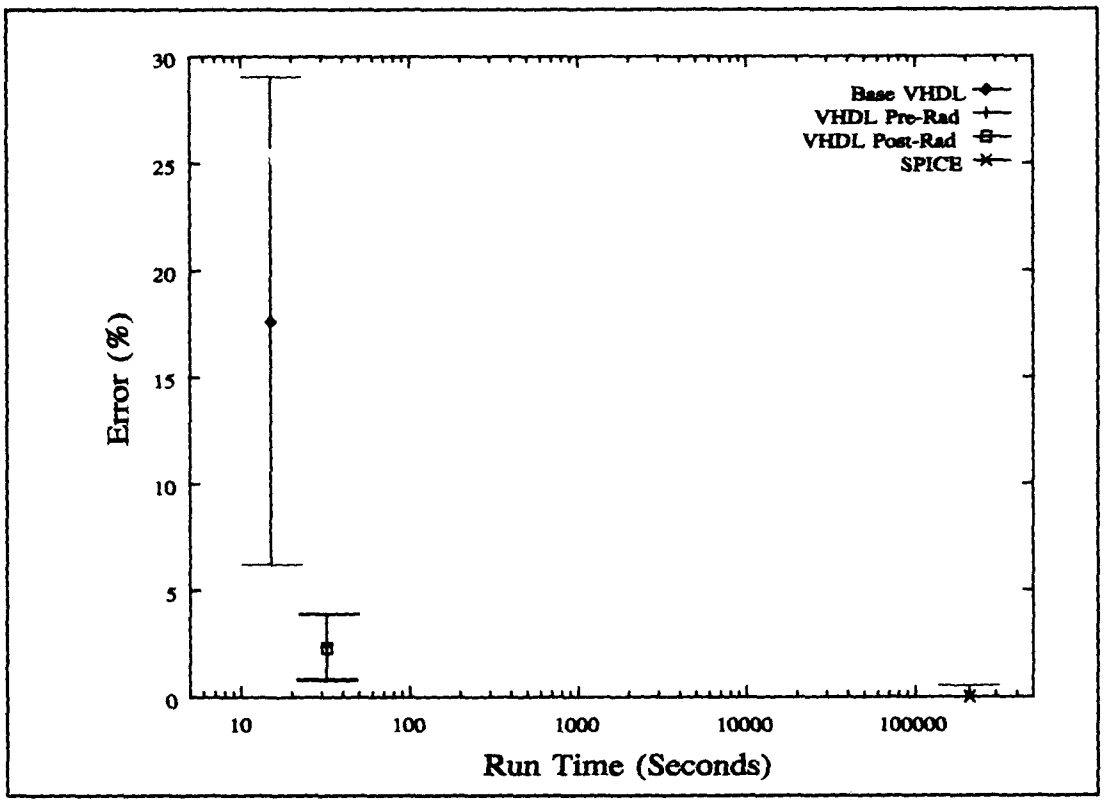

Figure 27. 16-Bit Microprocessor Control Unit, Simulation Timing Errors.

were far longer than the run times observed for any of the previous circuits. Each SPICE simulation pass took an average of 210,000 seconds (55 hours) to run, radiation-inclusive VHDL simulation took 32 seconds, and each base-VHDL simulation ran in 15 seconds. The mean of the absolute time delay error for the pre-radiation VHDL simulation was 2.4 percent while the error for the post-radiation VHDL simulation was 2.3 percent. The standard deviation for the pre- and post-radiation VHDL data were both 1.5 percent.

The base-VHDL error results are shown in Figure 27, at 15 seconds run time. The mean of the absolute error for the base-VHDL simulation run was 17.6 percent with a standard deviation of 11.4 percent. As with all the previous circuits tested, the SPICE simulation timing accuracy results varied less than one percent.

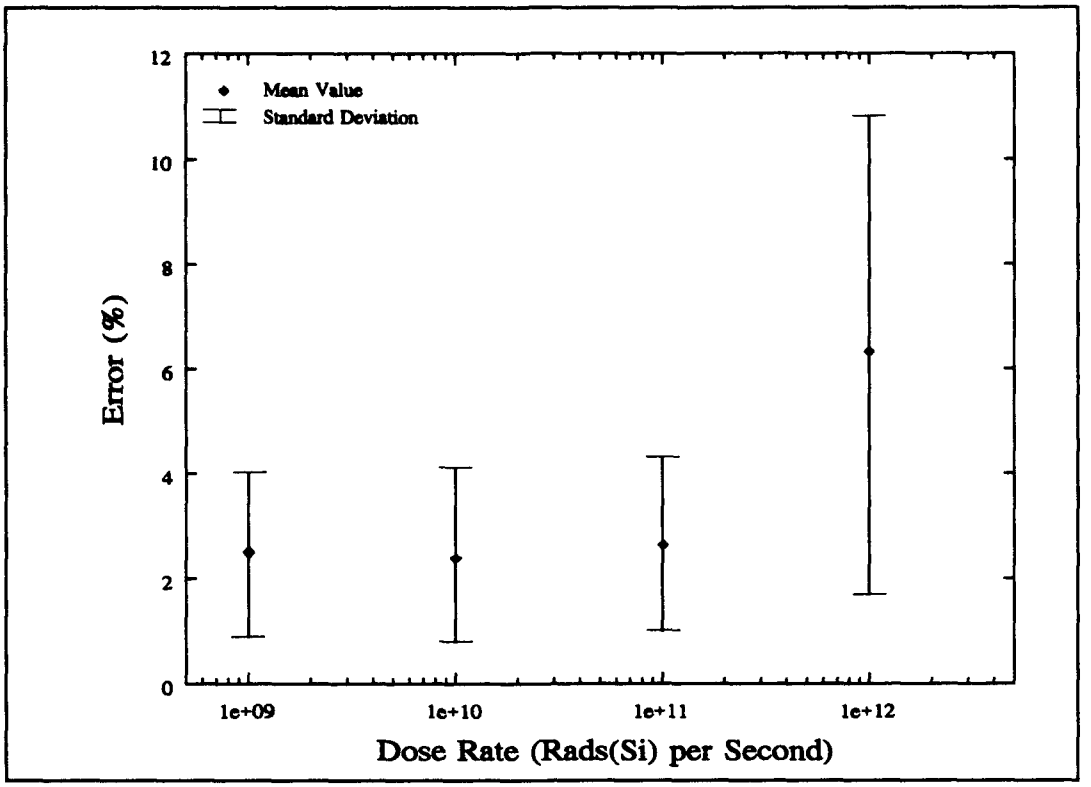

Figure 28. 16-Bit Microprocessor Control Unit Dose Rate Timing Accuracy.

Timing accuracy results are presented in Figure 28 for the simulation of the 16-bit microprocessor control unit when exposed to the range of radiation dose rates ranging from 1×10^{9} to 1×10^{12} rads(Si) per second. As with the last three circuits, timing accuracy remains close to that of the pre- and post-radiation dose environments for dose rates up to 1×10^{11} rads(Si) per second. For a dose rate of 1×10^{12} rads(Si) per second, the mean timing error increased slightly to just over six percent. At dose rates above 1×10^{12} rads(Si) per second, the circuit no longer functions correctly since the flip-flops do not change logic state.

Timing accuracy for the radiation-inclusive model VHDL simulating the 16-bit microprocessor agreed well with the SPICE simulation results, with the mean error being under 3 percent for all but the two highest radiation dose rates tested. Although the most

complex circuit tested, similar timing accuracy results were obtained from the radiation-inclusive model VHDL simulations, as were obtained with the first three circuits tested.

Table 10. Simulation Run Time and Timing Error Summary

	Base VHDL		Rad Model VHDL			SPICE
	Run Time (s)	Error (%)	Run Time (s)	Pre_Rad Error (%)	1 Mrad Error (%)	Run Time (s)
Four-Bit Adder	0.25	29.7	0.9	2.3	2.5	340
BCD to Seven-Segment	1.1	19.8	2.5	4.1	3.8	940
Oven Controller	1.8	13.5	5.0	3.0	3.2	10,800
Microprocessor	15	17.6	32	2.4	2.3	210,000

6.2.5 Measurement Summary. As the circuits increased in complexity, the ratio of the VHDL to SPICE run times increased significantly. Table 10 summarizes the run time and timing accuracy results for the four logic circuits simulated. The error values are the mean of the absolute value of the timing error, using the SPICE results as the baseline. The errors shown for the radiation-inclusive VHDL models include the results for both the pre-radiation and 1 Mrad(Si) total dose. The run time is the average run time for each pass of the simulator as shown. The base-VHDL shows the timing error of VHDL without the incorporation of the models developed for this research in the pre-radiation environment only. In the four-bit full-adder, the run time ratio of the SPICE to the radiation-inclusive model VHDL simulations was over 380 to 1. In the final circuit tested, the 16-bit microprocessor, the ratio of the run times of SPICE to the radiation-inclusive model VHDL simulations was over 6000 to 1. This increase in the run time ratio was due to the VHDL being an event driven simulator, while SPICE is a node driven simulator. The difference in run time between the two different VHDL simulators

was due to the increased complexity incurred in calculating each logic gate transition time delay for the radiation-inclusive model VHDL simulations.

Figure 29 shows the run time ratio of the microelectronic circuit simulators, where the run time ratio (τ) is defined by the equation:

$$\tau = \frac{\textit{Simulation Run Time on SPARCstation II}}{\textit{Event Time Simulated } (\mu S)} \qquad (18)$$

The simulation run time on the SPARCstation II is the measured run time of the simulation. The event time simulated is the time an actual circuit would operate in the real world, measured in microseconds (μS). The run time ratio increases with increasing transistor count for each simulator. The difference in run time ratios between the two VHDL simulators remain nearly constant for all cases tested. The VHDL-based simulations run over 100 times faster than SPICE on small circuits and increase to over 6000 times faster on the largest circuit tested. The run time ratios of the VHDL-based simulations diverge from the SPICE simulations as transistor count increases.

Timing accuracy of the radiation-inclusive model VHDL remains consistent over all four of the circuits tested, with the mean error remaining under 5 percent for all four circuits. Timing accuracy of the base-VHDL varied greatly, depending on individual signal paths. Since the time delay for each logic gate in the base-VHDL was fixed, any variance in fanout loading led to large errors in the time delay estimates. While the radiation-inclusive model VHDL required more CPU time to simulate than the base-VHDL, it was orders of magnitude faster than SPICE. The radiation-inclusive model VHDL provided timing estimates that were within a few percent of the values obtained from SPICE.

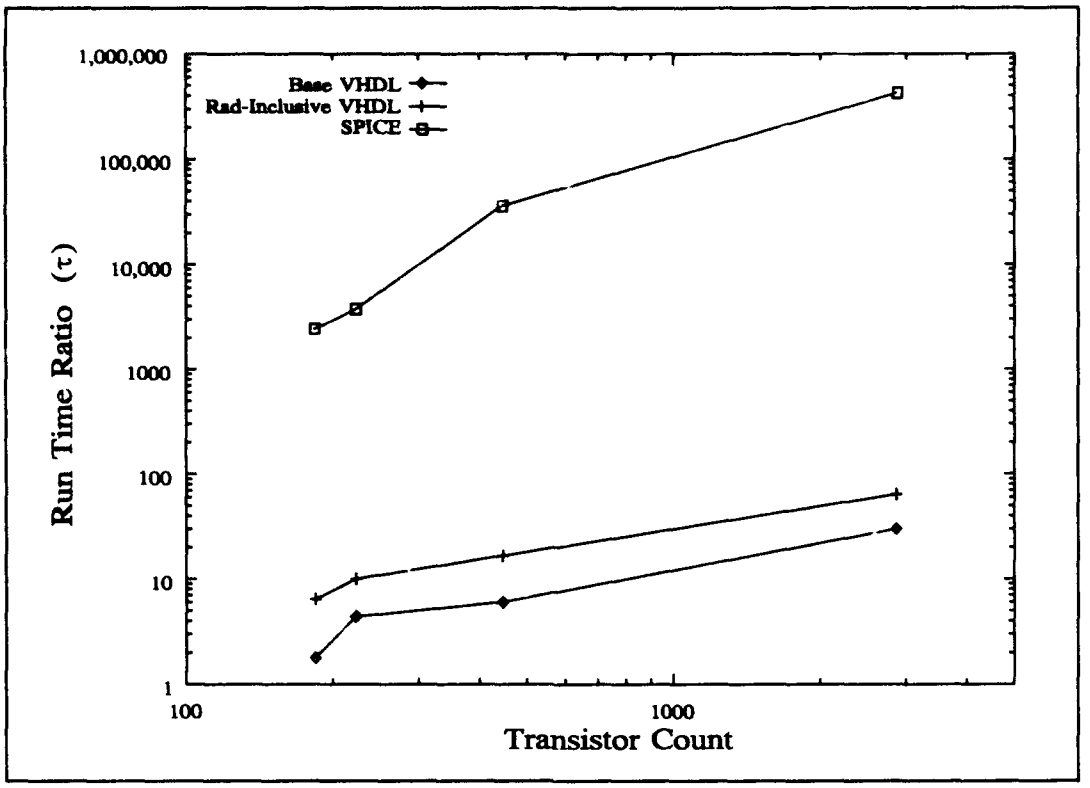

Figure 29. Simulation Run Time Ratio (τ) Versus Number of Transistors in Circuit.

6.3 Error Sources

This section discusses several identified sources of time delay estimation error in the radiation-inclusive model VHDL simulations. The identified sources of error include: multiple pull-up and pull-down, rise and fall rate variation, model variable units, SPICE run-to-run variability, and dose rate induced output voltage sag. The largest observed error source in the pre-radiation and 1 Mrad(Si) total dose radiation environment is multiple pull-up and pull-down. Another significant source of error is differences in logic gate rise and fall rates. Smaller error sources were identified due to limits imposed by the base units of the capacitance and resistance chosen for the time delay calculations. SPICE simulations were not perfectly repeatable, leading to errors in modeling the logic gate time delays. Finally, a large dose rate specific error source in time delay estimation

was observed; output voltages did not swing all the way to the rail voltages when the radiation dose rates exceeded 1×10^{10} Rads(Si) per second. Significant timing estimate errors were the result of the reduced output voltages at each logic gate output.

6.3.1 Multiple Pull-up and Pull-down. The phenomena causing the largest observed timing error, in the non-dose rate environment simulation, was due to multiple pull-up and pull-down induced timing errors. This error source was observed by examining the timing errors after the SPICE and VHDL simulations were completed. Errors exceeding 10 percent were observed. One example is the multiple pull-up found at the three-input OR gate at output *Seg-6* of the BCD to seven-segment converter which produced an error of 10.4 percent. This event occurs when the *I1* input drives *Seg-6* through two different signal paths; *I1* to *AN210* to *OR310* to *Seg-6* and *I1* to *EX210* to *OR310* to *Seg-6*. When the second input switches from a logic '1' to a logic '0' before the gate transitions from a logic '0' to a logic '1', the second input turns on a second PMOS transistor decreasing the overall switching time of the gate. Figure 30 shows the equivalent schematic of the three-input NOR and NAND gate. The NOR gate has the potential for the pull-down drive capability to be as large as three single pull-down outputs. The three-input NAND gate has the potential for the pull-up drive capability to be equivalent to three single pull-up outputs. In the radiation-inclusive model VHDL, the only provision for a NAND gate multiple pull-up or NOR gate pull-down timing change is a *Glitch* report that is issued as part of a procedure call. Appendix A contains the VHDL description for the two-input NAND gate and includes the procedure call to invoke the *Glitch* report.

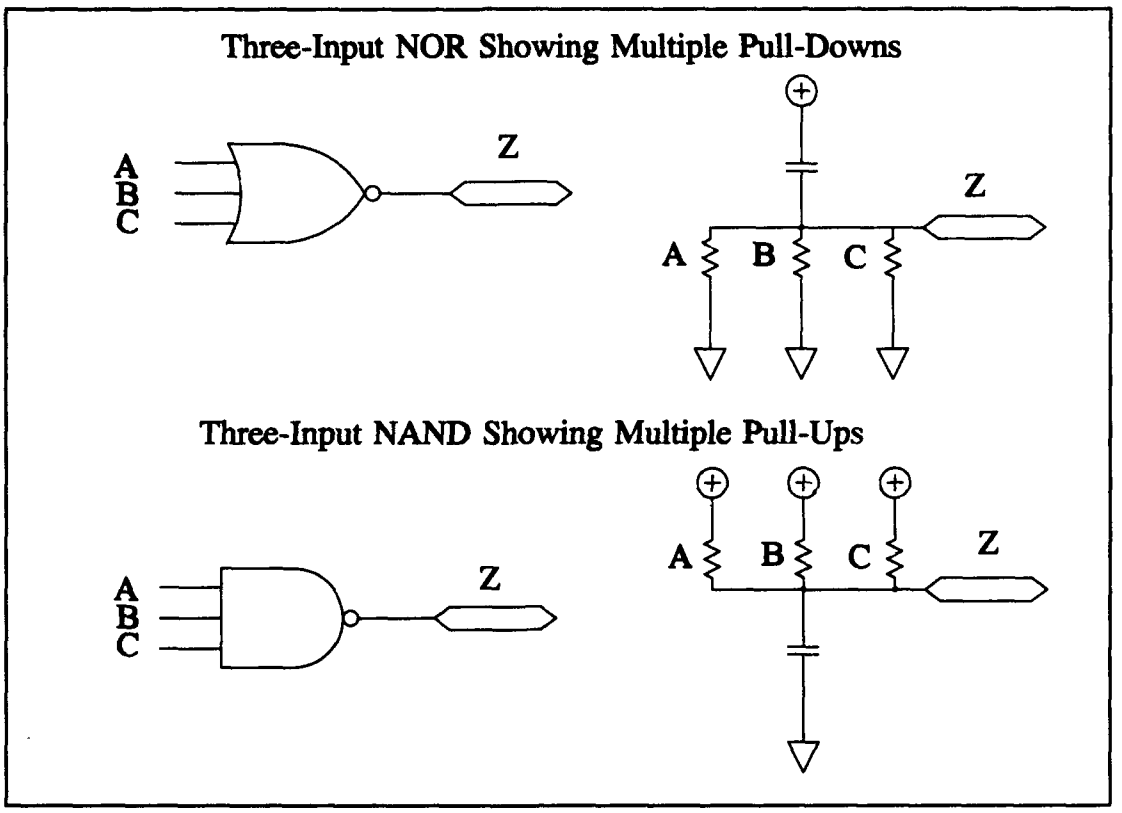

Figure 30. Logic Gate Multiple Pull-Downs and Pull-Ups.

To improve the radiation-inclusive model VHDL timing accuracy, multiple pull-up and pull-down timing effects must be determined and modeled. The multiple pull-up and pull-down timing effect will decrease the logic-gate state-transition time delay when a multiple pull-up or pull-down event occurs. The models should then be incorporated into the radiation-inclusive timing models. The models must then be incorporated into the radiation-inclusive model VHDL descriptions. This task must be accomplished for every multiple input logic gate in the VHDL Library. Simulation run time should not be affected significantly since these timing changes will replace a *Glitch* report when a multiple pull-up or pull-down occurs.

6.3.2 Rise and Fall Rate Variation. Every different configuration of each logic gate produces not only different transition delay times, but also different rise and fall times. Different rise and fall times affect not only the transition delay time of a gate, but also have an effect on the transition delay time of the gates in the succeeding stage. In this research effort, an attempt was made to account for differing rise and fall times by measuring transition delay time after an inverter in the succeeding stage. This method of rise and fall time compensation used in the radiation-inclusive model VHDL worked better than no rise and fall time compensation and provided over a five-percent improvement in the no rise and fall time compensation timing estimates, as tested in the single logic gate tests. The compensation employed was not ideal in predicting the changes in rise and fall times on the more complex logic gate stages. Better compensation could yield a one percent decrease in the overall timing error of the radiation-inclusive VHDL model simulations.

6.3.3 Model Variable Units. Changing the base units of the capacitance parameter would increase the accuracy of timing delay calculations. The base capacitance unit chosen for this research effort was the femtofarad, but after data collection, it became apparent that a smaller base unit would increase accuracy in intrinsic time delay estimates. Several of the logic gates had intrinsic time delay capacitance values below 50 fF with two below 20 fF. Round off, in the worse case condition, led to timing estimate errors of greater than one percent, as calculated by the equation:

$$E_T = \frac{(C_{load}+C_{pull-up-int-a})-(C_{load}+C_{pull-up-int})}{C_{load}+C_{pull-up-int-a}} \times 100\% \qquad (19)$$

$$E_T = \frac{(27+18.5)-(27+19)}{27+18.5} \times 100\% = -1.1\%$$

where:

E_T	-	Timing Estimate Error
$C_{pull-up-int-a}$	-	Calculated Intrinsic Capacitance, $IV110_{pull-up}$
$C_{pull-up-int}$	-	Model Value Intrinsic Capacitance, $IV110_{pull-up}$

The E_T shown in the equation above represents the model round-off error observed for the pull-up condition of the inverter IV110 when connected to a single fanout load of 27 fF. For example, a 1.1 percent error would be observed at each stage of a ring oscillator constructed from inverters. Changing the capacitance and resistance units would require modifying and executing all the model to radiation-inclusive VHDL description conversion programs for each of the logic gates in the VHDL library.

6.3.4 SPICE Run-to-Run Variability. Results of the circuit simulation runs of SPICE were not identical when the transistor net list order was changed. SPICE is a node driven simulator which generates variations in the results caused by the node variables as stored in the computer running the simulation. Variations in the simulation variable values used to calculate node voltage and current values for each time slice have an effect on simulation accuracy. Delta time errors also occur as the time slices are shortened in an attempt to simulate circuit operation more accurately. In some cases tested, input-to-output transition time delays varied by as much as one percent when the SPICE node matrix was reordered. Since SPICE simulation results varied, VHDL timing models

developed could not be expected to yield better results than the baseline SPICE data provided since SPICE was the standard.

6.3.5 Radiation Dose-Rate Induced Output Voltage Sag. Photocurrent generation in a radiation dose-rate environment limited each logic gate output voltage swing to less than full rail-to-rail output voltage swing. At radiation dose-rates greater than 1×10^{10} Rads(Si) per second, photocurrent generation was high enough in the turned-off transistors to keep the turned-on transistors from pulling the output voltage all the way to the rail voltage. An example of this phenomena is observed when the BCD to seven-segment converter is tested at 2×10^{12} rads(Si) per second. The three-input NAND gate only has a voltage swing from 1.97 to 4.90 volts while the two-input NOR gate has a voltage swing from 0.19 to 4.06 volts, as shown in Figure 31. The radiation-inclusive model VHDL does not include the potential effects of photocurrent induced power supply voltage decrease in the microelectronic circuit voltage rails.

One potential solution to modeling circuit operation when the radiation dose rate is high enough to prevent gate outputs from reaching the voltage supply values is to model circuit operation using a multi-level logic modeling technique [16]. This modeling technique involves dividing the output logic values into several different logic values based on the output voltage level. Since logic values are modeled using multi-level values, simulation run time would be slower than those observed in this research, by as much as an order of magnitude. Time delay errors for the radiation dose rates above 1×10^{11} rads(Si) per second should be able to match SPICE results to within 15 percent.

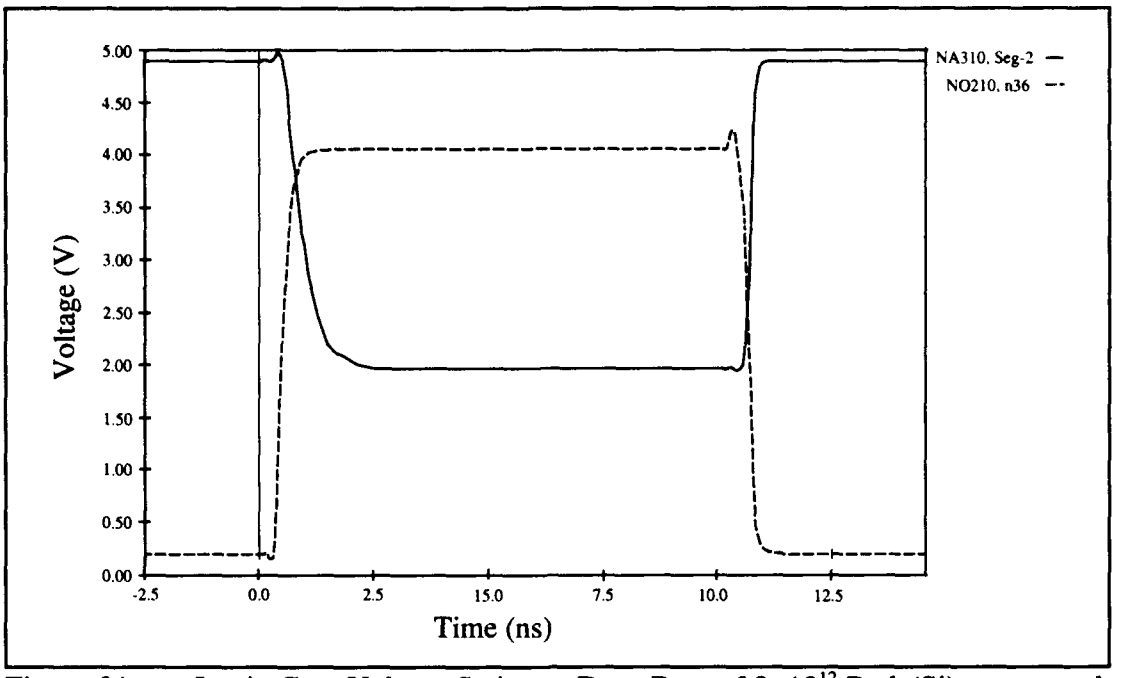

Figure 31. Logic Gate Voltage Swing at Dose Rate of 2×10^{12} Rads(Si) per second.

6.4 Summary

This chapter described the measurement results of the simulation runs using base VHDL, radiation-inclusive model VHDL, and SPICE for all four circuits tested. The results were discussed for the four-bit full-adder, BCD to seven-segment converter, microwave oven controller, and 16-bit microprocessor control unit. Summaries of the time delay accuracy and simulator run time were presented. The radiation-inclusive model VHDL provided timing estimate accuracy that compared favorably with the results obtained using SPICE; in the pre-radiation environment the mean error was less than 5 percent. The 1 Mrad(si) total dose simulations also yielded a mean error of less than 5 percent. While the dose rate simulation timing estimates had a significant increase in error when estimating time delays accurately at dose rates above 1×10^{11} rads(Si) per second, accuracy below that dose rate was comparable to the pre-radiation results.

The time delay error sources were discussed for radiation-inclusive VHDL-based simulator. The largest timing errors observed in the radiation dose rate environment were due to each logic gate having a different output-high and output-low voltage swing at dose rates above 1×10^{11} rads(Si) per second. The largest timing errors observed in the pre-radiation and 1 Mrad(Si) total dose environment were due to multiple pull-up and pull-down timing errors. Smaller, but easier to accommodate, timing estimate error sources in the radiation-inclusive model are: rise and fall time variation and model variable units.

VII. Conclusion

7.1 Summary

The overarching goal of this research was the rapid and accurate timing simulation of radiation-hardened microelectronic circuits. Two issues required consideration and resolution in reaching this goal; accurately simulating microelectronic circuits in a pre-radiation environment had to be addressed as well as changes in circuit timing performance caused by radiation effects.

Differing radiation total dose levels and dose rates affect the operation and timing performance of microelectronic circuits. Some changes are temporary and anneal with time while other changes are permanent. Two separate radiation effects were considered. The effects of total dose ionizing radiation were modeled at a level of 1 Mrad(Si), and the effects of radiation dose rates were modeled for dose rates ranging from 1×10^{9} to 2×10^{12} rads(Si) per second.

The development of simple generic models providing rapid and accurate timing estimates for simulating radiation-hardened microelectronic circuits, using a VHDL-based simulator, was the core of this research effort. The initial goal was for the simulator to run at least two orders of magnitude faster than SPICE while maintaining timing accuracy within ten to 15 percent of the SPICE values.

Development of the timing models was divided into several steps. First, all the time delay sources were determined. Defined time delay sources included: time delays due to logic gate fanout loading, logic gate intrinsic time delay, and radiation

environment. Next, the time delay source information was used to develop the timing models. The timing models were incorporated into VHDL descriptions and then validated in a simple logic circuit. Finally, after the timing models were incorporated into the complete VHDL description library, validation testing was conducted on circuits of differing complexity.

Model development focused on modeling the time delay sources to run in an efficient manner while incorporated into VHDL descriptions. The modeling process was divided into several separate processes. Defining time delay sources in three steps allowed the models to be developed in independent segments. First, logic gate input load values were determined, using SPICE, to be 27 fF for simple single CMOS transistor pairs in the TI 0.8μm SIMOX fabrication process. Second, the drive capability, modeled as a resistance, was determined. The drive resistance in combination with the load capacitance defined the fanout loading effects on timing. Third, the logic gate intrinsic time delay effects were modeled as capacitance values and used in combination with the drive resistance values to define the internal intrinsic time delay of the gate. Finally, the effects of radiation on circuit timing was modeled by adjusting the values of resistance and capacitance which define the timing characteristics of each gate.

VHDL code development focused on efficient implementation of the timing models describing the timing characteristics of each logic gate. VHDL descriptions were developed for each gate modeled in TI SIMOX SPICE library. Each description contained the code necessary to simulate the function and timing performance of the logic gate. After each description was developed, it was validated against data obtained using SPICE.

Initially, each timing model was checked via a VHDL description for each logic gate level. Next, the models were checked using a simple logic circuit, the four-bit full-adder. After completion of the initial testing, more comprehensive testing was conducted.

The results of testing the timing models, incorporated into VHDL descriptions and simulated as a four-bit full-adder, indicated the timing models would meet the indicated goals of simulating a circuit two orders of magnitude faster while retaining timing accuracy to within ten to 15 percent of the results obtained using SPICE. The next step was to select additional circuits to simulate, validating the accuracy and run time performance of the radiation-inclusive model VHDL. The three circuits selected included: a BCD to seven-segment converter, a microwave oven controller, and a 16-bit microprocessor control unit. The most complex circuit, the 16-bit microprocessor control unit containing over 2800 transistors, simulated over 6000 times faster in VHDL than in SPICE, and maintained timing accuracy with a mean error of less than four percent.

7.2 Conclusions

Evaluation of the radiation-inclusive model VHDL led to several observations. The radiation-inclusive models developed in this research are simple and easy to modify for specific microelectronic fabrication technologies, including the parameters modeling radiation effects on circuits. The time delay parameters are modeled as simple resistive and capacitive elements. Radiation effects are incorporated into the models by adjusting the resistive and capacitive element values.

The radiation-inclusive model VHDL simulator is an accurate timing simulator with the absolute value of the mean error remaining under 5 percent for all circuits tested

at dose rates of 1×10^{11} rads(Si) per second and lower. The radiation-inclusive model VHDL is able to simulate VLSI circuits quickly with the simulation run time ratio improving over SPICE as the circuit becomes more complex. The simulation run time for the four-bit full-adder was over 380 times faster for the radiation-inclusive model VHDL than SPICE. Likewise, the simulation run time for the complex 16-bit microprocessor was over 6000 times faster than SPICE with no degradation in timing accuracy.

Finally, the radiation-inclusive model VHDL descriptions can be simplified for implementation as a non-radiation environment timing simulator. The radiation-inclusive parameter variables and the radiation effects procedure calls can be removed from the generic declarations of the VHDL descriptions, simplifying the descriptions for use as a non-radiation environment timing simulator. Simplifying the radiation-inclusive VHDL model descriptions allows designers to adapt the models for use in circuit design when radiation effects are not a concern, while retaining the timing accuracy of the radiation-inclusive VHDL models. Simulation run time will be faster than the radiation-inclusive VHDL models but still slower than base VHDL.

7.3 Recommendations

Four areas of the timing estimation modeling have been identified as needing additional modifications to improve the accuracy of the VHDL-based timing simulator. First, significant errors were observed in the modeling of multiple pull-up and pull-down input to output transitions. Second, variability in rise and fall times affected logic transition of downstream gates. Third, the resistance and capacitive units used to

calculate output transition changes of gates are defined in terms of physical units with base units of the ohm and femtofarad. Fourth, at radiation dose rates above 1×10^{11} rads(Si) per second, logic gate outputs are unable to sink all the generated photocurrents and provide output voltages at the plus and minus supply voltages.

The largest errors observed in the pre- and post-radiation environment, over ten percent, were due to multiple pull-ups in NAND gates and multiple pull-downs in NOR gates. In the radiation-inclusive models developed for this research, all multiple pull-up and pull-down events were recognized by the VHDL descriptions, and reported as glitches during timing simulation. To correct this deficiency, the effect on drive capability by multiple pull-up and pull-down effects needs to be modeled for the gates and incorporated into the VHDL descriptions.

Gate timing is affected not only by the output load it is driving but also by the rise and fall time of the input signal driving that gate. The radiation-inclusive models developed for this research attempted to account for slower than nominal rise and fall times by allocating the additional time delay to the driving gate. The additional time delay was modeled by measuring the effect of driving an inverter with the slow rise and fall time signals and then allocating this additional delay to the driving gate. Additional research is required to determine a more accurate modeling and implementation technique to account for effects of differing rise and fall signal times.

The models developed for this research used physical types in VHDL to define the units for resistance (ohms) and capacitance (femtofarad). Changing the physical types to real number types in VHDL will increase timing accuracy by up to 1.1 percent for the worst-case conditions. Simulation run time should increase by less than ten percent due

to this change since calculation of delay time is a small part of the radiation-inclusive model VHDL simulation run time.

The worst timing accuracy problems encountered during this research occurred while simulating circuit operation for radiation dose rates at 1×10^{11} rads(Si) per second and greater. At high radiation dose rates, logic gate outputs are unable to provide output voltages at the plus and minus supply voltage levels. The effects of reduced voltage output affects circuit timing and performance. Depending on circuit configuration, time delays may increase or decrease or the circuit may not operate as expected. One possible solution is to incorporate multi-level logic values into the radiation-inclusive models and base circuit operation and timing on the multi-level logic values.

This research effort demonstrated that it is possible to simulate microelectronic circuits orders of magnitude faster than SPICE while still maintaining reasonable accuracy. Timing accuracy is maintained for the pre-radiation, 1 Mrad(Si) total dose, and radiation dose rates below 1×10^{11} rads(Si) per second. Additional modifications to the radiation-inclusive models could enable increases in timing accuracy without substantial simulation run time penalties.

Appendix A: Two-Input NAND Gate (NA210) VHDL Description

This appendix contains the complete VHDL description for the two-input NAND gate. This description was analyzed using the Synopsys VHDL Analyzer, Version 3.0b. Simulations were run using the Synopsys VHDL Debugger, Version 3.0b. Minor modifications may be necessary to analyze this description on different simulators. Specific functions and procedures that may require special handling include: NAND, P_DELAY, SCHEDULE, and GLITCH_HANDLE. Three procedures written by the author must be included in order to analyze NA210. They are: Radiation_drive_cap, Radiation_drive_res, and Radiation_time_delay. These procedures are available in Appendix B.

The VHDL description of the cell NA210 simulates the function of a two-input NAND gate and includes the models to accurately estimate timing of the NAND gate. The VHDL description begins with the listing of the libraries necessary to compile and simulate the NAND gate. Next, the "entity declaration" contains two subsections, the generic and the port declarations. Finally, the "architecture body" contains the code describing the operation of the NAND gate in VHDL.

Four libraries are called by the two-input NAND gate VHDL description: IEEE, IEEE_ASIC, SYNOPSYS, and WORK. The IEEE library contains the VHDL nine-level logic definitions for the logical functions used in this cell. The IEEE_ASIC library contains the functions for the logical operation of this cell. The SYNOPSYS library contains the procedures and functions for input collision detection and reporting. An

input collision occurs when a gate is in a logic transition due to an input stimulus and additional input stimuli occur before the first transition is completed. The WORK library contains the procedures and declarations necessary for the radiation-inclusive timing estimation.

The entity declaration for the VHDL description is just after the library listing. The generic declarations section contains the parameter variables necessary for accurate timing estimation. The port declarations describe the logic signal and load information passing requirements of the description. The core of the VHDL description follows the entity declaration.

The architecture body section of the VHDL description defines the operation of the two-input NAND gate. The architecture body is divided into three subsections: logic function call, radiation dose process, and connect process. The logic function call, Func_Z, establishes the logic function of the VHDL description as a two-input NAND gate. The radiation dose process is invoked at simulation start-up and any time the radiation environment changes. The radiation dose process changes the drive resistance and internal intrinsic load capacitance values to account for effects of the radiation environment being simulated. The connect process is the core of the VHDL description. This process contains the function and procedure calls to determine the logic output, time delays, and input collisions resulting from an input stimulus. The final function of the connect process is to update the NAND gate output with the time of the event.

```
------ CELL NA210 -----------------------------
library IEEE;
  use IEEE.STD_LOGIC_1164.all;
  use IEEE.STD_LOGIC_MISC.all;
library IEEE_ASIC;
```

```
  use IEEE_ASIC.LIBCORE.all;
library SYNOPSYS;
  use SYNOPSYS.attributes.REAL_NAME;
  use SYNOPSYS.attributes.PRIVATE;
USE WORK.rad_tools.all;

-- entity declaration --
entity NA210 is
   generic(
      drive_res_rise_a          : resistance  :=   2468.0 ohm;
      drive_cap_rise_a          : capacitance :=     29.0 femtoF;
      drive_res_fall_a          : resistance  :=   2397.0 ohm;
      drive_cap_fall_a          : capacitance :=     36.0 femtoF;
      drive_res_postrad_rise_a  : real  :=    257.4;
      drive_cap_postrad_rise_a  : real  :=   0.2876E-14;
      drive_res_postrad_fall_a  : real  :=     57.8;
      drive_cap_postrad_fall_a  : real  :=  -0.1108E-14;
      drive_res_dose_rise_x_a   : real  :=  -0.6398E-09;
      drive_cap_dose_rise_x_a   : real  :=   0.3805E-26;
      drive_res_dose_fall_x_a   : real  :=   0.1287E-09;
      drive_cap_dose_fall_x_a   : real  :=  -0.1047E-25;
      drive_res_dose_rise_xx_a  : real  :=   0.7451E-22;
      drive_cap_dose_rise_xx_a  : real  :=   0.1188E-38;
      drive_res_dose_fall_xx_a  : real  :=   0.1349E-21;
      drive_cap_dose_fall_xx_a  : real  :=   0.2924E-39;

      drive_res_rise_b          : resistance  :=   2444.0 ohm;
      drive_cap_rise_b          : capacitance :=     38.0 femtoF;
      drive_res_fall_b          : resistance  :=   2349.0 ohm;
      drive_cap_fall_b          : capacitance :=     38.0 femtoF;
      drive_res_postrad_rise_b  : real  :=    251.1;
      drive_cap_postrad_rise_b  : real  :=   0.3374E-14;
      drive_res_postrad_fall_b  : real  :=    129.2;
      drive_cap_postrad_fall_b  : real  :=  -0.3127E-14;
      drive_res_dose_rise_x_b   : real  :=  -0.6298E-09;
      drive_cap_dose_rise_x_b   : real  :=   0.5151E-26;
      drive_res_dose_fall_x_b   : real  :=   0.2121E-09;
      drive_cap_dose_fall_x_b   : real  :=  -0.1429E-25;
      drive_res_dose_rise_xx_b  : real  :=   0.7382E-22;
      drive_cap_dose_rise_xx_b  : real  :=   0.2028E-38;
      drive_res_dose_fall_xx_b  : real  :=   0.1171E-21;
      drive_cap_dose_fall_xx_b  : real  :=   0.1256E-38;

      load_res             : resistance := 1 Gohm;
      load_cap             : capacitance := 27 femtoF;
      Timing_mesg          : Boolean     := True;
      Timing_xgen          : Boolean     := False);

   port(
      radiation_dose        : in  dose_record :=  default_rad;
      A                     : in  std_ulogic;
      A_load                : out signal_load :=  default_load;
      B                     : in  std_ulogic;
      B_load                : out signal_load :=  default_load;
      Z                     : out std_ulogic  :=  default_signal;
      Z_load                : in signal_load  :=  default_load);
end NA210;

-- architecture body --
architecture A of NA210 is
   signal connect : std_ulogic_VECTOR (0 to 1)  := (others => 'U');
   signal prop_Z  : std_ulogic_VECTOR (0 to 1)  := (others => 'U');
   signal resistance_drive_r_a  : resistance  := drive_res_rise_a;
   signal resistance_drive_f_a  : resistance  := drive_res_fall_a;
```

```
   signal capacitance_drive_r_a : capacitance := drive_cap_rise_a;
   signal capacitance_drive_f_a : capacitance := drive_cap_fall_a;
   signal resistance_drive_r_b  : resistance  := drive_res_rise_b;
   signal resistance_drive_f_b  : resistance  := drive_res_fall_b;
   signal capacitance_drive_r_b : capacitance := drive_cap_rise_b;
   signal capacitance_drive_f_b : capacitance := drive_cap_fall_b;

function Func_Z(constant A : in std_ulogic;
           constant B : in std_ulogic) return std_ulogic is
begin
    -- func((A B)')
    return("NAND"(A, B));
end Func_Z;

begin -- architecture

------------- RAD effects drive & load calc --------------
process (radiation_dose)
   variable res_drive_r_a  : resistance  := drive_res_rise_a;
   variable res_drive_f_a  : resistance  := drive_res_fall_a;
   variable cap_drive_r_a  : capacitance := drive_cap_rise_a;
   variable cap_drive_f_a  : capacitance := drive_cap_fall_a;
   variable res_drive_r_b  : resistance  := drive_res_rise_b;
   variable res_drive_f_b  : resistance  := drive_res_fall_b;
   variable cap_drive_r_b  : capacitance := drive_cap_rise_b;
   variable cap_drive_f_b  : capacitance := drive_cap_fall_b;

begin
res_drive_r_a  := drive_res_rise_a;
res_drive_f_a  := drive_res_fall_a;
cap_drive_r_a  := drive_cap_rise_a;
cap_drive_f_a  := drive_cap_fall_a;
res_drive_r_b  := drive_res_rise_b;
res_drive_f_b  := drive_res_fall_b;
cap_drive_r_b  := drive_cap_rise_b;
cap_drive_f_b  := drive_cap_fall_b;

Radiation_drive_res(radiation_dose,    res_drive_r_a,
      drive_res_postrad_rise_a, drive_res_dose_rise_x_a,
       drive_res_dose_rise_xx_a);
Radiation_drive_cap(radiation_dose, cap_drive_r_a,
       drive_cap_postrad_rise_a, drive_cap_dose_rise_x_a,
       drive_cap_dose_rise_xx_a);
  resistance_drive_r_a    <= res_drive_r_a;
  capacitance_drive_r_a   <= cap_drive_r_a;
Radiation_drive_res(radiation_dose, res_drive_f_a,
       drive_res_postrad_fall_a, drive_res_dose_fall_x_a,
       drive_res_dose_fall_xx_a);
Radiation_drive_cap(radiation_dose, cap_drive_f_a,
       drive_cap_postrad_fall_a, drive_cap_dose_fall_x_a,
       drive_cap_dose_fall_xx_a);
  resistance_drive_f_a    <= res_drive_f_a;
  capacitance_drive_f_a   <= cap_drive_f_a;

Radiation_drive_res(radiation_dose, res_drive_r_b,
       drive_res_postrad_rise_b, drive_res_dose_rise_x_b,
       drive_res_dose_rise_xx_b);
Radiation_drive_cap(radiation_dose, cap_drive_r_b,
       drive_cap_postrad_rise_b, drive_cap_dose_rise_x_b,
       drive_cap_dose_rise_xx_b);
  resistance_drive_r_b    <= res_drive_r_b;
  capacitance_drive_r_b   <= cap_drive_r_b;
Radiation_drive_res(radiation_dose, res_drive_f_b,
       drive_res_postrad_fall_b, drive_res_dose_fall_x_b,
```

```
        drive_res_dose_fall_xx_b);
Radiation_drive_cap(radiation_dose, cap_drive_f_b,
        drive_cap_postrad_fall_b, drive_cap_dose_fall_x_b,
        drive_cap_dose_fall_xx_b);
  resistance_drive_f_b    <= res_drive_f_b;
  capacitance_drive_f_b   <= cap_drive_f_b;

  A_load.drive_load_res <= load_res ;
  A_load.load_cap       <= load_cap;
  B_load.drive_load_res <= load_res ;
  B_load.load_cap       <= load_cap;
end process;
-------------------------------------------------------------
   connect(0) <= transport To_UX01(A);
   connect(1) <= transport To_UX01(B);

process (connect)
   variable pend_out     : std_ulogic := 'U';
   variable current_out  : std_ulogic;
   variable proj_out     : std_ulogic;
   variable delay_rise   : time := 0 ns;
   variable delay_fall   : time := 0 ns;
   variable pend_event   : time := 0 ns;
   variable proj_delay   : time := 0 ns;
   variable drive_rise   : signal_load;
   variable drive_fall   : signal_load;
   variable hazard       : Boolean;

begin
   current_out := Func_Z(prop_Z(0), prop_Z(1));
   proj_out    := Func_Z(connect(0), connect(1));

   -- timing arcs A-Z
   if connect(0)'event then
  ------------ RAD effects delay clac ---------------------
  drive_rise.drive_load_res := resistance_drive_r_a;
  drive_fall.drive_load_res := resistance_drive_f_a;

  drive_rise.load_cap       := capacitance_drive_r_a;
  drive_fall.load_cap       := capacitance_drive_f_a;

    Radiation_time_delay   (drive_rise, drive_fall, Z_load,
                            delay_rise, delay_fall);
  -------------------------------------------------------------
        proj_delay := P_DELAY(connect(0)'delayed, connect(0),
                              delay_fall, delay_rise);
        SCHEDULE(connect(0),prop_Z(0),current_out,proj_out,pend_event,
                 pend_out,proj_delay,hazard);
        if hazard then
            GLITCH_HANDLE("Z","A", pend_event, proj_delay, Timing_mesg,
                          Timing_xgen, connect,prop_Z);
        end if;
        pend_event := proj_delay + Now;
   end if;

   -- timing arcs B-Z
   if connect(1)'event then
  ------------ RAD effects delay clac ---------------------
  drive_rise.drive_load_res := resistance_drive_r_b;
  drive_fall.drive_load_res := resistance_drive_f_b;

  drive_rise.load_cap       := capacitance_drive_r_b;
  drive_fall.load_cap       := capacitance_drive_f_b;
```

```
    Radiation_time_delay   (drive_rise, drive_fall, Z_load,
                            delay_rise, delay_fall);
  ------------------------------------------------------------
        proj_delay := P_DELAY(connect(1)'delayed, connect(1),
                              delay_fall, delay_rise);
        SCHEDULE(connect(1),prop_Z(1),current_out,proj_out,pend_event,
                 pend_out,proj_delay,hazard);
        if hazard then
           GLITCH_HANDLE("Z","B",pend_event,proj_delay,Timing_mesg,
                         Timing_xgen, connect, prop_Z);
        end if;
        pend_event := proj_delay + Now;
   end if;
end process;

   Z <= Func_Z(prop_Z(0), prop_Z(1));
end A;

configuration CFG_NA210_A of NA210 is
   for A
   end for;
end CFG_NA210_A;
------ END CELL NA210 -------------------------
```

Appendix B: VHDL Radiation Effects Procedures

This appendix contains the package rad-tools, which consists of the radiation-inclusive parameter unit declarations and the three radiation-inclusive procedures. The first procedure, Radiation_time_delay, is necessary to calculate each gate time delay. The second and third procedures are used to determine the drive resistance and the intrinsic time delay capacitance.

Radiation_time_delay has three inputs and two outputs. The inputs contain the composite drive and load values, while the two outputs provide the calling VHDL description with the time delay values. The composite drive and load values are composed of a resistance and a capacitance value. Radiation_time_delay procedure is simple. The capacitance values are summed and the time delay is calculated using the equation:

$$T_d = \frac{(R_{drive} + R_{load}) \times R_{drive} \times C_{sum}}{R_{load} - R_{Drive}} \tag{20}$$

where:

- T_d - Time Delay
- R_{drive} - Drive Resistance
- R_{load} - Sum of Load Resistance Values
- C_{sum} - Sum of Capacitance Values

This equation allows for the incorporation of stuck-at faults, if the load gate leakage becomes as large as the drive capability. For the technology used in this research (TI

SIMOX), the R_{load} values remain high and are not a factor. The balance of the Radiation_time_delay procedure is consumed in converting units.

The second and third procedures contained in this appendix, Radiation_drive_res and Radiation_drive_cap, are used to adjust values of the drive resistance and internal intrinsic load capacitance to account for the simulated radiation-inclusive environment. Both procedures determine the radiation-inclusive values using the equation:

$$X_{ri}=X+(X_p \times D_T)+((X_b \times D_R)+(X_a \times D_R^2)) \tag{21}$$

where:

X_{ri}	-	Value of Resistance or Capacitance, Radiation-Inclusive
X	-	Value of Resistance or Capacitance, Pre-Radiation
X_p	-	Value of Resistance or Capacitance, Post-Radition, Total Dose
X_a	-	Value of Resistance or Capacitance, Dose Rate Squared Term of Quadratic Equation
X_b	-	Value of Resistance or Capacitance, Dose Rate Term of Quadratic Equation
D_T	-	Total Dose, 1 Mrad(Si)
D_R	-	Dose Rate in Rads(Si) per Second

The balance of the two procedures is used in converting units.

```
----- PACKAGE rad_tools ----------------------
library IEEE;
  use IEEE.STD_LOGIC_1164.all;
  use IEEE.STD_LOGIC_MISC.all;
library IEEE_ASIC;
  use IEEE_ASIC.LIBCORE.all;
library SYNOPSYS;
  use SYNOPSYS.attributes.REAL_NAME;
  use SYNOPSYS.attributes.PRIVATE;

PACKAGE rad_tools IS

  TYPE capacitance IS  RANGE 0 to (2**30)
     UNITS
        femtoF;              -- base unit
        pF = 1000 femtoF;
        nF = 1000 pF;
        uf = 1000 nf;
     END UNITS;

  TYPE resistance IS  RANGE  0 to (2**30)
```

```
    UNITS
       ohm;                -- base unit
       kohm = 1000 ohm;
       Mohm = 1000 kohm;
       Gohm = 1000 Mohm;
    END UNITS;

  TYPE dose IS  RANGE  0 to (1000001)
    UNITS
       rads;               -- base unit
       krads = 1000 rads;
       Mrads = 1000 krads;
    END UNITS;

  TYPE dose_rate IS  RANGE  0 to (2000000001)
    UNITS
       krads_s;               -- base unit
       Mrads_s = 1000 krads_s;
       Grads_s = 1000 Mrads_s;
       Trads_s = 1000 Grads_s;
    END UNITS;

  TYPE dose_record IS
      RECORD      dose_value      : dose;
                  dose_rate_value : dose_rate;
      END RECORD;

  CONSTANT default_rad : dose_record :=  (0 rads, 0 krads_s);

  CONSTANT default_signal : std_ulogic := 'X';

  TYPE signal_load IS
      RECORD      drive_load_res : resistance;
            load_cap       : capacitance;
      END RECORD;

  TYPE load_array IS array (integer range <>) of signal_load;

  CONSTANT default_load : signal_load :=  (1 Gohm, 27 femtoF);

  PROCEDURE Radiation_time_delay(
      A_drive_rise        : in  signal_load;
      A_drive_fall        : in  signal_load;
      Z_load              : in  signal_load;
      delay_rise          : out time;
      delay_fall          : out time);

PROCEDURE Radiation_drive_res(
      radiation_dose      : in  dose_record;
      drive_res           : inout  resistance;
      drive_res_postrad   : in real;
      drive_res_dose_x    : in real;
      drive_res_dose_xx   : in real);

PROCEDURE Radiation_drive_cap(
      radiation_dose      : in  dose_record;
      drive_cap           : inout  capacitance;
      drive_cap_postrad   : in real;
      drive_cap_dose_x    : in real;
      drive_cap_dose_xx   : in real);

END rad_tools;
------ END PACKAGE rad_tools ----------------------
```

```
PACKAGE BODY rad_tools IS

PROCEDURE Radiation_time_delay(
      A_drive_rise         : in  signal_load;
      A_drive_fall         : in  signal_load;
      Z_load               : in  signal_load;
      delay_rise           : out time;
      delay_fall           : out time) is

   variable sum_cap        : real := 0.0;
   variable temp_time      : real := 0.0;
   variable Rd_real        : real := 0.0;
   variable Rl_real        : real := 0.0;

begin
--------------------------- RAD effects delay clac ---------------------
 sum_cap   := real(capacitance'POS(Z_load.load_cap));       -- C in femtoF
 sum_cap   := sum_cap + real(capacitance'POS(A_drive_rise.load_cap));
 Rl_real   := real(resistance'POS(Z_load.drive_load_res));  -- R in Ohms
 Rd_real   := real(resistance'POS(A_drive_rise.drive_load_res));
 temp_time  :=  ((Rl_real  +  Rd_real)  *  Rd_real  *  sum_cap)/((Rl_real  -
Rd_real)* 1.0e3);
    if temp_time < 0.0 then
     temp_time := (real(time'POS(time'HIGH)))/2.0;
   elsif temp_time > real(time'POS(time'HIGH)) then
     temp_time := (real(time'POS(time'HIGH)))/2.0;
   end if;
 delay_rise :=  (1 ps * (integer(temp_time))); -- timebase in ps

 sum_cap   := real(capacitance'POS(Z_load.load_cap));       -- C in femtoF
 sum_cap   := sum_cap + real(capacitance'POS(A_drive_fall.load_cap));
 Rd_real   := real(resistance'POS(A_drive_fall.drive_load_res));
 temp_time  :=  ((Rl_real  +  Rd_real)  *  Rd_real  *  sum_cap)/((Rl_real  -
Rd_real)* 1.0e3);
   if temp_time < 0.0 then
     temp_time := (real(time'POS(time'HIGH)))/2.0;
   elsif temp_time > real(time'POS(time'HIGH)) then
     temp_time := (real(time'POS(time'HIGH)))/2.0;
   end if;
 delay_fall := (1 ps * (integer(temp_time))); -- timebase in ps
-------------------------------------------------------------------------
end  Radiation_time_delay;


PROCEDURE Radiation_drive_res(
      radiation_dose       : in  dose_record;
      drive_res            : inout  resistance;
      drive_res_postrad    : in real;
      drive_res_dose_x     : in real;
      drive_res_dose_xx    : in real) is

   variable t_dose  : real := 0.0;
   variable d_rate  : real := 0.0;
   variable drive_resistance : real :=1.0;

begin
  t_dose  := real( dose'POS(radiation_dose.dose_value));
  d_rate := (real( dose_rate'POS(radiation_dose.dose_rate_value)))*1000.0;

  drive_resistance        :=    real(    resistance'POS(drive_res))    +
(drive_res_postrad * t_dose * 1.0e-6) + (drive_res_dose_x * d_rate) +
(drive_res_dose_xx * d_rate * d_rate);

if drive_resistance > 0.0 then
```

```
  drive_res := resistance'VAL(integer(drive_resistance));
else
  drive_res := 0 ohm;
end if;

end Radiation_drive_res;


PROCEDURE Radiation_drive_cap(
      radiation_dose      : in  dose_record;
      drive_cap           : inout  capacitance;
      drive_cap_postrad   : in real;
      drive_cap_dose_x    : in real;
      drive_cap_dose_xx   : in real) is

   variable t_dose  : real := 0.0;
   variable d_rate  : real := 0.0;
   variable drive_capacitance : real :=1.0;

begin
  t_dose  := real( dose'POS(radiation_dose.dose_value));
  d_rate := (real( dose_rate'POS(radiation_dose.dose_rate_value)))*1000.0;

  drive_capacitance       :=    real(    capacitance'POS(drive_cap))    +
(drive_cap_postrad * t_dose * 1.0e-6 * 1.0e15) + (drive_cap_dose_x *
d_rate * 1.0e15) +  (drive_cap_dose_xx * d_rate * d_rate * 1.0e15);

if drive_capacitance > 0.0 then
  drive_cap := capacitance'VAL(integer(drive_capacitance));
else
  drive_cap := 0 femtof;
end if;

end Radiation_drive_cap;

END rad_tools;
------ END PACKAGE BODY rad_tools ----------------------
```

Appendix C: WIRE Cell VHDL Description

This appendix contains the complete VHDL code for the WIRE cell. This description was analyzed using the Synopsys VHDL Analyzer, Version 3.0b. Simulations were run using the Synopsys VHDL Debugger, Version 3.0b.

The VHDL description of the cell WIRE simulates the operations of the special WIRE cell which passes load information from the load gates to the driving gate. The VHDL description begins with the listing of the libraries necessary to compile and simulate the WIRE cell. Next, the "entity declaration" contains two subsections, the generic and the port declarations. Finally, the "architecture body" contains the code describing the operation of the WIRE cell.

Two libraries are called by the WIRE cell: IEEE and WORK. The IEEE library contains the VHDL nine-level logic definitions for the logical functions used in this cell. The WORK library contains the procedures and declarations necessary for the radiation-inclusive timing estimation.

The entity declaration for the VHDL description is just after the library listing. The generic declarations section contains the parameter variables necessary for accurate timing estimation. The port declarations describe the logic signals and load information passing requirements of the description. The core of the VHDL description follows the entity declaration.

The architecture body section of the VHDL description defines the operation of the WIRE cell. The connect process is the core of the VHDL description. This process

contains the operations to sum the load values and pass the result back to the driving gate.

The final function of the connect process is to pass output signals to the load gates.

```
------ CELL WIRE ------------------------------
library IEEE;
  use IEEE.STD_LOGIC_1164.all;
  use IEEE.STD_LOGIC_MISC.all;
USE WORK.rad_tools.all;

-- entity declaration --
entity WIRE is
   generic(
      output_connect_num   : Positive    := 1; -- Number of outputs
      wire_res             : resistance  := 10 ohm;
      wire_cap             : capacitance := 1 femtoF);
   port(
      radiation_dose       : in  dose_record :=  default_rad;
      A                    : in  std_ulogic;
      A_load               : out signal_load :=  default_load;
      Z                    : out std_ulogic  :=  default_signal;
      Z_load                : in  load_array (0 to output_connect_num -
1):=
                             (0   to   (output_connect_num   -   1)   =>
default_load));
end WIRE;

-- architecture body --
architecture A of WIRE is
   signal connect        : std_ulogic :=  'U';
   signal load_factor    : real := 0.0;
   signal real_cap       : real := 0.0;
   signal real_res       : real := 0.0;
   signal real_dose      : real := 0.0;
   signal real_dose_rate : real := 0.0;

begin -- architecture

   connect           <= transport To_UX01(A);

process (connect)
   variable one_over_res : real    := 0.0;
   variable sum_res      : integer := 0;
   variable sum_cap      : integer := 0;
   variable y            : real    := 0.0;
begin
--------------------SUM Resistance and Capacitance --------------------
   sum_res := 0;
   sum_cap := 0;
   y       := 0.0;
   one_over_res := 0.0;

loop_res_cap_sum:
 FOR i IN 0 to (output_connect_num - 1) LOOP
   sum_cap  :=  sum_cap  +  capacitance'POS(Z_load(i).load_cap); -- C  in
femtoF
   y:= real(resistance'POS(Z_load(i).drive_load_res)); -- resistance in
Ohms
   one_over_res := one_over_res + 1.0/y;
 END LOOP loop_res_cap_sum;
 sum_cap := sum_cap +   capacitance'POS(wire_cap);
 sum_res := integer(1.0/one_over_res) + resistance'POS(wire_res);
```

```
 if sum_res > resistance'POS(resistance'HIGH) then
   sum_res :=  resistance'POS(resistance'HIGH);
 elsif sum_res <  resistance'POS(resistance'LOW) then
   sum_res :=  resistance'POS(resistance'LOW);
 end if;

A_load.load_cap       <=  capacitance'VAL(sum_cap);
A_load.drive_load_res <= resistance'VAL(sum_res);
--------------------------------------------------------------------------
Z <= A;

end process;
end A;

configuration CFG_WIRE_A of WIRE is
   for A
   end for;
end CFG_WIRE_A;
------ END CELL WIRE ------------------------
```

Appendix D: One-Bit Full-Adder VHDL Description

This appendix contains the complete VHDL description for the full-adder shown in Figure 16. This description was analyzed using the Synopsys VHDL Analyzer, Version 3.0b. Simulations were run using the Synopsys VHDL Debugger, Version 3.0b. This description is designed to be used with the elements *IV110*, *NA210*, *NA310*, and *WIRE*. The description for *NA210* is contained in Appendix A and for *WIRE* is contained in Appendix C.

```
---- beginning of Full Adder Circuit -------------------------------
-- FILENAME      :    /user1/eng/cbrother/vhdl/proj1/full_adder.vhd
-- LIBRARY       :    cell_lib.vhd
-- DATE ENTERED  :    Mar 1993
-- REVISION      :    1.0
-- TECHNOLOGY    :    cmos
-- TIME SCALE    :    1 ps
-- NOTES         :    Timing_mesg(TRUE), Timing_xgen(FALSE),
--               :    GLITCH_HANDLE
--------------------------------------------------------------------
library IEEE;
  use IEEE.STD_LOGIC_1164.all;
  use IEEE.STD_LOGIC_MISC.all;
library IEEE_ASIC;
  use IEEE_ASIC.LIBCORE.all;
library SYNOPSYS;
  use SYNOPSYS.attributes.REAL_NAME;
  use SYNOPSYS.attributes.PRIVATE;
library RADIATION;
  use RADIATION.rad_toc_s.all;
  use RADIATION.all;
use work.all;

entity full_adder is
  generic(
      radiation_dose                : dose      := 0 rads;
      radiation_dose_rate           : dose_rate := 0 krads_s; --rads/Sec
      Timing_message                : Boolean   := True;
      Timing_exgen                  : Boolean   := False);

  port (rad_dose                    : in  dose_record :=  default_rad;
        Ain, Bin, Cin               : in  std_ulogic;
        Ain_load, Bin_load, Cin_load: out signal_load := default_load;
        sum, carry                  : out std_ulogic;
        sum_load, carry_load        : in  signal_load := default_load);
end full_adder;

architecture structural of full_adder is
```

```
component IV110
   port(
      radiation_dose       : in  dose_record :=  default_rad;
      A                    : in  std_ulogic;
      A_load               : out signal_load :=  default_load;
      Z                    : out std_ulogic  := 'U';
      Z_load               : in  signal_load :=  default_load);
end component;


component NA210
   port(
      radiation_dose        : in  dose_record :=  default_rad;
      A                     : in  std_ulogic;
      A_load                : out signal_load :=  default_load;
      B                     : in  std_ulogic;
      B_load                : out signal_load :=  default_load;
      Z                     : out std_ulogic  := 'U';
      Z_load                : in signal_load  :=  default_load);
end component;

component NA310
   port(
      radiation_dose        : in  dose_record :=  default_rad;
      A                     : in  std_ulogic;
      A_load                : out signal_load :=  default_load;
      B                     : in  std_ulogic;
      B_load                : out signal_load :=  default_load;
      C                     : in  std_ulogic;
      C_load                : out signal_load :=  default_load;
      Z                     : out std_ulogic  := 'U';
      Z_load                : in  signal_load :=  default_load);
end component;

component WIRE
   generic(
      output_connect_num   : Positive    := 1; -- Number of outputs
      wire_res             : resistance  := 10 ohm;
      wire_cap             : capacitance := 1 femtoF);
   port(
      radiation_dose       : in  dose_record :=  default_rad;
      A                    : in  std_ulogic;
      A_load               : out signal_load :=  default_load;
      Z                    : out std_ulogic  := 'U';
      Z_load               : in  load_array
               (0 to output_connect_num - 1):=
               (0 to (output_connect_num - 1) => default_load));
end component;

for all : IV110 use entity RADIATION.IV110(a);
for all : NA210 use entity RADIATION.NA210(a);
for all : NA310 use entity RADIATION.NA310(a);
for all : WIRE use entity RADIATION.WIRE(a);

signal  anot, bnot,cnot, ab_nand, bc_nand,
        ac_nand, abc_or, abc_nand, carrynot,
        carryabc, carrybit: std_ulogic;

signal  anot_load, bnot_load, cnot_load, ab_nand_load,
        bc_nand_load, ac_nand_load, abc_or_load,
        abc_nand_load, carrynot_load, carryabc_load,
        carrybit_load : signal_load := default_load;

signal  carrybit_out : std_ulogic;
```

```
signal  carrybit_out_load : load_array (0 to 1):=
                    (0 to 1 => default_load);

signal  Ain_out, Bin_out, Cin_out : std_ulogic;

signal  Ain_out_load, Bin_out_load, Cin_out_load :
         load_array (0 to 3):= (0 to 3 => default_load);

begin

     INPUTain: WIRE generic map (
                output_connect_num  => 4,
                wire_res            => 10 ohm,
                wire_cap            => 1 femtoF)
          port map( radiation_dose => rad_dose,
                    A => Ain, A_load => Ain_load,
                    Z => Ain_out, Z_load => Ain_out_load);

     INPUTbin: WIRE generic map (
                output_connect_num  => 4,
                wire_res            => 10 ohm,
                wire_cap            => 1 femtoF)
               port map( radiation_dose => rad_dose,
                         A => Bin, A_load => Bin_load,
                         Z => Bin_out, Z_load => Bin_out_load);

     INPUTcin: WIRE generic map (
                output_connect_num  => 4,
                wire_res            => 10 ohm,
                wire_cap            => 1 femtoF)
              port map( radiation_dose => rad_dose,
                        A => Cin, A_load => Cin_load,
                        Z => Cin_out, Z_load => Cin_out_load);

     NANDAB: NA210  port map ( radiation_dose => rad_dose,
                          A => Ain_out, A_load => Ain_out_load(0),
                          B => Bin_out, B_load => Bin_out_load(0),
                          Z => ab_nand, Z_load => ab_nand_load);

     NANDBC: NA210  port map ( radiation_dose => rad_dose,
                          A => Bin_out, A_load => Bin_out_load(1),
                          B => Cin_out, B_load => Cin_out_load(0),
                          Z => bc_nand, Z_load => bc_nand_load);

     NANDAC: NA210  port map ( radiation_dose => rad_dose,
                          A => Ain_out, A_load => Ain_out_load(1),
                          B => Cin_out, B_load => Cin_out_load(1),
                          Z => ac_nand, Z_load => ac_nand_load);

     NAND3CARRY: NA310  port map (radiation_dose => rad_dose,
                          A => ab_nand, A_load => ab_nand_load,
                          B => bc_nand, B_load => bc_nand_load,
                          C => ac_nand, C_load => ac_nand_load,
                          Z => carrybit, Z_load => carrybit_load);

     carrybit_out_load(0) <= carry_load;

     WIREcarrybit: WIRE generic map (
                output_connect_num  => 2,
                wire_res            => 10 ohm,
                wire_cap            => 1 femtoF)
              port map( radiation_dose => rad_dose,
                        A => carrybit, A_load => carrybit_load,
```

```
                        Z => carrybit_out, Z_load => carrybit_out_load);

    carry <= carrybit_out;

    INVCARRY: IV110  port map (radiation_dose => rad_dose,
                      A => carrybit_out, A_load =>
                                        carrybit_out_load(1),
                      Z => carrynot, Z_load => carrynot_load);

    INVA: IV110  port map ( radiation_dose => rad_dose,
                        A => Ain_out, A_load => Ain_out_load(2),
                        Z => anot, Z_load => anot_load);

    INVB: IV110  port map ( radiation_dose => rad_dose,
                        A => Bin_out, A_load => Bin_out_load(2),
                        Z => bnot, Z_load => bnot_load);

    INVC: IV110 port map ( radiation_dose => rad_dose,
                        A => Cin_out, A_load => Cin_out_load(2),
                        Z => cnot, Z_load => cnot_load);

    NAND3OR: NA310  port map ( radiation_dose => rad_dose,
                       A => anot, A_load => anot_load,
                       B => bnot, B_load => bnot_load,
                       C => cnot, C_load => cnot_load,
                       Z => abc_or, Z_load => abc_or_load);

    NAND3ABC: NA310  port map ( radiation_dose => rad_dose,
                        A => Ain_out, A_load => Ain_out_load(3),
                        B => Bin_out, B_load => Bin_out_load(3),
                        C => Cin_out, C_load => Cin_out_load(3),
                        Z => abc_nand, Z_load => abc_nand_load);

    NANDCARRY: NA210  port map ( radiation_dose => rad_dose,
                         A => carrynot, A_load => carrynot_load,
                         B => abc_or, B_load => abc_or_load,
                         Z => carryabc, Z_load => carryabc_load);

    NANDSUM: NA210  port map (radiation_dose => rad_dose,
                      A => carryabc, A_load => carryabc_load,
                      B => abc_nand, B_load => abc_nand_load,
                      Z => sum, Z_load => sum_load);

end structural;
```

Appendix E: Four-Bit Full Adder Time Delay Results

This appendix contains three tabular listings for the adder circuit time delay measurement results. The first listing contains the time delay results of the radiation-inclusive model VHDL in both the pre- and post-radiation environments. The second listing contains the timing accuracy of the radiation-inclusive model VHDL in a dose-rate radiation environment. The third listing contains the timing accuracy of the standard library VHDL in a pre-radiation environment. In all cases, the SPICE values are used as the baseline.

The first tabular listing contains the radiation-inclusive model VHDL timing error results for both pre-radiation and 1 Mrad(Si) total dose using the SPICE results as the error baseline. The error is calculated using the equation:

$$E=\frac{T_v-T_s}{T_s}\times 100\% \tag{22}$$

where:

E - Error

T_v - VHDL Delay Time

T_s - SPICE Delay Time

Delta error indicates the relative pre- to post-radiation timing performance of the radiation-inclusive model VHDL results. The delta error is calculated using the equation:

$$\Delta E=\left(\frac{(T_v(pre)-T_v(post))-(T_s(pre)-T_s(post))}{T_s(pre)-T_s(post)}\right)\times 100\% \tag{23}$$

where:

ΔE - Delta Error

$T_v(pre)$ - VHDL Delay Time pre-radiation

$T_v(post)$ - VHDL Delay Time 1 Mrad(Si)

$T_s(pre)$ - SPICE Delay Time pre-radiation

$T_s(post)$ - SPICE Delay Time 1 Mrad(Si)

Signal	Dose	SPICE(ns)	VHDL(ns)	Error	Delta Error
A1rS1r	pre-rad	0.5519	0.5660	2.6%	
	1 Mrad(Si)	0.5977	0.6180	3.4%	13.6%
B1rS1f	pre-rad	1.0018	0.9960	-0.6%	
	1 Mrad(Si)	1.0761	1.0790	0.3%	11.8%
B1fS1r	pre-rad	1.1213	1.1030	-1.6%	
	1 Mrad(Si)	1.2170	1.1900	-2.2%	-9.1%
A1fS1f	pre-rad	0.6586	0.6260	-5.0%	
	1 Mrad(Si)	0.7048	0.6700	-4.9%	-4.7%
A2rS2r	pre-rad	0.5478	0.5660	3.3%	
	1 Mrad(Si)	0.5978	0.6180	3.4%	4.0%
B1rS2f	pre-rad	1.6341	1.6350	0.1%	
	1 Mrad(Si)	1.7638	1.7780	0.8%	10.3%
B1fS2r	pre-rad	1.8467	1.8340	-0.7%	
	1 Mrad(Si)	1.9907	1.9500	-2.0%	-19.5%
A2fS2f	pre-rad	0.6586	0.6260	-5.0%	
	1 Mrad(Si)	0.7048	0.6700	-4.9%	-4.7%
A3rS3r	pre-rad	0.5478	0.5660	3.3%	
	1 Mrad(Si)	0.5978	0.6180	3.4%	4.0%
B1rS3f	pre-rad	2.2619	2.2970	1.5%	
	1 Mrad(Si)	2.4668	2.5020	1.4%	0.0%
B1fS3r	pre-rad	2.5816	2.5694	-0.5%	
	1 Mrad(Si)	2.7755	2.7400	-1.3%	-12.0%
A3fS3f	pre-rad	0.6586	0.6260	-5.0%	
	1 Mrad(Si)	0.7048	0.6700	-4.9%	-4.7%
A4rS4r	pre-rad	0.5537	0.5660	2.2%	
	1 Mrad(Si)	0.5978	0.6180	3.4%	18.0%
B1rS4f	pre-rad	2.7040	2.7260	0.8%	
	1 Mrad(Si)	2.9402	2.9730	1.1%	4.5%
B1fS4r	pre-rad	3.0766	3.0570	-0.6%	
	1 Mrad(Si)	3.2977	3.2260	-2.2%	-23.6%
A4fS4f	pre-rad	0.6586	0.6260	-5.0%	
	1 Mrad(Si)	0.7048	0.6700	-4.9%	-4.7%
B1rC4r	pre-rad	2.2742	2.3310	2.5%	
	1 Mrad(Si)	2.4980	2.5540	2.2%	-0.4%
B1fC4f	pre-rad	2.6070	2.6540	1.8%	
	1 Mrad(Si)	2.7782	2.7820	0.1%	-25.3%

Pre-Rad absolute value of the time delay error percentages.
Mean error = 2.3% Standard Deviation = 1.8%

Post-Rad 1 Mrad(Si) absolute value of the time delay error percentages.
Mean error = 2.5% Standard Deviation = 1.7%

The second tabular listing contains the radiation-inclusive model VHDL timing error results for both pre-radiation and 1 Mrad(Si) total dose.

Signal	Dose Rate	SPICE(ns)	VHDL(ns)	Error
A1rS1r	0.000E+00	0.5519	0.5660	2.6%
	0.100E+10	0.5424	0.5660	4.4%
	0.100E+11	0.5412	0.5650	4.4%
	0.100E+12	0.5297	0.5570	5.2%
	0.100E+13	0.4244	0.4960	16.9%
	0.200E+13	0.3702	0.4450	20.2%
B1rS1f	0.000E+00	1.0018	0.9960	-0.6%
	0.100E+10	0.9913	0.9960	0.5%
	0.100E+11	0.9786	0.9940	1.6%
	0.100E+12	0.9485	0.9730	2.6%
	0.100E+13	0.7615	0.8030	5.5%
	0.200E+13	0.5929	0.6610	11.5%
B1fS1r	0.000E+00	1.1213	1.1030	-1.6%
	0.100E+10	1.1237	1.1030	-1.8%
	0.100E+11	1.1209	1.0990	-2.0%
	0.100E+12	1.1246	1.0710	-4.8%
	0.100E+13	1.2724	1.1900	-6.5%
	0.200E+13	2.0908	2.0320	-2.8%
A1fS1f	0.000E+00	0.6586	0.6260	-5.0%
	0.100E+10	0.6365	0.6250	-1.8%
	0.100E+11	0.6380	0.6240	-2.2%
	0.100E+12	0.6294	0.6070	-3.6%
	0.100E+13	0.6582	0.5710	-13.2%
	0.200E+13	0.8862	0.6710	-24.3%
A2rS2r	0.000E+00	0.5478	0.5660	3.3%
	0.100E+10	0.5460	0.5660	3.7%
	0.100E+11	0.5405	0.5650	4.5%
	0.100E+12	0.5252	0.5570	6.1%
	0.100E+13	0.4354	0.4960	13.9%
	0.200E+13	0.3713	0.4450	19.8%
B1rS2f	0.000E+00	1.6341	1.6350	0.1%
	0.100E+10	1.6171	1.6350	1.1%
	0.100E+11	1.6047	1.6310	1.6%
	0.100E+12	1.5559	1.5860	1.9%
	0.100E+13	1.2282	1.2960	5.5%
	0.200E+13	0.9346	1.0810	15.7%
B1fS2r	0.000E+00	1.8467	1.8340	-0.7%
	0.100E+10	1.8889	1.8320	-3.0%
	0.100E+11	1.8653	1.8260	-2.1%
	0.100E+12	1.8735	1.7730	-5.4%
	0.100E+13	2.1176	2.0310	-4.1%
	0.200E+13	3.5007	3.7340	6.7%
A2fS2f	0.000E+00	0.6586	0.6260	-5.0%
	0.100E+10	0.6365	0.6250	-1.8%
	0.100E+11	0.6380	0.6240	-2.2%
	0.100E+12	0.6294	0.6070	-3.6%
	0.100E+13	0.6583	0.5710	-13.3%
	0.200E+13	0.9345	0.6710	-28.2%

A3rS3r	0.000E+00	0.5478	0.5660	3.3%
	0.100E+10	0.5460	0.5660	3.7%
	0.100E+11	0.5405	0.5650	4.5%
	0.100E+12	0.5252	0.5570	6.1%
	0.100E+13	0.4354	0.4960	13.9%
	0.200E+13	0.3701	0.4450	20.2%
B1rS3f	0.000E+00	2.2619	2.2970	1.5%
	0.100E+10	2.2494	2.2970	2.1%
	0.100E+11	2.2302	2.2910	2.7%
	0.100E+12	2.1643	2.2210	2.6%
	0.100E+13	1.6981	1.8020	6.1%
	0.200E+13	1.2747	1.5070	18.2%
B1fS3r	0.000E+00	2.5816	2.5694	-0.5%
	0.100E+10	2.6183	2.5910	-1.0%
	0.100E+11	2.6126	2.5820	-1.2%
	0.100E+12	2.6234	2.5030	-4.6%
	0.100E+13	2.9740	2.9140	-2.0%
	0.200E+13	4.9349	5.5390	12.2%
A3fS3f	0.000E+00	0.6586	0.6260	-5.0%
	0.100E+10	0.6365	0.6250	-1.8%
	0.100E+11	0.6380	0.6240	-2.2%
	0.100E+12	0.6294	0.6070	-3.6%
	0.100E+13	0.6583	0.5710	-13.3%
	0.200E+13	0.9371	0.6710	-28.4%
A4rS4r	0.000E+00	0.5537	0.5660	2.2%
	0.100E+10	0.5460	0.5660	3.7%
	0.100E+11	0.5404	0.5650	4.5%
	0.100E+12	0.5252	0.5570	6.1%
	0.100E+13	0.4353	0.4960	13.9%
	0.200E+13	0.3668	0.4450	21.3%
B1rS4f	0.000E+00	2.7040	2.7260	0.8%
	0.100E+10	2.6797	2.7260	1.7%
	0.100E+11	2.6509	2.7190	2.6%
	0.100E+12	2.5705	2.6340	2.5%
	0.100E+13	2.0257	2.1710	7.2%
	0.200E+13	1.5376	1.8680	21.5%
B1fS4r	0.000E+00	3.0766	3.0570	-0.6%
	0.100E+10	3.1101	3.0530	-1.8%
	0.100E+11	3.1031	3.0420	-2.0%
	0.100E+12	3.1059	2.9450	-5.2%
	0.100E+13	3.4634	3.3670	-2.8%
	0.200E+13	5.5267	6.2910	13.8%
A4fS4f	0.000E+00	0.6586	0.6260	-5.0%
	0.100E+10	0.6365	0.6250	-1.8%
	0.100E+11	0.6380	0.6240	-2.2%
	0.100E+12	0.6294	0.6070	-3.6%
	0.100E+13	0.6583	0.5710	-13.3%
	0.200E+13	0.9373	0.6710	-28.4%
B1rC4r	0.000E+00	2.2742	2.3310	2.5%
	0.100E+10	2.2582	2.3310	3.2%
	0.100E+11	2.2320	2.3240	4.1%
	0.100E+12	2.1622	2.2440	3.8%
	0.100E+13	1.6779	1.8130	8.1%
	0.200E+13	1.2353	1.5310	23.9%

B1fC4f	0.000E+00	2.6070	2.6540	1.8%
	0.100E+10	2.6526	2.6500	-0.1%
	0.100E+11	2.6493	2.6390	-0.4%
	0.100E+12	2.6553	2.5470	-4.1%
	0.100E+13	2.9825	3.0070	0.8%
	0.200E+13	4.7830	5.9600	24.6%

The dose rate absolute value of the time delay error and standard deviation percentages.

Dose Rate	Mean	Std Dev
0.000E+00	2.3%	1.7%
0.100E+10	2.2%	1.2%
0.100E+11	2.6%	1.3%
0.100E+12	4.2%	1.3%
0.100E+13	8.9%	5.0%
0.200E+13	19.0%	7.3%

The third tabular listing contains the standard model VHDL timing error results for the pre-radiation environment.

Signal	SPICE(ns)	VHDL(ns)	Error
A1rS1r	0.5519	0.8740	58.4%
B1rS1f	1.0018	1.0780	7.6%
B1fS1r	1.1213	1.0520	-6.2%
A1fS1f	0.6586	0.8370	27.1%
A2rS2r	0.5478	0.8740	59.6%
B1rS2f	1.6341	1.6020	-2.0%
B1fS2r	1.8467	1.5410	-16.6%
A2fS2f	0.6586	0.8370	27.1%
A3rS3r	0.5478	0.8740	59.6%
B1rS3f	2.2619	2.1260	-6.0%
B1fS3r	2.5816	2.0304	-21.4%
A3fS3f	0.6586	0.8370	27.1%
A4rS4r	0.5537	0.8740	57.8%
B1rS4f	2.7040	2.1260	-21.4%
B1fS4r	3.0766	2.0300	-34.0%
A4fS4f	0.6586	0.8370	27.1%
B1rC4r	2.2742	1.5560	-31.6%
B1fC4f	2.6070	1.4300	-45.1%

The standard library absolute value of the time delay error and standard deviation percentages.

Mean error = 29.7% Standard Deviation = 19.4%

Appendix F: BCD to Seven-Segment Converter Time Delay Results

This appendix contains three tabular listings for the converter circuit time delay measurement results. The first listing contains the time delay results of the radiation-inclusive model VHDL in both the pre- and post-radiation environments. The second listing contains the timing accuracy of the radiation-inclusive model VHDL in a dose-rate radiation environment. The third listing shows the timing accuracy of the standard library VHDL in a pre-radiation environment. In all cases, the SPICE values are used as the baseline.

The first tabular listing contains the radiation-inclusive model VHDL timing error results for both pre-radiation and 1 Mrad(Si) total dose using the SPICE results as the error baseline. Delta error indicates the relative pre- to post-radiation timing performance of the radiation-inclusive model VHDL results. See Appendix E for the Error and Delta Error equations.

Signal	Dose	SPICE(ns)	VHDL(ns)	Error	Delta Error
I0rO2f	pre-rad	0.6459	0.6520	1.0%	
	1 Mrad(Si)	0.6859	0.6830	-0.4%	-22.6%
I0rO3f	pre-rad	0.6067	0.6260	3.2%	
	1 Mrad(Si)	0.6338	0.6520	2.9%	-3.9%
I0rO4f	pre-rad	0.6347	0.6460	1.8%	
	1 Mrad(Si)	0.6798	0.6900	1.5%	-2.4%
I0rO5f	pre-rad	0.5297	0.5690	7.4%	
	1 Mrad(Si)	0.5538	0.5950	7.4%	7.9%
I0fO2r	pre-rad	0.7756	0.8030	3.5%	
	1 Mrad(Si)	0.8641	0.8940	3.5%	2.8%
I0fO3r	pre-rad	0.8670	0.8070	-6.9%	
	1 Mrad(Si)	0.9612	0.8990	-6.5%	-2.3%
I0fO4r	pre-rad	0.7662	0.7570	-1.2%	
	1 Mrad(Si)	0.8385	0.8230	-1.8%	-8.7%
I0fO5r	pre-rad	0.8373	0.7810	-6.7%	
	1 Mrad(Si)	0.9234	0.8680	-6.0%	1.1%
I1rO0f	pre-rad	0.7377	0.7500	1.7%	
	1 Mrad(Si)	0.7762	0.7870	1.4%	-4.0%
I1rO2r	pre-rad	0.8809	0.8820	0.2%	
	1 Mrad(Si)	0.9486	0.9510	0.3%	1.9%
I1rO3r	pre-rad	0.6446	0.6890	6.9%	
	1 Mrad(Si)	0.7030	0.7530	7.1%	9.6%

I1rO5f	pre-rad	0.3268	0.3440	5.3%	
	1 Mrad(Si)	0.3546	0.3770	6.3%	18.5%
I1rO1f	pre-rad	0.7303	0.7390	1.2%	
	1 Mrad(Si)	0.7707	0.7770	0.8%	-6.0%
I1rO4f	pre-rad	0.6750	0.7000	3.7%	
	1 Mrad(Si)	0.7151	0.7410	3.6%	2.3%
I1rO6r	pre-rad	0.5688	0.6280	10.4%	
	1 Mrad(Si)	0.6180	0.6780	9.7%	1.5%
I1fO1r	pre-rad	0.8284	0.8410	1.5%	
	1 Mrad(Si)	0.9224	0.9270	0.5%	-8.5%
I1fO4r	pre-rad	0.9616	0.8800	-8.5%	
	1 Mrad(Si)	1.0564	0.9630	-8.8%	-12.4%
I1fO6f	pre-rad	1.0321	1.0450	1.2%	
	1 Mrad(Si)	1.1342	1.1450	1.0%	-2.0%
I2rO2f	pre-rad	0.6641	0.6750	1.6%	
	1 Mrad(Si)	0.6988	0.7090	1.5%	-2.0%
I2rO3f	pre-rad	0.6186	0.6490	4.9%	
	1 Mrad(Si)	0.6494	0.6780	4.4%	-5.7%
I2fO2r	pre-rad	0.7953	0.8290	4.2%	
	1 Mrad(Si)	0.8959	0.9280	3.6%	-1.6%
I2fO3r	pre-rad	0.8935	0.8330	-6.8%	
	1 Mrad(Si)	0.9987	0.9330	-6.6%	-4.9%
I3rO6r	pre-rad	0.2652	0.2720	2.6%	
	1 Mrad(Si)	0.2858	0.2930	2.5%	1.7%
I3fO6f	pre-rad	0.5557	0.5290	-4.8%	
	1 Mrad(Si)	0.5746	0.5510	-4.1%	16.7%

Pre-Rad absolute value of the time delay error percentages.
Mean error = 4.1% Standard Deviation = 2.7%

Post-Rad 1 Mrad(Si) absolute value of the time delay error percentages.
Mean error = 3.8% Standard Deviation = 2.8%

The second tabular listing contains the radiation-inclusive model VHDL timing error results for both pre-radiation and 1 Mrad(Si) total dose.

Signal	Dose Rate	SPICE(ns)	VHDL(ns)	Error
I0rO2f	0.000E+00	0.6459	0.6520	1.0%
	0.100E+10	0.6447	0.6520	1.1%
	0.100E+11	0.6422	0.6510	1.4%
	0.100E+12	0.6352	0.6310	-0.7%
	0.100E+13	0.6234	0.5720	-8.2%
	0.200E+13	0.7057	0.6660	-5.6%
I0rO3f	0.000E+00	0.6067	0.6260	3.2%
	0.100E+10	0.6016	0.6260	4.1%
	0.100E+11	0.6020	0.6250	3.8%
	0.100E+12	0.5923	0.6080	2.7%
	0.100E+13	0.5538	0.5700	2.9%
	0.200E+13	0.5622	0.6600	17.4%
I0rO4f	0.000E+00	0.6347	0.6460	1.8%
	0.100E+10	0.6354	0.6460	1.7%
	0.100E+11	0.6314	0.6450	2.2%
	0.100E+12	0.6159	0.6320	2.6%
	0.100E+13	0.4920	0.6060	23.2%
	0.200E+13	0.3631	0.6140	69.1%

I0rO5f	0.000E+00	0.5297	0.5690	7.4%
	0.100E+10	0.5273	0.5680	7.7%
	0.100E+11	0.5262	0.5680	7.9%
	0.100E+12	0.5146	0.5500	6.9%
	0.100E+13	0.4425	0.5180	17.1%
	0.200E+13	0.4167	0.6150	47.6%
I0fO2r	0.000E+00	0.7756	0.8030	3.5%
	0.100E+10	0.7796	0.8030	3.0%
	0.100E+11	0.7734	0.8020	3.7%
	0.100E+12	0.7582	0.7880	3.9%
	0.100E+13	0.6712	0.7580	12.9%
	0.200E+13	0.5905	0.7800	32.1%
I0fO3r	0.000E+00	0.8670	0.8070	-6.9%
	0.100E+10	0.8687	0.8070	-7.1%
	0.100E+11	0.8660	0.8060	-6.9%
	0.100E+12	0.8557	0.7940	-7.2%
	0.100E+13	0.8115	0.7500	-7.6%
	0.200E+13	0.7740	0.7500	-3.1%
I0fO4r	0.000E+00	0.7662	0.7570	0.0%
	0.100E+10	0.7671	0.7570	-1.3%
	0.100E+11	0.7616	0.7550	-0.9%
	0.100E+12	0.7598	0.7370	-3.0%
	0.100E+13	0.8344	0.6810	-18.4%
	0.200E+13	1.1743	0.6670	-43.2%
I0fO5f	0.000E+00	0.8373	0.7810	-6.7%
	0.100E+10	0.8374	0.7810	-6.7%
	0.100E+11	0.8354	0.7800	-6.6%
	0.100E+12	0.8330	0.7700	-7.6%
	0.100E+13	0.8575	0.7140	-16.7%
	0.200E+13	0.9016	0.6880	-23.7%
I1rO0f	0.000E+00	0.7377	0.7500	1.7%
	0.100E+10	0.7380	0.7500	1.6%
	0.100E+11	0.7361	0.7480	1.6%
	0.100E+12	0.7256	0.7310	0.8%
	0.100E+13	0.6673	0.6930	3.8%
	0.200E+13	0.6349	0.7910	24.6%
I1rO2r	0.000E+00	0.8809	0.8820	0.1%
	0.100E+10	0.8845	0.8820	-0.3%
	0.100E+11	0.8803	0.8810	0.1%
	0.100E+12	0.8719	0.8750	0.4%
	0.100E+13	0.8215	0.8420	2.5%
	0.200E+13	0.7637	0.8220	7.6%
I1rO3r	0.000E+00	0.6446	0.6890	6.9%
	0.100E+10	0.6471	0.6890	6.5%
	0.100E+11	0.6458	0.6880	6.5%
	0.100E+12	0.6352	0.6850	7.8%
	0.100E+13	0.5757	0.6590	14.5%
	0.200E+13	0.5234	0.6490	24.0%
I1rO5f	0.000E+00	0.3268	0.3440	5.3%
	0.100E+10	0.3260	0.3440	5.5%
	0.100E+11	0.3229	0.3430	6.2%
	0.100E+12	0.3147	0.3330	5.8%
	0.100E+13	0.2654	0.3120	17.5%
	0.200E+13	0.2140	0.3040	42.1%

I1rO1f	0.000E+00	0.7303	0.7390	1.2%
	0.100E+10	0.7358	0.7380	0.3%
	0.100E+11	0.7325	0.7370	0.6%
	0.100E+12	0.7214	0.7210	-0.1%
	0.100E+13	0.6670	0.6930	3.9%
	0.200E+13	0.6590	0.8000	21.4%
I1rO4f	0.000E+00	0.6750	0.7000	3.7%
	0.100E+10	0.6801	0.7000	2.9%
	0.100E+11	0.6756	0.6990	3.5%
	0.100E+12	0.6582	0.6930	5.3%
	0.100E+13	0.5191	0.6450	24.3%
	0.200E+13	0.3512	0.6040	72.0%
I1rO6r	0.000E+00	0.5688	0.6280	10.4%
	0.100E+10	0.5732	0.6290	9.7%
	0.100E+11	0.5658	0.6290	11.2%
	0.100E+12	0.5591	0.6180	10.5%
	0.100E+13	0.4992	0.5340	7.0%
	0.200E+13	0.4472	0.4750	6.2%
I1fO1r	0.000E+00	0.8284	0.8410	1.5%
	0.100E+10	0.8344	0.8410	0.8%
	0.100E+11	0.8219	0.8400	2.2%
	0.100E+12	0.8169	0.8320	1.8%
	0.100E+13	0.7696	0.7630	-0.9%
	0.200E+13	0.7123	0.7000	-1.7%
I1fO4r	0.000E+00	0.9616	0.8800	-8.5%
	0.100E+10	0.9506	0.8790	-7.5%
	0.100E+11	0.9409	0.8780	-6.7%
	0.100E+12	0.9496	0.8600	-9.4%
	0.100E+13	1.0873	0.8110	-25.4%
	0.200E+13	1.5031	0.8960	-40.4%
I1fO6f	0.000E+00	1.0321	1.0450	1.2%
	0.100E+10	1.0380	1.0450	0.7%
	0.100E+11	1.0350	1.0420	0.7%
	0.100E+12	1.0225	1.0220	0.0%
	0.100E+13	1.0277	1.0470	1.9%
	0.200E+13	1.2418	1.5510	24.9%
I2rO2f	0.000E+00	0.6641	0.6750	1.6%
	0.100E+10	0.6599	0.6750	2.3%
	0.100E+11	0.6591	0.6740	2.3%
	0.100E+12	0.6528	0.6550	0.3%
	0.100E+13	0.6397	0.6040	-5.6%
	0.200E+13	0.7190	0.7030	-2.2%
I2rO3f	0.000E+00	0.6186	0.6490	4.9%
	0.100E+10	0.6154	0.6490	5.5%
	0.100E+11	0.6155	0.6480	5.3%
	0.100E+12	0.6081	0.6320	3.9%
	0.100E+13	0.5693	0.6020	5.7%
	0.200E+13	0.5772	0.6970	20.8%
I2fO2r	0.000E+00	0.7953	0.8290	4.2%
	0.100E+10	0.7962	0.8290	4.1%
	0.100E+11	0.7966	0.8280	3.9%
	0.100E+12	0.7793	0.8150	4.6%
	0.100E+13	0.6871	0.7760	12.9%
	0.200E+13	0.5993	0.7850	31.0%

I2fO3r	0.000E+00	0.8935	0.8330	-6.8%
	0.100E+10	0.8875	0.8330	-6.1%
	0.100E+11	0.8845	0.8320	-5.9%
	0.100E+12	0.8767	0.8210	-6.4%
	0.100E+13	0.8243	0.7680	-6.8%
	0.200E+13	0.7811	0.7550	-3.3%
I3rO6r	0.000E+00	0.2652	0.2720	2.6%
	0.100E+10	0.2656	0.2720	2.4%
	0.100E+11	0.2652	0.2720	2.6%
	0.100E+12	0.2564	0.2630	2.6%
	0.100E+13	0.2011	0.1980	-1.6%
	0.200E+13	0.1502	0.1370	-8.8%
I3fO6f	0.000E+00	0.5557	0.5290	-4.8%
	0.100E+10	0.5336	0.5290	-0.9%
	0.100E+11	0.5344	0.5290	-1.0%
	0.100E+12	0.5340	0.5190	-2.8%
	0.100E+13	0.6044	0.6440	6.5%
	0.200E+13	0.8742	1.1700	33.8%

The dose rate absolute value of the time delay error and standard deviation percentages.

Dose Rate	Mean	Std Dev
0.000E+00	4.0%	2.8%
0.100E+10	3.7%	2.8%
0.100E+11	3.9%	2.9%
0.100E+12	4.0%	3.1%
0.100E+13	10.3%	7.7%
0.200E+13	25.3%	19.9%

The third tabular listing contains the standard model VHDL timing error results for the pre-radiation environment.

Signal	SPICE(ns)	VHDL(ns)	Error
I0rO2f	0.6459	0.7880	22.0%
I0rO3f	0.6067	0.7740	27.6%
I0rO4f	0.6347	0.6750	6.3%
I0rO5f	0.5297	0.7840	48.0%
I0fO2r	0.7756	0.8150	5.1%
I0fO3r	0.8670	0.6330	-27.0%
I0fO4r	0.7662	0.6700	-12.6%
I0fO5r	0.8373	0.6700	-20.0%
I1rO0f	0.7377	0.6270	-15.0%
I1rO2r	0.8809	0.8190	-7.0%
I1rO3r	0.6446	0.7790	20.8%
I1rO5f	0.3268	0.5040	54.2%
I1rO1f	0.7303	0.6030	-17.4%
I1rO4f	0.6750	0.6590	-2.4%
I1rO6r	0.5688	0.6600	16.0%
I1fO1r	0.8284	0.6890	-16.8%
I1fO4r	0.9616	0.6330	-34.2%
I1fO6f	1.0321	1.0980	6.4%
I2rO2f	0.6641	0.8140	22.6%
I2rO3f	0.6186	0.8000	29.3%
I2fO2r	0.7953	0.8390	5.5%
I2fO3r	0.8935	0.6570	-26.5%
I3rO6r	0.2652	0.3390	27.9%
I3fO6f	0.5557	0.5820	4.7%

The standard library absolute value of the time delay error and standard deviation percentages.

Mean error = 19.8% Standard Deviation = 13.3%

Appendix G: Microwave Oven Controller Time Delay Results

This appendix contains three tabular listings for the microwave oven controller circuit time delay measurement results. The first listing contains the time delay results of the radiation-inclusive model VHDL in both the pre- and post-radiation environments. The second listing contains the timing accuracy of the radiation-inclusive model VHDL in a dose-rate radiation environment. The third listing shows the timing accuracy of the standard library VHDL in a pre-radiation environment. In all cases, the SPICE values are used as the baseline.

The first tabular listing contains the radiation-inclusive model VHDL timing error results for both pre-radiation and 1 Mrad(Si) total dose using the SPICE results as the error baseline. Delta error indicates the relative pre- to post-radiation timing performance of the radiation-inclusive model VHDL results. See Appendix E for the Error and Delta Error equations.

Signal	Dose	SPICE(ns)	VHDL(ns)	Error	Delta Error
clk88r	pre-rad	2.4405	2.4030	-1.5%	
	post-rad	2.6672	2.6230	-1.7%	-2.9%
clk88f	pre-rad	3.0131	3.0350	0.7%	
	post-rad	3.2521	3.2760	0.7%	0.8%
clkckr	pre-rad	2.8458	2.6920	-5.4%	
	post-rad	3.1021	2.9410	-5.2%	-2.8%
clkckf	pre-rad	2.0291	2.0670	1.9%	
	post-rad	2.1797	2.2380	2.7%	13.5%
clkcoor	pre-rad	2.4644	2.3540	-4.5%	
	post-rad	2.6879	2.5670	-4.5%	-4.7%
dnrcoof	pre-rad	1.0544	1.1710	11.1%	
	post-rad	1.1309	1.2580	11.2%	13.6%
dnrlddr	pre-rad	1.4911	1.4520	-2.6%	
	post-rad	1.6192	1.5780	-2.5%	-1.6%
clklddf	pre-rad	3.3073	3.3760	2.1%	
	post-rad	3.5927	3.6910	2.7%	10.4%
cook255r	pre-rad	0.7938	0.7760	0.0%	
	post-rad	0.8594	0.8330	0.0%	-13.0%
done255f	pre-rad	0.7422	0.7490	0.9%	
	post-rad	0.7950	0.8080	1.6%	11.6%
cook275r	pre-rad	1.0459	1.0190	-2.6%	
	post-rad	1.1331	1.0940	-3.4%	-14.0%

done257f	pre-rad	0.7421	0.7490	0.9%	
	post-rad	0.7950	0.8080	1.6%	11.7%

Pre-Rad absolute value of the time delay error percentages.
Mean error = 3.0% Standard Deviation = 3.0%

Post-Rad 1 Mrad(Si) absolute value of the time delay error percentages.
Mean error = 3.2% Standard Deviation = 2.9%

The second tabular listing contains the radiation-inclusive model VHDL timing error results for both pre-radiation and 1 Mrad(Si) total dose.

Signal	Dose Rate	SPICE(ns)	VHDL(ns)	Error
clk88r	0.000E+00	2.4207	2.4030	-0.7%
	0.100E+10	2.4177	2.4030	-0.6%
	0.100E+11	2.4091	2.4020	-0.3%
	0.100E+12	2.3991	2.3740	-1.0%
	0.100E+13	2.4580	2.2720	-7.6%
clk88f	0.000E+00	3.0233	3.0350	0.4%
	0.100E+10	3.0023	3.0350	1.1%
	0.100E+11	2.9947	3.0330	1.3%
	0.100E+12	2.9518	3.0000	1.6%
	0.100E+13	2.6590	2.8180	6.0%
clkckr	0.000E+00	2.8145	2.6920	-4.4%
	0.100E+10	2.8148	2.6920	-4.4%
	0.100E+11	2.8150	2.6910	-4.4%
	0.100E+12	2.8046	2.6550	-5.3%
	0.100E+13	2.8571	2.5190	-11.8%
clkckf	0.000E+00	2.0157	2.0670	2.5%
	0.100E+10	2.0122	2.0670	2.7%
	0.100E+11	2.0062	2.0640	2.9%
	0.100E+12	1.9713	2.0370	3.3%
	0.100E+13	1.8007	1.8720	4.0%
clkcoor	0.000E+00	2.4647	2.3540	-4.5%
	0.100E+10	2.4631	2.3540	-4.4%
	0.100E+11	2.4641	2.3530	-4.5%
	0.100E+12	2.4549	2.3230	-5.4%
	0.100E+13	2.5074	2.2540	-10.1%
dnrcoof	0.000E+00	1.0571	1.1710	10.8%
	0.100E+10	1.0534	1.1710	11.2%
	0.100E+11	1.0507	1.1710	11.4%
	0.100E+12	1.0280	1.1460	11.5%
	0.100E+13	0.8886	1.0100	13.7%
dnrlddr	0.000E+00	1.4912	1.4520	-2.6%
	0.100E+10	1.4852	1.4520	-2.2%
	0.100E+11	1.4817	1.4510	-2.1%
	0.100E+12	1.4688	1.4190	-3.4%
	0.100E+13	1.4396	1.2660	-12.1%

clkldf	0.000E+00	3.3070	3.3760	2.1%
	0.100E+10	3.2968	3.3760	2.4%
	0.100E+11	3.2914	3.3720	2.4%
	0.100E+12	3.2612	3.3190	1.8%
	0.100E+13	3.1530	3.3790	7.2%
cook255r	0.000E+00	0.7938	0.7760	-2.2%
	0.100E+10	0.7938	0.7760	-2.2%
	0.100E+11	0.7890	0.7750	-1.8%
	0.100E+12	0.7838	0.7510	-4.2%
	0.100E+13	0.8341	0.6920	-17.0%
done257f	0.000E+00	0.7410	0.7490	1.1%
	0.100E+10	0.7415	0.7490	1.0%
	0.100E+11	0.7390	0.7480	1.2%
	0.100E+12	0.7204	0.7300	1.3%
	0.100E+13	0.5854	0.6220	6.2%
cook275r	0.000E+00	1.0459	1.0190	-2.6%
	0.100E+10	1.0458	1.0180	-2.7%
	0.100E+11	1.0423	1.0180	-2.3%
	0.100E+12	1.0381	0.9970	-4.0%
	0.100E+13	1.0671	0.9360	-12.3%
done257f	0.000E+00	0.7410	0.7490	1.1%
	0.100E+10	0.7415	0.7490	1.0%
	0.100E+11	0.7390	0.7480	1.2%
	0.100E+12	0.7203	0.7300	1.3%
	0.100E+13	0.5854	0.6220	6.2%

The dose rate absolute value of the time delay error and standard deviation percentages.

Dose Rate	Mean	Std Dev
0.000E+00	2.9%	2.8%
0.100E+10	3.0%	2.9%
0.100E+11	3.0%	2.9%
0.100E+12	3.7%	2.9%
0.100E+13	9.5%	3.9%

The third tabular listing contains the standard model VHDL timing error results for the pre-radiation environment.

Signal	SPICE(ns)	VHDL(ns)	Error
clk88r	2.4405	2.5130	3.0%
clk88f	3.0131	3.2950	9.4%
clkckr	2.8458	2.3000	-19.2%
clkckf	2.0291	1.8900	-6.9%
clkcoor	2.4644	2.0110	-18.4%
dnrcoof	1.0544	1.2600	19.5%
dnrlddr	1.4911	1.7240	15.6%
clklddf	3.3073	2.9710	-10.2%
cook255r	0.7938	0.8940	12.6%
done257f	0.7422	0.6750	-9.0%
cook257r	1.0459	1.3510	29.2%
done257f	0.7421	0.6750	-9.0%

The standard library absolute value of the time delay error and standard deviation percentages.

Mean error = 13.5% Standard Deviation = 7.2%

Appendix H: 16-Bit Microprocessor Control Unit Time Delay Results

This appendix contains three tabular listings for the microprocessor control unit circuit time delay measurement results. The first listing contains the time delay results of the radiation-inclusive model VHDL in both the pre- and post-radiation environments. The second listing contains the timing accuracy of the radiation-inclusive model VHDL in a dose-rate radiation environment. The third listing contains the timing accuracy of the standard library VHDL in a pre-radiation environment. In all cases, the SPICE values are used as the baseline.

The first tabular listing contains the radiation-inclusive model VHDL timing error results for both pre-radiation and 1 Mrad(Si) total dose using the SPICE results as the error baseline. Delta error indicates the relative pre- to post-radiation timing performance of the radiation-inclusive model VHDL results. See Appendix E for the Error and Delta Error equations.

Signal	Dose	SPICE(ns)	VHDL(ns)	Error	Delta Error
60iplf	pre-rad	2.2497	2.3120	2.8%	
	1 Mrad(Si)	2.4197	2.5080	3.7%	15.3%
60ipmuxf	pre-rad	2.5693	2.5750	0.2%	
	1 Mrad(Si)	2.7855	2.7900	0.2%	-0.6%
60DTRf	pre-rad	3.6962	3.5900	-2.9%	
	1 Mrad(Si)	4.0036	3.8780	-3.1%	-6.3%
60ALU2f	pre-rad	3.8713	3.7740	-2.5%	
	1 Mrad(Si)	4.1767	4.0840	-2.2%	1.5%
60BIPf	pre-rad	4.6532	4.6590	0.1%	
	1 Mrad(Si)	5.0662	5.0450	-0.4%	-6.5%
60ALEf	pre-rad	4.6865	4.7260	0.8%	
	1 Mrad(Si)	5.1005	5.1260	0.5%	-3.4%
100ALU2f	pre-rad	2.2742	2.2430	-1.4%	
	1 Mrad(Si)	2.4775	2.4380	-1.6%	-4.1%
100BIPf	pre-rad	3.3155	3.4160	3.0%	
	1 Mrad(Si)	3.5990	3.6820	2.3%	-6.1%
100ALEf	pre-rad	3.2915	3.4080	3.5%	
	1 Mrad(Si)	3.5696	3.6630	2.6%	-8.3%
100RDBRf	pre-rad	2.5028	2.4590	-1.8%	
	1 Mrad(Si)	2.7107	2.6580	-1.9%	-4.3%
180irlf	pre-rad	2.0704	2.1510	3.9%	
	1 Mrad(Si)	2.2313	2.3270	4.3%	9.4%

180DTRr	pre-rad	3.8292	3.8170	-0.3%	
	1 Mrad(Si)	4.1355	4.1300	-0.1%	2.2%
180ALU3r	pre-rad	3.0934	2.9320	-5.2%	
	1 Mrad(Si)	3.3397	3.1800	-4.8%	0.7%
220iplr	pre-rad	3.0742	2.9560	-3.8%	
	1 Mrad(Si)	3.3136	3.2070	-3.2%	4.9%
220ALU3f	pre-rad	2.6909	2.8060	4.3%	
	1 Mrad(Si)	2.9257	3.0370	3.8%	-1.6%
260iplf	pre-rad	3.3732	3.3880	0.4%	
	1 Mrad(Si)	3.6787	3.6850	0.2%	-2.8%
260ipmuxf	pre-rad	2.6896	2.7560	2.5%	
	1 Mrad(Si)	2.9330	2.9830	1.7%	-6.7%
260DTRf	pre-rad	3.4890	3.5260	1.1%	
	1 Mrad(Si)	3.7918	3.8270	0.9%	-0.6%
260ALU3r	pre-rad	2.8266	2.9320	3.7%	
	1 Mrad(Si)	3.0725	3.1800	3.5%	0.9%
260ALU1r	pre-rad	2.7133	2.7900	2.8%	
	1 Mrad(Si)	2.9639	3.0360	2.4%	-1.8%
260ALU0r	pre-rad	3.1820	3.2750	2.9%	
	1 Mrad(Si)	3.4709	3.5590	2.5%	-1.7%
260BIPr	pre-rad	3.3201	3.2880	-1.0%	
	1 Mrad(Si)	3.6119	3.5800	-0.9%	0.0%
340ir21r	pre-rad	3.6323	3.5450	-2.4%	
	1 Mrad(Si)	3.9913	3.8450	-3.7%	-16.4%
380ir21f	pre-rad	2.0986	2.2100	5.3%	
	1 Mrad(Si)	2.2711	2.3790	4.7%	-2.0%

Pre-Rad absolute value of the time delay error percentages.
Mean error = 2.4% Standard Deviation = 1.5%

Post-Rad 1 Mrad(Si) absolute value of the time delay error percentages.
Mean error = 2.3% Standard Deviation = 1.5%

The second tabular listing contains the radiation-inclusive model VHDL timing error results for both pre-radiation and 1 Mrad(Si) total dose.

Signal	Dose Rate	SPICE(ns)	VHDL(ns)	Error
60iplf	0.000E+00	2.2479	2.3120	2.9%
	0.100E+10	2.2380	2.3110	3.3%
	0.100E+11	2.2357	2.3110	3.4%
	0.100E+12	2.2190	2.2730	2.4%
	0.100E+13	2.2790	2.2020	-3.4%
60ipmuxf	0.000E+00	2.5659	2.5750	0.4%
	0.100E+10	2.5591	2.5750	0.6%
	0.100E+11	2.5581	2.5750	0.7%
	0.100E+12	2.5239	2.5510	1.1%
	0.100E+13	2.3068	2.3330	1.1%
60DTRf	0.000E+00	3.6888	3.5900	-2.7%
	0.100E+10	3.6815	3.5900	-2.5%
	0.100E+11	3.6799	3.5880	-2.5%
	0.100E+12	3.6474	3.5300	-3.2%
	0.100E+13	3.8413	3.2380	-15.7%

60ALU2f	0.000E+00	3.8574	3.7740	-2.2%
	0.100E+10	3.8573	3.7740	-2.2%
	0.100E+11	3.8620	3.7730	-2.3%
	0.100E+12	3.8358	3.7400	-2.5%
	0.100E+13	3.6473	3.5340	-3.1%
60BIPf	0.000E+00	4.6706	4.6590	-0.2%
	0.100E+10	4.6469	4.6590	0.3%
	0.100E+11	4.6519	4.6600	0.2%
	0.100E+12	4.6679	4.6320	-0.8%
	0.100E+13	4.8855	4.4780	-8.3%
60ALEf	0.000E+00	4.7038	4.7260	0.5%
	0.100E+10	4.6806	4.7260	1.0%
	0.100E+11	4.6835	4.7260	0.9%
	0.100E+12	4.6954	4.6940	0.0%
	0.100E+13	4.8792	4.5570	-6.6%
100ALU2f	0.000E+00	2.2728	2.2430	-1.3%
	0.100E+10	2.2775	2.2430	-1.5%
	0.100E+11	2.2719	2.2430	-1.3%
	0.100E+12	2.2430	2.2160	-1.2%
	0.100E+13	2.1956	2.2060	0.5%
100BIPf	0.000E+00	3.3159	3.4160	3.0%
	0.100E+10	3.3131	3.4160	3.1%
	0.100E+11	3.3102	3.4130	3.1%
	0.100E+12	3.2670	3.3840	3.6%
	0.100E+13	3.1583	3.3760	6.9%
100ALEf	0.000E+00	3.2929	3.4080	3.5%
	0.100E+10	3.2909	3.4080	3.6%
	0.100E+11	3.2857	3.4040	3.6%
	0.100E+12	3.2441	3.3610	3.6%
	0.100E+13	3.2092	3.3340	3.9%
100RDBRf	0.000E+00	2.5037	2.4590	-1.8%
	0.100E+10	2.5036	2.4580	-1.8%
	0.100E+11	2.4986	2.4570	-1.7%
	0.100E+12	2.4544	2.4220	-1.3%
	0.100E+13	2.3537	2.2470	-4.5%
180irlf	0.000E+00	2.0689	2.1510	4.0%
	0.100E+10	2.0625	2.1510	4.3%
	0.100E+11	2.0572	2.1490	4.5%
	0.100E+12	2.0282	2.1300	5.0%
	0.100E+13	1.8114	1.9540	7.9%
180DTRf	0.000E+00	3.8228	3.8170	-0.2%
	0.100E+10	3.8190	3.8170	-0.1%
	0.100E+11	3.8210	3.8140	-0.2%
	0.100E+12	3.8010	3.7820	-0.5%
	0.100E+13	3.5635	3.6350	2.0%
180ALU3r	0.000E+00	3.0918	2.9320	-5.2%
	0.100E+10	3.0971	2.9320	-5.3%
	0.100E+11	3.0951	2.9310	-5.3%
	0.100E+12	3.0887	2.9100	-5.8%
	0.100E+13	3.0139	2.7570	-8.5%

220iplr	0.000E+00	3.0419	2.9560	-2.8%
	0.100E+10	3.0569	2.9550	-3.3%
	0.100E+11	3.0802	2.9550	-4.1%
	0.100E+12	3.0541	2.9150	-4.6%
	0.100E+13	2.9653	2.8250	-4.7%
220ALU3f	0.000E+00	2.6831	2.8060	4.6%
	0.100E+10	2.6860	2.8060	4.5%
	0.100E+11	2.6864	2.8060	4.5%
	0.100E+12	2.6544	2.7830	4.8%
	0.100E+13	2.4363	2.6070	7.0%
260iplf	0.000E+00	3.3701	3.3880	0.5%
	0.100E+10	3.3754	3.3880	0.4%
	0.100E+11	3.3913	3.3880	-0.1%
	0.100E+12	3.3681	3.3330	-1.0%
	0.100E+13	3.2931	3.0550	-7.2%
260ipmux	0.000E+00	2.6900	2.7560	2.5%
	0.100E+10	2.6854	2.7560	2.6%
	0.100E+11	2.6827	2.7550	2.7%
	0.100E+12	2.6531	2.7350	3.1%
	0.100E+13	2.4571	2.5890	5.4%
260DTRf	0.000E+00	3.4878	3.5260	1.1%
	0.100E+10	3.4850	3.5250	1.1%
	0.100E+11	3.4839	3.5230	1.1%
	0.100E+12	3.4848	3.4540	-0.9%
	0.100E+13	3.9978	3.2890	-17.7%
260ALU3r	0.000E+00	2.8248	2.9320	3.8%
	0.100E+10	2.8236	2.9320	3.8%
	0.100E+11	2.8243	2.9310	3.8%
	0.100E+12	2.8134	2.9100	3.4%
	0.100E+13	2.7850	2.7530	-1.1%
260ALU1r	0.000E+00	2.7100	2.7900	3.0%
	0.100E+10	2.7089	2.7900	3.0%
	0.100E+11	2.7117	2.7880	2.8%
	0.100E+12	2.6932	2.7670	2.7%
	0.100E+13	2.5990	2.6270	1.1%
260ALU0r	0.000E+00	3.1822	3.2750	2.9%
	0.100E+10	3.1902	3.2750	2.7%
	0.100E+11	3.1927	3.2740	2.5%
	0.100E+12	3.1624	3.2220	1.9%
	0.100E+13	2.9695	3.0480	2.6%
260BIPr	0.000E+00	3.3174	3.2880	-0.9%
	0.100E+10	3.3148	3.2880	-0.8%
	0.100E+11	3.3115	3.2870	-0.7%
	0.100E+12	3.2922	3.2400	-1.6%
	0.100E+13	3.2318	3.0030	-7.1%
340ir2lr	0.000E+00	3.6290	3.5450	-2.3%
	0.100E+10	3.6303	3.5450	-2.3%
	0.100E+11	3.6093	3.5460	-1.8%
	0.100E+12	3.6108	3.5030	-3.0%
	0.100E+13	3.7052	3.3220	-10.3%

380ir21f	0.000E+00	2.0993	2.2100	5.3%
	0.100E+10	2.1019	2.2090	5.1%
	0.100E+11	2.1000	2.2090	5.2%
	0.100E+12	2.0783	2.1900	5.4%
	0.100E+13	1.8680	2.1170	13.3%

The dose rate absolute value of the time delay error and standard deviation percentages.

Dose Rate	Mean	Std Dev
0.000E+00	2.4%	1.5%
0.100E+10	2.5%	1.5%
0.100E+11	2.4%	1.6%
0.100E+12	2.6%	1.7%
0.100E+13	6.3%	4.5%

The third tabular listing contains the standard model VHDL timing error results for the pre-radiation environment.

Signal	SPICE(ns)	VHDL(ns)	Error
60iplf	2.2497	2.2240	-1.1%
60ipmuxf	2.5693	2.1910	-14.7%
60DTRf	3.6962	3.2460	-12.2%
60ALU2f	3.8713	3.2240	-16.7%
60BIPf	4.6532	2.6800	-42.4%
60ALEf	4.6865	2.8330	-39.6%
100ALU2f	2.2742	2.0490	-9.9%
100BIPf	3.3155	3.0480	-8.1%
100ALEf	3.2915	3.1050	-5.7%
100RDBRf	2.5028	2.2740	-9.1%
180irlf	2.0704	1.7570	-15.1%
180DTRr	3.8292	2.7250	-28.8%
180ALU3r	3.0934	1.9740	-36.2%
220iplr	3.0742	2.7290	-11.2%
220ALU3f	2.6909	2.3950	-11.0%
260iplf	3.3732	2.7840	-17.5%
260ipmuxf	2.6896	2.3540	-12.5%
260DTRf	3.4890	2.8960	-17.0%
260ALU3r	2.8266	2.2660	-19.8%
260ALU1r	2.7133	2.4090	-11.2%
260ALU0r	3.1820	2.7900	-12.3%
260BIPr	3.3201	2.5800	-22.3%
340ir21r	3.6323	2.2290	-38.6%
380ir21f	2.0986	1.9110	-8.9%

The standard library absolute value of the time delay error and standard deviation percentages.

Mean error = 17.6% Standard Deviation = 11.4%

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Vita

Captain Charles P. Brothers, Jr. was born 10 April 1958 in Portland, Oregon. He graduated from high school in Bend, Oregon in 1976. He then served in United States Air Force as a Precision Measurements Equipment Specialist until 1980, when Sergeant Brothers received an honorable discharge. He received a B.S.E.E. with honors in 1985 from Portland State University, Portland, Oregon . Reentering the Air Force, he received a commission through the Officer Training School in October 1985. He served as a project engineer, Peacekeeper Guidance and Control, Ballistic Missile Office, Norton AFB, CA from October 1985 through May 1989. While stationed at Norton AFB, he attended the University of Southern California and received a M.S. in Systems Management in 1987. He entered the School of Engineering, Air Force Institute of Technology in May 1989, completing a M.S.E.E. in December 1990. He then began a Ph.D program at the Air Force Institute of Technology. In 1992 he received his candidacy.

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March 1994 Doctoral Dissertation

RAPID AND ACCURATE TIMING SIMULATION OF RADIATION-HARDENED DIGITAL MICROELECTRONICS USING VHDL

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This dissertation presents the development of a fast, accurate, timing simulation capability based on VHSIC Hardware Description Language (VHDL) without the use of back annotation of timing delay information. This VHDL-based timing simulator is intended for use with radiation-hardened microelectronics in simulating timing of circuit operation in pre-radiation, post-radiation (1 Mrad(Si) total dose), and ionizing dose radiation environments. Development of the timing models are presented. The implementation of the timing models are incorporated into a VHDL library composed of basic logic gates and flip-flops. Simulations of complex circuits were run in SPICE and VHDL to assess the timing accuracy and simulation run time of the VHDL-based timing simulator versus SPICE. Results of the simulations are presented. Final evaluation of the simulator included testing of a microprocessor control unit. In all cases, the VHDL-based simulation ran over two orders of magnitude faster than the equivalent SPICE simulation. In the pre- and post-radiation environment, accuracy estimates are usually within five percent and never exceed 12 percent. Worst-case timing estimate errors increase above 15 percent for dose rates above 1.0×10^{11} rads(Si) per second. This VHDL-based timing simulator represents an improvement over SPICE in the ability to quickly simulate complex circuits.

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CMOS Logic Simulation, Logic Circuit Simulation, Radiation-hardened Microelectronics, Transient Radiation Effects, VHDL

Unclassified Unclassified Unclassified UL