QUARTERLY REPORT NO. 14
FOR
ANALOG-TO-DIGITAL CONVERTER
CONTRACT NO. N00014-87-C-0314
1 July 1991—30 September 1991

ARPA Order Number:	7356
Program Code Number:	7220
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Name of Contractor:	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655936, M.S. 105 Dallas, Texas 75265
Effective Date of Contract:	30 March 1987
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Contract Number:	N00014-87-C-0314
Program Manager:	W.R. Wisseman (214) 995-2451
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Short Title of Work:	GaAs A-to-D Converter
Contract Period Covered by Report:	1 July 1991—30 September 1991

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I. SUMMARY

A. Brief Program Definition

This is a research and development program to design and fabricate both a GaAs high sampling rate analog-to-digital converter (ADC) and a high-resolution GaAs ADC.

B. ADC Program Overview

The p-channel JFET process has been shown to meet the breakdown voltage requirements as well as the drain saturation current control requirements for the 12-bit ADC. The JFET output impedance is still somewhat less than the required 20 kohms, which may impact ultimate ADC accuracy but is sufficiently high to be compatible with a functional 12-bit ADC.

The 12-bit ADC mask set is scheduled to be released in October 1991 with fabrication to begin in November.

II. PROGRESS REPORT

A. Process Development

The modified p-channel JFET process demonstrated breakdown voltages greater than 9 volts, which meets the minimum specification of 8 volts. The modified process used a thicker n-collector epitaxial layer in which the JFETs are fabricated. Varying the epitaxial thickness from 0.6 μm to 1.3 μm resulted in the minimum gate-drain breakdown voltage varying from ~9 volts to greater than 14 volts. A thickness of 1 μm is scheduled to be used for the 12-bit ADC design.

Figure 1 illustrates the impact of the p-channel JFET channel implant dosage on the resulting saturation currents for a 40-μm-wide PJFET. The uniformity of I_{dss} across a chip is a key parameter. Figure 2 illustrates the variation in I_{dss} for an array of nine supposedly identical PJFETs from a given die. These data are illustrated for several different wafers, each using a different channel implant dose. It can be seen that the uniformity is better than 5% within a given chip, which is sufficient for 12-bit operation.

The solution to the problem of PJFET output impedance being less than 20 kohms, as illustrated in the I-V characteristics shown in Figure 3, was not obtained because of time and funding limitations. The lower output impedance will limit the accuracy of the ADC but should be sufficient to demonstrate a fully functional 12-bit ADC.

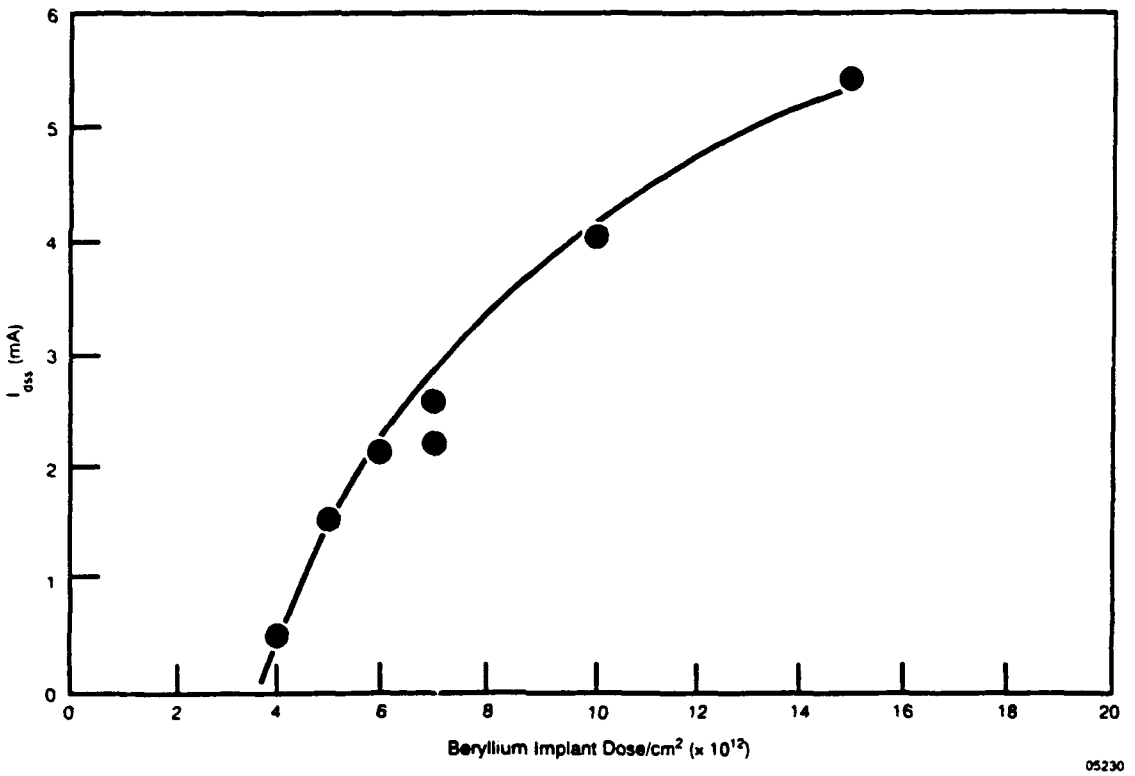


Figure 1. I_{dss} versus channel implant dose for 40-μm/2.5-μm p-channel JFET.

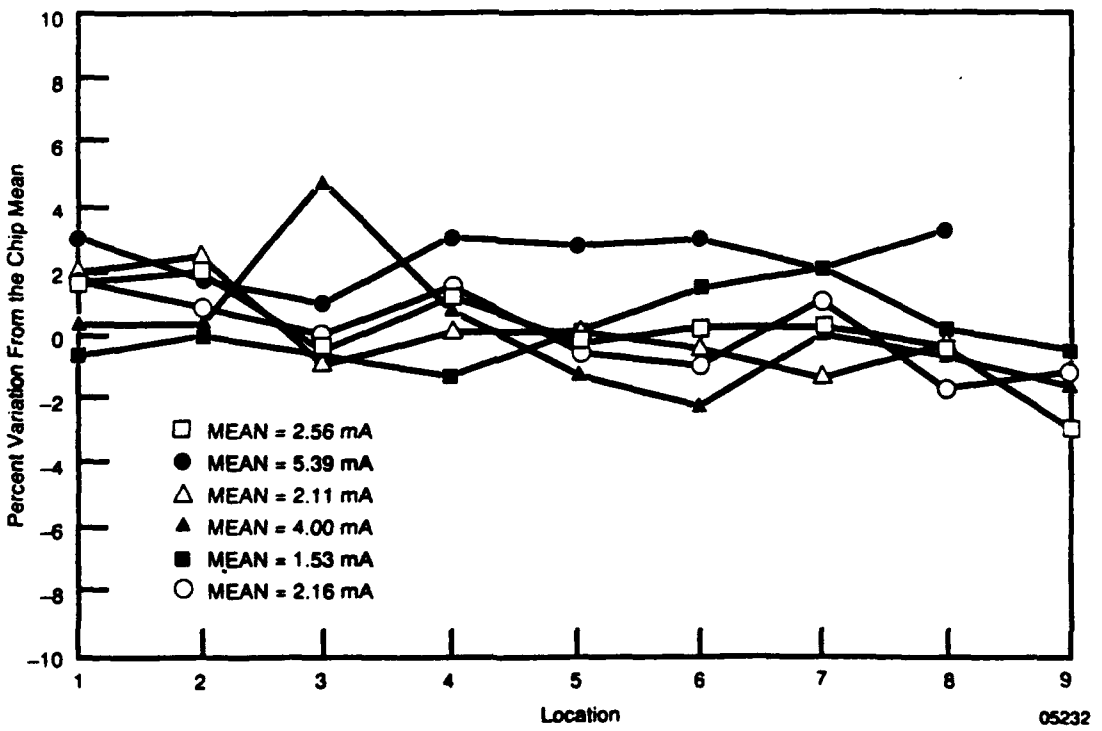
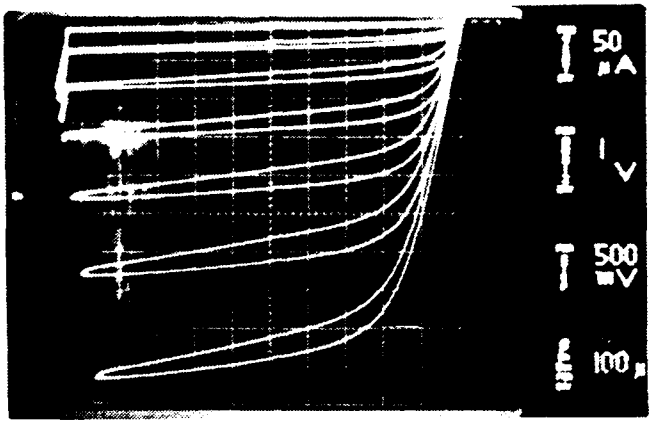
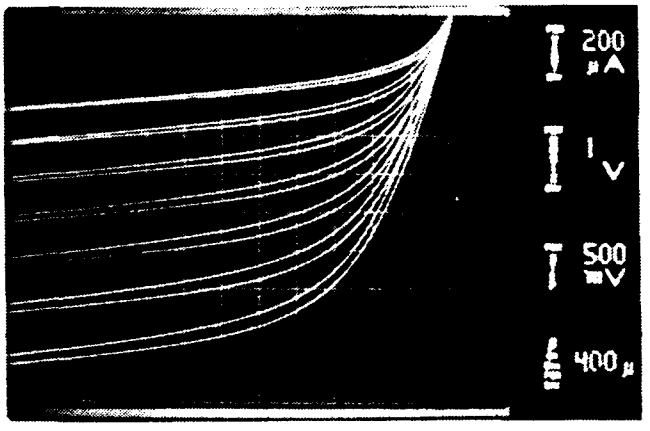


Figure 2. I_{dss} percent deviations from the local mean SWR 271.



(a) Be^+ Implant $4 \times 10^{12}/cm^2$



(b) $5 \times 10^{12}/cm^2$

Figure 3. PJFET I-Vcharacteristics.

B. Circuit Design/Testing

Hughes has made significant progress in the design and layout capture of the 12-bit ADC. Layout of the 12-bit ADC core IC is approximately 90% complete, while layout of the timing-and-control IC is 100% complete. Layout of the sample-and-hold, 5-bit quantizer, gain-switched residue amplifier, 8-bit digital-to-analog converter (DAC), error correction circuitry, and timing-and-control circuitry are complete and in final layout verification. Hughes began overall interconnection and power supply routing of the 12-bit circuit subelements. They are still on schedule and within the cost-to-complete spending plan. Hughes expects to release the 12-bit ADC for fabrication in October.

TI provided an updated p-channel JFET layout to Hughes, and Hughes has rebuilt their JFET device library based on the new device. Impact on the layout of the 12-bit ADC was minimal since the new device is design-rule compatible with the older version.

C. **Personnel Assignments**

There have been no changes in personnel.

IV. PLANS FOR NEXT QUARTER

Release the 12-bit ADC mask set and begin fabrication in the GaAs pilot line.

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