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Data Processing Units for Eight Magnetospheric Particle and Field Sensors

Prepared by

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Engineering and Technoloogy Group

THE AEROSPACE CORPORATION El Segundo, California

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This report has been reviewed by the Public Affairs Office (PAS) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nationals.

This technical report has been reviewed and is approved for publication. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

ROBERT D. MULLANY, Capt, USAF CHIEF, FEWS PAYLOADS DIVISION

GILBERT T. TAKAHASHI DIRECTOR, SPACE SEGMENT

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PREFACE

The authors wish to thank J. Bernard Blake, David L. Chennette, Joseph F. Fennell, Donald T. Katsuda, Patricia H. Lew, Dan J. Mabry, Michael T. Marra, and Walter J. Wong for their valuable contributions to the design, fabrication, and testing of the DPUs.

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Data Processing Units for Eight Magnetospheric Particle and Field Sensors

Rokutaro Koga,* Sam S. Imamoto,† Norman Katz,† and Steven D. Pinkerton; The Aerospace Corporation, Los Angeles, California 90009

The DPUA, DPUB, and DPU57 data processing units associated with eight CRRES particle and field experiments are described. Operation of the experiments is controlled by the data processing units (DPUs), which constitute the interface between the spacecraft and the sensors subserving the individual experiments. All data to and from the sensors pass through the associated DPUs. Each DPU consists of a microprocessor, power supply, signal handler, and various peripherals such as input/output buffers and specialized data processing hardware. In addition to experiment control and data processing functions, the DPU software performs such tasks as loading the system software from ROM into RAM, writing the memory-resident look-up tables aulized by the DPU hardware, checking the system RAMs for memory retention faults, outputing system memory to the telemetry stream, and outputing a fixed pattern of telemetry. To maximize the available telemetry bandwidth, much of the raw sensor data is analyzed by the DPUs using various onboard processing schemes and then compressed prior to being output in telemetry.

Introduction

W E have designed, built, and calibrated three data processing units (DPUs) for AFGL-701 experiments onboard combined release and radiation effects satellite (CR-RES). The DPUs are known as DPUA, DPUB, and DPU57, these units interface with one, two, and five sensors, respectively (see Table 1). Each DPU receives ground commands and timing pulses from the spacecraft; distributes power to the sensor(s); controls the experiment via sensor instructions; reads and compresses data from the sensor(s); and outputs the compressed data to telemetry. Two of the DPUs, namely DPUA and DPUB, also perform onboard processing of the sensor data. All data to and from the sensors pass through the associated data processing unit. The DPU is thus an integral part of the experiment.

Each DPU weighs about 5 lb 11 oz, measures $3 \times 8 \times 10$ in., and consumes approximately 260 mA at 28 V. The three DPUs are stacked together to form a large cubical structure.

DPUA is described in detail in the following section. Since the DPUs are designed to be very similar functionally, much of this description applies equally to DPUB and DPU57. Differences between these two DPUs and DPUA are discussed in a subsequent section. The DPU software and data compression schemes are described in the final sections.

DPUA

As shown in Fig. 1, DPUA consists of a computer, peripheral sections such as various input/output (I/O) buffers and the MICS event processor, a power supply, and an analog signal handler. All parts are biased at 6.8 V except the PROMs, which are biased at 5.0 V. The computer consists of a microprocessor (SANDIA 1802), control logic, and memory (12 K bytes of PROM and 16 Kbytes of RAM). The radiation-hardened 1802 microprocessor operates with a 1.6 MHz clock, and communicates with the various peripheral sections via address, data, and control buses (A, D, and C in Fig. 1).

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There are two groups of DPUA peripheral sections: one which interfaces with the spacecraft, and a second which interfaces with the MICS sensor. The first group includes the timer and Sun signal receiver (DPUA TIMER AND SUN in Fig. 1), the ground command handler (GROUND COM-MAND BUFFER), and the telemetry handler (OUTPUT TE-LEMETRY BUFFER). The functions of these sections are described in Table 2. Signals between the spacecraft and these sections pass through individual I/O interface signal conditioners. The second group of peripheral sections interfaces with the sensor via additional interface signal conditioners. This group includes the step instruction controlling the MICS high-voltage power supply (E/Q STEP), the HVPS step controlling the post acceleration high-voltage power supply (not shown), the MICS command instruction along with the clock (SENSOR INSTRUCTION AND CLOCK), the event data line from the sensor (EVENT DATA), and various analog monitor signals from MICS (ANALOG MONITORS). These sections also are described in Table 2.

An additional group of peripheral sections functions as the MICS event processor (EVENT PROCESSOR-see the area inside the dashed lines in Fig. 1), which analyzes MICS sensor data semiautonomously after initial preparation (table writing by the computer) has been performed. The MICS sensor generates energy E and time-of-flight T values for each event. In the event processor, the E and T values, along with the E/Qstep value, are used to classify the event into one of several mass M and mass per charge-state (M/Q) groups. This classification is performed by the hardware-based successive approximation routine (SAR), which utilizes look-up tables written by the DPU under software control. The values in these tables represent overlayed polynomial curves in E vs T (or E/Q vs T) parameter space, such that adjacent polynomials define the upper and lower bounds of a mass (or M/Q) group. Table values are calculated using coefficients stored in DPU memory. The default coefficients are derived from polynomial fits to extensive calibration data; new sets of coefficients can also be uplinked to DPUA using ground commands.

The assigned M and M/Q values for an event are used to address one scaler in a 512-element matrix of scalers (M vs M/Q in Fig. 1). DPUA also contains eight rate scalers (RATE SCALERS) in which events with special combinations of Mand M/Q are accumulated. The rate scaler select table (SCALER SELECT) determines which combinations of Mand M/Q are accumulated by the individual rate scalers. Sample direct events (E and associated T values) are collected from

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Fig. 1 DPUA functional block diagram.

Table 1 DPUs and associated sensors			
DPU	Associated sensors		
DPUA	Magnetospheric ion composition spectrometer (MICS, aka AFGL-701-11A)		
DPUB	 a) Low-energy magnetospheric ion composition sensor (LOMICS) b) Heavy ion telescope (HIT) [The combined LOMICS/HIT system is known as AFGL-701-11B] 		
DPU57	 a) Medium-energy electron sensor A (MEA, aka AFGL-701-5A) b) Medium-energy electron sensor B (MEB, aka AFGL-701-5B) c) Relativistic proton detector and photometers (RP, aka AFGL-701-7A) d) Proton switch 1 (PS1, aka AFGL-701-7B1) c) Reston switch 2 (PS2, aka AFGL-701-7B1) c) Reston switch 2 (PS2, aka AFGL-701-7B1) 		

the sensor and stored in the event buffer (DIRECT EVENT BUFFER). Direct events are selected according to a priority scheme determined using DPUA's event priority table (PRI-ORITY). The contents of the various scalers and the direct event buffer are read out periodically by the computer, processed (e.g., compressed), and then placed in the telemetry stream.

The throughput of DPUAs MICS event processor is about 3×10^4 events/s (35 µs/event for processing), which exceeds the maximum MICS event rate of about 2×10^4 events/s. Hence, there is no bottleneck in accepting events at the DPU, even for very high event rates.

The DPUA software is stored in power-strobed 4 K \times 8 PROMs (Raytheon 29673) of the highly power consuming T²L logic family because of the difficulty in obtaining radiationhardened low-power PROMs. Shortly after the DPU is turned on, the contents of the PROMs are copied to low-power RAMs, power to the PROMs is shut off, and thereafter the software executes exclusively in RAM. The 1802 microprocessor has a 64 K address space: locations 0000-3FFF (hex) are assigned to PROM (3000-3FFF are not used, however); locations 4000 - 7FFF are assigned to RAM; the remainder of the address space is allocated to DPUAs MICS event processor.

DPUB and DPU57

DPUB and DPU57 are very similar to DPUA in both design and function, hence much of the above description of DPUA is also applicable to these units. In this section, significant differences between these two processing units and DPUA are highlighted.

DPUB

DPUB interfaces with two instruments, LOMICS and HIT (see Table 1). The event processor section of this DPU must therefore analyze data from both these sensors, as shown in Fig. 2.

Events detected by LOMICS are specified by a 5-bit energy per charge-state (E/Q) value, a 2-bit detector (polar angle) identifier (ID), and a 10-bit time-of-flight T value. The timeof-flight and E/Q values are used by the event processor to classify the event into one of up to 32 mass per charge-state (M/Q) groups, based on a look-up table written previously to DPUB memory under software control. The event processor then increments one of six LOMICS rate scalers according to the values of ID and M/Q. These scalers are read and reset every 128 ms by the DPUB software, which compresses and places the data in the telemetry stream. A 128-element matrix scaler is used to accumulate event counts with finer ID vs M/Qresolution over a longer (16.384 s) period. Direct events, specified by E/Q, T, ID, and M/Q, may also be telemetered individually, but only after the DPU has been instructed to do so via a ground command.

The DPUB interface with the HIT sensor is functionally quite similar. Event data from HIT consist of 8-bit energy (E), 10-bit time-of-flight (T), and 5-bit energy-loss-rate (dE) values. The first two of these values (E and T) are used by the event processor to classify the event into one of up to 16 mass (M) groups, based on a memory resident look-up table. The derived M value and the five most significant bits of E are used to select one of twelve HIT rate scalers to increment. The HIT rate scalers are read and reset every 512 ms by the DPUB software, which places the data in the telemetry stream following compression. A 512-element matrix scaler accut. ulates event counts with finer M vs E resolution over a longer (65.536 s) period. HIT direct events, consisting of E, T, dE, and Mvalues, are also telemetered individually on a first-in basis, or

Table 2	DPUA	hardware	peripheral	sections
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Peripheral section	Signal flow	Description
DPUA TIMER	Spacecraft to DPUA	Various internal DPUA clock pulses are derived from the 16-kHz pulses provided by the spacecraft.
SUN	Spacecraft to DPUA	Sun detection signal.
GROUND COMMAND/ GATED CLOCK	Spacecraft to DPUA	Ground command and command clock (1.6 kHz). 16 bits/cmd; MSB first.
TELEMETRY BUFFER	DPUA to spacecraft	Telemetry data: Four 8-bit words per TM frame with the 109-kHz clock; MSB first.
ANALOG MONITORS	MICS to DPUA	Various analog monitors. Digitized by ADCs within DPUA.
EVENT DATA	MICS to DPUA	Singles rates and housekeeping data sent by MICS when requested by DPUA via sensor instructions. 128 bits/set of data, sent twice each 256 ms format period; MSB first.
MICS EVENT PROCESSOR	MICS to DPUA	MICS events are processed in this semiautonomous area of DPUA.
SENSOR INSTRUCTION	DPUA to MICS	16-bit command instruction sent to MICS twice each 256 ms format period; MSB first. (The eight MSBs contain the coded instruction.)
E/Q STEP	DPUA to MICS	ESA high-voltage step command (5 bits) sent to MICS once each 256 ms format period.
HVPS STEP	DPUA to MICS	Postacceleration high-voltage step command (3 bits) sent to MICS periodically.

according to a modifiable prioritization scheme determined by DPUBs event priority table.

DPUB also collects raw data from the sensors in the form of diagnostic rate scalers (START and STOP counts, etc.), digitized analog quantities (ESA voltage and housekeeping data), and HIT ID scalers which give a coarse ion group characterization based on front (dE) and back (E) surface barrier HIT sensor outputs.

DPU57

DPU57 interfaces with five sensors as shown in Fig. 3 (see also Table 1). One group of DPU57 peripheral sections interfaces with the spacecraft as described previously for DPUA, while a second group interfaces with the various sensors via additional interface signal conditioners. This group includes the MEB PHA selection instruction sent to MEB by DPU57 (MEB PHA SELECT), Lockheed scaler data from the AFGL-701-5,7 instruments (LOCKHEED SCALERS), electron and proton PHA data from MEB (E PHA and P PHA), and various analog monitors (DPU/SENSOR HK MONITOR).

Data Processed by DPUA, DPUB, and DPU57

A summary of the data processed by the three DPUs including data formats and accumulation periods, is provided in Table 3. The compression schemes used by the DPUs are described in the following.

DPU Software

The software for each DPU consists of the following six routines:

- 1) SYSM ROM to RAM transfer program
- 2) SYSR RAM integrity check program
- 3) SYSX Memory dump program
- 4) SYSQ Fixed telemetry pattern program

5) SYST Table calculation program (not used in DPU57)

6) SYSD Data collection and dissemination program

A summary of these program sections is given in the following; the flow of control among program sections is illustrated in Fig. 4.

Shortly after power-up, the DPU microprocessor begins executing the memory transfer routine (SYSM) stored at ROM location 0000. SYSM copies the contents of the ROMs (i.e., the DPU software) to RAM, then jumps to the RAM integrity check routine (SYSR), which executes in RAM. Power to the ROMs is then shut off and thereafter the DPU software executes exclusively in RAM. The SYSR routine cycles through system RAM performing a read/write/read test of memory integrity, recording the locations of any errors in the SYSR RAM check error table. After SYSR has completed, program control is automatically transferred to the data accumulation and dissemination routine (SYSD).

In SYSD, data are collected from the sensor, compressed, and telemetered to the ground. SYSD also controls the sensors and accepts ground commands. There are two distinct telemetry modes in SYSD for DPUA and DPUB: Normal mode in which preprocessed sensor related data are output, and Special Test mode in which raw direct event data replace much of the scaler (counter) data telemetered in normal mode. Unless a memory load (M/L) ground command is received instructing the DPU to execute one of the auxiliary routines (SYST, SYSX, SYSR, or SYSQ), the processor will remain in the SYSD routine indefinitely. After completion of SYST, SYSX, or SYSR, program control is automatically returned to SYSD (SYSQ never returns).

The SYST table calculation routine (DPUA and DPUB only) is used to write the mass group, M/Q group, and event priority/rate scaler select tables, based on coefficients stored in memory. Many of the data telemetered by SYSD make sense only after these tables have been written. The SYST routine may be executed by sending the DPU the proper M/L ground command.

Memory load ground commands can also be used to instruct the DPU to execute the memory dump routine (SYSX). In SYSX, normal telemetry data are replaced by the contents of a section of system memory. Eight separate SYSX M/Lground commands are provided to select different sections of the system memory.

The fixed telemetry routine (SYSQ) can by executed by sending the DPU the appropriate M/L ground command. SYSQ outputs a (nearly) fixed pattern of telemetry data, and may be used to check the telemetry link from the DPU to the ground receiving station. Unlike SYST, SYSX, and SYSR, SYSQ executes indefinitely and does not return to SYSD. To return to SYSD from SYSQ, it is necessary either to shut down the DPUs power and restart, or to reset the DPU using the (hardware-processed) cold start command.

As noted earlier, the initialization routine (SYSM) automatically passes program control to the SYSR RAM integrity check routine, which then jumps to SYSD upon completion. However, SYSR may also be executed directly from SYSD by uplinking the appropriate M/L ground command to the DPU. The integrity of the system RAMs may thereby be checked in-flight at regular intervals.

It may occasionally be necessary to force the DPU to execute the ROM to RAM transfer routine (SYSM). This may be accomplished in either of two ways: 1) By turning the main power off and then back on; or 2) by sending the cold start command to the DPU (unlike M/L ground commands, this command is processed directly by the DPU hardware without



a) HIT Mode



b) LOMICS Mode

Fig. 2 DPUB functional block diagram.

software involvement). The two methods differ in that SYSM always performs the memory transfer in response to the cold start command, whereas on power-up RAM is reloaded from ROM only when a comparison indicates that the contents of the two sections of memory differ. (The contents of the RAMs are maintained by a standby power supply even when the main power is off, hence it may be unnecessary to perform the transfer in the latter case.)

SYSD Scaler Compression Routines

The SYSD data processing routine uses two software-based compression schemes to compress scalers to approximately one-half or two-thirds of their precompression lengths (in bits), without significantly reducing resolution. Most telemetered values are compressed using the 19- to 8-bit compression scheme, the sole exception being the MEA outputs which are compressed by DPU57 via the 16- to 12-bit scheme.

1) 19- to 8-bit Compression: The first of the two onboard compression routines compresses scalers of up to 19 bits to 8-bit words. The compressed 8-bit word has the form XY (hex) where X is a 4-bit exponent formed by subtracting four from the number of significant bits in the original (precompression) word, and Y is a 4-bit mantissa formed from the five most significant bits of the original word by dropping the most

significant bit (which is "1" by definition). For example, the 19-bit data word 100 1100 0000 0000 0000 (311,296 decimal) would be compressed to F3 (hex), that is, to an exponent of 19 - 4 = 15 (F hex) and a mantissa of 0011 (3 hex). In the special case that the scaler to be compressed occupies five or fewer bits (i.e., X < 2), no loss in precision is incurred through compression: The precompression value equals $V = 2^{X-1} + \frac{1}{2}$ $2^{\chi-3}$ exactly. For example, 11001 (25 decimal) would be compressed to 10 (hex) and subsequently reconstructed as $9 \cdot 2^0 + 2^4 = 25$. However, when $X \ge 2$, each postcompression value XY corresponds to a range of precompression values. In particular, any value in the inclusive range $(Y \cdot 2^{X-1} + 2^{X-3})$ $(Y \cdot 2^{X-1} + 2^{X-3} + 2^{X-1} - 1)$ is compressed to XY. The nominal precompression value corresponding to XY may therefore be taken to be the midpoint of this interval, $2^{X-1} \cdot (Y+16.5) = 0.5$. For example, any scaler in the inclusive range 311,296 -327,679 (decimal) would be compressed to XY = F3 (hex), so that the compressed value F3 corresponds to a nominal value of 319,487.5. In any case, the error introduced by the 19- to 8-bit compression routine is less than $\pm 3.1\%$.

2) 16- to 12-bit compression: The second routine compresses scalers of up to 16 bits to 12-bit words, with a worst case error of less than 0.1%. Suppose the precompression scaler is $b_{15}b_{14}$



Fig. 3 DPU57 functional block diagram.

Table 3 Data entities processed by SYSD^a

DPUA		Type	Acc. Period
MS0-MS511	MICS matrix scalers	19 - 8	49.152 5
R0-R7	MICS rate scalers	16 - 8	192 ms
c	MICS event data	16 - 8	192 ms
Ē, T	MICS direct event	16 - 8	32 ms
DPU HSK	DPUA/sensor housekeeping data	8-bit DA	1.024 ms
DPUB			
MS0-MS127	LOMICS matrix scalers	19 - 8	16.384 5
LR0-LR5	LOMICS rate scalers	16 - 8	128 ms
LSO-LS5	LOMICS diagnostic scalers	16 - 8	128 ms
E/Q, T	LOMICS direct events	Event	32 ms
MS0-MS511	HIT matrix scalers	19 - 8	65.536 s
HR0-HR11	HIT rate scalers	16 - 8	512 ms
HS0-HS5	HIT diagnostic scalers	16 - 8	512 ms
D <i>E, T</i>	HIT direct events	Event	32 ms
HID0-HID11	HIT ID scalers	16 - 8	512 ms
HSK	DPUB/sensor housekeeping data	8-bit DA	512 ms
DPU57b			
MEA0-MEA17	MEA rate scalers	16 - 12	512 ms
IDE0-IDE9	MEB electron detector integral scalers	16 - 8	512 ms
E0-E13	MEB electron detector PHA scalers	16 - 8	256 ms
IDP0-IDP3	MEB proton detector integral scalers	16 - 8	512 ms
P0-P11	MEB proton detector PHA scalers	16 - 8	512 ms
PBKGND	MEB proton detector background scalers	16 - 8	512 ms
PCOINC	MEB proton detector coincidence scalers	16 - 8	512 ms
CA0-CA3	Alcohol radiator cerenkov rate scalers (RP)	19 - 8	1.024 ms
CS0-CS3	Fused-silica radiator cerenkov rate scalers (RP)	19 - 8	1.024 ms
RE0-RE3	Electron scatter detector rate scalers (RP)	19 - 8	2.048 ms
RM0-RM3	Minimum-ionizing detector rate scalers (RP)	19 - 8	2.048 ms
рно-рнз	Photometer rate scalers (RP)	16 - 8	256 ms
PS U,L (1,2)	Proton switch upper and lower rate scalers	19 - 8	4.096 ms
DPU HSK	DPU57/sensor housekeeping data	8-bit DA	1.024 ms

*The data types are as follows:

19 - 8: 19-bit scalers compressed to 8 bits.

16 - 8: 16-bit scalers compressed to 8 bits.

16 - 12: 16-bit scalers compressed to 12 bits.

8-bit DA: 8-bit digitized analog data. Event: Uncompressed event data.

bIDE0 and IDE6 (DPU57) have a 256-ms accumulation period.

The MICS event data (DPUA) consists of FSR (front singles rate), DCR (double coincidence rate), TCR (triple coincidence rate), MSS (M solid state detector pulse rate), P (proton event rate), and ALPHA (alpha particle event rate).



Fig. 4 Flow of control among DPU program sections.

 $\cdots \dot{v}_1 \ b_0$ and let $n \le 15$ be such that $b_n = 1$ and $b_k = 0$ for k > n, so that the scaler looks like: $0 \cdots 0 \ 1 \ b_{n-1} \ b_{n-2} \cdots b_1 \ b_0$. If $n \le 8$, then the postcompression value is obtained by simply eliminating the four highest order zeros (e.g., 0000 0001 1111 1111 $\rightarrow 0001 \ 1111 \ 1111$). On the other hand, when n > 8, the precompression value is first shifted M = n - 9 bits to the right, so that at most ten significant bits remain, and then the three highest order bits of this 12-bit value (which are 001 by definition) are replaced by the binary encoding of M + 1. No loss in precision is incurred for precompression values with fewer than 11 significant bits (i.e., the precompression value is given exactly by the postcompression value). For values with 11 or more significant bits (i.e., M > 0), the nominal precompression value corresponding to the compressed value $d_{11} d_{10} d_9 \cdots d_0$ is $N = 2^{X-1} \cdot (Y + 512.5) - 0.5$, where $X = d_{11} d_{10} d_9$ (= M + 1) and $Y = d_8 \cdots d_0$.

Summary

The DPUA DPUB, and DPU57 data processing units play essential roles in the eight CRRES experiments listed previously in Table 1. The DPUs are responsible for controlling the experiments, and for collecting, processing, and outputing sensor data to telemetry. The telemetry bandwidth required to downlink the sensor data is significantly reduced via onboard analysis and subsequent compression of raw sensor data, as described previously.

More detailed descriptions of the DPUs and associated experiments may be found in the following handbooks, which are available from the principal author: 1) CRRES AFGL-701-11A (DPUA/MICS) Experimentor's Handbook; 2) CR-RES AFGL-701-11B (DPUB/HMSB) Experimentor's Handbook; and 3) CRRES AFGL-701-5,7 (DPU57) Experimentor's Handbook.