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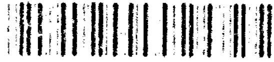

Gate-All-Around Device

Final technical report (RHD-04)

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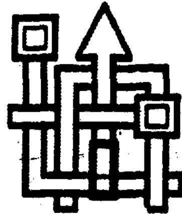

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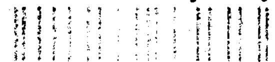

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The gate-all-around device is an SOI MOS field-effect transistor. The gate electrode and the thin gate oxide are wrapped around the active channel region. No other insulator (field oxide or buried oxide) is in contact with the active region of the device. The gate-all-around device exhibits a high transconductance (up to 4 times that of a normal SOI transistor), an ideally sharp subthreshold slope, and demonstrates the concept of volume inversion in thin SOI films. Both n-channel and p-channel devices have been fabricated.

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1. Description of the problem

SOI MOSFETs are known for their potential for application in circuits operating in harsh environments and have been shown to exhibit superior performances in high-temperature and ionizing environments. The resistance of SOI devices to alpha particle and heavy ion impact (SEU) is inversely proportional to the volume of silicon in which the device is made, *i.e.* inversely proportional to the thickness of the SOI layer. The same dependence on film thickness is expected for gamma-dot phenomena, for the same reasons[1].

The problem preventing one from utilizing thin-film, fully depleted devices for rad-hard applications is the poor total dose immunity of thin-film devices.[2] Indeed, as charges accumulate in the buried oxide layer upon irradiation, several problems do arise: at first, front threshold voltage shifts appear, due to the coupling between front and back gate depletion zones, and secondly, back-channel leakage appears as the back oxide charge density becomes too high.

The effect of total dose on the device properties depends on the thickness of the oxide in contact with the silicon. A much larger amount of oxide charges are generated in a SIMOX buried oxide, for instance, than in the gate oxide. The charge generated, ΔQ_{ox}, is roughly proportional to the oxide thickness. In addition, the threshold shift generated by oxide charges, ΔV_{th}, is also proportional to the oxide thickness. In consequence, back threshold voltage shift is roughly proportional to the square of the oxide thickness ($\Delta V_{th} \cong \frac{\Delta Q_{ox}\, t_{ox}}{\varepsilon_{ox}}$, with $\Delta Q_{ox} \cong t_{ox}$). The accumulation of charges in the buried oxide induces a shift of the front-side threshold voltage as well because of the electrical coupling present between the front and the back gate in thin-film fully depleted devices. An obvious way of minimizing the effects of total-dose exposure is to reduce the thickness of the oxide layers surrounding the active silicon. Unfortunately, no practical means have been found as yet to produce thin, gate-quality buried oxides. Buried oxides have typical thicknesses of 400 nm or 1 µm, when produced by the SIMOX or ZMR techniques, respectively.

2. The Gate-All-Around Device

The solution proposed by the gate-all-around device consists in surrounding the whole active area of the transistor with thin, gate-quality oxide. This gate oxide is itself surrounded by the polysilicon gate electrode, which provides ground potential when the device is turned OFF.

The work performed last year (see the first annual technical report (RHD-02)) has resulted in the publication of several scientific articles, one of which in association with the NRL, Washington D.C., and DNA, Alexandria, VA. These publications are:

---

1 J.P. Colinge, Silicon-On-Insulator Technology: Materials to VLSI, Kluwer Academic Publishers, p. 178, 1991

2 D.C. Mayer, "Modes of operation and radiation sensitivity of ultrathin SOI transistors", Proceedings of the IEEE SOS/SOI Technology Conference, pp. 52-53, 1989

"Silicon-on-insulator gate-all-around device", J.P. Colinge, M.H. Gao, A. Romano, H. Maes, and C. Claeys, Proc. IEEE SOS/SOI Technology Conf., p. 137, Oct. 1990

"Silicon-on-insulator gate-all-around device", J.P. Colinge, M.H. Gao, A. Romano, H. Maes, and C. Claeys, IEDM, P. 595, 1990

"Radiation effects in gate-all-around structures", R.K. Lawrence, J.P. Colinge, H.L. Hughes, and G.E. Davis, Proceedings IEEE International SOI Conference, 1991, p. 80

"An analytical model for GAA transistors", A. Terao and F. Van de Wiele, Microelectronic Engineering 15, (1991), pp. 233-236

"Characteristics of nMOS/GAA transistors near threshold", P. Francis, A. Terao, D. Flandre and F. Van de Wiele, paper accepted for ESSDERC (European Solid-State Research Conference), 1992

"High temperature characteristics of GAA/SOI transistors and circuits", P. Francis, A. Terao and D. Flandre, submitted to the IEEE International SOI Conference, 1992

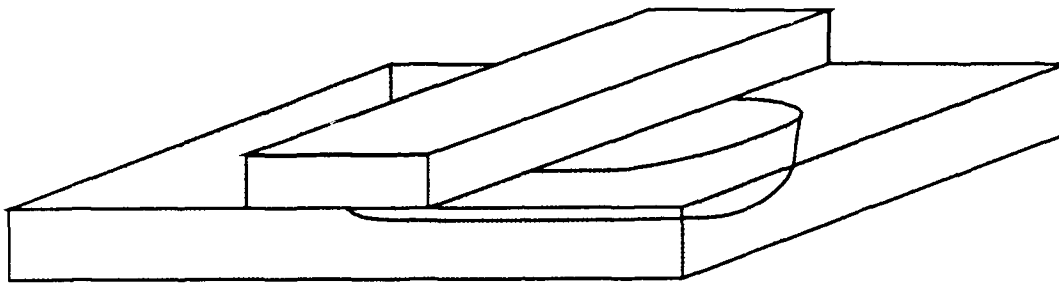
"Low-frequency behaviour of GAA SOI transistors", E. Simoen, U. Magnusson, C. Claeys, and J.P. Colinge, submitted to the IEEE International SOI Conference, 1992

3. Process Description

3.1. N-channel devices

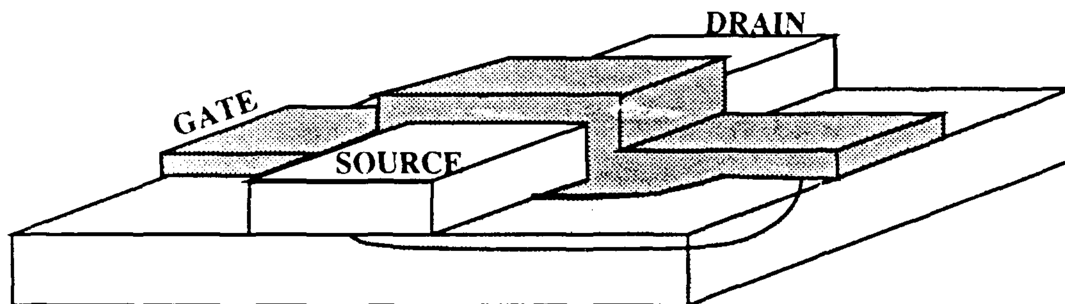
The process starts with standard SIMOX wafers. The thickness of the starting silicon film is 180 nm . A 60 nm-thick pad oxide is grown, and a 200 nm-thick film of silicon nitride is deposited. A mask step is used to pattern the nitride as well as the silicon film in a dry etch reactor. Using the nitride as a mask, 600 nm of oxide are grown on the edge of the silicon island. Such an oxidation as for consequence to smooth the edges of the silicon island and has been reported to be useful to improve gate oxide breakdown properties.[3] The nitride and the pad oxide are then wet etched, and a second masking step is used to define areas where the underlying oxide (as well as the edge oxide) will be etched. Etching of the buried silicon leaves a beam (bridge) of silicon free-standing over a cavity (Figure below) The silicon bridge is supported at both ends by the original buried oxide. The free-standing part of the silicon island will later on become the active part of the device (the channel region), while those parts still supported by the underlying oxide will become the source and the drain.

[3] M. Haond *et al*, "Gate oxide breakdown behaviour in a mesa SOI CMOS process", Proceedings of the IEEE SOS/SOI Technology Conference, pp. 68-69, 1989



Gate-All-Around device after etching of a cavity underneath the silicon island

A thick thermal gate oxide is then grown at 850°C in dry oxygen. Its thickness is either 50 nm (in one split) or 30 nm (in another split). Boron is there implanted to adjust threshold voltage. A 450 nm-thick polysilicon film is the deposited in a LPCVD furnace at a temperature of 620°C. Because of the excellent conformal deposition of LPCVD polysilicon, gate material is deposited not only at the top of the device, but also in the cavity below the silicon bridge. Polysilicon is, hence, deposited all around the gate oxide which itself is grown all around the channel region of the silicon island (hence the name: Gate-All-Around Device.) The polysilicon film is then implanted with phosphorous ions, and a long (4 hours) annealing step is used to diffuse the phosphorous everywhere in the polysilicon, even underneath the silicon bridge, where no ions are implanted. The polysilicon is then etched using a mask step to define the gate, after which phosphorous is implanted to form self-aligned sources and drains (Figure below) After source and drain anneal, low temperature oxide is deposited, and contact hole are etched. A standard metallization step completes the process. Care is taken not to use steps at temperatures higher than 800°C after the gate oxide has been grown.



Gate-All-Around device after source and drain formation

3.2. P-channel devices

The process starts with standard SIMOX wafers. The thickness of the starting silicon film is 180 nm . A 60 nm-thick pad oxide is grown, and a 200 nm-thick film of silicon nitride is deposited. A mask step is used to pattern the nitride as well as the silicon film in a dry etch reactor. Using the nitride as a mask, 600 nm of oxide are grown on the edge of the silicon island. Such an oxidation as for consequence to smooth the edges of the silicon island and has been reported to be useful to improve gate oxide breakdown properties. The nitride and the pad oxide are then wet etched, and a second masking step is used to define areas where the underlying oxide (as well as the edge oxide) will be etched. Etching of the buried silicon leaves a beam (bridge) of silicon free-standing over a cavity.The silicon bridge is supported at both ends by the original buried oxide. The free-standing part of the silicon island will later on become the active part of the device (the channel region), while those parts still supported by the underlying oxide will become the source and the drain. A thick thermal gate oxide is then grown at 850°C in dry oxygen. Its thickness is 50 nm . Boron is there implanted to adjust threshold voltage. A 450 nm-thick polysilicon film is the deposited in a LPCVD furnace at a temperature of 620°C. Because of the excellent conformal deposition of LPCVD polysilicon, gate material is deposited not only at the top of the device, but also in the cavity below the silicon bridge. Polysilicon is, hence, deposited all around the gate oxide which itself is grown all around the channel region of the silicon island (hence the name: Gate-All-Around Device.) The polysilicon film is then implanted with phosphorous ions, and a long (4 hours) annealing step is used to diffuse the phosphorous everywhere in the polysilicon, even underneath the silicon bridge, where no ions are implanted. The polysilicon is then etched using a mask step to define the gate, after which phosphorous is implanted to form self-aligned sources and drains. After source and drain anneal, low temperature oxide is deposited, and contact hole are etched. A standard metallization step completes the process. Care is taken not to use steps at temperatures higher than 800°C after the gate oxide has been grown.

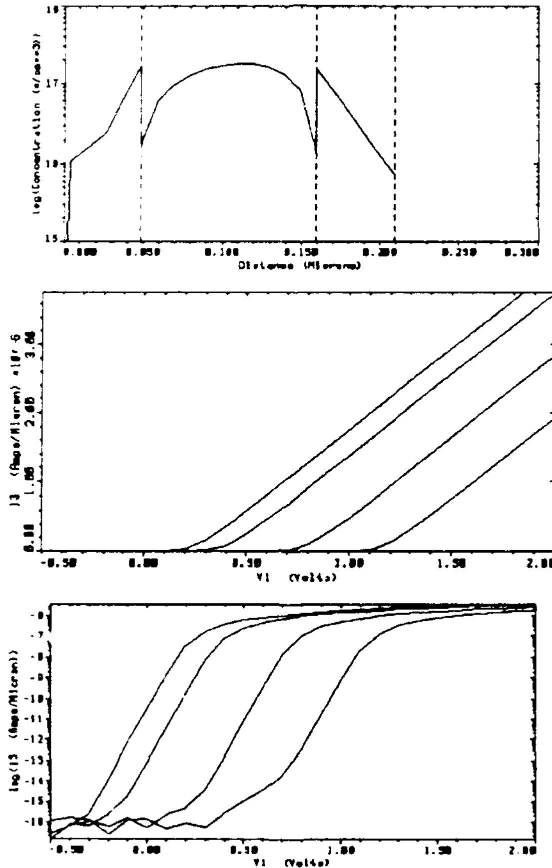
A lithography with minimum feature size of 3 μm was used for the process. Similar devices were made without etching a cavity underneath the silicon island. These devices are thus classical SOI MOSFETs, and can be used for comparing the electrical properties of Gate-All-Around devices and classical SOI MOSFETs, both before and after exposure to ionizing radiations.

The next page presents the SUPREM-III simulation files used to model the Gate-All-Around fabrication process as well as the result of PISCES-IIb simulation of the device behaviour.

3.3. Process simulation for the GAA device

```
title gaa 180 nm n-ch
init oxide thick=.05 dx=.1 spaces=50
deposit silicon <100> thick=0.18
diffusion time=85 temp=1000 dryo2
print layers
deposit nitride thick=.2
diffusion time=400 temp=1000 weto2
etch oxide.th
etch nitride
etch oxide.th
diffusion temp=850 time=660 dryo2
print layers
etch oxide.th
diffusion temp=850 time=660 dryo2
implant boron energy=30 dose=8,10,15,20e11
diffusion temp=800 time=240
diffusion temp=820 time=300
print layers
savefile file=supn1.out device
plot chemical phosphorus top=1e18 bottom=1e15 y.logar right=0.3
+ device=regis
plot chemical boron add pause
stop
```

n-ch, 3μm, 180nm, tox=50nm, GAA



Suprem simulation of the impurity profile (top) and Pisces simulation of the n-channel devices (middle and bottom top). The Suprem input file is listed above.

3.4. Process flow chart

Macro Step Description			WAFER		
	7	8	9	10	11
SIMOX=S, BULK P-CH=P, NCH=N, TEST=T	S	S	S	S	S
Get 10 SIMOX wafers from JP Colinge	x	x	x	x	x
Get 5 bulk wafers, p-type <100>, 10-25 ohm.cm					
Get 5 bulk wafers, n-type <100>, 4-6 ohm.cm					
Label SIMOX wafers with numbers 7 to 16	x	x	x	x	x
Label p-type bulk wafers wafers with numbers 1 to 3, and 17 and 19					
Label n-type bulk wafers wafers with numbers 4 to 6, and 18 and 20					
Measure thickness of SIMOX wafers with UV/vis reflectance	x	x	x	x	x
grow 100 nm of oxide	x	x	x	x	x
strip oxide in BHF	x	x	x	x	x
Measure thickness of SIMOX wafers with UV/vis reflectance	x	x	x	x	x
grow 31 nm of oxide	x	x	x	x	x
strip oxide in BHF					
Measure thickness of SIMOX wafers with UV/vis reflectance					
Pad oxidation: grow 30 nm, dry oxygen, 1000C					
Measure pad oxide thickness on wafers 22 to 25					
Deposit 200nm nitride	x	x	x	x	x
Measure nitride thickness					
*** Litho: active area *** Canon exposure, develop, hardbake	x	x	x	x	x
Plasma etch 200nm of nitride	x	x	x	x	x
Etch 30nm pad oxide in BHF (dewetting on bulk)	x	x	x	x	x
Wet/dry resist strip	x	x	x	x	x
*** Litho: n-channel mask *** Canon, develop, hardbake					
Field implant: Boron, 50 keV, 4e14	x	x	x	x	
Wet/dry resist strip					
anneal in N2, 950C, 90 min	x	x	x	x	
0.13 μm trench etch in silicon (stop on oxide)	x	x	x	x	x
Field oxidation: grow 400nm steam 1000C	x	x	x	x	x
Field oxidation: grow 600nm steam 1000C					
Inspect field oxidation	x	x	x	x	x
Wet etch oxide on nitride (20 sec BHF)	x	x	x	x	x
Wet etch 200nm nitride	x	x	x	x	x
Wet etch 30nm pad oxide	x	x	x	x	x
Implant phosphorus 100keV 1 e11					
Gate oxidation: 50 nm @ 850 C, steam					
implant boron 25 keV 1e11					
*** Litho: n-channel mask *** Canon, develop, hardbake					
Implant boron 170 keV 1e12					
implant boron 60 keV 2.5e11					
implant boron 60 keV 3e11					
Strip resist					

Step					
*** Litho: ETCH mask *** Canon, develop, hardbake	x	x	x	x	x
Oxide etch in BHF by JPC	x	x	x	x	x
resist strip (NO ULTRASOUNDS!!!)	x	x	x	x	x
Gate oxidation: 30 nm @ 850 C, steam	x				
Gate oxidation: 50 nm @ 850 C, steam		x	x	x	x
Measure gate oxide thickness					
implant boron 25 keV 1.5e12		x			
implant boron 25 keV 2e12			x		
implant boron 25 keV 2.5e12	x			x	
implant phosphorus 60 keV 1e11					x
implant boron 30 keV 6e11					
implant boron 30 keV 8e11					
implant boron 30 keV 1e12					
deposit polysilicon, thickness=450nm	x	x	x	x	x
measure polysilicon thickness					
implant phosphorus 50 keV, 1e16	x	x	x	x	x
annealing: 45 min @ 800 C in N2					
annealing: 240 min @ 800 C in N2	x	x	x	x	x
Etch native oxide on poly in HF (dewetting)	x	x	x	x	x
measure polysilicon sheet resistivity					
*** Litho: poly gate mask mask *** Canon, develop, hardbake	x	x	x	x	x
Polysilicon plasma etch (thickness=450nm)	x	x	x	x	x
strip resist (NO ULTRASOUNDS!!!)	x	x	x	x	x
measure remaining oxide thickness (on source & drain)					
thin S&D oxide to 20 nm in HF 2%	x	x	x	x	x
*** Litho: n-channel mask *** Canon, develop, hardbake					
implant phosphorus 70 keV 4e15	x	x	x	x	
strip resist					
*** Litho: p-channel mask *** Canon, develop, hardbake					
implant boron 25 keV 4e15					x
resist strip					
S&D anneal:180 min @ 800 C in N2	x	x	x	x	x
deposit 600 nm undoped TEOS	x	x	x	x	x
densify 30 min @ 800C in O2					
*** Litho: contact holes mask *** Canon, develop, hardbake	x	x	x	x	x
etch oxide in BHF; note time to dewetting					
wet etching contact holes in BHF	x	x	x	x	x
strip resist (NO ULTRASOUNDS!!!)	x	x	x	x	x
Al/Si sputtering: thickness=1 μm	x	x	x	x	x
*** Litho: metallization mask *** Canon, develop, hardbake	x	x	x	x	x
Plasma etch metal + inspection	x	x	x	x	x
resist strip in microstrip	x	x	x	x	x
sintering 3 wafers forming gas 420C + call JPC	x				
sintering forming gas 420C + call JPC	x	x	x	x	x
END	x	x	x	x	x

Process flow for the GAA device

The detailed process is given in **ANNEX I**

3.5. Process splits

As can be seen in the process flow, all devices were realized in thin-film SOI (contrarily to the devices in the first annual technical report (RHD-02)), where both thick-film and thin-film devices were made).

- Wafers 8, 9 and 10 contain n-channel devices, and the gate oxide thickness is 50 nm (500 Å).

- Wafer 7 contains n-channel devices, and the gate oxide thickness is 30 nm (300 Å).

- Wafers 11 contains p-channel devices, and the gate oxide thickness is 50 nm (500 Å).

Wafer ID	7	8	9	10	11
gate oxide thickness	30 nm	50 nm	50 nm	50 nm	50 nm
N or P channel	N	N	N	N	P

Process splits

4. Device results

All wafers yielded devices with the expected characteristics. The yield, when the devices were probed at the wafer level, was almost 100%.

The electrical characteristics of the GAA devices from the second run (one set of curves for each split) are reported in **ANNEX II**.

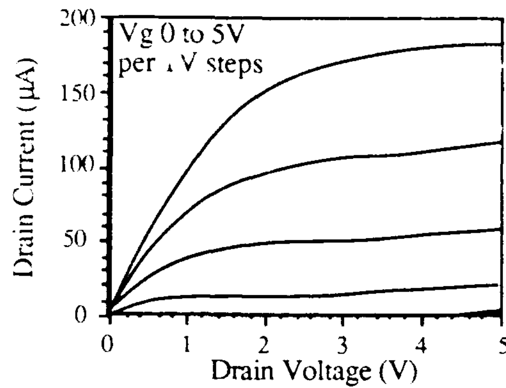
These characteristics are:

- $I_D(V_G)$ for V_{DS} = 100 mV, with both linear and logarithmic vertical scales (top left Figure)
- $I_D(V_{DS})$ for V_G = 0 to 5 volts, (bottom left Figure)
- Transconductance (g_m) at V_{DS} = 100 mV, as a function of gate voltage (bottom right Figure)

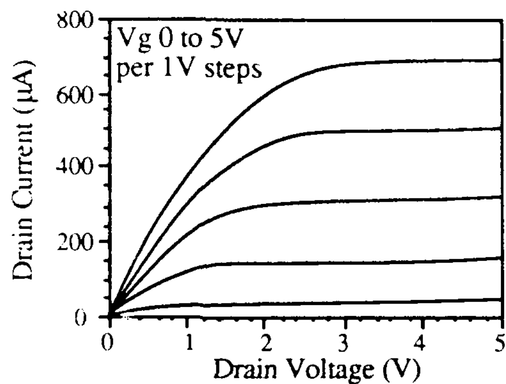
All observations made previously (see the first annual technical report (RHD-02)) about the sharp subthreshold slope, the high transconductance and the volume inversion phenomenon are still holding for the present devices. The novelties of the devices from the second run (compared to the previous fabrication run) are the presence of a thinner gate oxide (30 nm), and that of p-channel devices. The particularities of the GAA device physics (from report RHD-02) are recalled in Section 4.1 below.

4.1 Device physics

The two Figures below present the output characteristics of a conventional n-channel SOI MOSFET and a gate-all-around n-channel device. The final silicon thickness of the conventional device is 125 nm, while the thickness of the GAA device is 100 nm (the GAA device is thinner because gate oxide was grown on both front and back interfaces of the silicon film). The SOI MOSFET is partially depleted. Both devices have the same (drawn) physical dimensions (W/L=3µm/3µm), but, because of the presence of two channels (at the top and bottom of the silicon film), the effective width of the GAA device is 6 µm.



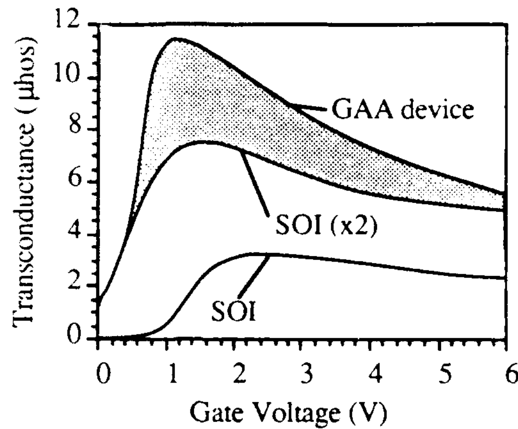
Output characteristics of a "normal" n-channel SOI MOSFET. $(W/L)_{mask}$=3μm/3μm.



Output characteristics of an n-channel GAA device. $(W/L)_{mask}$=3μm/3μm.

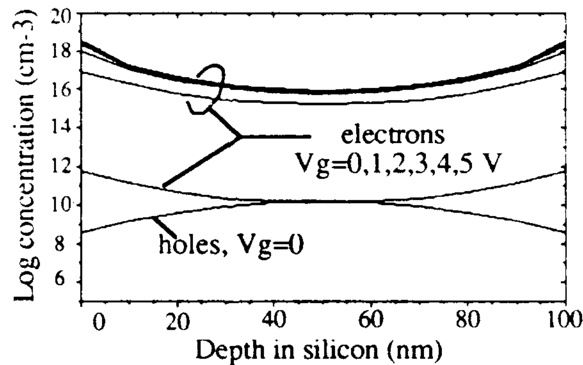
It can be observed that the current drive is much higher in the GAA device than in the SOI transistor. The increased drive is, of course, partly due to the larger effective width (6 μm instead of 3 μm) and to the lower threshold voltage (V_{th} is lower in the GAA device (0.45 V) than in the SOI MOSFET (1.2 V) because of the thinner silicon film and because of the interaction between the top and bottom depletion zones). But another effect has to be taken into consideration to fully account for the increased drive. This effect is called "volume inversion".[4] It can clearly be observed in the Figure below where the transconductance of a conventional device and that of a GAA device are compared. An additional curve labelled "SOI x 2" presents the transconductance of the SOI MOSFET multiplied by two and shifted to the left by the difference of threshold voltages ($V_{th,SOI}$ - $V_{th,GAA}$) to account for both the presence of two channels and the lower threshold voltage of the GAA device. The grey area represents the extra drive of the GAA device, which is attributed to volume inversion.

4 F. Balestra *et al.*, IEEE Electron Device Letters, Vol. 8, p. 410, 1987



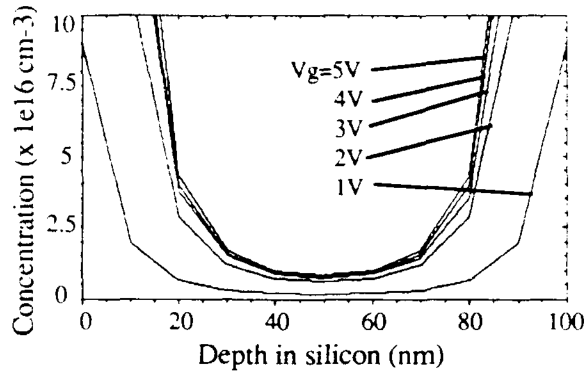
Transconductance (dI_d/dV_G) at Vds=100 mV in a conventional SOI MOSFET and a GAA device. $(W/L)_{mask}$ = 3μm / 3μm.

The Figure below shows that the electron concentration at all depths in the silicon film is much larger than the hole concentration, for all positive gate voltages. The contribution of volume inversion is more pronounced right above threshold, where the inversion layer is distributed across the entire silicon film and where the effects of bulk mobility (in contrast to surface mobility) can be felt.



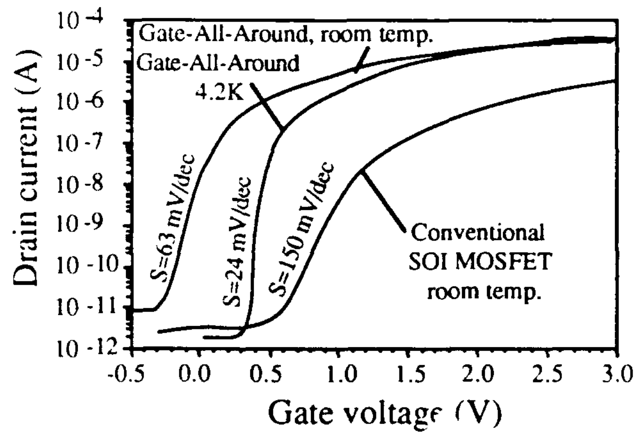
Carrier distribution as a function of depth in silicon for different gate voltages.

At higher gate voltages, there is still inversion in the centre of the silicon film, but the carriers are now mostly localized in inversion layers near the interfaces. As a result, more scattering occurs, and the transconductance tends to be equal to twice that of that a conventional device.



Electron concentration as a function of depth in silicon for different gate voltages.

Because of the excellent coupling between the surface potentials and the gate voltage, a subthreshold slope of 63 mV/decade is obtained at room temperature (vs. 150 mV/decade in the conventional, partially depleted SOI device). Device measurements were carried at liquid helium temperature (4.2 K) as well. As it was the case at room temperature, no kink is observed in the output characteristics, and the output characteristics are flat (high output impedance). At 4.2 K the subthreshold slope is equal to 24 mV/decade and the threshold voltage is 1.1 V (*vs.* 0.45 V at room temperature).

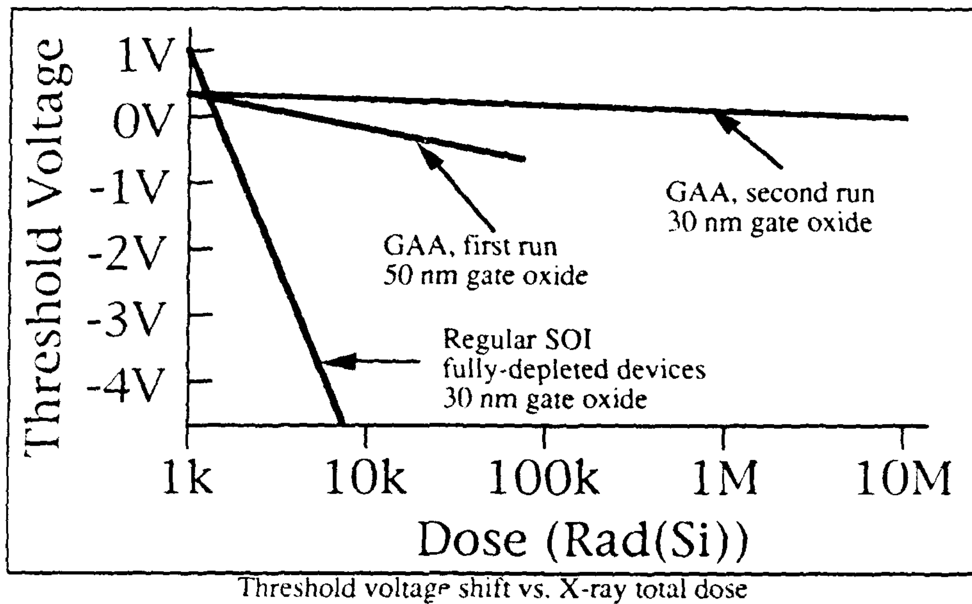


Log of current as a function of gate voltage (V_{DS}=100 mV).

The layout of the chip used for device fabrication and the dimensions of the different devices are reported in **ANNEX III**.

5. Irradiation results

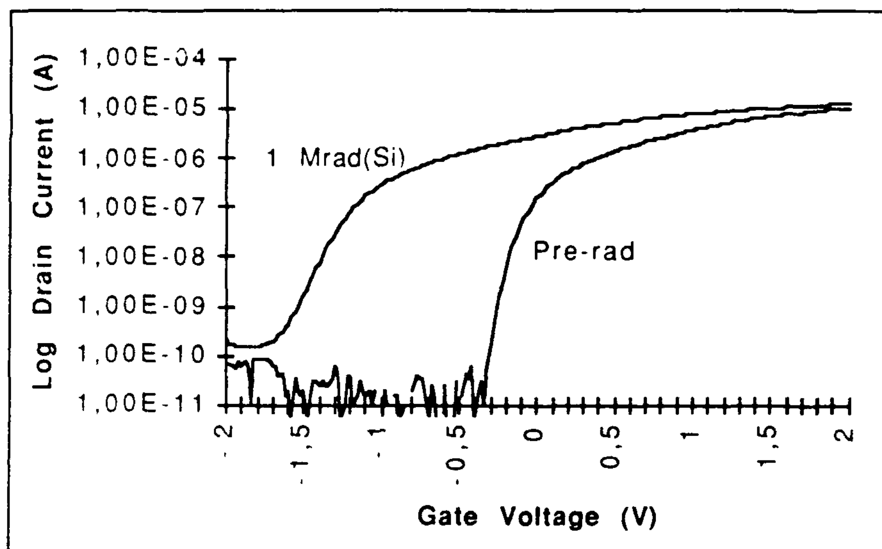
The goal of improving the radiation hardness has been achieved since the device show almost no degradation and only a 200 mV threshold voltage shift after exposure to 10 Mrad(Si) of X-rays [5] (ARACOR irradiation equipment). The results of these irradiation tests is presented in the Figure below.



Threshold voltage shift vs. X-ray total dose

5 R. Lawrence, Aracor, private communication

N-channel devices with a 30 nm gate oxide were irradiated using a ^{60}Co source in the Nuclear Sciences Department of the Université Catholique de Louvain (Belgium). Here are the results of such an irradiation test, carried out on a 3μm x 3μm n-channel device with a gate oxide thickness of 30 nm. The gate bias used during irradiation is +2 volts. Little leakage is observed after irradiation. The threshold shift is 1 volt, and corresponds to a hole trapping factor value of 0.08.



Logarithm of drain current *vs.* gate voltage on a 3μm x 3μm n-channel device with a gate oxide thickness of 30 nm

6. Packaged devices

Packaged devices are provided along with the present report. These devices are n- and p-channel Gate-all-around transistors and n- and p-channel regular thin-film SOI MOSFETs fabricated using the same process as the GAA devices (with the exception of the cavity etch). The Table below indicates the different types of devices found in **each** package.

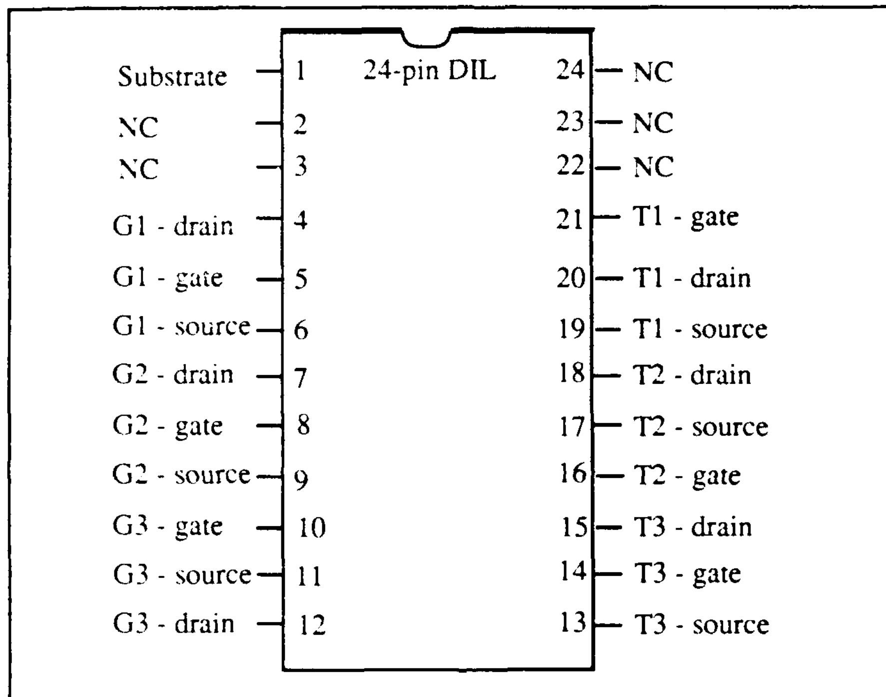
Name	Size (L/W)	Type device
G1	3/3 μm	GAA device
G2	3/4 μm	GAA device
G3	5/4 μm	GAA device
T1	3/3 μm	NMOS / PMOS
T2	3/4 μm	NMOS / PMOS
T3	5/4 μm	NMOS / PMOS

Devices in each package. G1, G2 and G3 are GAA devices, T1, T2 and T3 are regular thin-film SOI transistors.

It is worthwhile noting that each package contains only a chip from one of the process splits. Therefore each package contains devices with either a 30 nm or a 50 nm gate oxide, and contains either n- or p-channel devices, not both.

Quarter of wafers from each splits (unpackaged devices) have been mailed as well to Dr.Harold Hughes, Naval Research Labs, Washington D.C.

The bonding pad configuration of the chips is presented below. 24-pin DIL packages have been used. Pin #1 is connected to the silicon substrate (the back gate of the regular SOI transistors). The notations are self-explanatory. For instance, pin #4 is connected to the drain of the GAA device #1, and so on. The device names (G1, G2, G3, T1, T2 and T3) refer to the Table on the previous page.



Pin layout of the packages devices

Although all devices were functional prior to bonding, we noticed that some were degraded or destroyed after bonding. The wire-bonding machine of IMEC was indeed experiencing ESD problems at the time where these devices were packaged. As a result, some devices in the packages have lost their functionality. After bonding, all devices were re-tested in order to establish the three Tables below.

The devices which "survived" the bonding may also have been affected, in some way, by the ESD problem. Therefore, **we recommend that no voltage larger than 3 volts be used on any terminal of the devices** (gate, drain or back gate). **This is especially true for the devices with the thinner gate oxide** (wafer #7).

Wafer #7

NMOS, 30nm gate oxide

Package no.	Device name					
	G1	G2	G3	T1	T2	T3
7 - 1	X	X	X	X	X	X
7 - 2	OK	OK	X	X	OK	OK
7 - 3	OK	OK	X	OK	X	OK
7 - 4	OK	OK	OK	OK	OK	OK
7 - 5	X	OK	X	OK	OK	OK
7 - 6	OK	X	OK	OK	OK	OK
7 - 7	X	OK	OK	OK	OK	OK
7 - 8	X	X	X	X	OK	OK
7 - 9	X	X	OK	X	OK	OK
7 - 10	X	OK	OK	X	X	OK
7 - 11	X	OK	X	OK	X	X
7 - 12	X	X	X	X	X	X
7 - 13	OK	X	OK	X	OK	OK

Bonding functionality for packages from wafer 7 (n-channel devices with 30 nm-thick gate oxide. "OK" means that the device works fine, and "X" means that the device has been degraded by ESD during bonding.

Wafer #10

NMOS, 50nm gate oxide

Package no.	Device name					
	G1	G2	G3	T1	T2	T3
10 - 1	X	OK	OK	X	OK	OK
10 - 2	OK	OK	OK	OK	OK	OK
10 - 3	X	OK	OK	X	X	X
10 - 4	X	OK	OK	OK	OK	OK
10 - 5	X	OK	OK	OK	OK	OK
10 - 6	OK	OK	OK	OK	OK	OK
10 - 7	X	X	OK	X	OK	OK
10 - 8	X	OK	OK	OK	OK	OK
10 - 9	OK	X	OK	OK	OK	OK
10 - 10	X	OK	OK	X	OK	OK
10 - 11	X	OK	OK	X	OK	OK
10 - 12	OK	OK	OK	X	OK	OK
10 - 13	OK	OK	OK	X	OK	OK

Bonding functionality for packages from wafer 10 (n-channel devices with 50 nm-thick gate oxide. "OK" means that the device works fine, and "X" means that the device has been degraded by ESD during bonding.

Wafer #11

PMOS, 50nm gate oxide

	Device name					
Package no.	G1	G2	G3	T1	T2	T3
11 - 1	X	OK	OK	X	OK	OK
11 - 2	OK	OK	OK	OK	OK	OK
11 - 3	X	OK	OK	OK	OK	OK
11 - 4	X	OK	OK	OK	X	OK
11 - 5	X	OK	OK	OK	OK	OK
11 - 6	OK	OK	OK	OK	OK	OK
11 - 7	X	OK	OK	OK	OK	X
11 - 8	X	OK	OK	OK	OK	OK
11 - 9	X	OK	OK	OK	OK	OK
11 - 10	X	OK	OK	OK	OK	OK
11 - 11	X	OK	OK	OK	OK	OK
11 - 12	X	OK	OK	OK	OK	OK
11 - 13	X	OK	OK	OK	OK	OK

Bonding functionality for packages from wafer 11 (p-channel devices with 50 nm-thick gate oxide. "OK" means that the device works fine, and "X" means that the device has been degraded by ESD during bonding.

ANNEX I

PROCESS FLOW

The following pages describe in detail the different steps of the fabrication process

Lot number : PLINE240/1
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

SPLIT LOT 0900 27/03/91
SPLT
MVNS

CANON PR 4 6104 27/03/91
MVOU CANON

Parameter	Value	
# WAFERS		5
# TIMES		1
DEHYD TEMP		200
SOFTBAK TEMP		110
PHOTORESIST	S1713	
MASK ID	SOI ETCH	
EXPOSE TIME		39.00
SUBSTRATE	SIO2/SI	
D.U.V. TIME		5.00
POSTBAKETEMP		150
POST_METHOD	OVEN	
DEVELOPMENT	TRACK	
RESIST_SPEED		4300
VISUAL_INSP	PASS	
OXYGEN FLASH	NO	

INSP PH 4 7314 28/03/91
MVOU MICROSCOPE

Parameter	Value	
# WAFERS		5
PPI EXAMINE		50
PPI PASS		50
PPI FAIL		
PPI MARGINAL		
PPI ACTION	PASS	

WETCH OX 7104 28/03/91
MVOU WET BENCH

Parameter	Value	
# WAFERS		5
WETETCHSTUFF	THOX	
WET ETCHANT	BHF	
TEMPERATURE		[illegible]
DEVICEWAFER	[illegible]	
DEVWAFETCTIM		[illegible]

COMMENT : BHF: 20' - BAKE:130C 20' OVEN - BHF:5' [illegible]

Lot number : PLINE240/1
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

DRY US STR 7424 29/03/91
MVOU PRS800

# WAFERS	5
DRYSTRIPTIME	30.00
E_STRIP_TEMP	137.00
WETSTRIPSTUF	MICRO2001
WETSTRIPTIME	30
ULTRASON_PWR	.0
VISUAL_INSP	PASS

G_DOX 975 8436 29/03/91
MVOU I-4

# WAFERS	2
FUR TYPE	DRY
DRY OXIDTEMP	975
DRY OXID TIM	40
STANDARDRAMP	YES
TESTWAFER ID	SYSTEM
MEAN THICK	28.5
S.D. THICK	.7

READ ME 7010 03/04/91
MVOU

G_DOX 975 8437 04/04/91
MVOU I-4

# WAFERS	2
FUR TYPE	DRY
DRY OXIDTEMP	975
DRY OXID TIM	90
STANDARDRAMP	YES
TESTWAFER ID	SYSTEM
MEAN THICK	47.5
S.D. THICK	.7

READ ME 7011 05/04/91
HLLT
RLLT
COMMENT : SI-BRIDGE OK

Lot number : PLINE240/1
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

READ ME 7011 05/04/91
MVOU

G_DOX 975 8438 05/04/91
HLLT
COMMENT : DERDE WAFERLABELING NIET LEESBAAR IN SPEC
RLLT
MVOU I-4

# WAFERS		4
FUR TYPE	DRY	
DRY OXIDTEMP		975
DRY OXID TIM		90
STANDARDRAMP	YES	
TESTWAFER ID	SYSTEEM	
MEAN THICK		49.8
S.D. THICK		1.1

THK_MEAS_8 7358 08/04/91
MVOU LEITZ

# WAFERS		4
TESTWAFER ID	S3CM1/18,20	
MEAN THICK		29.7
S.D. THICK		.4
DEVICEWAFER1	S3CM1/18	
THICKNESS1		29.8
THICKNESS1		30.0
THICKNESS1		29.2
THICKNESS1		30.2
THICKNESS1		29.4
DEVICEWAFER2	S3CM1/20	
THICKNESS2		49.5
THICKNESS2		50.1
THICKNESS2		49.2
THICKNESS2		50.8
THICKNESS2		49.8
NOMTHICKNESS		50
GTM ACTION	PASS	

I/I-B MU L 3292 08/04/91
MVOU NV6200

# WAFERS		
ION SPECIES	[illegible]	
IMPLANT DOSE	150E [illegible]	

Lot number : PLINE240/1
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

Step	Equipment		Date	Parameter	Value	
I/I-B MU L	3292		08/04/91			
				IMP. ENERGY		25
				BEAM CURRENT		2
				TILT ANGLE		7.0
				RUN NUMBER	910408/3	
				RESIST ON ?	NO	
				POSTBAKE ?	NO	
				CHAMBER VAC	450E-08	
				H2 COOL PRES		3.0
				TOTAL TIME		16

Step	Equipment		Date	Parameter	Value	
I/I-P 1E11	3121		08/04/91			
	CEDA	NV6200		# WAFERS		1
				ION SPECIES	BORON	
				IMPLANT DOSE	200E 10	
				IMP. ENERGY		25
				BEAM CURRENT	************	
				TILT ANGLE		7.0
				RUN NUMBER	910408/4	
				RESIST ON ?	NO	
				POSTBAKE ?	NO	
				CHAMBER VAC	270E-08	
				H2 COOL PRES		3.0
				TOTAL TIME		22
	CEDA	NV6200		# WAFERS		2
				ION SPECIES	BORON	
				IMPLANT DOSE	250E 10	
				IMP. ENERGY		25
				BEAM CURRENT		2
				TILT ANGLE		7.0
				RUN NUMBER	910408	
				RESIST ON ?	NO	
				POSTBAKE ?	NO	
				CHAMBER VAC	314E-08	
				H2 COOL PRES		3.0
				TOTAL TIME		28
	MVOU	NV6200		# WAFERS		1
				ION SPECIES	PHOSPHORUS	
				IMPLANT DOSE	[illegible]	
				IMP. ENERGY		[illegible]
				BEAM CURRENT		
				TILT ANGLE		
				RUN NUMBER	[illegible]	
				RESIST ON ?	NO	

Lot number : PLINE240/1
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

I/I-P 1E11 3121 08/04/91

POSTBAKE ?	NO
CHAMBER VAC	515E-08
H2 COOL PRES	2.0
TOTAL TIME	60

MERGE LOT 0950 08/04/91
MRLT

```
+--------------------------------------------------------------------+
| UNITS used :                                                       |
|                                                                    |
| Oven times are in minutes                                          |
| Sputter times are in seconds                                       |
| Etch times per wafer are in seconds                                |
| Strip times are in minutes                                         |
| Temperatures are in degrees Celsius                                |
| Dimensions are in nm                                               |
| Implant dose (ions/cm2); Implant Energy (KeV); Beam current (uA)   |
+--------------------------------------------------------------------+
```

```
Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1


PRD INFO          7000        25/02/91
        CRLT
        MVOU
------------------------------------------------------------------------

WFR SELECT        7001        26/02/91
        MVOU       KRASPEN              LABEL            S3CM2/1-20
------------------------------------------------------------------------

THK MEAS_1        7351        26/02/91
        MVOU       LEITZ                # WAFERS                    10
                                        DEVICEWAFER1     ALL SOI
                                        NOMTHICKNESS               200
                                        GTM ACTION       PASS
COMMENT : SEE LTHL FOR SI-THICKNESSESS.
------------------------------------------------------------------------

FULL CLEAN        [illegible]  27/02/91
        [illegible] MERCURY             # WAFERS                    16
                                        CLEAN TYPE       FULL
------------------------------------------------------------------------

[illegible]       8640        27/02/91
        [illegible] I-3                 # WAFERS                    10
                                        FUR TYPE         DRY
                                        DRY OXIDTEMP              1000
                                        DRY OXID TIM               180
                                        STANDARDRAMP     YES
                                        TESTWAFER ID     SYSTEEM
                                        MEAN THICK               101.6
                                        S.D. THICK                 2.1
------------------------------------------------------------------------

WETCH OX          7101        27/02/91
        MVOU       WET BENCH            # WAFERS                    10
                                        WETETCHSTUFF     THOX
                                        WET ETCHANT      BHF
                                        TEMPERATURE               22.0
                                        DEVICEWAFER      7-16
                                        DEVWAFETCTIM               110
```

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

WETCH OX 7101 27/02/91

THK_MEAS_2 7352 27/02/91
MVOU LEITZ

# WAFERS		10
NOMTHICKNESS		160
GTM ACTION	PASS	

COMMENT : MEASUREMENTS SEE LTHL. MEASURED ON VS/VIS.

D_OX 1000 8641 28/02/91
MVOU I-3

# WAFERS		10
FUR TYPE	DRY	
DRY OXIDTEMP		1000
DRY OXID TIM		32
STANDARDRAMP	YES	
TESTWAFER ID	SYSTEEM	
MEAN THICK		31.1
S.D. THICK		.9

WETCH OX 7102 28/02/91
HLLT
RLLT
MVOU WET BENCH

# WAFERS		5
WETETCHSTUFF	THOX	
WET ETCHANT	BHF	
TEMPERATURE		22.0
DEVICEWAFER	12-16	
DEVWAFETCTIM		43

THK_MEAS_3 7353 04/03/91
MVOU LEITZ

# WAFERS		5
DEVICEWAFER1	12-16	
NOMTHICKNESS		142
GTM ACTION	PASS	

D_OX 1000 8642 04/03/91

```
Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1


D_OX  1000        8642        04/03/91
          MVOU        I-3                       # WAFERS                        15
                                                FUR TYPE          DRY
                                                DRY OXIDTEMP                  1000
                                                DRY OXID TIM                    31
                                                STANDARDRAMP      YES
                                                TESTWAFER ID      SYSTEEM
                                                MEAN THICK                    30.5
                                                S.D. THICK                      .4
------------------------------------------------------------------------------------

THK_MEAS_4        7354        05/03/91
          MVOU        LEITZ                     # WAFERS                         4
                                                TESTWAFER ID      S3CM1/17-20
                                                NOMTHICKNESS                    30
                                                GTM ACTION        PASS

COMMENT ANNOTATION : 17: C:32.9  N:33.4  Z:33.9  O:32.7  W:32.5
                     18: C:33.9  N:32.7  Z:32.7  O:32.9  W:32.3
                     19: C:32.5  N:32.5  Z:32.5  O:32.7  W:32.3
                     20: C:32.7  N:32.5  Z:33.2  O:33.0  W:32.1
                     PLINE240
                     WAFER S3CM1/16 VERTOONT ZWARTE VLEKJES
                     (HET IS GEEN RESIST)

COMMENT : MEASUREMENTS SEE LTHL (ALTH).
------------------------------------------------------------------------------------

NITR DEP          1201        05/03/91
          MVOU        NITRIDE                   # WAFERS                        20
                                                CLEAN_WIP         BASIC
                                                FILM_TYPE         NITRIDE
                                                STANDARD.?        YES
                                                DEPOSIT TIME                    99
                                                MEAN THICK S                 204.7
                                                S.D. THICK S                   2.9
                                                TESTWAFER ID      SYSTEEM
                                                PARTICLE_TOT                    65
                                                PARTICLE_CM2                   .78
                                                AREA                           .32
                                                PART_RANGE_1                    59
                                                PART_RANGE_2                     3
                                                PART_RANGE_3
                                                PART_RANGE_4
```

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

Step	Code	Equipment	Date	Parameter	Value
NITR DEP	1201		05/03/91		
				PART_RANGE_5	
				PART_RANGE_6	
				PART_RANGE_7	
				PART_RANGE_8	
				PART_RANGE_9	1
				PART_RANGE_0	2
				S_D_PARTIC.	239.57
				EXCLUSION	10

Step	Code	Equipment	Date	Parameter	Value
THK_MEAS_5	7355		05/03/91		
	MVOU	SPECTRAMAP		# WAFERS	4
				TESTWAFER ID	S3CM1/17-20
				NOMTHICKNESS	200
				GTM ACTION	PASS

COMMENT : MEASUREMENTS SEE LTHL (ALTH).

Step	Code	Equipment	Date	Parameter	Value
CANON PR 1	6101		05/03/91		
	MVOU	CANON		# WAFERS	16
				# TIMES	1
				DEHYD TEMP	200
				SOFTBAK TEMP	110
				PHOTORESIST	S1713
				MASK ID	SOI ACT
				EXPOSE TIME	35.00
				SUBSTRATE	NITRIDE
				D.U.V. TIME	.00
				POSTBAKETEMP	95
				POST_METHOD	HOTPLATE
				DEVELOPMENT	TRACK
				RESIST_SPEED	4300
				VISUAL_INSP	PASS
				OXYGEN FLASH	NO

Step	Code	Equipment	Date	Parameter	Value
INSP PH 1	7311		06/03/91		
	MVOU	MICROSCOPE		# WAFERS	5
				PPI EXAMINE	50
				PPI PASS	50
				PPI FAIL	
				PPI MARGINAL	

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

INSP PH 1 7311 06/03/91
PEI ACTION PASS
COMMENT : SI TOP LAYER FULL OF SI-DEFECTS (STAPELFOUTEN).

NIT D ETCH 4201 07/03/91
MVOU DUAL

# WAFERS		16
RECIPE ID	NI ETCH	
LOGBOOK REF	91/58	
DRYNITRSTUFF	NITRIDE	
ETCH_TIME		1105.00
VISUAL INSP	PASS	
MASK COND..	GOOD	
ETCHSTOPLEFT		30.4
ETCHSTOPLEFT		29.8
ETCHSTOPLEFT		29.0
ETCHSTOPLEFT		29.8
ETCHSTOPLEFT		31.3

POST ETCH1 7331 08/03/91
MVOU MICROSCOPE

# WAFERS		6
PEI EXAMINE		60
PEI PASS		55
PEI FAIL		
PEI MARGINAL		55
PEI ACTION	PASS	

COMMENT : WAFER 16: VLEKKEN!

DRY US STR 7421 11/03/91
MVOU PRS800

# WAFERS		16
DRYSTRIPTIME		30.00
WETSTRIPSTUF	MICRO2001	
WETSTRIPTIME		30
ULTRASON_PWR		100.0
VISUAL INSP	PASS	

WETCH OX 7103 11/03/91
MVOU WET BENCH

# WAFERS		16
WETETCHSTUFF	THOX	

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

```
WETCH OX        7103      11/03/91
                                         WET ETCHANT     BHF
                                         TEMPERATURE              22.0
                                         TESTWAFER ID    S3CM1/1
                                         TESWAFETCTIM               35
                                         DEVICEWAFER     S3CM1/2-16
                                         DEVWAFETCTIM               35
COMMENT : BHF ETCHTIME: 29" + 6" = 35".
--------------------------------------------------------------------

CANON PR 2      6102      12/03/91
        MVOU      CANON                  # WAFERS                    5
                                         # TIMES                     1
                                         DEHYD TEMP                200
                                         SOFTBAK TEMP              110
                                         PHOTORESIST     S1713
                                         MASK ID         SOI NCHAN VT
                                         EXPOSE TIME             43.00
                                         SUBSTRATE       SI/NITRIDE
                                         D.U.V. TIME             10.00
                                         POSTBAKETEMP              150
                                         POST_METHOD     OVEN
                                         DEVELOPMENT     TRACK
                                         RESIST_SPEED             4300
                                         VISUAL_INSP     PASS
                                         OXYGEN FLASH    NO
--------------------------------------------------------------------

INSP PH 2       7312      12/03/91
        MVOU      MICROSCOPE             # WAFERS                    5
                                         PPI EXAMINE                30
                                         PPI PASS                   30
                                         PPI FAIL
                                         PPI MARGINAL
                                         PPI ACTION      PASS
--------------------------------------------------------------------

I/I-B 1E14      3250      13/03/91
        MVOU      NV6200                 # WAFERS                   12
                                         ION SPECIES     BORON
                                         IMPLANT DOSE    100E 12
                                         IMP. ENERGY                50
                                         BEAM CURRENT              111
```

```
Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

I/I B 1E14      3250      13/03/91
                                        TILT ANGLE                    7.0
                                        RUN NUMBER       910313
                                        RESIST ON ?      YES
                                        POSTBAKE ?       NO
                                        TOTAL TIME                    60
--------------------------------------------------------------------------

DRY US STR      7422      13/03/91
        MVOU       PRS800               # WAFERS                      5
                                        DRYSTRIPTIME              60.00
                                        E_STRIP_TEMP             199.00
                                        WETSTRIPSTUF     MICRO2001
                                        WETSTRIPTIME                 30
                                        ULTRASON_PWR              100.0
                                        VISUAL INSP      PASS
--------------------------------------------------------------------------

C ANN 950       8330      14/03/91
        MVOU       I-2                  # WAFERS                      4
                                        FUR TYPE         ANN
                                        ANNEAL TEMP                 950
                                        ANNEAL TIME                  90
                                        STANDARDRAMP     YES
--------------------------------------------------------------------------

SI D ETCH       4001      21/03/91
        MVOU       DUAL                 # WAFERS                     10
                                        RECIPE ID        SI ETCH
                                        LOGBOOK REF      91/77
                                        DRYSIXTSTUFF     SI XTAL
                                        ETCH_TIME                420.00
                                        VISUAL INSP      PASS
                                        MASK COND..      GOOD
--------------------------------------------------------------------------

POST ETCH2      7332      25/03/91
        MVOU       MICROSCOPE           # WAFERS                      6
                                        PEI EXAMINE                  60
                                        PEI PASS                     60
                                        PEI FAIL
                                        PEI MARGINAL
```

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

POST_ETCH2 7332 25/03/91

PEI ACTION	PASS		

COMMENT : FOX MEASURED ON WAFERS 9.14.11: +/- 400NM.

C_WOX 1000 8140 25/03/91
MVOU I-2

# WAFERS		10
FUR TYPE	WET	
WET OXIDTEMP		1000
WET OXID TIM		138
STANDARDRAMP	YES	
TESTWAFER ID	SYSTEM	
MEAN THICK		592.4
S.D. THICK		2.7

C_WOX 1000 8141 26/03/91
MVOU I-1

# WAFERS		11
FUR TYPE	WET	
WET OXIDTEMP		1000
WET OXID TIM		75
STANDARDRAMP	YES	
TESTWAFER ID	SYSTEM	
MEAN THICK		393.1
S.D. THICK		4.9

THK_MEAS_6 7356 27/03/91
MVOU LEITZ

# WAFERS		4
DEVICEWAFER1	S3CM1/1	
THICKNESS1		584.9
THICKNESS1		588.0
THICKNESS1		587.4
THICKNESS1		586.6
THICKNESS1		587.3
DEVICEWAFER2	S3CM1/4	
THICKNESS2		588.7
THICKNESS2		591.8
THICKNESS2		590.1
THICKNESS2		592.2
THICKNESS2		588.5
NOMTHICKNESS		600
GTM ACTION	PASS	

```
Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

THK_MEAS_6        7356        27/03/91
-----------------------------------------------------------------------

C_WOX 1000        8142        27/03/91
          CEDA        LEITZ                      # WAFERS                  4
                                                 DEVICEWAFER1    S3CM1/7
                                                 THICKNESS1              653.0
                                                 THICKNESS1              641.2
                                                 THICKNESS1              640.8
                                                 THICKNESS1              629.9
                                                 THICKNESS1              638.0
                                                 DEVICEWAFER2    S3CM1/12
                                                 THICKNESS2              647.0
                                                 THICKNESS2              643.3
                                                 THICKNESS2              632.8
                                                 THICKNESS2              625.4
                                                 THICKNESS2              635.0
                                                 NOMTHICKNESS             633
                                                 GTM ACTION      PASS
COMMENT : FOX ON SOI-WAFERS:    .HICKNESS=THOX SI-FILM-INTERMEDIATE OX
          MVNS        I-1                        # WAFERS
                                                 WET OXID TIM
COMMENT : NO ADDITIONAL FIELD OXIDATION IS NEEDED.
-----------------------------------------------------------------------

WETCH NITR        .121        27/03/91
          MVOU        WET BENCH                  # WAFERS                 20
                                                 WETETCHSTUFF    THOX
                                                 WET ETCHANT     BHF
                                                 DEVWAFETCTIM             20
                                                 WETCHSTUFF_1    NITRIDE
                                                 WET ETCHANT1    TRANSETCH
                                                 DEVWAFETTIM1             60
COMMENT :
-----------------------------------------------------------------------

SPLIT LOT         0900        27/03/91
          SPLT
          MVOU
-----------------------------------------------------------------------
```

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

SPLIT LOT 0900 27/03/91
I/I-P 1E11 3120 28/03/91
MVOU NV6200

# WAFERS		3
ION SPECIES	PHOSPHORUS	
IMPLANT DOSE	100E 09	
IMP. ENERGY		100
BEAM CURRENT		
TILT ANGLE		7.0
RUN NUMBER	910328/4	
RESIST ON ?	NO	
POSTBAKE ?	NO	
CHAMBER VAC	586E-09	
H2 COOL PRES		1.5
TOTAL TIME		17

G_DOX 975 8435 29/03/91
MVOU I-4

# WAFERS		12
FUR TYPE	DRY	
DRY OXIDTEMP		975
DRY OXID TIM		90
STANDARDRAMP	YES	
TESTWAFER ID	SYSTEM	
MEAN THICK		53.6
S.D. THICK		3.8
TESTWAF ID 2	T17	
MEAN THICK 2		52.3
S.D. THICK 2		1.4

I/I-B MU L 3290 29/03/91
MVOU NV6200

# WAFERS		5
ION SPECIES	BORON	
IMPLANT DOSE	100E 09	
IMP. ENERGY		25
BEAM CURRENT		
TILT ANGLE		7.0
RUN NUMBER	910329/4	
RESIST ON ?	NO	
POSTBAKE ?	NO	
CHAMBER VAC	326E-08	
H2 COOL PRES		2.0
TOTAL TIME		13

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

THK_MEAS_7 7357 03/04/91
MVOU LEITZ

# WAFERS	2
TESTWAFER ID	17.19
NOMTHICKNESS	50
GTM ACTION	PASS

COMMENT ANNOTATION :
S3CM1/17: C=49.9 N=48.8 Z=49.7 O=49.4 W=48.7
S3CM1/19: C=48.9 N=49.9 Z=49.5 O=49.1 W=49.0

CANON PR 3 6103 03/04/91
MVOU CANON

# WAFERS	4
# TIMES	1
DEHYD TEMP	200
SOFTBAK TEMP	110
PHOTORESIST	S1713
MASK ID	SOI N CH VT
EXPOSE TIME	40.00
SUBSTRATE	THOX
D.U.V. TIME	10.00
POSTBAKETEMP	150
POST_METHOD	OVEN
DEVELOPMENT	TRACK
RESIST_SPEED	4300
VISUAL_INSP	PASS
OXYGEN FLASH	NO

INSP PH 3 7313 04/04/91
MVOU MICROSCOPE

# WAFERS	4
PPI EXAMINE	20
PPI PASS	20
PPI FAIL	
PPI MARGINAL	
PPI ACTION	PASS

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

Step			Parameter	Value	
INSP PH 3	7313	04/04/91			
I/I-B MU L	3291	04/04/91			
MVOU	NV6200		# WAFERS		3
			ION SPECIES	BORON	
			IMPLANT DOSE	100E 10	
			IMP. ENERGY		170
			BEAM CURRENT		2
			TILT ANGLE		7.0
			RUN NUMBER	91040473	
			RESIST ON ?	NO	
			POSTBAKE ?	NO	
			CHAMBER VAC	419E-08	
			H2 COOL PRES		3.0
			TOTAL TIME		16

Step			Parameter	Value	
DRY US STR	7423	04/04/91			
CEDA	NV6200		# WAFERS		2
			ION SPECIES	BORON	
			IMPLANT DOSE	600E 09	
			IMP. ENERGY		30
			BEAM CURRENT		1
			TILT ANGLE		7.0
			RUN NUMBER	91040474	
			RESIST ON ?	YES	
			POSTBAKE ?	NO	
			CHAMBER VAC	463E-09	
			H2 COOL PRES		3.0
			TOTAL TIME		19
CEDA	NV6200		# WAFERS		3
			ION SPECIES	BORON	
			IMPLANT DOSE	600E 09	
			IMP. ENERGY		30
			BEAM CURRENT		1
			TILT ANGLE		7.0
			RUN NUMBER	91040475	
			RESIST ON ?	YES	
			POSTBAKE ?	NO	
			CHAMBER VAC	503E-09	
			H2 COOL PRES		3.0
			TOTAL TIME		22
CEDA	NV6200		# WAFERS		2
			ION SPECIES	BORON	
			IMPLANT DOSE	100E 10	
			IMP. ENERGY		30

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

DRY US STR [illegible] [illegible]

MVOU PRS800

Parameter	Value	
BEAM CURRENT		[illegible]
TILT ANGLE		7.0
RUN NUMBER	[illegible]	
RESIST ON ?	YES	
POSTBAKE ?	NO	
CHAMBER VAC	537E-09	
H2 COOL PRES		3.0
TOTAL TIME		14
# WAFERS		4
DRYSTRIPTIME		30.00
E_STRIP_TEMP		166.00
WETSTRIPSTUF	MICRO2000	
WETSTRIPTIME		30
ULTRASON_PWR		100.0
VISUAL_INSP	PASS	

COMMENT : WAFER S3CM1/16:LITTLE SPOTS IN FIELD REGIONS: NOT RESIST.

JUMP TO OP [illegible] 05/04/91
[illegible]

MERGE LOT [illegible] 08/04/91
[illegible]
[illegible]

POLY GATE 1101 09/04/91
[illegible] POLY

Parameter	Value	
# WAFERS		20
CLEAN_WIP	BASIC	
FILM_TYPE	POLY	
STANDARD.?	YES	
DEPOSIT TIME		38.1
MEAN THICK S		447.4
S.D. THICK S		1.6
TESTWAFER ID	SYSTEEM	

THK_MEAS_? [illegible] [illegible]
MVOU LEITZ

Parameter	Value	
# WAFERS		4
TESTWAFER ID	S3CM1-17-20	

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

THK_MEAS_9   7359   09/04/91

DEVICEWAFER1	S3CM1/17
THICKNESS1	447.9
THICKNESS1	447.9
THICKNESS1	449.9
THICKNESS1	448.9
THICKNESS1	450.3
DEVICEWAFER2	S3CM1/18
THICKNESS2	446.4
THICKNESS2	446.4
THICKNESS2	447.9
THICKNESS2	446.4
THICKNESS2	448.6
NOMTHICKNESS	450
GTM ACTION	PASS

COMMENT ANNOTATION : VALUE CHANGED FOR PARAMETER THICKNESS2
UNIT Centre
FROM 444.9   TO 446.4
VALUE CHANGED FOR PARAMETER THICKNESS2
UNIT East
FROM 444.6   TO 446.4
VALUE CHANGED FOR PARAMETER THICKNESS2
UNIT North
FROM 448.9   TO 447.9
VALUE CHANGED FOR PARAMETER THICKNESS2
UNIT South
FROM 445.7   TO 446.4
VALUE CHANGED FOR PARAMETER THICKNESS2
UNIT West
FROM 448.9   TO 448.6
VALUE CHANGED FOR PARAMETER # WAFERS
UNIT
FROM 15   TO 19

COAT FRONT   6901   09/04/91
CEDA   LEITZ

# WAFERS	4
TESTWAFER ID	S3CM1/17-20
DEVICEWAFER1	S3CM1/19
THICKNESS1	444.9
THICKNESS1	444.6
THICKNESS1	448.9
THICKNESS1	445.7

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

Step	Code	Date	Parameter	Value
COAT FRONT	6901	09/04/91		
			THICKNESS1	448.9
			DEVICEWAFER2	S3CM1/20
			THICKNESS2	445.3
			THICKNESS2	444.9
			THICKNESS2	449.9
			THICKNESS2	447.0
			THICKNESS2	449.9
			NOMTHICKNESS	450
			GTM ACTION	PASS
MVOU	MTI		# WAFERS	19
			# TIMES	1
			DEHYD TEMP	200
			MISCSPINSTUF	S3413
			RESIST_SPEED	4600
			D.U.V._TIME	.00
			POSTBAKETEMP	150
			POST_METHOD	OVEN
			POSTBAKETIME	150E-01

Step	Code	Date	Parameter	Value
WETCH POLY	7111	09/04/91		
MVOU	WET BENCH		# WAFERS	19
			WETETCHSTUFF	POLY
			WET ETCHANT	POLYETCHSTUF
			TEMPERATURE	22.0
			TESTWAFER ID	S3CM1/20
			TESWAFETCTIM	120
			DEVICEWAFER	ALL
			DEVWAFETCTIM	190

COMMENT : BEFORE POLY WET ETCH, A BHF DIP OF 10" IS DONE.

Step	Code	Date	Parameter	Value
WETCH OX	7105	09/04/91		
MVOU	WET BENCH		# WAFERS	19
			WETETCHSTUFF	THOX
			WET ETCHANT	BHF
			TEMPERATURE	22.0
			TESTWAFER ID	S3CM1/20
			TESWAFETCTIM	58
			DEVICEWAFER	ALL
			DEVWAFETCTIM	56

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

DRY US STR 7425 10/04/91
MVOU PRS800

# WAFERS	19
DRYSTRIPTIME	20.00
E_STRIP_TEMP	165.00
WETSTRIPSTUF	MICRO2000
WETSTRIPTIME	30
ULTRASON_PWR	.0
VISUAL INSP	PASS

I/I-P 1E16 3170 12/04/91
MVOU NV6200

# WAFERS	19
ION SPECIES	PHOSPHORUS
IMPLANT DOSE	100E 14
IMP. ENERGY	50
BEAM CURRENT	700
TILT ANGLE	7.0
RUN NUMBER	910411/1
RESIST ON ?	NO
POSTBAKE ?	NO
CHAMBER VAC	400E-08
H2 COOL PRES	2.0
TOTAL TIME	334

C_ANN 800 8300 12/04/91
MVOU I-2

# WAFERS	12
FUR TYPE	ANN
ANNEAL TEMP	800
ANNEAL TIME	45
STANDARDRAMP	YES

COMMENT : SRCM1/5 GEBROKEN IN OVEN

C_ANN 800 8301 12/04/91
MVOU I-2

# WAFERS	7
FUR TYPE	ANN
ANNEAL TEMP	800
ANNEAL TIME	240
STANDARDRAMP	YES

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

```
WETCH OX        7106      15/04/91
        MVOU      WET BENCH          # WAFERS                  18
                                     WETETCHSTUFF    THOX
                                     WET ETCHANT     BHF
                                     TEMPERATURE              22.0
                                     TESTWAFER ID    S3CM1/17-20
                                     TESWAFETCTIM              14
                                     DEVICEWAFER     ALL -(5.12)
                                     DEVWAFETCTIM              14
-----------------------------------------------------------------

RES_MEAS_1      7371      15/04/91
        CEDA      FOURDIM            # WAFERS                   1
                                     TESTWAFER ID    S3CM1/19
                                     MEAN RESISVY    190E 00
                                     S.D. RESISVY    224E-02
                                     GRM ACTION      PASS
        MVOU      FOURDIM            # WAFERS                   1
                                     TESTWAFER ID    S3CM1/20
                                     MEAN RESISVY    140E 00
                                     S.D. RESISVY    314E-02
                                     GRM ACTION      PASS
-----------------------------------------------------------------

CANON PR 5      6105      24/04/91
        MVOU      CANON              # WAFERS                  14
                                     # TIMES                    1
                                     DEHYD TEMP               200
                                     SOFTBAK TEMP             110
                                     PHOTORESIST     S1713
                                     MASK ID         SOI POLY
                                     EXPOSE TIME            24.00
                                     SUBSTRATE       POLY
                                     D.U.V. TIME              .00
                                     POSTBAKETEMP              95
                                     POST_METHOD     HOTPLATE
                                     DEVELOPMENT     TRACK
                                     RESIST_SPEED            4300
                                     VISUAL_INSP     PASS
                                     OXYGEN FLASH    NO
-----------------------------------------------------------------
```

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

```
INSP PH 5        7315        24/04/91
        MVOU        MICROSCOPE            # WAFERS                    5
                                          PPI EXAMINE                50
                                          PPI PASS                   50
                                          PPI FAIL
                                          PPI MARGINAL
                                          PPI ACTION     PASS
---------------------------------------------------------------------------

PLY_1511e        4102        26/04/91
        MVOU        TEGAL                 # WAFERS                   14
                                          RECIPE ID      HBR-ETCH
                                          LOGBOOK REF    91/121
                                          DRYPOLYSTUFF   POLY
                                          ETCH_TIM_BRK               18
                                          ETCH_TIM_BLK               30
                                          ETCH_TIM_OVN              120
                                          DEVWAF_MV_1             518.3
                                          DEVWAF_SD_1               5.3
                                          DEVWAF_MV_2             565.2
                                          DEVWAF_SD_2              10.3
                                          VISUAL_INSP    PASS
                                          MASK COND..    GOOD
---------------------------------------------------------------------------

POST_ETCH3       7333        29/04/91
        MVOU        MICROSCOPE            # WAFERS                    7
                                          PEI EXAMINE                42
                                          PEI PASS                   42
                                          PEI FAIL
                                          PEI MARGINAL
                                          PEI ACTION     PASS
COMMENT : GAA TRNSTRS:ON A LOT OF THEM: BLACK DOTS AT THE EDGE OF A.A.
---------------------------------------------------------------------------

DRY US STR       7426        03/05/91
        MVOU        FRS800                # WAFERS                   14
                                          DRYSTRIPTIME            60.00
                                          E_STRIP_TEMP           149.00
                                          WETSTRIPSTUF   MICRO2000
```

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

DRY US STR 7426 03/05/91

WETSTRIPTIME		[illegible]
ULTRASON PWR		[illegible]
VISUAL INSP	PASS	

COMMENT ANNOTATION : WAFERS7-11: AFTER SUPPLEMENTARY DRY + WET STRIP: STILL VERY FEW PIECES OF THIN BLACK "WIRES" AT THE EDGE OF SOME POLY STRUCTURES OF THE AAG-WAFERS.
1: C=37.9 N=39.1 Z=38.9 O=38.3 W=39.2
2: C=39.8 N=40.3 Z=39.5 O=39.4 W=39.6
3: C=38.0 N=39.1 Z=38.9 O=36.7 W=38.4
4: C=37.7 N=38.8 Z=38.4 O=37.7 W=38.8
6: C=40.6 N=41.4 Z=42.0 O=40.2 W=41.0
17:C=40.2 N=42.0 Z=41.2 O=42.0 W=41.0
18:C=20.6 N=22.1 Z=23.1 O=23.0 W=22.3

COMMENT : ALL WAFERS: 2 X (DRY:30'-WET:30' STRIP). 7-11: + DRY: 30'.

THK_MEAS10 7360 03/05/91
MVOU LEITZ

# WAFERS		7
TESTWAFER ID	17	
MEAN THICK		38.7
S.D. THICK		.6
DEVICEWAFER1	1-4.6	
NOMTHICKNESS		40
GTM ACTION	PASS	

WETCH OX 7107 06/05/91
MVOU LEITZ

# WAFERS		6
WETETCHSTUFF	THOX	
WET ETCHANT	2%HF	
TEMPERATURE		22.0
TESTWAFER ID	17	
TESWAFETCTIM		104
DEVICEWAFER	ALL	
DEVWAFETCTIM		87

COMMENT ANNOTATION : S3CM1/1: C=17.2 N=18.4 Z=18.6 O=19.1 W=20.9
S3CM1/2: C=18.8 N=20.1 Z=19.5 O=20.1 W=20.1
S3CM1/3: C=18.2 N=20.0 Z=18.7 O=19.0 W=19.8
S3CM1/4: C=18.4 N=17.3 Z=20.7 O=19.5 W=20.1

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

WETCH OX 7107 06/05/91
S3CM1-e: C=20.9 M=20.6 T=22.5 O=21.7 W=22.0

CANON PR 6 6106 06/05/91
MVOU CANON

# WAFERS		4
# TIMES		1
DEHYD TEMP		200
SOFTBAK TEMP		110
PHOTORESIST	S1713	
MASK ID	SOI NPLUS	
EXPOSE TIME		31.00
SUBSTRATE	THOX	
D.U.V. TIME		10.00
POSTBAKETEMP		150
POST_METHOD	OVEN	
DEVELOPMENT	TRACK	
RESIST_SPEED		4300
VISUAL_INSP	PASS	
OXYGEN FLASH	NO	

INSP PH 6 7316 07/05/91
MVOU MICROSCOPE

# WAFERS		4
PPI EXAMINE		20
PPI PASS		20
PPI FAIL		
PPI MARGINAL		
PPI ACTION	PASS	

I/I-P MU H 3195 07/05/91
MVOU NV6200

# WAFERS		11
ION SPECIES	PHOSPHORUS	
IMPLANT DOSE	400E 13	
IMP. ENERGY		70
BEAM CURRENT		300
TILT ANGLE		7.0
RUN NUMBER	0105?7/2	
RESIST ON ?	YES	
POSTBAKE ?	NO	
CHAMBER VAC	200E-08	
HE COOL PRES		3.0

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

I/I-P MU H 3195 07/05/91

TOTAL TIME	331

DRY US STR 7427 08/05/91
MVOU PRS800

# WAFERS		4
DRYSTRIPTIME		60.00
E_STRIP_TEMP		189.00
WETSTRIPSTUF	MICRO2000	
WETSTRIPTIME		30
ULTRASON_PWR		.0
VISUAL_INSP	PASS	

COMMENT : ON WAFER S3CM1/13: ON A FEW PLACES: (POLY PRINT OF) RUBBISH.

CANON PR 7 6107 08/05/91
MVOU CANON

# WAFERS		4
# TIMES		1
DEHYD TEMP		200
SOFTBAK TEMP		110
PHOTORESIST	S1713	
MASK ID	SOI P PLUS	
EXPOSE TIME		32.00
SUBSTRATE	THOX	
D.U.V. TIME		10.00
POSTBAKETEMP		150
POST_METHOD	OVEN	
DEVELOPMENT	TRACK	
RESIST_SPEED		4300
VISUAL_INSP	PASS	
OXYGEN FLASH	NO	

INSP PH 7 7317 08/05/91
MVOU MICROSCOPE

# WAFERS		4
PPI EXAMINE		20
PPI PASS		20
PPI FAIL		
PPI MARGINAL		
PPI ACTION	PASS	

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

I-I-B MU H 3295 13/05/91
MVOU NV6200

Parameter	Value
# WAFERS	7
ION SPECIES	BORON
IMPLANT DOSE	400E 13
IMP. ENERGY	25
BEAM CURRENT	181
TILT ANGLE	7.0
RUN NUMBER	910513/2
RESIST ON ?	YES
POSTBAKE ?	YES
CHAMBER VAC	500E-08
H2 COOL PRES	3.0
TOTAL TIME	552

DRY US STR 7428 14/05/91
MVOU PRS800

Parameter	Value
# WAFERS	4
DRYSTRIPTIME	60.00
WETSTRIPSTUF	MICRO2001
WETSTRIPTIME	30
ULTRASON_PWR	.0
VISUAL_INSP	PASS

C_ANN 800 8302 14/05/91
MVOU I-2

Parameter	Value
# WAFERS	14
FUR TYPE	ANN
ANNEAL TEMP	800
ANNEAL TIME	180
STANDARDRAMP	YES

TEOS UNSG 1001 15/05/91
MVOU TEOS

Parameter	Value
# WAFERS	16
FILM TYPE	USG
STANDARD.?	YES
DEPOSIT TIME	56.6
MEAN THICK S	603.1
S.D. THICK S	5.6
PARTICLE_TOT	62
PARTICLE_CM2	.74
AREA	.00

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

Step			Parameter		Value
TEOS UNSG	1001	15/05/91	PART_RANGE_1		47
			PART_RANGE_2		14
			PART_RANGE_3		1
			PART_RANGE_4		
			PART_RANGE_5		
			PART_RANGE_6		
			PART_RANGE_7		
			PART_RANGE_8		
			PART_RANGE_9		
			PART_RANGE_0		
			S_D_PARTIC.		62.60
			EXCLUSION		10

Step			Parameter		Value
C_ANN 800	8303	15/05/91			
MVOU	I-2		# WAFERS		16
			FUR TYPE	ANN	
			ANNEAL TEMP		800
			ANNEAL TIME		30
			STANDARDRAMP	YES	

Step			Parameter		Value
CANON PR 8	6108	15/05/91			
MVOU	CANON		# WAFERS		16
			# TIMES		1
			DEHYD TEMP		200
			SOFTBAK TEMP		110
			PHOTORESIST	S1713	
			MASK ID	SOI CONTACT	
			EXPOSE TIME		35.80
			SUBSTRATE	UTEOS	
			D.U.V. TIME		5.00
			POSTBAKETEMP		150
			POST_METHOD	OVEN	
			DEVELOPMENT	TRACK	
			RESIST_SPEED		4300
			VISUAL_INSP	PASS	
			OXYGEN FLASH	NO	

INSP PH 8 7318 16/05/91

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

INSP PH 8 7318 16/05/91
MVOU MICROSCOPE

# WAFERS		[illegible]
PPI EXAMINE		[illegible]
PPI PASS		[illegible]
PPI FAIL		
PPI MARGINAL		
PPI ACTION	PASS	

COMMENT : CONTROLE OP:1,3,9,16. OP 1,3:SPORADISCH KLEINE LAKVLIESJES(?

WETCH OX 7108 16/05/91
MVOU WET BENCH

# WAFERS		16
WETETCHSTUFF	UTEOS	
WET ETCHANT	BHF	
TEMPERATURE		22.0
TESTWAFER ID	17.18	
TESWAFETCTIM		180
DEVICEWAFER	ALL	
DEVWAFETCTIM		200

COMMENT : TEST: 17: 2'45". 18: 3'.

DRY US STR 7429 17/05/91
MVOU PRS800

# WAFERS		14
DRYSTRIPTIME		30.00
WETSTRIPSTUF	MICRO2001	
WETSTRIPTIME		30
ULTRASON_PWR		.0
VISUAL_INSP	PASS	

FRNT ALSI 5201 21/05/91
MVOU LLS801

# WAFERS		14
SPUTTALSTUFF	ALSI	
SPUTTER TEMP	WARM	
PROCESS_NAME	310H	
TARGET_LIFE		32036
SPUTTER TIME		1100
TESTWAFER ID	TEST26	
MEAN SHEET_R	[illegible]	
S.D. SHEET_R	[illegible]	
REFLECTIVITY		93
LAYER_WEIGHT		27.2

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

FRNT ALSI 5201 21/05/91

CANON PR 9 6109 22/05/91
MVOU CANON

# WAFERS		14
# TIMES		1
DEHYD TEMP		130
SOFTBAK TEMP		110
PHOTORESIST	S1713	
MASK ID	SOI 3UM M1	
EXPOSE TIME		30.00
SUBSTRATE	AL/SI	
D.U.V. TIME		10.00
POSTBAKETEMP		150
POST_METHOD	HOTPLATE	
DEVELOPMENT	TRACK	
RESIST_SPEED		4300
VISUAL_INSP	PASS	
OXYGEN FLASH	NO	

INSP PH 9 7219 23/05/91
MVOU MICROSCOPE

# WAFERS		-
PPI EXAMINE		50
PPI PASS		50
PPI FAIL		
PPI MARGINAL		
PPI ACTION	PASS	

INL D_ETCH 4401 28/05/91
MVOU INLINE

# WAFERS		14
RECIPE ID	C001	
LOGBOOK REF	91/198	
DRY_AL_STUFF	ALSI	
TOPTIWETCTIM		
ETCH_TIM_BRK		10
ETCH_TIM_END		168
ETCH_TIM_OVN		25
BOTTIWETCTIM		
PASSIV TIME		15
VISUAL INSP	PASS	
MASK COND..	GOOD	

```
Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1


INL D_ETCH      4441      28/05/91

-------------------------------------------------------------------------

POST_ETCH4      7334      29/05/91
        MVOU      MICROSCOPE            # WAFERS               4
                                        PEI EXAMINE           32
                                        PEI PASS              32
                                        PEI FAIL
                                        PEI MARGINAL
                                        PEI ACTION      PASS
-------------------------------------------------------------------------

DRY US STR      7430      29/05/91
        MVOU      PRS800                # WAFERS              14
                                        DRYSTRIPTIME       40.00
                                        E_STRIP_TEMP      149.00
                                        WETSTRIPSTUF    MICRO2000
                                        WETSTRIPTIME          30
                                        ULTRASON_PWR          .0
                                        VISUAL INSP     PASS
COMMENT : SUPPLEMENTARY DRY STRIP IN PRS800: 20'.
-------------------------------------------------------------------------

SINTER 420      9720      29/05/91
        MVOU      II-4                  # WAFERS               2
                                        FUR TYPE        SIN
                                        SINT AMBIENT    FORMINGGAS
                                        TEMPERATURE        420.0
                                        SINTER TIME           20
-------------------------------------------------------------------------

SINTER 420      9721      29/05/91
        MVOU      II-4                  # WAFERS              14
                                        FUR TYPE        SIN
                                        SINT AMBIENT    FORMINGGAS
                                        TEMPERATURE        420.0
                                        SINTER TIME           20
-------------------------------------------------------------------------

END PROCES      9999      30/05/91
```

Lot number : PLINE240
Product : SOI 3UM CMOS
Route : GW_S3CMOS1

```
+---------------------------------------------------------------------+
| UNITS used :                                                        |
|                                                                     |
| Oven times are in minutes                                           |
| Sputter times are in seconds                                        |
| Etch times per wafer are in seconds                                 |
| Strip times are in minutes                                          |
| Temperatures are in degrees Celsius                                 |
| Dimensions are in nm                                                |
| Implant dose (ions/cm2): Implant Energy (KeV): Beam current (uA)    |
+---------------------------------------------------------------------+
```

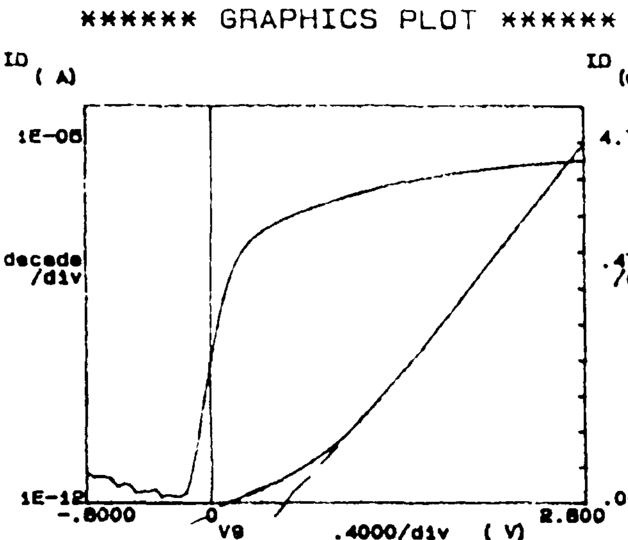
ELECTRICAL CHARACTERISTICS

This Annex reports the electrical characteristics of the GAA devices from the second run (one set of curves for each split).

These characteristics are:

- $I_D(V_G)$ for V_{DS} = 100 mV, with both linear and logarithmic vertical scales (top left Figure)
- $I_D(V_{DS})$ for V_G = 0 to 5 volts, (bottom left Figure)
- Transconductance (g_m) at V_{DS} = 100 mV, as a function of gate voltage (bottom right Figure)

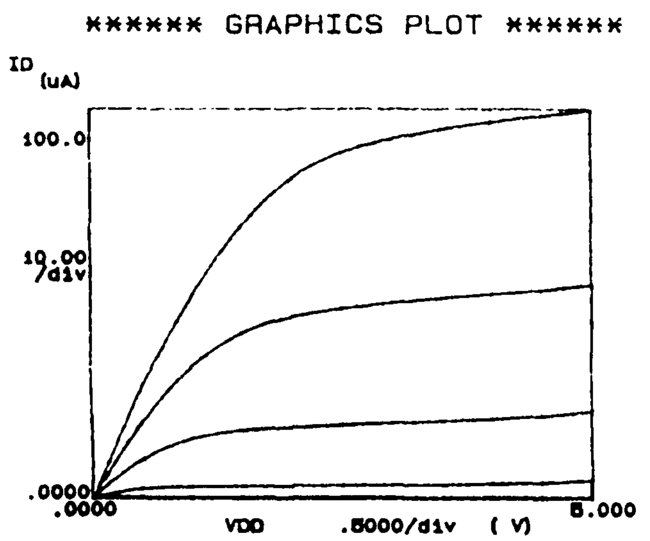
Wafer 7
GAA N-ch
t_{ox} = 300 Å



Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 3.0000V
Step .0000V

Variable2:
VBB -Ch4
Start .0000V
Stop .0000V
Step .0000V

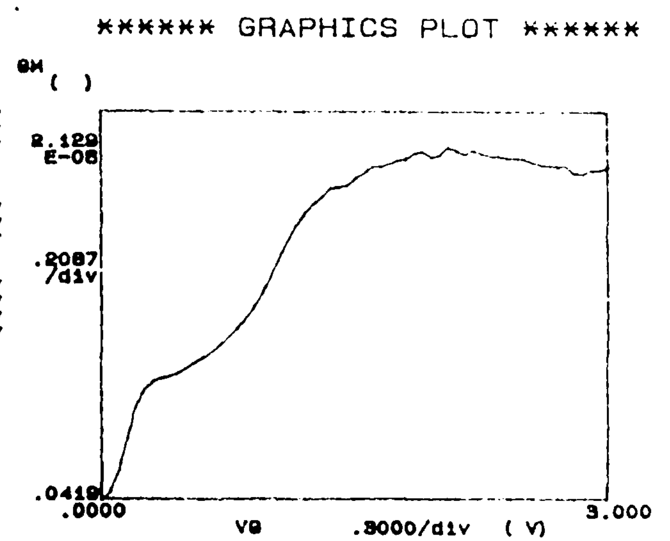
Constants:
VSS -Ch1 .0000V
VDD -Ch2 .1000V
VS1 -Vs1 .0000V
VS2 -Vs2 .0000V



Variable1:
VDD -Ch2
Linear sweep
Start .0000V
Stop 5.0000V
Step .0000V

Variable2:
VG -Ch3
Start .0000V
Stop 4.0000V
Step 1.0000V

Constants:
VSS -Ch1 .0000V
VBB -Ch4 .0000V
VS1 -Vs1 .0000V
VS2 -Vs2 .0000V

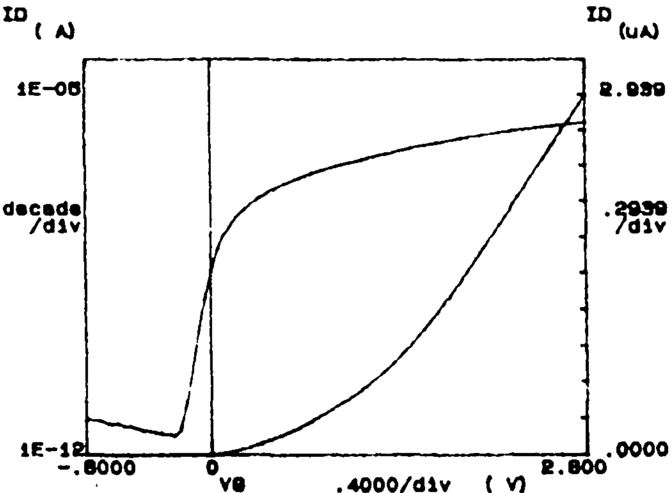


Variable1:
VG -Ch3
Linear sweep
Start .0000V
Stop 3.0000V
Step .0500V

Constants:
VSS -Ch1 .0000V
VDD -Ch2 .1000V
VBB -Ch4 .0000V
VS1 -Vs1 .0000V
VS2 -Vs2 .0000V

GM ( ) = ΔID/ΔVG

****** GRAPHICS PLOT ******



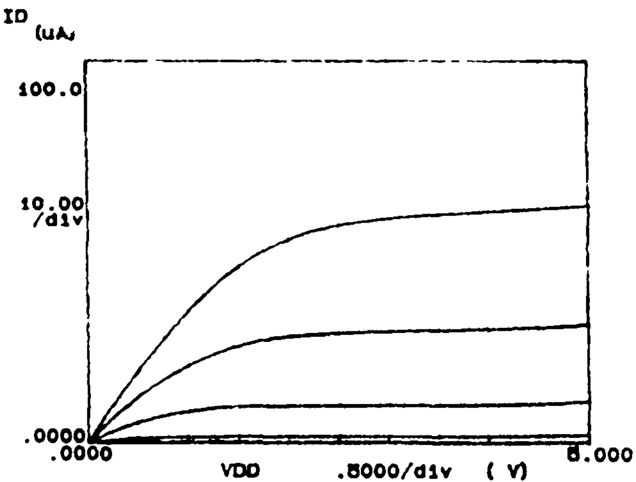
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 3.0000V
Step .0800V

Variable2:
VSS -Ch4
Start .0000V
Stop .0000V
Step .0000V

Constants:
VSS -Ch1 .0000V
VDD -Ch2 .1000V
VS1 -Vs1 .0000V
VS2 -Vs2 .0000V

Wafer 10
GAA m-ch
tox = 500 Å

****** GRAPHICS PLOT ******

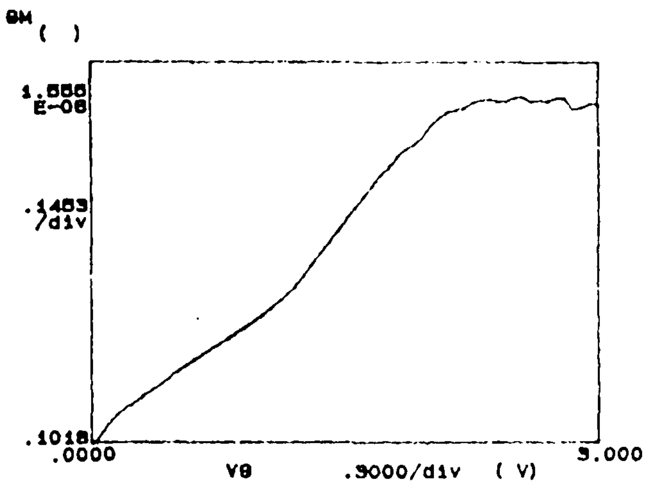


Variable1:
VDD -Ch2
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Variable2:
VG -Ch3
Start .0000V
Stop 4.0000V
Step 1.0000V

Constants:
VSS -Ch1 .0000V
VSS -Ch4 .0000V
VS1 -Vs1 .0000V
VS2 -Vs2 .0000V

****** GRAPHICS PLOT ******

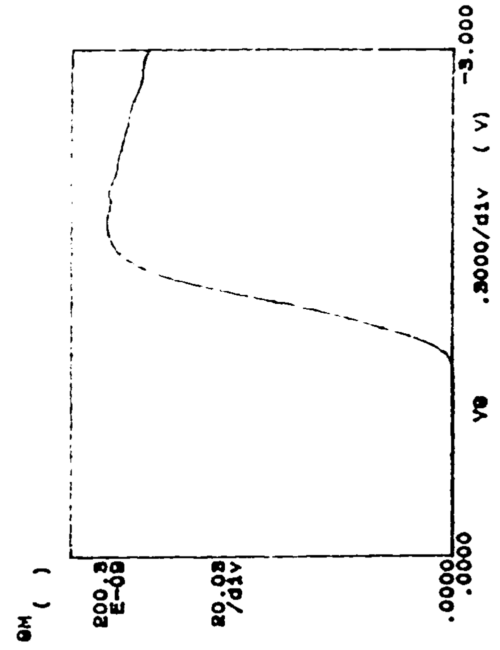


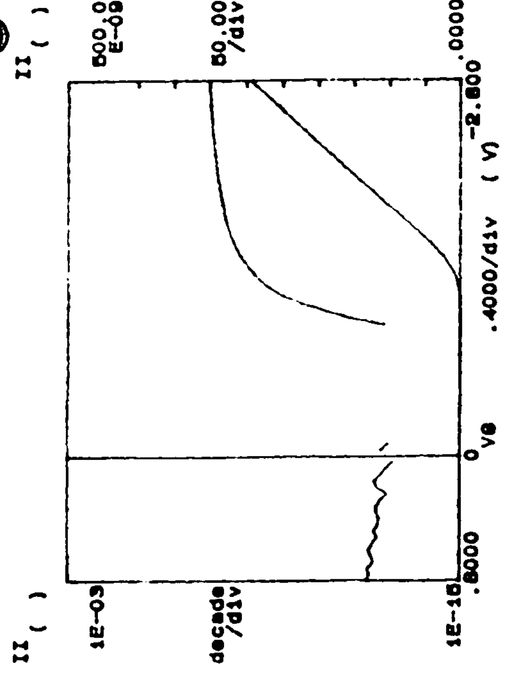
Variable1:
VG -Ch3
Linear sweep
Start .0000V
Stop 3.0000V
Step .0500V

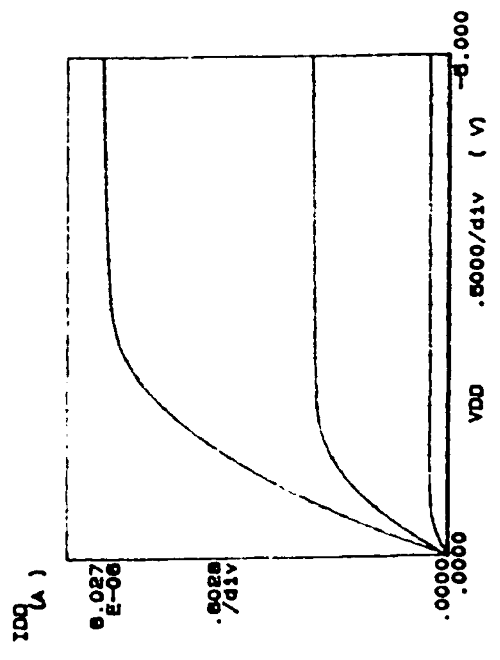
Constants:
VSS -Ch1 .0000V
VDD -Ch2 .1000V
VSS -Ch4 .0000V
VS1 -Vs1 .0000V
VS2 -Vs2 .0000V

GM ( ) = ΔID/ΔVG

Wafer 11
GAA P-ch
tox = 500 Å







CHIP LAYOUT

The following pages describe the layout of the GAA chip

6) Transistors with N/P source

W(UM)	L(UM)	NAME	SOURCE	GATE	DRAIN
10.0	3.0	H19	934	935	889
10.0	5.0	H20	936	890	891
50.0	3.0	H21	937	938	892
50.0	5.0	H22	939	893	894

7) Gate all-around transistors

a) Without etch

W(UM)	L(UM)	NAME	SOURCE	GATE	DRAIN
3.0	3.0	C23	359	358	297
3.0	5.0	C24	299	360	298
3.0	10.0	C25	362	361	300
4.0	3.0	C26	302	363	301
4.0	5.0	C27	365	364	303
4.0	10.0	C28	305	366	304

normal SOI

b) Etch L=2.0 UM

W(UM)	L(UM)	NAME	SOURCE	GATE	DRAIN
3.0	3.0	D25	481	480	419
3.0	5.0	D26	421	482	420
3.0	10.0	D27	484	483	422
4.0	3.0	D28	424	485	423
4.0	5.0	D29	487	486	425
4.0	10.0	D30	427	488	426

GAA

c) Etch L=3.0 UM

W(UM)	L(UM)	NAME	SOURCE	GATE	DRAIN
3.0	3.0	E29	603	602	541
3.0	5.0	E30	543	604	542
3.0	10.0	E31	606	605	544
4.0	3.0	E32	546	607	545
4.0	5.0	E33	609	608	547
4.0	10.0	E34	549	610	548

GAA

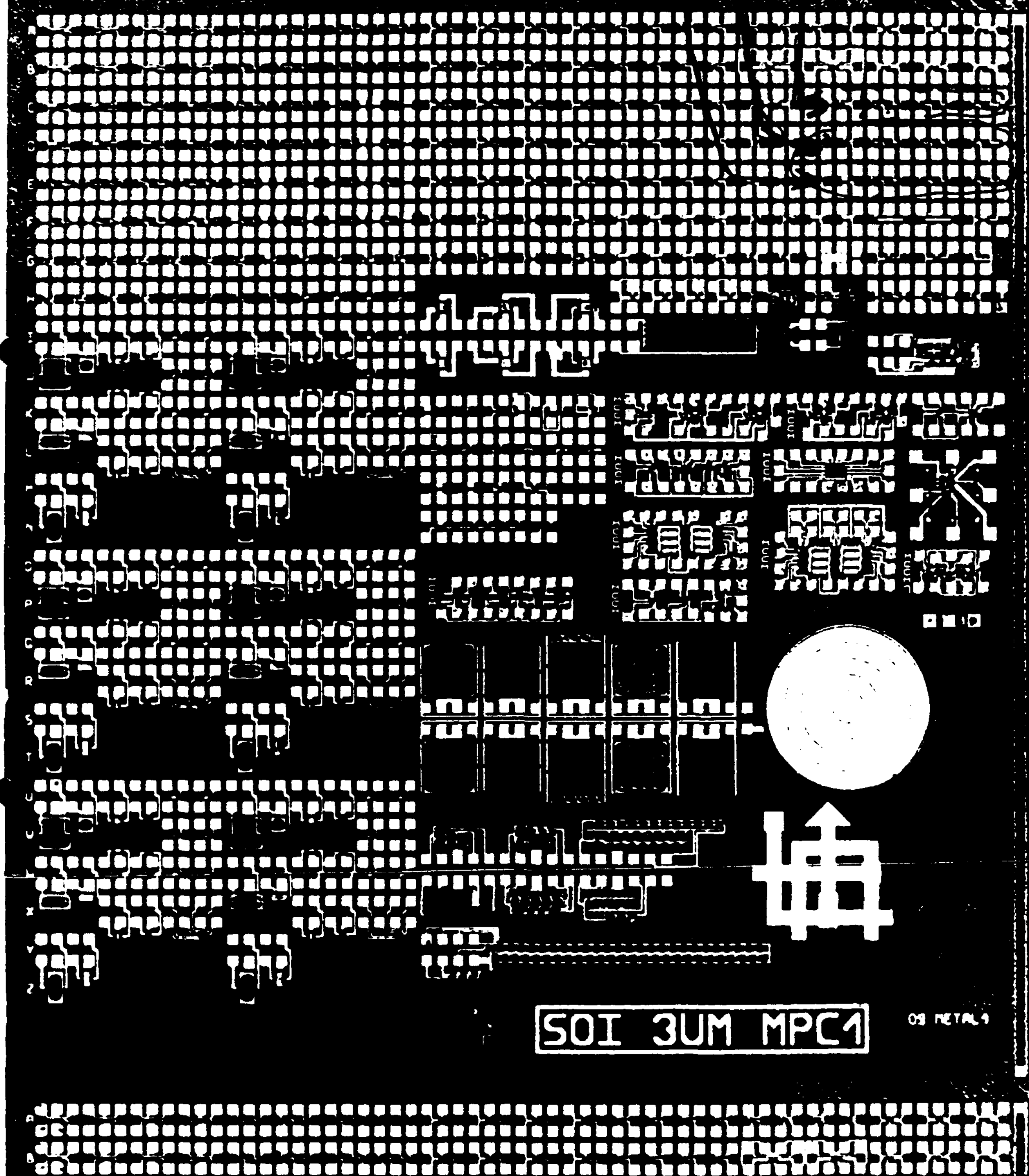
8) Input protections

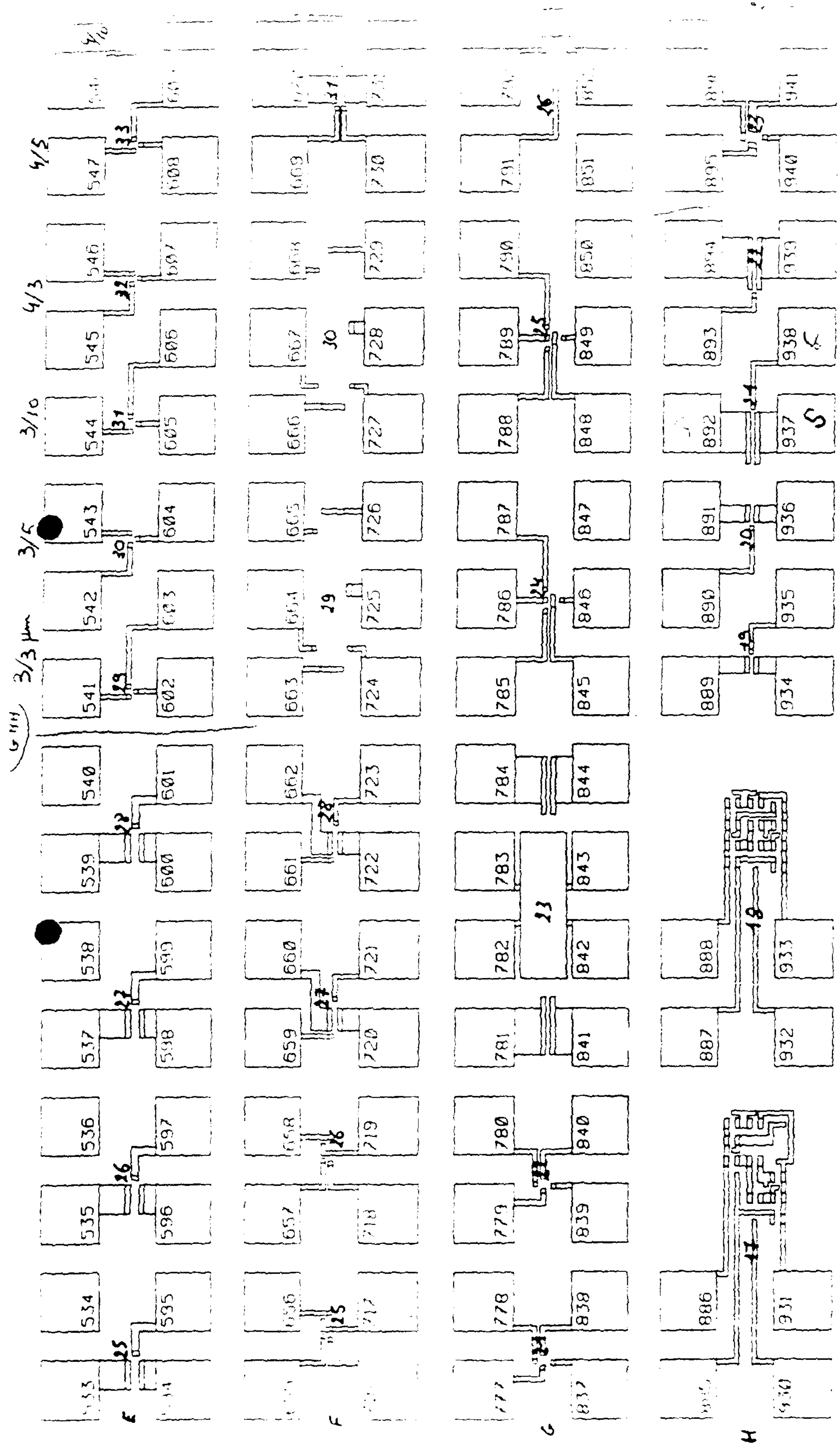
a) With PIN-diodes

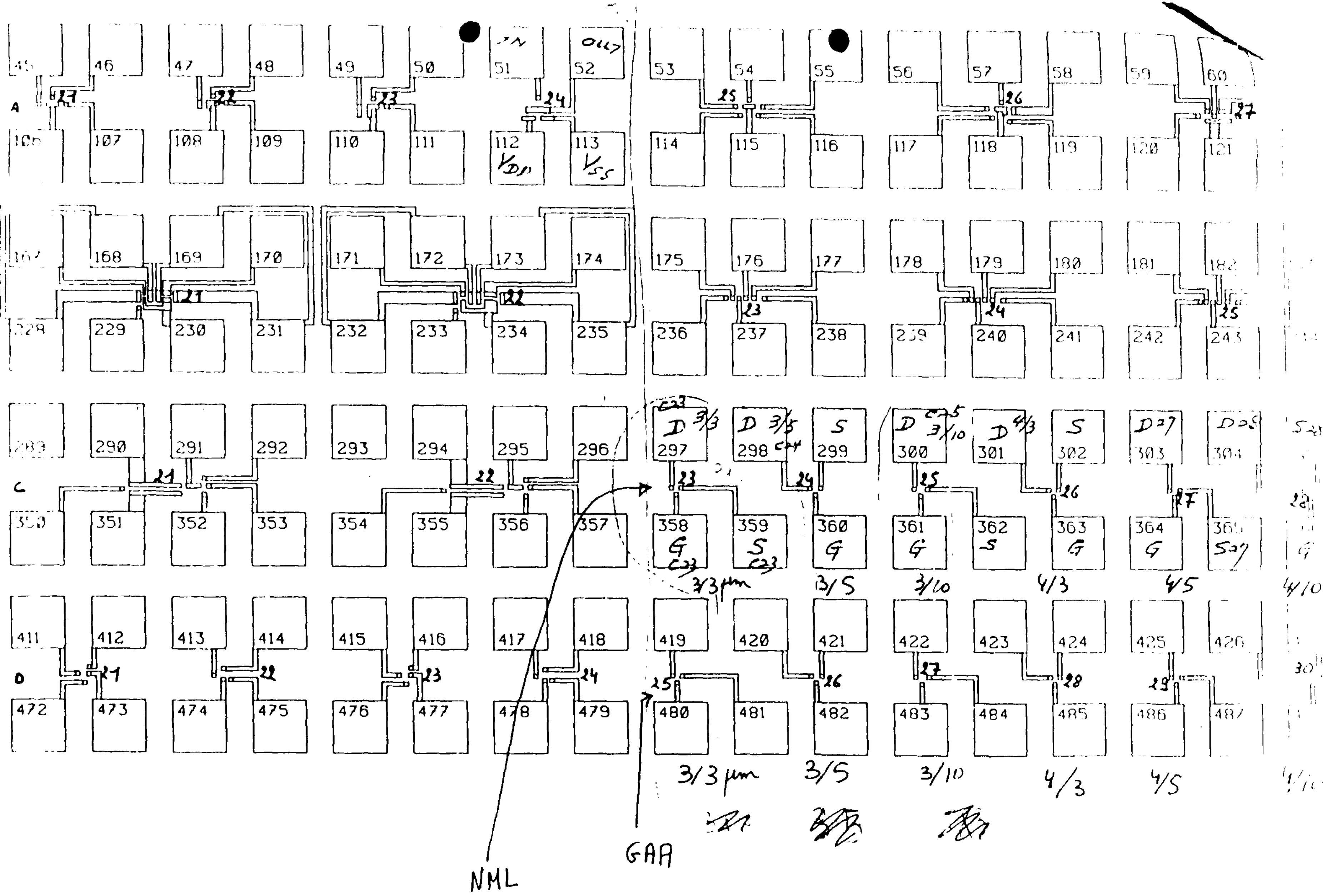
	NAME	IN	OUT1	OUT2	VDD	VSS
N+ RES	B1	125	186	184	123	185
P+ RES	B2	128	189	187	126	188
INT RES	B3	131	192	190	129	191
POLY RES	B4	134	195	193	132	194

b) With PNN-diodes

	NAME	IN	OUT1	OUT2	VDD	VSS
N+ RES	C1	247	308	306	245	307
P+ RES	B2	250	311	309	248	310
INT RES	B3	253	314	312	251	313
POLY RES	C4	256	317	315	254	316


SOI 3UM MPC1
SOI 3UM MPC1




A
3
C
D
VDD
VSS
3/3 µm
3/5
3/10
4/3
4/5
4/10
GAA
NML