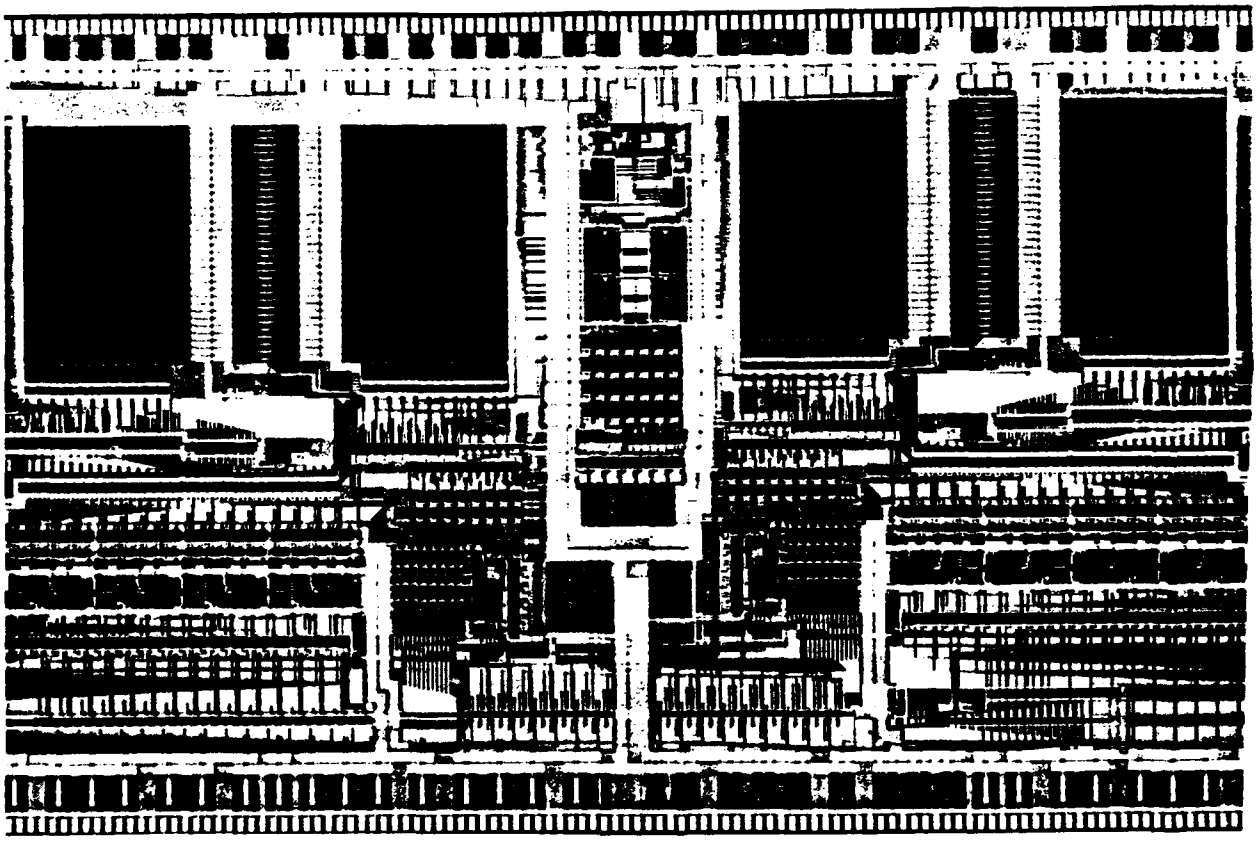
MCR-92-974

Project : Insertion Demonstrations of Digital Gallium Arsenide

CDRL Item A001

OBP-80 FINAL TECHNICAL REPORT

Volume 1/4 - Chip Set Schematics



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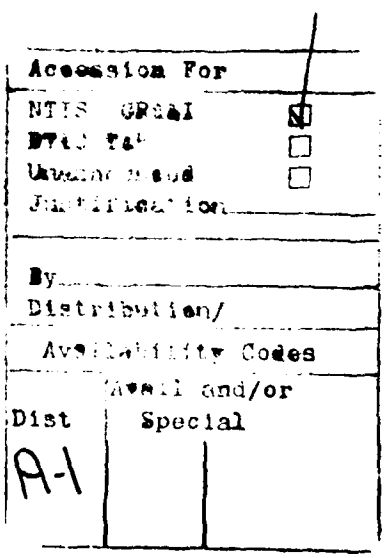
GLOSSARY

AALU	Address Arithmetic Logic Unit
ALU	Arithmetic Logic Unit
APG	Automatic Pattern Generation
ASIC	Application Specific Integrated Circuit
BCU	Bus Control Unit
BLM	Behavioral Language Model
CB	Communications Buffer
CDR	Critical Design Review
CMOS	Complementary Metal Oxide Semiconductor
CMOS/SOS	Complementary Metal Oxide Semiconductor/Silicon on Sapphire
CPU	Central Processing Unit
DALU	Data Arithmetic Logic Unit
DARPA	Defense Advanced Research Projects Administration
DC	Direct Current
DMSP	Defense Meteorological Satellite Program
DSP	Digital Signal Processing
FET	Field Effect Transistor
FIFO	First In First Out
FMEA	Failure Mode Effects Analysis
EDM	Engineering Development Model
GALU	Generic Arithmetic Logic Unit
GaAs	Gallium Arsenide
GTE	Ground Test Equipment
GFP	Government Furnished Property
I/O	Input/Output
IR&D	Independent Research and Development
MCS	Microcode Sequencer
MESFET	Metal Semiconductor Field Effect Transistor
MOPS	Million Operations Per Second
MOS	Metal Oxide Semiconductor
MPY	Multiplier Unit
MTBF	Mean Time Between Failures
NMOS	N channel Metal Oxide Semiconductor
NRL	Naval Research Laboratory
OBP	On Board Processor
OBP-80	On Board Processor - 80 MHz
OTS	Off The Shelf
PC	Personal Computer
PCA	Parts Characterization Analyzer
PCB	Printed Circuit Board
PDR	Preliminary Design Review
PIC	Priority Interrupt Controller
PS	Pipeline Slice
Qc	Critical Charge

RAM	Random Access Memory
SEU	Single Event Upset
SSI	Small Scale Integration
TMA	Timing Margin Analysis
TTL	Transistor - Transistor Logic
VLSI	Very Large Scale Integration
WBS	Work Breakdown Structure
WCA	Worst Case Analysis
WCS	Writable Control Store
WS	Working Store



APPLICABLE DOCUMENTS:

1. 'OBP ASSEMBLER USER'S MANUAL', Document ID = SSD-D-AS239, Item A016, Naval Research Laboratory.

2. 'OBP LINKER USER'S MANUAL', Document ID = SSD-D-AS239, Item A015, Naval Research Laboratory.

3. 'PAYLOAD DATA MANAGEMENT SYSTEM OBP-CPU PROGRAMMER'S REFERENCE MANUAL', Document ID = OB87A014-3, Item A014, Naval Research Laboratory.

4. 'Schematic Diagram - CPU', Document ID = AS-OP-5395, Naval Research Laboratory.

5. OBP80 Final Technical Report, Vol 1-4, Document ID = 849GOBP0100, Martin Marietta Defense Space & Communications.

FOREWORD

The OBP-80 is an Engineering Development Model (EDM) of a bit slice computer constructed by Martin Marietta Space Systems for the Naval Research Laboratory. The work described in this report was performed under contract N00014-89-C-2169, Insertion Demonstrations of Digital Gallium Arsenide - OBP Upgrade. The contract was performed in cooperation with the Defense Advanced Research Projects Agency technology insertion program for digital gallium arsenide.

This system has been developed to demonstrate, in a laboratory environment, an architecture that can be used to perform advanced signal processing functions onboard a spacecraft. Primary emphasis is placed on the transfer of an existing CMOS architecture to a higher performance, more radiation tolerant technology of Gallium Arsenide.

The following individuals provided technical direction and assistance:

Dr. Andrew J. Fox, Head, Advanced Systems Technology Branch, NRL
Dr. Arati Prabhakar, Director, Defense Sciences Office, DARPA
Dr. Alan Ross, Architecture Consultant

IDDGA Final Technical Report Volume 1 of 4 contains the chip set schematic diagrams.

This volume provides the schematic data which was used to generate the physical design of all seven VLSI components used in the OBP-80 EDM. It also presents top level graphical representations of the seven components. This data is provided as an aid to post-fabrication analysis.

The complete final technical report is composed of the following volumes:

Final Technical Report - Volume 1 of 4: Chip Set Schematic Diagrams

Final Technical Report - Volume 2 of 4: Chip Set Source Control Drawings

Final Technical Report - Volume 3 of 4: EDM Board Schematic Diagrams

Final Technical Report - Volume 4 of 4: OBP80 Software Model

1. INTRODUCTION

The OBP80 chip set is composed of the following circuits:

TABLE 1 OBP80 Chip Set Summary

DEVICE	PACKAGE	TRANSISTOR COUNT	EQUIVALENT GATES	POWER	I/O	MASK REVISION
GOBP001 - MPY VLSI	LDCC 256	27,105	9,035	3.35 W	43 GND, 27 VTT, 136 GaAs signal	Rev. A 7/15/91
GOBP002 - GALU VLSI	LDCC 344	73,564	24,521	6.6 W	80 GND, 36 VTT, 214 GaAs signal	Initial 3/15/91
GOBP003 - IPR VLSI	LDCC 344	26,600	8,867	4.4 W	64 GND,24 VTT,5 VREF, 112 ECL signal, 136 GaAs signal	Rev. A 7/30/91
GOBP004 - DMC VLSI	LDCC 344	14,887	4,962	2.95 W	77 GND,31 VTT,4 VREF, 102 ECL signal, 105 GaAs signal	Initial 3/15/91
GOBP005 - TICVLSI	LDCC 256	14,750	4,916			Initial 7/30/91
GOBP006 - COMM1 VLSI	LDCC 256	15,780	5,260		41 GND, 26 VTT, 15 PLUS5, 92 GaAs signal, 81 TTL signal	Initial 7/15/91
GOBP007 MCS VLSI	LDCC 344	37,094	12,364			Initial 8/15/91

The schematic diagrams provided in this manual are in Mentor Graphics Corporation format. The schematics provide a method for controlling design hierarchy within a CAE environment. Consequently, they do not resemble conventional 'flat' schematics very closely.

The designs are organized to help the reader quickly trace the hierarchy from top to bottom. The first sheet of each section contains a photomicrograph of the device with the major macrocells labeled. Following this header page, the integrated circuit macrocell symbols and schematics are presented alphabetically.

The macrocells are always presented in two pages. The macrocell symbol occurs first, and is always followed by a page schematic. The only exception to this is the represetation of the complete chip. Here, the first page is always the chip symbol. This is followed by a two sheet schematic. The first sheet serves as a block diagram of entire chip and the second schematic

page is exclusively reserved for I/O cells. The cells may be traced downward to transistor equivalents by indexing each macrocell element that occurs in the block diagram schematic.

A good example might be the Data Memory Controller, DMC. Consider the top level schematic of the DMC shown in Figure 1. In this figure, the arrow tails and heads represent sheet to sheet connections. Since sheet 2 contains only I/O cells, these signals are identified as primary inputs and outputs respectively. Figure 2 is used to confirm this, and to identify the voltage level of the interface (TTL, MM GaAs, ECL 100K).

Suppose one is concerned with the functionality or the timing of a particular logic block. Any functional block encountered in the schematics may be expanded for logic simulation, VSPICE simulation, or comparison with layout. To investigate the effects of loading on the 'Q' output of the DMA register shown in Figure 1, it is necessary to lookup the macrocell 'VOTEREG16' towards the rear of the DMC schematics.

Once there, it is easy to see that the 'VOTEREG16' macrocell is composed of 16 occurences of 'VOTEBIT' and one occurence of 'VOTEBUF'. Since the 'VOTEBUF' circuit appears to be buffering only the inputs, the output drive for the DMA register comes from the 'VOTEBIT' macrocell. Figure 3 shows the 'VOTEREG16' cell.

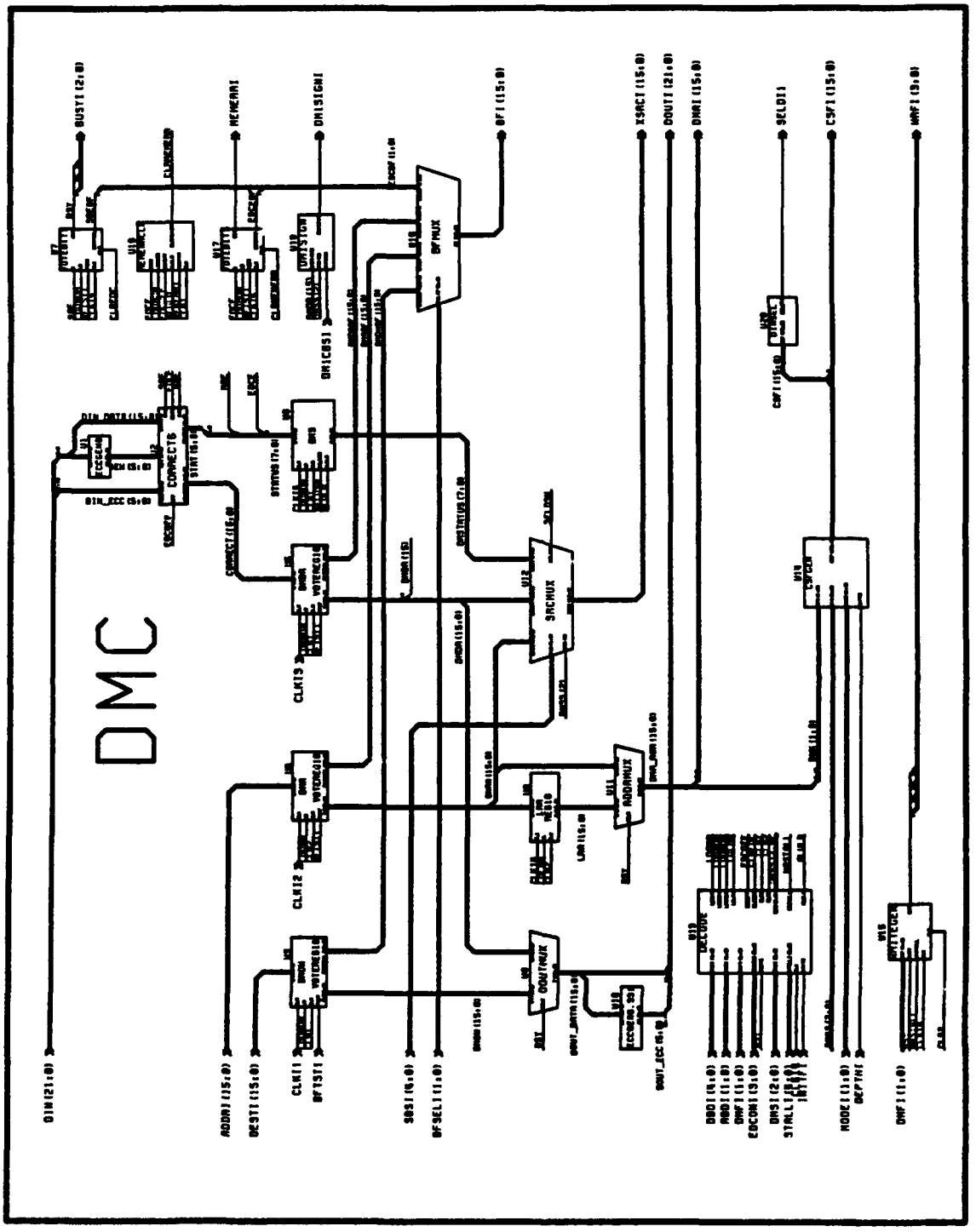


Figure 1 DMC Schematic Diagram, Page 1/2

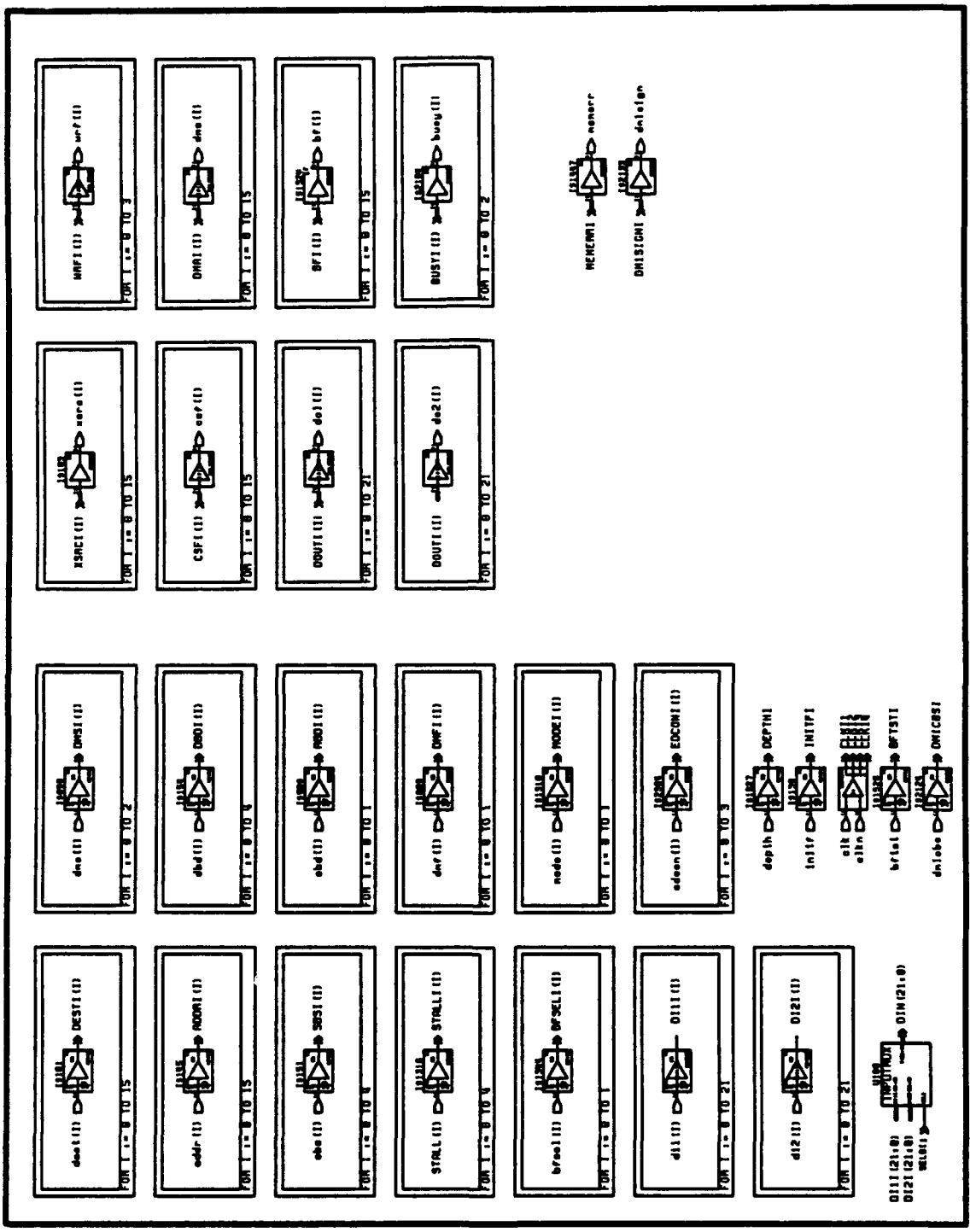


Figure 2 DMC Schematic Diagram, Page 2/2

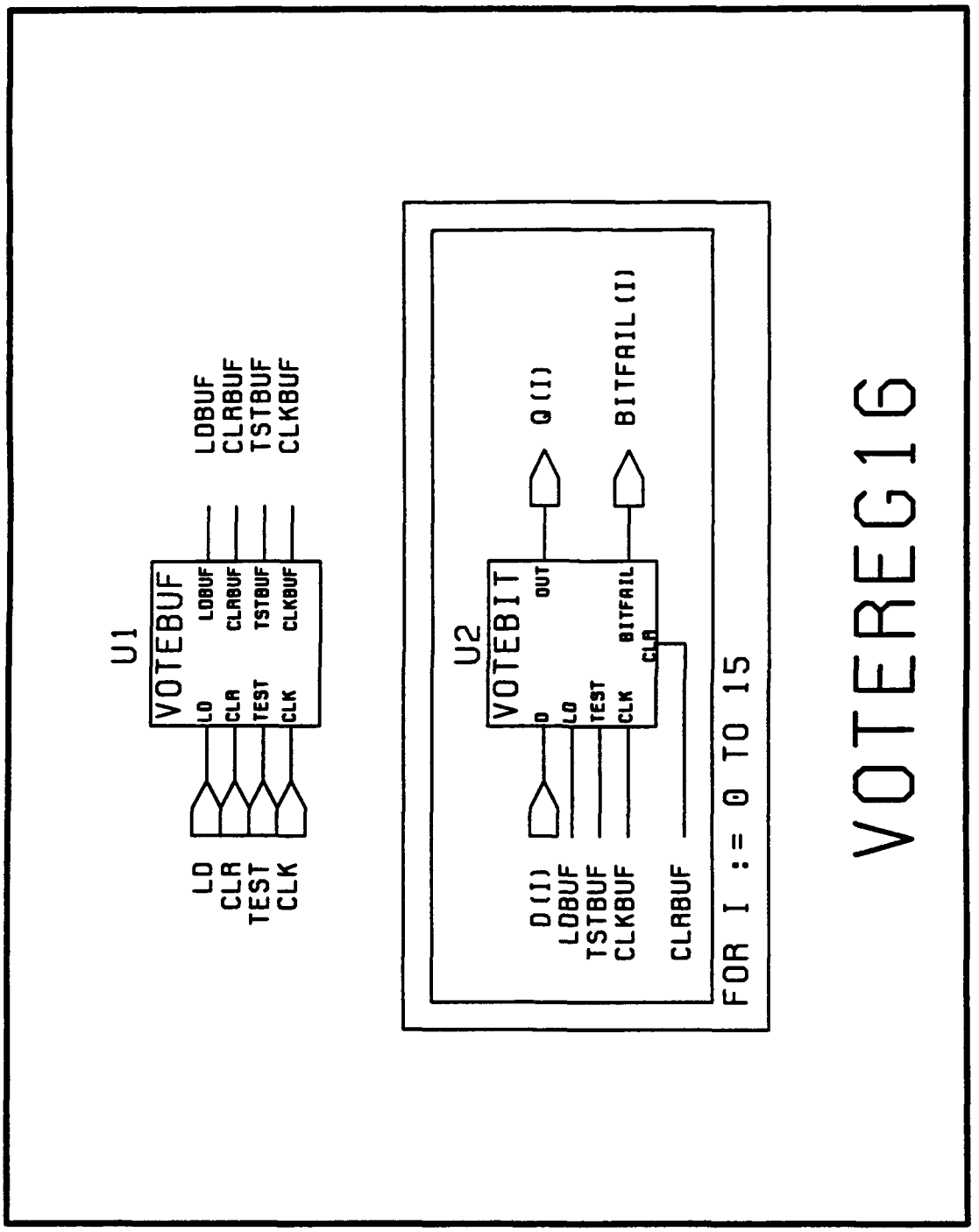


Figure 3 VOTEREG Macrocell Schematic Diagram

To locate the actual output drive capability of the 'VOTEBIT' macrocell, it is necessary to back up several pages in the alphabetized macrocell listing of schematics. Figure 4 at last locates the driver circuit for the DMA register. It is important to note that the feedback path load must also be added into the output delay.

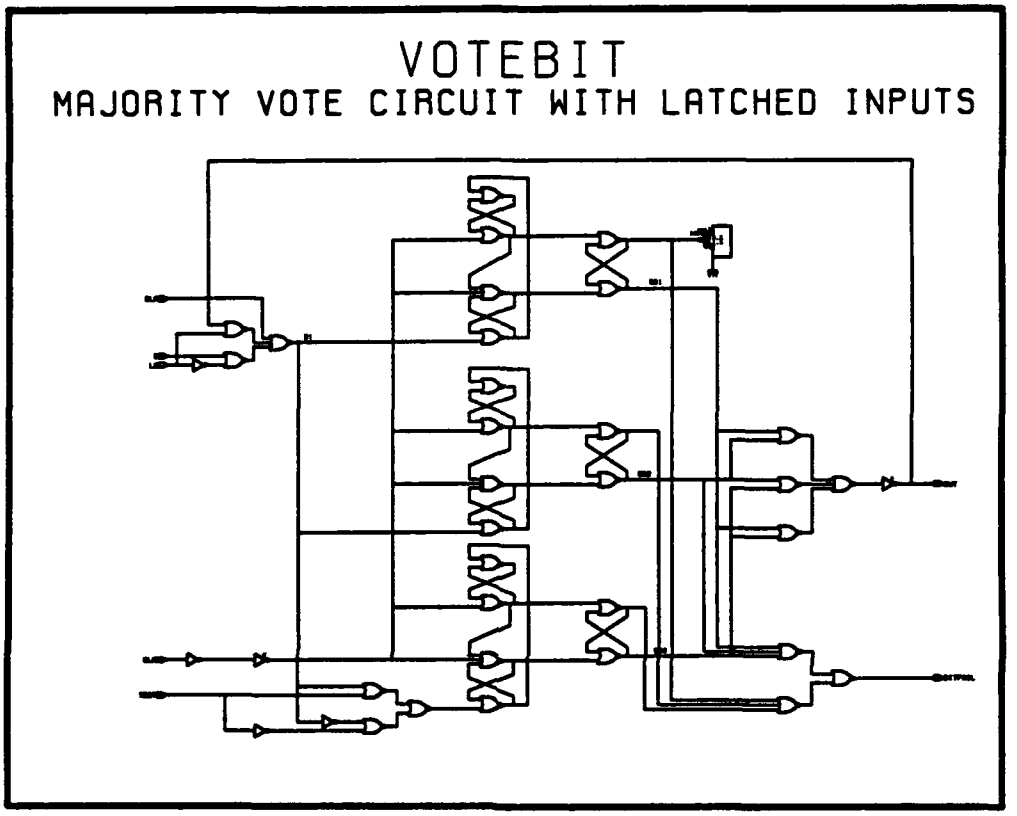


Figure 4 VOTEBIT Macrocell Schematic Diagram

The inverter output stage has the necessary properties attached to the symbol to determine the length/width ratio. A blowup of the inverter reveals that the output stage is actually a superinverter. This is seen by the 'S' designator shown on the inverter symbol in Figure 5. This symbol specifies the transistor topology shown in Figure 6.

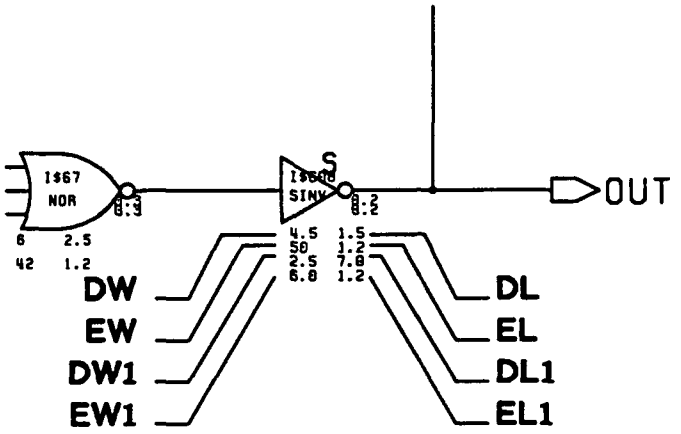


Figure 5 VOTEBIT Output Drive Inverter

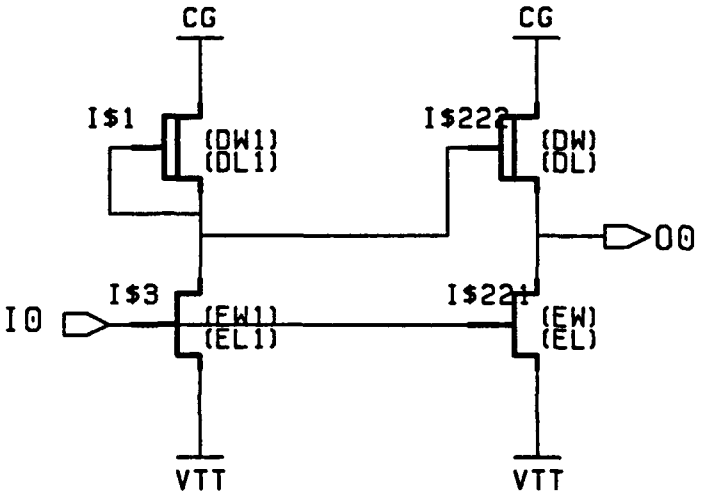


Figure 6 GaAs Super-Inverter Schematic

From Figures 5 and 6, it is easy to see the 'as-built' sizes of the transistors used in the super buffer. In a hierarchical schematic, the FET sizes are handed down to a generic super-inverter topology. The format is always that the widths appear on the left side of the symbol, and the lengths on the right. The depletion transistors always appear on top of the enhancements.

From the 'VOTEBIT' circuit directly, we can extract a VSPICE netlist. This was done using the Martin Marietta utilities mexpand and vspicenet. This produces only a netlist of the circuit. Figure 7 illustrates the generated netlist. The length of the circuit results directly from the number of transistors in 'VOTEBIT'. These can be summarized from:

```
* VSPICE netlist for VOTEBIT
*
* VOTEBIT SEU simulation 3/23/91
*
 .MODEL ENH NGAAS (KIND=1)
 .MODEL DEP NGAAS (KIND=4)
* power sources
VGND 1 0 -1.9
* circuit load
C1 538 546 2.2PF
B200 546 538 546 546 ENH W=50 L=1.2
B201 546 51 546 546 ENH W=50 L=1.2
* seu current pulse
ISEU  546 700 PULSE(.005P,0.6M,1NS,10P,10P,90P,10N)
VSEU 514 700 0
* zero value voltage sources
VCG 0 545 0
VTT 1 546 0
VCLR 53 0 -1.9
VLD 56 0 -1.9
VD 54 0 -1.9
VCLK 52 0 -1.4
VTST 542 0 -1.9
* initial conditions
.NODESET V(535) = -1.4 V(538) = -1.9
.NODESET V(522) = -1.4 V(55) = -1.9
.NODESET V(529) = -1.9 V(536) = -1.9
.NODESET V(530) = -1.9 V(539) = -1.4
.NODESET V(540) = -1.4 V(541) = -1.4
.NODESET V(526) = -1.9 V(527) = -1.9
.NODESET V(59) = -1.9 V(512) = -1.4
.NODESET V(515) = -1.4 V(524) = -1.4
.NODESET V(523) = -1.9 V(520) = -1.4
.NODESET V(57) = -1.9 V(58) = -1.4
*.NODESET V(51) = -1.9 V(510) = -1.9
.NODESET V(514) = -1.9 V(517) = -1.9
.NODESET V(528) = -1.9 V(518) = -1.4
.NODESET V(531) = -1.9 V(532) = -1.4
.NODESET V(543) = -1.85 V(544) = -0.6
.NODESET V(533) = -1.9 V(537) = -1.9
* SPICE Net List Extracted for Votebit
B1  532  55  546  546  ENH W=14 L=1.2
B2  532  532  545  546  DEP W=2 L=2.5
B3  525  542  546  546  ENH W=14 L=1.2
B4  525  525  545  546  DEP W=2 L=2.5
B5  534  56  546  546  ENH W=14 L=1.2
B6  534  534  545  546  DEP W=2 L=2.5
B7  537  52  546  546  ENH W=28 L=1.2
B8  537  537  545  546  DEP W=4 L=2.5
B9  51  57  546  546  ENH W=35 L=1.2
B10  51  58  546  546  ENH W=35 L=1.2
B11  51  51  545  546  DEP W=5 L=2.5
B12  529  539  546  546  ENH W=21 L=1.2
B13  529  540  546  546  ENH W=21 L=1.2
```

Figure 7 Extracted VSPICE Netlist for Votebit

```
B14   529   529   545   546   DEP W=3 L=2.5
B15   536   540   546   546   ENH W=21 L=1.2
B16   536   541   546   546   ENH W=21 L=1.2
B17   536   536   545   546   DEP W=3 L=2.5
B18   530   539   546   546   ENH W=21 L=1.2
B19   530   541   546   546   ENH W=21 L=1.2
B20   530   530   545   546   DEP W=3 L=2.5
B21   526   511   546   546   ENH W=28 L=1.2
B22   526   539   546   546   ENH W=28 L=1.2
B23   526   526   545   546   DEP W=4 L=2.5
B24   539   526   546   546   ENH W=42 L=1.2
B25   539   514   546   546   ENH W=42 L=1.2
B26   539   539   545   546   DEP W=6 L=2.5
B27   527   516   546   546   ENH W=28 L=1.2
B28   527   540   546   546   ENH W=28 L=1.2
B29   527   527   545   546   DEP W=4 L=2.5
B30   540   527   546   546   ENH W=42 L=1.2
B31   540   528   546   546   ENH W=42 L=1.2
B32   540   540   545   546   DEP W=6 L=2.5
B33   59   519   546   546   ENH W=28 L=1.2
B34   59   541   546   546   ENH W=28 L=1.2
B35   59   59   545   546   DEP W=4 L=2.5
B36   541   59   546   546   ENH W=42 L=1.2
B37   541   531   546   546   ENH W=42 L=1.2
B38   541   541   545   546   DEP W=6 L=2.5
B39   510   512   546   546   ENH W=21 L=1.2
B40   510   511   546   546   ENH W=21 L=1.2
B41   510   510   545   546   DEP W=3 L=2.5
B42   511   510   546   546   ENH W=35 L=1.2
B43   511   513   546   546   ENH W=35 L=1.2
B44   511   511   545   546   DEP W=5 L=2.5
B45   512   514   546   546   ENH W=21 L=1.2
B46   512   55   546   546   ENH W=21 L=1.2
B47   512   512   545   546   DEP W=3 L=2.5
B48   517   515   546   546   ENH W=21 L=1.2
B49   517   516   546   546   ENH W=21 L=1.2
B50   517   517   545   546   DEP W=3 L=2.5
B51   516   517   546   546   ENH W=35 L=1.2
B52   516   513   546   546   ENH W=35 L=1.2
B53   516   516   545   546   DEP W=5 L=2.5
B54   515   528   546   546   ENH W=21 L=1.2
B55   515   55   546   546   ENH W=21 L=1.2
B56   515   515   545   546   DEP W=3 L=2.5
B57   518   520   546   546   ENH W=21 L=1.2
B58   518   519   546   546   ENH W=21 L=1.2
B59   518   518   545   546   DEP W=3 L=2.5
B60   519   518   546   546   ENH W=35 L=1.2
B61   519   513   546   546   ENH W=35 L=1.2
B62   519   519   545   546   DEP W=5 L=2.5
B63   520   531   546   546   ENH W=21 L=1.2
B64   520   533   546   546   ENH W=21 L=1.2
B65   520   520   545   546   DEP W=3 L=2.5
B66   533   524   546   546   ENH W=14 L=1.2
B67   533   523   546   546   ENH W=14 L=1.2
```

Figure 7 Extracted VSPICE Netlist for Votebit (Con't)

```
B68   533   533   545   546   DEP W=2 L=2.5
B69   524   55   546   546   ENH W=14 L=1.2
B70   524   542   546   546   ENH W=14 L=1.2
B71   524   524   545   546   DEP W=2 L=2.5
B72   523   532   546   546   ENH W=14 L=1.2
B73   523   525   546   546   ENH W=14 L=1.2
B74   523   523   545   546   DEP W=2 L=2.5
B75   522   538   546   546   ENH W=14 L=1.2
B76   522   56   546   546   ENH W=14 L=1.2
B77   522   522   545   546   DEP W=2 L=2.5
B78   521   54   546   546   ENH W=14 L=1.2
B79   521   534   546   546   ENH W=14 L=1.2
B80   521   521   545   546   DEP W=2 L=2.5
B81   543   535   546   546   ENH W=6.0 L=1.2
B82   538   535   546   546   ENH W=50 L=1.2
B83   543   543   545   546   DEP W=2.5 L=7.0
B84   538   543   545   546   DEP W=4.5 L=1.5
B85   544   537   546   546   ENH W=6.0 L=1.2
B86   513   537   546   546   ENH W=50 L=1.2
B87   544   544   545   546   DEP W=2.5 L=7.0
B88   513   544   545   546   DEP W=4.5 L=1.5
B89   535   529   546   546   ENH W=42 L=1.2
B90   535   536   546   546   ENH W=42 L=1.2
B91   535   530   546   546   ENH W=42 L=1.2
B92   535   535   545   546   DEP W=6 L=2.5
B93   57   539   546   546   ENH W=14 L=1.2
B94   57   540   546   546   ENH W=14 L=1.2
B95   57   541   546   546   ENH W=14 L=1.2
B96   57   57   545   546   DEP W=2 L=2.5
B97   58   526   546   546   ENH W=14 L=1.2
B98   58   527   546   546   ENH W=14 L=1.2
B99   58   59   546   546   ENH W=14 L=1.2
B100   58   58   545   546   DEP W=2 L=2.5
B101   514   511   546   546   ENH W=28 L=1.2
B102   514   513   546   546   ENH W=28 L=1.2
B103   514   512   546   546   ENH W=28 L=1.2
B104   514   514   545   546   DEP W=4 L=2.5
B105   528   516   546   546   ENH W=28 L=1.2
B106   528   513   546   546   ENH W=28 L=1.2
B107   528   515   546   546   ENH W=28 L=1.2
B108   528   528   545   546   DEP W=4 L=2.5
B109   531   519   546   546   ENH W=28 L=1.2
B110   531   513   546   546   ENH W=28 L=1.2
B111   531   520   546   546   ENH W=28 L=1.2
B112   531   531   545   546   DEP W=4 L=2.5
B113   55   53   546   546   ENH W=35 L=1.2
B114   55   522   546   546   ENH W=35 L=1.2
B115   55   521   546   546   ENH W=35 L=1.2
B116   55   55   545   546   DEP W=5 L=2.5
B117   546   526   546   546   DEP W=3.5 L=1.5
*****   LIST OF MODELS USED   *****
*                ENH
*                DEP
*
```

Figure 7 Extracted VSPICE Netlist for Votebit (Con't)

```
* LIST OF REPLACED NAMES.
*
* I$592/I$3/B1 ==> B1
* I$592/I$1/B1 ==> B2
* I$1263/I$3/B1 ==> B3
* I$1263/I$1/B1 ==> B4
* I$1261/I$3/B1 ==> B5
* I$1261/I$1/B1 ==> B6
* I$901/I$3/B1 ==> B7
* I$901/I$1/B1 ==> B8
* I$106/I$3/B1 ==> B9
* I$106/I$2/B1 ==> B10
* I$106/I$1/B1 ==> B11
* I$57/I$3/B1 ==> B12
* I$57/I$2/B1 ==> B13
* I$57/I$1/B1 ==> B14
* I$58/I$3/B1 ==> B15
* I$58/I$2/B1 ==> B16
* I$58/I$1/B1 ==> B17
* I$59/I$3/B1 ==> B18
* I$59/I$2/B1 ==> B19
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* I$20/I$3/B1 ==> B21
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* I$36/I$1/B1 ==> B32
* I$52/I$3/B1 ==> B33
* I$52/I$2/B1 ==> B34
* I$52/I$1/B1 ==> B35
* I$51/I$3/B1 ==> B36
* I$51/I$2/B1 ==> B37
* I$51/I$1/B1 ==> B38
* I$1141/I$3/B1 ==> B39
* I$1141/I$2/B1 ==> B40
* I$1141/I$1/B1 ==> B41
* I$15/I$3/B1 ==> B42
* I$15/I$2/B1 ==> B43
* I$15/I$1/B1 ==> B44
* I$581/I$3/B1 ==> B45
* I$581/I$2/B1 ==> B46
* I$581/I$1/B1 ==> B47
* I$1144/I$3/B1 ==> B48
* I$1144/I$2/B1 ==> B49
* I$1144/I$1/B1 ==> B50
* I$586/I$3/B1 ==> B51
* I$586/I$2/B1 ==> B52
```

Figure 7 Extracted VSPICE Netlist for Votebit (Con't)

```
* I$586/I$1/B1 ==> B53
* I$585/I$3/B1 ==> B54
* I$585/I$2/B1 ==> B55
* I$585/I$1/B1 ==> B56
* I$1146/I$3/B1 ==> B57
* I$1146/I$2/B1 ==> B58
* I$1146/I$1/B1 ==> B59
* I$590/I$3/B1 ==> B60
* I$590/I$2/B1 ==> B61
* I$590/I$1/B1 ==> B62
* I$589/I$3/B1 ==> B63
* I$589/I$2/B1 ==> B64
* I$589/I$1/B1 ==> B65
* I$114/I$3/B1 ==> B66
* I$114/I$2/B1 ==> B67
* I$114/I$1/B1 ==> B68
* I$112/I$3/B1 ==> B69
* I$112/I$2/B1 ==> B70
* I$112/I$1/B1 ==> B71
* I$113/I$3/B1 ==> B72
* I$113/I$2/B1 ==> B73
* I$113/I$1/B1 ==> B74
* I$596/I$3/B1 ==> B75
* I$596/I$2/B1 ==> B76
* I$596/I$1/B1 ==> B77
* I$595/I$3/B1 ==> B78
* I$595/I$2/B1 ==> B79
* I$595/I$1/B1 ==> B80
* I$608/I$3/B1 ==> B81
* I$608/I$221/B1 ==> B82
* I$608/I$1/B1 ==> B83
* I$608/I$222/B1 ==> B84
* I$605/I$3/B1 ==> B85
* I$605/I$221/B1 ==> B86
* I$605/I$1/B1 ==> B87
* I$605/I$222/B1 ==> B88
* I$67/I$3/B1 ==> B89
* I$67/I$2/B1 ==> B90
* I$67/I$261/B1 ==> B91
* I$67/I$1/B1 ==> B92
* I$101/I$3/B1 ==> B93
* I$101/I$2/B1 ==> B94
* I$101/I$261/B1 ==> B95
* I$101/I$1/B1 ==> B96
* I$10?/I$3/B1 ==> B97
* I$ I$2/B1 ==> B98
* I$ I$261/B1 ==> B99
* I$102/I$1/B1 ==> B100
* I$1142/I$3/B1 ==> B101
* I$1142/I$2/B1 ==> B102
* I$1142/I$261/B1 ==> B103
* I$1142/I$1/B1 ==> B104
* I$1143/I$3/B1 ==> B105
* I$1143/I$2/B1 ==> B106
```

Figure 7 Extracted VSPICE Netlist for Votebit (Con't)

```
* I$1143/I$261/B1 ==> B107
* I$1143/I$1/B1 ==> B108
* I$1145/I$3/B1 ==> B109
* I$1145/I$2/B1 ==> B110
* I$1145/I$261/B1 ==> B111
* I$1145/I$1/B1 ==> B112
* I#/I$3/B1 ==> B113
* I#/I$2/B1 ==> B114
* I#/I$261/B1 ==> B115
* I#/I$1/B1 ==> B116
* I$944/B1 ==> B117
* NETLIST COMPLETED *
* run control
.TEMP=95
.TRAN 20PS 5NS
.OPTIONS LIMPTS=1000
.PRINT TRAN  V(535) V(529) V(511) V(526) V(539) V(514) I(VSEU)
.END
```

Figure 7 Extracted VSPICE Netlist for Votebit (Con't)

4 Inverters x 2 FET's/Inverter	= 8 FET's
2 Super-Inverters x 4 FET's/Super-Inverter	= 8 FET's
7 NOR3 x 4 FET's/NOR3	= 28 FET's
24 NOR2 x 3 FET's/NOR2	= 72 FET's
1 Isolated FET	= 1 FET
TOTAL	= 117 FET's

From the information contained on two primitive instances shown in Figure 5, we can easily identify their transistors in the VSPICE netlist. Notice the NOR3 gate is instance number I$67 and that the super-inverter is instance I$608. We expect to find 1 D mode transistor and 3 E mode transistors for the NOR 3, and two of each type for the super-inverter. Included at the back end of the netlist is a set of 'comments' which map the instance names into the actual VSPICENET transistor designation.

Consider the case of the super-inverter specification of Figure 6. This generic schematic has four instances within it: I$1, I$3, I$222, and I$221. Since their could be many instances of the super-inverter used in the DMC, we need to specify only that super-inverter which has been 'programmed' with the sizes from the 'VOTEBIT' application. Therefore, the instances we are looking for are I$608/I$1, I$608/I$3, etc. The comment list identifies that the FET's that implement the super-inverter in the VSPICE netlist are B81, B82, B83, and B84.

This netlist can now be used to simulate the circuit in various applications by appending the correct stimulus file. For example, it is possible to determine the critical charge needed to upset the 'VOTEBIT'. One potential weakness for any majority vote latch is to be struck in one of the single points of the feedback path that occur after the vote circuitry. It is known that only 60 fC of charge is needed to upset the latch elements. It is interesting to speculate how much charge is required to upset the circuit if the super-inverter or the NOR3 is struck.

Recall that the feedback path of the latch is loaded with the output load capacitance, and is driven by the super-inverter. This constitutes the SEU pulse swallowing filter which helps the 'VOTEBIT' resist SEU.

To locate the actual capacitance found on a node, we only have to look up the results from the Silvar-Lisco NCA parametric extraction run. We started out by trying to locate the DMA register circuit for simulation. We found this register on the top level schematic diagram of Figure 1. Notice that the output of the DMA register feeds a bus named 'DMAA(15:0)'. To properly simulate the sircuit, we investigate the capacitance connected to each element of this bus.

Figure 8 contains a small portion of the parametric extractor output. A few busses of interest are shown. The parametric extractor calculates these values based the physical sizes of the load devices, and on a configuration table that identifies interconnect parallel plate and fringing capacitance. The resulting capacitances are shown for parallel plate and total node capacitance in FemtoFarads.

The bus name, X and Y coordinates of the bus origin, and capacitive values make it easy to identify the load spread on the DMAA bus. We see that the VOTEBIT is connected to a bus that exhibits between 1.9 pF and 2.7 pF of total load capacitance. The squirt buffer structure was chosen to drive this load capacitance spread. The capacitive variation arises from the interconnect, sinc ethe number of, and physical size of the loads are identical for each signal in the DMAA bus. Thus, chip designs can be speed limited by elements not visible on the schematic.

The capacitive value of 2.2 pF was chosen for the simulation. The VSPICE statements which drive the simulation for this case are shown in the netlist of Figure 7. Iterative SPICE simulations were run until two simulations were achieved that bound the critical charge of the circuit. The results of these simulations are shown in Figure 9.

These simulations indicate an approximate critical charge of fC. This should be comapred against the intrinsic critical charge of a latch element, 60 fC.

3-27-91 N C A E P C N O D E R E P O R T F O R E P E

NODE NAME	COORDINATES		TOTAL CAPACITANCE	
	X	Y	XCAP	CAP
(DMAA<0>)	8308.50	1458.00	221.129	1913.963
(DMAA<10>)	6858.50	1458.00	291.401	2234.483
(DMAA<11>)	6728.50	1458.00	326.537	2506.187
(DMAA<12>)	6568.50	1458.00	303.113	2296.859
(DMAA<13>)	6438.50	1458.00	342.153	2584.731
(DMAA<14>)	6278.50	1458.00	314.825	2359.659
(DMAA<15>)	6148.50	1458.00	351.913	2654.875
(DMAA<1>)	8178.50	1458.00	238.697	2137.987
(DMAA<2>)	8018.50	1458.00	236.745	1979.219
(DMAA<3>)	7888.50	1458.00	258.217	2207.147
(DMAA<4>)	7728.50	1458.00	252.361	2044.475
(DMAA<5>)	7598.50	1458.00	277.737	2276.307
(DMAA<6>)	7438.50	1458.00	267.977	2112.187
(DMAA<7>)	7308.50	1458.00	295.305	2349.947
(DMAA<8>)	7148.50	1458.00	279.689	2172.107
(DMAA<9>)	7018.50	1458.00	310.921	2428.067
(XSRCI<0>)	9892.50	519.50	101.002	1792.325
(XSRCI<10>) ...	8116.00	519.50	93.194	1483.555
(XSRCI<11>) ...	7834.00	519.50	97.098	1416.733
(XSRCI<12>) ...	7416.00	519.50	101.002	1455.859
(XSRCI<13>) ...	7384.50	519.50	101.002	1434.699
(XSRCI<14>) ...	7108.00	519.50	83.434	1484.761
(XSRCI<15>) ...	7076.50	519.50	83.434	1463.601
(XSRCI<1>)	9610.50	519.50	101.002	1749.885
(XSRCI<2>)	9579.00	519.50	108.810	1754.269
(XSRCI<3>)	9297.00	519.50	108.810	1713.949
(XSRCI<4>)	9265.50	519.50	116.618	1718.333
(XSRCI<5>)	8879.00	519.50	89.290	1439.211
(XSRCI<6>)	8847.50	519.50	89.290	1435.315
(XSRCI<7>)	8461.00	519.50	89.290	1369.659
(XSRCI<8>)	8429.50	519.50	89.290	1433.403
(XSRCI<9>)	8147.50	519.50	89.290	1363.651
(DMAI<0>)	13104.50	519.50	24.874	1963.229
(DMAI<10>)	11328.00	519.50	24.874	1866.733
(DMAI<11>)	11178.50	519.50	24.874	1893.373
(DMAI<12>)	11014.50	519.50	28.778	1864.421
(DMAI<13>)	10865.00	519.50	28.778	1889.877
(DMAI<1>)	12955.00	519.50	24.874	1989.869
(DMAI<2>)	12791.00	519.50	20.970	1952.517
(DMAI<3>)	12641.50	519.50	20.970	1979.749
(DMAI<4>)	12373.00	519.50	17.066	1910.429
(DMAI<5>)	12223.50	519.50	17.066	1939.156
(DMAI<6>)	12059.50	519.50	17.066	1904.213
(DMAI<7>)	11910.00	519.50	17.066	1929.887
(DMAI<8>)	11746.00	519.50	20.970	1901.605
(DMAI<9>)	11596.50	519.50	20.970	1927.653
(CSFI<0>)	12972.00	7184.00	37.088	2505.721
(CSFI<10>)	12123.00	5847.00	52.704	2420.593

Figure 8 Partial Output from Electrical Parameter Extractor (EPE) Run for DMC

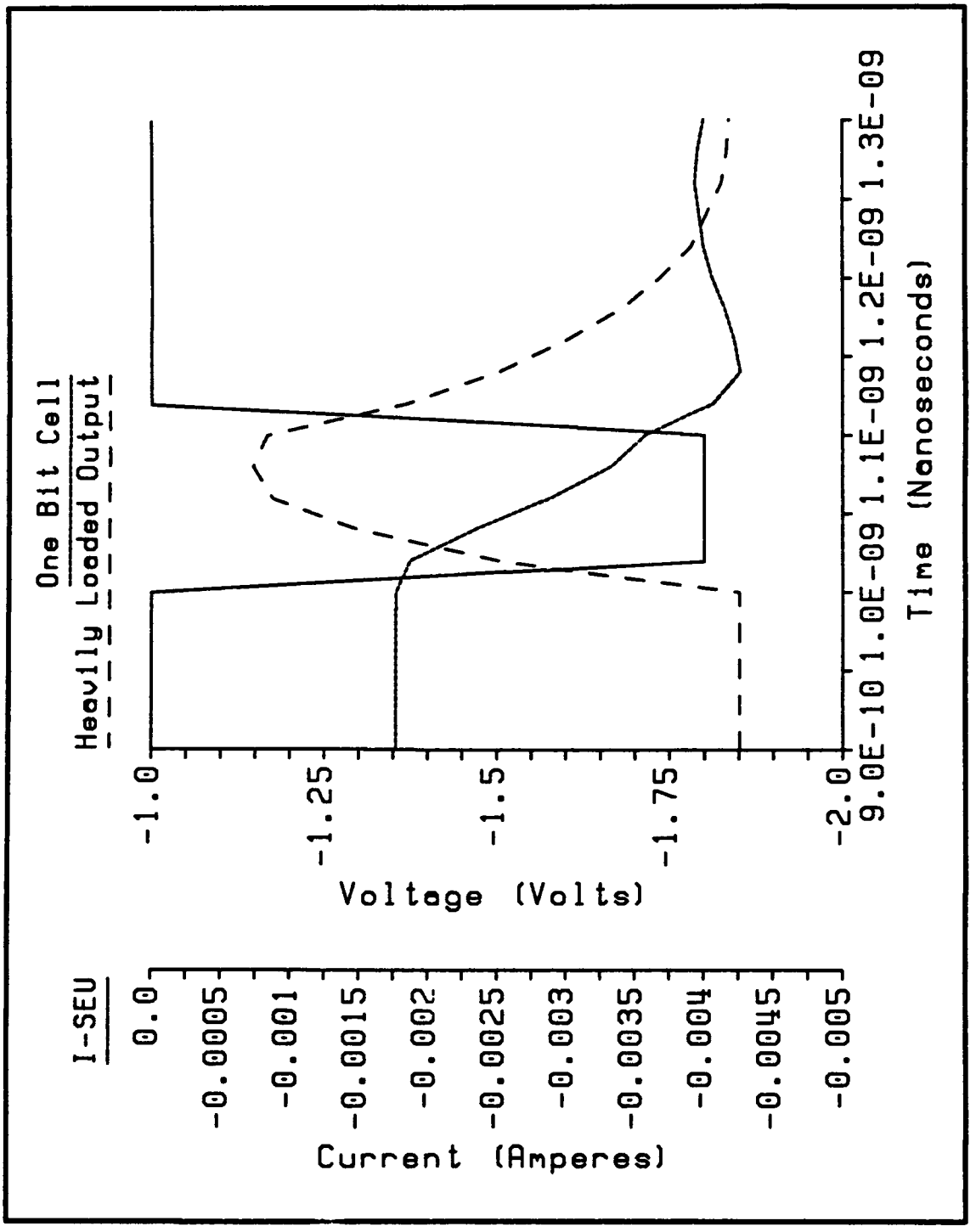


Figure 9 VOTEBIT SEU Simulation

Figure 9 is a simulation of the critical charge of the VOTEBIT. The trapezoidal pulse is an estimation of the amount of current produced during a single event upset. The current arises from the gate electric field sweeping the free carriers that were produced by ionization into the conduction channel. This current is expressed in Coulombs/second (Amperes) for a given time period. Since the duration of the event is thought to be fast, a 100 pS pulse was used. Thus the simulated charge deposition is represented by the area under the waveform.

The simulation results shown the inpact of depositing the SEU current pulse at differnt points in the circuit. If the current pulse is deposited on the 2.2 pF output node of the VOTEBIT register, no upset occurs. The current level is high enough to preturb the output, but not high enough or long enough to be loaded into the registers. This indicates that it is extremely difficult to upset the majority vote register from a hit to the logic that votes the output.

If the same current pulse is deposited into one of the internal nodes that is loaded with only 100 Femtofarads or so, an upset easily occurs. The upset occurs with deposited charge as little as 1/10 of the current shown in the figure, or approximately 40 fC. This indicates that the individual bits are very soft.

Thus, the following charcateristics are expected:

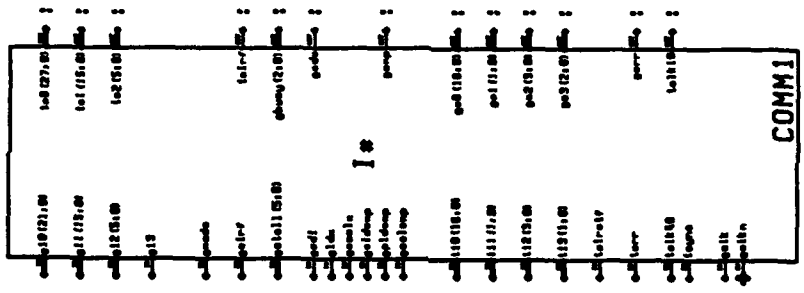
1. The individual bits will be upsetable by a much larger number of particles than 2 micron CMOS. This is because the particle spectrum in Earth orbit contains a large number ($\sim 10^2$ particles/cm) of low enengy particles that would normally not cause an upset in that technology.

2. The individual GaAs bits will exhibit a much lower critical charge than two micron CMOS. This results from from geometry (1.2 micron gate legth) and electric field intensity (gate voltage of 0.6 V instead of 5.0 V).

3. The VOTEBIT will not be sensitive to SEU hits in the logic where the vote is performed, nor will it propagate back into the individual storage elements.

4. The 'in circuit' hardness of the VOTEBIT element will be proportional to the operating clock speed. This follows since the scrub repition rate is increasing, and there appear to be no single points of sensitivity.

The previous analysis is indicitive of the ways in which the schematics for the OBP80 Chipset can be used. The actual SEU response of the VOTEBIT should be determined by experimentation. The schmatics can be prepared for logic simulation, fault analysis, layout, or critical path analysis in the same manner.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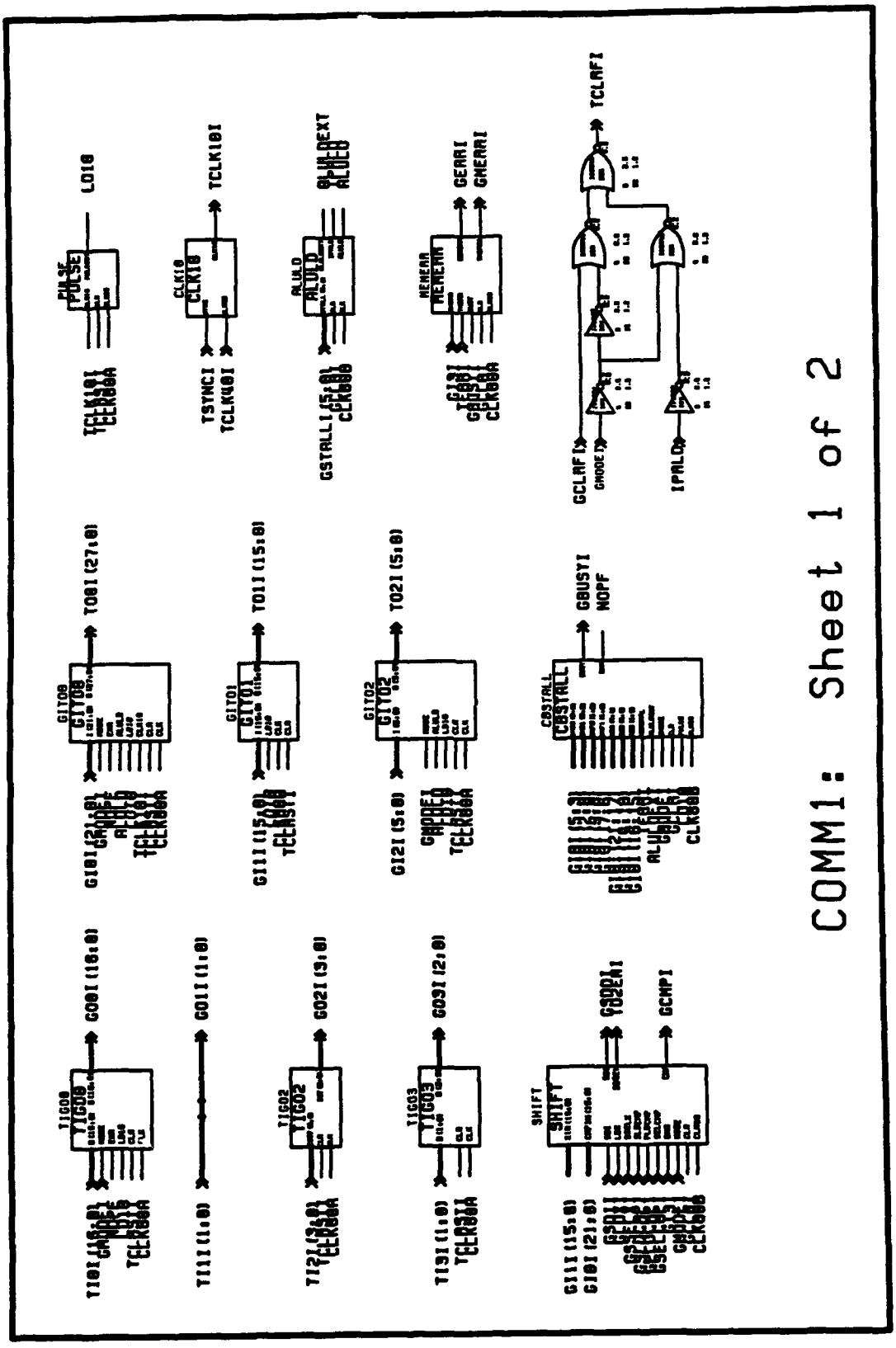
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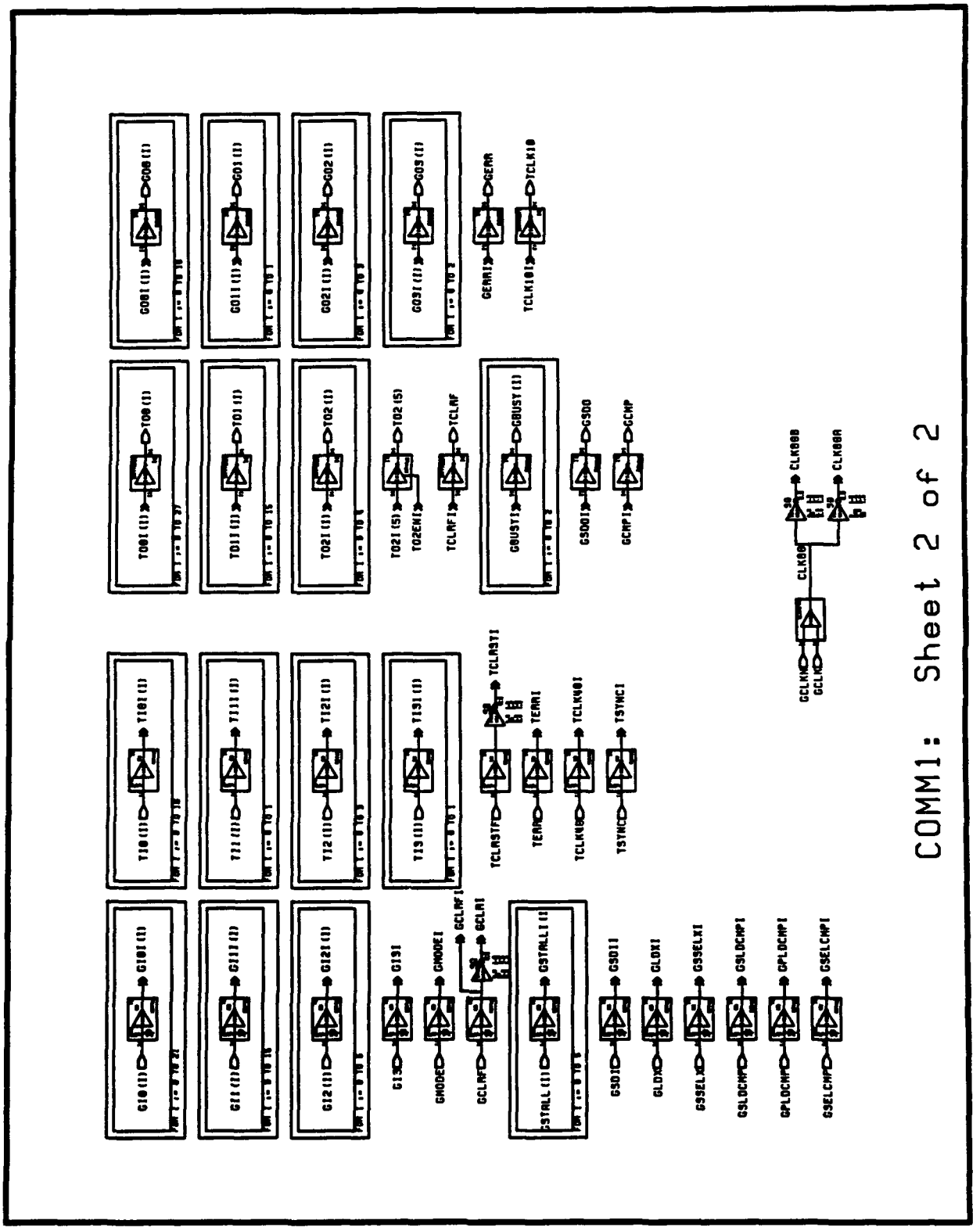
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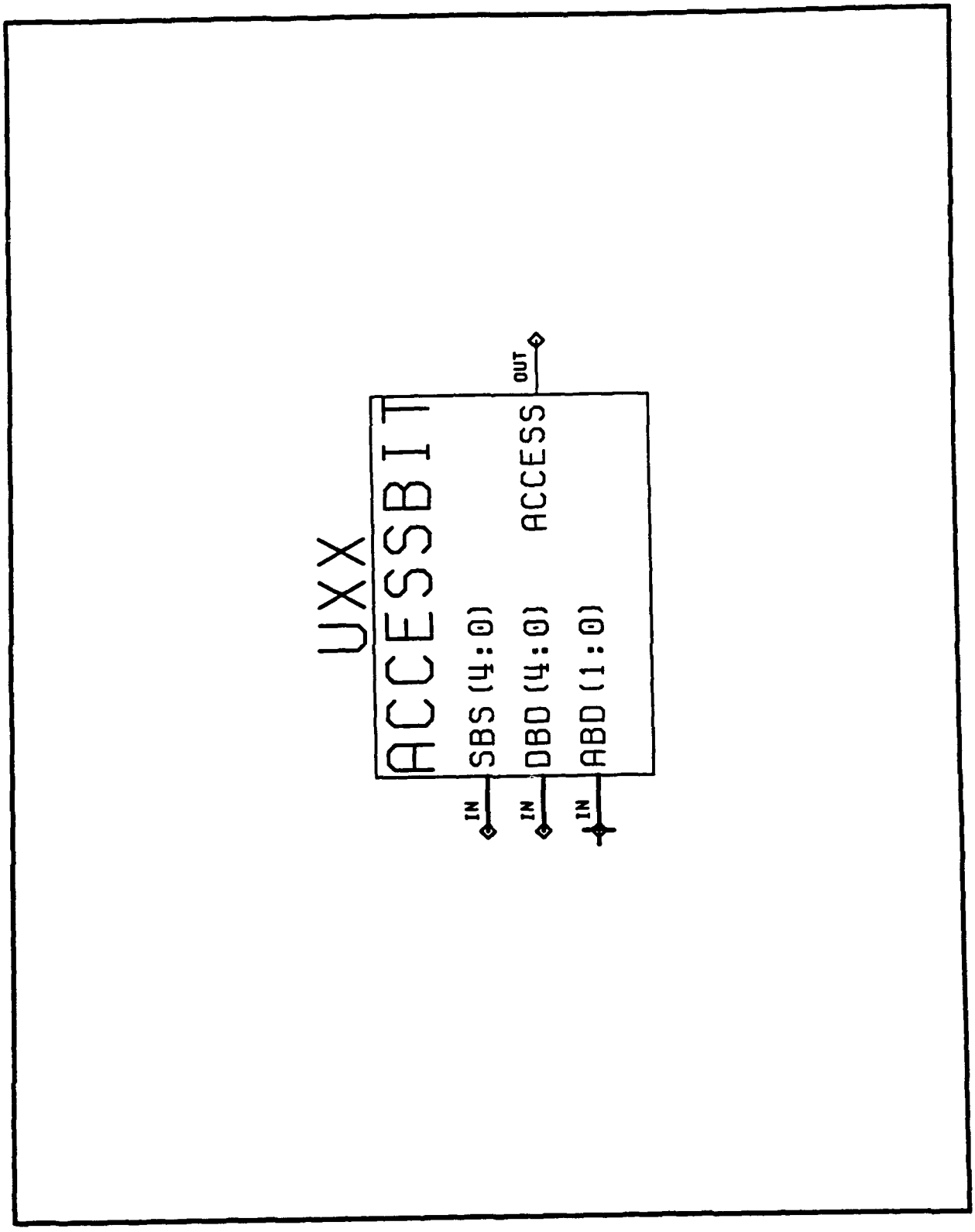
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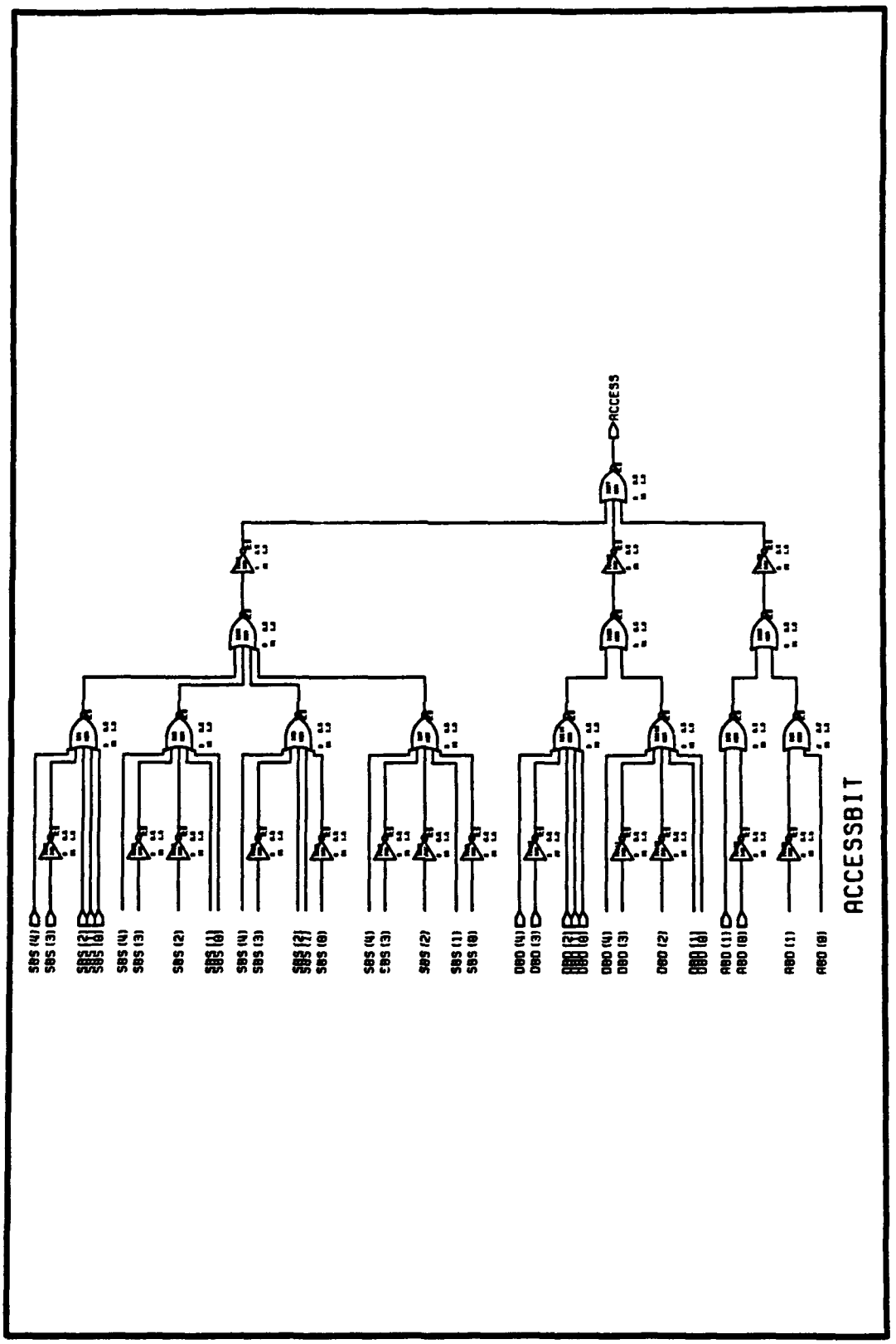
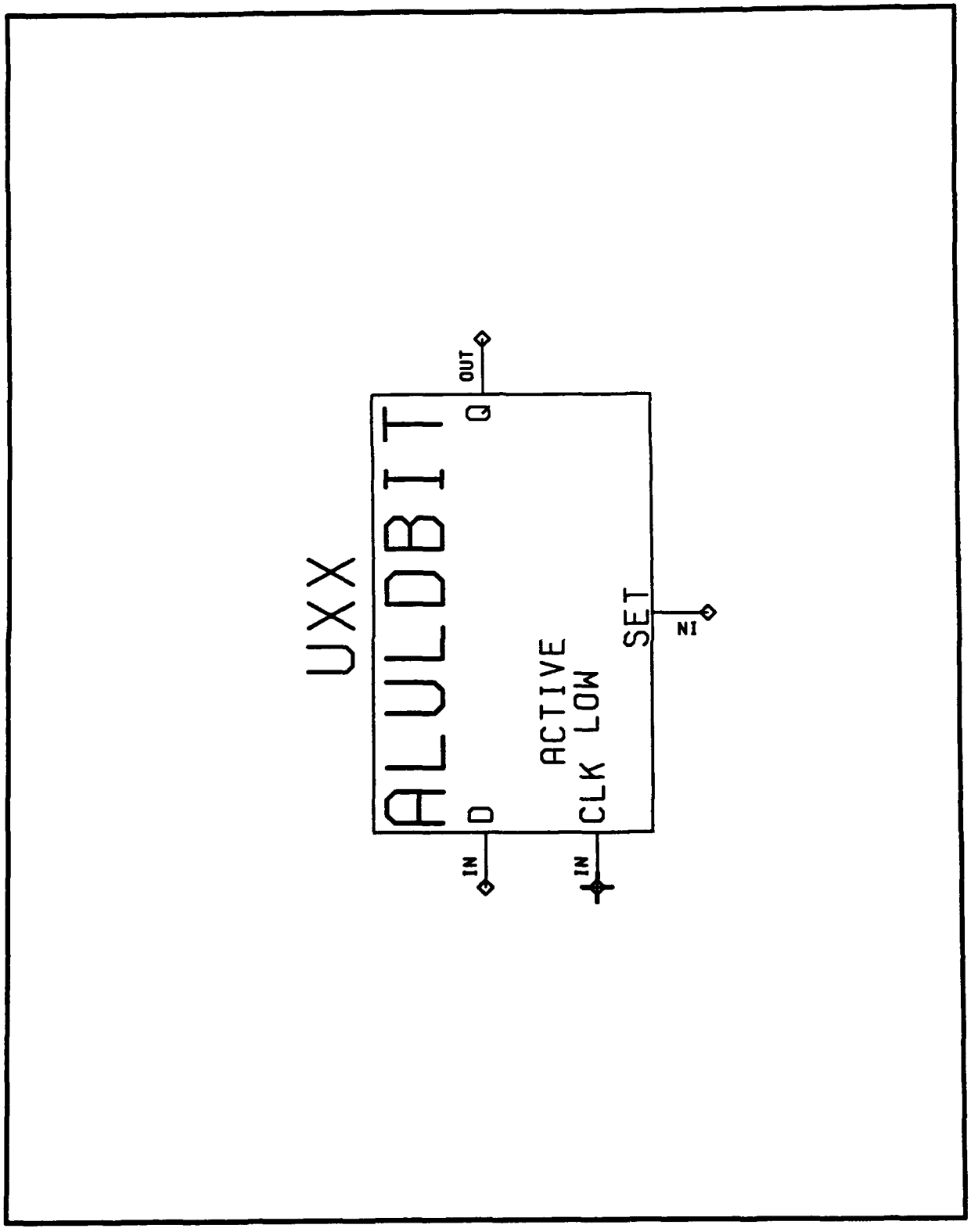
SBS(4:0)
DBD(4:0)
ABD(1:0)
ACCESS
IN
IN
IN
OUT


ACCESS
ACCESSBIT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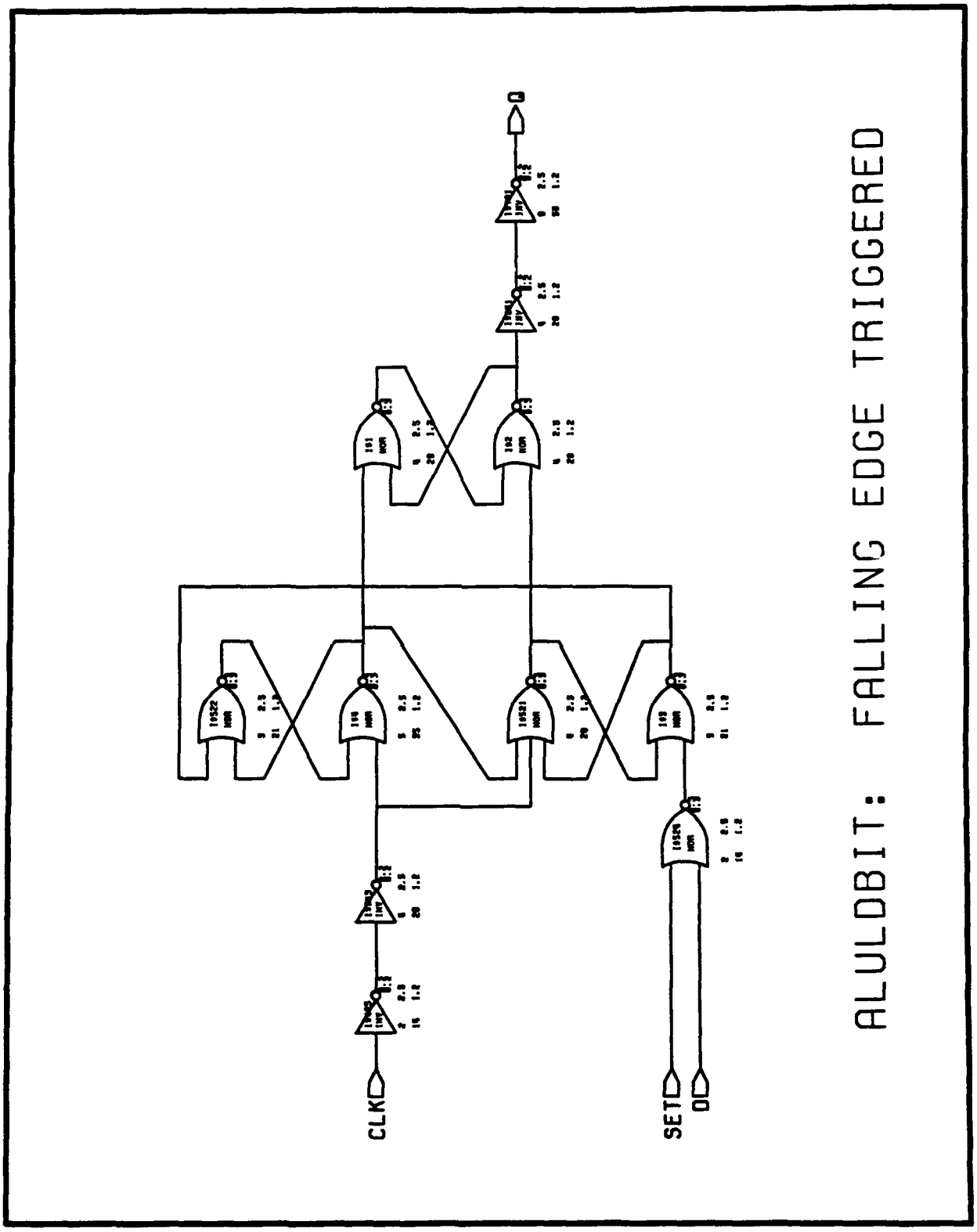
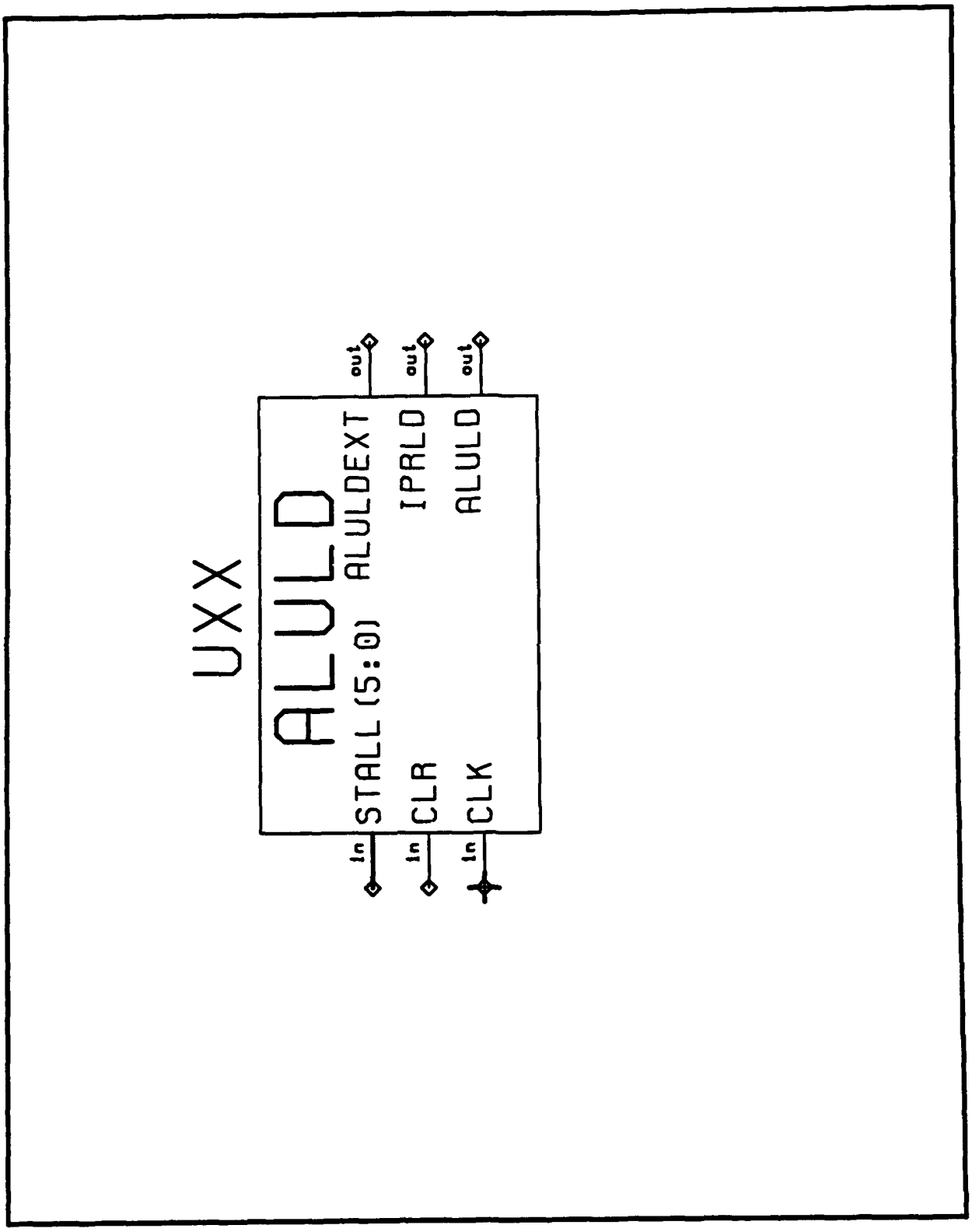
ALULDBIT
OUT
Q
D
IN
ACTIVE
CLK LOW
IN
SET
NI


ALULDBIT: FALLING EDGE TRIGGERED
Q
CLK
SET
D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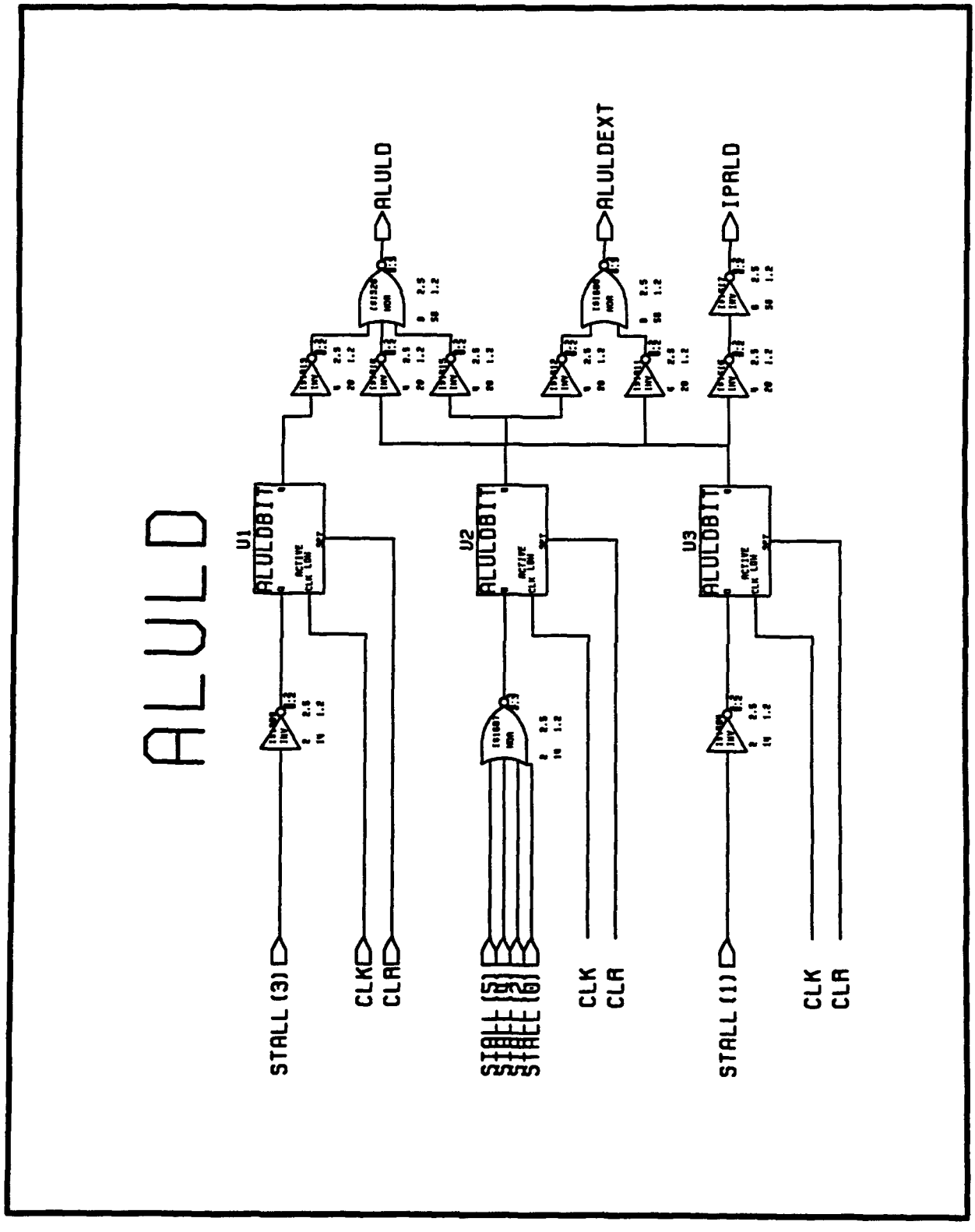
ALULD
STALL(5:0)
ALULDEXT
IPRLD
ALULD
CLR
CLK
out
out
out
in
in
in


ALULD
ALULD
ALULDEXT
IPALD
U1
U2
U3
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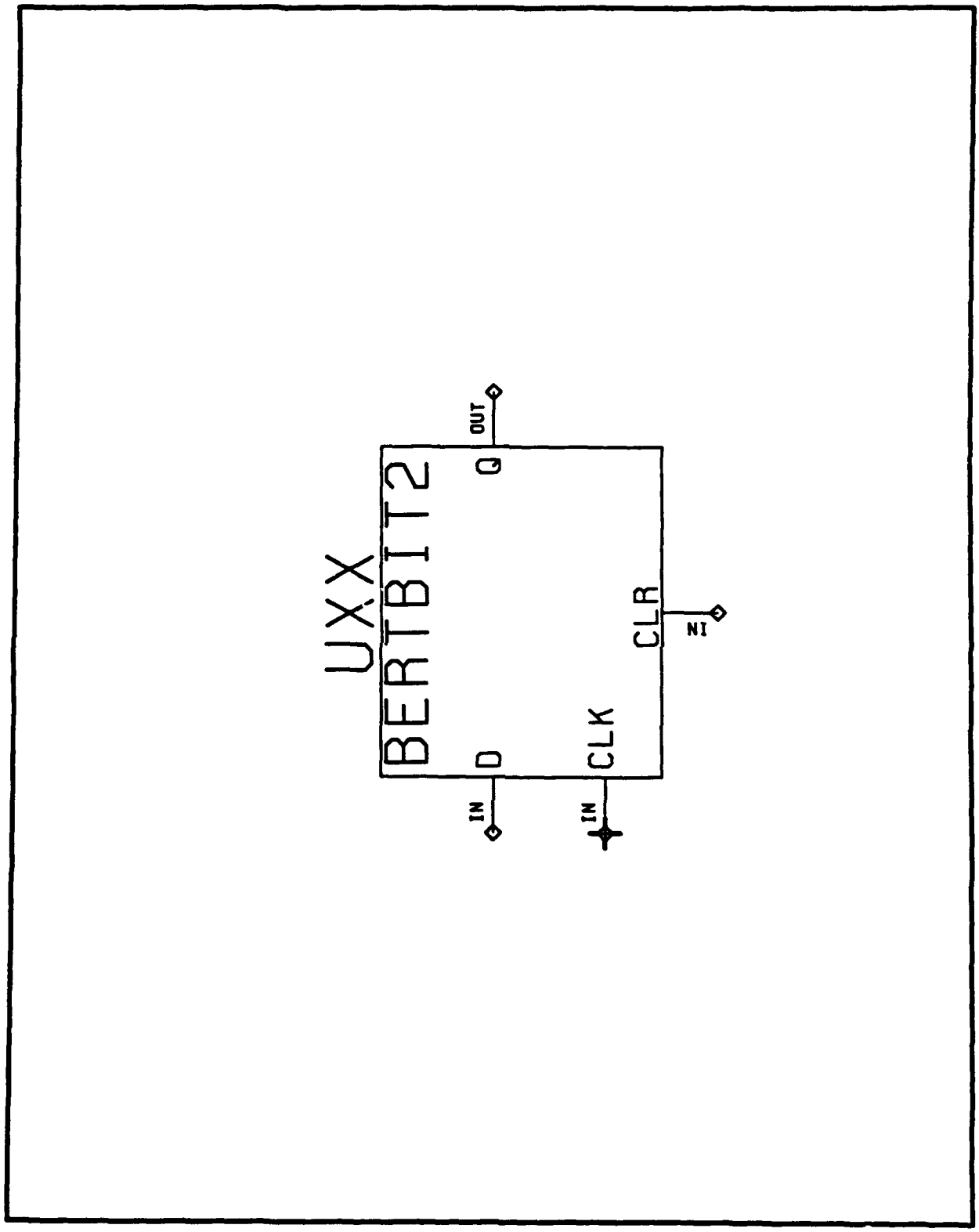
ALULDBIT
ALULDBIT
STALL (3)
CLK
CLR
CLK
CLR
CLK
CLR
STALL (1)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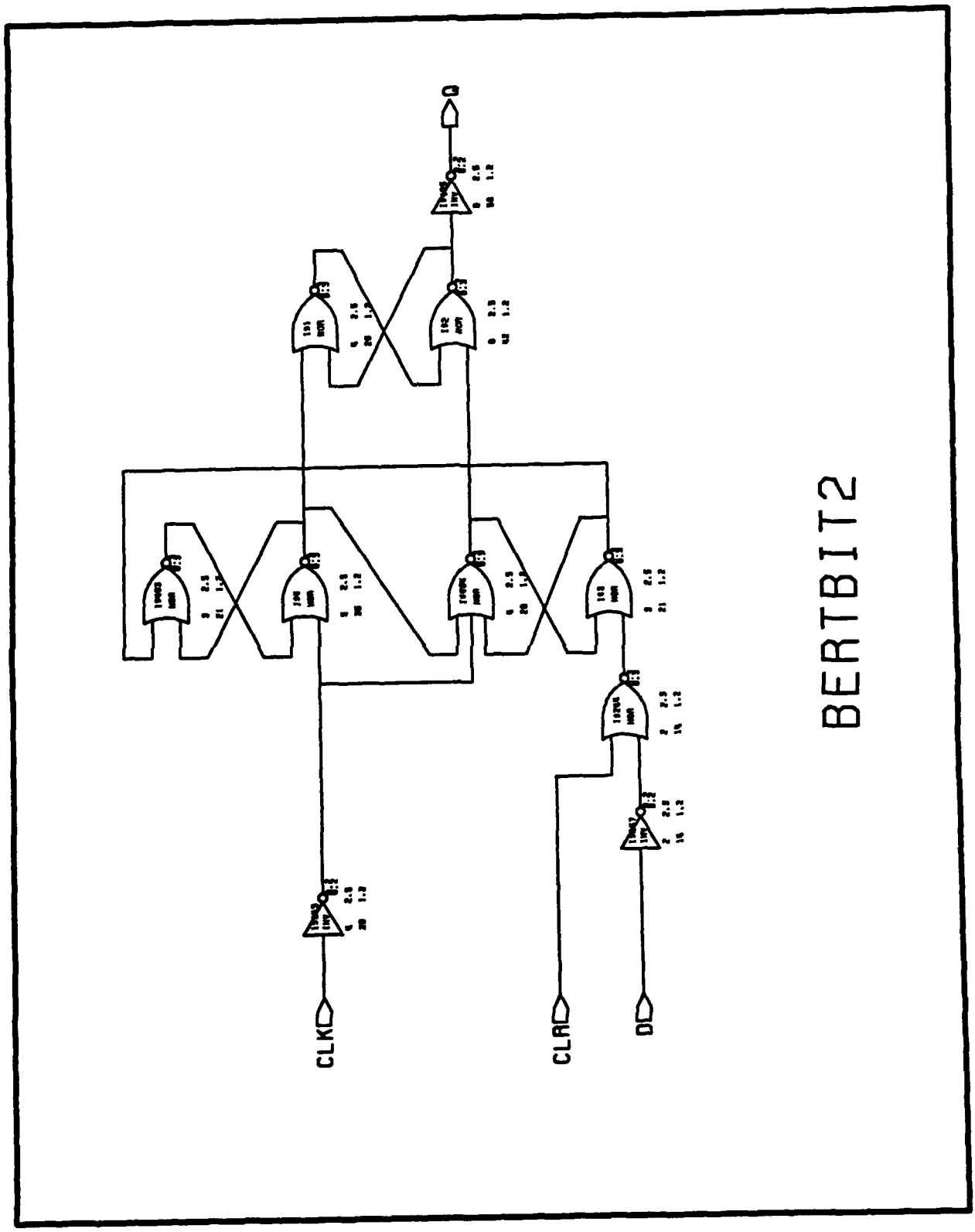
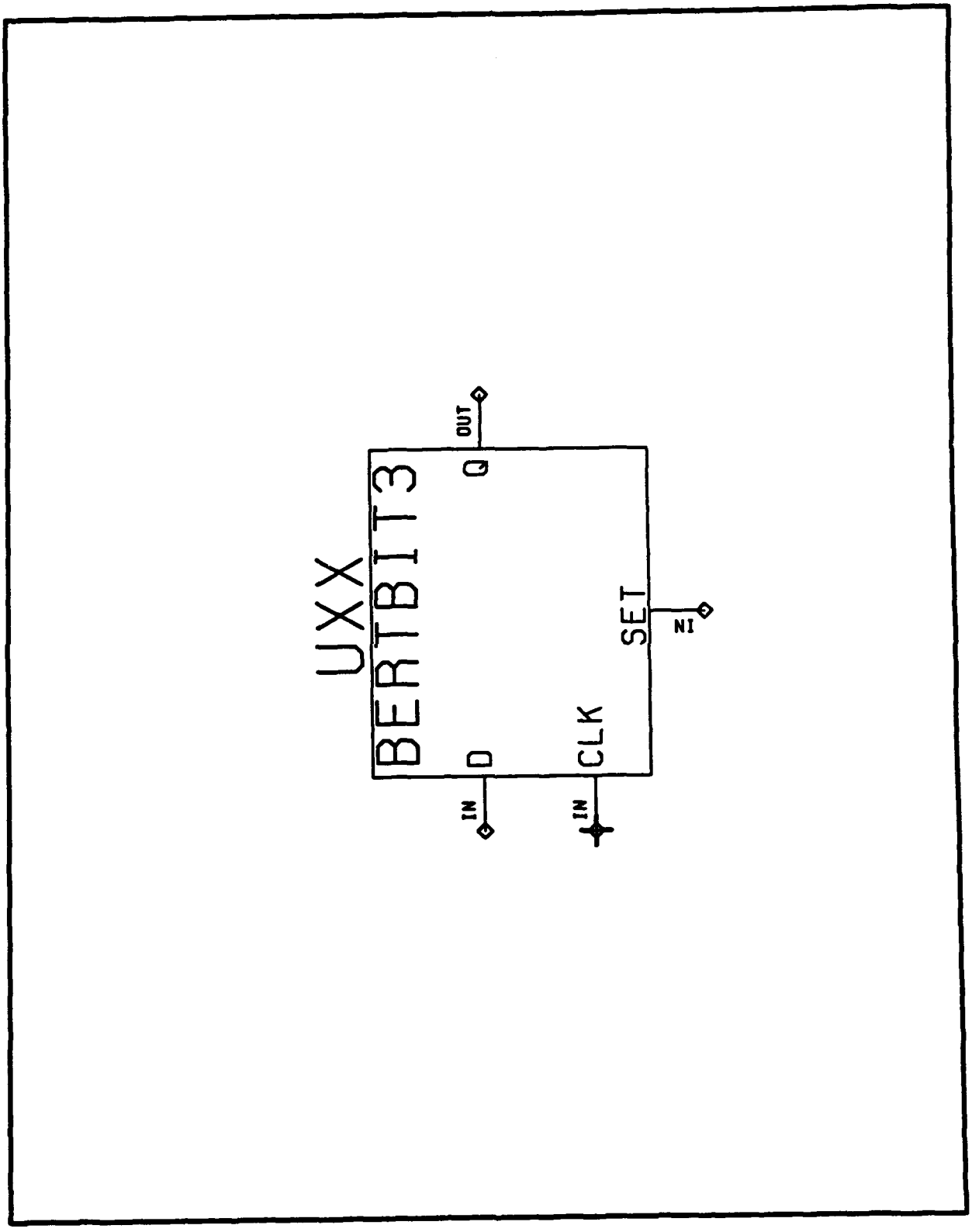
BERBIT2
OUT
Q
CLR
NI
D
CLK
IN
IN


Q
CLK
CLR
D
BERTBIT2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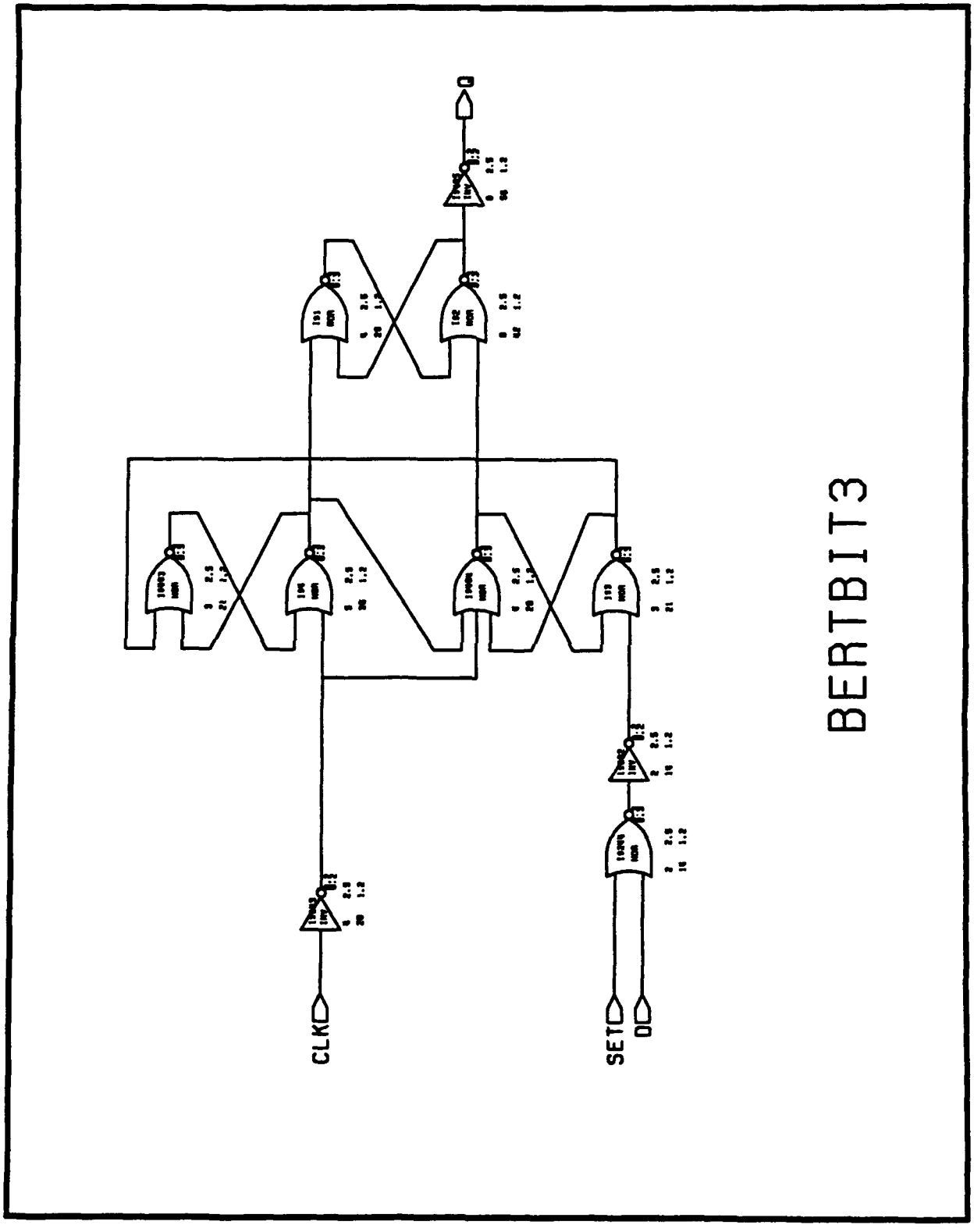
OUT
Q
SET
NI
D
CLK
IN
IN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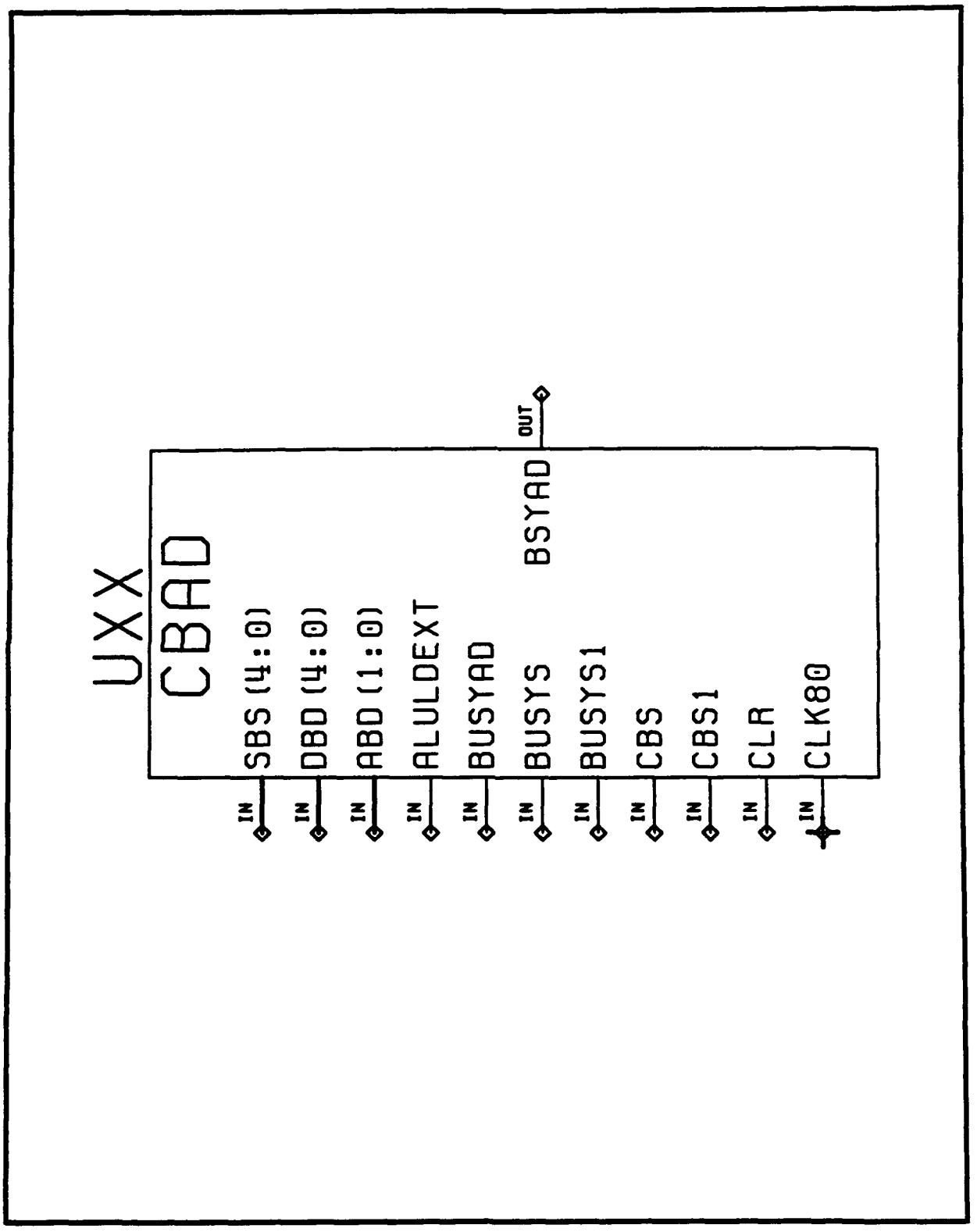
CLK
SET
D
BERTBIT3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CBAD
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DBD(4:0)
ABD(1:0)
ALULDEXT
BUSYAD
BUSYS
BUSYS1
CBS
CBS1
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CLK80
BSYAD
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IN
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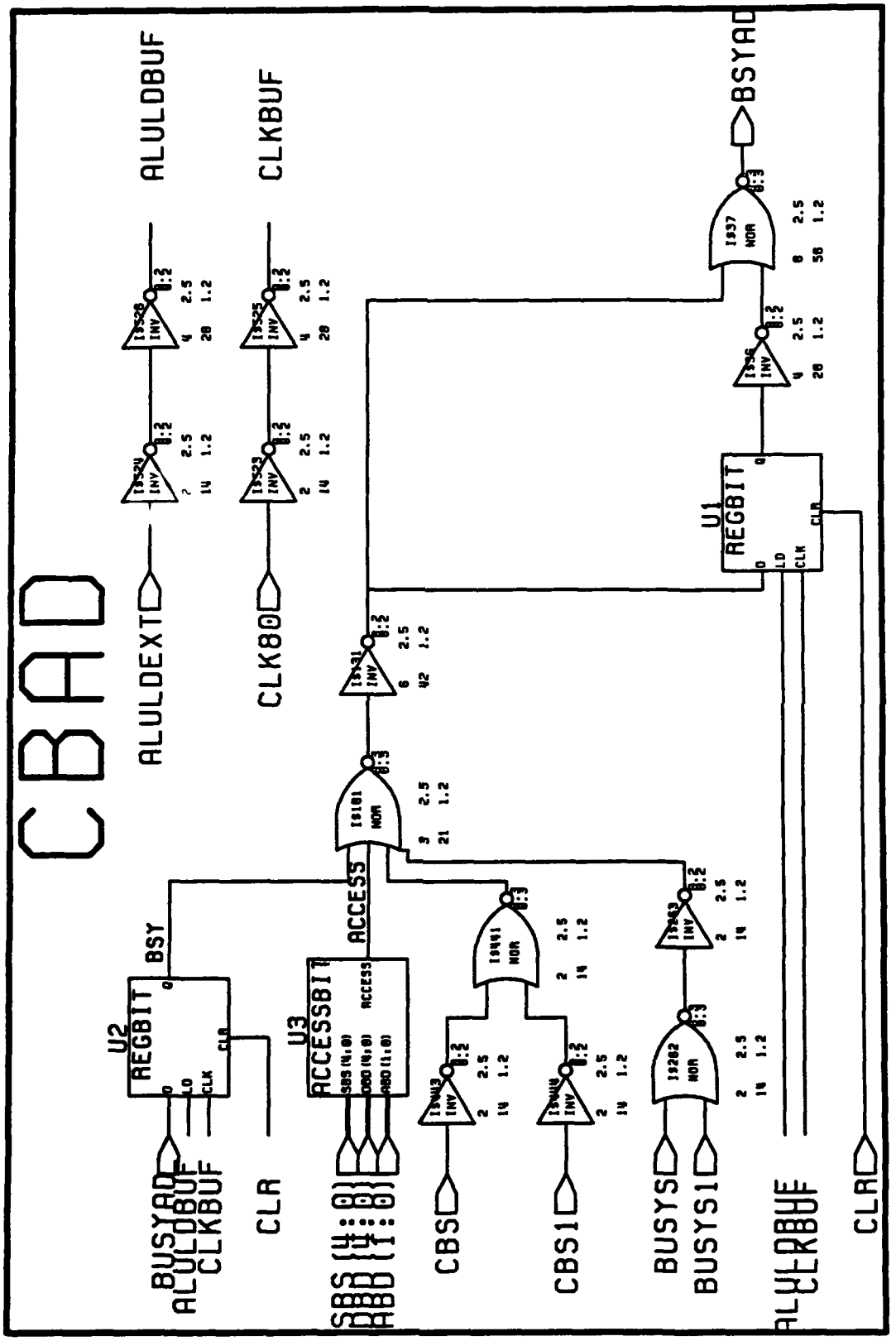
IN
IN
IN
IN
IN
IN
IN
IN
OUT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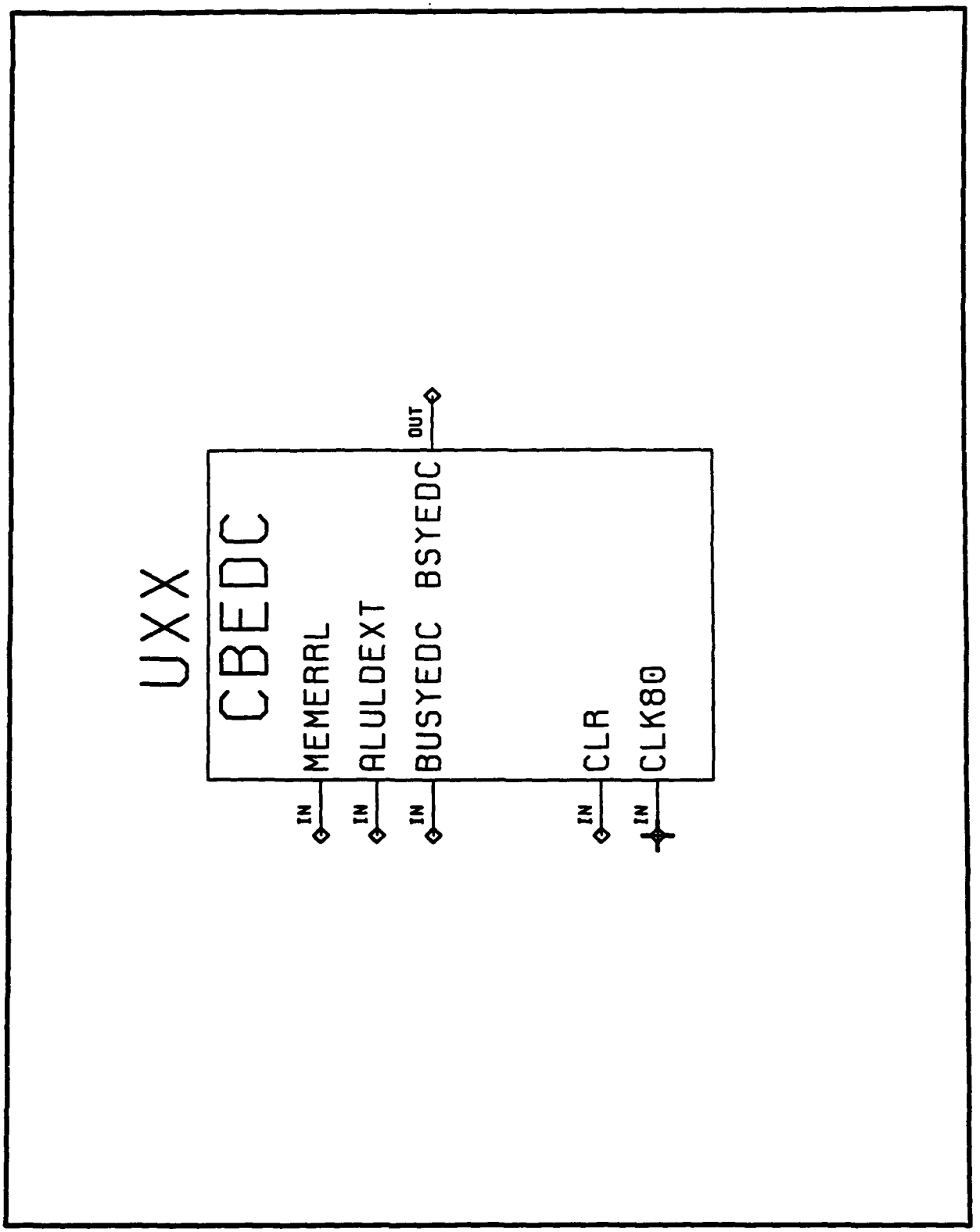
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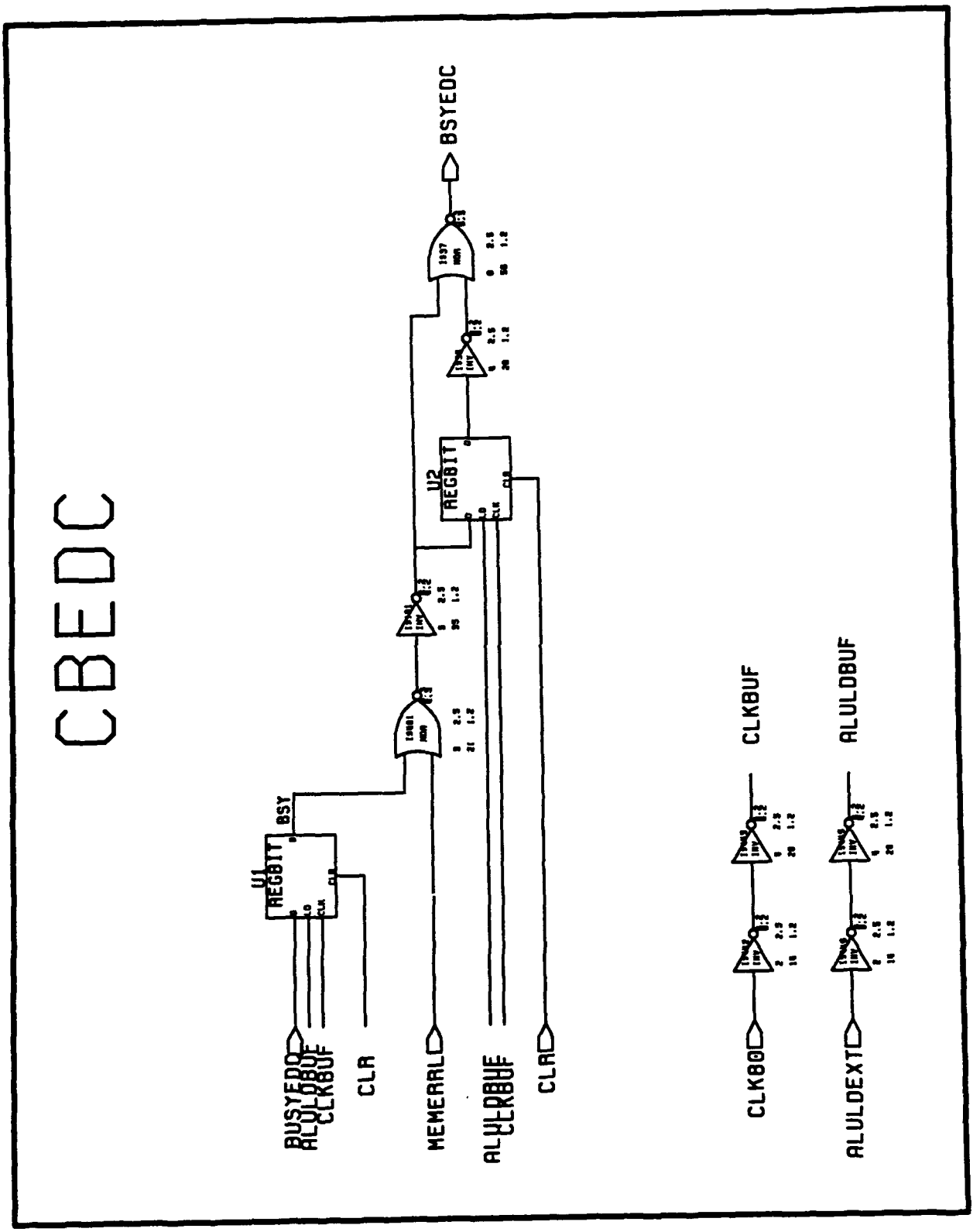
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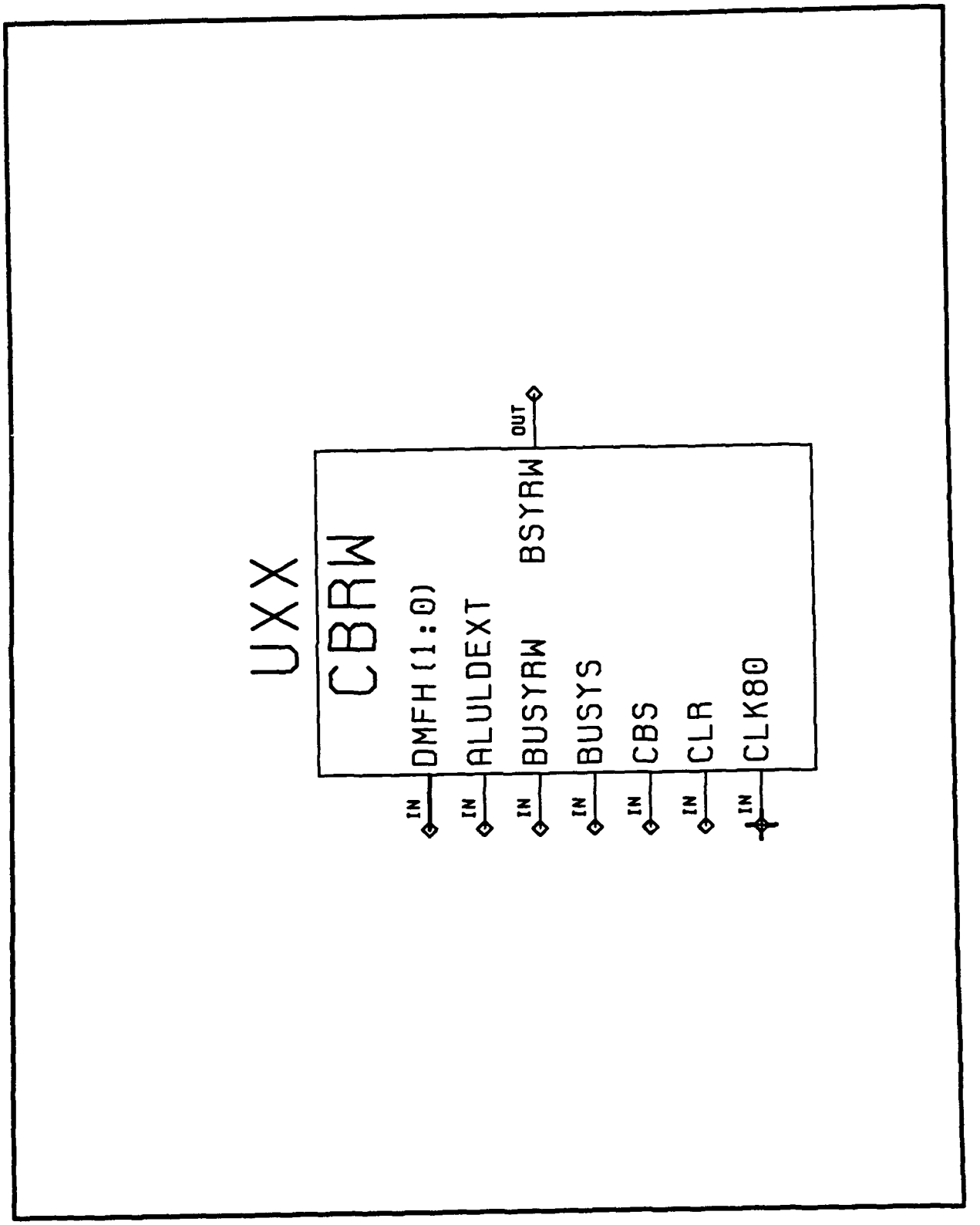
CLKBO
ALULDEXT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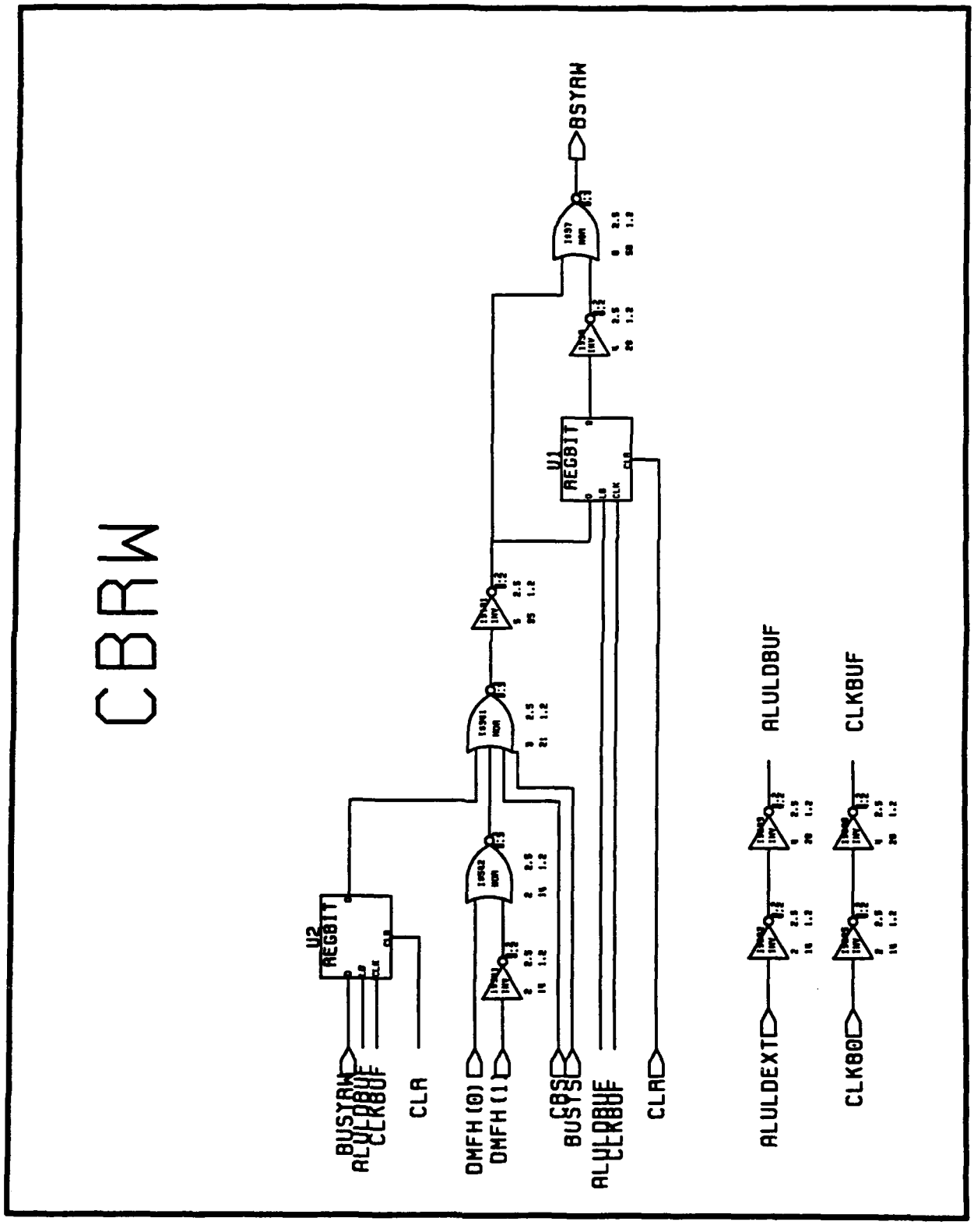
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U2
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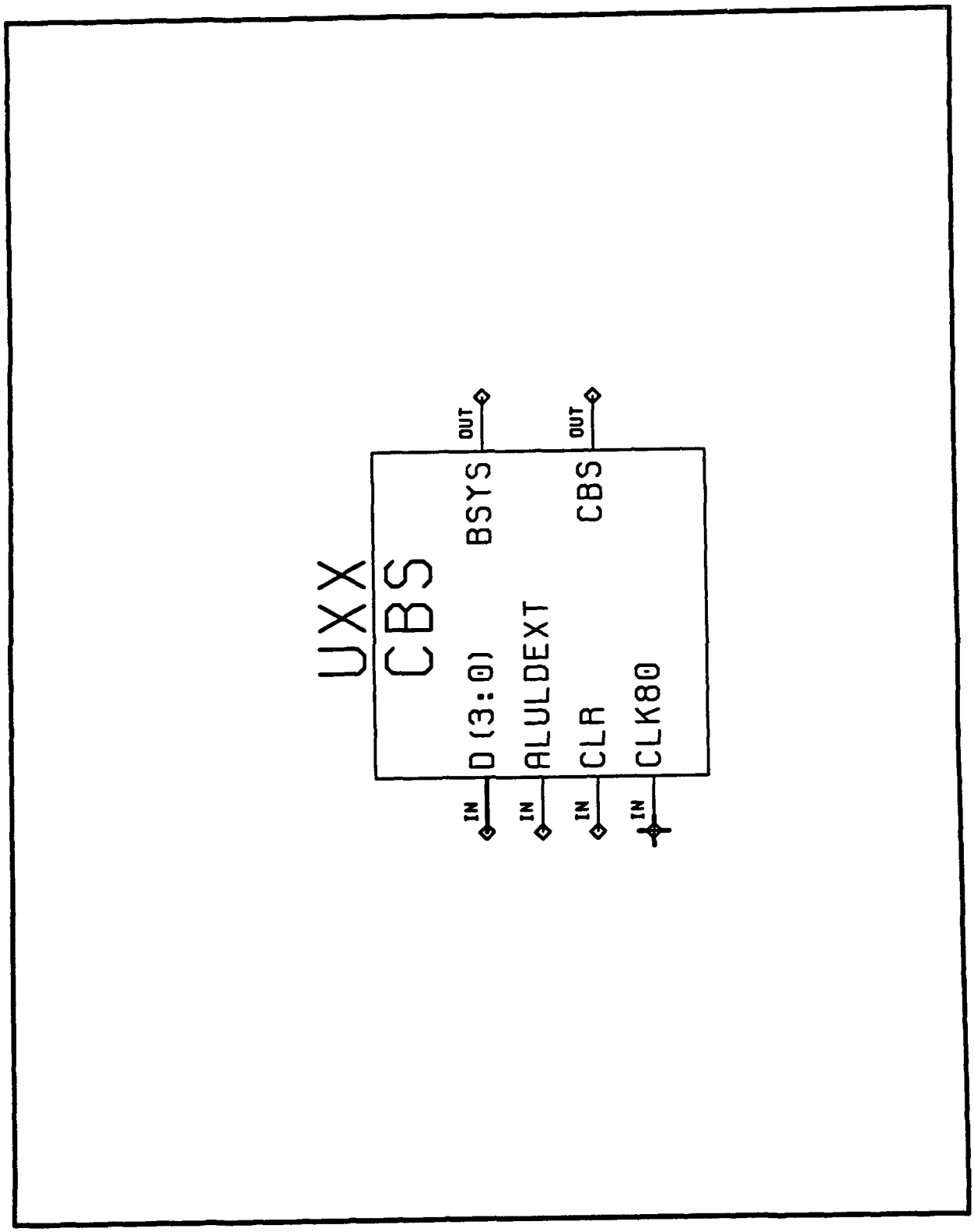
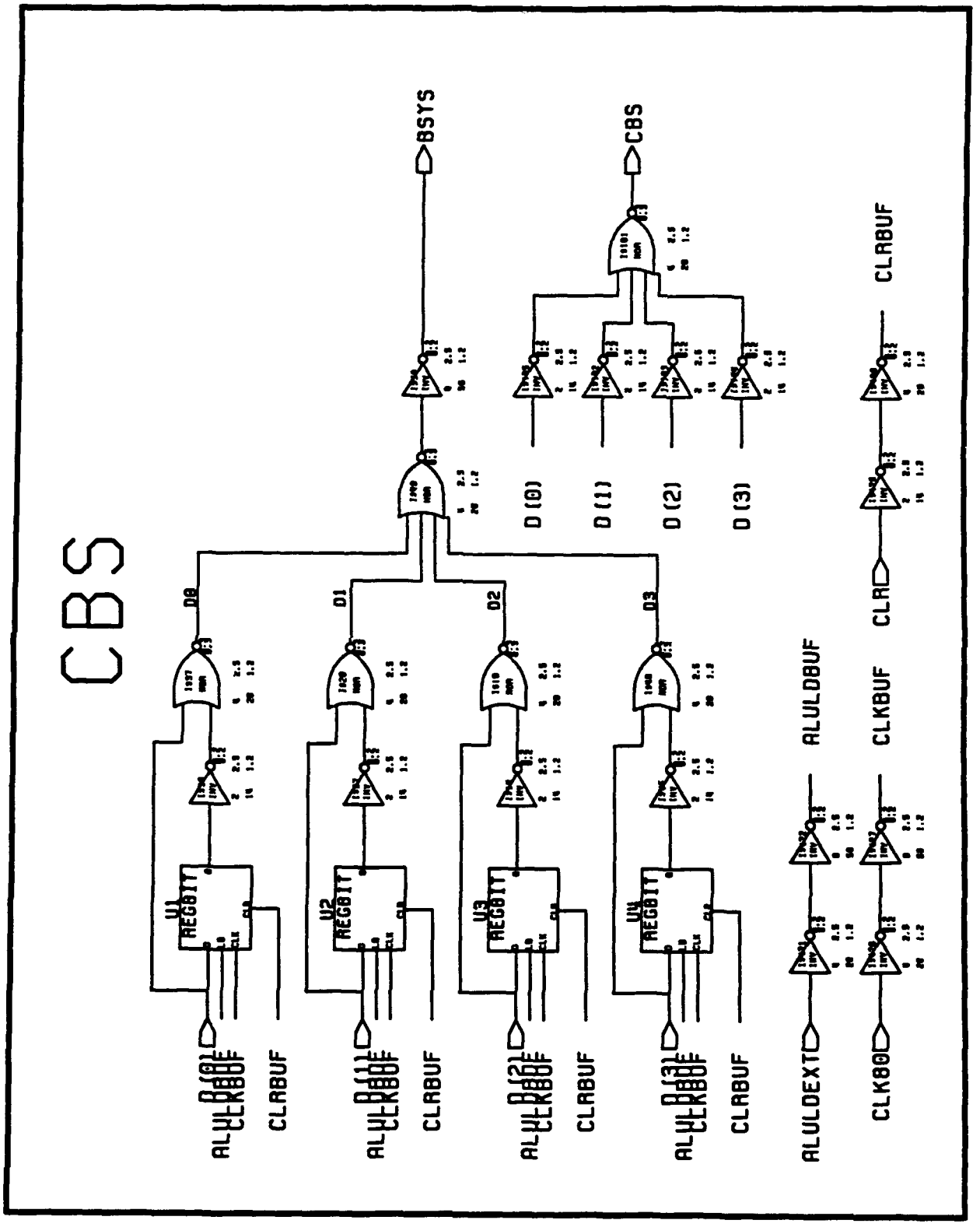
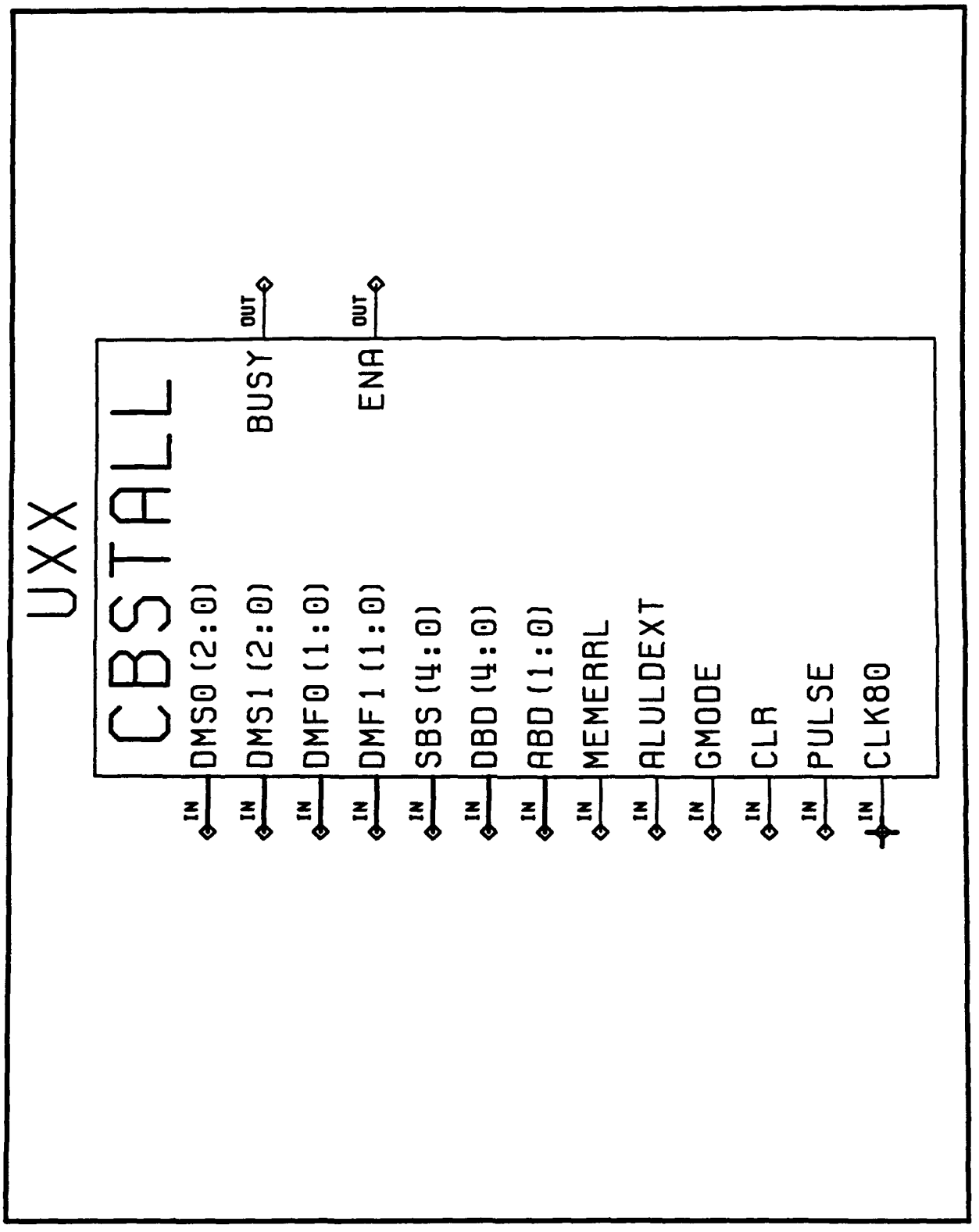
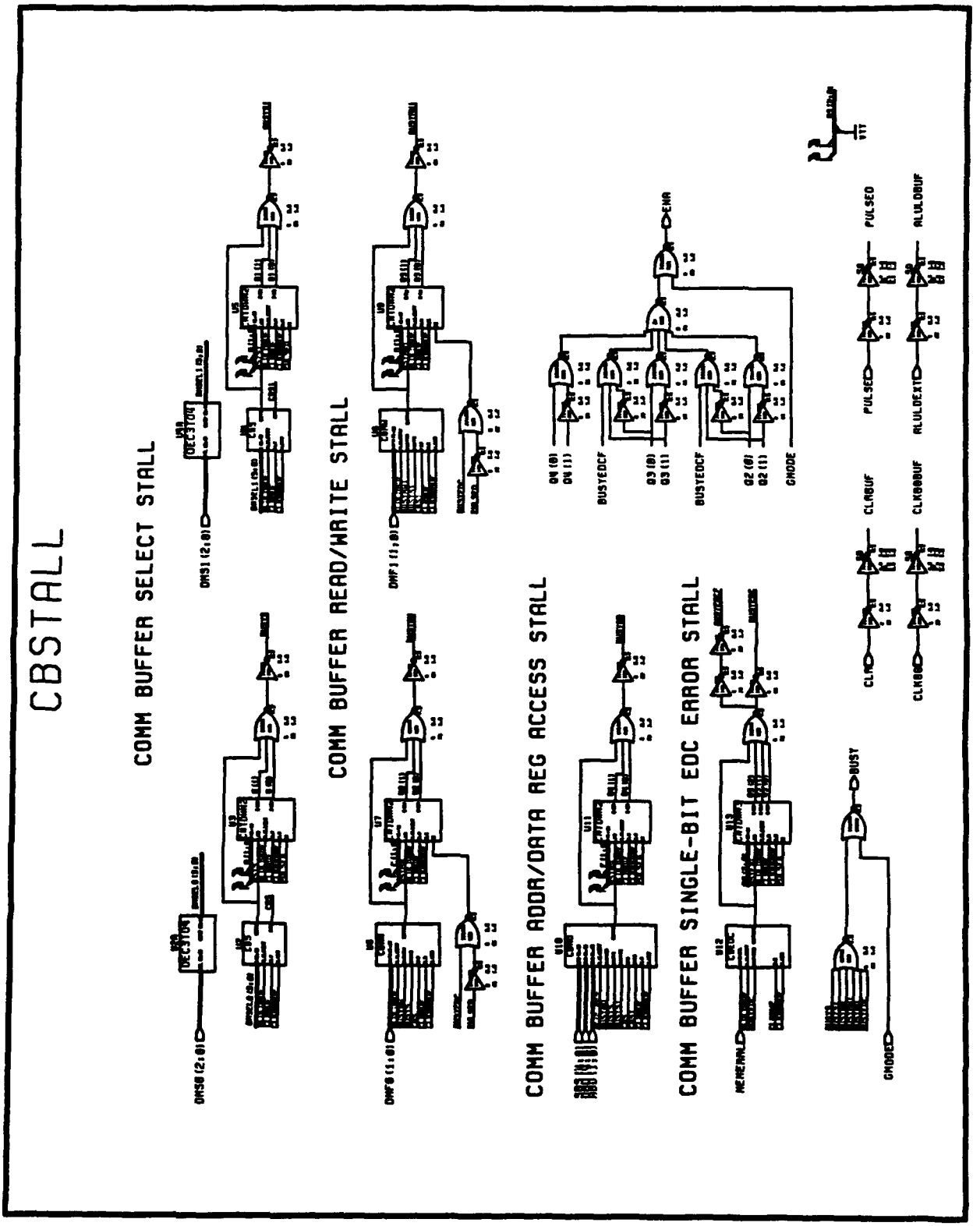
CBS
BUSYS
ALULDBUF
CLR
ALULDEXT
CLK80


UXX
CBS
OUT
BSYS
OUT
CBS
D(3:0)
ALULDEXT
CLR
CLK80
IN
IN
IN
IN


CBS
BSYS
CBS
D (0)
D (1)
D (2)
D (3)
CLRBUF
CLR
ALULDBUF
CLKBUF
D0
D1
D2
D3
U1
U2
U3
U4
REG8IT
CLRBUF
ALULDEXT
CLK80

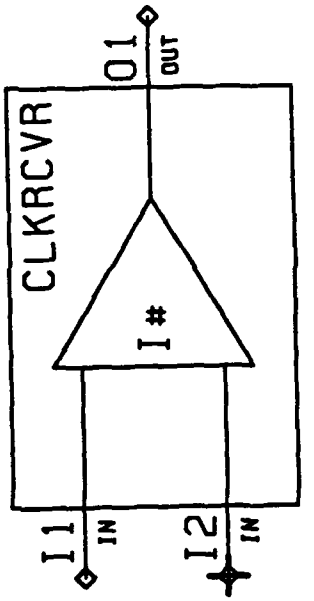

UXX
CBSTALL
BUSY
OUT
ENA
OUT
DMS0(2:0)
DMS1(2:0)
DMF0(1:0)
DMF1(1:0)
SBS(4:0)
DBD(4:0)
ABD(1:0)
MEMERRL
ALULDEXT
GMODE
CLR
PULSE
CLK80
IN


CBSTALL
COMM BUFFER SELECT STALL
COMM BUFFER READ/WRITE STALL
COMM BUFFER ADDR/DATA REG ACCESS STALL
COMM BUFFER SINGLE-BIT EDC ERROR STALL
BUSYEDCF
BUSYEDCF
ENA
PULSED
PULSED
ALULOBUF
ALULDEXT
CLKBUF
CLKBUF
CLKBUF
CLK
CLKBUF
BUSY
GNDDE

VITESSE GAAS CELL LIBRARY
Version 0.8

NAME: CLKRCVR

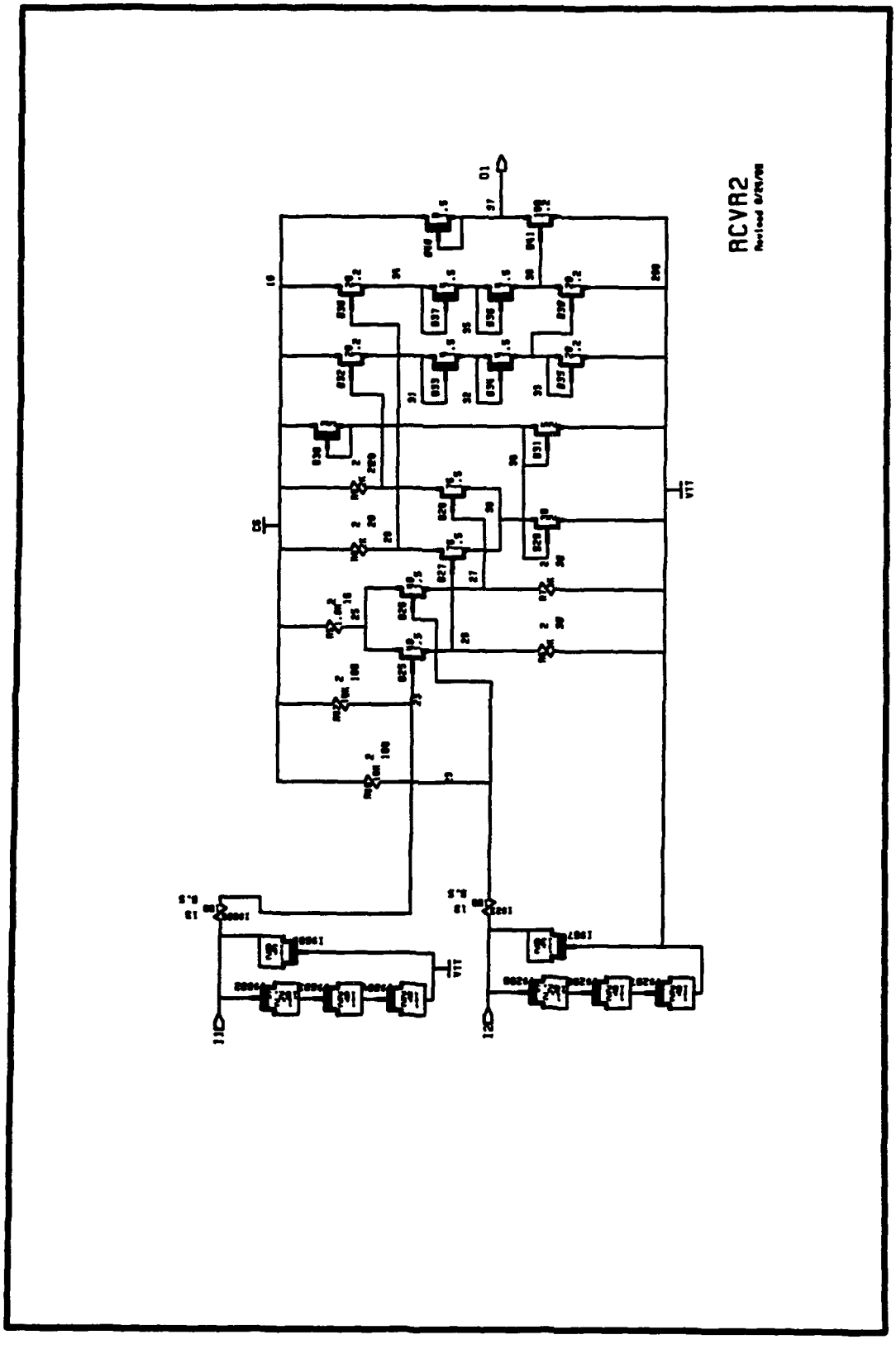
DESCRIPTION: DIFFERENTIAL INPUT CLOCK RECEIVER

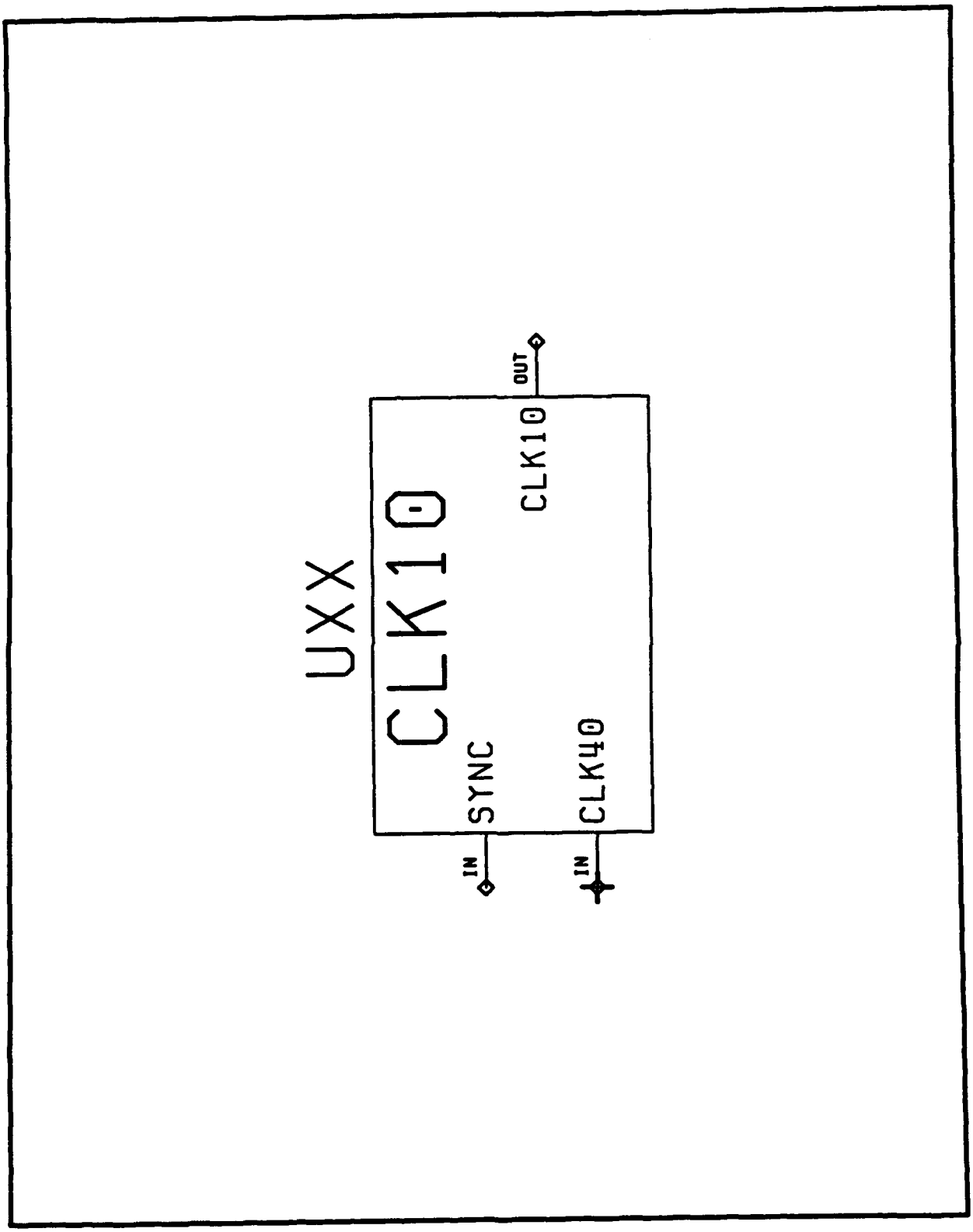


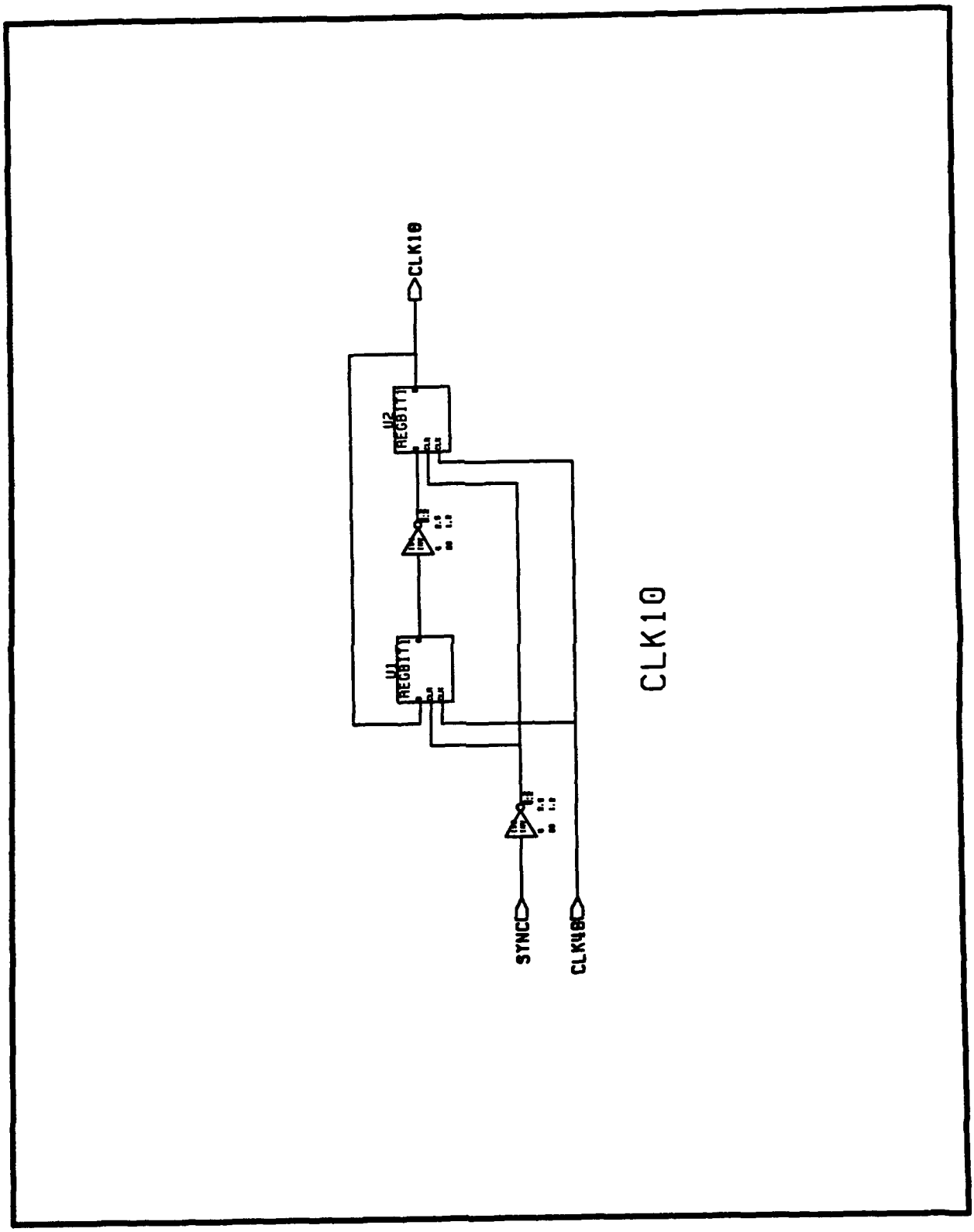
0.5 0.3 SSS

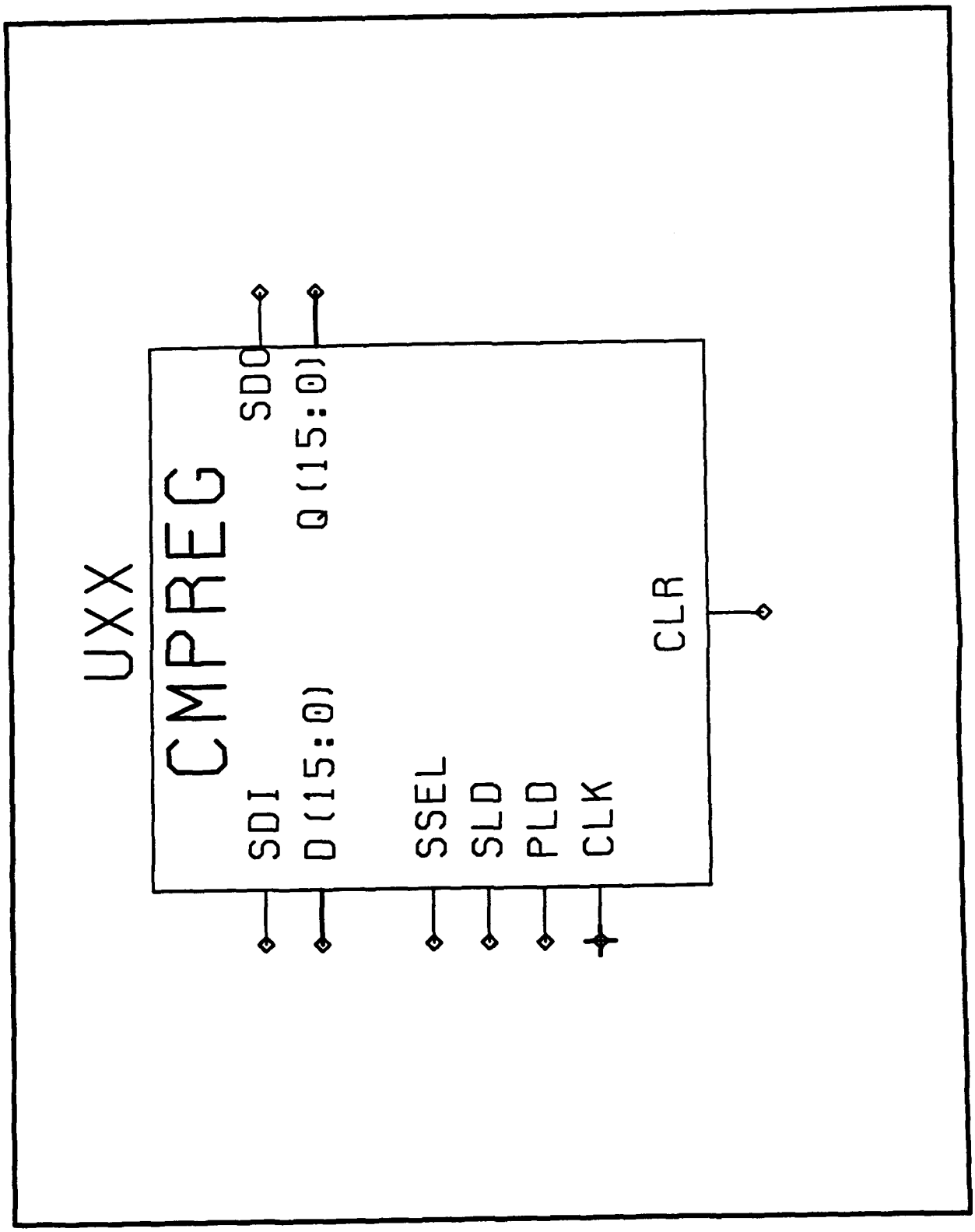
CLKRCVR

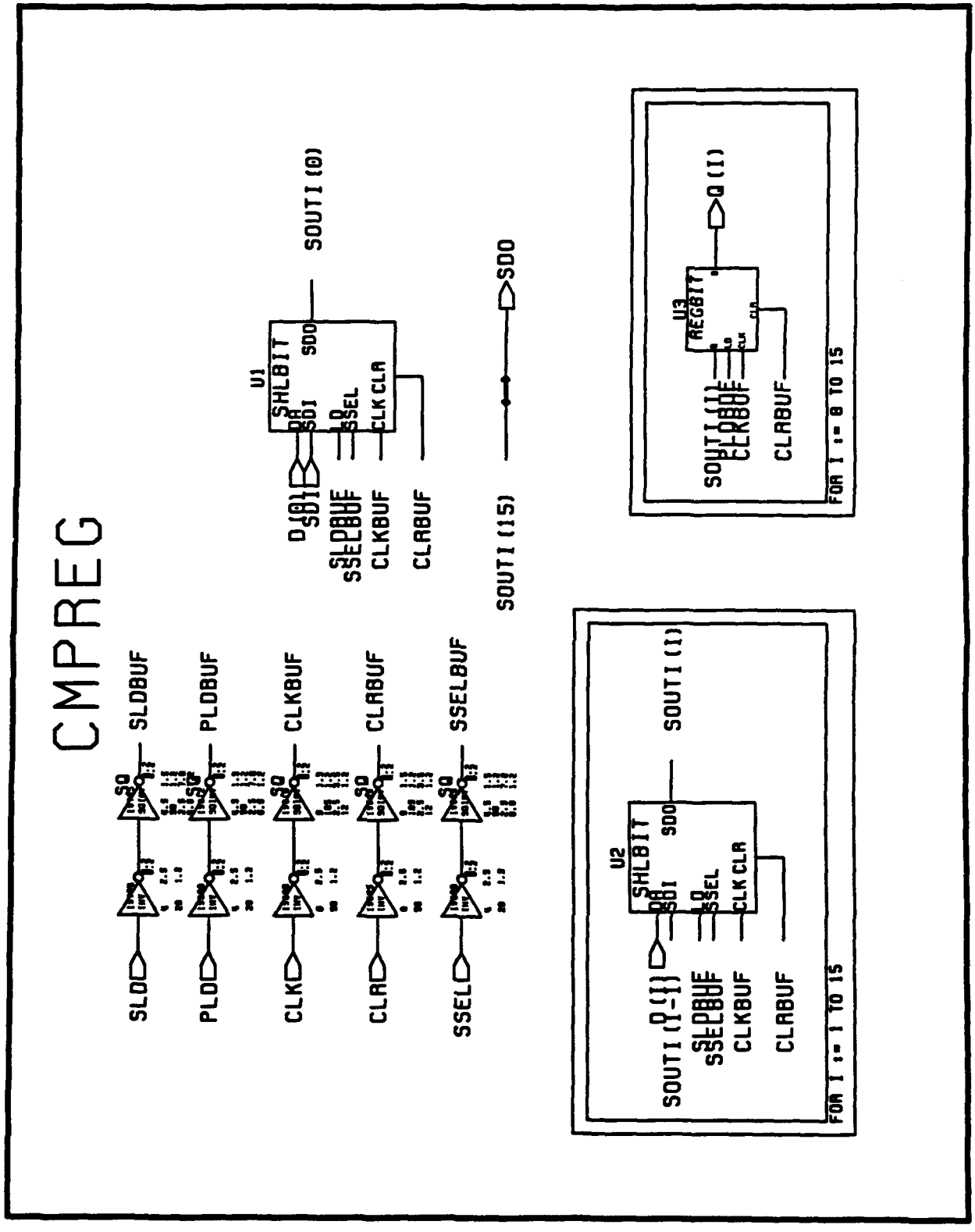
clkrcvr.bin

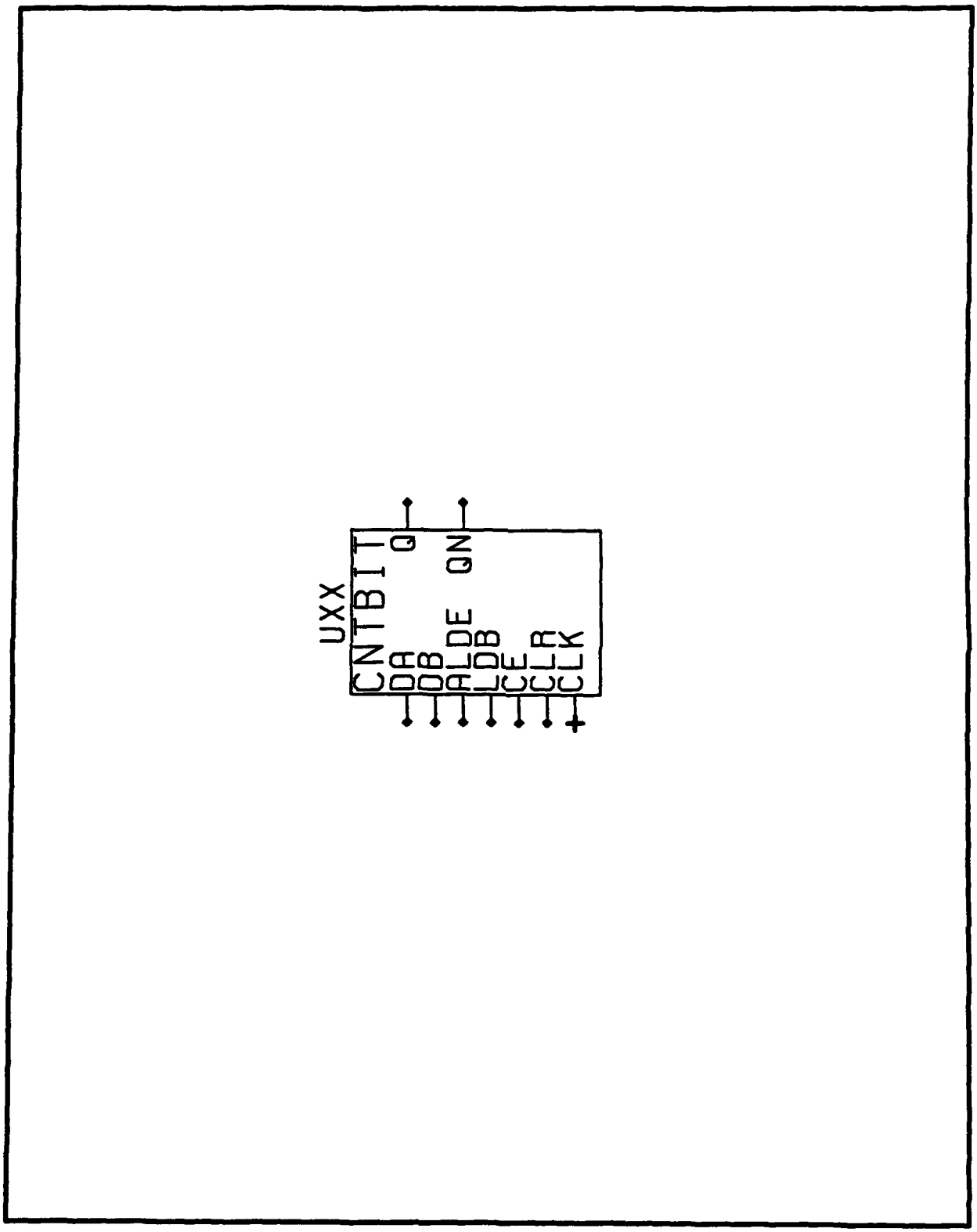

RCVR2

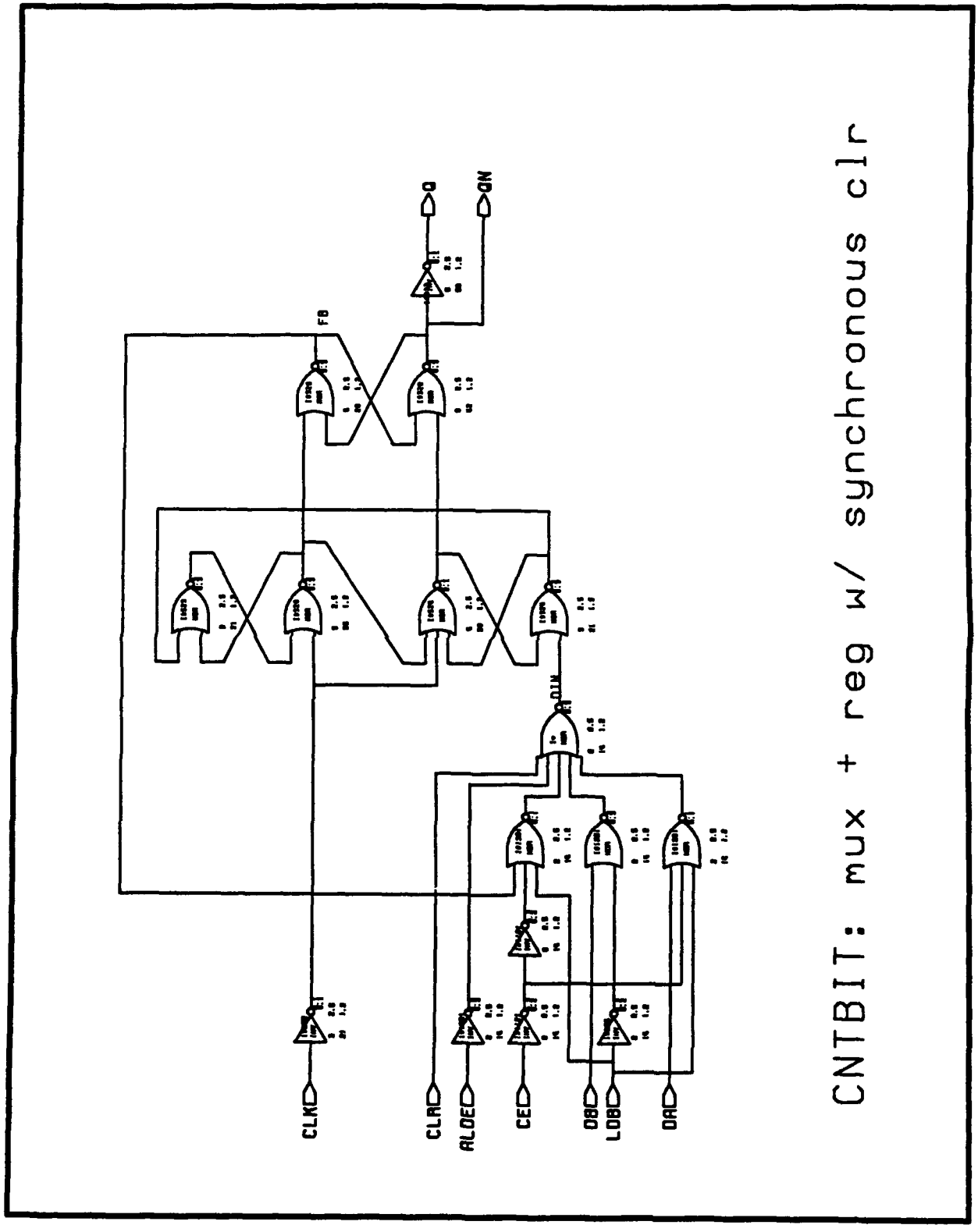

UXX
CLK10
OUT
CLK10
SYNC
CLK40
IN
IN

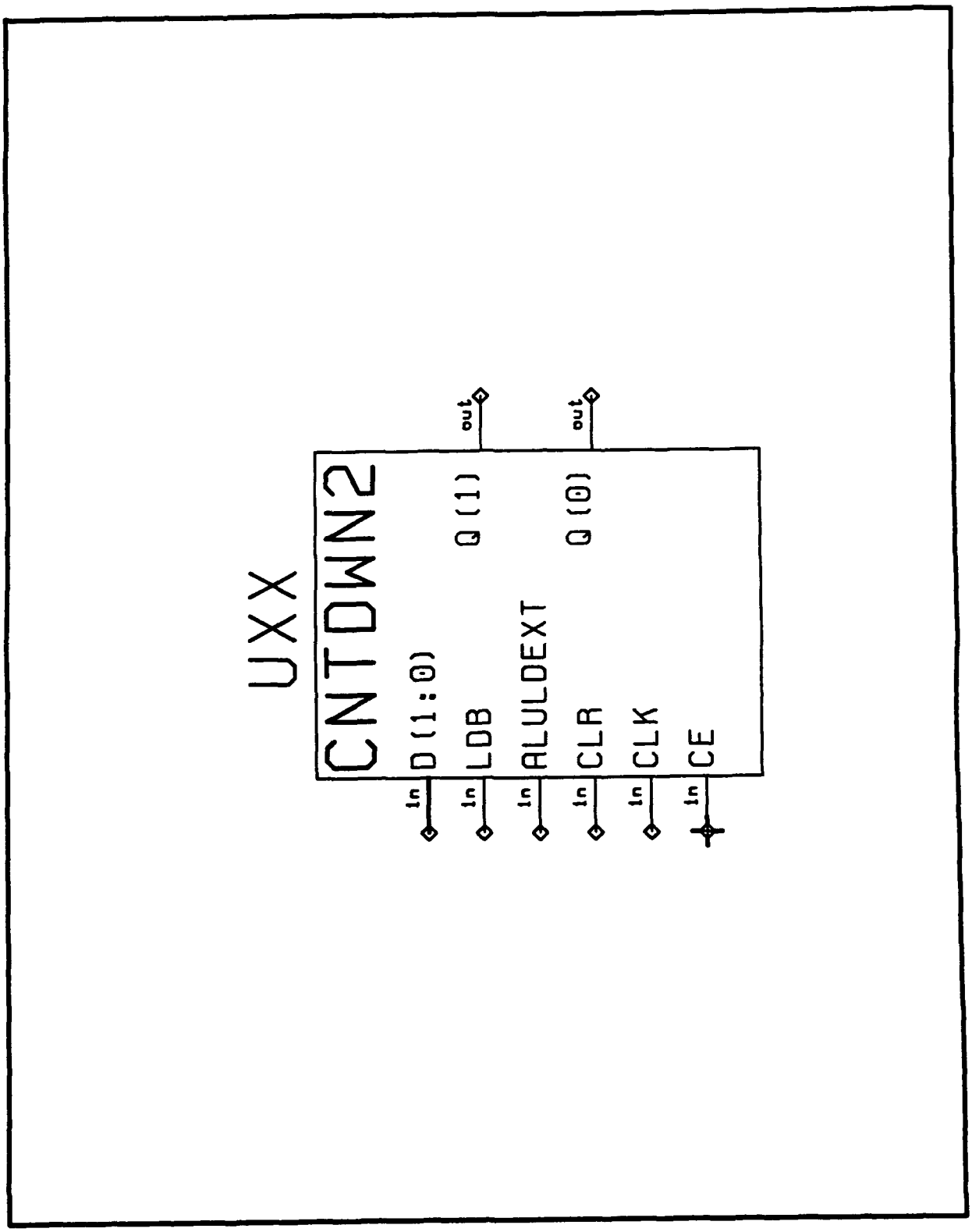

CLK10
U2
REGBIT1
U1
REGBIT1
SYNC
CLK10
CLK10

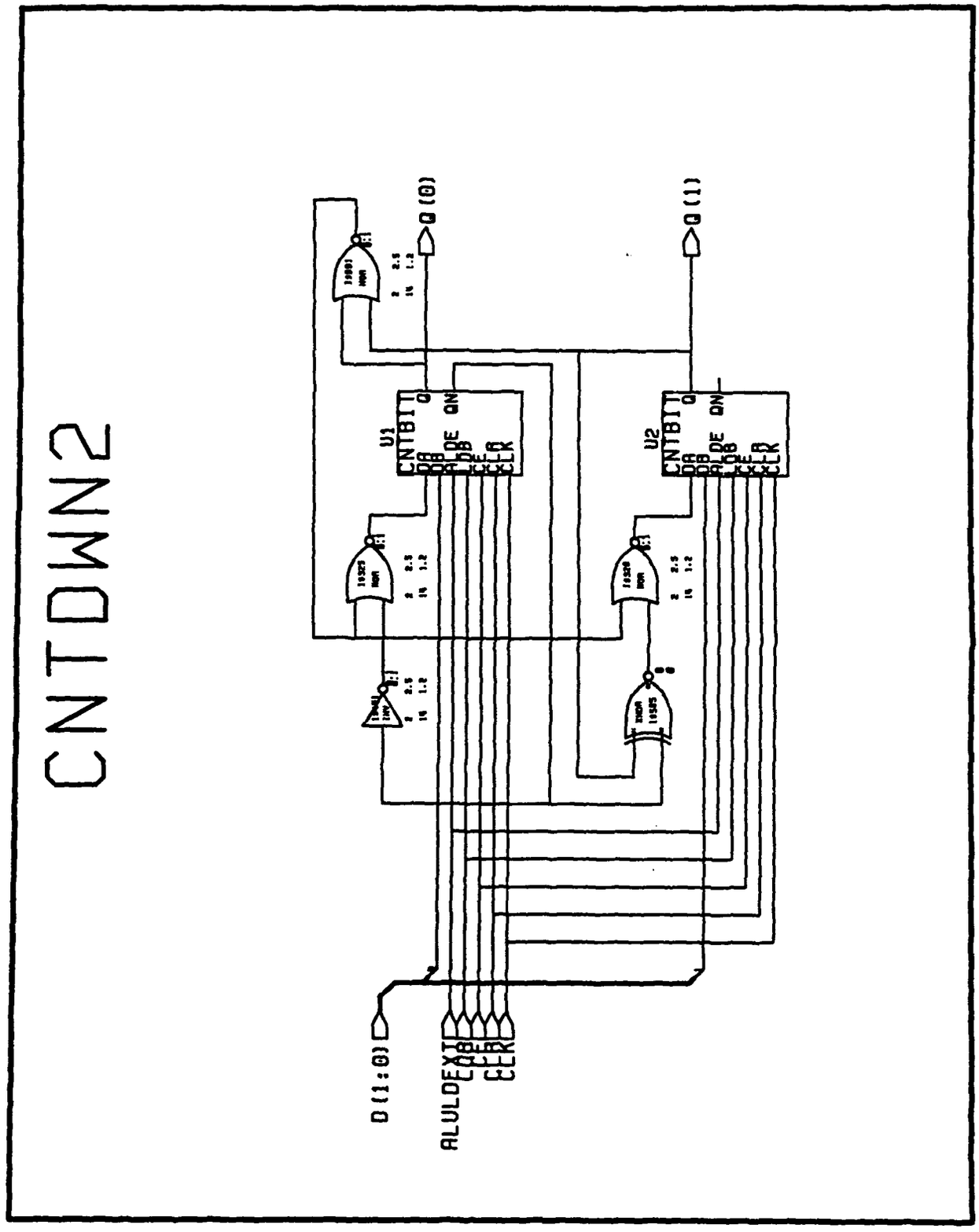

UXX
CMPREG
SDO
Q(15:0)
CLR
SDI
D(15:0)
SSEL
SLD
PLD
CLK

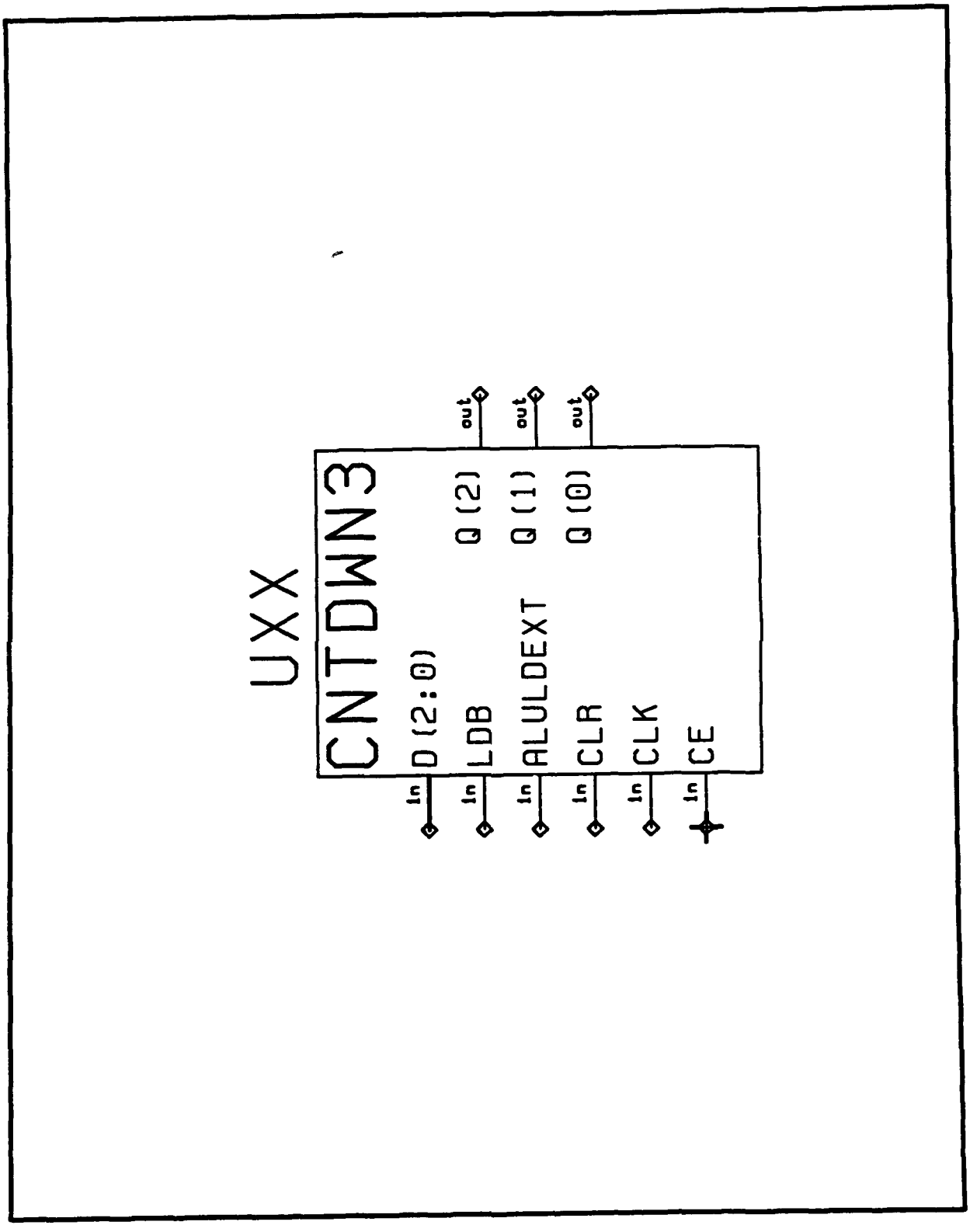

CMPREG
SLDBUF
PLDBUF
CLKBUF
CLRBUF
SSELBUF
SLD
PLD
CLK
CLR
SSEL
U1
SHLBIT
SDO
SDI
LD
SSEL
CLK CLR
SOUTI(0)
SDI(0)
SLDBUF
SSELBUF
CLKBUF
CLRBUF
SDO
SOUTI(15)
U2
SHLBIT
SOUTI(1)
SOUTI(I-1)
FOR I := 1 TO 15
U3
REGBIT
Q(I)
SOUTI(I)
CLRBUF
FOR I := 8 TO 15


UXX
CNTBIT
Q
QN
DA
DB
ALDE
ALDB
CE
CLR
CLK

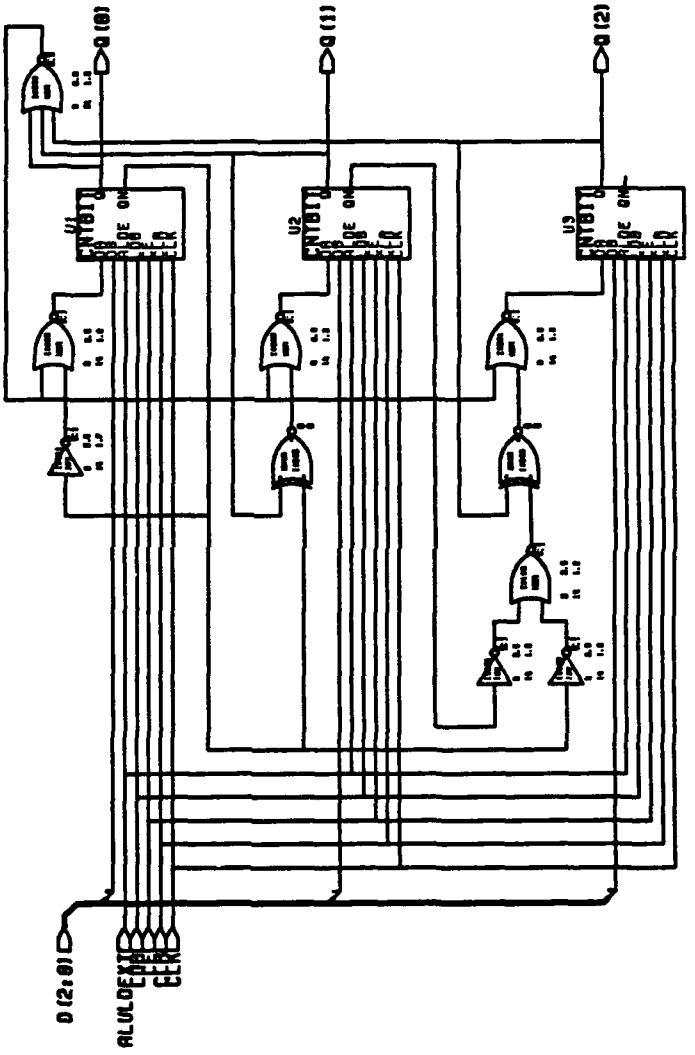

CNTBIT: mux + reg w/ synchronous clr
Q
QN
FB
DIN
CLK
CLR
ALOE
CE
DB
LOB
DA

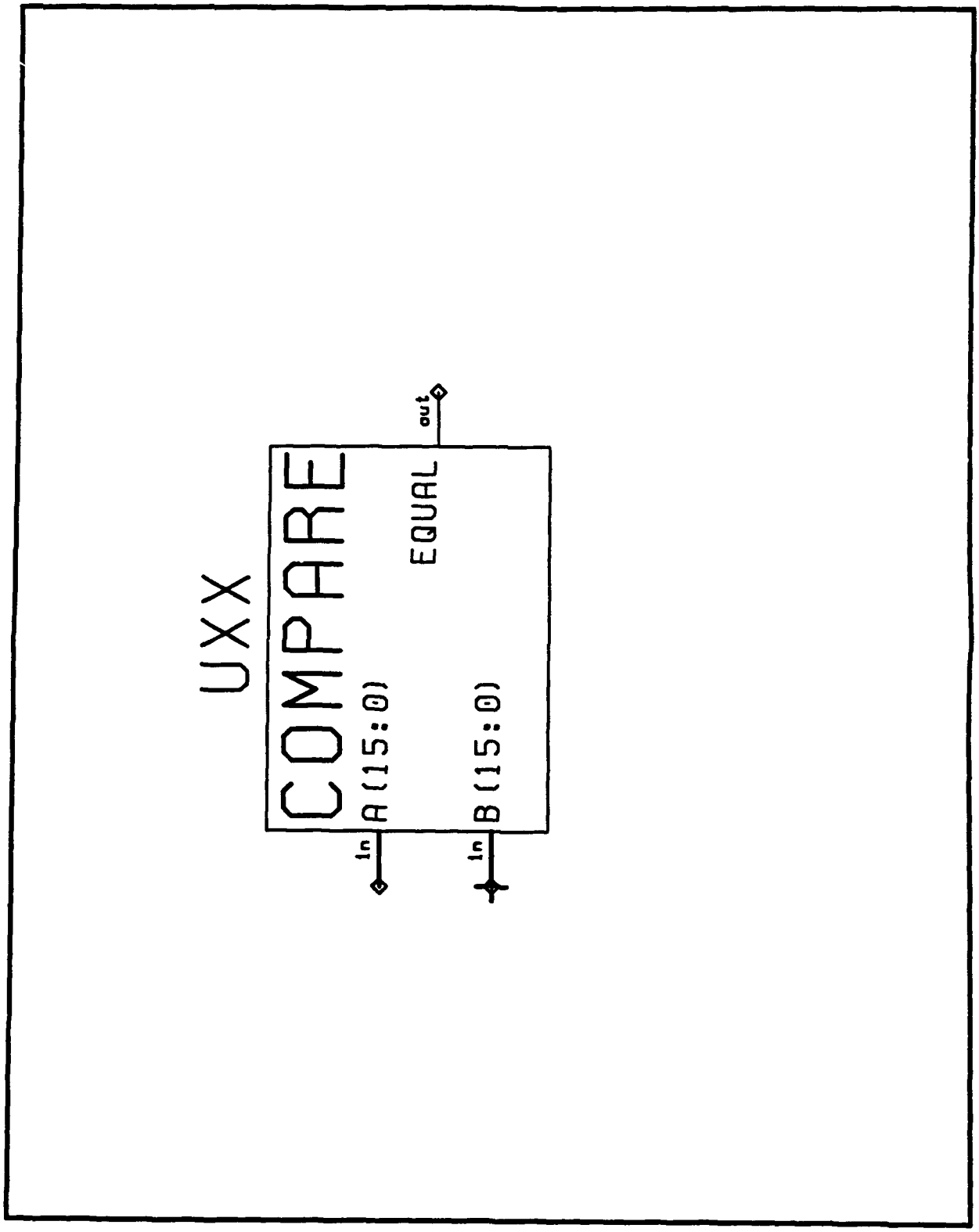

UXX
CNTDWN2
D(1:0)
LDB
ALULDEXT
CLR
CLK
CE
Q(1)
Q(0)
in
out

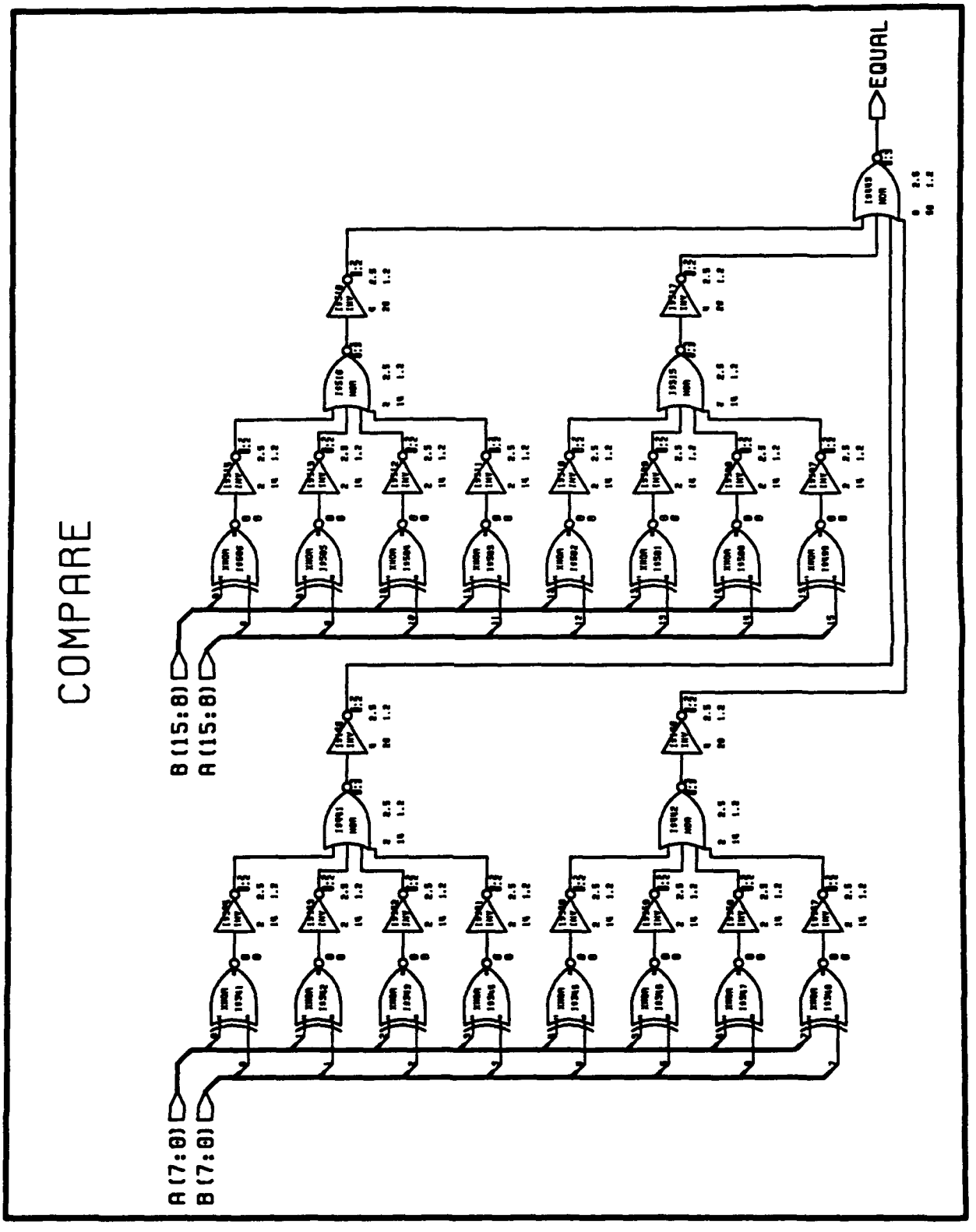

CNTDWN2
Q(0)
Q(1)
U1
U2
CNTBIT
Q
QN
DA
DB
DE
CEF
CLK
D(1:0)
ALULDEXT
CEF
CER

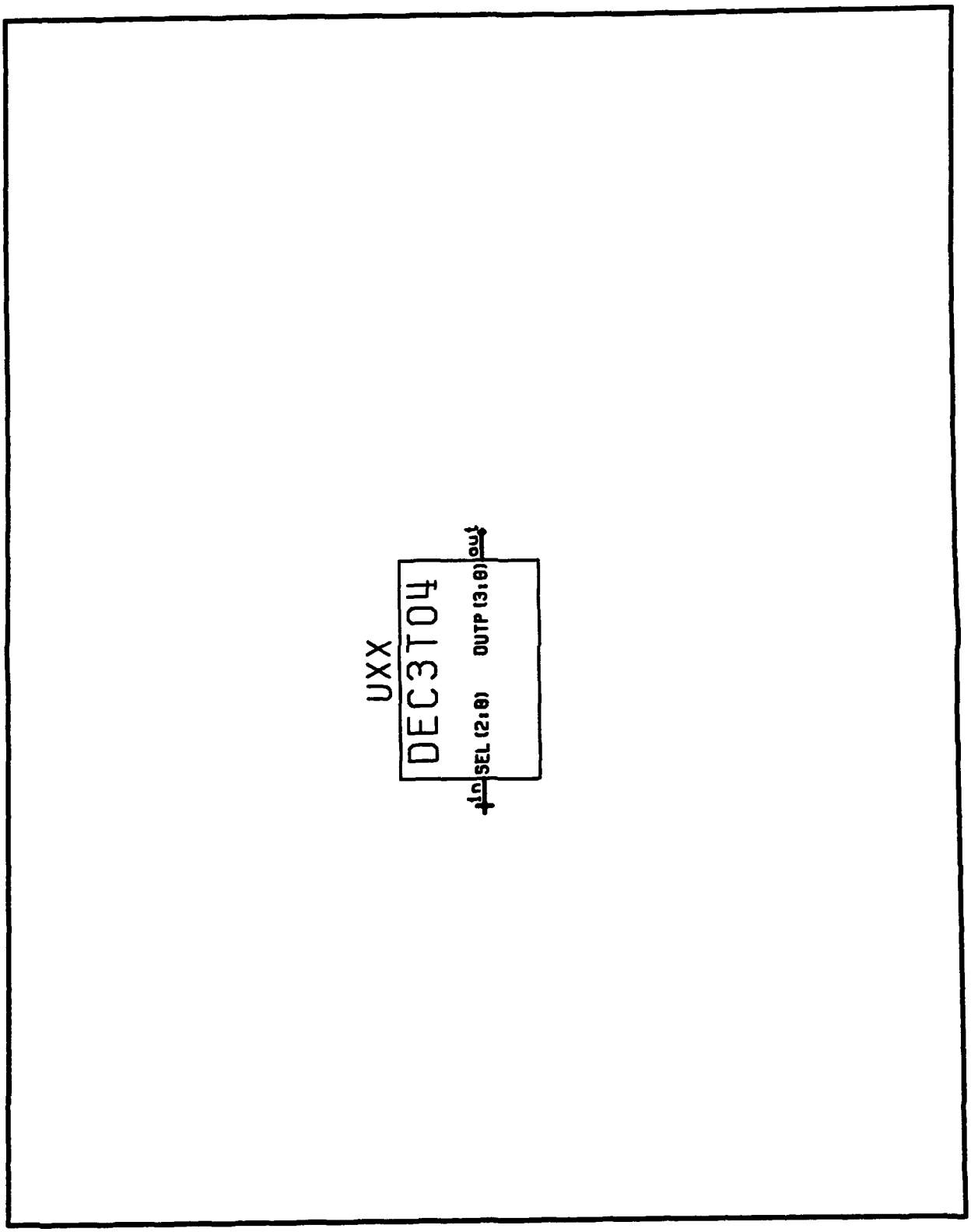

UXX
CNTDWN3
D(2:0)
LDB
ALULDEXT
CLR
CLK
CE
Q(2)
Q(1)
Q(0)
in
out

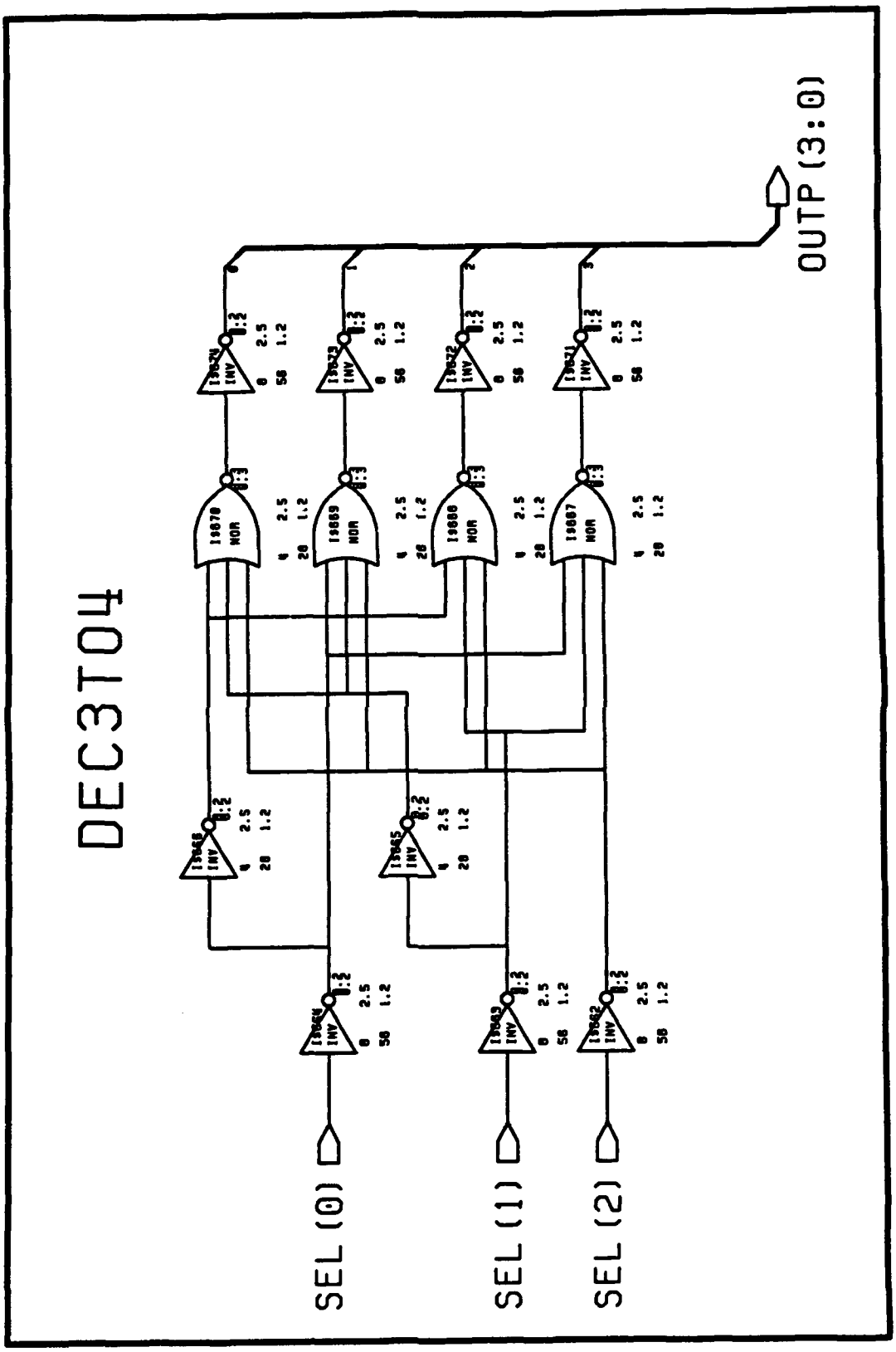
CNTDWN3

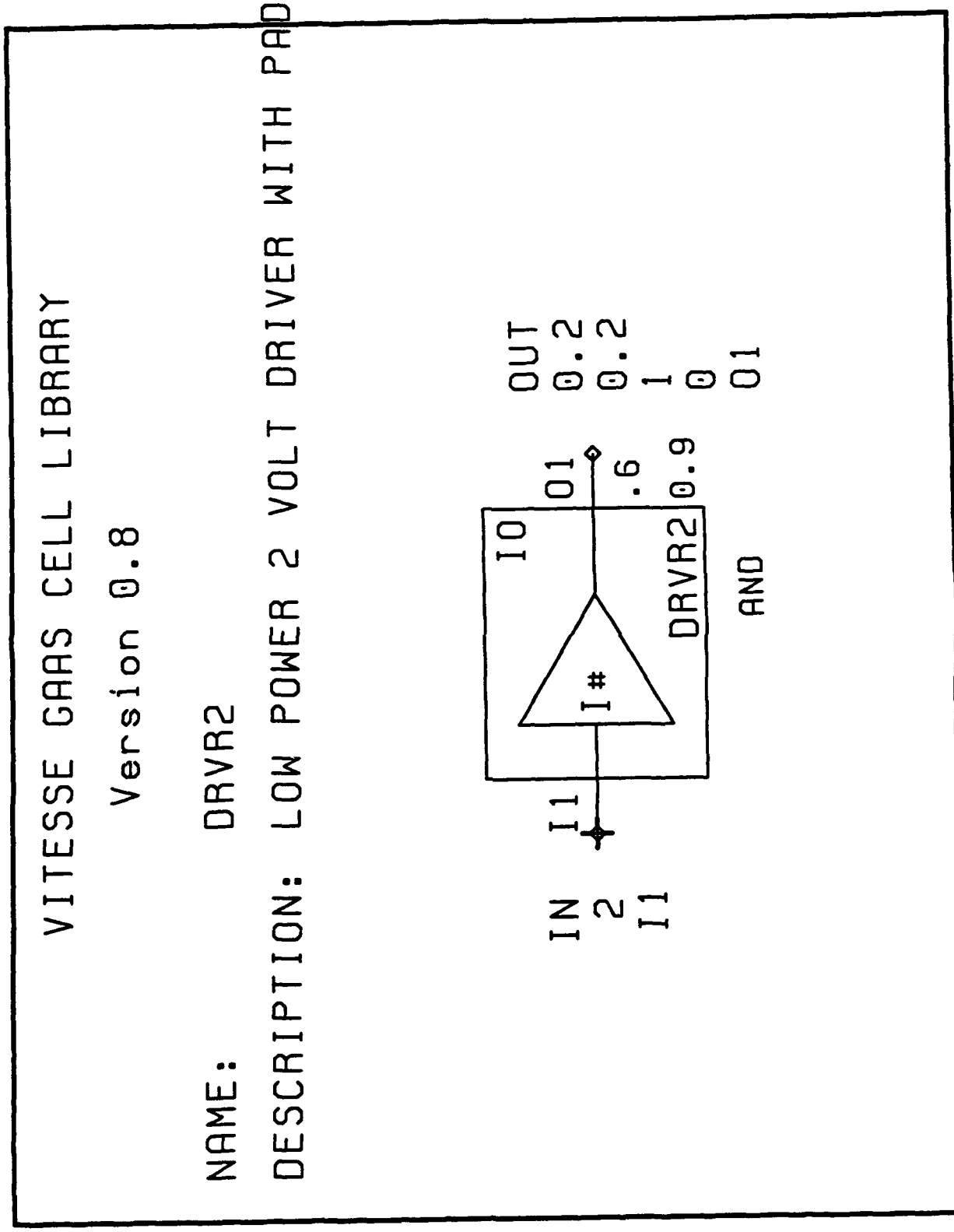


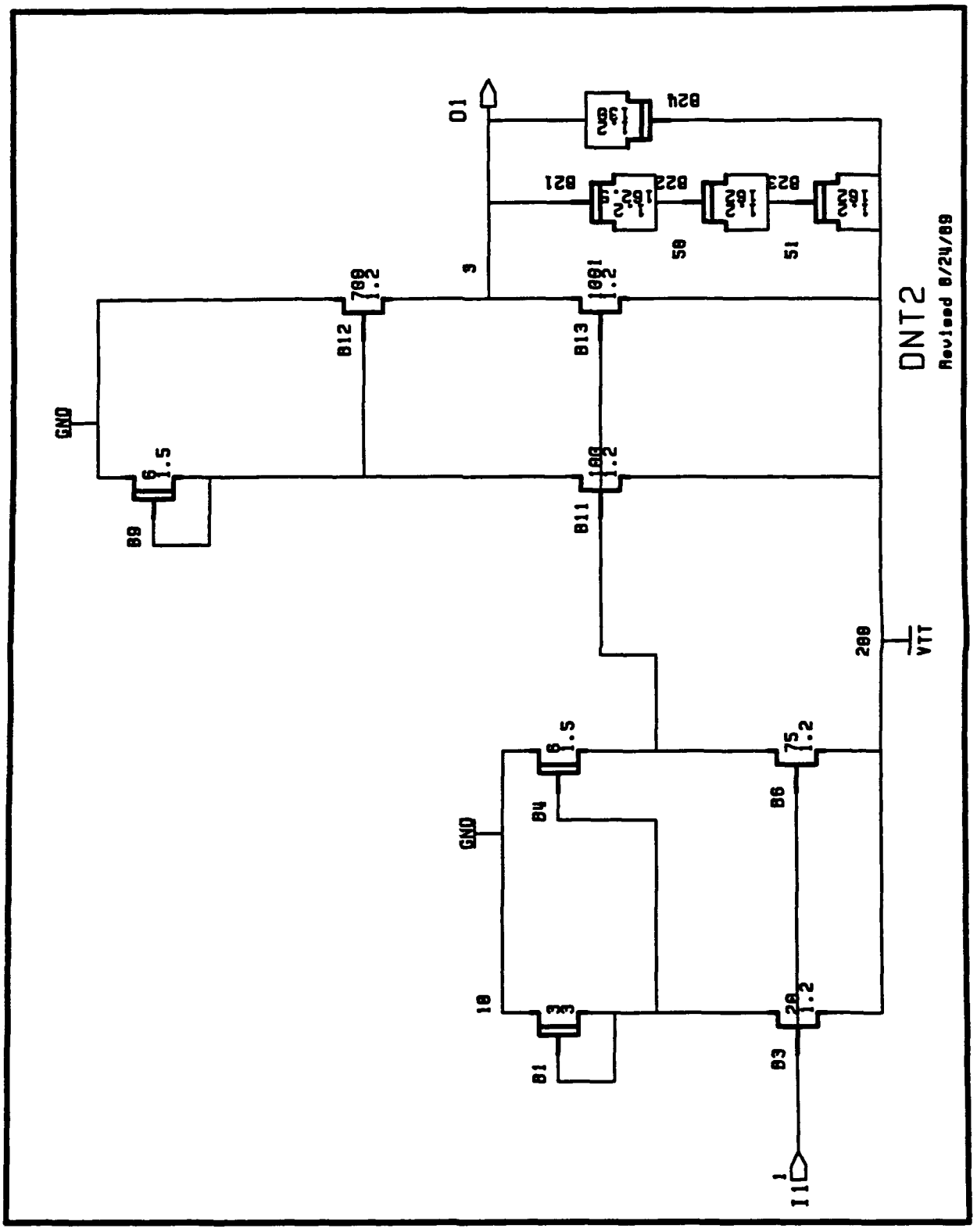

UXX
COMPARE
EQUAL
A(15:0)
B(15:0)
out
in
in

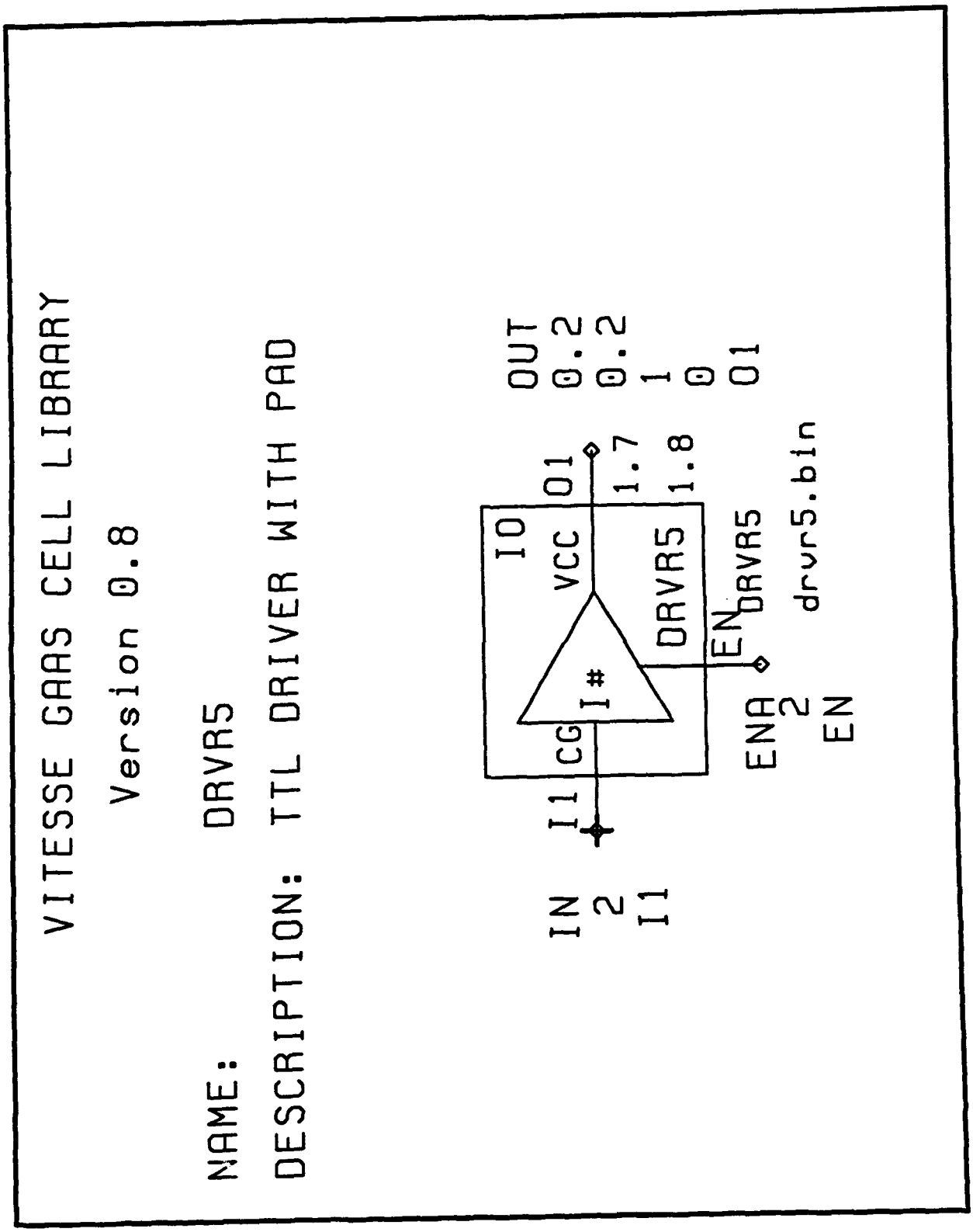

COMPARE
EQUAL
B(15:8)
A(15:8)
A(7:0)
B(7:0)

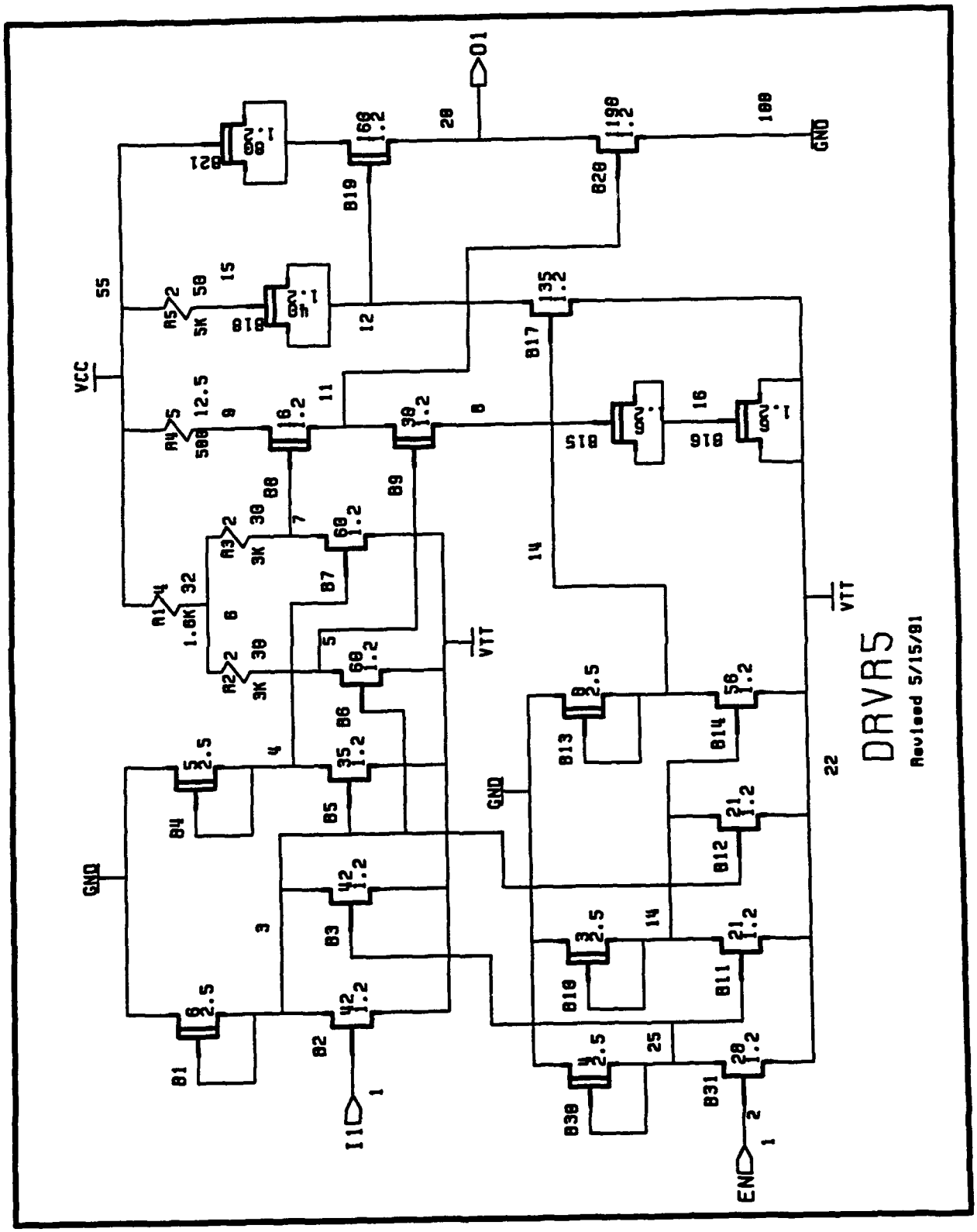

UXX
DEC3T04
OUTP (3:0)
SEL (2:0)

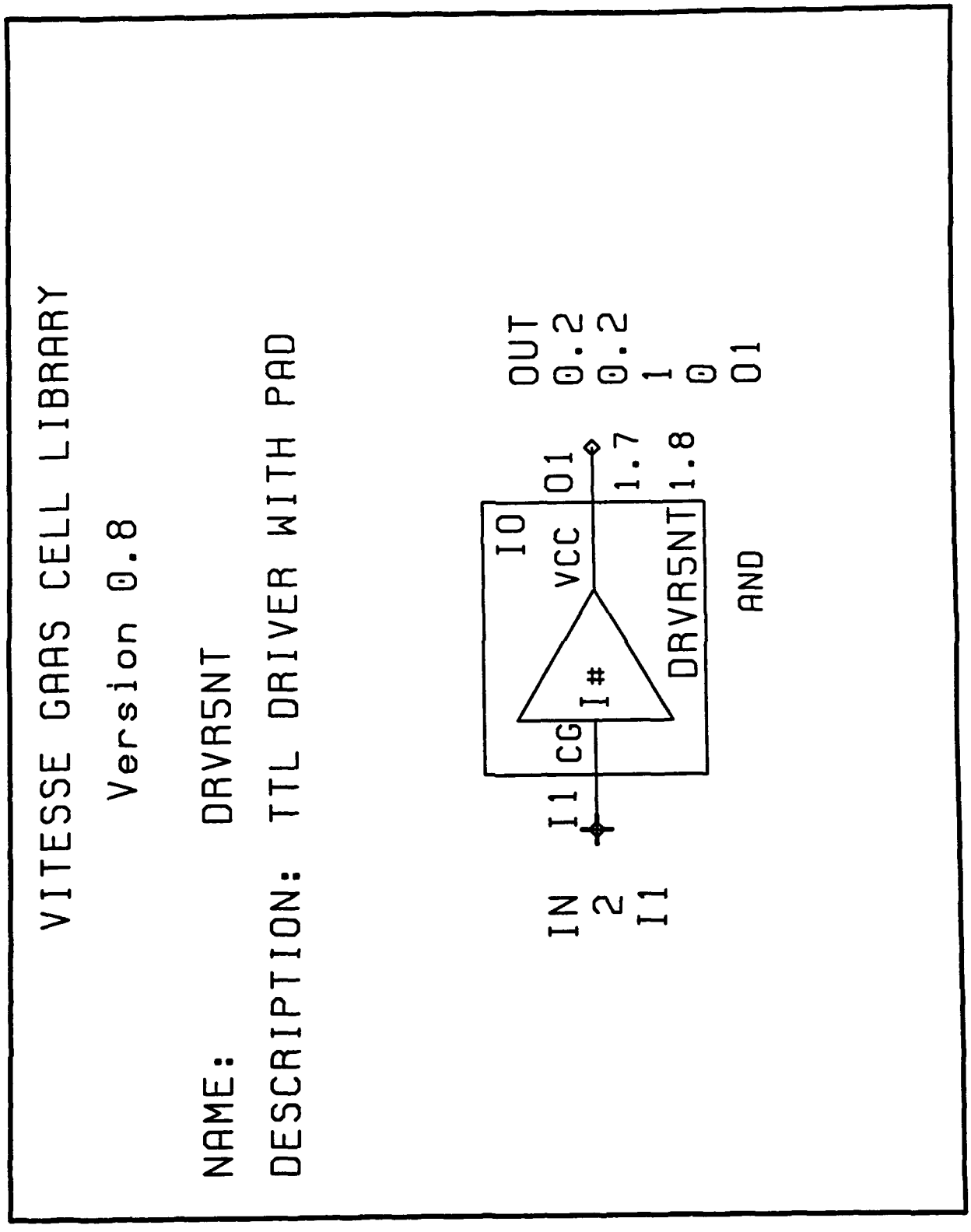

DEC3TO4
OUTP(3:0)
SEL(0)
SEL(1)
SEL(2)

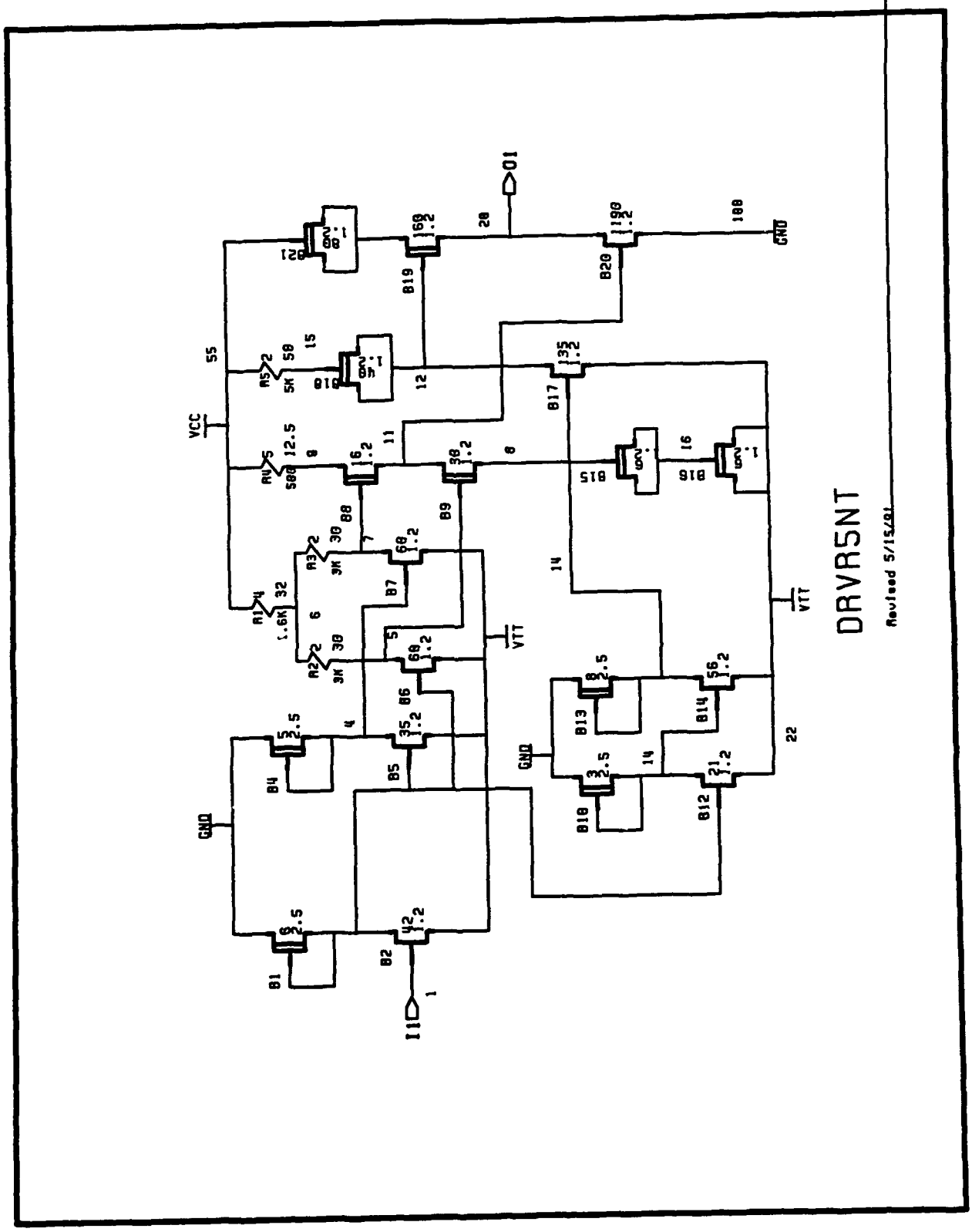

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: DRVR2
DESCRIPTION: LOW POWER 2 VOLT DRIVER WITH PAD
IN
2
I1
I1
IO
I#
O1
OUT
0.2
0.2
1
0
O1
.6
0.9
DRVR2
AND

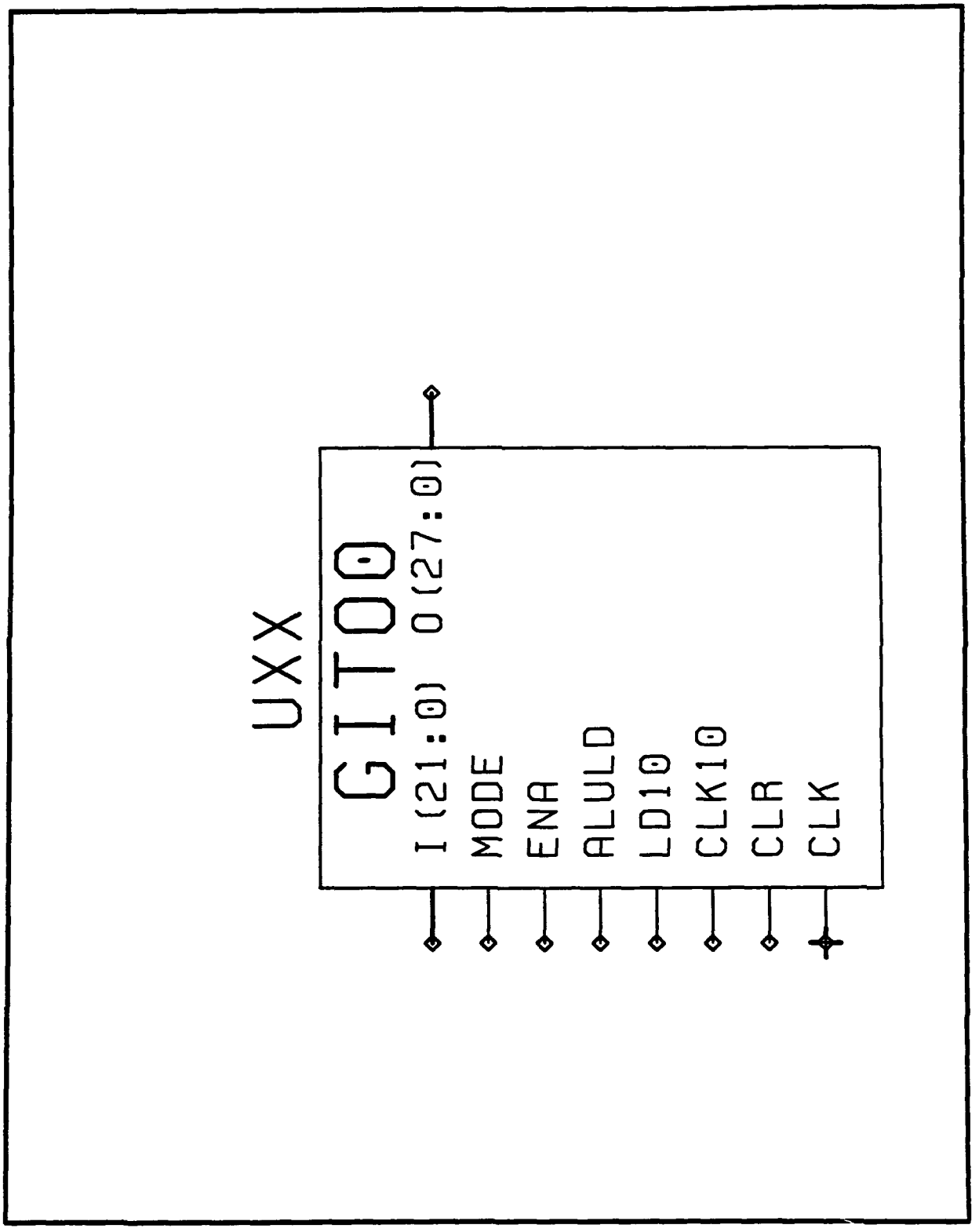

DNT2
Revised 8/24/89
GND
VTT
I1
I0
B1
B3
B4
B6
B8
B9
B11
B12
B13
B21
B22
B23
B24
50
51
5
10
200

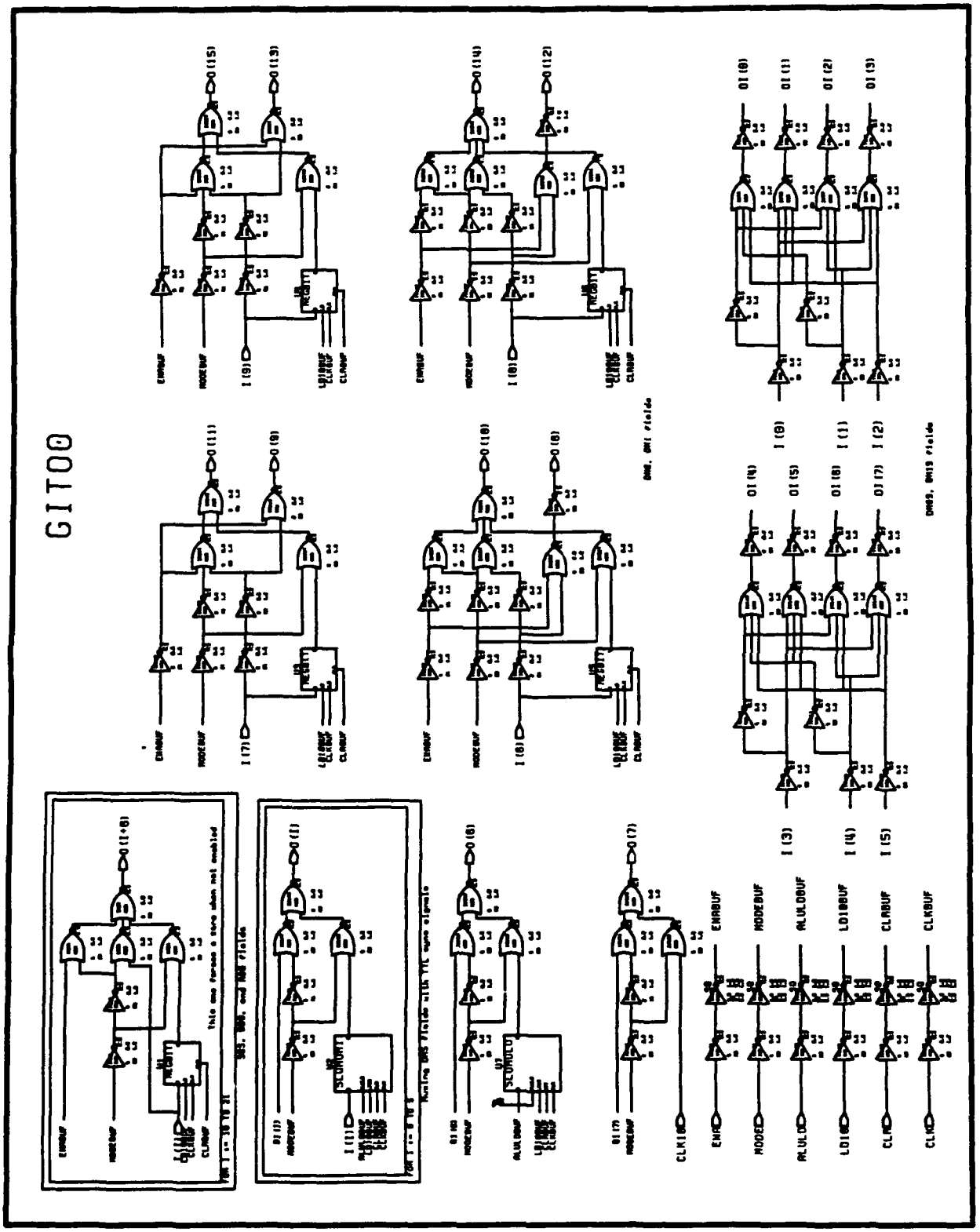

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: DRVR5
DESCRIPTION: TTL DRIVER WITH PAD
IO
VCC
DRVR5
I#
CG
I1
O1
EN
DRVR5
drvr5.bin
OUT
0.2
0.2
1
0
01
1.7
1.8
IN
2
I1
ENA
2
EN

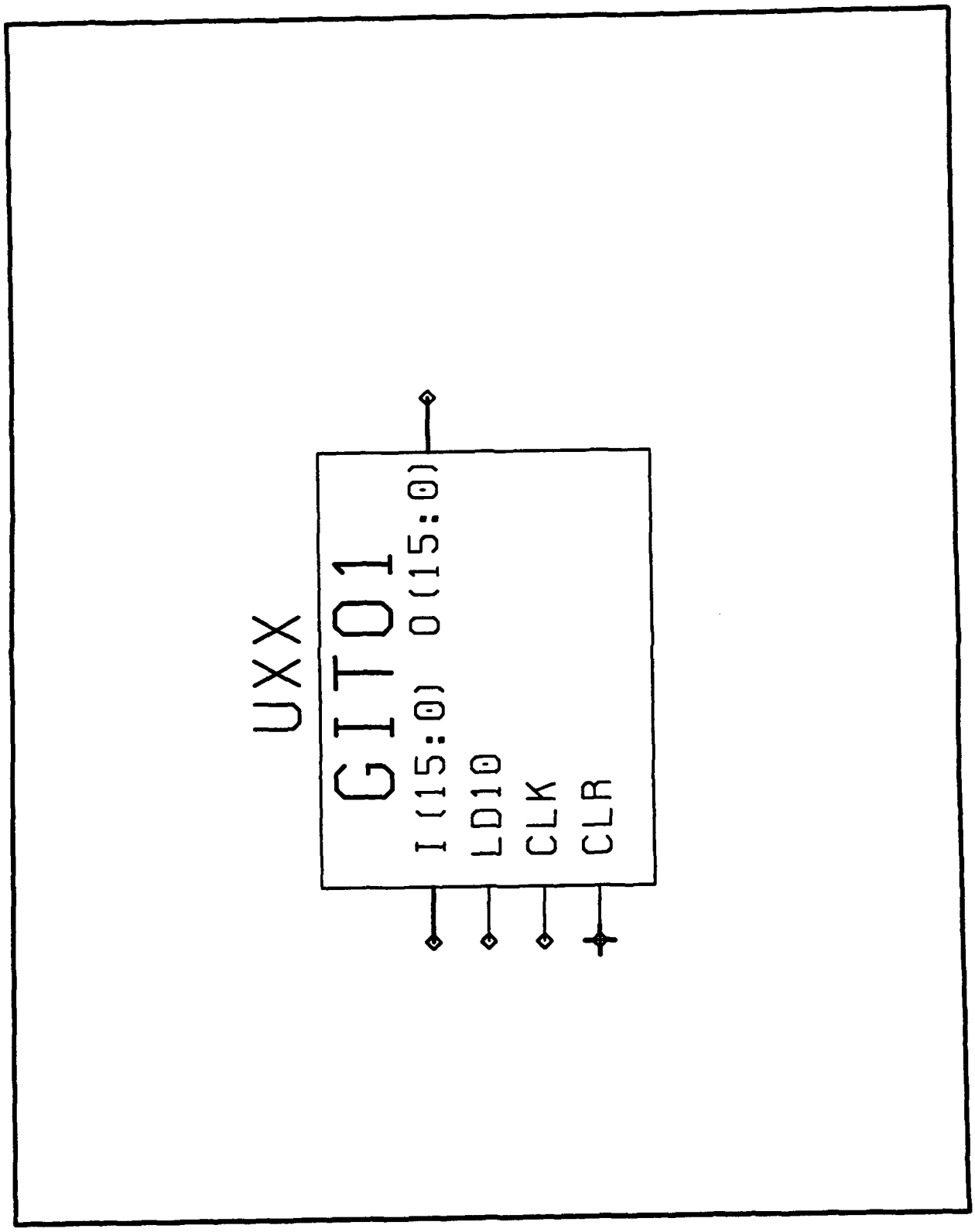

DRVR5
Revised 5/15/91
VCC
GND
VTT
I1
O1
END

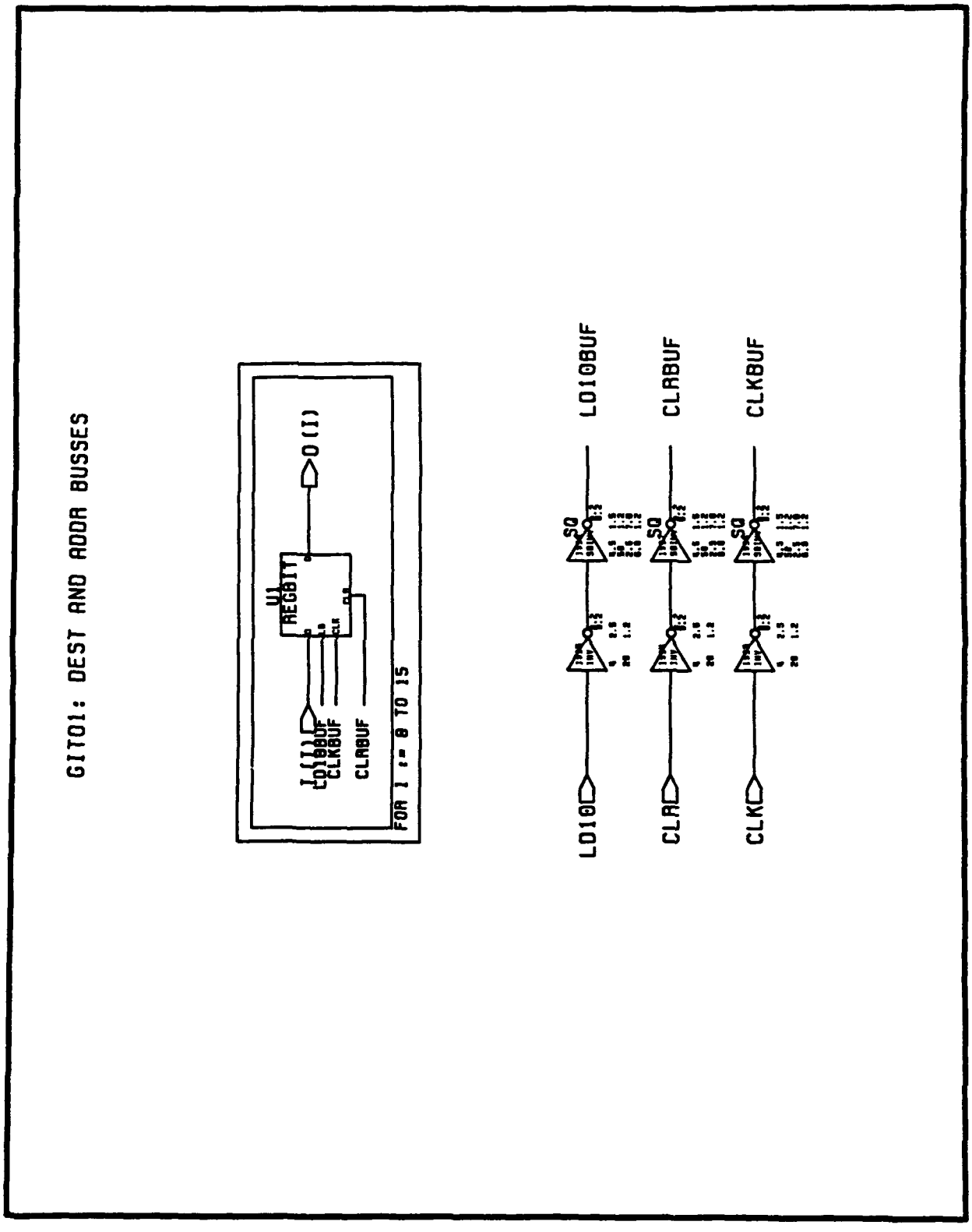

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: DRVR5NT
DESCRIPTION: TTL DRIVER WITH PAD
IN
2
I1
I1
CG
I#
IO
VCC
O1
DRVR5NT
OUT
0.2
0.2
1
0
O1
1.7
1.8
AND

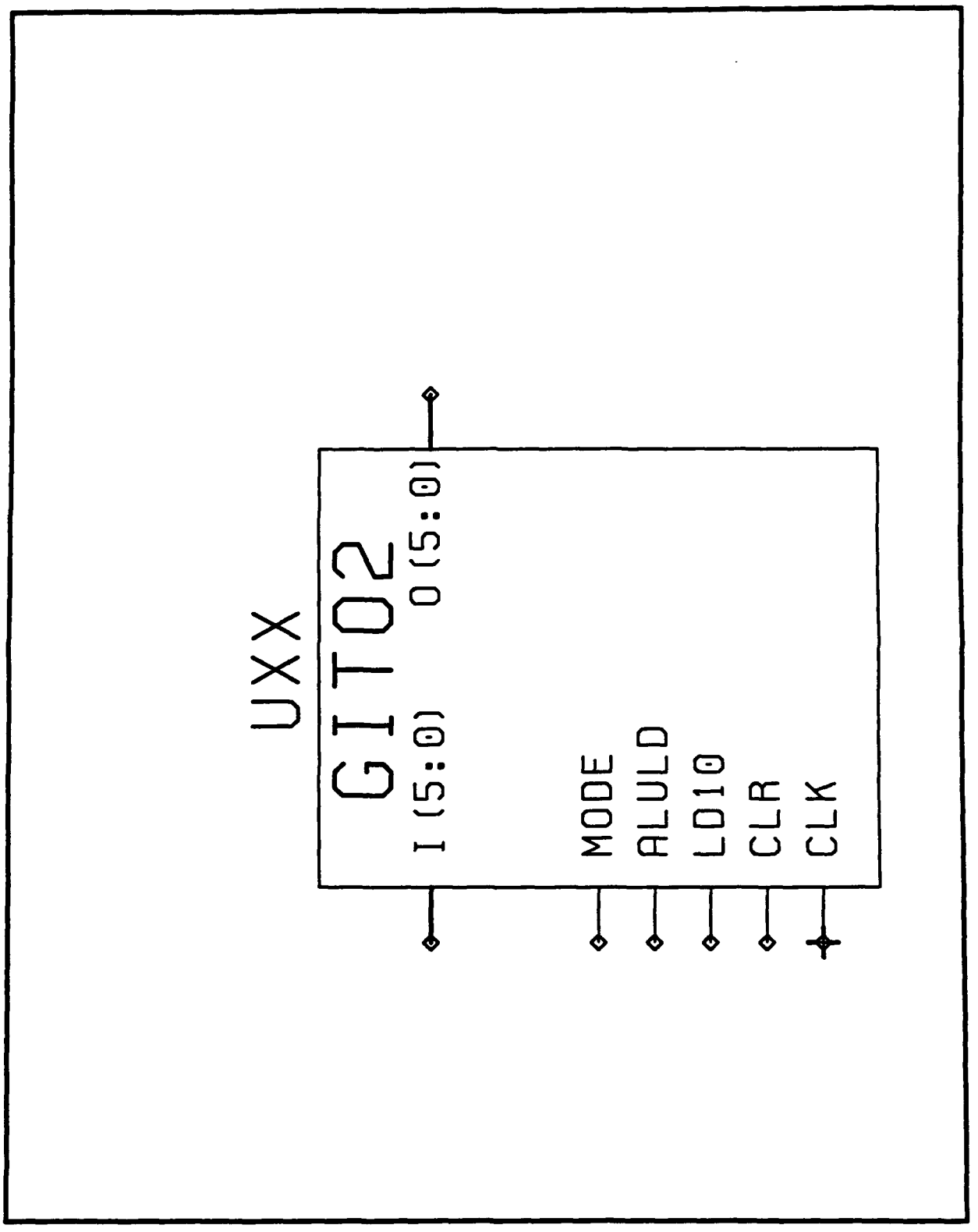

DRVR5NT
Revised 5/15/91
VCC
GND
VTT
I1
O1


UXX
GITOO
I(21:0)
O(27:0)
MODE
ENA
ALULD
LD10
CLK10
CLR
CLK

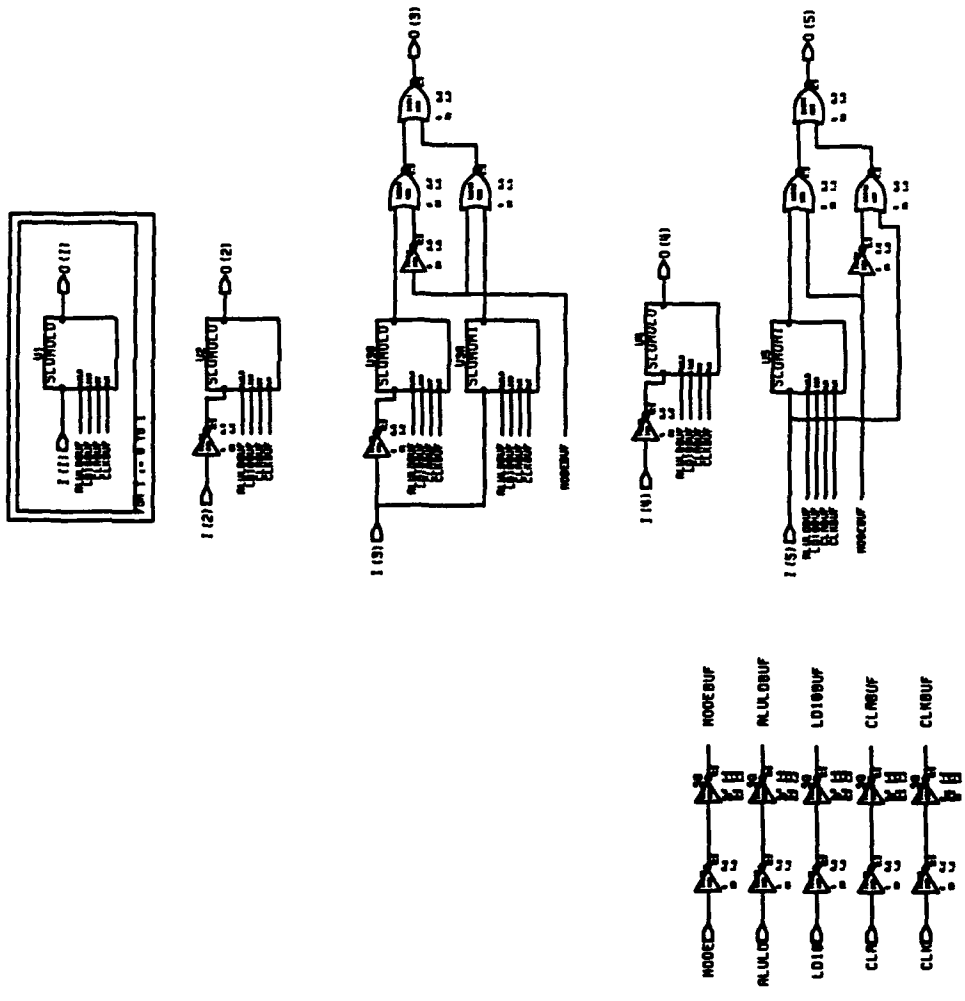

GITOO

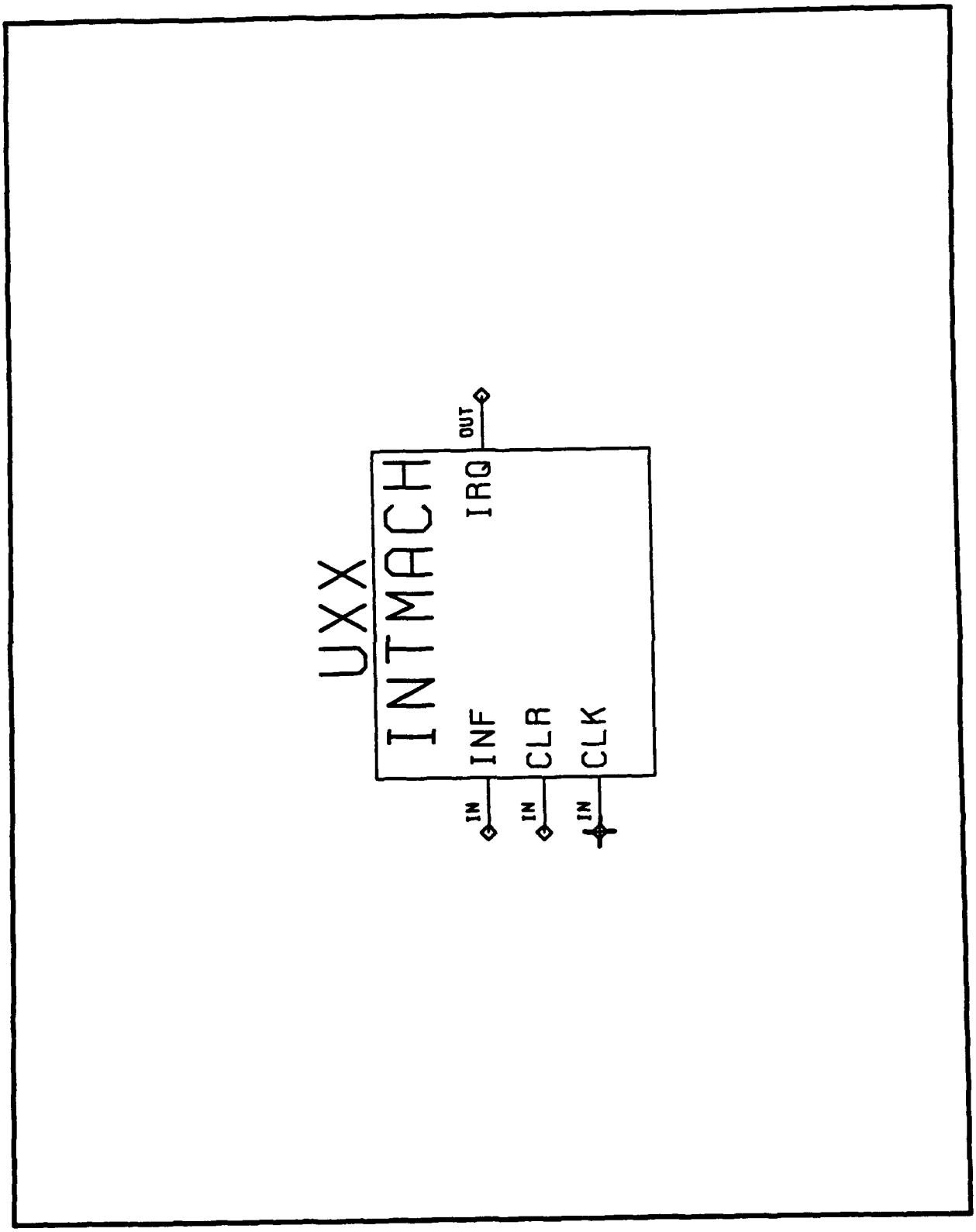

UXX
GIT01
I(15:0)
O(15:0)
LD10
CLK
CLR

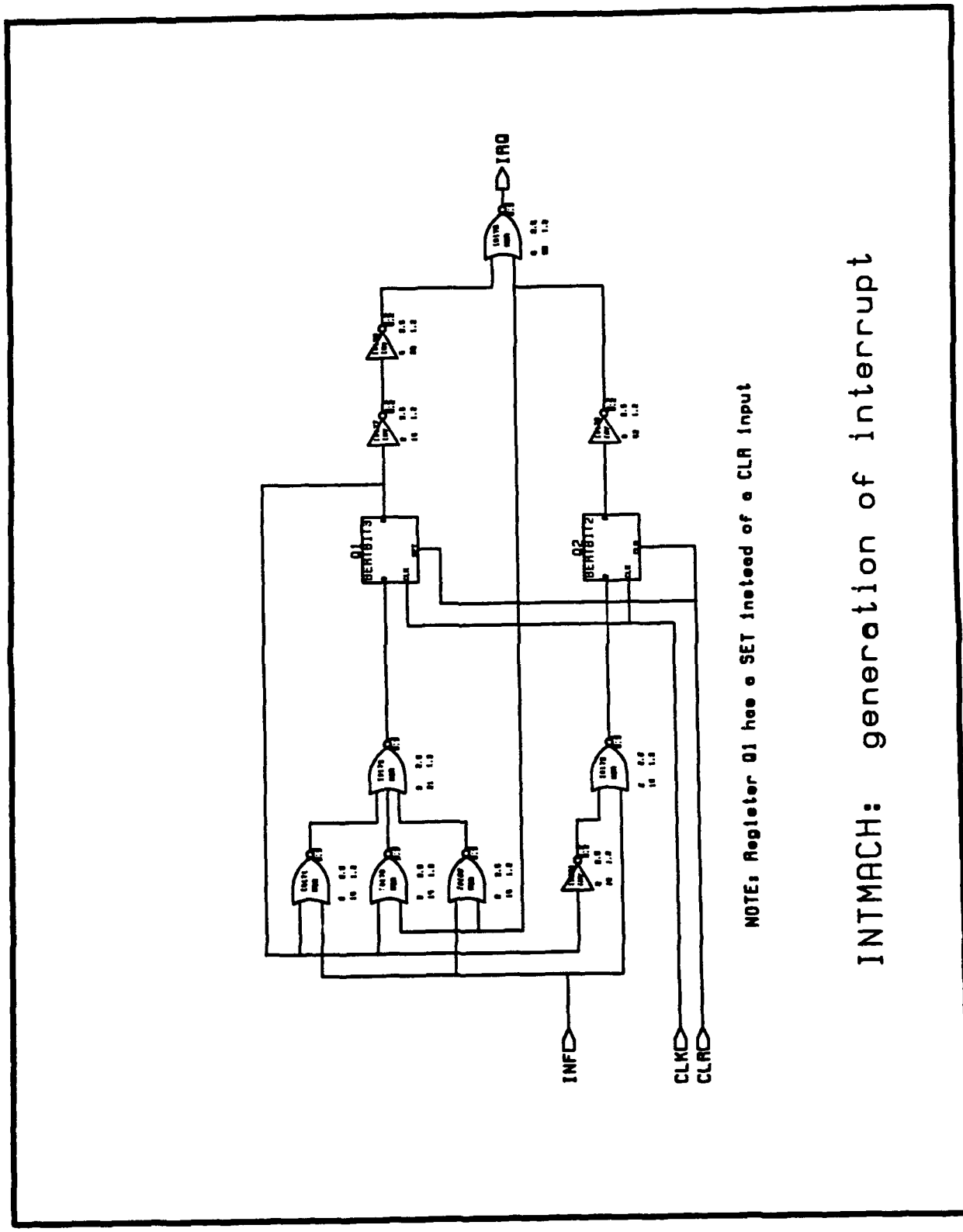

GIT01: DEST AND ADDR BUSSES
U1
REGBIT
O(I)
I(I)
LD10BUF
CLKBUF
CLRBUF
FOR I := 0 TO 15
LD10BUF
CLRBUF
CLKBUF
SQ
SQ
SQ
LD10
CLR
CLK

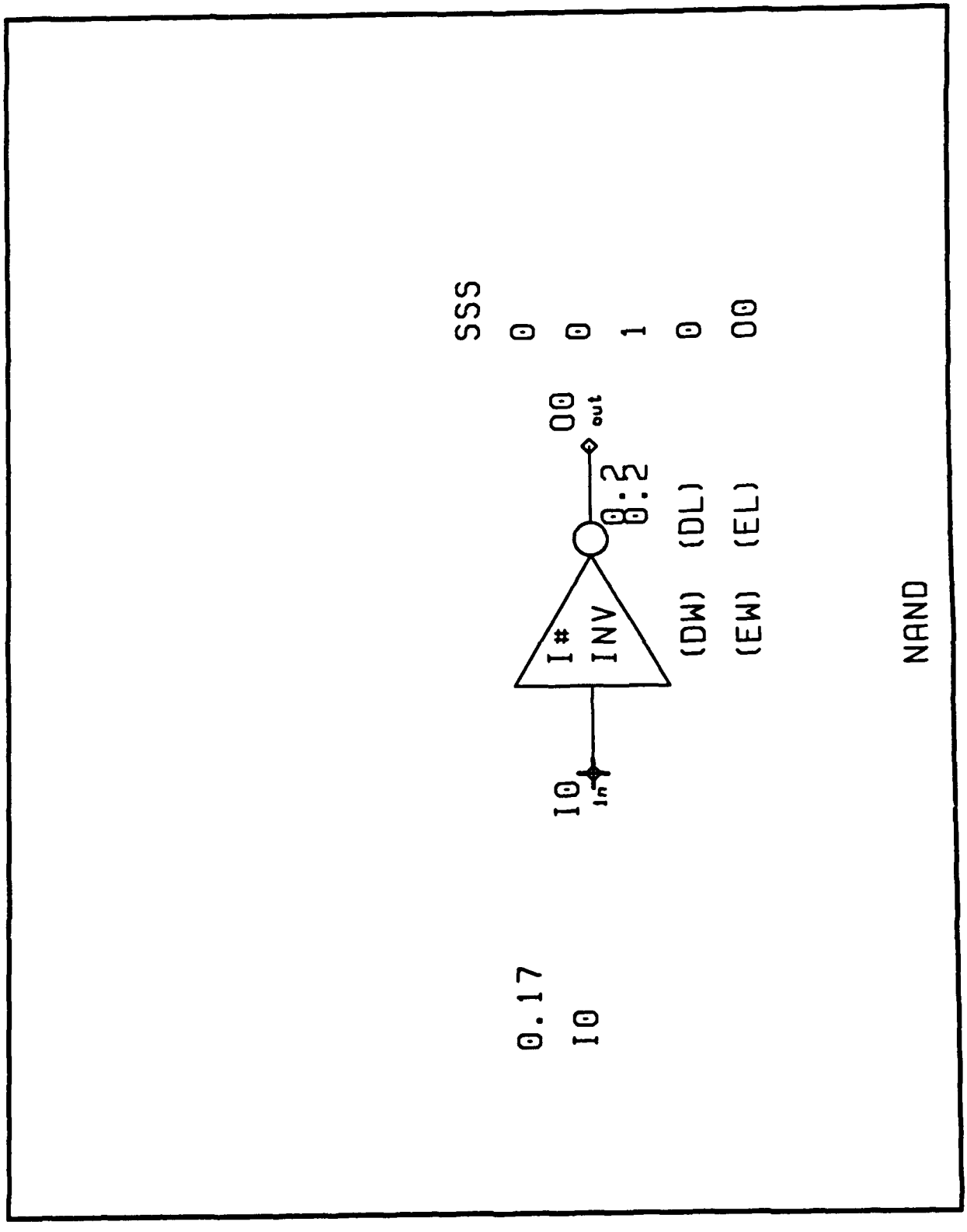

UXX
GIT02
I(5:0)
O(5:0)
MODE
ALULD
LD10
CLR
CLK

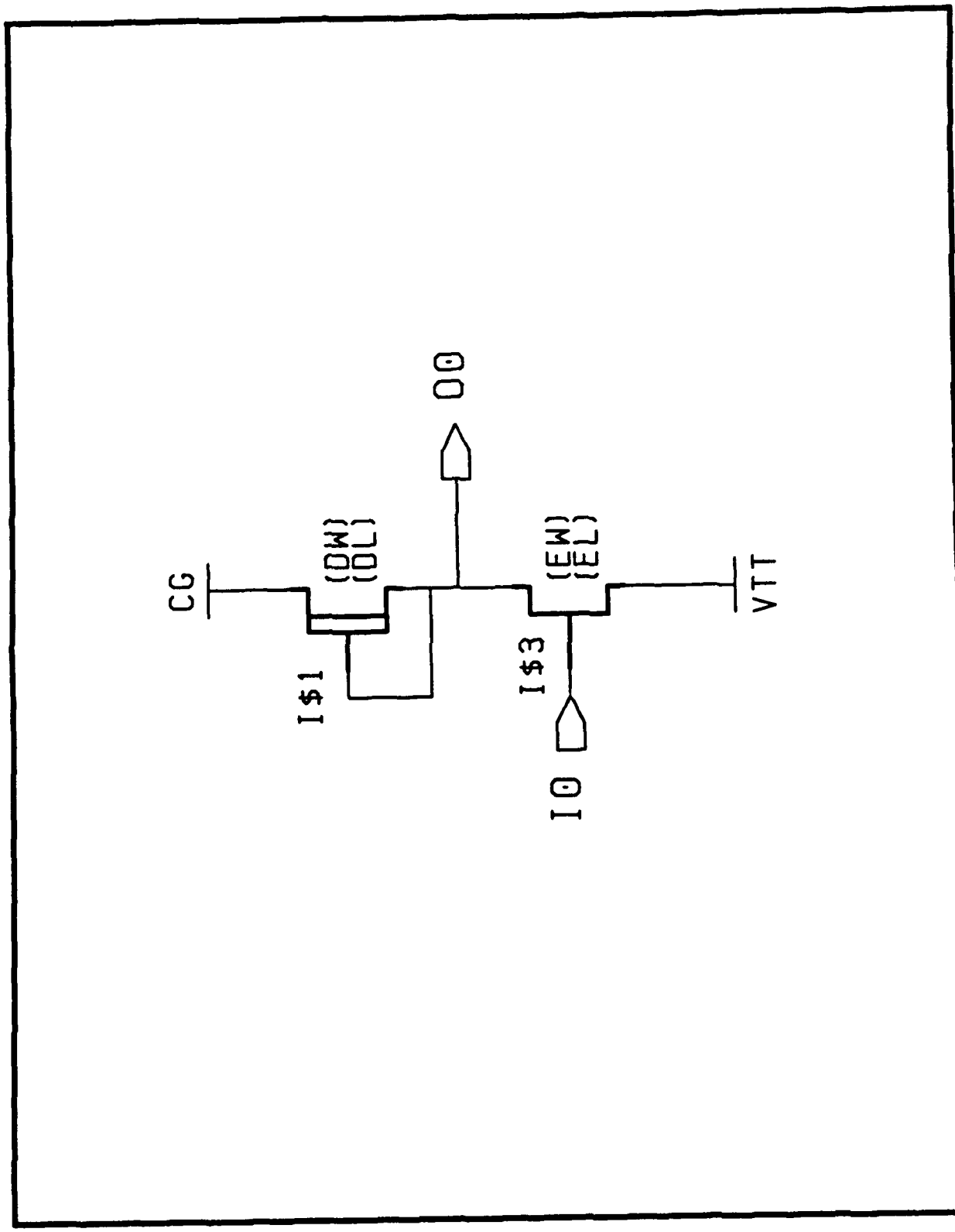
GIT02

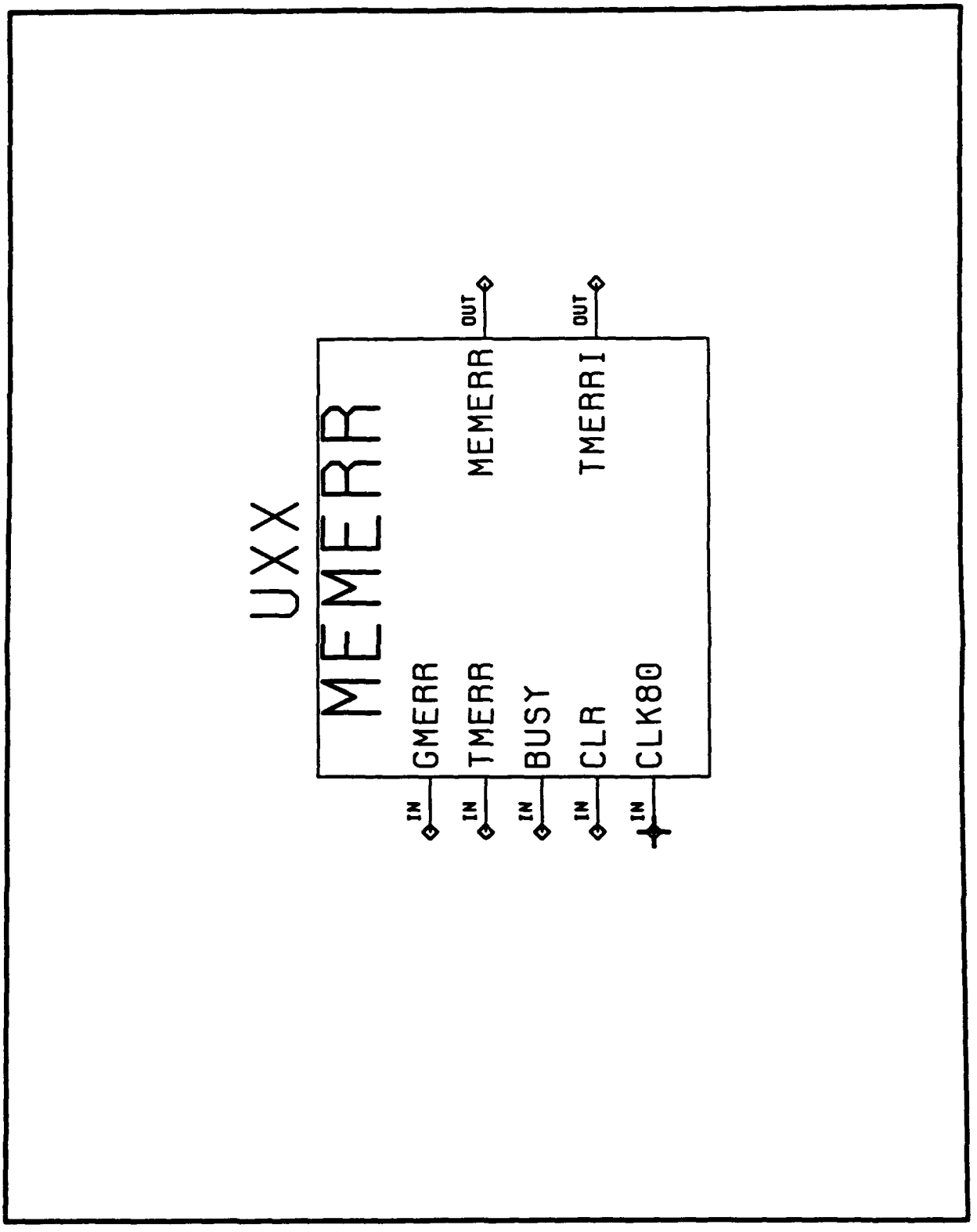


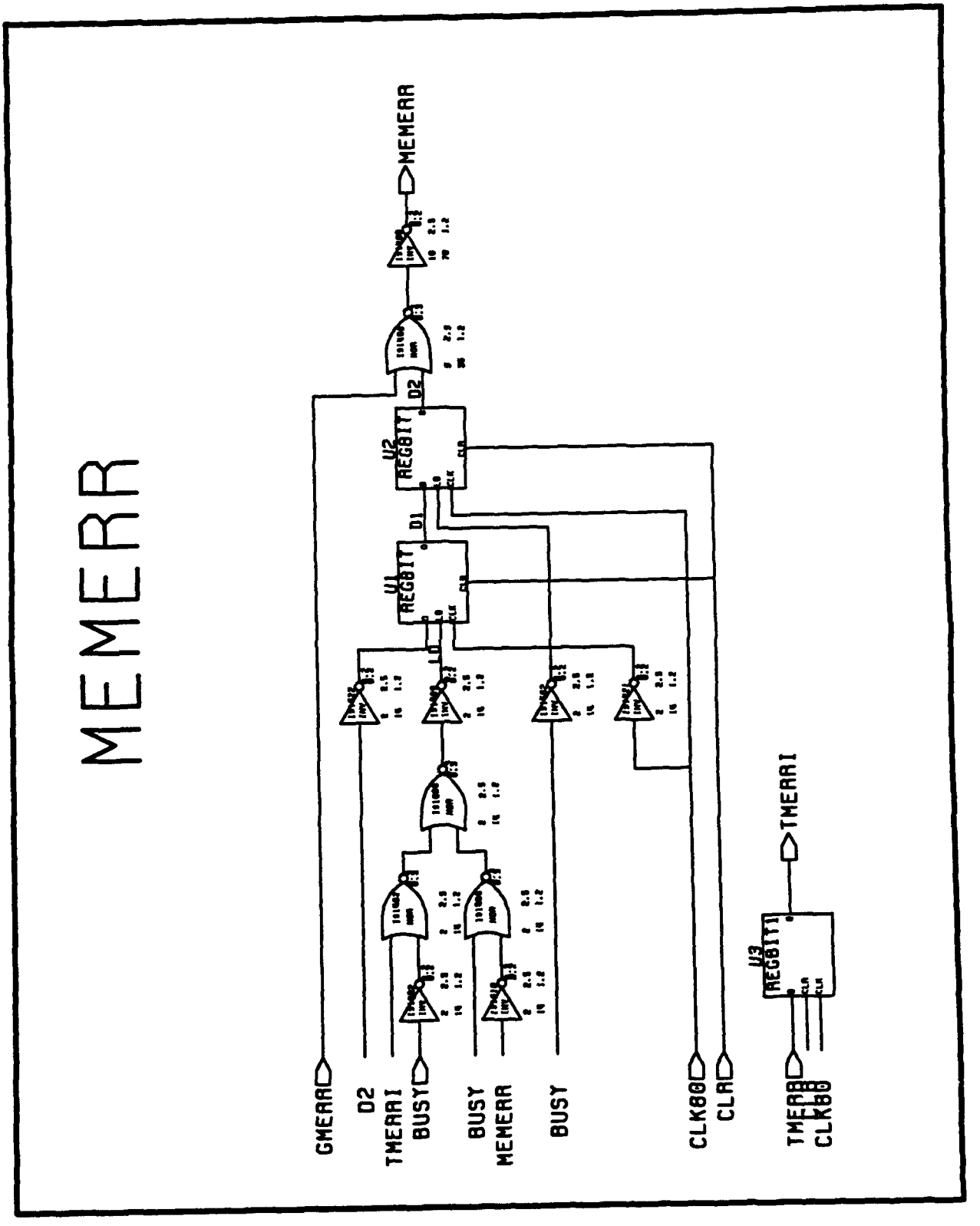

UXX
INTMACH
OUT
IRQ
INF
CLR
CLK
IN
IN
IN

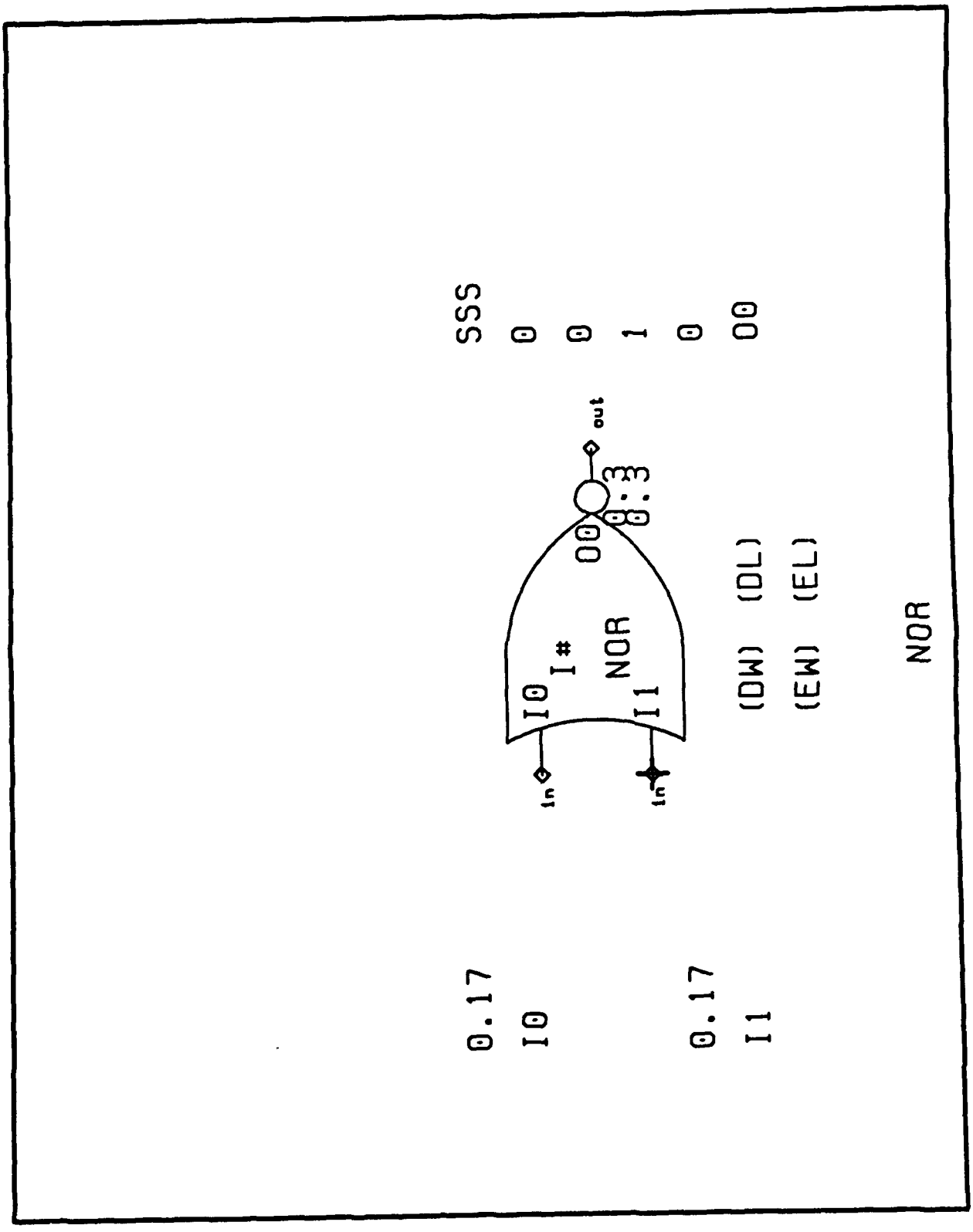

IRQ
Q1
BEN1BIT3
Q2
BEN1BIT2
INF
CLK
CLR
NOTE: Register Q1 has a SET instead of a CLR input
INTMACH: generation of interrupt

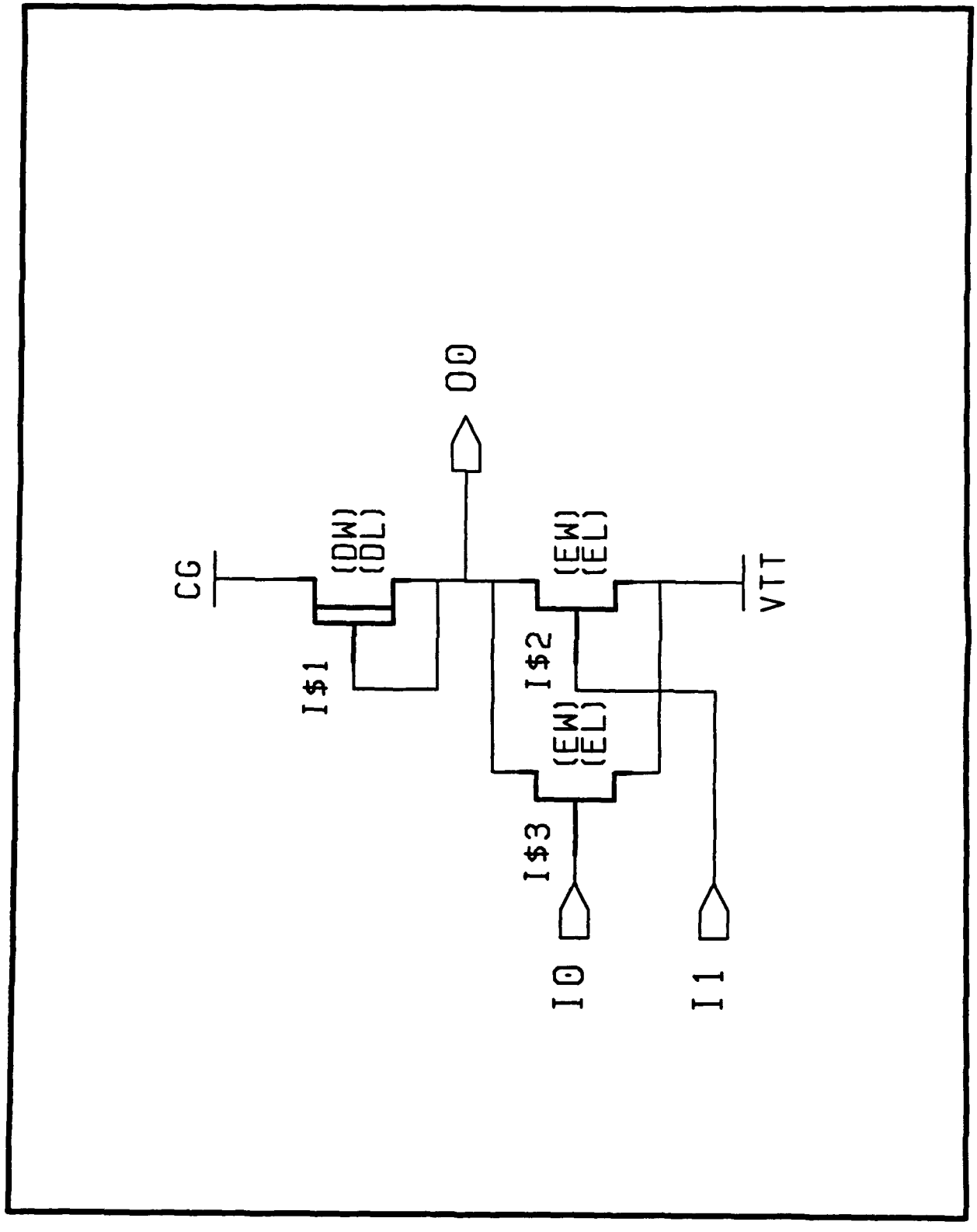

SSS
0 0 1 0 00
00
out
8.2
I# INV
(DW) (DL)
(EW) (EL)
NAND
I0
in
0.17
I0

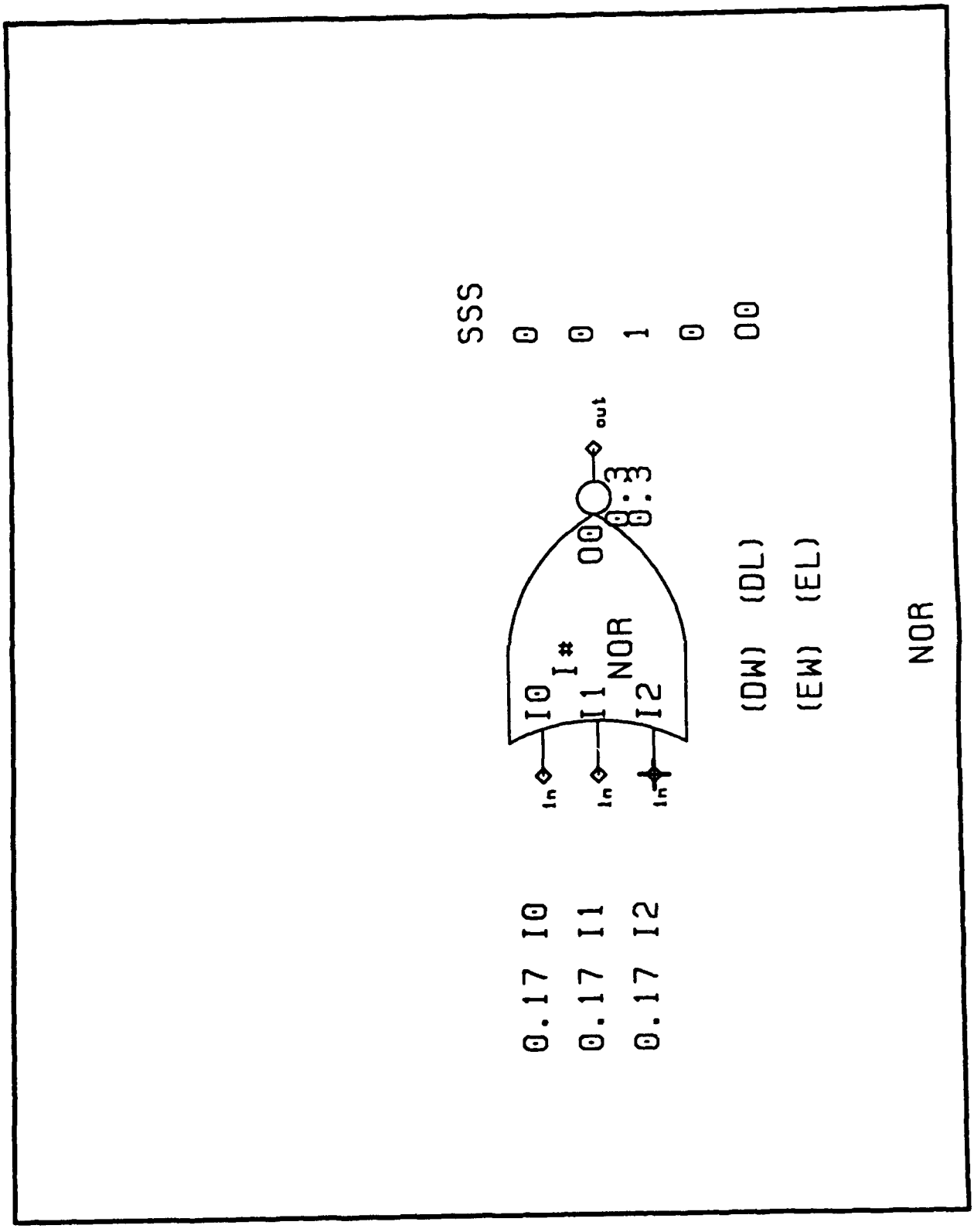

O0
CG
(DW)
(DL)
(EW)
(EL)
VTT
I$1
I$3
IO

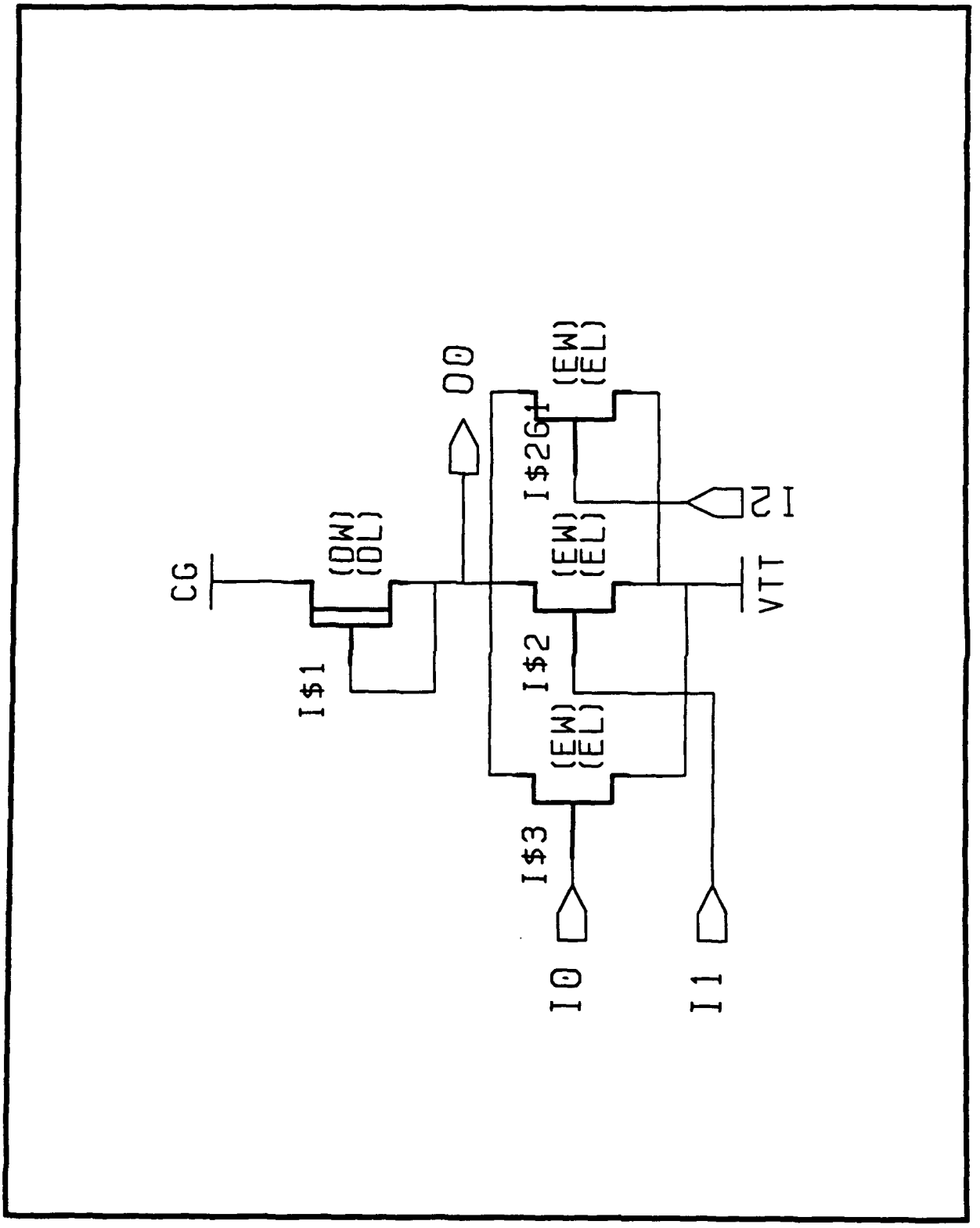

UXX
MEMERR
GMERR
TMERR
BUSY
CLR
CLK80
IN
IN
IN
IN
IN
MEMERR
TMERRI
OUT
OUT

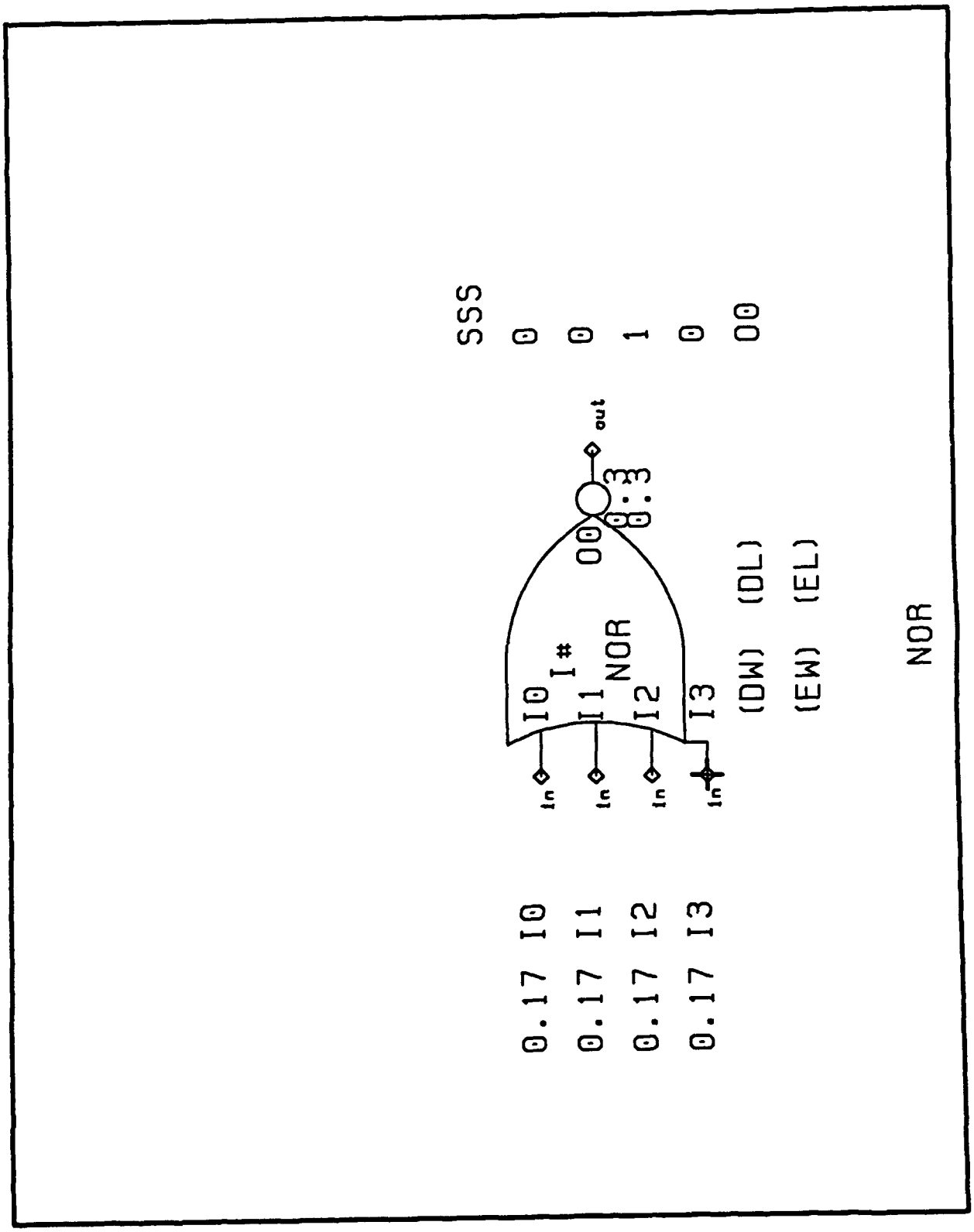

MEMERR
MEMERR
D2
REGBIT
U2
D1
REGBIT
U1
TMERR1
REGBIT
U3
GMERR
D2
TMERR1
BUSY
BUSY
MEMERR
BUSY
CLK80
CLR
TMERR
CLK80

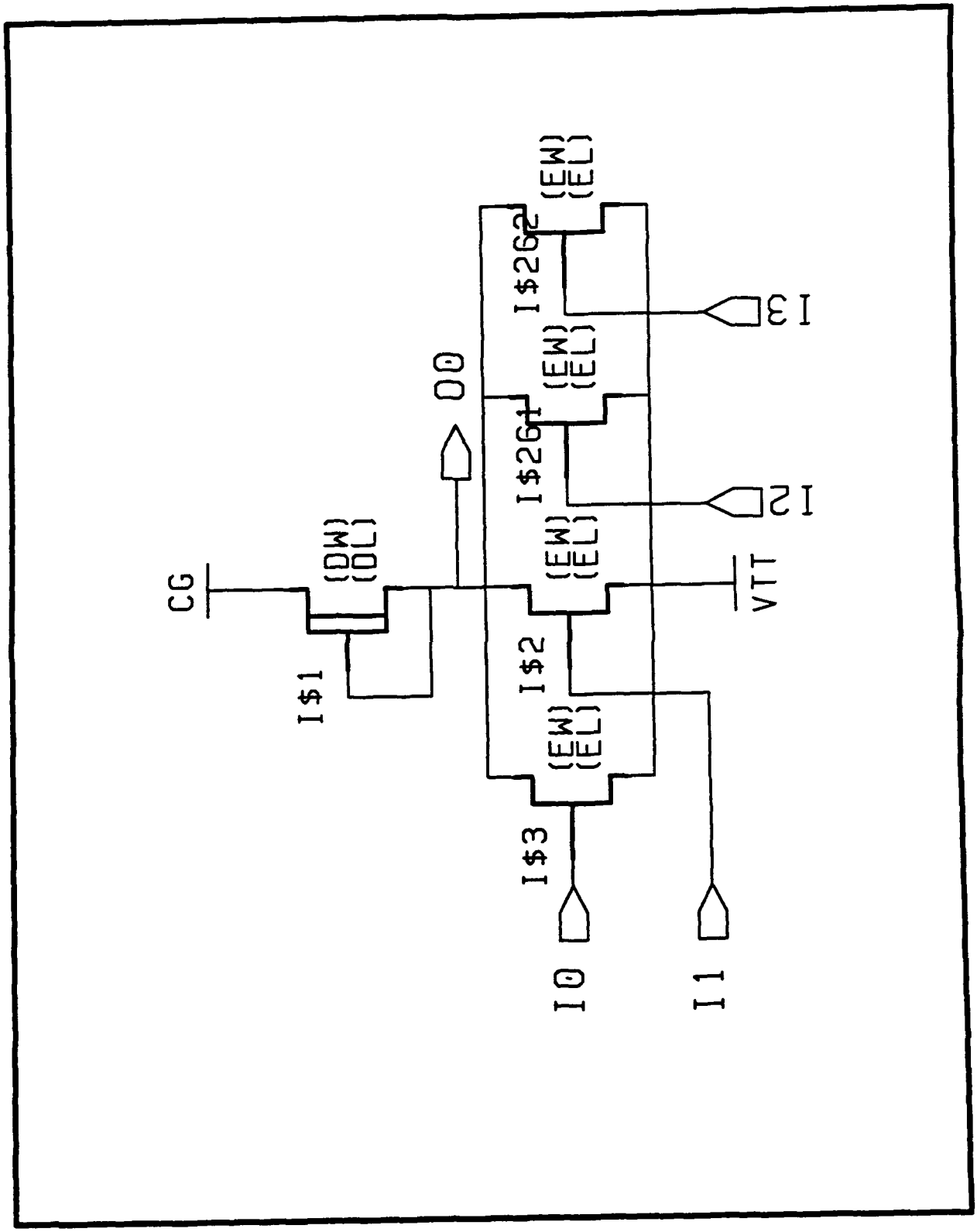

SSS
0 0 1 0 00
out
3.3
00
I0
I#
NOR
I1
in
in
(DW) (DL)
(EW) (EL)
NOR
0.17
I0
0.17
I1

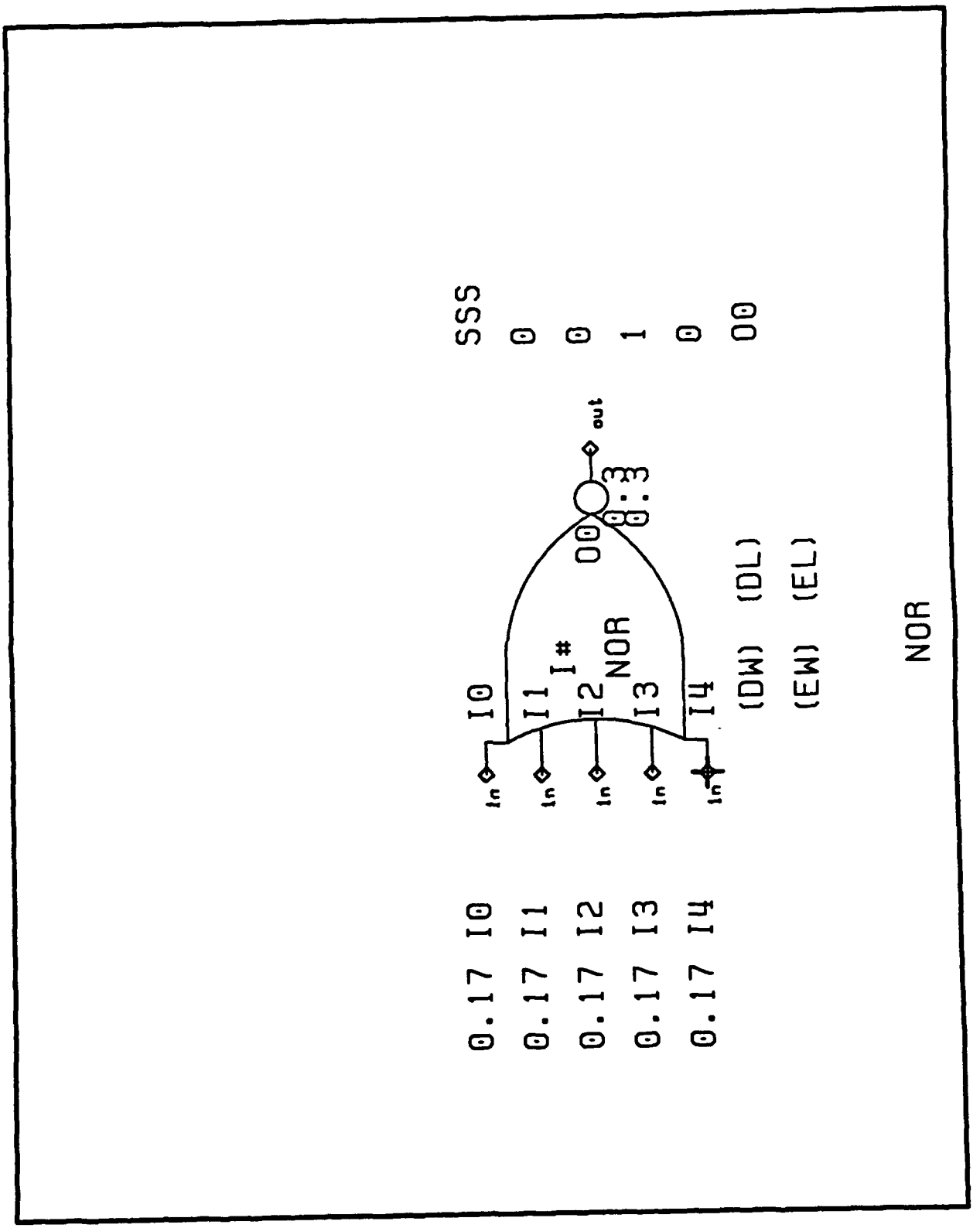

O0
CG
(DW)
(DL)
(EW)
(EL)
VTT
I$1
I$2
(EW)
(EL)
I$3
I0
I1

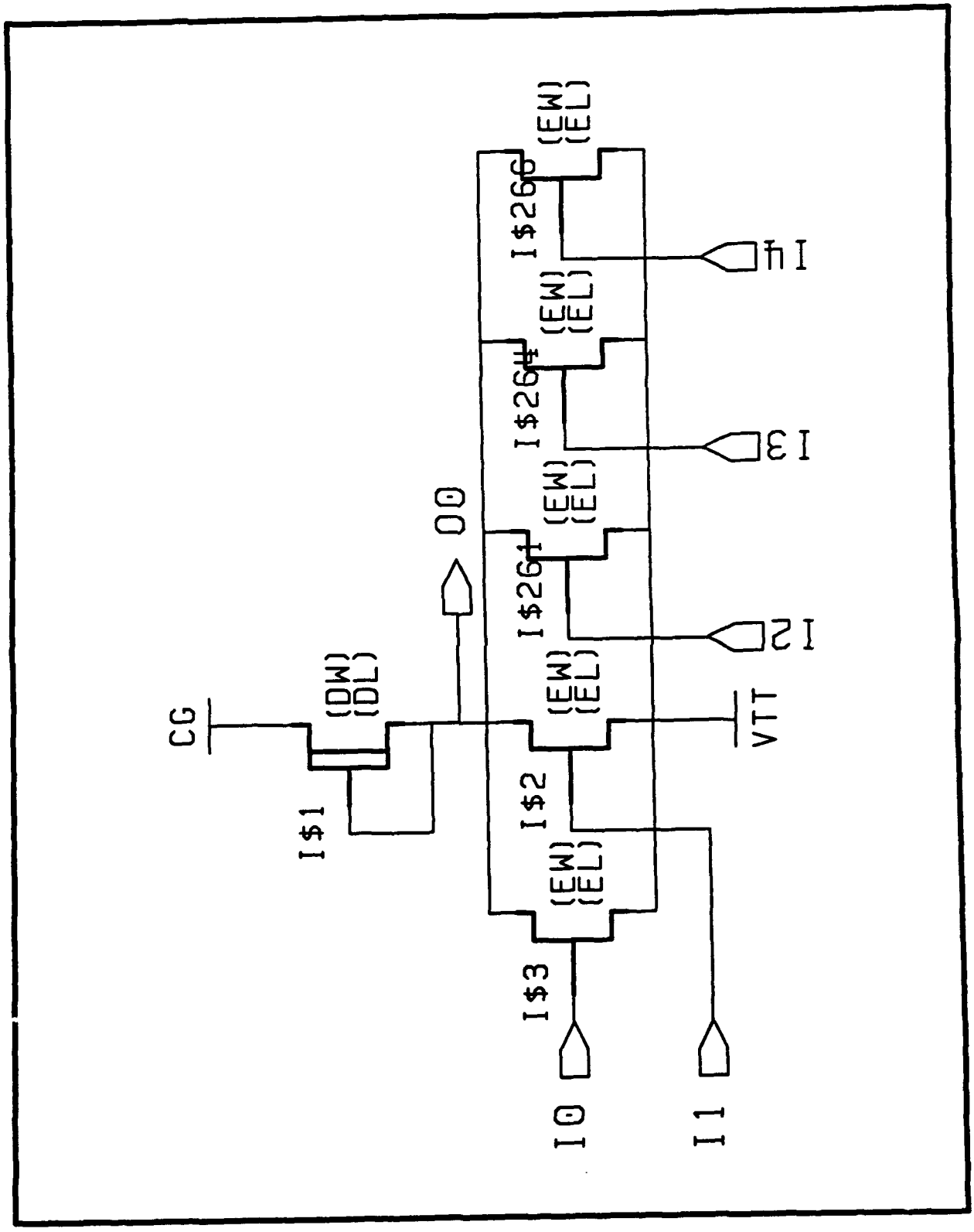

SSS
0 0 1 0 00
out
8.3
00
I0
I#
I1
NOR
I2
In
In
In
(DW) (DL)
(EW) (EL)
NOR
0.17 I0
0.17 I1
0.17 I2

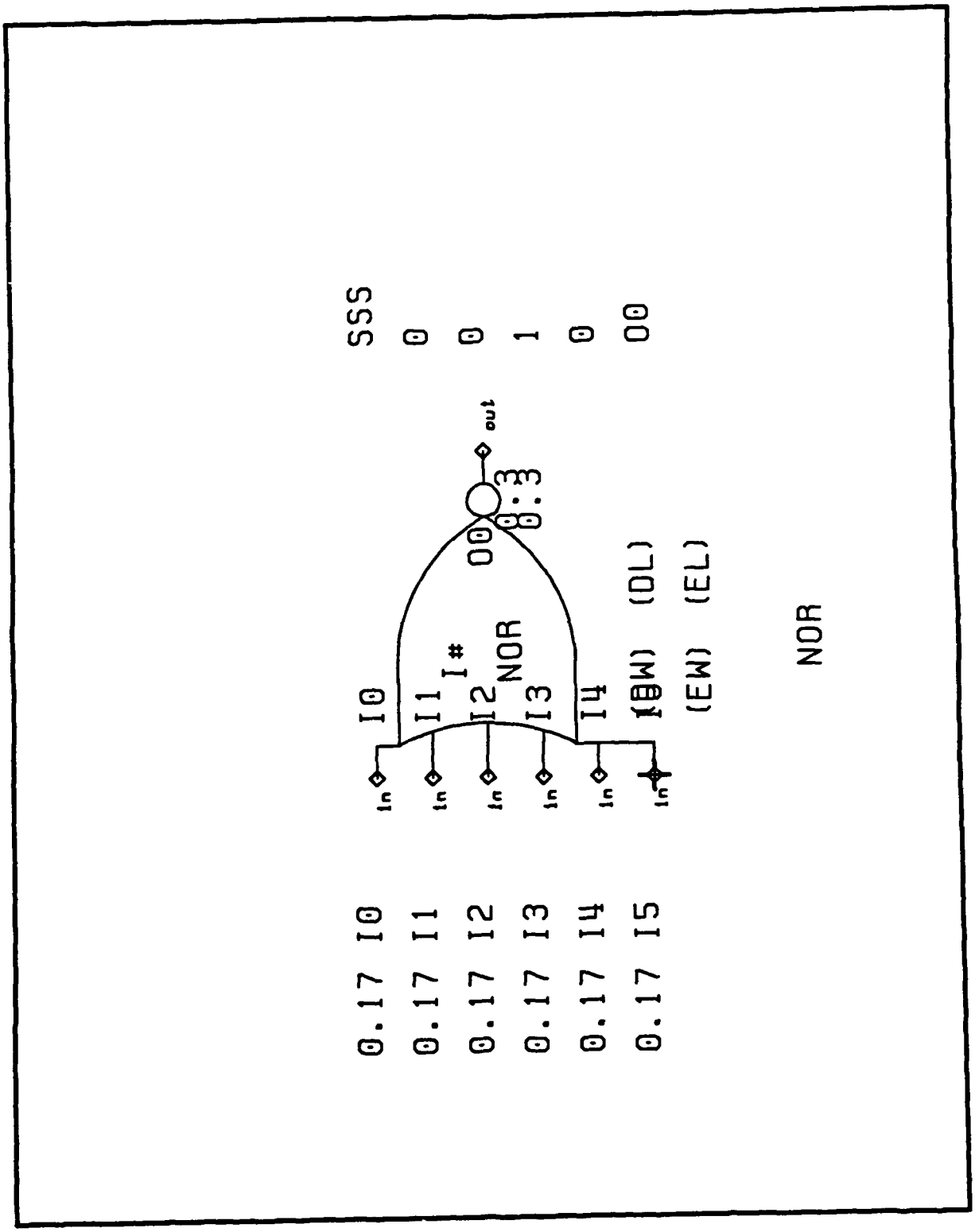

O0
(EW)
(EL)
I$26
I2
(OW)
(OL)
CG
(EW)
(EL)
VTT
I$1
I$2
(EW)
(EL)
I$3
I0
I1

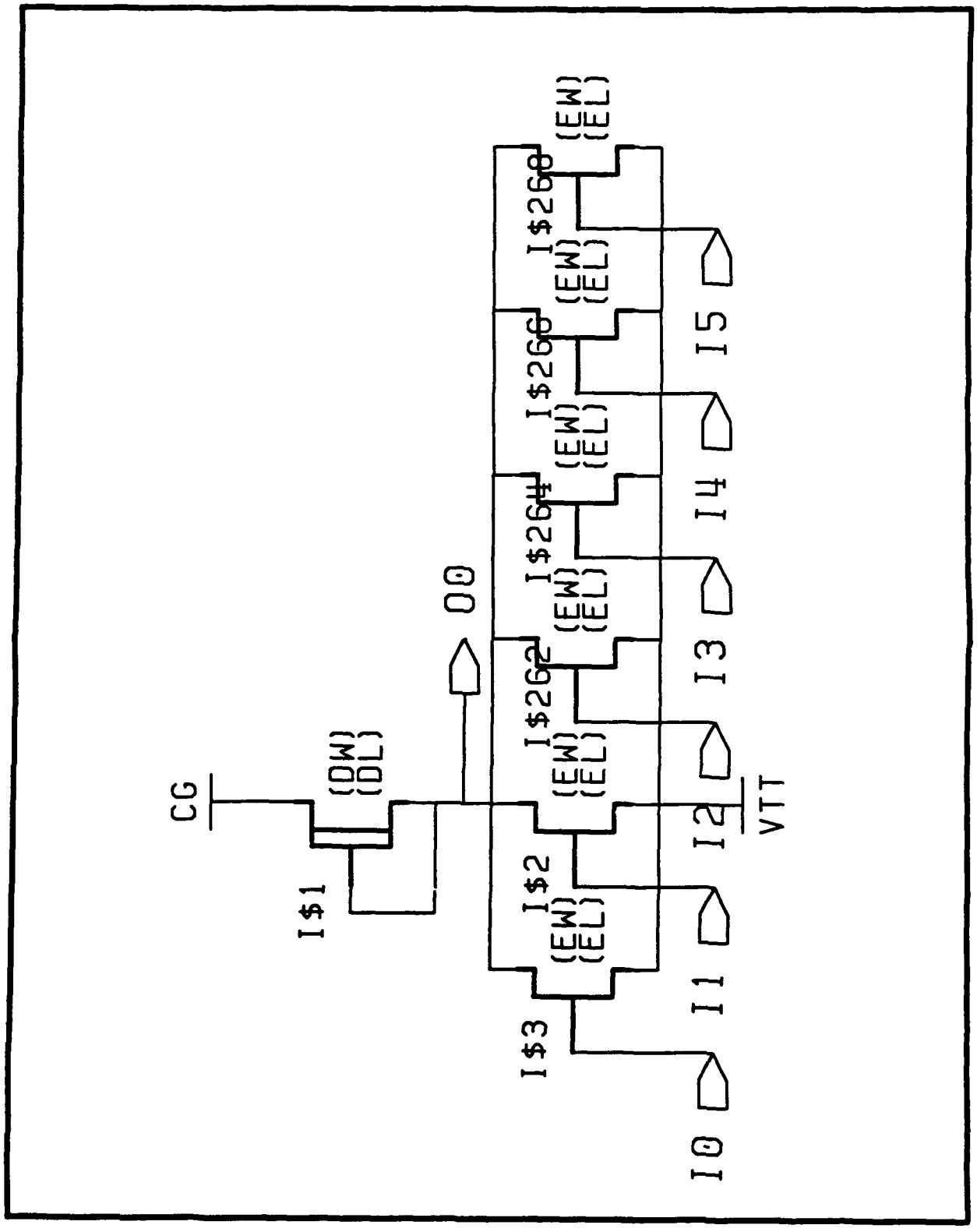

SSS
0 0 1 0 00
out
0.3
0.3
00
I#
NOR
I0
I1
I2
I3
(DW) (DL)
(EW) (EL)
NOR
In
In
In
In
0.17 I0
0.17 I1
0.17 I2
0.17 I3

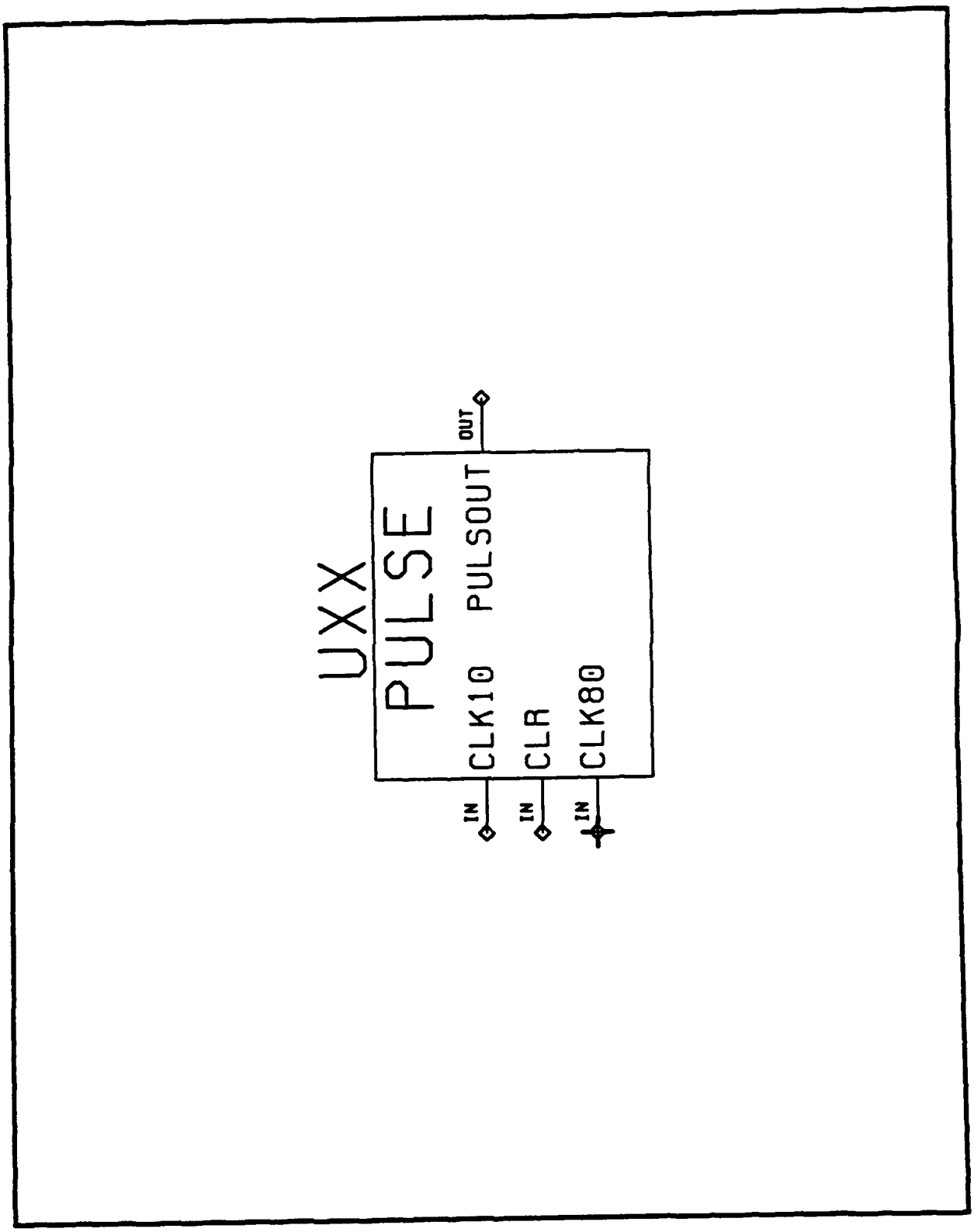

I$262
(EW)
(EL)
I3
O0
I$261
(EW)
(EL)
I2
CG
(DW)
(DL)
(EW)
(EL)
VTT
I$1
I$2
(EW)
(EL)
I$3
I0
I1

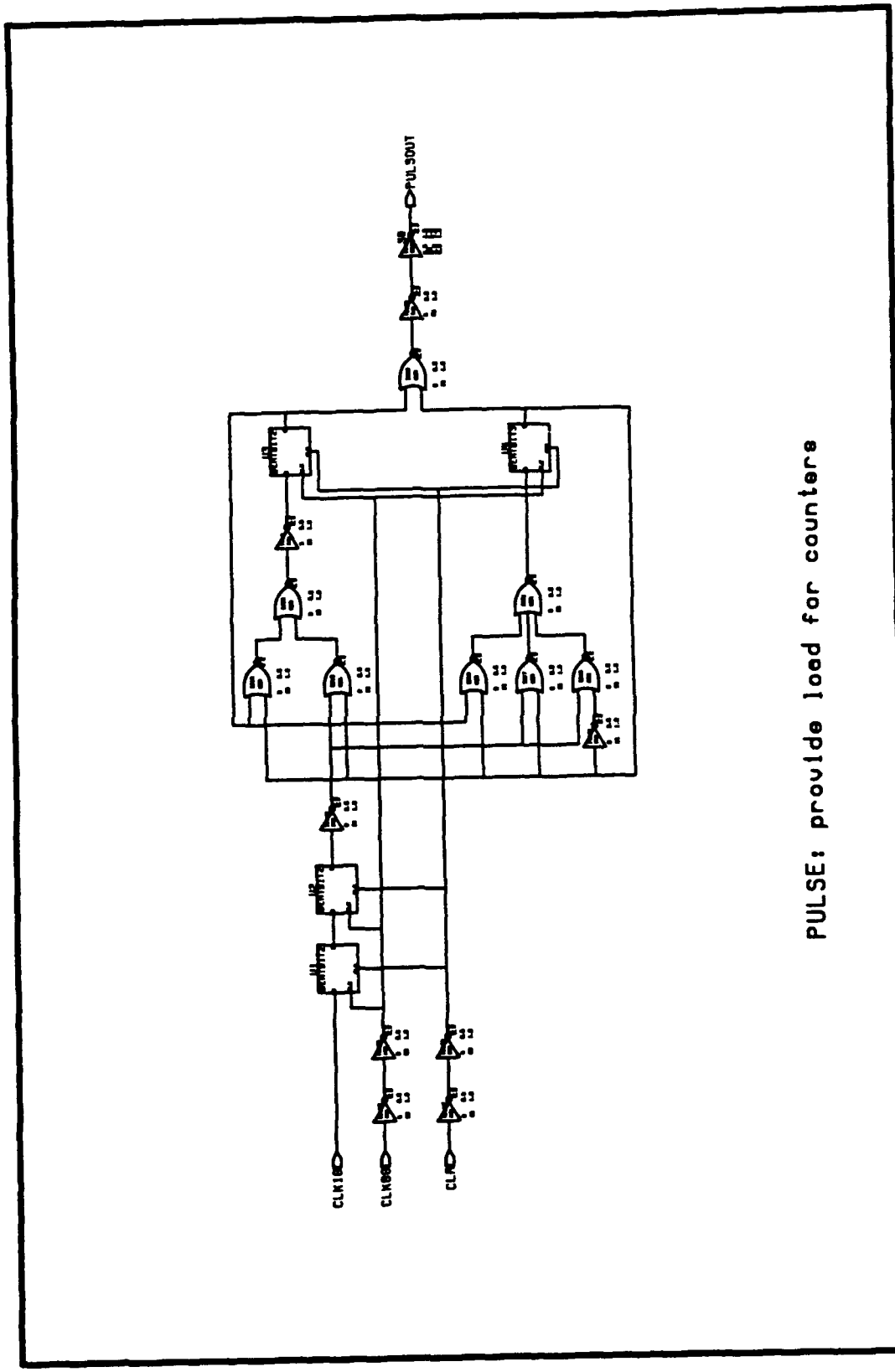

SSS
0 0 1 0 00
out
8:3
00
I#
NOR
I0
I1
I2
I3
I4
in
(DW) (DL)
(EW) (EL)
NOR
0.17 I0
0.17 I1
0.17 I2
0.17 I3
0.17 I4

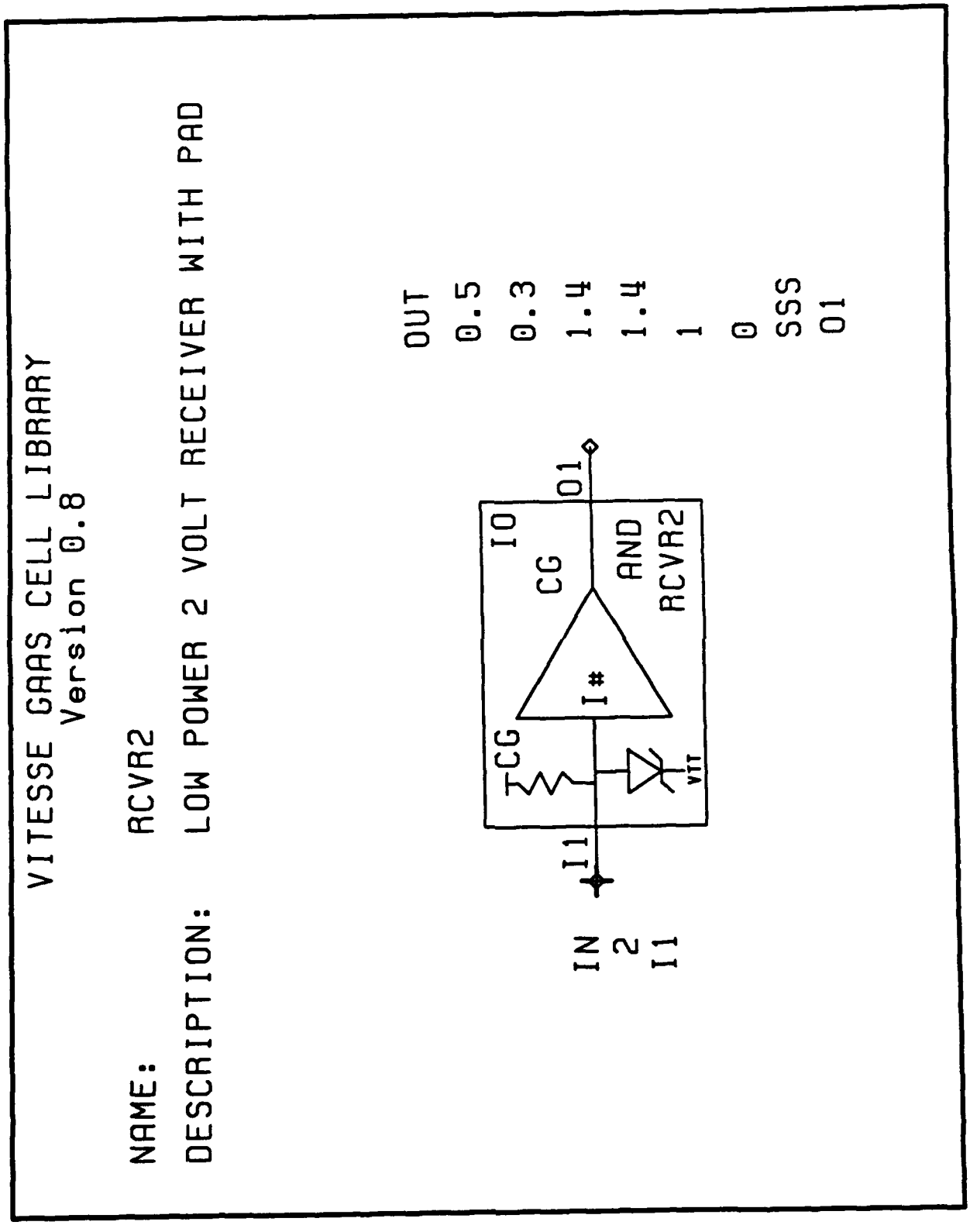

(EW)
(EL)
I$266
I4
(EW)
(EL)
I$264
I3
(EW)
(EL)
I$261
I2
(EW)
(EL)
I$2
(EW)
(EL)
I$3
I0
I1
O0
(DW)
(DL)
I$1
CG
VTT

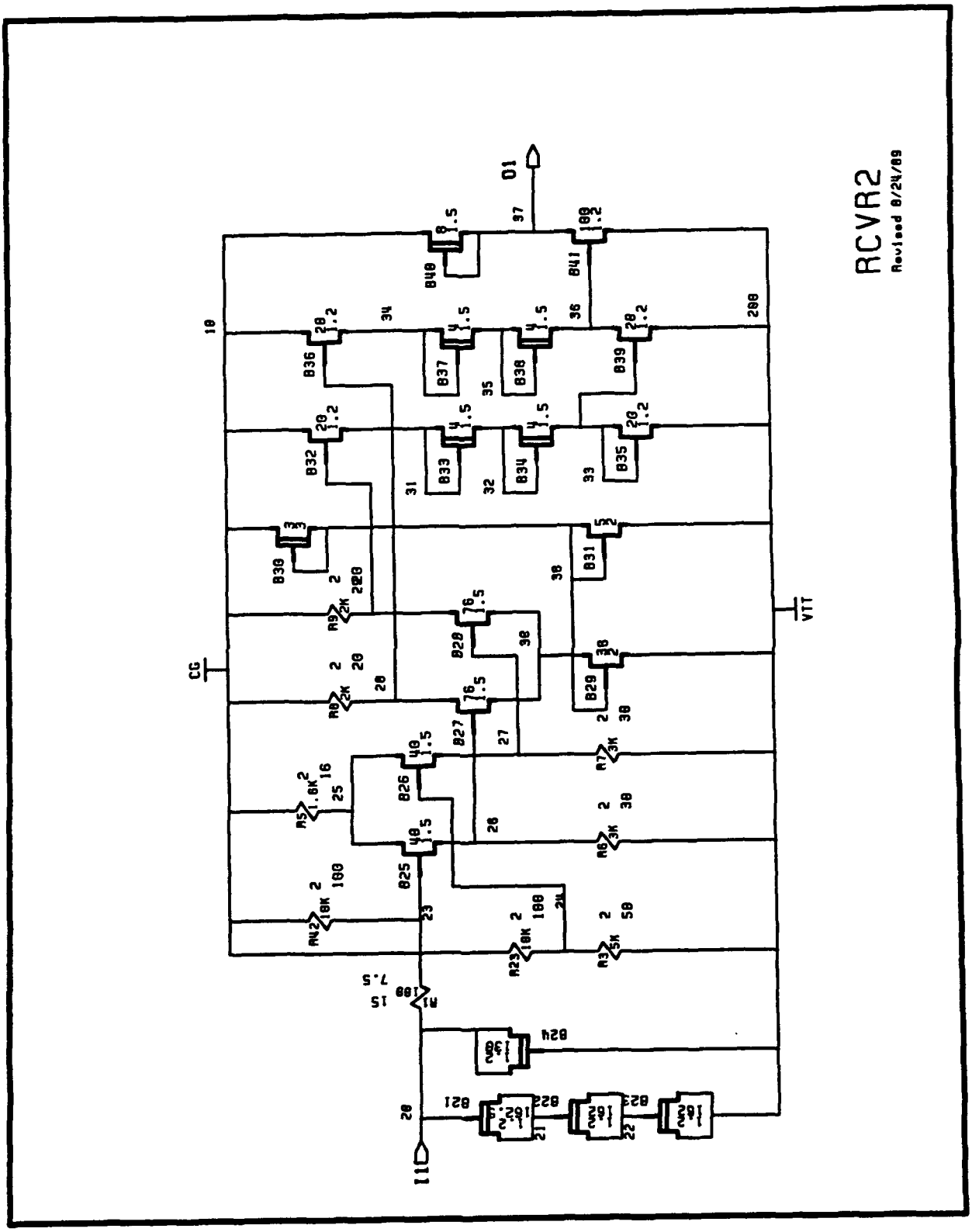

SSS
0 0 1 0 00
out
00 8:3
I0
I1
I#
I2 NOR
I3
I4
(BW) (DL)
(EW) (EL)
NOR
0.17 I0
0.17 I1
0.17 I2
0.17 I3
0.17 I4
0.17 I5

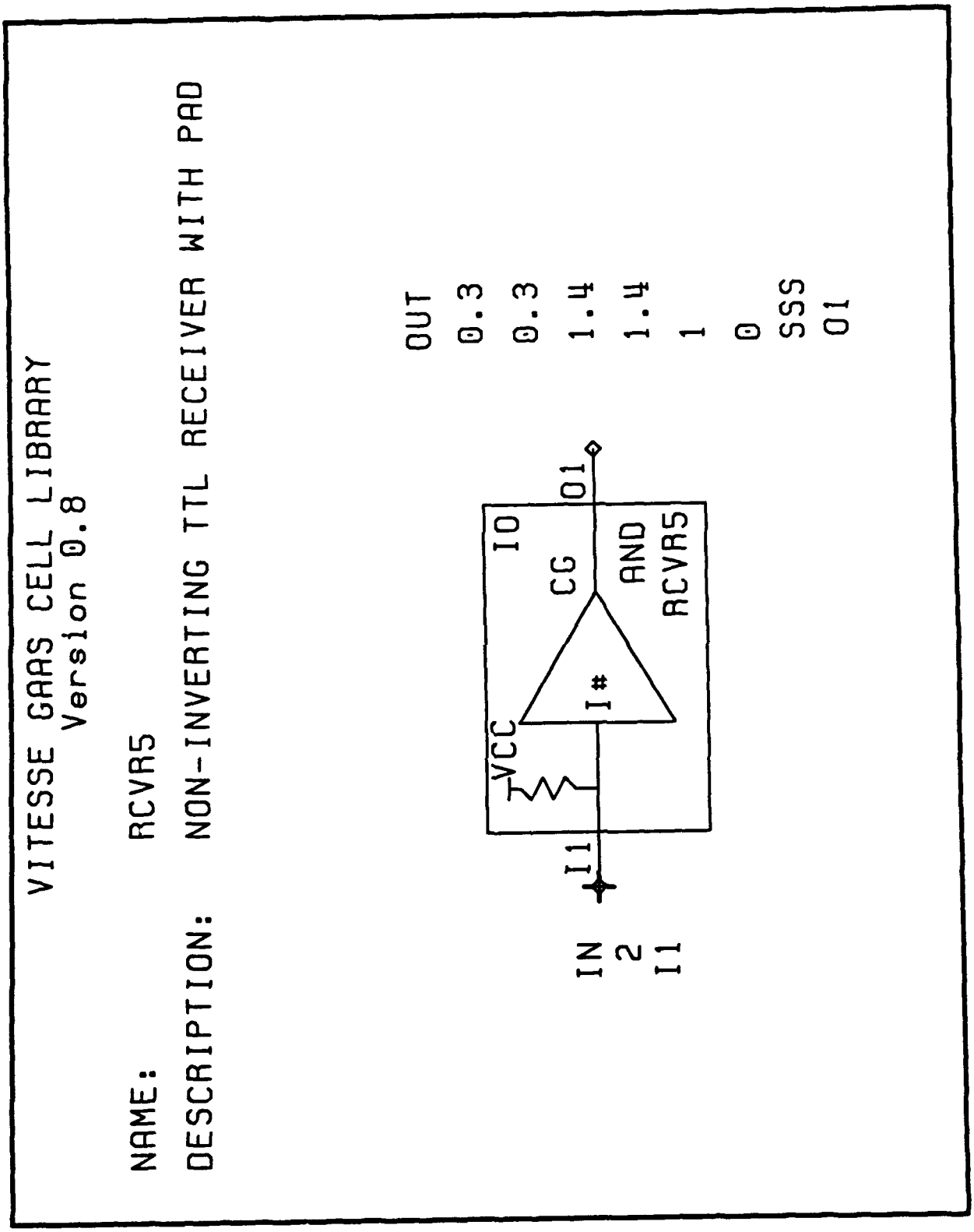

CG
(OW)
(OL)
I$1
O0
I$2
(EW)
(EL)
I$3
I$262
I$264
I$266
I$268
I0
I1
I2
VTT
I3
I4
I5

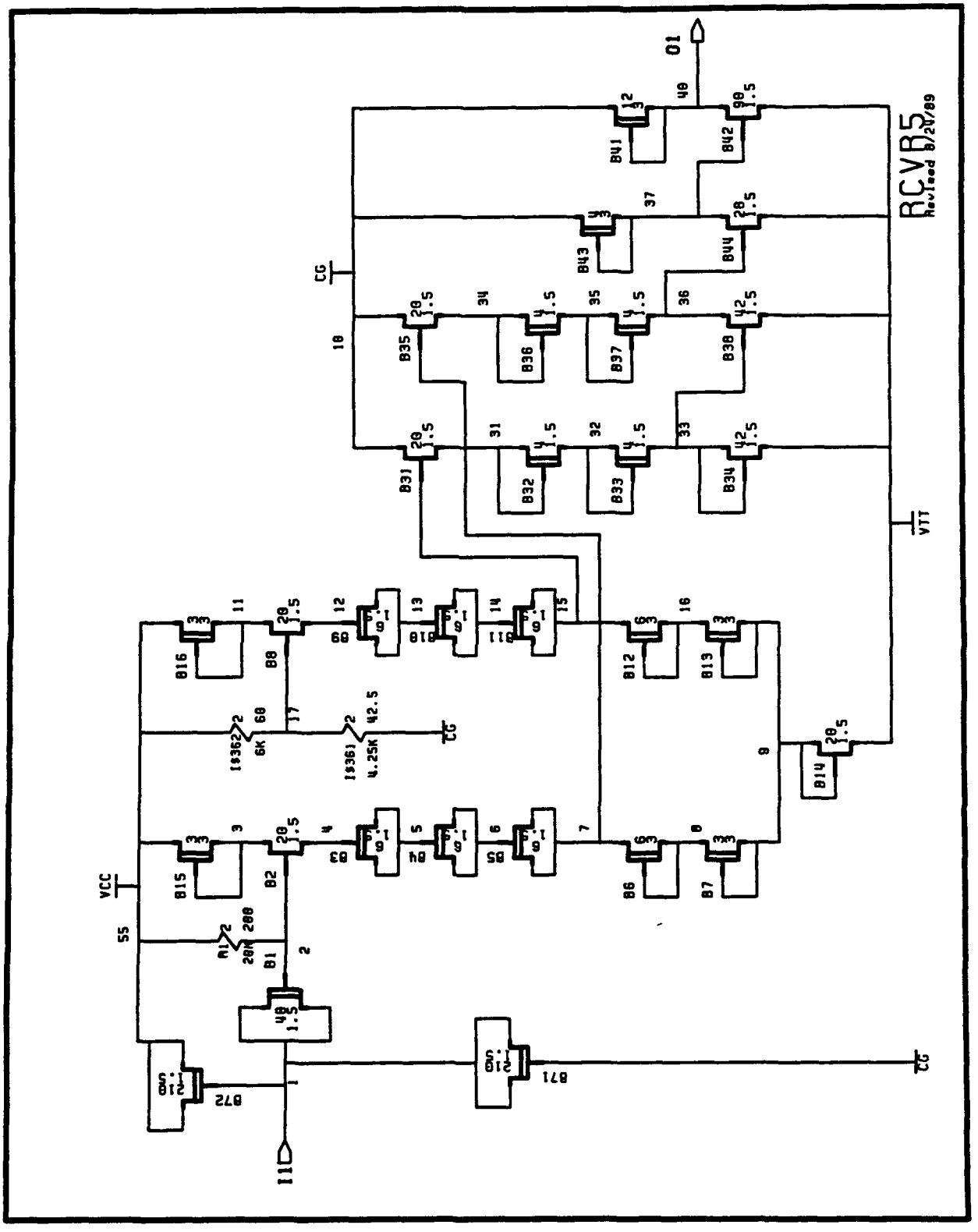

UXX
PULSE
CLK10
CLR
CLK80
PULSOUT
OUT
IN
IN
IN

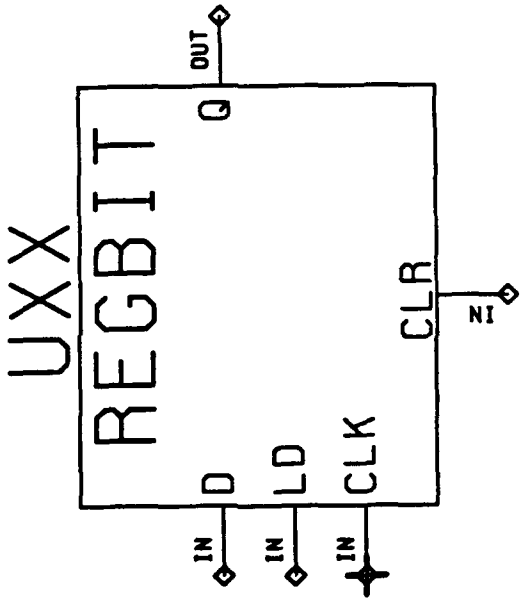

PULSOUT
CLK1MC
CLK8MC
CLKC
PULSE: provide load for counters

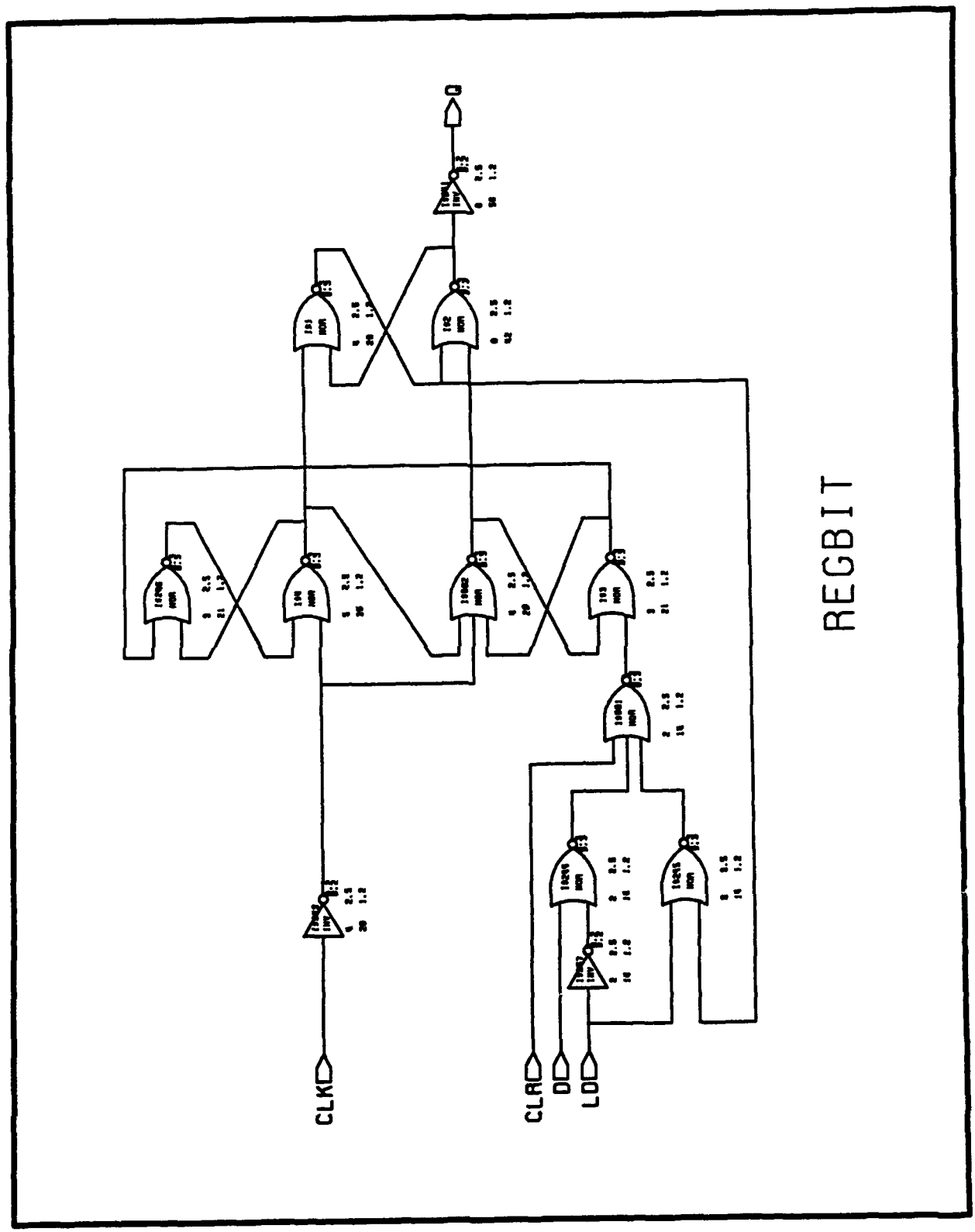

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: RCVR2
DESCRIPTION: LOW POWER 2 VOLT RECEIVER WITH PAD
OUT
0.5
0.3
1.4
1.4
1
0
SSS
01
IO
CG
AND
RCVR2
O1
I#
ICG
VTT
I1
IN
2
I1

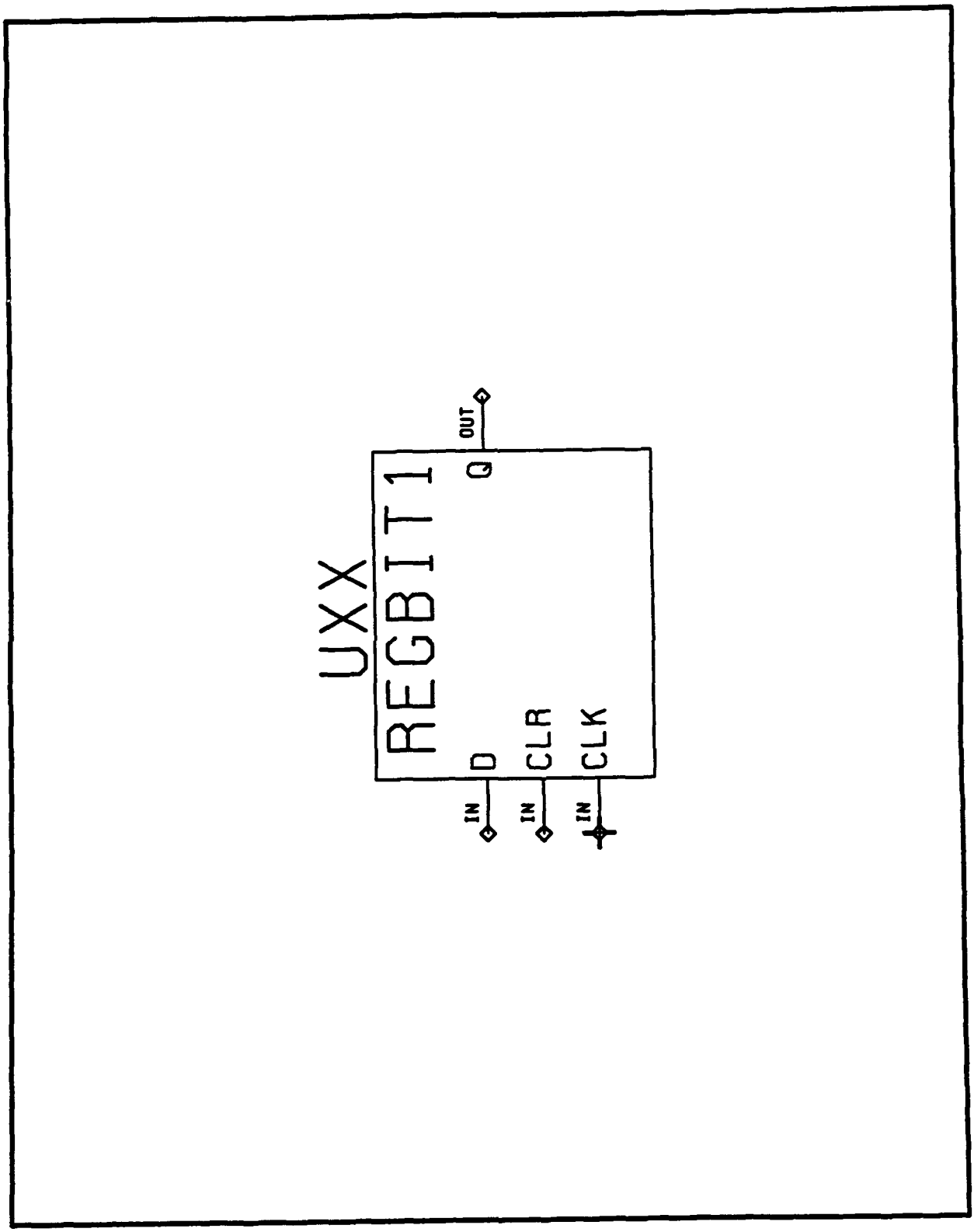

RCVR2
Revised 8/24/89
D1
D11
CG
VTT

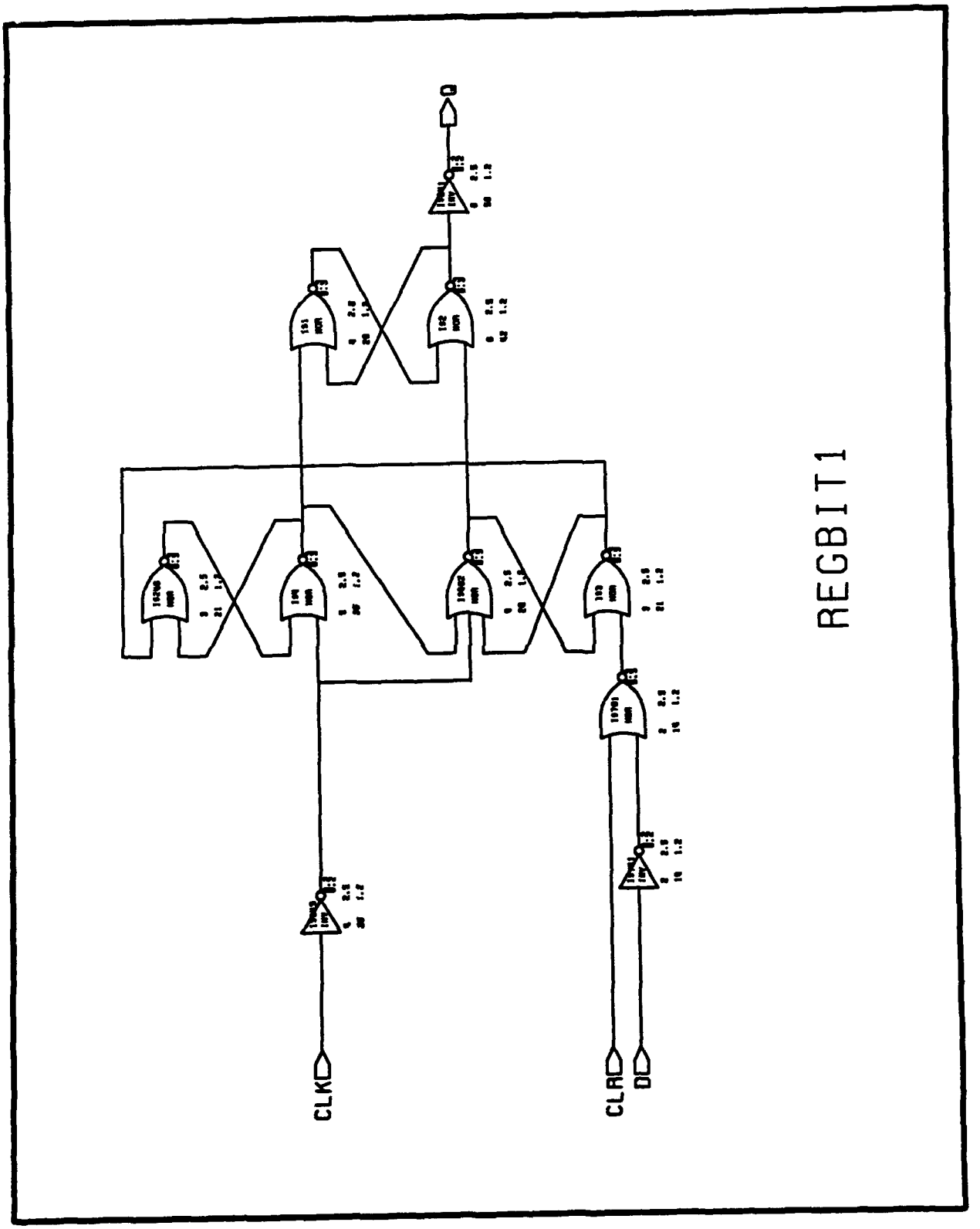

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: RCVR5
DESCRIPTION: NON-INVERTING TTL RECEIVER WITH PAD
OUT
0.3
0.3
1.4
1.4
1
0
SSS
01
IN
2
I1
I1
VCC
I#
IO
CG
O1
AND
RCVR5

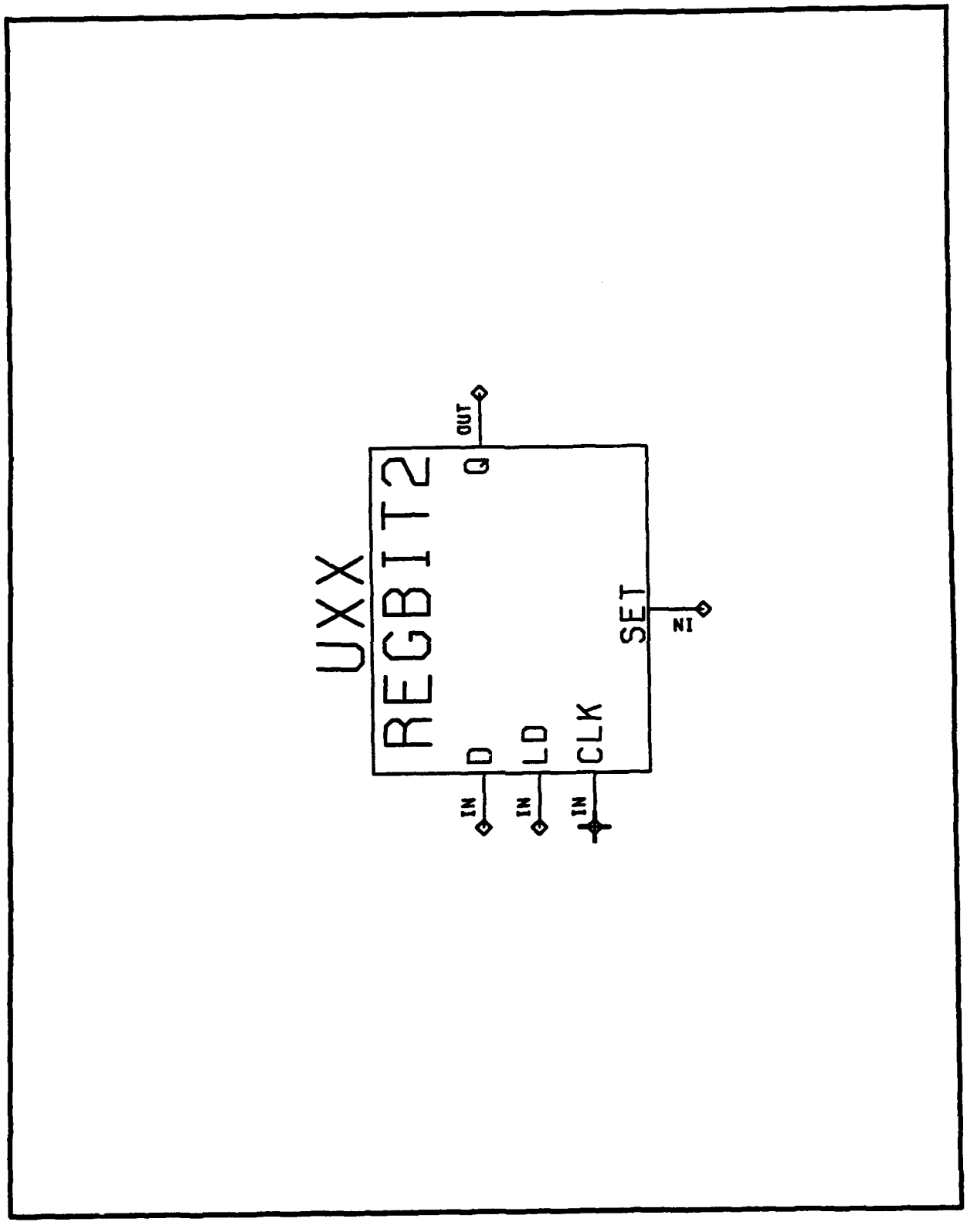

RCVR5
Revised 8/20/89
O1
CG
VTT
VCC
I1
I$362
6K
I$361
4.25K
42.5
200
20K

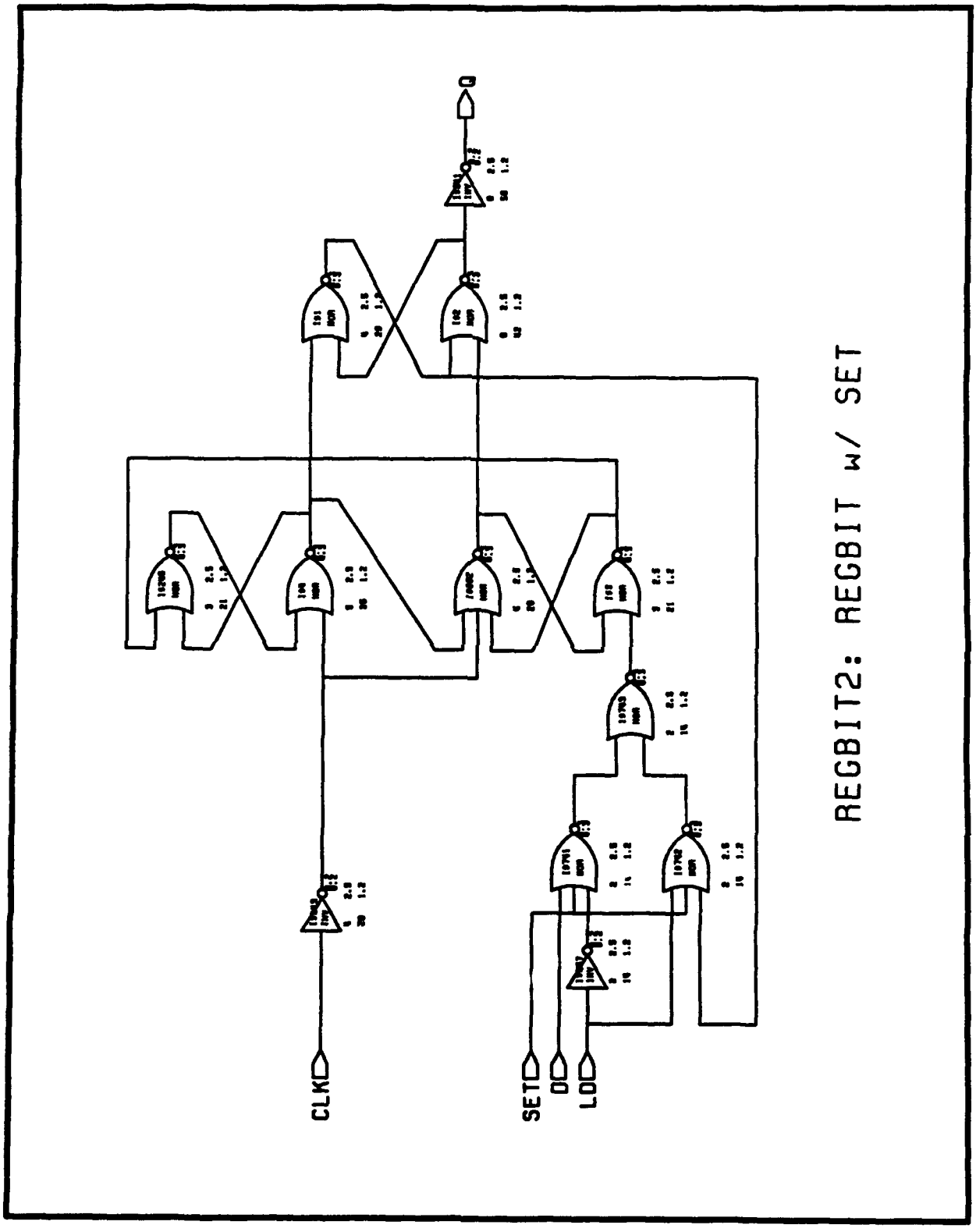

UXX
REGBIT
OUT
Q
CLR
NI
D
LD
CLK
IN
IN
IN

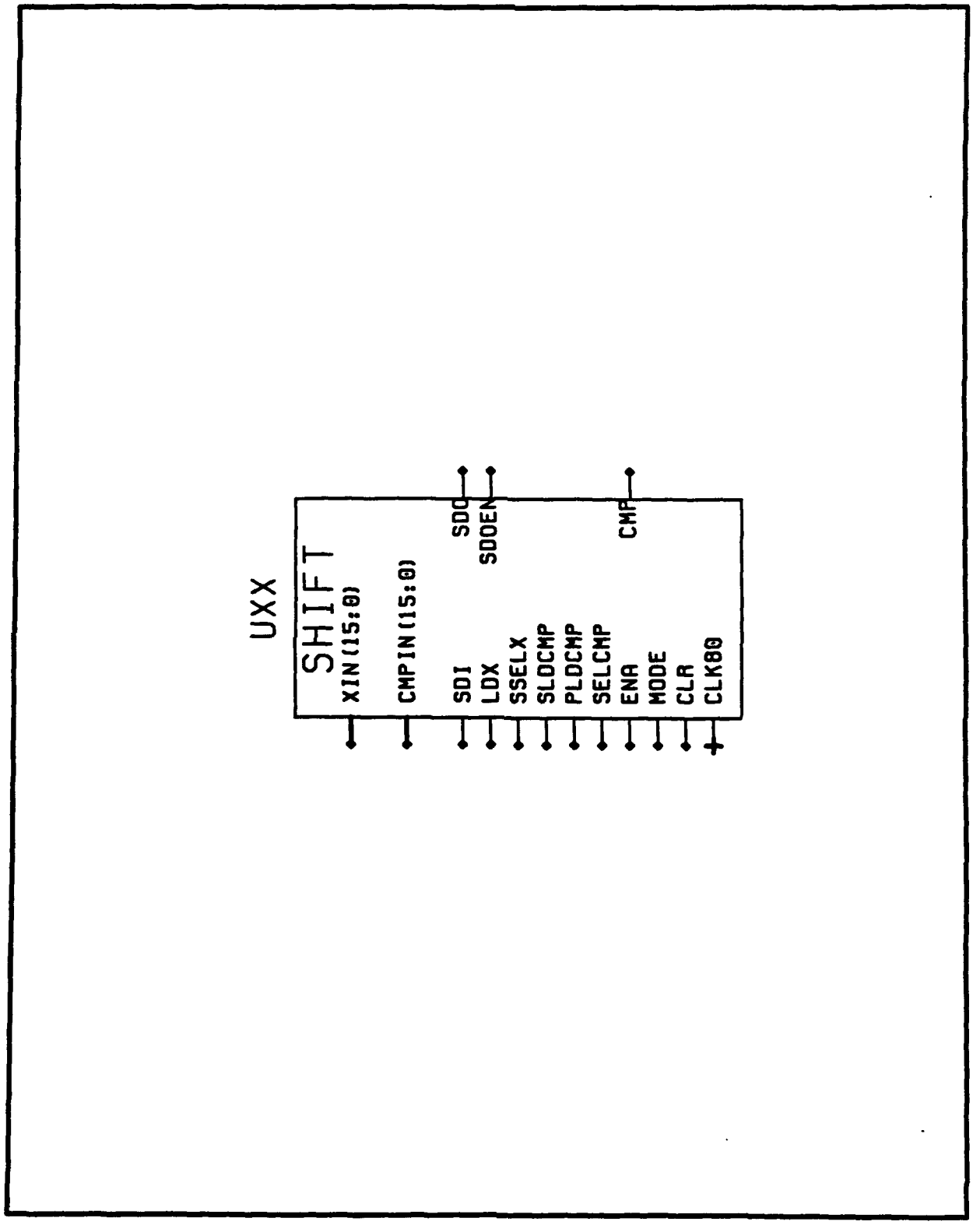

Q
REGBIT
CLK
CLR
D
LD

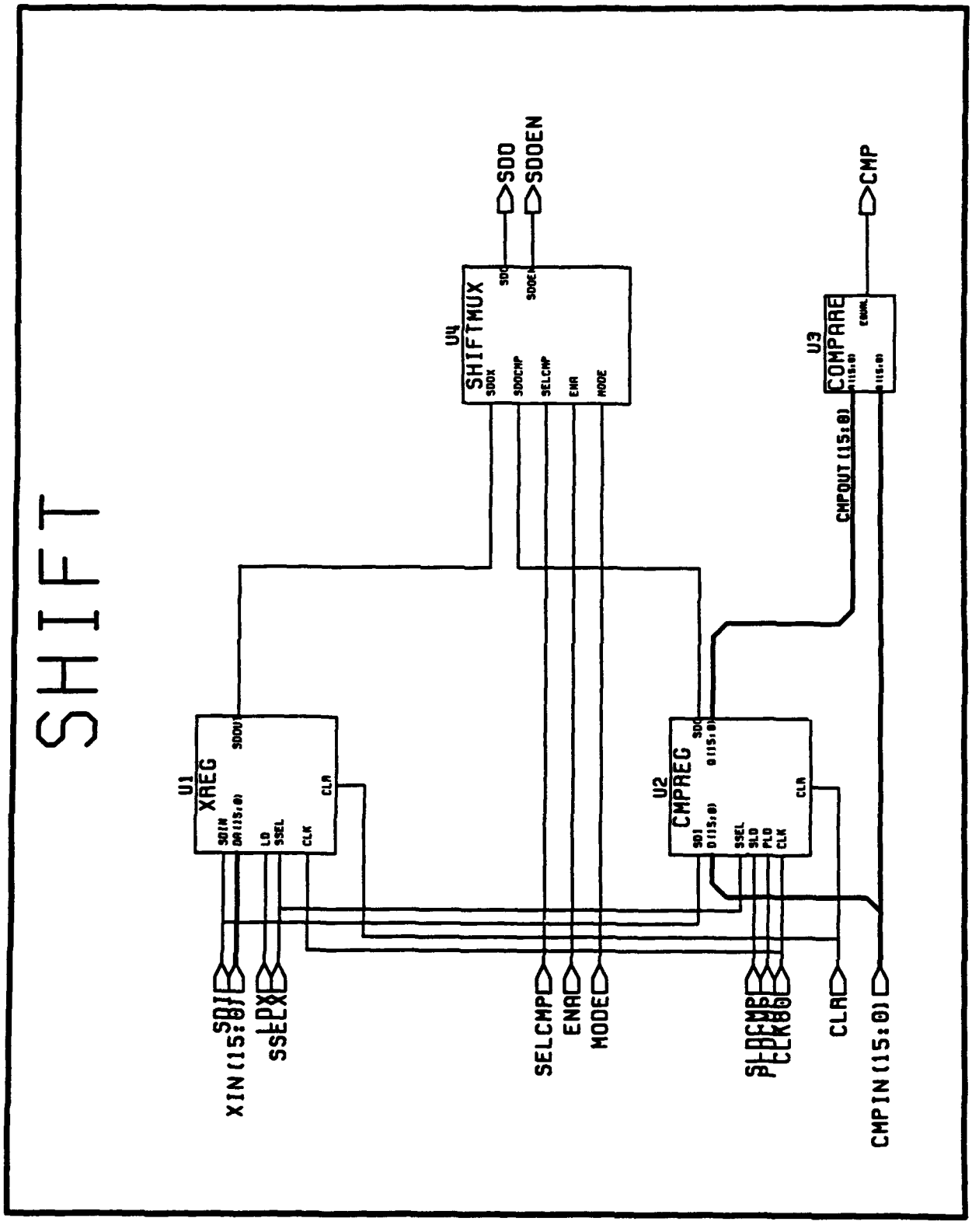

UXX
REGBIT1
OUT
Q
D
CLR
CLK
IN
IN
IN

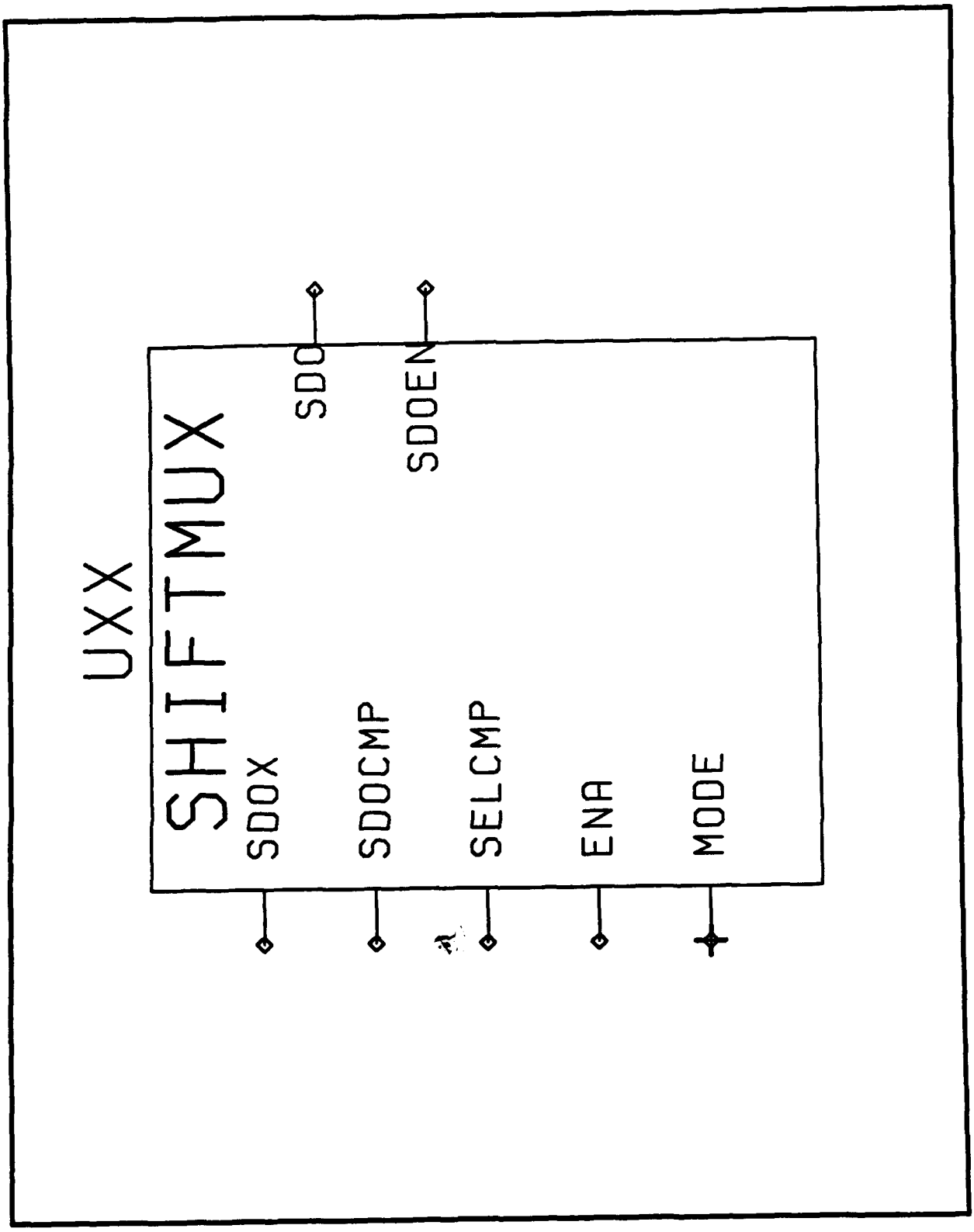

Q
CLK
CLR
D
REGBIT1

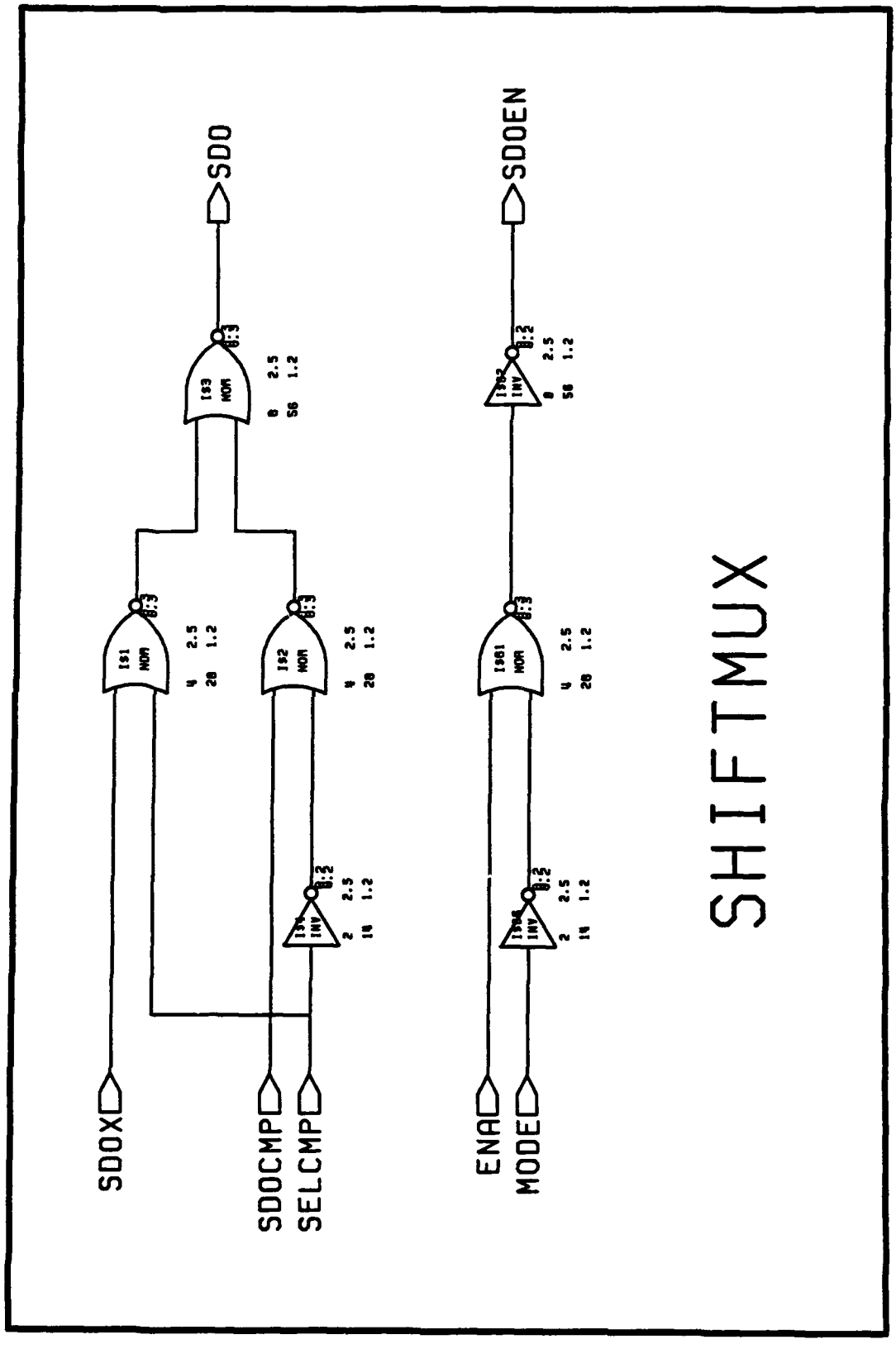

UXX
REGBIT2
OUT
Q
SET
NI
D
LD
CLK
IN
IN
IN

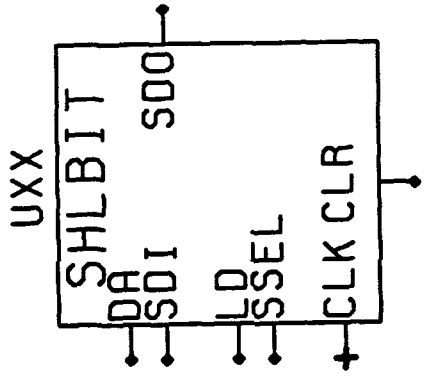

REGBIT2: REGBIT w/ SET
Q
CLK
SET
D
LD

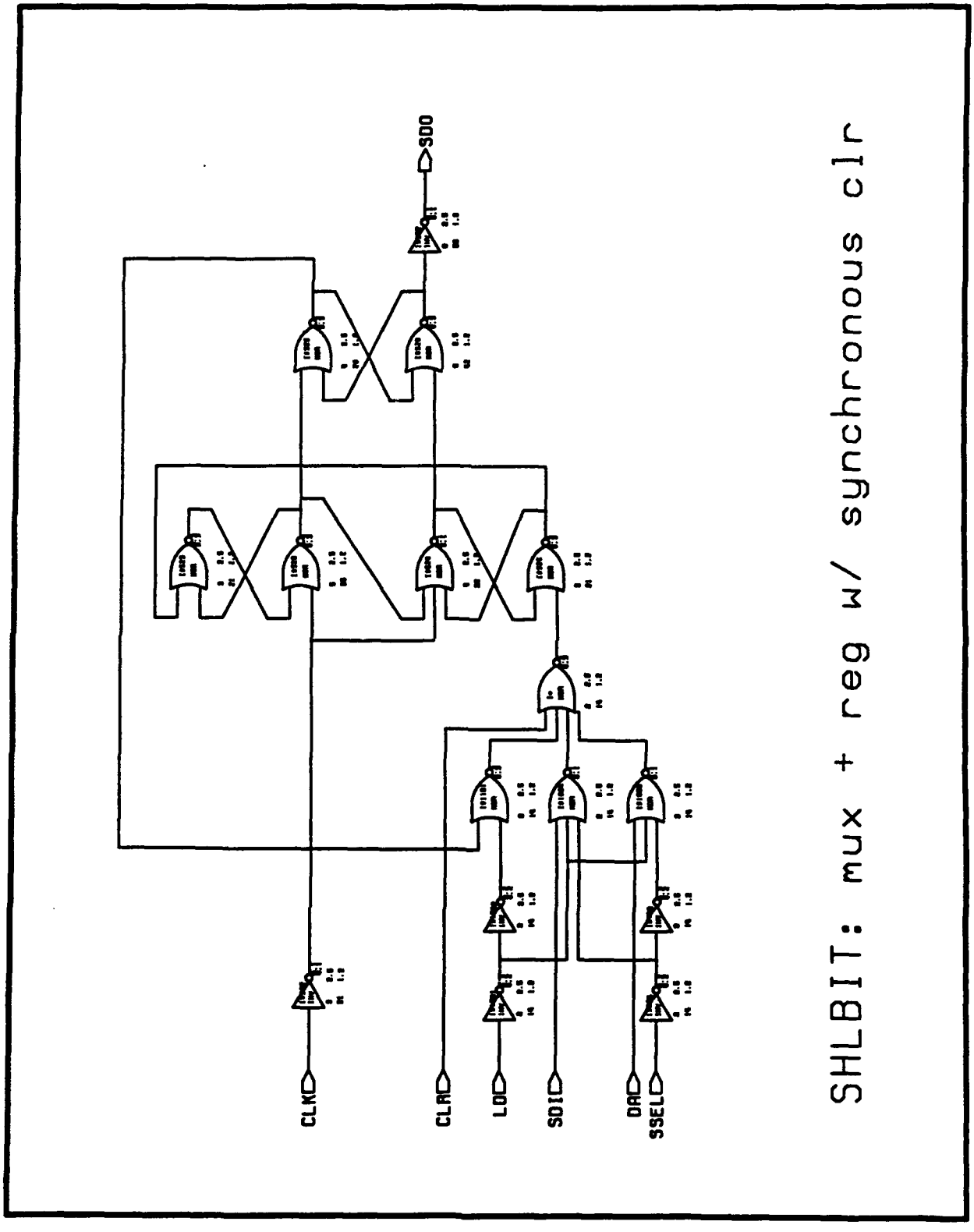

UXX
SHIFT
XIN(15:0)
CMPIN(15:0)
SDO
SDOEN
CMP
SDI
LDX
SSELX
SLDCMP
PLDCMP
SELCMP
ENA
MODE
CLR
CLK80

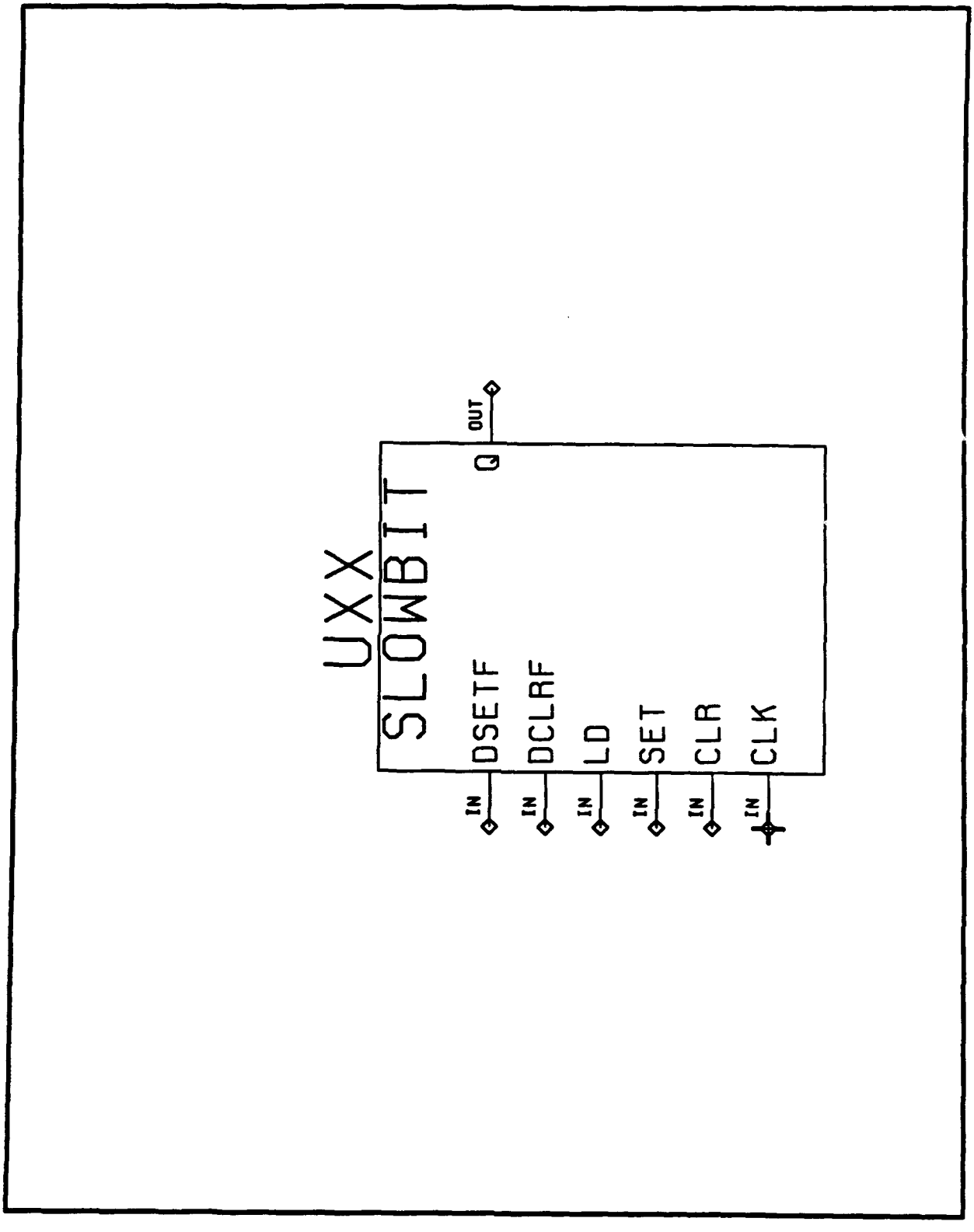

SHIFT
U1
XREG
SDOUT
SDIN
DA[15:0]
LD
SSEL
CLK
CLR
U2
CMPREG
SDO
SDI
D[15:0]
SSEL
SLD
PLD
CLK
CLR
U3
COMPARE
CMPOUT
A[15:0]
B[15:0]
U4
SHIFTMUX
SDOX
SDOCMP
SELCMP
ENA
MODE
SDO
SDOEN
CMP
CMPOUT[15:0]
XIN[15:0]
SDI
SSEL
LDX
SELCMP
ENA
MODE
SLDCMP
PLDCMP
CLKCMP
CLR
CMPIN[15:0]

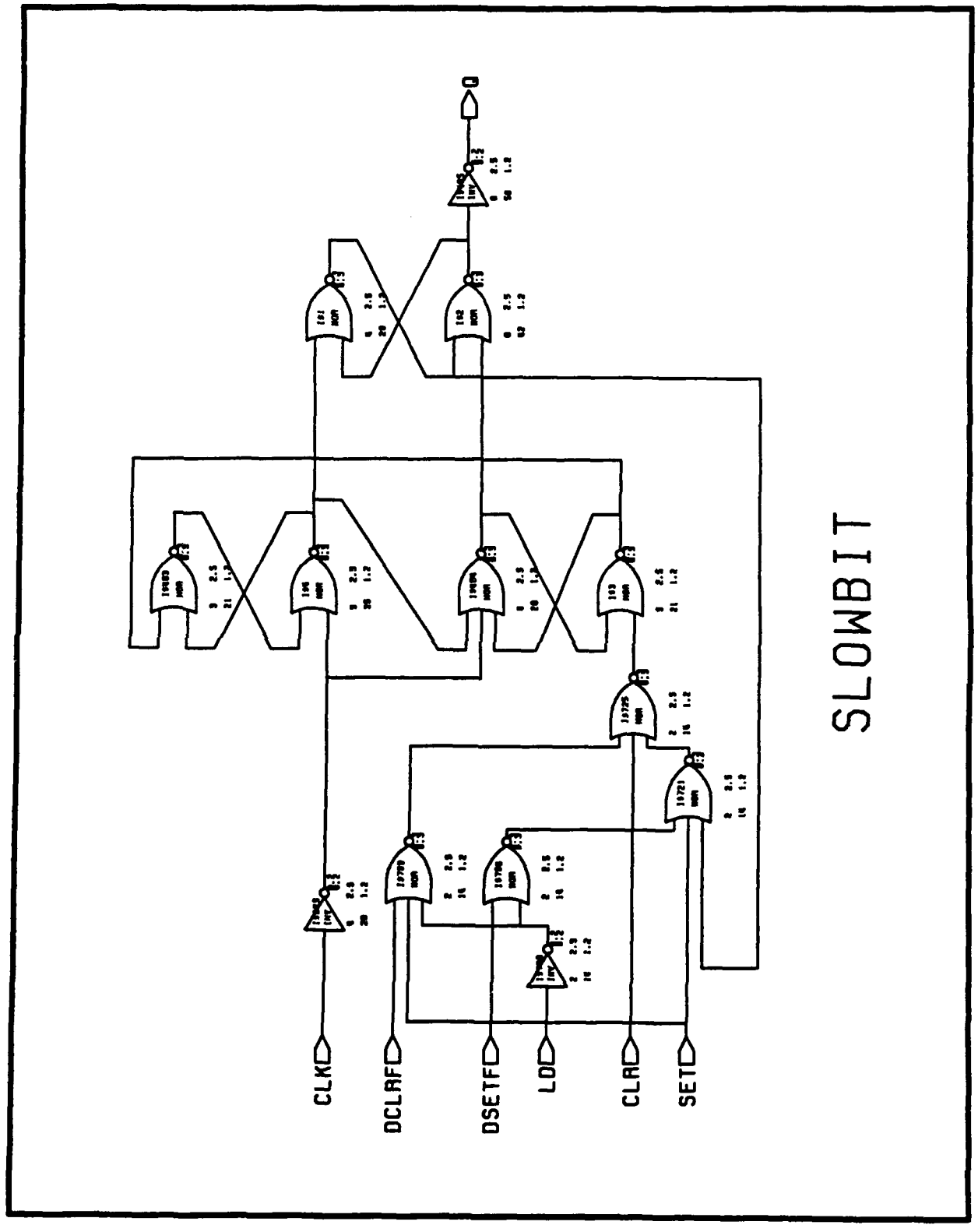

UXX
SHIFTMUX
SDO
SDOEN
SDOX
SDOCMP
SELCMP
ENA
MODE

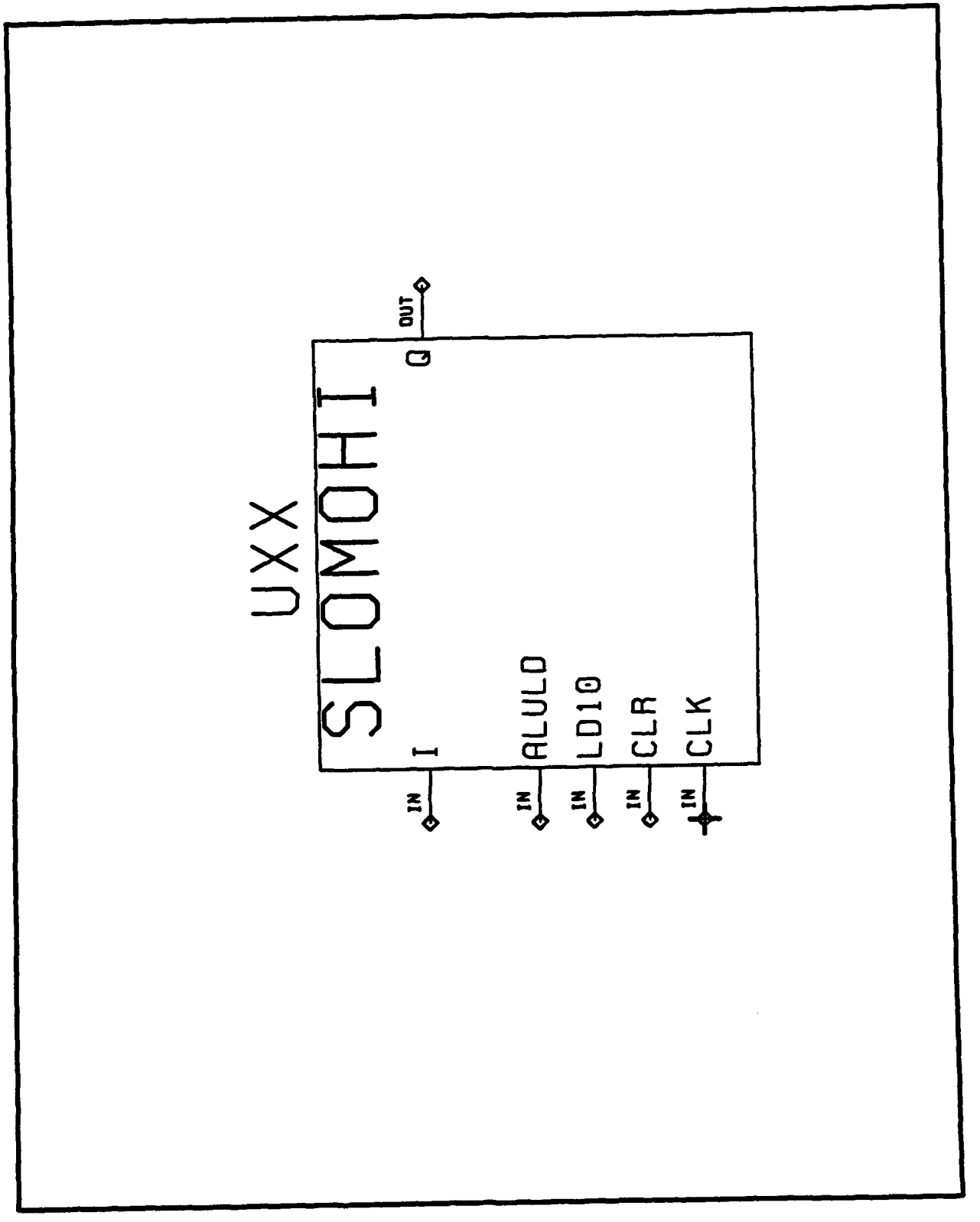

SDO
SDOEN
SHIFTMUX
SDOX
SDOCMP
SELCMP
ENA
MODE

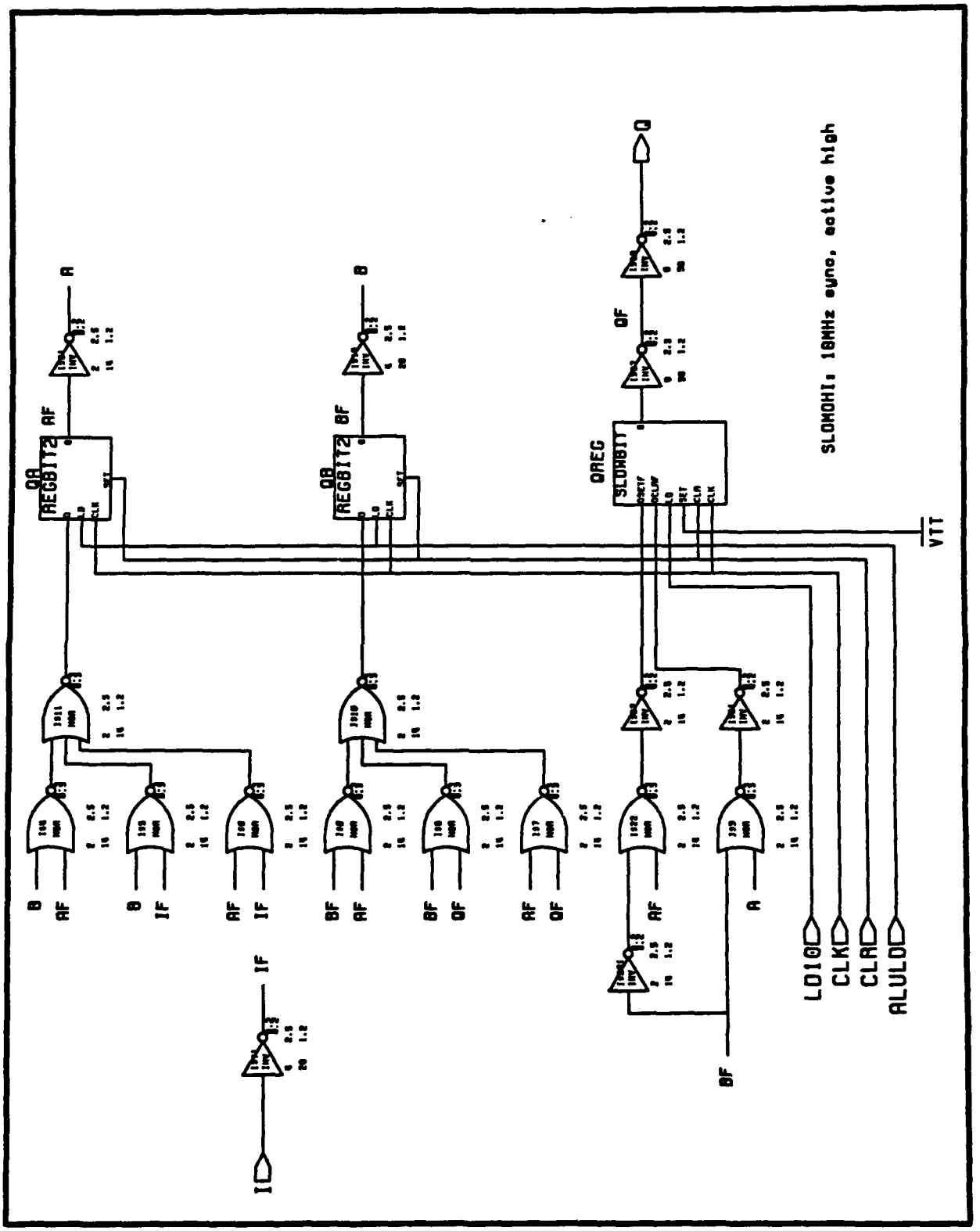

UXX
SHLBIT
SDO
DA
SDI
LD
SSEL
CLK
CLR

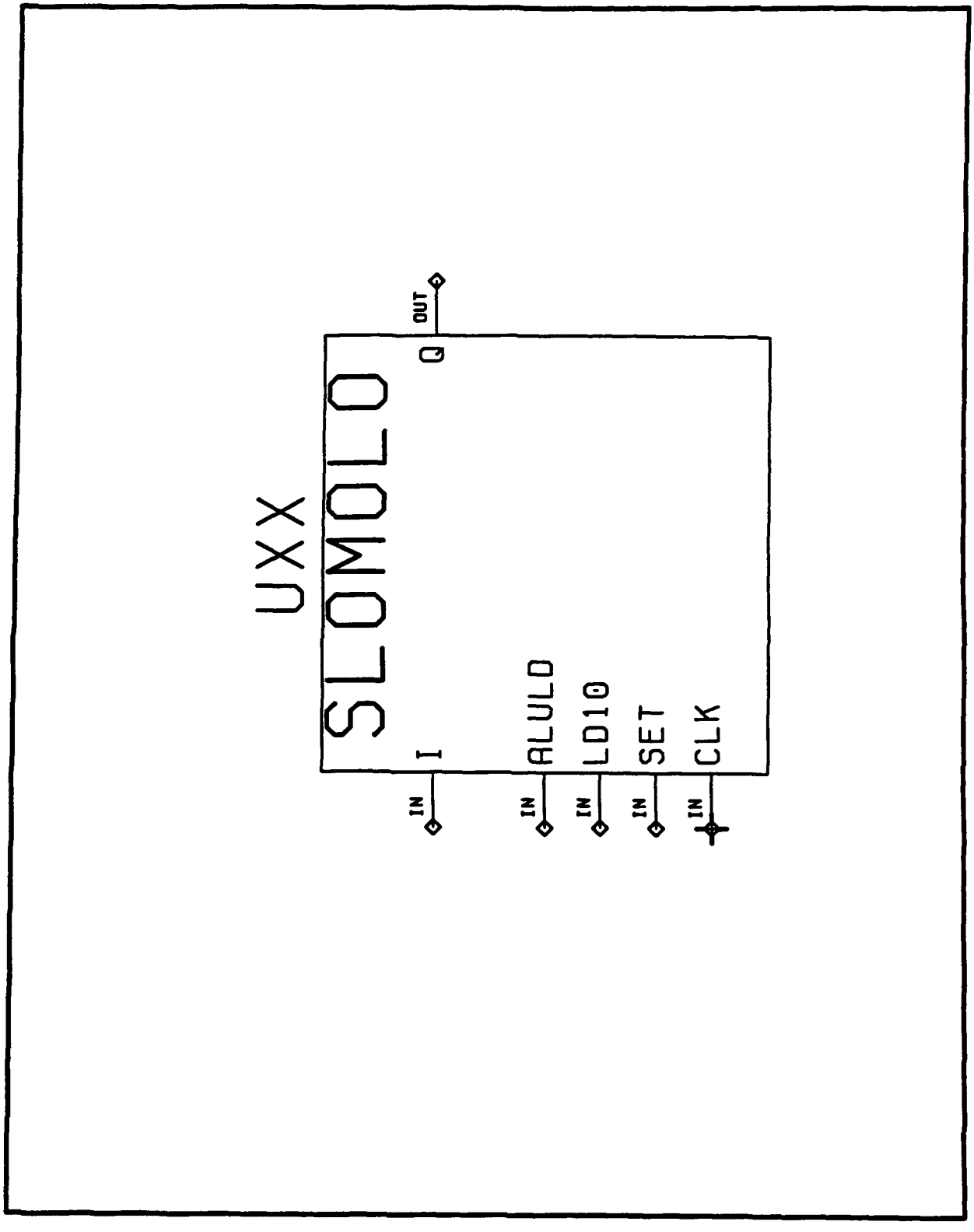

SHLBIT: mux + reg w/ synchronous clr
SDO
CLK
CLR
LOD
SDI
DAC
SSEL

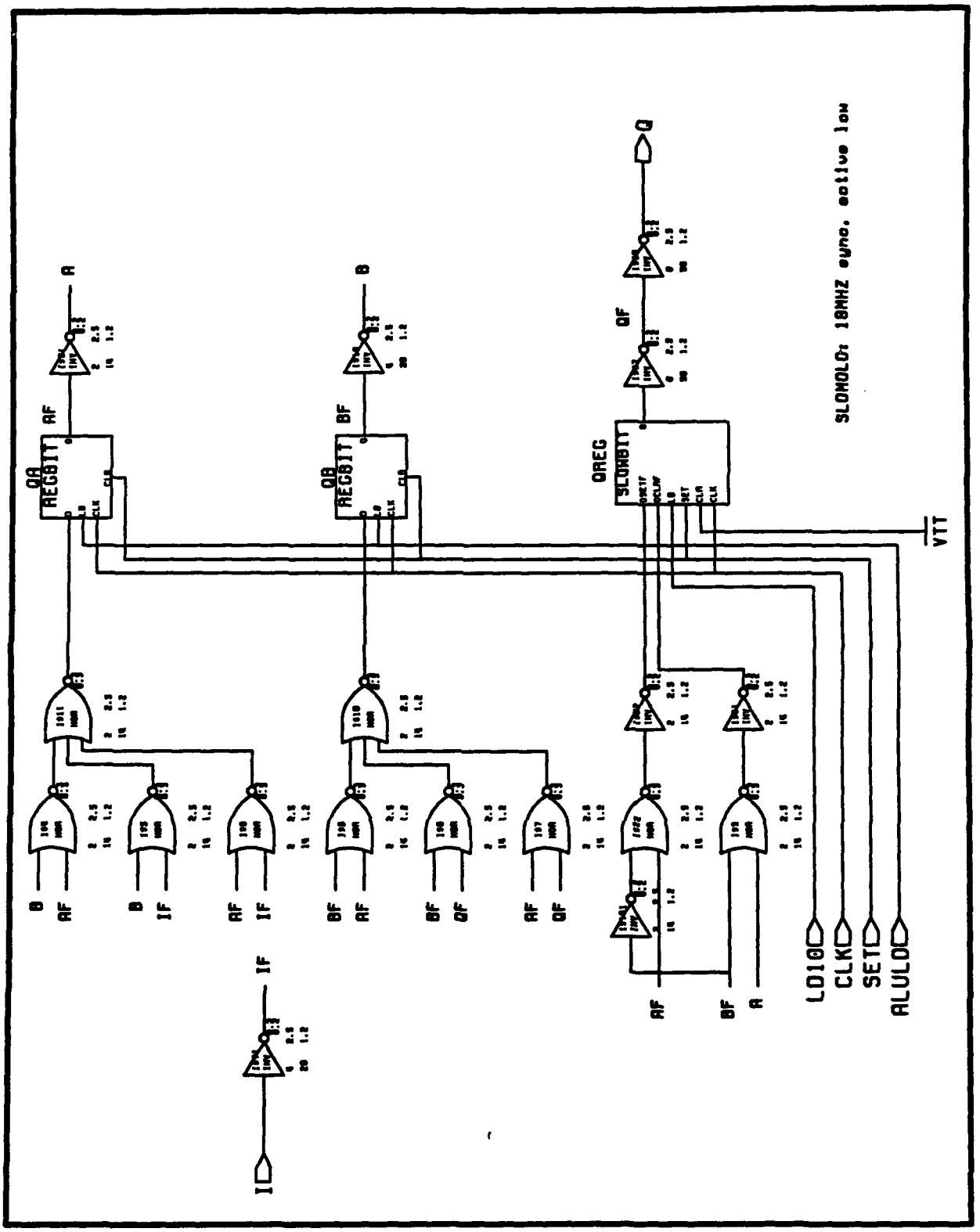

UXX
SLOWBIT
Q
OUT
DSETF
DCLRF
LD
SET
CLR
CLK
IN
IN
IN
IN
IN
IN

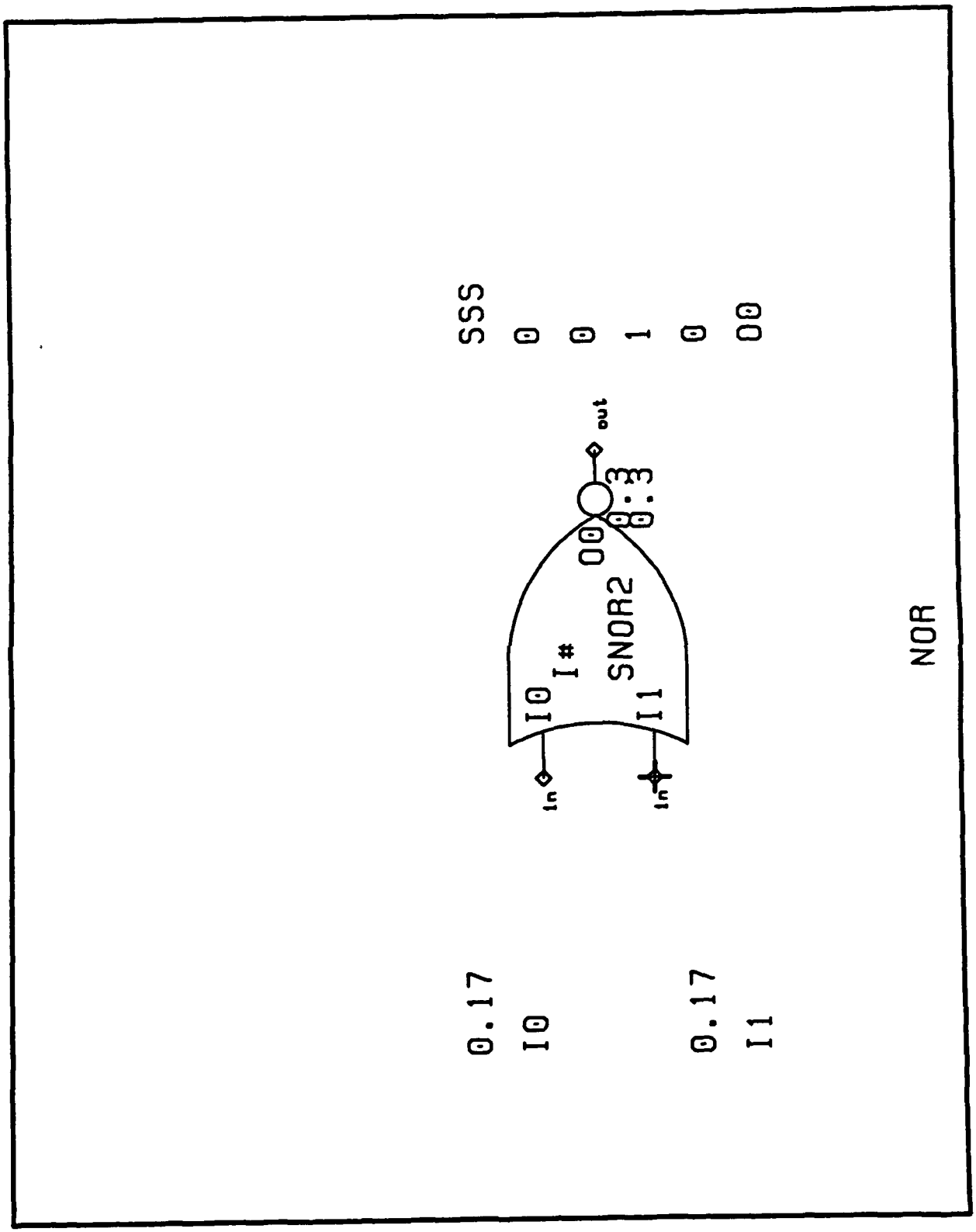

SLOWBIT
CLK
DCLRFF
DSETFF
LD
CLR
SET

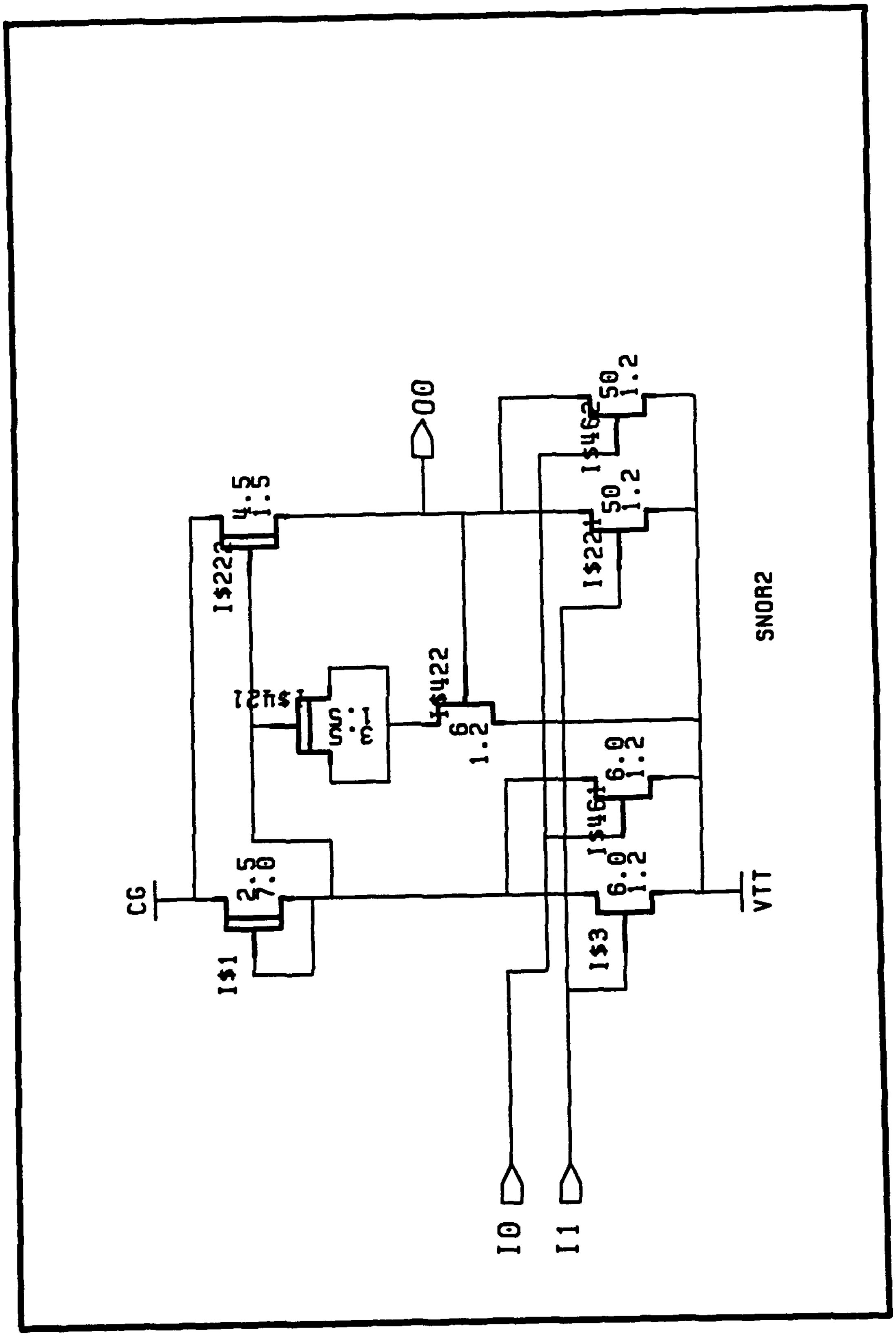

UXX
SLOMOHI
OUT
Q
I
ALULD
LD10
CLR
CLK
IN
IN
IN
IN
IN

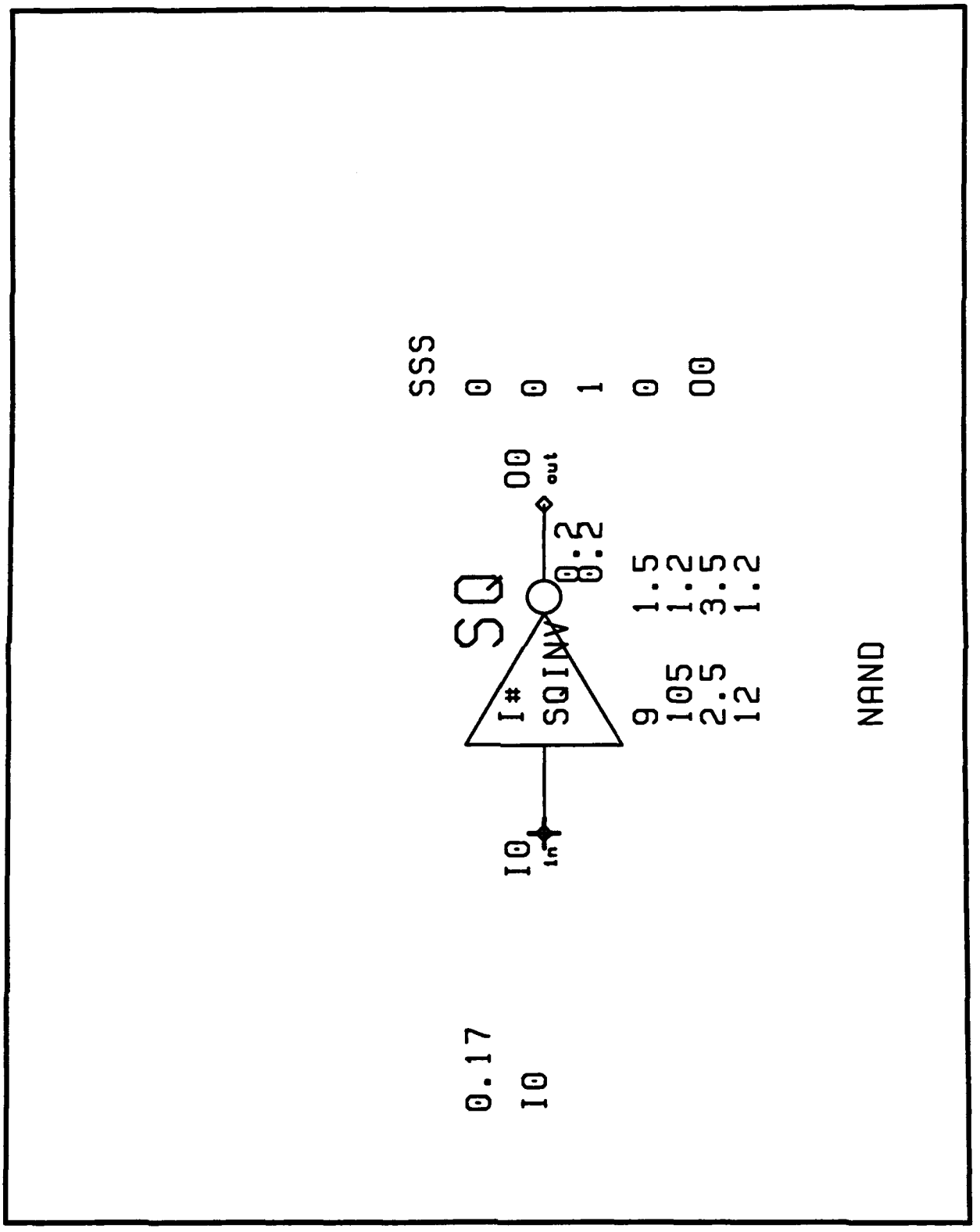

A
B
Q
AF
BF
QF
QB
REGBIT2
QREG
SLOWBIT
SLOWOHI: 10MHz sync, active high
VTT
B
AF
B
IF
AF
IF
BF
AF
BF
QF
AF
QF
AF
A
IF
BF
LOIO
CLK
CLR
ALULO
I

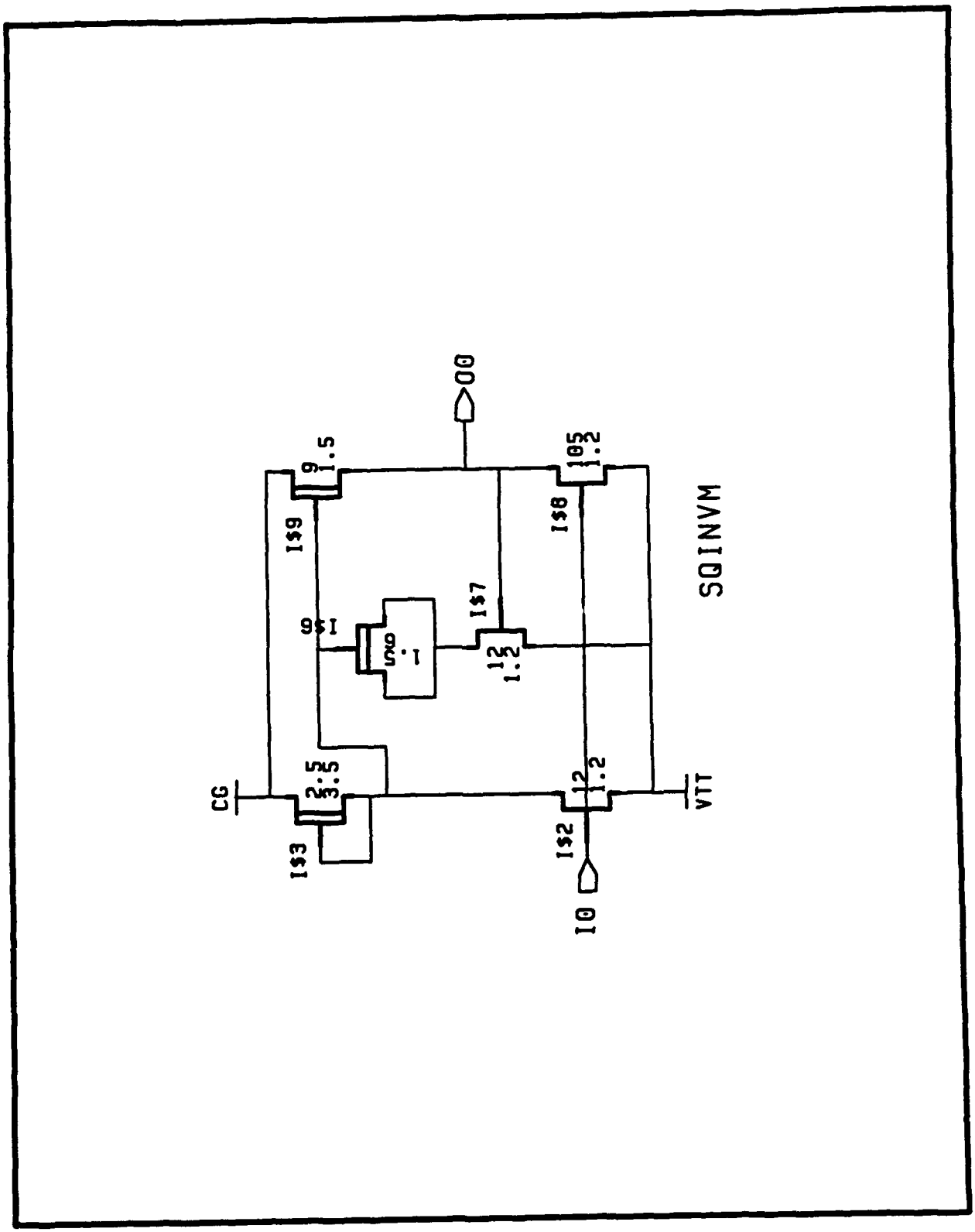

UXX
SLOMOLO
I
Q
OUT
IN
ALULD
LD10
SET
CLK

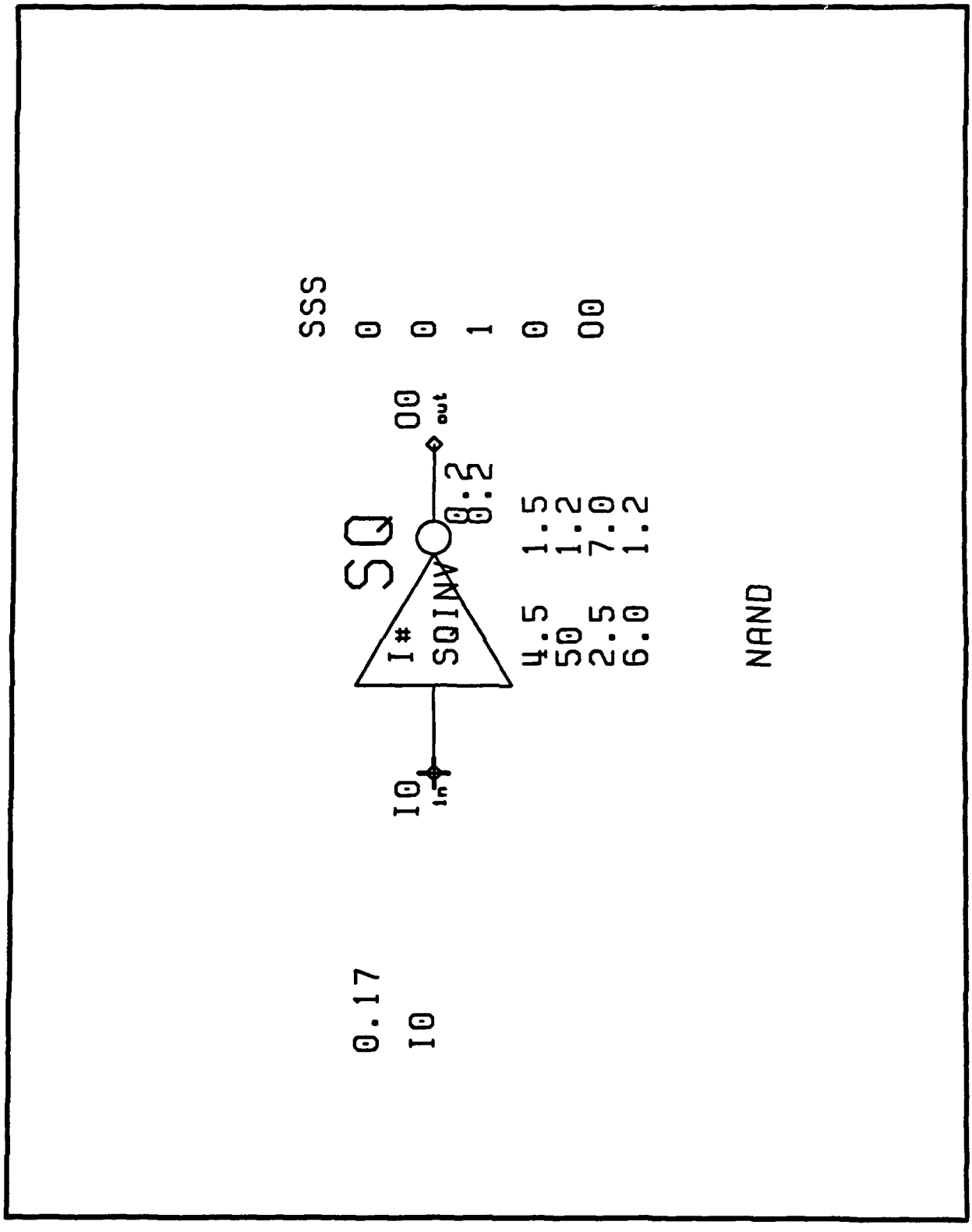

SLOWOLO: 18MHZ sync, active low
A
B
Q
AF
BF
QF
QA
REGBIT
QB
REGBIT
QREG
SLOWBIT
VTT
IF
I
LD10
CLK
SET
ALULO

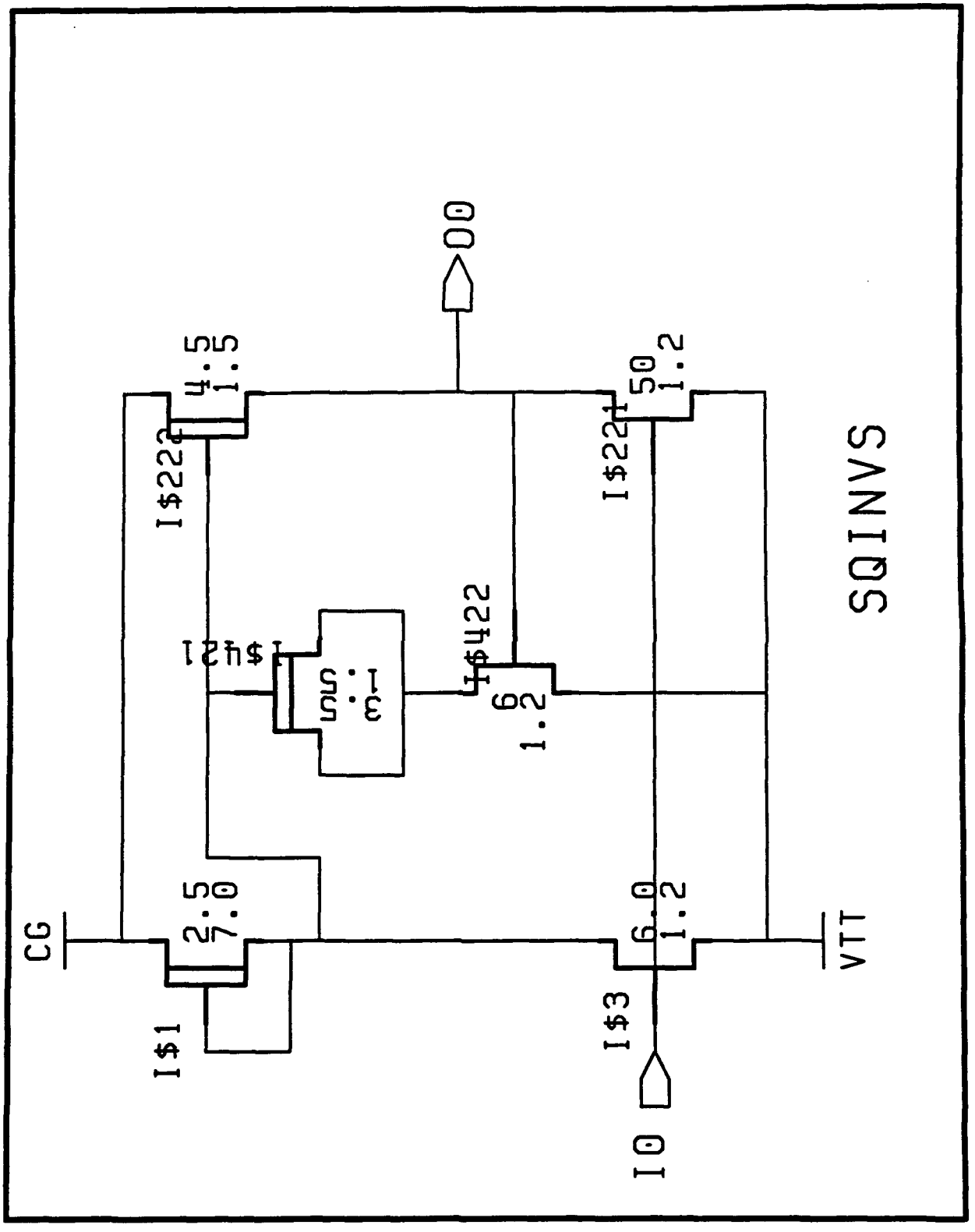

SSS
0 0 1 0 00
out
8:3
00
SNOR2
I#
I0
I1
In
In
NOR
0.17
I0
0.17
I1

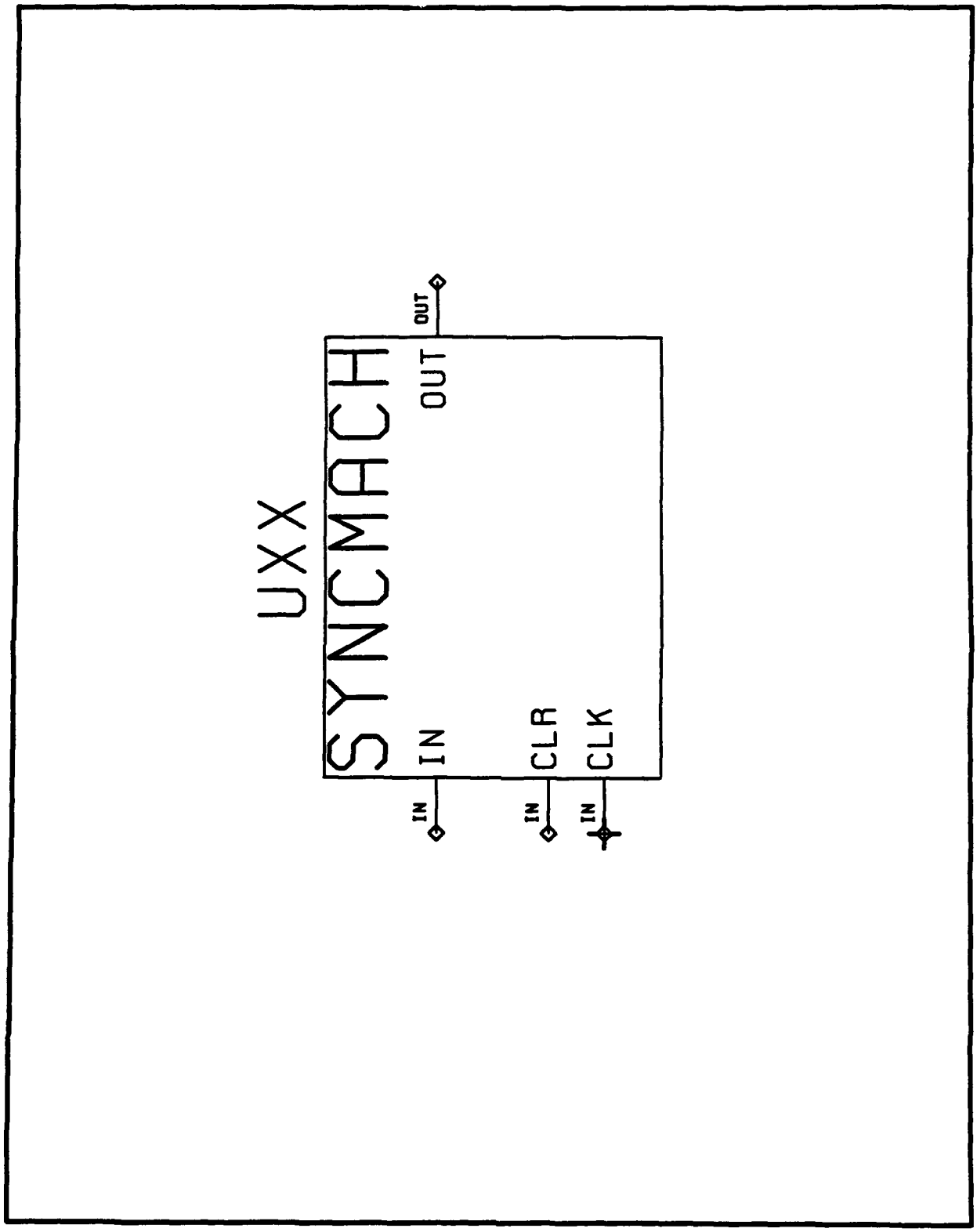

SNOR2
O0
I0
I1
CG
VTT
I$1
I$3
I$222
I$221
I$421
I$422
I$461
I$462

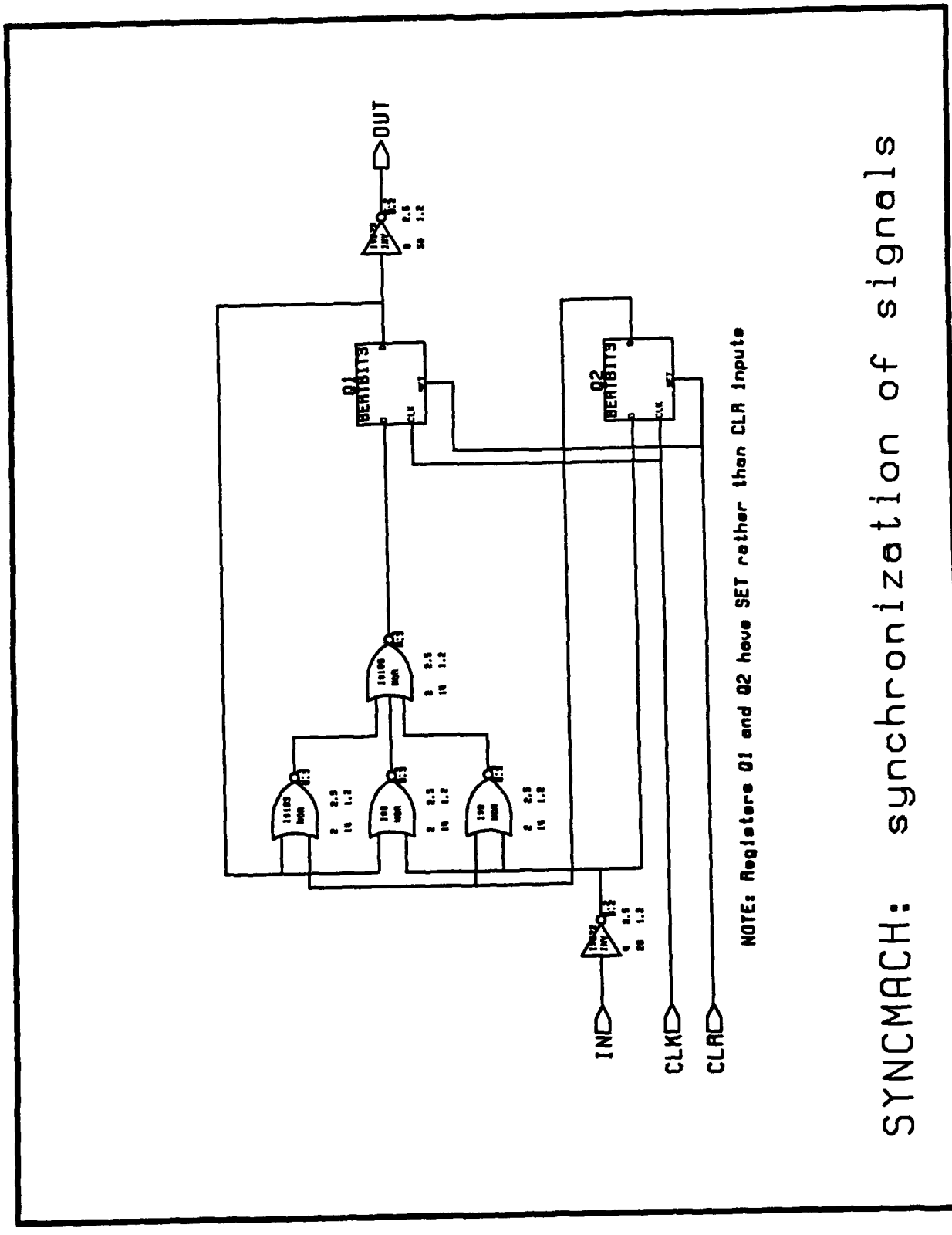

SSS
0 0 1 0 00
00
out
8.2
SQ
1.5
1.2
3.5
1.2
I#
SQINV
9
105
2.5
12
NAND
IO
in
0.17
IO

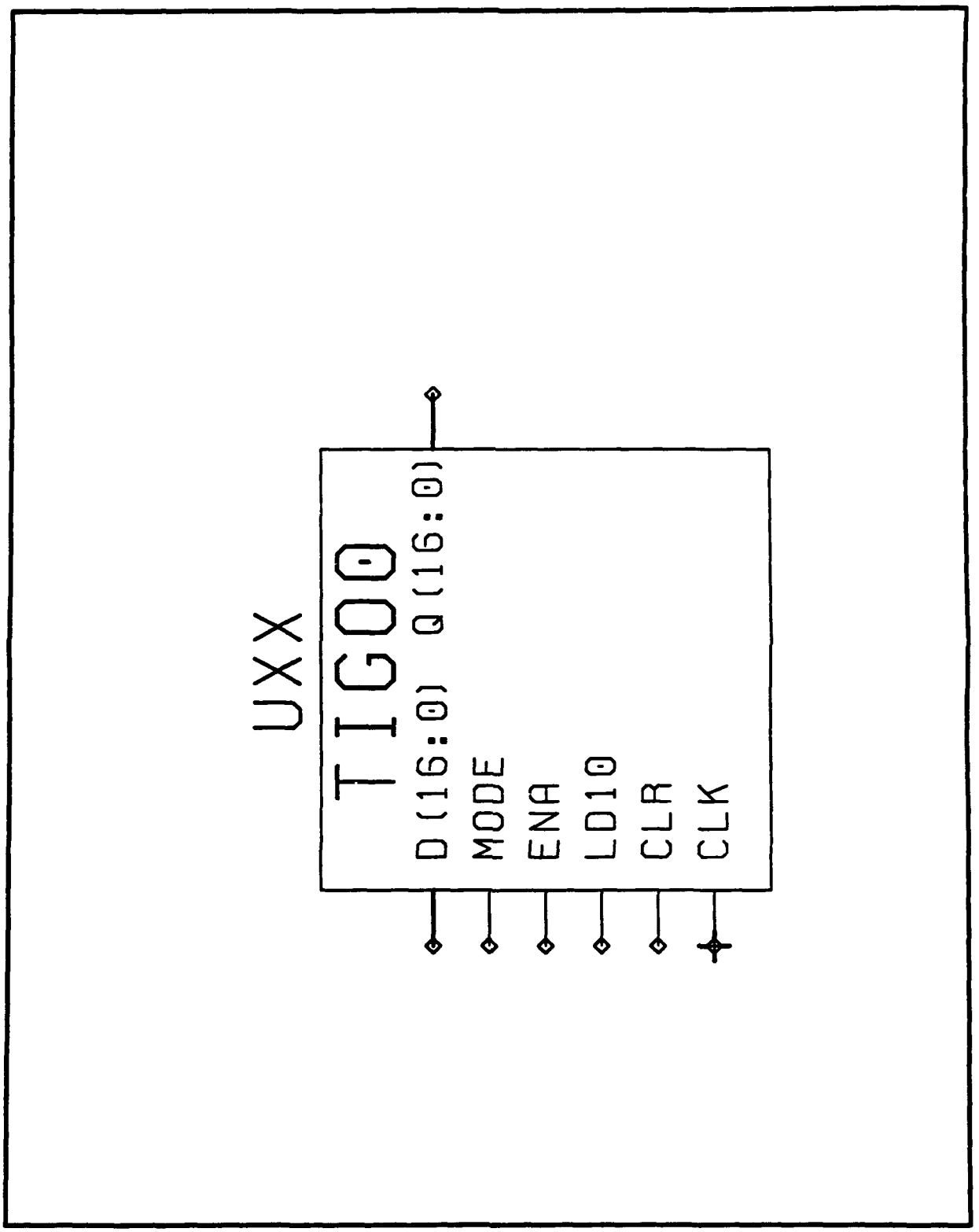

OO
I$9
I$8
I$7
I$6
I$3
I$2
I0
CG
VTT
SQINVM

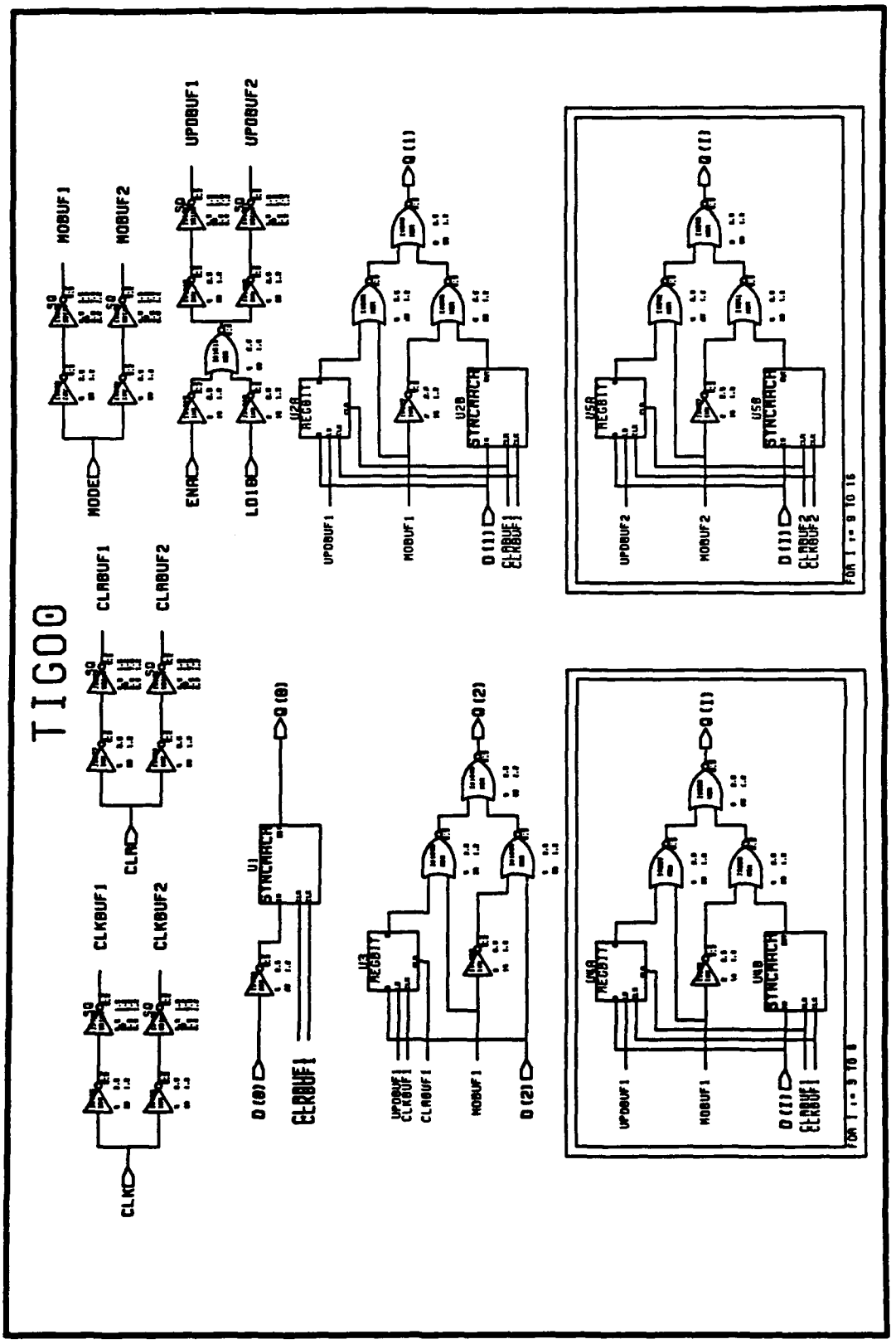

SSS
0 0 1 0 00
00
out
8.2
SQ
I#
SQINV
4.5 1.5
50 1.2
2.5 7.0
6.0 1.2
NAND
IO
in
0.17
IO

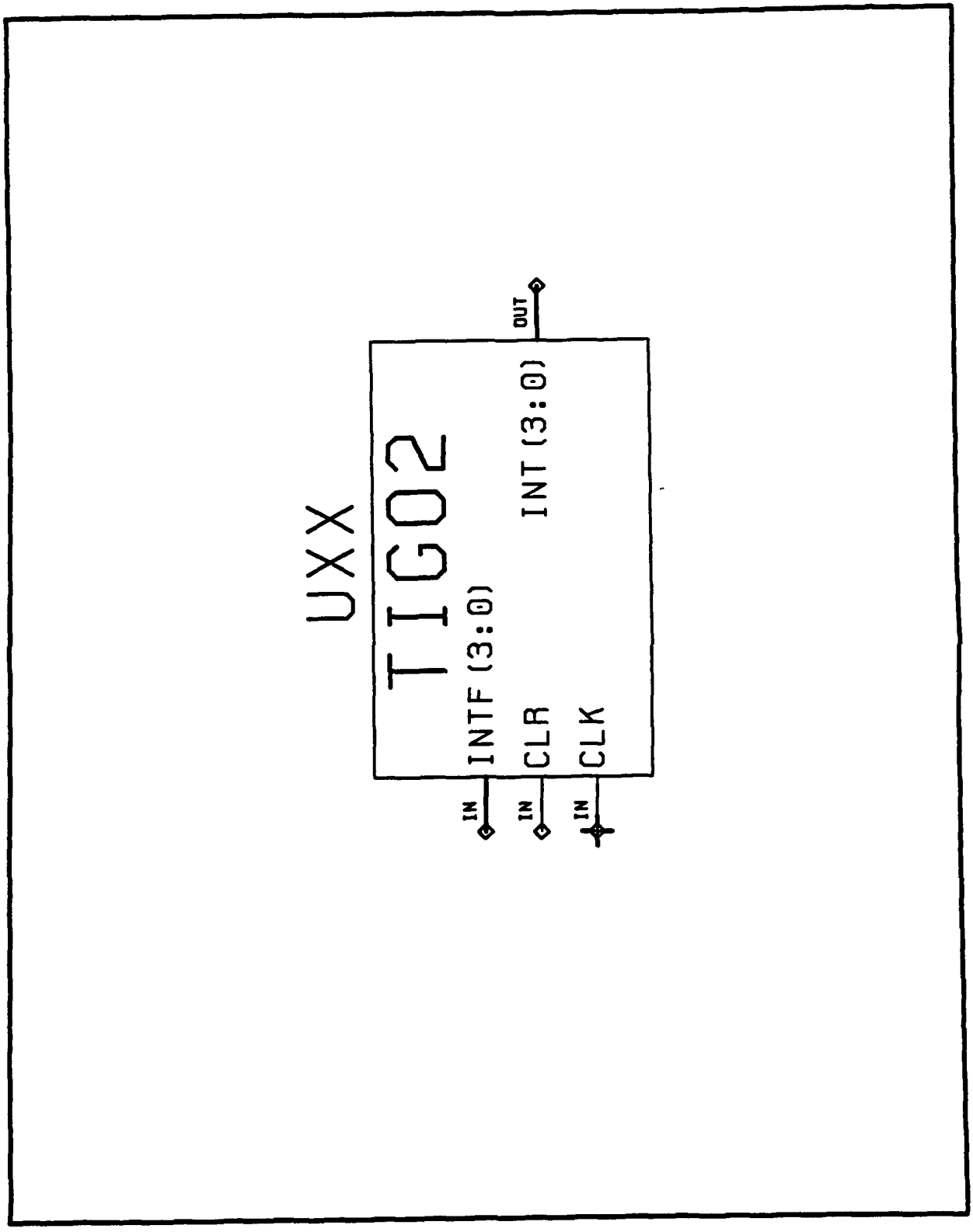

SQINVS
O0
I0
CG
VTT
I$1
I$3
I$221
I$222
I$421
I$422
4.5
1.5
50
1.2
2.5
7.0
6.0
1.2
3.5
1.3
1.6
1.2

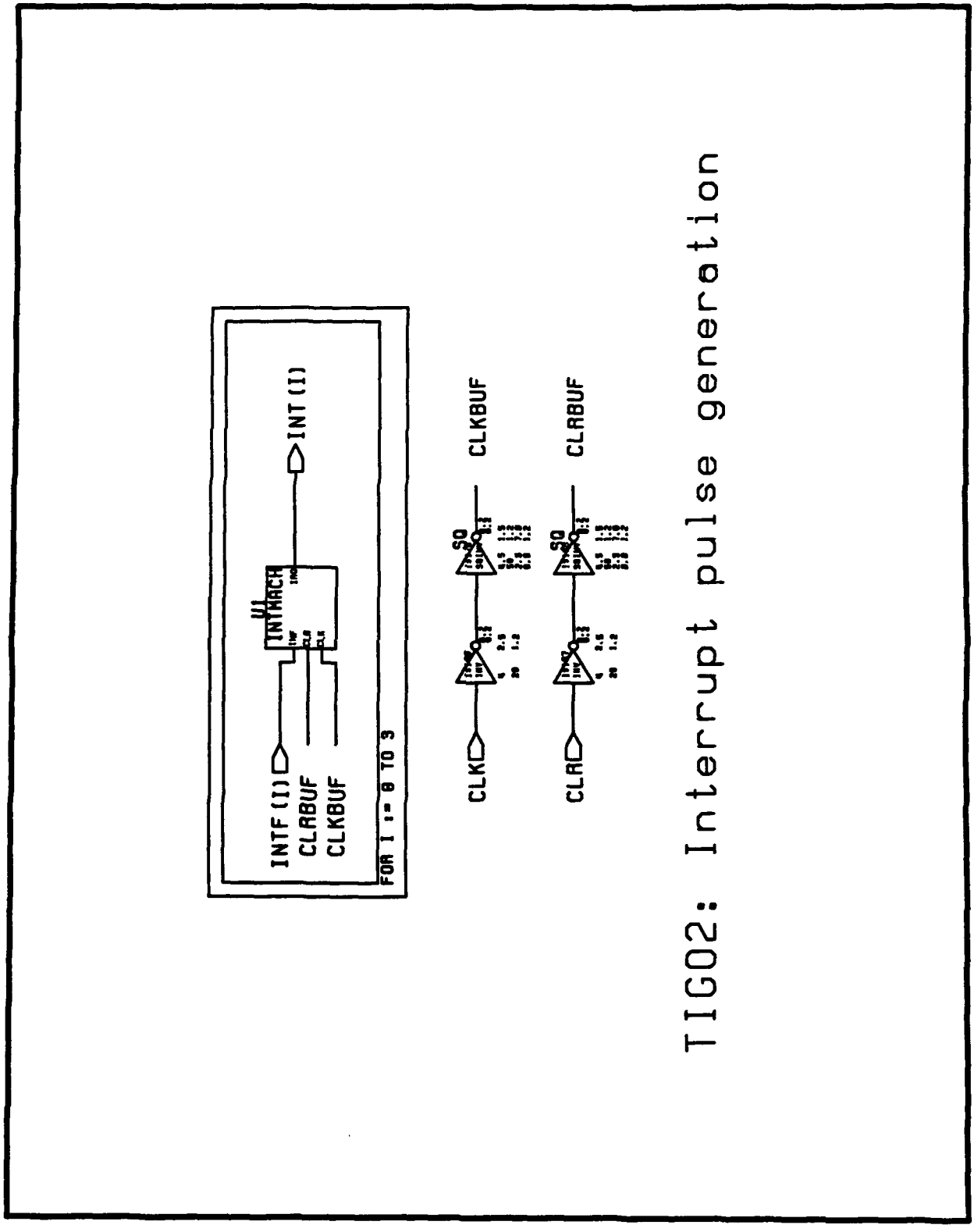

UXX
SYNCMACH
OUT
IN
CLR
CLK
OUT
IN
IN
IN

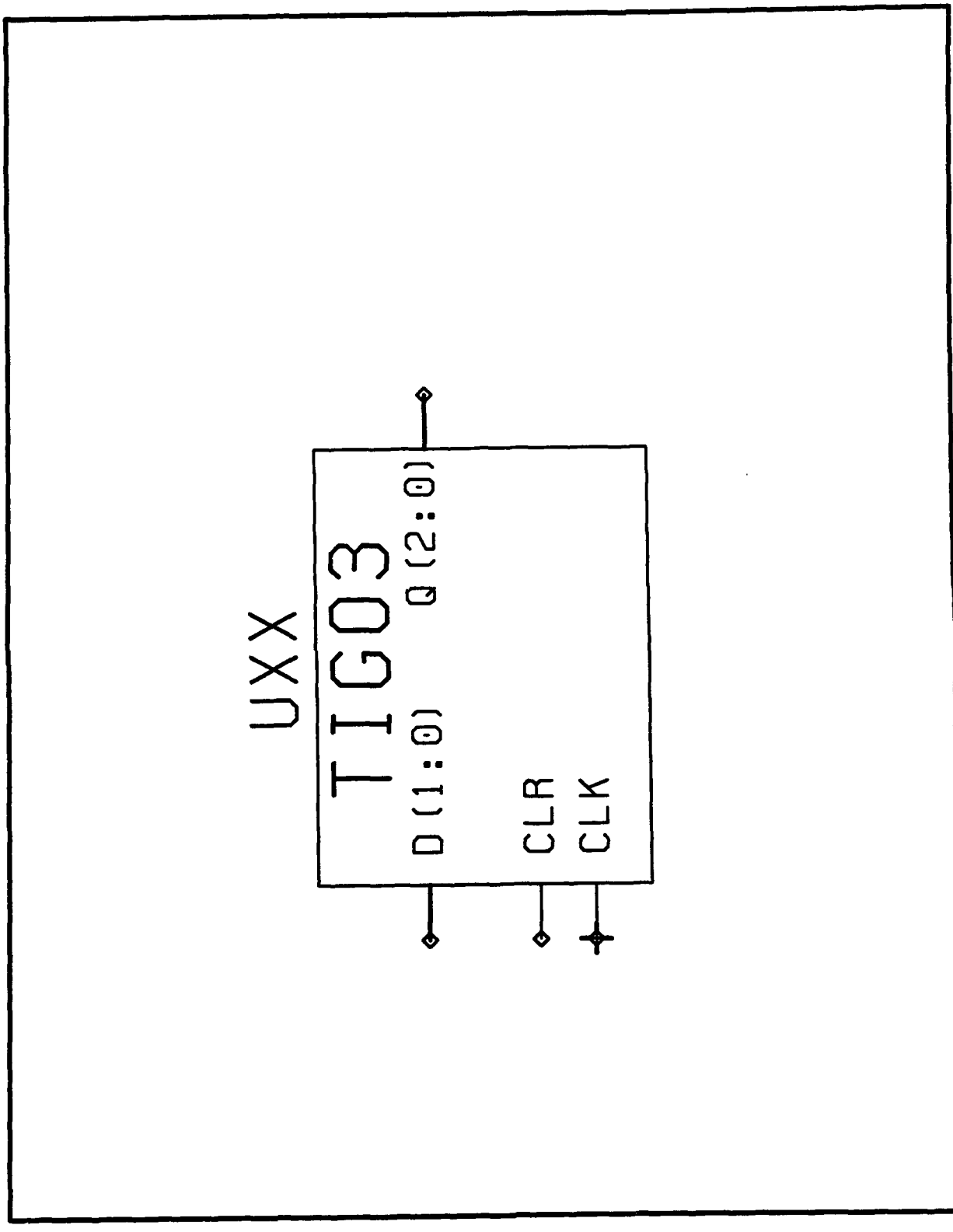

SYNCMACH: synchronization of signals
NOTE: Registers 01 and 02 have SET rather than CLR inputs
OUT
IN
CLK
CLR
01
02
BEN1B1T3

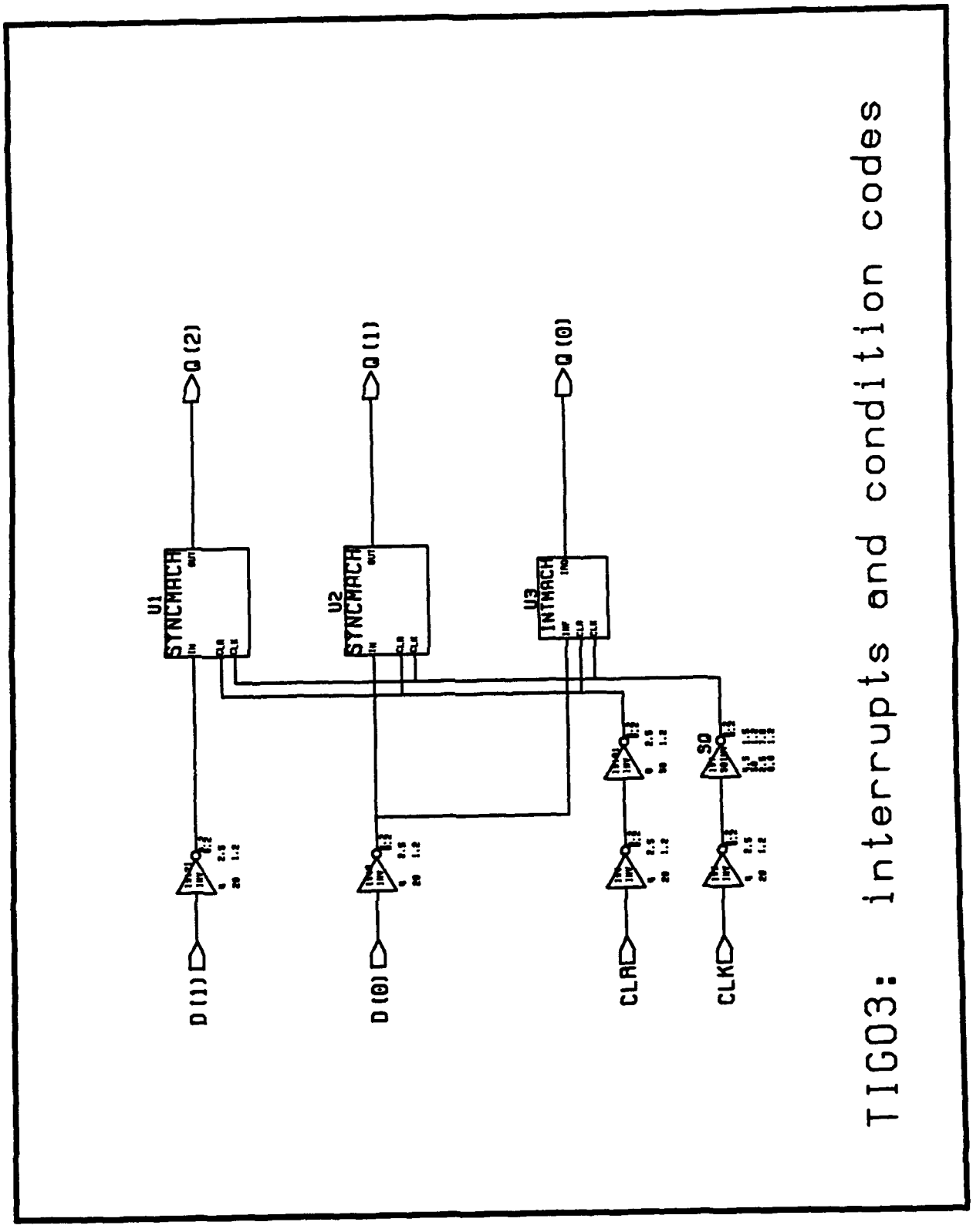

UXX
TIGQQ
D(16:0)
Q(16:0)
MODE
ENA
LD10
CLR
CLK

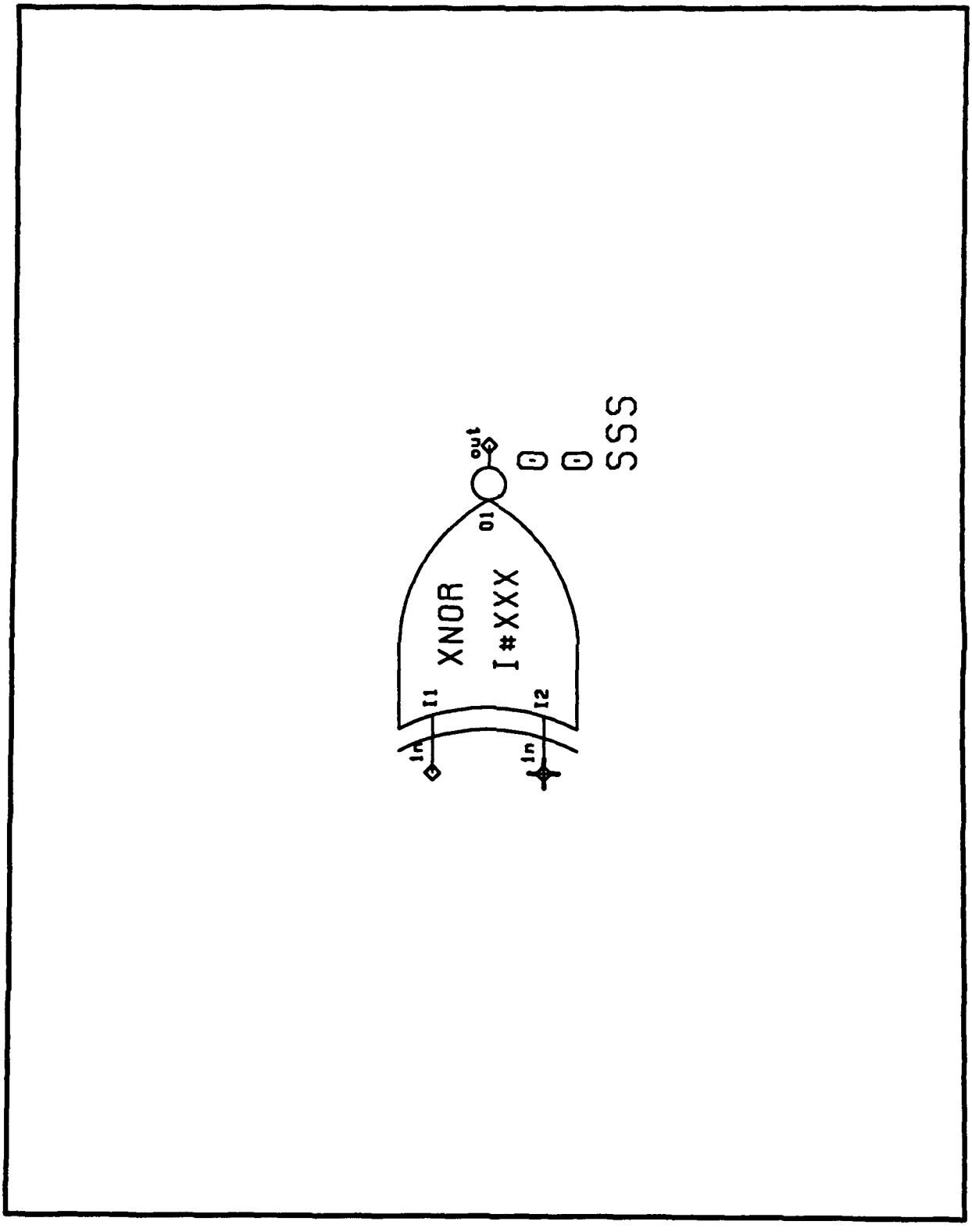

TIC00
MODBUF1
MODBUF2
UPDBUF1
UPDBUF2
MODE
ENA
LOAD
CLABUF1
CLABUF2
CLKBUF1
CLKBUF2
CLA
CLK
U1
SYNCHRCH
U2B
REGBIT
U3
U4B
U5B
D(1)
D(2)
D(0)

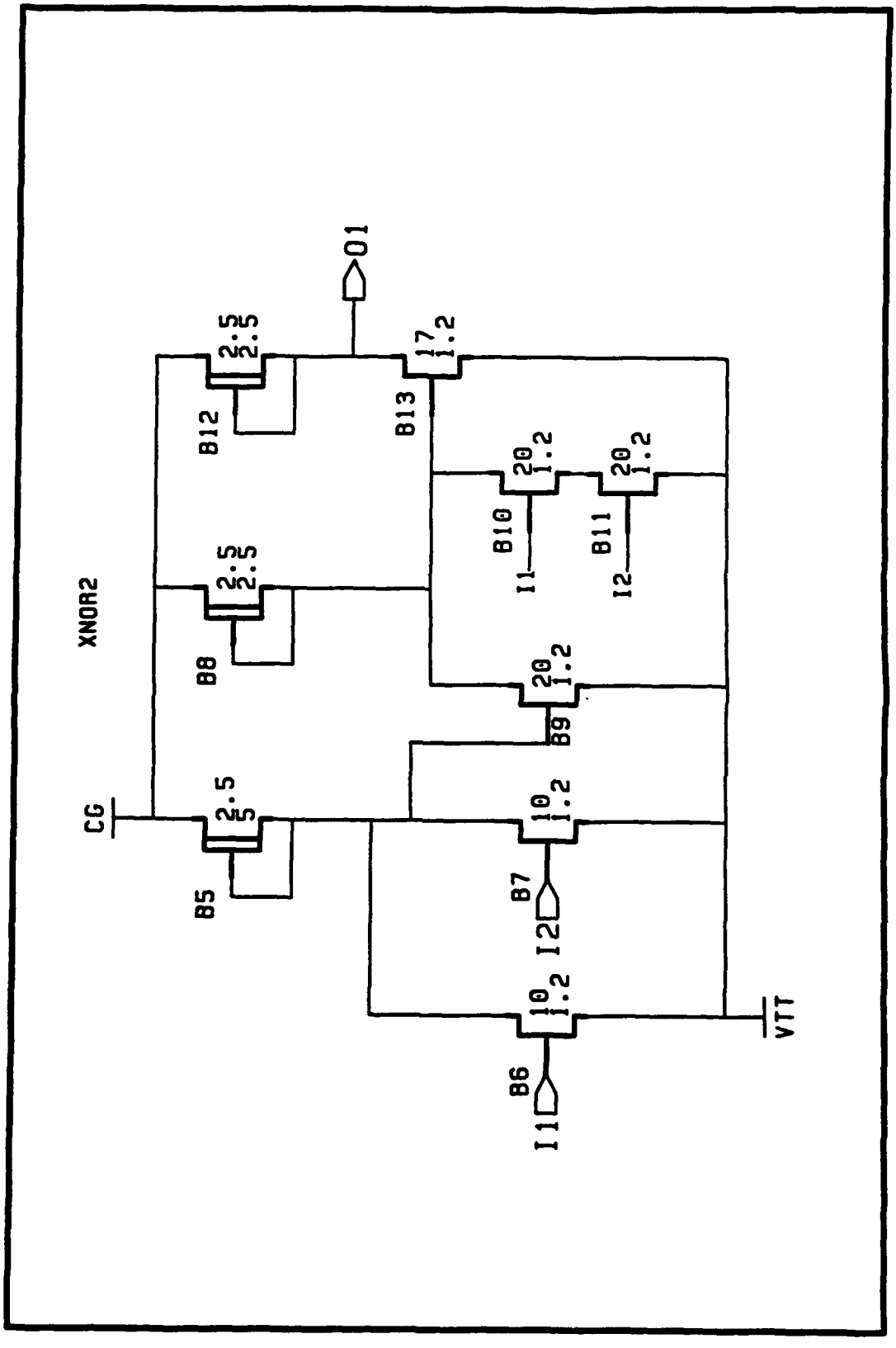

UXX
TIG02
INTF(3:0)
CLR
CLK
INT(3:0)
IN
IN
IN
OUT

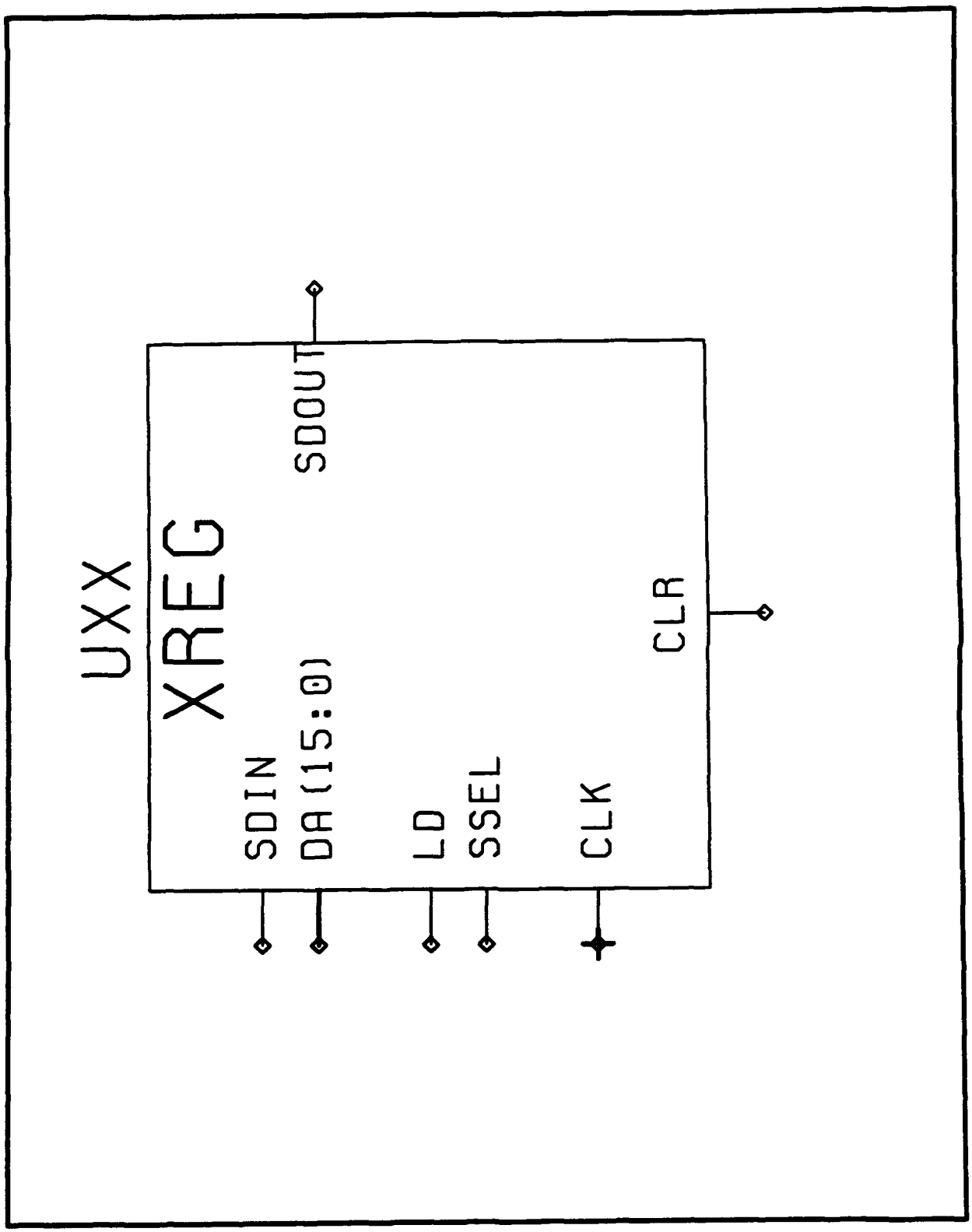

TIG02: Interrupt pulse generation
INT (I)
U1
INTMACH
INTF (I)
CLRBUF
CLKBUF
FOR I := 0 TO 3
CLKBUF
CLRBUF
SO
SO
CLK
CLR

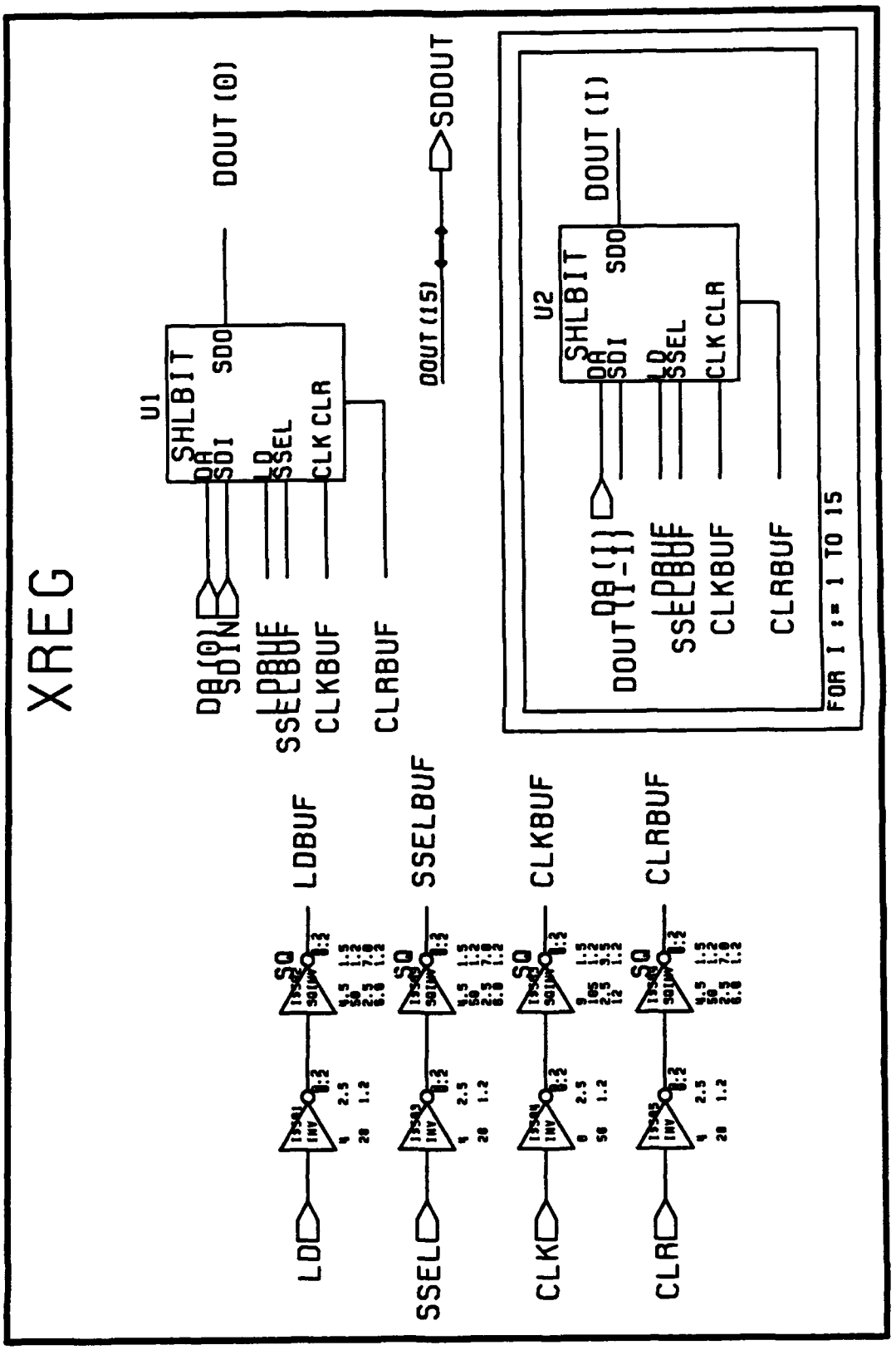

UXX
TIG03
D(1:0)
Q(2:0)
CLR
CLK

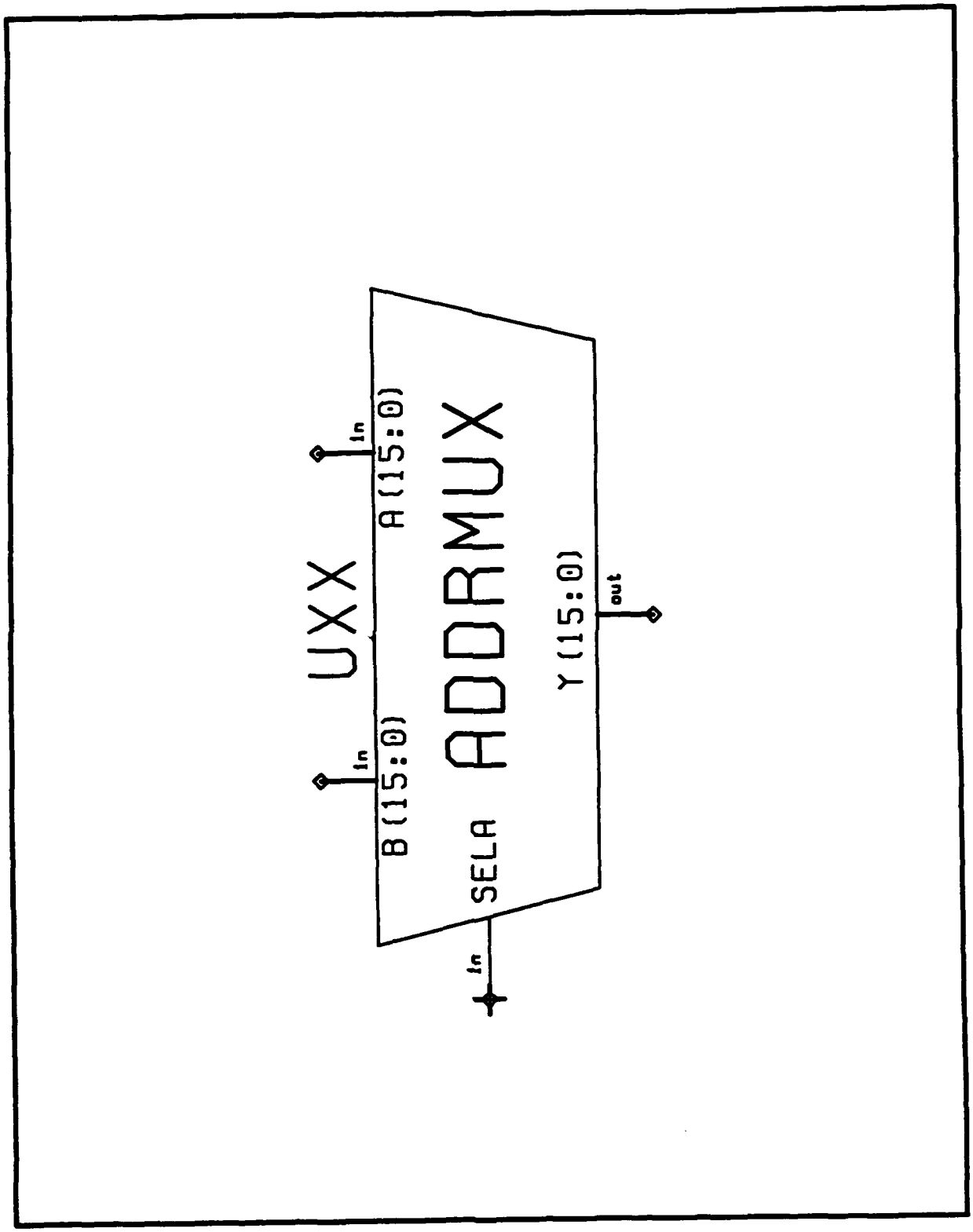

TIC03: interrupts and condition codes
Q(2)
Q(1)
Q(0)
U1
SYNCMACH
U2
SYNCMACH
U3
INTMACH
SO
D(1)
D(0)
CLR
CLK

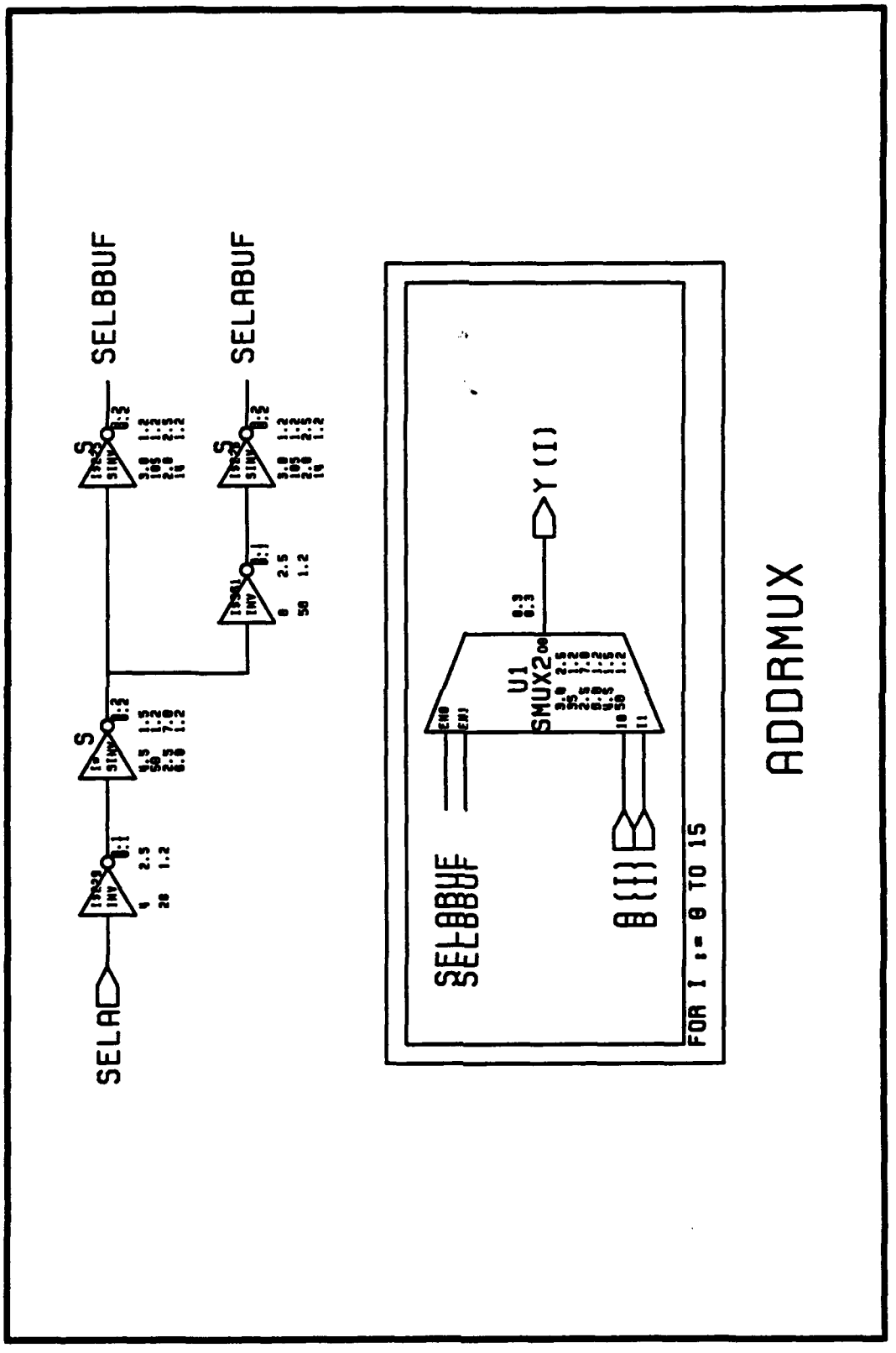

SSS
0
0
out
01
XNOR
I#XXX
I1
I2
In
In

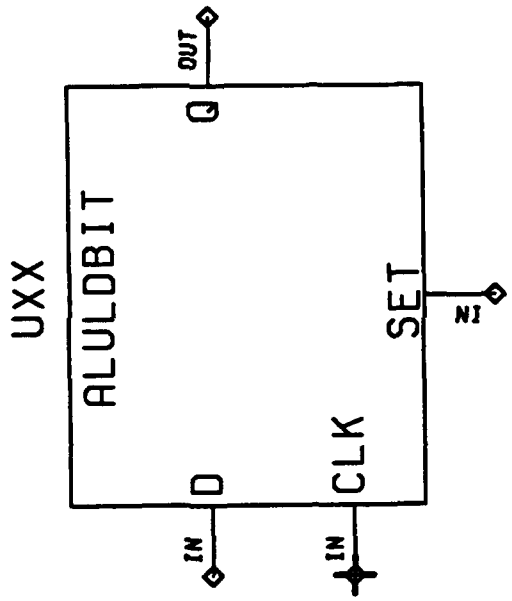

XNOR2
O1
B12
B13
B10
B11
B8
B9
B5
B7
B6
I1
I2
CG
VTT
2.5
2.5
17
1.2
20
1.2
20
1.2
2.5
2.5
20
1.2
2.5
2.5
10
1.2
10
1.2

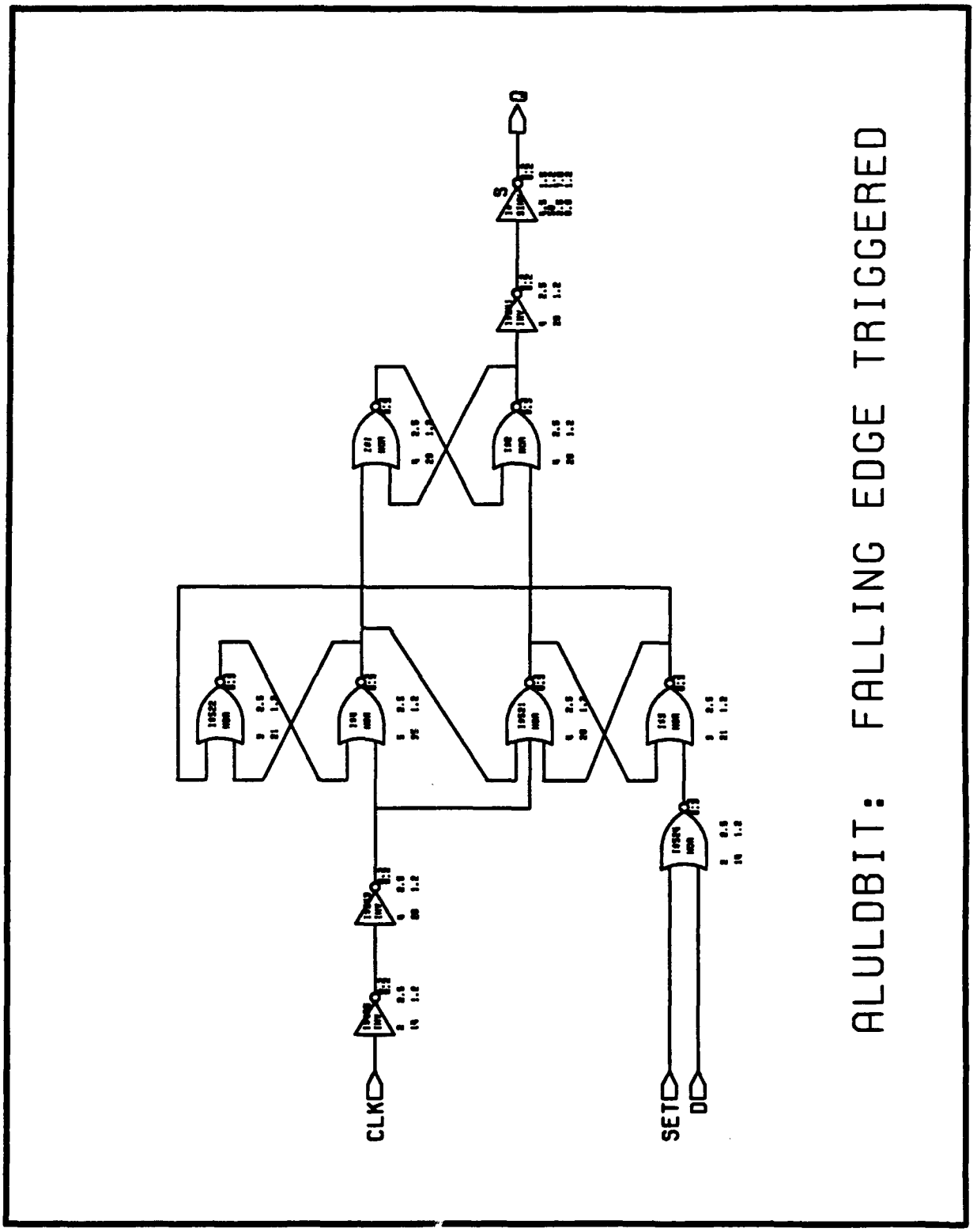

UXX
XREG
SDOUT
SDIN
DA(15:0)
LD
SSEL
CLK
CLR

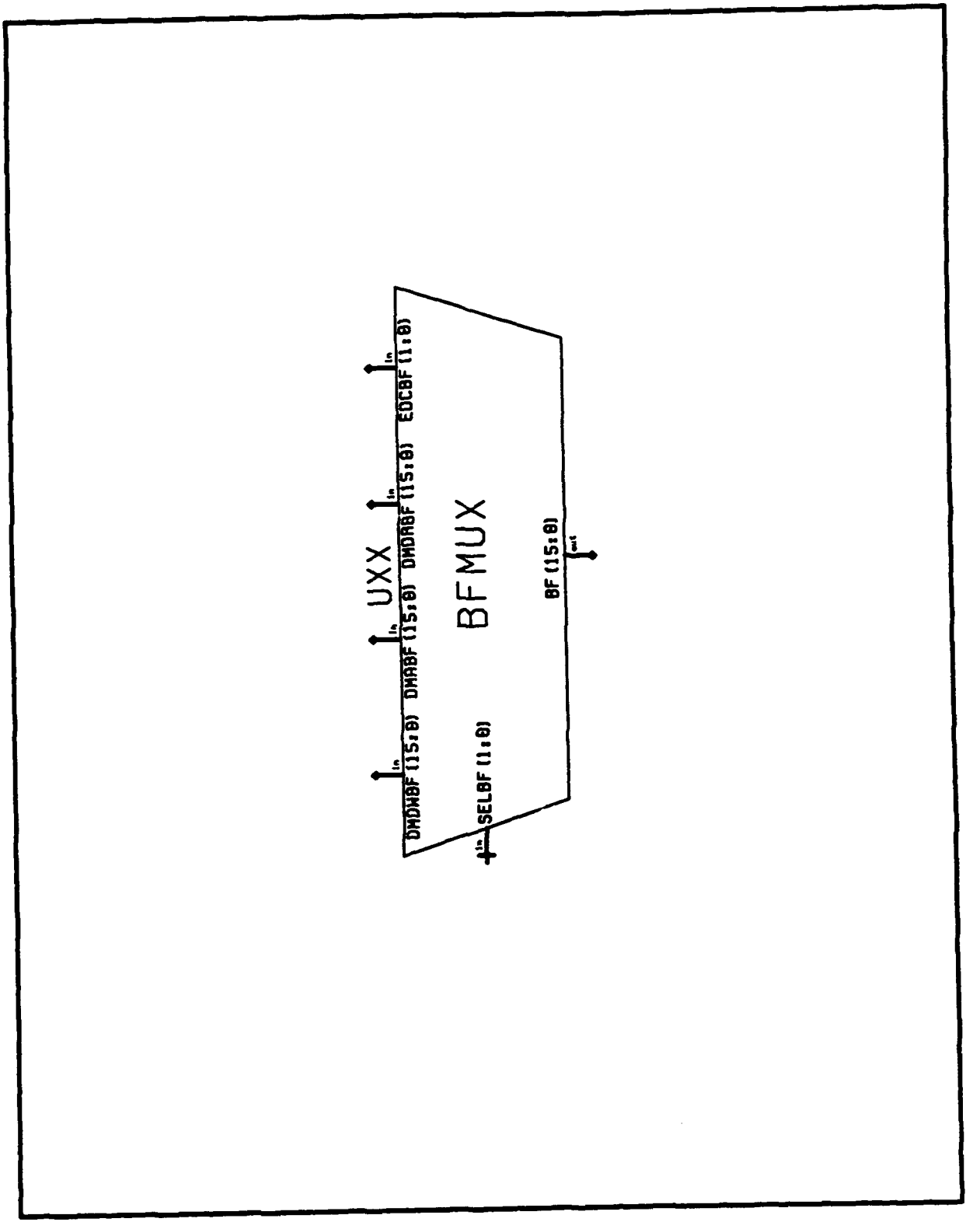

XREG
U1
SHLBIT
DA
SDI
LD
SSEL
CLK
CLR
SDO
DOUT (0)
SDOUT
DOUT (15)
U2
DOUT (I)
DOUT[DA-1]
FOR I := 1 TO 15
DA(0)
SDIN
LDBUF
SSELBUF
CLKBUF
CLRBUF
LD
SSEL
CLK
CLR

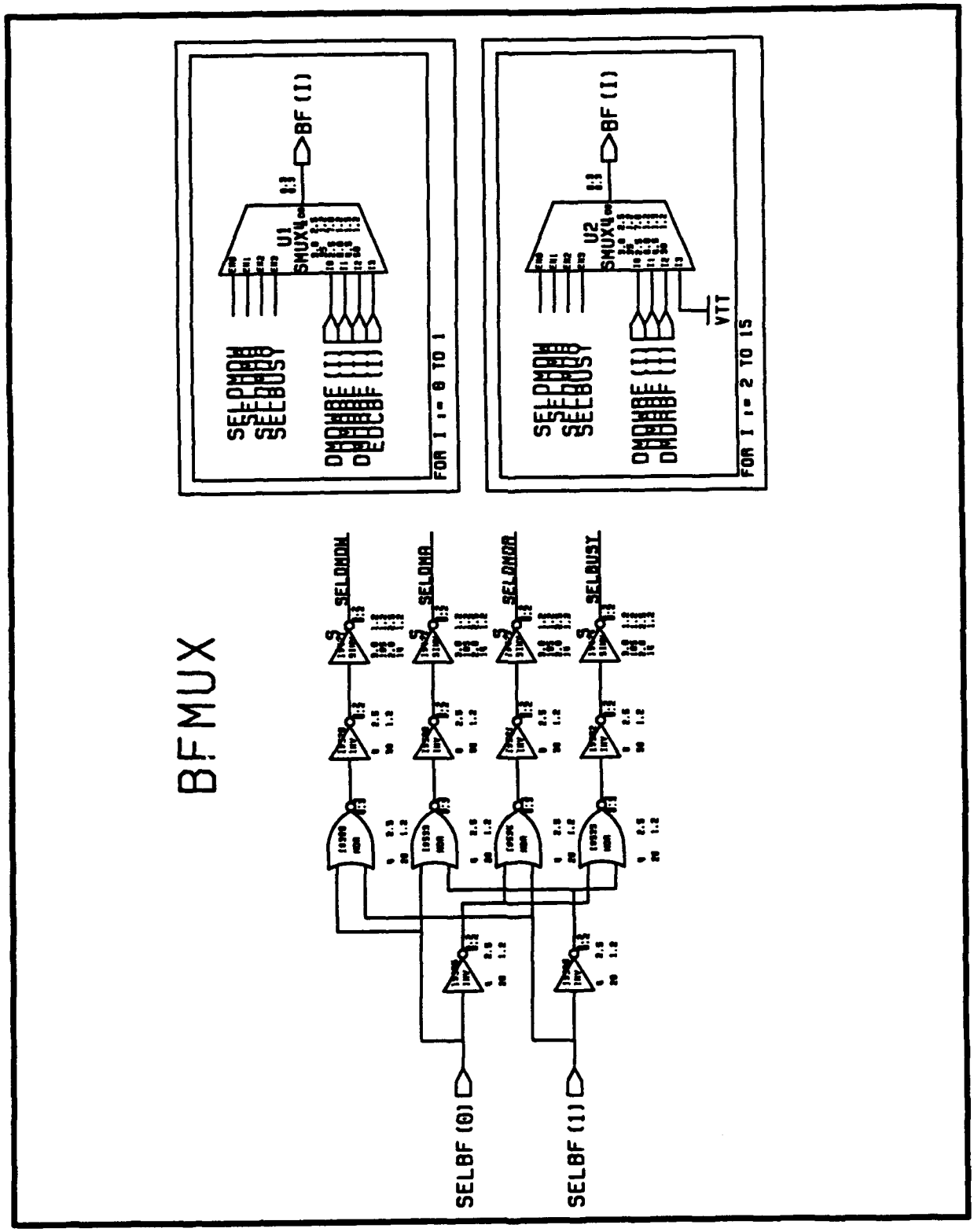

UXX
ADDRMUX
A(15:0)
B(15:0)
SELA
Y(15:0)
in
in
in
out

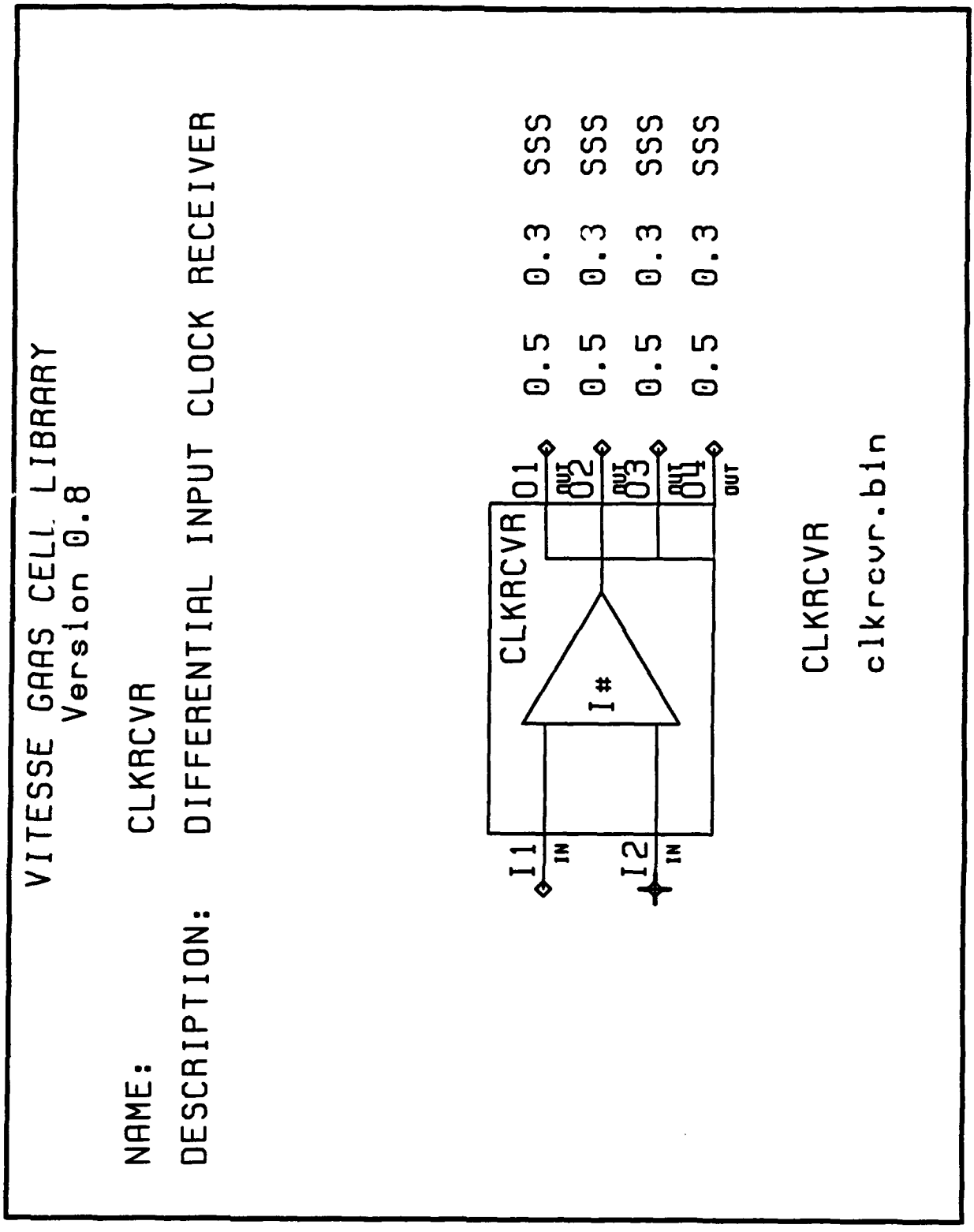

SELBBUF
SELABUF
S
S
S
SELA
SELBBUF
Y (I)
U1
SMUX2
B(I)
FOR I := 0 TO 15
ADDRMUX

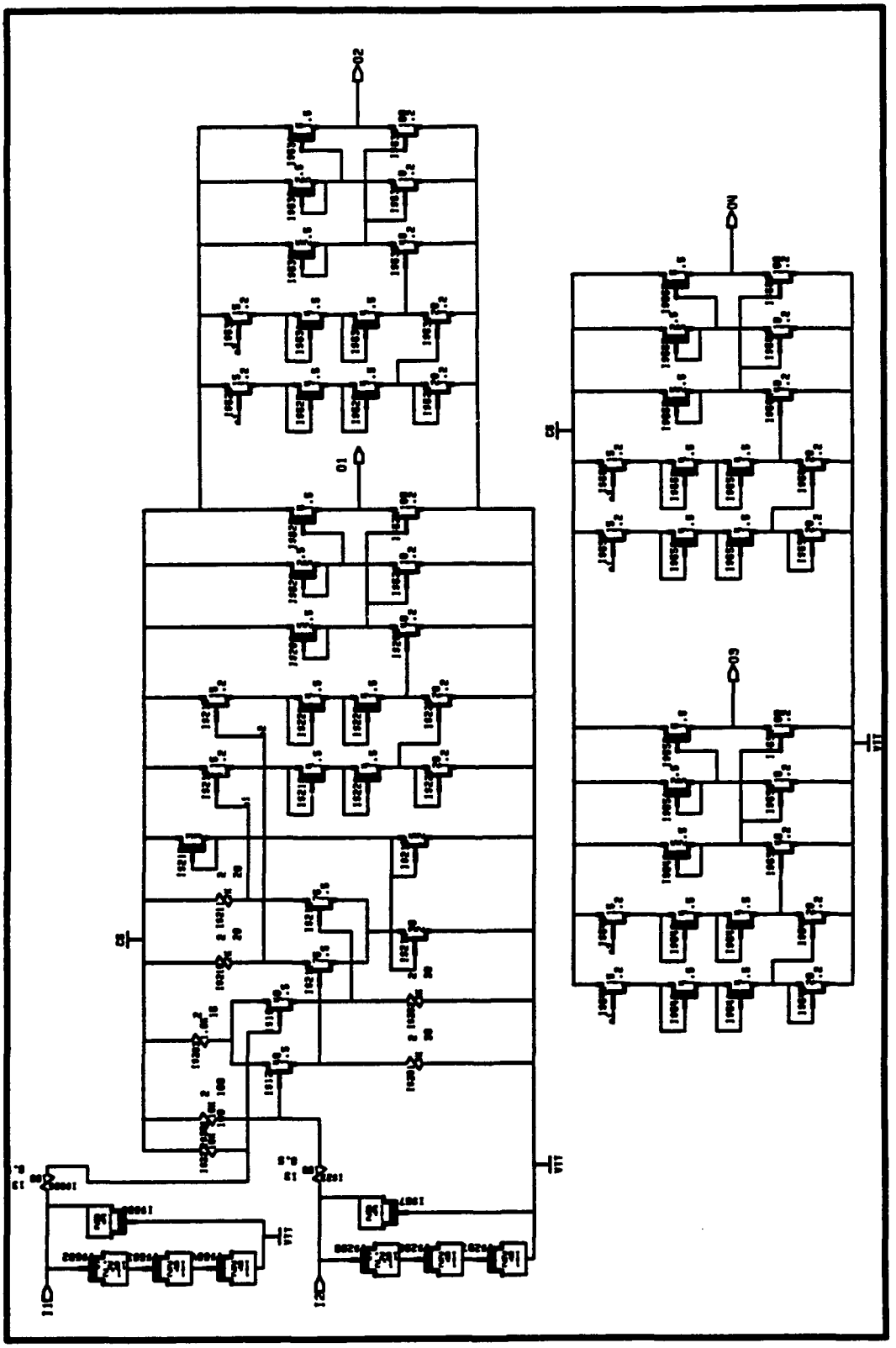

UXX
ALULDBIT
Q
OUT
SET
NI
D
IN
CLK
IN

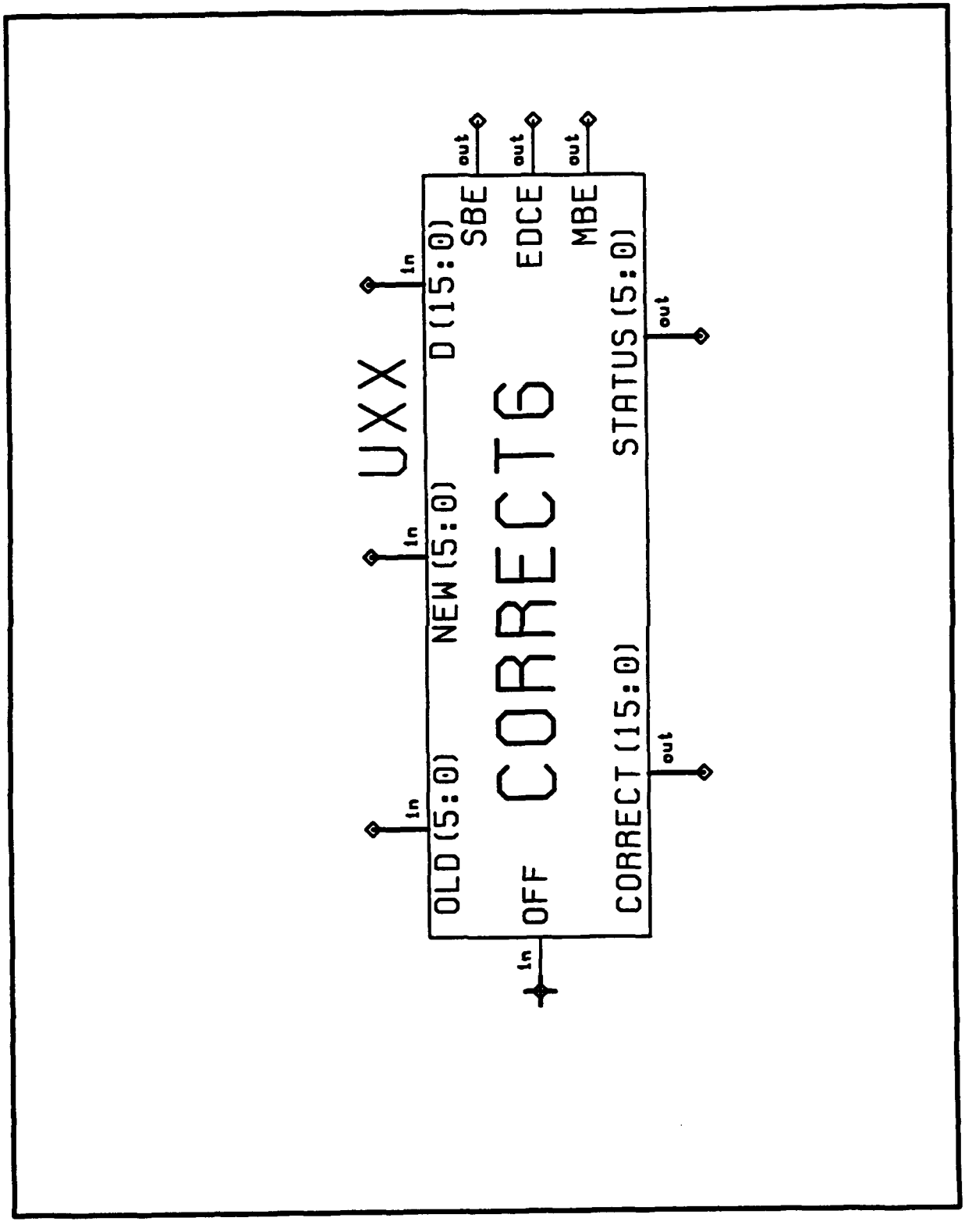

ALULDBIT: FALLING EDGE TRIGGERED
Q
S
CLK
SET
D

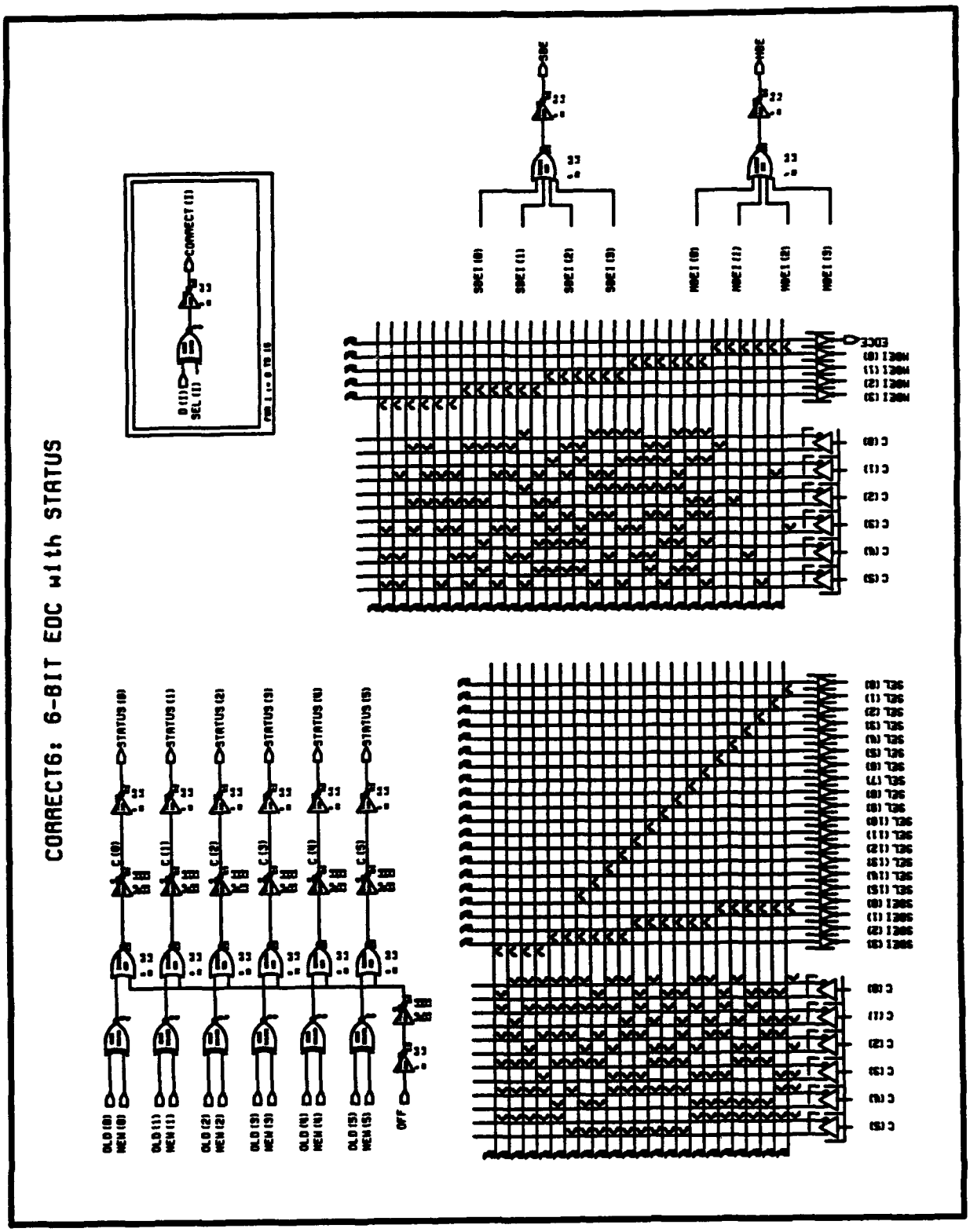

UXX
BFMUX
DMDXHBF (15:0)
DMAHBF (15:0)
DMDRHBF (15:0)
EDCBF (1:0)
SELBF (1:0)
BF (15:0)

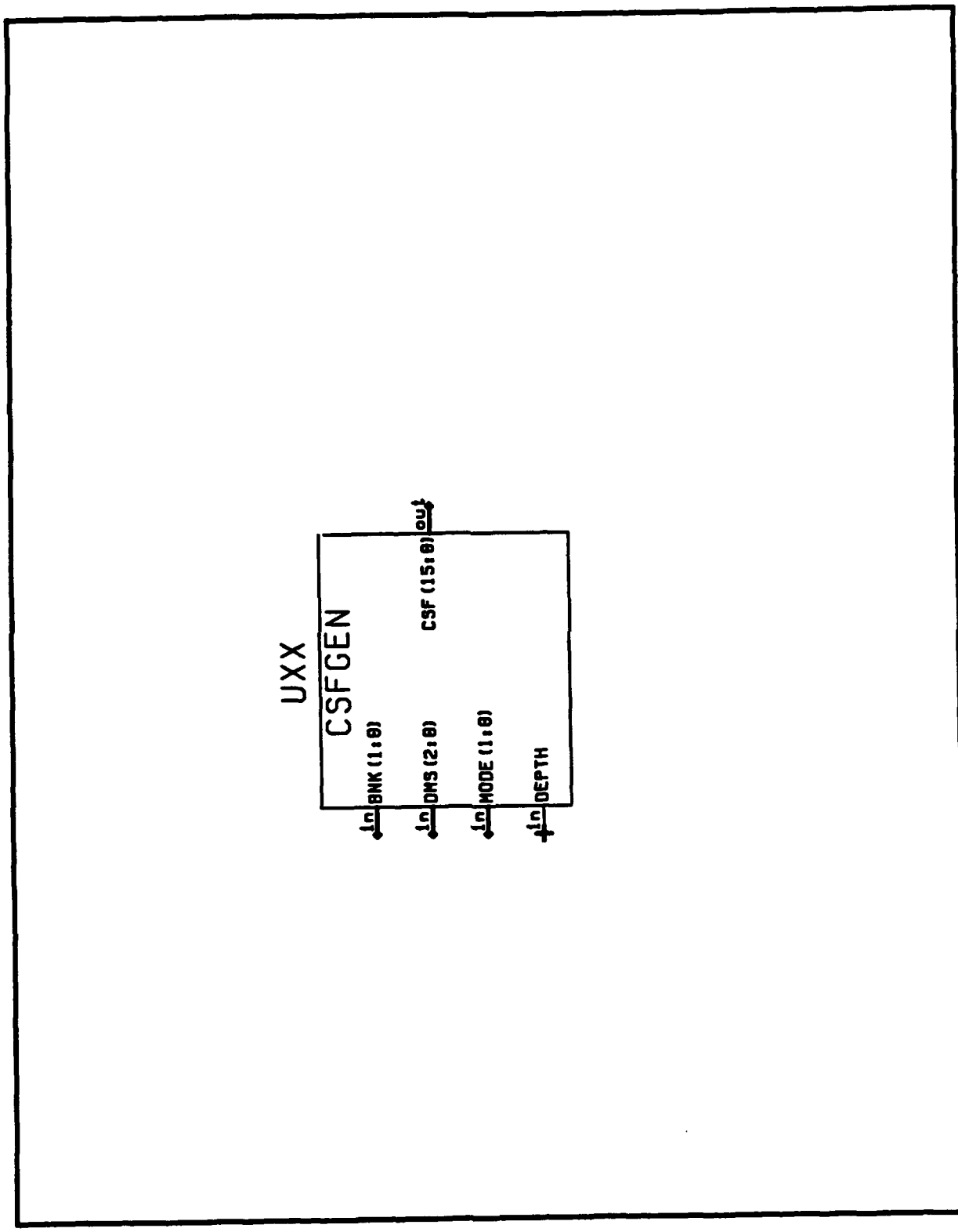

BF (1)
U1
SMUX4
SELDMDW
SELBUSY
DMDWBE (1:1)
DMDWBF
FOR I := 0 TO 1
BF (1)
U2
SMUX4
VTT
SELDMDW
SELBUSY
DMDWBE (1:1)
DMDWBF
FOR I := 2 TO 15
BFMUX
SELDMDW
SELDMDR
SELDMDR
SELBUSY
SELBF (0)
SELBF (1)

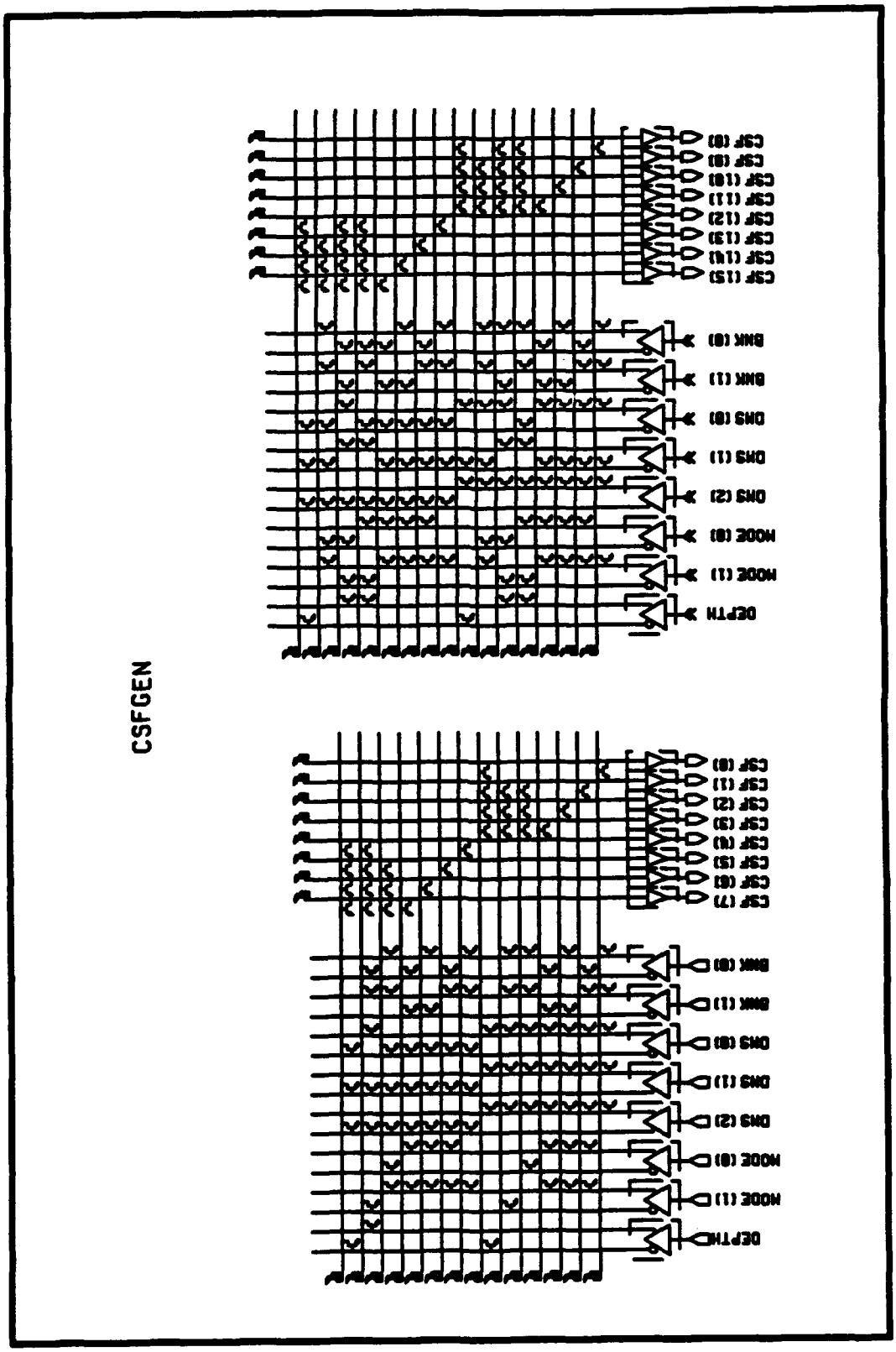

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: CLKRCVR
DESCRIPTION: DIFFERENTIAL INPUT CLOCK RECEIVER
0.5 0.3 SSS
0.5 0.3 SSS
0.5 0.3 SSS
0.5 0.3 SSS
CLKRCVR
O1
O2
O3
O4
OUT
I#
I1
I2
IN
IN
CLKRCVR
clkrcvr.bin

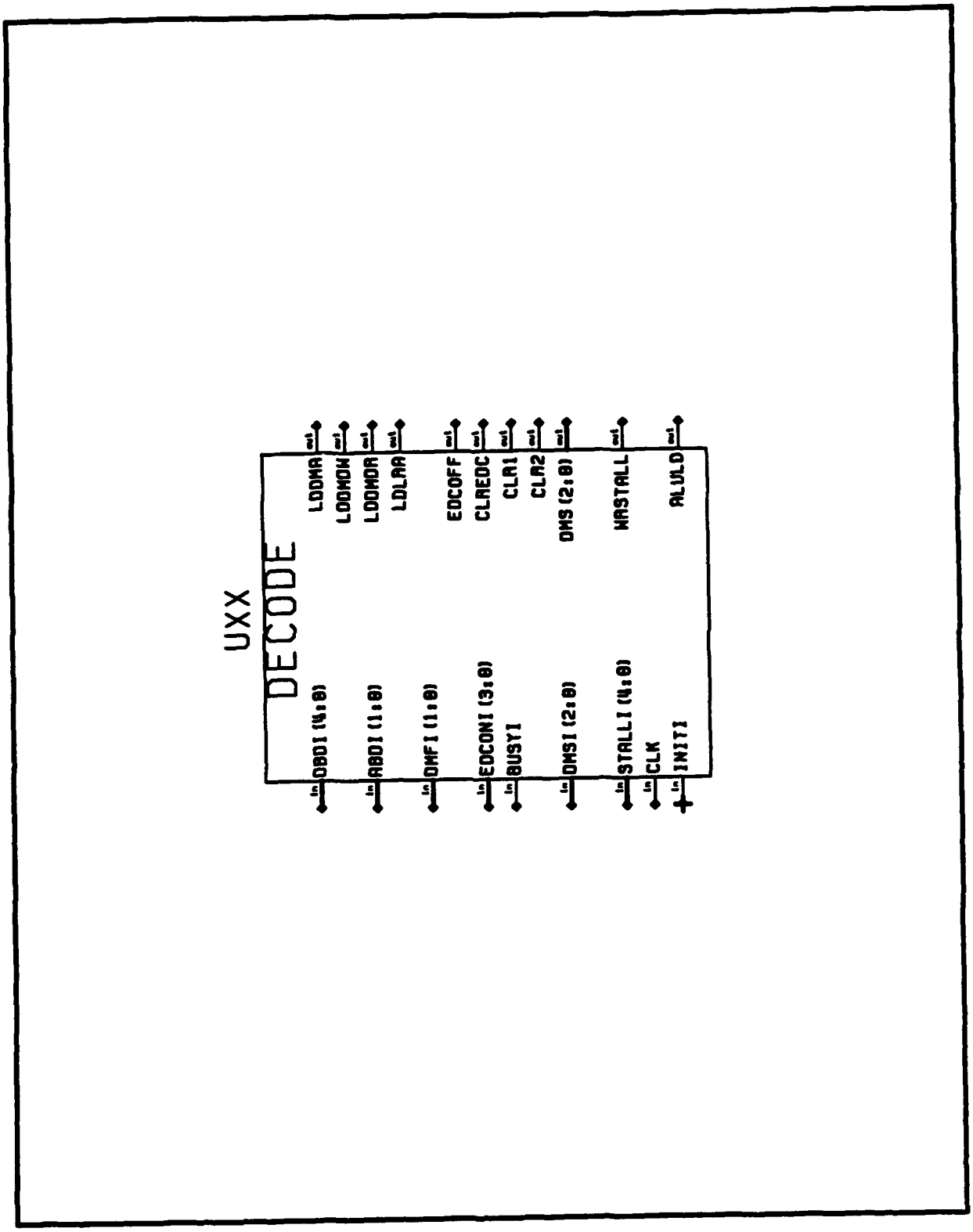


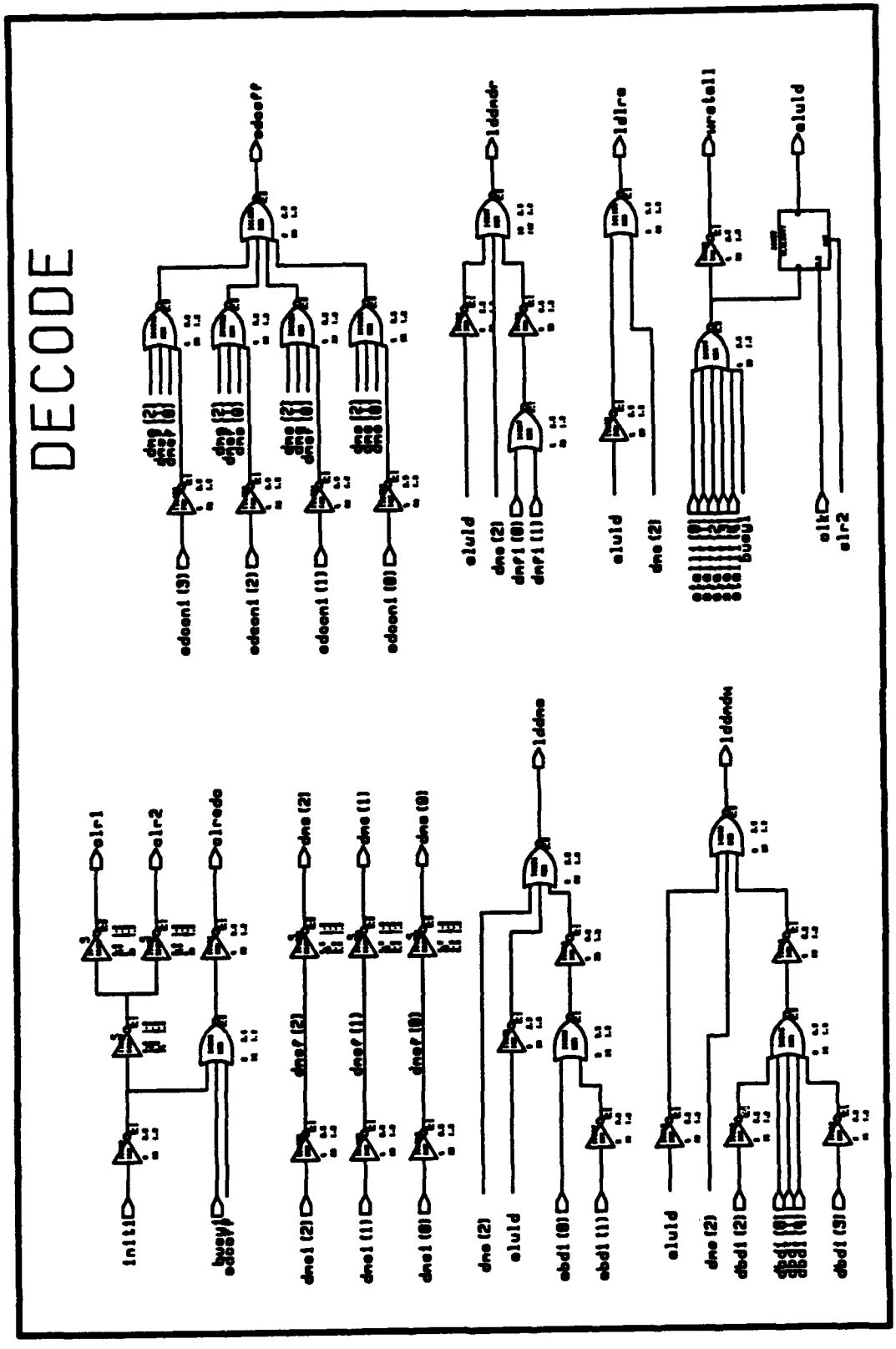

UXX
CORRECT6
D(15:0)
NEW(5:0)
OLD(5:0)
OFF
SBE
EDCE
MBE
STATUS(5:0)
CORRECT(15:0)
in
out

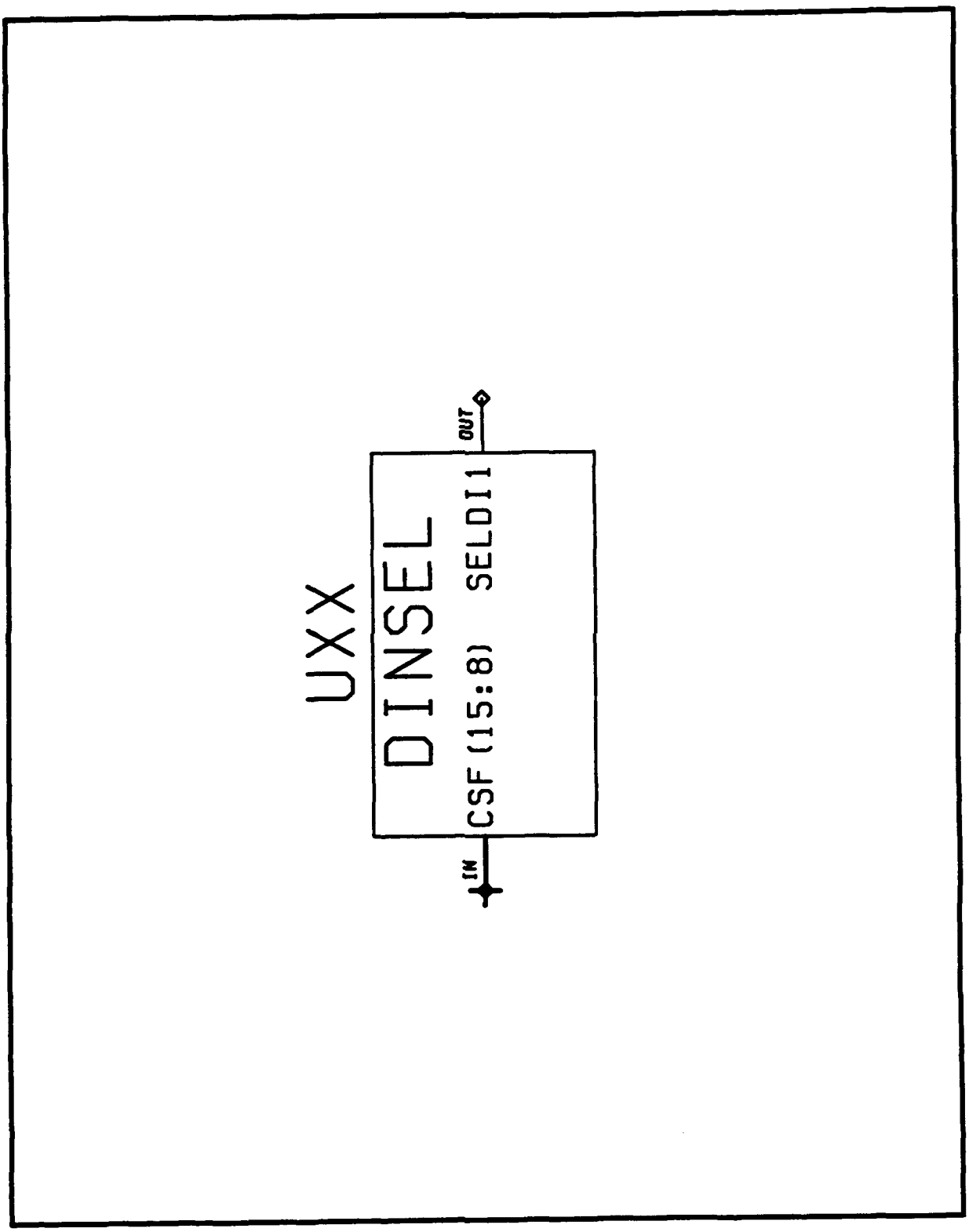

CORRECT6: 6-BIT EDC with STATUS

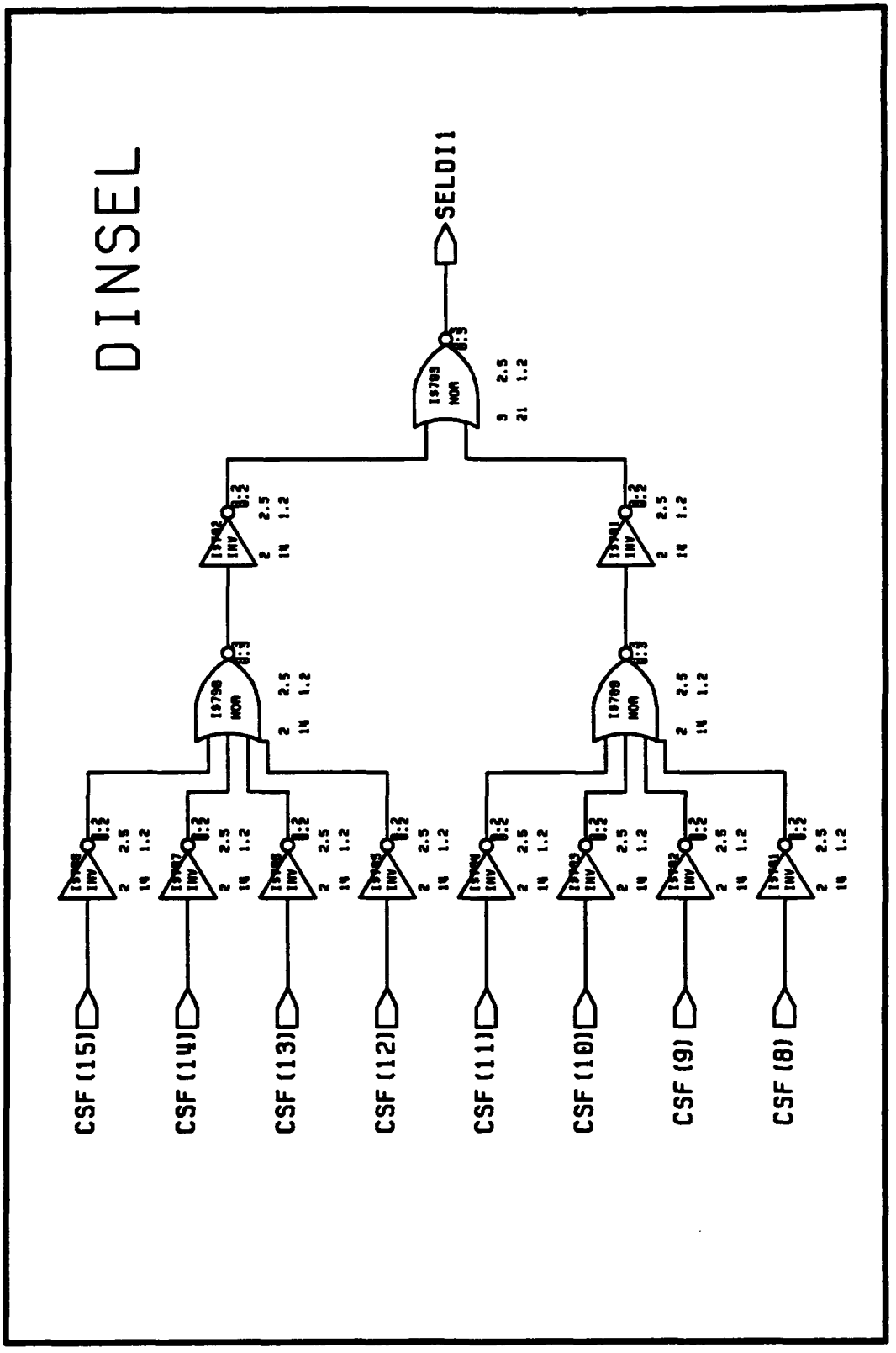

UXX
CSFGEN
CSF (15:0)
BNK (1:0)
DNS (2:0)
MODE (1:0)
DEPTH

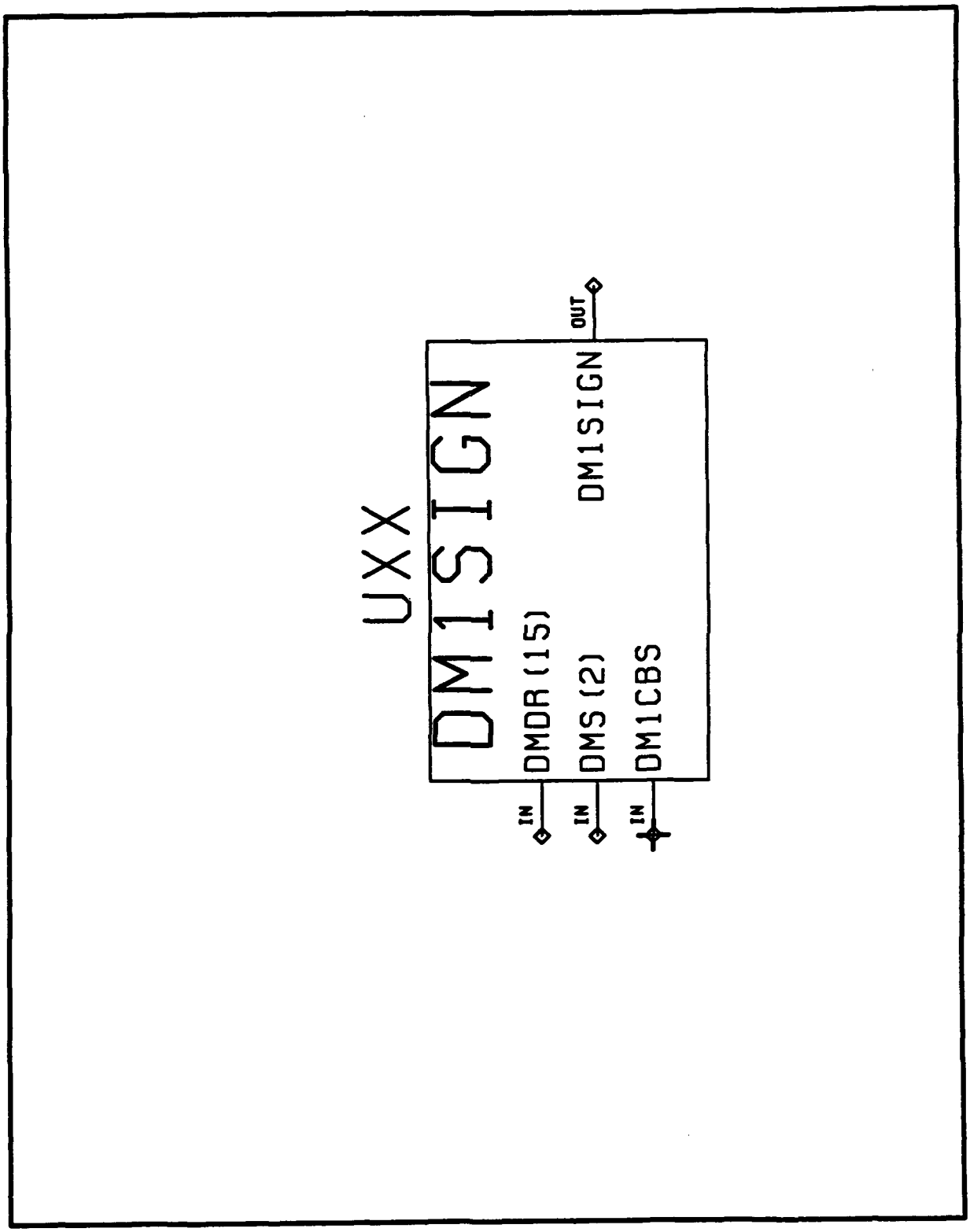

CSFGEN

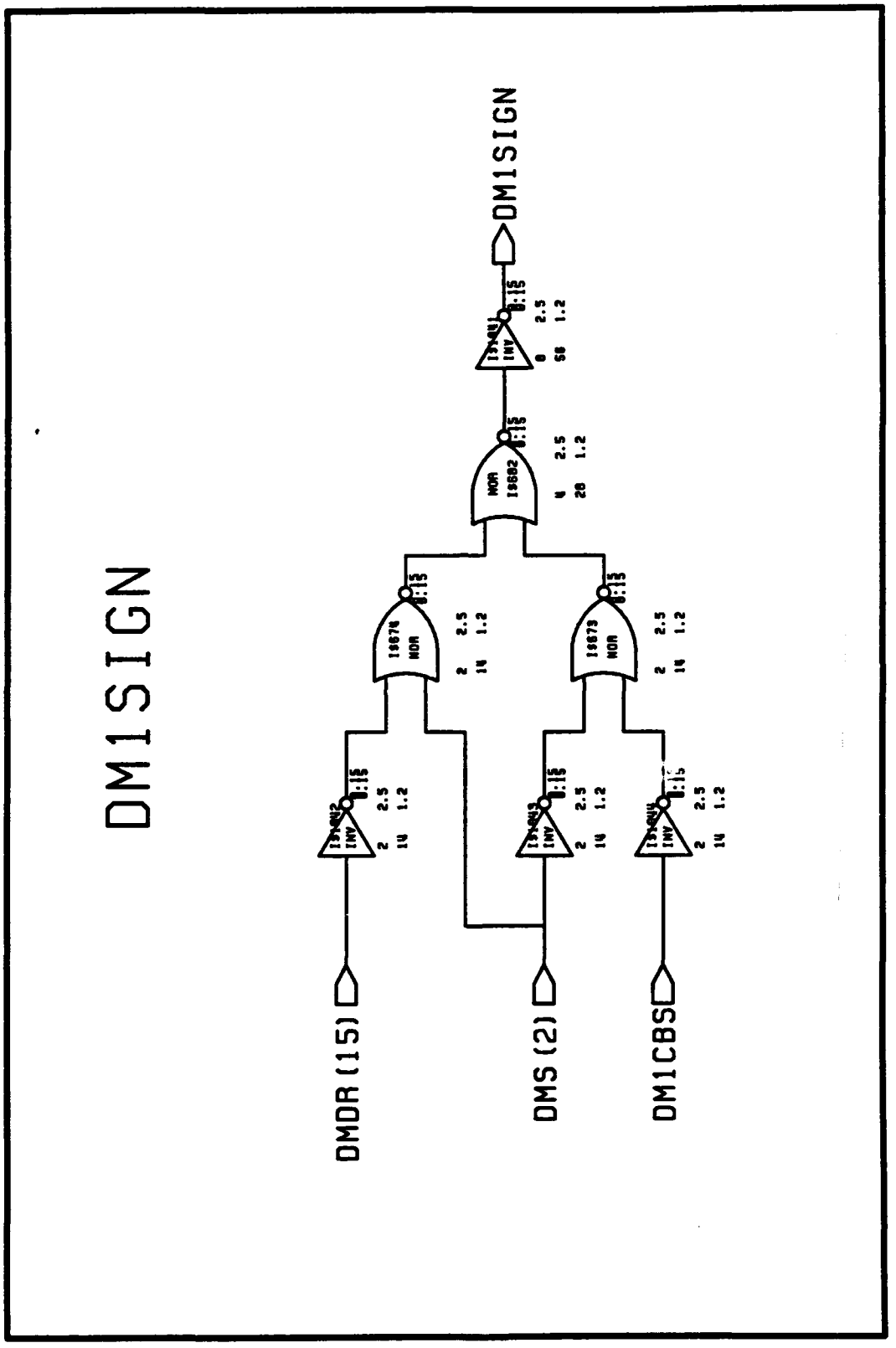

UXX
DECODE
LDDMA
LDDMOW
LDDMOR
LDLAA
EDCOFF
CLREDC
CLR1
CLR2
DMS(2:0)
WRSTALL
ALULD
OBDI(1:0)
ABDI(1:0)
DMFI(1:0)
EDCONI(3:0)
BUSYI
DMSI(2:0)
STALLI(1:0)
CLK
INITI

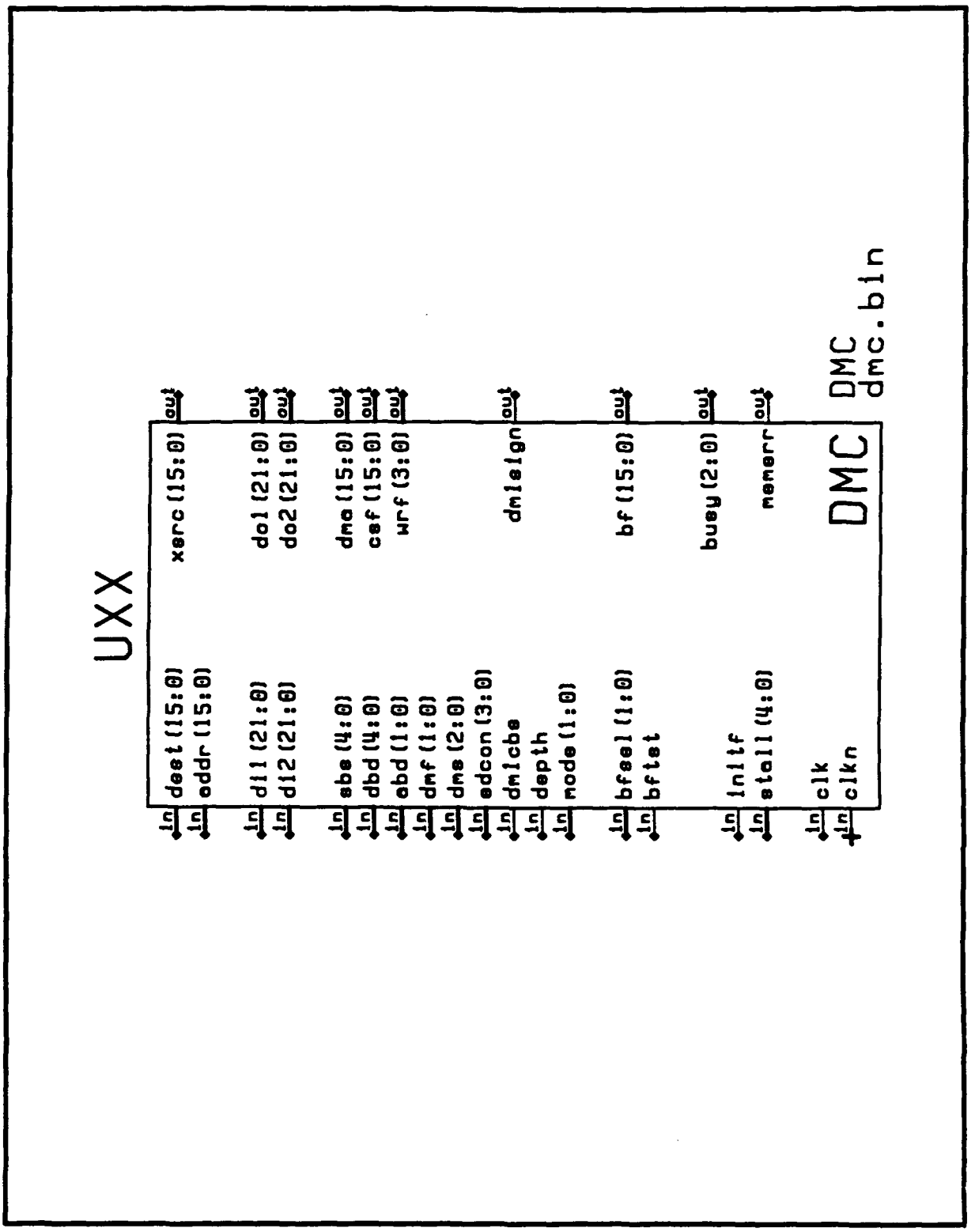

DECODE

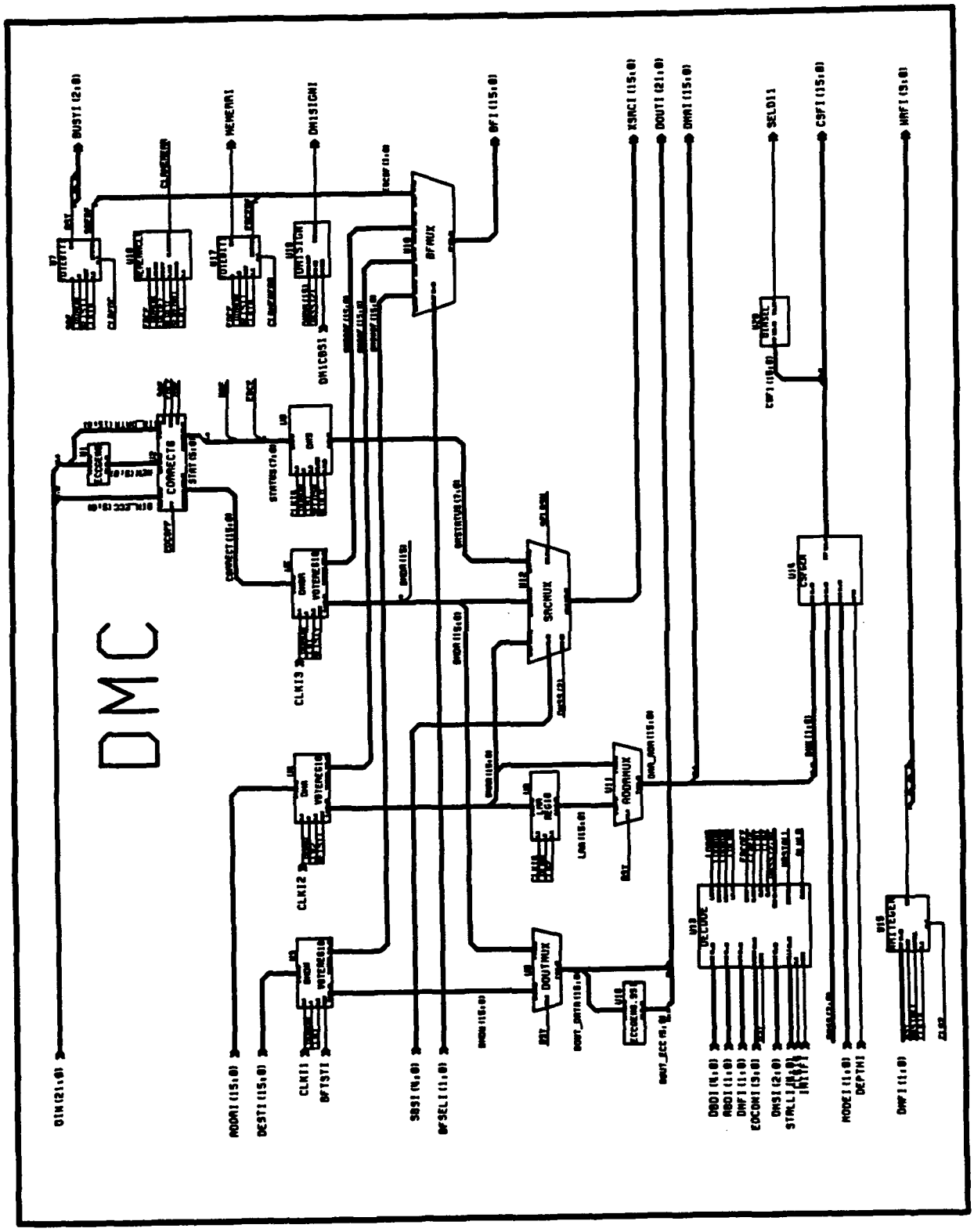

UXX
DINSEL
CSF(15:8)
SELDI1
OUT
IN

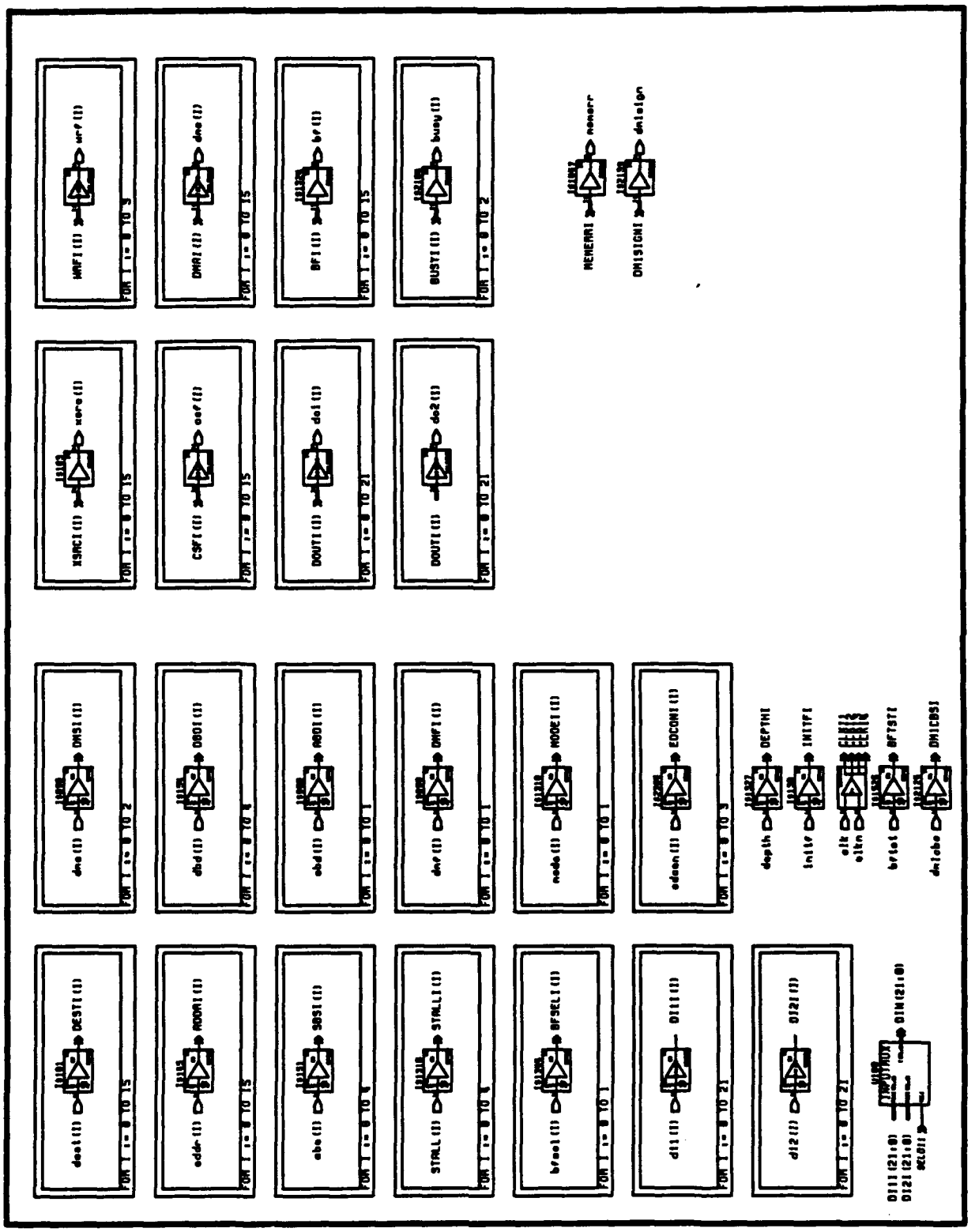

DINSEL
SELDI1
CSF (15)
CSF (14)
CSF (13)
CSF (12)
CSF (11)
CSF (10)
CSF (9)
CSF (8)

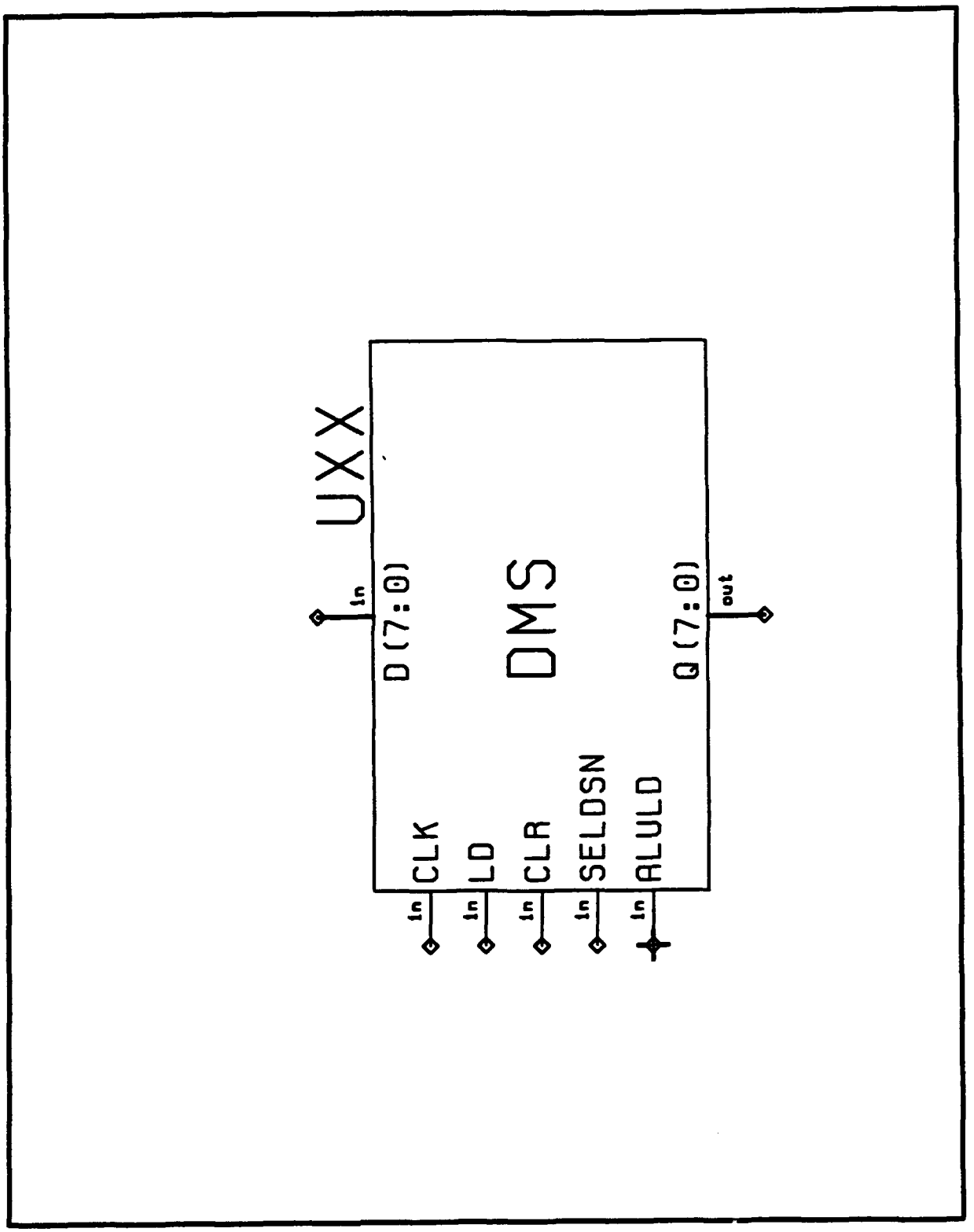

UXX
DM1SIGN
DMDR(15)
DMS(2)
DM1CBS
DM1SIGN
OUT
IN
IN
IN

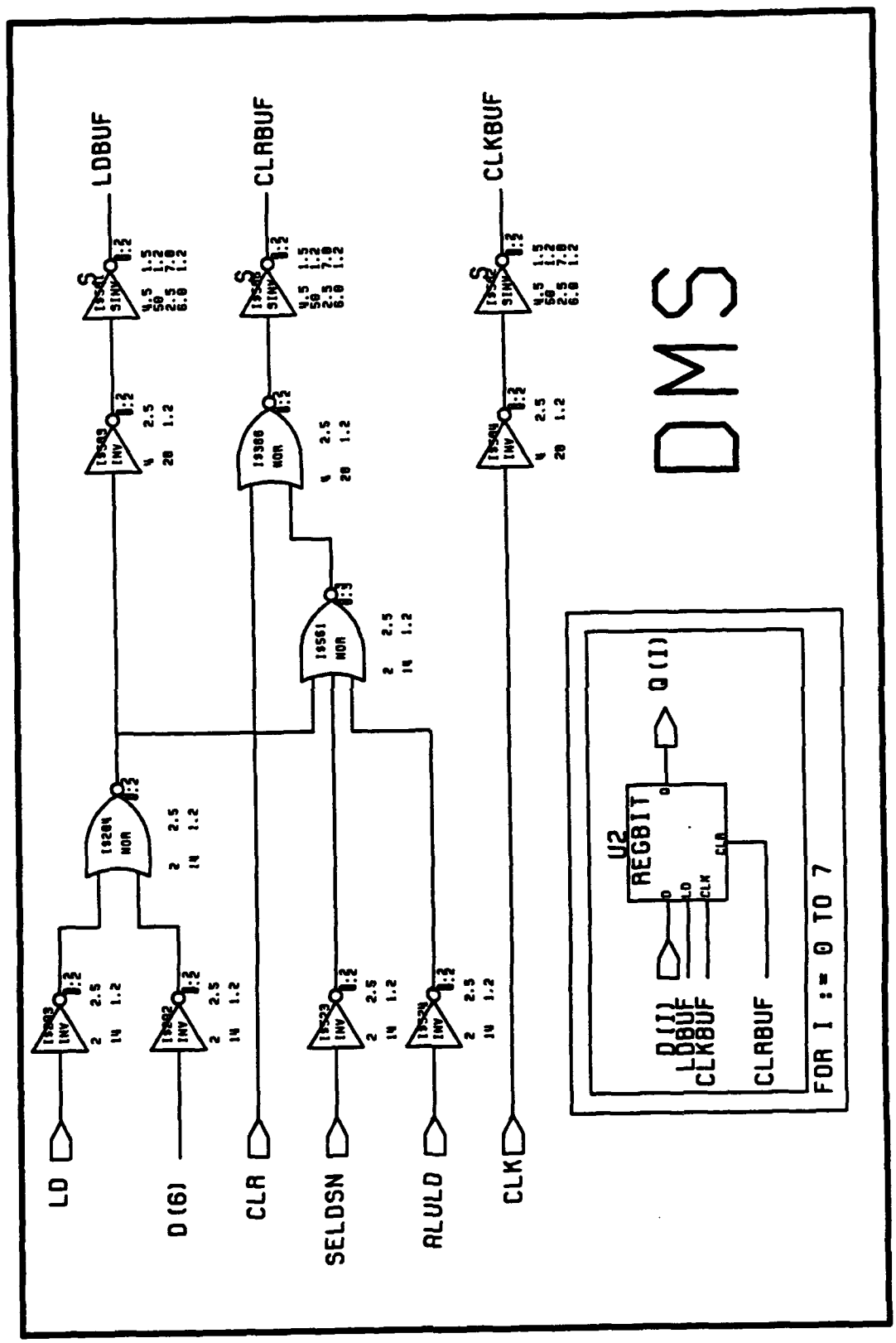

DM1SIGN
DM1SIGN
DMDR(15)
DMS(2)
DM1CBS

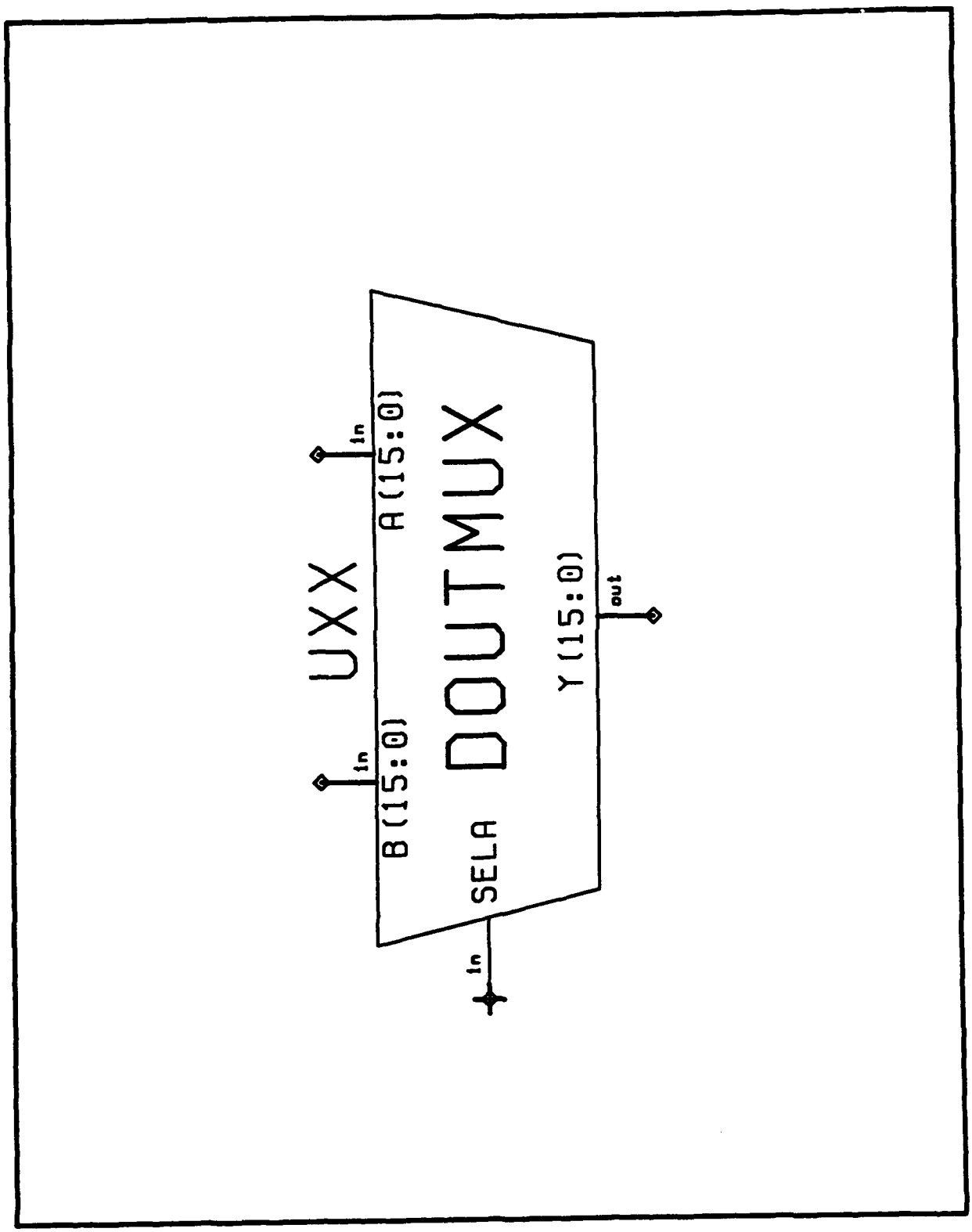

UXX
DMC
dmc.bin
dest(15:0)
addr(15:0)
d11(21:0)
d12(21:0)
sbs(4:0)
dbd(4:0)
abd(1:0)
dmf(1:0)
dms(2:0)
sdcon(3:0)
dmlcbs
depth
mode(1:0)
bfsel(1:0)
bftst
inlif
stall(4:0)
clk
clkn
xerc(15:0)
do1(21:0)
do2(21:0)
dma(15:0)
csf(15:0)
wrf(3:0)
dmlsign
bf(15:0)
busy(2:0)
memerr
DMC

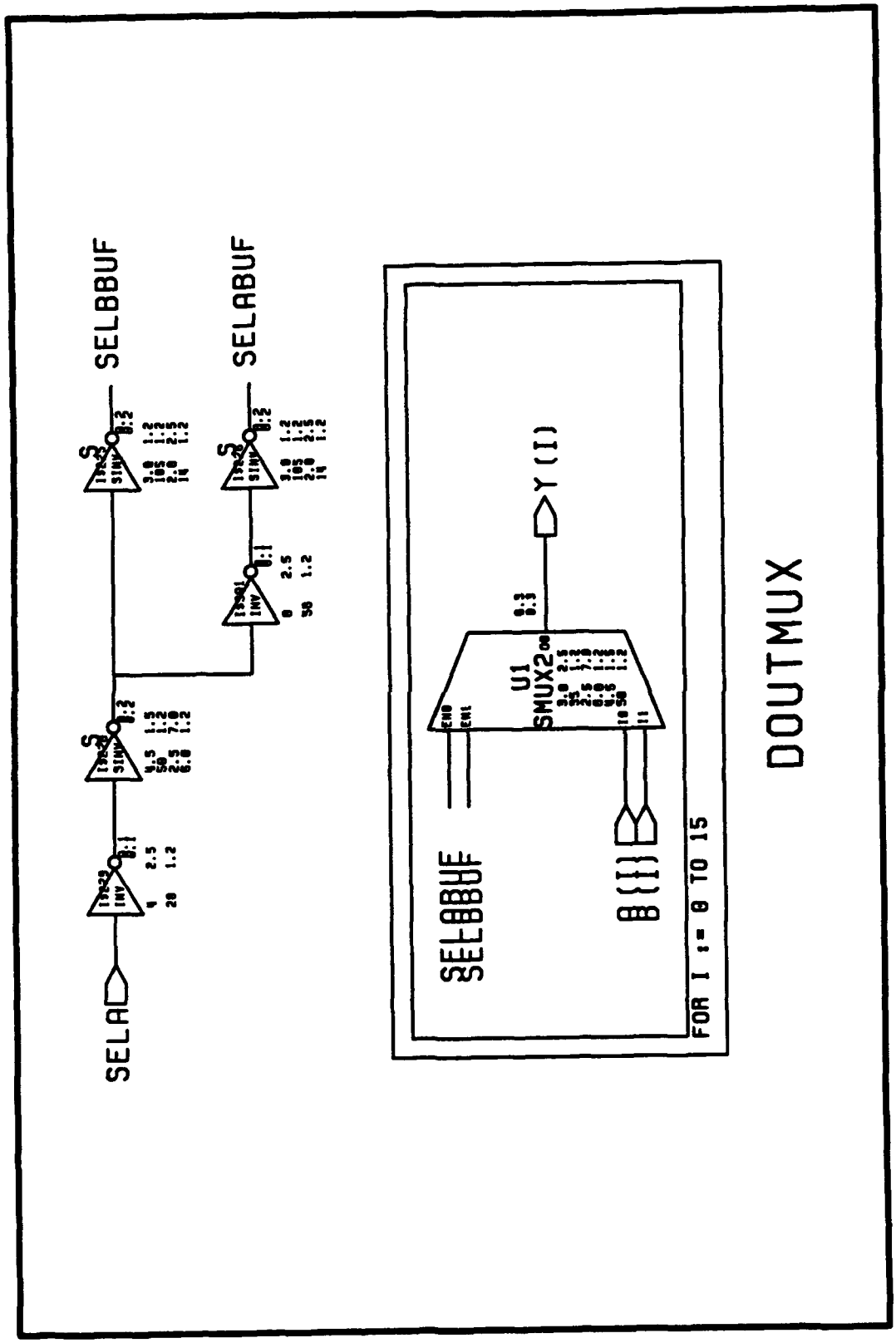

DMC

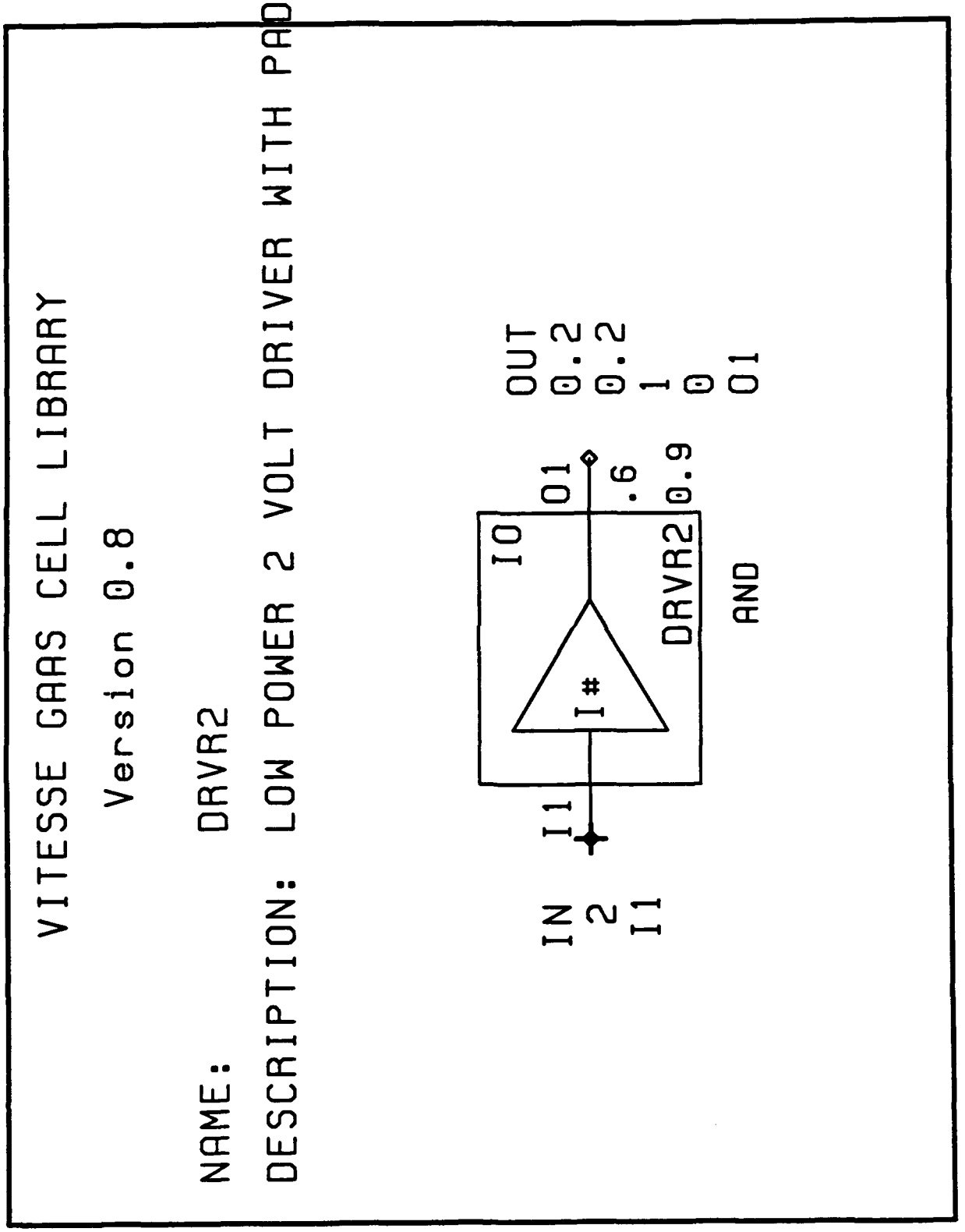


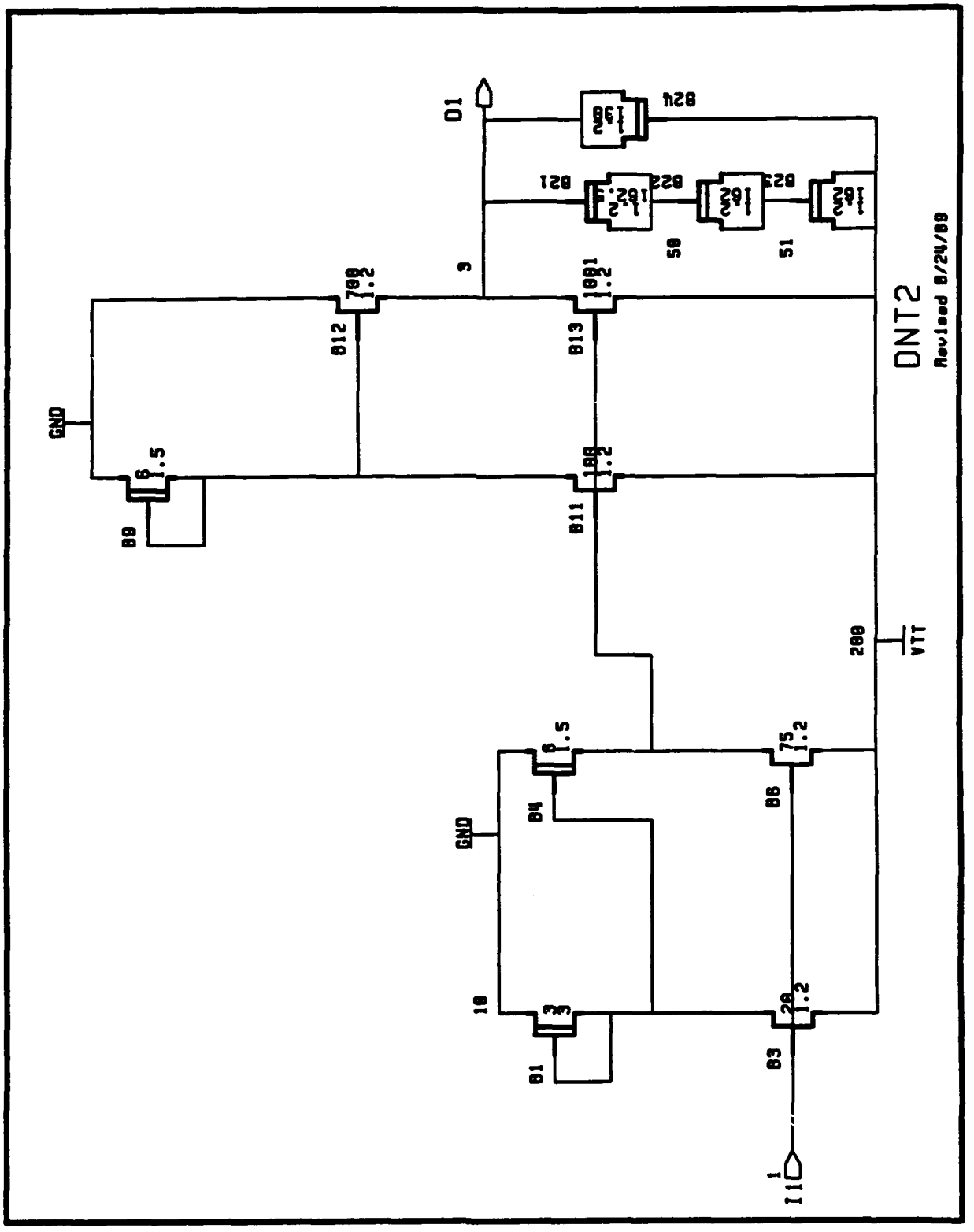

UXX
DMS
D(7:0)
Q(7:0)
in
out
CLK
LD
CLR
SELDSN
ALULD

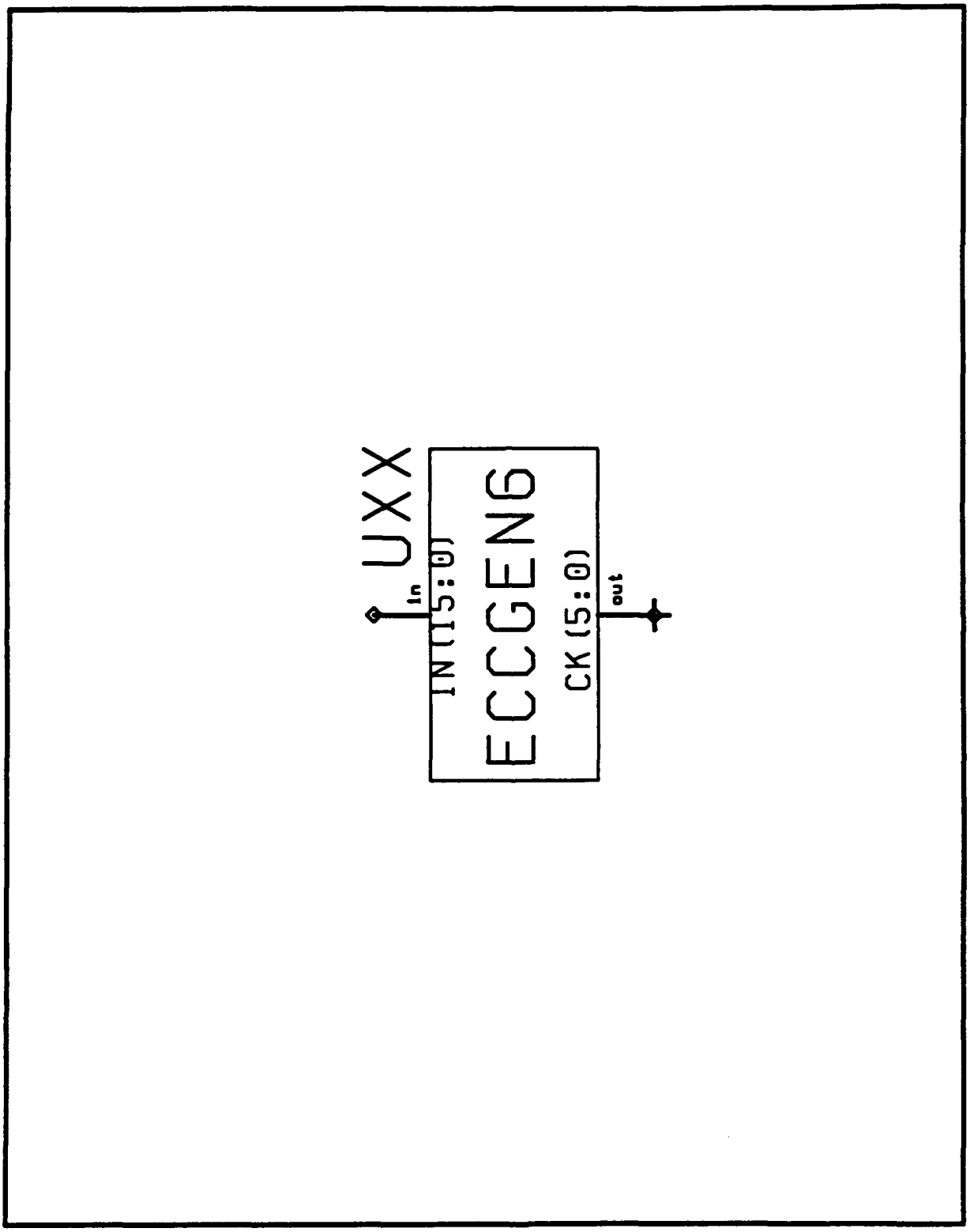

LDBUF
CLRBUF
CLKBUF
DMS
LD
D(6)
CLR
SELDSN
ALULD
CLK
U2
REGBIT
Q(I)
D(I)
LDBUF
CLKBUF
CLRBUF
FOR I := 0 TO 7

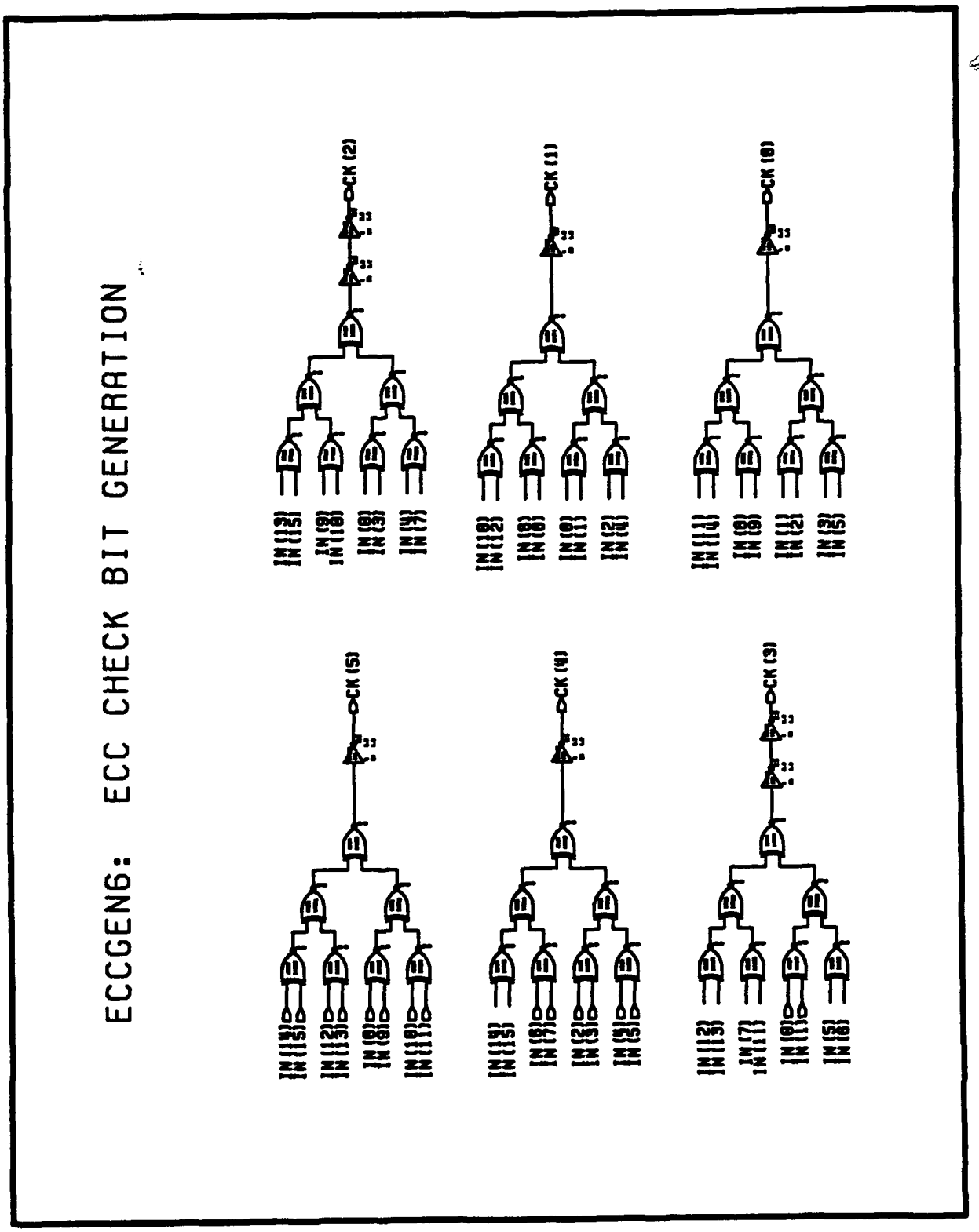

UXX
DOUTMUX
A(15:0)
B(15:0)
SELA
Y(15:0)
in
in
in
out

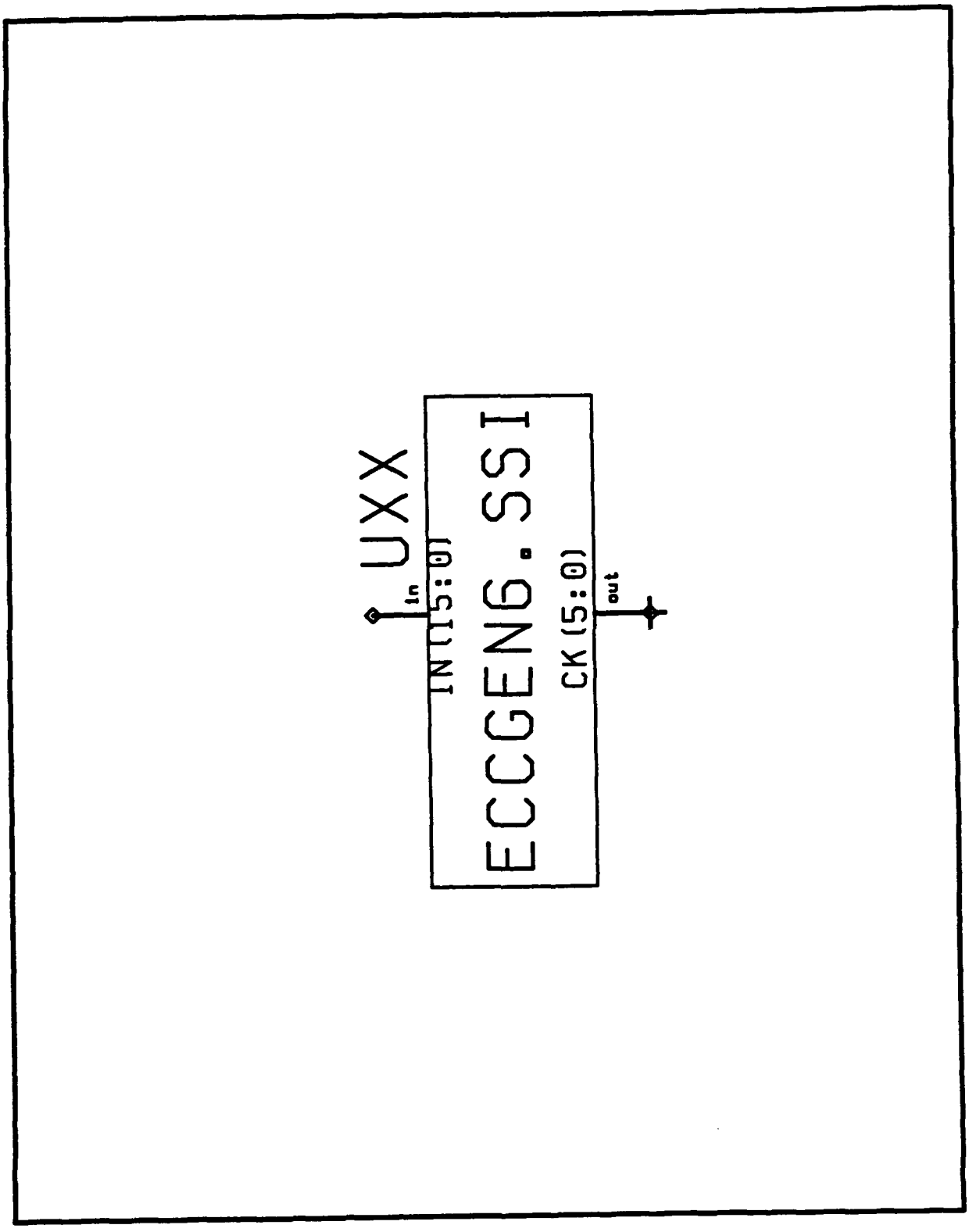

SELBBUF
SELABUF
SELA
U1
SMUX2
Y (I)
SELBBUF
B (I)
FOR I := 0 TO 15
DOUTMUX

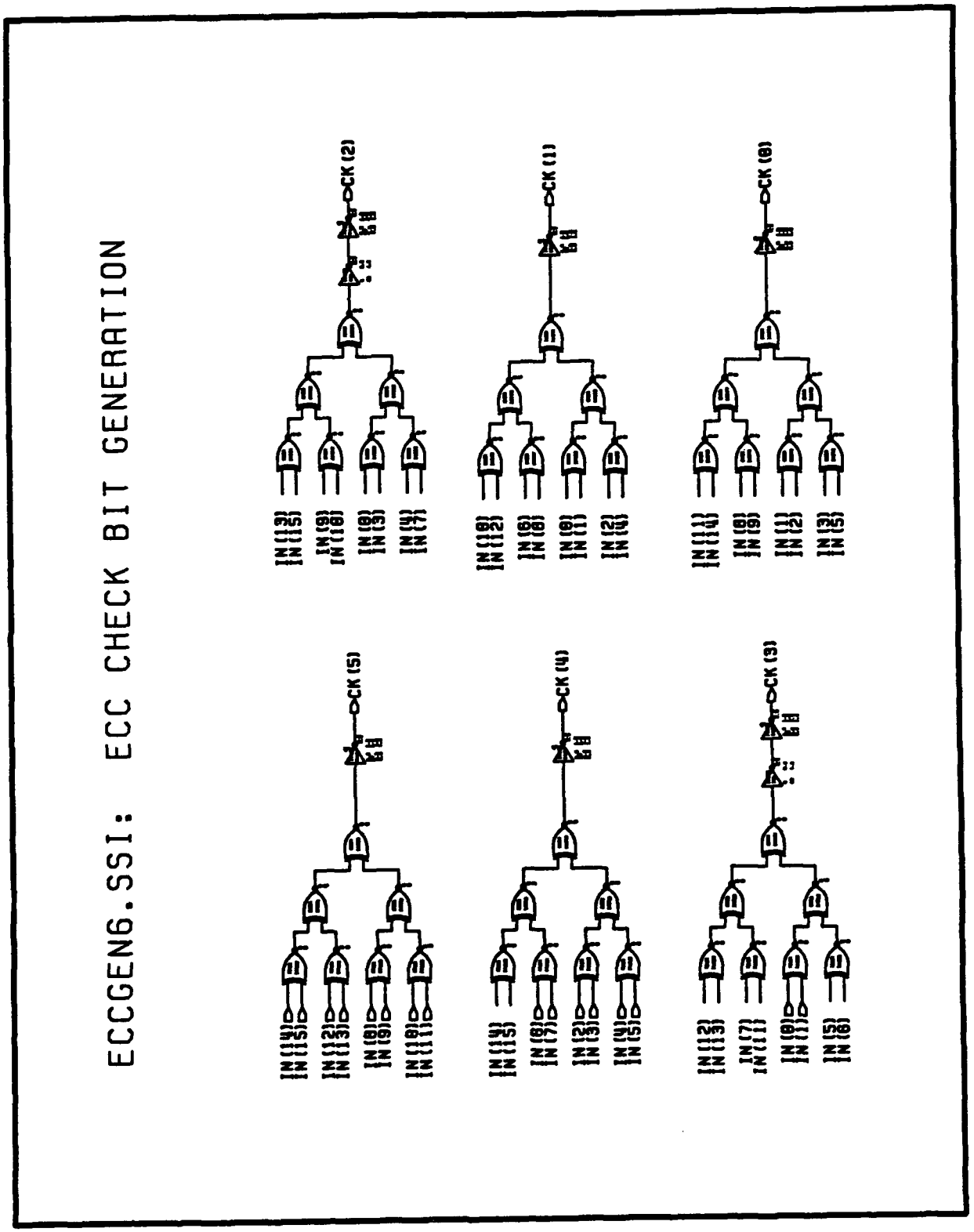

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: DRVR2
DESCRIPTION: LOW POWER 2 VOLT DRIVER WITH PAD
IN
2
I1
I1
IO
O1
I#
OUT
0.2
0.2
1
0
O1
.6
0.9
DRVR2
AND

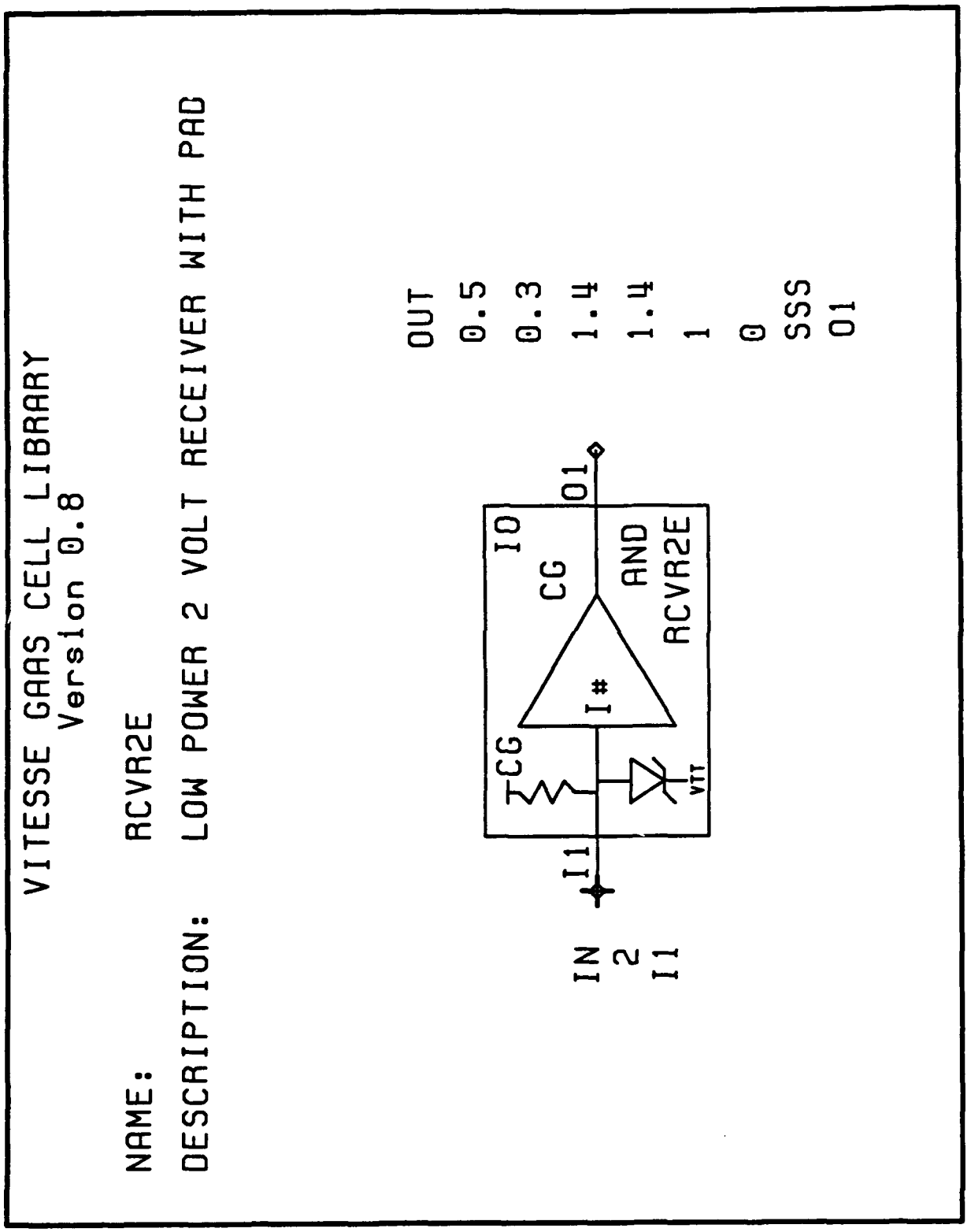

DNT2
Revised 8/24/89
GND
VTT
B1
B3
B4
B6
B9
B11
B12
B13
B21
B22
B23
B24
50
51
10
11

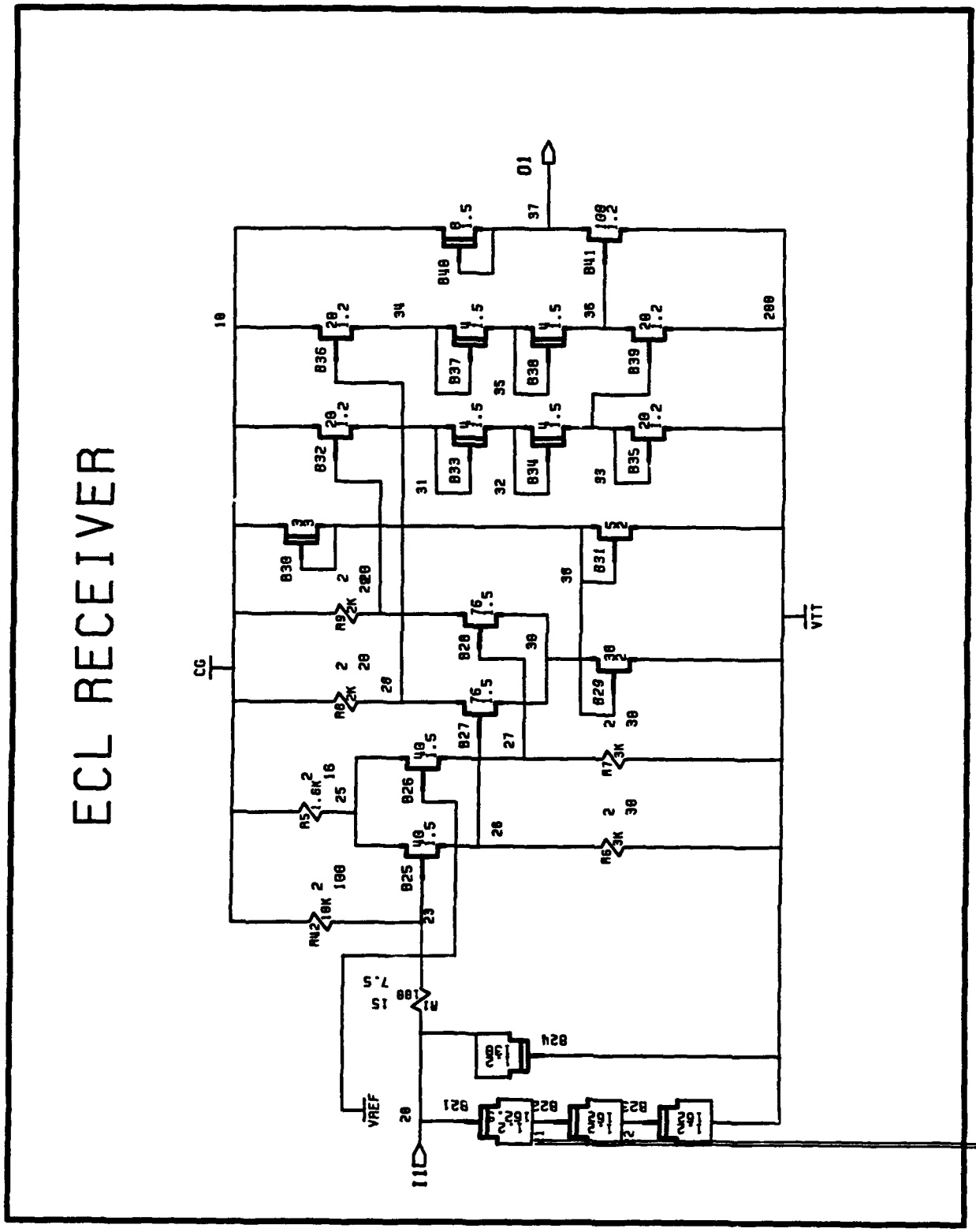

UXX
in
IN[15:0]
ECCGEN6
CK[5:0]
out

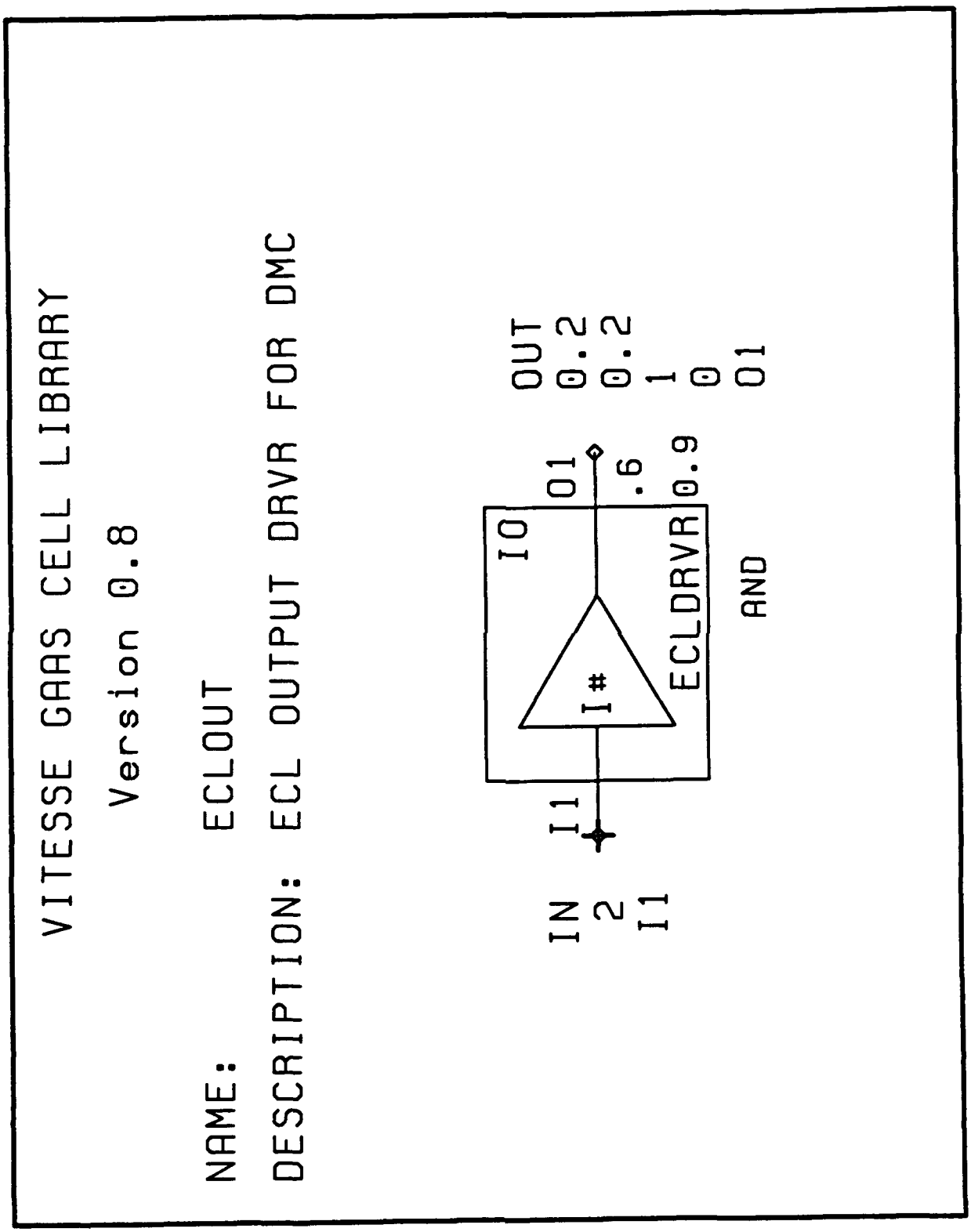

ECCGEN6: ECC CHECK BIT GENERATION
CK(2)
CK(1)
CK(0)
CK(5)
CK(4)
CK(3)

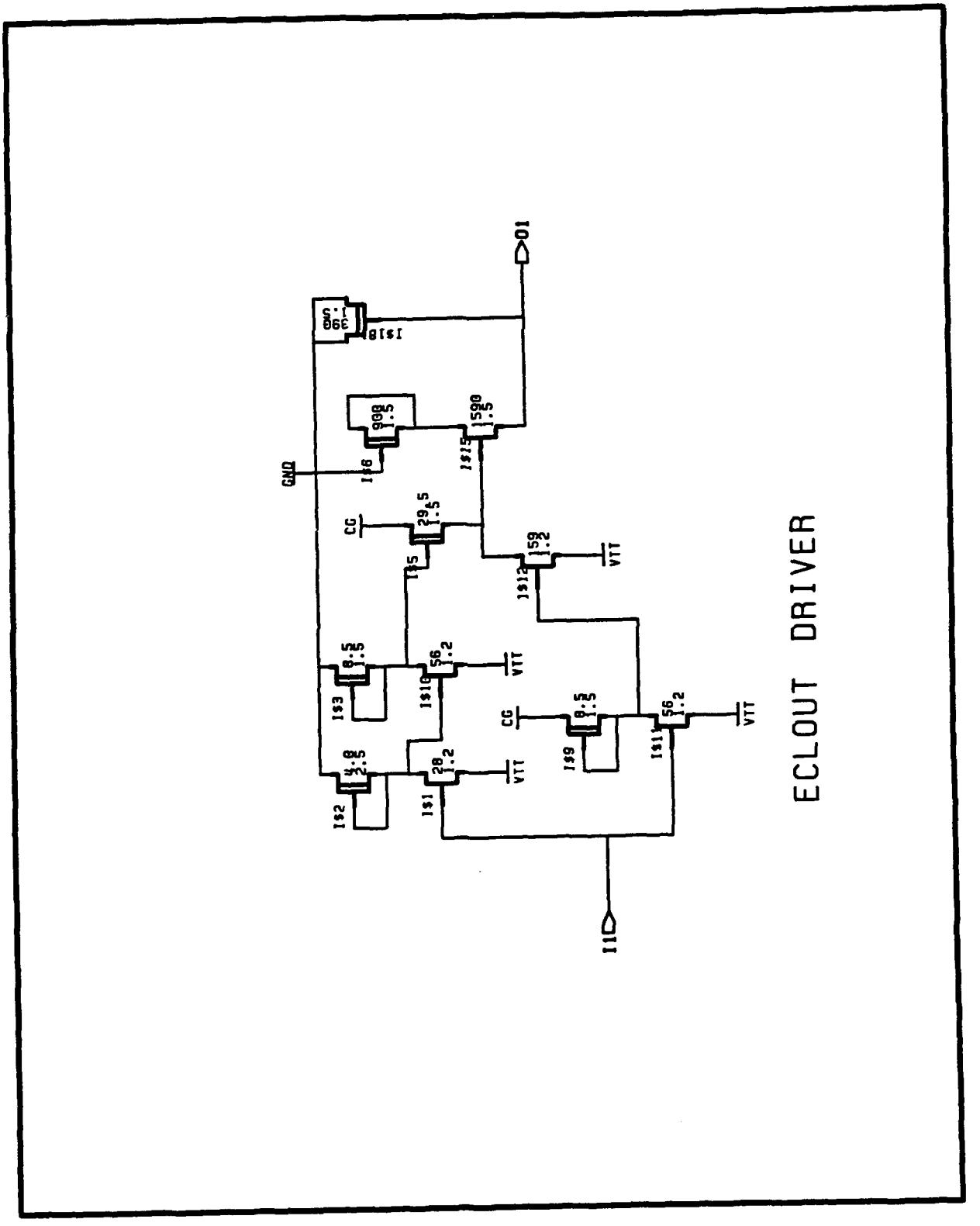

UXX
In
IN(15:0)
ECCGEN6.SSI
CK(5:0)
out

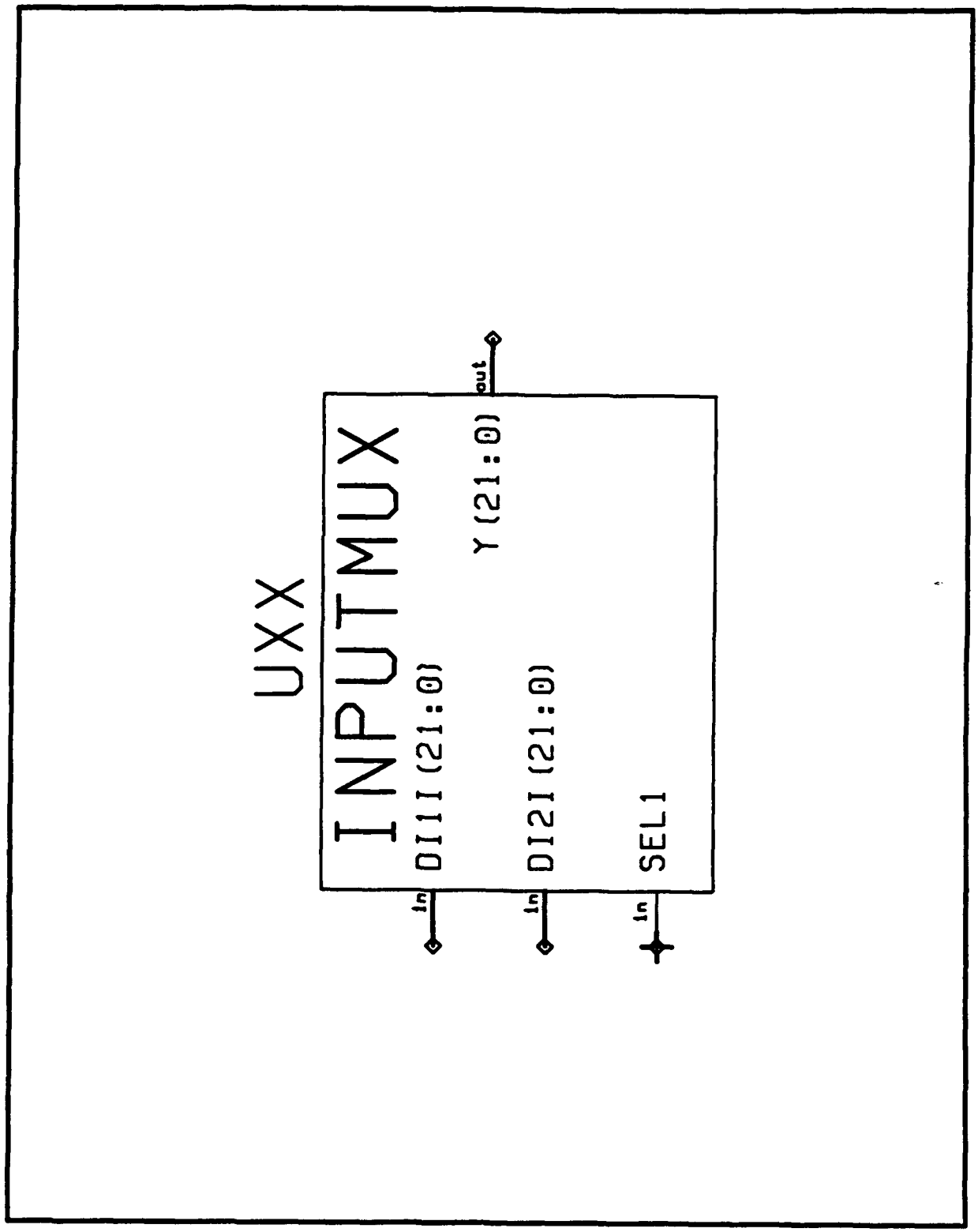

ECCGEN6.SSI: ECC CHECK BIT GENERATION
CK(2)
CK(1)
CK(0)
CK(5)
CK(4)
CK(3)

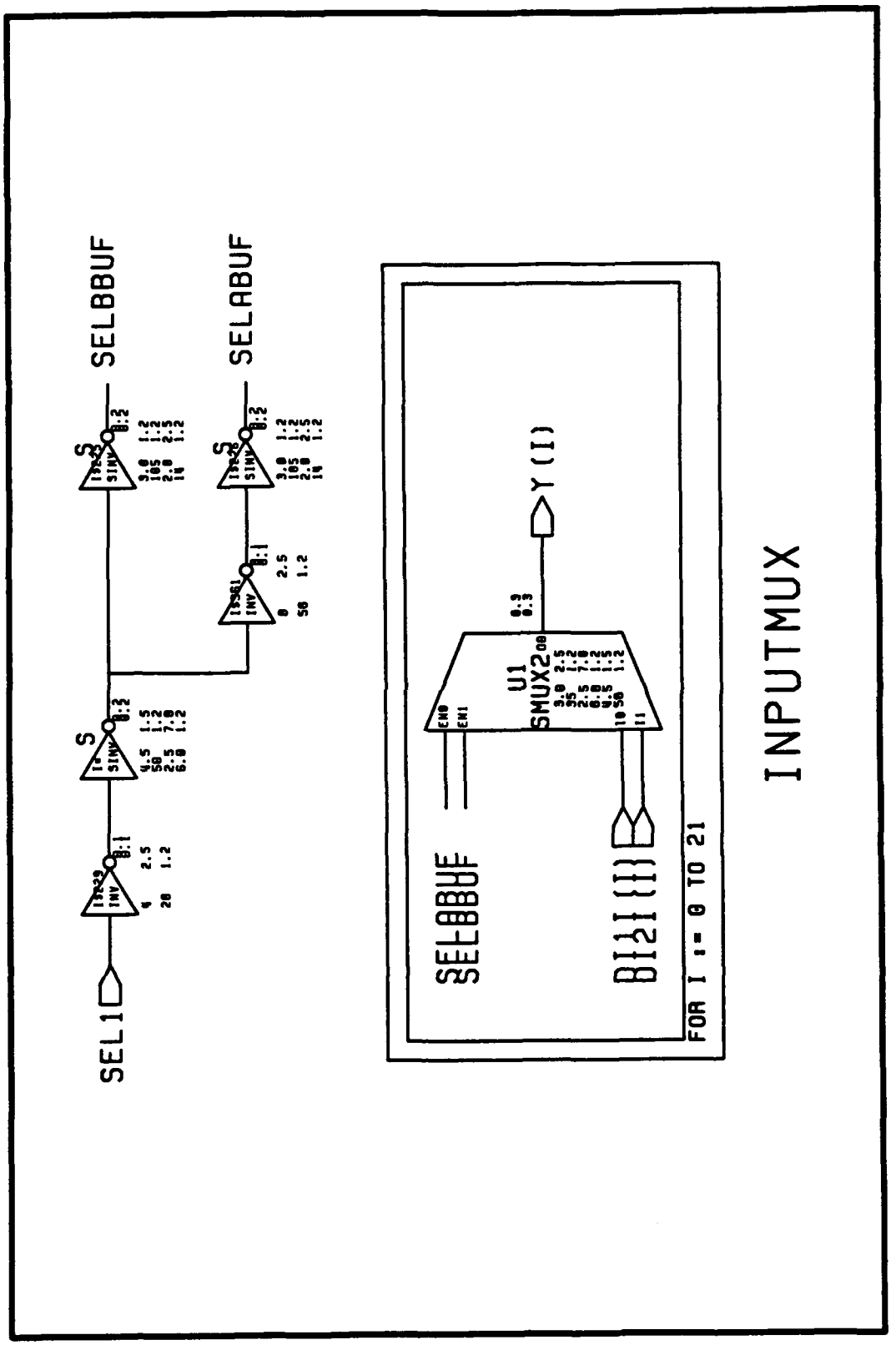

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: RCVR2E
DESCRIPTION: LOW POWER 2 VOLT RECEIVER WITH PAD
OUT
0.5
0.3
1.4
1.4
1
0
SSS
01
IO
CG
AND
RCVR2E
O1
I#
CG
VTT
I1
IN
2
I1

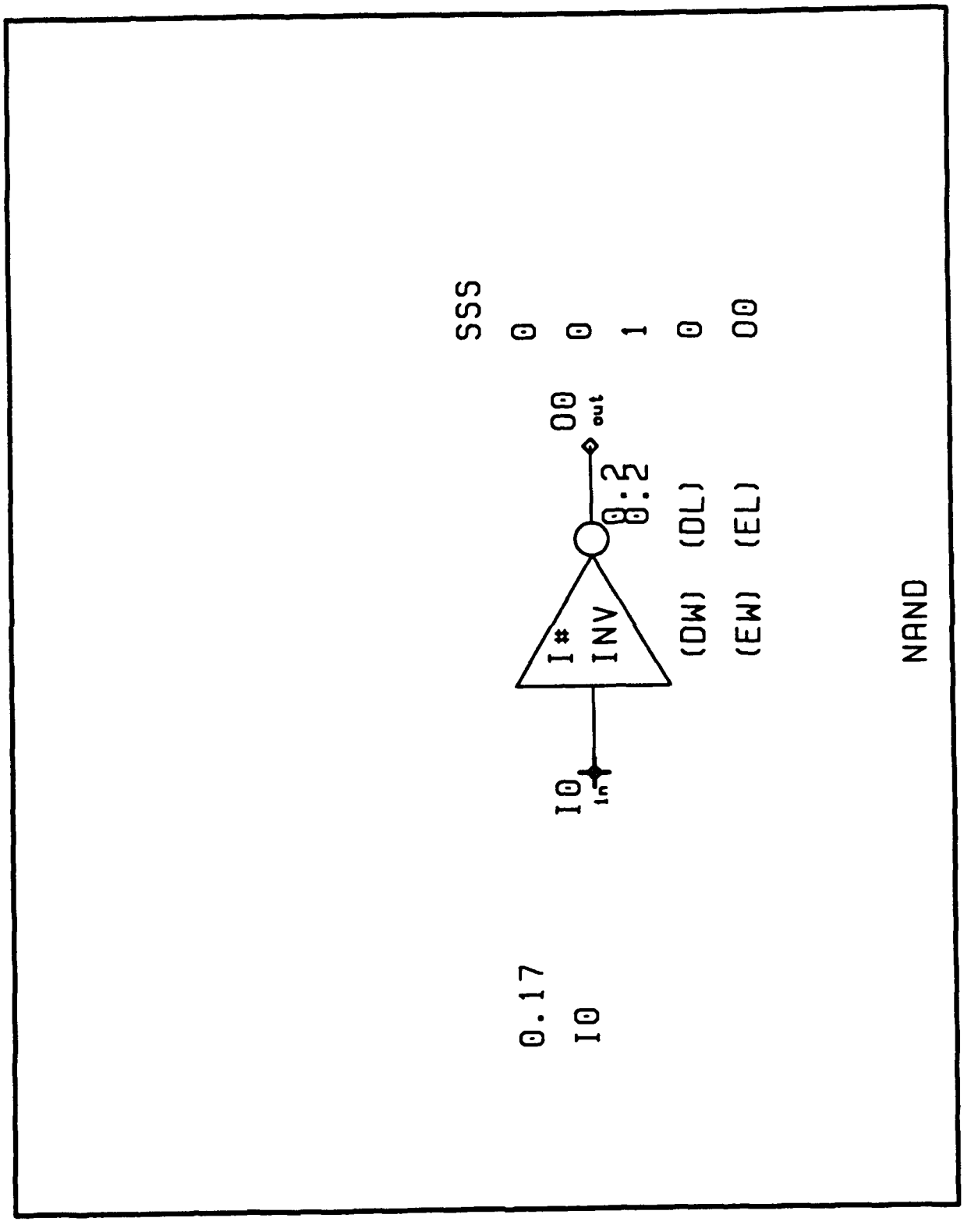

ECL RECEIVER
O1
I1
CG
VTT
VREF

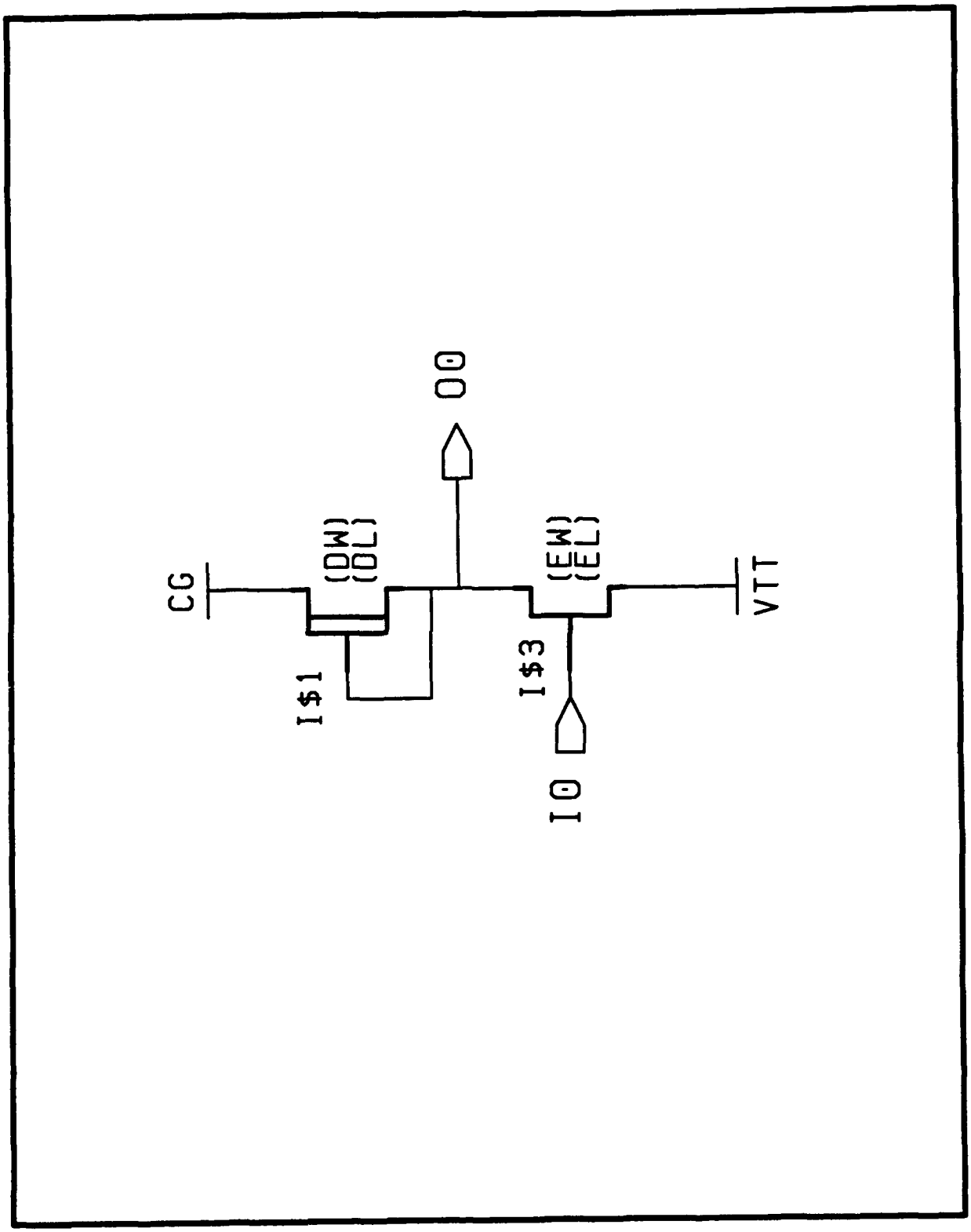

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: ECLOUT
DESCRIPTION: ECL OUTPUT DRVR FOR DMC
IN
2
I1
I1
O1
.6
IO
I#
ECLDRVR
0.9
OUT
0.2
0.2
1
0
O1
AND

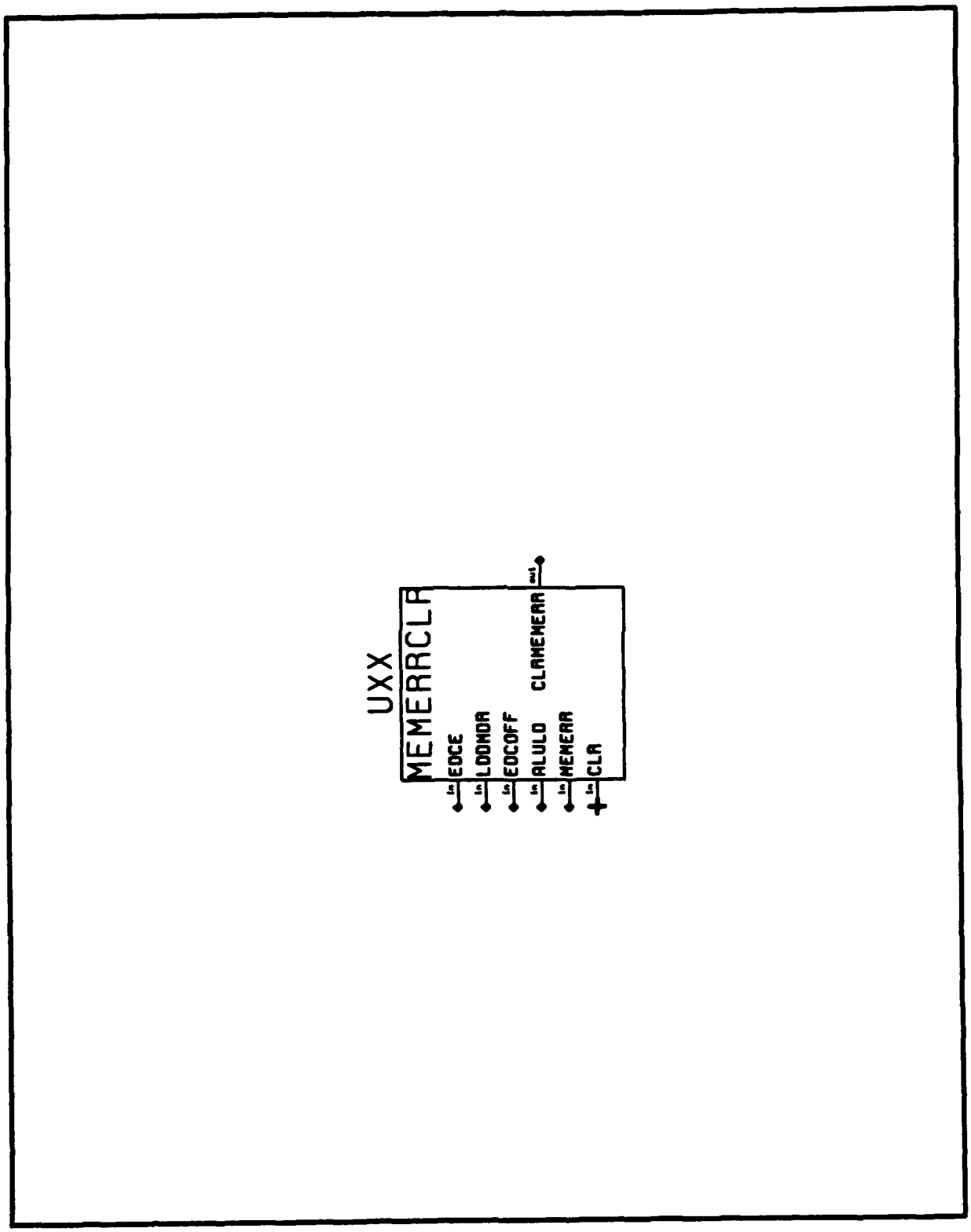

ECLOUT DRIVER
O1
O2
GND
CG
VTT
I$18
I$16
I$15
I$5
I$12
I$3
I$10
I$9
I$11
I$2
I$1

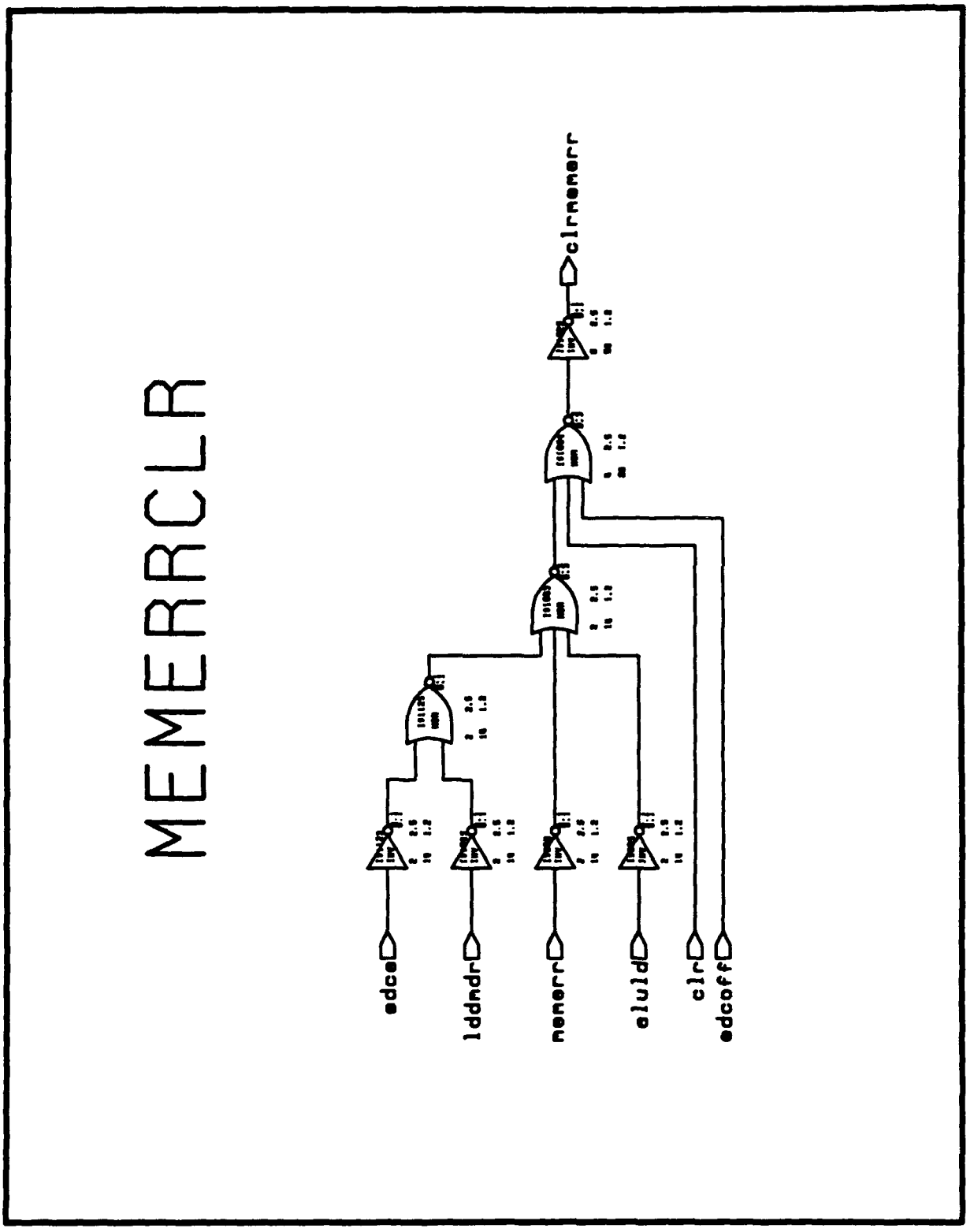

UXX
INPUTMUX
DI1I(21:0)
DI2I(21:0)
SEL1
Y(21:0)
in
in
in
out

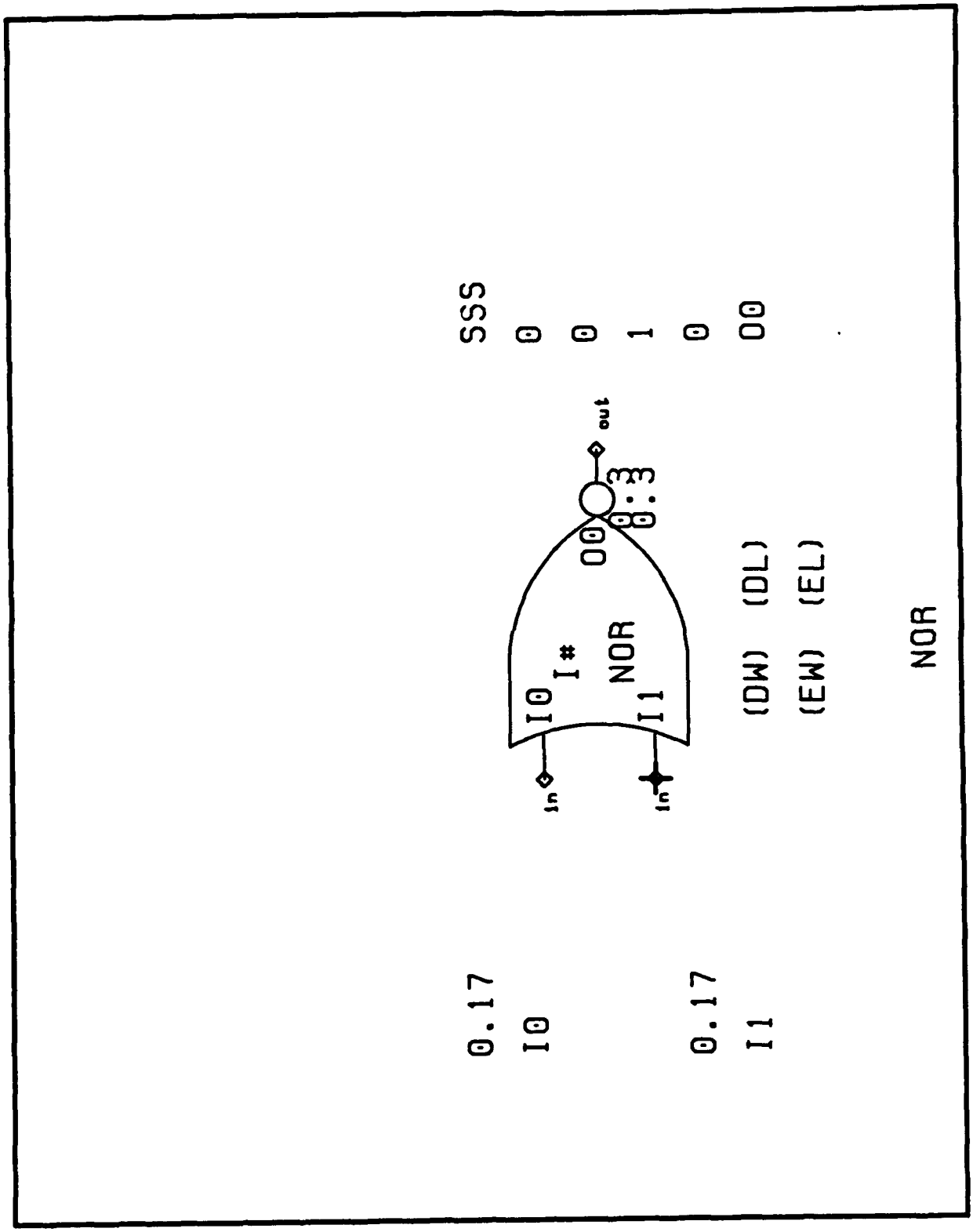

INPUTMUX
SELBBUF
SELABUF
SEL1
Y(1)
U1
SMUX2
SELBBUF
B[21:0]
FOR I := 0 TO 21

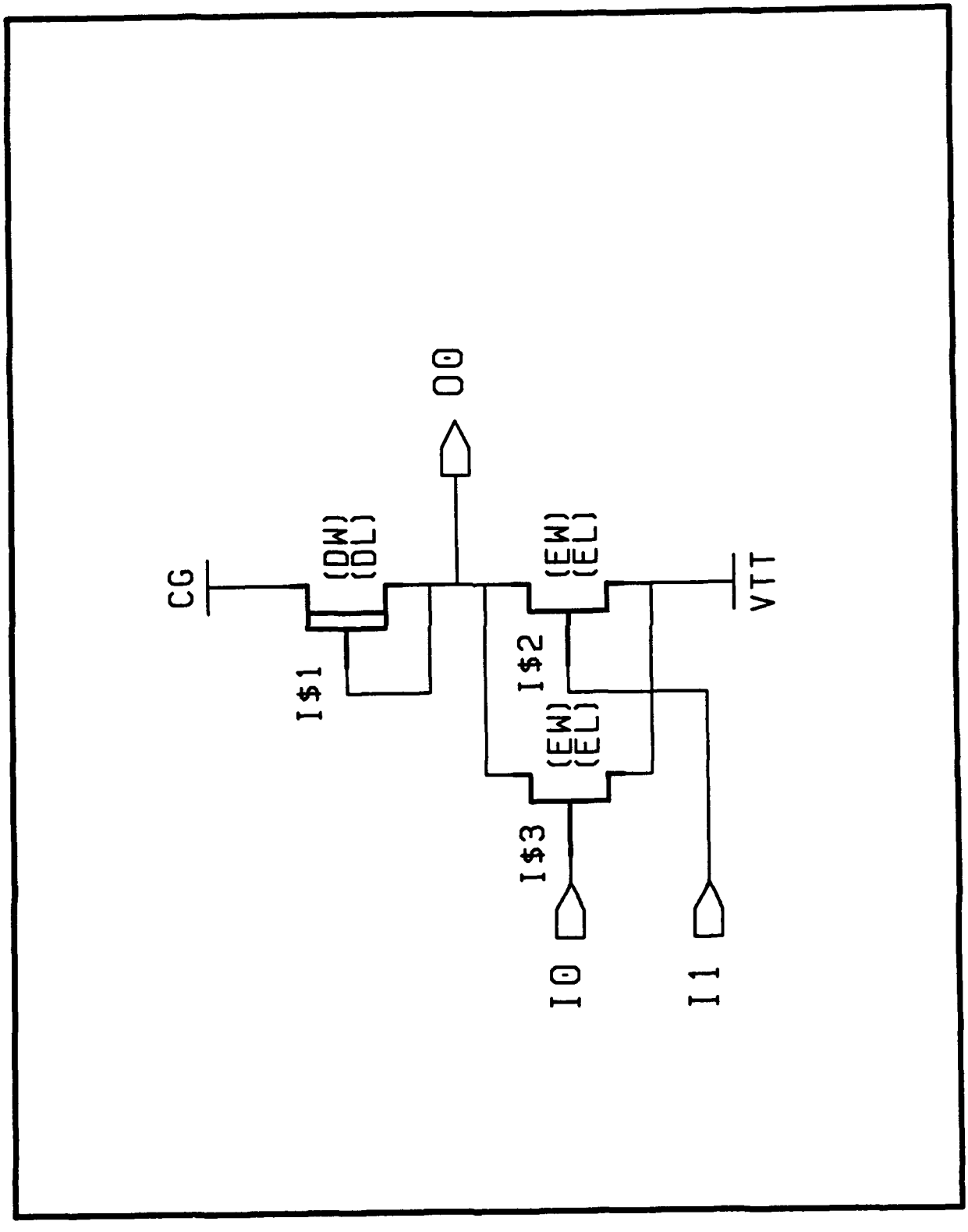

SSS
0 0 1 0 00
00
out
8.2
I#
INV
(OW) (OL)
(EW) (EL)
NAND
I0
in
0.17
I0

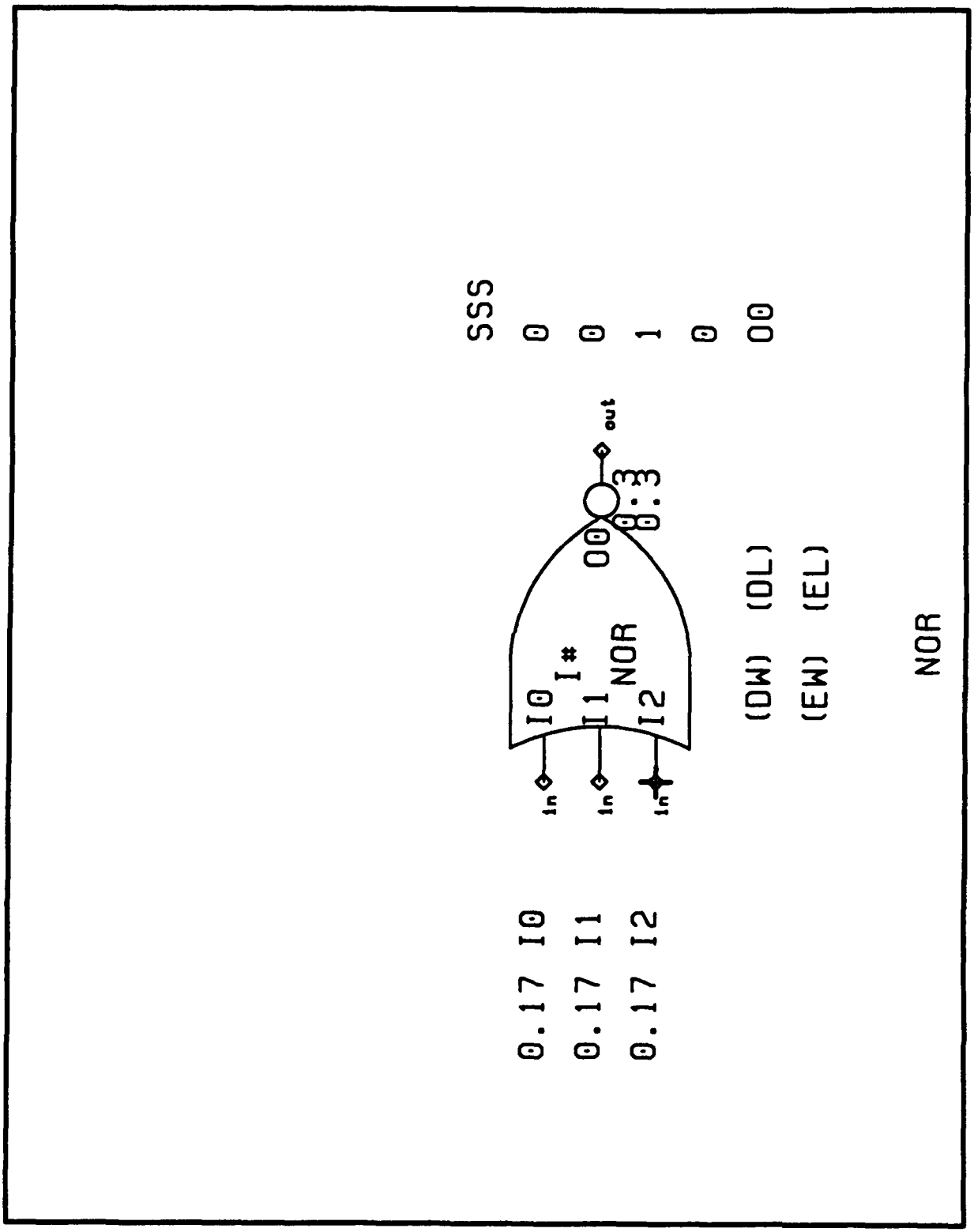

O0
(0W)
(0L)
(EW)
(EL)
CG
VTT
I$1
I$3
IO

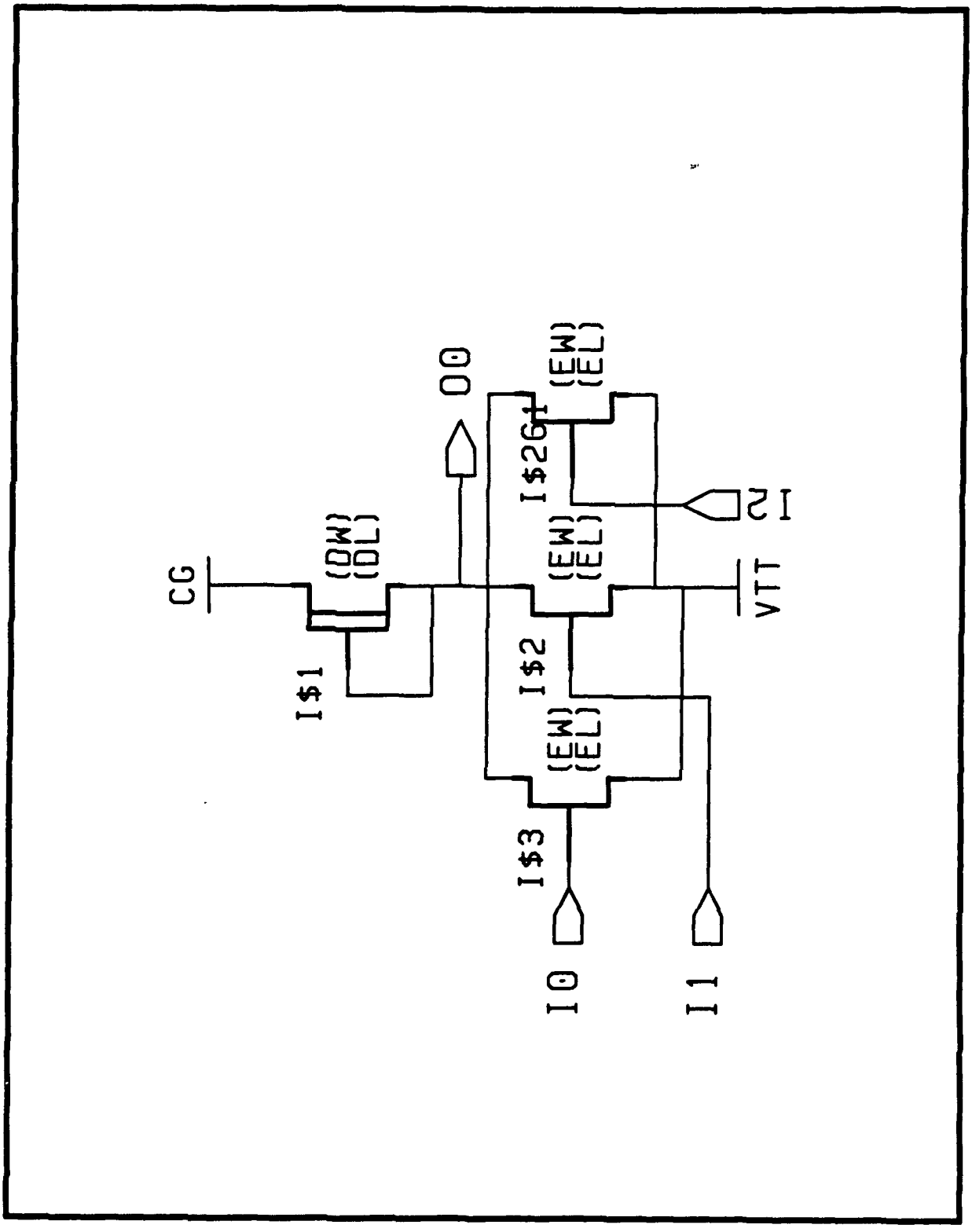

UXX
MEMERRCLR
EDCE
LDDMDA
EDCOFF
ALULO
MEMERR
CLA
CLRMEMERR

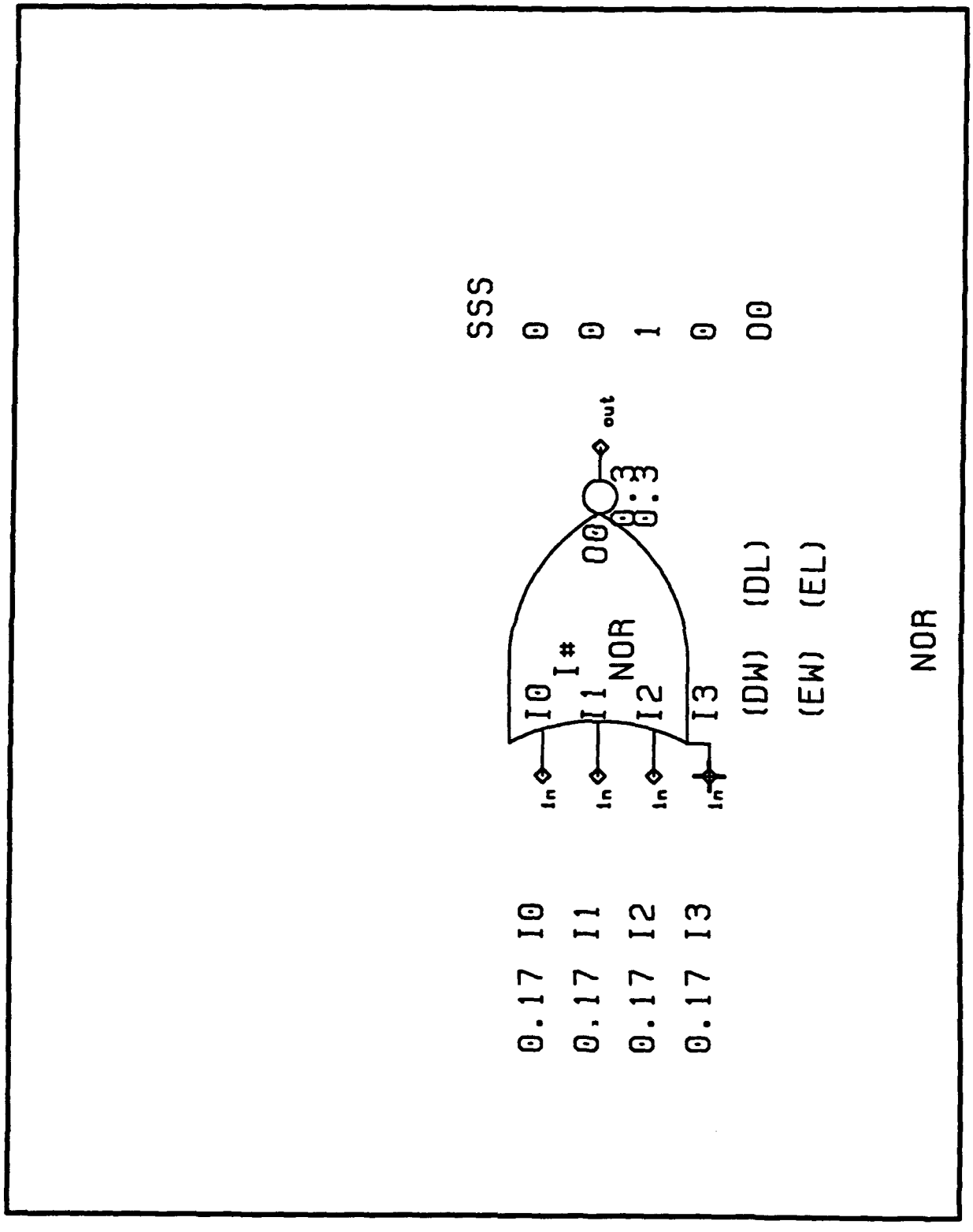

MEMERRCLR
clrmemerr
edce
lddndr
memerr
eluld
clr
edcoff

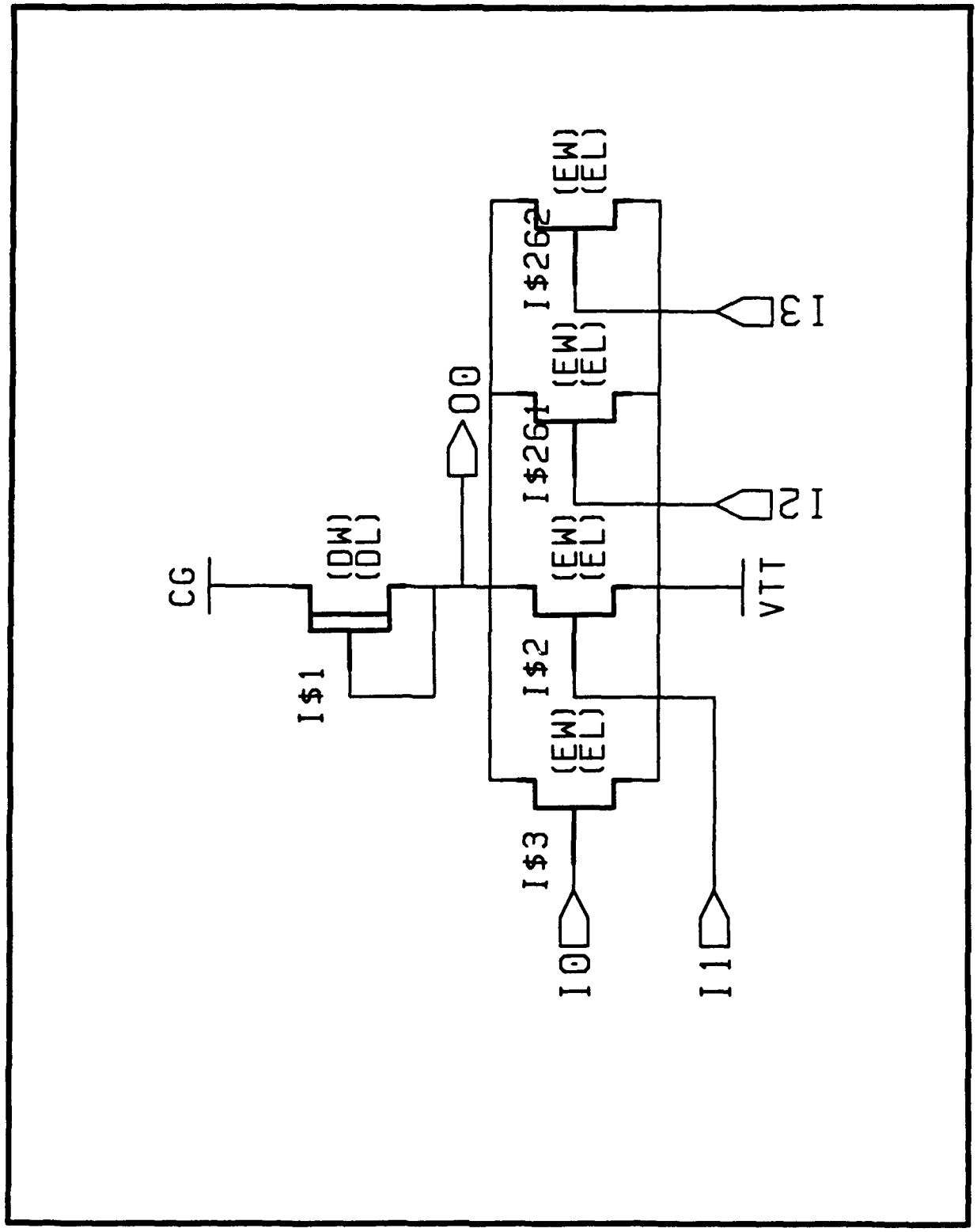

SSS
0
0
1
0
00
out
0.3
0.3
00
I#
NOR
I0
I1
in
in
(DW) (DL)
(EW) (EL)
NOR
0.17
I0
0.17
I1

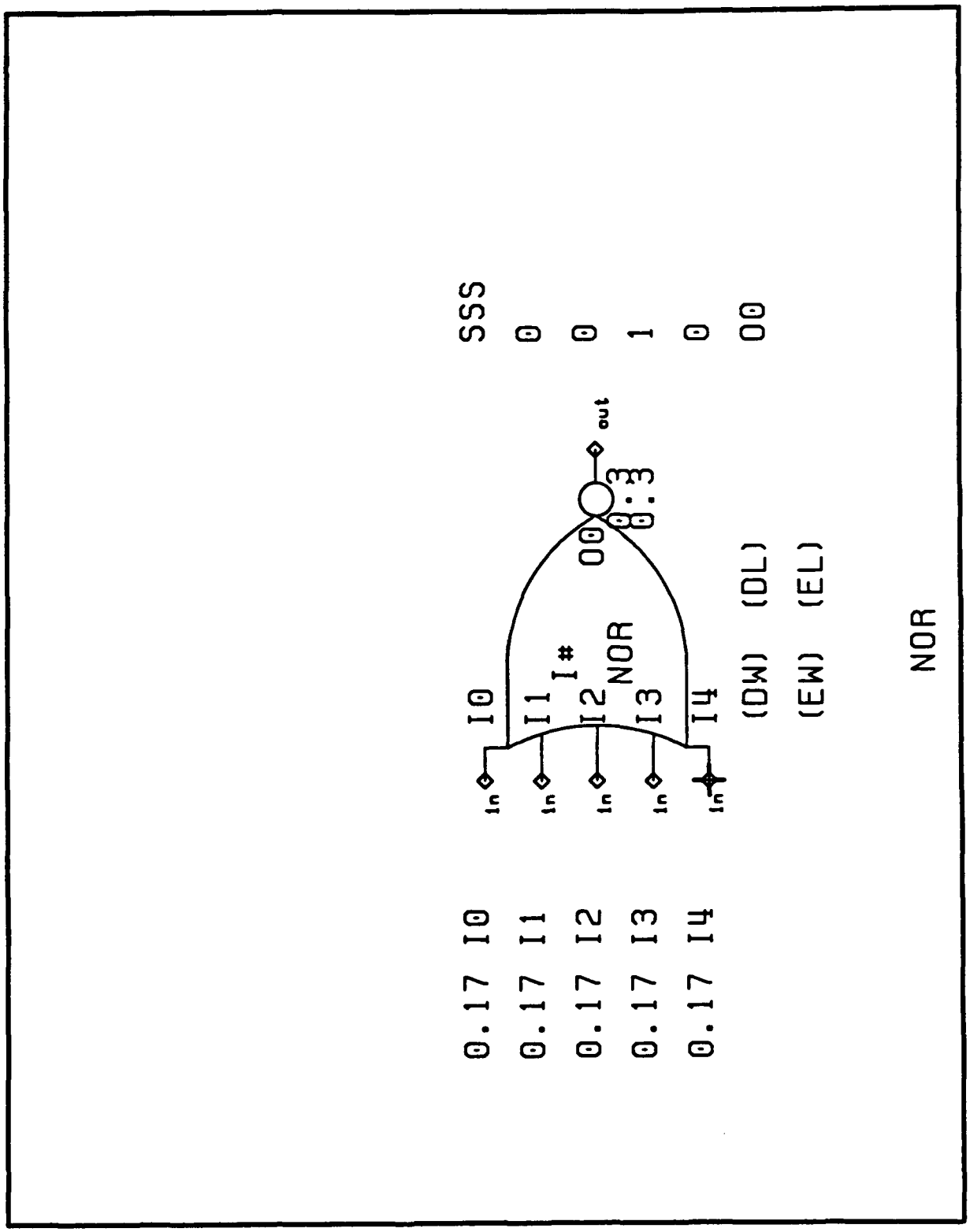

O0
CG
(DW)
(DL)
(EW)
(EL)
VTT
I$1
I$2
(EW)
(EL)
I$3
I0
I1

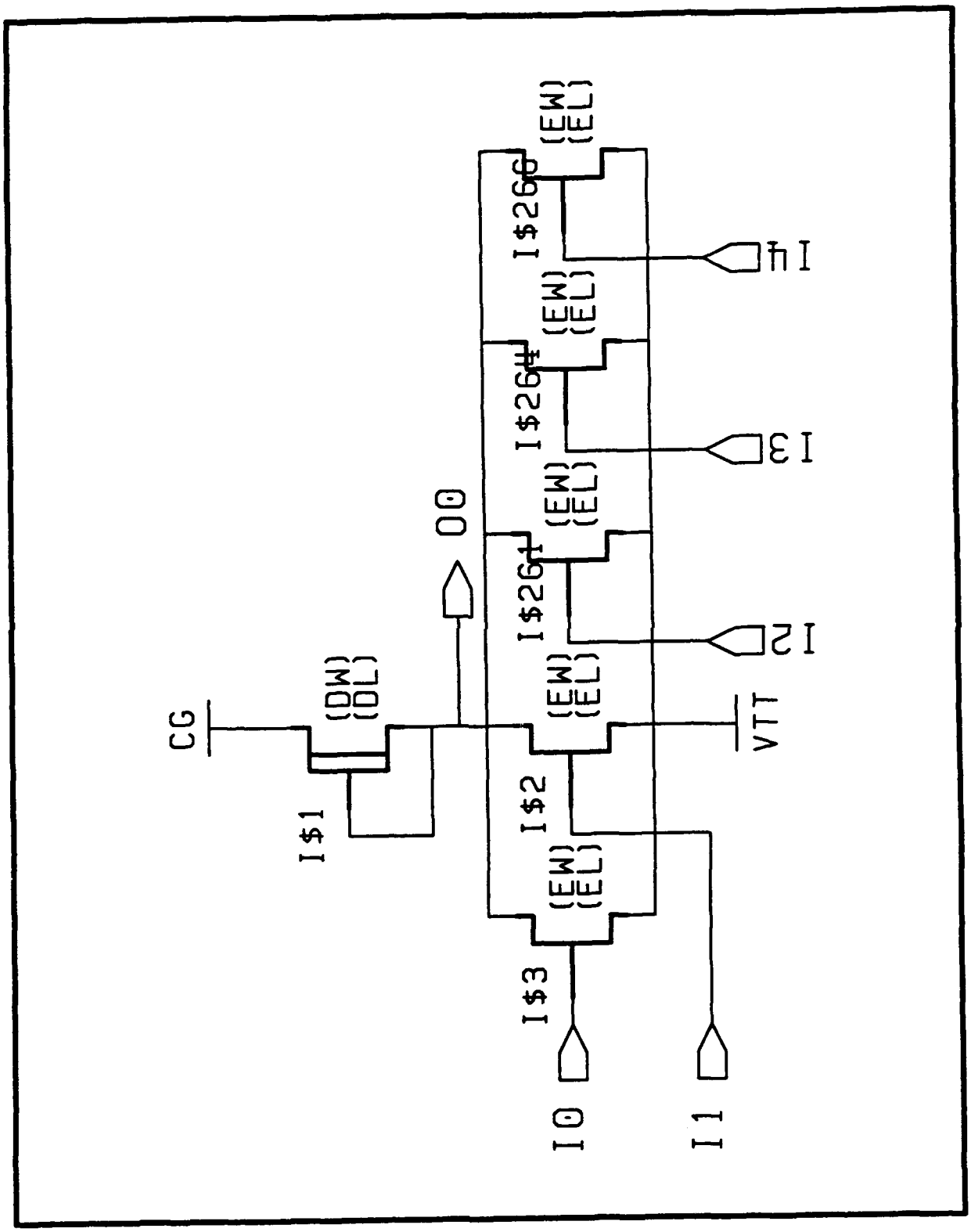

SSS
0
0
1
0
00
out
8:3
00
I0
I#
I1
NOR
I2
In
In
In
(DW) (DL)
(EW) (EL)
NOR
0.17 I0
0.17 I1
0.17 I2

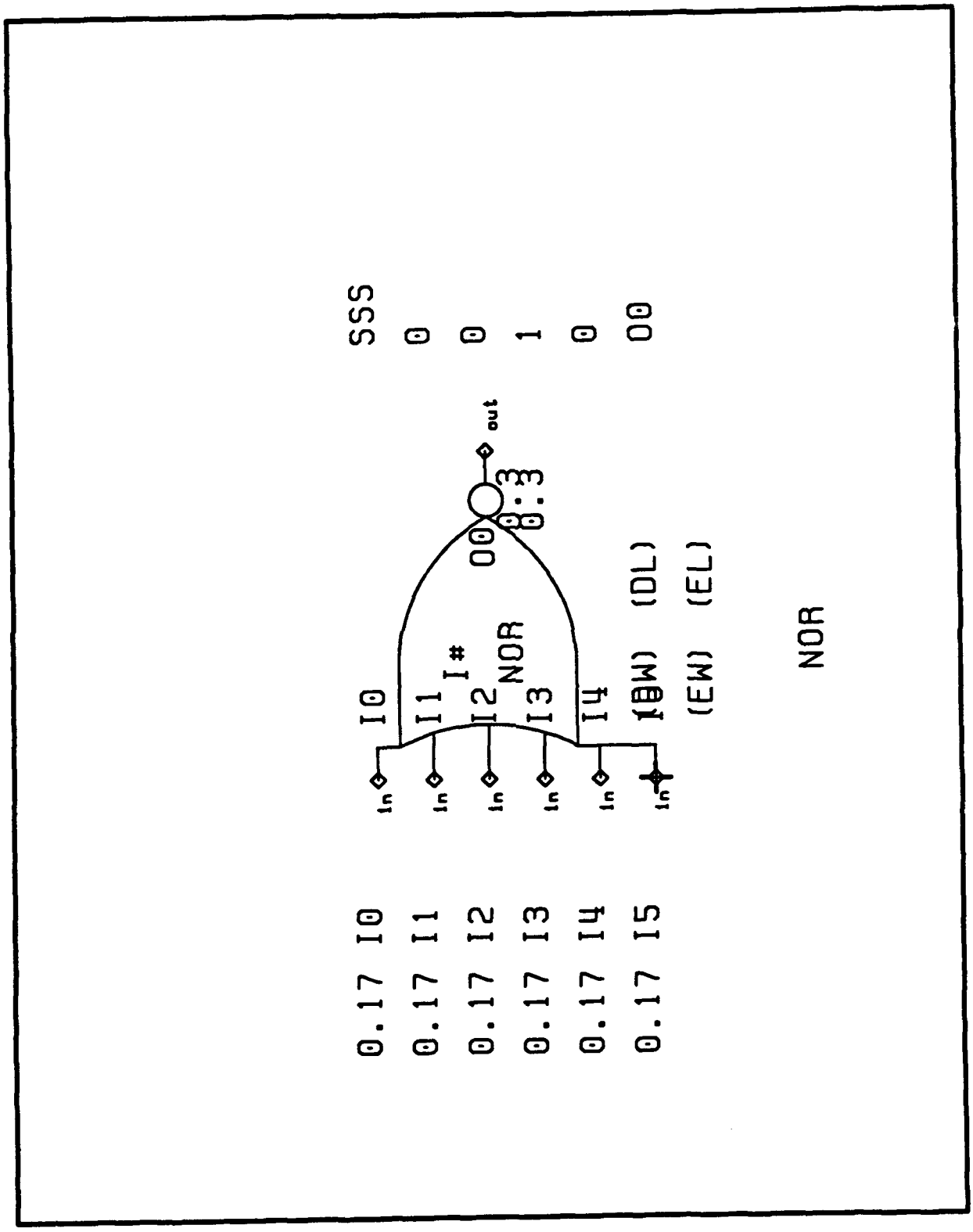

O0
(EW)
(EL)
I$26
I2
(OW)
(OL)
CG
(EW)
(EL)
VTT
I$1
I$2
(EW)
(EL)
I$3
I0
I1

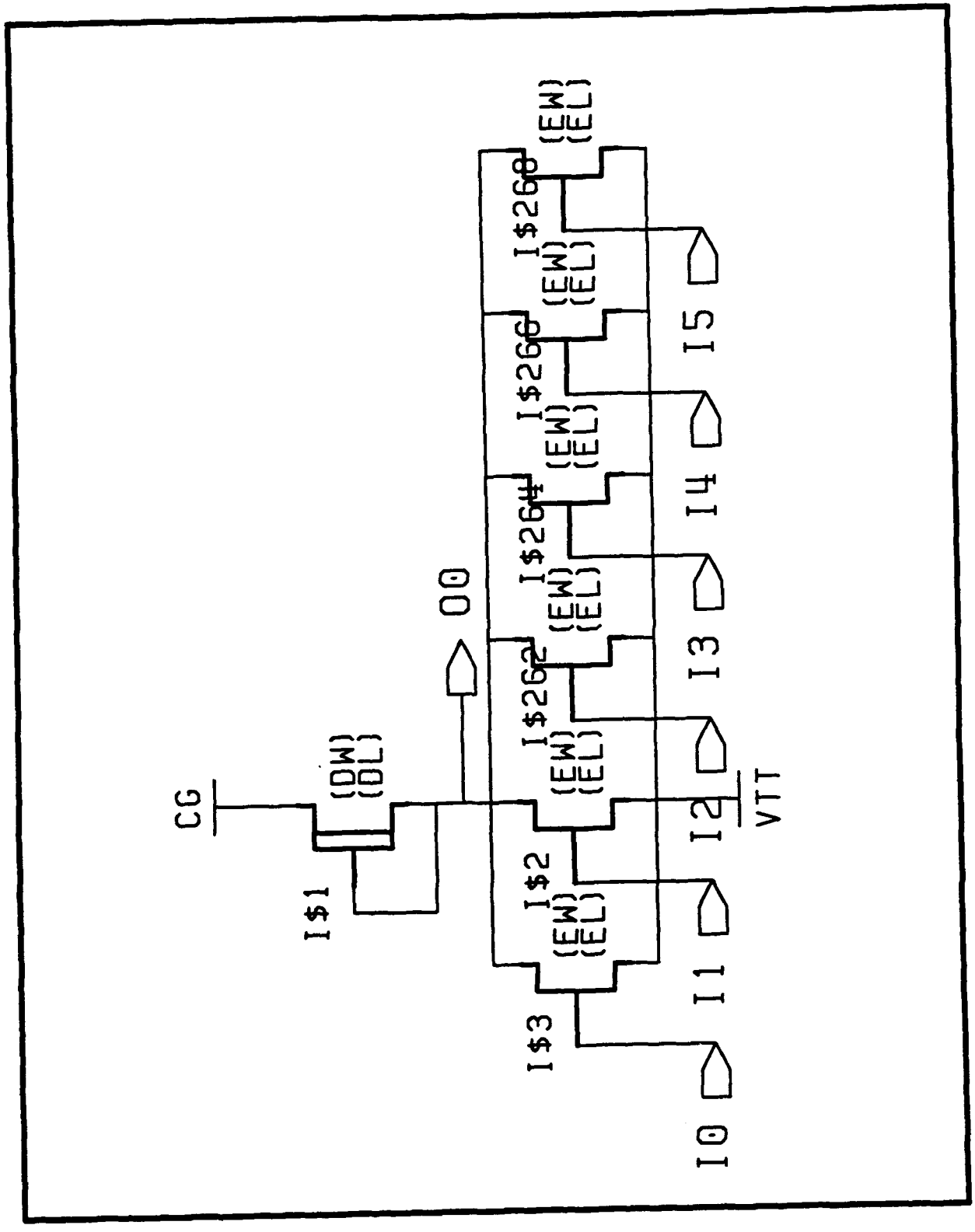

SSS
0 0 1 0 00
out
8:3
00
I0 I# I1 NOR I2 I3
(DW) (DL)
(EW) (EL)
NOR
In In In In
0.17 I0
0.17 I1
0.17 I2
0.17 I3

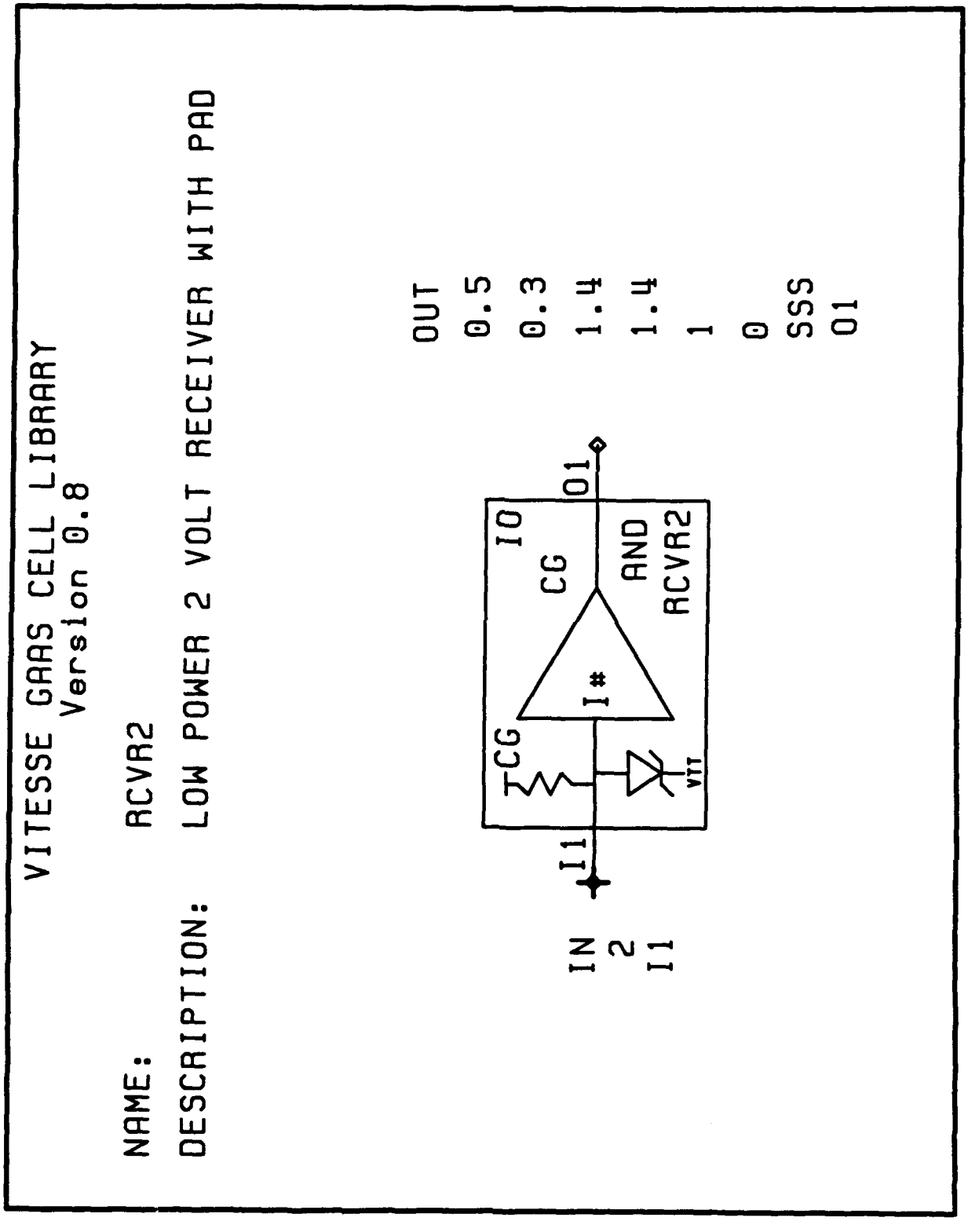

I$262
(EW)
(EL)
I3
O0
I$264
(EW)
(EL)
I2
CG
(DW)
(DL)
I$1
I$2
(EW)
(EL)
VTT
I$3
I0
I1

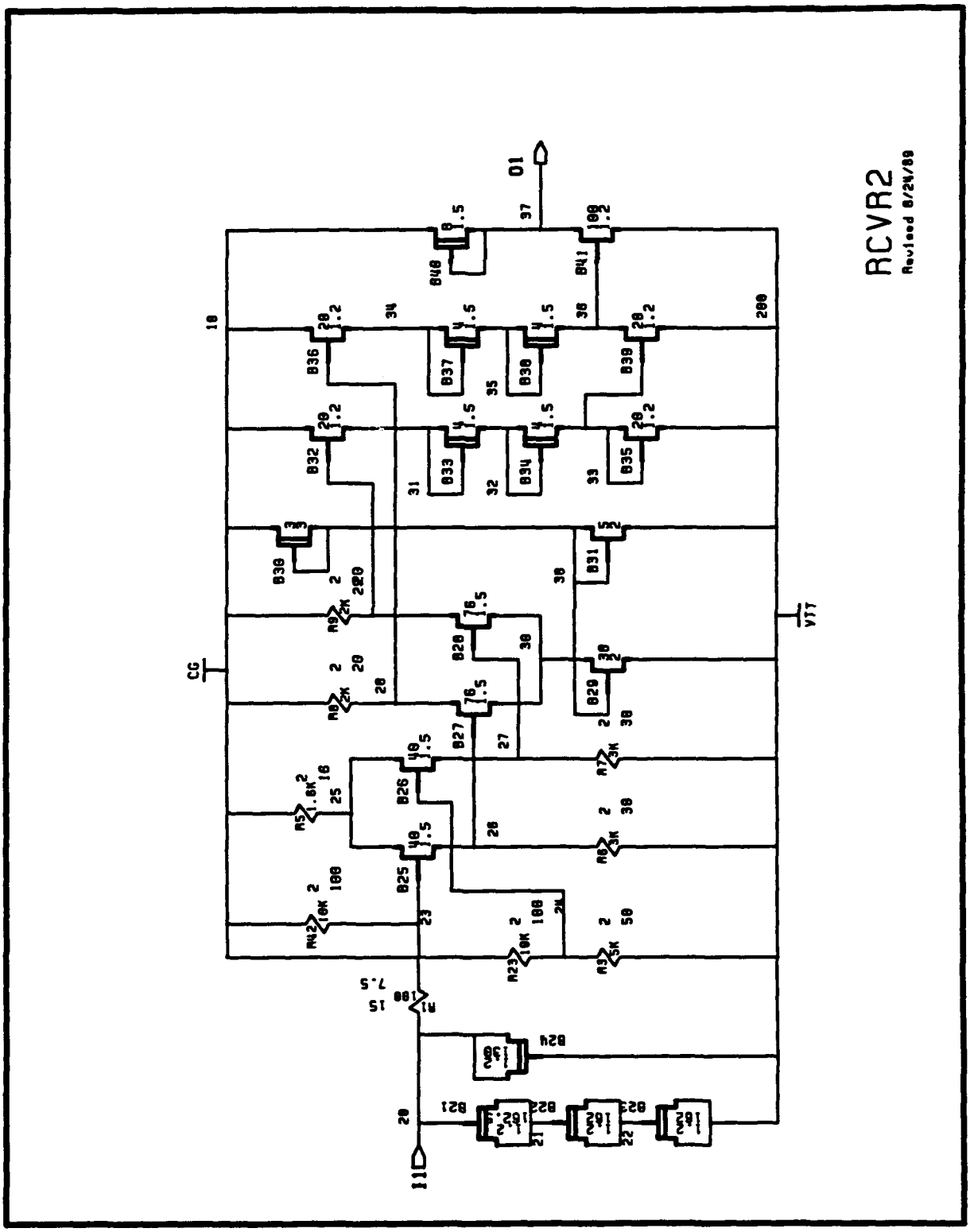

SSS
0
0
1
0
00
out
0.3
0.3
00
(DW) (DL)
(EW) (EL)
NOR
I0
I1
I#
I2
NOR
I3
I4
in
in
in
in
in
0.17 I0
0.17 I1
0.17 I2
0.17 I3
0.17 I4

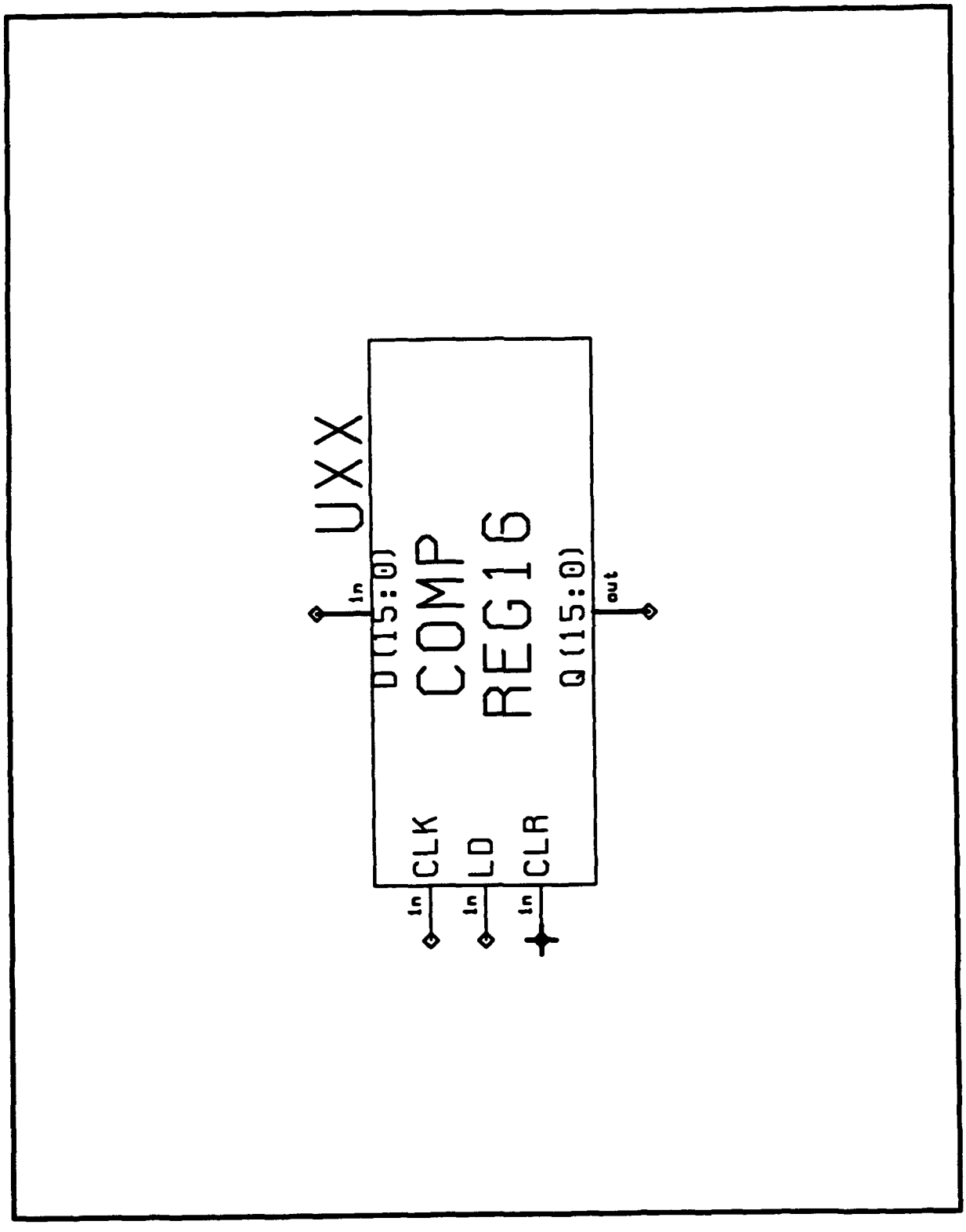

I$266
(EW)
(EL)
I4
I$264
(EW)
(EL)
I3
O0
I$261
(EW)
(EL)
I2
CG
(DW)
(DL)
I$1
(EW)
(EL)
VTT
I$2
(EW)
(EL)
I$3
I0
I1

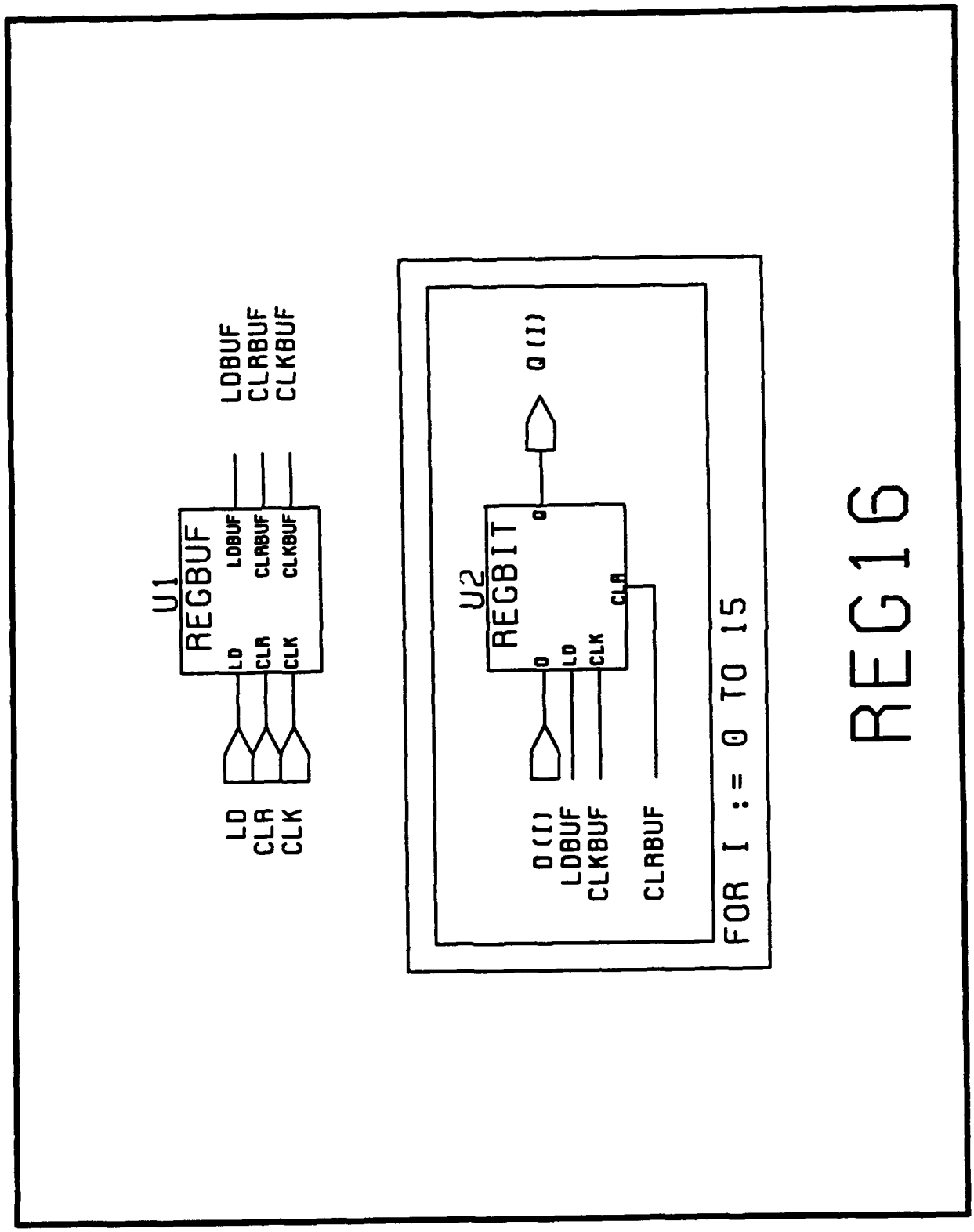

SSS
0 0 1 0 00
out
8:3
00
I0
I1
I#
I2
NOR
I3
I4
(BW) (DL)
(EW) (EL)
NOR
In
0.17 I0
0.17 I1
0.17 I2
0.17 I3
0.17 I4
0.17 I5

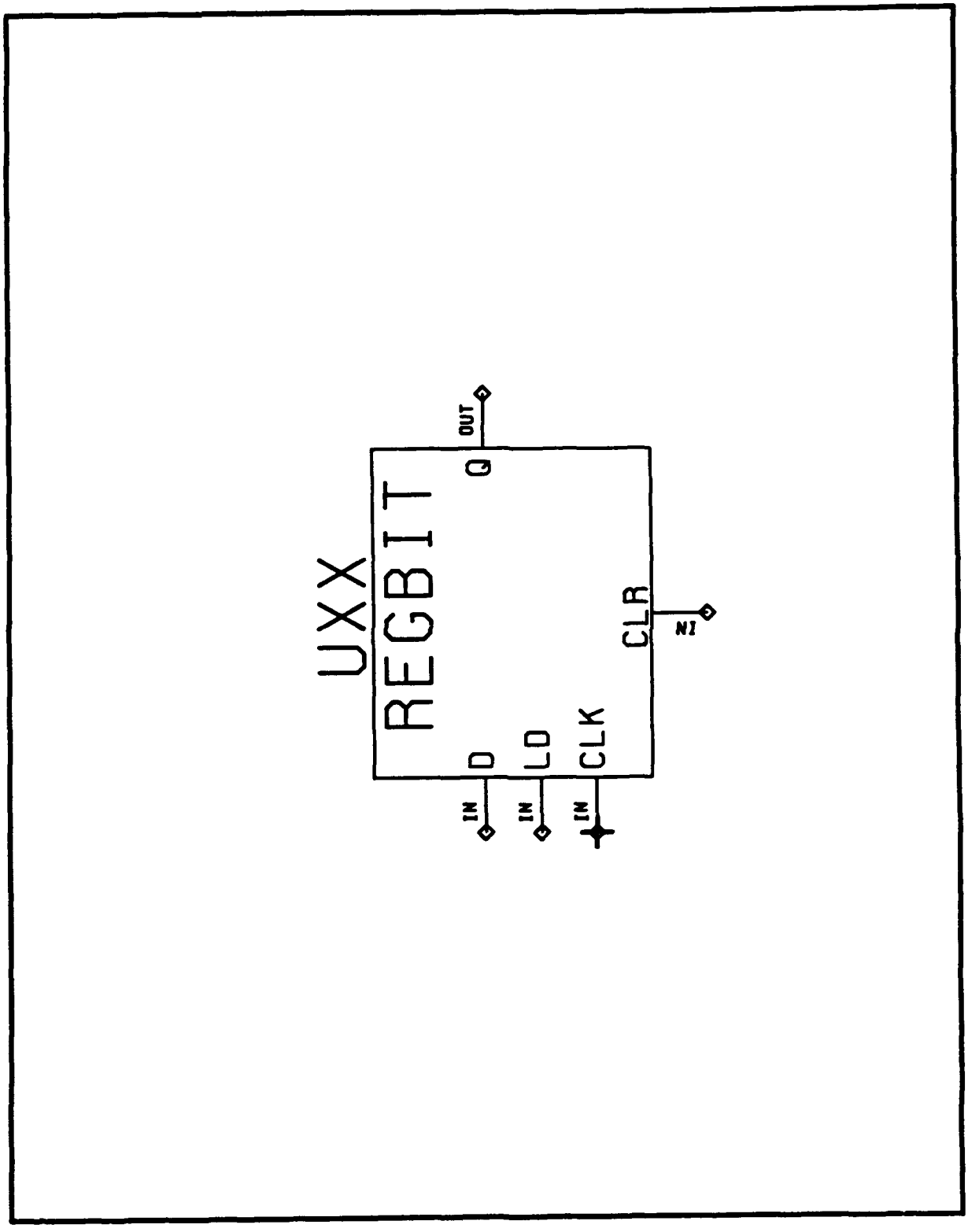

CG
(DW)
(DL)
I$1
O0
I$2
(EW)
(EL)
I$3
I$262
I$264
I$266
I$268
I0
I1
I2
VTT
I3
I4
I5

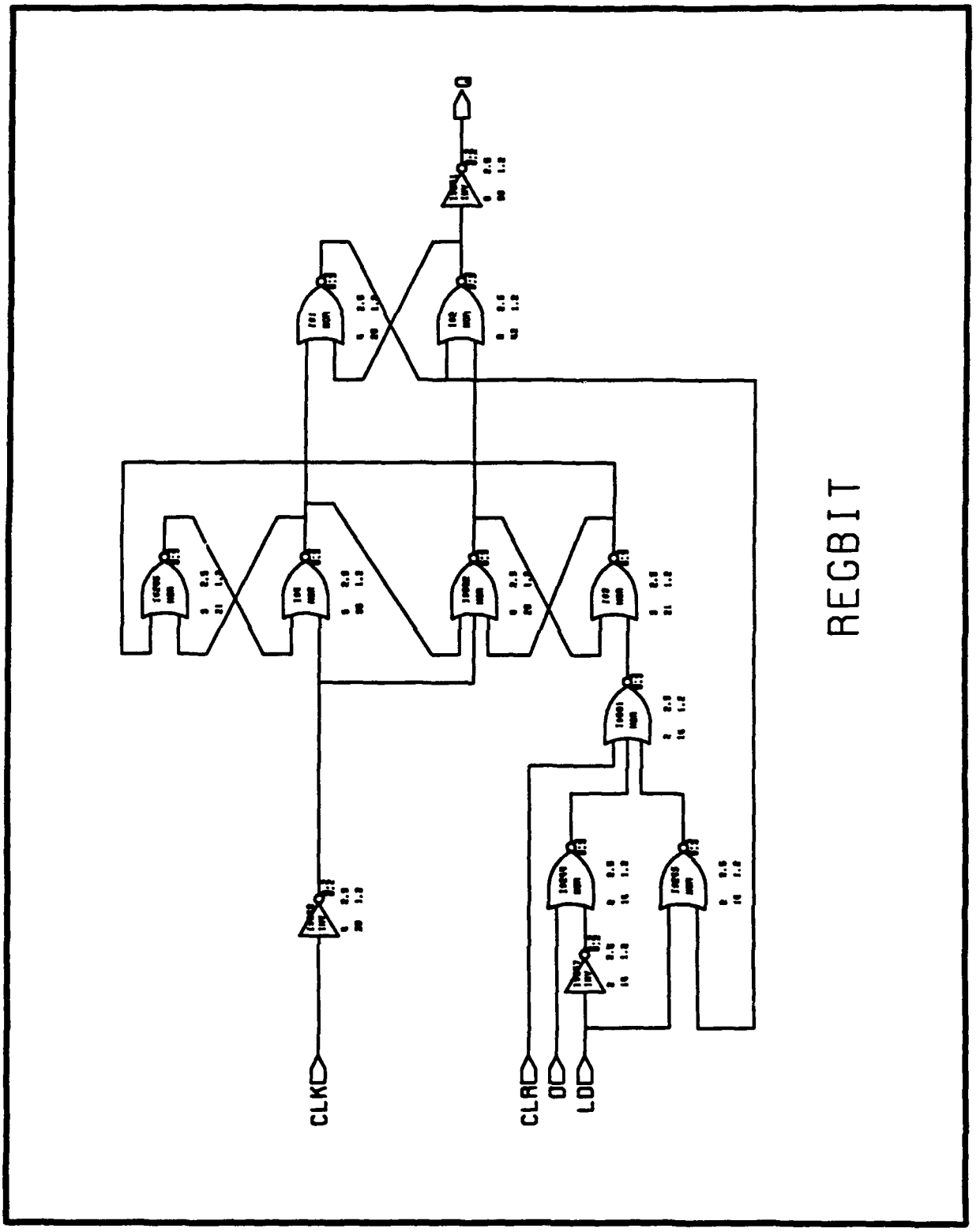

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: RCVR2
DESCRIPTION: LOW POWER 2 VOLT RECEIVER WITH PAD
OUT
0.5
0.3
1.4
1.4
1
0
SSS
01
IN
2
I1
I1
IO
CG
I#
O1
AND
RCVR2
CG
VTT

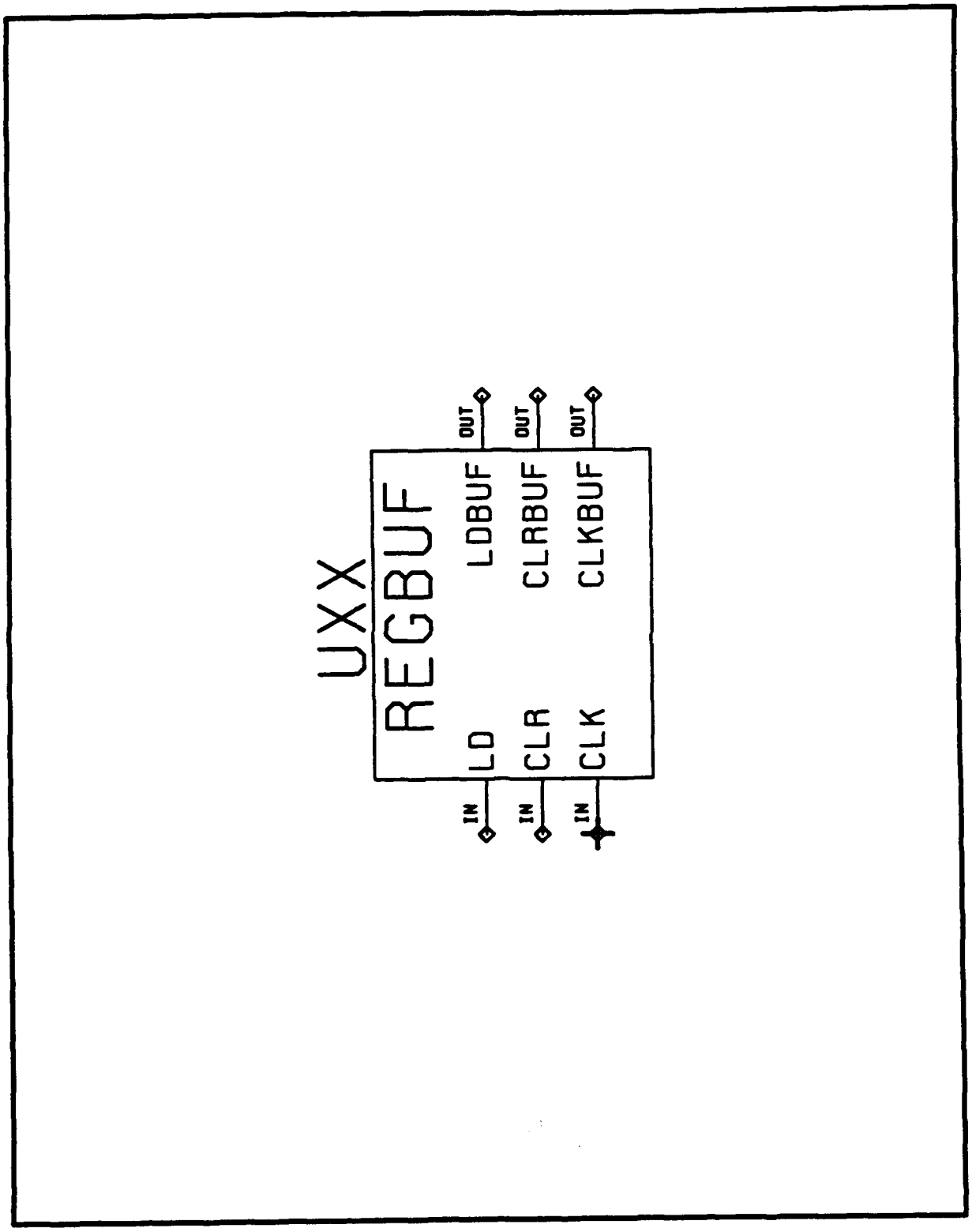

RCVR2
Revised 6/24/89
I1
CG
VTT

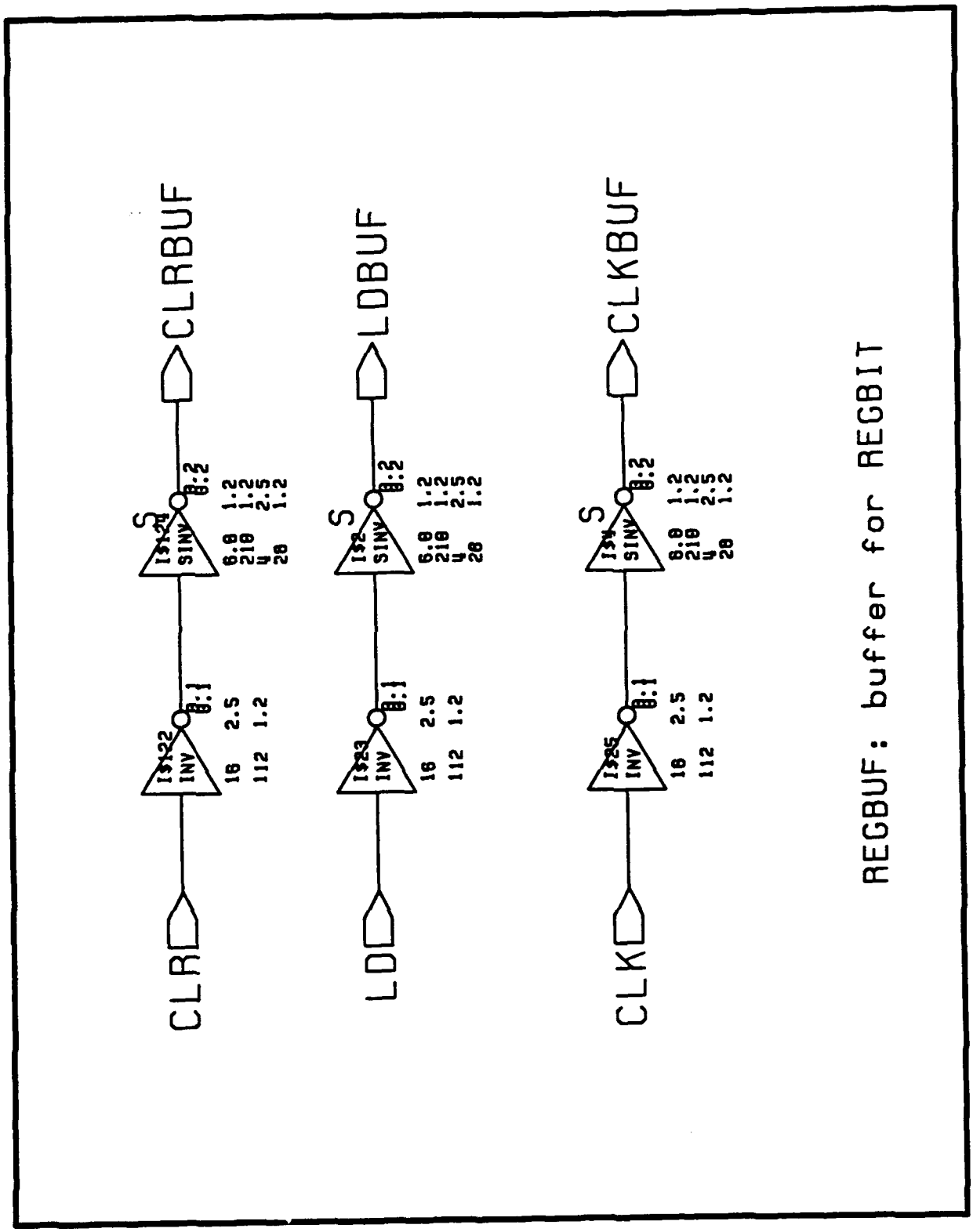

UXX
COMP
REG16
in
D(15:0)
Q(15:0)
out
CLK
LD
CLR
in
in
in

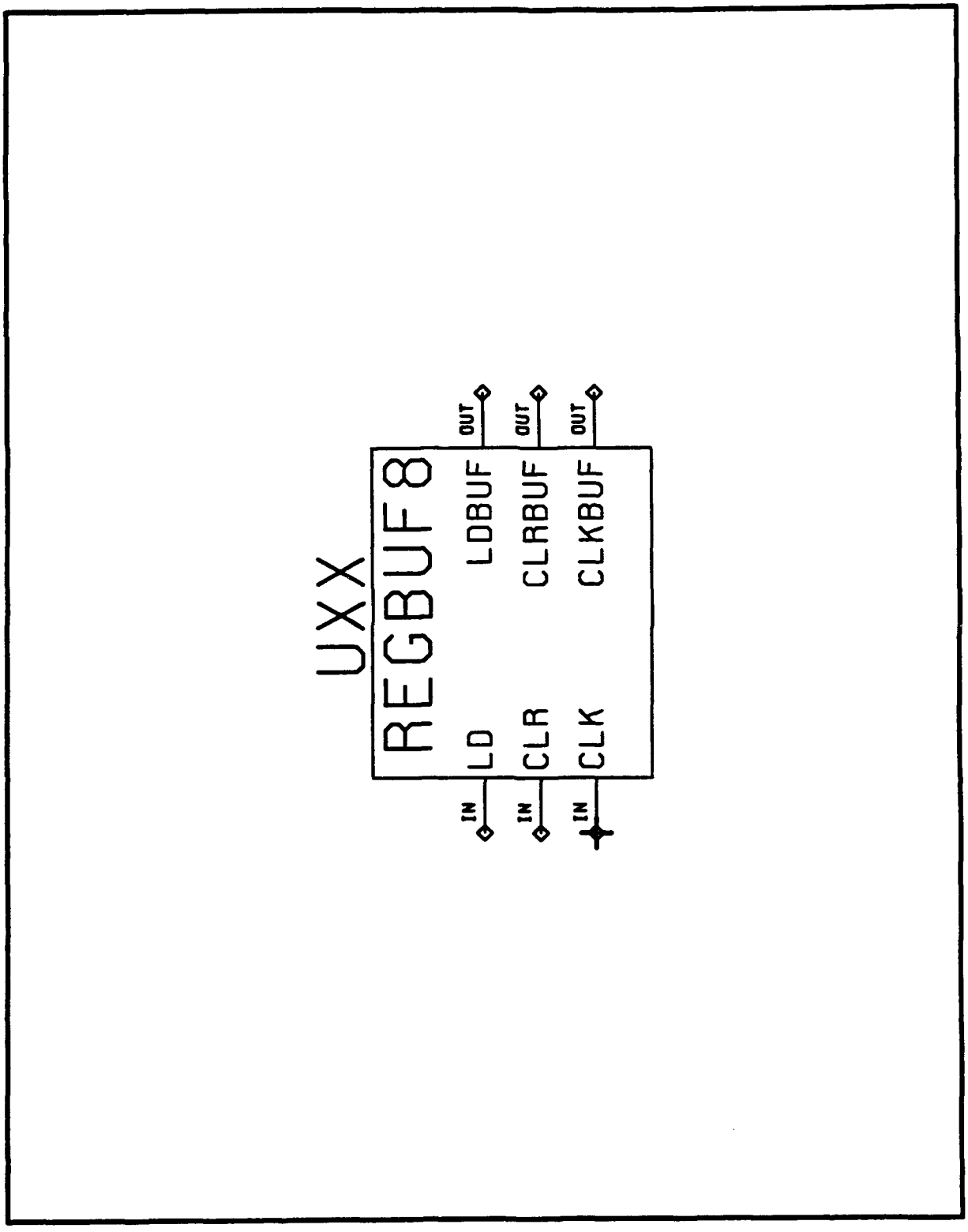

REG16
FOR I := 0 TO 15
U2
REGBIT
D
LD
CLR
CLK
Q (I)
D (I)
LDBUF
CLKBUF
CLRBUF
U1
REGBUF
LDBUF
CLRBUF
CLKBUF
LD
CLR
CLK

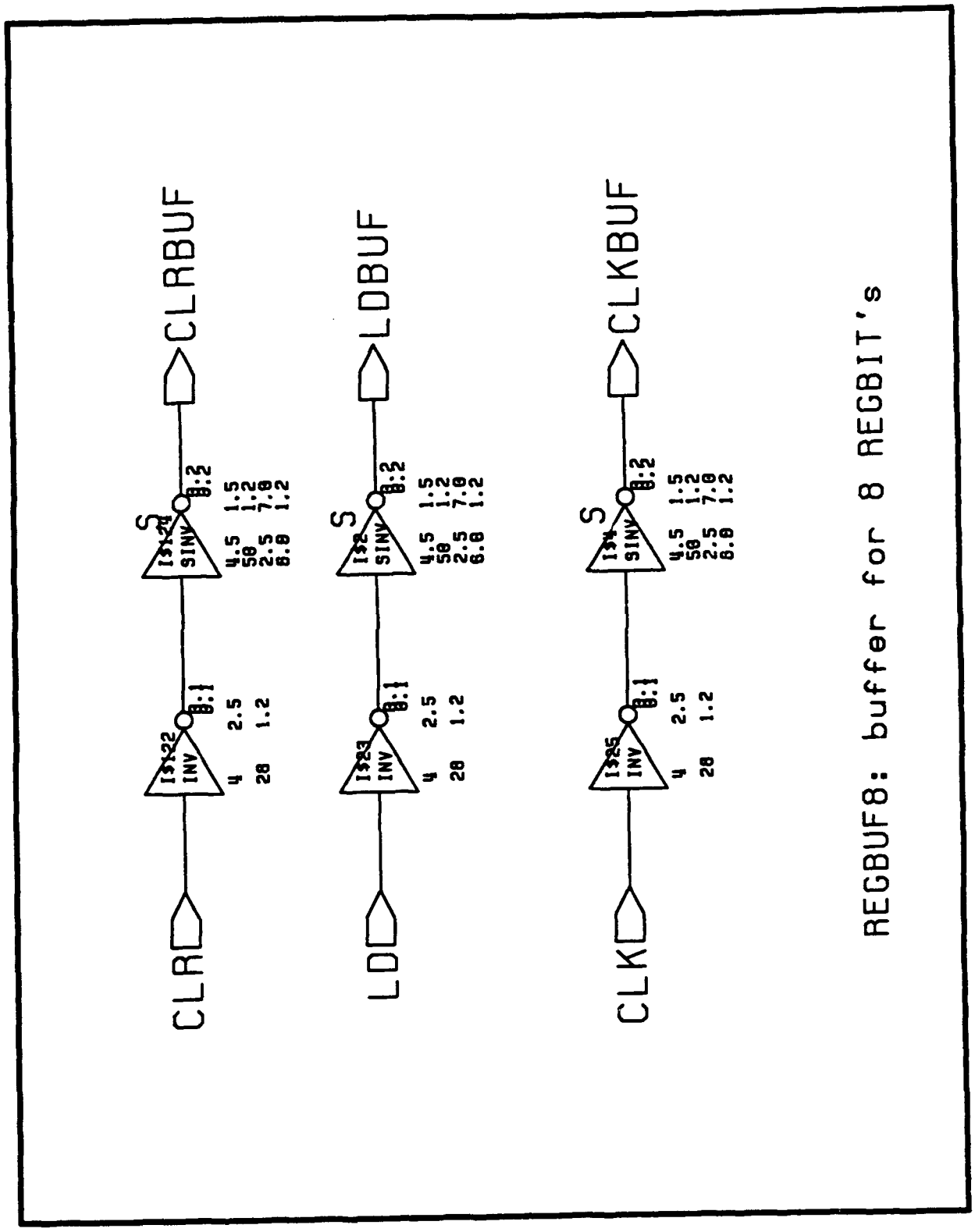

UXX
REGBIT
OUT
Q
CLR
NI
D
LD
CLK
IN
IN
IN

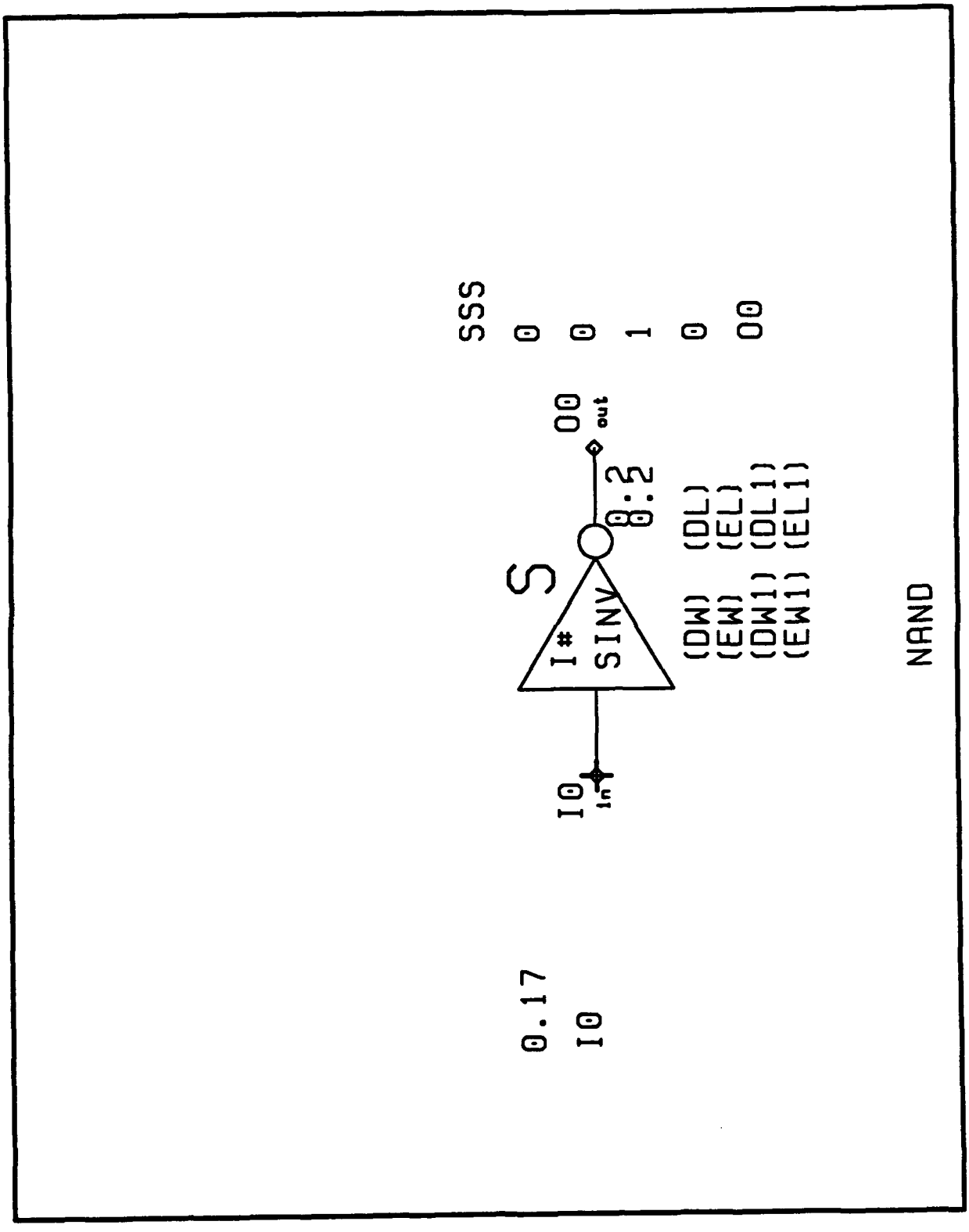

Q
REGBIT
CLK
CLR
D
LD

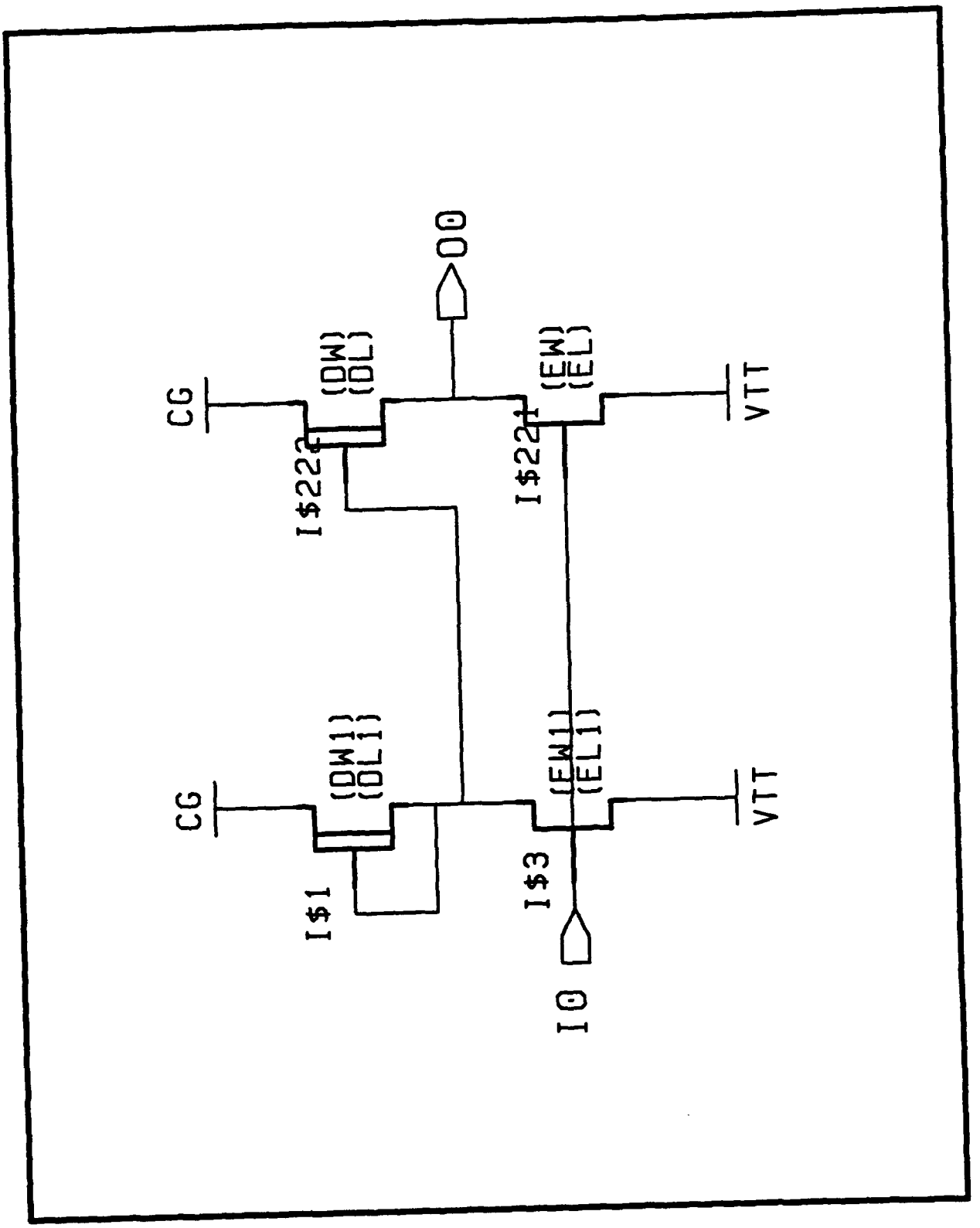

UXX
REGBUF
LDBUF
CLRBUF
CLKBUF
LD
CLR
CLK
OUT
OUT
OUT
IN
IN
IN

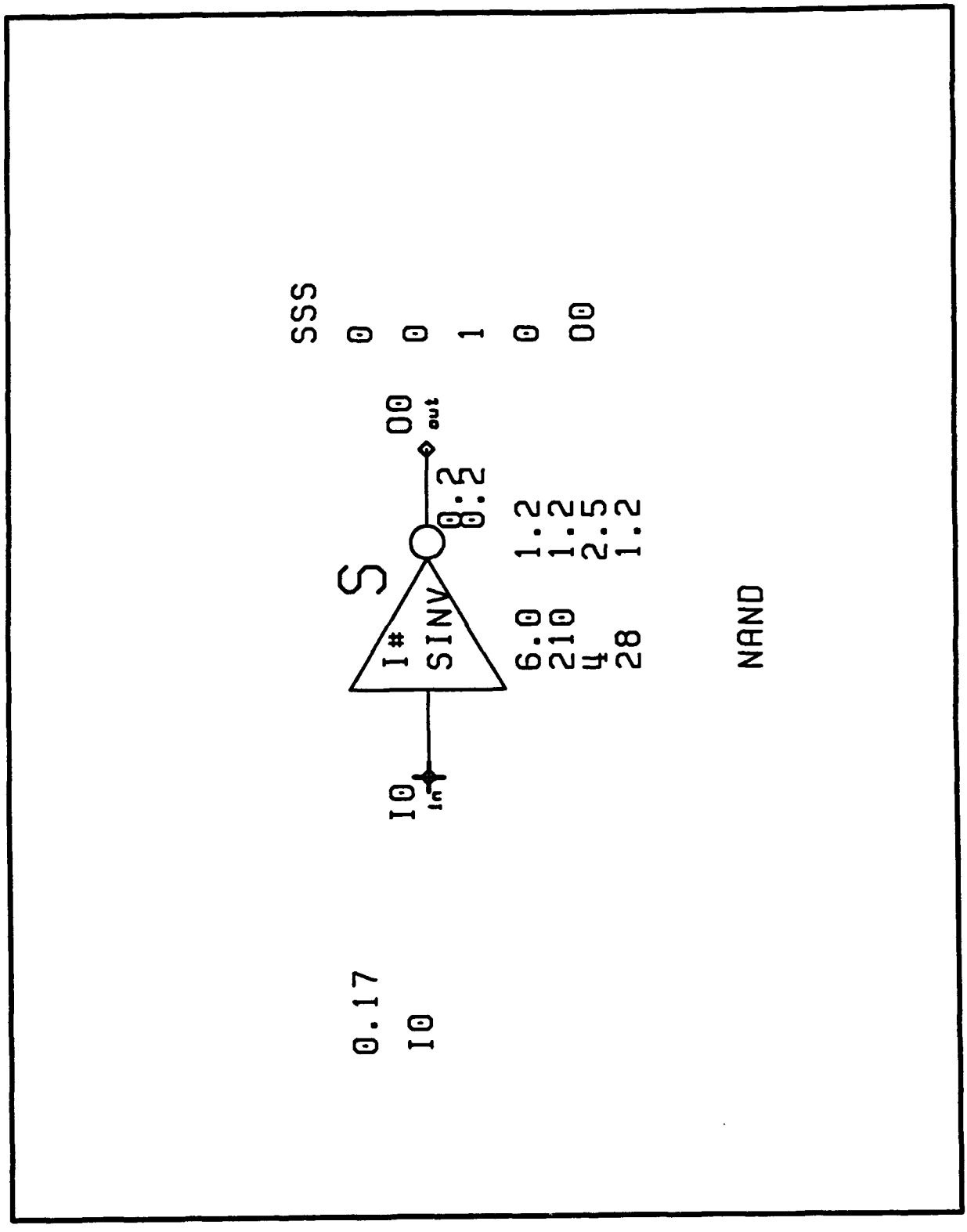

REGBUF: buffer for REGBIT
CLRBUF
LDBUF
CLKBUF
CLR
LD
CLK
I$122
I$123
I$125
I$124
I$2
I$4
INV
SINV
B:1
B:2
16 2.5
112 1.2
6.0 1.2
210 1.2
4 2.5
28 1.2

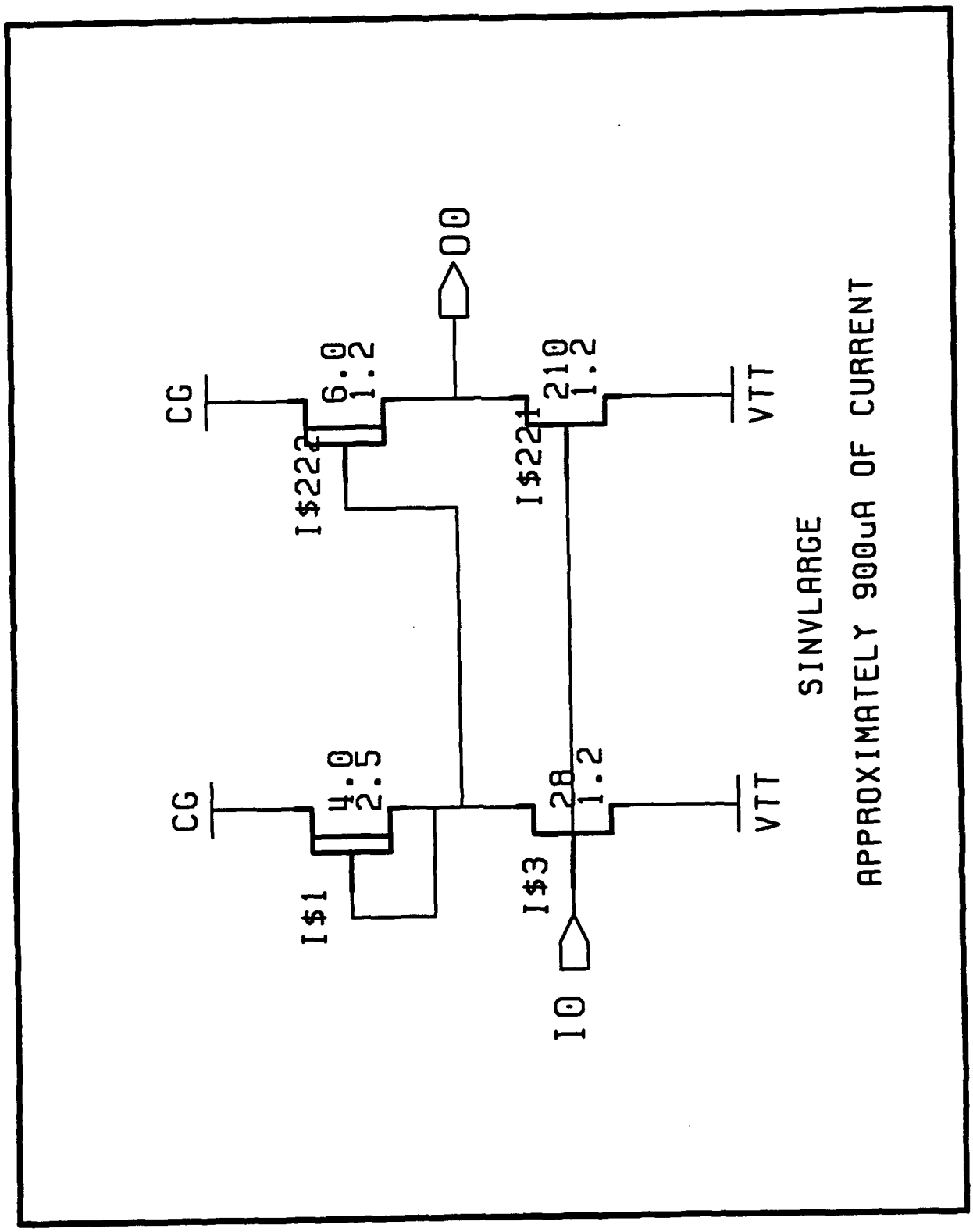

UXX
REGBUF8
LD
CLR
CLK
LDBUF
CLRBUF
CLKBUF
IN
IN
IN
OUT
OUT
OUT

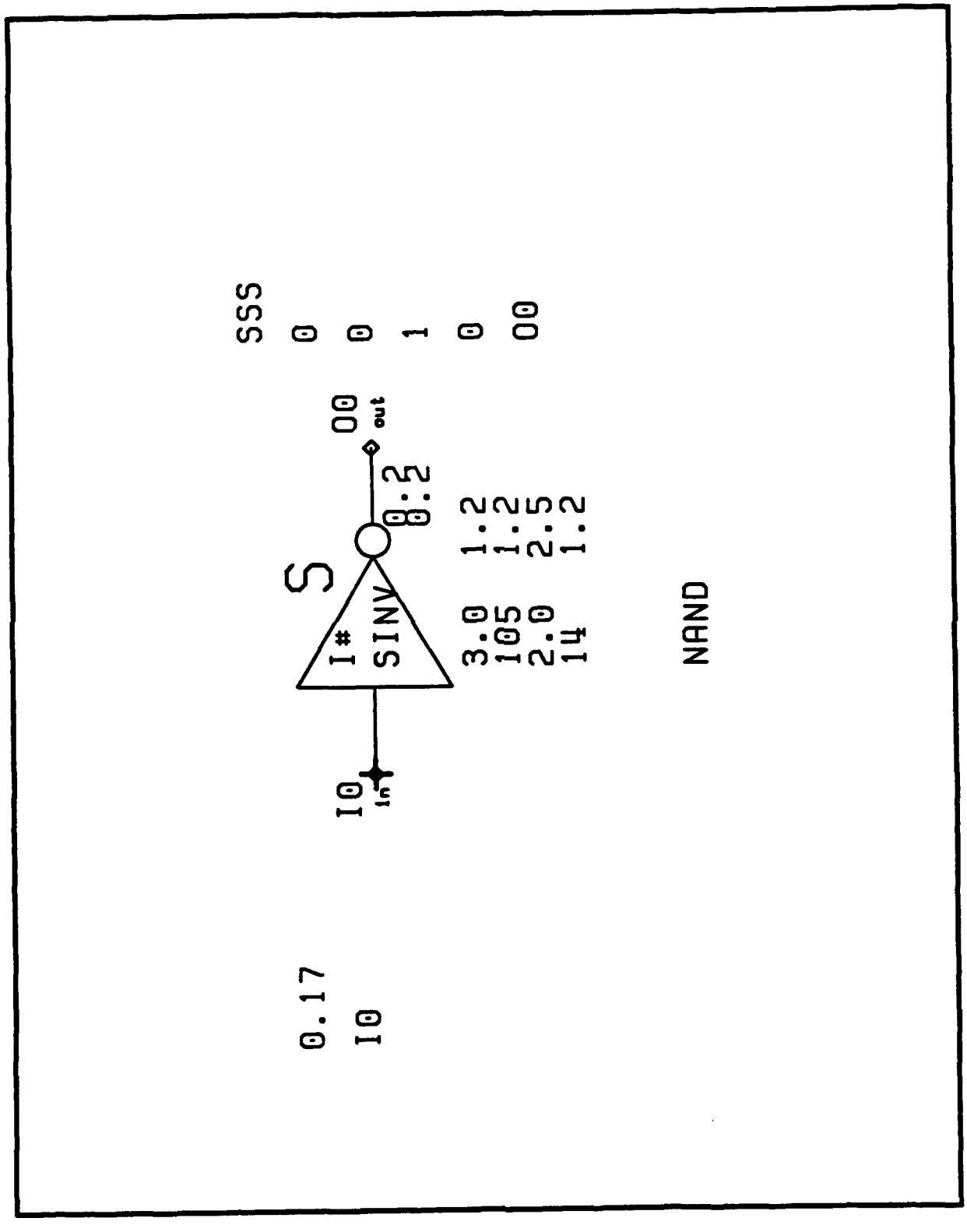

REGBUF8: buffer for 8 REGBIT's
CLRBUF
LDBUF
CLKBUF
CLR
LD
CLK
INV
SINV
4.5 1.5
50 1.2
2.5 7.0
6.0 1.2
4 2.5
28 1.2

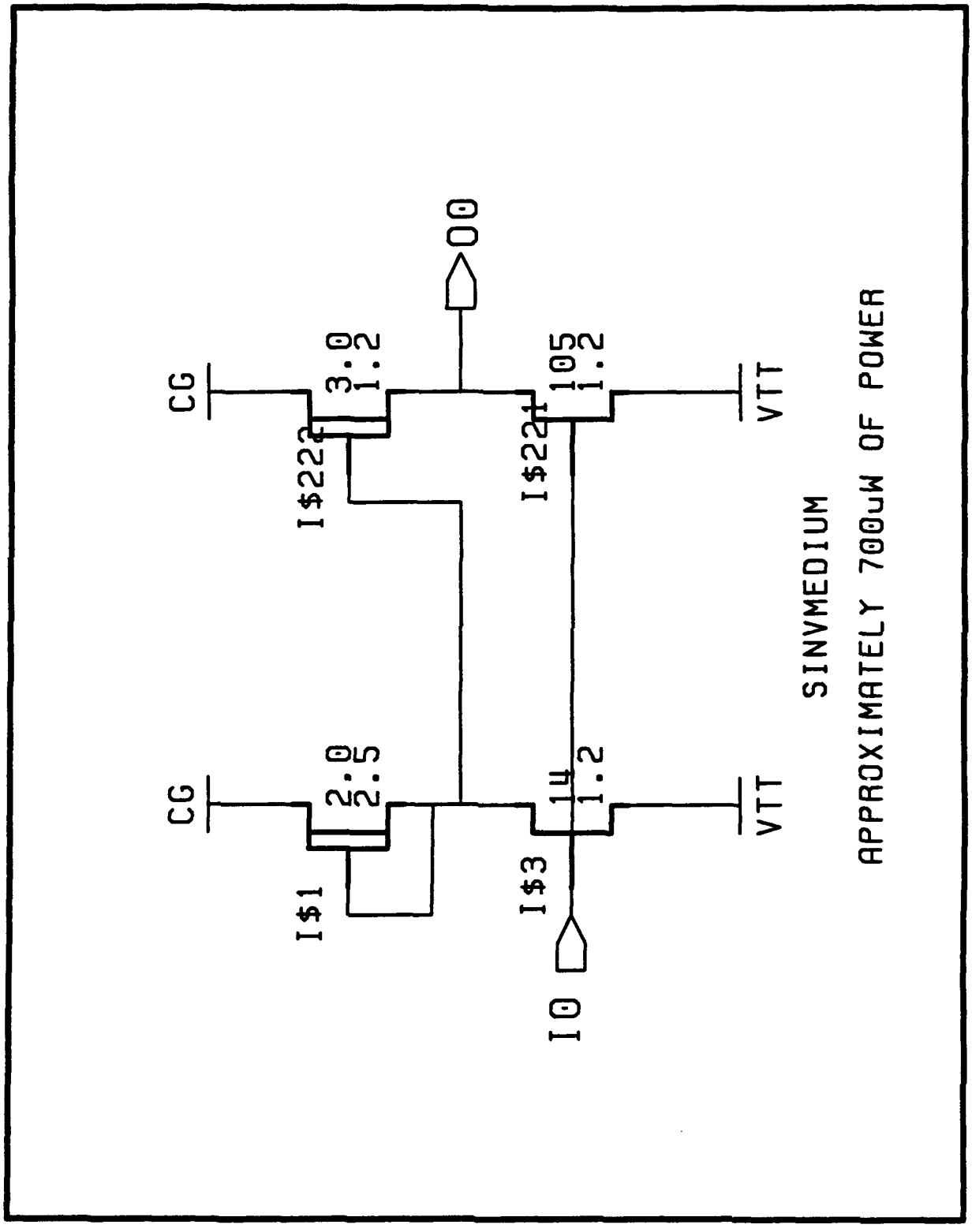

SSS
0 0 1 0 00
00
out
8.2
S
I#
SINV
(DW) (DL)
(EW) (EL)
(DW1) (OL1)
(EW1) (EL1)
NAND
I0
In
0.17
I0

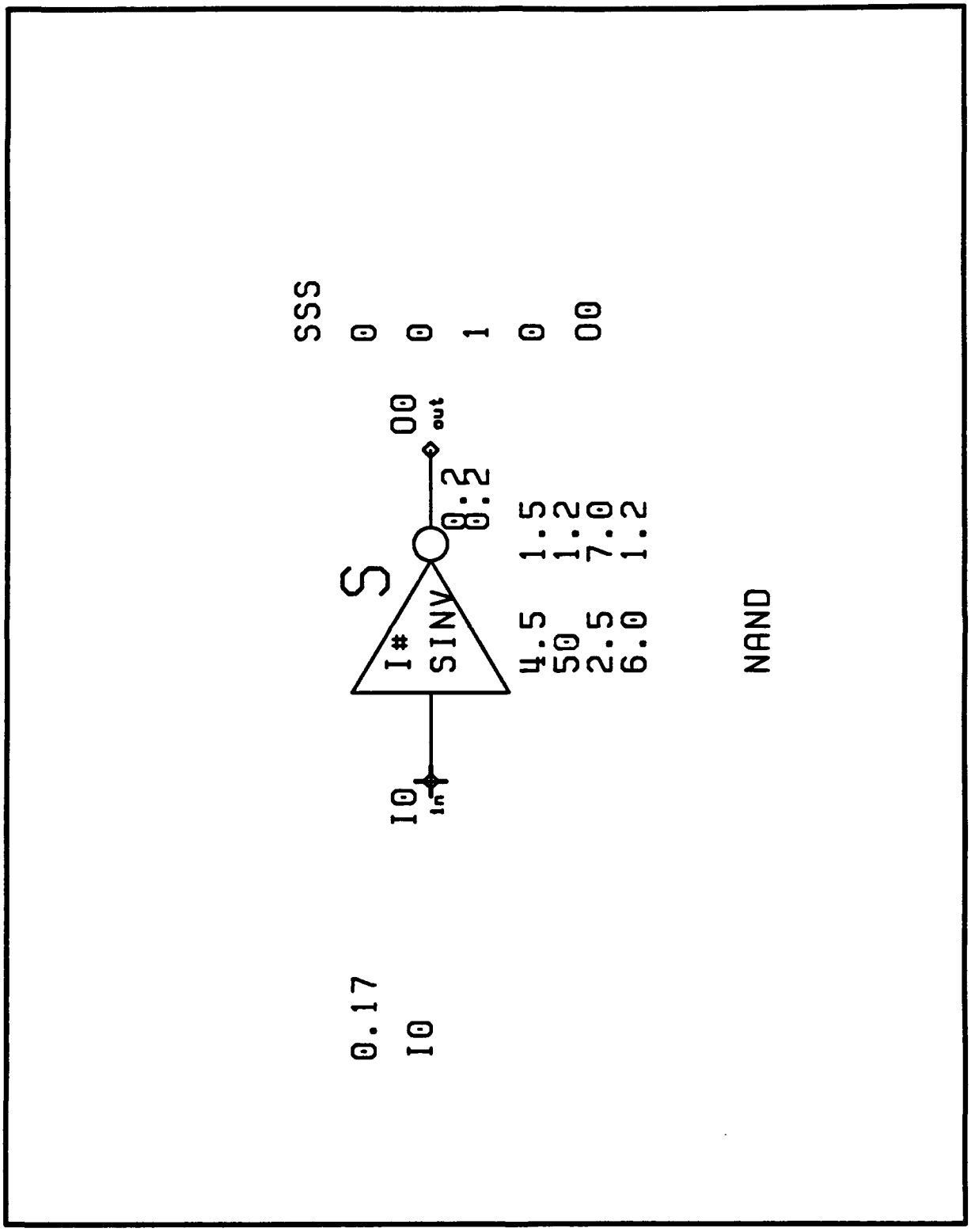

O0
CG
(DW)
(DL)
I$22
(EW)
(EL)
I$22
VTT
CG
(DW1)
(DL1)
I$1
(EW1)
(EL1)
I$3
VTT
IO

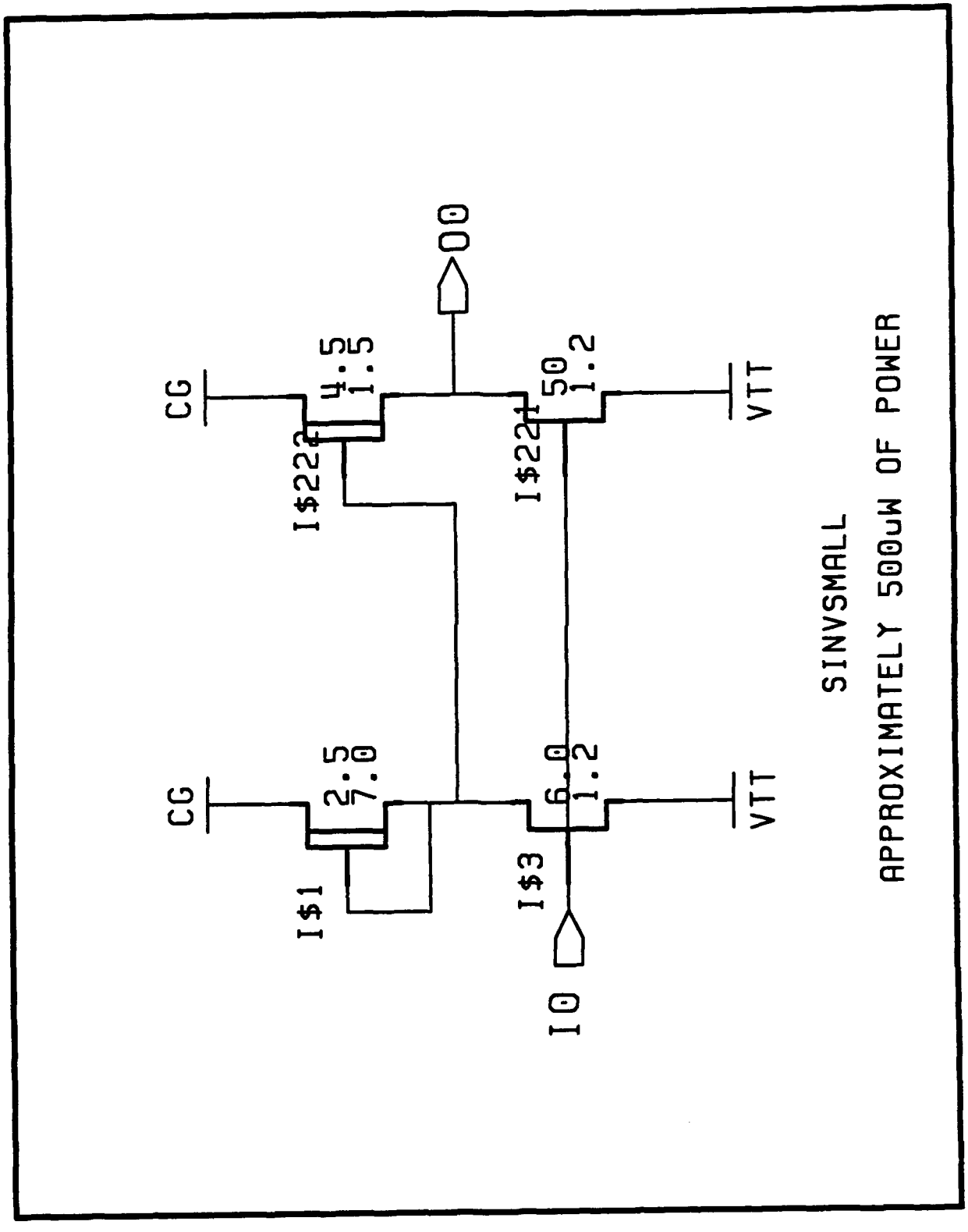

SSS
0 0 1 0 00
00
out
8.2
S
I#
SINV
6.0 1.2
210 1.2
4 2.5
28 1.2
NAND
IO
in
0.17
IO

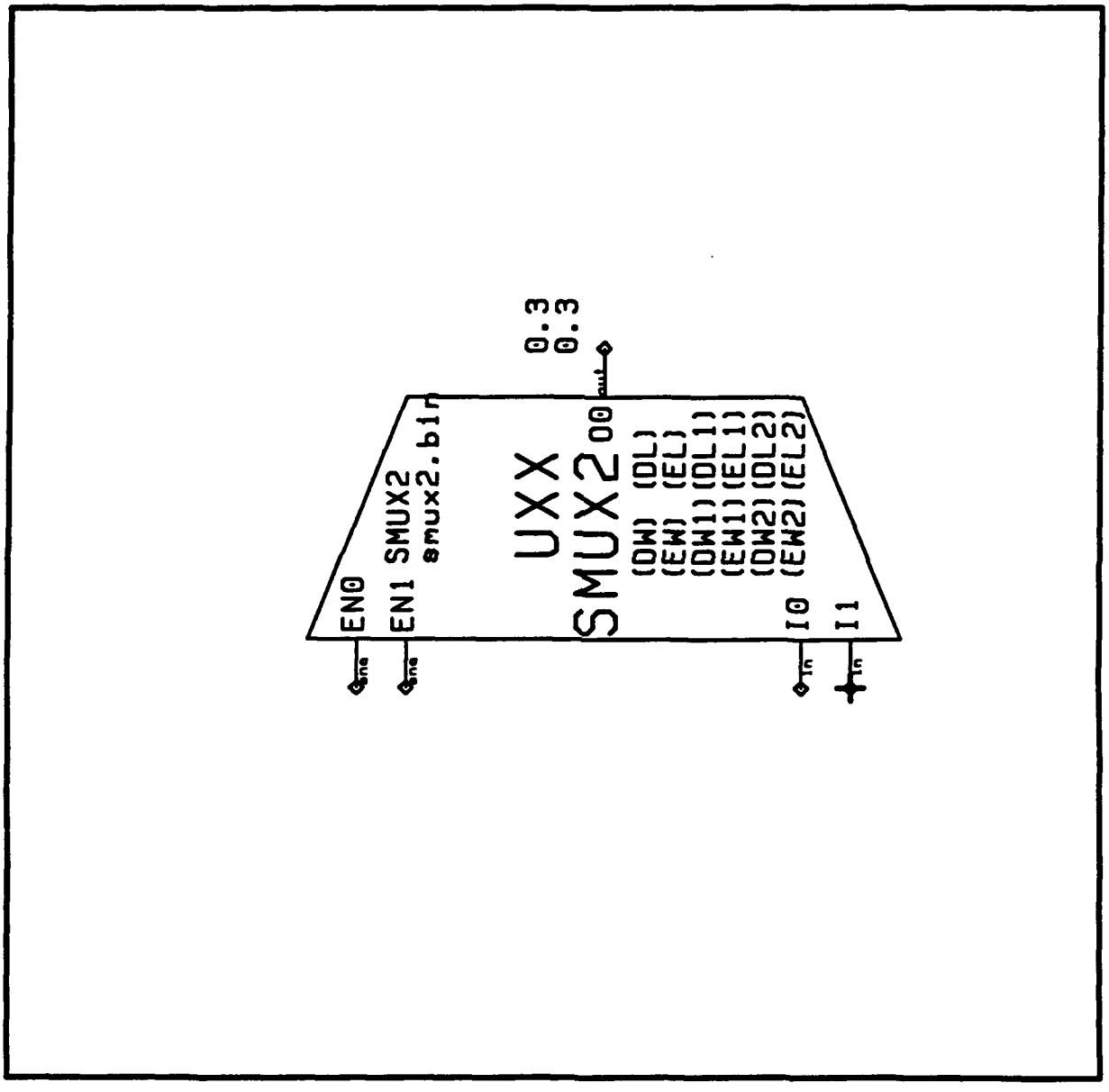

SINVLARGE
APPROXIMATELY 900uA OF CURRENT
CG
6.0
1.2
I$22
O0
210
1.2
I$21
VTT
CG
4.0
2.5
I$1
28
1.2
I$3
VTT
IO

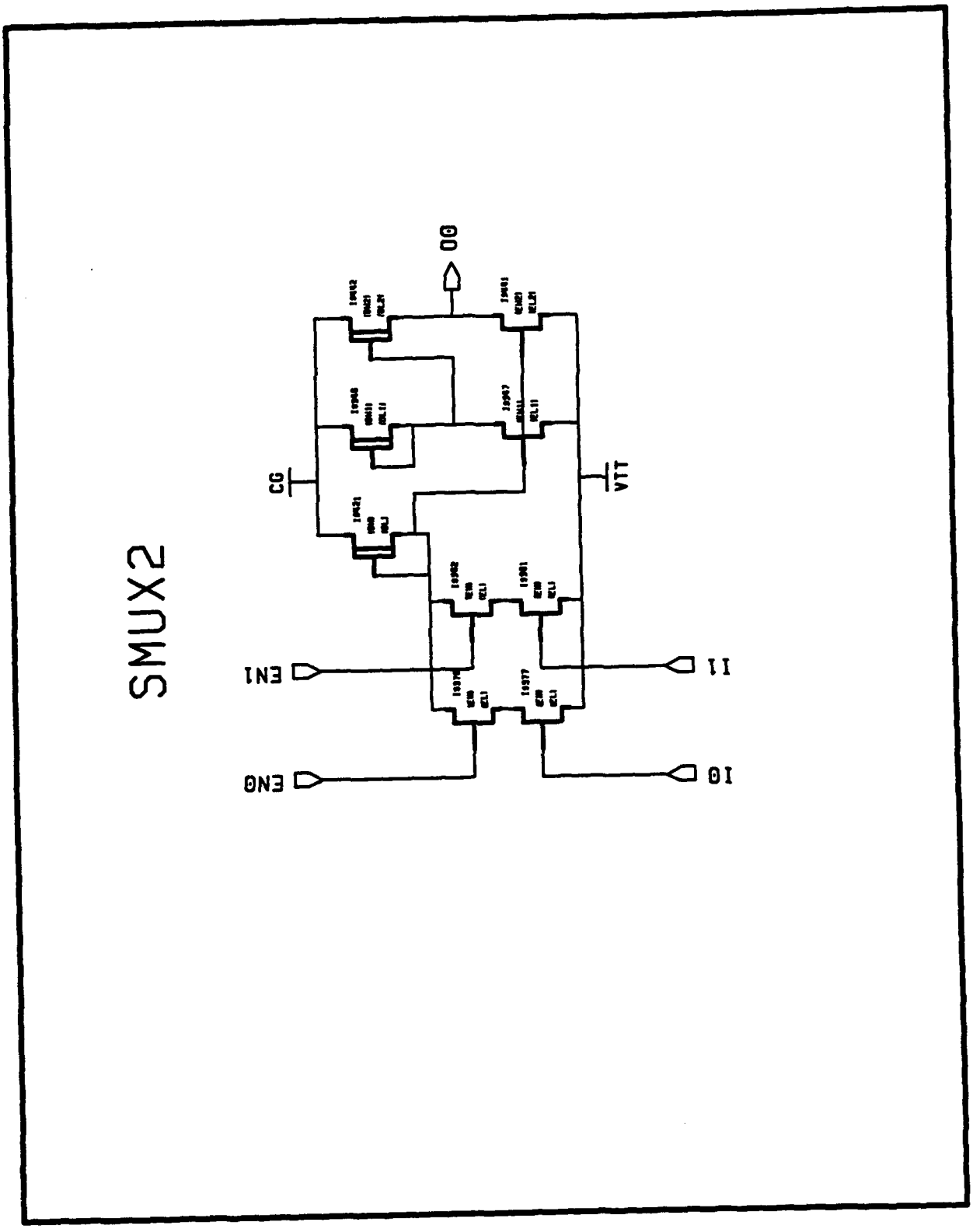

SSS
0 0 1 0 00
00
out
8.2
1.2
1.2
2.5
1.2
S
I#
SINV
3.0
105
2.0
14
NAND
I0
in
0.17
I0

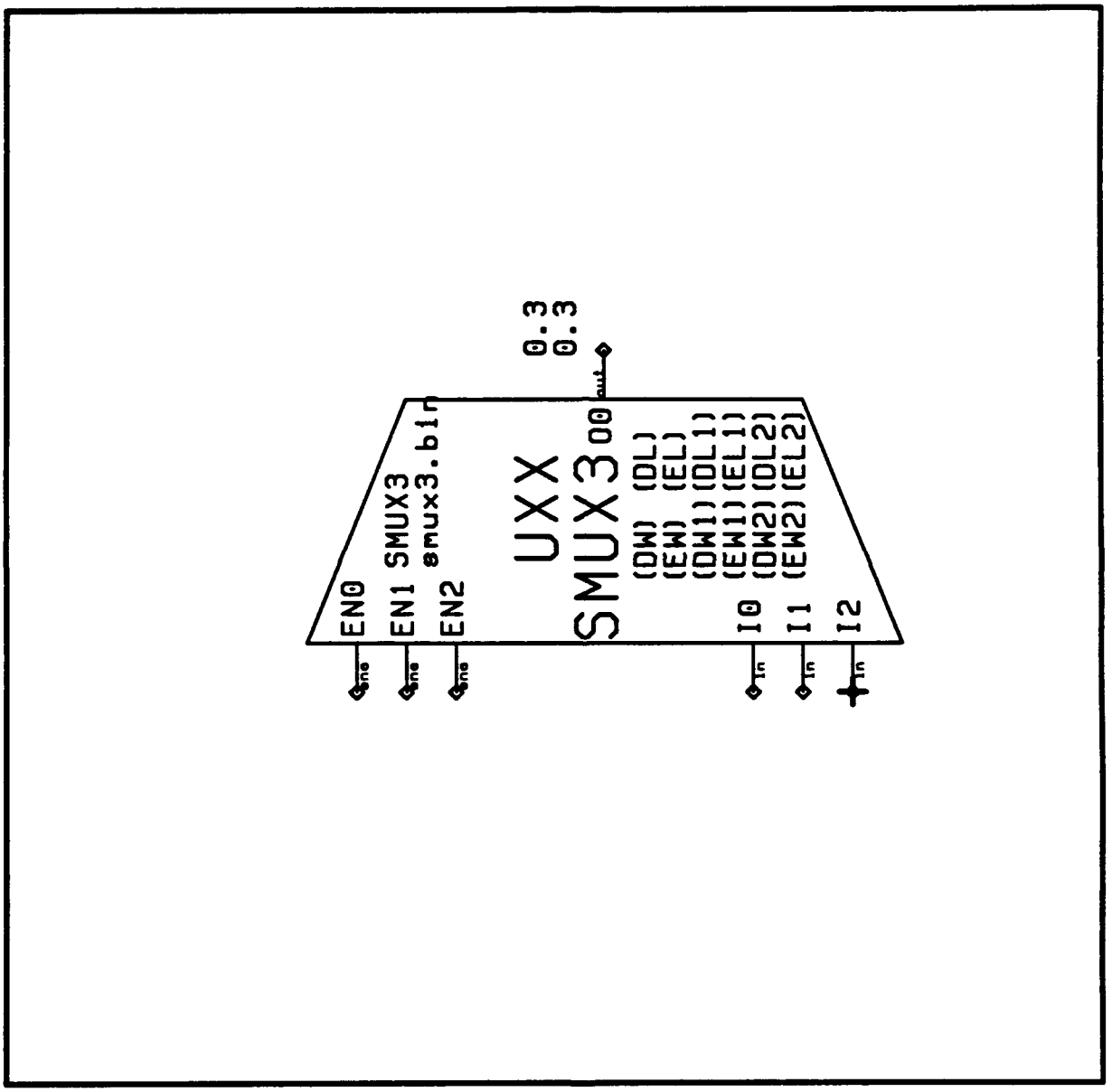

O0
CG
3.0
1.2
I$22
105
1.2
I$21
VTT
CG
2.0
2.5
I$1
14
1.2
I$3
VTT
IO
SINVMEDIUM
APPROXIMATELY 700uW OF POWER

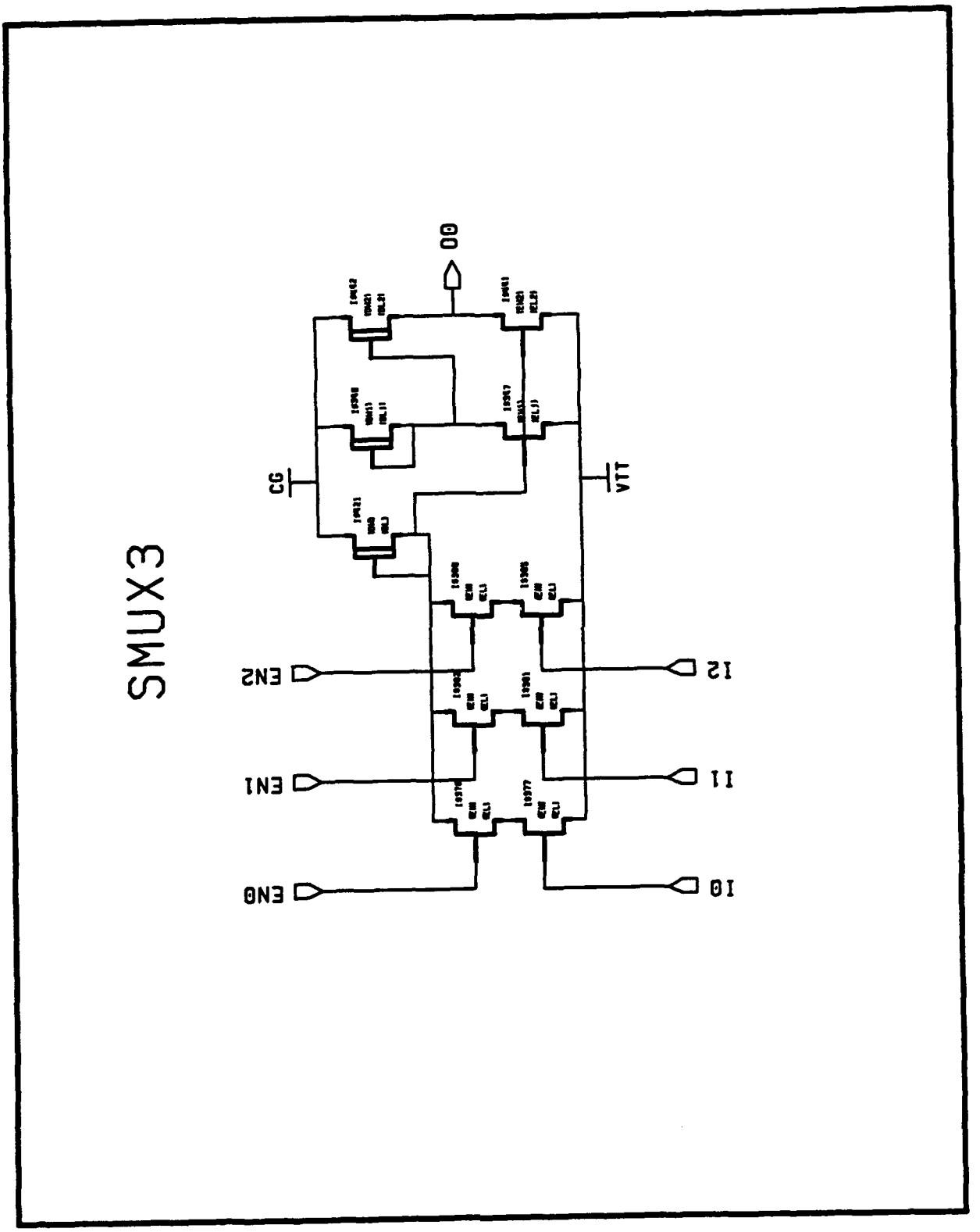

SSS
0 0 1 0 00
00
out
8.2
S
I#
SINV
4.5 1.5
50 1.2
2.5 7.0
6.0 1.2
NAND
I0
in
0.17
I0

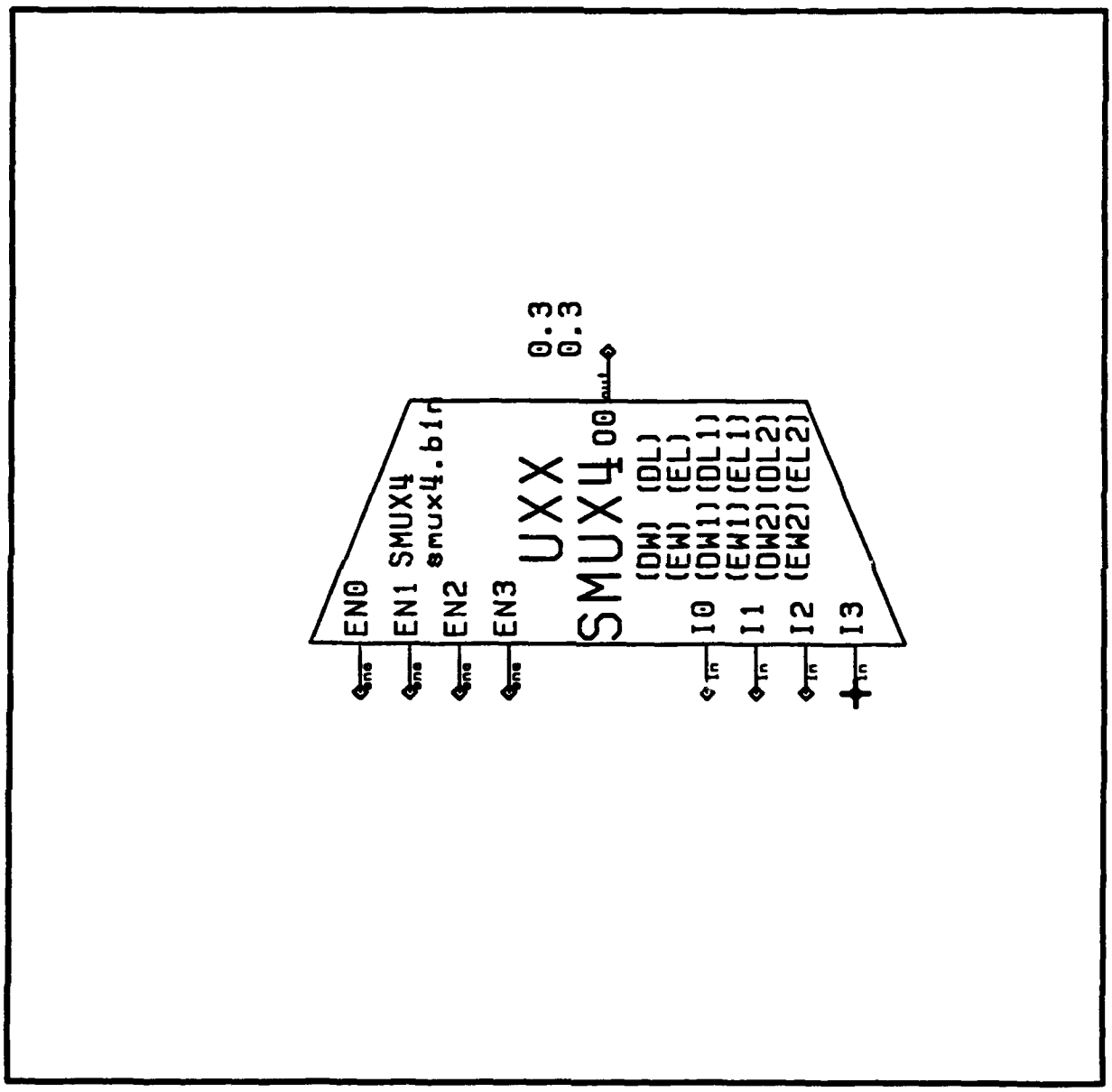

O0
CG
4.5
1.5
I$22
50
1.2
I$21
VTT
SINVSMALL
APPROXIMATELY 500uW OF POWER
CG
2.5
7.0
I$1
6.0
1.2
I$3
VTT
IO

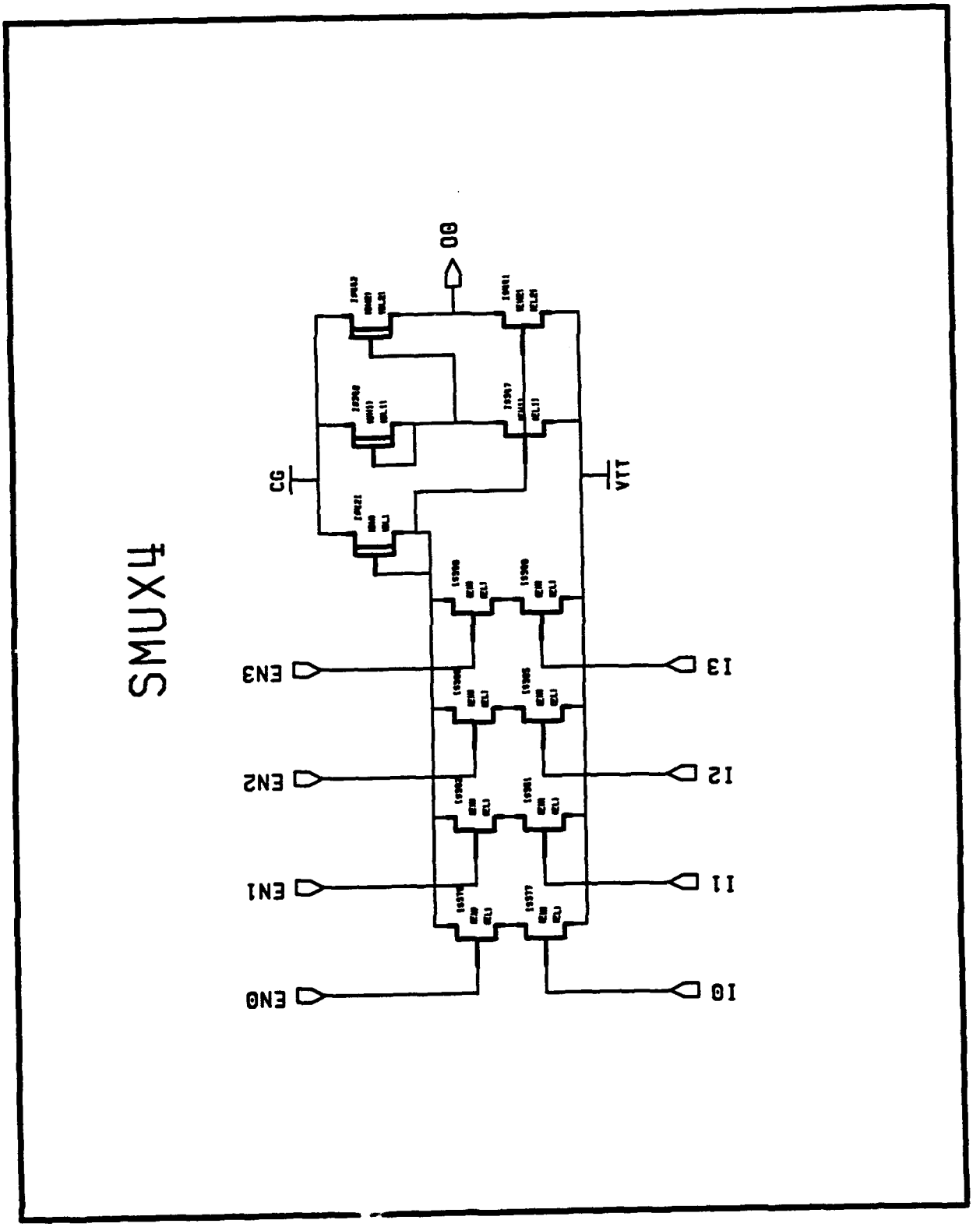

0.3
0.3
UXX
SMUX200
smux2.bin
EN0
EN1 SMUX2
(0W) (0L)
(EW) (EL)
(0W1)(0L1)
(EW1)(EL1)
(0W2)(0L2)
(EW2)(EL2)
I0
I1

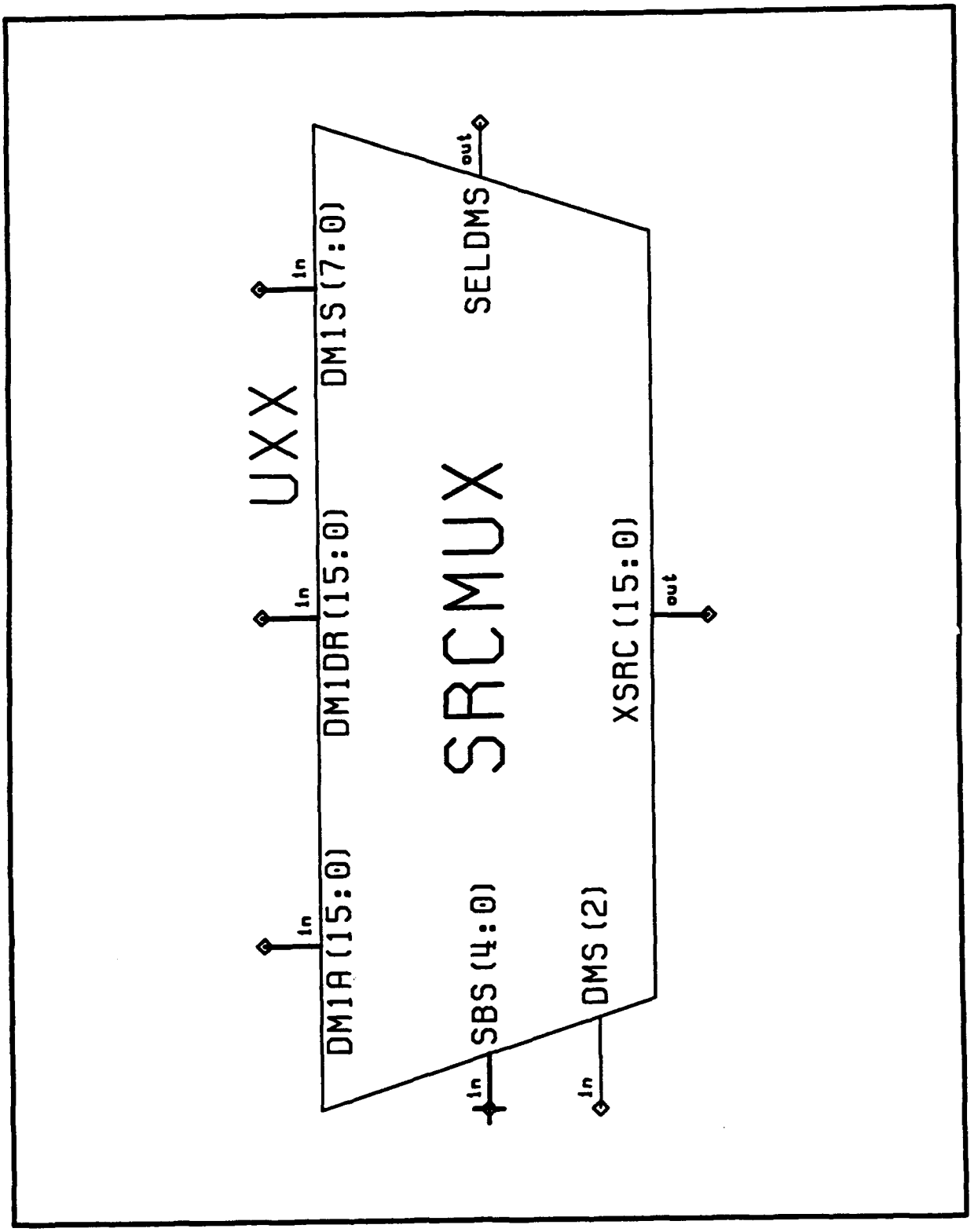

SMUX2
O0
CG
VTT
EN1
I1
EN0
I0

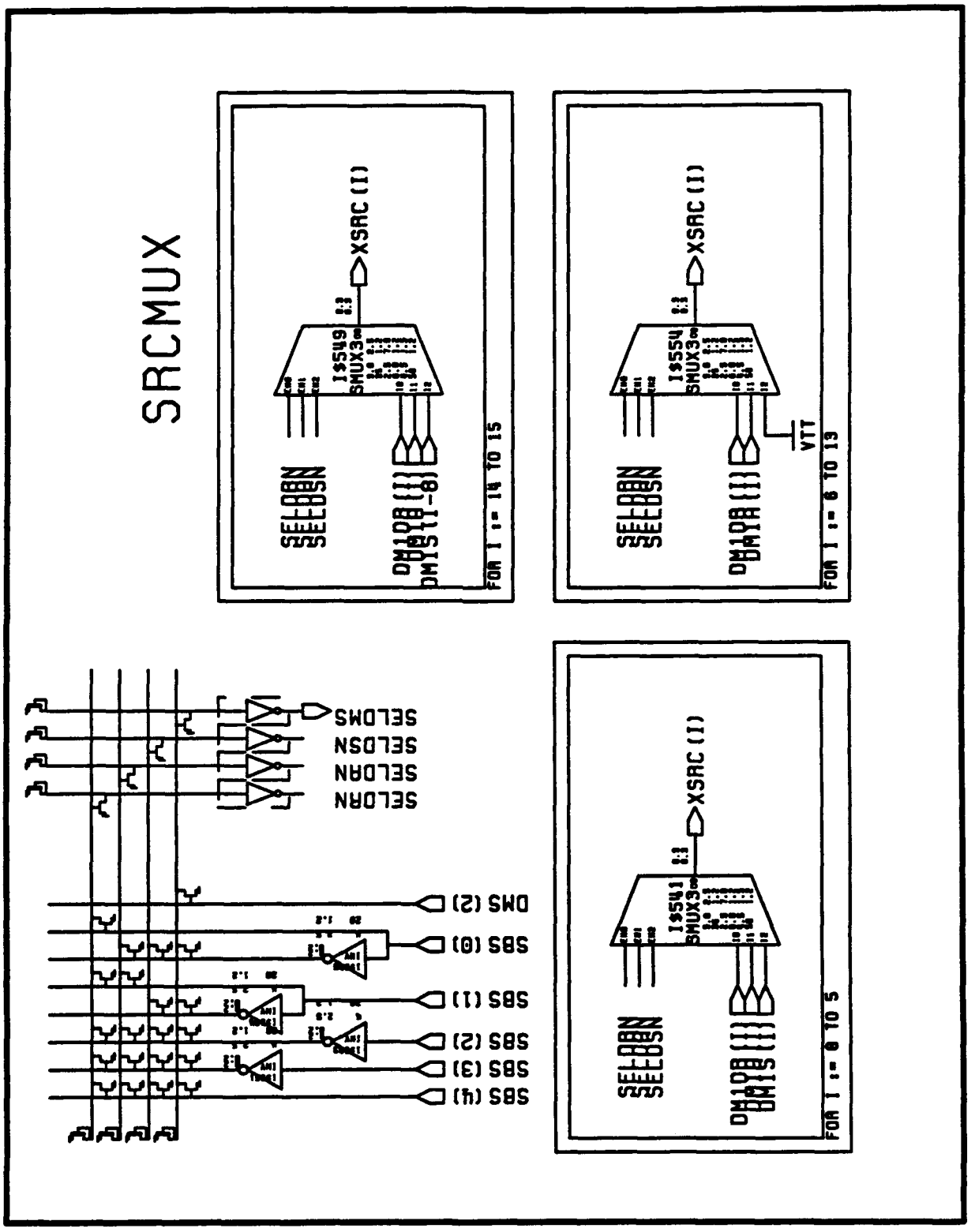

0.3
0.3
UXX
SMUX300
(DW) (DL)
(EW) (EL)
(DW1)(DL1)
(EW1)(EL1)
(DW2)(DL2)
(EW2)(EL2)
EN0
EN1 SMUX3
smux3.bin
EN2
I0
I1
I2
ena
ena
ena
in
in
in

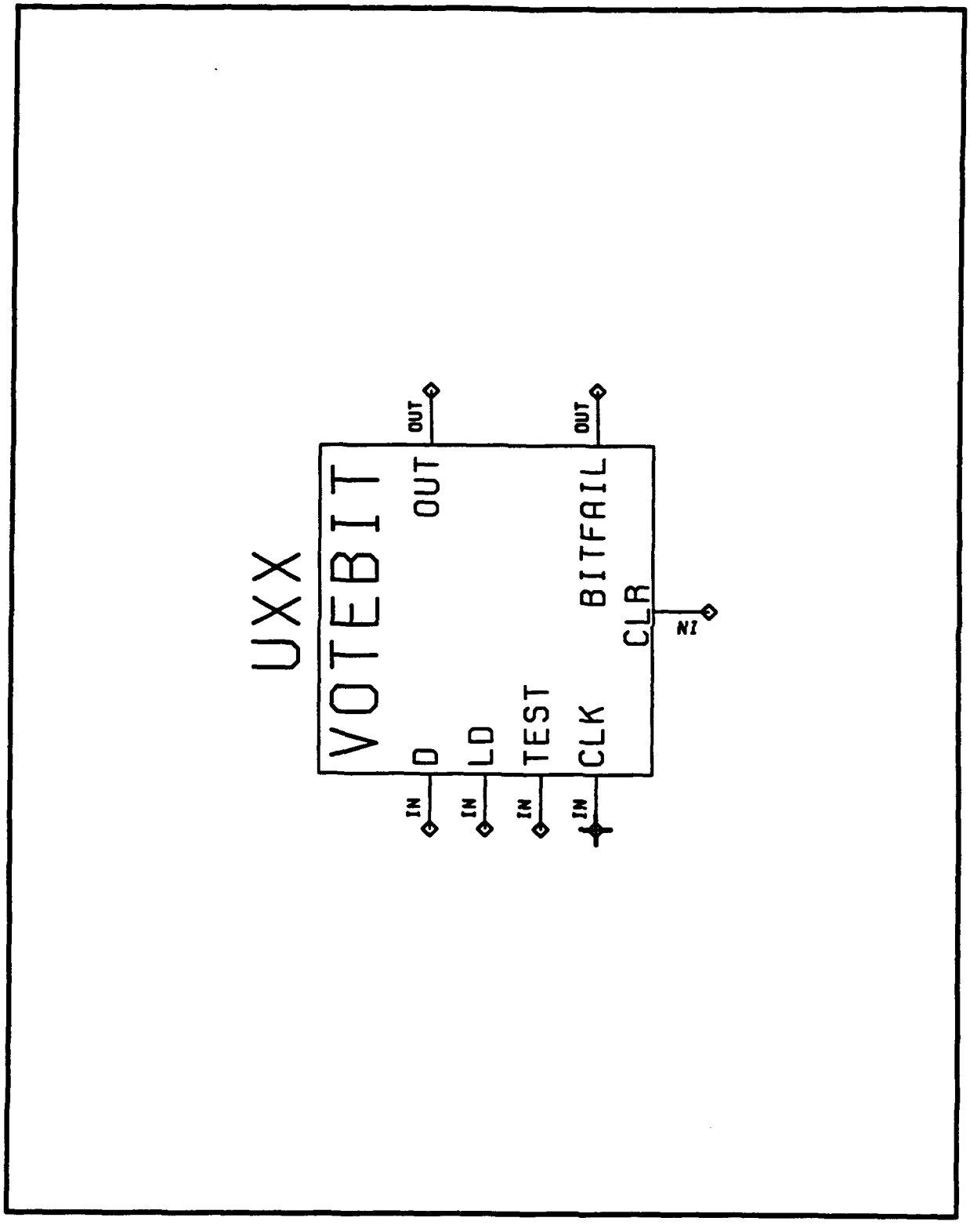

SMUX3
O0
CG
VTT
EN2
EN1
EN0
I2
I1
I0

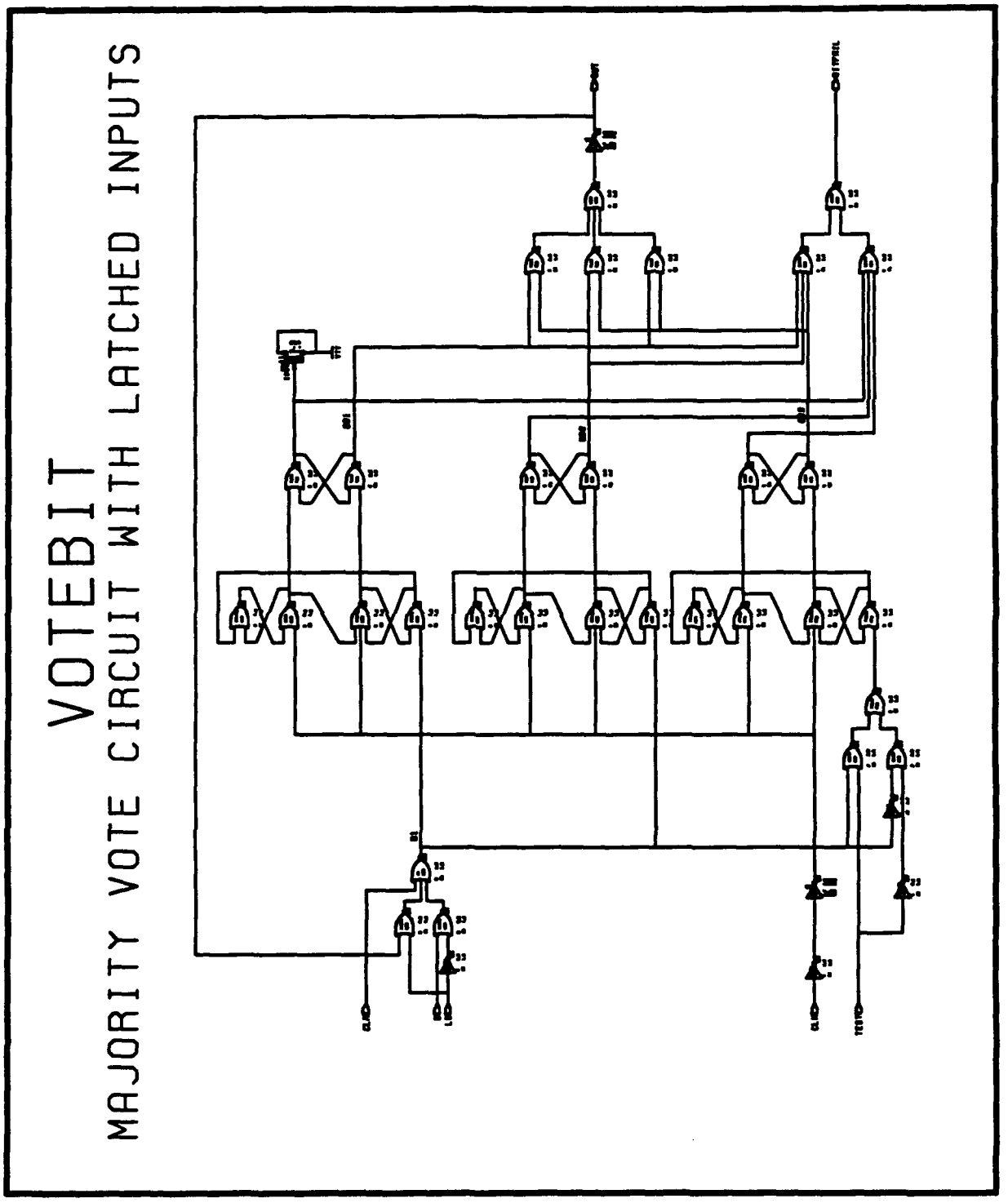

0.3
0.3
EN0
EN1 SMUX4
smux4.bin
EN2
EN3
UXX
SMUX4 00
(OW) (OL)
(EW) (EL)
I0 (OW1) (OL1)
I1 (EW1) (EL1)
I2 (OW2) (OL2)
I3 (EW2) (EL2)

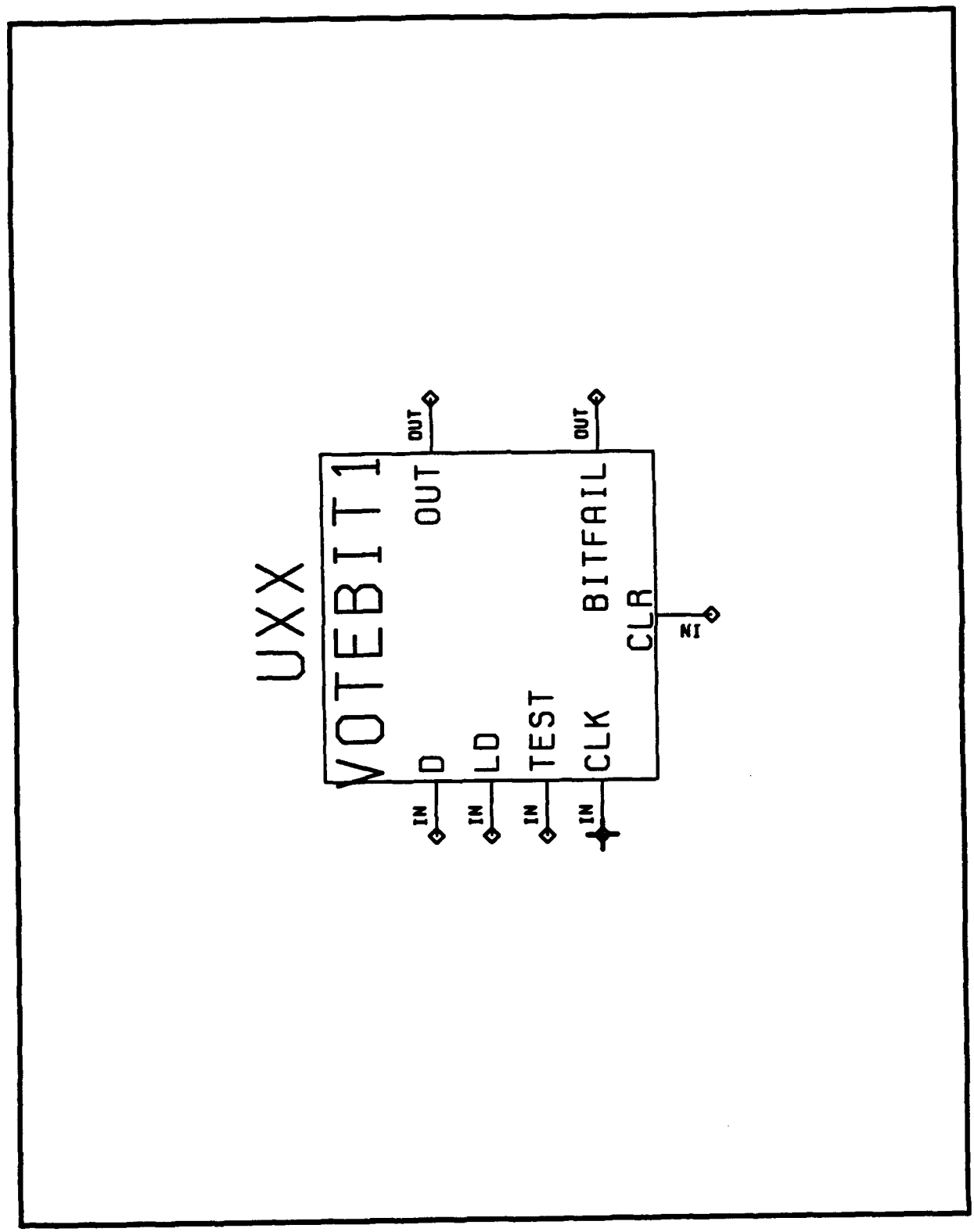

SMUX4
O0
CG
VTT
EN3
EN2
EN1
EN0
I3
I2
I1
I0

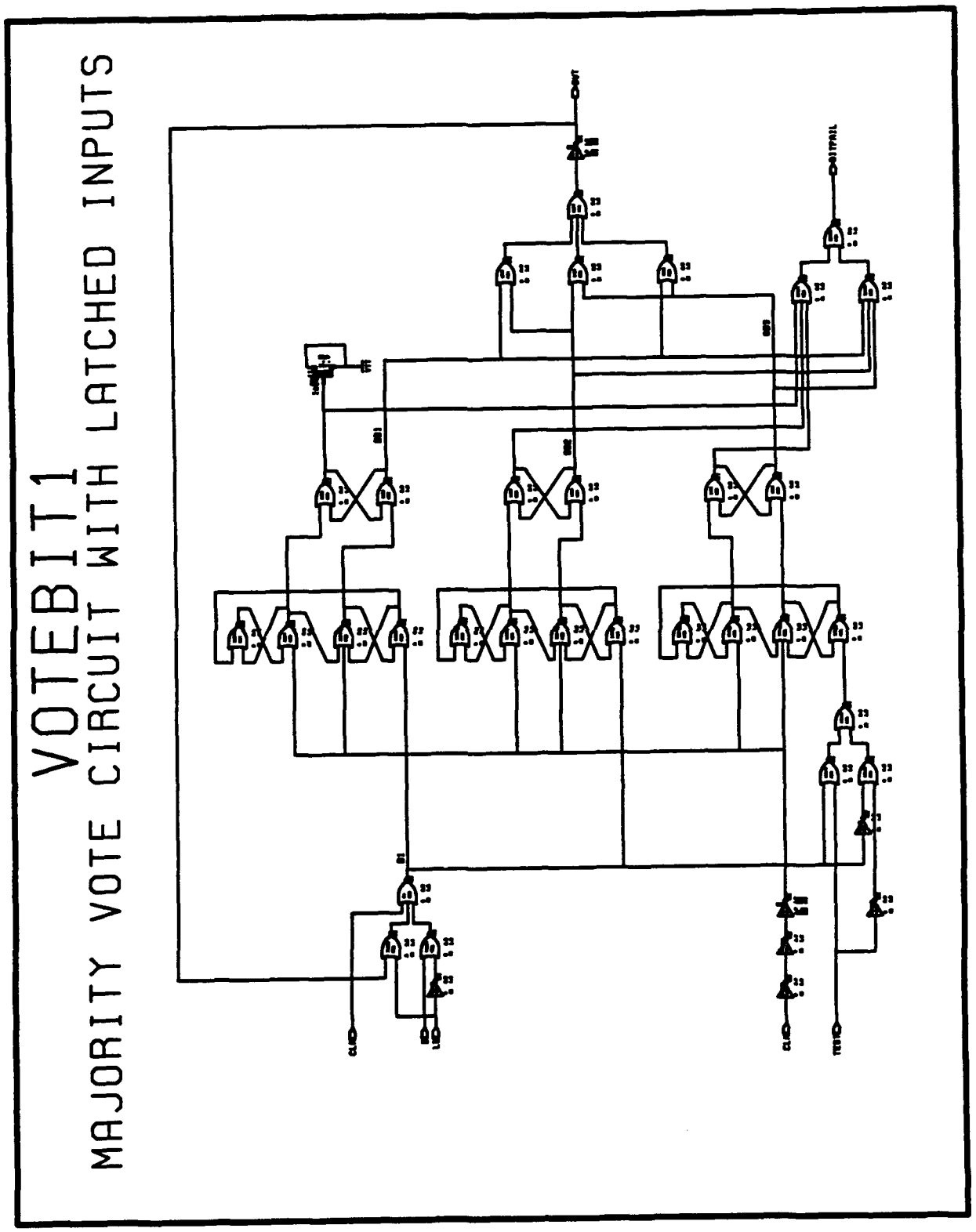

SRCMUX
UXX
DM1A (15:0)
DM1DR (15:0)
DM1S (7:0)
SBS (4:0)
DMS (2)
SELDMS
XSRC (15:0)
in
in
in
in
in
out
out

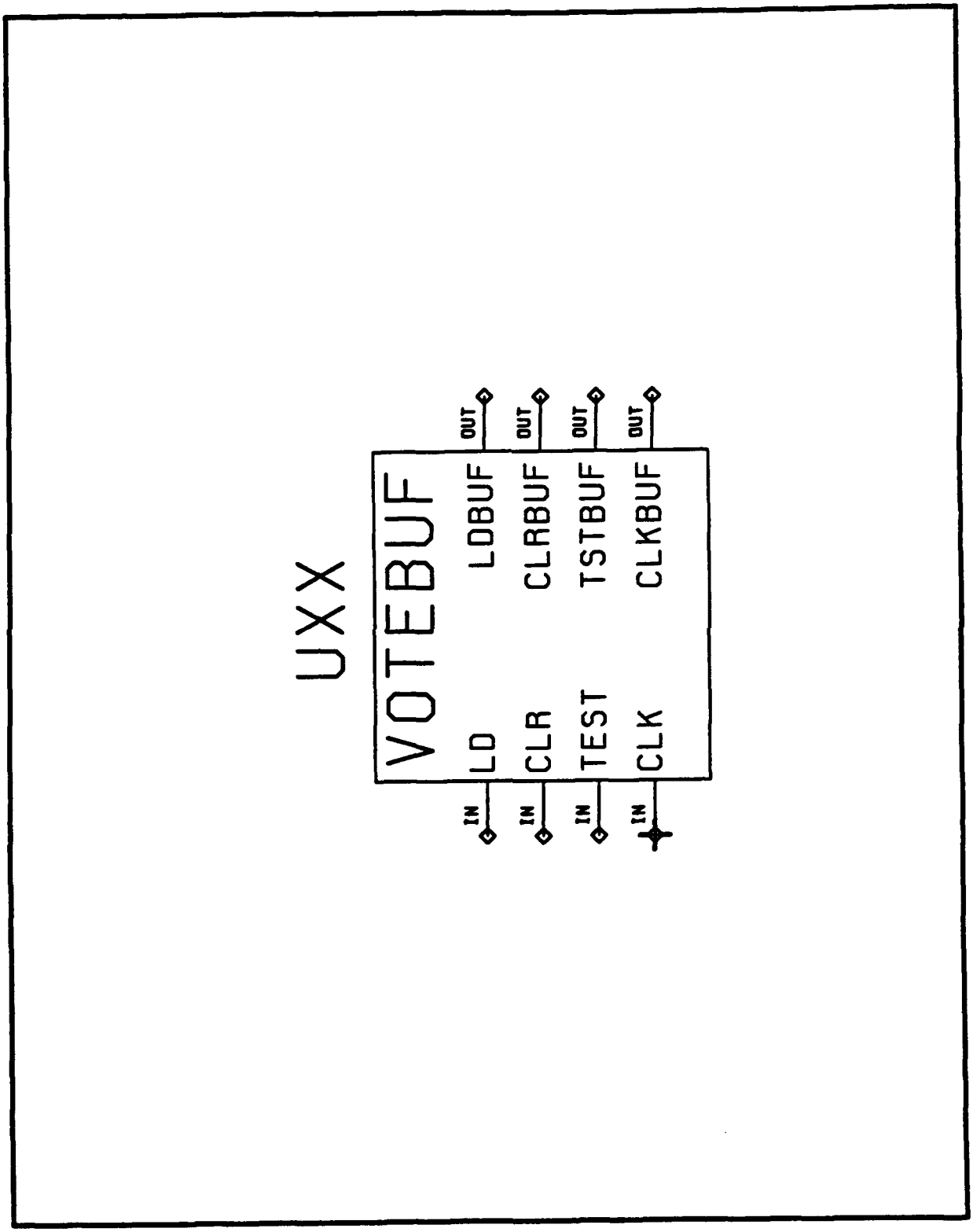

SRCMUX
XSRC(1)
I$549
SMUX3
SELOBSN
SELEBSN
DMIS(8-11)
FOR I := 14 TO 15
XSRC(1)
I$554
SMUX3
VTT
SELOBSN
SELEBSN
DMIS(8)
FOR I := 6 TO 13
XSRC(1)
I$541
SMUX3
SELOBSN
SELEBSN
DMIS(8)
FOR I := 0 TO 5
SELORN
SELORN
SELOSN
SELOMS
DMS(2)
SBS(0)
SBS(1)
SBS(2)
SBS(3)
SBS(4)

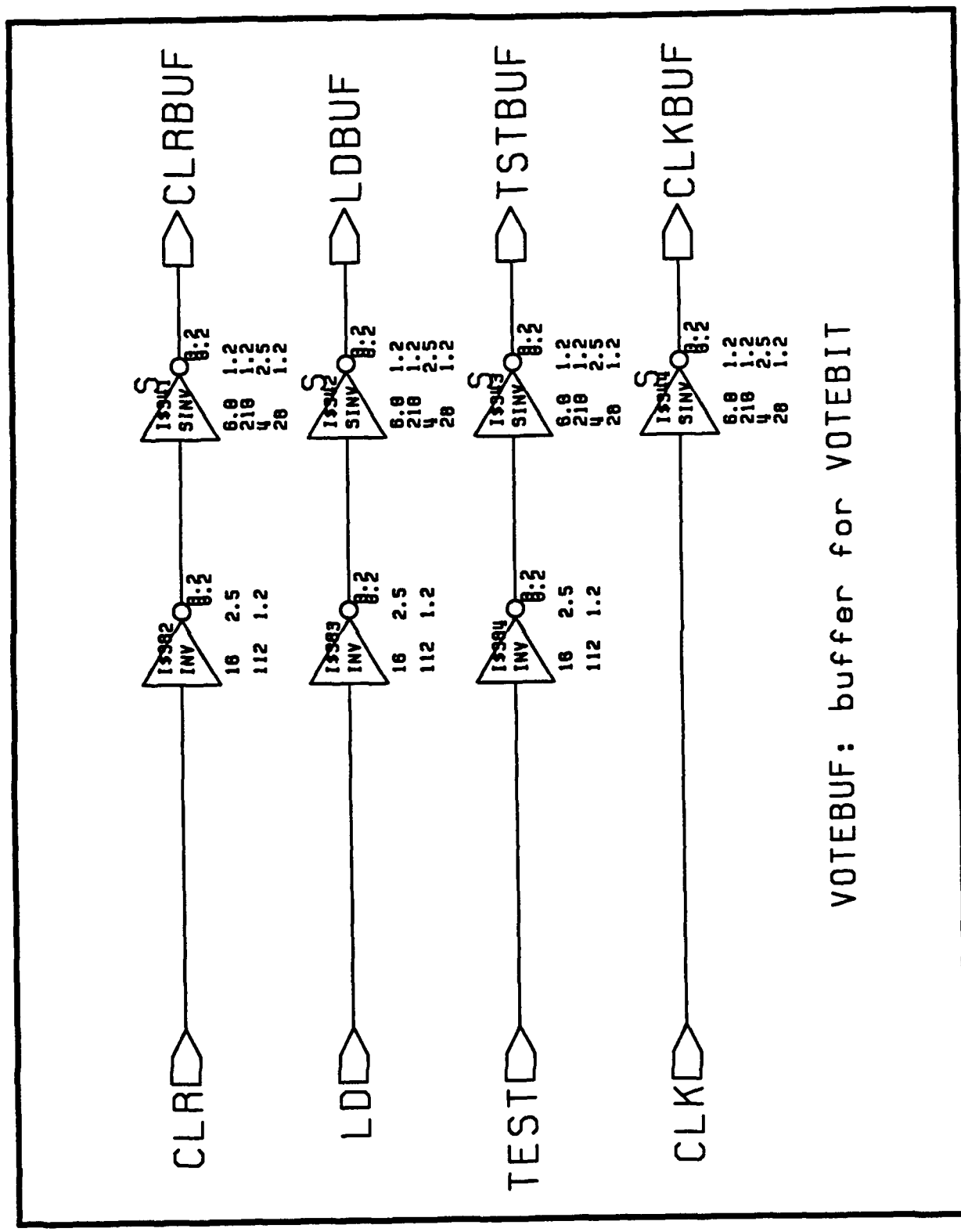

UXX
VOTEBIT
OUT
OUT
BITFAIL
CLR
NI
D
LD
TEST
CLK
IN
IN
IN
IN

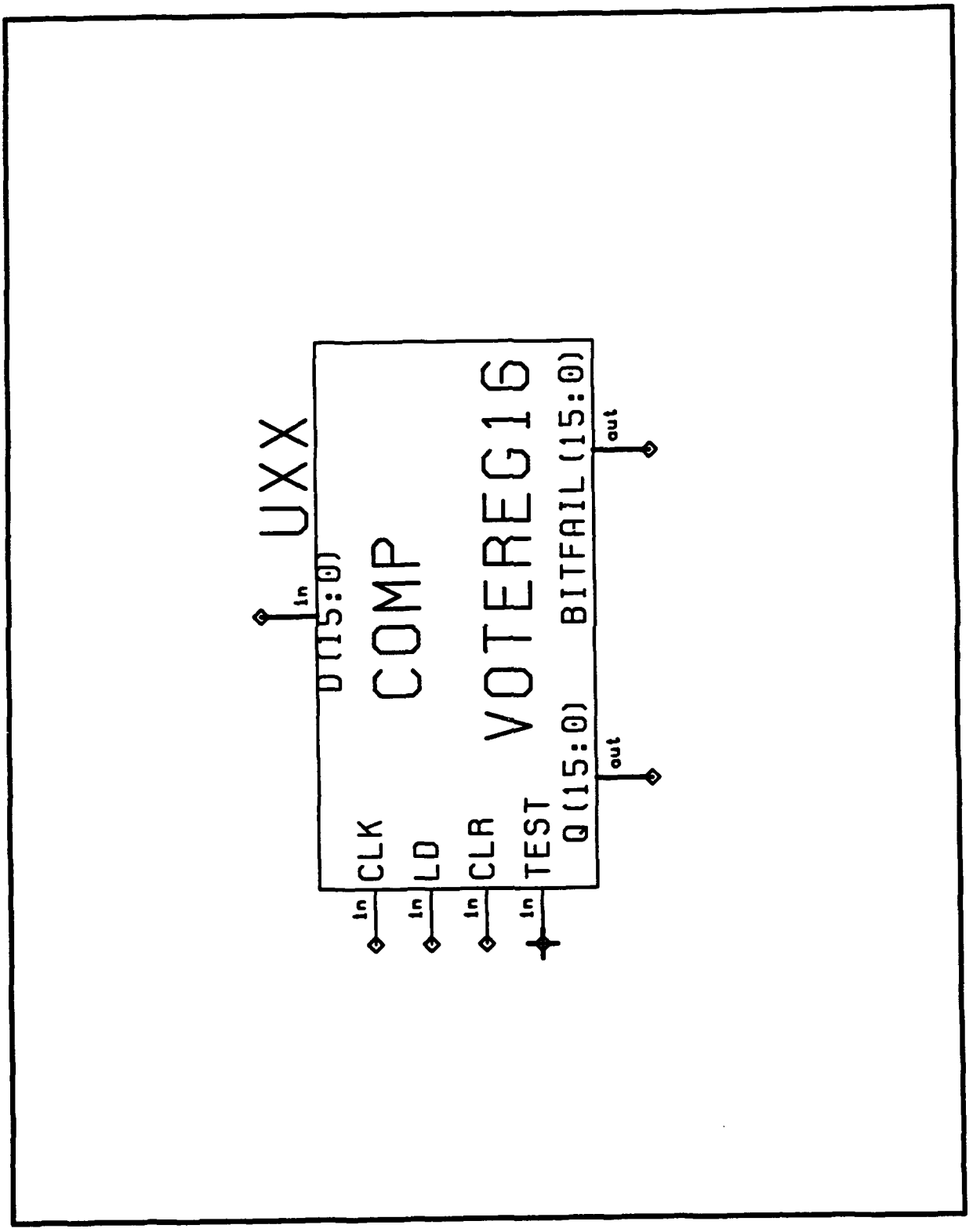

VOTEBIT
MAJORITY VOTE CIRCUIT WITH LATCHED INPUTS

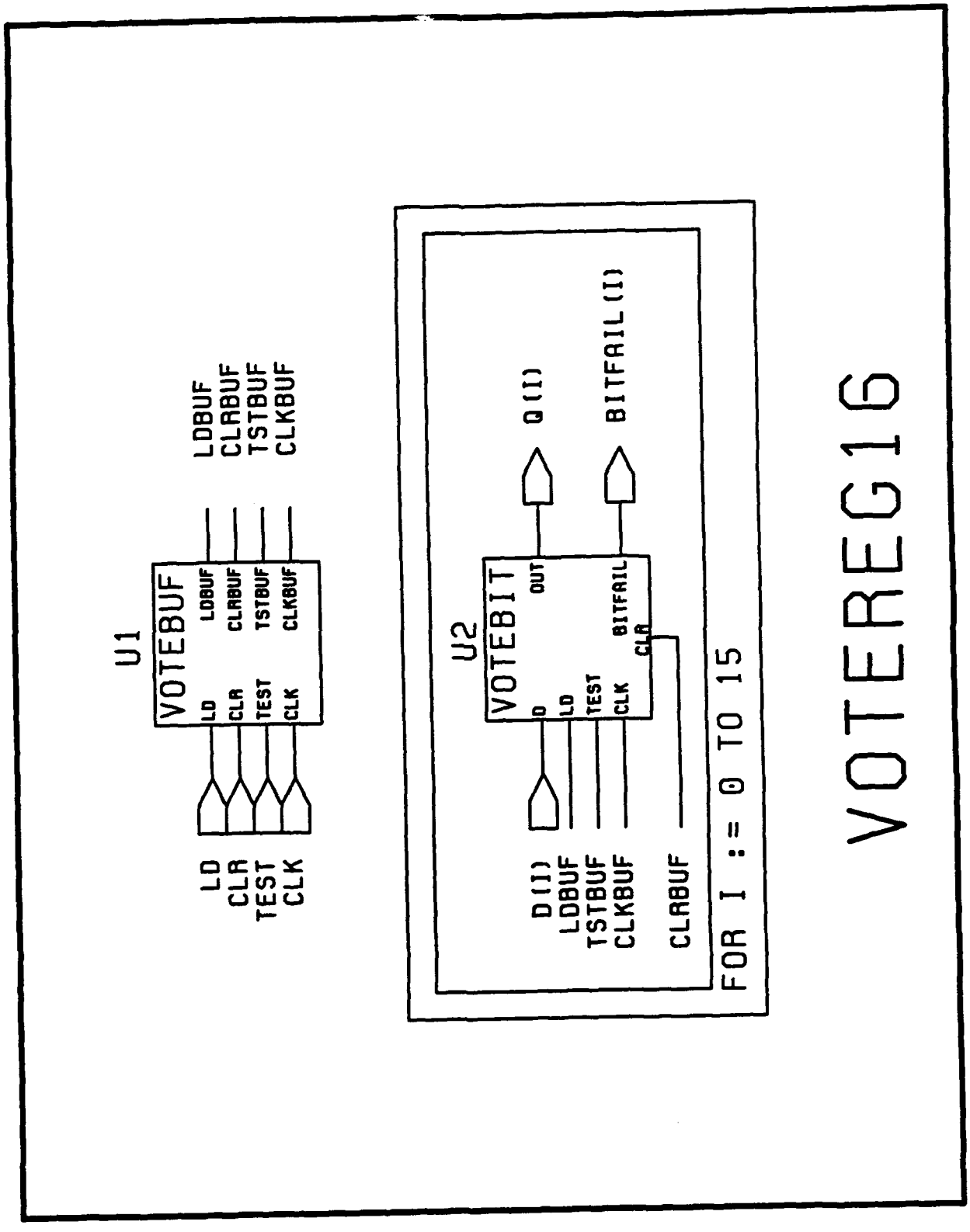

UXX
VOTEBIT1
OUT
BITFAIL
CLR
D
LD
TEST
CLK
OUT
OUT
NI
IN
IN
IN
IN

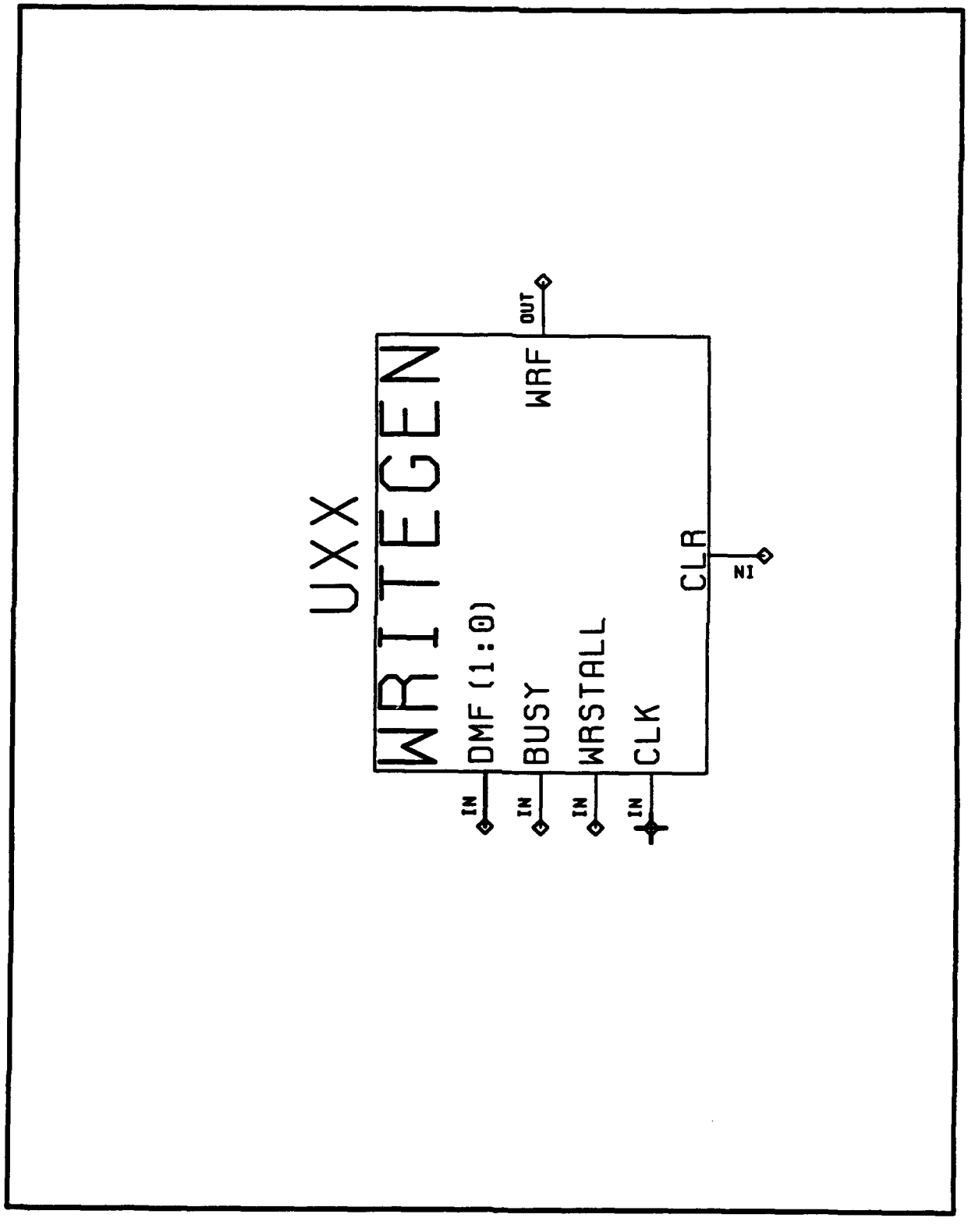

VOTEBIT1
MAJORITY VOTE CIRCUIT WITH LATCHED INPUTS

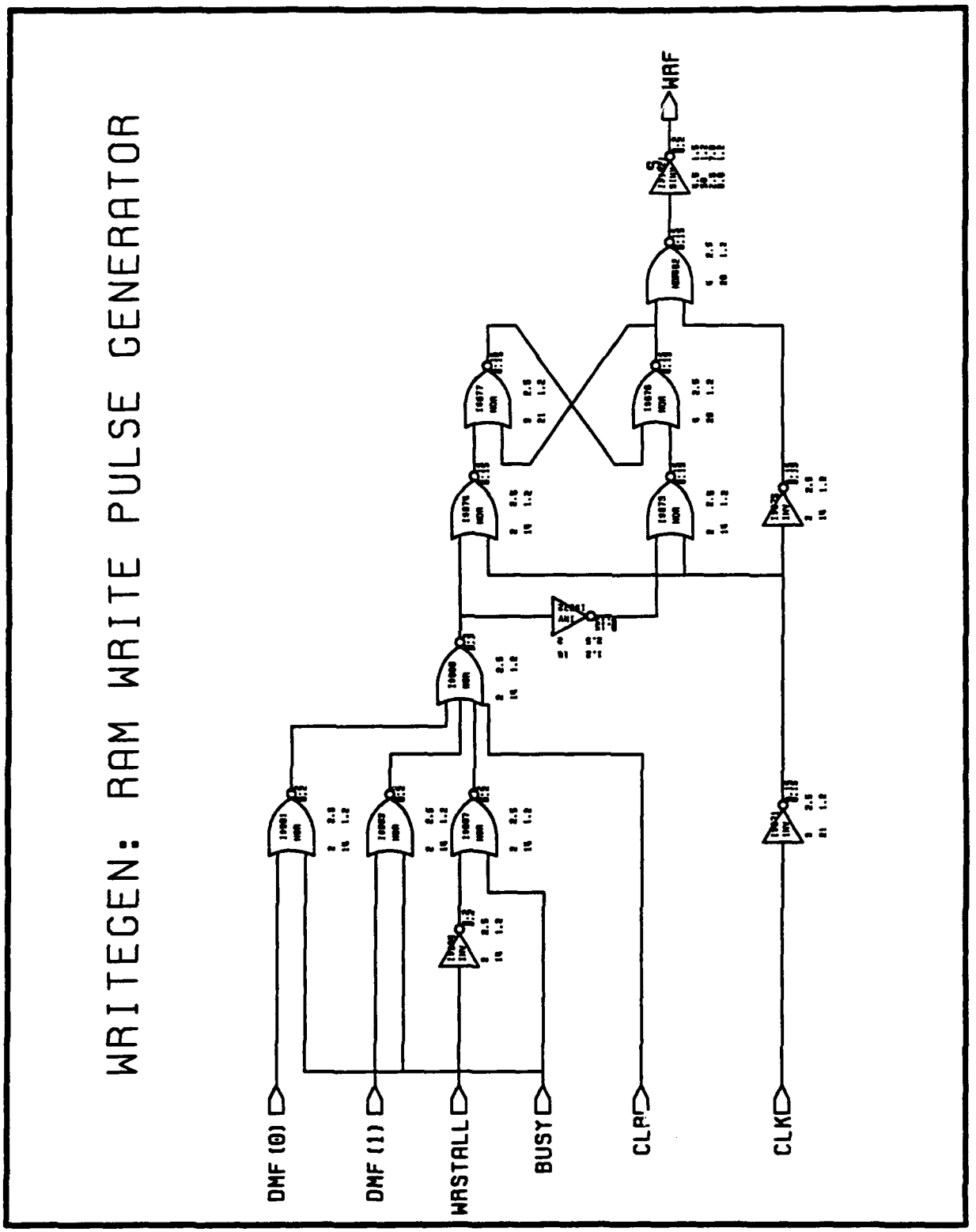

UXX
VOTEBUF
LD
CLR
TEST
CLK
LDBUF
CLRBUF
TSTBUF
CLKBUF
IN
IN
IN
IN
OUT
OUT
OUT
OUT

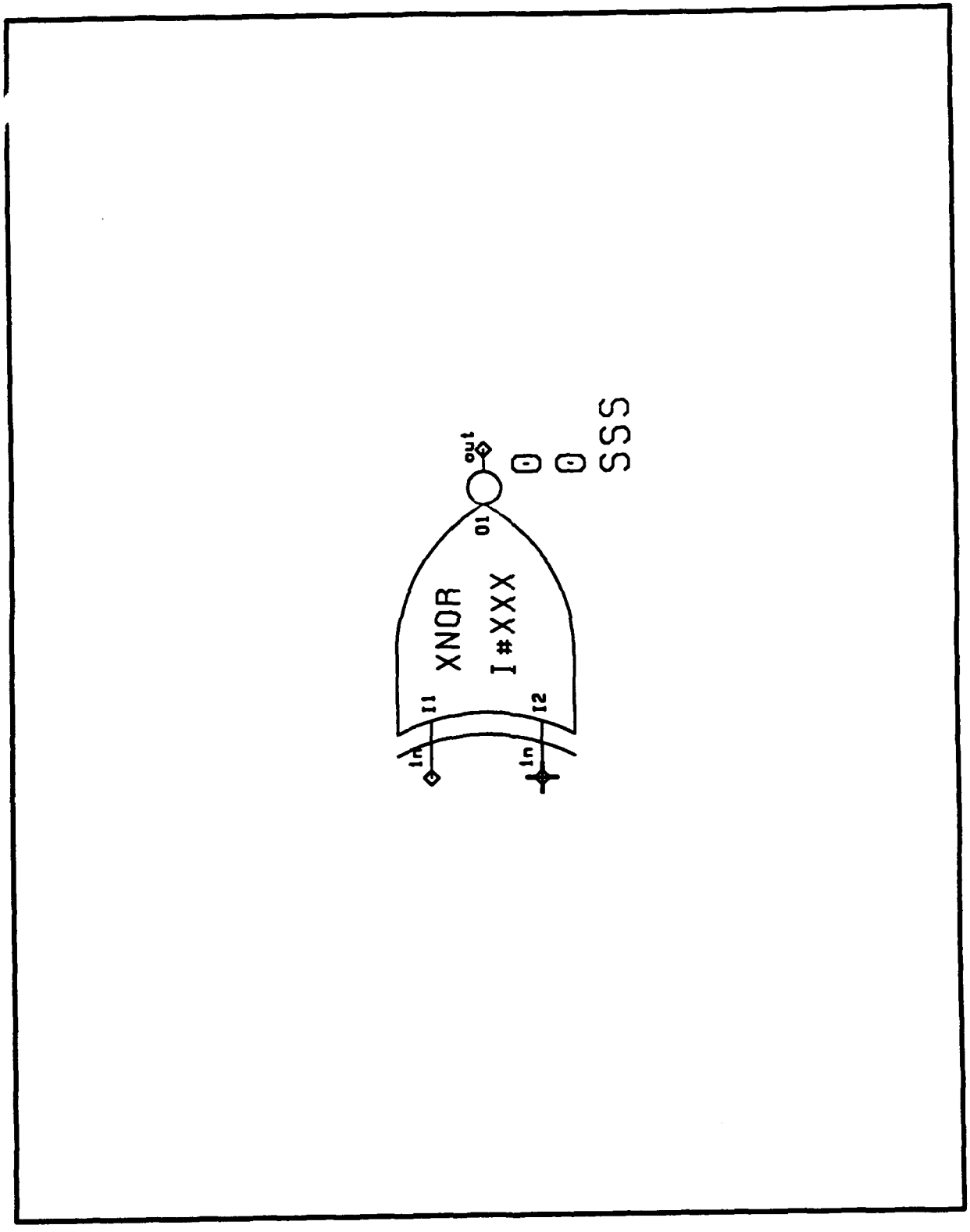

CLRBUF
LDBUF
TSTBUF
CLKBUF
I3381
I3382
I3383
I3384
I3385
I3386
I3387
I3388
SINV
INV
8.2
6.0 1.2
21.0 1.2
4 2.5
28 1.2
16 2.5
112 1.2
CLR
LD
TEST
CLK
VOTEBUF: buffer for VOTEBIT

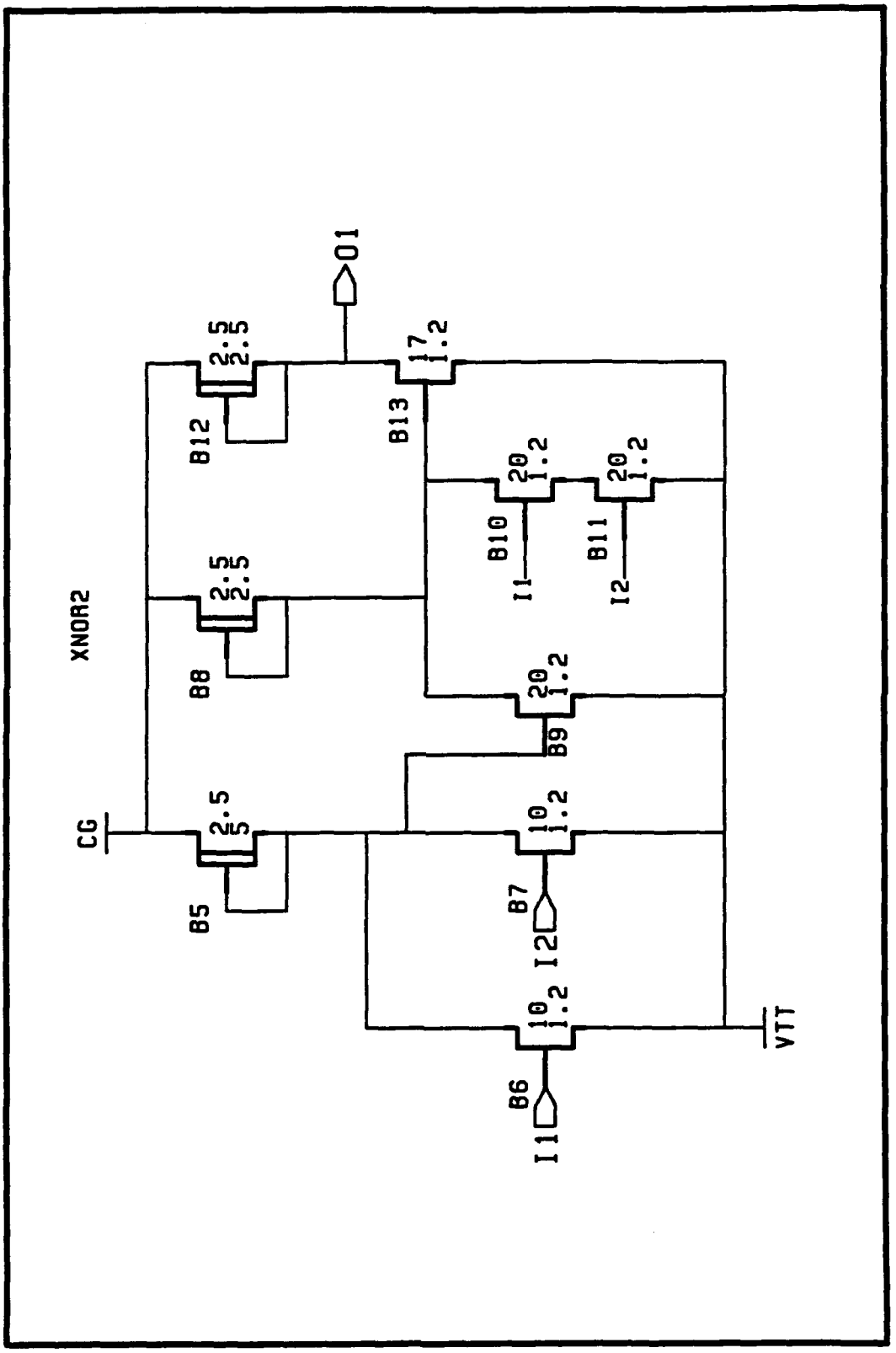

UXX
COMP
VOTEREG16
D(15:0)
in
CLK
LD
CLR
TEST
Q(15:0)
BITFAIL(15:0)
out
out

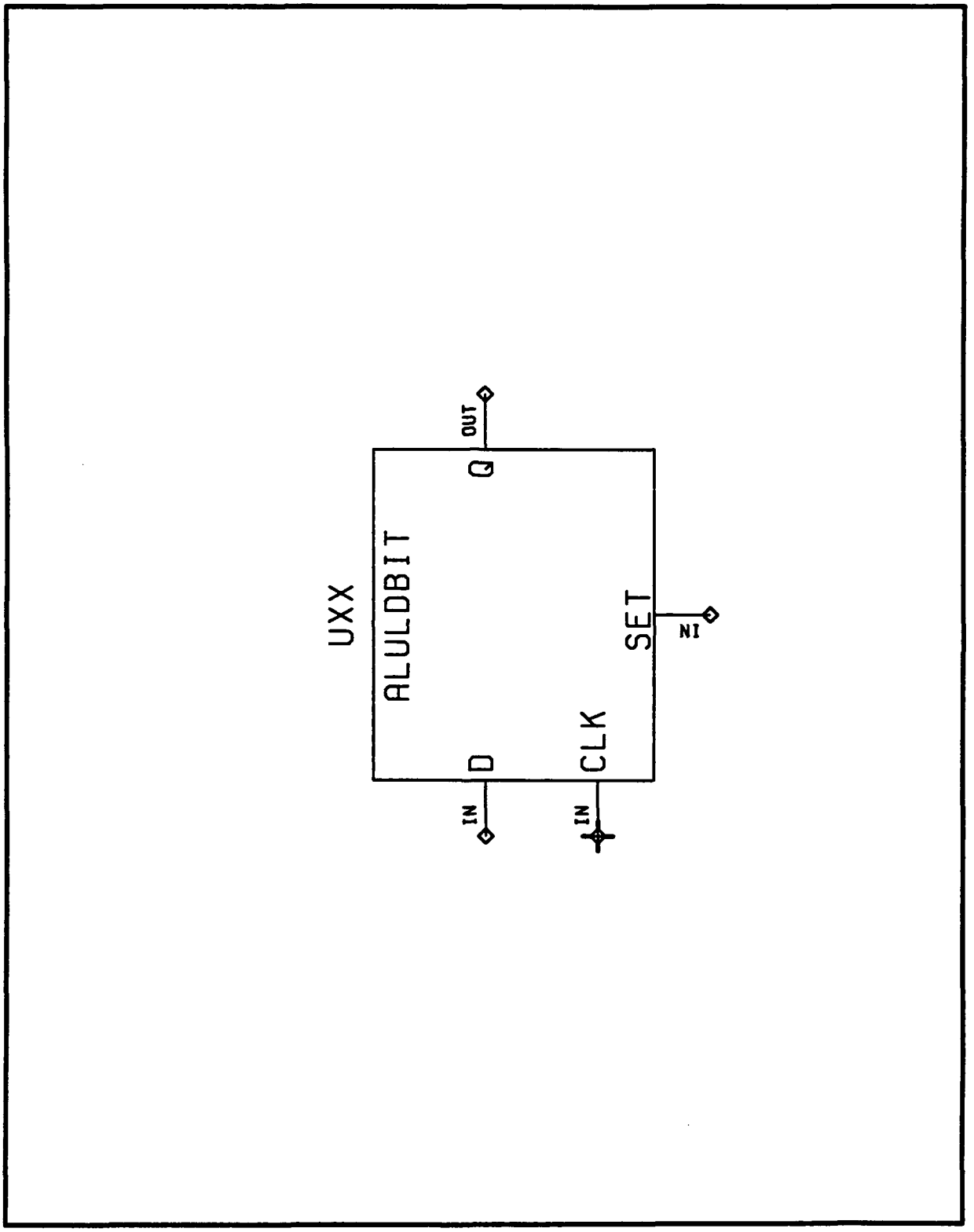

VOTEREG16
FOR I := 0 TO 15
U1
VOTEBUF
LD
CLR
TEST
CLK
LDBUF
CLRBUF
TSTBUF
CLKBUF
U2
VOTEBIT
D
LD
TEST
CLK
CLR
OUT
BITFAIL
Q(I)
BITFAIL(I)
D(I)
LDBUF
TSTBUF
CLKBUF
CLRBUF

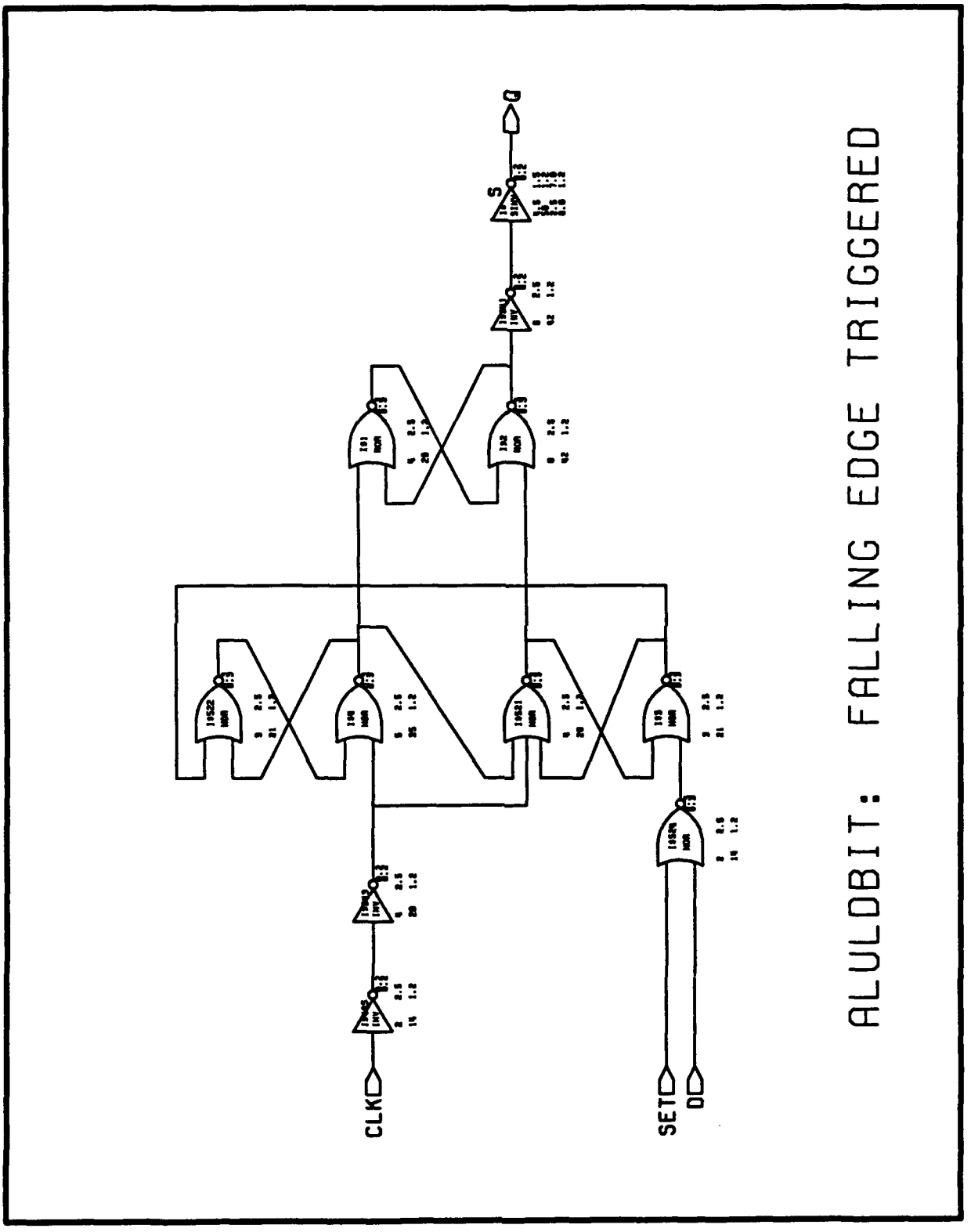

UXX
WRITEGEN
OUT
WRF
CLR
NI
DMF(1:0)
BUSY
WRSTALL
CLK
IN
IN
IN
IN

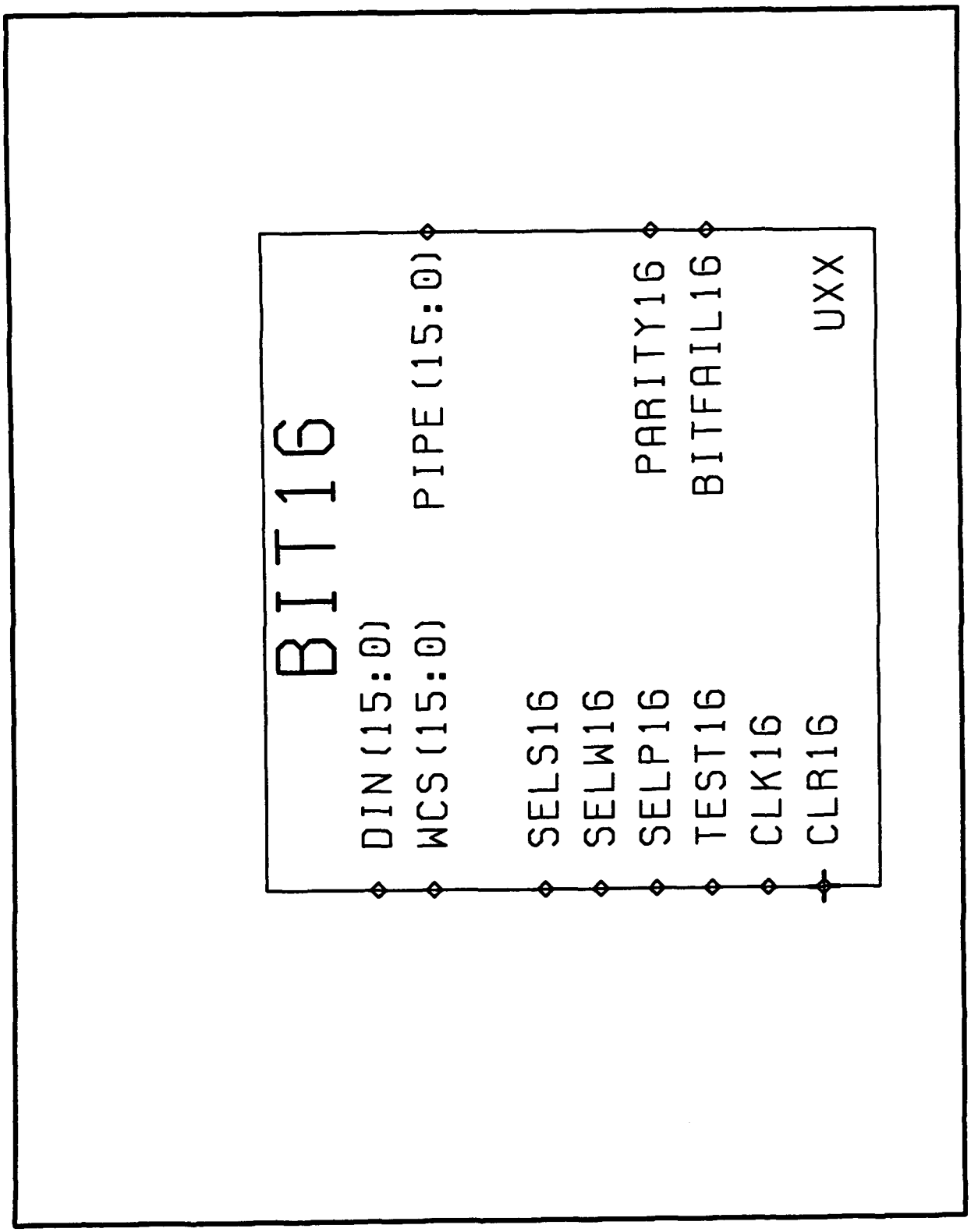

WRITEGEN: RAM WRITE PULSE GENERATOR
WAF
DMF (0)
DMF (1)
WRSTALL
BUSY
CLR
CLK

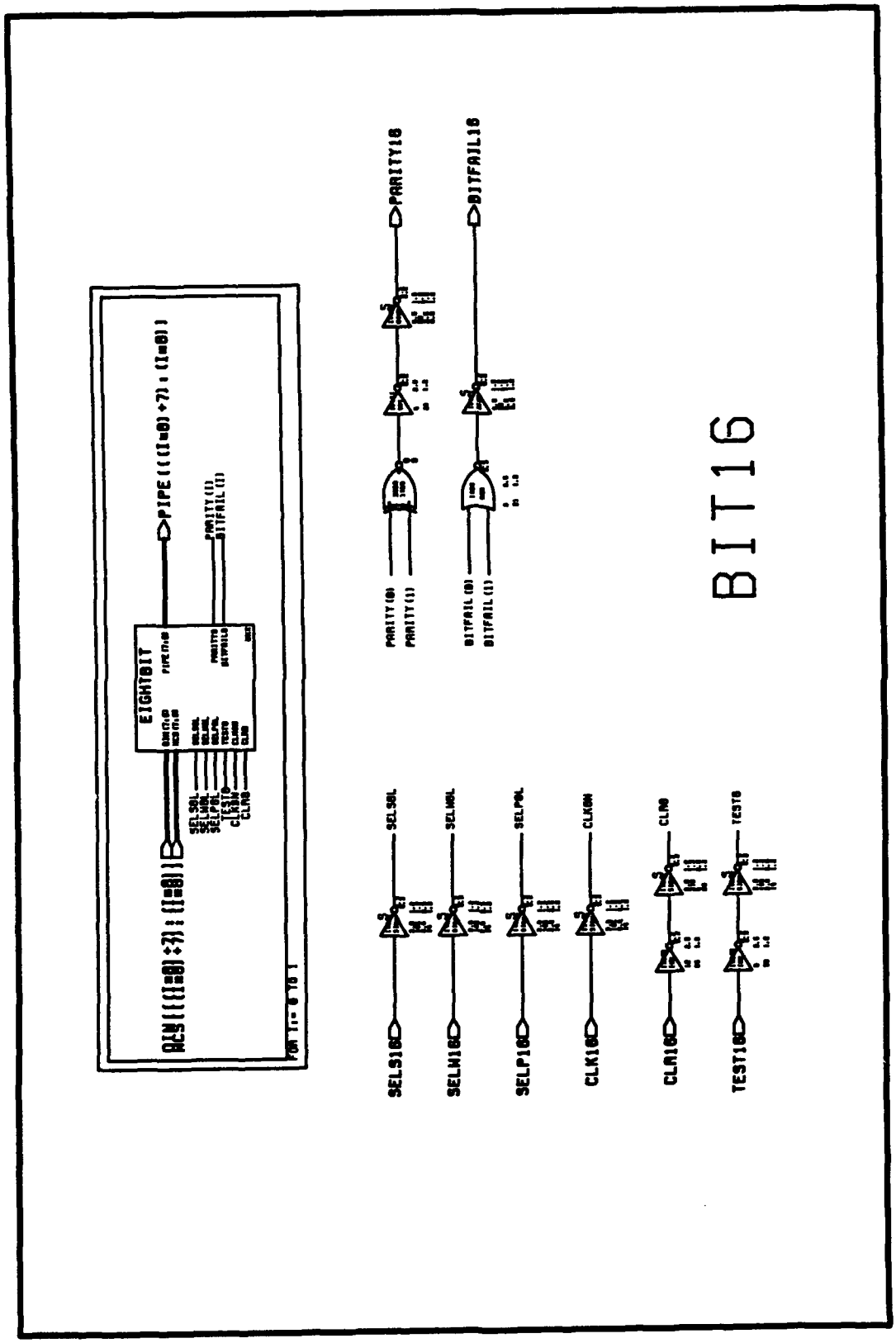

SSS
0
0
out
01
XNOR
I#XXX
I1
I2
In
In

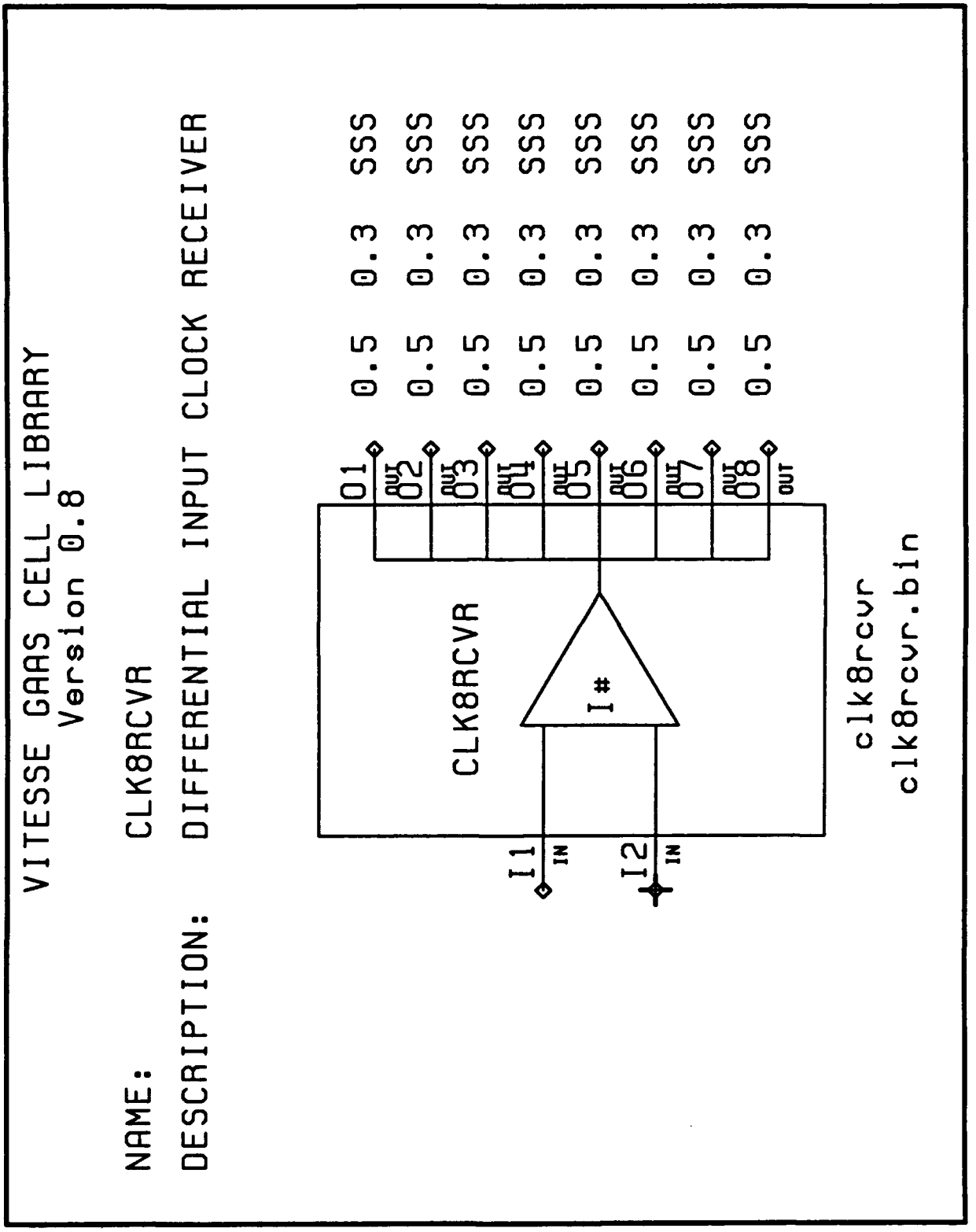

O1
B12
2.5
2.5
B13
17
1.2
B10
20
1.2
I1
B11
20
1.2
I2
XNOR2
B8
2.5
2.5
B9
20
1.2
CG
B5
2.5
2.5
B7
10
1.2
I2
B6
10
1.2
I1
VTT

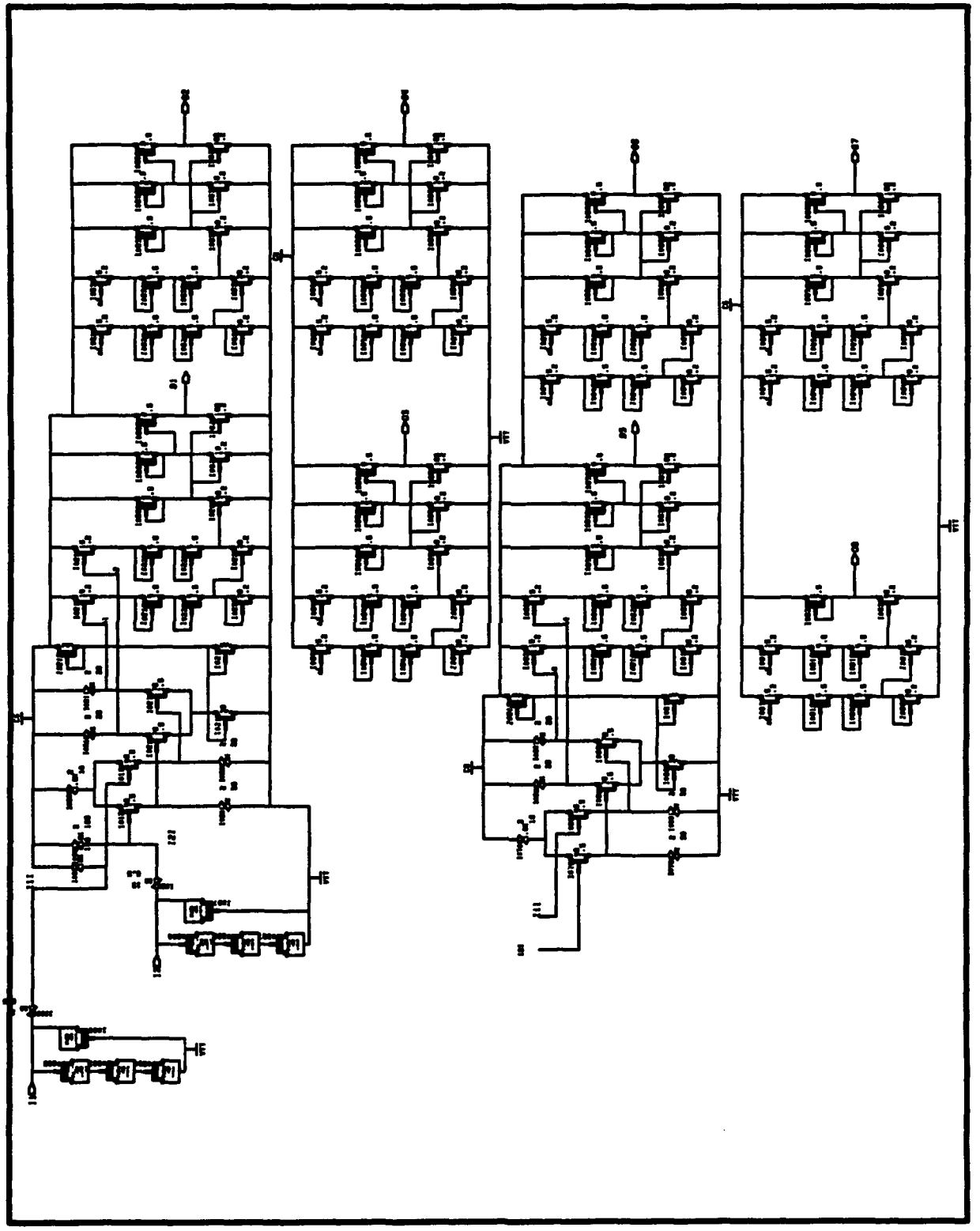

UXX
ALULDBIT
OUT
Q
SET
NI
D
CLK
IN
IN

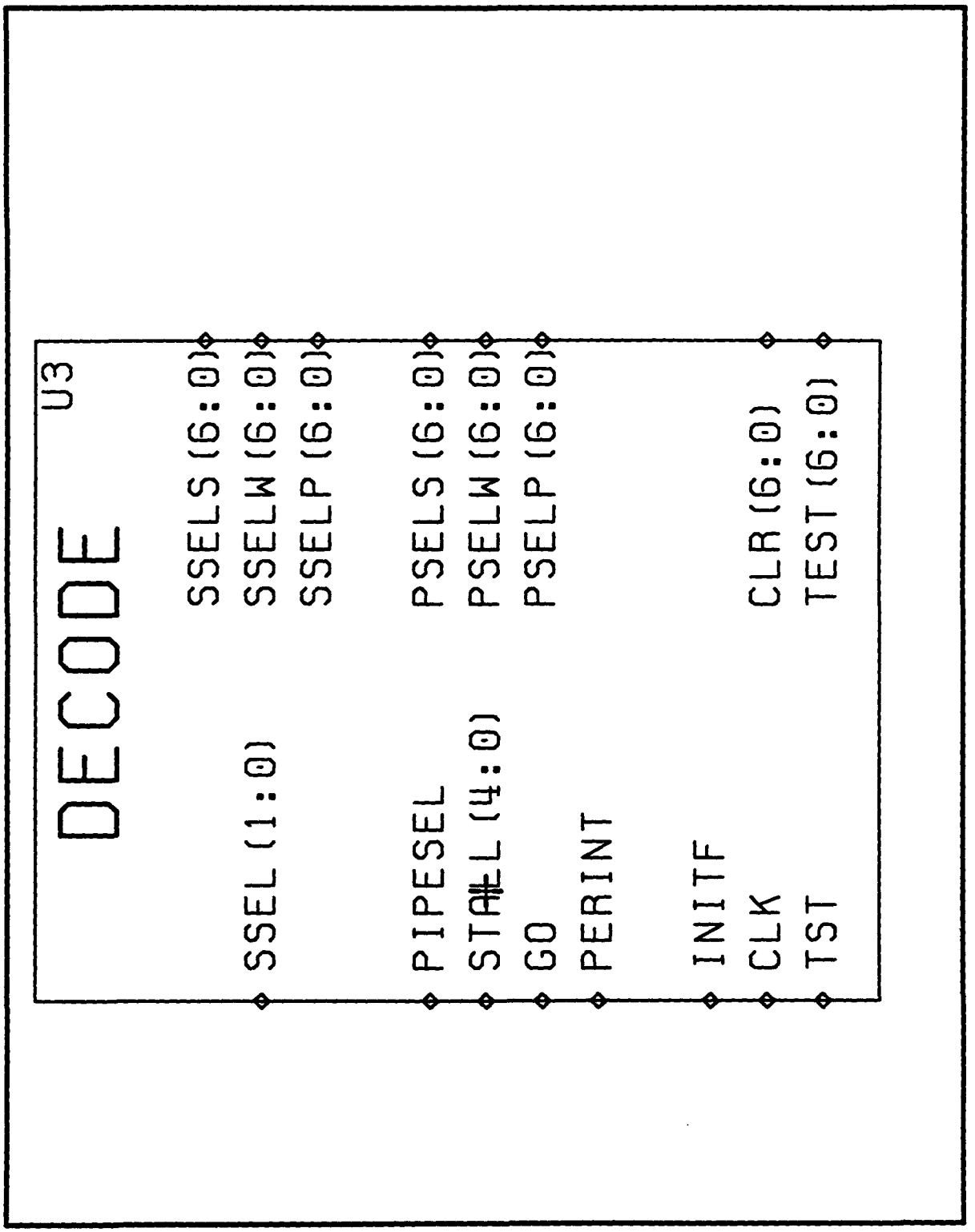

ALULOBIT: FALLING EDGE TRIGGERED
Q
S
CLK
SET
D

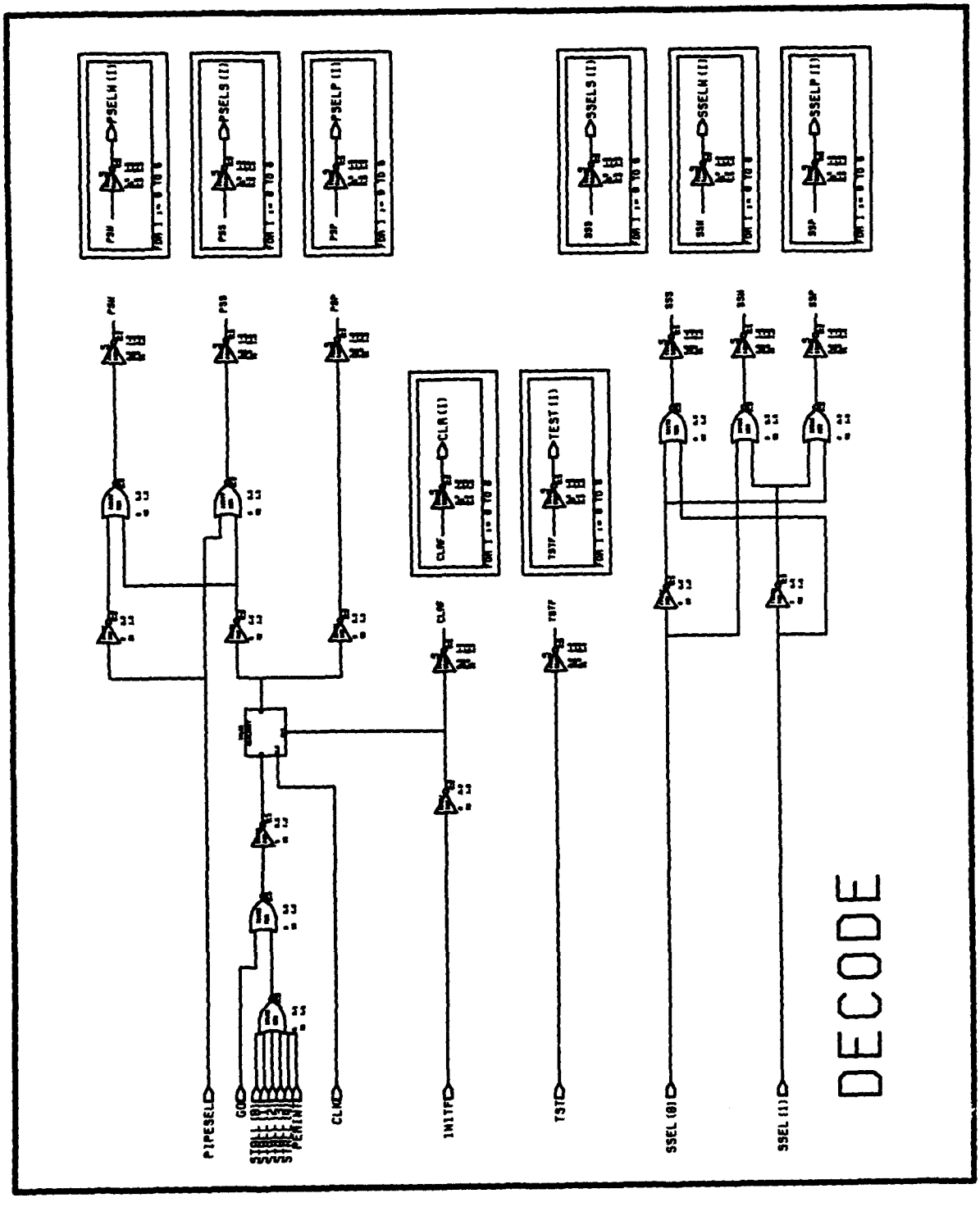

BIT16
DIN(15:0)
WCS(15:0)
PIPE(15:0)
SELS16
SELW16
SELP16
PARITY16
TEST16
BITFAIL16
CLK16
CLR16
UXX

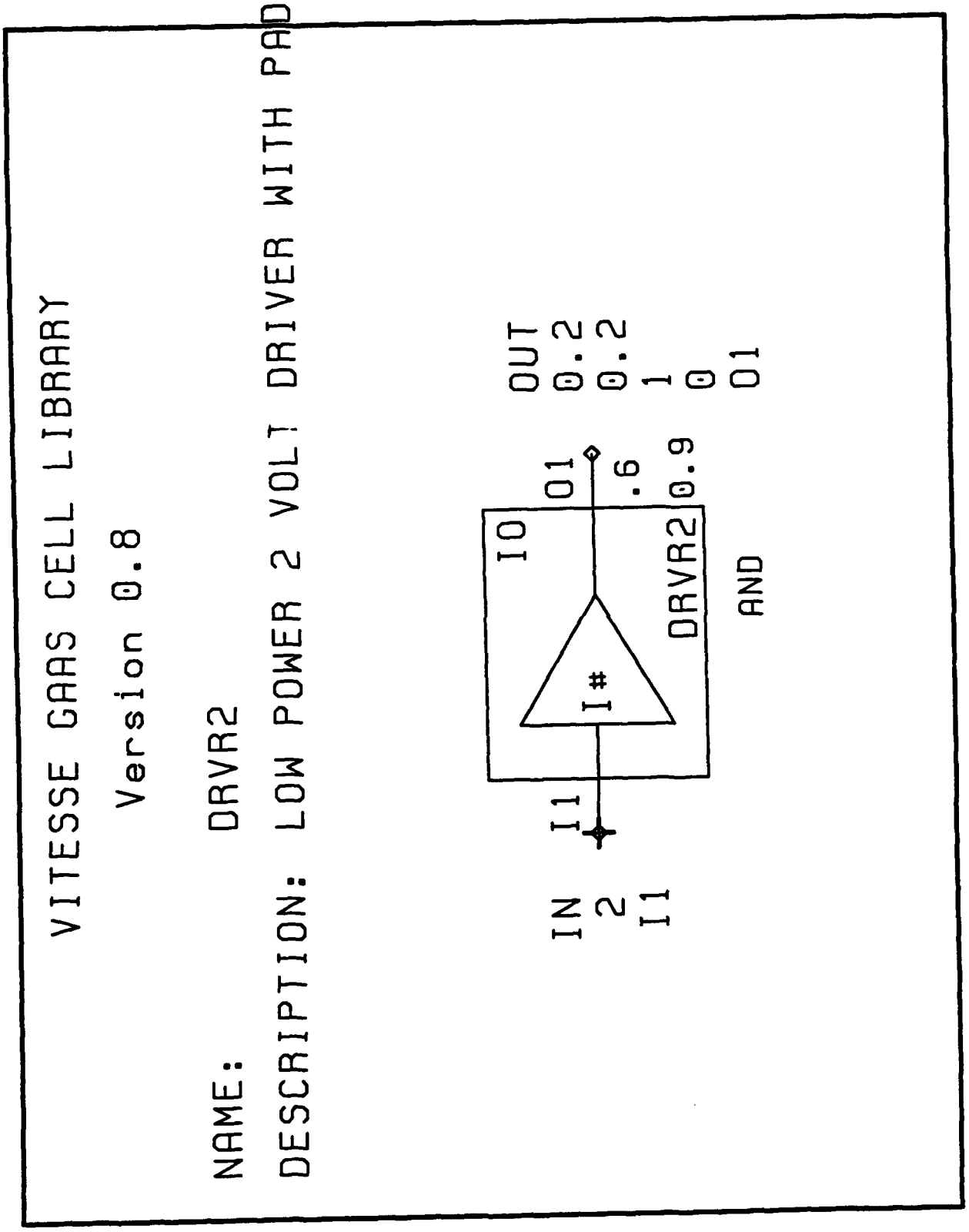

BIT16
EIGHTBIT
PARITY16
BITFAIL16
SEL316
SELN16
SELP16
CLK16
CLR16
TEST16

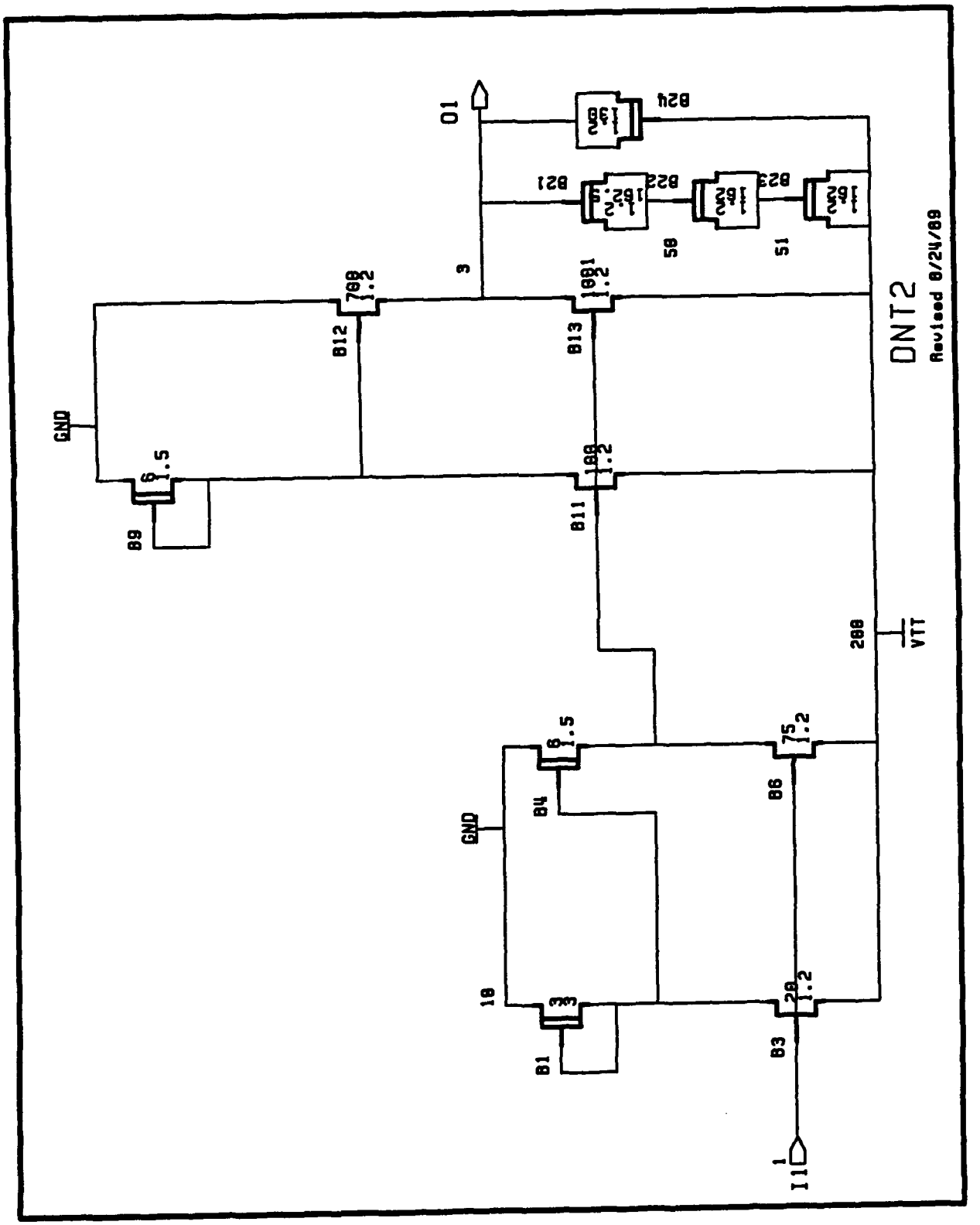

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: CLK8RCVR
DESCRIPTION: DIFFERENTIAL INPUT CLOCK RECEIVER
0.5 0.3 SSS
CLK8RCVR
I#
I1
I2
IN
OUT
clk8rcvr
clk8rcvr.bin

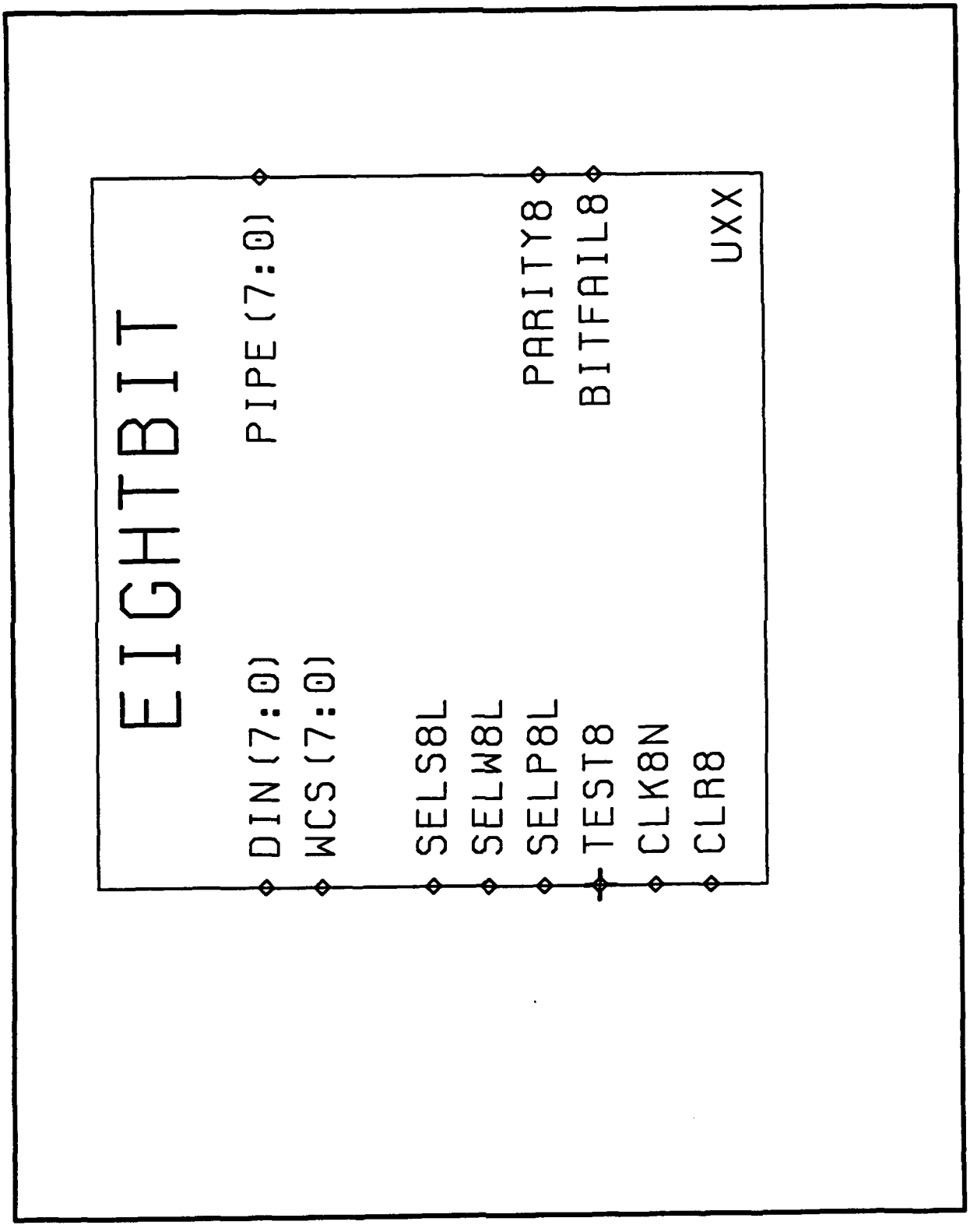


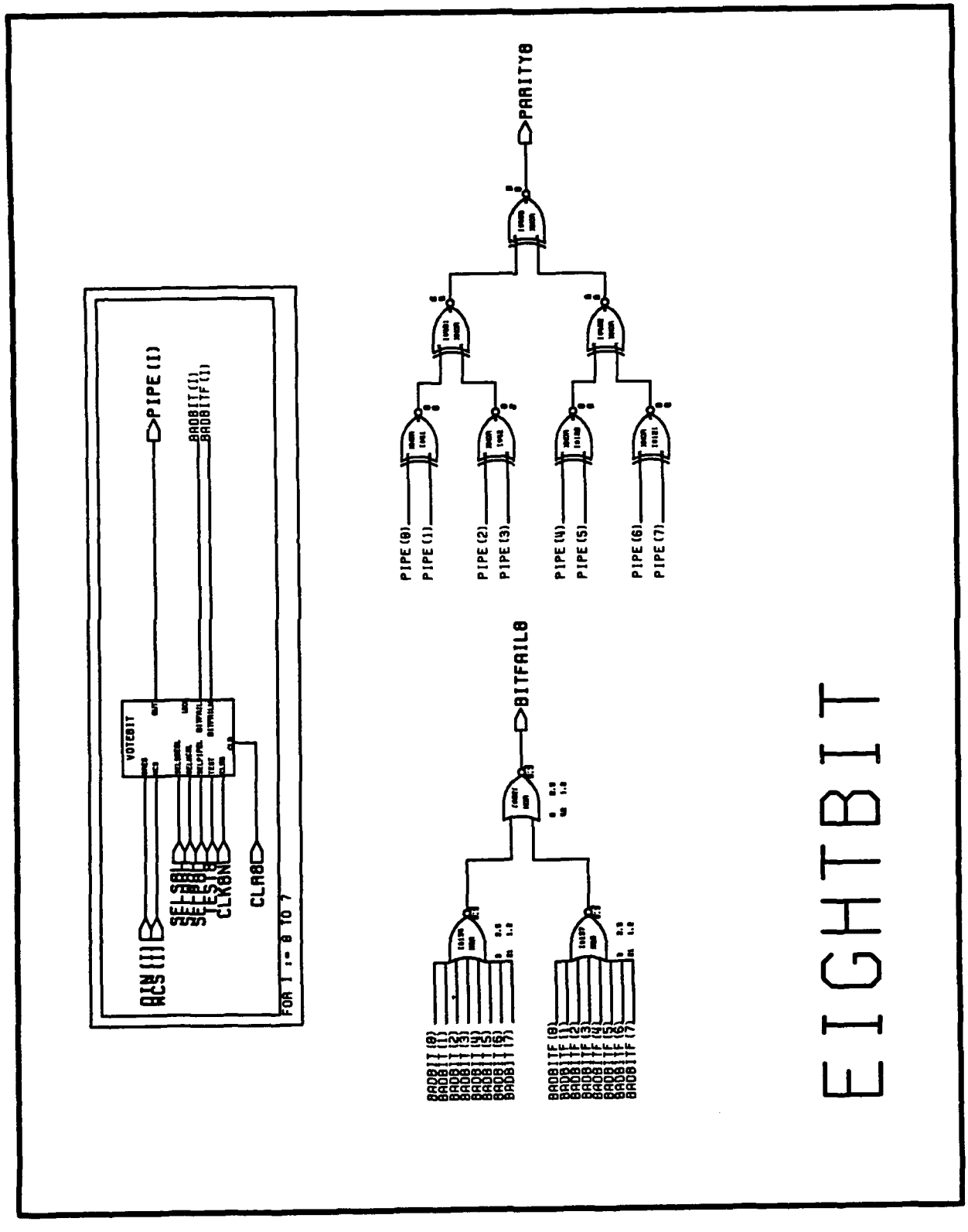

U3
DECODE
SSEL(1:0)
PIPESEL
STALL(4:0)
GO
PERINT
INITF
CLK
TST
SSELS(6:0)
SSELW(6:0)
SSELP(6:0)
PSELS(6:0)
PSELW(6:0)
PSELP(6:0)
CLR(6:0)
TEST(6:0)

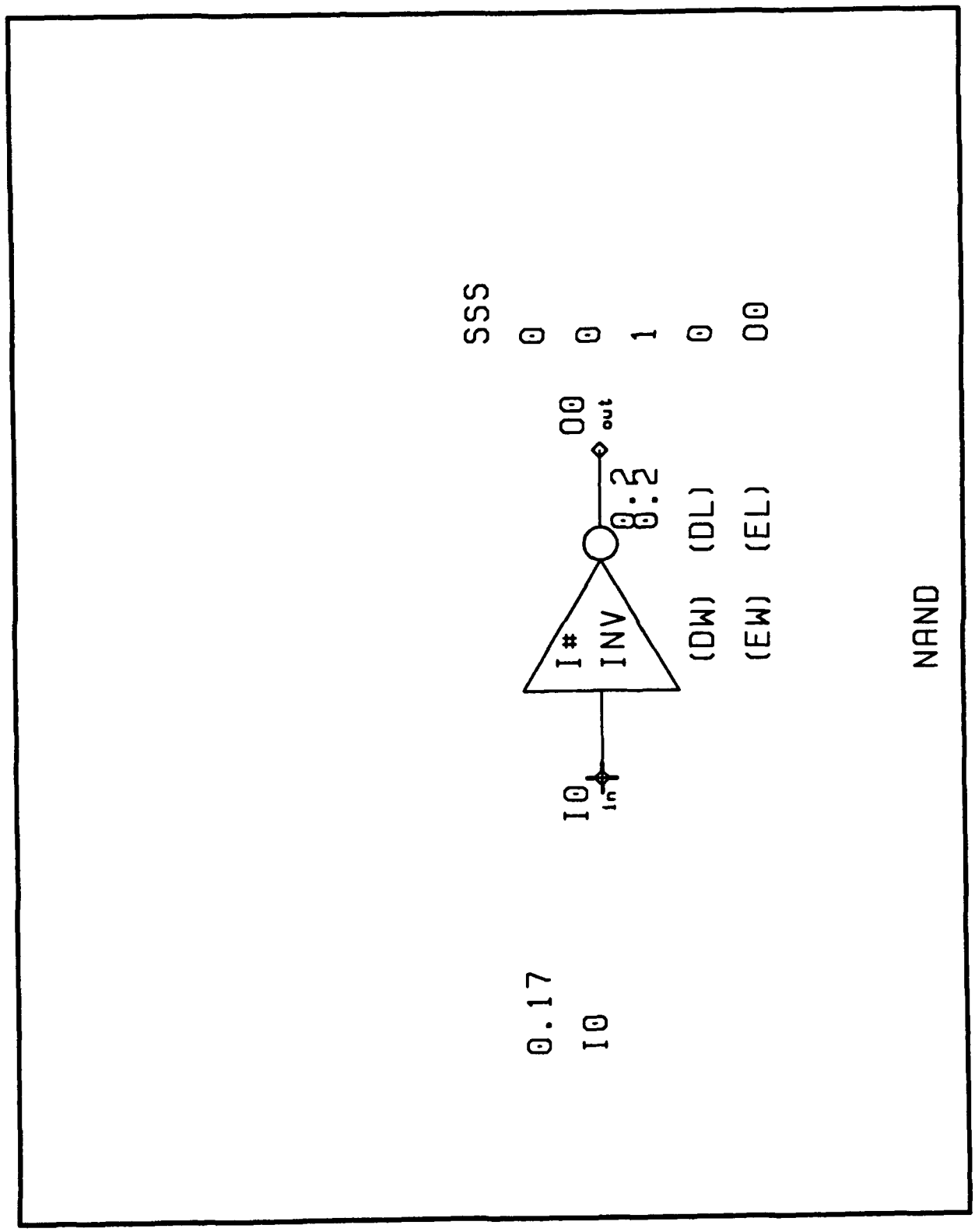

DECODE

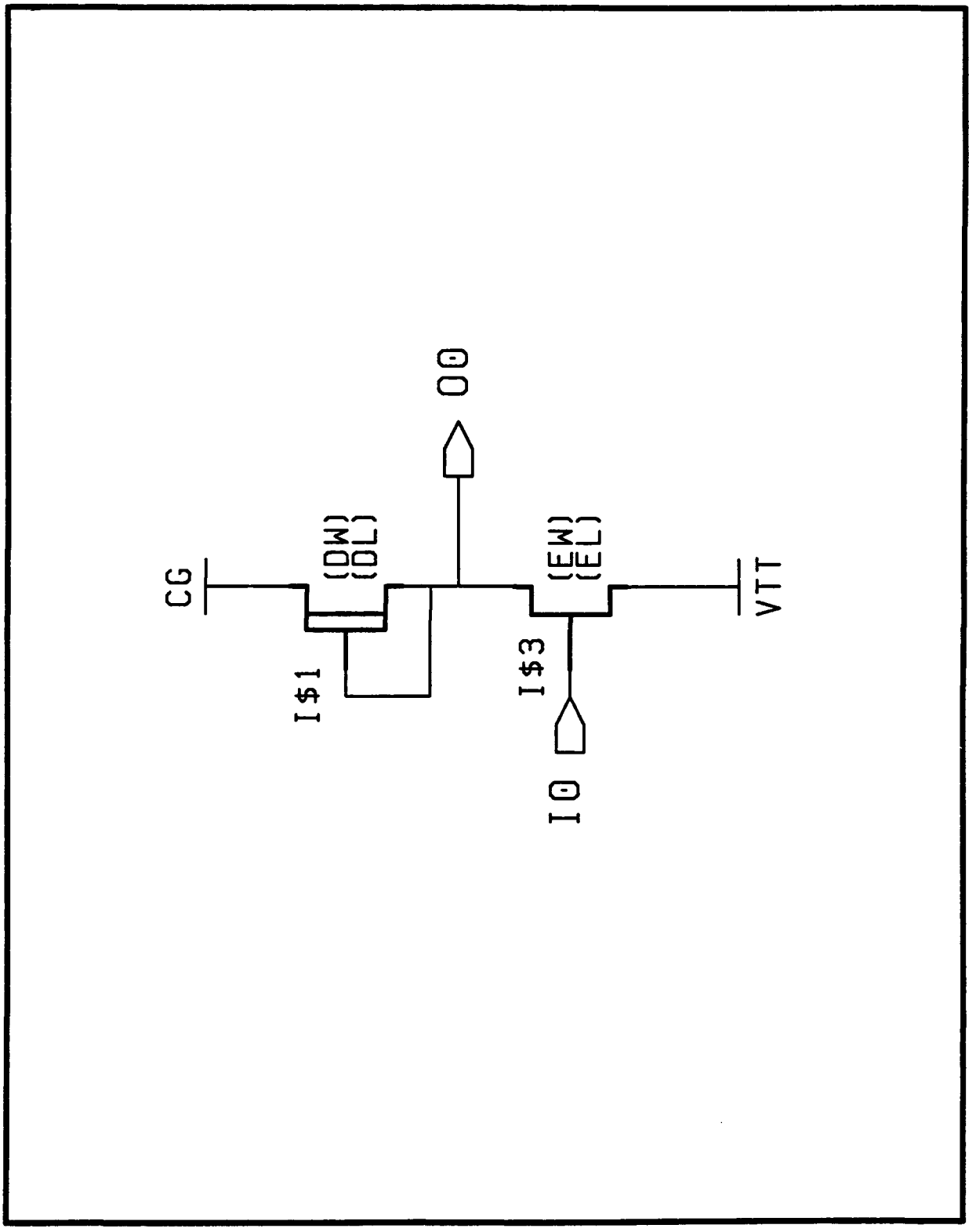

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: DRVR2
DESCRIPTION: LOW POWER 2 VOLT DRIVER WITH PAD
OUT
0.2
0.2
1
0
01
IO
O1
.6
0.9
DRVR2
I#
AND
I1
IN
2
I1

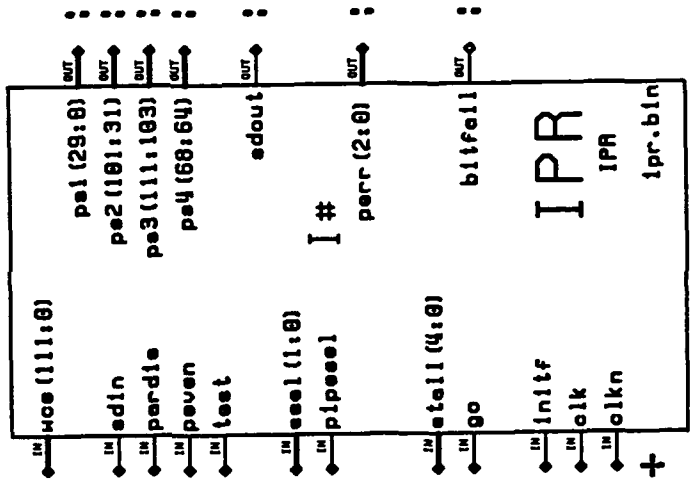

O1
B24
B21
B22
B23
58
51
3
B12
B13
B9
B11
B4
B6
B1
B3
GND
VTT
I1
DNT2
Revised 8/24/89

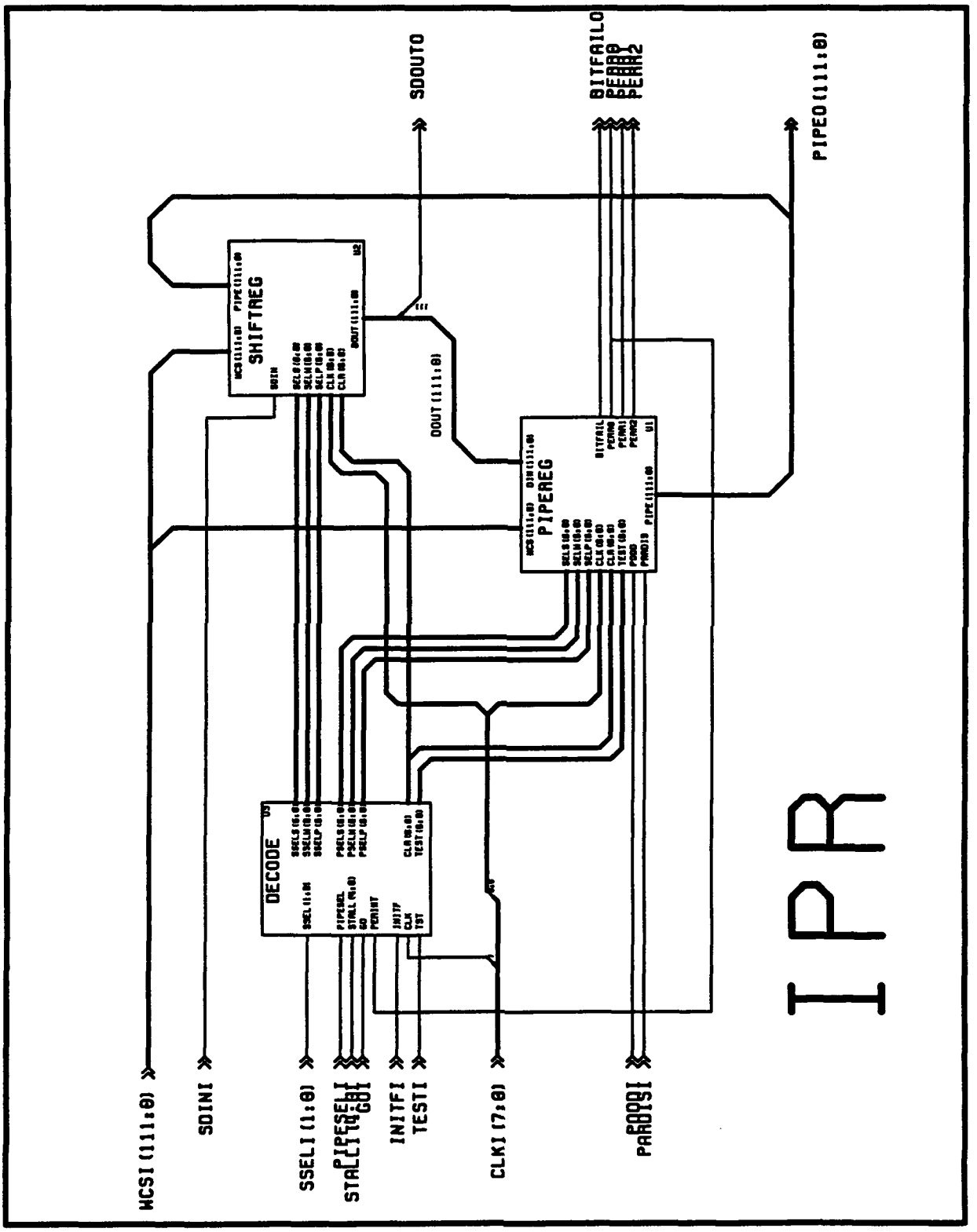

EIGHTBIT
DIN(7:0)
WCS(7:0)
SELS8L
SELW8L
SELP8L
TEST8
CLK8N
CLR8
PIPE(7:0)
PARITY8
BITFAIL8
UXX

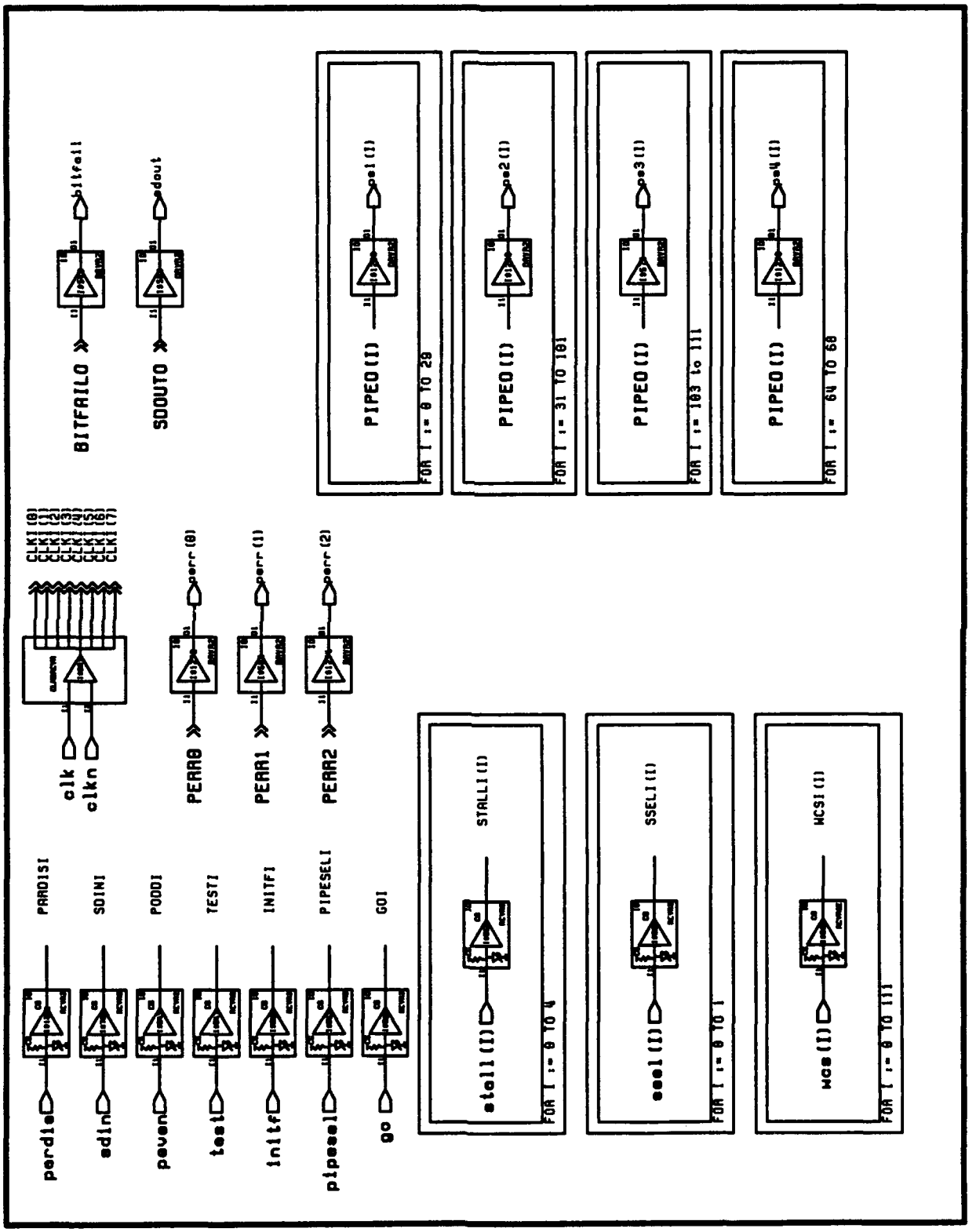

PARITY8
PIPE (0)
PIPE (1)
PIPE (2)
PIPE (3)
PIPE (4)
PIPE (5)
PIPE (6)
PIPE (7)
BITFAIL8
EIGHTBIT
PIPE (I)
VOTEBIT
CLK8N
CLR8
FOR I := 0 TO 7

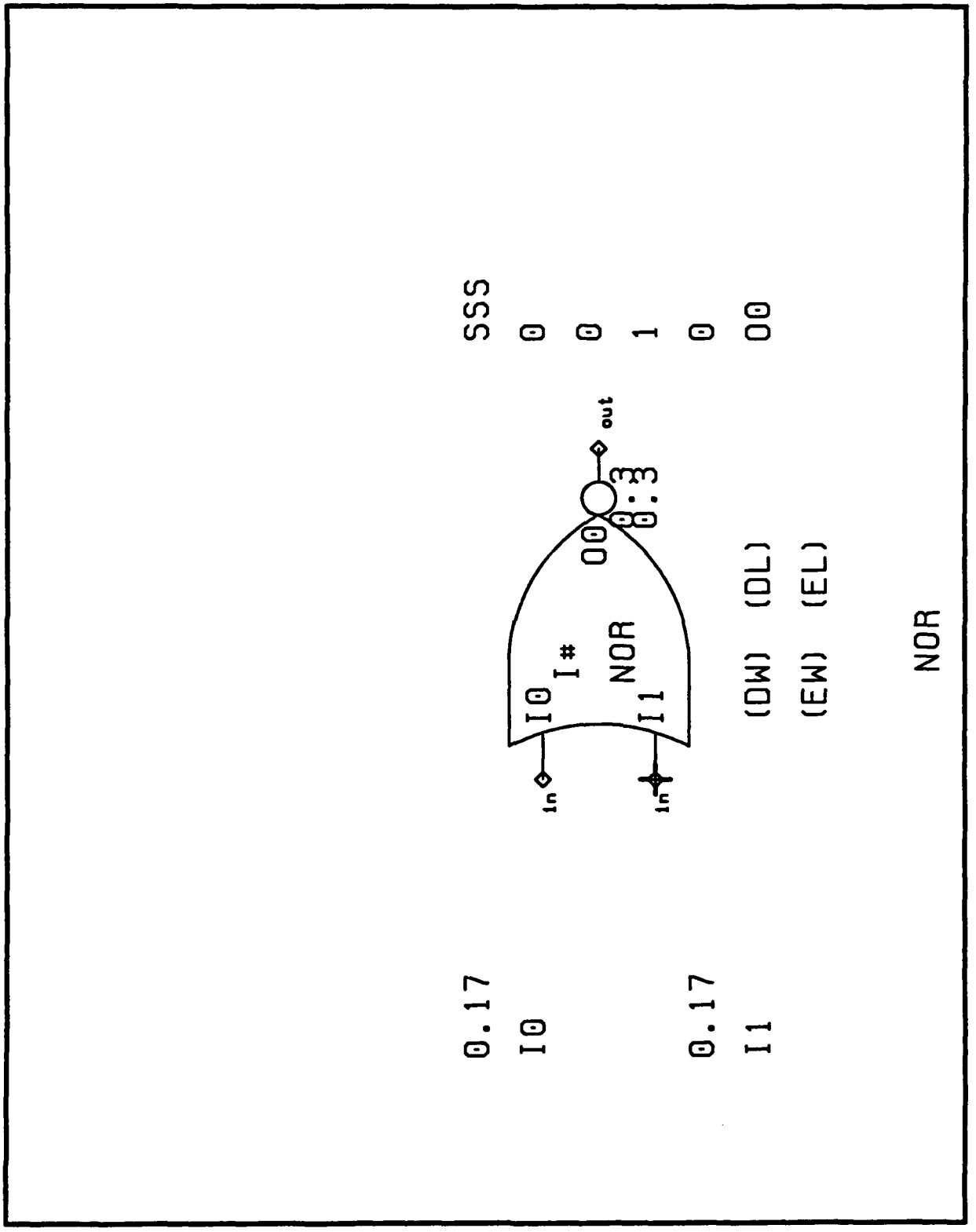

SSS
0 0 1 0 00
00
out
8.2
I#
INV
(DW) (DL)
(EW) (EL)
NAND
IO
in
0.17
IO

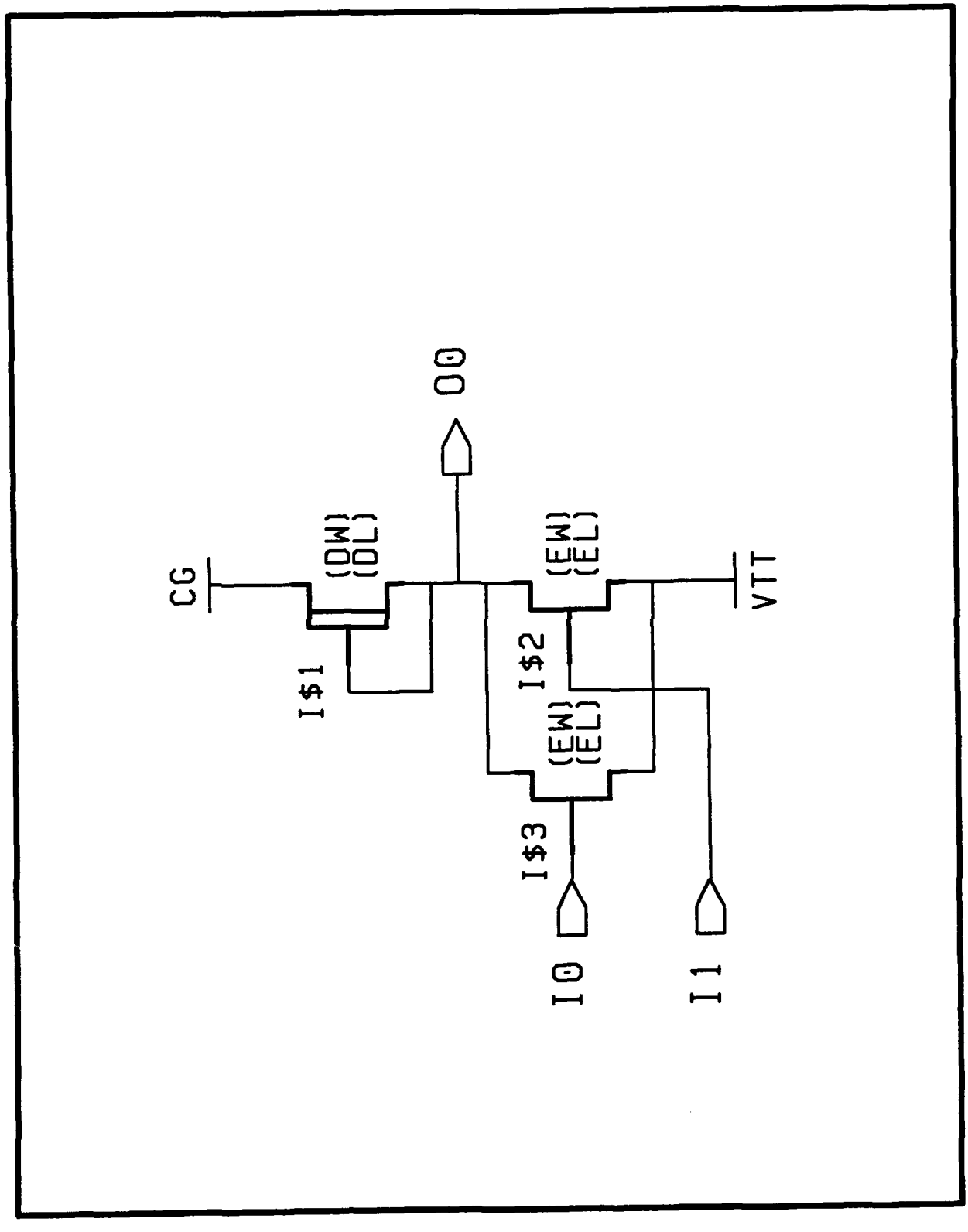

O0
(OW)
(OL)
(EW)
(EL)
CG
VTT
I$1
I$3
IO

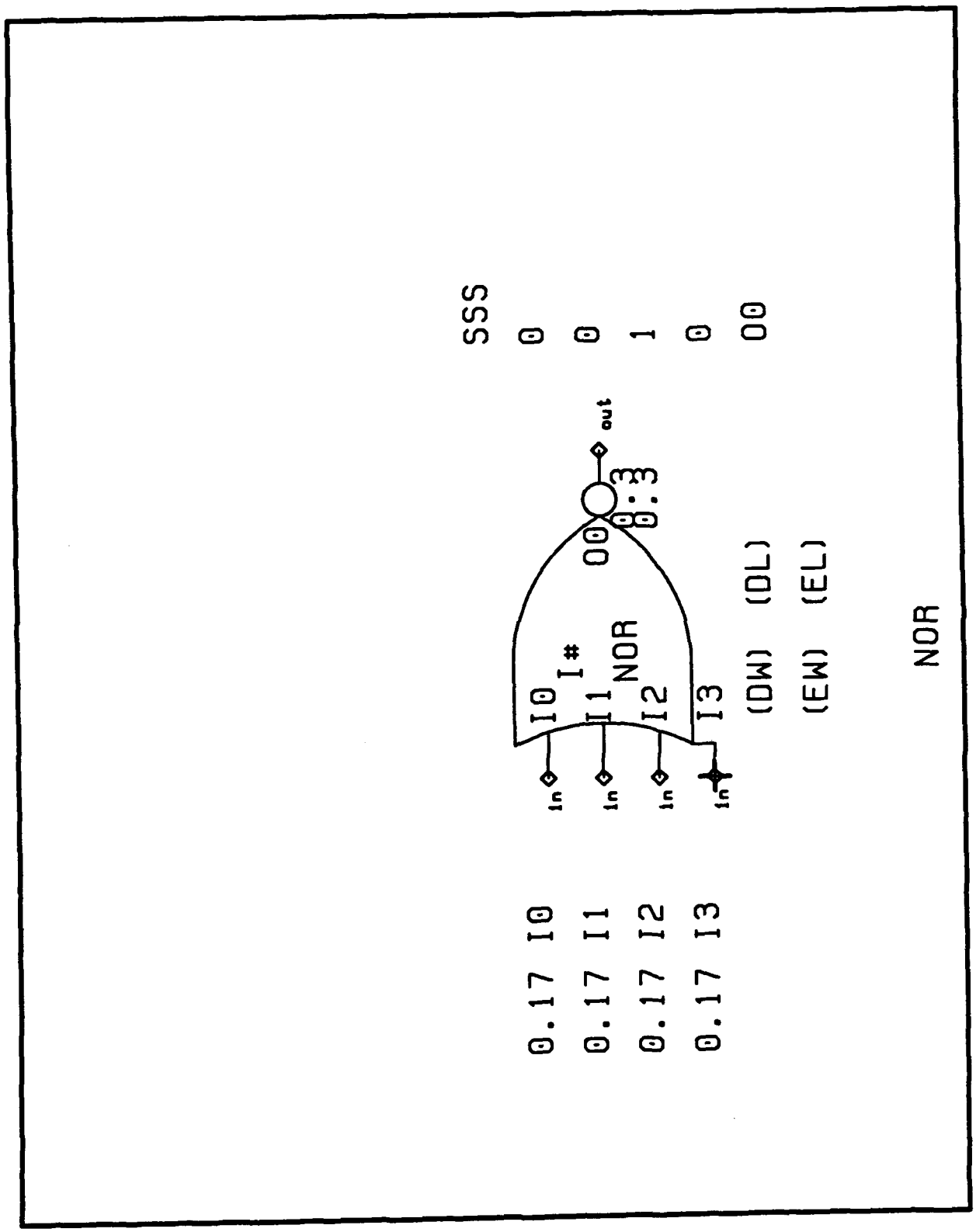

IPR
IPR
ipr.bln
wce(11:0)
sdin
pardis
paven
test
ssel(1:0)
pipssel
stall(4:0)
go
initf
clk
clkn
ps1(29:8)
ps2(181:31)
ps3(111:103)
ps4(68:64)
sdout
perr(2:0)
bitfail

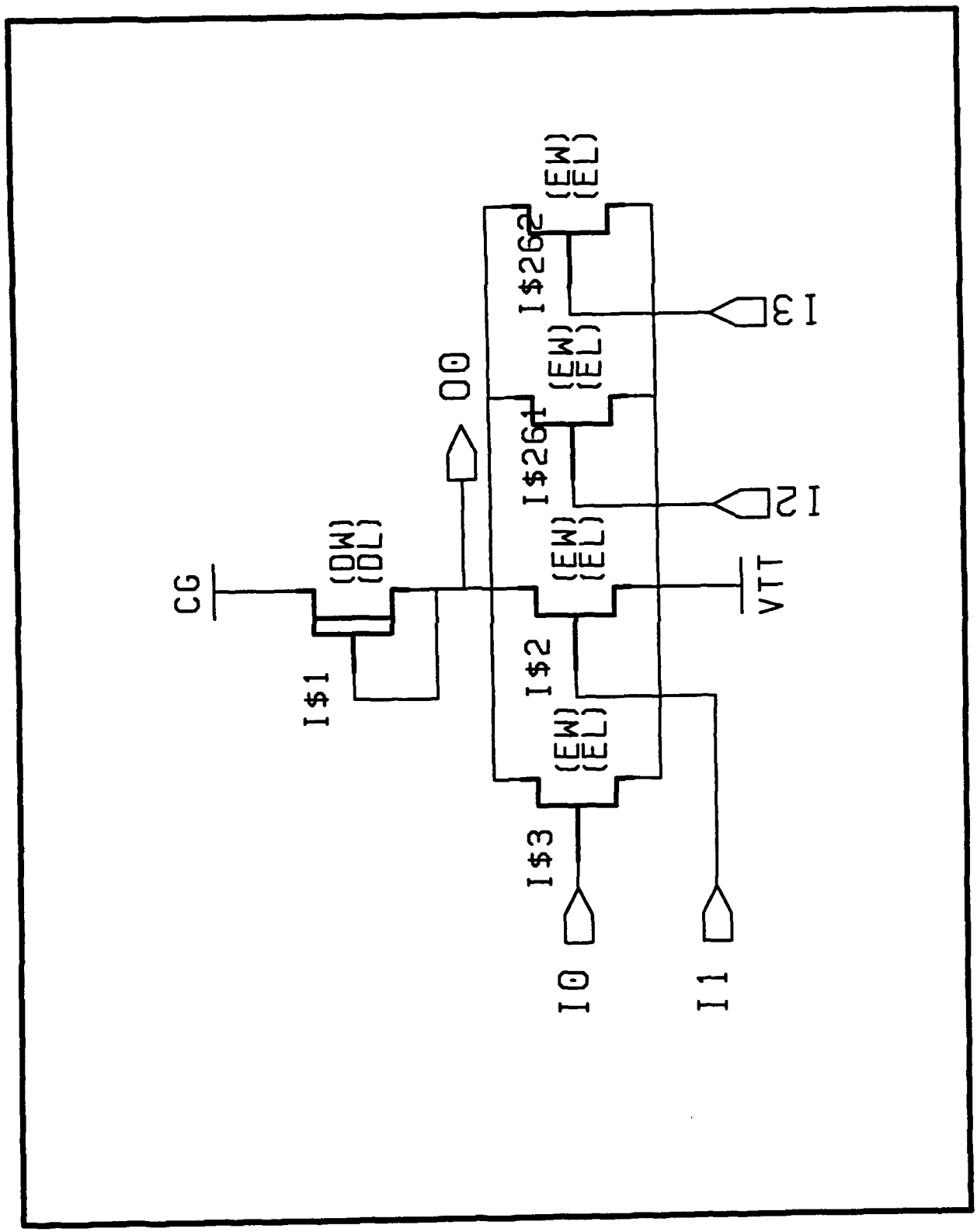

SDOUTO
BITFAILO
PERR0
PERR1
PERR2
PIPEO(111:0)
SHIFTREG
DOUT(111:0)
PIPEREG
DECODE
IPR
WCSI(111:0)
SDINI
SSELI(1:0)
PIPESELI
STALLI
GOI
INITFI
TESTI
CLKI(7:0)
PARODSI

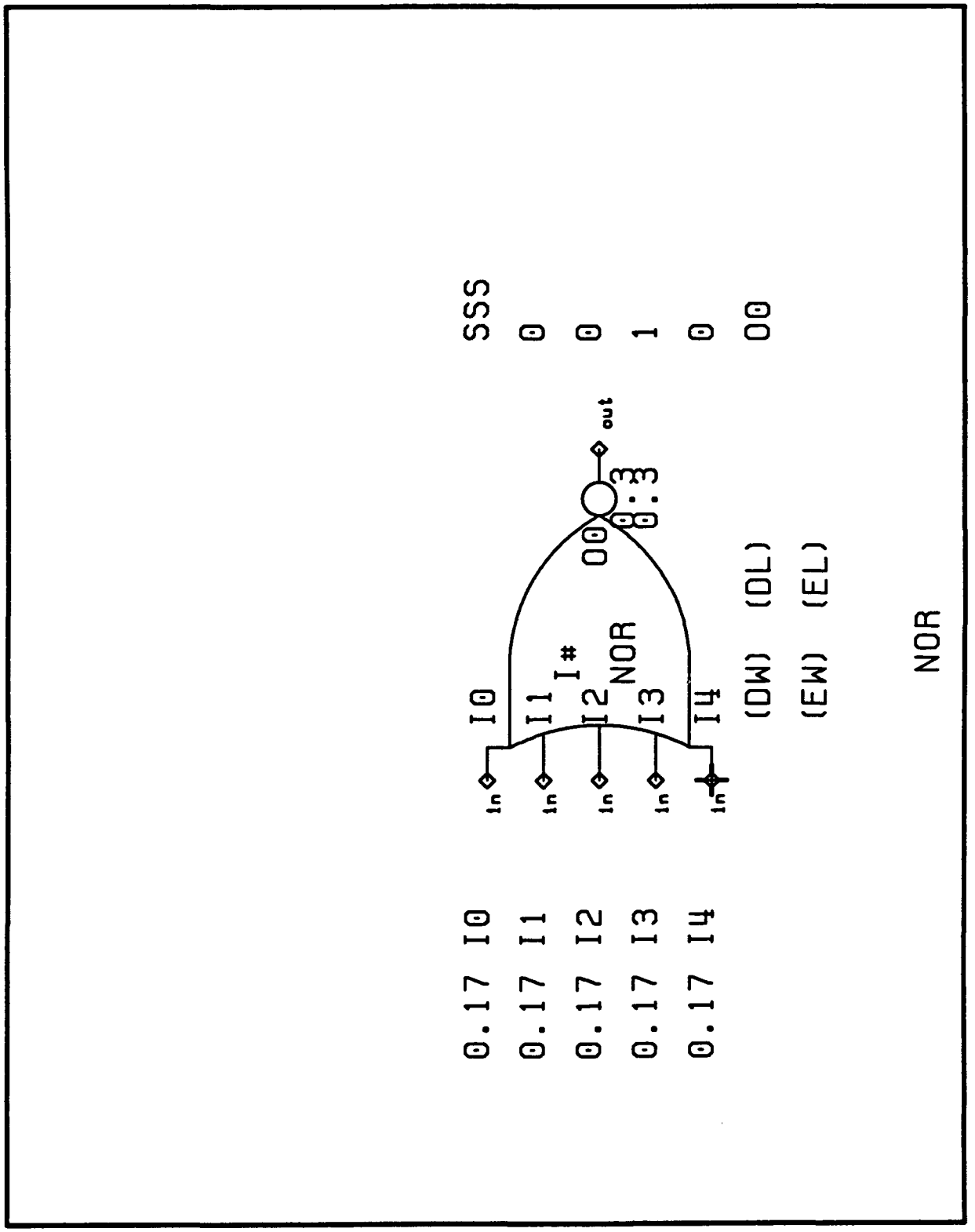

bitfail
sdout
BITFAIL0
SDOUT0
pe1(I)
pe2(I)
pe3(I)
pe4(I)
PIPEO(I)
FOR I := 0 TO 28
FOR I := 31 TO 101
FOR I := 103 to 111
FOR I := 64 TO 68
CLKI(0)
CLKI(1)
CLKI(2)
CLKI(3)
CLKI(4)
CLKI(5)
CLKI(6)
CLKI(7)
perr(0)
perr(1)
perr(2)
clk
clkn
PERR0
PERR1
PERR2
PARDISI
SDINI
PODDI
TESTI
INITFI
PIPESELI
GOI
STALLI(I)
SSELI(I)
WCSI(I)
stall(I)
ssel(I)
wcs(I)
FOR I := 0 TO 4
FOR I := 0 TO 1
FOR I := 0 TO 111
pardis
sdin
podd
test
initf
pipesel
go

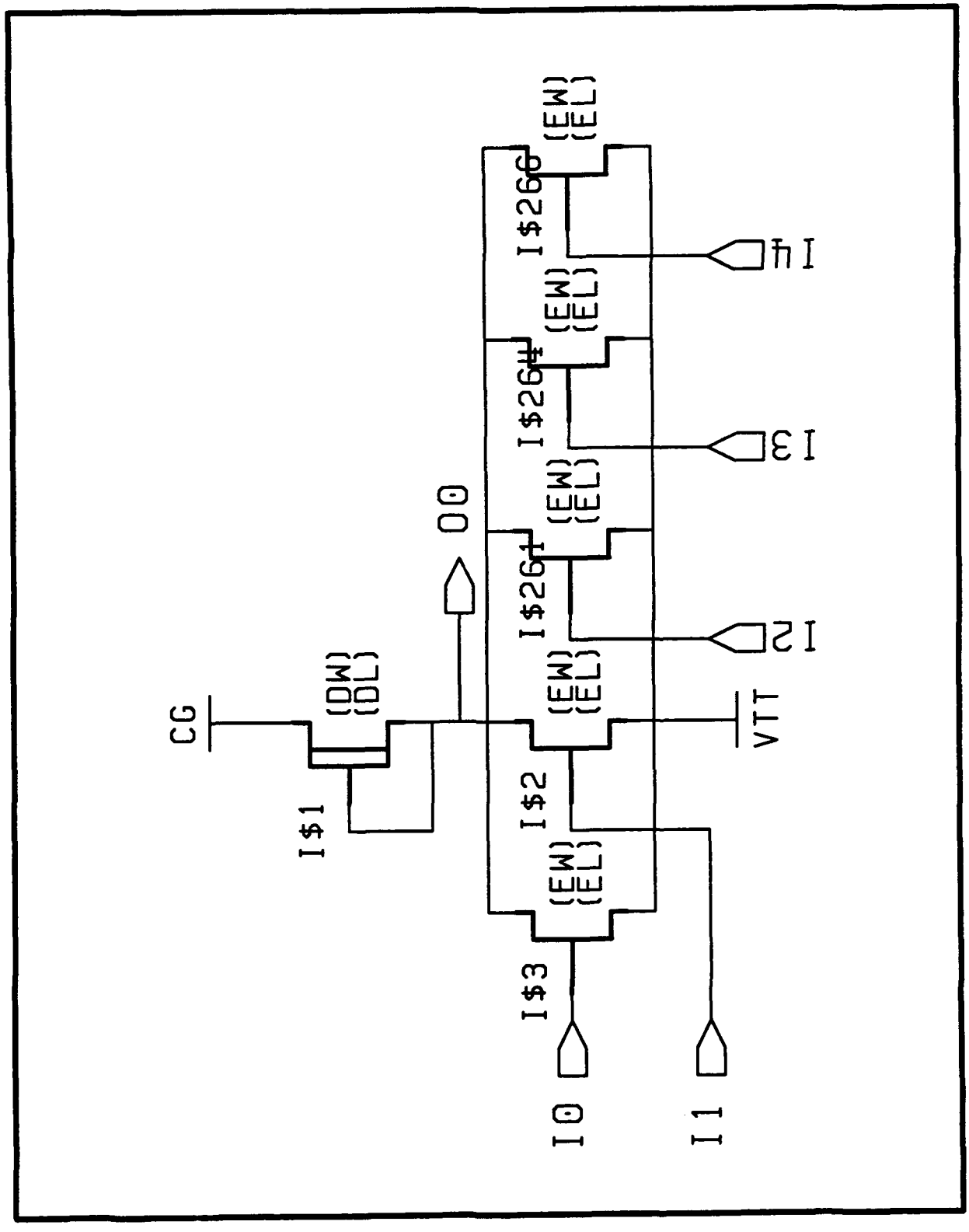

SSS
0
0
1
0
00
out
0.3
00
I0
I#
NOR
I1
in
in
(OW) (OL)
(EW) (EL)
NOR
0.17
I0
0.17
I1

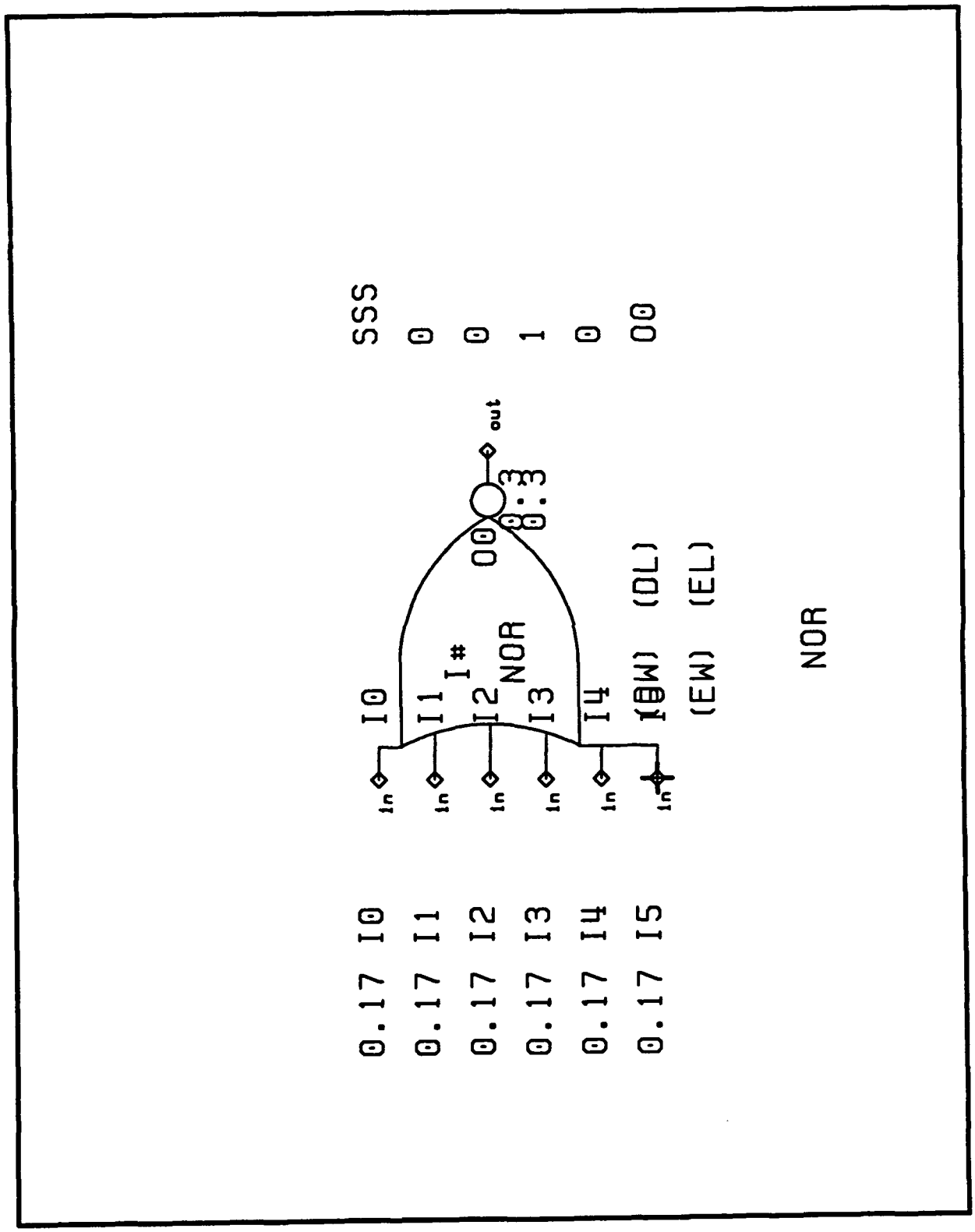

O0
CG
(DW)
(DL)
(EW)
(EL)
VTT
I$1
I$2
(EW)
(EL)
I$3
I0
I1

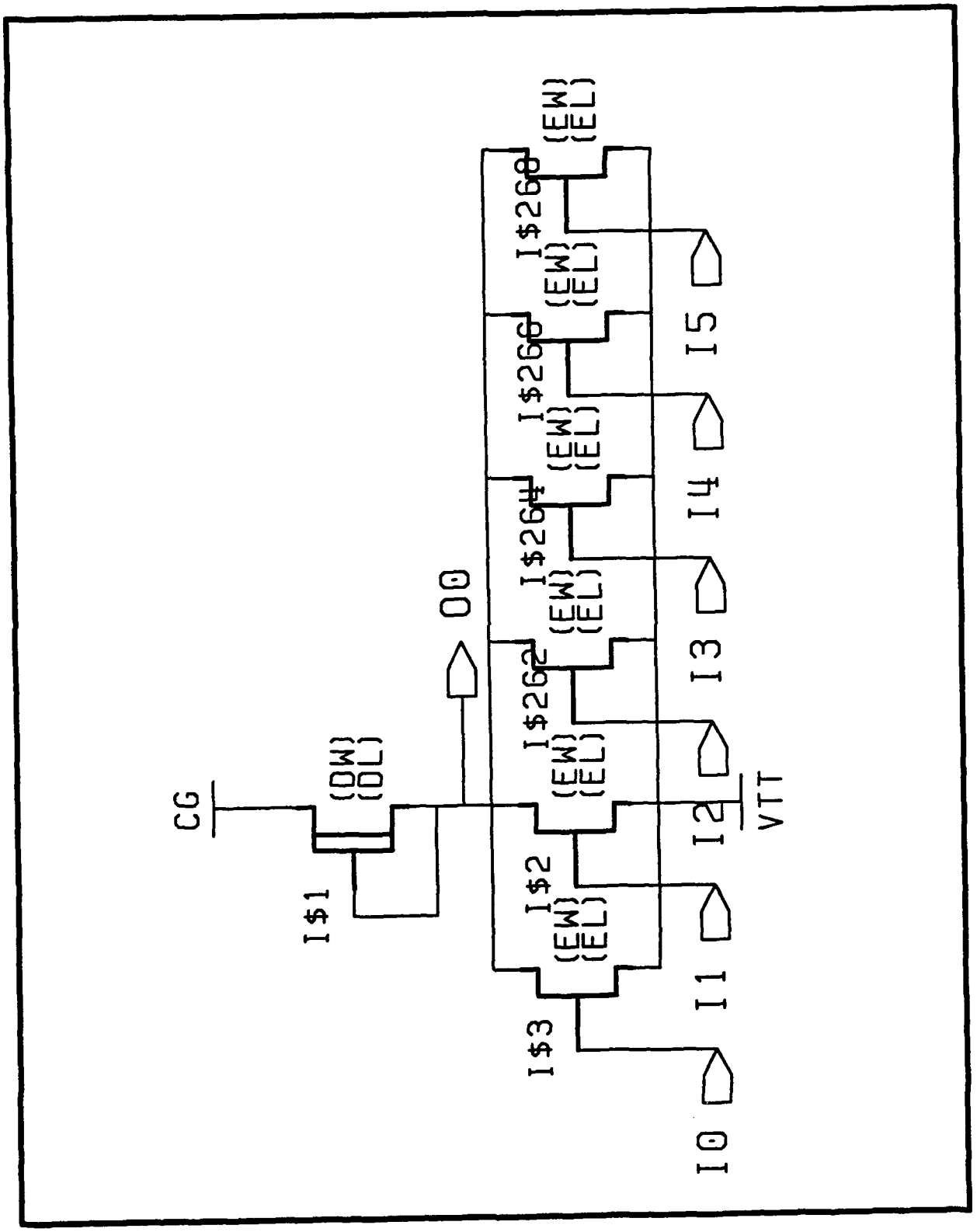

SSS
0 0 1 0 00
out
8:3
00
I0 I# I1 NOR I2 I3
(DW) (DL)
(EW) (EL)
NOR
In In In In
0.17 I0
0.17 I1
0.17 I2
0.17 I3

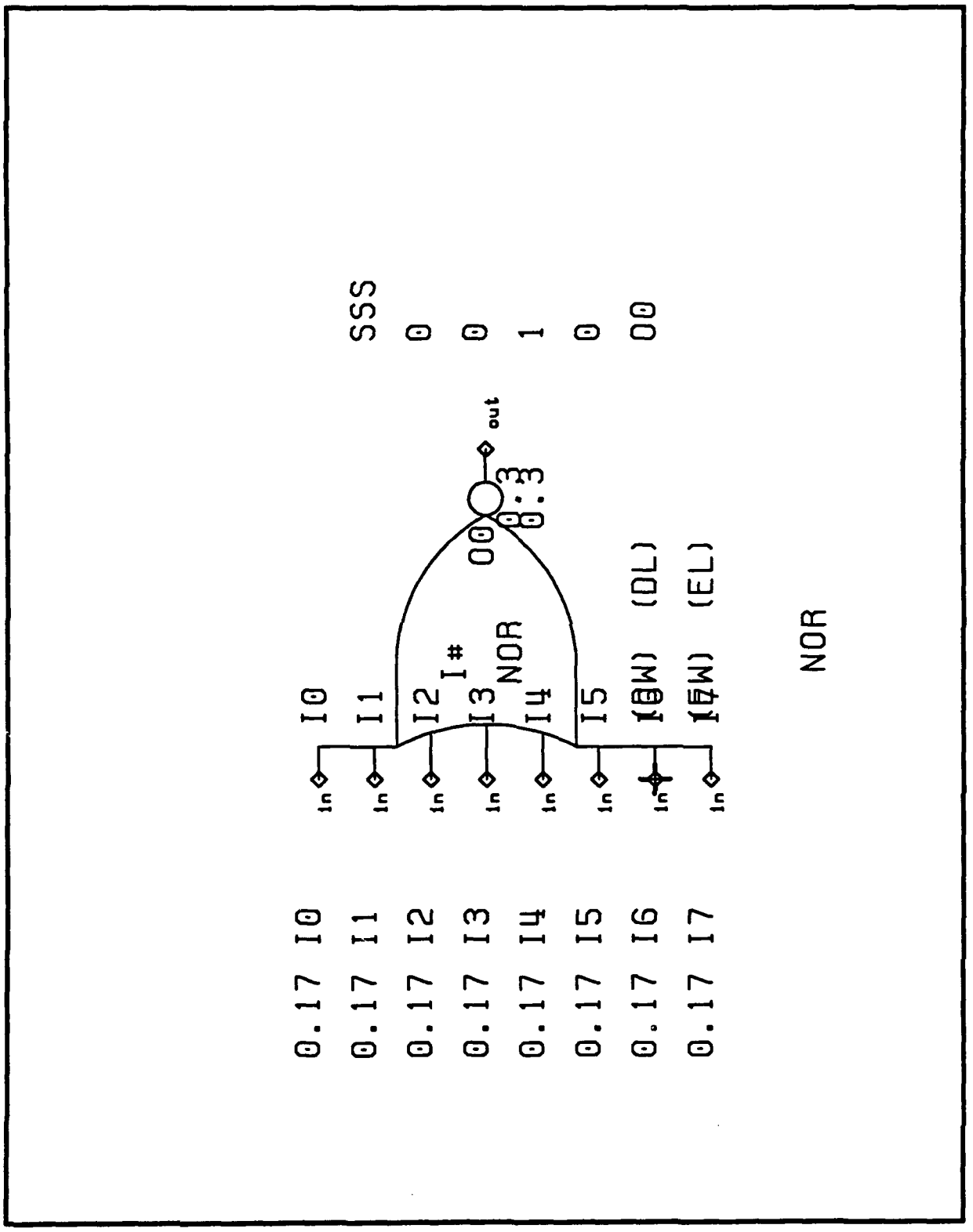

I$262
(EW)
(EL)
I3
O0
I$264
(EW)
(EL)
I2
CG
(DW)
(DL)
(EW)
(EL)
VTT
I$1
I$2
(EW)
(EL)
I$3
I0
I1

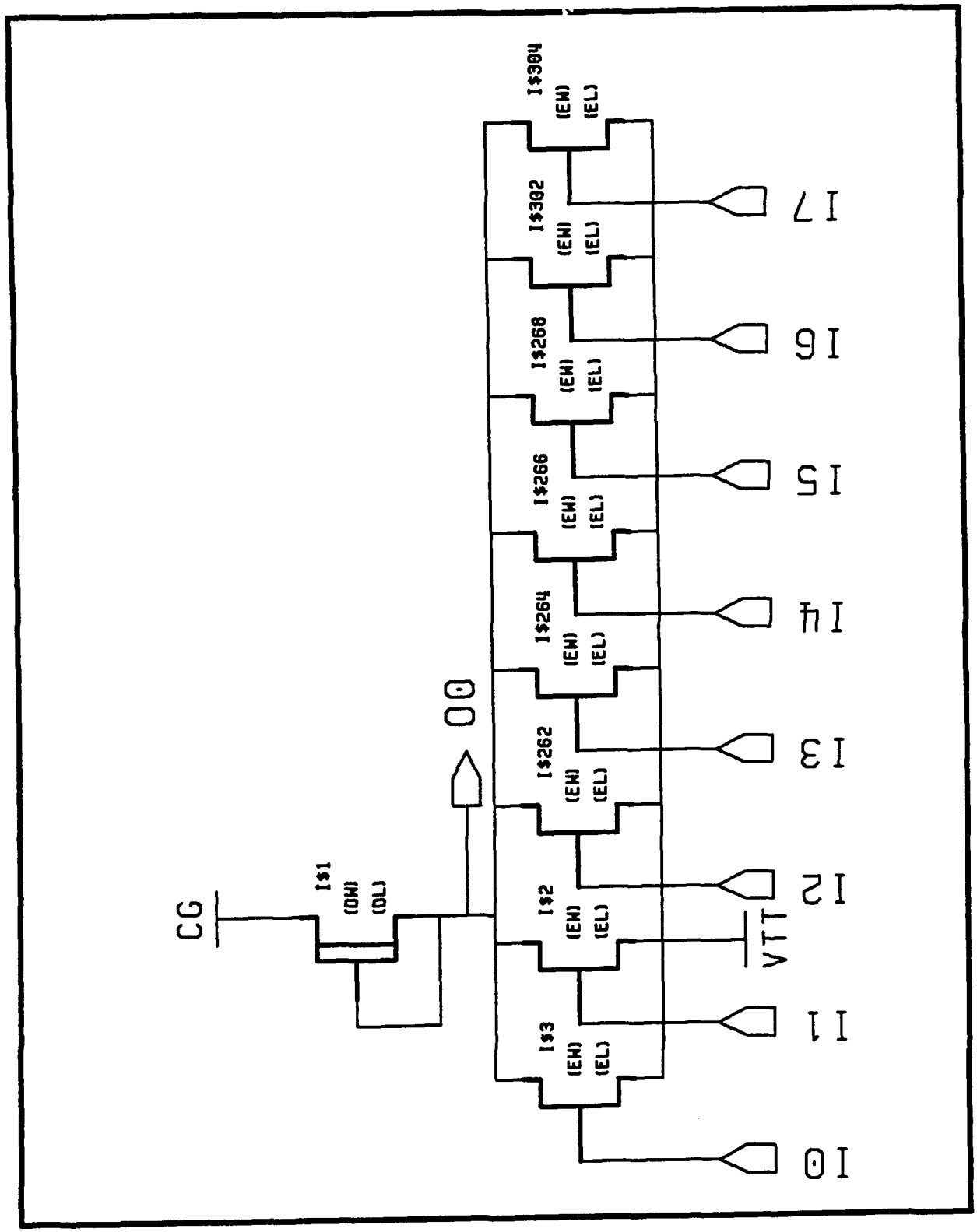

SSS
0
0
1
0
00
(DW) (DL)
(EW) (EL)
NOR
out
00
8:3
I0
I1
I#
I2
NOR
I3
I4
in
in
in
in
in
0.17 I0
0.17 I1
0.17 I2
0.17 I3
0.17 I4

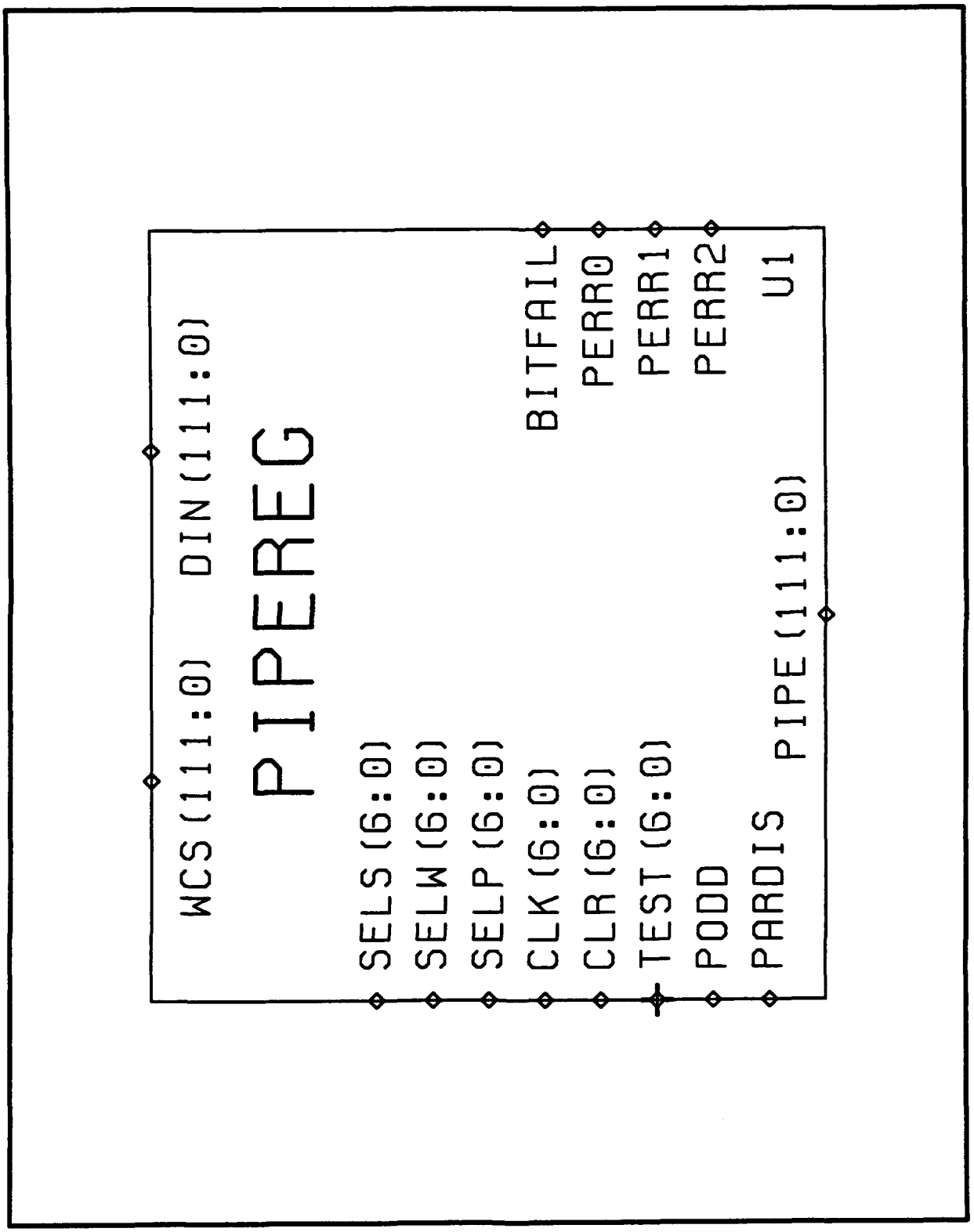

I$266
(EW)
(EL)
I4
I$264
(EW)
(EL)
I3
O0
I$261
(EW)
(EL)
I2
CG
(DW)
(DL)
I$1
I$2
(EW)
(EL)
VTT
I$3
(EW)
(EL)
I0
I1

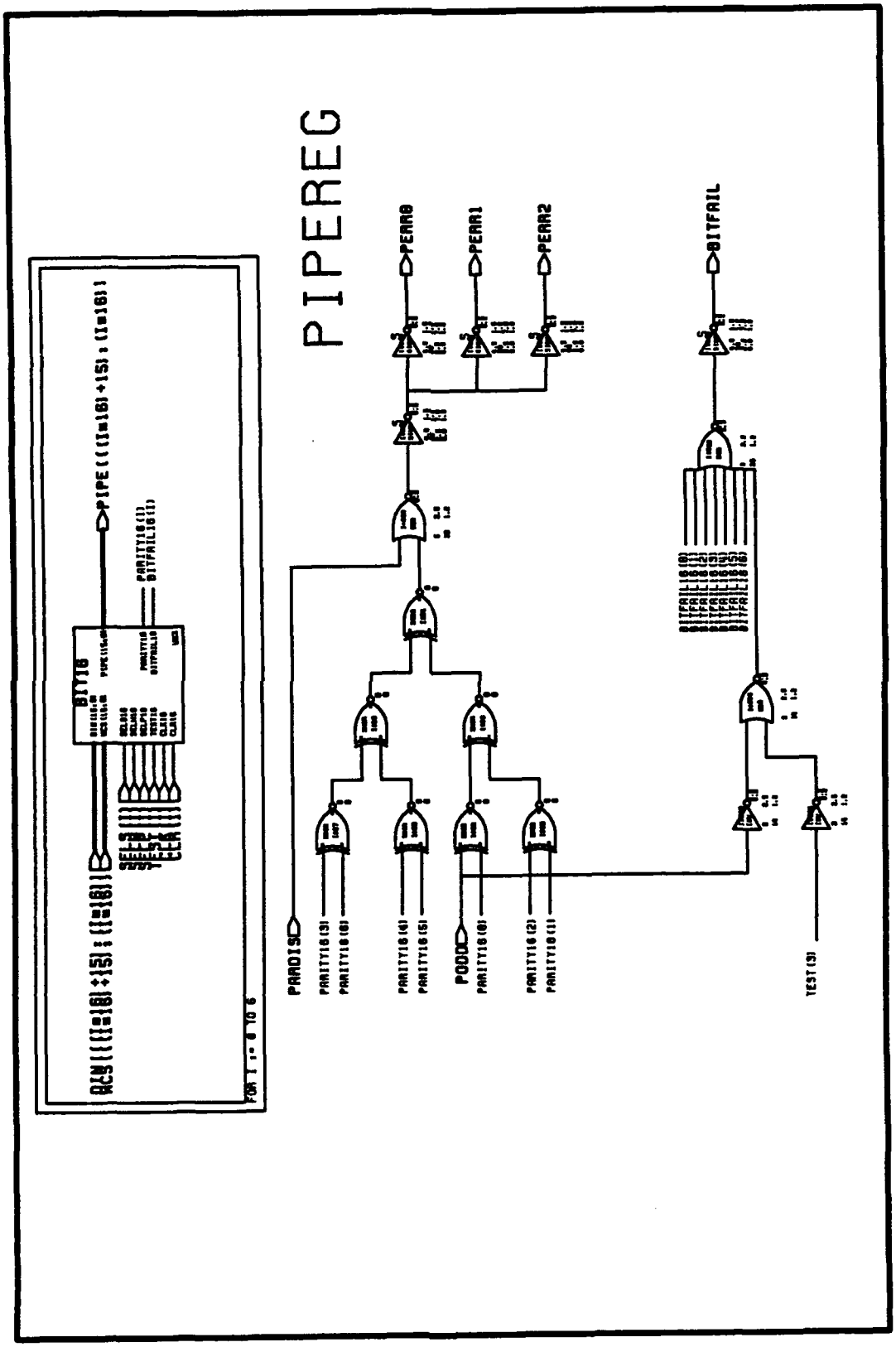

SSS
0
0
1
0
00
out
8.3
00
I#
NOR
I0
I1
I2
I3
I4
(BW)
(DL)
(EW)
(EL)
NOR
0.17 I0
0.17 I1
0.17 I2
0.17 I3
0.17 I4
0.17 I5

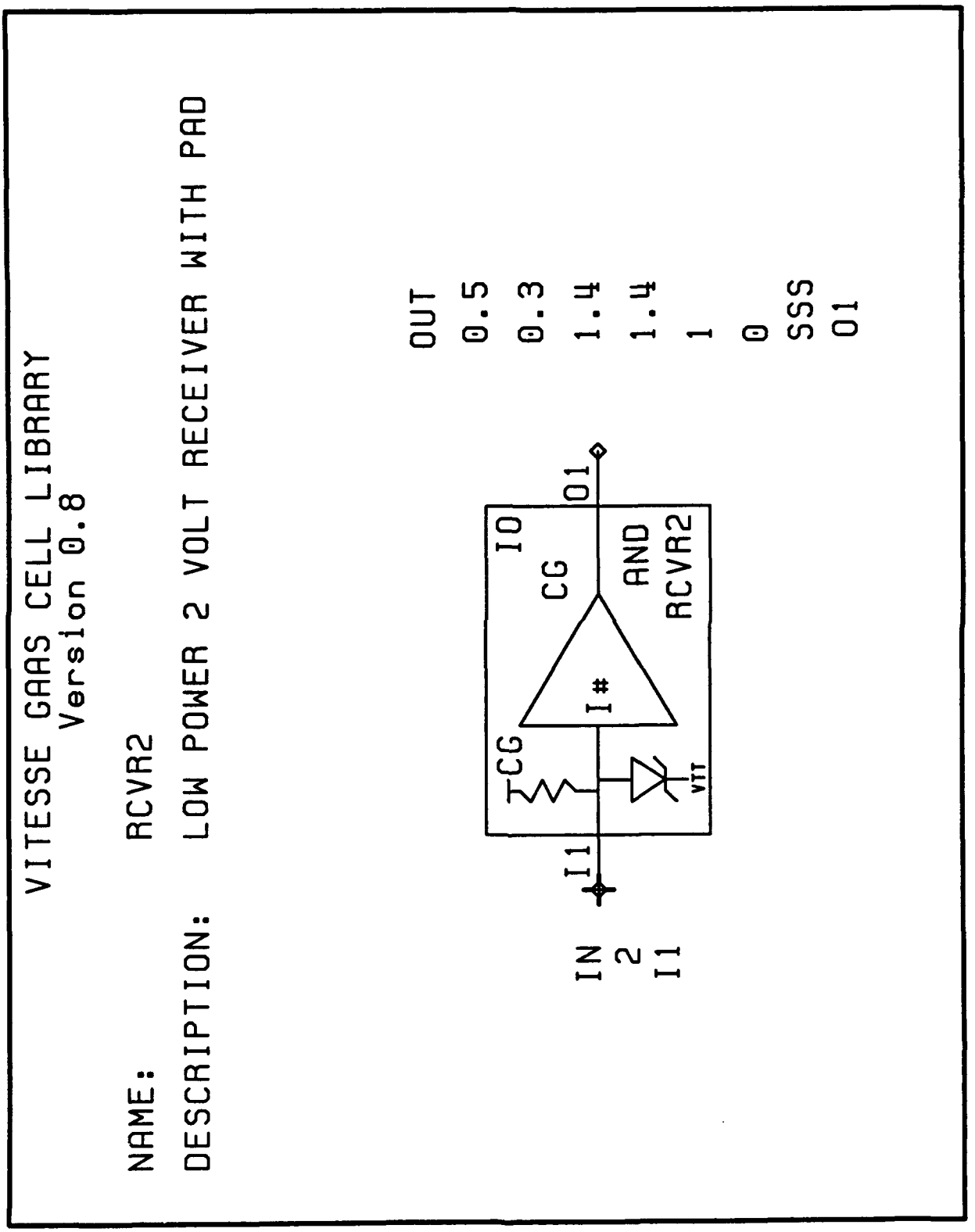

I$268
(EW)
(EL)
I$266
(EW)
(EL)
I$264
(EW)
(EL)
I$262
(EW)
(EL)
I$2
(EW)
(EL)
I$3
I$1
(OW)
(OL)
CG
OO
I5
I4
I3
I2
I1
I0
VTT

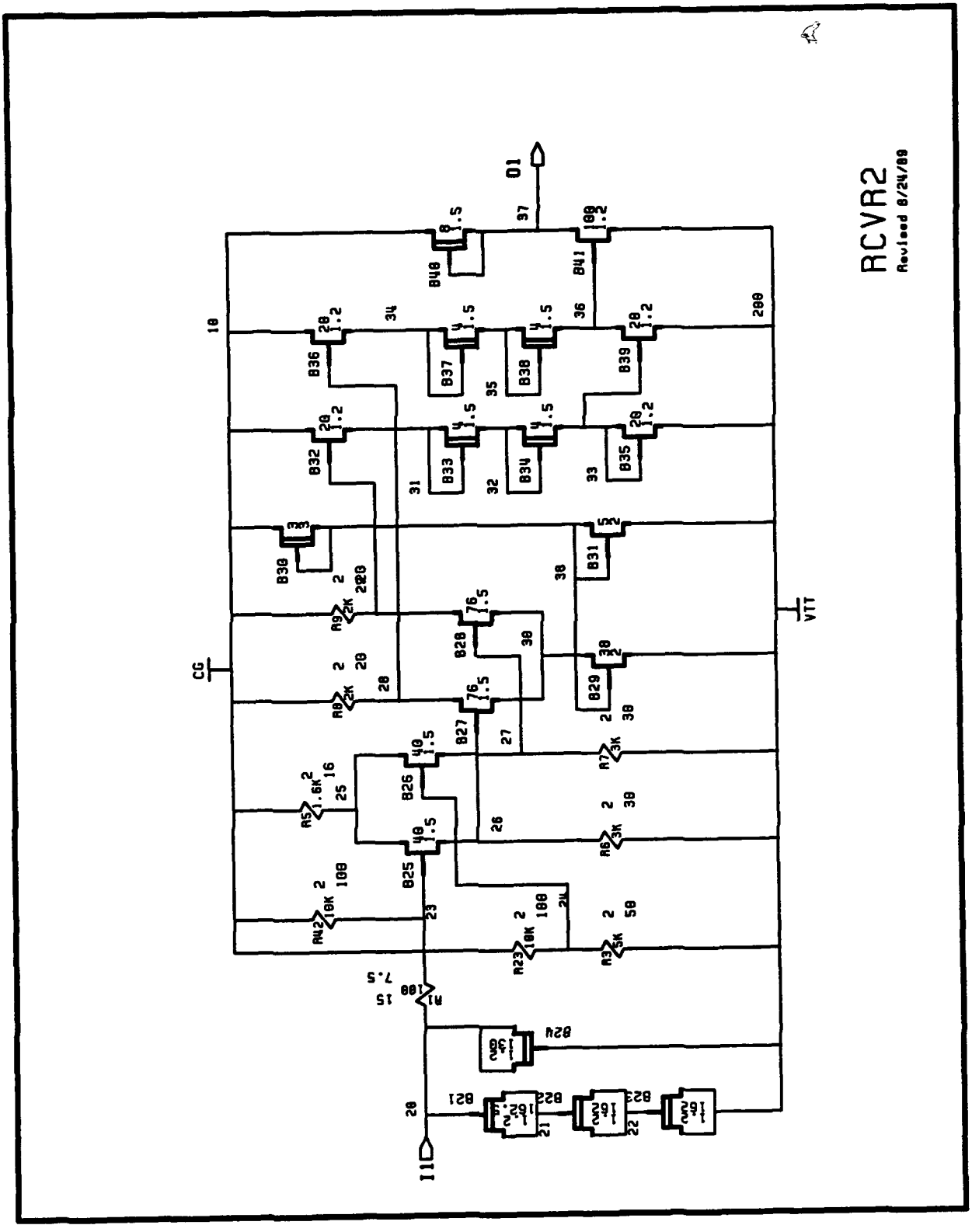

SSS
0 0 1 0 00
out
8:3
00
I#
NOR
I0
I1
I2
I3
I4
I5
(DL)
(EL)
NOR
0.17 I0
0.17 I1
0.17 I2
0.17 I3
0.17 I4
0.17 I5
0.17 I6
0.17 I7

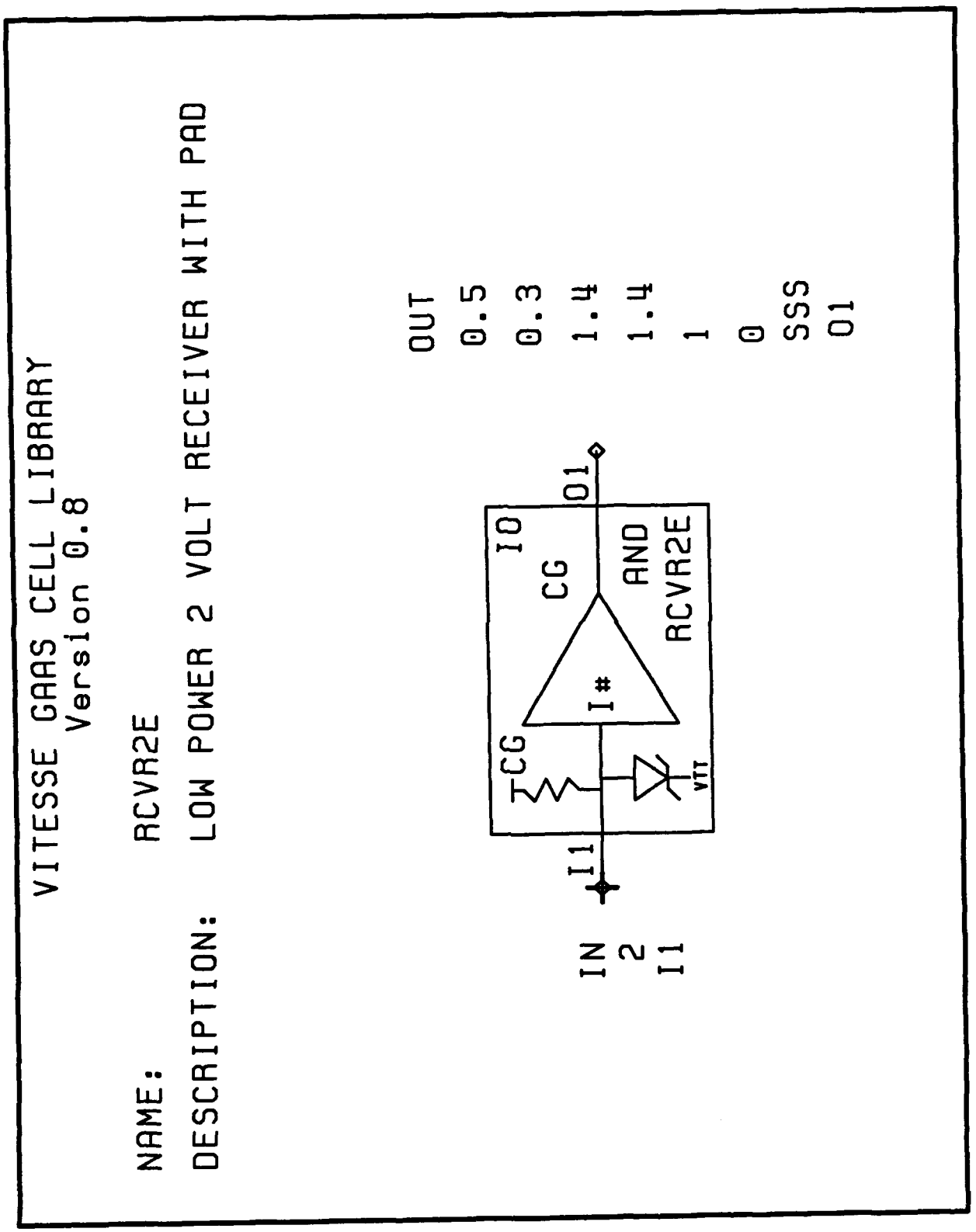

I$304
(EW)
(EL)
I$302
(EW)
(EL)
I$268
(EW)
(EL)
I$266
(EW)
(EL)
I$264
(EW)
(EL)
I$262
(EW)
(EL)
I$2
(EW)
(EL)
I$3
(EW)
(EL)
I$1
(OW)
(OL)
I7
I6
I5
I4
I3
I2
I1
I0
O0
CG
VTT

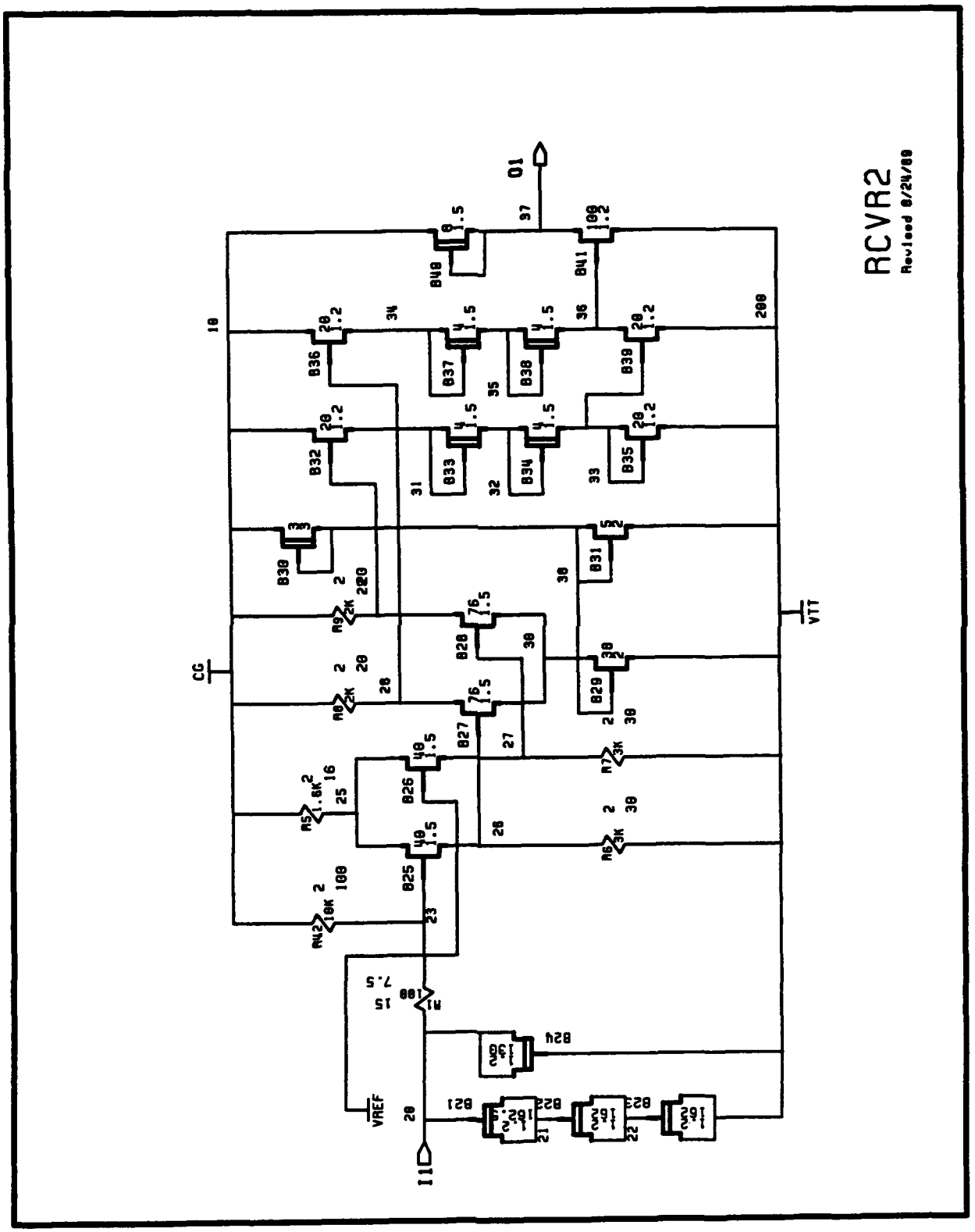

PIPEREG
WCS(111:0)
DIN(111:0)
SELS(6:0)
SELW(6:0)
SELP(6:0)
CLK(6:0)
CLR(6:0)
TEST(6:0)
PODD
PARDIS
PIPE(111:0)
BITFAIL
PERR0
PERR1
PERR2
U1

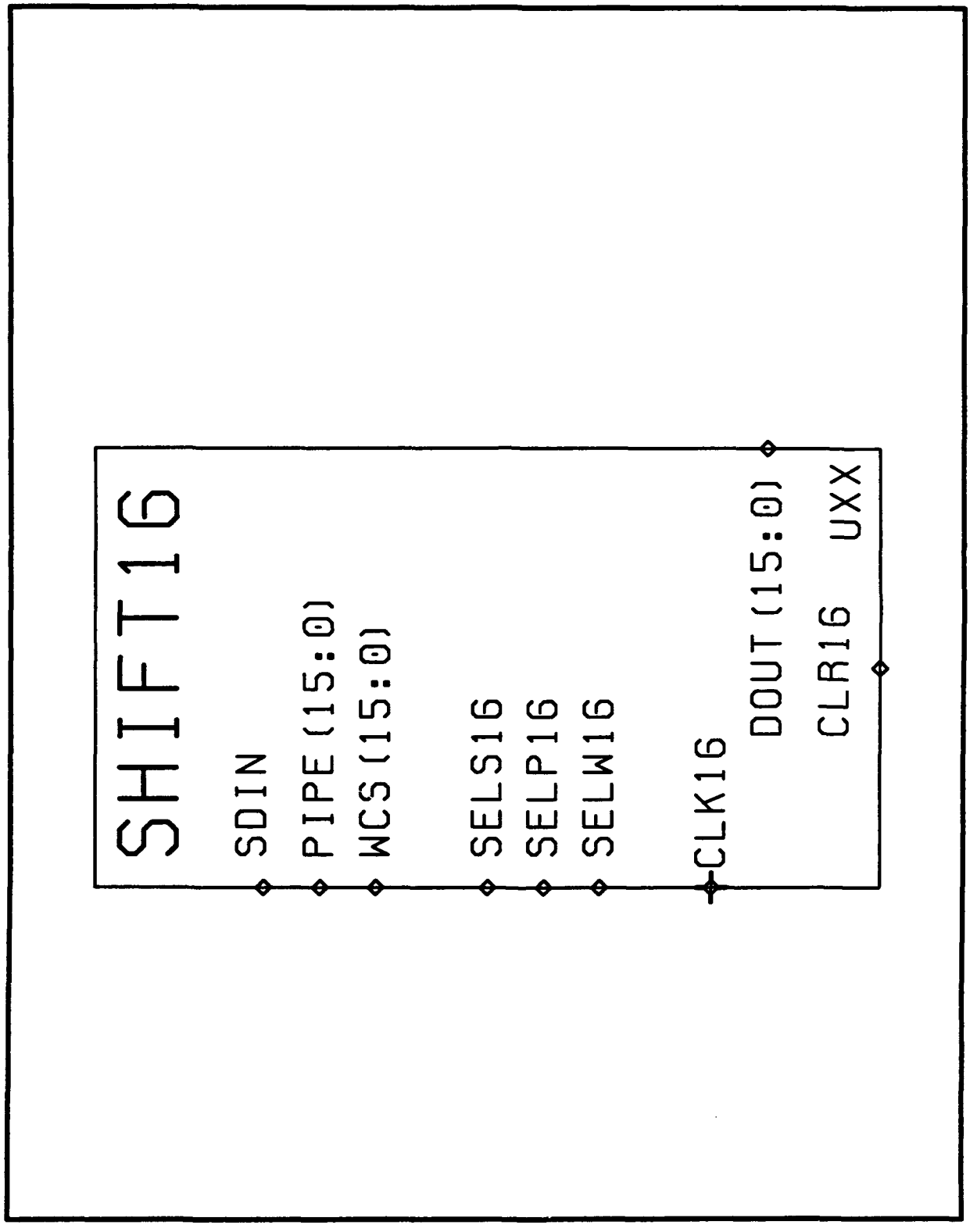

PIPEREG
PERR0
PERR1
PERR2
BITFAIL
PARDIS
POOD
TEST(3)

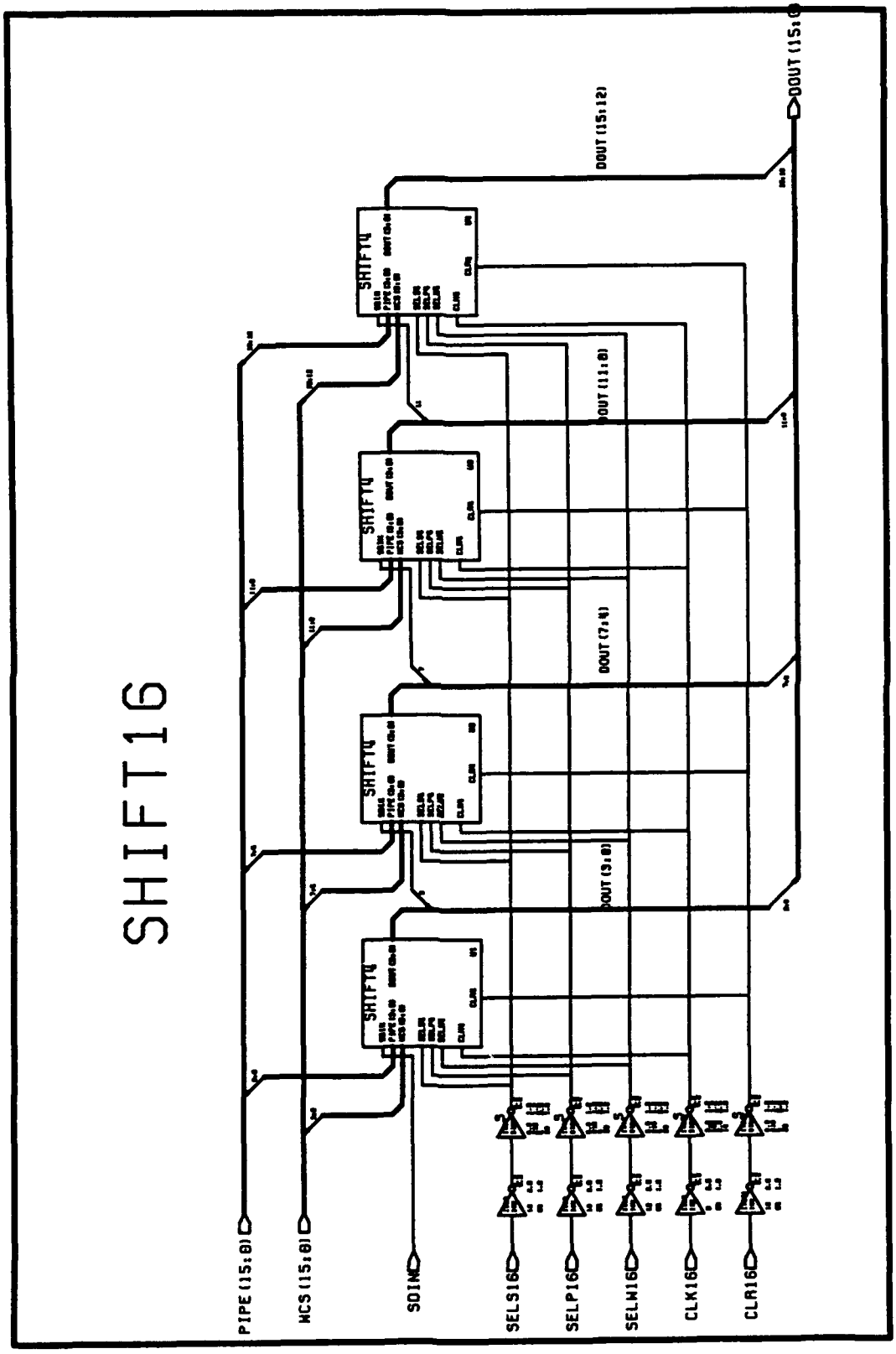

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: RCVR2
DESCRIPTION: LOW POWER 2 VOLT RECEIVER WITH PAD
OUT
0.5
0.3
1.4
1.4
1
0
SSS
01
IO
O1
CG
AND
RCVR2
I#
CG
VTT
I1
IN
2
I1

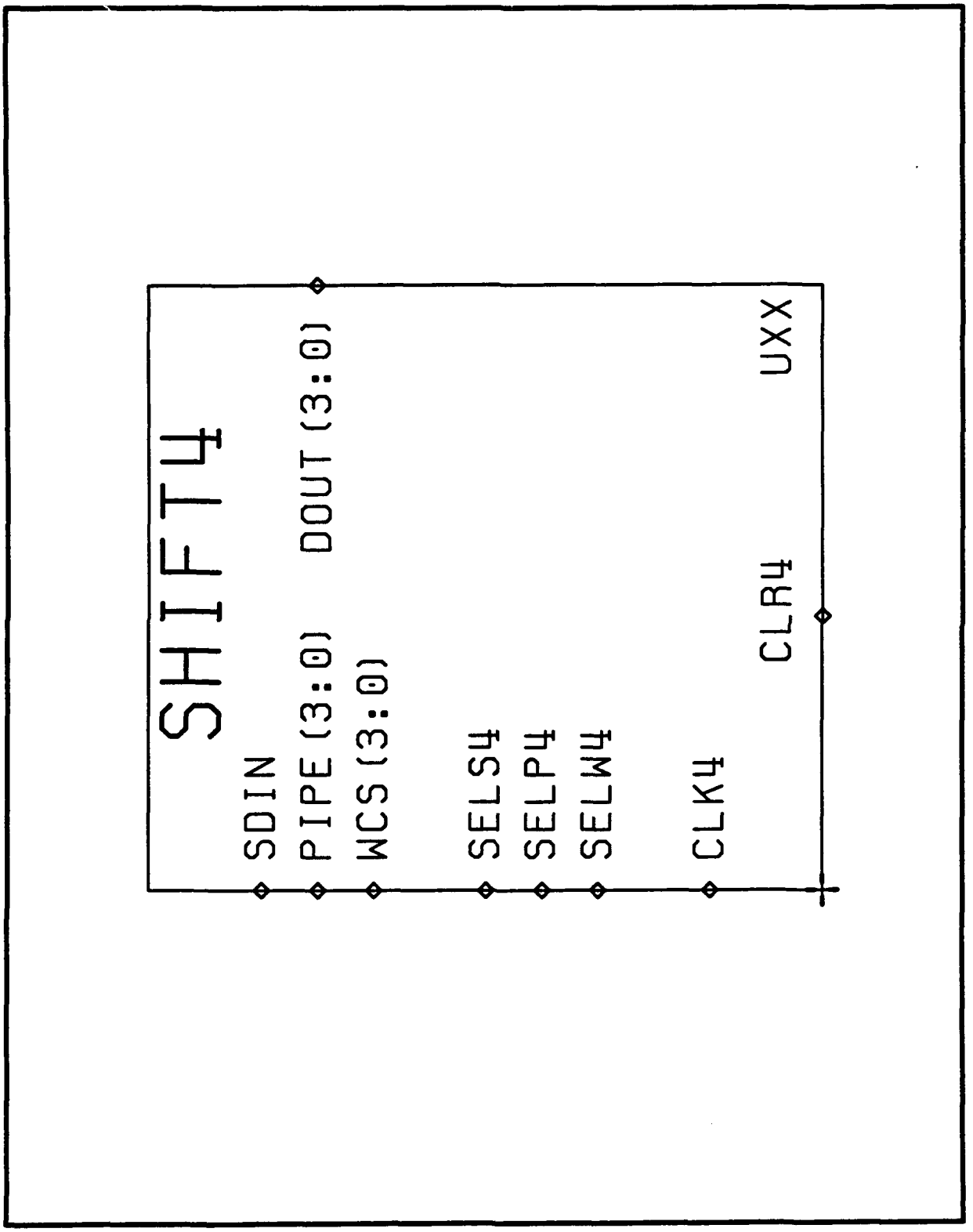

RCVR2
Revised 8/24/89
O1
I1
CG
VTT

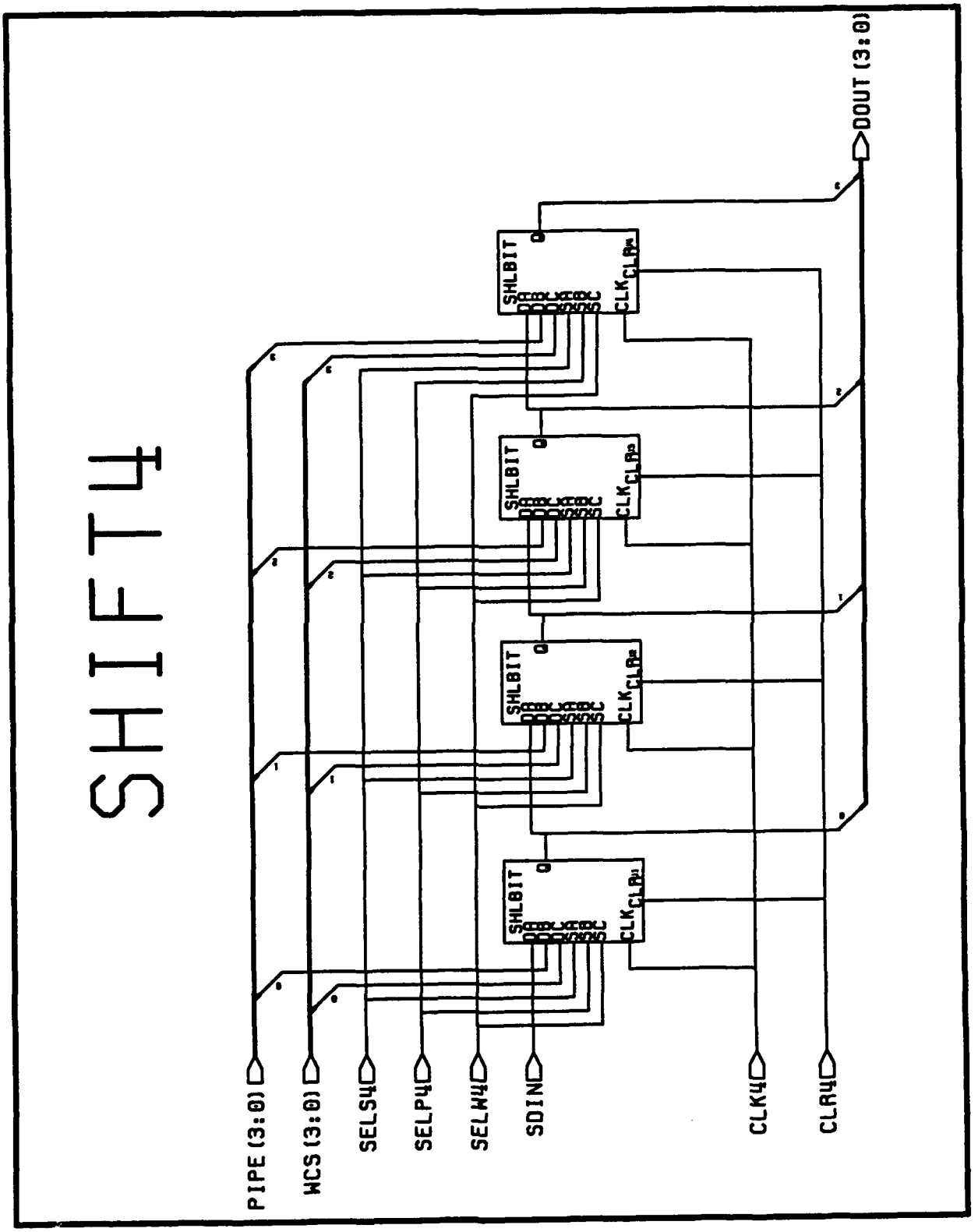

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: RCVR2E
DESCRIPTION: LOW POWER 2 VOLT RECEIVER WITH PAD
OUT
0.5
0.3
1.4
1.4
1
0
SSS
01
IO
CG
AND
RCVR2E
I#
O1
I1
CG
VTT
IN
2
I1

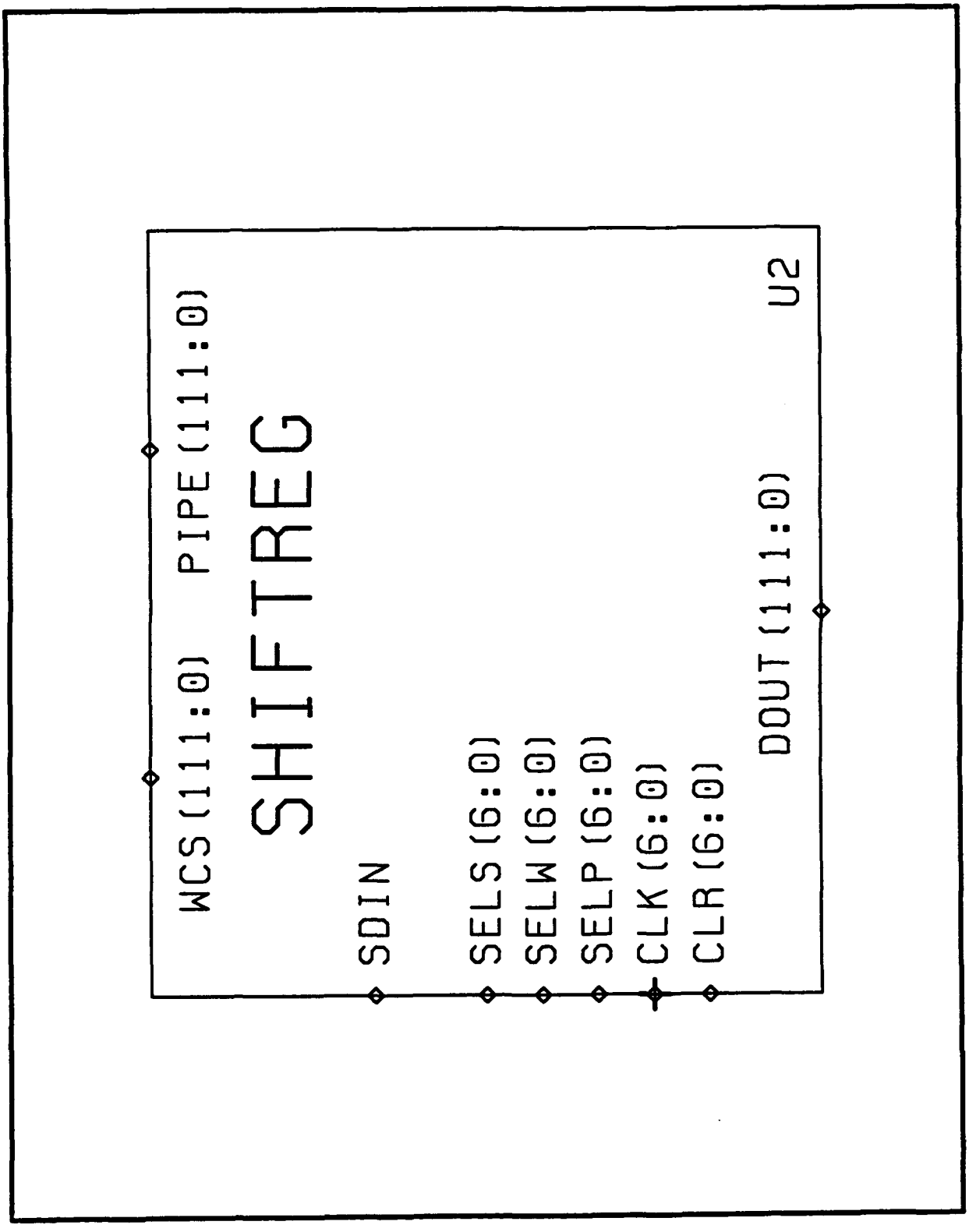

RCVR2
Revised 6/24/88
O1
I1
CG
VTT
VREF

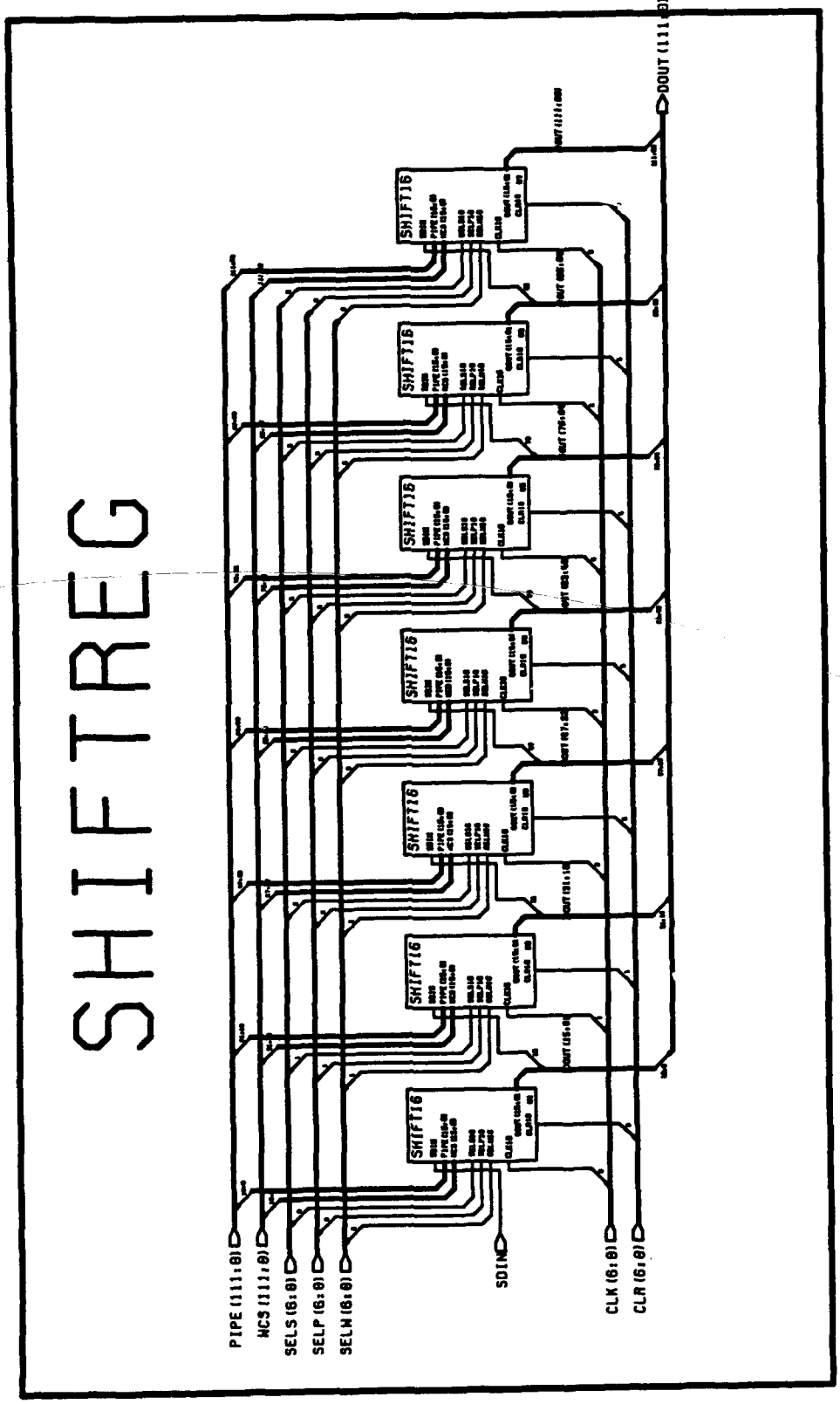

SHIFT16
SDIN
PIPE(15:0)
WCS(15:0)
SELS16
SELP16
SELW16
CLK16
DOUT(15:0)
CLR16
UXX

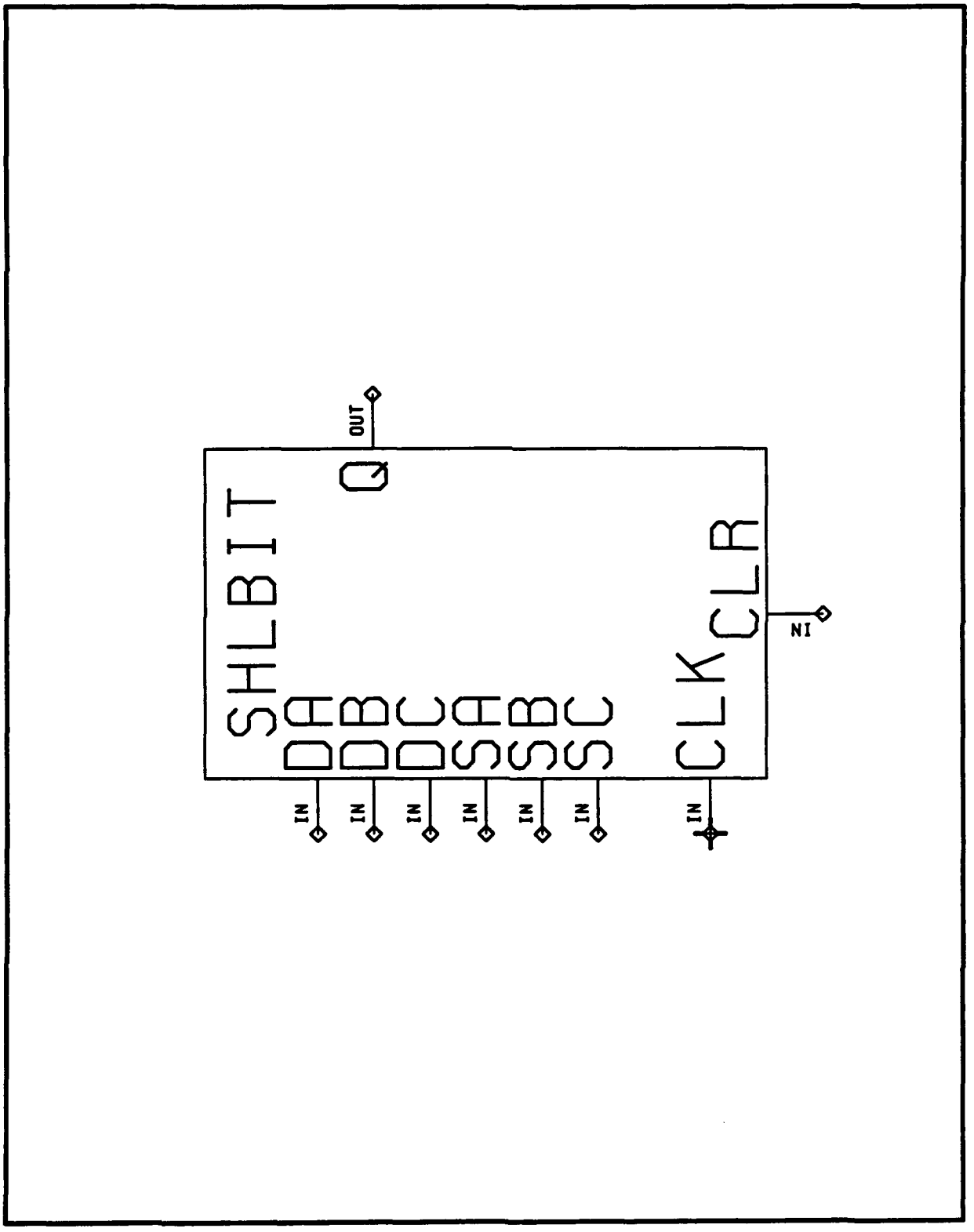

SHIFT16
DOUT(15:12)
DOUT(11:8)
DOUT(7:4)
DOUT(3:0)
SHIFTV
PIPE(15:8)
MCS(15:8)
SDIN
SELS16
SELP16
SELW16
CLK16
CLR16

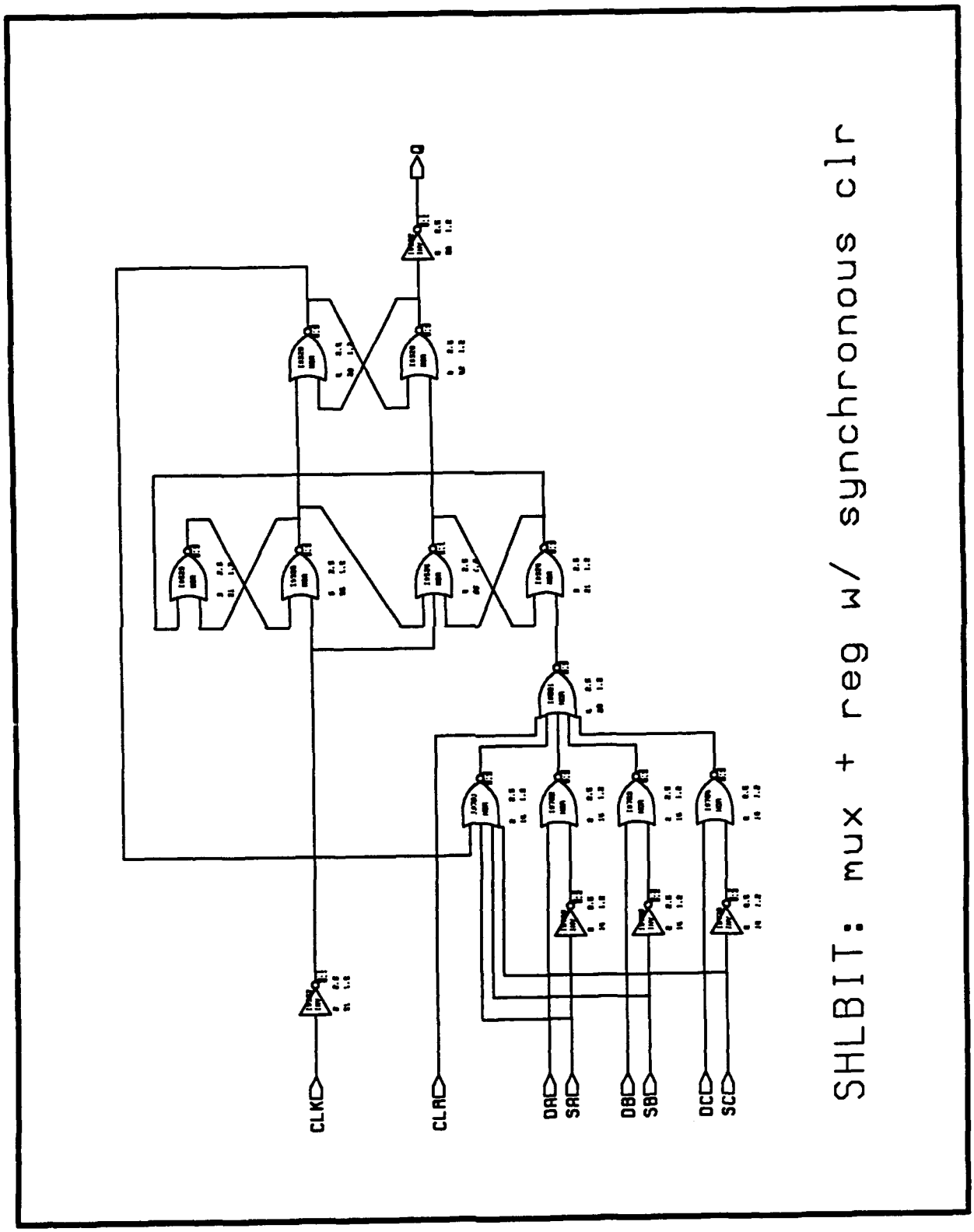

SHIFT4
SDIN
PIPE(3:0)
WCS(3:0)
SELS4
SELP4
SELW4
CLK4
DOUT(3:0)
UXX
CLR4

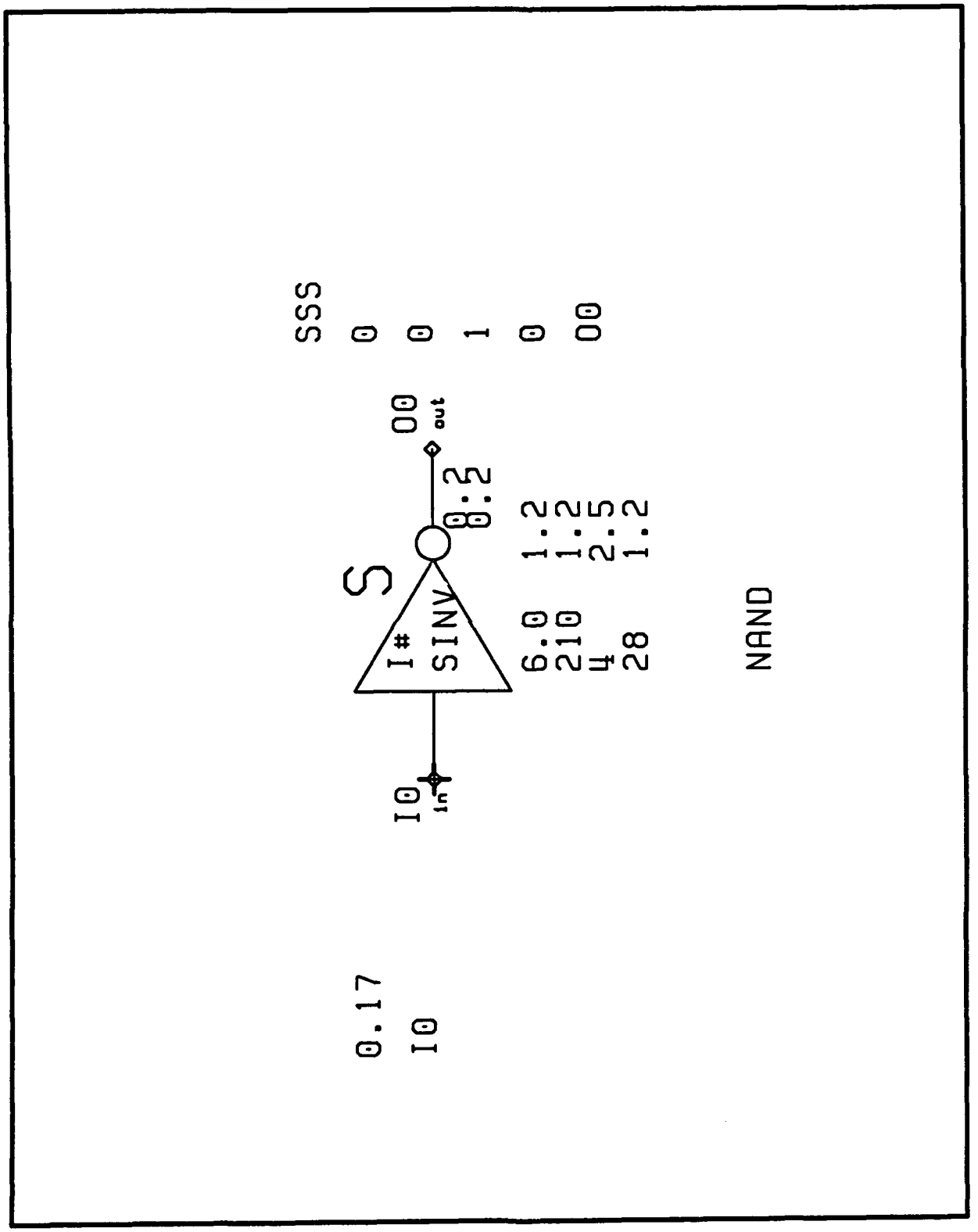

SHIFT4
DOUT(3:0)
SHLBIT
CLK
PIPE(3:0)
WCS(3:0)
SELS4
SELP4
SELW4
SDIN
CLK4
CLR4

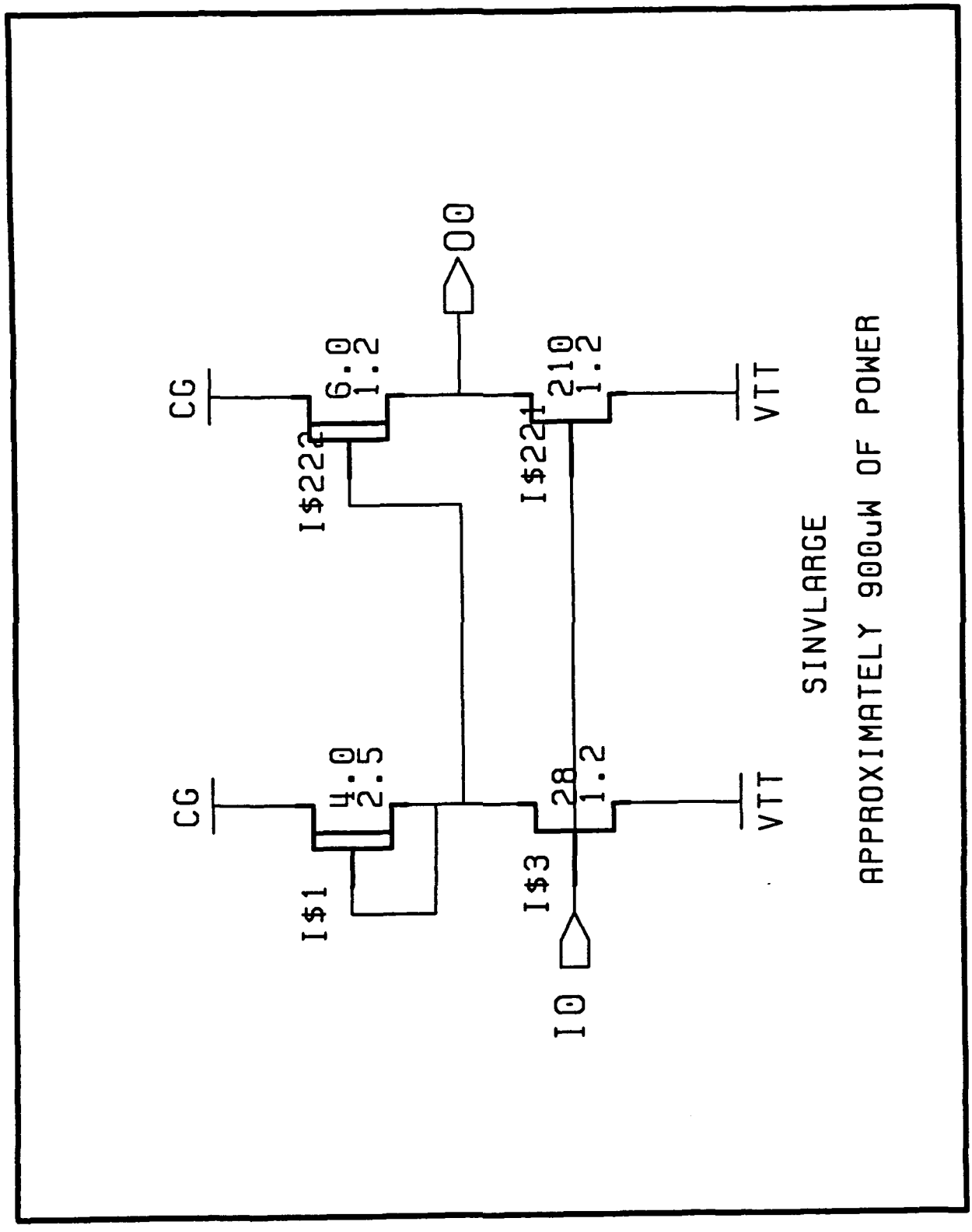

SHIFTREG
WCS(11:0)
PIPE(11:0)
SDIN
SELS(6:0)
SELW(6:0)
SELP(6:0)
CLK(6:0)
CLR(6:0)
DOUT(11:0)
U2

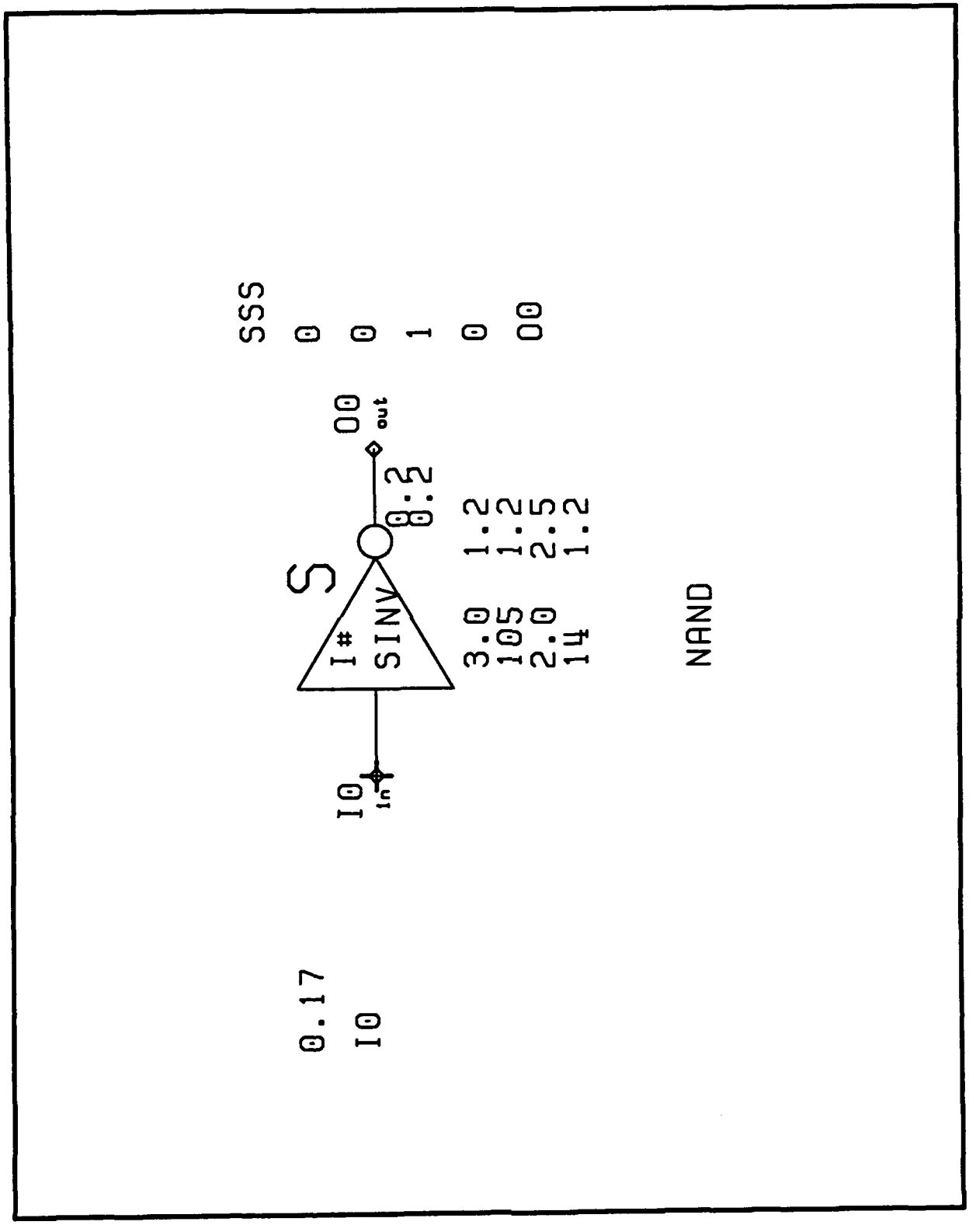

SHIFTREG
SHIFT16
DOUT (111:0)
PIPE (111:0)
NCS (111:0)
SELS (8:0)
SELP (8:0)
SELN (8:0)
SDIN
CLK (8:0)
CLR (8:0)

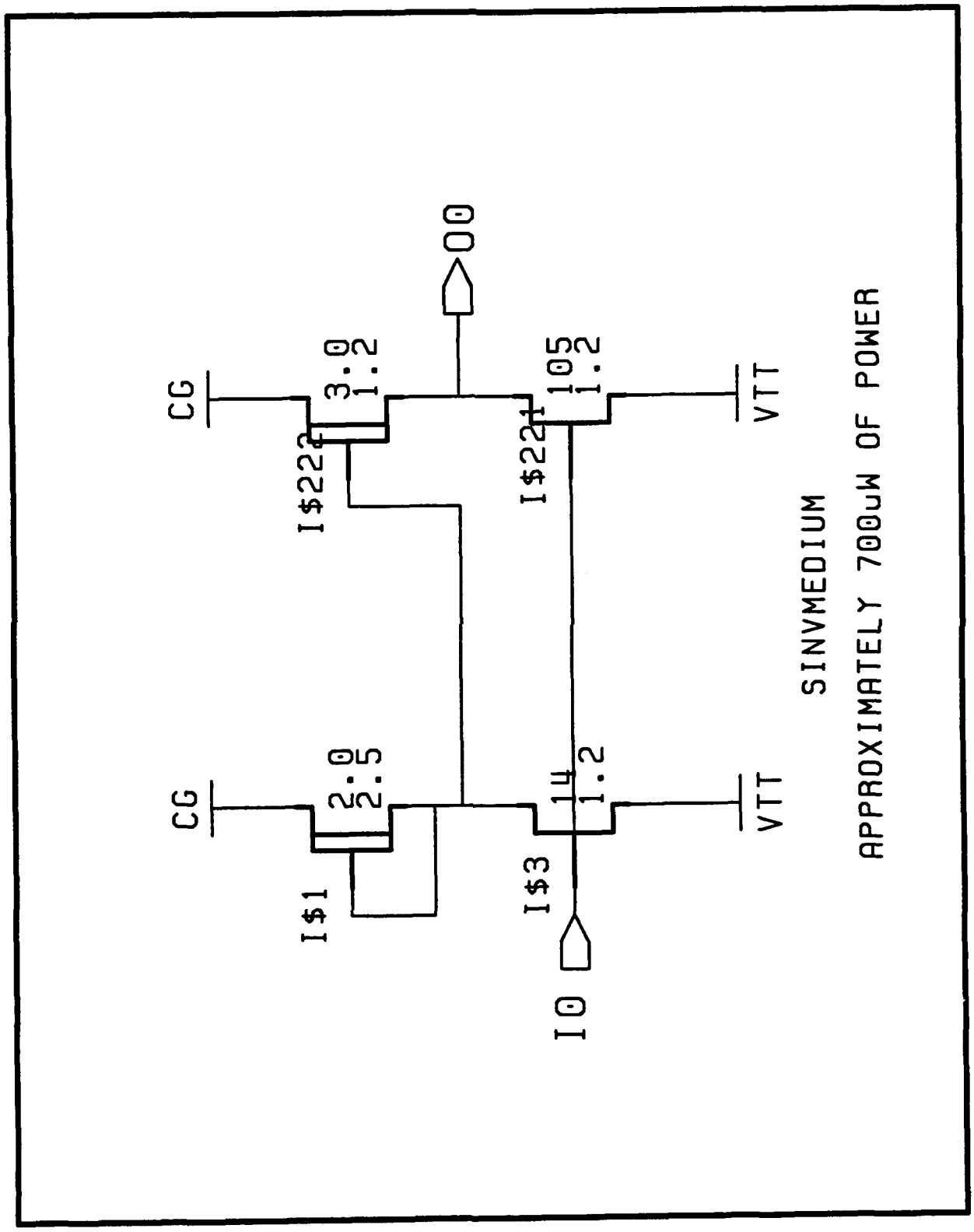

OUT
Q
SHLBIT
SA
SB
SC
DA
DB
DC
CLK
CLR
NI
IN
IN
IN
IN
IN
IN
IN

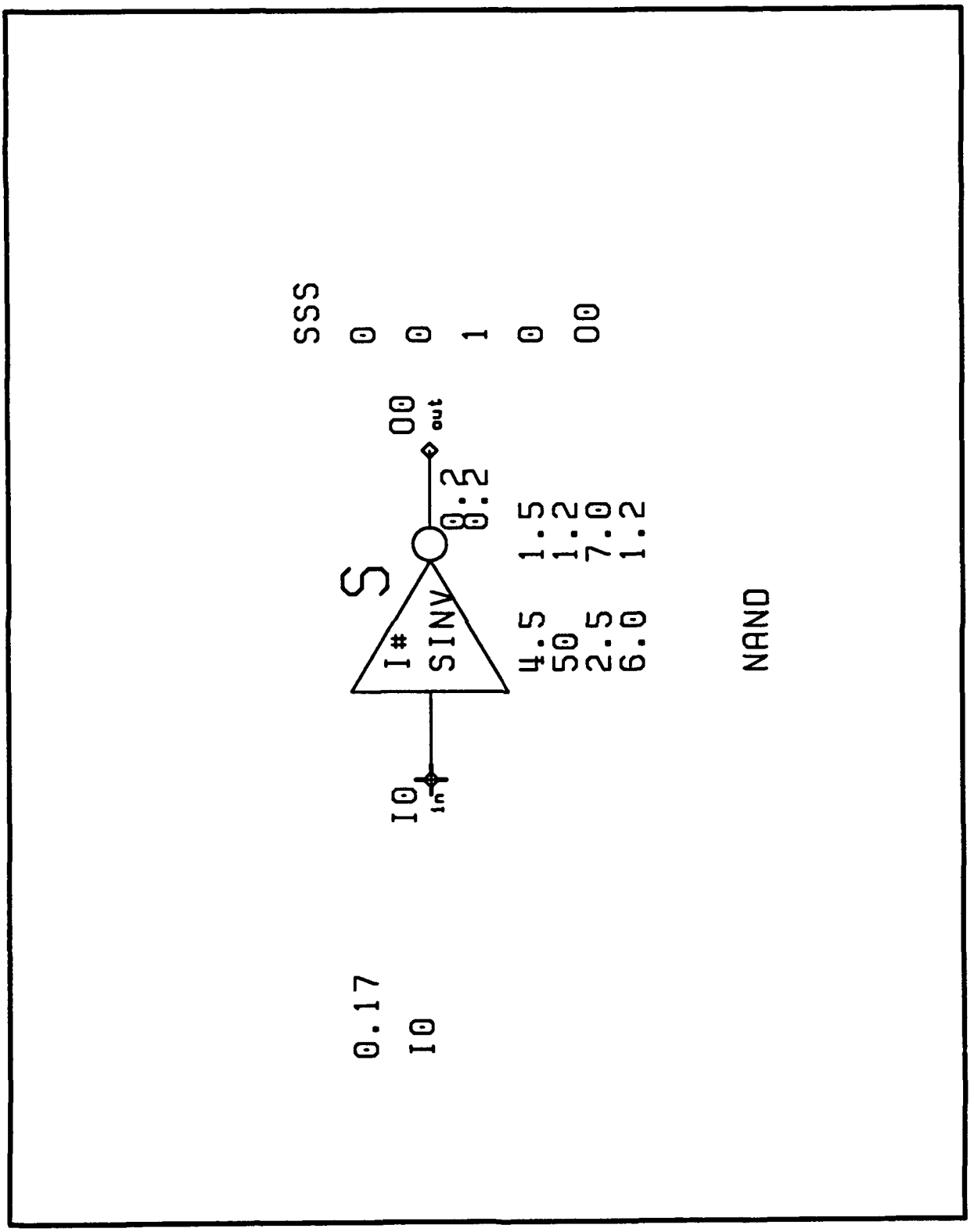

SHLBIT: mux + reg w/ synchronous clr
Q
CLK
CLR
DA
SA
DB
SB
DC
SC

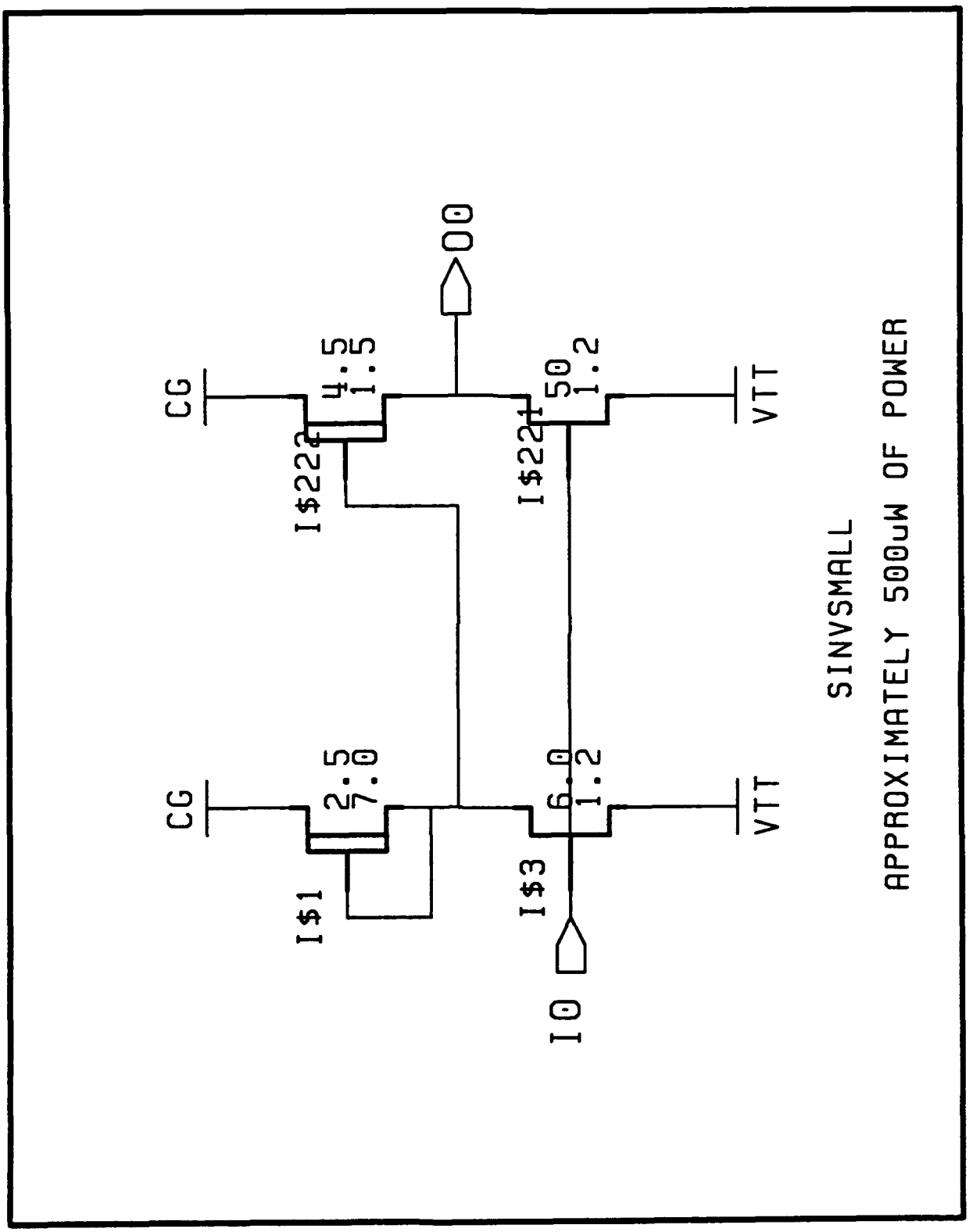

SSS
0 0 1 0 00
00
out
8.2
S
I#
SINV
6.0 1.2
210 1.2
4 2.5
28 1.2
NAND
IO
in
0.17
IO

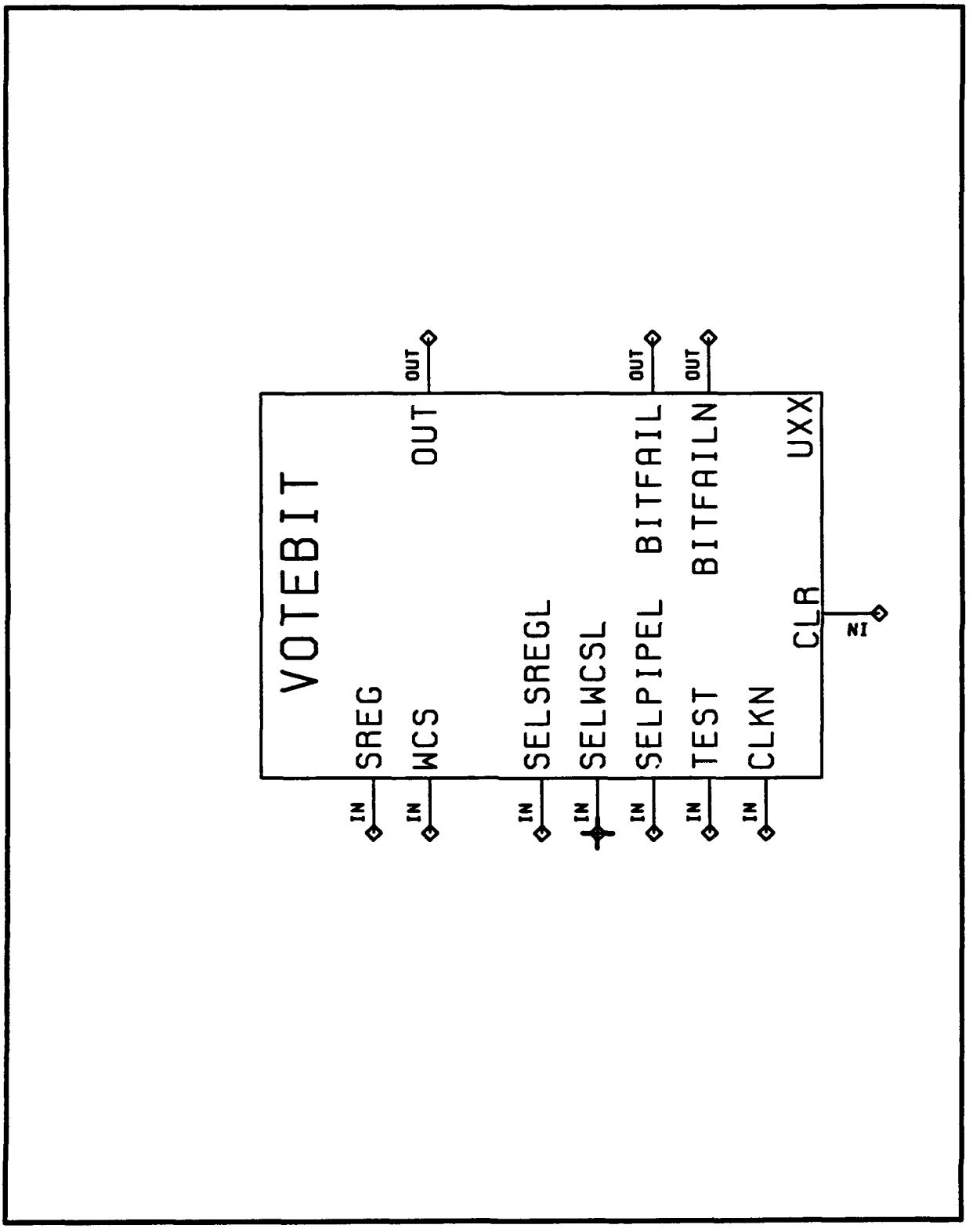

O0
CG
6.0
1.2
I$22
210
1.2
I$21
VTT
SINVLARGE
APPROXIMATELY 900uW OF POWER
CG
4.0
2.5
I$1
28
1.2
I$3
VTT
I0

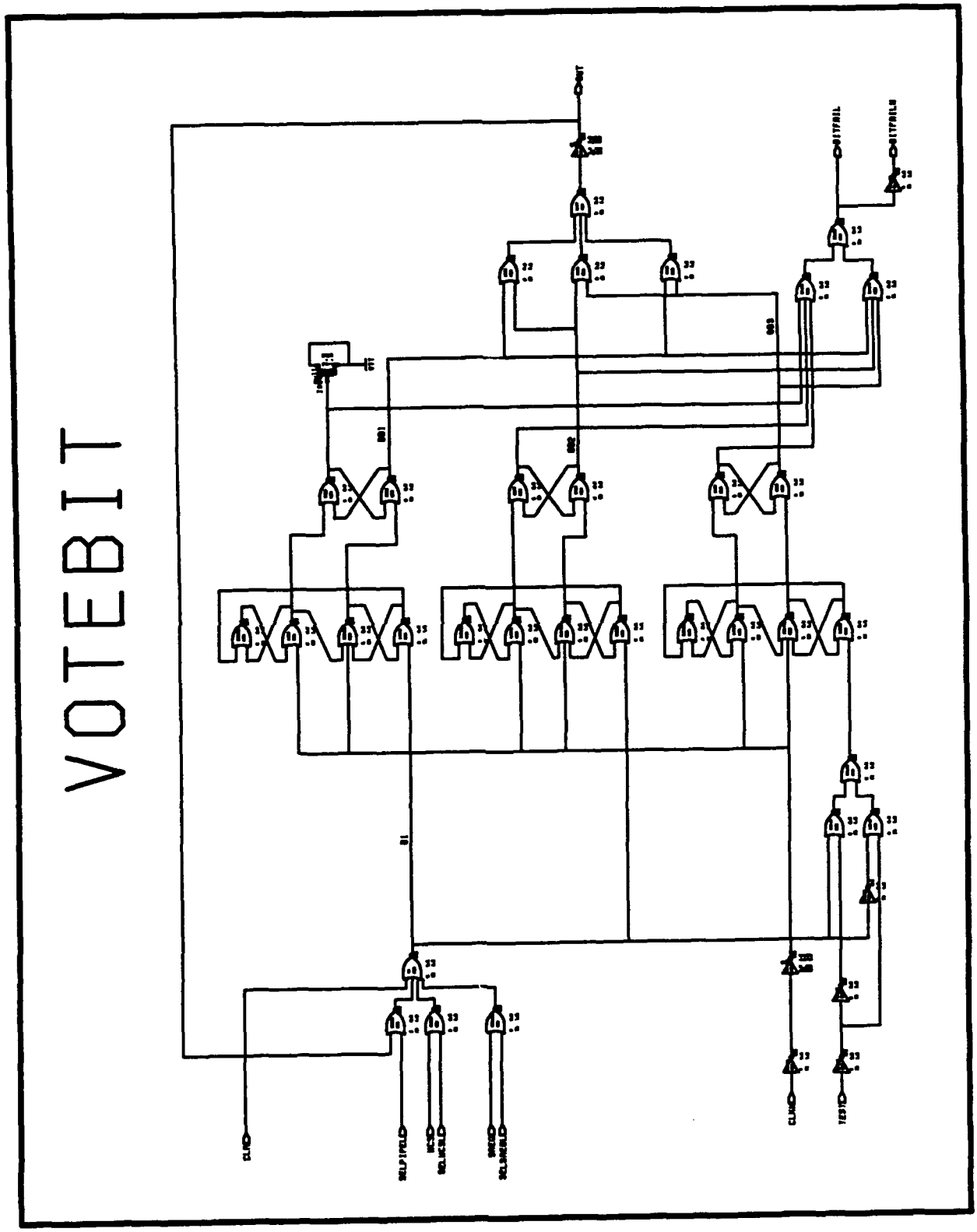

SSS
0 0 1 0 00
00
out
8.2
1.2
1.2
2.5
1.2
S
I#
SINV
3.0
105
2.0
14
NAND
IO
in
0.17
IO

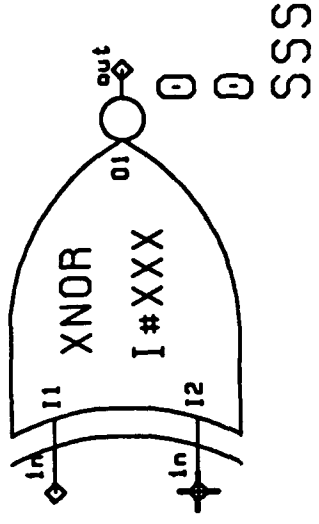

O0
CG
3.0
1.2
I$22
105
1.2
I$21
VTT
SINVMEDIUM
APPROXIMATELY 700uW OF POWER
CG
2.0
2.5
I$1
14
1.2
I$3
VTT
IO

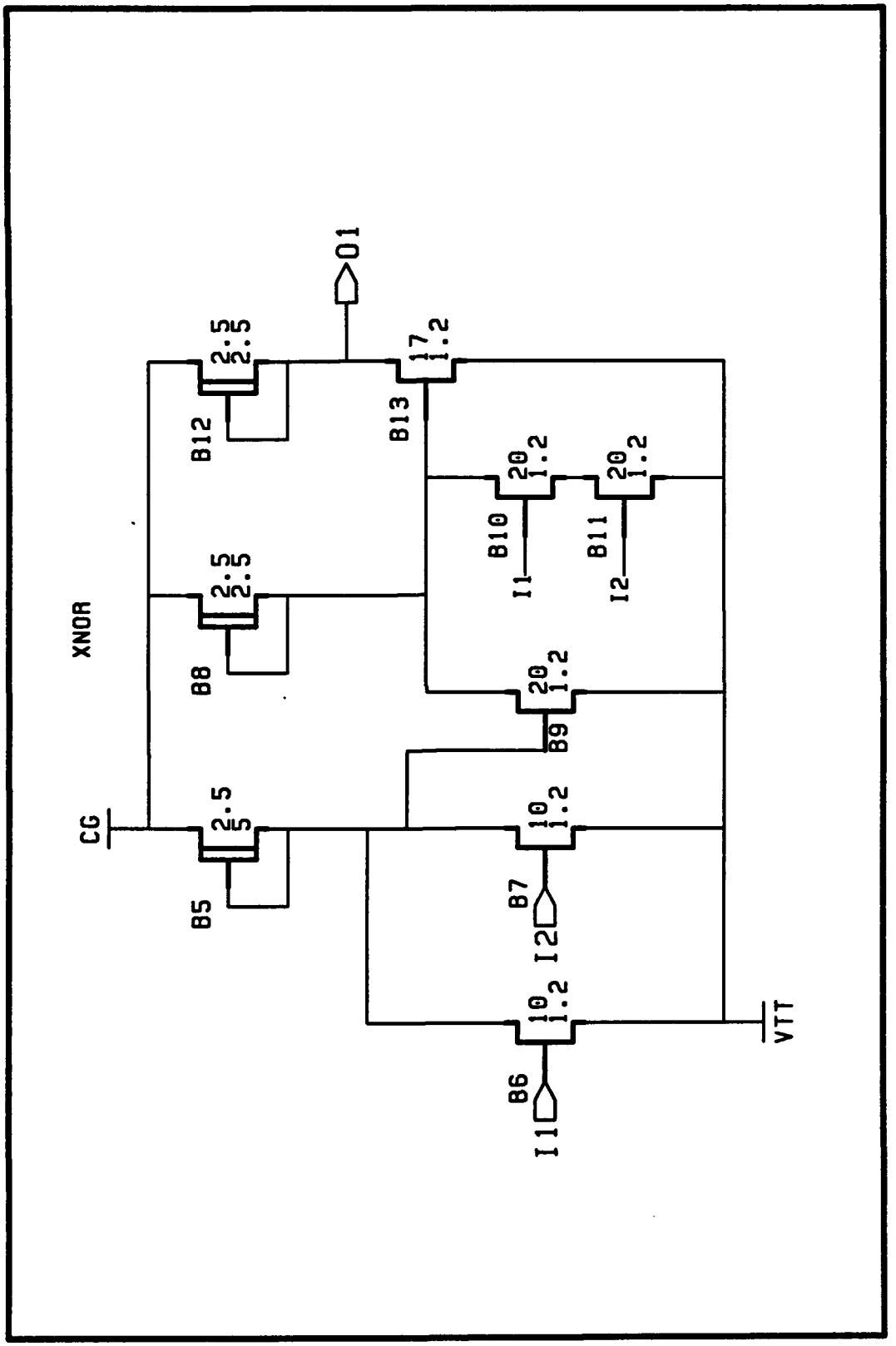

SSS
0 0 1 0 00
00
out
8.2
S
I# SINV
4.5 1.5
50 1.2
2.5 7.0
6.0 1.2
NAND
IO
in
0.17
IO

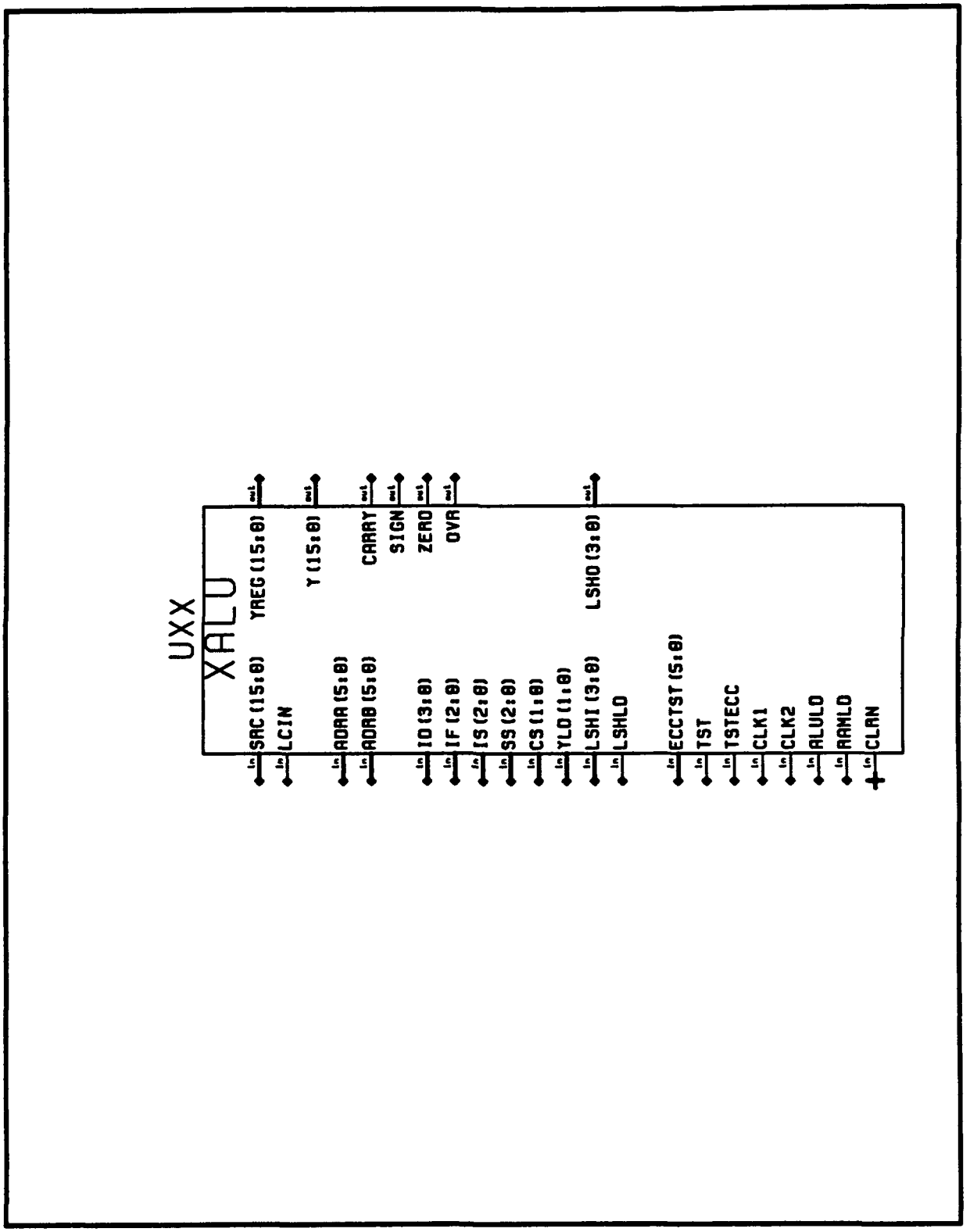

SINVSMALL
APPROXIMATELY 500uW OF POWER
CG
4.5
1.5
I$22
O0
50
1.2
I$21
VTT
CG
2.5
7.0
I$1
6.0
1.2
I$3
VTT
IO

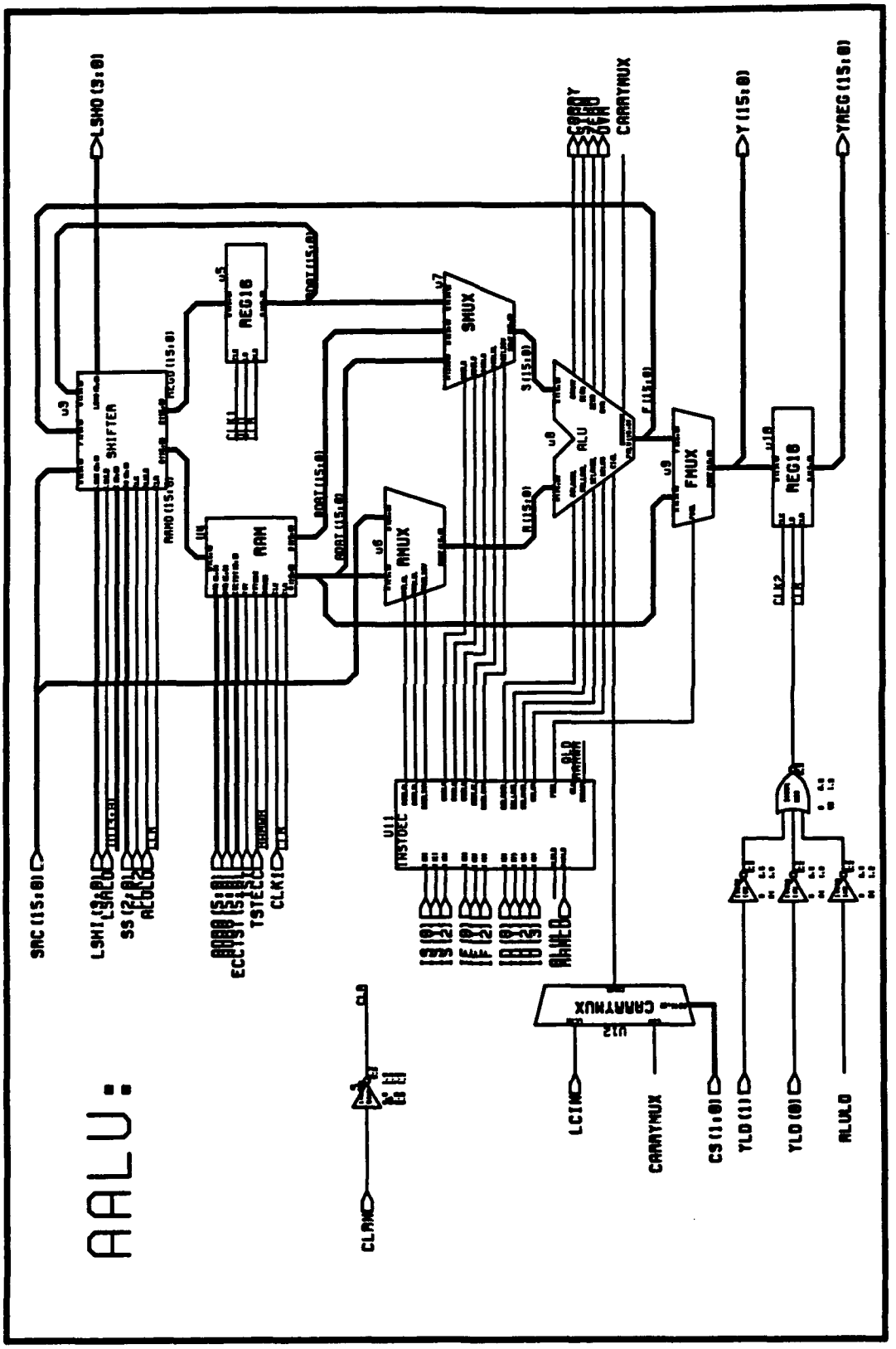

VOTEBIT
SREG
WCS
SELSREGL
SELWCSL
SELPIPEL
TEST
CLKN
CLR
BITFAILN
BITFAIL
UXX
OUT
IN
NI

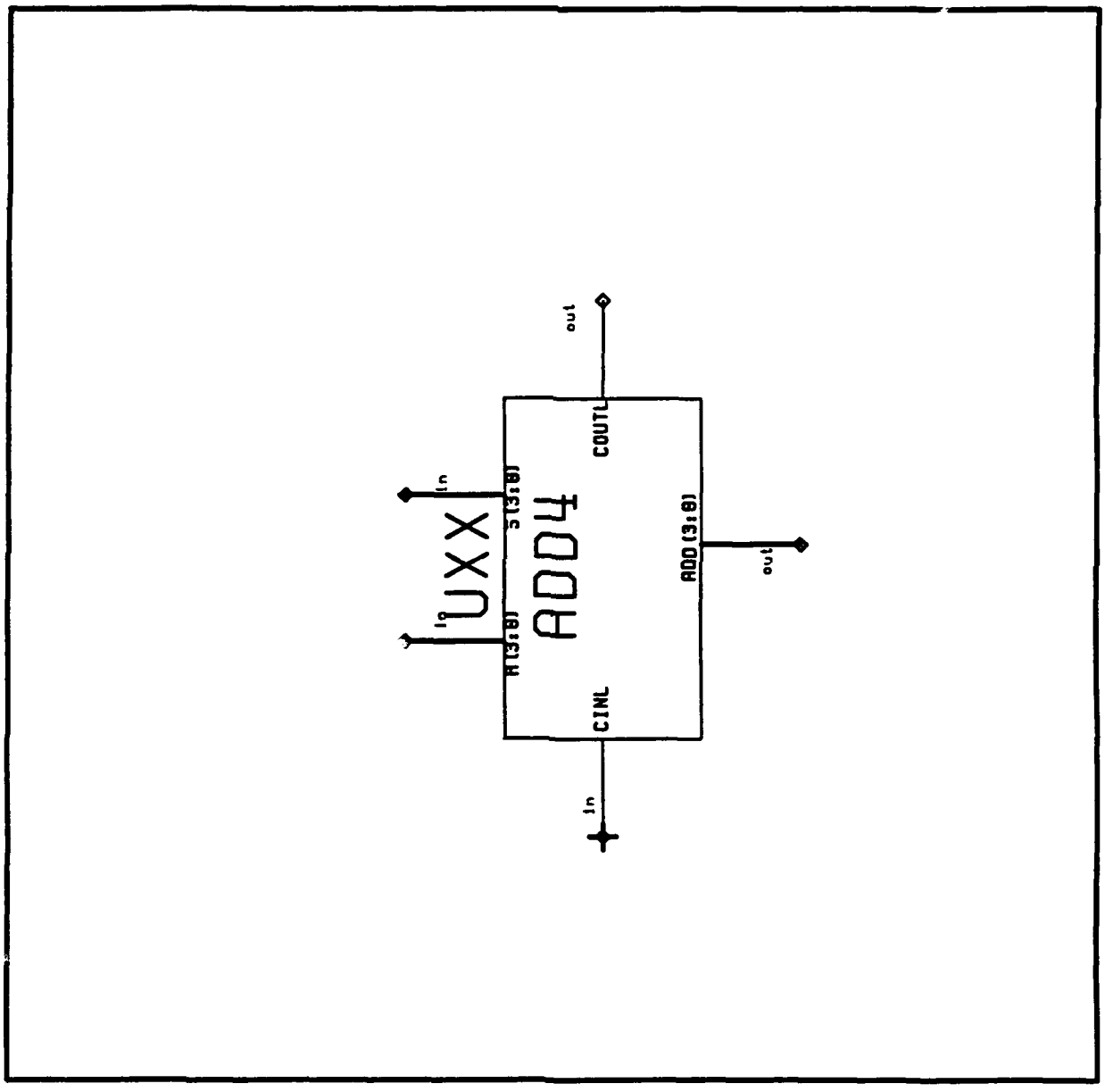

VOTEBIT

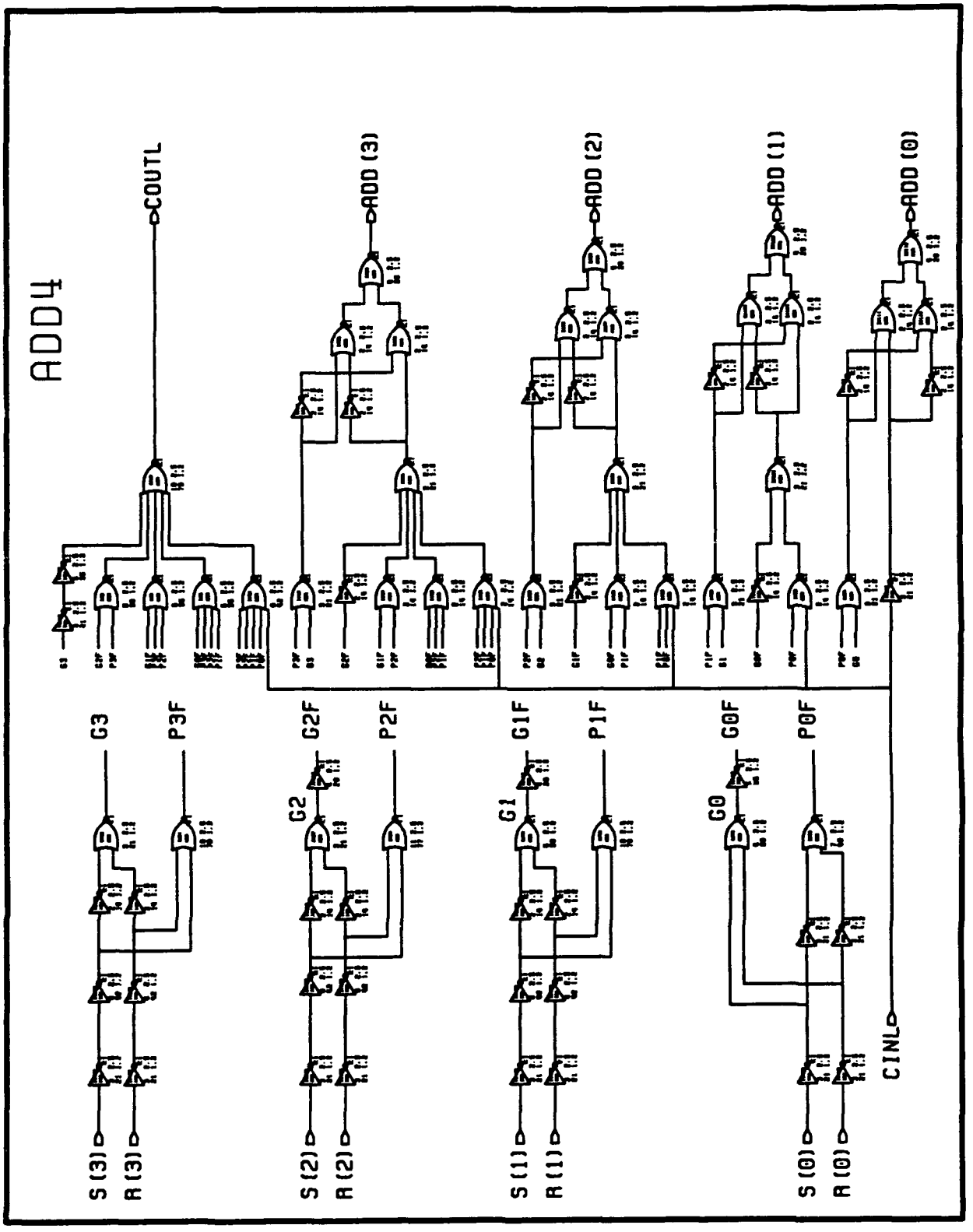

SSS
0
0
out
o1
XNOR
I#XXX
i1
i2
in
in

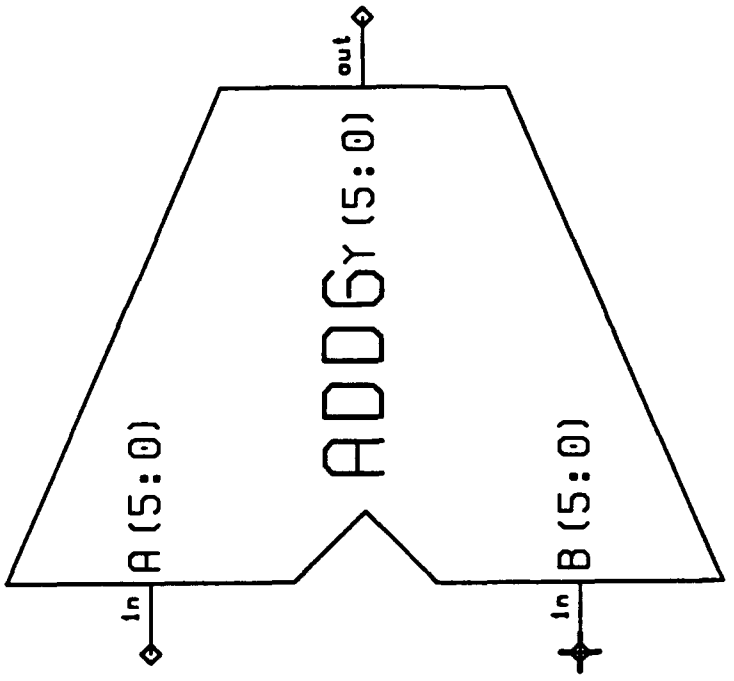

O1
2.5
2.5
B12
17
1.2
B13
20
1.2
B10
I1
20
1.2
B11
I2
XNOR
2.5
2.5
B8
20
1.2
B9
CG
2.5
5
B5
10
1.2
B7
I2
10
1.2
B6
I1
VTT

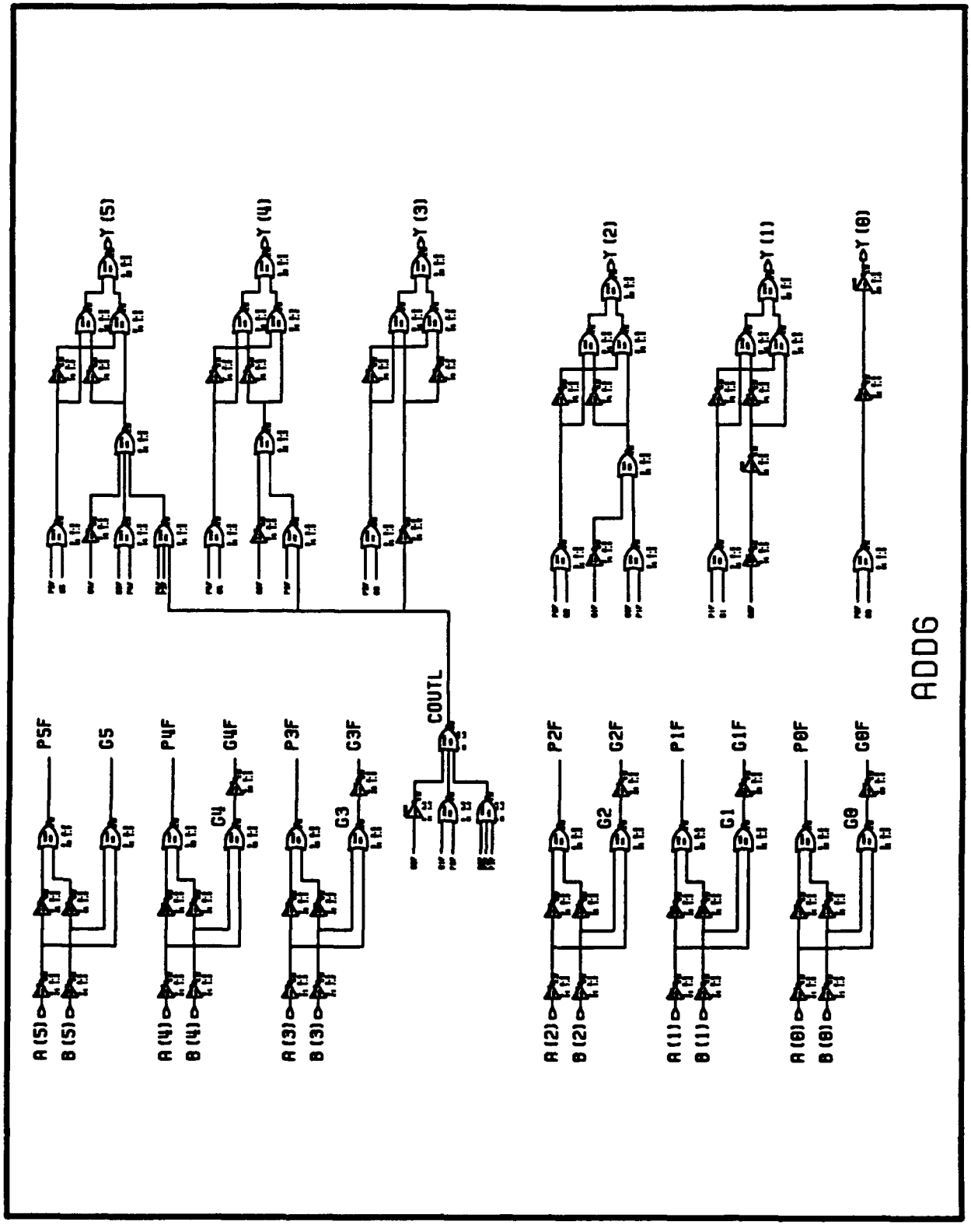

UXX
XALU
SRC (15:0)
LCIN
ADAA (5:0)
ADAB (5:0)
ID (3:0)
IF (2:0)
IS (2:0)
SS (2:0)
CS (1:0)
YLD (1:0)
LSHI (3:0)
LSHLD
ECCTST (5:0)
TST
TSTECC
CLK1
CLK2
ALULD
RAMLD
CLAN
YREG (15:0)
Y (15:0)
CARRY
SIGN
ZERO
OVR
LSHO (3:0)

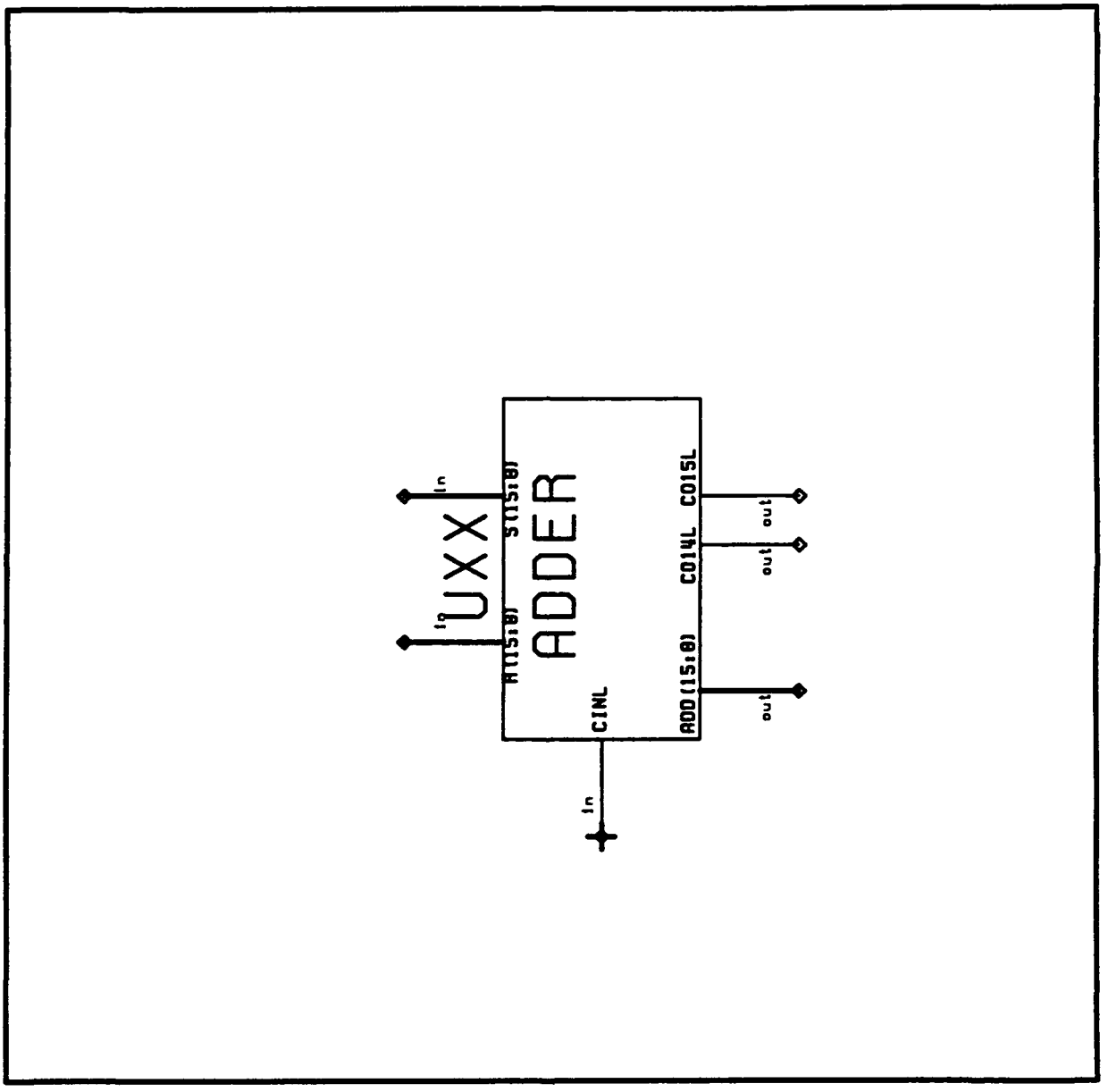

ALU:
LSHO (3:0)
CARRY
OVR
CARRYMUX
Y (15:0)
YREG (15:0)
REG16
SHIFTER
SMUX
ALU
FMUX
AMUX
RAM
SRC (15:0)
CLK1
CLK2
CLKMC
LCIMC
CARRYMUX
CS (1:0)
YLD (1)
YLD (0)
ALULD

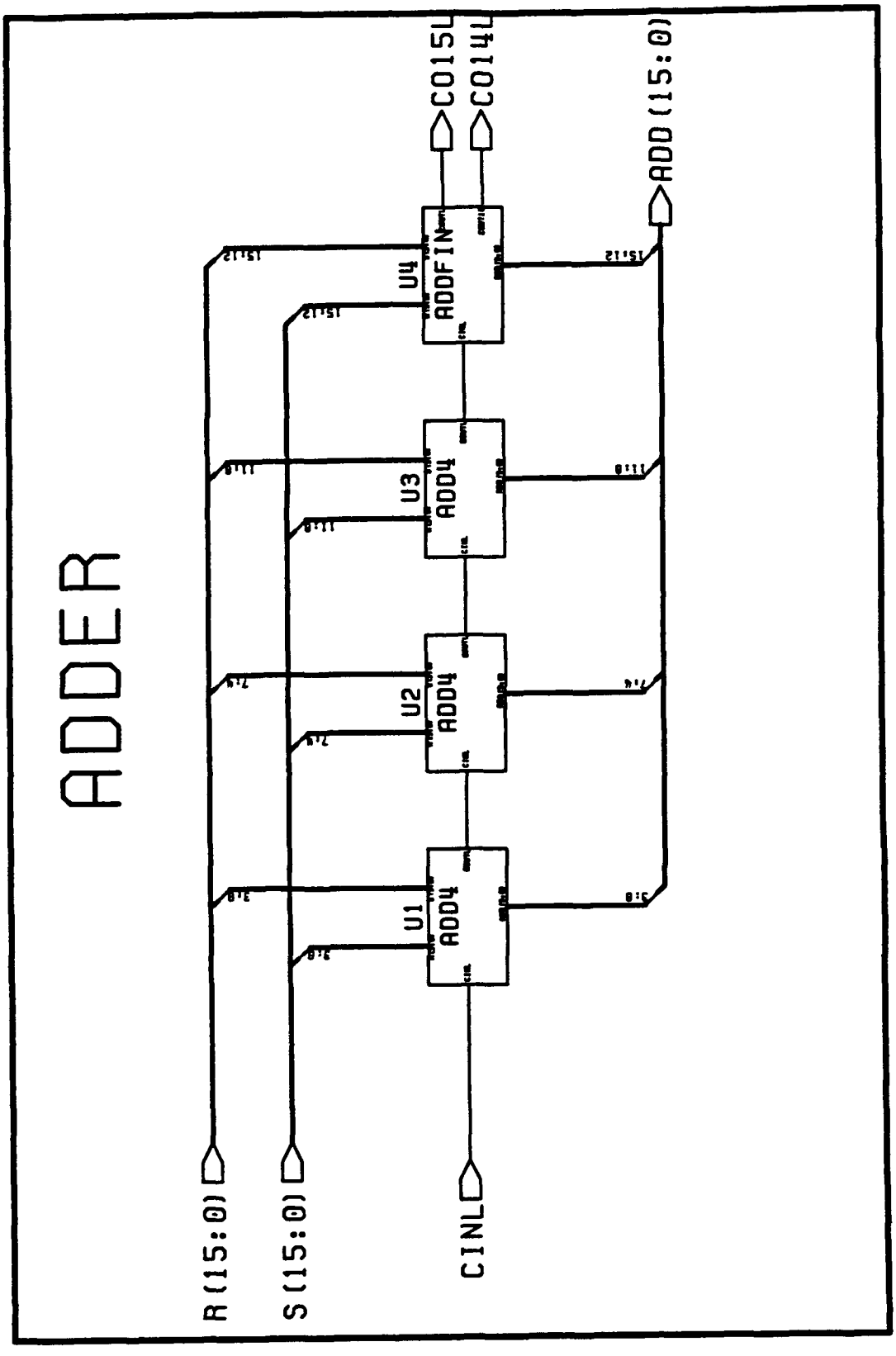

UXX
ADD4
in
A[3:0]
in
B[3:0]
CINL
in
COUTL
out
ADD[3:0]
out

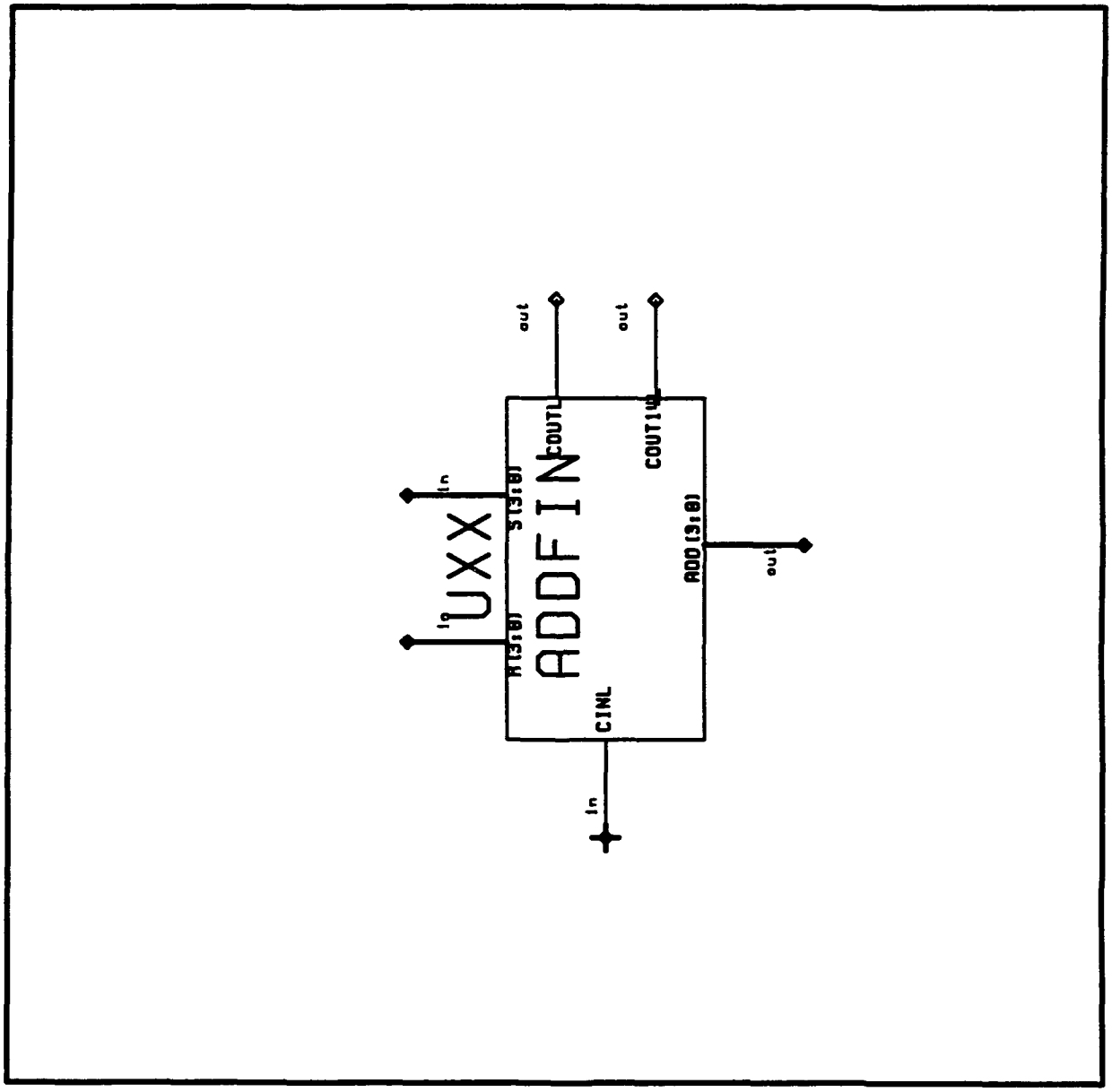

ADD4
COUTL
ADD (3)
ADD (2)
ADD (1)
ADD (0)
G3
P3F
G2F
P2F
G1F
P1F
G0F
P0F
G2
G1
G0
CINL
S(3)
R(3)
S(2)
R(2)
S(1)
R(1)
S(0)
R(0)

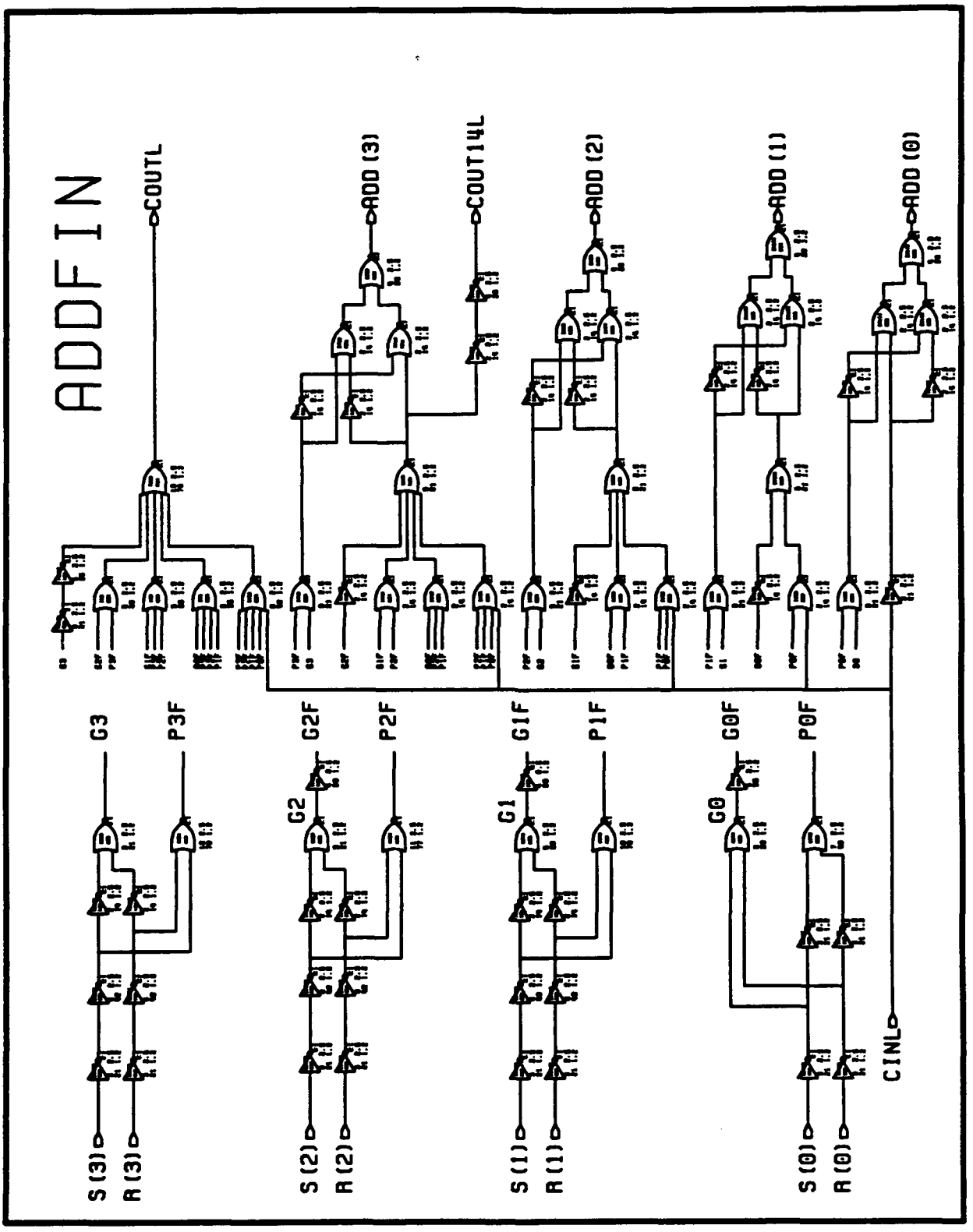

out
ADDSY(5:0)
A(5:0)
B(5:0)
in
in

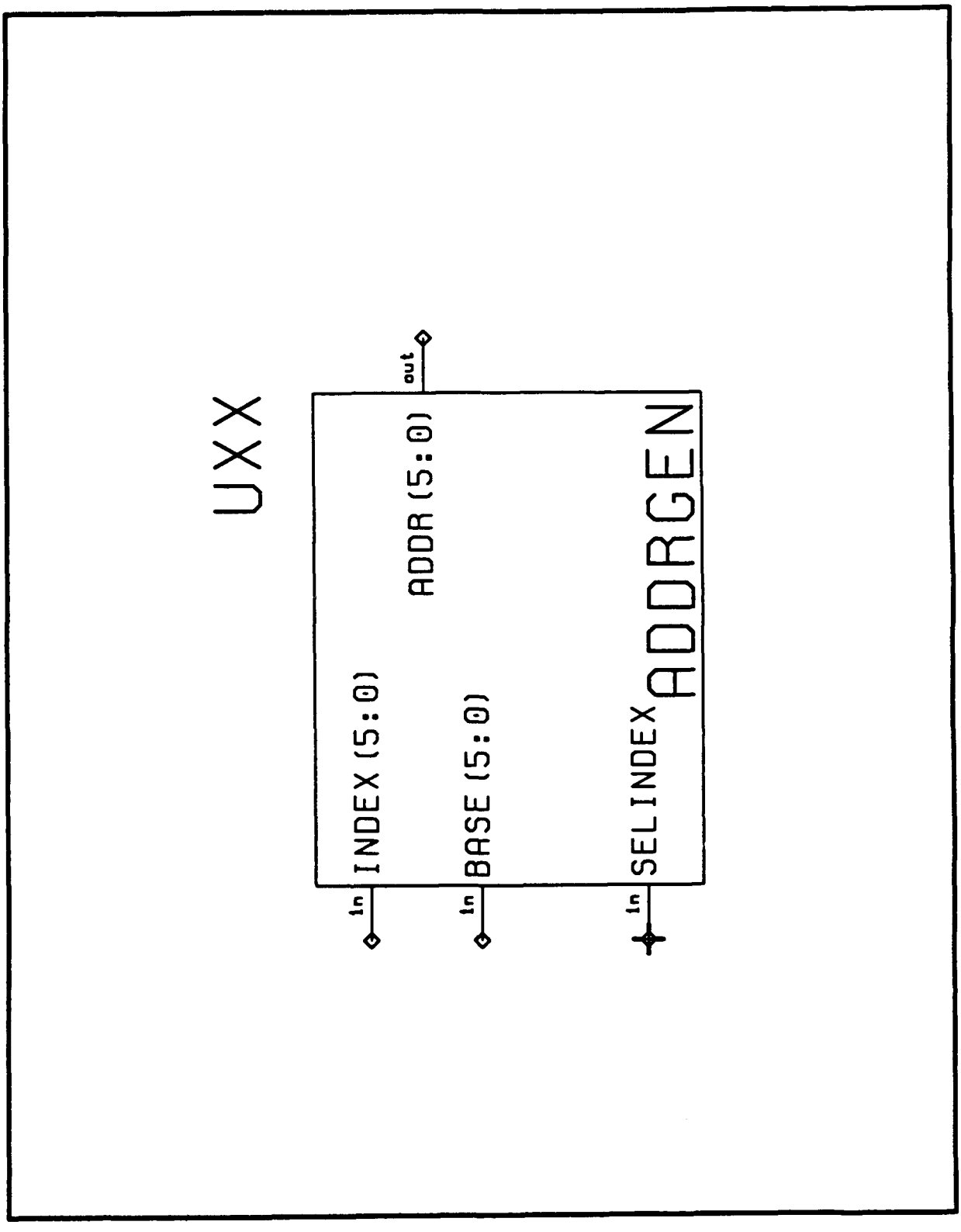

ADD6
Y (5)
Y (4)
Y (3)
Y (2)
Y (1)
Y (0)
COUTL
P5F
G5
P4F
G4F
P3F
G3F
P2F
G2F
P1F
G1F
P0F
G0F
G4
G3
G2
G1
G0
A (5)
B (5)
A (4)
B (4)
A (3)
B (3)
A (2)
B (2)
A (1)
B (1)
A (0)
B (0)

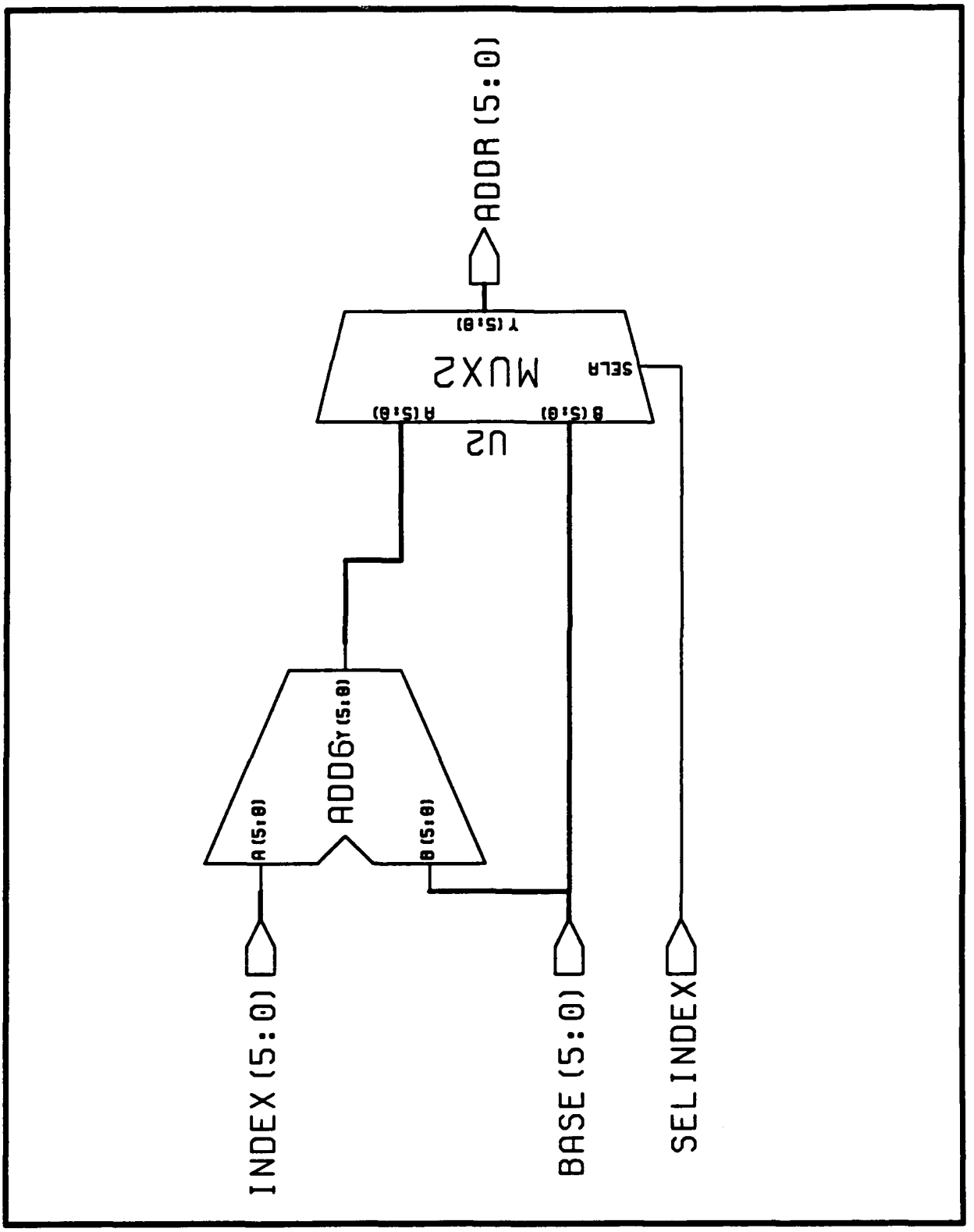

UXX
ADDER
in
in
in
S[15:0]
A[15:0]
CIN
C15
C14
ADD[15:0]
out
out
out

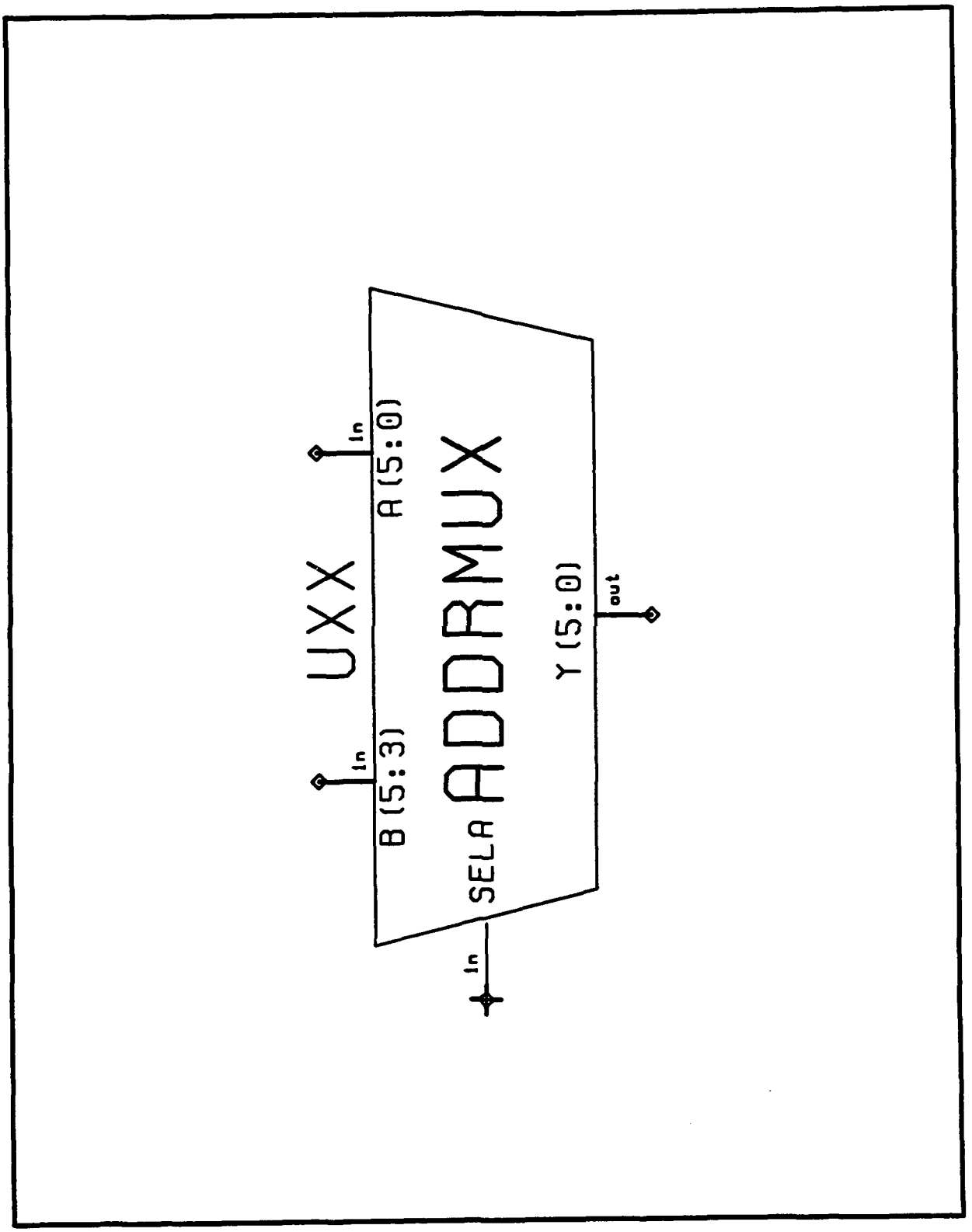

ADDER
C015L
C014L
ADD(15:0)
U4
ADDFIN
U3
ADD4
U2
ADD4
U1
ADD4
R(15:0)
S(15:0)
CINL

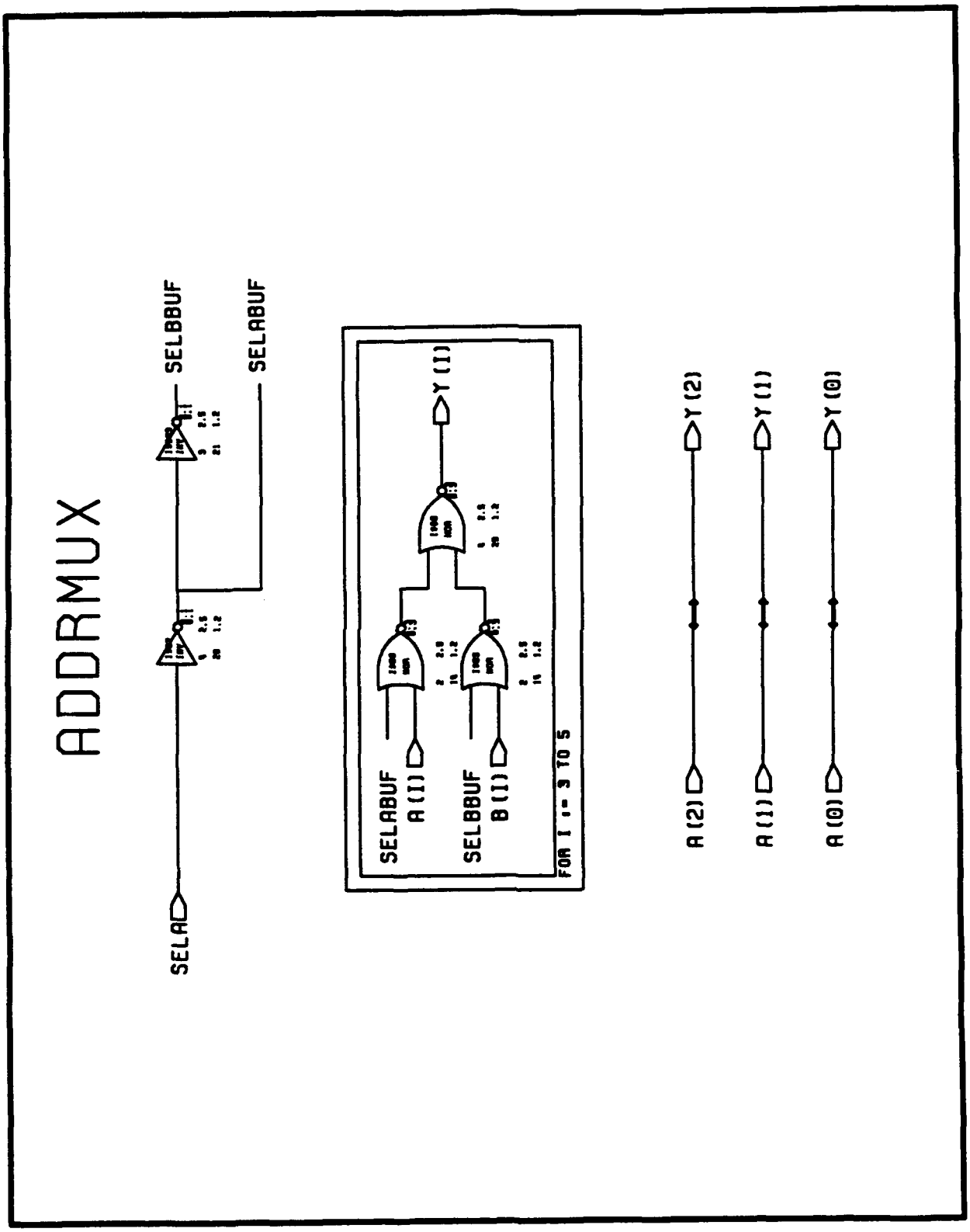

UXX
ADDFIN
A[3:0]
B[3:0]
CIN
COUT
COUT1
ADD[3:0]
in
in
out
out
out

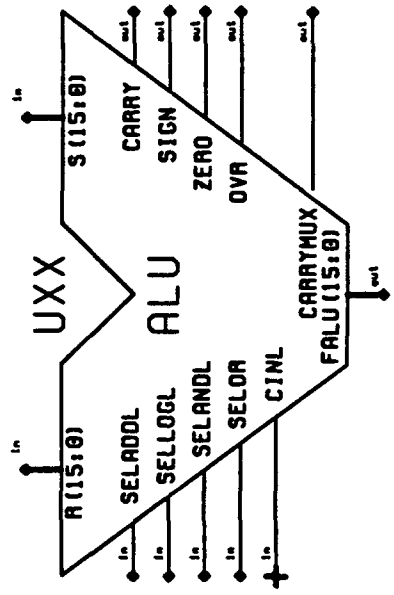

ADDFIN
COUTL
ADD(3)
COUT14L
ADD(2)
ADD(1)
ADD(0)
G3
P3F
G2F
P2F
G1F
P1F
G0F
P0F
G2
G1
G0
CINL
S(3)
R(3)
S(2)
R(2)
S(1)
R(1)
S(0)
R(0)

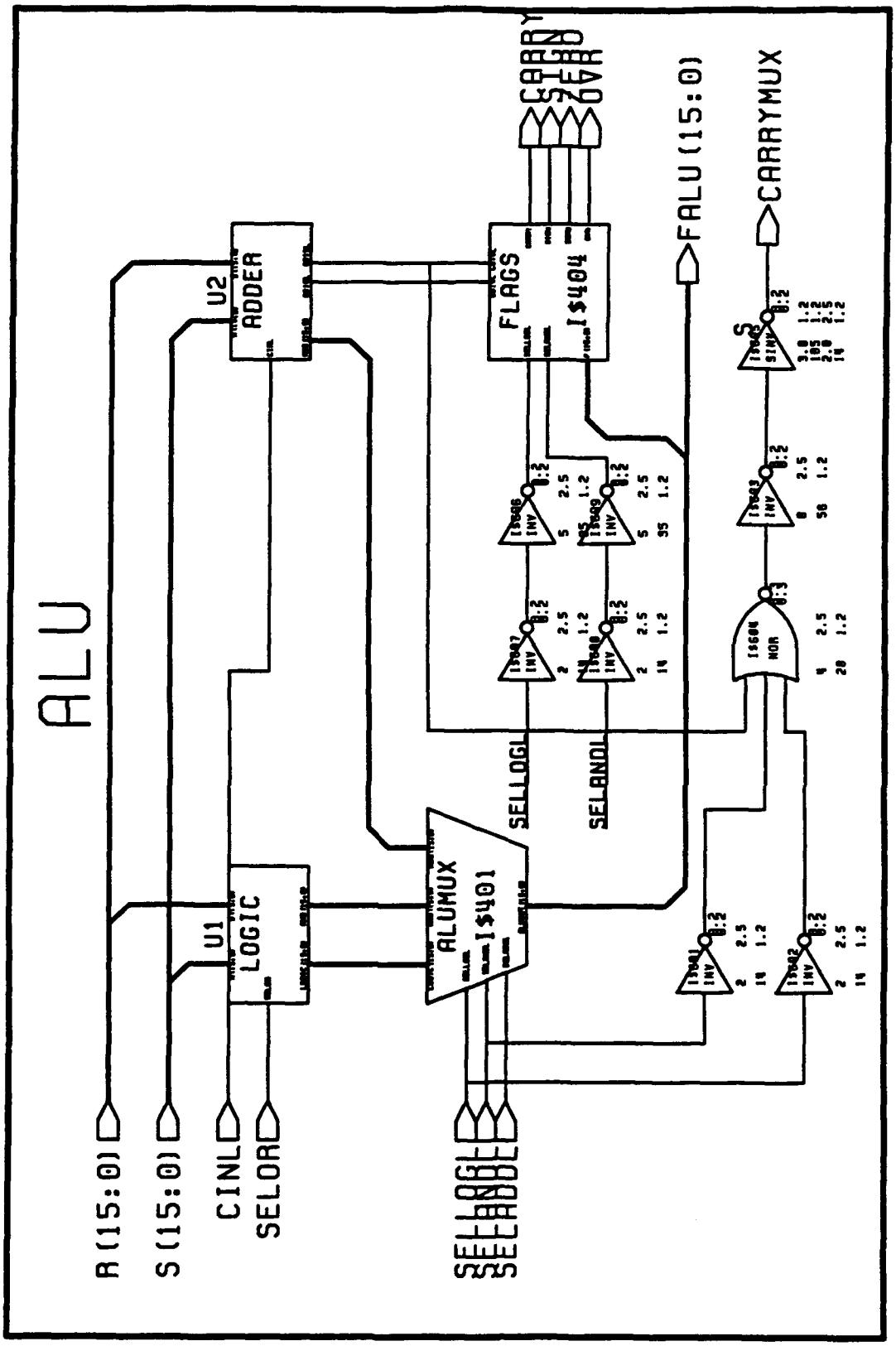

UXX
ADDRGEN
out
ADDR(5:0)
in
INDEX(5:0)
in
BASE(5:0)
in
SELINDEX

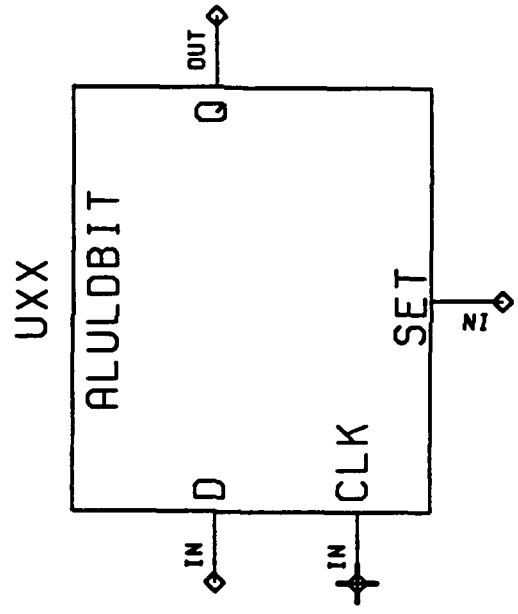

ADDR(5:0)
Y(5:0)
MUX2
SELA
B(5:0)
A(5:0)
U2
ADD6
A(5:0)
B(5:0)
INDEX(5:0)
BASE(5:0)
SELINDEX

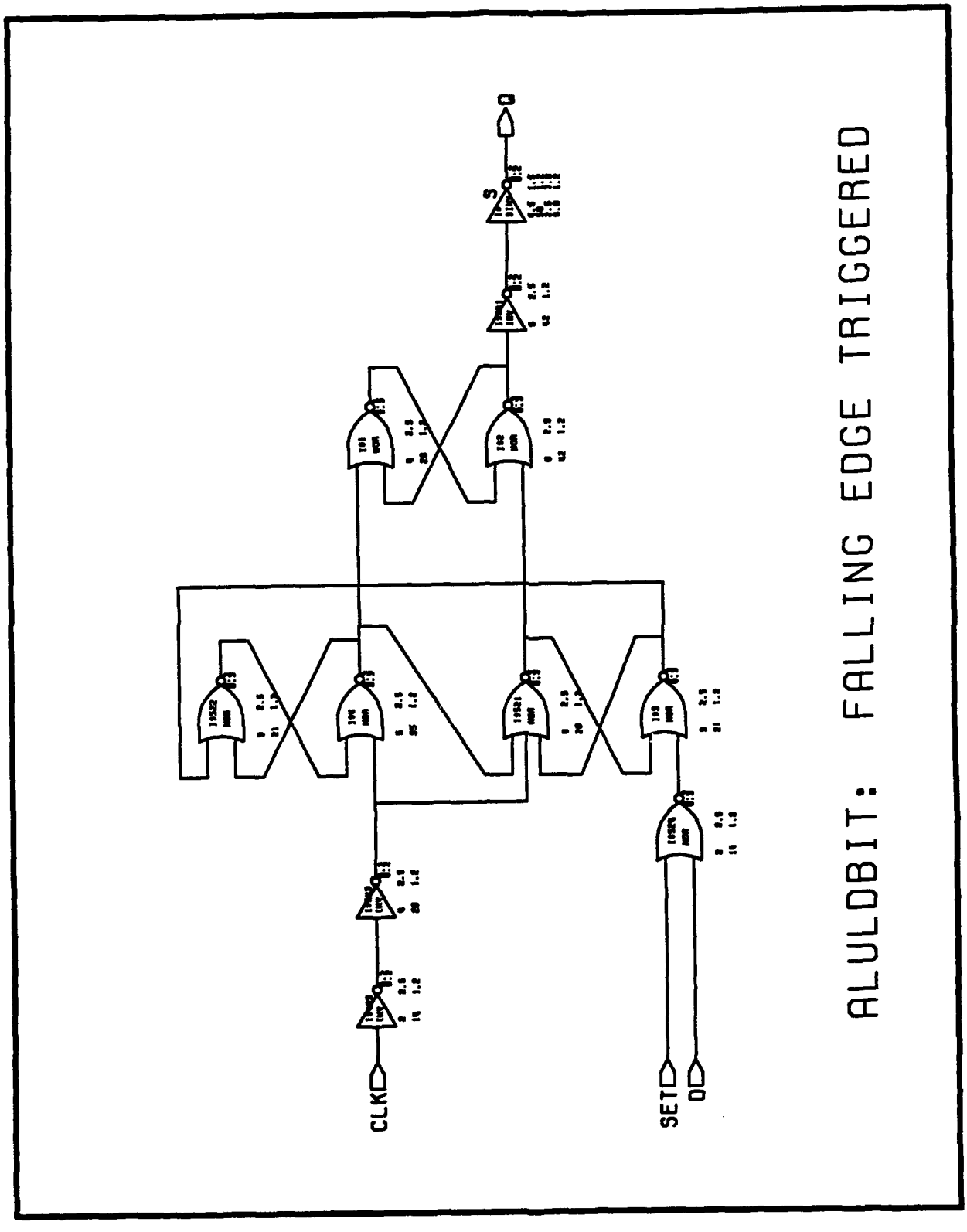

UXX
ADDRMUX
In
A(5:0)
In
B(5:3)
SELA
In
Y(5:0)
out

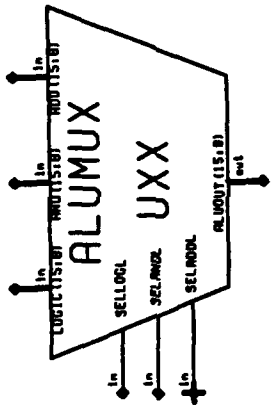

ADDRMUX
SELBBUF
SELABUF
SELA
SELABUF
A(I)
SELBBUF
B(I)
Y(I)
FOR I := 3 TO 5
A(2)
A(1)
A(0)
Y(2)
Y(1)
Y(0)

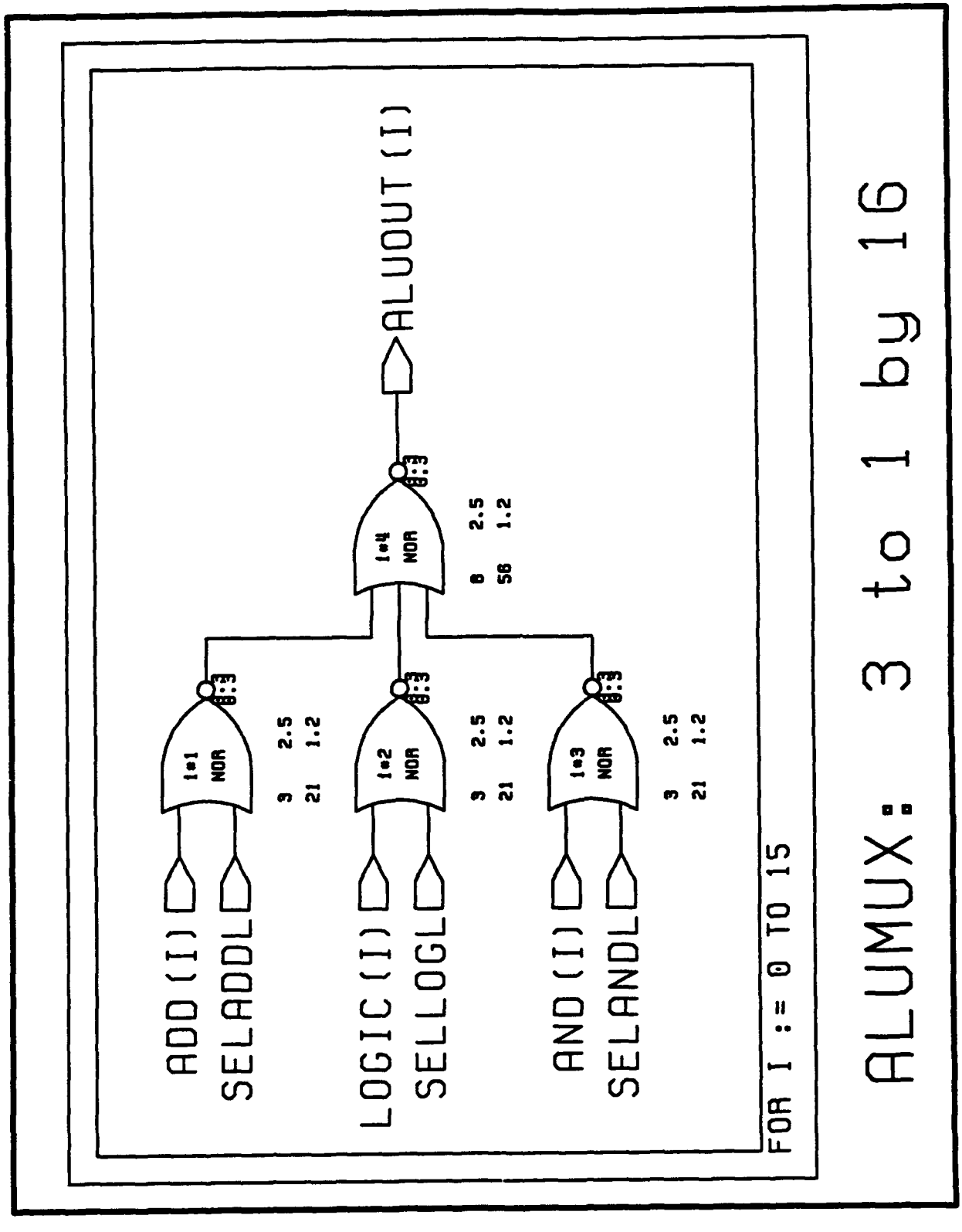

UXX
ALU
S(15:0)
R(15:0)
SELADDL
SELLOGL
SELANDL
SELOR
CINL
CARRY
SIGN
ZERO
OVR
CARRYMUX
FALU(15:0)

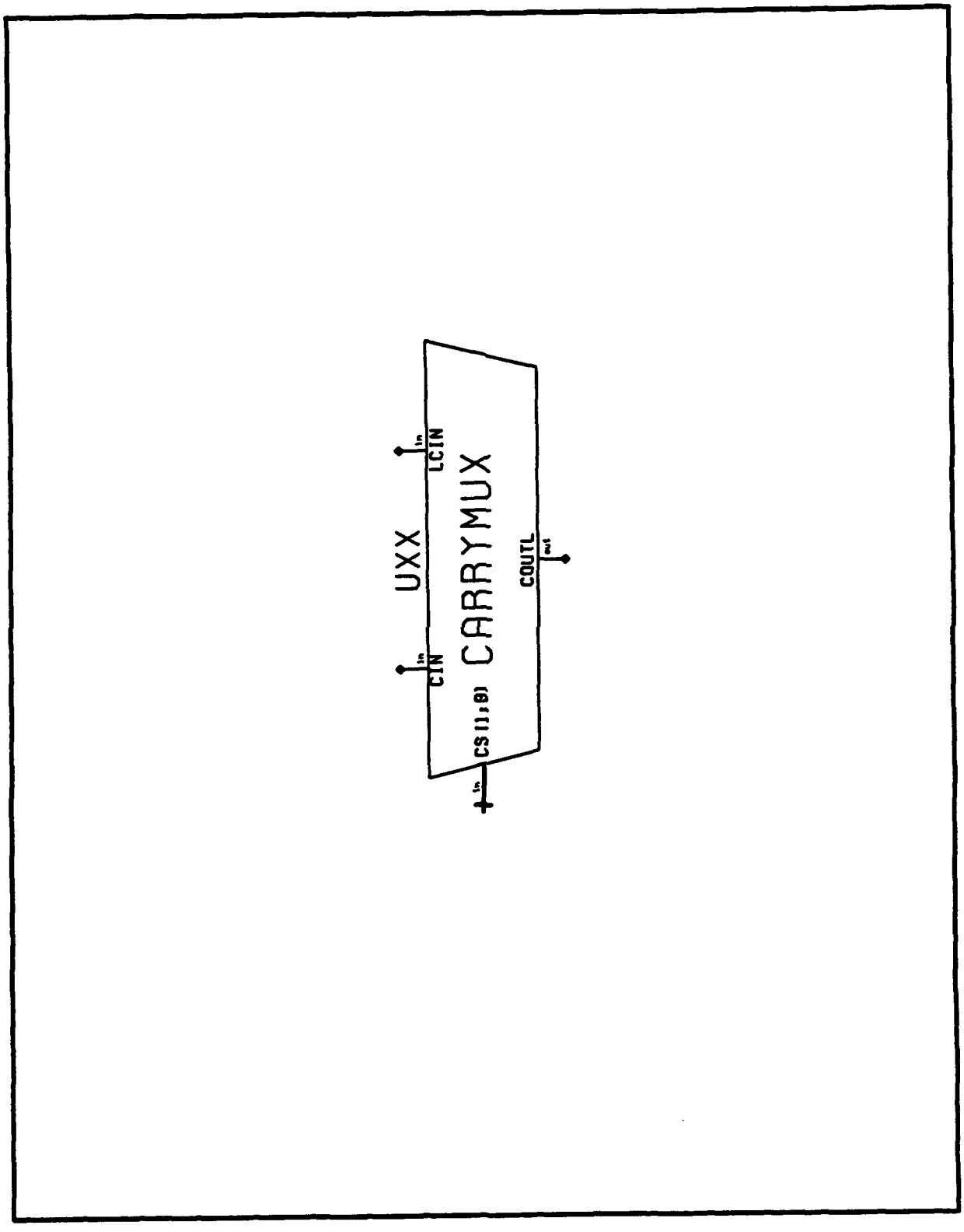

ALU
U2
ADDER
U1
LOGIC
ALUMUX
I$401
FLAGS
I$404
CARRY
SIGN
ZERO
OVR
FALU(15:0)
CARRYMUX
SELLOGL
SELANDL
R(15:0)
S(15:0)
CINL
SELORL
SELLOGL
SELADDL

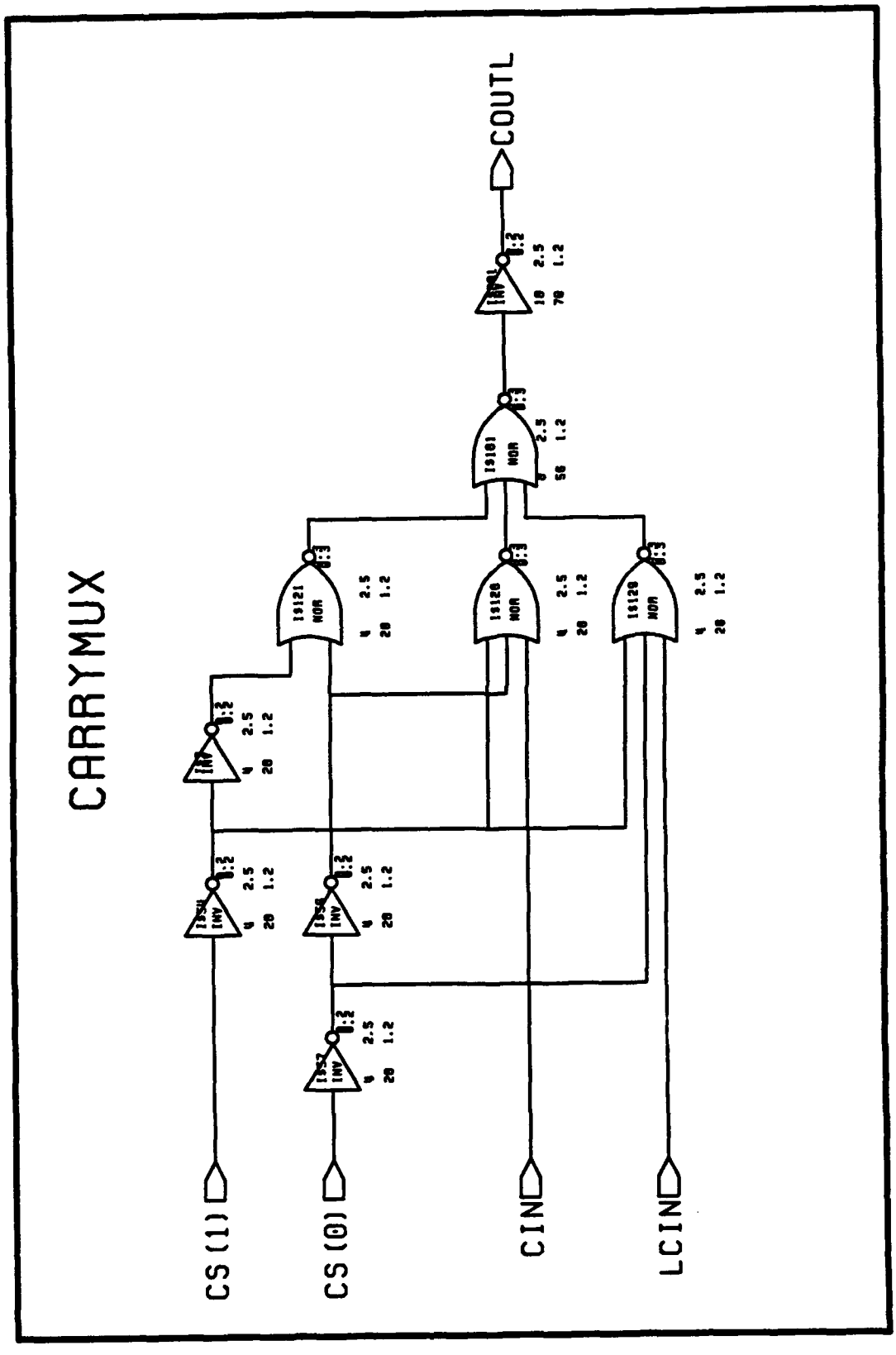

OUT
Q
UXX
ALULDBIT
SET
NI
D
CLK
IN
IN

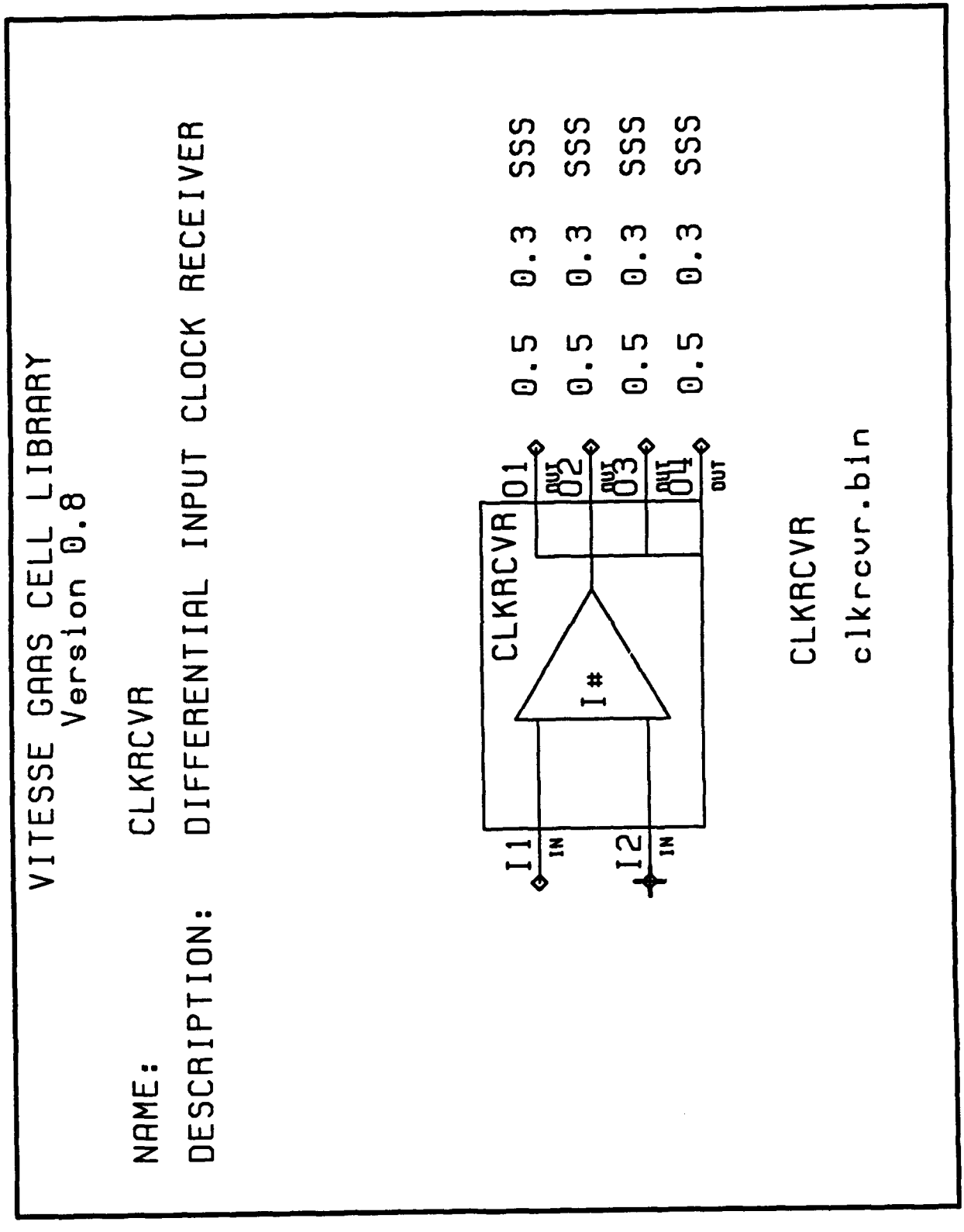

ALULDBIT: FALLING EDGE TRIGGERED
Q
S
CLK
SET
D

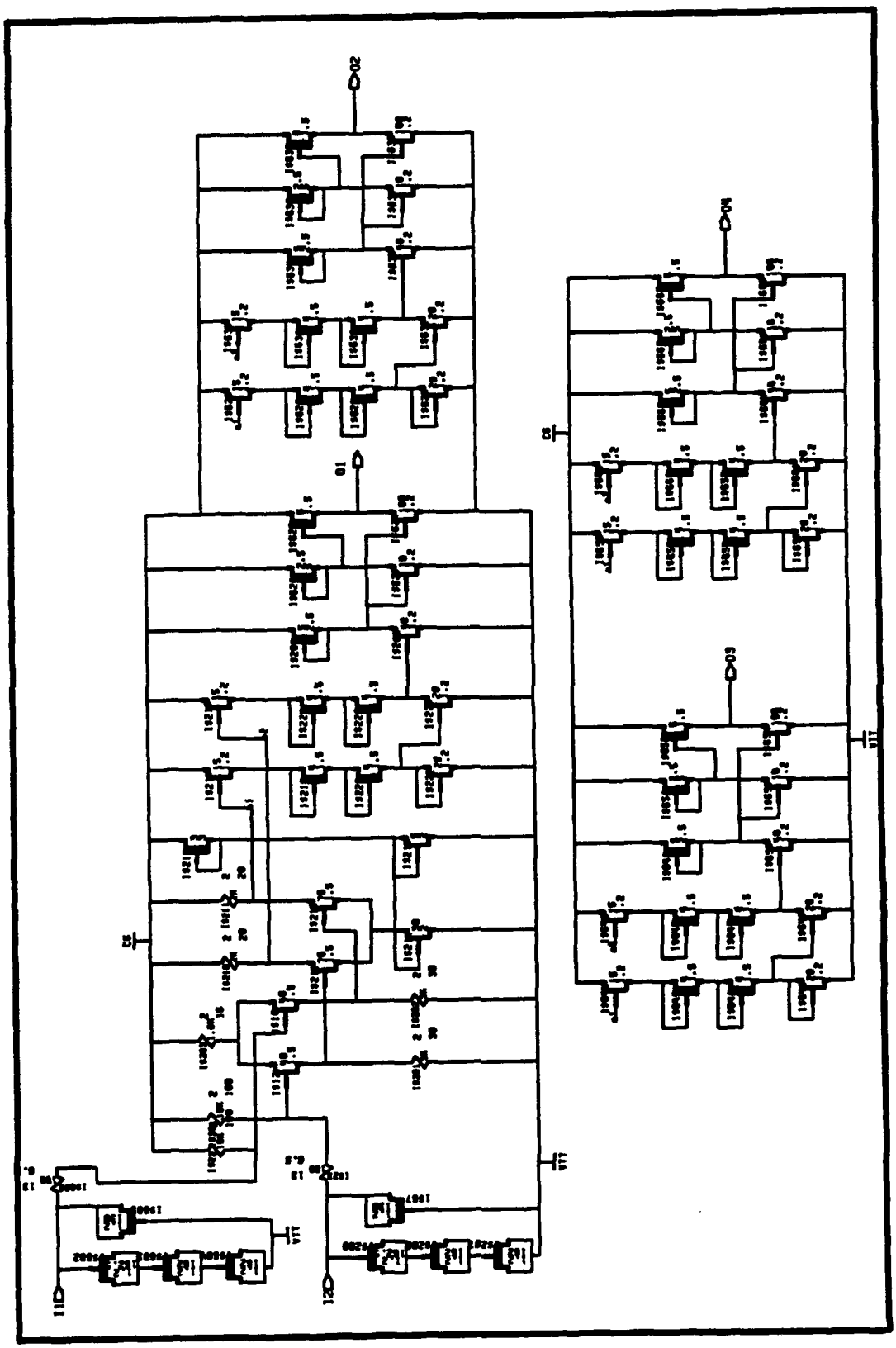

ALUMUX
UXX
in
SELLOGL
SELARDL
out

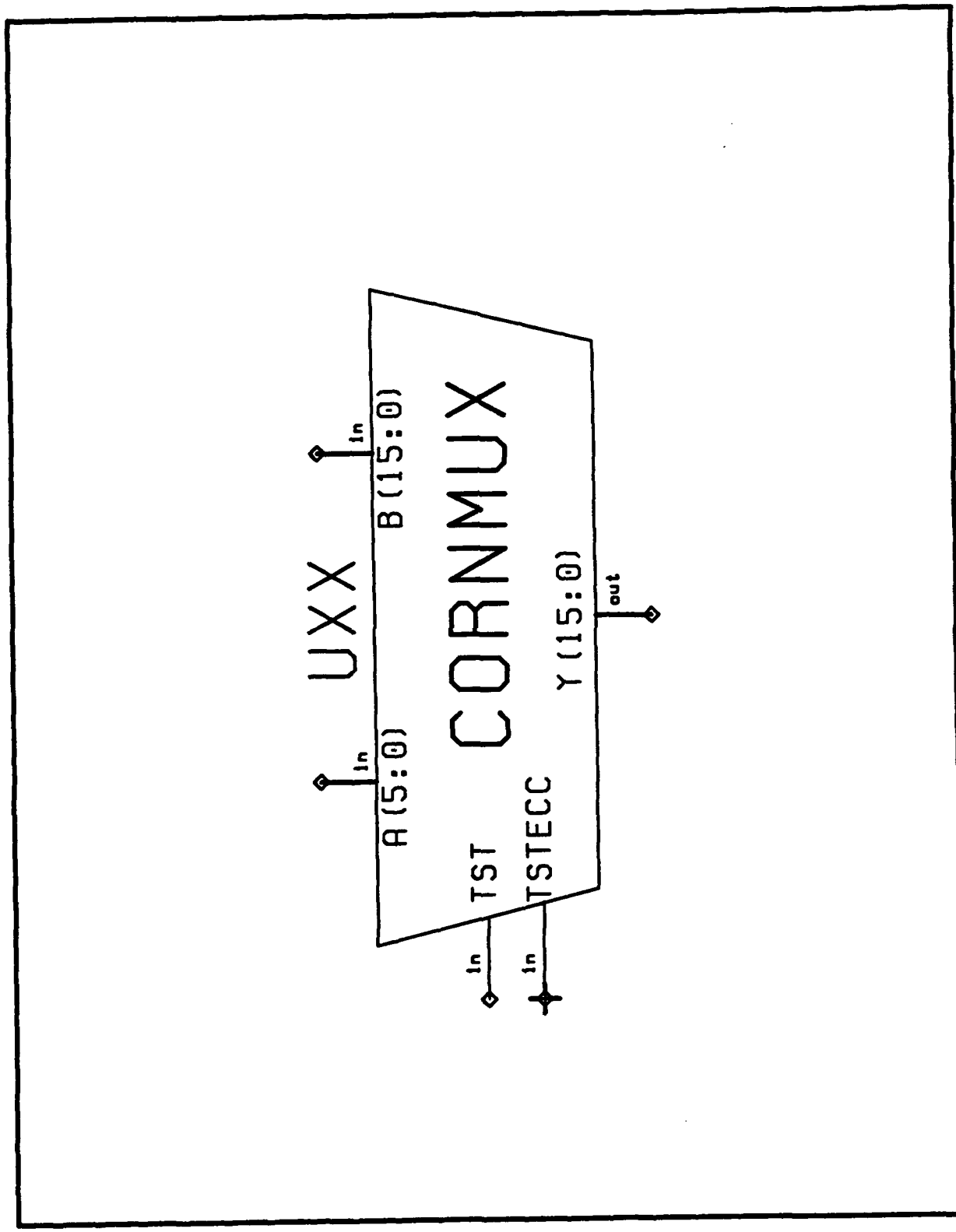

ALUMUX: 3 to 1 by 16
FOR I := 0 TO 15
ADD(I)
SELADDL
LOGIC(I)
SELLOGL
AND(I)
SELANDL
1:1 NOR
1:2 NOR
1:3 NOR
1:4 NOR
3 2.5
21 1.2
6 2.5
56 1.2
ALUOUT(I)

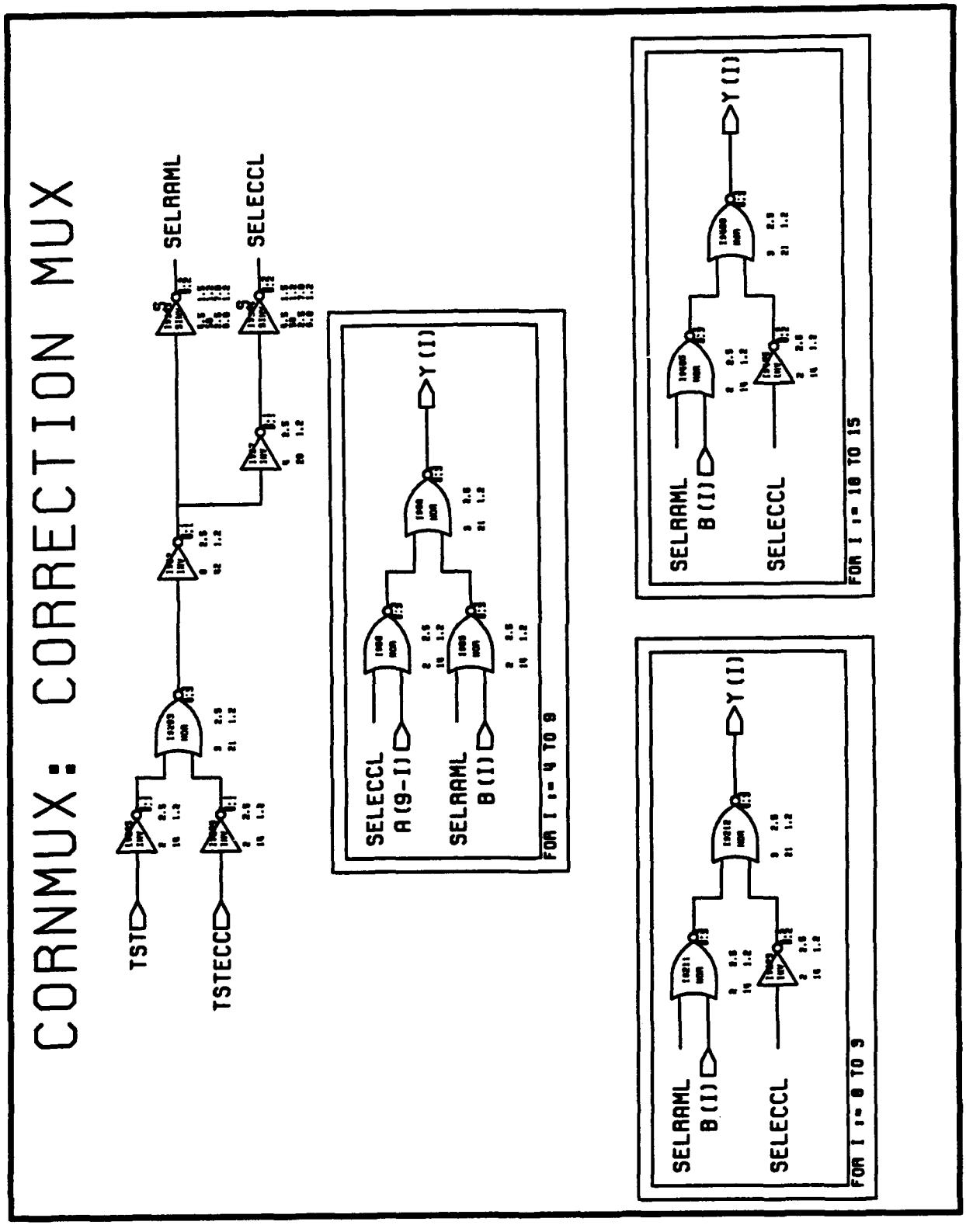

UXX
LCIN
CIN
CARRYMUX
COUTL
CS(1:0)

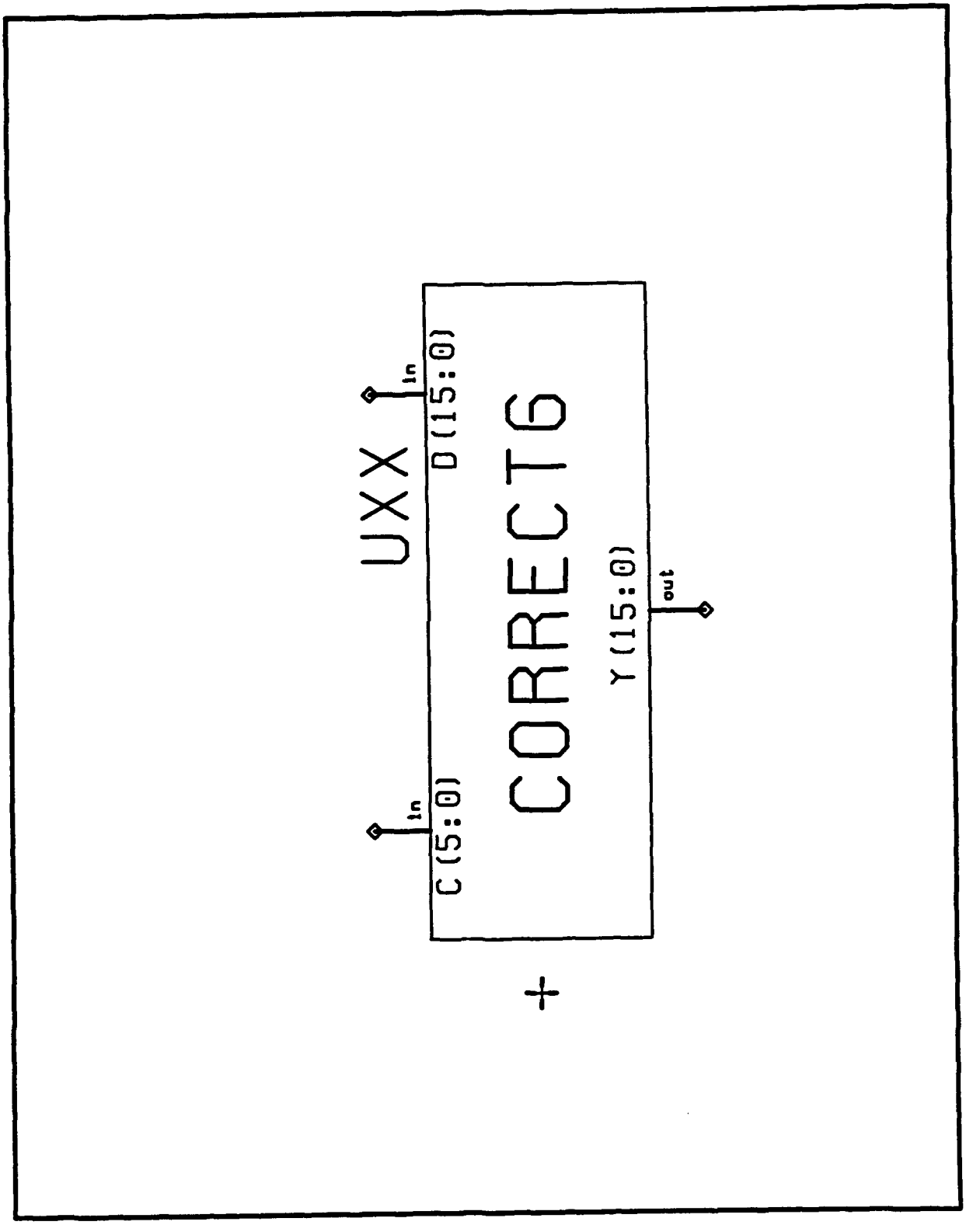

CARRYMUX
COUTL
CS(1)
CS(0)
CIN
LCIN

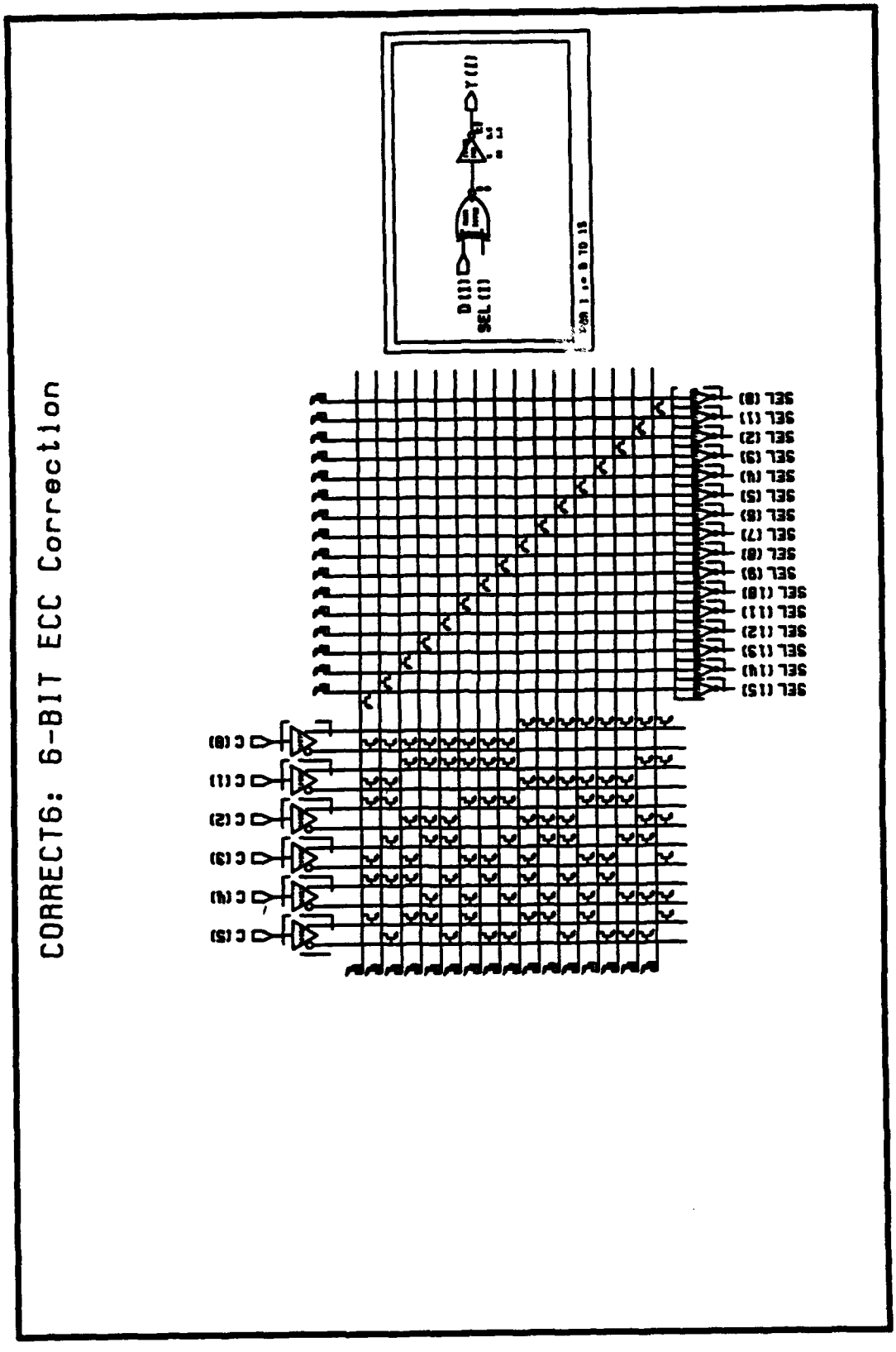

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: CLKRCVR
DESCRIPTION: DIFFERENTIAL INPUT CLOCK RECEIVER
0.5 0.3 SSS
0.5 0.3 SSS
0.5 0.3 SSS
0.5 0.3 SSS
CLKRCVR
O1
O2
O3
O4
OUT
I#
I1
I2
IN
IN
CLKRCVR
clkrcvr.bln

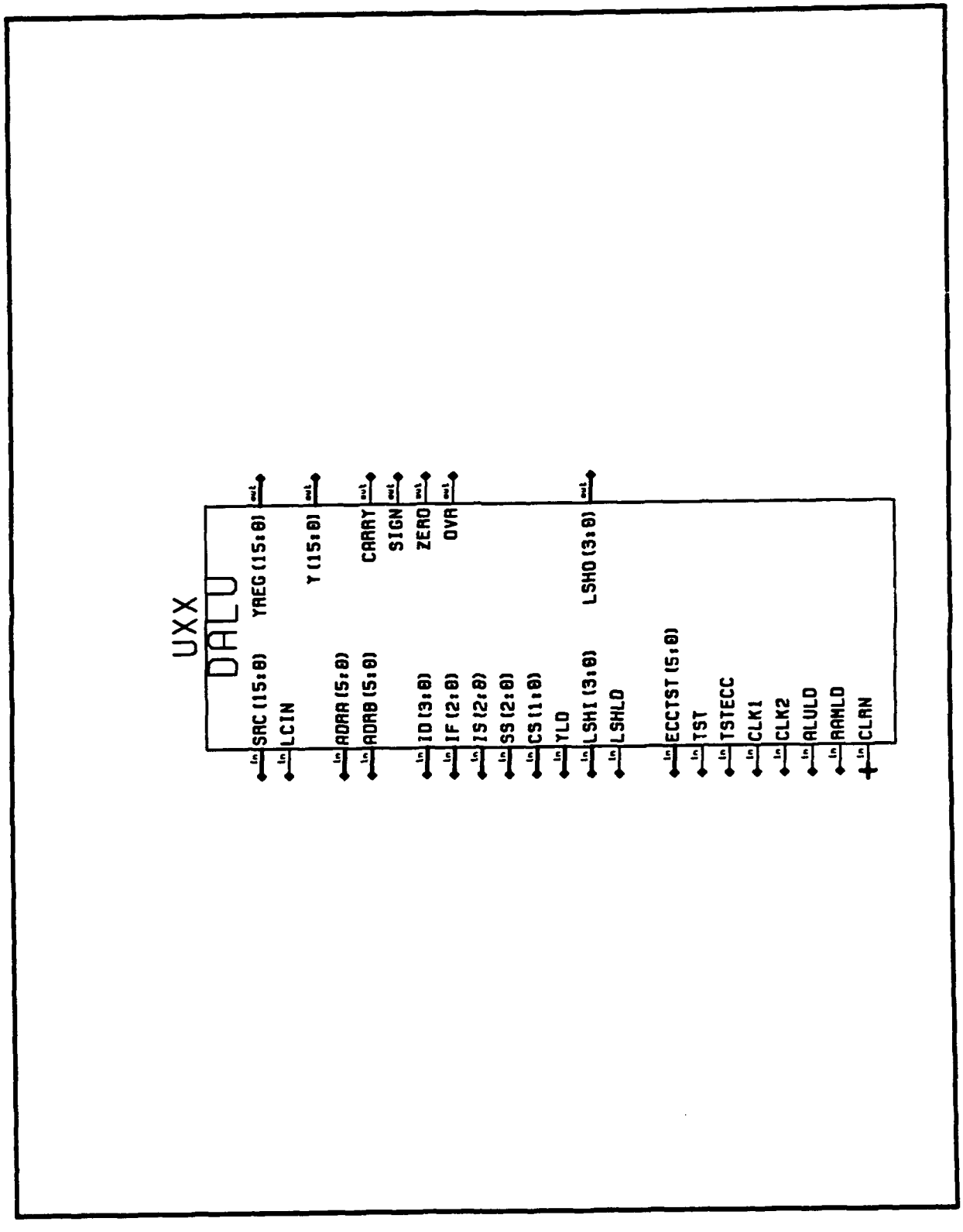


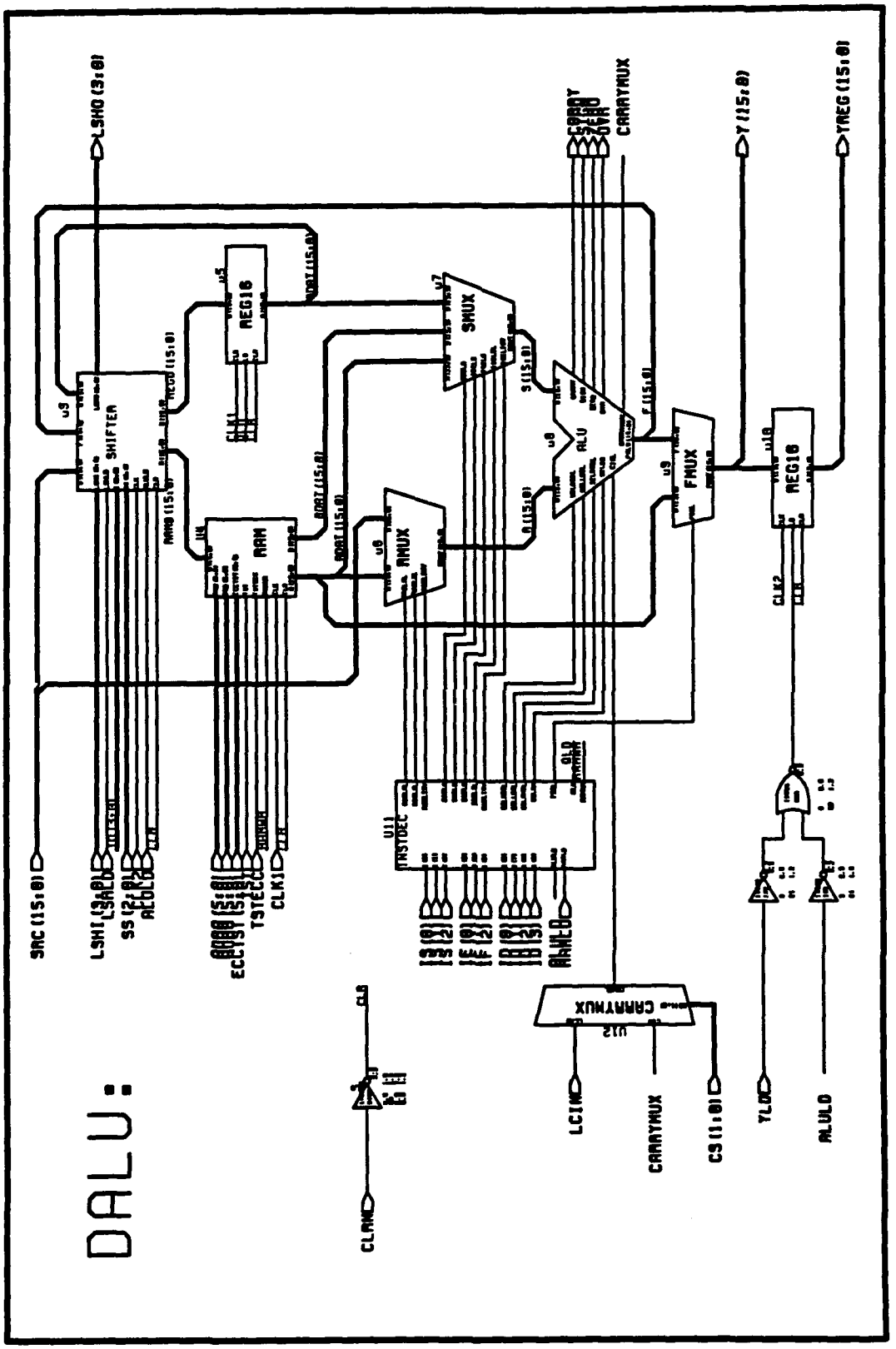

UXX
CORNMUX
in
B(15:0)
in
A(5:0)
TST
TSTECC
Y(15:0)
out
in
in

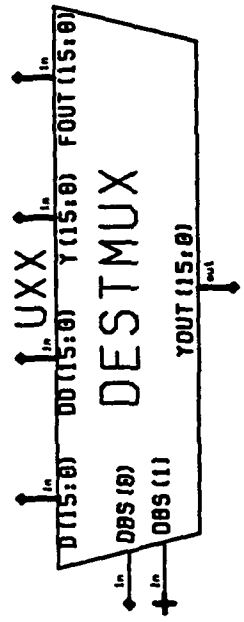

CORNMUX: CORRECTION MUX
SELRAML
SELECCL
TST
TSTECC
SELECCL
A(9-I)
SELRAML
B(I)
Y(I)
FOR I := 4 TO 9
SELRAML
B(I)
SELECCL
Y(I)
FOR I := 10 TO 15
SELRAML
B(I)
SELECCL
Y(I)
FOR I := 0 TO 3

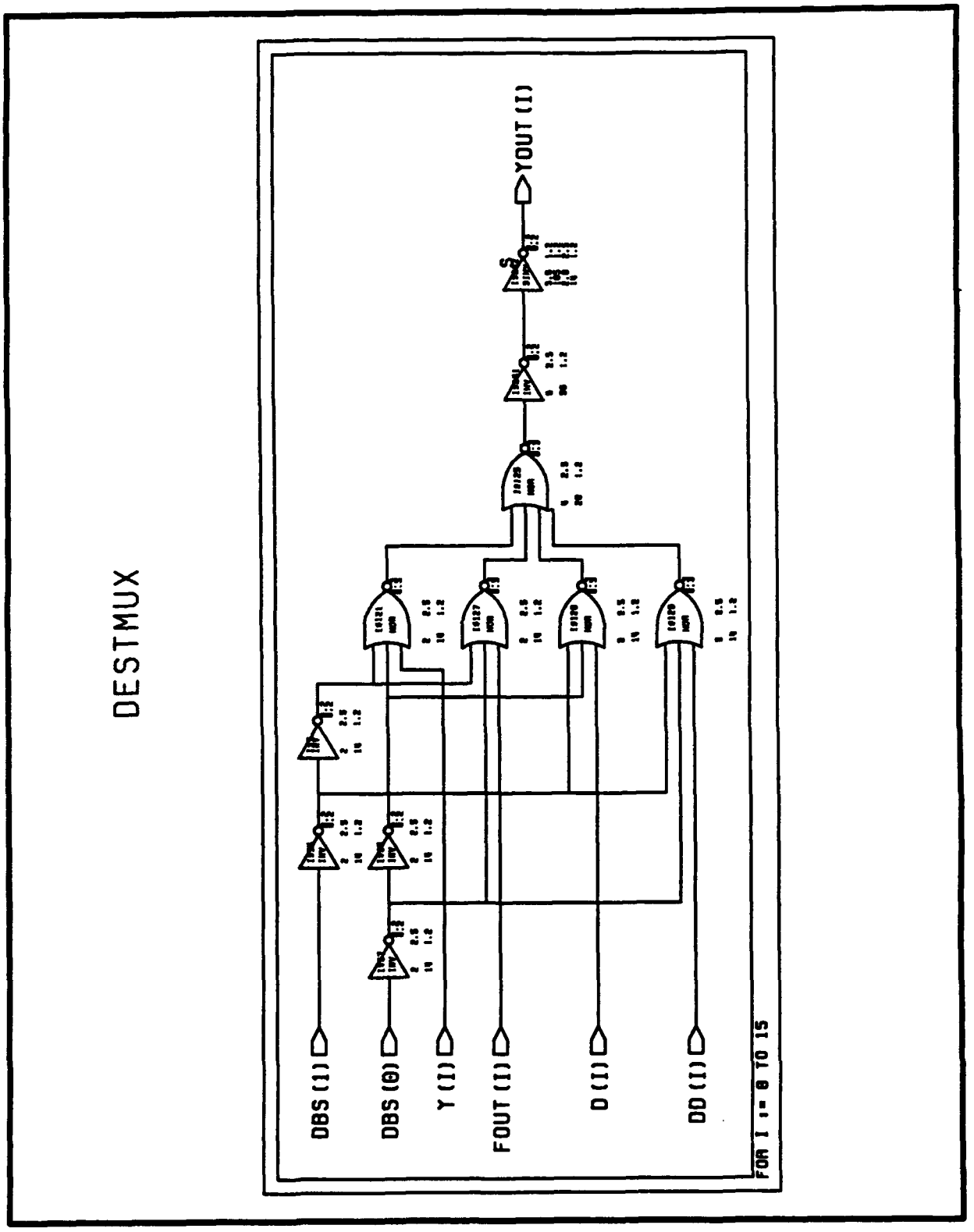

UXX
in
D(15:0)
CORRECT6
Y(15:0)
out
in
C(5:0)

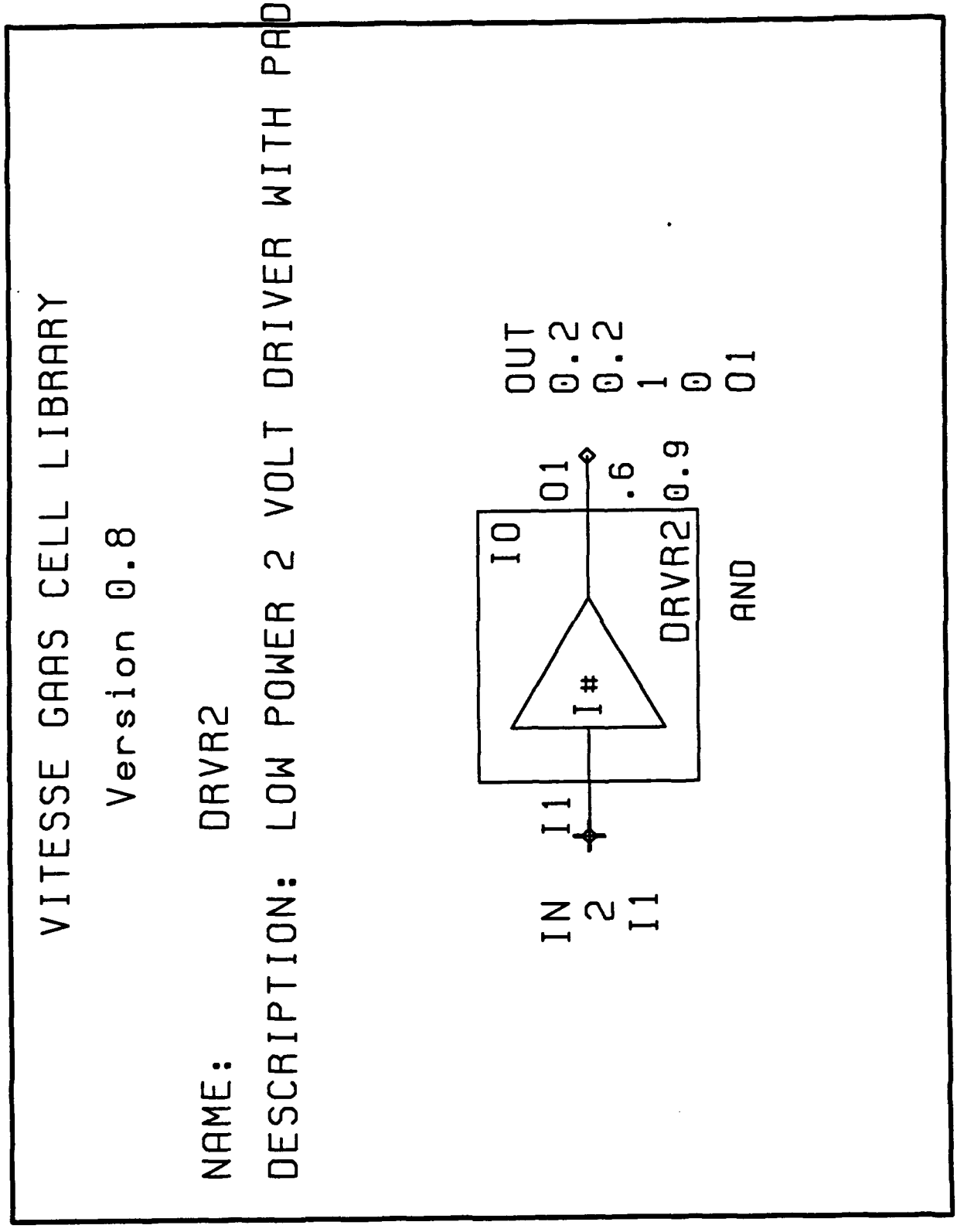

CORRECT6: 6-BIT ECC Correction

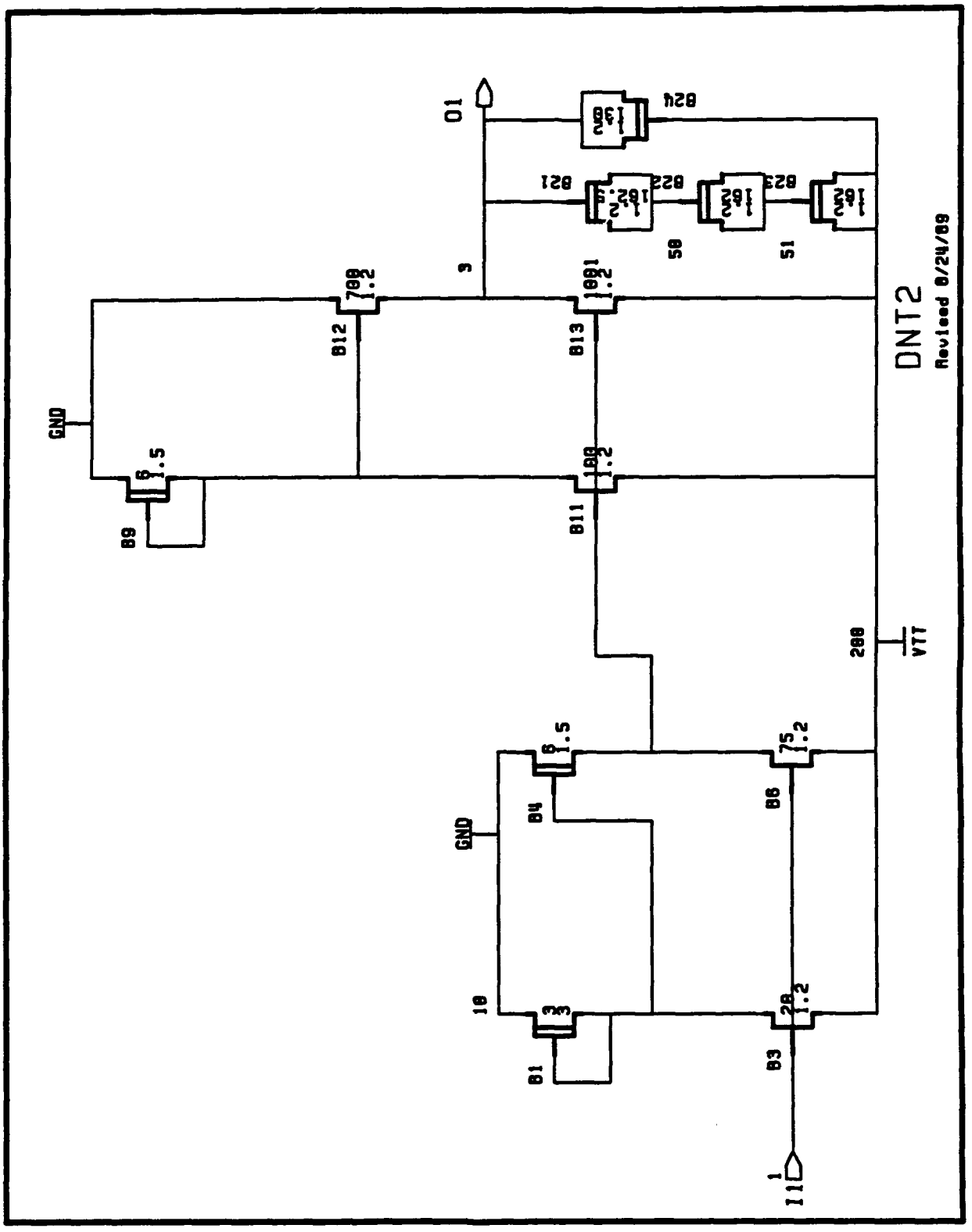

UXX
DALU
SRC (15:0)
LCIN
ADAA (5:0)
ADAB (5:0)
ID (3:0)
IF (2:0)
IS (2:0)
SS (2:0)
CS (1:0)
YLD
LSHI (3:0)
LSHLD
ECCTST (5:0)
TST
TSTECC
CLK1
CLK2
ALULD
RAMLD
CLAN
YREG (15:0)
Y (15:0)
CARRY
SIGN
ZERO
OVR
LSHO (3:0)

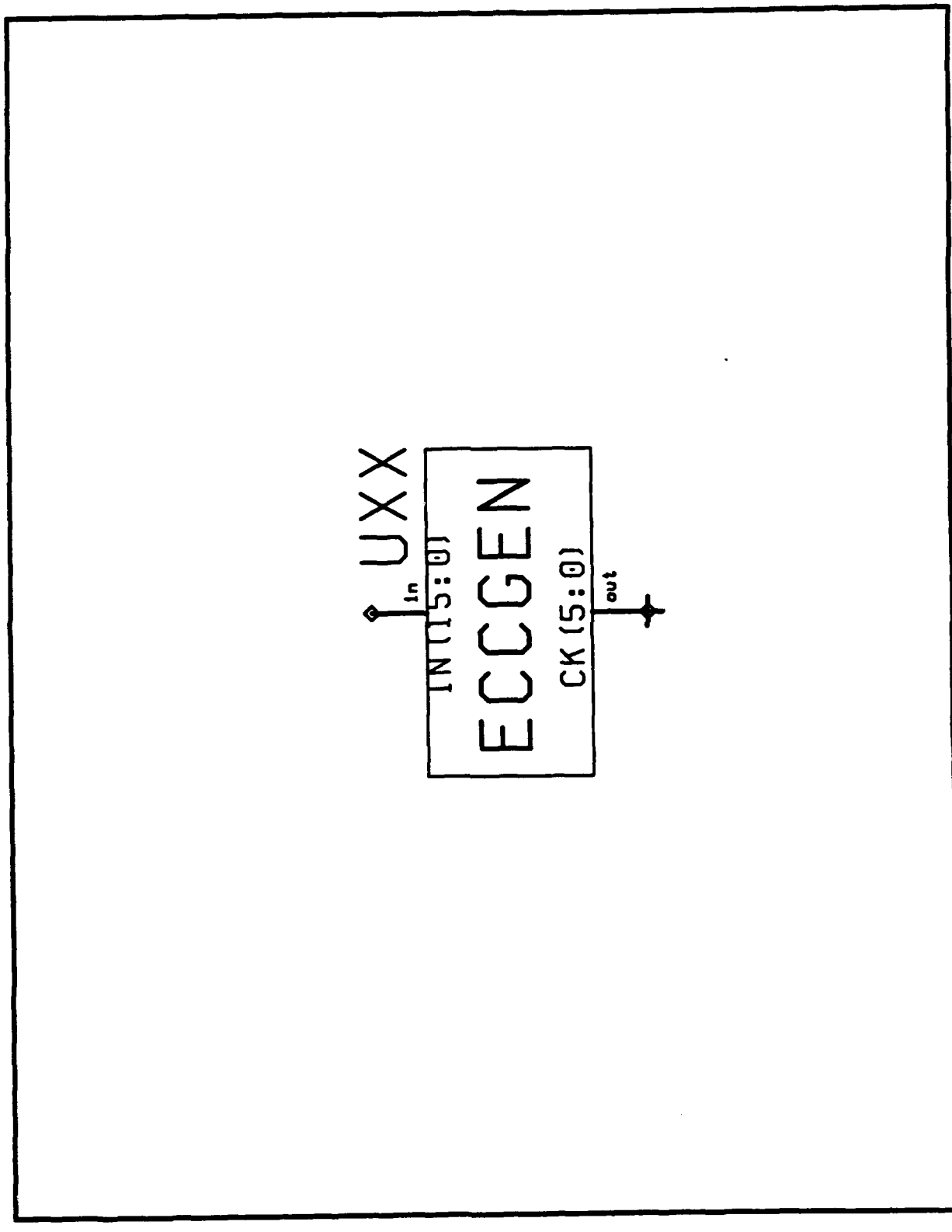

DALU:
LSHO(3:0)
CARRY
SIGN
OVFL
CARRYMUX
Y(15:0)
YREG(15:0)
REG16
SHIFTER
SMUX
ALU
FMUX
AMUX
RAM
MSTDEC
CARRYMUX
SRC(15:0)
CLK1
CLK2
CLKC
LCIN
CARRYMUX
CS(1:0)
YLOC
ALULO

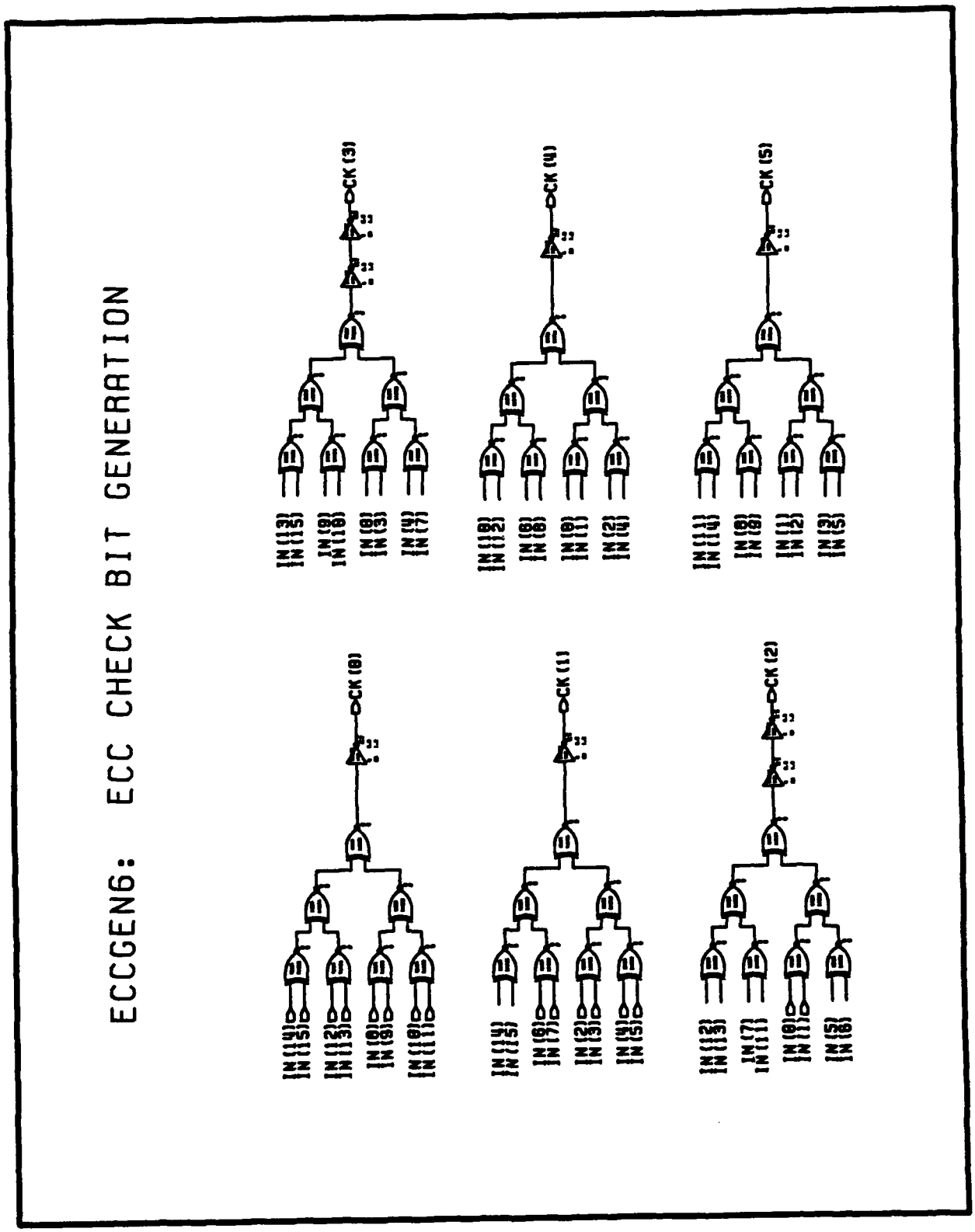

DESTMUX
UXX
D[15:0]
DO[15:0]
Y[15:0]
FOUT[15:0]
YOUT[15:0]
OBS(0)
OBS(1)

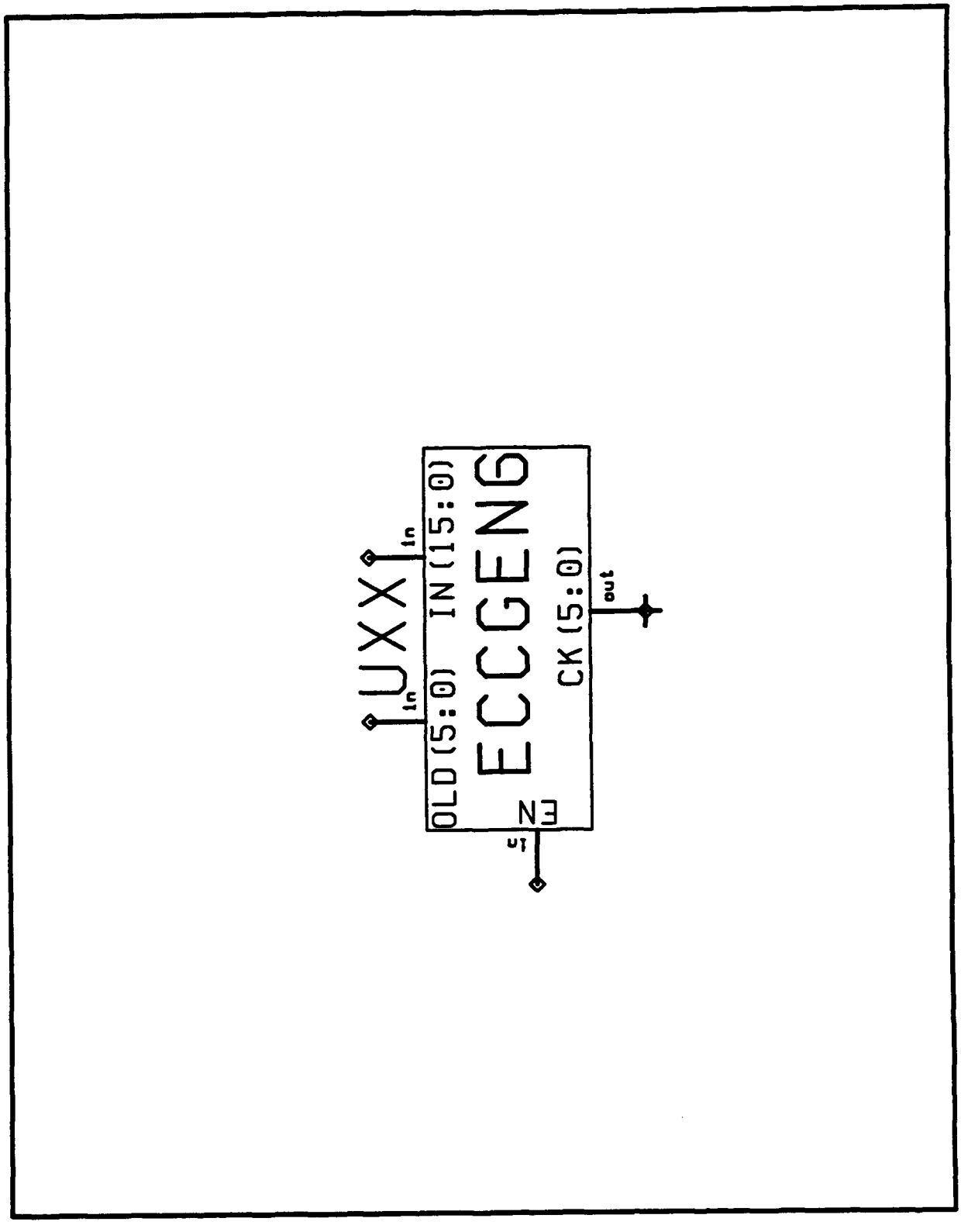

DESTMUX
YOUT (I)
DBS (1)
DBS (0)
Y (I)
FOUT (I)
D (I)
DD (I)
FOR I := 0 TO 15

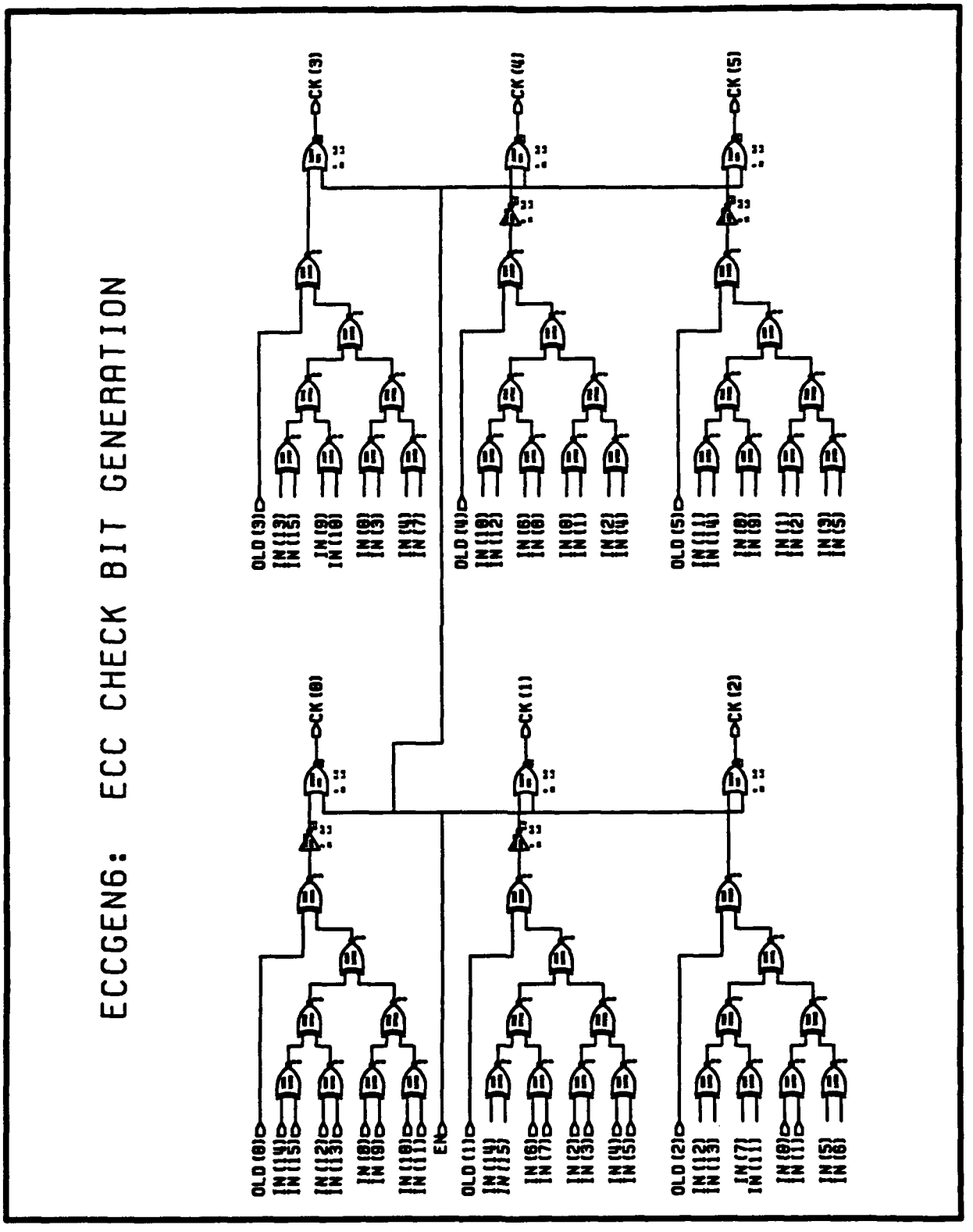

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: DRVR2
DESCRIPTION: LOW POWER 2 VOLT DRIVER WITH PAD
IN 2 I1
I1
IO
I#
O1
.6
DRVR2 0.9
OUT 0.2 0.2 1 0 O1
AND

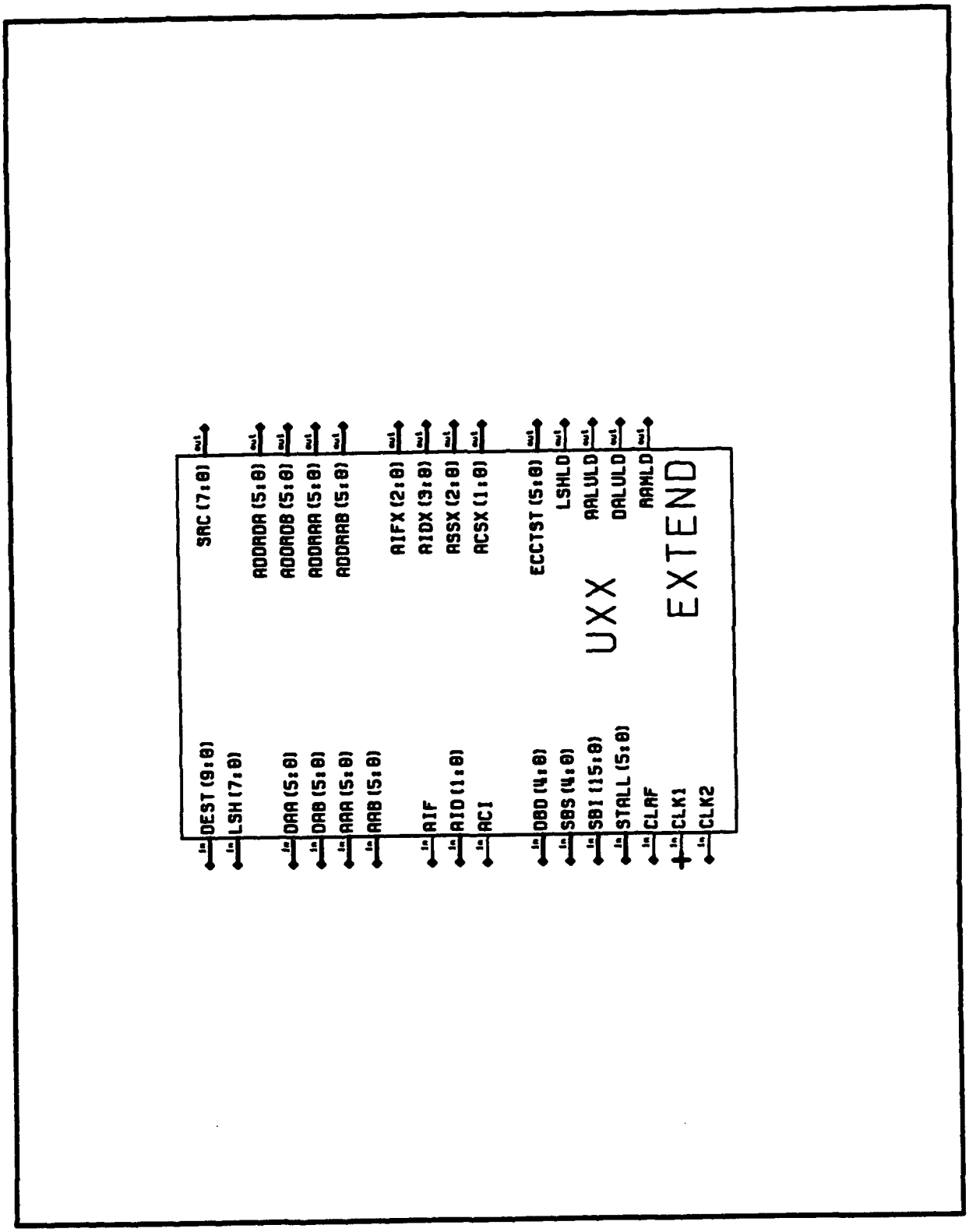

DNT2
Revised 8/24/89
GND
VTT
B9
B11
B12
B13
B4
B6
B1
B3
B21
B22
B23
B24
50
51
10
11

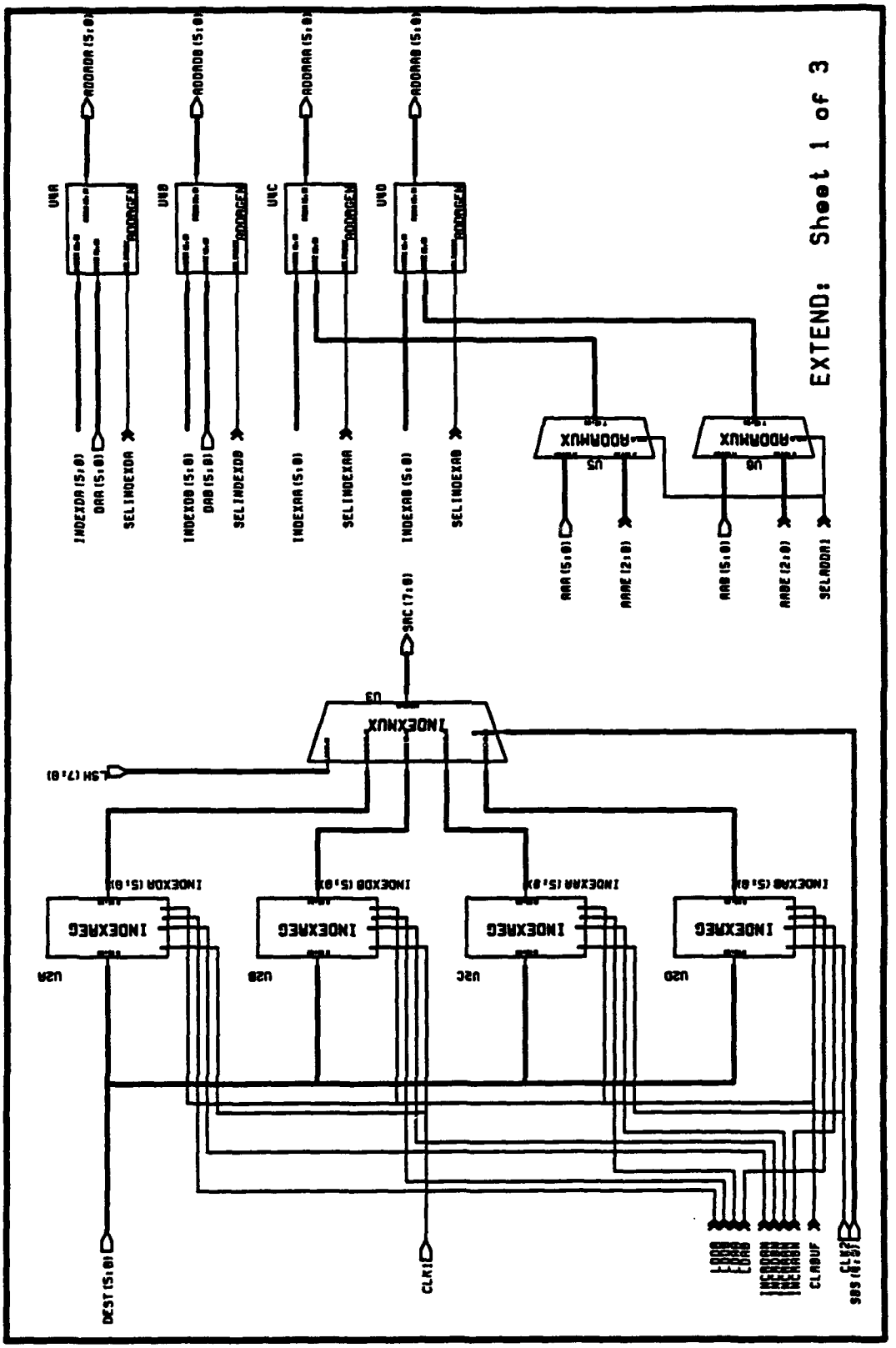

UXX
In
INT(5:0)
ECCGEN
CK(5:0)
out

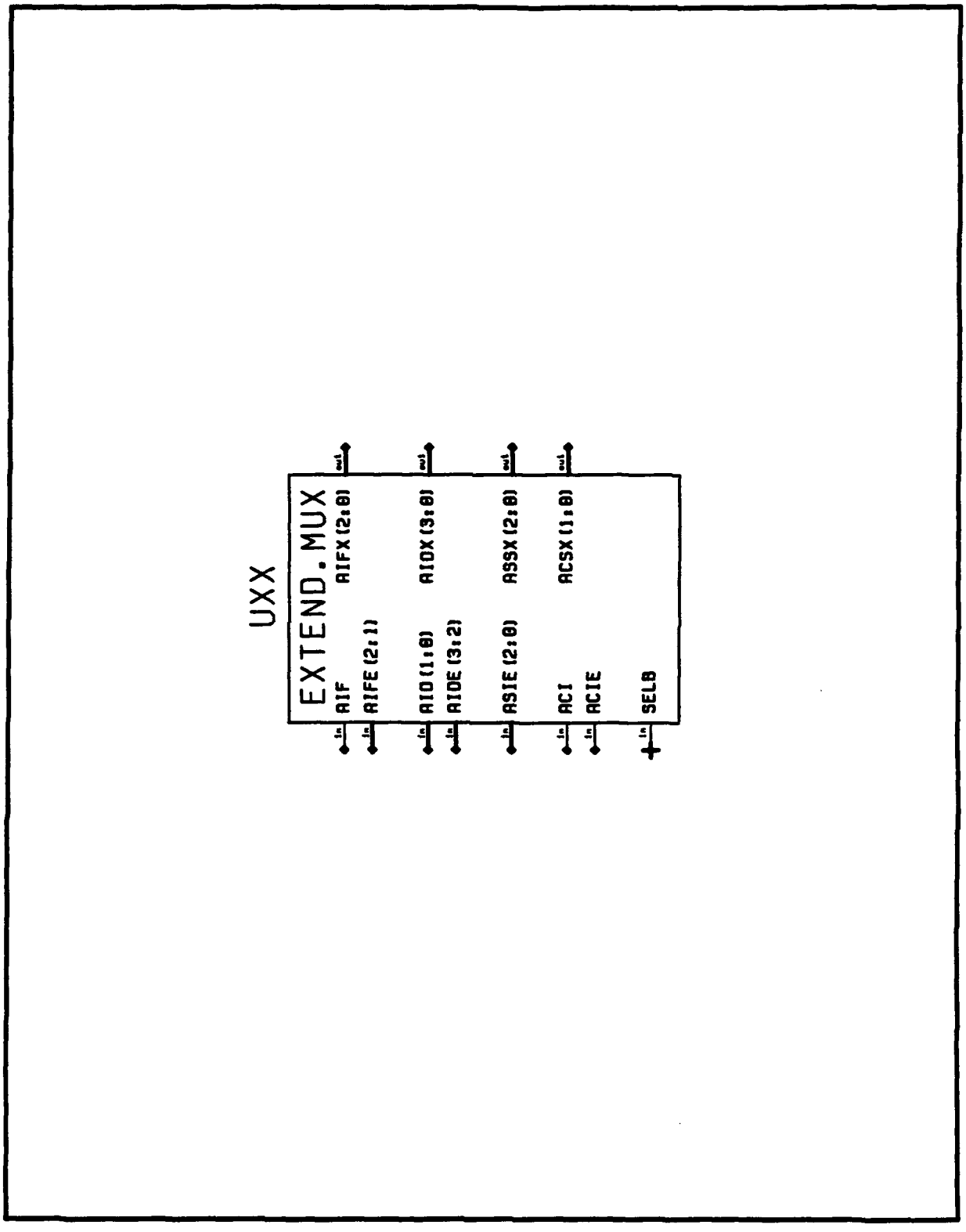

ECCGEN6: ECC CHECK BIT GENERATION
CK(3)
CK(4)
CK(5)
CK(0)
CK(1)
CK(2)

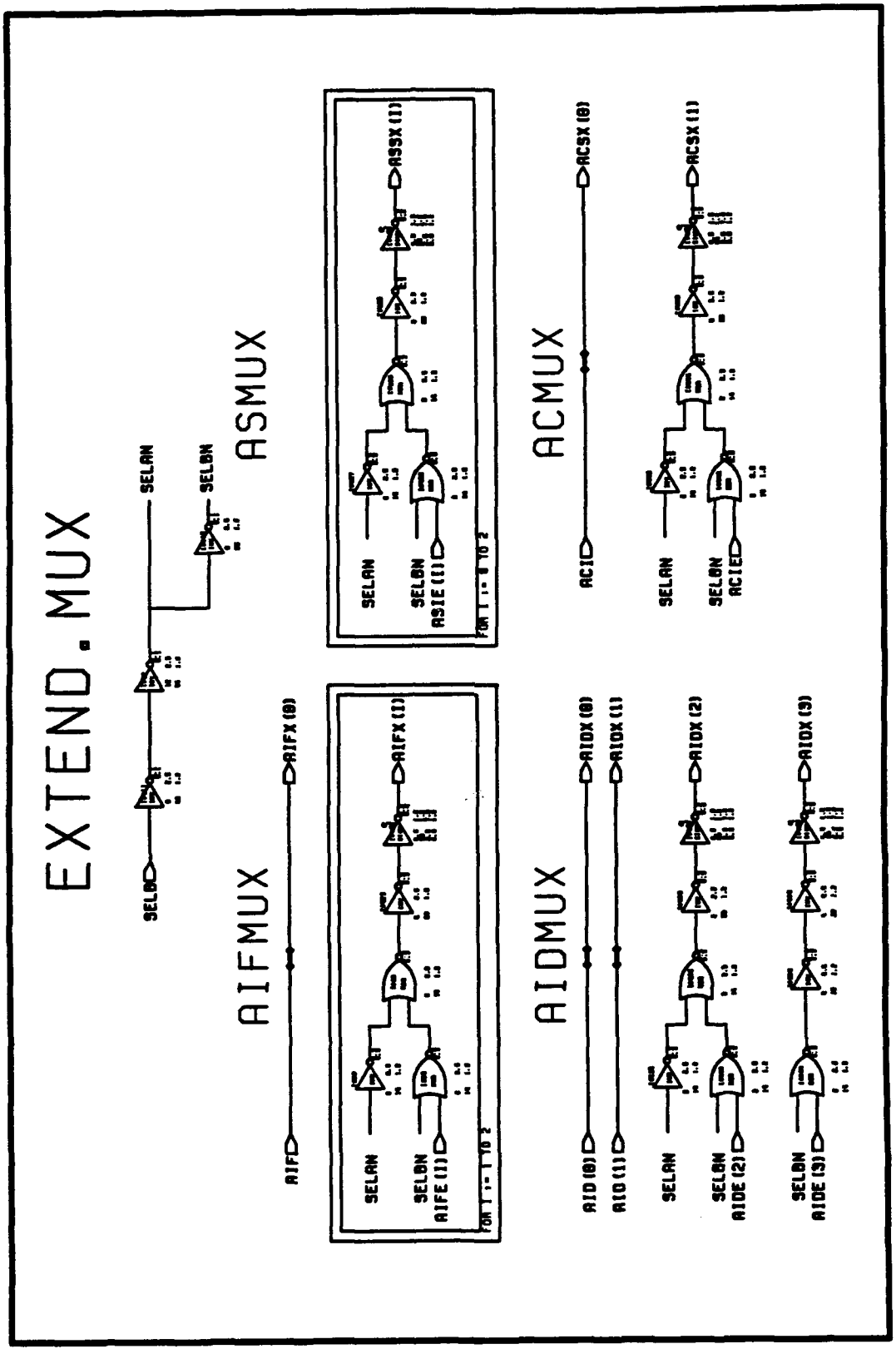

UXX1
In
In
OLD(5:0)
IN(15:0)
ECCGEN6
EN
CK(5:0)
out
In

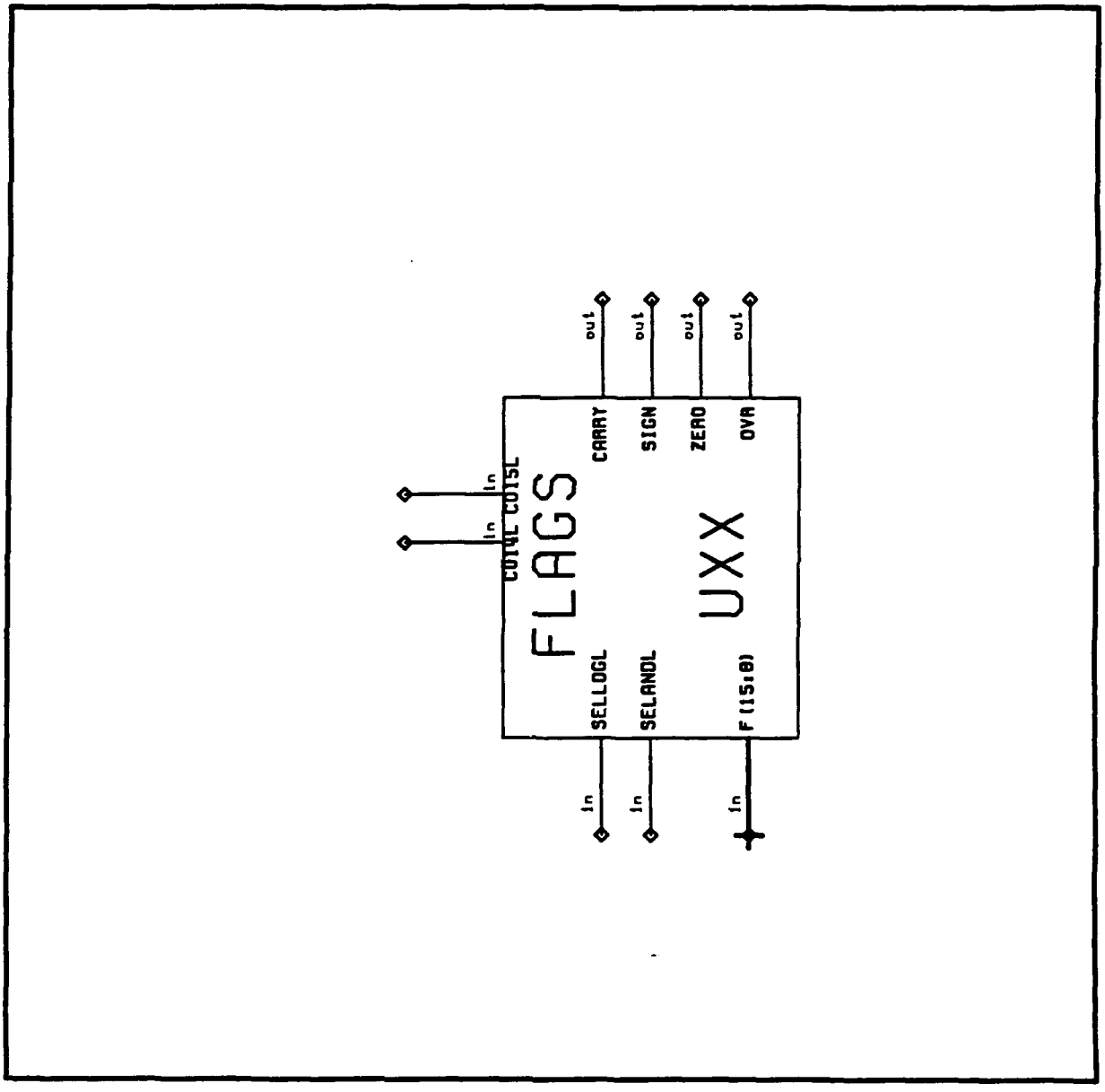

ECCGEN6: ECC CHECK BIT GENERATION
CK (3)
CK (4)
CK (5)
CK (0)
CK (1)
CK (2)
OLD (3)
OLD (4)
OLD (5)
OLD (0)
OLD (1)
OLD (2)
EN

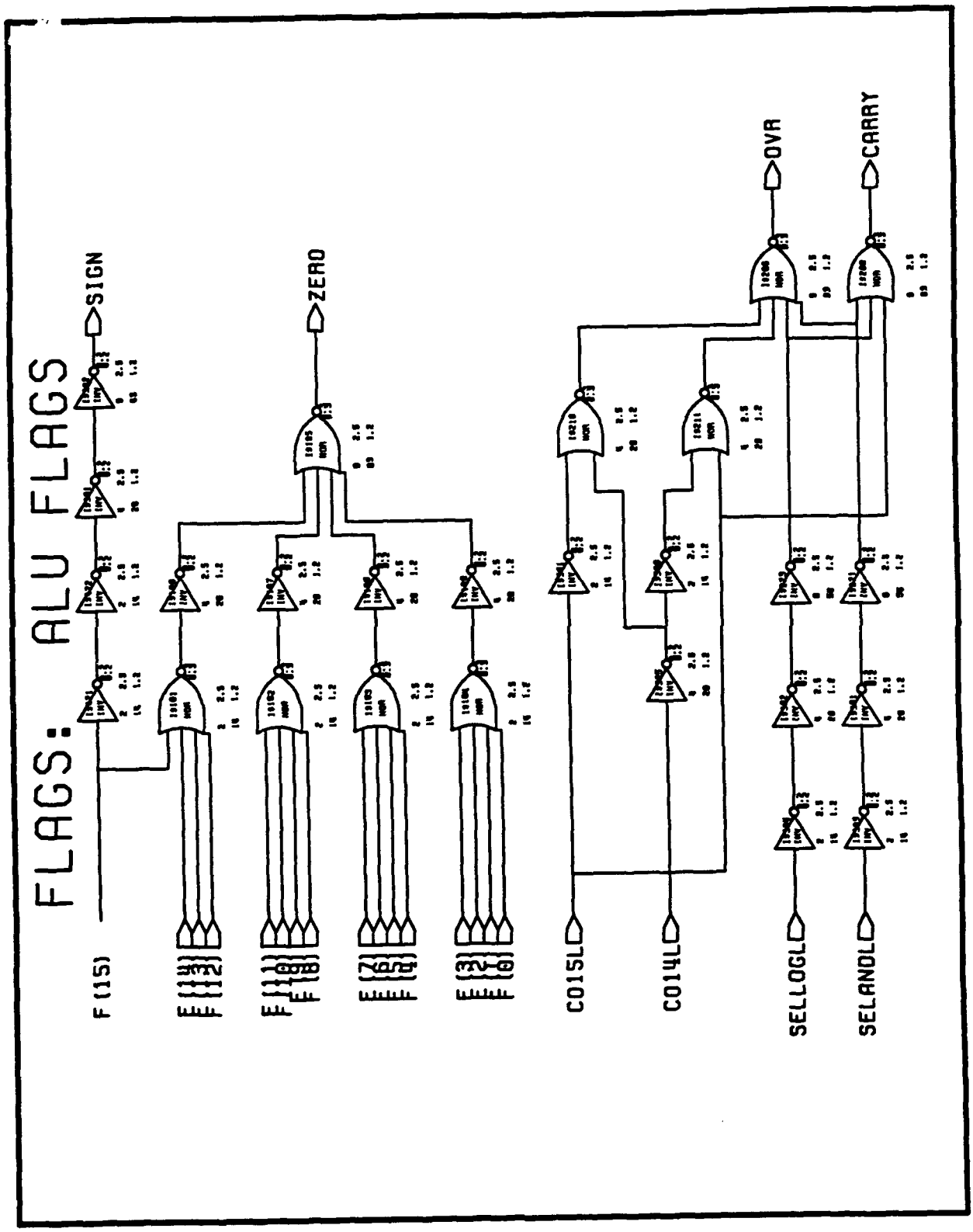

SRC (7:0)
ADDRDA (5:0)
ADDRDB (5:0)
ADDRAA (5:0)
ADDRAB (5:0)
AIFX (2:0)
AIDX (3:0)
ASSX (2:0)
ACSX (1:0)
ECCTST (5:0)
LSHLD
AALULD
DALULD
AAHLD
DEST (9:0)
LSH (7:0)
DAA (5:0)
DAB (5:0)
AAA (5:0)
AAB (5:0)
AIF
AID (1:0)
AC1
DBD (4:0)
SBS (4:0)
SBI (15:0)
STALL (5:0)
CLAF
CLK1
CLK2
UXX
EXTEND

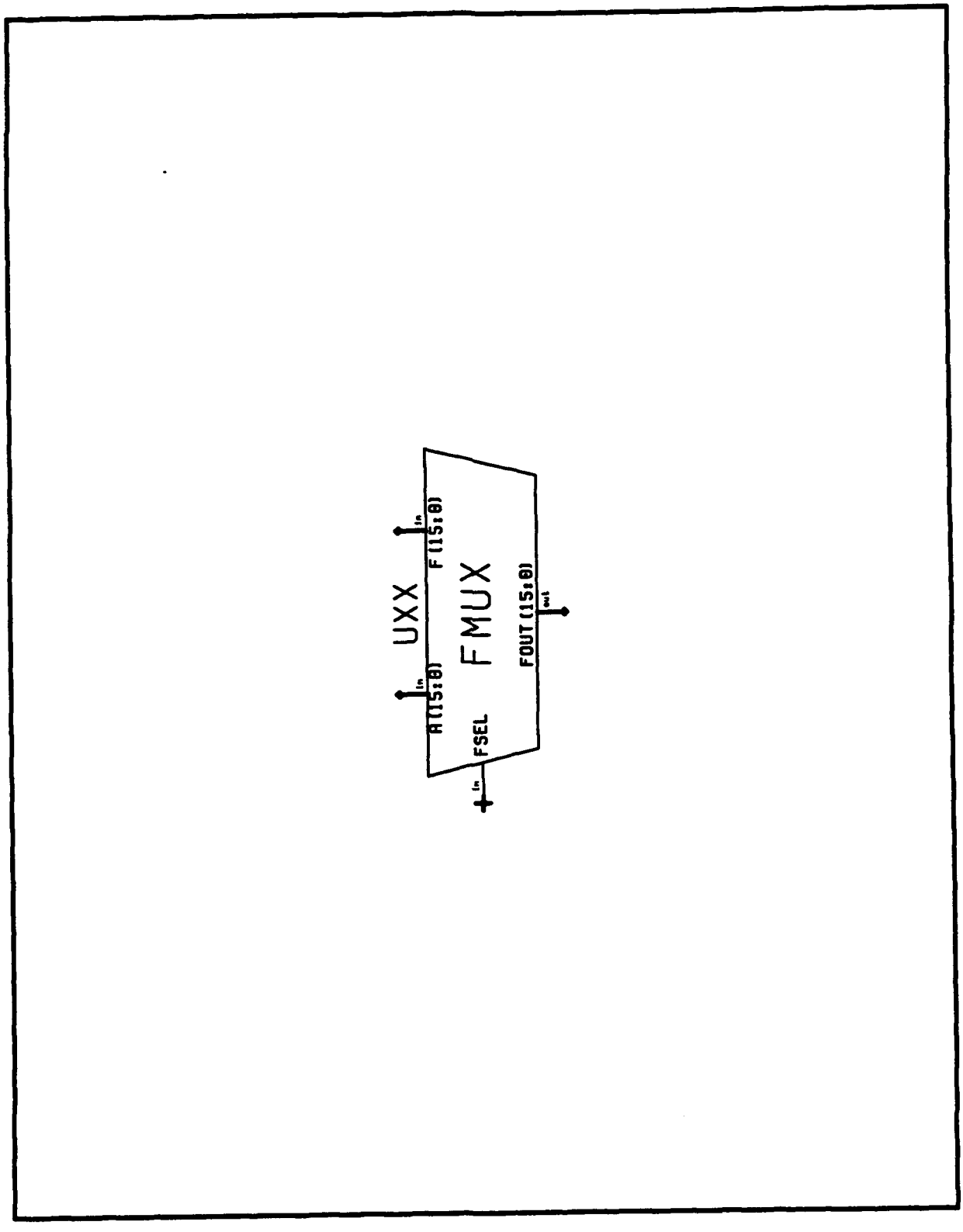

EXTEND: Sheet 1 of 3
U8A
U8B
U8C
U8D
ADDRDR (5:0)
ADDRDB (5:0)
ADDRAR (5:0)
ADDRAB (5:0)
INDEXDR (5:0)
DAR (5:0)
SELINDEXDA
INDEXDB (5:0)
DAB (5:0)
SELINDEXDB
INDEXAR (5:0)
SELINDEXAA
INDEXAB (5:0)
SELINDEXAB
ADDRGEN
ADDRMUX
U5
U6
AAR (5:0)
AARE (2:0)
AAB (5:0)
AABE (2:0)
SELADDR1
SRC (7:0)
U9
INDEXMUX
SH (7:0)
INDEXAR (5:0)
INDEXAB (5:0)
INDEXREG
U2A
U2B
U2C
U2D
DEST (5:0)
CLK1
CLKBUF

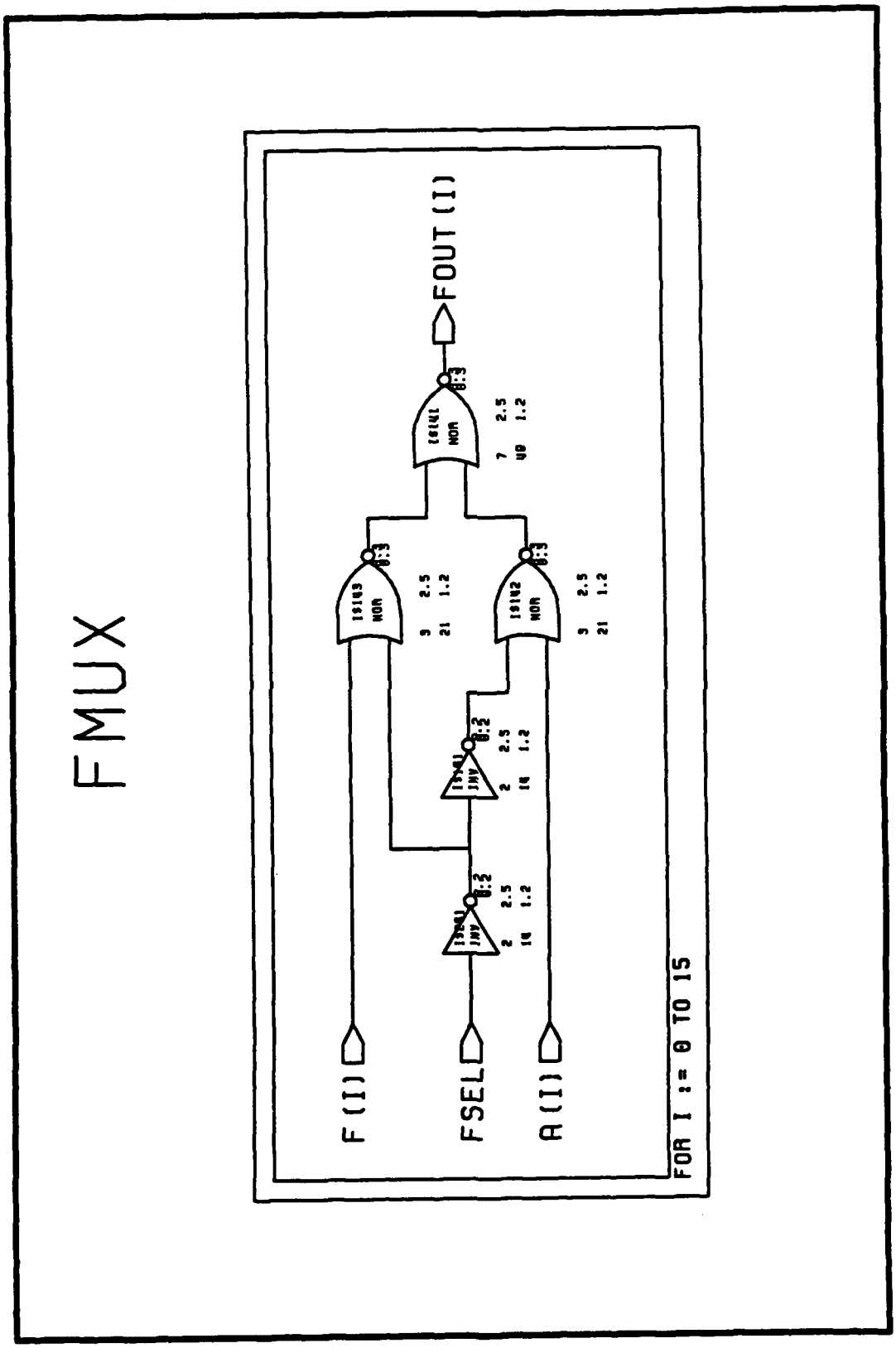

UXX
EXTEND.MUX
AIF
AIFE(2:1)
AIO(1:0)
AIDE(3:2)
ASIE(2:0)
ACI
ACIE
SELB
AIFX(2:0)
AIOX(3:0)
ASSX(2:0)
ACSX(1:0)

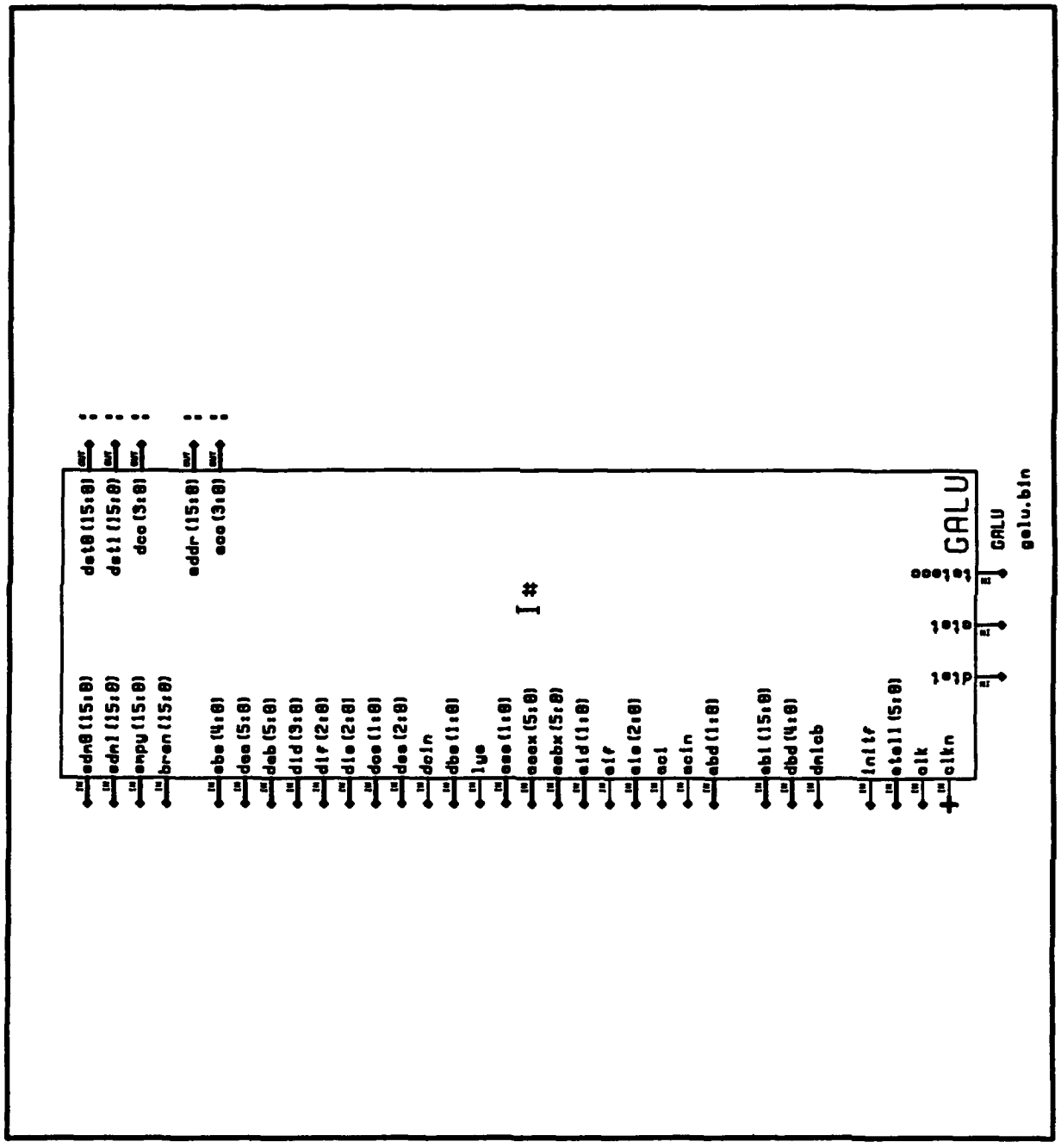

EXTEND.MUX
SELAN
SELBN
SELBO
ASMUX
ASSX(1)
SELAN
SELBN
ASIE(1)
ACMUX
ACSX(0)
ACI
ACSX(1)
SELAN
SELBN
ACIE
AIFMUX
AIFX(0)
AIF
AIFX(1)
SELAN
SELBN
AIFE(1)
AIDMUX
AIDX(0)
AID(0)
AIDX(1)
AID(1)
AIDX(2)
SELAN
SELBN
AIDE(2)
AIDX(3)
SELAN
SELBN
AIDE(3)

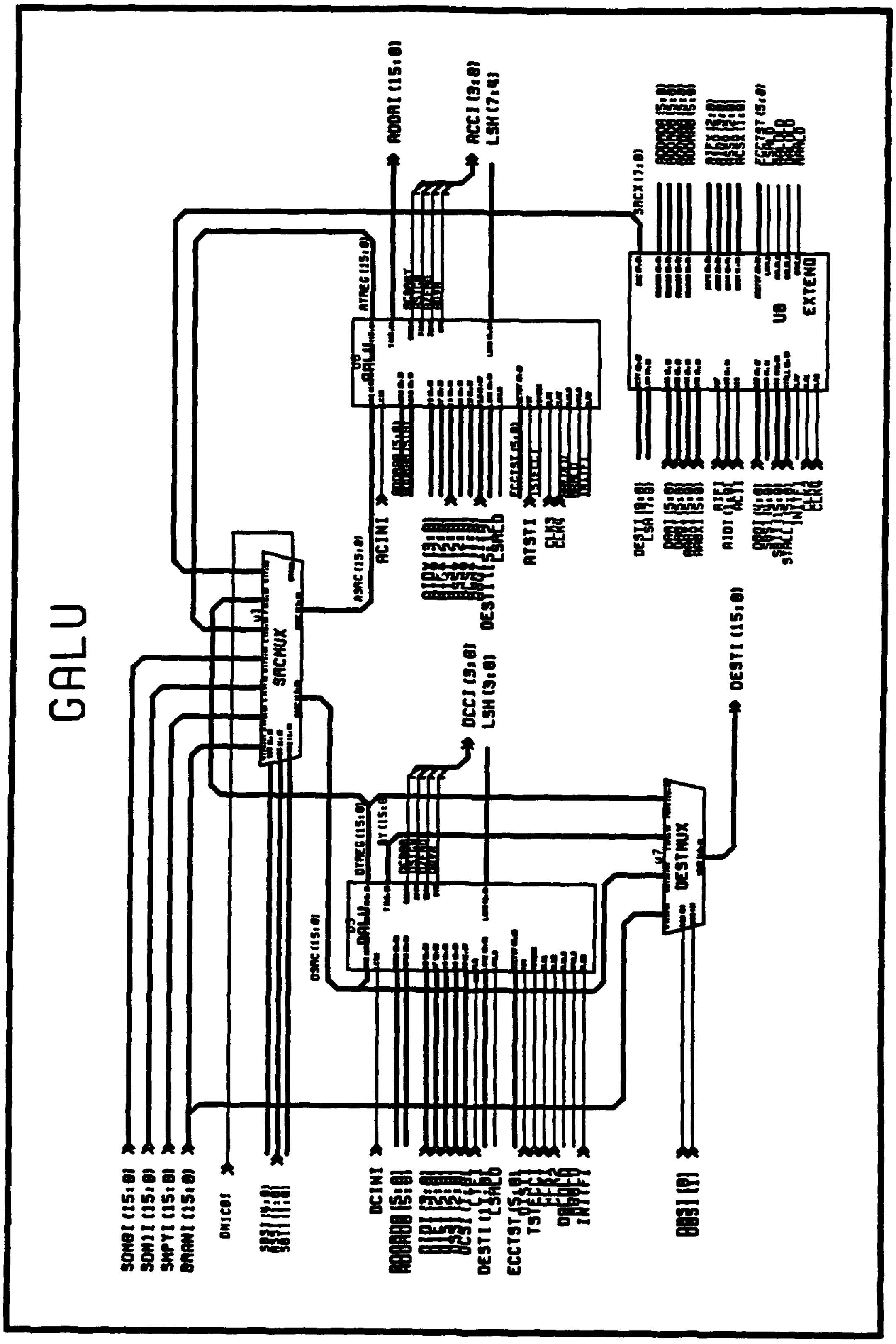

out
out
out
out
CARRY
SIGN
ZERO
OVR
in
in
COUT COUTL
FLAGS
UXX
SELLOGL
SELANDL
F(15:0)
in
in
in

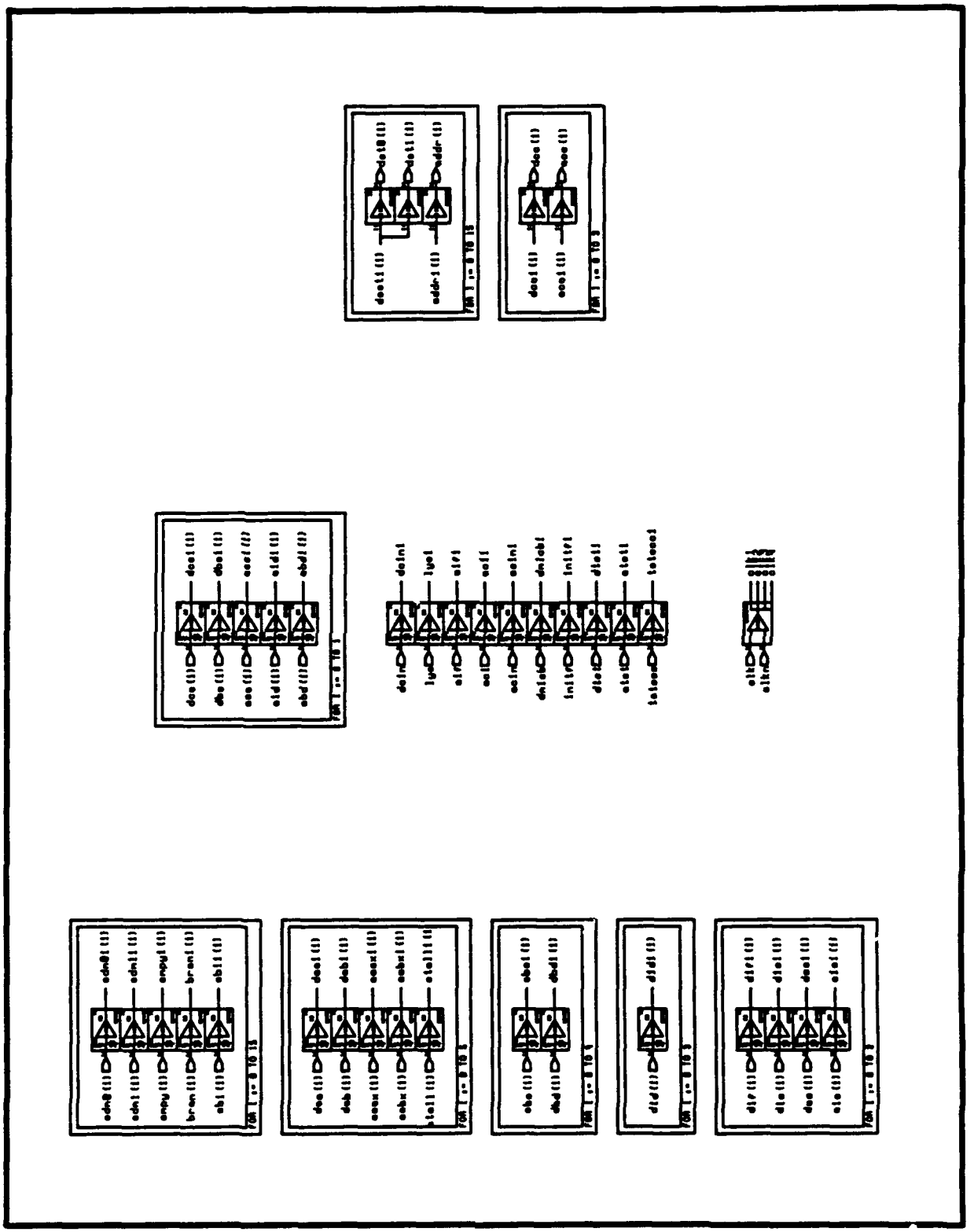

FLAGS: ALU FLAGS
SIGN
ZERO
OVR
CARRY
F(15)
F(14:12)
F(11:8)
F(7:4)
F(3:0)
C015L
C014L
SELLOGL
SELANDL

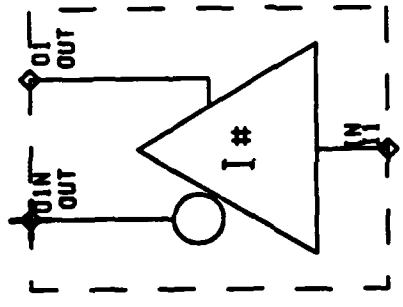

UXX
FMUX
F(15:0)
A(15:0)
FSEL
FOUT(15:0)
in
out

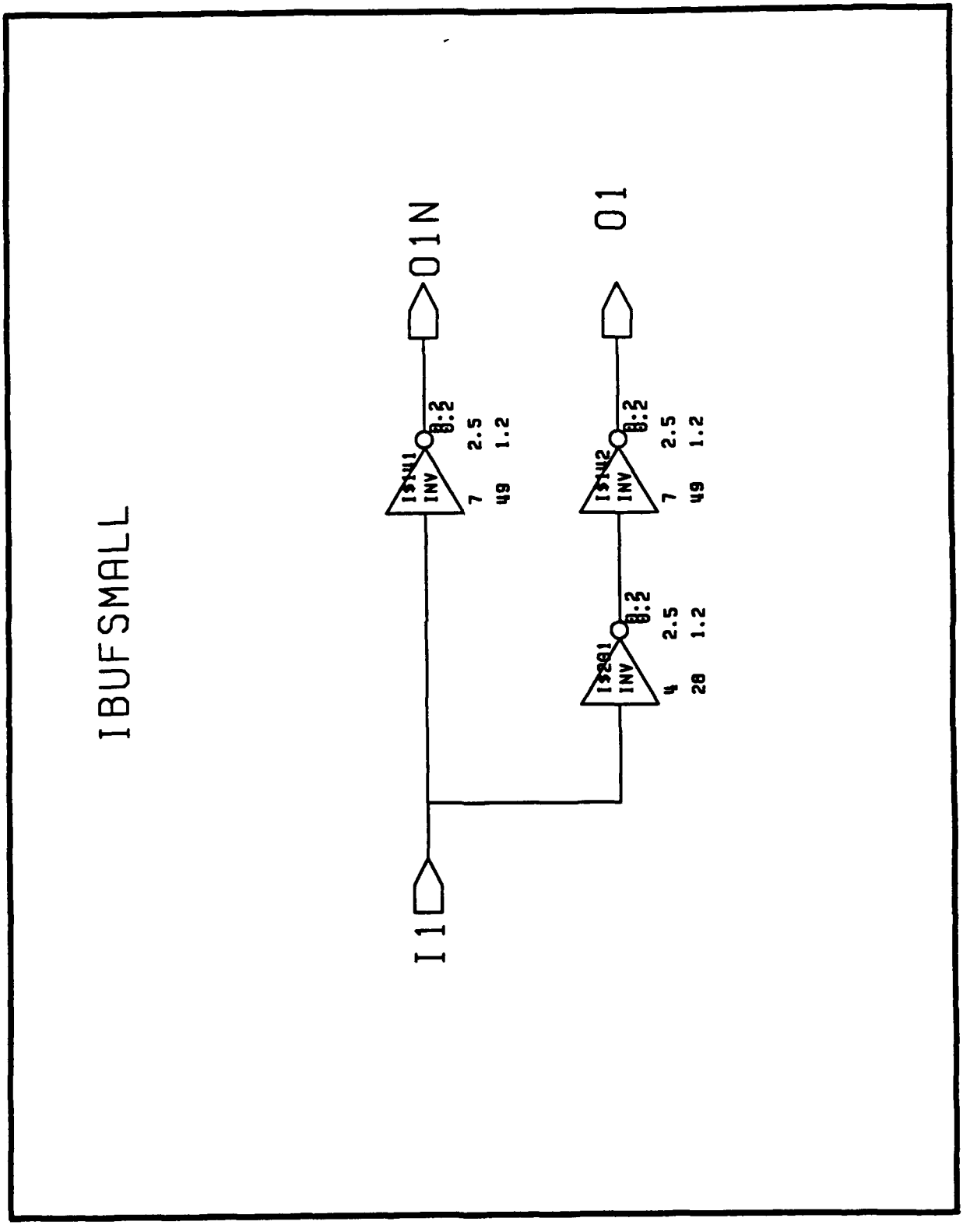

FMUX
FOUT(I)
F(I)
FSEL
A(I)
FOR I := 0 TO 15

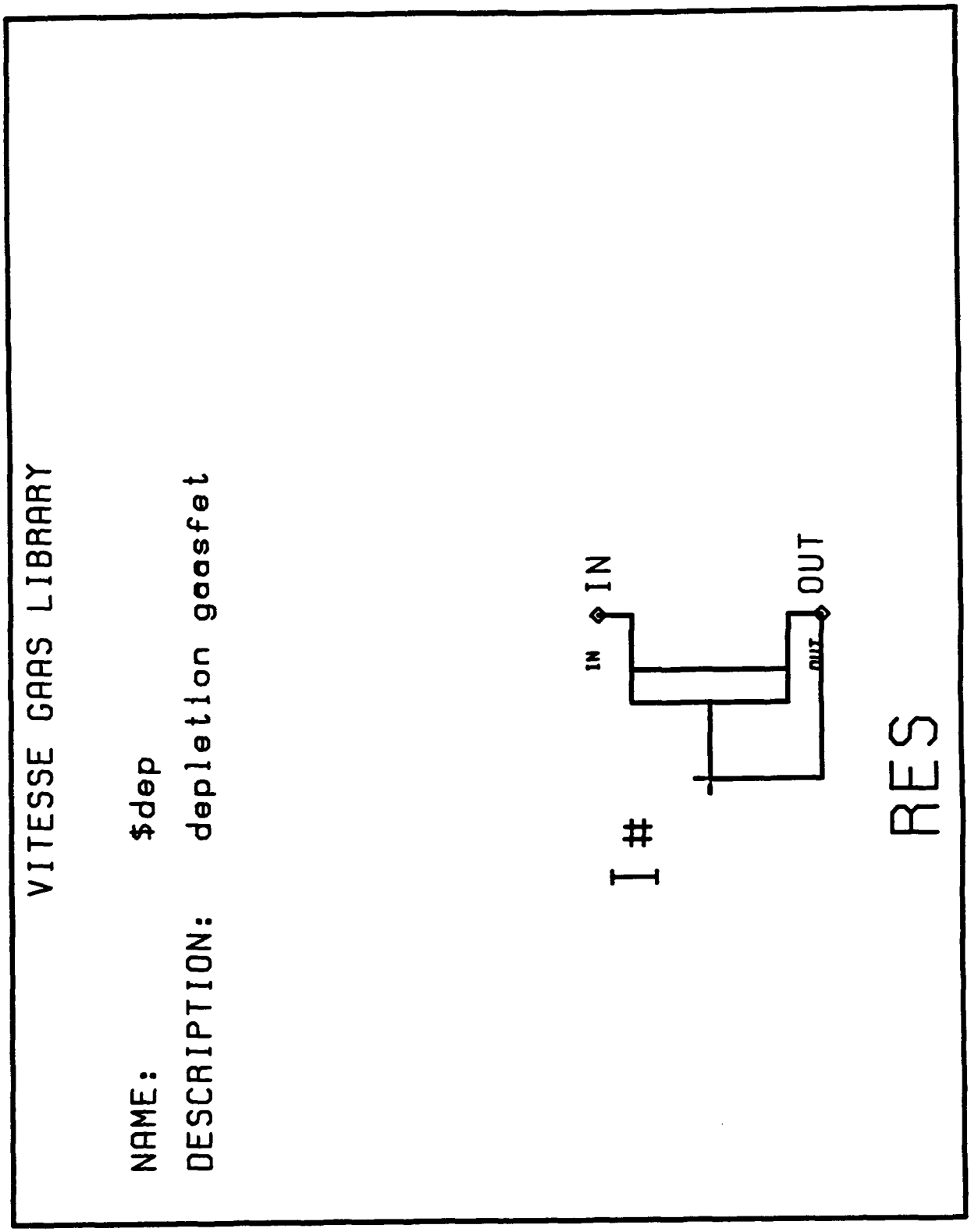

GALU
galu.bin
dst0(15:0)
dst1(15:0)
dco(3:0)
addr(15:0)
aco(3:0)
sdn0(15:0)
sdn1(15:0)
smpy(15:0)
bran(15:0)
sbe(4:0)
dso(5:0)
dab(5:0)
dld(3:0)
dir(2:0)
dle(2:0)
doe(1:0)
dse(2:0)
dcin
dbe(1:0)
lye
sse(1:0)
saax(5:0)
sabx(5:0)
sld(1:0)
slf
sle(2:0)
acl
acin
sbd(1:0)
sbl(15:0)
dbd(4:0)
dnleb
init
stall(5:0)
clk
clkn

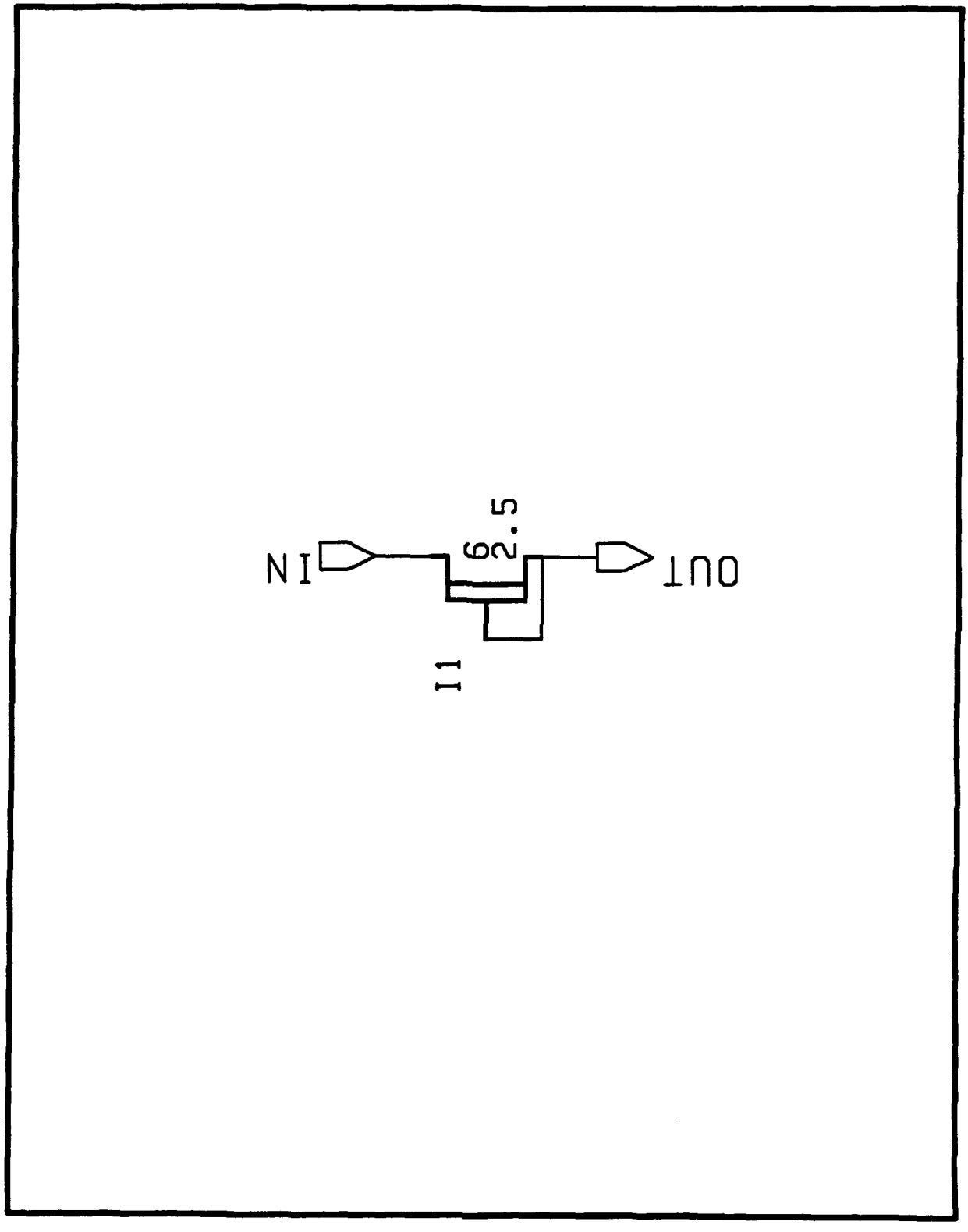

GALU
SRCMUX
DESTMUX
EXTEND
DESTI (15:0)

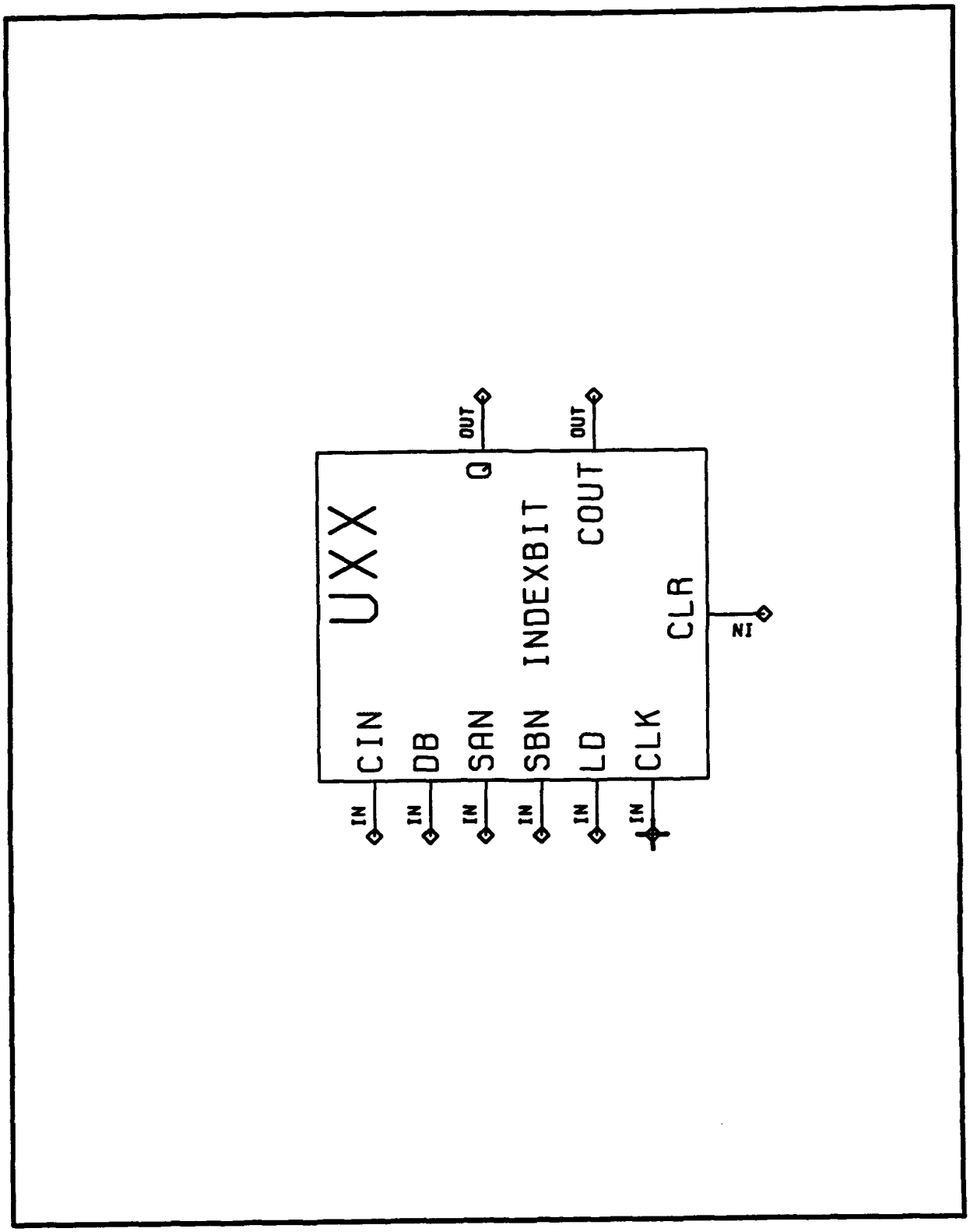


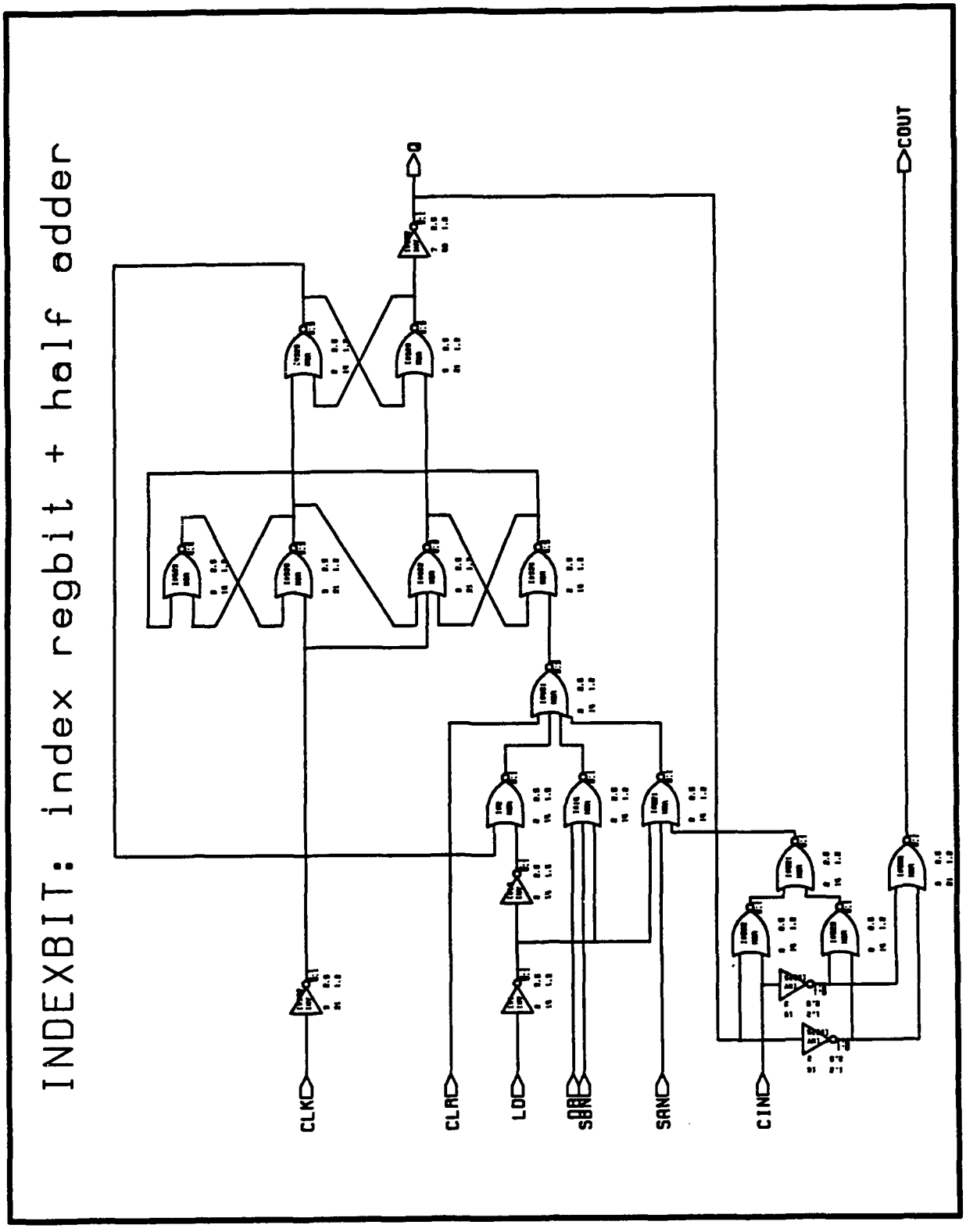

OUT
I #
IN
OUT

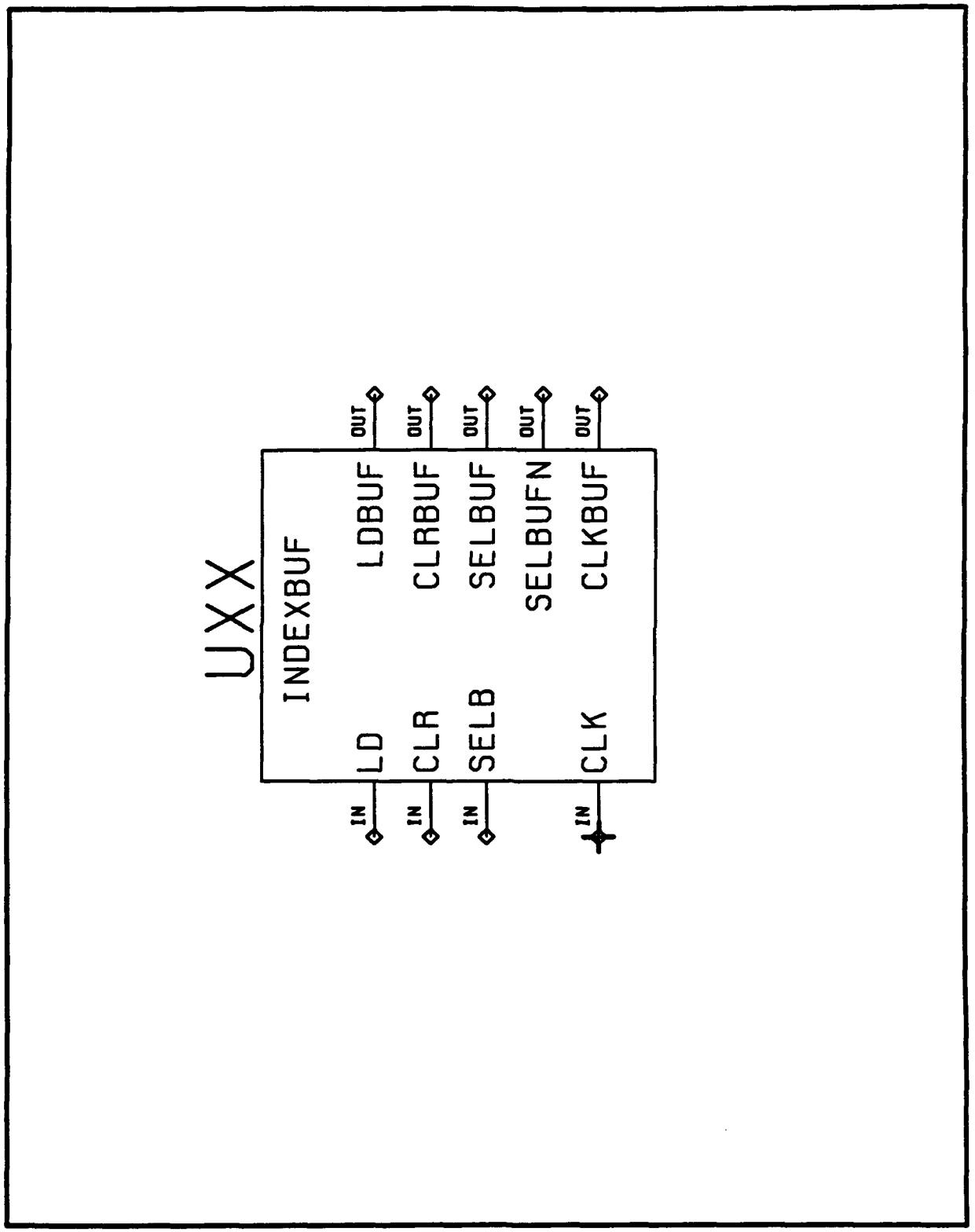

IBUFSMALL
O1N
O1
I1
INV
INV
INV
8.2
2.5
1.2
7
49
4
28

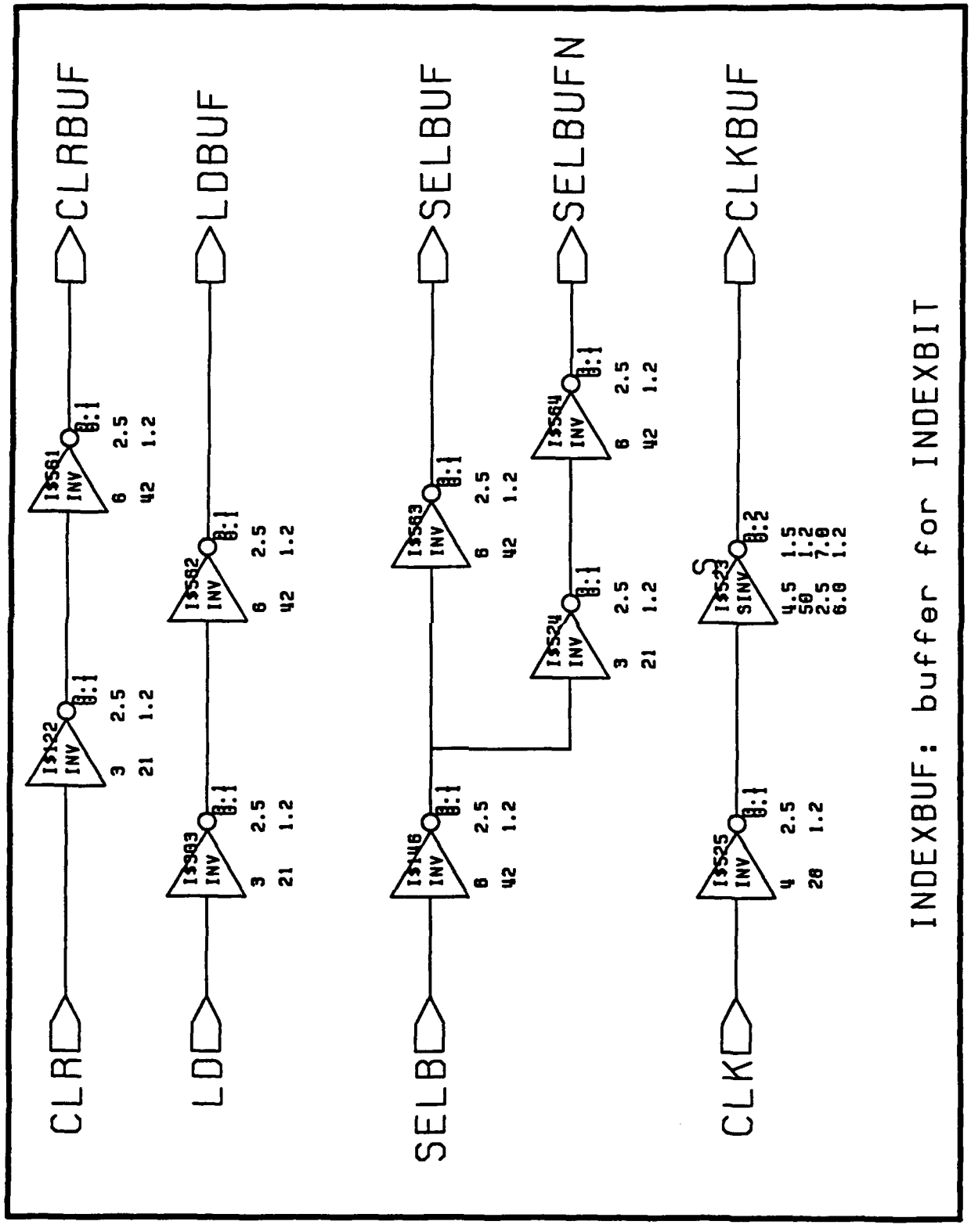

VITESSE GAAS LIBRARY
NAME: $dep
DESCRIPTION: depletion gaasfet
IN
OUT
I#
RES

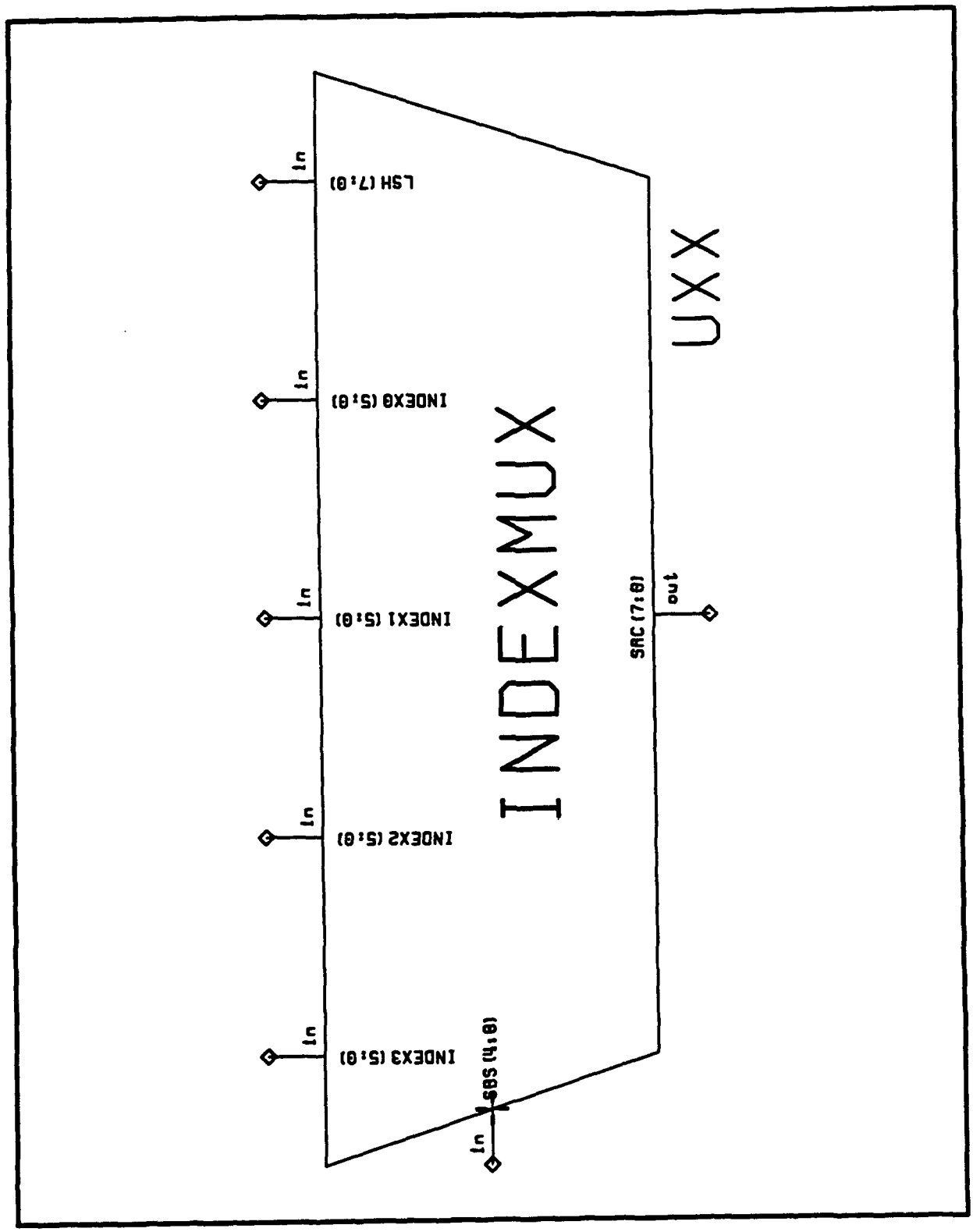

IN
62.5
OUT
11

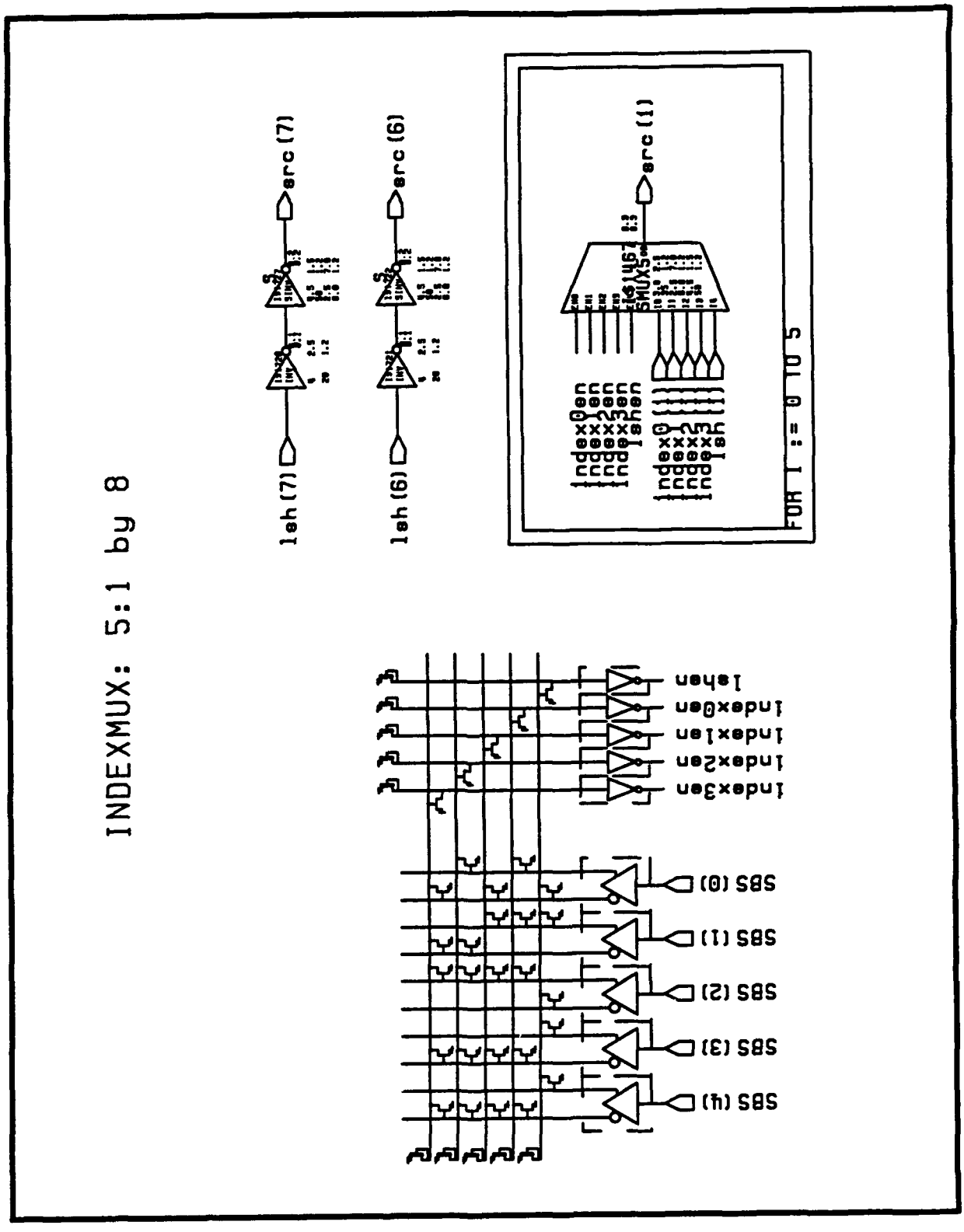

UXX
CIN
DB
SAN
SBN
LD
CLK
IN
IN
IN
IN
IN
IN
Q
INDEXBIT
COUT
CLR
OUT
OUT
NI

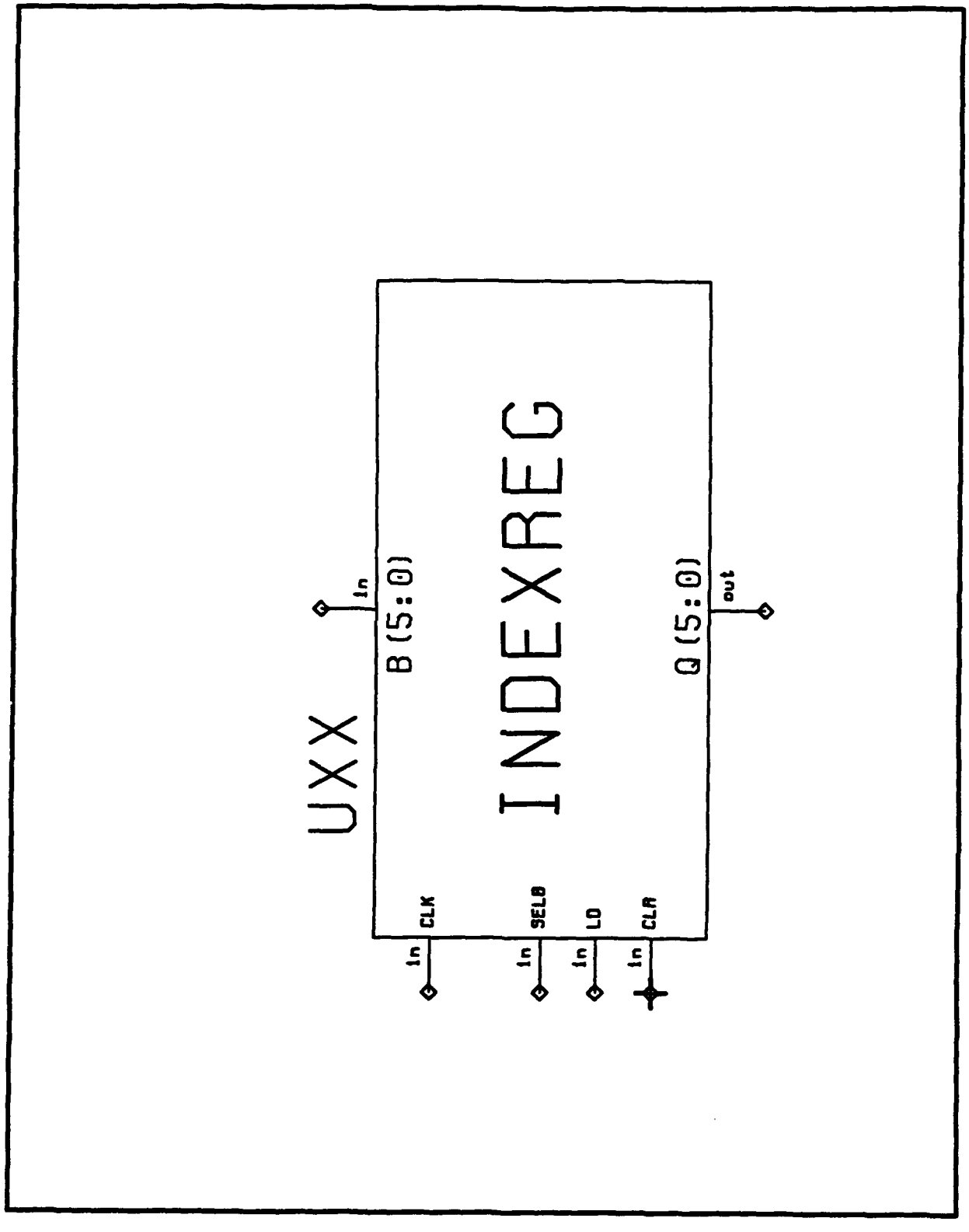

INDEXBIT: index regbit + half adder
Q
COUT
CLKD
CLRD
LDD
SBRD
SAND
CIND

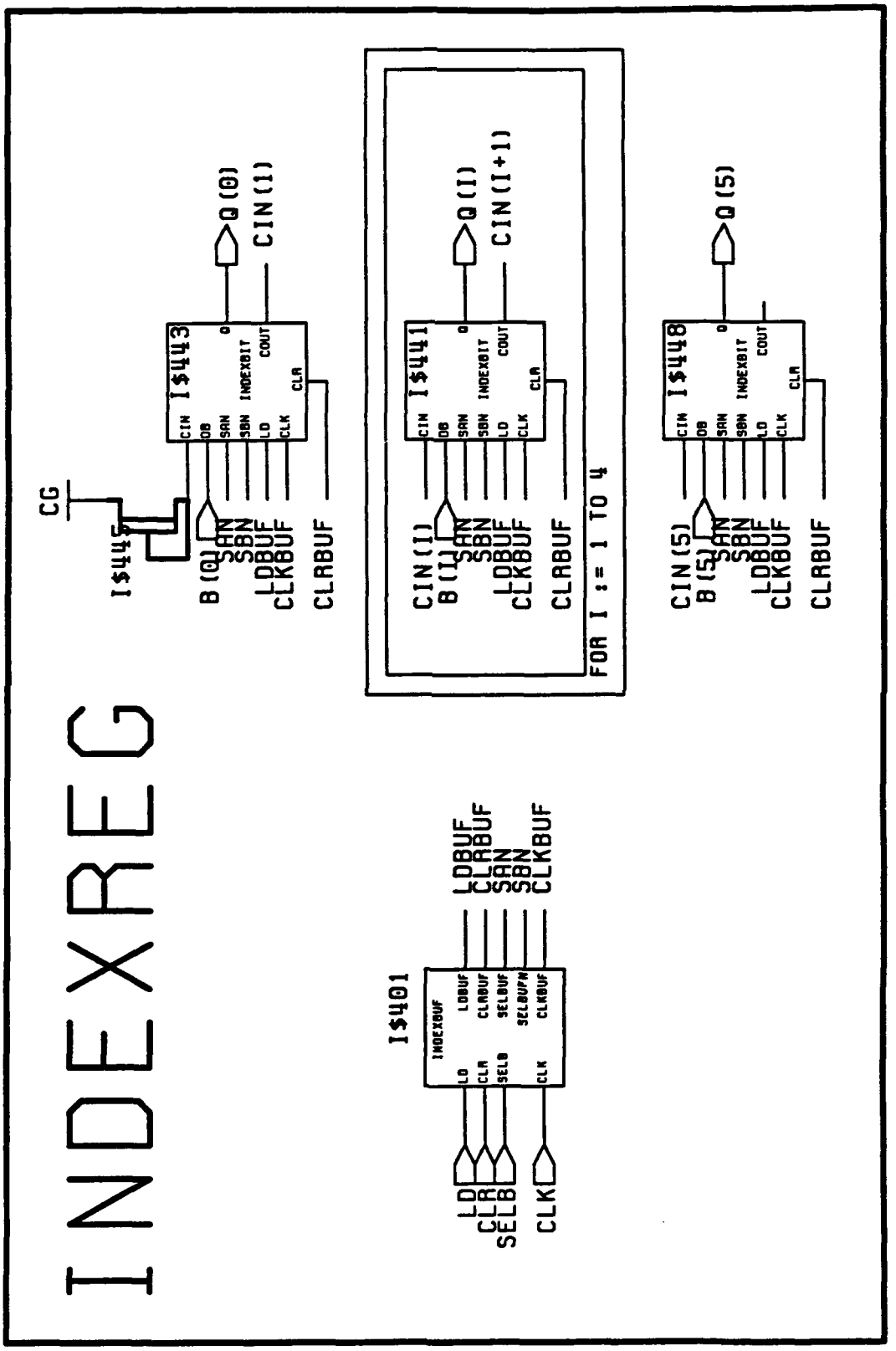

UXX
INDEXBUF
LDBUF
CLRBUF
SELBUF
SELBUFN
CLKBUF
LD
CLR
SELB
CLK
OUT
OUT
OUT
OUT
OUT
IN
IN
IN
IN

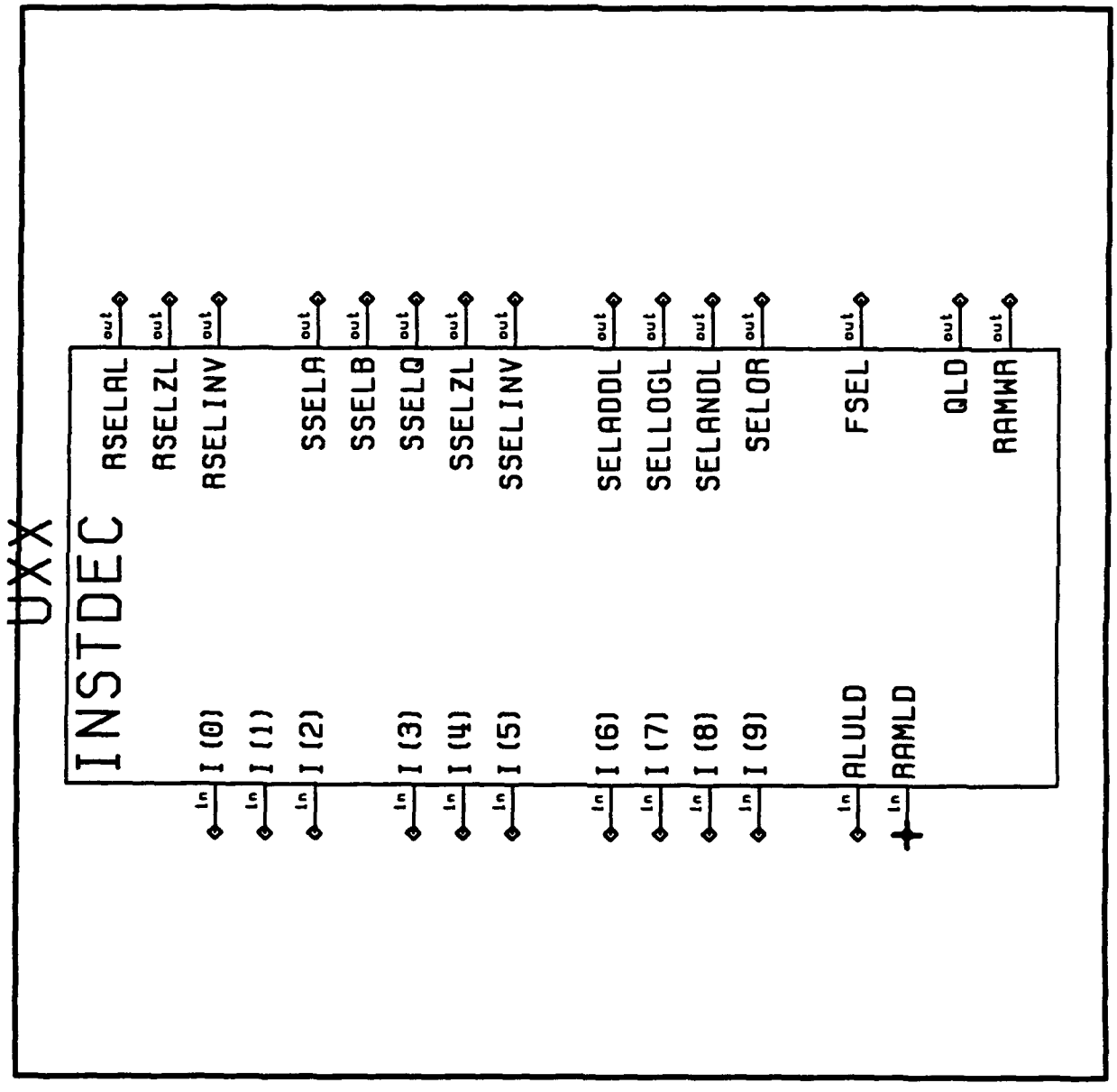

INDEXBUF: buffer for INDEXBIT
CLRBUF
LDBUF
SELBUF
SELBUFN
CLKBUF
CLR
LD
SELB
CLK
S
I3522 INV 3 2.5 21 1.2
I3561 INV 6 2.5 42 1.2
I3562 INV 6 2.5 42 1.2
I3563 INV 3 2.5 21 1.2
I3546 INV 6 2.5 42 1.2
I3583 INV 6 2.5 42 1.2
I3524 INV 3 2.5 21 1.2
I3564 INV 6 2.5 42 1.2
I3525 INV 4 2.5 20 1.2
I3523 SINV 4.5 1.5 50 1.2 2.5 7.0 6.0 1.2

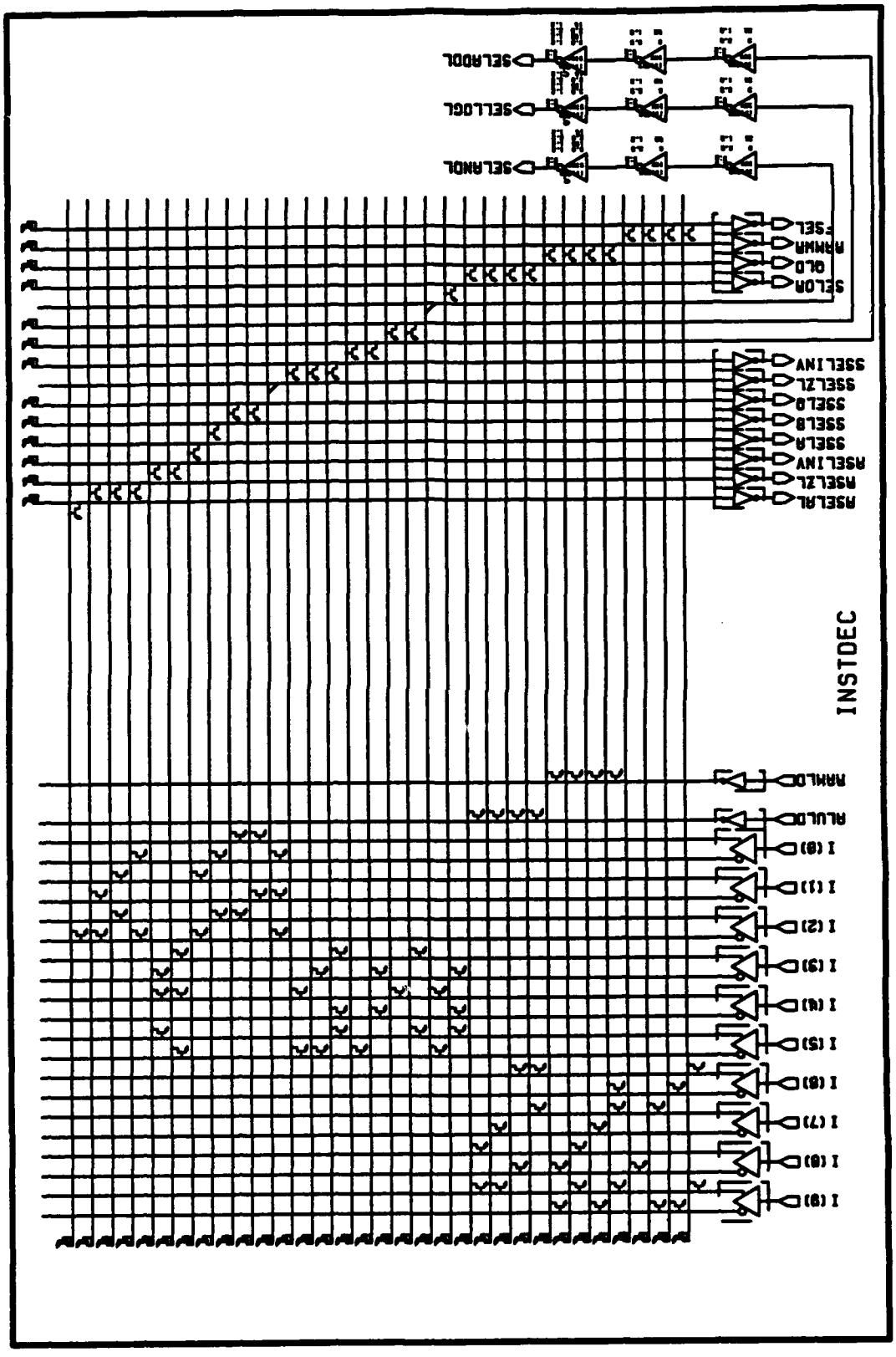

UXX
INDEXMUX
LSH (7:0)
INDEX0 (5:0)
INDEX1 (5:0)
INDEX2 (5:0)
INDEX3 (5:0)
SBS (4:0)
SRC (7:0)
in
out

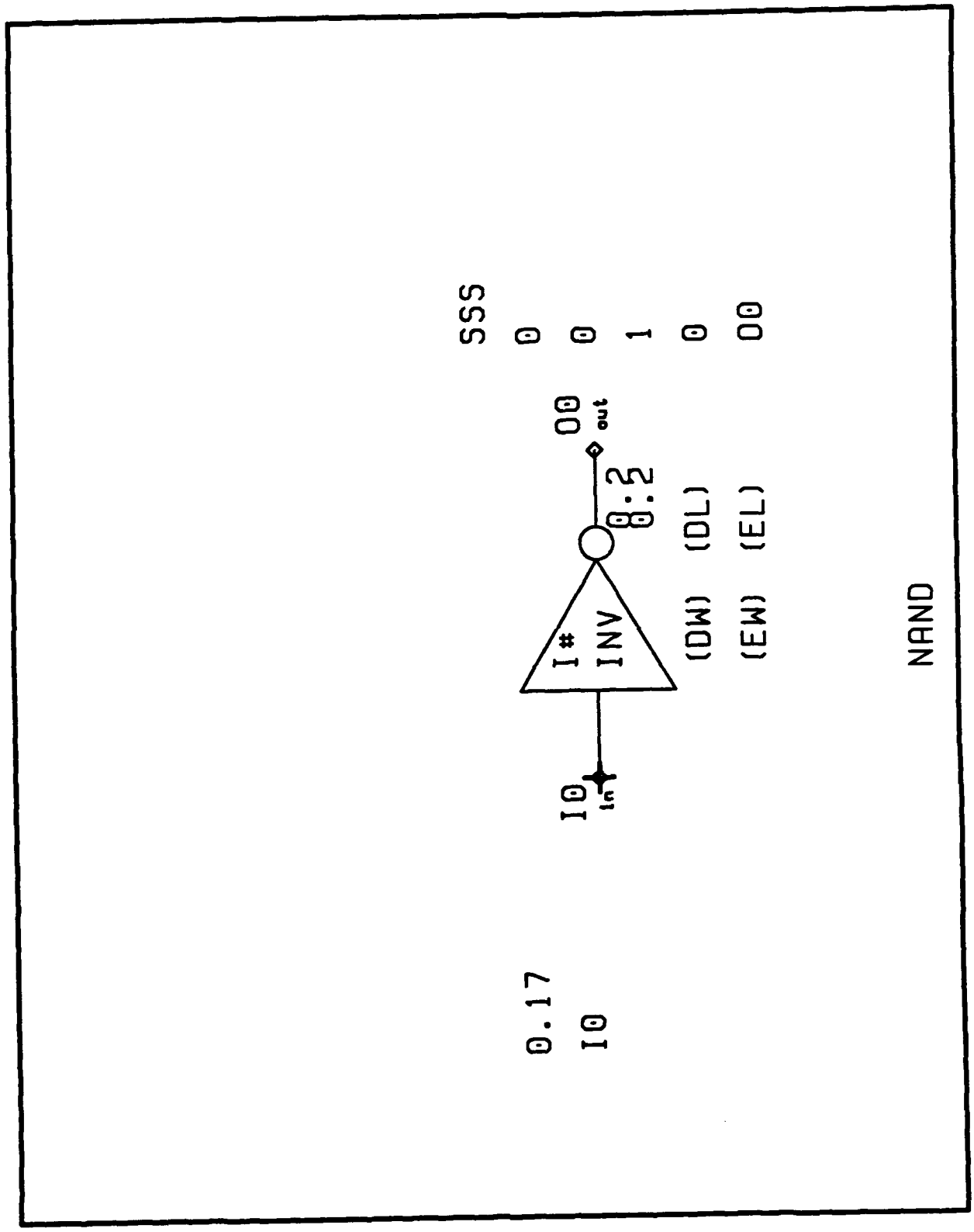

INDEXMUX: 5:1 by 8
src(7)
src(6)
src(1)
lsh(7)
lsh(6)
FOR I := 0 TO 5
lshen
index0en
index1en
index2en
index3en
SBS(0)
SBS(1)
SBS(2)
SBS(3)
SBS(4)

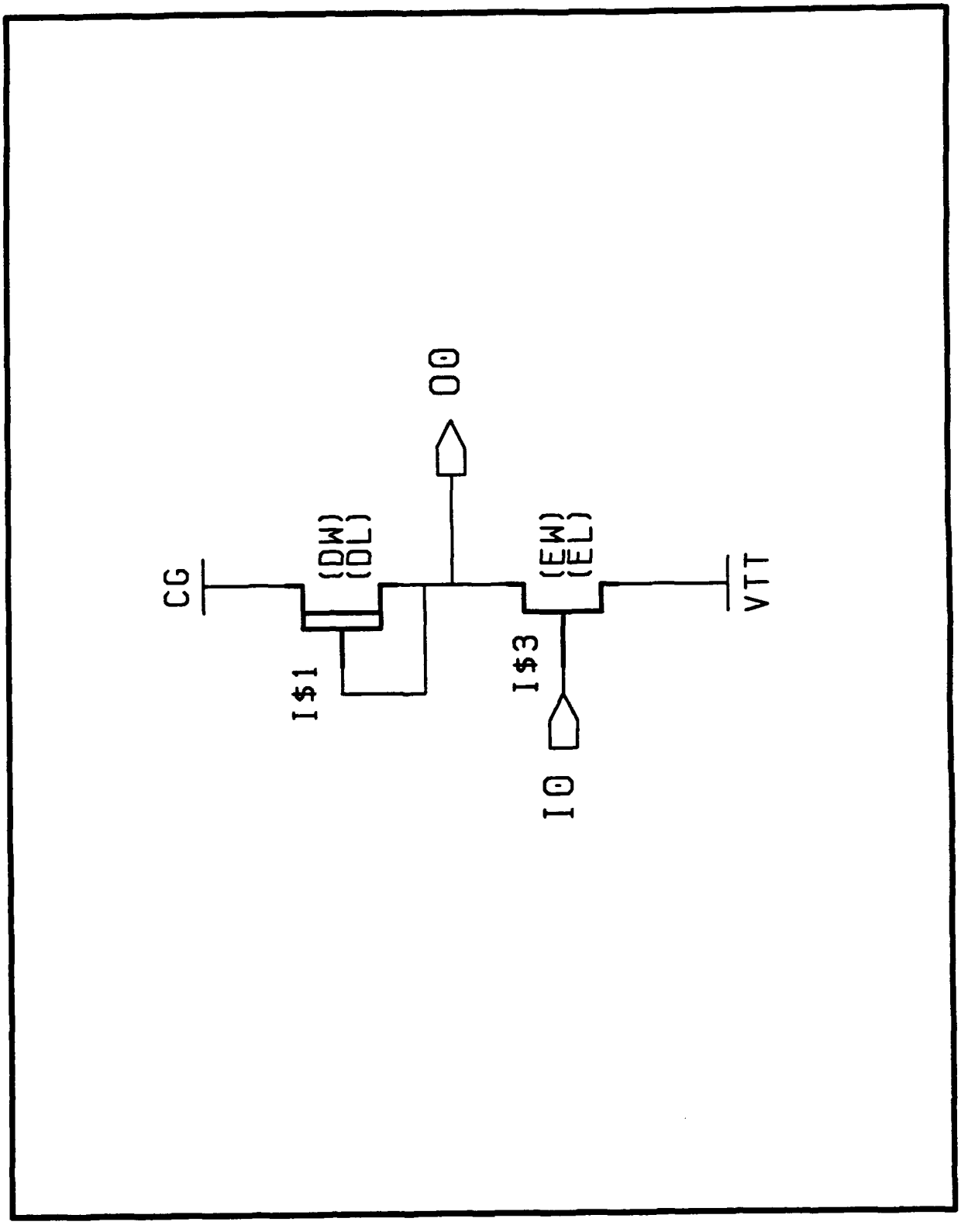

UXX
INDEXREG
B(5:0)
Q(5:0)
In
out
CLK
SELB
LD
CLR
In
In
In
In

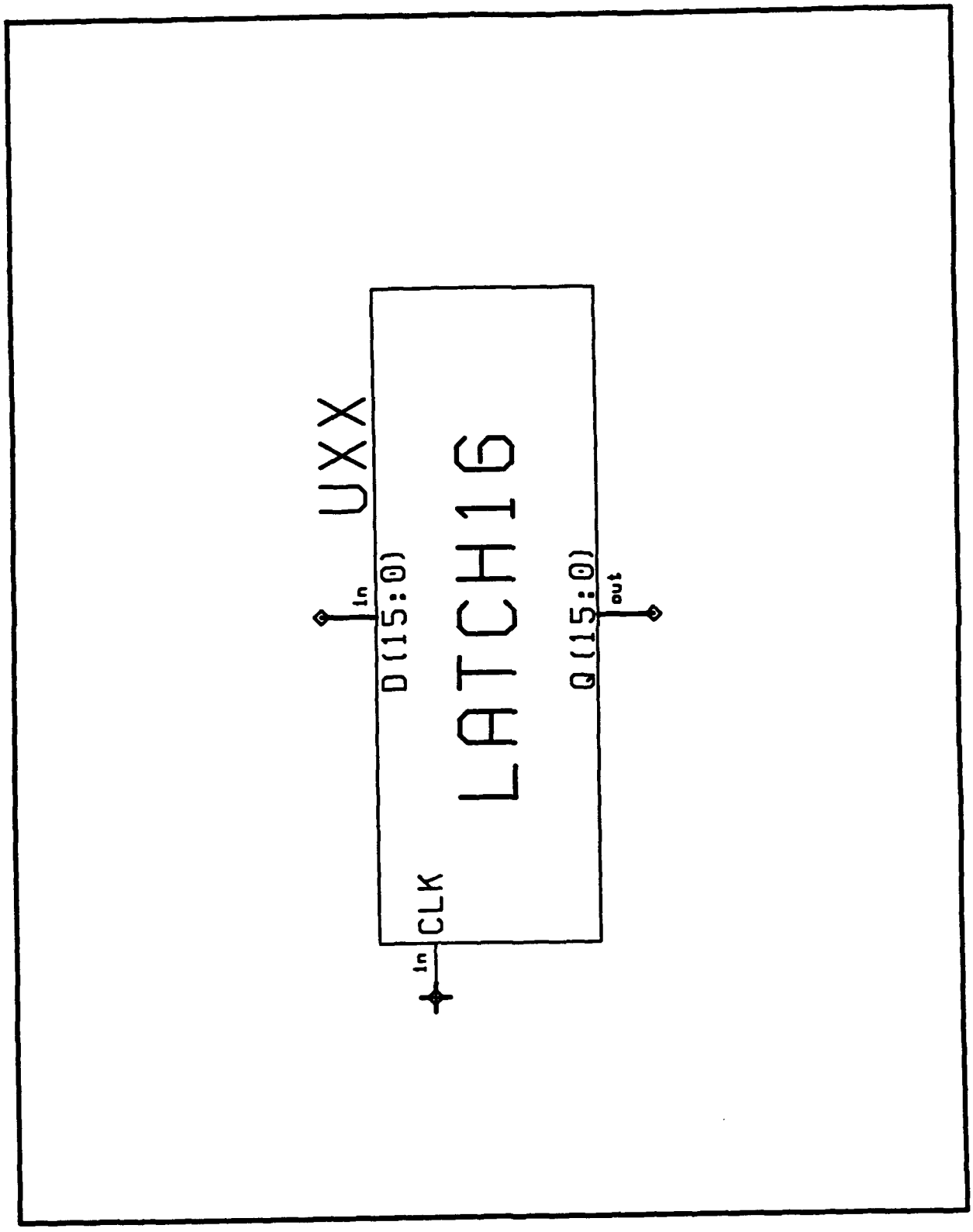

INDEXREG
I$401
INDEXBUF
LO
CLR
SELB
SELBUFN
CLKBUF
LDBUF
CLRBUF
SAN
SBN
CLKBUF
LD
CLR
SELB
CLK
FOR I := 1 TO 4
I$443
I$441
I$448
CIN
DB
SAN
SBN
LD
CLK
CLR
INDEXBIT
COUT
Q(0)
CIN(1)
Q(I)
CIN(I+1)
Q(5)
CG
I$445
B(0)
B(I)
B(5)
CIN(I)
CIN(5)
LDBUF
CLKBUF
CLRBUF

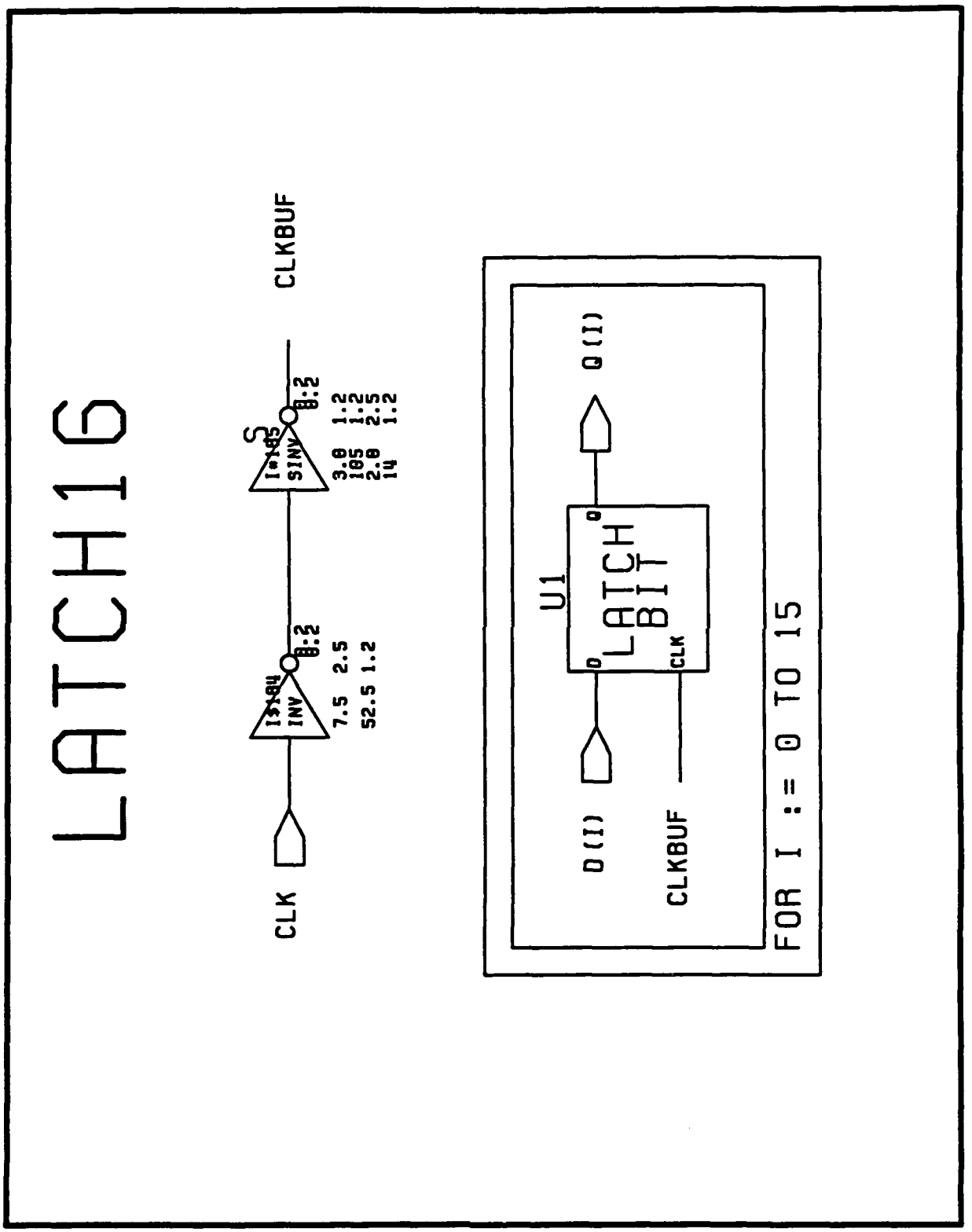

UXX
INSTDEC
RSELAL
RSELZL
RSELINV
SSELA
SSELB
SSELQ
SSELZL
SSELINV
SELADDL
SELLOGL
SELANDL
SELOR
FSEL
QLD
RAMWR
I (0)
I (1)
I (2)
I (3)
I (4)
I (5)
I (6)
I (7)
I (8)
I (9)
ALULD
RAMLD
out
in

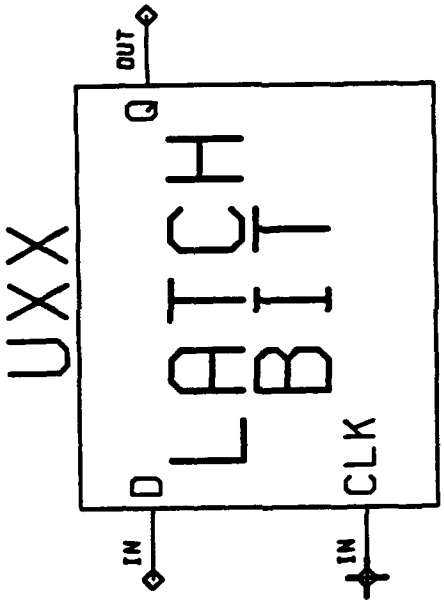

INSTDEC

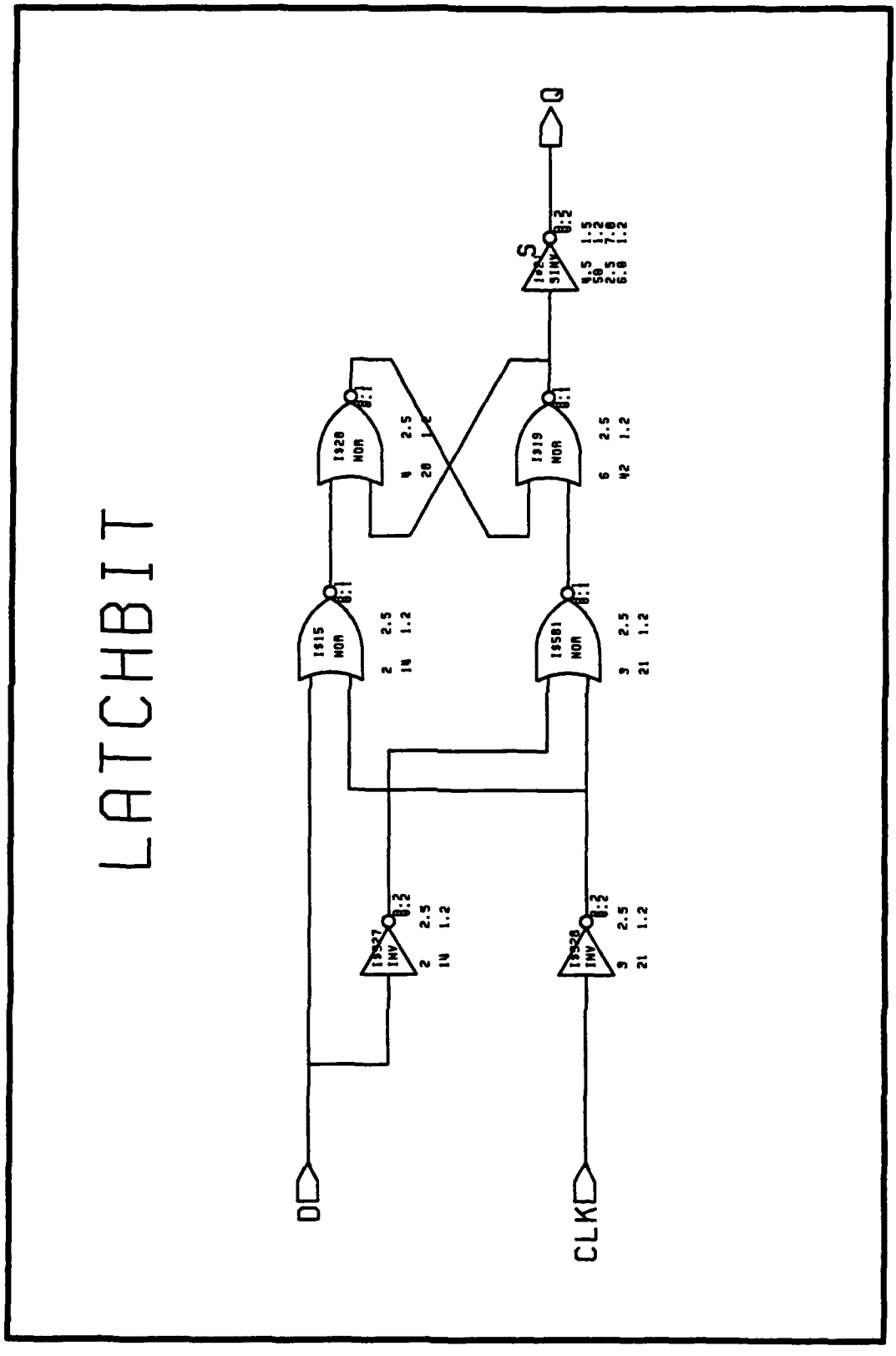

SSS
0 0 1 0 00
00
out
8.2
I#
INV
(DW) (DL)
(EW) (EL)
NAND
I0
in
0.17
I0

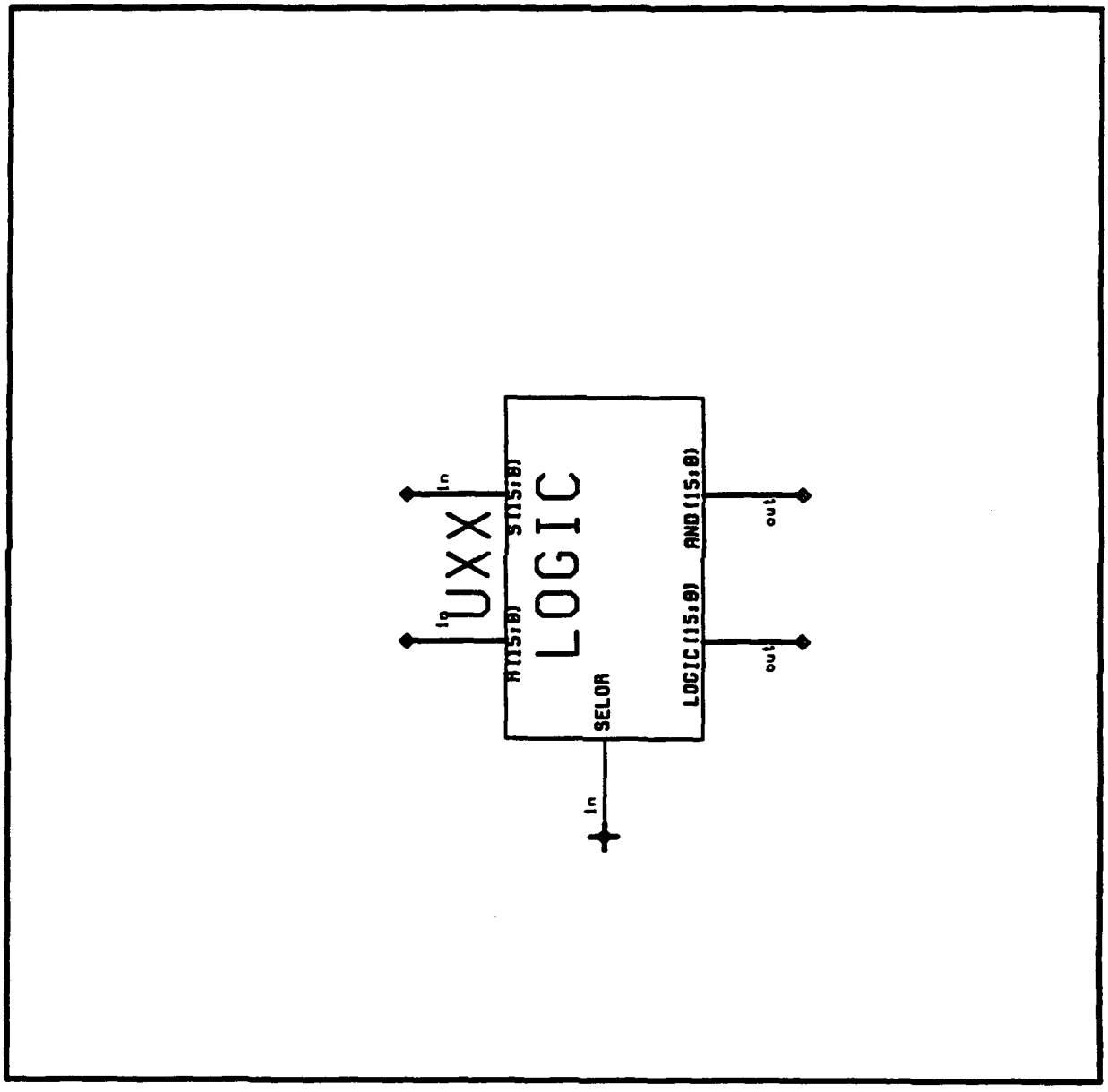

O0
CG
(DW)
(DL)
(EW)
(EL)
VTT
I$1
I$3
IO

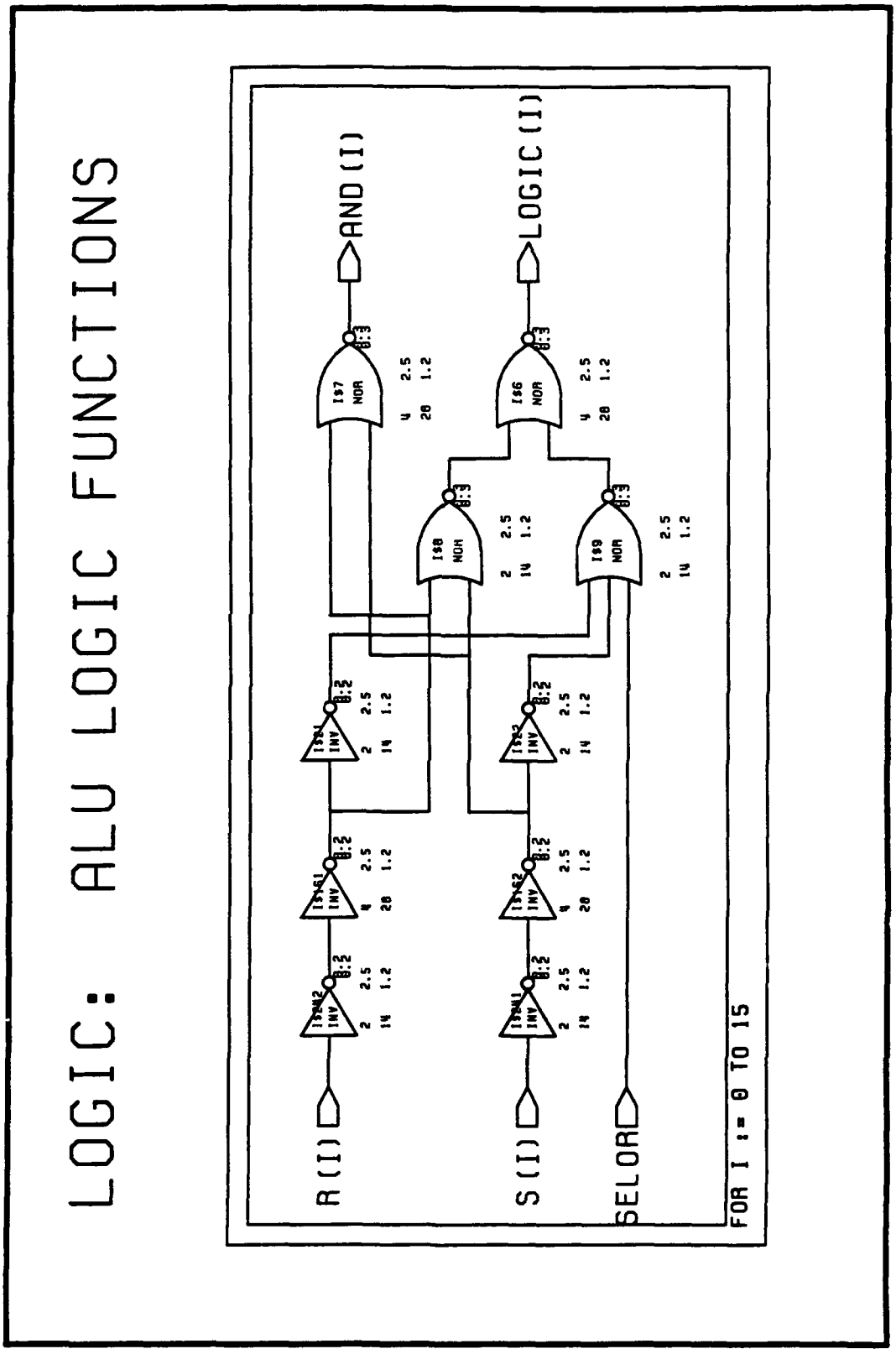

UXX
LATCH16
In
D(15:0)
Q(15:0)
out
CLK
In

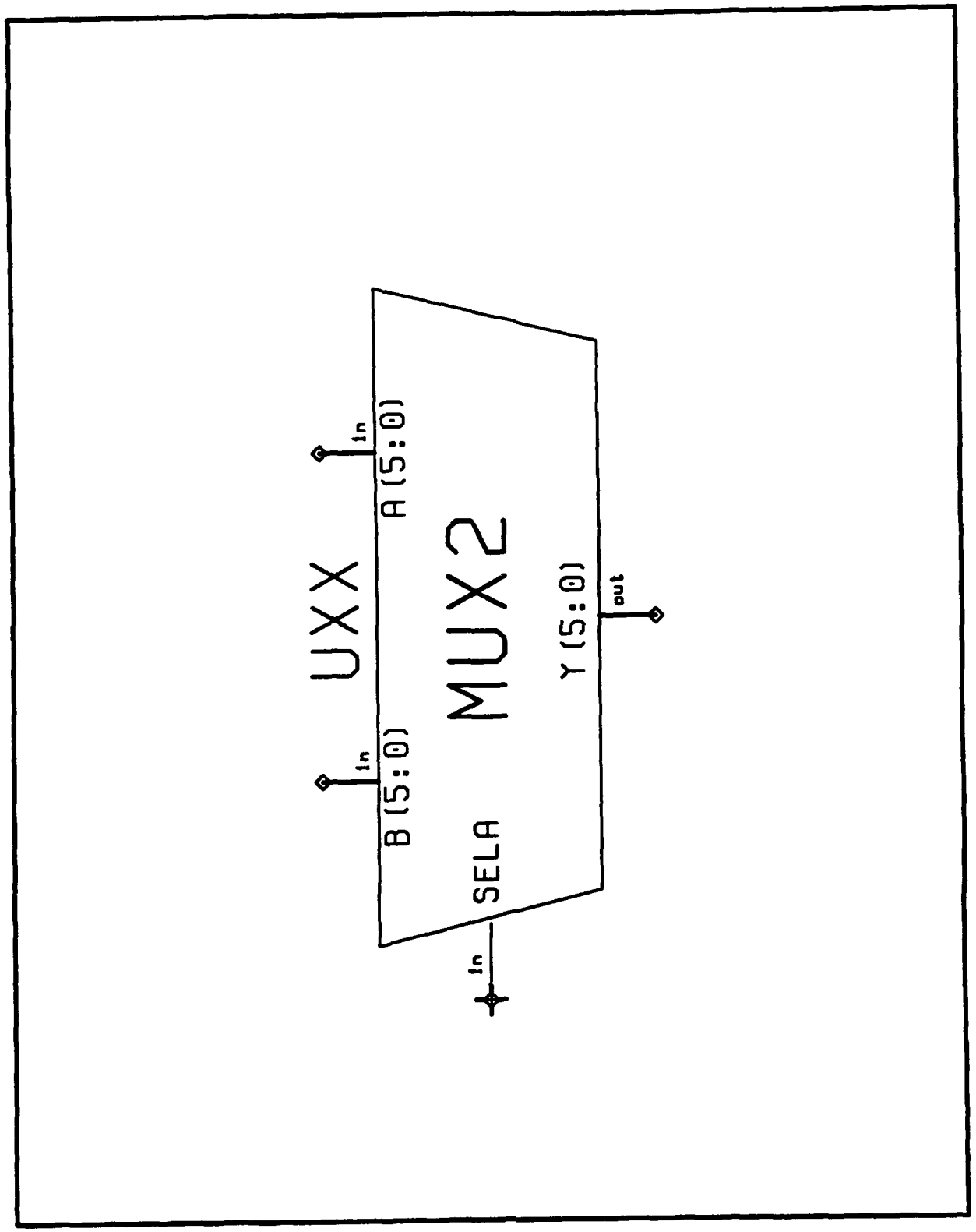

LATCH16
CLKBUF
S
I*185
SINV
8.2
3.0 1.2
105 1.2
2.0 2.5
14 1.2
I*184
INV
8.2
7.5 2.5
52.5 1.2
CLK
U1
LATCH
BIT
D
Q
CLK
Q(I)
D(I)
CLKBUF
FOR I := 0 TO 15

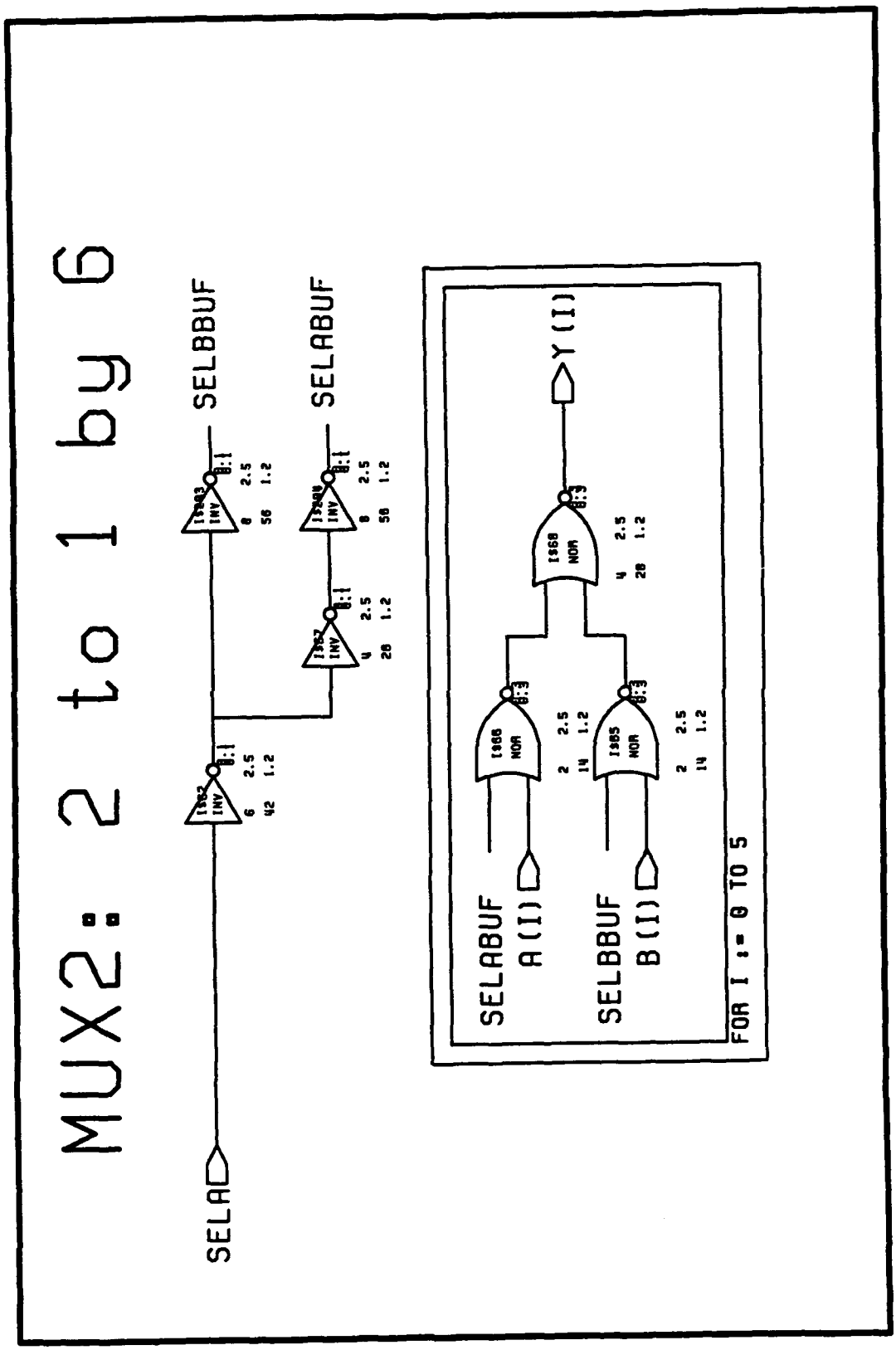

UXX
1BIT LATCH
D
Q
CLK
IN
IN
OUT

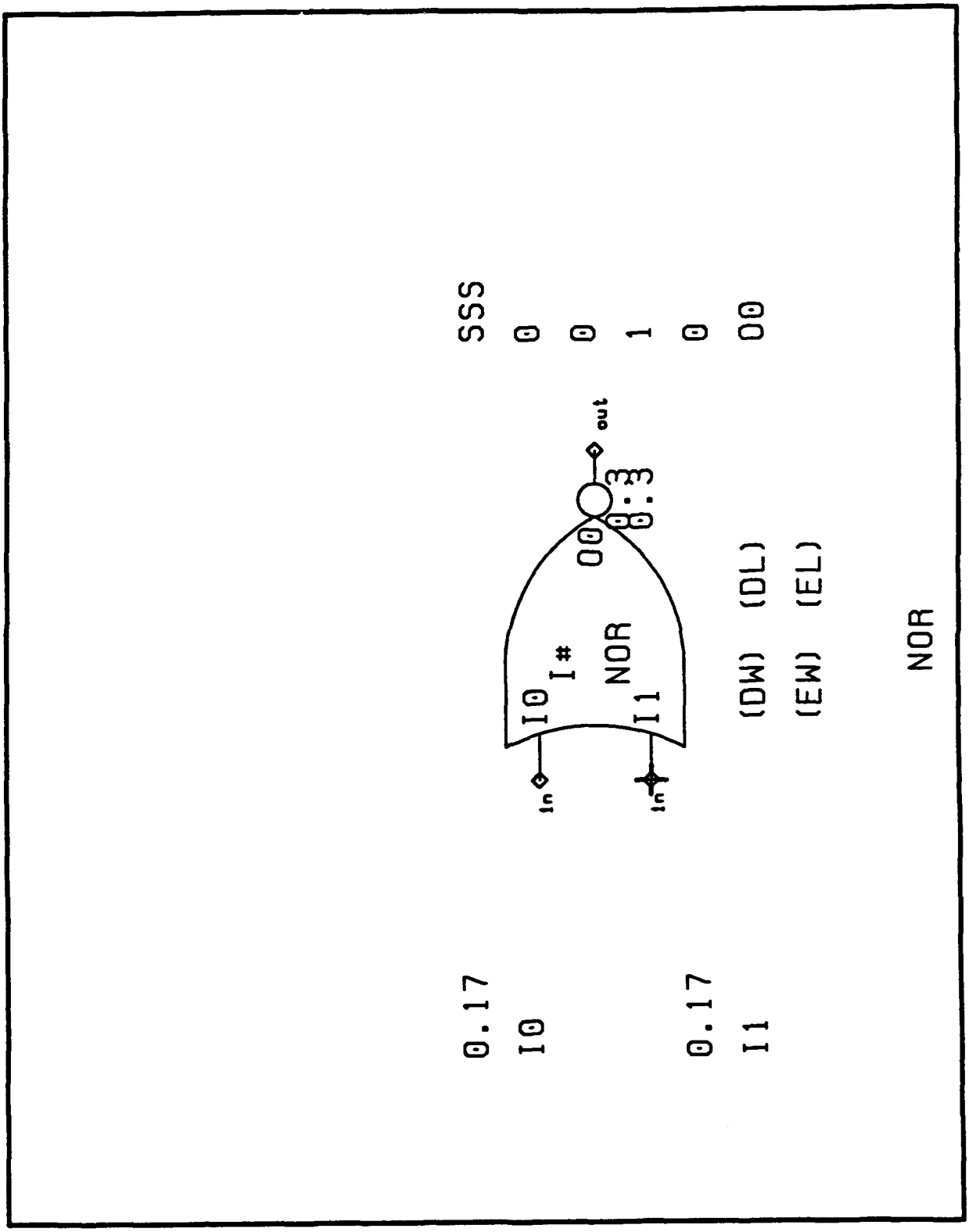

LATCHBIT
Q
S
D
CLK
I920 NOR
I919 NOR
I915 NOR
I9581 NOR
I9537 INV
I9538 INV

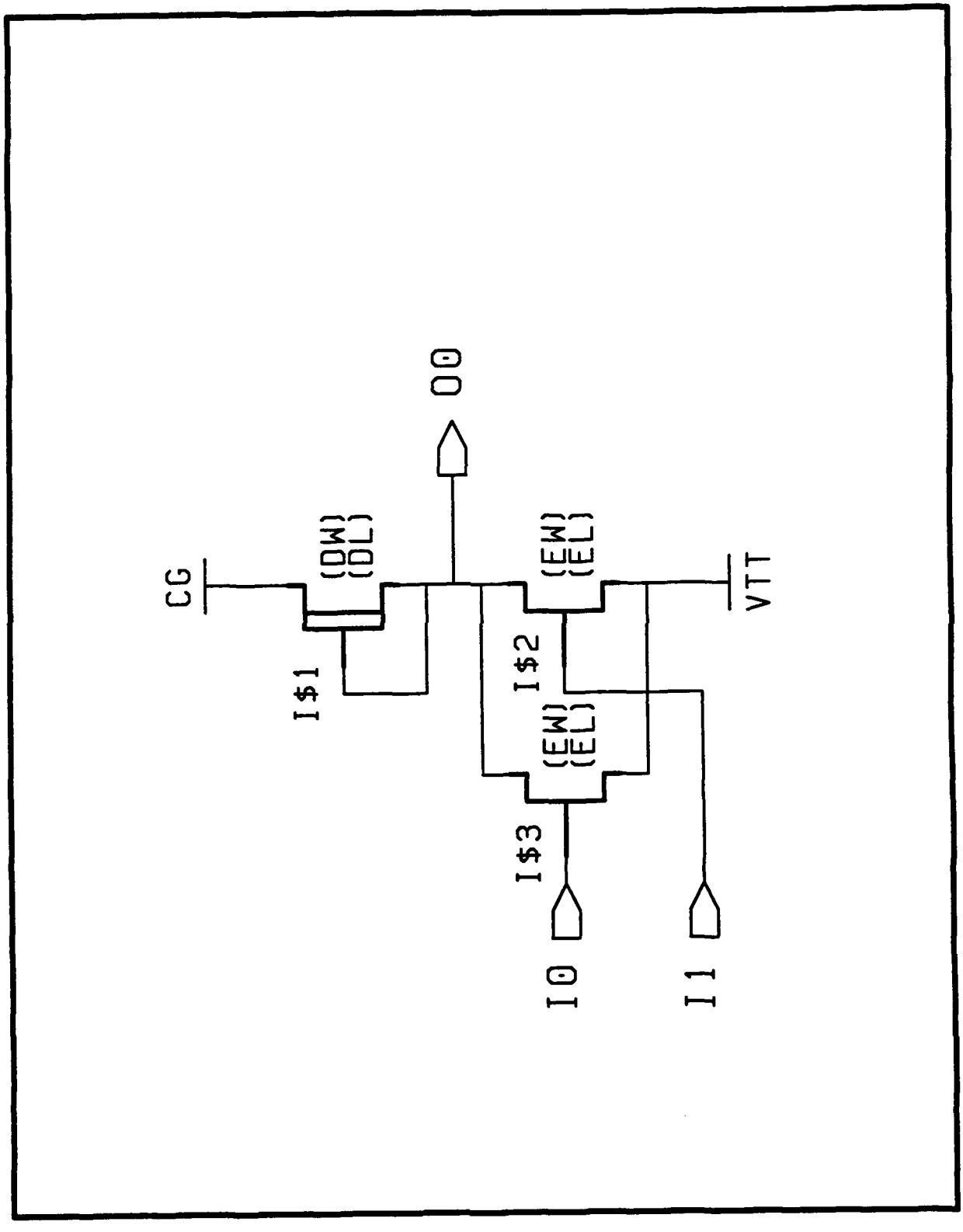

UXX
LOGIC
in
S[15:0]
A[15:0]
SELOR
in
AND[15:0]
out
LOGIC[15:0]
out

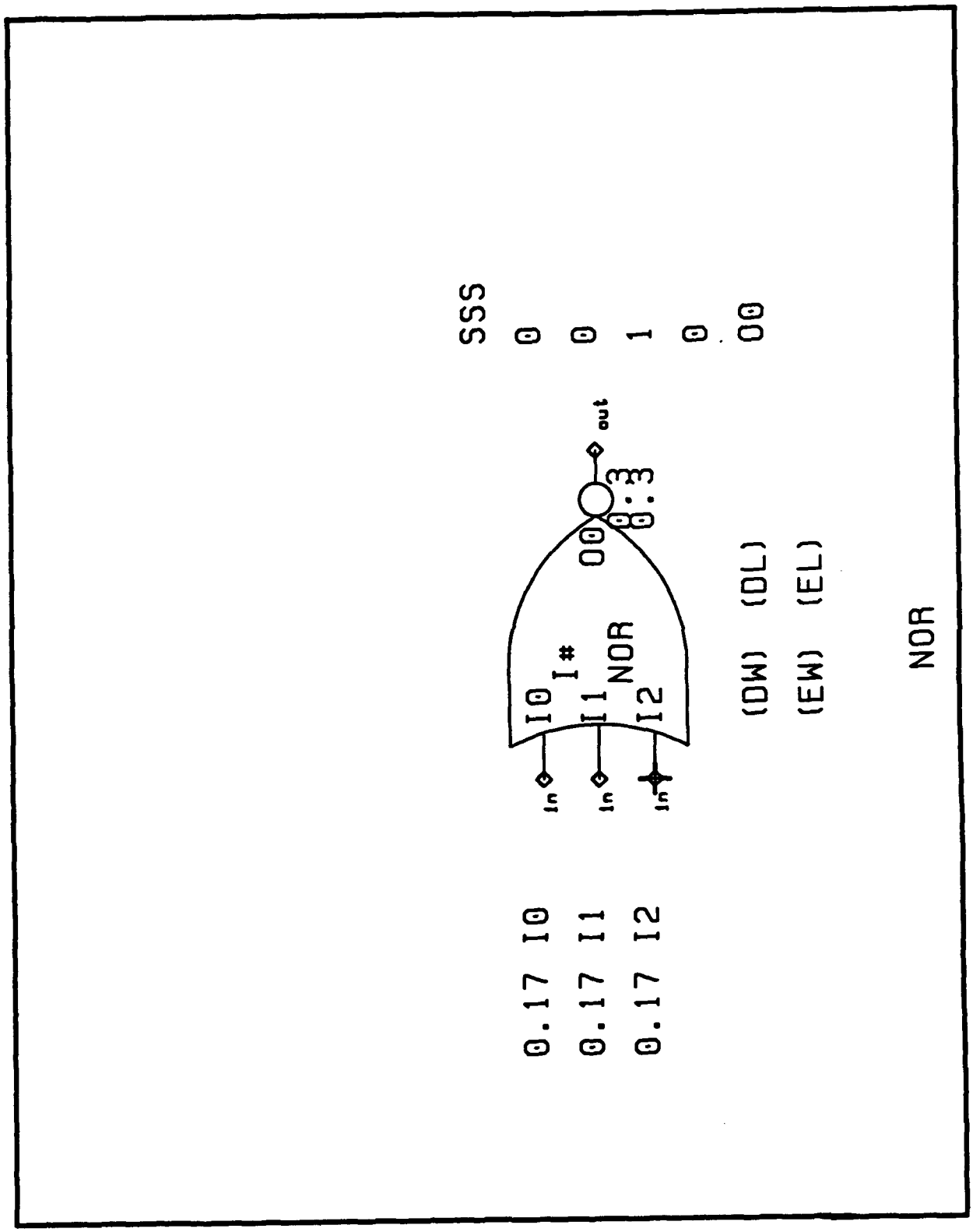

LOGIC: ALU LOGIC FUNCTIONS
AND(I)
LOGIC(I)
R(I)
S(I)
SELOR
FOR I := 0 TO 15

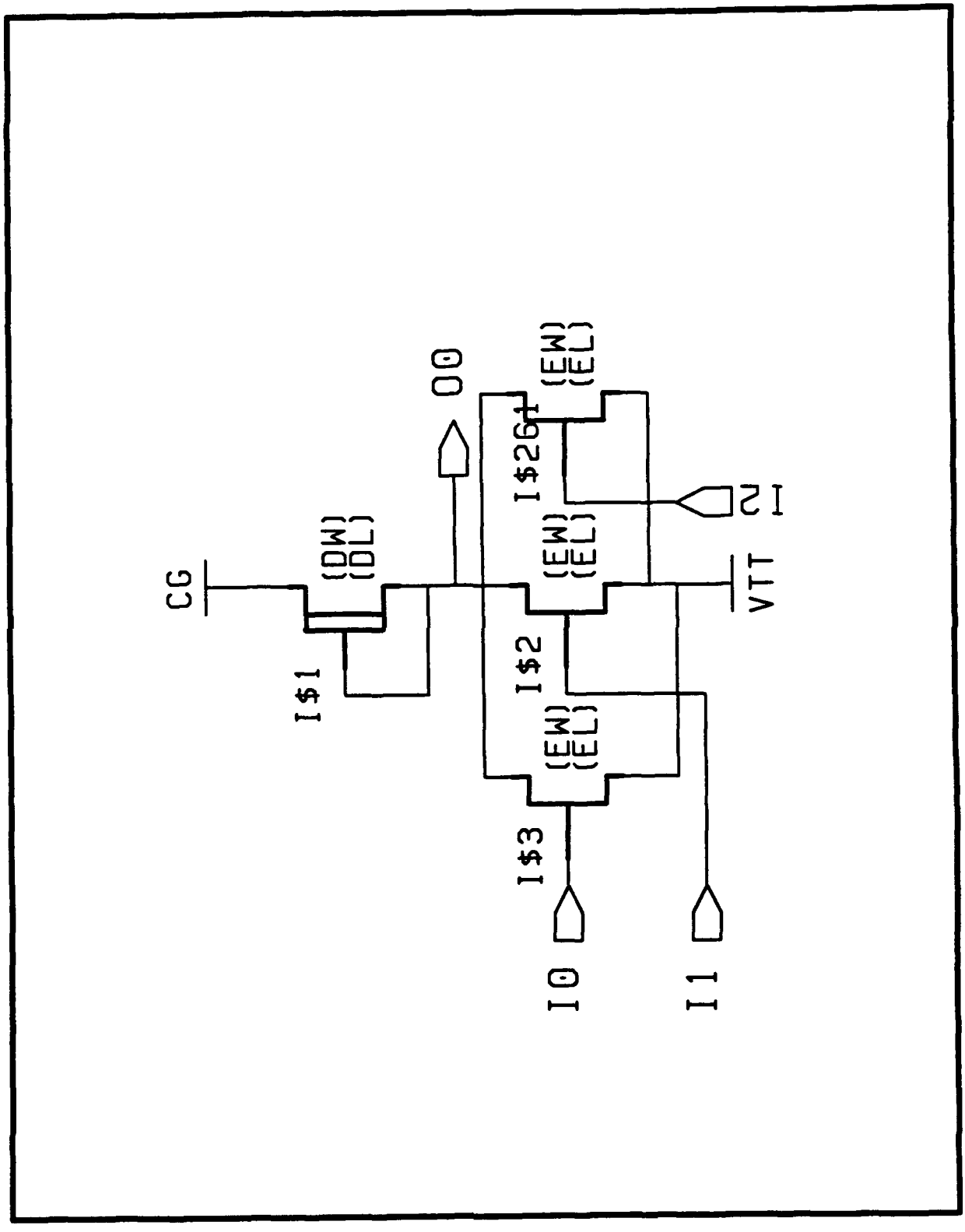

UXX
MUX2
A(5:0)
B(5:0)
SELA
Y(5:0)
in
in
in
out

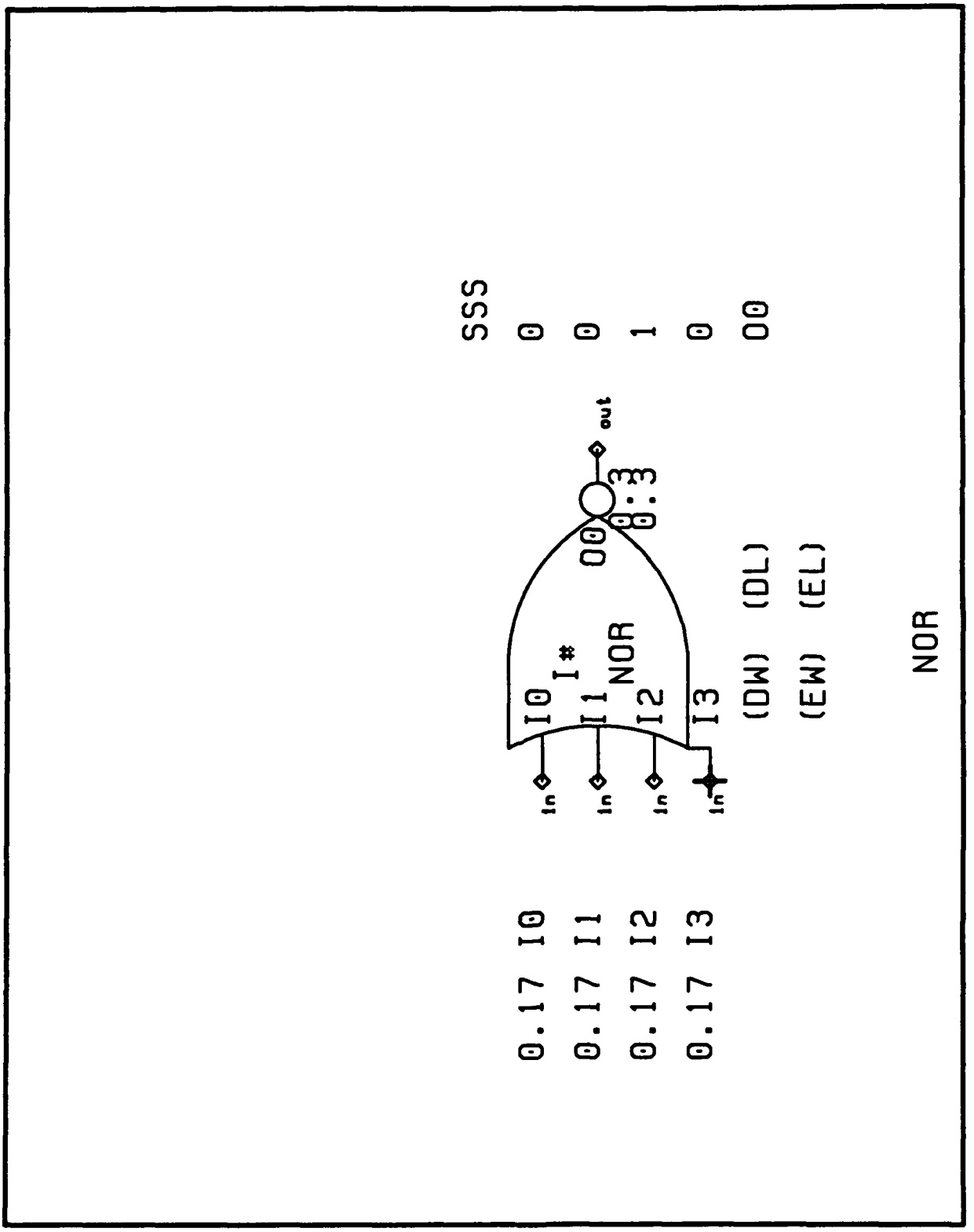

MUX2: 2 to 1 by 6
SELBBUF
SELABUF
SELA
Y(I)
SELABUF
A(I)
SELBBUF
B(I)
FOR I := 0 TO 5

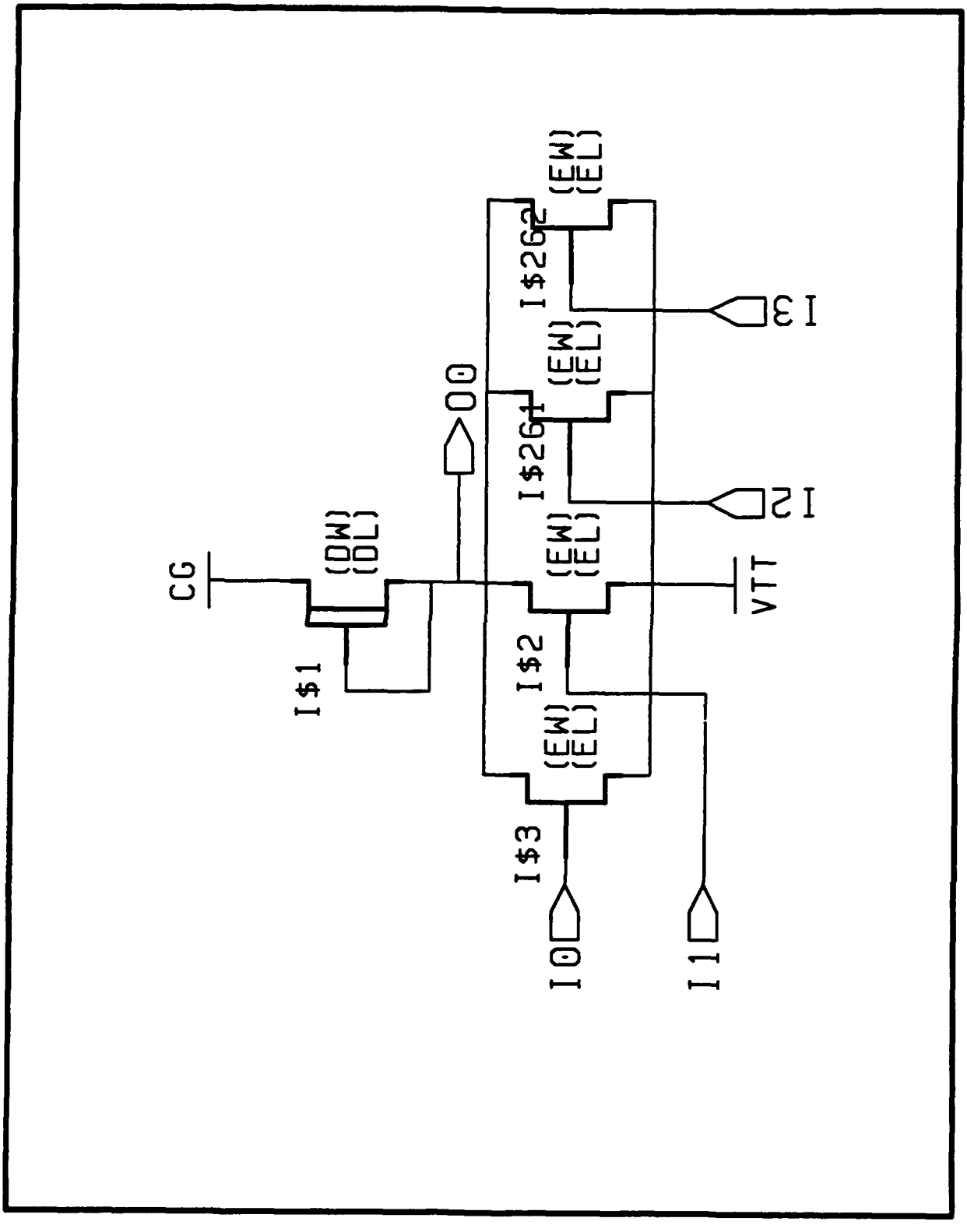

SSS
0
0
1
0
00
out
8.3
00
I0
I#
NOR
I1
In
In
(DW) (DL)
(EW) (EL)
NOR
0.17
I0
0.17
I1

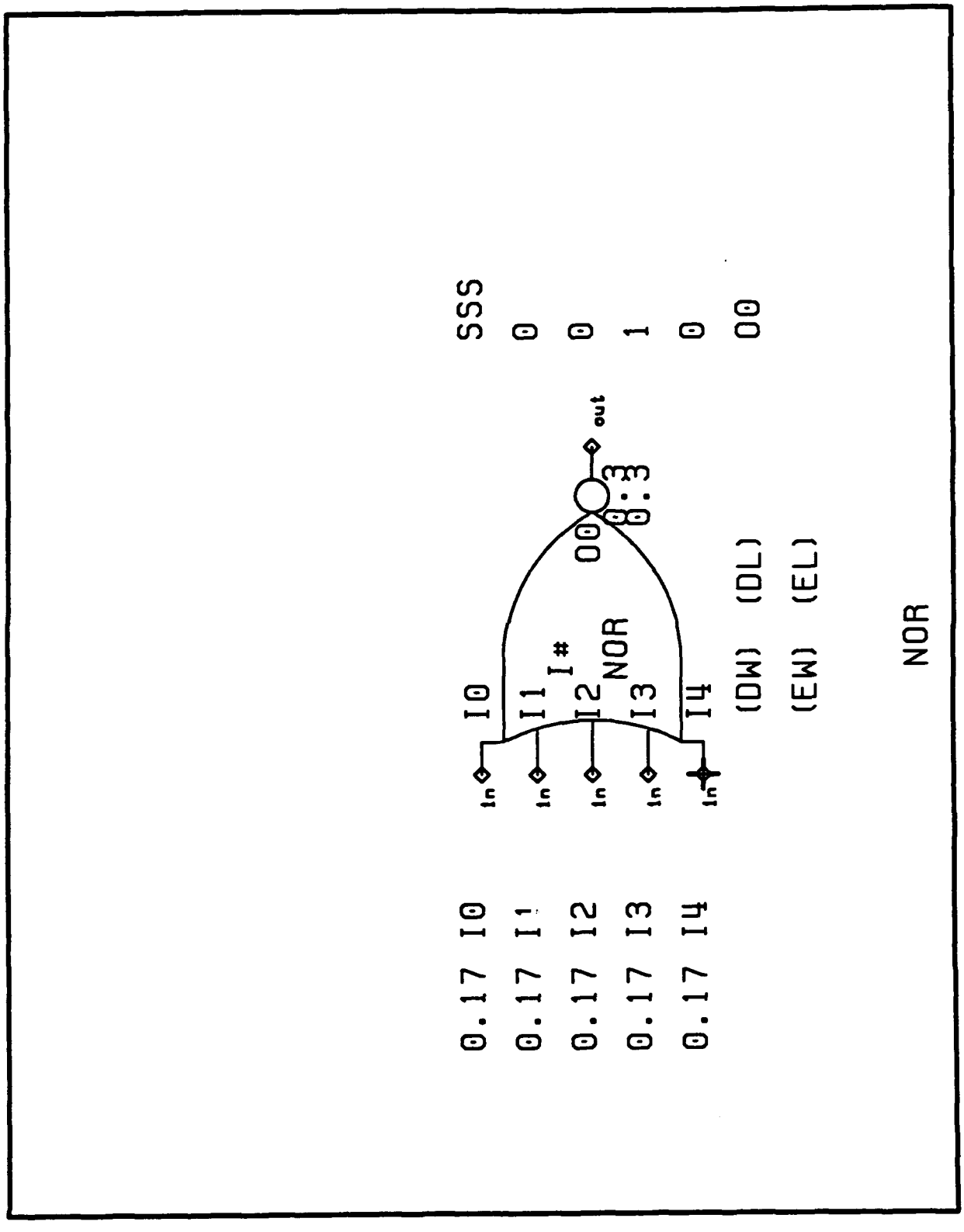

O0
CG
(DW)
(DL)
(EW)
(EL)
VTT
I$1
I$2
(EW)
(EL)
I$3
I0
I1

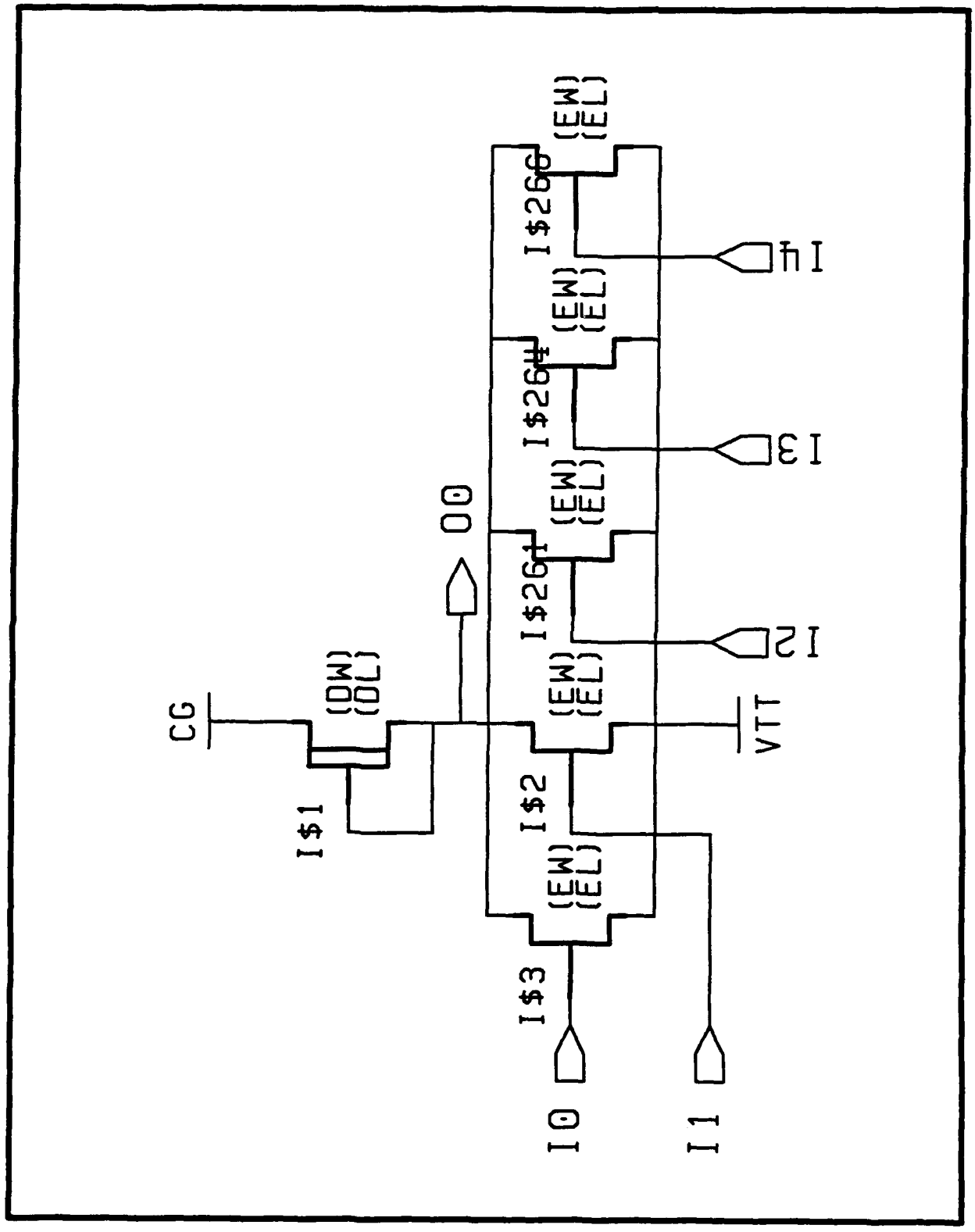

SSS
0 0 1 0.00
out
0.3
00
I0
I#
I1
NOR
I2
in
in
in
(DW) (DL)
(EW) (EL)
NOR
0.17 I0
0.17 I1
0.17 I2

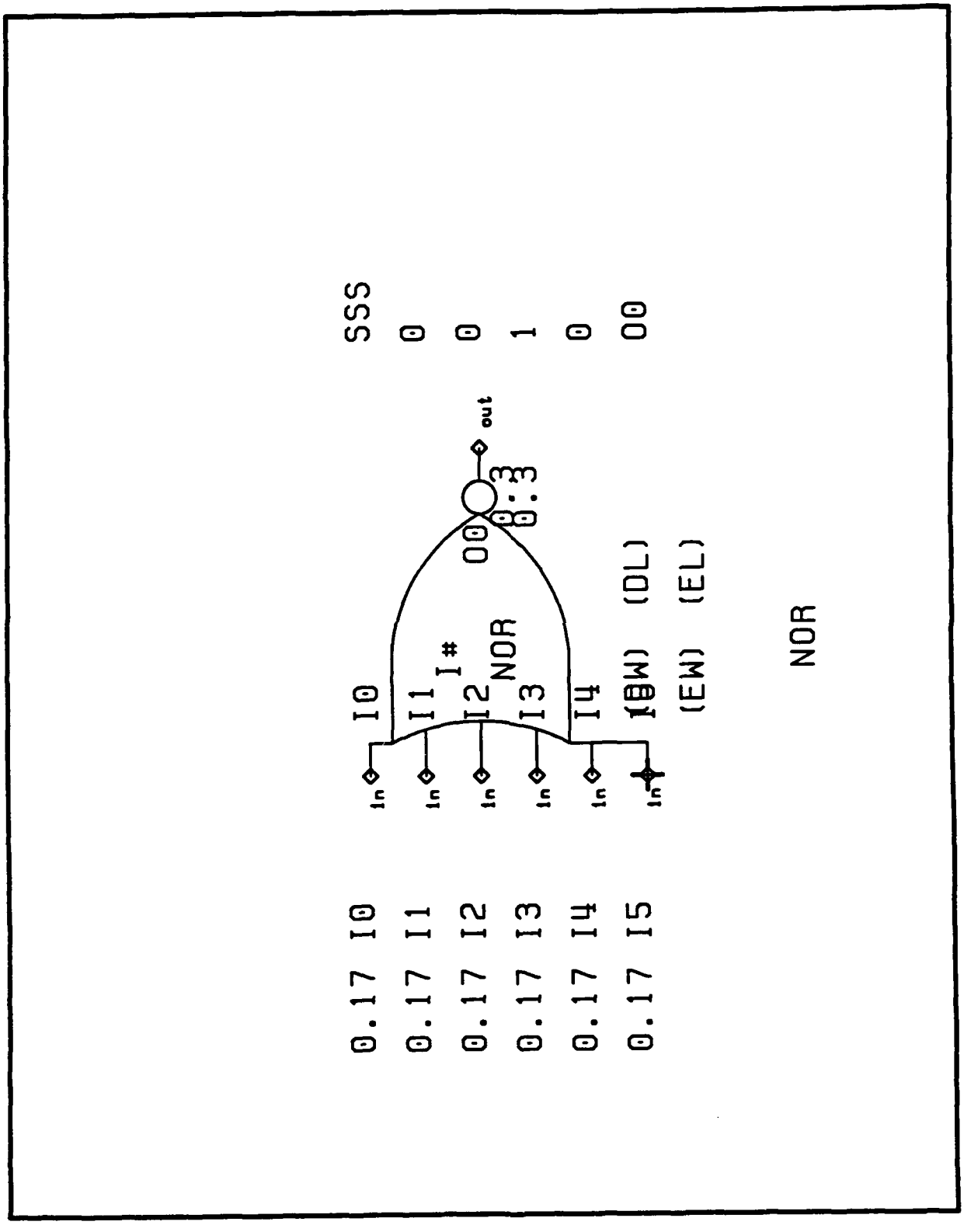

O0
(EW)
(EL)
I$26
I2
(DW)
(DL)
CG
(EW)
(EL)
VTT
I$1
I$2
(EW)
(EL)
I$3
I0
I1

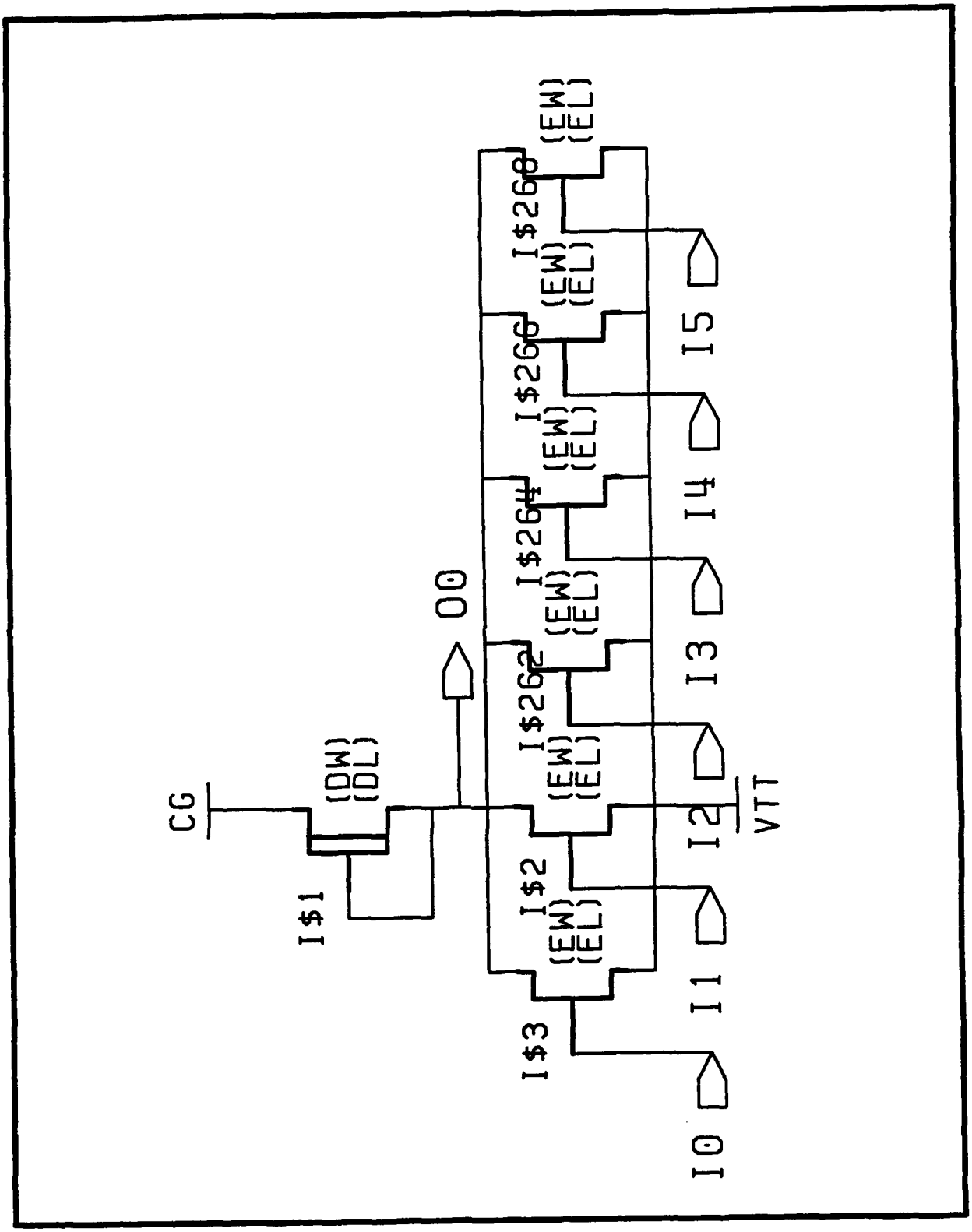

SSS
0
0
1
0
00
out
00
0.3
I0
I*
I1
NOR
I2
I3
(DW) (DL)
(EW) (EL)
NOR
In
In
In
In
0.17 I0
0.17 I1
0.17 I2
0.17 I3

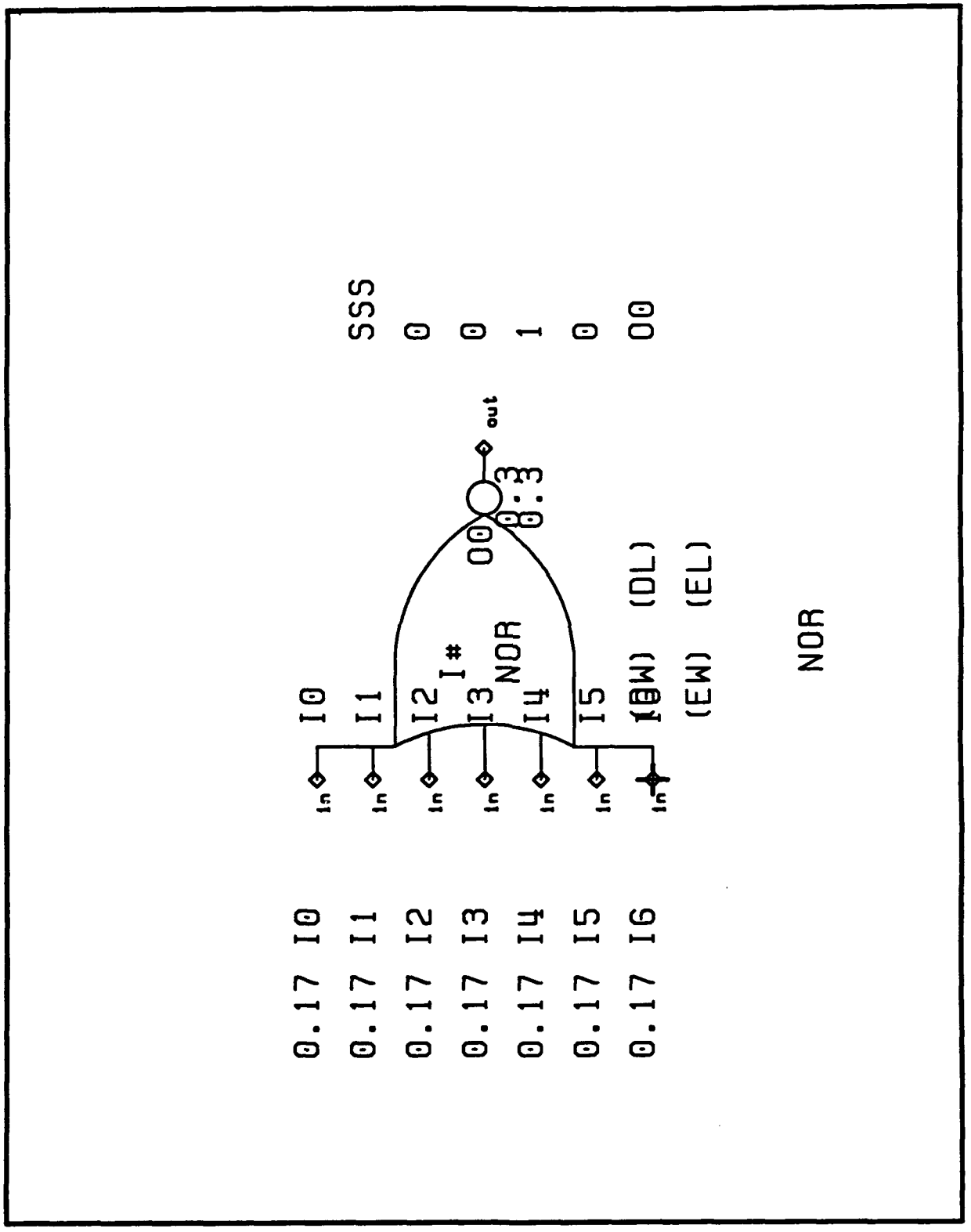

(EW)
(EL)
I$262
I3
(EW)
(EL)
O0
I$261
I2
(OW)
(OL)
(EW)
(EL)
CG
VTT
I$1
I$2
(EW)
(EL)
I$3
I0
I1

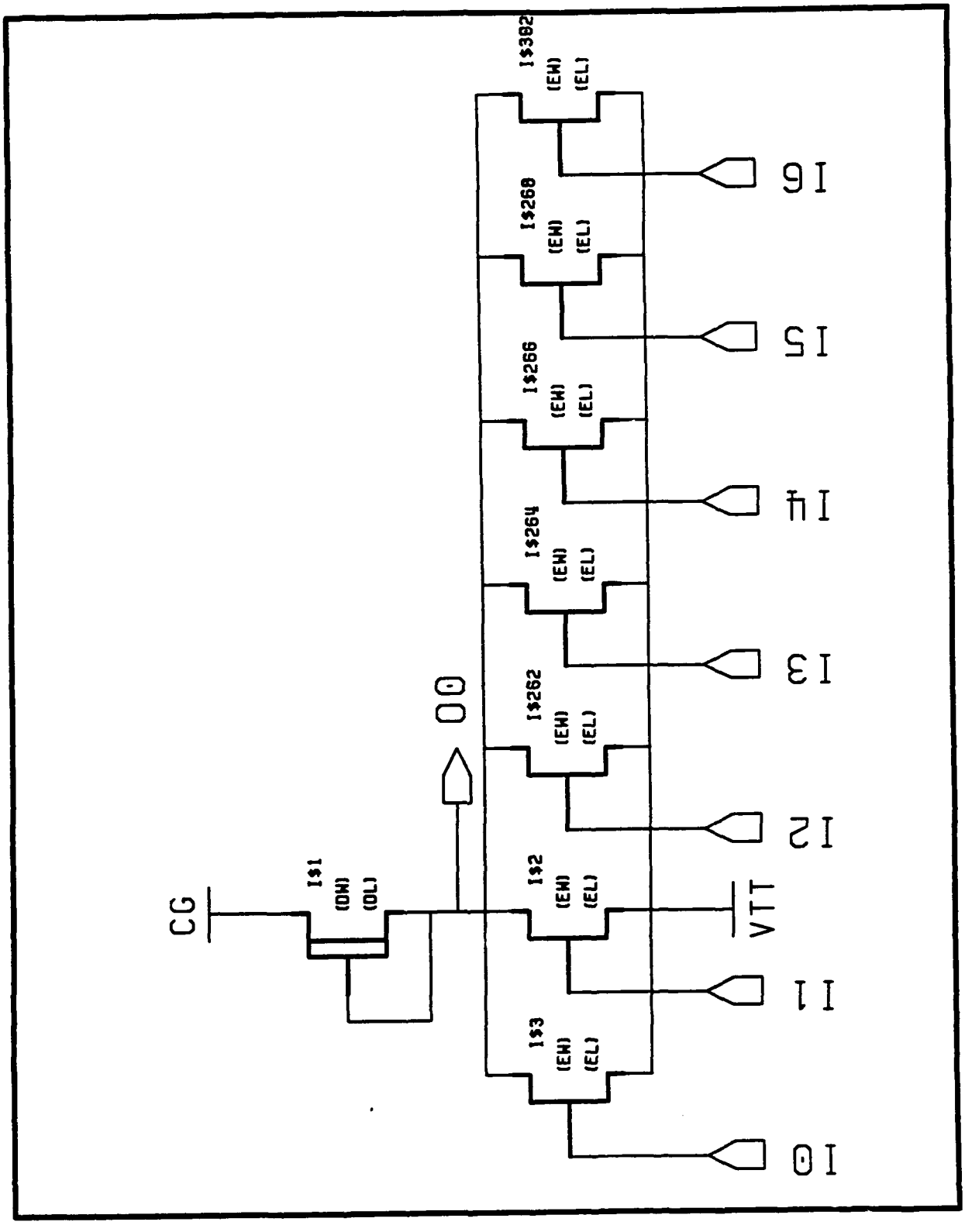

SSS
0
0
1
0
00
out
8:3
00
I#
NOR
I0
I1
I2
I3
I4
(DW) (DL)
(EW) (EL)
NOR
In
In
In
In
In
0.17 I0
0.17 I1
0.17 I2
0.17 I3
0.17 I4

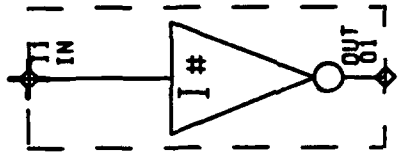

I$266
(EW)
(EL)
I4
I$264
(EW)
(EL)
I3
O0
I$262
(EW)
(EL)
I2
CG
(OW)
(OL)
I$1
I$2
(EW)
(EL)
VTT
I$3
(EW)
(EL)
I0
I1

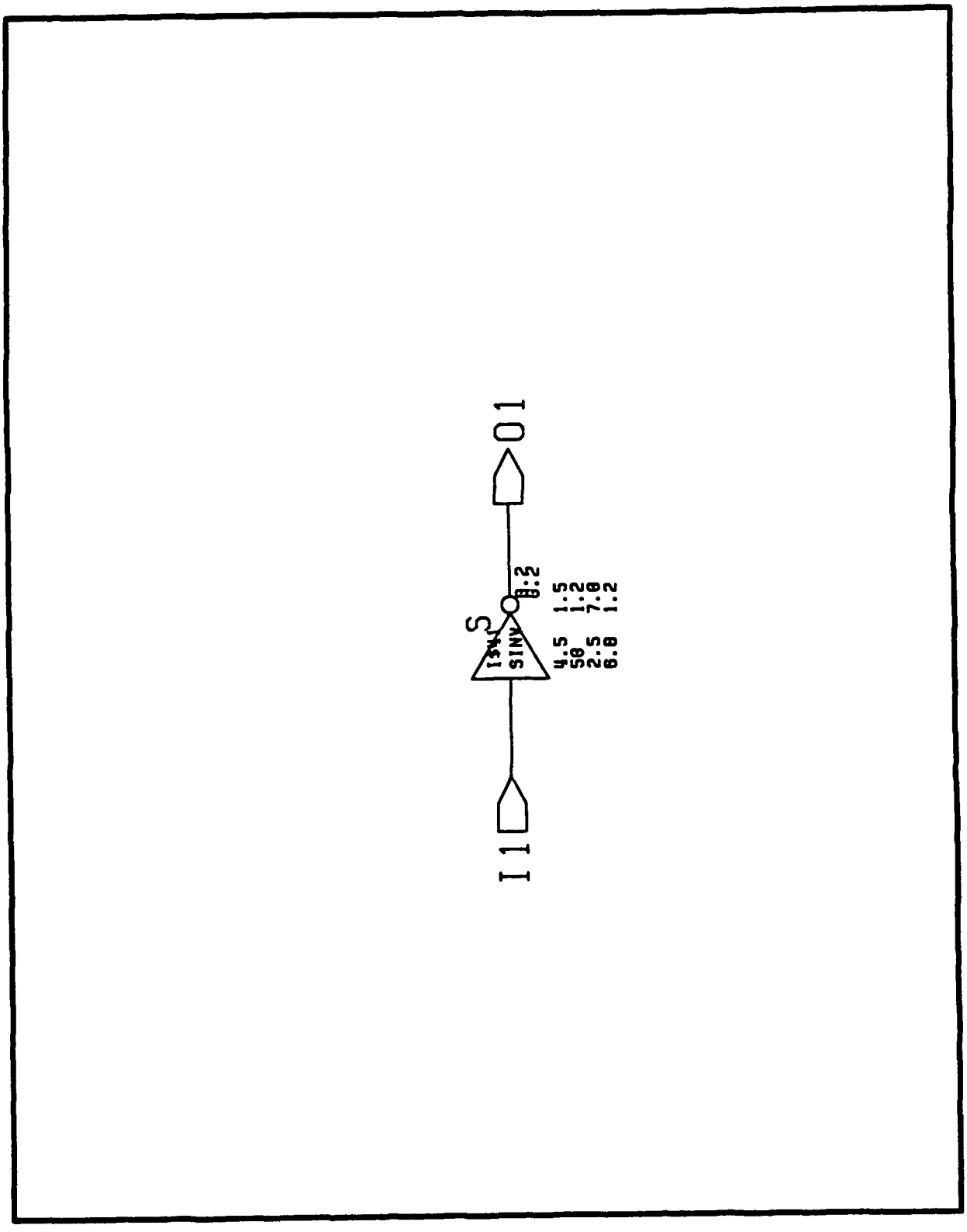

SSS
0
0
1
0
00
out
0.3
0.3
00
I#
NOR
I0
I1
I2
I3
I4
(DL)
(EL)
NOR
0.17 I0
0.17 I1
0.17 I2
0.17 I3
0.17 I4
0.17 I5

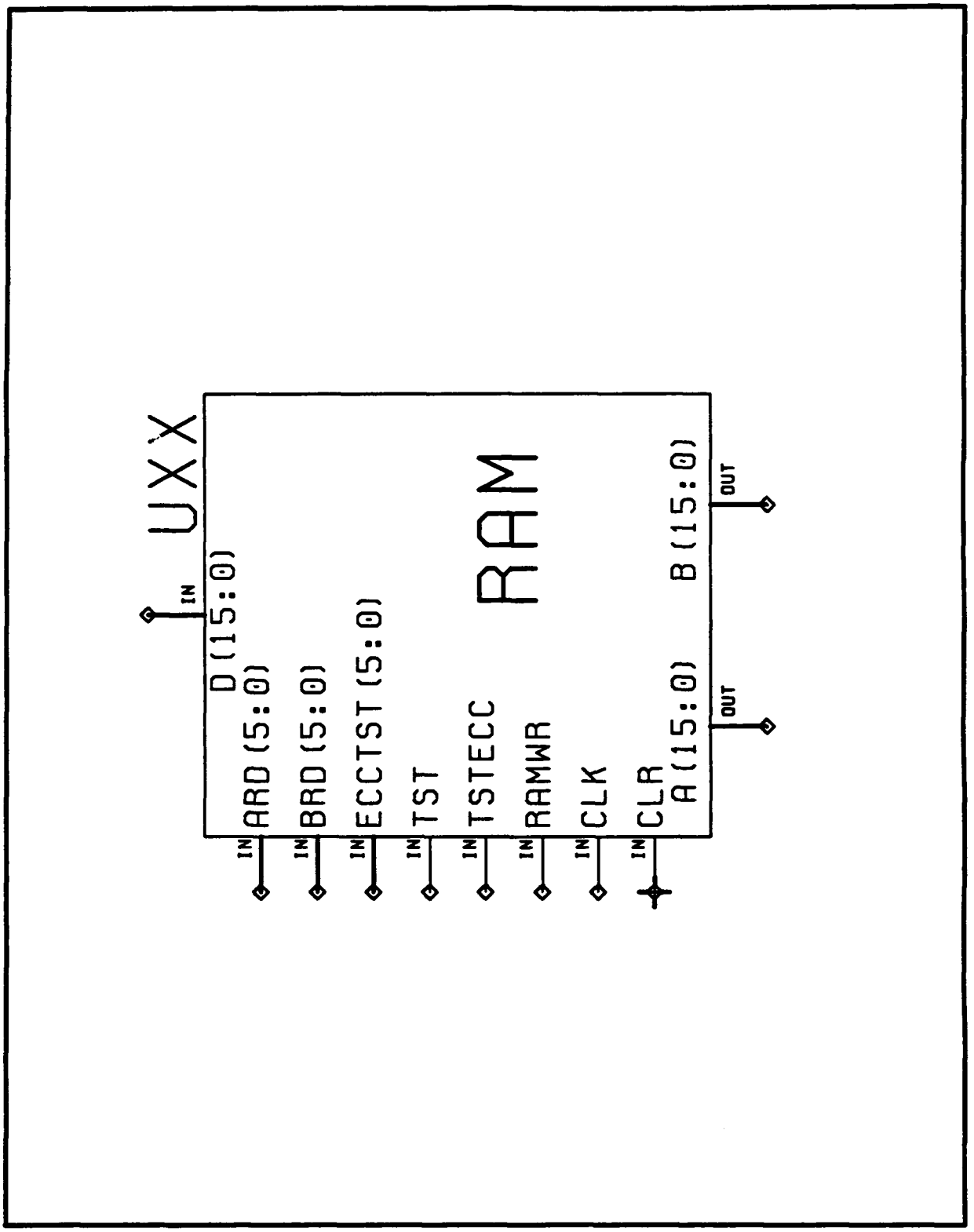

I$268
(EW)
(EL)
I$266
(EW)
(EL)
I$264
(EW)
(EL)
I$262
(EW)
(EL)
I$2
(EW)
(EL)
I$3
I5
I4
I3
I2
I1
I0
O0
VTT
CG
(DW)
(DL)
I$1

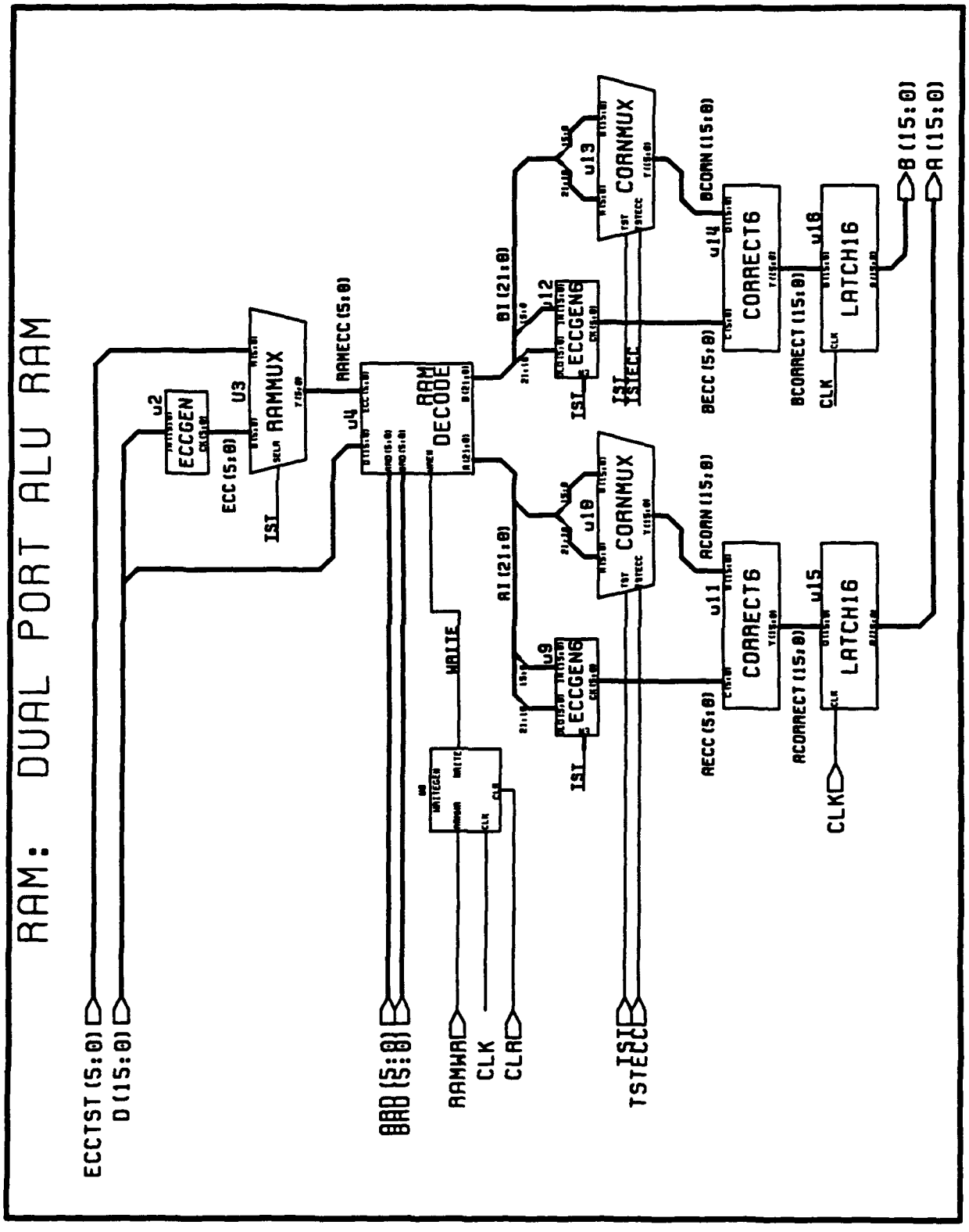

SSS
0
0
1
0
00
out
8:3
00
I#
NOR
I0
I1
I2
I3
I4
I5
(DL)
(EL)
NOR
0.17 I0
0.17 I1
0.17 I2
0.17 I3
0.17 I4
0.17 I5
0.17 I6

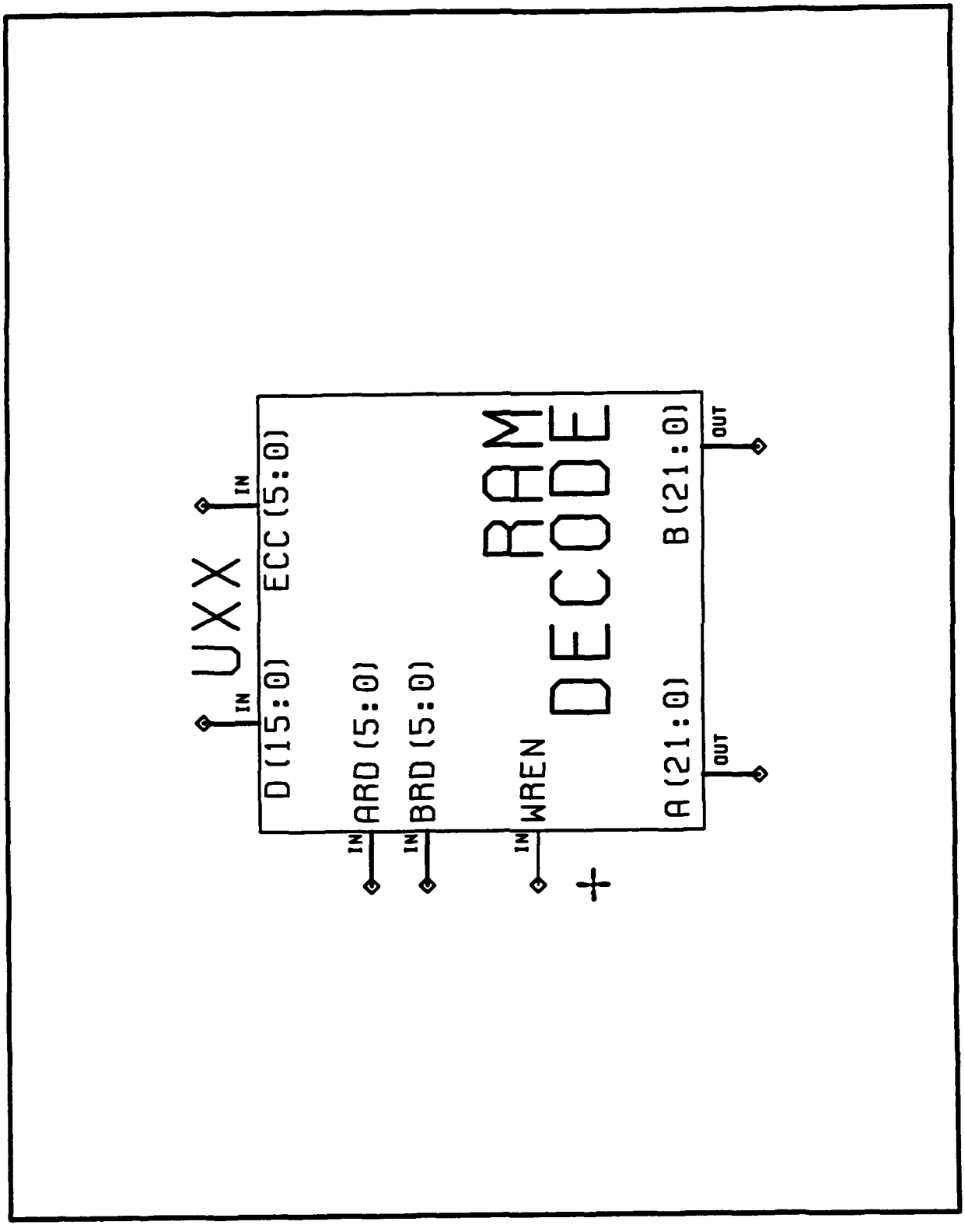

I$302
(EH)
(EL)
I6
I$268
(EH)
(EL)
I5
I$266
(EH)
(EL)
I4
I$264
(EH)
(EL)
I3
I$262
(EH)
(EL)
I2
O0
I$1
(DH)
(DL)
CG
I$2
(EH)
(EL)
VTT
I1
I$3
(EH)
(EL)
I0

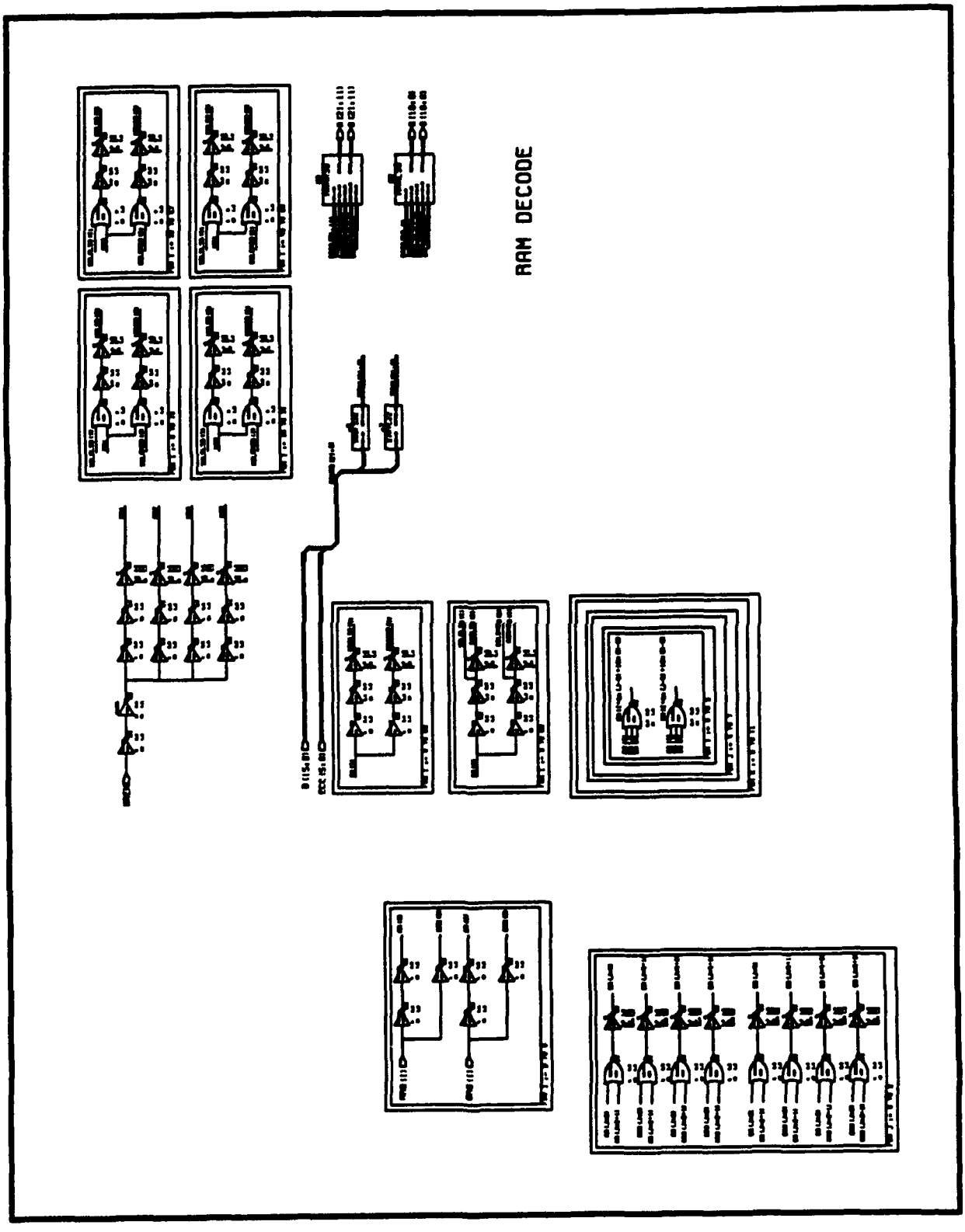

IN
I#
OUT

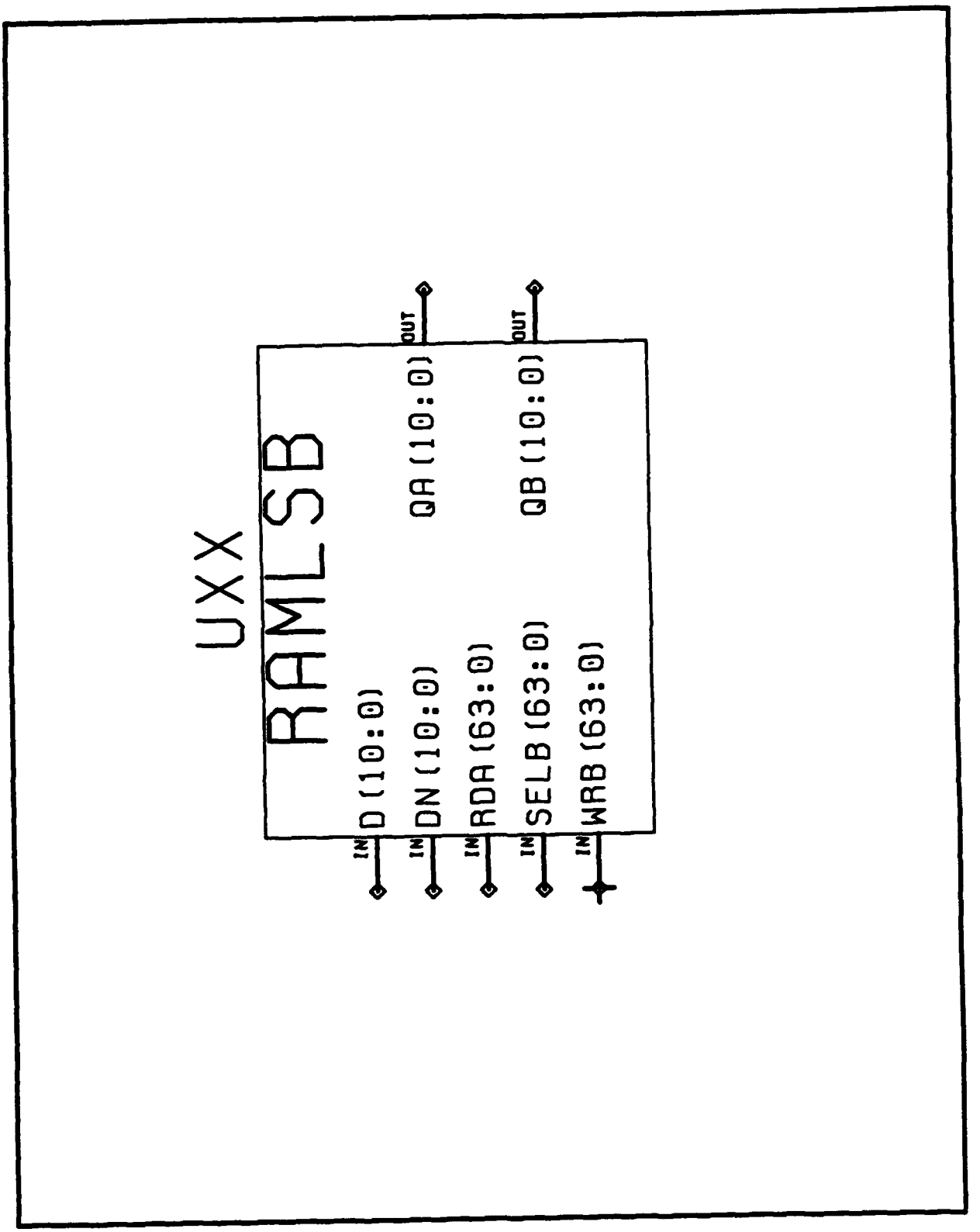

O1
8.2
1.5
1.2
7.0
1.2
S
I3L
SINV
4.5
50
2.5
6.0
I1

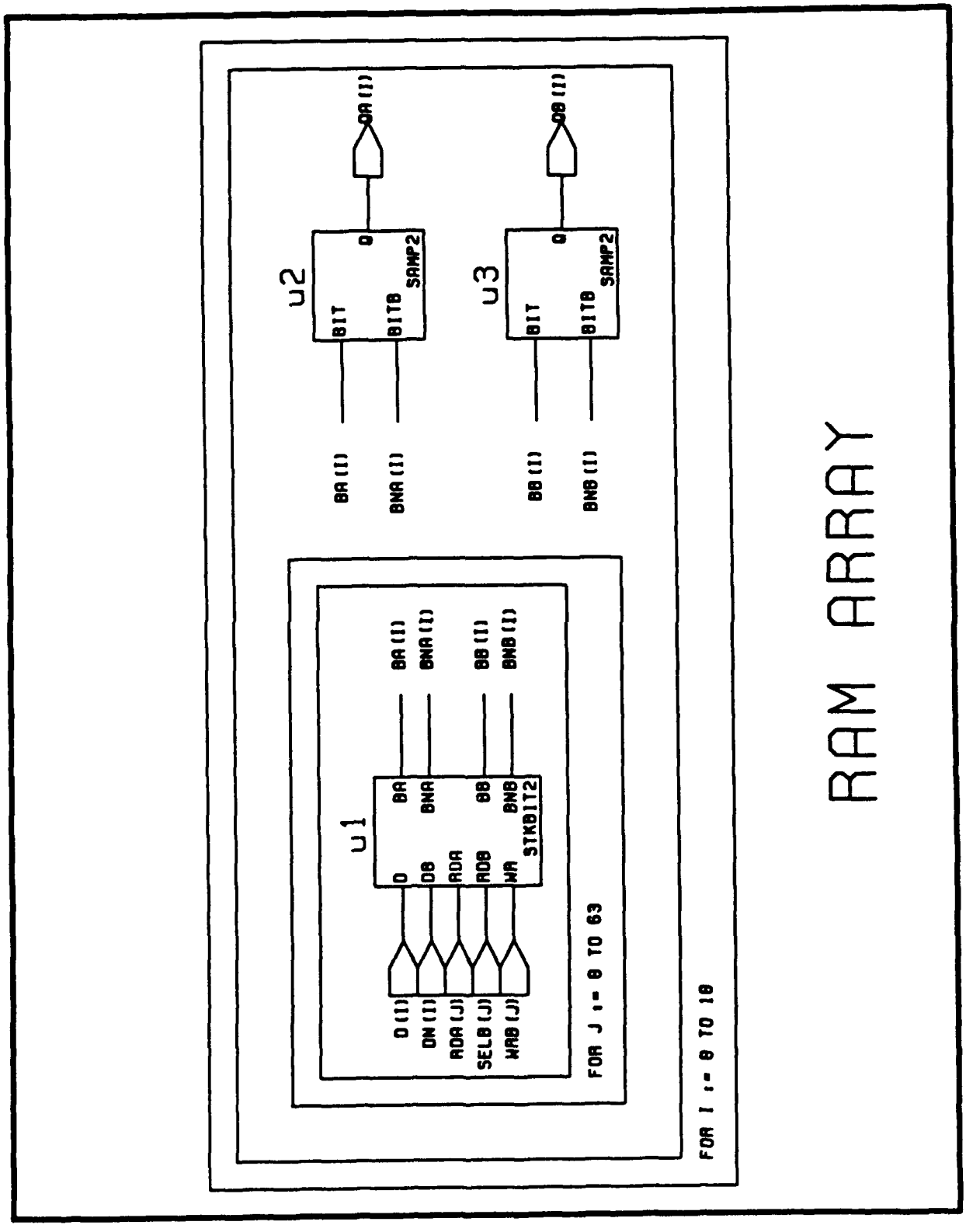

UXX
RAM
IN
D(15:0)
ARD(5:0)
BRD(5:0)
ECCTST(5:0)
TST
TSTECC
RAMWR
CLK
CLR
A(15:0)
B(15:0)
OUT
OUT

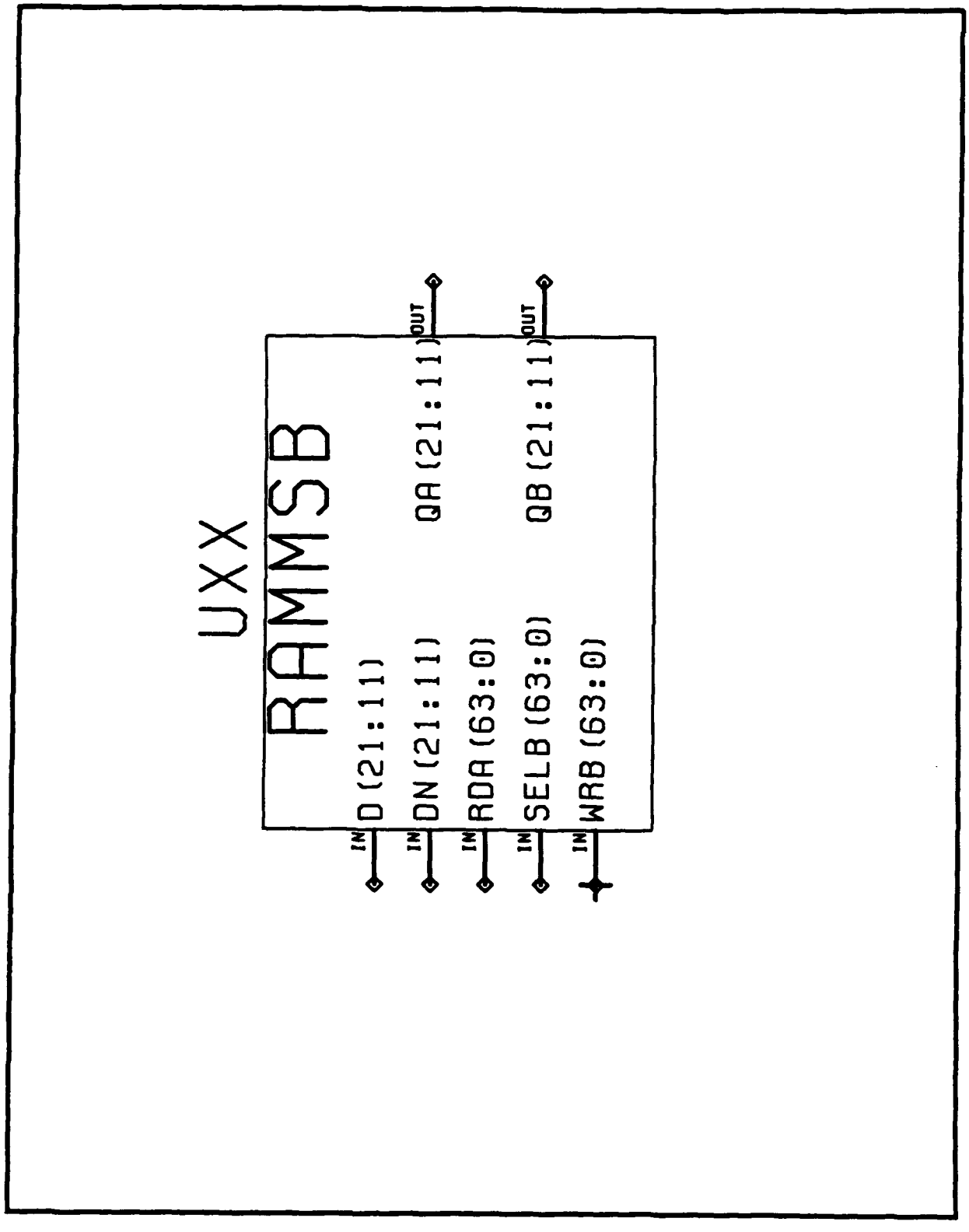

RAM: DUAL PORT ALU RAM
ECCTST (5:0)
D (15:0)
BAD (5:0)
RAMWR
CLK
CLR
TSTECC
ISI
CLK
u2
ECCGEN
ECC (5:0)
U3
RAMMUX
ISI
RAMECC (5:0)
u4
RAM DECODE
WRITE
A1 (21:0)
B1 (21:0)
u9
ECCGENG
u10
CORNMUX
u11
CORRECT6
ACORN (15:0)
AECC (5:0)
ACORRECT (15:0)
u15
LATCH16
A (15:0)
u12
ECCGENG
u13
CORNMUX
u14
CORRECT6
BCORN (15:0)
BECC (5:0)
BCORRECT (15:0)
u16
LATCH16
B (15:0)

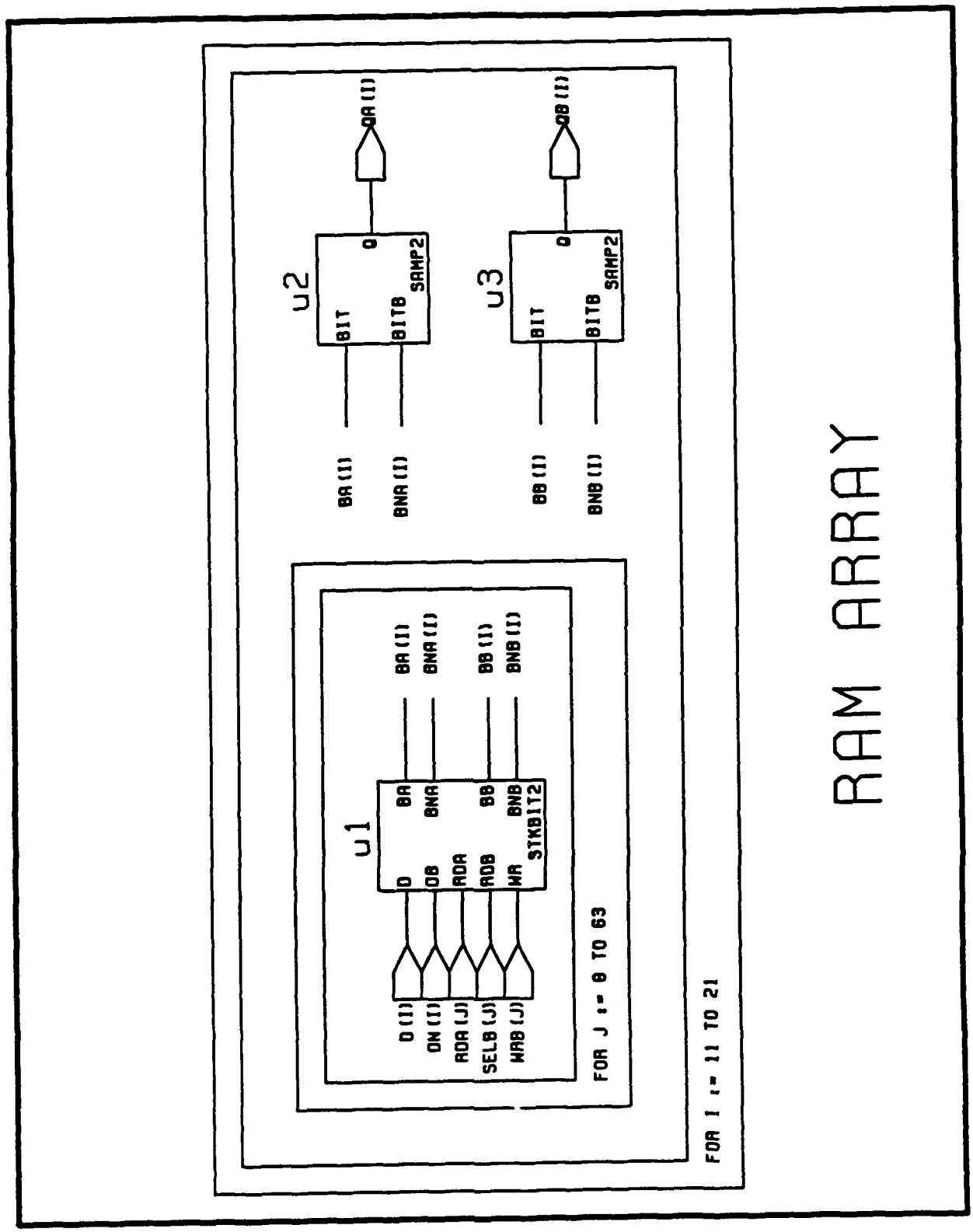

UXX
IN
D(15:0)
ECC(5:0)
RAM
DECODE
ARD(5:0)
BRD(5:0)
WREN
B(21:0)
A(21:0)
OUT
OUT
IN
IN
IN

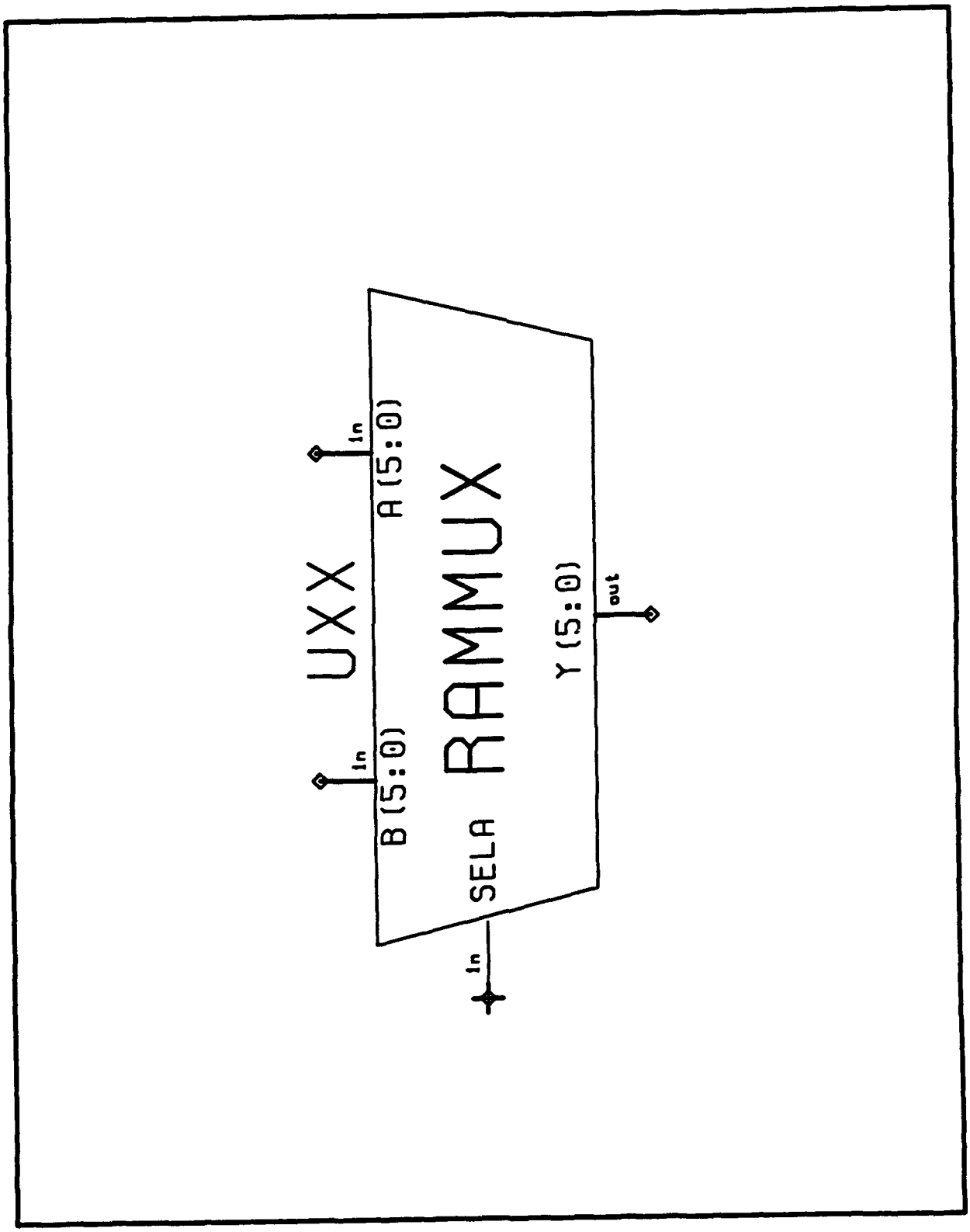

RAM DECODE

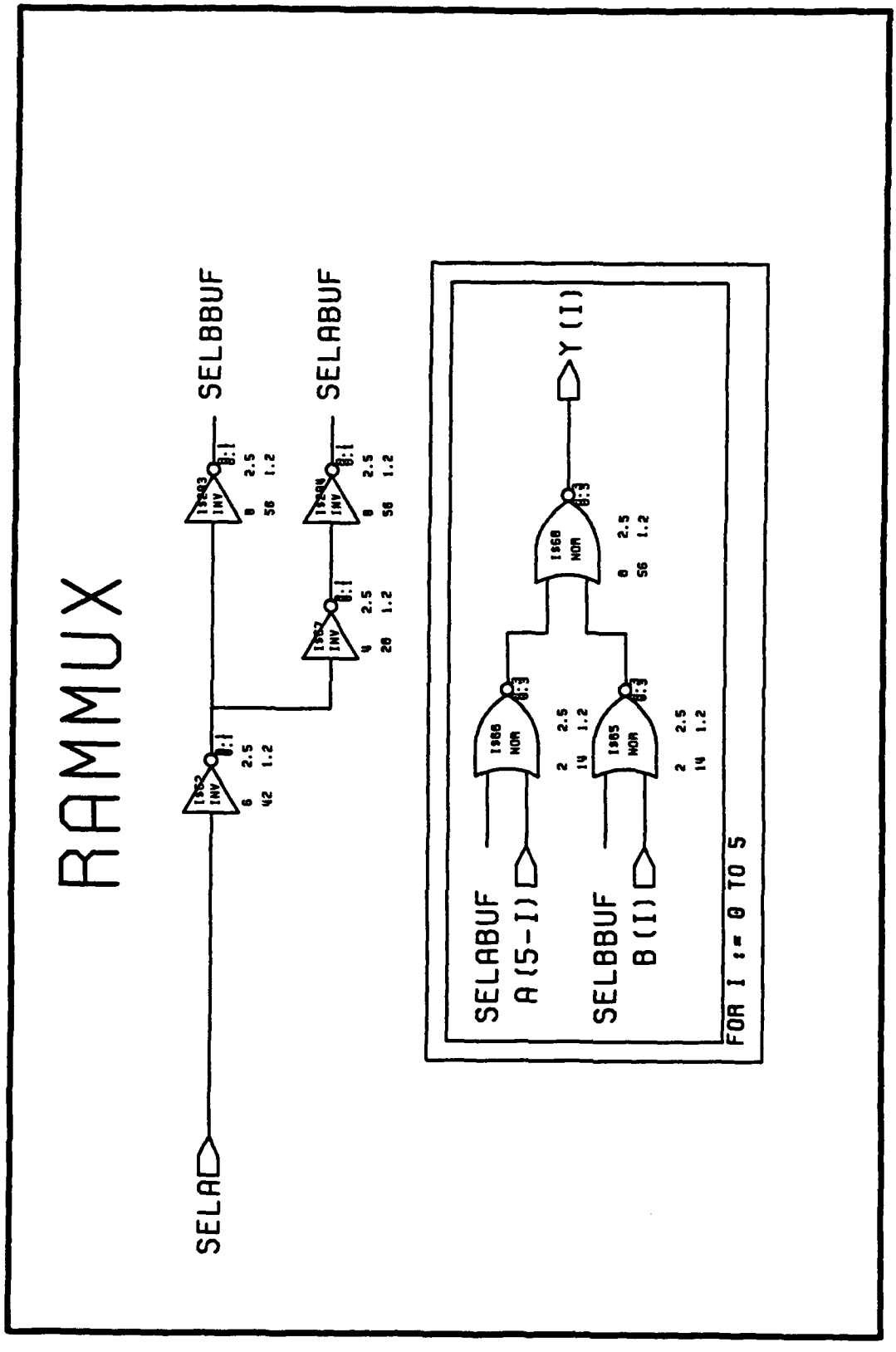

UXX
RAMLSB
D(10:0)
DN(10:0)
RDA(63:0)
SELB(63:0)
WRB(63:0)
QA(10:0)
QB(10:0)
IN
IN
IN
IN
IN
OUT
OUT

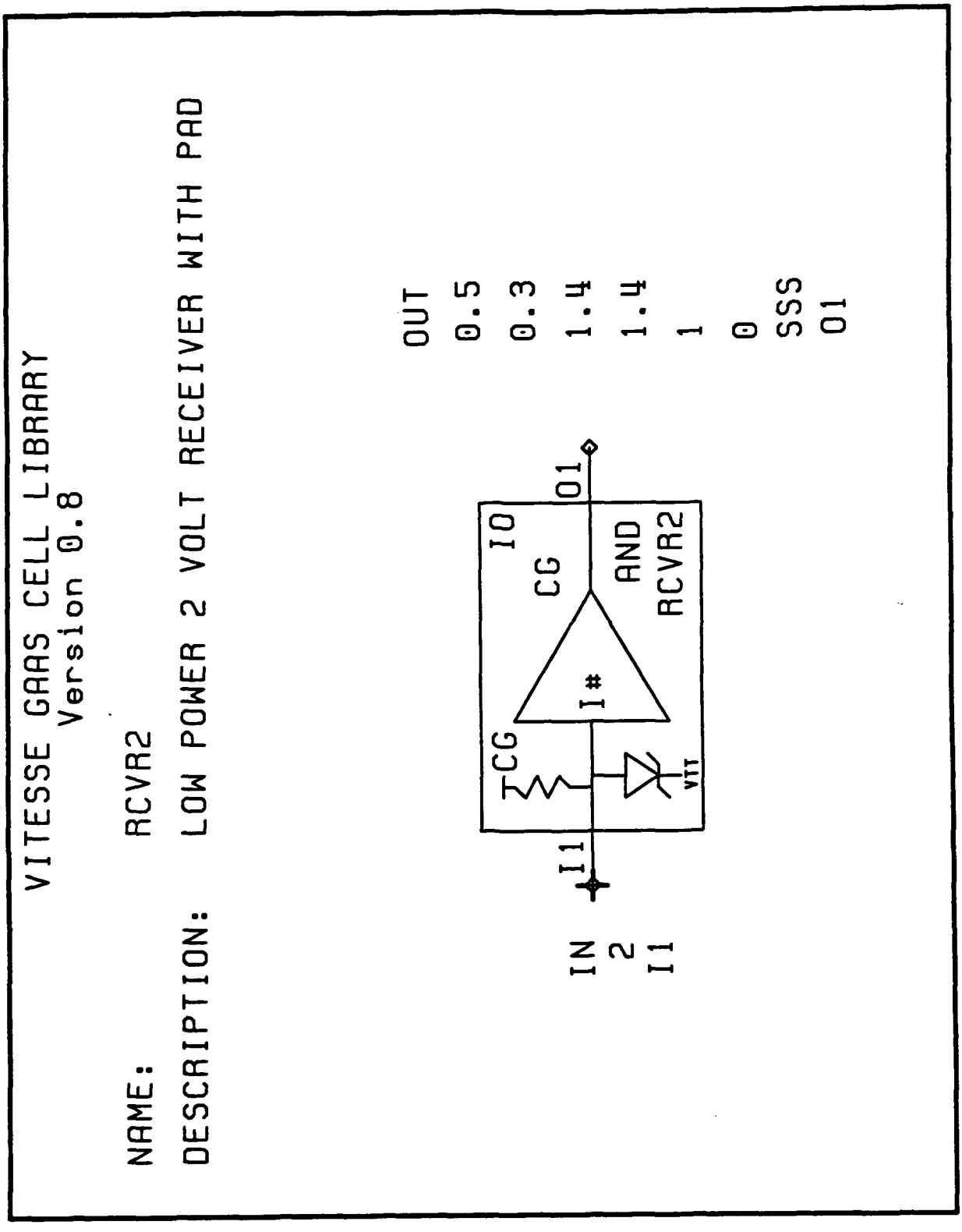

RAM ARRAY
FOR I := 0 TO 10
FOR J := 0 TO 63
u1
STKBIT2
BA
BNA
BB
BNB
D
DB
RDA
RDB
WA
u2
u3
SAMP2
BIT
BITB
Q
DA (I)
DB (I)
BA (I)
BNA (I)
BB (I)
BNB (I)
D (I)
DN (I)
RDA (J)
SELB (J)
WAB (J)

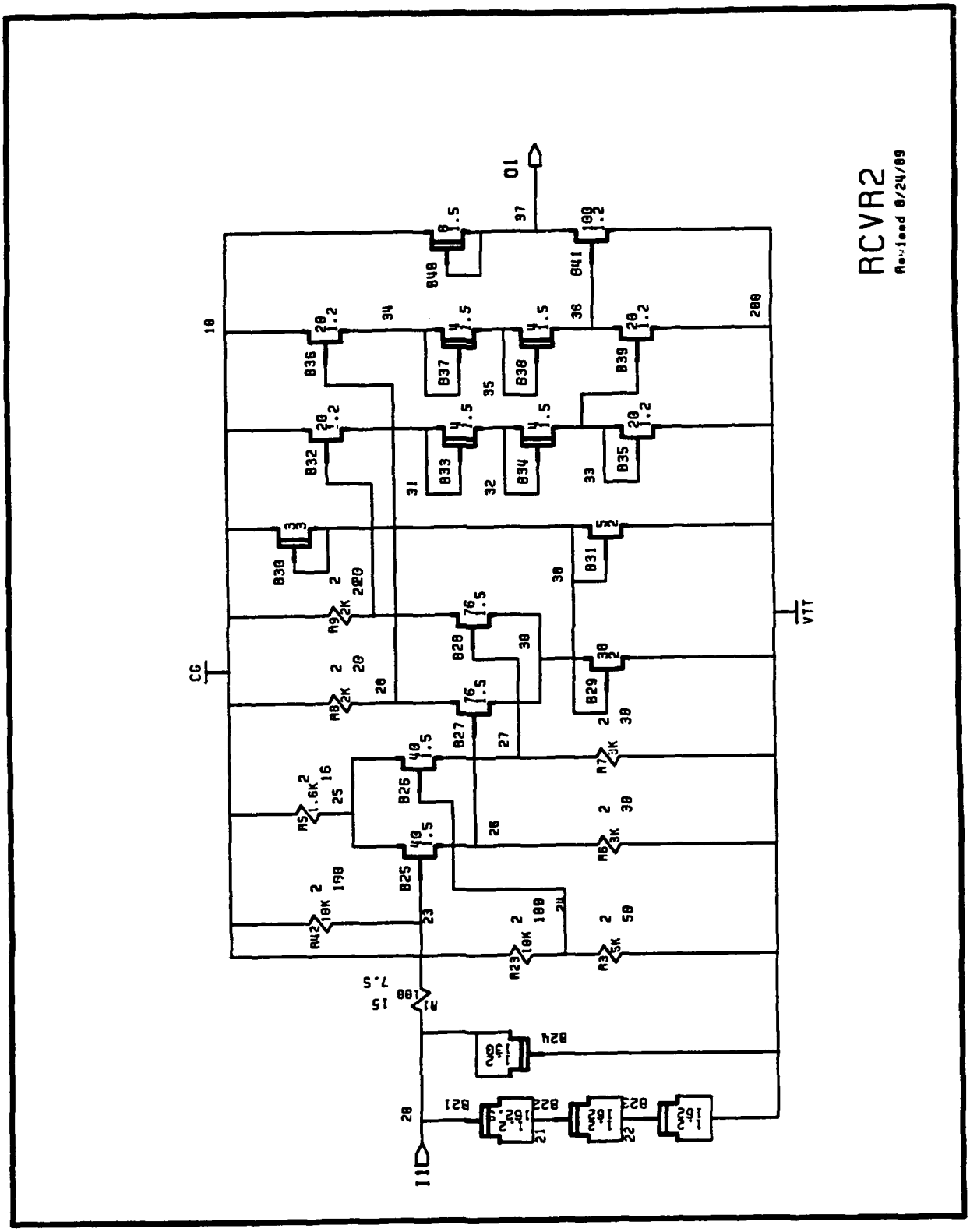

UXX
RAMSB
D(21:11)
DN(21:11)
RDA(63:0)
SELB(63:0)
WRB(63:0)
QA(21:11)
QB(21:11)
IN
IN
IN
IN
IN
OUT
OUT

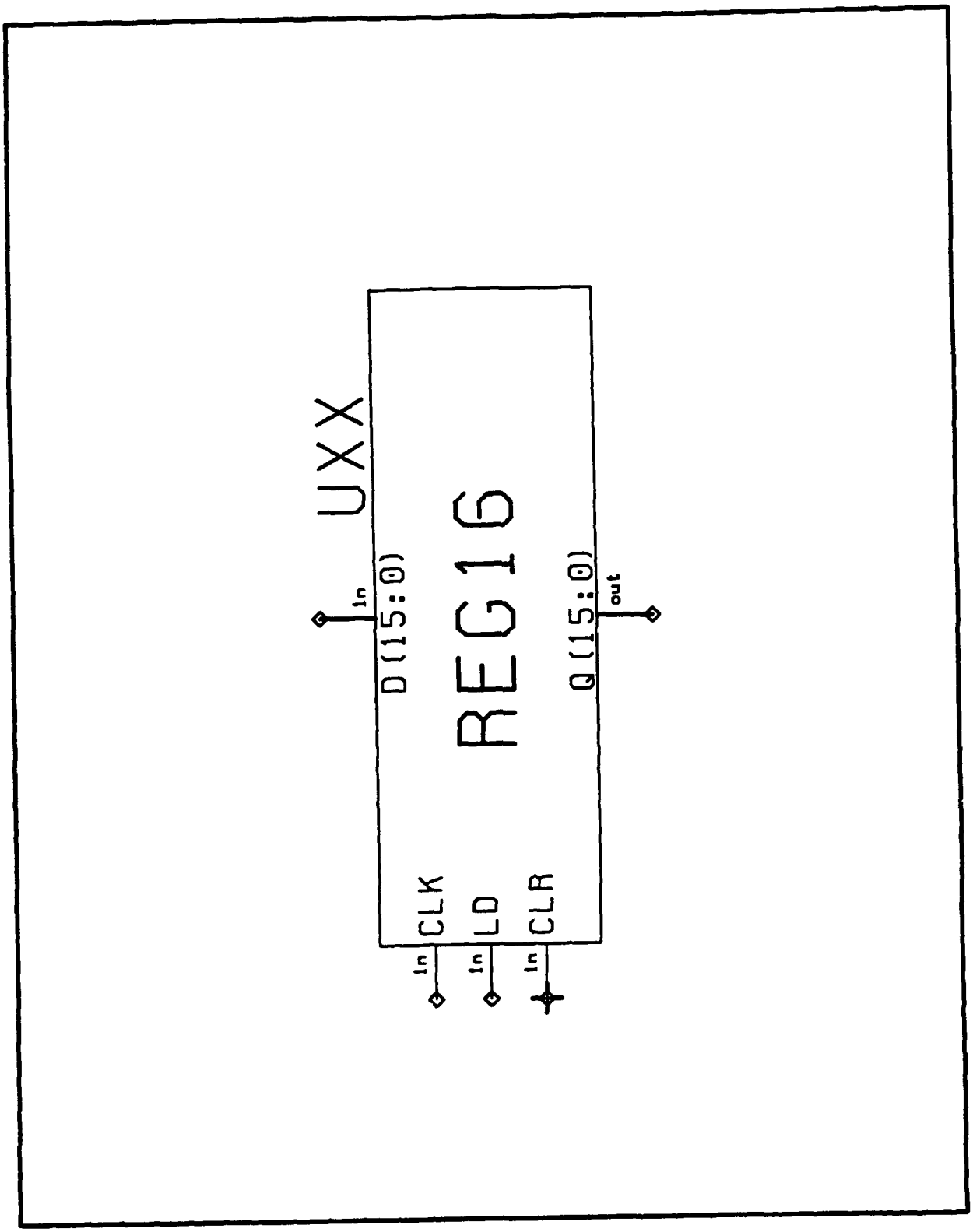

RAM ARRAY
FOR I := 11 TO 21
FOR J := 0 TO 63
u1
STKB1T2
D
OB
RDA
RDB
WR
BA
BNA
BB
BNB
D (I)
ON (I)
RDA (J)
SELB (J)
WAB (J)
BA (I)
BNA (I)
BB (I)
BNB (I)
u2
u3
BIT
BITB
SAMP2
OA (I)
OB (I)

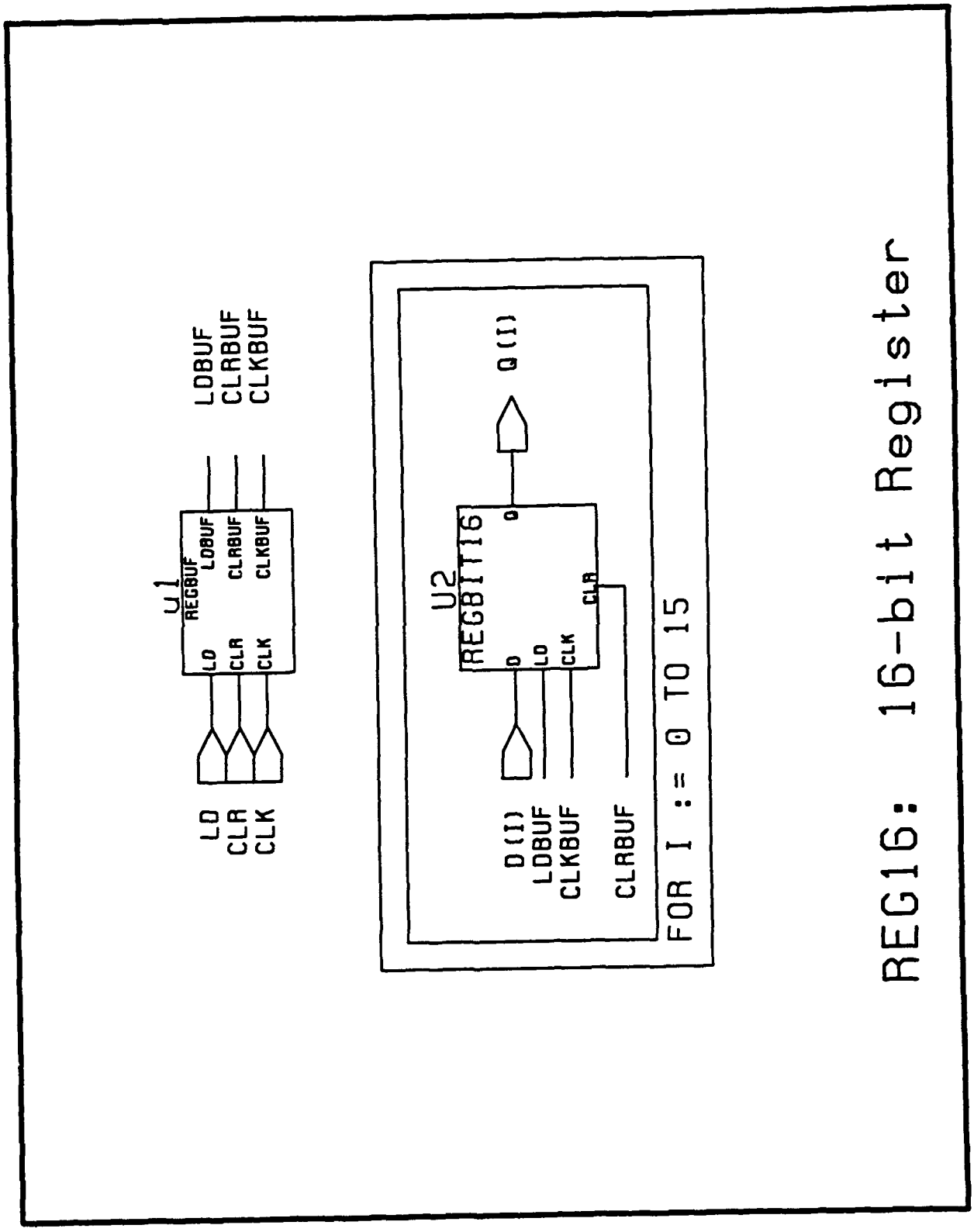

UXX
RAMUX
In
A(5:0)
In
B(5:0)
SELA
In
Y(5:0)
out

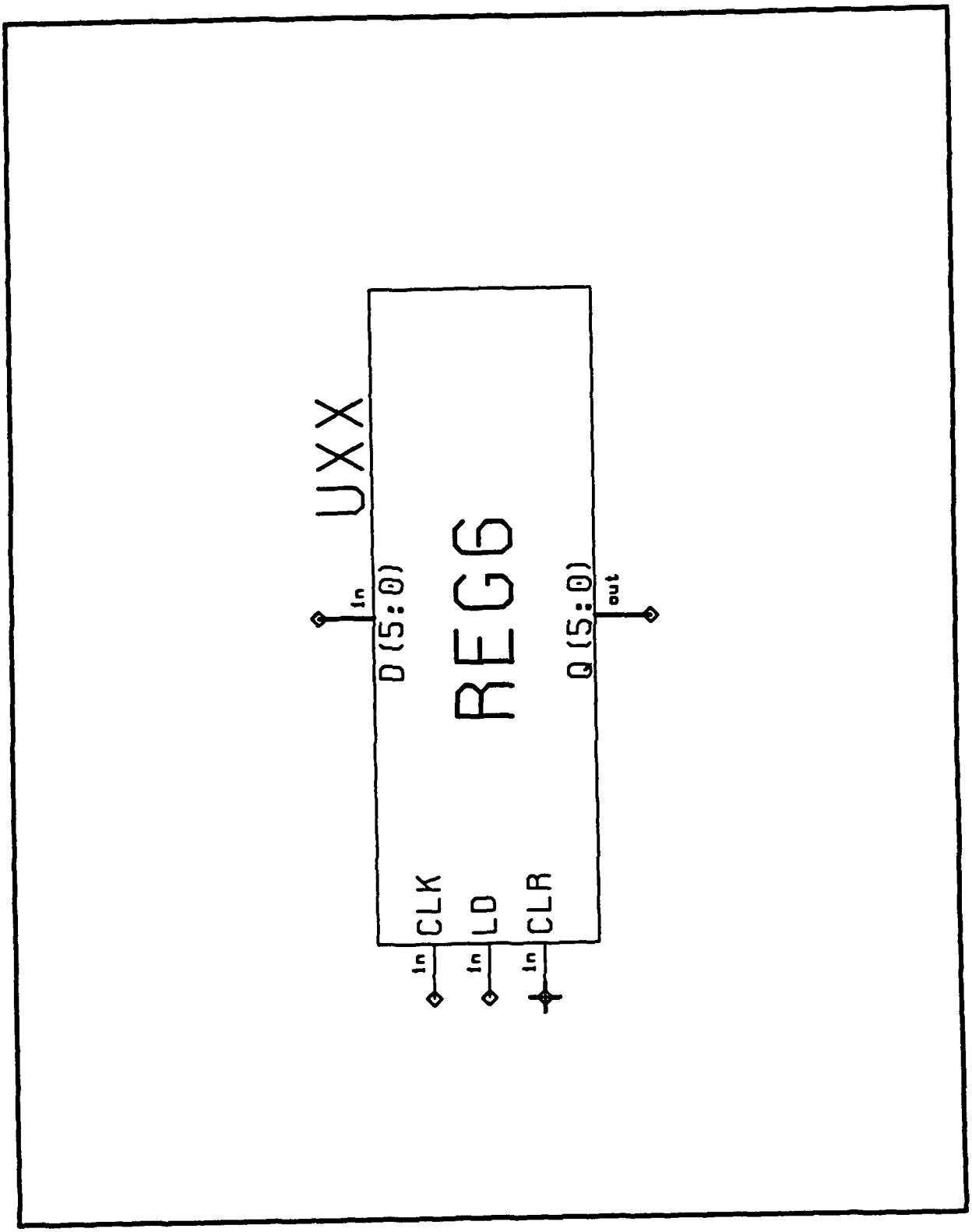

RAMUX
SELBBUF
SELABUF
SELA
Y(I)
SELABUF
A(5-I)
SELBBUF
B(I)
FOR I := 0 TO 5

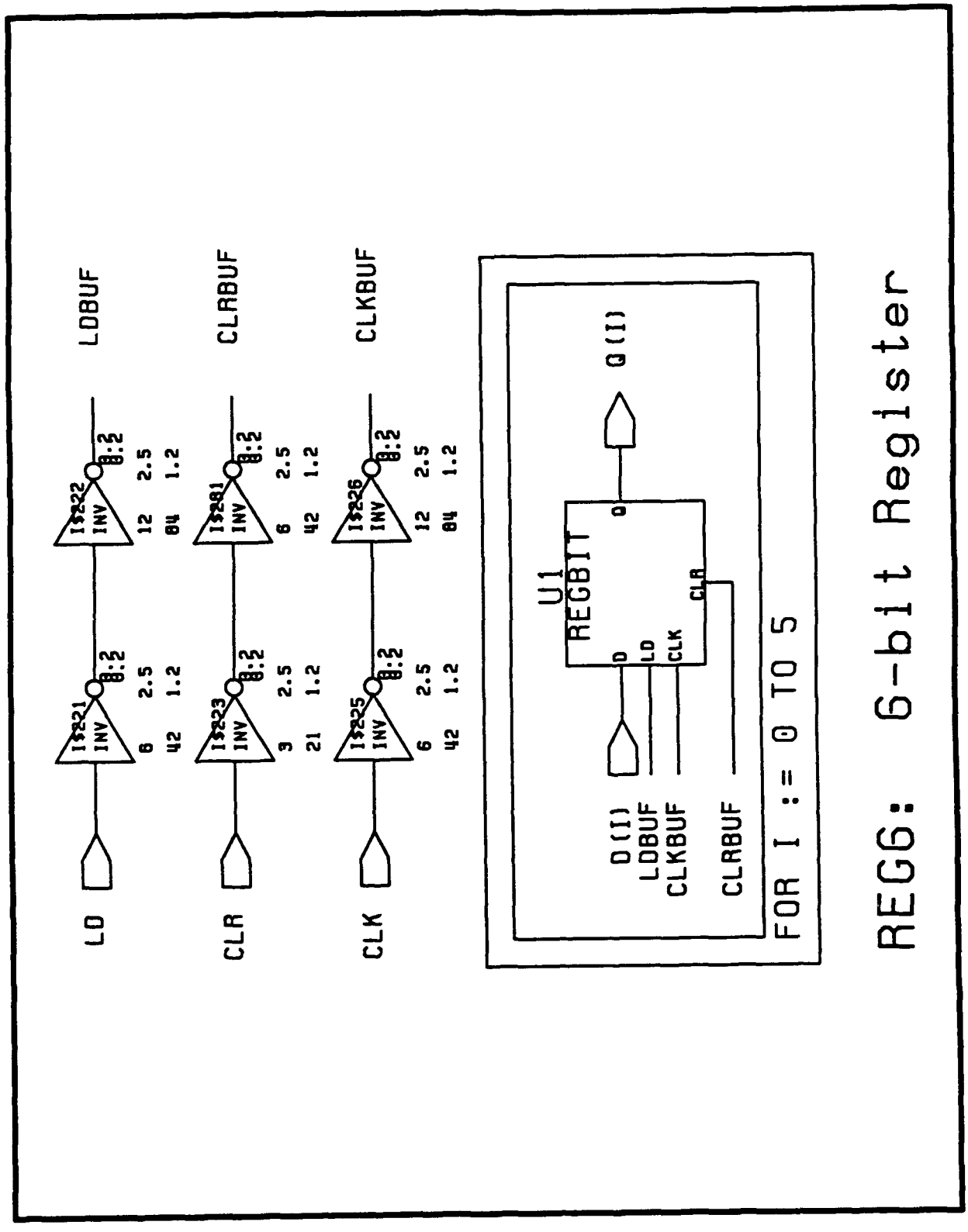

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: RCVR2
DESCRIPTION: LOW POWER 2 VOLT RECEIVER WITH PAD
OUT
0.5
0.3
1.4
1.4
1
0
SSS
01
IO
CG
AND
RCVR2
I#
O1
I1
CG
VTT
IN
2
I1

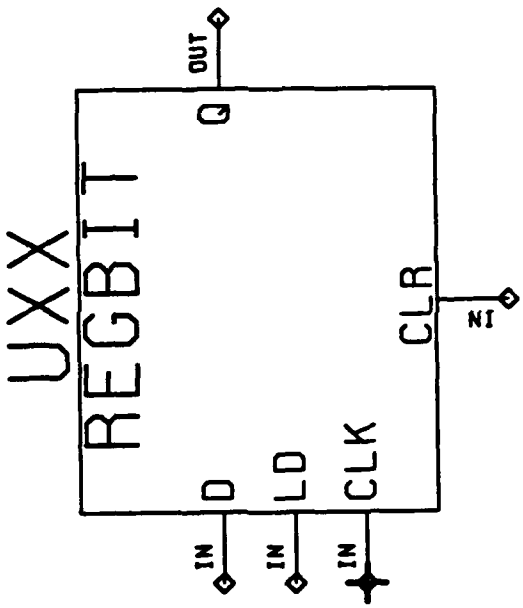

RCVR2
Revised 6/24/89
O1
I1
CG
VTT

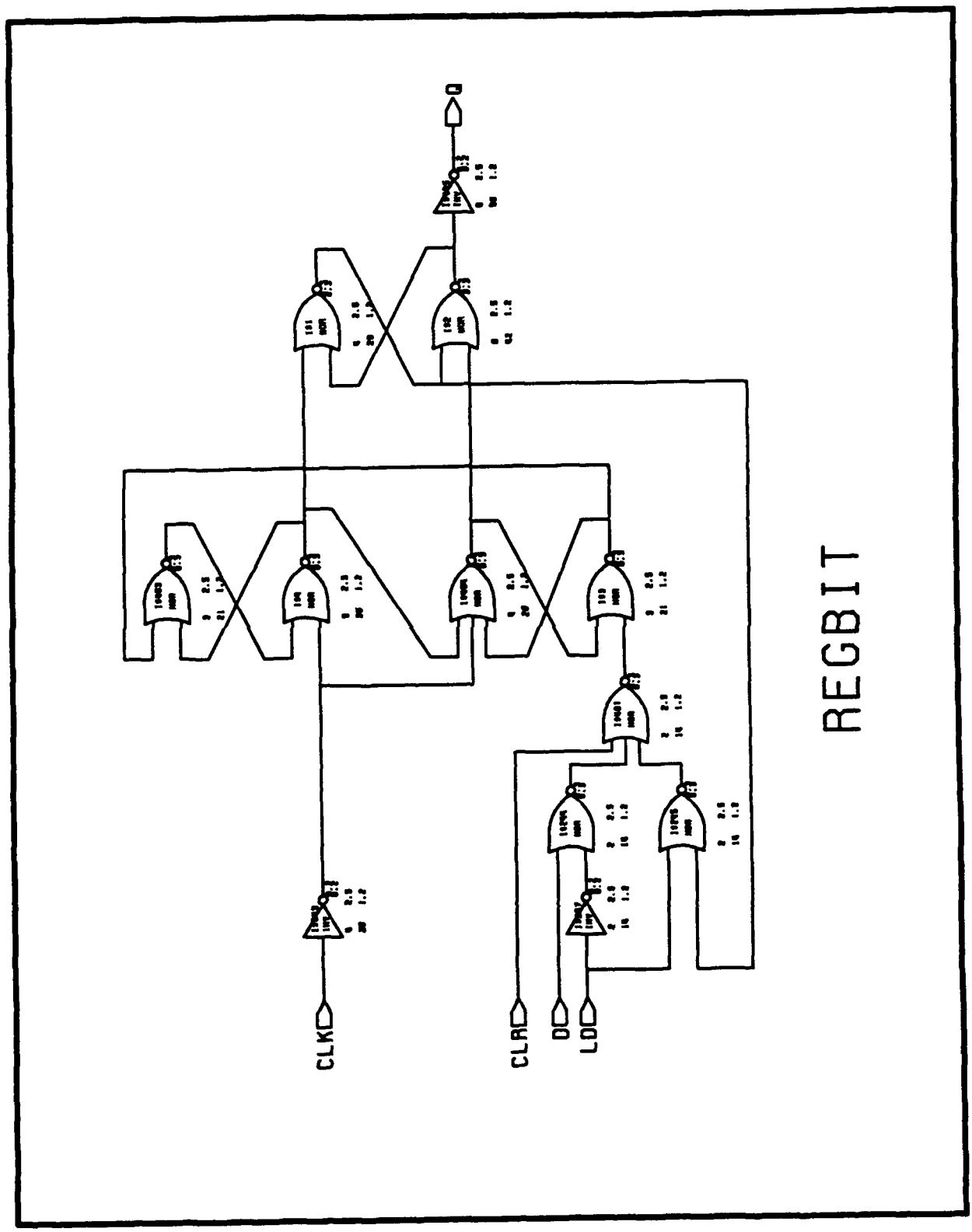

UXX
REG16
D(15:0)
Q(15:0)
In
out
CLK
LD
CLR
In
In
In

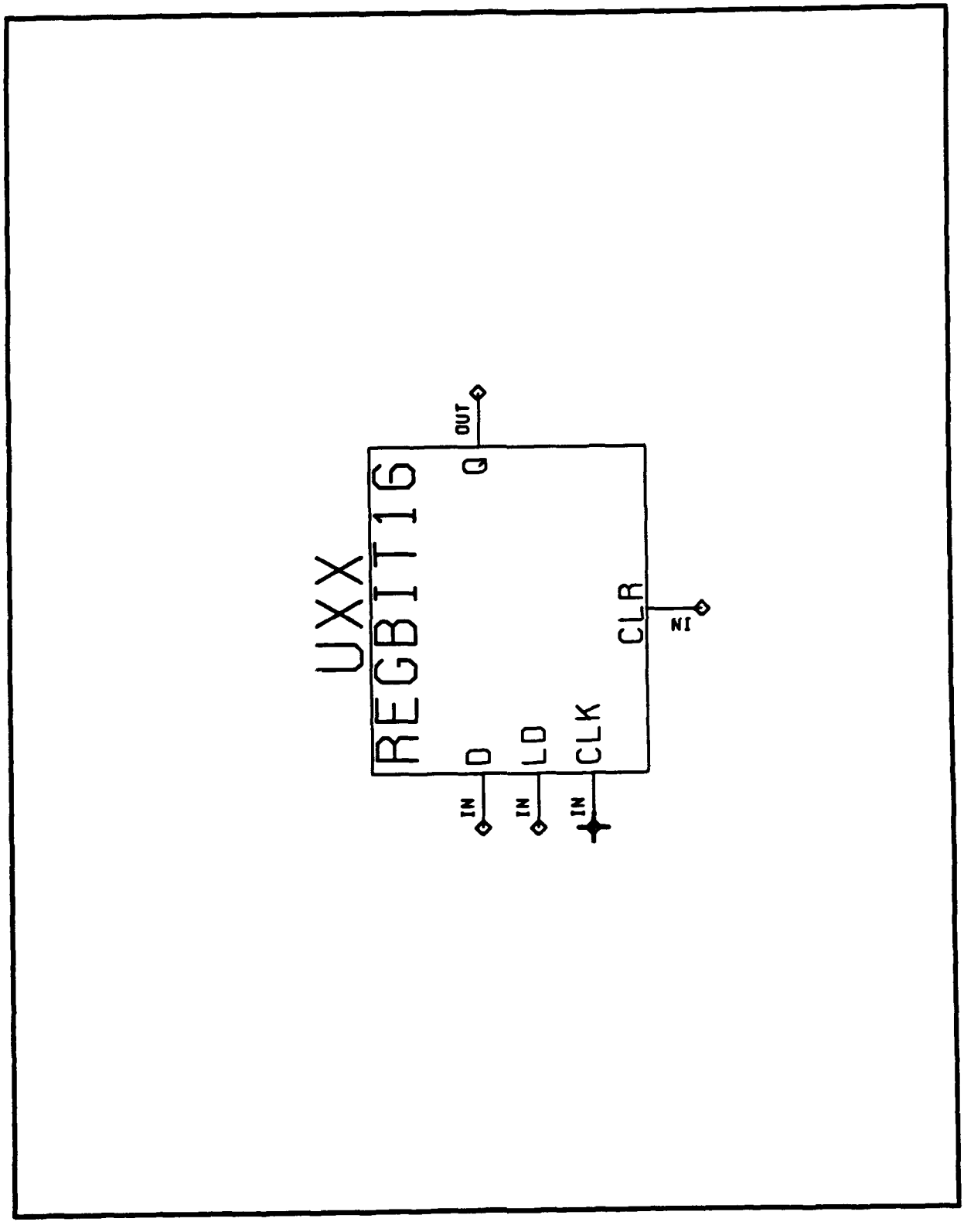

REG16: 16-bit Register
FOR I := 0 TO 15
U2
REGBIT16
Q(I)
D
LD
CLR
D(I)
LDBUF
CLKBUF
CLRBUF
U1
REGBUF
LDBUF
CLRBUF
CLKBUF
LD
CLR
CLK

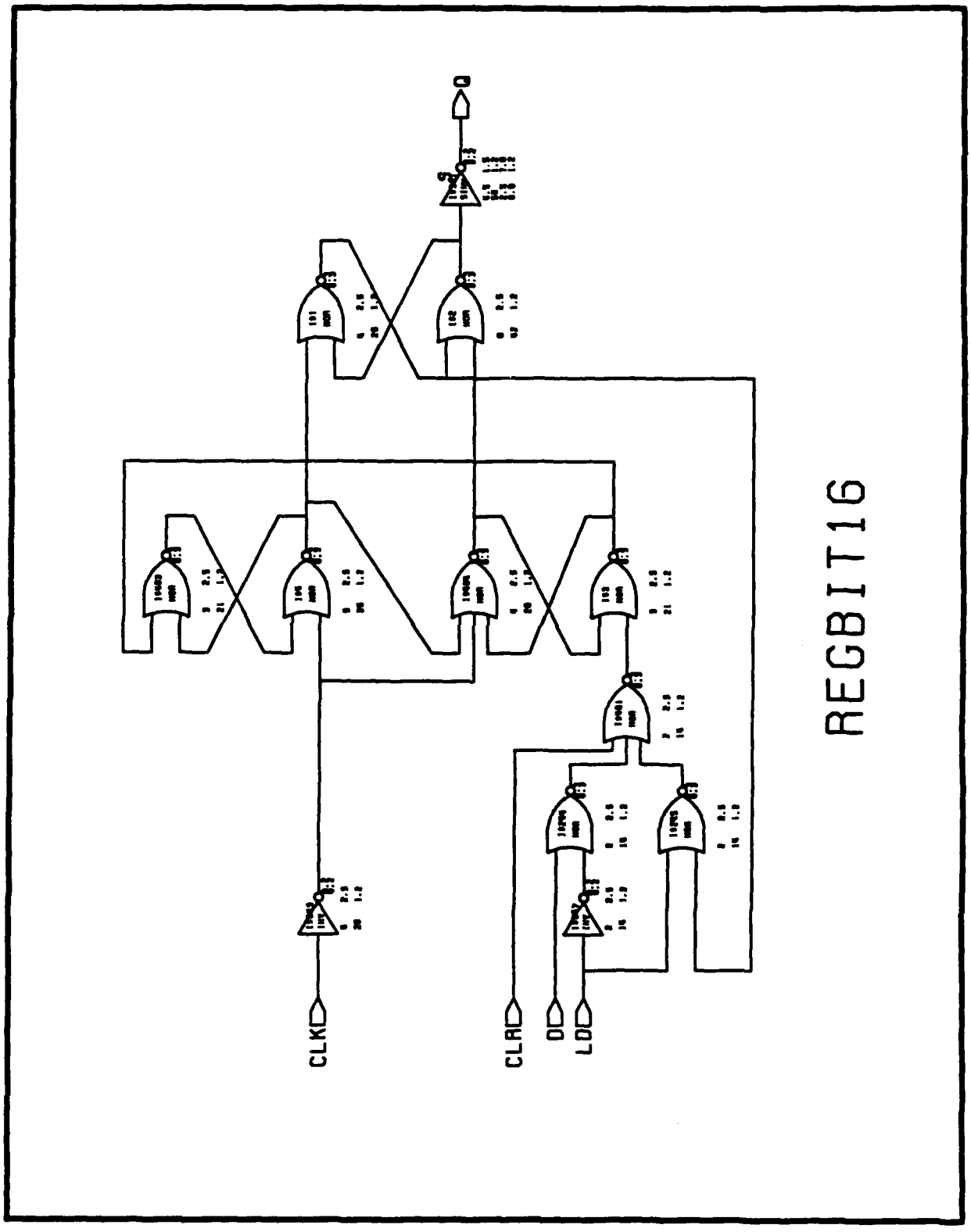

UXX
REG6
D(5:0)
Q(5:0)
in
out
CLK
LD
CLR
in
in
in

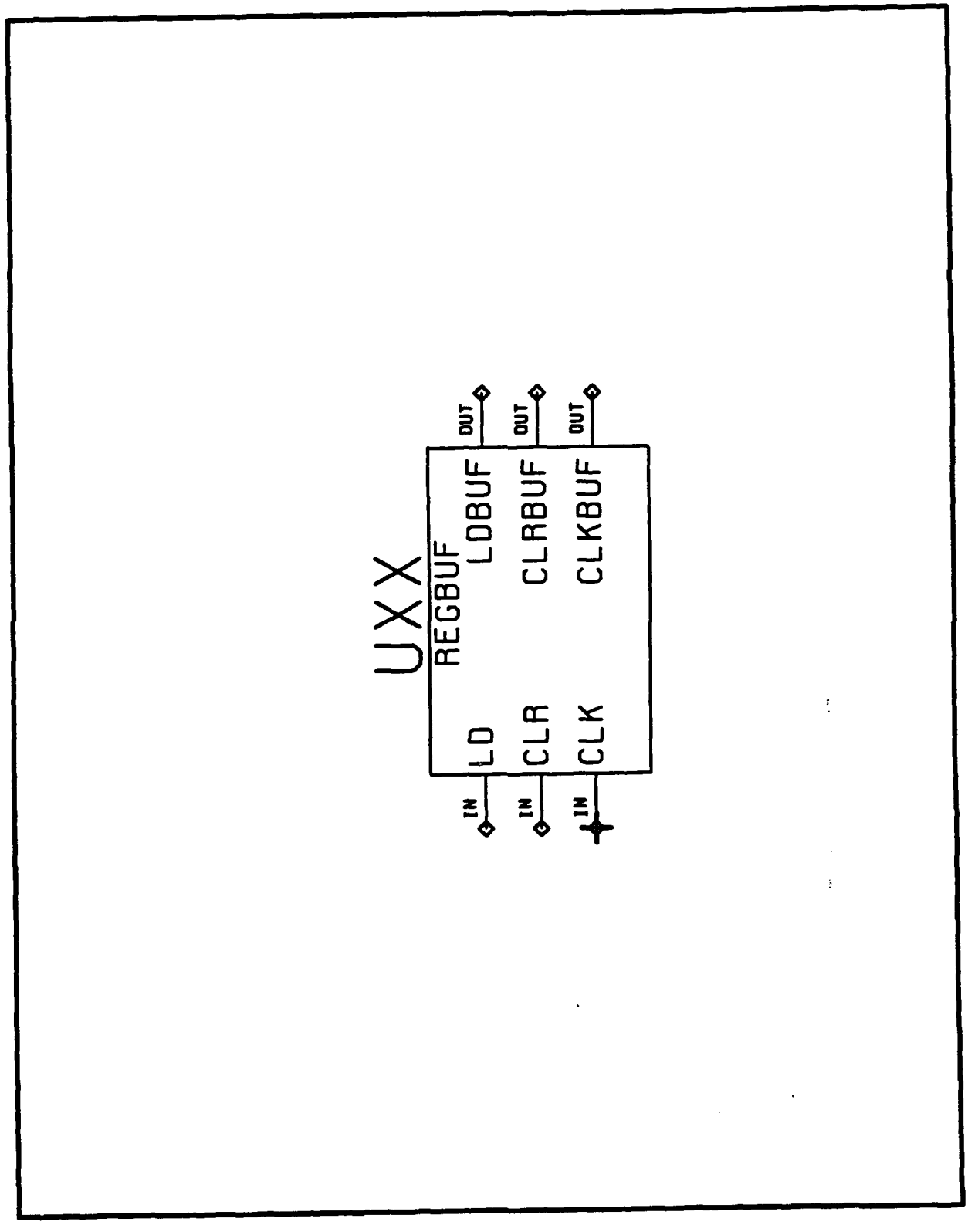

REG6: 6-bit Register
FOR I := 0 TO 5
U1
REGBIT
D
LD
CLK
CLR
Q(I)
D(I)
LDBUF
CLKBUF
CLRBUF
LDBUF
CLRBUF
CLKBUF
LD
CLR
CLK
I$221
I$222
I$223
I$225
I$226
I$281
INV
8:2
2.5
1.2
6
12
3
21
42
84

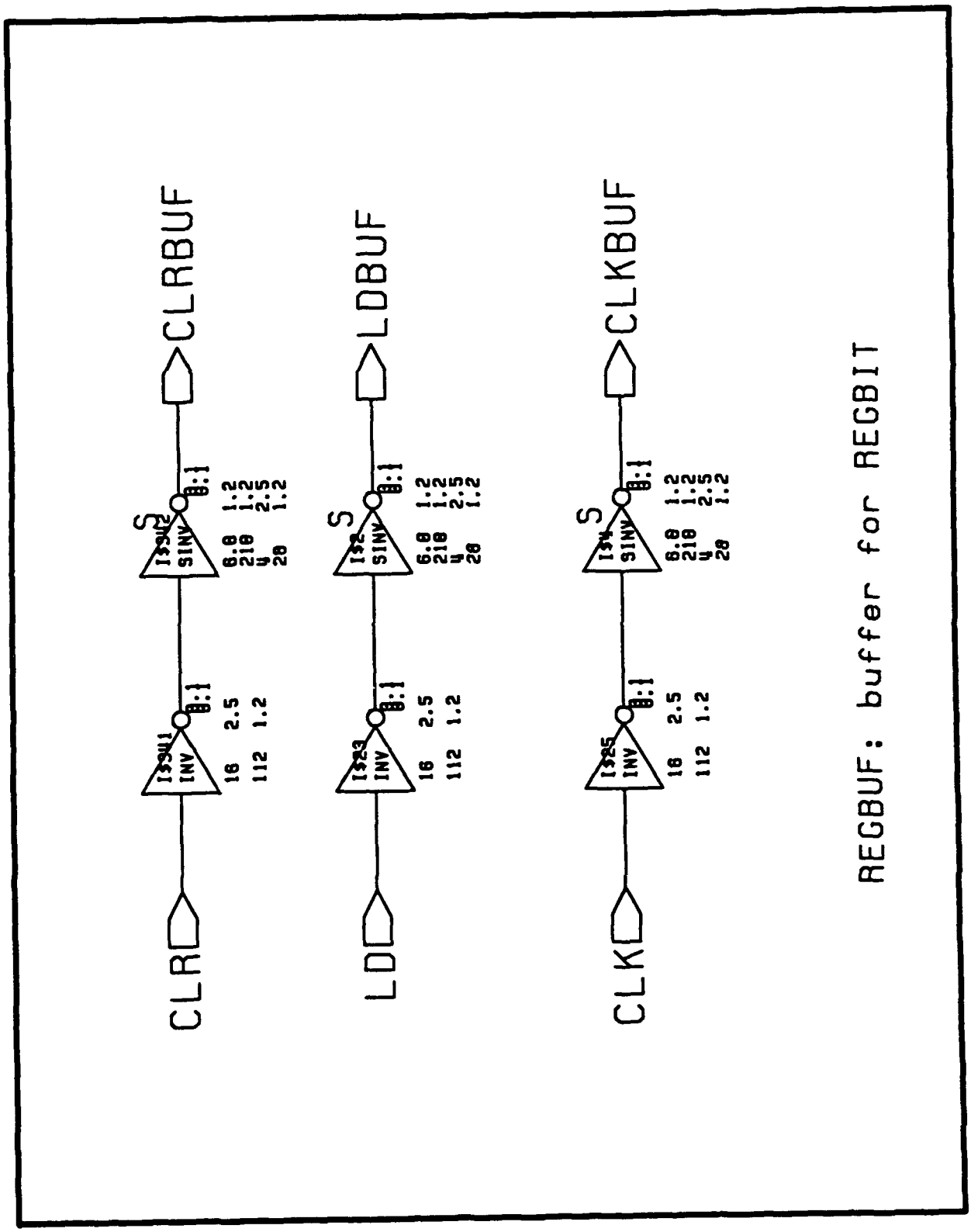

UXX
REGBIT
OUT
Q
CLR
NI
D
LD
CLK
IN
IN
IN

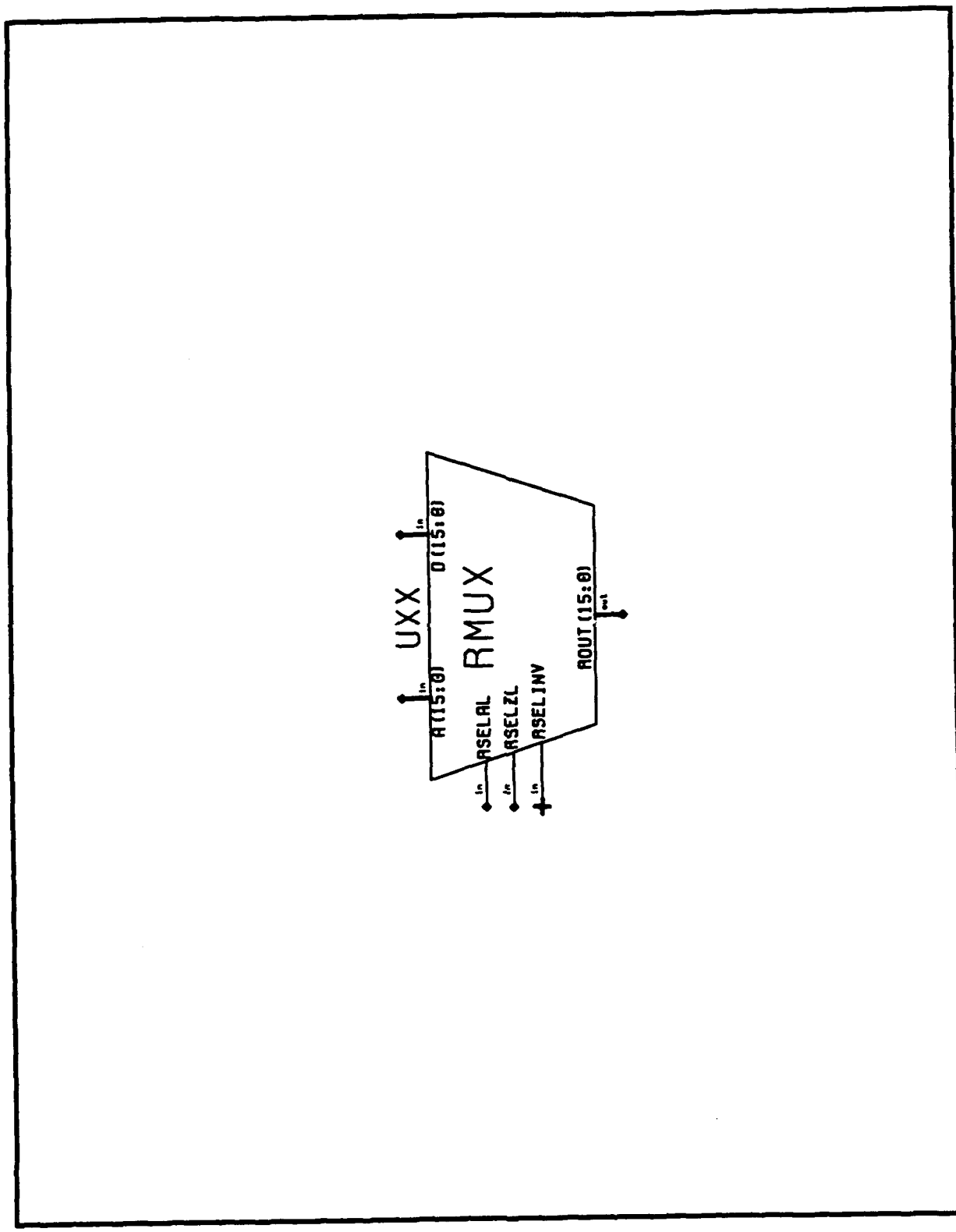

Q
CLK
CLR
D
LD
REGBIT


UXX
REGBIT16
OUT
Q
CLR
NI
D
LD
CLK
IN
IN
IN

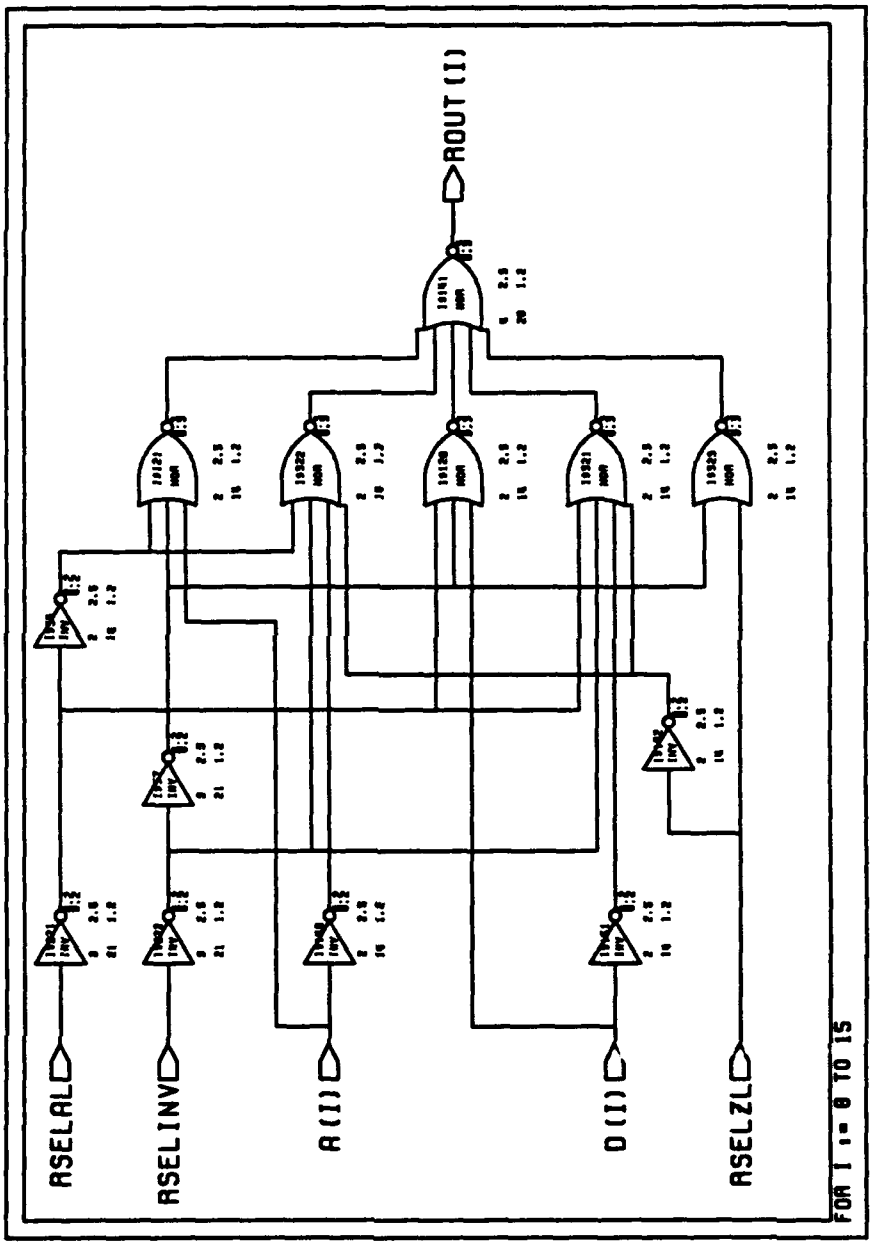

Q
CLK
CLR
D
LD
REGBIT16

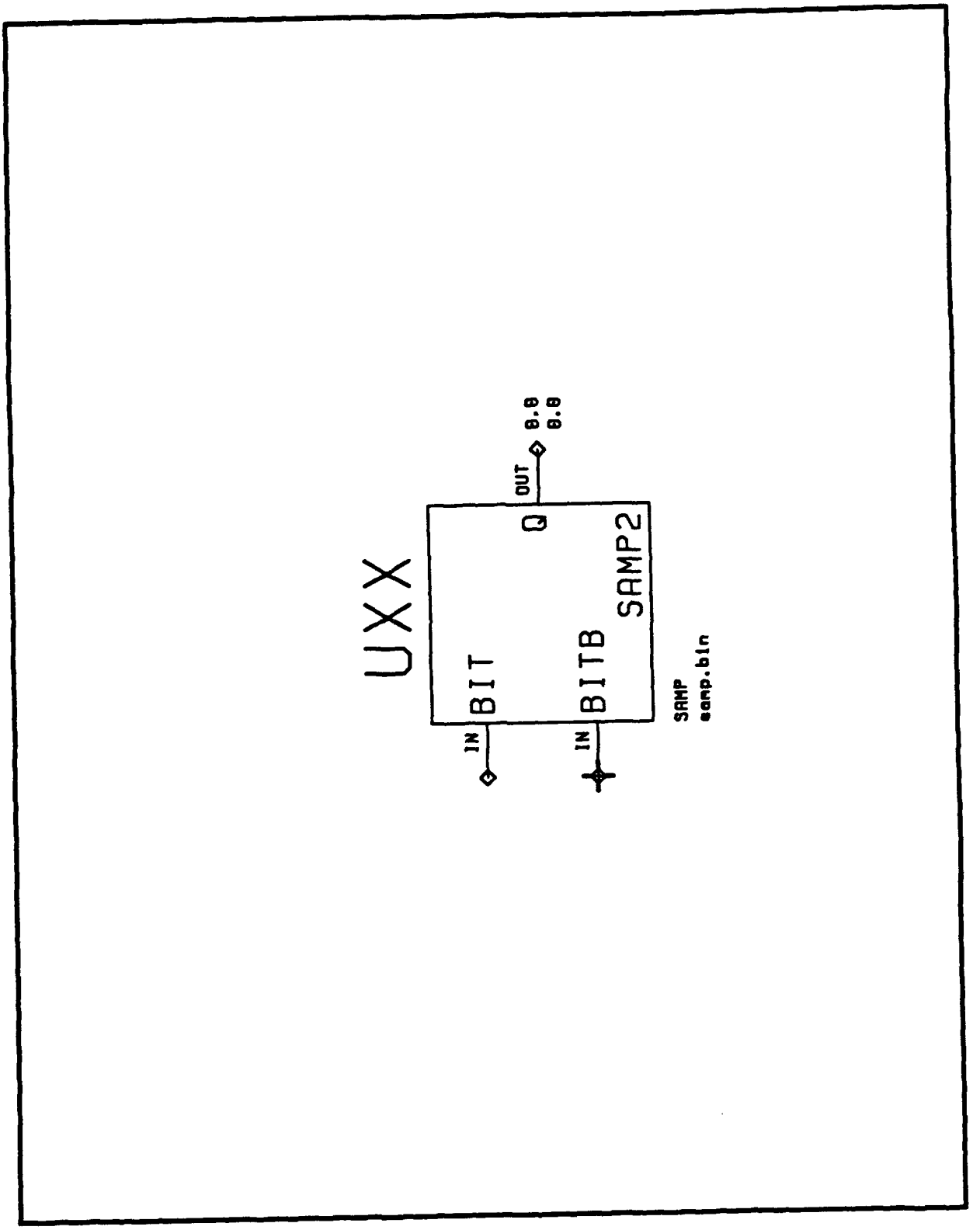

UXX
REGBUF
LDBUF
CLRBUF
CLKBUF
LD
CLR
CLK
IN
IN
IN
OUT
OUT
OUT

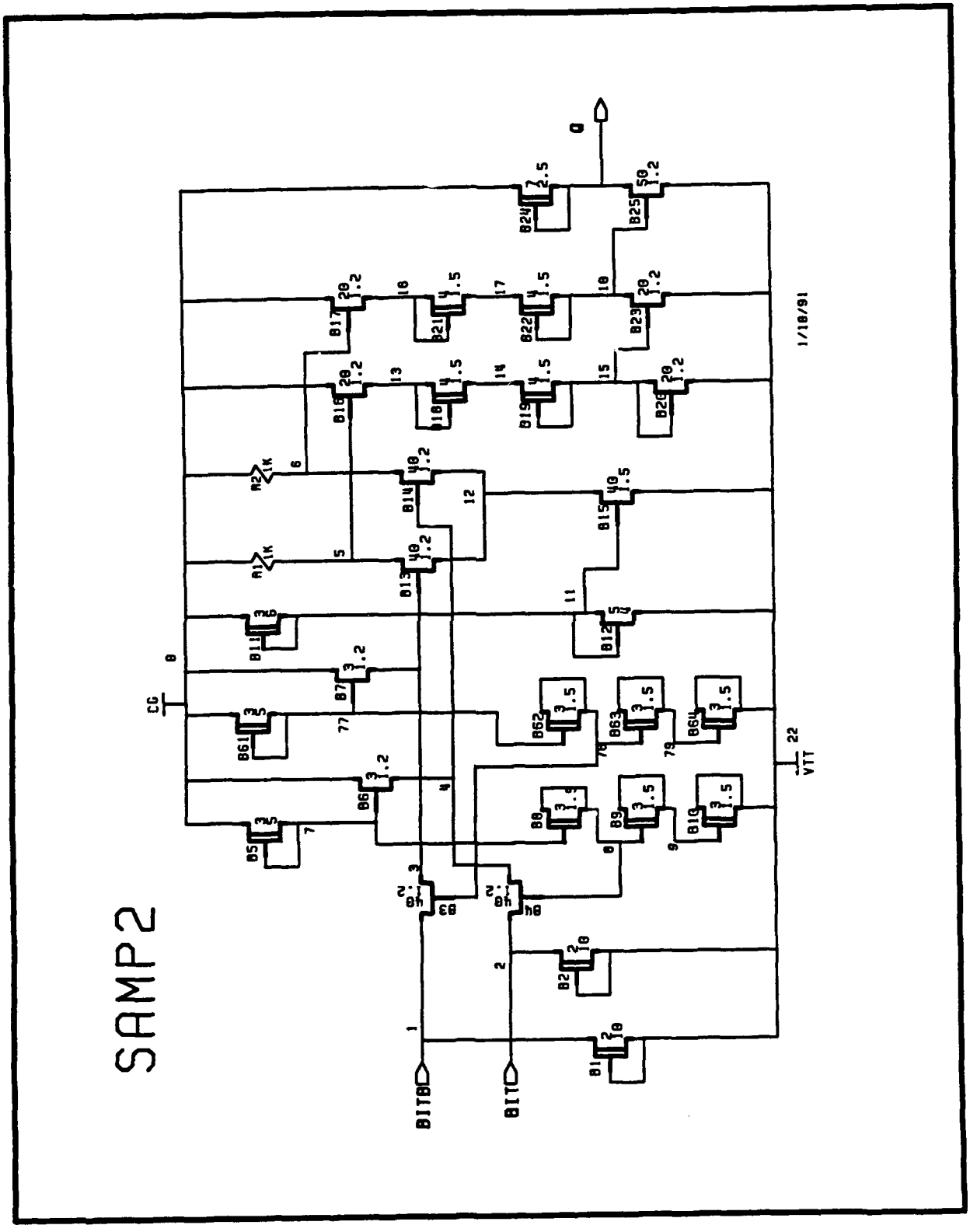

CLRBUF
LDBUF
CLKBUF
CLR
LD
CLK
INV
SINV
REGBUF: buffer for REGBIT

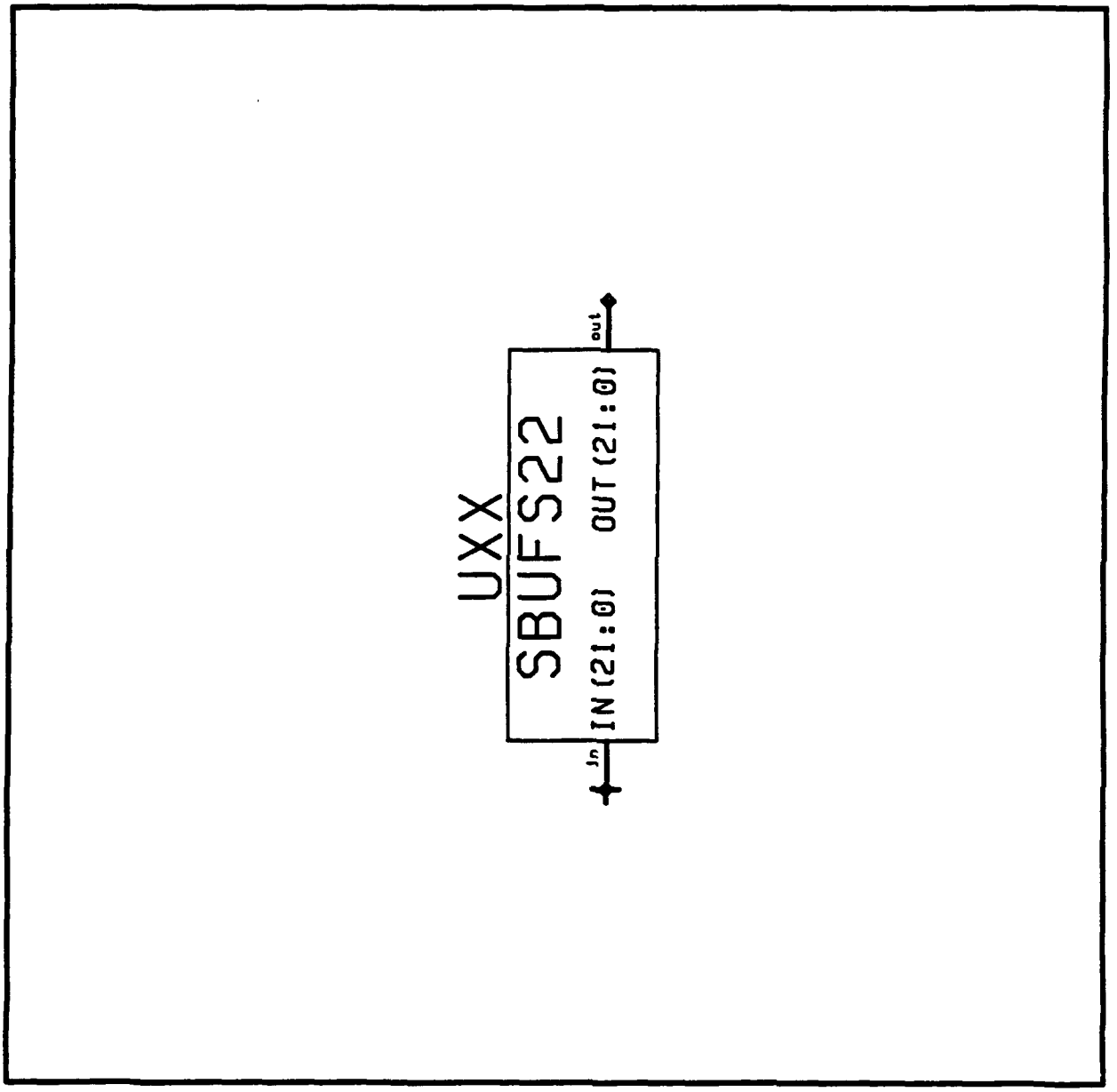

UXX
RMUX
A[15:0]
D[15:0]
ASELAL
ASELZL
ASELINV
AOUT[15:0]
in
out

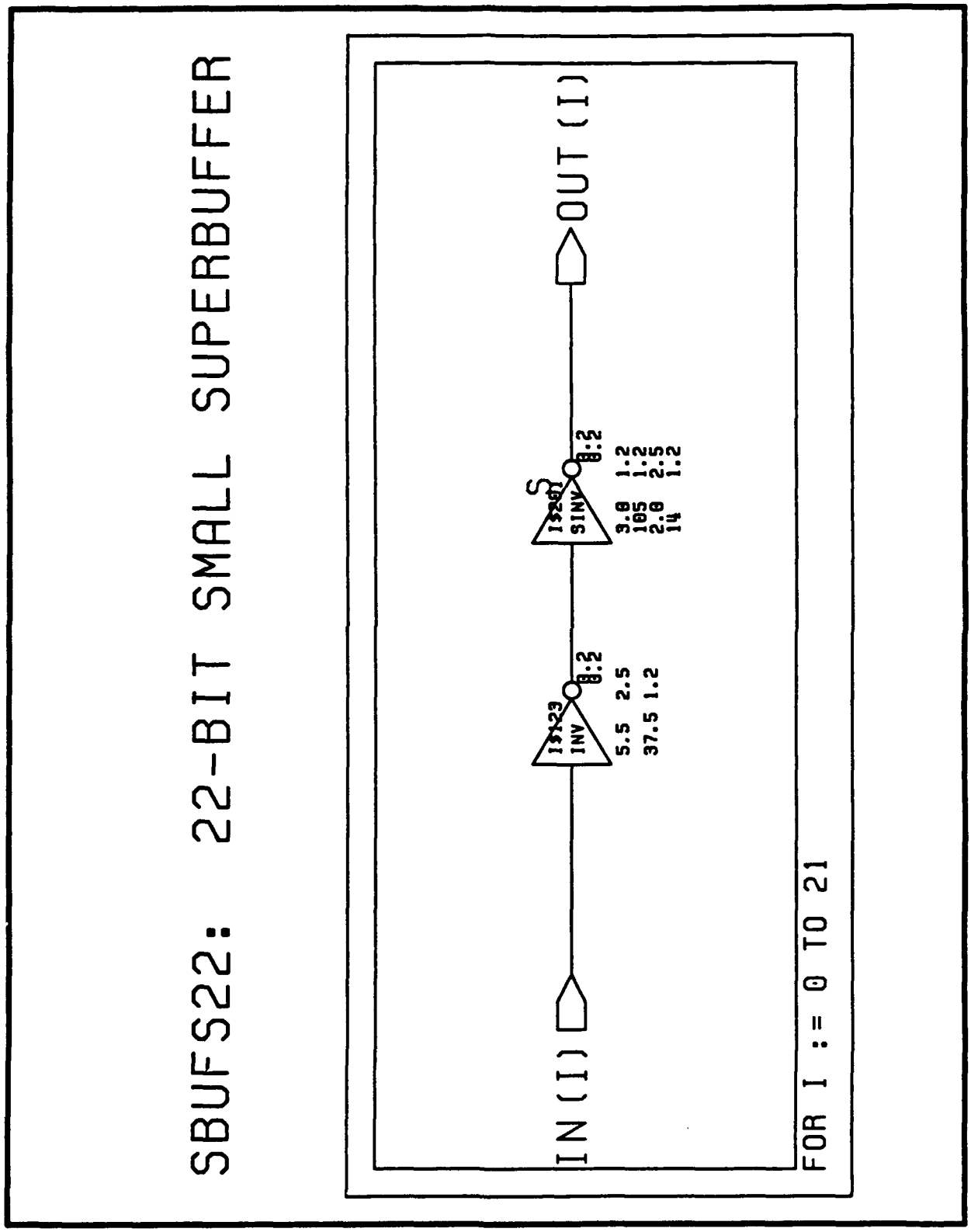
RMUX

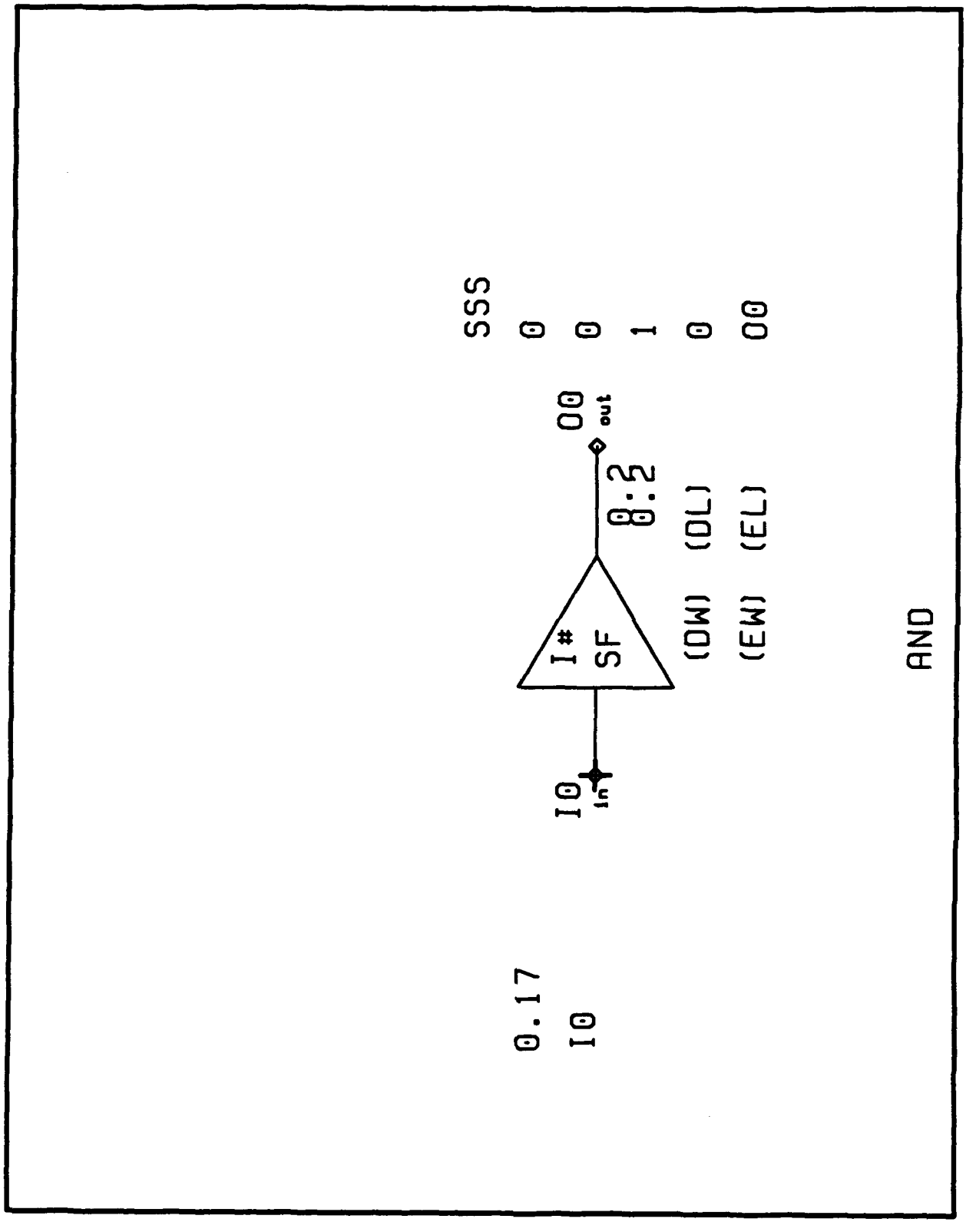


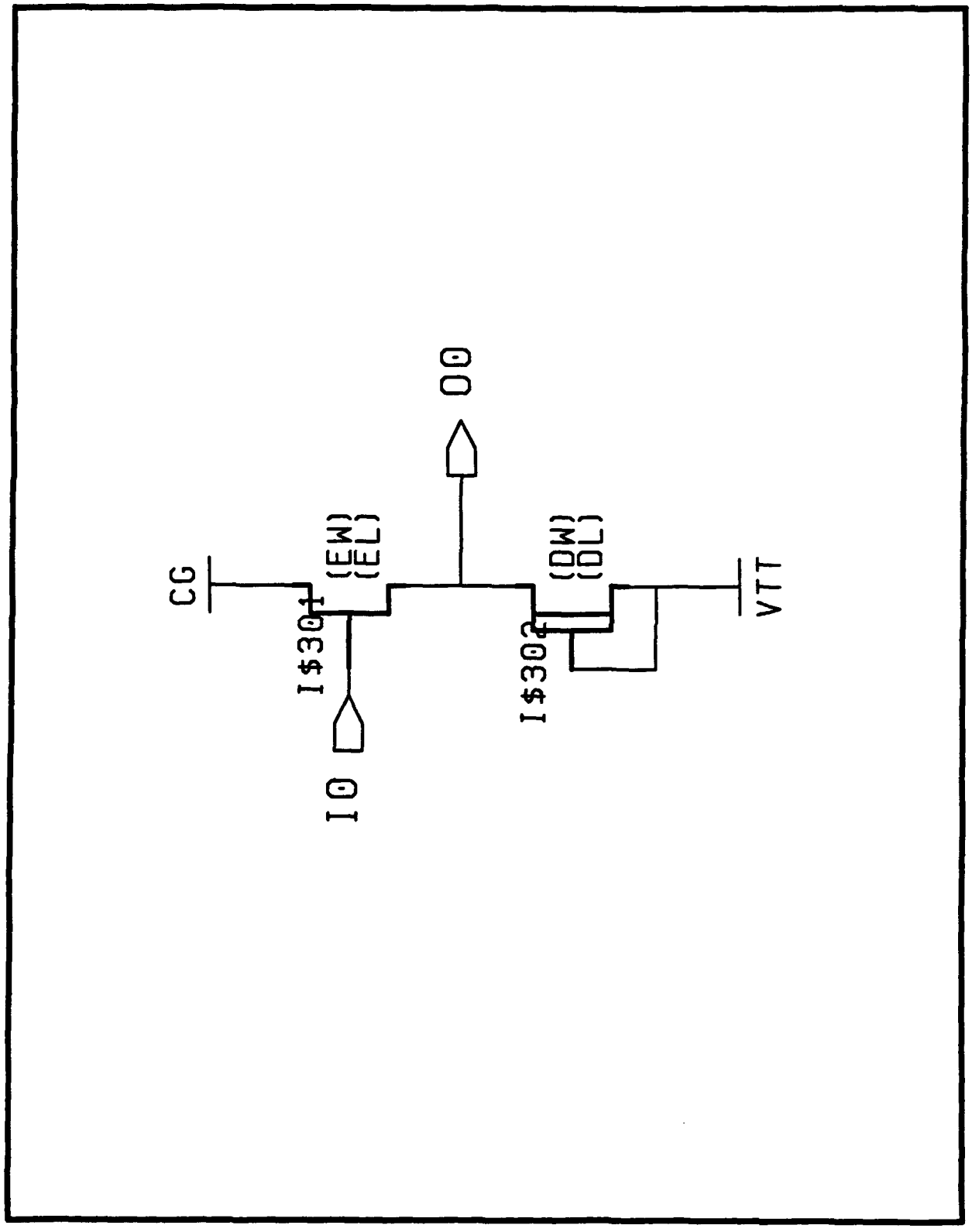

UXX
BIT
BITB
SAMP2
Q
OUT
IN
IN
8.0
8.0
SAMP
samp.bin

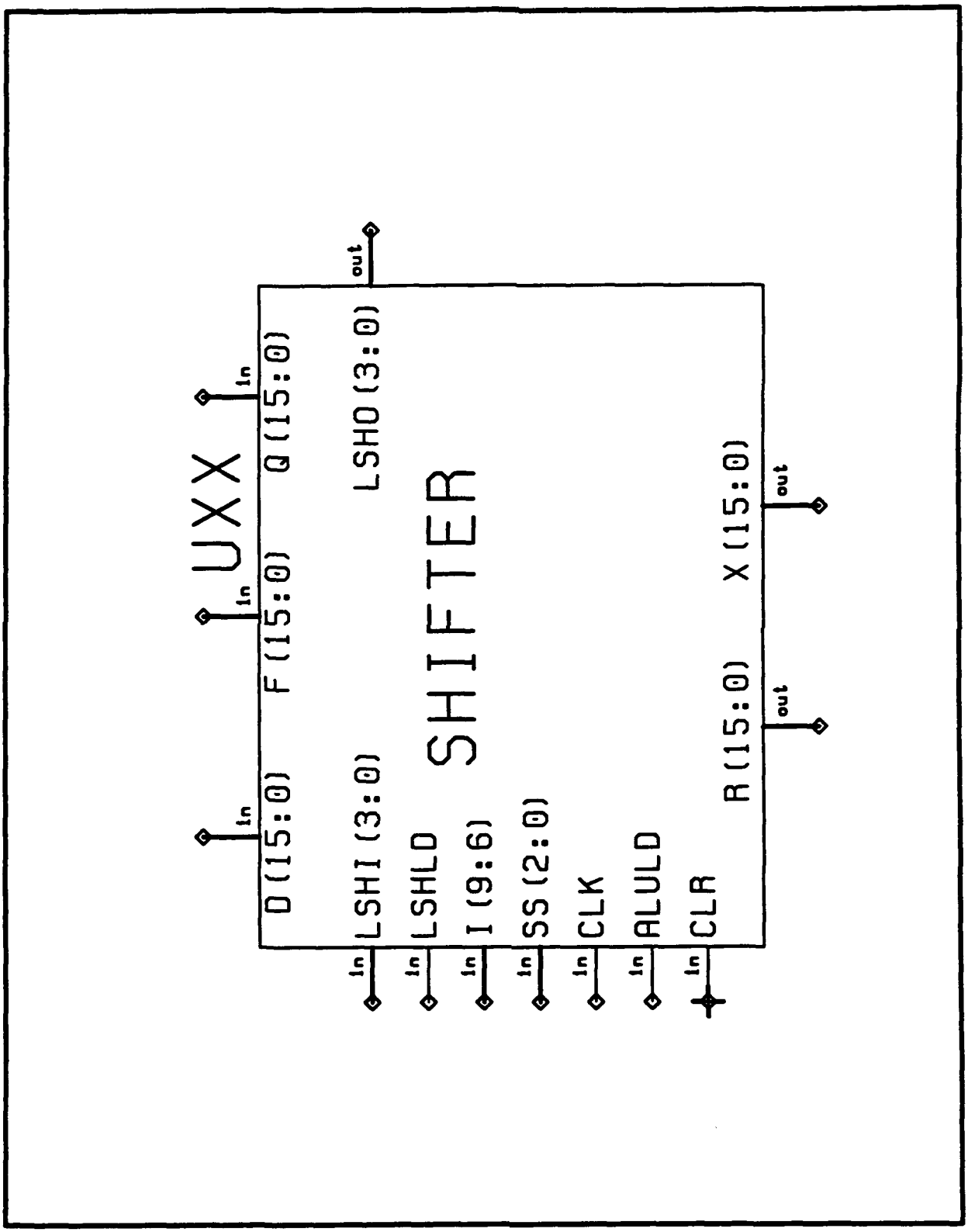

SAMP2
Q
CG
VTT
BITB
BIT
1/18/91

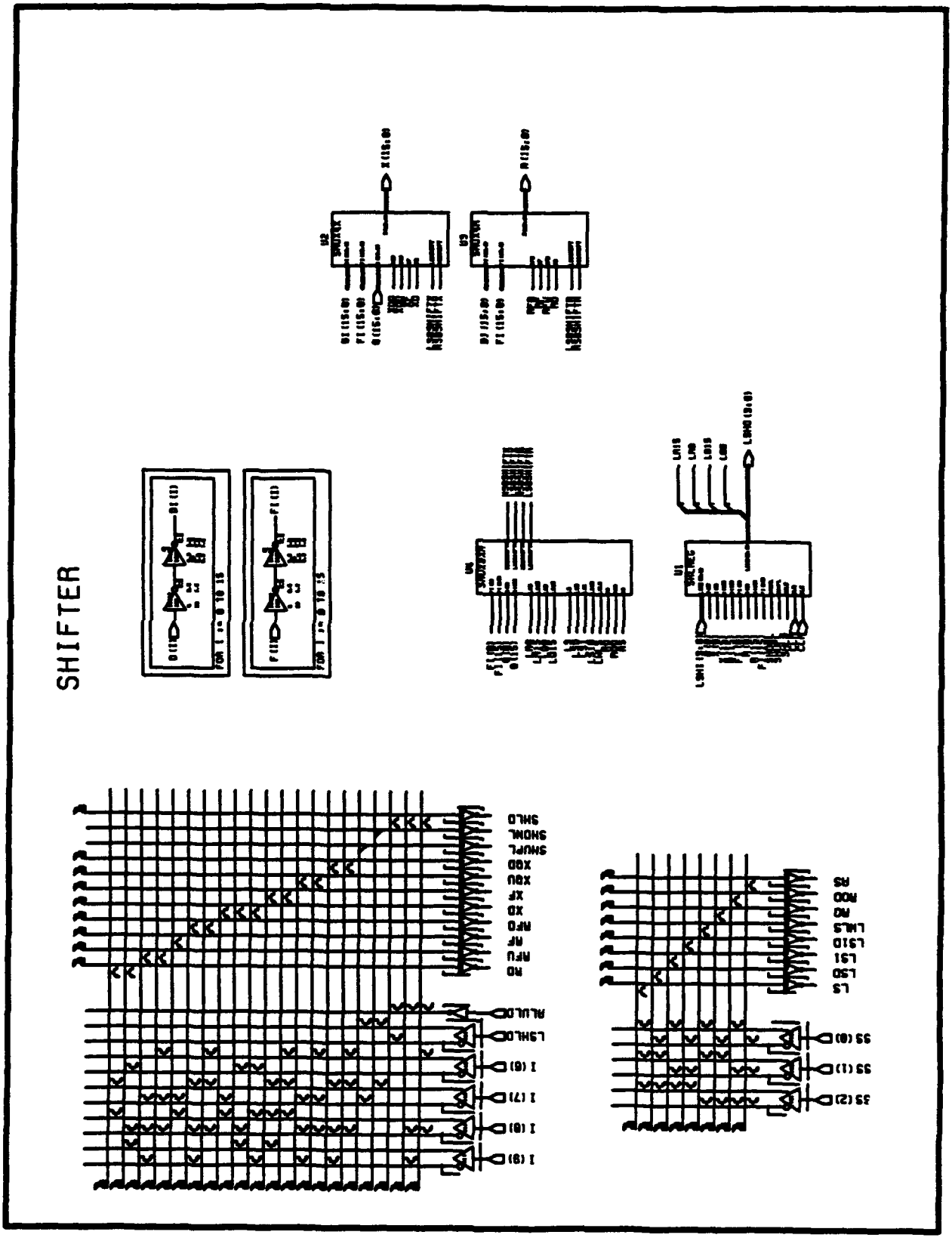

UXX
SBUFS22
IN(21:0)
OUT(21:0)
in
out

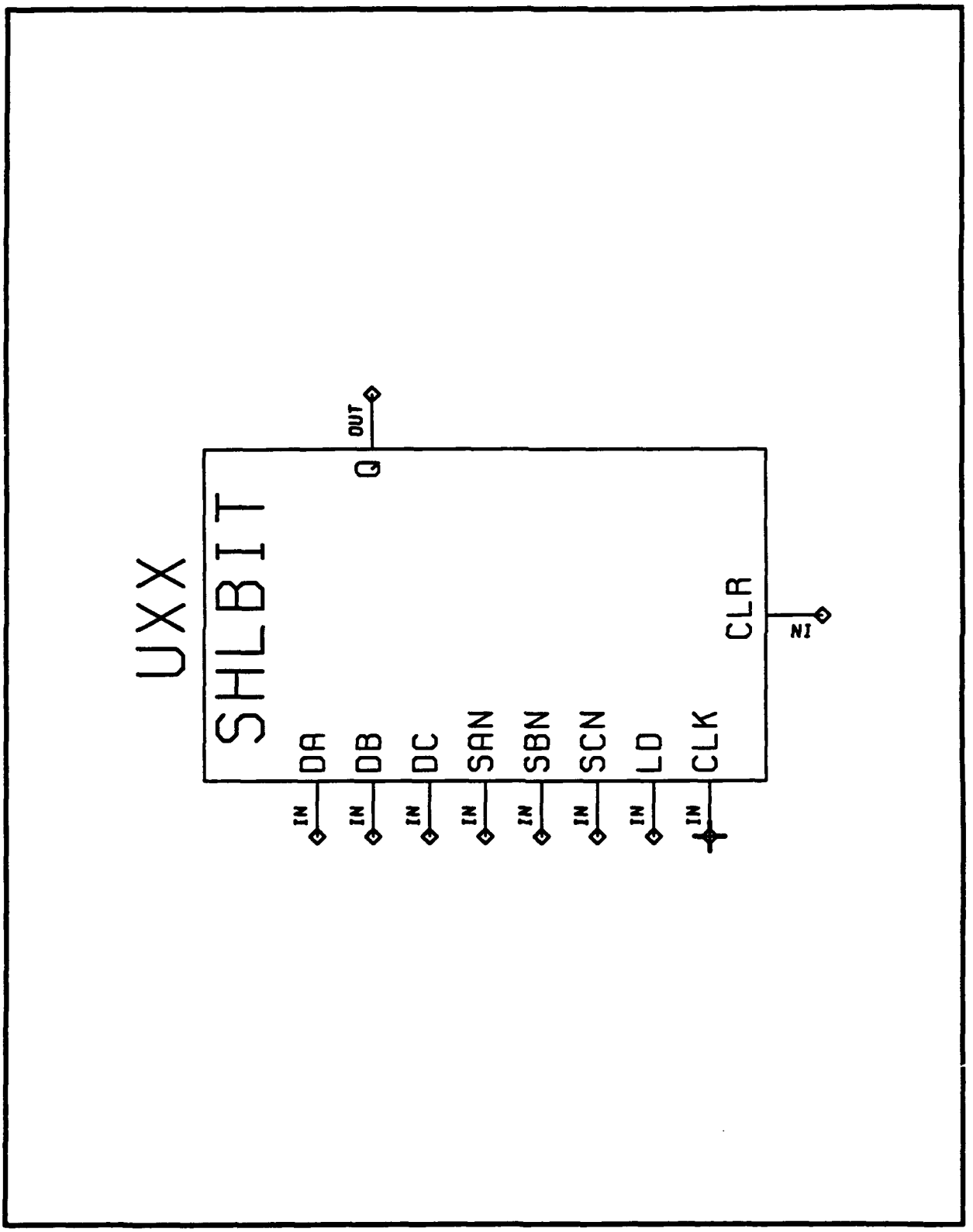

SBUFS22: 22-BIT SMALL SUPERBUFFER
IN(I)
OUT(I)
FOR I := 0 TO 21
I1423
INV
5.5 2.5
37.5 1.2
8.2
I1421
SINV
3.0 1.2
105 1.2
2.0 2.5
14 1.2
8.2

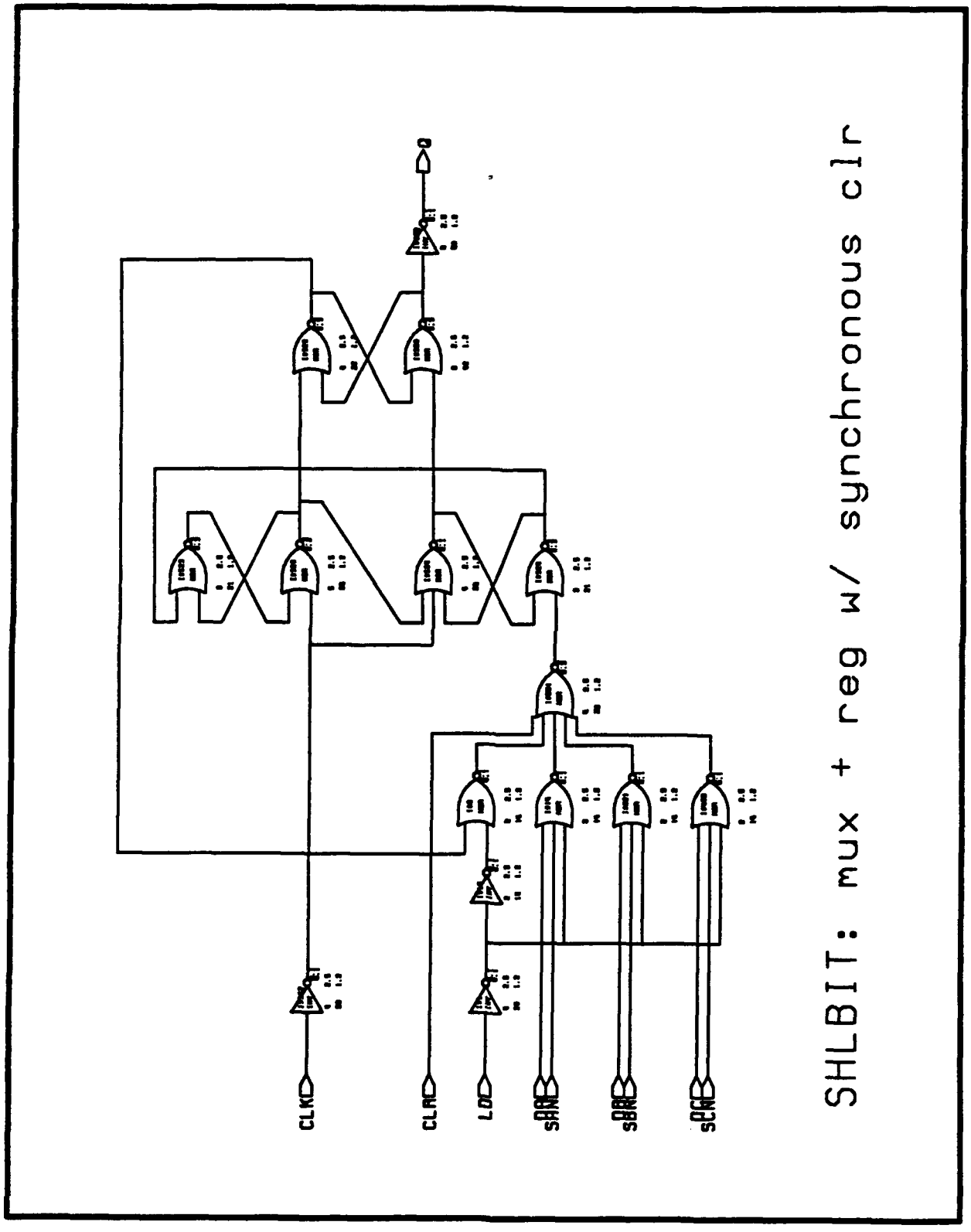

SSS
0
0
1
0
00
00
out
8.2
(DL)
(EL)
I#
SF
(DW)
(EW)
AND
IO
in
0.17
IO

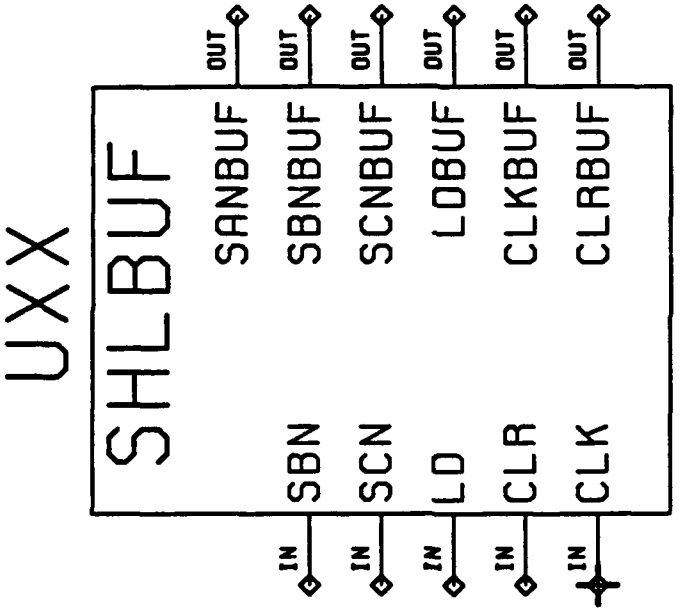

OO
CG
(EW)
(EL)
(OW)
(OL)
VTT
I$301
I$302
IO

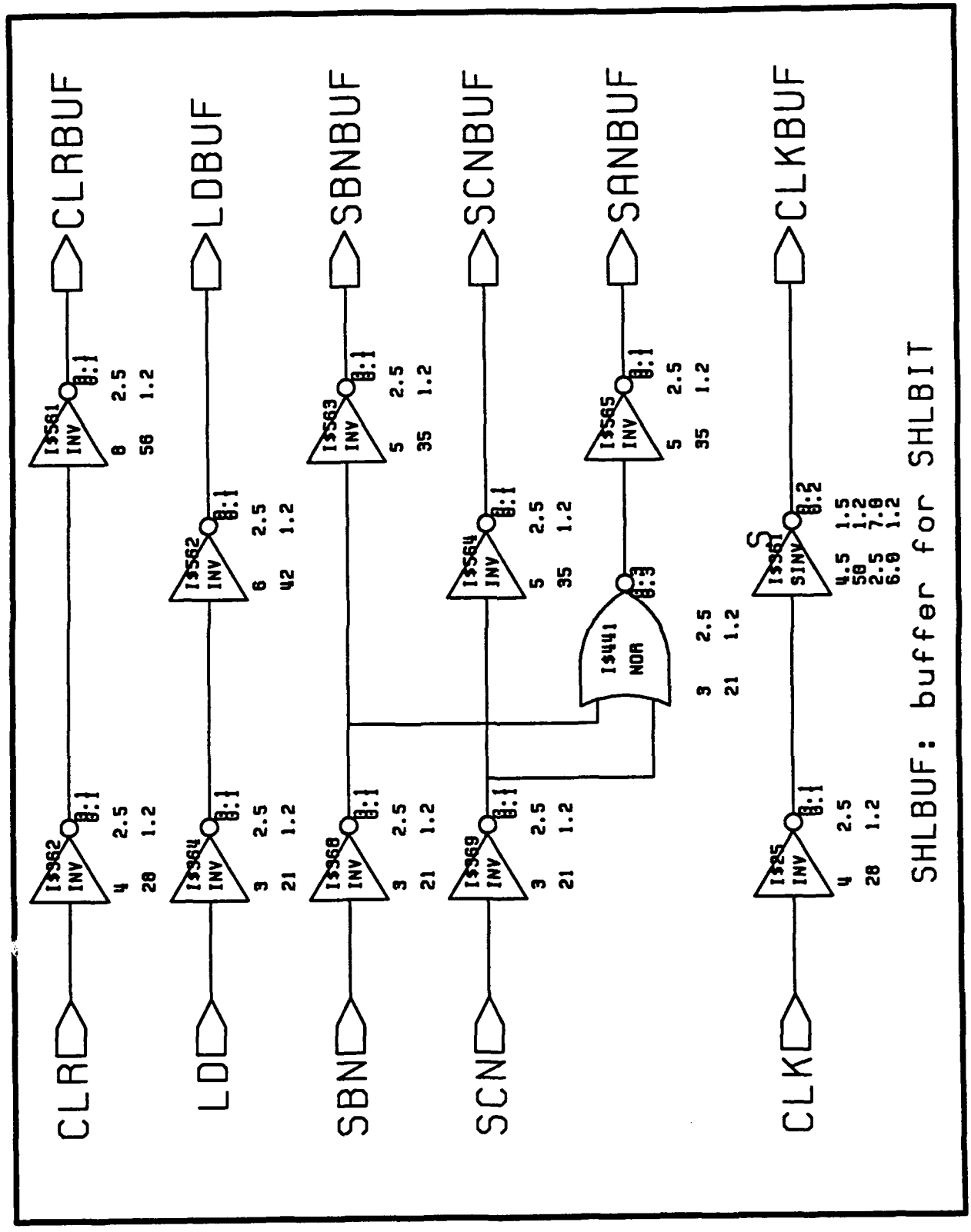

UXX
SHIFTER
D(15:0)
F(15:0)
Q(15:0)
LSHO(3:0)
X(15:0)
R(15:0)
LSHI(3:0)
LSHLD
I(9:6)
SS(2:0)
CLK
ALULD
CLR
in
out

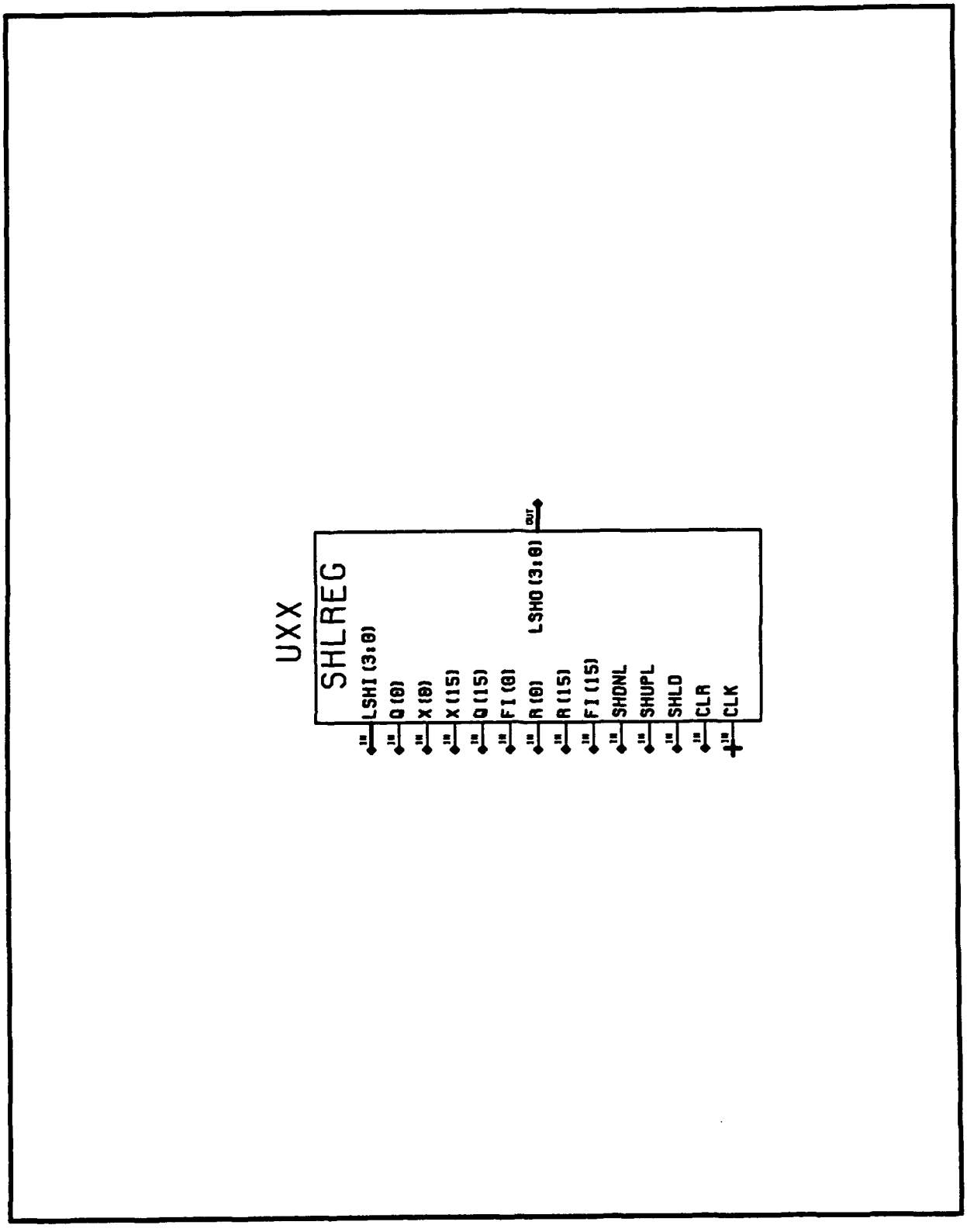

SHIFTER

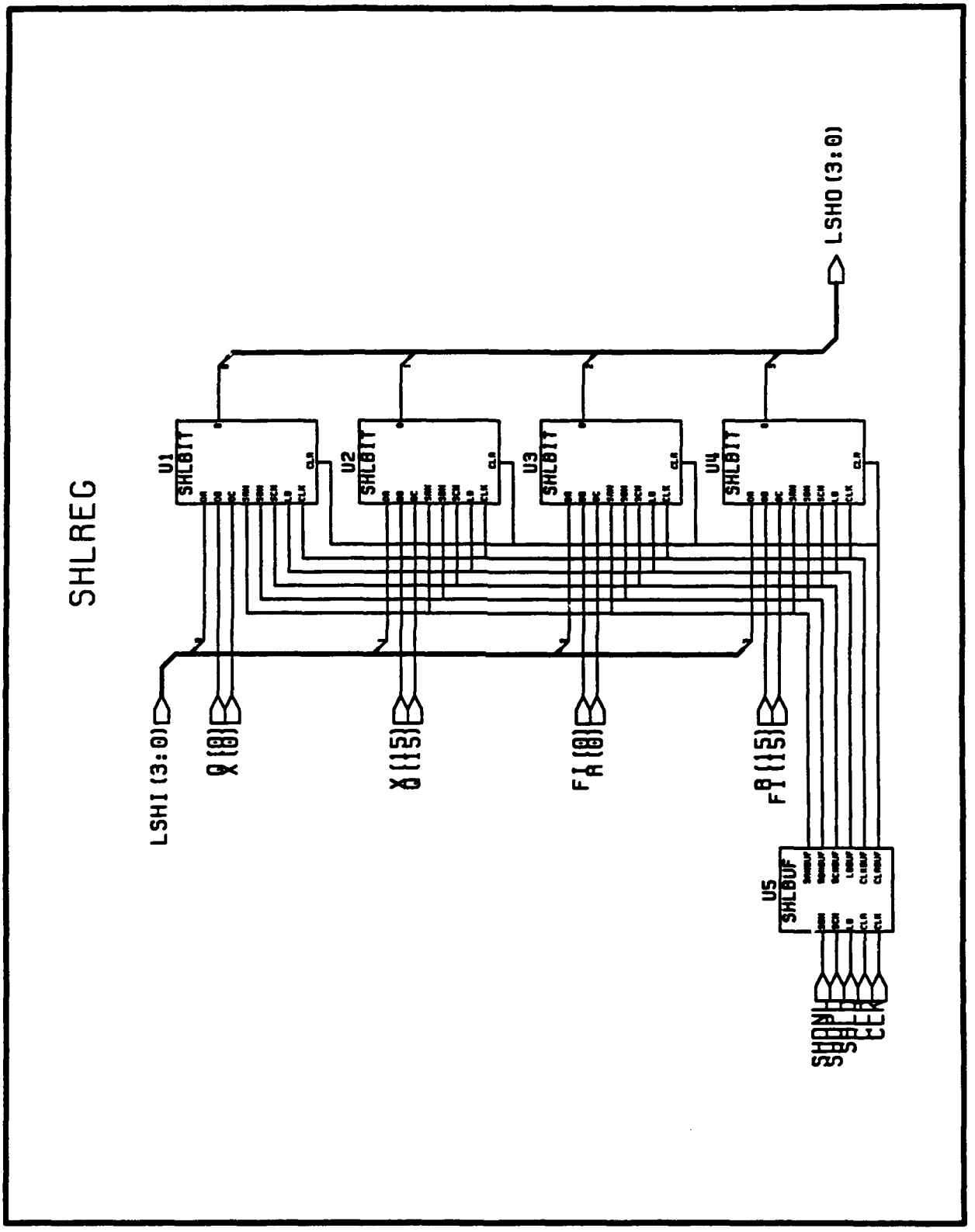

UXX
SHLBIT
OUT
Q
CLR
NI
DA
DB
DC
SAN
SBN
SCN
LD
CLK
IN
IN
IN
IN
IN
IN
IN
IN

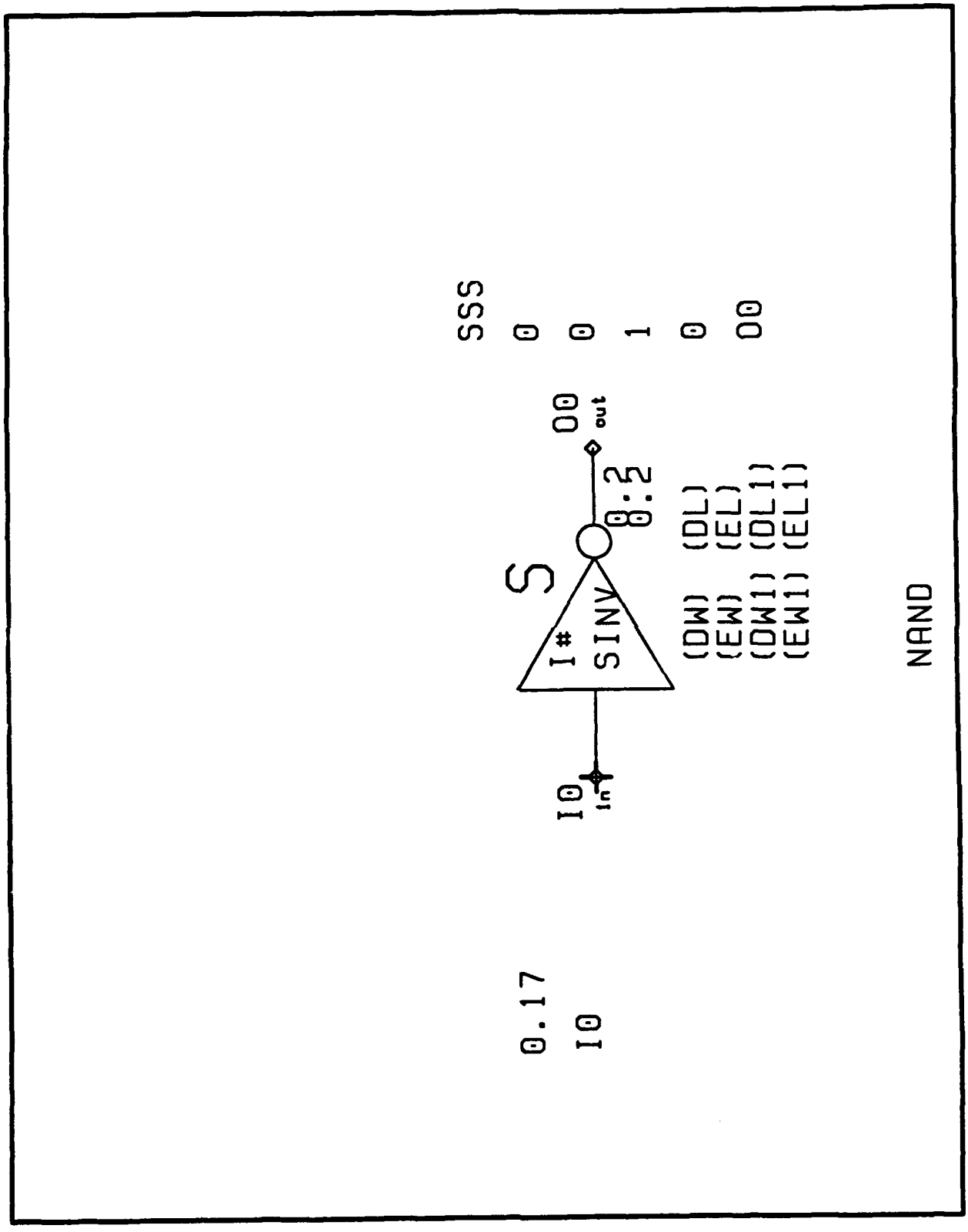

SHLBIT: mux + reg w/ synchronous clr
CLK
CLR
LD
SAR
SBR
SCR

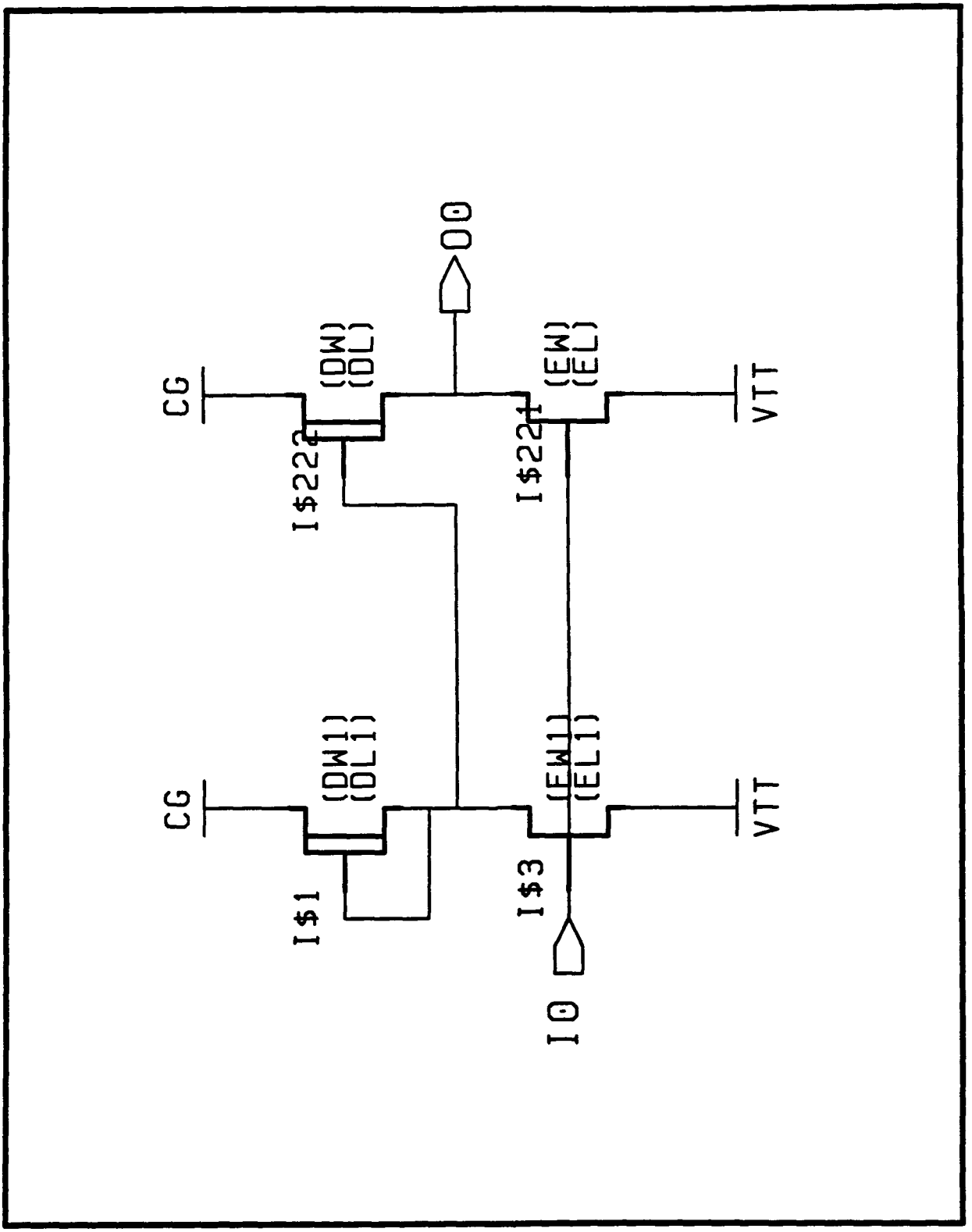

UXX
SHLBUF
OUT
SANBUF
OUT
SBNBUF
OUT
SCNBUF
OUT
LOBUF
OUT
CLKBUF
OUT
CLRBUF
SBN
IN
SCN
IN
LO
IN
CLR
IN
CLK
IN

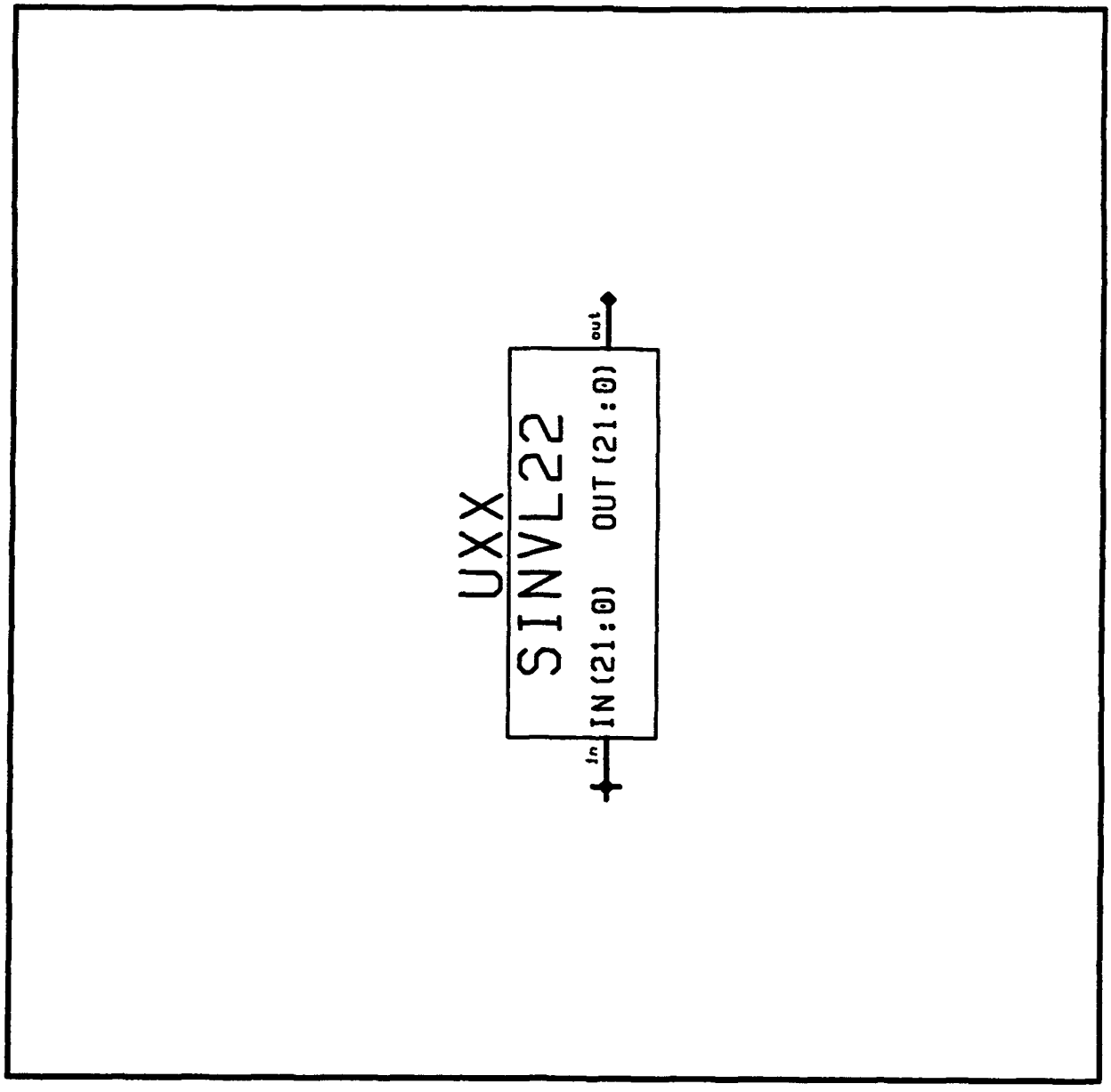

SHLBUF: buffer for SHLBIT
CLRBUF
LDBUF
SBNBUF
SCNBUF
SANBUF
CLKBUF
CLR
LD
SBN
SCN
CLK
S
I$561 INV 8:1 8 2.5 56 1.2
I$562 INV 8:1 6 2.5 42 1.2
I$563 INV 8:1 5 2.5 35 1.2
I$564 INV 8:1 5 2.5 35 1.2
I$565 INV 8:1 5 2.5 35 1.2
I$441 NOR 8:3 3 2.5 21 1.2
I$961 SINV 8:2 4.5 1.5 50 1.2 2.5 7.0 6.0 1.2
I$962 INV 8:1 4 2.5 28 1.2
I$964 INV 8:1 3 2.5 21 1.2
I$968 INV 8:1 3 2.5 21 1.2
I$969 INV 8:1 3 2.5 21 1.2
I$25 INV 8:1 4 2.5 28 1.2

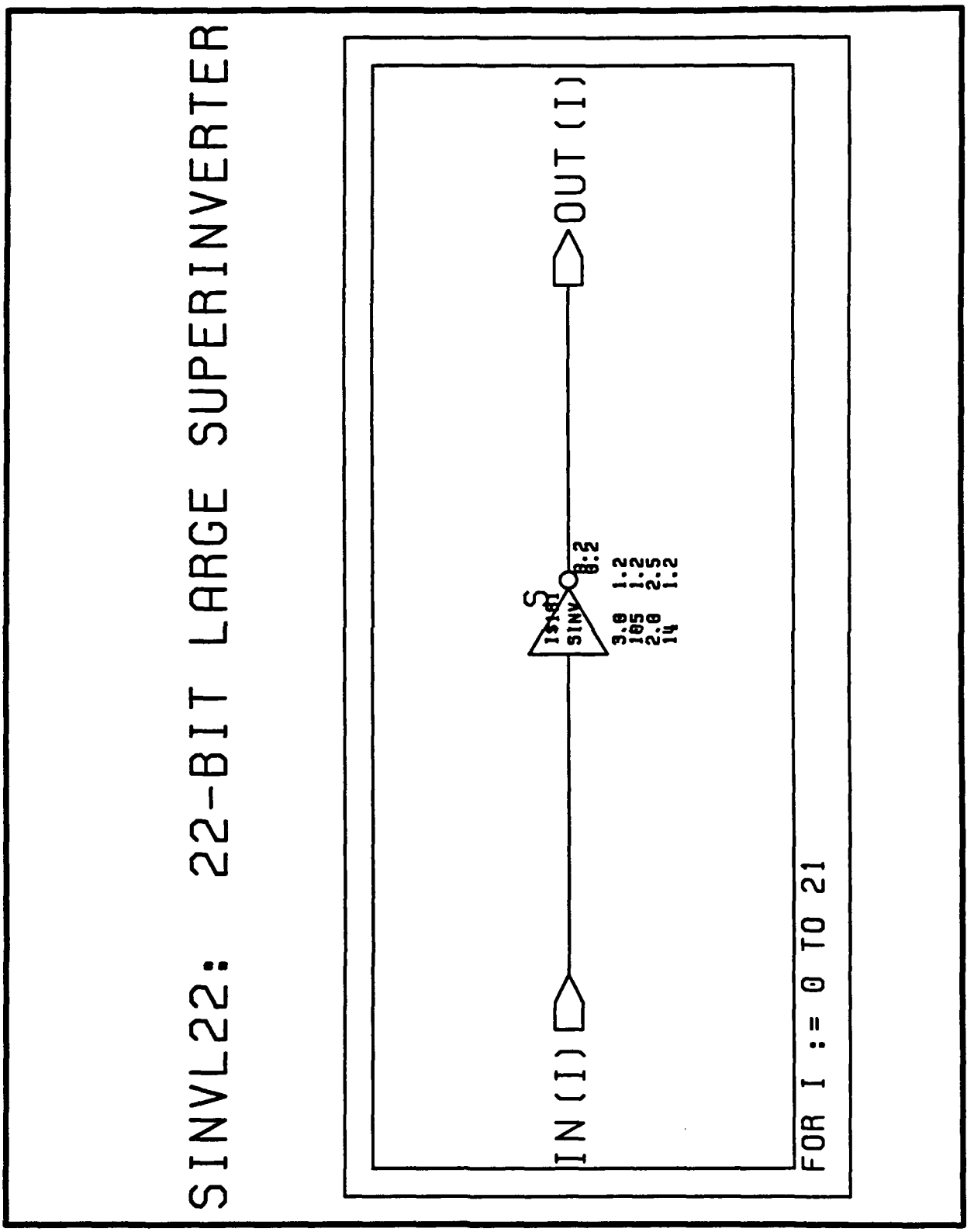

UXX
SHLREG
LSHI(3:0)
Q(0)
X(0)
X(15)
Q(15)
FI(0)
R(0)
R(15)
FI(15)
SHDNL
SHUPL
SHLD
CLR
CLK
LSHO(3:0)
OUT

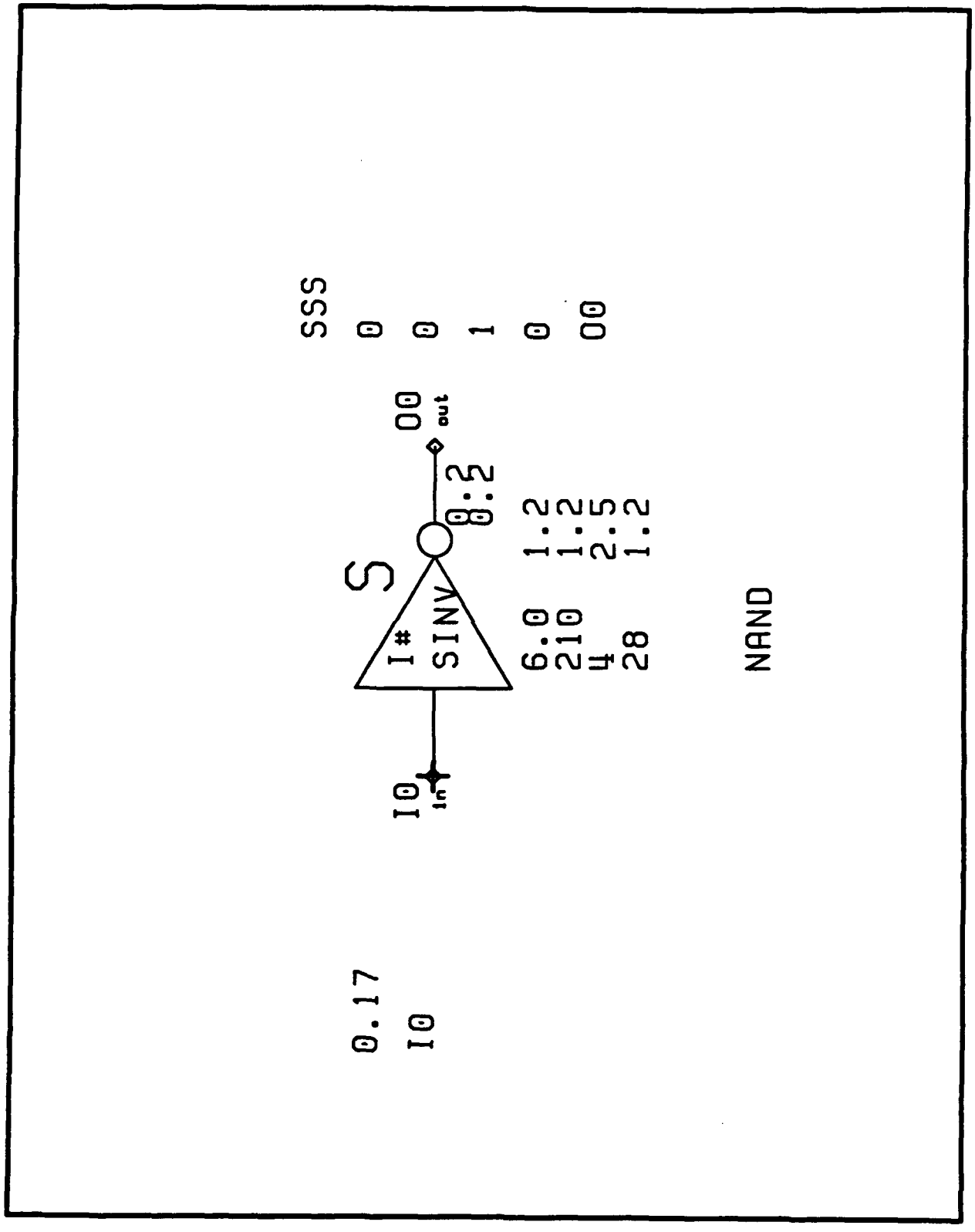

SHLREG
U1
SHLBIT
U2
SHLBIT
U3
SHLBIT
U4
SHLBIT
U5
SHLBUF
LSHO(3:0)
LSHI(3:0)
Q(8)
X(15)
FA(8)
FB(15)

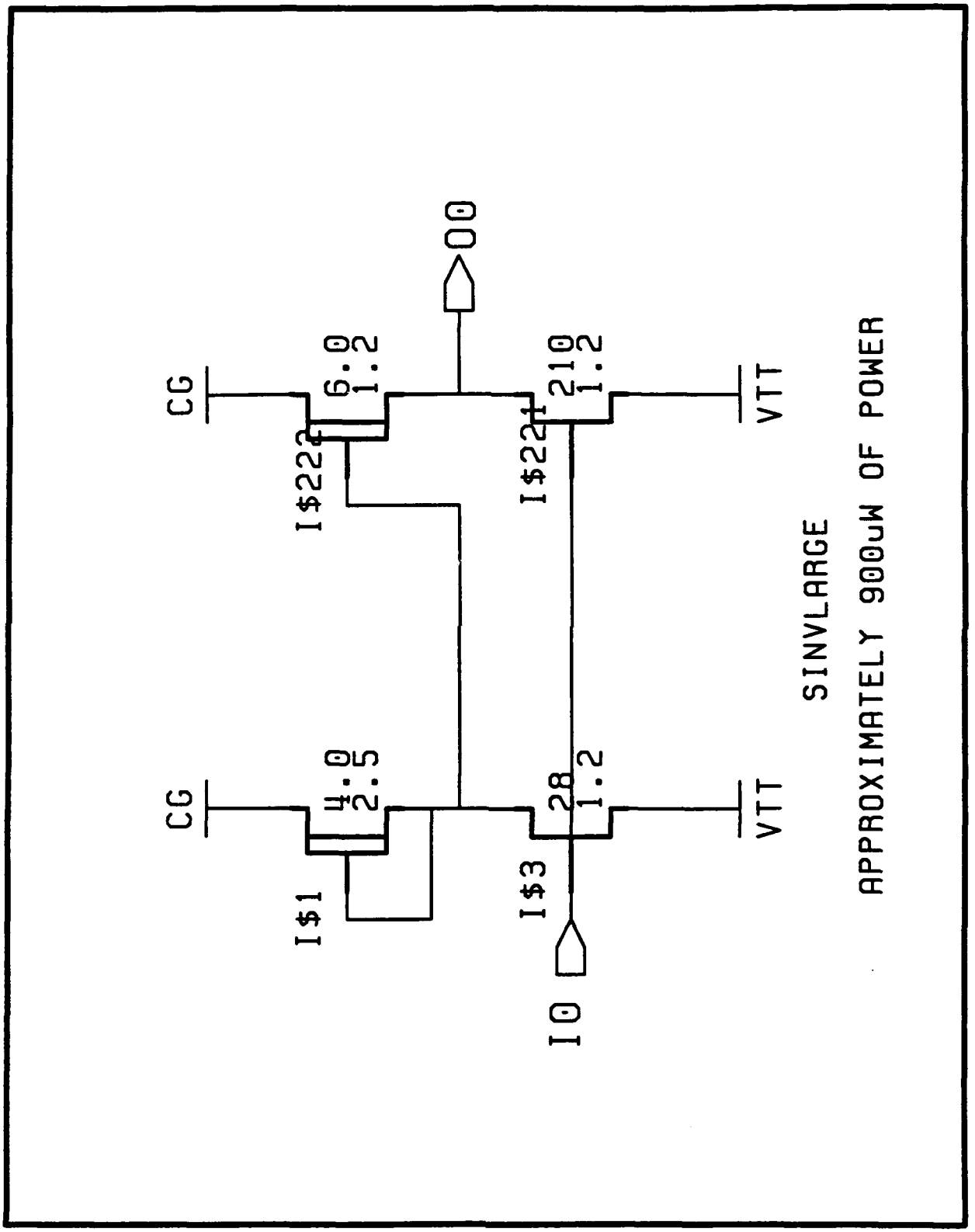

SSS
0 0 1 0 00
00
out
8.2
S
I#
SINV
(OW) (DL)
(EW) (EL)
(OW1) (OL1)
(EW1) (EL1)
NAND
IO
in
0.17
IO

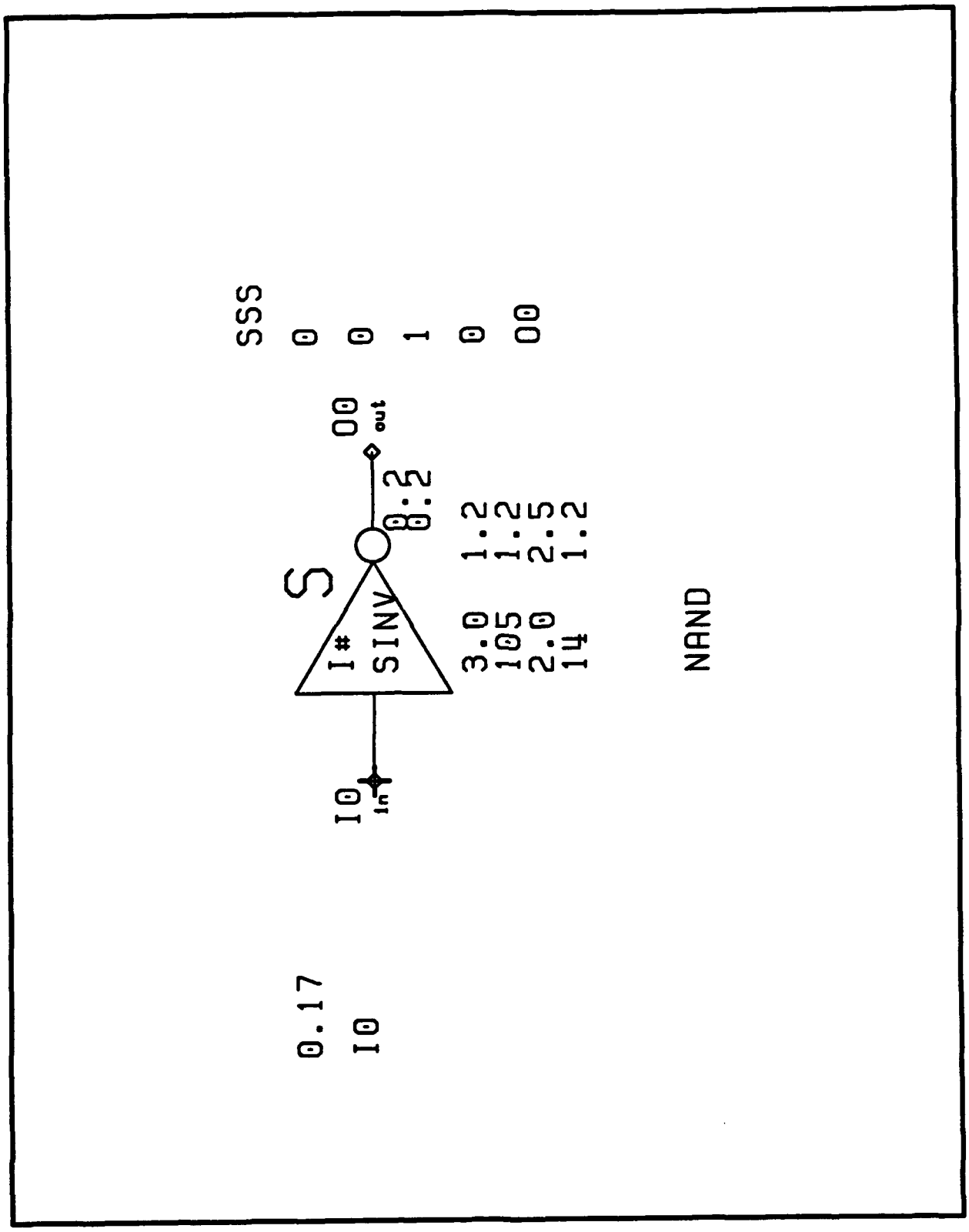

O0
CG
(DW)
(DL)
I$22
(EW)
(EL)
I$21
VTT
CG
(DW1)
(DL1)
I$1
(EW1)
(EL1)
I$3
VTT
I0

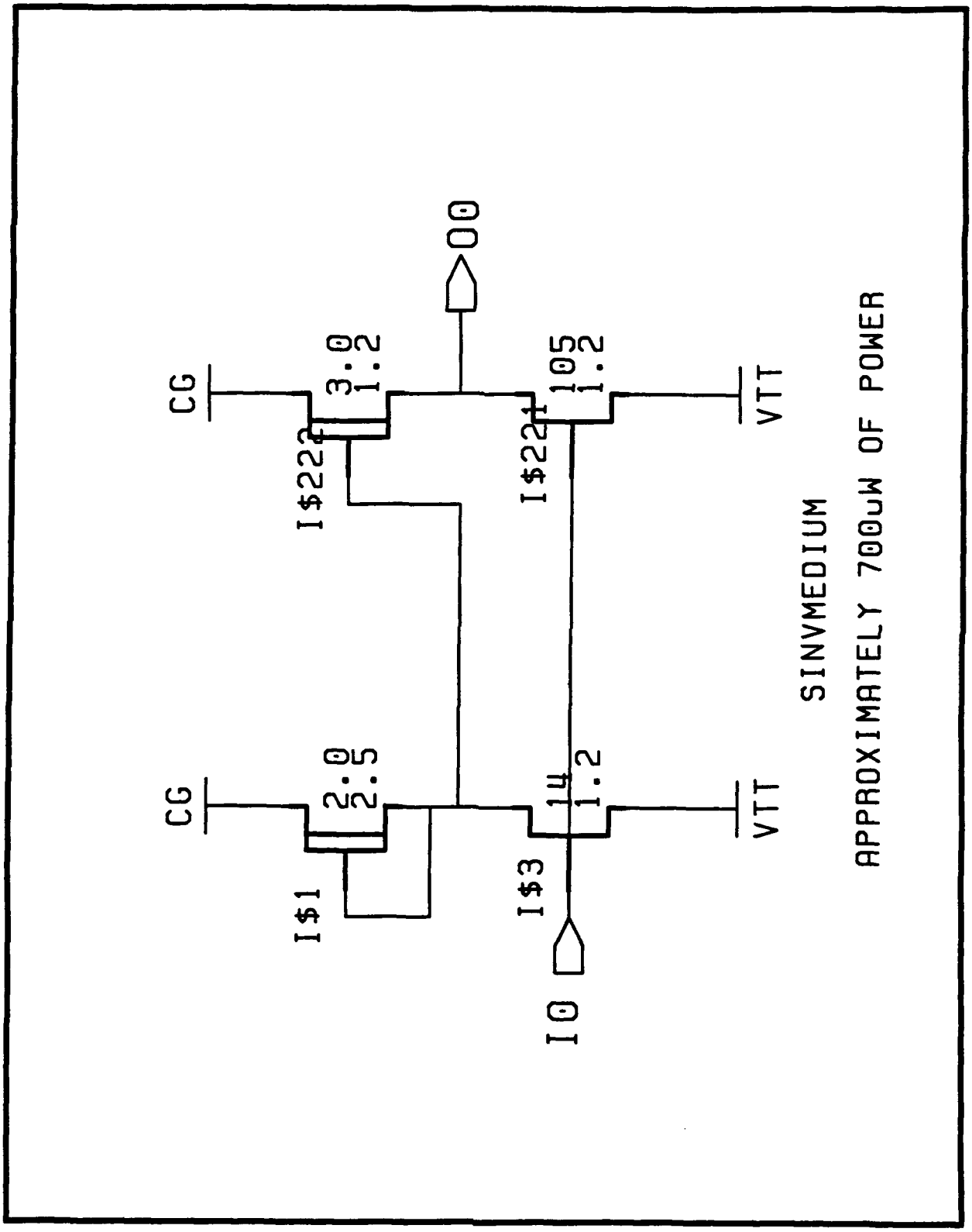

UXX
SINVL22
IN(21:0)
OUT(21:0)
in
out

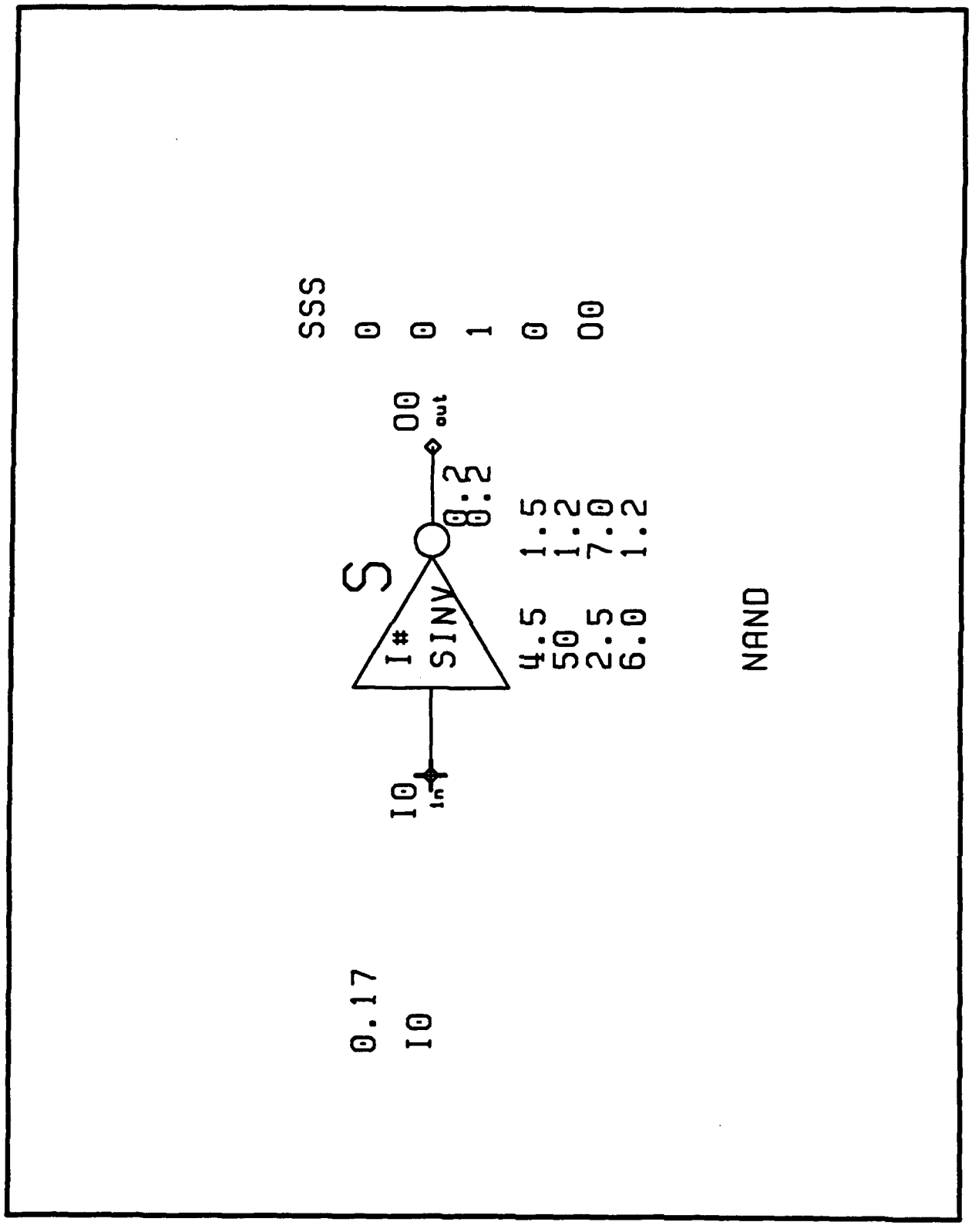

SINVL22: 22-BIT LARGE SUPERINVERTER
OUT(I)
IN(I)
FOR I := 0 TO 21
S
8.2
SINV
3.0 1.2
105 1.5
2.0 2.5
14 1.2

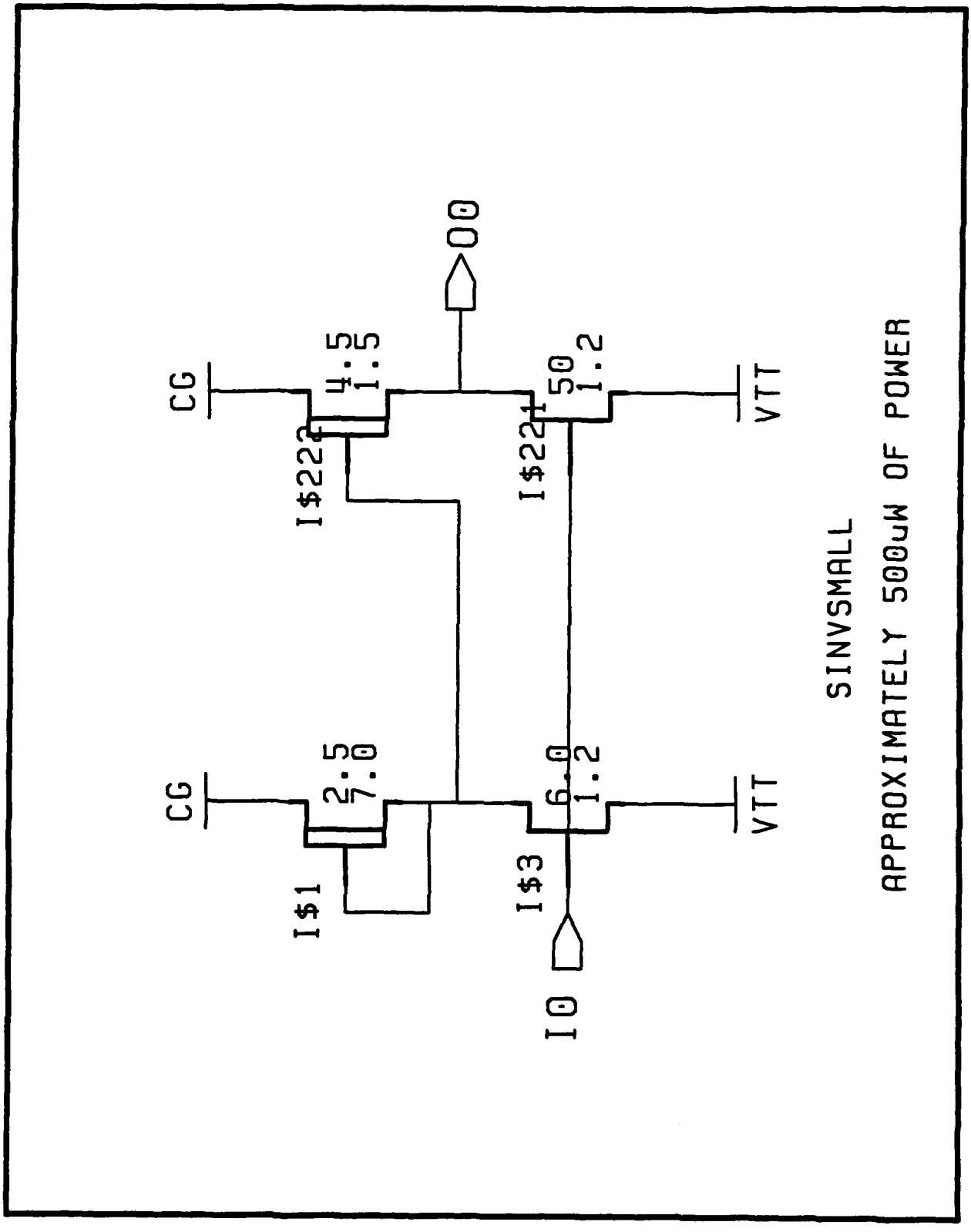

SSS
0 0 1 0 00
00
out
8.5
S
I#
SINV
6.0 1.2
210 1.2
4 2.5
28 1.2
NAND
I0
in
0.17
I0

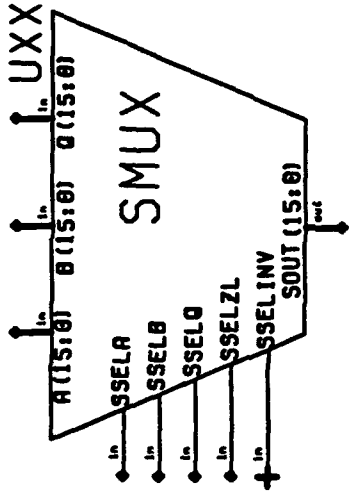

O0
CG
6.0
1.2
I$22
210
1.2
I$21
VTT
SINVLARGE
APPROXIMATELY 900uW OF POWER
CG
4.0
2.5
I$1
28
1.2
I$3
VTT
IO

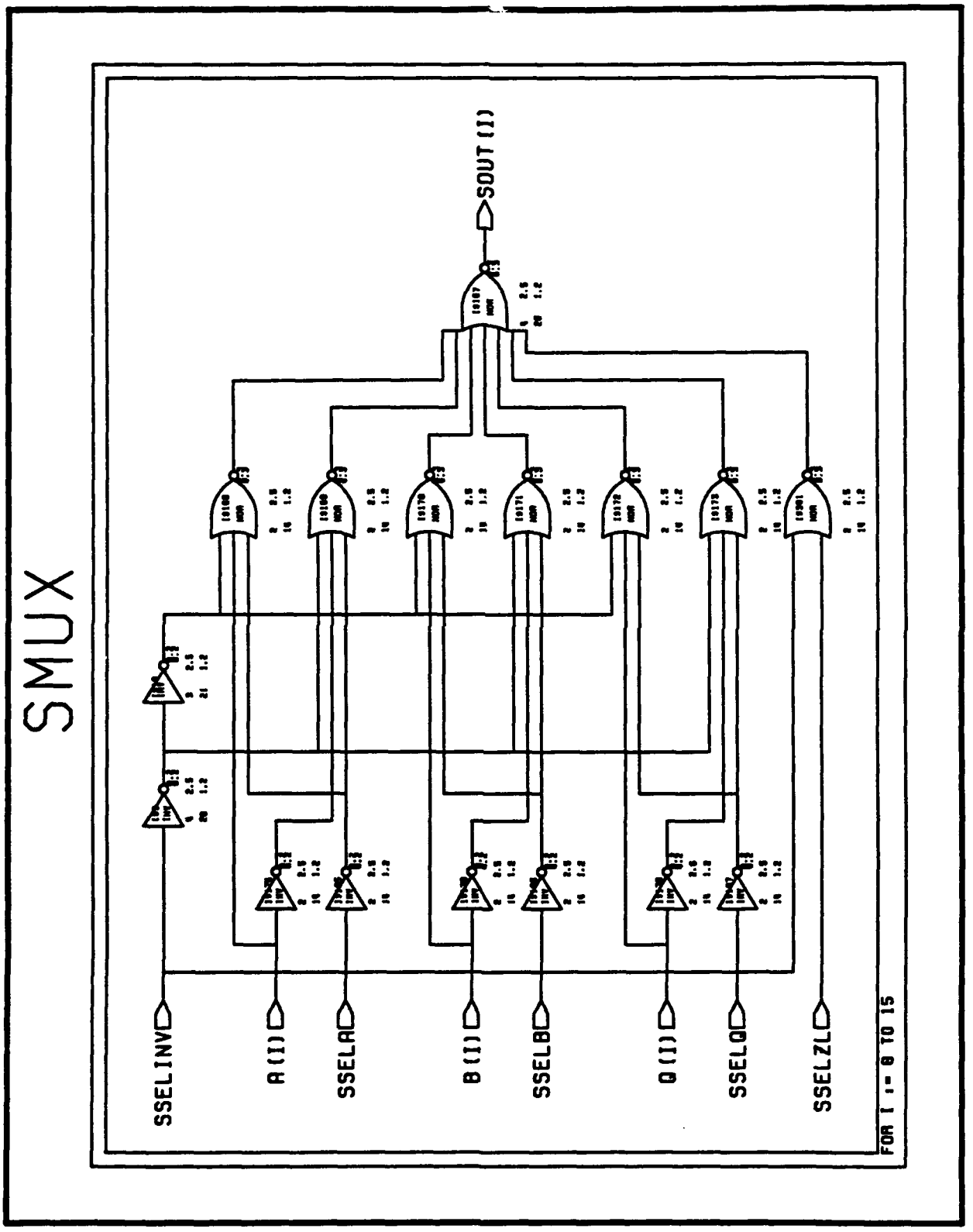

SSS
0 0 1 0 00
00
out
8.2
S
I#
SINV
3.0 1.2
105 1.2
2.0 2.5
14 1.2
NAND
I0
in
0.17
I0

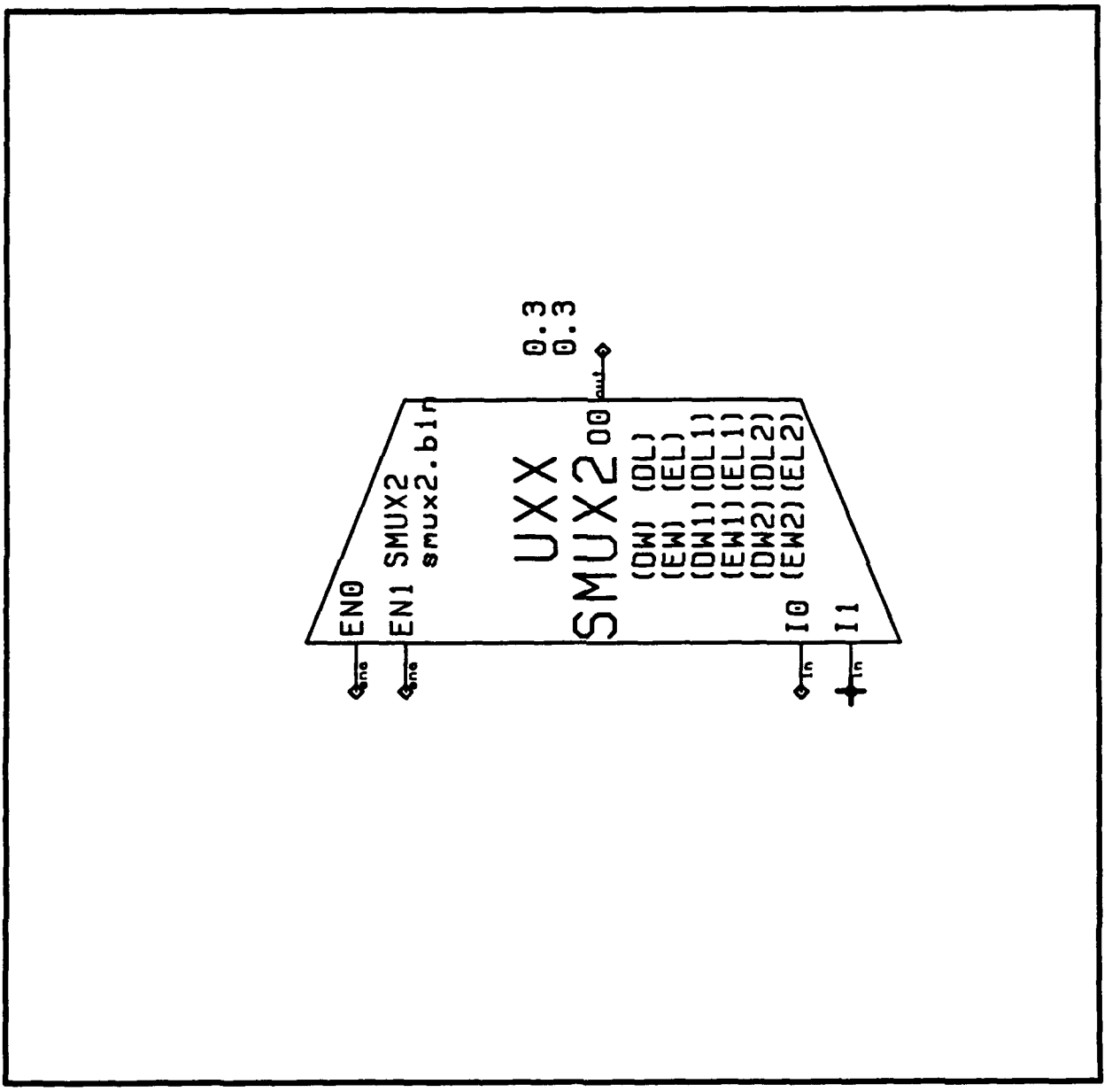

O0
CG
3.0
1.2
I$22
105
1.2
I$21
VTT
SINVMEDIUM
APPROXIMATELY 700uW OF POWER
CG
2.0
2.5
I$1
14
1.2
I$3
VTT
IO

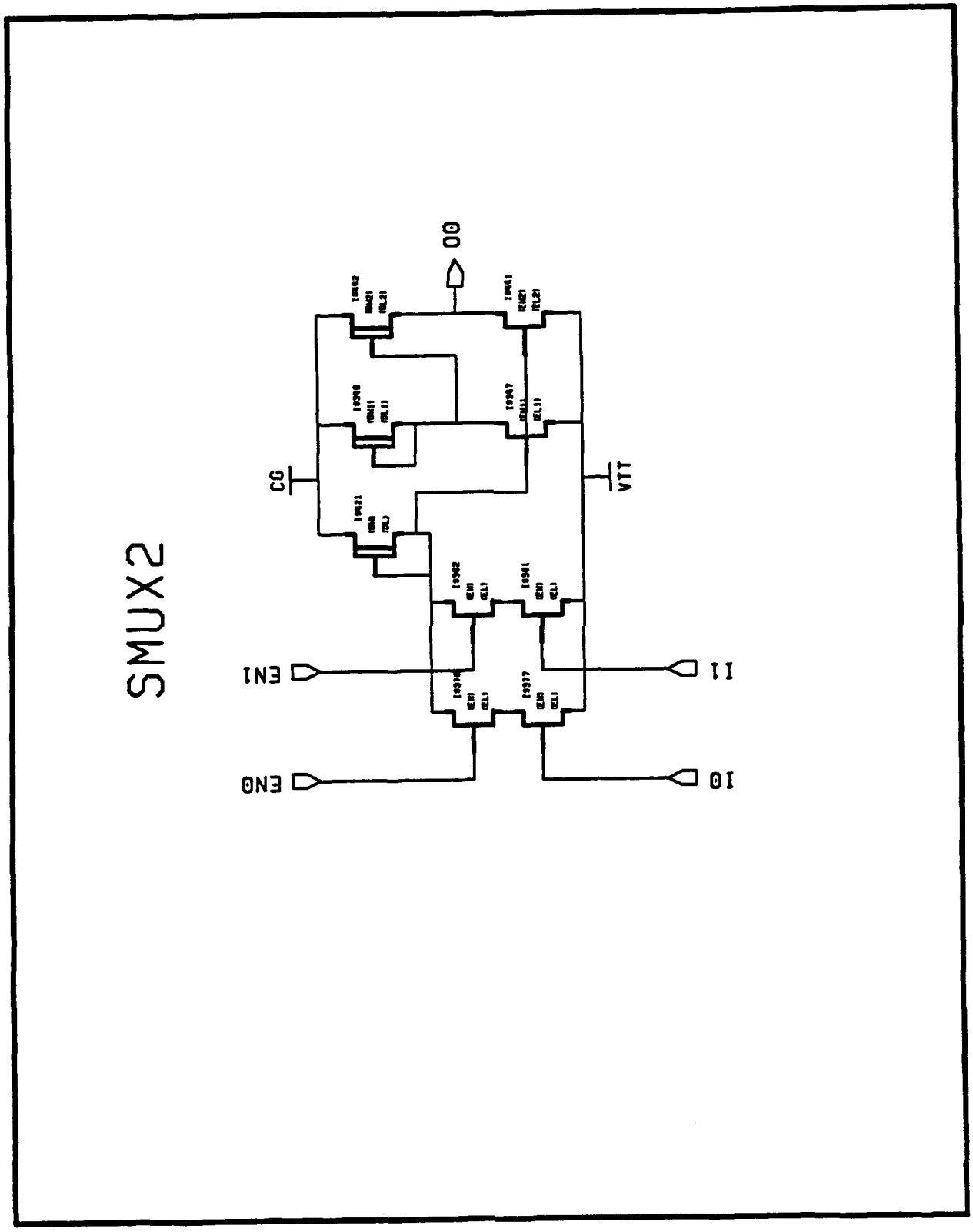

SSS
0 0 1 0 00
00
out
8.2
S
I#
SINV
4.5 1.5
50 1.2
2.5 7.0
6.0 1.2
NAND
IO
in
0.17
IO

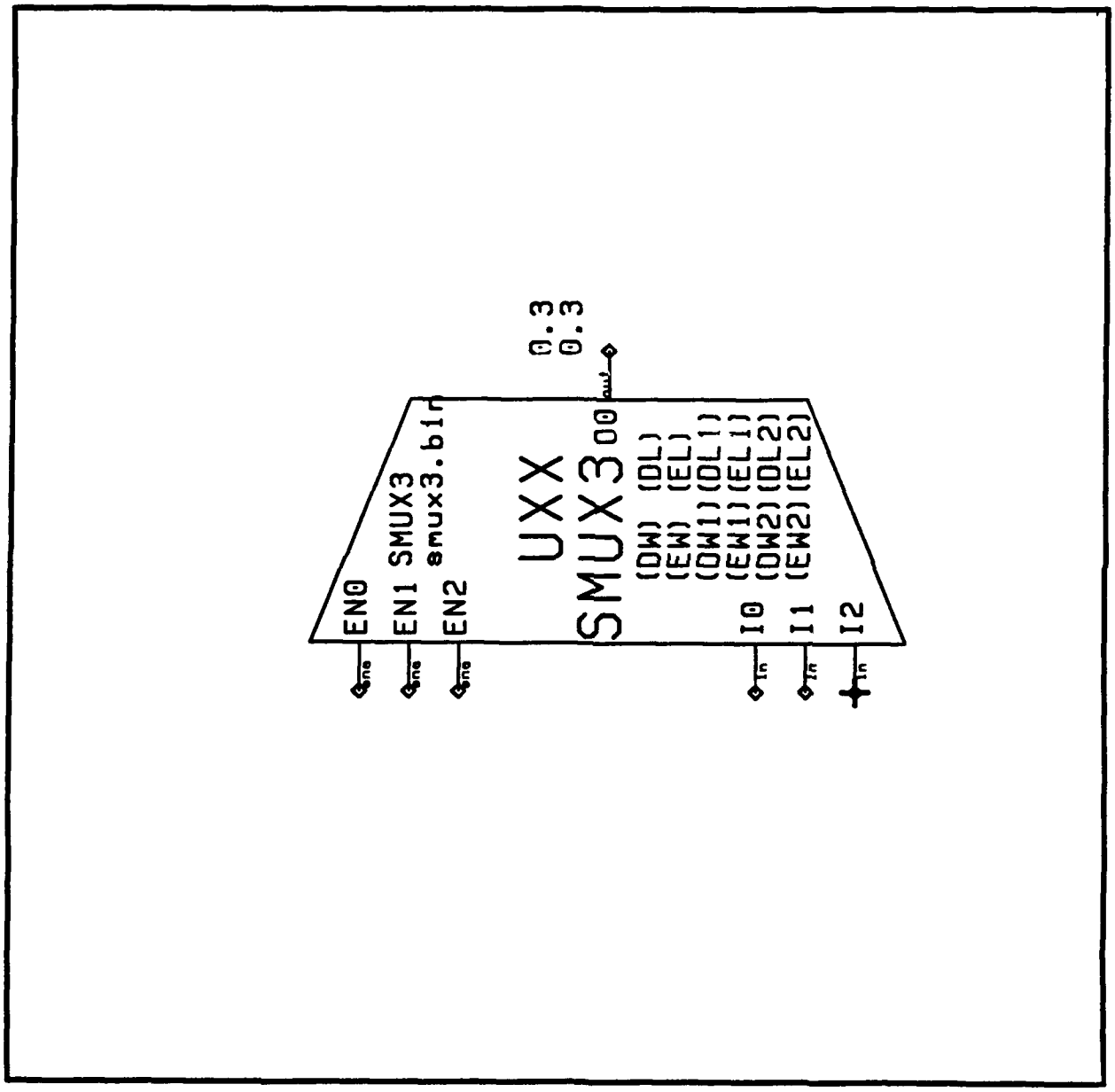

O0
CG
4.5
1.5
I$22
50
1.2
VTT
I$21
SINVSMALL
APPROXIMATELY 500uW OF POWER
CG
2.5
7.0
I$1
6.0
1.2
VTT
I$3
I0

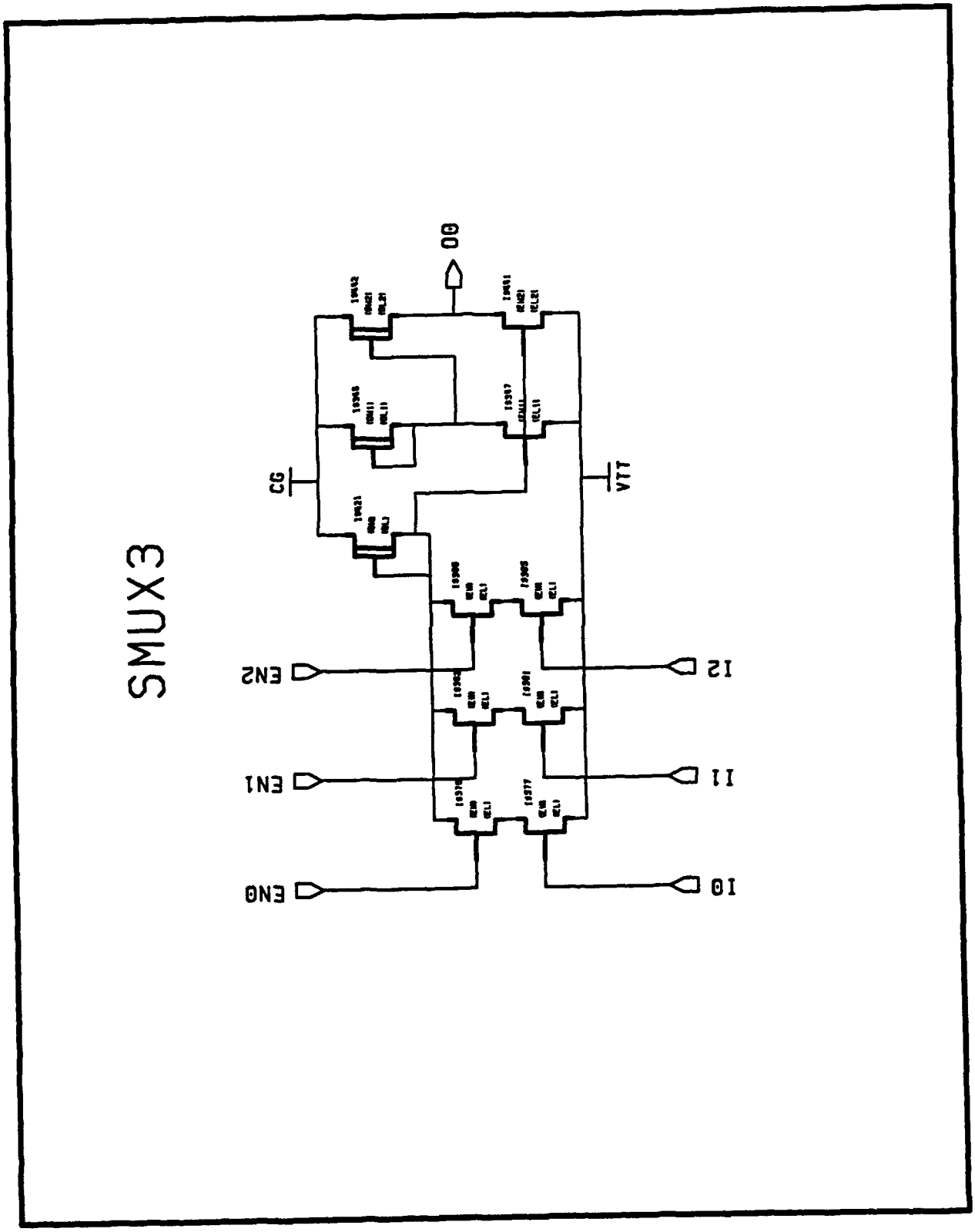

UXX
SMUX
A(15:0)
B(15:0)
B(15:0)
SSELA
SSELB
SSELC
SSELZL
SSELINV
SOUT(15:0)

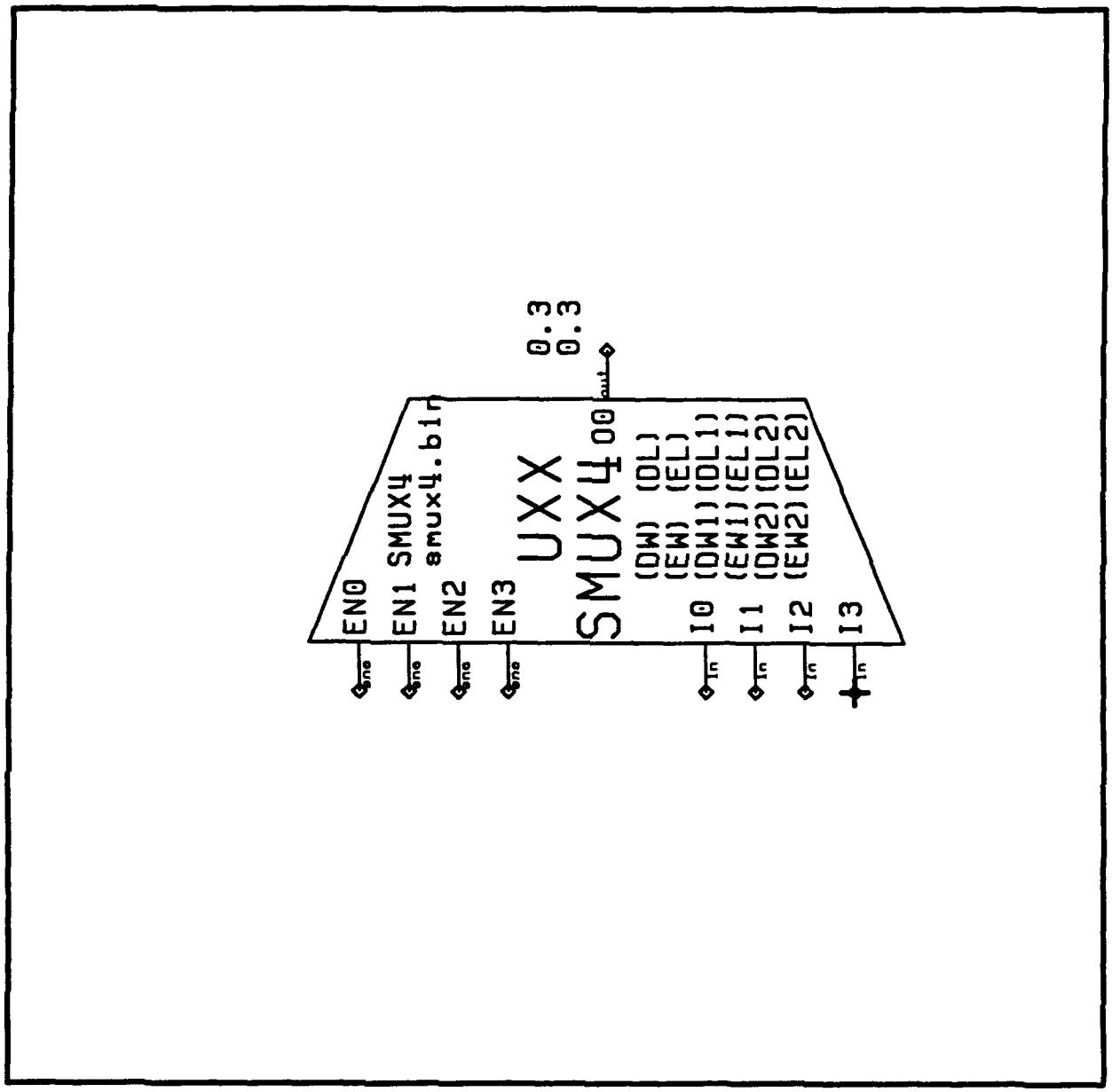

SMUX
SOUT (I)
SSELINV
A (I)
SSELA
B (I)
SSELB
Q (I)
SSELQ
SSELZL
FOR I := 0 TO 15

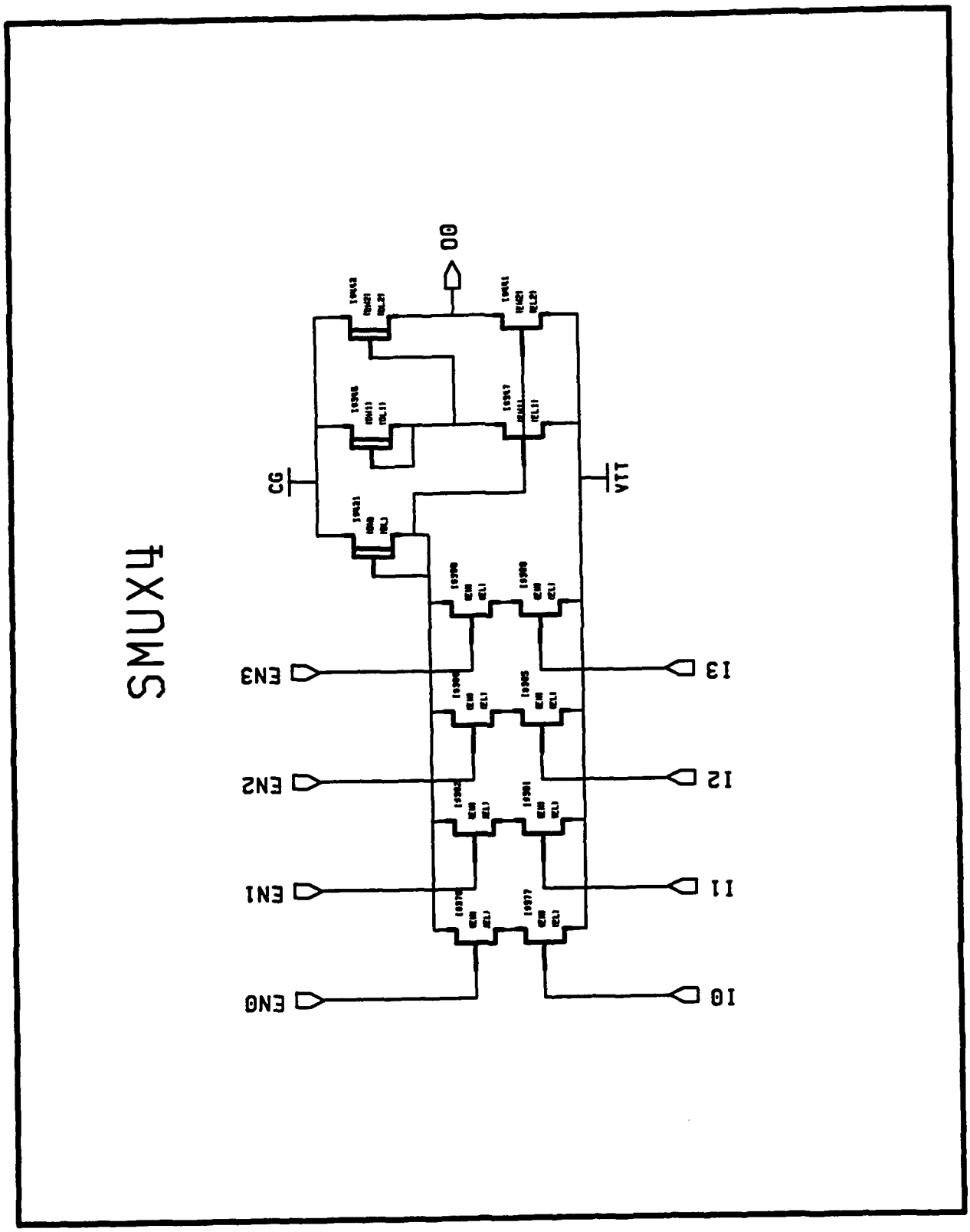

0.3
0.3
UXX
SMUX200
EN0
EN1 SMUX2
smux2.bin
(OW) (OL)
(EW) (EL)
(OW1)(OL1)
(EW1)(EL1)
(OW2)(OL2)
(EW2)(EL2)
I0
I1

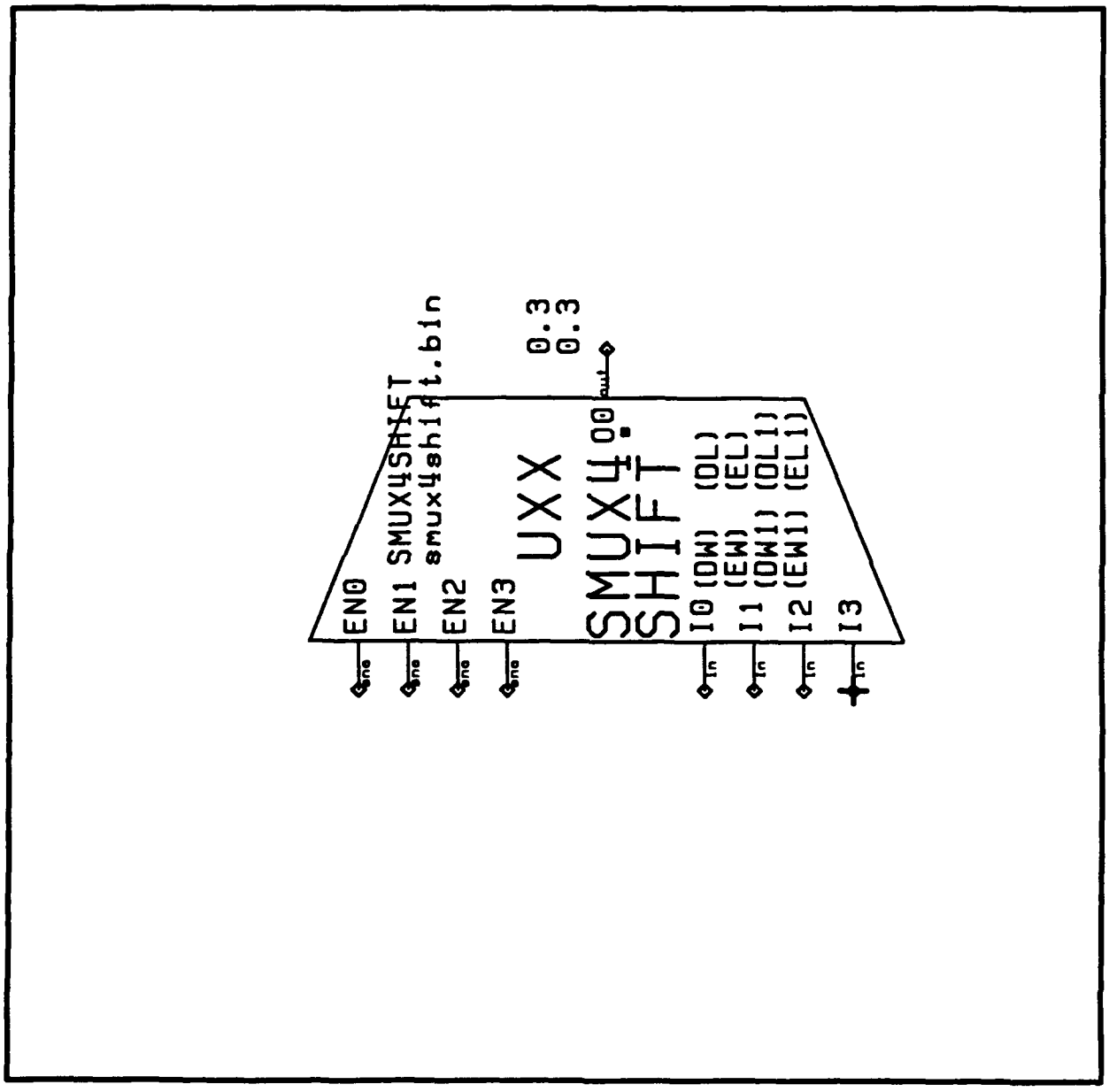

SMUX2
O0
CG
VTT
EN1
I1
EN0
I0

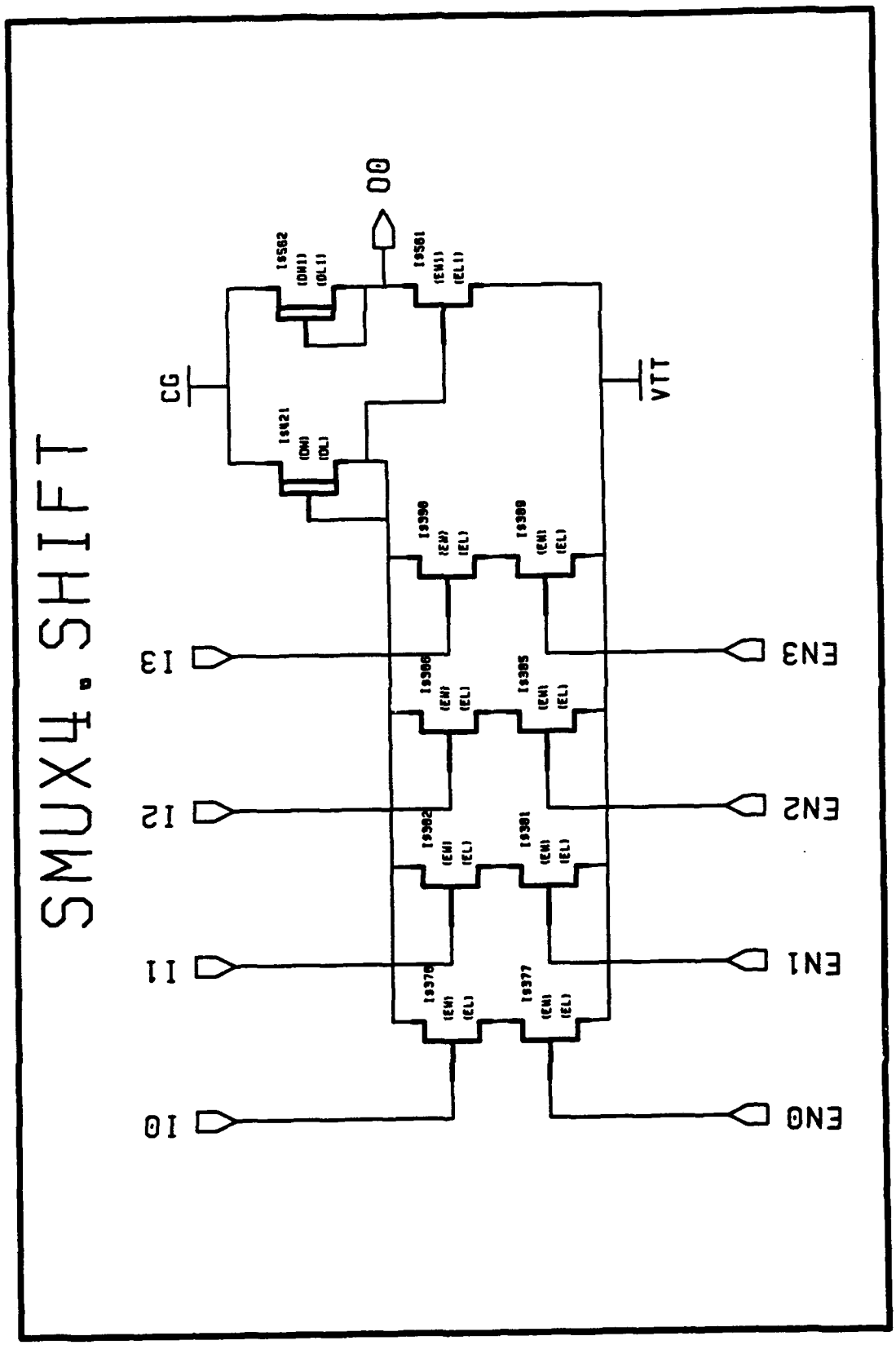

0.3
0.3
UXX
SMUX3 00
smux3.bin
SMUX3
EN0
EN1
EN2
(DW) (DL)
(EW) (EL)
(DW1)(DL1)
(EW1)(EL1)
(DW2)(DL2)
(EW2)(EL2)
I0
I1
I2

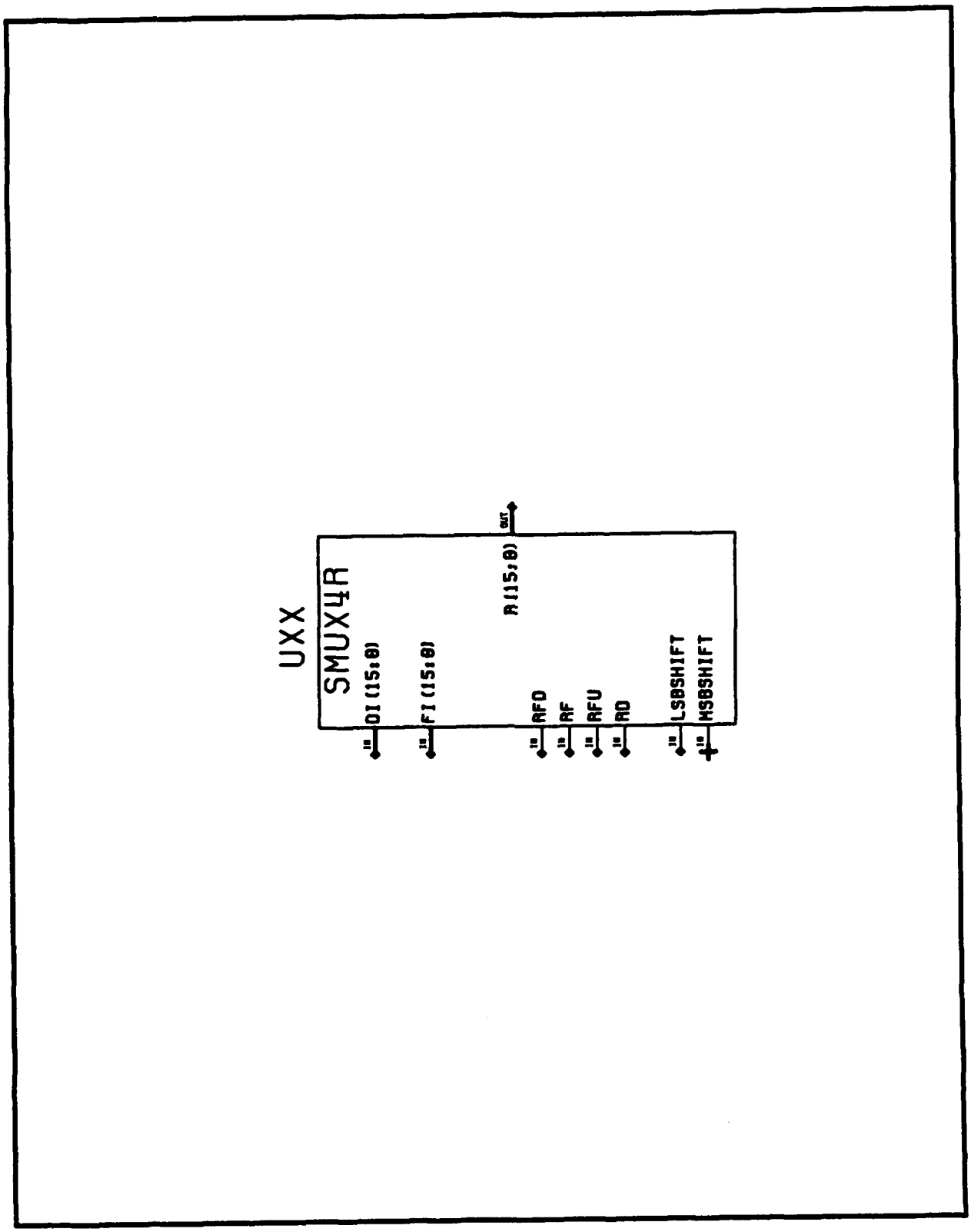

SMUX3
O0
CG
VTT
EN2
EN1
EN0
I2
I1
I0

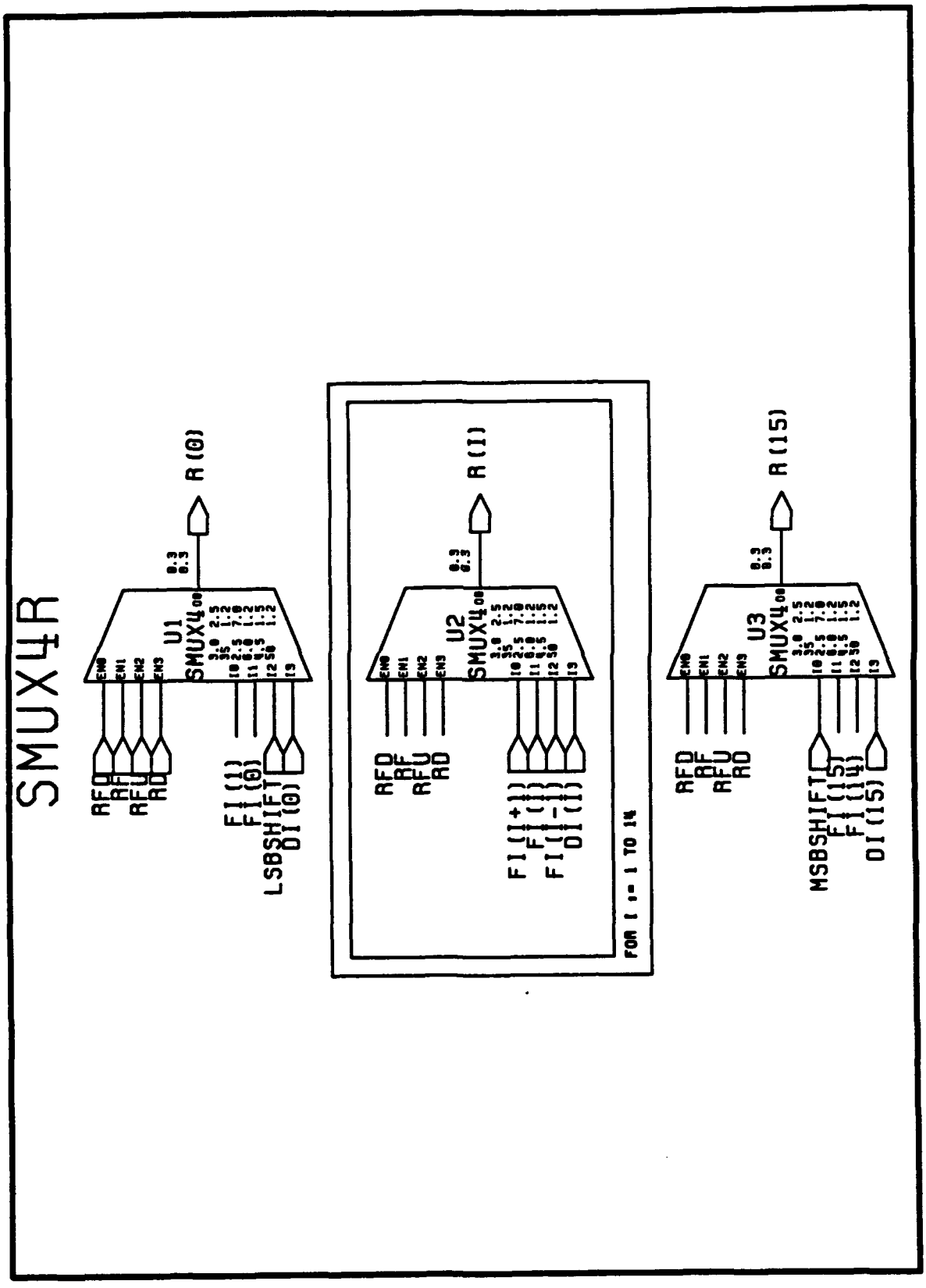

0.3
0.3
UXX
SMUX400
smux4.bin
SMUX4
EN0
EN1
EN2
EN3
(DW) (DL)
(EW) (EL)
(DW1)(DL1)
(EW1)(EL1)
(DW2)(DL2)
(EW2)(EL2)
I0
I1
I2
I3
ena
in

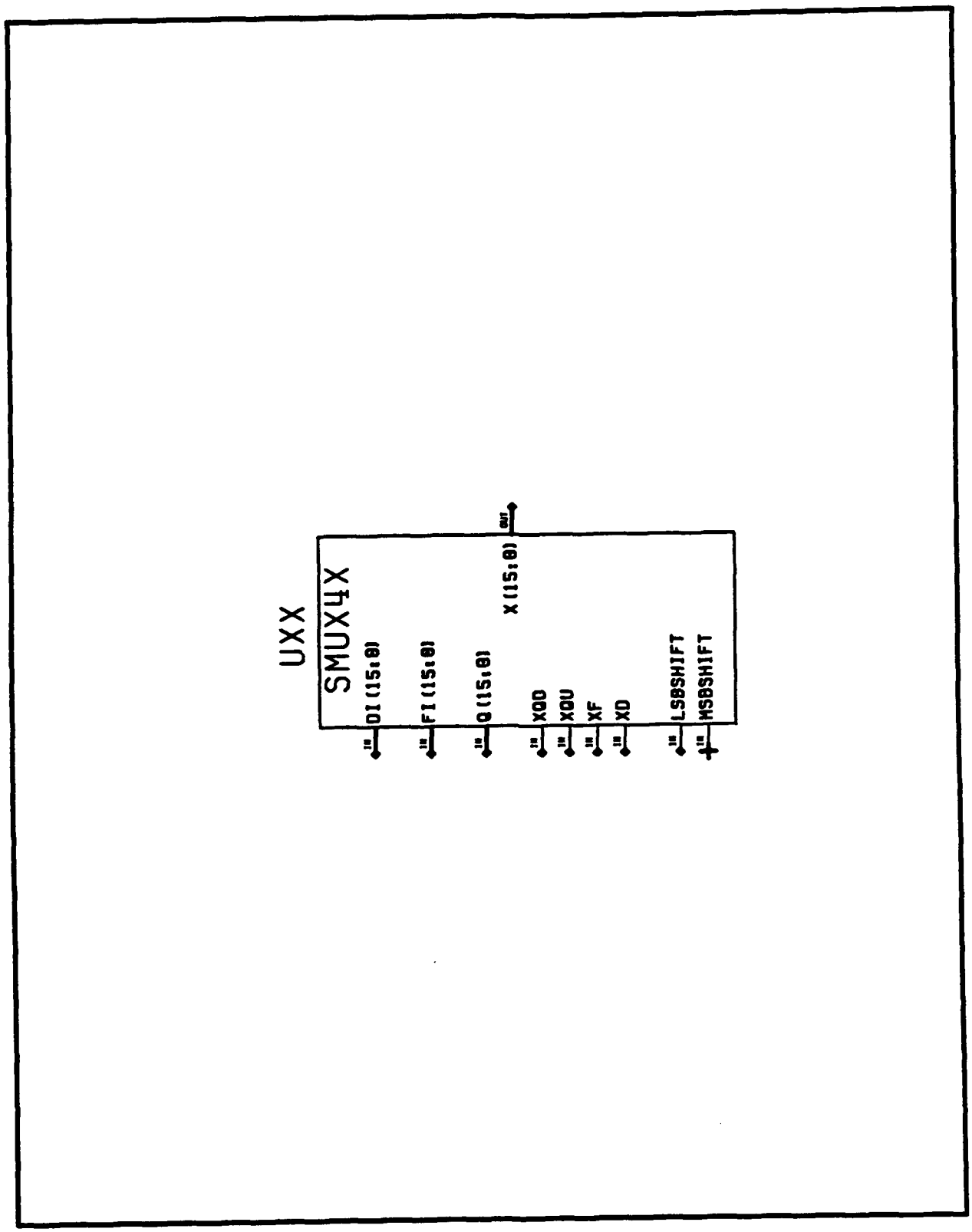

SMUX4
O0
CG
VTT
EN3
EN2
EN1
EN0
I3
I2
I1
I0

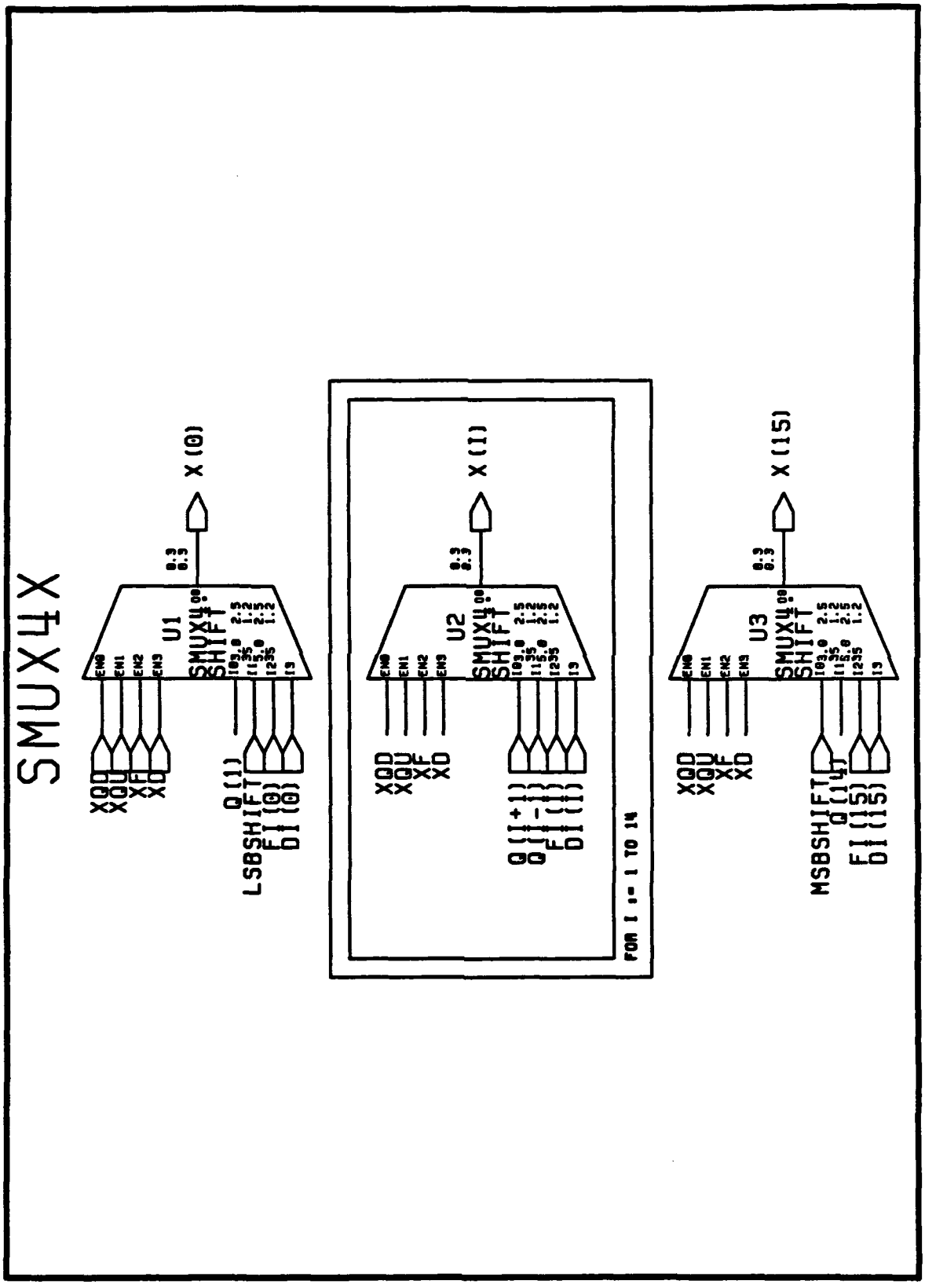

0.3
0.3
smux4shift.bin
SMUX4SHIFT
UXX
SMUX4.00
SHIFT
EN0
EN1
EN2
EN3
I0 (OW) (OL)
I1 (EW) (EL)
I2 (EW1) (OL1)
I3 (EL1)

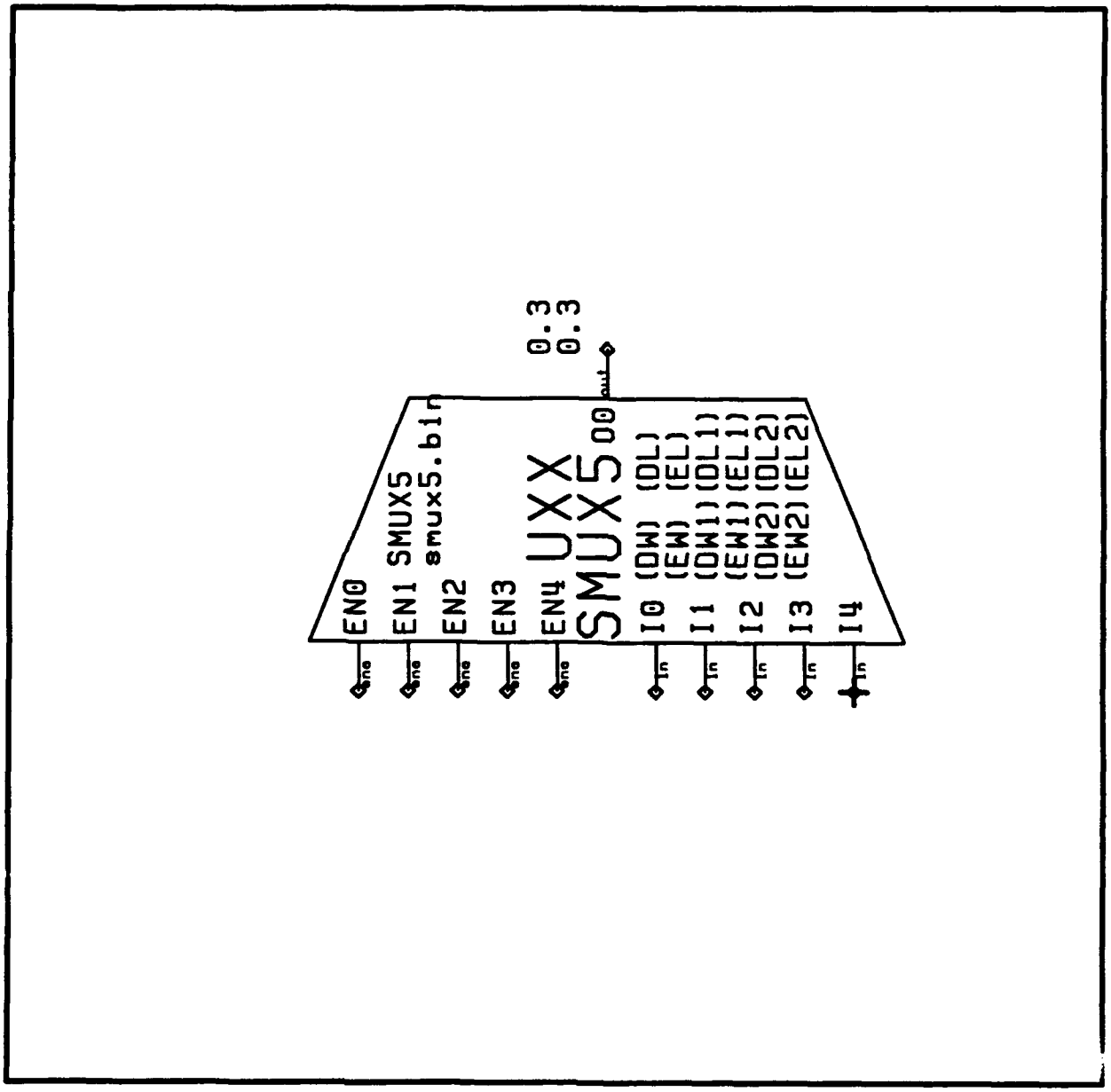

SMUX4.SHIFT
O0
CG
VTT
I3
I2
I1
I0
EN3
EN2
EN1
EN0

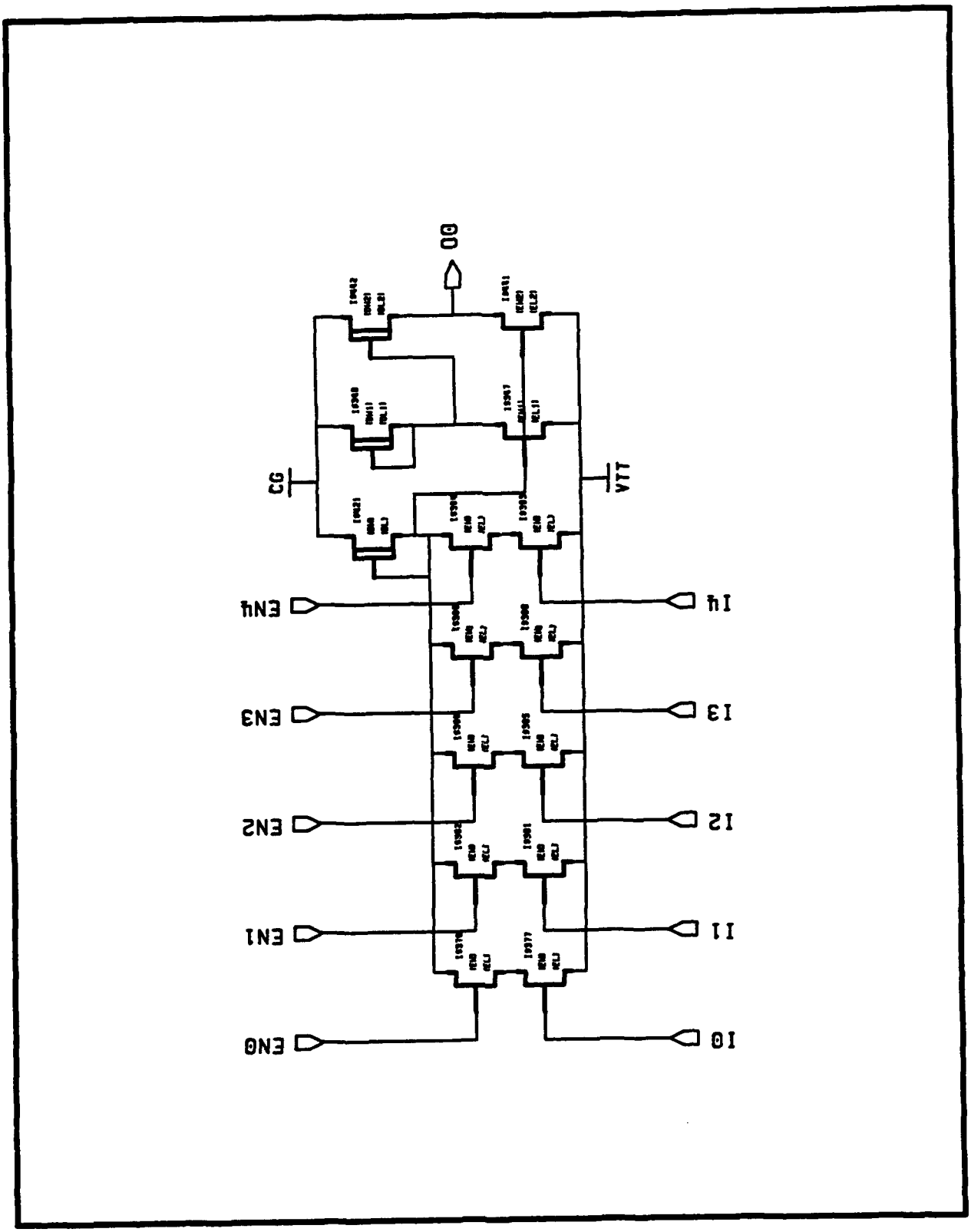

UXX
SMUX4R
DI(15:0)
FI(15:0)
R(15:0)
OUT
RFD
RF
RFU
RD
LSBSHIFT
MSBSHIFT

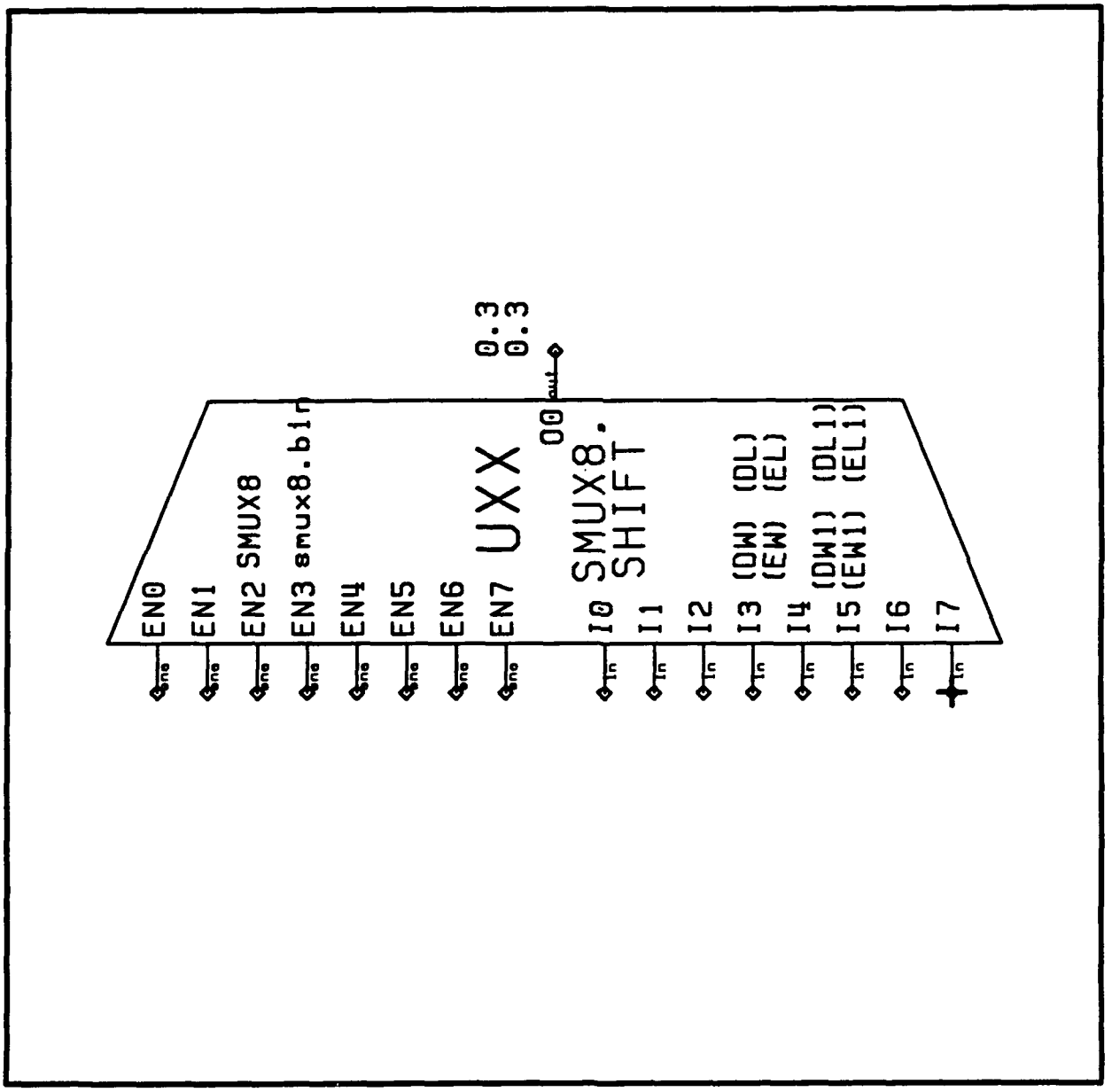

SMUX4R
U1
SMUX4
R(0)
RFD
RF
RFU
RD
FI(1)
FI(0)
LSBSHIFT
DI(0)
U2
SMUX4
R(1)
FI(I+1)
FI(I)
FI(I-1)
DI(I)
FOR I := 1 TO 14
U3
SMUX4
R(15)
MSBSHIFT
FI(15)
FI(14)
DI(15)

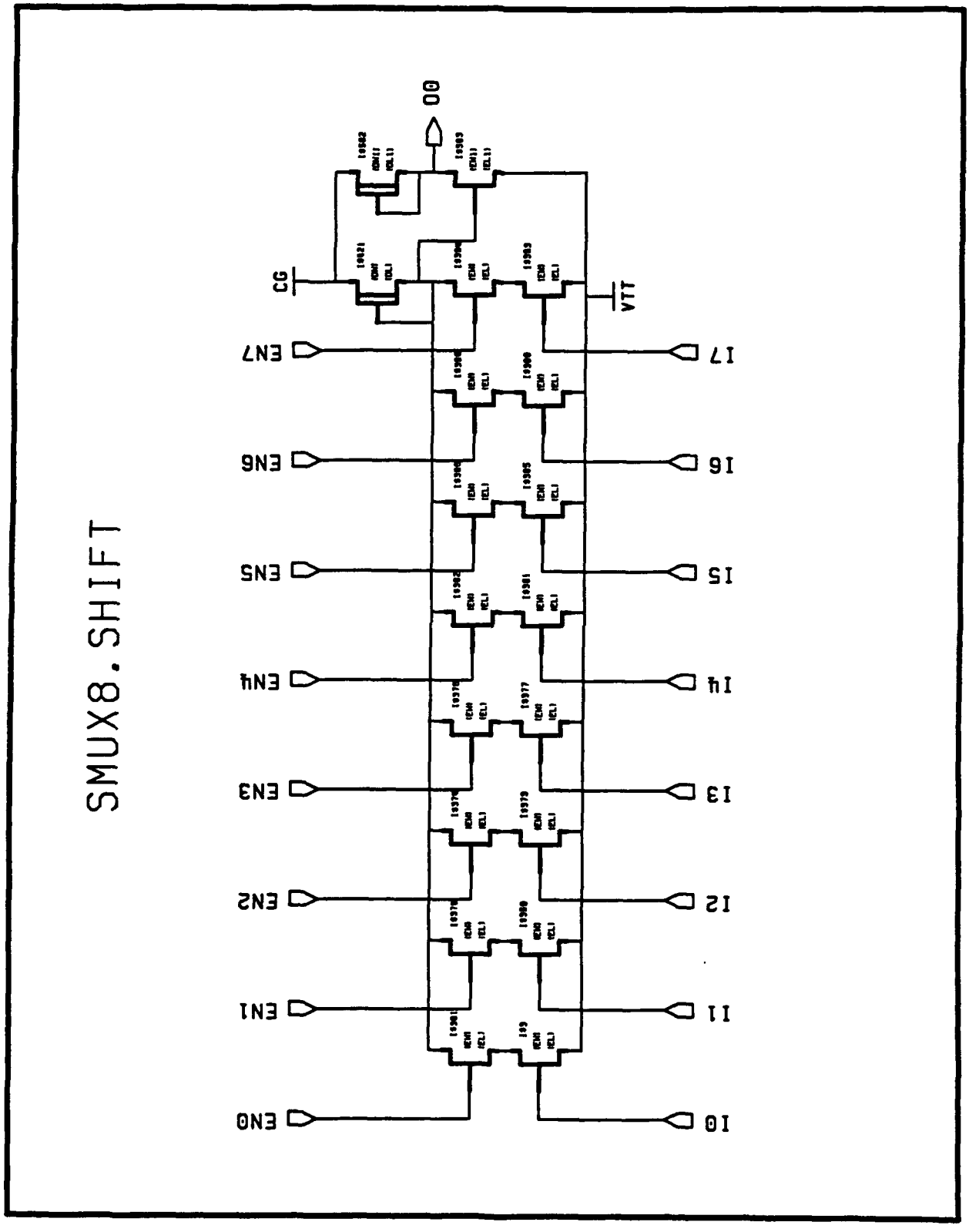

UXX
SMUX4X
DI(15:0)
FI(15:0)
QI(15:0)
XQD
XQU
XF
XD
X(15:0)
LSBSHIFT
MSBSHIFT

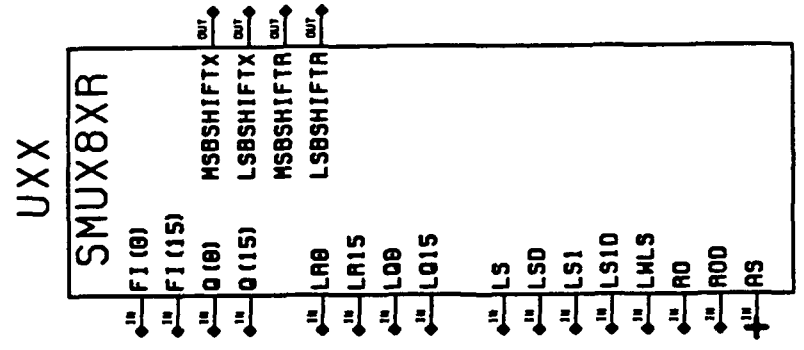

SMUX4X
X(0)
X(1)
X(15)
U1
U2
U3
SMUX4
SHIFT
XOD
XQU
XF
XO
Q(1)
LSBSHIFT
FI(0)
DI(0)
Q(I+1)
Q(I-1)
FI(I)
DI(I)
MSBSHIFT
Q(14)
FI(15)
DI(15)
FOR I := 1 TO 14

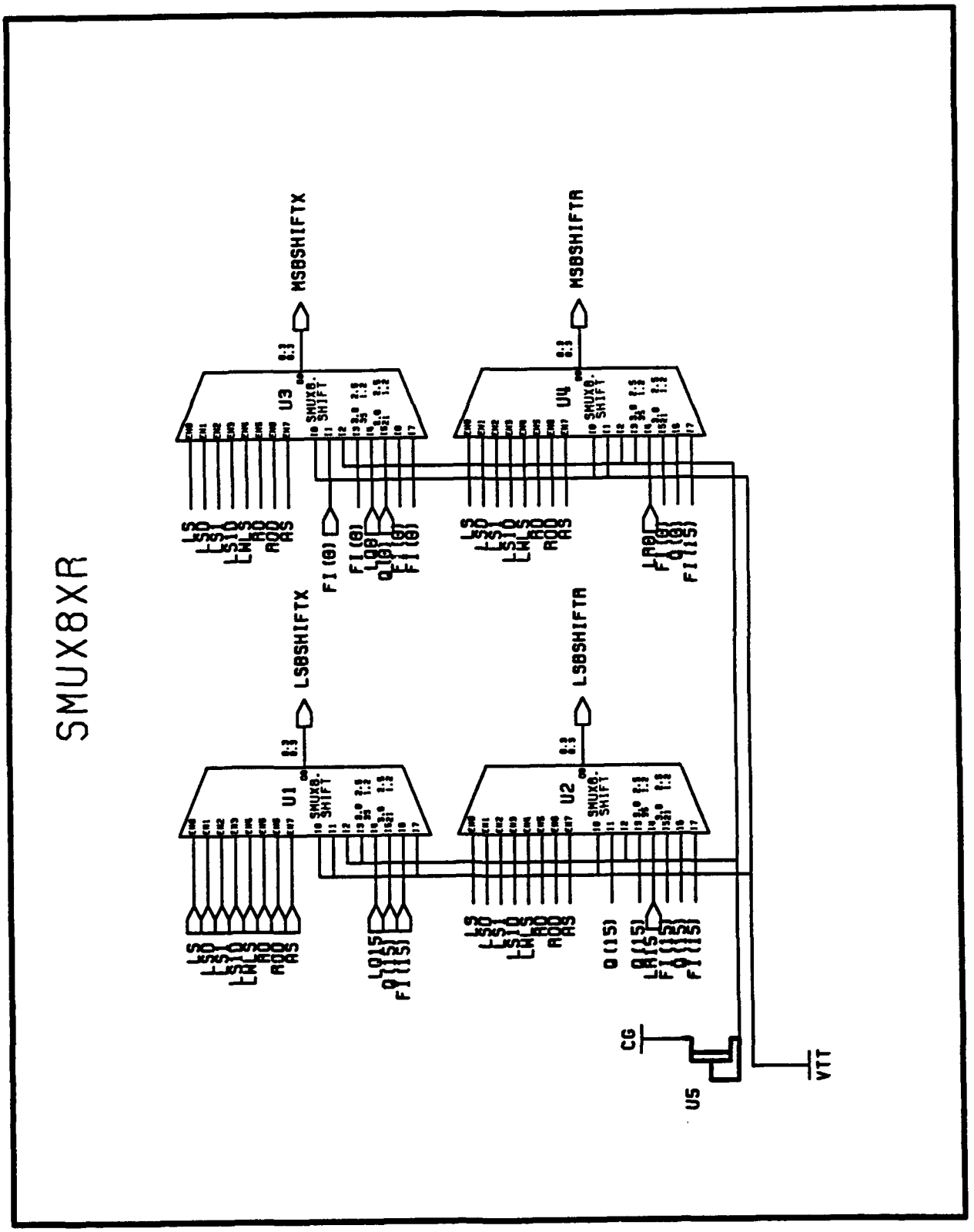

0.3
0.3
SMUX5
smux5.bin
UXX
SMUX500
EN0
EN1
EN2
EN3
EN4
I0 (0W) (0L)
(EW) (EL)
I1 (0W1) (0L1)
(EW1) (EL1)
I2 (0W2) (0L2)
I3 (EW2) (EL2)
I4

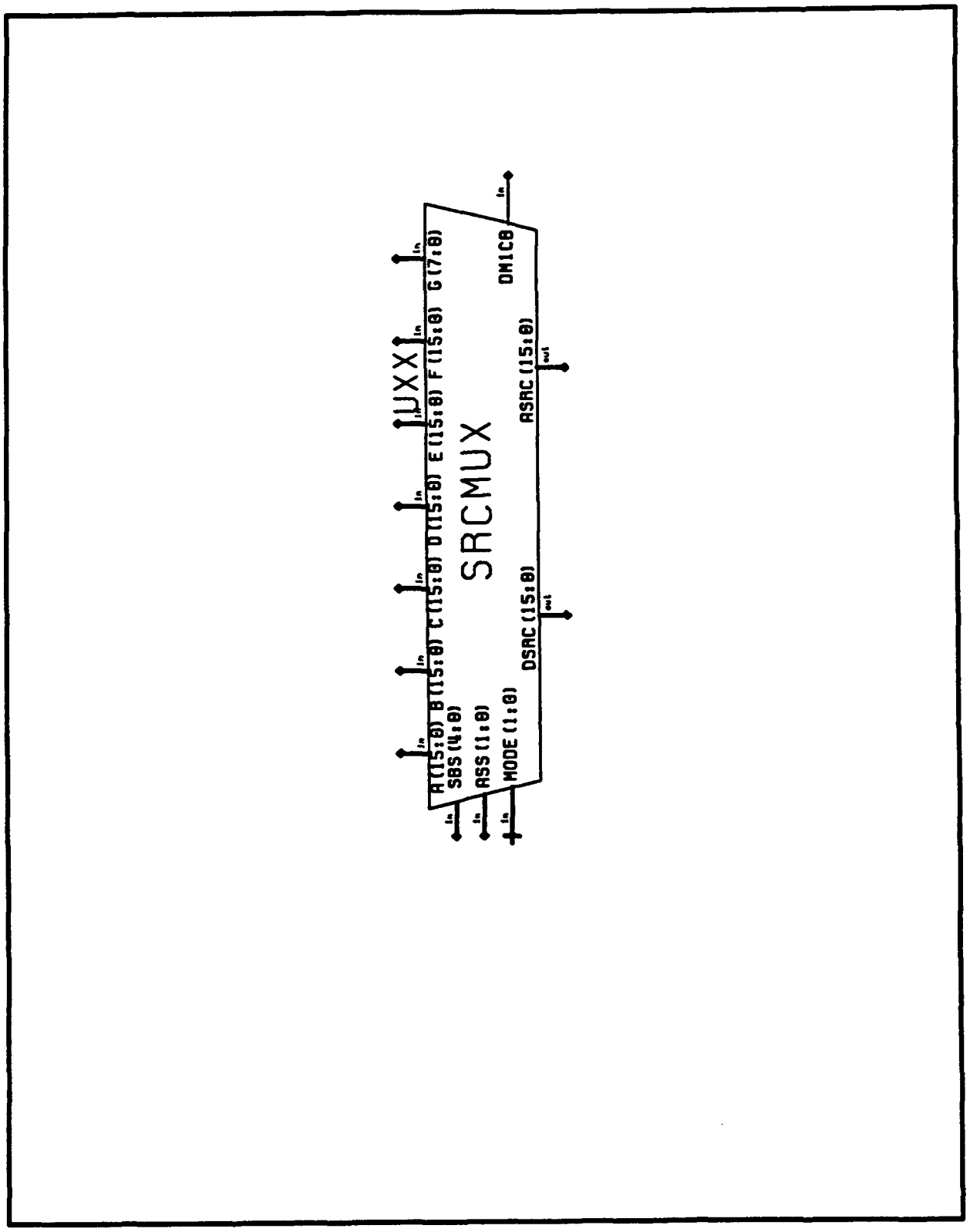

O0
CG
VTT
EN4
EN3
EN2
EN1
EN0
I4
I3
I2
I1
I0

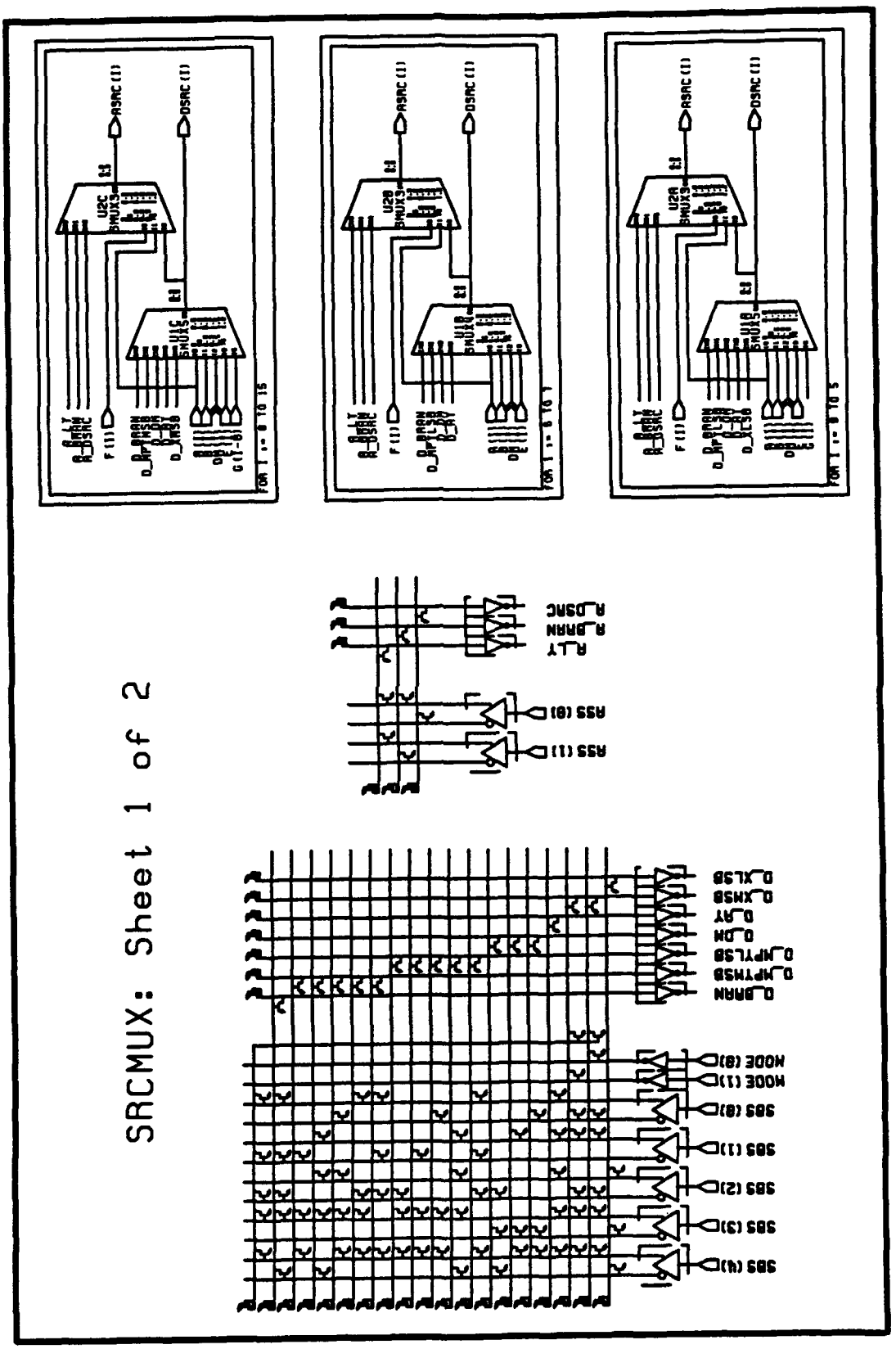

0.3
0.3
O0
SMUX8.
SHIFT
UXX
smux8.bin
SMUX8
EN0
EN1
EN2
EN3
EN4
EN5
EN6
EN7
I0
I1
I2
I3 (DW) (DL)
(EW) (EL)
I4
I5 (DW1) (DL1)
(EW1) (EL1)
I6
I7

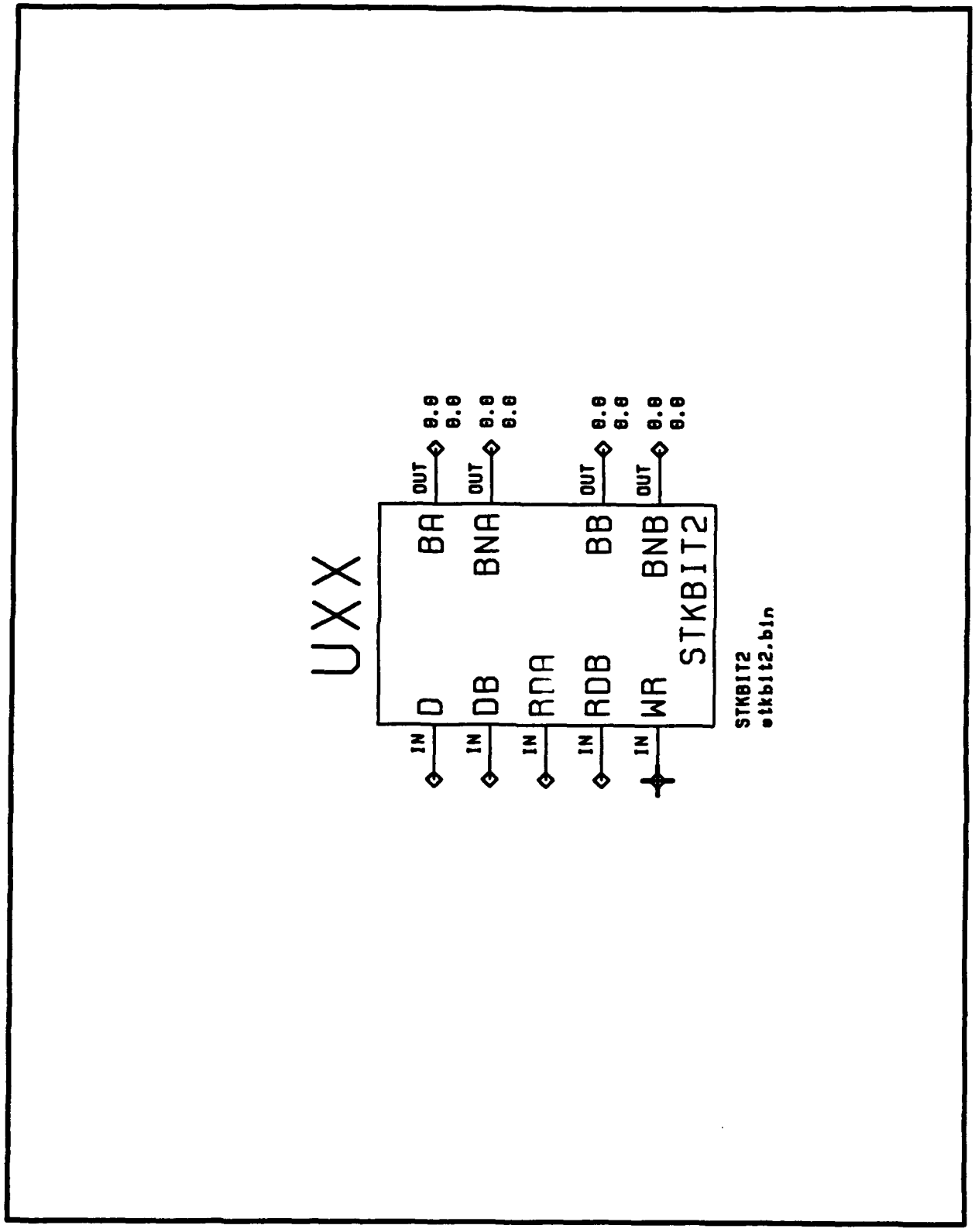

SMUX8.SHIFT
O0
CG
VTT
EN7
EN6
EN5
EN4
EN3
EN2
EN1
EN0
I7
I6
I5
I4
I3
I2
I1
I0

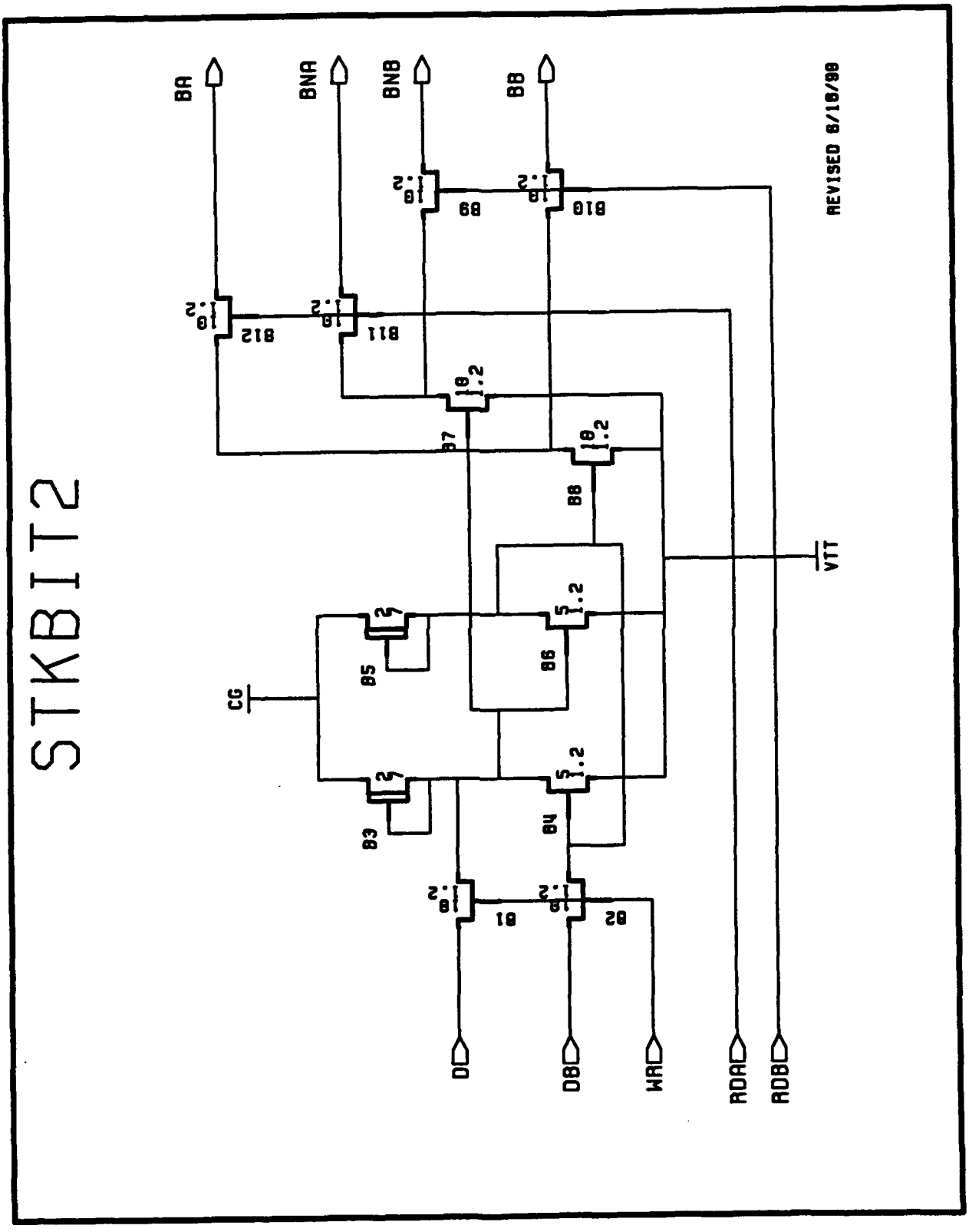

UXX
SMUX8XR
F1(0)
F1(15)
Q(0)
Q(15)
MSBSHIFTX
LSBSHIFTX
MSBSHIFTR
LSBSHIFTR
LR0
LR15
LQ0
LQ15
LS
LSD
LS1
LS10
LWLS
RO
ROD
AS
IN
OUT

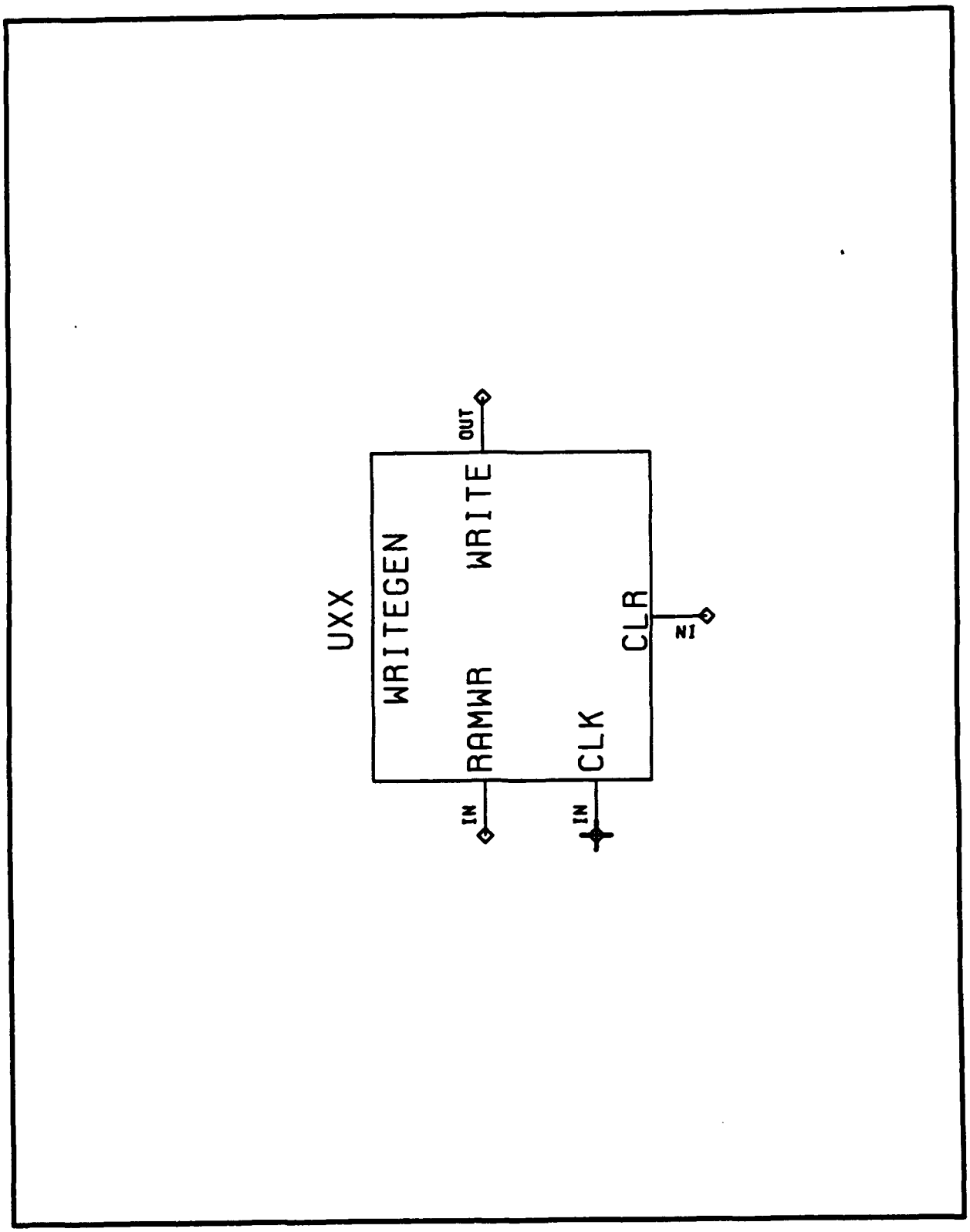

SMUX8XR
MSBSHIFTX
MSBSHIFTA
LSBSHIFTX
LSBSHIFTA
U1
U2
U3
U4
U5
SMUX8-SHIFT
CG
VTT


SRCMUX
4WXX
A(15:0)
B(15:0)
C(15:0)
D(15:0)
E(15:0)
F(15:0)
G(7:0)
SBS(4:0)
ASS(1:0)
MODE(1:0)
DMICB
ASRC(15:0)
DSRC(15:0)

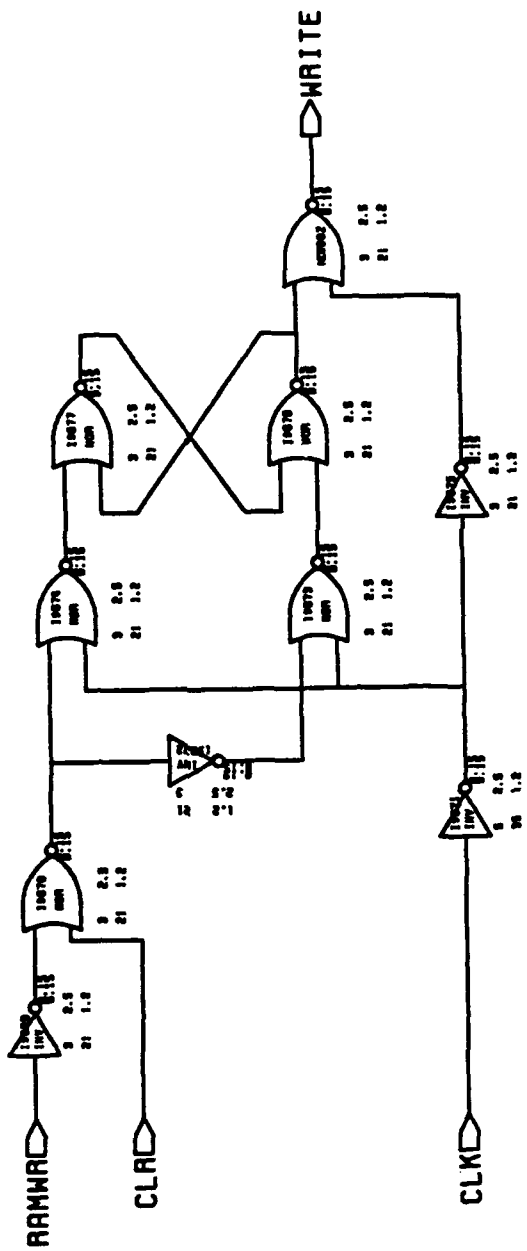

SRCMUX: Sheet 1 of 2
R_LY
R_BRAN
R_DSRC
RSS (0)
RSS (1)
D_XLSB
D_XMSB
D_LY
D_DM
D_MPYLSB
D_MPYMSB
D_BRAN
MODE (0)
MODE (1)
SBS (0)
SBS (1)
SBS (2)
SBS (3)
SBS (4)

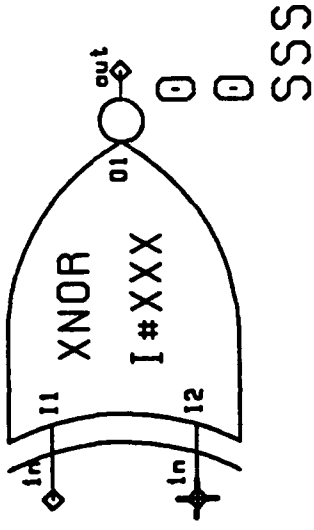

UXX
BA
BNA
BB
BNB
STKBIT2
D
DB
RDA
RDB
WR
OUT
IN
0.0
STKBIT2
stkbit2.bin

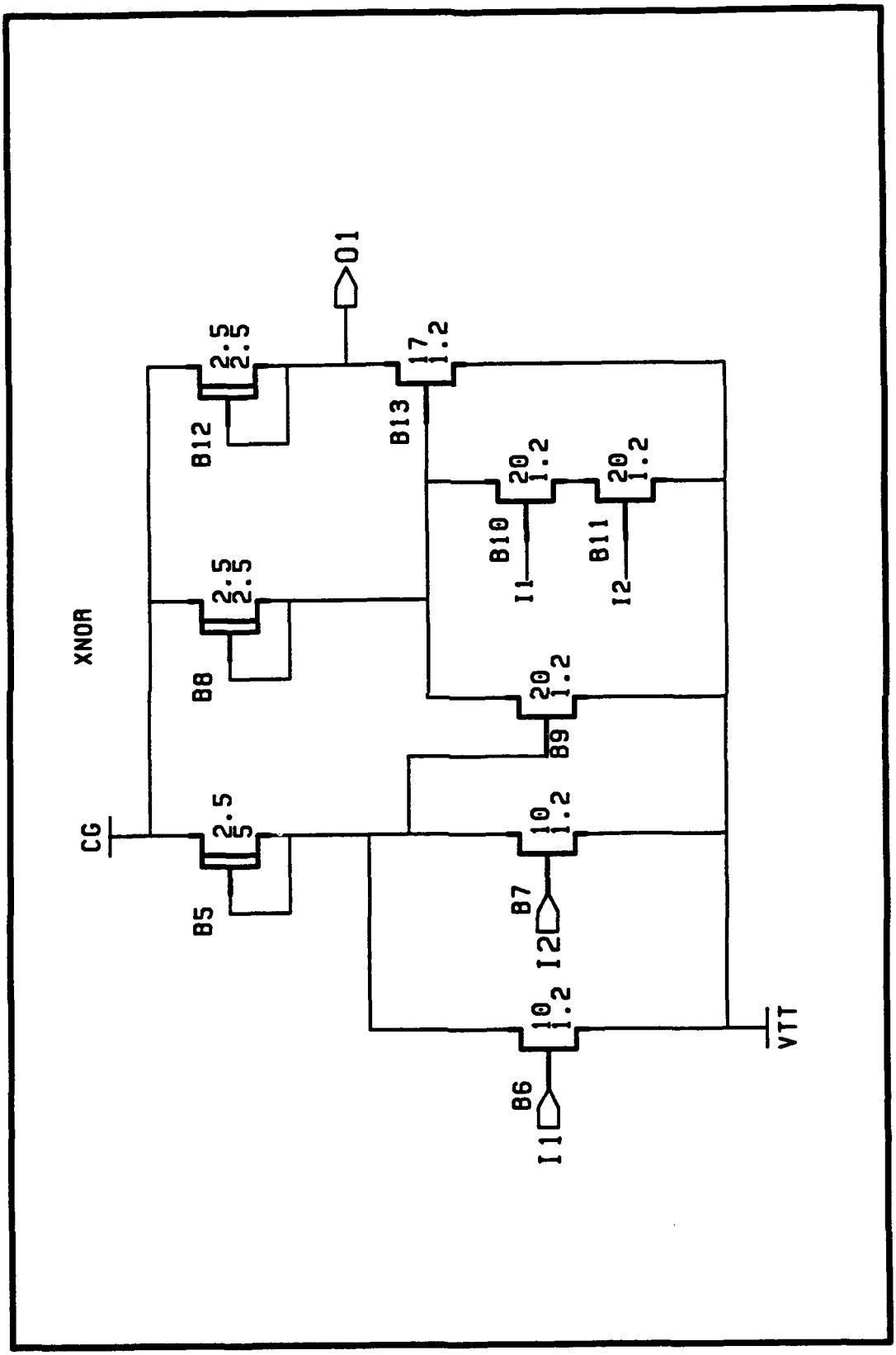

STKBIT2
BA
BNA
BNB
BB
REVISED 8/10/90
B9
B10
B12
B11
B7
B8
B5
B6
B3
B4
B1
B2
CG
VTT
D
DB
WR
RDA
RDB

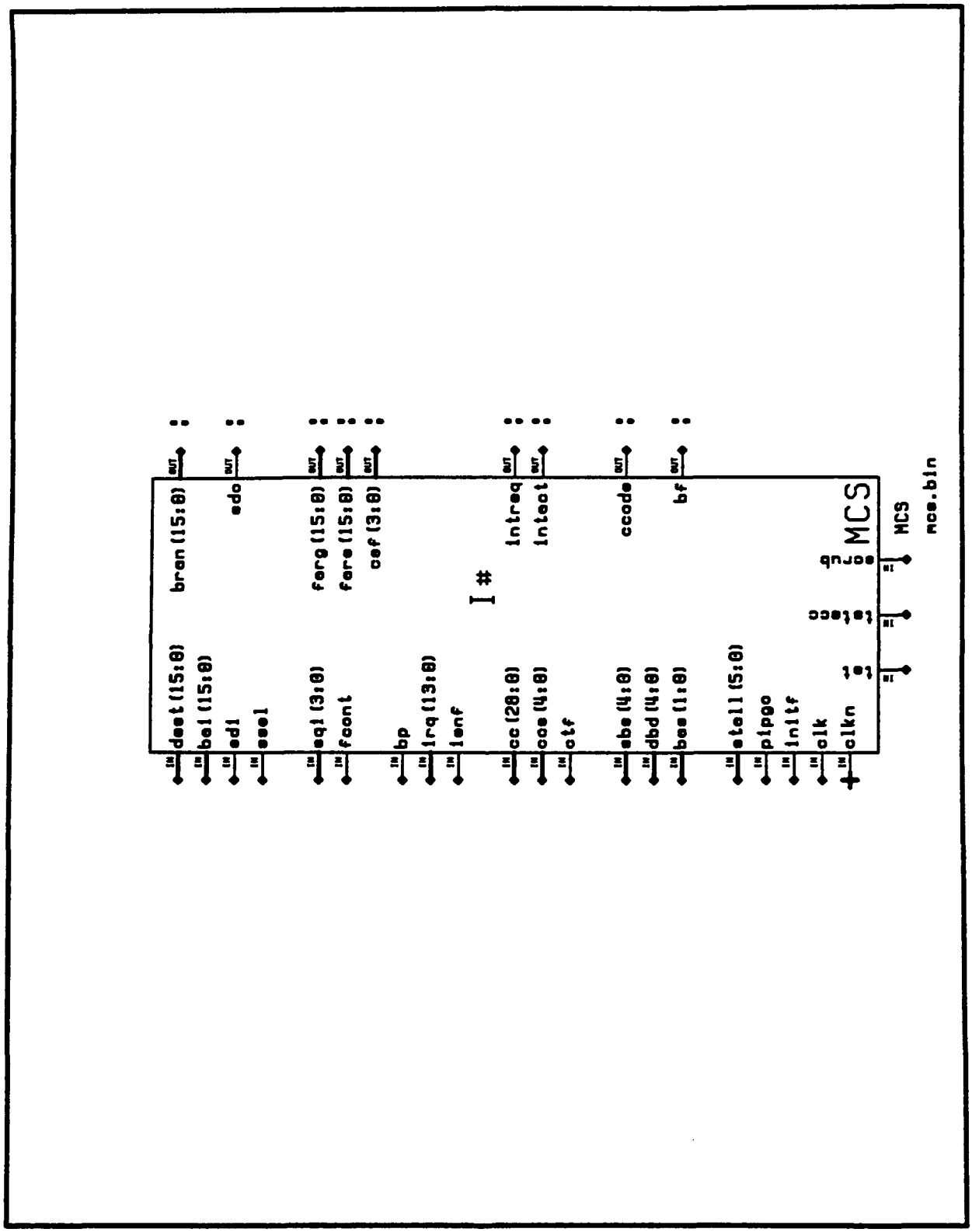

UXX
WRITEGEN
OUT
WRITE
RAMWR
IN
CLK
IN
CLR
N1

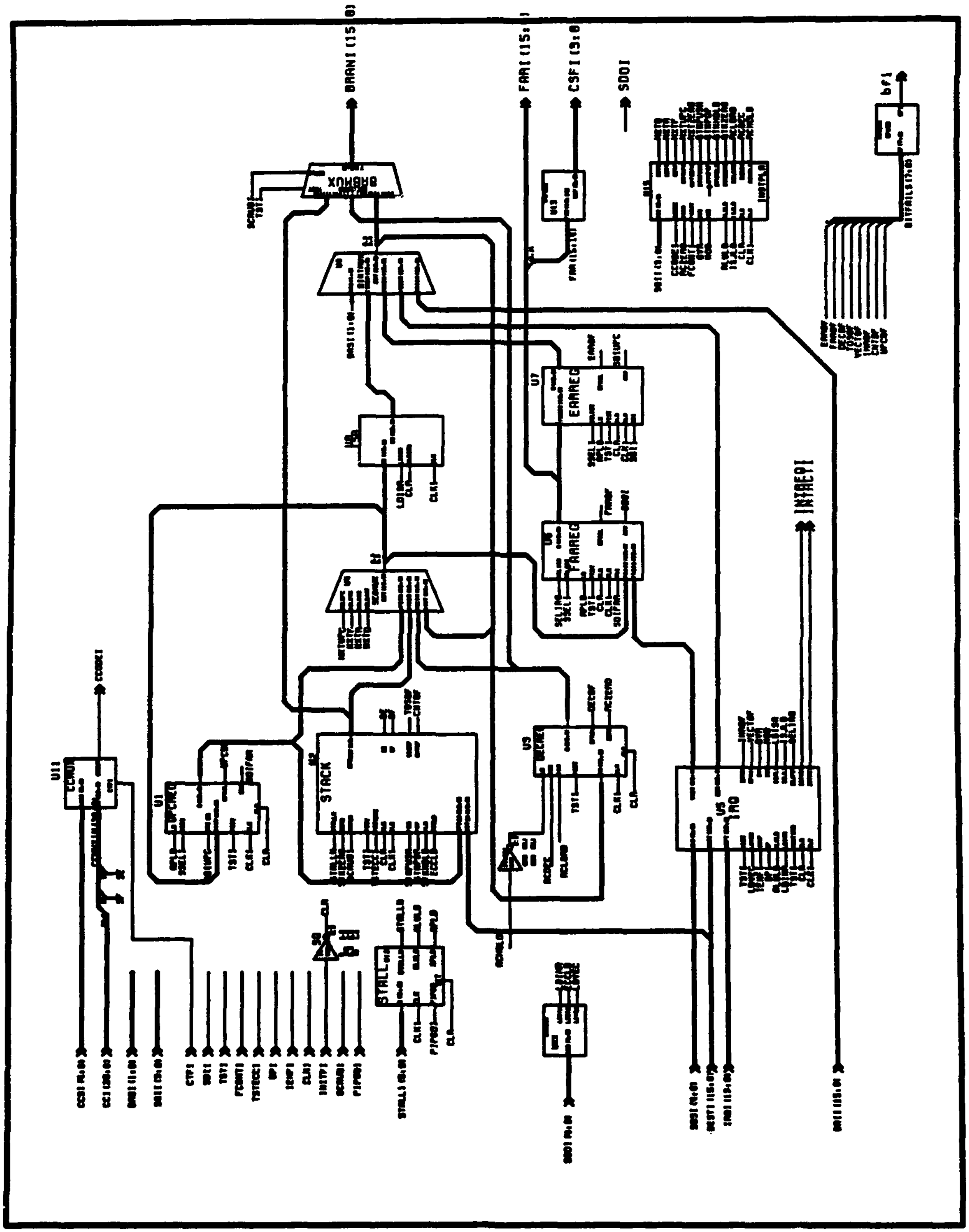
WRITEGEN: RAM WRITE PULSE GENERATOR

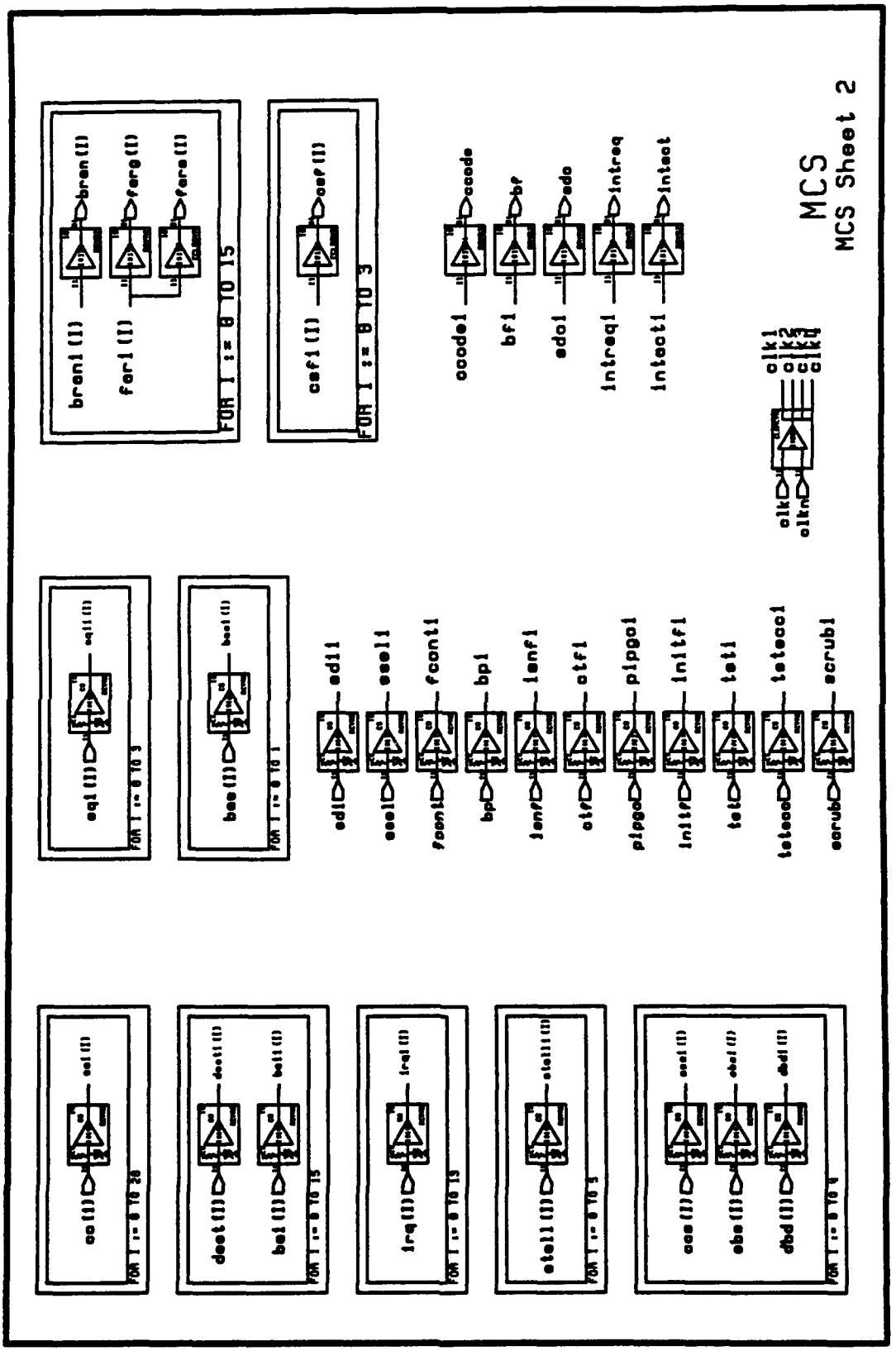


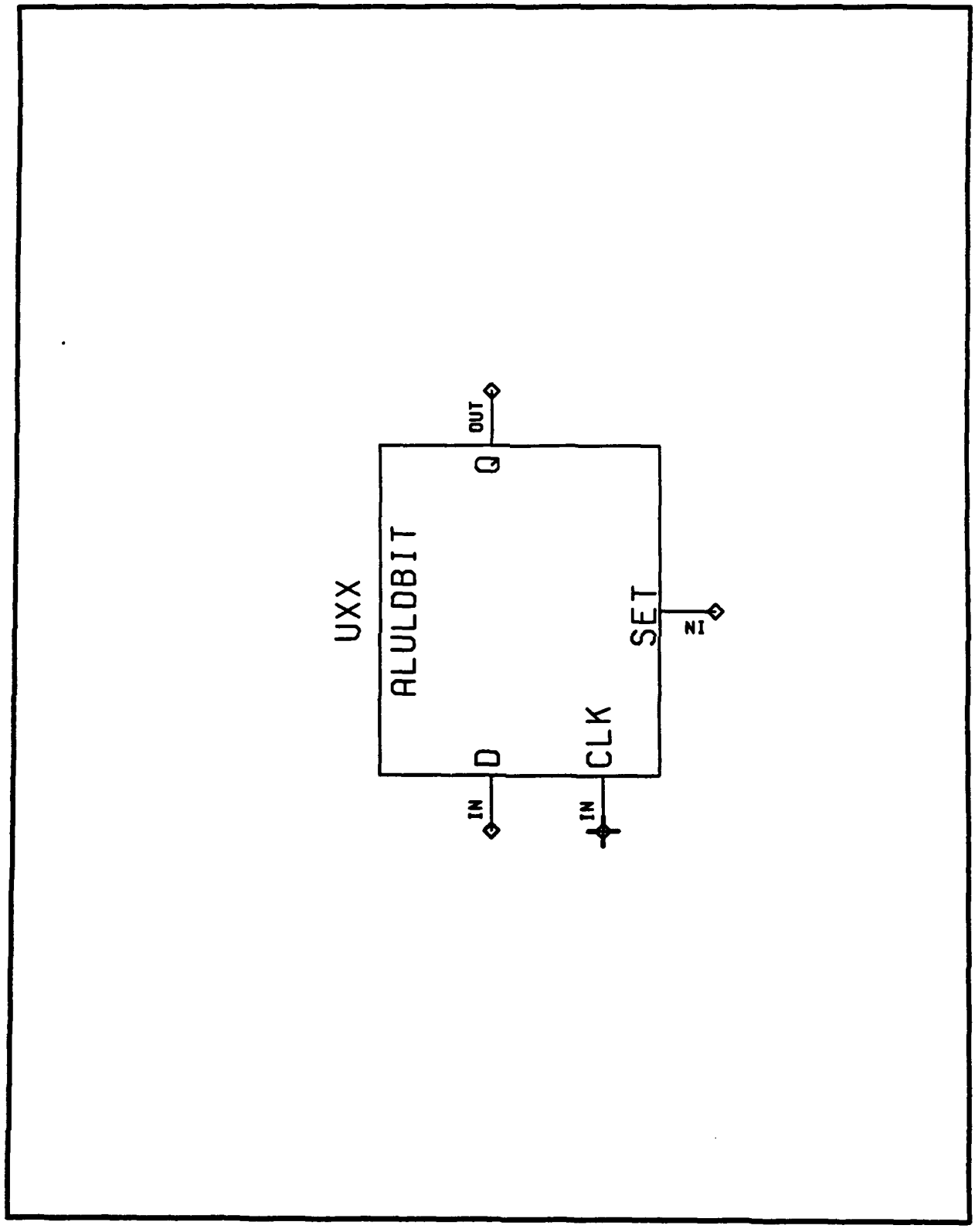

out
O
O
SSS
I0
I1
XNOR
I#XXX
I1
I2
In
In

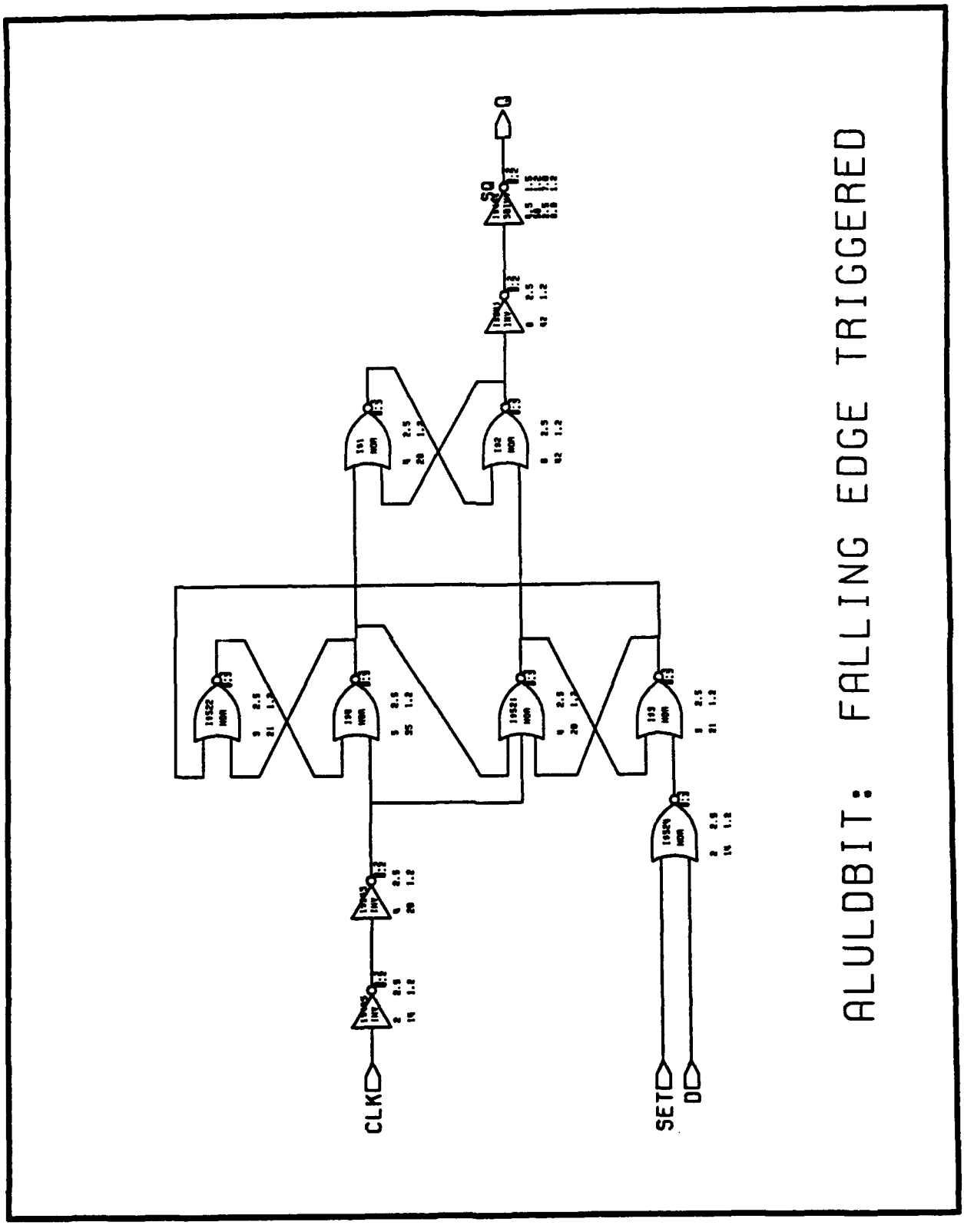

O1
2.5
2.5
B12
17
1.2
B13
20
1.2
B10
I1
20
1.2
B11
I2
XNOR
2.5
2.5
B8
20
1.2
B9
CG
2.5
2.5
B5
10
1.2
B7
I2
10
1.2
B6
I1
VTT

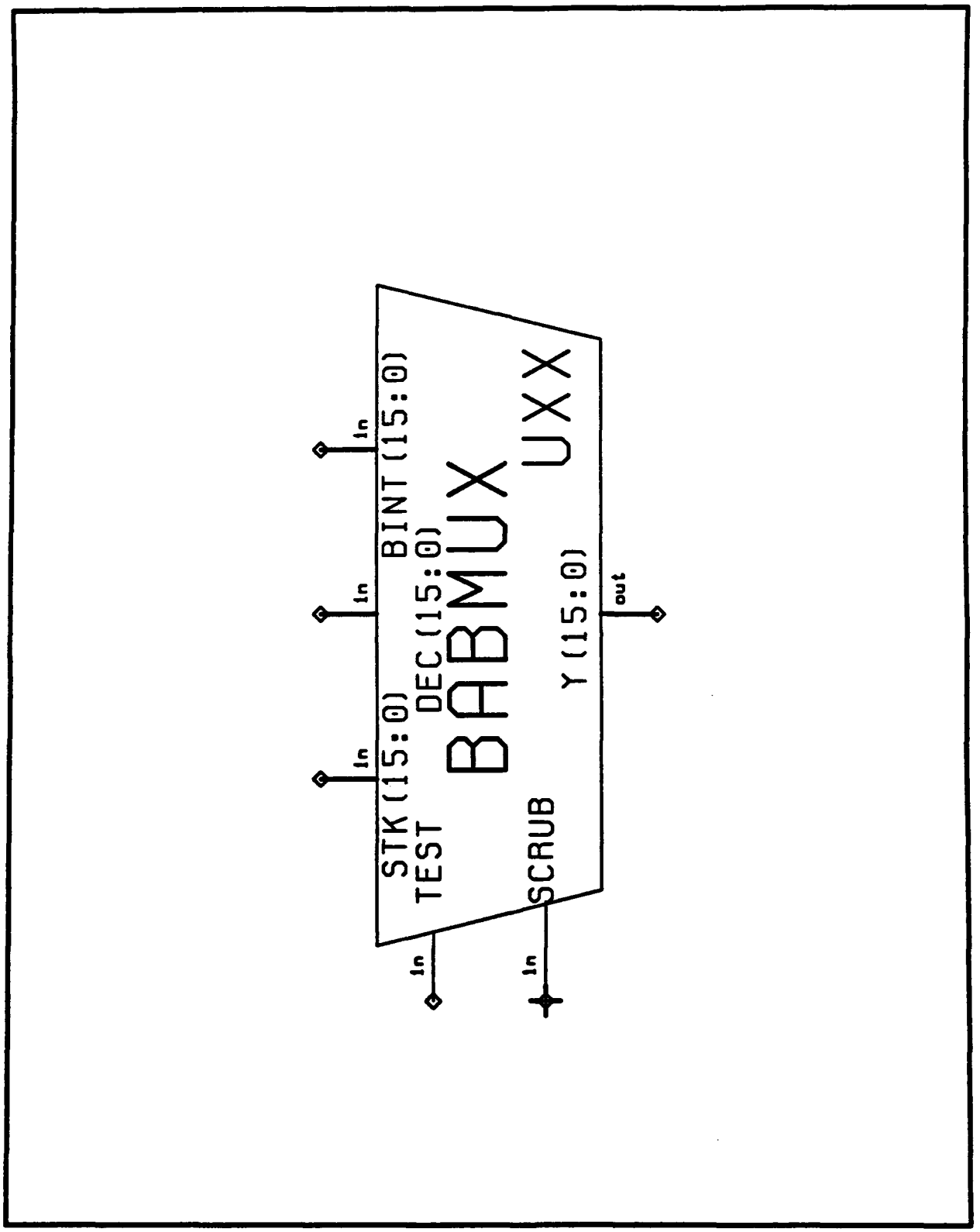

MCS
mcs.bin
bran(15:0)
edo
farg(15:0)
fare(15:0)
cef(3:0)
intreq
intack
ccode
bf
dest(15:0)
bal(15:0)
edl
essl
eql(3:0)
fcont
bp
irq(13:0)
lenf
cc(28:0)
cce(4:0)
ctf
abs(4:0)
dbd(4:0)
bas(1:0)
etall(5:0)
pipe
initf
clk
clkn

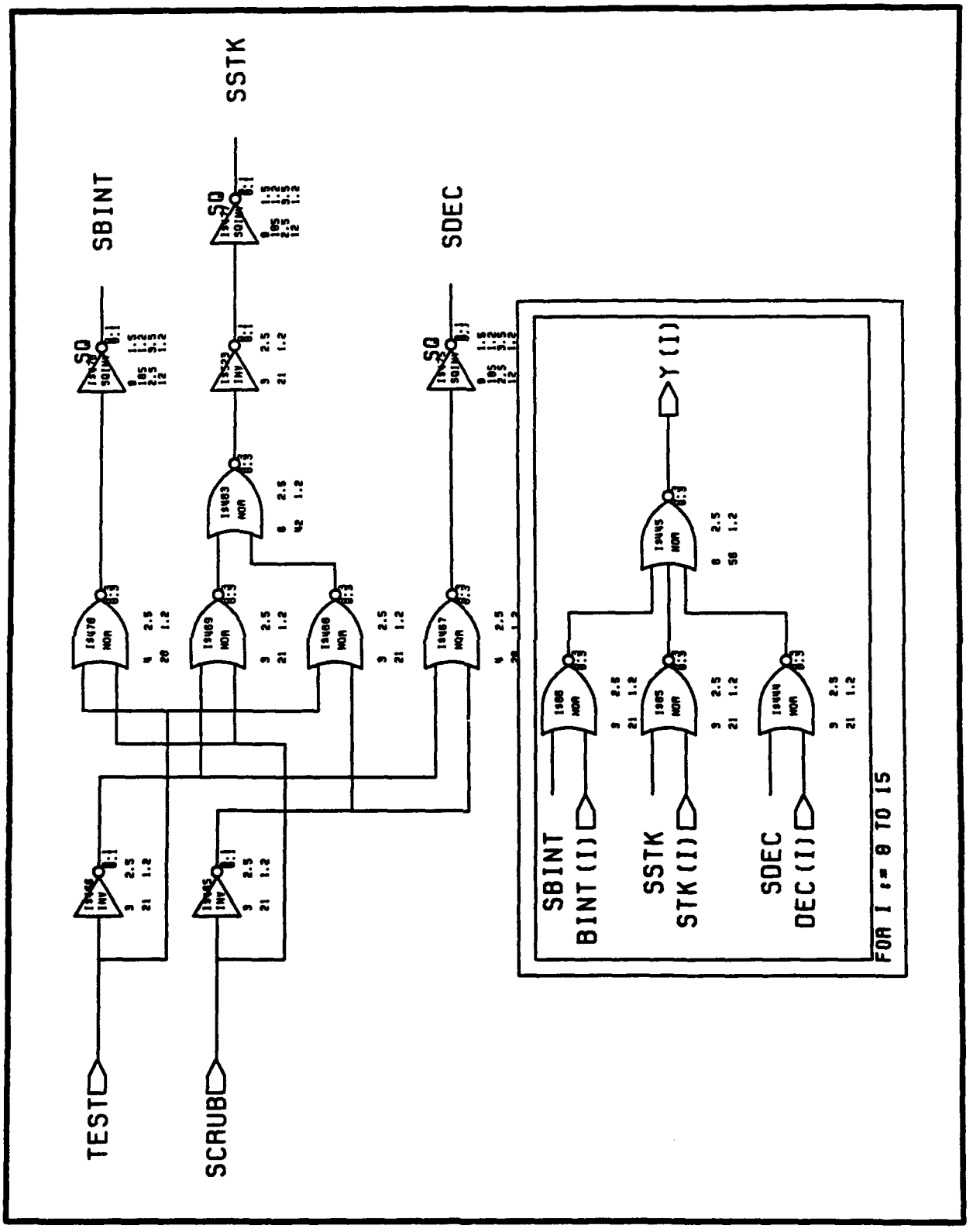


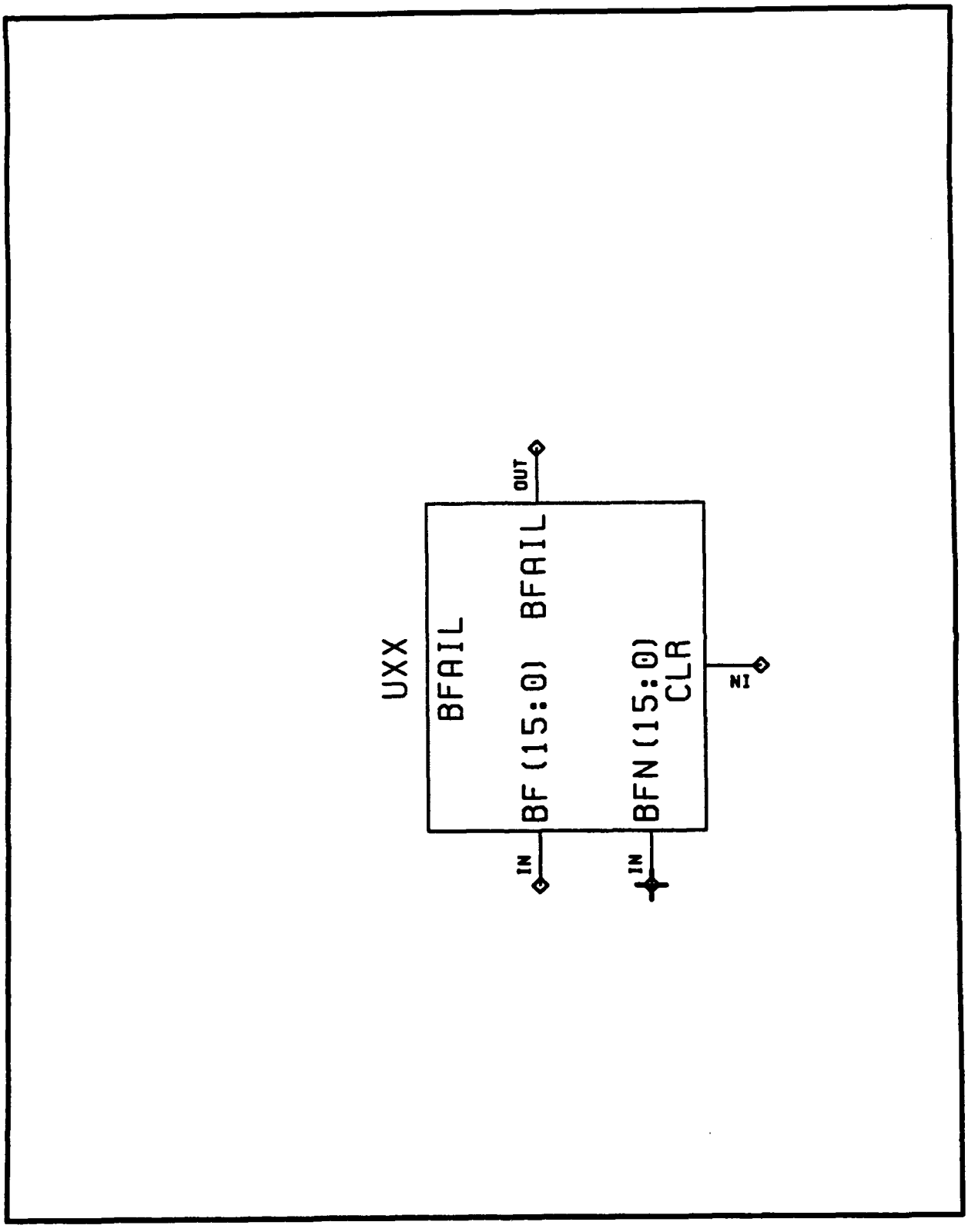

MCS
MCS Sheet 2
FOR I := 0 TO 15
FOR I := 0 TO 3
FOR I := 0 TO 3
FOR I := 0 TO 1
FOR I := 0 TO 28
FOR I := 0 TO 15
FOR I := 0 TO 15
FOR I := 0 TO 15
FOR I := 0 TO 4

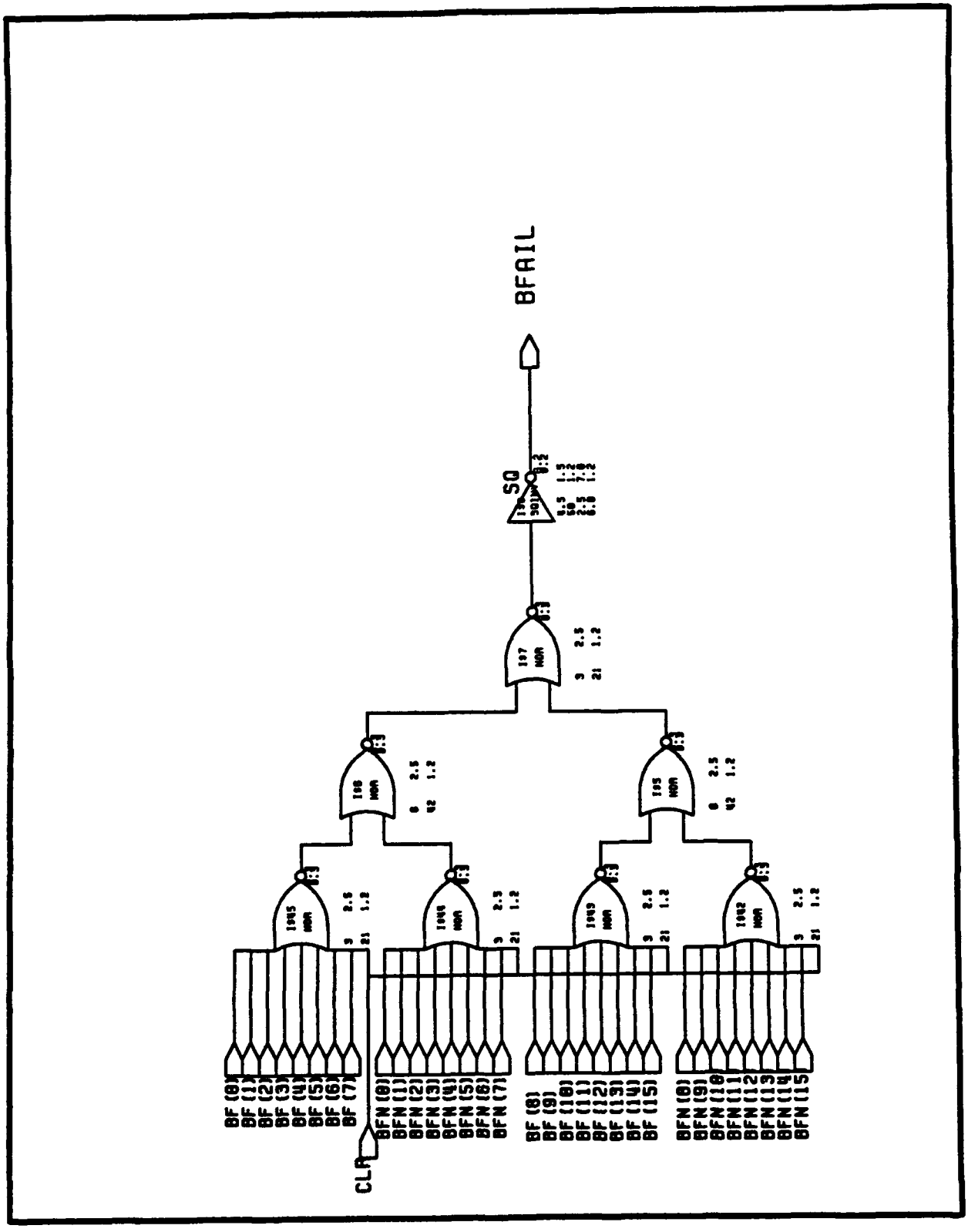

OUT
Q
UXX
ALULDBIT
SET
NI
D
CLK
IN
IN

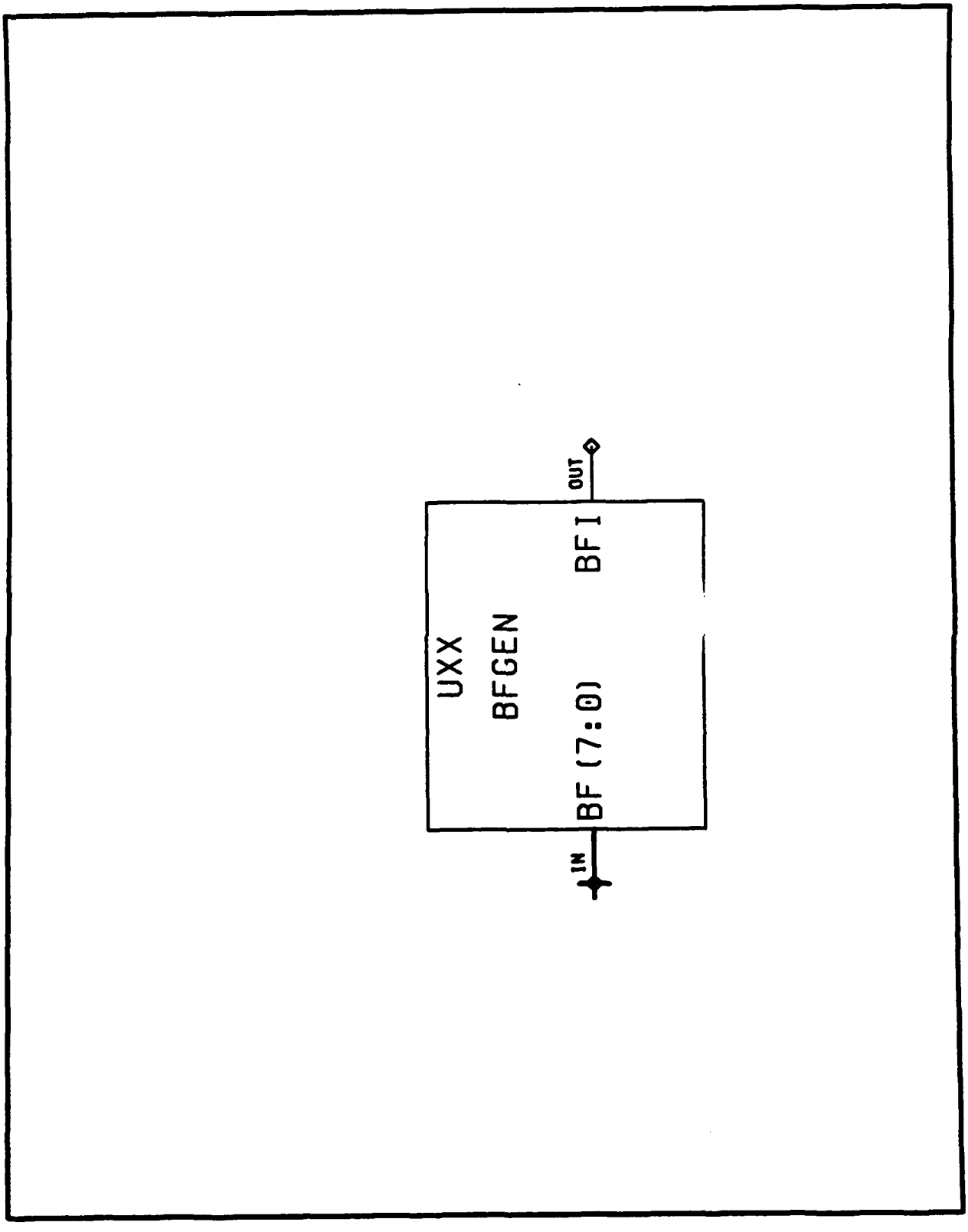

ALULDBIT: FALLING EDGE TRIGGERED
Q
SQ
CLK
SET
D

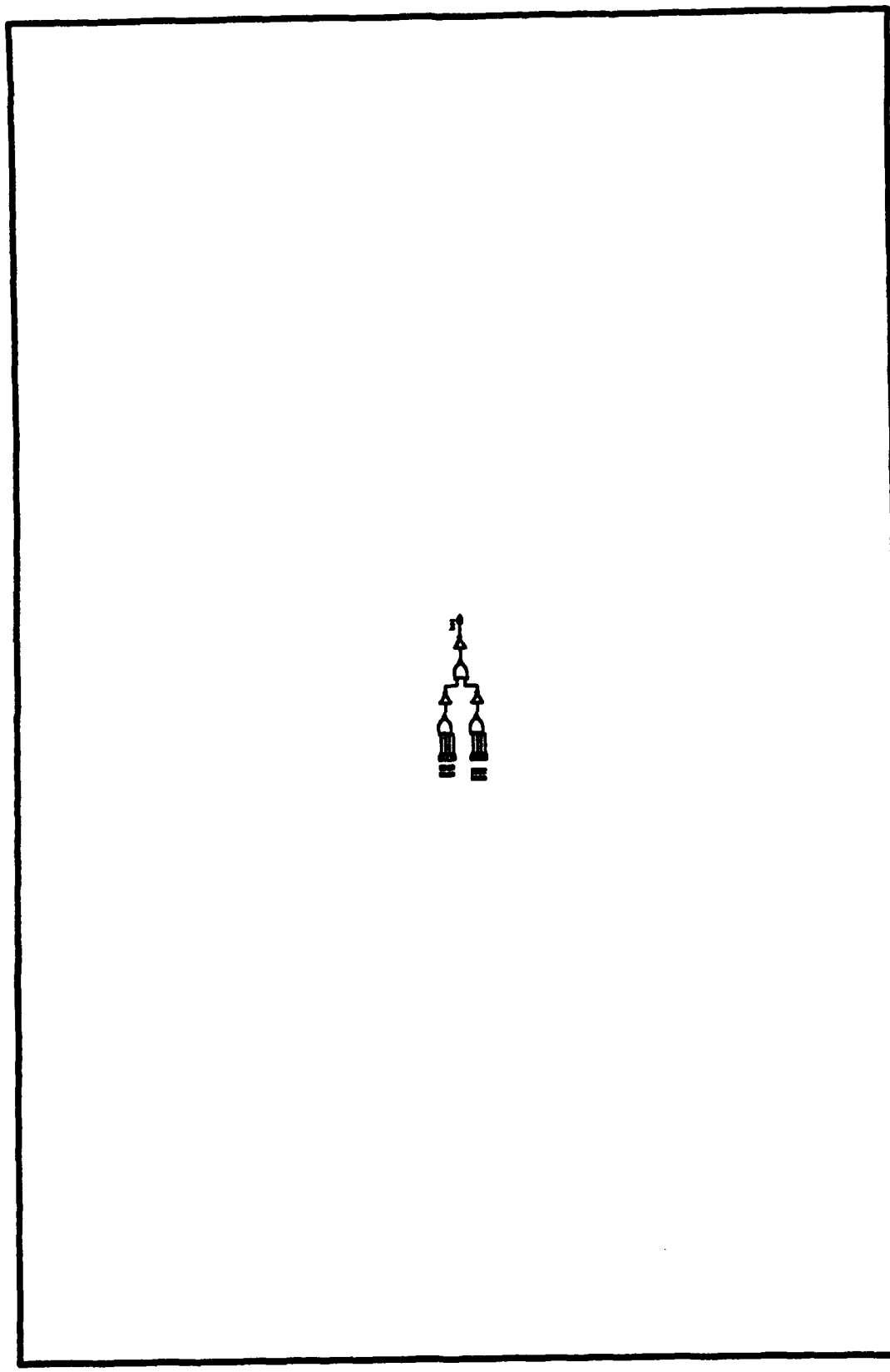

BABMUX UXX
BINT(15:0)
DEC(15:0)
STK(15:0)
TEST
SCRUB
Y(15:0)
in
in
in
in
in
out

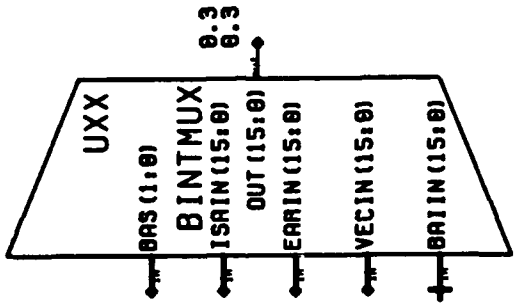

SBINT
SSTK
SDEC
TEST
SCRUB
Y (I)
SBINT
BINT (I)
SSTK
STK (I)
SDEC
DEC (I)
FOR I := 0 TO 15

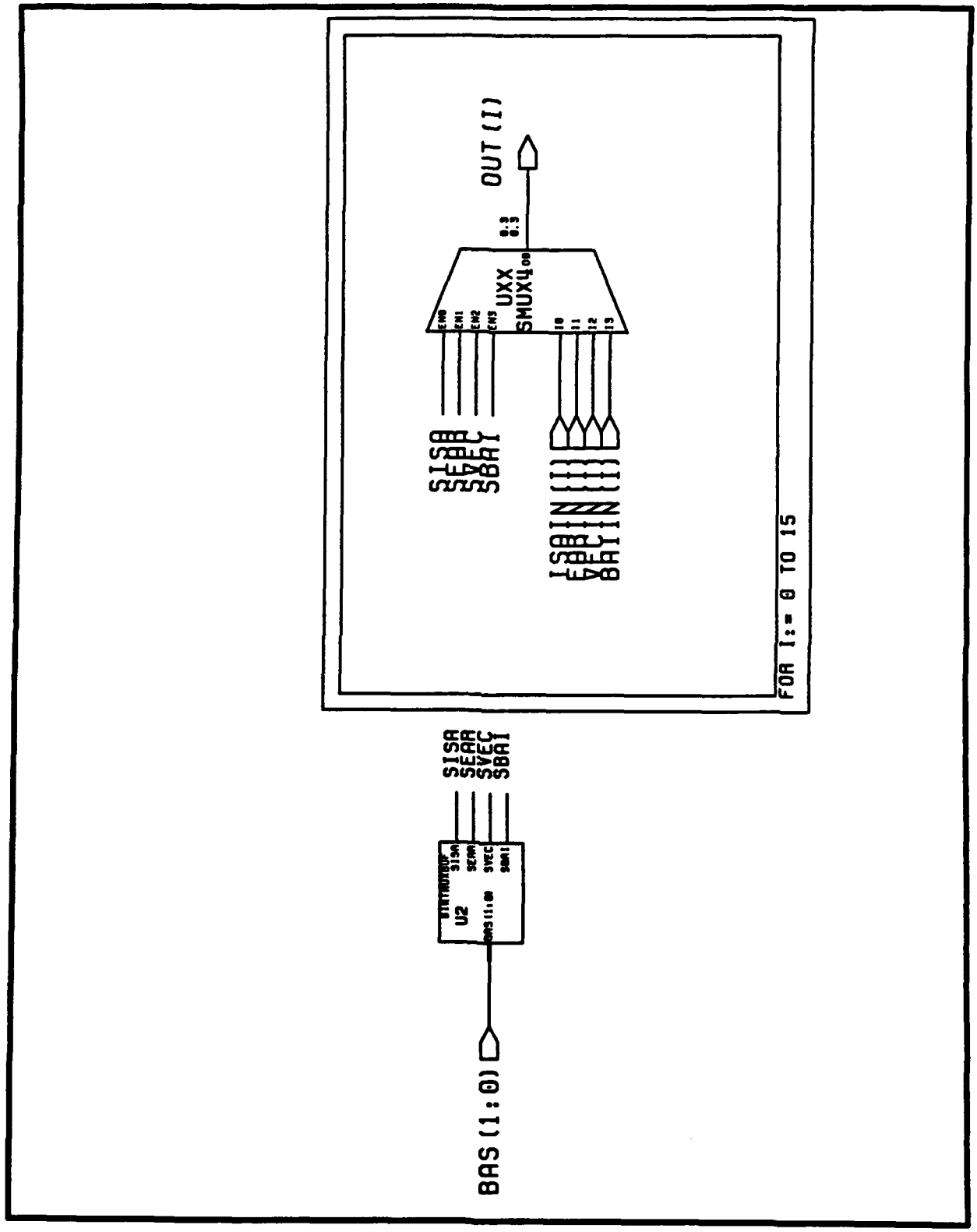

UXX
BFAIL
BF(15:0) BFAIL
BFN(15:0) CLR
OUT
NI
IN
IN

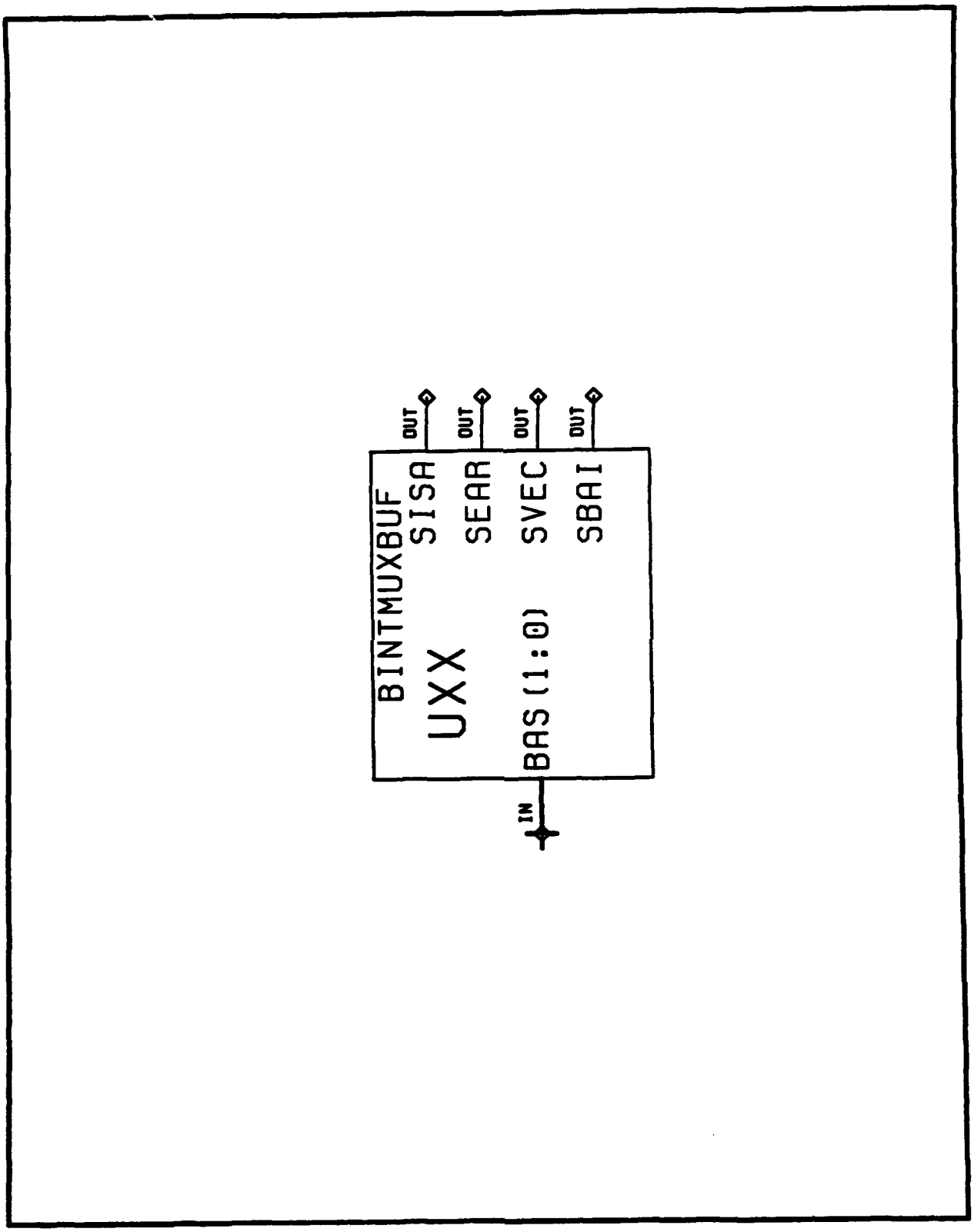

BFAIL
SQ
197
NOR
196
NOR
195
NOR
1965
NOR
1966
NOR
1963
NOR
1962
NOR
BF (0)
BF (1)
BF (2)
BF (3)
BF (4)
BF (5)
BF (6)
BF (7)
BFN (0)
BFN (1)
BFN (2)
BFN (3)
BFN (4)
BFN (5)
BFN (6)
BFN (7)
BF (8)
BF (9)
BF (10)
BF (11)
BF (12)
BF (13)
BF (14)
BF (15)
BFN (8)
BFN (9)
BFN (10)
BFN (11)
BFN (12)
BFN (13)
BFN (14)
BFN (15)
CLR

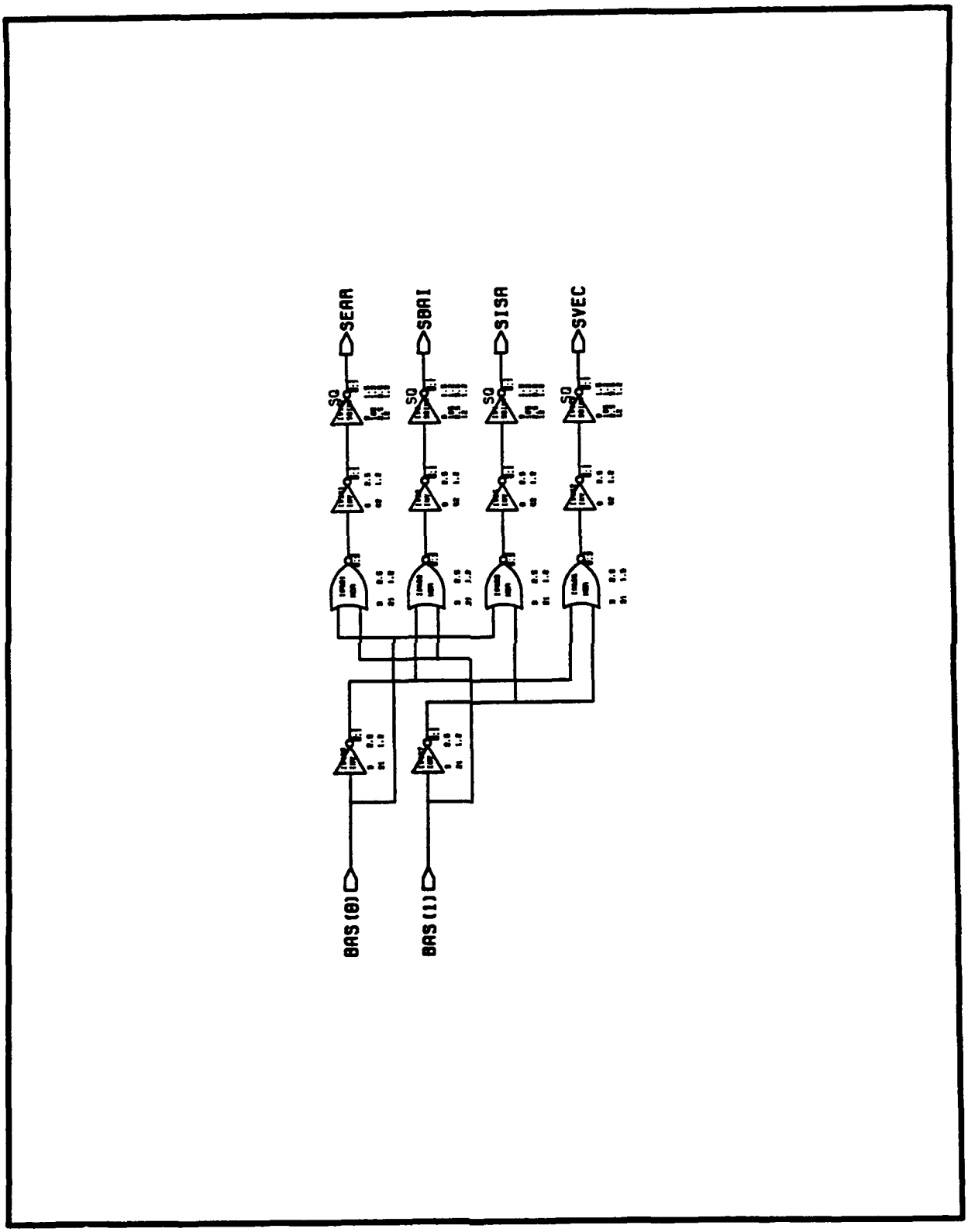

OUT
BFI
UXX
BFGEN
BF(7:0)
IN

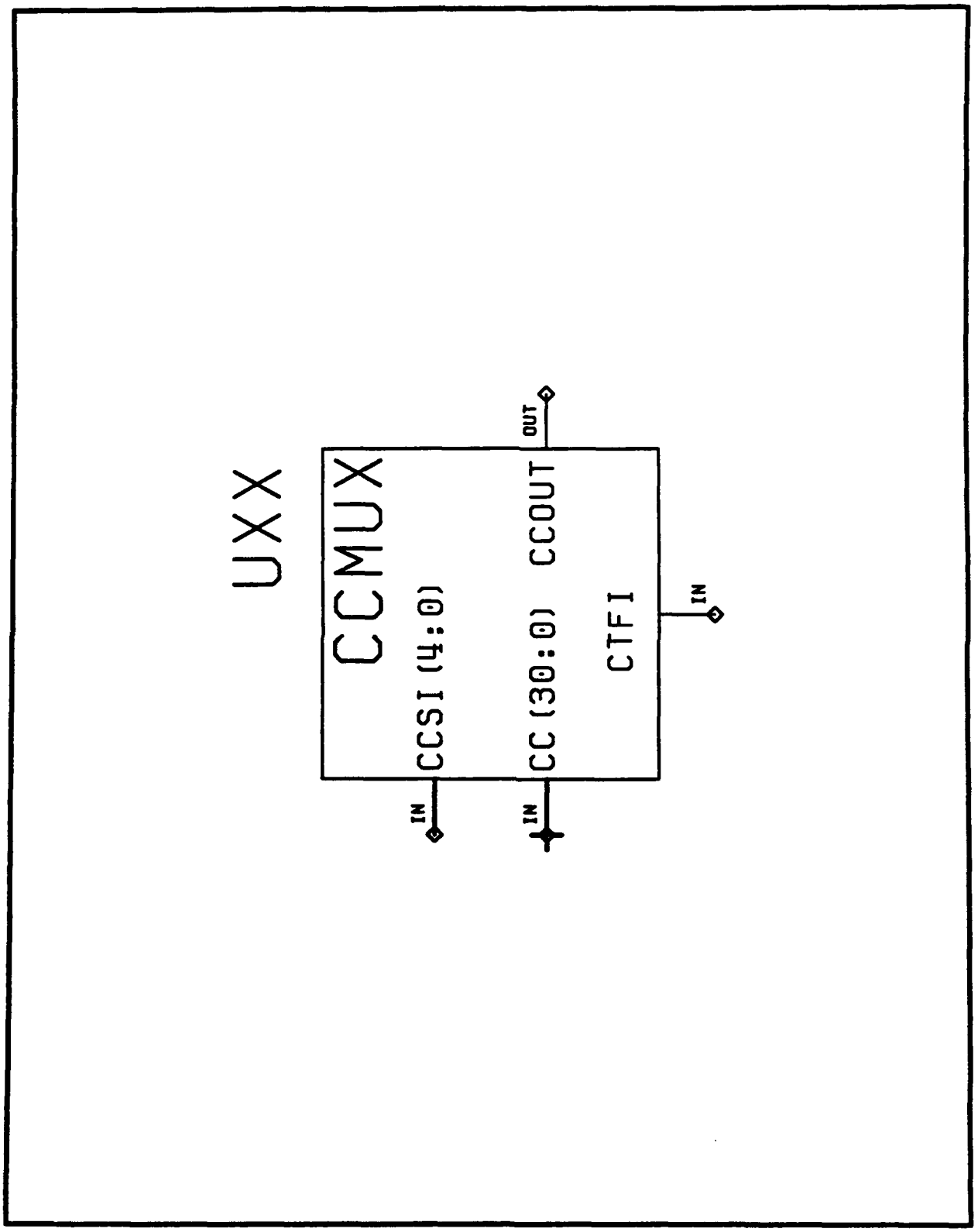


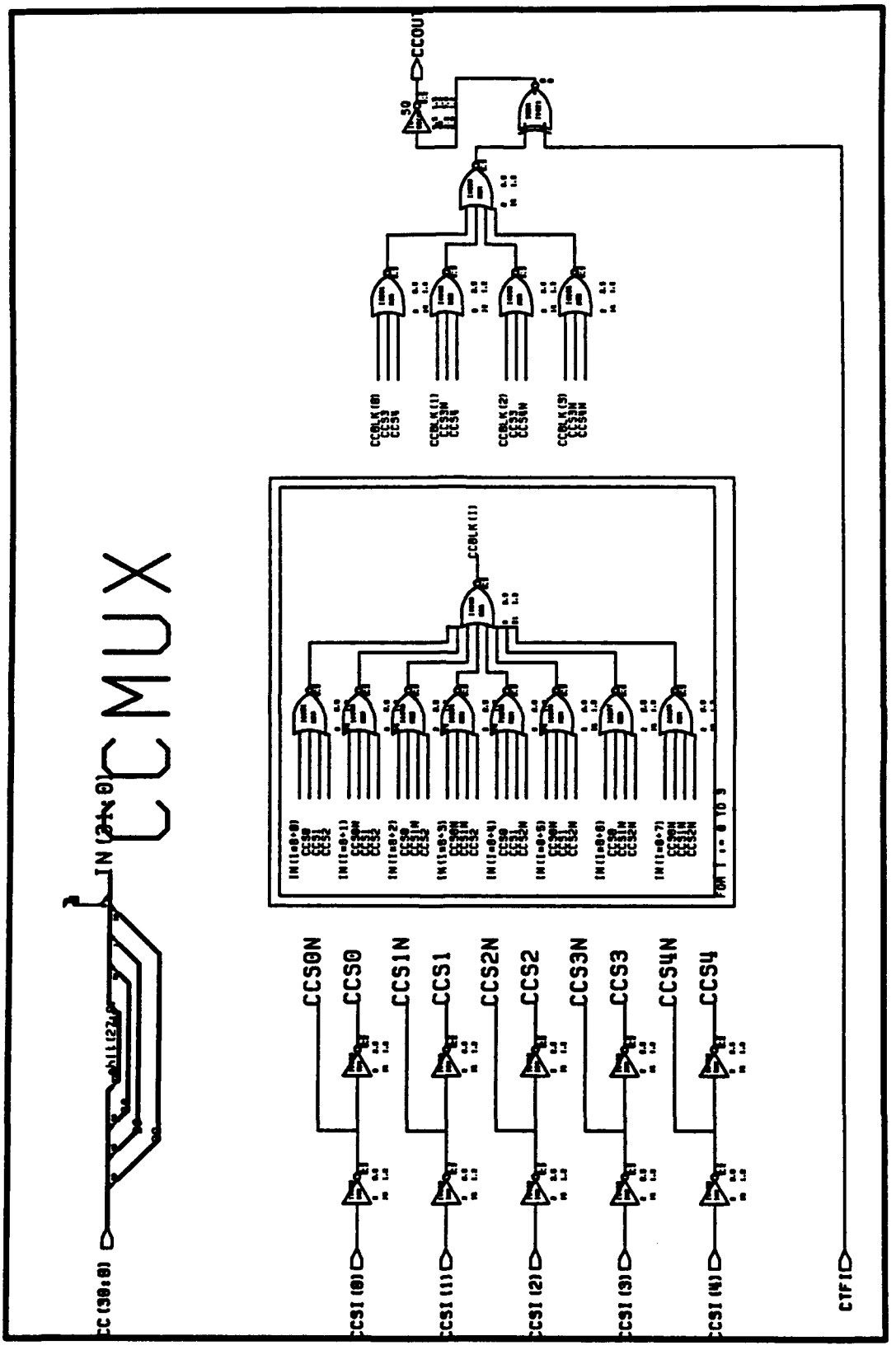

0.3
0.3
UXX
BINTMUX
BAS(1:0)
ISAIN(15:0)
OUT(15:0)
EAAIN(15:0)
VECIN(15:0)
BAIIN(15:0)


OUT (I)
UXX
SMUX4
SISA
SEAA
SVEC
SBAT
ISA
EAA
VEC
BAT
FOR I:= 0 TO 15
SISA
SEAA
SVEC
SBAT
U2
BAS (1:0)


OUT
OUT
OUT
OUT
BINTMUXBUF
SISA
SEAR
SVEC
SBAI
UXX
BAS(1:0)
IN


SEAR
SBAI
SISA
SVEC
SO
SO
SO
SO
BAS(0)
BAS(1)

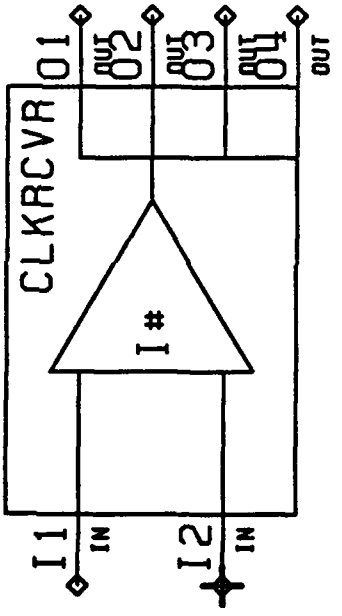

UXX
CCMUX
CCSI(4:0)
CC(30:0)
CCOUT
CTFI
OUT
IN
IN
IN


CCMUX
CCOUT
CCBLK(1)
IN(30:0)
CCS0N
CCS0
CCS1N
CCS1
CCS2N
CCS2
CCS3N
CCS3
CCS4N
CCS4
CCSI(0)
CCSI(1)
CCSI(2)
CCSI(3)
CCSI(4)
CTFI

VITESSE GAAS CELL LIBRARY
Version 0.8

NAME: CLKRCVR

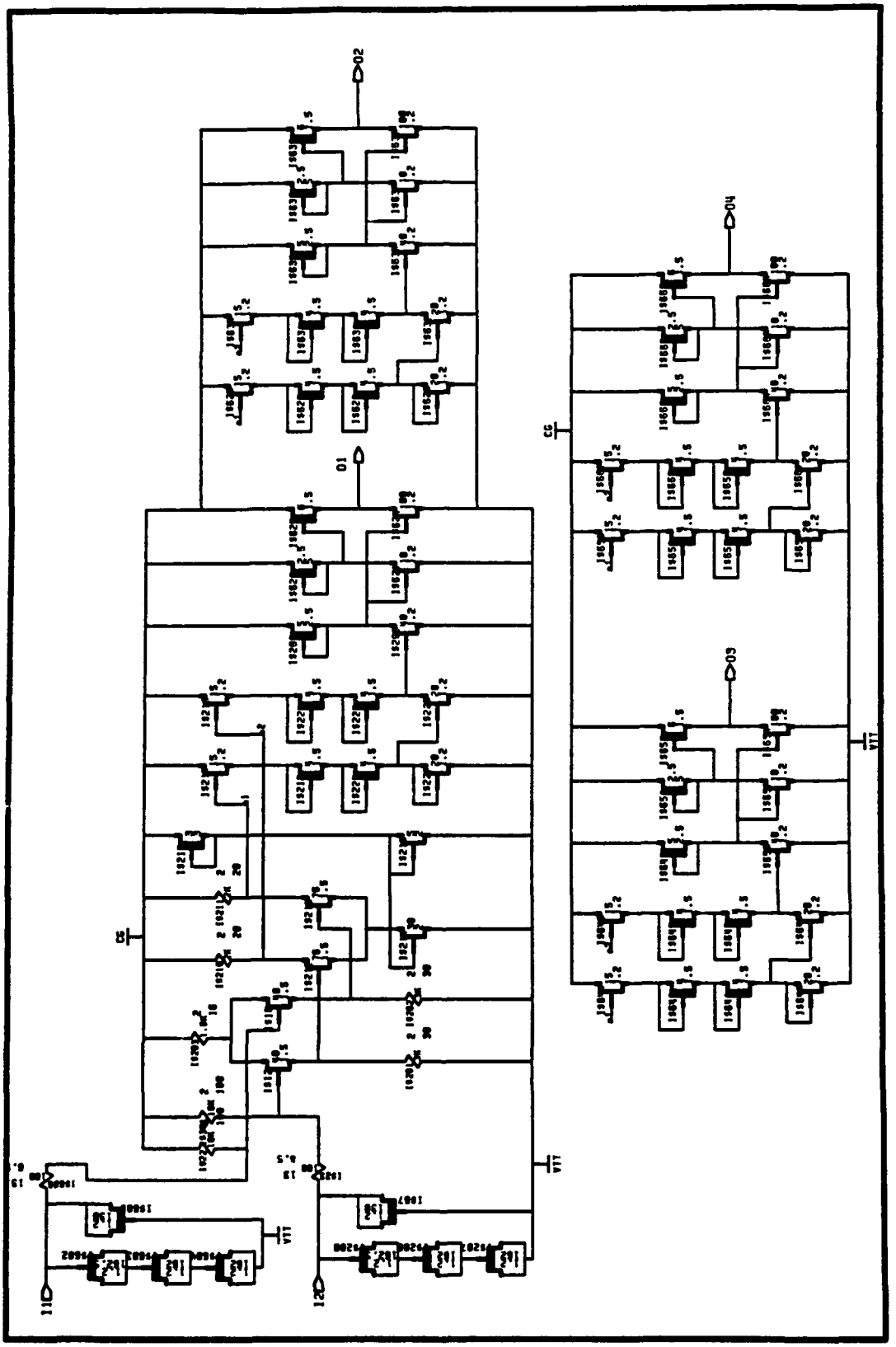
DESCRIPTION: DIFFERENTIAL INPUT CLOCK RECEIVER

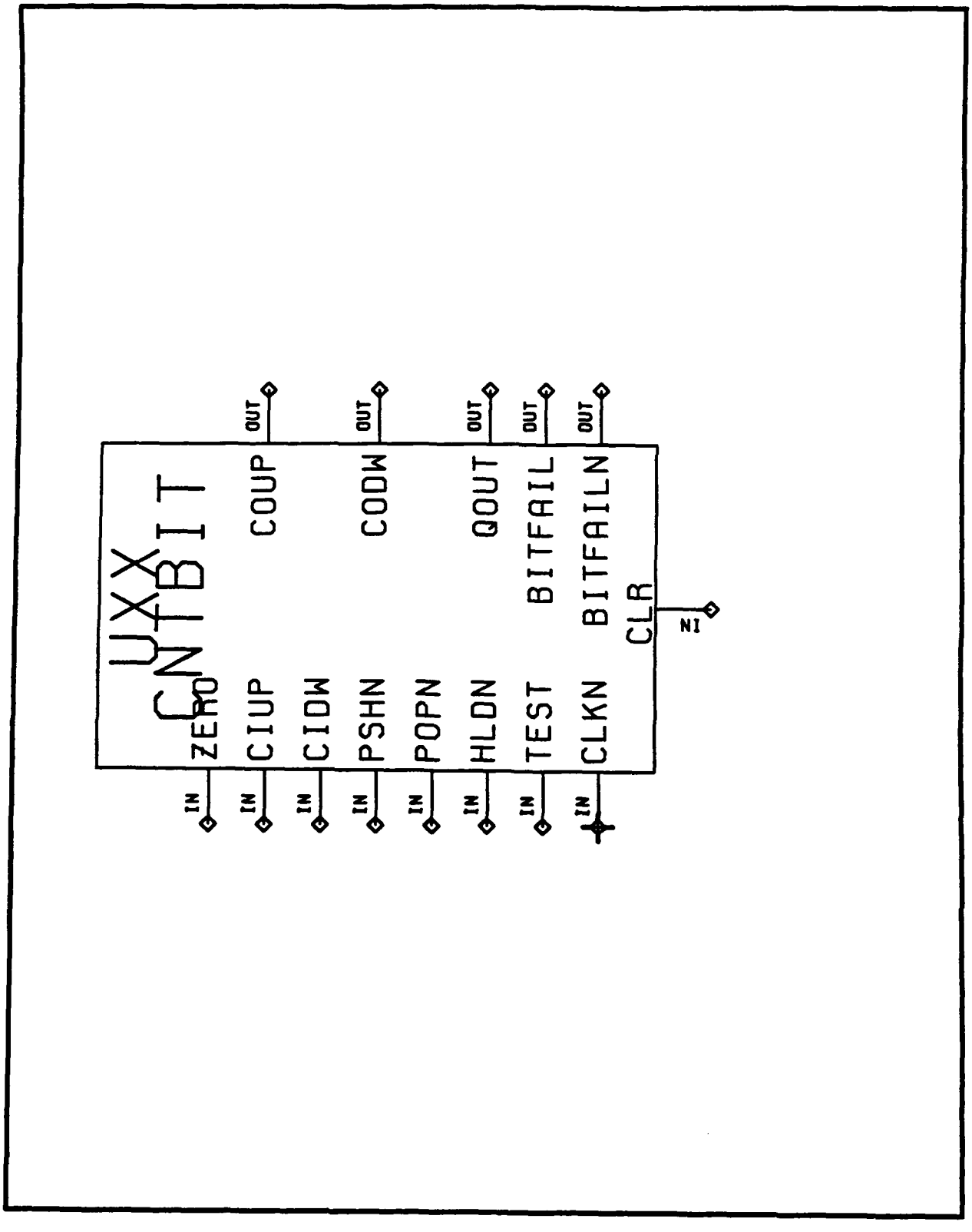


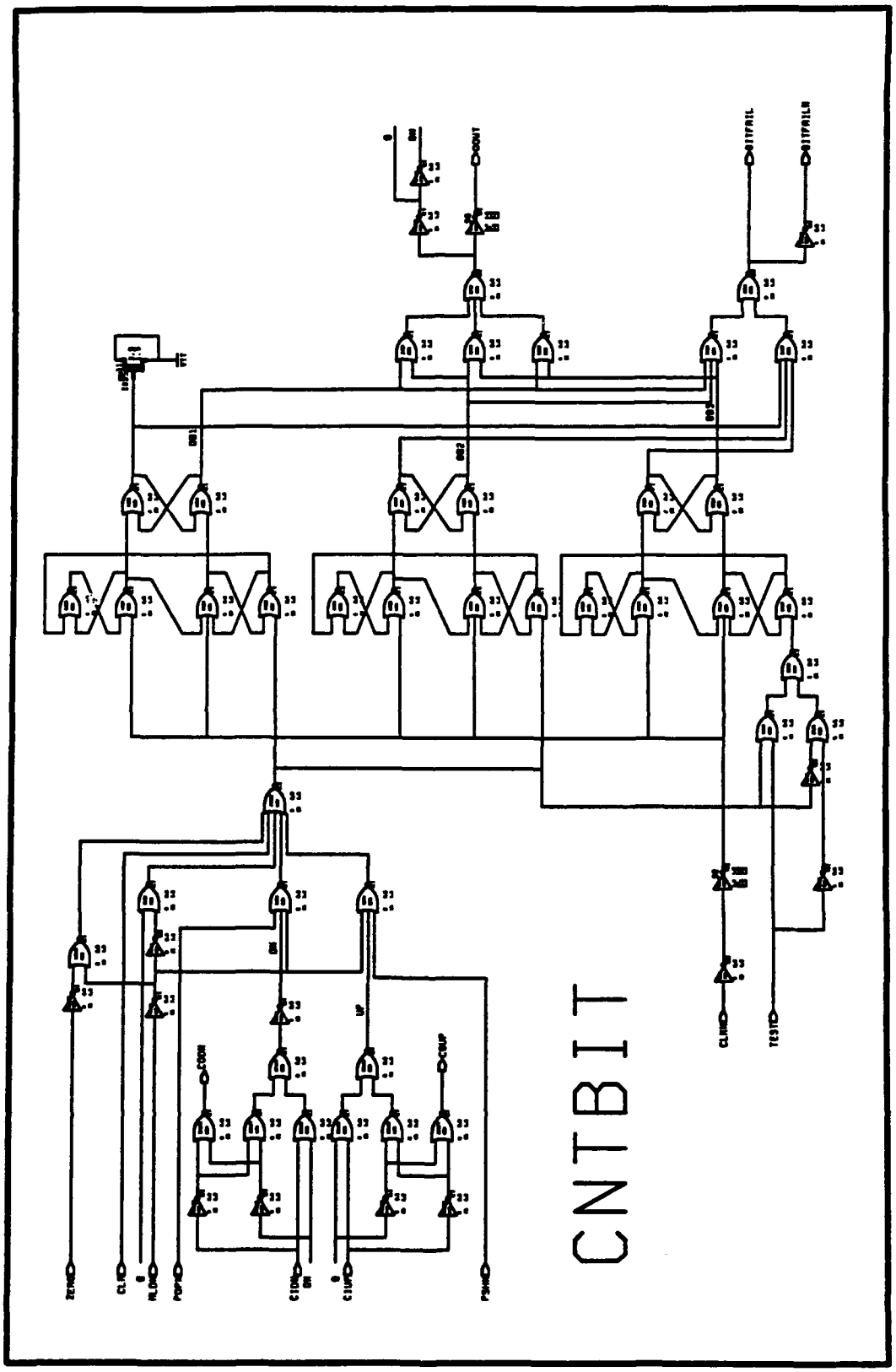
0.5	0.3	SSS
0.5	0.3	SSS
0.5	0.3	SSS
0.5	0.3	SSS

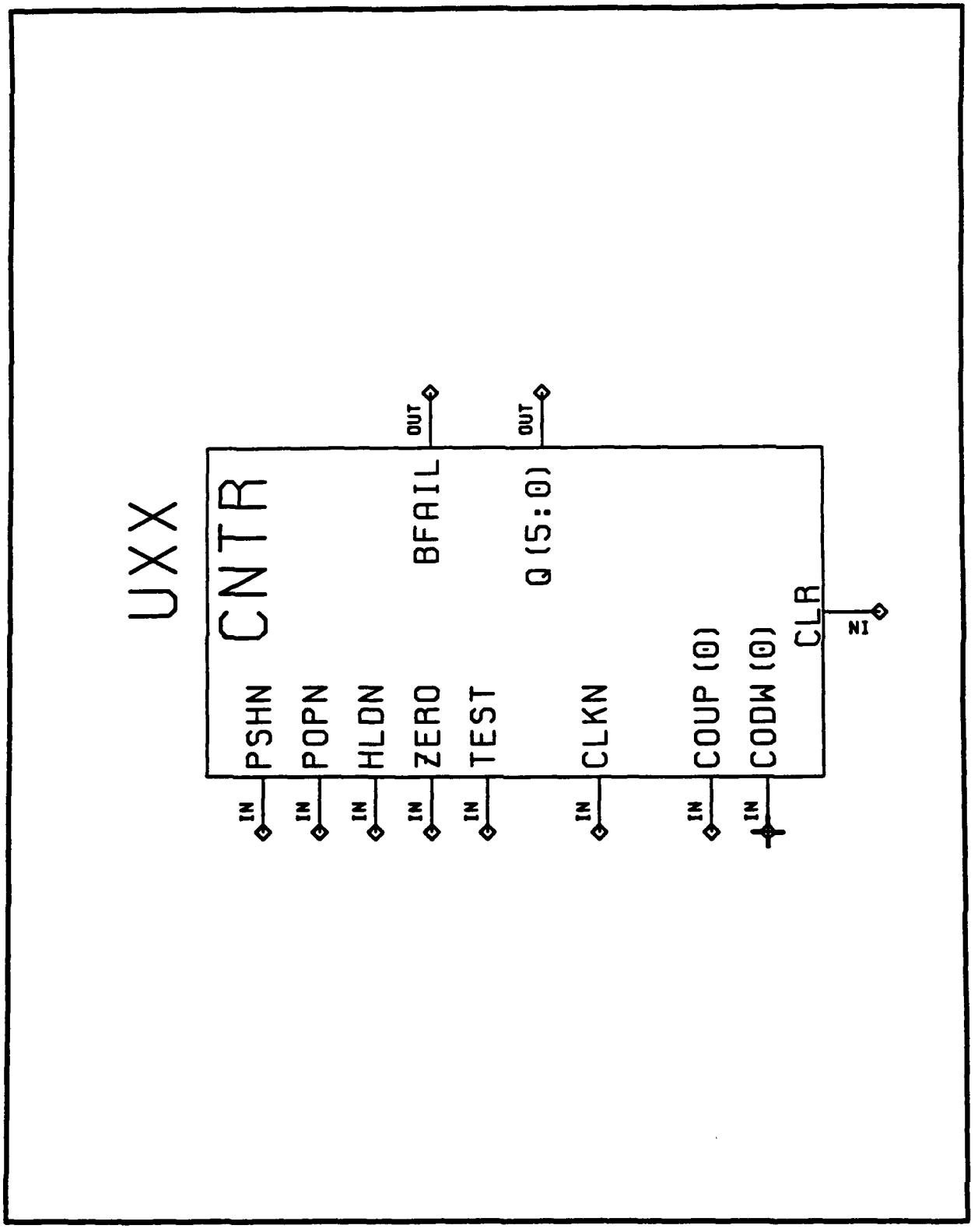
CLKRCVR

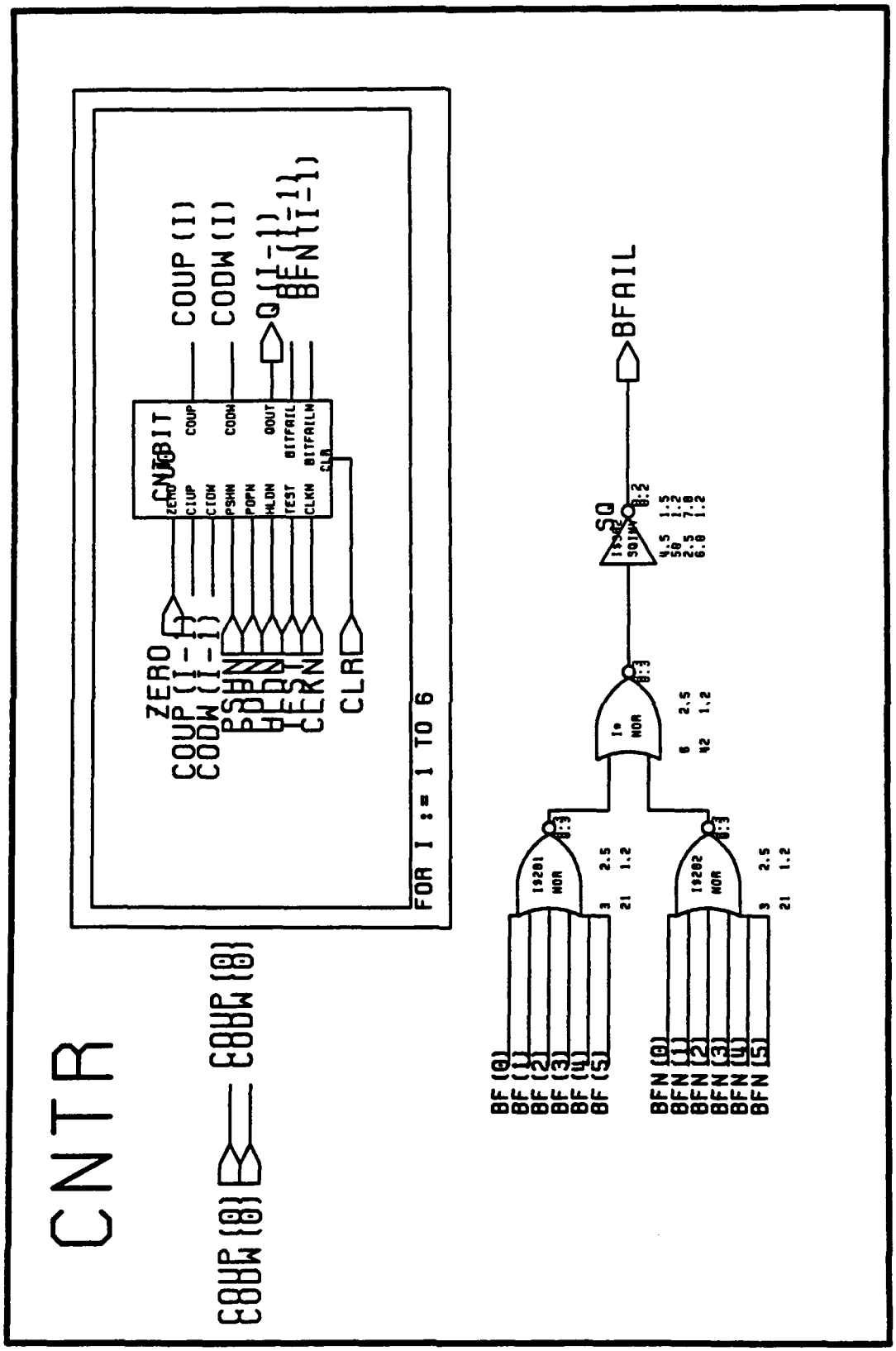
clkrcvr.bin

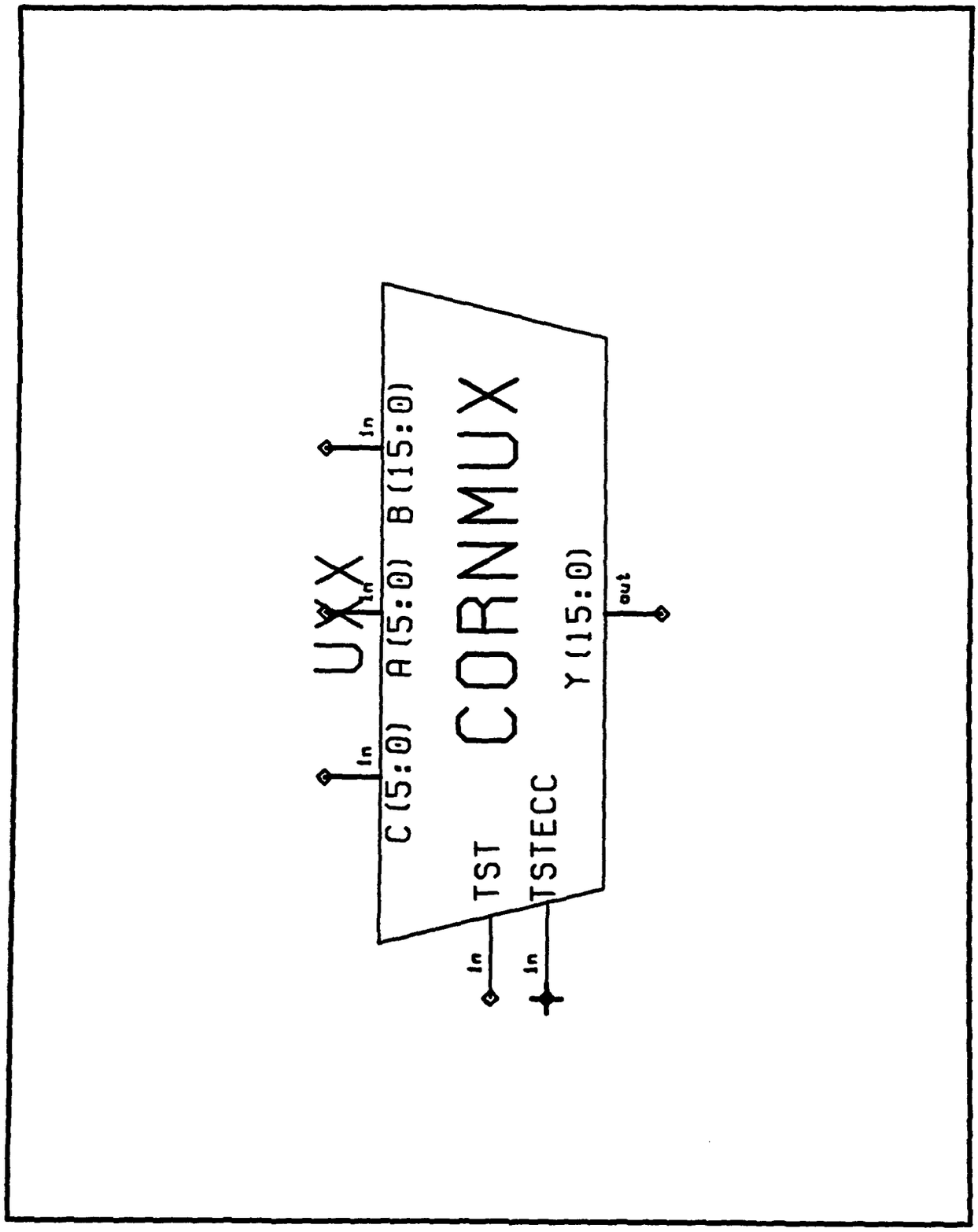


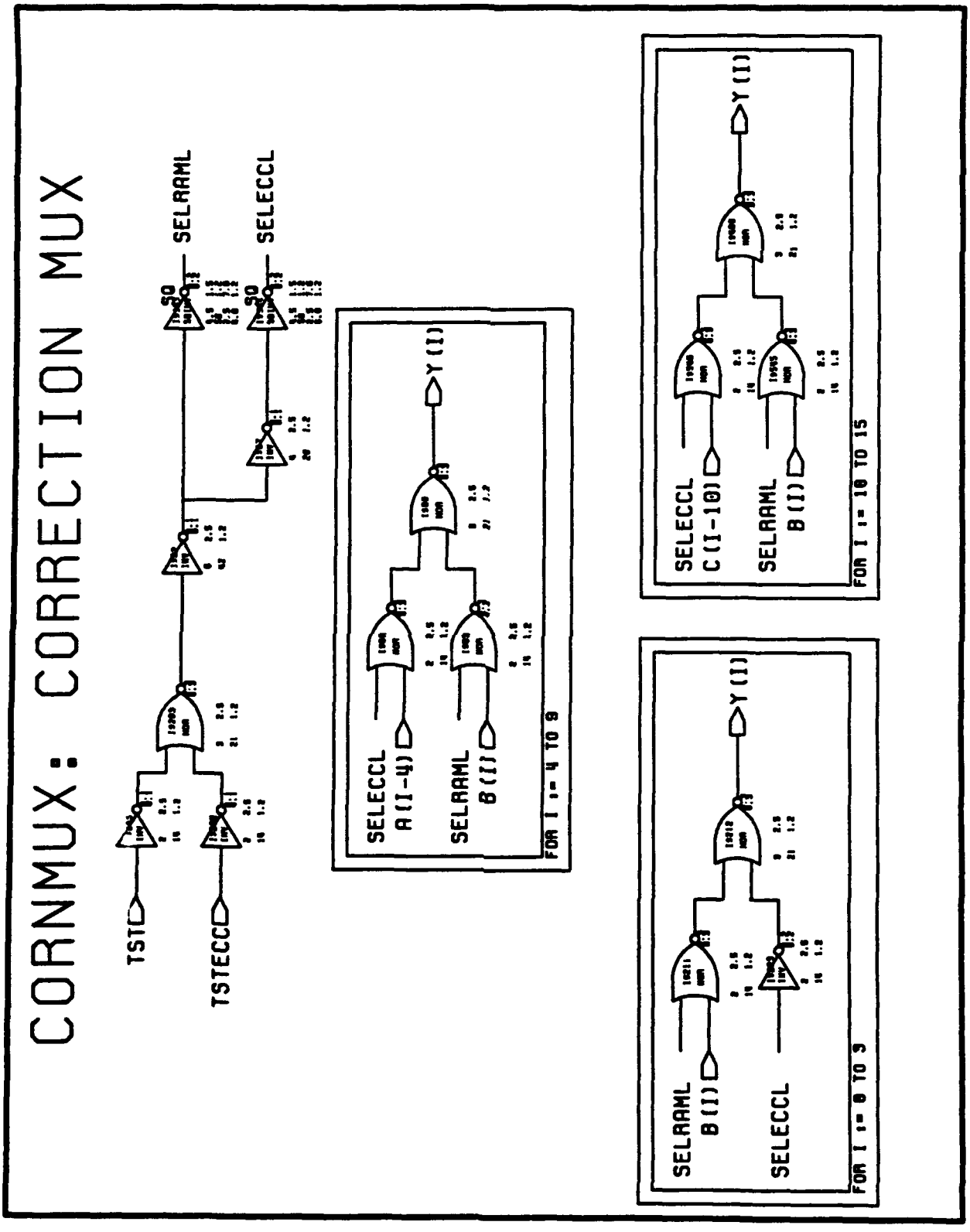

CNTBIT
UXX
ZERO
CIUP
CIDW
PSHN
POPN
HLDN
TEST
CLKN
CLR
COUP
CODW
QOUT
BITFAIL
BITFAILN
IN
OUT
NI

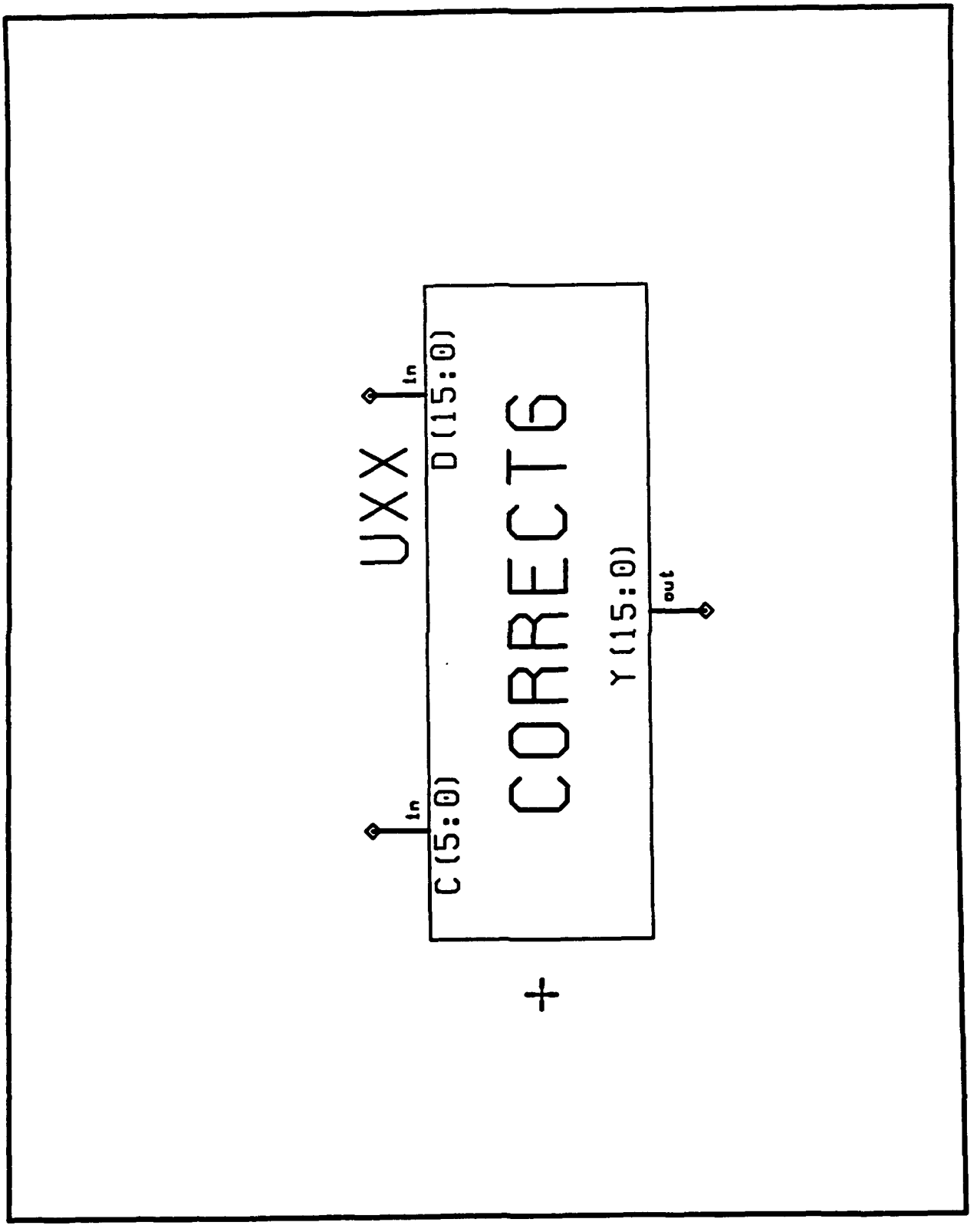

CNTBIT

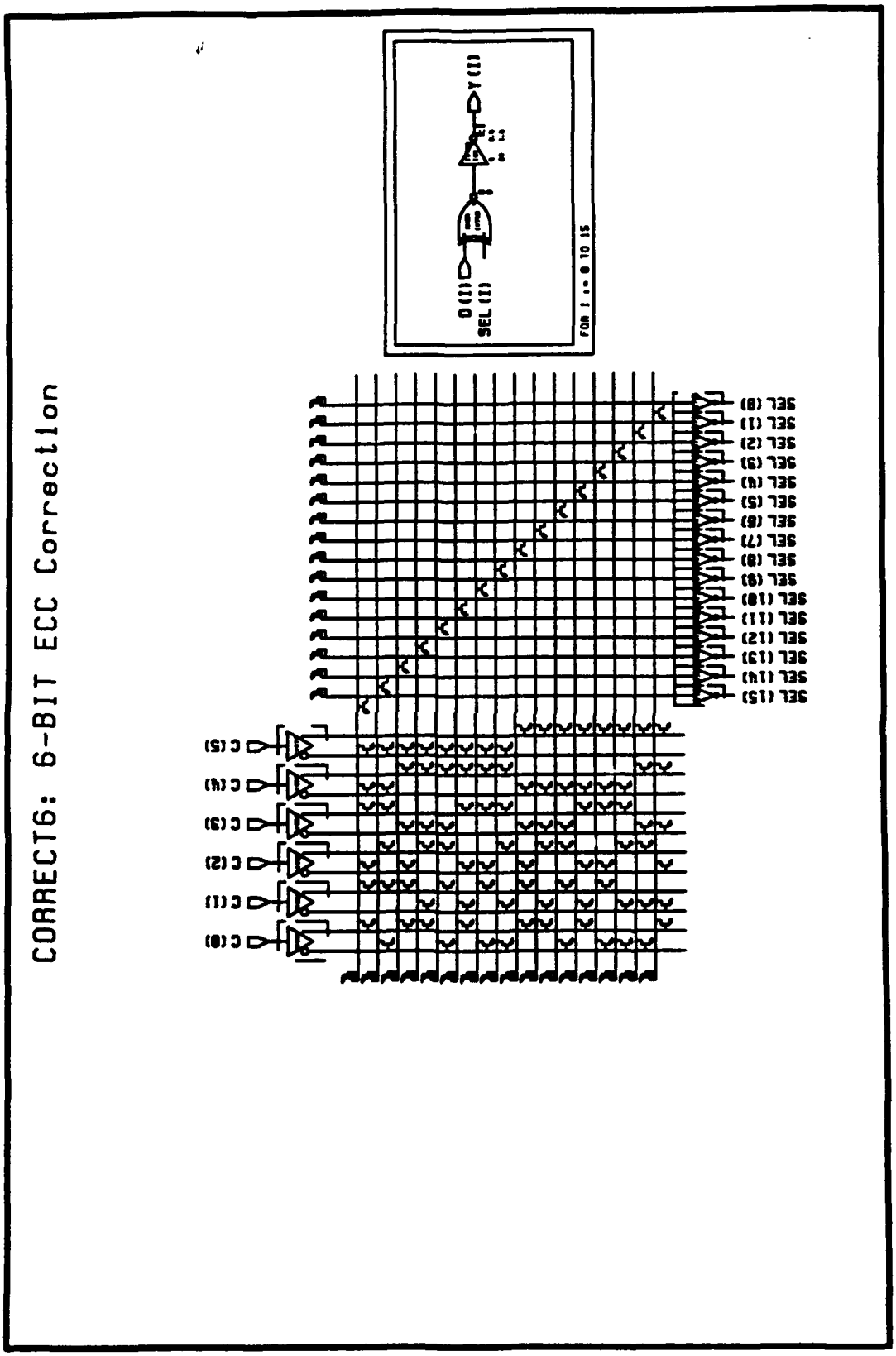

UXX
CNTR
BFAIL
Q(5:0)
CLR
PSHN
POPN
HLDN
ZERO
TEST
CLKN
COUP(0)
CODW(0)
OUT
OUT
IN
IN
IN
IN
IN
IN
IN
IN
NI

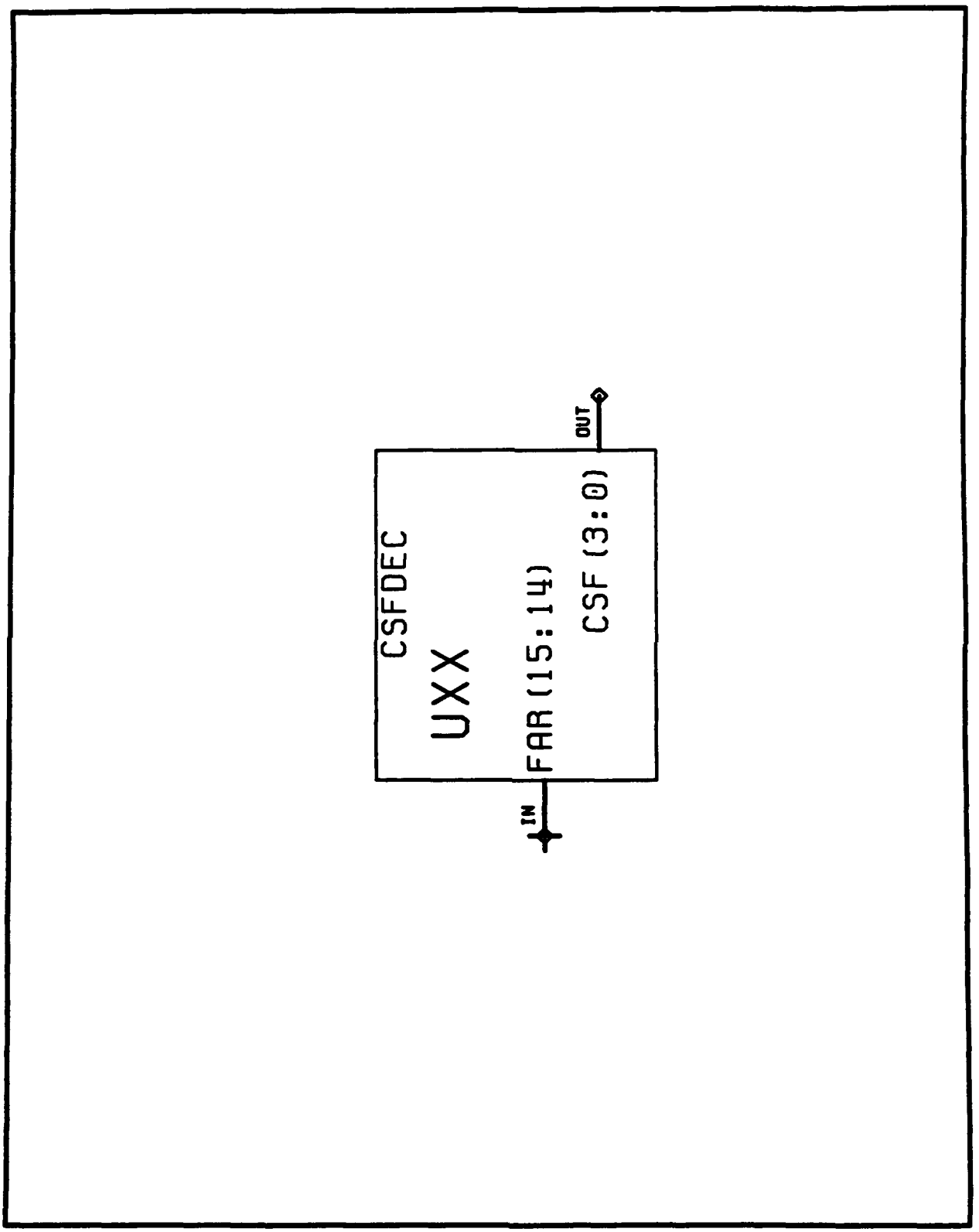

CNTR
COUP (8)
CODW (8)
FOR I := 1 TO 6
CNT8IT
COUP (I)
CODW (I)
BFN (I-1)
ZERO
COUP (I-1)
CODW (I-1)
PSHN
POPN
HLDN
TESTN
CLRN
CLR
BFAIL
SQ
BF (0)
BF (1)
BF (2)
BF (3)
BF (4)
BF (5)
BFN (0)
BFN (1)
BFN (2)
BFN (3)
BFN (4)
BFN (5)

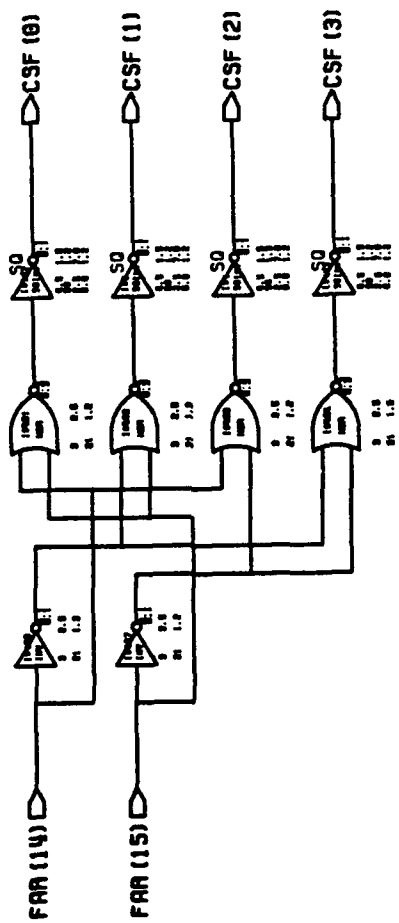

UXX
CORNMUX
C(5:0)
A(5:0)
B(15:0)
Y(15:0)
TST
TSTECC
in
out

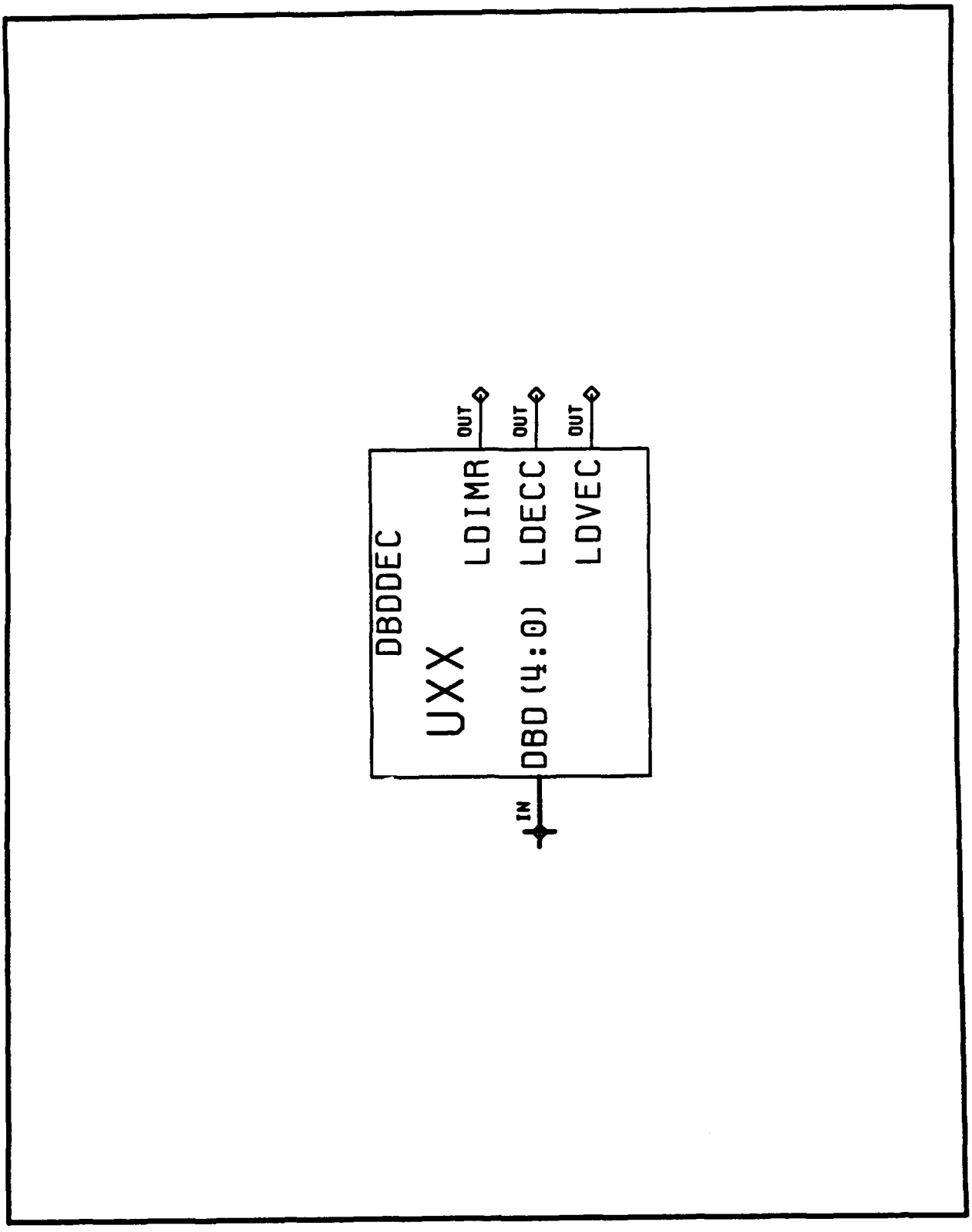

CORNMUX: CORRECTION MUX
SELRAML
SELECCL
S0
S0
TSTD
TSTECCD
SELECCL
A(I-4)
SELRAML
B(I)
Y(I)
FOR I := 4 TO 8
SELECCL
C(I-10)
SELRAML
B(I)
Y(I)
FOR I := 10 TO 15
SELRAML
B(I)
SELECCL
Y(I)
FOR I := 0 TO 3

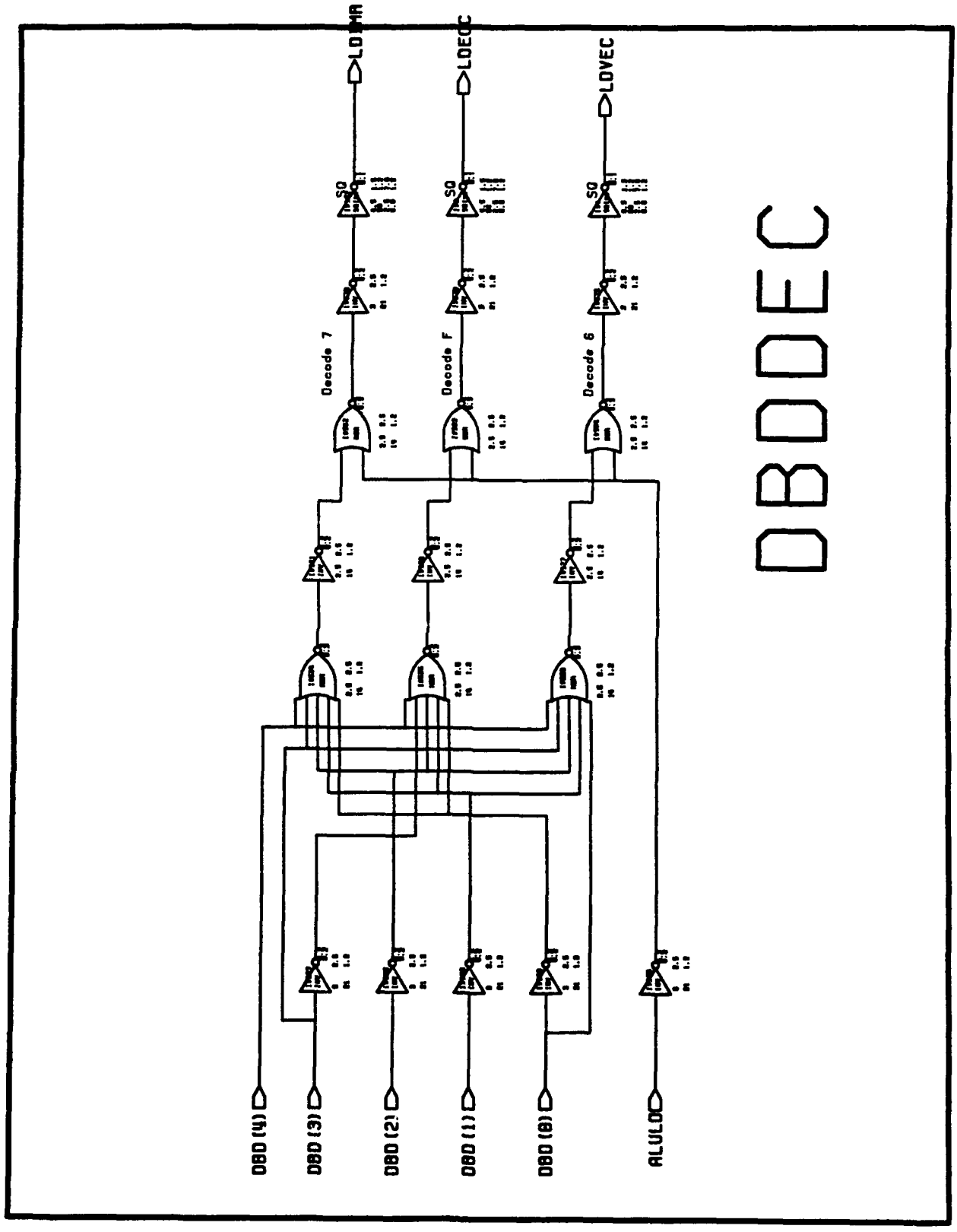

UXX
in
D(15:0)
in
C(5:0)
CORRECT6
Y(15:0)
out

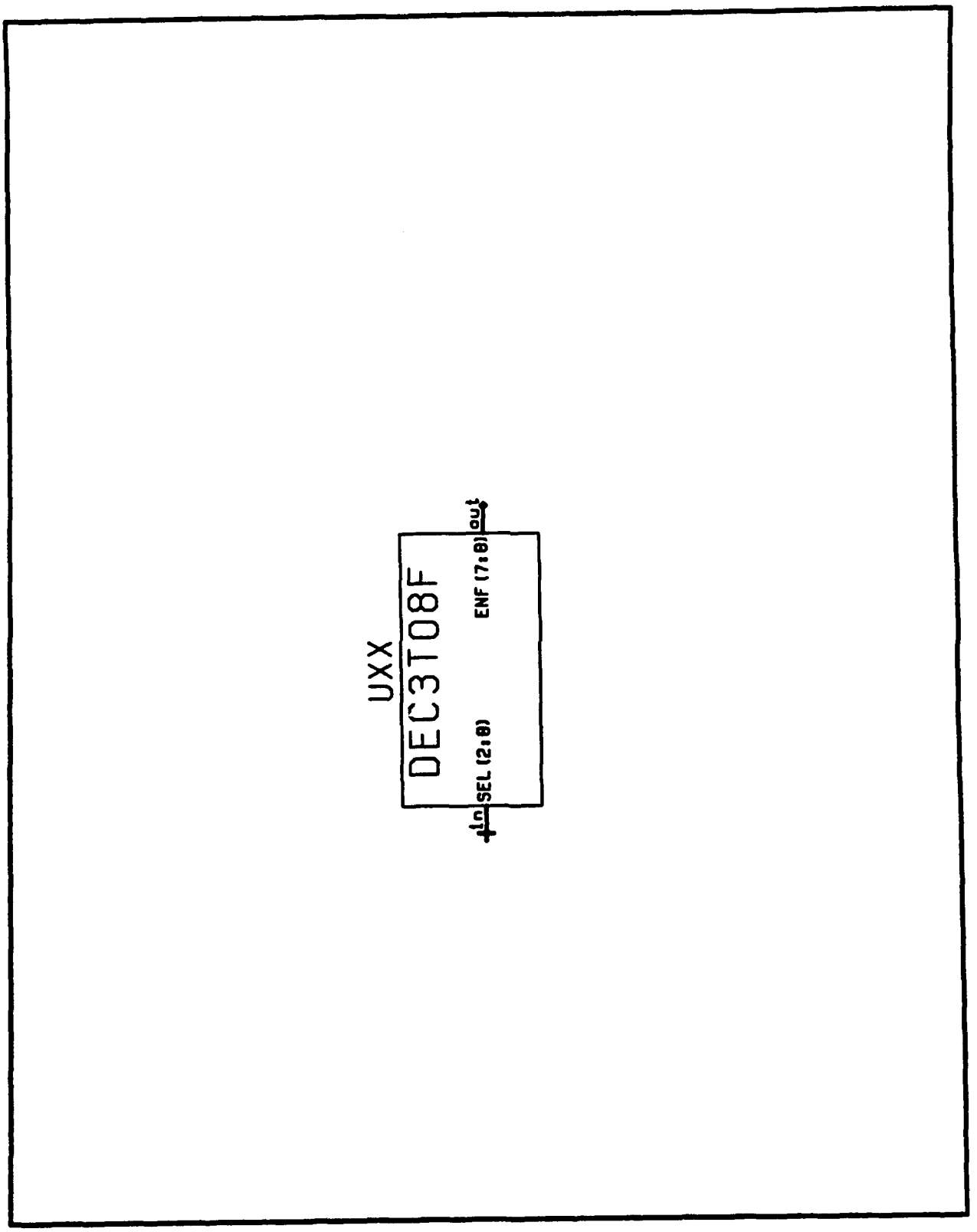

CORRECT6: 6-BIT ECC Correction
D (I)
SEL (I)
FOR I = 0 TO 15
SEL (0)
SEL (1)
SEL (2)
SEL (3)
SEL (4)
SEL (5)
SEL (6)
SEL (7)
SEL (8)
SEL (9)
SEL (10)
SEL (11)
SEL (12)
SEL (13)
SEL (14)
SEL (15)
C (5)
C (4)
C (3)
C (2)
C (1)
C (0)

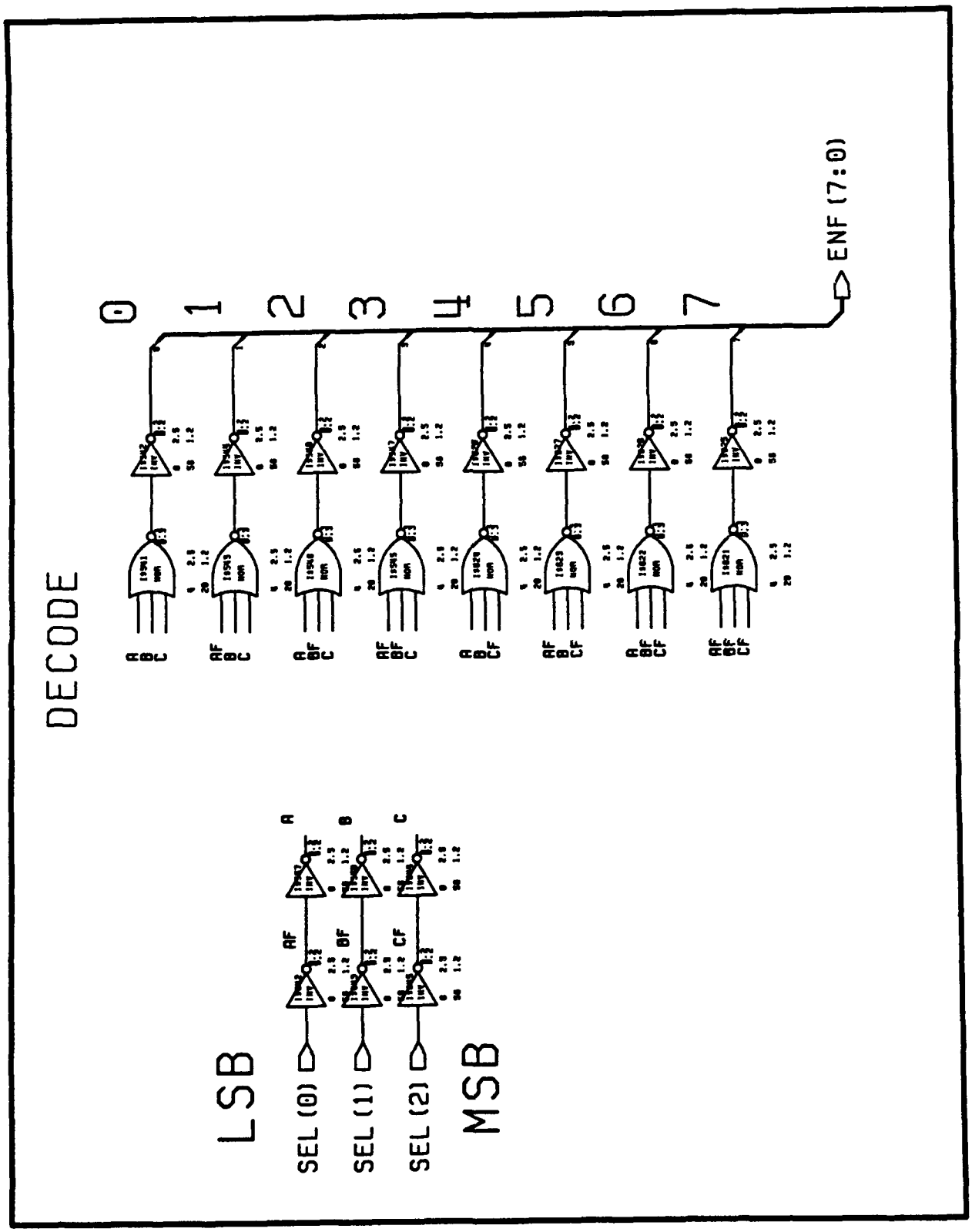

CSFDEC
UXX
FAR(15:14)
CSF(3:0)
OUT
IN

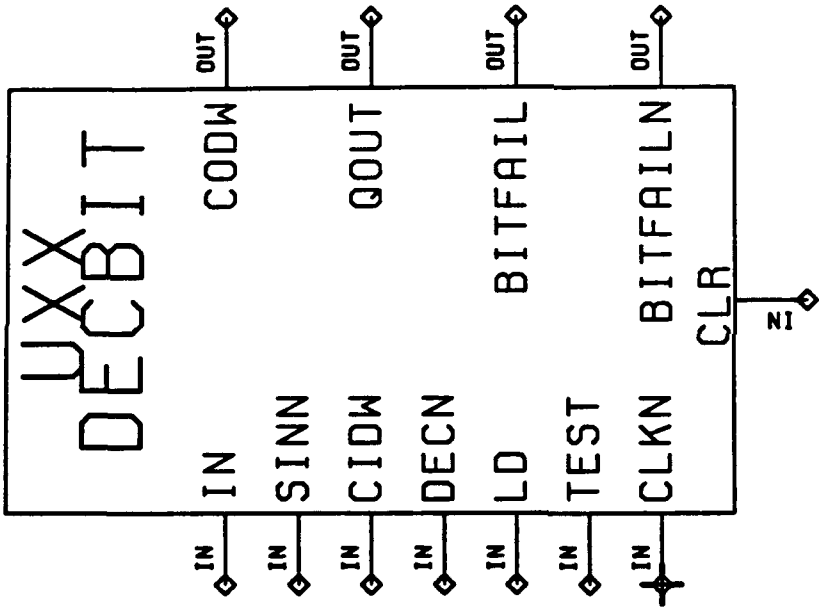

CSF (0)
CSF (1)
CSF (2)
CSF (3)
FAR (14)
FAR (15)

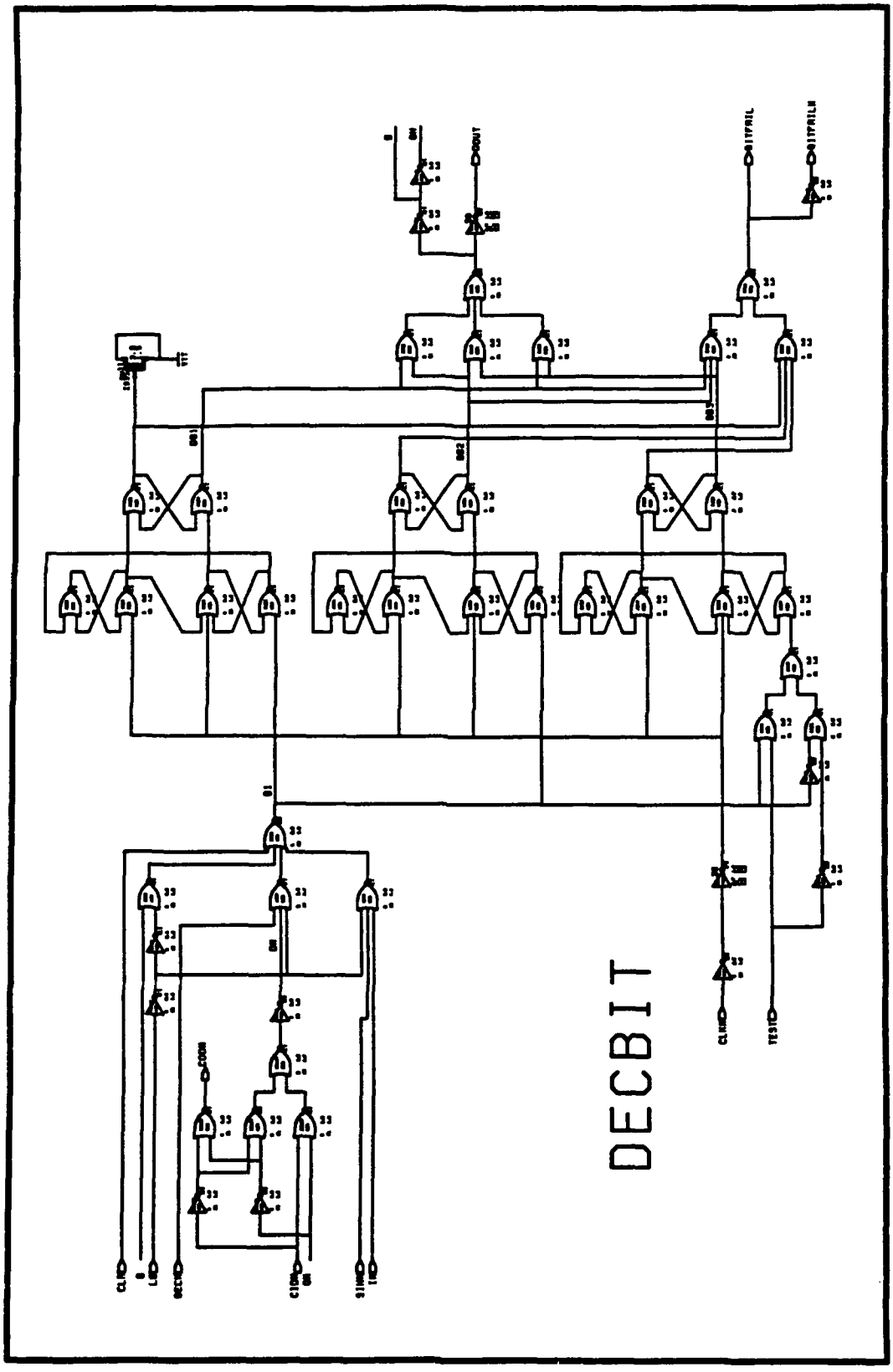

OUT
OUT
OUT
DBDDEC
UXX
LDIMR
LDECC
LDVEC
DBD(4:0)
IN

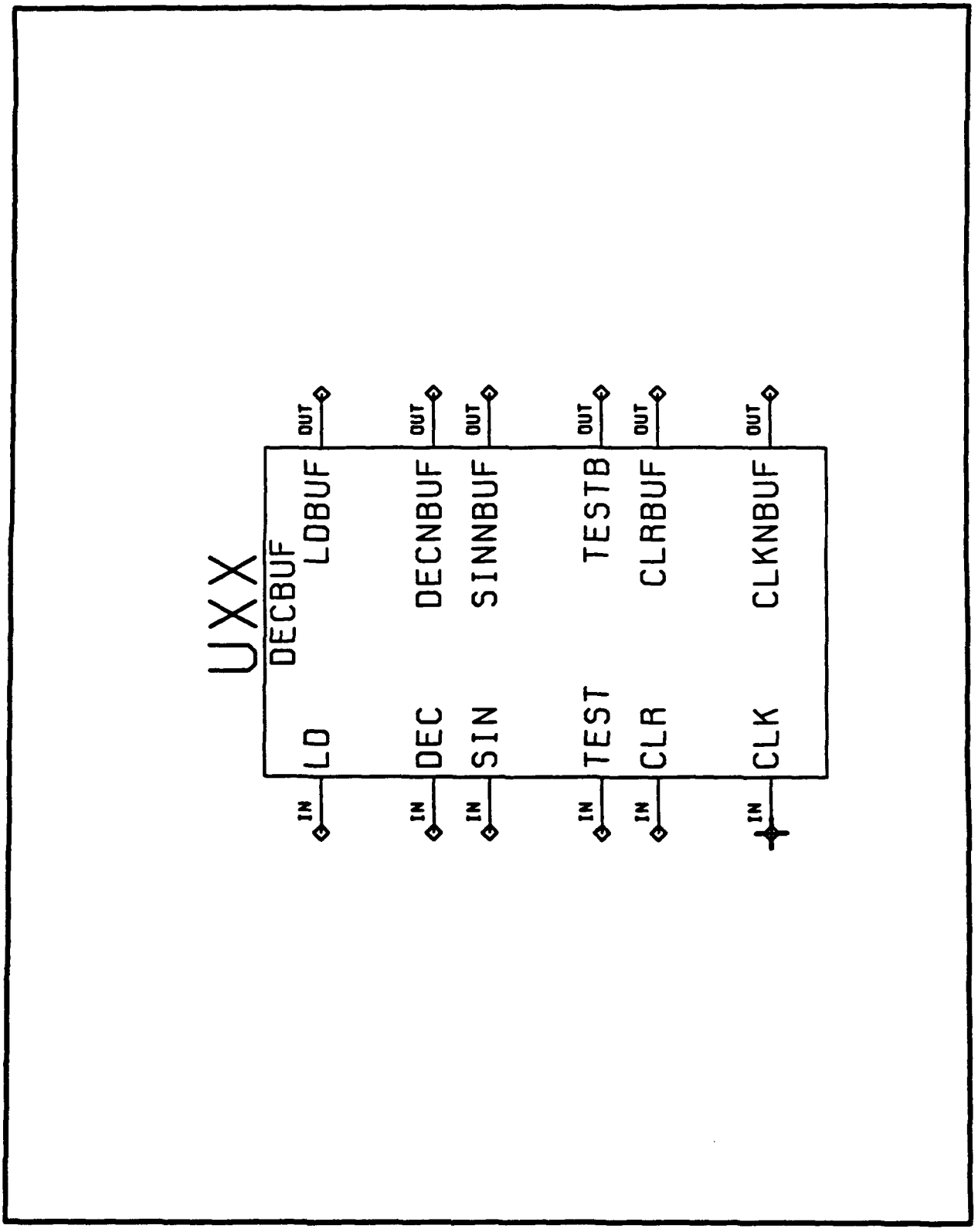

LDMR
LDECC
LDVEC
SO
SO
SO
Decode 7
Decode F
Decode 6
OBDEC
OBD (4)
OBD (3)
OBD (2)
OBD (1)
OBD (8)
ALULO

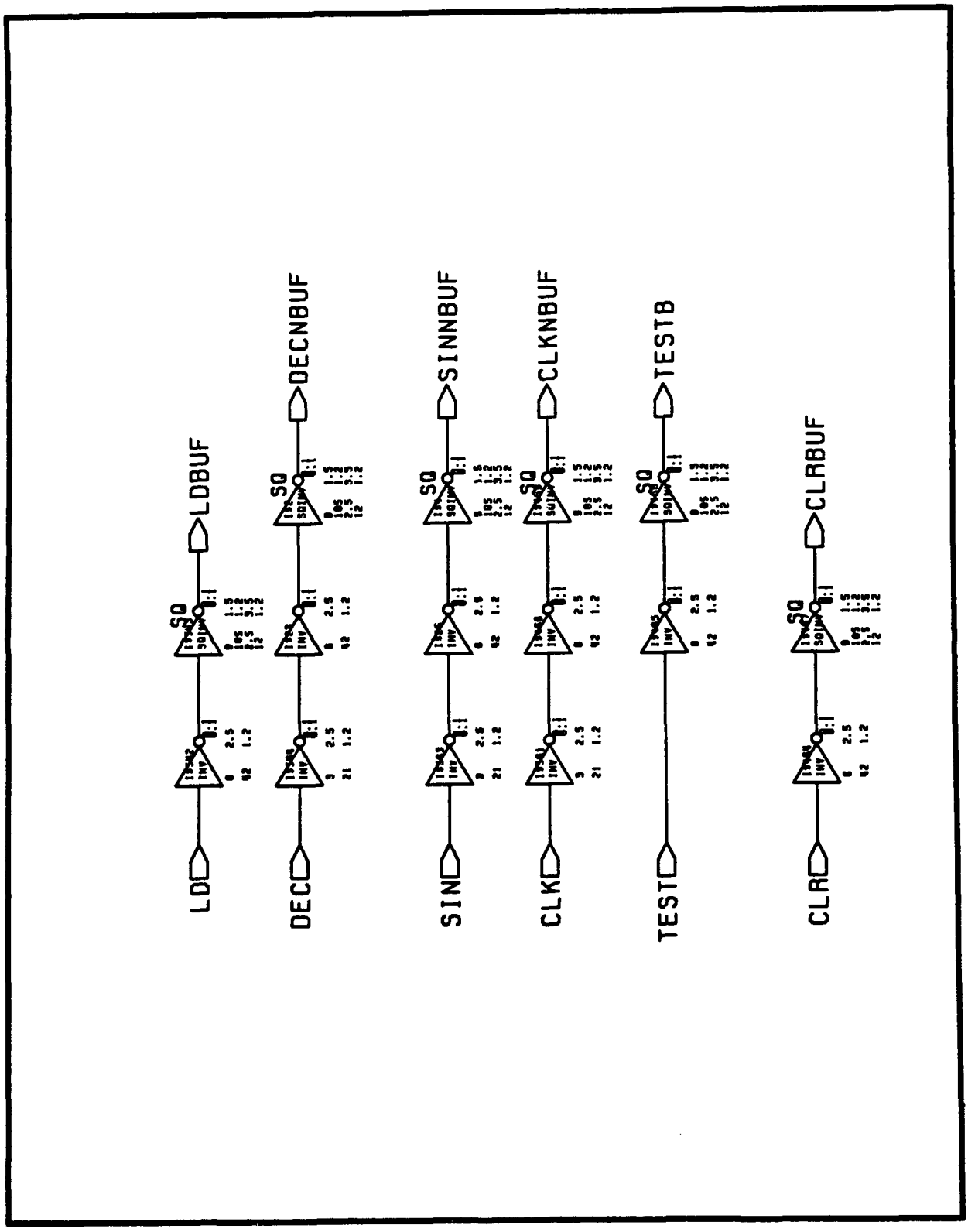

UXX
DEC3T08F
ENF (7:0)
SEL (2:0)
out
in

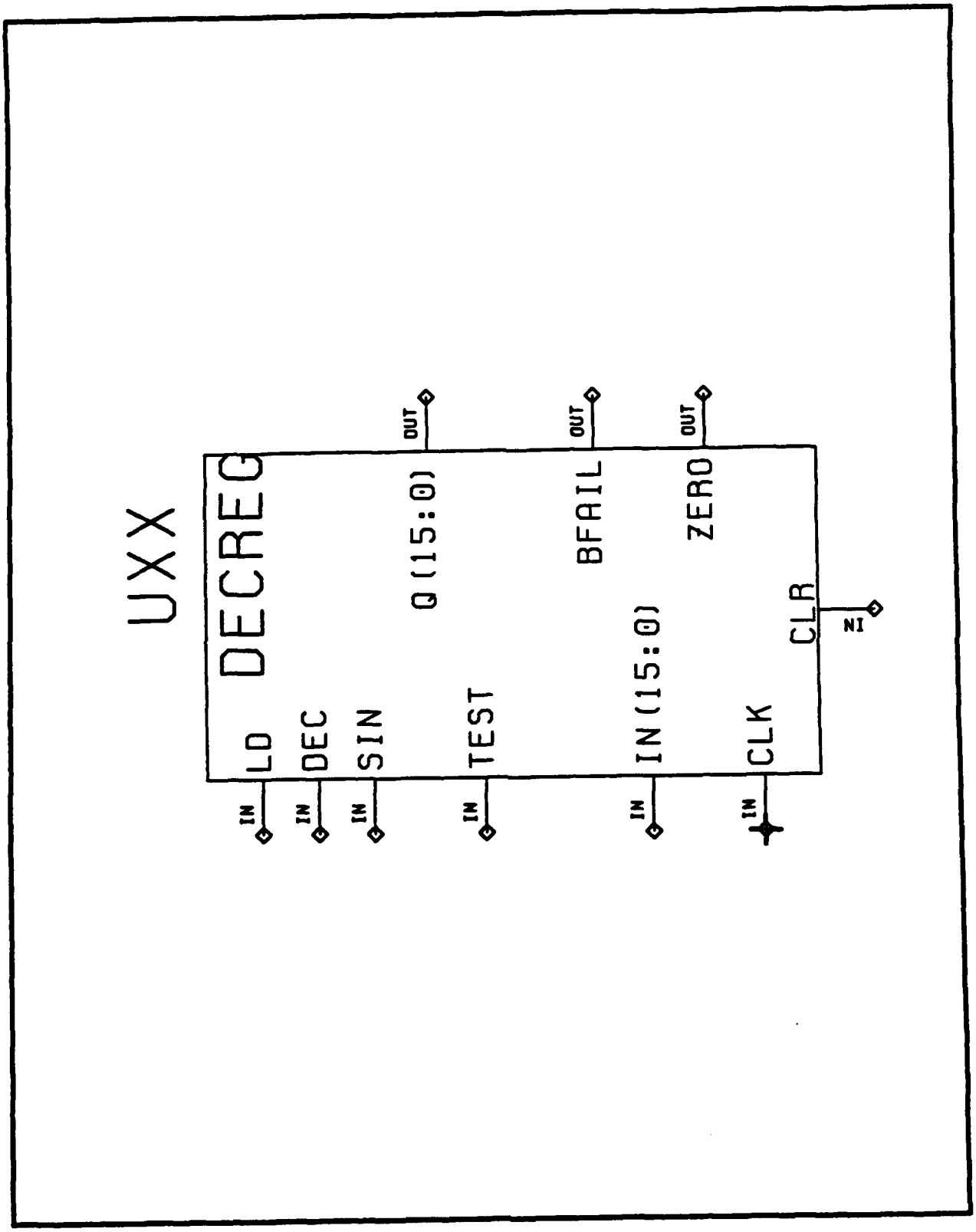

DECODE
0
1
2
3
4
5
6
7
ENF (7:0)
A B C
AF B C
A BF C
AF BF C
A B CF
AF B CF
A BF CF
AF BF CF
A
B
C
AF
BF
CF
LSB
SEL (0)
SEL (1)
SEL (2)
MSB

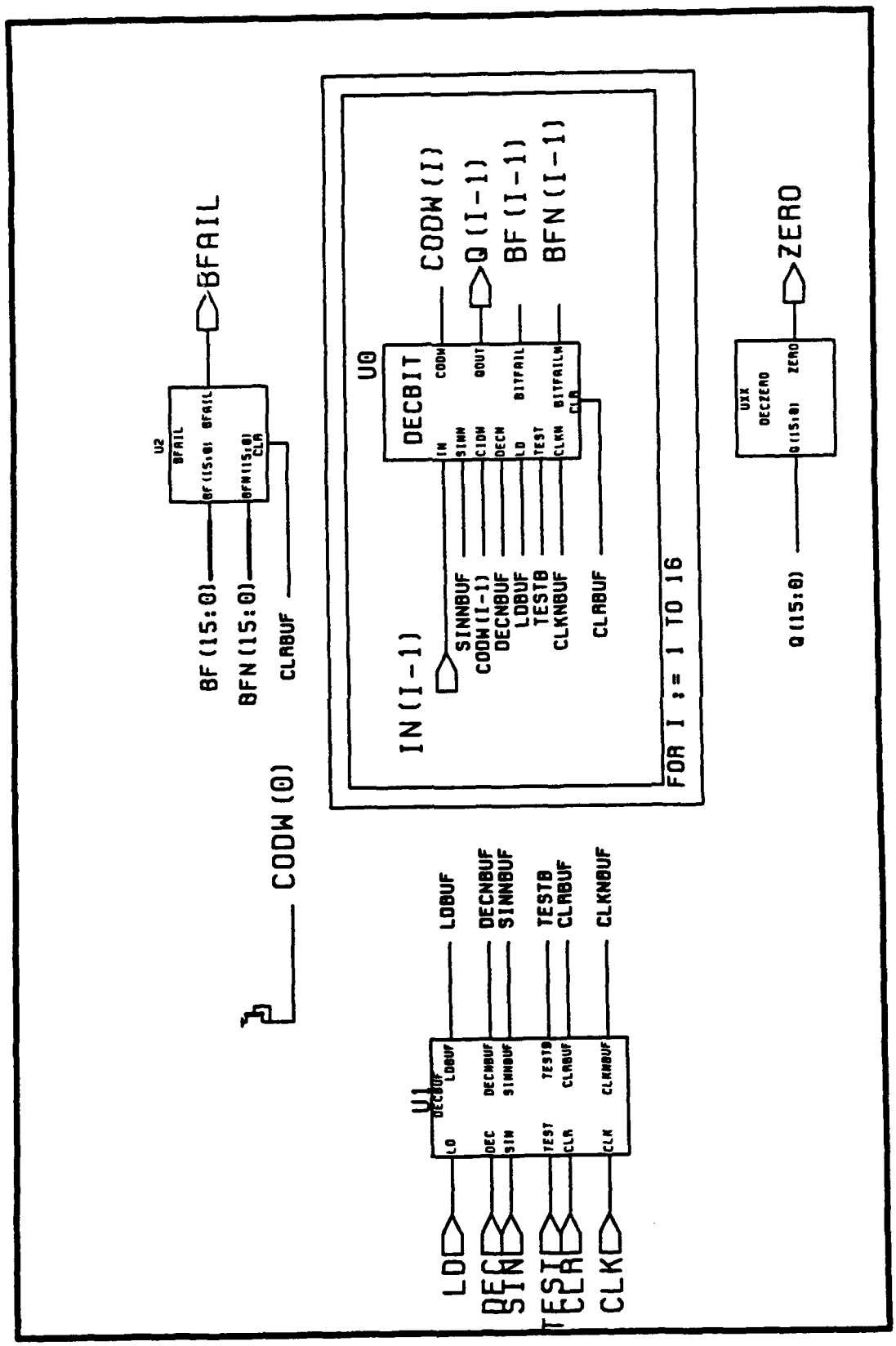

UXX
DECBIT
OUT
CODW
OUT
QOUT
OUT
BITFAIL
OUT
BITFAILN
CLR
NI
IN
SINN
CIDW
DECN
LD
TEST
CLKN
IN
IN
IN
IN
IN
IN
IN

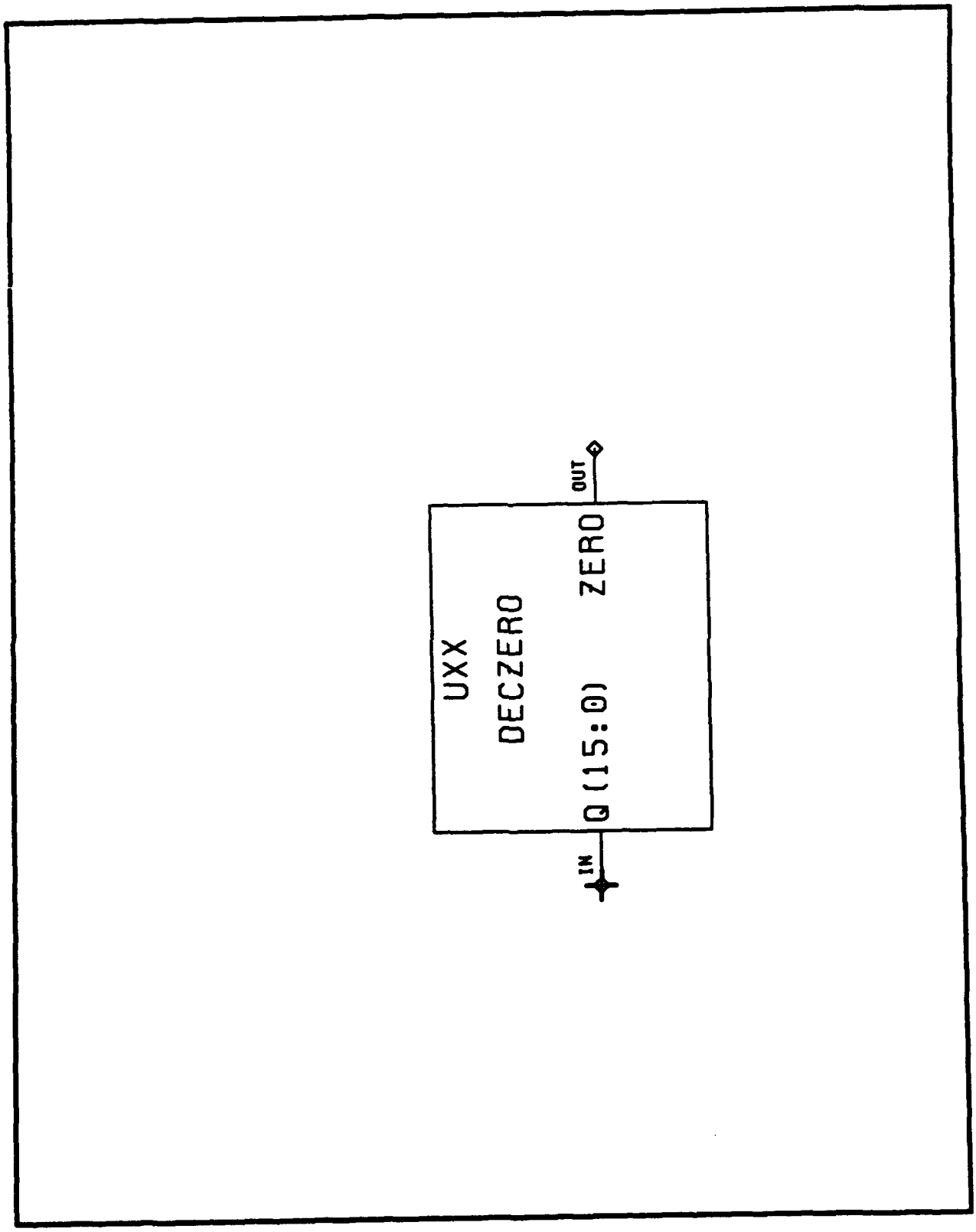

DECBIT

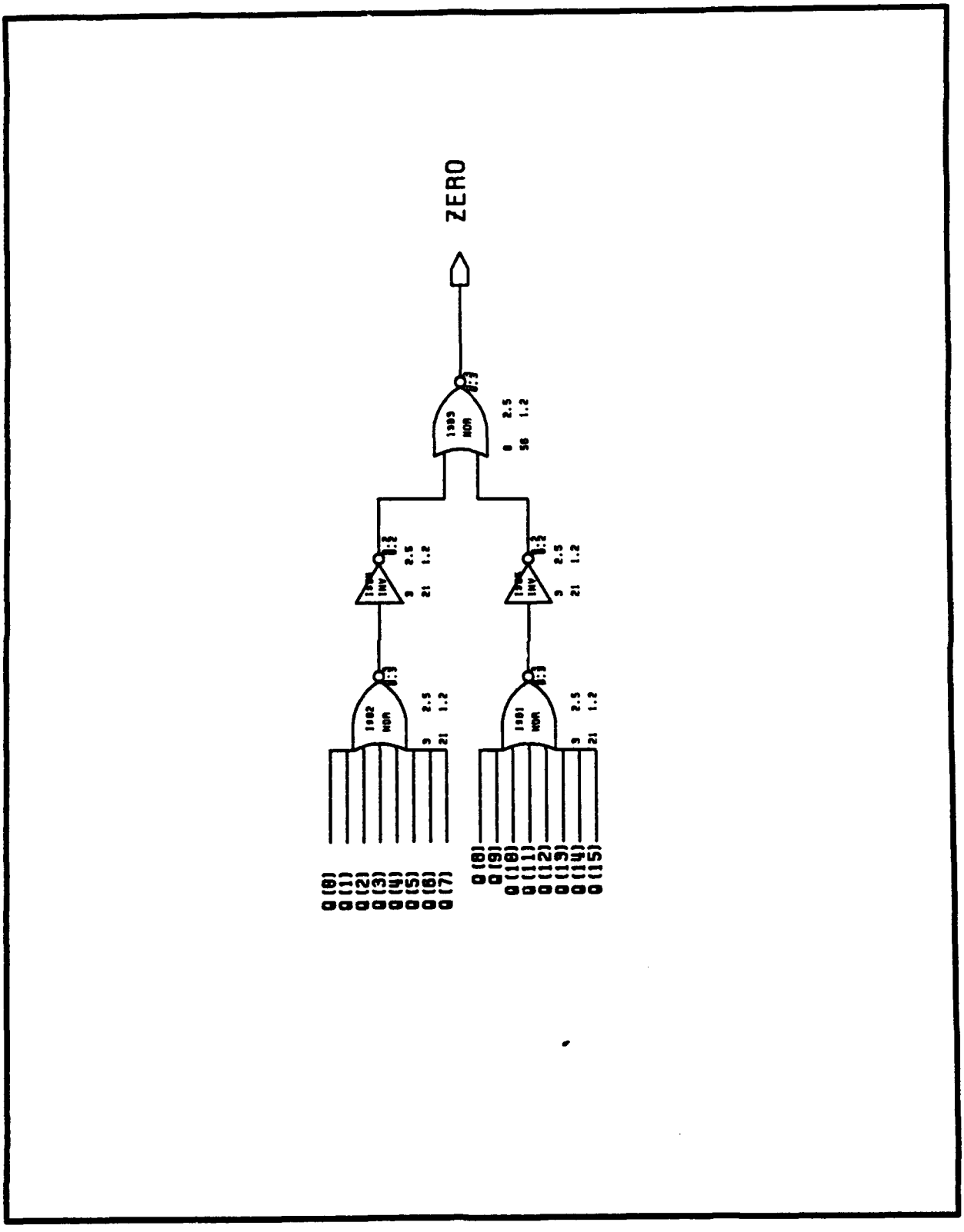

UXX
DECBUF
LDBUF
DECNBUF
SINNBUF
TESTB
CLRBUF
CLKNBUF
LD
DEC
SIN
TEST
CLR
CLK
OUT
IN

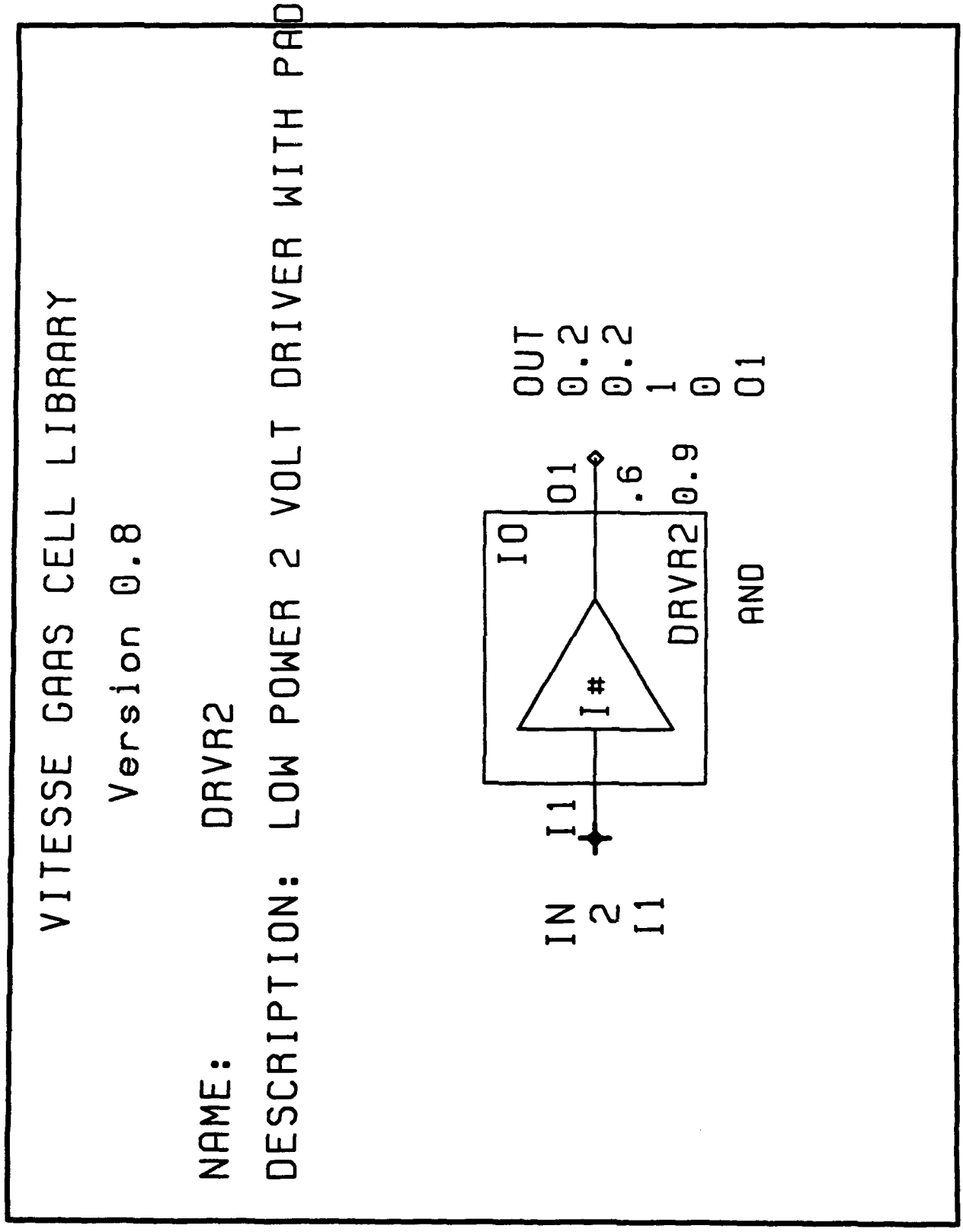

LDBUF
DECNBUF
SINNBUF
CLKNBUF
TESTB
CLRBUF
SQ
LD
DEC
SIN
CLK
TEST
CLR

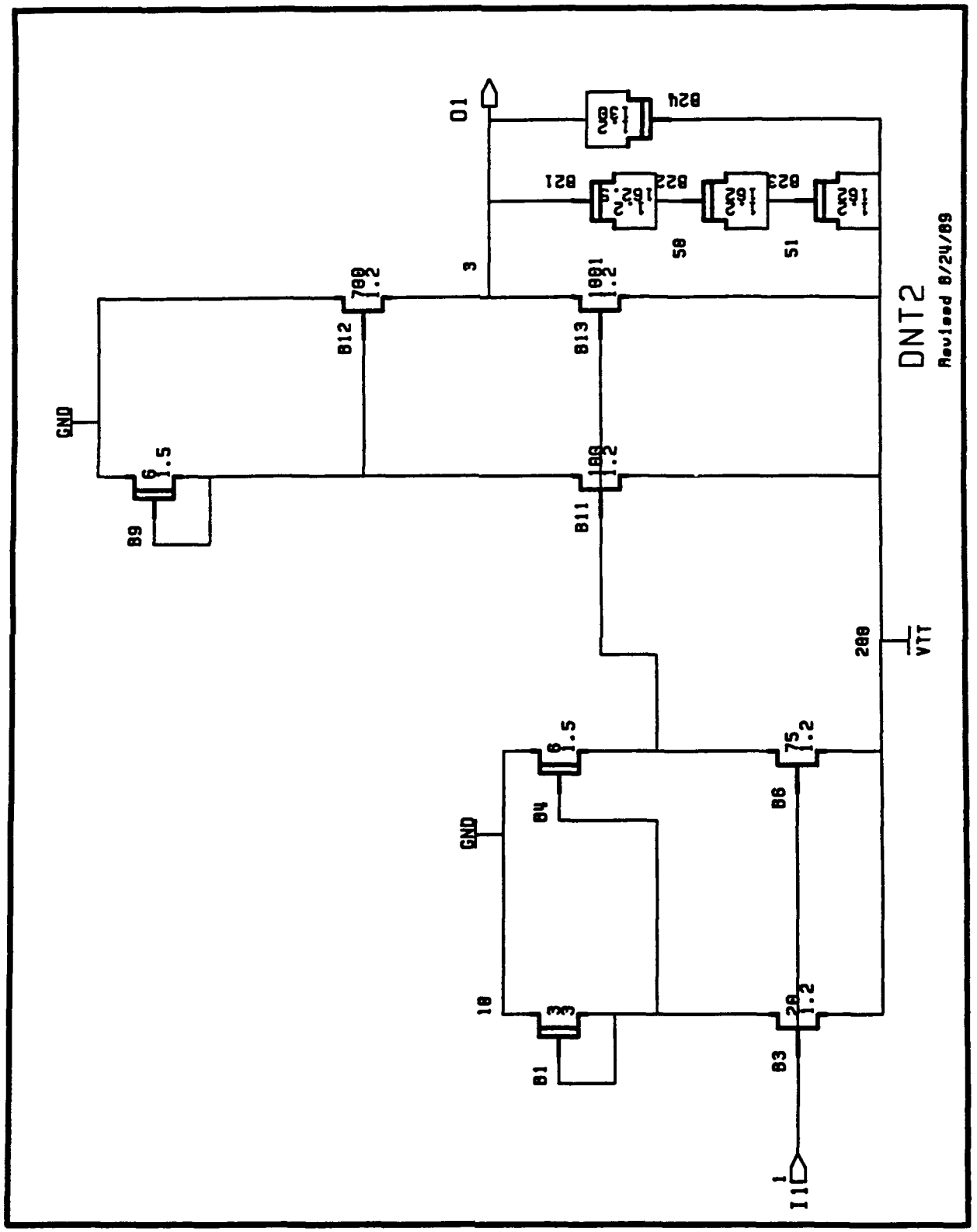

UXX
DECREG
LD
DEC
SIN
TEST
IN(15:0)
CLK
CLR
Q(15:0)
BFAIL
ZERO
IN
IN
IN
IN
IN
IN
OUT
OUT
OUT
NI

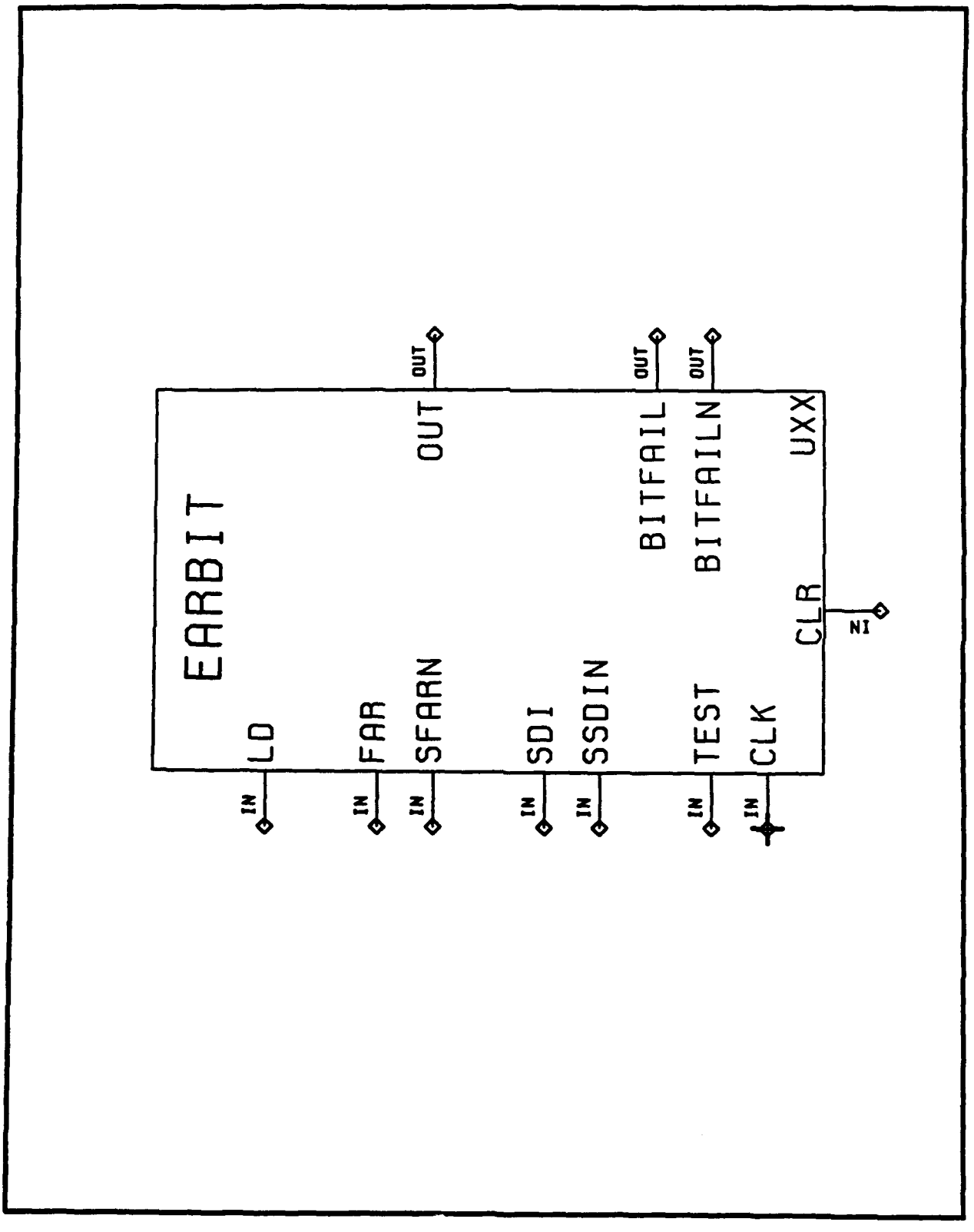

BFAIL
ZERO
U2
BFAIL
BF[15:0]
BFN[15:0]
CLR
BF(15:0)
BFN(15:0)
CLRBUF
U0
DECBIT
IN
SINN
CIDN
DECN
LD
TEST
CLKN
CODW
DOUT
BITFAIL
BITFAILN
CLR
CODW(I)
Q(I-1)
BF(I-1)
BFN(I-1)
IN(I-1)
SINNBUF
CODW(I-1)
DECNBUF
LDBUF
TESTB
CLKNBUF
CLRBUF
FOR I := 1 TO 16
UXX
DECZERO
D[15:0]
ZERO
Q(15:0)
CODW(0)
U1
DECBUF
LDBUF
DECNBUF
SINNBUF
TESTB
CLRBUF
CLKNBUF
LD
DEC
SIN
TEST
CLR
CLK

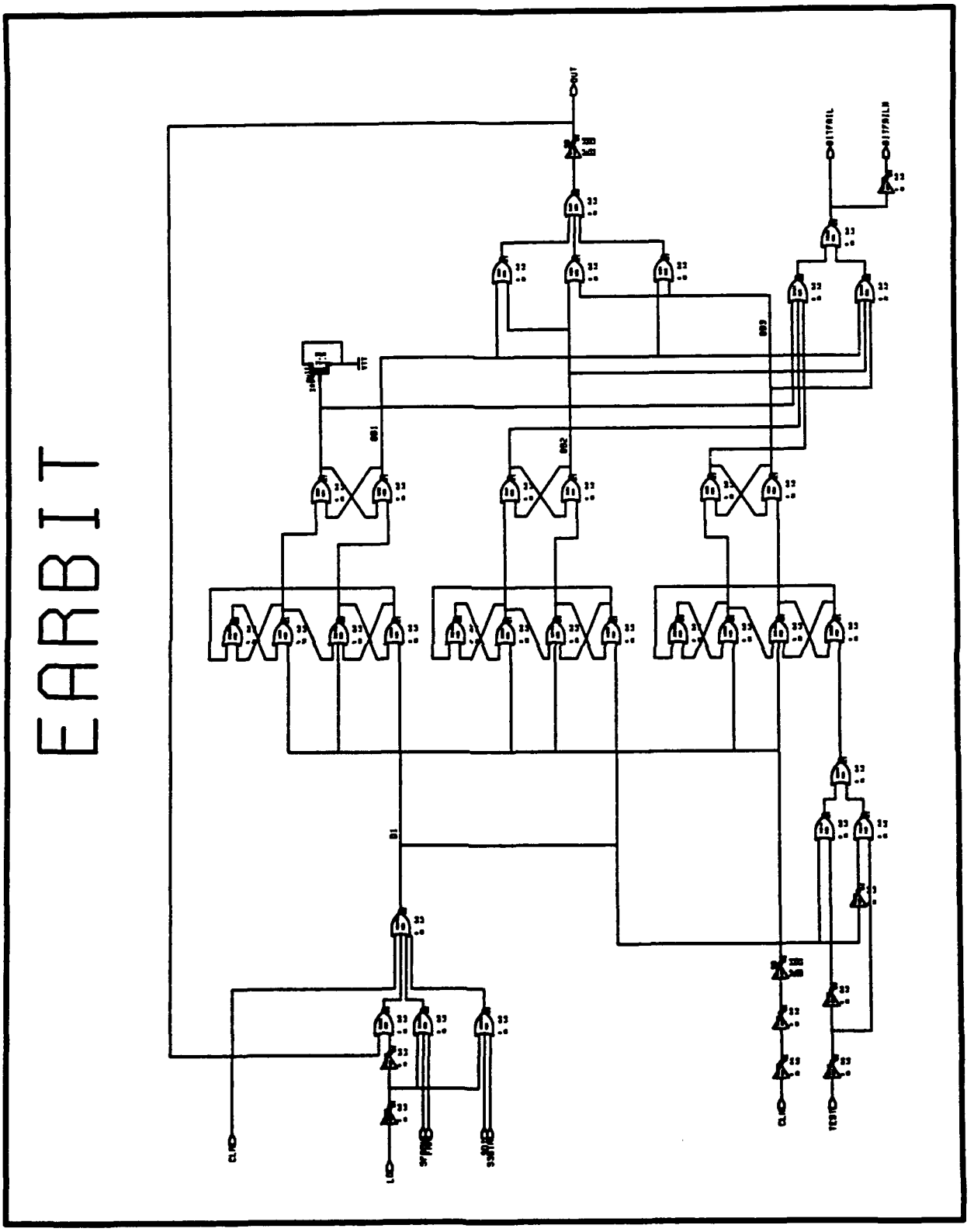

OUT
ZERO
UXX
DECZERO
Q(15:0)
IN

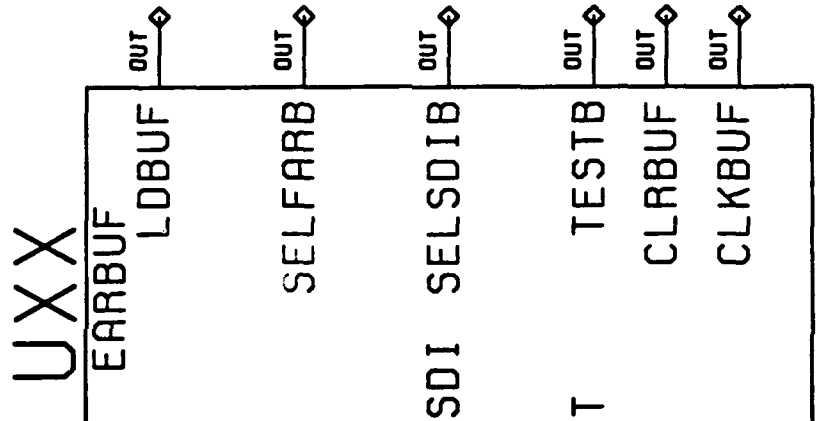

ZERO
(8)
(9)
(10)
(11)
(12)
(13)
(14)
(15)
(0)
(1)
(2)
(3)
(4)
(5)
(6)
(7)

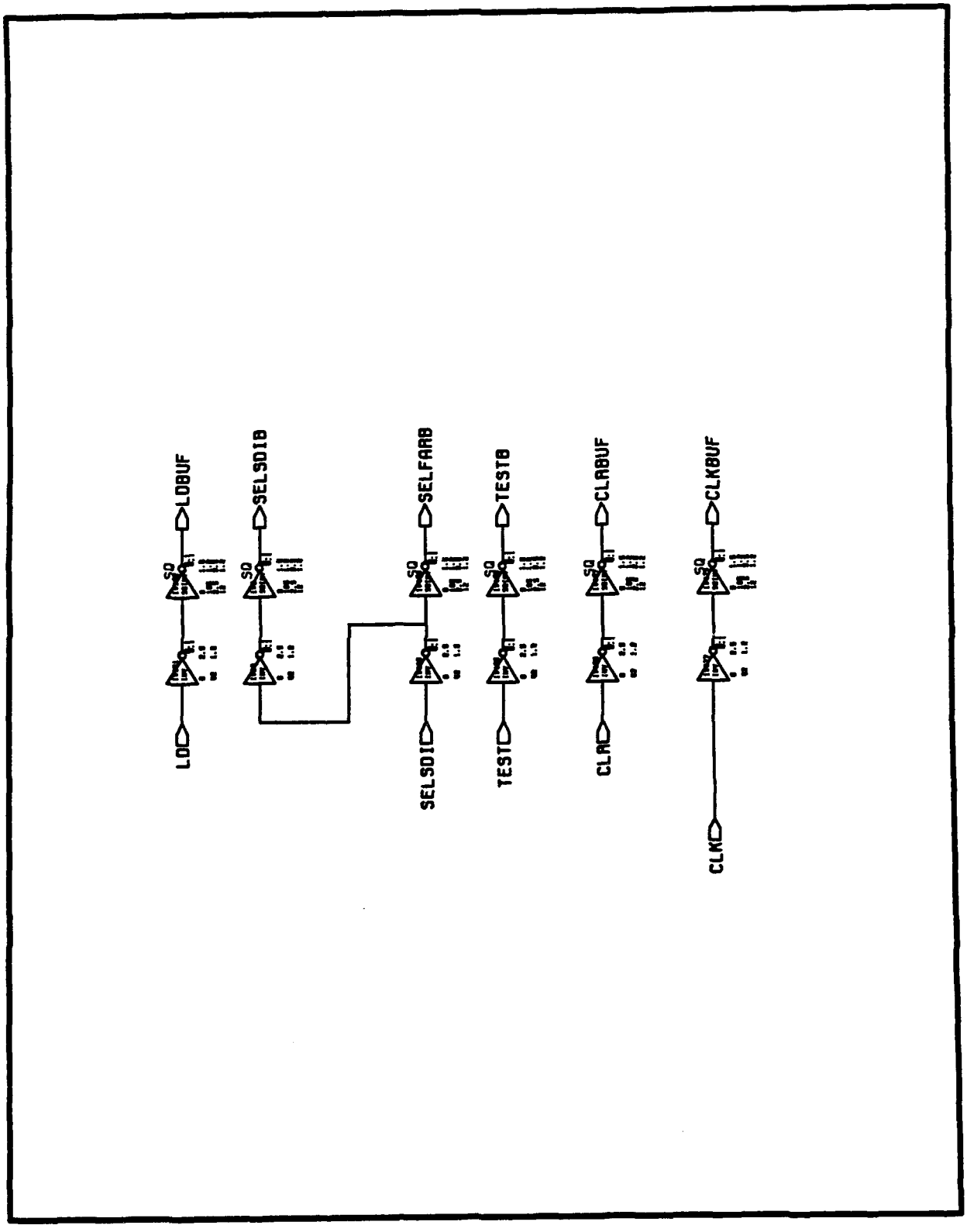

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: DRVR2
DESCRIPTION: LOW POWER 2 VOLT DRIVER WITH PAD
OUT
0.2
0.2
1
0
01
IO
O1
.6
0.9
DRVR2
I#
AND
IN
2
I1
I1

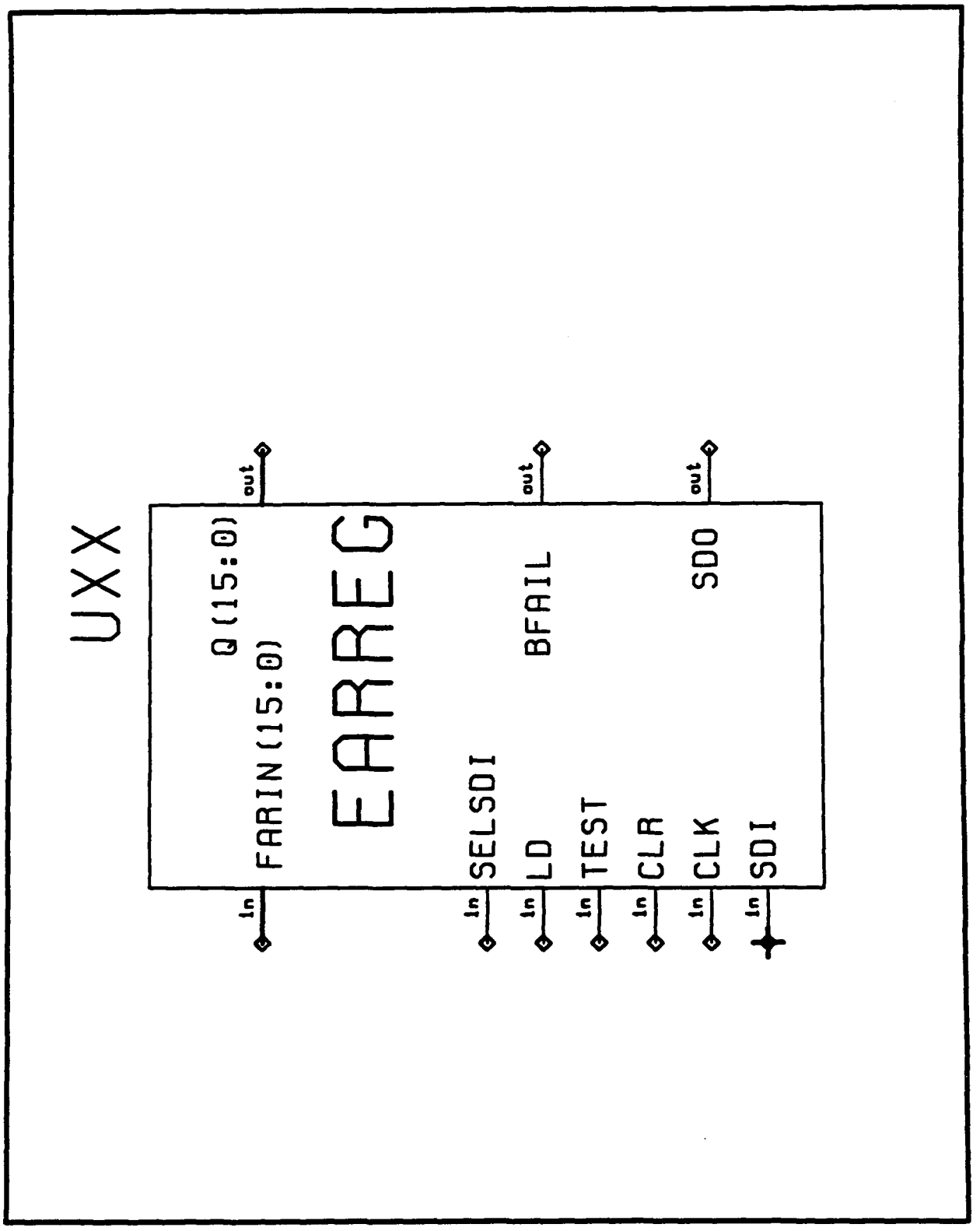

O1
B24
B21
B22
B23
50
51
3
B12
B13
GND
B9
B11
200
VTT
B4
B6
GND
10
B1
B3
I1
DNT2
Revised 8/24/89

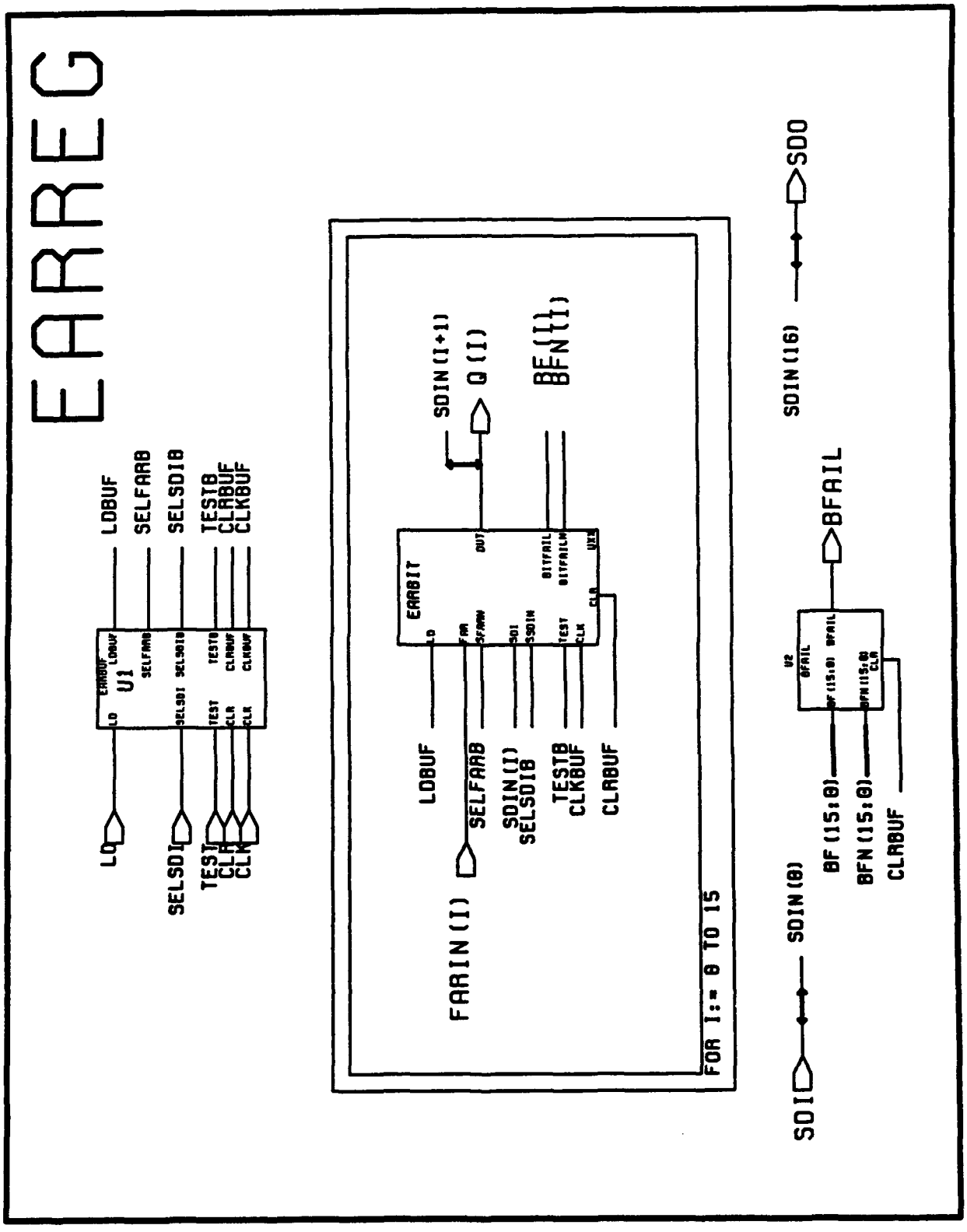

EARBIT
LD
FAR
SFARN
SDI
SSDIN
TEST
CLK
CLR
BITFAILN
BITFAIL
OUT
UXX
IN
OUT
NI

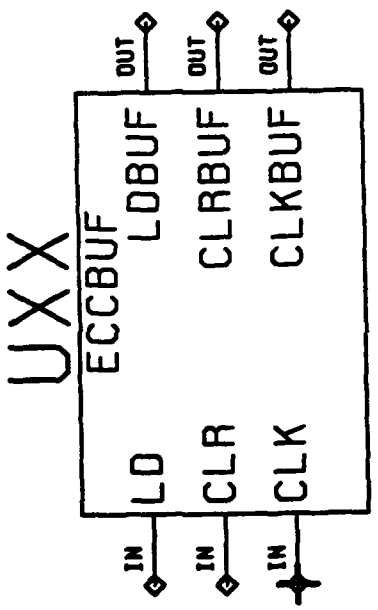

EARBIT

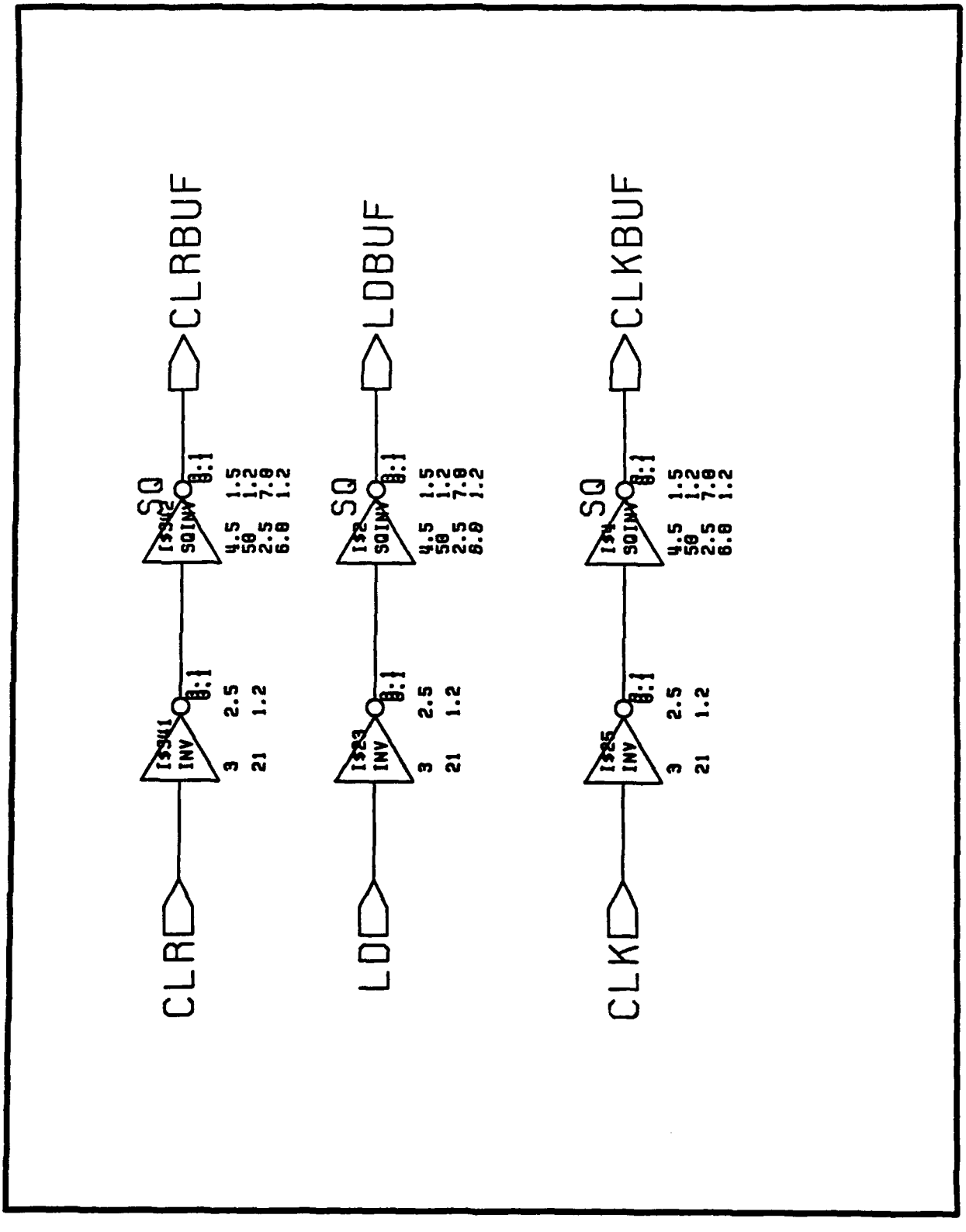

UXX
EARBUF
LDBUF
SELFARB
SELSDIB
TESTB
CLRBUF
CLKBUF
LD
SELSDI
TEST
CLR
CLK
OUT
IN

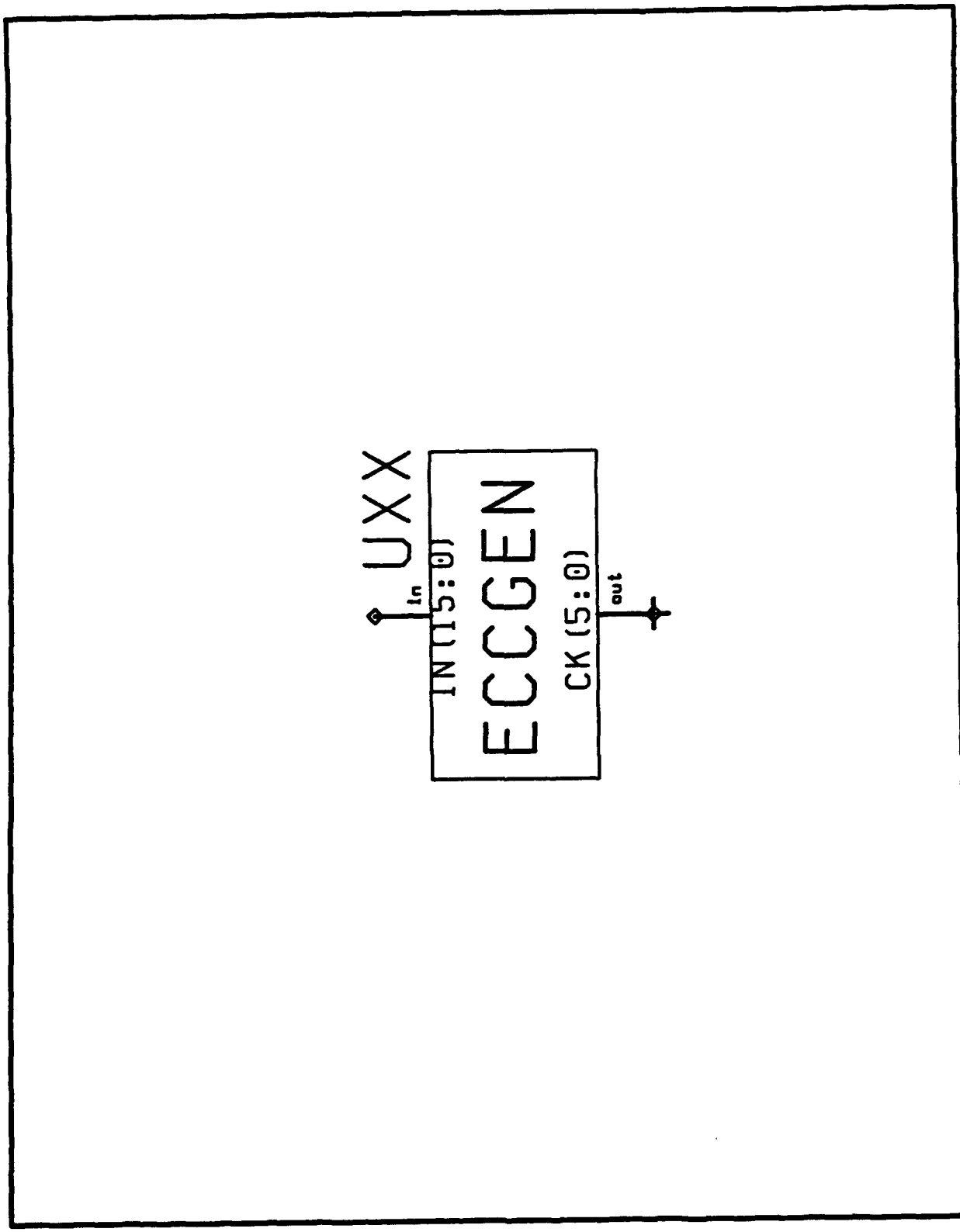

LDBUF
SELSDIB
SELFARB
TESTB
CLABUF
CLKBUF
LD
SELSDI
TEST
CLA
CLK

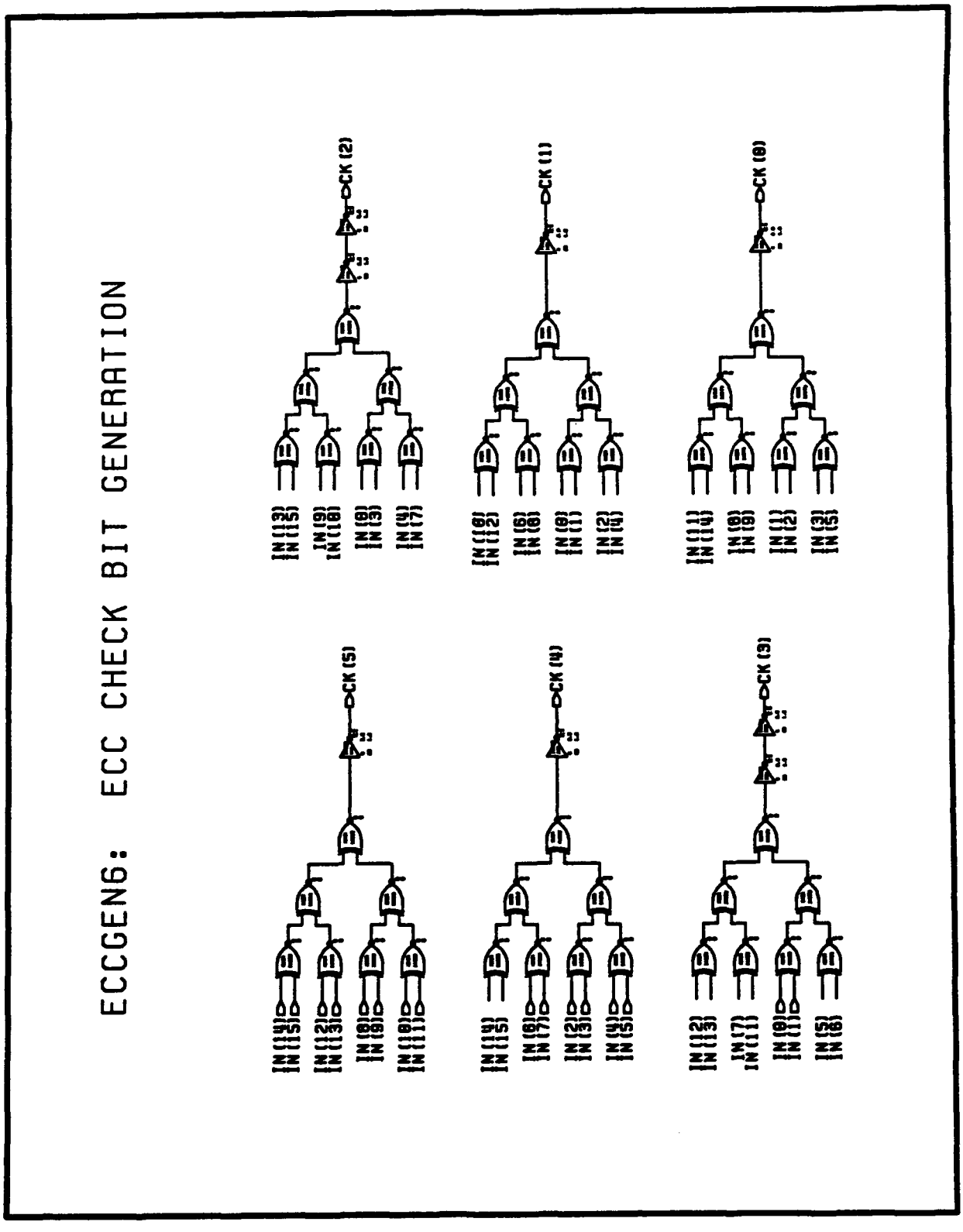

UXX
EARREG
Q(15:0)
FARIN(15:0)
BFAIL
SDO
SELSDI
LD
TEST
CLR
CLK
SDI
out
out
out
in
in
in
in
in
in

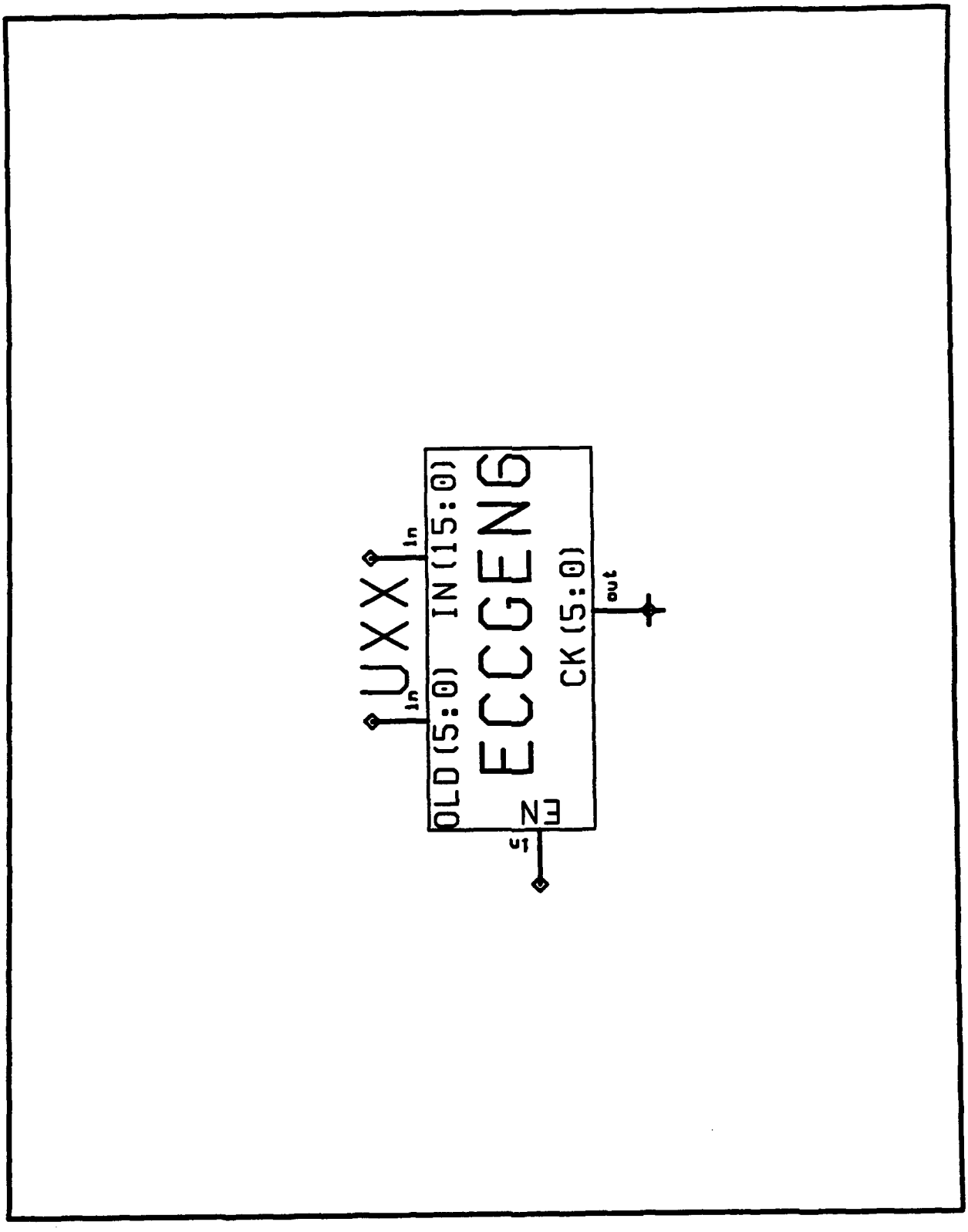

EARREG
LDBUF
SELFARB
SELSDIB
TESTB
CLRBUF
CLKBUF
U1
LD
SELSDI
TEST
CLR
CLK
SDIN(I+1)
Q(I)
BFN(I)
EARBIT
LDBUF
SELFARB
FARIN(I)
SDIN(I)
SELSDIB
TESTB
CLKBUF
CLRBUF
FOR I:= 0 TO 15
SDIN(16)
SDO
BFAIL
U2
SDIN(0)
BF(15:0)
BFN(15:0)
CLRBUF
SDI

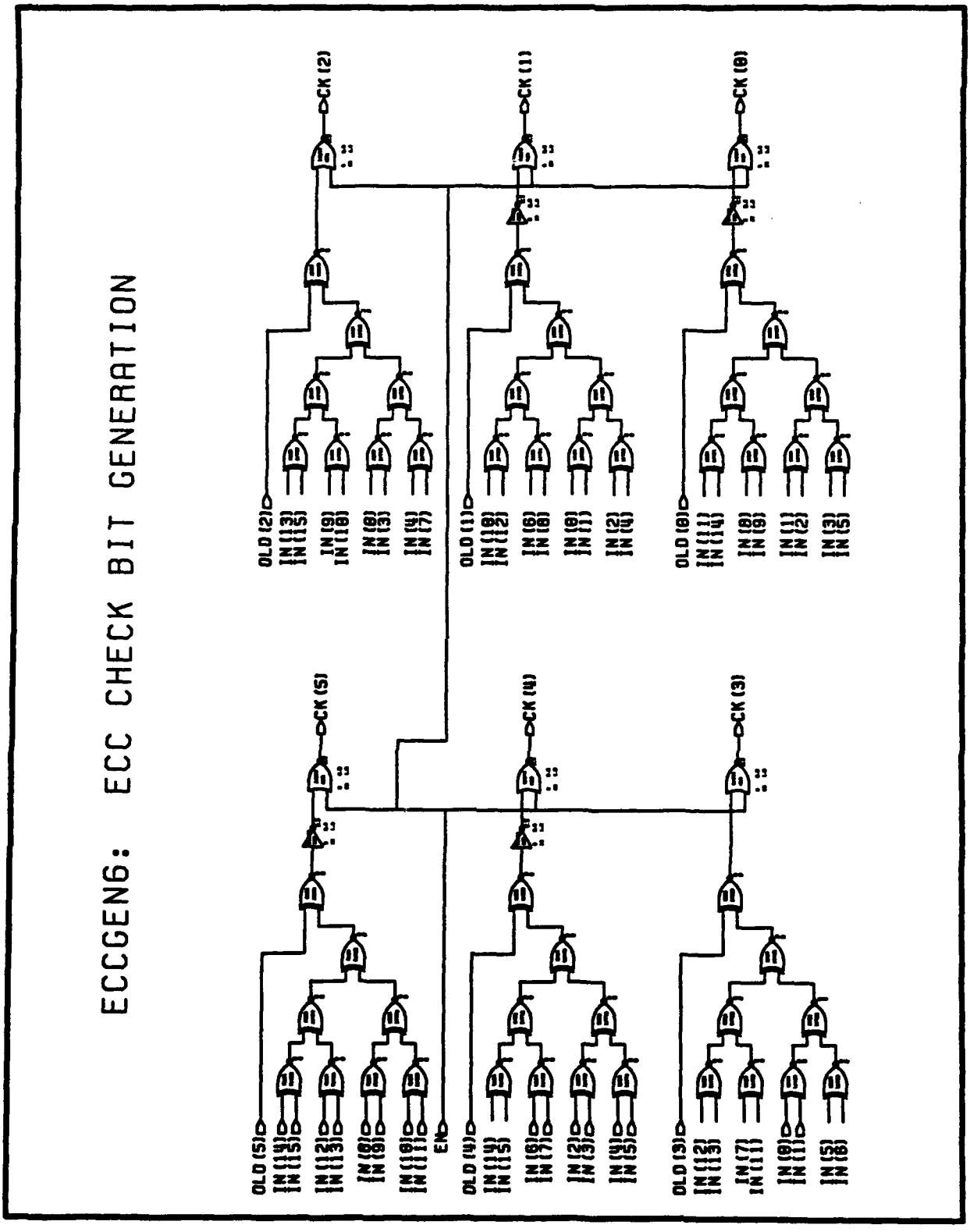

UXX
ECCBUF
LDBUF
CLRBUF
CLKBUF
OUT
OUT
OUT
LD
CLR
CLK
IN
IN
IN

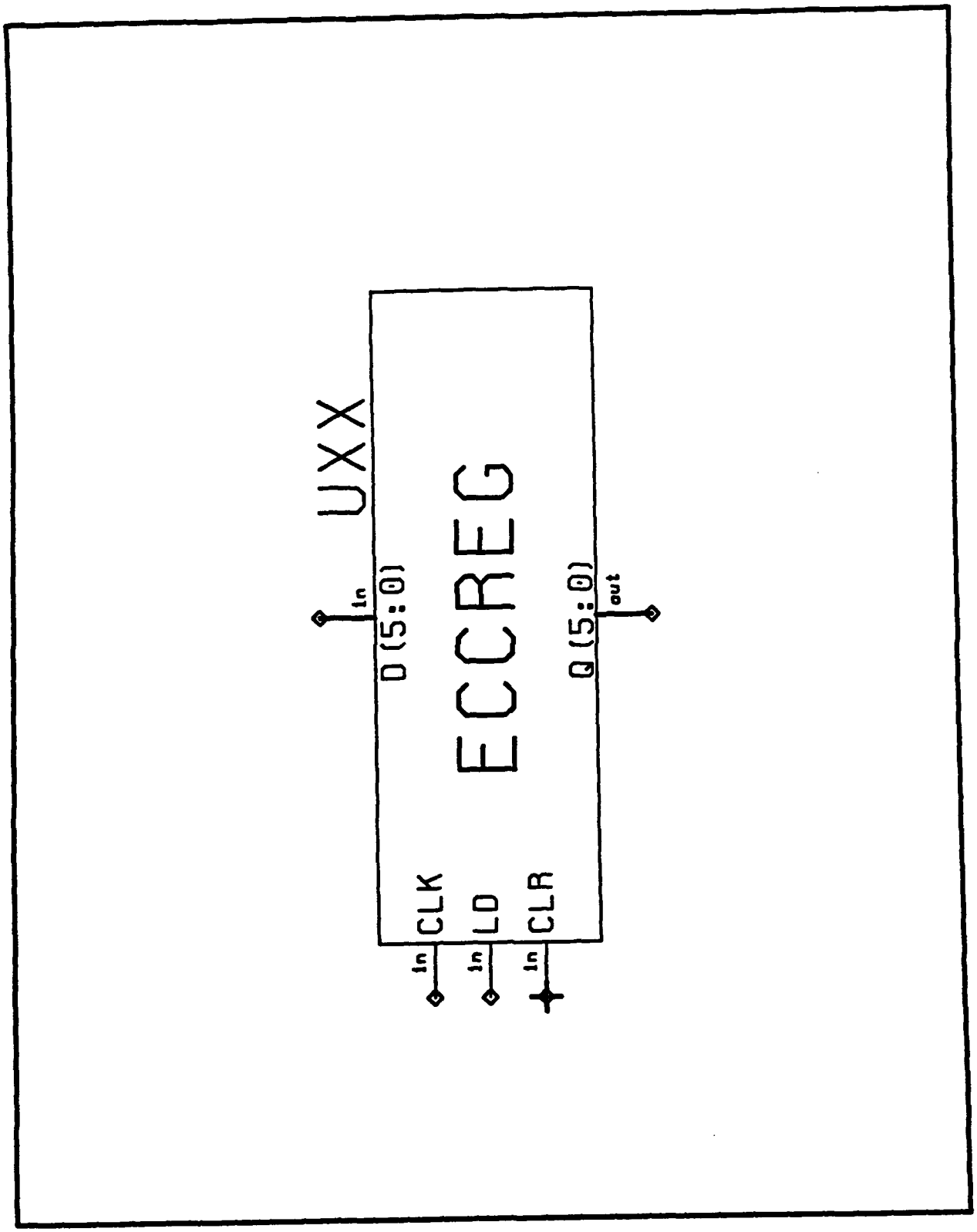

CLRBUF
LDBUF
CLKBUF
SQ
SQ
SQ
8:1
8:1
8:1
4.5 1.5
50 1.2
2.5 7.0
6.0 1.2
3 2.5
21 1.2
INV
SQINV
CLR
LD
CLK

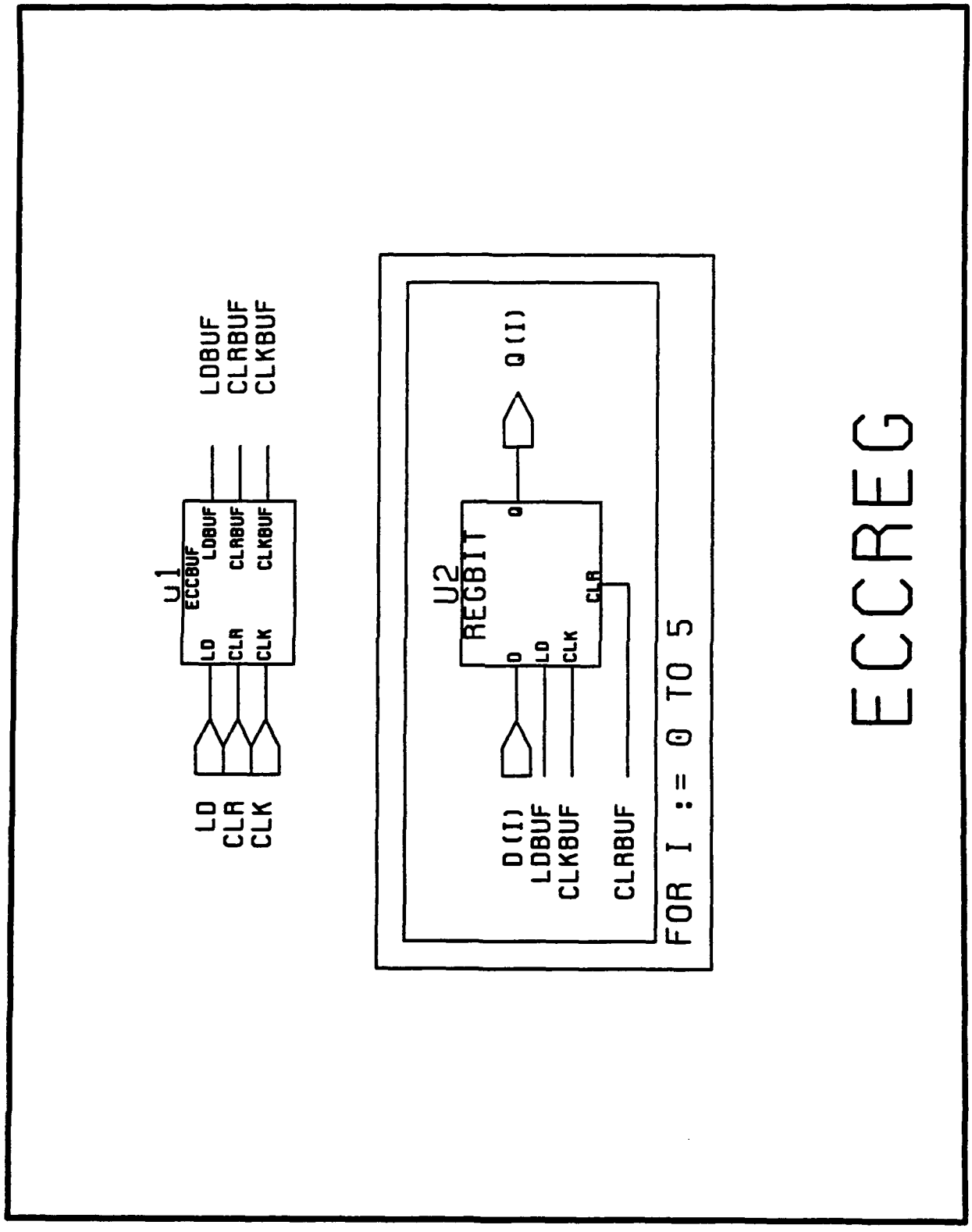

UXX
in
IN[15:0]
ECCGEN
CK[5:0]
out

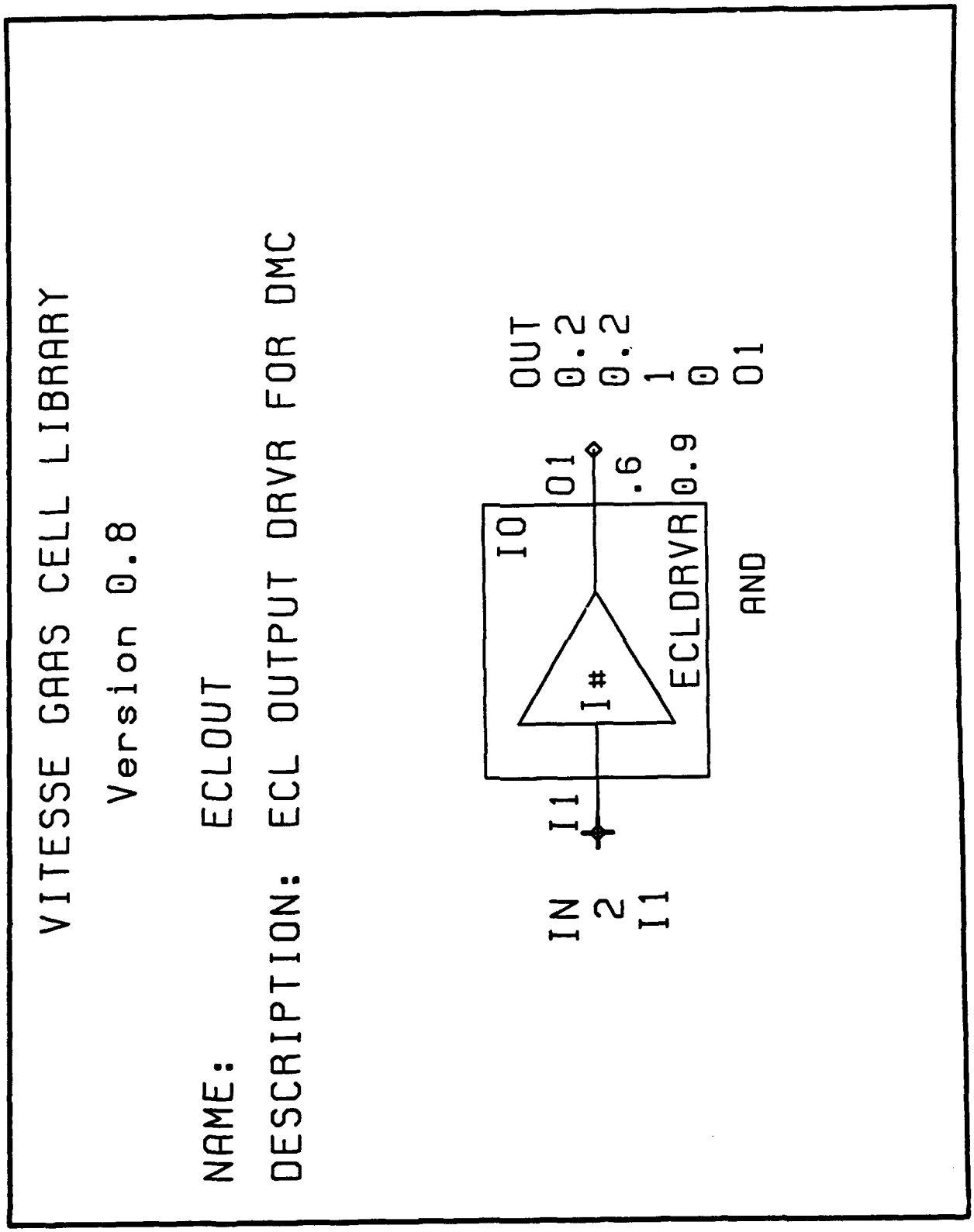

ECCGEN6: ECC CHECK BIT GENERATION
CK (2)
CK (1)
CK (0)
CK (5)
CK (4)
CK (3)

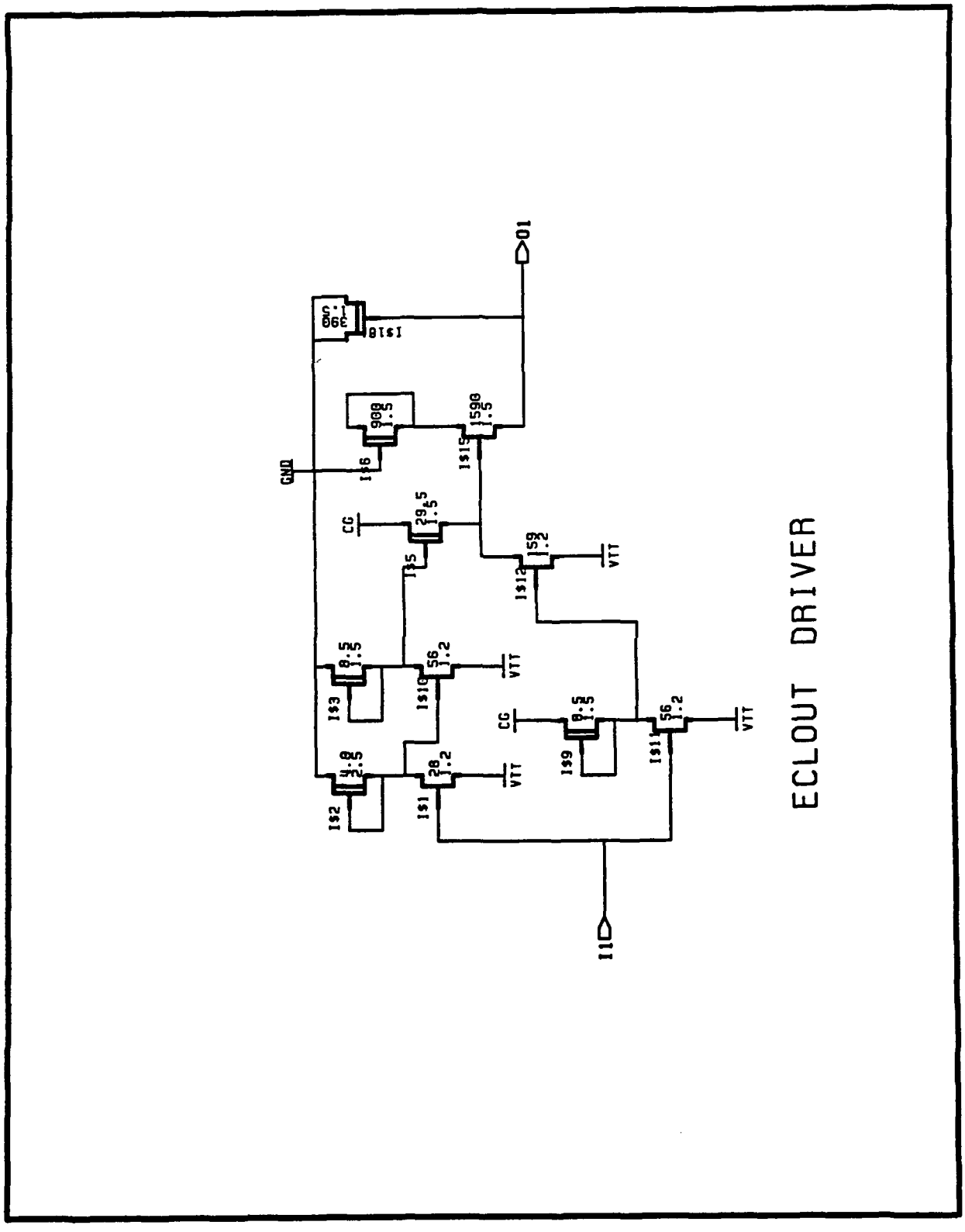

UXX
in
in
OLD(5:0)
IN(15:0)
ECCGEN6
EN
CK(5:0)
out
in

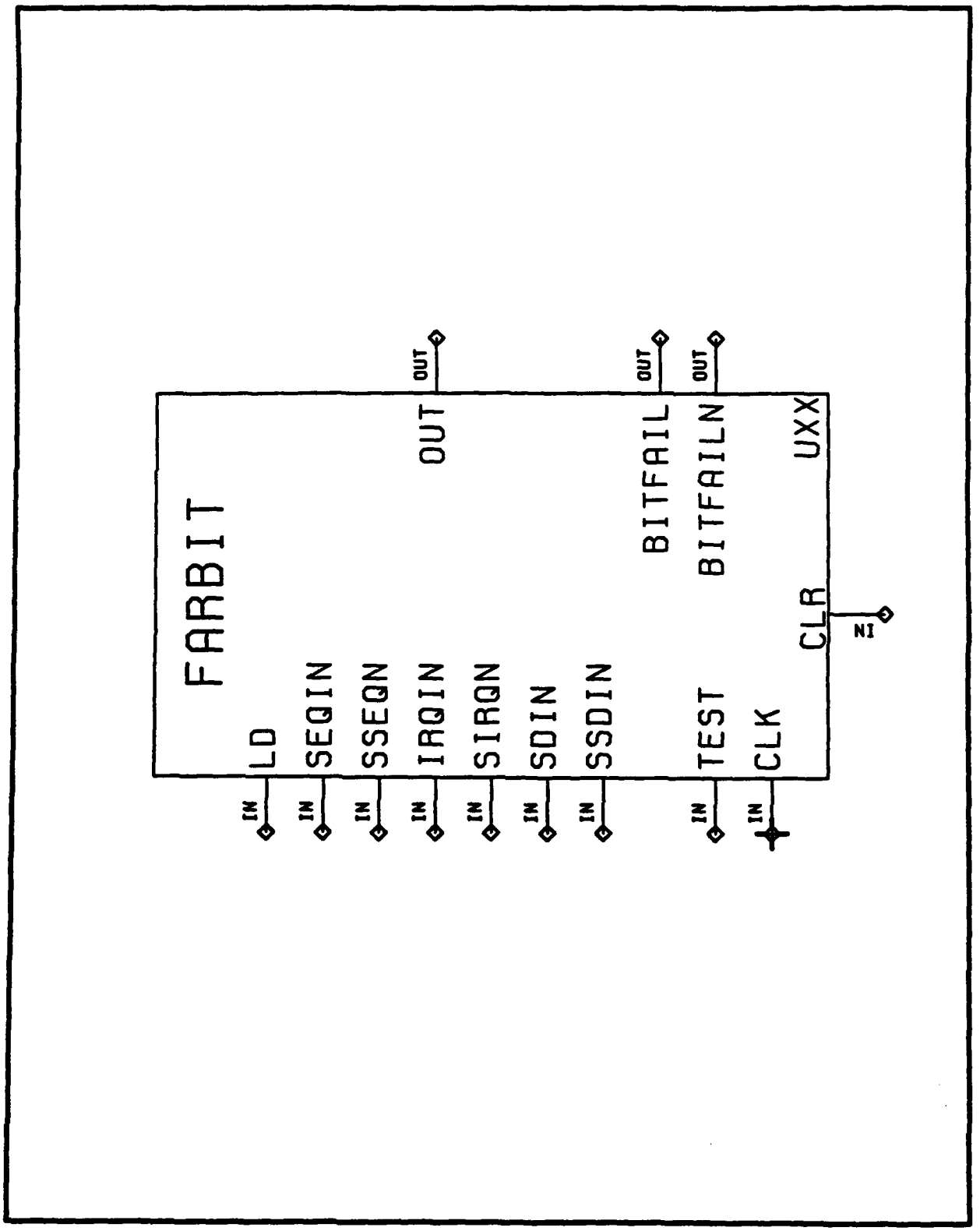

ECCGEN6: ECC CHECK BIT GENERATION
CK (2)
CK (1)
CK (0)
CK (5)
CK (4)
CK (3)
OLD (2)
IN (13)
IN (15)
IN (9)
IN (10)
IN (8)
IN (13)
IN (4)
IN (7)
OLD (1)
IN (10)
IN (12)
IN (6)
IN (8)
IN (0)
IN (1)
IN (2)
IN (4)
OLD (0)
IN (11)
IN (14)
IN (8)
IN (9)
IN (1)
IN (2)
IN (3)
IN (5)
OLD (5)
IN (14)
IN (15)
IN (12)
IN (13)
IN (8)
IN (9)
IN (10)
IN (11)
EN
OLD (4)
IN (14)
IN (15)
IN (6)
IN (7)
IN (2)
IN (3)
IN (4)
IN (5)
OLD (3)
IN (12)
IN (13)
IN (7)
IN (11)
IN (0)
IN (1)
IN (5)
IN (8)

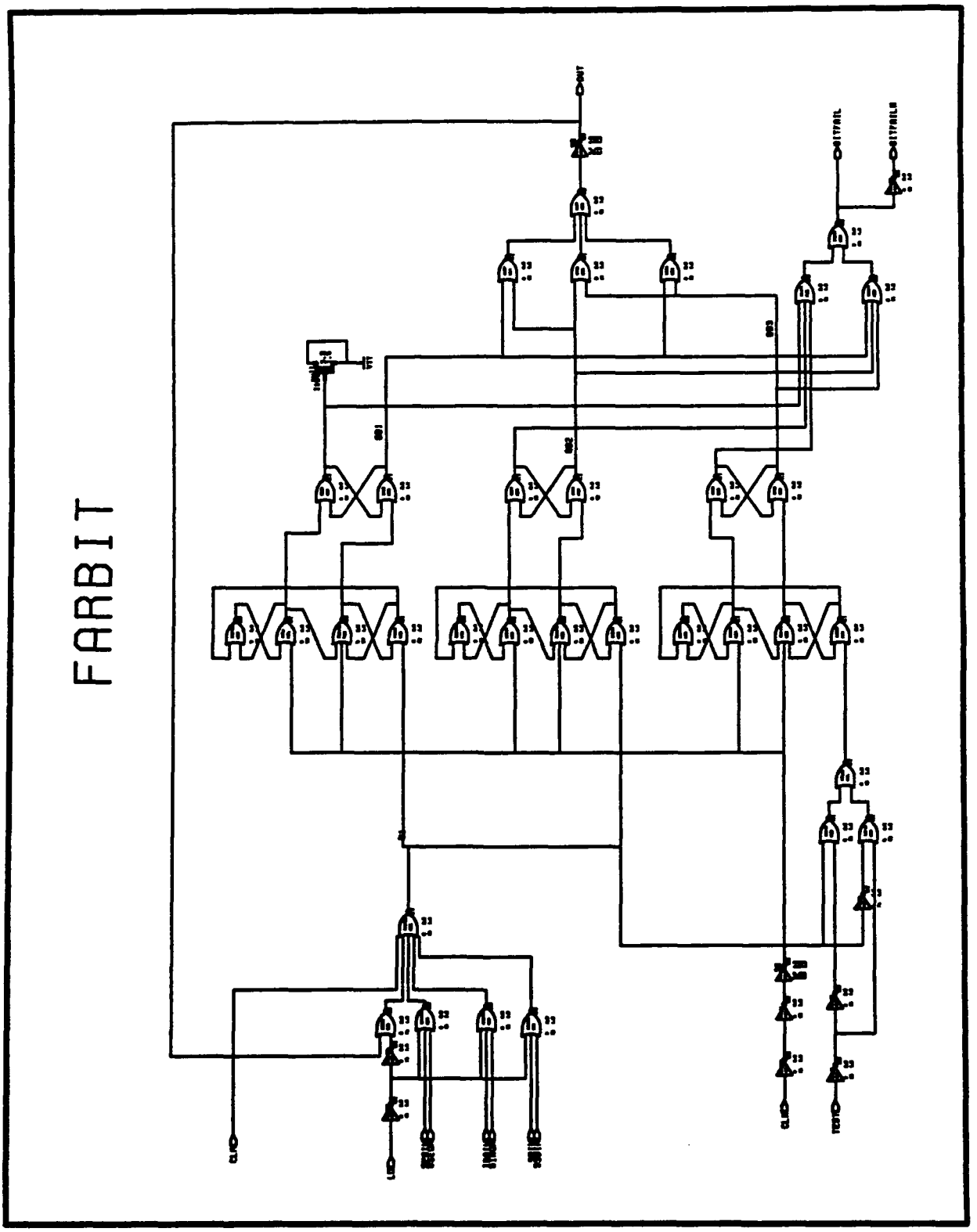

UXX
ECCREG
in
D(5:0)
Q(5:0)
out
CLK
LD
CLR
in
in
in

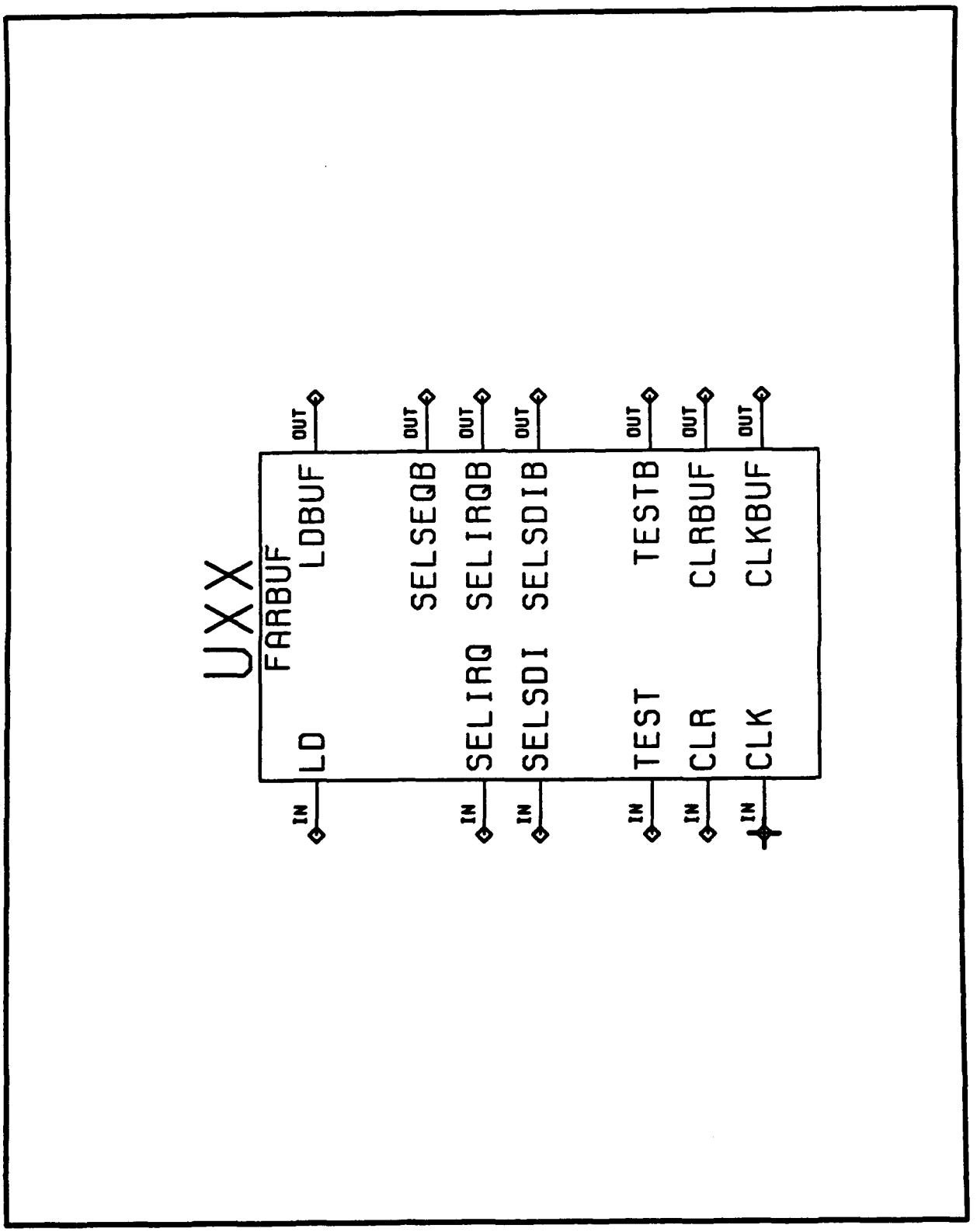

ECCREG
U1
ECCBUF
LDBUF
CLRBUF
CLKBUF
LD
CLR
CLK
LDBUF
CLRBUF
CLKBUF
LD
CLR
CLK
U2
REGBIT
Q(I)
D
Q
LD
CLK
CLR
D(I)
LDBUF
CLKBUF
CLRBUF
FOR I := 0 TO 5

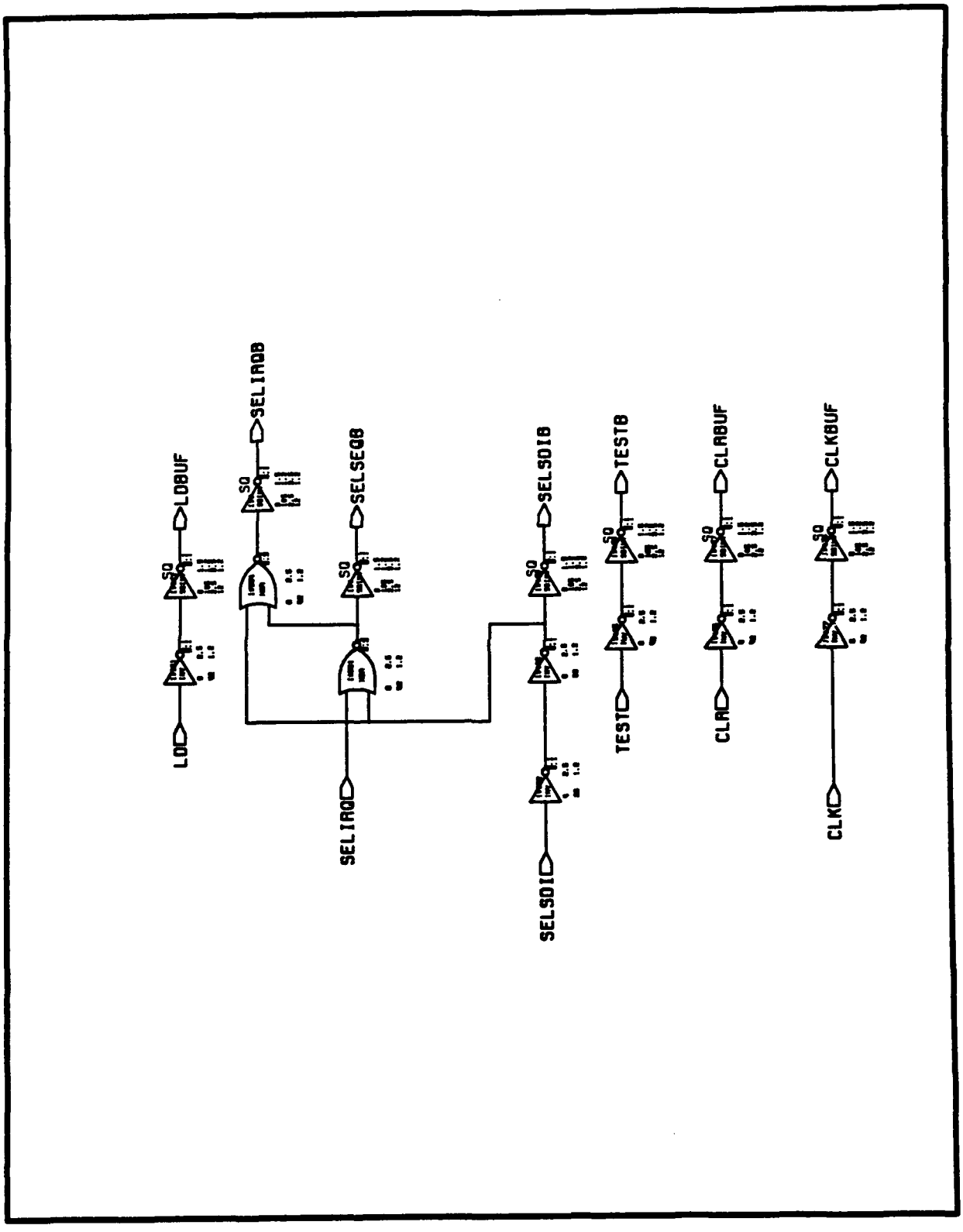

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: ECLOUT
DESCRIPTION: ECL OUTPUT DRVR FOR DMC
IN
2
I1
I1
IO
O1
I#
.6
0.9
ECLDRVR
AND
OUT
0.2
0.2
1
0
O1

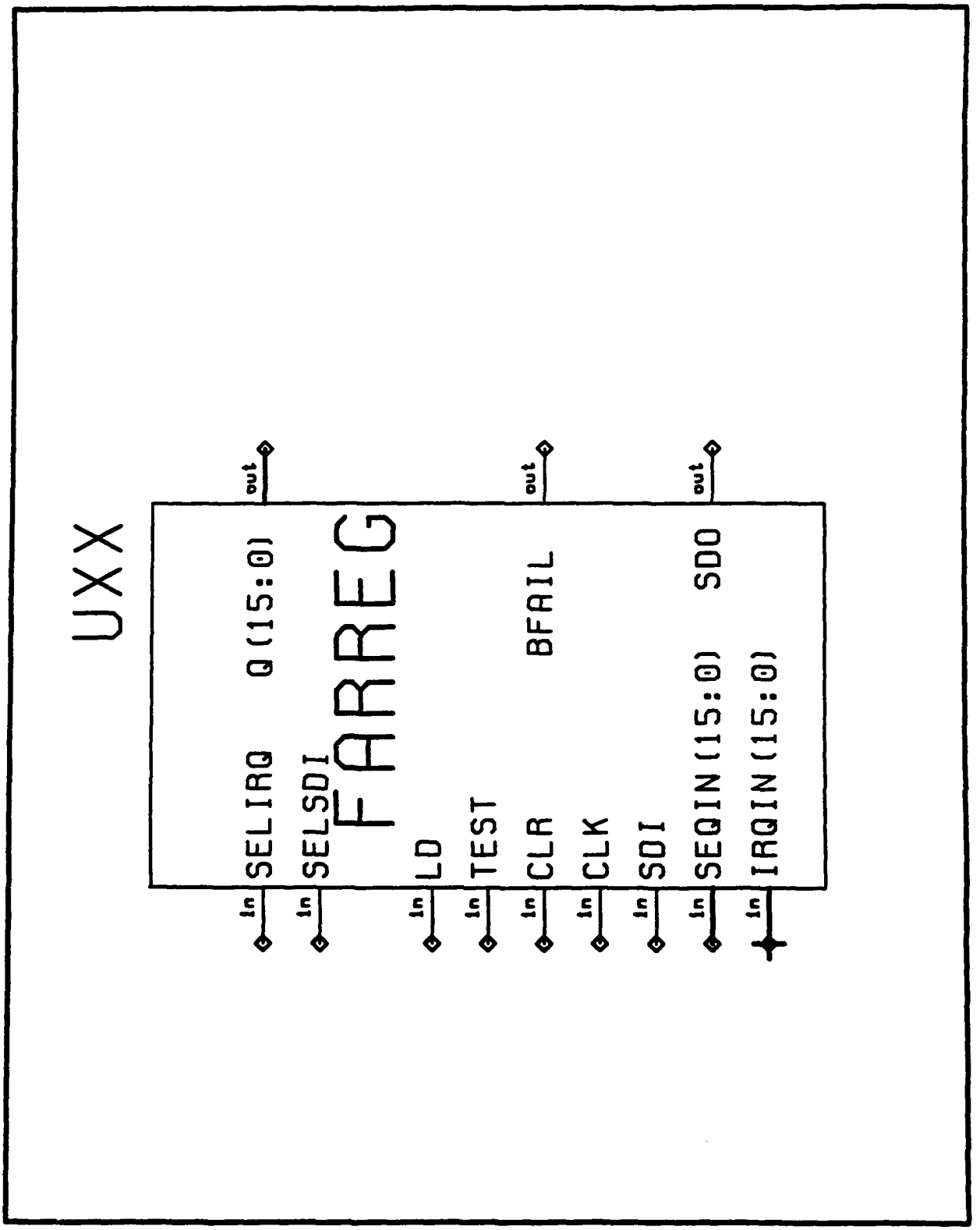

ECLOUT DRIVER
I01
I11
GND
VTT
CG

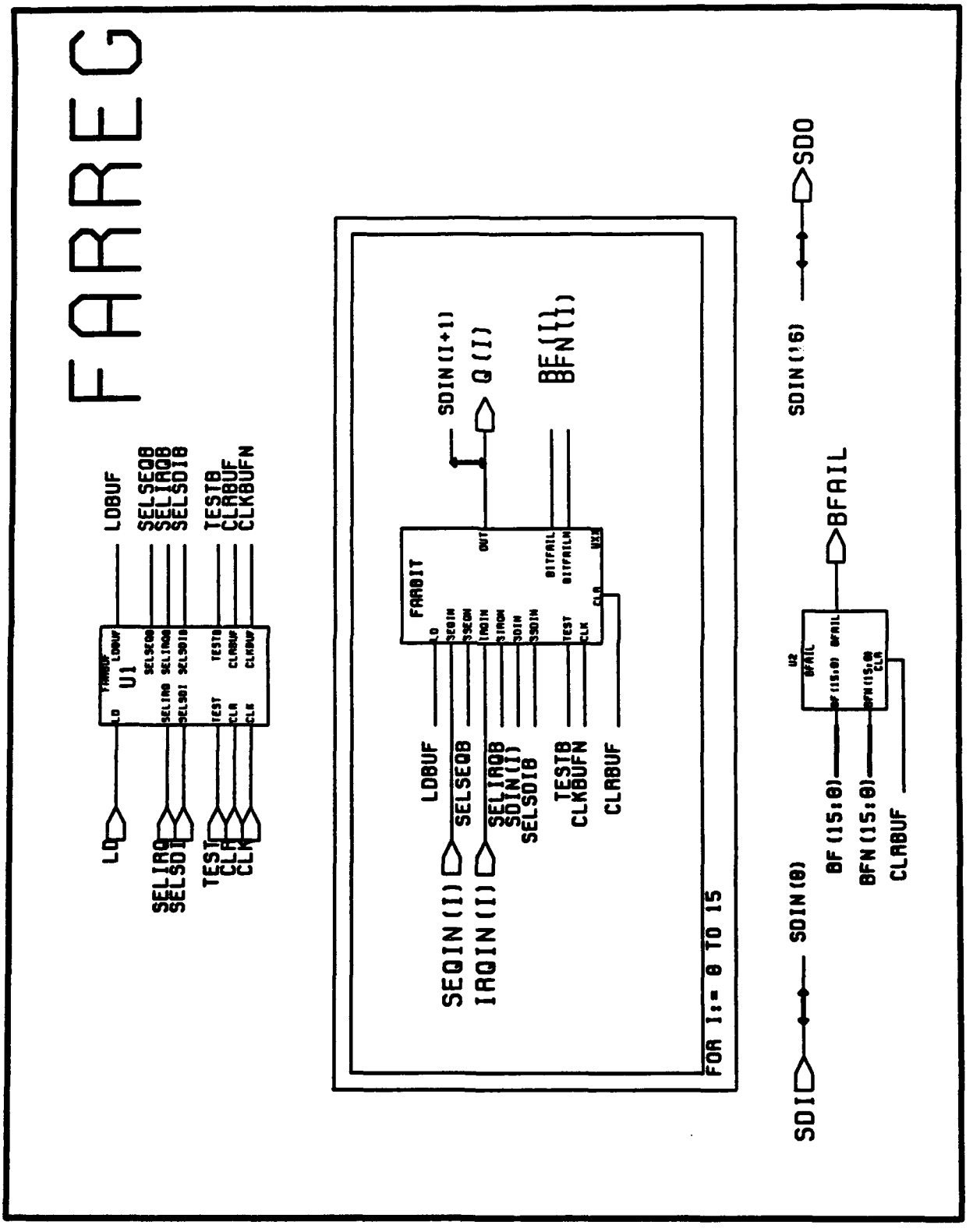

FARBIT
LD
SEQIN
SSEQN
IRQIN
SIRQN
SDIN
SSDIN
TEST
CLK
CLR
OUT
BITFAIL
BITFAILN
UXX
IN
OUT
NI

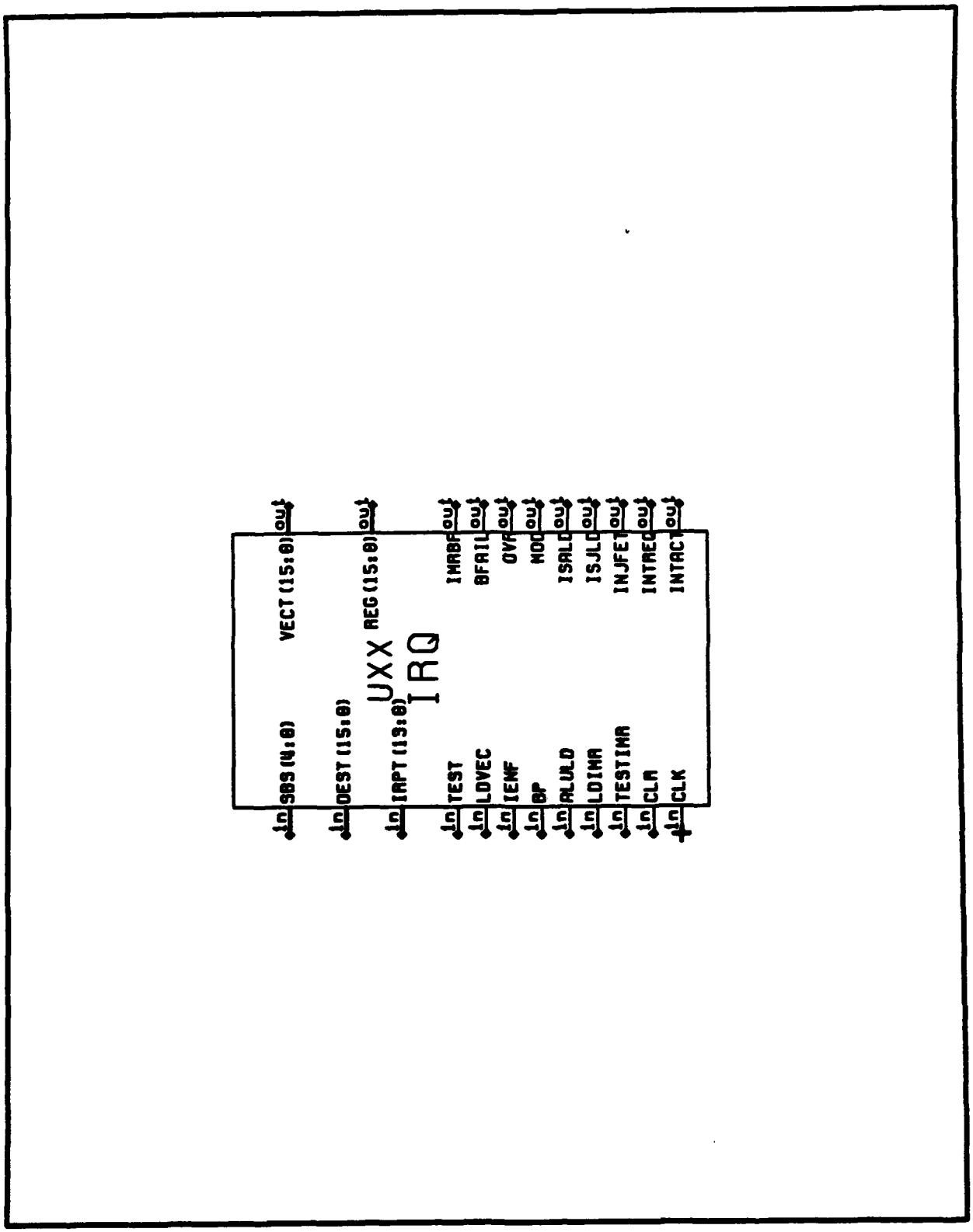

FARBIT

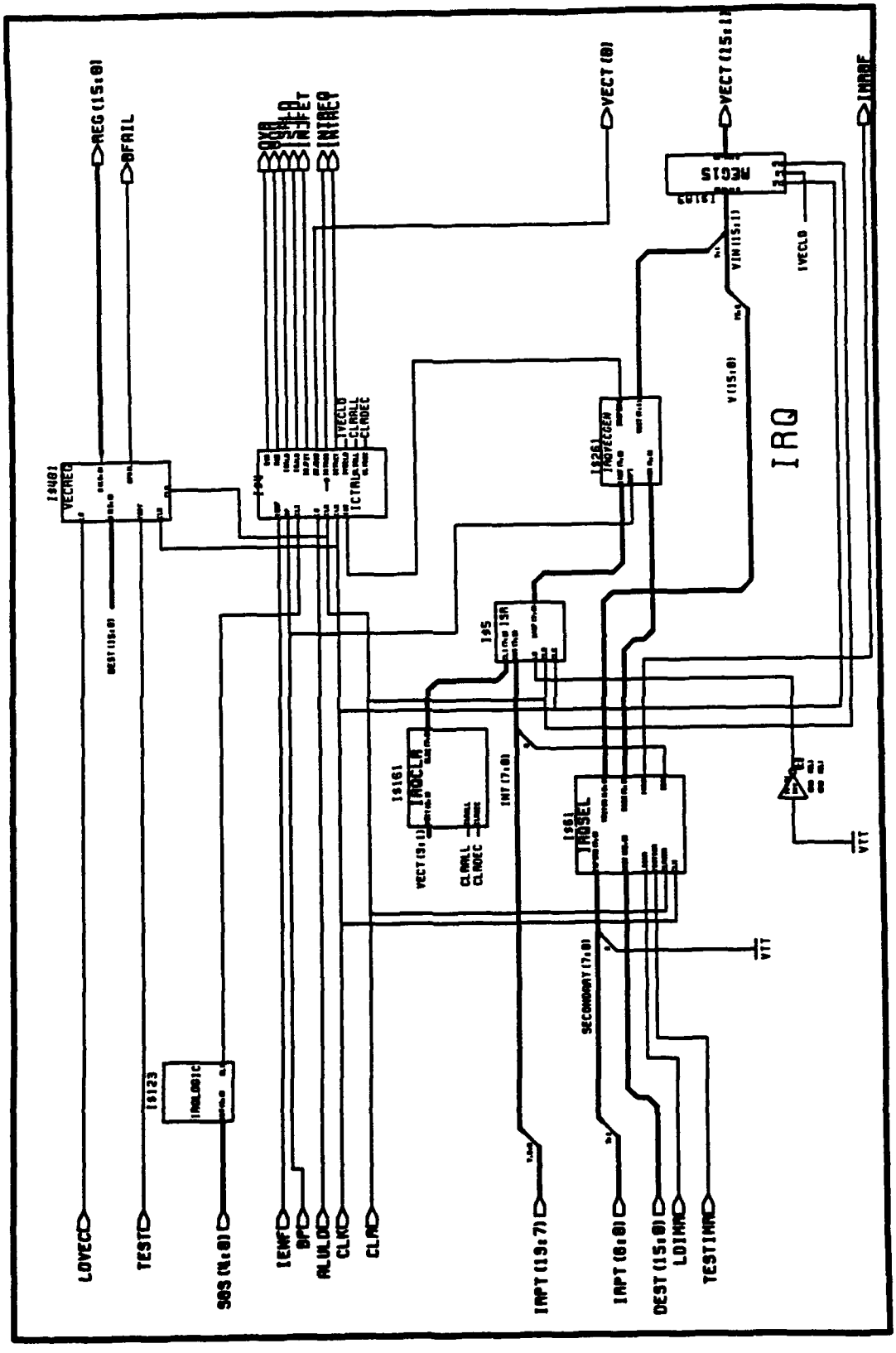

UXX
FARBUF
LDBUF
SELSEQB
SELIRQB
SELSDIB
TESTB
CLRBUF
CLKBUF
LD
SELIRQ
SELSDI
TEST
CLR
CLK
OUT
IN

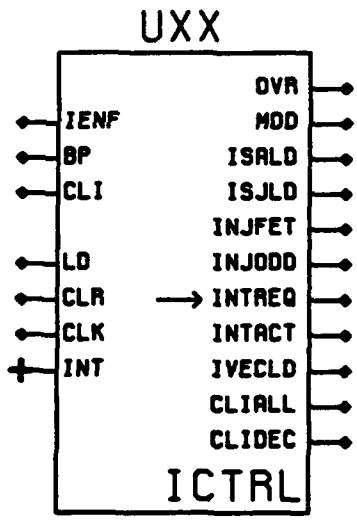

LDBUF
SELIRQB
SELSEQB
SELSDIB
TESTB
CLABUF
CLKBUF
LD
SELIRQ
SELSDI
TEST
CLR
CLK

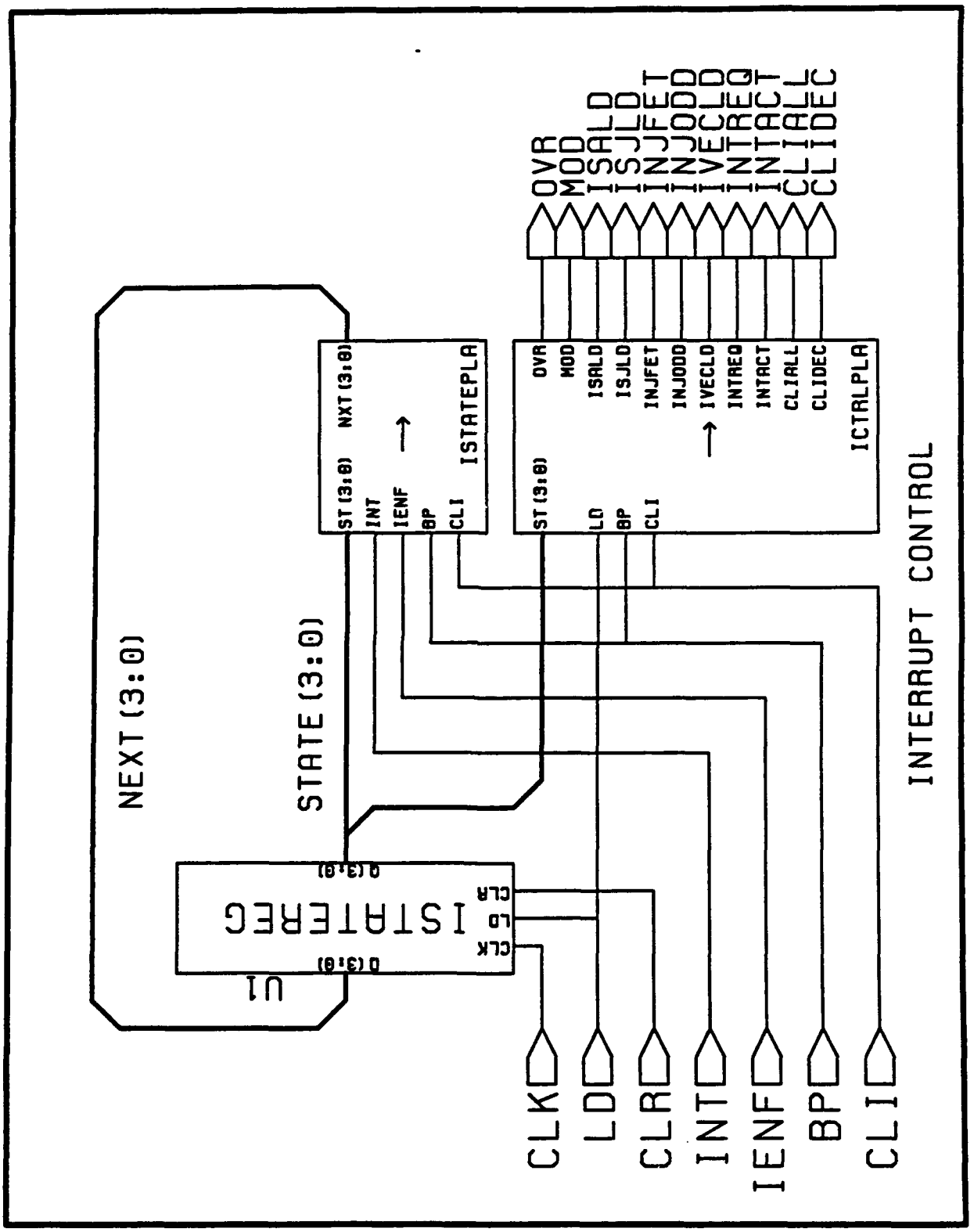

UXX
FARREG
SELIRQ
SELSDI
LD
TEST
CLR
CLK
SDI
SEQIN(15:0)
IRQIN(15:0)
Q(15:0)
BFAIL
SDO
in
out

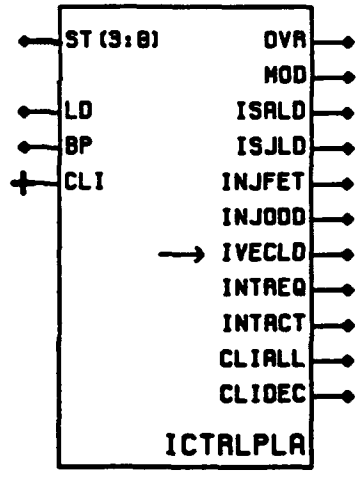

FARREG
LDBUF
SELSE0B
SELIRQB
SELSDI8
TESTB
CLRBUF
CLKBUFN
U1
LD
SELIRQ
SELSDI
TEST
CLR
CLK
SDIN(I+1)
Q(I)
BFN(I)
FARBIT
OUT
BITFAIL
BITFAILN
SEQIN
IRQIN
SDIN
TEST
CLK
SEQIN(I)
IRQIN(I)
SDIN(I)
CLKBUFN
FOR I:= 0 TO 15
SDO
SDIN(16)
BFAIL
U2
BFAIL
BF(15:0)
BFN(15:0)
SDI
SDIN(0)
CLRBUF

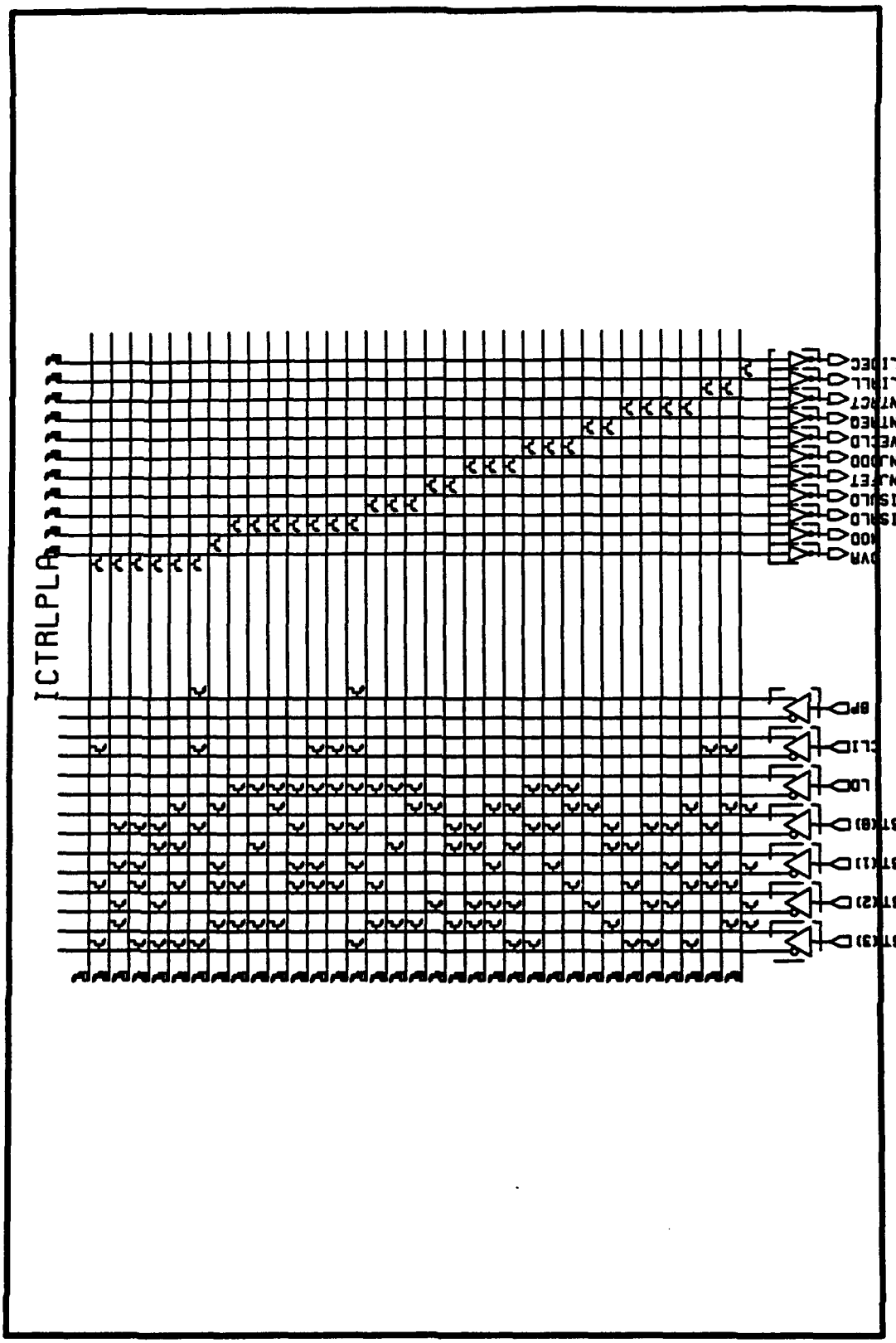

UXX
IRQ
SBS(N:0)
DEST(15:0)
IRPT(13:0)
TEST
LOVEC
IENF
BP
ALULD
LDIMA
TESTIMA
CLR
CLK
VECT(15:0)
REG(15:0)
IMABF
BFAIL
OVR
NOD
ISALD
ISJLD
INJFET
INTREQ
INTACT

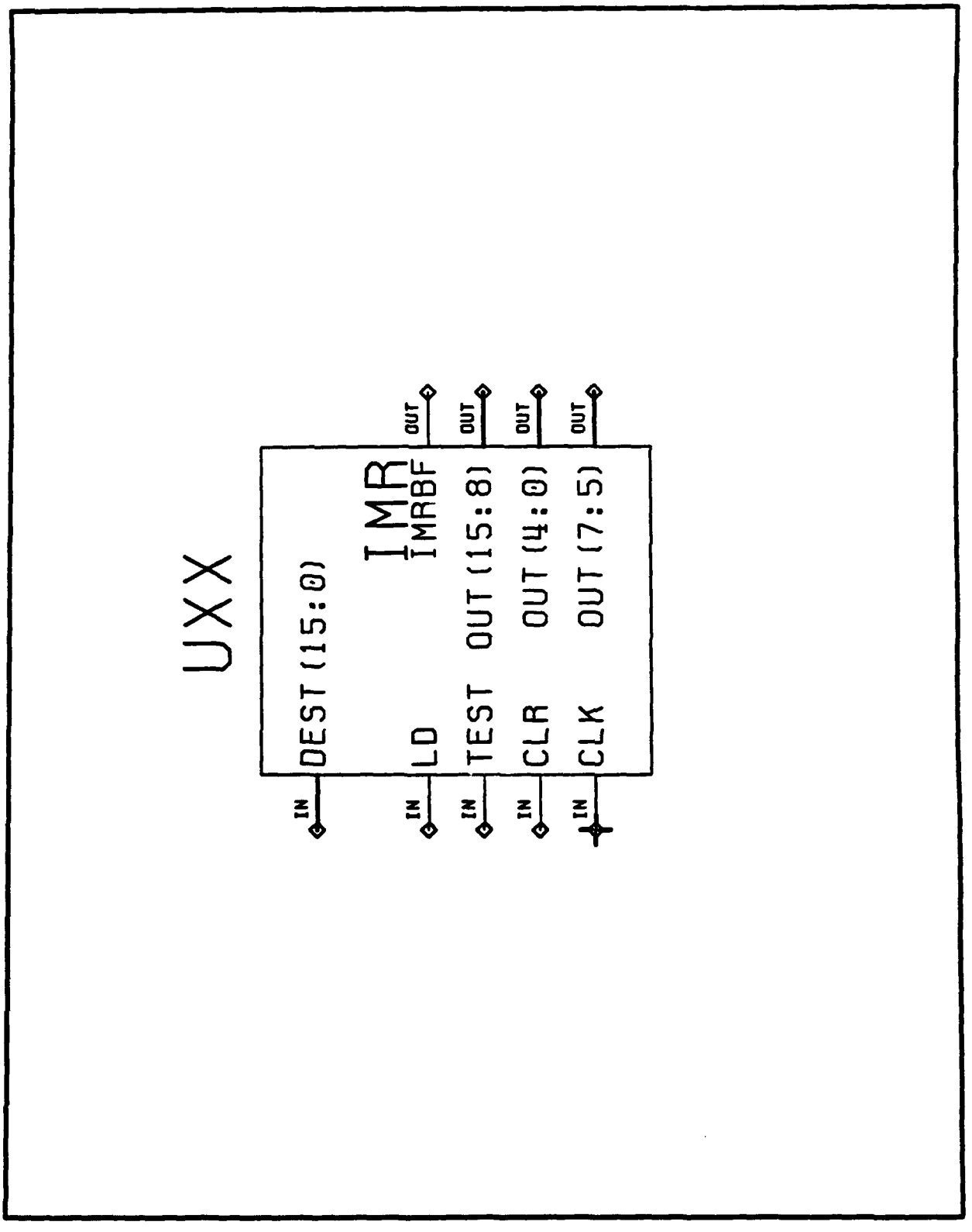

REG(15:0)
BFAIL
VECT(0)
VECT(15:1)
INBUF
IRQ
LOVEC
TEST
SOS(1:0)
IENF
DPC
ALULOC
CLK
CLR
INPT(15:7)
INPT(6:0)
DEST(15:0)
LDIMM
TESTIMM

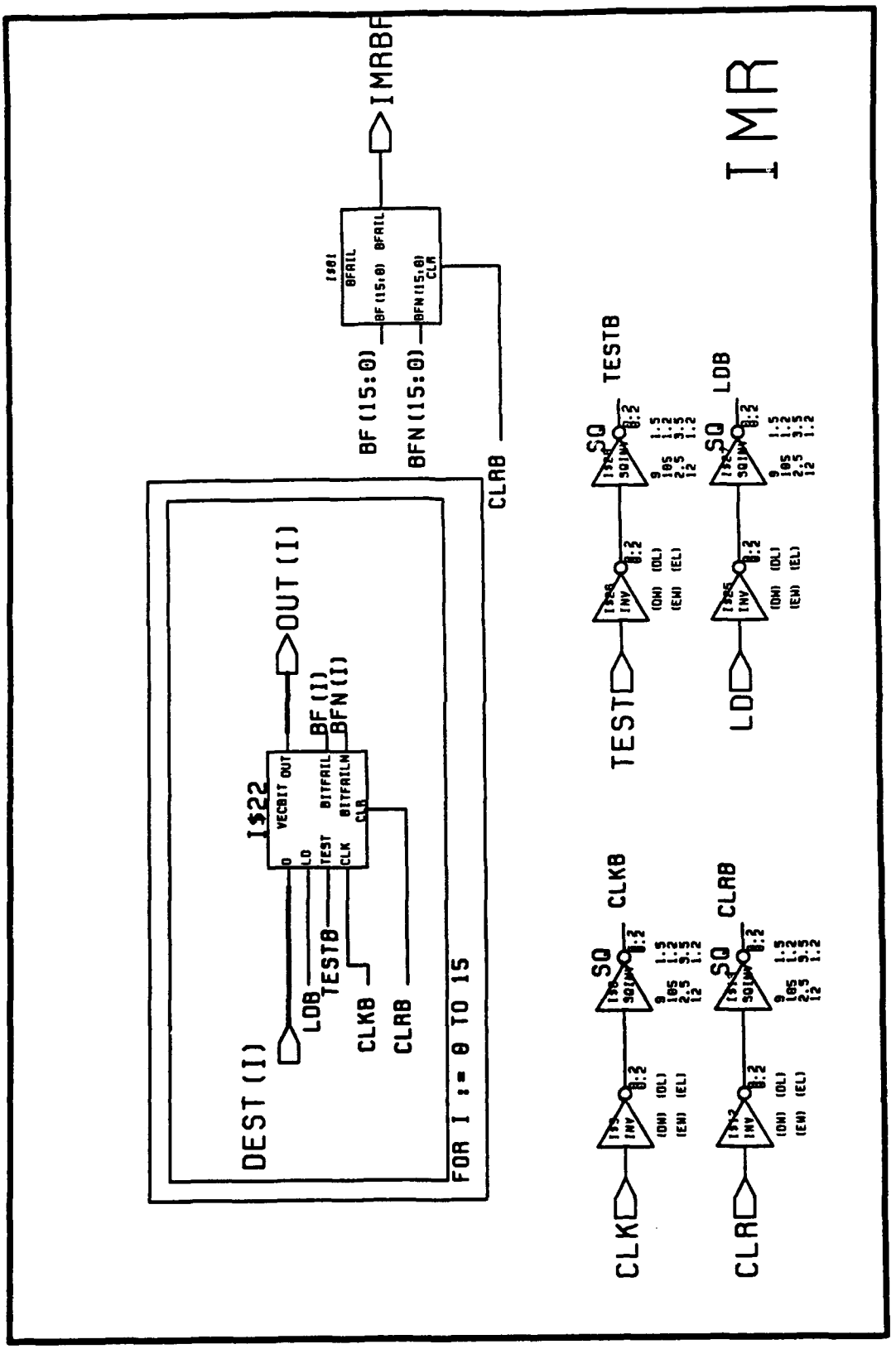

UXX
IENF
BP
CLI
LD
CLR
CLK
INT
OVR
MOD
ISRLD
ISJLD
INJFET
INJODD
INTREQ
INTACT
IVECLD
CLIALL
CLIDEC
ICTRL

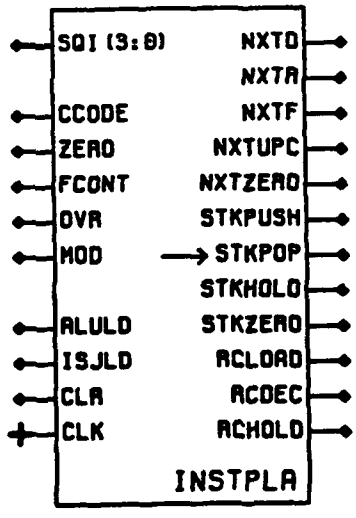

OVR
MOD
ISALD
ISJLD
INJFET
INJODD
IVECLD
INTREQ
INTACT
CLIALL
CLIDEC
NXT(3:0)
ISTATEPLA
ST(3:0)
INT
IENF
BP
CLI
ICTRLPLA
LD
NEXT(3:0)
STATE(3:0)
INTERRUPT CONTROL
ISTATEREG
D(3:0)
Q(3:0)
CLR
CLK
U1
CLK
LD
CLR
INT
IENF
BP
CLI

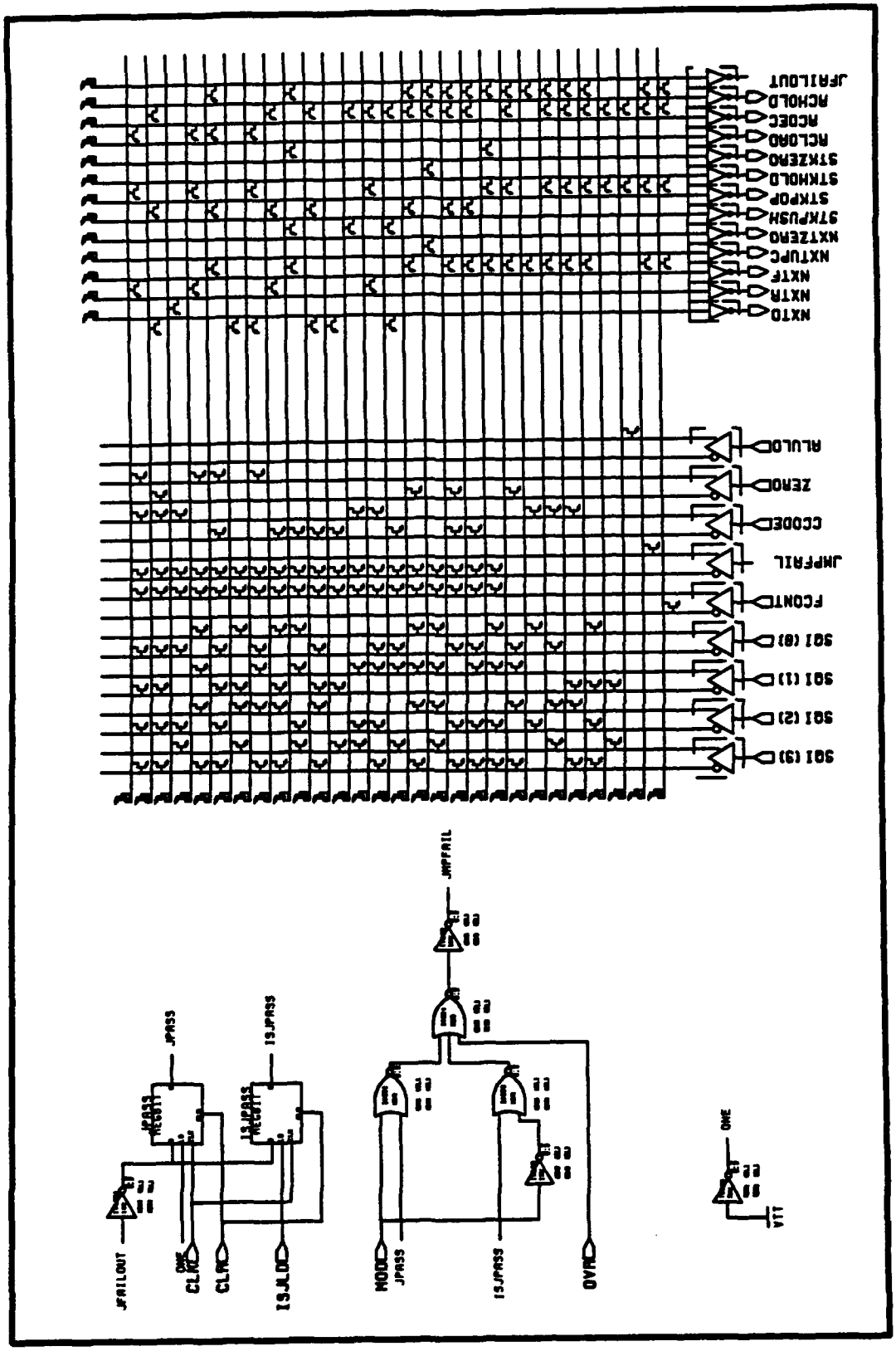

ST (3:0)
LD
BP
CLI
OVR
MOD
ISALD
ISJLD
INJFET
INJODD
IVECLD
INTREQ
INTACT
CLIALL
CLIDEC
ICTRLPLA

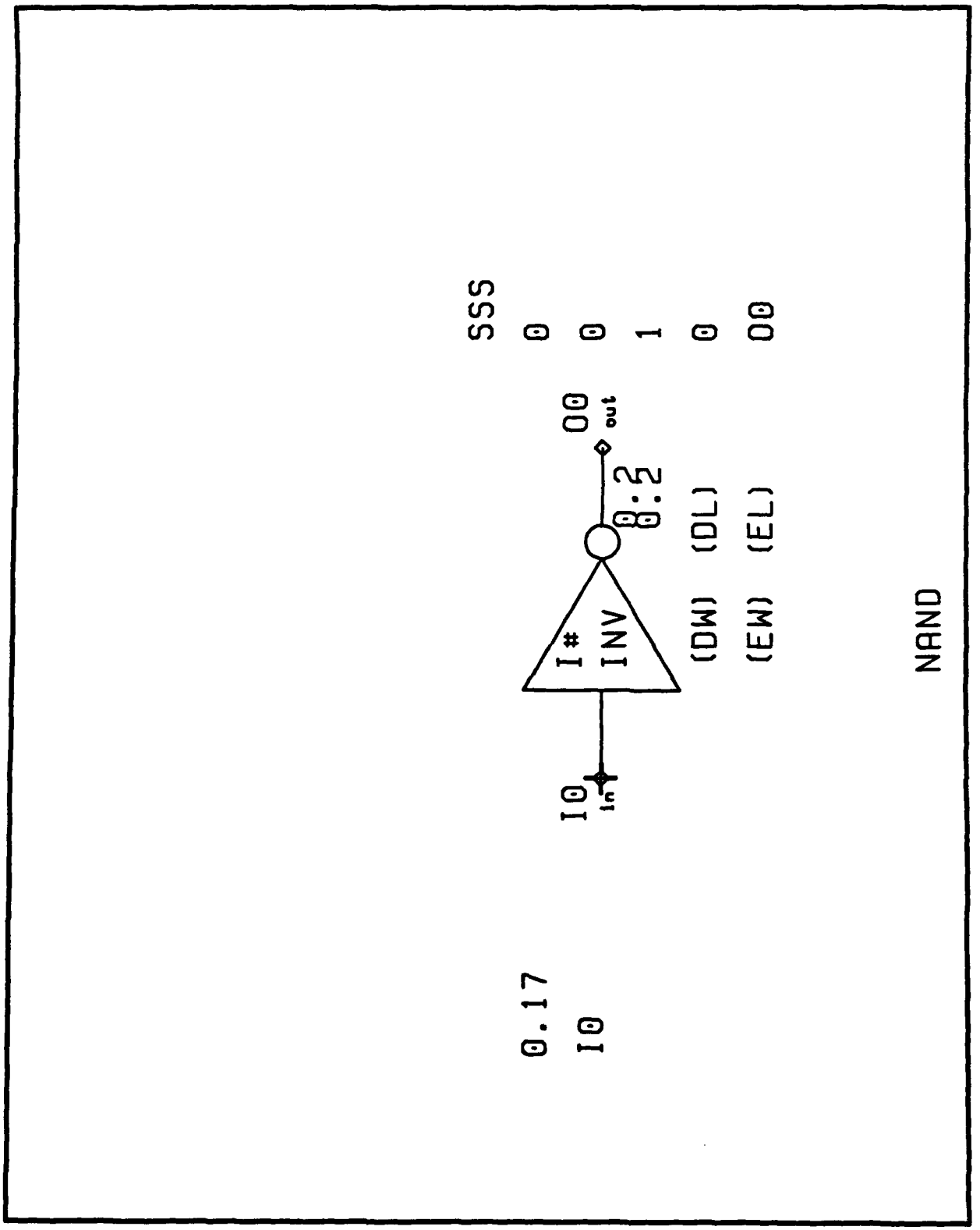

CTRLPLA
BP
CLI
LO
ST(0)
ST(1)
ST(2)
ST(3)

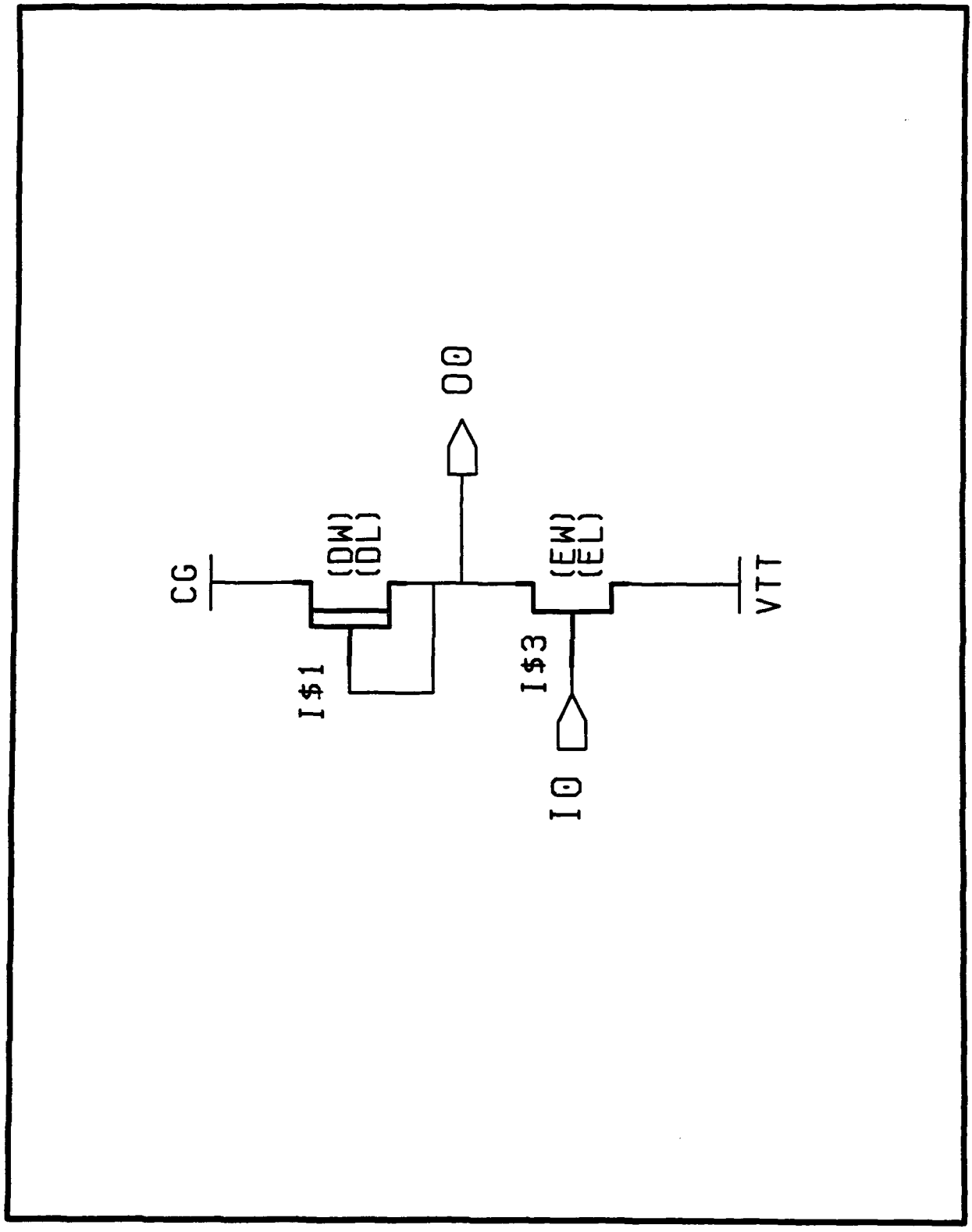

UXX
IMR
IMRBF
DEST (15:0)
LD
TEST
CLR
CLK
OUT (15:8)
OUT (4:0)
OUT (7:5)
IN
IN
IN
IN
IN
OUT
OUT
OUT
OUT

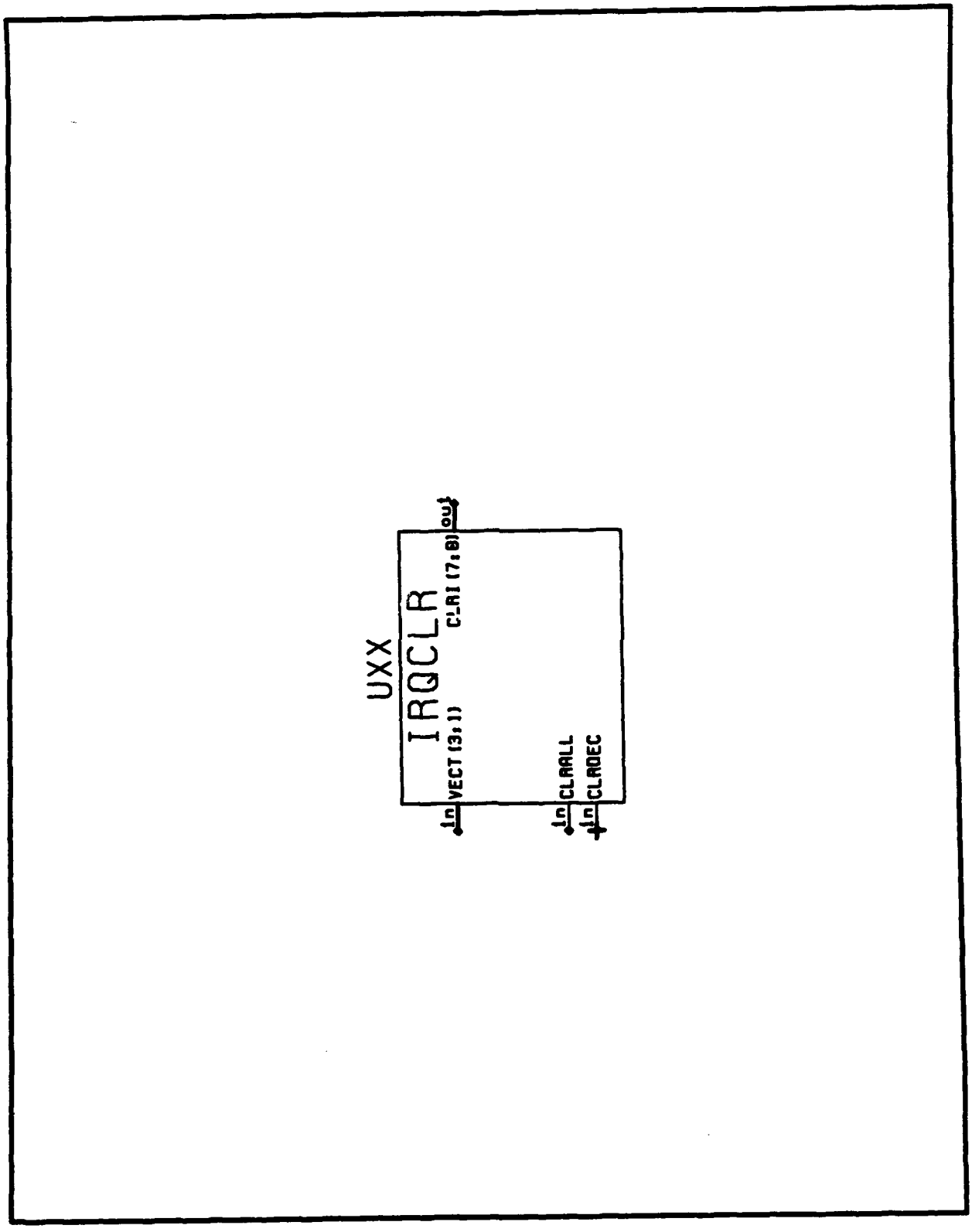

IMR
IMRBF
BF (15:0)
BFN (15:0)
CLRB
FOR I := 0 TO 15
DEST (I)
OUT (I)
BF (I)
BFN (I)
I$22
VECBIT OUT
D
LD
TEST
CLK
BITFAIL
BITFAILN
CLR
LDB
TESTB
CLKB
CLRB
TEST
LD
CLK
CLR
SQ
INV

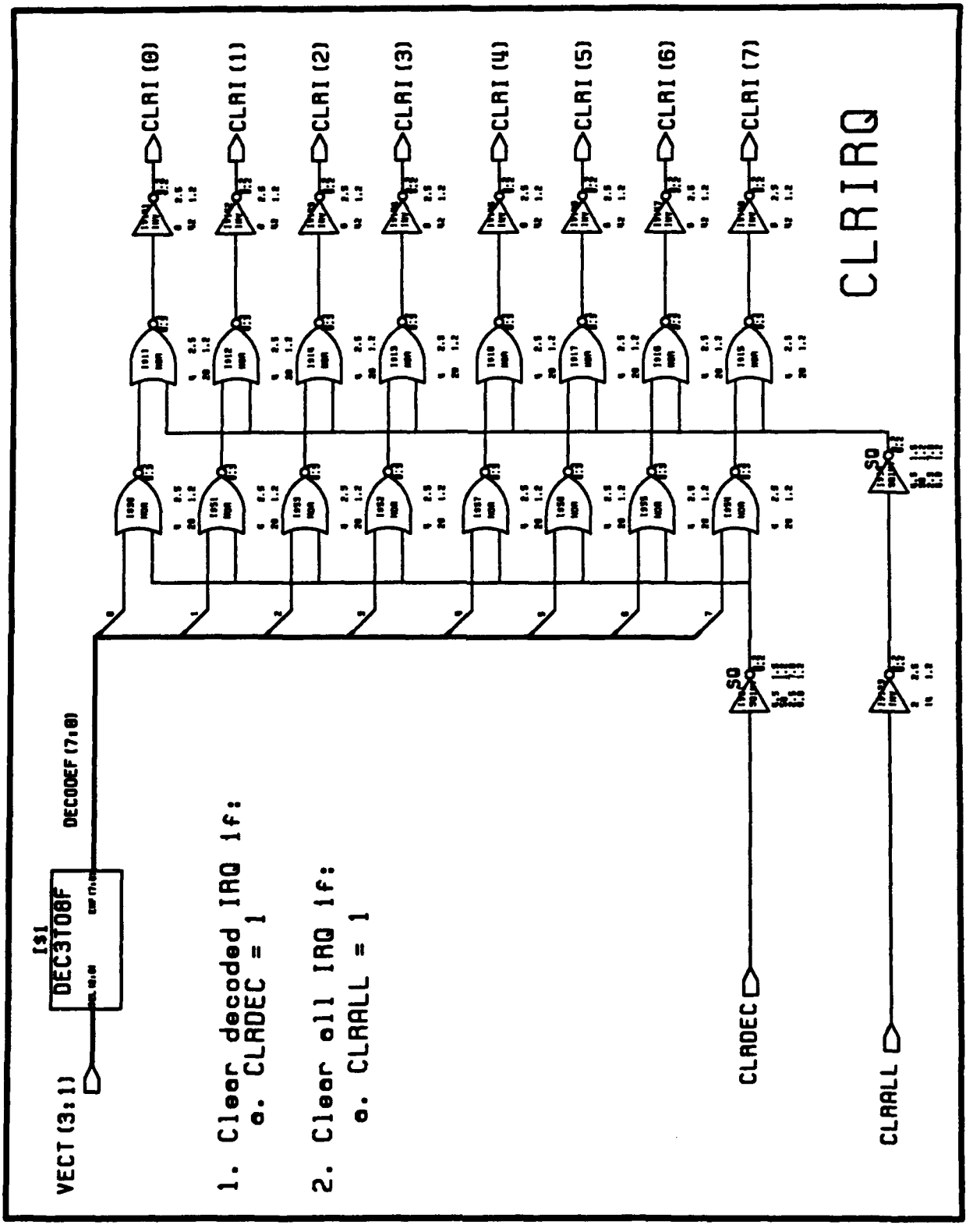

SQI (3:0)
CCODE
ZERO
FCONT
OVR
MOD
ALULD
ISJLD
CLR
CLK
NXTD
NXTR
NXTF
NXTUPC
NXTZERO
STKPUSH
STKPOP
STKHOLD
STKZERO
RCLOAD
RCDEC
RCHOLD
INSTPLA

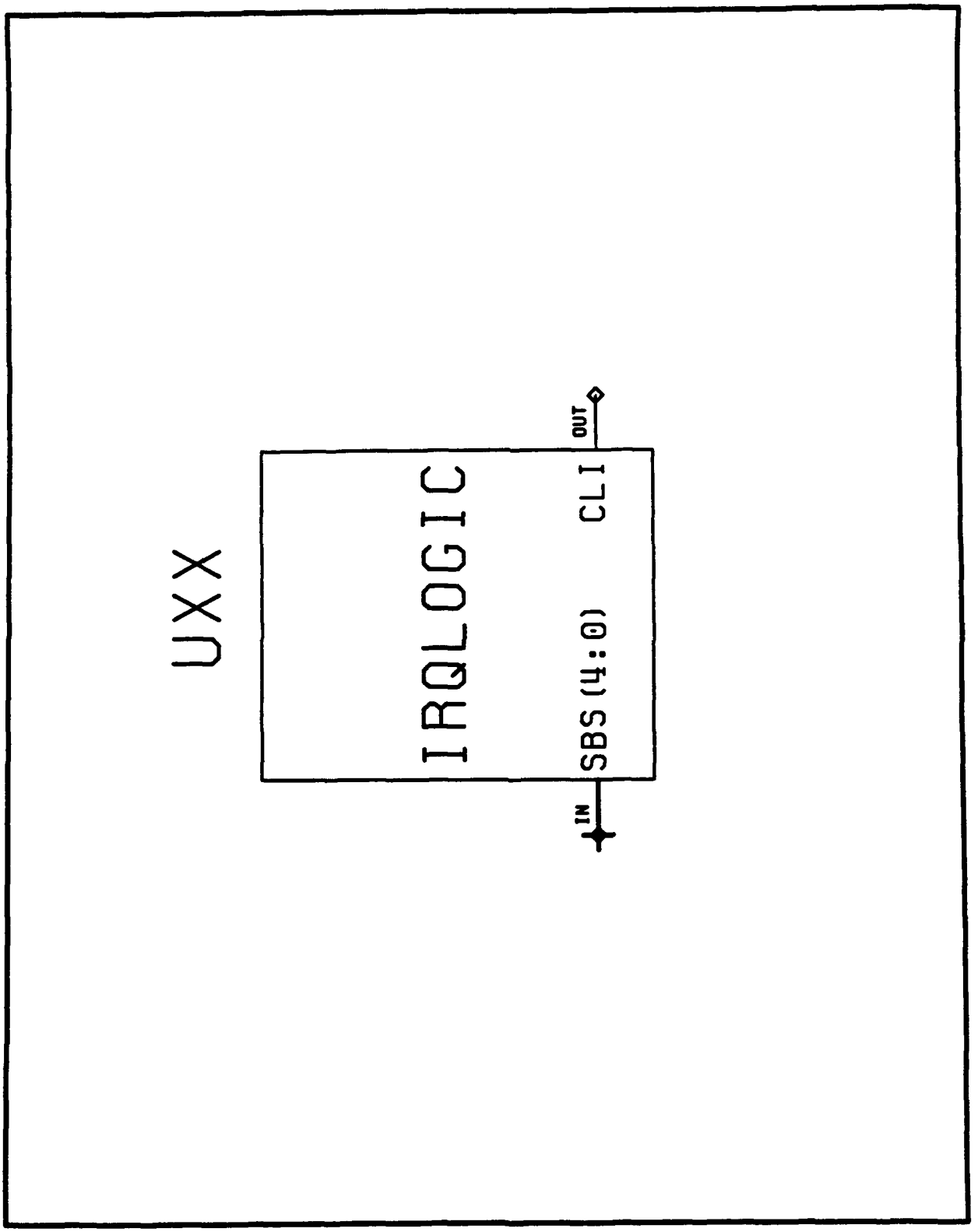

JFAILOUT
RCHOLD
RCOEC
RCLOAD
STKZERO
STKHOLD
STKPOP
STKPUSH
NXTZERO
NXTUPC
NXTF
NXTR
NXTO
RLULO
ZERO
CCODE
JMPFAIL
FCONT
SQI (0)
SQI (1)
SQI (2)
SQI (3)
JMPFAIL
JPASS
IGJPASS
JFAILOUT
ONE
CLRC
CLRC
IGJLOC
MODE
JPASS
IGJPASS
OVRO
ONE
VCC

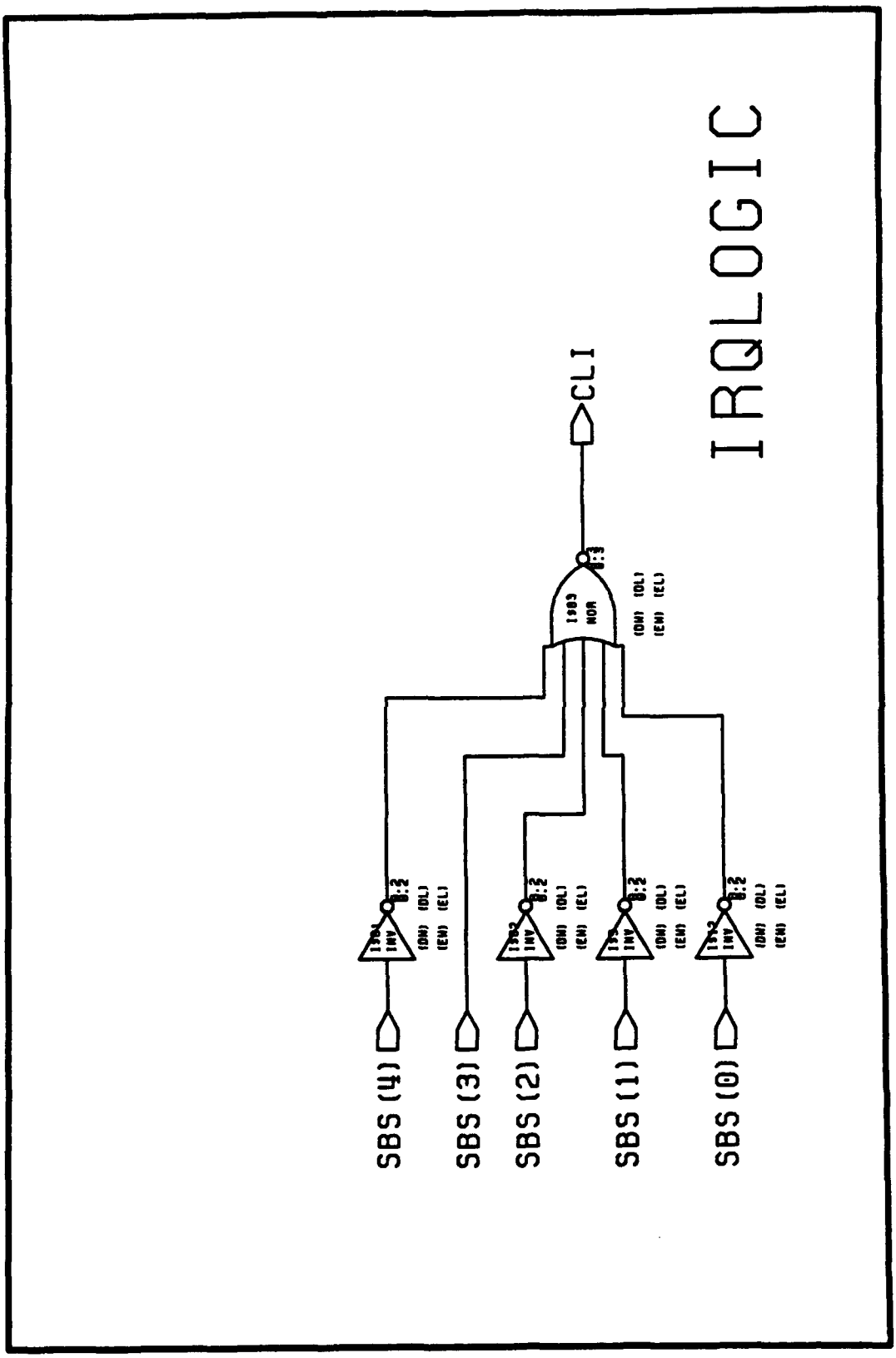

SSS
0 0 1 0 00
00
out
8.2
I#
INV
(DW) (DL)
(EW) (EL)
NAND
IO
in
0.17
IO

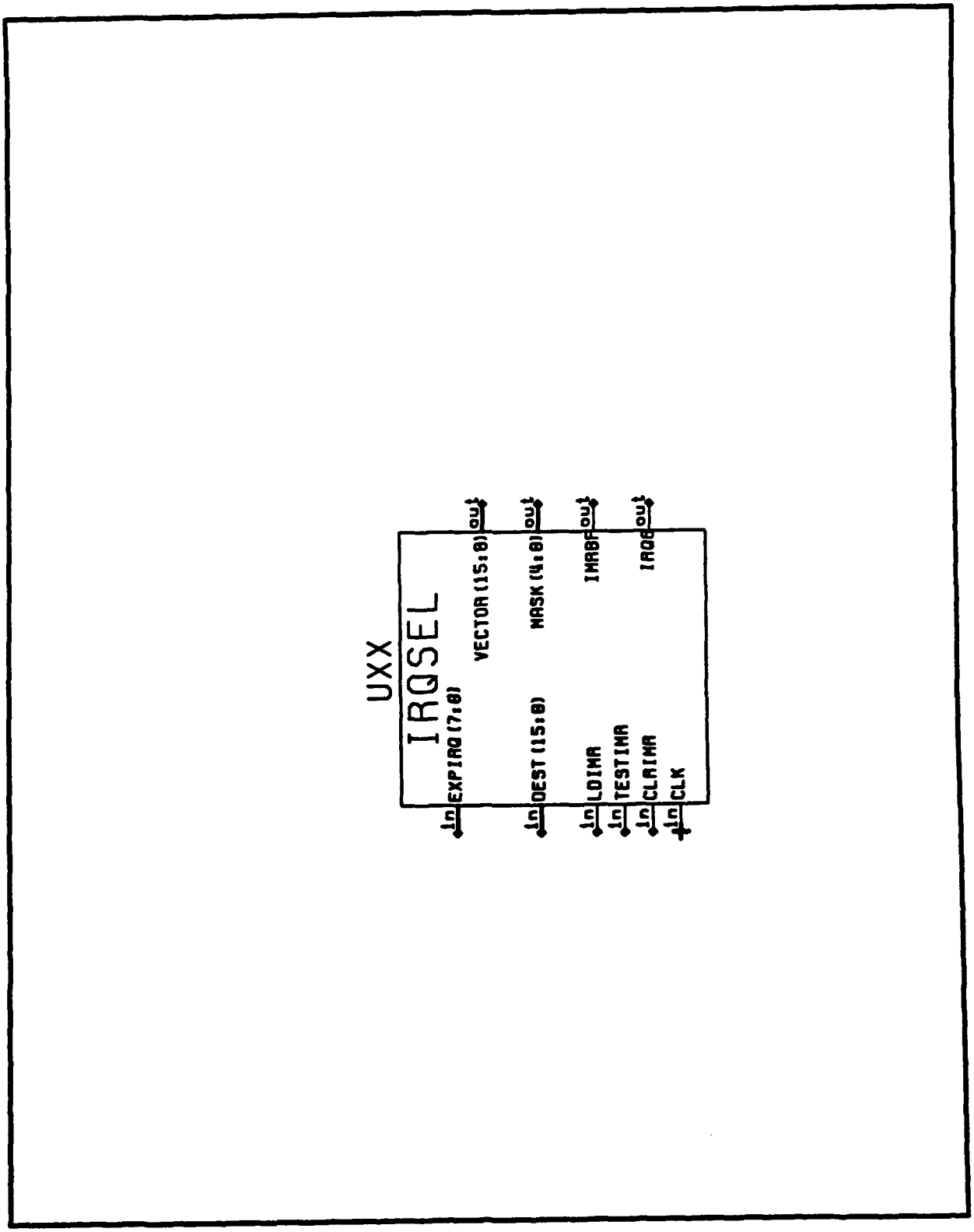

O0
CG
(DW)
(DL)
(EW)
(EL)
VTT
I$1
I$3
I0

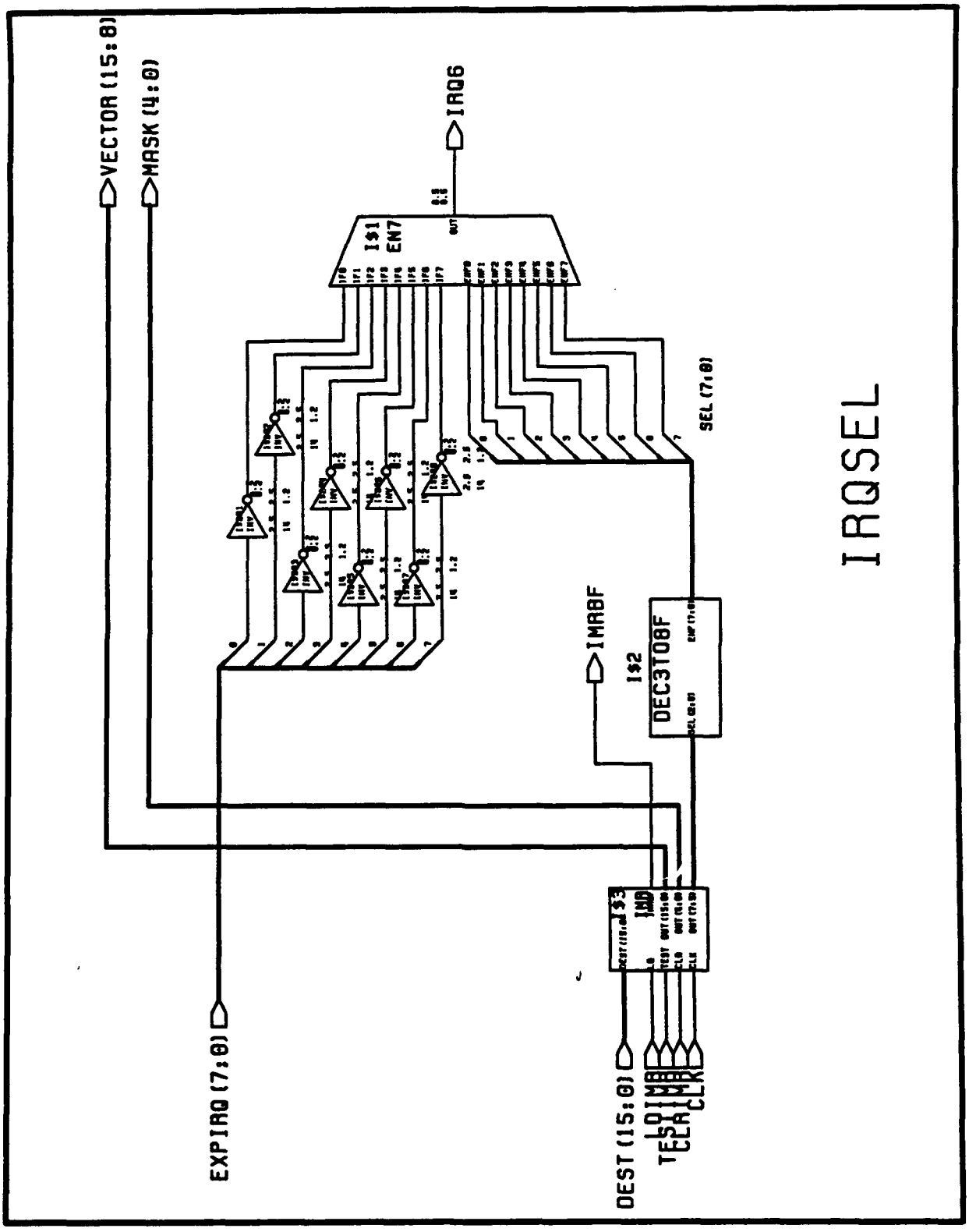

UXX
IRQCLR
CLRI (7,0)
out
VECT (3,1)
in
CLRALL
in
CLRDEC
in

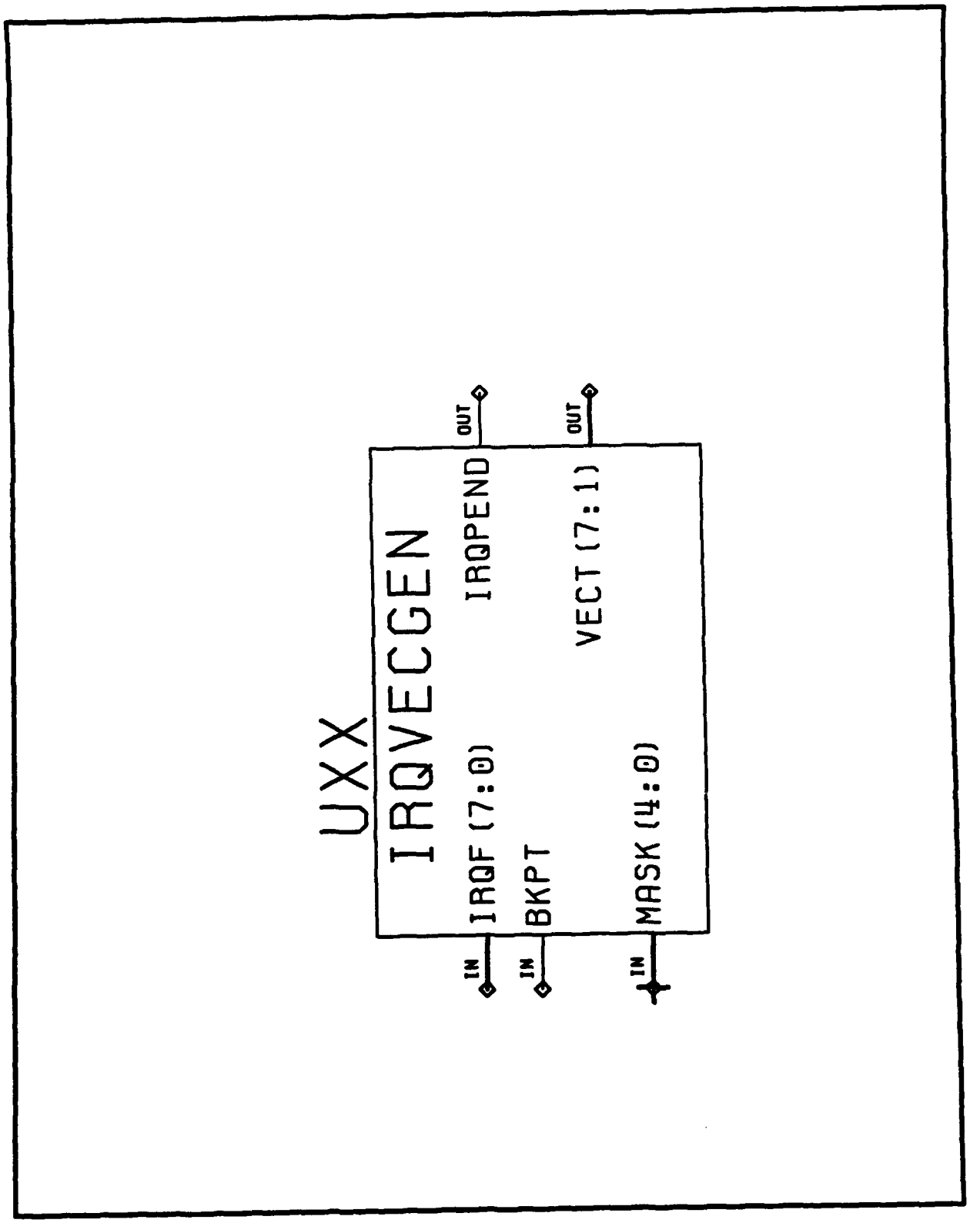

CLRIRQ
CLRI (0)
CLRI (1)
CLRI (2)
CLRI (3)
CLRI (4)
CLRI (5)
CLRI (6)
CLRI (7)
SO
SO
I$1
DEC3TO8F
DECODEF (7:0)
VECT (3:1)
1. Clear decoded IRQ if:
a. CLRDEC = 1
2. Clear all IRQ if:
a. CLRALL = 1
CLRDEC
CLRALL

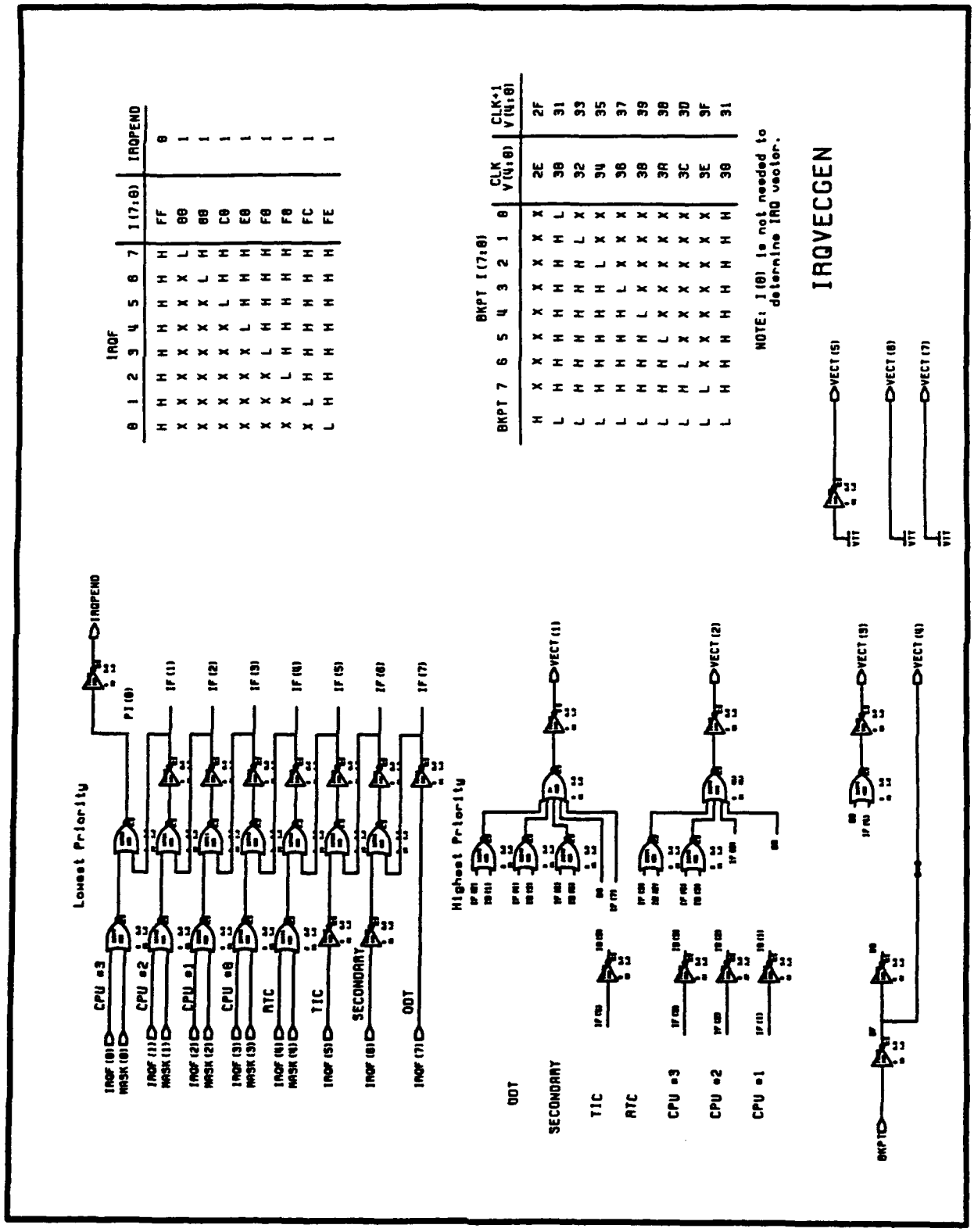

UXX
IRQLOGIC
OUT
CLI
SBS(4:0)
IN

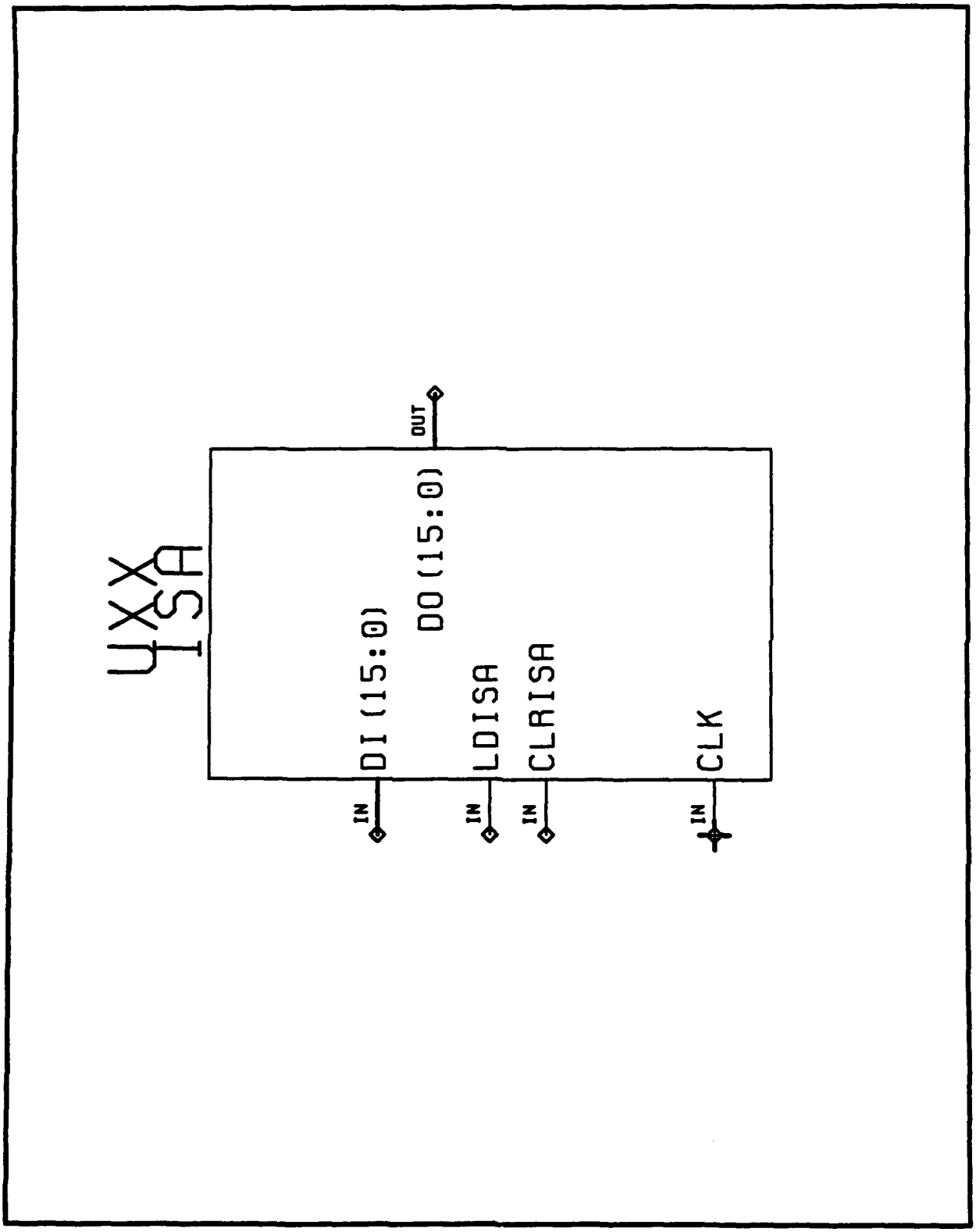

IRQLOGIC
CLI
SBS (4)
SBS (3)
SBS (2)
SBS (1)
SBS (0)

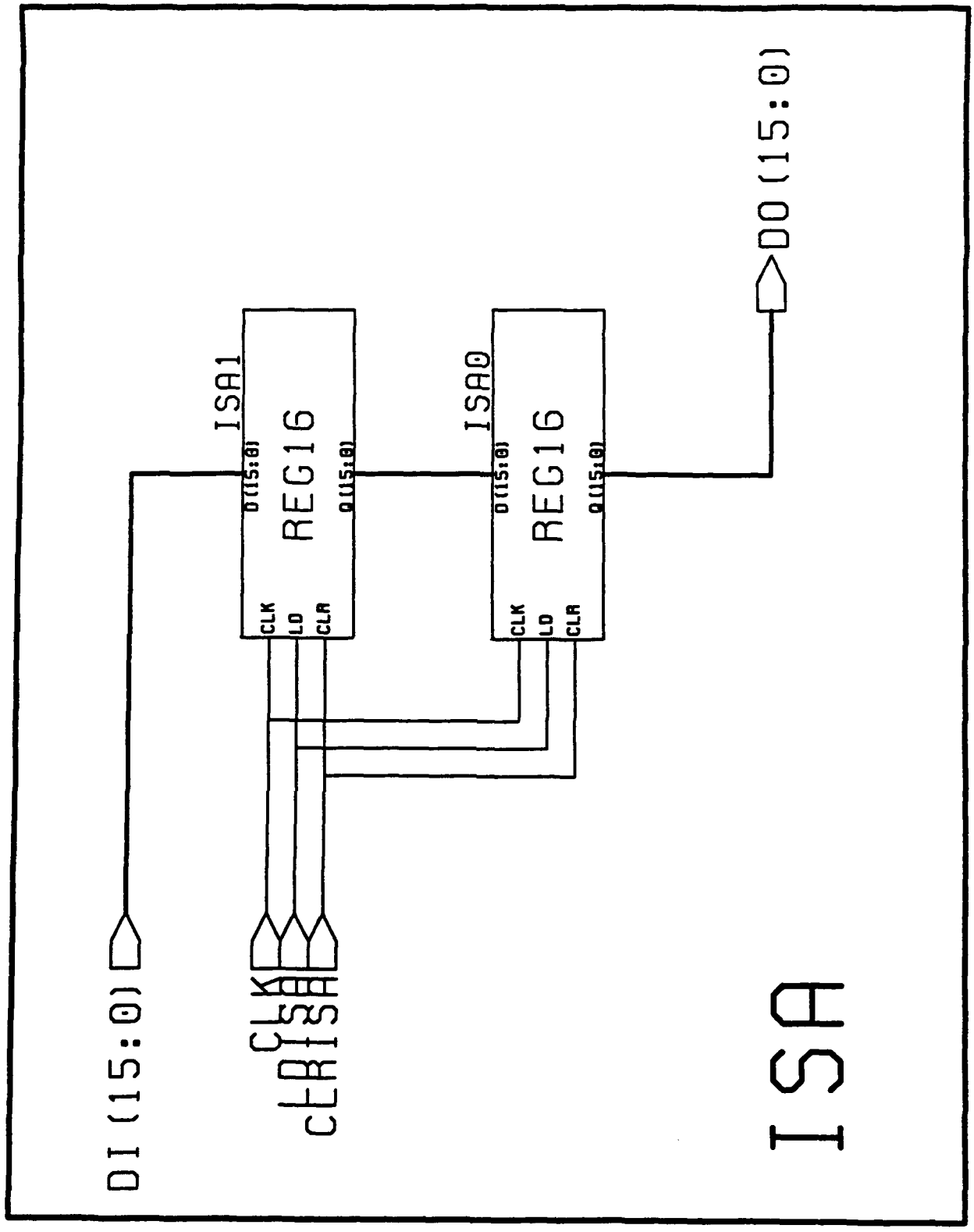

UXX
IRQSEL
EXPIRQ (7:0)
DEST (15:0)
LDIMR
TESTIMR
CLRIMR
CLK
VECTOR (15:0)
MASK (4:0)
IMRBF
IRQB

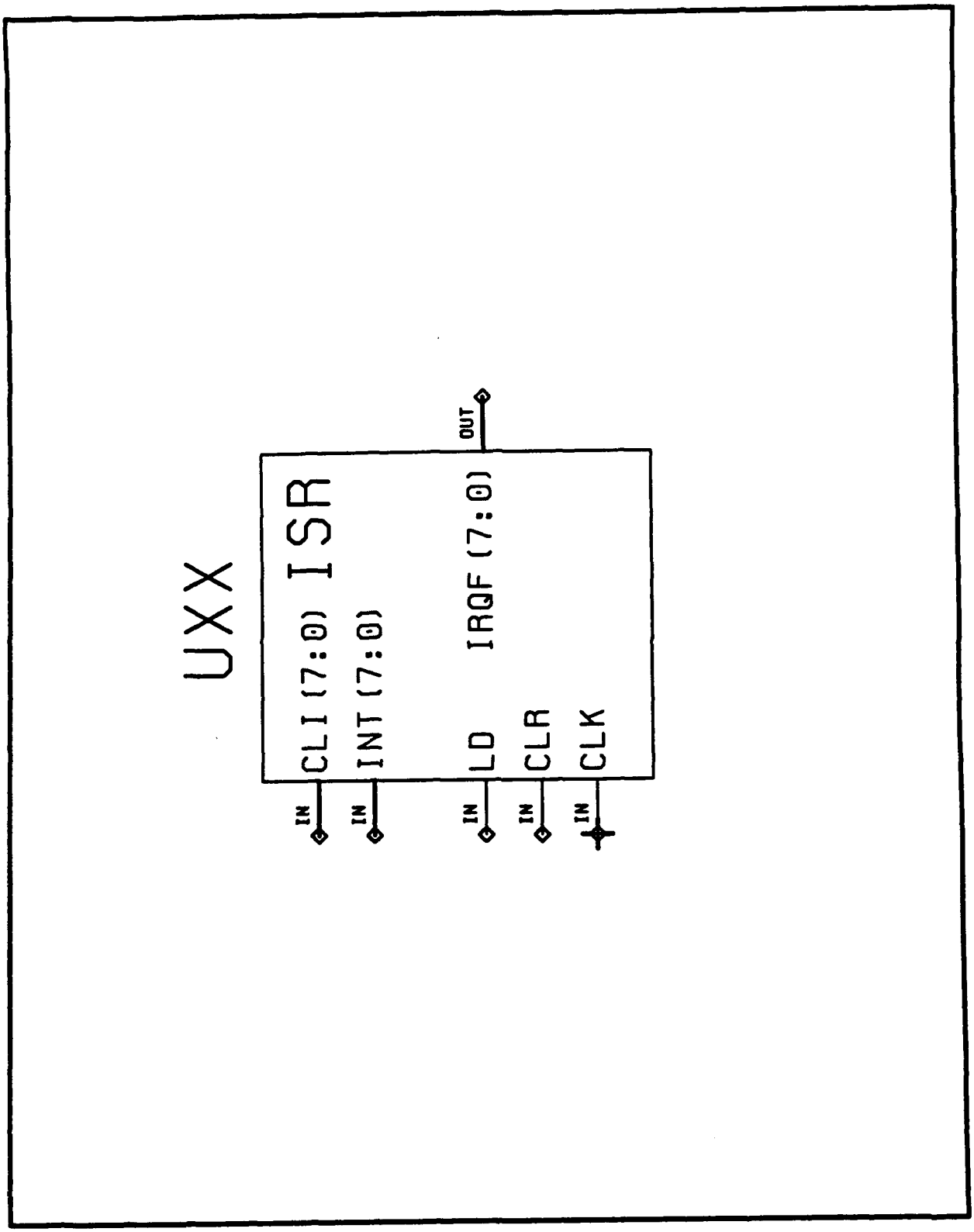

IRQSEL
VECTOR(15:8)
MASK(4:0)
IRQ6
I$1
EN7
SEL(7:0)
IMA8F
I$2
DEC3TO8F
EXPIRQ(7:0)
DEST(15:0)
TEST
CLR

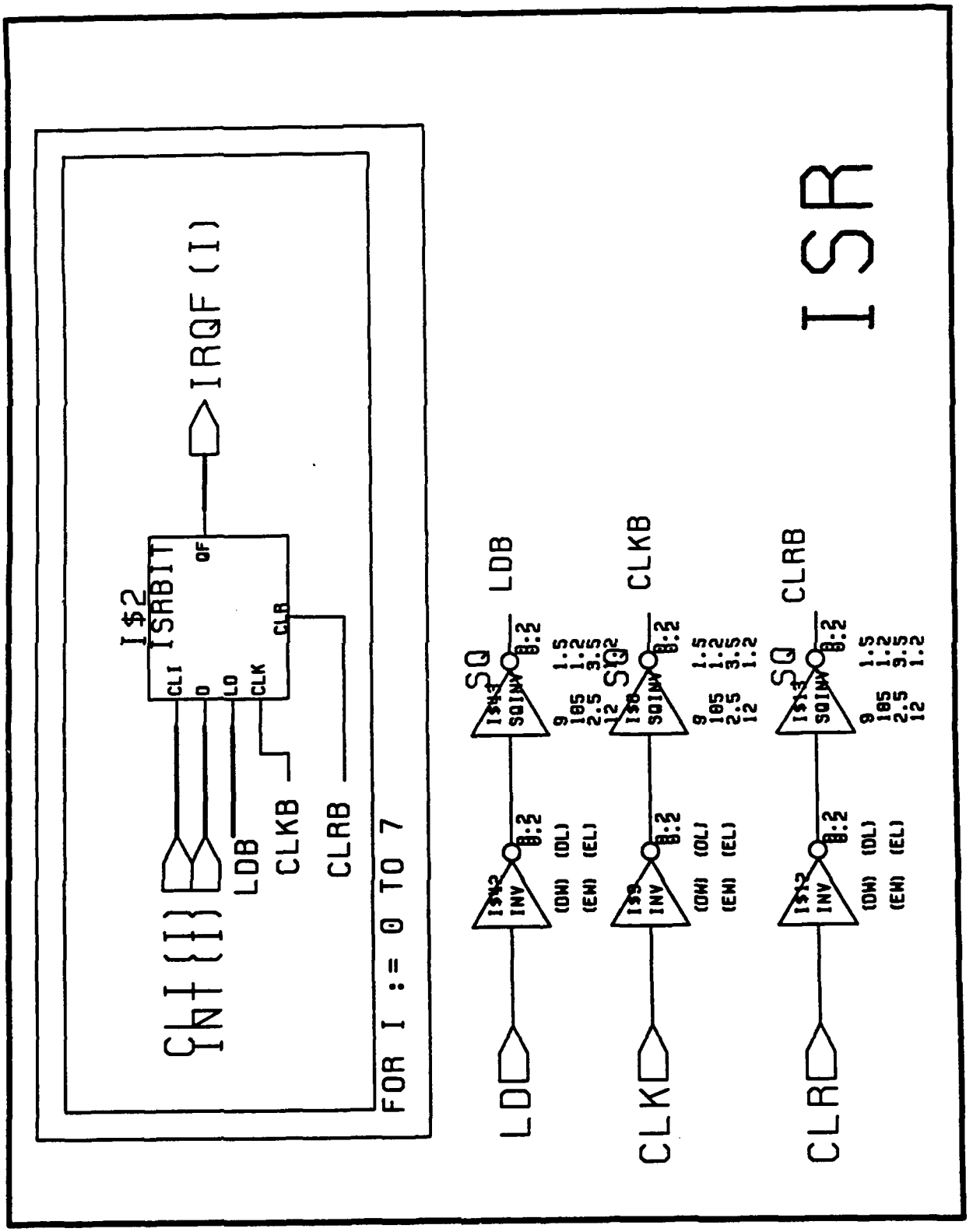

UXX
IRQVECGEN
IRQF (7:0)
BKPT
MASK (4:0)
IRQPEND
VECT (7:1)
IN
IN
IN
OUT
OUT

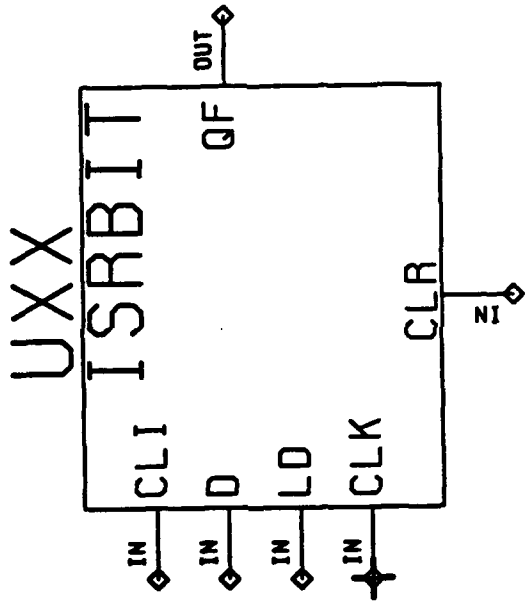

IRQVECGEN
IRQPEND
IRQF
I(7:0)
BKPT I(7:0)
CLK V(4:0)
CLK+1 V(4:0)
NOTE: I(0) is not needed to determine IRQ vector.
Lowest Priority
Highest Priority
CPU #3
CPU #2
CPU #1
CPU #0
ATC
TIC
SECONDARY
ODT
VECT(5)
VECT(6)
VECT(7)
BKPT

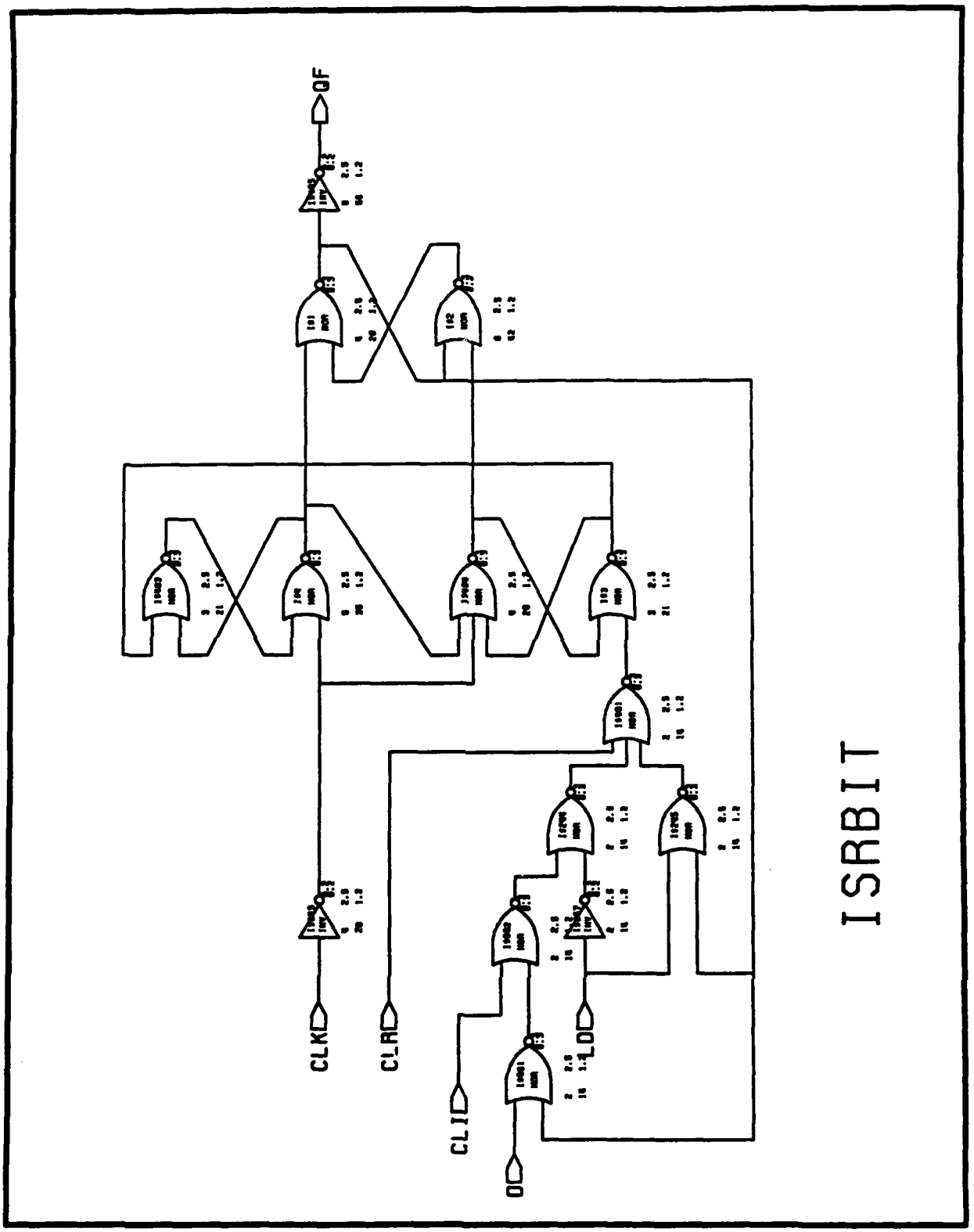

U4XX
1SA
OUT
DO(15:0)
DI(15:0)
LDISA
CLRISA
CLK
IN
IN
IN
IN

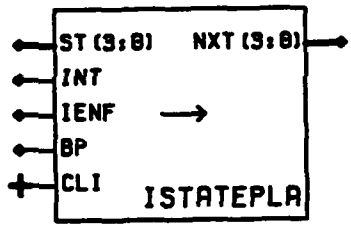

ISA
DI(15:0)
CLRISA
CLKISA
ISA1
ISA0
REG16
REG16
D(15:0)
Q(15:0)
CLK
LD
CLR
DO(15:0)

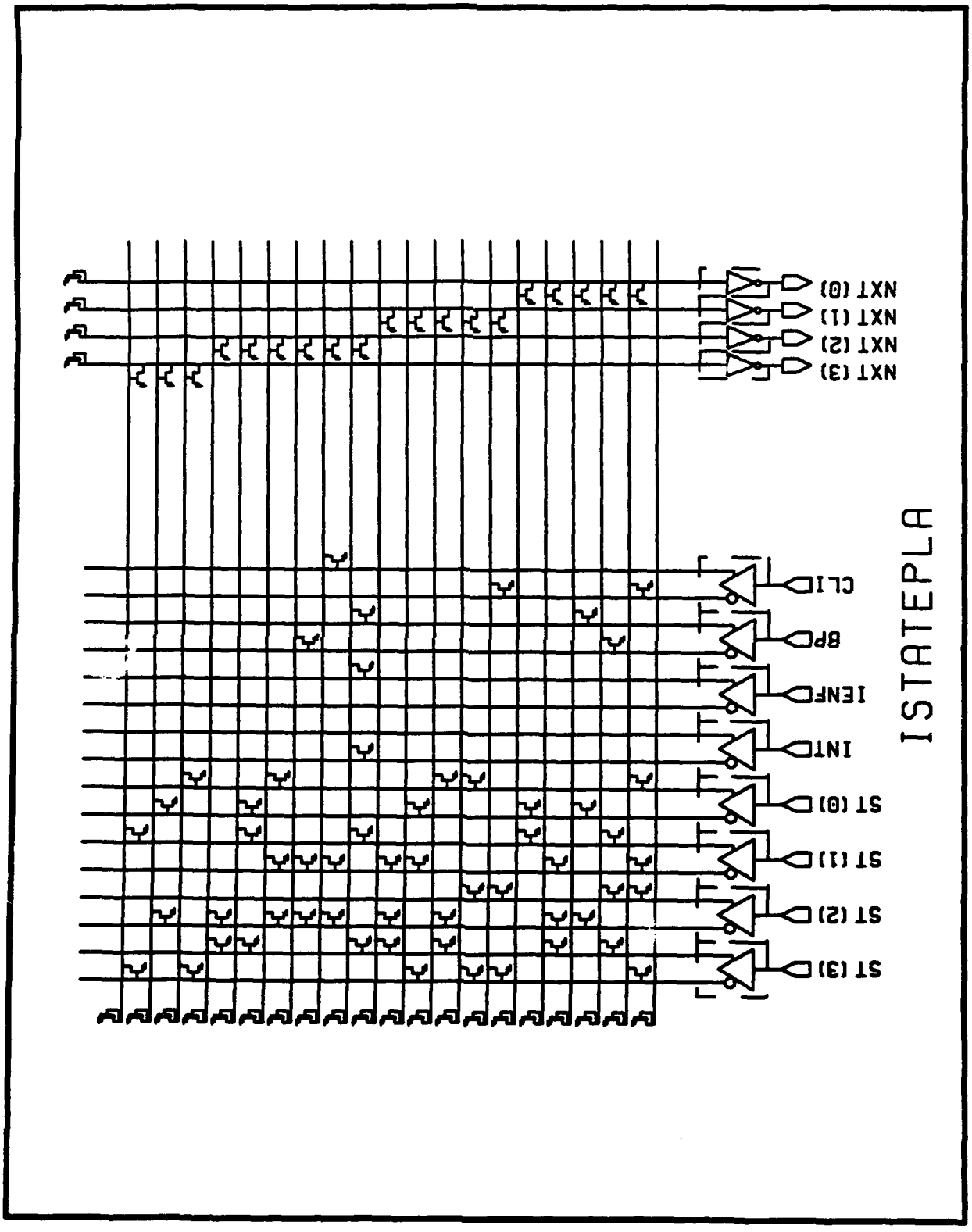

UXX
ISR
CLI(7:0)
INT(7:0)
IRQF(7:0)
LD
CLR
CLK
OUT
IN
IN
IN
IN
IN

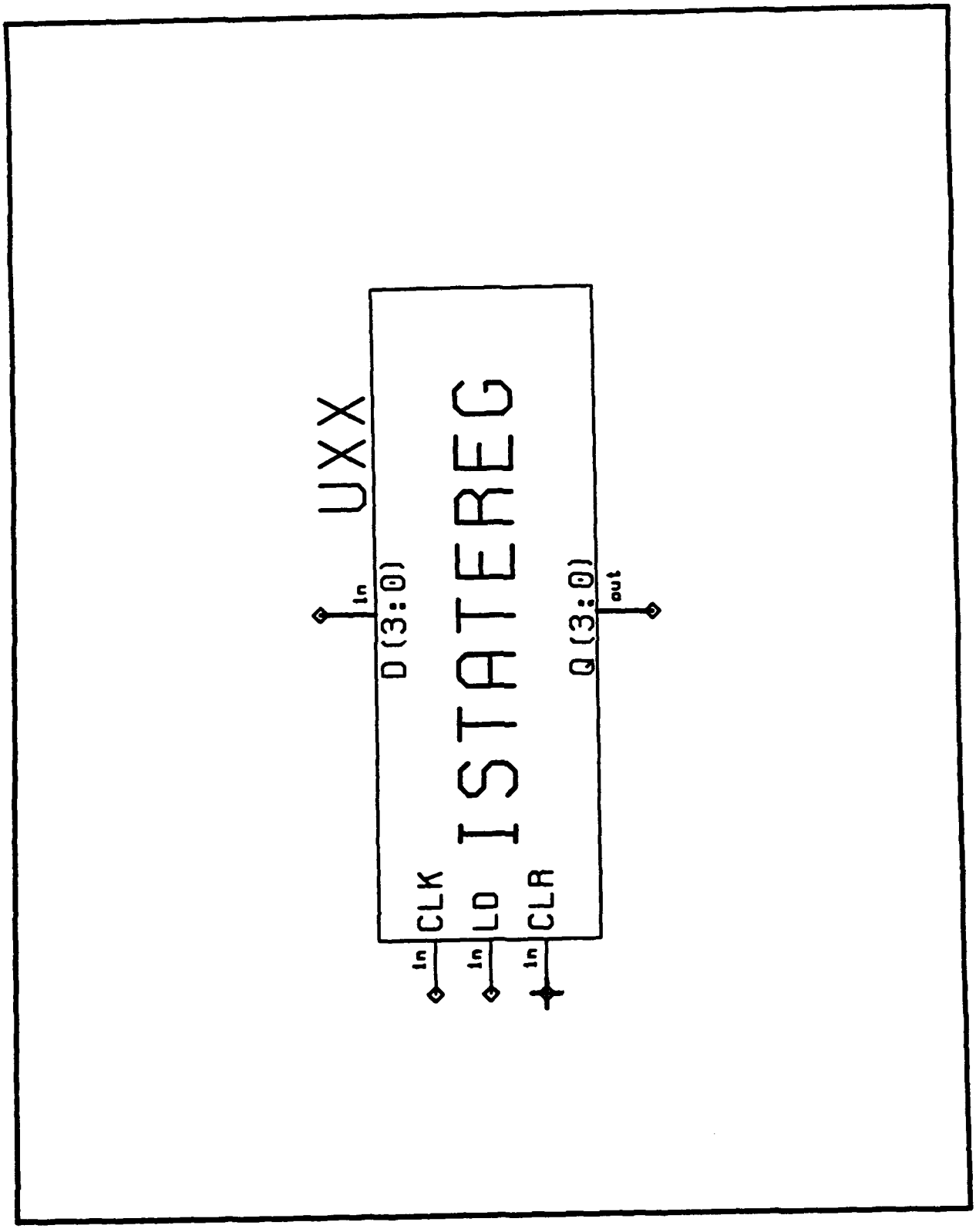

ISR
IRQF (I)
I$2
ISRBIT
OF
CLI
D
LD
CLK
CLR
LDB
CLKB
CLRB
FOR I := 0 TO 7
SQ
SQIW
INV
(DH) (DL)
(EH) (EL)
LD
CLK
CLR

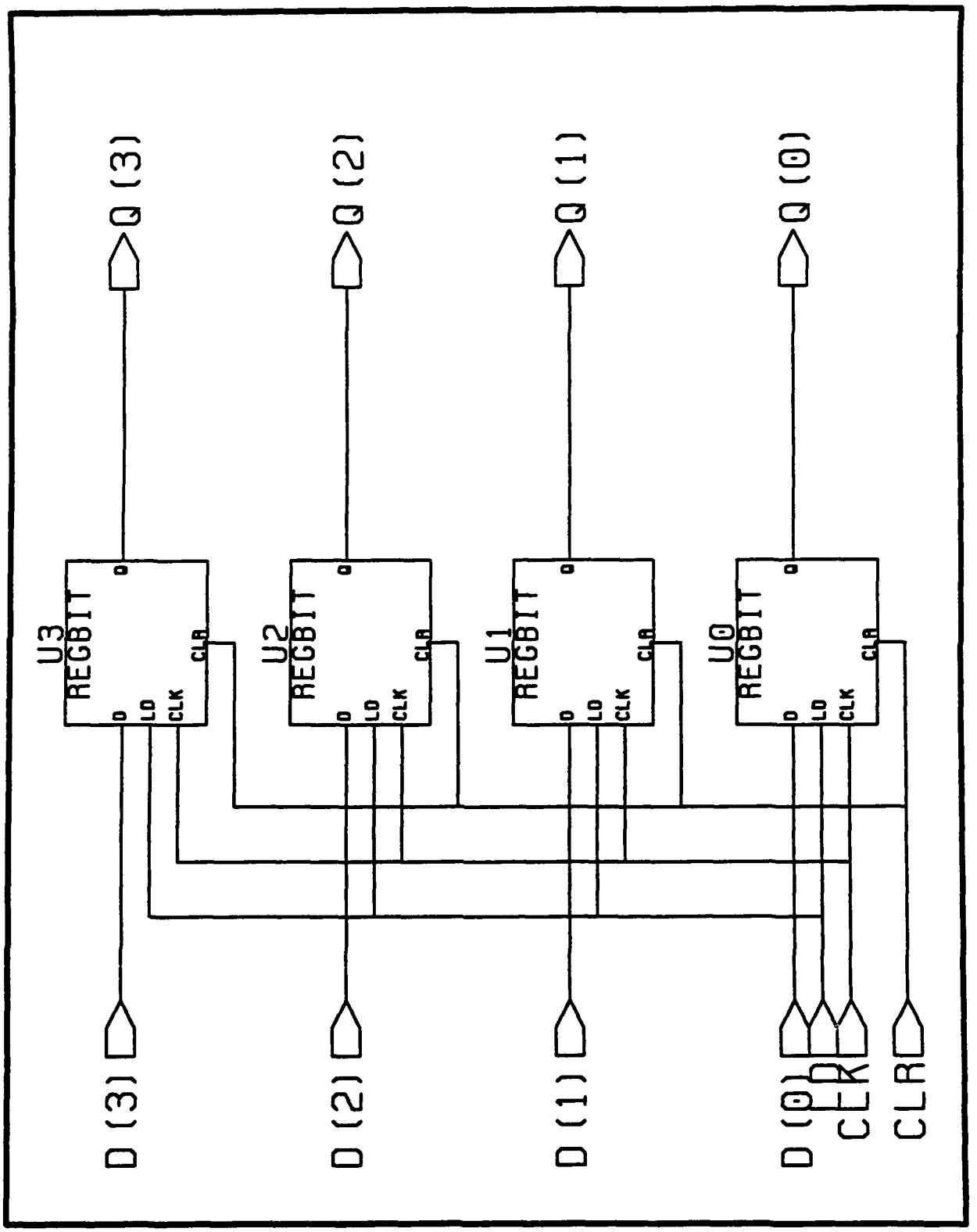

UXX
ISRBIT
OUT
QF
CLR
NI
CLI
D
LD
CLK
IN
IN
IN
IN

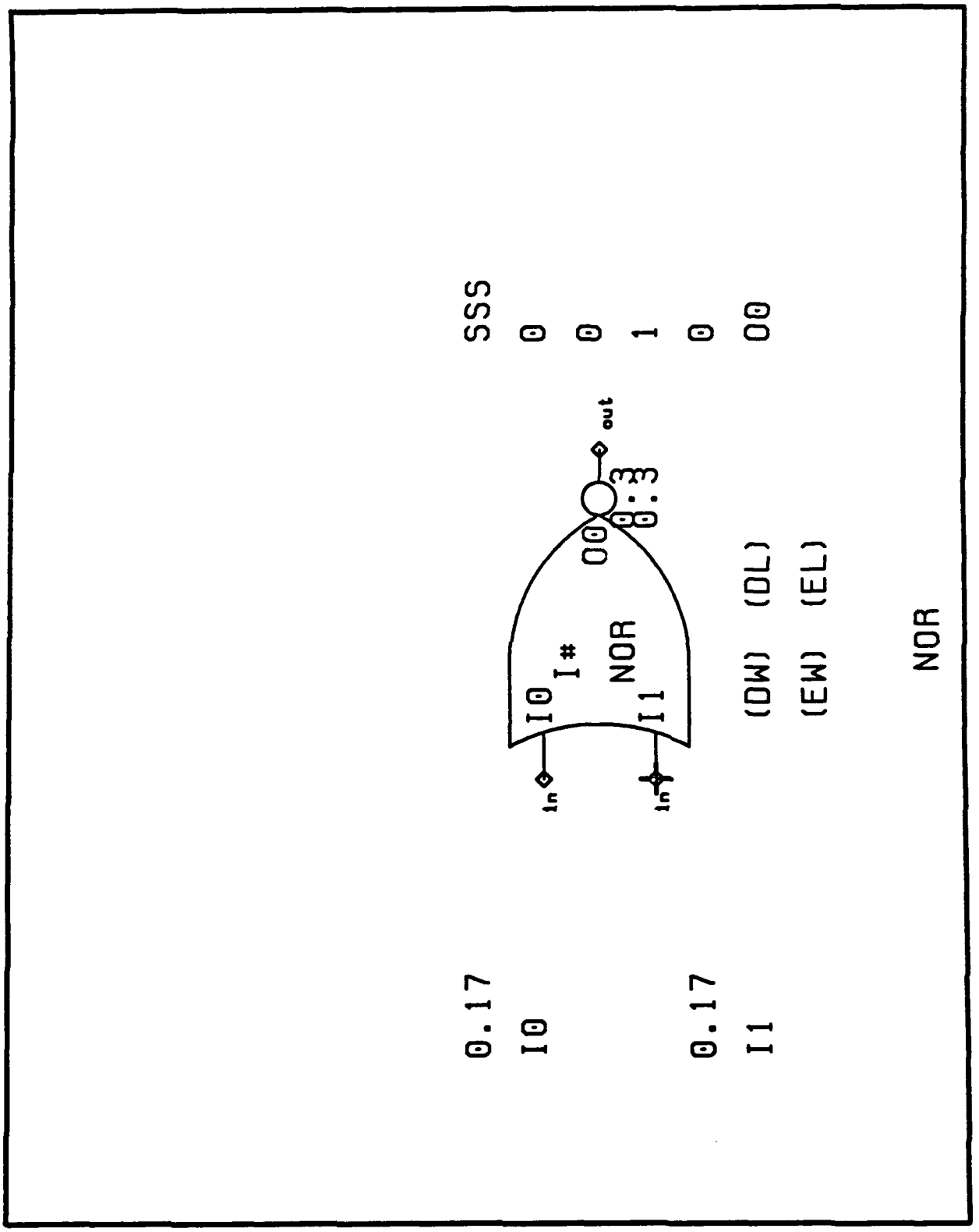

QF
CLK
CLRD
CLID
LD
D
ISRBIT

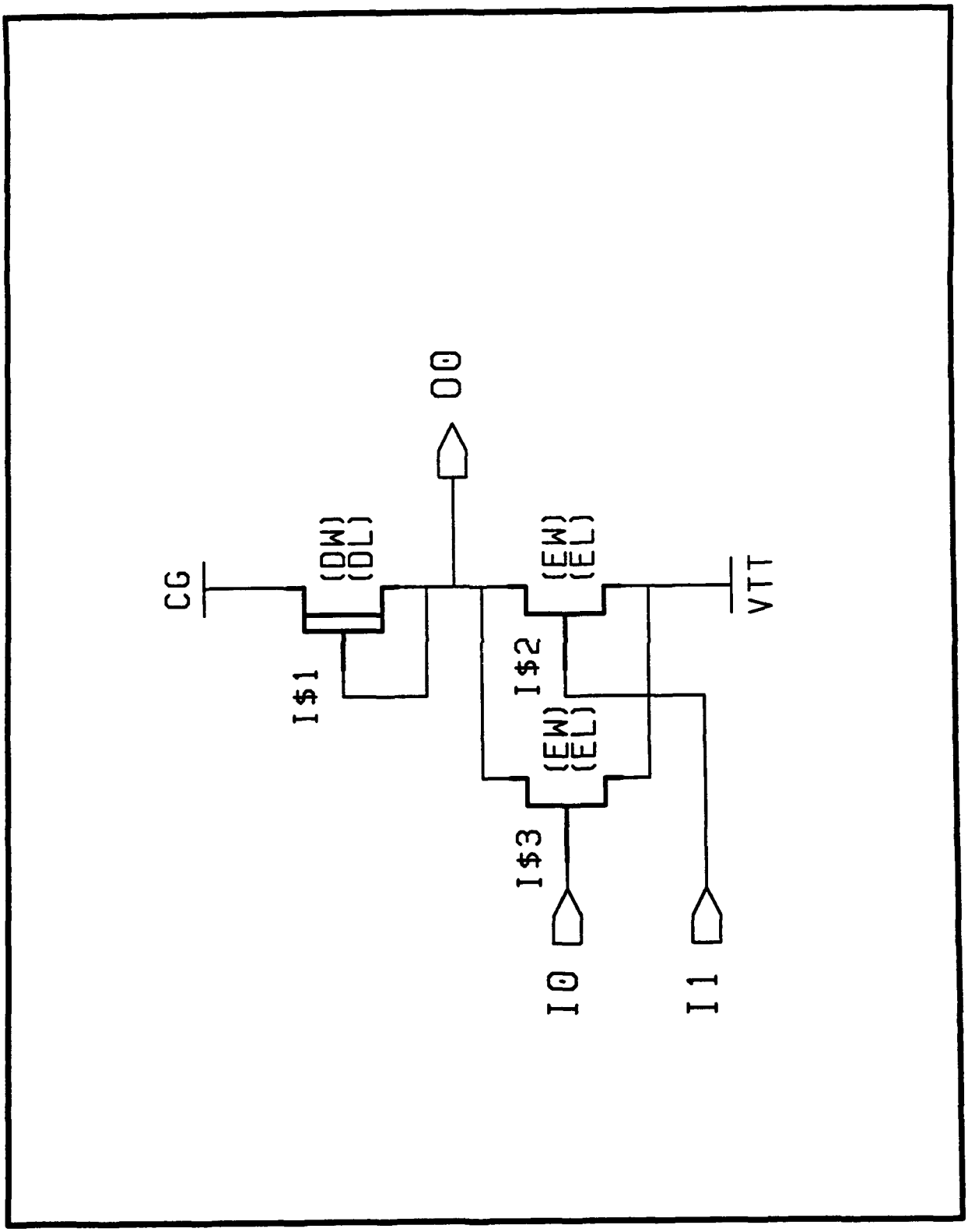

ST (3:0)
NXT (3:0)
INT
IENF
BP
CLI
ISTATEPLA

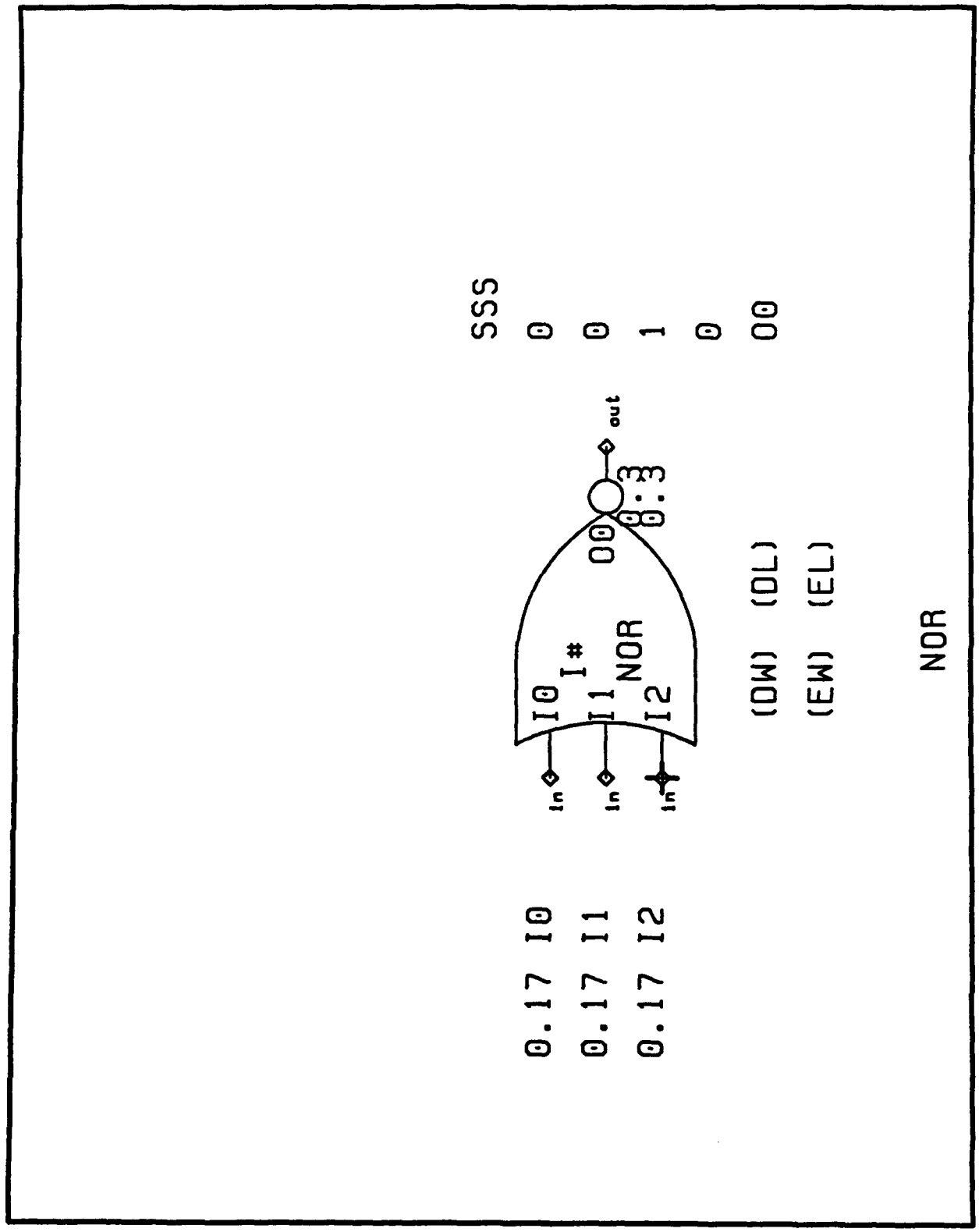

NXT (0)
NXT (1)
NXT (2)
NXT (3)
CLI
BP
IENF
INT
ST (0)
ST (1)
ST (2)
ST (3)
ISTATEPLA

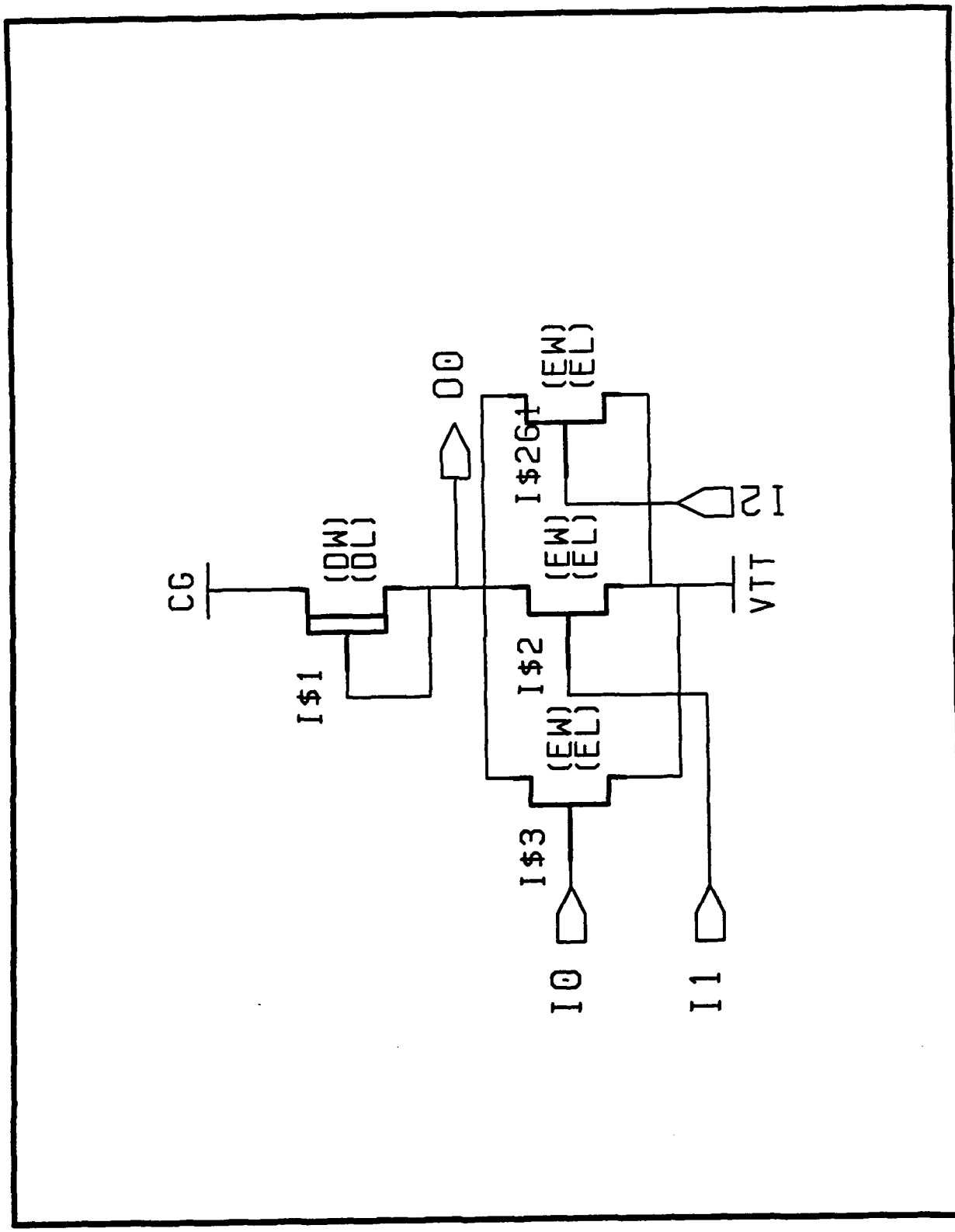

UXX
ISTATEREG
D(3:0)
Q(3:0)
In
out
CLK
LD
CLR
In
In
In

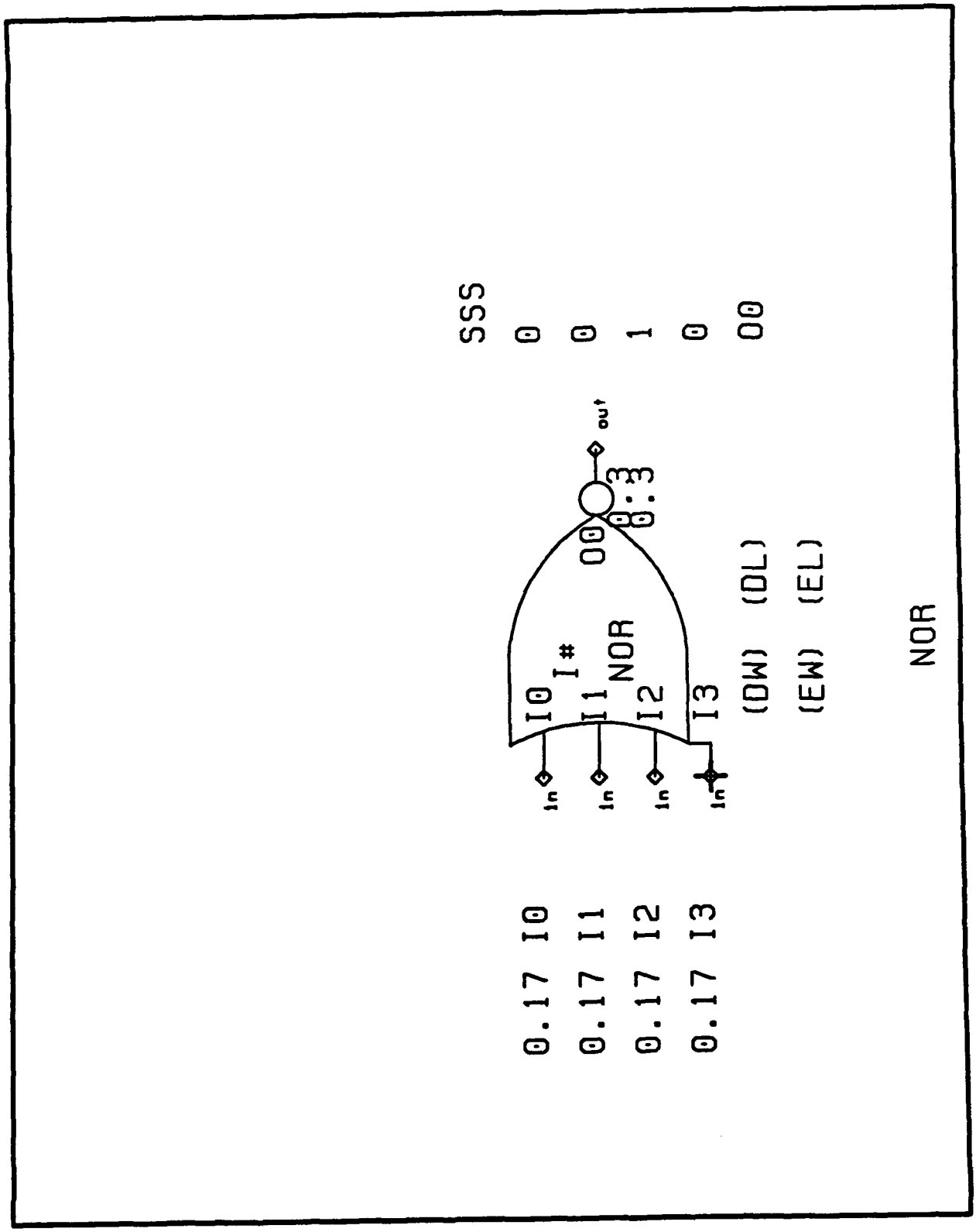

Q(3)
Q(2)
Q(1)
Q(0)
U3
U2
U1
U0
REGBIT
D
LD
CLK
CLR
D(3)
D(2)
D(1)
D(0)
CLK
CLR

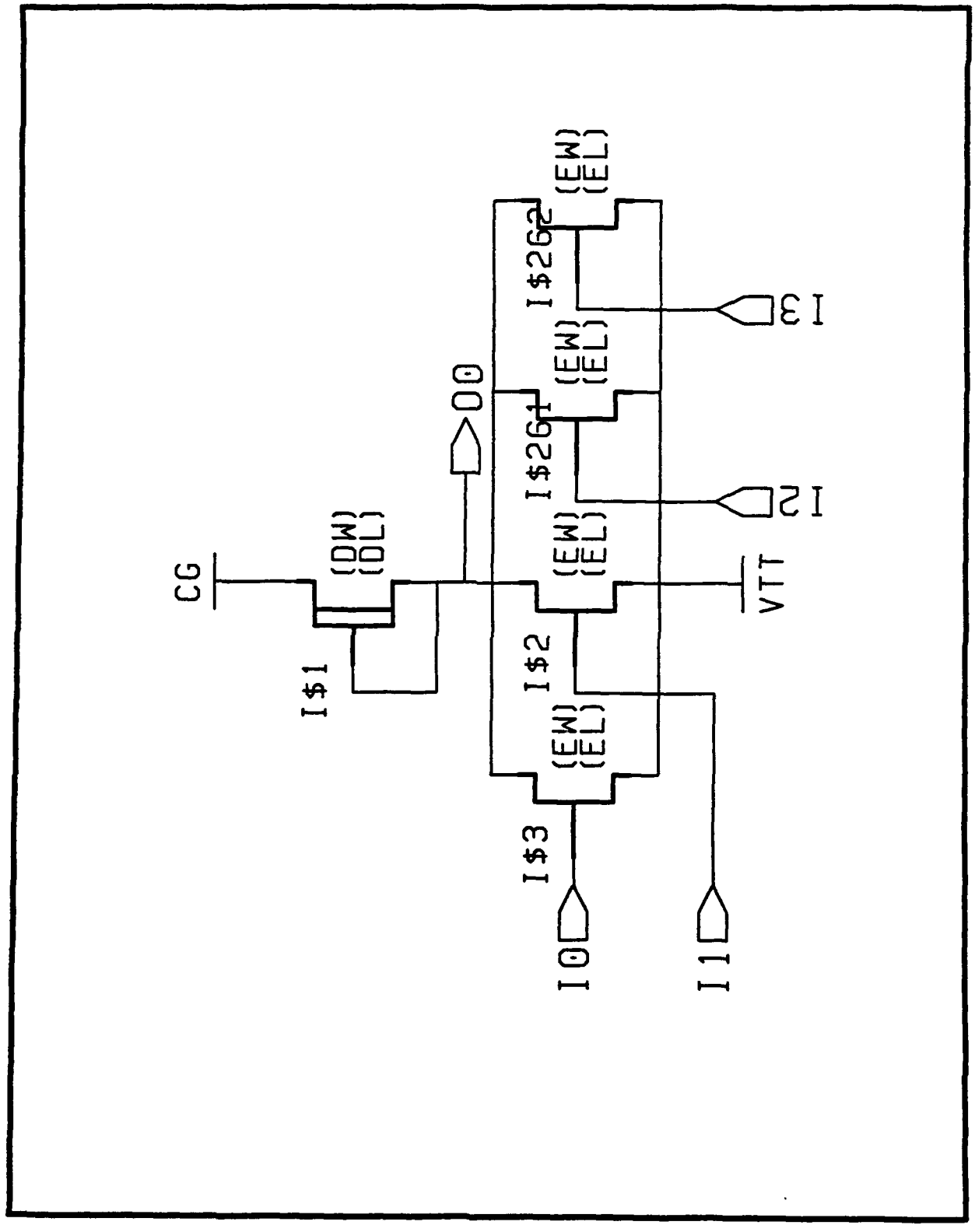

SSS
0 0 1 0 00
out
0.3
00
I0
I#
NOR
I1
In
In
(DW) (DL)
(EW) (EL)
NOR
0.17
I0
0.17
I1

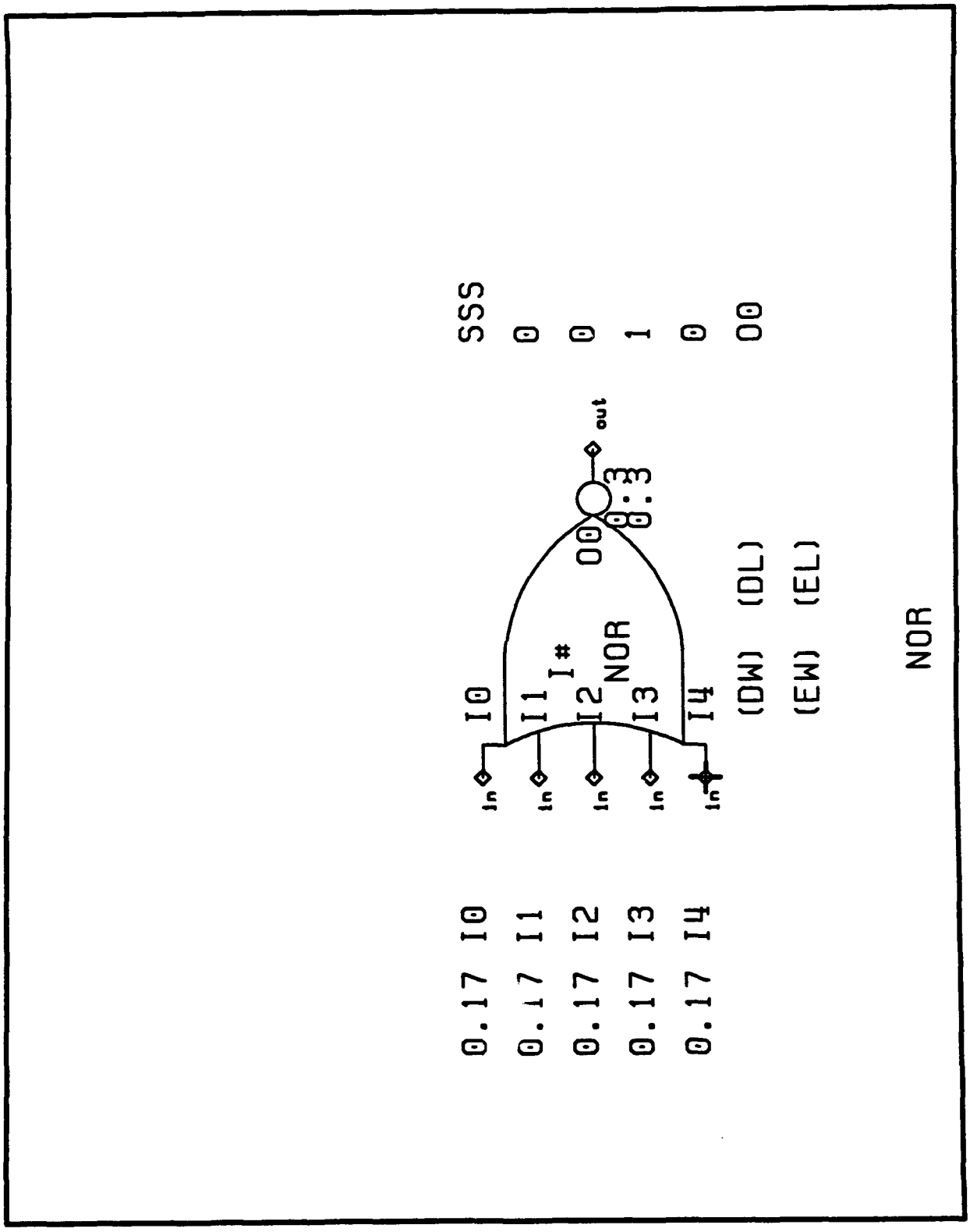

O0
CG
(DW)
(DL)
(EW)
(EL)
VTT
I$1
I$2
(EW)
(EL)
I$3
I0
I1

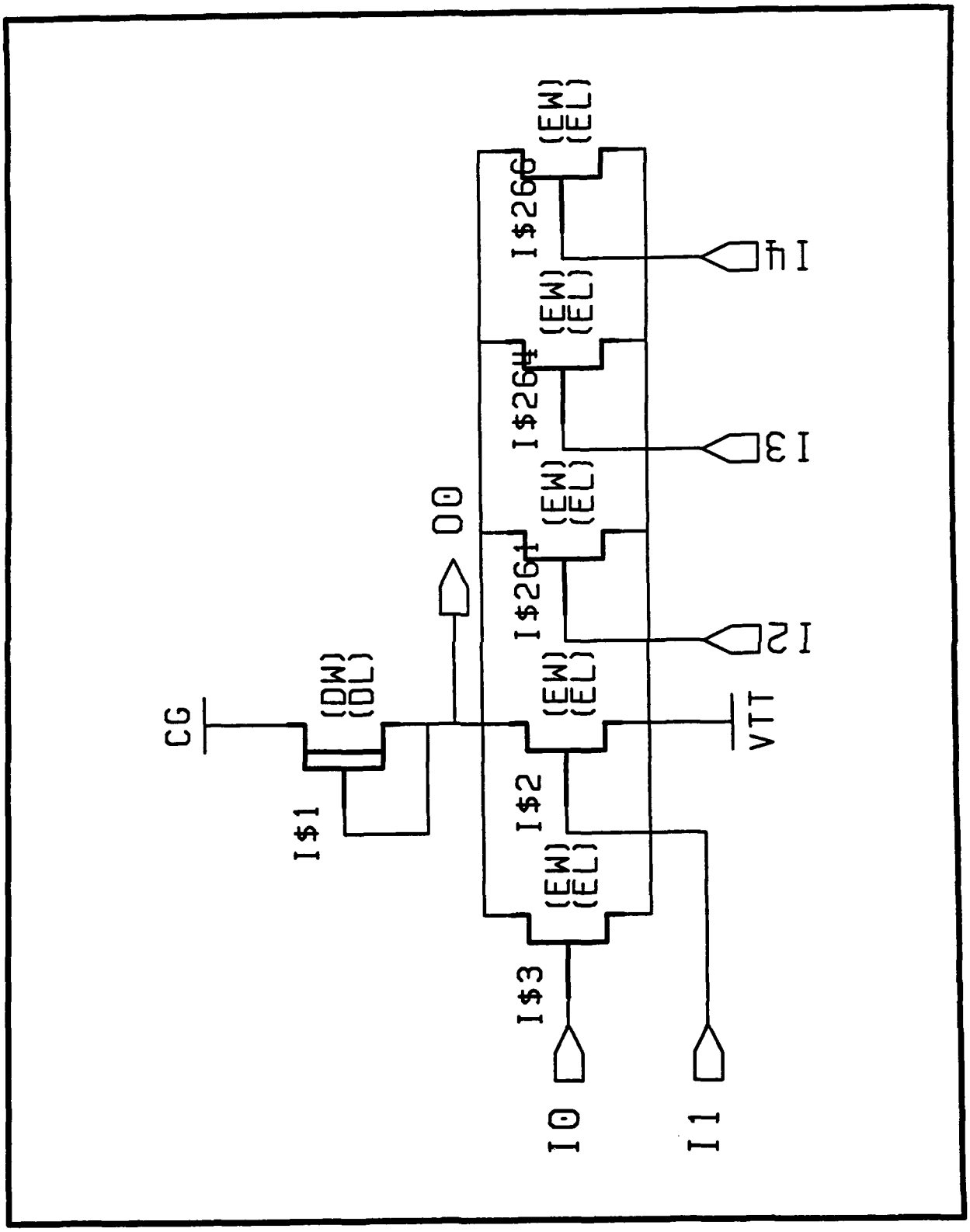

SSS
0
0
1
0
00
out
8:3
00
I0
I#
I1
NOR
I2
In
In
In
(OW) (OL)
(EW) (EL)
NOR
0.17 I0
0.17 I1
0.17 I2

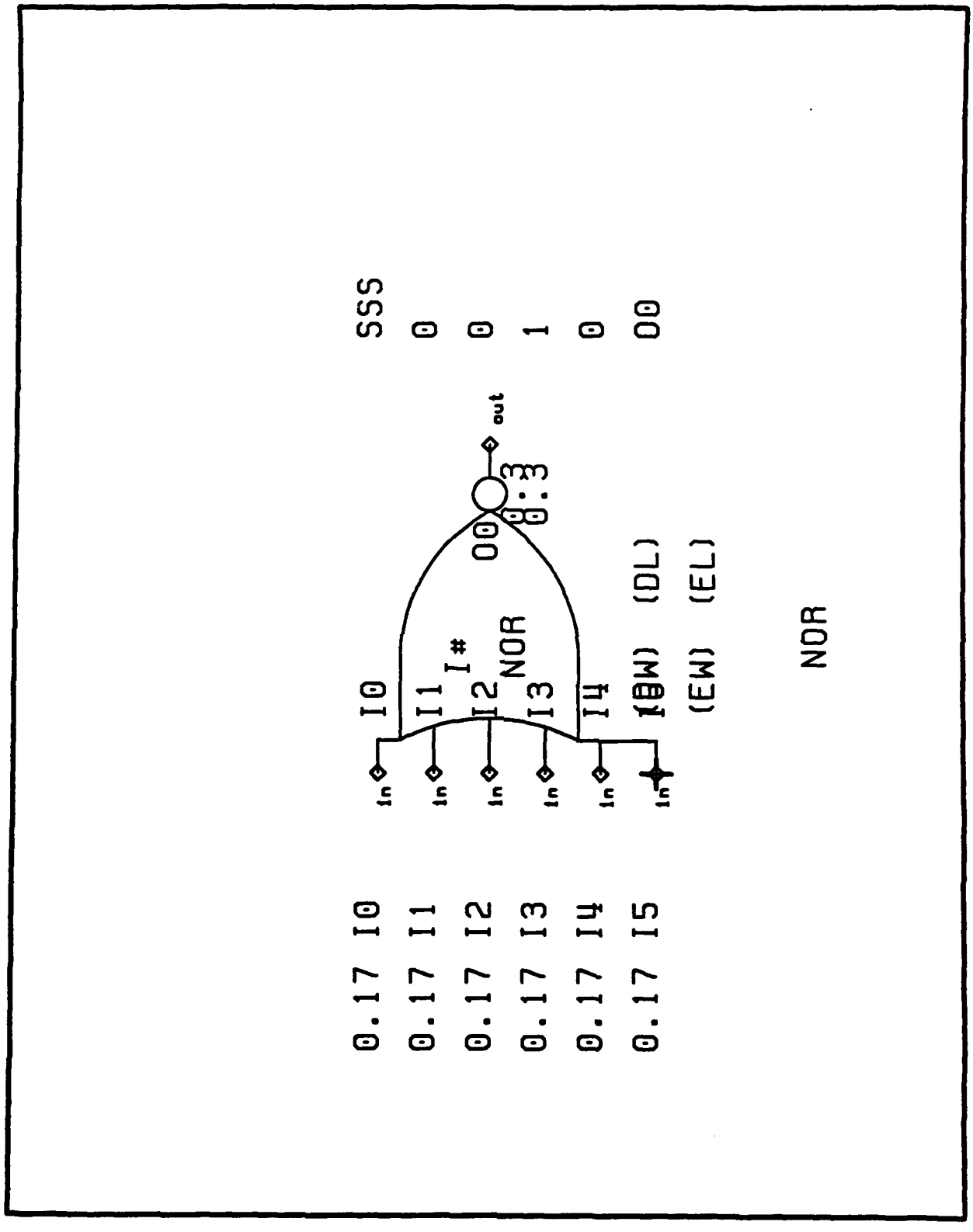

O0
(EW)
(EL)
I$26
I2
(DW)
(DL)
(EW)
(EL)
CG
VTT
I$1
I$2
(EW)
(EL)
I$3
I0
I1

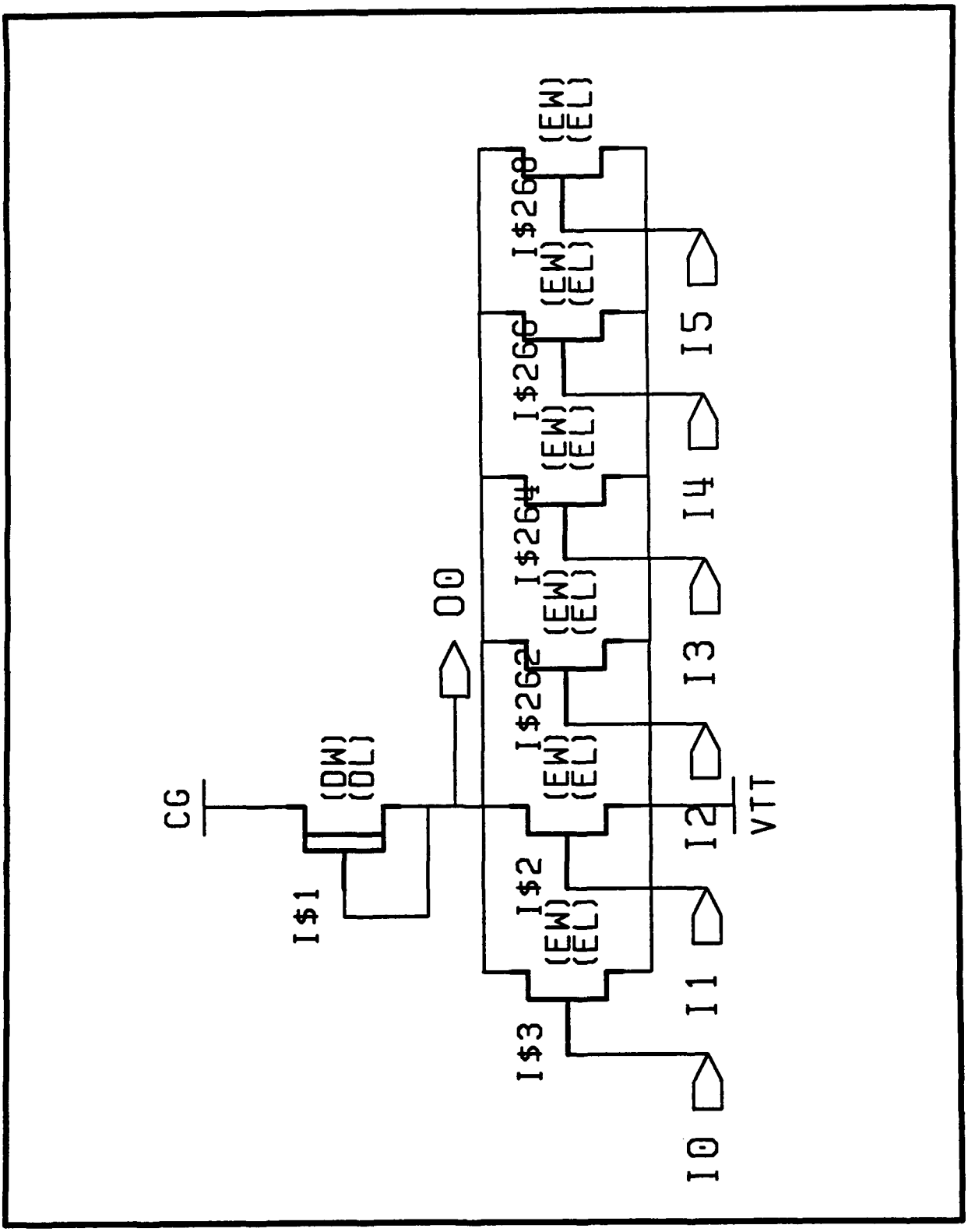

SSS
0 0 1 0 00
out
0.3
0.3
00
I0
I#
I1
NOR
I2
I3
(DW) (DL)
(EW) (EL)
NOR
in
in
in
in
0.17 I0
0.17 I1
0.17 I2
0.17 I3

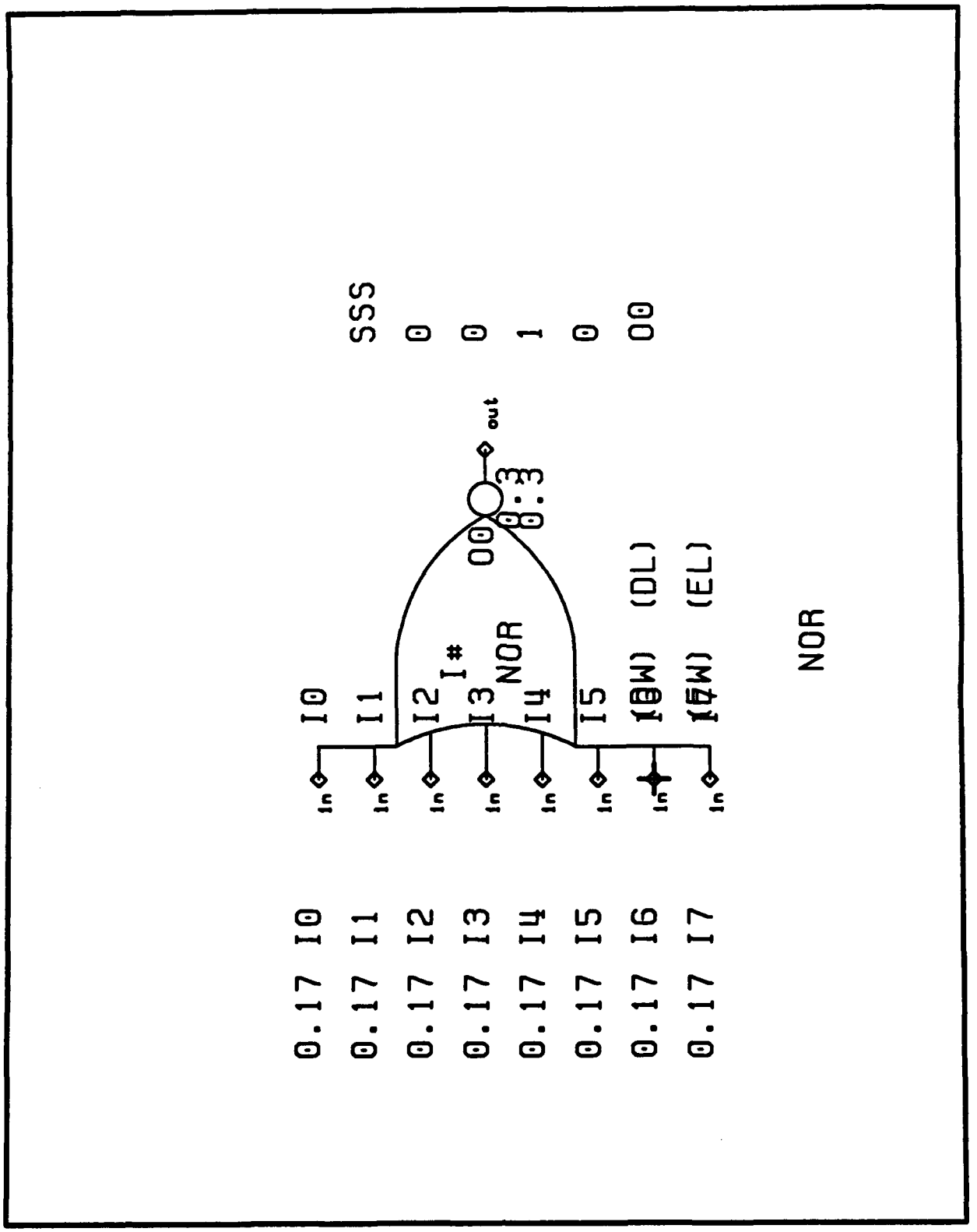

I3
I2
I1
I0
O0
CG
VTT
I$1
I$2
I$3
I$261
I$262
(DW)
(DL)
(EW)
(EL)

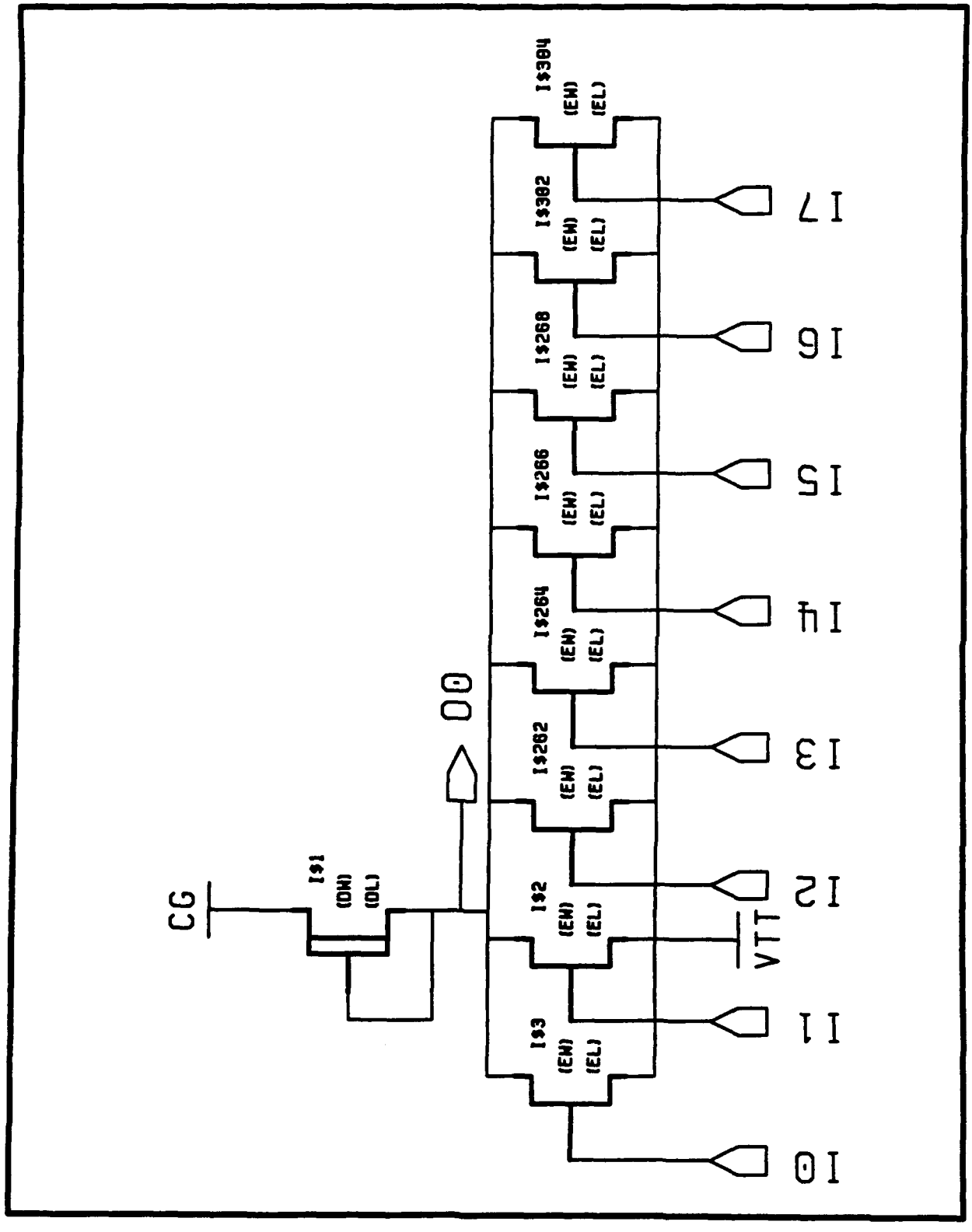

SSS
0
0
1
0
00
out
0:3
00
I#
NOR
I0
I1
I2
I3
I4
in
in
in
in
in
(DW) (DL)
(EW) (EL)
NOR
0.17 I0
0.17 I1
0.17 I2
0.17 I3
0.17 I4

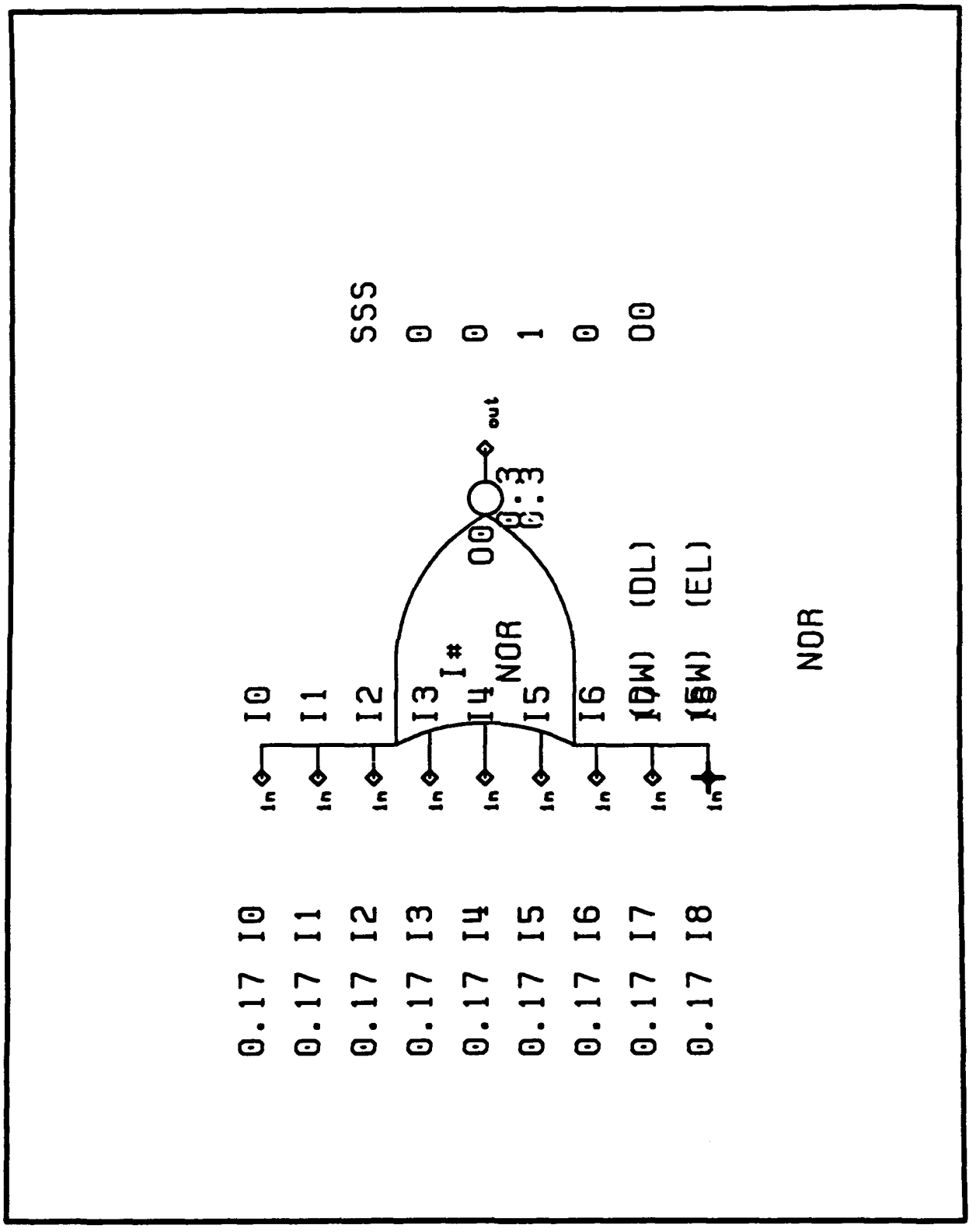

I$266
(EW)
(EL)
I4
I$264
(EW)
(EL)
I3
I$262
(EW)
(EL)
I2
I$2
(EW)
(EL)
VTT
I$3
(EW)
(EL)
I0
I1
O0
I$1
(DW)
(DL)
CG

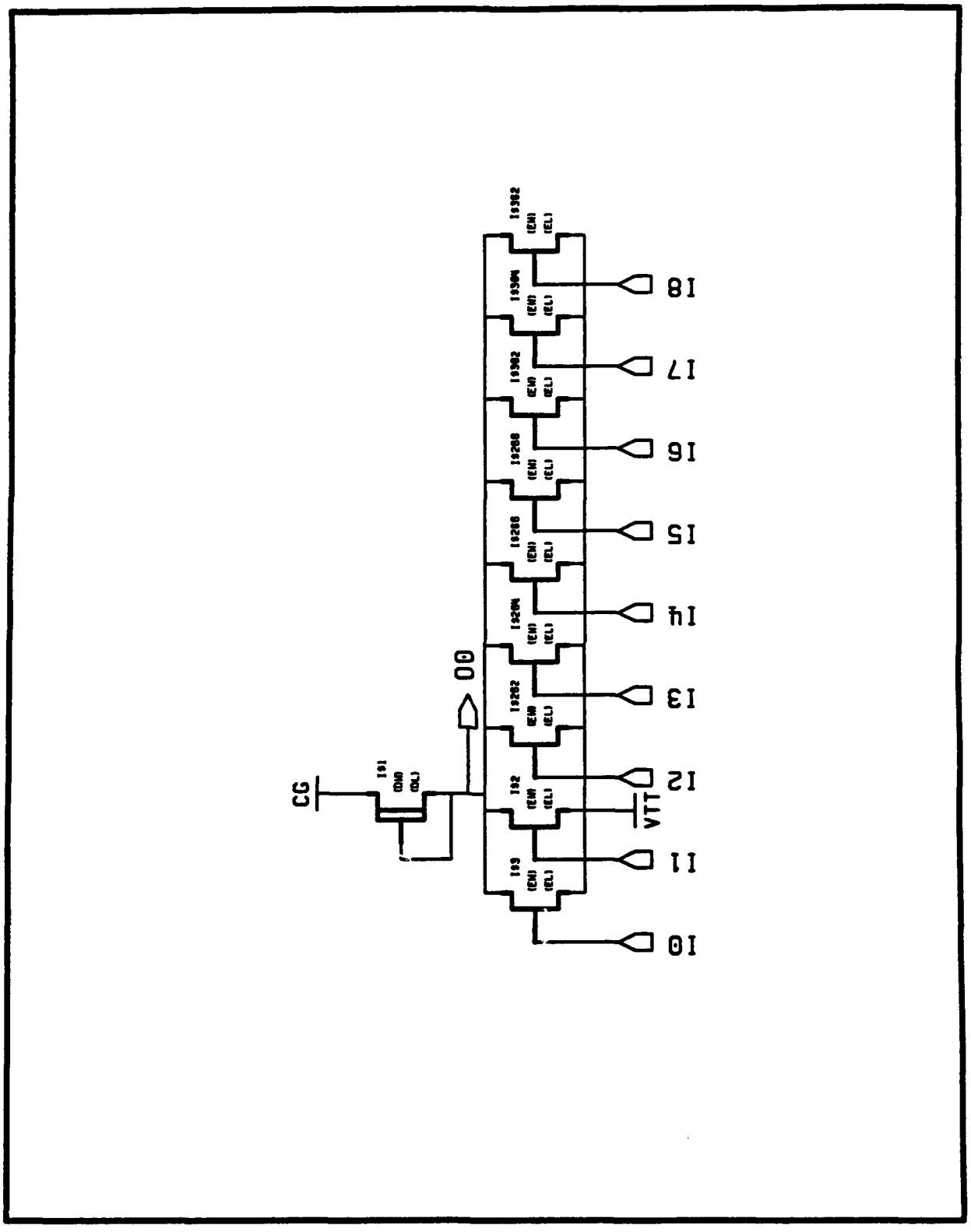

SSS
0
0
1
0
00
out
00
8.3
8.3
I0
I1
I#
I2
NOR
I3
I4
(BW)
(DL)
(EW)
(EL)
In
In
In
In
In
In
NOR
0.17 I0
0.17 I1
0.17 I2
0.17 I3
0.17 I4
0.17 I5

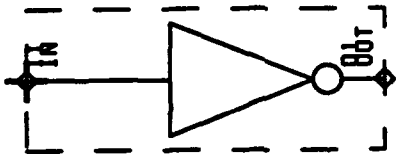

CG
(DW)
(DL)
I$1
O0
I$3
I$2
I$262
I$264
I$266
I$268
(EW)
(EL)
I0
I1
I2
I3
I4
I5
VTT

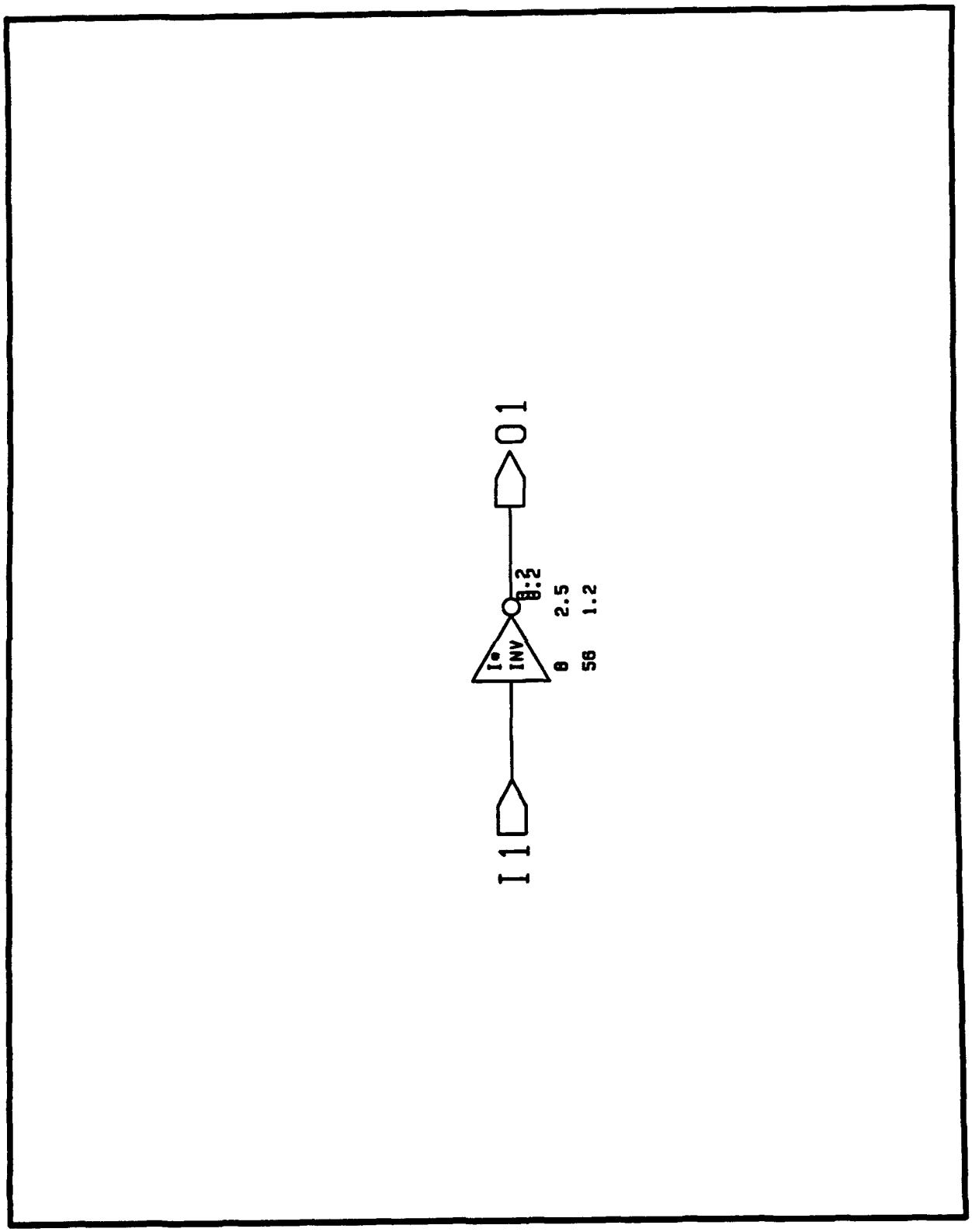

SSS
0
0
1
0
00
out
8.3
00
I0
I1
I2
I#
I3
NOR
I4
I5
(DL)
(EL)
NOR
0.17 I0
0.17 I1
0.17 I2
0.17 I3
0.17 I4
0.17 I5
0.17 I6
0.17 I7

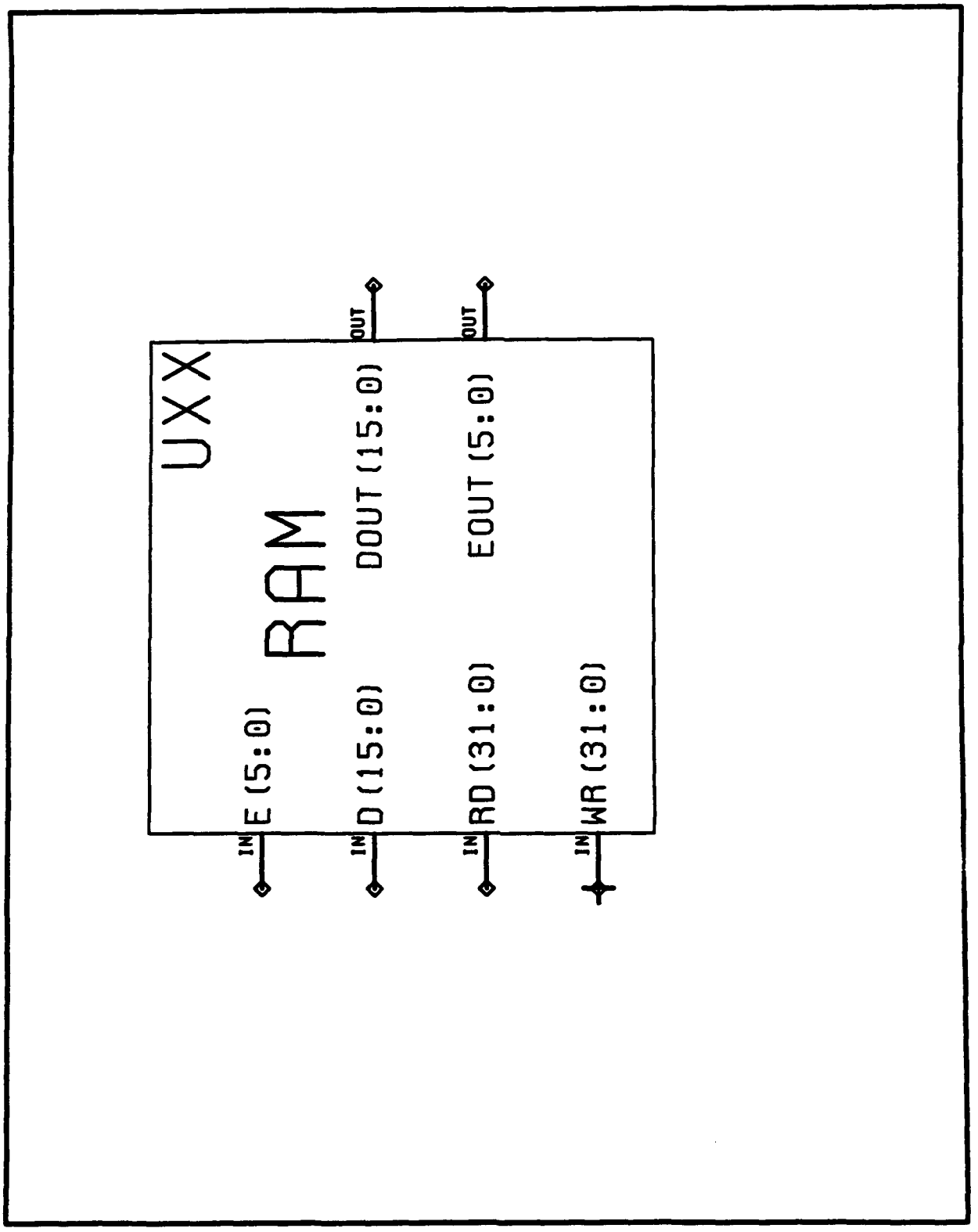

I$304
(EH)
(EL)
I$302
(EH)
(EL)
I$268
(EH)
(EL)
I$266
(EH)
(EL)
I$264
(EH)
(EL)
I$262
(EH)
(EL)
I$2
(EH)
(EL)
I$3
(EH)
(EL)
I$1
(DN)
(DL)
I7
I6
I5
I4
I3
I2
I1
I0
OO
CG
VTT

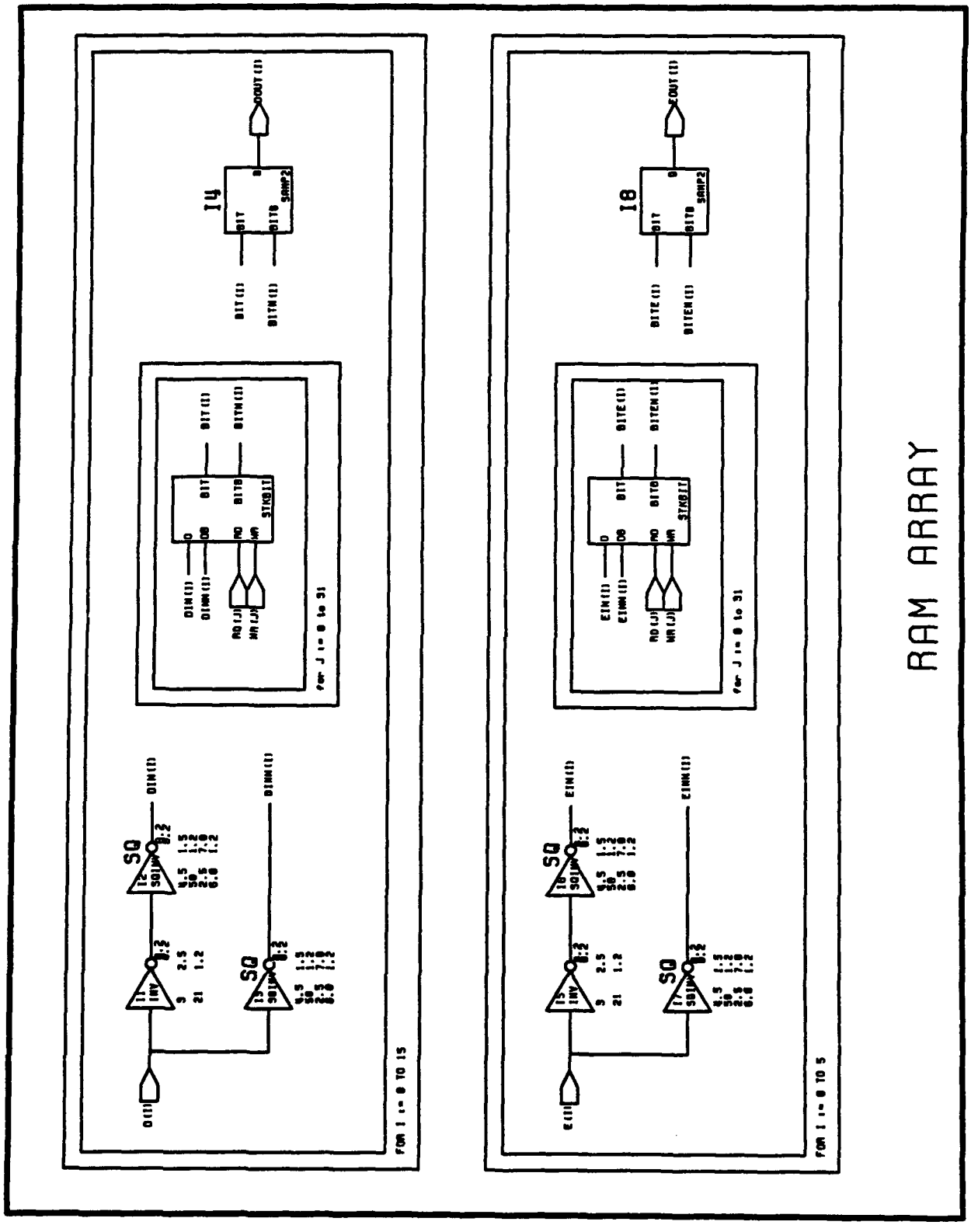

SSS
0
0
1
0
00
out
00
Q:3
Q:3
I0
I1
I2
I3
I#
I4
NOR
I5
I6
(DL)
(EL)
NOR
0.17 I0
0.17 I1
0.17 I2
0.17 I3
0.17 I4
0.17 I5
0.17 I6
0.17 I7
0.17 I8

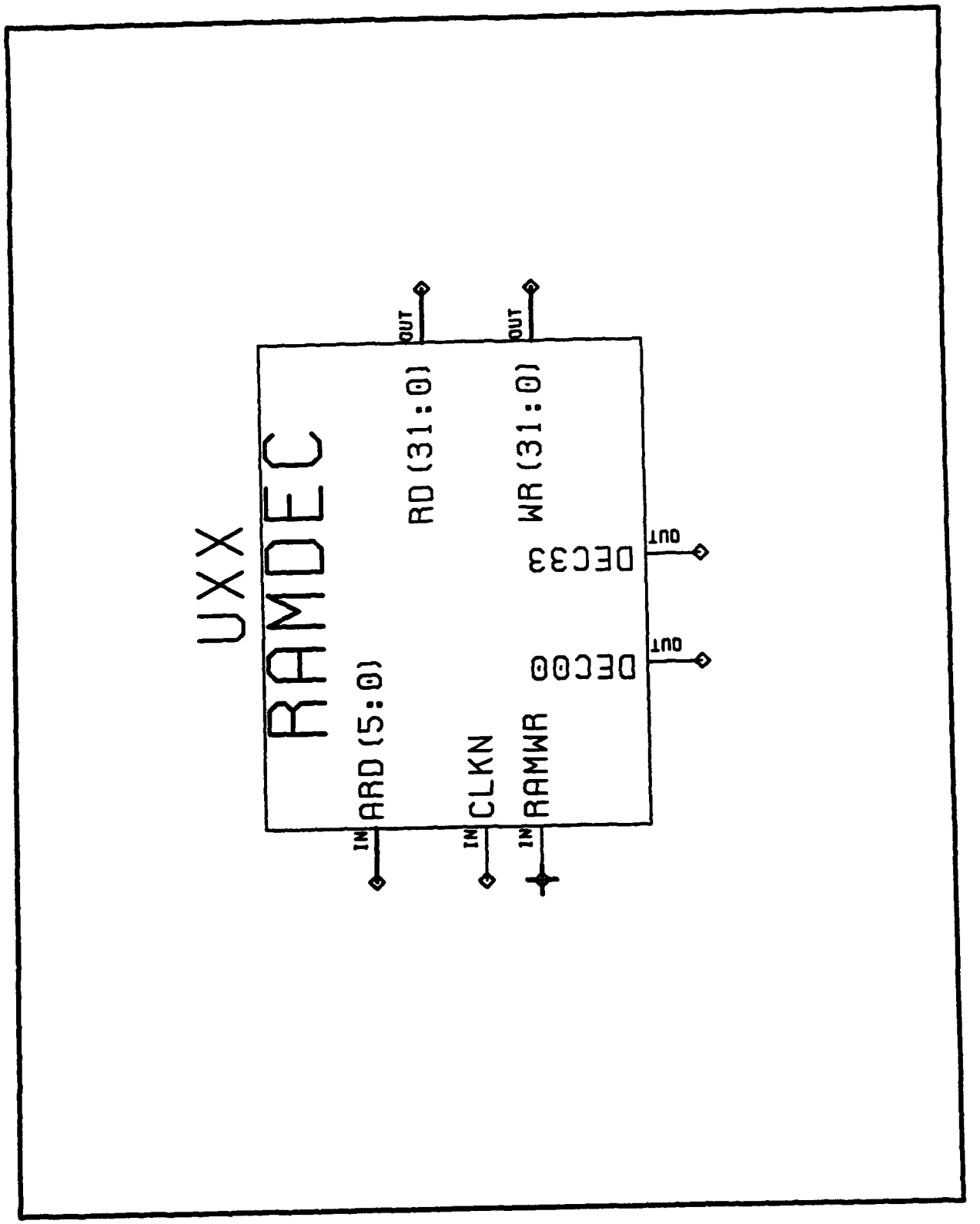

CG
VTT
I8
I7
I6
I5
I4
I3
I2
I1
I0

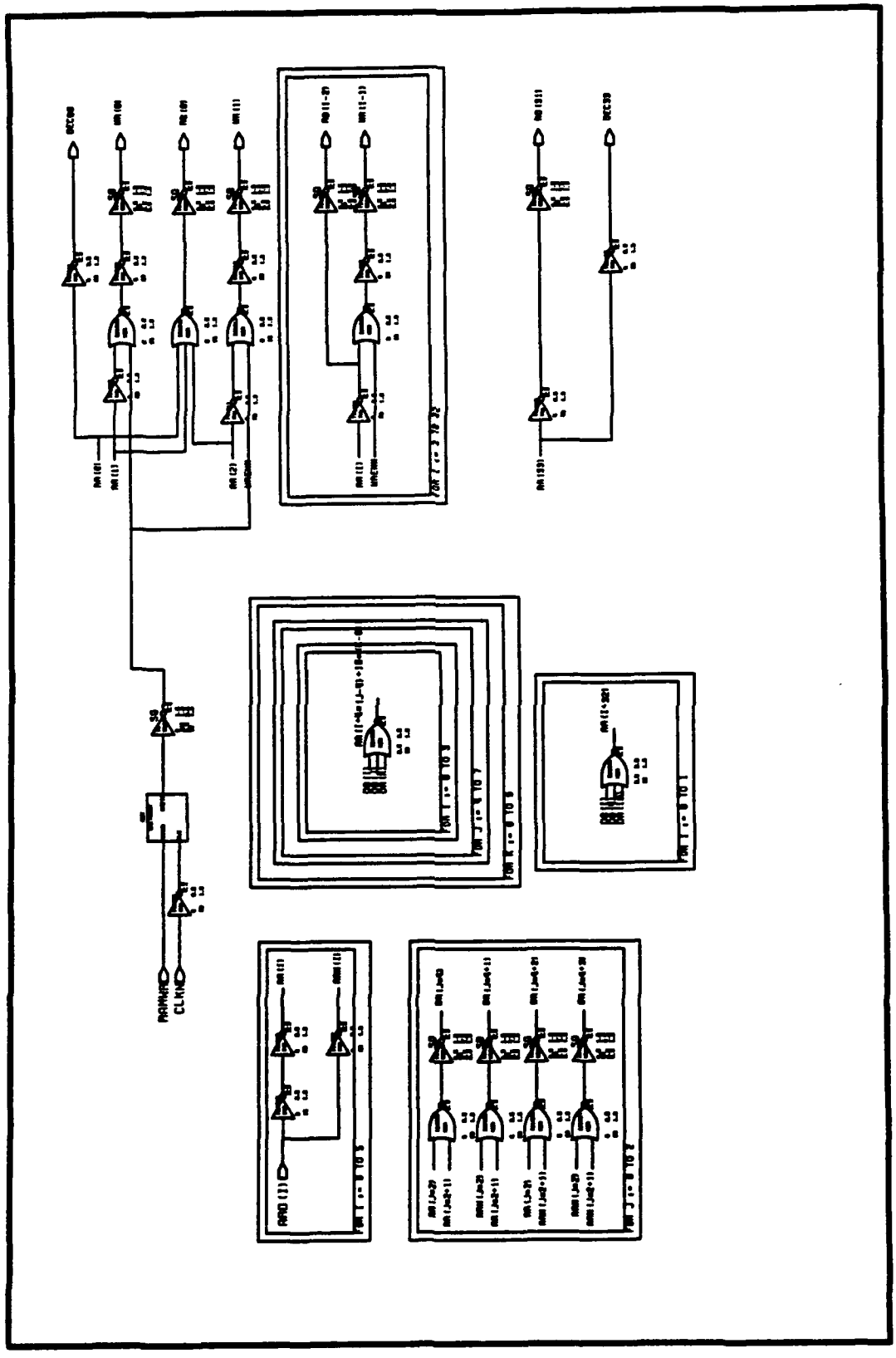

IN
Bdr

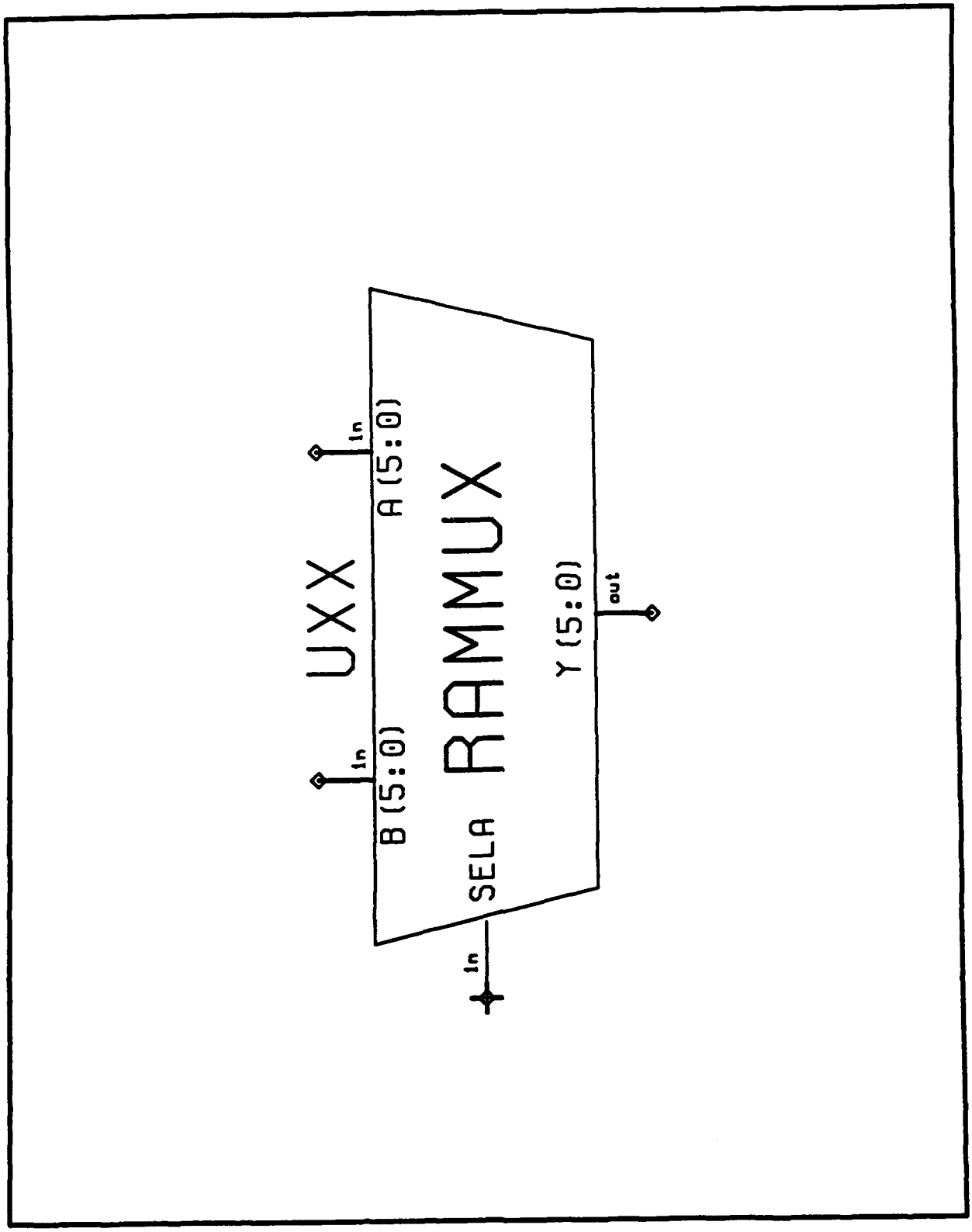

O1
8.2
2.5
1.2
I•
INV
8
56
I1

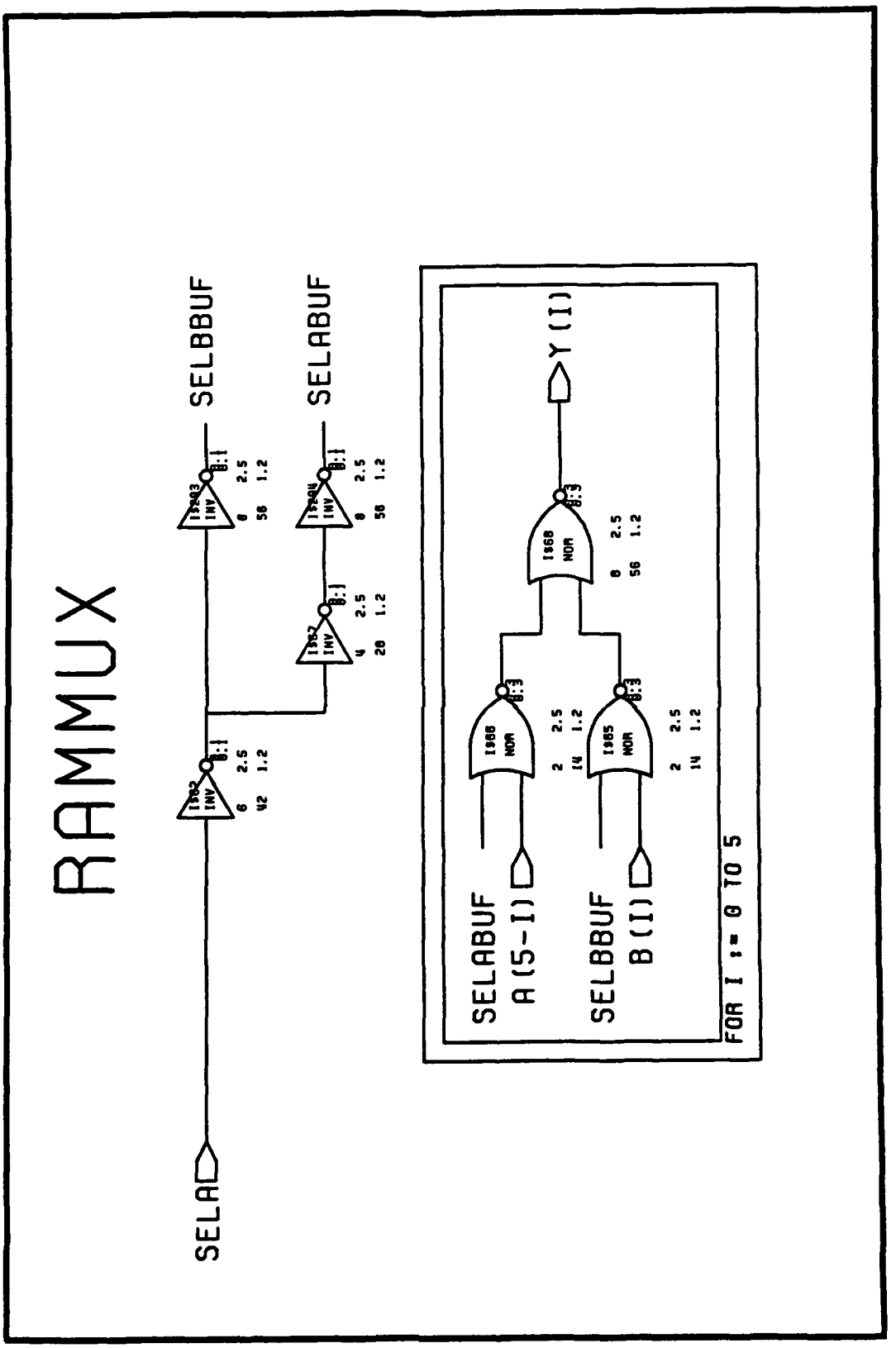

UXX
RAM
DOUT (15:0)
EOUT (5:0)
E (5:0)
D (15:0)
RD (31:0)
WR (31:0)
OUT
OUT
IN
IN
IN
IN

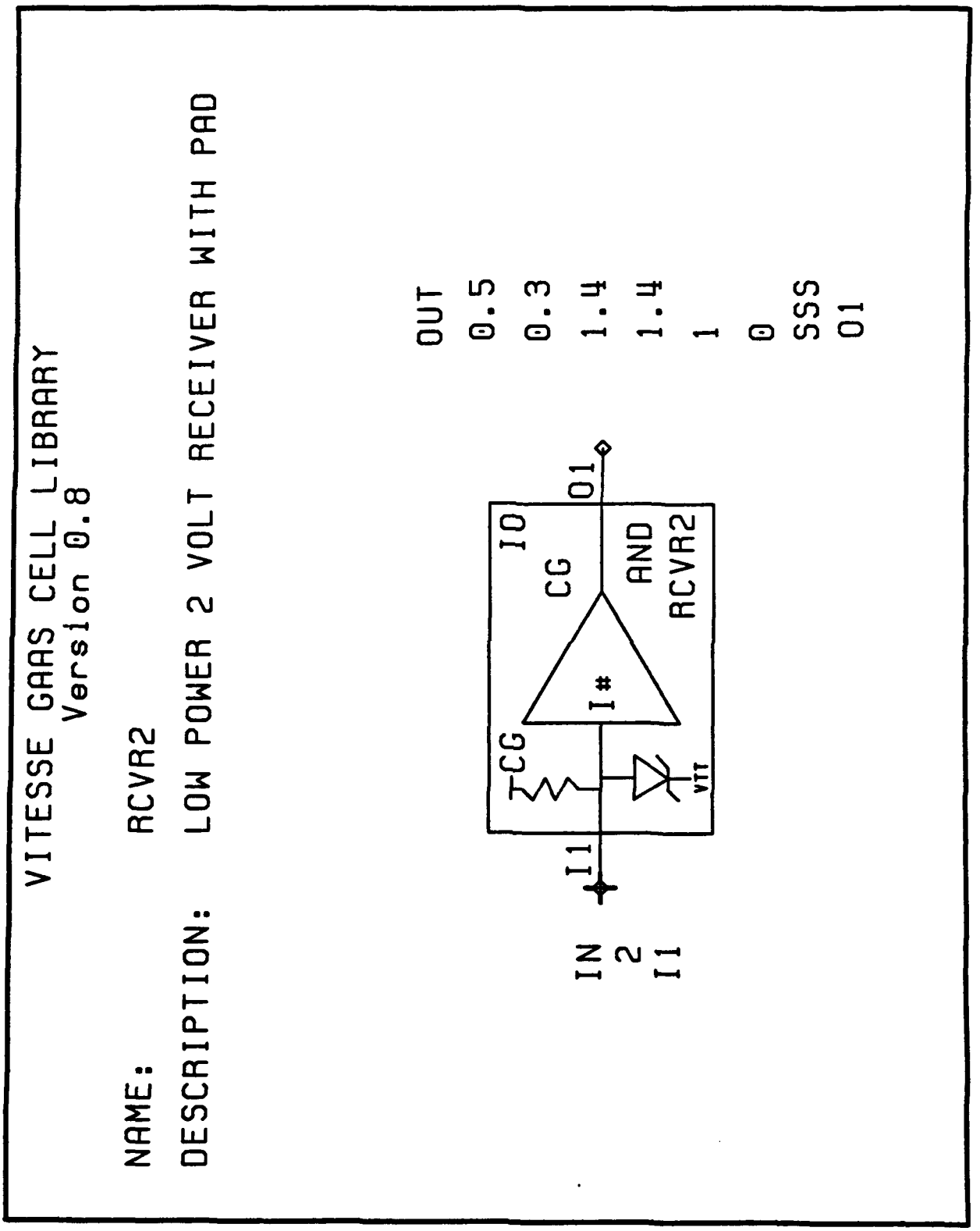

RAM ARRAY

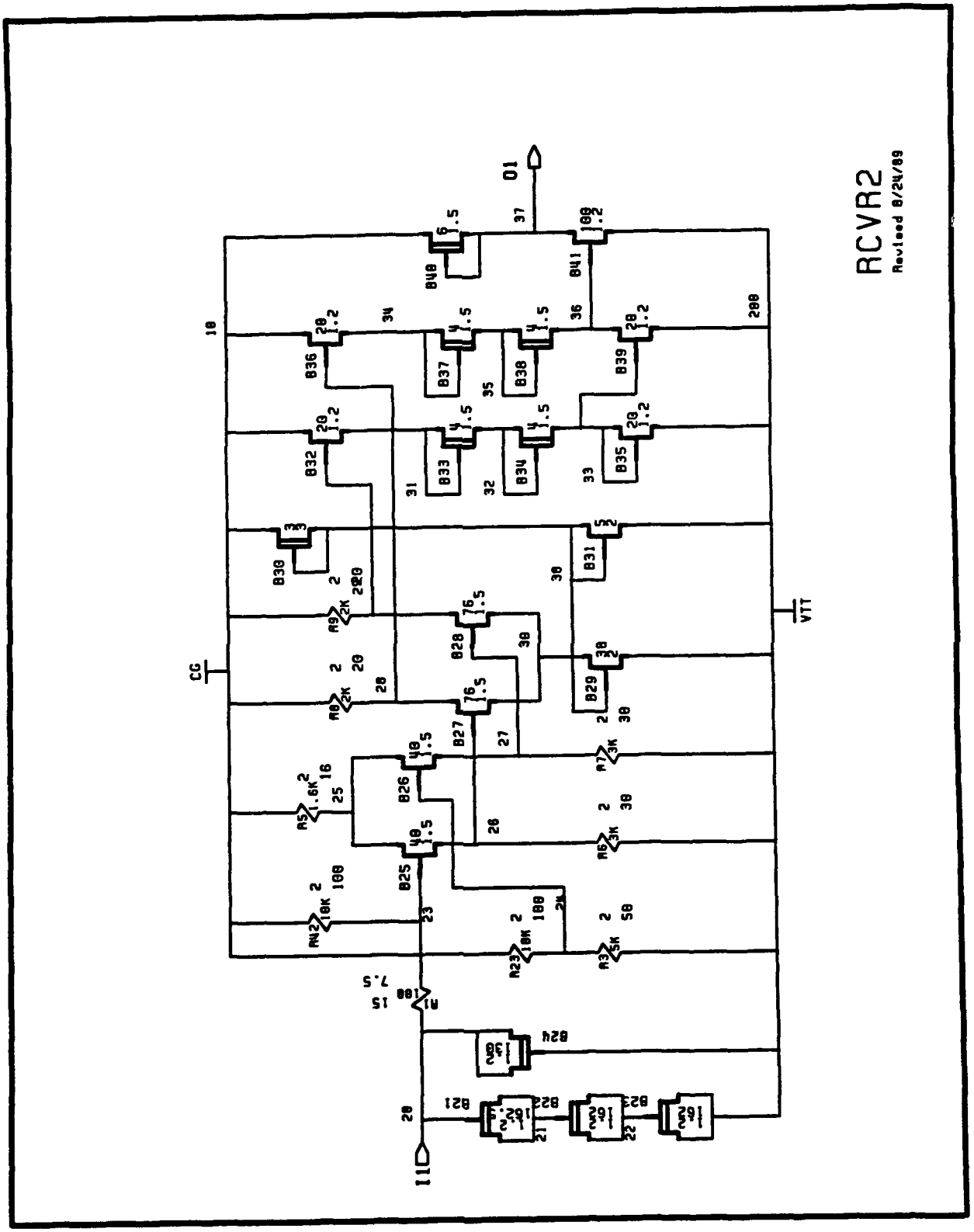

UXX
RAMDEC
RD(31:0)
WR(31:0)
DEC33
DEC00
ARD(5:0)
CLKN
RAMWR
OUT
OUT
OUT
IN
IN
IN

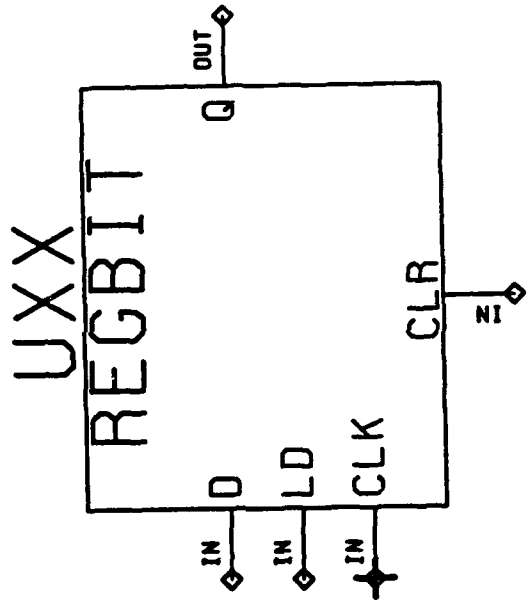


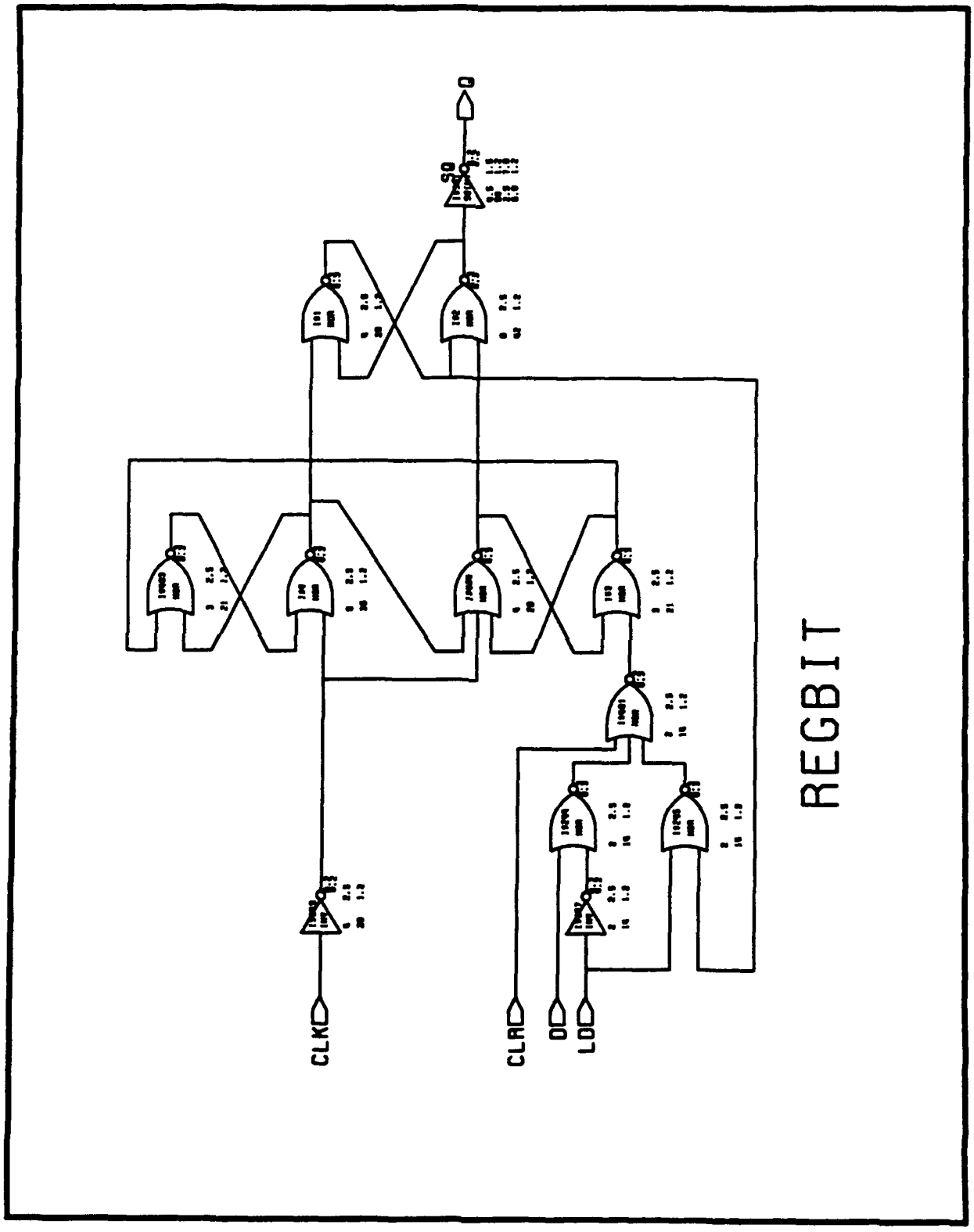

UXX
RAMUX
A(5:0)
B(5:0)
SELA
Y(5:0)
in
in
in
out

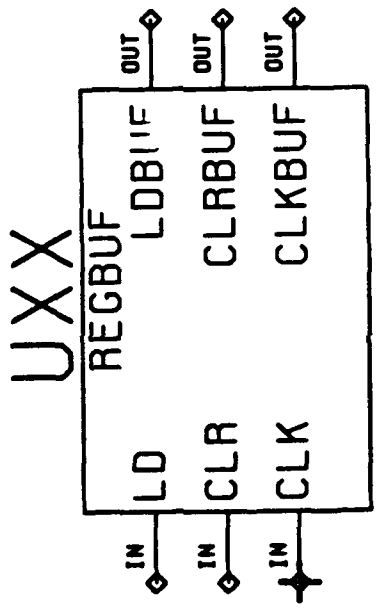

RAMUX
SELBBUF
SELABUF
SELA
Y (I)
SELABUF
A (5-I)
SELBBUF
B (I)
FOR I := 0 TO 5

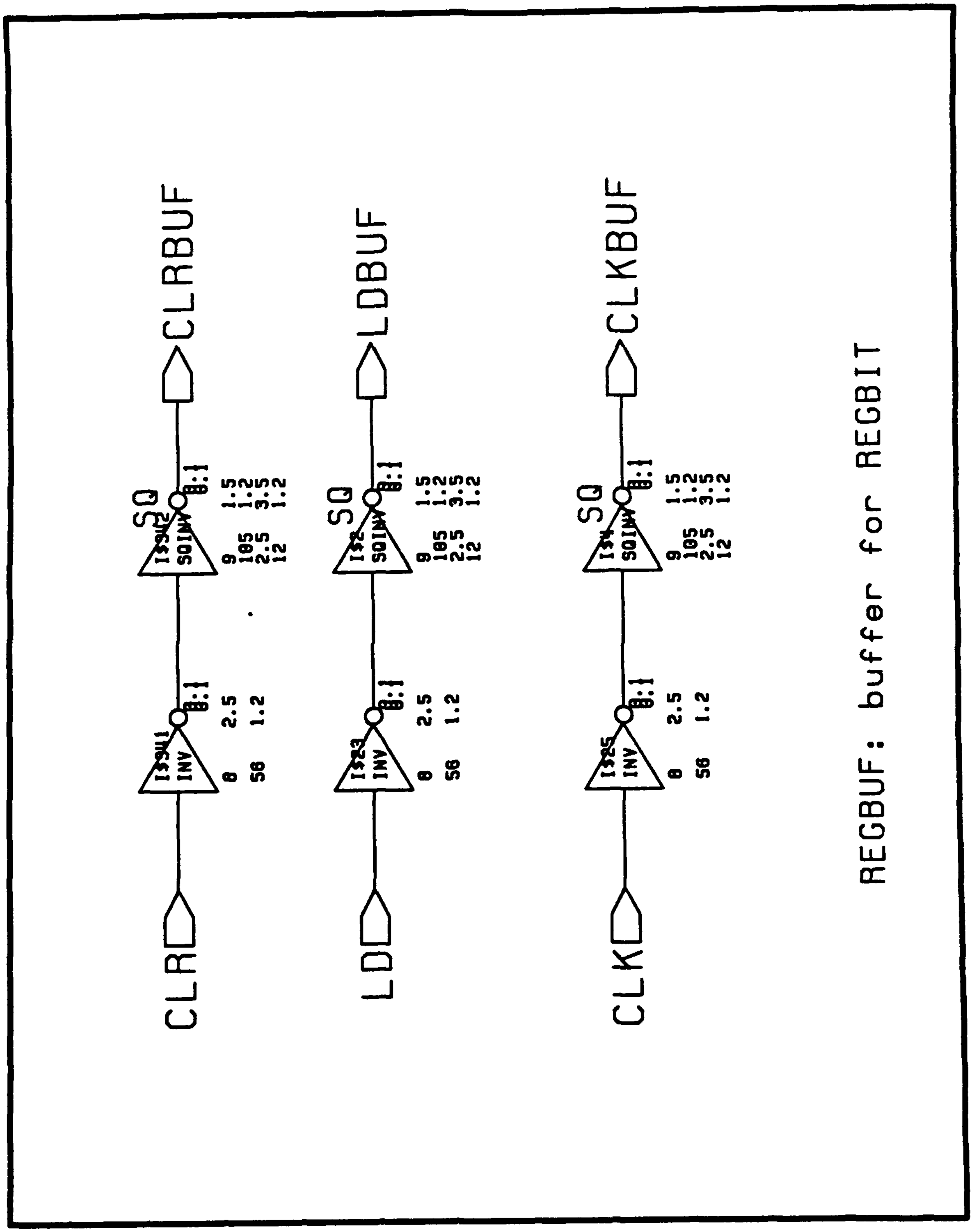

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: RCVR2
DESCRIPTION: LOW POWER 2 VOLT RECEIVER WITH PAD
OUT
0.5
0.3
1.4
1.4
1
0
SSS
01
IN
2
I1
I1
IO
CG
I#
O1
AND
RCVR2
CG
VTT

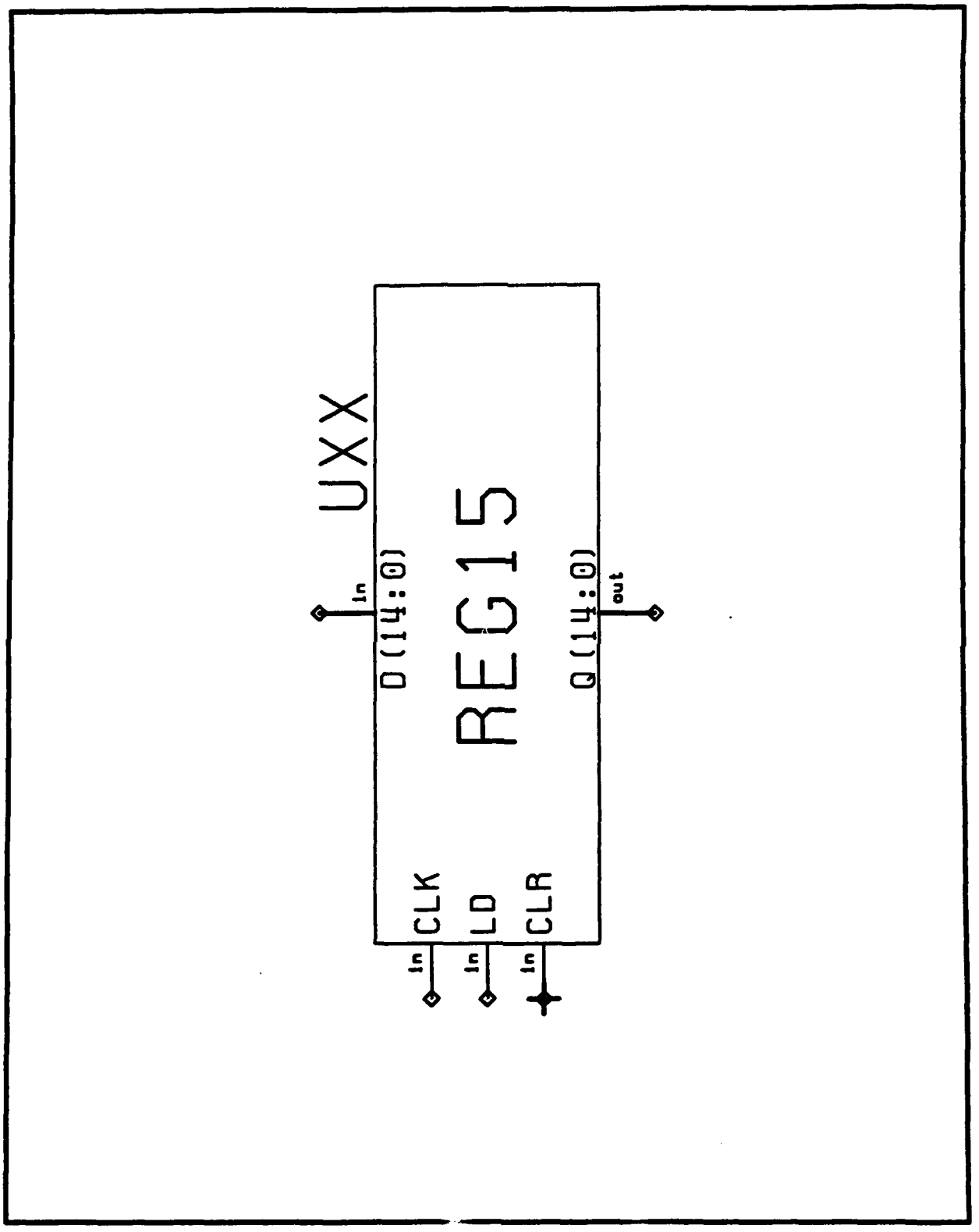

RCVR2
Revised 8/24/89
O1
I1
CC
VTT

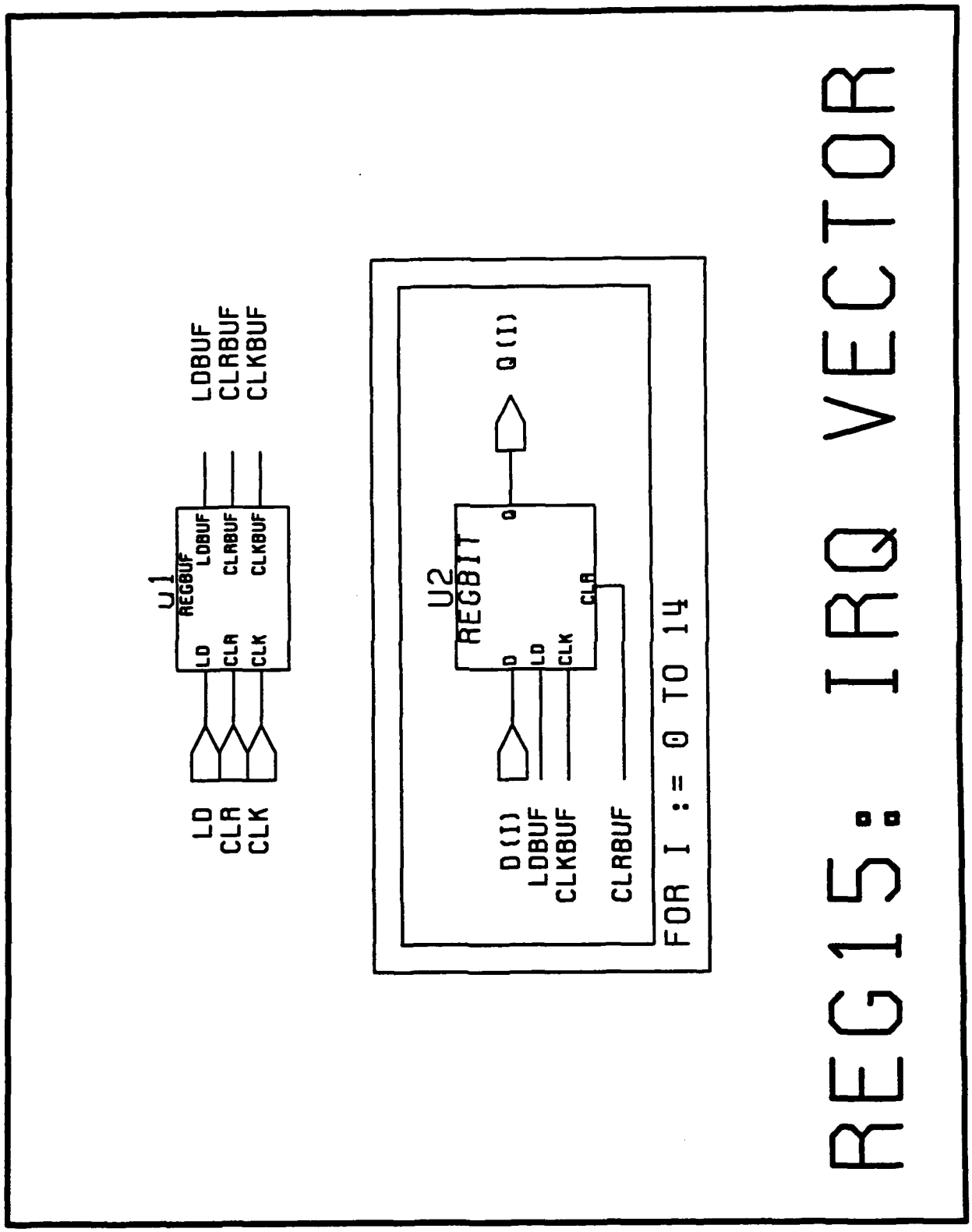

UXX
REGBIT
OUT
Q
CLR
NI
D
LD
CLK
IN
IN
IN

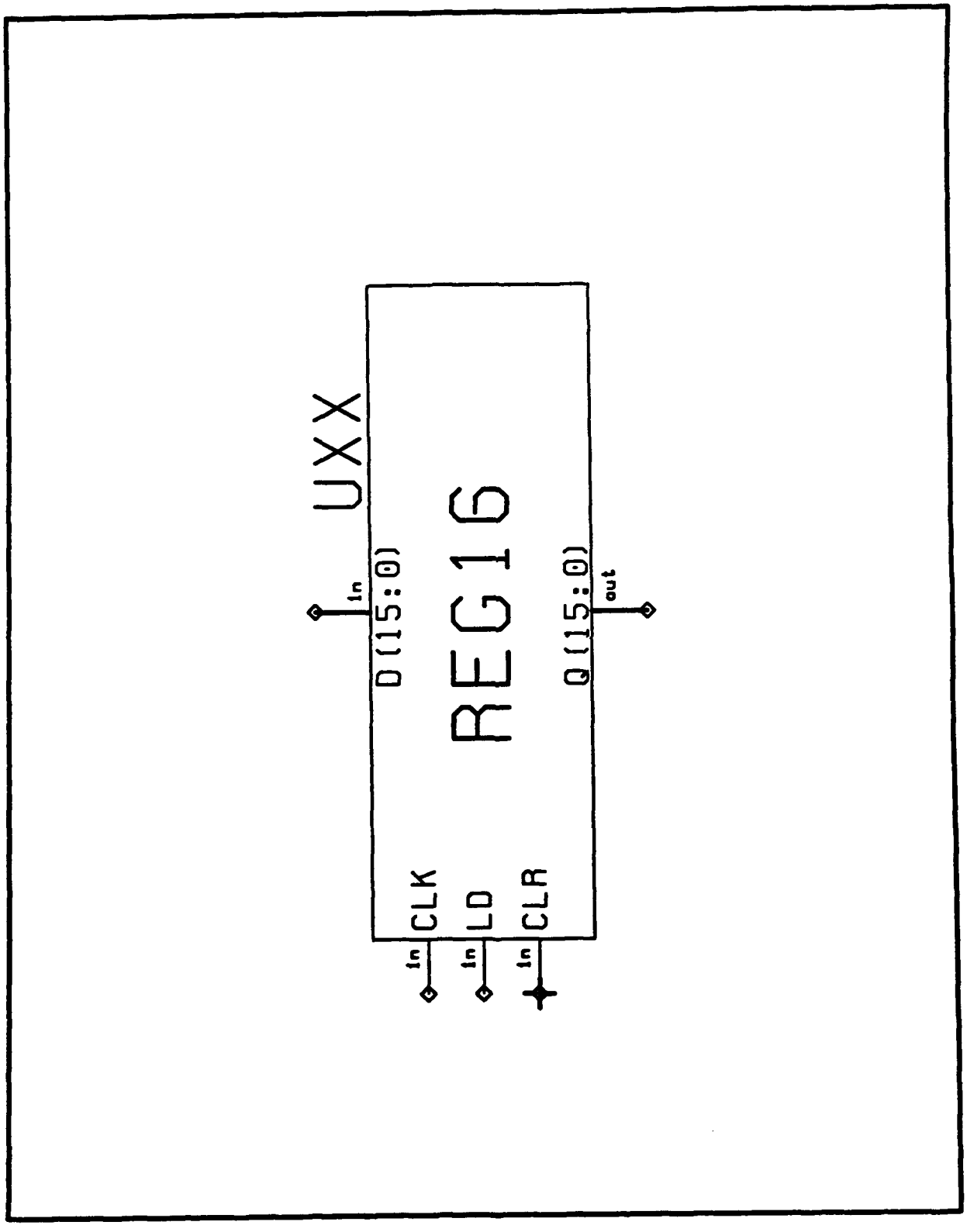

Q
SD
CLK
CLR
D
LD
REGBIT

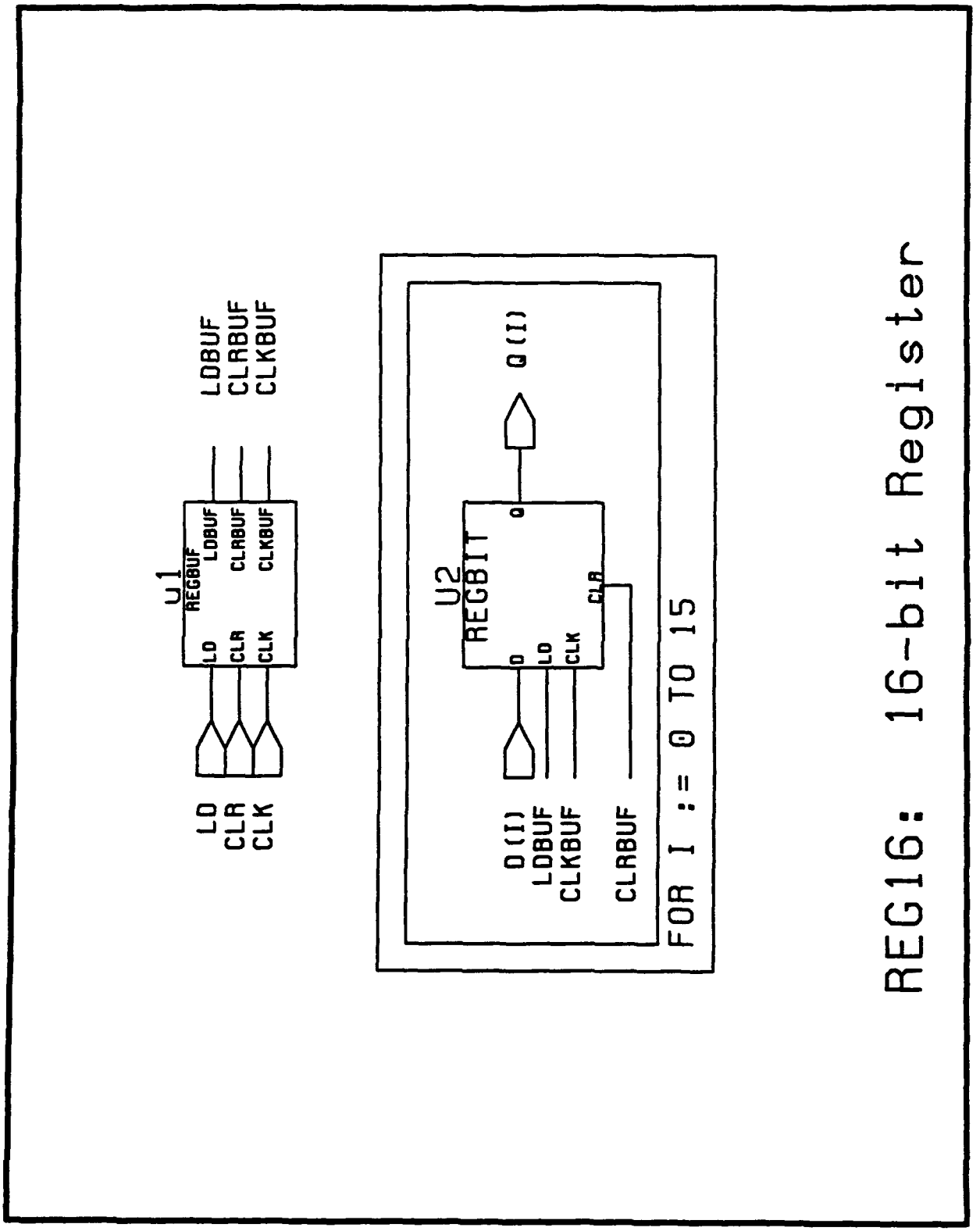

UXX
REGBUF
LDBUF
CLRBUF
CLKBUF
LD
CLR
CLK
IN
IN
IN
OUT
OUT
OUT

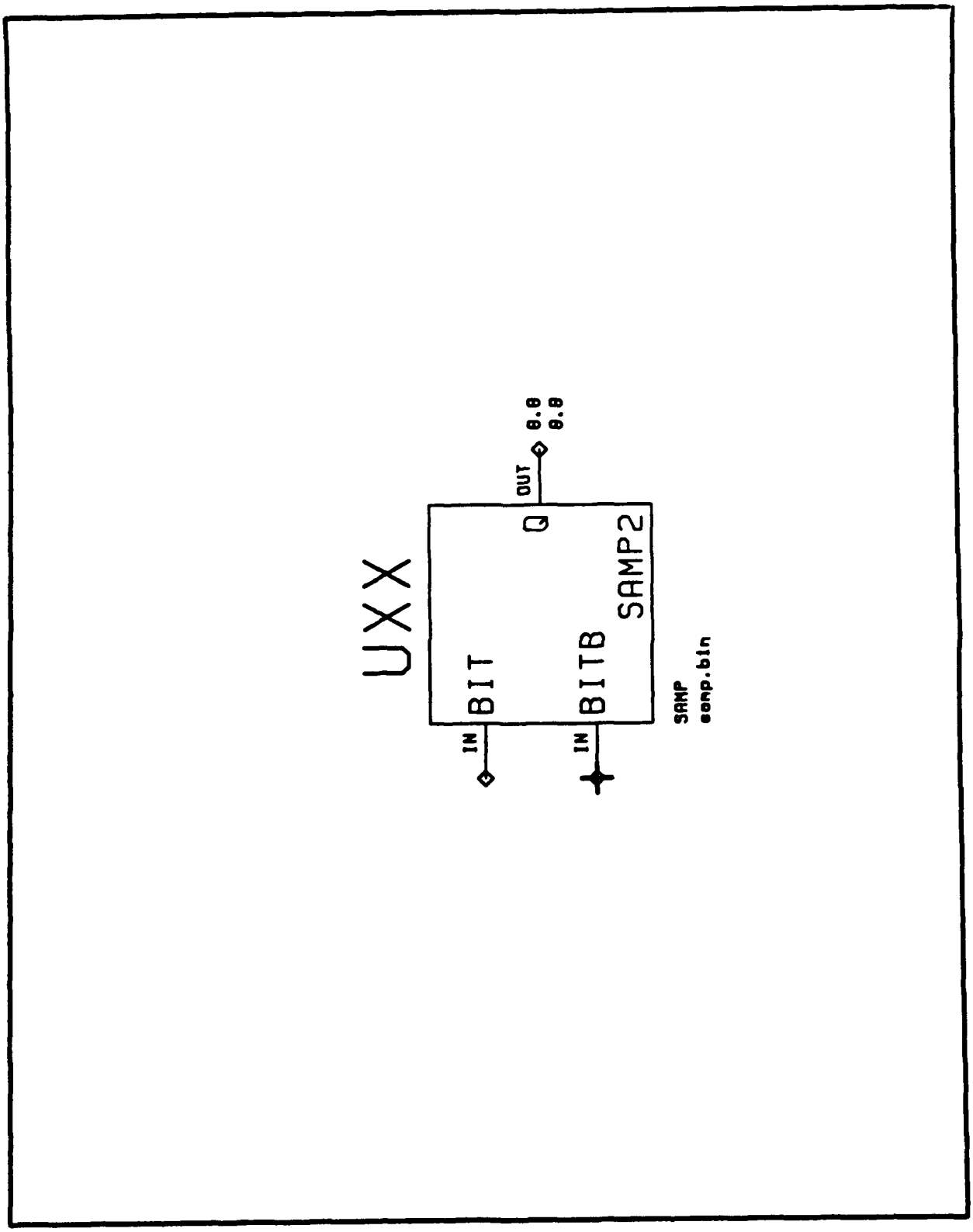

CLR
CLRBUF
LD
LDBUF
CLK
CLKBUF
INV
SQINV
SQ
REGBUF: buffer for REGBIT

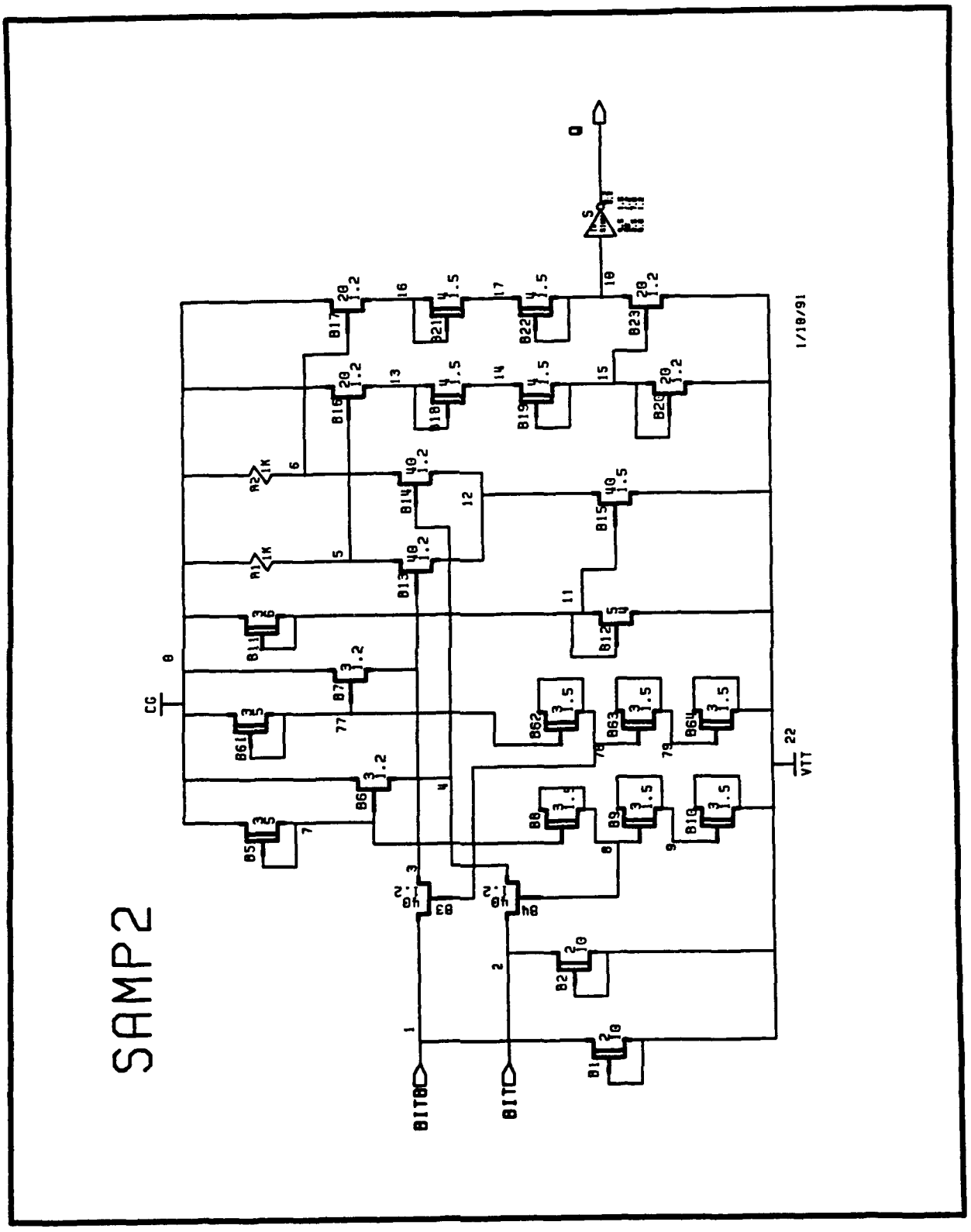

UXX
REG15
D(14:0)
Q(14:0)
in
out
CLK
LD
CLR
in
in
in

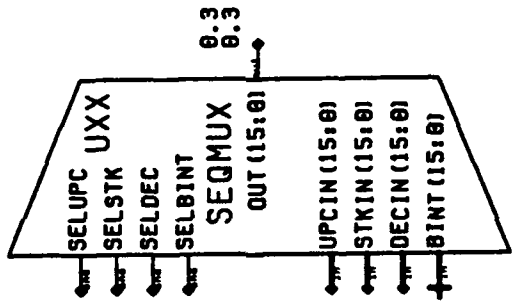

REG15: IRQ VECTOR
FOR I := 0 TO 14
U2
REGBIT
D
Q
CLR
D(I)
LDBUF
CLKBUF
CLRBUF
Q(I)
U1
REGBUF
LDBUF
CLRBUF
CLKBUF
LD
CLR
CLK
LDBUF
CLRBUF
CLKBUF

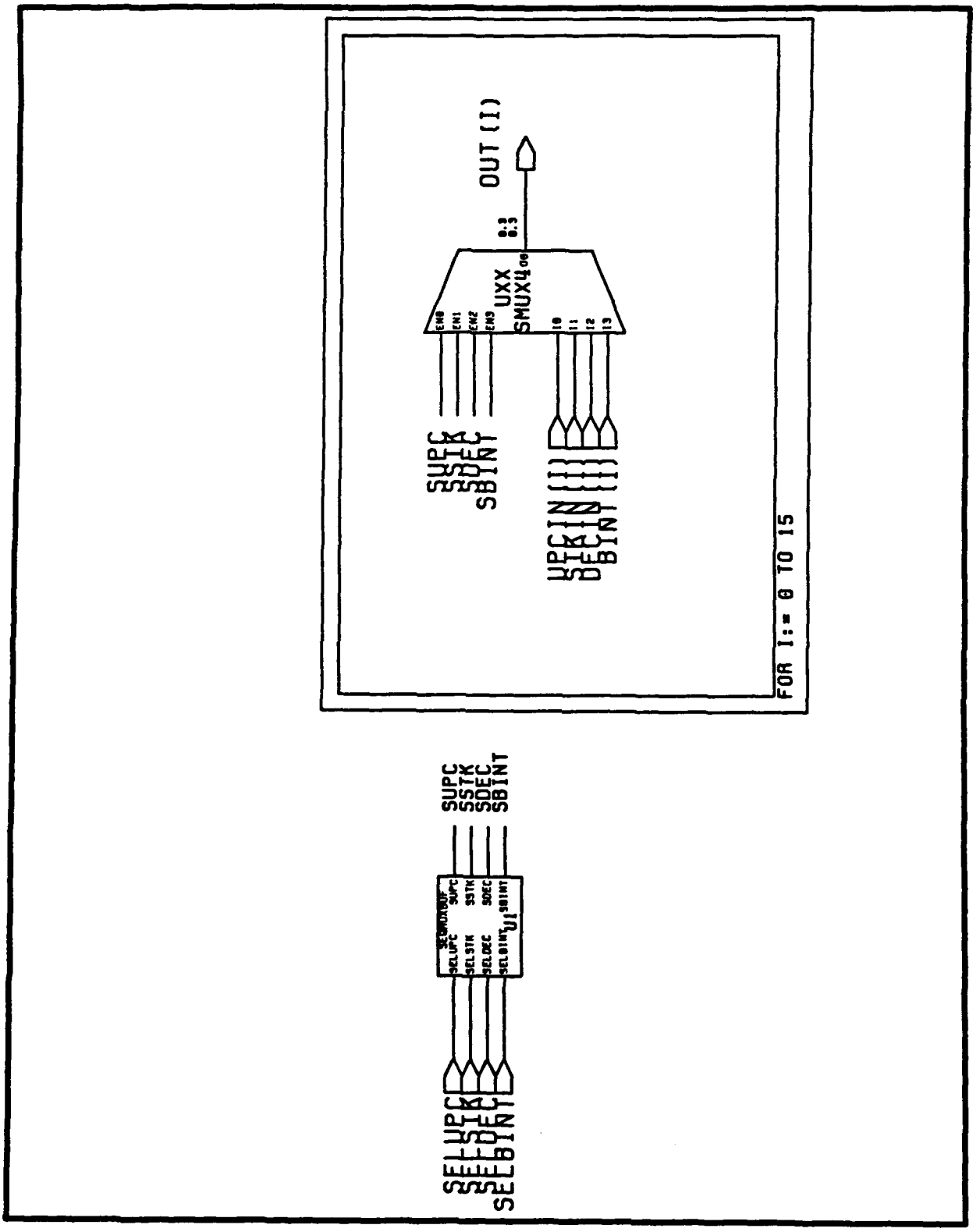

UXX
REG16
D(15:0)
Q(15:0)
in
out
CLK
LD
CLR
in
in
in

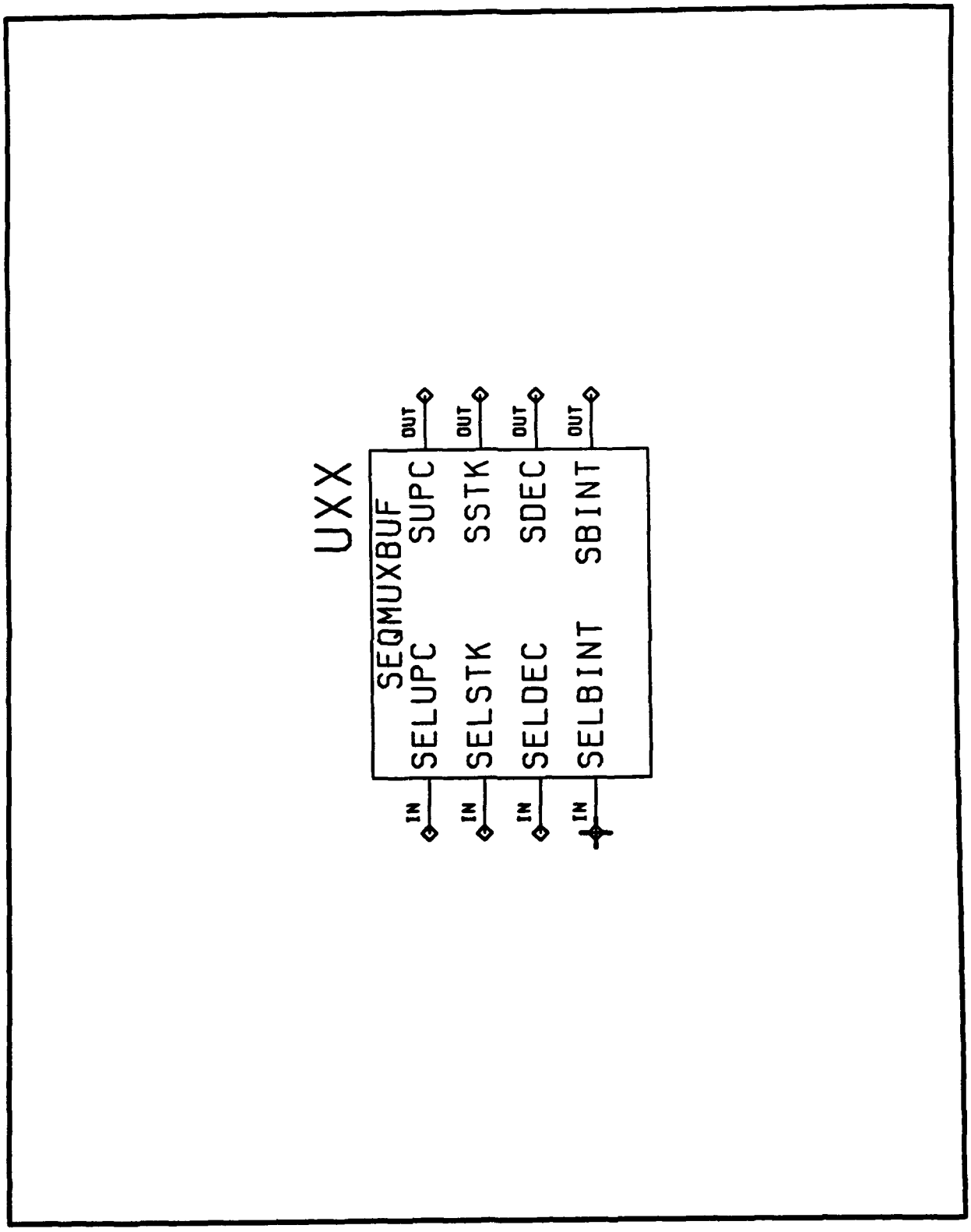

REG16: 16-bit Register
FOR I := 0 TO 15
U2
REGBIT
D(I)
LDBUF
CLKBUF
CLRBUF
Q(I)
U1
REGBUF
LDBUF
CLRBUF
CLKBUF
LD
CLR
CLK

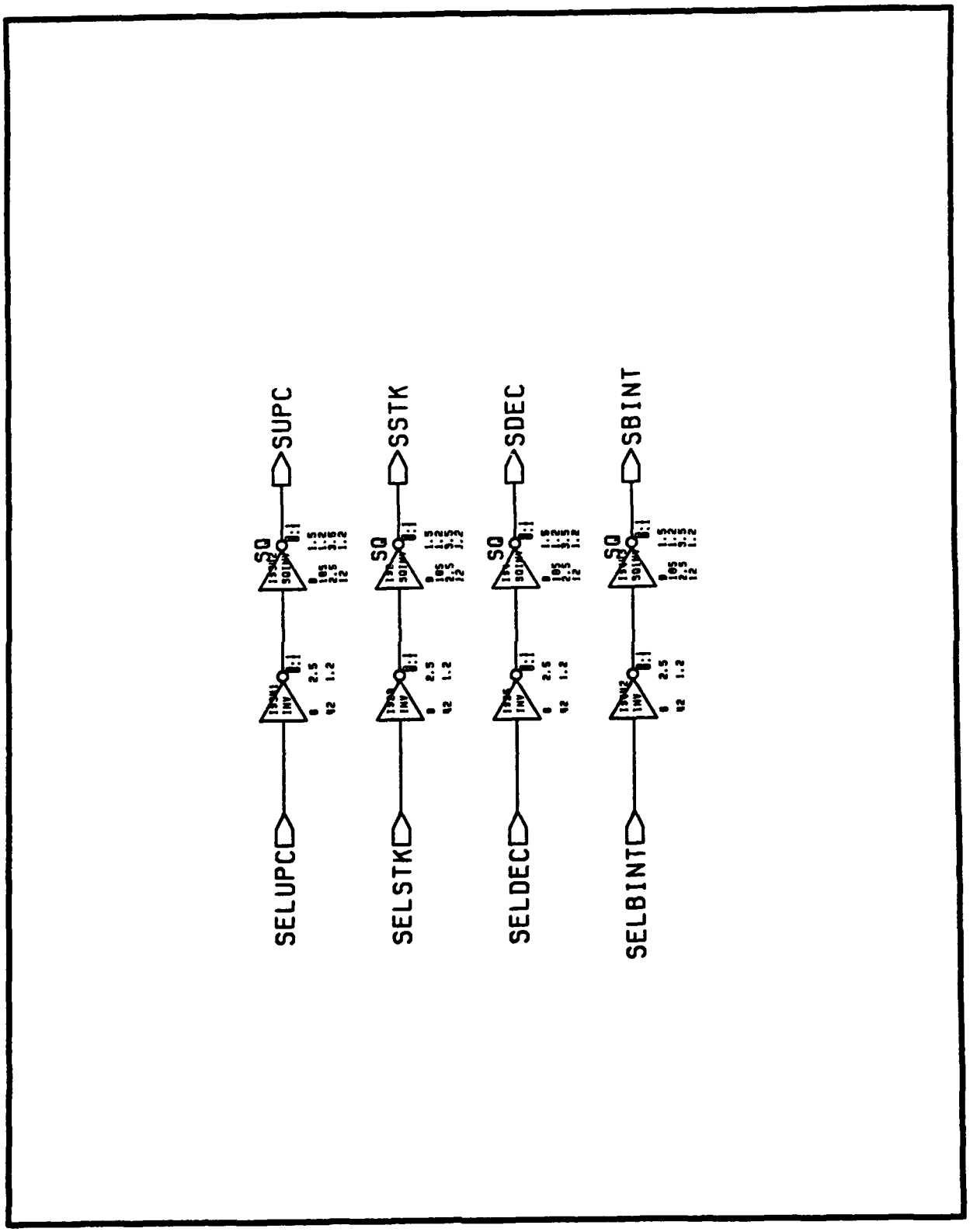

UXX
BIT
BITB
SAMP2
Q
OUT
IN
IN
0.0
0.0
SAMP
samp.bin

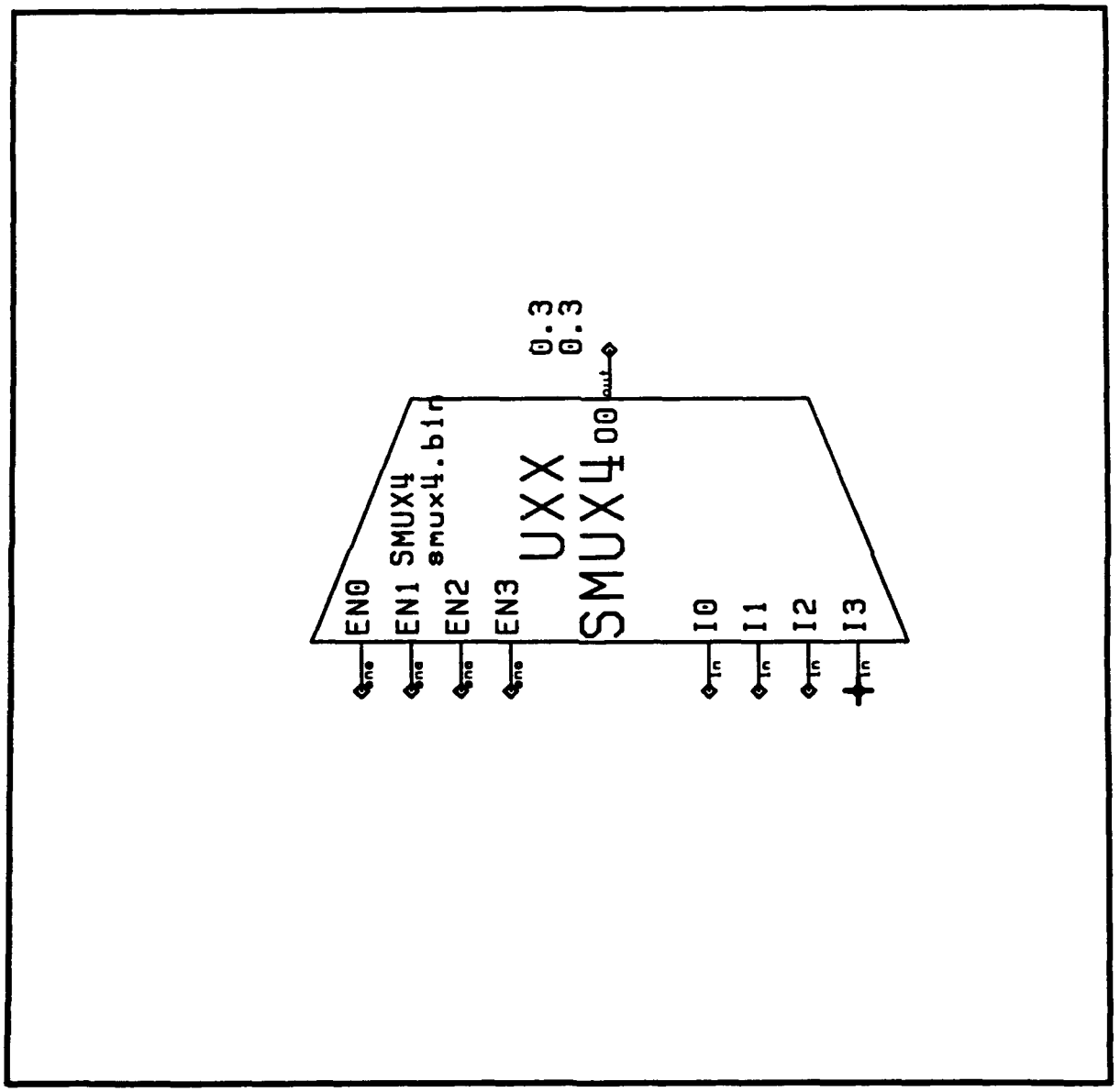

SAMP2
1/18/91
CG
VTT
BITB
BIT

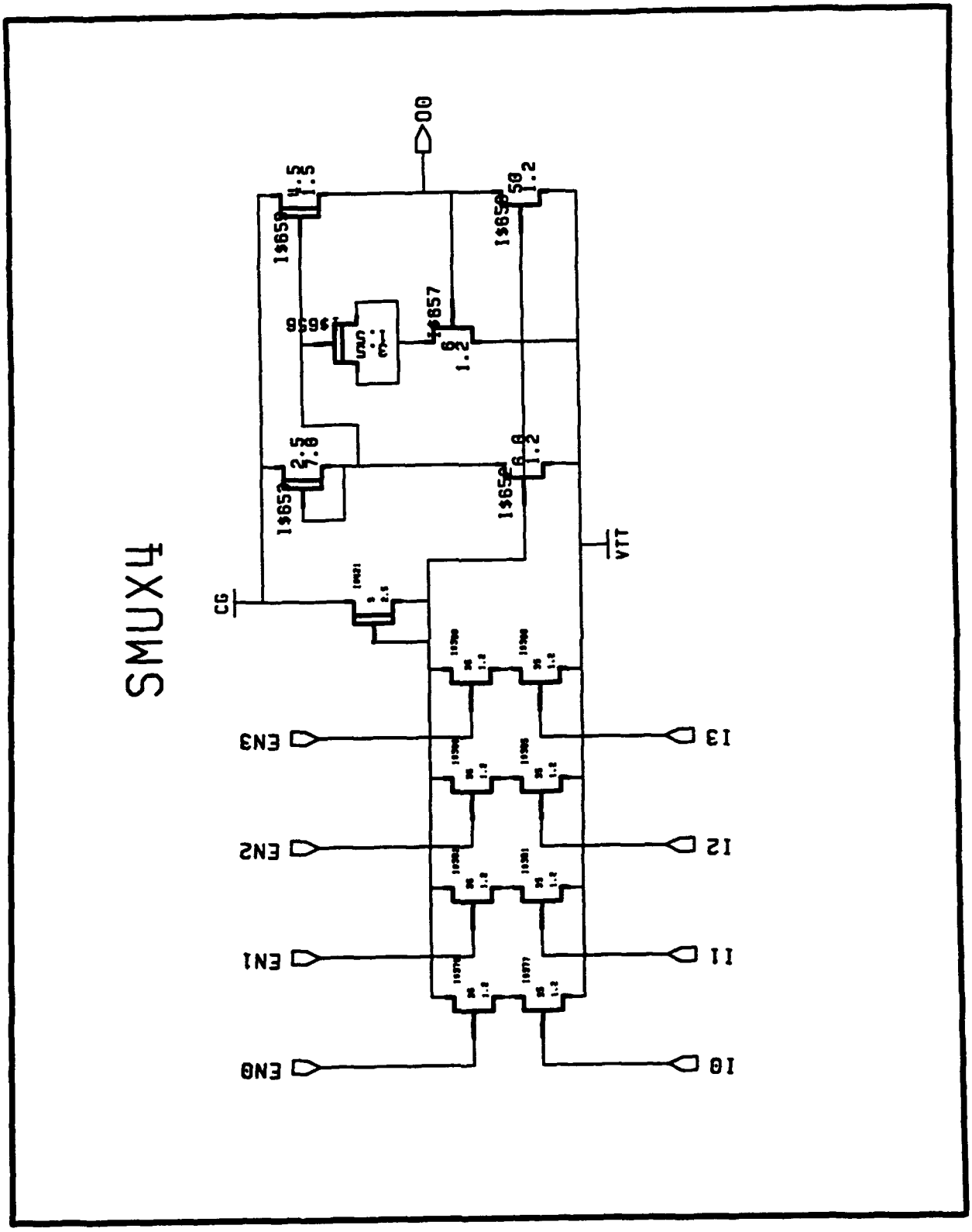

0.3
0.3
UXX
SEQMUX
SELUPC
SELSTK
SELDEC
SELBINT
OUT(15:0)
UPCIN(15:0)
STKIN(15:0)
DECIN(15:0)
BINT(15:0)

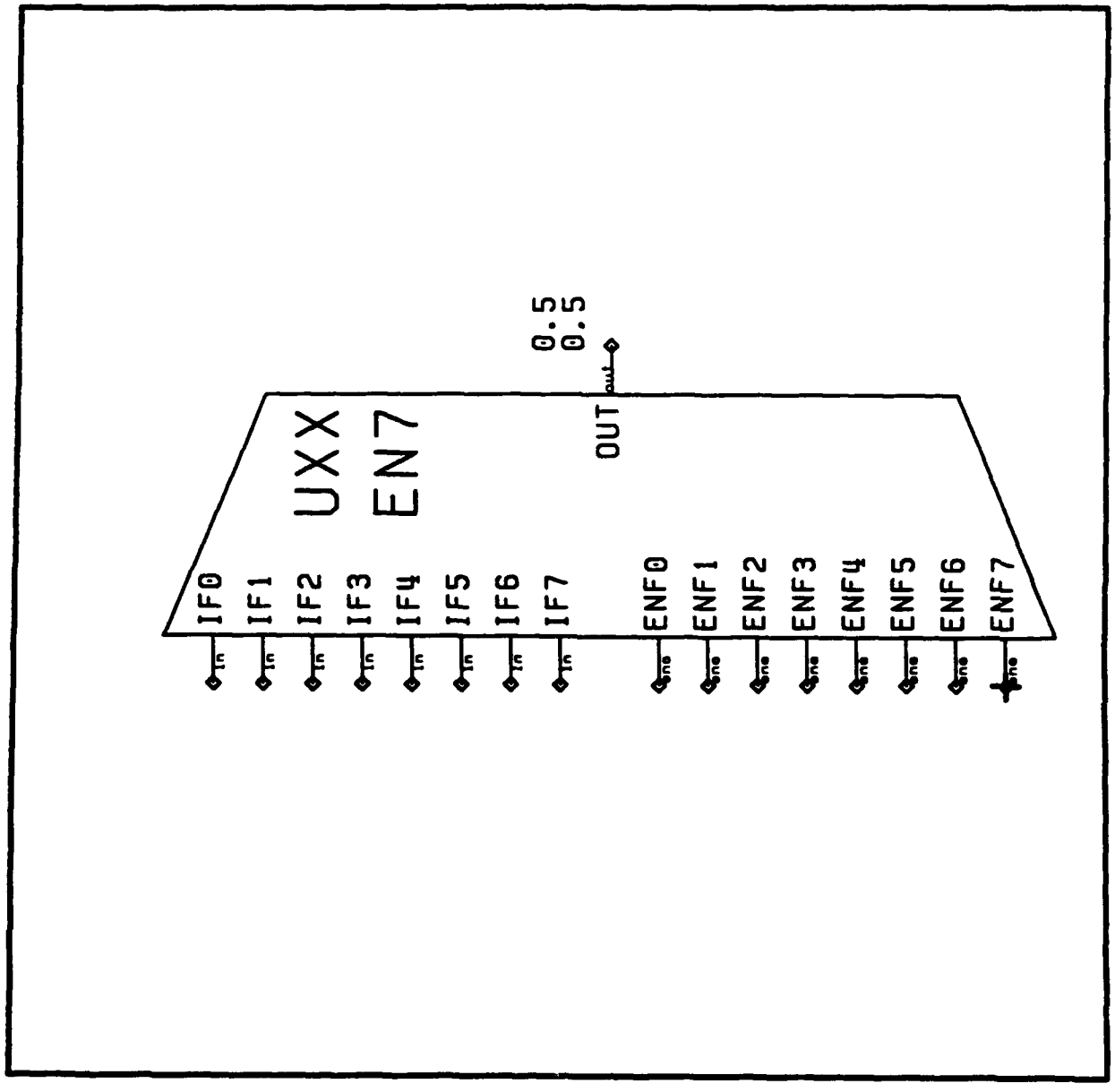

OUT (I)
8:3
UXX
SMUX4
EN0
EN1
EN2
EN3
I0
I1
I2
I3
SUPC
SSTK
SDEC
SBINT
UPCIN
STKIN
DECIN
BINT
FOR I:= 0 TO 15
SUPC
SSTK
SDEC
SBINT
SELUPC
SELSTK
SELDEC
SELBINT

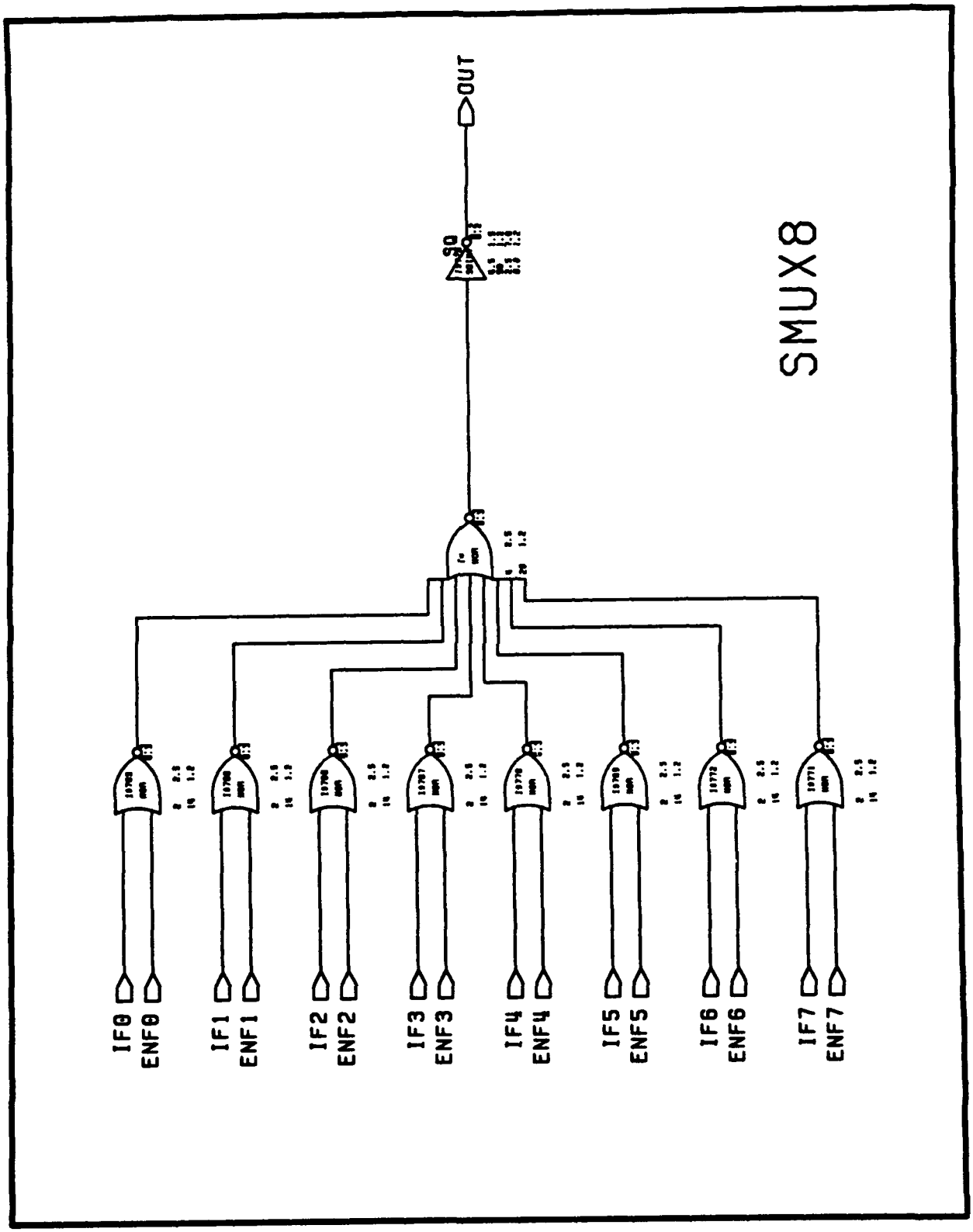

UXX
SEQMUXBUF
SELUPC
SELSTK
SELDEC
SELBINT
SUPC
SSTK
SDEC
SBINT
OUT
OUT
OUT
OUT
IN
IN
IN
IN

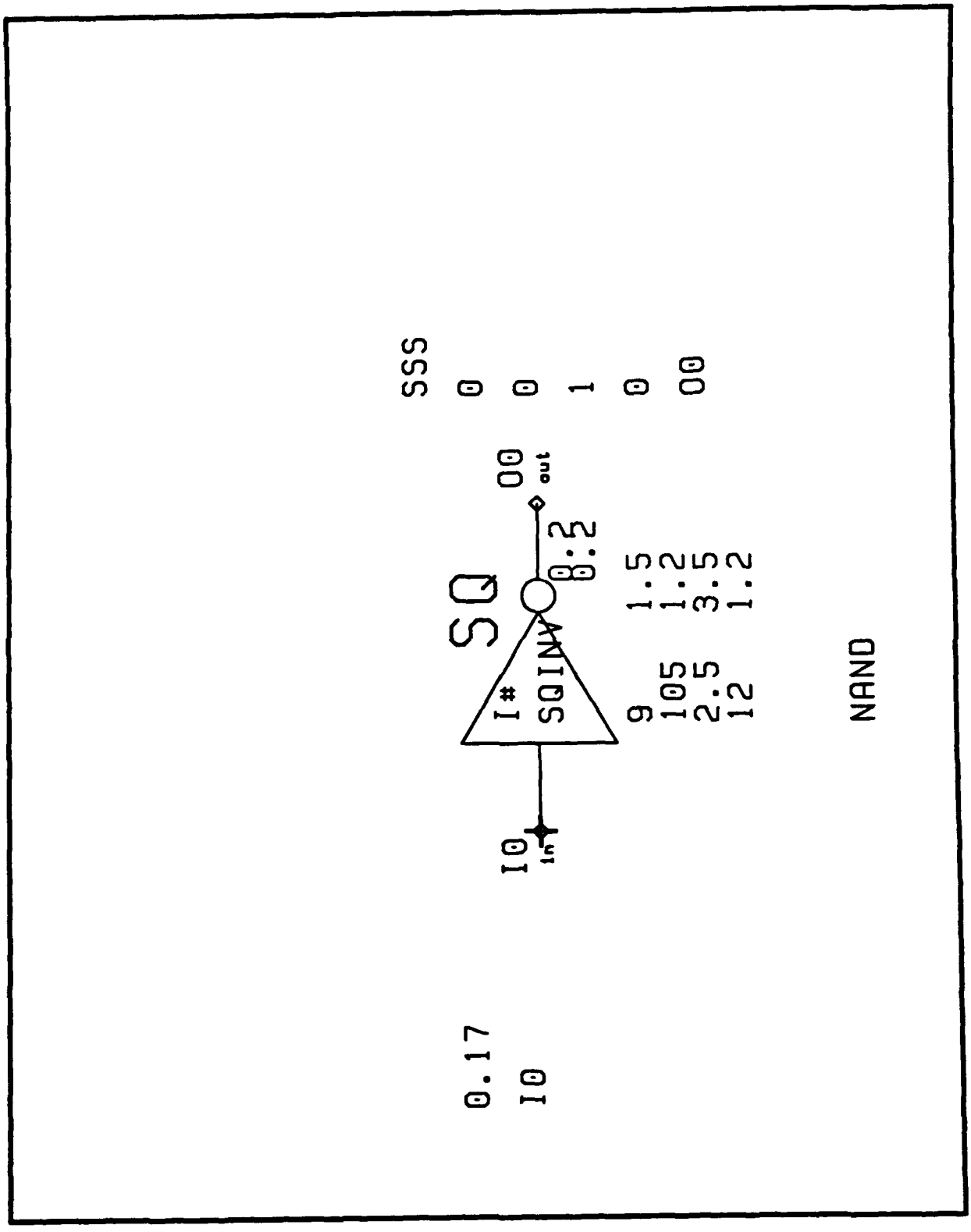

SUPC
SSTK
SDEC
SBINT
SELUPC
SELSTK
SELDEC
SELBINT

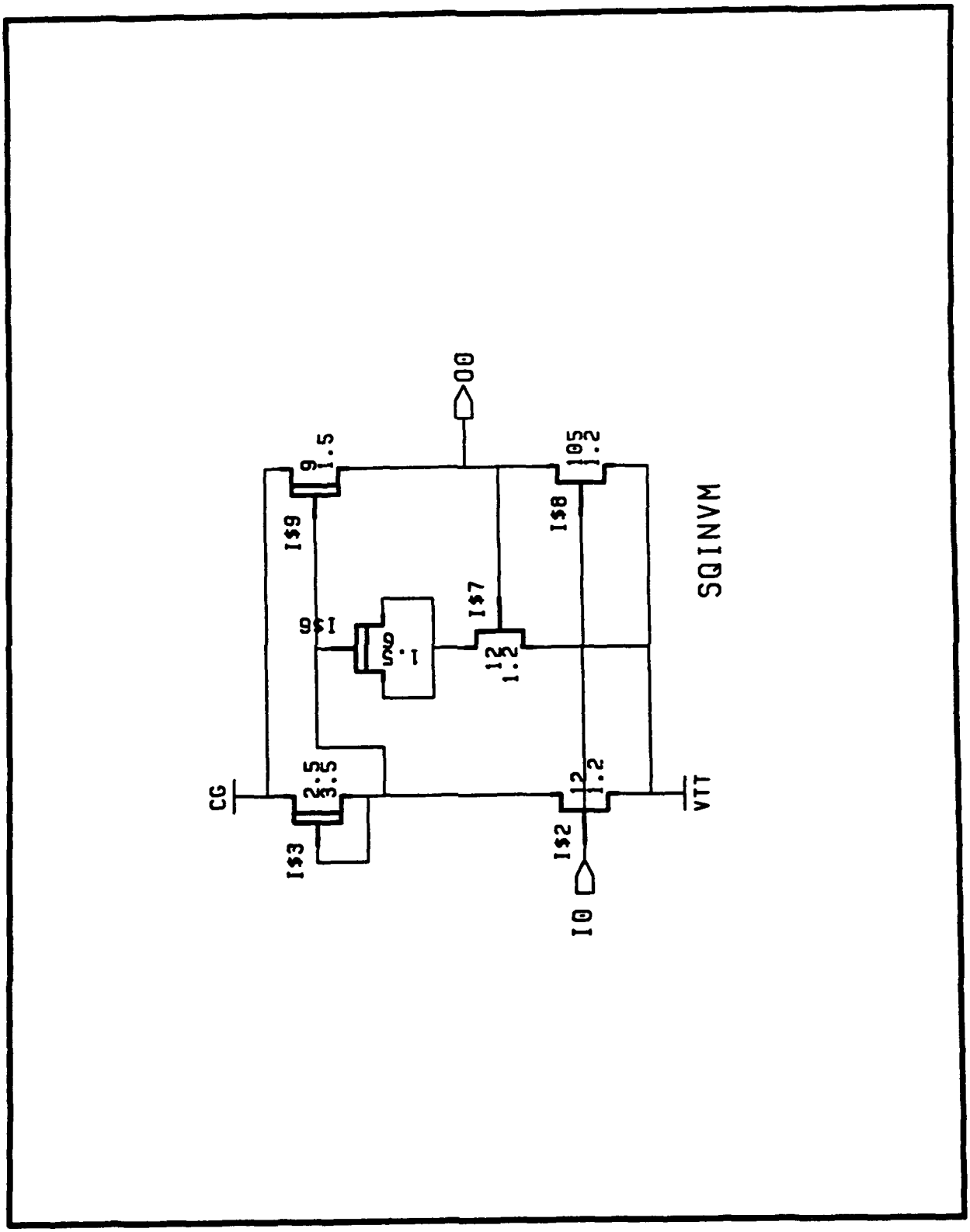

0.3
0.3
EN0
EN1
EN2
EN3
SMUX4
smux4.bin
UXX
SMUX4
I0
I1
I2
I3

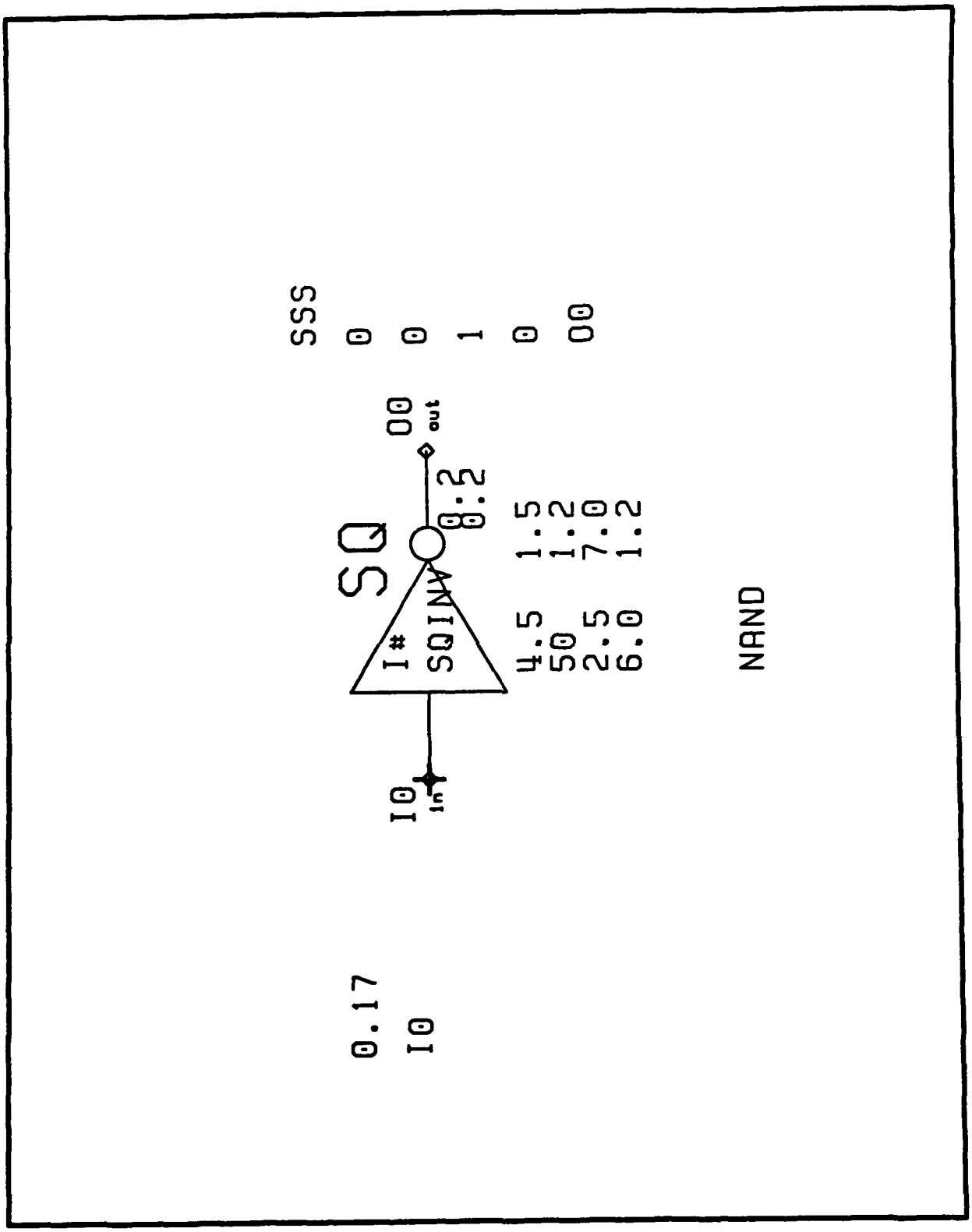

SMUX4
OO
4.5
1.5
50
1.2
6.0
1.2
2.5
7.8
6.0
1.2
VTT
CG
EN3
EN2
EN1
EN0
I3
I2
I1
I0

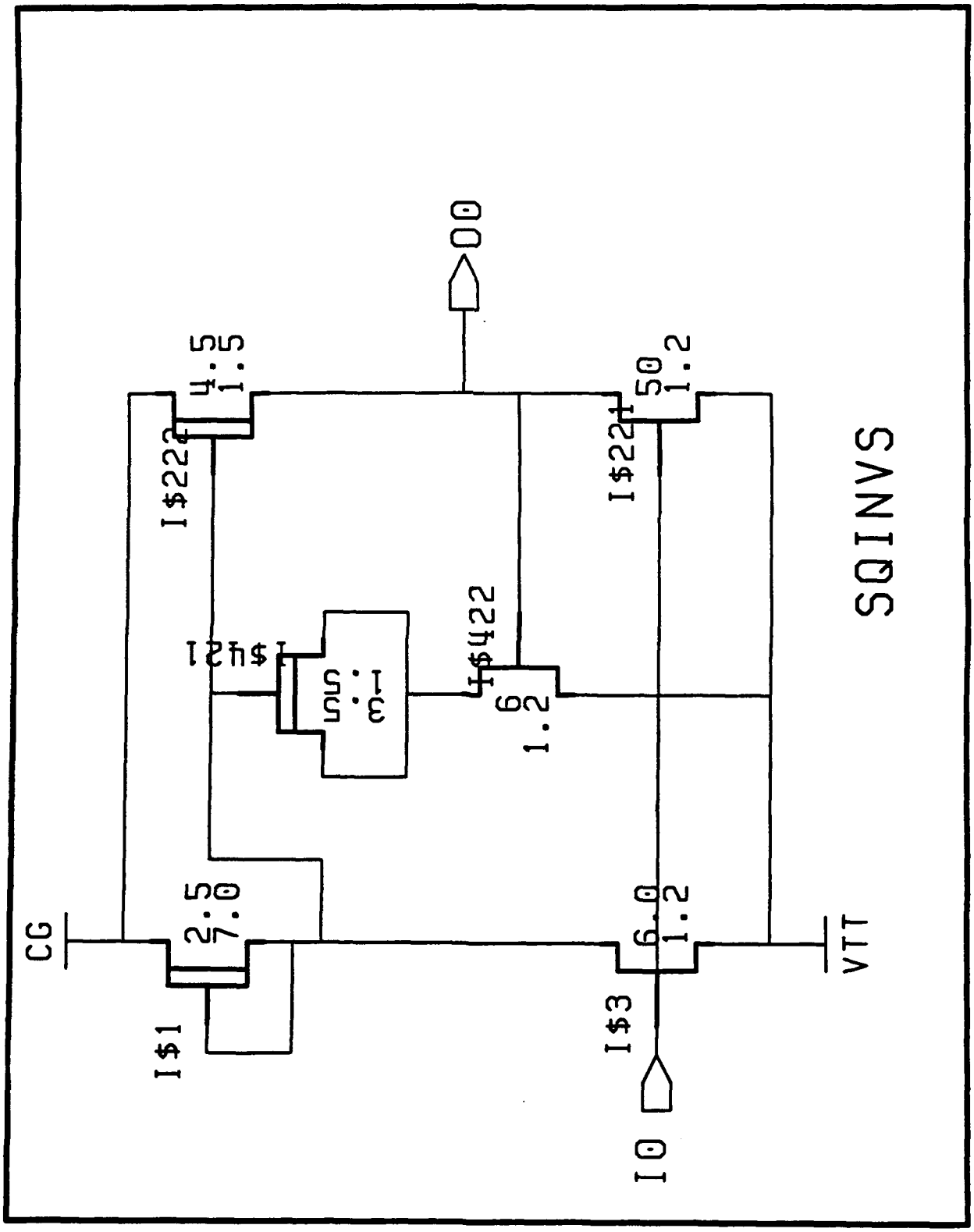

0.5
0.5
OUT
UXX
EN7
IF0
IF1
IF2
IF3
IF4
IF5
IF6
IF7
ENF0
ENF1
ENF2
ENF3
ENF4
ENF5
ENF6
ENF7

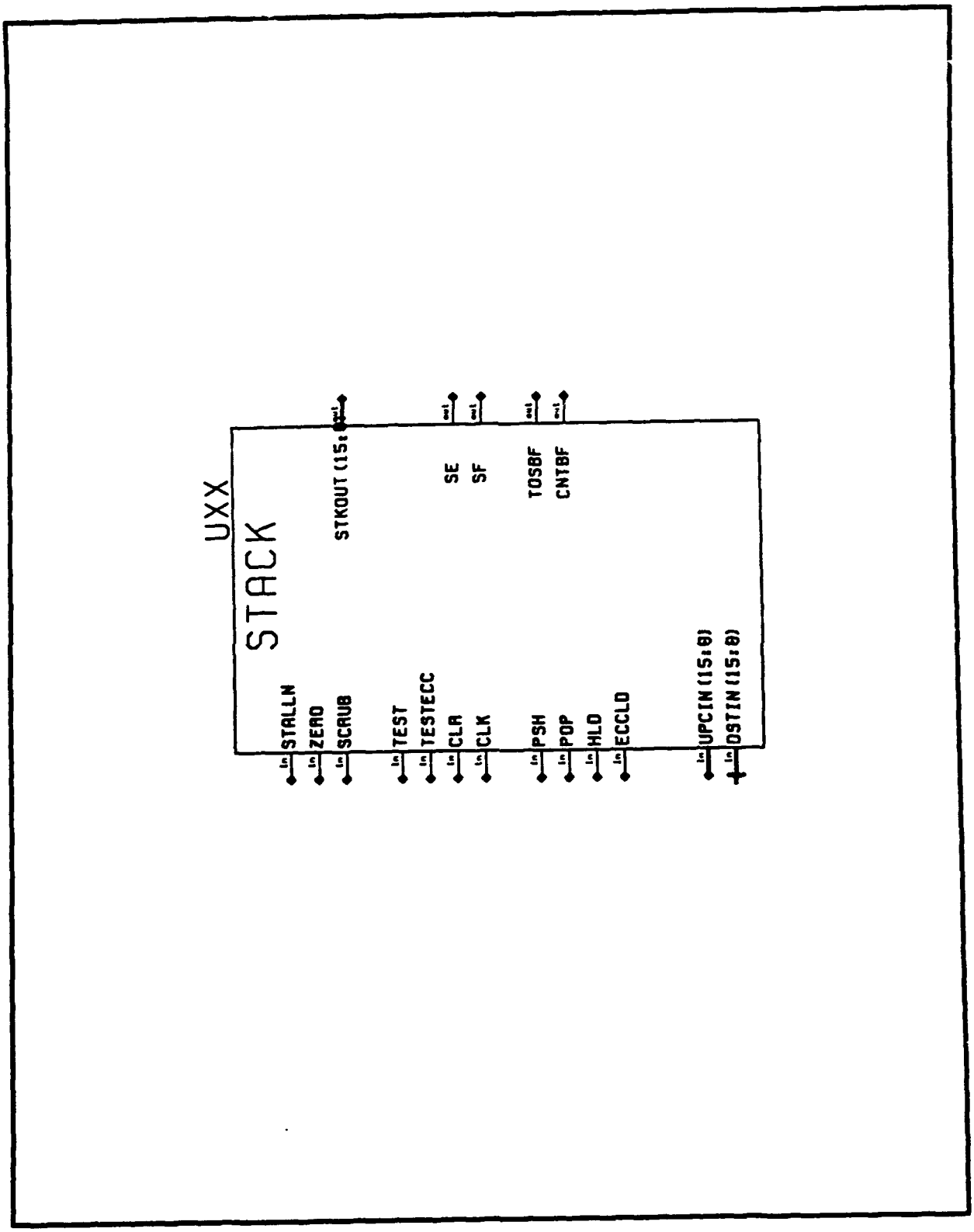

SMUX8
OUT
S0
IF0
ENF0
IF1
ENF1
IF2
ENF2
IF3
ENF3
IF4
ENF4
IF5
ENF5
IF6
ENF6
IF7
ENF7

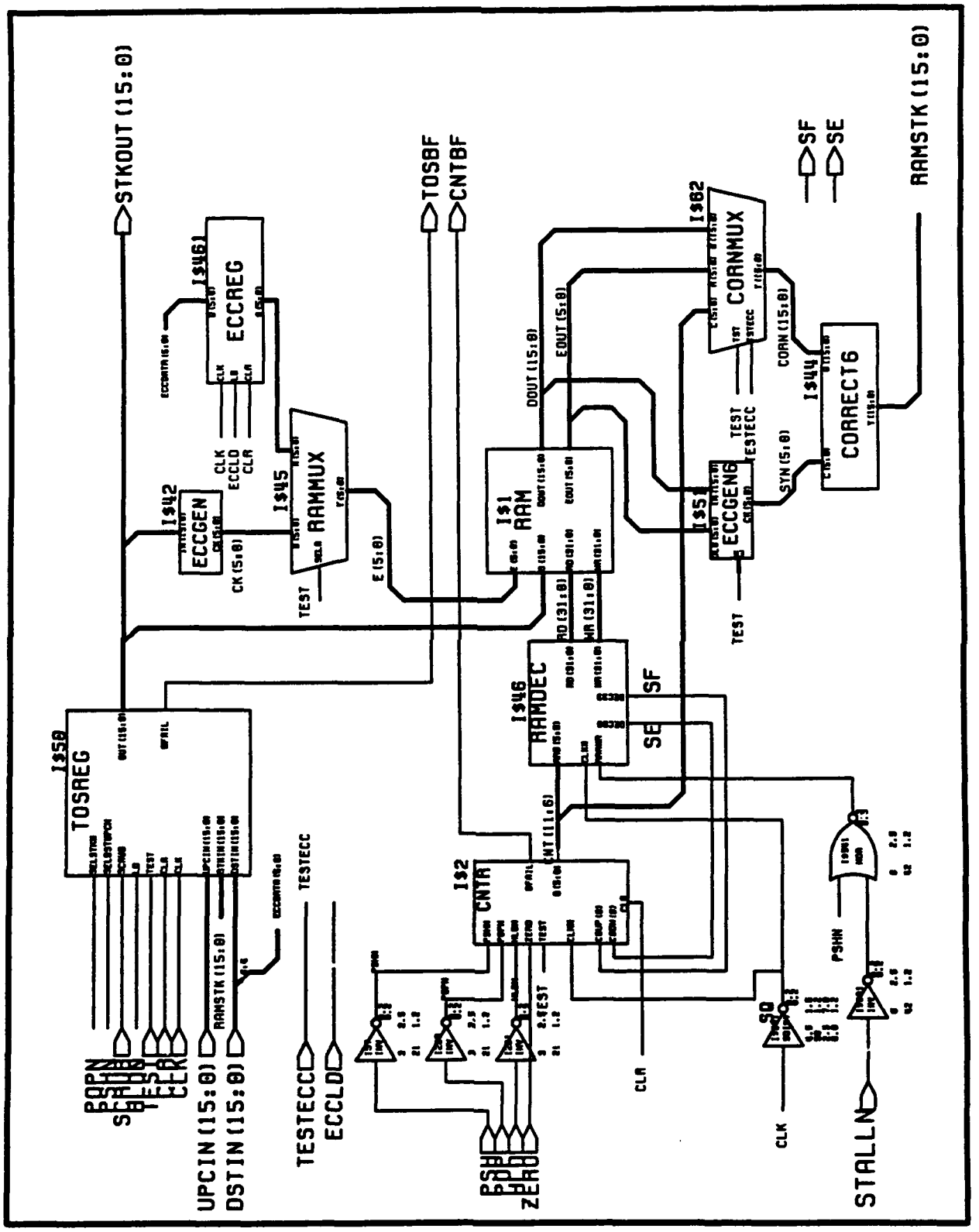

SSS
0 0 1 0 00
00
out
8.2
SQ
I#
SQINV
1.5
1.2
3.5
1.2
9
105
2.5
12
NAND
I0
in
0.17
I0

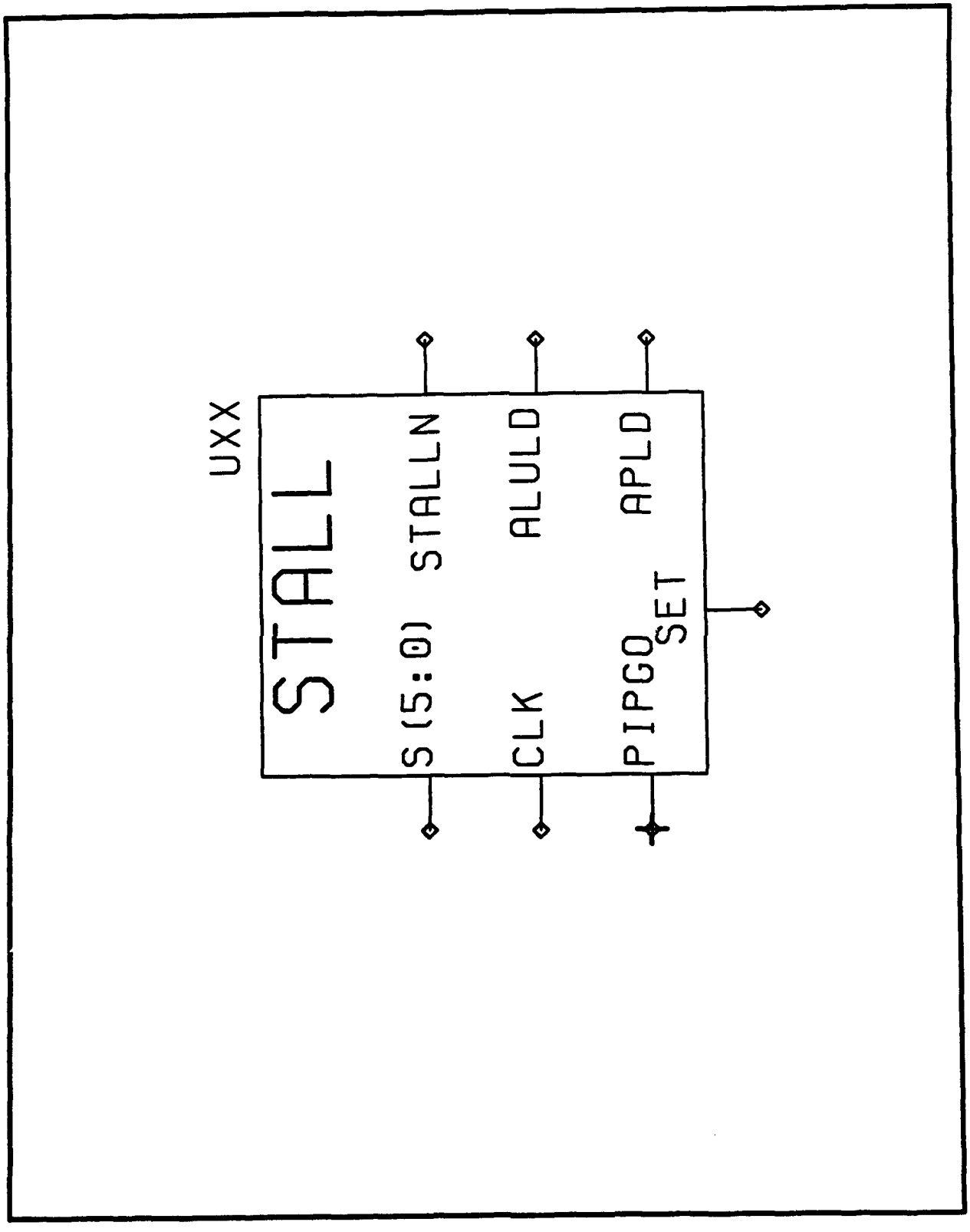

OD
I$5
I$8
I$9
I$7
I$1
I$6
I$3
I$2
CG
VTT
IO
SQINVM

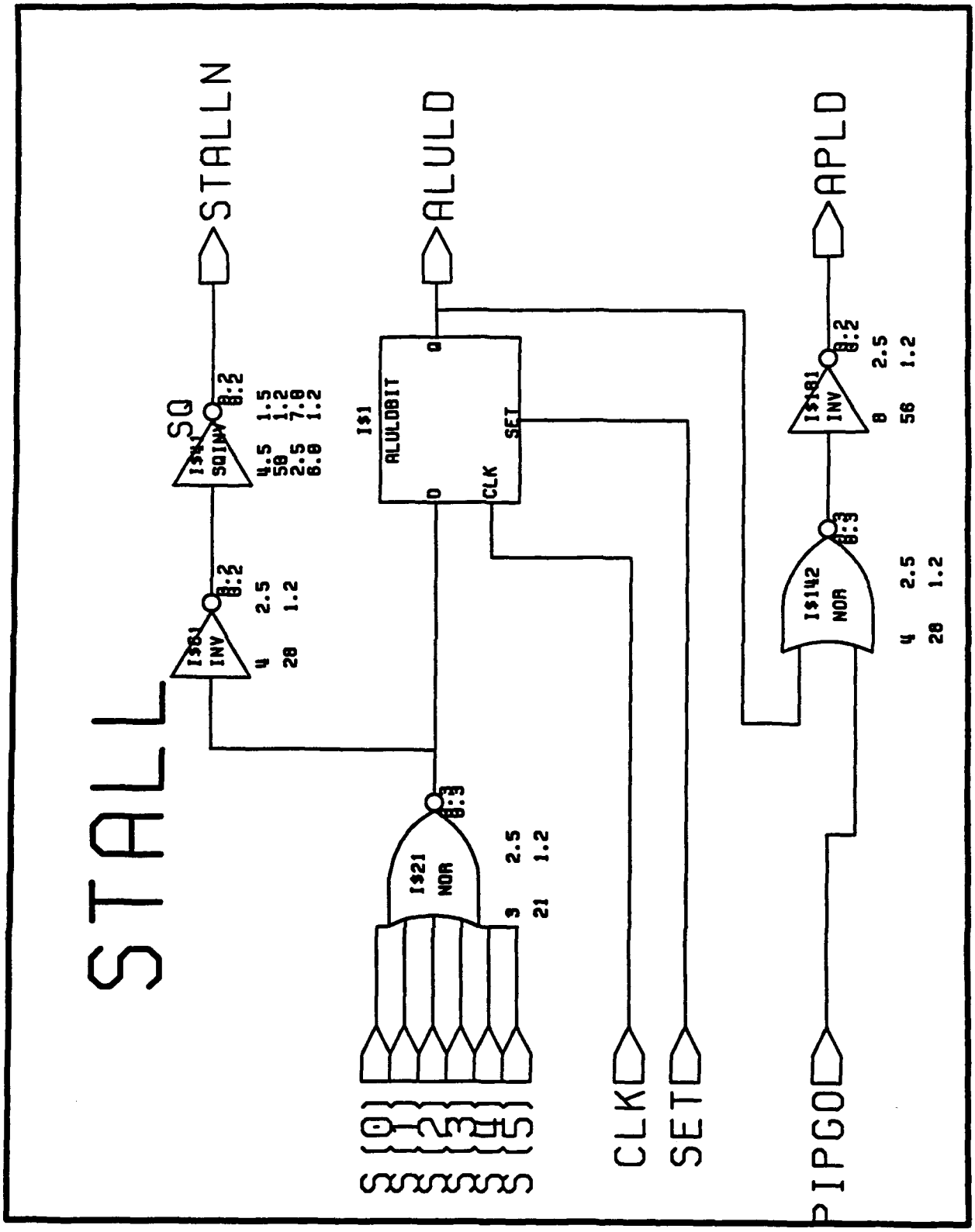

SSS
0 0 1 0 00
00
out
8.2
SQ
I#
SQINV
4.5 1.5
50 1.2
2.5 7.0
6.0 1.2
NAND
IO
in
0.17
IO

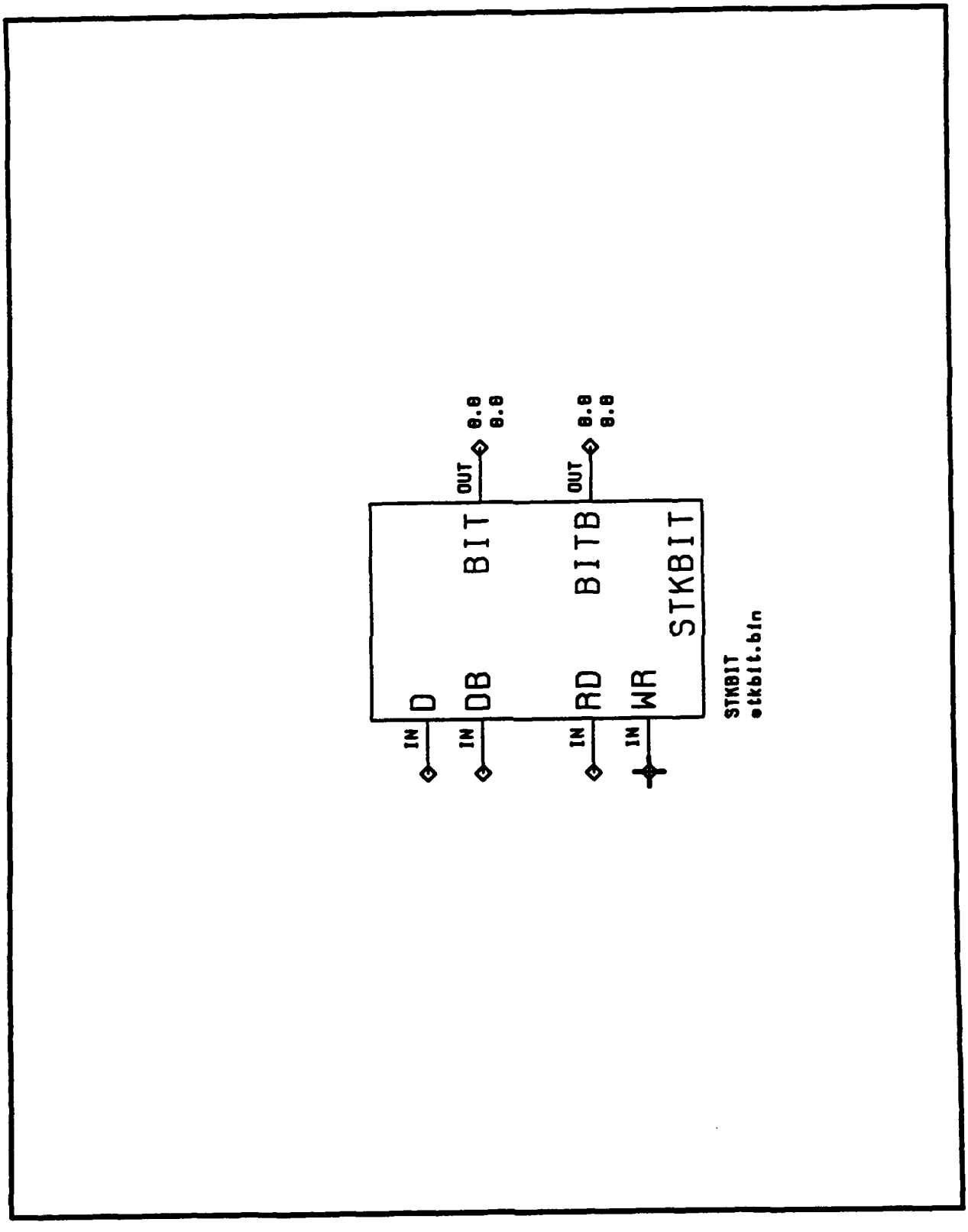

SQINVS
O0
4.5
1.5
I$222
50
1.2
I$221
I$421
3.5
1.5
I$422
6
1.2
CG
2.5
7.0
I$1
6.0
1.2
I$3
VTT
IO

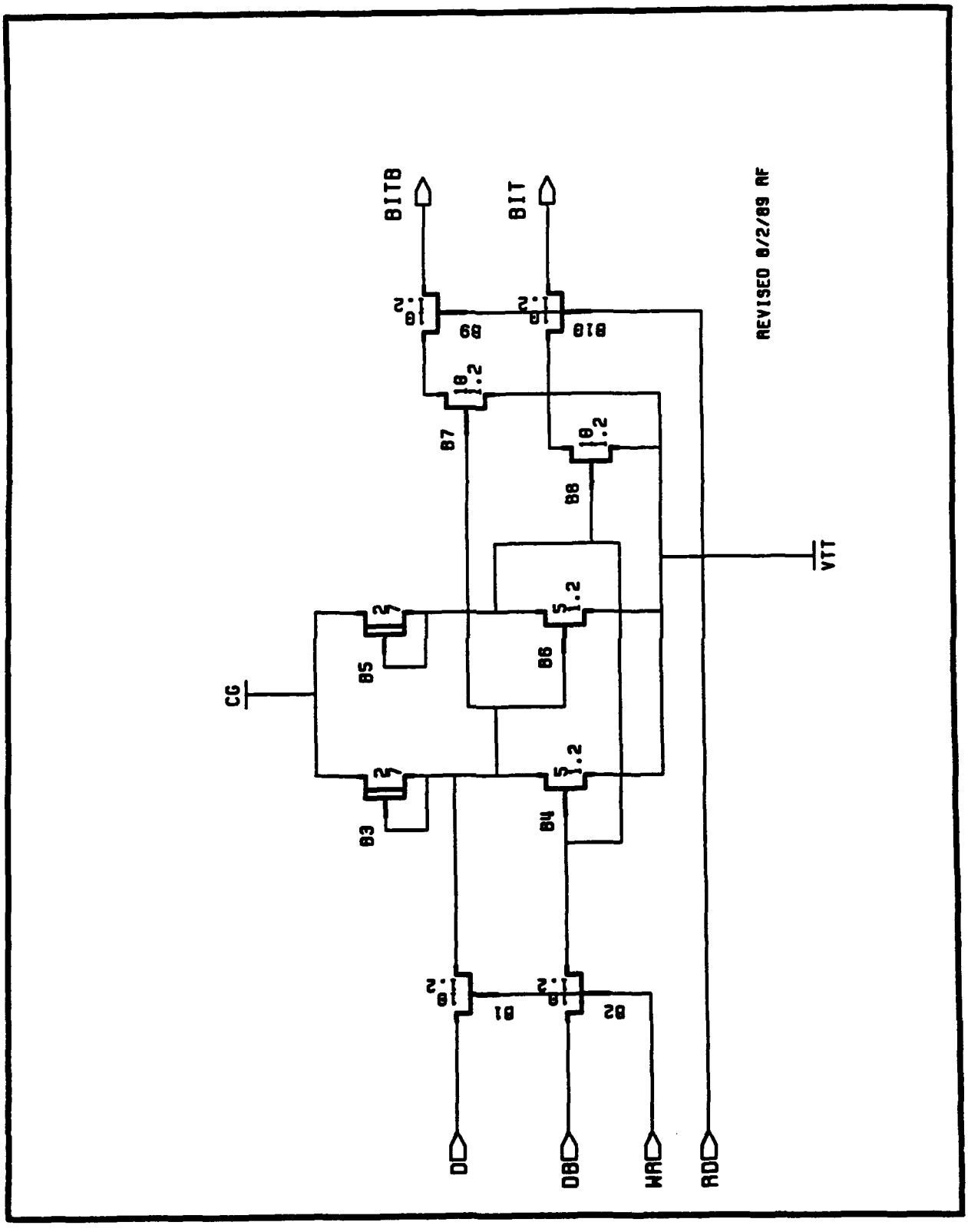

UXX
STACK
STKOUT (15:0)
SE
SF
TOSBF
CNTBF
STALLN
ZERO
SCRUB
TEST
TESTECC
CLR
CLK
PSH
POP
HLD
ECCLD
UPCIN (15:0)
DSTIN (15:0)

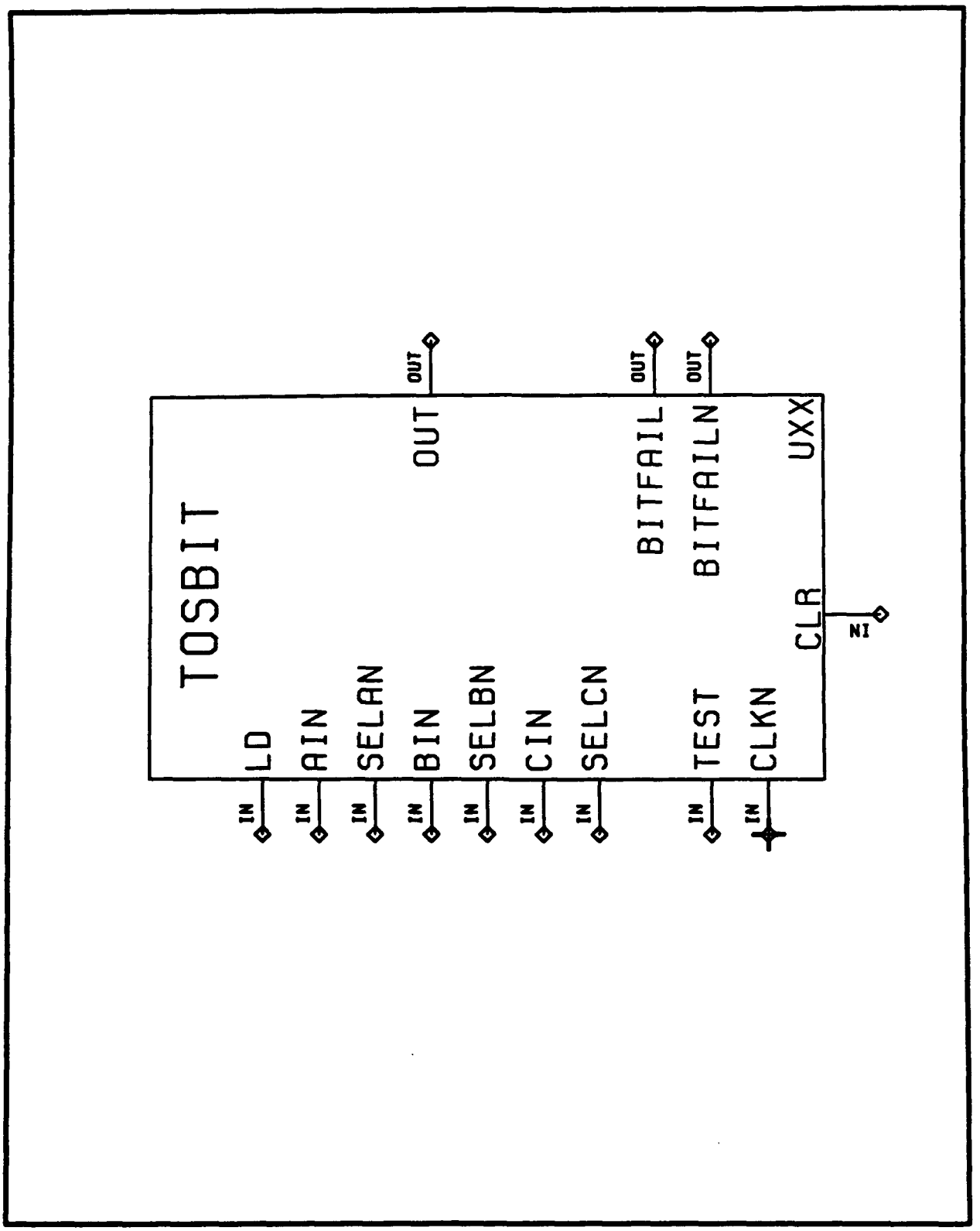

STKOUT(15:0)
TOSBF
CNTBF
SF
SE
RAMSTK(15:0)
I$46
ECCREG
I$42
ECCGEN
I$45
RAMMUX
I$1
RAM
I$62
CORNMUX
I$44
CORRECT6
I$51
ECCGENG
I$50
TOSREG
I$46
RAMDEC
I$2
CNTR
CK(5:0)
CLK
ECCLD
CLR
TEST
E(5:0)
DOUT(15:0)
EOUT(5:0)
CORN(15:0)
TESTECC
SYN(5:0)
RD(31:0)
WR(31:0)
CNT(11:6)
PSHN
SD
CLR
CLK
STALLN
BORN
SCRUB
TEST
ECR
UPCIN(15:0)
DSTIN(15:0)
RAMSTK(15:0)
TESTECC
ECCLD
PSH
POP
ZERO

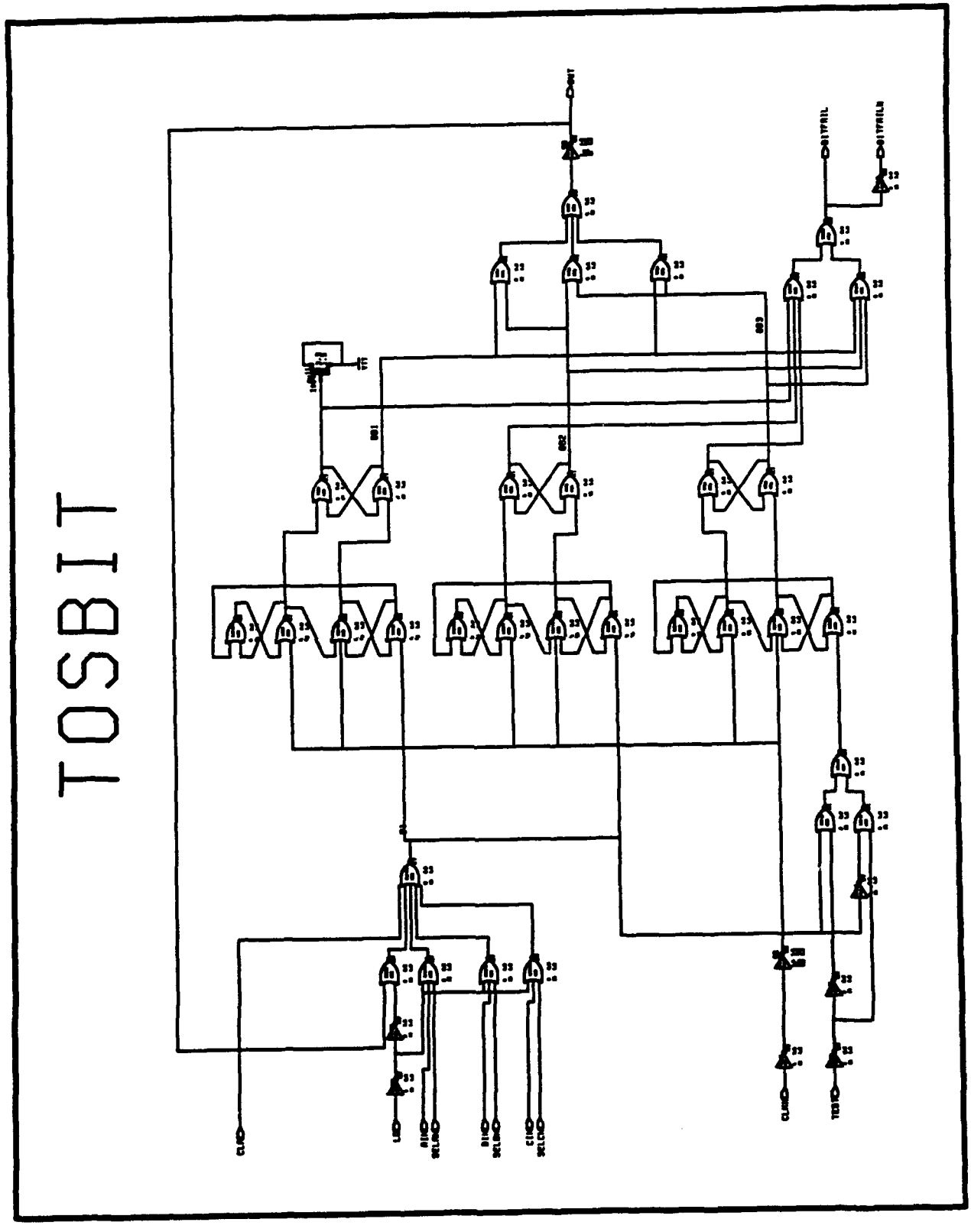

UXX
STALL
S(5:0)
STALLN
ALULD
APLD
CLK
PIPGO
SET

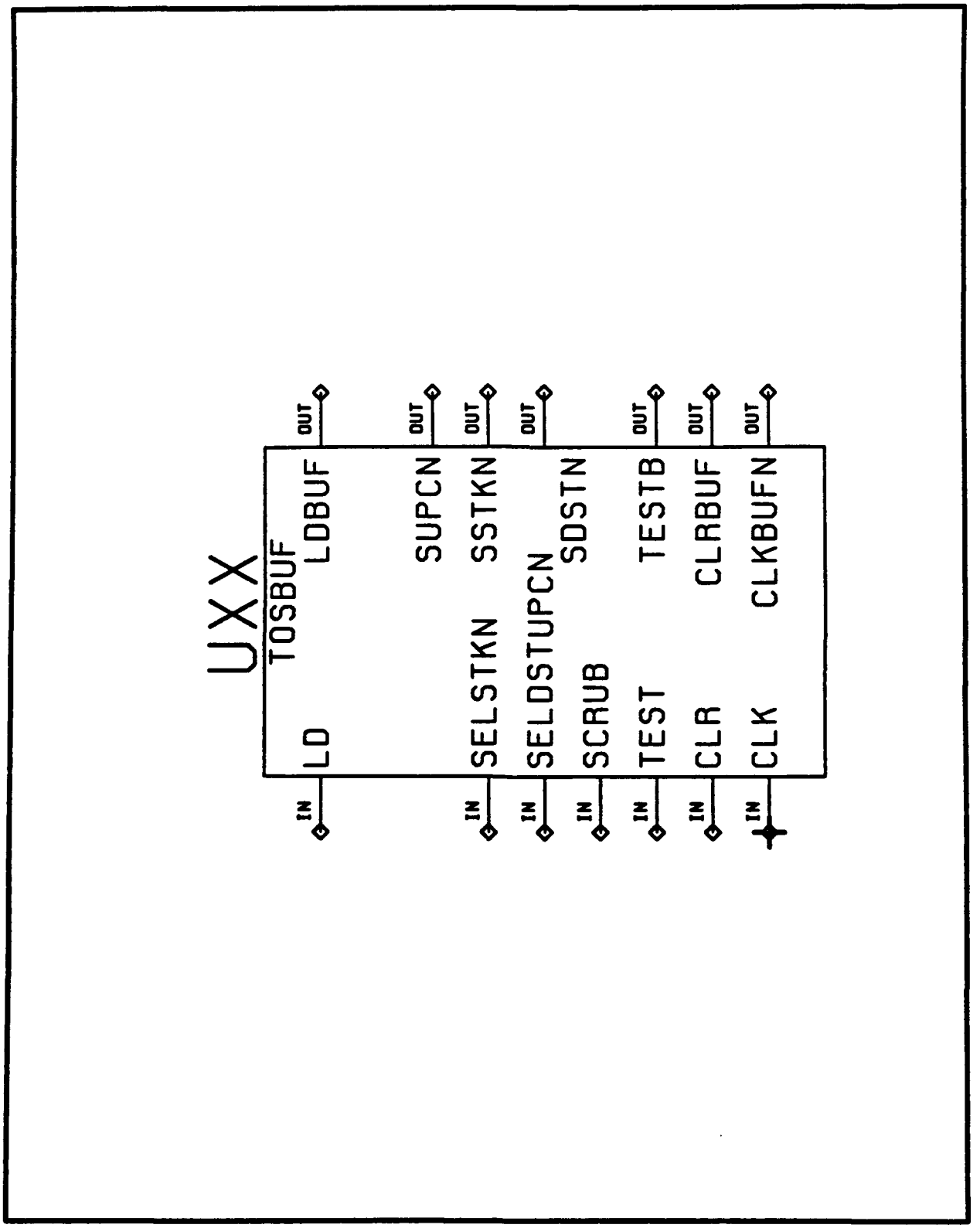

STALL
STALLN
ALULD
APLD
SQ
I$4
SQINV
I$61
INV
I$1
ALULDBIT
I$21
NOR
I$141
INV
I$142
NOR
D
Q
CLK
SET
0
1
2
3
4
5
CLK
SET
PIPGO

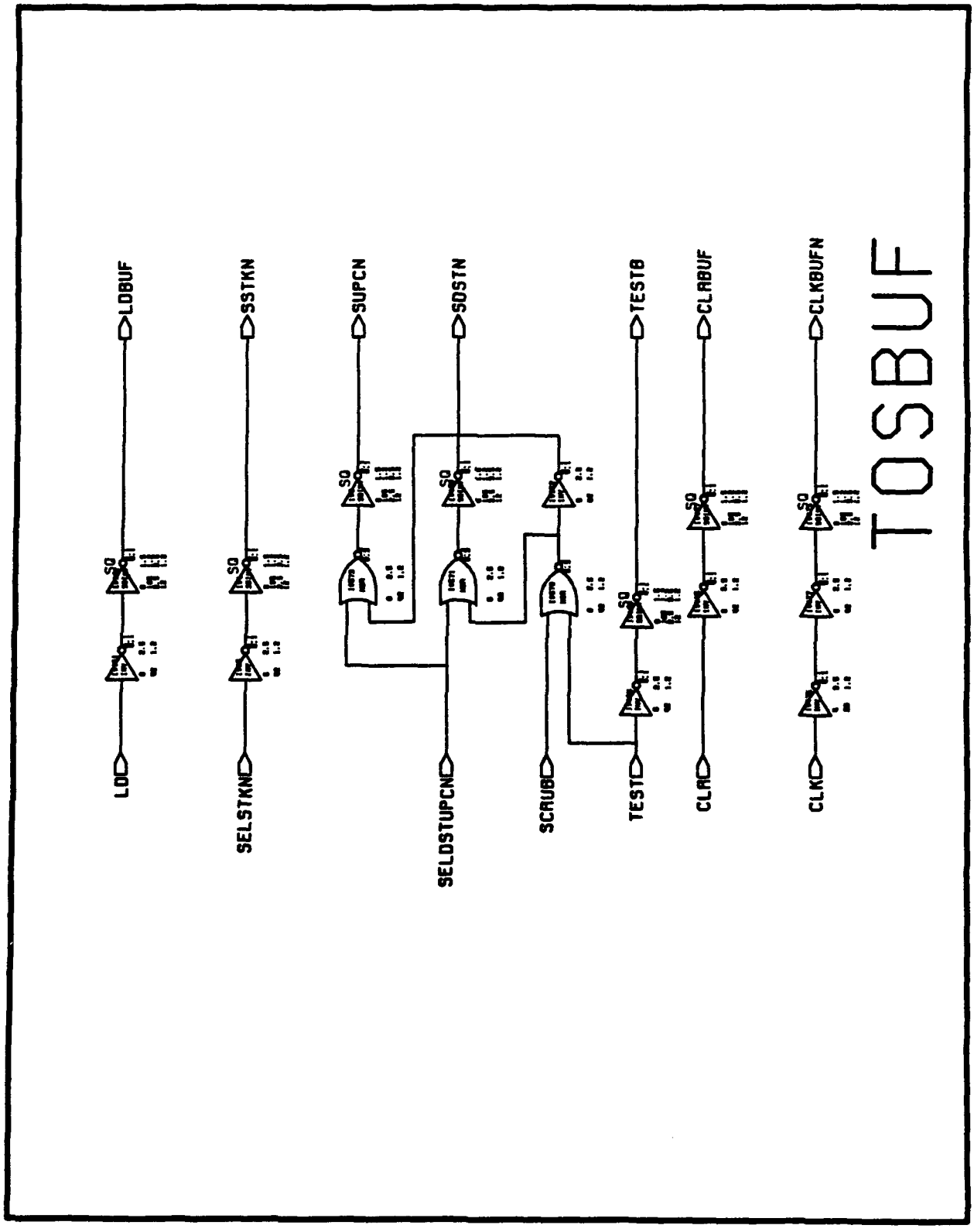

0.0
0.0
OUT
BIT
0.0
0.0
OUT
BITB
STKBIT
D
DB
RD
WR
IN
IN
IN
IN
STKBIT
stkbit.bin

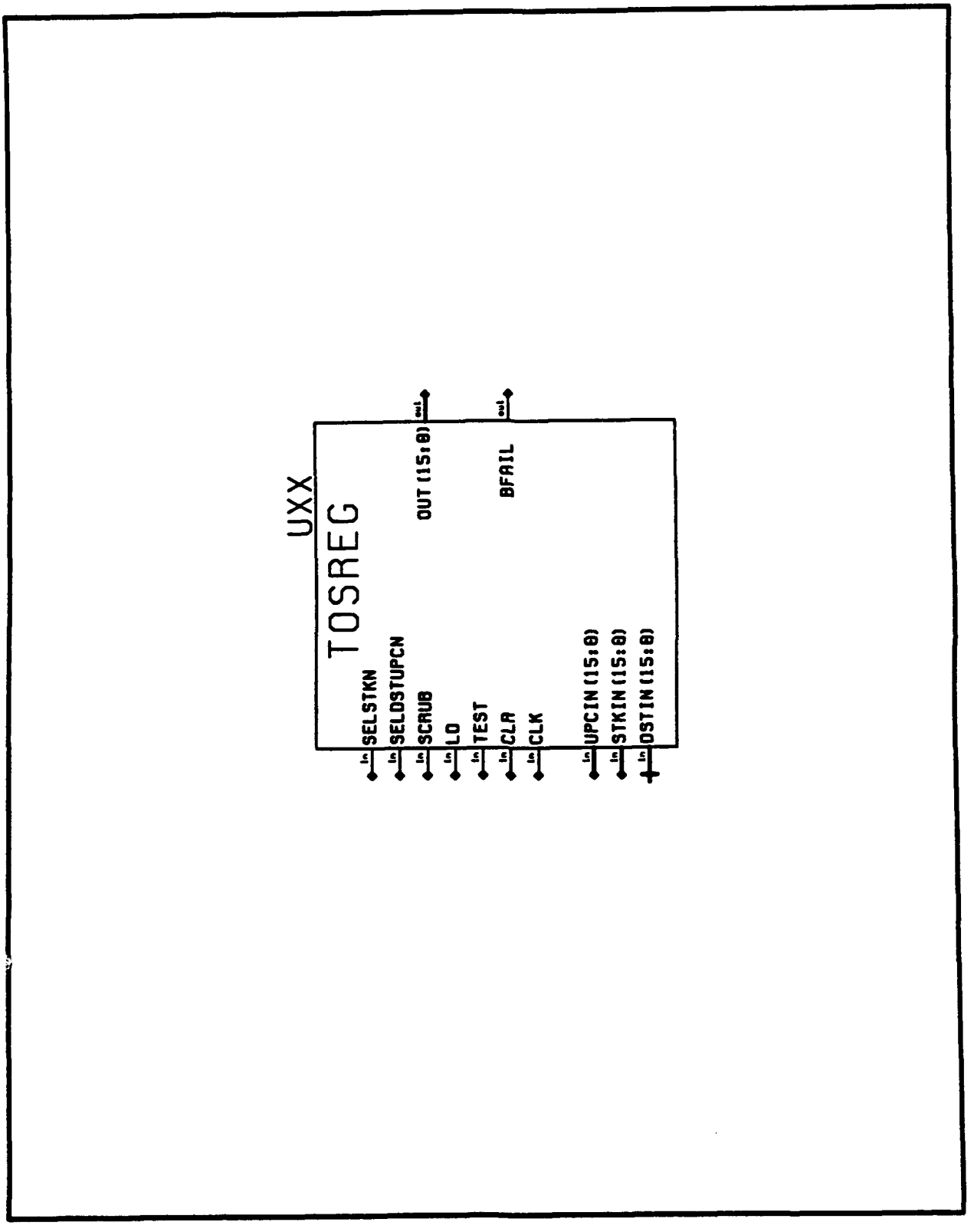

BITB
BIT
REVISED 8/2/89 RF
B9
B10
B7
B8
VTT
B5
B6
CG
B3
B4
B1
B2
D
DB
WR
RD

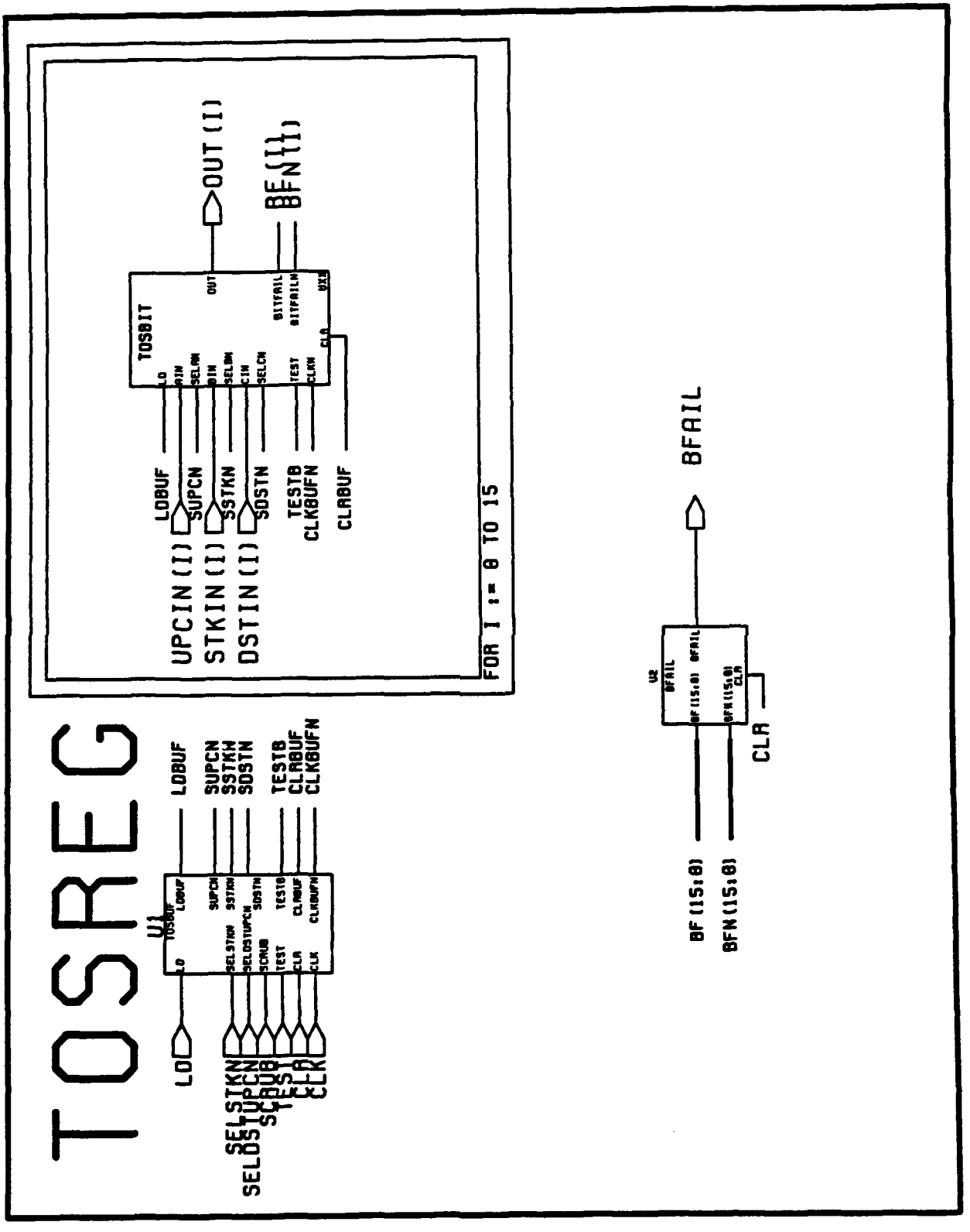

TOSBIT
LD
AIN
SELAN
BIN
SELBN
CIN
SELCN
TEST
CLKN
CLR
OUT
BITFAIL
BITFAILN
UXX
IN
OUT
NI

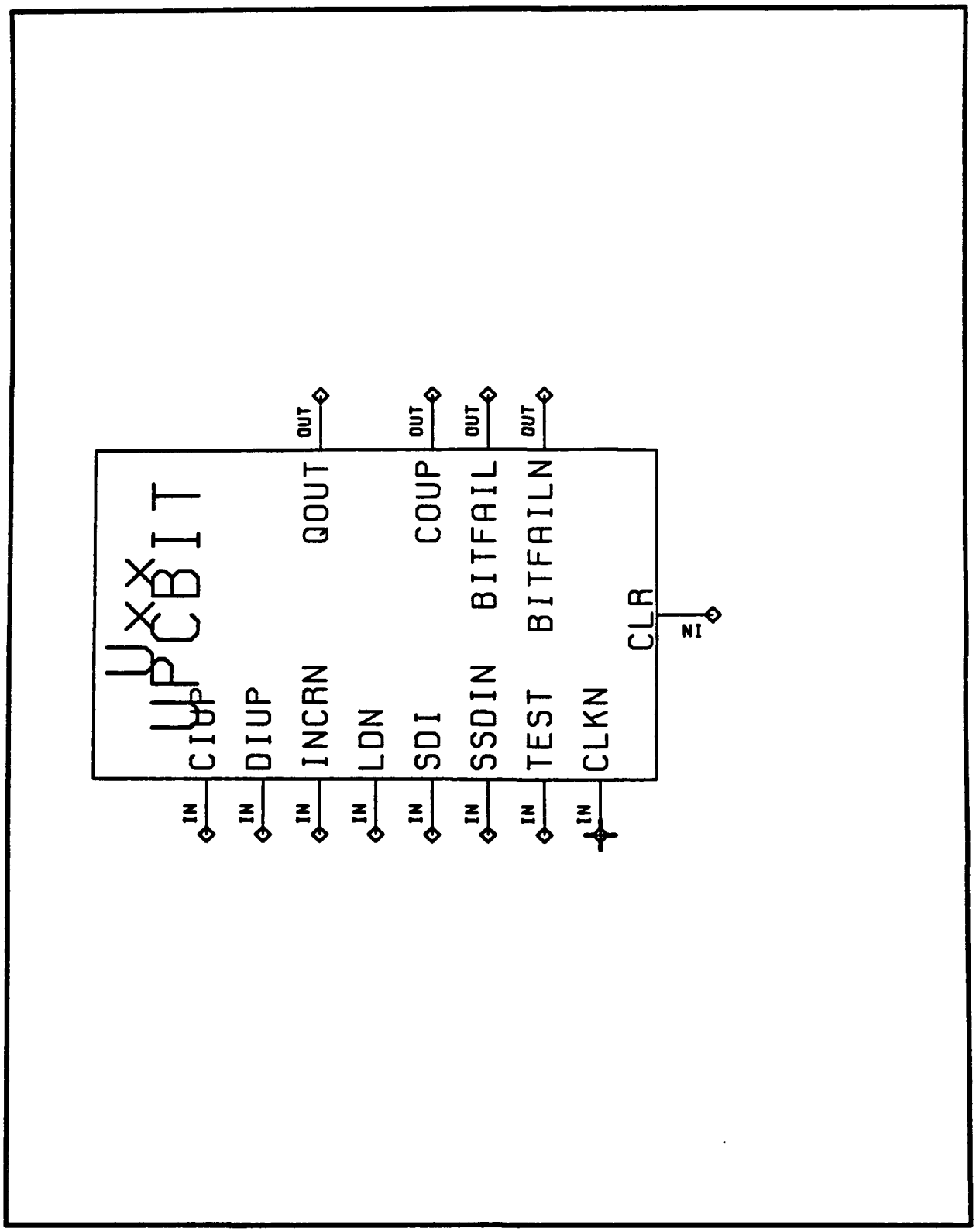

TOSBIT

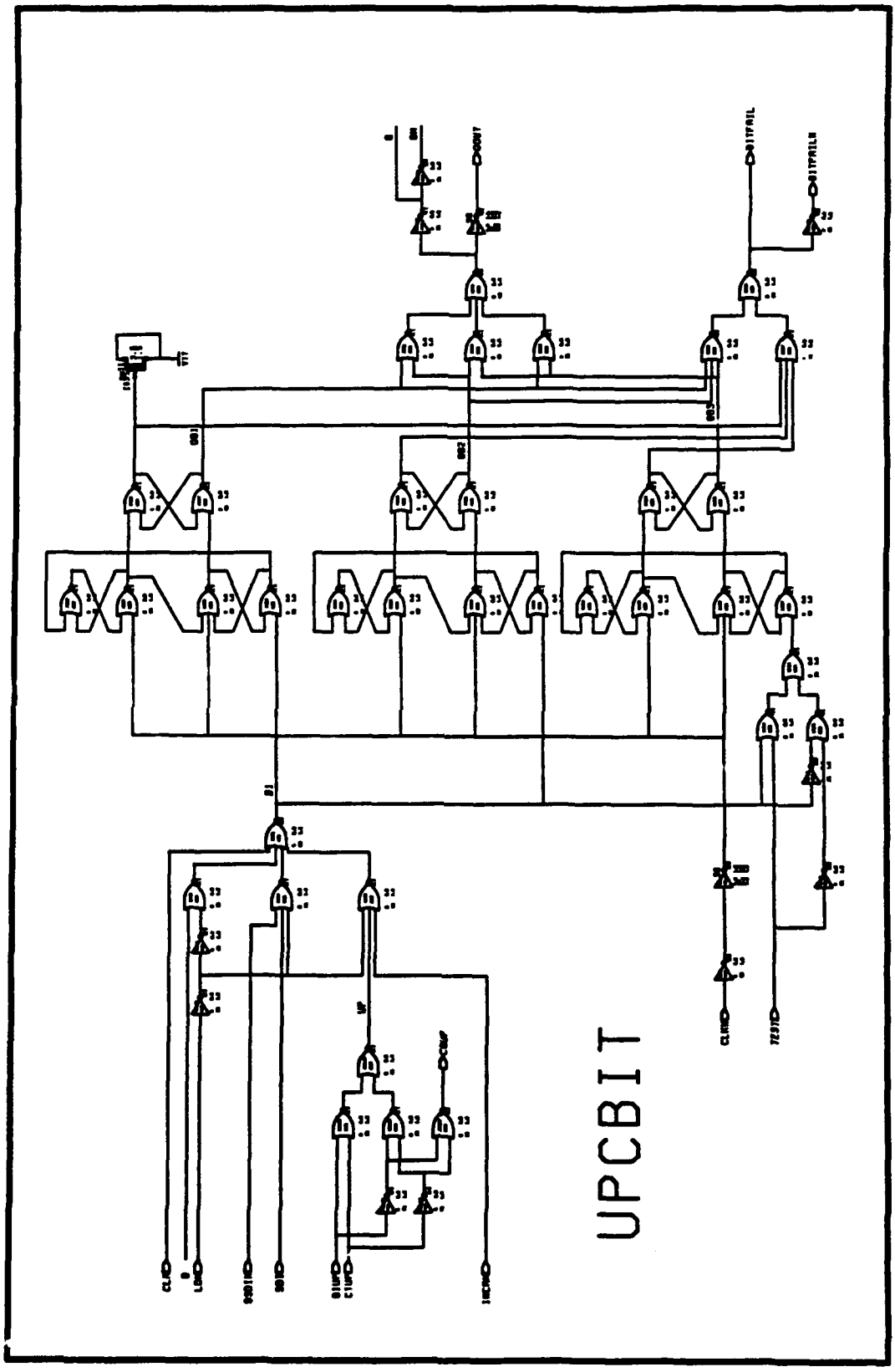

UXX
TOSBUF
LDBUF
SUPCN
SSTKN
SDSTN
TESTB
CLRBUF
CLKBUFN
LD
SELSTKN
SELDSTUPCN
SCRUB
TEST
CLR
CLK
OUT
IN

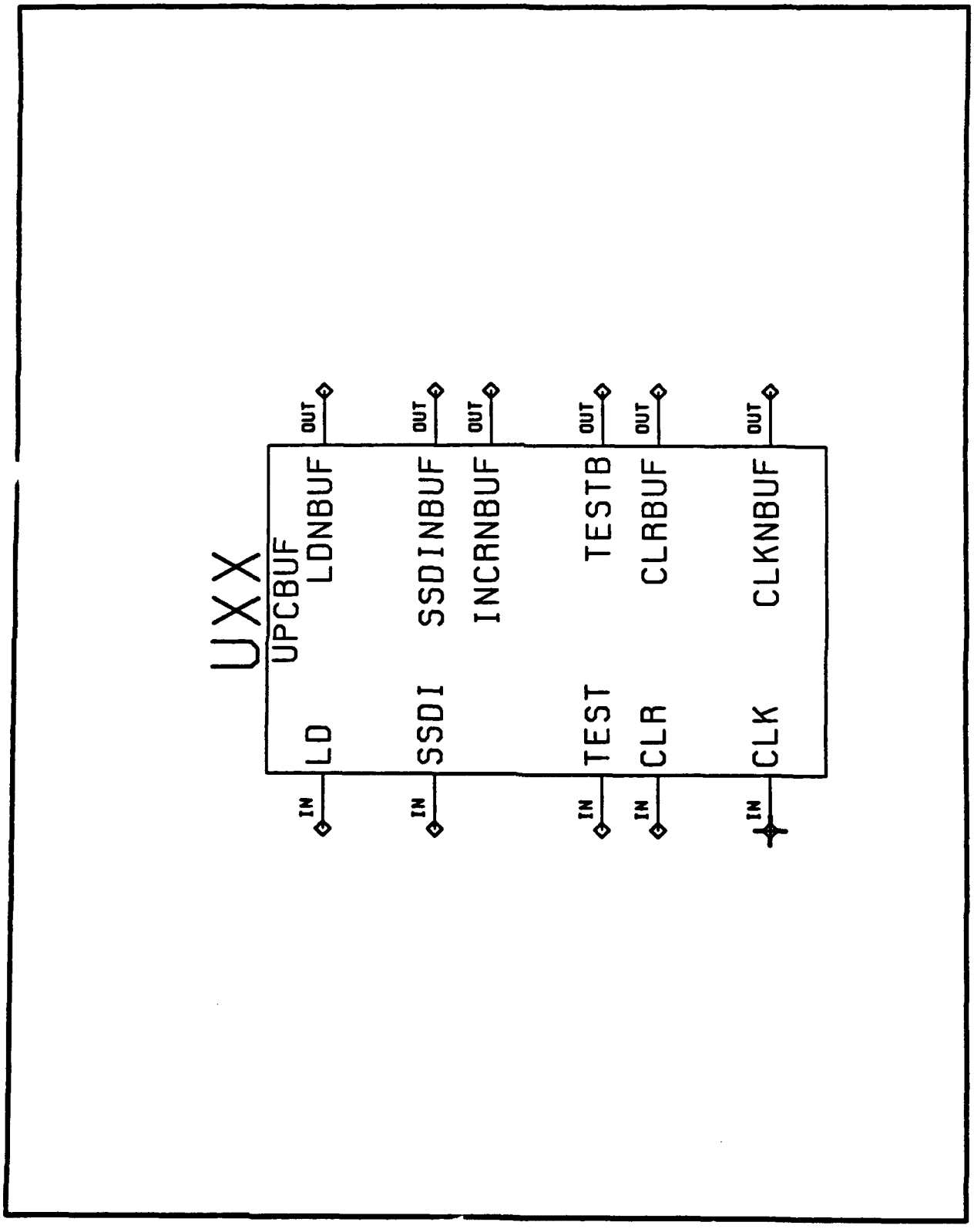

TOSBUF
LDBUF
SSTKN
SUPCN
SDSTN
TESTB
CLRBUF
CLKBUFN
LD
SELSTKN
SELDSTUPCN
SCRUB
TEST
CLR
CLK

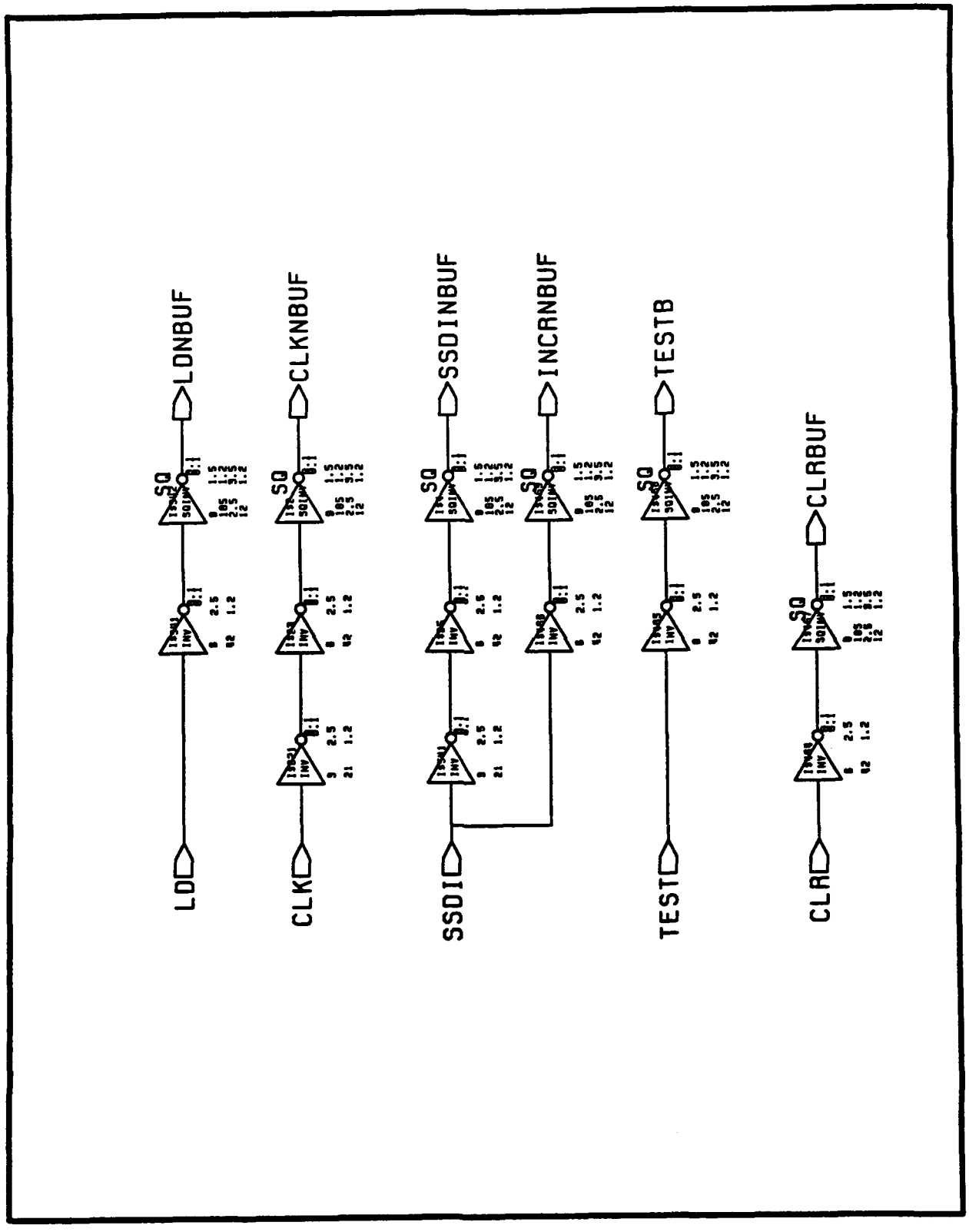

UXX
TOSREG
OUT(15:0)
BFAIL
SELSTKN
SELDSTUPCN
SCRUB
LO
TEST
CLR
CLK
UPCIN(15:0)
STKIN(15:0)
DSTIN(15:0)

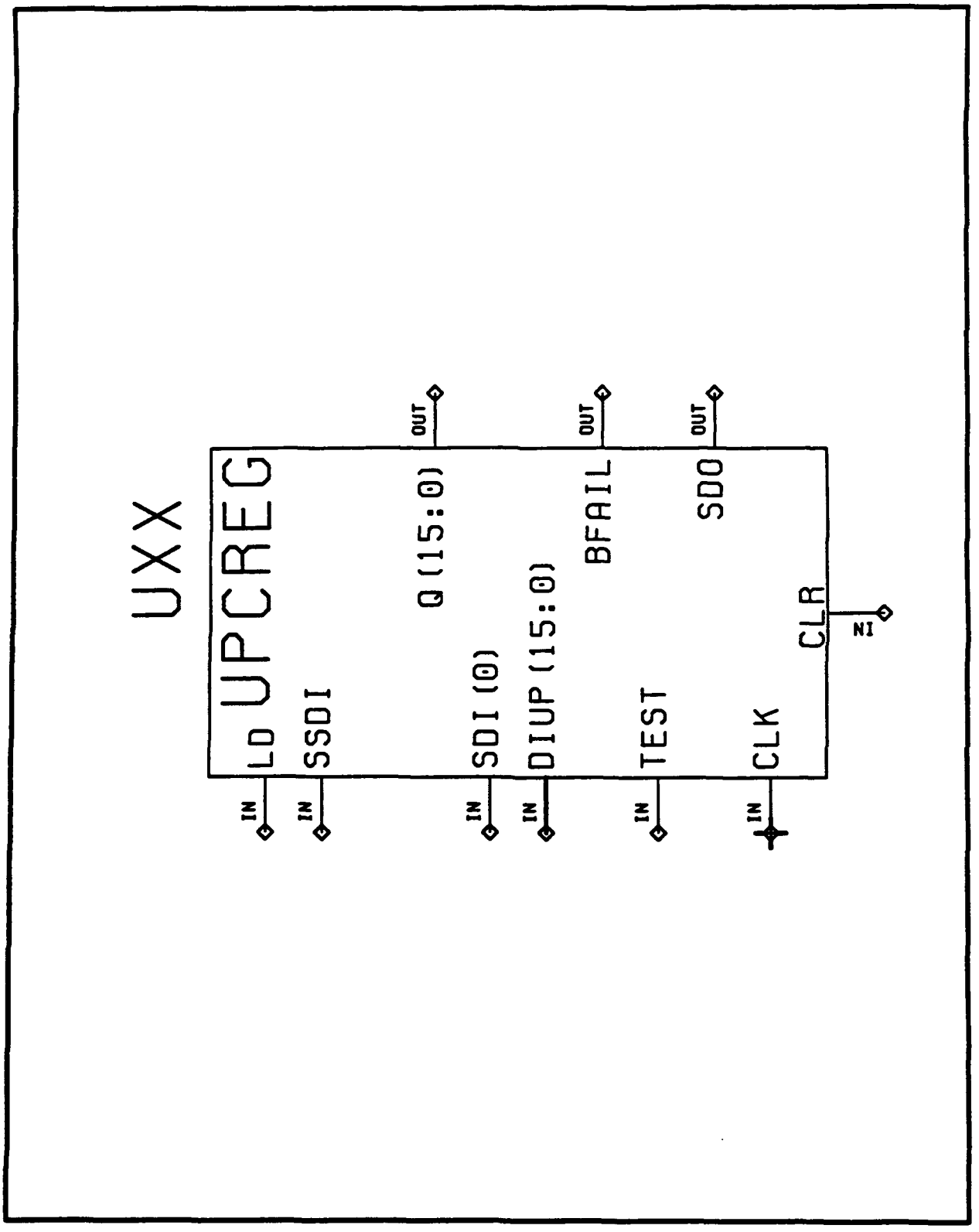

TOSREG
U1
TOSBUF
LO
LDBUF
SUPCN
SSTKN
SDSTN
TESTB
CLRBUF
CLKBUFN
SELSTKN
SELDSTUPCN
SCRUB
TEST
CLR
CLK
FOR I := 0 TO 15
TOSBIT
OUT
BITFAIL
CIN
SELCN
UPCIN(I)
STKIN(I)
DSTIN(I)
OUT(I)
BFN(I)
U2
BFAIL
BF(15:0)
BFN(15:0)

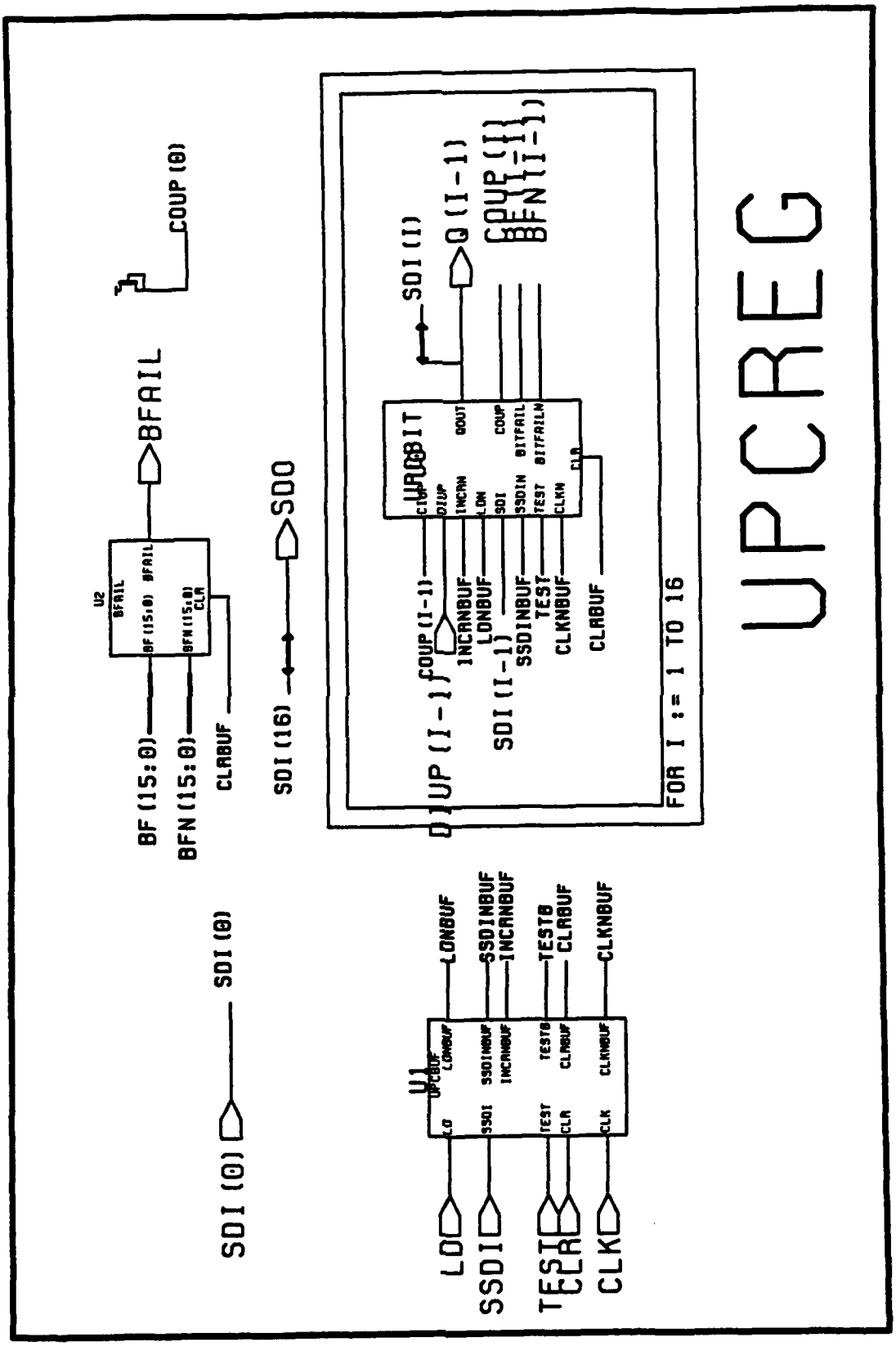

UXXUPCBIT
CIUP
DIUP
INCRN
LDN
SDI
SSDIN
TEST
CLKN
QOUT
COUP
BITFAIL
BITFAILN
CLR
IN
OUT
NI

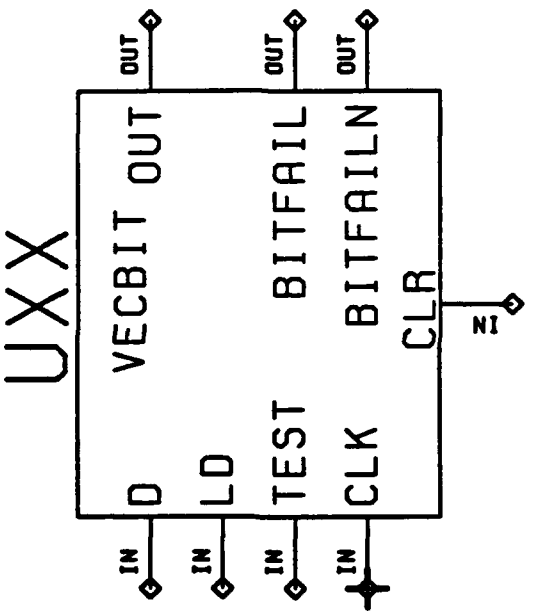

UPCBIT


UXX
UPCBUF
LDNBUF
SSDINBUF
INCRNBUF
TESTB
CLRBUF
CLKNBUF
LD
SSDI
TEST
CLR
CLK
IN
OUT

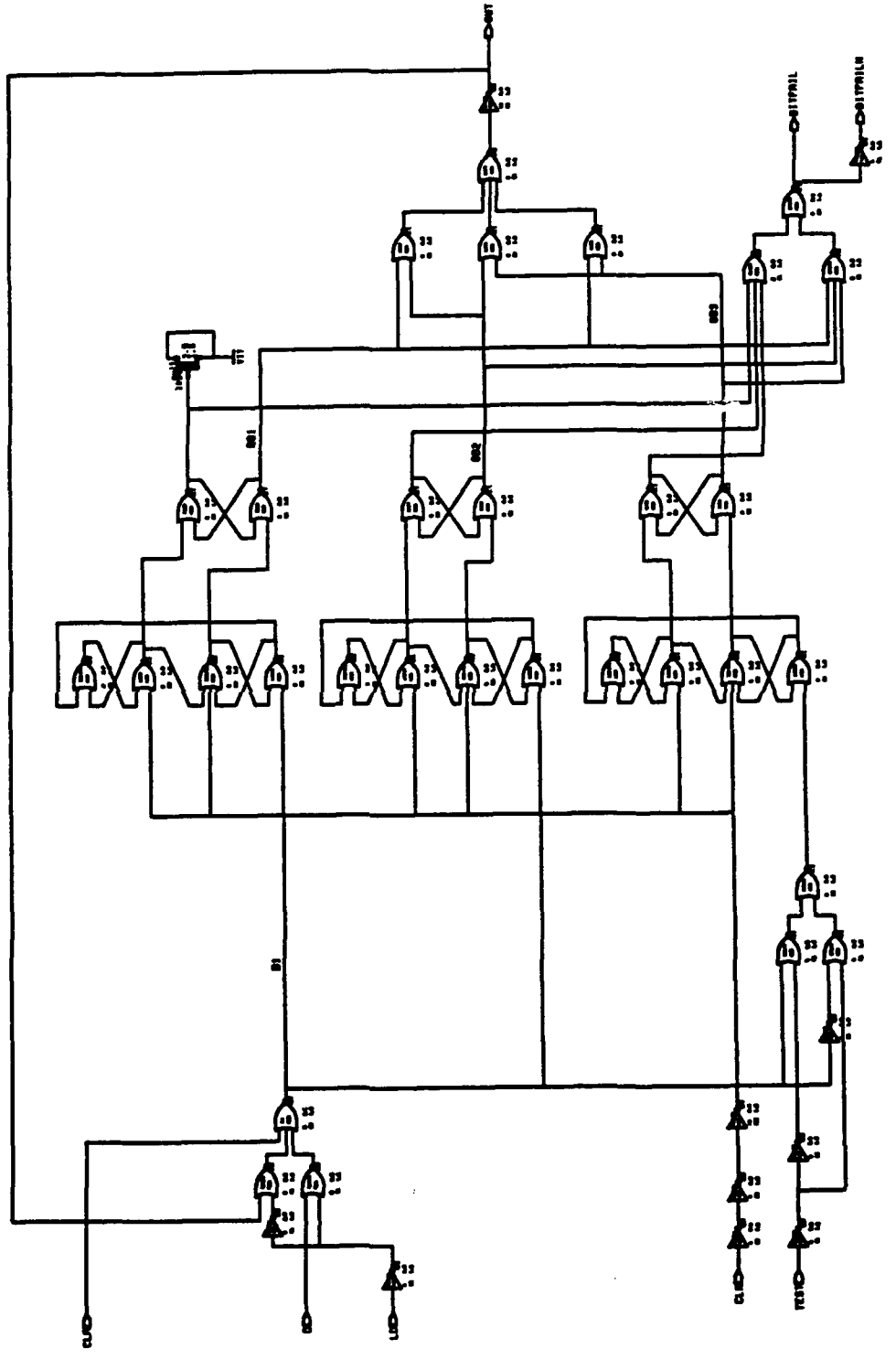

LDNBUF
CLKNBUF
SSDINBUF
INCRNBUF
TESTB
CLRBUF
LD
CLK
SSDI
TEST
CLR

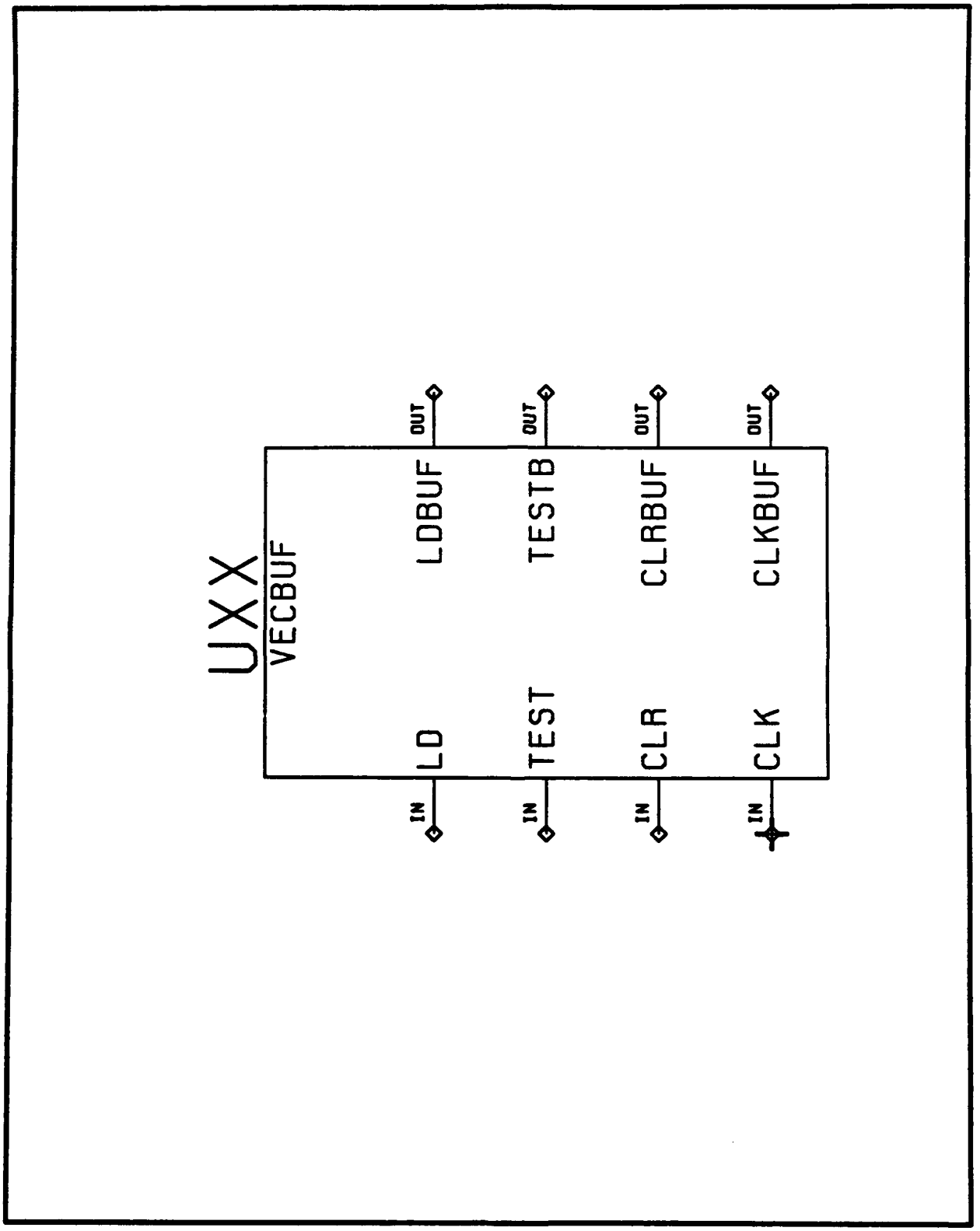

UXX
UPCREG
LD
SSDI
SDI(0)
DIUP(15:0)
TEST
CLK
CLR
Q(15:0)
BFAIL
SDO
IN
OUT
NI

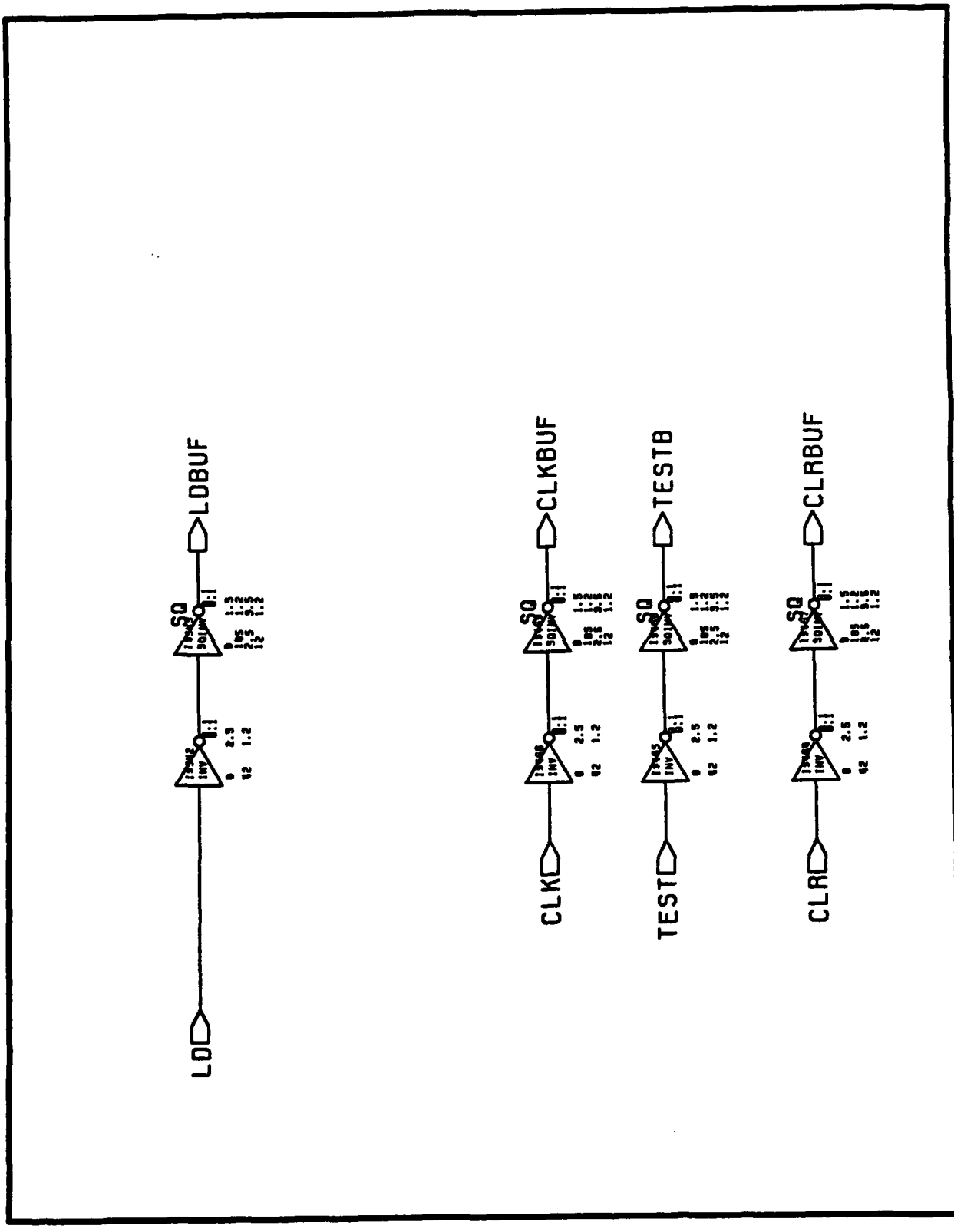

UPCREG
FOR I := 1 TO 16
UPBIT
U1
U2
COUP (0)
BFAIL
SDO
SDI (16)
SDI (I)
Q (I-1)
COUP (I)
BFN (I-1)
UP (I-1)
COUP (I-1)
INCRNBUF
LONBUF
SSDINBUF
TEST
CLKNBUF
CLRBUF
BF (15:0)
BFN (15:0)
SDI (0)
LD
SSDI
TEST
CLR
CLK

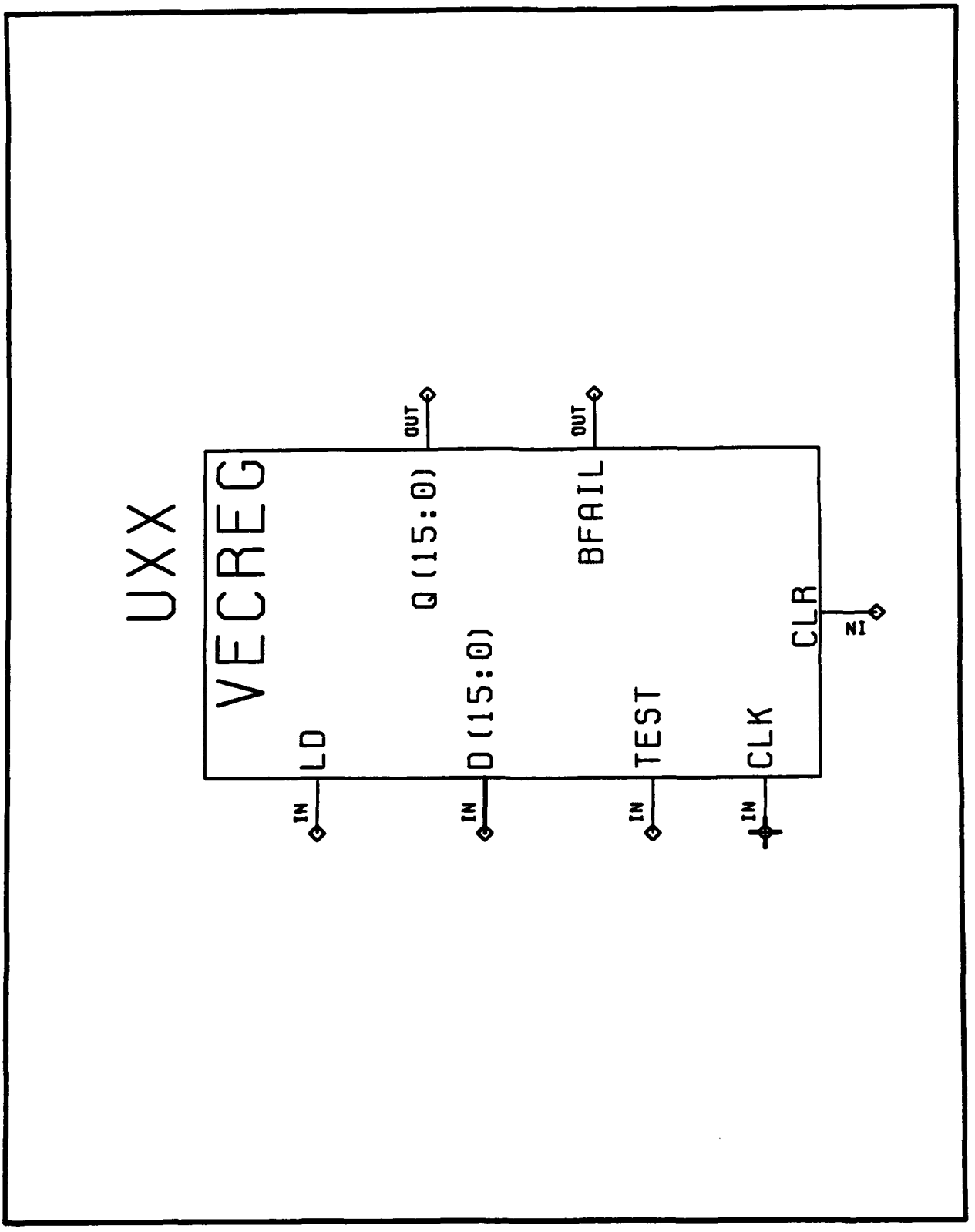

UXX
VECBIT OUT
BITFAIL
BITFAILN
CLR
D
LD
TEST
CLK
OUT
OUT
OUT
IN
IN
IN
IN
NI

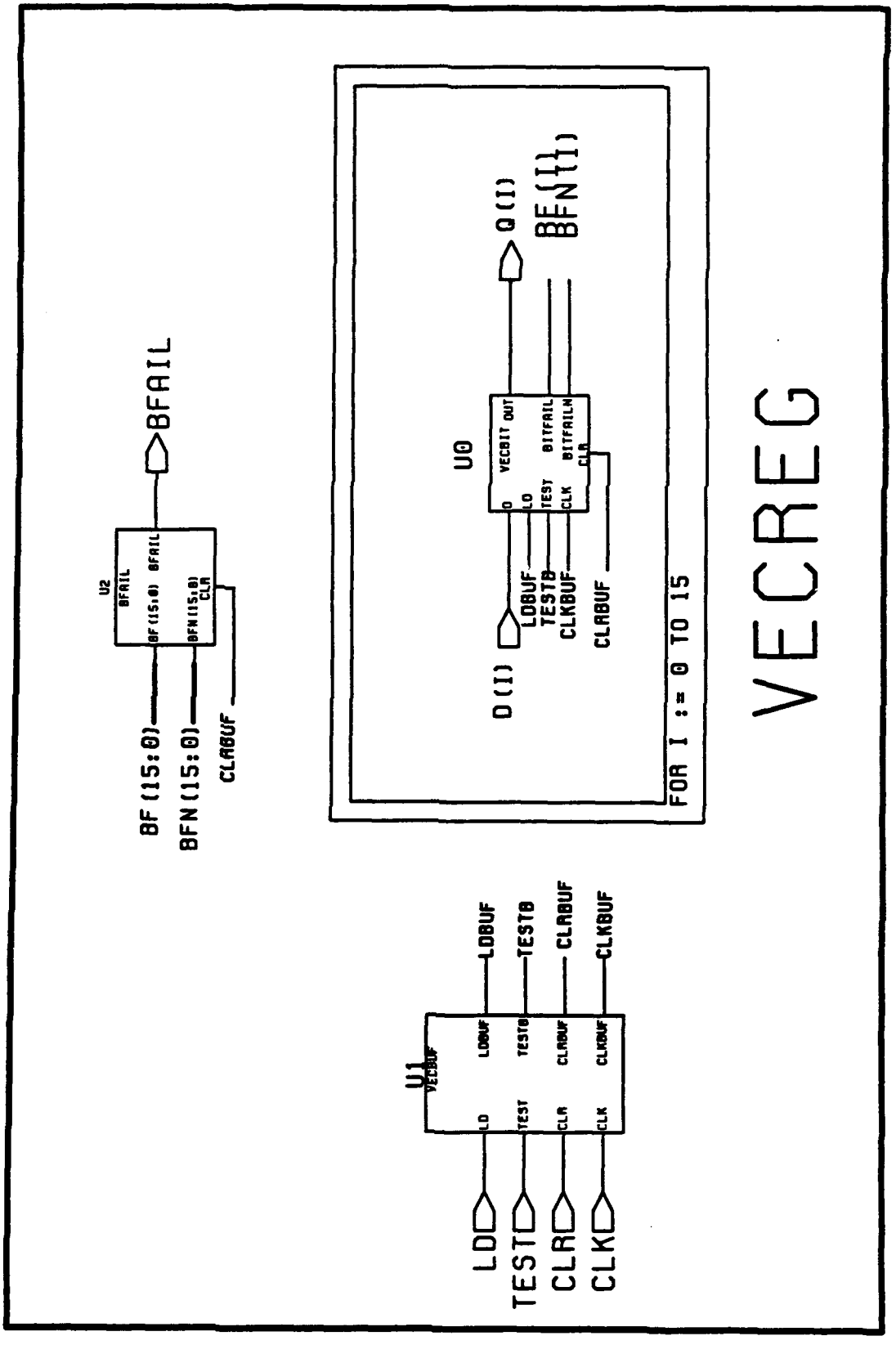
MAJORITY VOTE CIRCUIT WITH LATCHED INPUTS

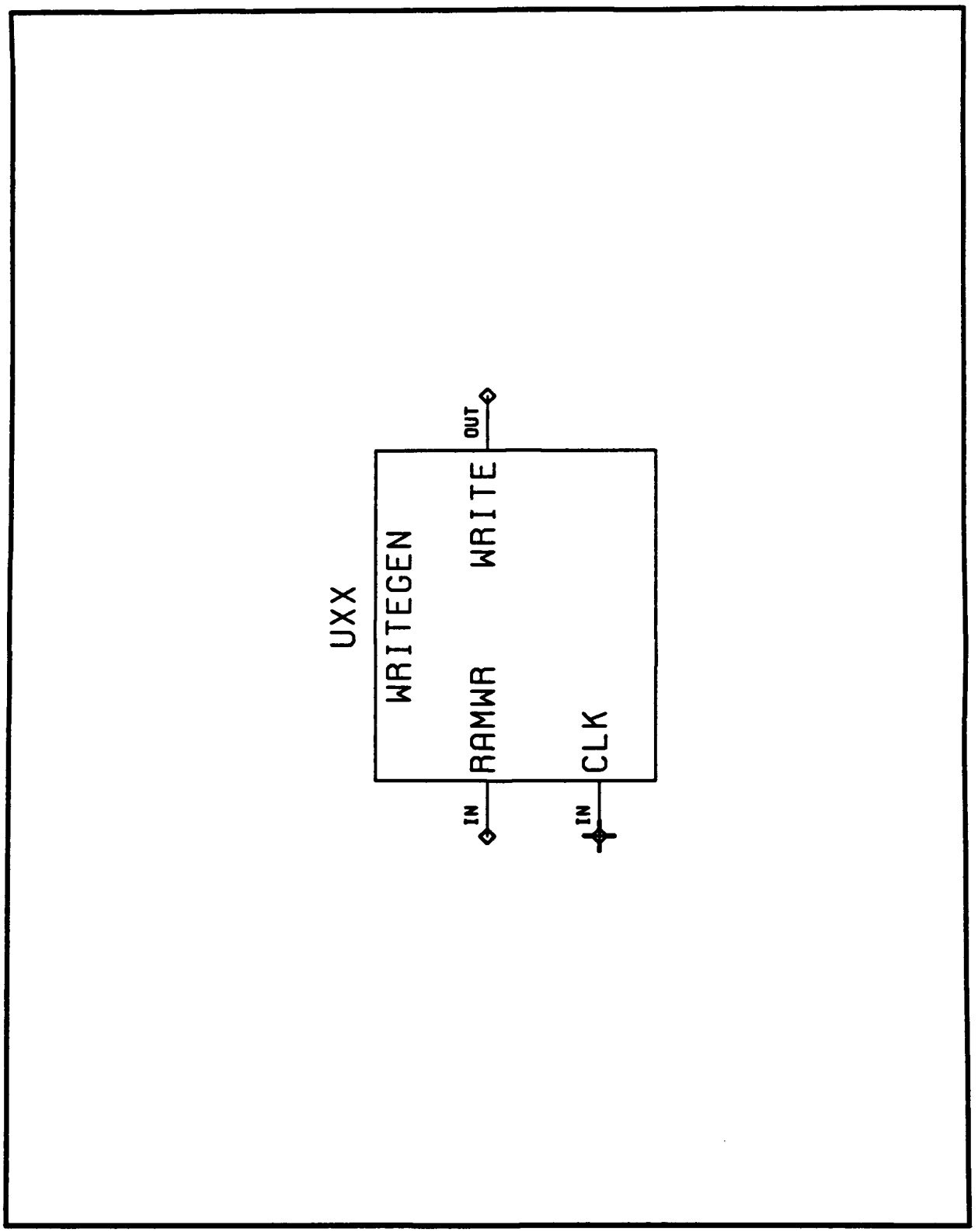



UXX
VECBUF
LDBUF
TESTB
CLRBUF
CLKBUF
LD
TEST
CLR
CLK
OUT
OUT
OUT
OUT
IN
IN
IN
IN

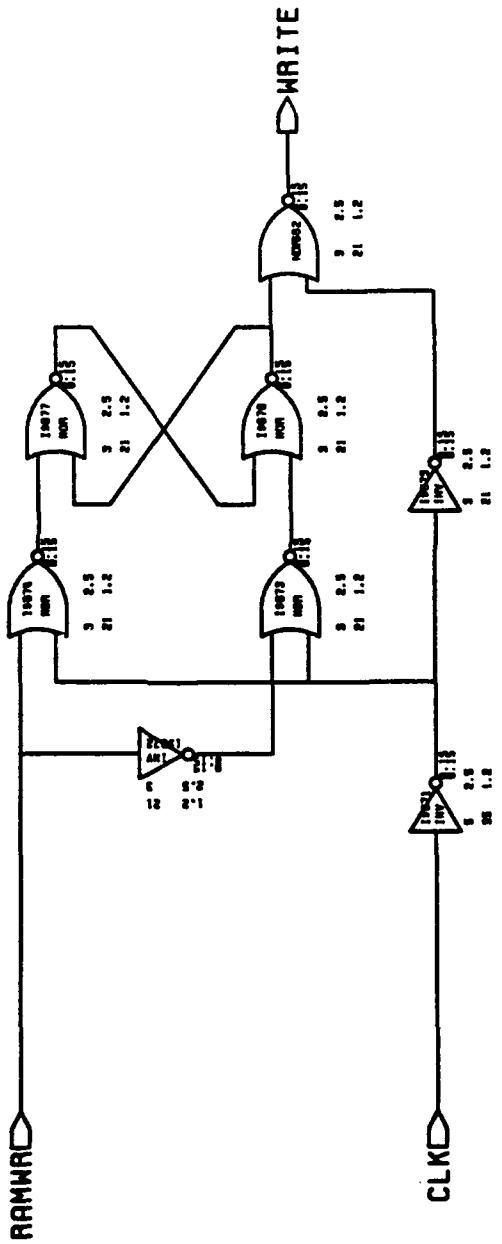

LDBUF
SO
INV
LD
CLKBUF
SO
INV
CLK
TESTB
SO
INV
TEST
CLRBUF
SO
INV
CLR

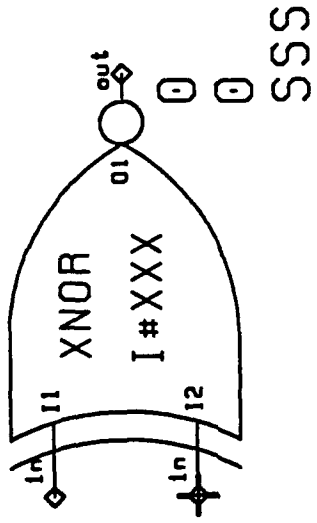

UXX
VECREG
LD
D(15:0)
TEST
CLK
CLR
Q(15:0)
BFAIL
IN
IN
IN
IN
OUT
OUT
NI

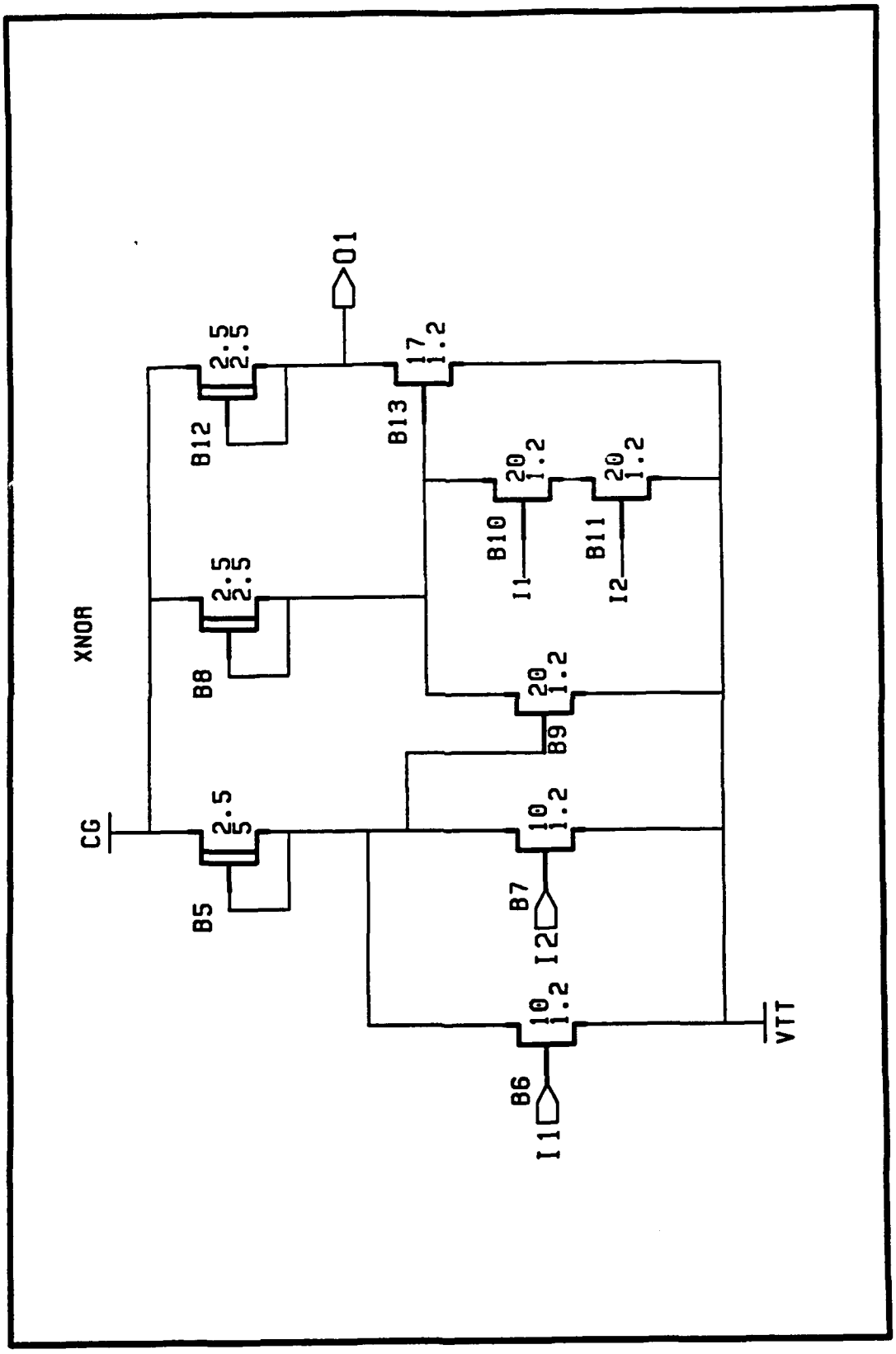

VECREG
FOR I := 0 TO 15
U0
VECBIT OUT
BITFAIL
BITFAILM
D
LO
TEST
CLK
CLR
D(I)
Q(I)
BFN(I)
LOBUF
TESTB
CLKBUF
CLABUF
U1
VECBUF
LD
TEST
CLR
CLK
U2
BFAIL
BF(15:0)
BFN(15:0)
BF(15:0)
BFN(15:0)
CLABUF

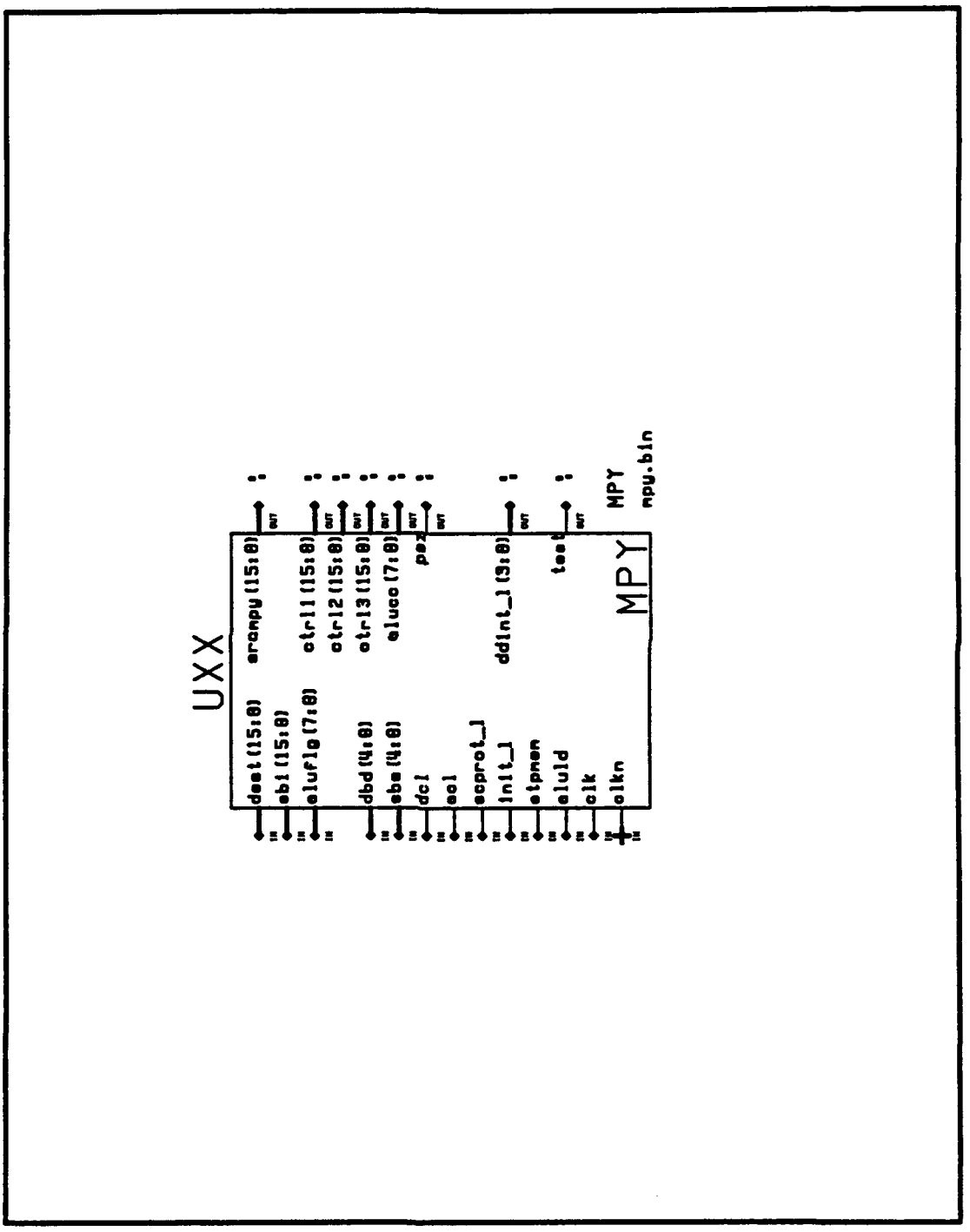

UXX
WRITEGEN
WRITE
RAMWR
CLK
OUT
IN
IN

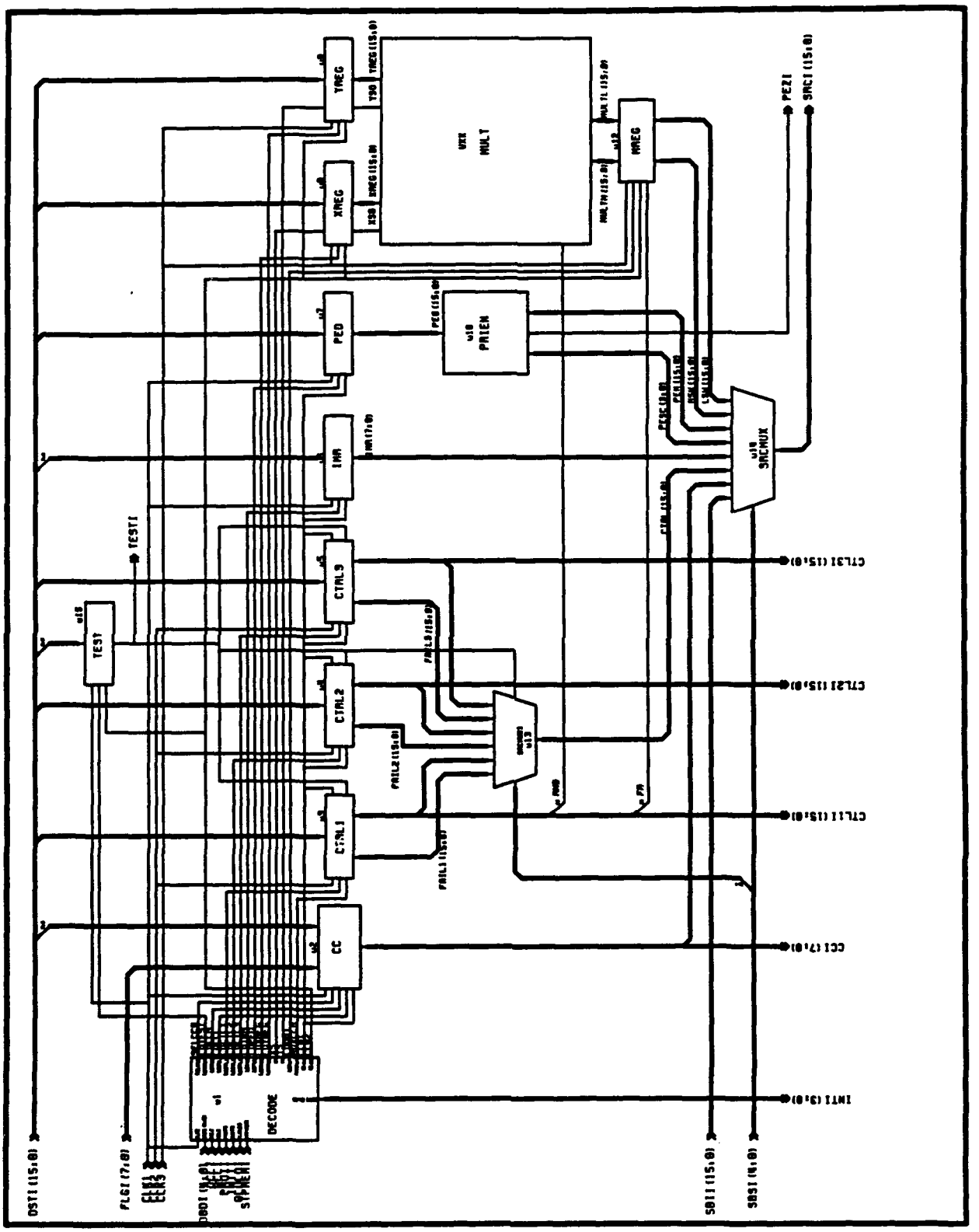
WRITEGEN: RAM WRITE PULSE GENERATOR

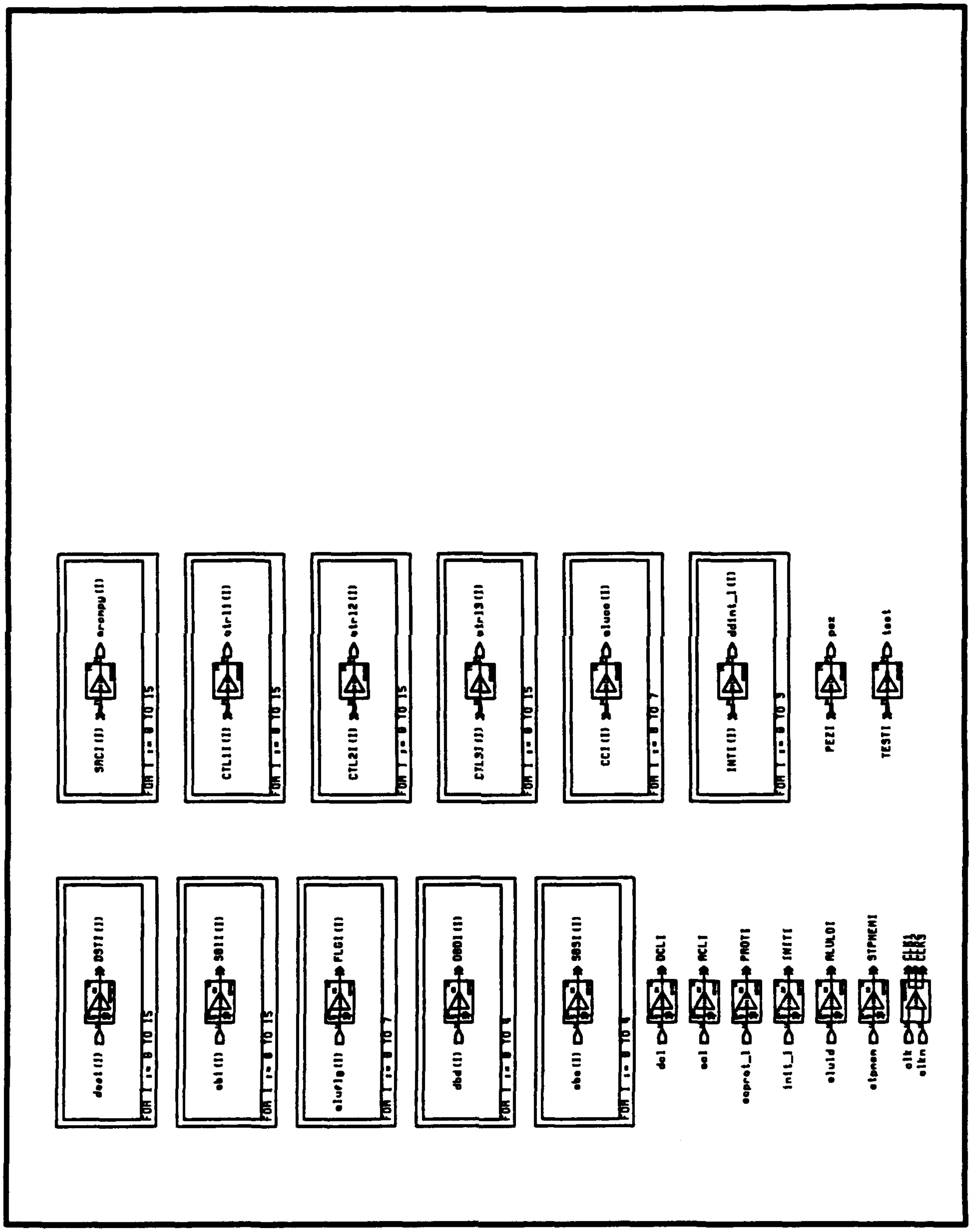


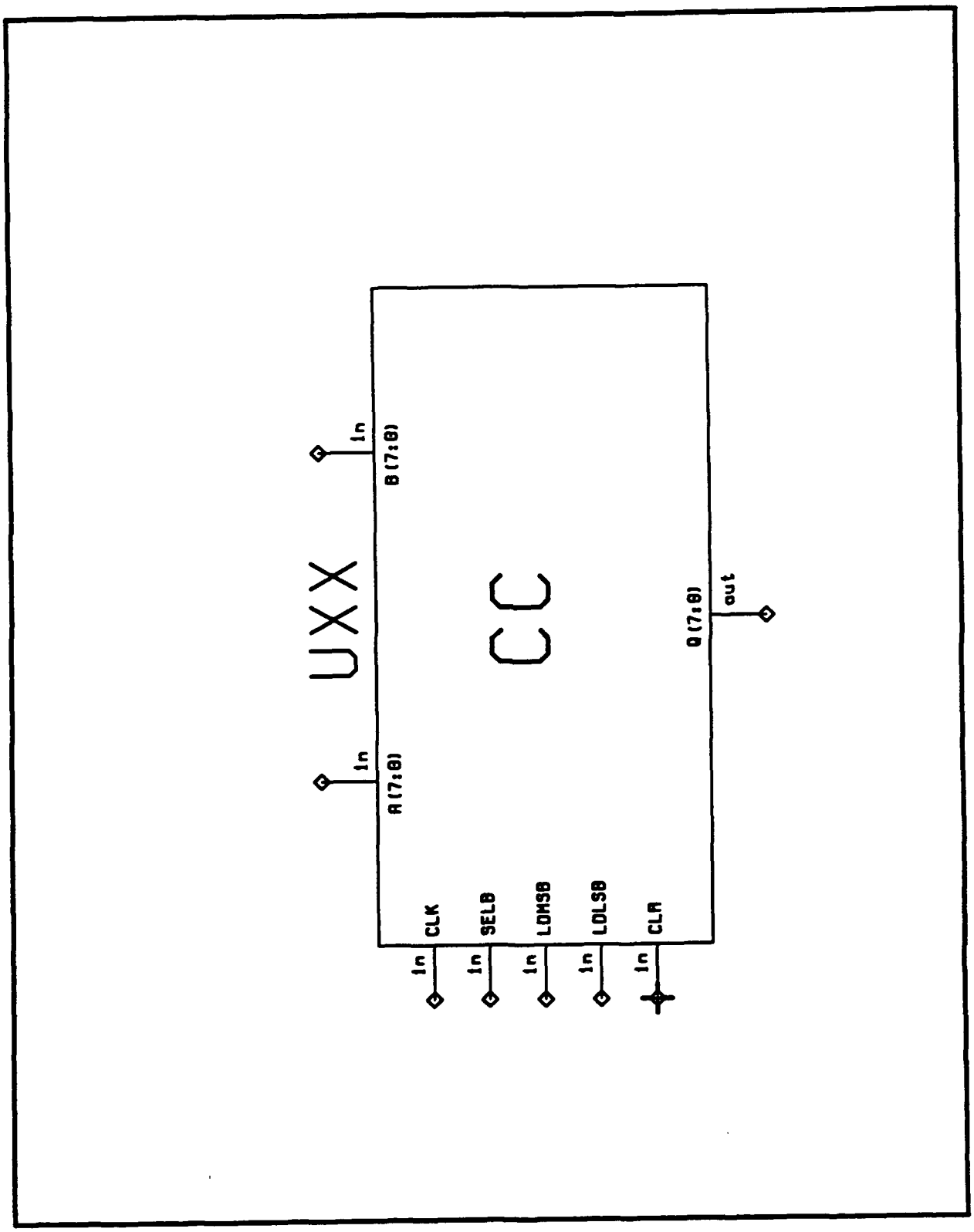

out
01
10
XNOR
I#XXX
11
12
In
In
0
0
SSS

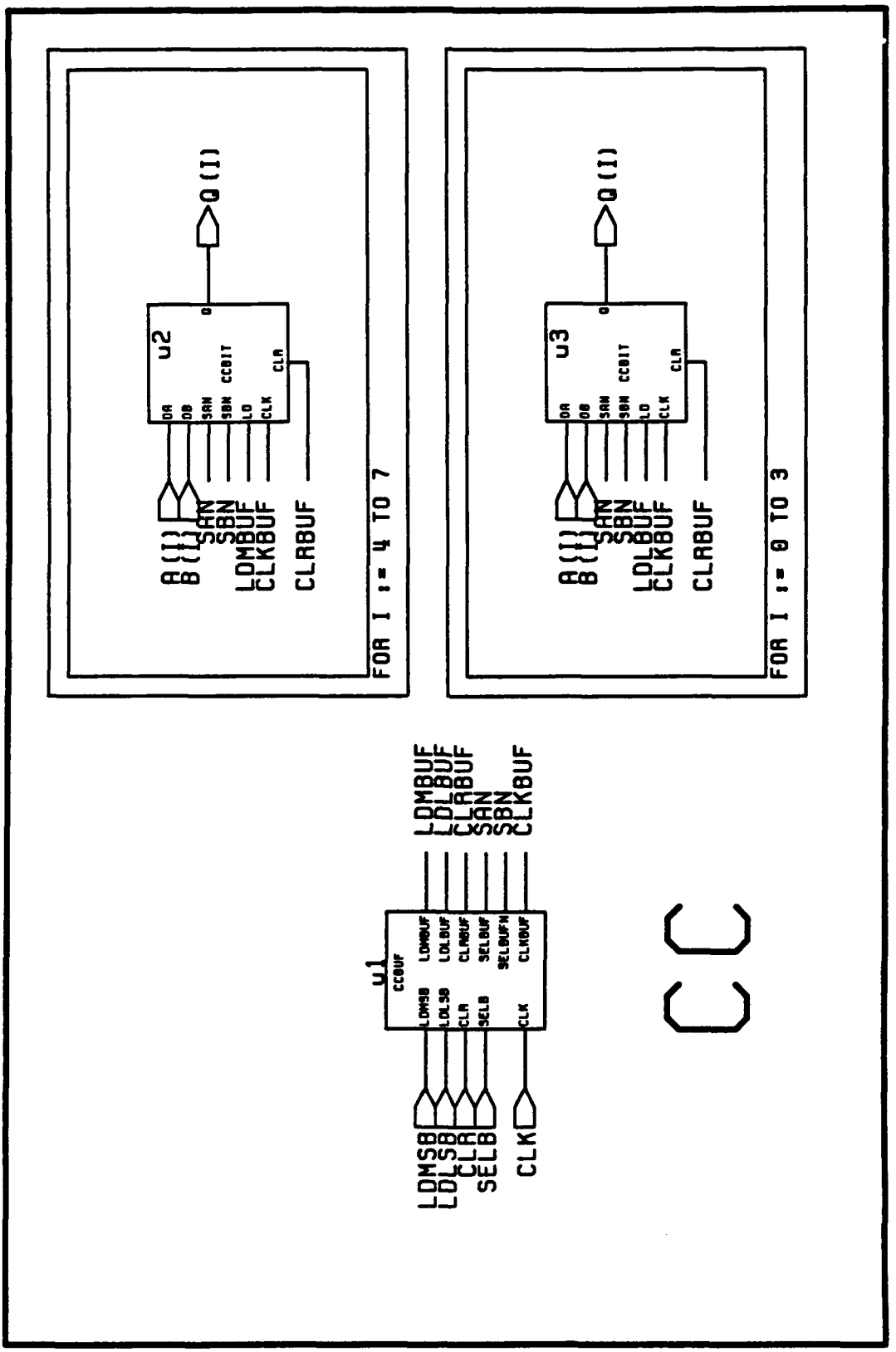

O1
2.5
2.5
17
1.2
B12
B13
20
1.2
20
1.2
B10
B11
I1
I2
2.5
2.5
XNOR
B8
20
1.2
B9
CG
2.5
5
10
1.2
B5
B7
I2
10
1.2
VTT
B6
I1

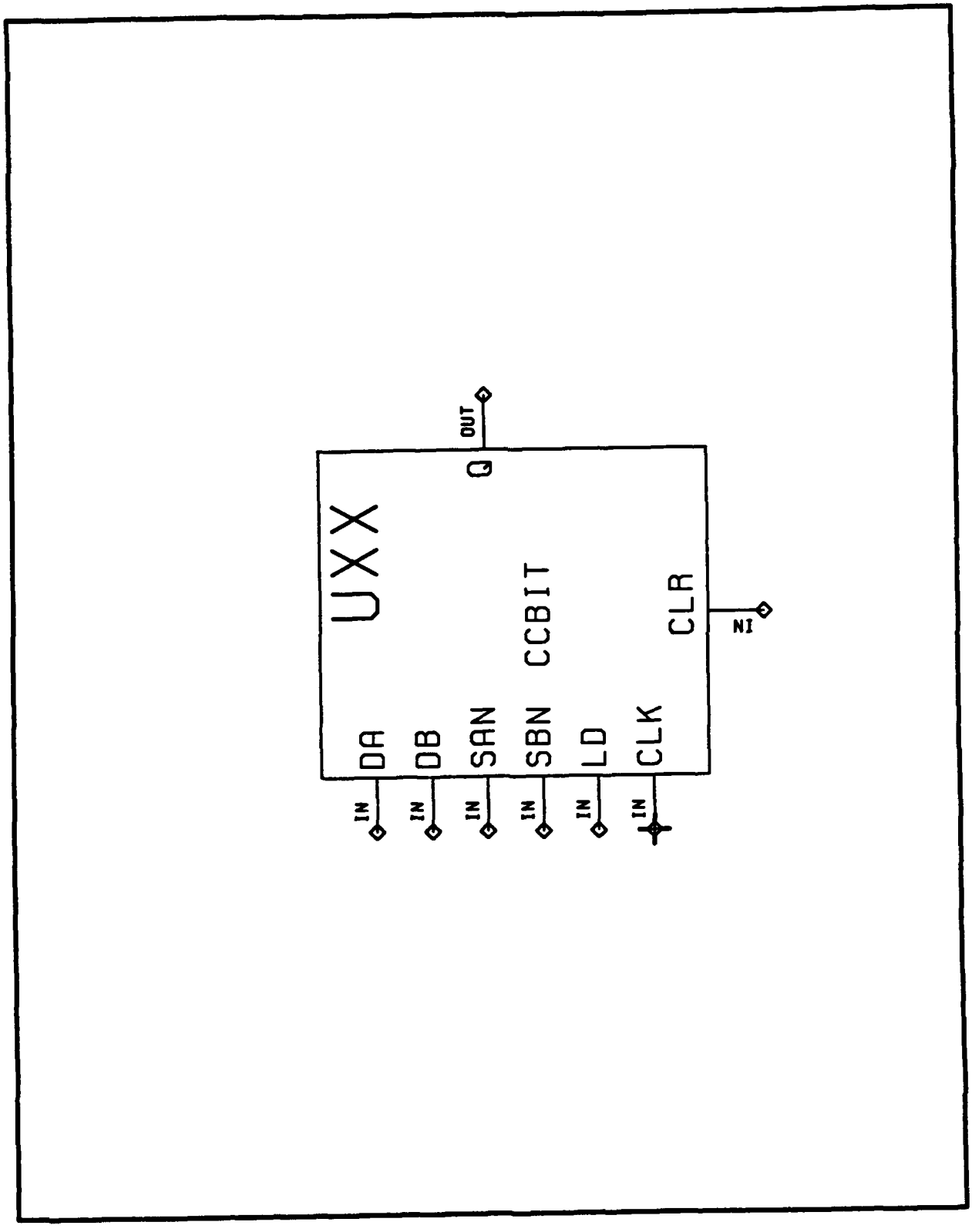

UXX
MPY
npu.bin
dest(15:0)
ebi(15:0)
aluflg(7:0)
dbd(4:0)
ebs(4:0)
dcl
ecl
ecprot_l
init_l
clpnen
cluld
clk
clkn
crapy(15:0)
ctrl1(15:0)
ctrl2(15:0)
ctrl3(15:0)
aluco(7:0)
pez
ddint_l(3:0)
test
MPY

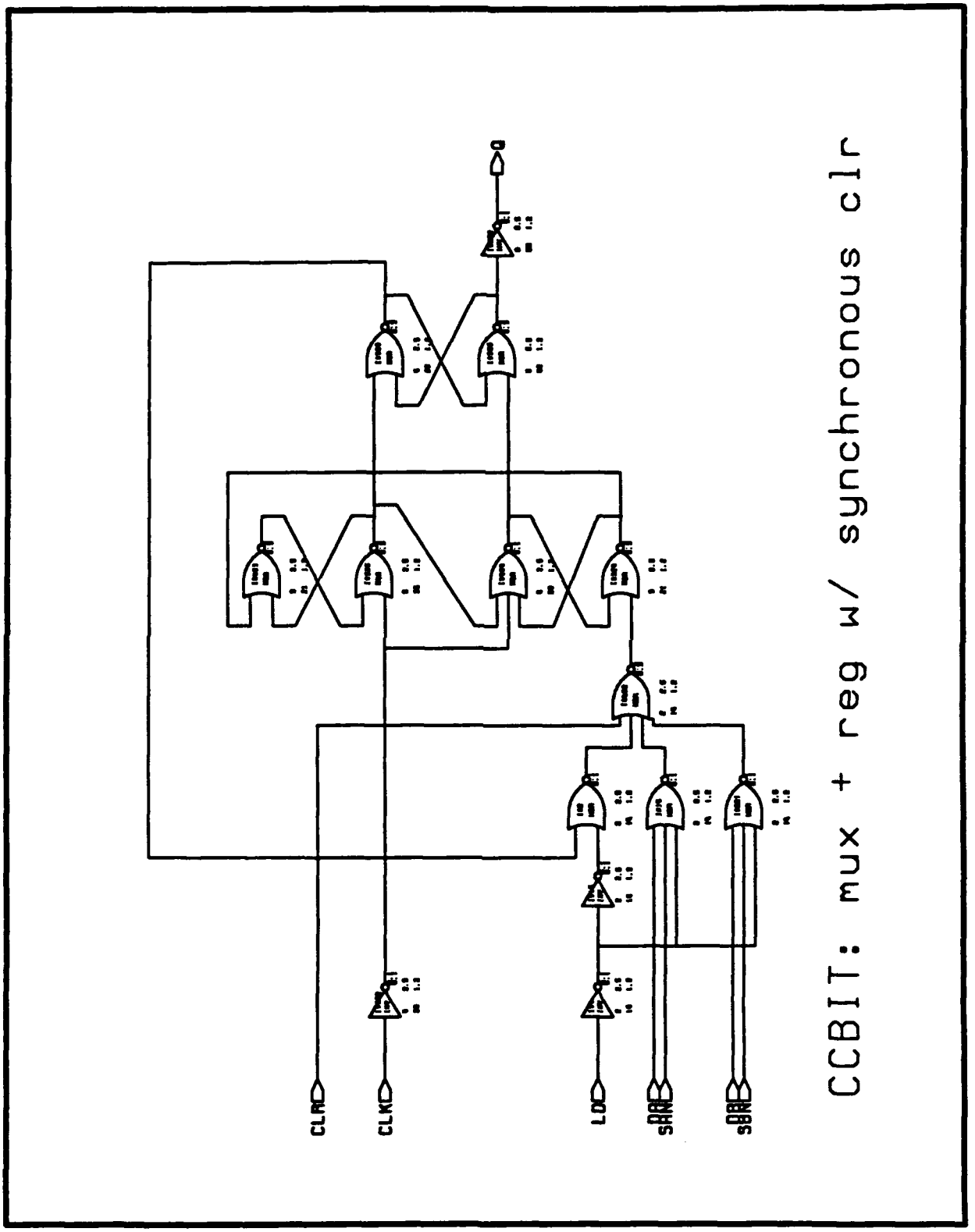

YREG
XREG
VXX
MULT
MREG
PEZI
SRCI (15:0)
PED
PRIEN
INR
SRCMUX
TEST1
TEST
CTRL3
CTRL2
CTRL1
CC
DECODE
CTL31 (15:0)
CTL21 (15:0)
CTL11 (15:0)
CCI (7:0)
INT1 (3:0)
DST1 (15:0)
SB11 (15:0)
SB31 (4:0)

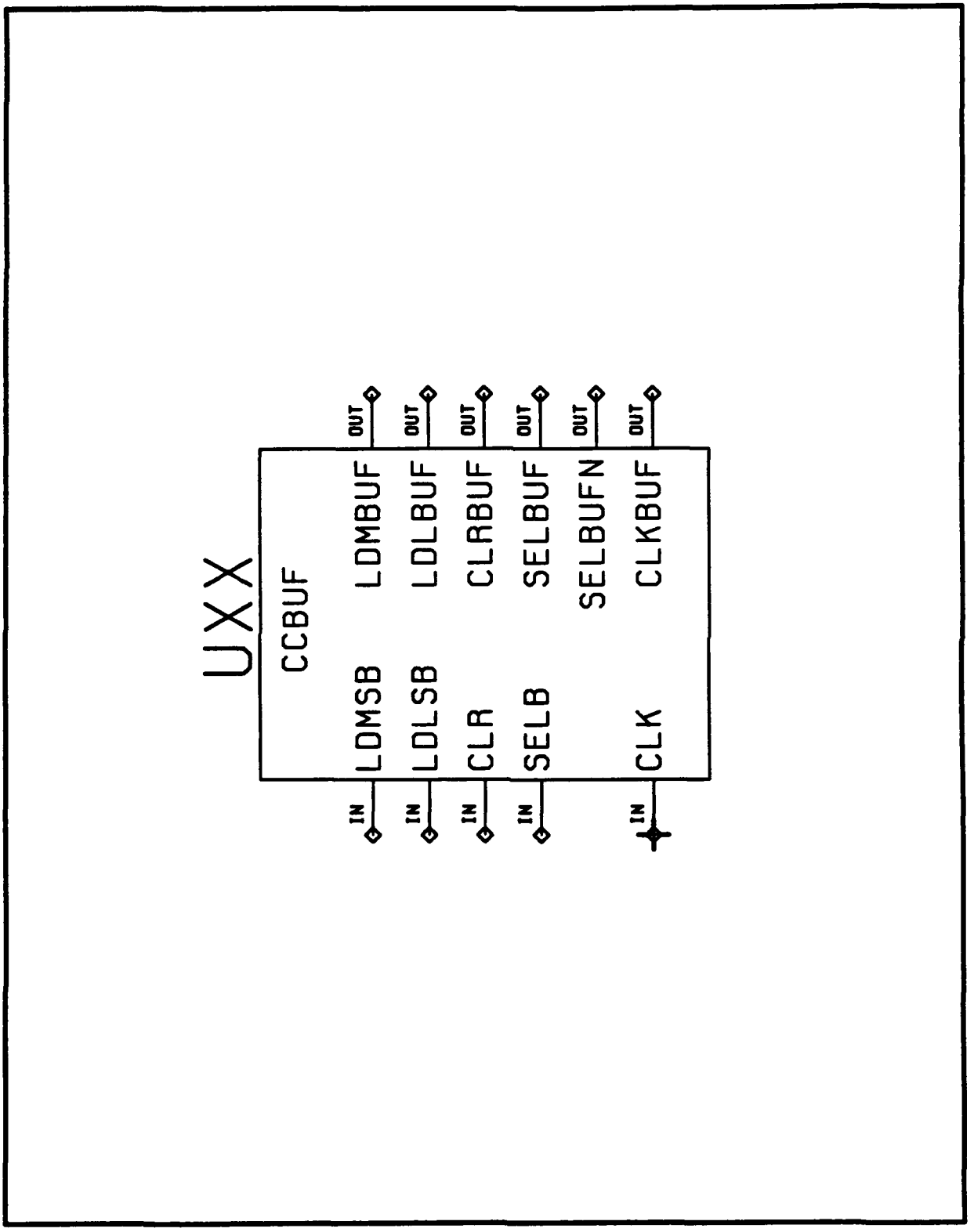


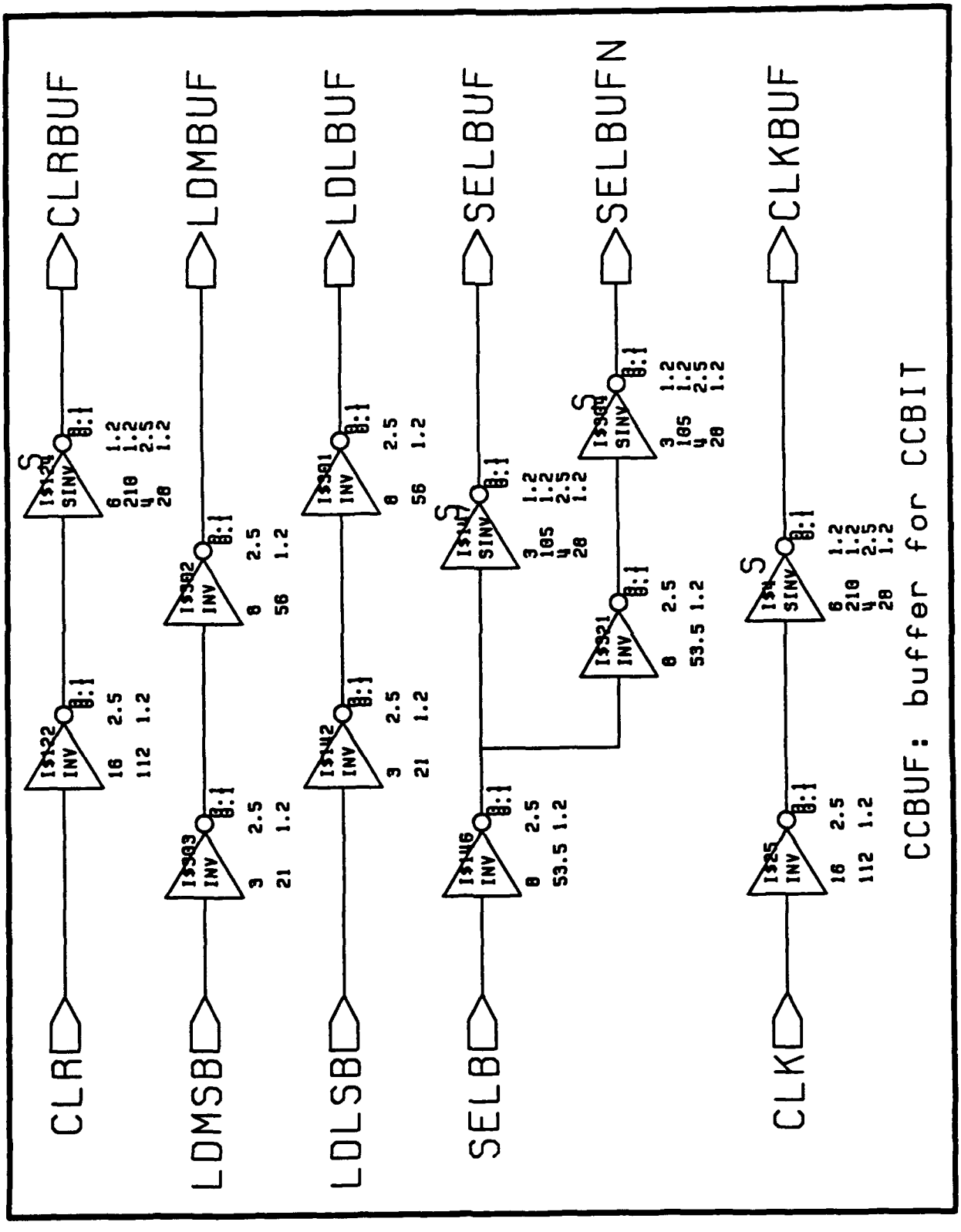

UXX
CC
In
B(7:0)
In
A(7:0)
Q(7:0)
out
CLK
SELB
LOMSB
LOLSB
CLR
In
In
In
In
In


FOR I := 4 TO 7
U2
CCBIT
CLR
DA
DB
SAN
SBN
LO
CLK
Q(I)
A(I)
B(I)
SAN
SBN
LDMBUF
CLKBUF
CLRBUF
FOR I := 0 TO 3
U3
CCBIT
CLR
DA
DB
SAN
SBN
LO
CLK
Q(I)
A(I)
B(I)
SAN
SBN
LDLBUF
CLKBUF
CLRBUF
U1
CCBUF
LDMSB
LDLSB
CLR
SELB
CLK
LDMBUF
LDLBUF
CLRBUF
SELBUF
SELBUFN
CLKBUF
LDMBUF
LDLBUF
CLRBUF
SAN
SBN
CLKBUF
LDMSB
LDLSB
CLR
SELB
CLK


OUT
Q
UXX
CCBIT
CLR
NI
DA
DB
SAN
SBN
LD
CLK
IN
IN
IN
IN
IN
IN


CCBIT: mux + reg w/ synchronous clr
Q
CLR
CLK
LD
SA
SB

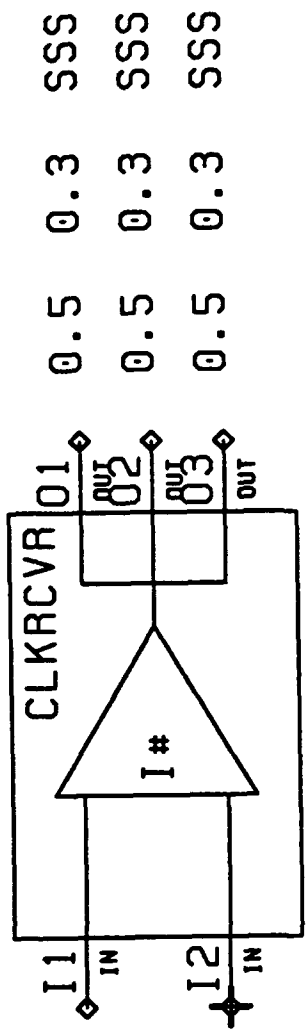

UXX
CCBUF
LDMSB
LDLSB
CLR
SELB
CLK
LDMBUF
LDLBUF
CLRBUF
SELBUF
SELBUFN
CLKBUF
IN
IN
IN
IN
IN
OUT
OUT
OUT
OUT
OUT
OUT


CLRBUF
LDMBUF
LDLBUF
SELBUF
SELBUFN
CLKBUF
CLR
LDMSB
LDLSB
SELB
CLK
CCBUF: buffer for CCBIT

MPY LIBRARY

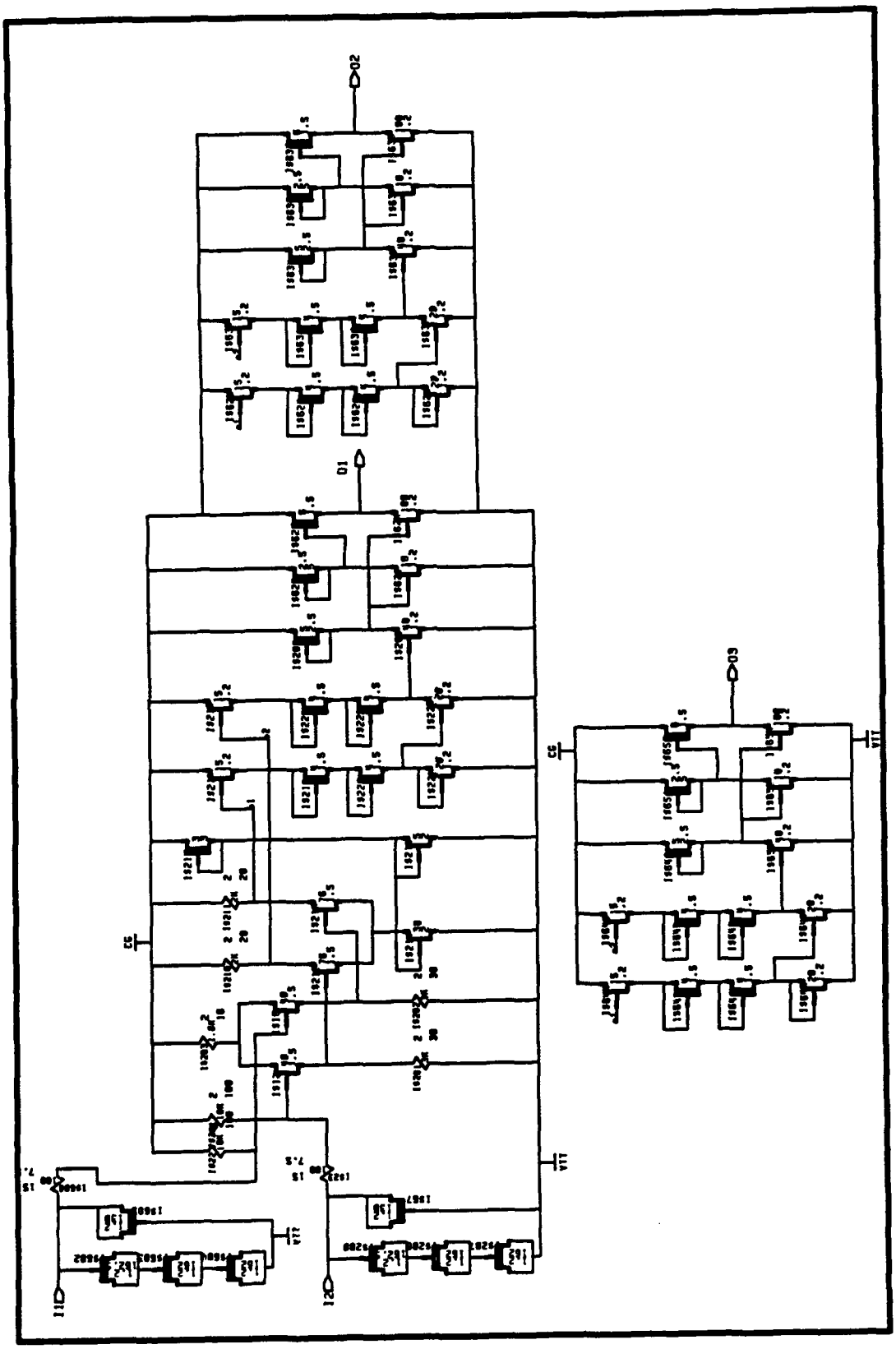
NAME: CLKRCVR FOR MPY

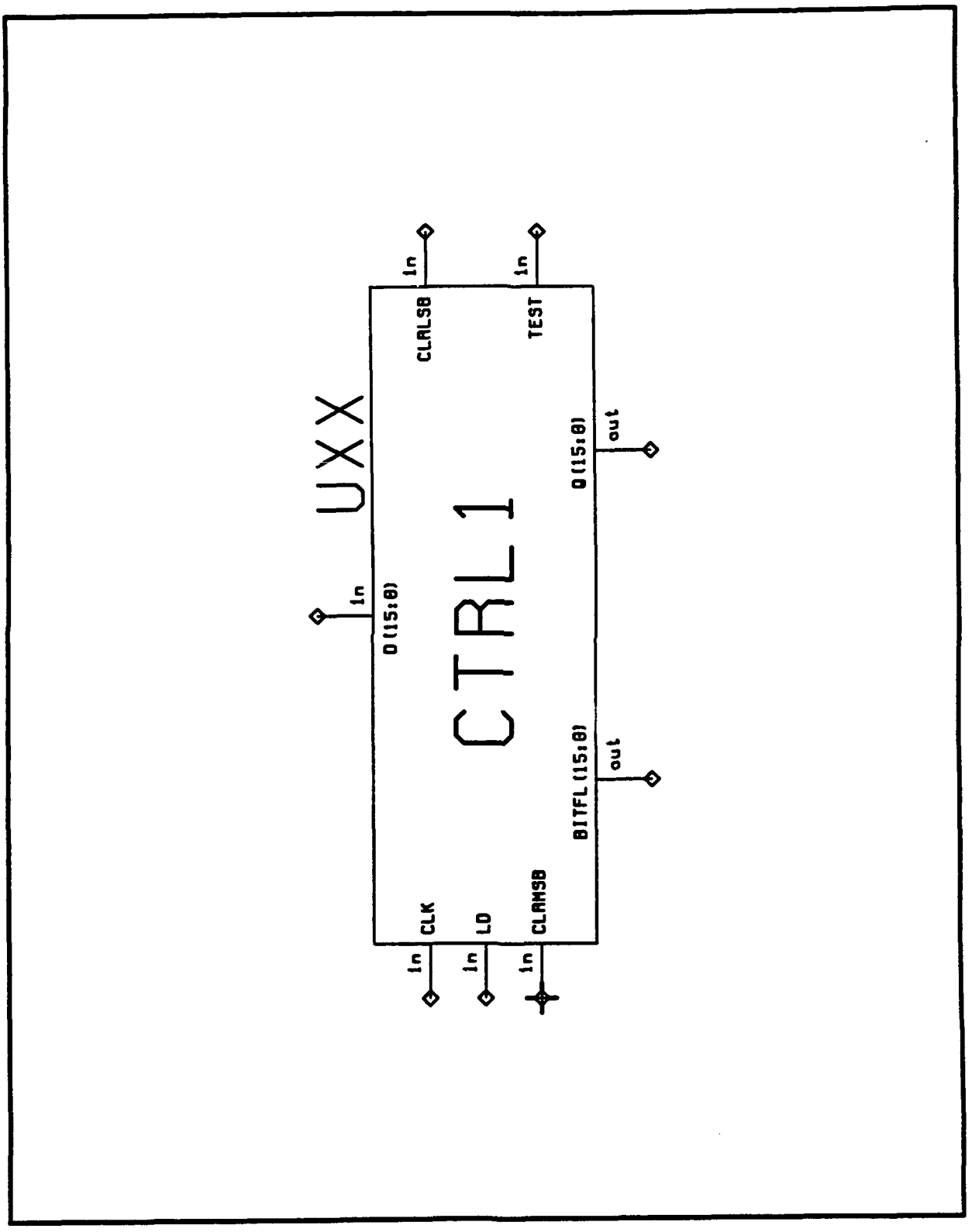
DESCRIPTION: DIFFERENTIAL INPUT CLOCK RECEIVER

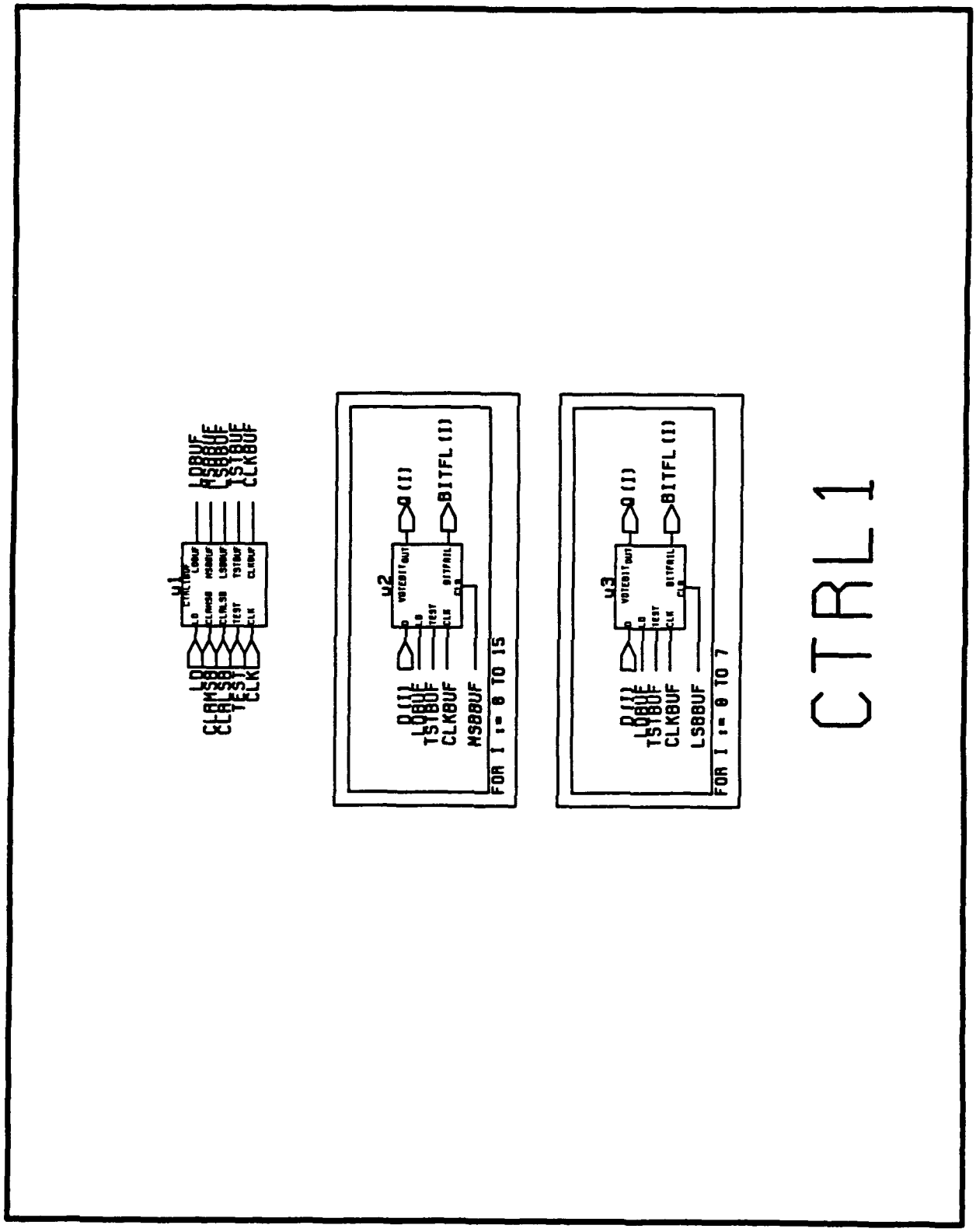


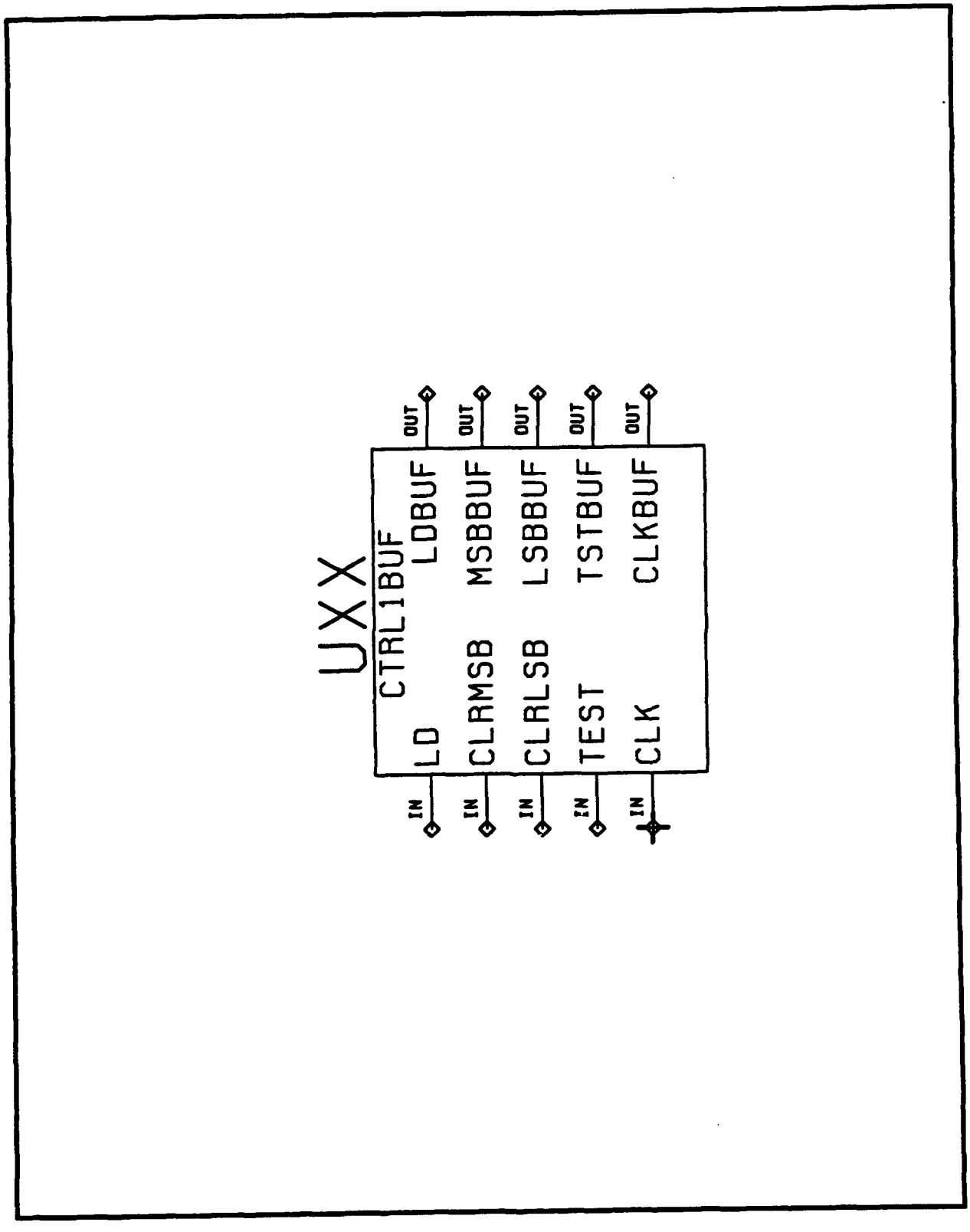
CLKRCVR

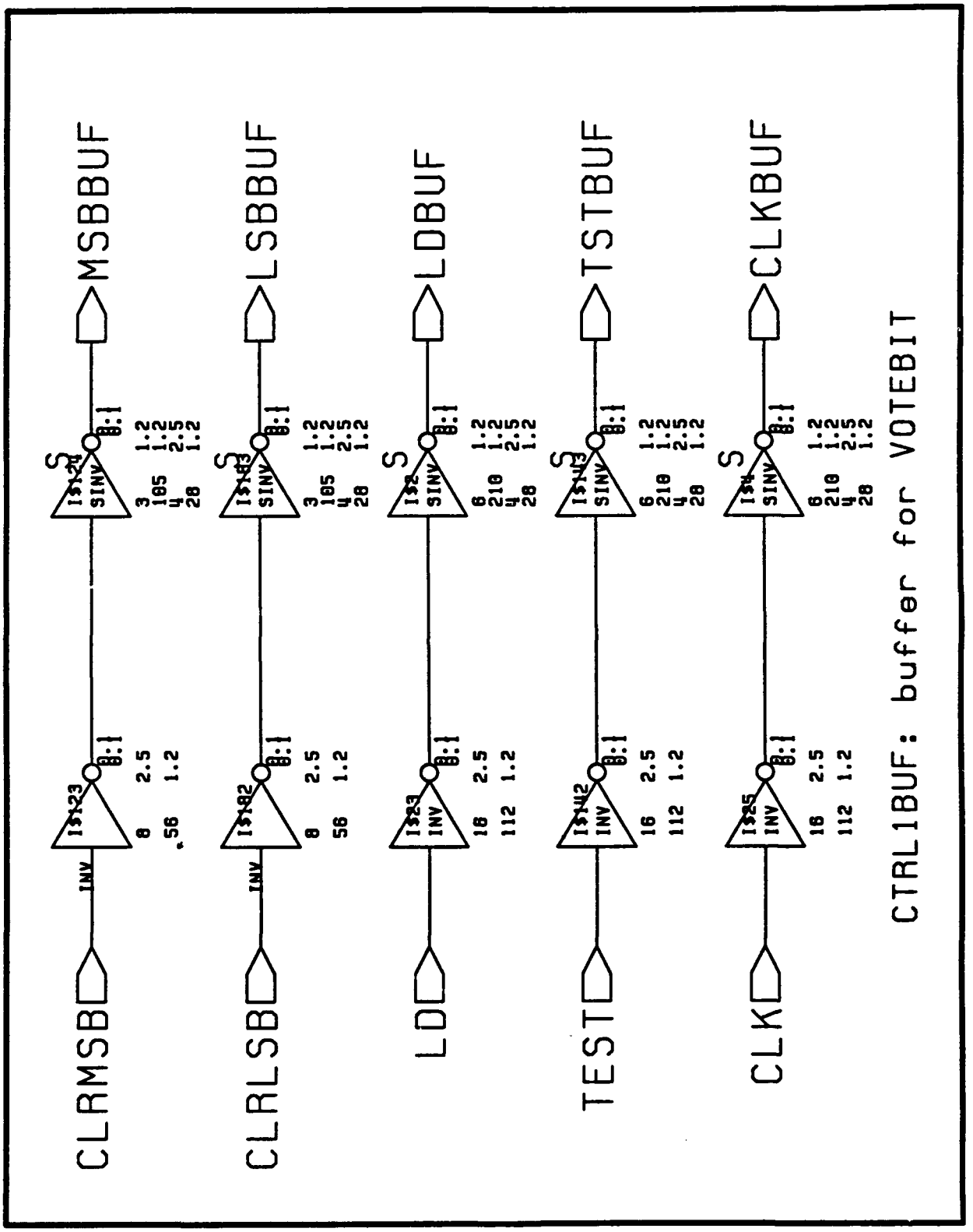
clkrcvr.bin

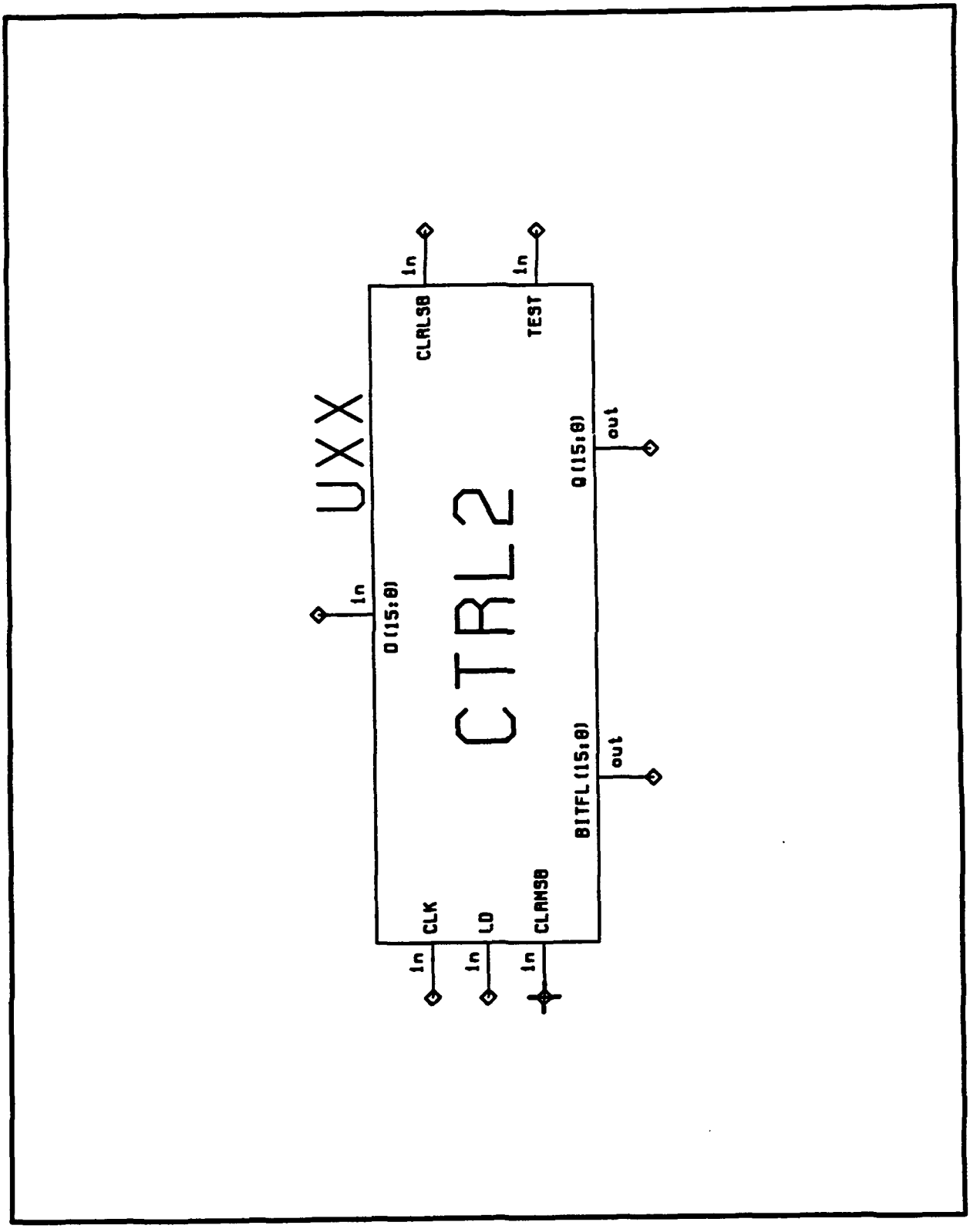


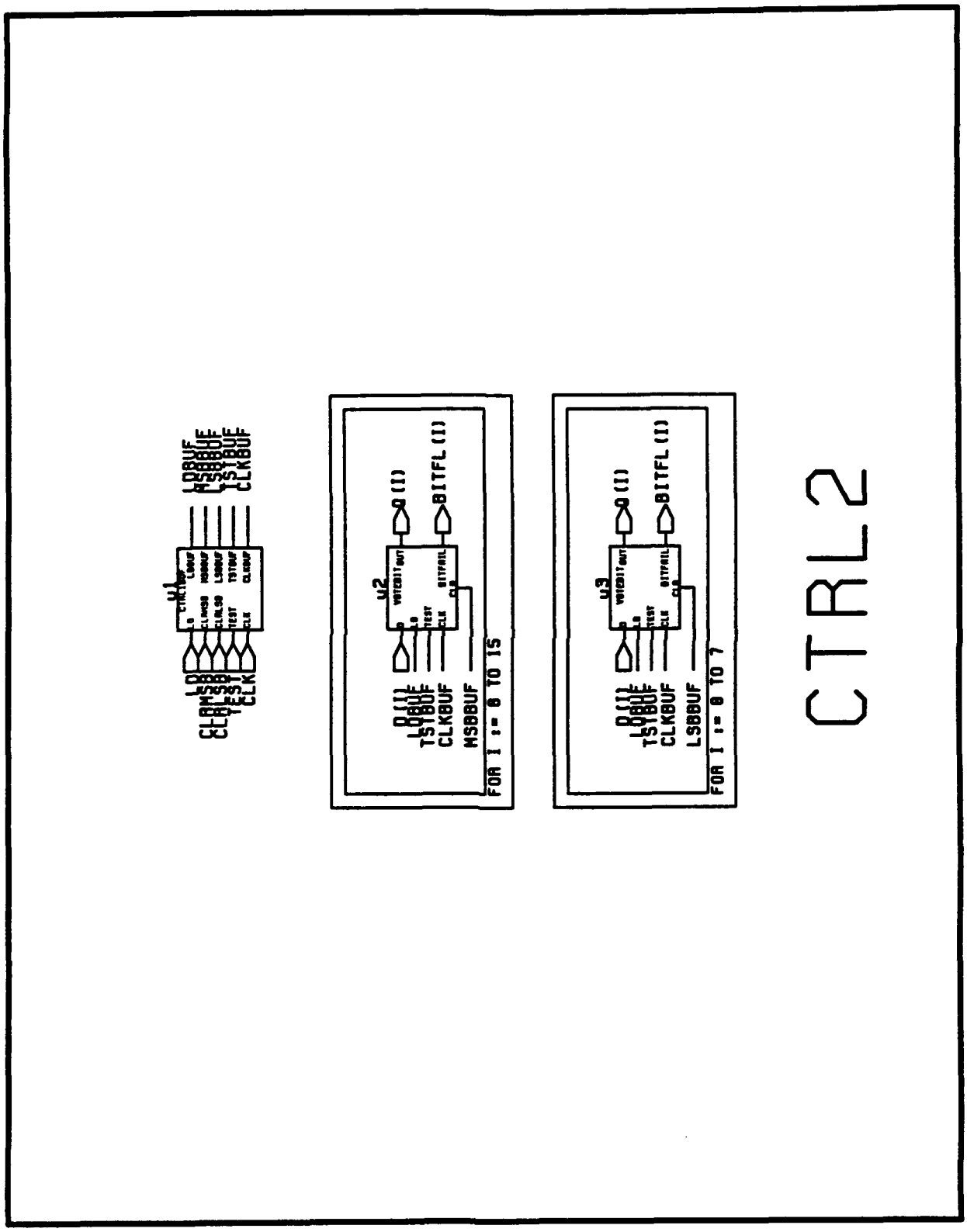

UXX
CTRL 1
in
D(15:0)
in
CLRLSB
in
TEST
out
Q(15:0)
out
BITFL(15:0)
in
CLK
in
LD
in
CLRMSB

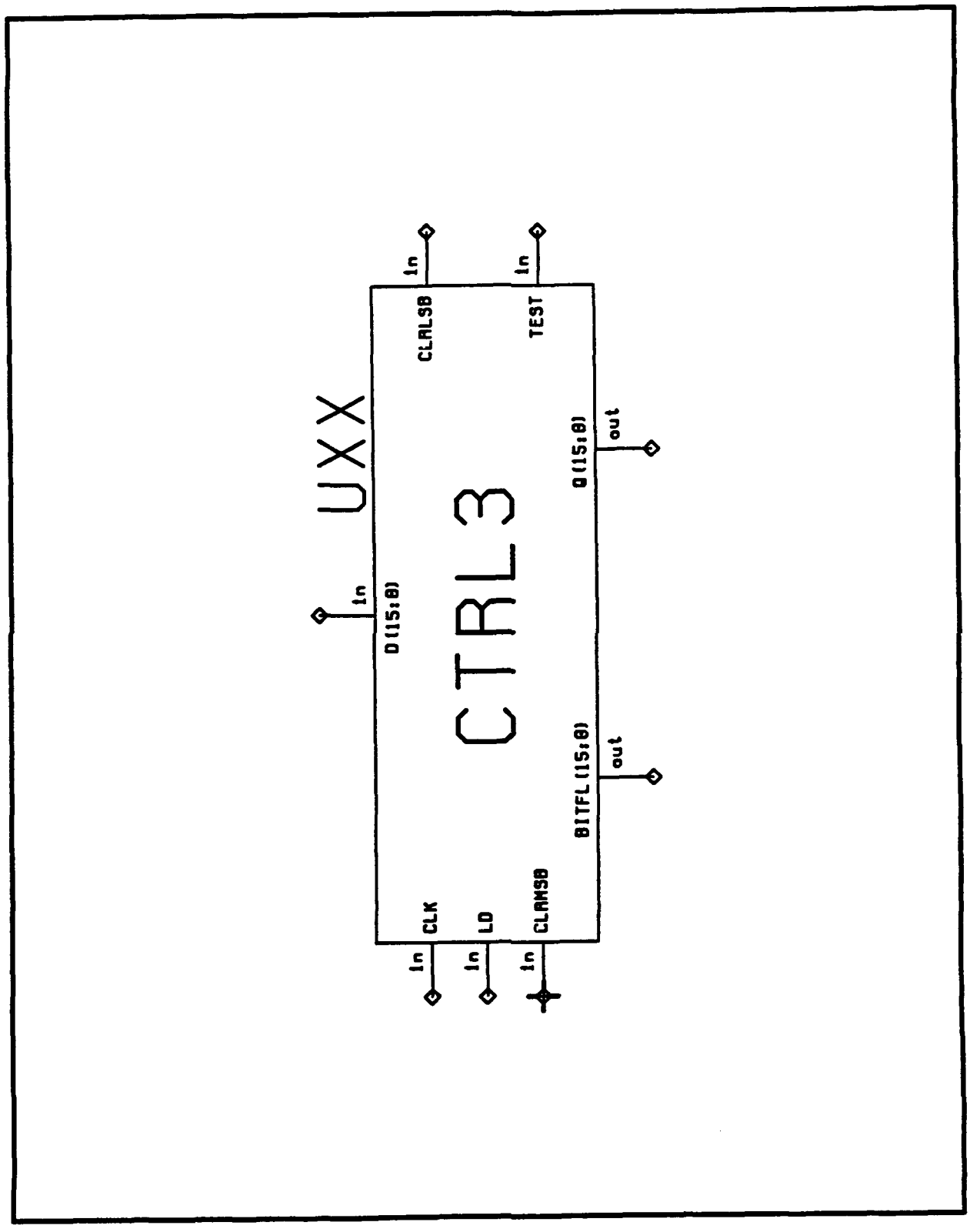

CTRL1
U1
LDBUF
MSBBUF
LSBBUF
TSTBUF
CLKBUF
LD
CLRMSB
CLRLSB
TEST
CLK
U2
D (I)
BITFL (I)
LDBUF
TSTBUF
CLKBUF
MSBBUF
FOR I := 0 TO 15
U3
D (I)
BITFL (I)
LDBUF
TSTBUF
CLKBUF
LSBBUF
FOR I := 0 TO 7

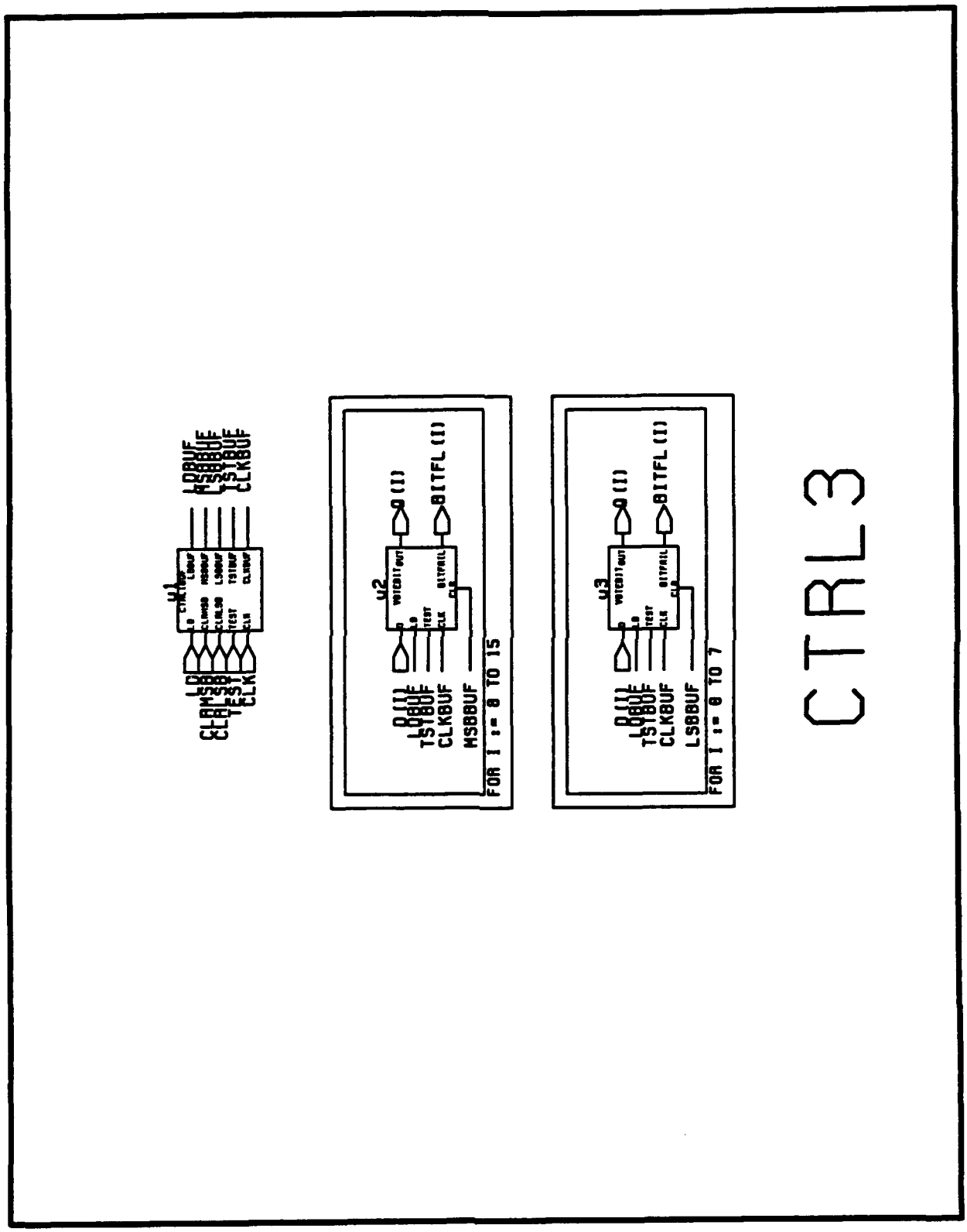

UXX
CTRL1BUF
LDBUF
MSBBUF
LSBBUF
TSTBUF
CLKBUF
LD
CLRMSB
CLRLSB
TEST
CLK
IN
IN
IN
IN
IN
OUT
OUT
OUT
OUT
OUT

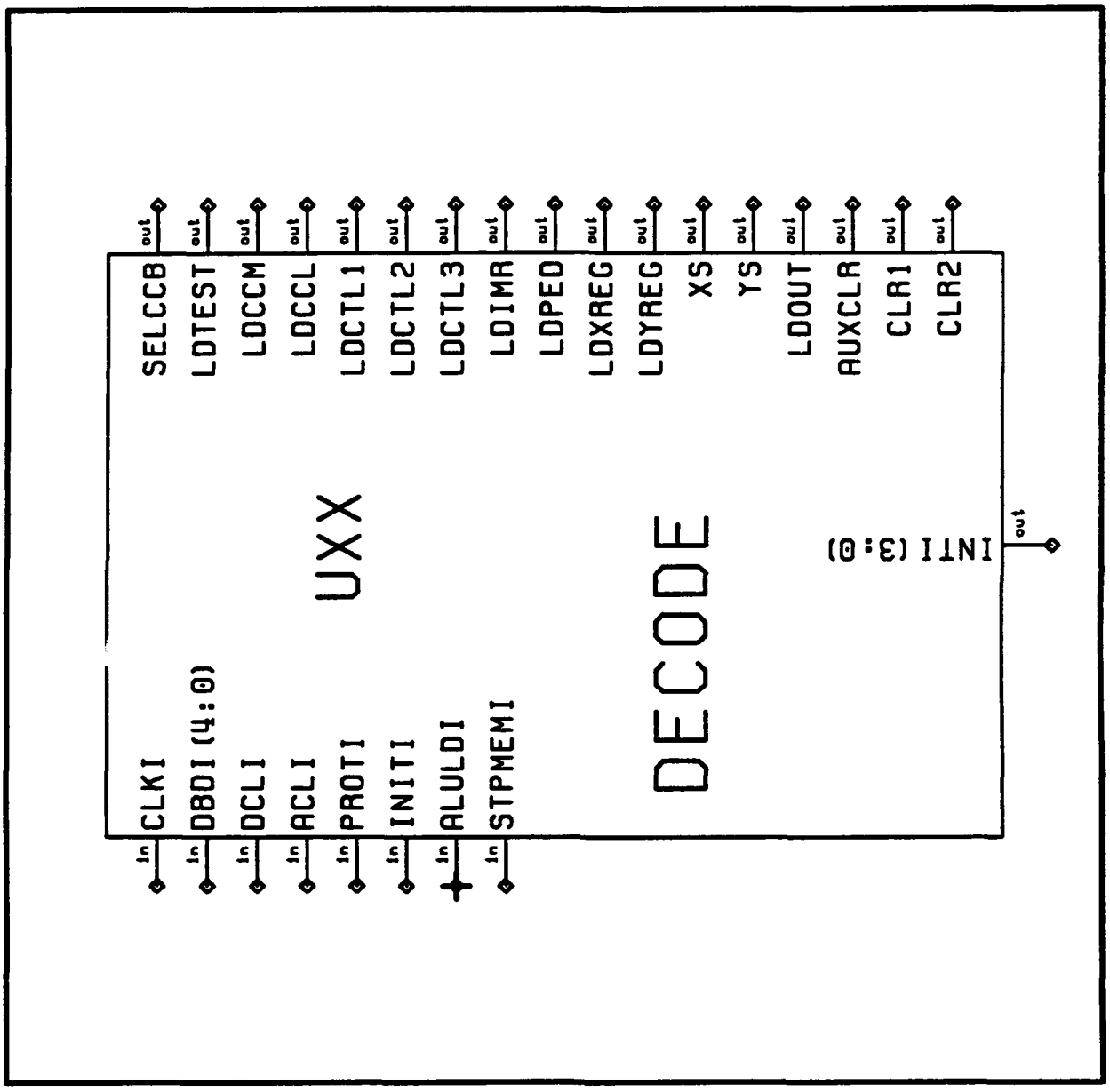

CTRL1BUF: buffer for VOTEBIT
CLRMSB
CLRLSB
LD
TEST
CLK
MSBBUF
LSBBUF
LDBUF
TSTBUF
CLKBUF
INV
SINV
8:1
S

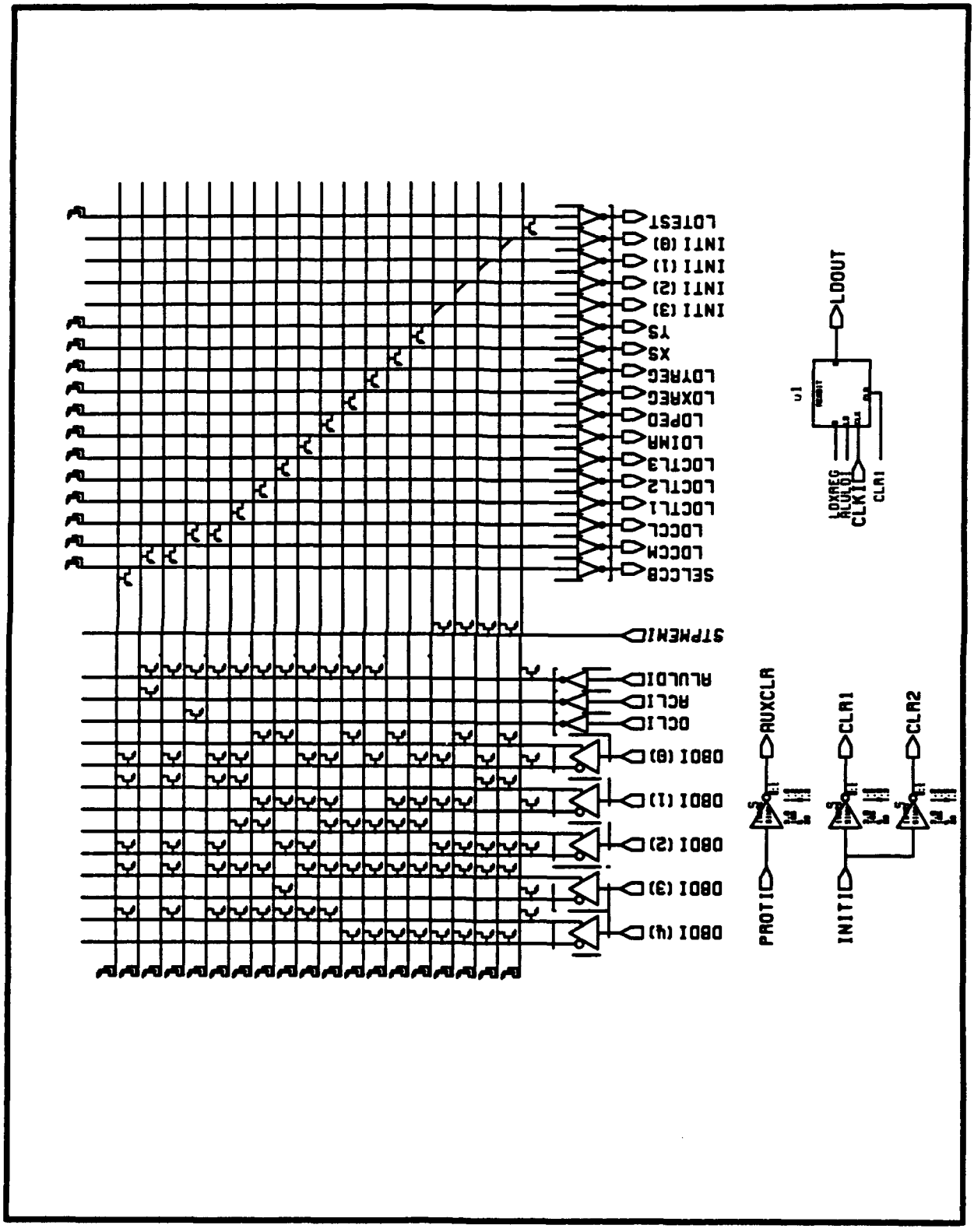

UXX
CTRL2
In
CLRLSB
In
TEST
Q(15:0)
out
In
D(15:0)
BITFL(15:0)
out
In
CLK
In
LD
In
CLRMSB

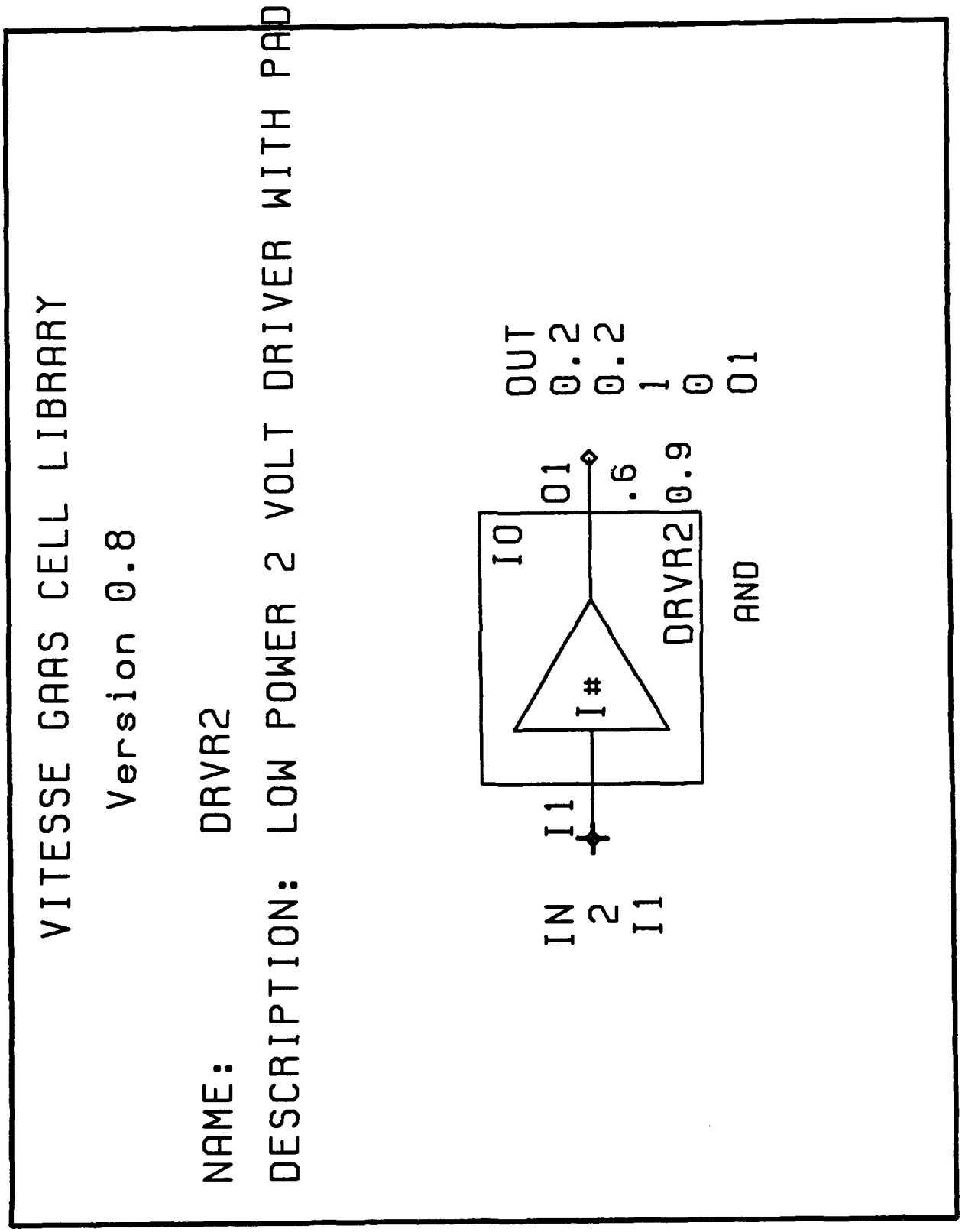

CTRL2
u1
LDBUF
MSBBUF
TSTBUF
CLKBUF
LD
MSB
TEST
CLK
u2
D (I)
BITFL (I)
R (I)
LDBUF
TSTBUF
CLKBUF
MSBBUF
FOR I := 0 TO 15
u3
D (I)
BITFL (I)
R (I)
LDBUF
TSTBUF
CLKBUF
LSBBUF
FOR I := 0 TO 7

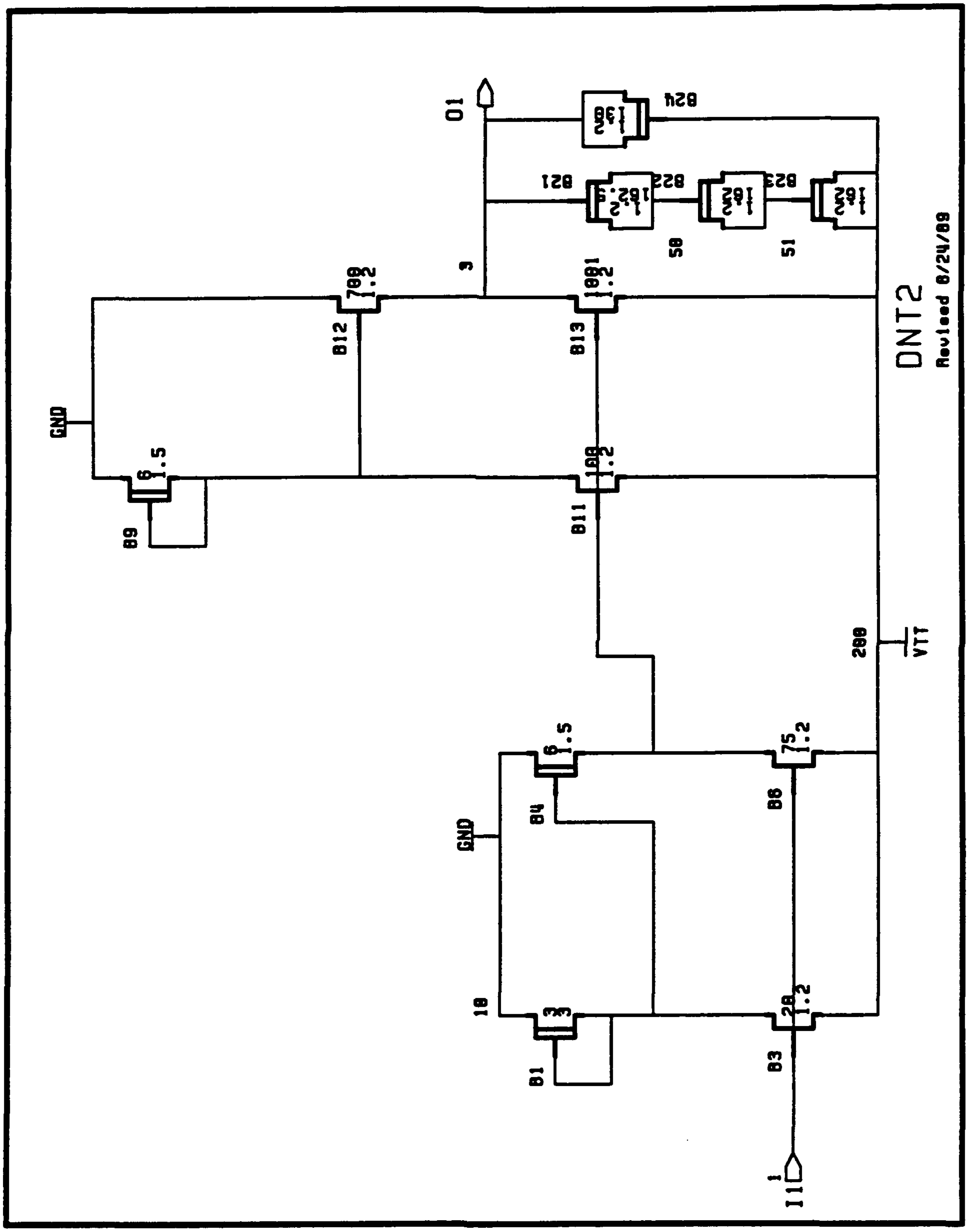

UXX
CTRL3
In
CLRLSB
In
TEST
Q(15:0)
out
In
D(15:0)
BITFL(15:0)
out
CLK
LD
CLRMSB
In
In
In

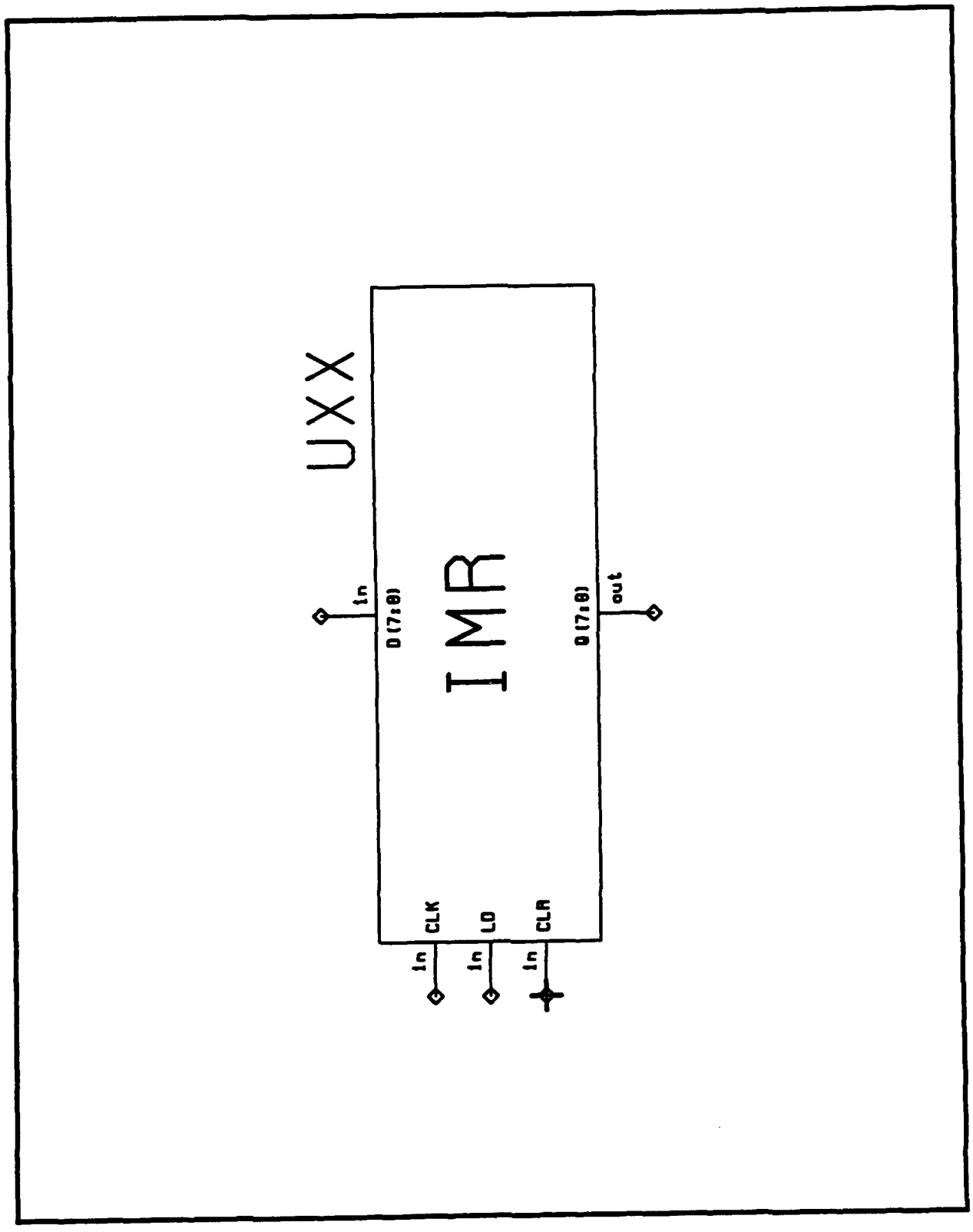

CTRL3
u1
LDBUF
MSBBUF
LSBBUF
TSTBUF
CLKBUF
LD
CLAMSB
CLALSB
TEST
CLK
u2
D(I)
BITFL(I)
D(I)
LDBUF
TSTBUF
CLKBUF
MSBBUF
FOR I := 0 TO 15
u3
D(I)
BITFL(I)
D(I)
LDBUF
TSTBUF
CLKBUF
LSBBUF
FOR I := 0 TO 7

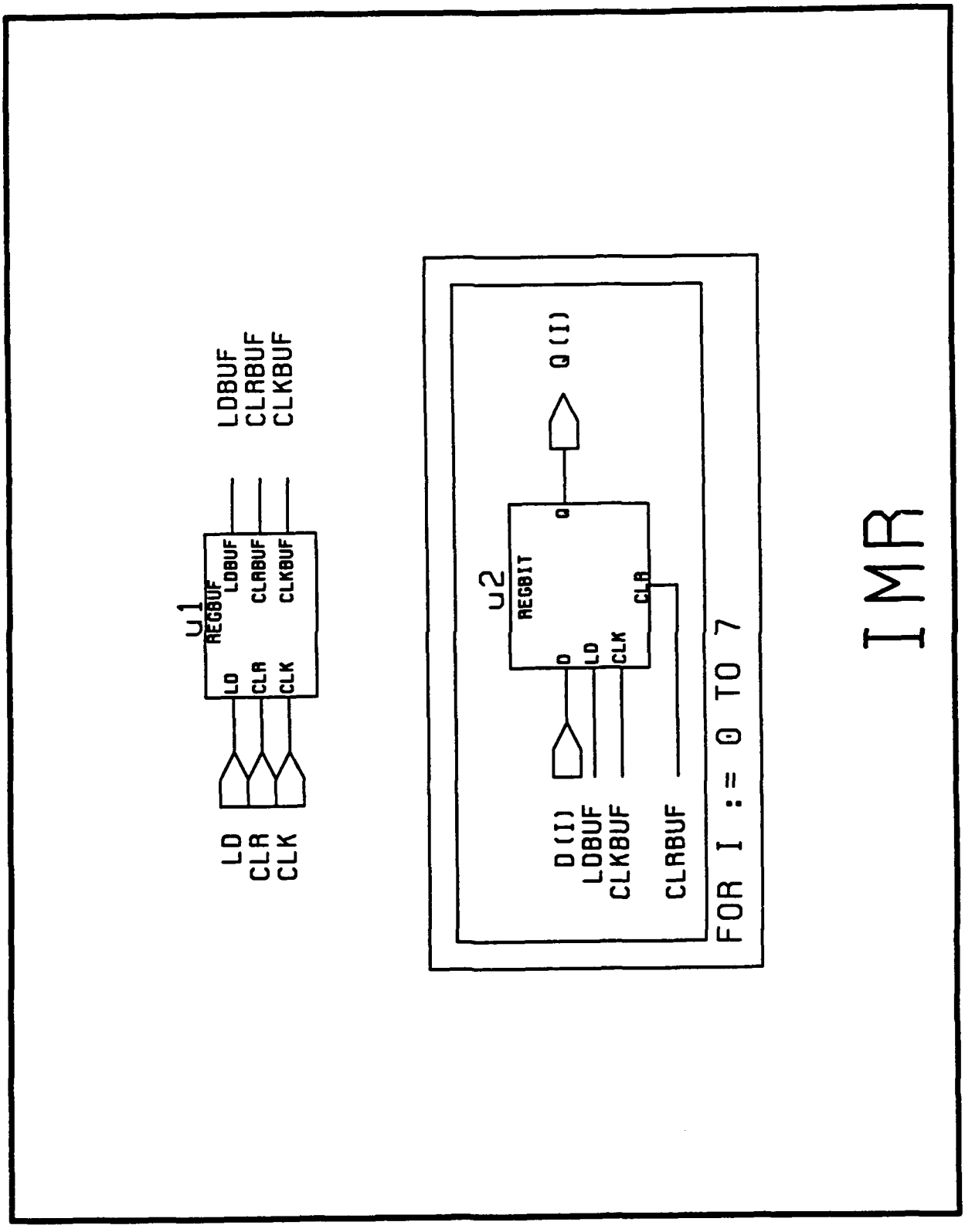

DECODE
UXX
CLKI
DBDI(4:0)
DCLI
ACLI
PROTI
INITI
ALULDI
STPMEMI
SELCCB
LDTEST
LDCCM
LDCCL
LDCTL1
LDCTL2
LDCTL3
LDIMR
LDPED
LDXREG
LDYREG
XS
YS
LDOUT
AUXCLR
CLR1
CLR2
INTI(3:0)

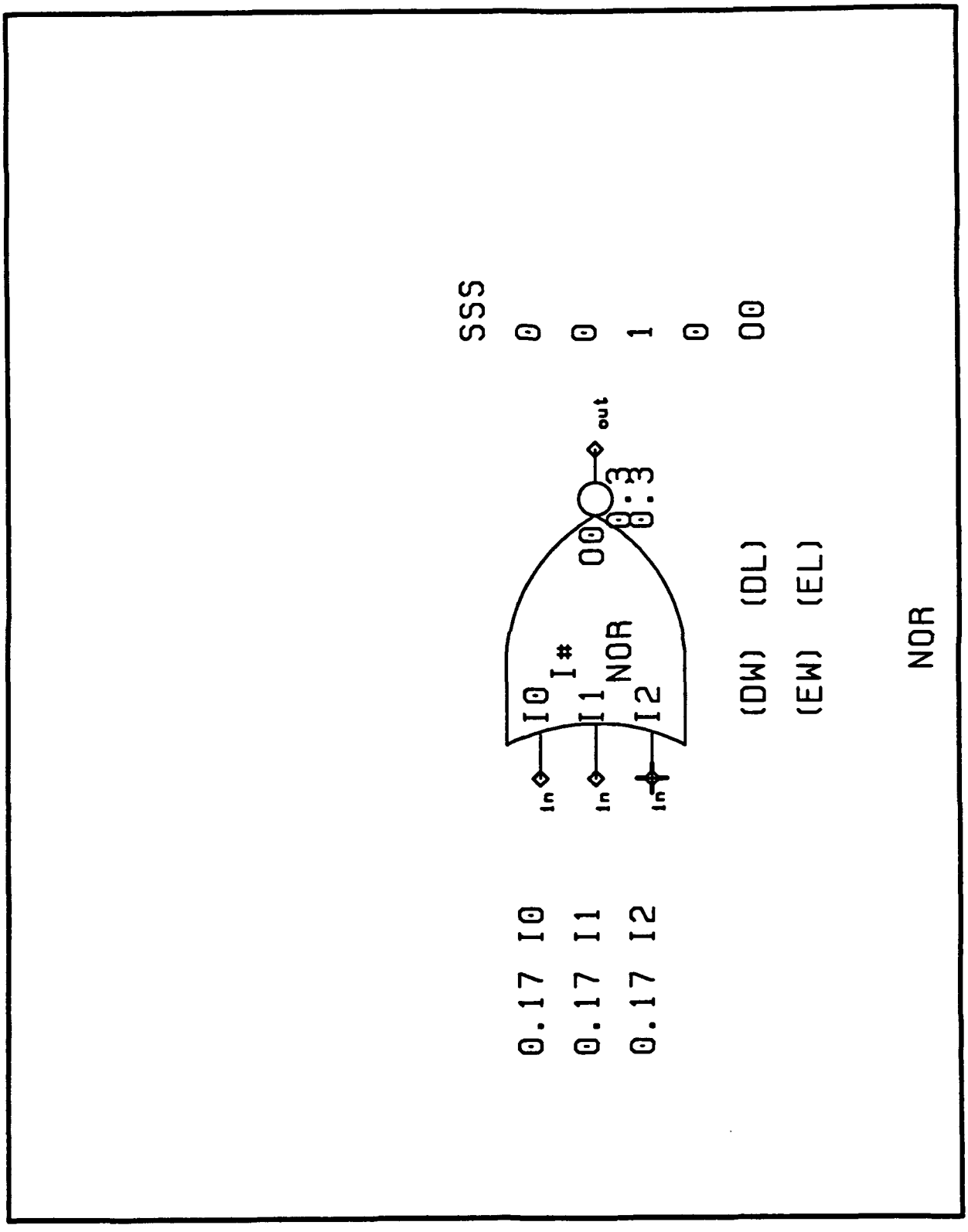

LOTEST
INTI (0)
INTI (1)
INTI (2)
INTI (3)
YS
XS
LOYREG
LOXREG
LOPEO
LOIMR
LOCTL3
LOCTL2
LOCTL1
LOCCL
LOCCM
SELCCB
STPMEMI
RLULDI
RCLI
OCLI
OBOI (0)
OBOI (1)
OBOI (2)
OBOI (3)
OBOI (4)
LDOUT
u1
LOXREG
ALULDI
CLKI
CLRI
AUXCLR
CLR1
CLR2
PROTID
INITID

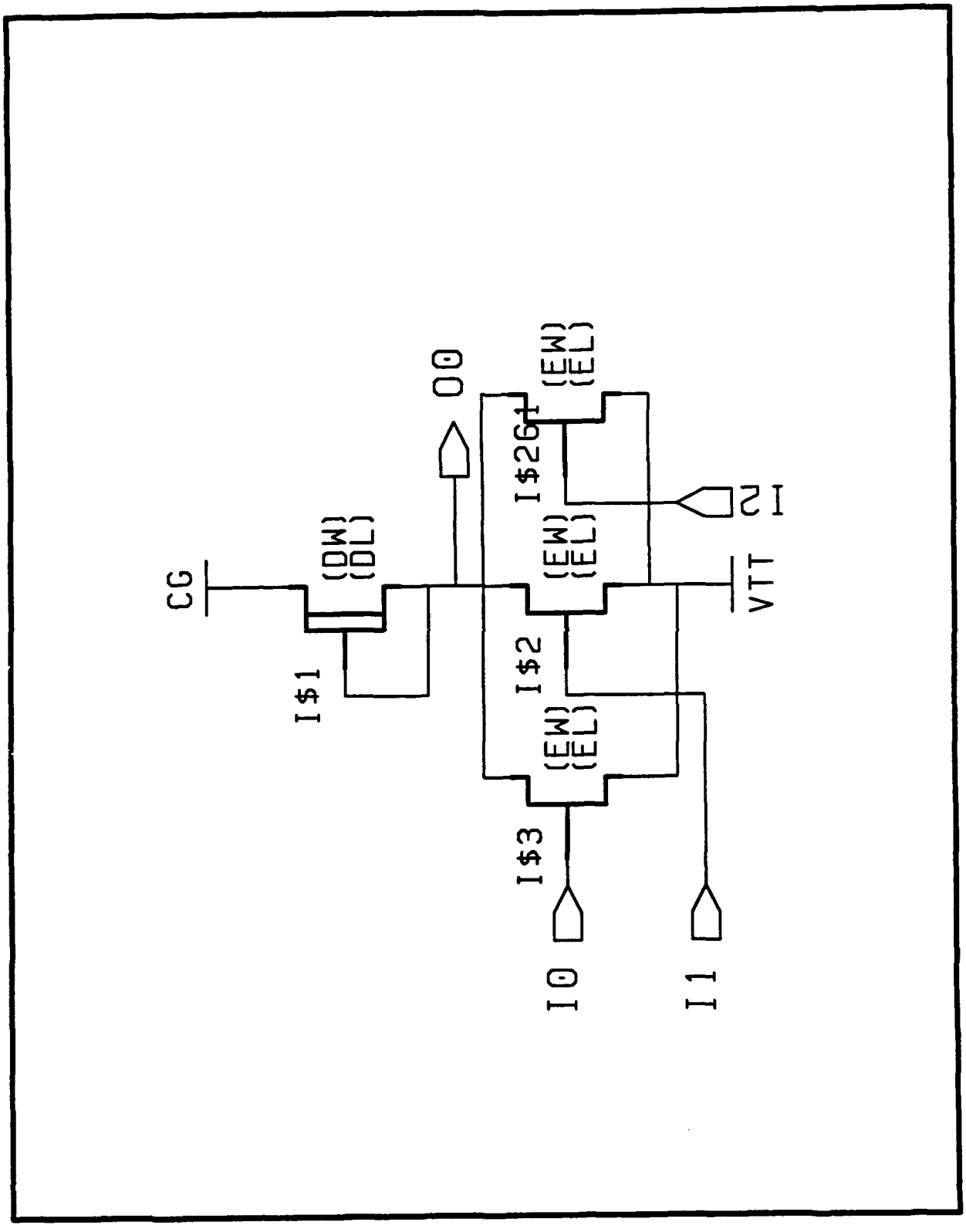

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: DRVR2
DESCRIPTION: LOW POWER 2 VOLT DRIVER WITH PAD
OUT
0.2
0.2
1
0
O1
IO
O1
.6
0.9
DRVR2
I#
AND
I1
IN
2
I1

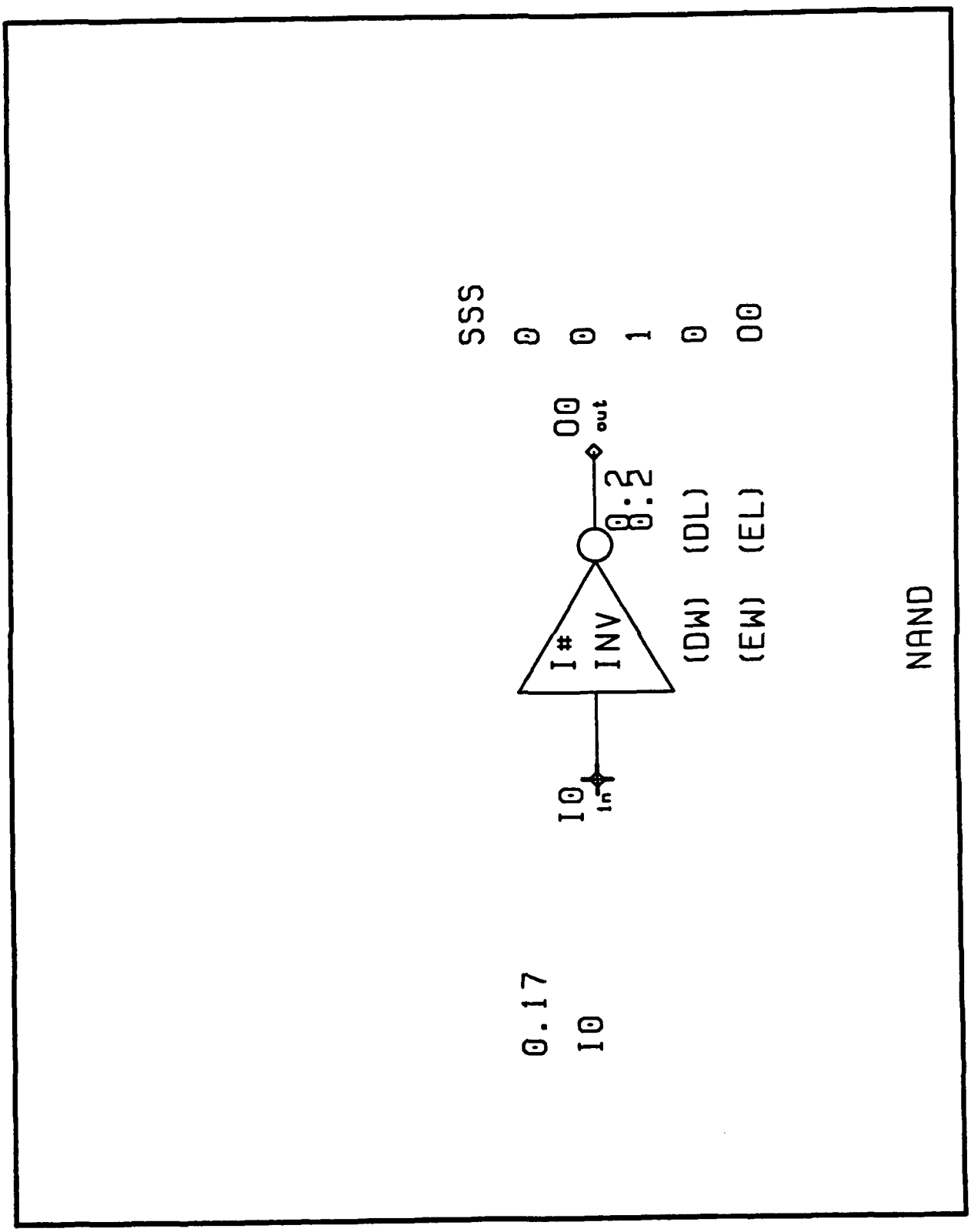

DNT2
Revised 8/24/89
GND
VTT
O1
I1

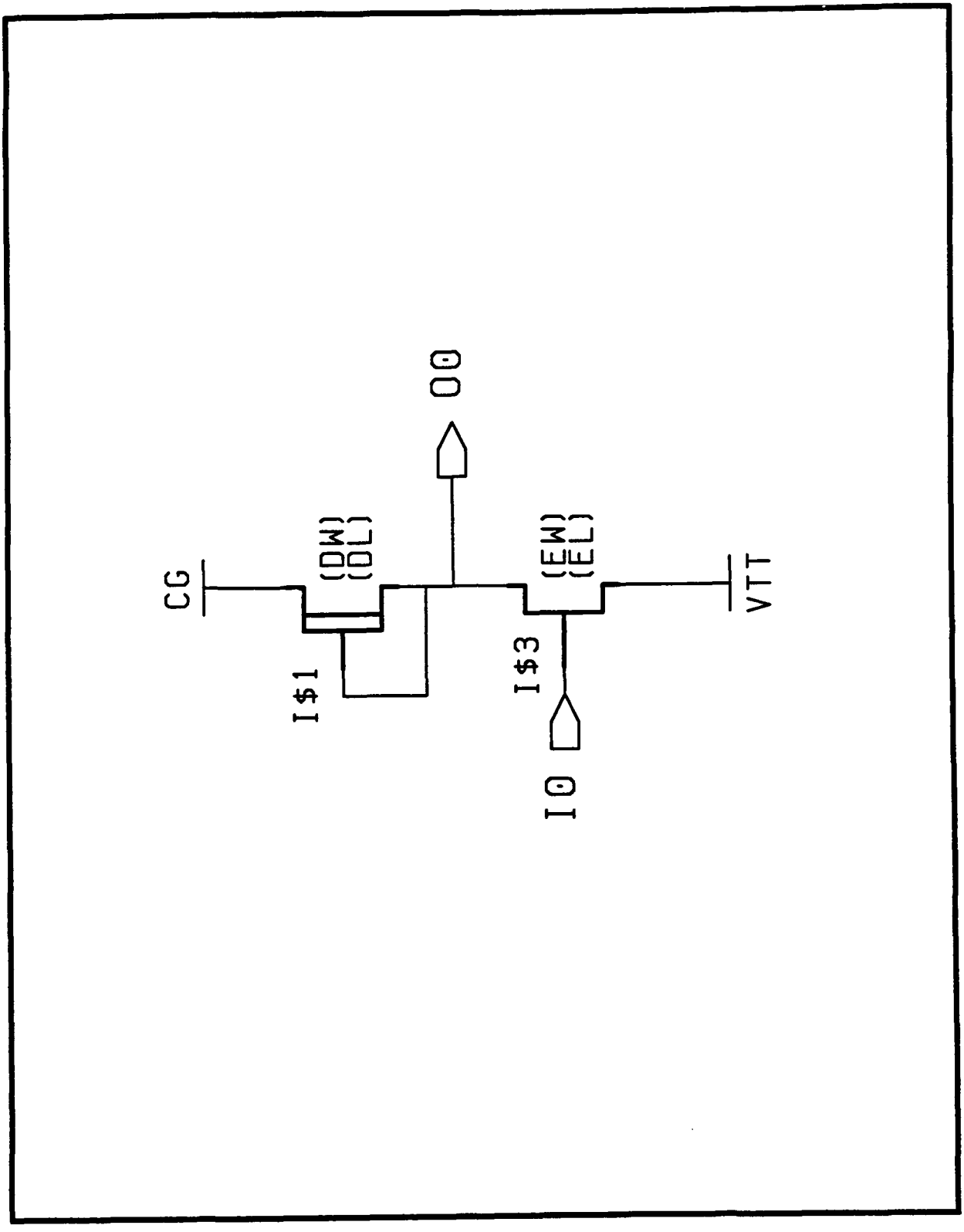

UXX
IMR
In
D(7:0)
D(7:0)
out
CLK
LD
CLR
In
In
In

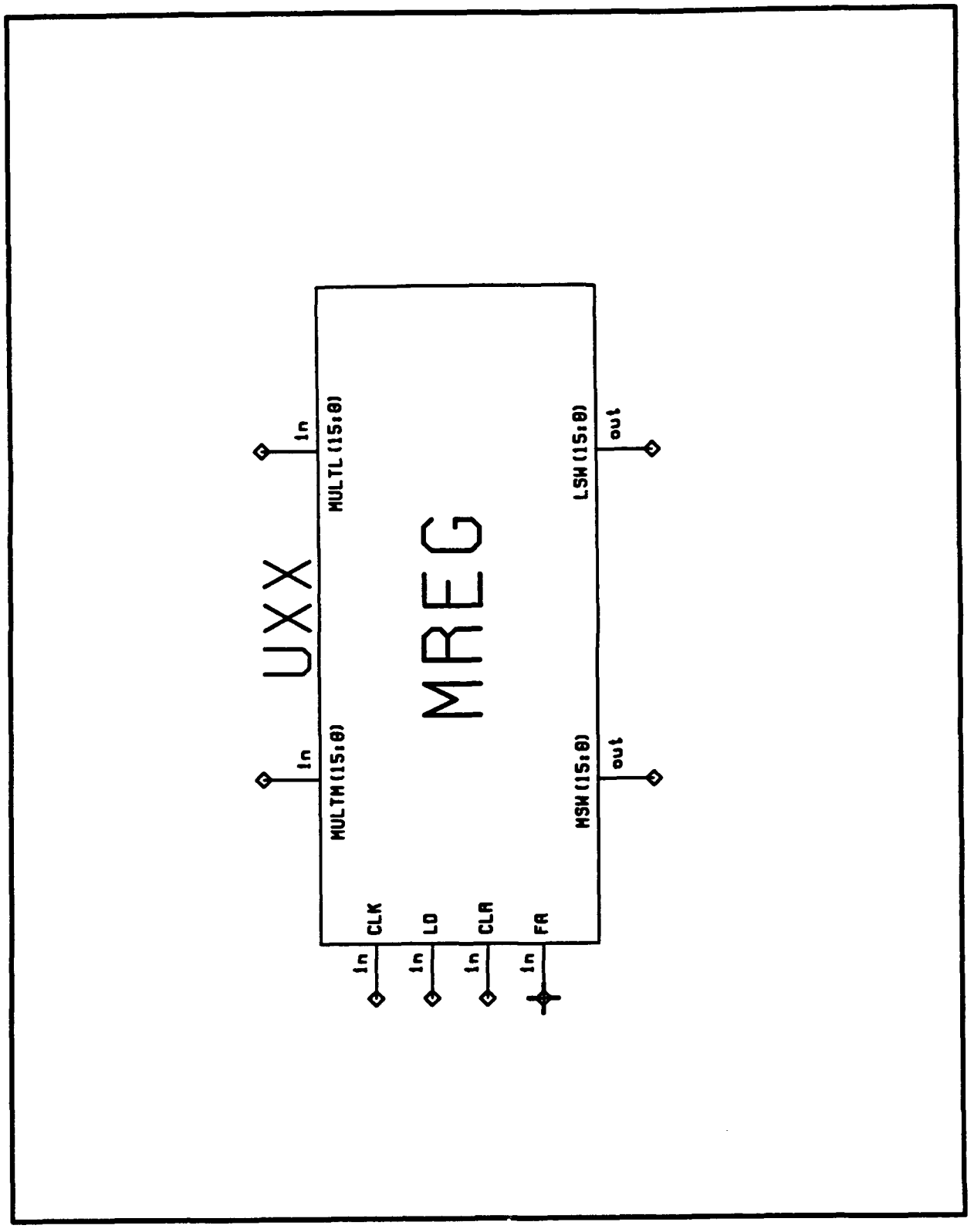

IMR
FOR I := 0 TO 7
u2
REGBIT
Q
D
LD
CLK
CLR
Q(I)
D(I)
LDBUF
CLKBUF
CLRBUF
u1
REGBUF
LDBUF
CLRBUF
CLKBUF
LD
CLR
CLK

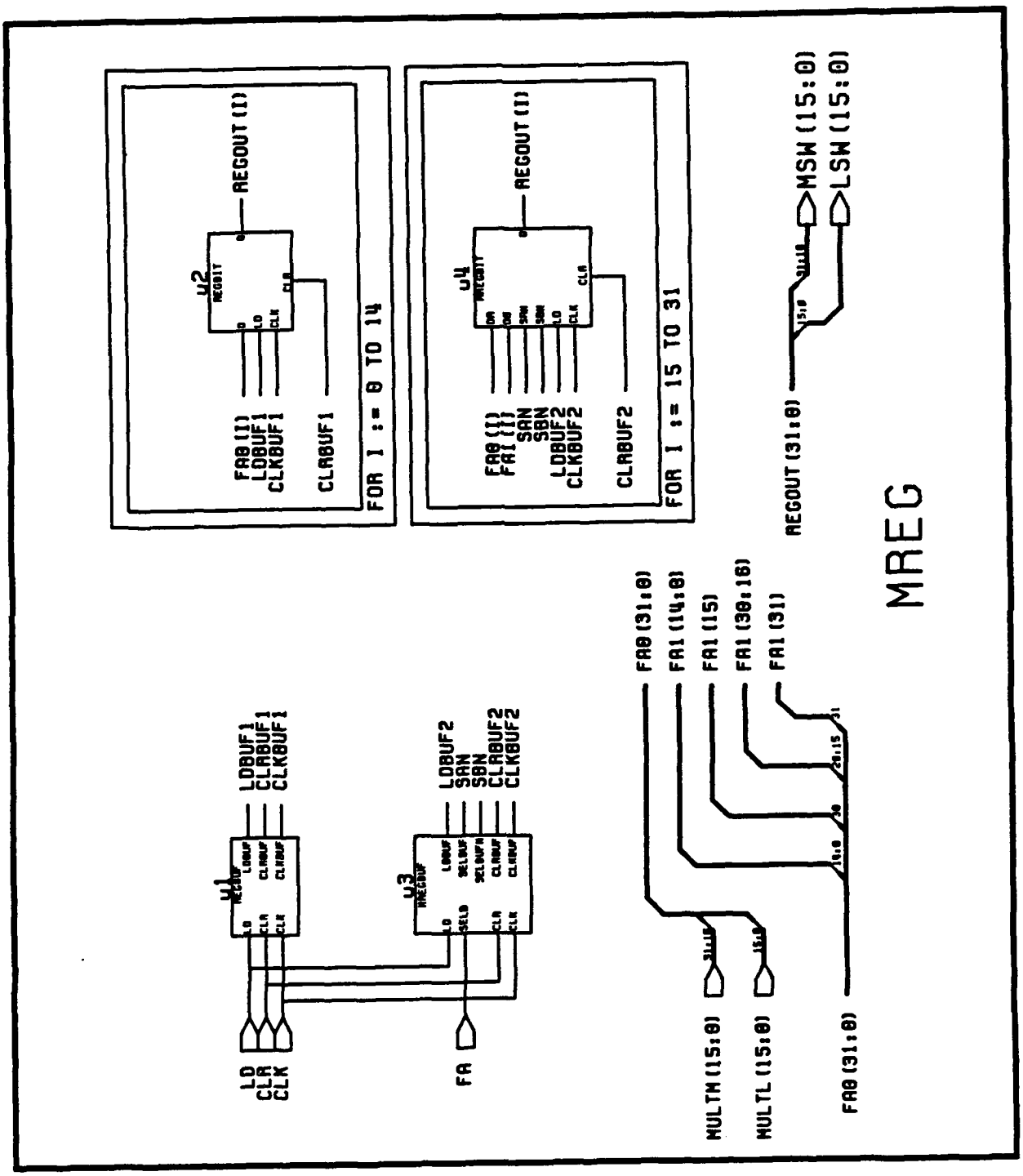

SSS
0
0
1
0
00
out
8.3
00
I0
I#
I1
NOR
I2
(DW) (DL)
(EW) (EL)
NOR
In
In
In
0.17 I0
0.17 I1
0.17 I2

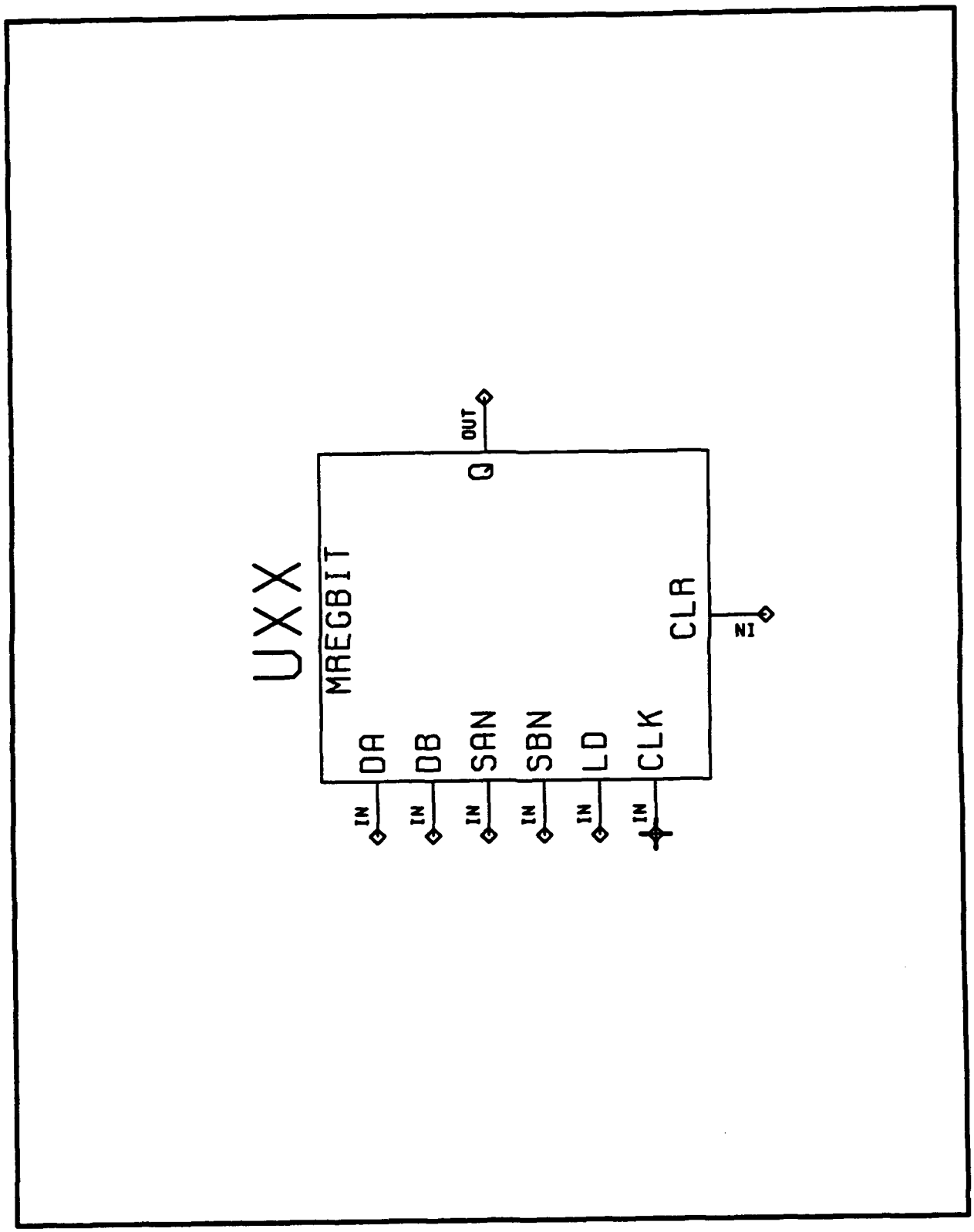

O0
(EW)
(EL)
I$26
I2
CG
(DW)
(DL)
(EW)
(EL)
VTT
I$1
I$2
(EW)
(EL)
I$3
I0
I1

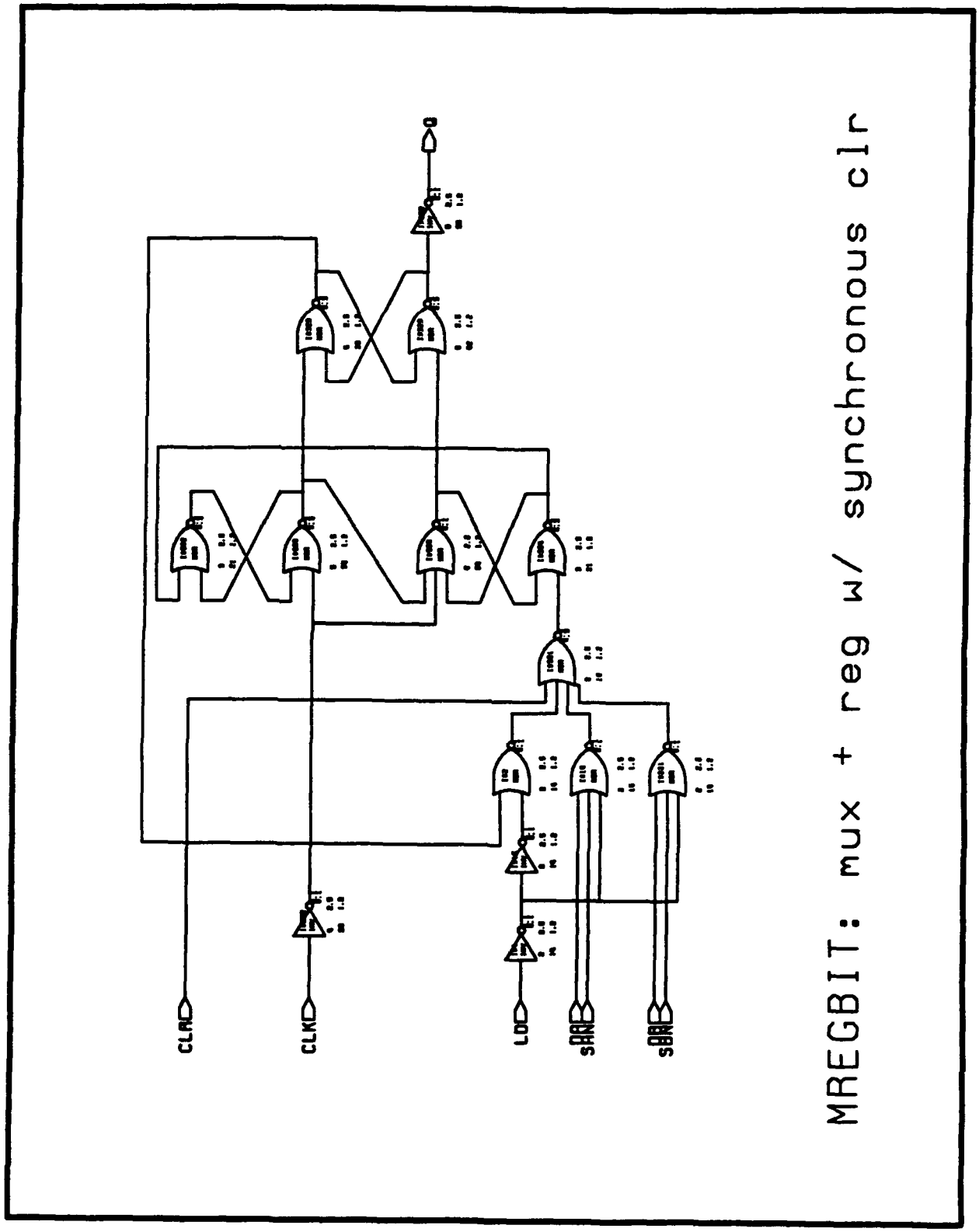

SSS
0 0 1 0 00
00
out
8.2
I#
INV
(DW) (DL)
(EW) (EL)
NAND
IO
in
0.17
IO

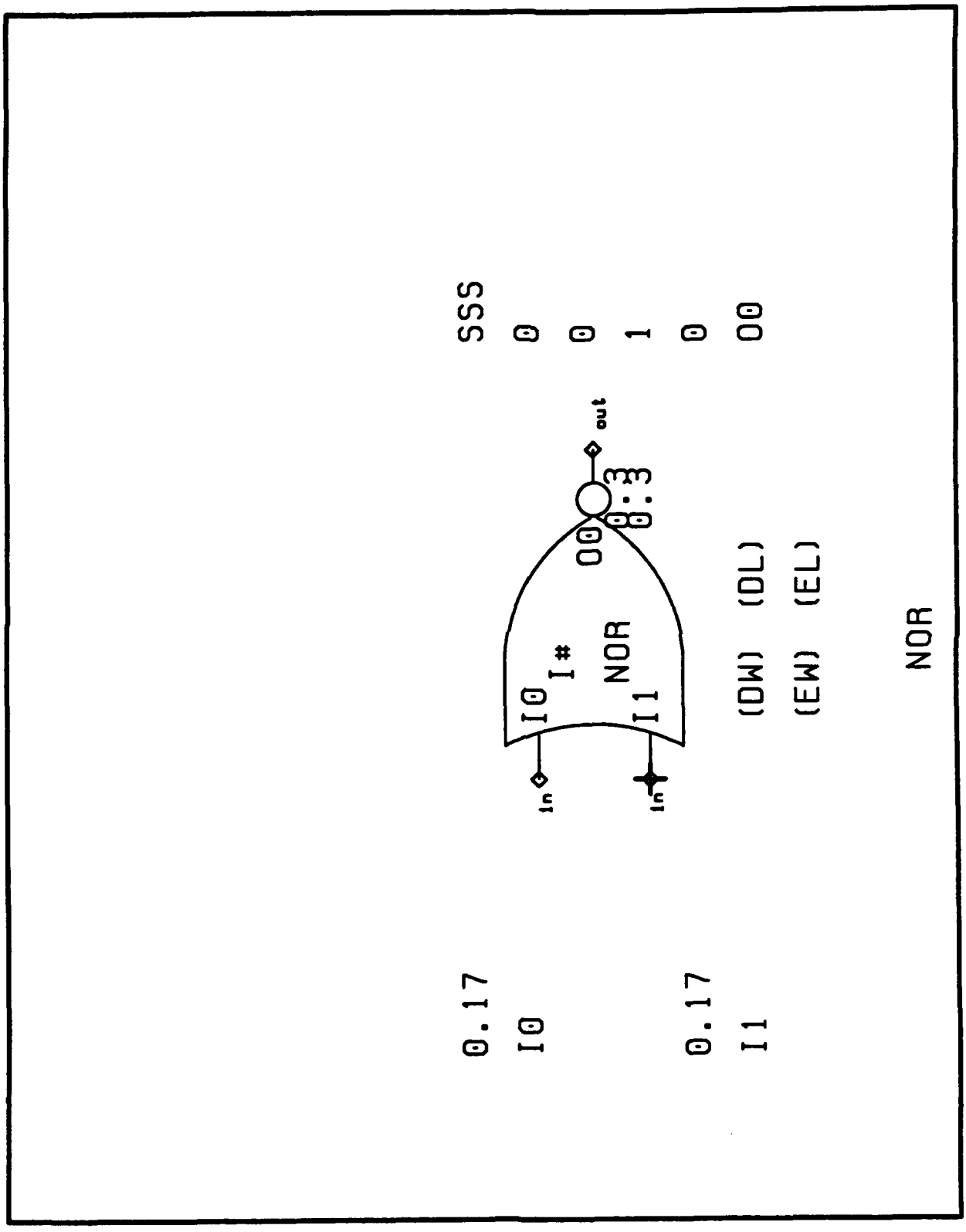

OO
CG
(DW)
(DL)
(EW)
(EL)
VTT
I$1
I$3
IO

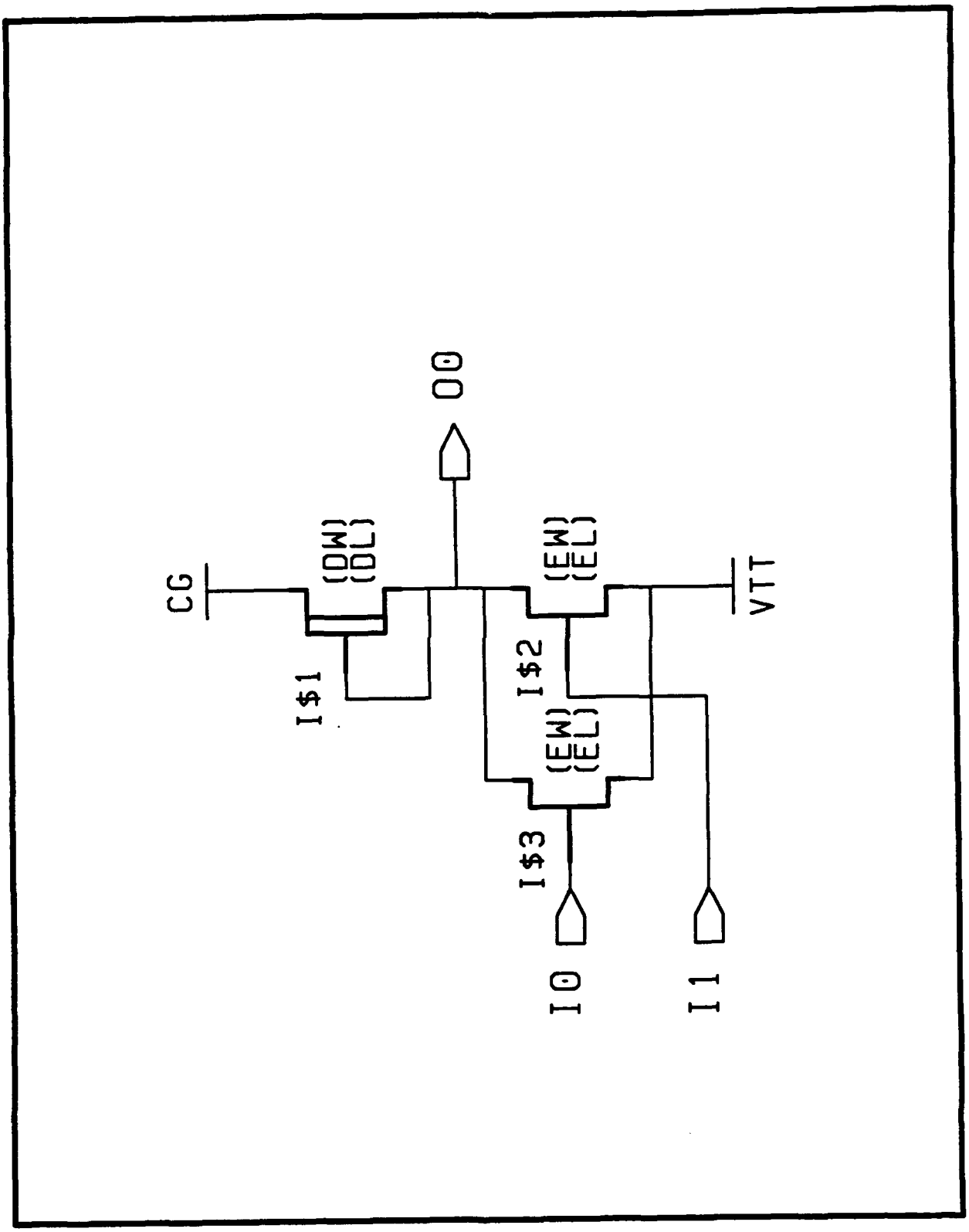

UXX
MREG
in
MULTL(15:0)
LSW(15:0)
out
in
MULTH(15:0)
MSW(15:0)
out
CLK
LD
CLR
FR
in
in
in
in

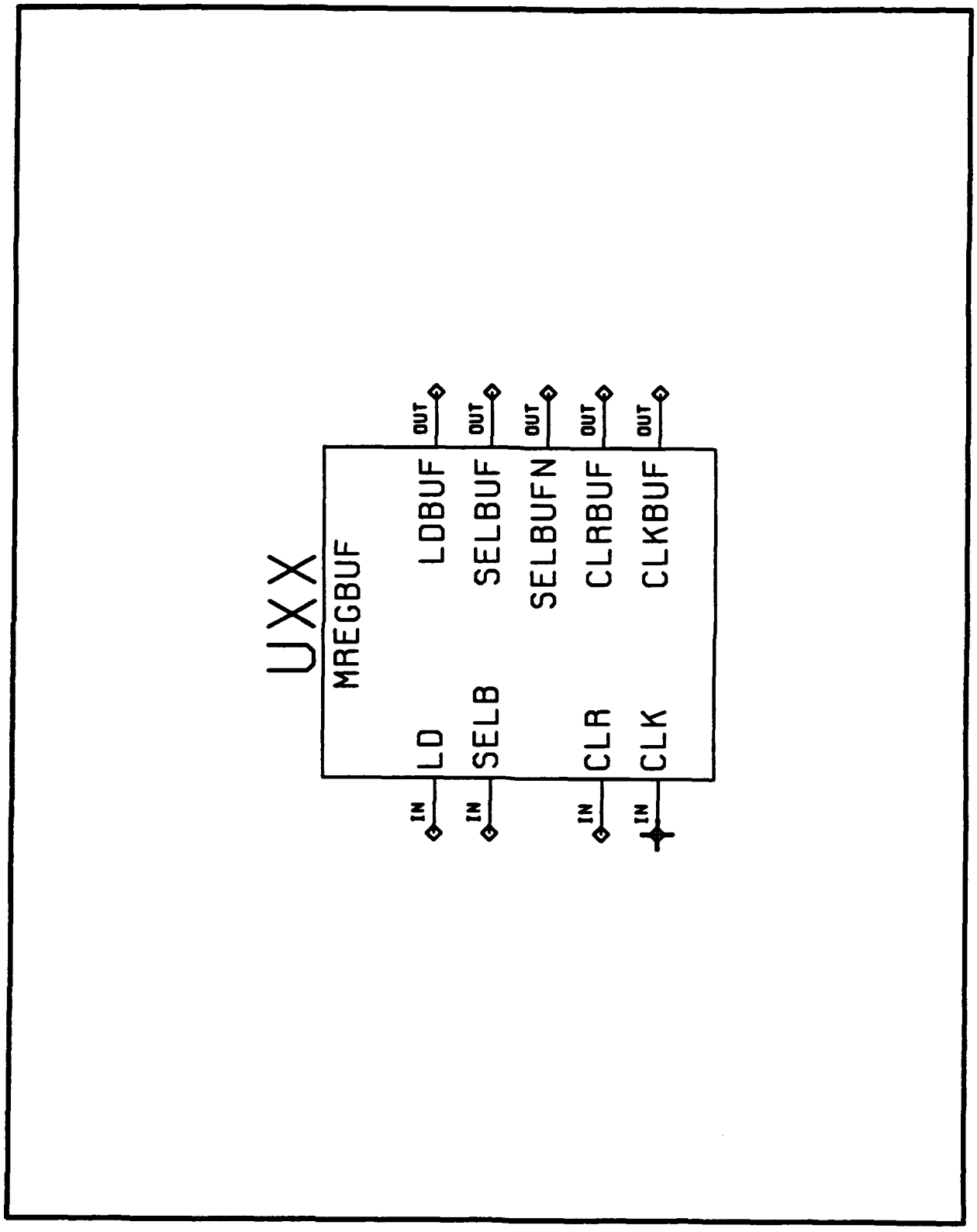

MREG
FOR I := 0 TO 14
FOR I := 15 TO 31
REGOUT (I)
FA0 (I)
LDBUF1
CLKBUF1
CLABUF1
FA1 (I)
SAN
SBN
LDBUF2
CLKBUF2
CLABUF2
REGOUT (31:0)
MSW (15:0)
LSW (15:0)
FA0 (31:0)
FA1 (14:0)
FA1 (15)
FA1 (30:16)
FA1 (31)
MULTM (15:0)
MULTL (15:0)
LD
CLR
CLK
FA

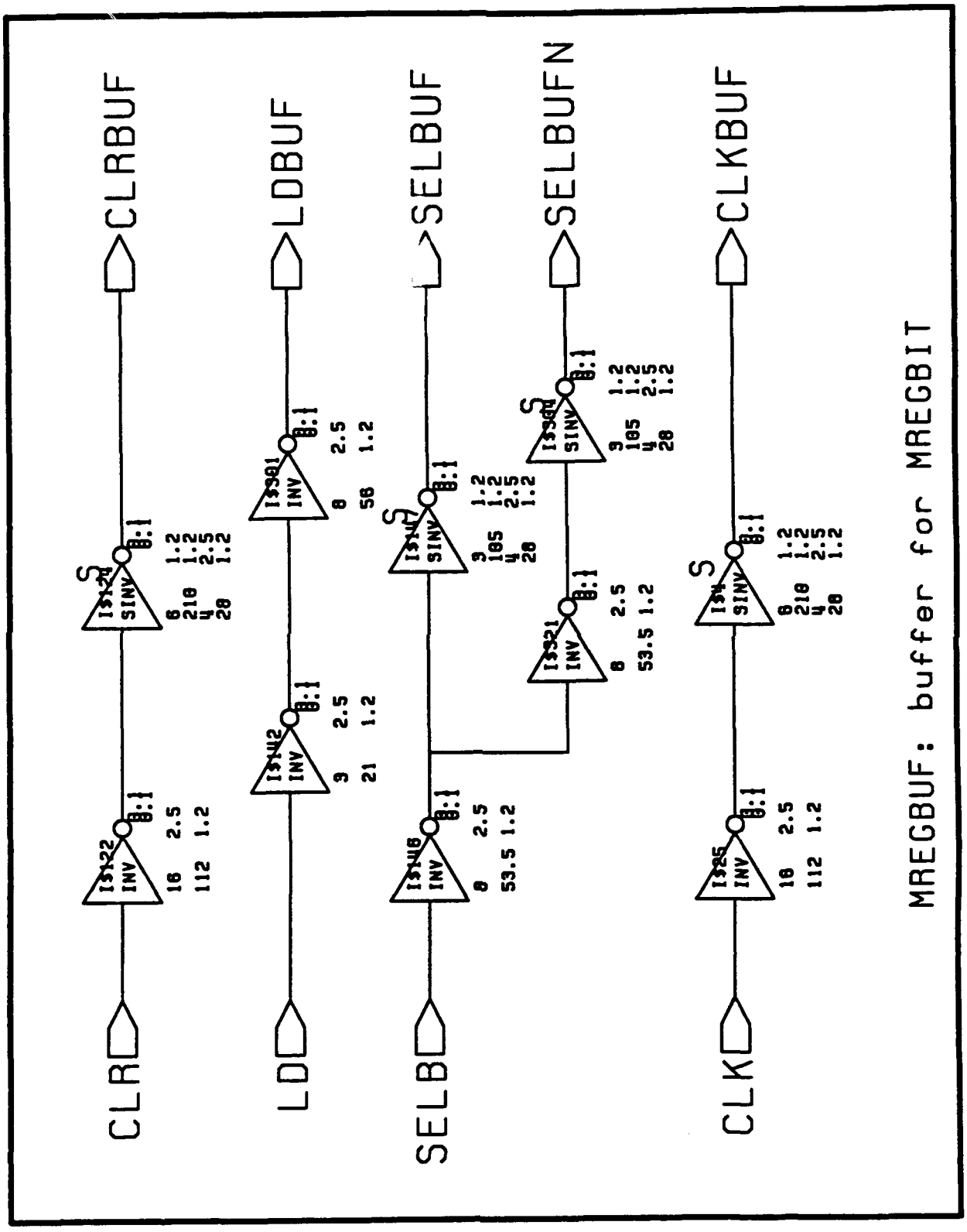

UXX
MREGBIT
OUT
Q
CLR
NI
DA
DB
SAN
SBN
LD
CLK
IN
IN
IN
IN
IN
IN

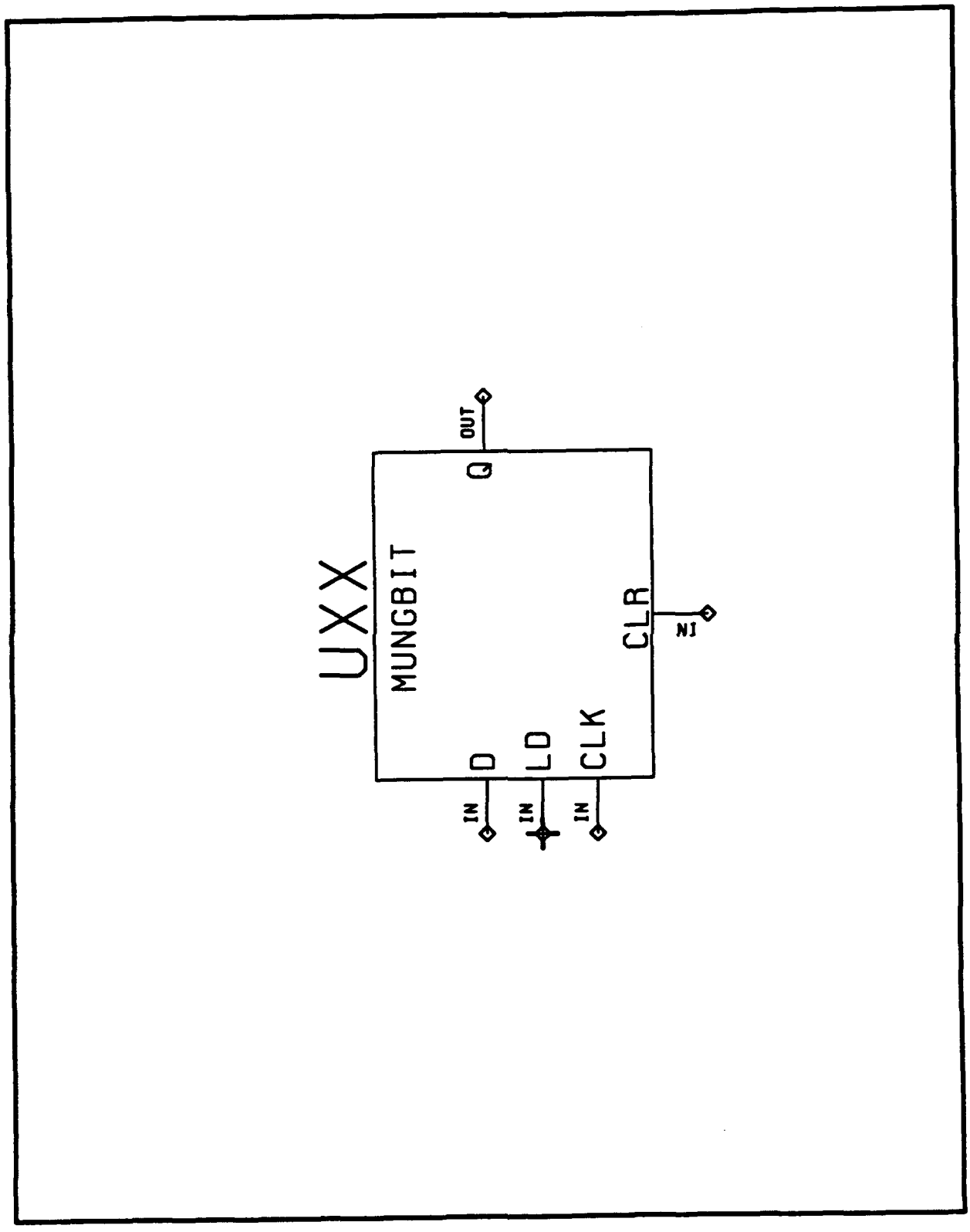

MREGBIT: mux + reg w/ synchronous clr
Q
CLR
CLK
LD
SIN
SIN

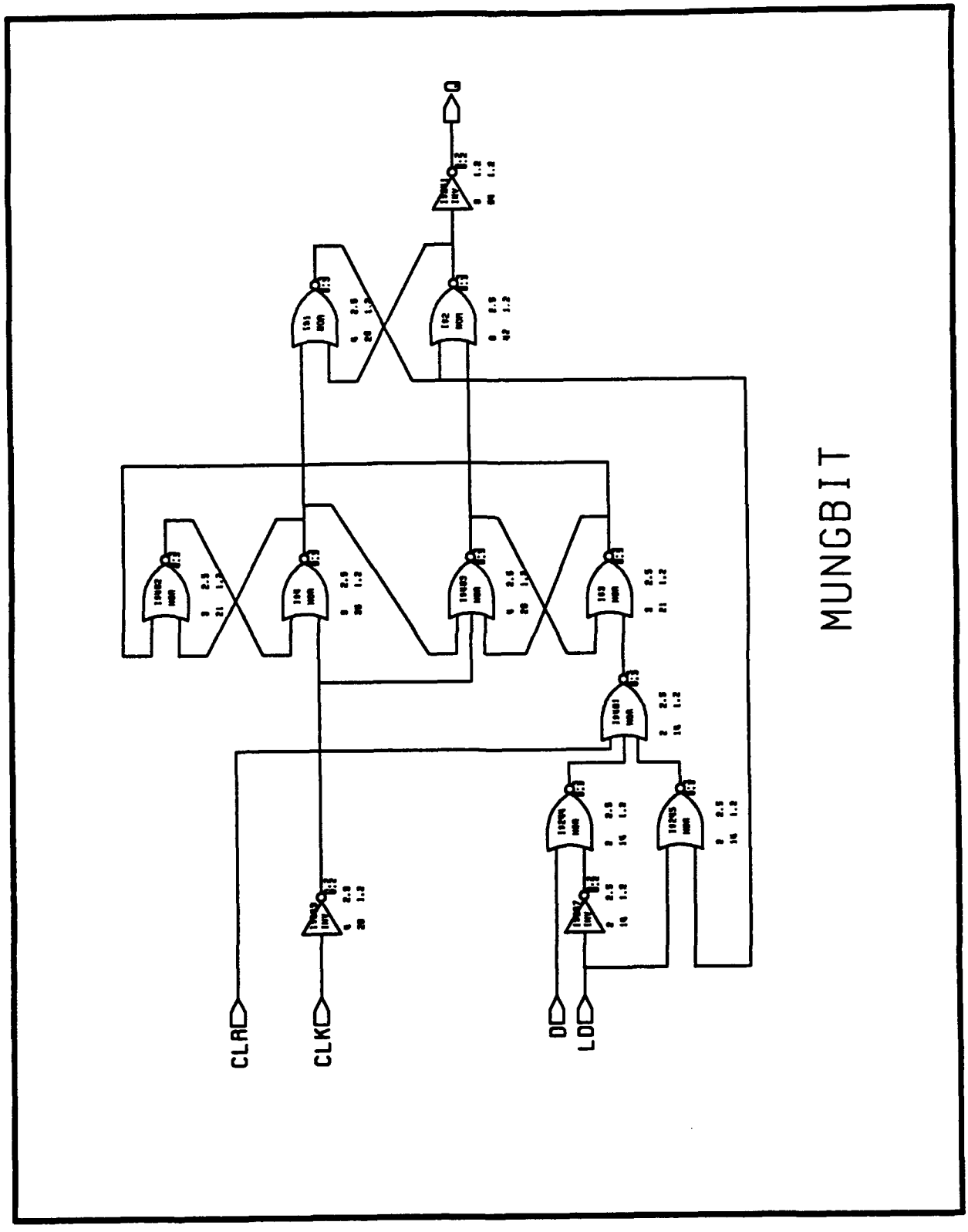

SSS
0
0
1
0
00
out
0.3
00
I#
NOR
I0
I1
in
in
(DW) (DL)
(EW) (EL)
NOR
0.17
I0
0.17
I1

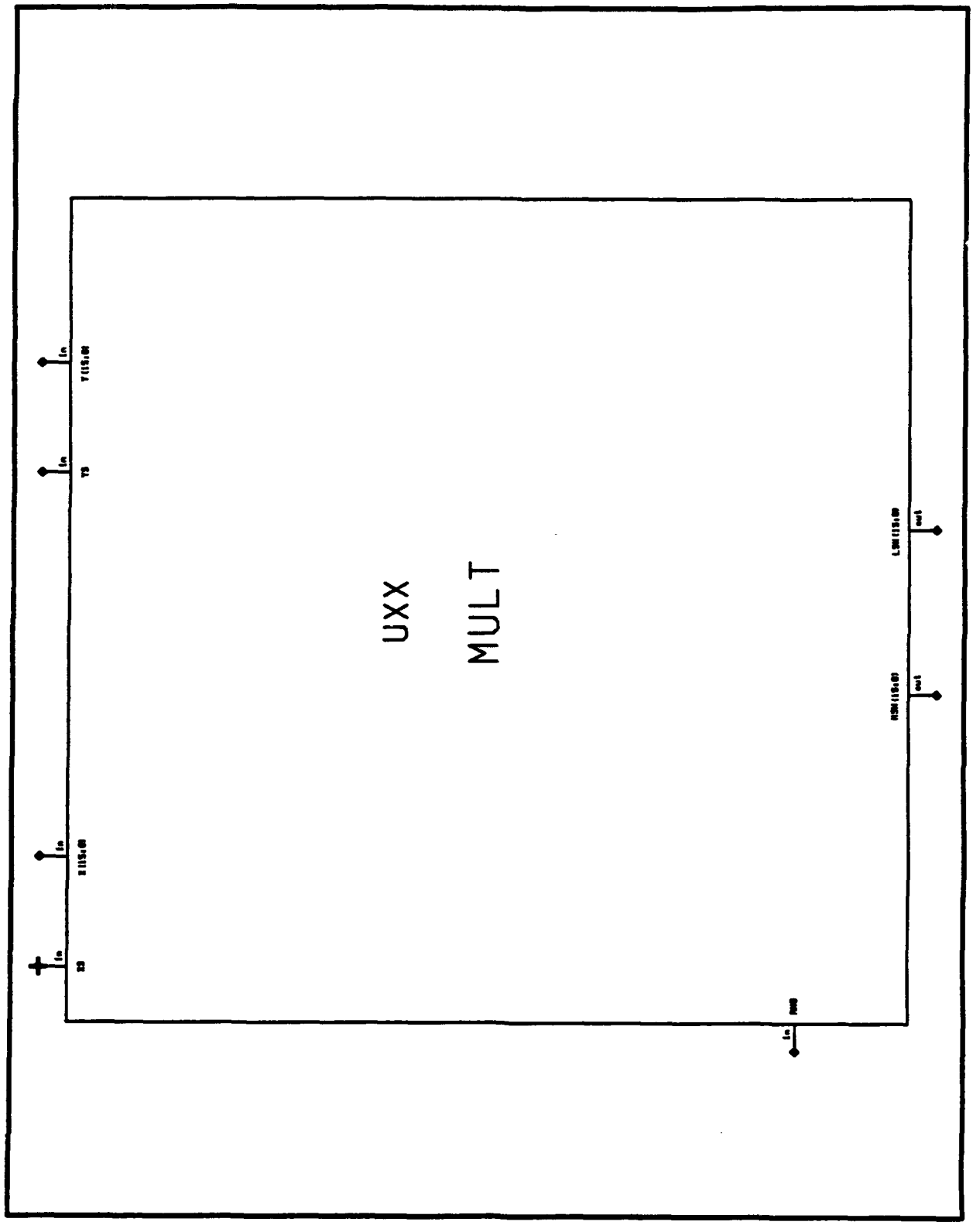

O0
CG
(DW)
(DL)
(EW)
(EL)
VTT
I$1
I$2
(EW)
(EL)
I$3
I0
I1

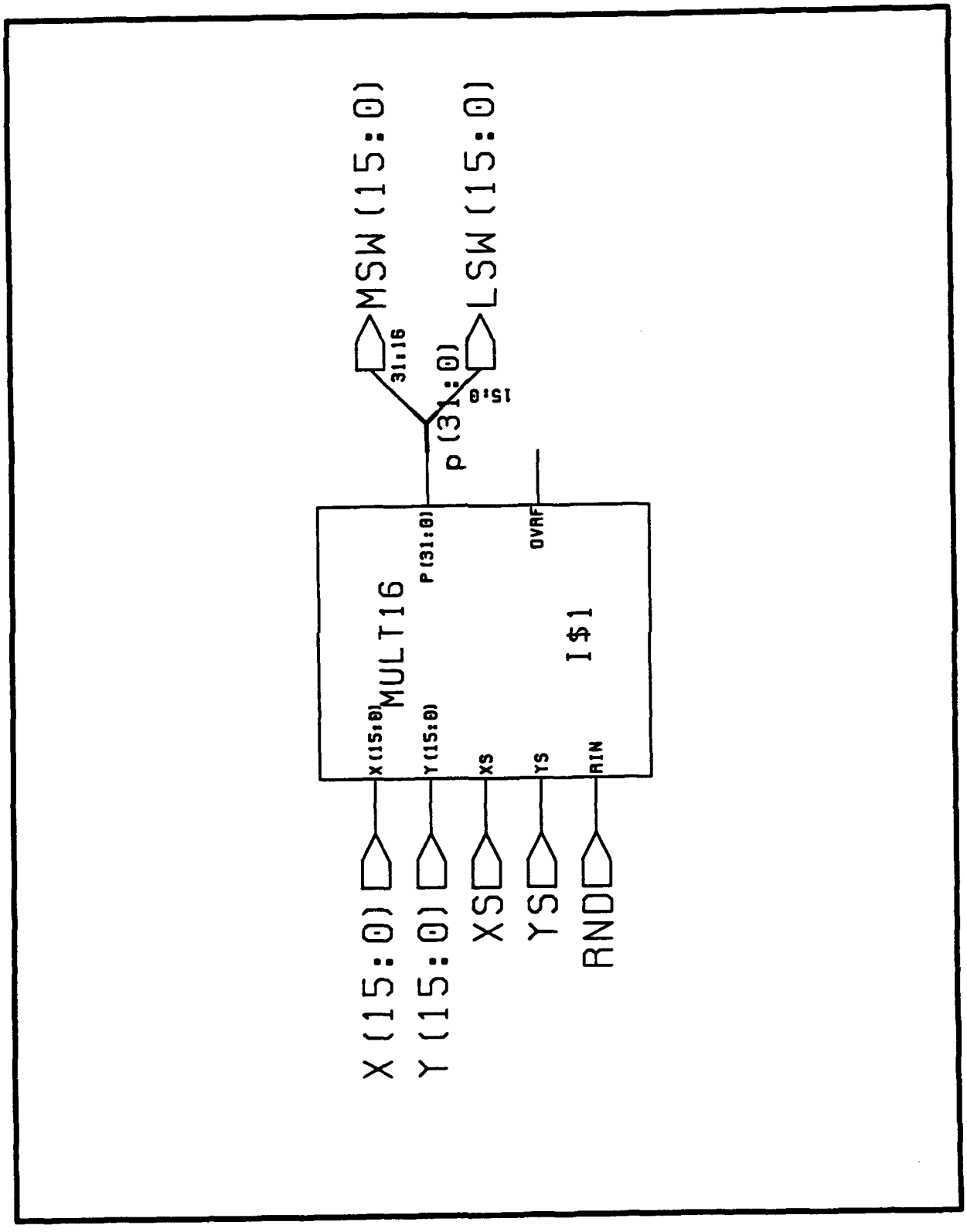

UXX
MREGBUF
LDBUF
SELBUF
SELBUFN
CLRBUF
CLKBUF
OUT
OUT
OUT
OUT
OUT
LD
SELB
CLR
CLK
IN
IN
IN
IN

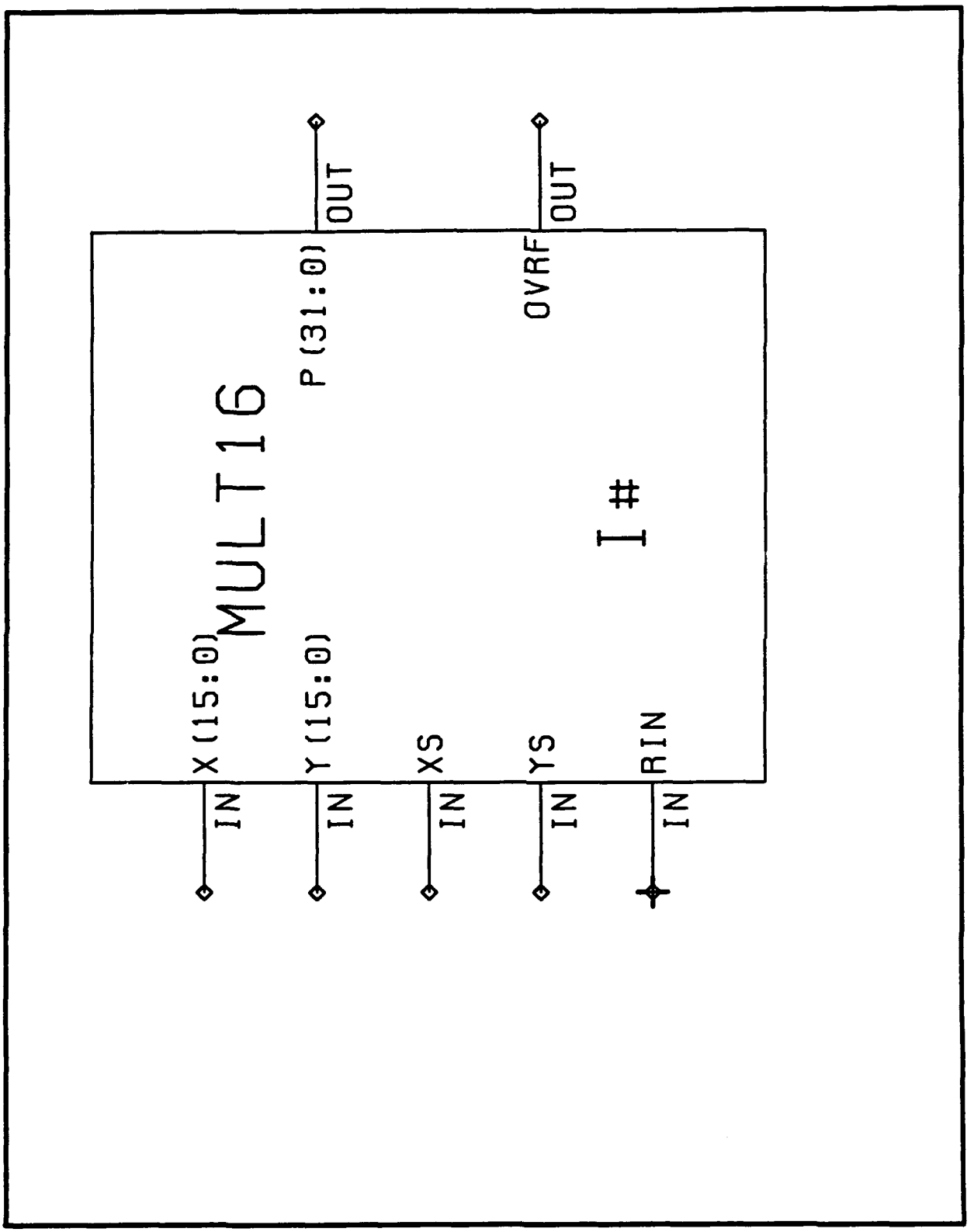

MREGBUF: buffer for MREGBIT
CLRBUF
LDBUF
SELBUF
SELBUFN
CLKBUF
CLR
LD
SELB
CLK
I3322 INV
I3301 INV
I3342 INV
I3348 INV
I3321 INV
I3325 INV
I3324 SINV
I3347 SINV
I3340 SINV
I3341 SINV

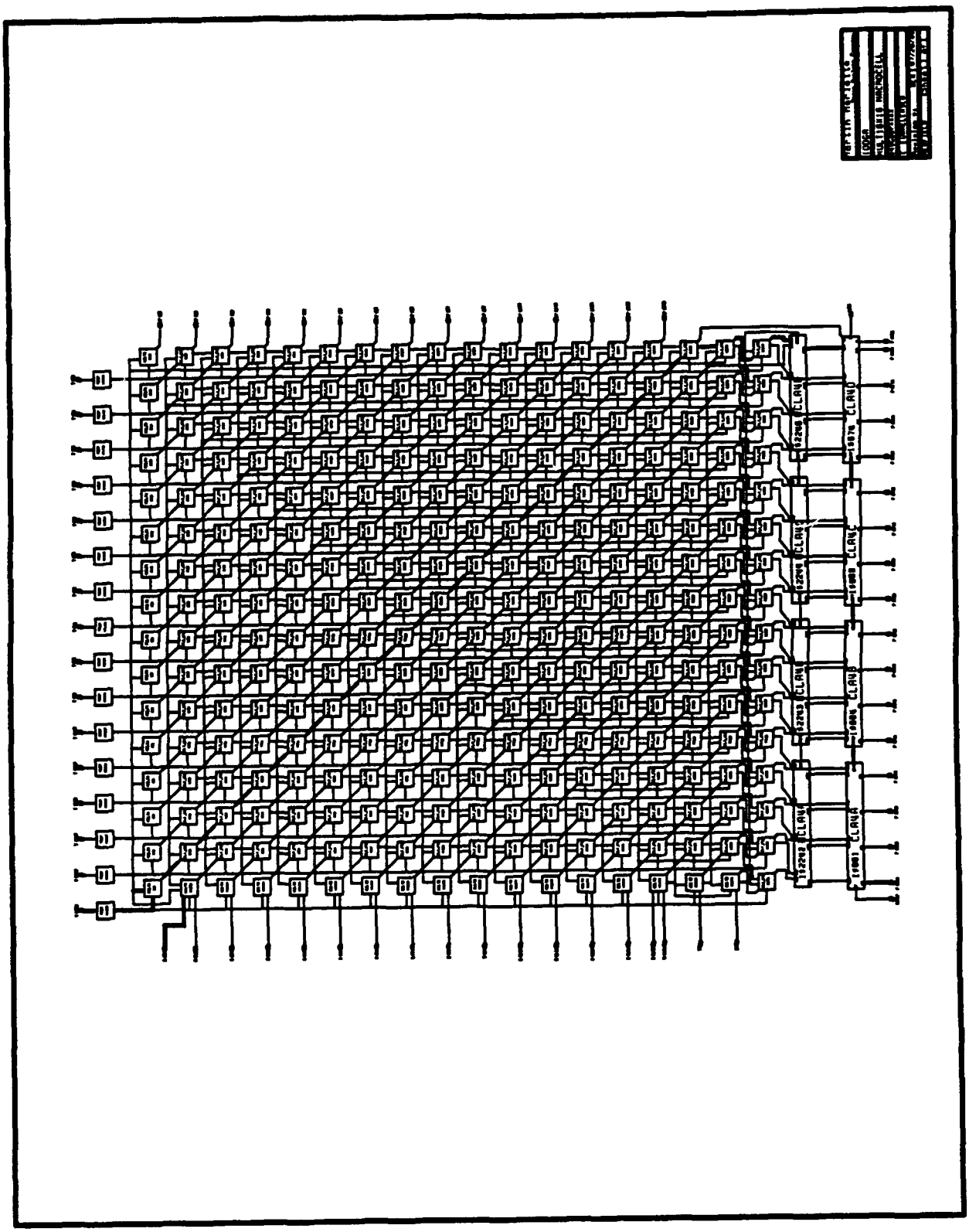

UXX
MUNGBIT
OUT
Q
CLR
NI
D
LD
CLK
IN
IN
IN

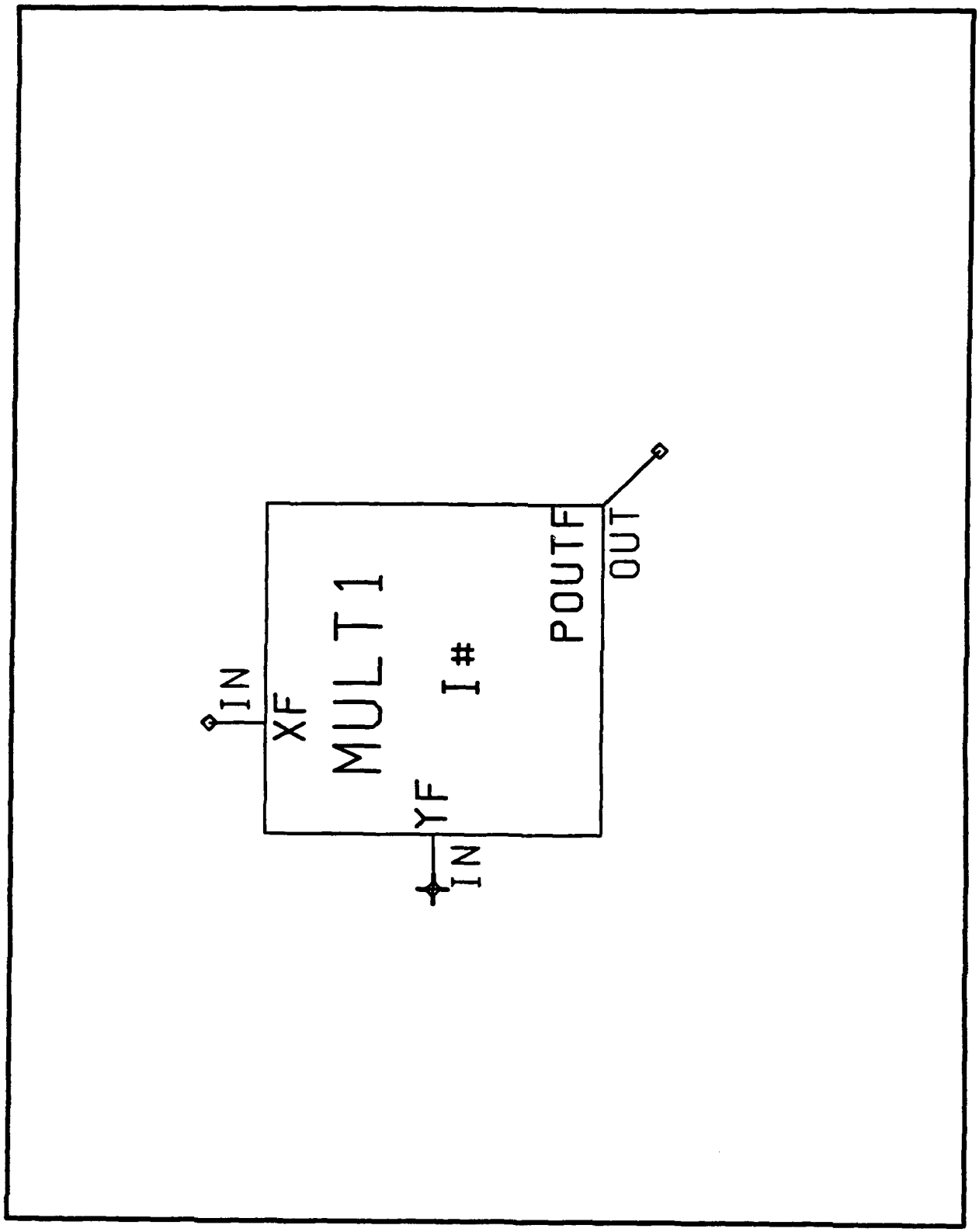

MUNGBIT
CLR
CLK
D
LD

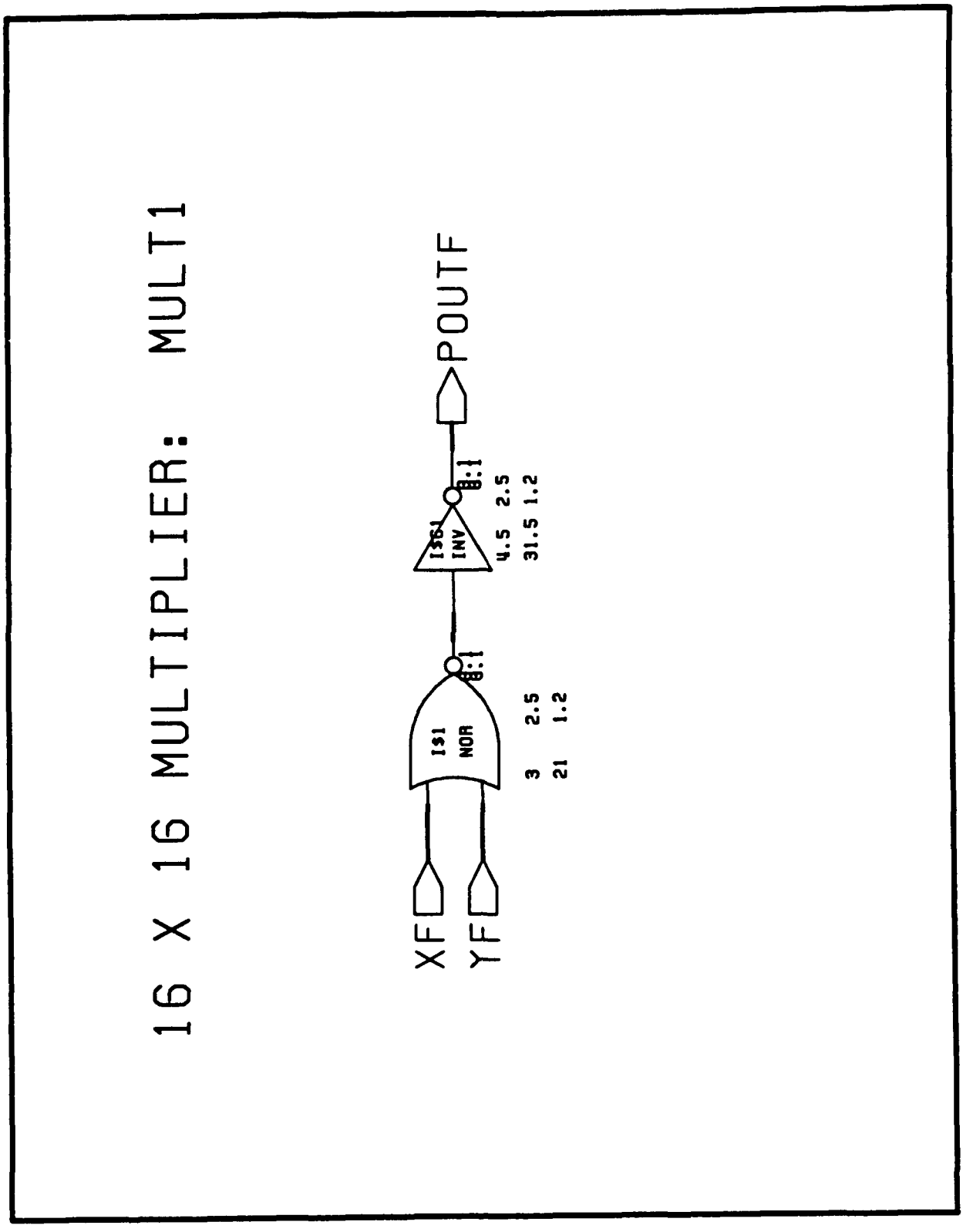

UXX
MULT

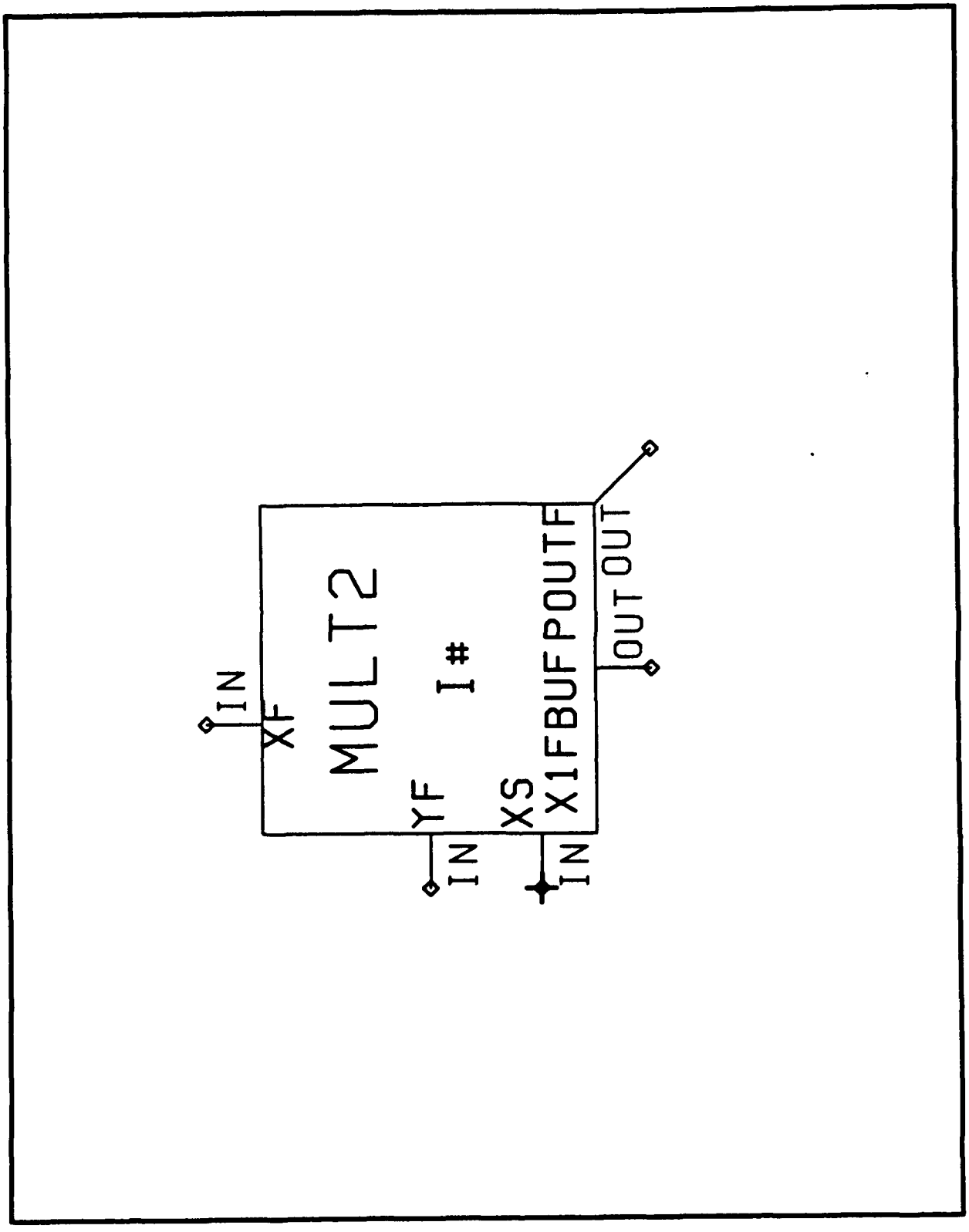

MSW(15:0)
LSW(15:0)
31:16
15:0
P(31:0)
MULT16
P(31:0)
OVRF
I$1
X(15:0)
Y(15:0)
XS
YS
RIN
X(15:0)
Y(15:0)
XS
YS
RND

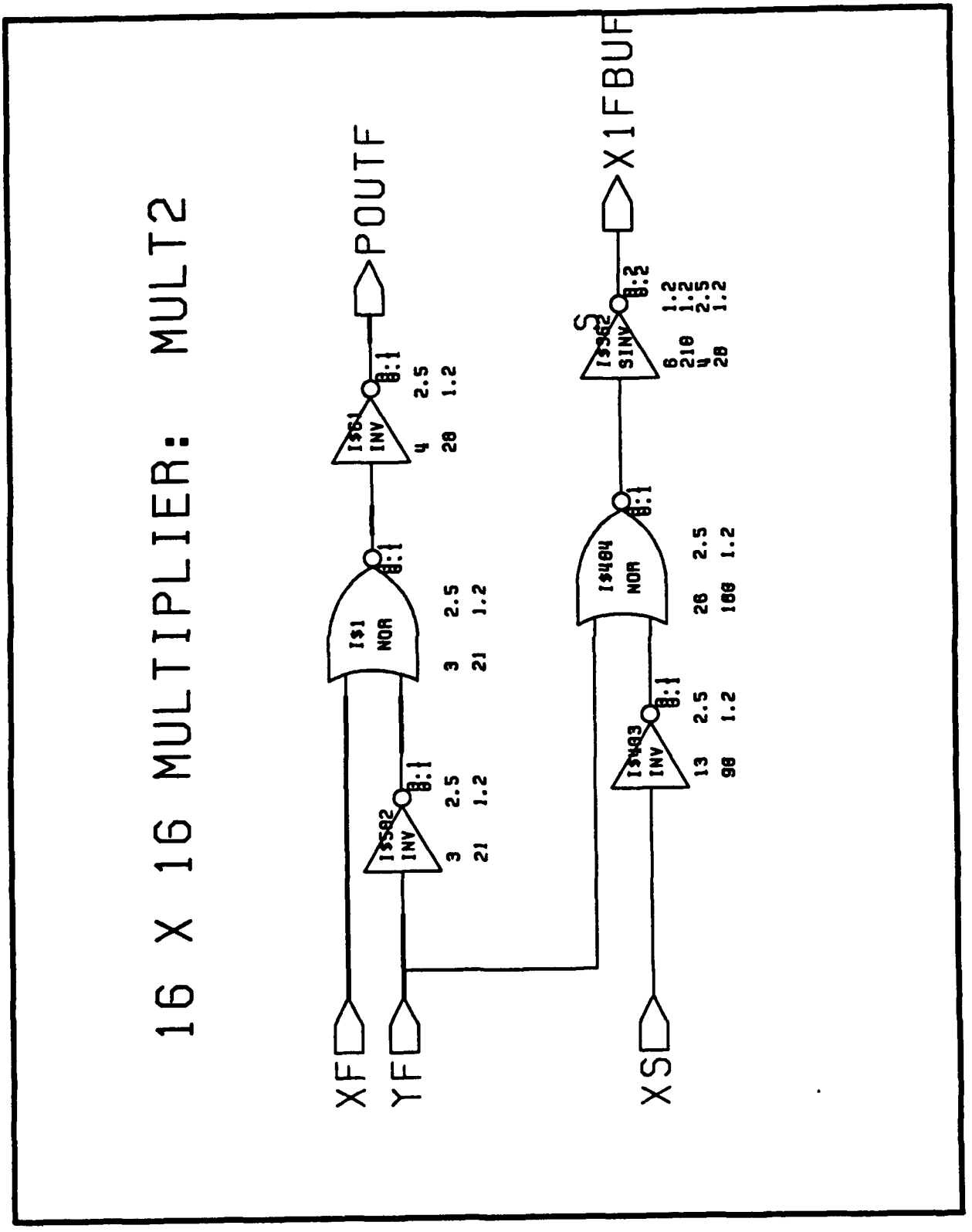

MULT16
I#
X(15:0)
Y(15:0)
XS
YS
RIN
IN
IN
IN
IN
IN
P(31:0)
OVRF
OUT
OUT

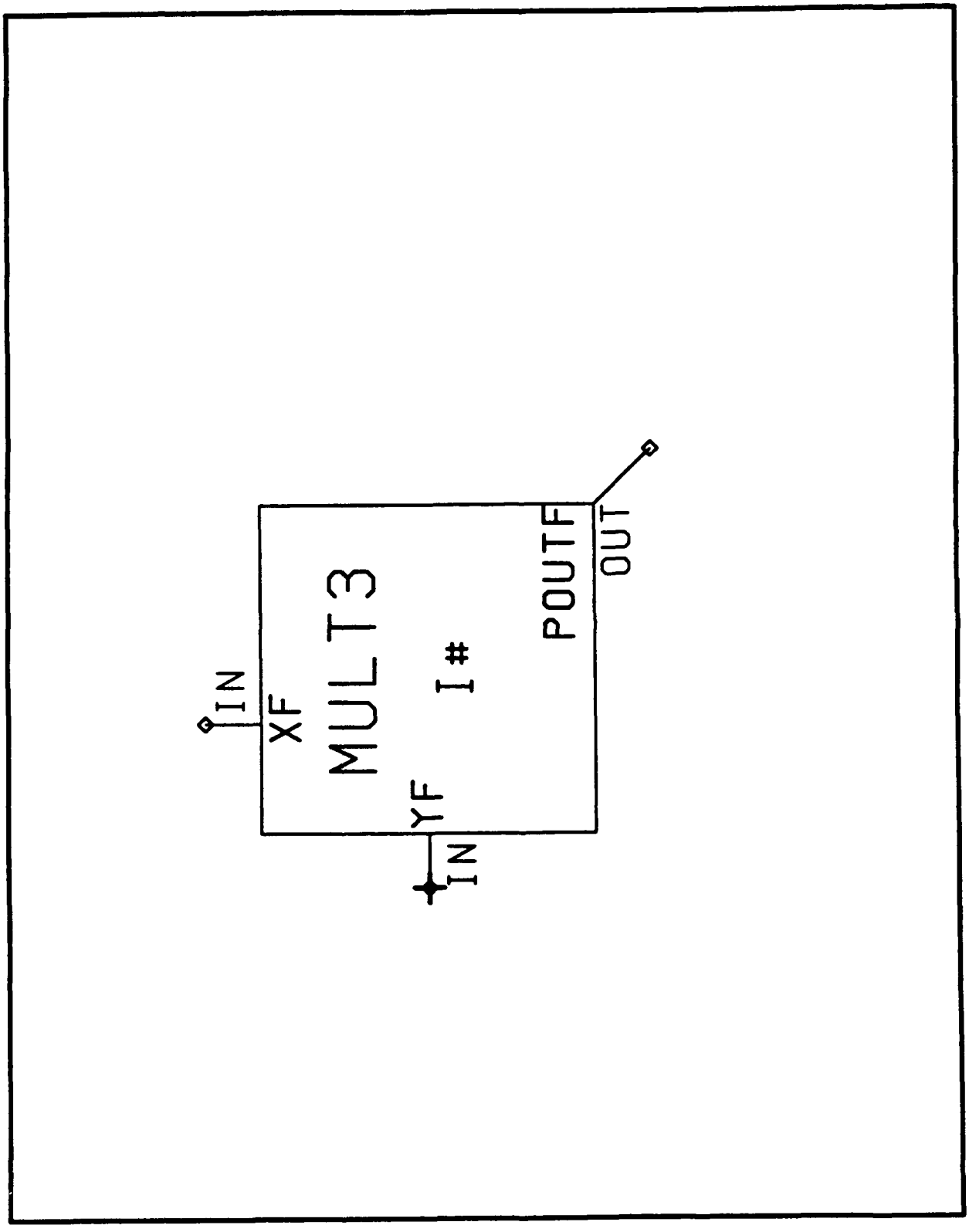


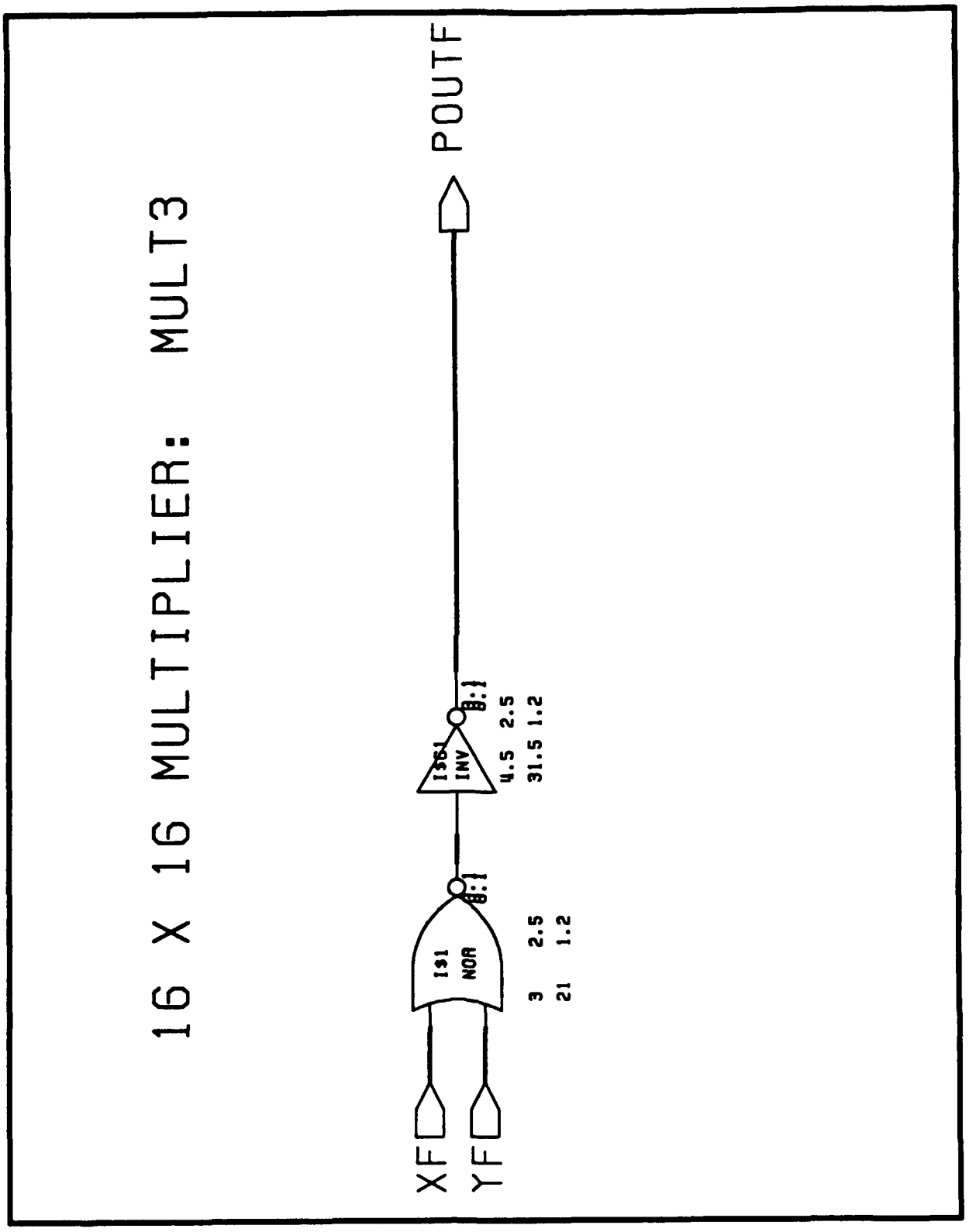

IN
XF
MULT1
I#
YF
IN
POUTF
OUT

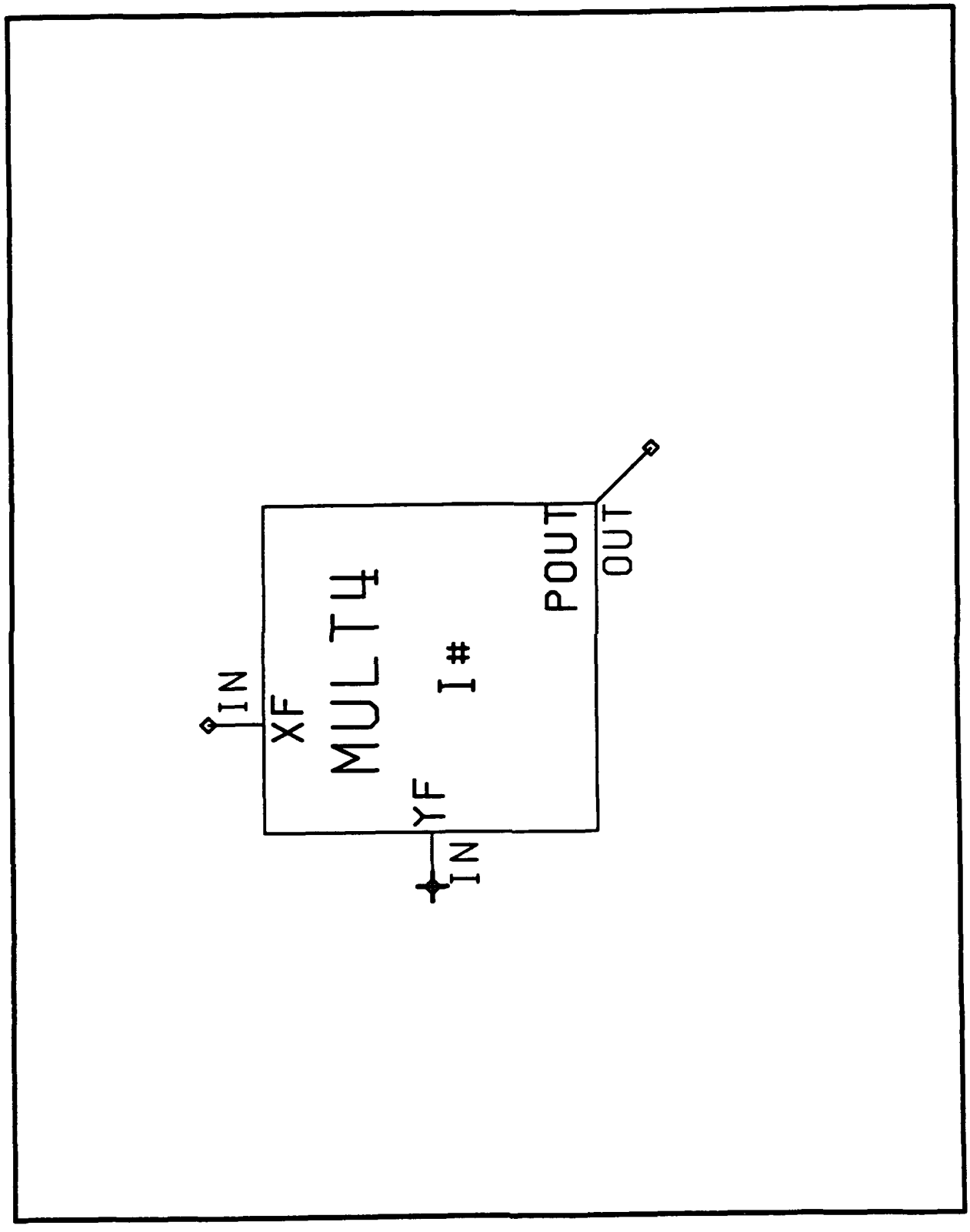

16 X 16 MULTIPLIER: MULT1
POUTF
XF
YF
INV
NOR
4.5 2.5
31.5 1.2
3 2.5
21 1.2

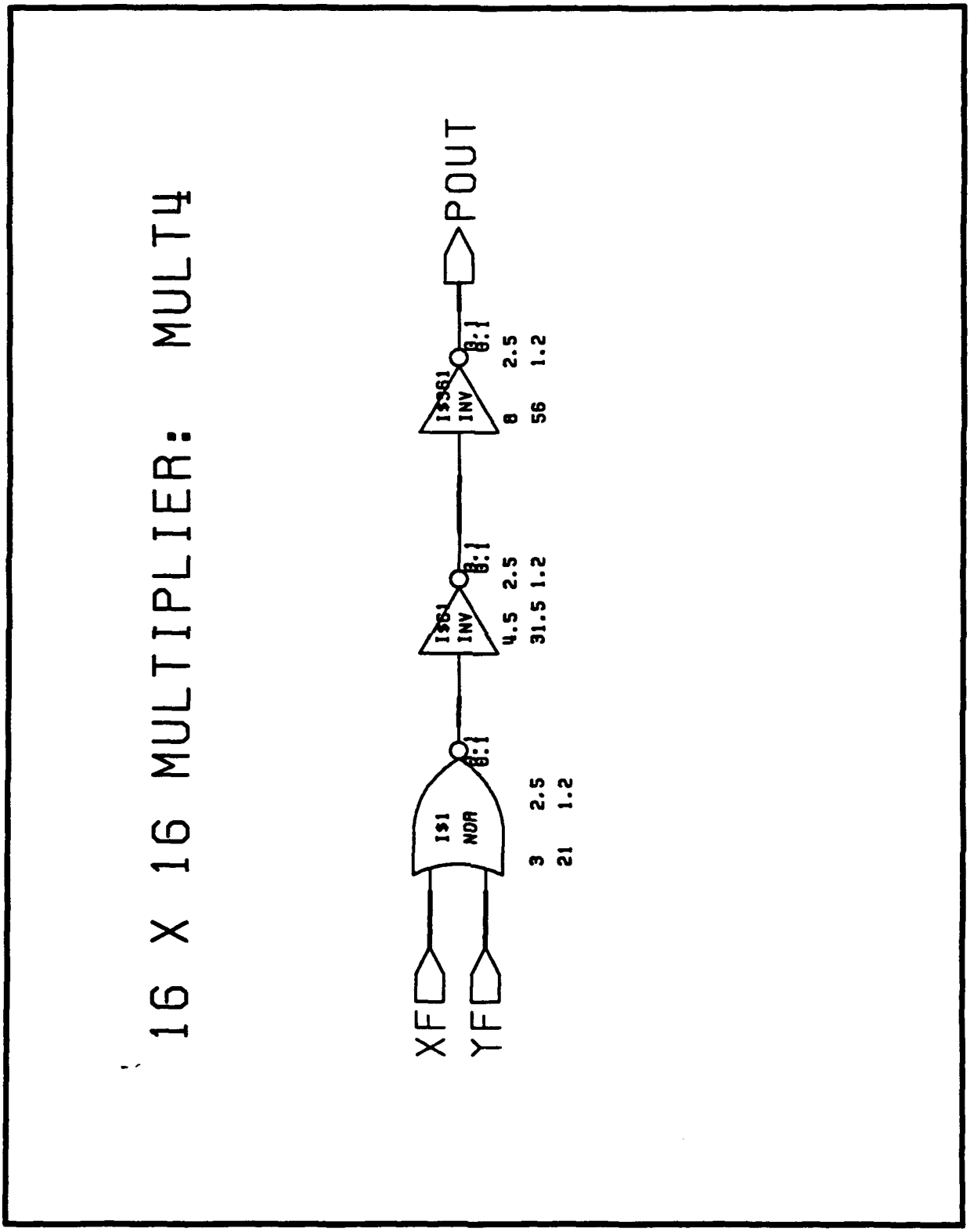

MULT2
I#
IN
XF
YF
XS
X1FBUFPOUTF
OUT
OUT
IN
IN

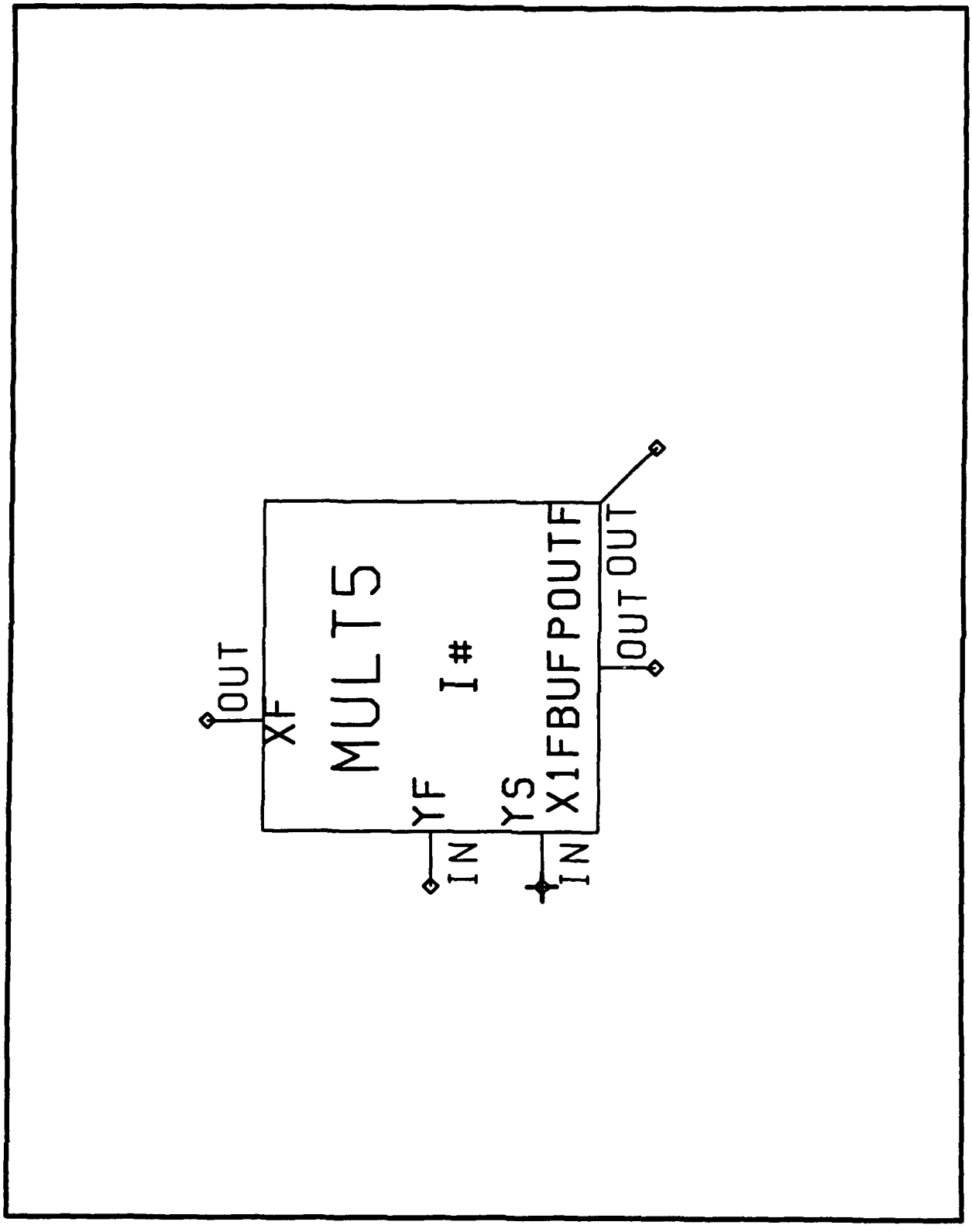

16 X 16 MULTIPLIER: MULT2
POUTF
X1FBUF
I$1
NOR
I$61
INV
I$362
SINV
I$404
NOR
I$482
INV
I$483
INV
XF
YF
XS

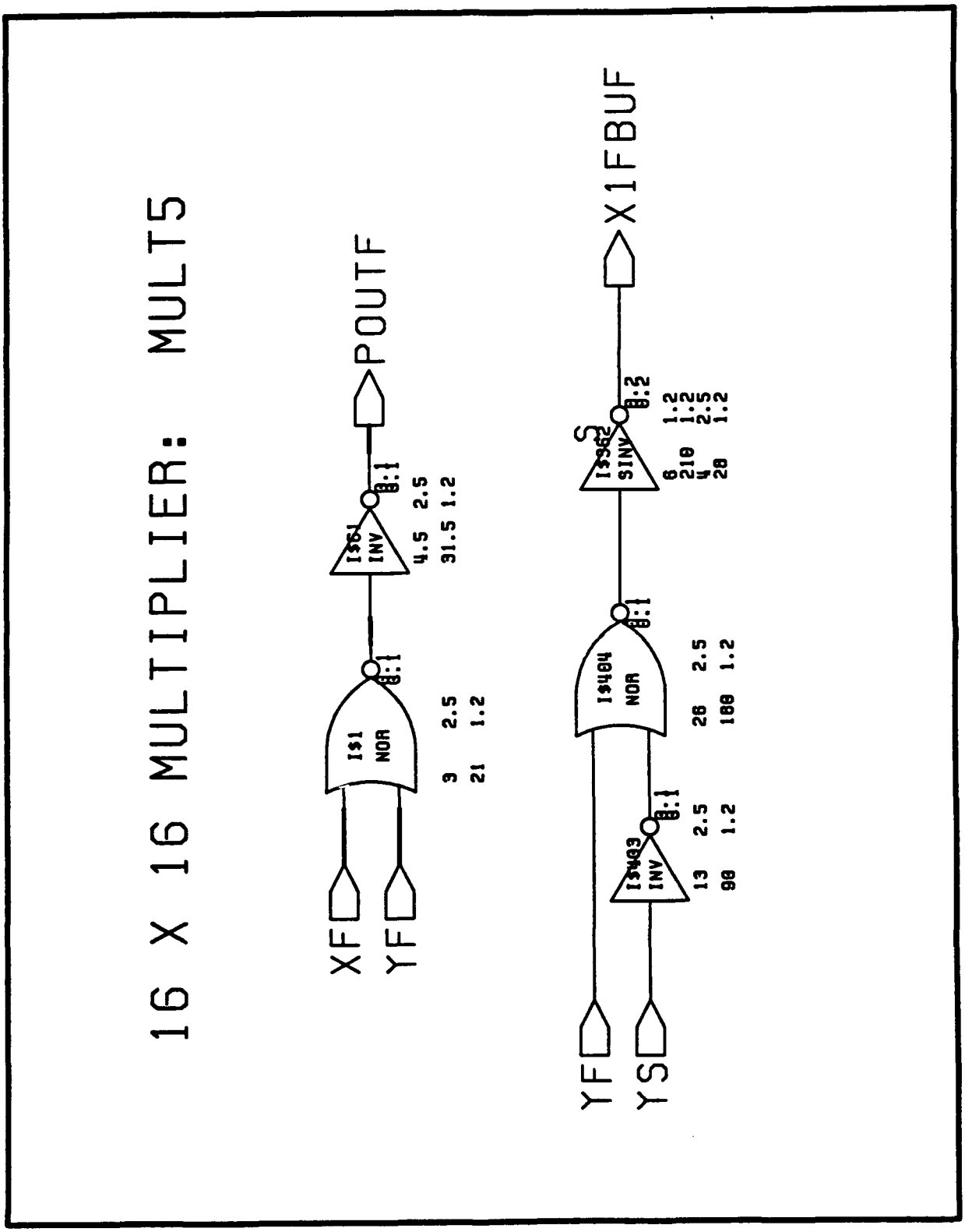

IN
XF
MULT3
I#
POUTF
OUT
YF
IN

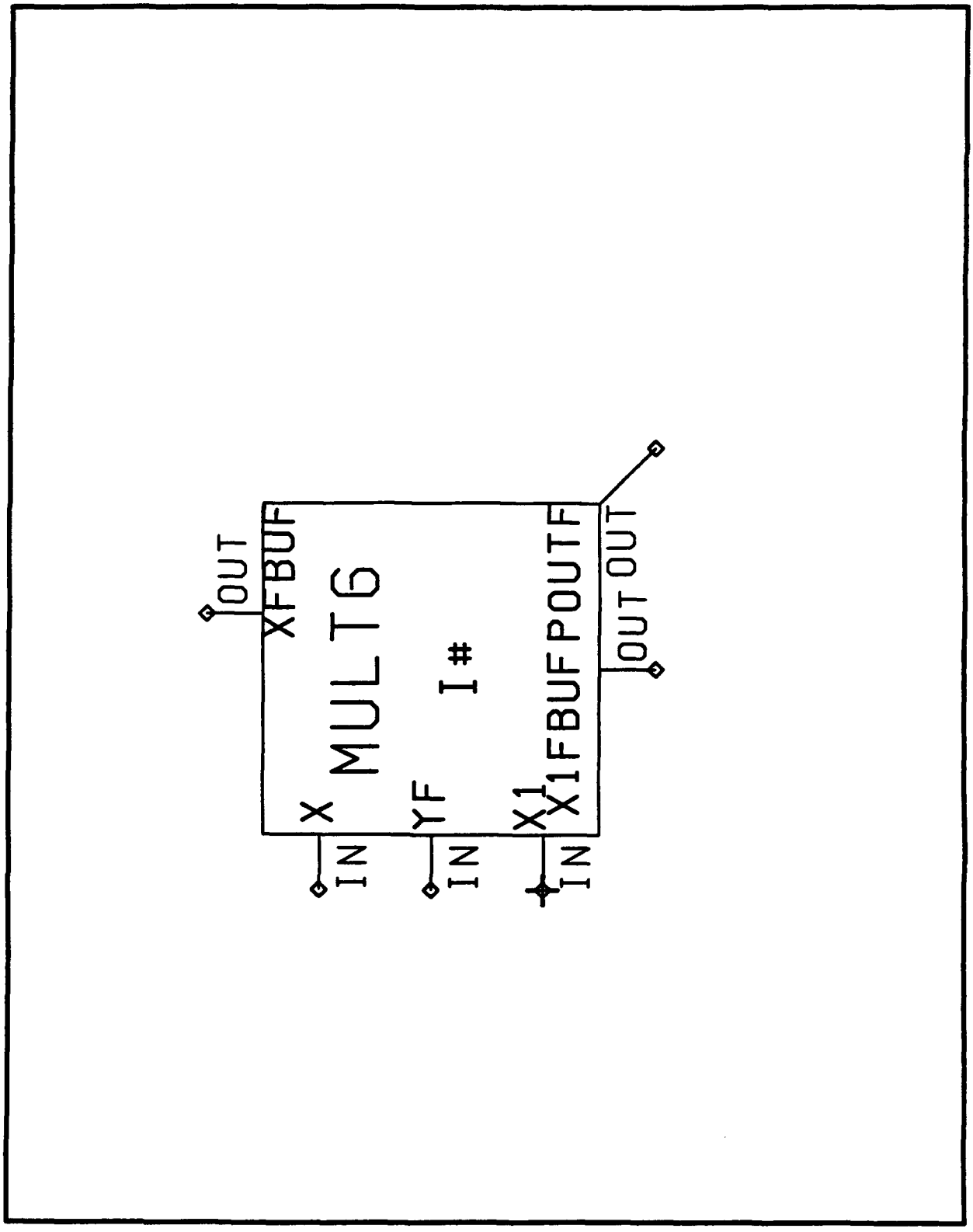

16 X 16 MULTIPLIER: MULT3
POUTF
I361
INV
4.5 2.5
31.5 1.2
I91
NOR
3 2.5
21 1.2
XF
YF

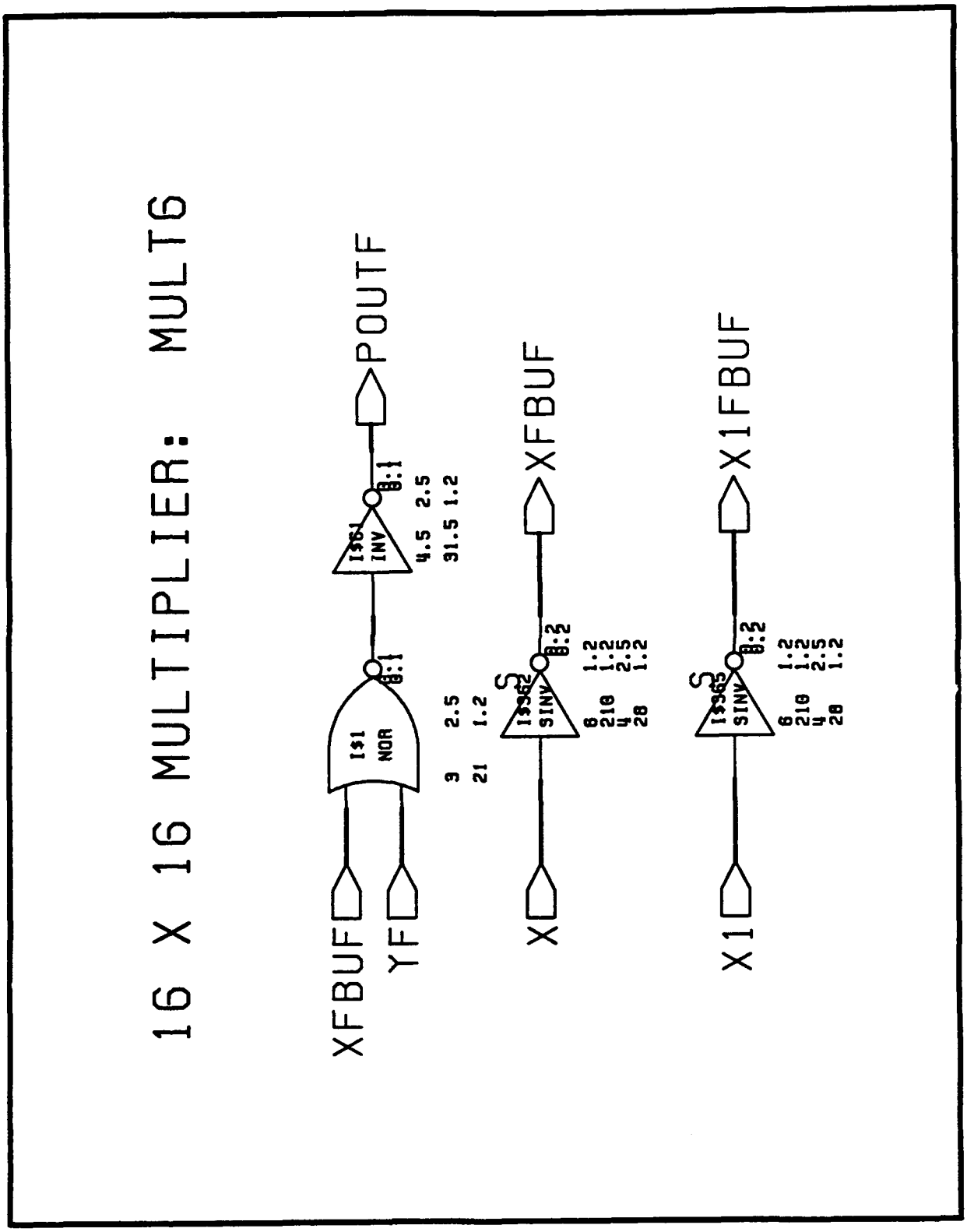

MULT4
I#
XF
IN
YF
IN
POUT
OUT

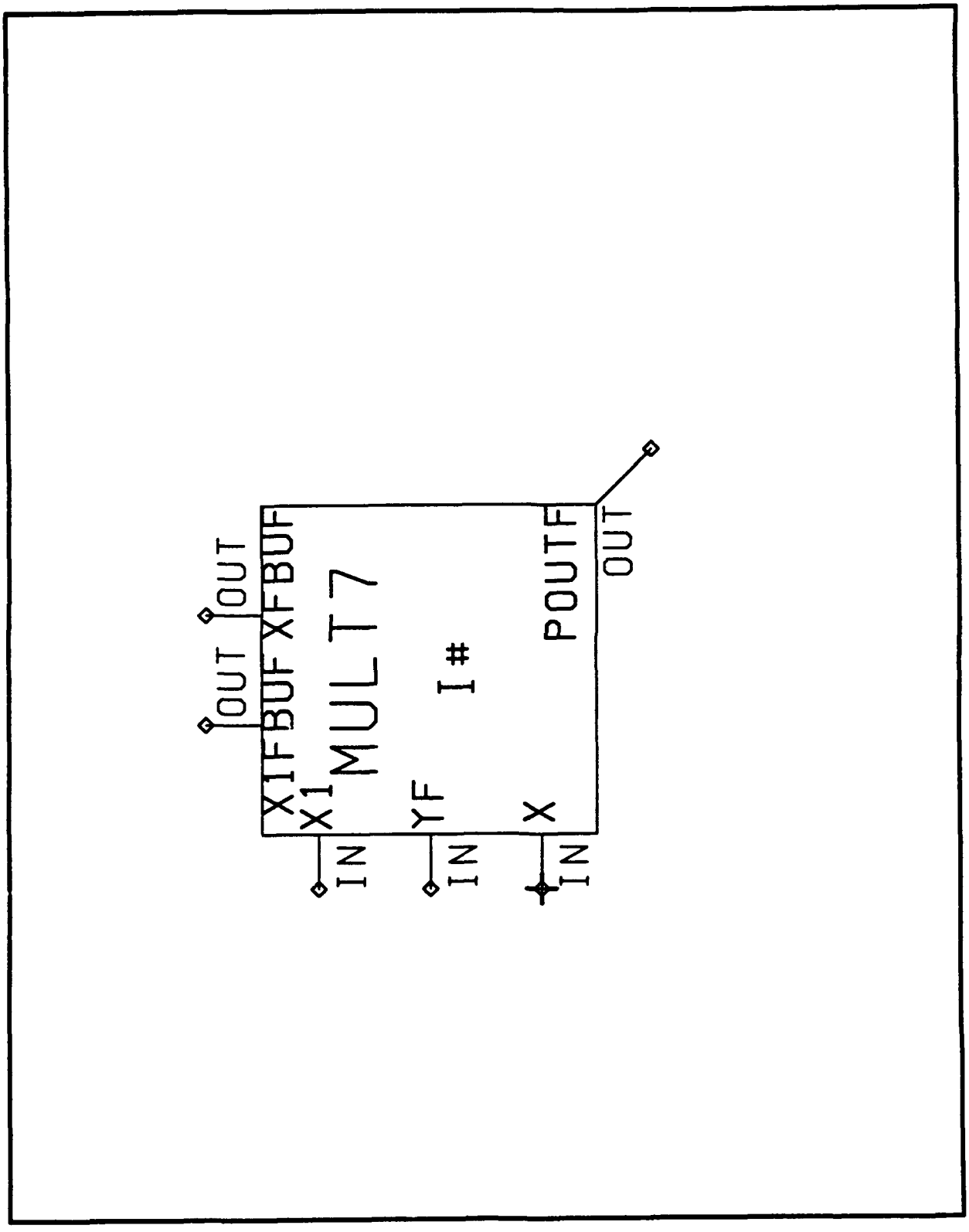

16 X 16 MULTIPLIER: MULT4
POUT
XF
YF
I3361
INV
I361
INV
I31
NOR
8.1
8.1
8.1
8 2.5 1.2
56
4.5 2.5 1.2
31.5
3 2.5 1.2
21

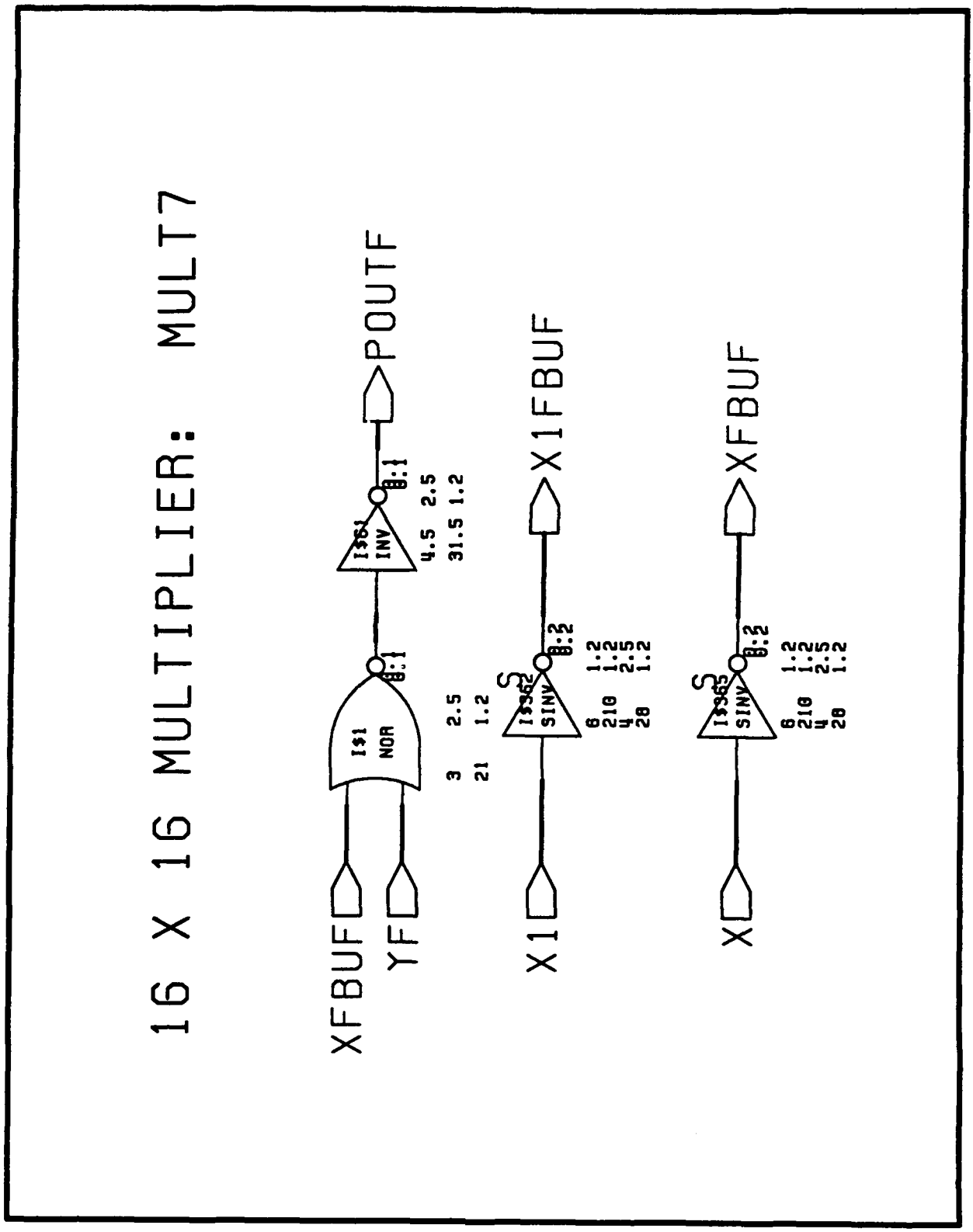

MULT5
I#
OUT
XF
YF
IN
YS
IN
X1FBUFPOUTF
OUT OUT

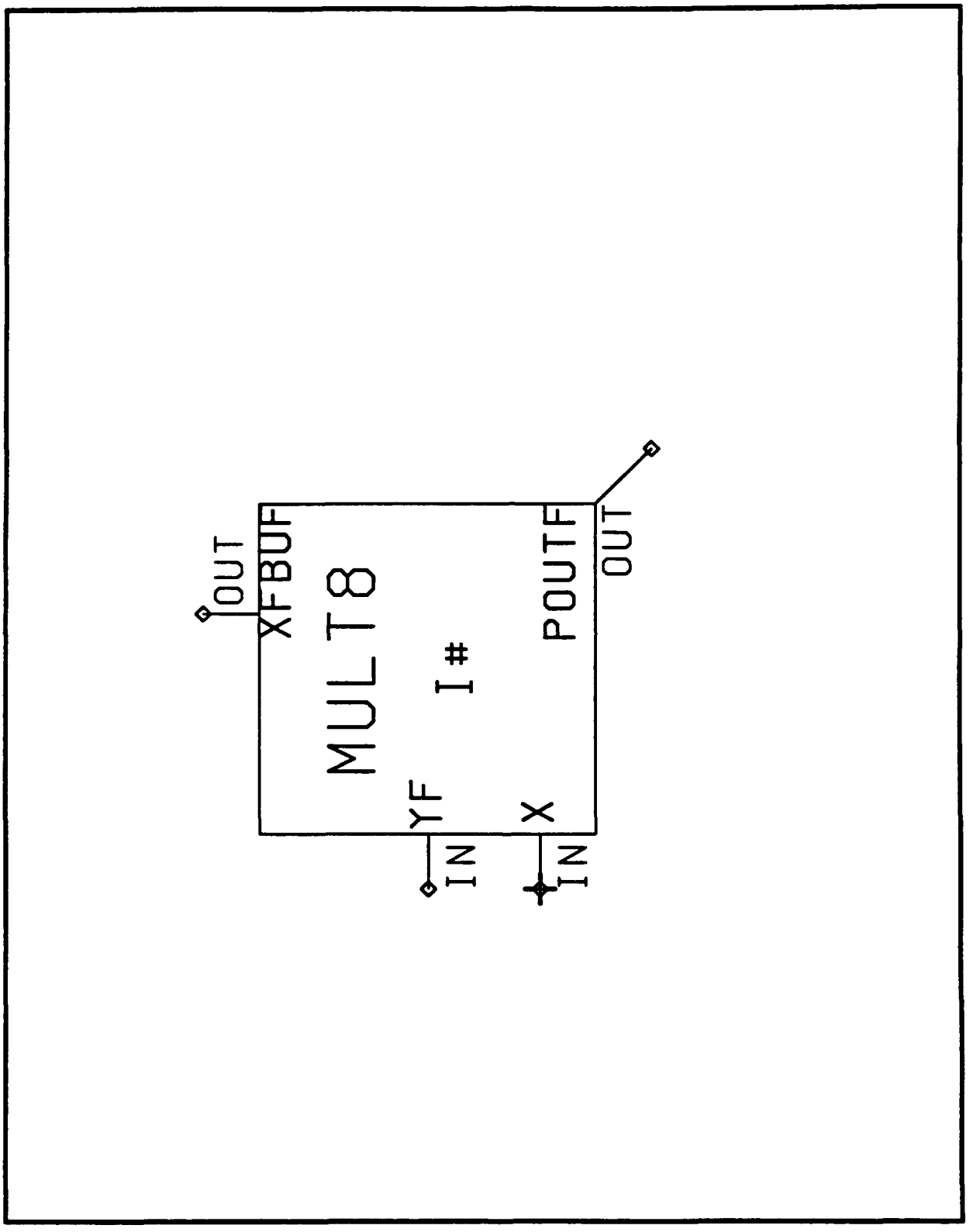

16 X 16 MULTIPLIER: MULT5
XF
YF
I$1
NOR
I$61
INV
POUTF
YF
YS
I$484
NOR
I$483
INV
I$962
SINV
S
X1FBUF

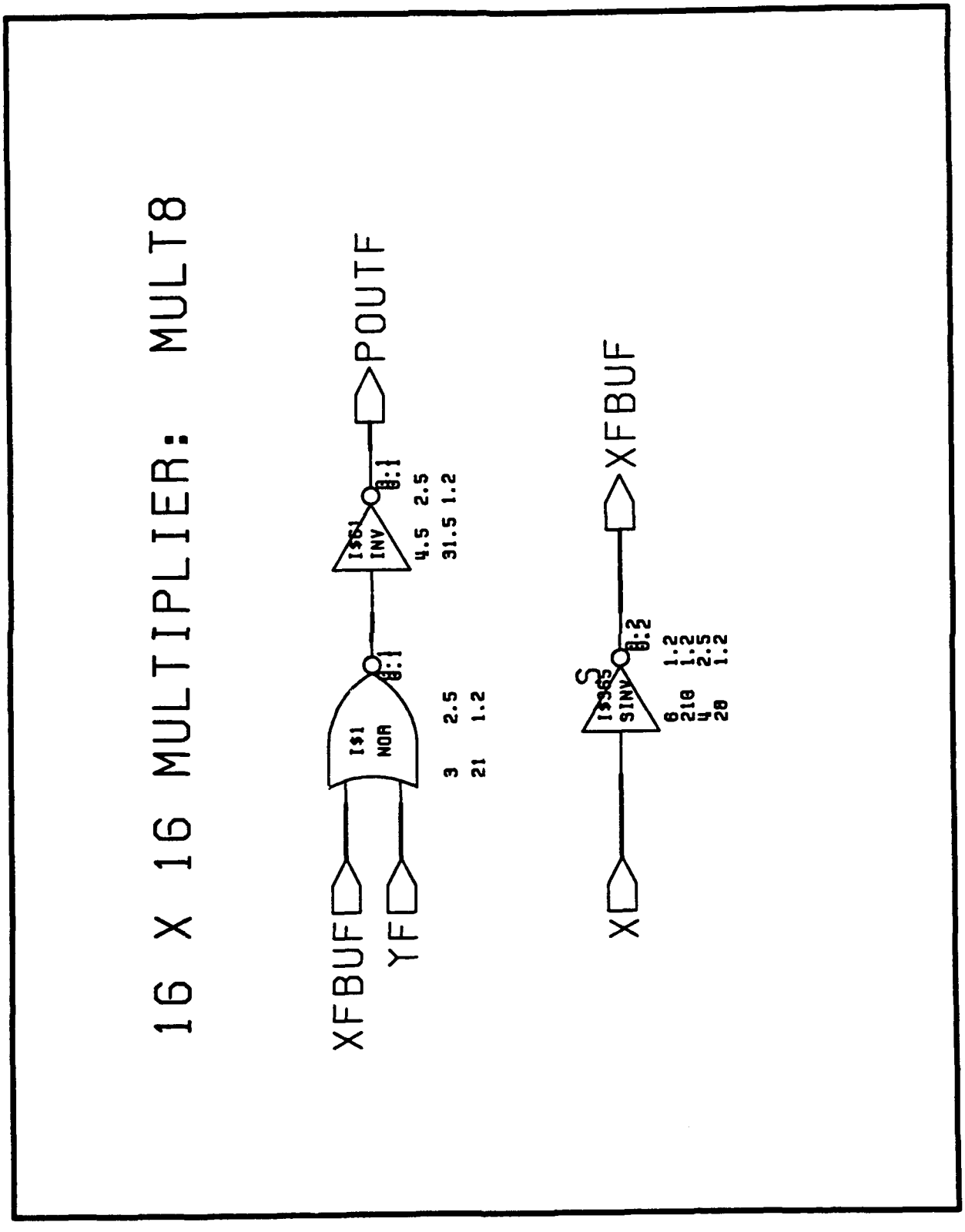

OUT
XFBUF
X
MULT6
I#
YF
X1
X1FBUFPOUTF
OUT OUT
IN
IN
IN

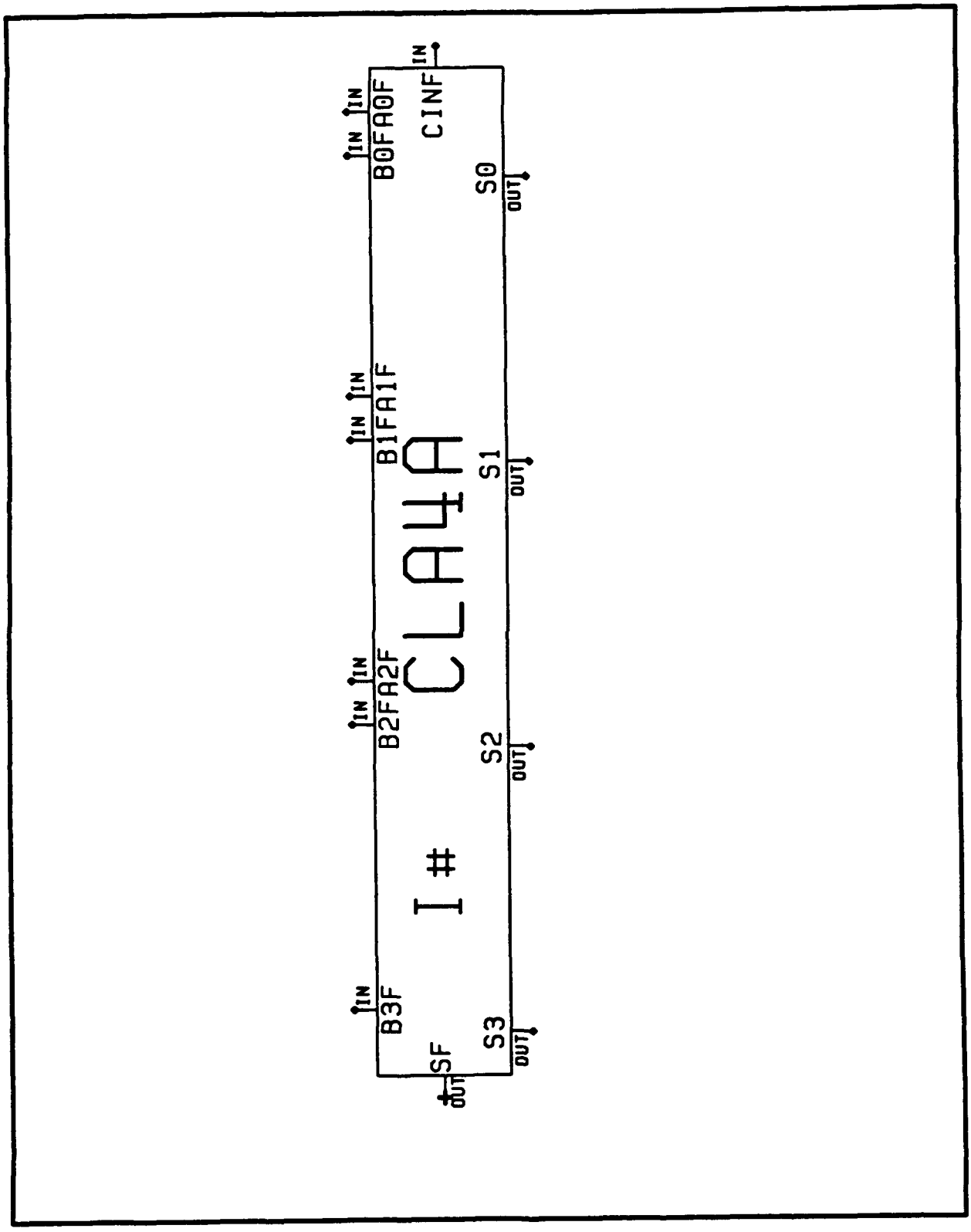

16 X 16 MULTIPLIER: MULT6
XFBUF
YF
I$1
NOR
I$61
INV
POUTF
XFBUF
I$62
SINV
X
X1FBUF
I$63
SINV
X1

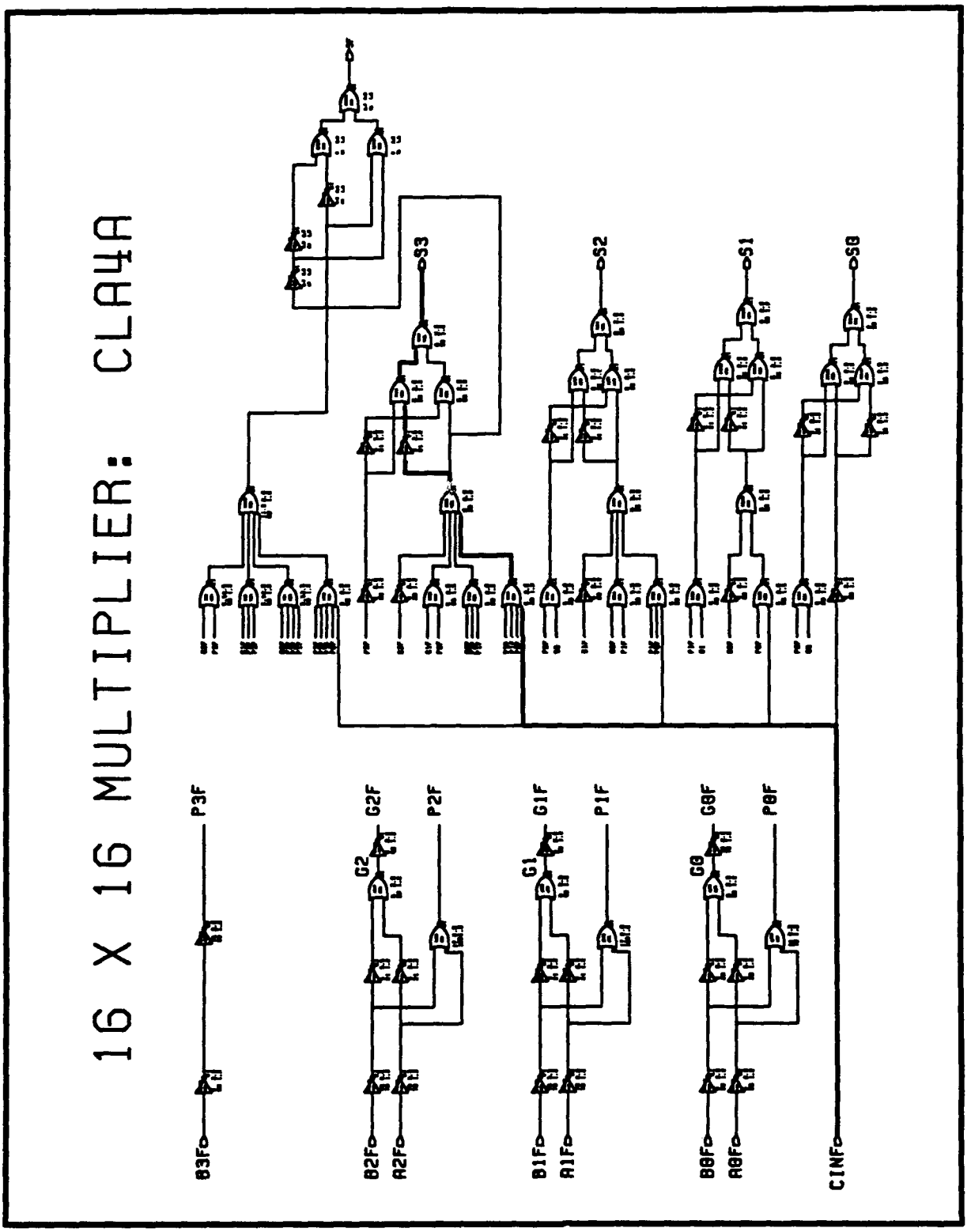

OUT
OUT
XFBUF
XIFBUF
MULT7
I#
POUTF
OUT
X1
YF
X
IN
IN
IN

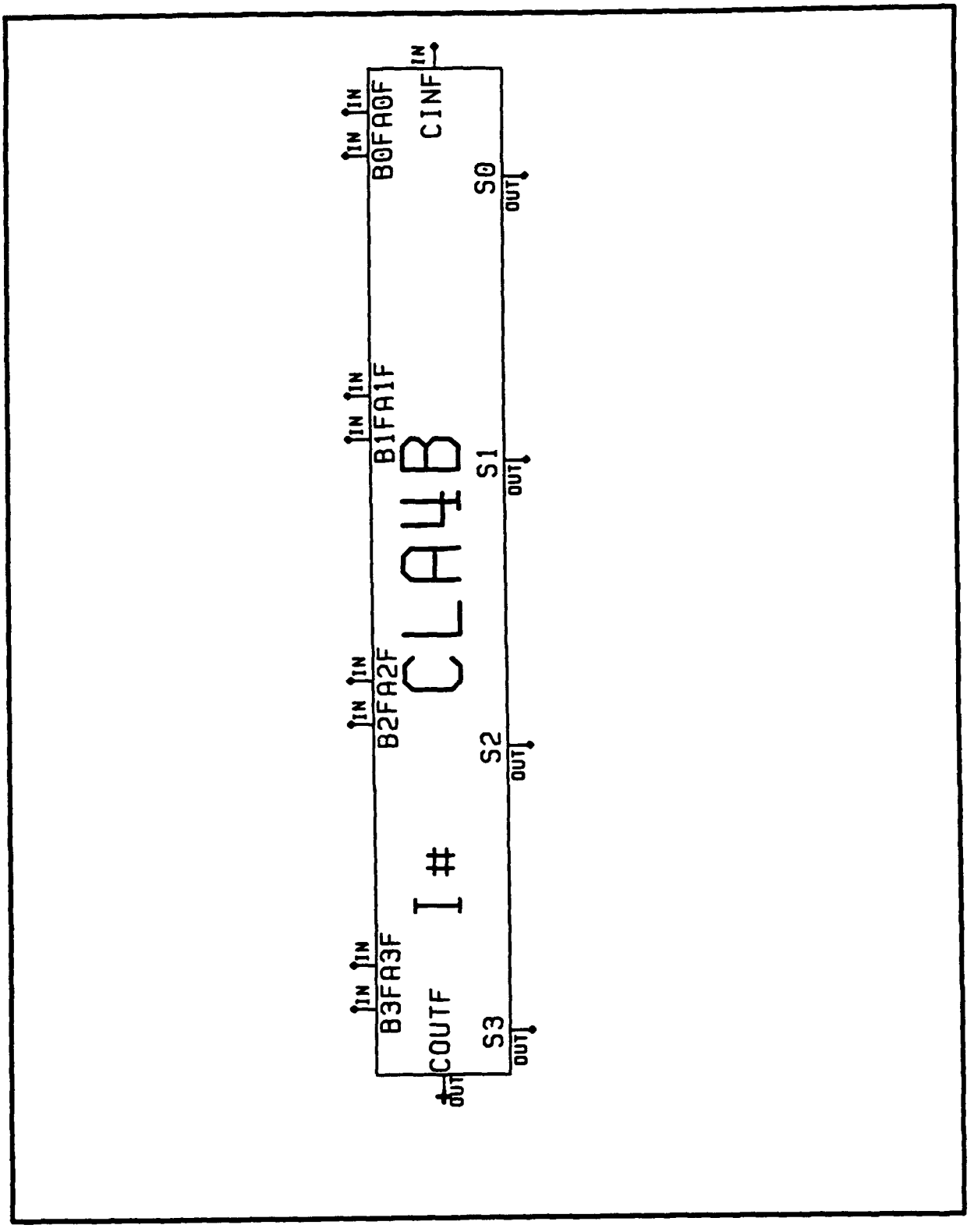

16 X 16 MULTIPLIER: MULT7
XFBUF
YF
I$1
NOR
I$61
INV
POUTF
X1
I$62
SINV
X1FBUF
X
I$65
SINV
XFBUF

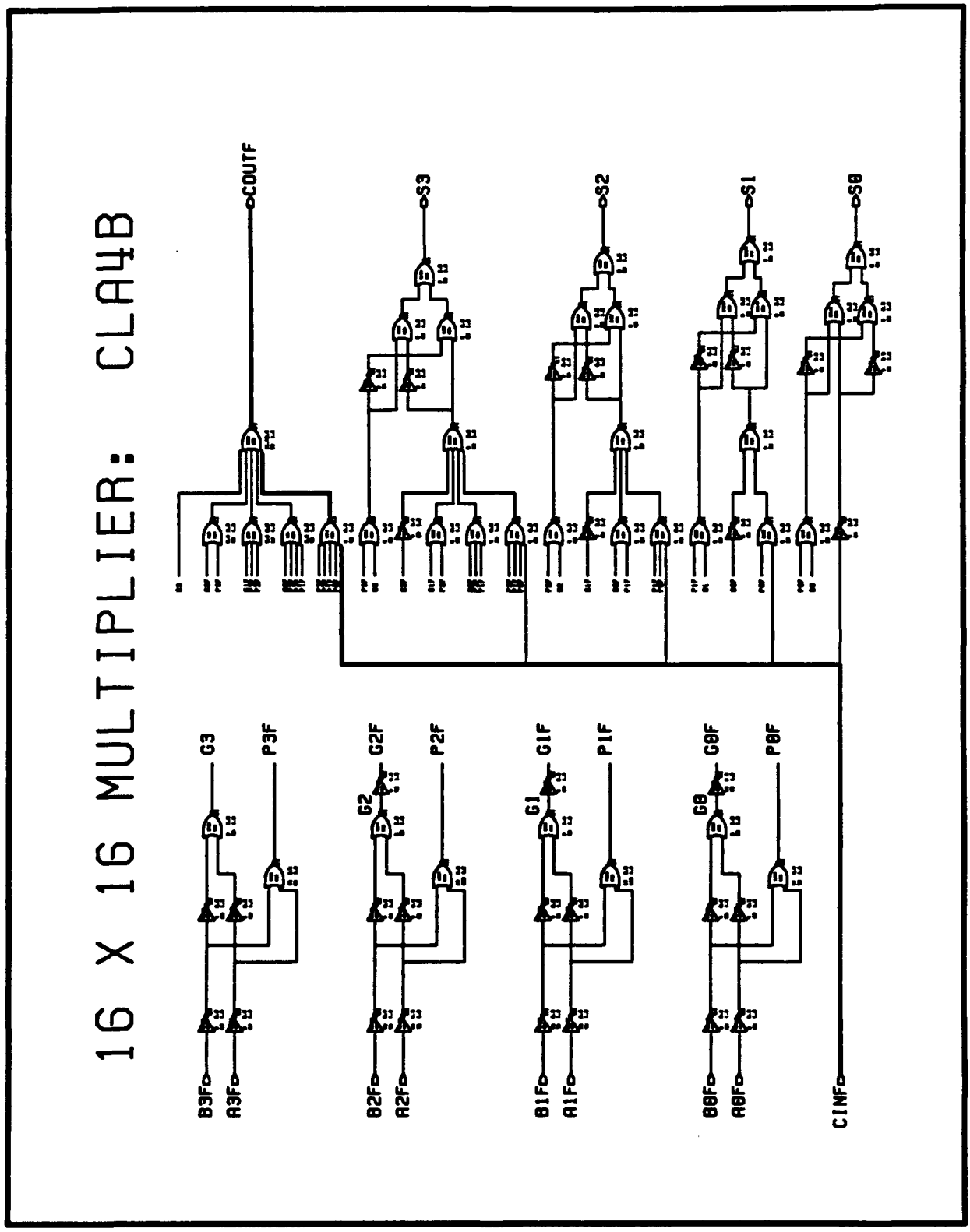

OUT
XFBUF
MULT8
I#
POUTF
OUT
YF
IN
X
IN

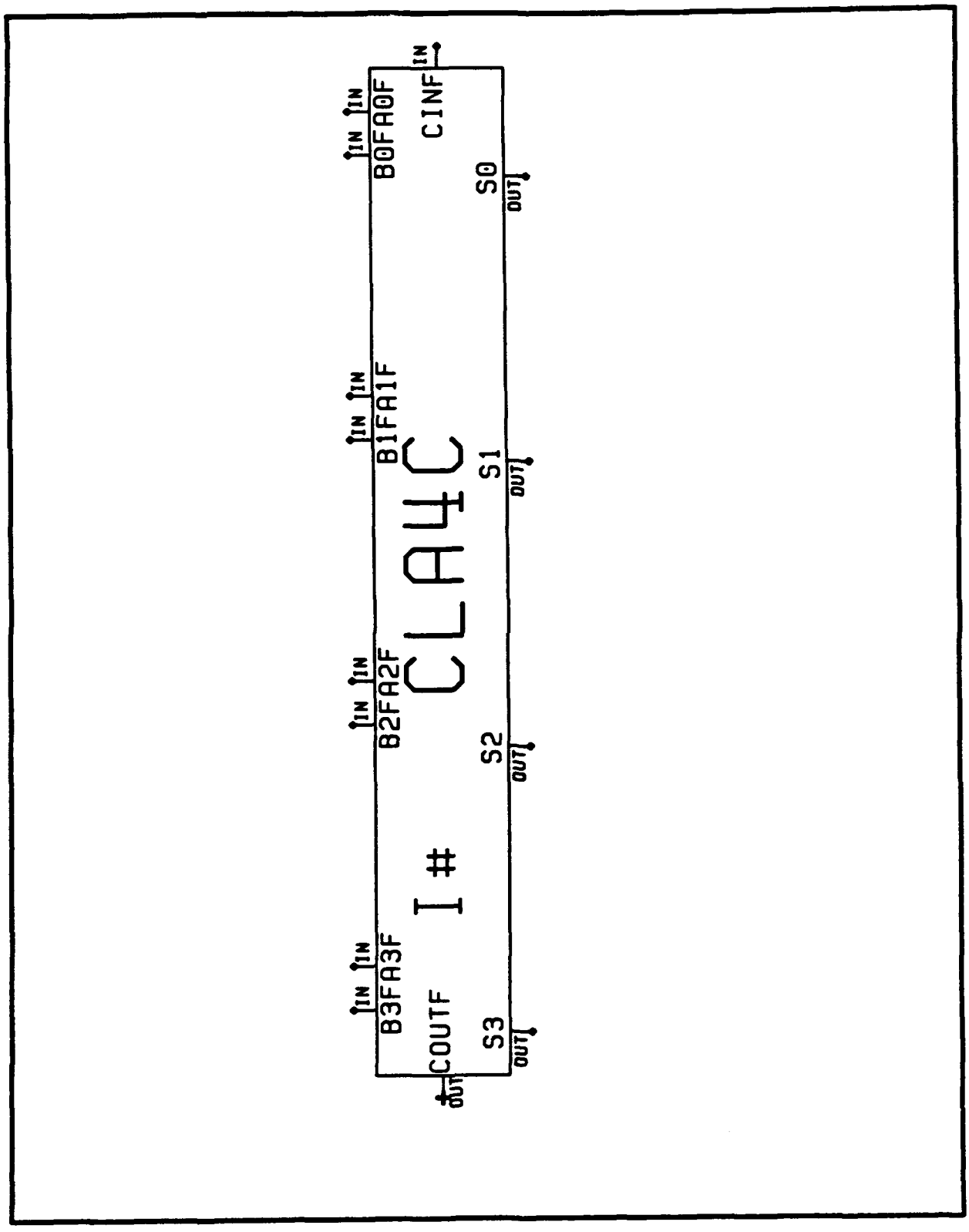

16 X 16 MULTIPLIER: MULT8
POUTF
XFBUF
YF
XFBUF
X
I361
INV
I$1
NOR
I$365
SINV
4.5 2.5
31.5 1.2
3 2.5
21 1.2
1.2
1.2
2.5
1.2
8
210
4
20

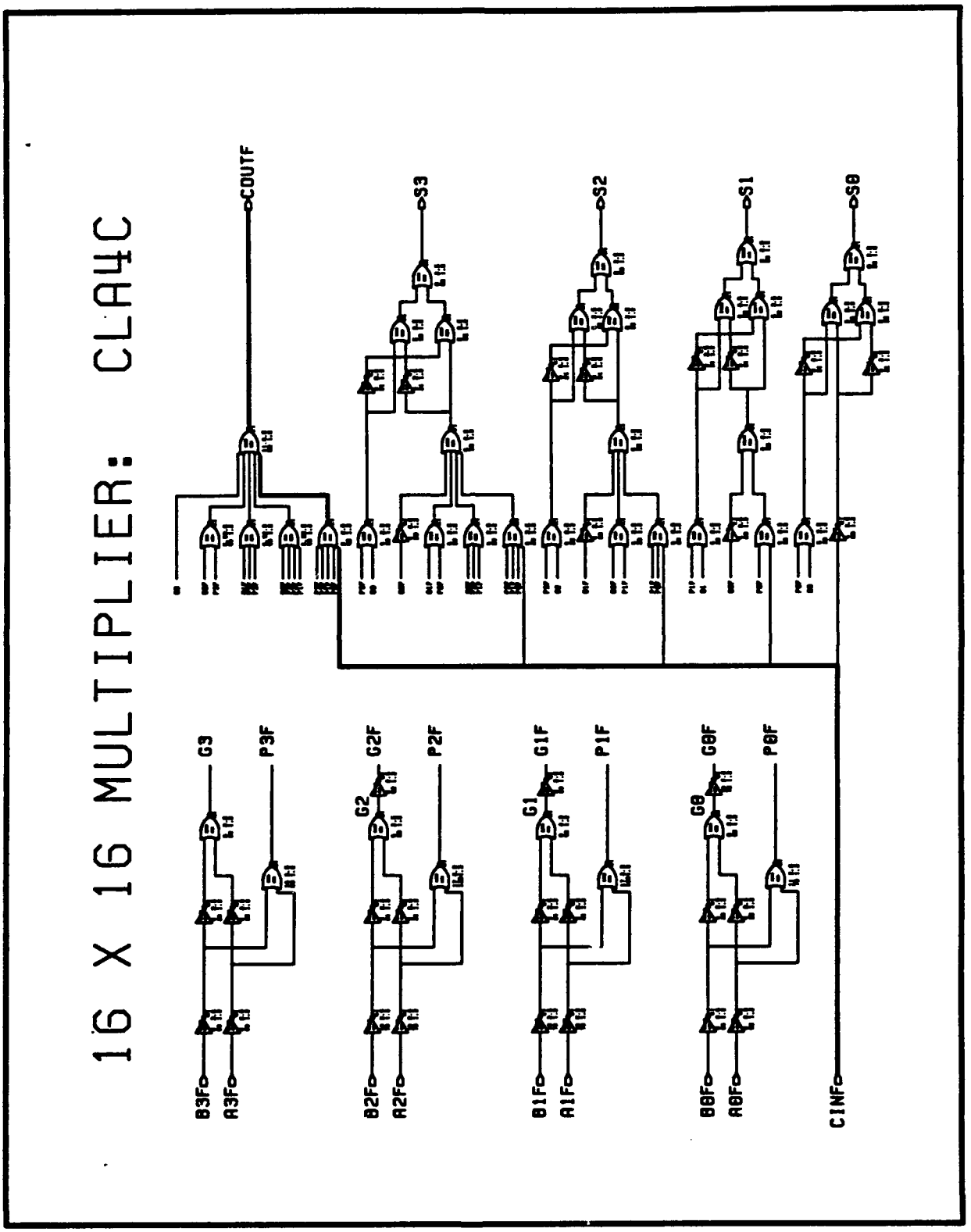

CLA4
I #
IN
B0FA0F
CINF
S0
OUT
B1FA1F
S1
B2FA2F
S2
B3F
SF
S3


16 X 16 MULTIPLIER: CLA4A
S3
S2
S1
S0
P3F
G2F
P2F
G1F
P1F
G0F
P0F
G2
G1
G0
B3F
B2F
A2F
B1F
A1F
B0F
A0F
C1NF


CLA4B
I #
B0FA0F
B1FA1F
B2FA2F
B3FA3F
CINF
COUTF
S0
S1
S2
S3
IN
OUT


16 X 16 MULTIPLIER: CLA4B
COUTF
S3
S2
S1
S0
G3
P3F
G2F
P2F
G2
G1F
P1F
G1
G0F
P0F
G0
B3F
A3F
B2F
A2F
B1F
A1F
B0F
A0F
CINF


CLA4C
I #
B0FA0F
B1FA1F
B2FA2F
B3FA3F
CINF
COUTF
S0
S1
S2
S3
IN
OUT


16 X 16 MULTIPLIER: CLA4C
COUTF
S3
S2
S1
S0
G3
P3F
G2F
P2F
G2
G1F
P1F
G1
G0F
P0F
G0
B3F
A3F
B2F
A2F
B1F
A1F
B0F
A0F
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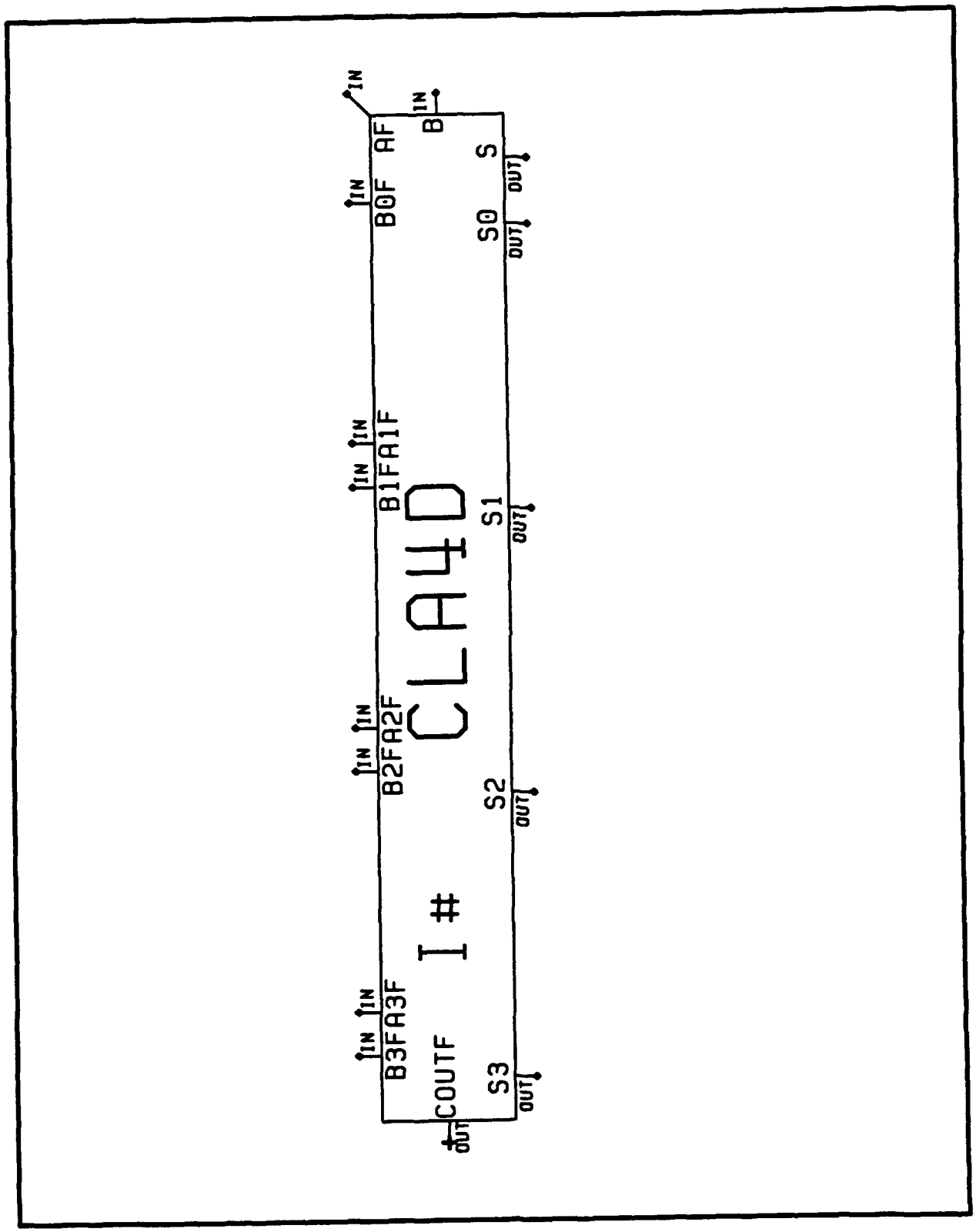
CLA4D
I #
IN
B
AF
B0F
S
S0
S1
S2
S3
B1FA1F
B2FA2F
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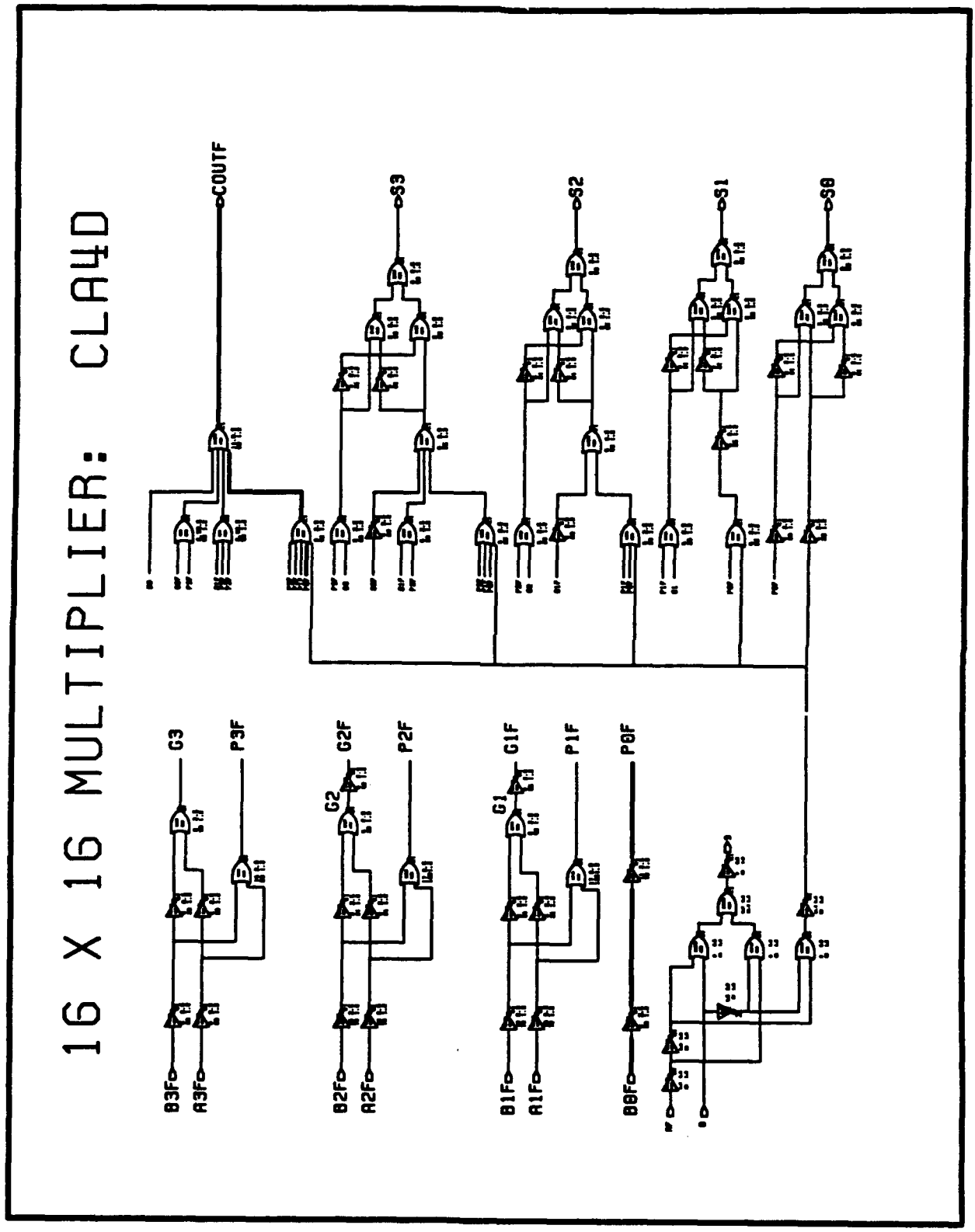
COUTF
OUT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COUTF
S3
S2
S1
S0
G3
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G2F
G2
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P1F
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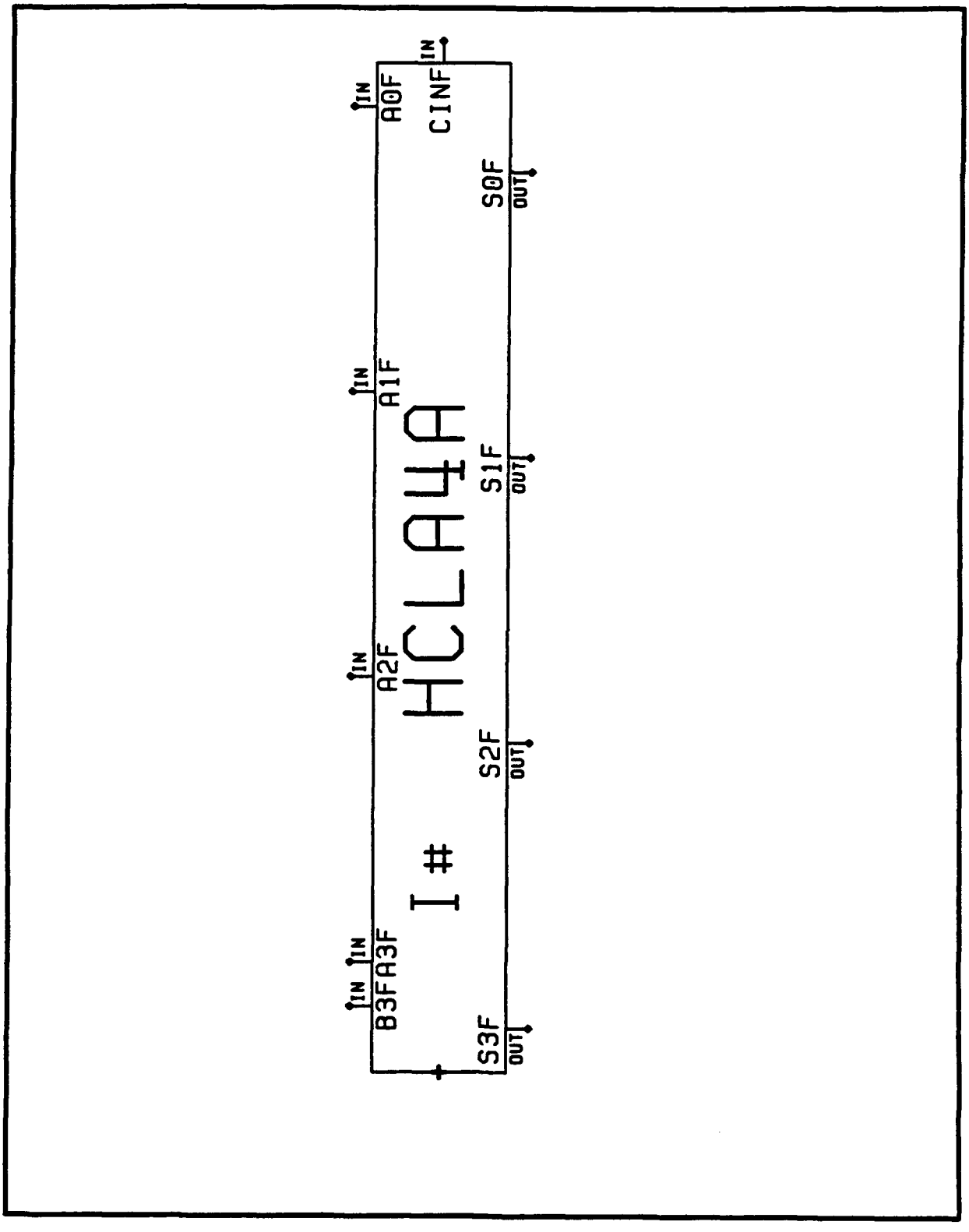
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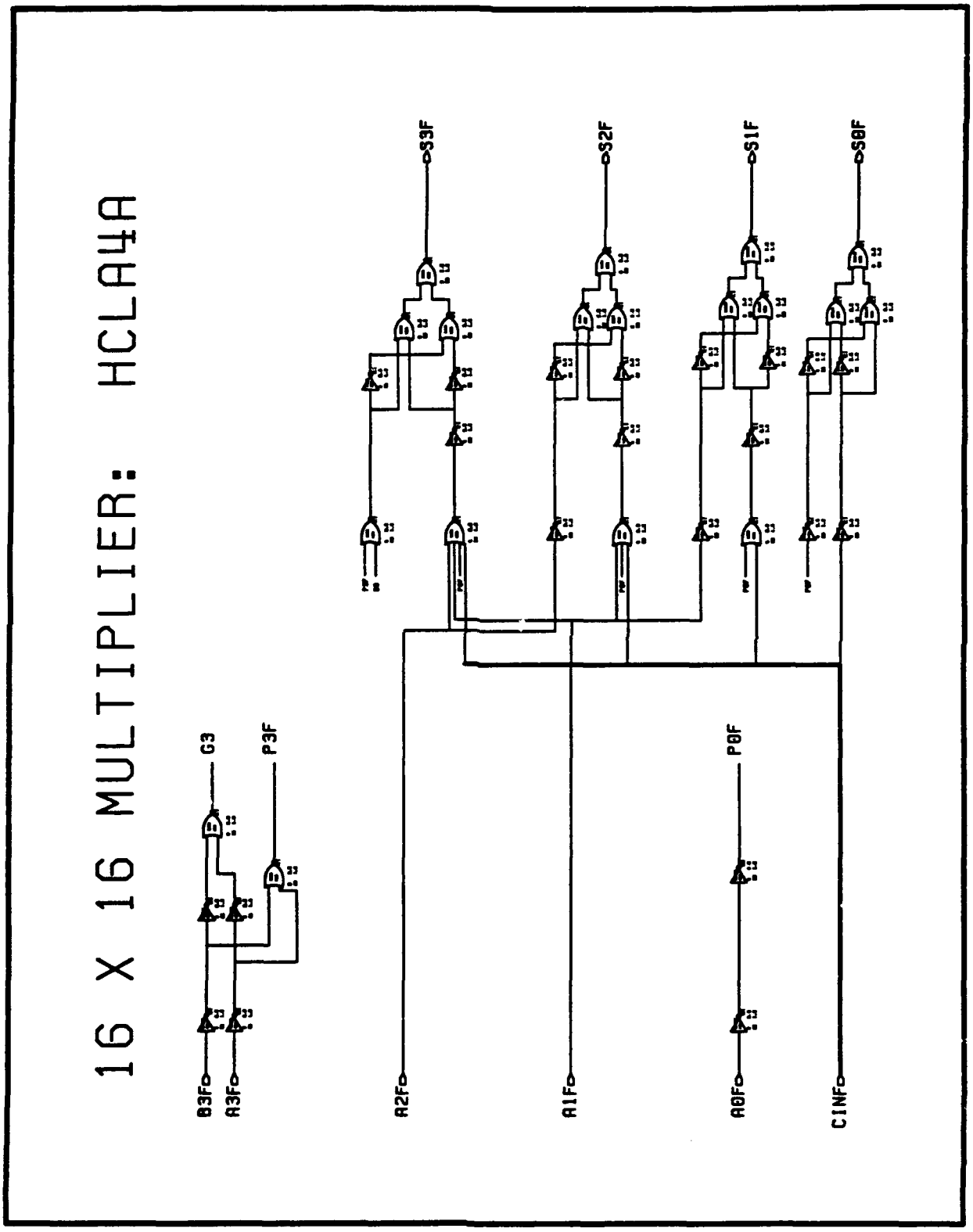
S3F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S3F
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S0F
G3
P3F
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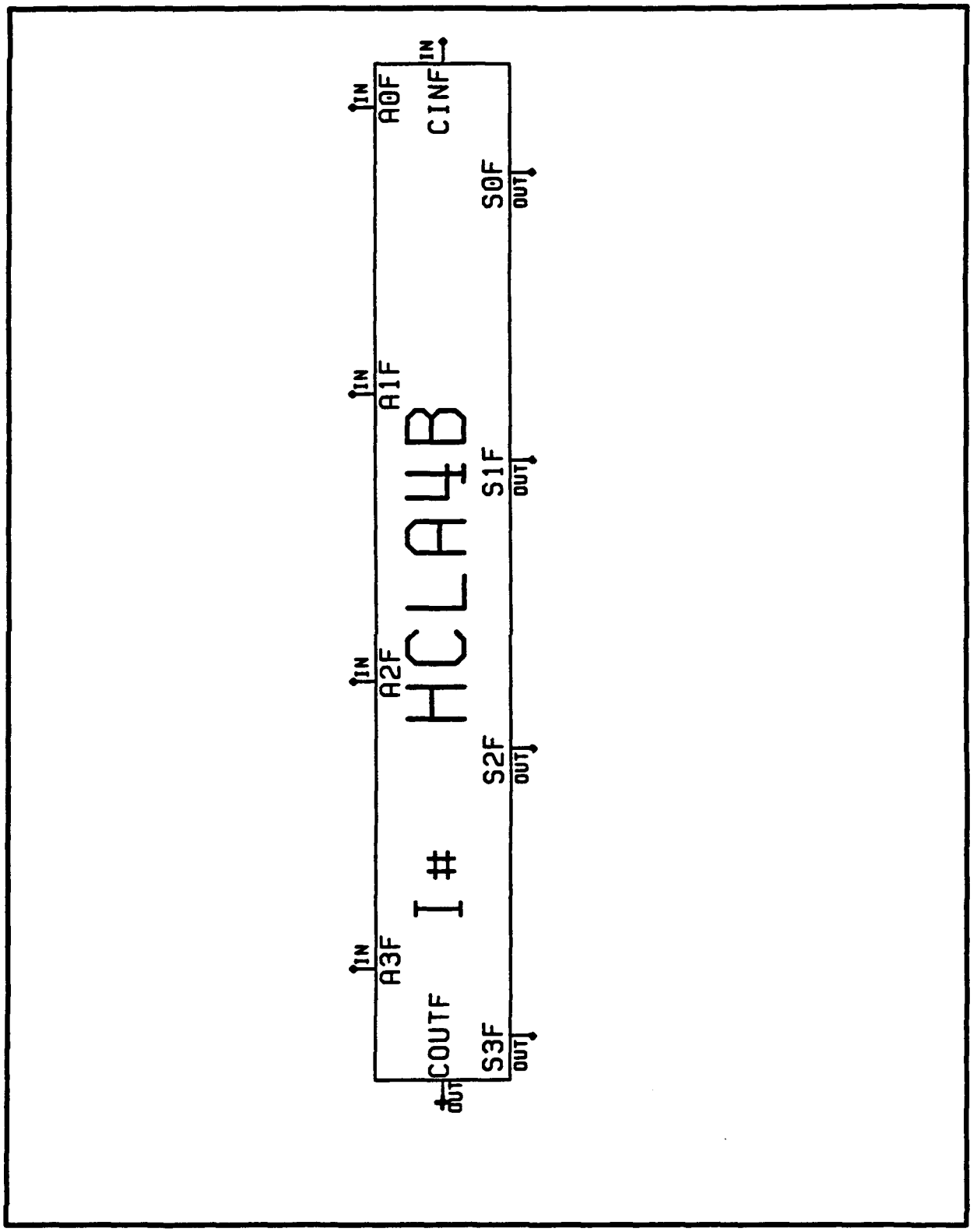
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I #
IN
A0F
CINF
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OUT
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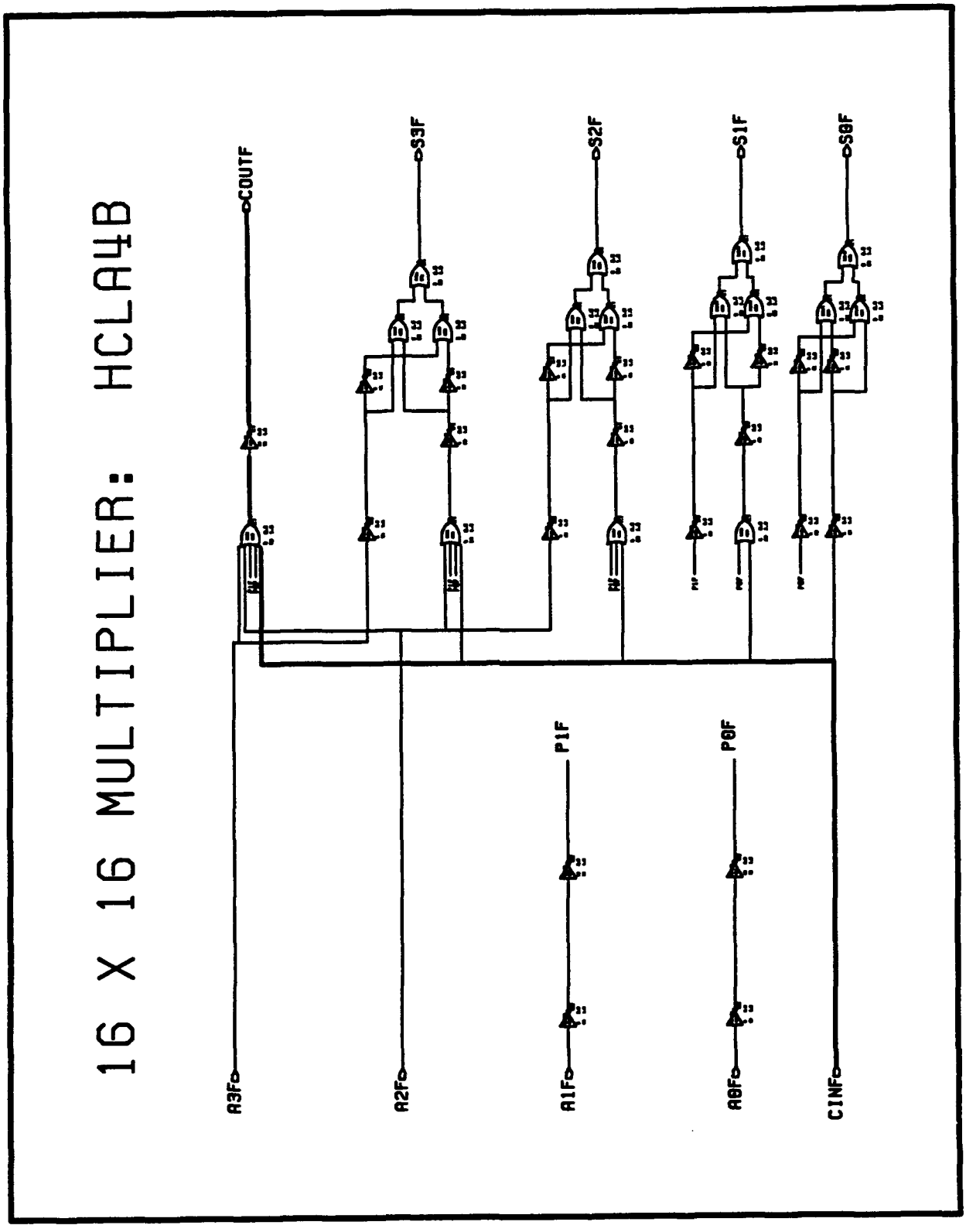
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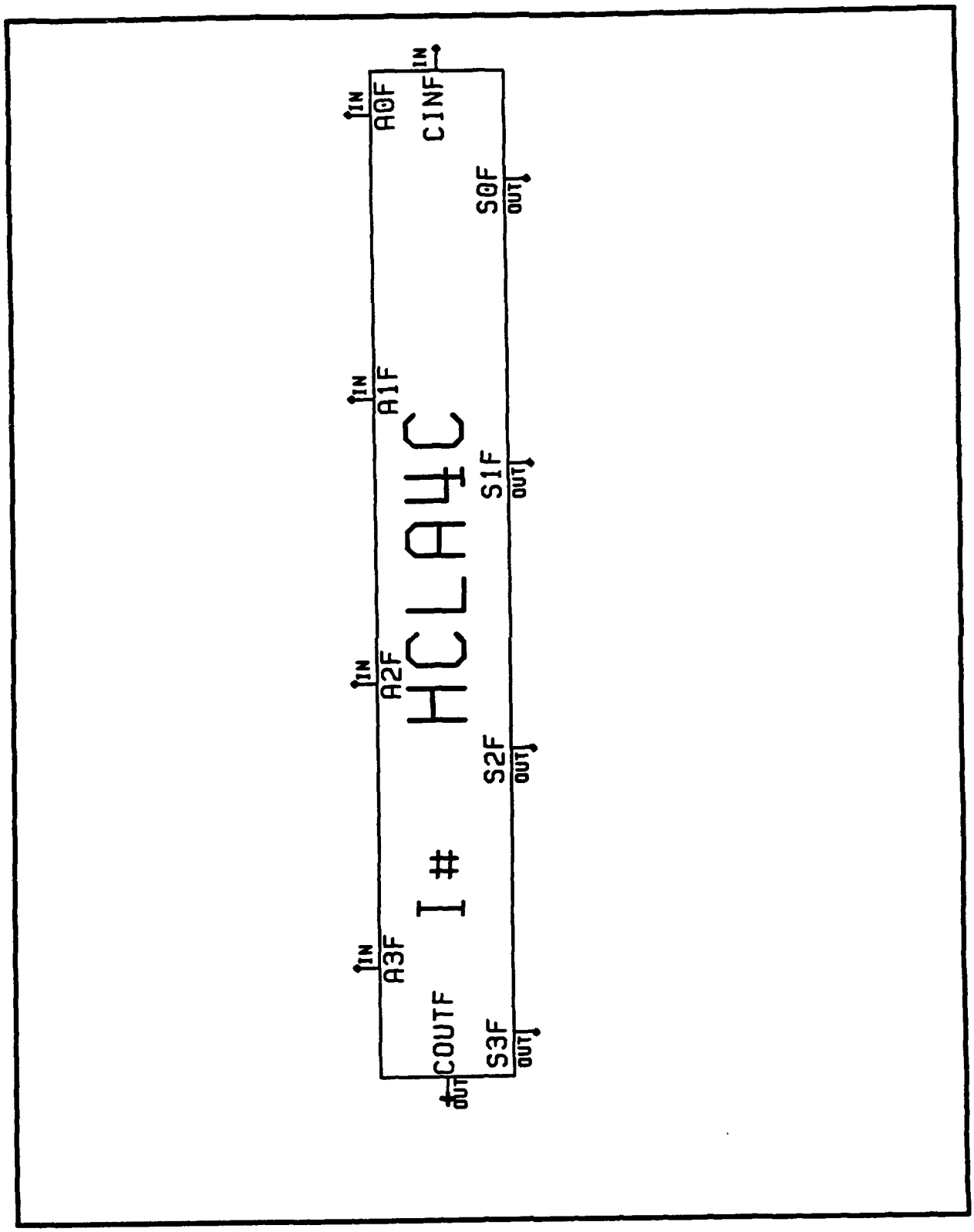
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IN CINF
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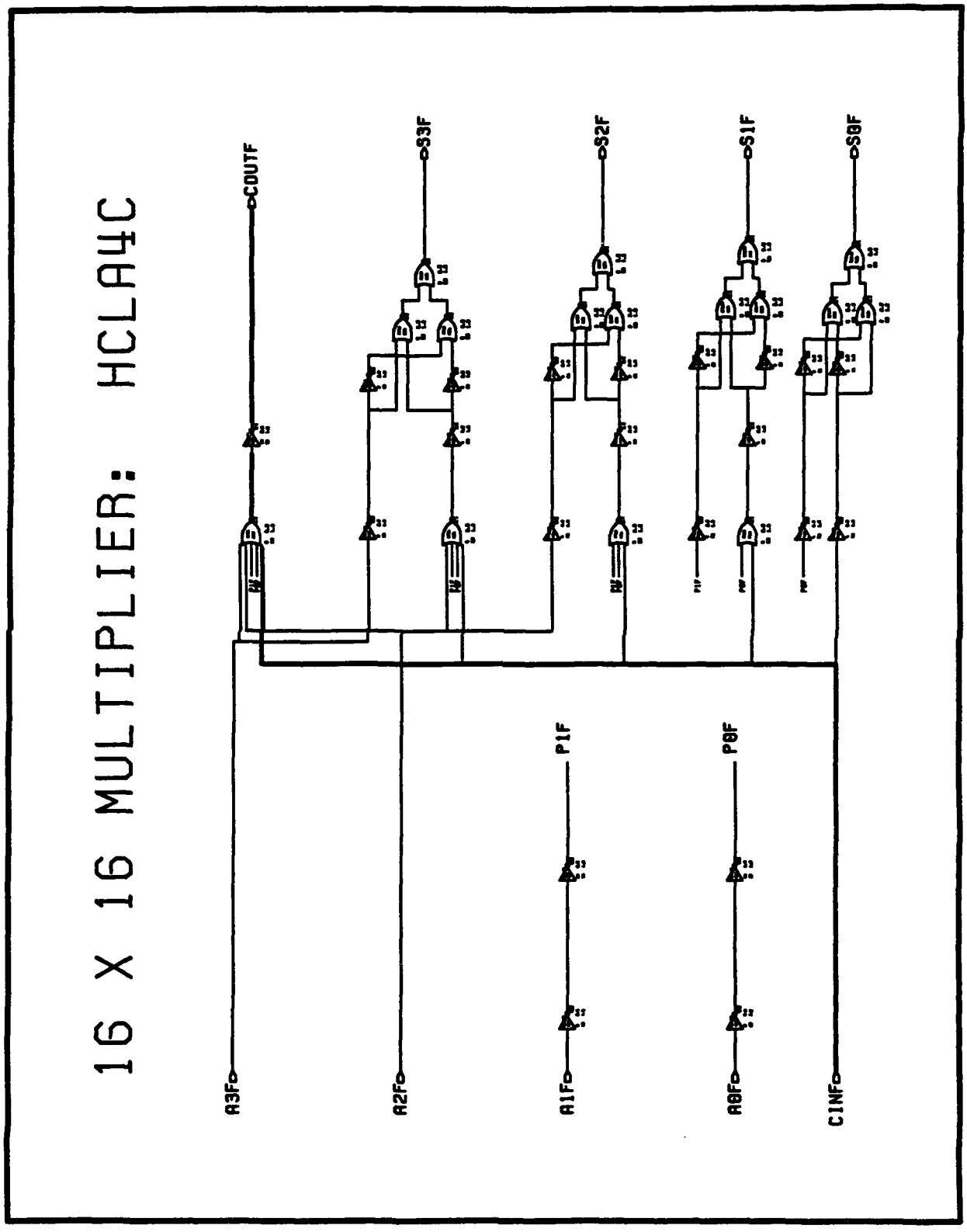
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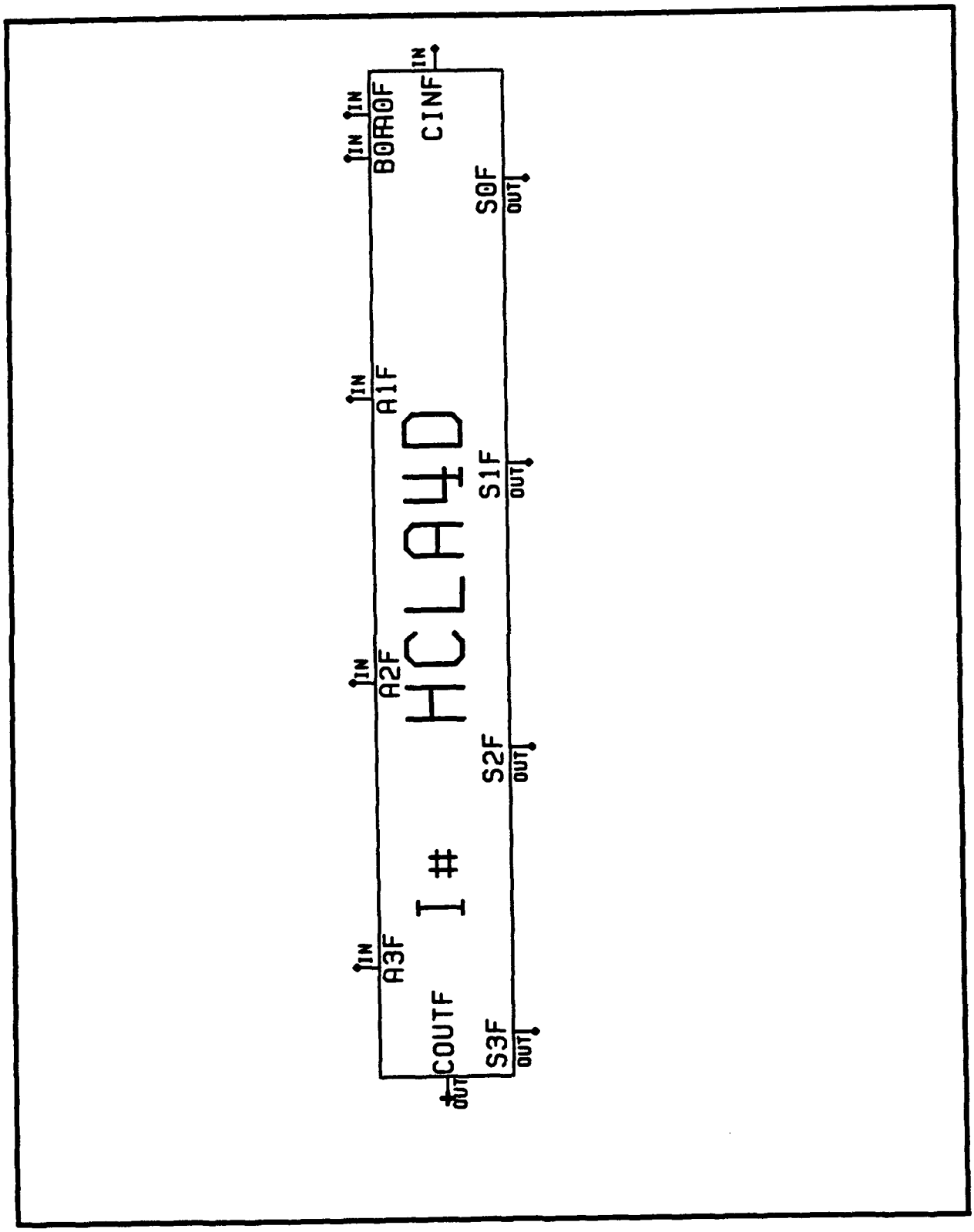
HCLA4D
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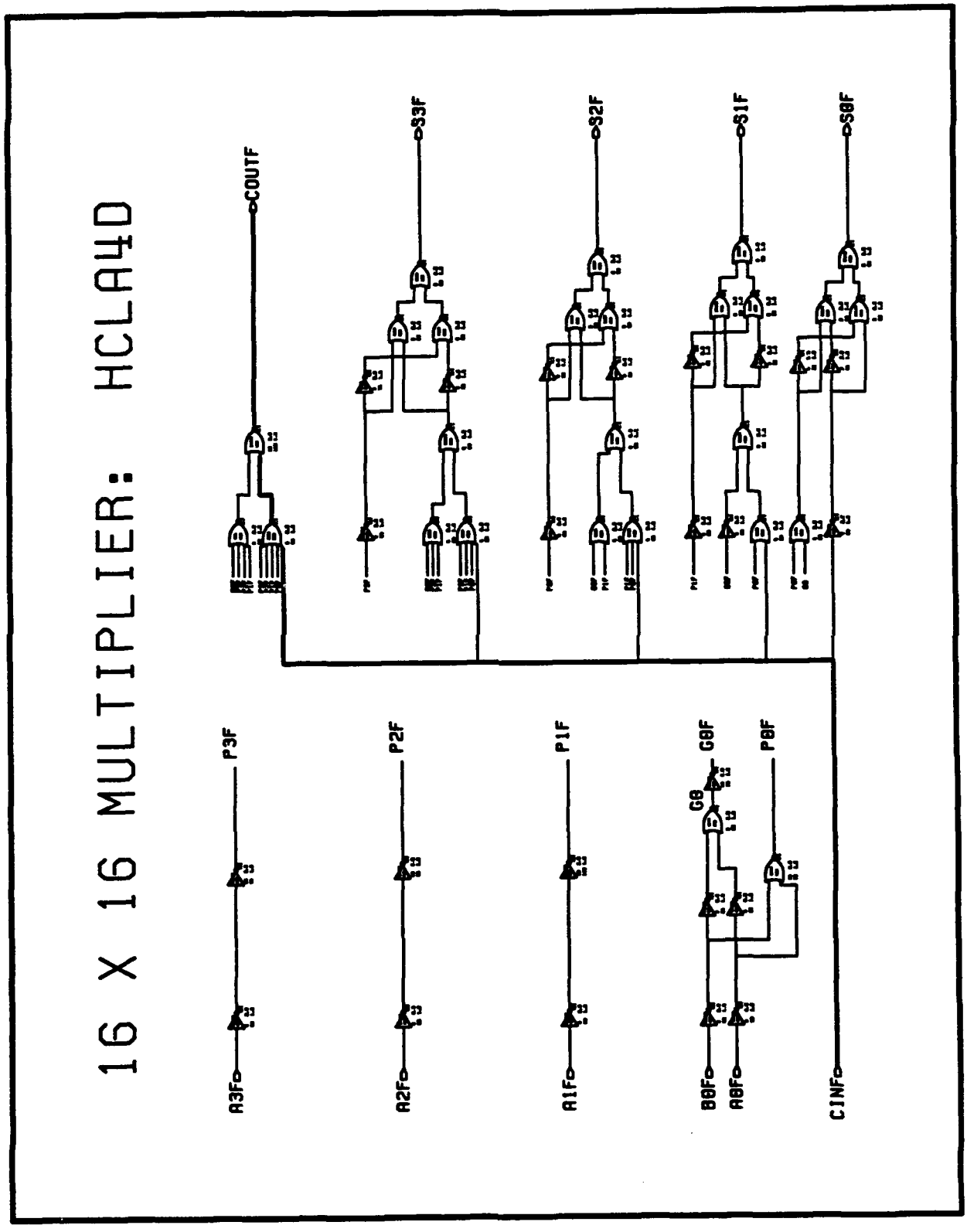
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S2F
S1F
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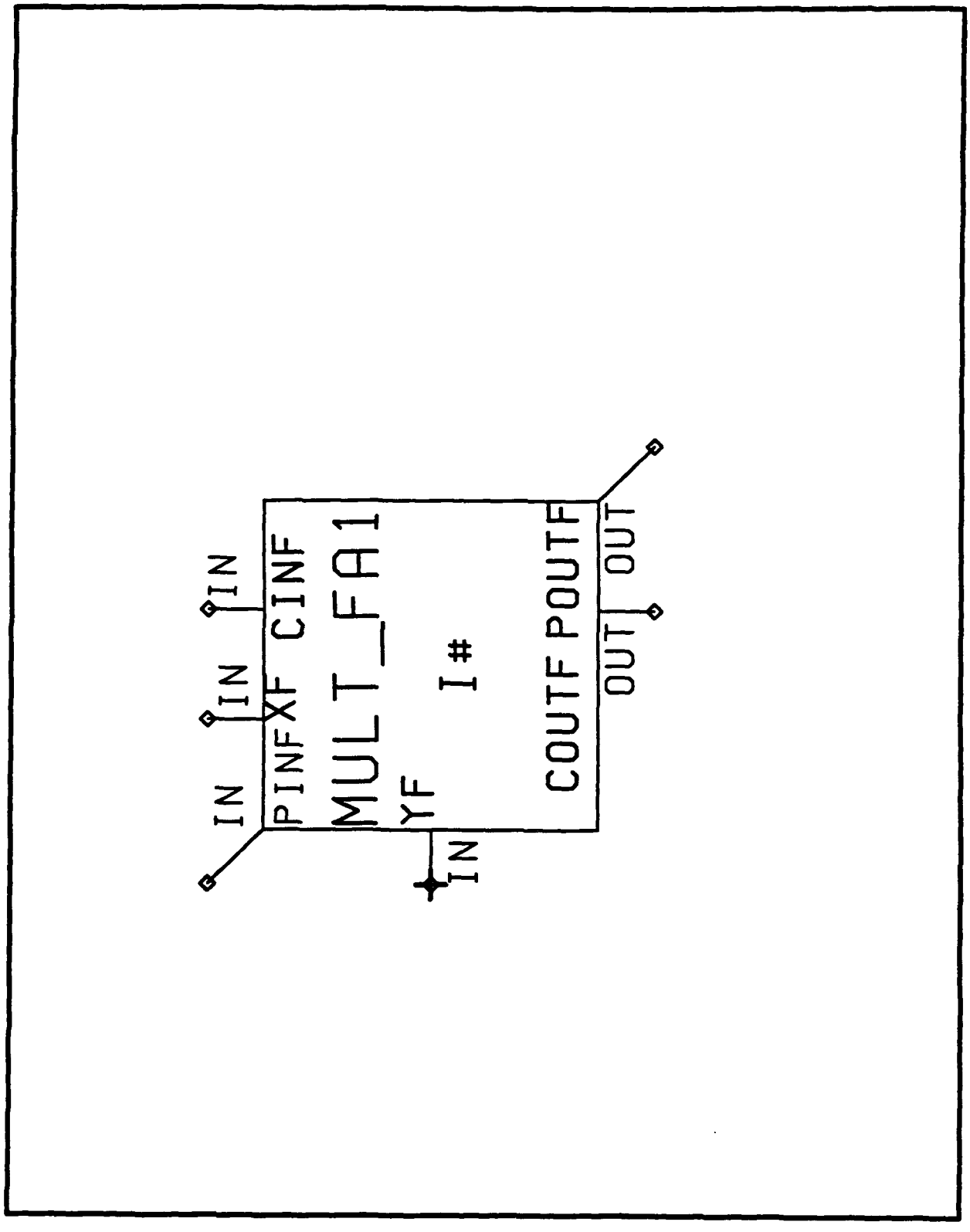
CINF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CINF
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I#
YF
COUTF
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OUT
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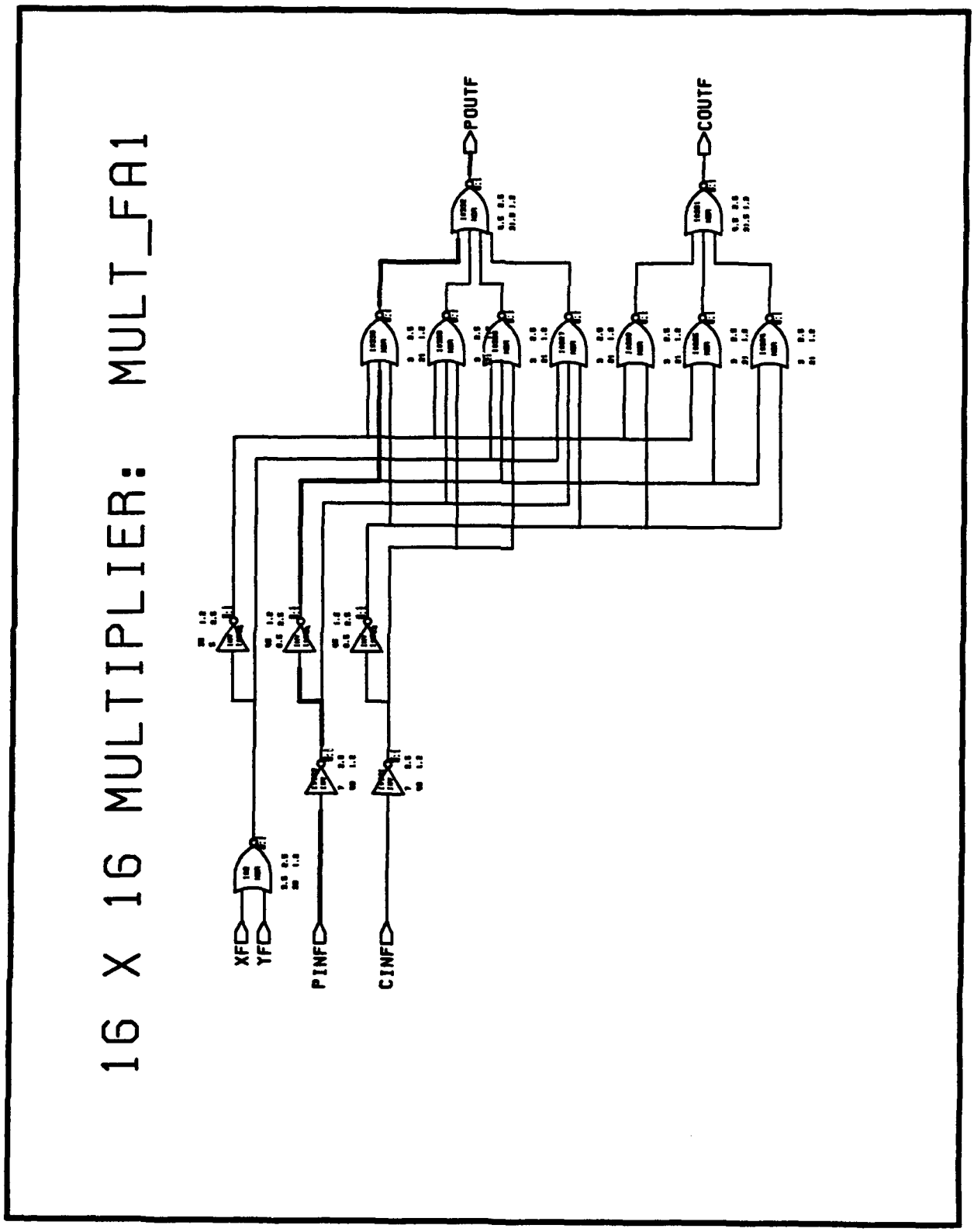
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COUTF
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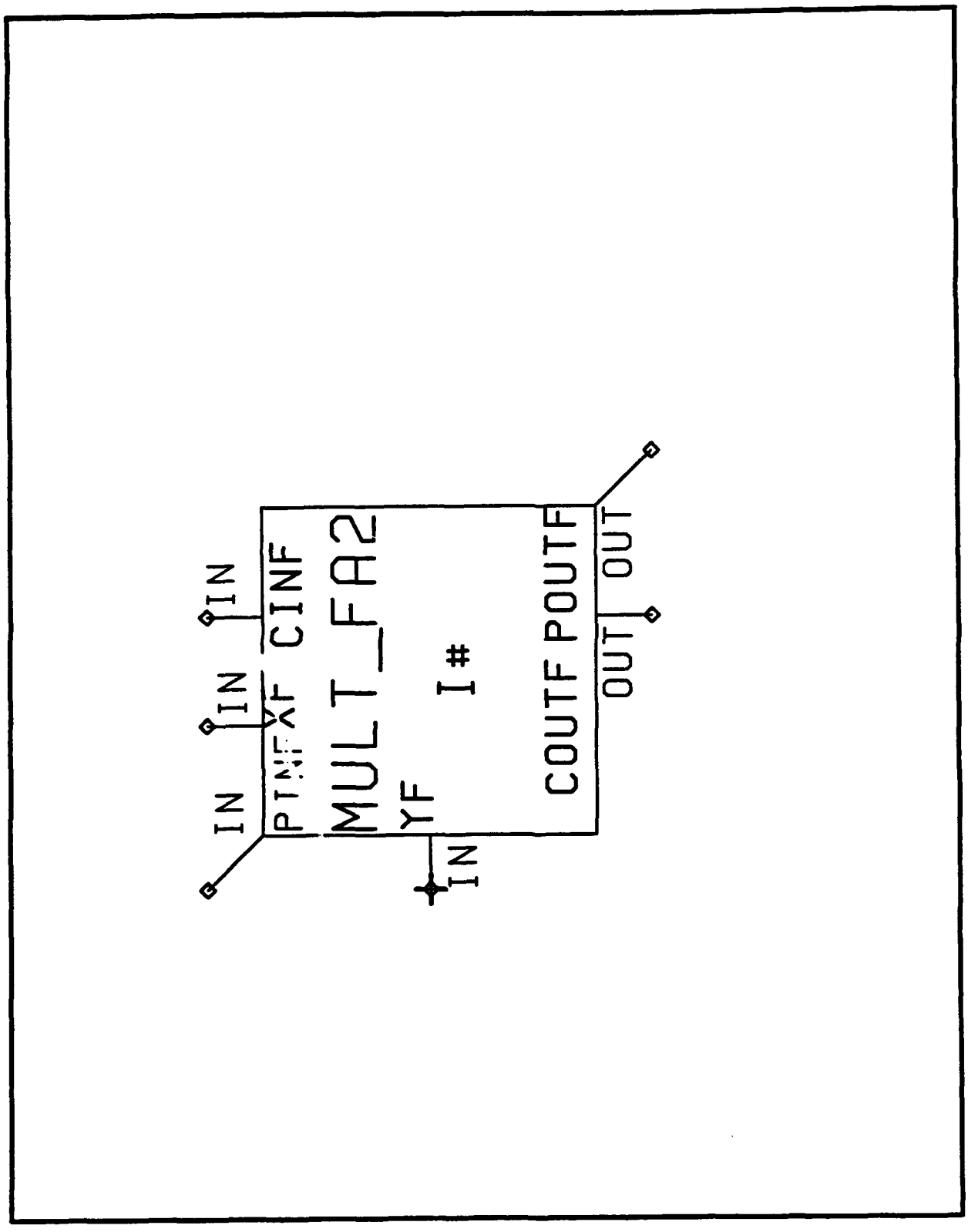
CINFD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I#
YF
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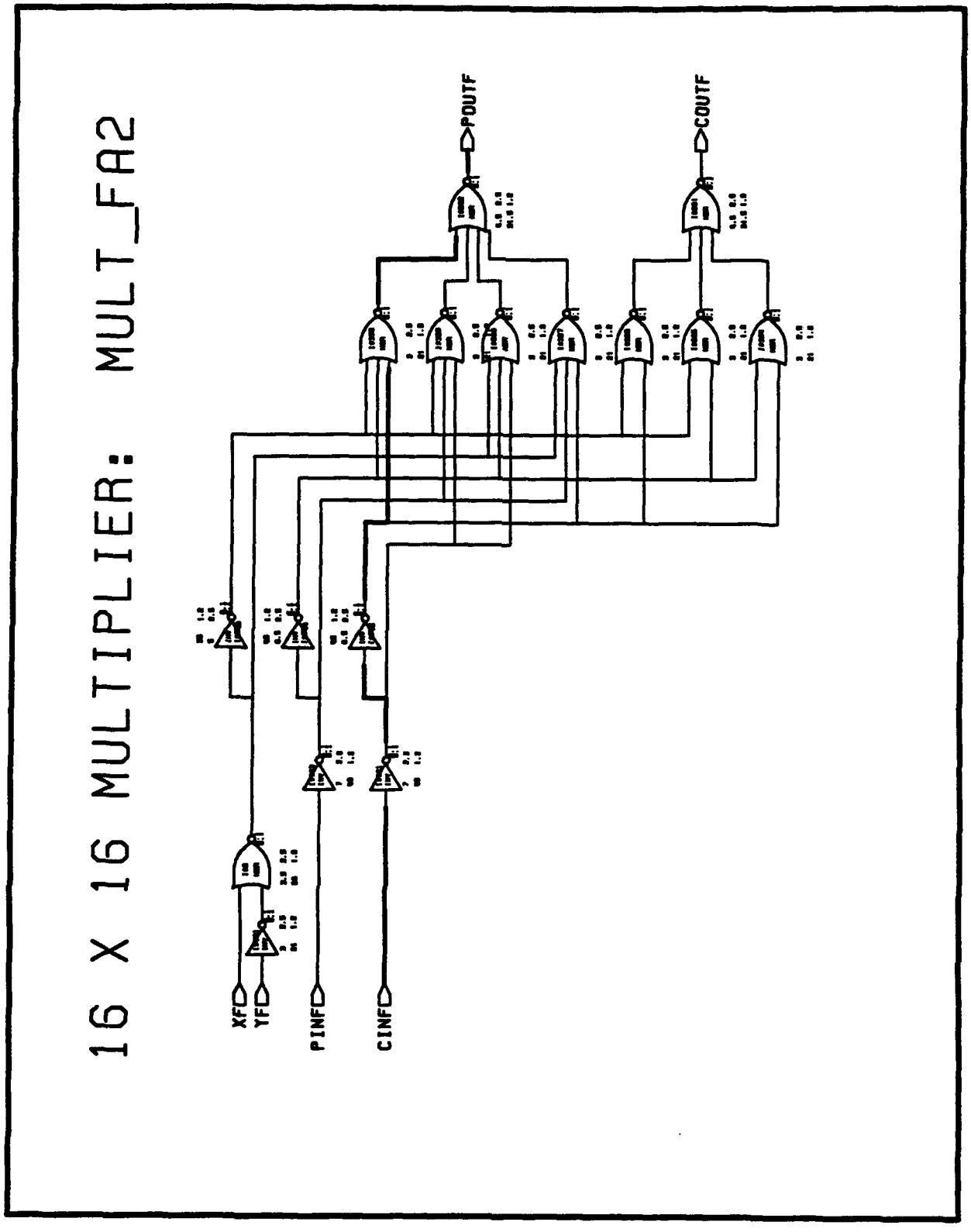
OUT
OUT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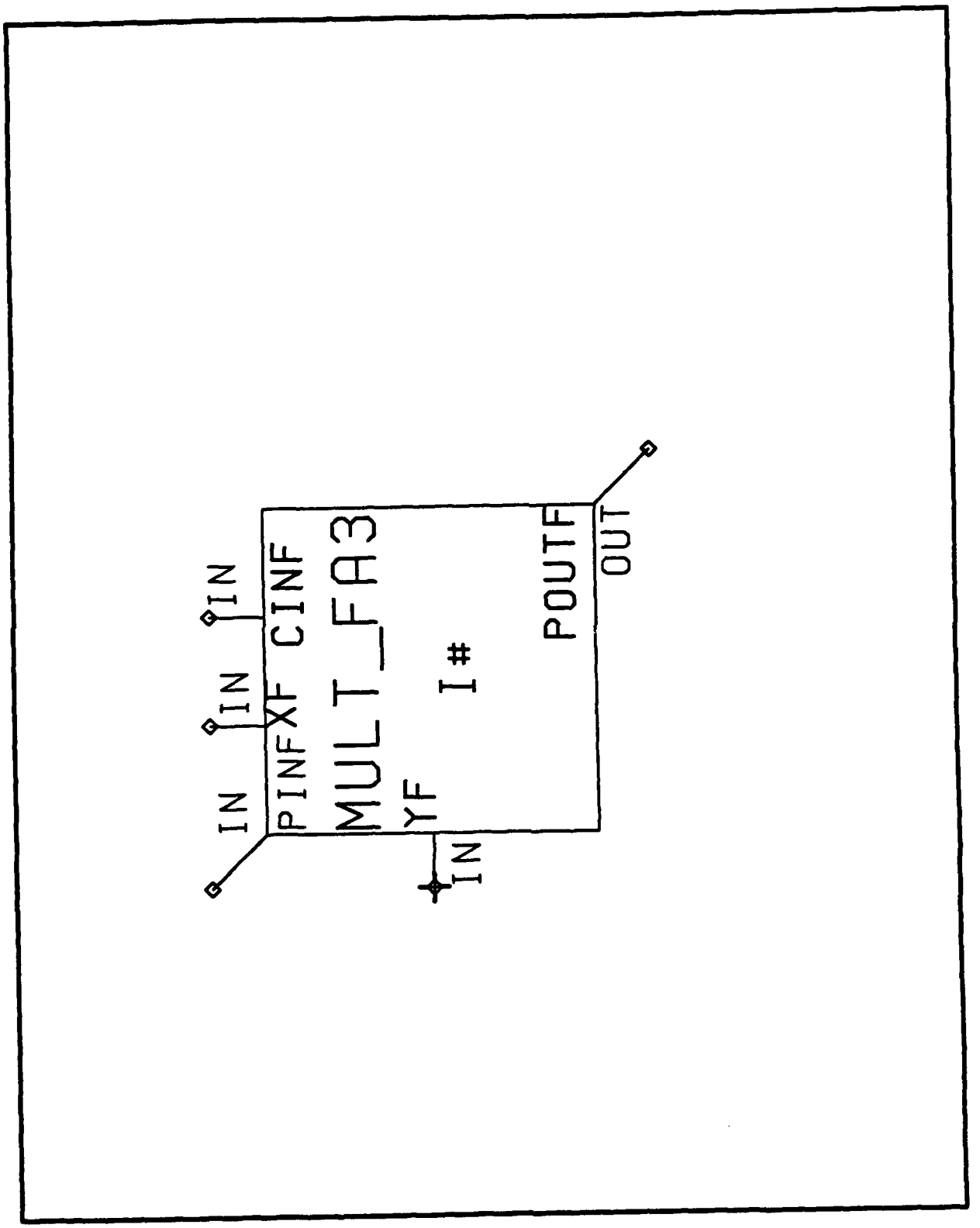
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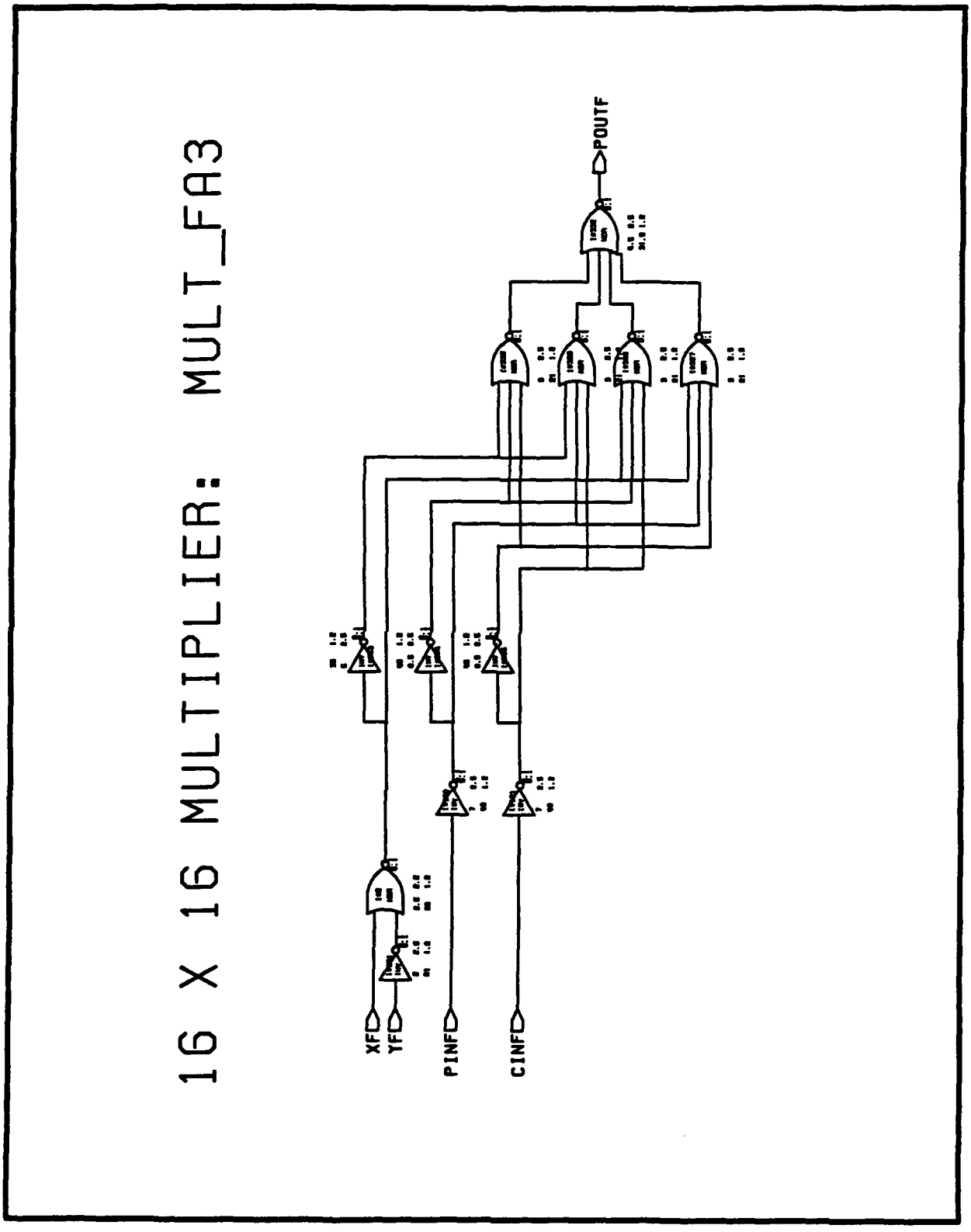
POUTF
OUT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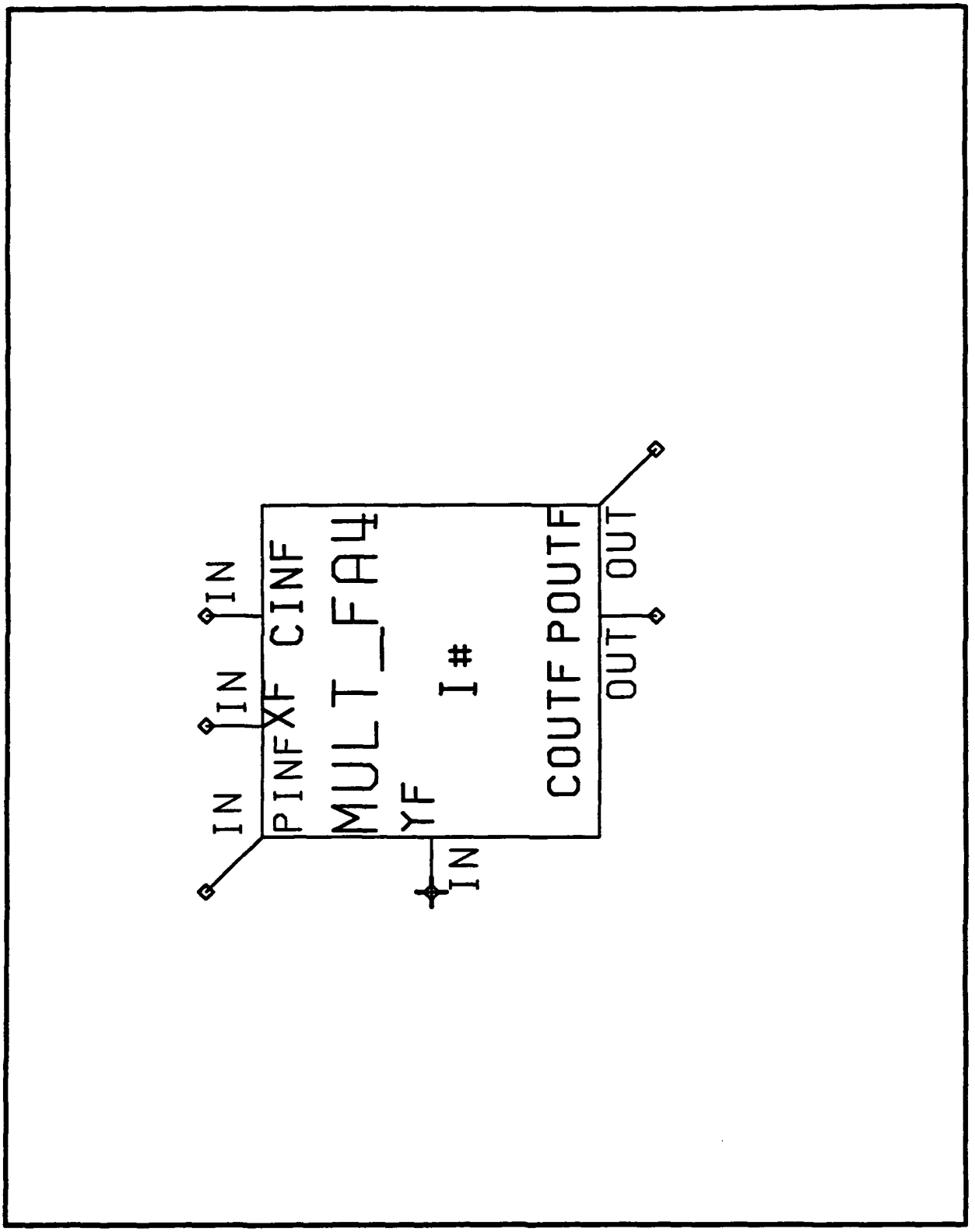
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OUT
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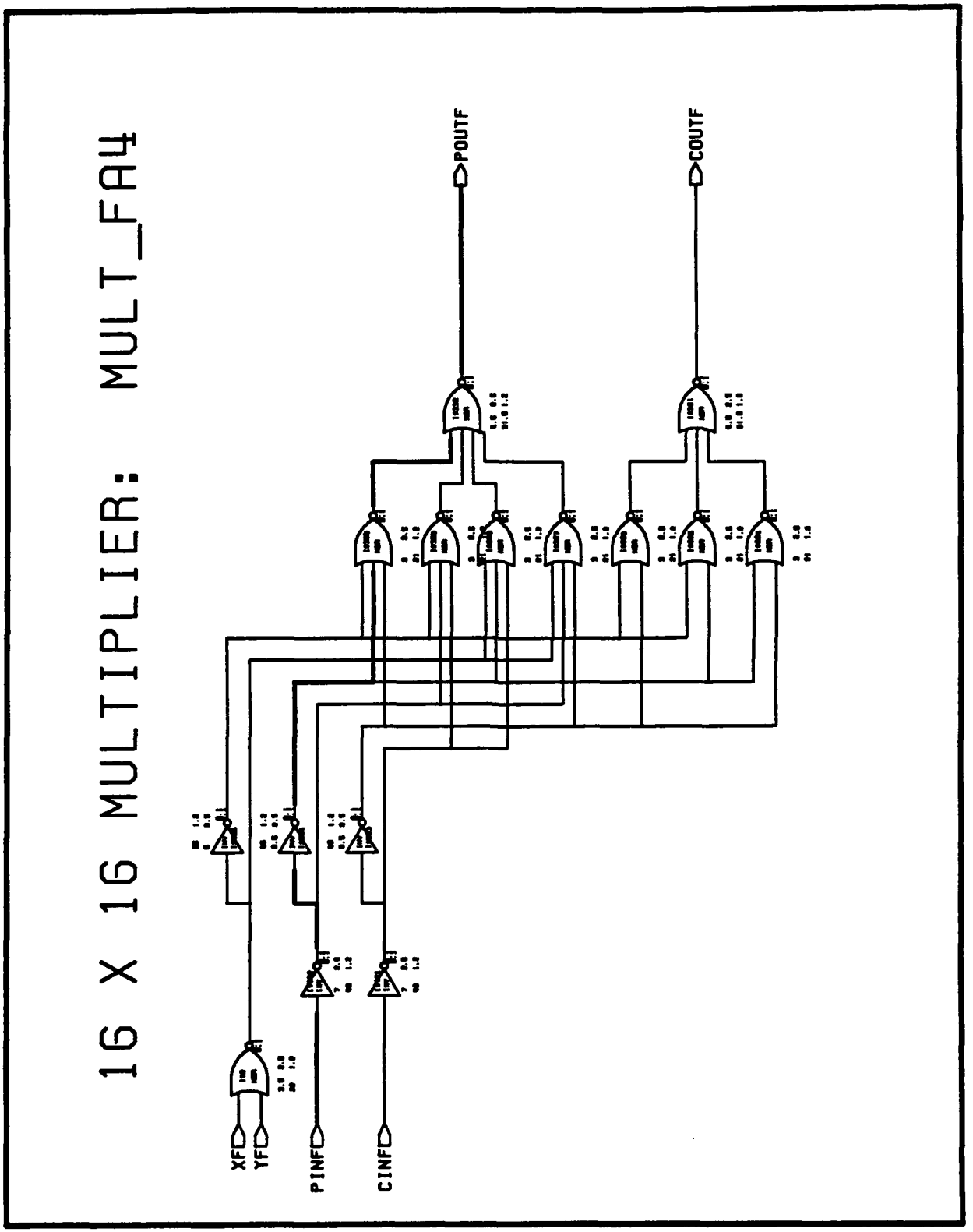
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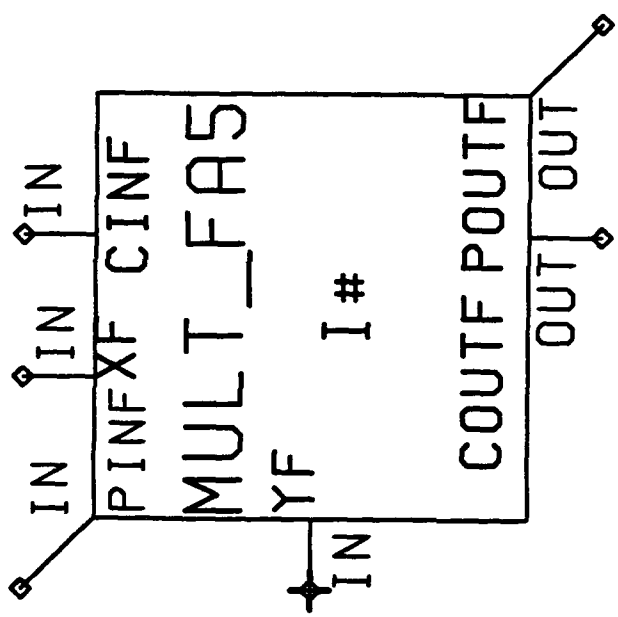
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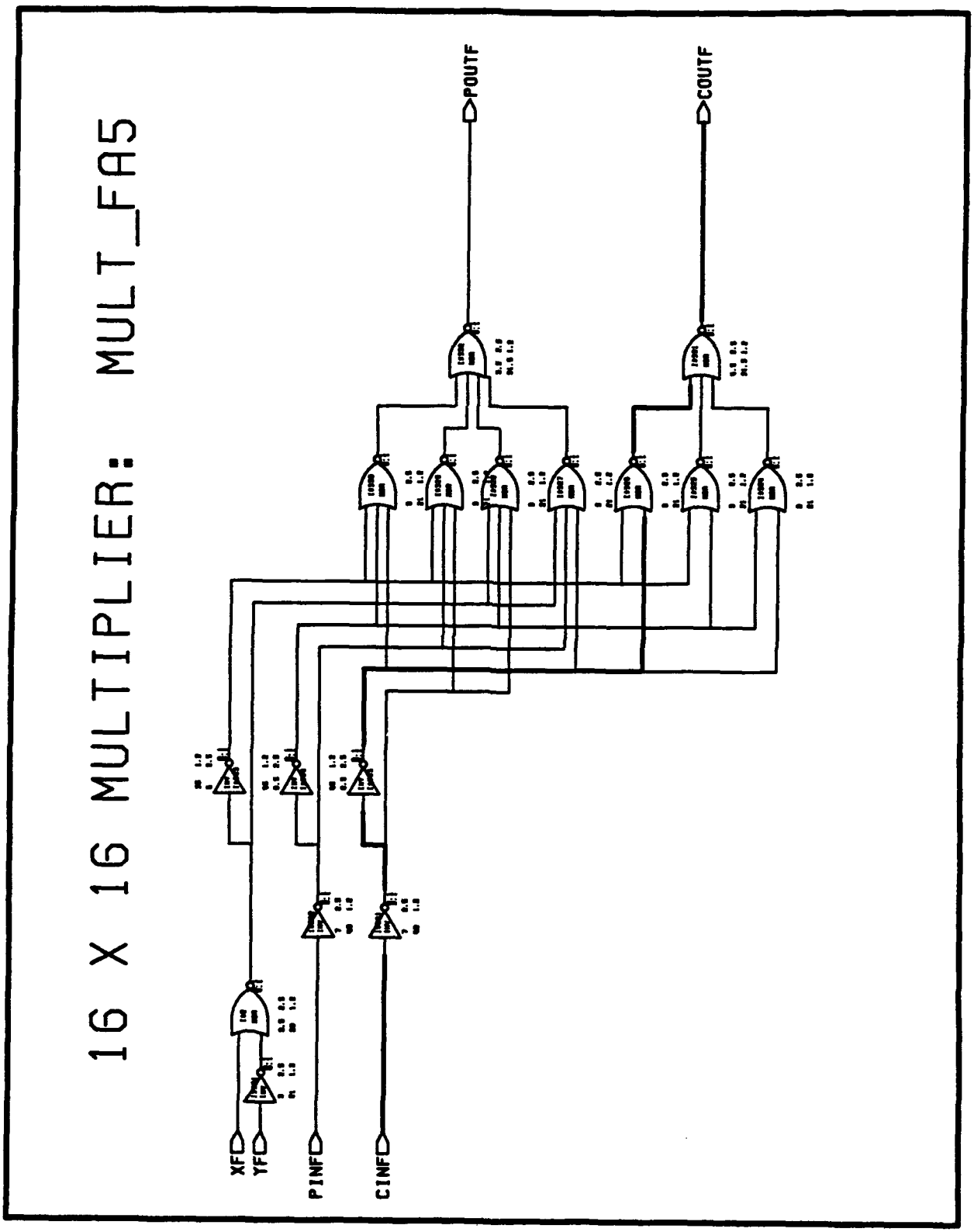
YF
I#
COUTF POUTF
OUT OUT
IN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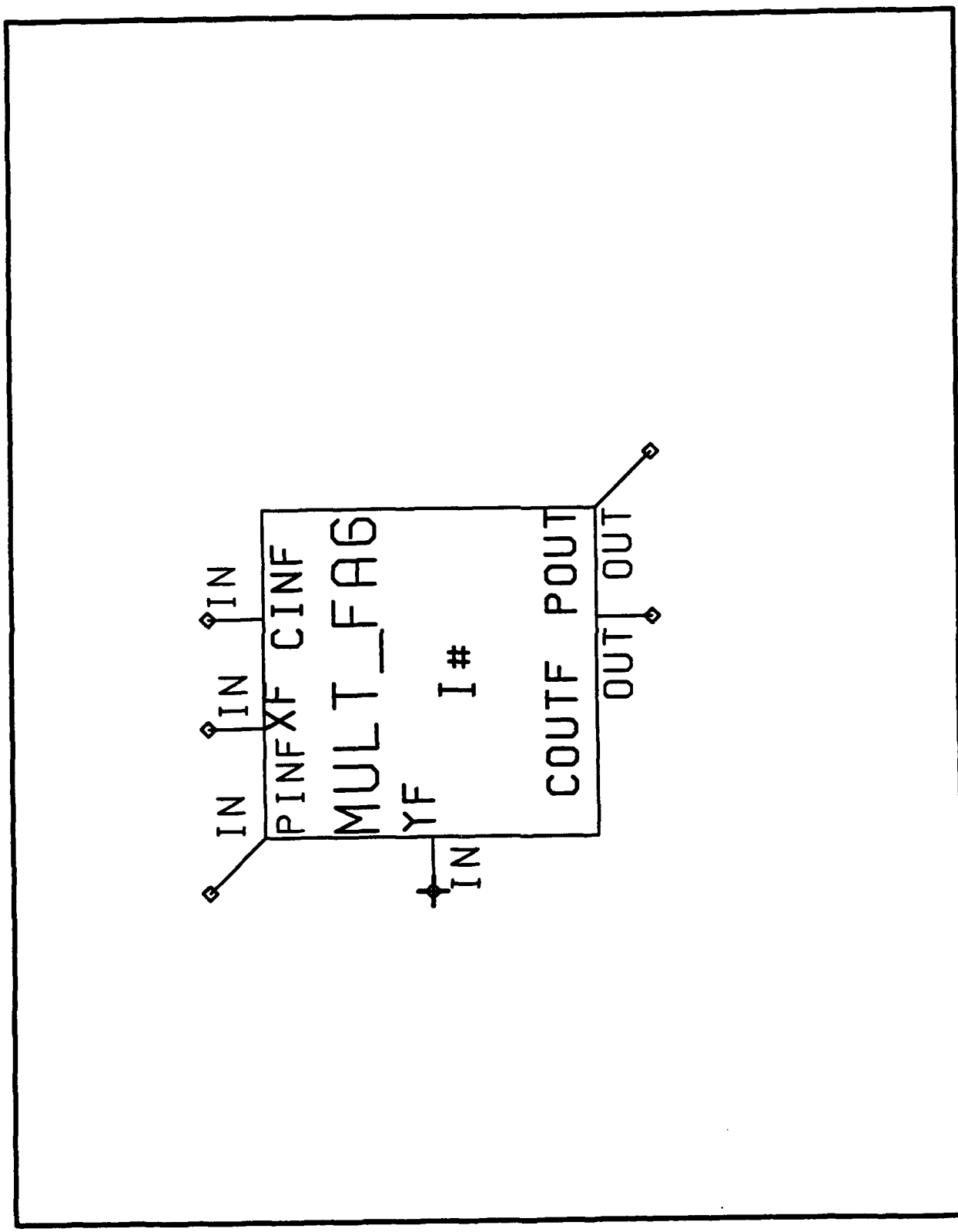
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PINF
XF
CINF
MULT_FA6
YF
I#
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COUTF
POUT
OUT
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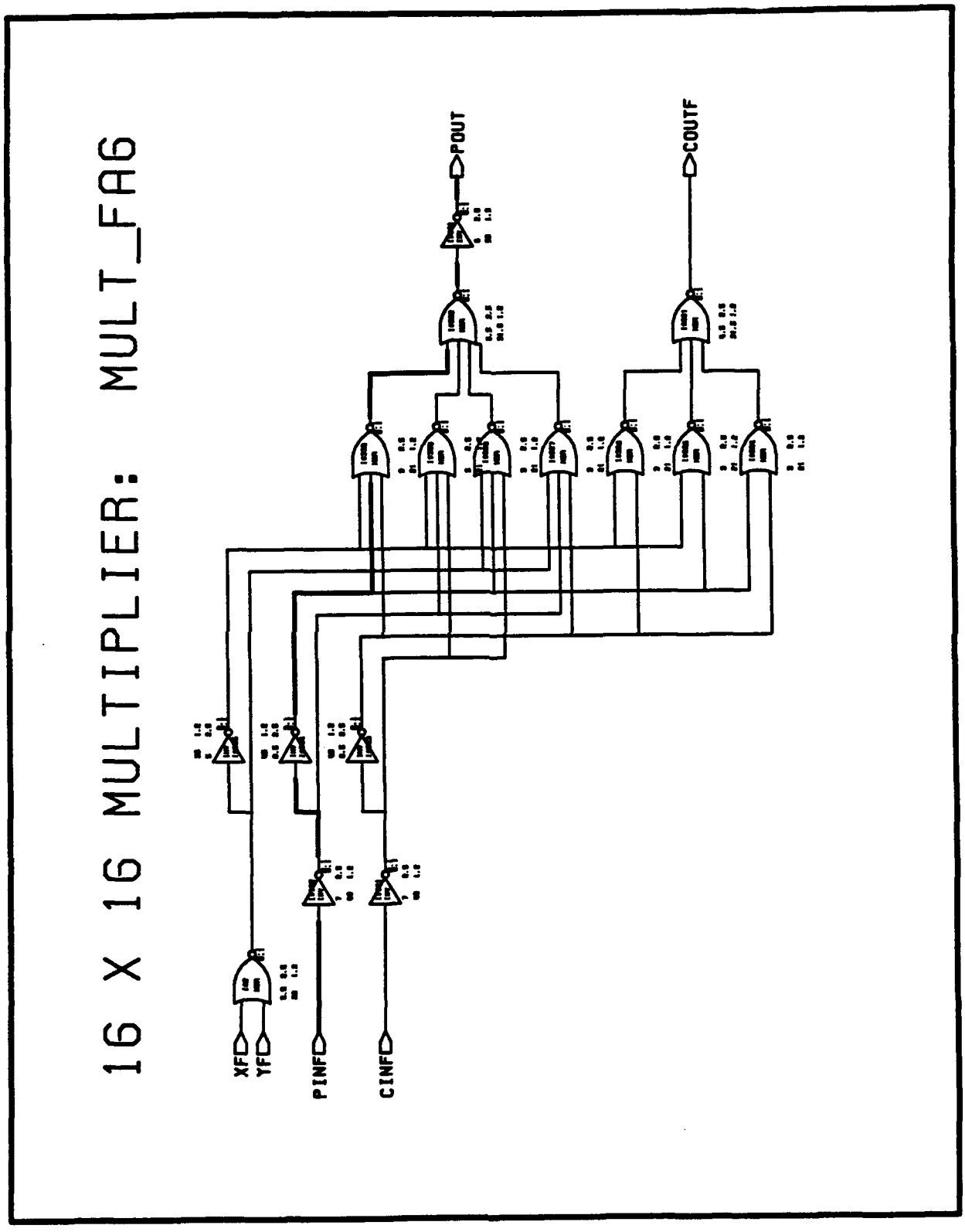
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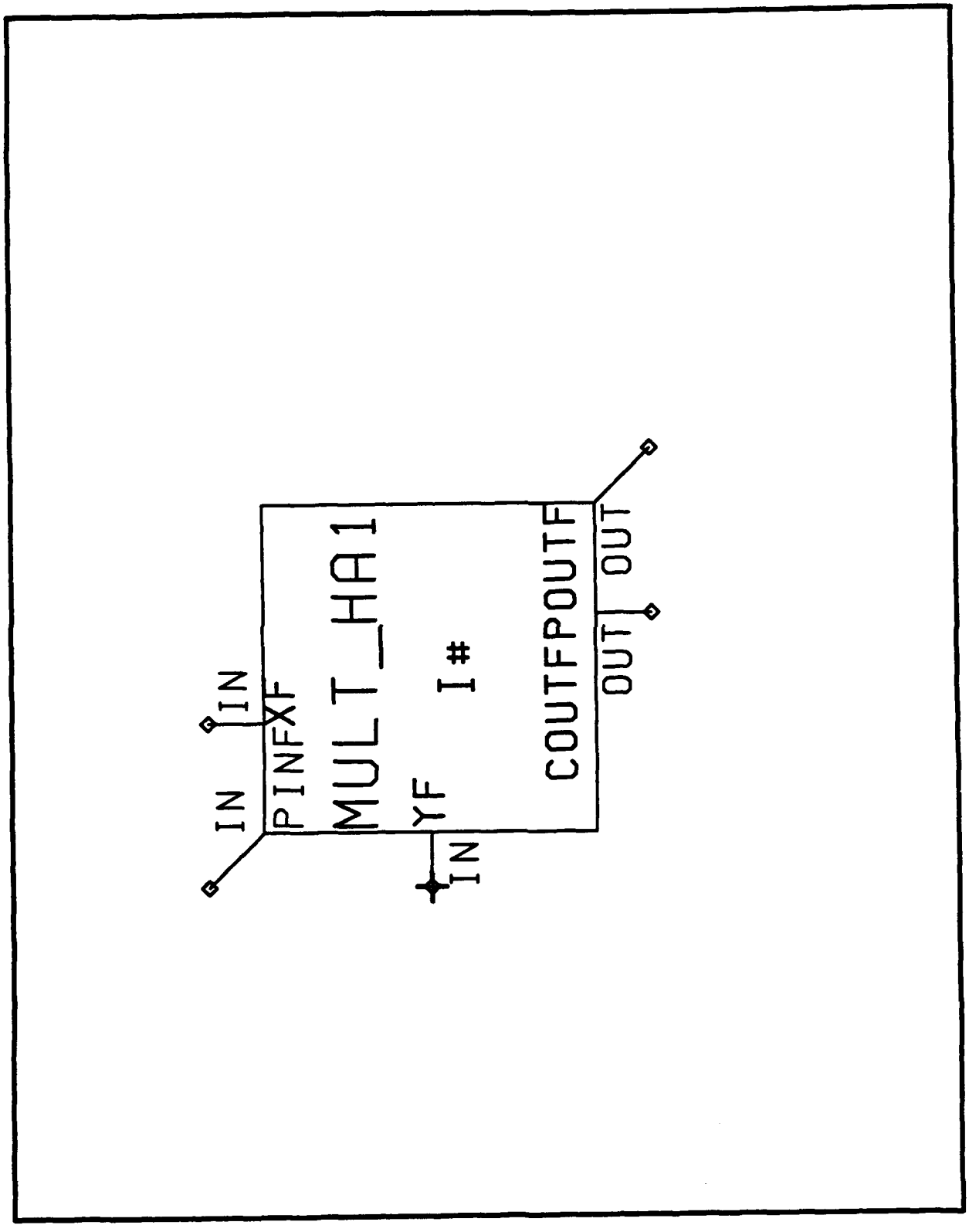
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YF
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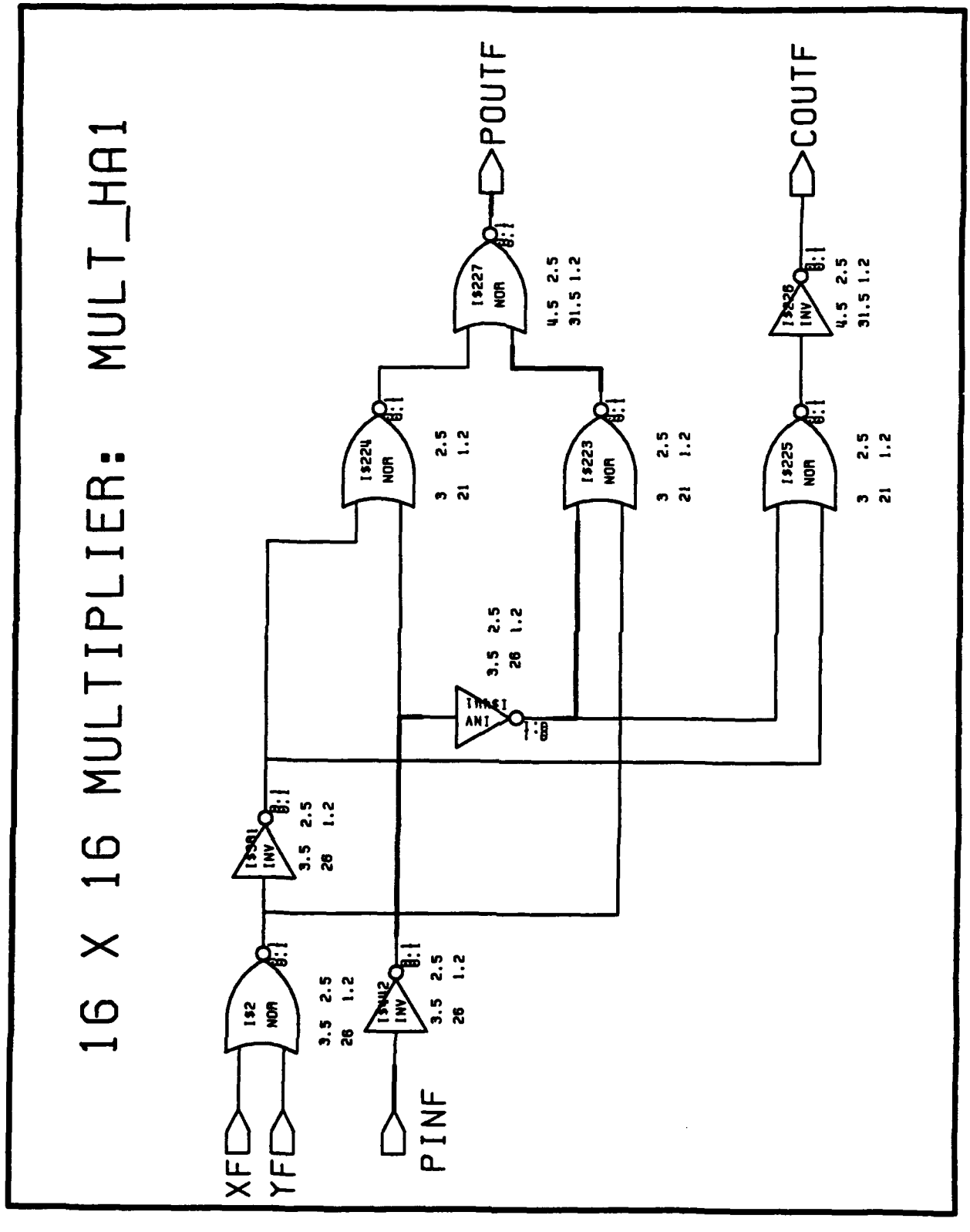
OUT
OUT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POUTF
COUTF
XF
YF
PINF
I$227 NOR
I$224 NOR
I$223 NOR
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I$2 NOR
I$36 INV
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I$112 INV
I$1 ANI
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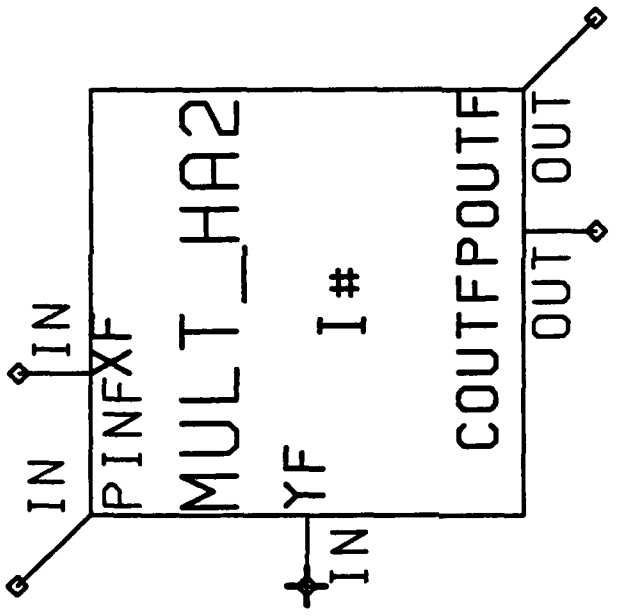
31.5 1.2
3 2.5
21 1.2
3.5 2.5
28 1.2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YF
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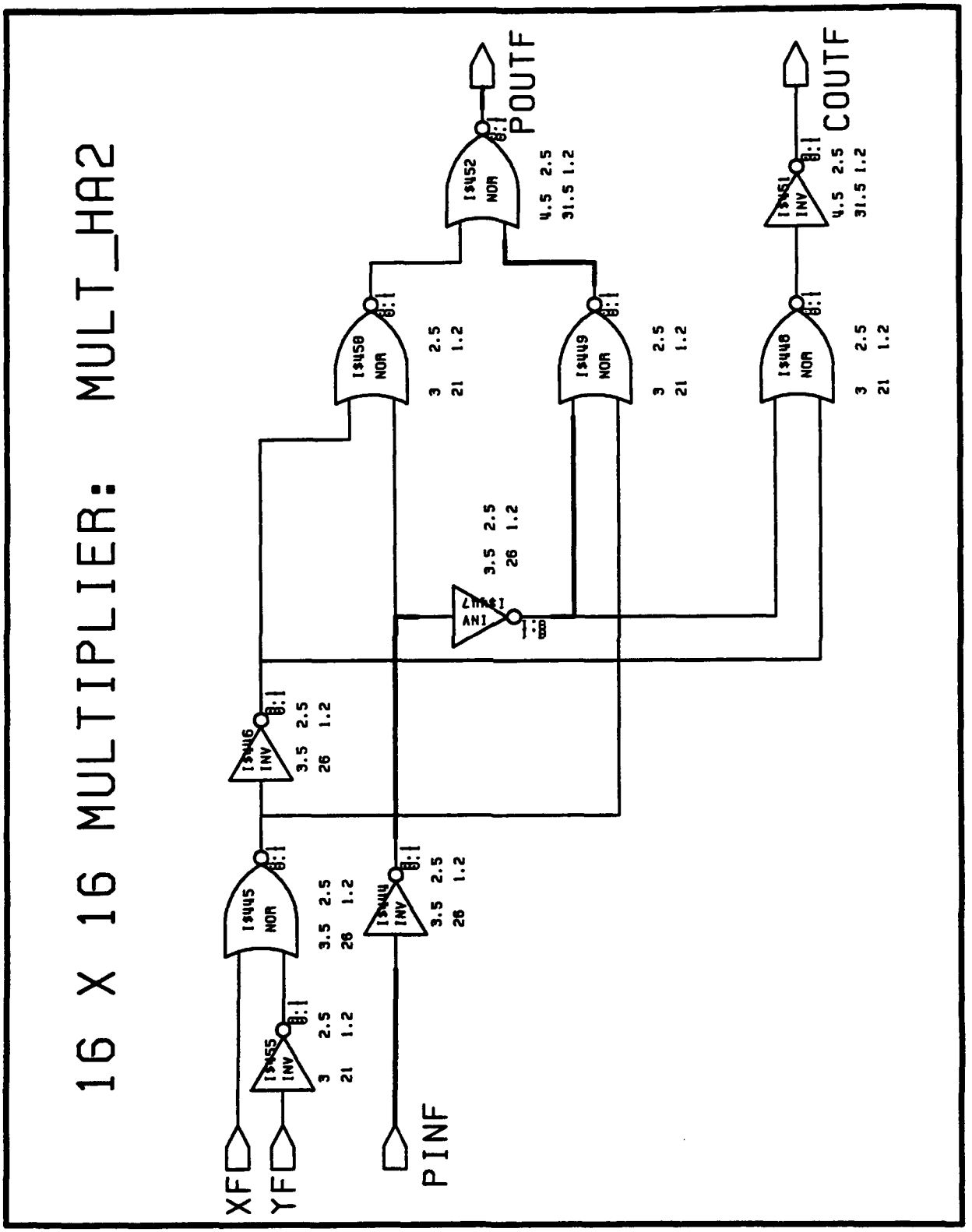
OUT
OUT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COUTF
PINF
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YF
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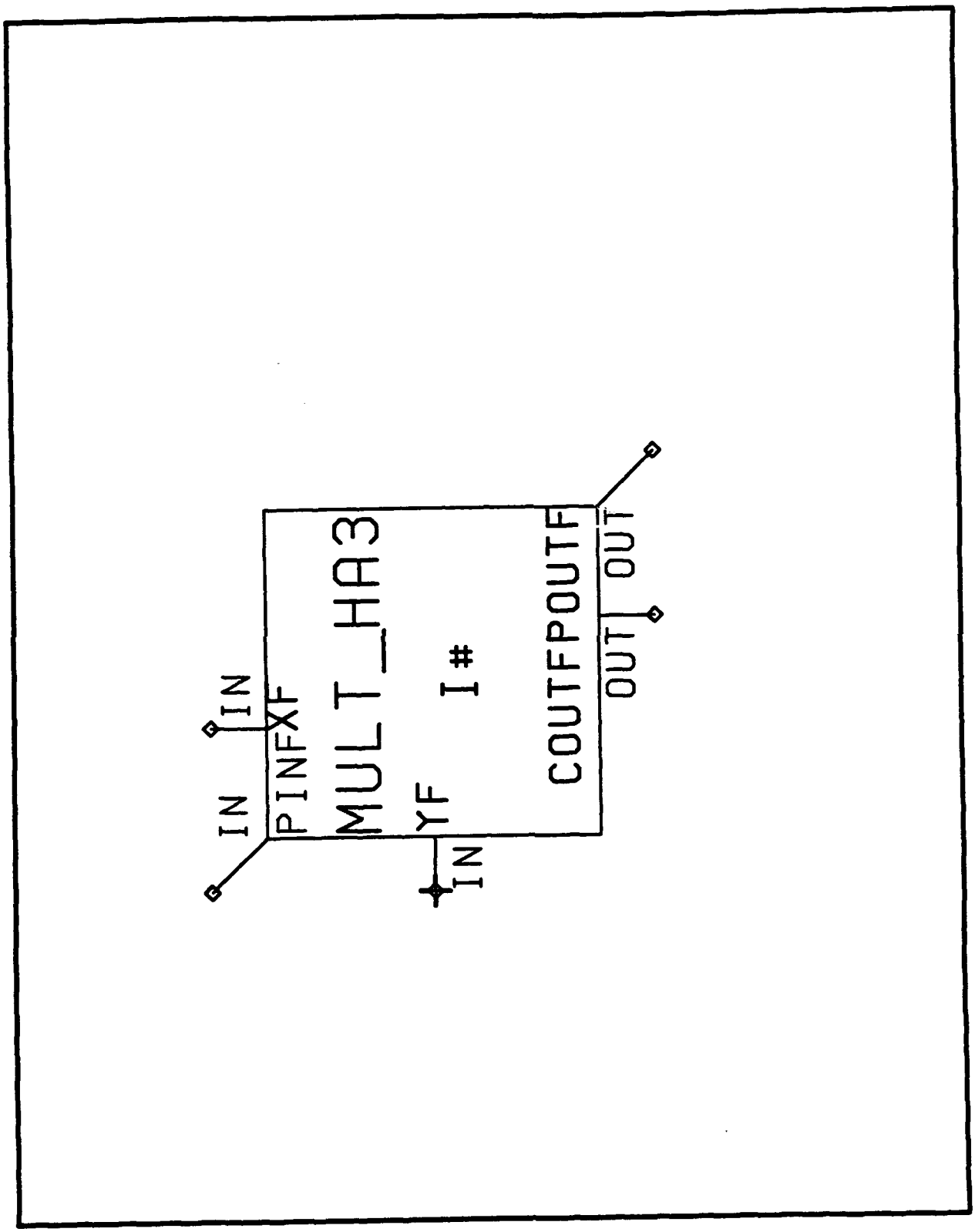
31.5 1.2
3 2.5
21 1.2
3.5 2.5
26 1.2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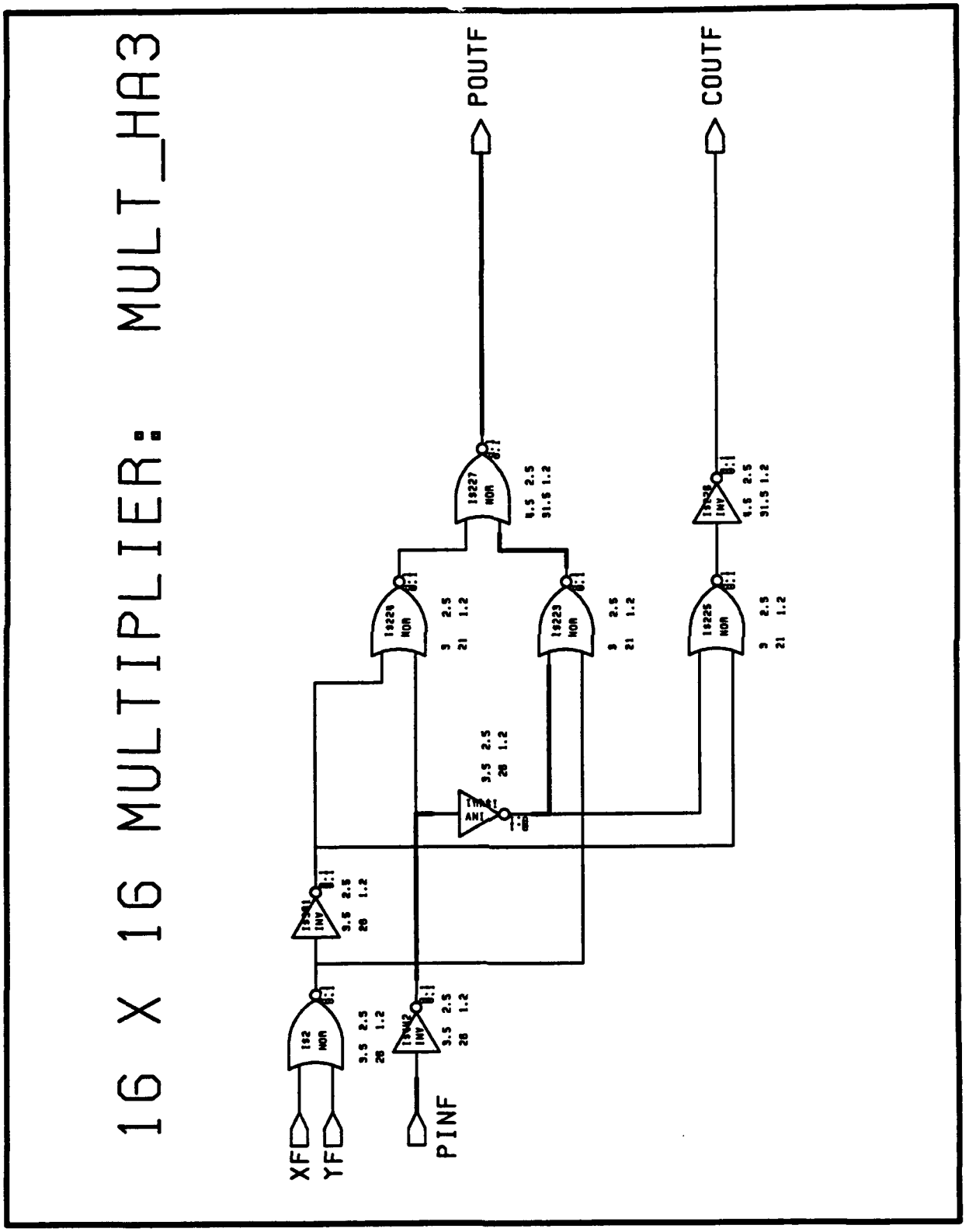
OUT
OUT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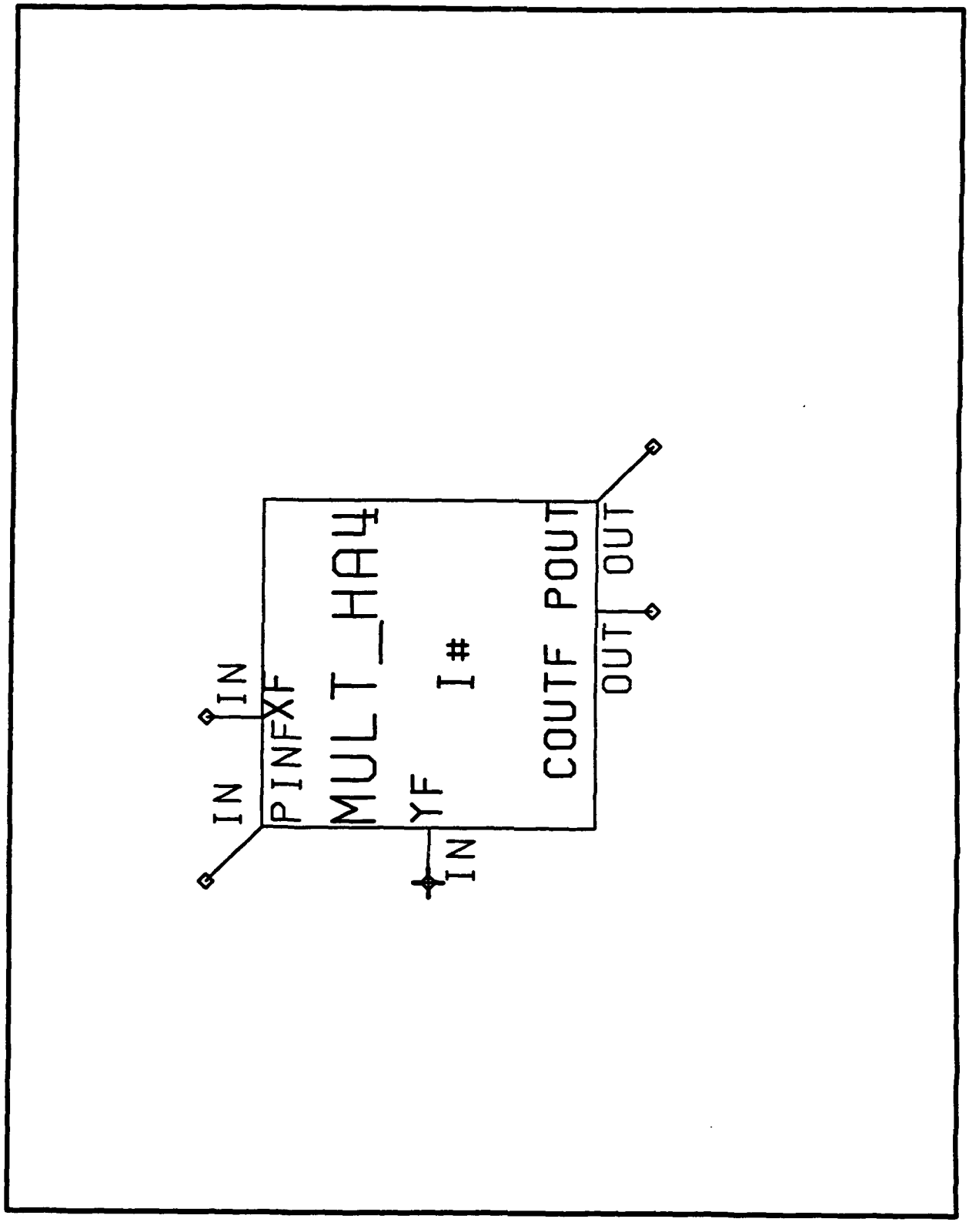
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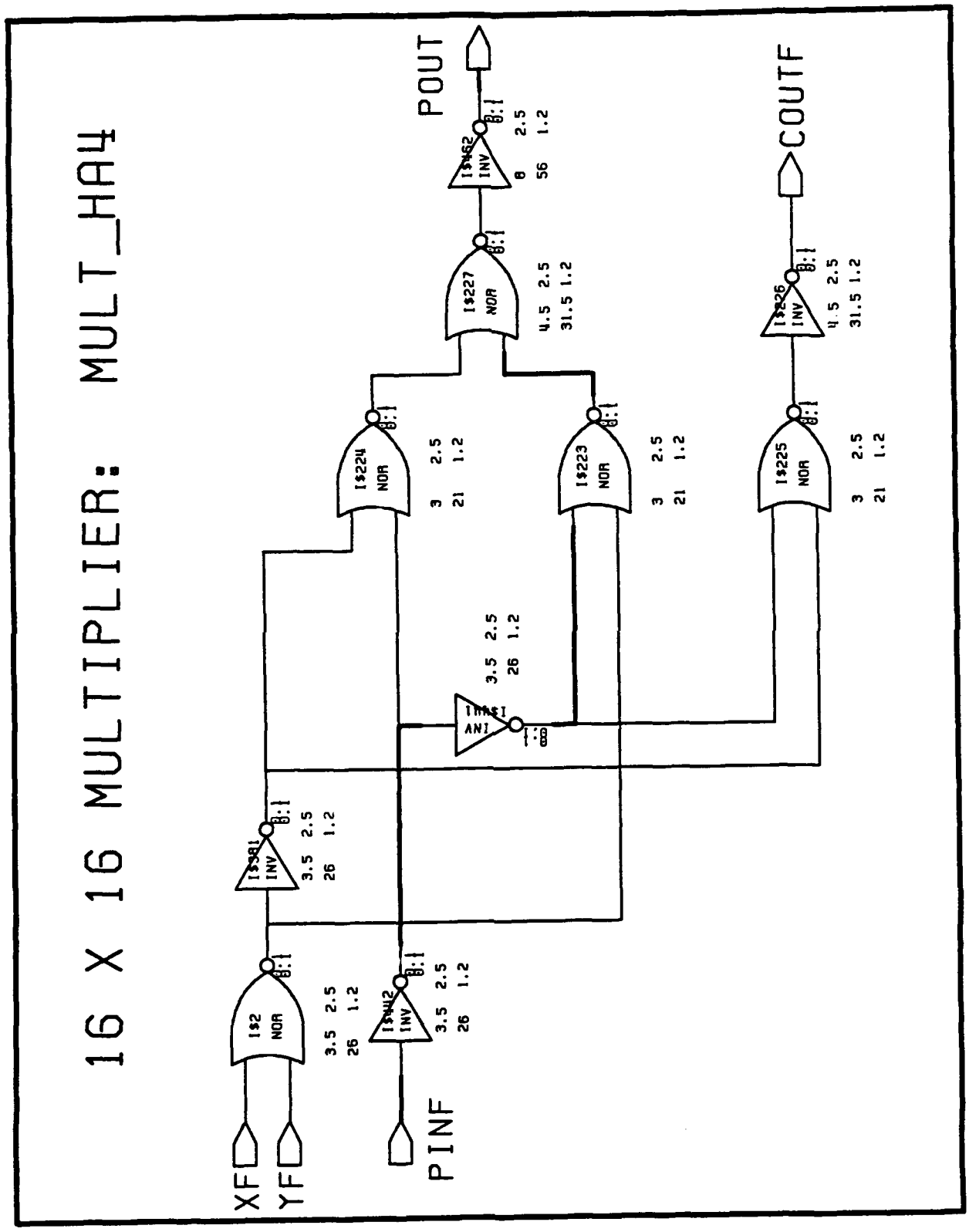
OUT
OUT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YF
PINF
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I$224 NOR
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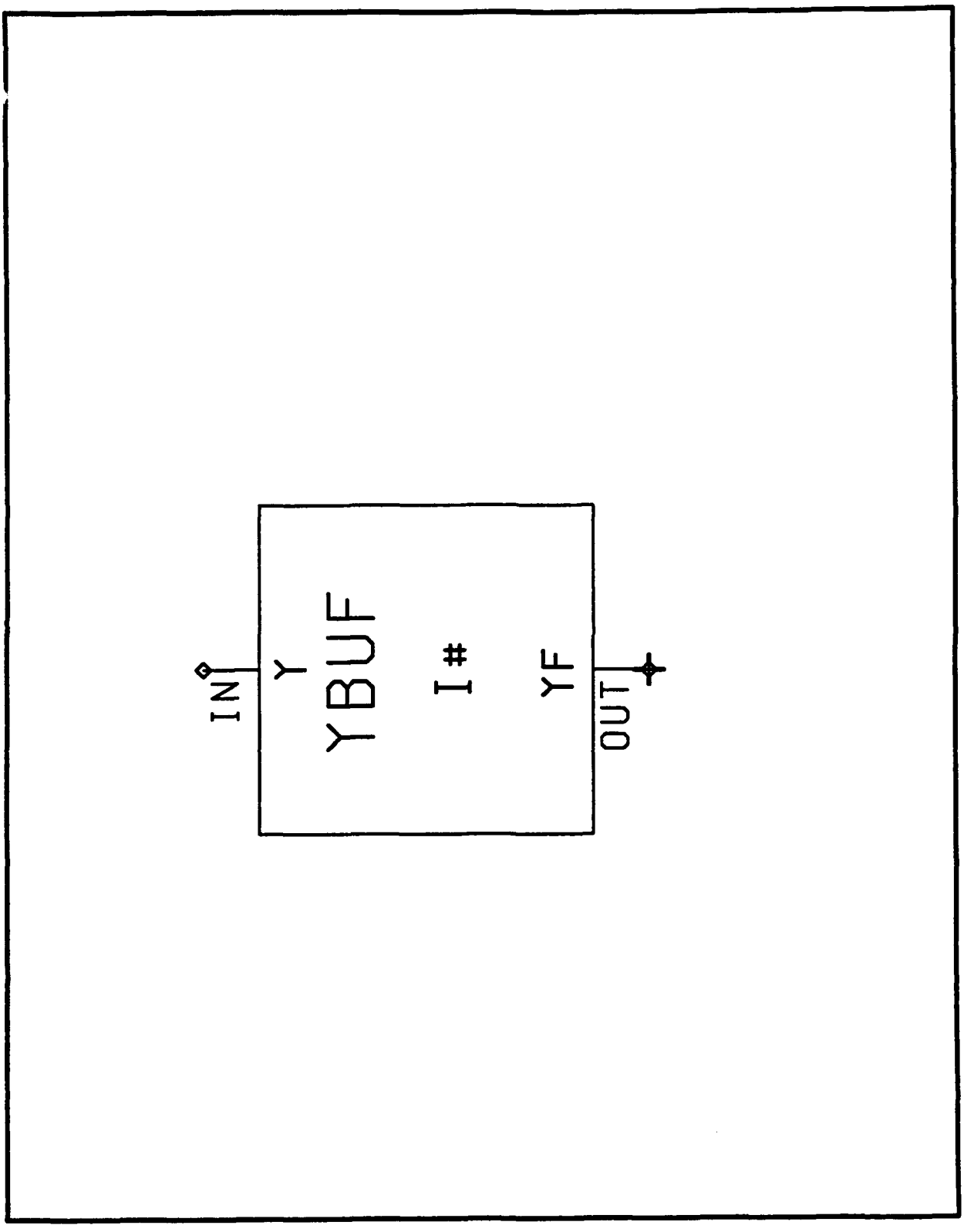
INV
ANI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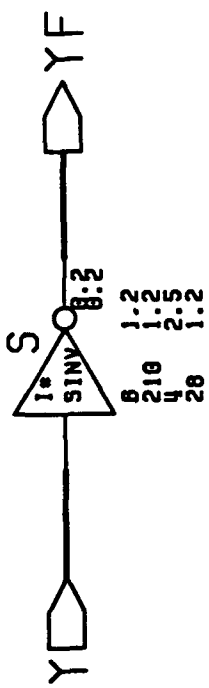
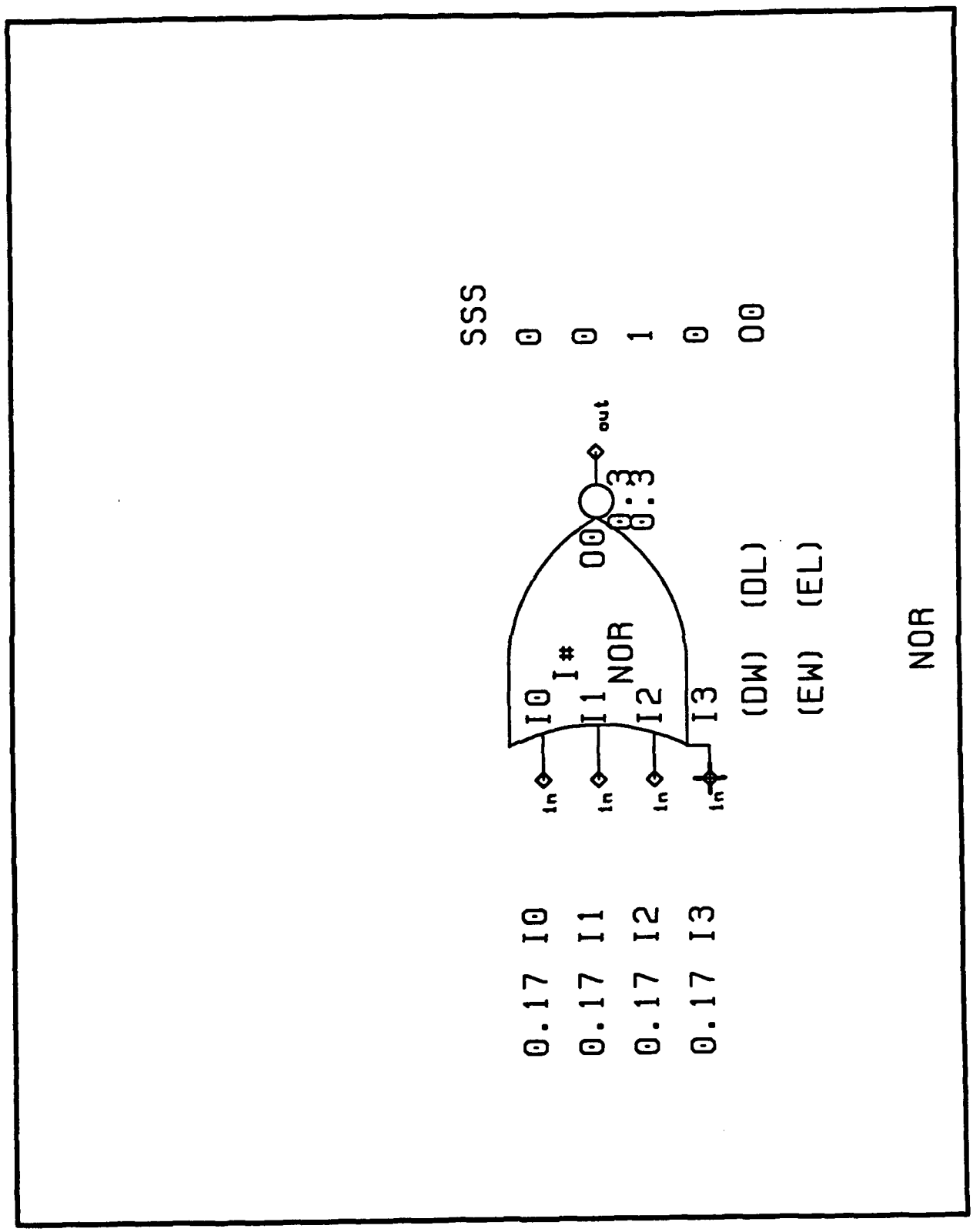
Y
YBUF
I#
YF
OUT

16 X 16 MULTIPLIER: YBUF




SSS
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out
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8.3
8.3
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I#
I1
NOR
I2
I3
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(EW) (EL)
NOR
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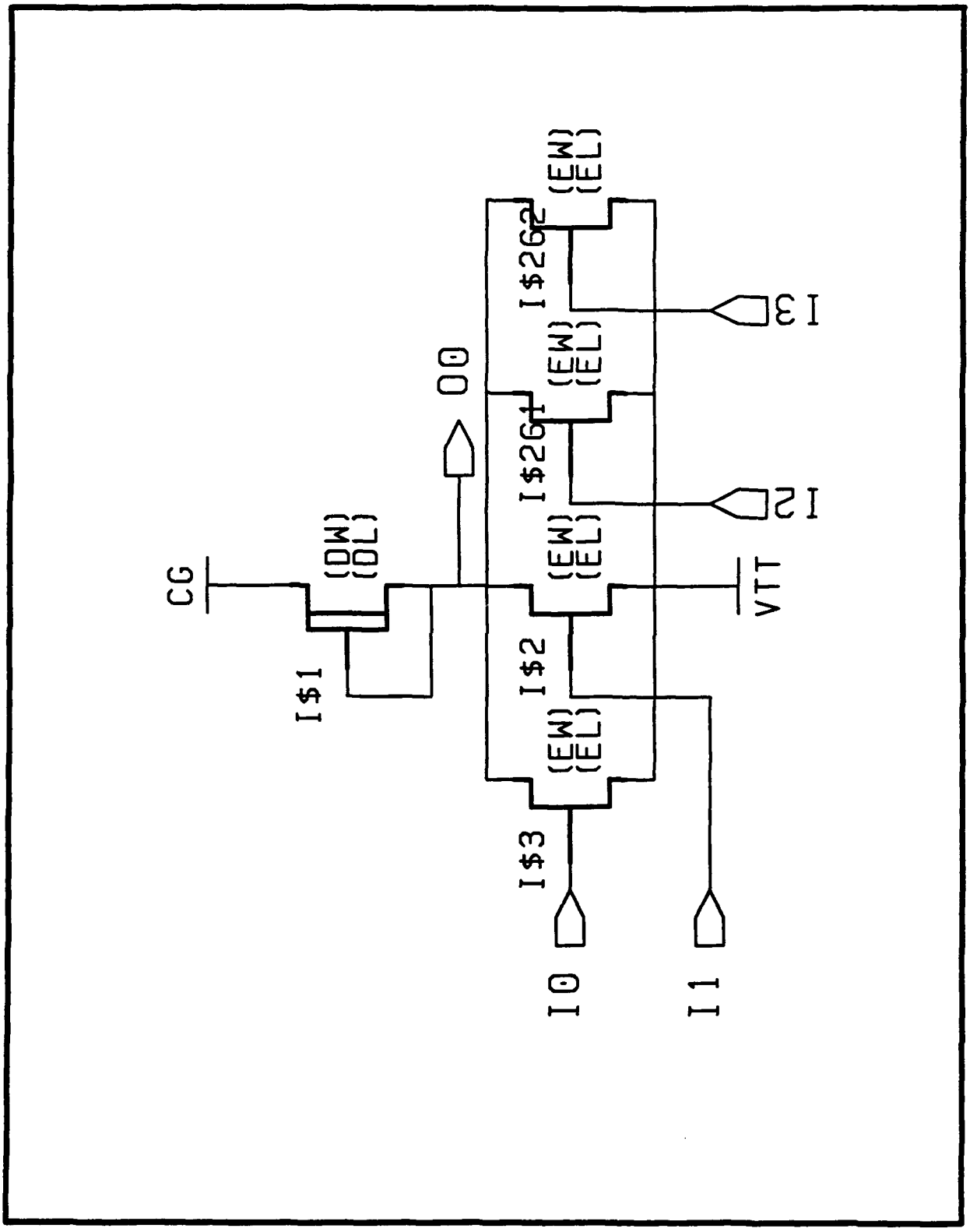
In
In
In
0.17 I0
0.17 I1
0.17 I2
0.17 I3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(EL)
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(EW)
(EL)
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(EW)
(EL)
VTT
I$1
I$2
(EW)
(EL)
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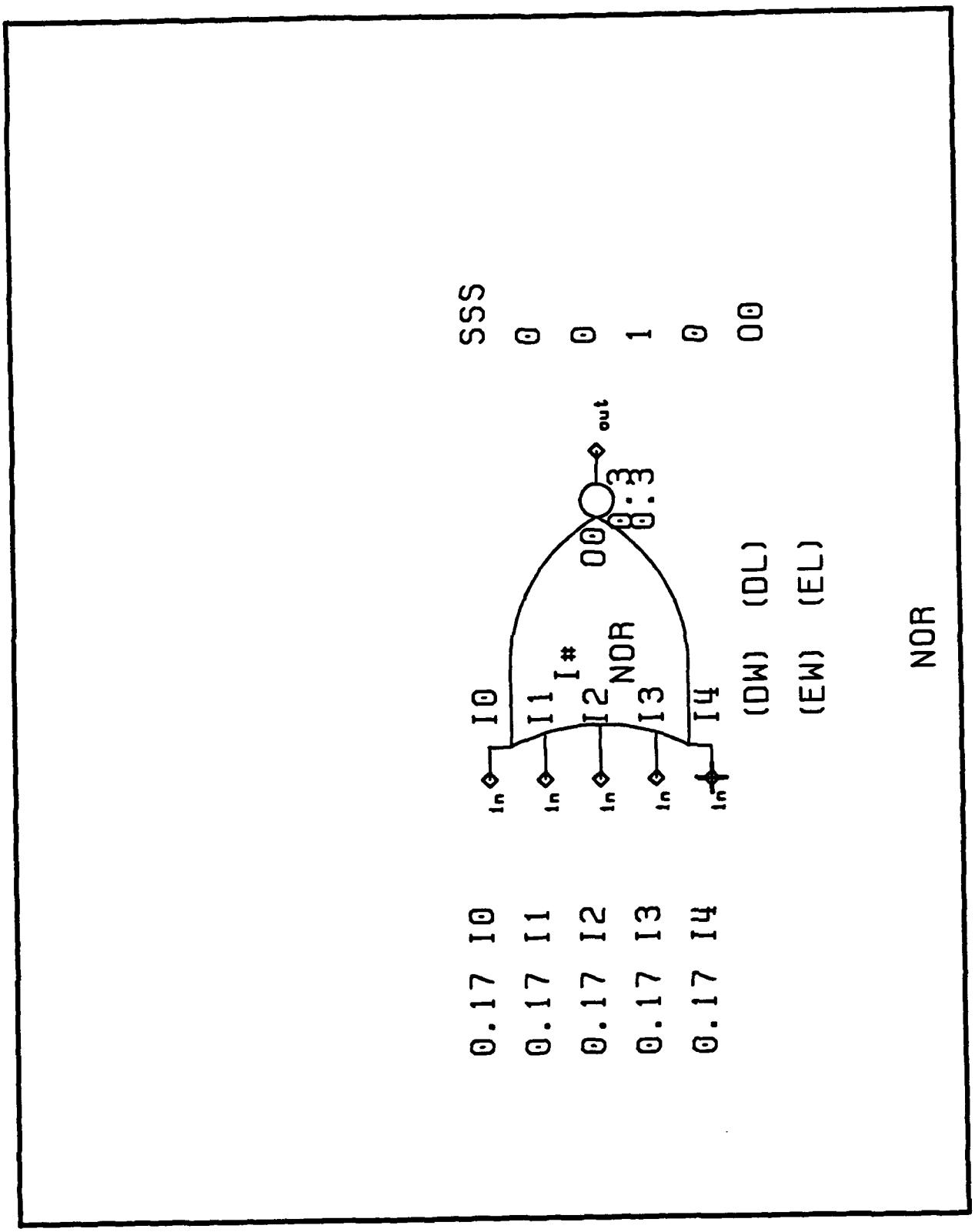
I0
I1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NOR
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I2
I3
I4
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In
In
In
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(DW) (DL)
(EW) (EL)
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0.17 I1
0.17 I2
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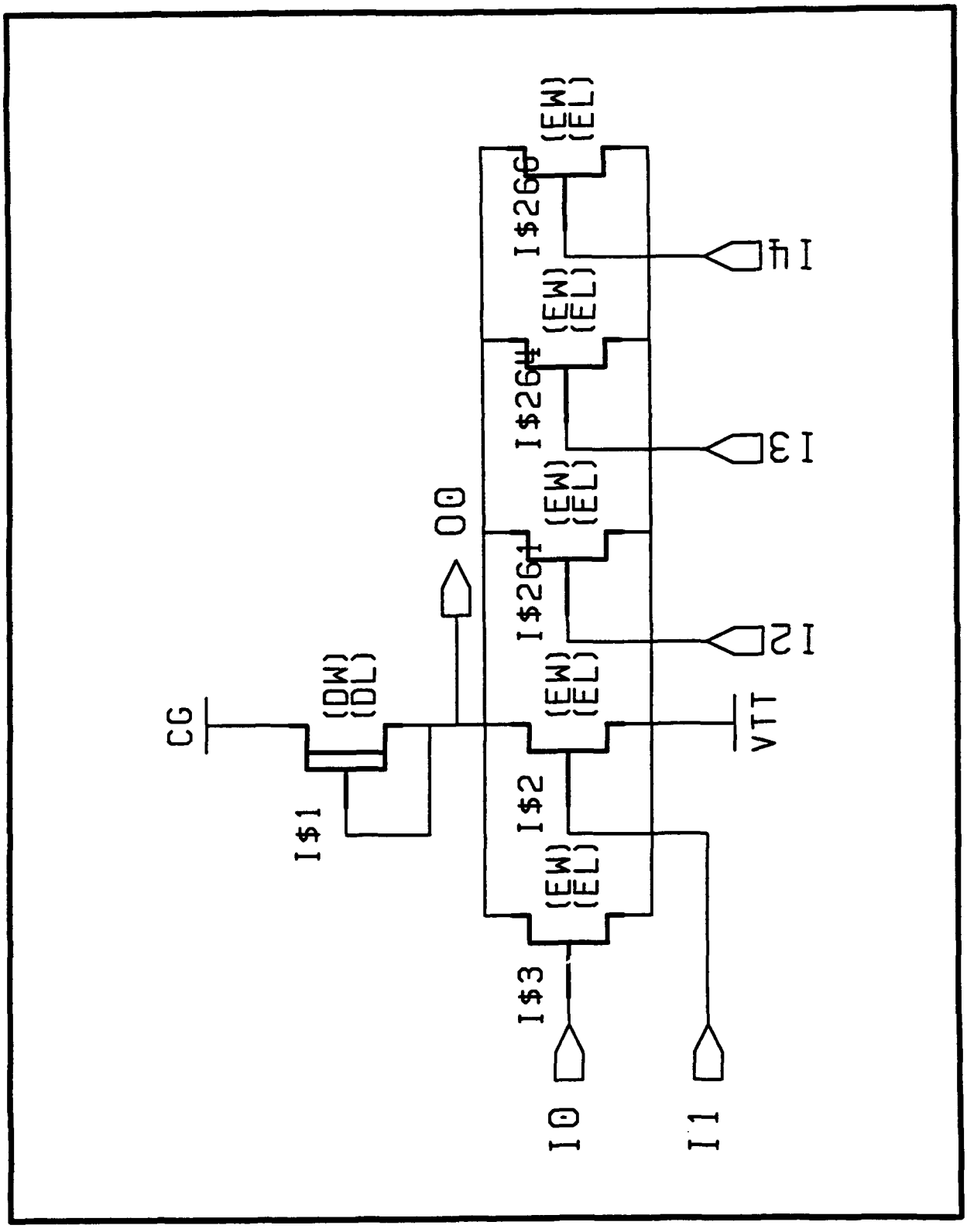
0.17 I4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(EL)
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(EW)
(EL)
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(EW)
(EL)
I2
I$2
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I0
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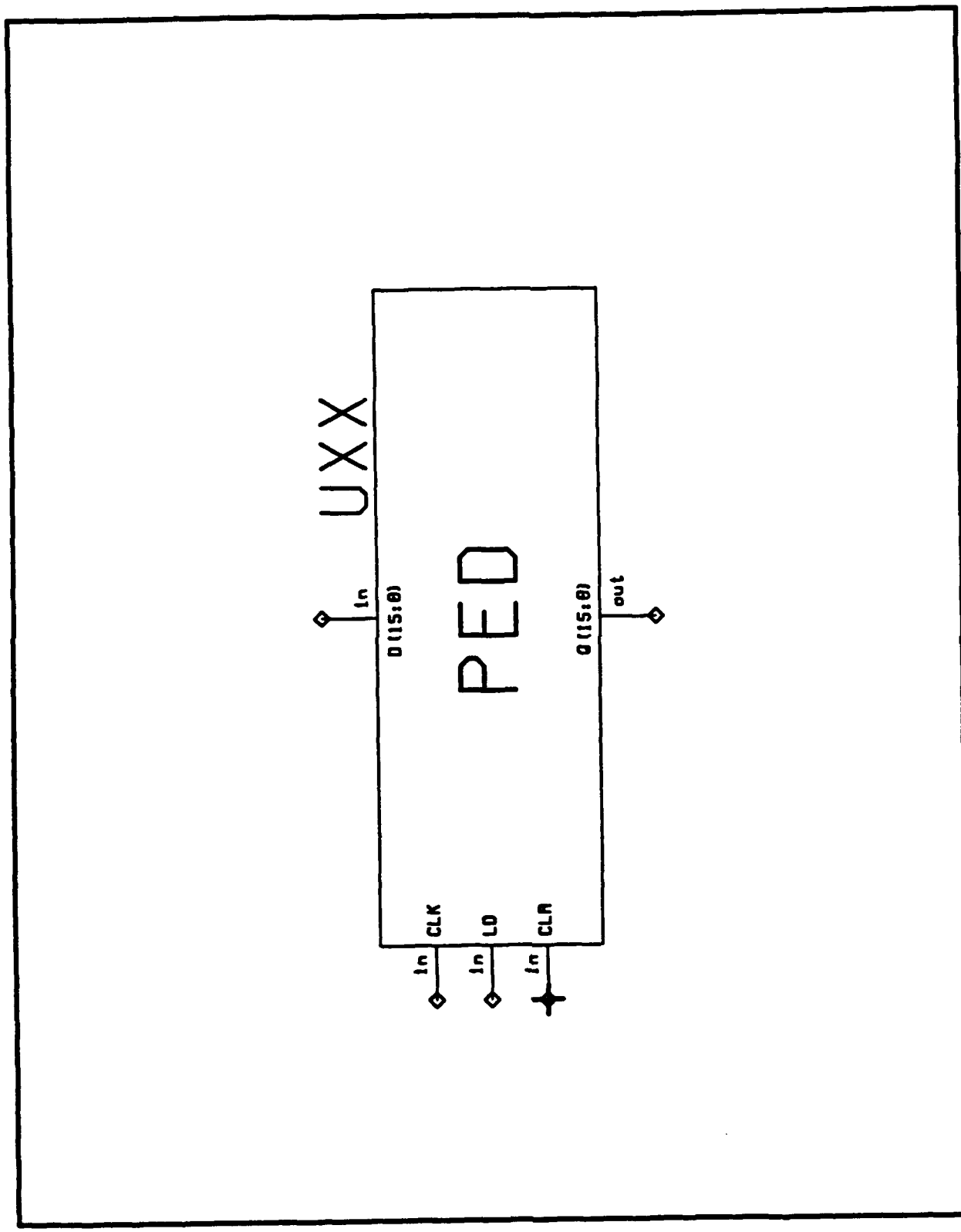
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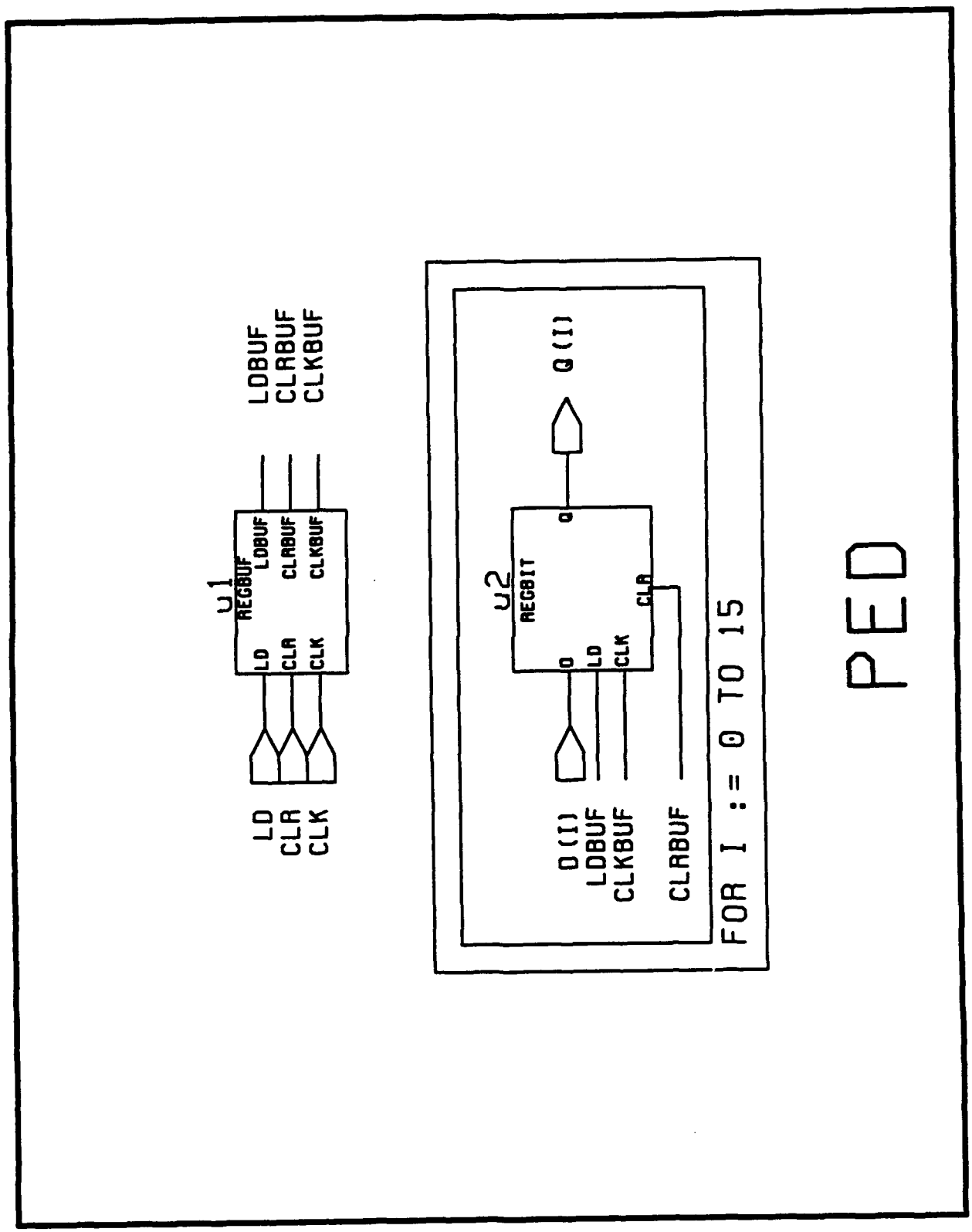
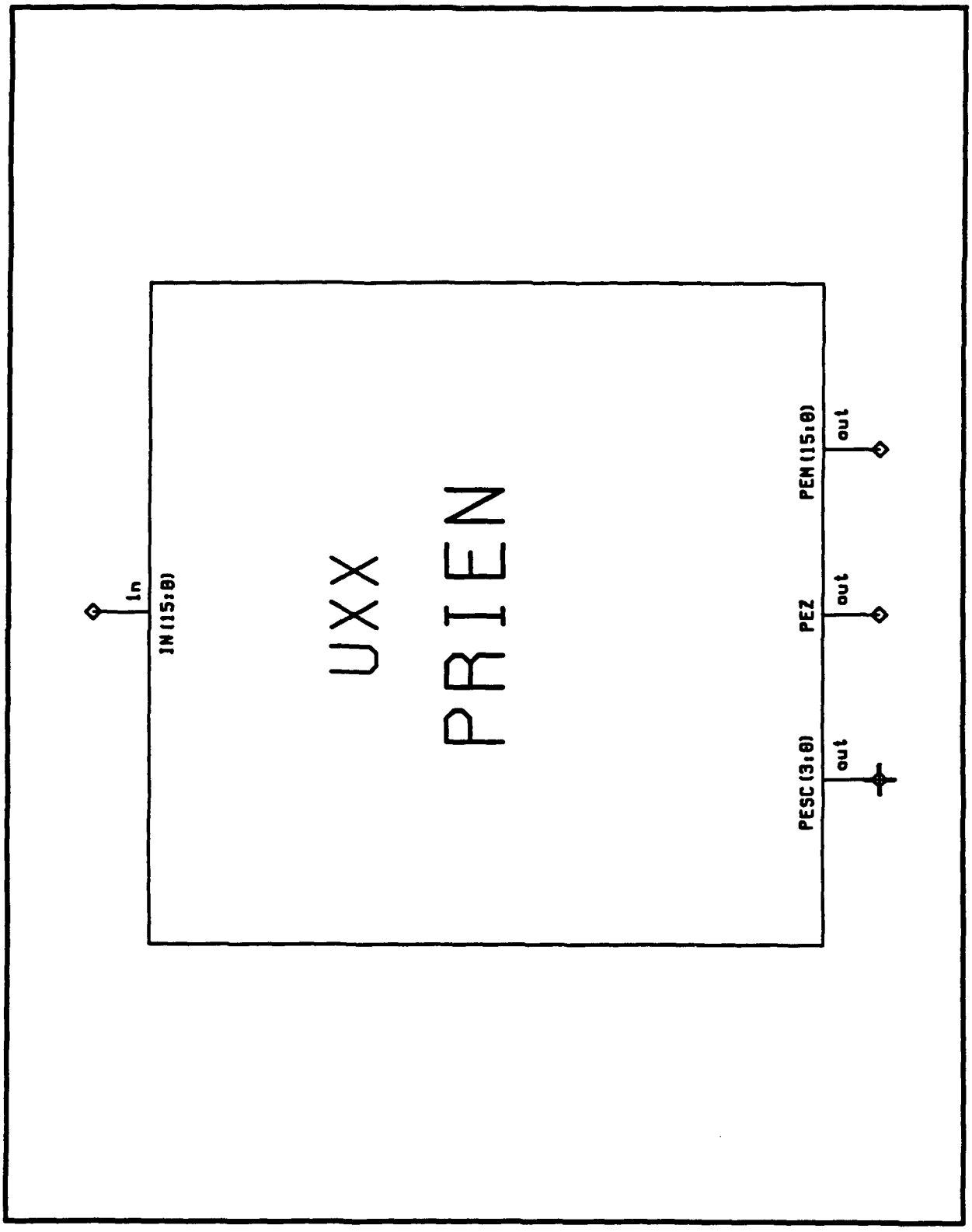
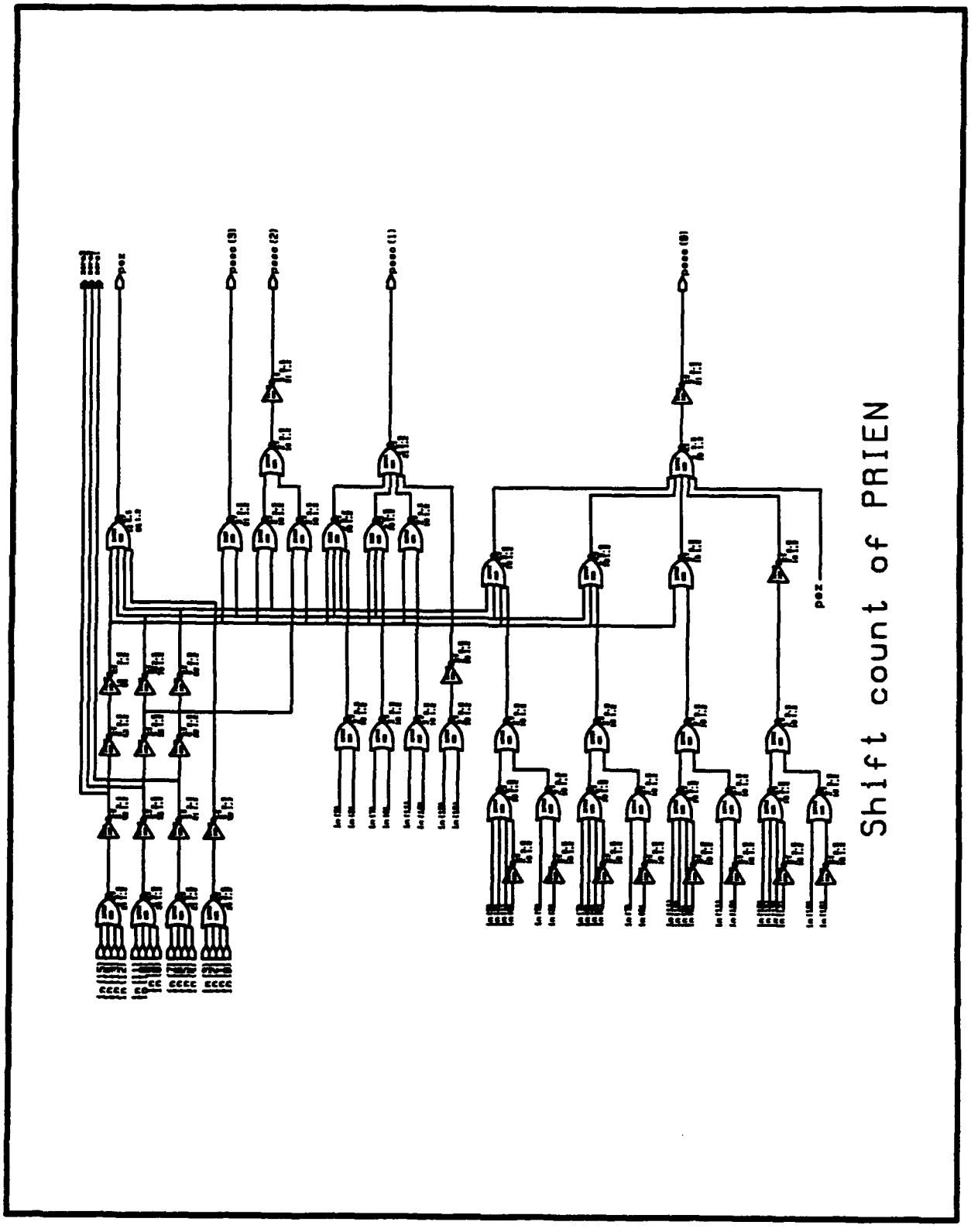
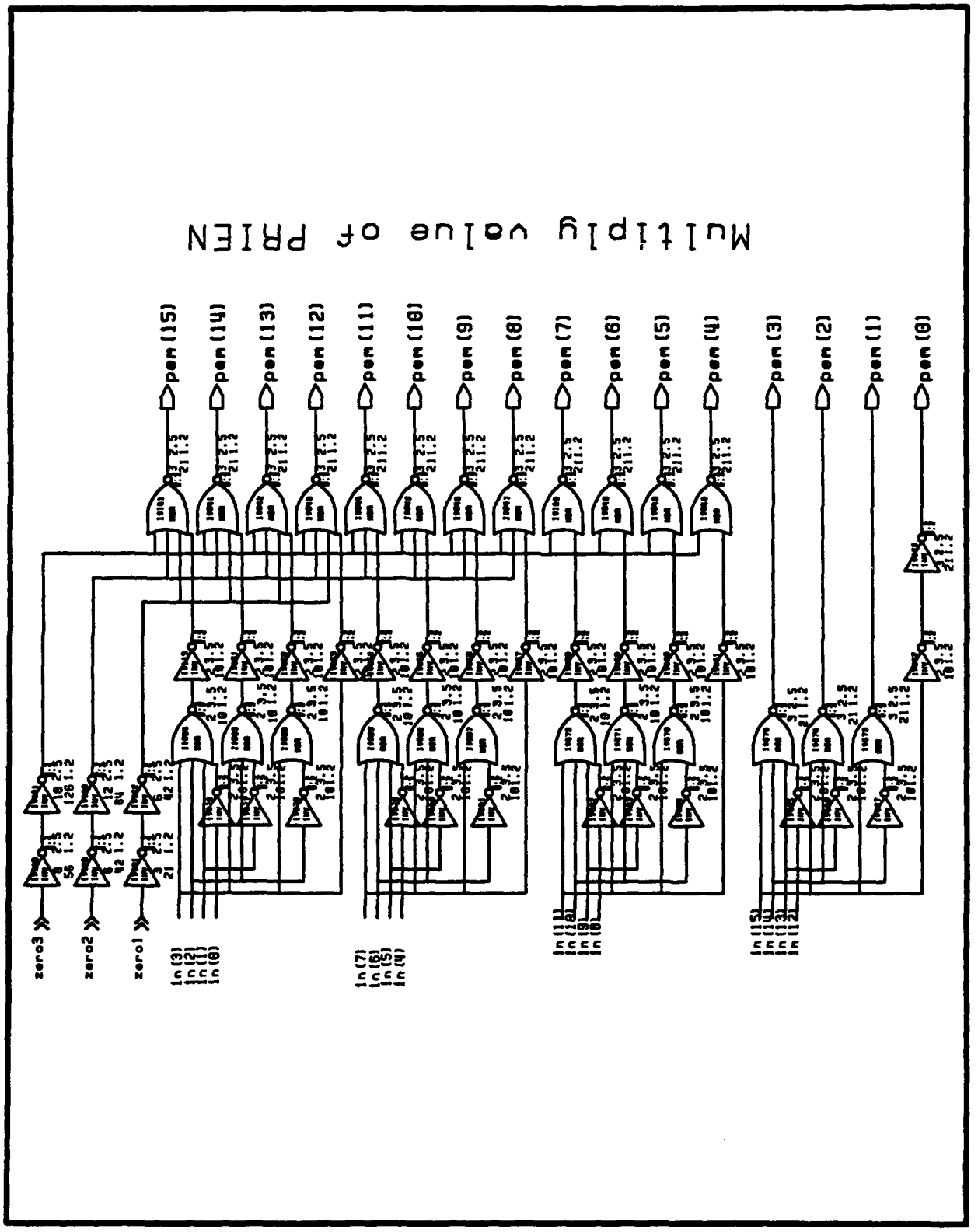
PED
In
D(15:0)
Q(15:0)
out
CLK
LD
CLR
In
In
In


PED
FOR I := 0 TO 15
u1
REGBUF
LDBUF
CLRBUF
CLKBUF
LD
CLR
CLK
u2
REGBIT
Q(I)
D(I)
LDBUF
CLKBUF
CLRBUF


UXX
PRIEN
In
IN(15:0)
PEM(15:0)
out
PEZ
out
PESC(3:0)
out


Shift count of PRIEN

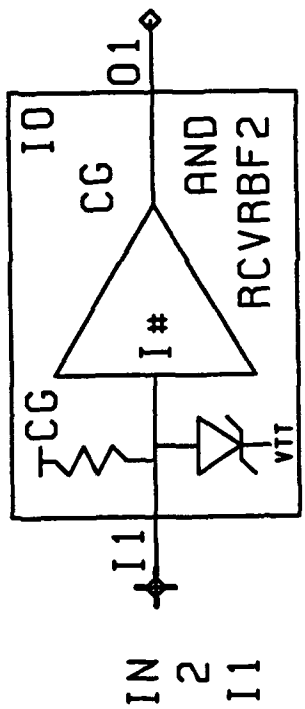

Multiply value of PRIEN
pen(15)
pen(14)
pen(13)
pen(12)
pen(11)
pen(10)
pen(9)
pen(8)
pen(7)
pen(6)
pen(5)
pen(4)
pen(3)
pen(2)
pen(1)
pen(0)
zero3
zero2
zero1

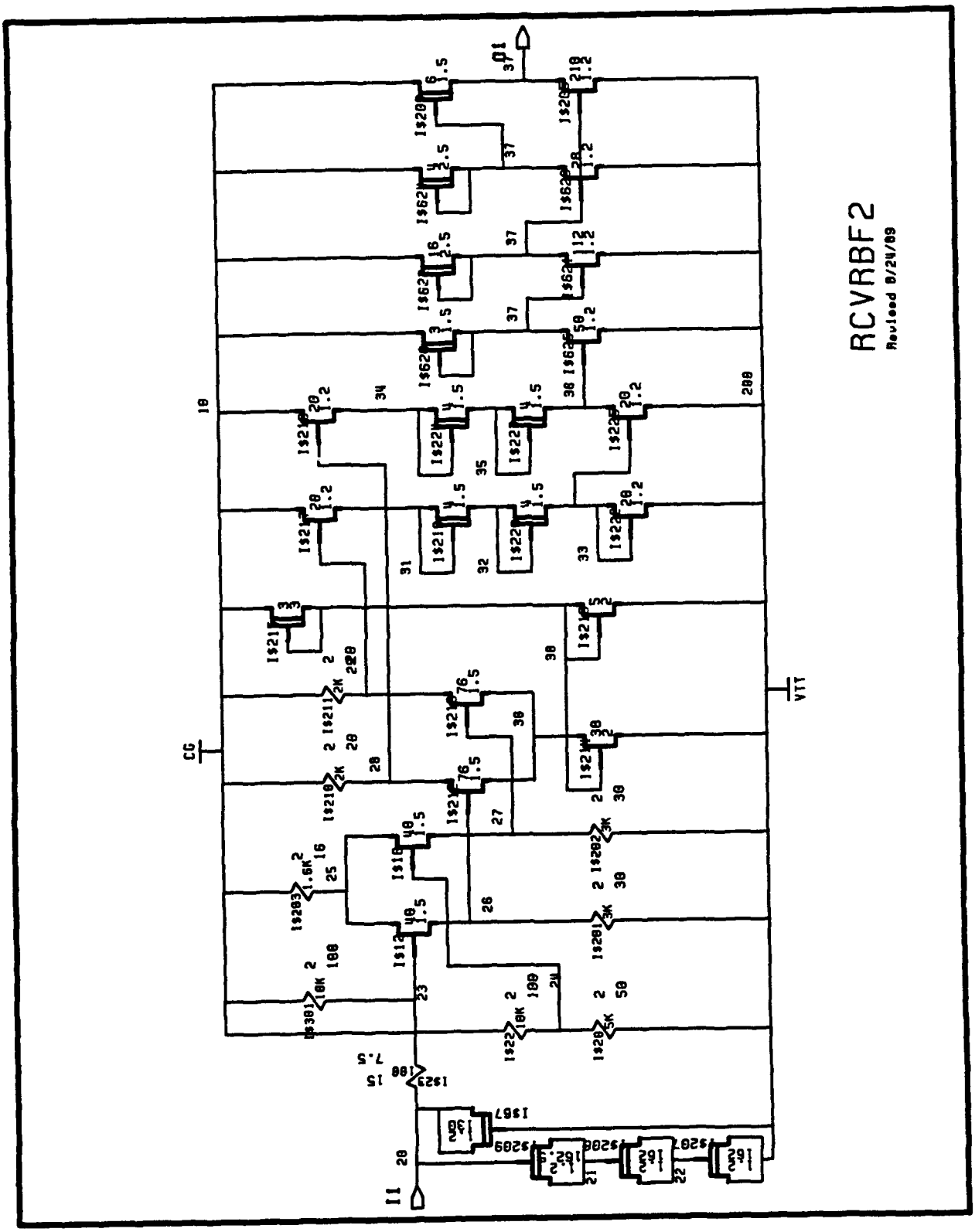
VITESSE GAAS CELL LIBRARY
Version 0.8

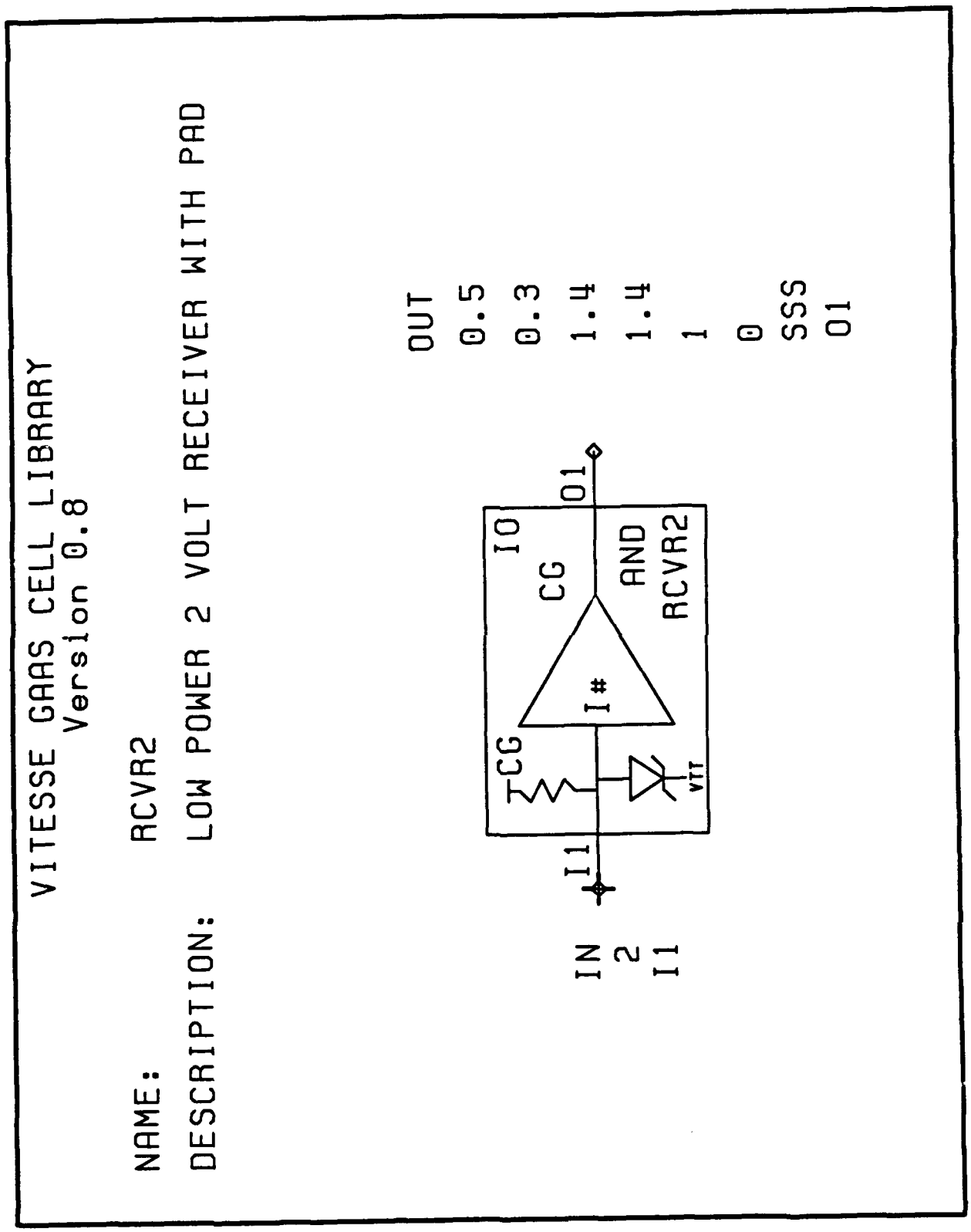
NAME: RCVRBF2

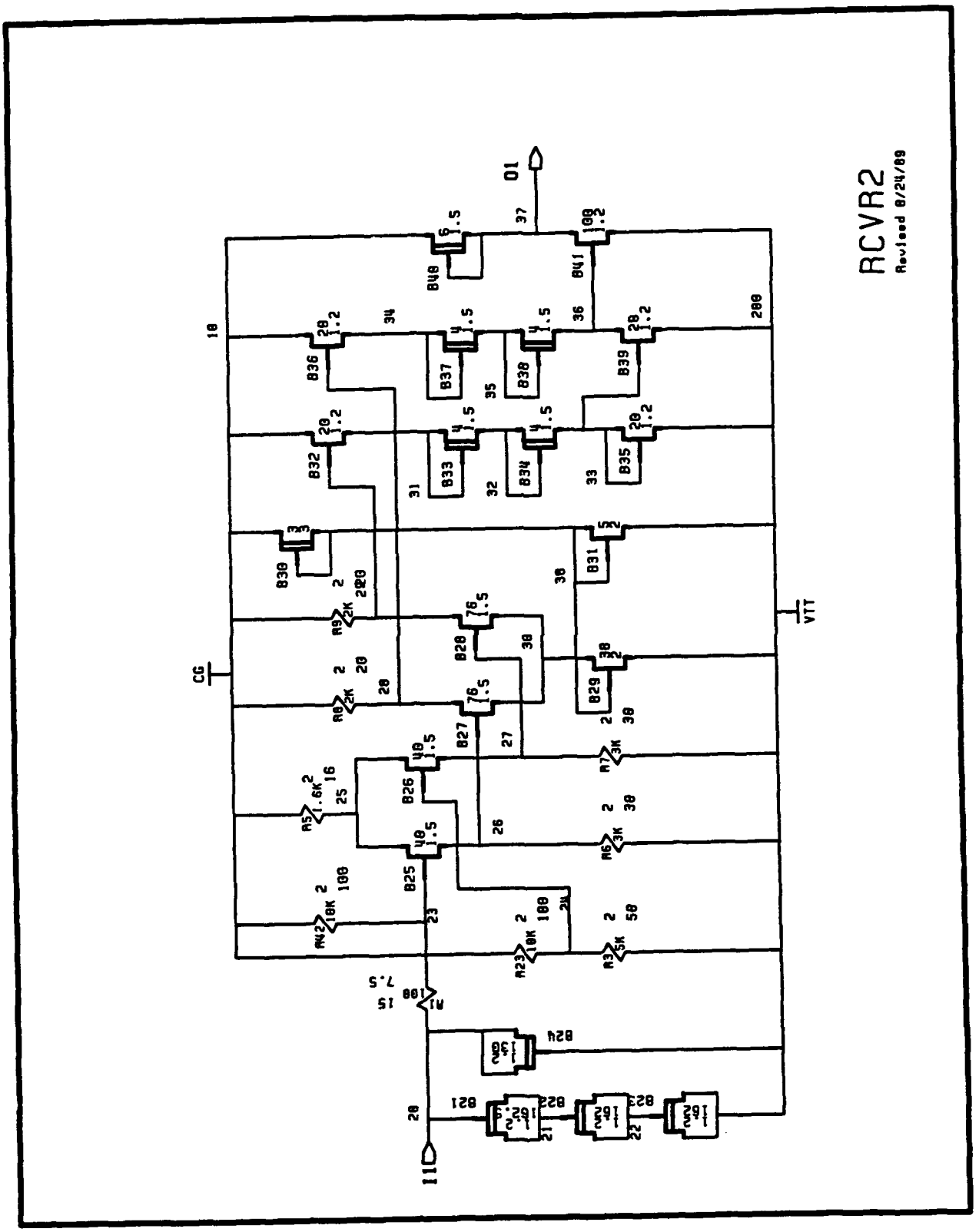
DESCRIPTION: HIGH POWER 2 VOLT RECEIVER

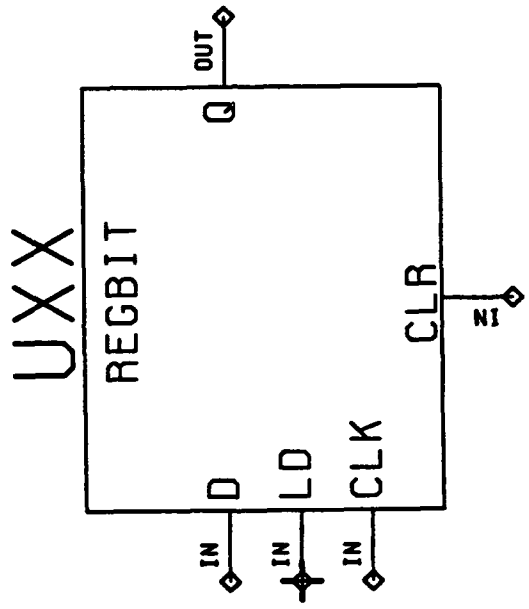
OUT
0.5
0.3
1.4
1.4
1
0
SSS
01

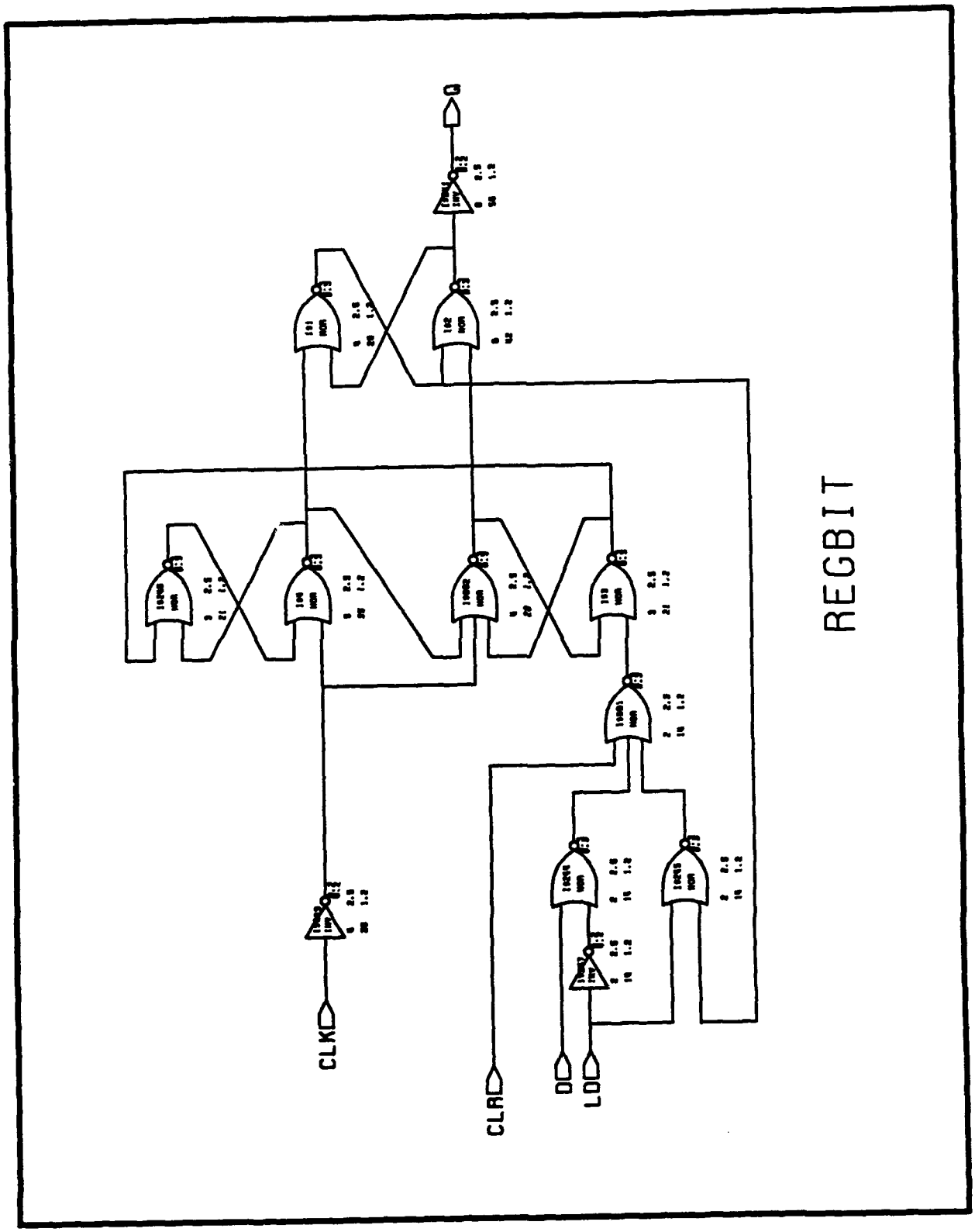


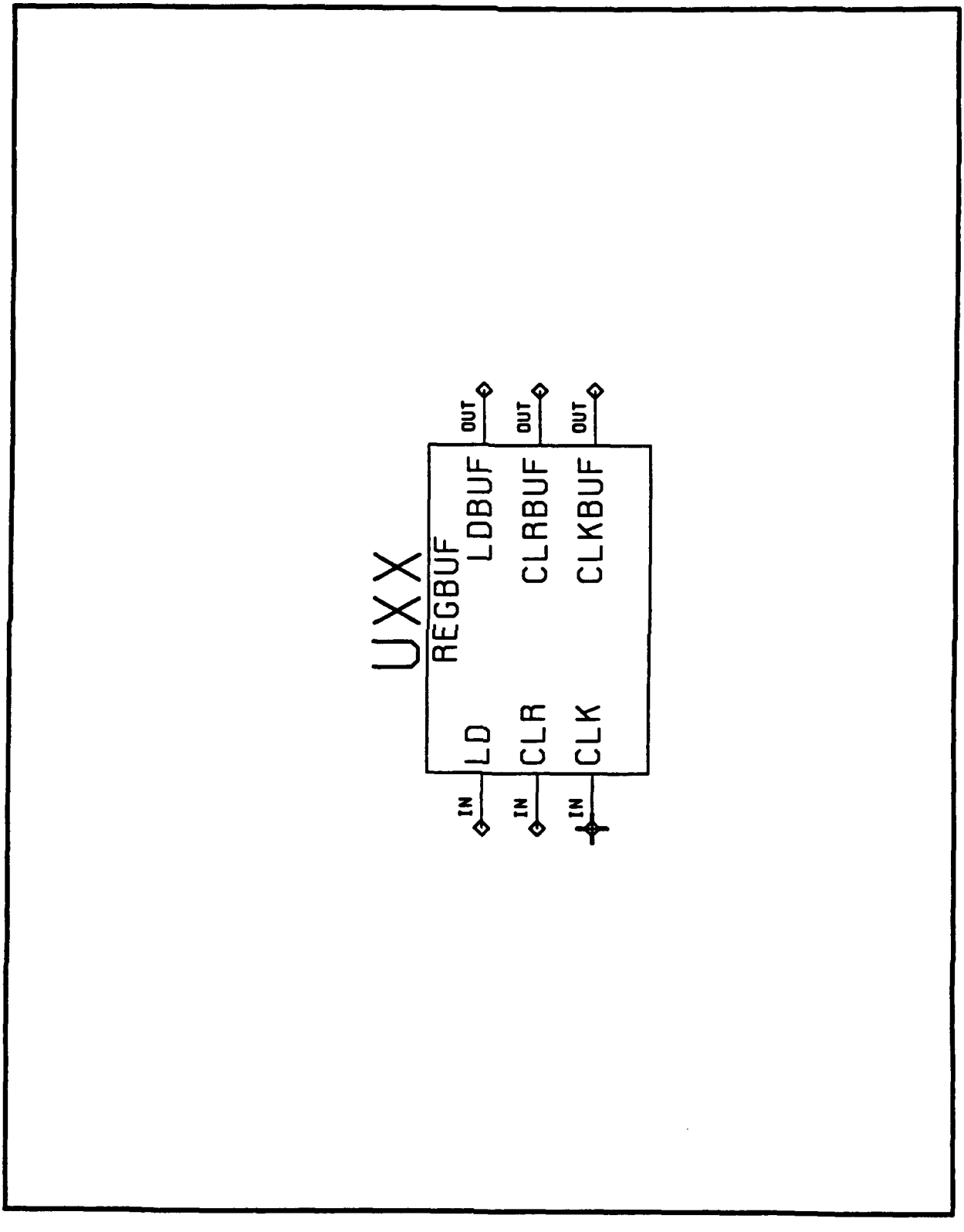

RCVRBF2
Revised 8/28/89
CG
VTT
I1
I0

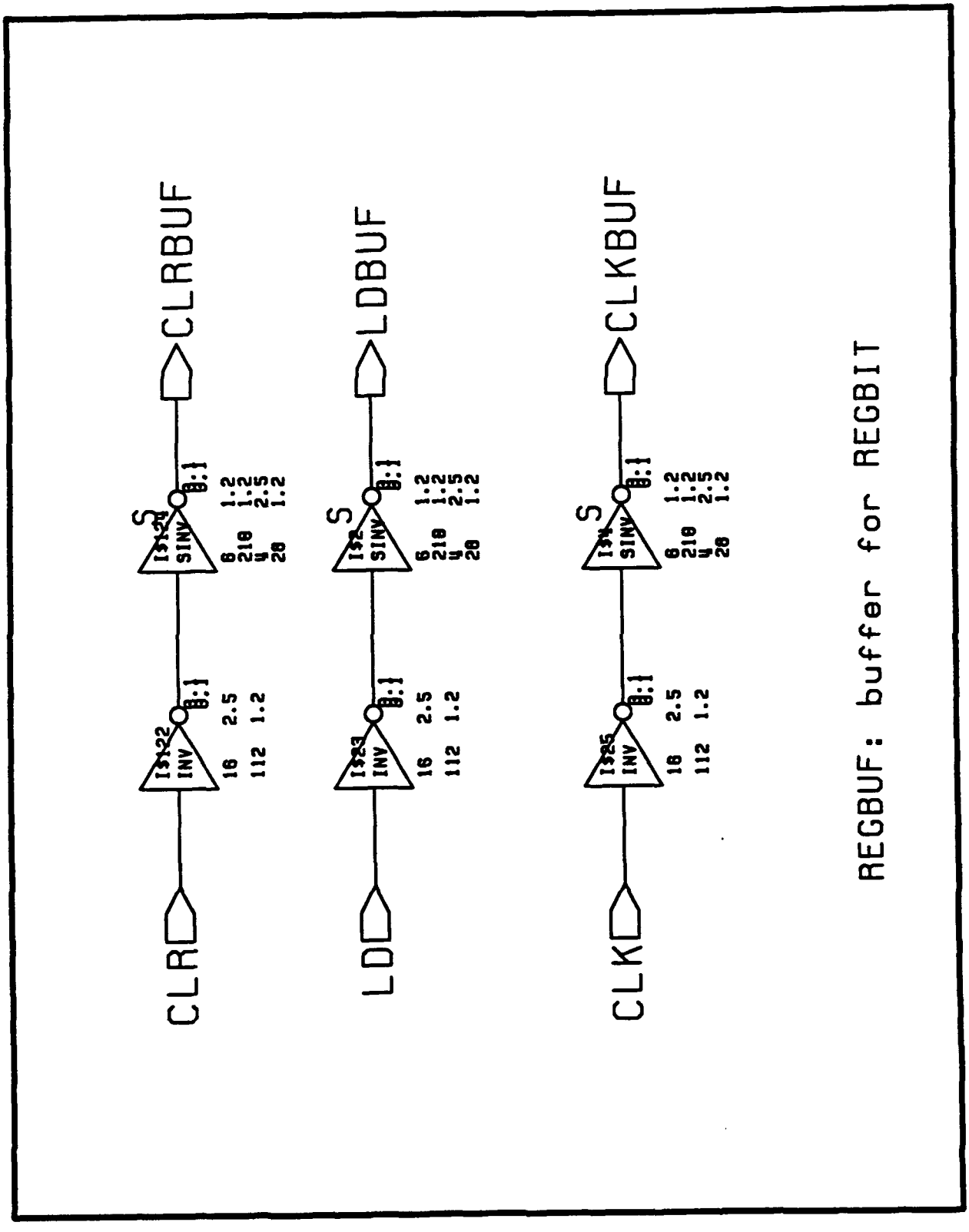

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: RCVR2
DESCRIPTION: LOW POWER 2 VOLT RECEIVER WITH PAD
OUT
0.5
0.3
1.4
1.4
1
0
SSS
01
IN
2
I1
I1
CG
I#
IO
CG
O1
AND
RCVR2
VTT

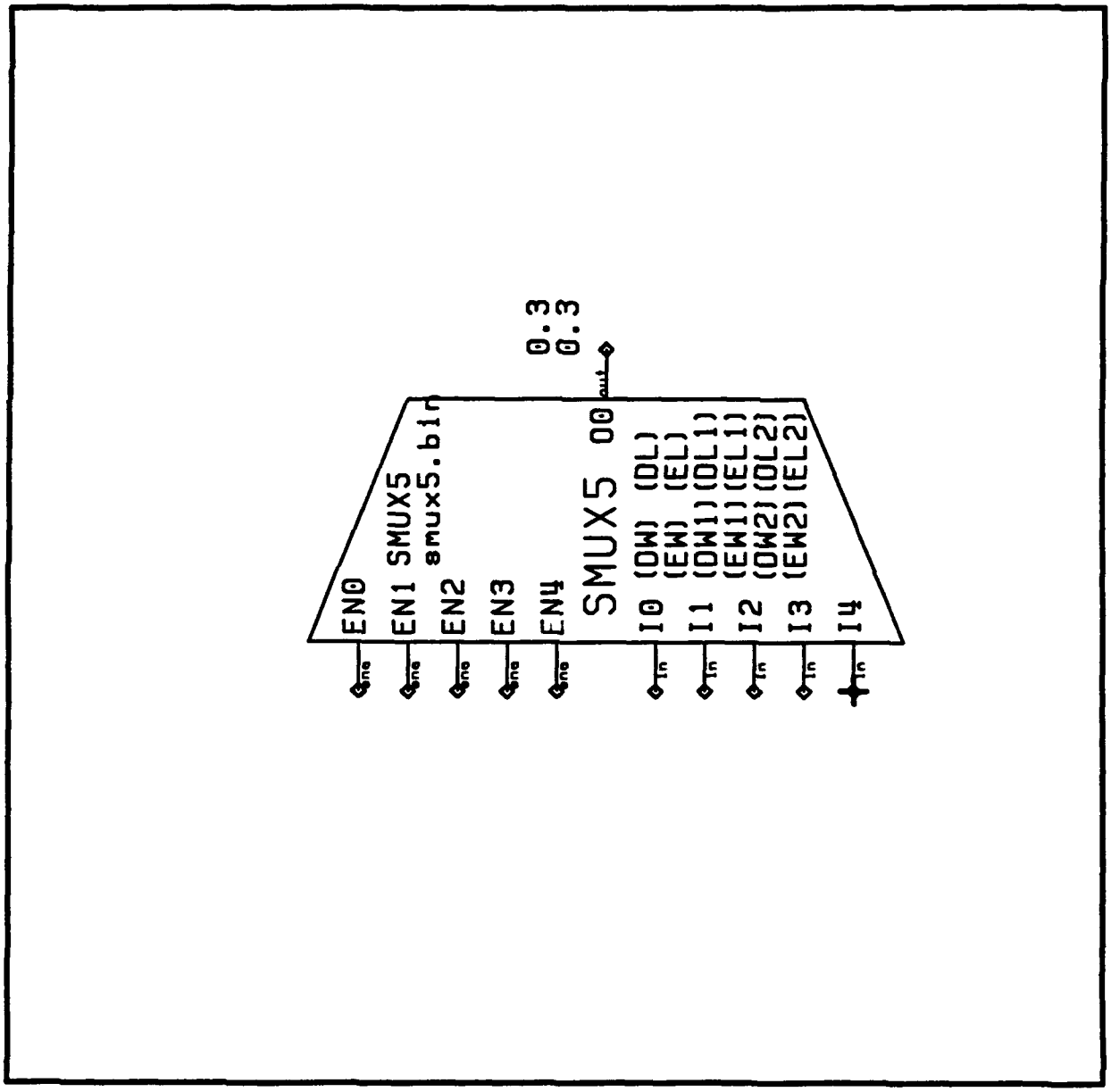

RCVR2
Revised 8/24/89
O1
I1
CG
VTT

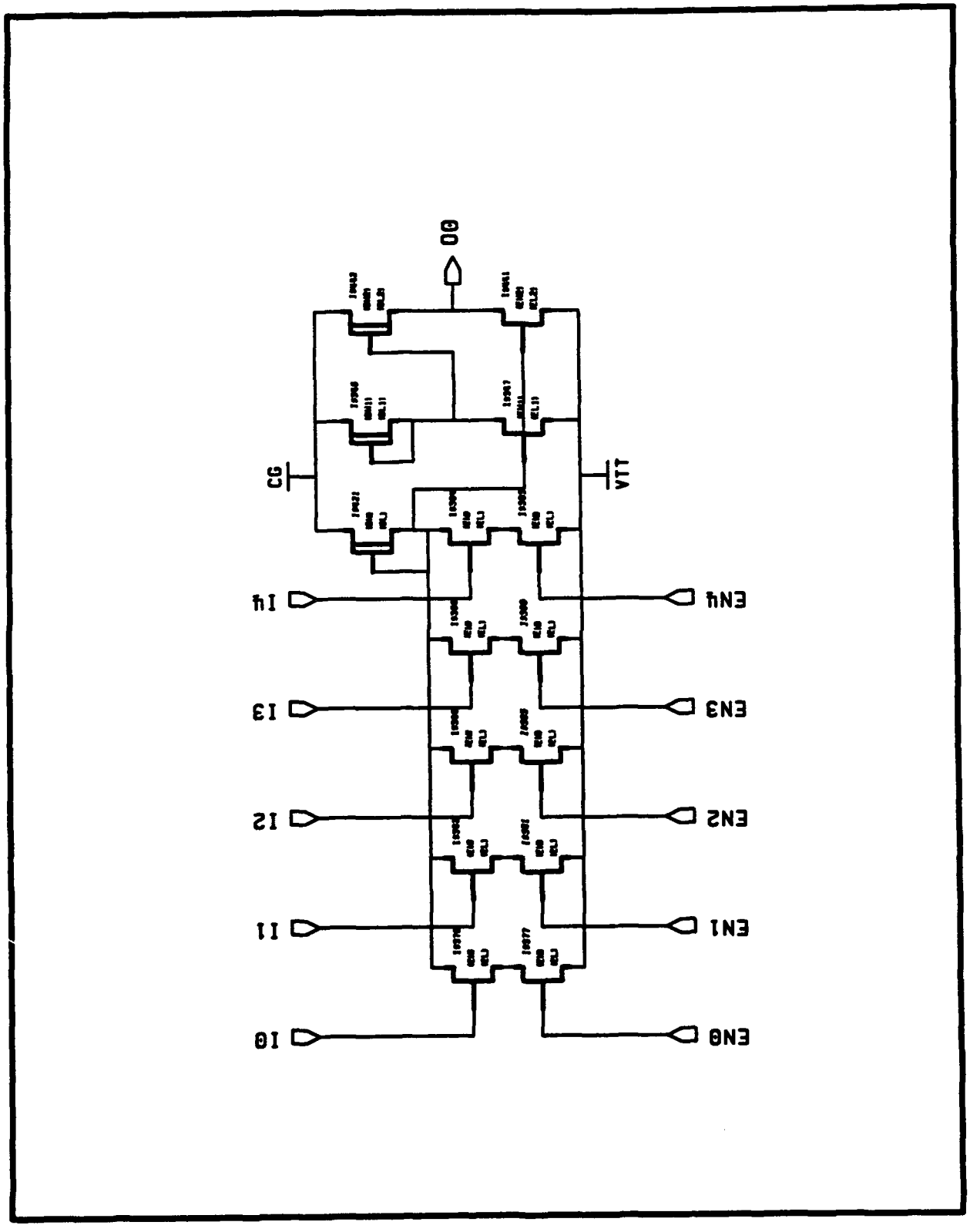

UXX
REGBIT
OUT
Q
CLR
NI
D
LD
CLK
IN
IN
IN

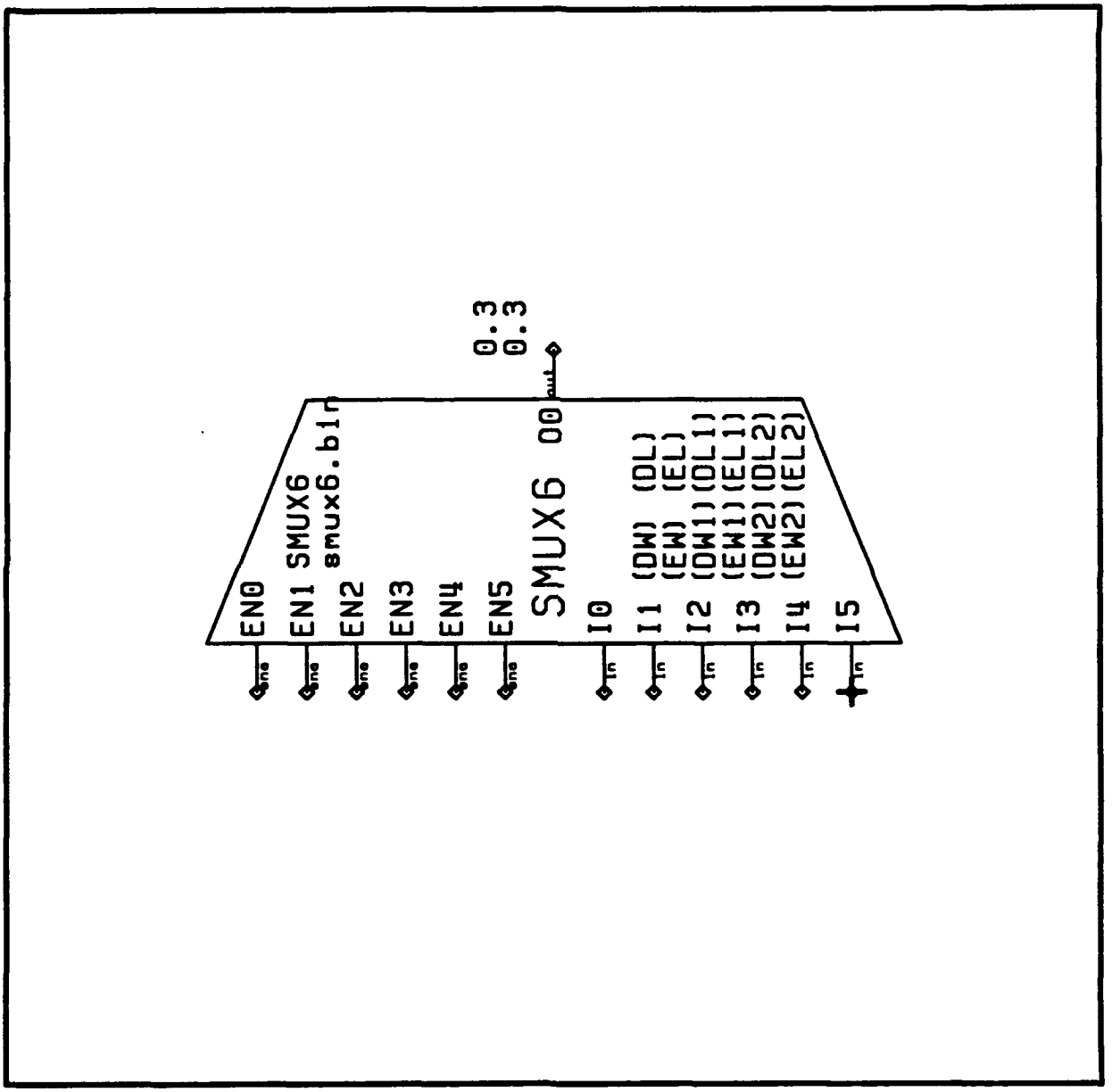

Q
CLK
CLR
D
LD
REGBIT

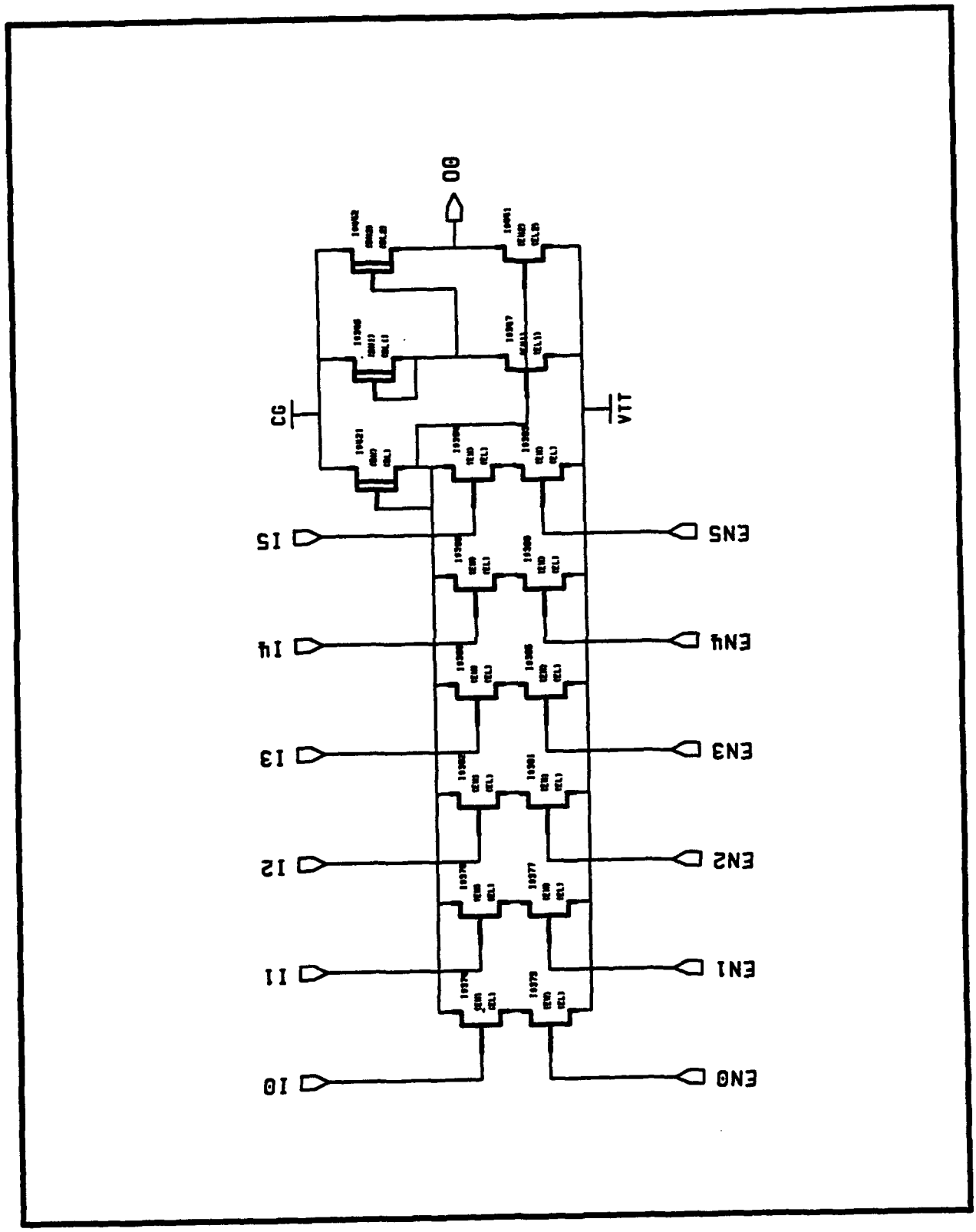

UXX
REGBUF
LDBUF
CLRBUF
CLKBUF
OUT
OUT
OUT
LD
CLR
CLK
IN
IN
IN

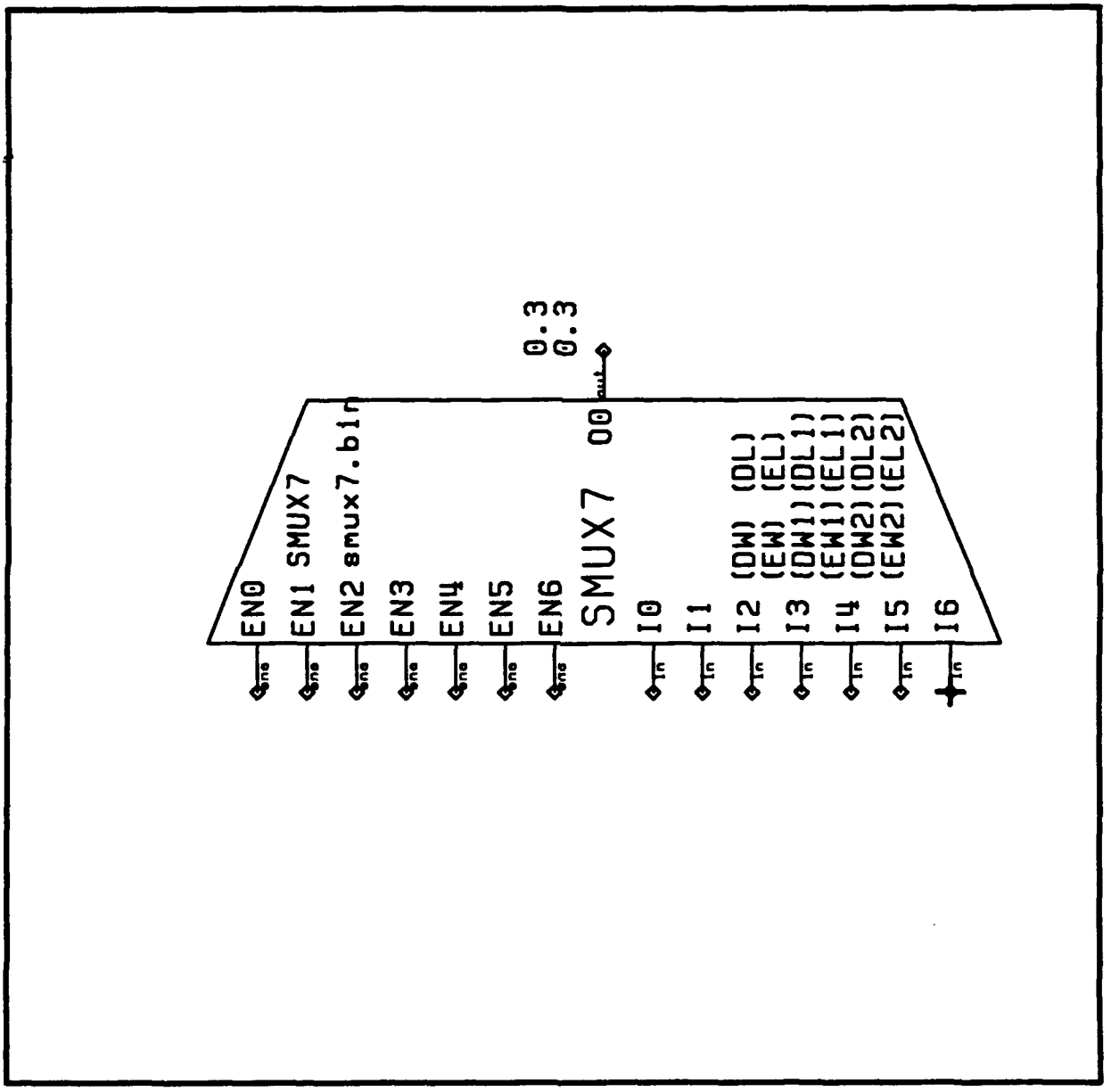

CLRBUF
LDBUF
CLKBUF
S
I1:2
SINV
I1:22
INV
I1:3
I1:4
I1:5
CLR
LD
CLK
REGBUF: buffer for REGBIT

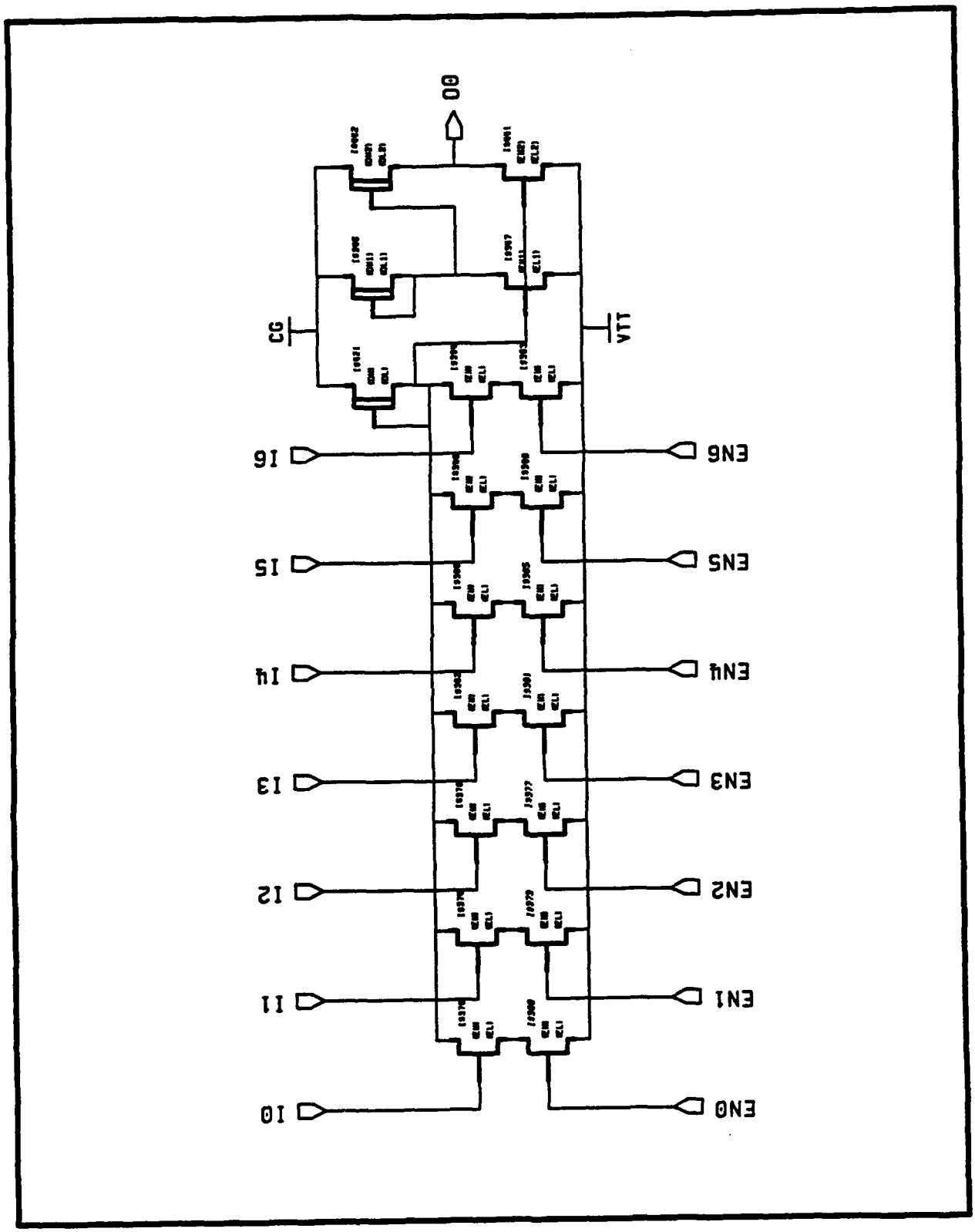

0.3
0.3
SMUX5 00
SMUX5
smux5.bin
EN0
EN1
EN2
EN3
EN4
I0 (0W) (0L)
(EW) (EL)
I1 (0W1)(0L1)
(EW1)(EL1)
I2 (0W2)(0L2)
I3 (EW2)(EL2)
I4

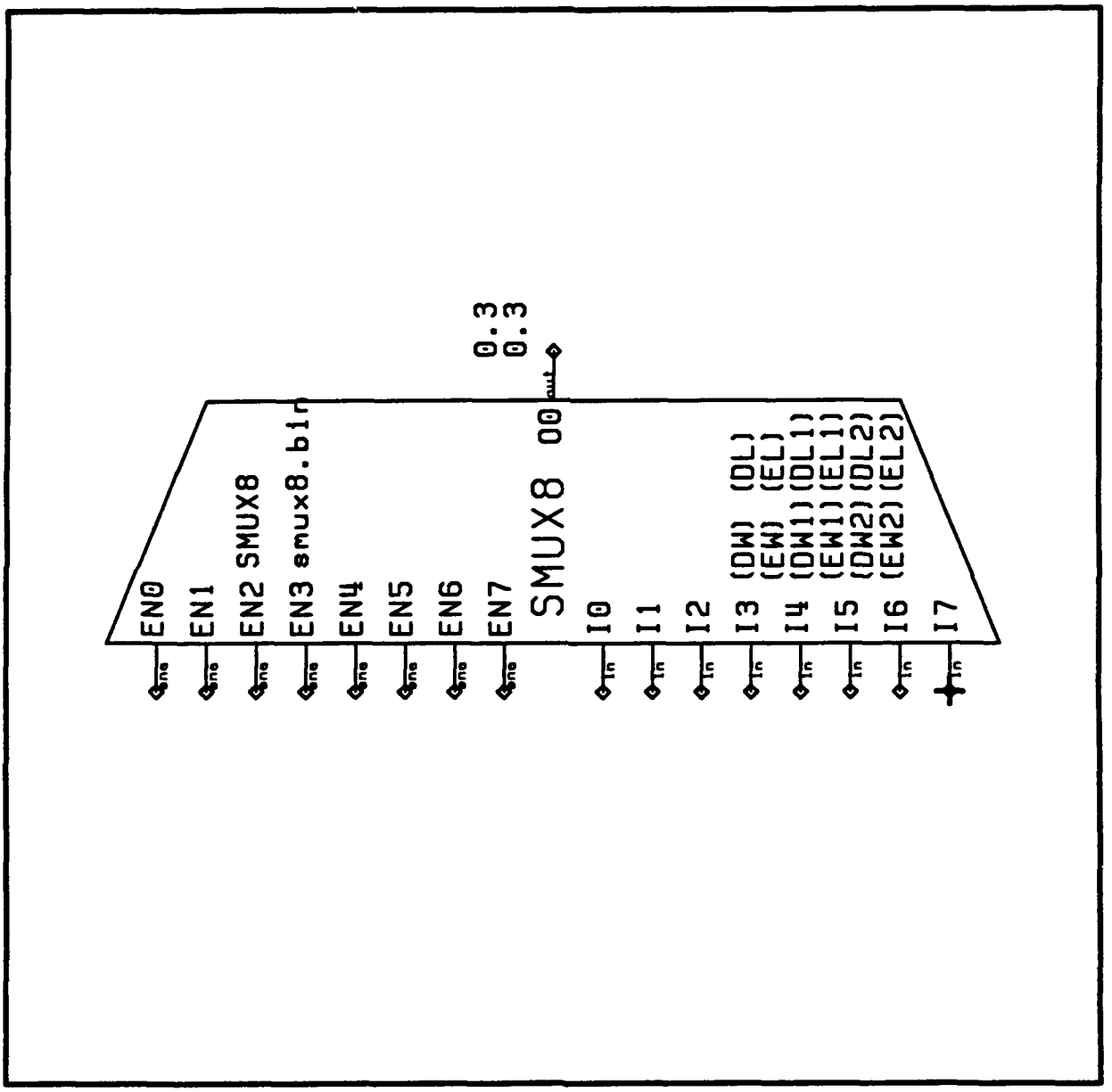

OD
CG
VTT
I4
I3
I2
I1
I0
EN4
EN3
EN2
EN1
EN0

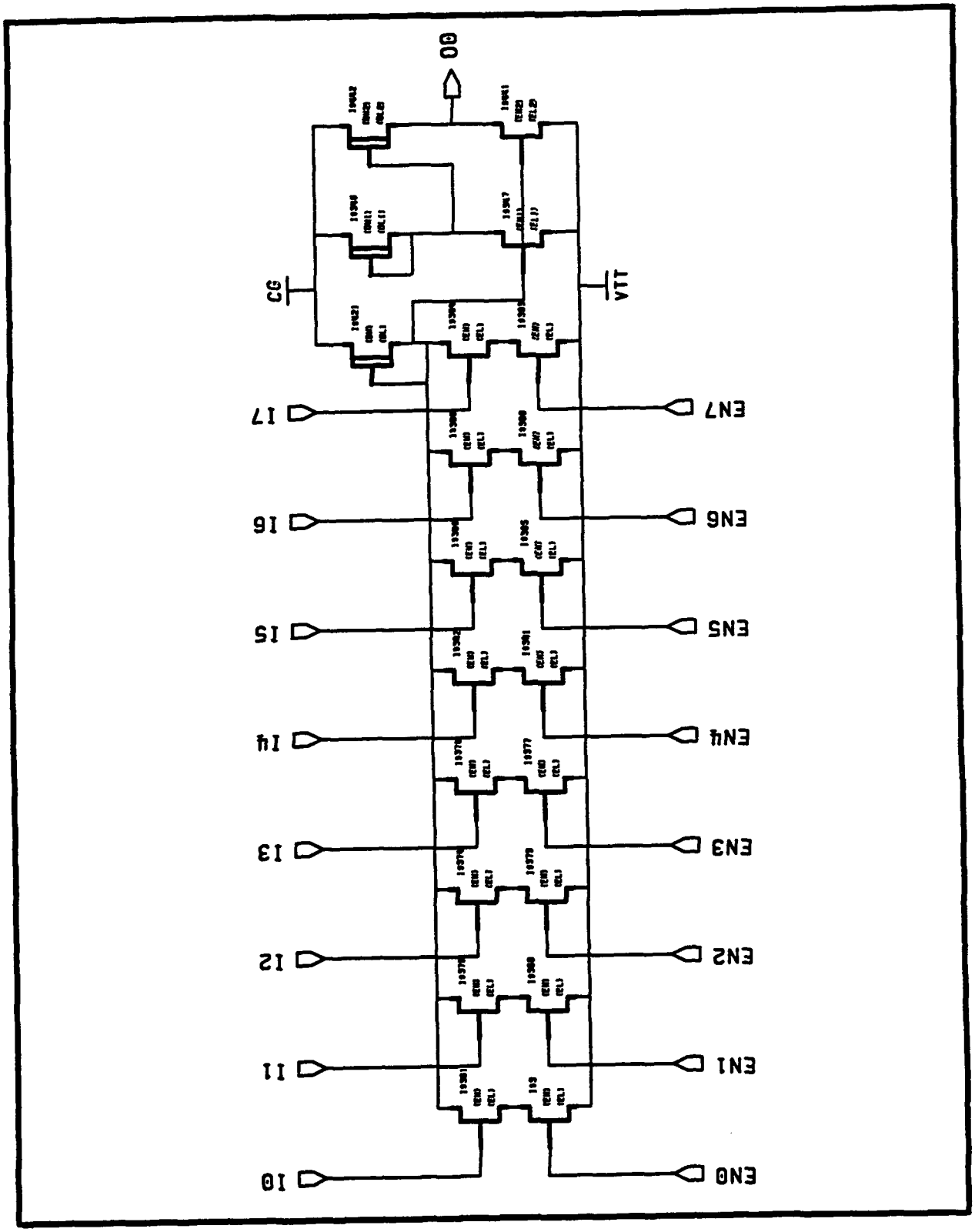

0.3
0.3
EN0
EN1 SMUX6
smux6.bin
EN2
EN3
EN4
EN5
SMUX6 00
I0
I1 (DW) (DL)
(EW) (EL)
I2 (DW1)(DL1)
(EW1)(EL1)
I3 (DW2)(DL2)
I4 (EW2)(EL2)
I5

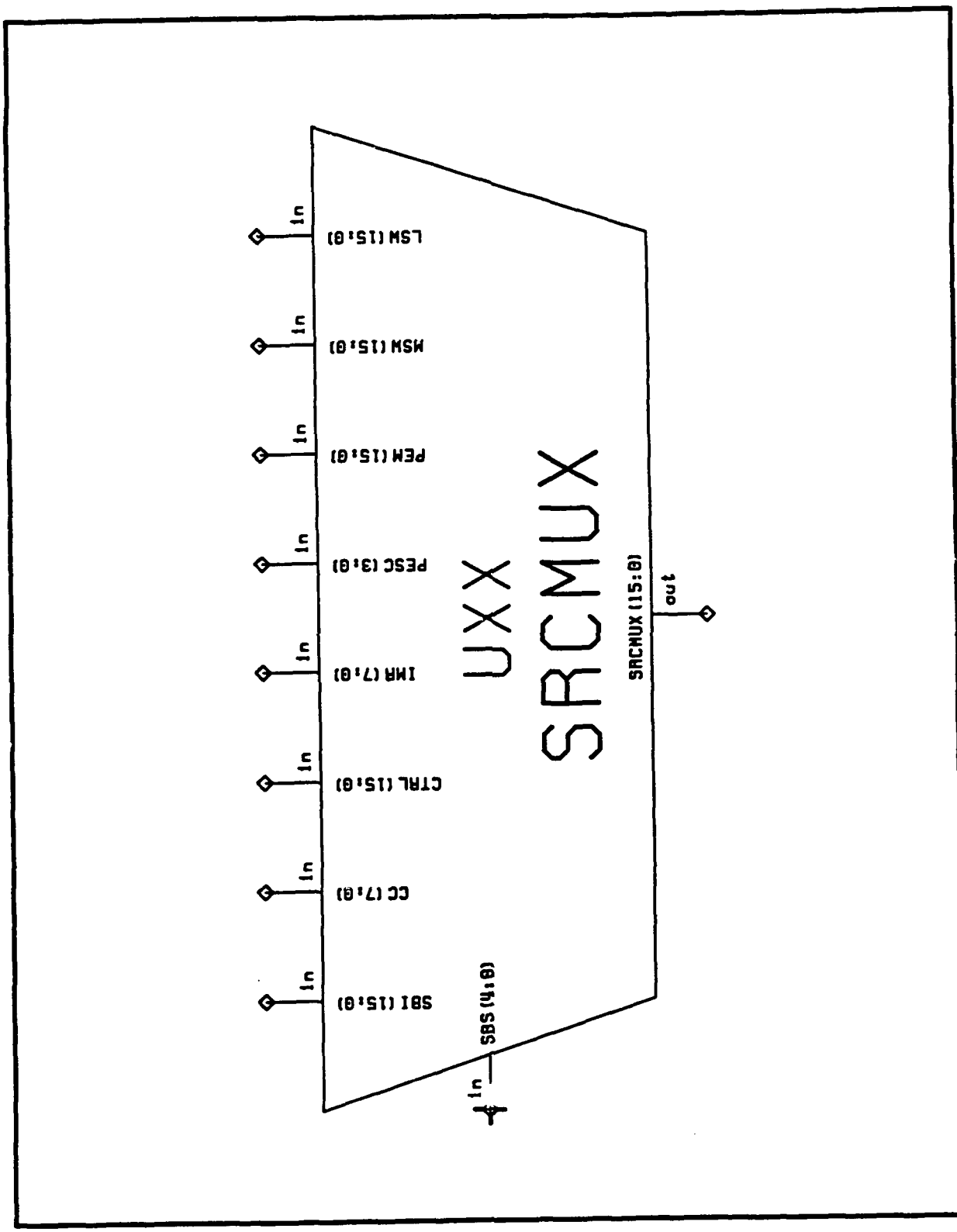

OO
CG
VTT
I5
I4
I3
I2
I1
I0
EN5
EN4
EN3
EN2
EN1
EN0

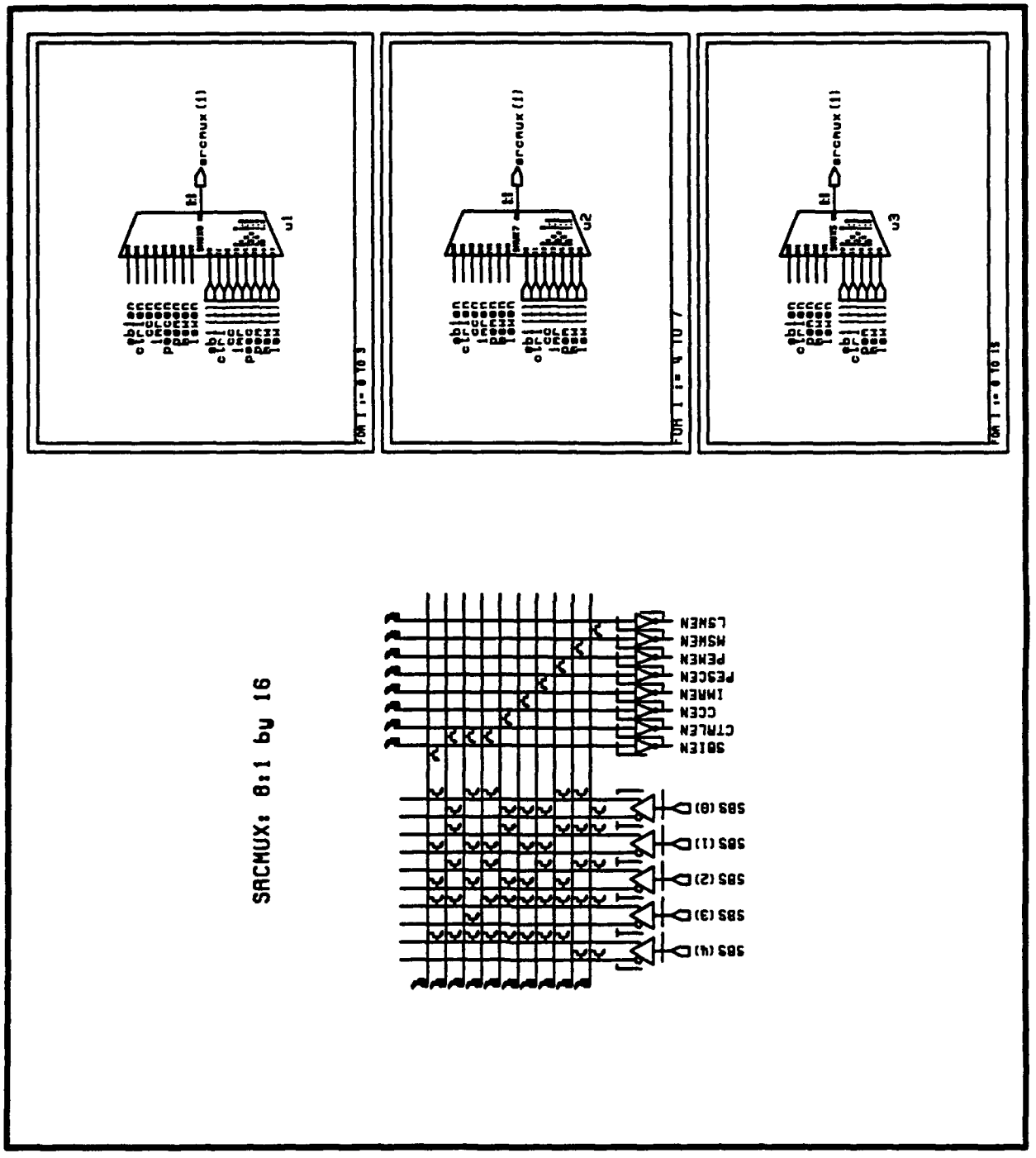

0.3
0.3
SMUX7
O0
EN0
EN1 SMUX7
EN2 smux7.bin
EN3
EN4
EN5
EN6
I0
I1
I2 (DW) (DL)
(EW) (EL)
I3 (DW1)(DL1)
(EW1)(EL1)
I4 (DW2)(DL2)
(EW2)(EL2)
I5
I6

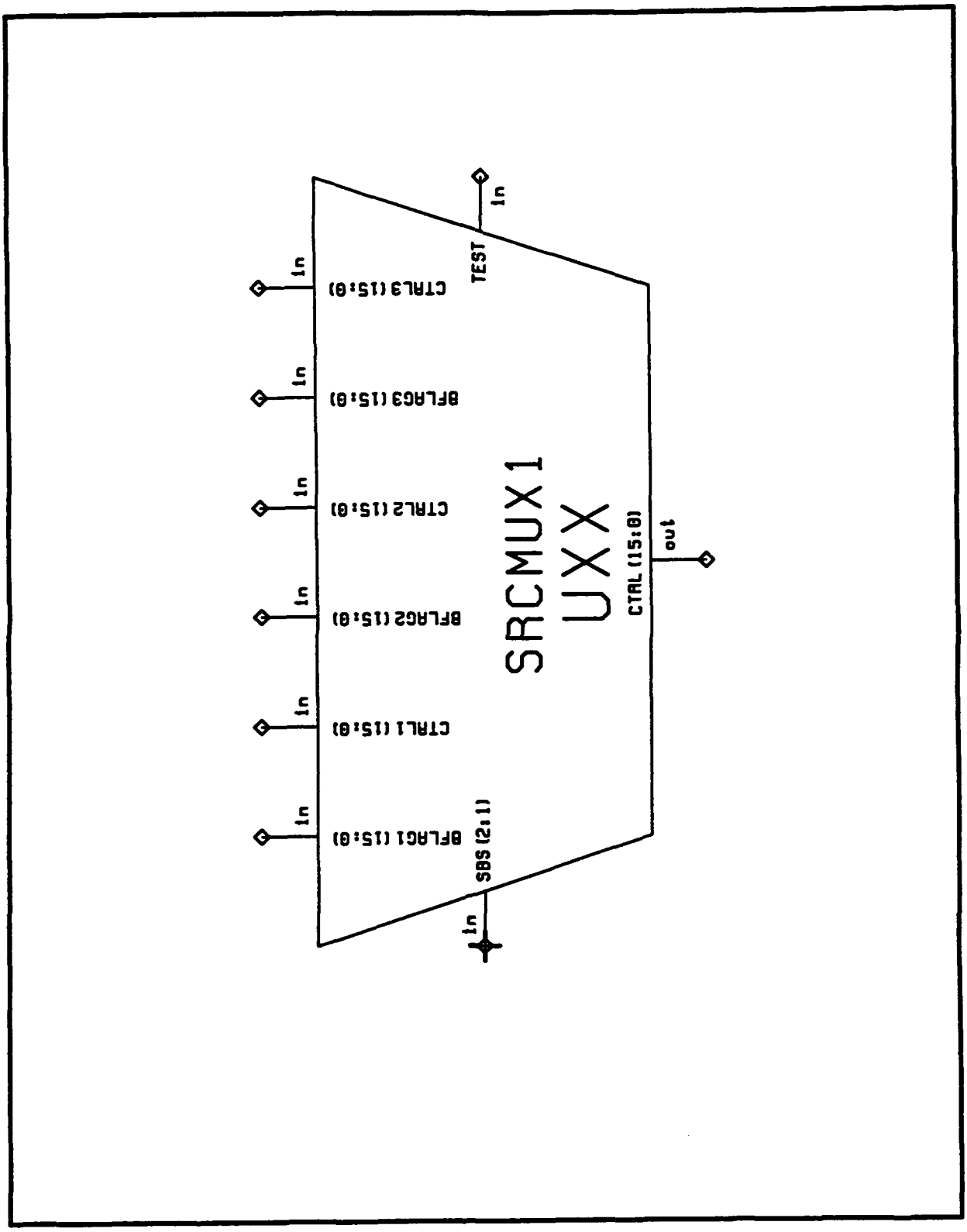

OD
CG
VTT
I6
I5
I4
I3
I2
I1
I0
EN6
EN5
EN4
EN3
EN2
EN1
EN0

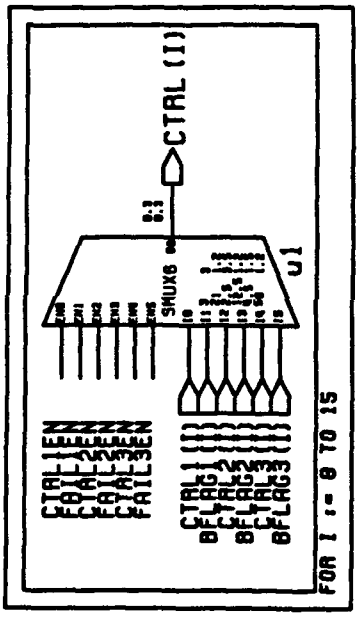

0.3
0.3
SMUX8
EN0
EN1
EN2 SMUX8
EN3 smux8.bin
EN4
EN5
EN6
EN7
I0
I1
I2
I3 (DW) (DL)
(EW) (EL)
I4 (DW1)(DL1)
(EW1)(EL1)
I5 (DW2)(DL2)
(EW2)(EL2)
I6
I7

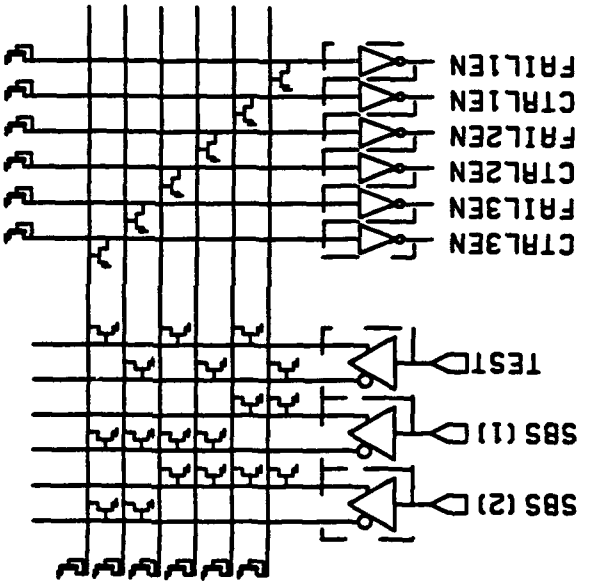

O0
CG
VTT
I7
I6
I5
I4
I3
I2
I1
I0
EN7
EN6
EN5
EN4
EN3
EN2
EN1
EN0

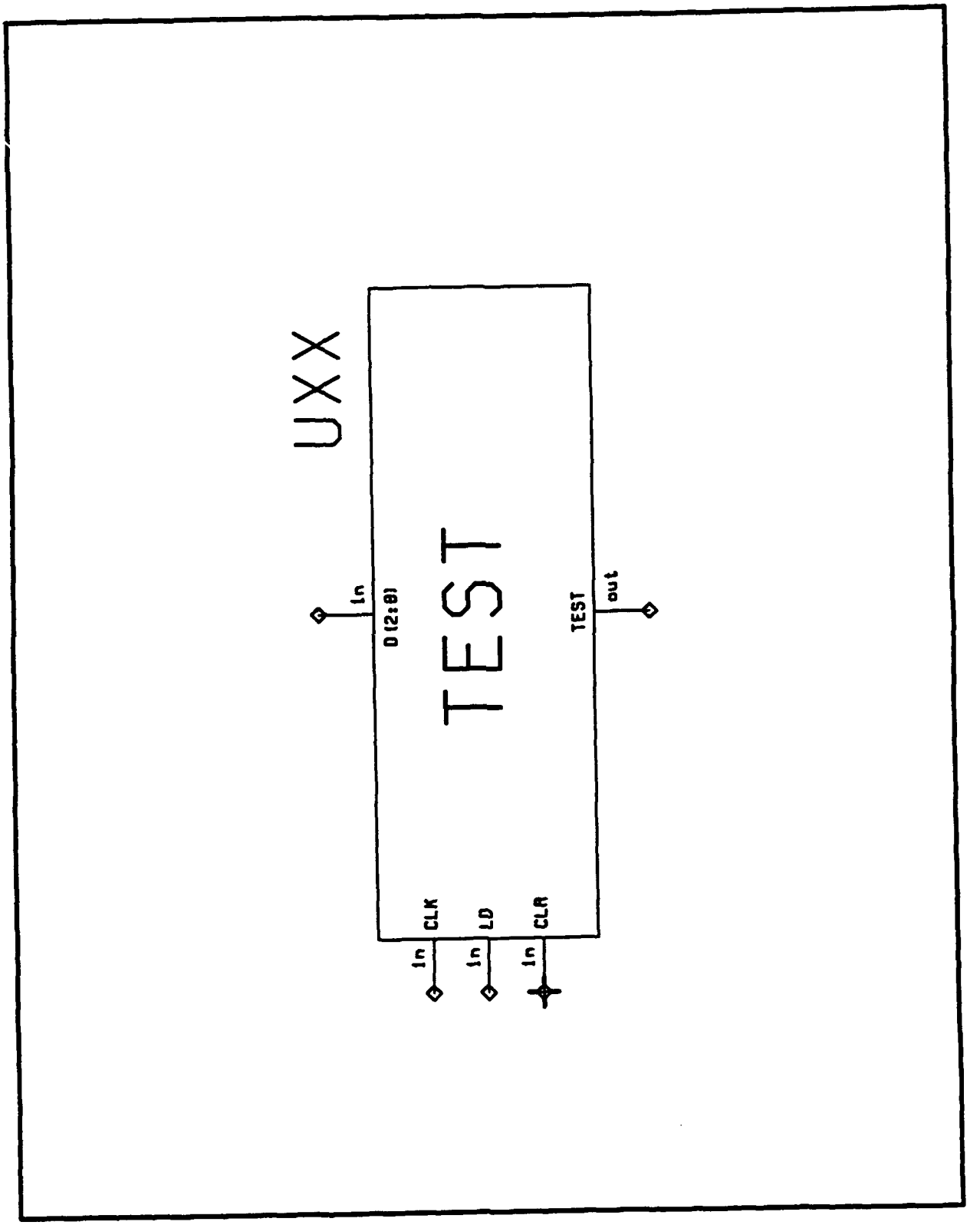

UXX
SRCMUX
LSW (15:0)
MSW (15:0)
PEM (15:0)
PESC (3:0)
IMR (7:0)
CTRL (15:0)
CC (7:0)
SBI (15:0)
SBS (4:0)
SRCMUX (15:0)
in
out

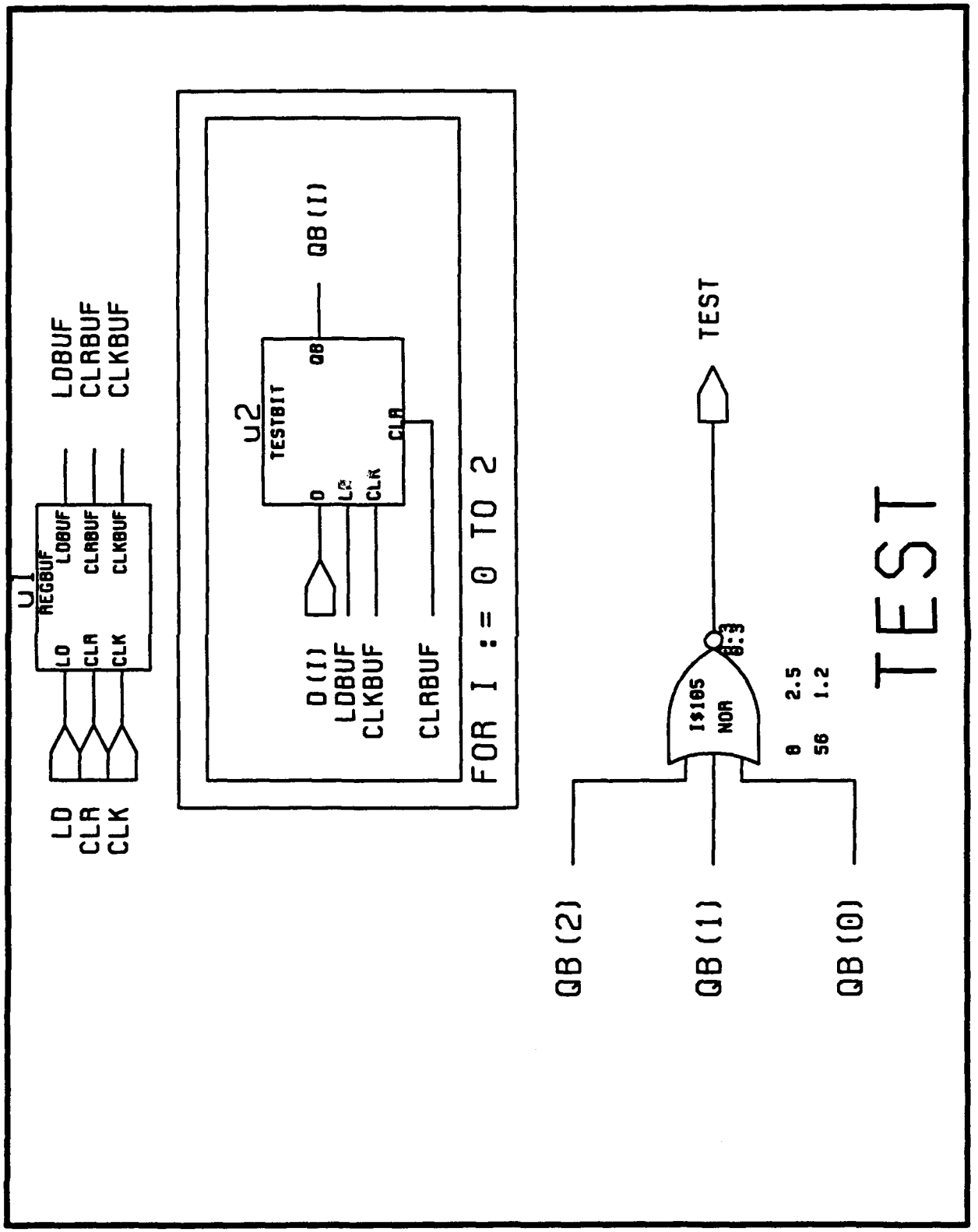

SRCMUX: 8:1 by 16
LSNEN
MSNEN
PENEN
PESCEN
IMMEN
CCEN
CTMLEN
SBIEN
SBS(0)
SBS(1)
SBS(2)
SBS(3)
SBS(4)

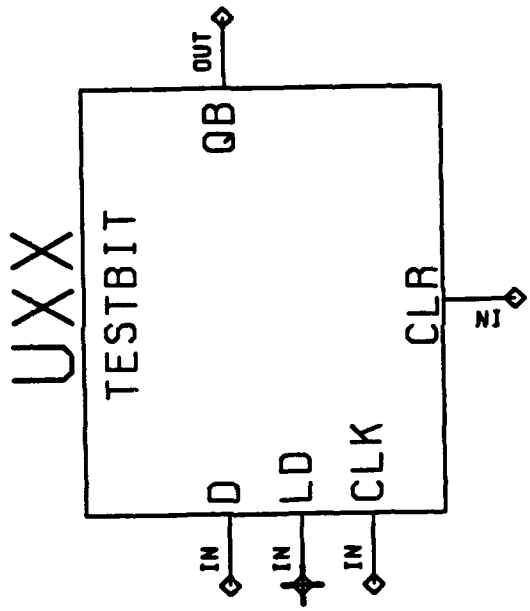

SRCMUX1
UXX
in
TEST
in
CTRL3 (15:0)
in
BFLAG3 (15:0)
in
CTRL2 (15:0)
in
BFLAG2 (15:0)
in
CTRL1 (15:0)
in
BFLAG1 (15:0)
SBS (2:1)
in
CTRL (15:0)
out

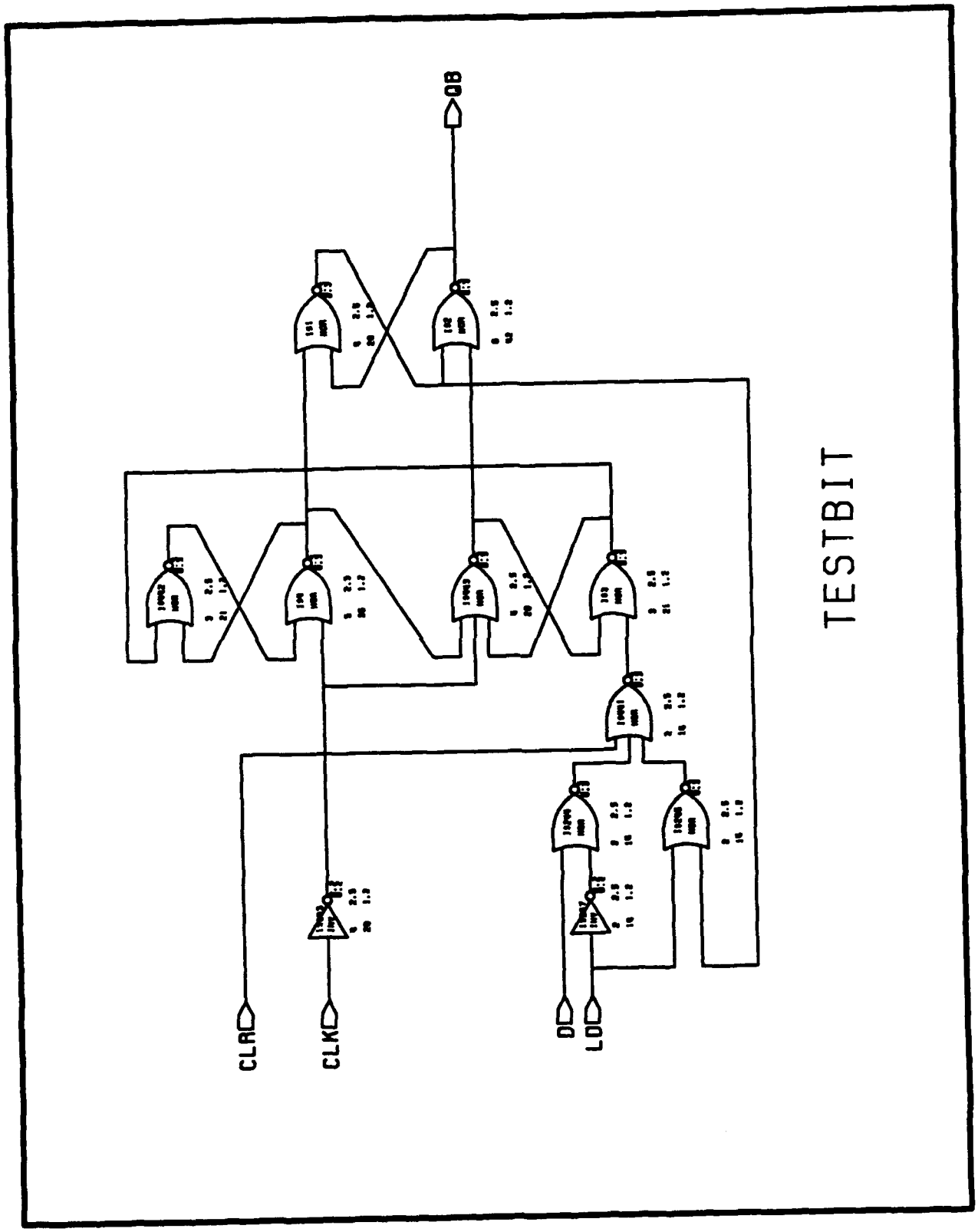

CTRL (I)
U1
SMUX6
FOR I := 0 TO 15

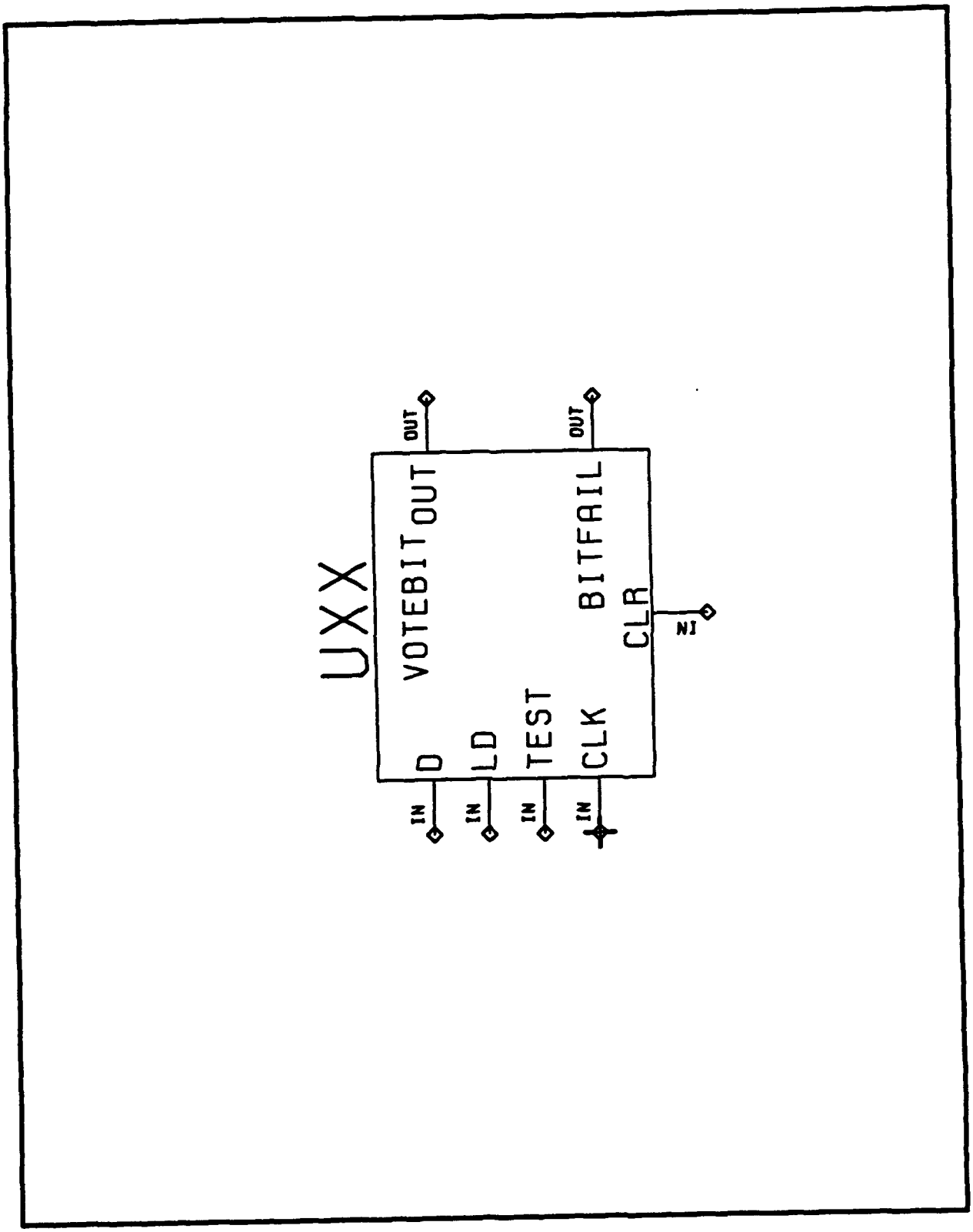

FAIL1EN
CTRL1EN
FAIL2EN
CTRL2EN
FAIL3EN
CTRL3EN
TEST
SBS (1)
SBS (2)
SRCMUX1


UXX
TEST
In
D(2:8)
TEST
out
CLK
LD
CLR
In
In
In

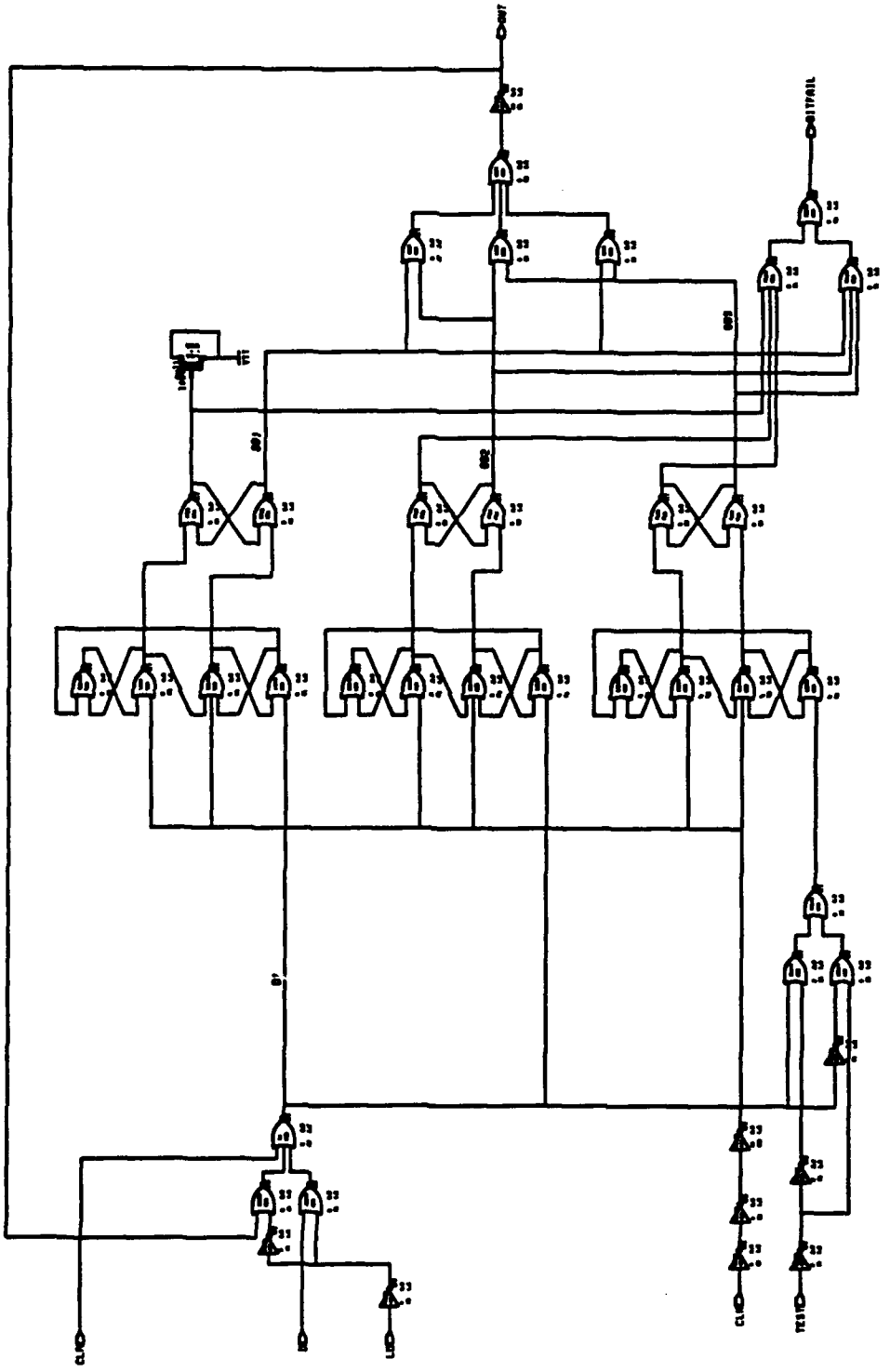

TEST
TEST
QB(2)
QB(1)
QB(0)
I$105
NOR
8:3
8 2.5
56 1.2
FOR I := 0 TO 2
QB(I)
U2
TESTBIT
D
CLR
D(I)
LDBUF
CLKBUF
CLRBUF
U1
REGBUF
LDBUF
CLRBUF
CLKBUF
LD
CLR
CLK

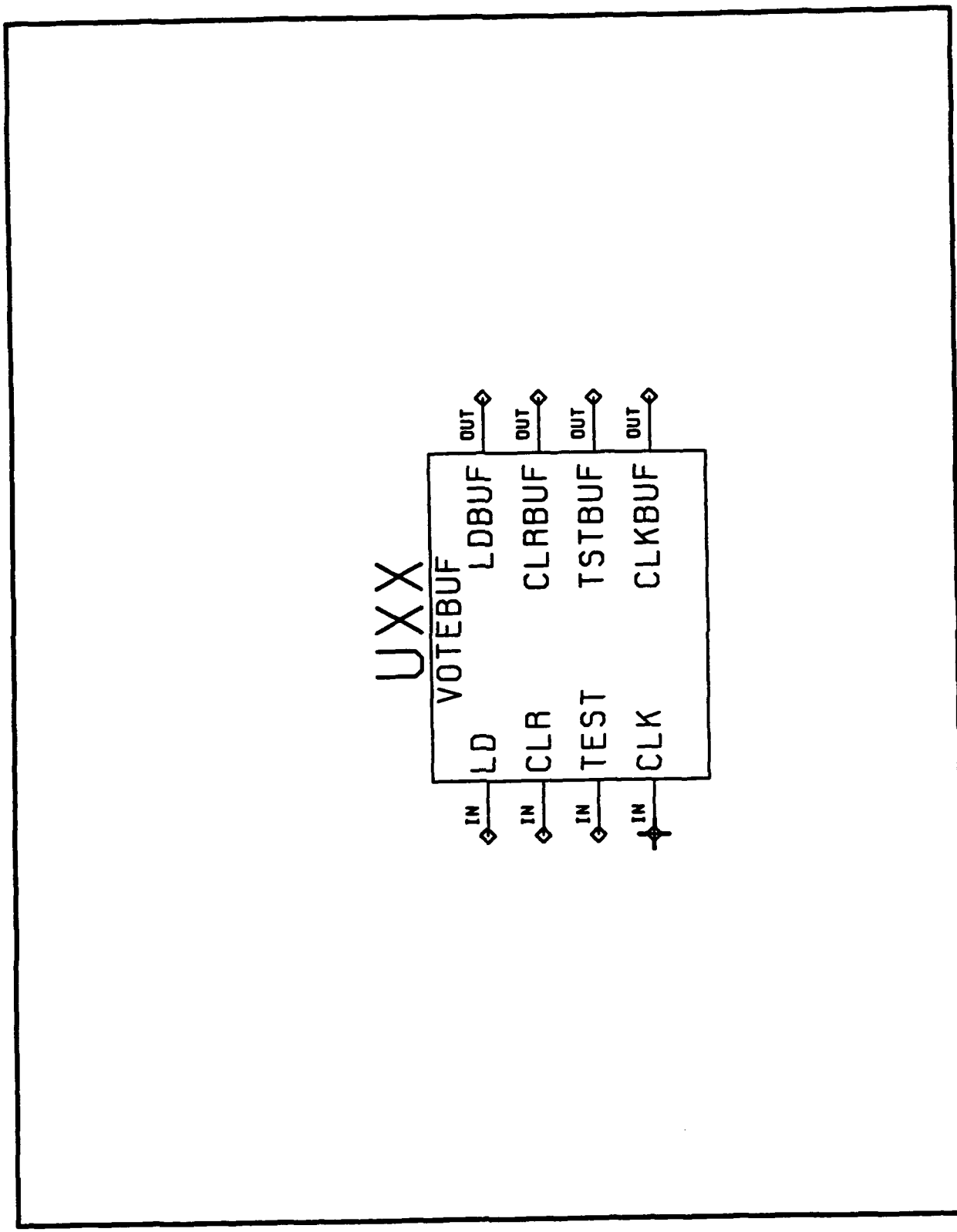

UXX
TESTBIT
QB
OUT
CLR
NI
D
LD
CLK
IN
IN
IN

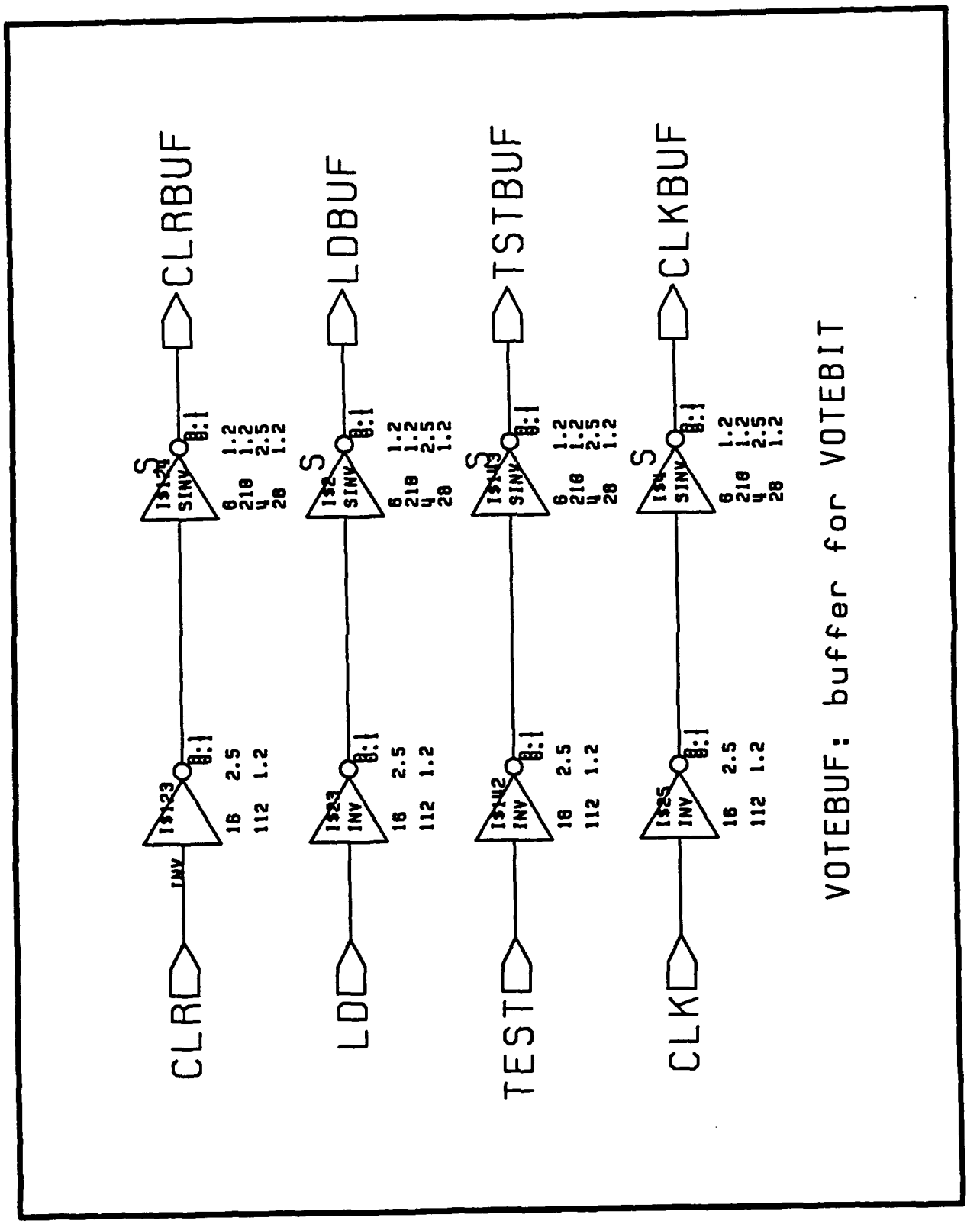

OB
TESTBIT
CLR
CLK
D
LD

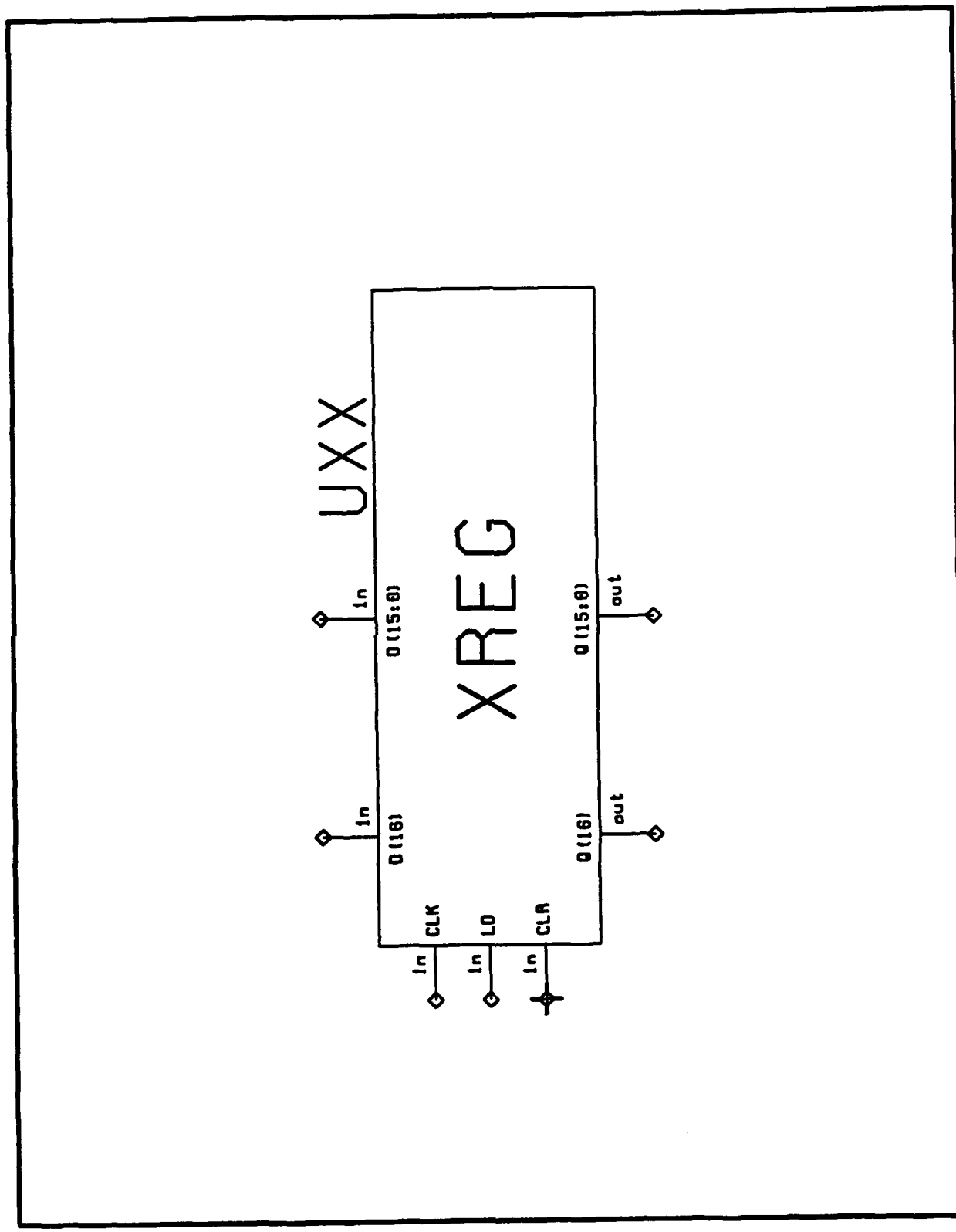

UXX
VOTEBIT OUT
BITFAIL
CLR
D
LD
TEST
CLK
OUT
OUT
IN
IN
IN
IN
NI

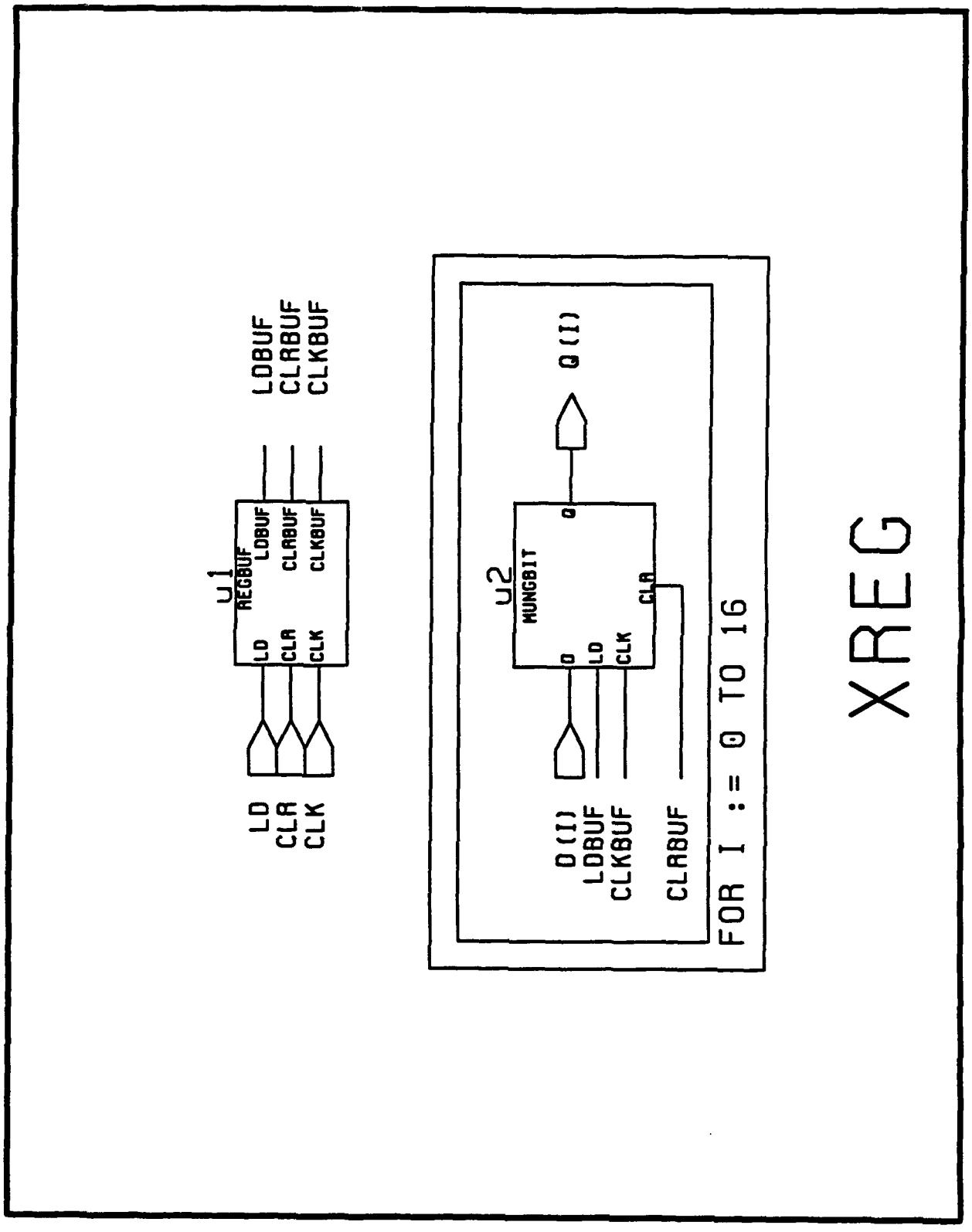
MAJORITY VOTE CIRCUIT WITH LATCHED INPUTS

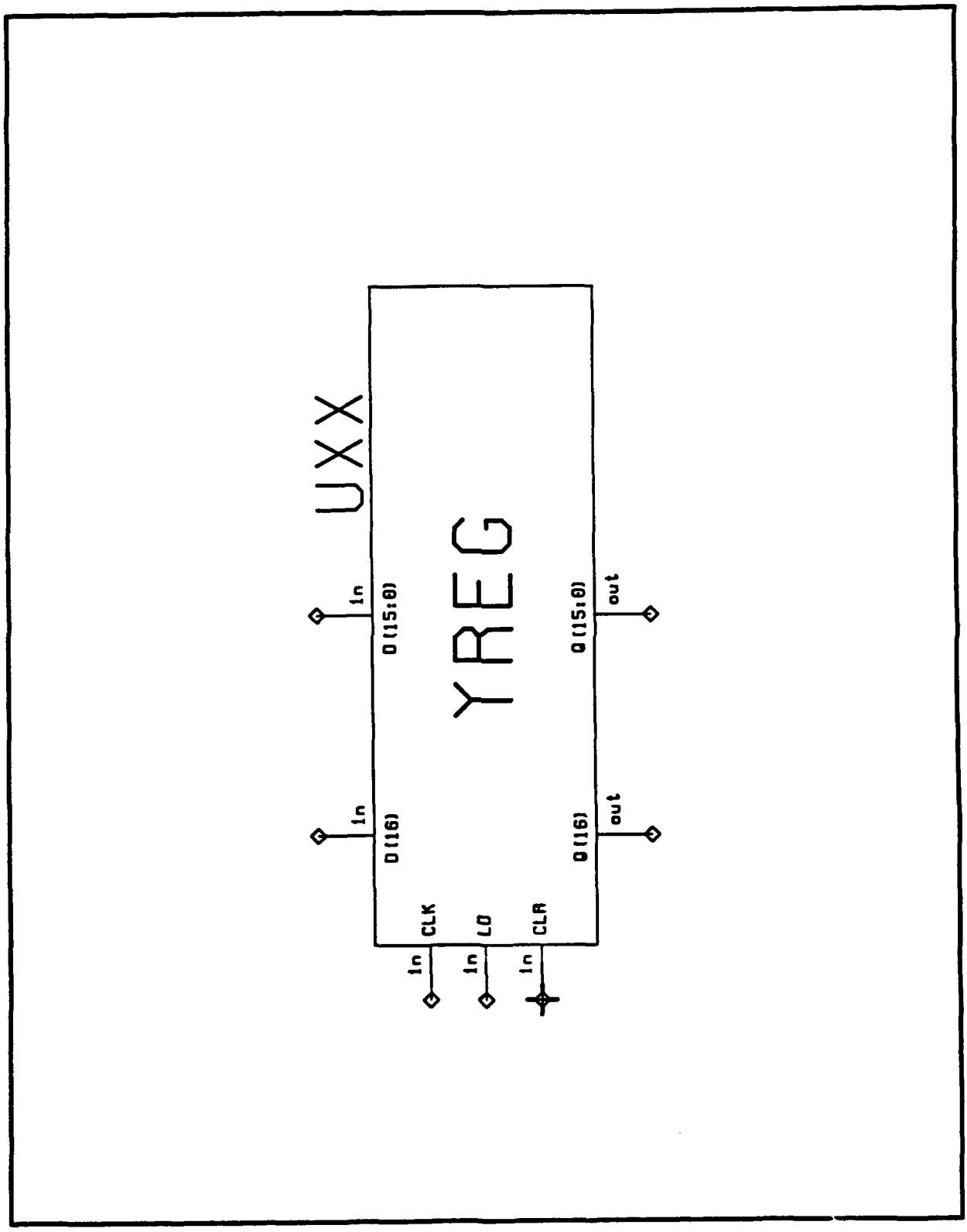


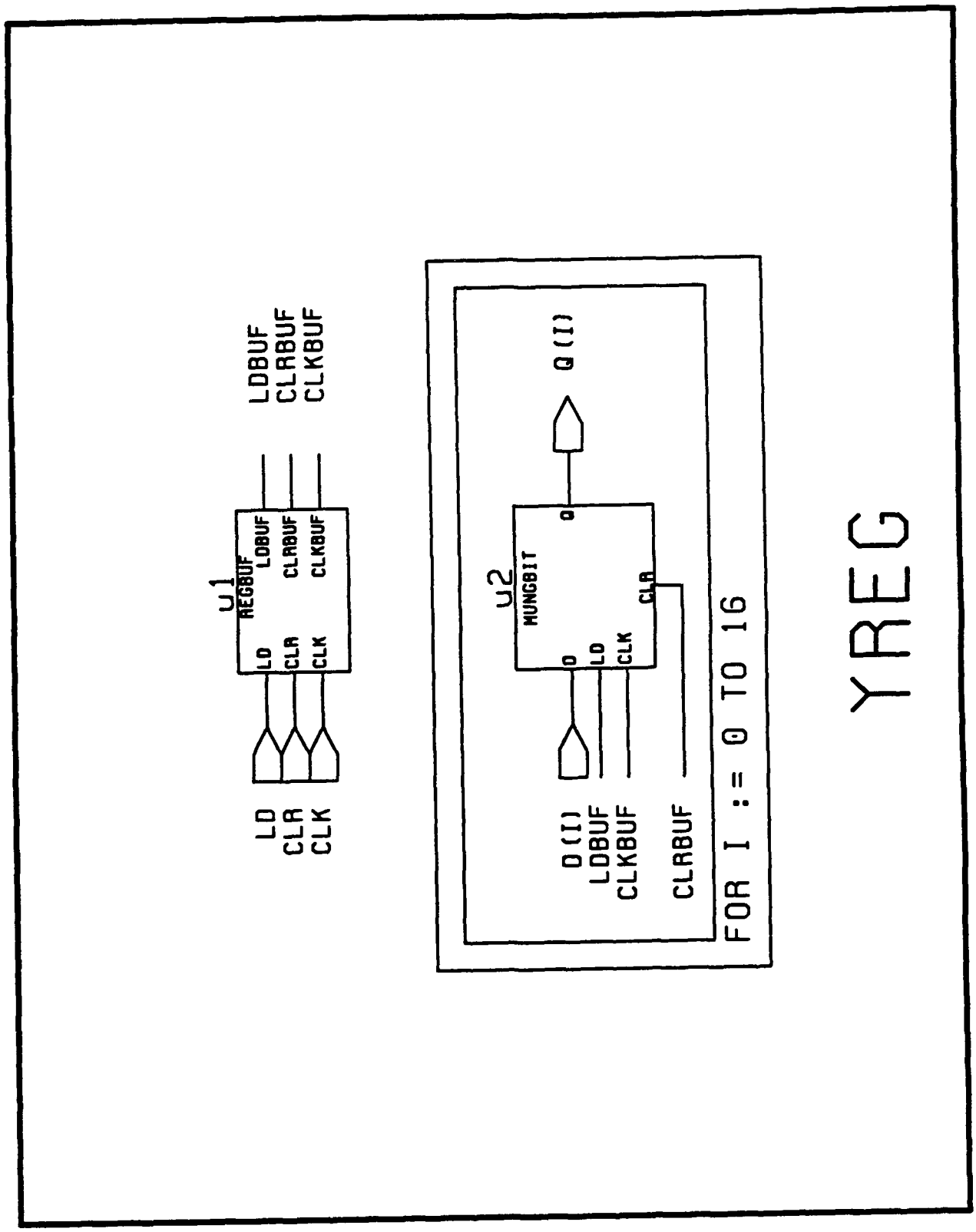

UXX
VOTEBUF
LDBUF
CLRBUF
TSTBUF
CLKBUF
LD
CLR
TEST
CLK
IN
IN
IN
IN
OUT
OUT
OUT
OUT

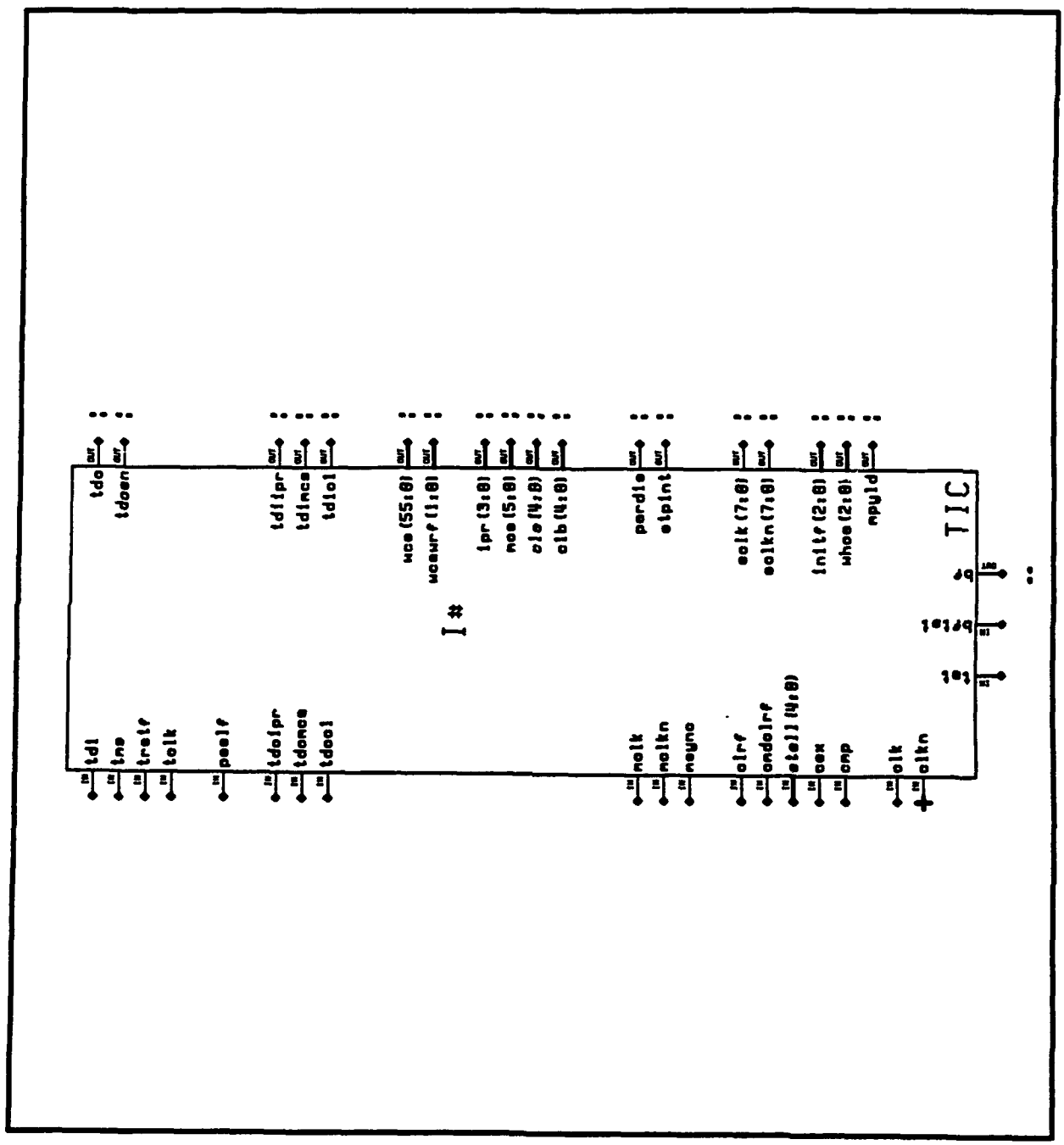

VOTEBUF: buffer for VOTEBIT
CLRBUF
LDBUF
TSTBUF
CLKBUF
CLR
LD
TEST
CLK
INV
SINV
S
B:1
1.2 1.2 2.5 1.2
6 210 4 28
16 2.5 1.2
112

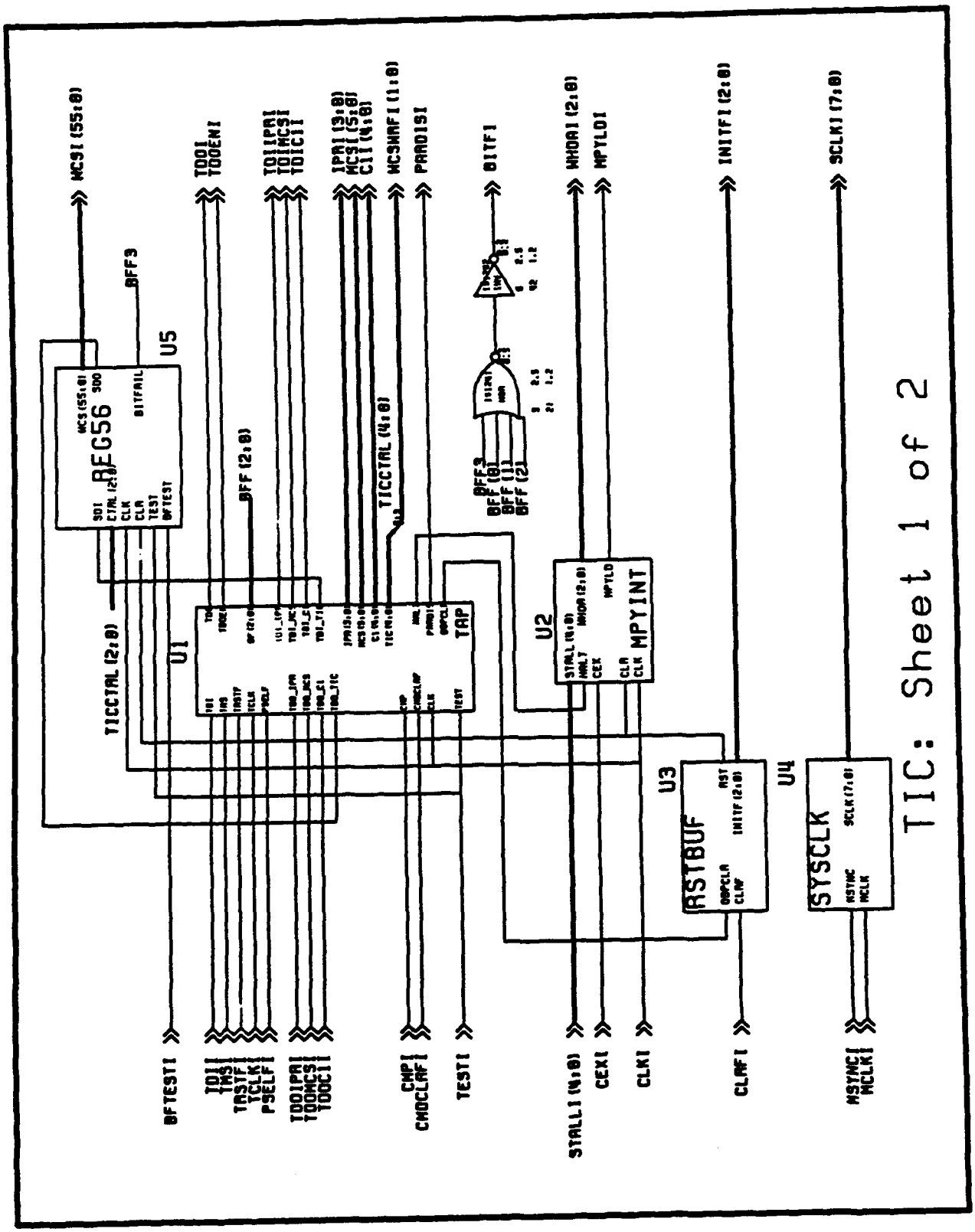

UXX
XREG
In
D(15:0)
In
D(16)
CLK
LD
CLR
In
In
In
Q(15:0)
out
Q(16)
out

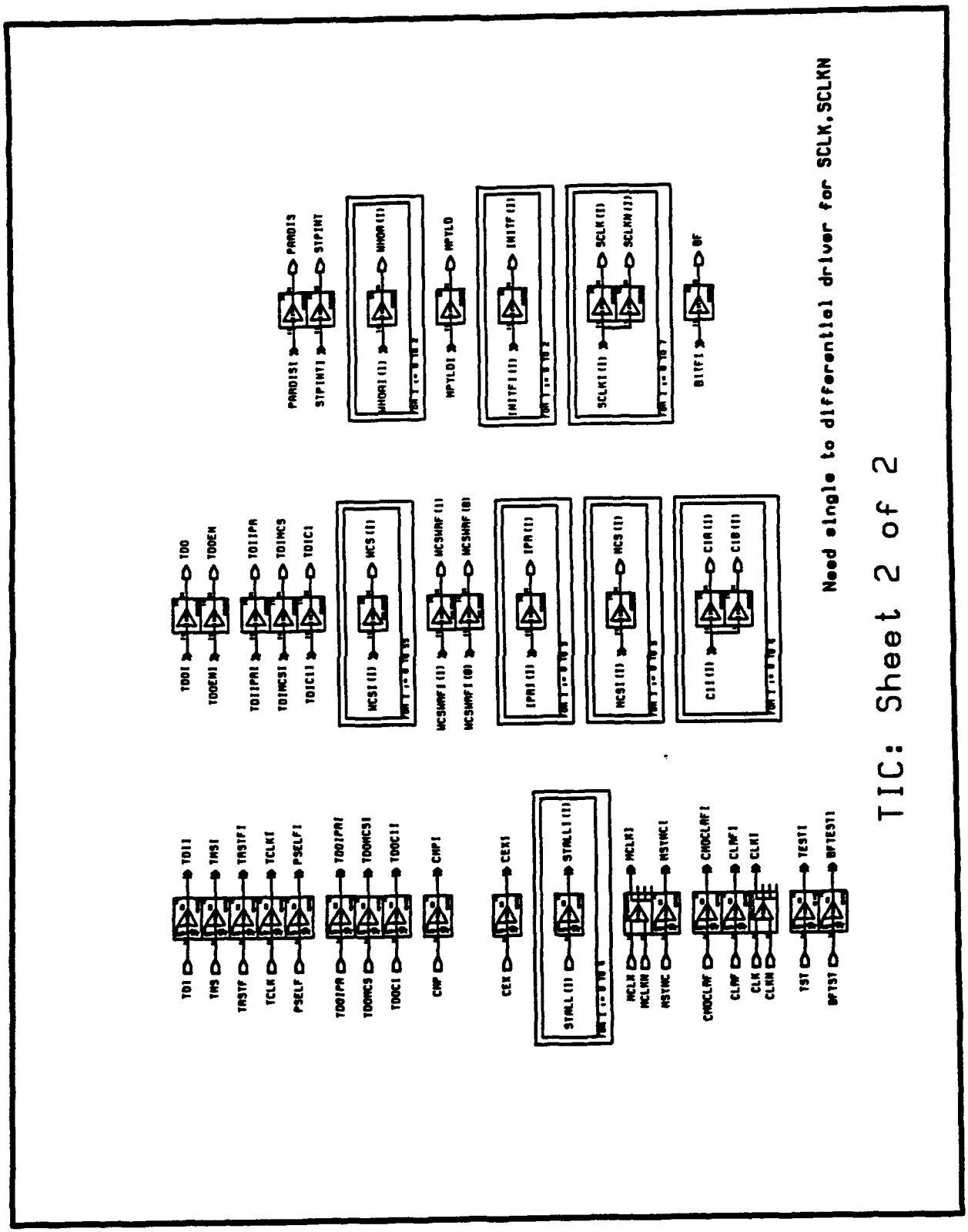

XREG
FOR I := 0 TO 16
u1
REGBUF
LDBUF
CLRBUF
CLKBUF
LD
CLR
CLK
LDBUF
CLRBUF
CLKBUF
u2
MUNGBIT
D
Q
LD
CLK
CLR
Q(I)
D(I)
LDBUF
CLKBUF
CLRBUF

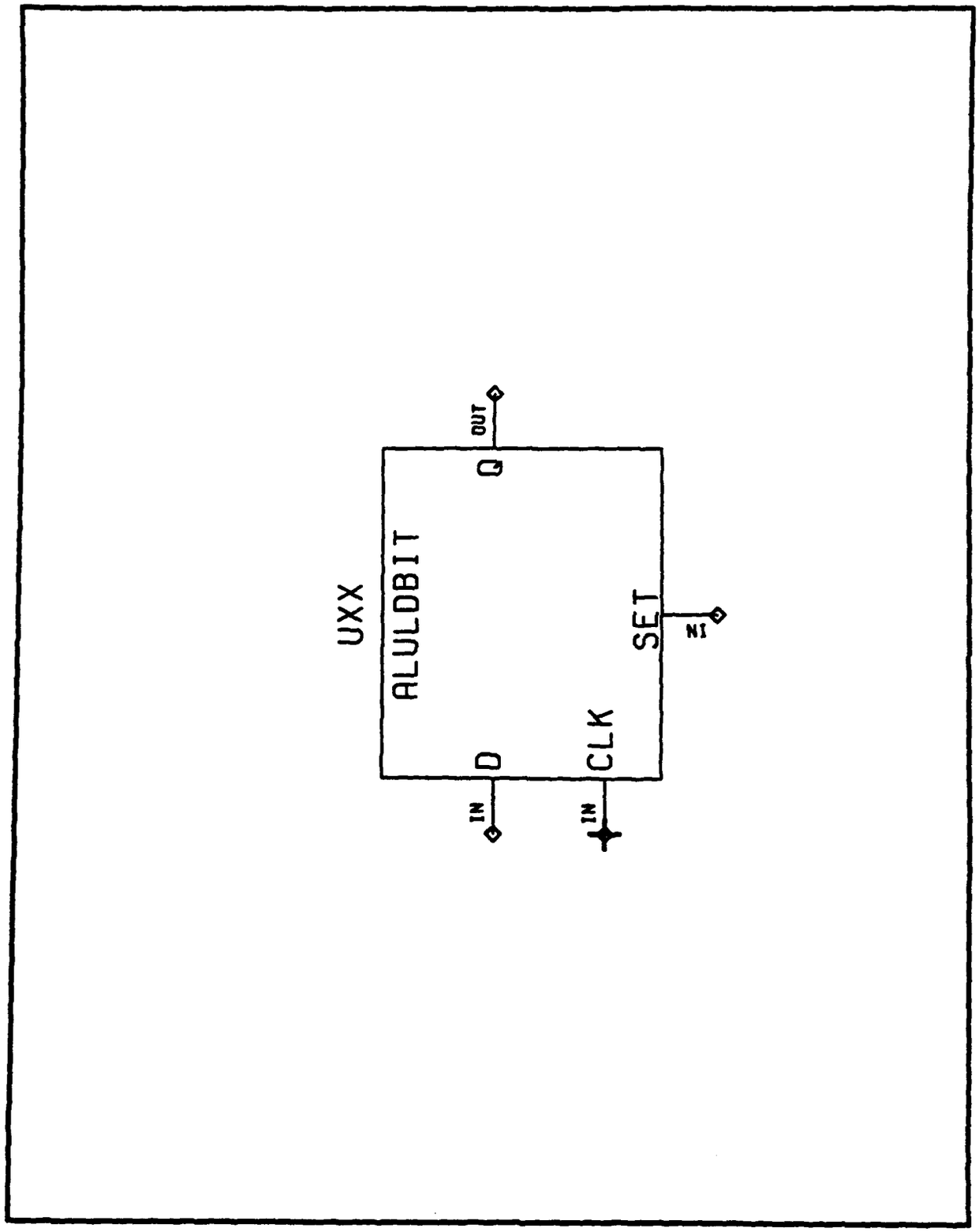

UXX
YREG
In
D(15:0)
Q(15:0)
out
In
D(16)
Q(16)
out
CLK
LD
CLR
In
In
In

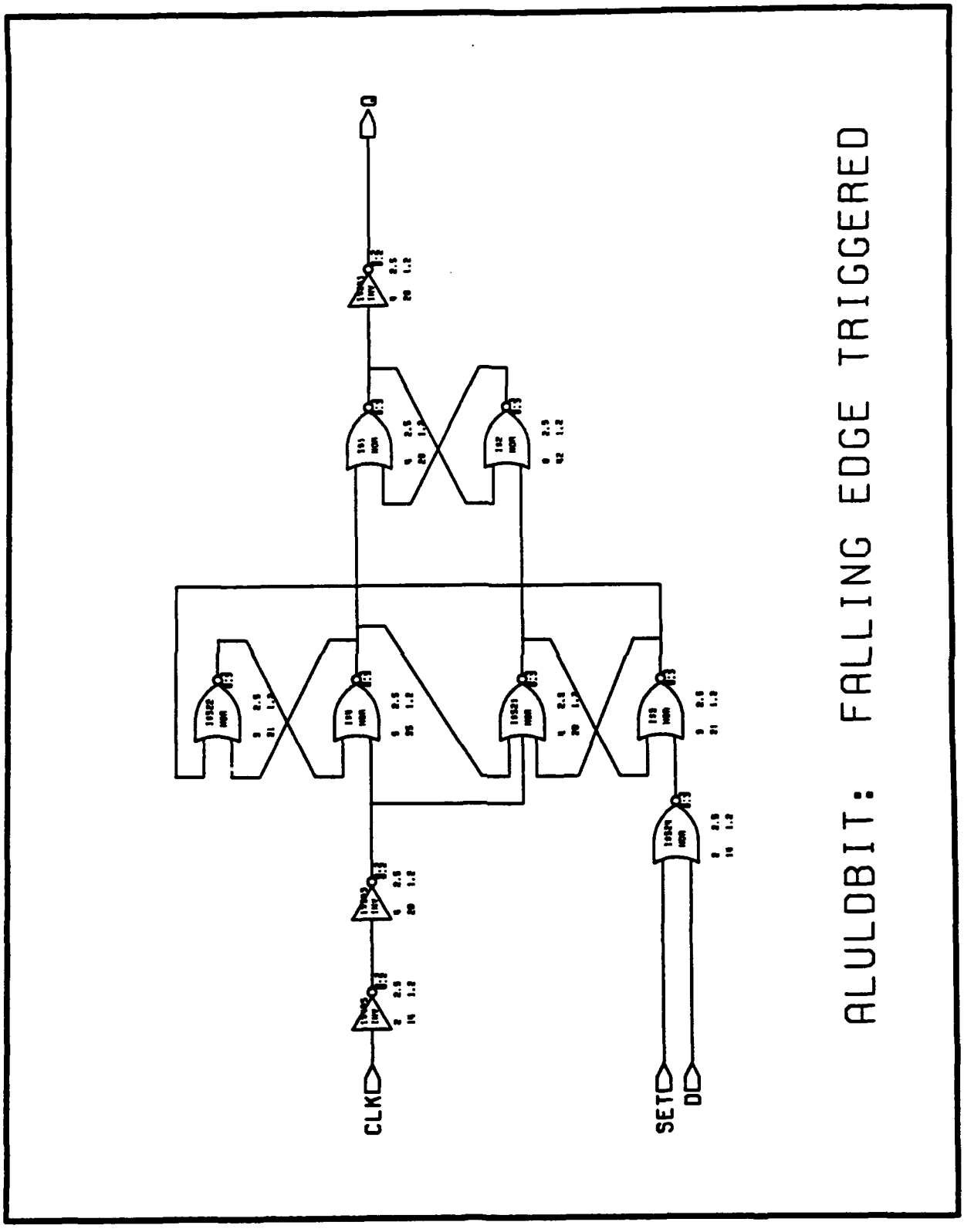

YREG
FOR I := 0 TO 16
u1
REGBUF
LDBUF
CLRBUF
CLKBUF
LD
CLR
CLK
u2
MUNGBIT
Q(I)
D(I)
LDBUF
CLKBUF
CLRBUF

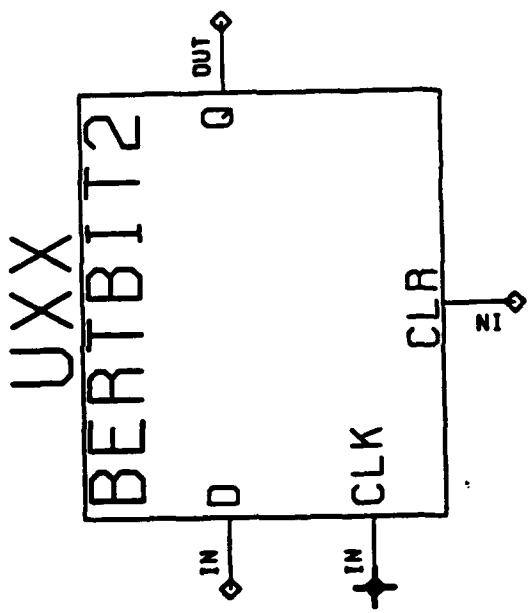

TIC
tdo
tdoen
tdilpr
tdince
tdiol
mca(55:0)
mcawrf(1:0)
ipr(3:0)
mca(5:0)
clo(N:0)
clb(4:0)
perdle
elpint
eolk(7:0)
eolkn(7:0)
intlf(2:0)
whea(2:0)
mpuld
tdl
tne
trelf
tolk
peelf
tdolpr
tdonce
tdool
nolk
nolkn
neyne
olrf
endolrf
etell(N:0)
cex
cnp
olk
olkn

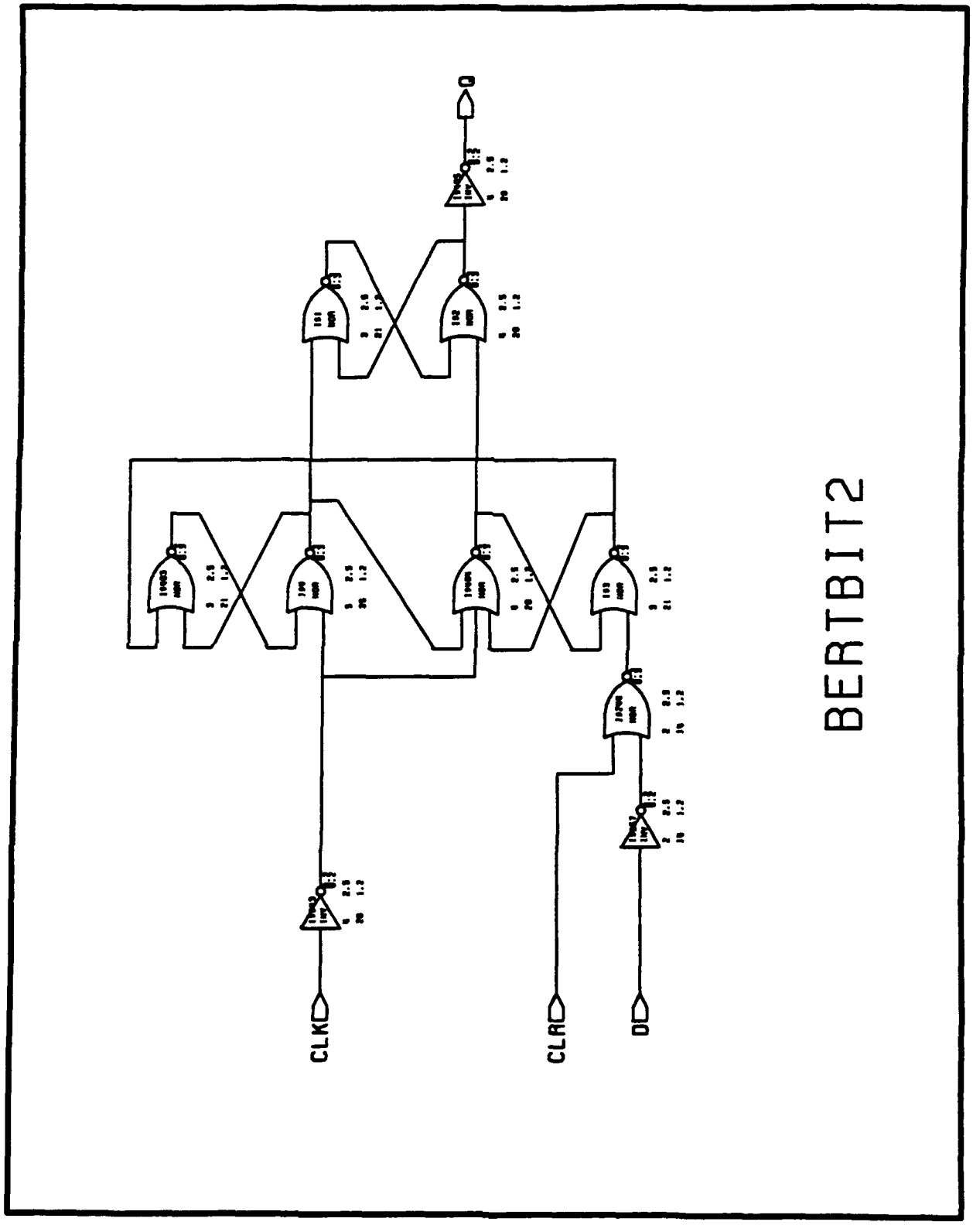

TIC: Sheet 1 of 2
U1
TAP
U2
MPYINT
U3
RSTBUF
U4
SYSCLK
U5
REG56
TICCTRL (4:0)
TICCTRL (2:0)
BFF (2:0)
BFF3
BITF1
PARD1I
IPA1 (3:0)
MCS1 (5:0)
C11 (4:0)
TDO1
TDOEN1
TDI1 (PA1)
TDI1 (MCS1)
TDI1C11
MC3WAF1 (1:0)
WHDA1 (2:0)
MPYLO1
INITF1 (2:0)
SCLK1 (7:0)
BFTEST1
TDI1
TMS1
TRSTF1
TCLK1
PSELF1
TDOIPA1
TDOMCS1
TDOC11
CHP1
CHOCLAF1
TEST1
STALL1 (1:0)
CEX1
CLK1
CLAF1
HSYNC1
HCLK1

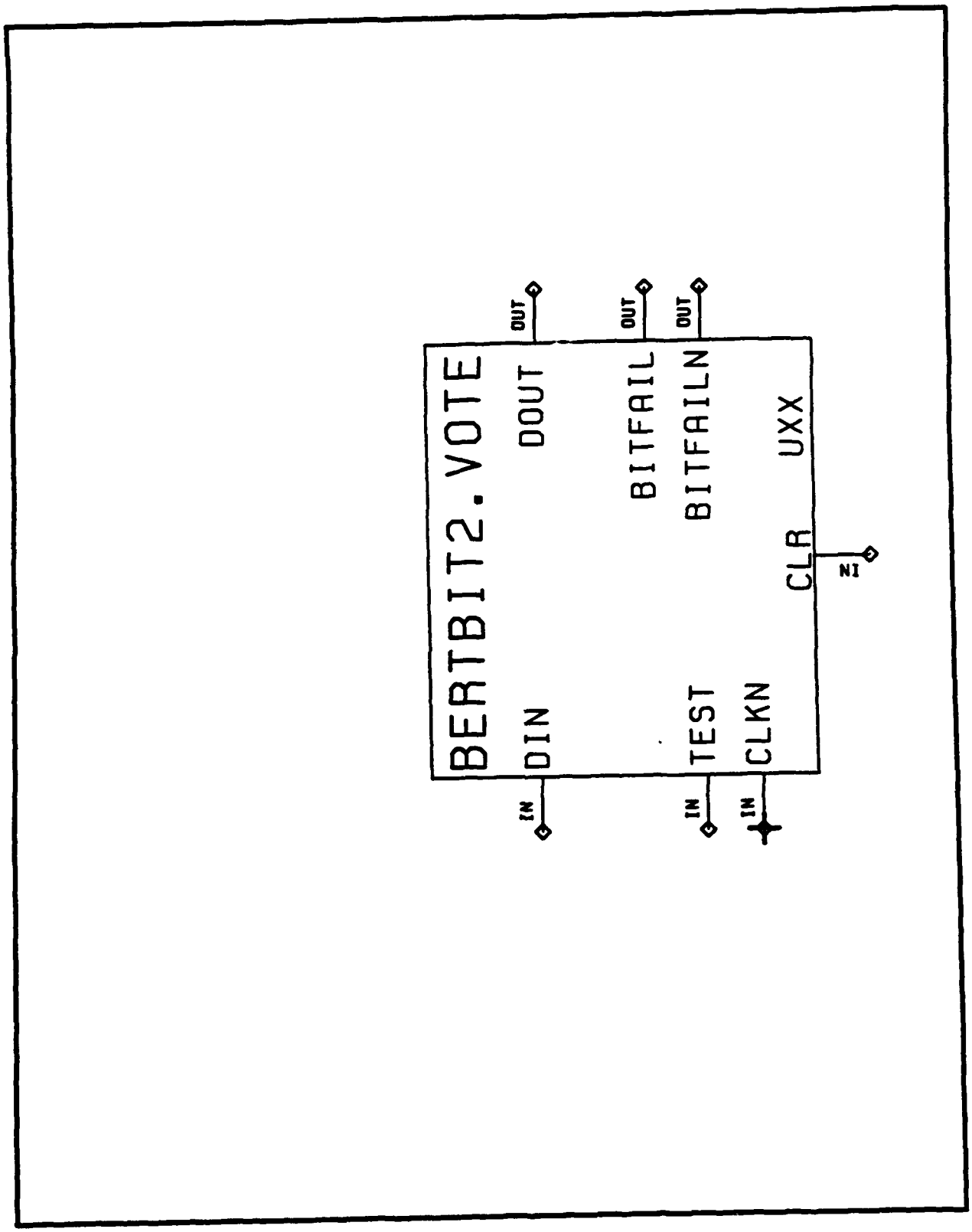

TIC: Sheet 2 of 2
Need single to differential driver for SCLK,SCLKN
PARDIS
SIPINT
NHDR(1)
NPYLD
INITF(1)
SCLK(1)
SCLKN(1)
BF
TDO
TDOEN
TDIIPA
TDIHCS
TDICI
HCS(1)
MCSHNF(1)
MCSHNF(0)
IPA(1)
C1A(1)
C1B(1)
TDI
TMS
TRSTF
TCLK
PSELF
TDOIPA
TDOHCS
TDOCI
CHP
CEX
STALL(1)
MCLK
MSYNC
CHOCLKF
CLKF
CLK
TEST
BFTEST

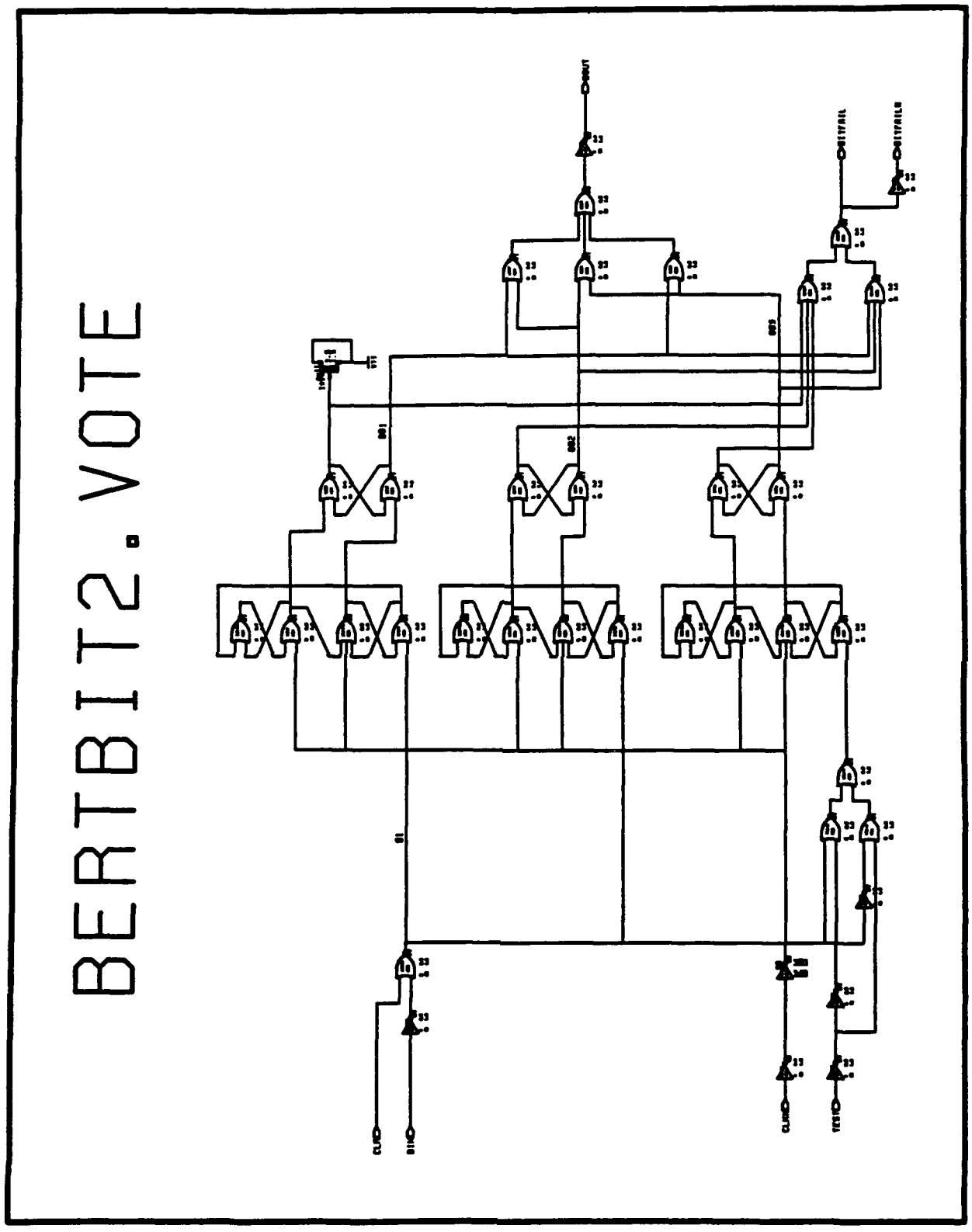

UXX
ALULDBIT
OUT
Q
SET
NI
D
CLK
IN
IN

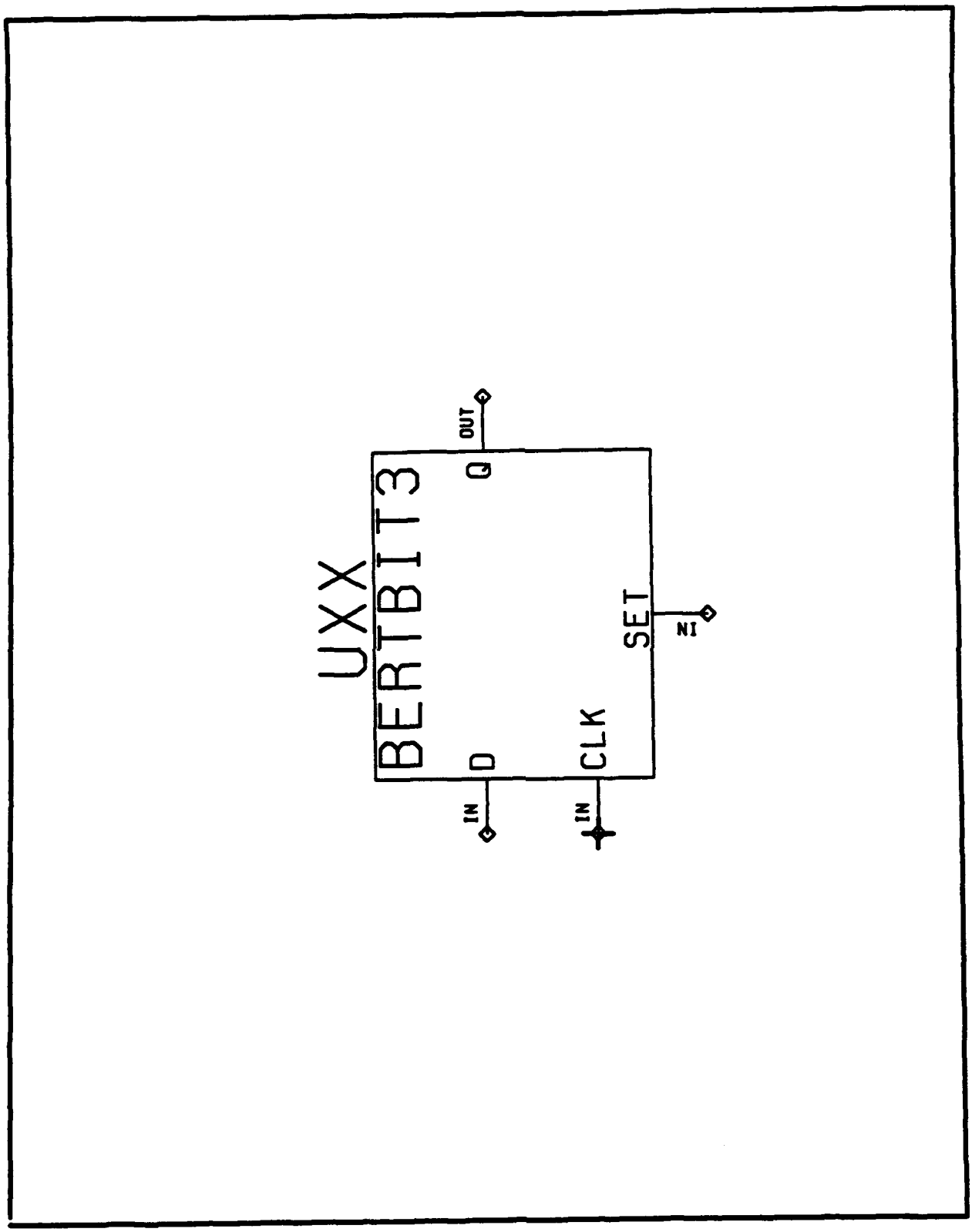

ALULDBIT: FALLING EDGE TRIGGERED
CLK
SET
D

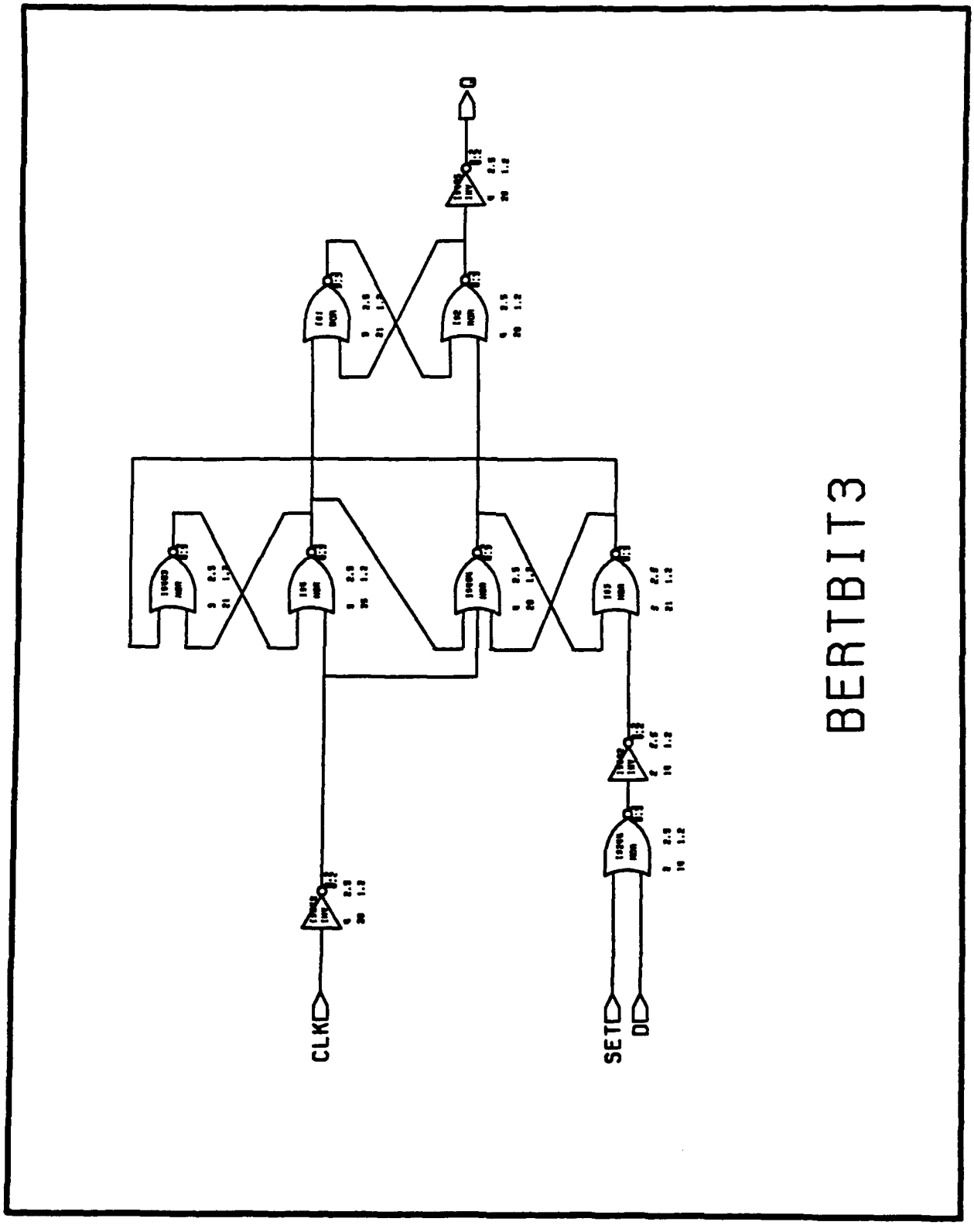

UXX
BERBIT2
OUT
Q
CLR
NI
D
CLK
IN
IN

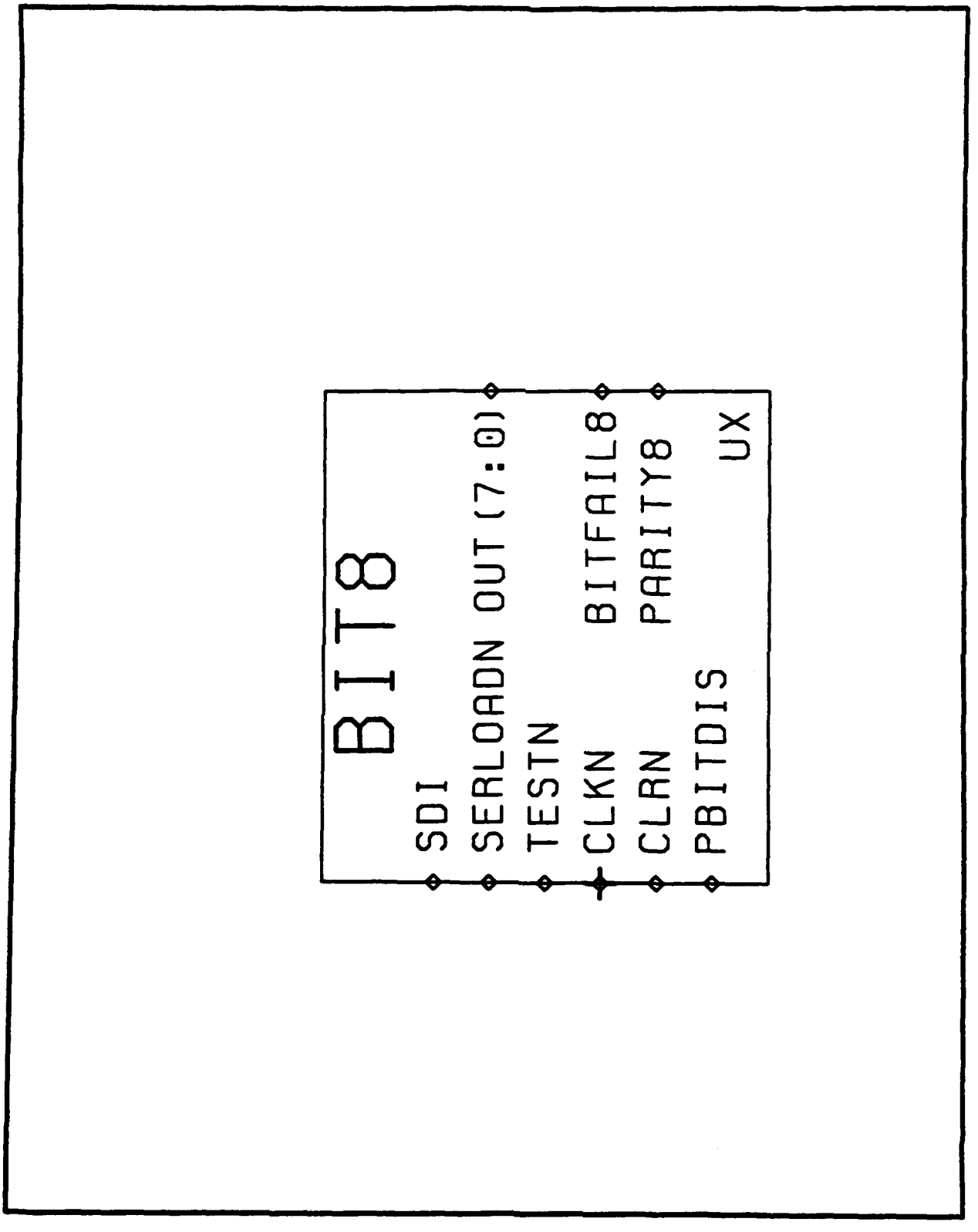

Q
CLK
CLR
D
BERTBIT2

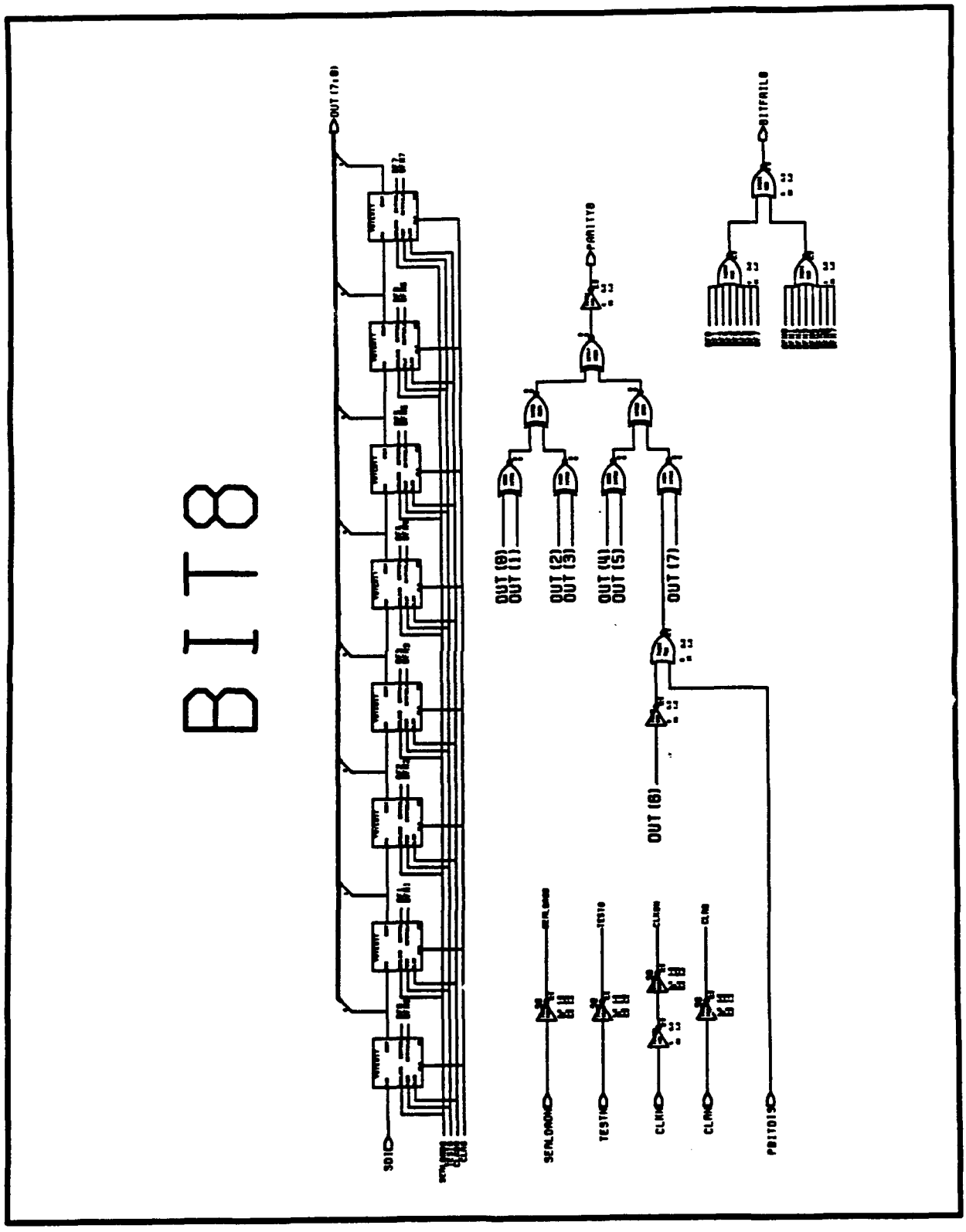

BERTBIT2.VOTE
DOUT
BITFAIL
BITFAILN
UXX
CLR
DIN
TEST
CLKN
OUT
OUT
OUT
NI
IN
IN
IN

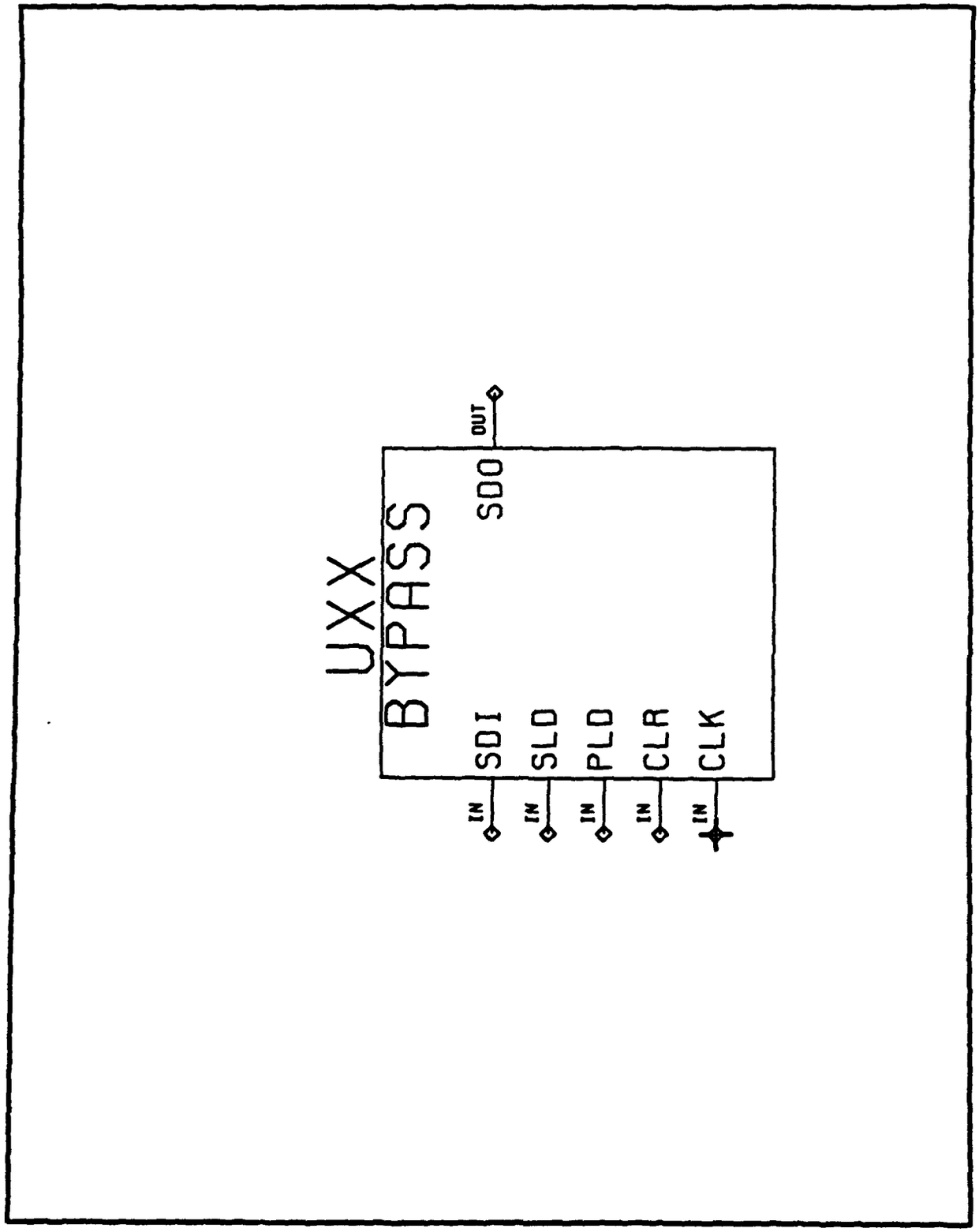

BERTBIT2.VOTE

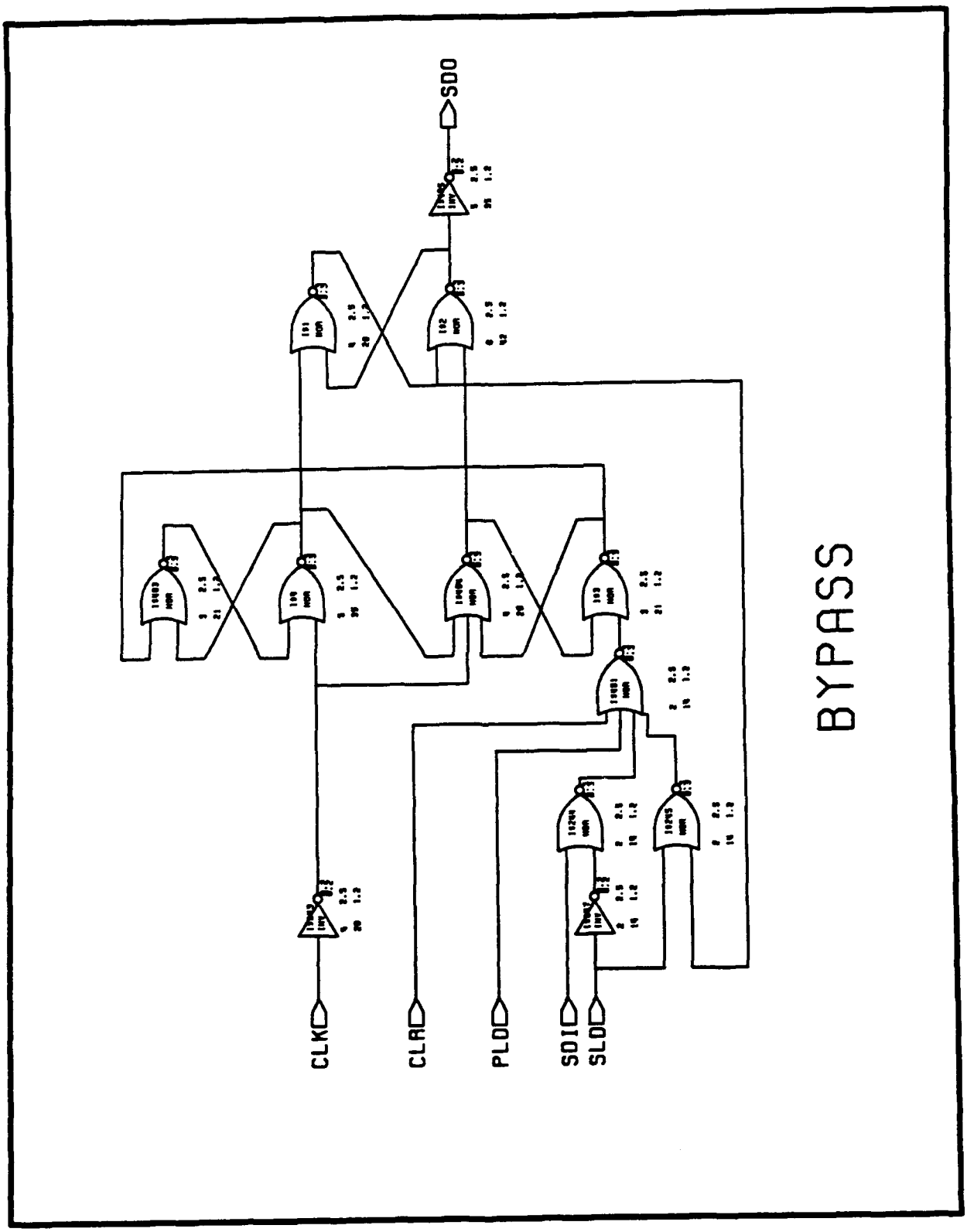

UXX
BERTBIT3
OUT
Q
SET
NI
D
CLK
IN
IN

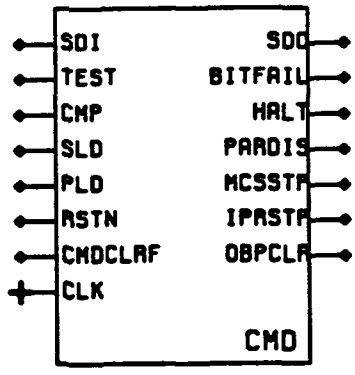

Q
CLK
SET
D
BERTBIT3

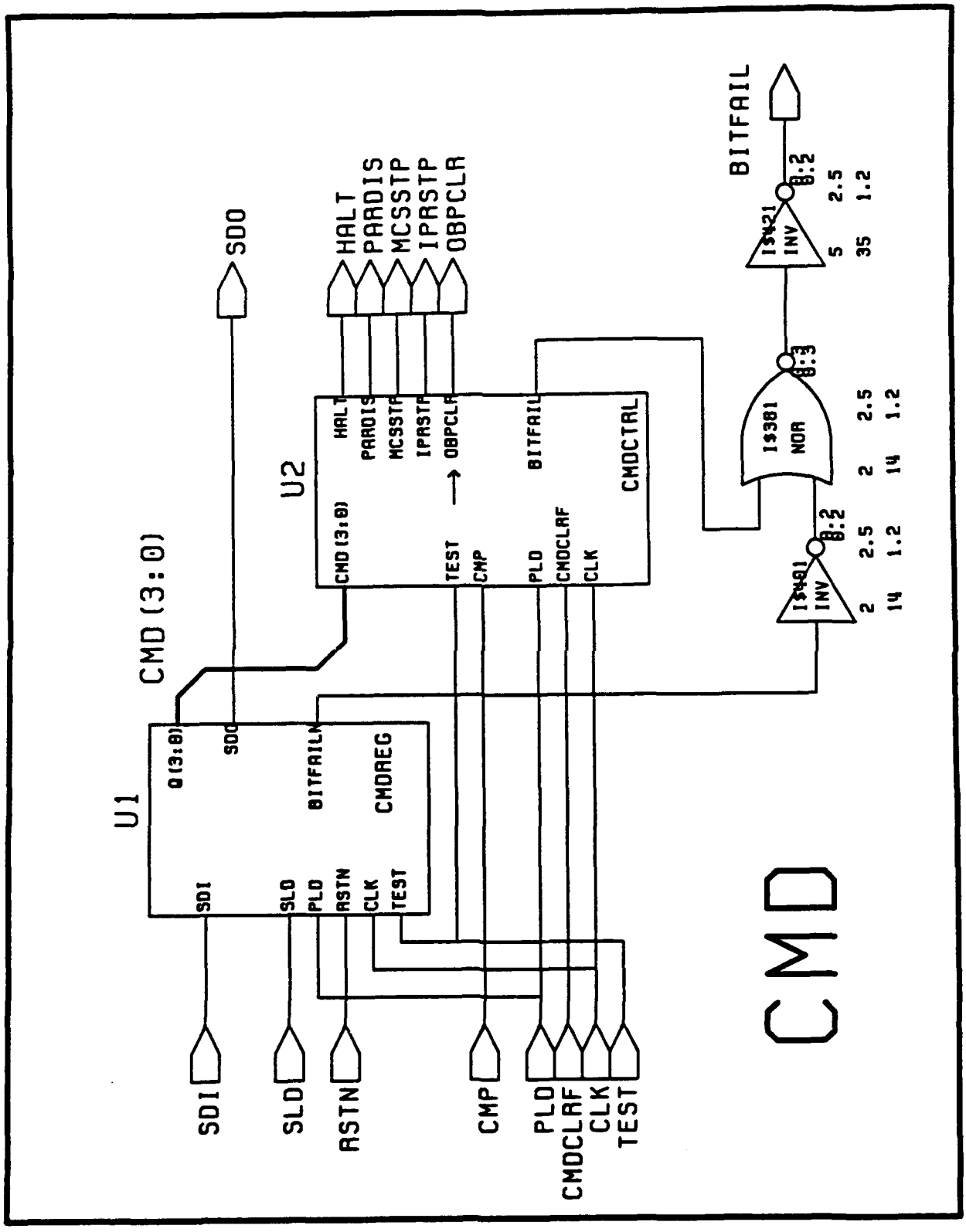

BIT8
SDI
SERLOADN
OUT(7:0)
TESTN
CLKN
BITFAIL8
CLRN
PARITY8
PBITDIS
UX

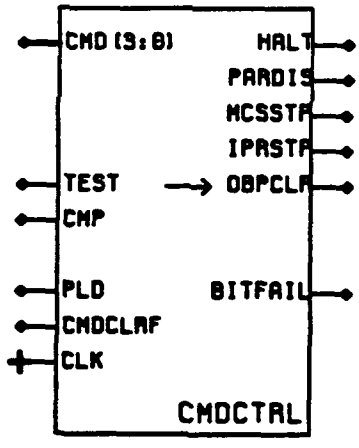

BIT8
OUT (0)
OUT (1)
OUT (2)
OUT (3)
OUT (4)
OUT (5)
OUT (7)
OUT (6)
SDIO
SCLK
SERLOAD
TESTIO
CLKIN
CLKIO
PBITOIS

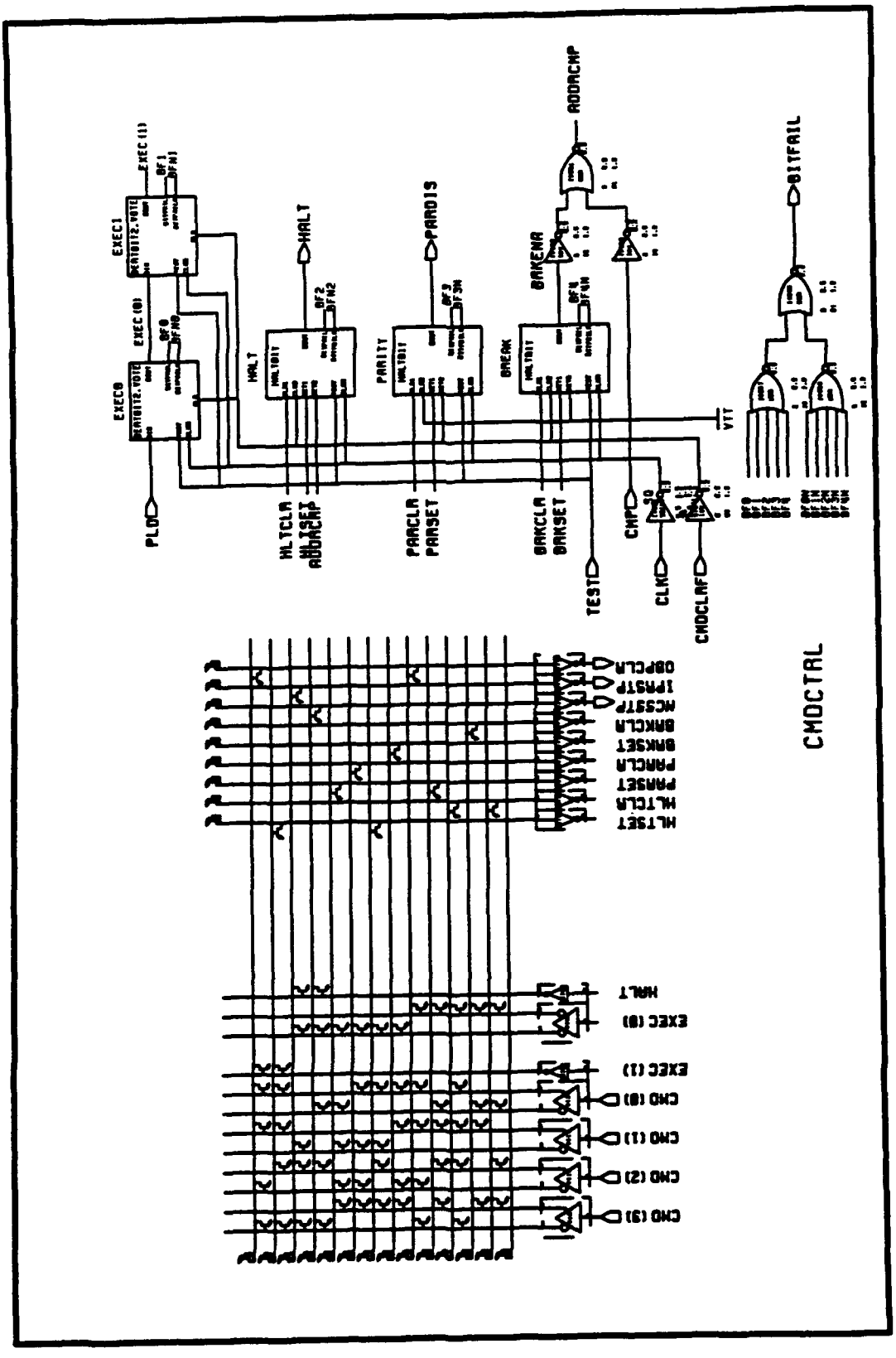

UXX
BYPASS
OUT
SDO
SDI
SLD
PLD
CLR
CLK
IN
IN
IN
IN
IN

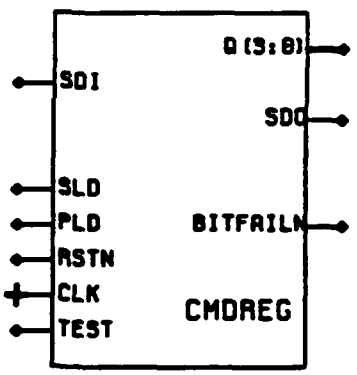

SDO
BYPASS
CLK
CLR
PLD
SDI
SLD

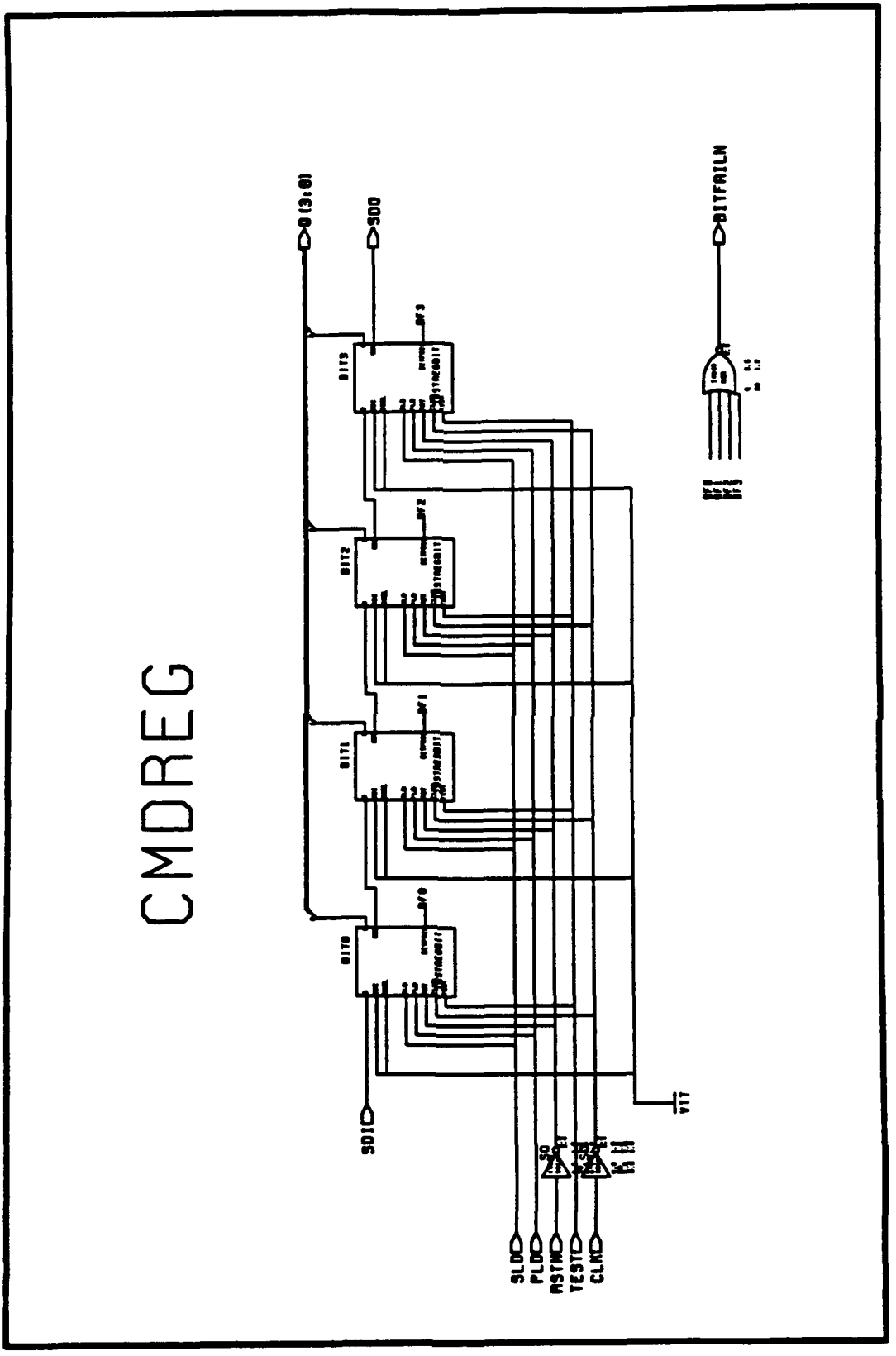

SDI
TEST
CMP
SLD
PLD
RSTN
CMDCLRF
CLK
SDO
BITFAIL
HALT
PARDIS
MCSSTR
IPRSTR
OBPCLR
CMD

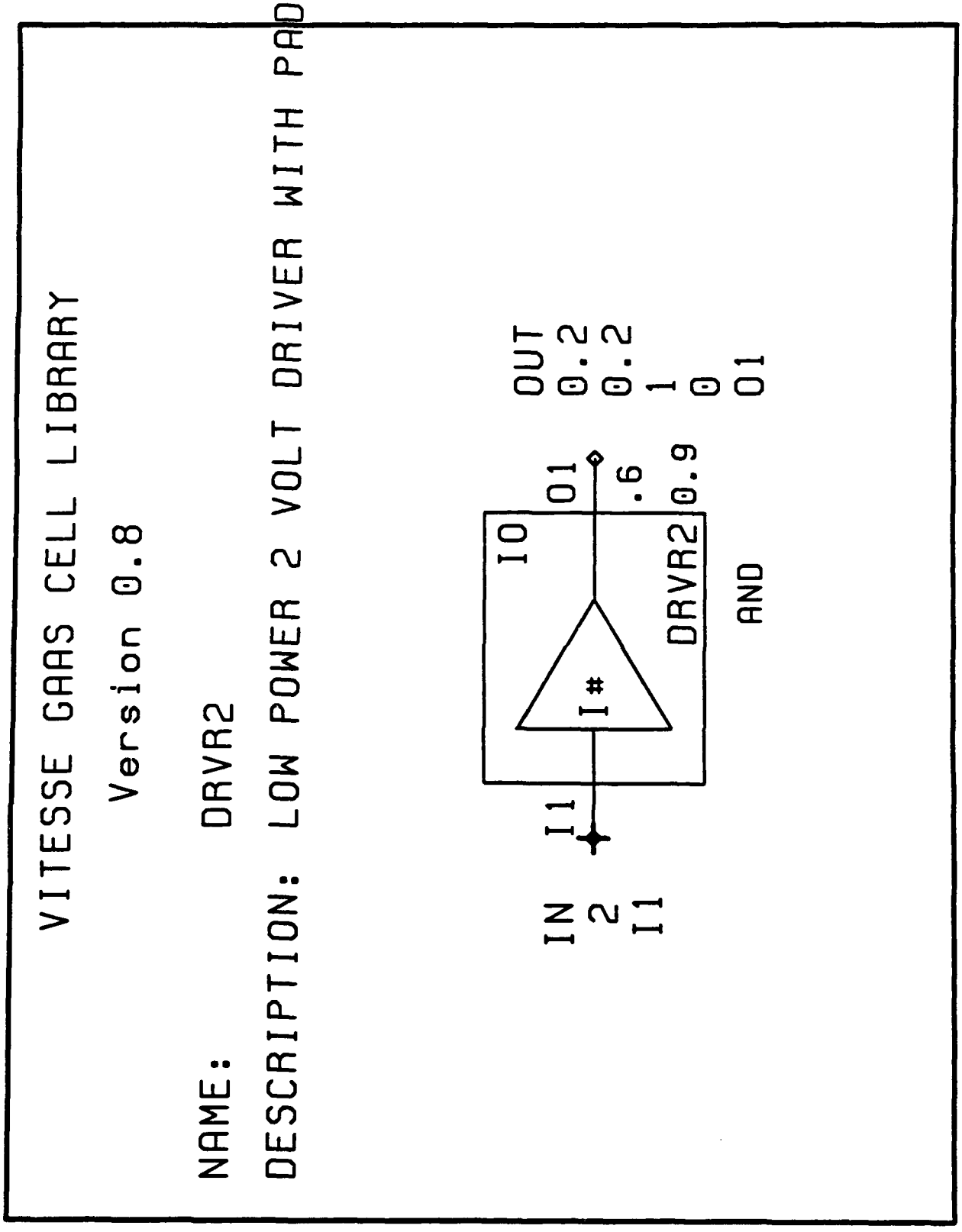

CMD
U1
U2
CMD(3:0)
SDO
HALT
PARDIS
MCSSTP
IPRSTP
OBPCLR
BITFAIL
CMDCTRL
CMDREG
SDI
SLD
RSTN
CMP
PLD
CMDCLRF
CLK
TEST
I$381
NOR
INV

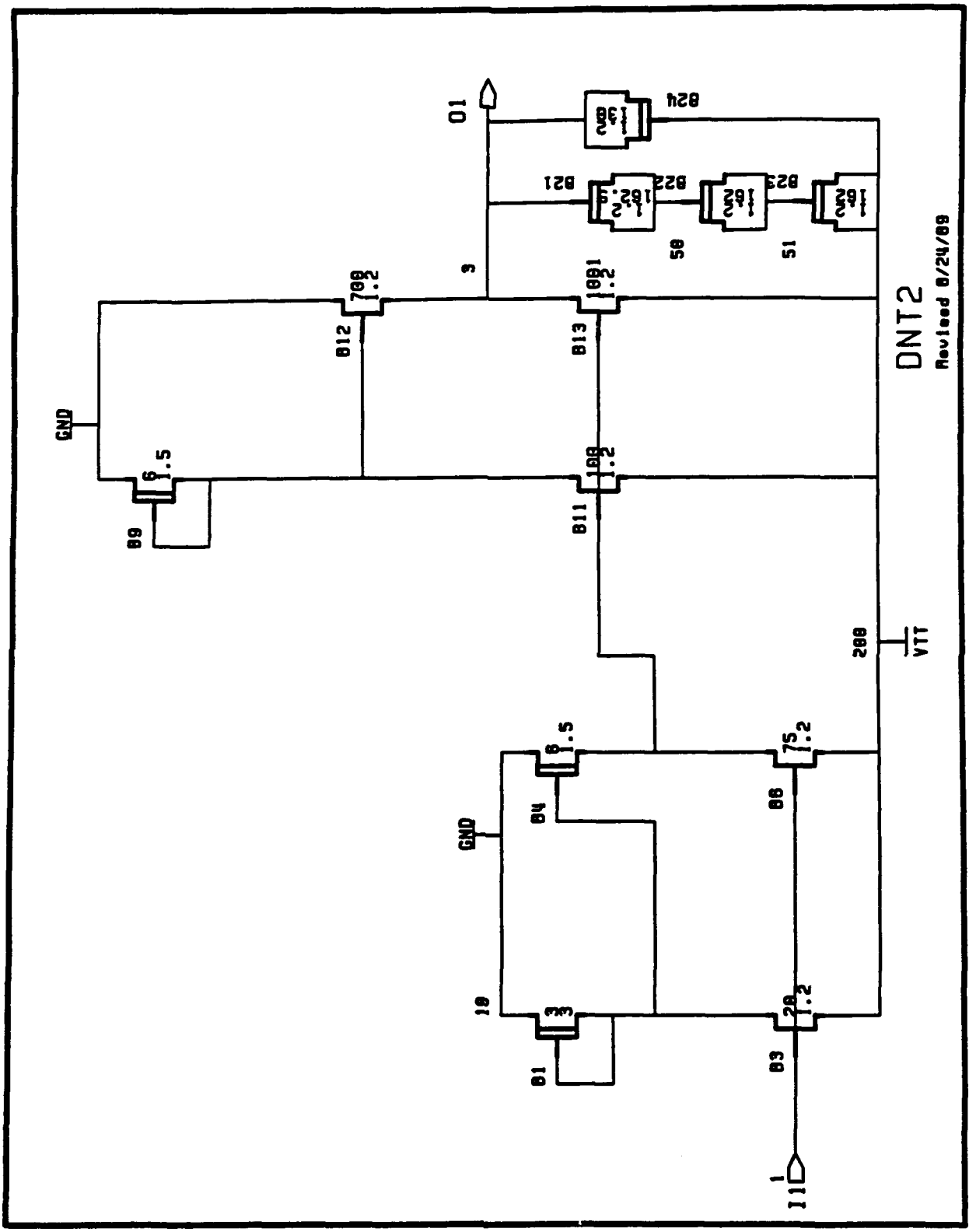

CMD(3:0)
HALT
PARDIS
MCSSTR
IPRSTR
TEST
OBPCLR
CMP
PLD
BITFAIL
CMDCLRF
CLK
CMDCTRL

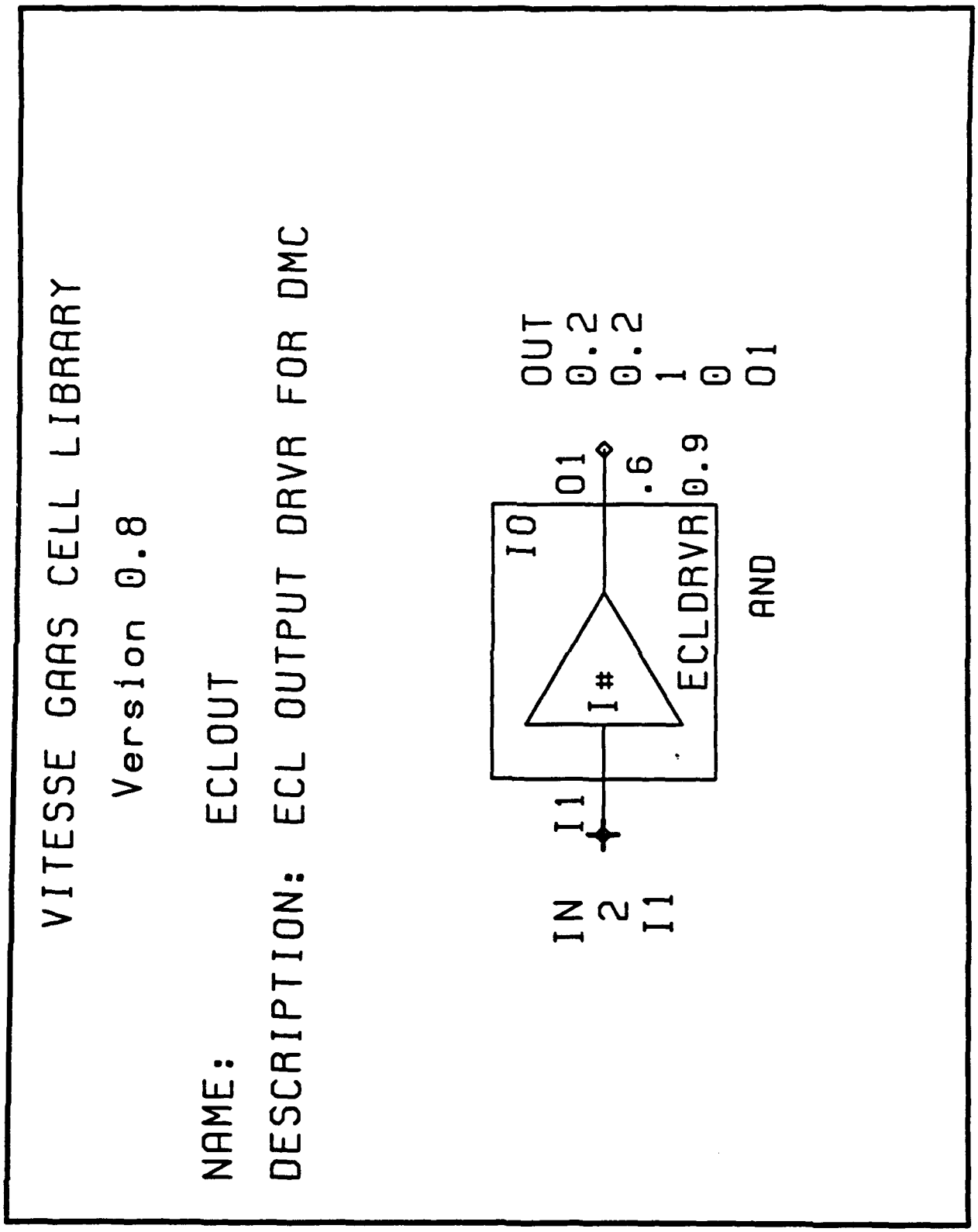

ADDRCMP
BITFAIL
HALT
PARDIS
BRKENA
EXEC1
EXEC0
HALT
PARITY
BREAK
VTT
PLD
HLTCLR
HLTSET
ADDRCMP
PARCLR
PARSET
BRKCLR
BRKSET
TEST
CMP
CLK
CMDCLRF
CMDCTRL
HLTSET
HLTCLR
PRMSET
PRRCLR
BRKSET
BRKCLR
MCSSTP
IPRSTP
OBPCLR
HALT
EXEC (0)
EXEC (1)
CMD (0)
CMD (1)
CMD (2)
CMD (3)

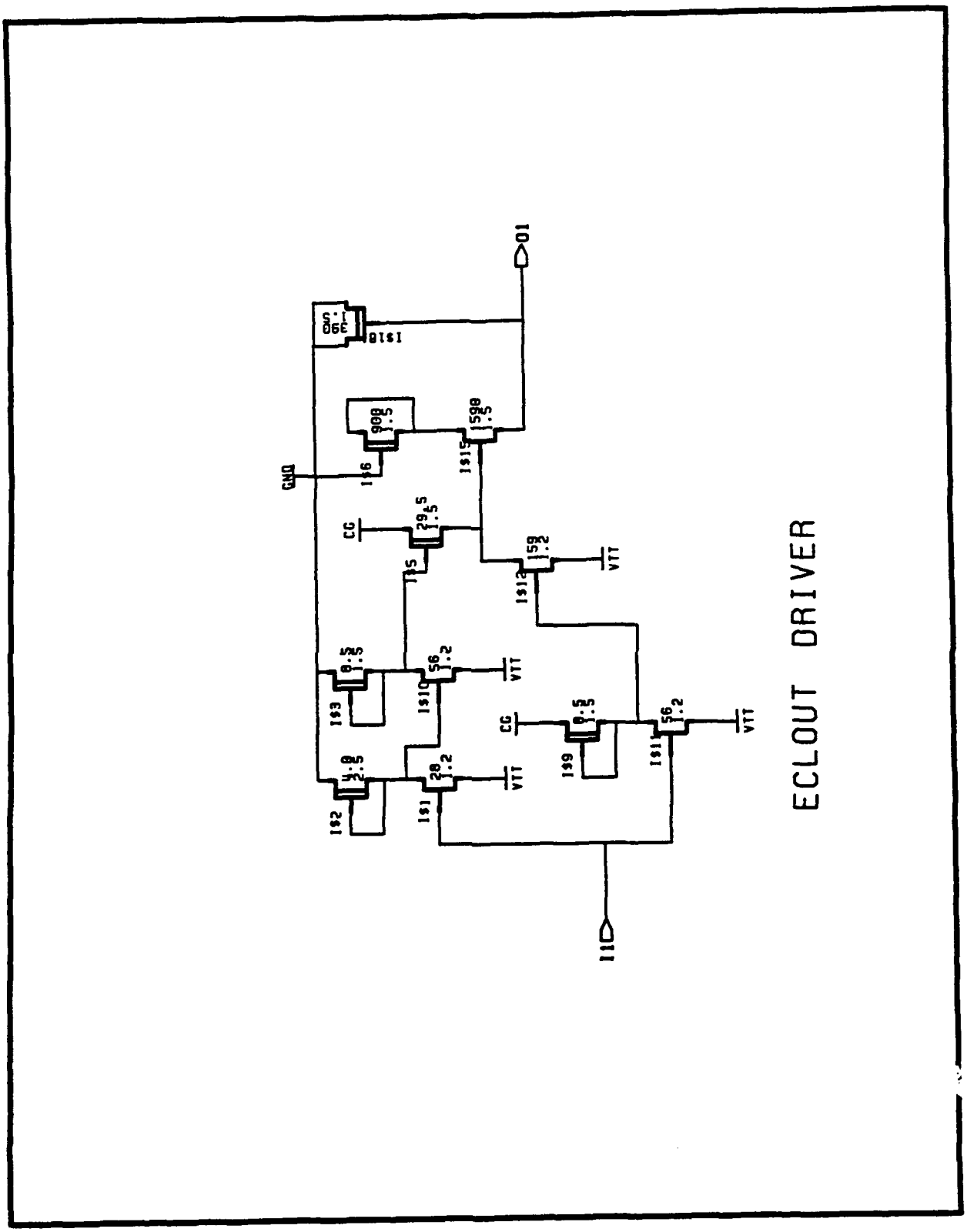

Q(3:0)
SDI
SDO
SLD
PLD
BITFAILN
RSTN
CLK
TEST
CMDREG

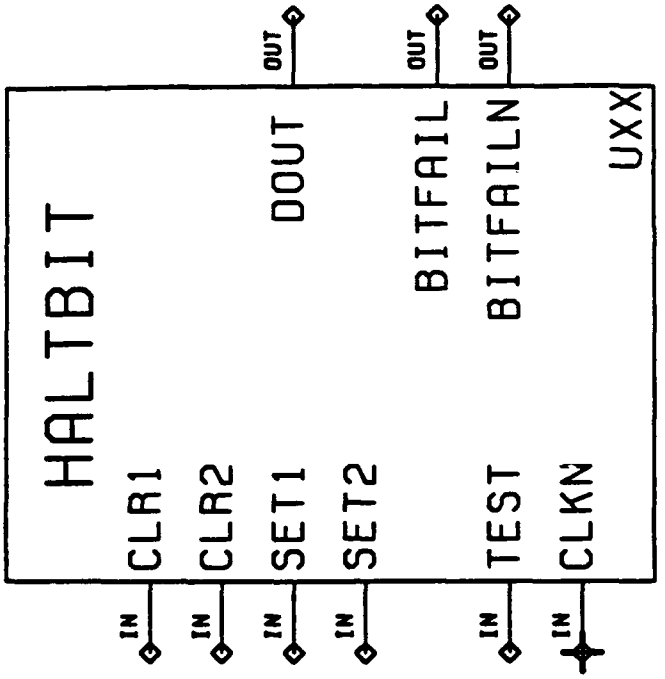

CMDREG
D(3:0)
SDO
BITFAILN
SDI
SLOC
PLOC
RSTMC
TESTC
CLKC

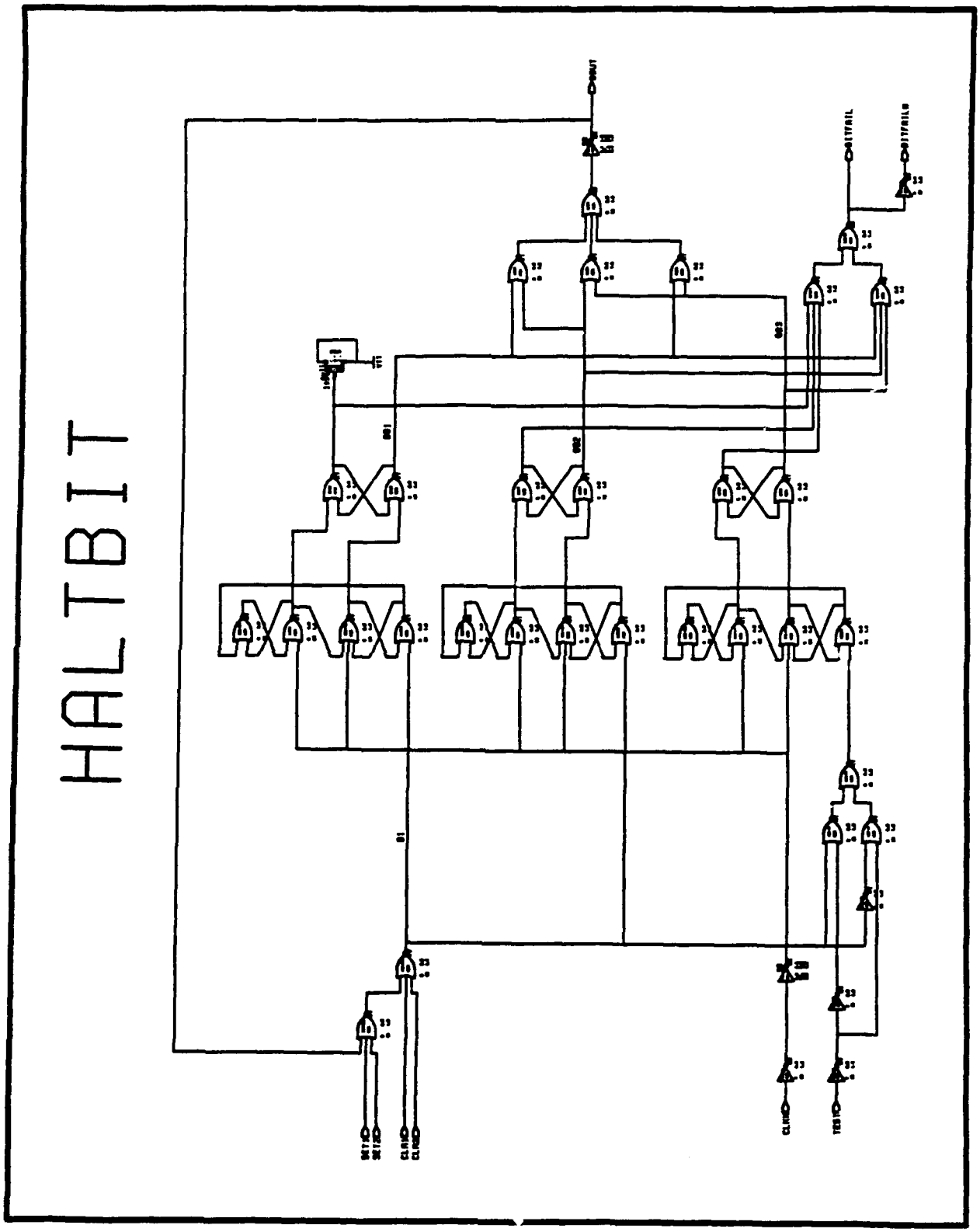

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: DRVR2
DESCRIPTION: LOW POWER 2 VOLT DRIVER WITH PAD
IN
2
I1
I1
IO
O1
I#
.6
DRVR2
0.9
OUT
0.2
0.2
1
0
O1
AND

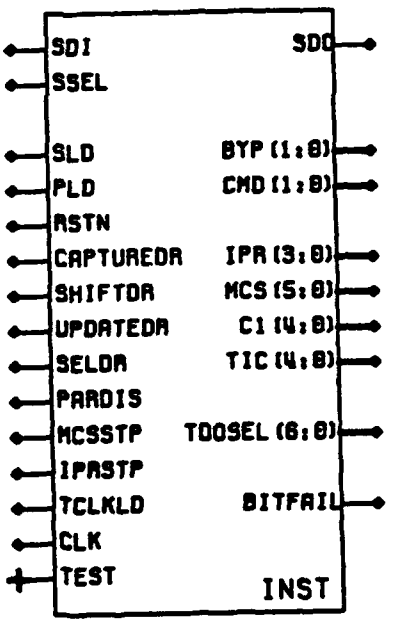

DNT2
Revised 8/24/89
GND
VTT
I1
I0
B1
B3
B4
B6
B9
B11
B12
B13
B21
B22
B23
B24
50
51
5
10
200

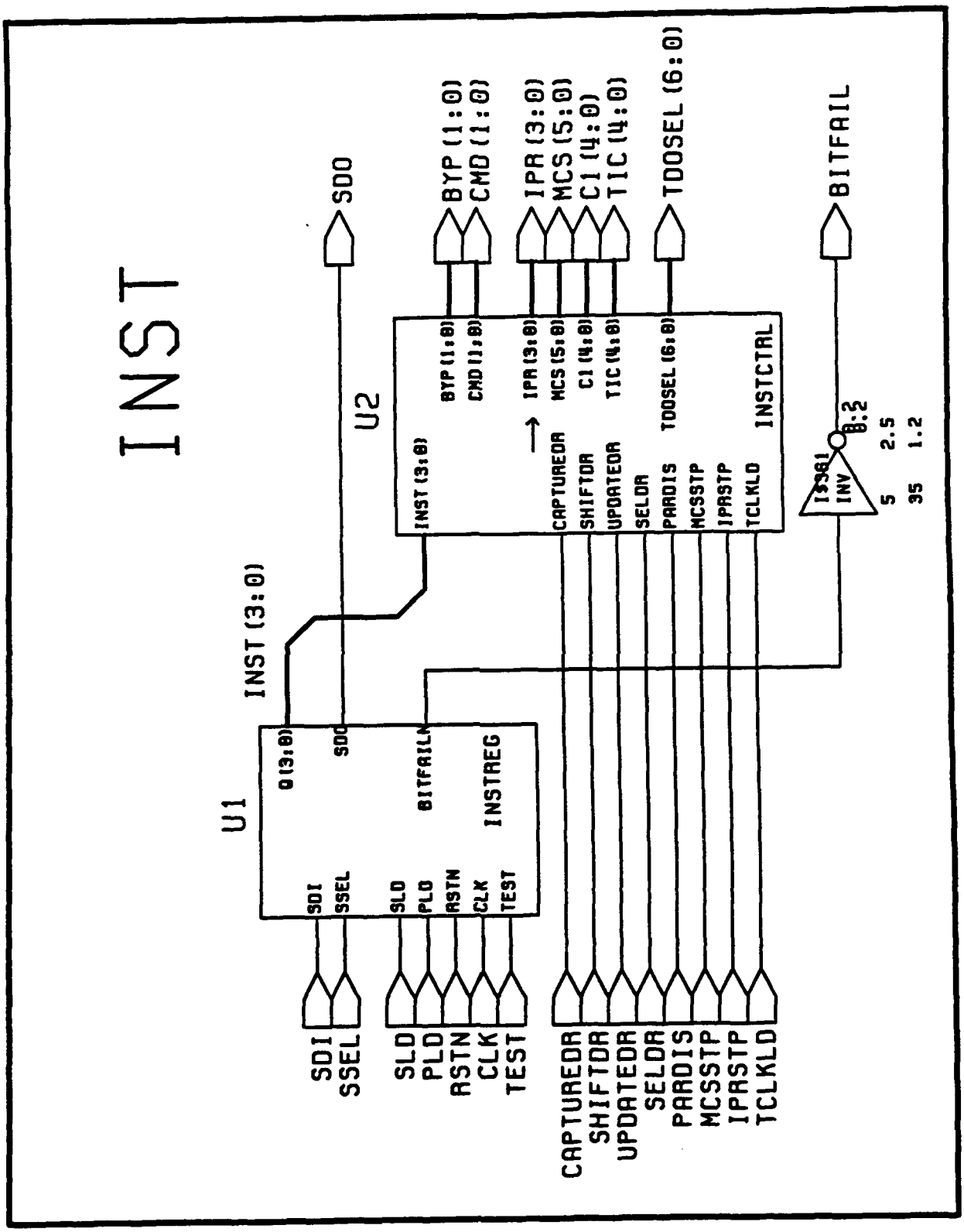

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: ECLOUT
DESCRIPTION: ECL OUTPUT DRVR FOR DMC
IN
2
I1
I1
O1
IO
I#
.6
0.9
ECLDRVR
OUT
0.2
0.2
1
0
O1
AND

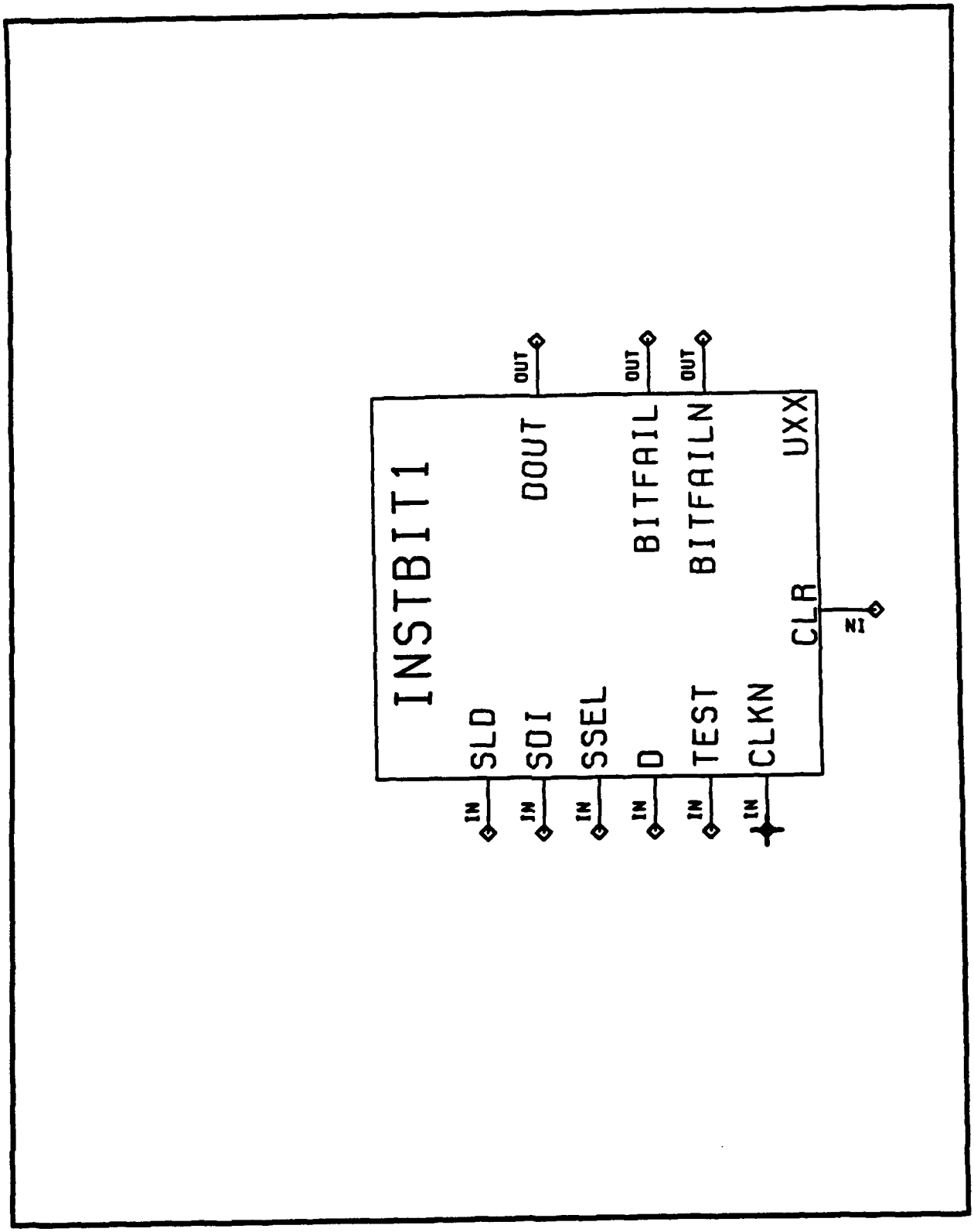

ECLOUT DRIVER
O1
O2
GND
CG
VTT


HALTBIT
CLR1
CLR2
SET1
SET2
TEST
CLKN
DOUT
BITFAIL
BITFAILN
UXX
IN
OUT

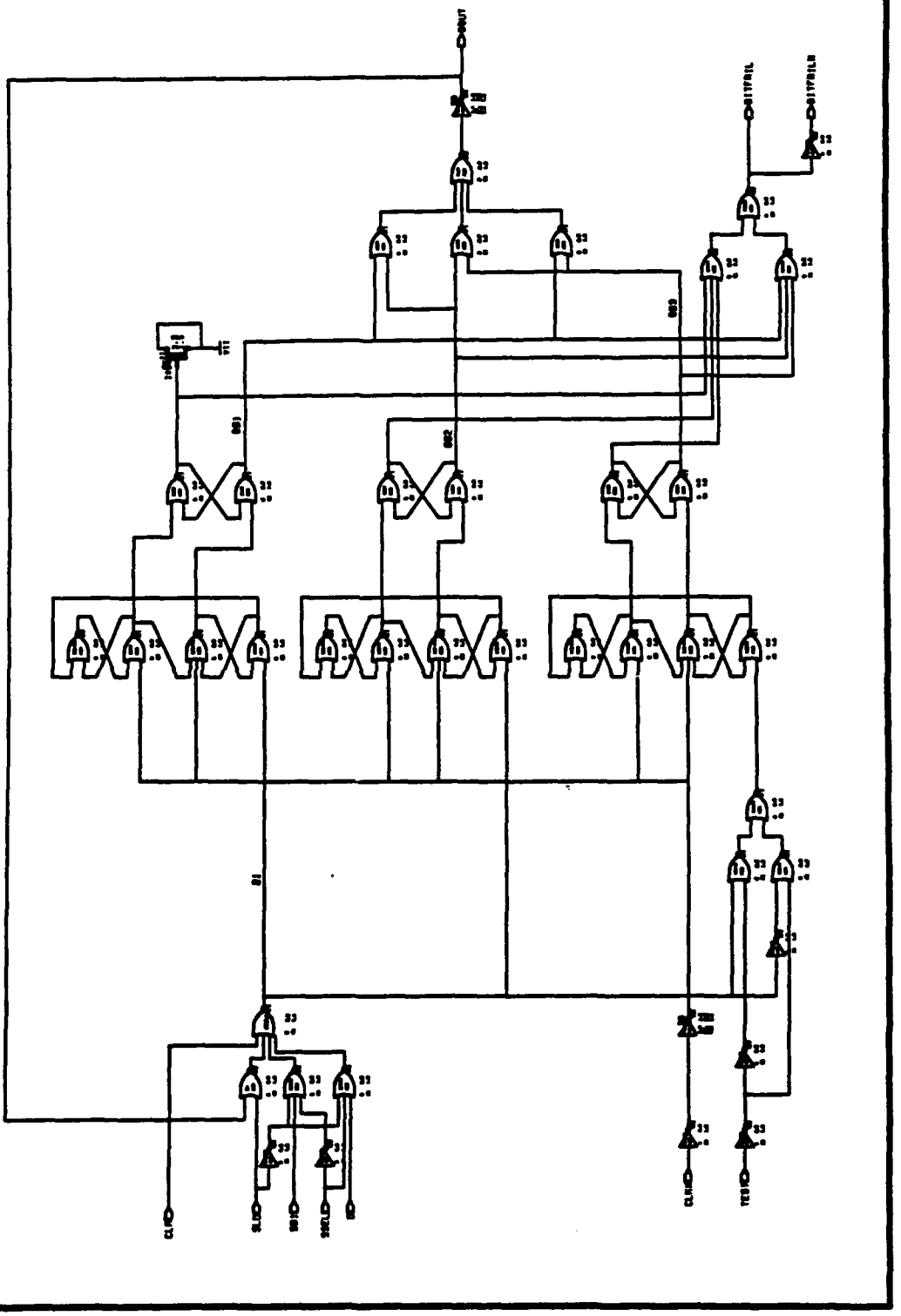

HALTBIT

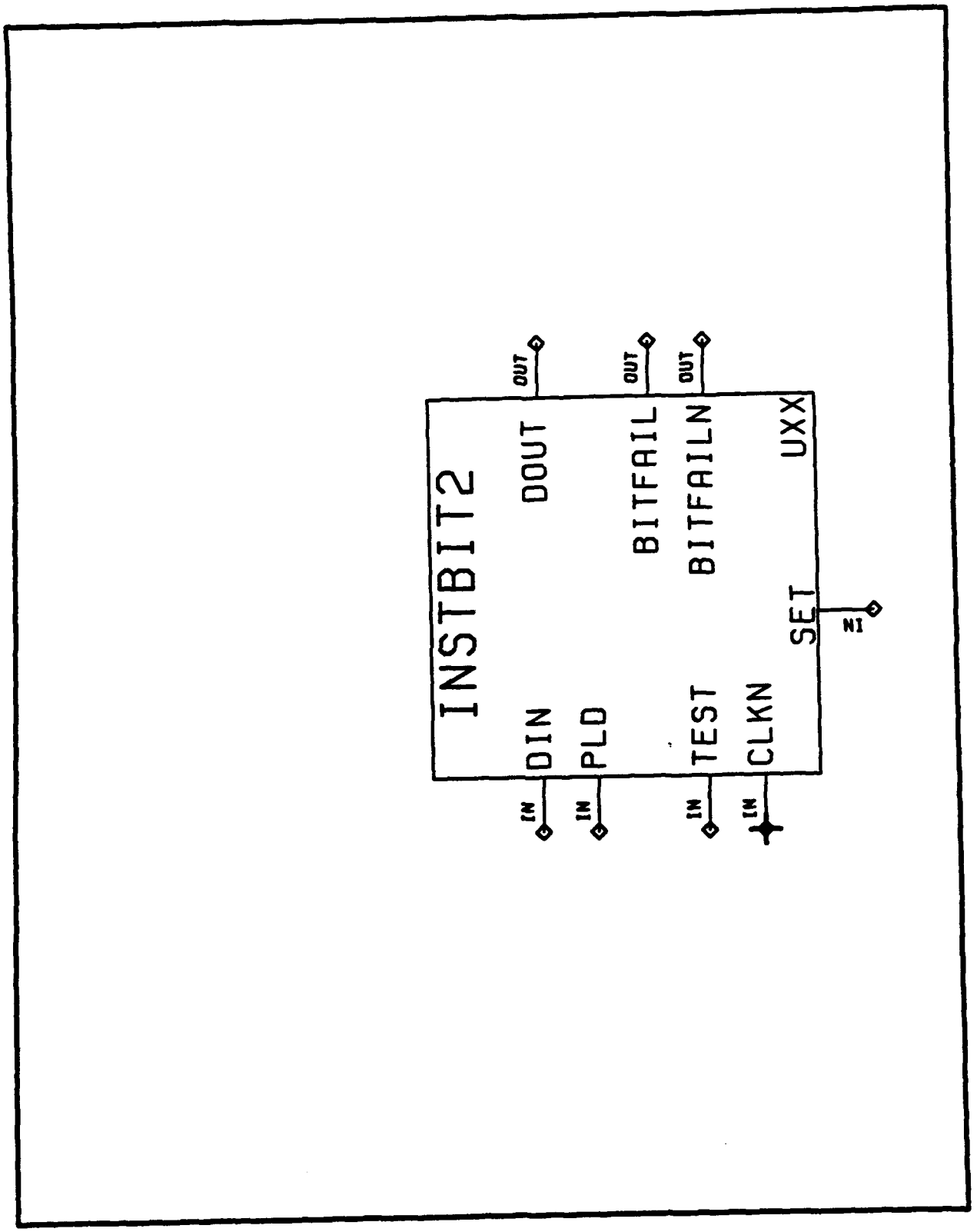

SDI
SSEL
SLD
PLD
RSTN
CAPTUREDR
SHIFTDR
UPDATEDR
SELDR
PARDIS
MCSSTP
IPRSTP
TCLKLD
CLK
TEST
SDO
BYP (1:0)
CMD (1:0)
IPR (3:0)
MCS (5:0)
C1 (4:0)
TIC (4:0)
TDOSEL (6:0)
BITFAIL
INST

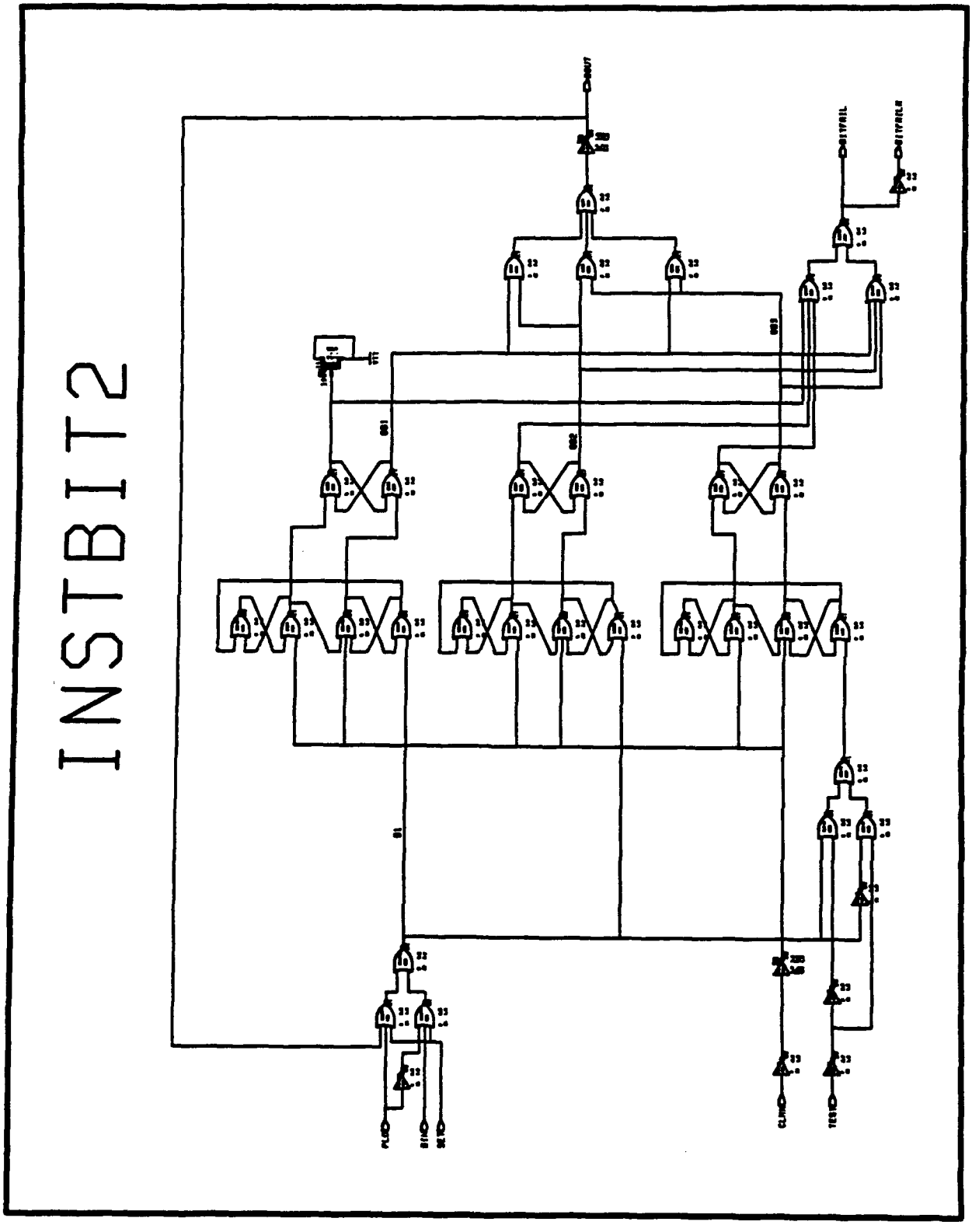

INST
U1
U2
INST(3:0)
SDO
BYP(1:0)
CMD(1:0)
IPR(3:0)
MCS(5:0)
C1(4:0)
TIC(4:0)
TDOSEL(6:0)
BITFAIL
INSTCTRL
INSTREG
SDI
SSEL
SLD
PLD
RSTN
CLK
TEST
CAPTUREDR
SHIFTDR
UPDATEDR
SELDR
PARDIS
MCSSTP
IPRSTP
TCLKLD
INV
8.2
2.5
1.2
5
35

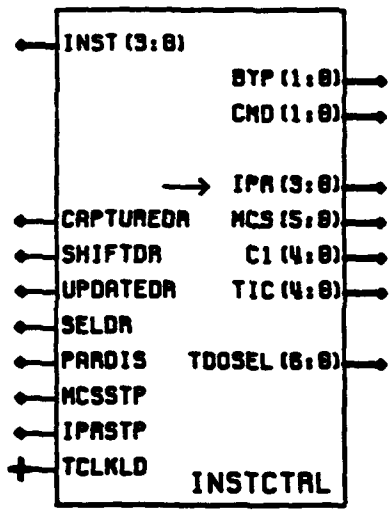

INSTBIT1
DOUT
BITFAIL
BITFAILN
UXX
CLR
SLD
SDI
SSEL
D
TEST
CLKN
OUT
OUT
OUT
IN
IN
IN
IN
IN
IN
NI

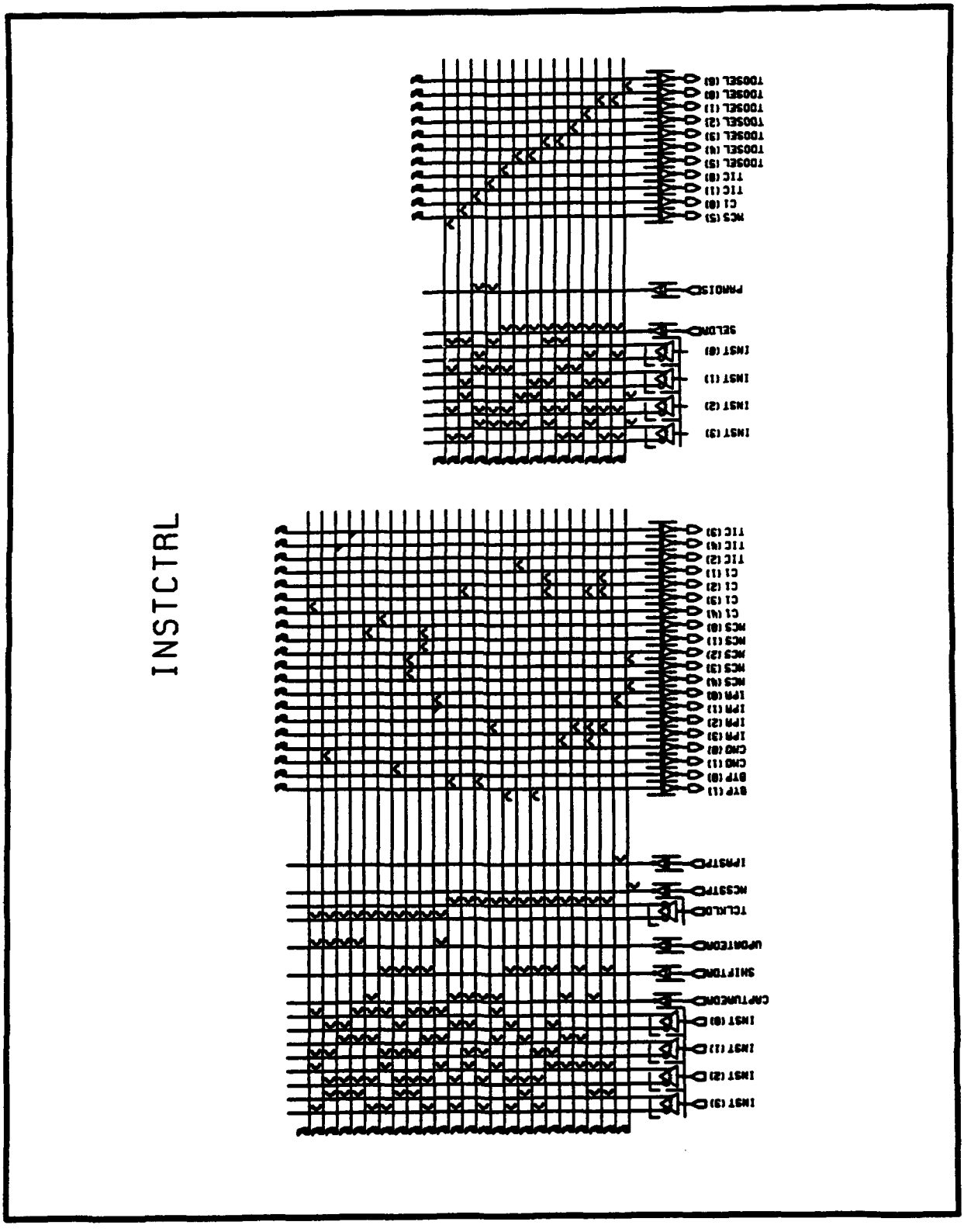
INSTBIT1

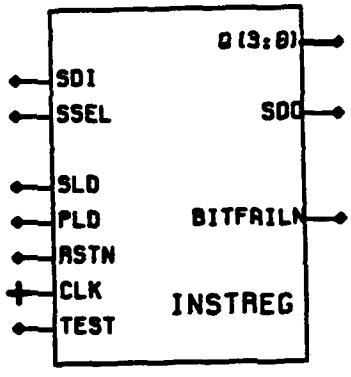


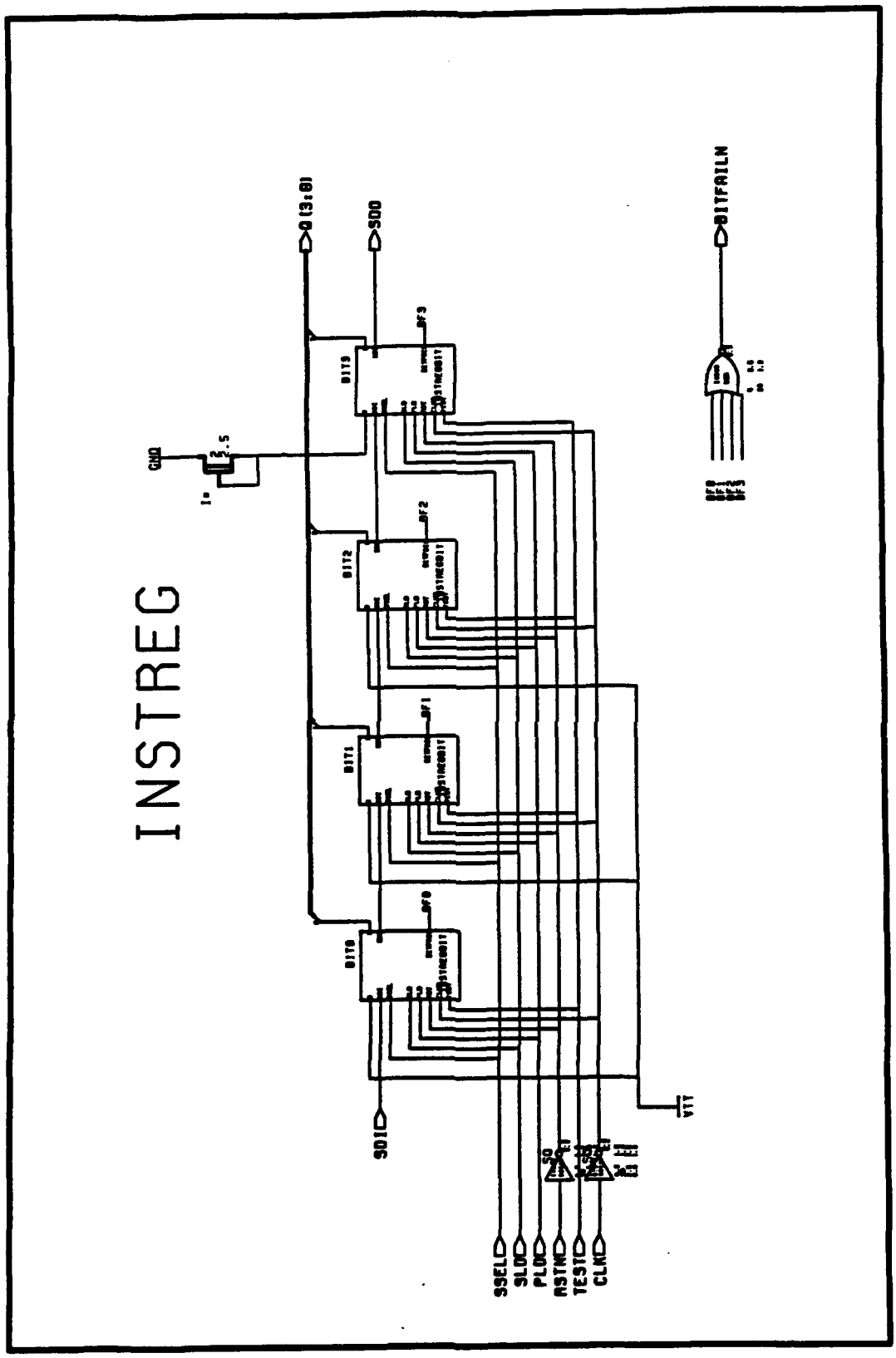

INSTBIT2
DOUT
BITFAIL
BITFAILN
UXX
SET
N1
DIN
PLD
TEST
CLKN
OUT
OUT
OUT
IN
IN
IN
IN

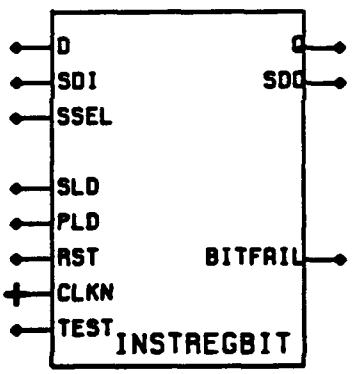

INSTBIT2

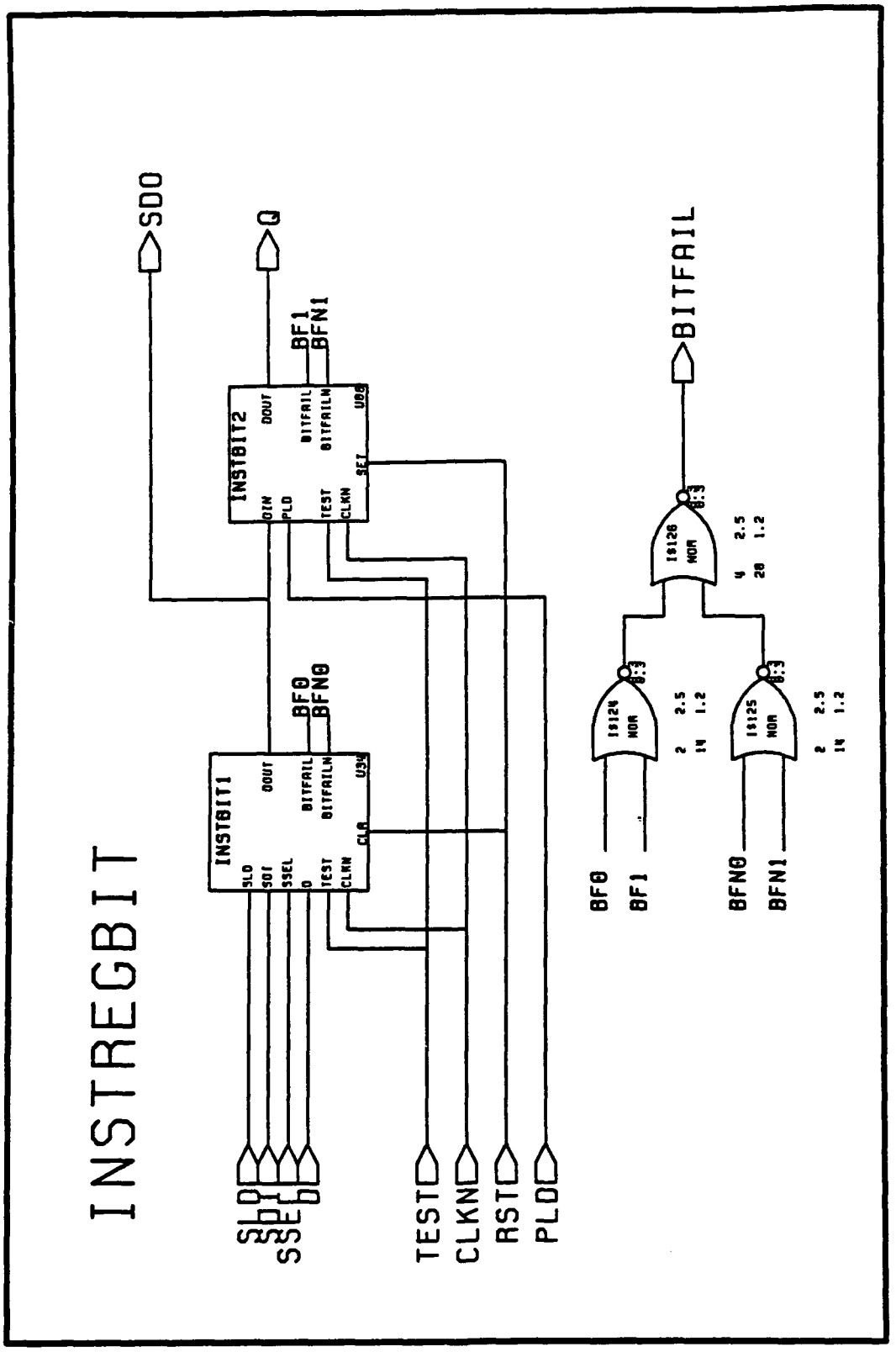

INST (3:0)
BYP (1:0)
CMD (1:0)
IPR (3:0)
CAPTUREDR
MCS (5:0)
SHIFTDR
C1 (4:0)
UPDATEDR
TIC (4:0)
SELDR
PARDIS
TDOSEL (6:0)
MCSSTP
IPRSTP
TCLKLD
INSTCTRL

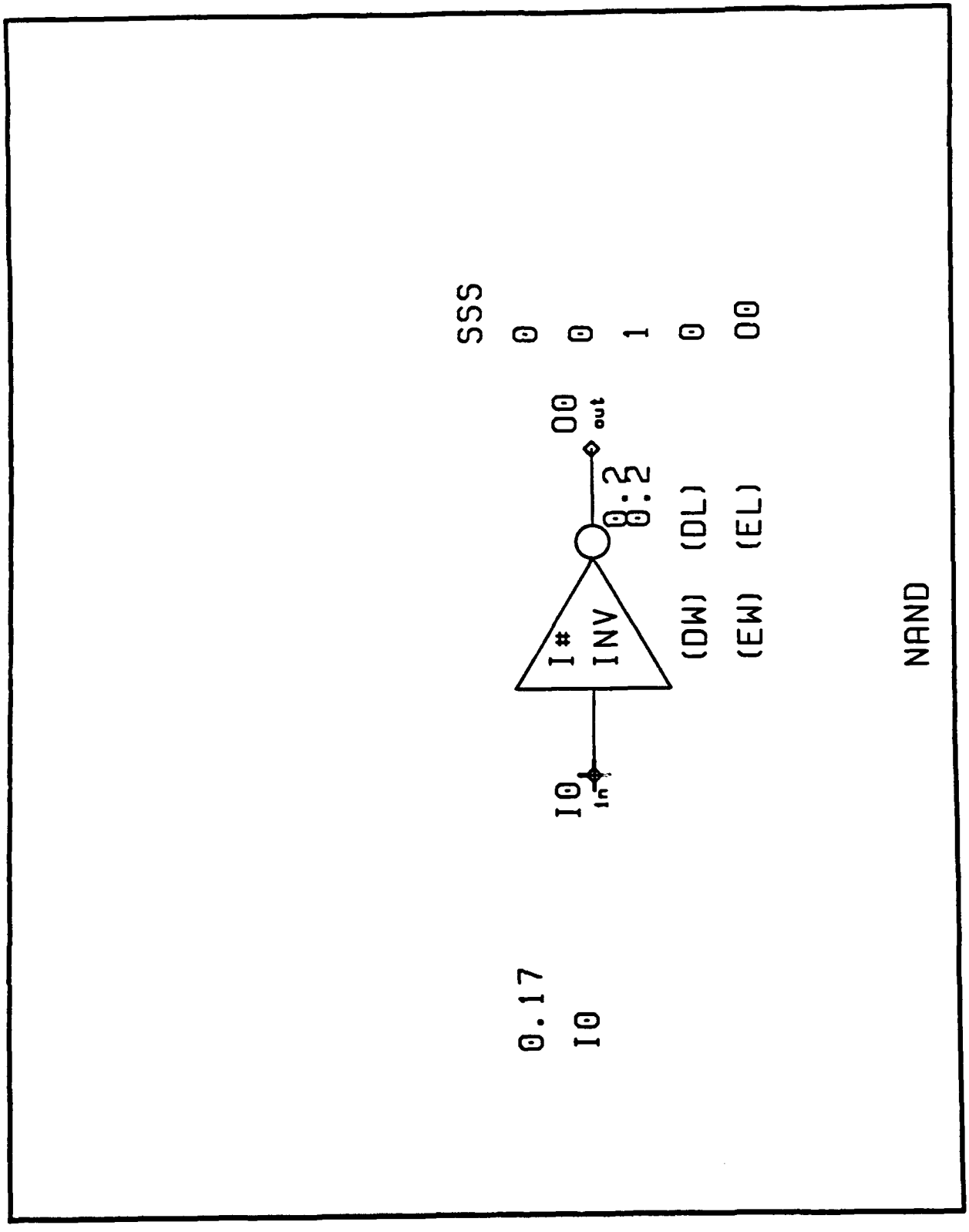

INSTCTRL

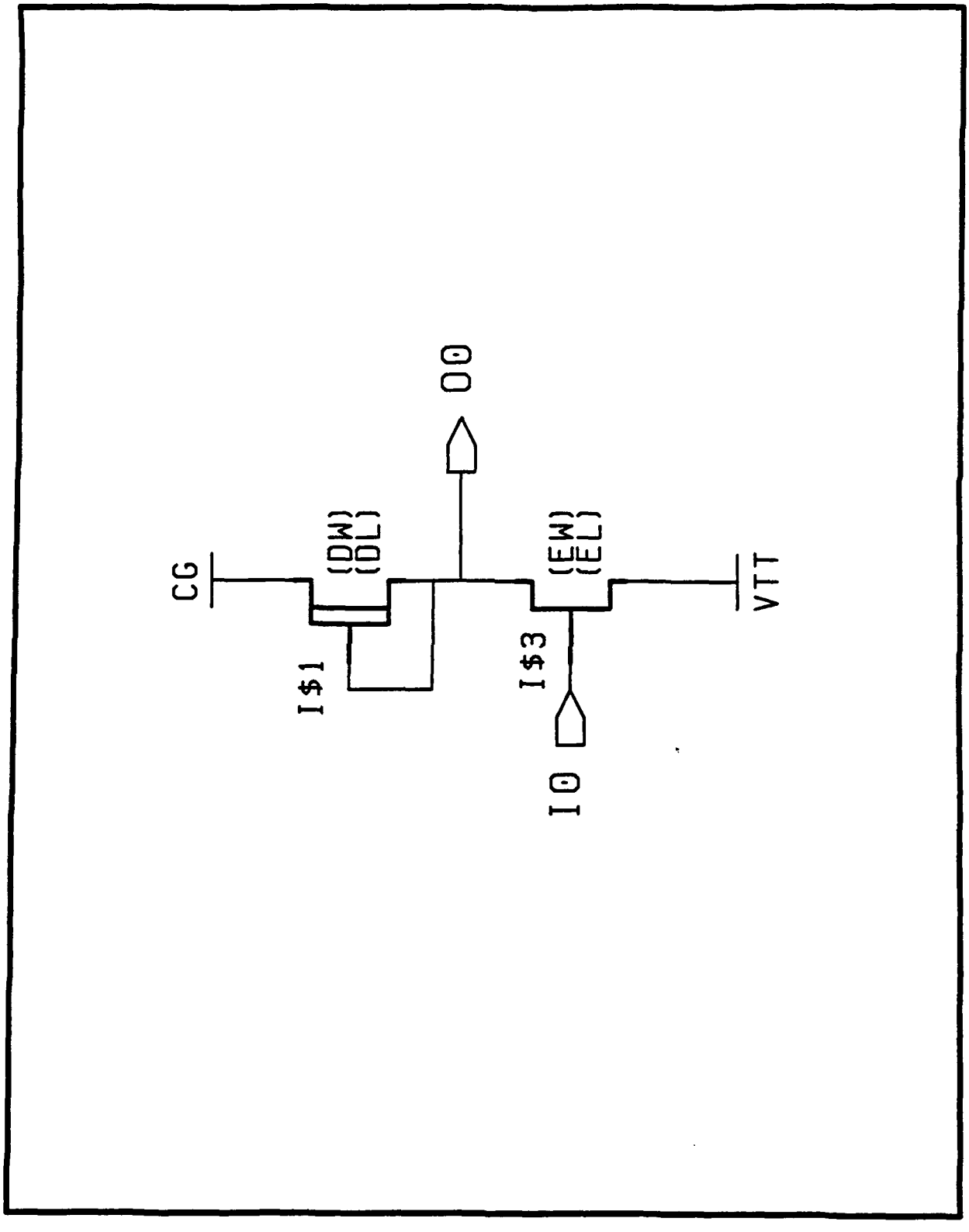

Q(3:0)
SDI
SSEL
SDO
SLD
PLD
BITFAILN
RSTN
CLK
INSTREG
TEST

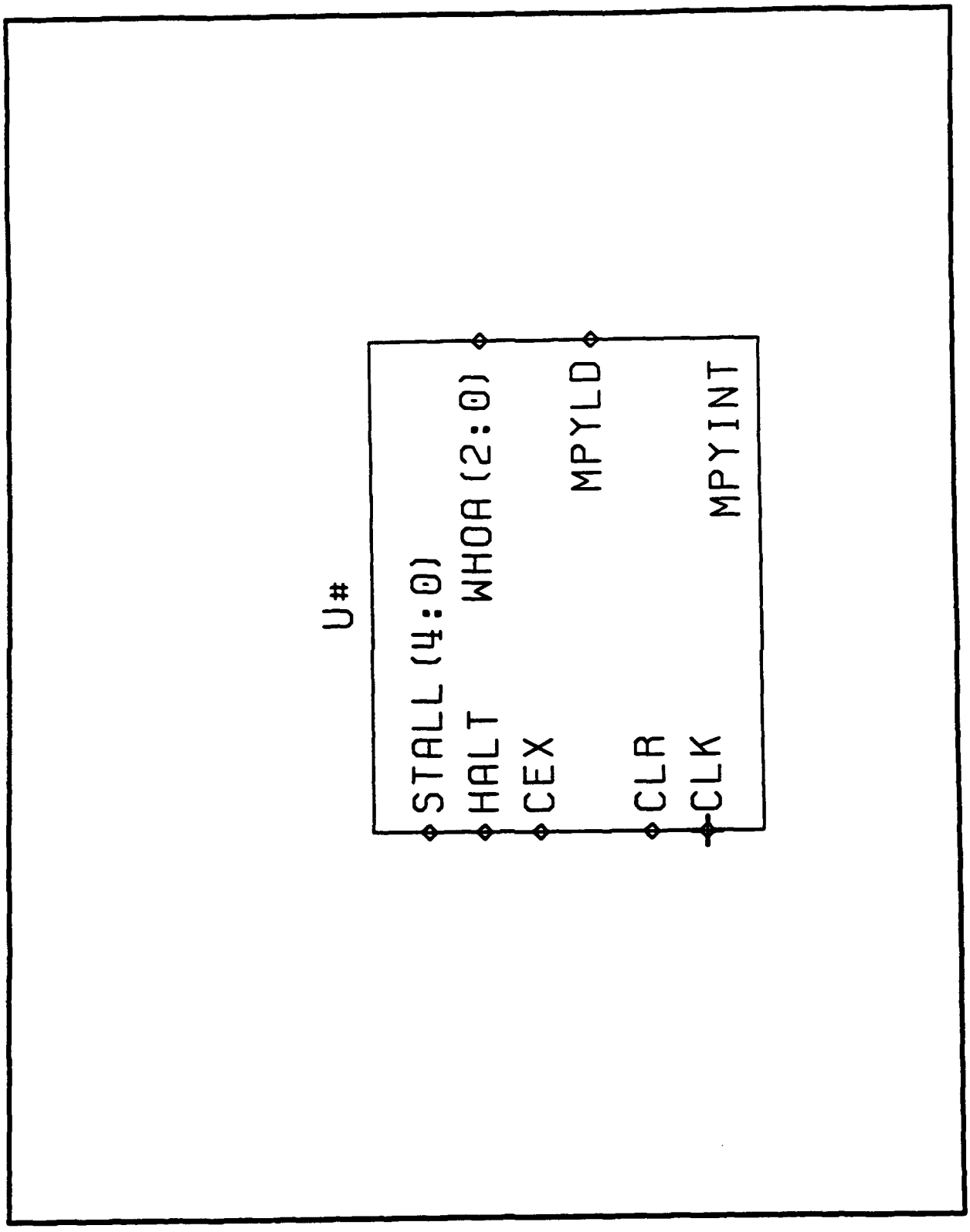

INSTREG
D[3:0]
SDO
BITFAILN
GND
SDI
VTT
SSELD
SLOD
PLOD
RSTMC
TESTC
CLKD

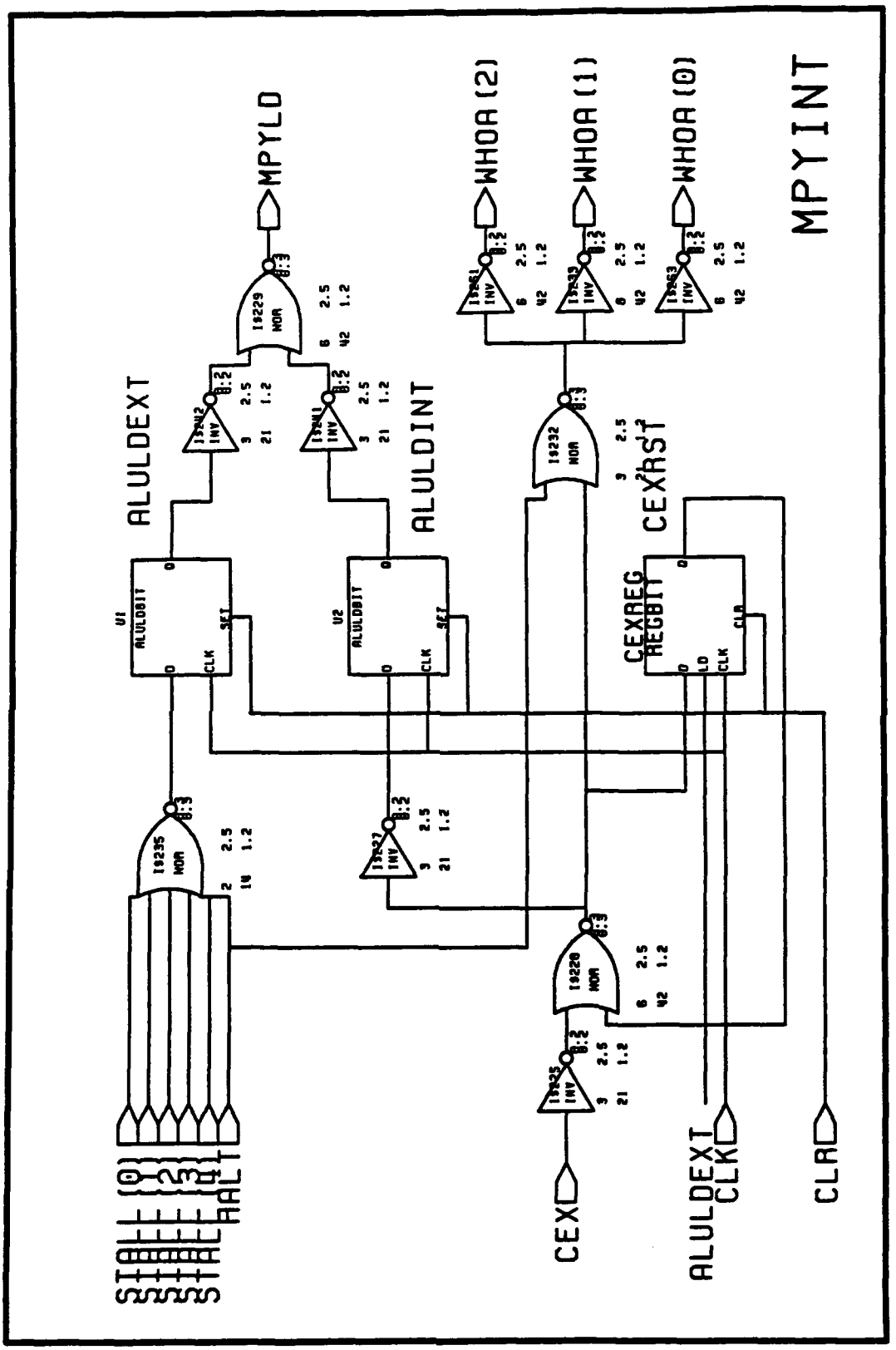

D
SDI
SSEL
SLD
PLD
RST
CLKN
TEST
Q
SDO
BITFAIL
INSTREGBIT

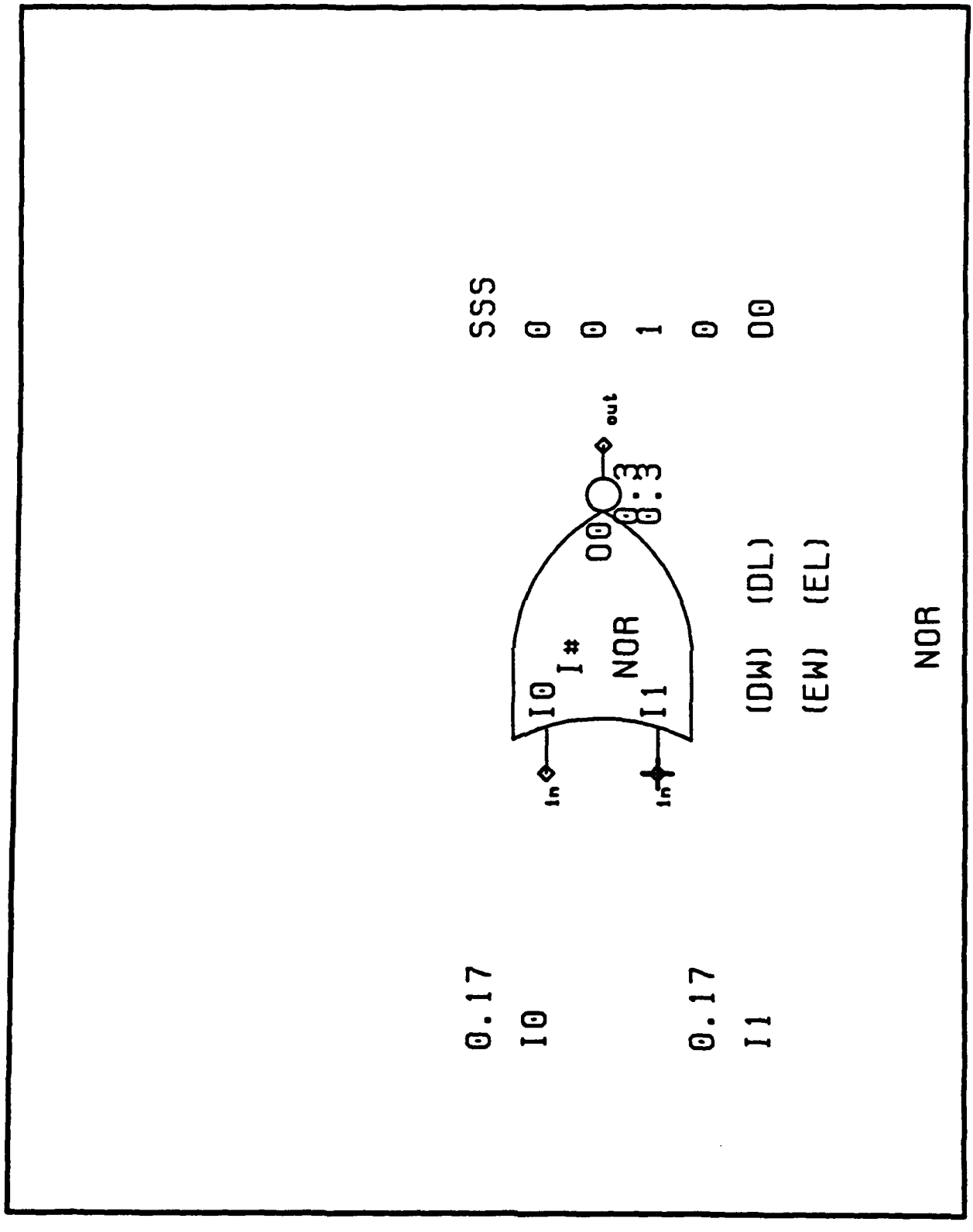

INSTREGBIT
SDO
Q
BF1
BFN1
BITFAIL
INST8IT2
DOUT
BITFAIL
BITFAILN
U8
DIN
PLO
TEST
CLKN
SET
BF0
BFN0
INST8IT1
DOUT
BITFAIL
BITFAILN
U36
SLO
SOI
SSEL
D
TEST
CLKN
CLR
I8128
NOR
I8124
NOR
I8125
NOR
BF0
BF1
BFN0
BFN1
SLO
SOI
SSEL
D
TEST
CLKN
RST
PLO

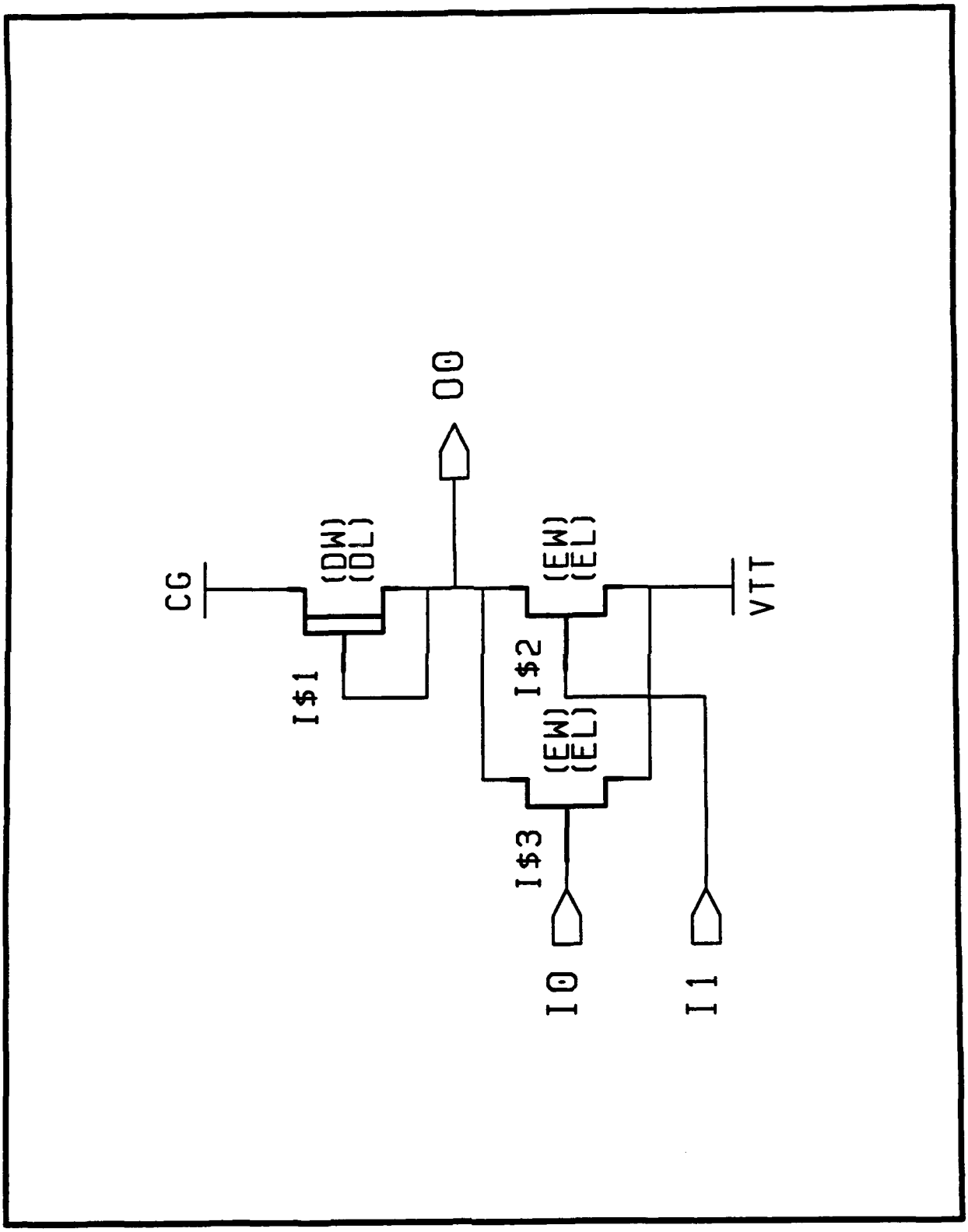

SSS
0 0 1 0 00
00
out
8.2
I#
INV
(DW) (DL)
(EW) (EL)
NAND
IO
In
0.17
IO

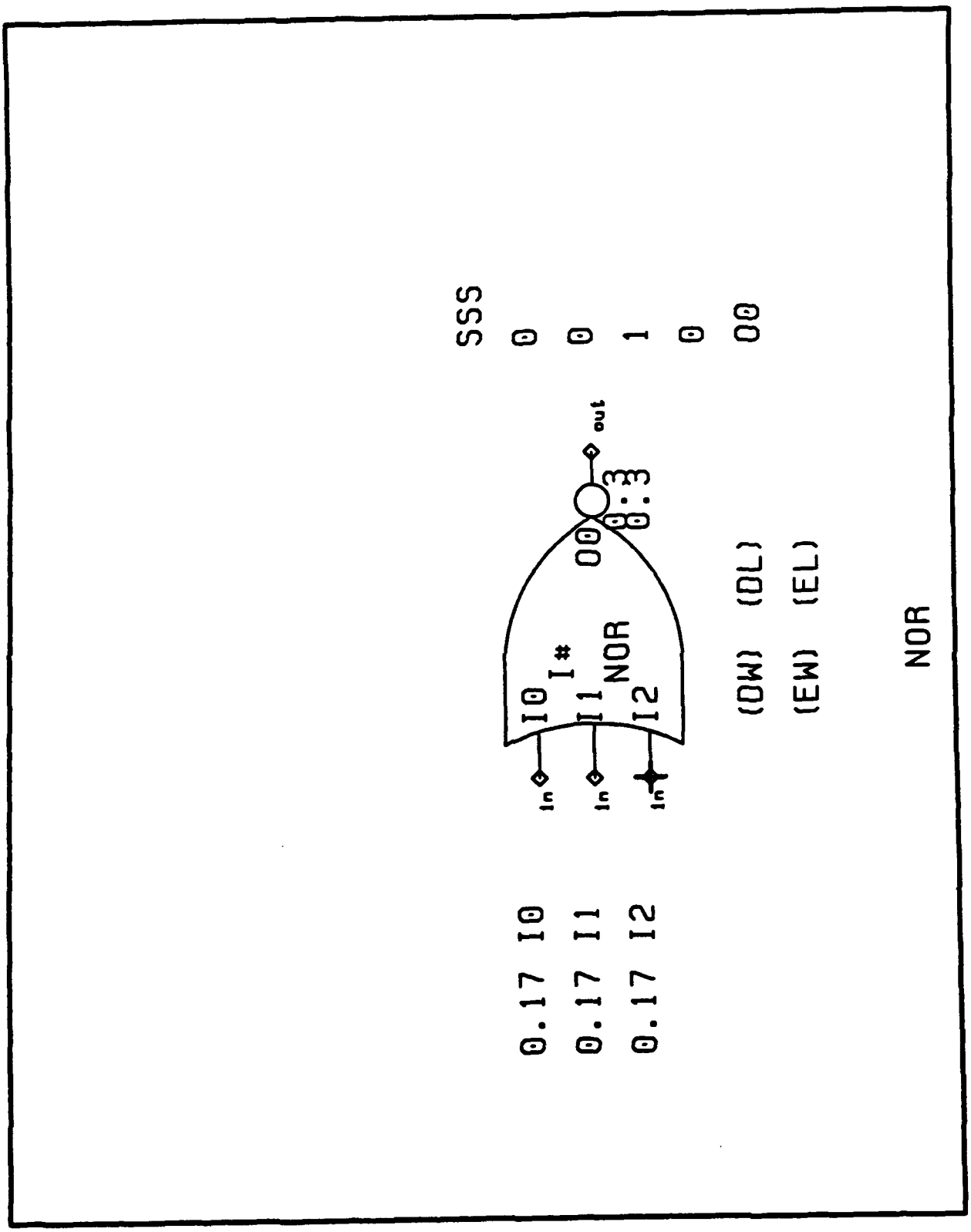

O0
CG
(DW)
(DL)
(EW)
(EL)
VTT
I$1
I$3
I0

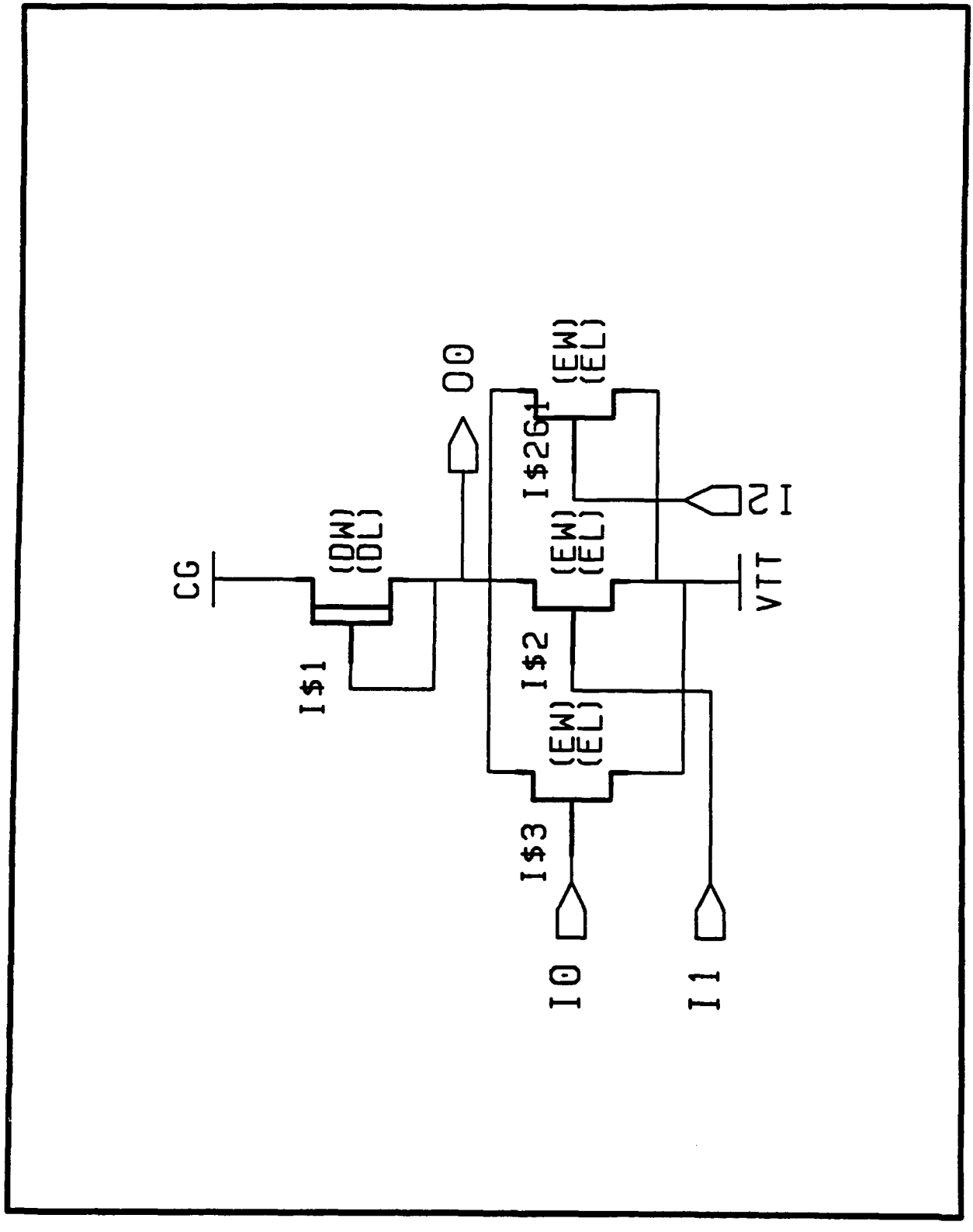

U#
STALL(4:0)
HALT
CEX
CLR
CLK
WHOA(2:0)
MPYLD
MPYINT

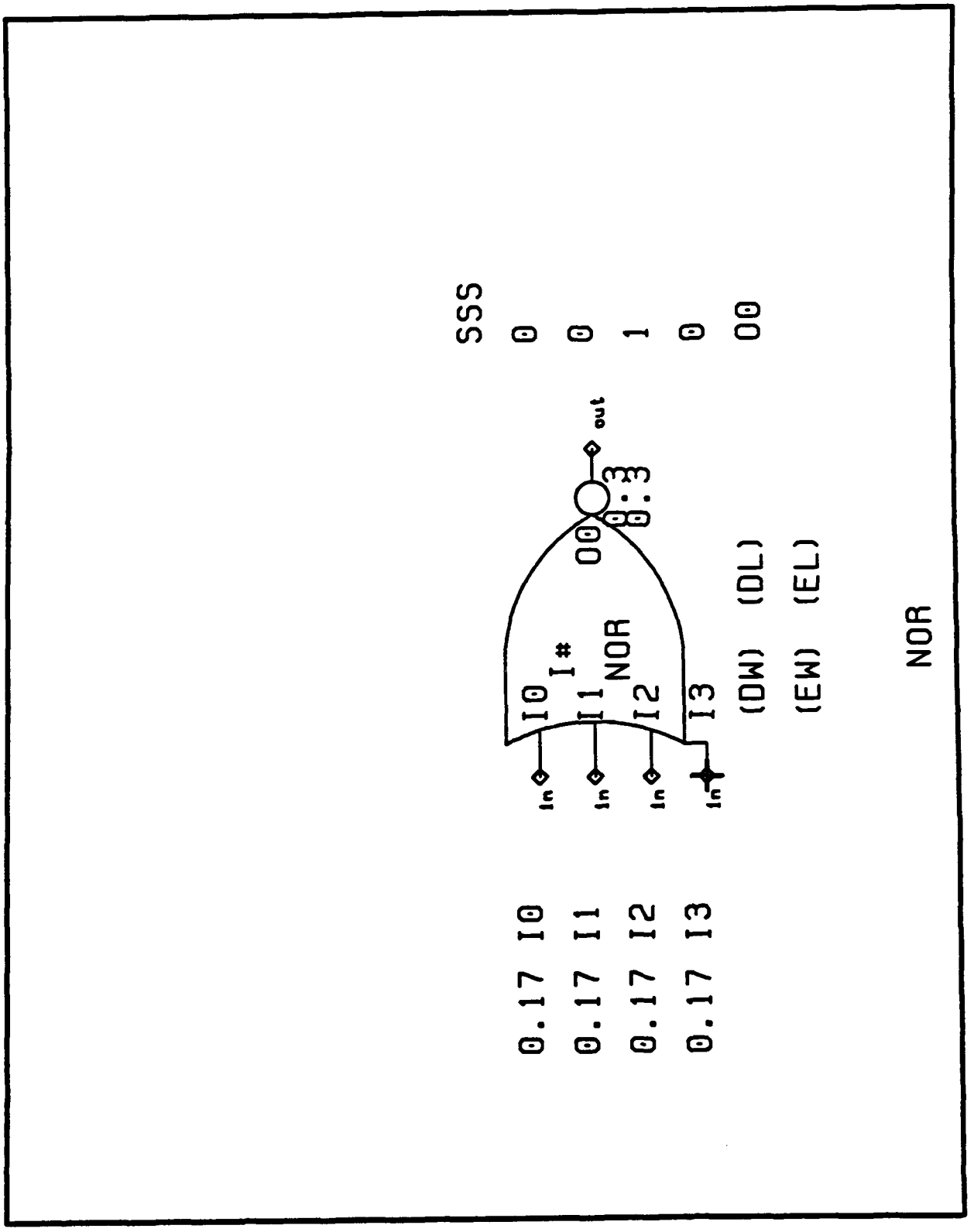

MPYINT
WHOA(2)
WHOA(1)
WHOA(0)
MPYLD
ALULDEXT
ALULDINT
CEXRST
CEXREG
REGBIT
ALULDBIT
U1
U2
SET
CLK
CLR
LD
INV
NOR
CEX
ALULDEXT CLK
CLR

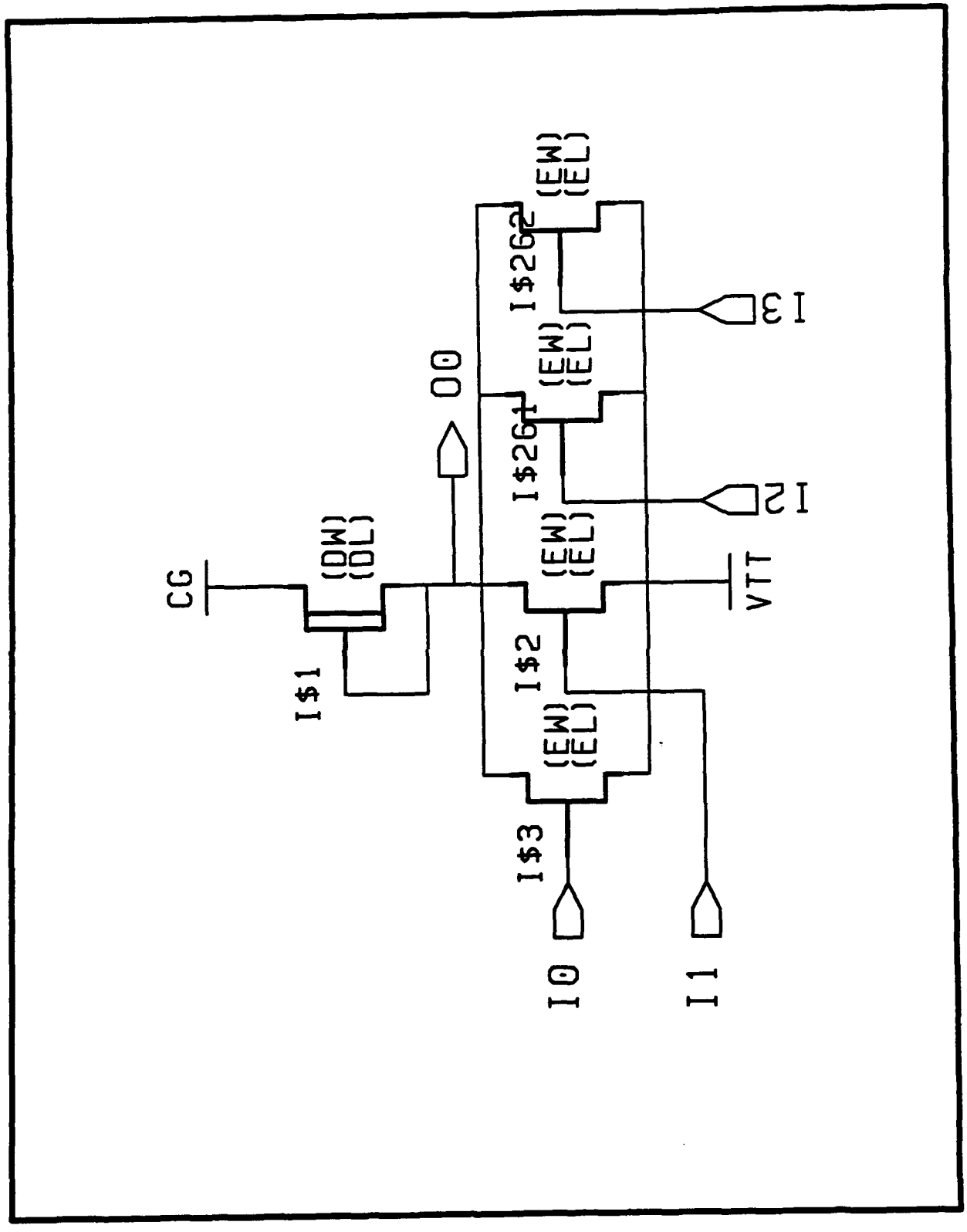

SSS
0
0
1
0
00
out
8.3
00
I0
I#
NOR
I1
in
in
(DW) (DL)
(EW) (EL)
NOR
0.17
I0
0.17
I1

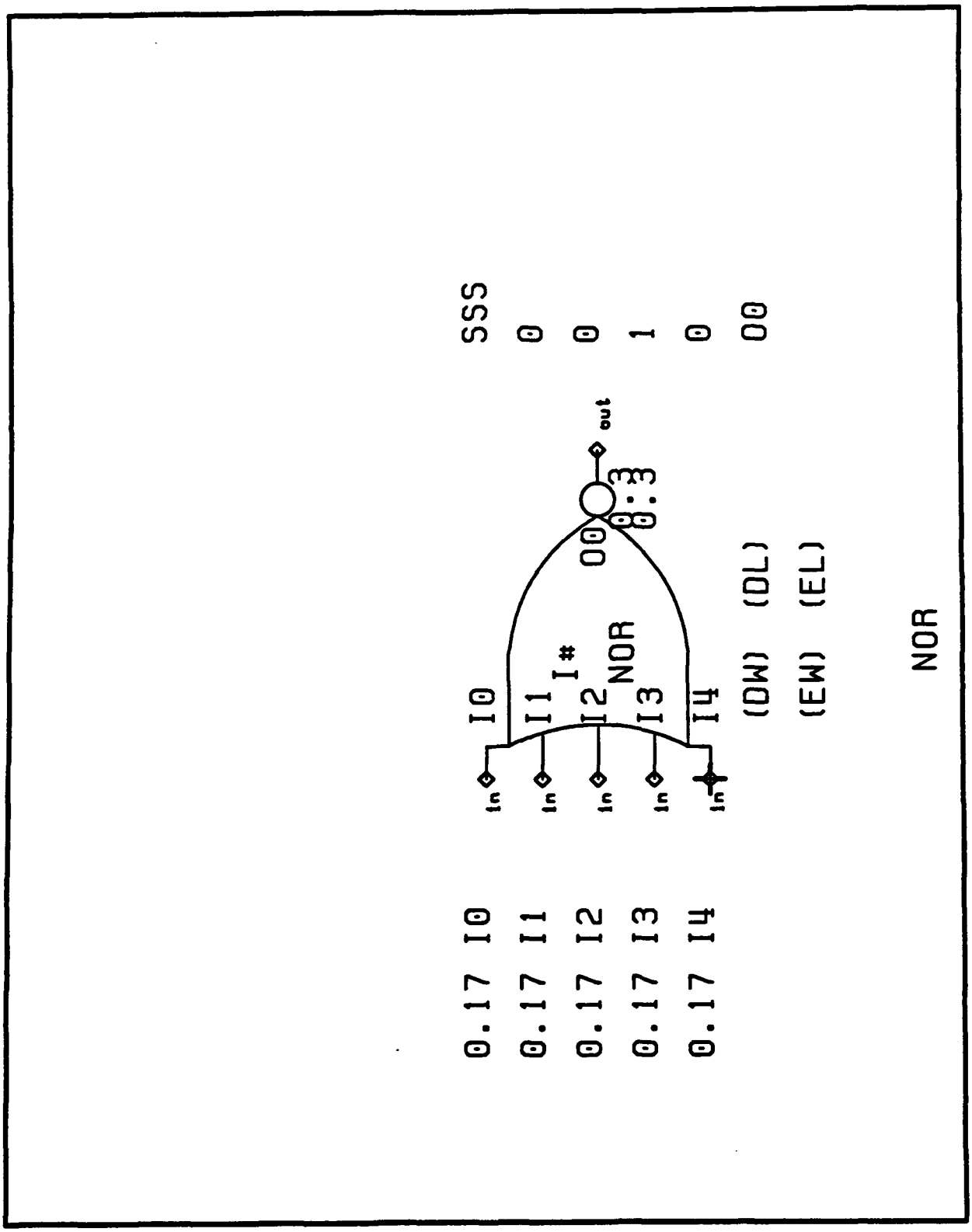

O0
CG
(DW)
(DL)
(EW)
(EL)
VTT
I$1
I$2
(EW)
(EL)
I$3
I0
I1

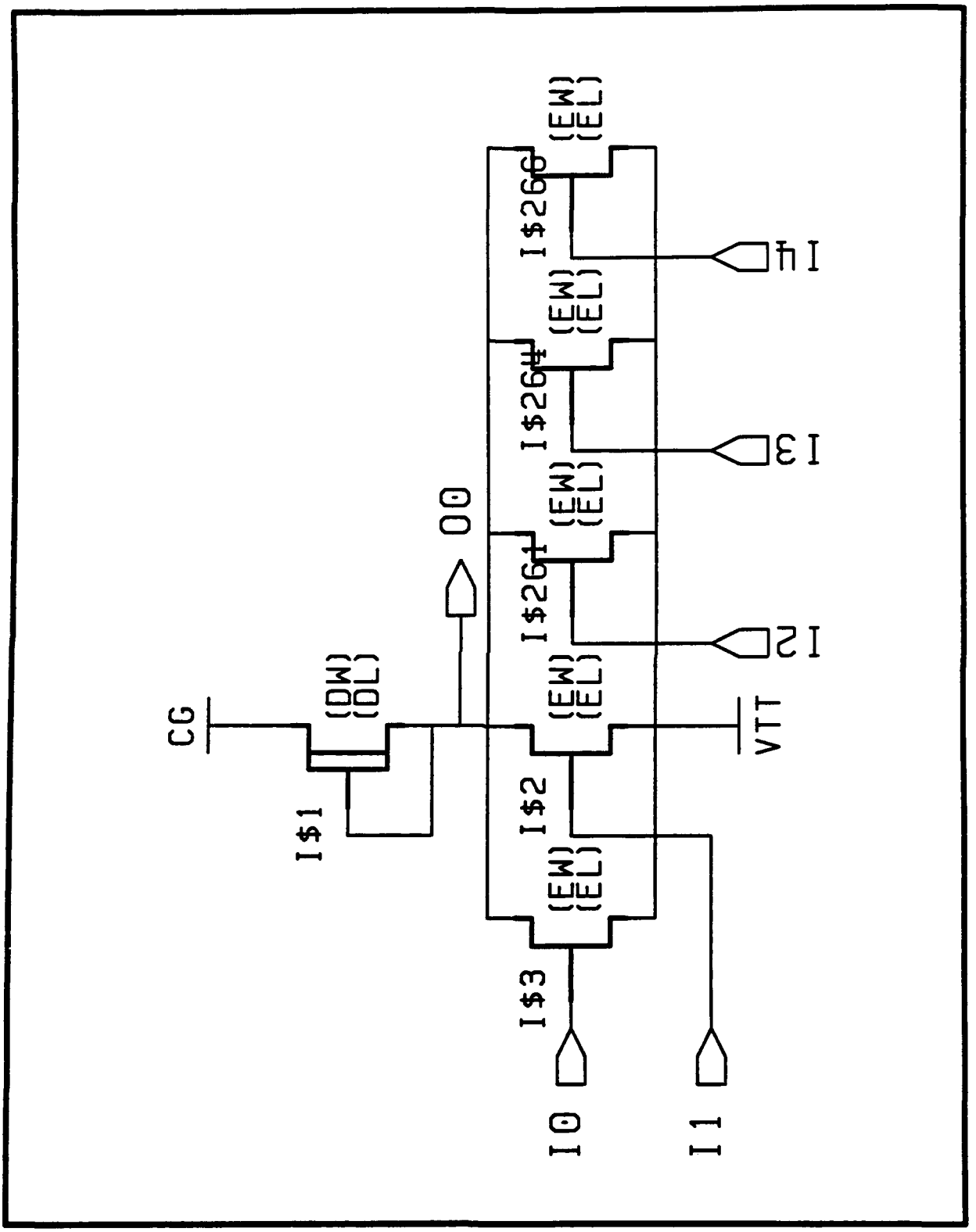

SSS
0 0 1 0 00
out
8:3
00
I0
I#
I1
NOR
I2
In
In
In
(OW) (DL)
(EW) (EL)
NOR
0.17 I0
0.17 I1
0.17 I2

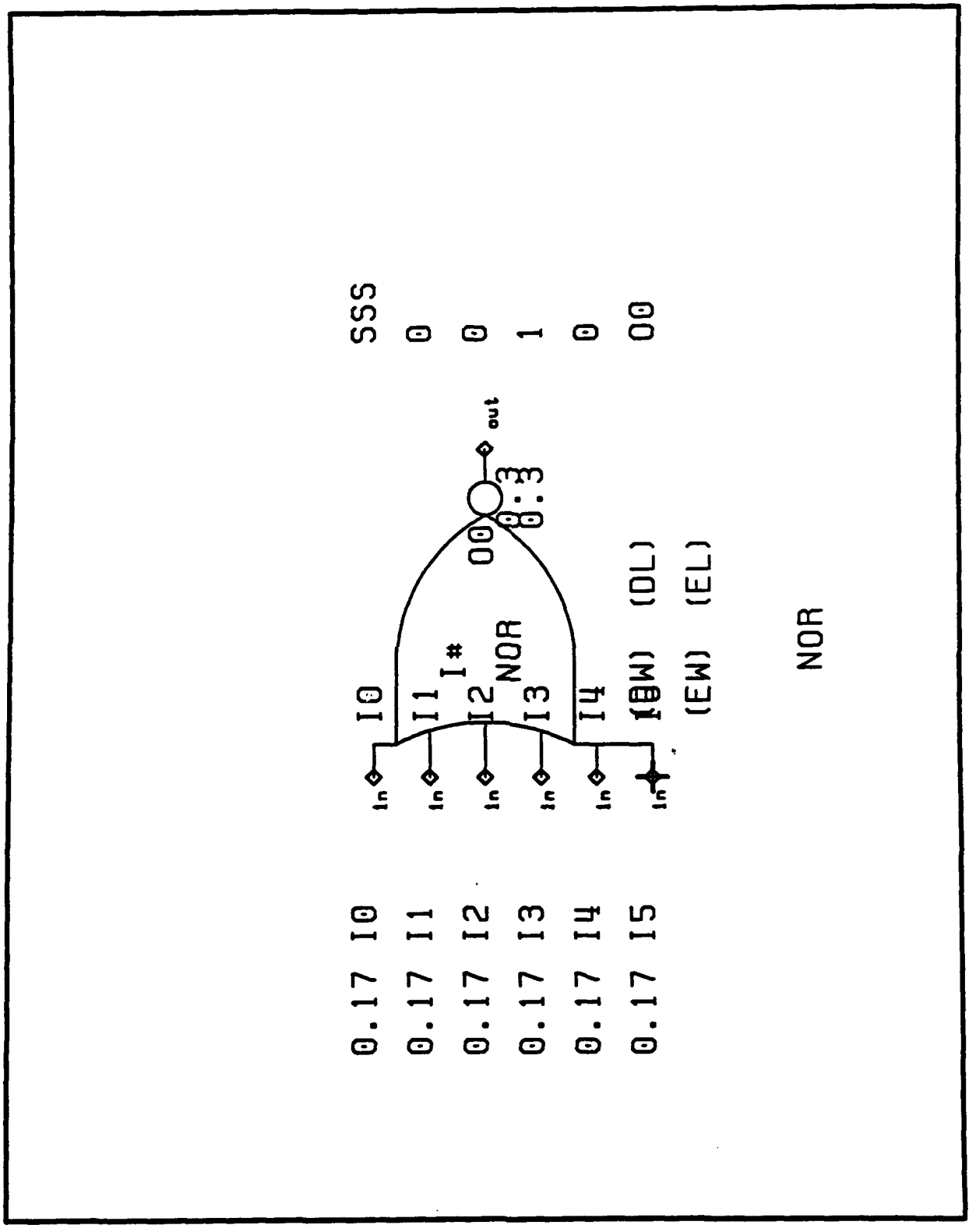

O0
(EW)
(EL)
I$261
I2
CG
(DW)
(DL)
(EW)
(EL)
VTT
I$1
I$2
(EW)
(EL)
I$3
I0
I1

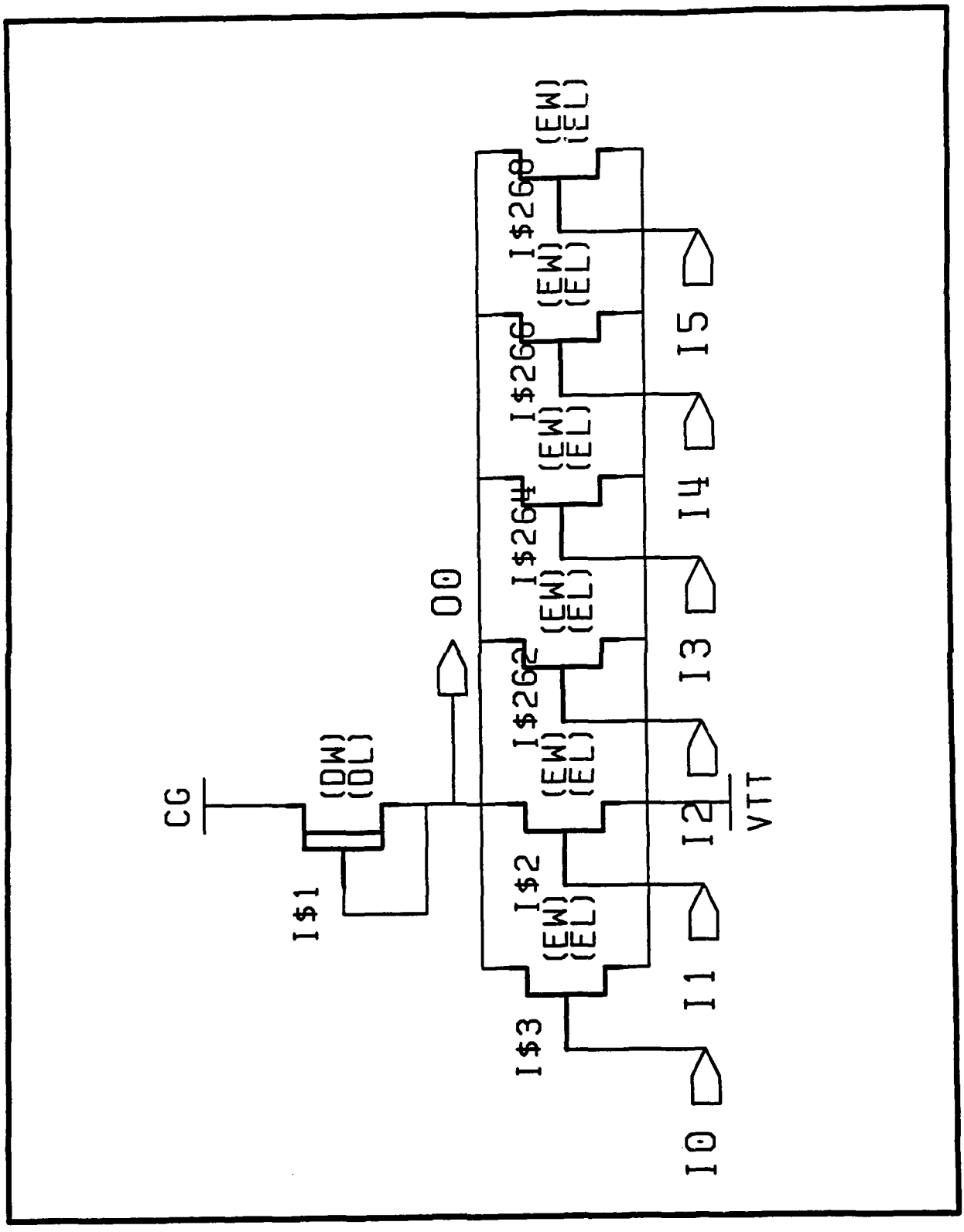

SSS
0 0 1 0 00
out
0.3
00
I0 I# NOR
I1
I2
I3
(DW) (DL)
(EW) (EL)
NOR
In
In
In
In
0.17 I0
0.17 I1
0.17 I2
0.17 I3

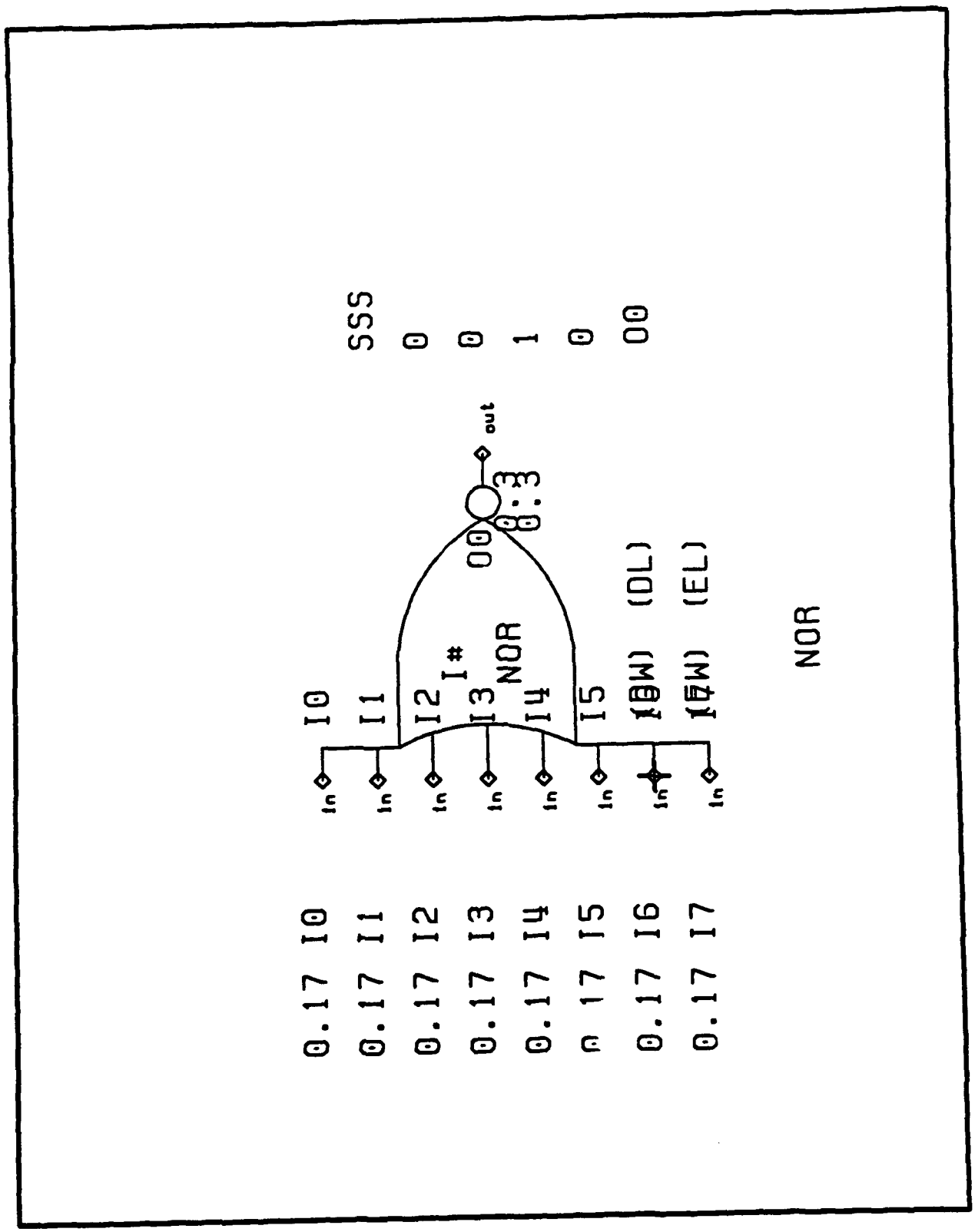

I$262
(EW)
(EL)
I3
O0
I$261
(EW)
(EL)
I2
CG
(DW)
(DL)
I$1
(EW)
(EL)
VTT
I$2
(EW)
(EL)
I$3
I0
I1

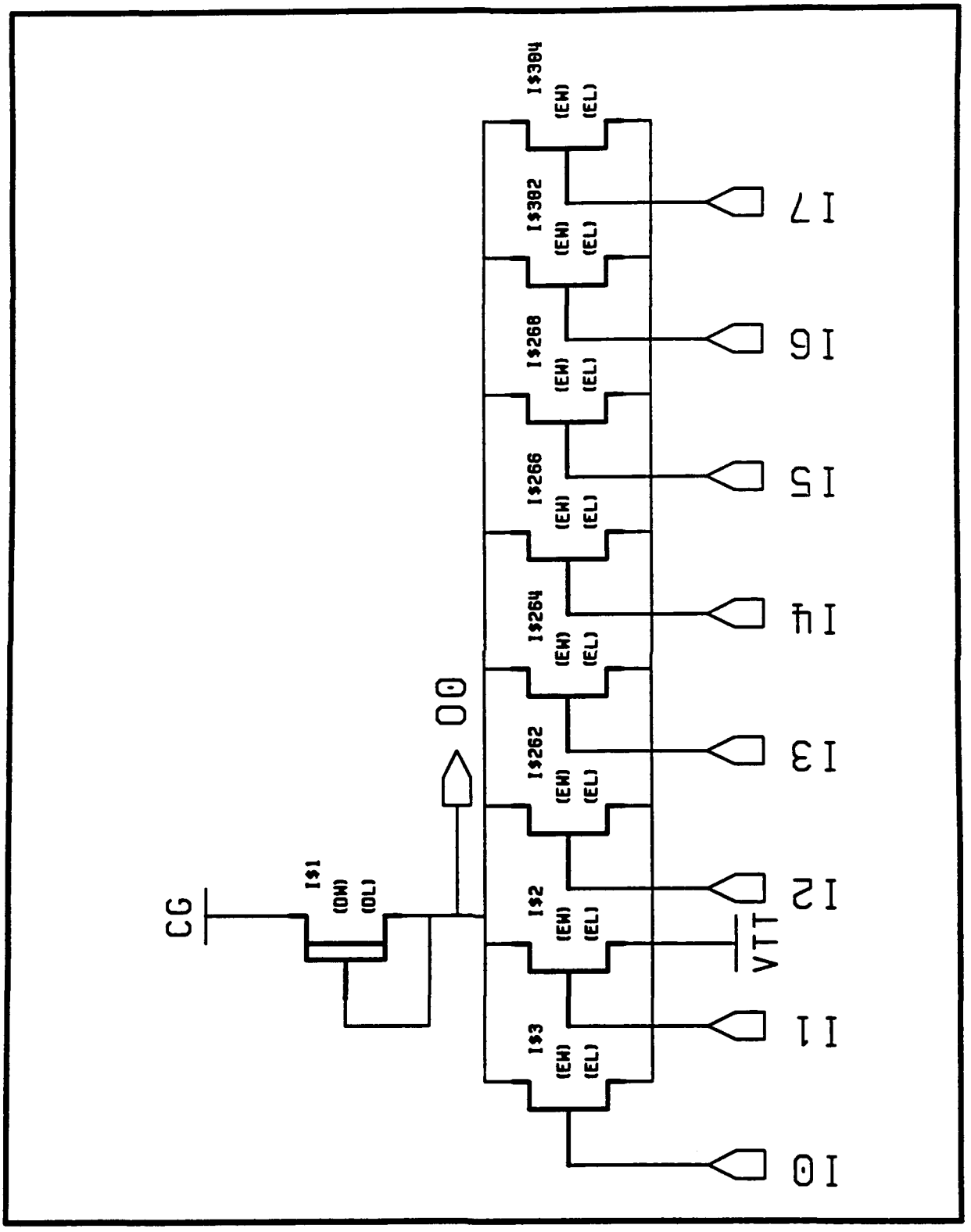

SSS
0
0
1
0
00
out
00
0.3
0.3
I0
I1
I#
I2
NOR
I3
I4
in
in
in
in
in
(OW) (DL)
(EW) (EL)
NOR
0.17 I0
0.17 I1
0.17 I2
0.17 I3
0.17 I4

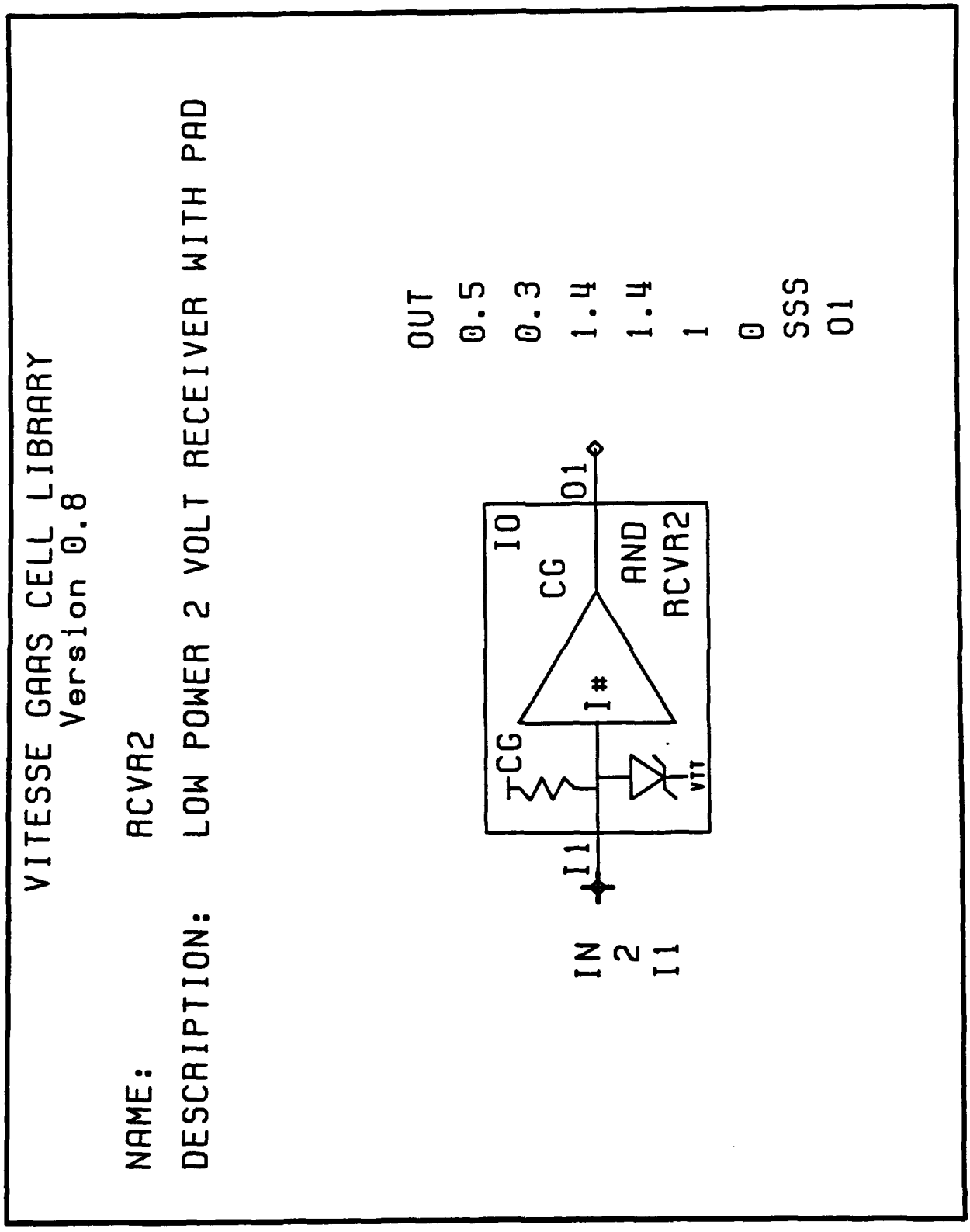

I$266
(EW)
(EL)
I4
I$264
(EW)
(EL)
I3
I$261
(EW)
(EL)
I2
O0
CG
(DW)
(DL)
I$1
I$2
(EW)
(EL)
VTT
I$3
(EW)
(EL)
I0
I1

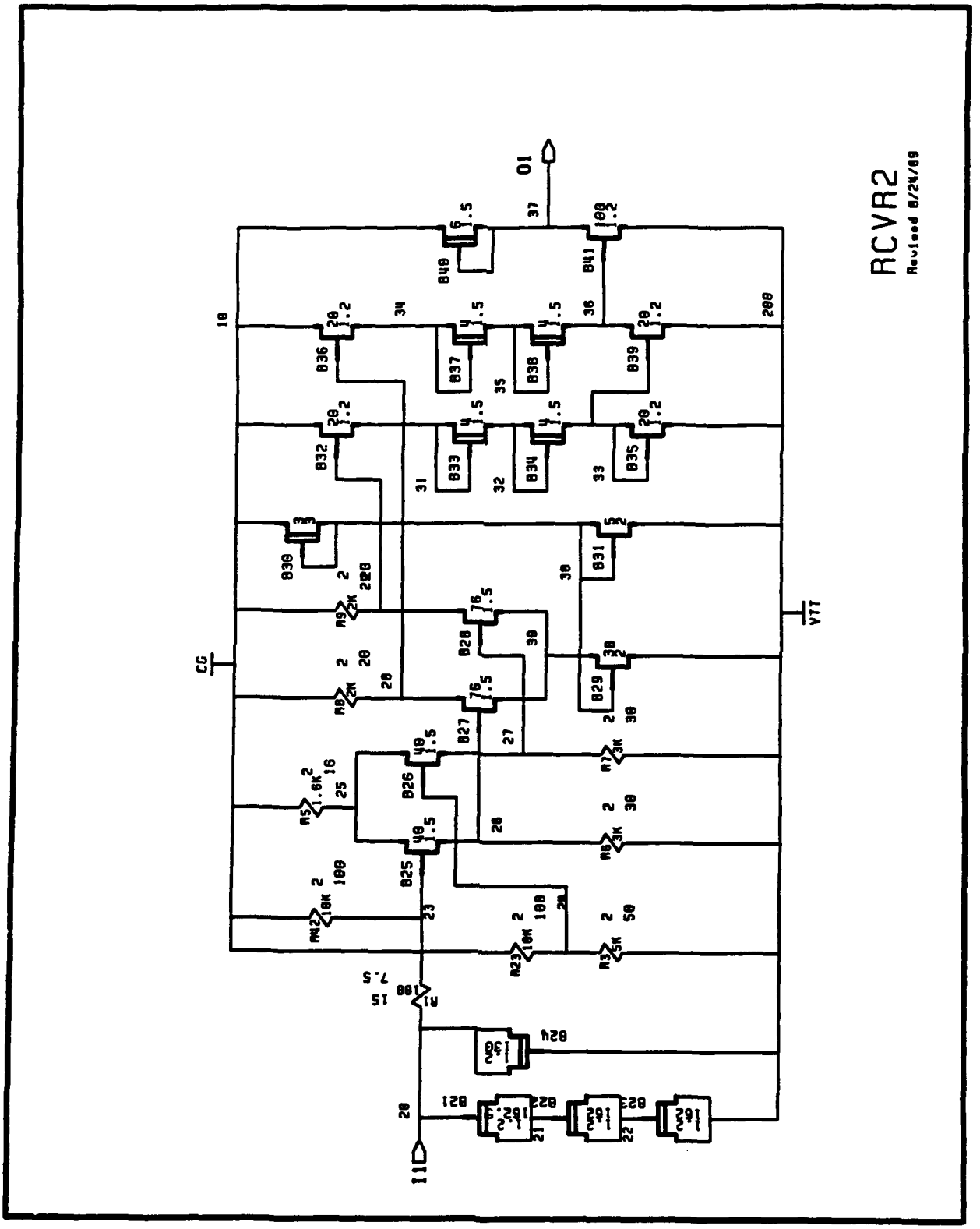

SSS
0
0
1
0
00
out
8:3
00
I0
I1
I#
I2
NOR
I3
I4
(DL)
(EW)
(EL)
NOR
0.17 I0
0.17 I1
0.17 I2
0.17 I3
0.17 I4
0.17 I5

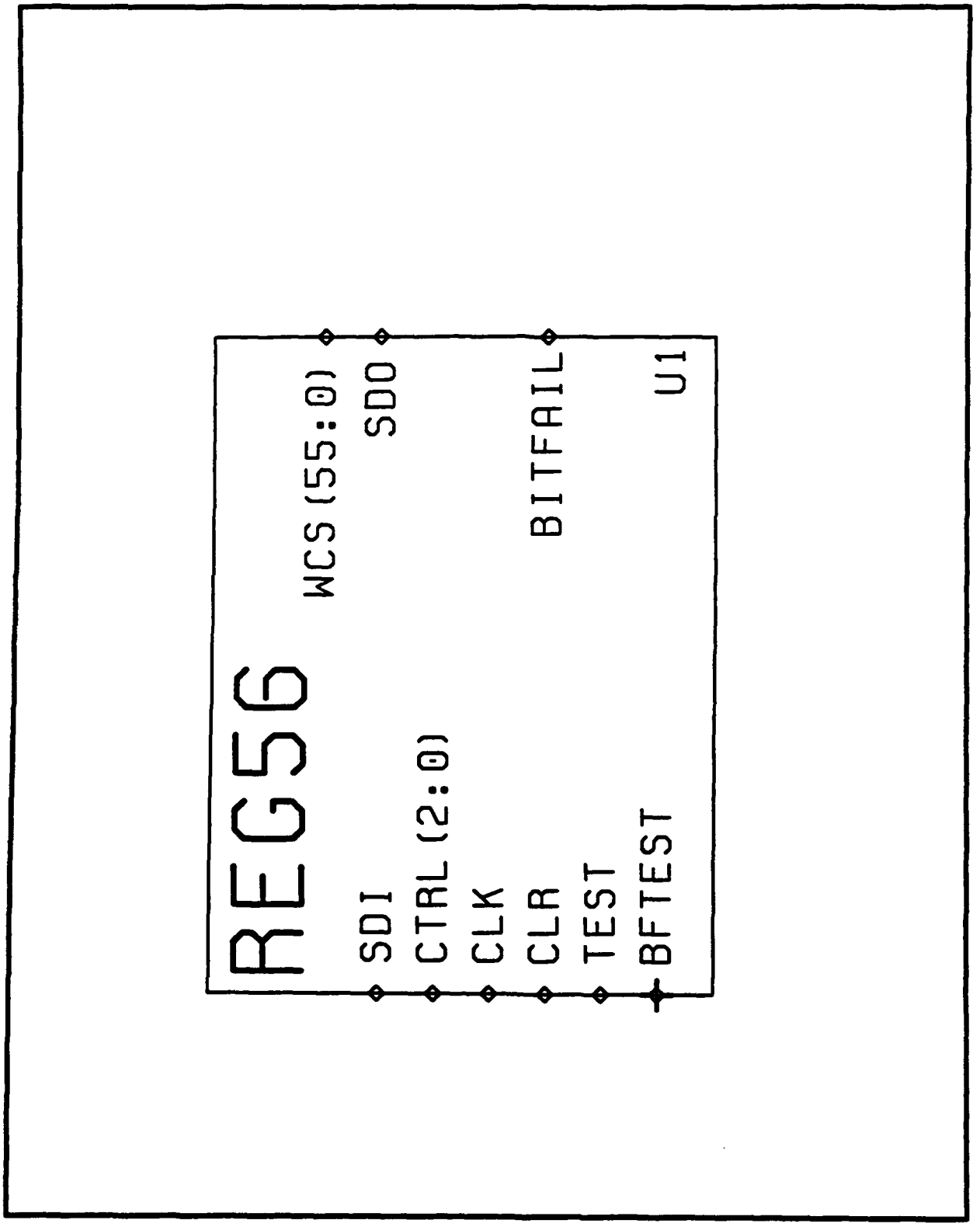

I$268
(EW)
(EL)
I$266
(EW)
(EL)
I$264
(EW)
(EL)
I$262
(EW)
(EL)
I$2
(EW)
(EL)
I$3
I5
I4
I3
I2
I1
I0
O0
CG
(DW)
(DL)
I$1
VTT

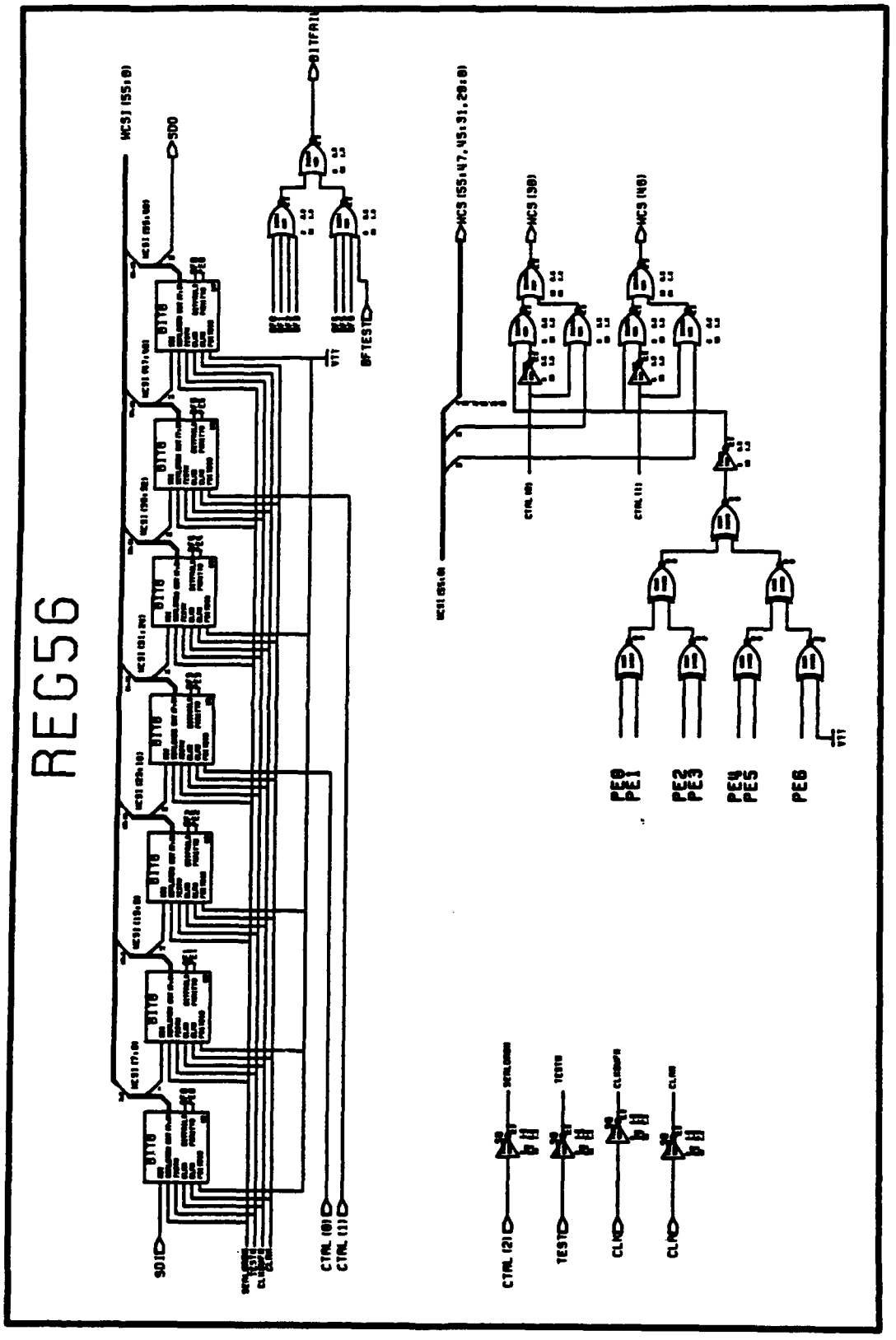

SSS
0 0 1 0 00
out
8.3
00
I#
NOR
I0
I1
I2
I3
I4
I5
(8W) (DL)
(4W) (EL)
In
NOR
0.17 I0
0.17 I1
0.17 I2
0.17 I3
0.17 I4
n 17 I5
0.17 I6
0.17 I7

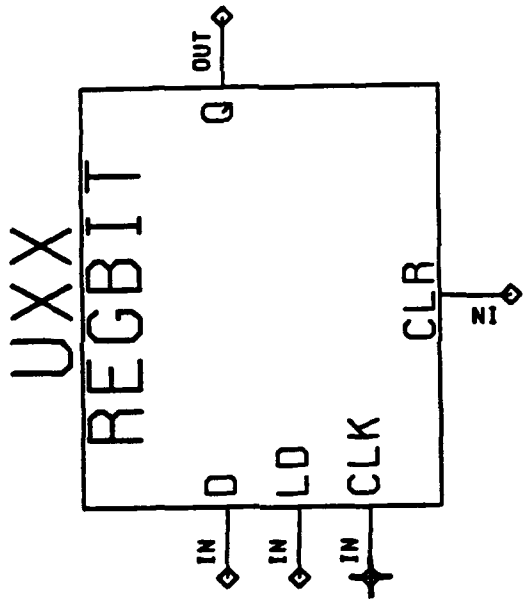

I$304
(EW)
(EL)
I$302
(EW)
(EL)
I$268
(EW)
(EL)
I$266
(EW)
(EL)
I$264
(EW)
(EL)
I$262
(EW)
(EL)
I$2
(EW)
(EL)
I$3
(EW)
(EL)
I$1
(DW)
(DL)
I7
I6
I5
I4
I3
I2
I1
I0
OO
CG
VTT

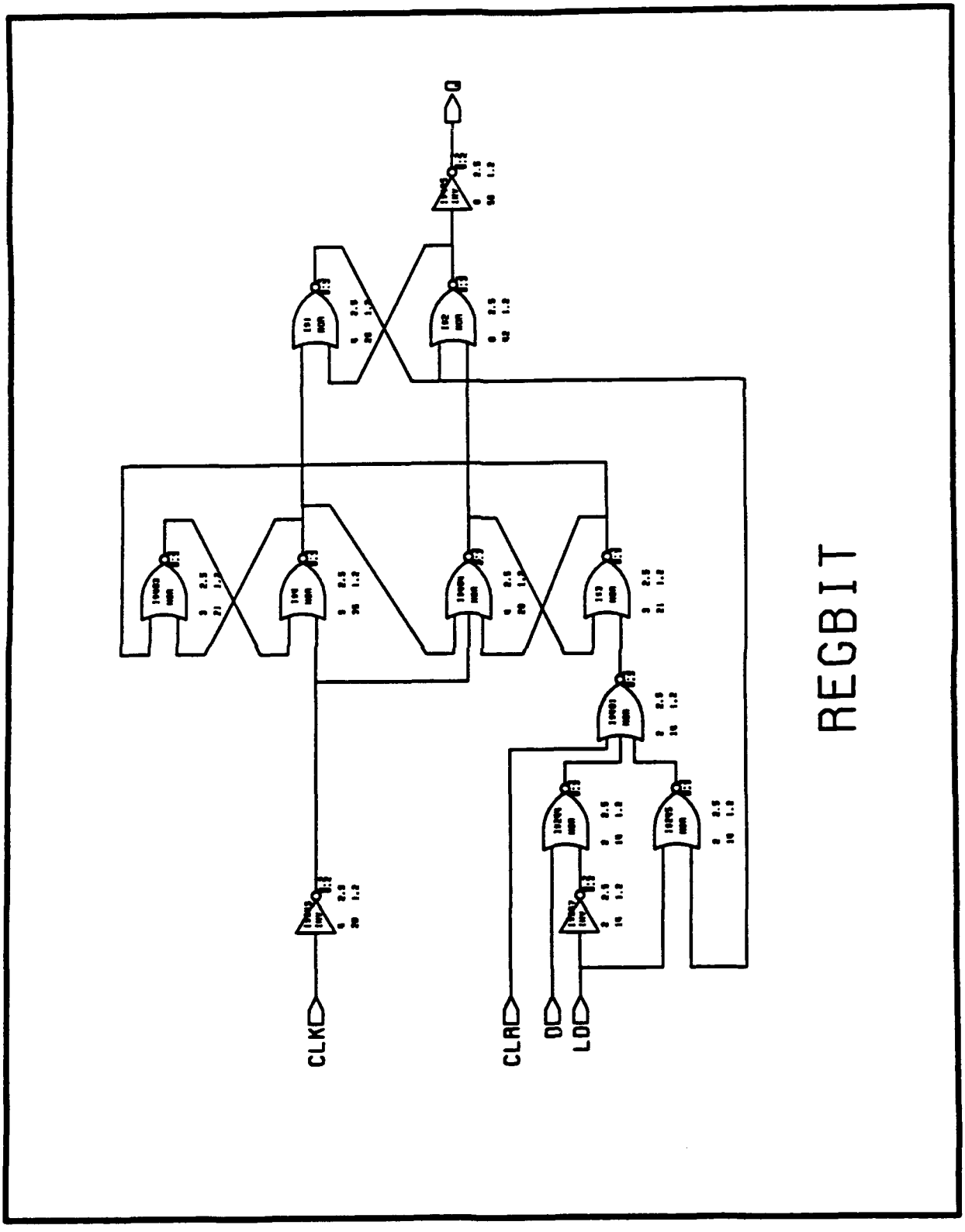

VITESSE GAAS CELL LIBRARY
Version 0.8
NAME: RCVR2
DESCRIPTION: LOW POWER 2 VOLT RECEIVER WITH PAD
OUT
0.5
0.3
1.4
1.4
1
0
SSS
01
IO
CG
AND
RCVR2
O1
I#
CG
VTT
I1
IN
2
I1


RCVR2
Revised 8/24/88
O1
I1
CG
VTT

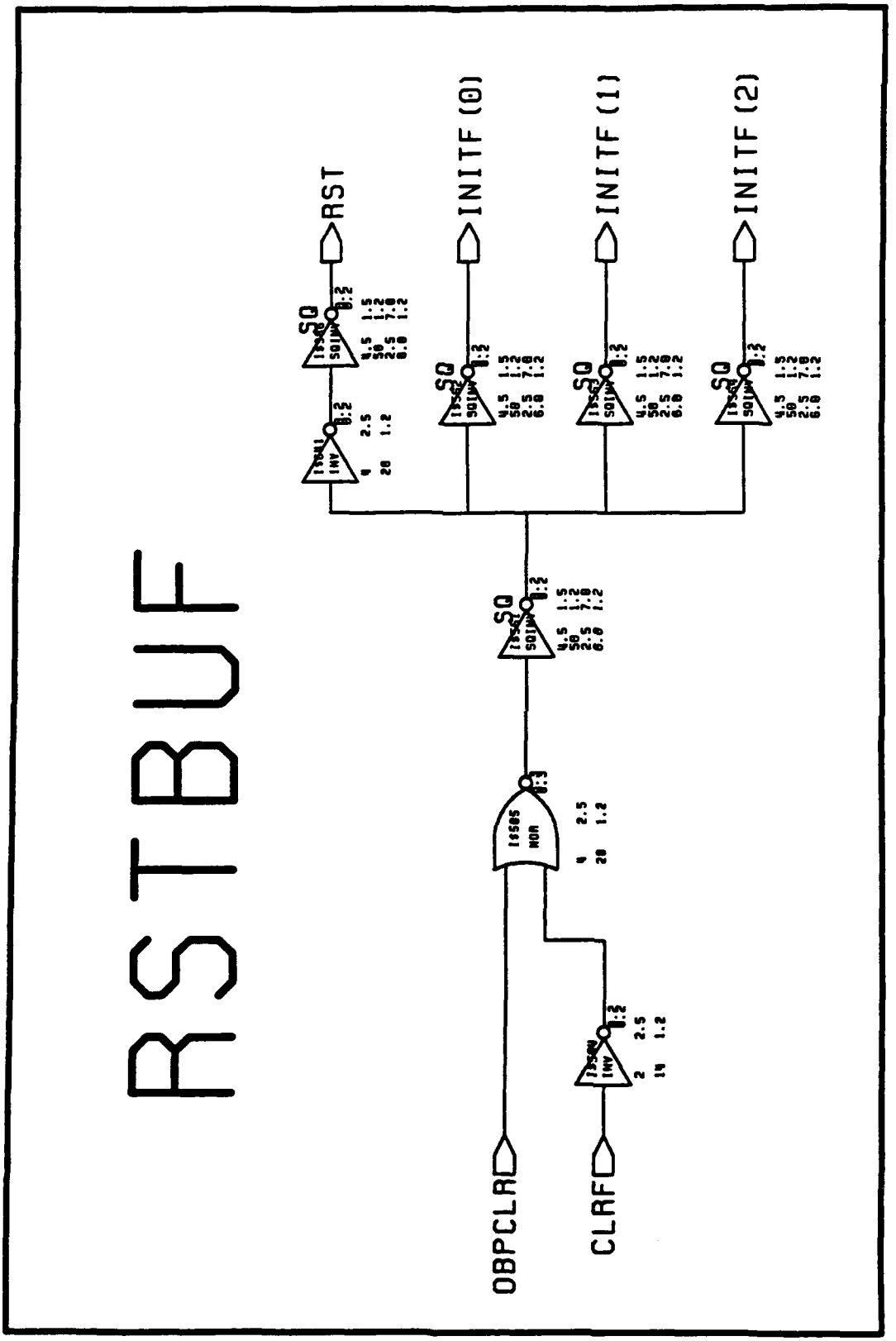

REG56
WCS(55:0)
SDO
BITFAIL
U1
SDI
CTRL(2:0)
CLK
CLR
TEST
BFTEST

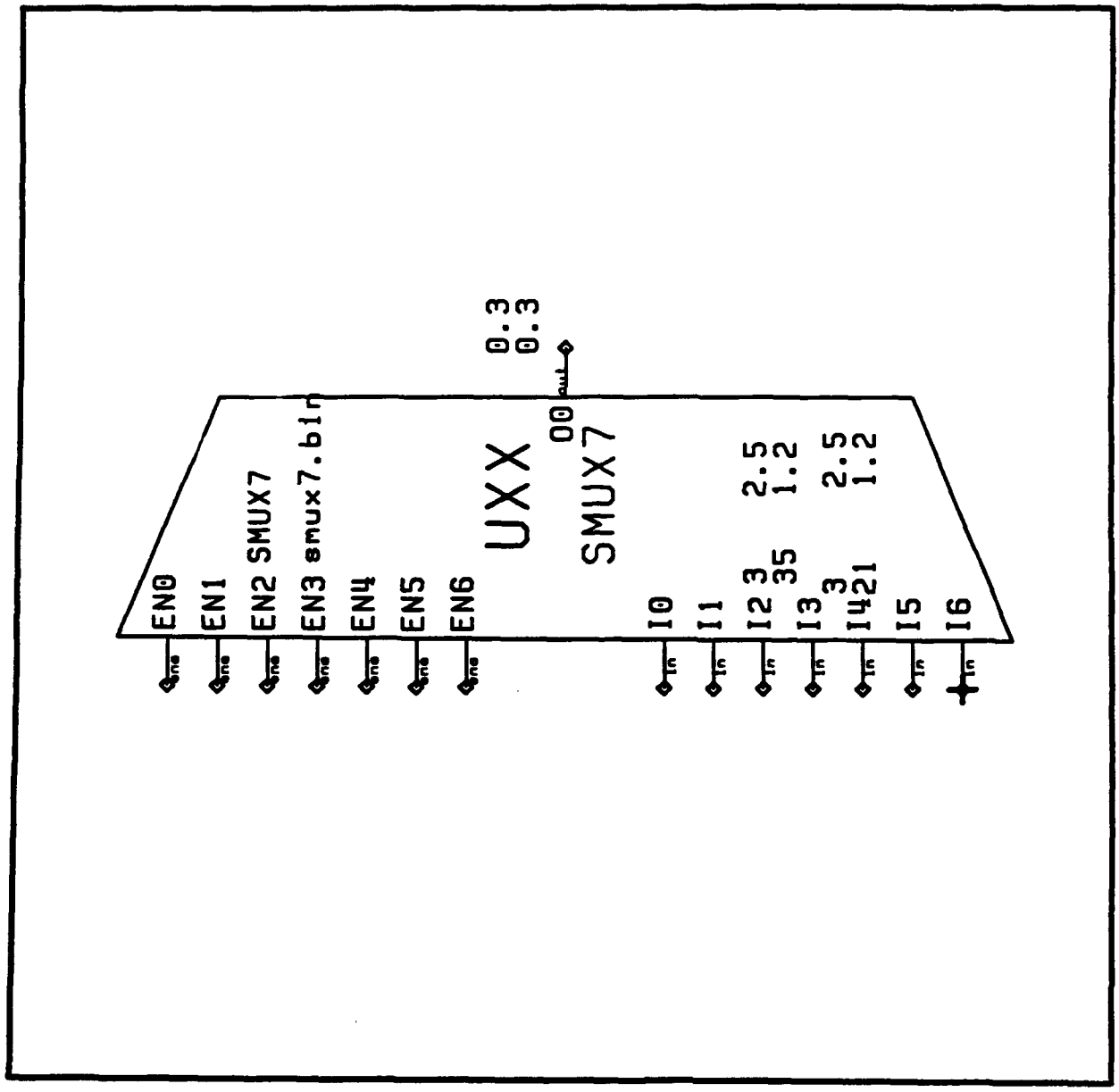

REG56
SDO
SDI
CTRL (0)
CTRL (1)
PE0
PE1
PE2
PE3
PE4
PE5
PE6
CTRL (2)
TEST
CLK0
CLK1

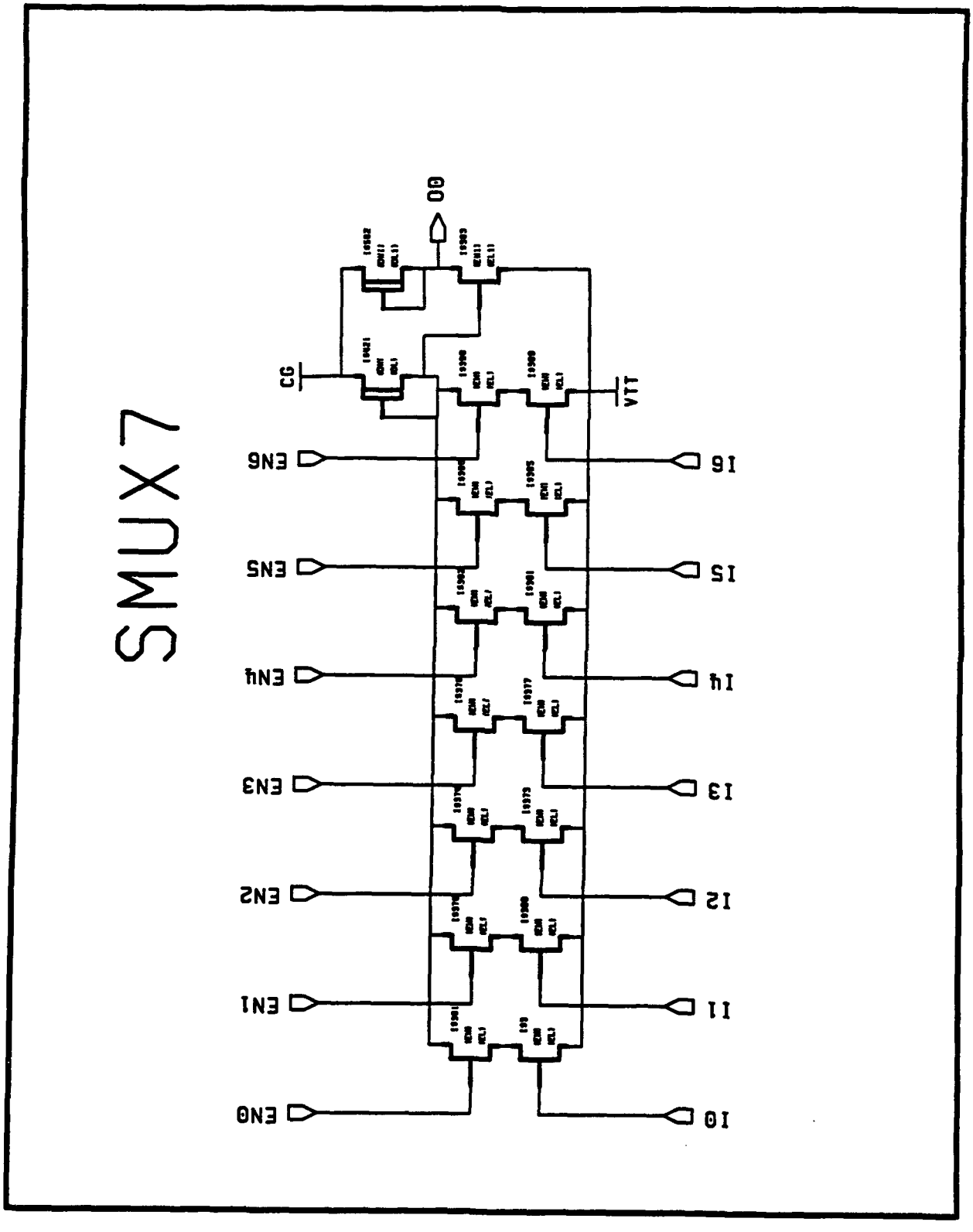

UXX
REGBIT
OUT
Q
CLR
NI
D
LD
CLK
IN
IN
IN

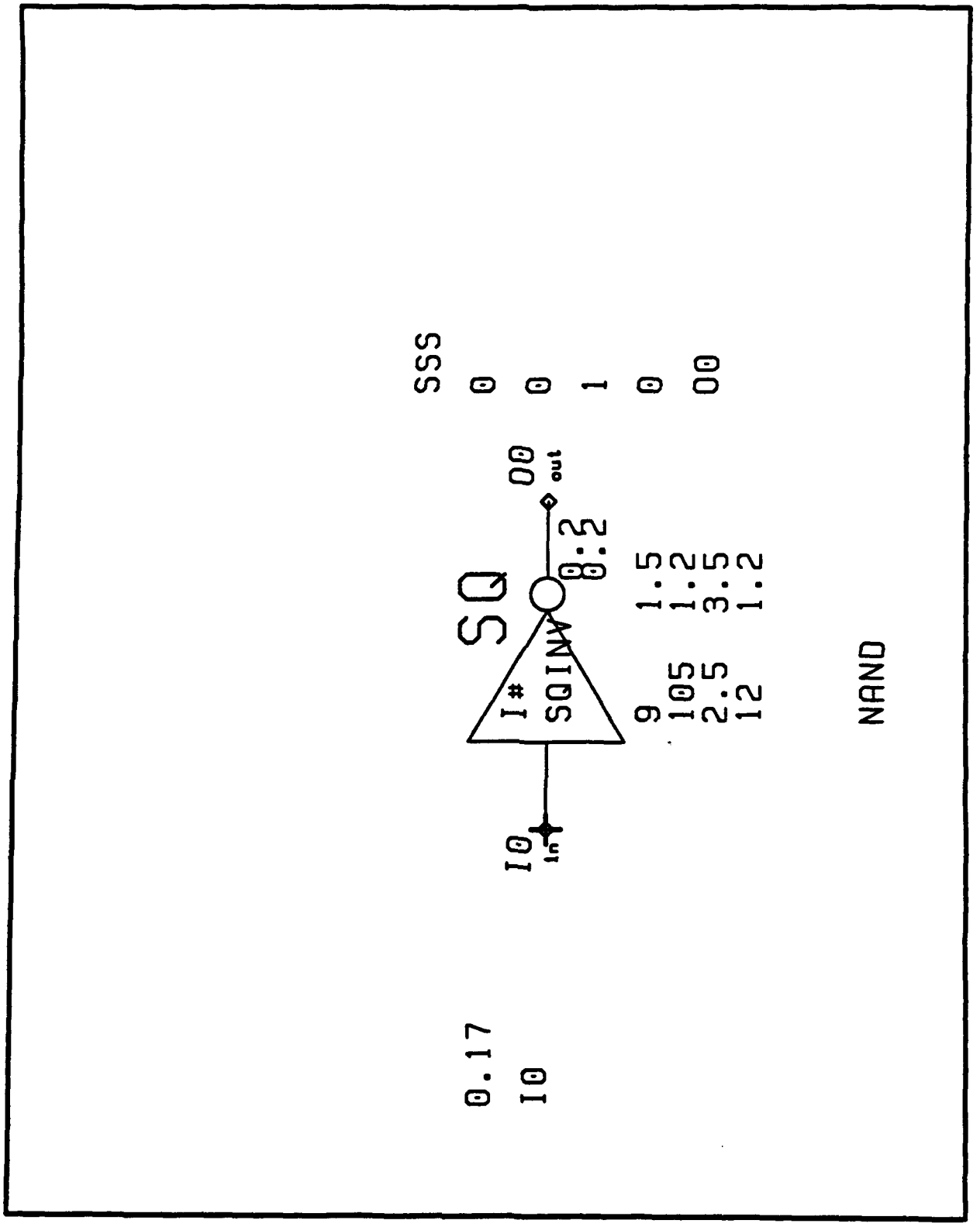

Q
CLK
CLR
D
LD
REGBIT

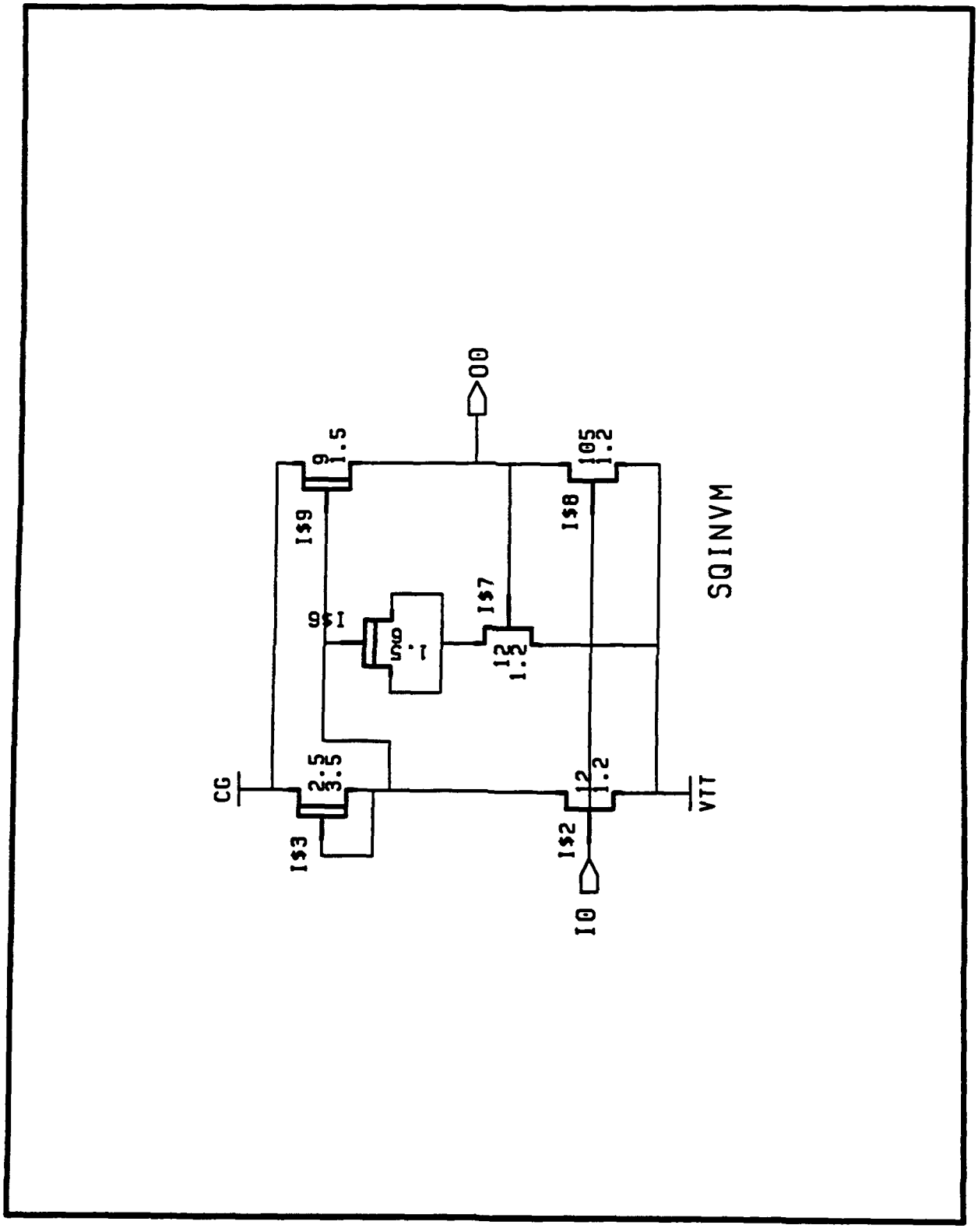

RSTBUF

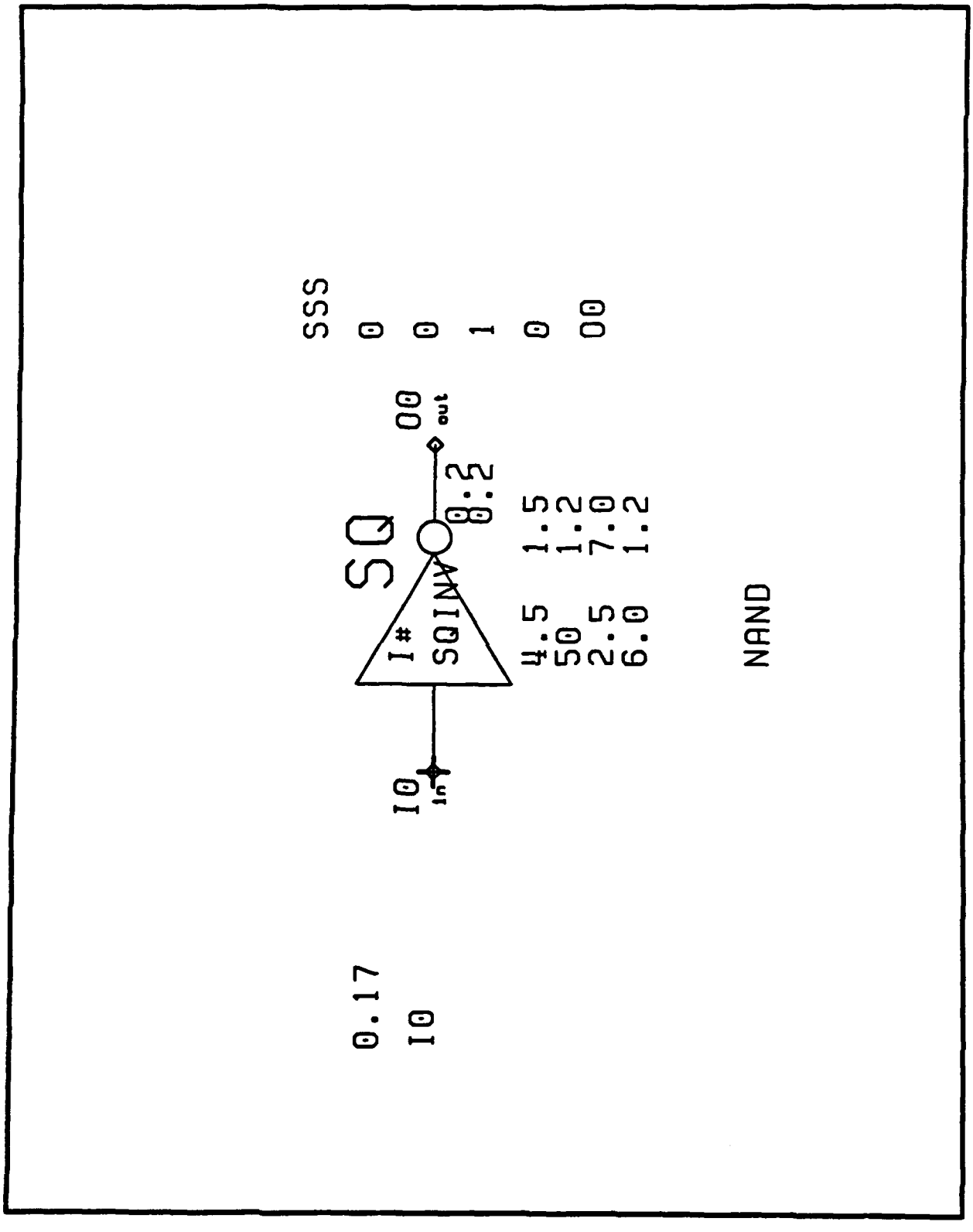

RSTBUF
RST
INITF(0)
INITF(1)
INITF(2)
OBPCLR
CLRF

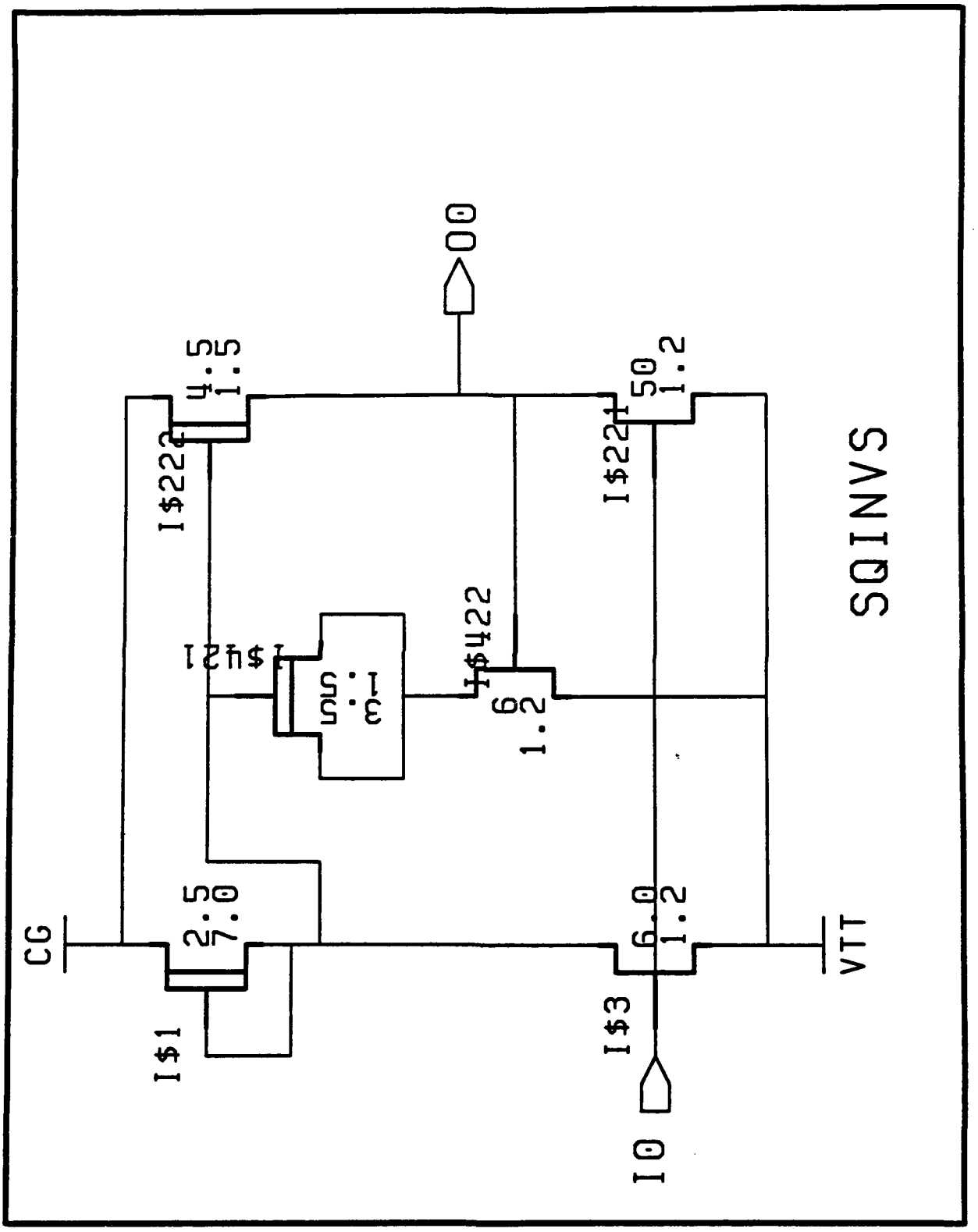

0.3
0.3
UXX
00
SMUX7
smux7.bin
SMUX7
EN0
EN1
EN2
EN3
EN4
EN5
EN6
I0
I1
I2
I3
I4
I5
I6
2.5
1.2
2.5
1.2
3
35
3
21

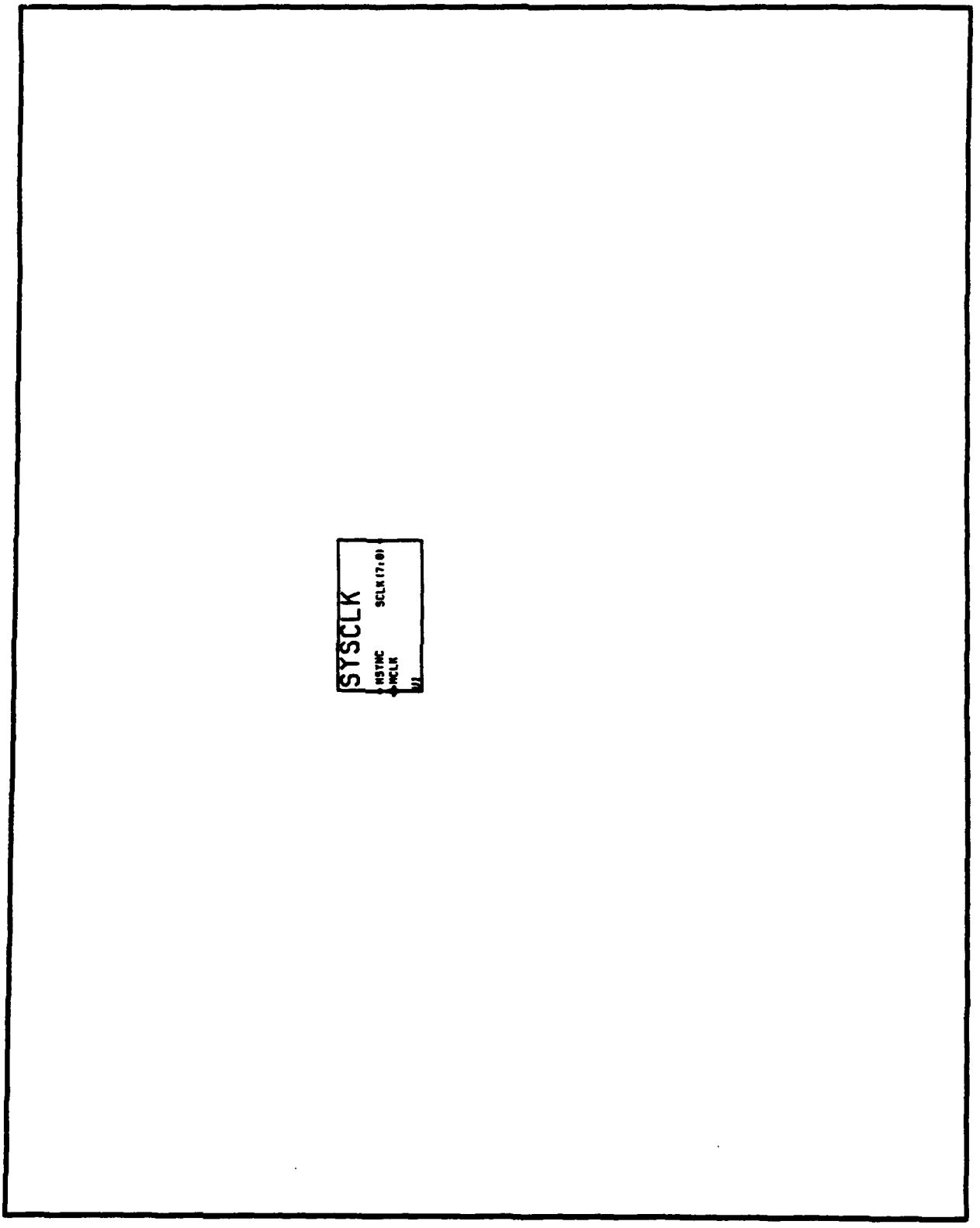

SMUX7
O0
CG
VTT
EN6
I6
EN5
I5
EN4
I4
EN3
I3
EN2
I2
EN1
I1
EN0
I0

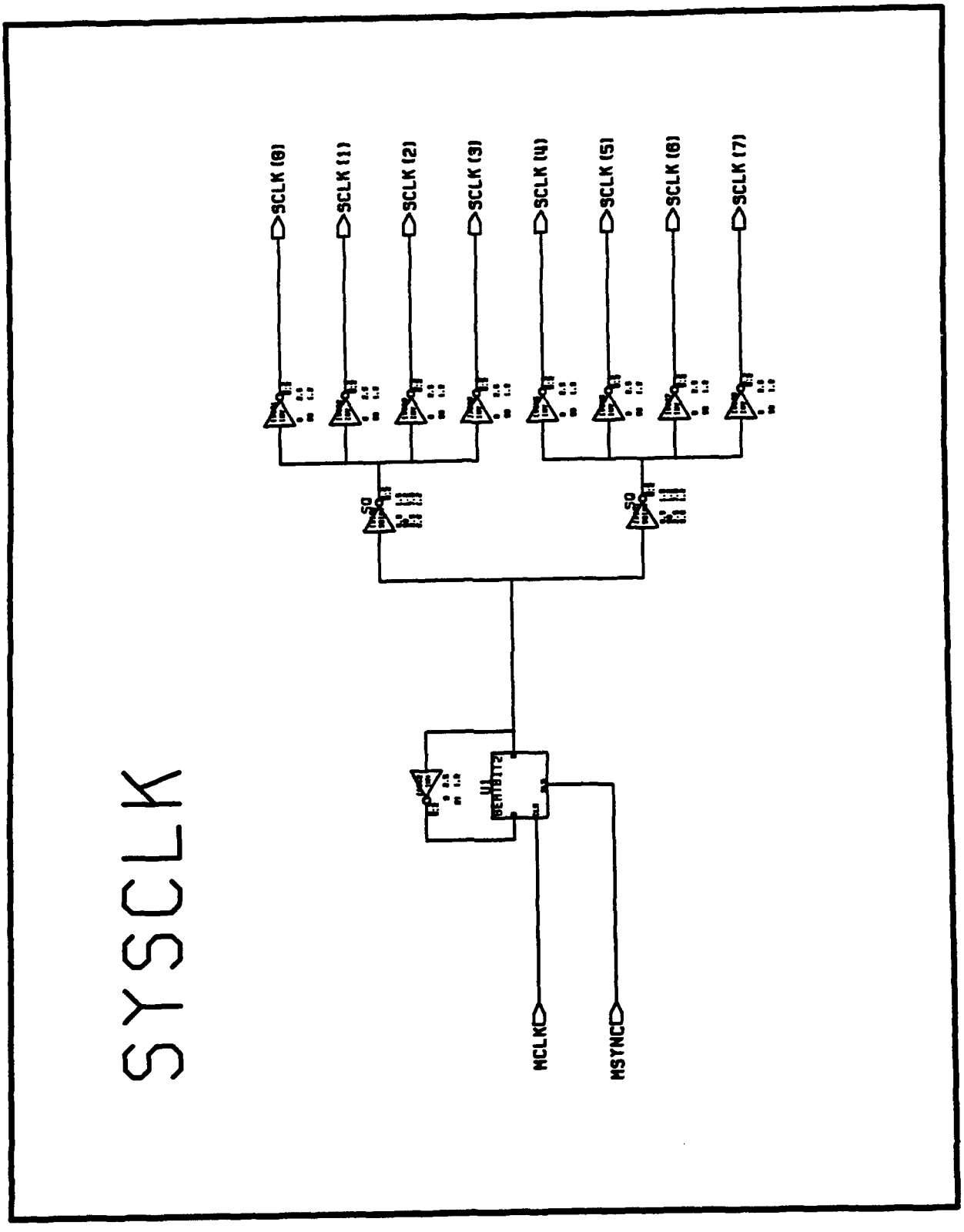

SSS
0 0 1 0 00
00
out
8.2
SQ
1.5
1.2
3.5
1.2
I#
SQINV
9
105
2.5
12
NAND
I0
in
0.17
I0

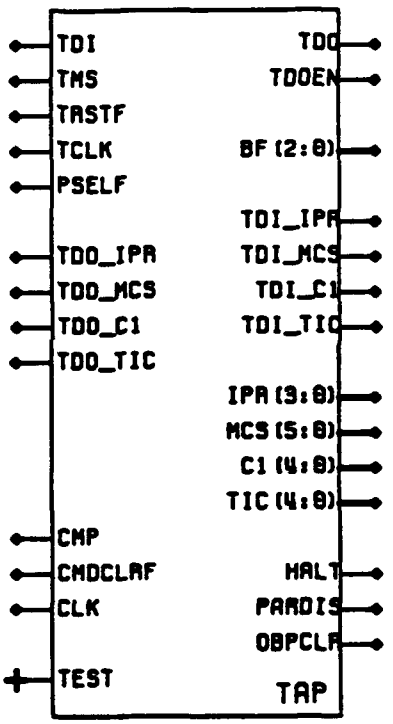

O0
I$9
I$8
I$7
I$1
I$3
I$2
I0
CG
VTT
SQINVM

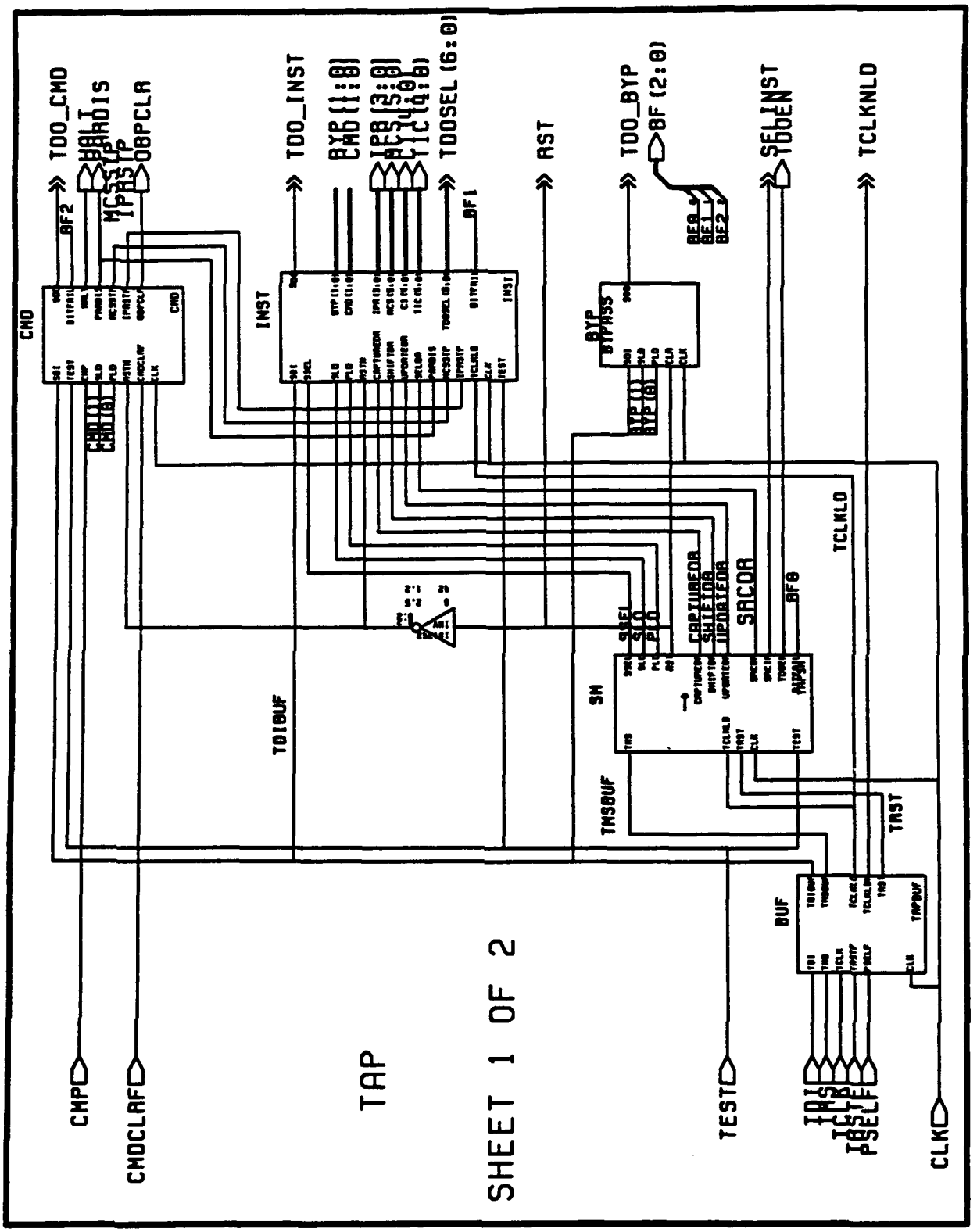

SSS
0 0 1 0 00
00
out
8.2
SQ
I#
SQINV
4.5 1.5
50 1.2
2.5 7.0
6.0 1.2
NAND
IO
in
0.17
IO

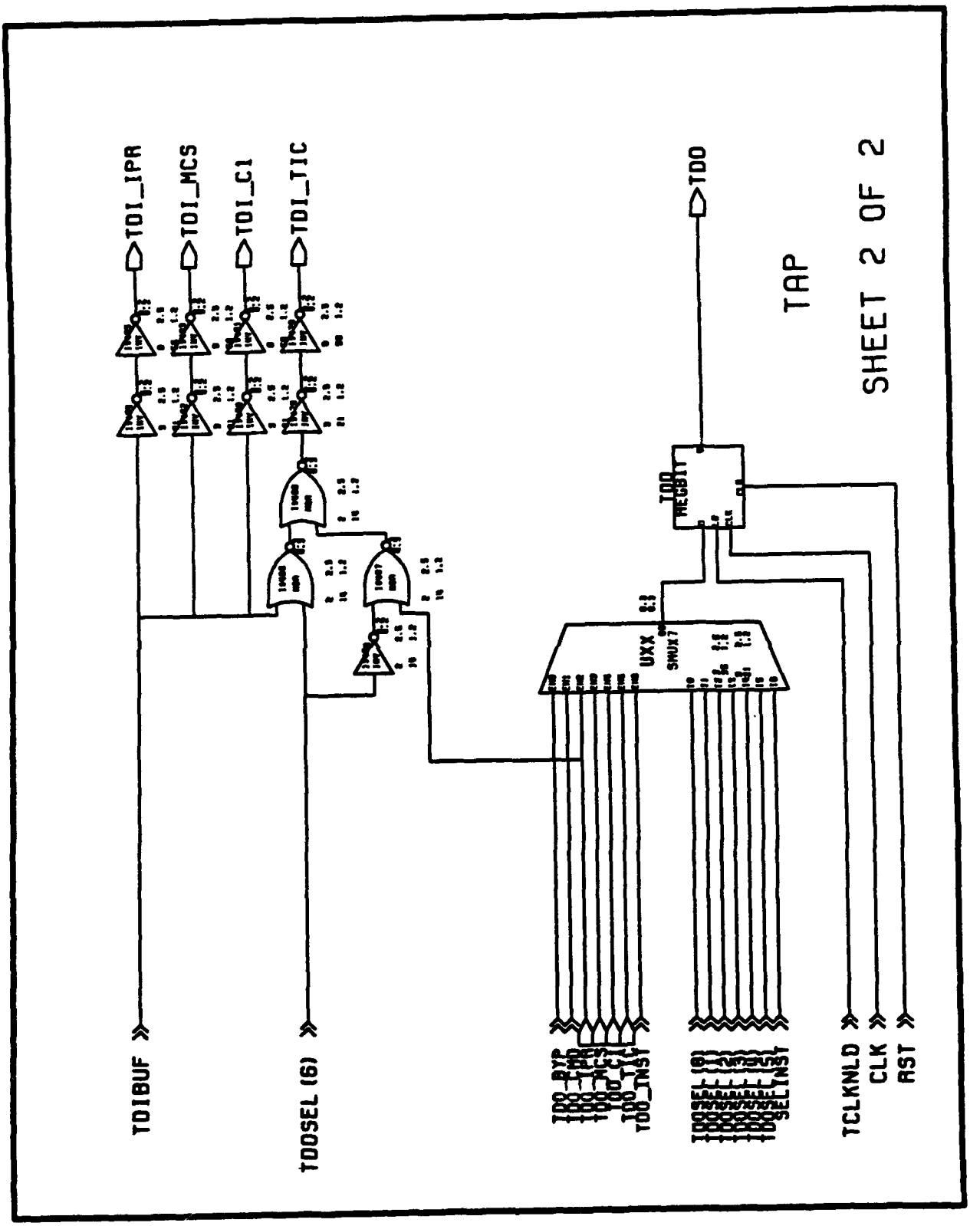

SQINVS
O0
4.5
1.5
I$22
50
1.2
I$21
I$422
1.3
1.5
6
1.2
CG
2.5
7.0
I$1
6.0
1.2
I$3
VTT
IO

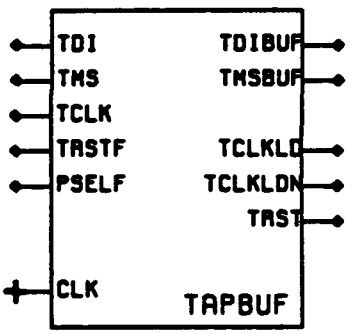

SYSCLK
SCLK(7:0)
HSYNC
MCLK

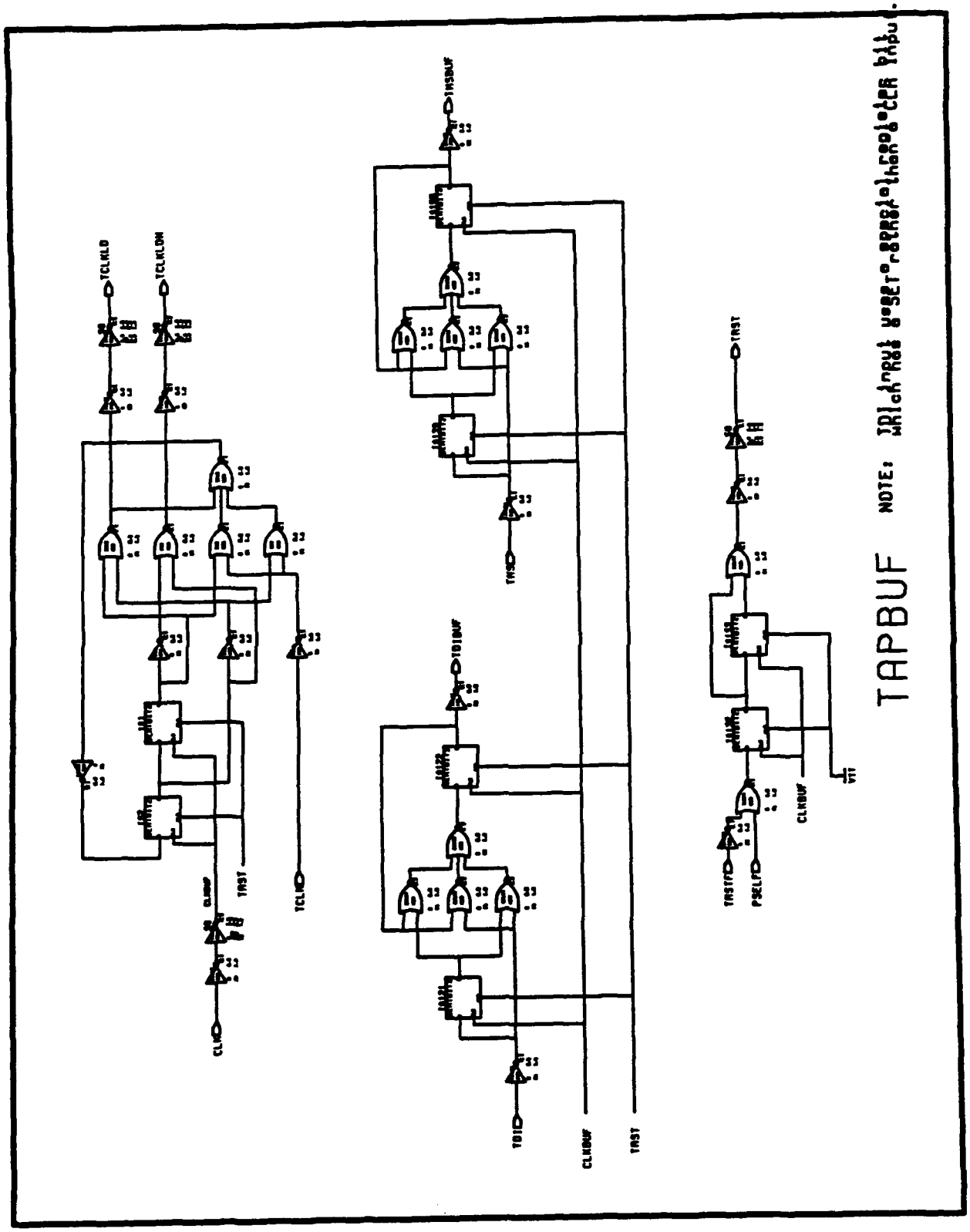

SYSCLK
SCLK (0)
SCLK (1)
SCLK (2)
SCLK (3)
SCLK (4)
SCLK (5)
SCLK (6)
SCLK (7)
MCLK
MSYNC

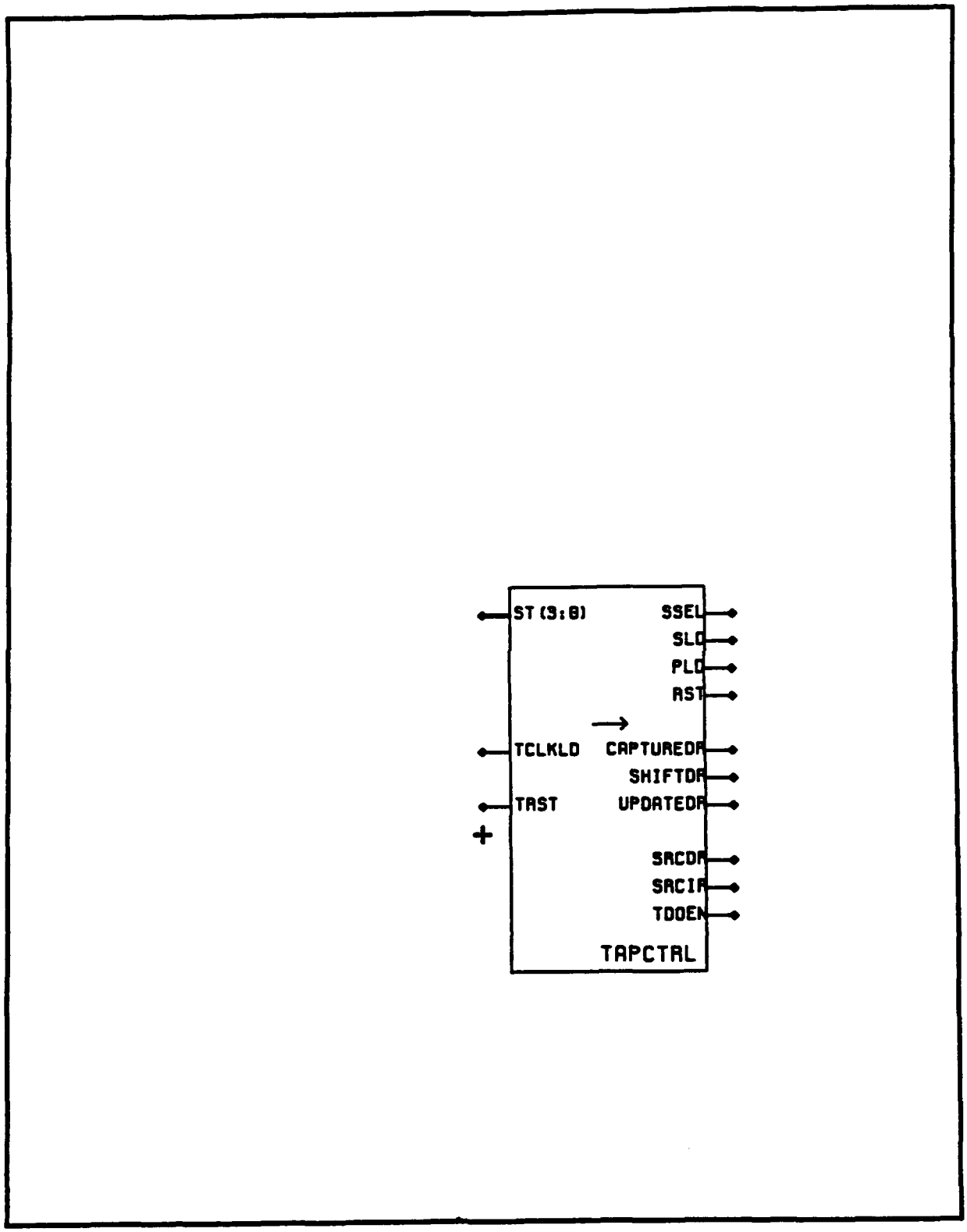

TDI
TMS
TRSTF
TCLK
PSELF
TDO_IPR
TDO_MCS
TDO_C1
TDO_TIC
CMP
CMDCLRF
CLK
TEST
TDO
TDOEN
BF(2:0)
TDI_IPR
TDI_MCS
TDI_C1
TDI_TIC
IPR(3:0)
MCS(5:0)
C1(4:0)
TIC(4:0)
HALT
PARDIS
OBPCLR
TAP

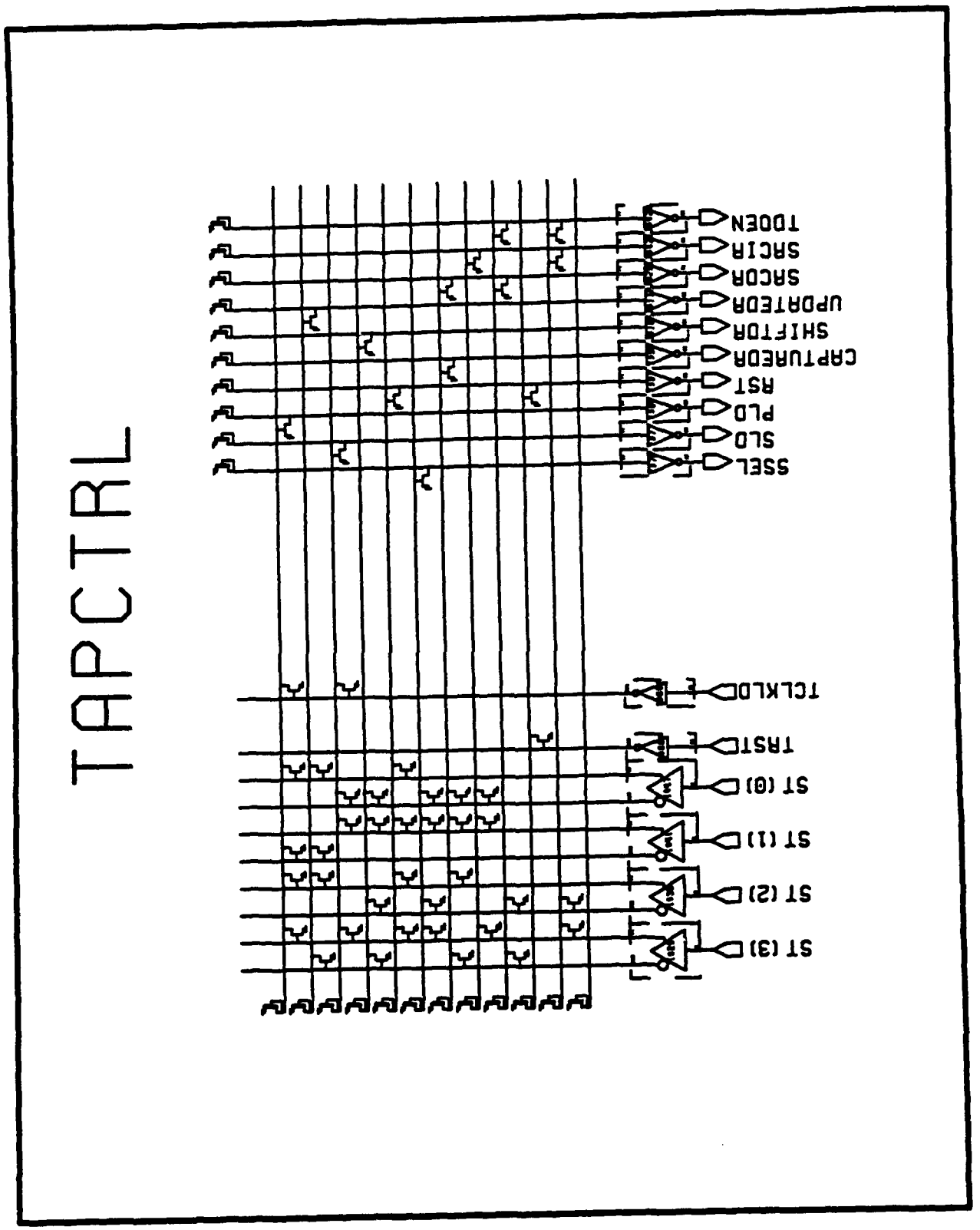

TAP
SHEET 1 OF 2
TDO_CMD
TDO_INST
TDO_BYP
RST
TCLKNLD
TDIBUF
TMSBUF
TRST
TCLKLD
CMP
CMDCLRF
TEST
CLK
CMD
INST
BYP
BUF
SM
SRCOR

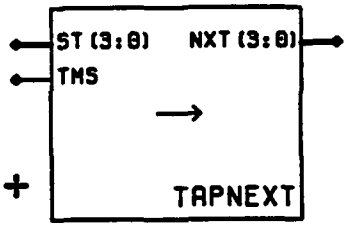

TDI_IPR
TDI_MCS
TDI_C1
TDI_TIC
TDO
TAP
SHEET 2 OF 2
TDIBUF
TDOSEL (6)
TCLKNLD
CLK
RST

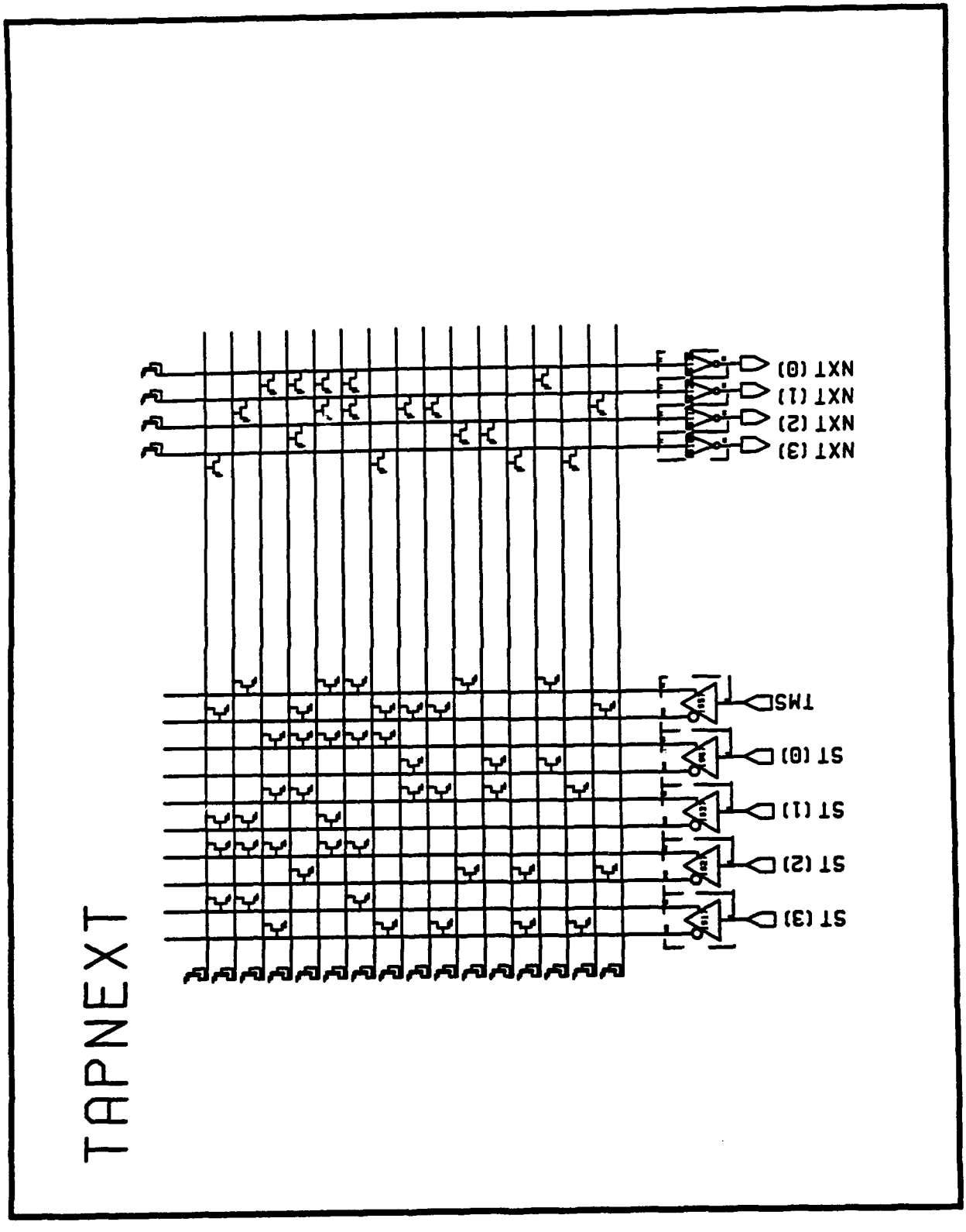

TDI
TMS
TCLK
TRSTF
PSELF
CLK
TDIBUF
TMSBUF
TCLKLD
TCLKLDN
TRST
TAPBUF

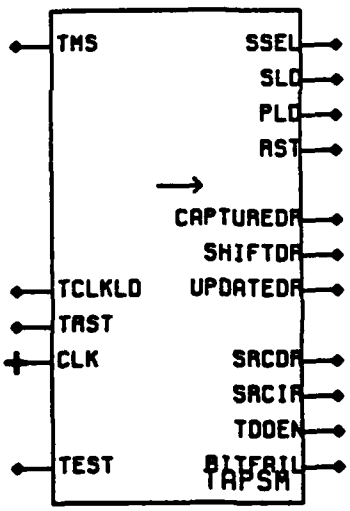

TAPBUF
TCLKLD
TCLKLDN
TRST
TCLKO
TDIBUF
TDIO
CLKBUF
TMSBUF
TMSO
TRSTFD
PSELFD
VII

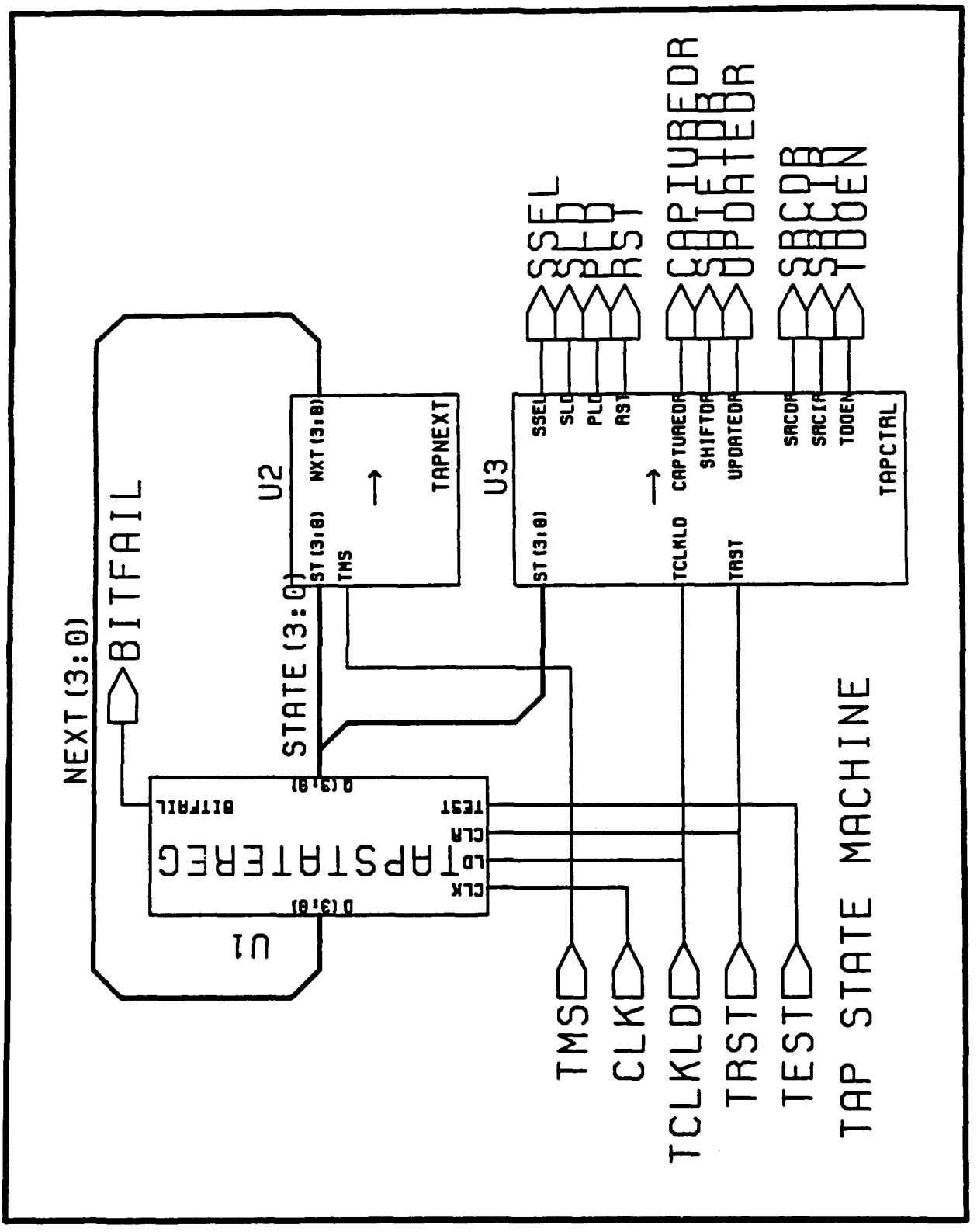

ST(3:0)
SSEL
SLC
PLC
RST
TCLKLD
CAPTUREDR
SHIFTDR
TRST
UPDATEDR
SRCDR
SRCIR
TDOEN
TAPCTRL

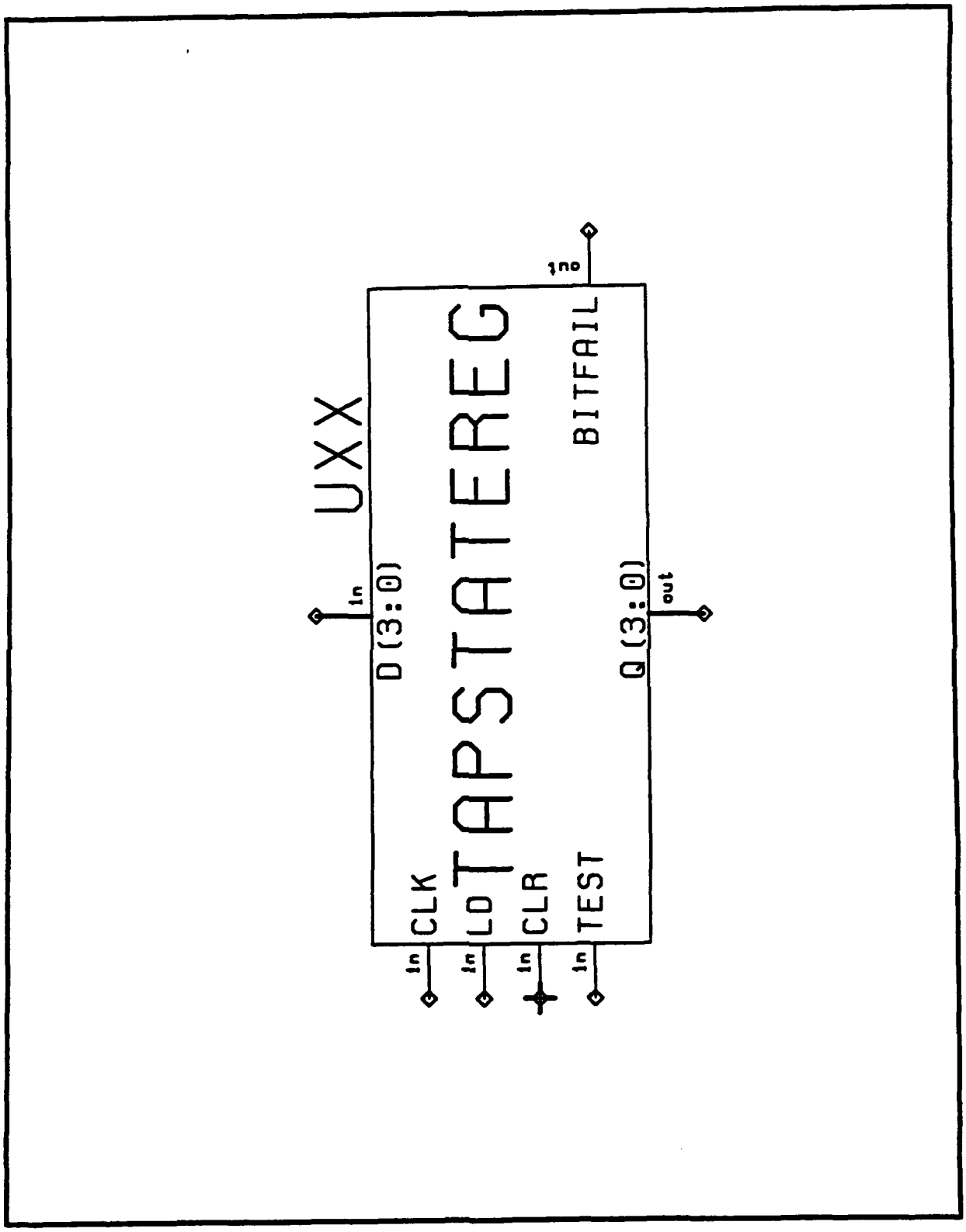

TAPCTRL
TDOEN
SRCIR
SRCOR
UPDRTEDR
SHIFTDR
CAPTUREDR
RST
PLO
SLO
SSEL
TCLKLD
TRST
ST(0)
ST(1)
ST(2)
ST(3)

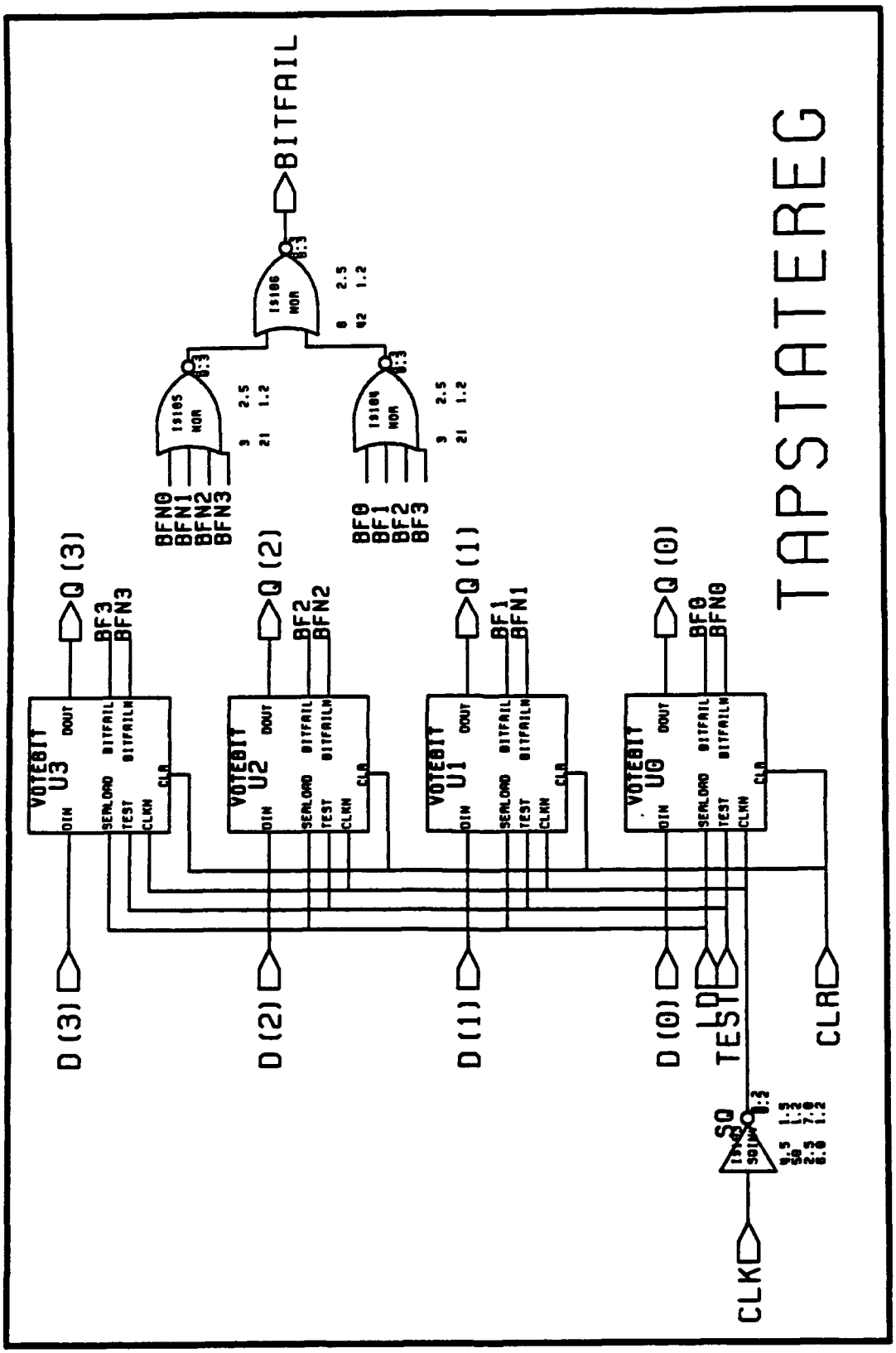

ST (3:0)
NXT (3:0)
TMS
TAPNEXT


TAPNEXT
NXT (0)
NXT (1)
NXT (2)
NXT (3)
TMS
ST (0)
ST (1)
ST (2)
ST (3)


TMS
SSEL
SLC
PLC
RST
CAPTUREDR
SHIFTDR
TCLKLD
UPDATEDR
TRST
CLK
SRCDR
SRCIR
TDOEN
TEST
BITFAIL
TAPSM


TAP STATE MACHINE
TMS
CLK
TCLKLD
TRST
TEST
SSEL
SLD
RST
CAPTUREDR
SHIFTDR
UPDATEDR
SRCDR
SRCIR
TDOEN
BITFAIL
NEXT(3:0)
STATE(3:0)
U1
U2
U3
TAPSTATEREG
TAPNEXT
TAPCTRL
NXT(3:0)
ST(3:0)
TMS
SSEL
SLD
PLD
RST
CAPTUREDR
SHIFTDR
UPDATEDR
SRCDR
SRCIR
TDOEN
TCLKLD
TRST
TEST
CLK


UXX
TAPSTATEREG
in
D(3:0)
out
Q(3:0)
out
BITFAIL
in
CLK
in
LD
in
CLR
in
TEST


TAPSTATEREG
BITFAIL
BFN0
BFN1
BFN2
BFN3
BF0
BF1
BF2
BF3
Q (3)
Q (2)
Q (1)
Q (0)
VOTEBIT
U3
U2
U1
U0
DIN
DOUT
SERLOAD
TEST
CLKIN
BITFAIL
BITFAILN
CLR
D (3)
D (2)
D (1)
D (0)
LD
TEST
CLR
SO
CLK

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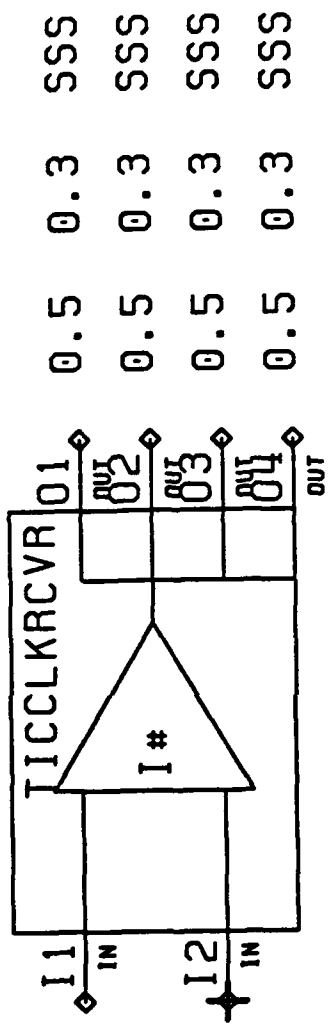
Version 0.8

NAME: CLKRCVR

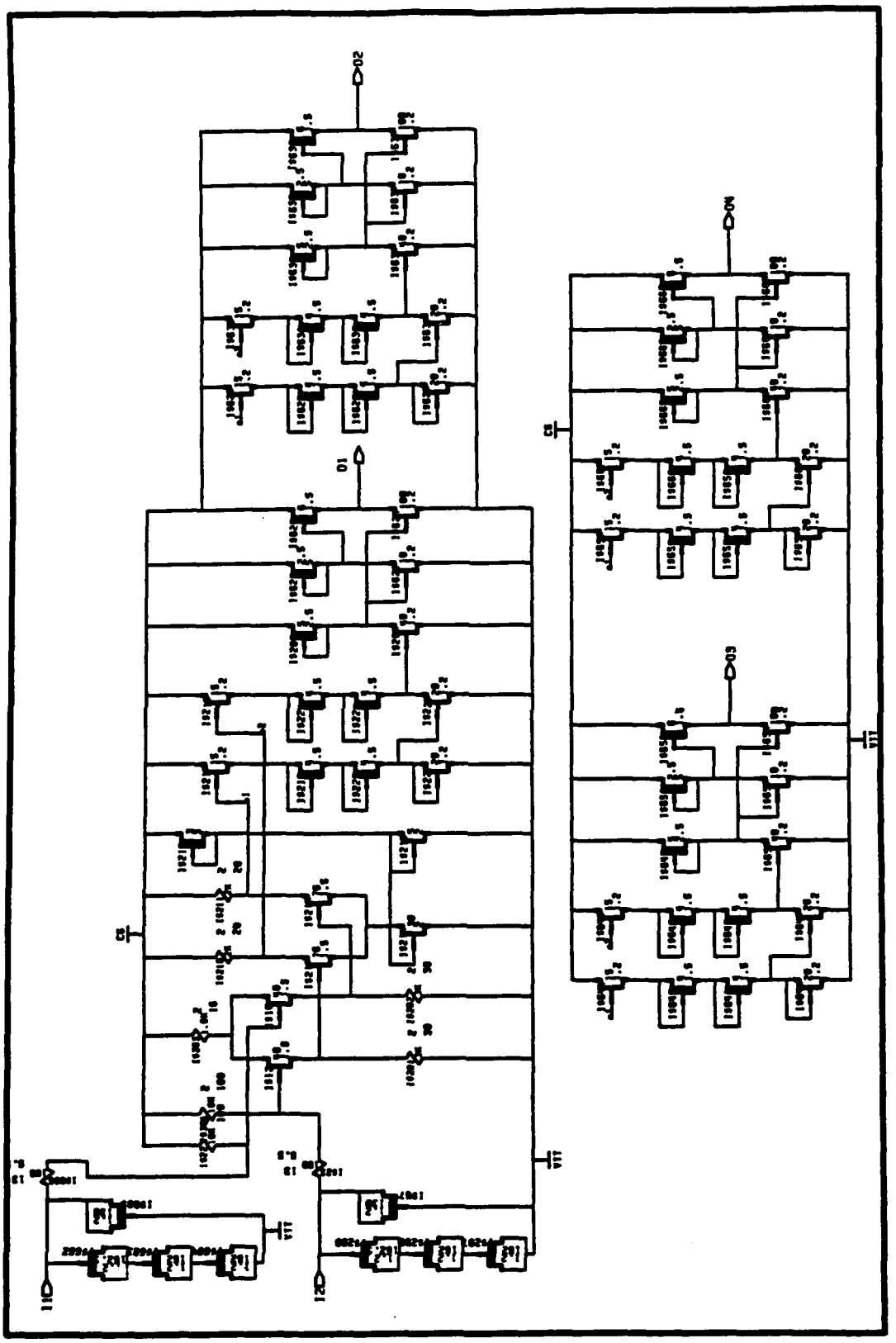
DESCRIPTION: DIFFERENTIAL INPUT CLOCK RECEIVER

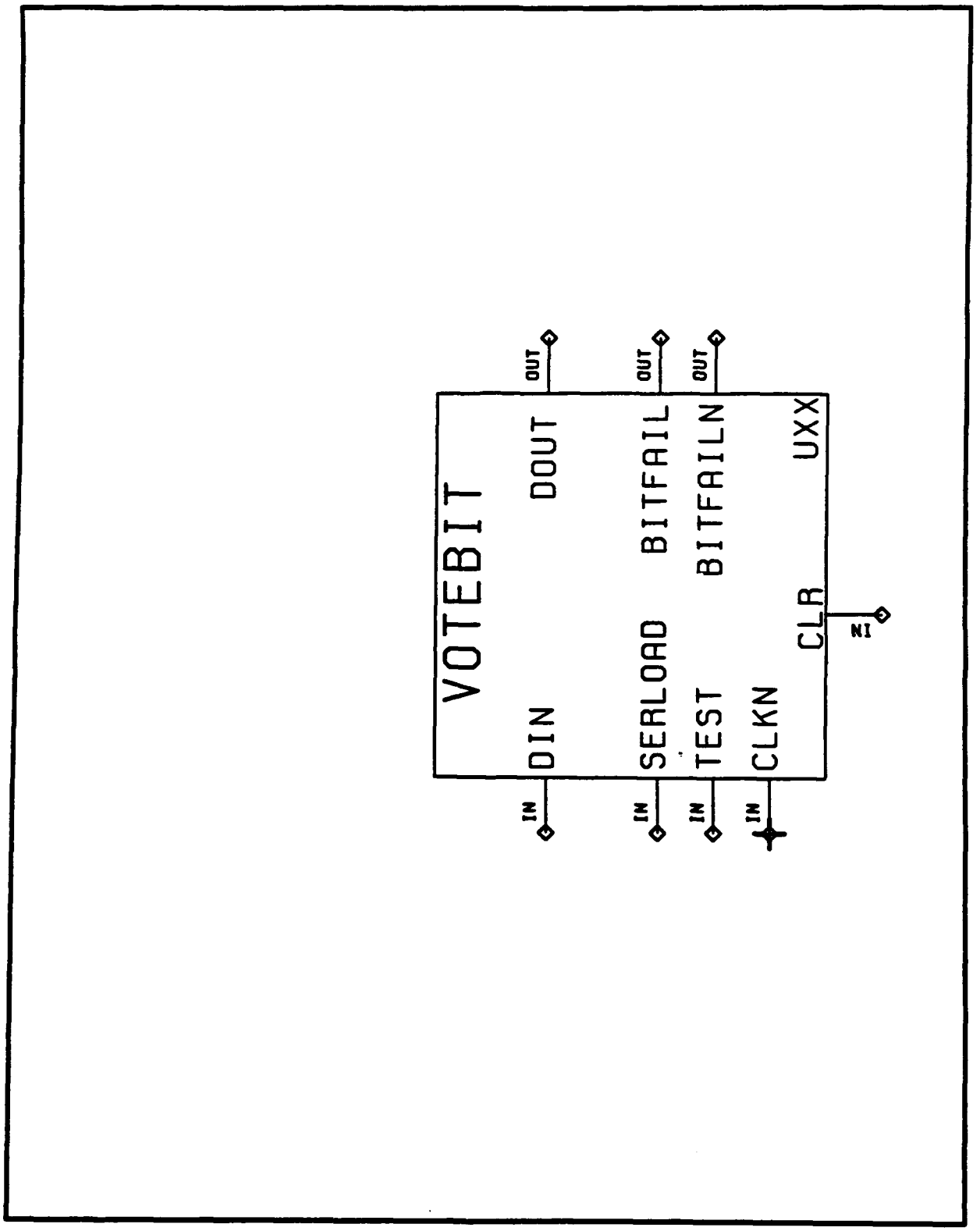


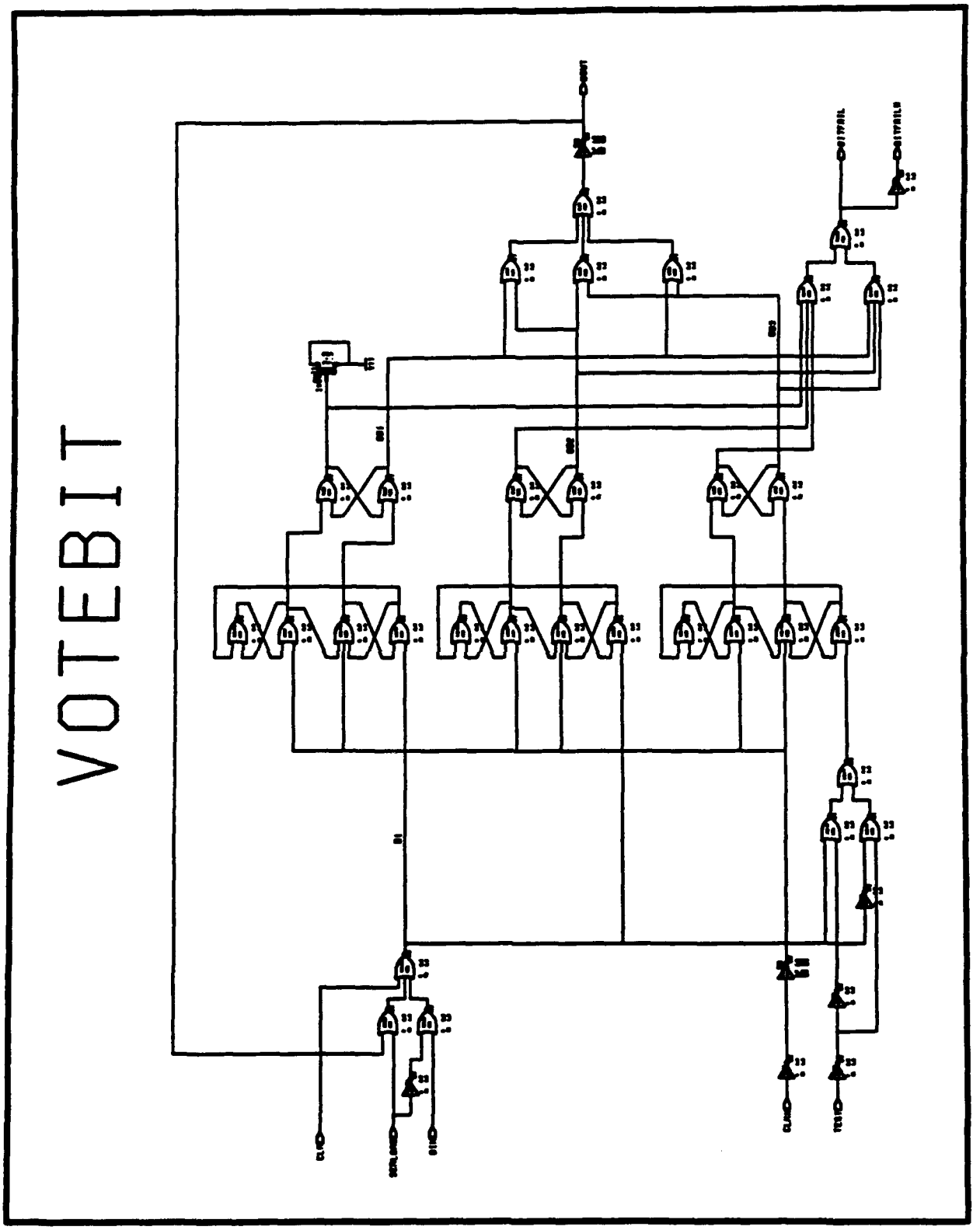
0.5	0.3	SSS	
0.5	0.3	SSS	
0.5	0.3	SSS	
0.5	0.3	SSS	

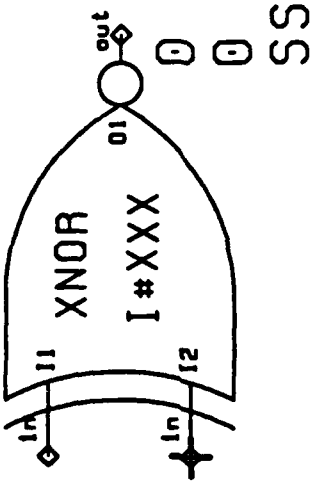
TICCLKRCVR

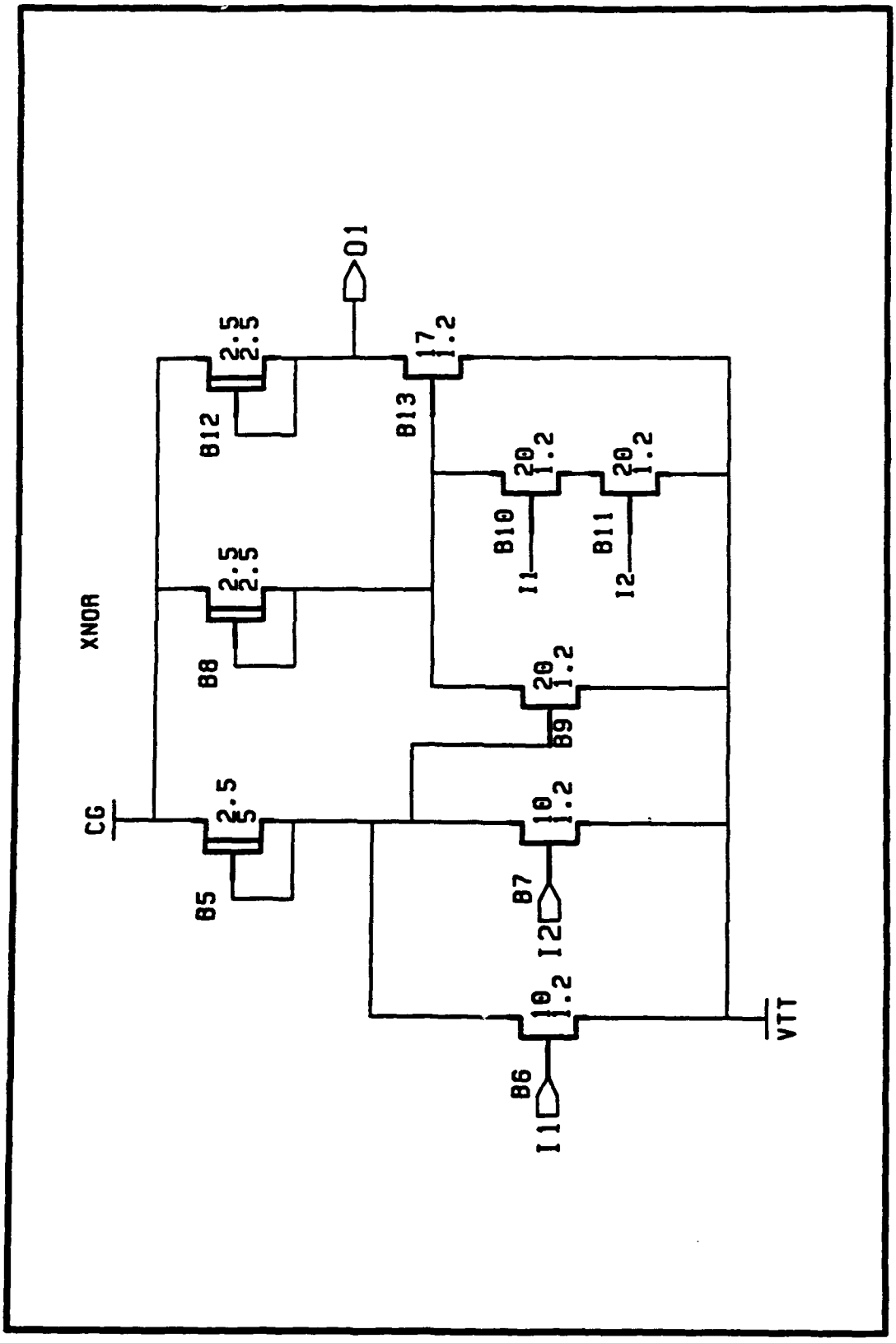
ticclkrcvr.bin




VOTEBIT
DOUT
BITFAIL
BITFAILN
UXX
DIN
SERLOAD
TEST
CLKN
CLR
OUT
OUT
OUT
IN
IN
IN
IN
NI


VOTEBIT


SSS
0
0
out
01
XNOR
I#XXX
11
12
In
In


O1
2.5
2.5
17
1.2
B12
B13
20
1.2
20
1.2
B10
B11
I1
I2
2.5
2.5
XNOR
B8
20
1.2
B9
CG
2.5
2.5
10
1.2
B5
B7
I2
10
1.2
VTT
B6
I1