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13. ABSTRACT (Maximum 200 words) The performance of digital VLSI signal processing and communications systems is often limited by the data conversion interfaces between digital system-level components and the analog environment in which those components are embedded. The focus of this program has been research into the fundamental nature of such interfaces in systems that digitally process high-bandwidth signals for purposes such as radar imaging, high-resolution graphics, high-definition video, mobile and fiber-optic communications, and broadband instrumentation. Effort has been devoted to the study of both generic circuit functions, such as sampling and comparison, and architectural alternatives relevant to the implementation of high-speed data converters in present and emerging VLSI technologies. Specific results of the research include the design and realization of novel low-power CMOS and BiCMOS sampled-data comparators operating at rates as high as 200 MHz, the exploration of various design approaches to the implementation of high-speed sample-and-hold circuits in CMOS and BiCMOS technologies, and the design of a subranging CMOS analog-to-digital converter that provides 12-bit resolution at a conversion rate of 10 MHz.					
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PROBLEM STUDIED

As a result of the increased circuit speeds and densities that accompany the continued scaling of semiconductor integrated circuit technologies, digital means of processing, storing, and communicating information are rapidly displacing analog alternatives across a broad spectrum of applications. Relative to analog implementations, digital signal processing and communications systems provide improved noise immunity, precision, and flexibility. In addition, they are both more amenable to design automation and easier to test.

The performance of digital signal processing and communications systems is generally limited by the data conversion interfaces between digital system components and the analog environment in which those components are embedded. The focus of this research program has been an investigation into the fundamental nature of these interfaces for applications requiring the digital processing of signals with video, and higher, bandwidths. Examples of such applications are radar imaging, high-resolution graphics, high-definition video, fiber-optic and mobile communications, and broadband instrumentation. Specific objectives of the research have included identifying the limitations VLSI technologies impose on the performance of data conversion interfaces and devising approaches to overcoming these limitations by means of novel architectures, circuits, and design methodologies. An important component of the program has been the fabrication and thorough characterization of monolithic experimental prototypes.

SUMMARY OF IMPORTANT RESULTS

The research in this program has addressed both architectural issues and generic circuit functions relevant to high-speed data conversion across a range of sampling rates and precision. In particular, considerable effort has been devoted to exploring two generic functions, *comparison* and *sampling*, that generally govern the performance achievable in an analog-to-digital converter. Both of these functions have been examined with respect to the engineering limitations various integrated circuit technologies impose on their implementation.

The realization of high-speed data conversion interfaces in present and emerging VLSI technologies, in particular CMOS and BiCMOS, has been emphasized in this work. Although CMOS has long since established itself as the mainstream VLSI technology, heretofore relatively little research has been directed toward exploring the implementation of analog

circuits operating at frequencies above a few tens of MegaHertz in this technology. For this reason, substantial effort was devoted to studying the CMOS implementation of data conversion circuits operating with modest precision (8 bits) at clock rates on the order of 100 MHz. The initial vehicle for this study was a high-speed regenerative comparator integrated in a 2- μ m CMOS technology. The results of this work were, in part, intended to serve as a baseline against which future research accomplishments could be measured.

The highest speed monolithic data converters have, for the most part, been realized using silicon bipolar technology. This dominance stems largely from the suitability of bipolar transistors for providing low-noise amplification over large bandwidths. However, scaled CMOS technologies offer their own set of unique advantages with respect to the implementation of high-speed sampled-data circuits; namely, fast analog switches with zero offset, high-impedance charge storage nodes, and complementary transistors. These attributes allow for the extensive use of analog sampling, pipelining, and multiplexing, as well as offset cancellation and self calibration, in order to improve the speed and precision with which functions such as comparison can be performed.

The basic function of a comparator is that of providing amplification sufficient to generate digital output levels in response to small differences between two analog input signals. This amplification need not be linear nor continuous in time. However, for use in applications such as fully parallel analog-to-digital converters it must be accomplished as quickly as possible and at an economy of power and silicon area. Based on the study of various approaches to comparator design it was concluded that, in order to achieve the minimum delay and power-delay product, the required amplification was best obtained by means of regeneration [1]. However, the implementation of the comparator function directly by means of regeneration poses severe offset and overdrive recovery problems. Research was initiated into methods by which these difficulties could be overcome, and this effort culminated in the successful design and implementation of a CMOS sampled-data comparator based on a pipelined cascade of regenerative sense amplifiers [2,4].

The regenerative CMOS comparator was integrated in a 2- μ m CMOS gate array technology. This circuit was experimentally found to operate at sampling rates of over 100 MHz and maintain a resolution of at least 8 bits at rates as high as 40 MHz. The comparator dissipates less than 4 mW from a single 5-V supply, thus making it suitable for use in fully parallel (flash) A/D converters, as well as a variety of instrumentation and communications systems wherein low power dissipation is essential.

Among the difficulties revealed by the research into the design of high-speed sampling CMOS comparators were the relatively large input capacitance, poor rejection of common-mode transients at the inputs, and clock feedthrough within the regenerative sense amplifier. In response to these concerns, we began to explore the use of BiCMOS technology for performing high-speed comparisons. Owing to the performance advantages it provides in applications such as high-speed static memory and semi-custom digital circuits, BiCMOS appears likely to establish itself as a mainstream technology for VLSI. The emergence of this technology offers new opportunities to improve the performance of analog, as well as digital, integrated circuits through a combination of the distinct, and complementary, advantages of bipolar and MOS technologies.

Through the use of BiCMOS we expected that high-speed comparison to an accuracy of at least 8 bits could be achieved by means of regeneration without either preamplification or offset cancellation. This research led to the design of a low-power comparator that combines MOS sampling at the input with a cross-coupled bipolar differential pair that provides regenerative amplification by means of charge steering [6,10]. During sampling the bipolar pair is held inactive by opening the common emitters of the pair while the sampled signals establish a voltage imbalance at the input. The sampled input imbalance is then amplified by using MOS switches and capacitors to transfer a fixed quantity of charge through the bipolar pair from their common emitter node to the collector outputs. The bipolar pair dissipates no static power, and in the sampling mode it drains no current from the capacitors on which the input samples are stored.

An experimental realization of the charge-steering BiCMOS comparator was integrated in a 1- μ m BiCMOS technology and shown to provide comparisons accurate to 8 bits at clock rates as high as 200 MHz. The circuit operates from a single 5-V supply and dissipates only 1.6 mW at the maximum comparison rate. The comparator thus functions at speeds approaching those achievable in conventional bipolar designs while dissipating substantially less power.

Within this program significant effort has also been devoted to investigating the potential of BiCMOS technology for extending the performance of monolithic *sampling* systems. The increasing interest in digitizing high-resolution video signals has stimulated the demand for monolithic track-and-hold amplifiers operating at video frequencies with a precision of at least 10 bits. Such circuits are essential in both multistage and fully parallel high-speed A/D converters. In multistage architectures it is typically necessary to sample and hold the analog

input for several clock cycles to within the accuracy of the overall converter. In fully parallel converters, the use of a track-and-hold amplifier reduces aperture and sampling time uncertainties while easing the demands on the quantizer itself.

High-performance track-and-hold circuits have traditionally been implemented in hybrid technologies that incorporate components such as Schottky-diode bridges for use as sampling switches and step recovery diodes. Our research focussed initially on an investigation into means of providing a fully monolithic alternative to such hybrid implementations that was suitable for use either in stand-alone applications or integrated within combined analog and digital video signal processing systems [8]. This effort led to the design and implementation of a monolithic BiCMOS track-and-hold amplifier with performance that is competitive with hybrid alternatives and surpasses that of previously reported monolithic designs by nearly two orders of magnitude [5,7]. In order to achieve an accuracy of at least 10 bits, a closed loop topology was adopted and then BiCMOS circuits were used to mitigate the bandwidth limitations of this configuration. The amplifier comprises an NMOS sampling switch, two BiCMOS folded-cascode transconductance amplifiers with unity-gain bandwidths of 250 MHz [3], a class AB output buffer capable of driving a 50- Ω load, and a BiCMOS switch driver that provides 1-nsec transitions between ± 4 V. When integrated in a BiCMOS technology with 1.2- μm design rules and a peak bipolar transistor f_t of 7 GHz, the overall track-and-hold circuit was shown experimentally to settle to an accuracy of at least 10 bits within an acquisition time of 15 nsec.

In general, open loop architectures provide the fastest implementation of the sampling function. However, amplifier offsets and switch errors in typical open loop configurations appear unattenuated when referred to the input, thereby severely limiting the achievable precision. In high-speed applications, the need for maximum acquisition bandwidth dictates the use of a large sampling switch, a small hold capacitance, and fast clock transitions; however, these constraints result in large, input dependent pedestal errors in the hold mode. Therefore, we began to explore several approaches to improving the accuracy of open loop sampling circuits, focussing especially on reducing the pedestal error. In one of these approaches, the input signal is sampled onto a capacitance that is small in the tracking mode, but is increased to a significantly larger value by means of Miller feedback during the transition to the hold mode [9,11].

A sample-and-hold circuit in which the equivalent hold capacitance is increased through the use of Miller feedback was successfully designed and integrated in a 1- μm CMOS technology. Experimental measurements confirm that an order-of-magnitude reduction in the input-

dependent pedestal error was achieved with this design. The circuit was shown to settle to an accuracy of 8 bits in an acquisition time of 5 nsec. Although the approach was demonstrated in a scaled CMOS technology, it has potential application in other technologies as well.

In addition to our research into the generic functions of comparison and sampling, we have also investigated architectures and circuit design approaches for digitizing radar and high-resolution video signals. In particular, we have focussed on data acquisition interfaces for quantizing signals with resolutions between 10 and 14 bits at sampling rates ranging from a few MegaHertz to more than 50 MHz. Although the state-of-the art in data conversion is often thought of in terms of digitizing signals with a precision of 4 to 6 bits at sampling rates of 1 GHz or more, the problem of providing 12-bit digitization at sampling rates on the order of 10 MHz is at least as, and perhaps more, challenging. Above a resolution of 8 bits, something other than a fully parallel approach must be used, and for better than 10-bit precision, error correction is essential. These constraints, as well as the simple need for longer settling, impose severe limitations on the achievable conversion bandwidth.

Conceptually, the same progress in fabrication technology that provides for continuing increases in the sampling rate at which low-resolution A/D conversion can be accomplished can also be exploited to increase the precision with which signals can be digitized at lower rates. At lower sampling rates, a variety of architectural approaches are possible, including multistage, subranging, and folding converters wherein varying degrees of analog and digital pipelining can be employed. Our initial efforts have been directed toward the study of subranging architectures and the potential for improving the performance achievable in CMOS and BiCMOS implementations of such topologies. Of particular interest is a two-stage subranging configuration that avoids the use of precision subtractors. In one approach being studied, self-calibration is used in the first stage to greatly relax the resolution, linearity, and settling requirements in the second stage. An implementation of this approach has been designed and integrated in a 1- μ m CMOS technology, and is presently being evaluated.

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