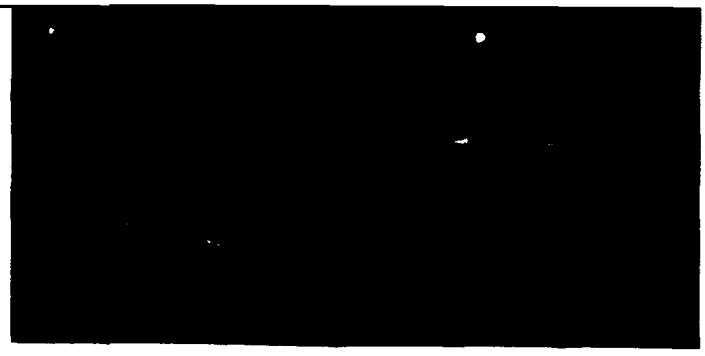
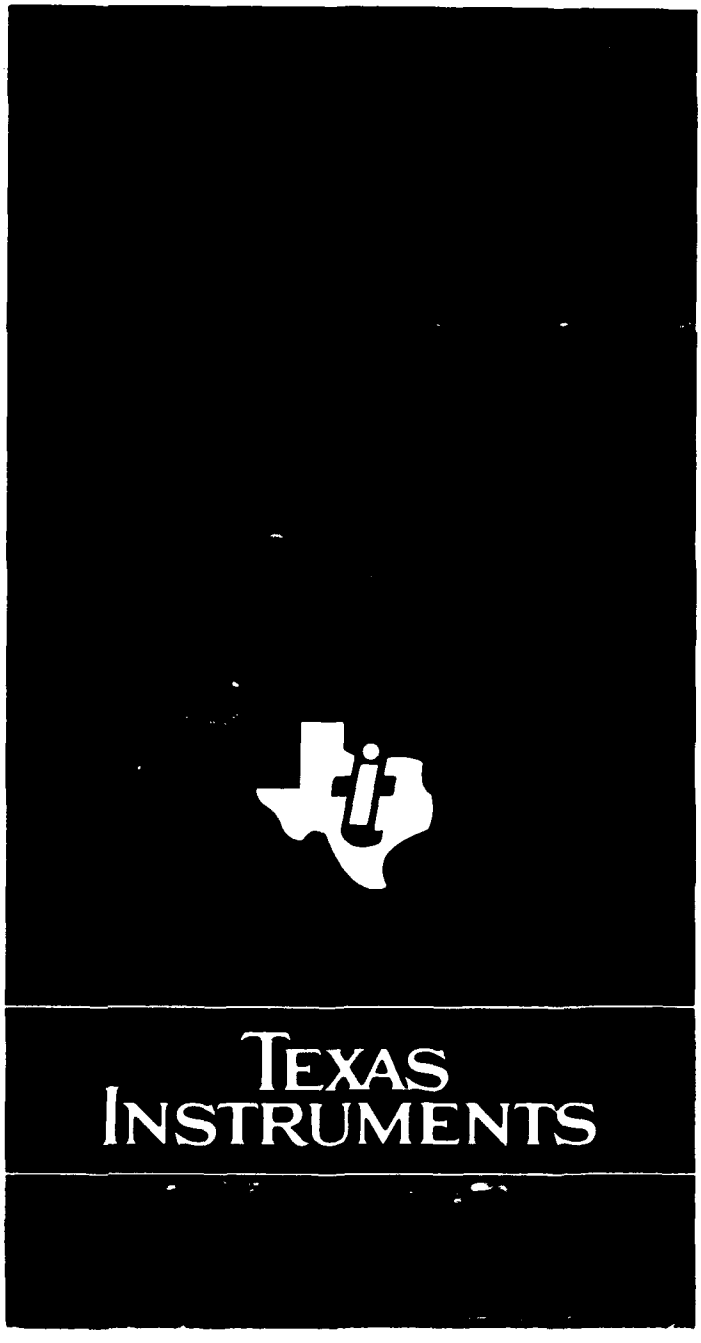


SILICON WAFER ADVANCED PACKAGING (SWAP)

MULTICHIP MODULE (MCM) FOUNDRY STUDY
FINAL REPORT
(VERSION 2)

OCTOBER 1990 - MARCH 1991



TEXAS INSTRUMENTS

SILICON WAFER ADVANCED PACKAGING (SWAP)

MULTICHIP MODULE (MCM) FOUNDRY STUDY
FINAL REPORT
(VERSION 2)

OCTOBER 1990 - MARCH 1991

Prepared for and sponsored by:

Defense Advanced Research Projects Agency
Defense Manufacturing Office
ARPA Order No. 7549
Issued by DARPA/CMO under Contract #MDA972-90-C-0045

Prepared by:

General Electric
and
Texas Instruments Incorporated
13500 N. Central Expressway
Dallas, Texas 75266

TEXAS INSTRUMENTS

8 April 1991

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION Unclassified	1b. RESTRICTIVE MARKINGS N/A
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE Date Month Year	
4. PERFORMING ORGANIZATION REPORT NUMBER(S) SWAP001-AC	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION Texas Instruments 6b. OFFICE SYMBOL (If applicable)	7a. NAME OF MONITORING ORGANIZATION Defense Advanced Research Project Agency (DARPA)
6c. ADDRESS (City, State, and Zip Code) 13536 N. Central Expressway P.O. Box 655012 Dallas, TX 75265	7b. ADDRESS (City, State, and Zip Code) 1400 Wilson Blvd. Arlington, VA 22209-2308
8a. NAME OF FUNDING/SPONSORING ORG DARPA 8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c. ADDRESS (City, State, and Zip Code) 1400 Wilson Blvd. Arlington, VA 22209-2308	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO. / WORK UNIT ACCESSION NO.
11. TITLE (Include Security Classification) Silicon Wafer Advanced Packaging (SWAP) Multichip Module (MCM) Foundry Study	
12. PERSONAL AUTHOR(S) Written with the cooperation of the TI/GE Technical Team: Larry Mowatt, Frank Henry, Mark Avery, Porter Sadler, Mark Eskew, Lynn Roszel, (Continued on page 2)	
13a. TYPE OF REPORT Final	13b. TIME COVERED FROM 10/90 TO 3/91
14. DATE OF REPORT (Year, Month, Day) 8 April 1991	15. PAGE COUNT
16. SUPPLEMENTARY NOTATION	

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

MCM technology is crucial to maintaining the competitive position of the U.S. electronics industry - military and commercial. The driving force is performance, and MCM users will seek off-shore suppliers if capabilities are lacking. In the long term, low-cost overseas capabilities will make their way into the U.S. military market and put it at risk.

The proven GE-HDI MCM technology was developed with combined government and GE funding, and its chips first approach offers the lowest non-recurring cost. Rapid prototyping, high performance, and technology flexibility are characteristic, and the potential exists for extension to high-volume.

(Continued on page 2)

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT ☐ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT. ☐ DTIC USERS	21. ABSTRACT SECURITY CLASSIFICATION UNCLASSIFIED	
22a. NAME OF RESPONSIBLE INDIVIDUAL Larry Mowatt	22b. TELEPHONE (Include Area Code) (214) 995-1287	22c. OFFICE SYMBOL

DD FORM 1473, 84 MAR

00. TITLE (Continued)

12. (Continued)

Dave Counts, Bob Raulerson, Dave Walter, Wolfgang Daum, Ed Bernard, Charles Becker, Ray Fillion, Bill Elkington, Glenn Forman, Bernard Gorwitz, Bill Hatfield, G.E. Personnel.

19. (Continued)

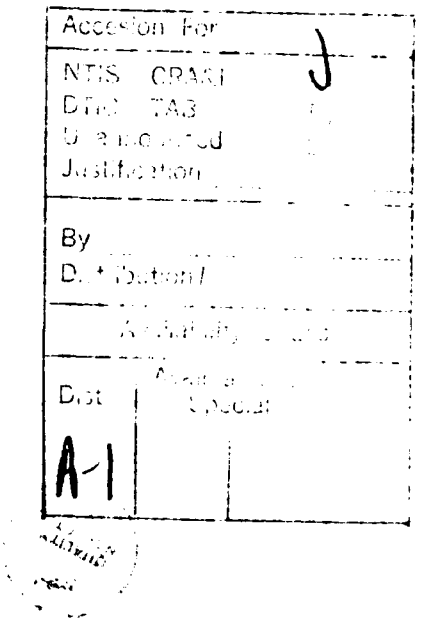
GE's research and TI's applications engineering experience and worldwide marketing infrastructure provide the base for foundry implementation.

Technology enhancements supporting implementation include an integrated foundry automation system and 20 manufacturing enhancements enabling high-volume production. TI's 3-D memory packaging capability will be integrated with GE-HDI providing systems level advantages. The potential impact of these applied manufacturing improvements for DoD is $200M or greater.

TI and GE recommend that DARPA integrate the Merchant MCM Foundry program and SWAP follow-on programs. When combined, these address the total MCM technology insertion challenge - rapid prototyping and high-volume.

ACRONYM LIST

AHDL	-	Analog Hierarchical Description Language
AI	-	artificial intelligence
AIN	-	aluminum nitride
AME	-	advanced microelectronics
AOQ	-	average outgoing quality
ATE	-	automated test equipment
ATPG	-	automatic test pattern generation
BCB	-	benzocyclobutenes
BILBO	-	Built-In-Logic-Block-Observer
BIST	-	built-in self-test
BIT	-	built-in-test
BSDL	-	boundary scan description language
CA	-	Cellular Automate
CAD	-	computer aided design
CAM	-	computer aided manufacturing
CAE	-	computer aided engineering
CALCE	-	computer aided life cycle engineering center
CARMA	-	computer aided reliability and maintainability applications
CAT	-	computer automated test
CEPCO	-	Coors Electronic Packaging Company
CFI	-	CAD framework initiative
CIM	-	computer integrated manufacturing
CM	-	conformance modules
CMP	-	Chip Model Library
COB	-	chip-on-board
CTE	-	coefficient of thermal expansion
CVD	-	chemical vapor deposition
DA	-	design automation
DEC	-	Digital Equipment Corporation
DFT	-	design for testability
DMCS	-	Data Management Control System
DPE	-	Digital Pin Electronics
DSEG	-	Defense Systems & Electronics Group
DUT	-	device-under-test
ECN	-	engineering change notice
EDI	-	electronic data interchange
EDIF	-	Electronic Data Interchange Format
FIT	-	failures in time
FTP	-	file transfer process
GDSII	-	autocad format
GE	-	General Electric
HDI	-	high density interconnect
HYPACK	-	high density high frequency hybrid interconnection software package for digital circuits



ACRONYM LIST (Continued)

HYPLACE	-	high density placement (GE)
IC	-	integrated circuit
IGES	-	Initial Graphs Exchange Specification
IITRI	-	Illinois Institute of Technology Research
"ILITIES"	-	testability, producibility, reliability, manufacturability
JIT	-	just-in-time
LAN	-	local area network
LEGGEN	-	legend generation
LFSR	-	Linear Feedback Shift Registers
LSSD	-	level sensitive scan design
MCM	-	multichip module
MDT	-	Manufacturing Defects Testing
MEPL	-	master engineering parts library
MISR	-	multiple input signature register
MMST	-	Microelectronic Manufacturing Science & Technology
MOE	-	metal on elastomer
MOSFET/BJT	-	metal oxide field effect transistor/bipolar junction transistor
PCM	-	process control monitor
PDCS	-	Product Data Control System
PDS	-	packaging design system
PLA	-	programmable logic array
PML	-	part model library
PPGEN	-	pick and place generation
PRPG	-	Pseudo Random Pattern Generation
PSA	-	Parallel Signature Analysis
PWB	-	printed wiring board
QC	-	quality control
QML	-	qualified manufacturers list
QRA	-	quality reliability assurance
R&M	-	reliability and maintainability
RAC	-	reliability analysis center
RADC	-	Rome Air Development Center
RAM	-	random access memory
RIE	-	reactive ion etch
ROM	-	read only memory
SC	-	semiconductor
SDRC	-	structural dynamics research corporation
SEC	-	standard evaluation circuit
SEMI	-	Semiconductor Equipment and Materials International
SMT	-	Surface Mount Technology
SNL	-	Sandia National Laboratory
SOI	-	silicon on insulator
SOS	-	silicon on silicon
SPC	-	Statistical Process Control

ACRONYM LIST (Continued)

SPICE	-	simulation program with integrated circuit emphasis
SRL	-	level sensitive scan design shift register latches
TAP	-	test access port
TEG	-	test element group
TM	-	test maintenance
TQC	-	Total Quality Control
TSSI	-	Test Systems Strategies, Inc.
TTC	-	test technology center
UACSL	-	University of Arizona coupled line simulator with linear terminations
UAMOM	-	University of Arizona methods of moments
UANTL	-	University of Arizona simulator for nonlinearity terminated transmission line network
UAPDSE	-	University of Arizona Package Design Support Environment
VAC	-	University of Arizona capacitance calculator
VER	-	verification system (TI)
VHDL	-	VHSIC Hierarchical Description Language
WIP	-	work-in-process
WSI	-	wafer scale integration

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF TABLES

EXECUTIVE SUMMARY

MCM technology is crucial to maintaining the competitive position of the U.S. electronics industry in both military and commercial applications. The driving force for MCM insertion is increasing system performance requirements. Initial high volume manufacturing demand will be in commercial market segments. Pressure to maintain performance requirements will drive users to off shore suppliers if cost effective domestic capability is not available. Without volume demand to drive down manufacturing costs, domestic merchant suppliers will be limited to the high end, lower volume segments of the military and commercial markets. In this event, low cost overseas capabilities will penetrate the U.S. domestic and military markets, putting the U.S. based military electronics industry at risk. The DoD can expect to gain a price advantage from this technology only through domestic competence in high volume manufacturing of MCMs.

The SWAP market study indicates that MCMs are clearly the next generation system-level packaging solution. Rapid development of domestic foundry capability is necessary to keep abreast of the predicted market growth in the military, automotive, computer, telecommunication, and consumer segments. The window for initial market penetration is in the late 1992-1994 period.

The proven GE-HDI overlay MCM technology was developed with combined DARPA, Air Force, and GE funding. This "chips first" approach offers the lowest non-recurring cost and is ideal for low volume manufacturing. Advantages of this technology are capability for rapid prototyping, high performance, and applications flexibility. Tremendous potential exists for extension to high-volume, low cost manufacturing to meet the approaching market demands.

TI and GE have formed a strategic business alliance to implement a MCM foundry owned by TI based on the GE HDI overlay interconnect technology. TI and GE bring complementary strengths to this challenge. GE's strength in research and development, and TI's strengths in applications engineering, manufacturing expertise, and worldwide marketing infrastructure provide a strong team for foundry implementation. Also, an initial group of universities, national laboratories, systems manufacturers, and suppliers have been identified to complement this base.

TI's Custom Manufacturing Service (CMS) Division currently provides Surface Mount Technology (SMT) manufacturing and assembly services to a portfolio of customers worldwide. This organization has in place a worldwide infrastructure to support product marketing and customer interface needs. The commercialization of the MCM foundry as a part of the CMS organization will be a natural extension of TI's existing custom manufacturing business.

The award by DARPA of the Merchant MCM Foundry program to the TI/GE team recognizes the strengths of this team and the HDI overlay technology. This program will result in technology transfer into a low volume facility at TI. The resulting facility will be ideally positioned to evolve into the high volume, low cost objective of the SWAP program.

Technology enhancements identified during this study include an integrated foundry automation system supporting the total design, manufacture, and test process and over 20 manufacturing enhancements that enable high-volume production. TI's 3-D memory packaging capability, developed with DARPA funding, will be integrated with GE-HDI technology, providing systems level packaging and performance advantages. System-level packaging solutions integrating the best elements of the "chip first" and "chip last" technologies are the next logical step. Near-term high-volume manufacturing barriers will be overcome by maturing processes and materials. The potential impact of these applied manufacturing improvements for DoD is $200M or greater.

TI and GE recommends that DARPA integrate the Merchant MCM Foundry program and SWAP follow-on programs. When combined, these address the total MCM technology insertion challenge - rapid prototyping, high performance, and high volume manufacturing. It is recommended that DARPA sponsor insertion programs to transition production MCM technology into program offices. Candidates for such programs include SADARM, ATCURE, ALLADIN, LH, and ATF.

1.0 INTRODUCTION

1.1 TI/GE SWAP TEAM OVERVIEW

TI/GE, industry suppliers, national laboratories, universities, and systems houses have contributed to the Silicon Wafer Advanced Packaging Program (SWAP) study effort. This team participated in program reviews, contributed to the report, reviewed the results, and submitted proposals and plans for support of the follow-on program.

1.1.1 TI Team

The TI team consists of Larry Mowatt (Program Manager), Mark Avery, David Counts, Mark Eskew, Frank Henry, Bob Raulerson, Lynn Roszel, Porter Sadler, and David Walter. This group worked closely with GE to understand the GE-HDI technology, defined high-volume production enhancements, planned the technology transfer, performed marketing surveys, and was responsible for coordination of the SWAP report.

1.1.2 GE Team

The GE team consists of Charles Becker, Ed Bernard, Wolfgang Daum, Ray Fillion, Glenn Forman, Bernard Gorwitz, Ted Haller and Bill Hatfield. The GE team worked closely with TI in sharing their knowledge of the GE-HDI process, furnished documentation, defined system enhancements, and contributed to the SWAP report.

1.1.3 Industry Suppliers/Systems Houses

The TI/GE team gratefully acknowledges the participation and contributions of its industry team members and others in the execution of the SWAP study program:

Alliant Techsystems
Boeing Aerospace and Electronics
BPA
Ceramics Process Systems
Digital Equipment, Inc.
ElectroniCast Corporation
Illinois Institute of Technology Research Institute
Layout Concepts, Inc.
Martin Marietta Missile Systems
Mentor Graphics, Inc.
Sandia National Laboratories
Sun Microsystems, Inc.
Task Technologies, Inc.
Techsearch International, Inc.
University of Arizona
University of Maryland
W.R. Grace and Coors Ceramic
Wright Laboratories WL/EL

1.1.4 National Laboratories

Sandia National Laboratories, represented by Dave Palmer, participated in SWAP reviews, furnished input on their test research, and helped define approaches to MCM test.

1.1.5 Universities

The University of Arizona, under the direction of Dr. John Prince, defined a plan for enhancing existing MCM tools, developed under GE's guidance, that support high-speed electrical and thermal/electrical analysis.

The University of Maryland, under the direction of Dr. Michael Pecht, submitted a proposal for enhancing CALCE reliability and maintainability to meet MCM requirements.

1.2 MCM FOUNDRY VISION

1.2.1 Overview

Multi Chip Module (MCM) packaging is the next logical step in advanced packaging development. Although being used in several different forms by various companies throughout the world, the technology is in its infancy in commercial use of this high density packaging approach is small. Much of the current production of MCMs is in a captive form internal to the user company. Growth potential is enormous for commercial and military use - there is a definite market gap which a viable MCM product will fill. Whether or not the MCM technology can intercept a large share of the high density packaging market need will be a function of how quickly industry can develop the engineering expertise, design tools, manufacturing capability that are required to support the technology and contribute to successful products meeting customer needs.

1.2.2 TI/GE Experience

Texas Instruments Incorporated (TI) and GE are currently involved in the MCM thrust and are producing hardware of a prototype nature. Major internal thrusts are in the areas of technology development and preliminary, limited quantity product demonstration for several internal project relationships and external customers.

The TI thrust has been directed, with Defense Advanced Research Project Agency (DARPA) and Air Force funding, at development of high density memory packaging using 3-D memory stacks and Tape Automated Bonding (TAB) technology for memory IO interconnect. The 3-D memory packaging, combined with 2-D processor IC packaging, has lead to the development of a prototype capability used for internal TI programs known as Silicon on Silicon (SOS). The TI SOS is similar to other standard industry MCM approaches, using a thin film polyimide interconnect constructed on a silicon substrate, with chip assembly requiring ICs tested with TAB interconnect thermal compression bonded to the thin

film interconnect. Experience with this "chip last" approach provides a foundation of MCM expertise to build upon for future MCM developments as well as firsthand background for "chip first" and "chip last" comparisons detailed later in this report.

The GE thrust has been directed, also with DARPA and Air Force funding, at development of a high density interconnect chip overlay process, unique to the industry. This technology is known as the GE-HDI process and is truly a "chip first" interconnect approach. It offers significant advantages in:

- Performance, both electrical and thermal/mechanical
- Reliability, demonstrated to full complement of Mil-Std-883
- 2-D IC array packaging density
- Rapid prototyping, using a direct design to manufacturing database technique
- Flexibility, in both design application format and in potential for future technology enhancements
- Low cost, both for rapid prototyping and for high volume production.

It is the TI/GE team's belief that the HDI approach answers the widest array of technical and cost issues at present and has tremendous potential for enhancement and growth. It is for these reasons that the GE-HDI technology was selected by the TI/GE team as the baseline technology for joint effort.

TI and GE have teamed together to execute the Silicon Wafer Advanced Packaging (SWAP) program, and have formed a strategic business alliance for long term MCM capability insertion as well. Together, both have combined experience in the development and application in prototype MCMs of "chip first", "chip last", and 3-D memory high density packaging. The SWAP team believes the elements of the GE-HDI, the TI 3-D memory technology, and some high volume processing techniques used in chip last MCM approaches such as TI-SOS technology, when combined in an optimized fashion will offer the highest performance, lowest cost, and most effective application of MCM packaging technologies to the market. It is this approach that the team presents as the fundamental elements of the TI/GE MCM technology roadmap.

1.2.3 DARPA Role

The potential role of DARPA in the development of a merchant MCM infrastructure is that of a catalyst. DARPA has filled a key role in sponsoring the development of basic technology in the area of MCM packaging with both TI and with GE over the past five years, and has resulted in the TI 3-D memory packaging capability and the GE-HDI 2-D overlay technology, which offer significant advantages in system level MCM packaging. The team believes these elements need to be integrated in a production MCM foundry to offer a suite of solutions to the customer. DARPA can become a catalyst to both accelerate the insertion of MCM packaging technologies into industry and to sponsor the industry infrastructure cooperation needed to further develop domestic advanced packaging capabilities. The issues of startup investment for facilities and capital, research and development to bring baseline production capability to the market, and the overall infrastructure issues that must be

developed do not yet exist, are formidable for any one company to attempt to breach alone. DARPA provides a path for strategic teaming of companies in a merchant foundry startup and reduces the risk for both these companies and the government in the early stages of MCM technology insertion.

1.2.4 Importance of MCM Technology Development and Insertion

Advanced packaging technology is key to maintaining the competitive position of U.S. industry in military electronics packaging. The SWAP team also believes it is a major development to maintaining the domestic leadership positions in the computer industry. Preliminary market data indicates that the primary opportunities in the near term are in the computer industry, in super computers, workstation applications, or in some cases, personal computers. It is certain that the commercial market in these areas will drive the overall MCM capability, and due to the volumes in the commercial sector, benefit the military insertion with a lower cost capability.

The MCM thrust is a key development for both TI and GE. TI/GE believes the success of any MCM Merchant Foundry in the MCM market place will be determined as much by how the insertion of the foundry engineering, design, manufacturing, and test infrastructure is managed and executed as by the basic interconnect technology itself. Strategic relationships must be developed between the MCM Foundry and industry to address the multitude of materials, process, equipment, requirements and standards, and interface issues that will need to be dealt with for production capability.

Developing operational MCM capability in a timely fashion to intercept the market demand must be the major target for success in this market place. This indicates that primary emphasis will be on establishing a strong foundry infrastructure for supporting MCMs as a turnkey product. A Merchant Foundry must have operational capability from design through end item test if it is to become a major player within this evolving market. The TI/GE team is uniquely positioned to meet this challenge. There is a high degree of vertical integration within both companies. The team brings complementary expertise and strength in research and development and in applications and manufacturing, as well as a strategic roadmap for market insertion to leverage from a technology development position to a custom manufacturing services deployment and marketing strategy.

1.2.5 Integration of the 90-09 and 90-10 Programs

TI and GE believe there is a need to investigate integration of the Defense Science Office (DSO) program, BAA 90-09 "Merchant MCM Foundry", and the Defense Manufacturing Office (DMO) program, BAA 90-10 "Silicon Wafer Advanced Packaging" (SWAP). This study leads to the conclusion that these programs are directed at two segments of the total MCM technology development issue that, when combined, will allow TI to address the whole of the MCM development and insertion requirements.

In the initial stages, a Merchant foundry will be faced with supporting market demand for capability to handle a high part number mix, small volume runs per part number (less than 100 units per design), and relatively high performance applications. Many initial designs will be conversions of existing functional designs packaged in some other format - in essence, breadboarded in another technology before implementation into a MCM format. Performance in system throughput and packaging volume will be the key elements sought by users of MCM technology. The ability to provide rapid prototyping service and quick design to manufacture turnaround will be critical.

This capability will need to be supplemented by the ability to provide high volume (greater than 1000 units per part number), low cost manufacturing capability very early in the technology insertion. Preliminary market surveys indicate this demand will happen between 1992 and 1994 and will be driven by the computer industry. It is in this mode of operation that a Merchant foundry will need to have established the key relationships and have developed a methodology to address the infrastructure issues mentioned previously. In this niche, the cost to performance relationship the high volume MCM foundry offers will be dominant in determining the degree of market opportunity penetration by the foundry.

The elements that need to be addressed for both of these phases of MCM Merchant foundry capability are contained in both BAAs. This study concludes that the high volume, low cost facility should be an extension of the low volume, high design mix facility developed under the BAA 90-09 Merchant Foundry program. The MCM technology roadmap indicates a need to develop first low volume, high design mix, rapid prototyping capability contained within the BAA 90-09 program that can transition to high volume, low cost production goals of the BAA 90-10 program as the MCM market grows. The TI/GE plan is to support rapid prototype, small volume runs, and rework with the BAA 90-09 facility in this planned growth scenario.

1.2.6 MCM Foundry Roadmap

The MCM Foundry Roadmap targets low volume production of MCMs within a foundry located at TI during 1992. Market forecasts show transitioning to high volume production (greater than 1000 units/month) during 1993. Two rates of volume ramp-up have been identified. The minimum business plan requires greater than 10,000 units/month in 1996, and the accelerated business plan requires greater than 10,000 units/month in early 1994. Current indications from potential users lend credibility to the actual opportunity being equal or greater than the accelerated business plan.

Integration of the 3-D memory packaging technology with the GE HDI 2-D planar chip overlay process is crucial to reaching ultimate system packaging goals, and is targeted for late 1992. Insertion of "chip last" assembly capability into the baseline foundry in the late 1992 time frame will serve existing TI-SOS program follow on products to offer a broad MCM technology base to customers. Merging the best elements of wafer scale "batch" processing with the baseline HDI overlay approach will result in the lowest cost, highest performance, and most flexible MCM packaging approach. This is projected between 1993

and 1995 and will depend on the degree of acceleration of the business plan due to developing market forces.

This long term, low cost, high volume enhancement of the GE-HDI will offer all the advantages of the technology at present and manufacturing modeling studies show it will be more cost effective in high volume production than current standard and enhanced, or "chip last" approaches.

Foundry qualification is planned in late 1993. The objective will be to set up and run the operation for both military and commercial products with the same procedures and processes. The only major difference is expected to be the value added hermetic assembly and additional testing required to qualify military products. Qualification will be based on MIL-I-38535 and is very similar to the Mil-Std-1772 procedure for both the facility certification and product qualification. The cost impact is minimal if the objective of military and commercial products manufactured in one facility with common standards is targeted from the outset. In fact, this study has lead to the conclusion that the commercial products will benefit from higher yields and lower unit costs over the long term with this approach, and government MCMs will benefit from commercial volume leverage as well.

2.0 ADVANCED TECHNOLOGY COMPARISON

In the broad sense, the GE-HDI process must be compared with not only other MCM technologies, but with other advanced packaging approaches. These other non-MCM technologies include high density surface mount technology (SMT), Chip-on-Board (COB), and monolithic Wafer Scale Integration (WSI). Technologies such as traditional hybrids and state-of-the-art SMT can not compete because of limits in both feature size and dielectric constants that limit density and performance. The following sections of this report will examine the critical features, advantages and disadvantages of the leading MCM and non-MCM packaging technologies.

2.1 COMPARISON OF ADVANCED PACKAGING TECHNOLOGIES

The driving forces behind the development of multichip and other advanced packaging technologies is the inability of the present packaging technologies to effectively interconnect the latest semiconductor devices without compromising performance. The areas of concern are electrical performance (i.e., clock rates and throughput), thermal performance and density, both area and density. As semiconductor technology (i.e., predominantly CMOS based silicon) has transitioned to sub-micron feature sizes, the device gate count, pin count, clock rate and power density have continued to increase.

Application specific ICs (ASICs) and complex processors now regularly have 50,000 to 100,000 gates, 200 to 400 I/O pins, clock rates of 40 MHz or more, and chip power dissipation of 2 to 5 Watts. Standard packaging approaches with one chip per package have fixed I/O feature sizes with SMT limited to 25 milli-inch perimeter pitch and through-hole limited to 50 milli-inch perimeter pitch on grid. As pin counts double, perimeter package footprints increase by a factor of four. This leads to less components per board area and longer interconnect distances between components. Table 2-1 compares the GE-HDI MCM technology with other high density MCM technologies, SMT, hybrid and WSI.

2.2 SURFACE MOUNT TECHNOLOGY AND CONVENTIONAL THROUGH-HOLE

SMT and through-hole are limited to only 2% to 5% silicon density because of their large package footprint and limited board connectivity, and hybrids are limited to 10% to 15% because of interconnect feature size. MCM technologies and WSI are capable of 25% to 70% silicon density. In addition, present board technology limits package-to-package performance to the 50 MHz range because of the higher dielectric constant and the long interconnect length. WSI and MCM technologies can be extended to operate in the hundreds of MHz range.

TABLE 2-1. COMPARISON OF ADVANCED PACKAGING APPROACHES

	Minimum Feature	Silicon Density	Dielectric Constant	Radiation Hardened	Reliability	Tested to 883R
GE-HDI	1 mil	80%	2.8	Yes	High	Yes
Monolithic Wafer Scale	0.2-1.0 Mil	45%	8.0	No	Unknown	No
Ceramic Hybrid	5 Mil	10-15%	9.0	No	Moderate	Yes
Surface Mount Assembly	5 Mil	2-5%	4.0	N/A	Moderate	Yes
Silicon Substrate (i.e., Raychem, ATT, Etc.)						
- Wirebond	1 Mil	40%	3.5	Some	Moderate	Yes
- TAB	1 Mil	50%	3.5	Some	Moderate	?
- Flip Chip	1 Mil	60%	3.5	No	Unknown	No
* Assumes 50% Wafer Die Yield						

	Chip Repairability	Interconnect Repair/Rework	Prototype Costs	Production Costs
GE-HDI	Yes	100%	Moderate	Moderate***
Monolithic Wafer Scale	No	No	Ultra High	High
Ceramic Hybrid	Limited	No	High	Moderate
Surface Mount Assembly	Yes	Jumper Wing	Moderate	Low
Silicon Substrate				
- Wire Bond	Limited	No	High	Moderate
- TAB	Limited	No	High	Moderate
- Flip Chip	Poor	No	High	Moderate
*** Baseline GE-HDI without enhancements				

2.3 WAFER SCALE INTEGRATION

The inherent drawbacks of WSI are that the monolithic nature of this approach limit it to:

- One device technology rather than different semiconductor technologies optimized for different functions
- Low wafer fab yield because of the increased die area and the increased gate count (both 10x or more than conventional IC's)
- No ability for rework for defects or redesign

- Limited application of a WSI design because a "system on a chip" tends to be too application specific
- CAE and test capability does not exist for complex WSI designs.

These limitations will force WSI to be too expensive for any application specific design. The only areas that WSI may make a practical impact within the next ten years are structured logic functions that have a large number of common repeated elements that lend themselves to redundancy to increase yield and to generic usage. This would include memory arrays, distributed processing elements and the like.

2.4 HYBRIDS

State-of-the-art hybrid technology is limited by both the minimum feature size of the interconnect process and the electrical performance limits of the interconnect materials. Most hybrids are based on a multilayer ceramic process. These include thick film, thin film and co-fired structures. These processes have feature sizes that limit interconnect density to 100 lines per inch per layer (less than half the capacity of MCM technologies), limiting the silicon density to 15% (less than one fourth the capacity of MCM). The electrical performance is limited by the poor conductivity of the ceramic metal systems (except gold processes that are costly), and to the poor dielectric constant of the ceramic insulating layers (9 for ceramic verses 3 for MCM).

2.5 MCM TECHNOLOGIES

The comparisons of differing MCM technologies with each other and with the GE-HDI process shows many more similarities then differences. Most of the MCM industry has developed common interconnect processes with differences occurring in materials and structures. The typical MCM substrate has a thin film polymer interconnection structure composed of polyimide dielectric and a copper or aluminum metallization (often with a barrier metallization of Cr or Ti). Multilayer structures are built up on a silicon, ceramic or aluminum nitride substrate.

The polymer dialectric layer is spun-on or sprayed-on in multiple coats to minimize pin hole shorts. The metallization is then applied by a combination of sputtering and or electroplating and then patterned with the application of a photo-resist, developing, etching and cleaning (a fully subtractive metal process). The dielectric process is repeated and vias are formed through the dielectric to the metallization below through a masked based wet or dry etch process. These steps are repeated for each of the interconnect layers. There are typically five layers, X and Y interconnect layers, a power plane, a ground plane and a pad layer for chip attach. The chip attach for most of these MCM substrates is wirebonding, TAB, or flip chip solder bump.

Some of the variations from these standard MCM processes are:

- Laser drilling of via holes (GE)
- Solid plated-up vias with mechanical planarization (MCC, NEC, NTK, NTT)

- Barrier metal on trace sidewalls (MCC, NEC, NTT)
- Direct chip pads to interconnect metallization (GE, Polylithics)
- Lower CTE, dielectric constant and moisture absorption polymers (Rogers, Rockwell, MCNS, GE)
- Silicon Dioxide dielectric layers (nChip, ATT)
- Laser photo-patterning of metallization photo-resist (GE)
- Fabrication of power and ground planes and decoupling capacitance within the substrate (nChip, Honeywell, NEC, ATT)
- Thin film resistor elements (nChip, ATT).

Table 2-2 and Table 2-3 compare the leading thin film MCM technologies for merchant and captive facilities, respectively. These tables compare substrate, conductor and dielectric materials, line, space and via feature sizes, number of layers, conductor and via processes and chip contact processes. All of these MCM technologies can offer about a 10:1 density improvement, a 2:1 interconnect speed improvement and a 2:1 or better reduction in off-chip connections (a key determinant of system reliability), over SMT approaches. At best, the differences between these MCM technologies are 50% for density and the number of off-chip connections and 25% for interconnect delays. There are other features of these MCM technologies that though not as obvious will have a major impact on the cost effectiveness of each of these approaches.

2.5.1 Die Interconnect

There are four basic approaches to bare chip interconnect to an MCM substrate:

- Wirebond
- TAB
- Bump (solder)
- Direct metallurgical contact.

The advantages of wirebonds are that no special chip and metallization is required, no tooling is required and the industry infrastructure for the process is well established. The disadvantages are that wirebonds have lower bond yield, lower reliability, higher inductance, limited density, are only applicable to peripheral I/O pads and require a larger bonding footprint.

TAB advantages are higher pad density, lower inductance than wirebonds, area pad capability, pre-test capability and higher yield and reliability. The disadvantages of TAB are increased chip costs due to the need for additional wafer processing required to form the TAB bumps, the limited availability of TABed chips, the added non-recurring and recurring costs of TAB lead frames, the immaturity of the TAB industry infrastructure and a TAB footprint only slightly smaller than wirebond.

Bump technology advantages are the small bonding footprint, area pad capability and low inductance. The disadvantages of bump technology are the increased chip costs due to the need for additional wafer processing required to form the bumps, the limited availability

TABLE 2-2. THIN FILM MULTICHIP MODULE TECHNOLOGIES - MERCHANT

Company	Substrate	Conductor	Dielectric	Features Line/Space/ Via	Max. No. Layers	Conductor Process	Via Process	Chip Contact
APS/Ray Chem	Si/Al_2O_3	Al	PI	25/50/35	7	Sputter	Dry Etch	WB/TAB
Alcoa	Al_2O_3	Cu	Pi	20/25/20	9	Sputter/Plate	Dry Etch	WB/TAB
Hughes	Si/Al_2O_3	Al	PI	20/40/35	5	Sputter	Dry Etch	WB/TAB
n Chip	Si	Al/Cu	SiO_2	25/ /	5	Sputter/Plate	Dry Etch	WB
Polycon	Si/AlN	Al	PI/BCB	20/50/35	5	Sputter	Dry Etch	WB
Polylithics	Glass/Quartz	Cu	PI	15/35/6	7	Evaporation	Dry Etch	Solder Bump
Rogers	Moly	Cu	Fluoropolymer	50/15/75		Plate	Plate-Up	TAB
Tektronics	Al_2O_3	Au	PI	10/10/10	8	Sputter/Plate	Wet Etch	TAB
Uni Structures	Mo/AlN	Cr/Cu	PI/epoxy	50/50/50	6	Sputter/Plate	Plate-Up	Bump TAB
MCC	Al_2O_3	Cr/Cu/Cr	PI	15/35/	5	Sputter/Plate	Plate-Up	TAB
MCNC	Al_2O_3/AlN	Cu/Al	PI/BCB	8/24/8		Evaporation	Plate-Up	Dry Etch
GE/TI	Al_20_3/AlN	Ti/Cu/Ti	PI	35/65/35	5	Sputter/Plate	Laser Ablate	Sputtered Contact

TABLE 2-3. THIN FILM MULTICHIP MODULE TECHNOLOGIES - CAPTIVE

Company	Substrate	Conductor	Dielectric	Baseline Line/Space/ Via	Max. No. Layers	Conductor Process	Via Process	Chip Contact
ATT	Si	Ti/Cu/Ti	PI/SiO_2	10/10/	3x2	Sputter/Plate	Dry Etch	Solder Bump
DEC	N/A	Cu	PI	18/57/	9	Sputter/Plate	Dry Etch	TAB
Honeywell	Al_2O_3/Si	Ti/Cu/Ti	PI	25/100/100	5	Sputter/Plate	Dry Etch	Bump/TAB
IBM	Si	Al	PI	15/10/5	4	Sputter	Dry Etch	Solder Bump
Rockwell	Si/AlN	Al	PI/BCB	20/60/	6	Sputter	Dry Etch	WB/TAB
HP	Si/AlN	Cr/Cu/Cr	PI	15/35/6	7	Sputter/Plate	Plate-Up	Solder Bump
NEC	Sapphire	Cr/Cu/Ni	PI	25/50/30	7	Sputter/Plate	Plate-Up	TAB
NTK	Al_2O_3	Cu	PI	25/40/		Evaporated	Plate-Up	TAB
NTT	Al_2O_3	Cu	PI	25/25/30	6	Sputter/Plate		Solder Bump
Toshiba	Si	Ti/Cu/Ti	PI	50/150/50	8	Sputter/Plate		Solder Bump
Hitachi	Si	Al	SiO_2			Sputter		Solder Bump
Thompson-CSF	Si	Sl	Silica	20/20/8	4	Sputter	Dry Etch	WB/TAB

of bumped chips, the immaturity of the bump industry infrastructure, the inability of chip pretest, the questionable reliability of bumps to thermal cycling requirements and the inability to inspect bump joints.

The advantages of direct metallurgical contact to chip pads are the smallest bonding footprint, lowest thermal path, lowest interconnect inductance, highest interconnect reliability, compatibility with pads, no special wafer processing required, compatibility with any chip technology or chip supplier and no unique placement technology required. The disadvantages of direct metallurgical contact technology are the difficulty of chip pretest and the increased complexity of module test and module repair because of the imbedding of the chips within the interconnect structure.

Table 2-4 compiles these MCM to chip interconnect features for the four interconnect approaches examined above.

2.5.2 Via Formation

There are three basic approaches to via formation; wet or dry etch through a photomask, plated-up vias, and laser ablation.

- The advantages of the wet or dry etch using plasma or reactive ion etch (RIE) are that they will be documented, batch processes that lend themselves to higher volume. The disadvantages are poor via sidewall control that often leads to undercutting, poor metallization and lower via yield.

- The plated-up via process has the advantages of a planar structure (after mechanical grinding), barrier metal coverage of sidewalls, and lower via resistance. The disadvantages of plated-up vias are the high processing costs of the process and the questionable interconnect yield. Both the etched via processes and the plated-up process require costly, long lead time mask sets.

- The laser ablation process advantages are the elimination of masks, the controlled via shape (sloped sidewalls), the high via yield (virtually 100%), the adaptability of laser drilling and the ability to do rapid prototyping and lots of one on a high volume fabrication line. The disadvantages of laser ablation are the uniqueness and costs of the laser system and the questionable extension of a serial laser process to high volume and low costs.

2.5.3 Metallization Photopatterning

There are basically three approaches to the photopatterning of MCM interconnection metallization; a fully subtractive etching process using a photomask/photoresist process, a plated-up, semi-additive photomask/photoresist process and a fully subtractive etching process using a laser photopatterning/photoresist process.

TABLE 2-4. MCM TO CHIP INTERCONNECT FEATURES

Interconnect Technology	MCM to Chip Interconnect Features					
	Footprint % Silicon	Min. I/O Pac Pitch	Pad Array Capability	I/O Inductance (nH)	Resistance (milliΩ)	Capacitance (pF)
Wirebond	50%	6-8 mils	No	2.00	100	0.038
TAB	70%	4-6 mils	Yes	0.40-1.20	13	0.027
Bump	80%	25 mils	Yes	<0.10	2.6	0.010
Metallurgical Contact	80%	3-4 mils	Yes	<0.05	<1.0	0.001

Interconnect Technology	MCM to Chip Interconnect Features					
	Contact Reliability	Special Chip Costs	Chip Availability	Tooling Costs	Chip Pretest	Equipment Maturity
Wirebond	Low	None	Any	None	No	High
TAB	Good	High	Limited	High	Yes	Low
Bump	Unknown	High	Limit	Moderate	No	Low
Metallurgical Contact	Excellent	None	Any	None	No	High

- The photomask based subtractive process advantages are that they are well known processes, batch processes and easily scalable to high volume. The disadvantages of the photomask subtractive processes are that they require a mask set that increases costs, increases lead time and is not compatible with prototype fabrication and the lack of barrier metallization on trace sidewalls.

- The photomask plated-up process advantages are better line width and shape control, ability to process barrier metallization on trace sidewalls, easily scalable to high volume and high interconnect yield. The disadvantages of photomask plated-up processes are that they require a mask set that increases costs, increases lead time and is not compatible with prototype fabrication.

- The laser photopatterned subtractive process advantages are that no mask sets are required thereby reducing both non-recurring and recurring costs, minimizing lead time, providing for engineering change capability and making lot sizes of one possible. The disadvantages of the laser photopatterning

subtractive process is the questionable extension of a serial laser process to high volume and low costs, the uniqueness and costs of the laser system and the lack of barrier metallization on trace sidewalls.

2.5.4 Dielectric Material Selection

- Virtually all of the MCM technologies that use a polymer thin film dielectric use or have used a polyimide dielectric. These typically have a dielectric constant of 2.8 to 3.5, CTE of 50 to 70 ppm °C, and a moisture uptake of about 1%. The other thin film polymer MCMs have gone to new and innovative materials that offer higher performance or less complex processing. Finally, there are a limited number of MCM technologies that use $Si0_2$ as a dielectric layer.

- The improved polymeric materials in use and under evaluation include benzocyclobutenes (BCB), polyquinolines and low stress polyimides and generally offer lower dielectric constants, 2.0 to 2.7, lower moisture uptake, 0.3% to 0.1%, and lower CTE, 6 to 10 ppm/°C. These materials still require process development to get them into broad based MCM usage. But they may offer finer line spacing, reduced crosstalk, better transmission line stability and lower stress. It can be expected that all of the high performance MCM technologies, including GE-HDI, will turn to these improved polymers as they continue to become more readily available and easier to process.

- The advantages of $Si0_2$ are that it has a relatively low dielectric constant (3.8), a very low dissipation loss (.00006) and it is an inorganic material that is less likely to have pin holes or moisture related reliability problems. The difficulty with using SiO_2 is that it is difficult to get a thick dielectric layer (greater than 3 to 5 microns) due to excessive stress and defects. With the thinner dielectric isolating the interconnect lines and the ground planes, line widths more than 10 microns will have excessive capacitance while the narrower lines have high resistance. The combination of higher capacitance and high series resistance would limit performance to 40 to 50 MHz. nChip has announced that they have a thick SiO_2 low temperature process that minimizes stress. Their baseline process has one 7 micron SiO_2 layer isolating the two signal layers from the two reference layers. This thin, narrow (2 microns thick by 5 microns wide) sputtered aluminum lines are resistive with 15 ohms per cm.

2.6 CHIPS LAST MCM VERSUS GE-HDI SUMMARY

- The GE-HDI overlay MCM technology is much more distinctive than a MCM approach that imbeds the chips into the interconnect structure, as shown in Table 2-5. The GE-HDI approach provides the highest electrical, thermal, mechanical and reliability performance approach to high speed, high complexity semiconductor devices available in the electronics industry. The technology has been shown to surpass Mil-Std Class B and Class S reliability

TABLE 2-5. GE-HDI CHIP UNDER SUBSTRATE ADVANTAGES

Low Stress Structures	Robust in harsh thermal, mechanical and radiation environments High reliability, long field life
Maskless, Laser-Based Process	Low NRE cost, cycle time Quick turn prototyping High yield via process
Chip Under Interconnect	High thermal capacity No on-wafer bump process required
Direct Chip Pad Contacts	No TAB NRE/Recurring Costs Higher silicon density Higher speed logic(>1 GHz)

and environmental screens and requirements on a limited sample size including radiation environments, thermal cycling, thermal shock, acceleration, mechanical shock, vibration, burn-in and hermeticity. Its laser based patterning minimizes development cost and design to hardware cycles.

It has been demonstrated to be extendable over the full range of digital electronics, from low MHz to multiple GHz, to analog and mixed analog/digital circuits, to power conversion, IR and acoustic sensors and to microwave circuitry. The GE-HDI process has been shown to be compatible with virtually all semiconductor device technologies including silicon (SOS, SOI, CMOS and Bipolar), GaAs and InSb, as well as piezo electric transducers. The benign nature of the GE-HDI fabrication and repair processes has been used to develop a full array of bare chip pretest and burn-in approaches using the temporary application of portions of the basic GE-HDI process. The technology enhancements section of this report will address developments in processes, equipment, materials and computer innovative approaches to extend the GE-HDI process to high volume and low cost.

2.7 TECHNOLOGY COMPARISON CASE STUDIES/ASSUMPTIONS

The following two case studies compare GE-HDI to various other MCM technologies. The comparison methodology was to:

- Draw on existing TI and GE MCM technical expertise
- Include an outside company's MCM interconnect technology in the comparison
- Select major performance characteristics important to MCM customers

- Compare known designs
- Compare designs that represent varying module complexity
- Make simplifying assumptions to provide direct comparisons of major performance parameters and production costs.

2.7.1 Experience

TI and GE have technical experience in both the SOS chips last approach and the GE-HDI chips first approach. In addition, technical design inputs were provided by Microelectronics and Computer Technology Corporation (MCC) on their Quick Turnaround Interconnect (QTAI) technology. Comparisons were made based on this experience.

2.7.2 Performance Characteristics

The major performance characteristics studied in this comparison are:

- Mechanical performance (line widths, line spaces, silicon density, etc.)
- Electrical performance (line impedance, resistance, propagation delays)
- Thermal performance

These parameters are important because they influence decisions on which interconnect technology best meets requirements. Also, production costs associated with each interconnect technology are important because they determine the final cost to the MCM customer. Therefore, two currently existing MCM designs were selected to provide a wide range of module performance characteristics and production costs. The designs selected represent both:

- Small and large number of Integrated Circuit (IC) chips
- Low and high thermal performance
- Low and high number of nets per module

2.7.3 Case Study for 1750A

Separate 1750A module designs have been demonstrated by GE and MCC. However, the actual number of chips and chip sizes vary. To solve these variations, all technologies compared assumed a common functional chip set. In addition, the comparison data used for the SOS chips last approach was obtained directly from TI's current design rules and is within current design parameters for this type of module.

2.7.3.1 Mechanical and Electrical Results. The mechanical and electrical performance parameters from this 1750A case study are shown in Tables 2-6 and 2-7. This data shows that the GE-HDI chips first technology can interconnect the 18 chips in the dual 1750A module in a much smaller area with higher silicon density than either the chips last SOS technology or the QTAI technology. The more than 2:1 area reduction is due to the tighter chip spacing, 15 mils, and the more efficient interconnect routing of the GE-HDI technology.

TABLE 2-6. 1750A MODULE DESCRIPTION

Module Description	GE-HDI Chips First	SOS Chips Last	QTAI Chips Last
Module Size (in^2)	1.7	4.0	4.0
Number of ICs	18	18	18
Number of Capacitors	5	5	5
Total Module I/O	184	184	184
Total Number of Nets	398	398	398
Number of Layers	4	5	6

TABLE 2-7. 1750A CIRCUIT DESCRIPTION

Circuit Description	GE-HDI Chips First	SOS Chips Last	QTAI Chips Last
Line Pitch (in)	0.0036	0.0030	0.0030
Line Width (in)	0.0015	0.0010	0.0006
Available Interconnect Capacity (lines/in/layer)	278	334	334
Average Routing Density (% of all channels available)	40	N/A	44
Minimum Spacing Between ICs (in)	0.016	0.080	0.080
Silicon Density (%)	60	30	30
Total Interconnect Length (in)	378	582	1176
Avg Interconnect Length (in)	0.95	1.46	2.97

The GE-HDI design has fewer layers than the two chips last designs due to the added pad layer for both SOS and QTAI (see Table 2-6) and due to the personalization layer needed on QTAI.

While all three designs have the same number of interconnect nets, the increased substrate area of the SOS and the QTAI designs causes an increased interconnect wiring in both of the chips last designs. The GE-HDI design has 378 inches of interconnect in its 398 nets for an average of 0.95 inches per net. The SOS and the QTAI designs has 583 and 1176 inches of interconnect respectively for average interconnect distances of 1.46 and 2.97 inches respectively. The increase in the SOS average interconnect distance is due solely to the lower silicon density, while the much larger increase in the QTAI average is due to both the lower silicon density and the inherent inefficiencies of the QTAI top level personalization technique.

The electrical parameters for these three designs are shown in Table 2-8. The QTAI design has higher line capacitance, line inductance, line DC resistance and propagation delay than the baseline SOS design, on either a per net or per inch basis. The GE-HDI design has lower values for all of these line parameters than either the SOS or QTAI designs. The average line DC resistance for the GE-HDI design is only 2.61 ohms while the SOS is 8.76 ohms and the QTAI is 16.8 ohms.

Finally, the QTAI process will have a limited application to high frequency designs because of this poor electrical interconnect performance. The GE-HDI process will be applicable to high frequency designs into the multiple 100 MHz clock rate (300 MHz designs have been successfully fabricated with the GE-HDI process). The GE-HDI electrical improvements include:

- Lower and better matched line impedances
- Lower DC resistance (6:1)
- Shorter interconnect distances (3:1)
- Lower capacitance (3:1)
- Lower inductance (5:1)
- Lower propagation delays (4:1).

The results show a lower interconnect capacity for the GE-HDI chips last approach. This situation is a result of the larger line widths and larger line pitch used by the GE-HDI technology. However, the average routing density for the GE-HDI is the same (or slightly less) as the QTAI approach for a larger module. This indicates that the QTAI process pays a penalty in routing efficiency due to their unpersonalized layer method. Data for the SOS process is not possible due to the design never being actually routed. An estimate of the routing density should not be any greater than either the GE-HDI or the QTAI approach.

Finally, (where the QTAI approach may pay a penalty) the GE-HDI approach gains the advantage of improved electrical characteristics due to larger line widths and shorter interconnect distances. The areas of improvement are:

TABLE 2-8. 1750A ELECTRICAL DESCRIPTION

Electrical Description	GE-HDI Chips First	SOS Chips Last	QTAI Chips Last
Line Impedance			
Upper Trace (ohms)	70.3	75	90
Lower Trace (ohms)	57.0	51	70
Line Capacitance			
Upper Trace (pf/in)	1.9	2.2	2.1
Lower Trace (pf/in)	2.8	3.8	2.6
Average per Net	2.2	4.4	7.0
Line Inductance			
Upper Trace (nH/in)	9.3	12.2	16.7
Lower Trace (nH/in)	9.18	10.2	13.0
Average per Net	8.79	16.4	44.1
DC Resistance (ohm/in)	2.75	6.00	5.66
Average per Net line	2.61	8.76	16.8
Propagation Delay (ps/in)	132.5	157.5	185.0
Average per Net	125.9	230.0	549.5

- Lower line impedance and better matching
- Lower DC resistance
- Lower propagation delays.

2.7.3.2 **Fabrication Cost Assumptions.** The process steps outlined in Table 2-9 for GE-HDI and SOS Flip-Tab were used to effectively determine a comparable total module cost. The process steps used by MCC were consistent with their QTAI method of processing MCMs. The following assumptions were agreed upon and used for all technologies evaluated:

- All total module dollar estimates are normalized manufacturing costs and do not report MCM prices
- Substrate material costs are not included, but substrate processing costs are included
- Rework costs and cycle times are not included
- Wafer size is a standard eight inches
- Manufacturing equipment costs and space estimates are assumed constant values for all approaches.

TABLE 2-9. PROCESSING FLOWS

	GE-HDI Process Description Total Flow		Flip-TAB Process Description Substrate
1	Substrate Milling	1	Metallize TIW/AL
2	Metal 0	2	Photoresist
3	Photoresist	3	Expose Photoresist
4	Expose Photoresist	4	Develop Photoresist
5	Develop Photoresist	5	Clean Up Photoresist
6	Clean Up Photoresist	6	Etch Metal TIW/AL
7	Etch Metal 0	7	Strip Photoresist
8	Strip Photoresist	8	Deposit PI
9	"Epoxy" + Chip Place	9	Photoresist
10	Chip Mapping Mech.	10	Expose Photoresist
11	Adhesive Spray	11	Develop Photoresist
12	Lamination Dielec. 1	12	Via Etch
13	Via Etch	13	Strip Photoresist
14	Via Clean Up	14	Metallize TIW/AL
15	Surface Prep. Dielec.	15	Photoresist
16	Metal TI/CU Metal 1	16	Expose Photoresist
17	Plate CU	17	Develop Photoresist
18	Metal TI Metal 1	18	Clean Up Photoresist
19	Photoresist	19	Etch Metal TIW/AL
20	Expose Photoresist	20	Strip Photoresist
21	Develop Photoresist	21	Deposit P1
22	Clean Up Photoresist	22	Photoresist
23	Etch TI/CU/TI Metal	23	Expose Photoresist
24	Strip Photoresist	24	Develop Photoresist
25	Surface Prep Dielec	25	Via Etch
26	Deposit Dielec 2	26	Metallize TIW/AU
27	Via Etch	27	Photoresist
28	Via Clean Up	28	Expose Photoresist
29	Surface Prep Dielec	29	Develop Photoresist
30	Metal TI/CU Metal 2	30	Clean Up Photoresist
31	Plate CU	31	Plate AU
32	Metal TI Metal 2	32	Strip Photoresist
33	Photoresist	33	Photoresist
34	Expose Photoresist	34	Expose Photoresist
35	Develop Photoresist	35	Develop Photoresist
36	Clean Up Photoresist	36	Clean Up Photoresist
37	Etch TI/CU/TI Metal	37	Etch TIW/AU
38	Strip Photoresist	38	Strip Photoresist
			Chip Processing Flip-TAB Wafers
		1	Metallize TTW/AU
		2	Photoresist
		3	Expose Photoresist
		4	Develop Photoresist
		5	Clean Up Photoresist
		6	Plate AU
		7	Strip Photoresist
		8	Photoresist
		9	Expose Photoresist
		10	Develop Photoresist
		11	Clean Up Photoresist
		12	Etch TIW/AU
			Flip-TAB Assembly
		1	Innerlead Bonding
		2	Excise
		3	Chip Placement
		4	Outerlead Binding
Total Processing Steps			
GE-HDI	**38**	**Flip-TAB**	**54**

- No tooling costs are included
- No CAD, CAE, CAM costs are included
- QTAI processes include costs of manufacture of personalized and unpersonalized layer processing
- Overhead and labor rate estimates are assumed constant values for all processes.

2.7.3.3 Costs Comparison. Tables 2-10 and 2-11 present the results of the production cost analysis. This analysis was systematically performed to represent the various production cost differences between each technology. The costs presented are theoretical and do not necessarily correspond with estimates given in sections 4.5 and 4.6 of this report. However, the magnitude of the cost differences between technologies is a good representation of the price competitiveness between the technologies. The cost variations between this section and later sections of this report are due to the simplifying assumptions made here. These assumptions provide a common set of cost variables (equipment, labor, overhead and facilities) necessary to calculate manufacturing cost comparisons between different MCM interconnect technologies.

The major module cost drivers are the number of substrates per carrier, capital expenditures, and additional chip processing and assembly costs. As expected, the reduced substrate size of the GE-HDI chips first approach allows more substrates to be processed per carrier. This increased lot size reduces the touch hours per module and reduces fabrication costs. In addition, the GE-HDI process gains further reduction in production costs due to no added TAB and TAB attach costs. Capital expenditure costs are higher for the low volume QTAI facility due to added equipment needed for the QTAI batch processes. The increase touch hours per module for the QTAI and SOS processing are due to the additional touch hours required for TAB attach processes and limited number of substrates per carrier. Also, the difference in touch hours between QTAI and SOS approach is a result of the QTAI mass processing of unpersonalized interconnect layers.

Finally, when all the major cost drivers are taken into consideration, the cost analysis shows the GE-HDI chips first technology increasingly cost competitive. Evaluation of the MCM cost savings using the module cost per square inch, is misleading. As an example, using the cost per square inch for the 1750A module evaluated provides the following values:

	Low Volume	High Volume
• GE-HDI chips first	$.9X/in^2	$.7X/in^2
• SOS chips last	$1X/in^2	$1X/in^2
• QTAI chips last	$1.4X/in^2	$1X/in^2

These values describe reductions in cost for the HDI approach on the order of 11% SOS to 34% QTAI for low volume production, and 23% QTAI to 26% SOS for high volume production.

TABLE 2-10. 1750a COST ANALYSIS - 1000 PER MONTH

1000 Month	GE-HDI Chips First	SOS Chips Last	QTAI Chips Last
Substrate/Carrier	16	7	7
Carrier/Lot	4	4	4
Facility Space (ft^2)	2764	2601	3133
Number of Shifts	2	2	2
Capital ($M)	4.2	4.5	6.0
HRS/Module	0.39	2.20	1.09
Estimated TAB Cost ($)	Not Required	$126/module $7/site	$126/module $7/site
Final TAB Attach Cost ($)	Not Required	$83/module	$80/module
Total Module Cost - Factor	**.38X**	**X**	**1.36X**

TABLE 2-11. 1750a COST ANALYSIS 10,000 PER MONTH

10,000 Month	GE-HDI Chips First	SOS Chips Last	QTAI Chips Last
Substrate/Carrier	16	7	7
Carrier/Lot	12	12	12
Facility Space (ft^2)	8127	8000	5716
Number of Shifts	2	2	2
Capital ($M)	15.2	11.4	12.1
HRS/Module	0.294	0.800	0.610
Estimated TAB Cost ($)	Not Required	$68/module $3.75/site	$68/module $3.75/site
Final TAB Attach Cost ($)	Not Required	$38/module	$38/module
Total Module Cost ($)	**.31X**	**X**	**.96X**

A more accurate measure of cost savings are given by the total module cost shown in Tables 2-10 and 2-11. The analysis shows a minimum 62% reduction in cost for 1000 modules per month facility and a minimum 67% reduction in cost for the 10,000 module per month facility. The differences between cost per square inch and total module cost numbers exist because of the reduced module size for the GE-HDI chips first approach. Cost comparison based solely on $\$1/in^2$ mask the true savings achievable by a higher density process such as GE-HDI. Furthermore, the final total module cost is the critical value judged by customers when considering different interconnect options.

2.7.4 Case Study for the ERIM Pipeline Processing Module

The ERIM pipeline processing module was evaluated using the GE-HDI chips first and SOS chips last design rules. Unlike the 1750A, this module has not been manufactured by either GE or TI but does provide another design comparison for comparison. Established design parameters were used for each technology and verified against other designs with similar complexity (number of nets, chip count, etc.).

2.7.4.1 Mechanical and Electrical Results. Tables 2-12 and 2-13 present the results of the ERIM module design utilizing the GE-HDI chips first and SOS chips last technology. This module design has a total chip count of 59 chips and nets totaling 1050. Also, similar to the 1750A case study, the reduced spacing between ICs provides the GE-HDI technology the benefits of increased silicon density and reduced module size. The line pitch for the SOS technology was reduced to accommodate additional thermal vias. As a result the SOS approach has to increase the available interconnect by reducing the line pitch which increased cross-talk.

2.7.4.2 Cost Assumptions/Comparison. A cost comparison was done on the ERIM module design using the same factory models and assumptions outlined for the 1750A analysis. The comparison done on this module solidified and magnified the cost differences previously discussed. This can be seem in the following values:

	GE-HDI CHIPS FIRST	SOS CHIPS LAST
Total Model Cost Factor 1000/Month Facility	$.24X	$X
Total Model Cost Factor 10,000/Month Facility	$.23X	$X

These numbers represent an average 77% decrease in cost for the HDI chips first approach. The cost difference between these two technologies has increased from the 62% shown in Section 2.7.3.3. The increased cost difference is due to the added cost for TAB and final TAB attach. This situation is expected because the ERIM module design has more chips and requires added chip processing time per module. However, the module costs for the HDI chips first approach are not largely dependent on the number of chips per module. Therefore, this provides the HDI chips first approach which is a major cost advantage.

TABLE 2-12. ERIM MODULE DESCRIPTION

Module Description	GE-HDI Chips First	SOS Chips Last
Module Size (in^2)	4.8	7.85
Number of ICs	59	59
Total Module I/O	140	140
Total Number of Nets	1050	1050
Number of Layers	4	5

TABLE 2-13. ERIM MODULE CIRCUIT DESCRIPTION

Circuit Description	GE-HDI Chips First	SOS Chips Last
Line Pitch (in)	0.0036	0.0020
Line Width (in)	0.0015	0.0010
Available Interconnect Capacity (lines/in/layer)	278	500
Minimum Spacing Between ICs (in)	0.016	0.080
Silicon Density (%)	63	39

2.7.5 Thermal Comparison

Figure 2-1 presents a graphical representation of the thermal performance advantage gained by the GE-HDI chips first approach. This advantage is due to the direct attachment of chips to the substrate in GE-HDI. The thermal paths are depicted in the figure. The major difference between chips last approach and the chips first approach is that the heat generated by the chip must pass through a layered interconnect in the latter before reaching the substrate. As shown in the graph, a chip having a side length of 0.15 inch produces a temperature rise difference between the two approaches of approximately 2.5°C. Similarly, a large ASIC that has a power dissipation of 10.7 watts and a side length equal to 0.550 inch would have a temperature rise of 1.6°C for the GE-HDI approach and a temperature rise of 6.5°C for the SOS approach. This results in a 5°C advantage with the GE-HDI chips last approach having the advantage.

2.7.6 Conclusions

Several factors determine the final manufacturing costs of a MCM and the customer's decision of which technology to use. The factors that determine MCM costs for all interconnect technologies are:

- Module complexity
- Volume
- Yields
- Assembly costs.

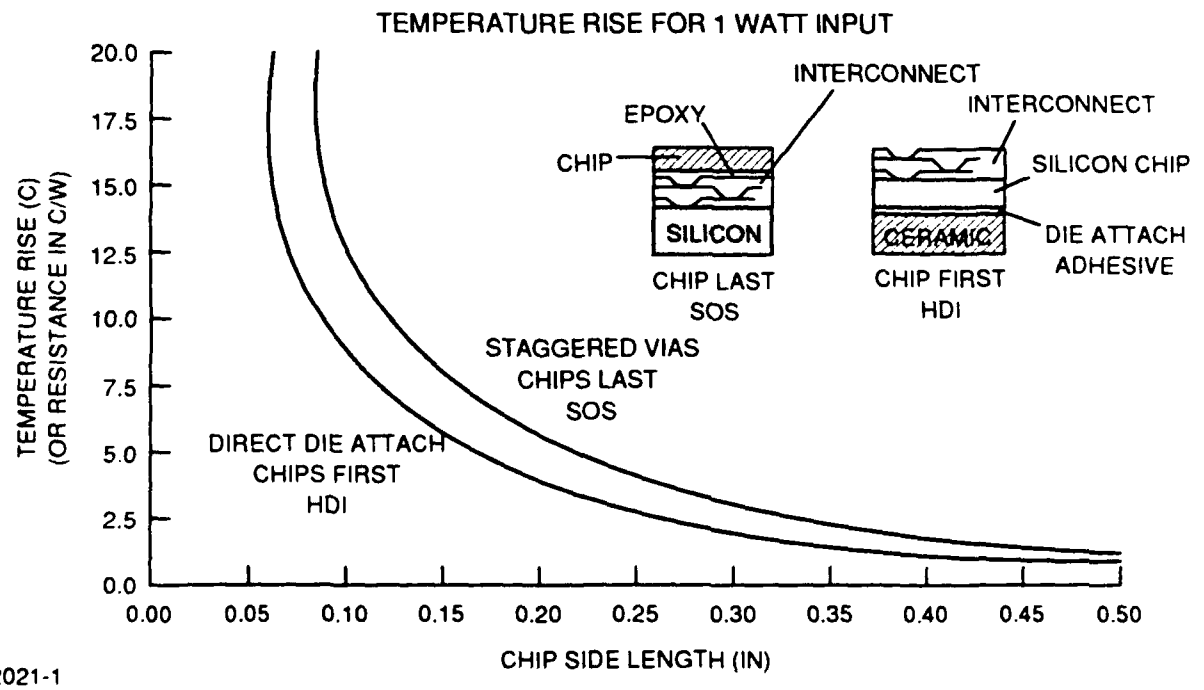


Figure 2-1. Temperature Rise for 1 Watt Input

The GE-HDI chips first interconnect technology has advantages in all these areas. Both case studies showed these advantages to be:

- Better silicon chip to substrate utilization
- Smaller size
- Enhanced thermal performance
- Enhanced electrical performance
- No added IC processing costs
- Reduced interconnect fabrication costs.

Additionally, the QTAI approach would provide reduced non-recurring costs and faster prototyping when compared to other SOS chips last approaches. However, the GE-HDI chips first approach has the advantage of no added non-recurring costs.

Overall, the GE-HDI chips first approach is a lower cost process for rapid prototyping, low volume production and high volume production.

3.0 BUSINESS PLAN

The business plan proposed by the TI/GE team is focused on developing a market driven merchant multichip module foundry. A baseline market survey has identified the total available market for multichip modules in the United States, segregated the captive multichip market as unavailable to a merchant foundry and categorized the remaining market requirements as the served available market from which the proposed foundry would develop its business base.

The market survey provides the basis for selecting and qualifying target market segments that will generate the business base to support the foundry and fan out the technology for business growth. Product requirement definition in the selected market segments enhances this ability to define the facility and investment requirements to successfully compete in the market place.

A competitive analysis reveals the competing technologies and the unique strengths of the companies offering these technologies. From this analysis, the TI/GE team has been able to determine the product and service offerings which reflect the distinctive competence in achieving a competitive advantage in those market segments TI has chosen to pursue.

3.1 MARKET SURVEY

The market survey methodology consists of an analysis of purchased surveys and a sample survey of selected respondents in key DoD programs and commercial market areas. Drawing on lessons learned from new technology introductions over the past several years, namely ASIC and SMT, TI's study purposely sought a broad market perspective to insure the proposed MCM technology represented real system solutions and not a technology seeking system insertion opportunities.

The analysis of purchased surveys focused on the commonality of reported market metrics, technology descriptions, product descriptions, market timing, market segmentation, competitive technologies and companies, and customer service and support requirements.

An emerging technology is difficult to analyze and often suffers from pragmatic subjectivity. MCM technology is especially difficult to study due to the lack of a mature technology base. Descriptions of what an MCM is and the technology relationship to hybrids further complicate the issue. A definition of MCM was developed by the team as a technology baseline to test our business plan assumptions.

The definition is as follows:

MCMs are high density, high performance assemblies of multiple bar ICs interconnected with thin film dielectric structures. These are characterized by fine line conductors (approximately 1.0 milli-inch), high silicon density (approximately 50 percent), low dielectric constant (2.0 to 3.5), and high speed capability (100 MHz or greater).

To achieve the broadest perspective of the MCM market, the SWAP team chose two companies who have provided consistently good market analysis for TI, a company with a focus on the DoD market, the Hybrid Marketing Research Council 1990 program, and a company with a good perspective of global technology and market status.

The TI/GE team with the help of its university and industry team members developed a MCM market survey for distribution to a small market sample of DoD programs and commercial market segments. Survey participants were selected on the basis of a perceived near term need for MCM technology and potential for significant production volumes within the next 2-4 years. Where possible, the requirements of the respondents were extrapolated based on the published share of market data for their company to arrive at a total available market for the segment participated in. The results of the survey were compared to the analysis of the purchased surveys where applicable. Any significant differences were rationalized and the final results normalized to reflect the highest figure of probability. (See Figure 3-1).

Responses to the SWAP Program Multichip Customer Survey are shown in Appendix A. Extrapolation of data in segments of the computer and military survey results were found to be in essential agreement with purchased surveys.

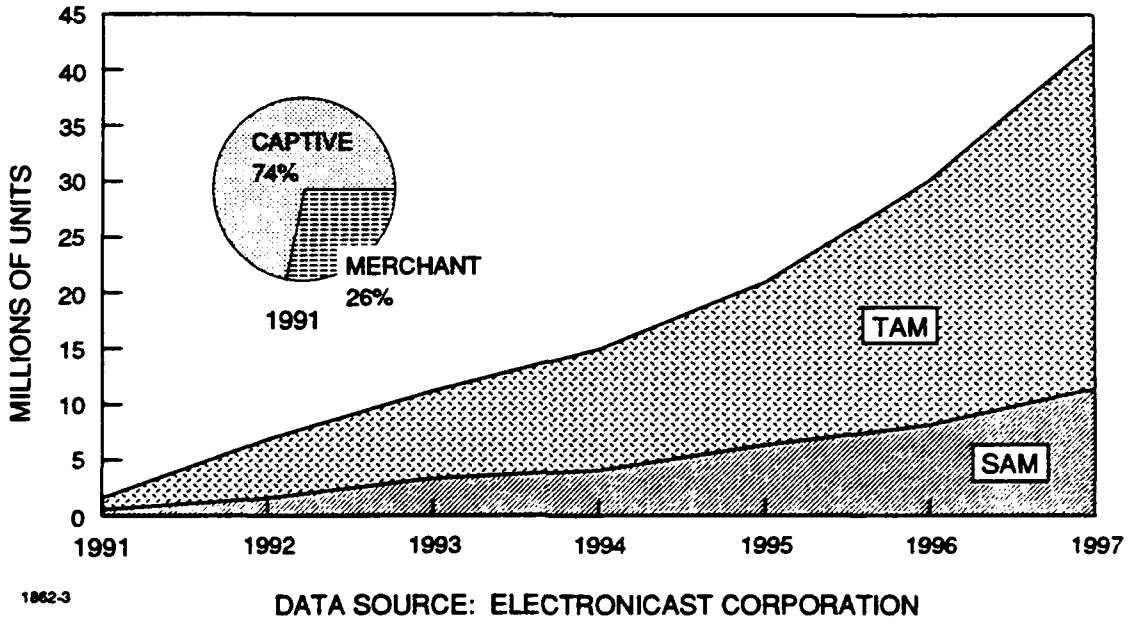


Figure 3-1. MCM Module TAM/SAM Analysis

3.1.1 Market Segmentation

There is industry consensus on the most viable market segments for multichip module insertion. They are:

- Computer
- Military
- Telecom
- Automotive
- Test
- Consumer

The computer market is being driven by competitive pressure in system performance and packaging - faster and smaller! The mainframe segment is characterized as having a high MCM content with leading edge performance requirements. Workstation opportunities will have a smaller MCM content, but a large number of system shipments. The personal computer/laptop/notebook segment will require extremely large numbers of MCMs, but will place a requirement on the market only after the technology approaches or meets parity with current technology costs.

The military market will continue to be the mainstream driver for leading edge, high performance MCM designs. With the exception of some smart munitions applications, the volumes for military MCM requirements will be relatively low when compared to other market segments. However, the military market will benefit from the commercial volumes and the process improvements developed to achieve low cost, high volume production to meet commercial requirements.

A possible exception to predicted low military MCM requirements is predicated on implementation of a number of system upgrades under discussion. MCM solutions appear to be the technology of choice in a large number of the proposed upgrades.

The telecommunications market MCM requirements are performance and packaging related but face severe competitive price pressures. Availability of high volume, low cost MCMs will be the basic requirement for market participation except in those cases where system performance requirements dictate the use of the most advanced technology available.

The rapidly growing electronic content of automobiles and increasing functionality requirements of electronic systems on board represent a major MCM insertion opportunity. The automotive market segment has, in addition to cost sensitivity, some unique packaging requirements relating to the operating environment. Low cost solutions with high reliability designs that address hermiticity, temperature, and mechanical stress issues will successfully compete in this market.

High end consumer and test equipment will present an oportunity for MCM insertion as the technology matures and will be the beneficiary of MCM volume production cost reductions driven by other market segments. High Definition Display Technology (HDDT) designers are evaluating MCM technology as a system solution.

In Table 3-1, a further analysis of MCM market segments is shown. Due to the immaturity of the technology, the MCM served available market (SAM) as shown in Figure 3-1 is perceived as having some of its requirements met by current packaging technologies, primarily hybrids. That perception coupled with the clear lack of an industry standard definition for MCM led to the reduction of the SAM shown in Table 3-1 to reflect a judged MCM SAM.

The market threshold price data shown in column(s) A in Table 3-1 is plotted in Figure 3-2. This represents the threshold price for given market segments and is based on market survey data. The baseline and enhanced HDI price forecasts are plotted for 2 and 4 layer complexity MCMs for both military and commercial manufacturing requirements. The projected MCM price curve reflects change as a function of volume and foundry enhancements proposed in the SWAP program. Where the projected price less chips is below the market survey threshold value, penetration into this market segment is expected to be large. Where the projected price less chips is above or boardering the market survey threshold value, penetration into this market segment is expected to be limited to higher end applications.

Note that the foundry may be expected to serve both military and computer market segments per this analysis; both are performance driven into MCM use and the price less chip forecases are compatible with customer market survey results. As MCM prices are reduced due to technology improvements and learning, new market segments will open up, specifically in the areas of telecommunications and automation.

3.1.2 Market Opportunity

Based on the market analysis in the previous section, the Merchant MCM foundry market penetration levels were determined. Three levels of market penetration are identified in Figure 3-3 to describe the scope of the business opportunity which will drive the TI foundry manufacturing and capital planning.

The market analysis concludes that in order for the foundry to take advantage of the late 1992 to mid 1994 market gap and fan out MCM technology, a more aggressive business plan must be executed than represented by the minimum market share curve. The detailed facility, capital, and technology development plans described in Section 4.0 are based on the aggressive market share curve.

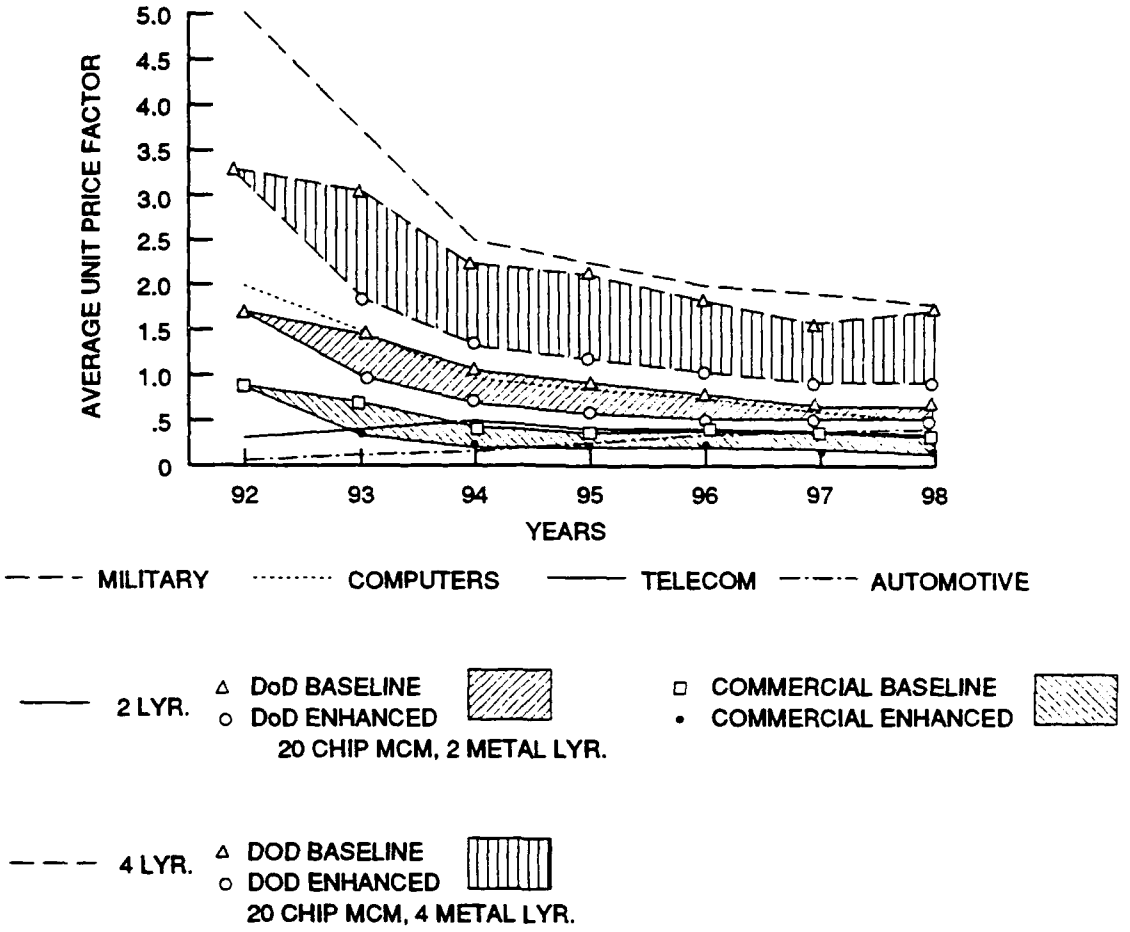


Figure 3-2. MCM Price Sensitivity Analysis

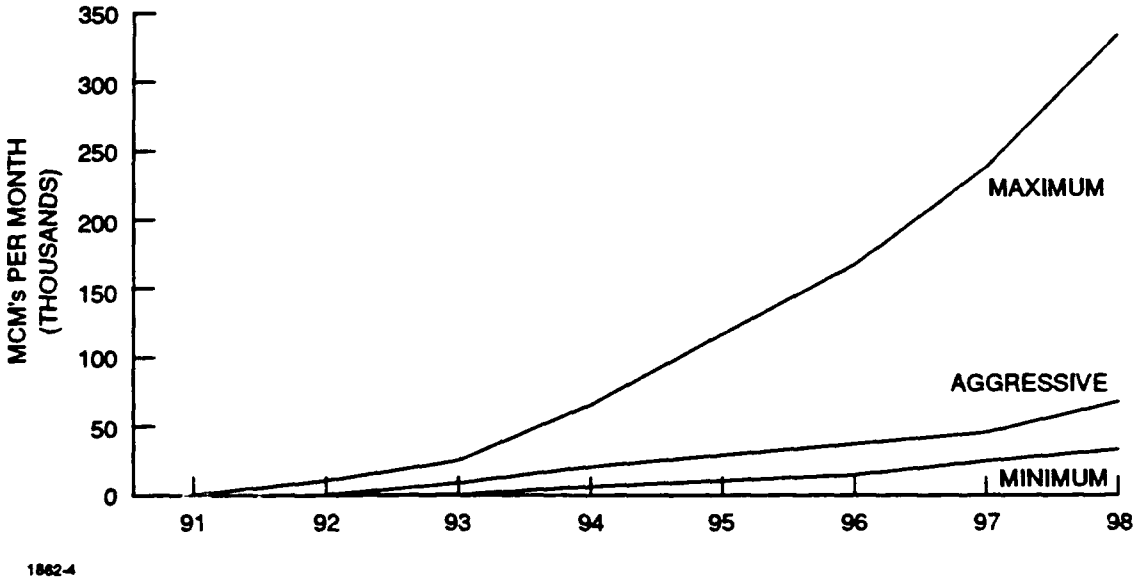


Figure 3-3. MCM Foundry Market Opportunity

TABLE 3-1. THIN FILM MCM MARKET SEGMENT ANALYSIS*

Market Segment	1992				1995				1997			
	(A)	(B)	(C)	(D)	(A)	(B)	(C)	(D)	(A)	(B)	(C)	(D)
Military	$50X	170K	50.0%	85K	$22.5X	1175K	65.0%	800K	$18X	5000K	80.0%	4000K
Computers	$20X	600K	10.0%	60K	$ 8.5X	2500K	25.0%	700K	$ 5X	12000K	50.0%	6000K
Telecommunications	$ 3X	220K	15.0%	33K	$ 4.5X	2000K	27.5%	575K	$ 3X	7000K	50.0%	3500K
Automotive	$.75X	0	0.0%	0	$ 2.25X	550K	30.0%	210K	$ 4X	10000K	50.0%	5000K

* Data extrapolated from Electronicast and TI/GE SWAP Survey

(A) Market Threshold Unit Price
(B) Thin Film Total Available Market (TAM)
(C) Percent of TAM Served by Merchant Foundry
(D) Thin Film MCM Served Available Market (SAM)

3.2 PRODUCT DESCRIPTION

In order to determine how the MCM foundry can respond to each of the MCM market segments described above, the TI/GE team must determine what the products are for each of these. The MCM products must be defined in terms of complexity (number of chips, interconnections and I/O), performance (clock rate, power), environmental requirements, second level packaging approach and, most importantly, cost requirements.

Complexity and performance requirements will drive the costs of the MCM for a particular product type through module area and module yield. The module area will be determined by the number of chips per module, the total chip area and the interconnect density. The consultant surveys and our own questionnaires provide the following product mix:

Chips per MCM	Percentage
5 or less	6%
6 - 10	36%
11 - 15	33%
16 - 30	16%
31 or more	9%

To meet the dual goals of cost effective rapid prototyping and low cost for high volume, conservative design rules would be used in the design of MCMs. The number of chips that can be interconnected per one square inch of substrate area with the HDI technology will vary with size, pin count and power dissipation of the chips and the interconnect complexity of the module design. With current state of the art IC technology, 6 to 10 chips can typically be interconnected on only 1 square inch of substrate with conservative HDI design rules. With the above estimated MCM chip count spread, the average number of chips per substrate will be 12 to 15, while the average HDI MCM substrate will be 2 square inches or less. This market survey by outside consultants is supported by TI's own SWAP survey of military and commercial MCM users.

For any MCM foundry to achieve both low costs at high volumes and rapid prototyping of low volume designs, a family of standardized substrate footprints and packaging options must be established. The IEEE sponsored MCM Size Standards Task Force has been organized to establish standards for both the substrate footprints and for MCM. This committee established the LCC and LDCC package standards in the 1980's. The task force is looking at substrate standards that are compatible with both silicon wafer sizes (5, 6 and 8 inch diameter wafers) and ceramic and other non-silicon substrates (6, 8, and 10 inch square substrates). These standards will be independent of choice of substrate material, MCM process, or manufacture.

Both GE and TI are participating in this standardization activity and plan to insure that the proposed TI SWAP foundry support the industry standards that are expected to come out of its work. This will be critical to the success of the foundry in several areas. The substrate carrier standards will drive down the costs of carrier handling equipment, the substrate size standards will allow customers to use substrates from different MCM foundries

in common packages and the package standards will reduce the costs associated with substrate fixturing and package fixturing for test, the costs of the MCM packages and the costs associated with inserting a new technology into the board assembly world. As an example of these costs, although ceramic MCM packages can be soft tooled for as little as $10K, the costs of tooling a test socket for the same package can cost more than $100K.

3.2.1 MCM Market Analysis

In TI's market surveys, a broad range of market segments were included; automotive, military (including mainframe, workstations, PC and portables), Telecommunication, and Consumer. The military, mainframe and, to some extent, workstation segments are performance driven while the automotive, lower commercial, telecommunication and computer segments are price driven. All of these market segments have different performance versus price curves that relate how much more a segment will pay for more performance. High end systems have a 1:1 relationship, willing to pay nearly twice as much for twice the performance. The lower end systems will pay nothing for performance beyond the minimum required. Each of these MCM market segments have different requirements in terms of module complexity, chip complexity, performance, environmental tolerance and reliability. Any MCM foundry will be able to make inroads into these different segments only to the extent that it can meet the price/performance requirements of each segment. The following paragraphs of this sections will look at each of these MCM market segments, identify the price/performance requirements and forecast the likely MCM foundry penetration.

3.2.2 Military Electronics

The military electronics market, though very diverse is generally performance and reliability driven with component price a lower priority. The market can be broken down into several key areas; Avionics, shipboard and ground based missiles, satellites, man-portable hardware, and smart munitions and weapons. Performance is measured not only in terms of throughput but also in terms of size and weight, reliability, and robustness in harsh environments. Shipboard and ground based electronics have had little need for smaller hardware while satellites and smart weapons systems will pay a high premium for smaller and lighter hardware.

Space and missile applications have reliability as the most critical requirement, with weight the next most critical area. The extra prices associated with achieving high reliability and light weight are trivial next to the price of lifting larger payloads and replacing failing systems. A summary of environmental characteristics for the MCM market is shown in Tables 3-2 and 3-3.

At this time, most satellite electronics use old devices and old packaging technologies that, although lower on performance (i.e., less computational power per pound), have a demonstrated reliability track record. As the data, signal, command and control, and communication requirements increase for these systems, the latest ICs and the latest packaging technologies will have to be used. The leading areas of MCM insertion are solid

TABLE 3-2. ENVIRONMENTAL CHARACTERISTICS: AUTOMOTIVE/COMMERCIAL/CONSUMER/MILITARY

	Automotive	Commercial	Consumer	Military
Temperature	-40 to 125°C	0 to 70°C	0 to 40°C	-55 to 125°C
Humidity	65% RH/85°C	Controlled	Normal ambient	85% RH/85°C
Shock	150 g	Minimal	Minimal	1,000-100,000 g
Vibration	20 g, 20-2000 Hz	Minimal	Minimal	20-100g/20-2000 Hz
Chemical Resistance	Salt spray, Automotive fluids	Generally not resistant	Not resistant	Salt spray

TABLE 3-3. BASIC CHARACTERISTIC: AUTOMOTIVE/COMMERCIAL/CONSUMER/MILITARY

	Automotive	Commercial	Consumer	Military
Volume	High	High	Very High	Low
Price	Low	Low-Moderate	Very Low	High
Reliability	High	Moderate	Low-Moderate	High
Product Life	Moderate	Moderate	Short-Moderate	Long
Product Cycle	Short-Moderate	Moderate	Short	Long

state memories, built-in-self-test (BIST), data processing, signal processing and communication. Satellite systems must shrink in size as they are asked to perform more tasks. Once the predicted higher reliability of MCM technology has been demonstrated and a number of qualified suppliers are available, all new satellite designs will begin incorporating MCM technology. Once the reliability of the technology is demonstrated, then the size and weight advantages of MCM technologies will sell the technology at virtually any price. This is also true, to a lesser degree, on commercial satellites.

Ground based and shipboard electronics will not enter into the MCM world until they are driven there by the use of higher performance semiconductors or the switch to smaller platforms. For retrofit of newer, higher performance electronics into older platforms with fixed footprints, there will be opportunities for MCM insertions.

Avionics and electronics located on aircraft are driven by a combination of size, performance, reliability and prices factors. In addition to the added weight that inefficient electronics add to an aircraft, a take-off weight multiplier of 4:1 results from the added aircraft structure and fuel necessary to support the extra electronics weight. As higher performance devices are used to meet the ever increasing performance requirements of the next generation aircraft, there will be a larger and larger size, weight and performance payoff in switching to MCM technology.

Smart weapons and smart munitions are two fast growing military electronics areas that both require MCM technology. In addition to a sensor system that locates and tracks targets, these smart weapons require a large signal processing capability and data storage. MCM technology is necessary to package the complex ICs in a small volume. Because most of these systems have distributed processing, faster processing speeds means fewer processors. Since these systems are either launched or shot, they have severe mechanical environmental requirements. Therefore, MCM technology is required for size, robustness and performance while prices will be a secondary issue. MCM technology will dominate this area with price targets comparable to missile electronics.

The area of man-portable electronics has always required smaller and lighter hardware. What is changing now is the increase in capability that is being required for the same or less weight. This pushes this area into complex ICs and into MCM technology. High performance signal processor chipsets and data processing chipsets will be the main MCM application area with memory a secondary area.

3.2.3 Automotive Electronics

The automotive electronics market is a rapidly growing MCM market segment. Automotive electronics have moved from discrete components performing simple sensing and control to todays medium level of integration for more sophisticated sensors and controllers to tomorrow's complex multi-processor smart systems. The electronic content has grown from less than $400 per vehicle in 1980 to over $800 in 1990 and is forecast to surpass $2000 by the year 2000. With more than 5 million US cars per year, that will represent a $10 billion market.

Automotive electronics must withstand a harsh environment (see Table 3-1), often in excess of military requirements, at prices comparable to low end commercial electronics. Most of these modules are mounted within the engine compartment where temperatures range from -40°C to +125°C. Mechanical shock and vibration are as severe as military Class 8. Non-hermetic multi-component modules with gasket seals and polymer potting are used to provide a long product life in a harsh environment at low prices.

As the electronic content of each vehicle increases, the complexity of automotive modules will increase beyond the limits of traditional hybrids much like the high end commercial has outpaced single chip packaging. A lower price form of multichip module packaging will be required with high density interconnect, robustness in harsh environments, low prices and high reliability. To meet the price goals, non-hermetic MCM technologies

will be needed. An HDI MCM with a plastic (composite polymer) substrate would be lower price and could have robustness and high reliability. The Automotive MCM market will have a low chip count and will have a price target in the $100 to $200 range for prices per module less chips. The high volumes per type of automotive MCM, 100,000 to 500,000 per design, will also drive the prices lower.

3.2.4 Computer Electronics

The computer electronics market segment for MCM volumes, because of its diversity, must be broken into three groups: mainframes, workstations and PC's and portables. The mainframe MCM market is generally captive (>90%) with IBM in the U.S. and NEC, NTT and others in Japan controlling most of the market. State-of-the-art mainframes will have virtually all of their high end electronics assembled into MCMs. The mainframe market is already becoming dominated with high performance, high chip count (to 100 or more), high module I/O count (1000 to 2000 or more) MCMs. This market area is driven by performance first, then reliability and finally prices. Because the market is dominated by large vertically integrated companies, the MCM volume is generally captive and not available for foundry penetration.

Workstations and servers represent the mid-range of the commercial performance spectrum. Workstation chip sets are now coming available with a 50 to 80 MHz clock rate and with 300 pins per chip. For the next generation workstation, both a data processor MCM and a graphics processor MCM will be included with each system. These markets will be willing to pay a premium in terms of higher prices for the higher performance that MCMs offer. For a typical 5 to 8 chip processor chipset, this could mean module price less chips in the $300 to $400 range. Servers with higher throughput requirements, will have more chips per module (30 to 40), higher clock rates (200 MHz or higher) and higher power dissipation (100 watts or more). These modules will be performance driven with prices a secondary issue and the increased complexity of these modules pushing the MCM price less chips to $500 or more.

PCs and portable electronics such as "lap tops" are in a more cost driven market area. Present requirements do not require the higher performance that MCM technology can bring. This market area will only utilize an MCM technology if it is price effective. As the performance requirements of PCs start to approach that of workstations and the processor chipsets go beyond 40 MHz or so, MCM approaches must be considered. A small price differential would be acceptable for a higher PC performance. MCM price less chips in the $100 to $200 range would be necessary for significant market penetration.

3.2.5 Consumer Electronics

The consumer electronics market place is characterized by high volume, low prices, lower performance and short product life. It is a market dominated by Japanese, and other Pacific basin countries. These countries utilize the large market as a funding source for their whole electronics industry. The market includes audio, TV, watches, games, telephones and some PCs. The objective is increased features rather than strictly performance, at minimum

prices with rapid product development to product insertion cycles to meet rapid growth, short product life markets. First to market means market share and large profits. Prices per module would have to be in the tens of dollars per substrate to be competitive. Market penetration by any MCM foundry would have to be limited to only the high end consumer products and have to be at much lower prices than now forecast for MCM technologies.

3.3 COMPETITIVE ASSESSMENT

Packaging in the United States has suffered from lack of "System Level Solution" thrust to the introduction and coordination of new technologies. Industry has suffered from lack of a coordinated development of a supporting infrastructure. Corporate capital has focused on the short term need, rather than on the long term vision; a trait encouraged by the point solution tendency and lack of infrastructure coordination. Industry focus has been on device development and manufacturing improvements. With the notable exception of DEC and IBM's work in MCMs and work funded by the Air Force and DARPA, advanced MCM concept development has occurred in mainly several start-up companies funded by venture capital. However, a review of the patent positions held by U.S. companies does indicate a growing portfolio of key MCM processes as shown in Table 3-4.

Some advanced MCM concepts have been demonstrated in prototype production with unique features as shown in Table 3-5. However, industry observers are concerned over the start-up companies apparent lack of financial resources to fully commercialize developments and compete in the market until it begins to expand in the mid-1990s.

TABLE 3-4. POTENTIAL MCM PATENT BARRIERS

Features	Patent Holder
Mechanical Planarization	MCC, NTT, Uni Structures
Laser Weld TAB Attach	MCC or GE
Solder Bump Process	IBM, Toshiba
Bare Chip Bump Process	Uni Structures
Thick SiO^2 Process	n Chip
Laser Pentography	n Chip, GE
Hermetic AlN MCM Package	Rockwell, GE
AlN Large Cavity MCM Package	Hughes/WR Grace
MCM TAB Process	DEC, GE
3D RAM CUBE	Irvine Sensors, TI, Thomson-CSF

TABLE 3-5. UNIQUE FEATURES OF COMPETITIVE MCM TECHNOLOGIES

Competitive Features	Companies	Advantages/ Drawbacks	GE-HDI Status
Plated-Up Vias and Lines	MCC, NEC, NTK, N77 Uni Structures	Planarization Lower via resistance	Under development on GE-ONR research contract
Barrier Metal on Line Edges	MCC, NEC, N77	Theoretically higher reliability	Under development on GE-ONR research contract
SiO_2 on Si	n Chip, ATT	High thermal conductivity Integrated decoupling capacitor	Develop high K dielectrics
Thin Film Resistors	n Chip, ATT	Few components Better termination	Under development
Improved Dielectrics	Rogers, Rockwell, MCNC	Improved signal integrity Improved reliability	Under development
Substrate Testing Prior to Chip Mounting	All	Simple Go/No Go testing Scrap at lower costs Easier chip removal	Bare chip pre-test Short/Open & Testing ECN capability

With the increased competitive pressure for improved system performance being placed on key market segments including military, computers and telecommunications and the advancement of MCM technology as a leading edge technological system performance solution, a market window of opportunity is rapidly opening. The U.S. packaging industry will be seriously challenged in filling domestic MCM requirements. Lack of manufacturing capacity, immature technologies, and the lack of an MCM industry infrastructure are major road blocks that will have to be overcome to successfully compete in world markets and continue support of U.S. defense technology development.

Part of the U.S. MCM market will be filled by IC suppliers who will offer high end processor chipsets using, 3 to 10 chips, as an MCM. This will increase performance and density for those functions over single chip approaches. Suppliers will then be limited to standard chipsets and to only their own chips. Most MCM's are ASICs in nature and require chips from a number of IC suppliers. This will severly limit market penetration of the single chip source approach.

Given the market economies and the visibility of MCM technology, the probability of the shortfall in domestic MCM capacity being filled by off-shore manufacturers is very high. Companies in Japan have for a number of years committed financial and human resources to develop packaging/interconnect and assembly technologies. A recent review of

companies with active MCM development activities shows at least nine Japanese firms with technology in place.

Packaging in Europe has been advanced by either large, vertically companies or by government sponsored multi-country consortiums. Some mainframe MCM insertions have been observed, but most of the work is in the prototype stage for both captive and cooperative research efforts.

A clear picture has emerged from this study which leads to the conclusions that:

- MCM technology has broad acceptance in the electronics industry as the next technology evolution required to meet the increased challenge for system performance, size, and thermal management.

- The primary drivers for MCM technology insertion are the military, computer, and telecommunications market segments.

- A viable business opportunity to fill the requirements of the military, computer, and telecommunications exists.

- The pent up market demand for MCM technology will be filled by the accelerated development of domestic MCM merchant foundry capacity, or the business opportunity represented by the forecasted market demand will become the target of off-shore competition.

3.4 CUSTOMER INTERFACE

The initial customer interface will utilize existing field service representatives of TI's Semiconductor Group and Defense Systems and Electronics Group. Additionally, a direct marketing activity will be focused on contacting DoD laboratories and key commercial opportunities regarding MCM technology and the availability of foundry services. Foundry services will be available to all customers requiring multichip module products and services.

The foundry customer interface will be integrated from the initial customer interface to the shipment of completed modules. In essense, the foundry will be blended with the customer and his requirements through the Computer Integrated Manufacturing (CIM) concept described in Section 4. This concept comprehends the integration of design, manufacturing, and test within the foundry as well as providing effective, validated customer interfaces.

The customer will have the ability to integrate the outputs of the CAD and CAE Systems into the foundry with the procurement and factory planning systems allowing tracking of production status. The CAD system must support design entry at various phases of the MCM design process to accommodate both foundry CAD and customer CAD.

The MCM test methodology roadmap, delineates the basic test areas; incoming, manufacturing defects, and functional. A flexible methodology is proposed to allow the

foundry to take advantage of vendor capabilities and foundry test methodologies in offering the customer options in making the determination of the specific test method, or combination, to use on an individual product based on factors such as cost and performance.

The customer interface must be dynamic in nature, continually evolving to meet the changing needs of the customer. Implementation of concurrent engineering is a key enabler to MCM success. Consideration of "all elements of the product life cycle from conception through disposal" will insure the user's best interest is served with a product that best meets their performance, cost, reliability, and delivery requirements.

3.5 FACILITY DESCRIPTION

3.5.1 Facility Requirements

The initial facility, implemented as a result of the Merchant MCM foundry program, will require 2000 square feet of manufacturing clean room space and can be extended to produce 1000 MCM/month. The high volume, low cost facility will be an addition to the initial low rate foundry, and will require 9,000 square feet of additional clean room space. This facility addition will have a capacity of 15,000 MCM/month. Administration and support area will be separate.

The addition of the high volume, low cost facility will be market driven, and is anticipated to begin between 1992 and 1994. The baseline low rate facility will initially supply low volume production and will transition to a production mixture of military MCMs, rapid prototyping, relatively low volume manufacturing, and rework support as the high volume facility is added.

3.5.2 GE Baseline Process Equipment Requirements

The GE HDI overlay process was implemented and currently exists in a laboratory environment. The current equipment set in the GE facility is based upon the need for basic capability rather than production efficiency. Over 390 MCMs of 40 designs have been produced to date in the GE facility.

The TI foundry startup will begin with essentially the same basic process and equipment capability used in the GE facility. Enhancements are necessary to transition this baseline system to a high volume production capability.

Planned enhancements include:

- Pre-molded substrates with metal 0 applied
- Polyimide film lamination for all layers
- Batch lamination of carriers
- Layer 1 pads snapped to grid; adaptive layer 1 only
- Mask image processing layer 2 - layer N.

3.5.3 Unique Equipment Requirements

A critical piece of equipment in the foundry is a customized adaptive lithography laser. This machine is the principal enabler for the GE HDI overlay process, and was developed and patented by the research engineering at GE.

The lithography laser has several unique features. It is able to both drill controlled shape vias for layer to layer interconnections and to pattern interconnect layers. The interconnect patterning uses the adaptive lithography feature of the equipment, where positional inaccuracies of IC placement are corrected by adaptive imaging. The adaptive feature is needed for both via drilling and image patterning because of IC placement tolerances. This machine allows the patterning and drilling laser to adjust vias and image position to true IC locations.

TI and GE have teamed to jointly develop a production version of this machine. Two lasers will be produced from this activity, one for the GE facility, and one for the baseline MCM foundry at TI. A common specification has been agreed to, and work has started on the new model adaptive patterning and drilling laser by TI's Industrial Automation Group.

3.5.4 Equipment Requirements

Long term capital planning for the foundry is driven by the business plan. At the beginning, the facility will require at least one item of each type of equipment. Some of the equipment will not be fully utilized in the early phases of production.

As the foundry production rate increases (due to increased penetration into the market) equipment needs will be driven by other factors, such as improved capacity or new requirements to facilitate cost reduction efforts. Some of the cost reduction efforts are related to a higher degree of automation to reduce operator labor content and increase productivity. Other cost reduction efforts will involve new equipment capability to support the implementation of process and material developments planned to further improve productivity and increase process yields.

3.5.5 Equipment Automation

Equipment and process automation will be the key element to the manufacture of high volume and low cost MCMs. The equipment and technology available to the semiconductor and printed circuit board industries can be used extensively to produce MCMs with minor modifications to a limited number of machines.

Automated equipment for MCM manufacture is justified by:

- Higher production output
- Reduced fabrication labor content
- Reduced contamination potential in a clean room environment

- Elimination of the human factor in repetitive work
- Improved repeatability of processes.

The latter have a positive impact on the foundry product quality as well as employee satisfaction.

The plan proposed for the high volume and low cost factory stresses flexibility in the implementation of automation. The baseline facility will be established with rudimentary process automation. The basics of process automation will be installed where applicable. Provisions will be made for planned migration into a highly automated environment within the foundry when the market demands and production opportunities justify the associated investment.

3.6 MCM COST FORECAST

3.6.1 MCM Technology Cost Comparison

TI and GE modeled the HDI overlay process against other MCM chips last technologies. Two chips last technologies considered were the MCC QTAI process and the TI SOS flip TAB process. A dual 1750A digital processing module was the basis for comparison. The results, detailed in section 2, show the optimized GE HDI overlay process to have a distinct fabrication cost advantage over other MCM approaches in both low volume and high volume production environments. While current manufacturing costs are high for all MCM interconnect technologies, the HDI overlay technology is at the beginning of its learning curve with few high volume enhancements implemented. There is tremendous untapped potential for manufacturing cost reductions as this technology matures. Competing technologies such as TAB or wire bond chip interconnect on thin film polyimide substrates have been in some form of production for up to five years, and will not see as rapid cost reductions during the next several years.

Another aspect of the cost comparison of the "chip first" and "chips last" approaches modeled in section 2 should be examined. A distinct cost advantage at the final MCM assembly level is indicated for the HDI overlay technology. This is driven by two primary factors:

- Higher silicon area density, and therefore smaller MCM interconnect area
- Chip connections are accomplished at no added cost during the interconnect fabrication process - extra TAB or wire bond IC assembly operations are required in other approaches.

For example, in the 1750A trade comparison, the HDI overlay design rules result in a MCM 1.7 square inch in interconnect area. For the same chipset, either of the chip last approaches require an interconnect area of 4 square inches. The larger interconnect area requirement for the chip last approaches is driven by the need to meet bond pad fanout pattern clearances for either the TAB or wire bond connections.

This leads to the conclusion that the common metric of cost per square inch is a poor gauge when comparing MCM technologies that offer vastly different packaging density performance for comparable interconnect fabrication cost. The cost comparison for the 1750A study, when reduced to dollar/square inch, indicates the chip first and chip last approaches are at relative parity. Extrapolation of this metric to absolute MCM cost, however, leads to a completely different conclusion. Comparison at a functional level, or at the final MCM assembly, shows the HDI overlay MCM will be an average 65% of the cost of either of the TAB IC approach. This significant reduction in cost is due primarily to the inherent simplicity of this overlay process, and it is an advantage that will be carried forward into the high volume, low cost manufacturing line.

3.6.1.1 MCM Process Cost Models. The TI/GE team developed two different factory process cost models to determine and evaluate the costs associated with manufacturing the GE-HDI overlay technology. These models are designed to determine the amount of labor, support, and capital equipment required to operate the facility based on the production levels defined in the business plan.

3.6.1.2 Static Process Cost Model. The first process cost model was developed from current process flow documents. A spreadsheet is used to model the HDI overlay process in a static environment. Labor and equipment requirements are input for the step by step process listing, and the number of MCMs per carrier, interconnect layers, and final process yields can be varied. The model outputs operator time required for a given manufacturing scenario, and indicates total machine utilization. This provides a limited tool to evaluate near term facility size and cost.

This static facility modeling method provides a snapshot viewof the HDI overlay process. It is an adequate comparison of different manufacturing options for the baseline equipment configuration. The static modeling approach is configured for processing with little or no automation.

3.6.1.3 Dynamic Process Cost Model. A second process cost model was developed using commercially available facility modeling software. The WITNESS™ software package was used to allow the facility to "learn" how to build HDI overlay MCMs better by adjusting for planned process enhancements. This capability evaluates:

- Degrees of automation
- Process yield changes
- New process techniques
- Methods and tooling changes.

The dynamic process cost model is more representative of a real world environment, where changes in the facility equipment automation and processing technique will be market driven. Equipment changes were inserted into the modeled facility per points in the forecasted growth. The effects of higher capital investment for equipment with increased throughput and automation can then be evaluated against the impact of extending the baseline

equipment set to the volume requirement. Effects on capital investment, personnel, and facility throughput can be evaluated over time.

3.6.2 MCM Process Cost Model Results

TI and GE used both the static and dynamic process cost models to determine the amount of equipment and number of operators that would be required to produce MCM modules over time. These two studies are treated as the Baseline facility and the Enhanced facility.

A study of the static and dynamic model with the aggressive business plan opportunity as a production base over time was completed. These models indicate the amount of capital equipment and staffing required and the time phasing for this business plan opportunity.

The capital equipment results are represented graphically in Figure 3-4. Static model results, designated as Baseline facility and represented with a dashed line, indicate replication of the initial facility without both equipment and process upgrades will result in significant capital investment for each business plan opportunity from 1991 through 1998. The Enhanced facility projection, represented by the solid line and generated with the dynamic model, shows significant reduction in capital investment for the same three cases of MCM production demand from 1991 to 1998.

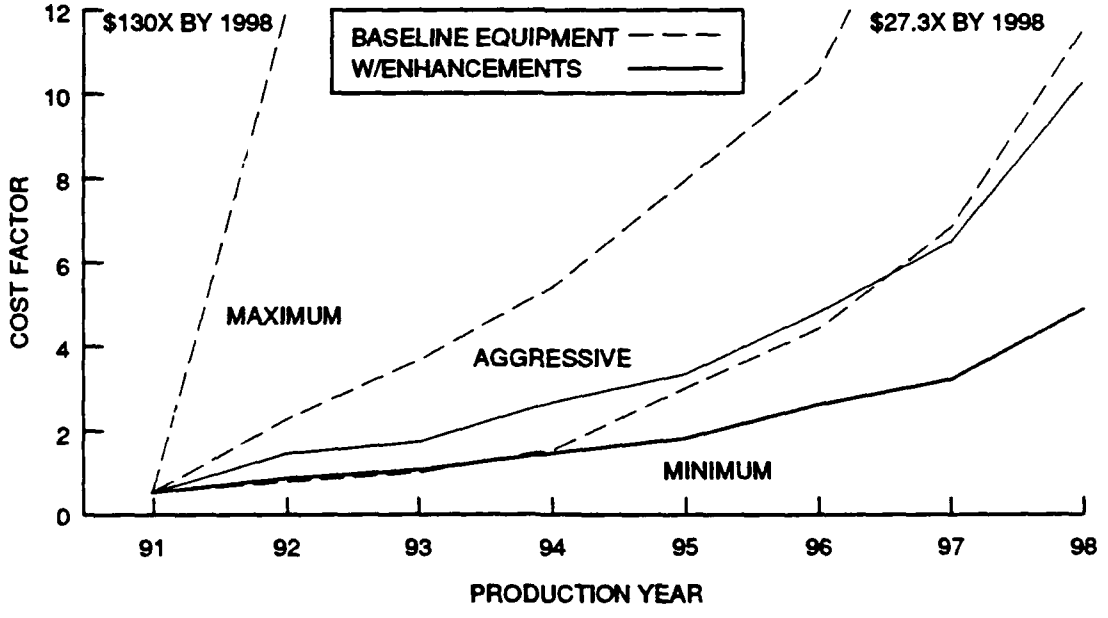


Figure 3-4. Total Foundry Capital

The staffing requirements for the foundry are represented graphically in Figure 3-5. Results are for the Aggressive business plan opportunity only. Trends are similar to those seen in the previous capital baseline and enhanced model analysis. For the aggressive business plan analysis, extension of the baseline facility will result in unmanageable staffing growth between 1993 and 1996. Analysis with the dynamic model assumptions predicts a far more achievable staff growth rate for both direct labor and support.

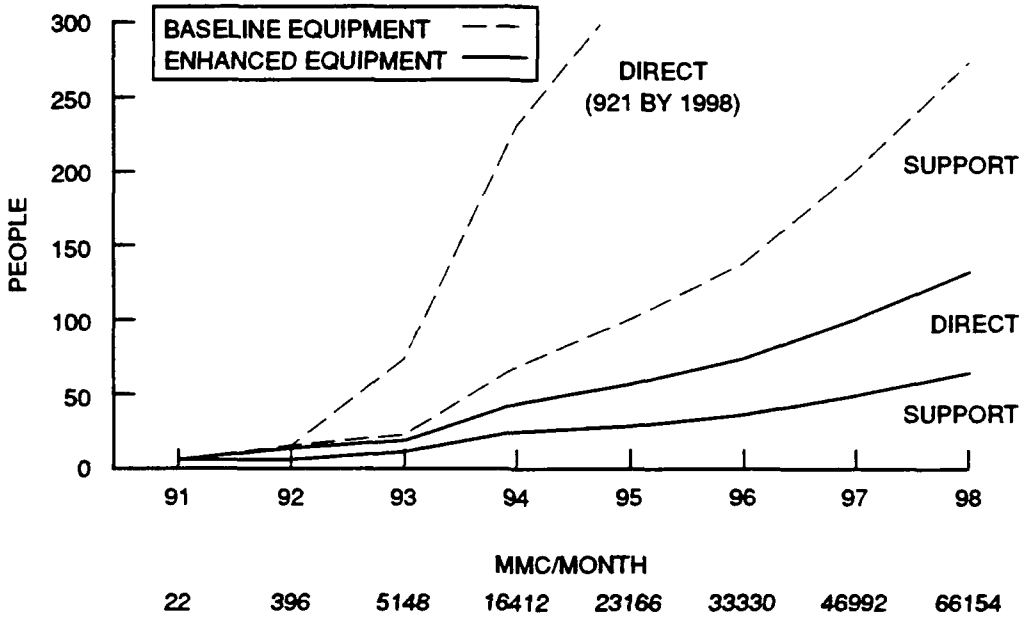


Figure 3-5. Foundry Labor Aggressive Opportunity

The analysis of the trade-offs for the Baseline facility and Enhanced facility extension into high volume lead to the following conclusions:

- The baseline facility is well matched to the near term low volume market opportunity
- Significant capital investment will be required to extend the baseline process and facility to high volume production
- Facility and process enhancement assumptions show promise to reduce both the long term investment and manufacturing labor requirements
- The window of opportunity for an enhancement program to reduce the required capital investment and foundry staff is between 1992 and 1994.

Note that the window of opportunity for implementation of enhancements to reduce high volume labor and capital corresponds to the window of opportunity for market penetration and business base growth by the foundry. There is significant risk in achieving required production improvements in time to lower both the investment and labor requirements of the baseline process, given the near term position of the high volume market opportunity. There is also risk in assuming the production foundry, deployed with the

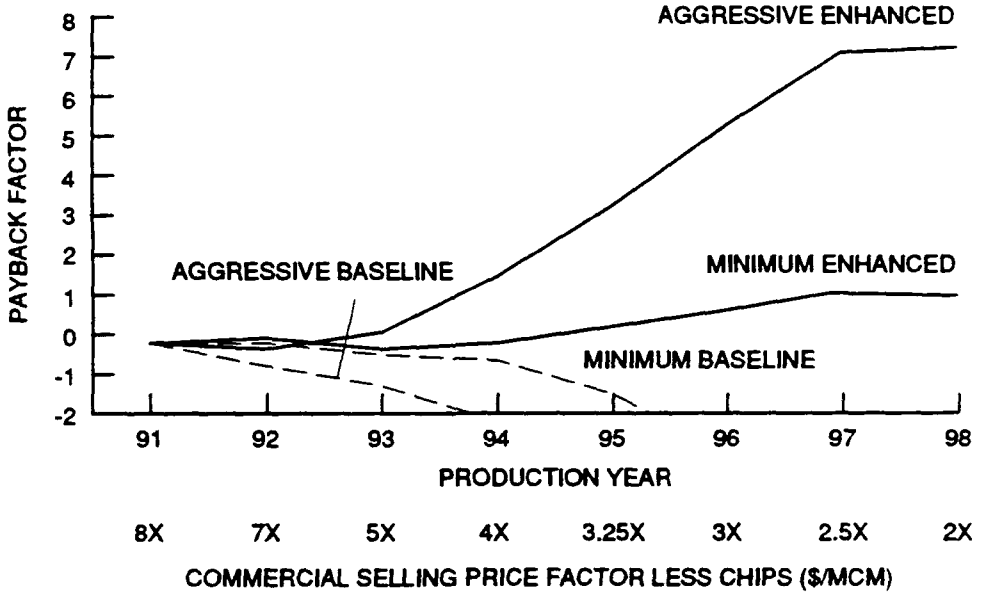
baseline MCM process, will expand as quickly as the market opportunity is forecast to develop, given the large inertial effects of the baseline capital and staffing forecasts.

A manufacturing improvements program will provide the opportunity to accelerate development of the technology and strengthen the domestic military and commercial production capability to meet this near term need. The capital and staffing facility analyses further confirm the need for such a program.

3.7 FACILITY AND EQUIPMENT INVESTMENT

3.7.1 Payback Analysis

The payback analysis is shown graphically in Figure 3-6. This chart indicates the effect of implementing two of the business plan opportunities with the Baseline and Enhanced high volume facilities. In all cases, the selling price less chips assumption was held constant at the market forecast values.



2118-4

Figure 3-6. Financial Payback

Clearly, the losses indicated by the Baseline facility extension into high volume would not be continued as depicted on this graph. Instead, the foundry would be forced to increase the selling price less chips charged to the customer to avoid a loss. This would in turn result in:

- Loss of potential market share
- Limited market segments available to the foundry
- Slower growth of foundry volume production
- Slower reduction of foundry cost; learning rate reduced

The recoveries indicated by the Enhanced facility extensions into high volume manufacturing both show positive cash flow recovery in an acceptable period of time. At the point positive cash flow is reached, the foundry would be able to lower the selling price less chips charged to the customer base. This would results in:

- Gain in potential market share
- Increase in market segments available to the foundry
- Accelerate growth of foundry volume production
- Increase rate of foundry cost reduction.

3.7.2 Investment Summary

The payback analysis indicates the baseline facility established by the Merchant MCM Foundry program can be financially viable, but in limited market segments. Figure 3-2, MCM Price Sensitivity Analysis, indicates the different market segments and the related price sensitivity over time. The baseline facility will enter the higher value market segments where the performance/cost relationship demands the MCM packaging advantages. These will be mostly military market segments, and restricted to the high end applications.

Without a manufacturing improvements program, enhancements will be driven by revenues into the foundry. These revenues will be generated by the low volume, baseline facility and are expected to be low due to this facility's focus on a narrow market segment and the low volume demand within this segment. With the demand for low cost, volume production approaching as early as late 1992, significant enhancement effort must be underway to intercept the opportunity in other market segments. Accelerated foundry manufacturing enhancement and technology development is not likely to happen without an external catalyst, such as a manufacturing improvements program. It is certain that this window of opportunity will be missed by extending the baseline process.

The payback analysis indicates an enhanced facility and process established by a SWAP program follow-on as a strategic extension of the Merchant MCM Foundry facility will be financially viable. In addition, there will be an opportunity between 1993 and late 1994 to rapidly penetrate low cost, high volume market segments and accelerate the foundry production base. A manufacturing improvements program will be essential to accelerate the high volume, low cost facility implementation and penetration into the domestic market.

4.0 FOUNDRY TECHNOLOGY INSERTION

4.1 COMPUTER INTEGRATED MANUFACTURING (CIM)

The foundry provides high-volume low-cost production of high performance (MCMs) as well as rapid prototyping at lower volumes. The design and manufacturing processes are well defined, controlled and integrated. A high degree of computer integration is determined by the product mix and productivity requirements. An integrated system manages the data, design, manufacturing, test and assembly processes as a product moves from customer requirements to a delivered product. This is referred to as computer integrated manufacturing (CIM).

Figure 4-1 shows the design and manufacturing flow. The customer may enter the system as early as the initial design concept or as late as completion of physical layout; planned entry levels are represented by shaded boxes. How the current baseline foundry systems, transferred from GE to TI, fit into the overall flow is also indicated.

4.1.1 Current Foundry System

The baseline tools are:

- HYPACK (GE developed) - designs a MCM
- Process data conversion - generates CIM data files
- PROMIS™ (commercially available) - controls and monitors fabrication processes and supports module test.

MCM designs from a number of sources have been fabricated successfully in the GE HDI facility. Much of the process is manual, and the available computer control systems are not fully integrated.

HYPACK, based upon a commercially available layout system, permits netlist information input from a large number of design platforms and allows a trained designer to perform:

- Module placement
- Routing
- Design rule check
- Parameter extraction
- Generation of a database for handoff to the CIM system.

The data conversion system is a collection of prototype software tools that generate manufacturing databases from the layout database. This collection of tools generates manufacturing files for:

- Substrate milling
- Die placement
- Laser via drilling
- Metallization patterning.

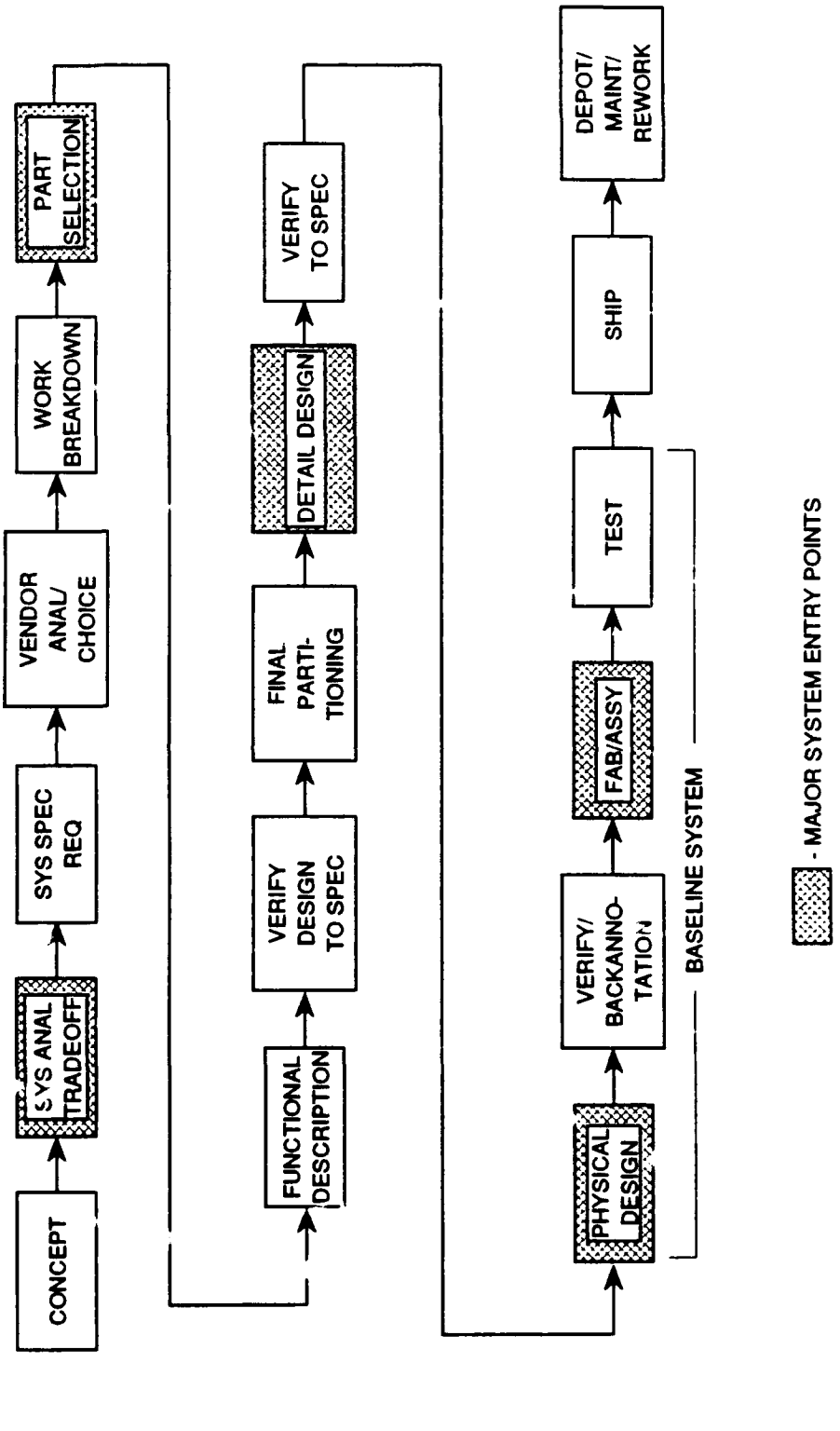


Figure 4-1. Product Flow and Roadmap

Other manufacturing steps are driven by a combination of lot travelers and process instructions.

A short/open test generated directly from the module netlist and pattern files links layout and test. Parameters from the engineering design system pass to the layout system. Within the year, the development of direct links allowing modelling and simulation capability will be complete. Data input, layout, parts selection and procurement, test plan generation, and factory scheduling are independent elements.

4.1.2 Initial Enhancements to the Baseline System

The initial enhancements generate information control systems for all foundry elements. These systems generate and transfer compatible data files designed to be integrated. A comprehensive engineering design system linked to the foundry's layout and test system is required for the design of complex MCM circuits containing as many as 20 or more chips with 50,000 to 100,000 gates per chip. To achieve first-time working designs, full MCM electrical simulation and interconnect modelling is desirable. Unlike a computer-aided engineering (CAE) system for ASIC design, which supports only one database and the gate complexity of one chip, the system for a merchant MCM foundry supports the design of chips from multiple sources, with varying CAE databases and gate complexity of 20-30 times that of one chip.

An integrated CAE system and test system is critical. The test system:

- Develops test vectors
- Translates vectors from outside sources
- Evaluates the testability of MCM designs
- Measures the fault coverage of vectors.

When integrated with the CAE system, it will take test vectors, supplied by the customer, and verify them or measure their fault coverage on an IC level. Full fault coverage and isolation to interconnect related faults is a requirement. Without an integrated test/CAE system, modules with design or defect errors might pass the available test vectors and fail later in operation. For memory intensive designs, high fault coverage test vectors are readily generated in-house with limited effort. Labor intensive test vector generation is required for those designs without customer supplied vectors.

Layout tools which aid the MCM designer to optimize a MCM design are required. Initially, a high level expertise in MCM design is required to access features such as:

- Number of interconnect layers in the substrate
- Need for dedicated power and ground planes
- Need for termination resistors
- Number and type of decoupling capacitors required
- Size of substrate
- Packaging approach.

Design requirements for test, manufacturability, and cost are being addressed currently at the GE HDI facility by experienced MCM design engineers. In the proposed foundry, these requirements will be addressed by expert systems that incorporate the expertise of GE and TI designers.

4.1.3 Proposed MCM Foundry CIM

An integrated computer system will serve the foundry from the first customer interface to the shipment of the completed modules. A structured management and planning system will control the interface between the customer and foundry. The integrated computer system will have the following functionality:

- Data management
- Part model library
- Business/marketing support
- Data communication
- CAE support
- Layout
- Testing
- Reliability modelling
- Material tracking.

The foundry requires access to a CAE capability that can extend chip modelling and simulation from the behavioral to the subsystem level. The goal is to have a commercially available system which will extract behavioral level models of a broad mix of IC types and:

- Generate a model for the MCM design
- Verify the correctness of the design
- Generate test vectors
- Verify fault coverage.

Until then, commercially available tools supplemented by in-house-sponsored tools meeting specific MCM needs will be used.

A commercially available layout system for MCM and other high performance packaging approaches allow circuits designed for one foundry or process to port to another. This layout system permits designers to input design and component data into a database once. A design starting out as a board design will then flow into one or more MCM foundries for prototype and production. Thus, the designs are transportable, allowing a cost effective method of providing a second source capability. HYPACK, the present HDI layout baseline system, can design and layout a MCM circuit for either the HDI process or one of the standard chips-last silicon substrate processes.

The layout system supports design entry at various phases of the process to accommodate both foundry and customer layout systems and allows enhancements for:

- Higher performance

- Analog, microwave, and optical electric applications
- Throughput improvements
- Yield improvements.

Layout and design system outputs must be integrated with procurement and factory planning to coordinate the arrival of databases, parts, components, and materials to the factory floor. "Just-in-time" concepts reduce MCM build time as well as inventory costs and waste. The manufacturing system tracks all lots in process and monitor material inventory. It has the capability to fulfil critical orders and perform rapid prototyping without major disruption.

4.1.4 CIM Approach

A MCM Automation Committee was formed to bring together the requirements, issues, and approaches resulting from this concept. This team consists of individuals who, collectively, have expertise in all areas of automation: design, layout, manufacturing, and test. This team relies heavily on TI's production experience and on GE's MCM research and development experience as input. Figure 4-2 lists the members of this committee and shows areas where contact was made and MCM roadmaps generated. The output from this committee includes the roadmaps which are described in the sections below.

4.2 DESIGN AUTOMATION

Section Overview: The design automation section is divided into two parts: Concurrent Engineering and Computer Aided Engineering/Layout

Concurrent engineering, a key enabler for achieving productivity in the MCM foundry, is defined, and customer requirements making this approach necessary are listed. Also, a discussion of a design automation vision and roadmap supporting the concurrent engineering strategy, implementation items, related technical challenges, and the many aspects of customer communications is presented.

The Computer Aided Engineering/Layout section presents the status of GE's HYPACK system, the strong base on which the MCM team will build the foundry's automation system. An overview of the consultants contributing to the project is given. In conclusion, design automation milestones which support the foundry's implementation are shown.

The following terms are used to group automation activities and tools used in the product design and manufacture flow:

- Design Automation (DA): entire product design and manufacturing process
- Computer Aided Engineering (CAE): electrical and mechanical design and analysis
- Computer Aided Design (CAD): component placement, circuit layout, and associated verification
- Computer Aided Manufacturing (CAM): manufacturing process.

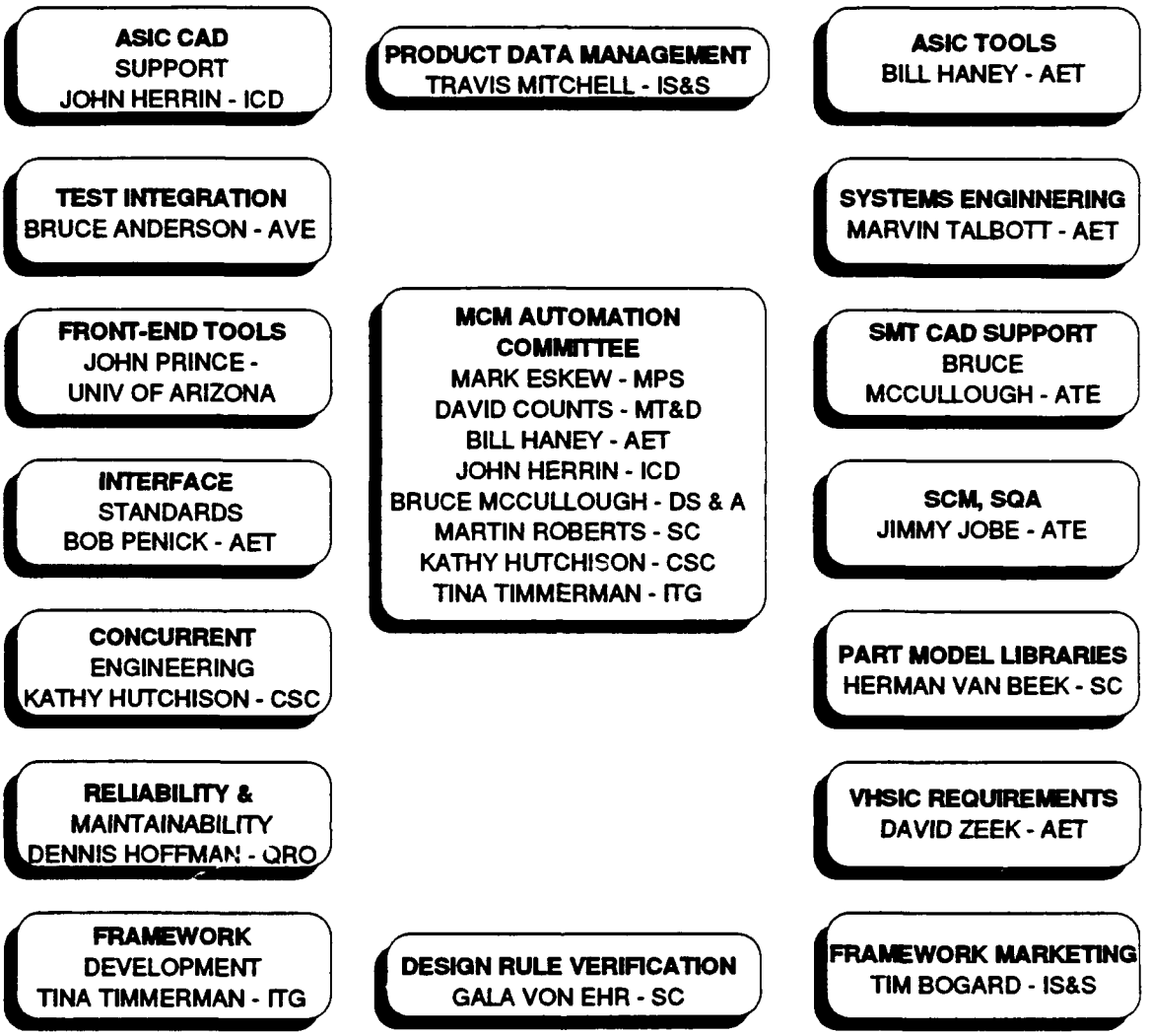


Figure 4-2. MCM Automation Committee

Abstract: **Concurrent engineering**, a key enabler for achieving productivity in the MCM foundry, is defined as a systematic approach to creating a product design that considers the total product life cycle. The following customer requirements for MCM automation systems have made this approach a requirement.

- Multiple technology support
- Transparent customer access
- Availability to customer
- Design verification
- Integration with the factory.

A MCM automation vision supporting the concurrent engineering concept was generated starting with GE's effective MCM system. It facilitates customer interfaces at the systems analysis, part selection, detail design, physical design, and manufacturing levels. Implementation of this vision includes:

- Realization of a design methodology
- Establishment of testability, producibility, and manufacturability procedures
- Provision for design rule verification
- Provision for electrical and mechanical simulation
- Encapsulation of MCM tools under a commercially available framework.

Implementation of concurrent engineering for a high-volume foundry environment leads to related challenges. They include data management, data communication, part model library, MCM-specific requirements, and system support. GE and TI expertise was employed in each of these areas, and roadmaps for addressing these issues were established.

The foundry/customer interface supporting concurrent engineering consists of many aspects. Included are data communications, input interfaces, data validation, standard formats, and interfaces to existing CAD systems.

The **Computer Aided Engineering, Computer Aided Design** section describes GE's current MCM system, summarizes the contributions of consultants to the project, gives an implementation roadmap, and discusses risks.

An integrated set of GE-developed and purchased software, called HYPACK, is in place and consists of the following tools:

- MCM placement and router
- Noise analysis
- PROMIS™ factory management system
- Input interfaces from CAD systems
- Milling operation interface
- Design rule checker
- Laser interface
- Output interfaces.

Additional software supporting the GE MCM approach includes test interfaces that run independently of HYPACK and factory automation data control systems.

HYPACK enhancements are necessary to serve the design environment well for circuits with performance greater than 100 MHz and for high-volume production. Improved transmission line simulators, back annotation capability, and more sophisticated tools for analysis of impedance and data I-noise in power and ground structures are desirable. In manufacture, design for manufacture and improved data management tools will enhance productivity.

Consultants contributed to the program in complementary areas, and several are referenced in the appendices.

The University of Arizona proposed enhancements to existing MCM tools developed under GE's guidance in support of high-speed electrical and thermal/electrical analysis.

The University of Maryland proposed enhancements to existing reliability and maintainability tools developed under their CALCE organization in support of MCM.

Task Technologies, Inc. performed a benchmark showing that the same routing system used for the "chips first" approach is capable of producing data for the "chips last" approach.

Mentor Graphics, Inc. submitted a roadmap for the encapsulation of MCM tools under their Falcon framework as driven by market requirements.

Digital Equipment, Inc. worked with the MCM team to produce a roadmap for foundry hardware and software which uses existing TI equipment as a starting point.

Layout Concepts, Inc., supplier of the router for the Task Technologies layout system, was contacted as a potential second source for enhancement and procurement of layout software.

The implementation plan consists of milestones supporting the initial GE/TI technology transfer and milestones supporting the high-volume environment, such as improved data management and ties to existing TI Management Information Systems.

Risks include the ability of the router to handle large circuits (10K -15K from to's), backup for Task Technologies routing system, the ability to incorporate analog, microwave, and optical circuitry into digital designs, and a viable part model library approach. With the exception of a layout alternative, these risks are associated with all MCM technologies.

4.2.1 Concurrent Engineering

The concurrent engineering concept is a key enabler for achieving MCM productivity goals. The Department of Defense issued a definition of concurrent engineering in MIL-HDBK-59 which states, "Concurrent engineering is a systematic approach to creating a product design that considers all elements of the product life cycle from conception through disposal." In doing so, concurrent engineering simultaneously defines the products, its manufacturing process, and all other required life cycle processes."

Concurrent engineering concepts help eliminate costly components of the manufacturing and support processes which often result when products are designed without appropriate considerations for the requirements of these operations. In the manufacturing process, for example, effort previously expended in costly special operations can be redirected to normal operations, resulting in higher throughput.

Various approaches can be taken to achieve the goals of concurrent engineering. Each of these approaches exploits a specific instance of product, factory, organization, and culture interaction. TI has considerable experience with a number of approaches to concurrent engineering, has invested in the research and development of leading edge technologies for concurrent engineering, and has taken a leadership position in industry-wide and Government sponsored initiatives involving concurrent engineering. The MCM effort will take advantage of this experience and expertise through the participation of appropriate personnel.

A single extendable, unifying data representation will ultimately be used by all capture and analysis tools to consider aspects of the design while performing an analysis. The MCM DA vision and roadmap, shown elsewhere in this document, supports this concept. The path toward this goal leverages off current capabilities and builds toward the ultimate vision.

4.2.1.1 High-level Customer Requirements. The following are key customer requirements for automation tools supporting concurrent engineering.

4.2.1.1.1 Multiple Technology Support. The DA system and its associated databases must be extendable to allow for the introduction of new technology. This includes supporting multiple implementations of the MCM technology; particularly, chips first and chips last.

Also, the system must include effective methods for not only supporting one technology on a substrate but also the integration of multiple technologies on the same substrate; particularly, passive components, ICs, and connectors for digital, analog (microwave and millimeter wave frequencies), and, if appropriate, optical functions.

Front-end analysis tools are required to ensure successful implementation of the product specification, especially during the design phase of higher frequency circuits (greater than 100 MHz). University research will aid in defining and implementing this capability.

Techniques for ensuring successful package interconnection to the encompassing system are required. System level design and analysis capabilities during the DA and manufacturing processes play an important role.

A data management approach which will support tool integration and tool evolution on the workstation, CAD/manufacturing data integration, and customer data control supporting military and commercial standards is required. Frameworks, commercial data management tools, and implementation of standards such as CALS, EDIF, IGES, VHDL, and others will facilitate this requirement.

4.2.1.1.2 Transparent Customer Access. The DA system must be capable of accepting data from multiple DA systems, commercial and proprietary. Implementation priorities for this capability are driven by the business plan and related customer environments.

Also, the DA system must support either high-volume or rapid prototyping as determined by customer business requisites and provide a cost-effective solution for either environment. Identification of the differing approaches for satisfying this requirement are critical and will be discussed in a following section.

Finally, the DA system must provide for protection of the customer's proprietary designs. CALS standards, data security, and approved foundry procedures are fundamental.

4.2.1.1.3 DA System Availability. The DA system must be configured for fanout to a customer's site. A design methodology, detailing the steps in the design process and interface, and input requirements must accompany the system. Also, a support infrastructure must exist which provides documentation, consulting services, problem resolution, software configuration management, and measurement of system performance.

The long-term goal is to implement and maintain an integrated DA system supporting design, manufacturing, and test. Phases preceding this goal are the implementation of a DA system supporting (1) fabrication services and then (2) fabrication and design services.

4.2.1.1.4 Design Verification. Verification is a key element to MCM success. The verification process becomes critical when circuit speeds exceed 100 MHz. Research from universities and national laboratories is desirable for accomplishment of this requirement.

The overall capability includes electrical/mechanical verification. High-speed digital and thermal verification are seen as necessary elements for thorough design. Integration of these tools with the CAD system, allowing system technology requirements to drive the layout, is necessary.

4.2.1.1.5 DA/Factory Integration. A data management system is required for DA/factory integration and for capturing data used for continuing product/process improvements. Information fed back for this purpose includes both CAD, manufacturing, and test data.

The data management system must provide data access and validation for all MCM activities from customer interface through product delivery and maintenance. This capability is critical for meeting the volume and cost goals of this facility.

4.2.1.2 DA Vision, Roadmap. The DA Vision and Roadmap support the concurrent engineering strategy. A more in-depth discussion of the DA vision, summarized earlier in the document, follows. Figure 4-3, depicts the vision.

4.2.1.2.1 Major Customer Entry Levels. To provide adequate procedures and tools to insure accurate communication, customer entry into the DA system must be restricted to several major points. The following discussion addresses these links with the system.

Systems Analysis/Tradeoff is the first entry level indicated. The following list of tools provides capabilities necessary to support this entry at the conceptual level:

- Partitioning
- Decision (capability requirements, tradeoffs, manufacturing, analog, cost estimating)
- What-if (power, thermal)
- Quote capability
- Life-cycle reliability data.

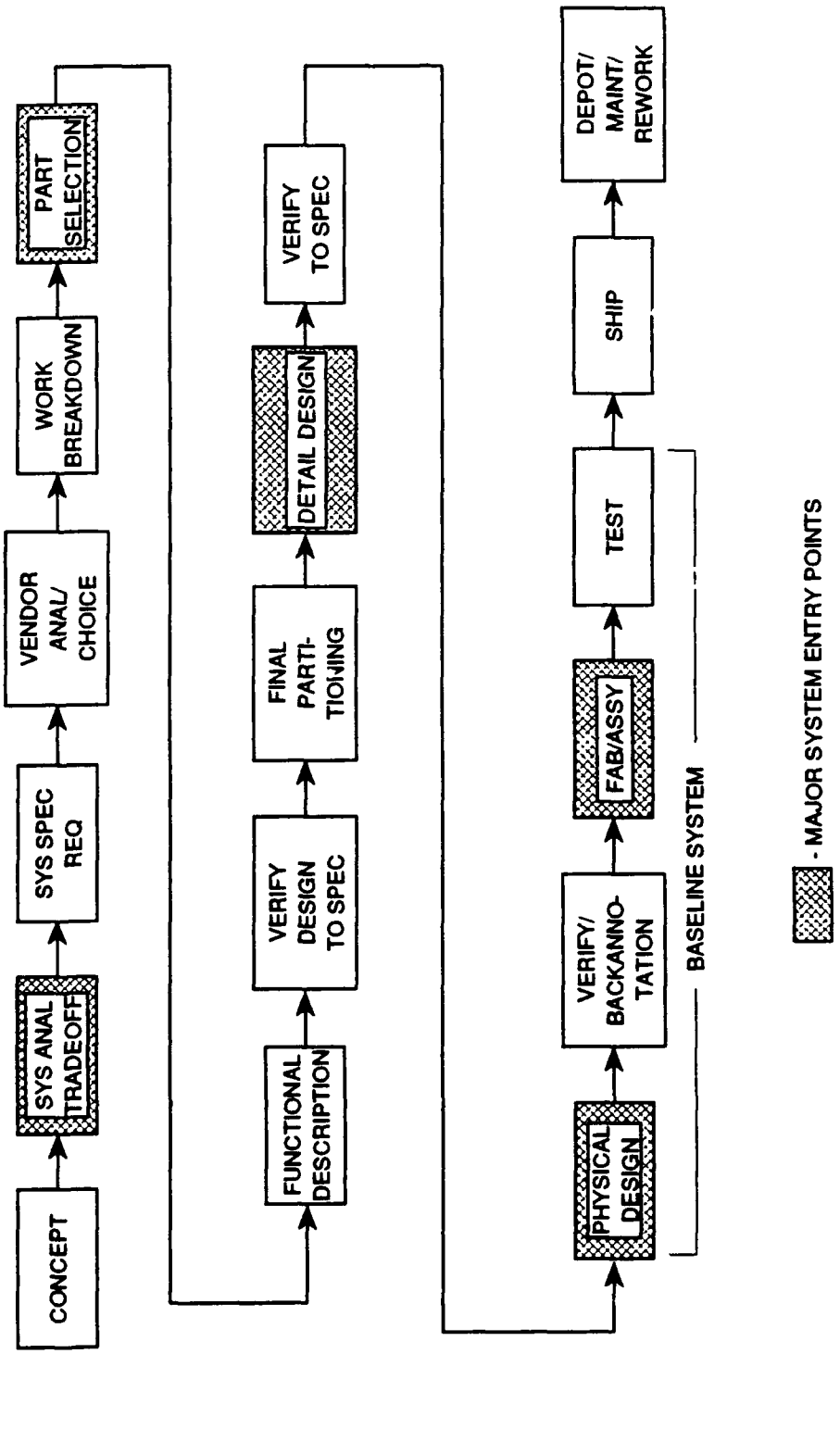


Figure 4-3. MCM Vision and Roadmap

TI has an effort underway to offer a systems level design automation capability and plans to meet these needs by 1992. Figure 4-4 gives features needed at the systems level. This capability will give two-way traceability between requirements and implementation. Also, support of hierarchical detailed system decomposition is included which is necessary when MCMs are integrated into the overall system. The MCM project will use the results of this effort in its long-range plans.

Part selection is an area of concern to all MCM manufacturers. Once the system requirements are in place, an initial cut at a parts list is made. Due to long part procurement cycles, incoming test requirements, and the desirability of parts qualified for the MCM process, the DA system must permit the use of custom parts and must encourage the use of preferred parts. This implies defining MCM part criteria and establishing a database allowing the customer to choose from a list of qualified parts at his location. A feature of the GE-HDI process is the lack of physical die restrictions, such as solder bumps, TABs, or peripheral pads.

Concurrent detail design is the next step. At this level, tools are necessary to aid in:

- Design for manufacturing and test
- Part selection (model libraries) supporting electrical and mechanical analysis
- MCM interface characteristic analysis
- AC/DC timing analysis
- Automatic test pattern generation
- Electrical simulation.

Physical design is the traditional entry level for foundry services in the printed wiring board (PWB) environment, and it will be the first level implemented in the MCM foundry. A schematic in the form of a drawing or parts list/node list defines the circuit. Establishing control over this pre-release data is critical. Validation of the data at the foundry and an effective customer interface is a necessity. Also, support of input standards such as VHDL and EDIF is required at this level. Tools enabling the customer to do his job include:

- Schematic capture
- Manufacturability and testability tools
- Placement and routing analysis
- Parasitic analysis
- Part selection (model libraries) supporting electrical, mechanical, and design rule checkers
- Assembly drawing
- Mechanical analysis (thermal, stress, vibration)
- Electrical analysis (termination, impedance, cross talk)
- EMI, RFI
- Layout system installed at the customer's location or at the foundry.

Fab/Assembly entry level is desirable for customers with access to the entire suite of MCM tools and who intend to do all analysis and design work at their facility. Cost/cycle

IDENTIFIED DESIGN AUTOMATION FEATURES NEEDED
- SINGLE MASTER SYSTEM DESIGN DATABASE ("OODB" PARADIGM)
-MULTIPLE PERSPECTIVES OF SYSTEM DESIGN "OBJECTS" (CUSTOMER REQUIREMENTS, SYSTEM SPECIFICATIONS, DESIGN IMPLEMENTATION)
- TWO WAY TRACEABILITY BETWEEN REQUIREMENTS & IMPLEMENTATION
- EXECUTABLE SPECIFICATION (SIMULATED FUNCTIONALITY, AND COMPUTED ALTERNATIVE IMPACT)
- "SELF DOCUMENTING DESIGN CONCEPTS (ENGINEER NOTES ATTACHED TO DESIGN "OBJECTS". AUTOGEN DOCUMENTS FROM DESIGN STRUCTURE & TEMPLATES)
- HIERARCHIAL DETAILED DECOMPOSITION

2111-2

Figure 4-4. System Level Design Automation

time management or protection of proprietary data are possible reasons for keeping the design and layout at the customer's site. Again, support for standard interface formats such as IGES, PDES, GDS2, and EDIF is required. Software capable of building the database(s) necessary for manufacturing and test from this input data is necessary.

Table 4-1 lists customer input and foundry services for the system analysis, detail design, physical design, and fabrication entry points.

Table 4-1. Customer Input

MCM Foundry Access Points	Foundry Services
Functional Spec	Full Electrical Design
Block Diagram	Functional Description
Timing Requirements	Part Selection
Operating Spec	Modeling and Simulation
	Test Vector Generation
Detailed Design	Partitioning
Net List	DFM and DFT
Parts List	Timing Analysis
Samples	Parts Analysis/Substitution
Test Vectors	Place and Rent
	Substrate/Package Selection
Physical Design	DRC
Interconnect Data Files	Parameter Extraction
Package Selection	Manufacturing Files
Test Vectors	
Fabrication	
Non-Tested Substrates	TEG and PCM Testing
Tested Substrates	Substrate Test
Assembled Modules	Packaging and Assembly

4.2.1.2.2 Overview of Required Capabilities. The roadmap shown in Figure 4-5 lists the major capabilities necessary to implement the automation vision. Asterisks represent accomplishments at the end of the initial technology transfer from GE to TI. They include enhancements to the basic system necessary to move it into a foundry environment. Comments on several of these listed capabilities follow.

- **Data management:** For reasons which will be discussed later, in-process data supporting the GE MCM approach must be maintained on a part-by-part basis. The increase in data volume, and its required accessibility during the manufacturing process, requires a formal data management procedure. The extent to which the data management procedure is automated is driven by production volume; thus, the timeline indicates evolution of capabilities across several years.

- **Strategic systems:** TI maintains many systems supporting its internal PWB and semiconductor (SC) capabilities. These systems are both in-house developed and vendor purchased. Using these existing resources reduces overall costs and shortens implementation cycle time. Examples of such systems are TI's military qualified financial systems and semiconductor verification system.

- **VHDL pass through:** The DA system will accept VHDL descriptions of a die-level parts list/node list and input the information into the DA database. Other VHDL descriptions will be preserved and passed through the DA system.

- **Product data management:** Provides the necessary capability to manage large amounts and maintain proper relationships among the data items for the engineering and manufacturing data generated by the MCM design and manufacturing process. The system is designed to be extensible as new requirements are identified and capabilities added.

- **Framework:** Commercially available frameworks play a key role in the integration and fanout of the MCM system. Migration to a framework environment will occur after initial system transfer and validation.

- **Computer-aided Engineering (CAE)/Layout coupling:** Before CAE tools are truly integrated into the routing process, a method for feeding forward CAE results into layout, and feeding back layout results into CAE for analysis is necessary. Task Technologies, a GE-HDI CAD vendor, made their "D-File" output bidirectional. This feature implements a path to and from layout.

- **Test data collection:** Collects foundry data for analysis of test failure trends. It is an on-line system allowing access to current tester data.

- **Standards support:** The DA system must support emerging PDES, EDIF, IGES, VHDL... standards to accept data from a broad customer base at the system's major entry levels.

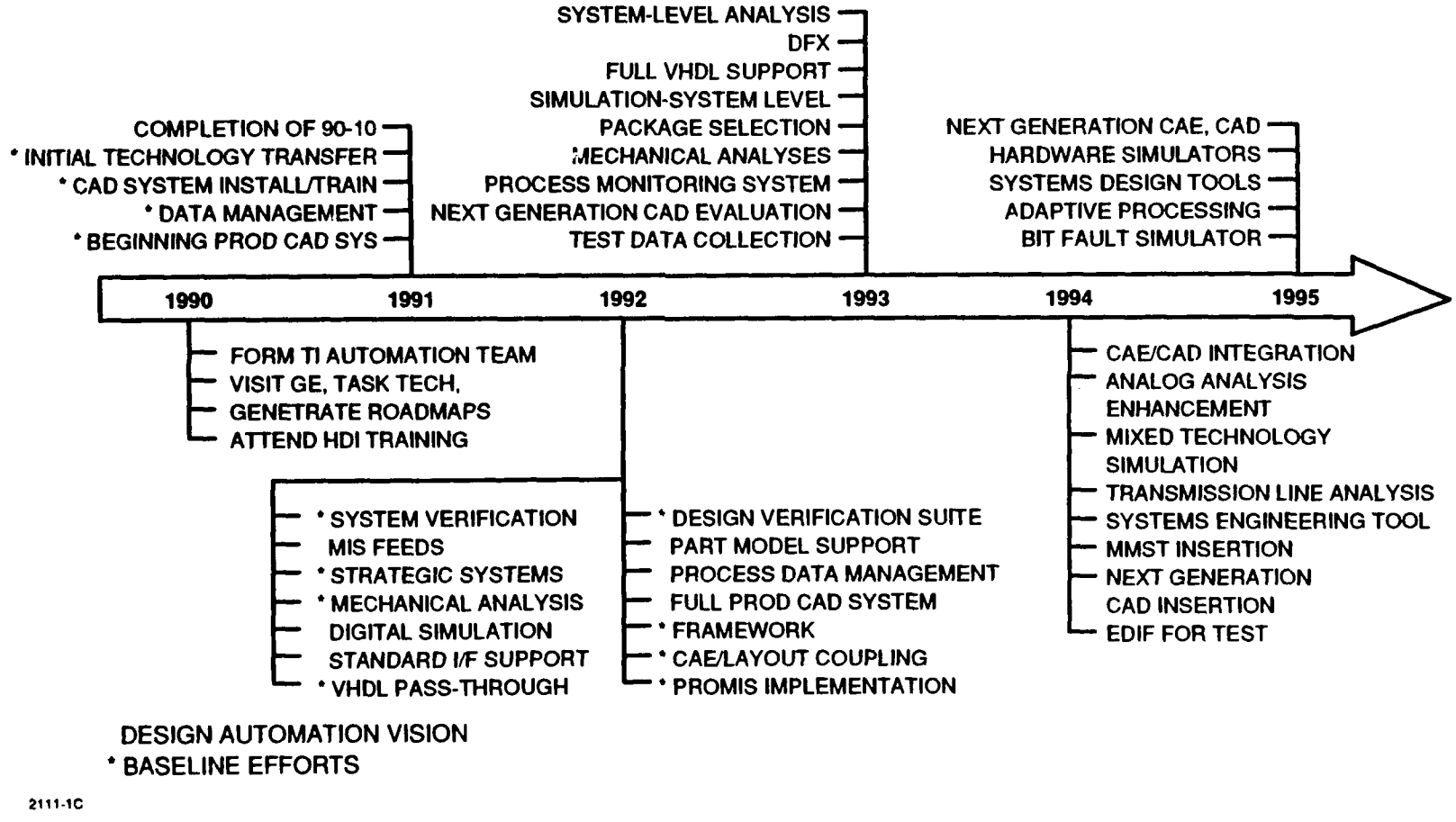


Figure 4-5. MCM Roadmap

- **PROMIS™:** Will initially serve as the factory information and planning system. This system will additionally provide the primary link between the factory floor and strategic business systems for the enterprise.

- **Microelectronic Manufacturing Science and Technology (MMST):** Will provide a next generation capability for factory control. Developed originally for semiconductor wafer fabrication processing and extended for the multichip technology, this system will fully integrate all aspects of the factory floor, including process data collection, equipment interface, and work-in-process management.

- **EDIF for test:** This industry standard will be defined, approved, and available for incorporation into tools. It will accommodate transfer of test programs between platforms without translation.

- **Built-In-Test (BIT) fault simulator:** Will comprehend BIT and allow fault grading providing fault isolation to the die level.

4.2.1.2.3 Time Phasing of Capabilities. Capabilities necessary for support of the initial technology transfer from GE to TI are scheduled for the first two years. Generally, the DA system's capabilities are extended backwards from physical design to the conceptual stage. This approach is reflected in the roadmap's time phasing.

4.2.1.3 Computing Architecture. A phased plan for implementing a computing architecture necessary to support concurrent engineering was developed. Summarizing,

- Initially use existing computer equipment, software, and support resources. Purchase only what is necessary to support the technology transfer (e.g., SUN computers, Omnicards CAD software).
- Purchase new technology and assign and train support personnel after successful low volume implementation on existing computers (e.g., data management and framework software, data communications hardware).
- Ramp to high volume with trained people on tested computer configuration (e.g., database server, additional data storage media).

4.2.1.4 Concurrent Engineering Implementation. TI and GE have groups supporting the different aspects of concurrent engineering. The project's success depends on the continuing support of these concepts within each company. Within TI, meetings were held with a number of these groups and roadmaps were revised to include supporting MCM. Discussions of these meetings and the resulting plans follow.

4.2.1.4.1 Design Methodology. The development of a design methodology addressing MCM unique issues affecting the methods for high-volume and low cost is required. TI implemented such methodologies in the electrical and mechanical areas and applied the results on actual projects. The MCM project will use these implementations and GE's existing "Design Guide" as a starting point for the implementation of a methodology. The methodology must support the DA Vision and provide support for the various system interface points.

4.2.1.4.2 Testability, Producibility, Reliability, and Manufacturability ("-ilities"). TI is a member of the University of Maryland's Computer Aided Life Cycle Engineering Center (CALCE) which sponsors the development of Reliability and Maintainability (R&M) tools. TI personnel developed a workstation environment integrating CALCE tools, commercially available tools, and TI in-house tools. The R&M workstation is named Computer Aided Reliability and Maintainability Applications (CARMA). An overview of this system and some of its tools is shown in Figures 4-6 A and B.

The MCM project will utilize systems in place and will work with the CARMA team to enhance the system to support MCM applications. A working session was held, and the MCM roadmap shown in Figure 4-7 was generated. Items on this roadmap specifically added for MCM are the port to a SUN/UNIX™ environment and to the MENTOR Falcon environment. Also, key to the effort is working with the University of Maryland to define a MCM ruleset for the CALCI tools. Note that tools supporting the testability analysis are already included in the 1991 CARMA effort. Issues relating to the fanout of these tools to non-CALCE members are yet to be resolved.

TI also developed and supports a manufacturability workstation. This system, marketed commercially, was designed for PWB applications and will be available to MCM customers.

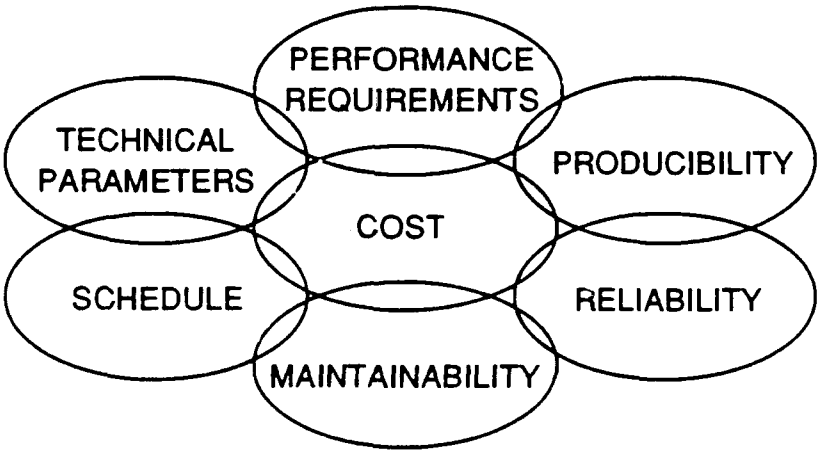
4.2.1.4.3 Design Rule Verification. A near-term system enhancement is the replacement of the vendor analysis tool, "DRACULA", with TI's "VER" design rule verification tool. This tool is encapsulated under Mentor's Falcon framework and will be commercially available. Also, the potential for customization of this tool to meet the foundry's specific needs is a possibility. Figure 4-8 outlines a roadmap for this strategy. In 1991, TI's tools will be evaluated against the current MCM rule set to determine if VER's capabilities meet MCM requirements.

4.2.1.4.4 Simulation - Digital, Analog, Mechanical. Figure 4-9 is a roadmap showing TI's DSEG design analysis strategy including simulation. Analog and VHDL driven digital simulation will be available in 1991, while mixed-mode and mixed-level simulation and integration of electrical and mechanical simulation will be available in 1994. In the interim, the University of Arizona's analysis tools are made available, and support of the standard analog language AHDL occurs. The Mentor Graphics system is key to this strategy's near-term implementation.

R & M AUTOMATION APPROACH:

- IMPLEMENT CONCURRENT ENGINEERING CONCEPTS/ENVIRONMENT
- EMPHASIZE COMPLIANCE WITH TOTAL REQUIREMENTS, ASSURING CUSTOMER SATISFACTION
- UTILIZE AVAILABLE CAE FUNCTIONALITY, FOCUS ON DATA INTERFACES AND COMMON DATABASE
- PROACTIVE UP-FRONT DESIGN IMPACT APPROACH THROUGH TIMELY ACCESS TO DESIGN DATA
- PROVIDE MAXIMUM UTILIZATION OF ELECTRONIC DATA SHARING
- AUTOMATE KEY LABOR INTENSIVE R&M TASKS
- ENSURE ADEQUATE TIME TO ITERATE DESIGN FROM A MULTI-DISCIPLINARY PERSPECTIVE
- PROVIDE DESIGN SYNTHESIS, ANALYSIS, SIMULATION CAE CAPABILITIES
- PROVIDE A BROADER SCOPE OF CAE FUNCTIONALITY TO YIELD A MORE ROBUST DESIGN
- PLAN TO UTILIZE SERVER BASED ANALYSIS/SIMULATION CAPABILITIES WITH NETWORK ACCESS TO PROJECT DATA MANAGEMENT SYSTEM

CONCURRENT ENGINEERING PRINCIPLES



TRADE-OFFS NAME OF THE GAME

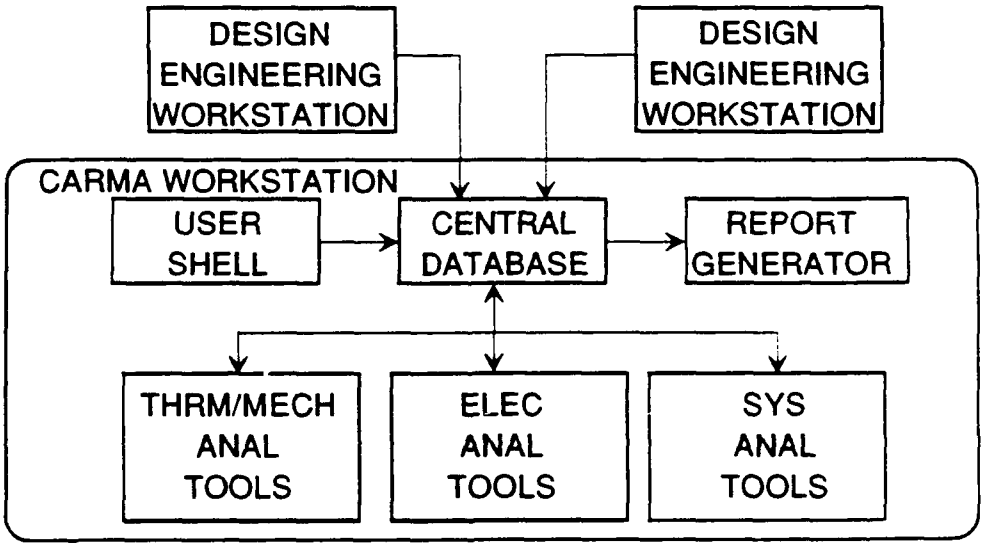
2111-3A

Figure 4-6A. CARMA Approach

CARMA OVERVIEW:

- BUILDS ON FOUNDATION OF DESIGN TEAM METHODOLOGY AND TRAINING
- PROVIDES AUTOMATED DESIGN-TO R&M DATA RETRIEVAL AND FILTERING
- UTILIZES CONCEPT OF "ENTER DATA ONCE, USE MANY TIMES."
- SHARES DESIGN DATA AND VALUE ADDED ANALYSIS RESULTS ELECTRONICALLY BETWEEN CAE TOOLS
- PROVIDES A USER FRIENDLY INTERFACE AND MENU DRIVEN TASK STRUCTURE
- FACILITATES SYSTEM LEVEL R&M ANALYSES: PREDICTIONS, ALLOCATIONS, MODELING, FMECA, ETC.
- PROVIDES MULTI-DICIPLINARY PWB ANALYSIS CAPABILITIES: ELECTRICAL, THERMAL, AND MECHANICAL ANALYSES
- FEEDS PERTINENT R&M DATA ELECTRONICALLY TO LOGISTICS

RELIABILITY & MAINTAINABILITY WORKSTATION



THRM RELBL	WORST CASE	MODELING
VIB/SHOCK	TOLERANCE	ALLOCATION
SLDR FATIGUE	STRESS DERATING	PREDICTION
	TESTABILITY	PLANNING
	POWER	FMECA

2111-38

Figure 4-6B. CARMA Overview

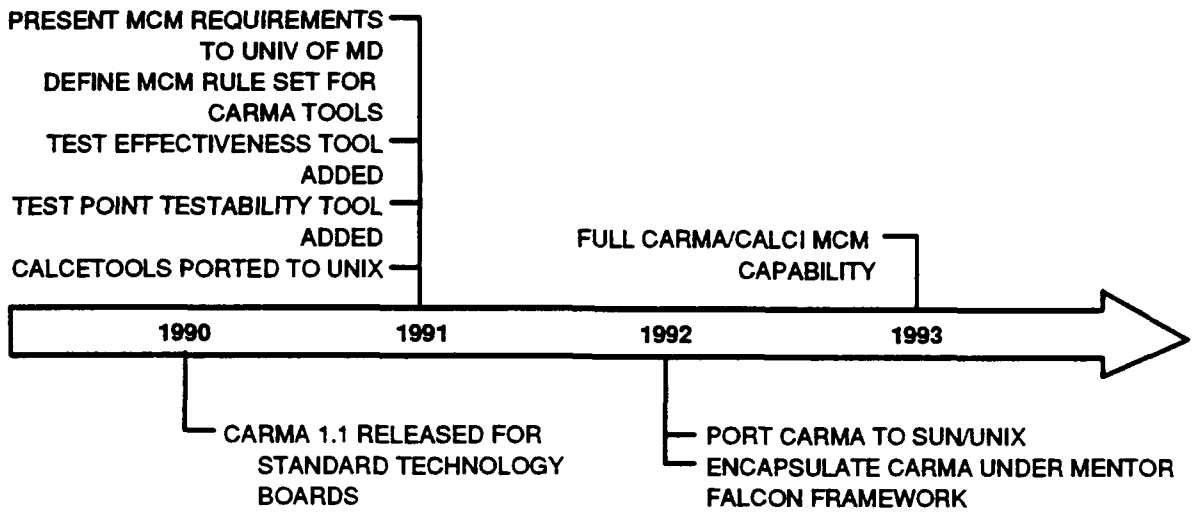


Figure 4-7. MCM "-Ility" Roadmap

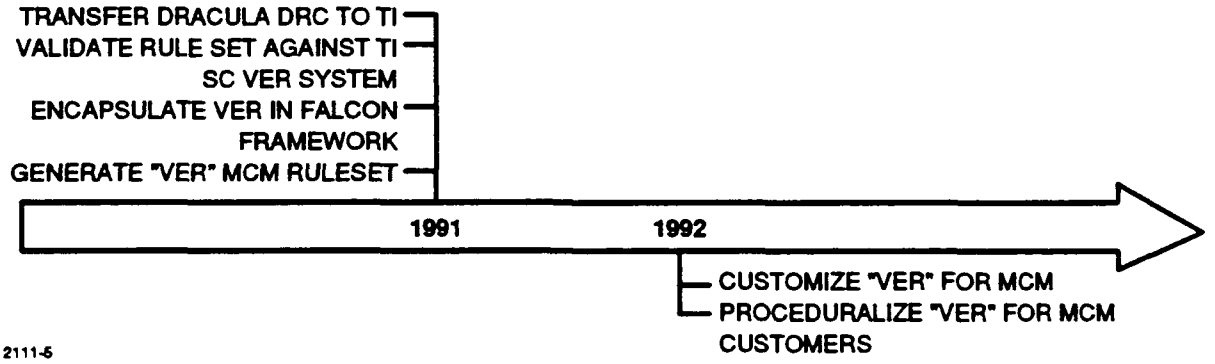


Figure 4-8. MCM Design Rule Verification Roadmap

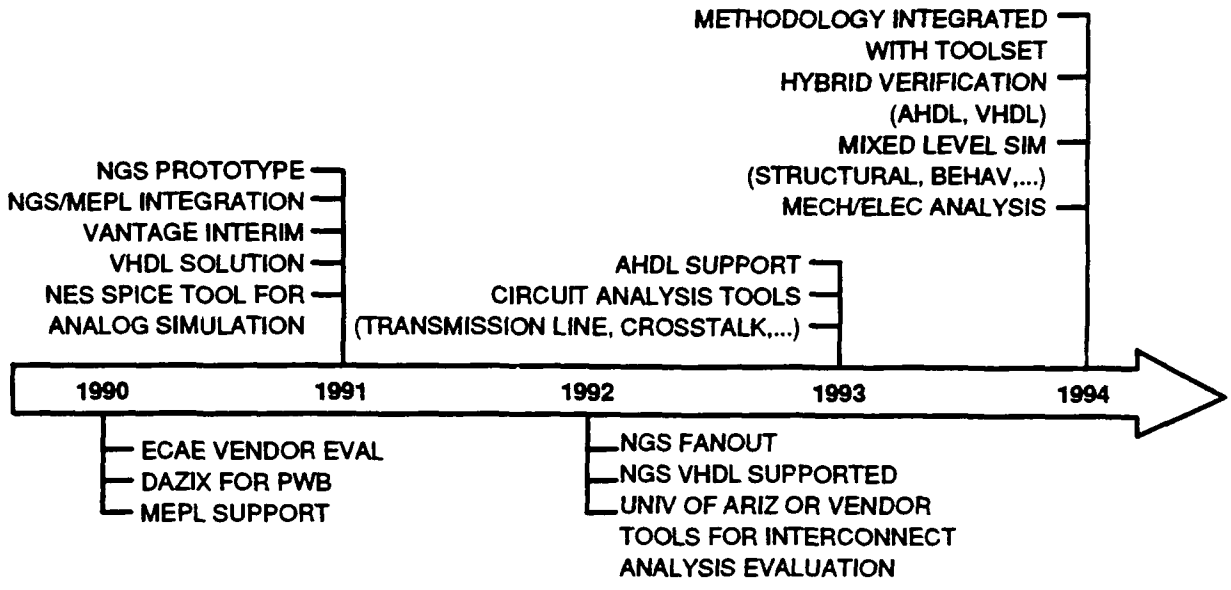


Figure 4-9. Design Analysis

4.2.1.4.5 Frameworks. CAD frameworks provide data and tool management to the design engineer. They keep track of data configurations and relationships and the current state of the design. Frameworks also present a consistent user interface to the design environment.

Using a framework, tools from different vendors are incorporated into the same design environment so all data can be managed as it is created, ensuring data consistency and eliminating many errors created by use of the wrong data file. Since the MCM module process depends on computer generated data, data consistency is imperative. Therefore, all tools in the MCM design process should be encapsulated into a framework. Figure 4-10 illustrates how a framework is used to couple MCM tools.

There are two philosophies for incorporating tools into a framework. The first, sometimes called "encapsulation", provides loose integration between the tool and the facilities of the framework. A software program called an "agent" is developed to make calls to the framework on behalf of the tool. The tool itself remains completely independent of the framework. The benefits of this approach are that the tool remains framework vendor independent, and requires less time to incorporate the tool into the framework because the tool's code is not modified. The costs are that the "agent" has only limited visibility into the activity performed by the tool, and the tool will not cooperate with other tools in the design environment any better than it did independently.

The second philosophy can be called "integration". Integration involves modifying the tool code to make direct calls to framework services. The benefits of this approach are better control of the tool's data, and tighter integration of the tool with the framework and other tools in the design environment. The costs are that source code changes, possibly a complete redesign of the tool, are required, and the tool becomes framework vendor dependent.

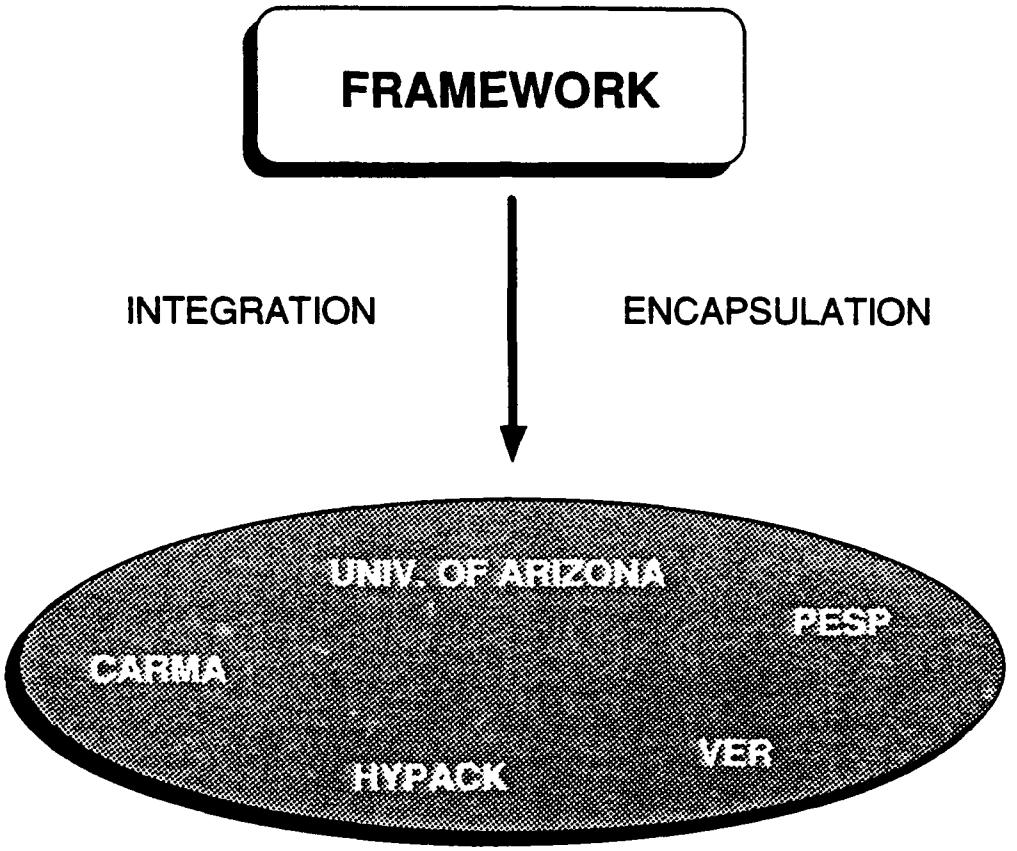


Figure 4-10. Framework to Couple MCM Tools

Incorporation of MCM tools into a commercially available framework, whether by encapsulation or integration, is a key element to fanout of the MCM automation system across a broad customer base. For the MCM project, TI and GE chose to use the Mentor Graphics, Inc., CAD environment, which includes the Falcon framework.

The framework roadmap is shown in Figure 4-11. Initially, the MCM design tools will be encapsulated into Mentor's Falcon framework, providing loose integration with minimum time investment. The timing for encapsulation will be market driven. The next step will be to determine the status of the CAD framework integration standards being developed by the CAD Framework Initiative (CFI). If CFI's standards are successful, the CAD framework vendors (including Mentor) should provide support for these interfaces, allowing tools to be more tightly integrated into the design environment while maintaining portability between frameworks. If the CFI standards are not successful, a decision must be made on the priority of framework portability versus the benefits of an integrated environment, and the Mentor Falcon interfaces may be selected for integrating the design tools more tightly into the design environment.

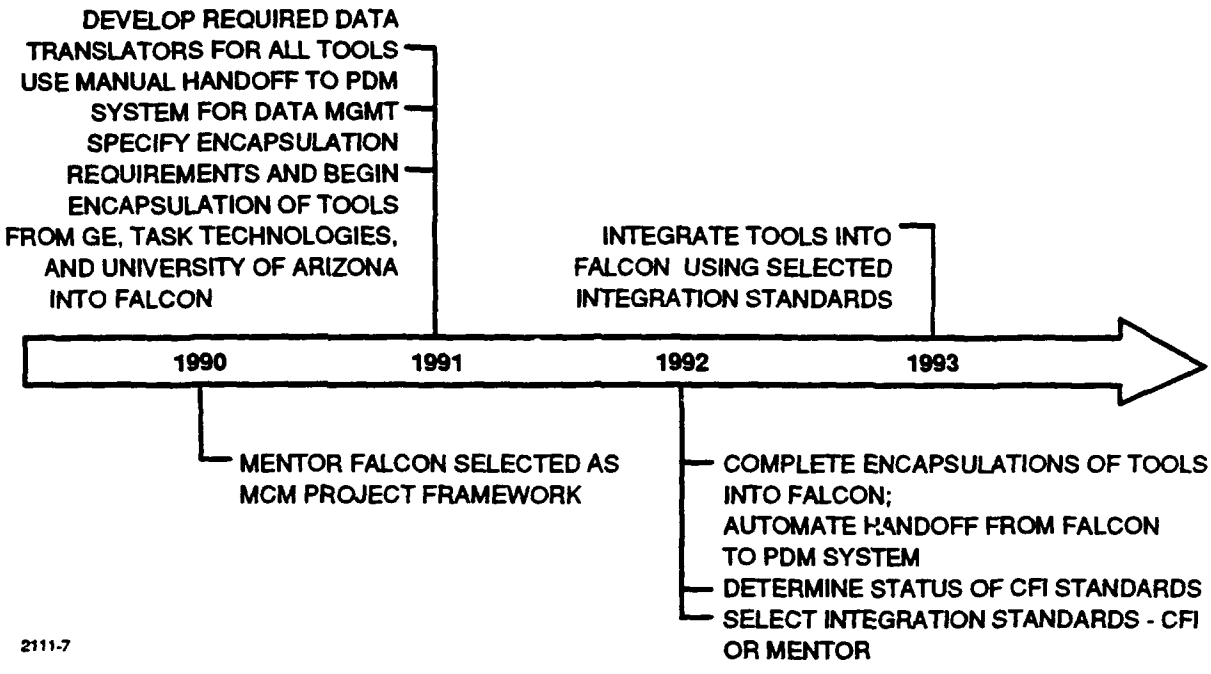


Figure 4-11. MCM Framework Roadmap

4.2.1.5 Related Technical Challenges. GE's HDI technology has characteristics setting it apart from the SOS, or "chips last," approach to MCM implementation. The following aspects have special implications resulting in technical challenges while implementing the CAD system:

- Embedded dice
- Data driven manufacture.

4.2.1.5.1 Data Management. Dice embedded in wells in the substrate lead to placements that are not orthogonal to the substrate's axes. This is compensated during manufacturing by GE's Adaptive Lithography process on a part-by-part basis. As a result, each MCM has unique in-process manufacturing data even though the parts perform identical functions (i.e., have the same part number). As a result, the volume of data that must be managed exceeds that of a "chips last" approach which uses masks during the manufacturing process.

Figure 4-12 illustrates this property. At the top is a representation of the traditional CAD process. One set of manufacturing data is archived per part. In the middle is a portrayal of the adaptive lithography process compensating for a chip's orientation, and a picture of a bare die, noting that in the GE process the thickness (z) is as important as the length and width (x and y). At the bottom is an illustration of the resulting data management issue.

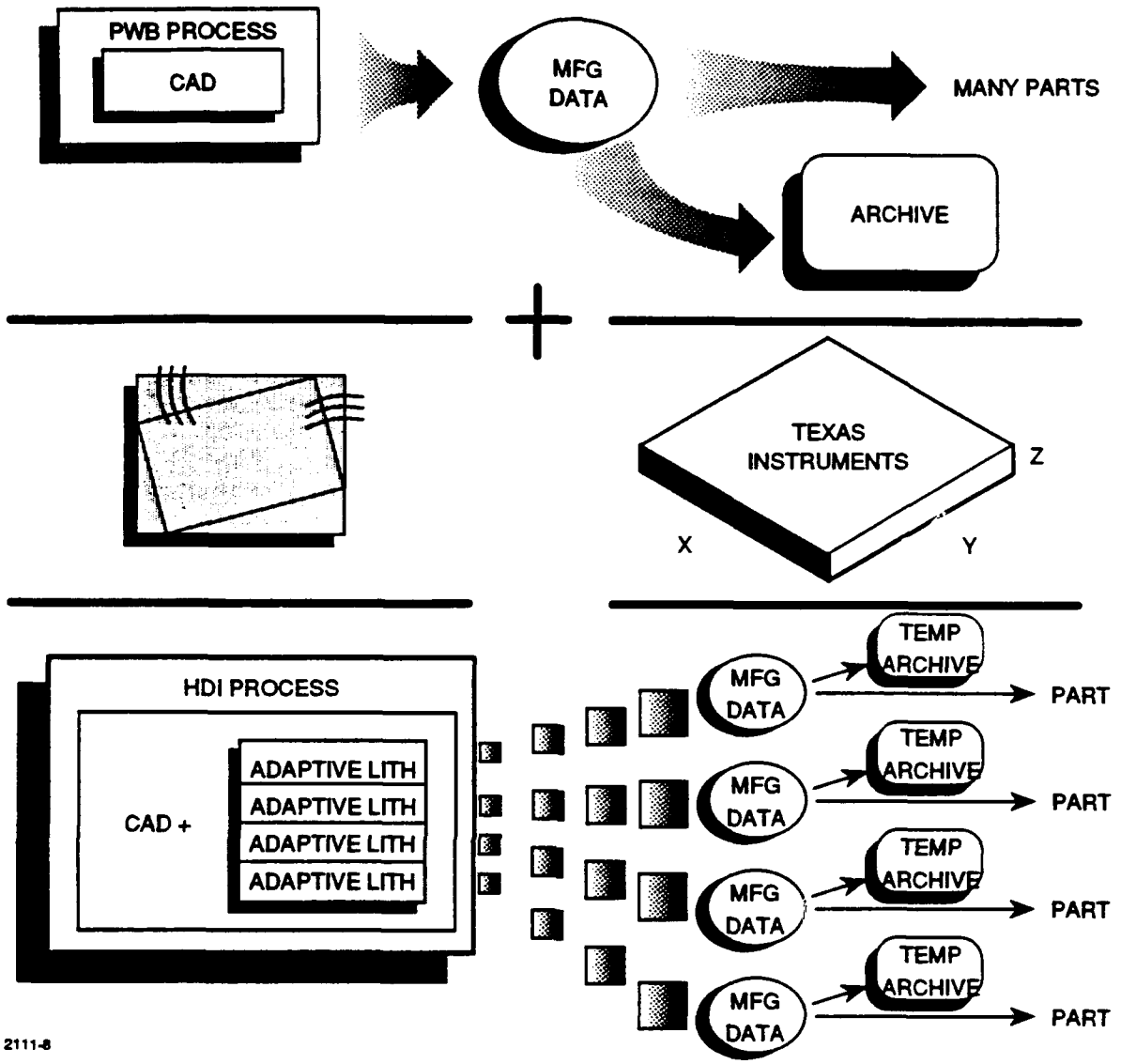


Figure 4-12. MCM Data Volumes

The amount of in-process data is directly related to the volume of MCMs produced. As a result, data management capabilities must evolve and become more robust as volumes increase. The required capabilities must fit into an overall strategy to avoid wasted effort and to yield continuing improvements. Figure 4-13 depicts a model of a data management strategy which will meet MCM requirements.

At the center of Figure 4-13 is a framework which facilitates tool integration, availability, and swapout. Frameworks have flow process control capability allowing for management of parts passing through the design and manufacturing process. Also, widespread availability of HDI tools is made possible by encapsulation under a commercially available framework. Frameworks were discussed in more detail earlier in paragraph 4.2.1.4.5.

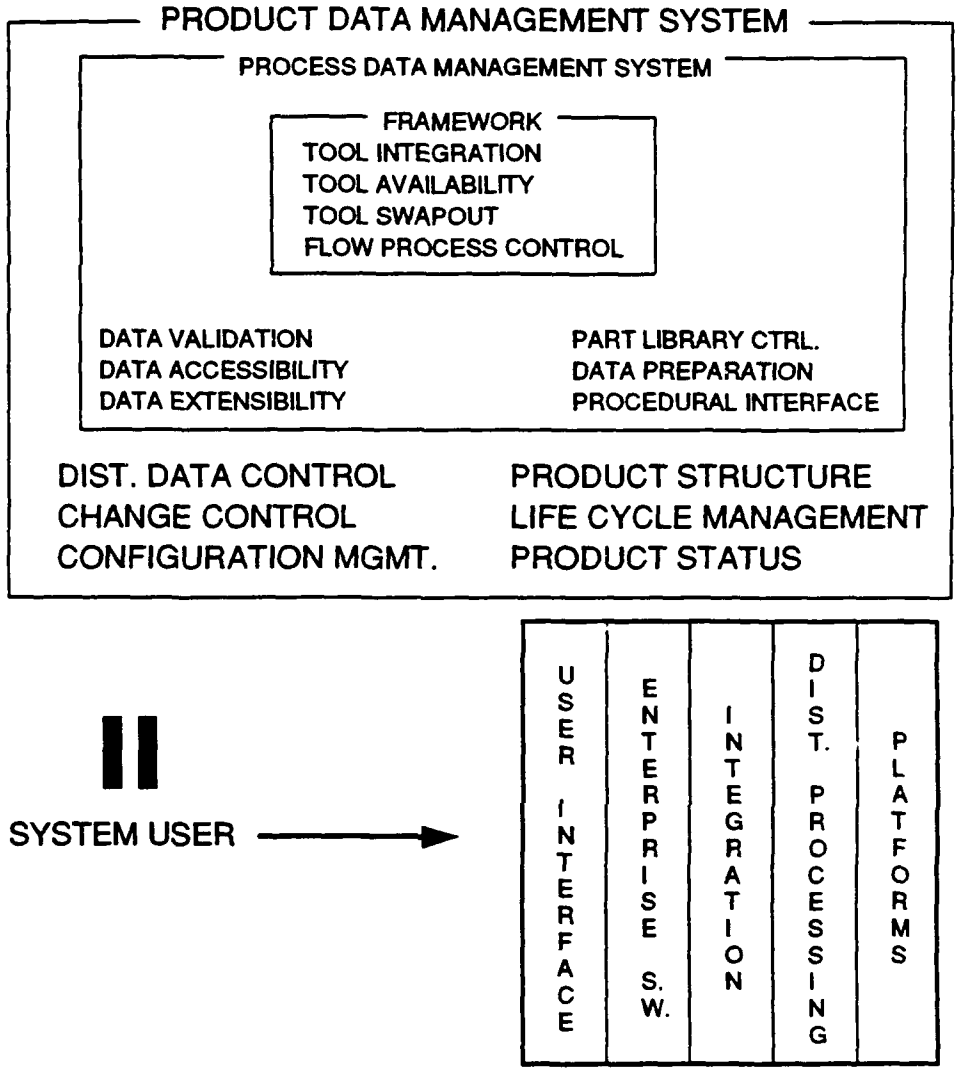


Figure 4-13. Data Management Approach

The next level is used to implement data management within the foundry. *Capabilities* supported by this level include:

- Data validation
- Data accessibility
- Data extensibility
- Part library control
- Data preparation
- Procedural interfaces.

TI is evaluating internal and external tools with potential for fulfilling these requirements. The TI/GE team will leverage these efforts to good advantage.

Finally, the outer shell provides high-level data management capabilities such as configuration management of released data, CALS compliance during customer interface, and the control of distributed data. Also included is product life cycle and product structure management.

The lower part of this figure shows how this approach insulates the user from the details of data management and allows the user to deal with MCM design and manufacturing problems more effectively.

4.2.1.5.3 Part Model Library(ies). The MCM process places unique requirements on part model libraries supporting design, layout, and manufacture.

Libraries supporting electrical analysis tools must include hierarchical descriptions of parts for simulation to be practical. Also, parameters associated with high-speed logic must be present to run analysis tools. Figure 4-14 shows an electrical part model library strategy that supports MCM. The near-term strategy is to use existing part libraries supporting individual analysis tools and perform partial simulations in critical areas. This approach is practical since most near-term work will be a remake of working designs. In the midterm, the project will use commercially available part libraries, such as that offered by Logic Automation. Another possibility is the use of TI's ASIC library approach which is already in place; customization is a possibility. The long-term approach which is comprehends the need for mixing technologies on the same substrate: digital and analog. System-level part descriptions with VHDL input is decomposed into part formats compatible with analysis tools and then synthesized into a VHDL description of the part. The results of this approach are input to simulations at still higher levels. Research is underway in several aspects of this tactic at the university level.

Libraries supporting mechanical analysis tools must support software interfacing with electrical analysis and layout tools (because of analysis requirements placed on the system when producing high-speed MCMs). In TI's high-density power supply area, ties between electrical and mechanical systems are in place and the project will benefit as a result.

Libraries supporting layout must include thickness parameters for each die and must comprehend the mapping between the die pads and package pins. The latter is true because, to date, most schematics are done at the board level. In summary, layout libraries are mixtures of board and integrated circuit (IC) requirements. GE's MCM system provides for these requirements. The project will use existing software.

Libraries supporting manufacturing must be tied to the design and layout libraries to support the Adaptive Lithography, assembly, and test processes, and to eliminate redundant data that needs to be synchronized with other libraries. Circuit traces, node names, test locations, and package types are examples of such data.

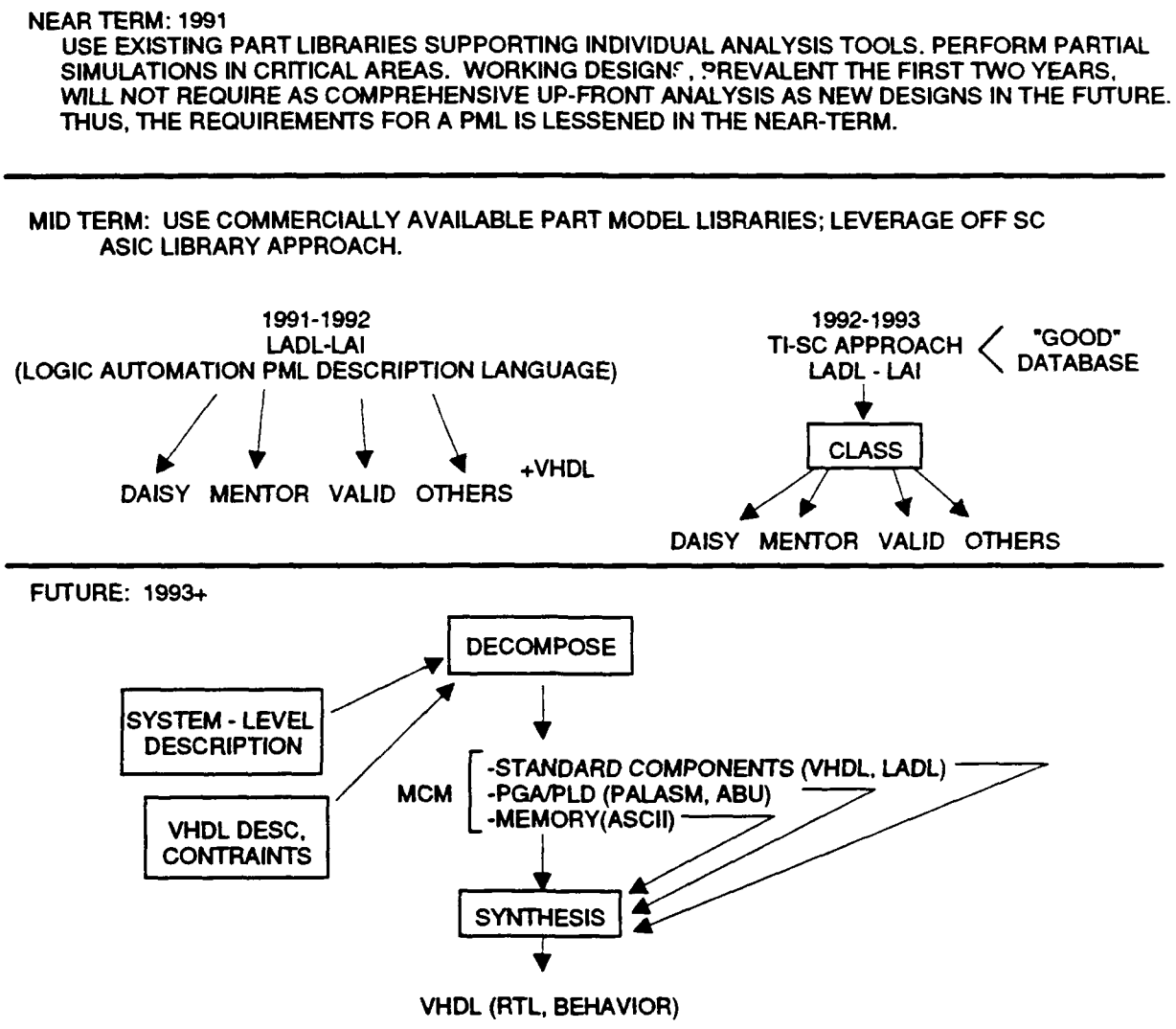


Figure 4-14. MCM Electrical Part Model Library Strategy

4.2.1.5.4 **PWB versus MCM Requirements**. MCM part descriptions are a mixture of board and integrated circuit data. Bare die parameters as well as package descriptions are necessary to drive the MCM system. Arrangements with IC manufacturers will make die thickness data and pad-to-pin mappings, known during the IC manufacturing process, available to the MCM foundry. When this approach is impossible, die measurements made on incoming inspection must be captured and made available to all downstream processes. Data gathered at the foundry concerning pad-to-pin mappings also must be collected and made available.

4.2.1.5.5 **Required Support**. Recognition and funding of the support requirements associated with these challenges is critical to the success of the foundry. This is especially

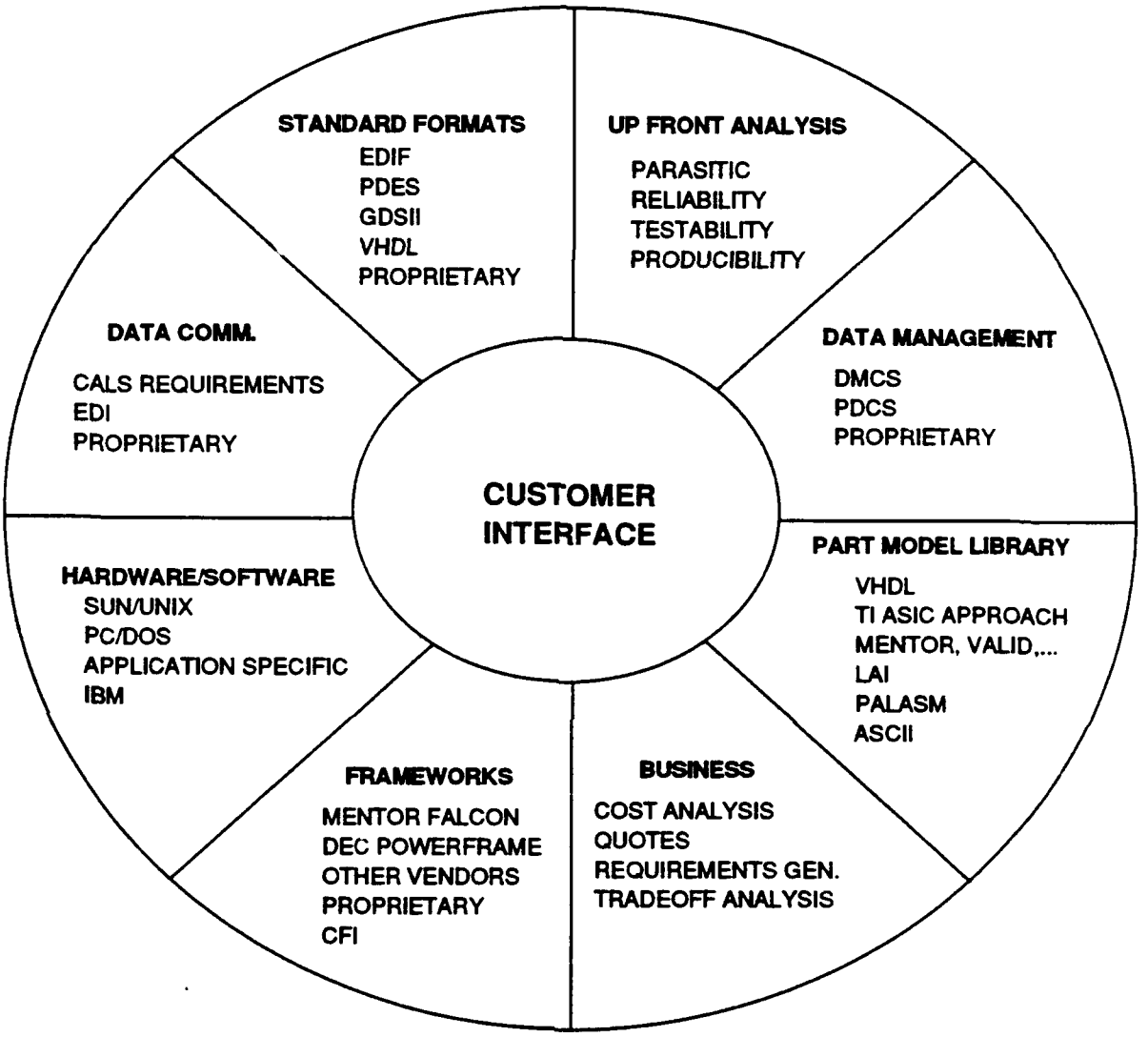
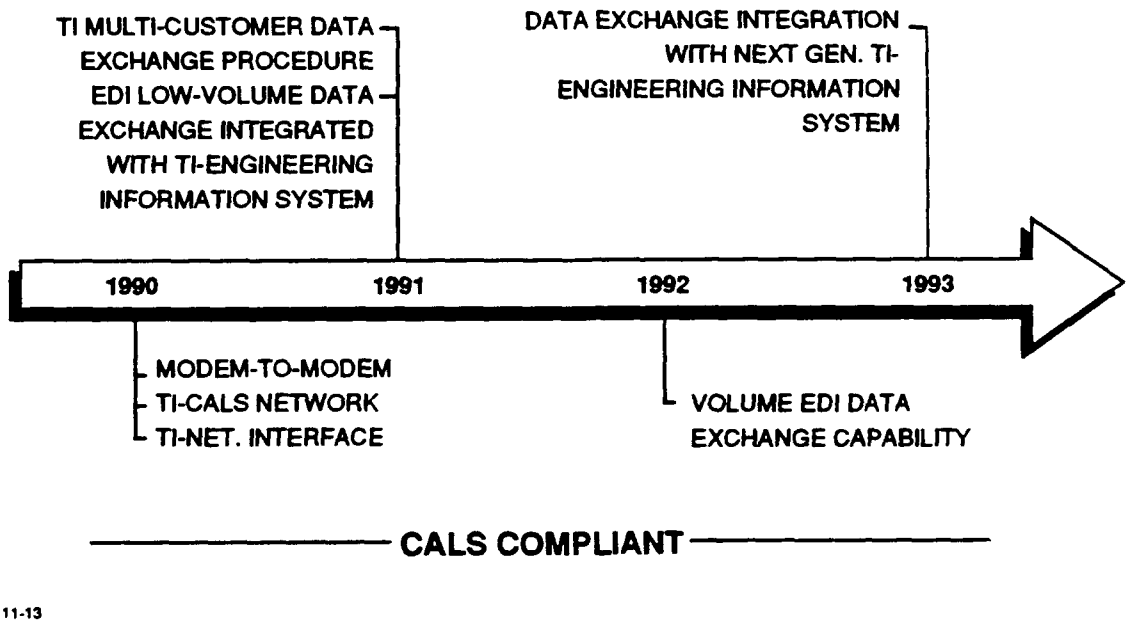


Figure 4-15. Customer Interface Perspectives

	RAPID PROTOTYPE	HIGH VOLUME
MILITARY	DESIGN/MANUFACTURE INTEGRATION HDI TOOLS UNDER COMMON FRAMEWORK UP-FRONT ANALYSIS AT CUSTOMER'S SITE CALS COMPLIANCE DATA MANAGEMENT PART MODEL SUPPORT, MECHANICAL, AND ELECTRICAL	DESIGN/MANUFACTURE INTEGRATION VHDL-BASED CIRCUIT DESCRIPTION SYSTEM ENGINEERING TOOL AVAILABILITY CALS COMPLIANCE DATA MANAGEMENT
COM-MERCIAL	DESIGN/MANUFACTURE INTEGRATION HDI TOOLS UNDER COMMON FRAMEWORK EDI COMMUNICATION EDIF CIRCUIT DESRIPTION DATA MANAGEMENT PART MODEL SUPPORT, MECHANICAL, AND ELECTRICAL	DESIGN/MANUFACTURE INTEGRATION MULTI-LEVEL CUSTOMER INPUT/OUTPUT & SUPPORTING TOOLS PART MODELS COMMERCIALLY AVAILABLE DATA MANAGEMENT

2111-12

Figure 4-16. MCM Capability Matrix



2111-13

Figure 4-17. MCM Customer Communications Roadmap

4.2.1.6.4 Test Interface. Testable foundry input is required. The customer and foundry must have a close working relationship in the area of design for testability to increase the probability of first pass success. Incoming products will be reviewed for testability by the foundry's engineering staff who will work with the customer to improve testability and provide test coverage and times in the cost response. The final test vectors must come from the customer.

4.2.1.6.5 Test Vector Transfer. Few interfaces are available directly from the customer's simulation to a given foundry test system. EDIF will be of great benefit if the plans to include test vector and test sequence data are incorporated. The current plan of interface will be via the translator. Third party software companies generate quality translators from simulators to a common data base format. Translation into other formats is then available from the common database. Translators need to be expanded for the new test systems that will be used in the MCM foundry until EDIF is available. Work is underway to address the fault diagnostics required by IC type test systems.

4.2.1.6.6 Existing CAD Systems. The Task Technologies system supports the following proprietary input interfaces:

- GE's proprietary parts list/node list
- Viewlogic
- Cadence
- Futurenet
- Teradyne/EDA
- SCI-Cards
- Orcad
- Omation Schema
- Ulticap

The "D-file", a generic input/output file for the Task system, offers a mechanism to develop further CAD interface capabilities. Task Technologies offers this service. An immediate requirement is support of the Mentor system input.

4.2.1.6.7 Requirements Validation (to and from foundry). Customer support procedures must ensure that the foundry's customer data interface is validated against the customer's requirements at both input and output levels. Two important capabilities exist and will be used to define interfaces at the layout level.

TI's DSEG surface mount factory supports a system used to validate the customer's parts list/node list input as a spread sheet and to track this pre-released data. The MCM system will employ this capability for input at this level. Also, Task Technologies furnished TI with an existing system for validation of Futurenet input data defined in a PC-based database system, an example to be used as a model for further extensions.

4.2.1.7 Support. Recognition and implementation of the support functions accompanying the system's installation is required for success. If the HDI Concurrent Engineering concept is improperly integrated into the foundry environment, costs will soar, and the DA system

itself, in spite of its positive aspects, will fail. The following discussion defines these functions.

CAD system management: One person must assume total responsibility for the success of the DA system by:

- Assuming management responsibilities (cost, schedule, reporting,..)
- Arranging for control of DA software changes
- Measuring and reporting system performance.

Software verification: Required to insure the quality of the software. Included in this task are:

- The generation of vendor comparisons
- Generation and execution of a configuration management plan
- Audit of production software
- Coordination of software updates.

Software integration: Ensures that all software meets the user's operational requirements. Included in this task are:

- Validation that all software fits the MCM foundry's operational environment
- Maintenance of hardware and software configuration lists
- Execution of acceptance tests.

Documentation: Ensures that documentation is in place to support HDI tools installed in the TI foundry as well as at customer's sites. Included in this task are:

- Arrangement for software specification reviews
- Generation of required documentation
- Maintenance of documentation standards
- Fanout of document upgrades.

System support: Provides for the overall support of the software after formal release. Included in this task are:

- Provision of user support
- Creation of software activity reports
- Maintenance of performance indices
- Generation of user requirement specifications
- Provision for user training.

4.2.2 Computer Aided Engineering, Computer Aided Design

The Computer Aided Engineering, Computer Aided Design section considers several aspects of implementation. Thework planned by consultants contributing to the study is discussed, and it also considers the status of GE's MCM system, called HYPACK.

4.2.2.1 HYPACK. GE's HYPACK system is the basis from which the overall MCM automation system will be implemented. A description of the existing system is shown in Figure 4-18.

4.2.2.1.1 Current Capabilities. HYPACK is a design environment which facilitates layout, routing, and electrical performance analysis of multichip modules. The environment integrates several commercially available tools with custom software developed specifically to support the GE HDI process.

Commercially available tools include the Omnicards layout system, the HYTRACK router, and Omniroute II router, all distributed by Task Technologies, Inc. Included are the transmission line parameter calculators and transmission line system simulators created by the University of Arizona, Department of Computer Science and Electrical Engineering under Semiconductor Research Corporation funding. Project flow is indicated in Figure 4-19. Electrical performance requirements, including noise margin and expected rise times, are provided along with physical design rules which are inputs to a noise analyzer module. Electrical performance is guaranteed by calculating maximum permissible line length based on a worst case analysis. Maximum line lengths are input to a custom developed autoplacement algorithm which satisfies the noise required lengths with the shortest overall interconnect length. A net list and parts description are also required as input for HYPLACE.

The approach to noise analysis involves deriving a matrix of inductance and capacitance parameters associated with a two-dimensional conductor array using the parameter calculator UAMOM from the University of Arizona. This tool can consider strip line or microstrip configurations with up to six layered dielectrics. Arbitrary conductor cross sections (piecewise linear) are possible. A matrix inversion is used to find the inductance matrix in the skin effect limit. From the transmission line parameters and transmission line analysis (including reflections, delays, crosstalk and attenuation) the line length is incremented until the sum of all noise contributions reaches the level set by the noise margin budget.

The router used in the HYPACK environment is a product of Task Technologies, Incorporated. The output is a NC Compfile used to program automatic insertion equipment, and a DFL file containing a complete record of all artwork. The NC Compfile:

- Is input into manufacturing translation programs generating software to drive machines to mill substrates and pick-and-place equipment.
- Provides for a CIF translation giving DRC capability using DRACULA.
- Is input into a custom software module called HYPWR which autogenerates power and ground mesh grids automatically attaching to chip pads and edge connector fingers.

The HDICON translator transforms the artwork data from the DFL file's neutral database to metal and drill artwork files which drive the GE laser lithography system.

4.2.2.1.2 Digital, Analog, Optical Integration. GE's HDI offers the capability to mix IC technologies allowing non-digital circuits to be incorporated into a single design.

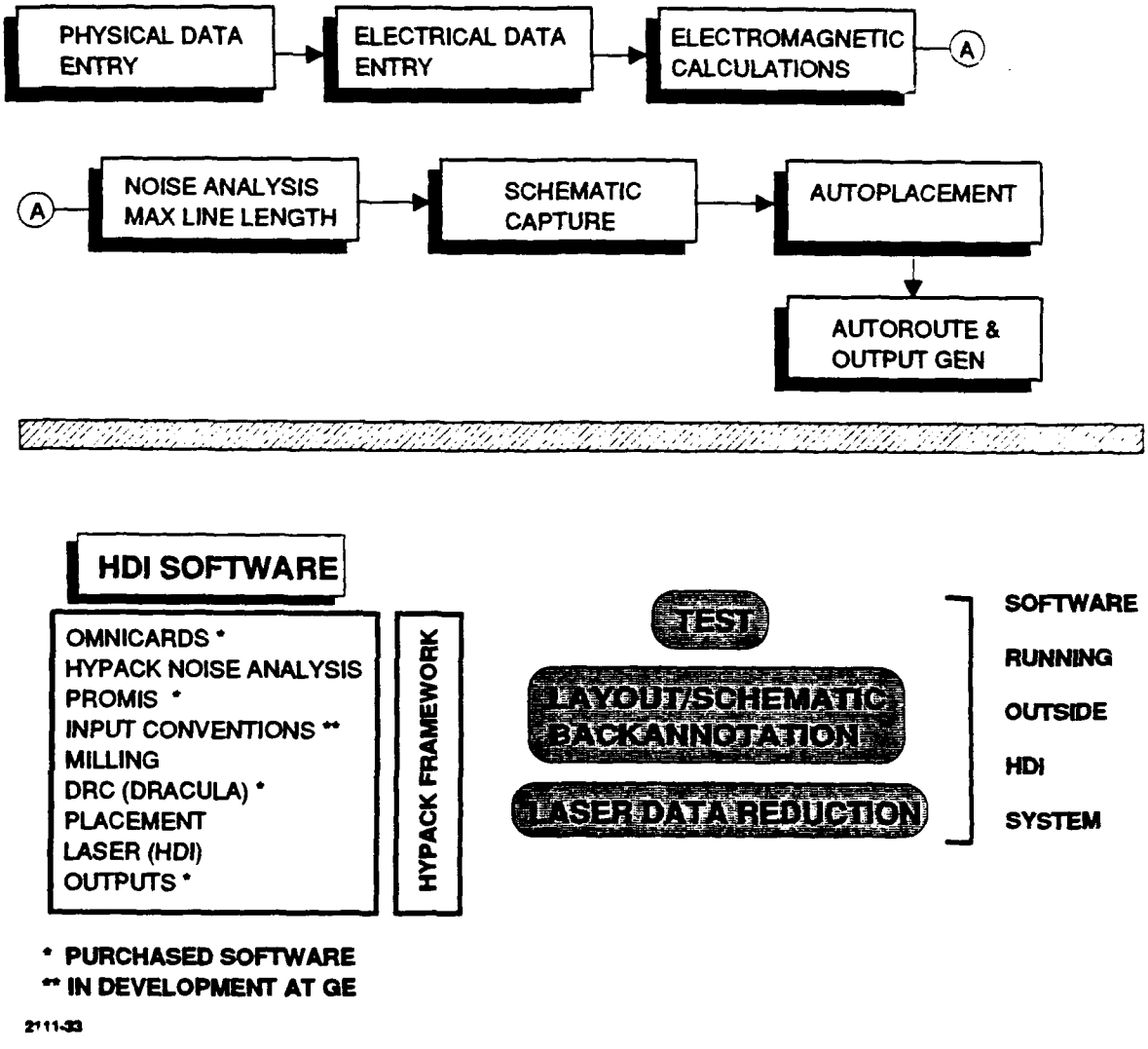


Figure 4-18. HDI Software System

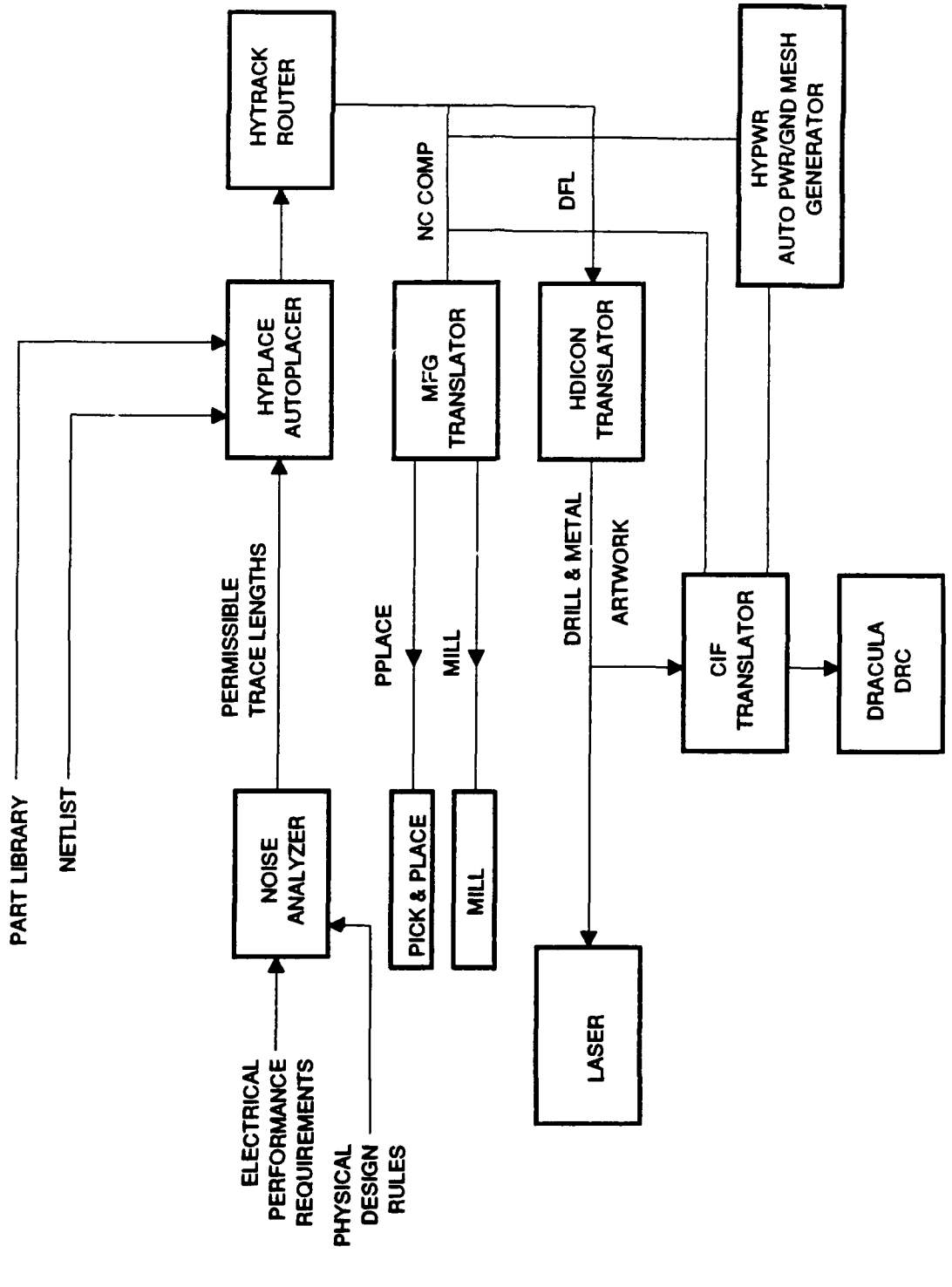


Figure 4-19. HYPACK Project Flow

The absence of wirebonds and the close physical tolerances of the overlay structure allow a close proximity of sensitive analog and noisy digital circuits so shielding can be maintained. In the microwave region, the ability of HDI to maintain controlled impedances to the IC pads results in a repeatable design.

Adaptive lithography and innovative materials allow light piping to optical cells within the design eliminating the alignment needs of other MCM technologies.

4.2.2.1.3 Production History. The HYPACK environment is the basis of virtually all the GE HDI modules; over 25 designs in prototype production.

4.2.2.1.4 Identified Enhancements. Although it serves well as a design environment for circuits with performance less than 100 MHz clock rate and for relatively low volume and prototype applications, HYPACK needs enhancements to provide for increased volume and performance capability.

For high performance the present 2-D parameter extractor is inadequate. 3-D capability for modeling discontinuities, such as vias, right angle bends, and crossovers, becomes important beyond 100 MHz clock rates. The required enhancements are:

- Improved transmission line simulators taking into account skin effect in resistance and inductance, nonlinear terminations, and losses within the line.
- Back annotation capability (as performance tolerances grow tighter).
- More sophisticated tools to analyze the impedance and data I-noise in power and ground structures.

Finally, because of the complexity of these tools, a means for determining the appropriate level of analysis is desirable. These identified enhancements to HYPACK were analyzed by the University of Arizona, and a time-phased development plan for an integrated system called Package Design/Simulation System (PDS) was developed. It will provide integration of electrical and thermal/mechanical simulation capabilities with testability, manufacturability, reliability, and cost analysis, and will provide interfaces to critical databases. These include CAD, mechanical and electrical CAE, CIM, Chip Model Library, and CAT databases. The major milestones include an integrated 250-MHz clock capability by 1994 (year 3) and an integrated 750-MHz capability by 1996 (year 5).

Enhancements are also needed to facilitate manufacturability for high-volume production. This would require design for manufacture specifying trace widths, separations, and other important physical parameters. Post processing of the artwork database, following layout and route, will be required to spread traces, reduce vias, and provide other manufacturing enhancements to improve yield. Also, database approaches will be required to minimize the storage space used for the data in a high-volume fabrication facility.

4.2.2.2 Consultant Overview. While developing the MCM automation plans, the TI/GE team relied on the expertise of several consultants whose input strongly influenced this report.

Two reviews were conducted during the execution of the 90-10 study program during which input from project consultants was gathered.

4.2.2.2.1 University of Arizona. The University of Arizona has performed research in the area of design and analysis since 1984. This is an area identified as needing improvement in the HYPACK MCM system. The following are among the tools that resulted and are crucial to designers of MCMs.

- University of Arizona Capacitance Calculator (UAC)
- Methods of Moments TEM Transmission Line Parameter Calculator (UAMOM)
- University of Arizona Simulator for Nonlinearly Terminated Transmission Line Network (UANTL).

GE and TI have served as "mentors" during the development of these capabilities, and a simple prototype system, developed at the university, is installed and in use in TI's semiconductor area.

Because of this tie, the University of Arizona was selected as a team member on the 90-10 contract. They proposed to study and develop a plan for implementing a high-confidence integrated packaging design simulation system which will enable rapid prototyping of complex MCMs. The system will provide insight into performance contributors so that detailed debugging and design optimization can be performed for high-volume products. The integrated system will include both electrical and thermal-mechanical capabilities, with the latter derived from commercially available tools. A summary of their 90-10 study effort result follows.

The University of Arizona plan will provide the required extensions to HYPACK to accommodate electrical and thermal/mechanical simulation/analysis of higher frequency digital and mixed digital/analog MCMs of the future. The extensions will also integrate concurrent engineering software tools (reliability, testability, etc.,) into the design system, and provide interfaces to design and manufacturing databases. Some critical database interfaces which must be comprehended in the system are:

1.	Mechanical CAE-to-Packaging Design System (PDS)	Mechanical/thermal design data base, preplace floorplanning
2.	Electrical CAE-to-PDS	Schematic data base
3.	Chip Model Library-to-PDS	Individual parts data
4.	CAD-to-PDS	Layout/routing (tight feedback loop)
5.	CIM-to-PDS	Manufacturability
6.	Test-to-PDS	Testability evaluation

These planned extensions include electrical analysis upgrades aimed at a 250-MHz clock rate capability in five years. Major development milestones are:

Year 2 - PDS 1.2 (100-MHz clock)

- 100-MHz, 2-D electrical modeling and simulation capability
- Integrated thermal/mechanical analysis capability
- Mechanical and electrical design database interfaces

Year 3 - PDS 2.0 (250-MHz clock)

- 250-MHz, 3-D electrical modeling and simulation capability
- Interfaces to a prototype Package Model Library (PML)
- Prototype interfaces to a Chip Model Library (CML)

Year 4 - PDS 2.2 (250-MHz clock)

- Final interfaces to CML and completed PML databases
- Intelligent analysis tool auto-selection by PDS
- Built-in expertness for simplifying simulation and analysis of results
- Prototype "ilities" tools selected and integrated

Year 5 - PDS 3.1 (750 MHz clock)

- Final "ilities" tools integrated
- Prototype tool auto-select and expertness for 750-MHz clock integrated.

Mechanical/thermal coupling to ANSYS and interfaces to chip and package libraries will permit thermal/mechanical simulation. Package Model Libraries will also store precalculated equivalent circuit models of common packaging structures (generated from 3-D electromagnetic analysis) for call-up as required.

To be useful, the system must be built for use by designers who, in many cases, have limited expertise in one or more areas; thus it must have expertness or intelligence built in. It must be able to provide modeling/simulation guidance for less-experienced designers, and must have the capability to simplify or approximate simulation of very complex designs so that results are available in time scales appropriate to the design process (minutes rather than days).

A package design support environment (PDSE) will provide a spread-sheet-like capability to do "what if" analysis of a variety of design options, expediting the design process. PDSE will be flexible enough to incorporate existing commercially available tools, when available, and will have provision to be encapsulated into a higher level framework. Integration of the system into the framework the engineer normally uses should facilitate its use.

4.2.2.2.2 Task Technologies, Inc. Task Technologies, Inc., vendor for the Omnicards layout system supporting GE's HDI process, worked closely with GE to customize their layout system to adhere to routing restrictions that make Adaptive Lithography possible during the manufacturing process. Task also integrated software developed at GE into their system making the link from and to the foundry function smoothly. Figure 4-20 shows the Omnicards software system that will be installed at TI as part of the initial technology transfer.

The Task system supports interfaces with GE's proprietary input and output formats as well as other vendor formats. These are indicated in Figure 4-21. Task plans biannual product updates and will support EDIF 2.2 in the fourth quarter of 1991.

In the future, the MCM foundry will support multiple MCM technologies - chips first and chips last. Having one CAD system that is capable of performing the layout of either technology and quickly transforming one technology into the other is of critical economic importance because of reduced support costs. As a result, TI asked Task to re-layout a circuit implemented at TI with SOS technology using the system designed for the HDI process. Adherence to all SOS design rules was a requirement. The circuit had two TMS320C30s, 75 stacked memories, 20 chip resistors, and 40 other IC dies; around 1500 point-to-point interconnects were required. Task responded within two weeks with an SOS circuit layout routing to 100% completion. Varying complexities and circuit speeds may require multiple routers in the future, but it is anticipated that the majority of designs may be done with the same CAD system.

Tony Mazzullo, president of Task Technologies, was asked to participate in the team reviews. He also critiqued this report for accuracy relative to the Task CAD system.

4.2.2.2.3 Other Consultants. Digital Equipment Inc. (DEC), worked with the SWAP team to define a hardware/software environment balancing autonomy and standardization. Their proposed strategy keeps functional capabilities, such as the Task software, on workstations best serving their purpose while providing links between these capabilities compatible with the data management strategy mentioned in the Concurrent Engineering section.

Layout Concepts, Inc., was contacted as a possible second source for the layout system. Their software forms the basis for the Task Technologies product. If Task Technologies is unable to support GE's MCM approach in the future, TI and GE could establish a development/support relationship with Layout Concepts or purchase source code for internal development.

Mentor Graphics, Inc., met with both TI and GE and discussed the MCM project. Mentor submitted a draft proposal to TI and GE discussing:

- Mentor's current MCM capabilities
- A suggested MCM Design System Roadmap based on the Mentor design environment, integrating additional tools as needed. Implementation of the roadmap will be market driven.

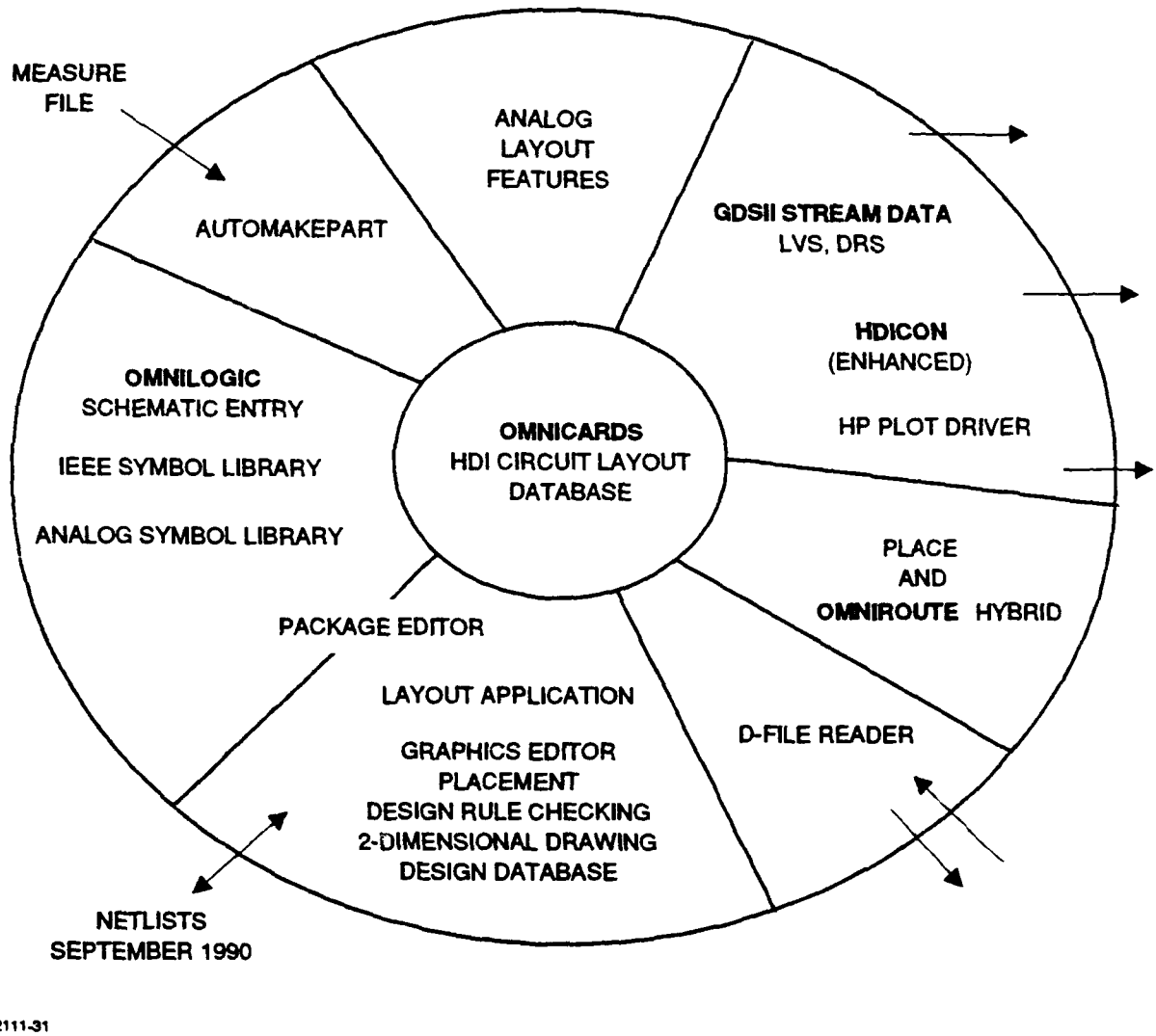


Figure 4-20. HDI DA at General Electric Company

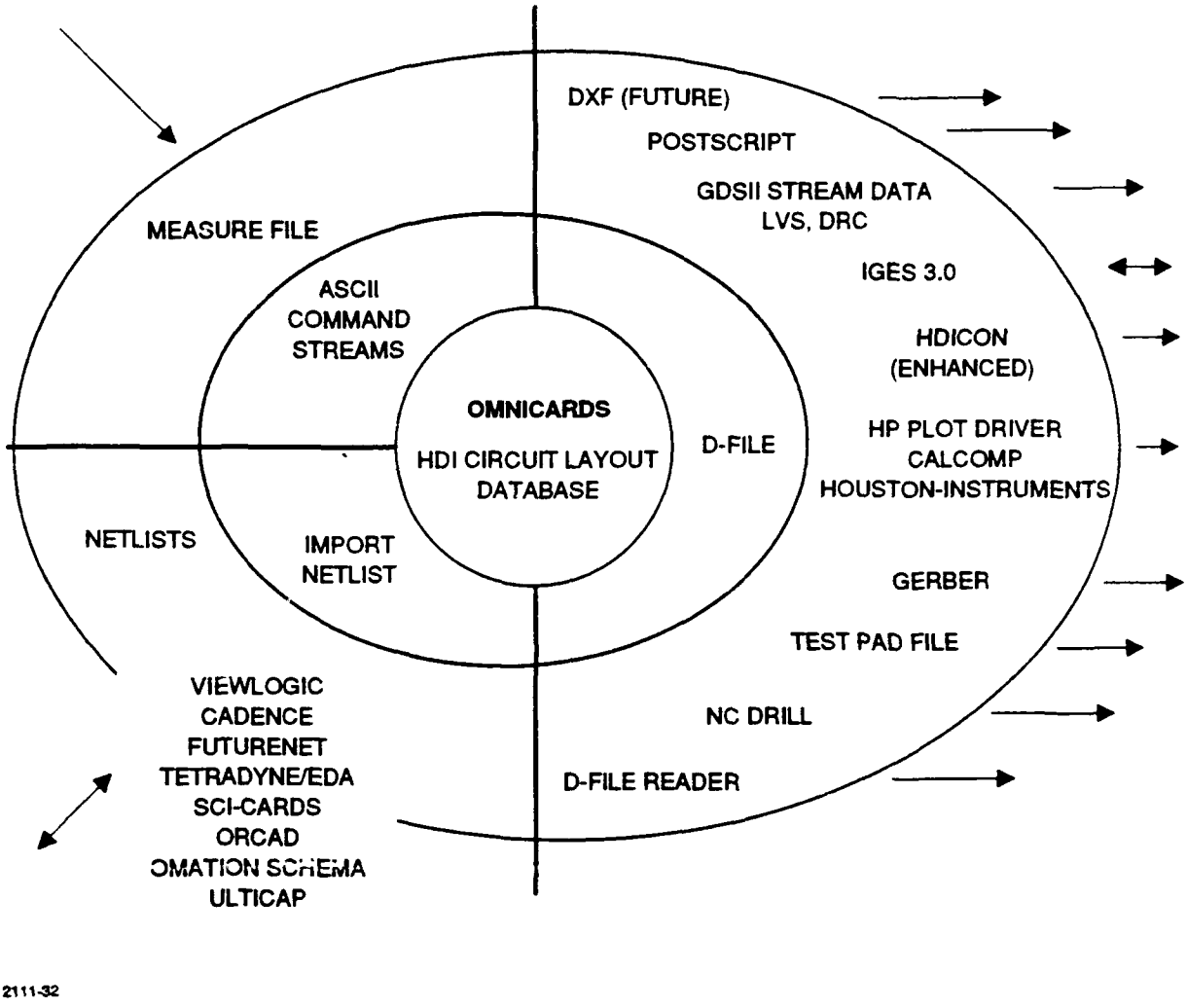


Figure 4-21. Integration and Data Interfaces for Omnicards

- The MCM design process entry points and Mentor's capabilities for addressing them.

4.2.2.3 Implementation Plan. A high-level implementation plan was generated and will be discussed in following sections.

4.2.2.3.1 DA Milestones. The baseline technology transfer is followed by a series of milestones supporting the DA vision.

The baseline system addresses:

- Initial technology transfer
- Items necessary for supporting production

- Items that lay groundwork for the enhancements necessary to support foundry requirements.

The Phase I automation system gives the customer the capability of entering the system at the detail design level. Phase II adds capabilities necessary for entry at the system level. Phase III adds enhancements necessary for supporting high-frequency designs.

4.2.2.3.2 Foundry Hardware Configuration. Figure 4-22 is the recommended configuration for the CAD workstations supporting circuit analysis and layout. The TI MCM team and TI's computer configuration group met and priced out the hardware configuration necessary to support the business plan. The results are shown in Section 3.

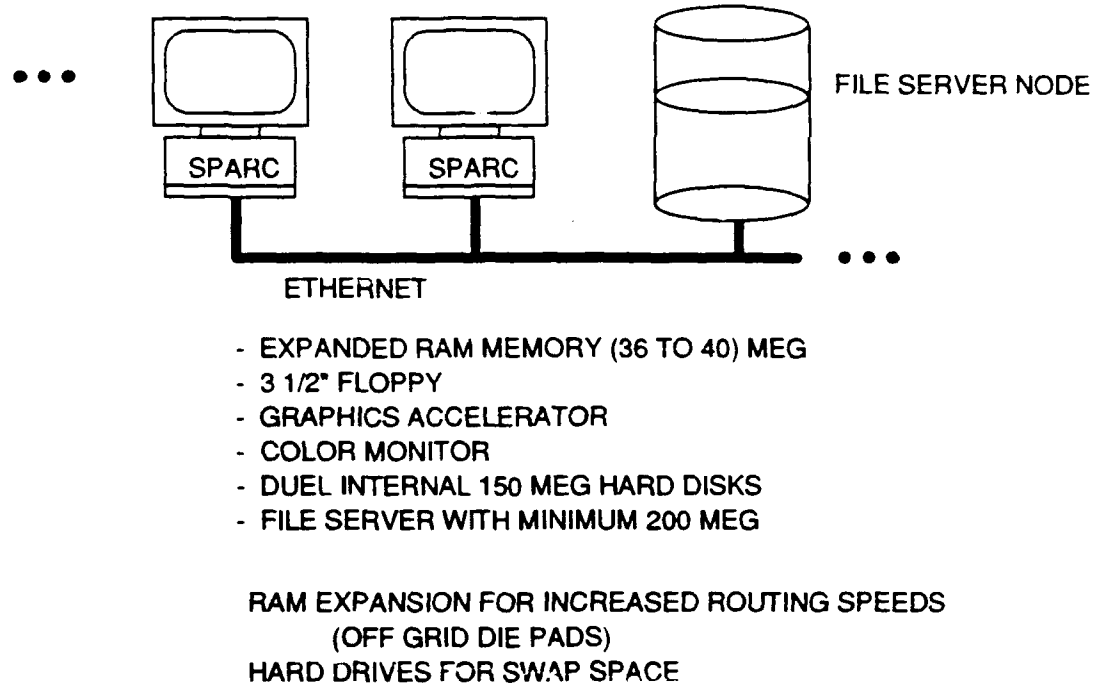


Figure 4-22. Suggested Configuration

4.2.2.3.3 Foundry Software Configuration. Task Technologies worked with the MCM team to put together a phased software plan to support the MCM business plan. This report's cost analysis reflects this work. The plan's first stage is the configuration of a baseline system to support technology transfer. The following steps increase the design capacity of the foundry by adding additional layout systems. Each layout configuration includes the following software:

- OMNICARDS Interactive HDI Layout Software
- OMNIROUTE Hybrid automatic router
- D-file Parser for custom database interface programs
- P-CAD bi-directional netlist.

4.2.2.4 DA Risk Assessment. The following areas are regarded as DA risks. They are categorized into high, medium, and low risk categories, and progress toward resolving the issues is also stated.

High — Ability of Task Technology router to handle large (10K- 15K from-to) circuits.

Task performed a medium complexity benchmark for the MCM team (1500 from-tos) that routed to completion. Long routing times, not system capability, will be the limiting factor on larger circuits. Faster computers and dedicated resources will relax this problem. The MCM market survey will define the extent of the problem.

Medium — No layout alternative exists for GE's MCM approach.

The MCM team met with Mentor Graphics who committed to giving an estimate for enhancing their router for GE MCM capability. Their decision on implementation will be business driven.

Also, Layout Concepts, Inc., was contacted and is willing to work with the MCM team on enhancements. Layout Concepts furnished the core router to Task Technologies from which the Omnicards system was built.

Medium — Ability to incorporate analog, microwave, and optical circuitry into digital designs.

Though fundamentally possible, this capability is missing from the baseline system. University and commercial development is underway in this area.

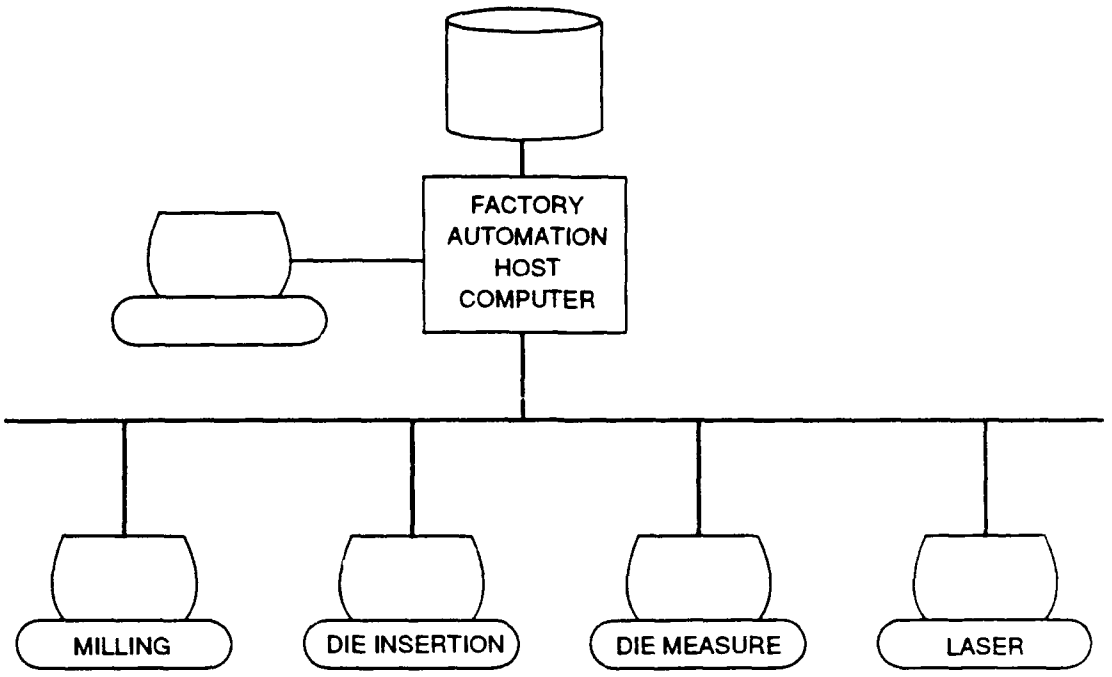
Low — No part model library approach is in place to supports the entire MCM design and manufacturing system.

Enhancement and use to TI's ASIC part model library approach was investigated and is a good mid-term possibility. A part model library approach was constructed and is discussed in this document.

With the exception of layout alternatives, the risks are associated with all MCM technologies.

4.2.3 Factory Automation Data Control

4.2.3.1 Current Environment. Figure 4-23 shows the N/C controlled machine environment established for the HDI process. This environment provides a common HDI database which is available to all process centers. Data files which are basic to the HDI process are contained in reference libraries. Data files which are project specific reside in a subdirectory created specifically for that project.



2011-5

Figure 4-23. Multichip Foundry Manufacturing Automation System

Figure 4-24 shows GE's current overall N/C data flow methodology.

Module layout and routing tools produce a D-file and NC-comp file. The D-file contains the via and metal run information while the NC-comp file contains component placement and pad locations. A mechanical file is also generated which contains information such as substrate size, fiducial location, chips requiring back-side bias, etc. Component dimensions and pad locations are contained in the measure file library. Commonly used adhesive dot patterns are contained in the epoxy pattern library. The waffle file library contains descriptions of standard waffle packs used to supply components for the die insertion operation. These reference files, along with the D-file and NC-comp files, comprise the basic information database which is required to build an HDI module.

Milling and placement information is extracted from the NC-comp, epoxy pattern, measure, and mechanical files. The milling information file which contains the location and dimension of each pocket, along with the location of mill fiducials. The chip file contains component placement information. The epoxy file contains the location of dots of adhesive to be placed under each component.

The D-file is fractured into via drill and metal files. One drill file is generated for each layer. The drill files contain the location of each via on a particular layer. One metal file is generated for each interconnect layer. In addition, a legend layer is generated from either the D-file or the NC-comp file by LEGGEN which identifies the adaptive lithography region.

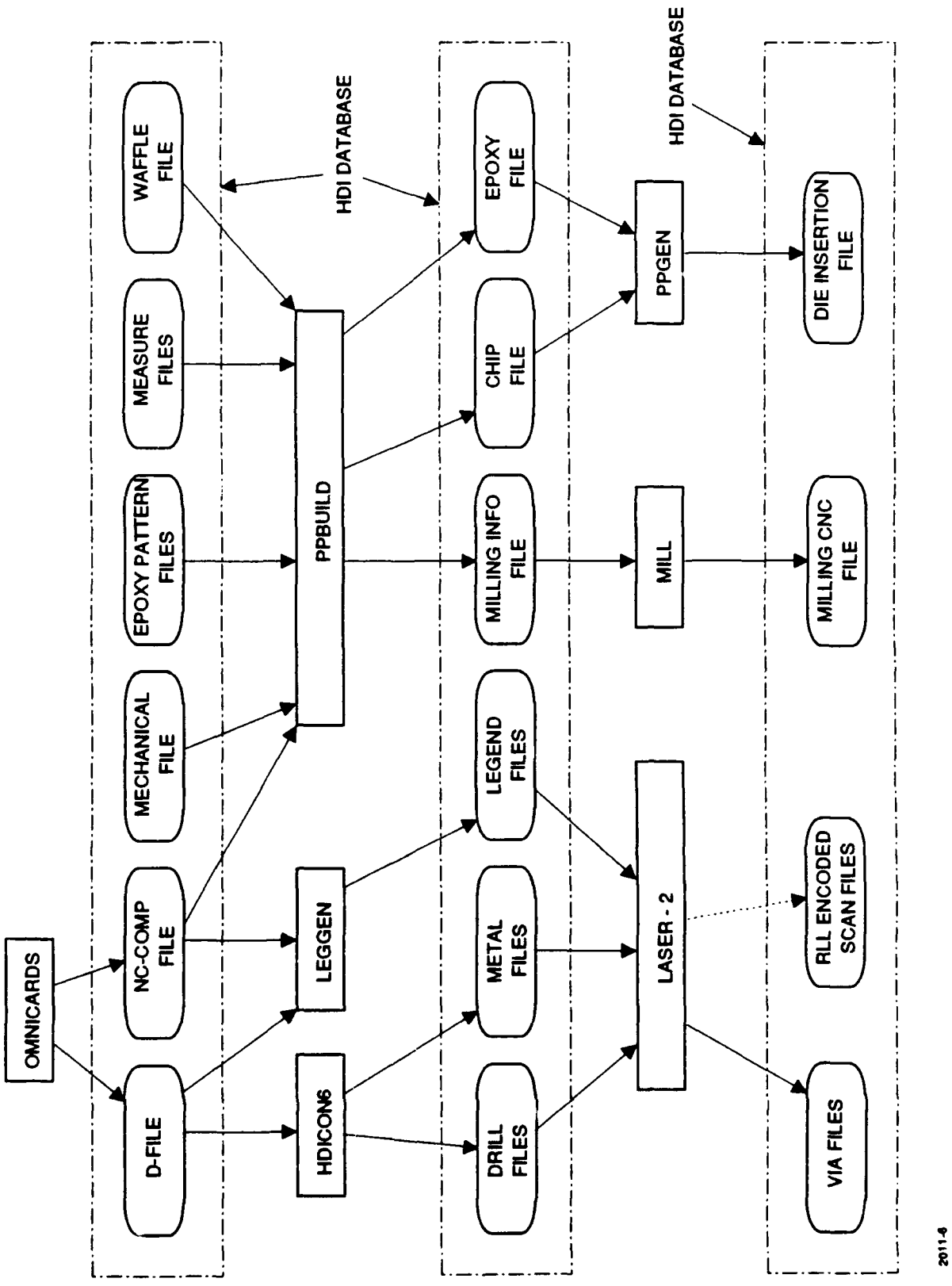


Figure 4-24. N/C Data Flow Methodology

The MILL program operates on the milling information and produces a N/C file which is compatible with the milling machine. PPGEN takes the chip and epoxy files, along with the waffle pack information, and produces a file which is compatible with the die insertion machine. LASER-2 uses the drill, metal, and legend files to produce a via scan and RLL encoded scan file for each layer. The via scan files contain the via sorted so they can be drilled as the laser scans over the module in successive swaths. Similarly, in the RLL encoded scan files, the metal run information is set up so the metal can be patterned as the laser scans the module in swaths.

4.2.3.2 **System Evolution.** Figure 4-25 depicts a future architecture for the factory automation control system.

This automation system is part of the in-process data management environment for the HDI process. The system will be designed to permit importation of data and files from customers at the various identified insertion points in the design flow.

The system is expected to take advantage of relational data structures to provide extensibility of the factory automation data dictionary. The data base kernel is expected to consist of a relational data base. Access is controlled through a security system to ensure only authorized applications access the data contained in the data base. The data in the data base will be configuration controlled to ensure current versions of the data is provided to the various applications. A communication layer provides remote access by the various applications which need to access the data.

The data base is expected to contain:

- Released design data bases
- Parts and reference designator lists for specific designs
- Chip library data
- Packaging library data
- Manufacturing process and machine specific data
- MCM manufacturing data; measure files, inspection data, etc.

Software applications shall be developed for each N/C machine to extract data relationally from the data base and process the data into machine data files. These files may either be in machine format or neutral files, which may be post processed into machine files.

Operation results will be collected and fed back to the data base for use by subsequent operations.

Initially, files in the data base will be a local format. The system will be constructed to permit a migration to industry standard formats, such as PDES, etc., as these formats comprehend MCM product design requirements.

Access to the automation system will be provided through a seamless interface architecture designed to permit easy navigation between factory control and automation systems.

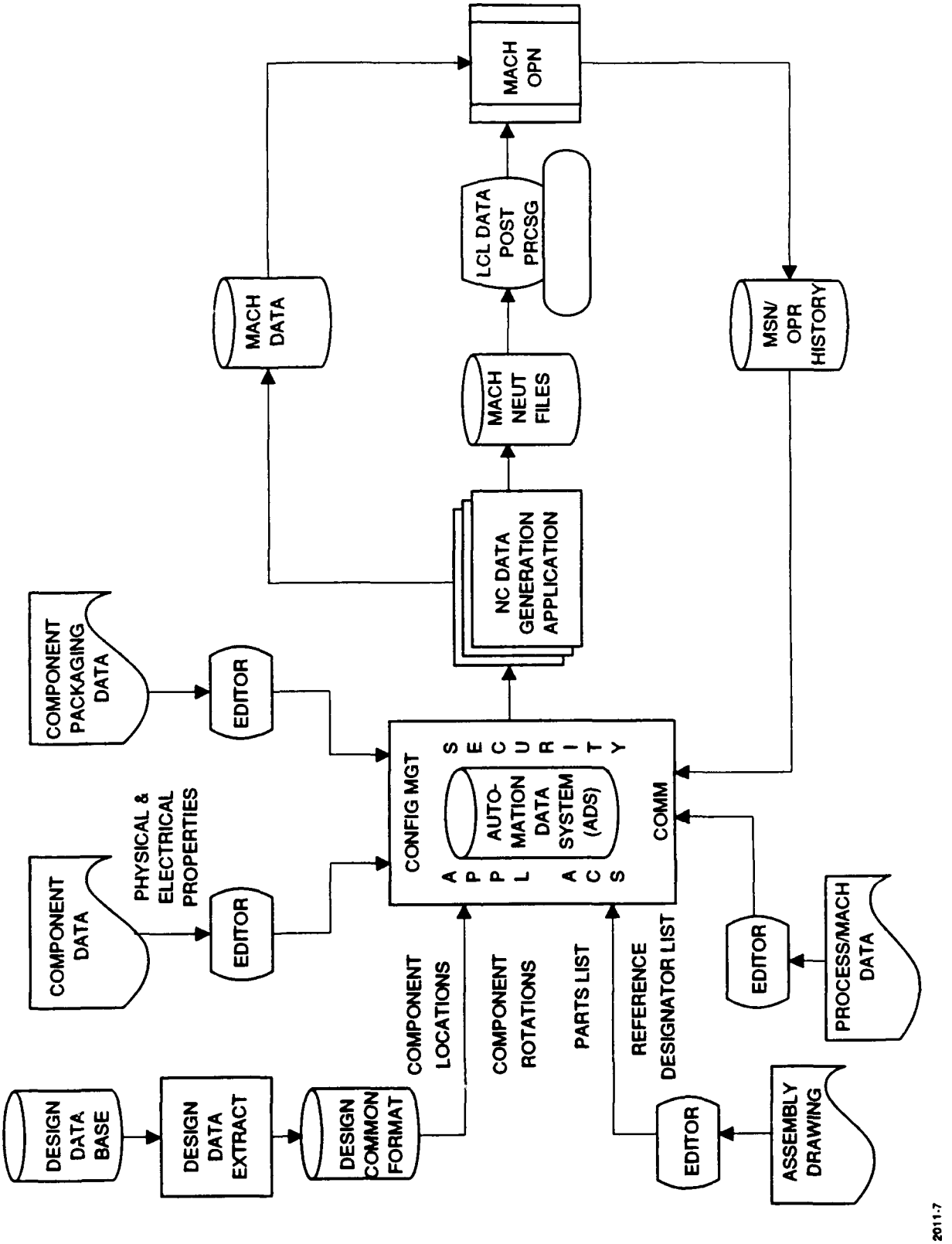


Figure 4-25. Multichip Foundry Factory Automation Control System

4.3 MANUFACTURING PLANNING & CONTROL

4.3.1 Preface

Purpose: This section describes a proposed manufacturing planning and control application systems environment for the high volume multichip facility.

Organization of Section: This section presents an overview of the issues and plans for creating a manufacturing control environment which is necessary for the support of a high volume MCM facility. Specifically, the section will look at the background and status of these capabilities at the General Electric Central Research Facility and Texas Instruments.

4.3.2 Summary

Texas Instruments and General Electric, as part of their technology sharing arrangement, have agreed to transfer the existing factory control structure for the manufacture of MCMs. This transfer includes the process flows and recipes for controlling the fabrication of MCMs. TI will accept this initial transfer and enter it into its factory control system as a baseline from which to build processing and manufacturing improvements. In addition, TI will integrate the manufacturing control environment into the existing business environment for Custom Manufacturing Services through a series of interfaces. These include both organizational and systematic interfaces. Much of this work will be accomplished during the execution of the Merchant MCM Foundry Program. Extensions of this basic technology transfer will be accomplished as part of the commercialization of the product. A goal of the factory control environment is to remain flexible, allowing insertion of new product technologies, such as microwave and analog, with little or no system impact. The control system environment itself must remain flexible to permit insertion of new planning and control system technologies, such as the Microelectronic Manufacturing Science and Technology (MMST) control system, as the processes in the foundry become more automated.

Project Background and Status: The TI program team has completed several preliminary technology transfer visits to the General Electric Facility to determine the best approach for accomplishing the initial technology transfer. GE controls the fabrication process with a series of recipe steps recorded in a commercially available planning and control system, PROMIS™. The TI team is familiar with this product. PROMIS™ is used in the Microelectronics Packaging Systems (MPS) organization for manufacturing control of surface mount and hybrid technology products. Additionally, the technology transfer team has looked at the business and manufacturing planning systems currently installed in TI's Custom Manufacturing Services (CMS). The purpose of this investigation is to determine how the MCM factory planning and control system would interface with these systems.

Implementation Summary: The most direct approach for the initial technology transfer is to use the PROMIS™ factory control system. Both GE and TI are familiar with the system. Using this common transfer vehicle, the initial technology transfer is accomplished with a minimum of resources and utilizes existing computer platforms. TI will

conduct a further investigation to determine if PROMIS™ is the most attractive long term solution for the high volume facility.

The CMS systems goal is to leverage off the experience of other TI organizations and systems for support. As previously mentioned, MPS has experience with managing several technology products using PROMIS™. The Semiconductor Business segment of TI is currently using an in-house developed product, Semiconductor Manufacturing System 370. Unlike PROMIS™, which executes on a VAX™ platform, this system executes from an IBM Mainframe platform. A goal of the CMS organization is not to develop a computer support organization. The choice of system will include a system support agreement which allows that organization to buy computer support services. An additional factory control system which will be considered for insertion at some year in the future is the MMST factory control system. This system is being developed initially for automated slice processing wafer fabrication facilities. Discussions have been initiated to determine what resources will be required to extend the system capability to include the requirements for multi-chip processing if TI's processing technology approaches full automation.

4.3.3 Vision

The vision for the high volume manufacturing factory control system includes an organization and system which functionally mirror each other. Both the factory control system and MCM manufacturing organization will complement existing CMS organizations and systems through a series of regulated interfaces. These interfaces will appear to be seamless as information freely flows between both systems and organizations facilitating the goals of the concurrent engineering environment.

4.3.4 Approach

The approach for accomplishing the initial technology transfer, to be followed by an evolution into the high volume environment, is described below. For the initial technology transfer a TI systems analyst will spend at least one month at the GE facility gathering the details of the existing product process flows. These details will include copies of the processing recipes, data collection operations, lot processing rules, product identification schemes, etc. Upon returning, the TI engineer will form a PROMIS™ implementation team. Using program planning documents from other successful implementations of PROMIS™, a custom program plan will be developed. The team will consist of members from the various factory functional organizations. The team members will have decision making authority. Using this decision making authority, the factory procedures and rules governing the factories operations will be constructed in parallel with the PROMIS™ system implementation. This ensures that the factory procedures are very tightly coupled to the factory systems and organizational environment. The team will be responsible for constructing an initial model and to complete test tracking of lots through the model in order to validate the flow. Several product flows will be constructed with the customization reflecting the various customer requirement differences which are activated at the various points in the flow, such as required inspections or tests.

PROMIS™ is very powerful from this standpoint, as conditional processing is provided and controlled by a series of parameters which activate or deactivate various processing options and control procedures. Initially, it is anticipated that PROMIS will not interface with other systems. This interface will be accomplished manually in the low volume, early days of the technology transfer.

To grow from the low volume baseline HDI technology facility to the high volume facility, the planning and control system will evolve. This evolution will take two paths. First, the PROMIS™ implementation will evolve as the process plan is modified for high volume production. Possibly, a replacement for the PROMIS™ system may be required. After the initial implementation is completed, a second team will begin an evaluation of high volume facility requirements and features offered by various systems. These requirements should include an analysis of interface requirements for both business systems and automation systems in the factory. The high volume factory control system should permit the free flow of information between the various systems through a series of regulated interfaces. TI has experience in its current PROMIS™ environment interfacing to both interactive and batch updated systems. Similarly, interfaces have also been developed for the SMS370 system. Using the experience gained in accomplishing these interfaces, the factory control system for the MCM facility will be integrated into the CMS environment and custom MCM factory automation systems. As part of the high volume facility study, strong consideration will be given to the MMST manufacturing control system. This system features integrated factory control and process control. If determined that the long term solution includes the MMST system, then the choice to continue to use PROMIS™, SMS370, etc., must be considered a temporary solution and, as such, initial cost to implement and cost of conversion must be a major consideration in addition to the functionality provided.

4.3.5 Microelectronics Manufacturing Science and Technology Insertion

The MMST program is developing a generic manufacturing technology for the mid-1990's. The program is being jointly funded by DARPA, the Air Force, and Texas Instruments. The program is to develop and demonstrate fast cycle time, cost effective microelectronic manufacturing. While the initial demonstration will be on silicon devices, the technology is applicable to other technologies. The SWAP team is working very closely with the MMST development team to make our technology requirements known. Their system is not yet sufficiently developed to determine the cost of extending the capability to include the multi-chip technology.

The MMST control system must provide:

- Flexible manufacturing
- Reduction of cycle time
- Closed-loop supervisory process control with recipe management
- Graphical user interface for multiple user groups
- Embedded artificial intelligence based on scheduling and planning
- Integrated factory simulation capability.

The MMST program is working with equipment manufacturing suppliers to develop "cluster tools". Cluster tools are arrays of processing equipment around a central module handling host. Worldwide cluster tool standards are being developed through Semiconductor Equipment and Materials International (SEMI). Mechanical utilities and communications standards are under development. Once implemented, any "SEMI Standards" process module will fit on any "SEMI Standards" module handler. Modularity in manufacturing equipment will be a key contributor to cost control.

The process equipment manufacturer with the best process, the best mean time between failures (MTBF), and with the best price will win the market. This will stop and, hopefully, reverse equipment cost escalation. It will also result in reliable equipment. This argument is also valid for the central module handler. The equipment manufacturing scenario changes the way industry operates. It fosters "best-of-breed" while controlling costs through equipment modularity and volume learning.

The microelectronics industry uses statistical process control. This requires the use of extensive "pilots or TEGs". The pilot modules are removed from the process line and analyzed off-line. These off-line activities are labor intensive, time consuming, and a major contributor to poor cycle times. MMST will not use pilot lots. Each module will be its own pilot and will have laser inscribed identification. This ID will be read and the appropriate recipe downloaded from the factory control system. The recipes will give the process equipment the target value along with pertinent past processing information. The process chamber will then compute equipment settings. These settings will be validated and then passed to process. The modules will be processed and sensors will measure the module state.

Statistical analysis of the module data, along with that from past modules, will define whether model tuning is required. If tuning moves outside control limits, other actions such as chamber cleaning will be used.

Sensors will be used both in the process chamber and in the load lock chamber. Module characterization will be done on each module after processing. Statistical analysis of the results will be fed back into the process model to drive the process to the target value.

It is intended that the high volume facility be constructed such that it can take advantage of this new technology as it becomes available both in terms of computing functions and equipment availability.

4.3.6 Manufacturing Planning & Control Functions

4.3.6.1 Factory Control System. The factory control system, as depicted in (Figure 4-26) shall be expected to provide the following functional support:

- Factory Communications
- External Systems Interface
- Automated Material Movement
- Engineering Data Collection

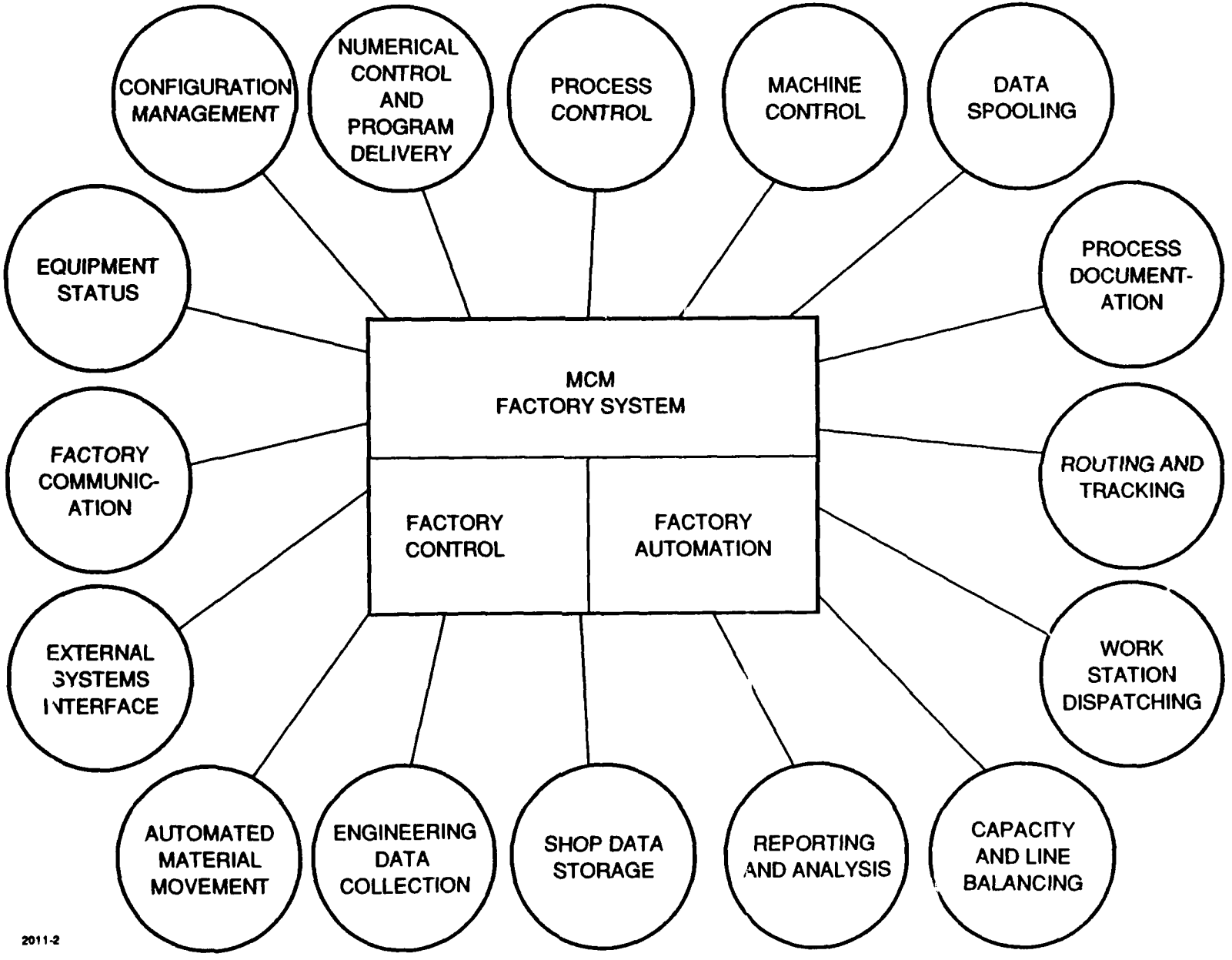


Figure 4-26. MCM Factory System.

- Shop Data Storage
- Reporting and analysis
- Capacity and Line Balancing
- Work Station Dispatching
- Routing and Tracking
- Process Documentation
- Data Spooling
- Machine Control
- Process Control
- Numerical Control Program Generation and Delivery
- Configuration Management
- Equipment Status.

Factory Communications: The factory control system shall be expected to provide a factory electronic mail system for communicating changes in equipment status or lots which have been placed on hold. The shall additionally be used as a vehicle for ad-hoc factory communications and announcements.

External Systems Interface: The factory control system shall be capable of interfacing with external systems. This interface shall be constructed such that the communications may be accomplished by batch file transfers or interactive transaction based communications.

Automated Material Movement: The factory control system shall be capable of interfacing and controlling automated material movement devices which transports the factory work-in-process from workstation to workstation.

Engineering Data Collection: The factory control system shall feature an engineering data collection facility which may be user configured to collect process data, either manually or through automated collection devices. This data collection may be either directly related to lots being processed or related to the facility as a whole.

Shop Data Storage: The factory control system shall provide a capability to store engineering and product status data collected during the build cycle for a given product.

Reporting and Analysis: The factory control system will contain a user configurable reporting and analysis to permit access and processing of engineering data collected within the factory control system.

Capacity and Line Balancing: The factory control system will contain a factory planning capability to permit the local planning for work-in-process consistent with just-in-time philosophy of the factory.

Work Station Dispatching: The factory control system will provide a capability for operators to display lots in queue for their workstation in priority order, as determined from the shop work-in-process planning system.

Routing and Tracking: The factory control system will provide a routing system to control the process plan for individual lots. This system shall contain conditional processing capabilities which permit the customization of the process plan to recognize individual customer requirements.

Process Documentation: The factory control system will contain a capability to display textual and graphical instructions supplementing the information in the routing. These documents may be referenced standards or specific customer requirements.

Data Spooling: The factory control system will have the capability to extract and store both batch and interactive interfaces. The data shall be spooled to staging libraries prior to transfer to the interfaced systems.

Machine Control: The factory control system will provide an environment in which machine control operations may be seamlessly accessed from within a common user interface.

Process Control: The factory control system will provide for the manual or automated delivery of process parameters to process controlled operations.

Numerical Control Program Generation and Delivery: The factory control system will provide a seamless interface capability to automation system which generates and delivers numerical control programs to equipment in the factory.

Configuration Management: The factory control system will provide for configuration management of controlled data and documents within the control of the system. The system will provide for revision level approval and activation.

Equipment Status: The factory control system will provide a mechanism for monitoring equipment status and availability. If equipment is not available for production, lots will not be allowed to be tracked into that operation.

4.3.6.2 Organizational Interface. The manufacturing organization will interface with the factory control system for both an input and output. It is important that each organization contribute to the overall operation of the system from an input standpoint. It is equally important that the organizations get something in return for their efforts. This interface is shown in Figure 4-27.

Process Engineering: Process Engineering will provide processing documentation and parameter cards for the various operations in the flow. In return, this organization will receive feedback from actual lot processing in the form of control charts and engineering data which can be fed to their analysis systems to aid in continuous process improvement.

Production: Production records the build history for individual lots and inputs the engineering data associated with each lot. In return, production receives from the system build instructions in the routing and documentation. In addition, changes in equipment status are reported to ensure that the product is not built on equipment which is not production

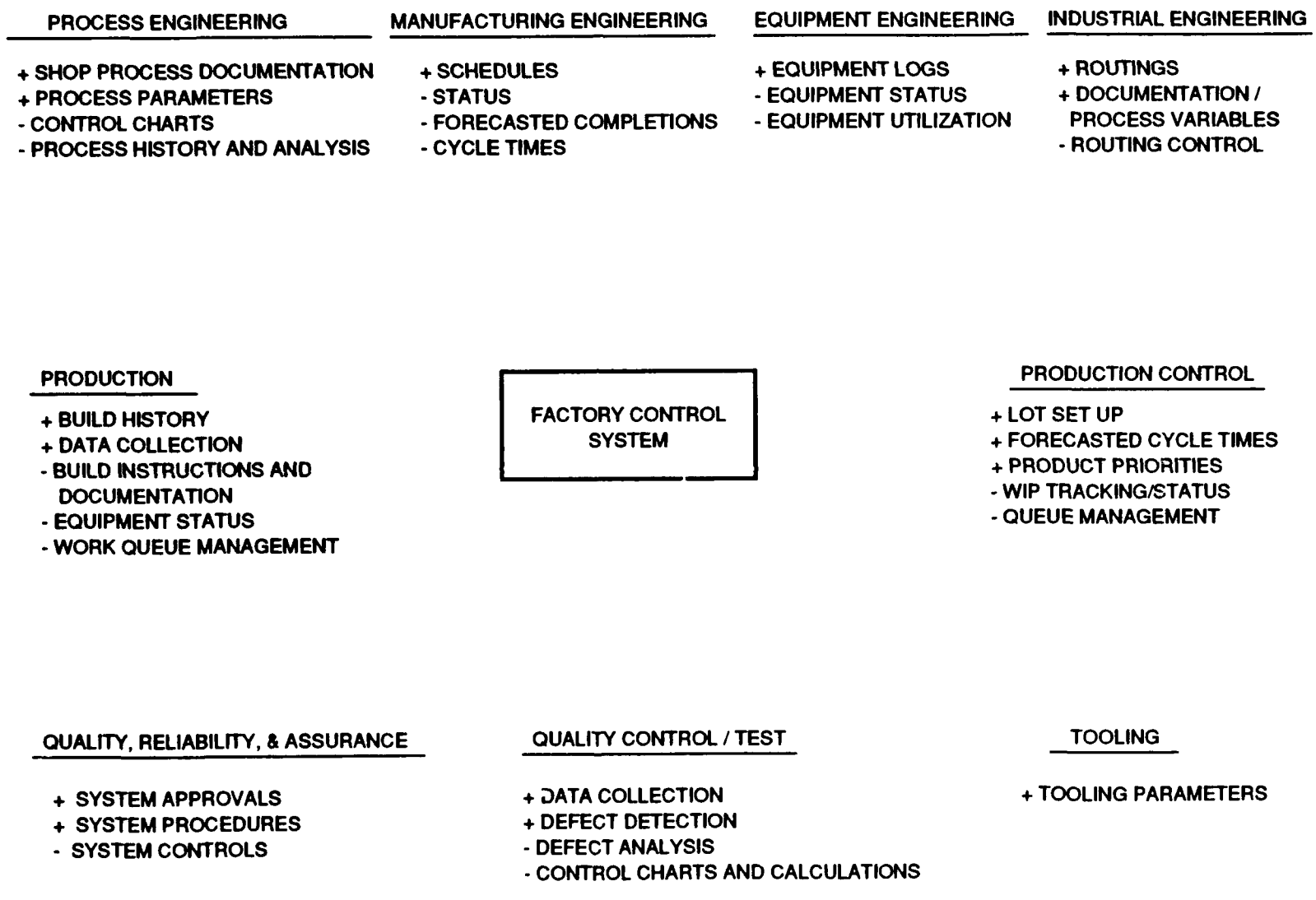


Figure 4-27. MCM Factory Control System Users.

ready. The system also assists with work queue management by maintaining a work station dispatch list in priority order for each operation.

Quality & Reliability Assurance: QRA manages the integrity of the system by providing signoff and approval for the various procedural changes in the system. These changes include document and recipe revisions, as well as lot identification information. In addition, QRA maintains the operational procedures and audits for compliance. In turn, the system is designed to take advantage of these control procedures by providing a control manufacturing environment to ensure that customer requirements are met.

Quality Control and Test: QC and test record defects are identified as a result of completing various specified inspections and tests. The results are passed on to production for correction of the nonconformance. In return, QC and test receive detailed analysis of defects and control charts to indicate if the factory is in control of its various processing limits.

Tooling: Tooling provided the system with tooling specifications to ensure that the correct tool is matched with the correct module.

Production Control: Production Control sets up the lots within the system. During this set-up, specific parameters are assigned to the lot to facilitate status reporting. In addition, the lots are assigned a priority to be used by the system in scheduling the lot through the shop. In return, production control receives status of work-in-process. This data may be analyzed to ensure that the product continues to move, minimizing cycle time for the various products in the shop.

Industrial Engineering: Industrial engineering is responsible for setting up the routing and specifications for the various products in the shop. In return, the system provides a controlled environment to ensure lots will be processed according to the customer requirements which have been provided.

Equipment Engineering: Equipment Engineering is responsible for data entry into the equipment logs recording Maintenance activities and unplanned down-time occurrences. In return, the system provides reporting, describing equipment status, and equipment utilization.

Manufacturing Engineering: The manufacturing engineers provide schedule of end item delivery requirements. In return, the system provides status of work-in-process versus these delivery requirements, forecasted completions, and cycle time data

4.3.6.3 Multichip Manufacturing Planning and Control Systems. The multichip planning and control system needs will be served by two system families; a) marketing and shipping systems b) manufacturing systems (Figure 4-28). The marketing and shipping systems are used to service the customer requirements for sales order management and shipping. The manufacturing system serves internal needs to build the product to the customers requirements.

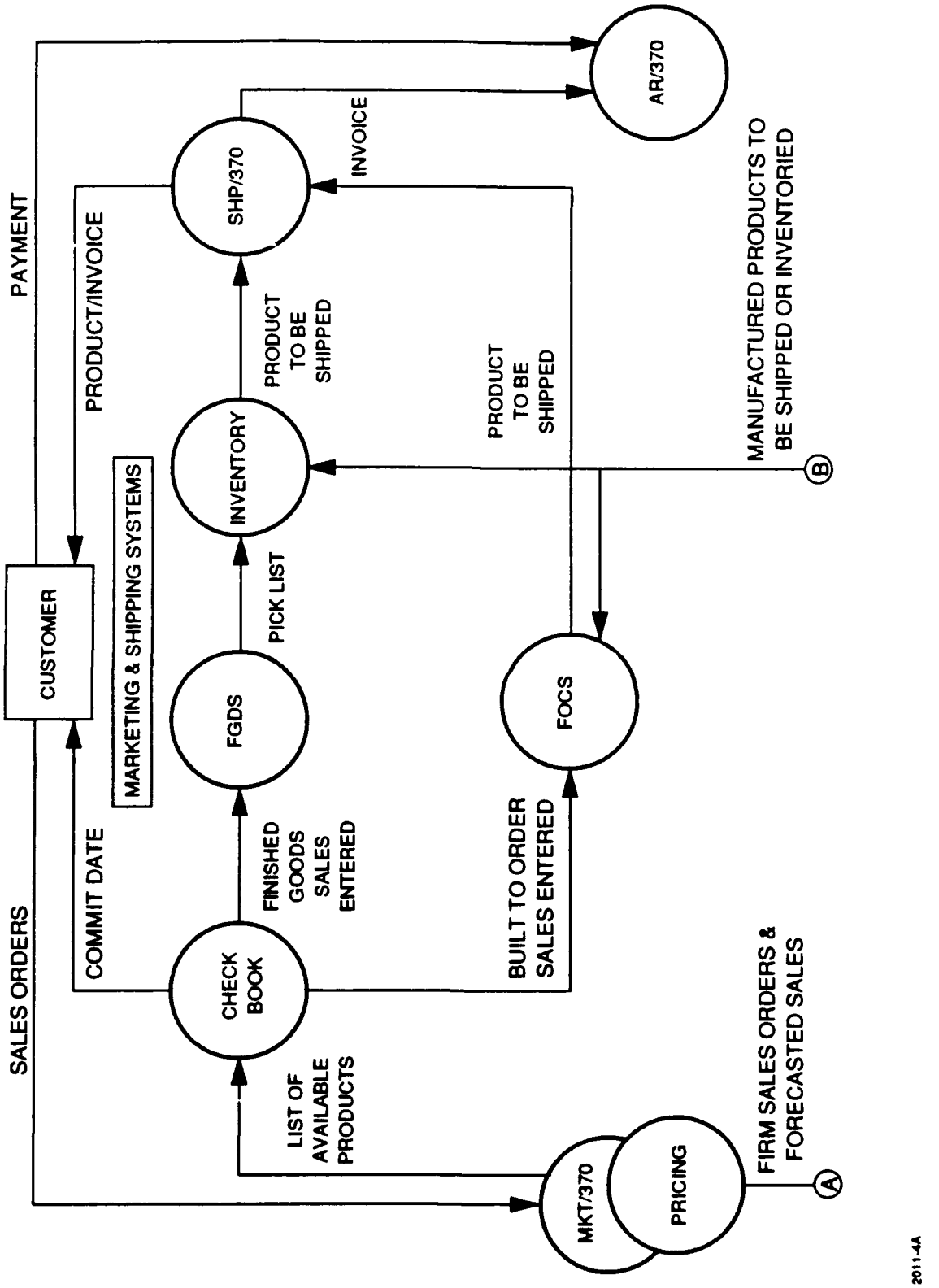


Figure 4-28. Multichip Manufacturing Planning and Control Systems.

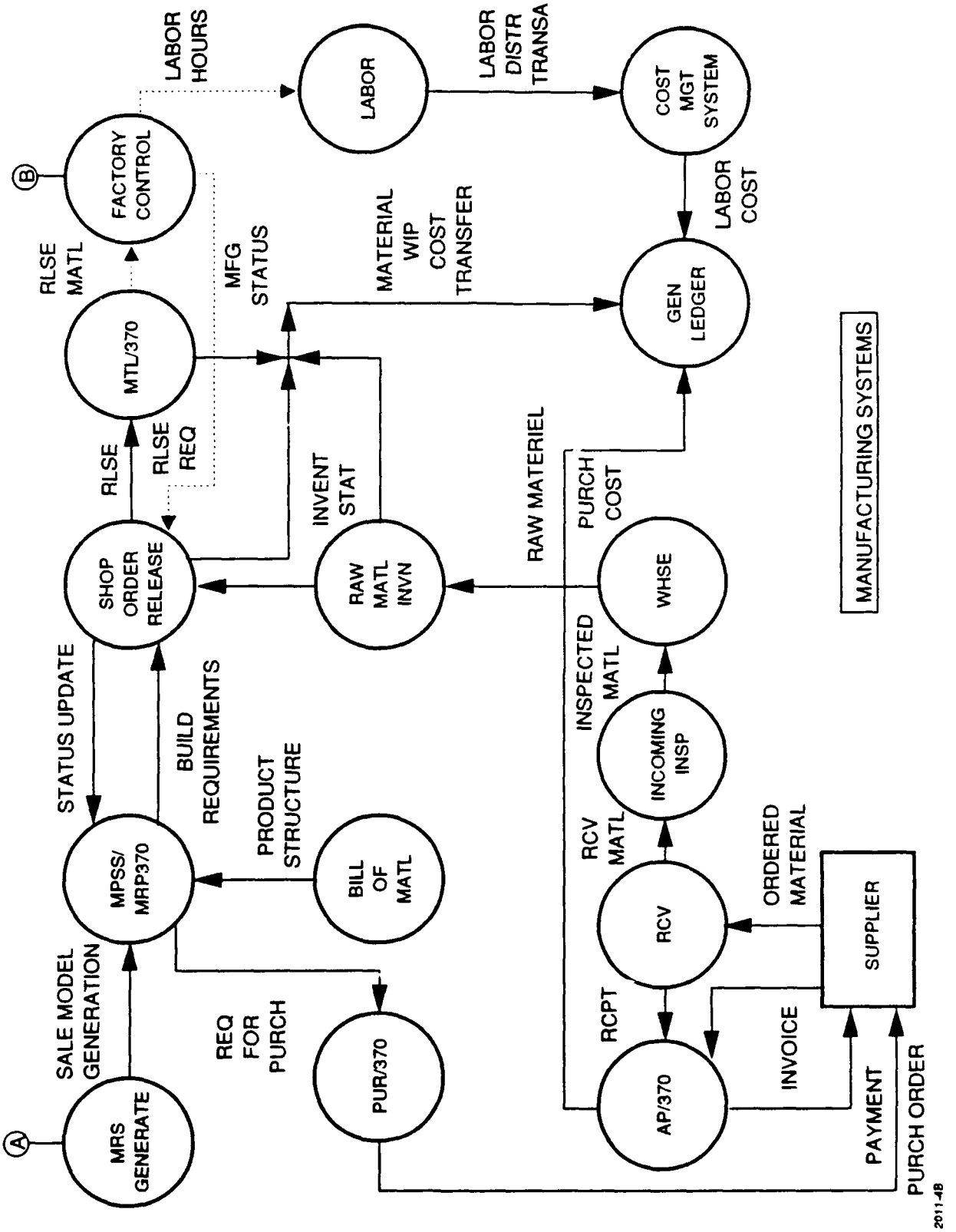


Figure 4-28. Multichip Manufacturing Planning and Control Systems (Continued).

4.3.6.3.1 Marketing and Shipping Systems. The MKT/370 and Pricing system is used by the marketing staff to record customers orders. This is the source data base for recording the monthly net sales entered. These data bases are configured with standard and non-standard product descriptions and their prices. This system can access the check book system to determine availability of finished goods to determine lead times. In addition, the firm and forecasted data can be fed to the material requirements generation system to provide a potential build plan to the manufacturing systems.

Check Book: The Check Book system, in addition to providing product availability data to the MKT/370 system, also provides detailed sales data to the finished goods distribution system and factory order control system. This detailed sales data is used to generate the detailed pick lists for shipping personnel to configure shipments to the customer.

Finished Goods Distribution System and Factory Order Control System: These systems are used to configure customers shipments as products become available for shipment. The finished goods shipment distribution system is used to service parts which are built to a standard configuration and placed in inventory prior to orders being received. The factory order control system is used to process orders for non-standard configurations built to a specific customer order. Both systems generate pick lists for material control personnel to fill customer orders.

Finished Goods Inventory: The Finished Goods Inventory is the system used to record the status of warehoused finished goods staged for potential sale.

SHP/370: The SHP/370 system is used to record the actual material pulled and readied for shipment to the customer. The SHP/370 system generates the shipping documents and invoice sent to the customer. In addition, the shipment record is forwarded to accounting for creation of the accounts receivable record.

4.3.6.3.2 Manufacturing Systems. MRS Generate System: The MRS Generate system is the system which converts firm and projected sales into manufacturing requirements. This projected plan can be organized into a suitable manufacturing plan and fed to the manufacturing planning systems.

Master Planning and Schedule System and Material Requirements Planning System: These systems are used to convert the system requirements into detailed manufacturing requirements. These systems use a Bill of Material system to specify purchase part requirements and build requirements. Purchased part requirements, which cannot be satisfied by existing raw material inventory quantities or open purchase orders, are requested for purchase. The planning systems receive status updates from the shop order release system.

PUR/370: The PUR/370 system is used to record negotiated purchase order details with suppliers. Upon receipt of material from suppliers, the purchase order is updated, and a payable transaction is created with accounting, awaiting receipt of the supplier invoice.

Incoming Inspection: The Incoming Inspection system notifies receiving personnel of the incoming inspection requirements for received material. After the incoming inspection has been completed the material is transferred to warehouse personnel for stocking.

Warehouse and Raw Material Inventory: Warehouse personnel use the Warehouse and Raw Material Inventory system to stock raw material for manufacturing. These systems record material location and quantity.

Shop Order Release System: The shop Order Release system is used to initiate requests to the warehouse to remove inventory from stock and to deliver the material in kits to the manufacturing floor. This system also provides status updates to the manufacturing planning systems.

MTL/370: The MTL/370 system is material control system used to assist with the material management on the shop floor. The system provides for automatic replenishment of material when shop floor material reaches reorder points.

Manufacturing Control System: As discussed in a previous section, the manufacturing control system is an integrated factory control system which is used to provide for material routing, WIP status, shop data collection, process recipe specification, factory floor scheduling, etc.

Labor and Cost Management System: The Labor and Cost management system are used to collect labor inputs from operators distribute the inputs to the correct manufacturing workorders and feed the transactions to the general ledger.

4.3.7 Just-In-Time/Total Quality Control

TI has implemented of Just-In-Time (JIT) Manufacturing in its production areas. The lessons learned here are applicable to the MCM facility. JIT production is a method of continuously increasing productivity and improving quality. This is accomplished by using the minimum amount of material, labor, and space required to do the job. JIT is not an inventory program, scheduling technique, methodology, or lot sizes of one, but rather a philosophy of simplification and returning to basics. TI began using several elements of JIT in an effort to reduce cycle time, and these efforts are now being focused together under a JIT umbrella.

Just-In-Time is a method of operating to eliminate waste. Three key elements of JIT are:

- Decrease Work-in-Process (WIP)
- Expose Quality and Efficiency Problems
- Correct the Cause of the Problem.

These three steps are repeated over and over again in a JIT environment, which promotes continuous improvement. Although JIT is thought of primarily as a manufacturing

tool, this problem-solving technique can be applied to all areas of business. Another way to look at JIT is to picture the operation as a ship, sailing on a sea of inventory. Underneath the inventory are hidden rocks (problems) such as long setup times, low yields, poor quality, and excessive schedules. JIT lowers the level of the water (WIP) until a rock (problem) is uncovered. Production is immediately stopped so that a non-conforming product is not built, and everyone works to remove the rock (problem). Once the problem is solved, production starts up and the water (WIP) level is lowered again.

Since Just-In-Time promotes quality improvements, a supporting concept which must be implemented with JIT is that of Total Quality Control (TQC). Total Quality Control emphasizes: 1) continual quality improvement, with a goal of Zero Defects, 2) moving responsibility for quality from QC to the worker - building quality into a part instead of inspecting defects out, 3) quality control of every process and every part eliminate lot sampling, which allows some defects to pass, only to be reworked later, and 4) develop measures of quality which are visible, simple, and understandable.

JIT/TQC techniques which TI is addressing in an effort to reduce cycle time and cost are:

- Lot-Size Reductions - Reduce lot sizes toward a goal of one.
- Setup Time Reduction - Reduce operation setup times to allow smaller lot sizes to be processed efficiently.
- Pull Scheduling - Use the last operation to pace the assembly line, rather than pushing work through from the front of the line. A worker cannot produce more product until the downstream operation has completed and needs more work. If someone is stopped for a problem, the entire line is stopped and directed to solve the problem, rather than continuing to build non-compliant parts.
- Under-Capacity Scheduling - Allow enough time in the daily work schedule for problems to be identified and worked, while ensuring the daily schedule will be met.
- Worker-Centered Quality Control - Everyone is responsible for building in quality. Operator inspection of the product is a part of each step.
- Multifunctional Workers - Workers are cross-trained for numerous tasks. They can move to the work or aid in solving problems, rather than working to stay busy.
- Flow Lines - Shops are organized by product flow, not functional groups, to promote communication and teamwork.
- Rigorous Preventative Maintenance - Operators perform daily maintenance on their own equipment, reducing line shutdowns due to equipment breakdowns.

By implementing JIT/TQC, TI will see significant cost, cycle time reductions, and quality improvements.

4.4 TEST AUTOMATION

4.4.1 Current Test Strategy

Many tools and techniques will be used in the high volume and prototype environment to reduce test costs and cycle time. The test automation plan will need to be flexible to take advantage of tools, test strategies of die manufacturers, and foundry capabilities, to produce the most cost effective solution for each MCM design.

Current test methods are not extendable from one level of test to another due to the unstructured methods used. A limited amount of access through test pins or probes will be available on MCMs to support the unstructured test methods. Design for Testability (DFT) methods will be used in the foundry to allow access to test circuitry and reduce the cost of test for MCMs. DFT methods are based on a structured approach that uses test structures of one level to be reused at the next level of test. As an example, the IEEE 1149.1 boundary scan bus standard will be used for both interconnect testing of die, and for four-wire access to built-in self-test and communication to other test structures. DFT will be linked to the CAE/CAD system for design rule checking of test structures. The foundry will provide DFT services to the customer to improve the chance of first pass success.

Factory test equipment will be developed for Manufacturing Defects Testing (MDT) that will make maximum use of testability features. Software tools for improving DFT and test program generation times will be integrated into the test strategy. Examples of the software needed in the foundry include:

- Analysis tools
  - Noise analysis
  - DFT analysis/advisor
- Algorithmic test generation tools
  - Boundry scan pattern generation
- Fault Simulation tools
  - Understands boundry scan as available I/O
  - Fault grade of built-in-test
- Translation tools
  - Net list and fault dictionary for IC type tester
  - EDIF for test
- Execution tools
  - Test routines on ATE for fault dictionary
  - Interactive software for diagnostics

Standards will be used to improve communication with the customer and for reducing the time to create test programs. Electronic Data Interchange Format (EDIF) will be

used as test formats are incorporated into the standard. The IEEE 1149.1 bus standard, and future 1149 standards, will be used to improve access to MCM test circuitry.

Incoming die quality will be of major importance to the first pass yield of MCMs regardless of the assembly technique. The foundry will interface with die manufacturers to establish incoming die quality and any further testing that is required. Temporary packaging techniques, transferred from GE, will be used to accommodate die test and burn-in until the die manufacturers transition to a level of testing at probe that is equal to the tests currently done at the package level. Lot qualification will be part of the incoming strategy to reduce costs. Die handling techniques need to be developed to test, or burn-in those die not tested adequately at the manufacturer. The implementation plan includes a roadmap for incoming die test, MDT test, final test, and software support.

Risks include the ability of the die manufacturers to transition to improve testing at the die level and the incorporation of DFT into the customers designs. These risks are associated with all MCM technologies.

4.4.1.1 Applicability to Foundry. In general, ad-hoc test methods are being used in most areas of the electronics industry, including GE and TI. These methods vary widely depending upon the technology, application, customer, etc. Products developed for a military customer have test methods that are dictated to some extent by the contract and military guidelines such as MIL-STD-883. Built-in self-test (BIST) and built-in test (BIT) are contract requirements. The term BIST is used in this document to mean that hardware built into the deliverable product that is specifically included for testing purposes. The term BIT is used in this document to mean the software delivered with the product that is executed by the deliverable product to test itself in its application environment. Another typical military contract requirement is the product environmental test. These military requirements result in unique solutions which are not generally transportable to other products.

The situation is usually quite different in the commercial arena. The commercial electronics industry employs a variety of test strategies. They are driven by the need to satisfy their customer(s), deliver a quality product, and keep the manufacturing cost minimized. The test methodology is often driven from the internal organization that is prevalent, such as manufacturing or marketing.

MCMs may be used in a wide variety of commercial and military products. Each of the products may require a different test method. Therefore, the MCM foundry has an absolute requirement for test flexibility.

Current test methods, like in-circuit test and 100% parallel pattern based tests, cannot be extended to be effective as the foundation for MCM test because of circuit complexity, mix in components, and unstructured test methods used. The foundry will, to a large extent, depend upon the testability built into the MCMs, in conjunction with current methods, to address all of the diverse product designs.

4.4.2 Foundry Estimates and Assumptions

There were several assumptions and estimates that had to be made to establish the foundry baseline. This section documents the assumptions and estimates that were made. These assumptions form the basis for the test portion of this study.

4.4.2.1 Mix. The amount and type of testing required in the MCM foundry and by vendors supplying the foundry, will depend on the ratio of commercial and military business. We recognize that the commercial world may have strict test requirements in some areas and performance beyond military programs, due to the rapid change that is possible in commercial products. TI estimates that the ratio of commercial to military units per design is about 20 to 1 with 1000 or greater units to be built for commercial designs. Some of these designs will require redesign to improve manufacturability. Others may be upgrades from low volume prototype designs.

The foundry will see products that are being converted from PWB designs that previously were tested with probes. This creates two problems: probing is limited and the design is already in production without the possibility of major design change. Some products will be new, or upgraded, and can be enhanced with testability to meet the mutual testability requirements of the customer and MCM foundry.

The range of circuit speed (frequency) and complexity will be determined by the individual customer, but it is expected that either performance or complexity, or both, will be a feature of all MCMs. Some customers will require testing at system speed.

The market survey portion of the study documented the pin count and frequency range which are likely to occur. It is expected that these features will remain at the forefront of technology from the start of the foundry.

4.4.2.2 Flow. Procurement of die for the MCM foundry is an area that will require flexibility. No one method will cover all the situations that are anticipated. Therefore, it is important to note that the foundry will require coordination for the purchase of die from vendors. This should include test methods, yield information, die changes, and emphasis on improved wafer testing.

Due to the mechanical constraints of MCMs, current internal probing techniques will not be cost effective. Other test methods are becoming available and will be utilized. Some customers may only require a manufacturing defects test (MDT) if adequate design verification and die testing has been done. The environmental and final tests will be determined by the customer.

The production facility will be able to produce prototypes and handle volume production. As volume increases, a volume production area will be integrated with, yet separate from the prototype production area. Rework from test will be performed on the prototype line.

4.4.2.3 Yields. Incoming die will range from simple device drivers to the latest ASICs and microprocessors. Yield data will be collected for each device type and vendor whether found at incoming test or functional test. It is estimated that about 70% of the incoming die will be adequately tested for functionality within the next few years. This is largely due to the complexity and cost of the devices selected for use in MCMs. They will be tested to a greater degree than high volume, low cost parts.

The yields at MDT and final test must be held high. The decision to test the remaining 30% of the incoming die will be determined by the cost of test and cost of repair. Each design configuration will be different and requires a combination of incoming IC test methods.

4.4.3 Foundry Research

4.4.3.1 Requirements for Test

4.4.3.1.1 Design for Testability. Figures 4-29 and 4-30 shows the historical distribution of a products life cycle cost among the different phases of its life as well as the impact of each phase. An impact on the concept phase can be accomplished by incorporating design for testability.

The purpose of the DFT guideline is to familiarize the MCM design engineer with design for testability concepts that assist in implementing designs which possess necessary characteristics for production and field testing. These methods will allow the project to control the MCM product life cycle cost by reducing the cost of test. These methods include both electrical and electromechanical structures.

Rules or software for checking, partitioning, etc., designs are being developed. Tools, like MCC's TIGER™, advises the design engineer on the partitioning and insertion of some test structures. The rule based methodology generated from an overall system design strategy, however, will apply to more designs and allows more flexibility in fault detection and isolation.

The requirements for a DFT guideline document cover the design from methodology to specific problems that need to be evaluated. The requirements for a MCM guideline are as follows:

DFT GUIDELINE REQUIREMENTS:

- Methodology Guidelines
  - Implement a hierarchical methodology for use of test structures and software.
  - Use or refer to the MIL-STD-2165 checklist.
  - Include rules for checking the CAE/CAD data base for testability.

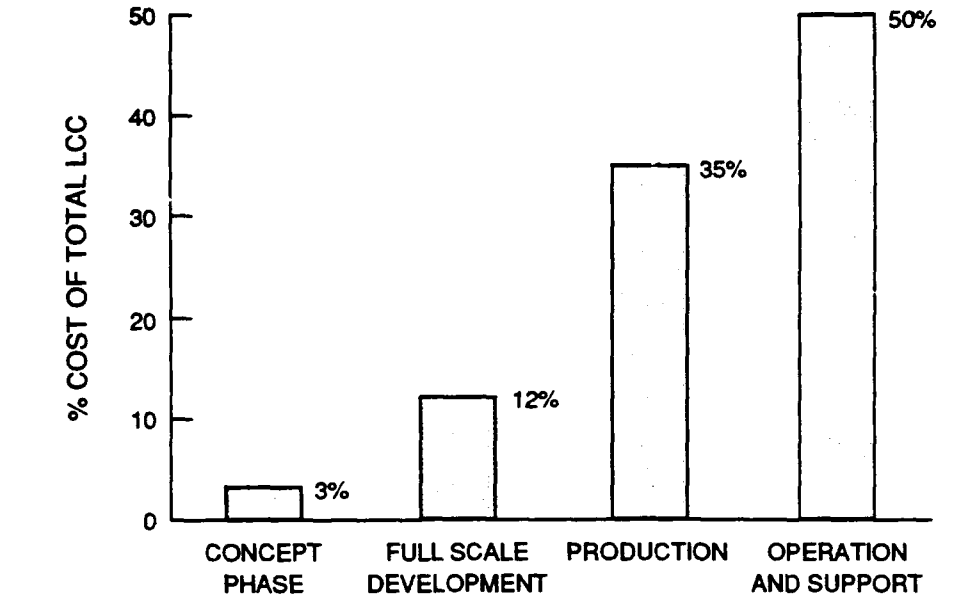


Figure 4-29. Life Cycle Costs Expended per Program Phase

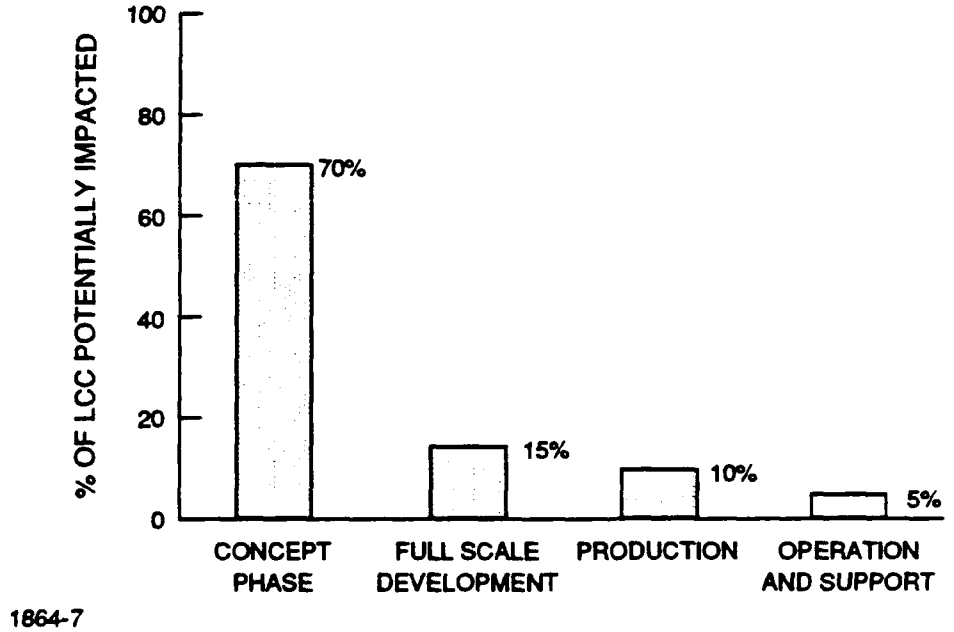


Figure 4-30. Potential to Affect Life Cycle Costs per Program Phase

- Boundary scan guidelines
  - Include an introduction to structured testability including:
    - Full internal scan
    - Level Sensitive Scan Design (LSSD)
    - IEEE Std. 1149.1 boundary scan.
  - Require the use of IEEE Std. 1149.1 Test Access Port (TAP) and Boundary Scan.
  - Comprehend when and where to use boundary scan.
- BIST Guidelines
  - Include an introduction to BIST including:
    - Pseudo Random Pattern Generation (PRPG)
    - Parallel Signature Analysis (PSA).
  - Define the minimum acceptable level of BIST in ASICs.
  - Require the use of the IEEE Std. 1149.1 TAP as the access to the BIST.
  - Define the methodology for proving the compliance with the minimum BIST level.
- General Guidelines
  - Define the key digital ad-hoc techniques that will be required.
  - Define the key analog ad-hoc techniques that will be required.

A sample of ad-hoc DFT guidelines are included later in this section, described as the methodology currently in place at GE.

The following are examples of specific items that apply to MCMs and should be included in a DFT guideline:

DFT GUIDELINE

SPECIFIC MCM REQUIREMENTS:

- Methodology Guidelines
  - Test pads on the surface of the HDI interconnect may be used up to 200 MHz without noise analysis on a standard 2-inch by 2-inch substrate.
  - Access to lower level test structures should be available.
  - Software should be modular to allow selection for the next level of test.
- Boundary Scan Guidelines
  - IEEE 1149.1 boundary scan on all ASICs
  - IEEE 1149.1 boundary scan on all transceivers
  - IEEE 1149.1 boundary scan on all microprocessors
- BIST Guidelines
  - BIST in all ASICs for 98% fault detection
  - BIST for all memory cells
- General Guidelines
  - No unbroken feedback loops
  - No sequential chains, ie., counters, longer than 8 bits
  - No monostable circuits, ie., one-shots

- Initialization of all nodes with few clock cycles
- Partition logic function and families, if possible
- Internal monitoring of all critical analog signals (either comparators or analog to digital converters).

The following design and test methodologies are currently in place at GE.

1. A preliminary design review will be held with the customer to determine the approach to be used in the design. It will include:

   - Obtain:
     - schematics
     - block diagrams
     - pin-out
     - footprint, outline
     - module attach/lead attach plan
     - die technology, size, ratings, expected yields
     - other components size, ratings
     - clock speeds, rise time tolerances, skew
     - ambient specifications: storage, operation
     - cooling available

   - Assess Testability:
     - reset all logic to know states
     - external clocks
     - boundary scan in chips
     - built in test
     - built in controllability/observability
     - die test plan, test vectors, test program
     - module test plan, test vectors, test program
     - internal nodes brought out to module pads, package pads.

2. An analysis will be carried out to determine whether the chips to be included in the HDI module will be pretested or not. Factors to consider:

   - Number of chips total
   - Chip yield data
   - Process yield of chips
   - Cost of chips
   - Interconnect yield
   - Fault coverage of the functional test vector set for HDI opens and shorts
   - Fault isolation capability of the fault isolation test vector set to isolate specific failed chip.

Chips will be pretested if the predicted module yield from the first fabrication cycle is less than 0.7 and the chip cost is such that failed modules may not be discarded.

Chip test vectors will be developed by the chip designer. GE has developed a chip carrier and interconnect for the chips to be tested, if required. The chip designer will have the chips tested at operating speed, with optional burn-in, and return the tested chips with their corresponding data to GE for disassembly and inventory.

3. Every interconnect fabricated at GE will undergo the following inspection procedures:

   - Visual inspection of every interconnect layer after fabrication to determine that interconnect is complete and there are no shorts. Every pad may be tested to determine that there are no shorts between pads. Tools: Dracula to extract those pads having lines close enough together such that a potential short could occur. The roving probe tester to detect shorts between potentially shorted lines.

4. Every interconnect fabricated will undergo a test using an open/shorts and functional test vector set. Those passing the functional test vector set will be delivered to the customer without further testing. Those interconnects not passing the functional test vector set will be tested using the fault isolation test vector set whether the units are to be repaired or scrapped. The results of the fault isolation test vector set will be used for process control and for design improvement.

The test methodology currently used at GE for HDI module testing is based to a large extent on ad-hoc test approaches coupled with good design for testability. This is based on the fact that only a small portion of HDI projects undertaken to date are specifically designed for testability or for MCMs. However, to make the MCM design testable and stay within the test budget constraints, the following ad-hoc test methods are being employed:

- All signal busses have to be tristatable.
- Device and bus control lines have to be accessible as MCM primary IOs or as MCM test pads.
- No control lines may be "hard-wired".
- MCM internally generated clocks have to be controlled by external signals and clock inputs have to be available at the MCM perimeter.
- Where applicable boundary scan will be used.
- Simple buffer ICs should be replaced by buffers with boundary scan, e.g., SN54LS373 by SN54BCT8323, etc.
- To aid fault isolation buffers should be inserted between functionally separate portions of the design.
- To improve yield, redundant components should be added where applicable.

The purpose of the above test approach is to enable testing and fault isolation of existing designs with no impact on the MCM functional performance while generating modular test sets that allow a comprehensive test of the MCM and its individual components.

The ad-hoc test approach is supplemented with a full functional vector set generation capability for designs consisting of memories and associated buffers which allow fault isolation to the component I/Os, the HDI interconnect, and ICs themselves. Although a fault coverage number cannot be generated, since full functional models do not exist for the devices, a comprehensive functional test can be generated.

The testing of the unpackaged MCM is being performed to ascertain the functionality of the MCM and reject the faulty parts for repair. The tests performed are a visual inspection for obvious damage, as well as electrical tests. These electrical tests are the same acceptance test of the packaged MCM as well as a fault isolation test in case repair is necessary. In addition, inprocess testing and inspection is available for further testing of the MCM components. This, however, should only be exercised on random samples or prototypes.

The test vector set is typically developed by the customer. The one exception being that a memory module is being built, or that portions of the MCM are partitioned into memory groups and their I/O are available for testing. In this case, the test vectors can be developed in-house without the need for a full gate model and an integrated CAD, CIM, and CAT system.

TI's DSEG has an infrastructure in place to support DFT in major programs. The Test Technology Center (TTC) and Lab within DSEG are the focal points for development of IEEE 1149.1 boundary scan technology and DFT methodology, as well as TI's ASSET system. DFT training is available from the TTC through TI's Regional Technology Centers.

4.4.3.1.2 CAE/CAD Design Rules. The following examples are the types of CAE/CAD rules that need to be generated and included in the design guides. Test points may be created on the top layer or brought out to the MCM I/O if pins are available. Any long runs on a module running at or above 200 MHz should be evaluated for noise, crosstalk, impedance, and stub effects.

Test pads on the top layer need to have spacing and area defined based on current probe technology.

The placement of power and ground layers needs to be considered if test points are to be used on the top layer. Placing power and ground on the bottom layers facilitates routing signal on the upper layers and access to test points.

Similar conditions need to be generated and incorporated into the DFT guidelines for the foundry as a function of MCM speed, die count, package size, power requirements, etc.

The University of Arizona noise analysis tool, currently included in HYPACK at GE, is capable of evaluating test points and pads for noise contribution. This type of tool should be used to help determine the feasibility of test routing and pads.

4.4.3.1.3 Customer Interfaces. The basis for customer interfaces is to reduce the time required to capture the design information. The design includes the schematic, net list, parts list, layout, and simulation information for go no/go and diagnostic testing.

The Electronic Design Interchange Format (EDIF) is one of the promising ways to communicate between companies. This ANSI standard currently incorporates schematic, netlist, and IC information. Technical subcommittees are currently working on the representation of test patterns, boundary scan, fault diagnostics, and test flow for future consideration into the standard. These improvements will be required before the standard will be useful in the test area and could be ready about 1993. The issue then becomes one of incorporation into tools after that date.

One current method of interface would be with third party translation software similar to that available from Test Systems Strategies, Inc (TSSI). Test vectors generated for go no/go testing can be translated to major test systems or to ASCII format for further translation. This method is widely used, even for communication between different systems in-house. These third party translators would also offer translation to EDIF.

Translation of the net list and fault dictionary information from a fault simulator is not as common as translation of go no/go vectors from a design simulator, and largely depends on the capability of the test system. In the absence of MCM software models, interconnect faults can be tested and fault dictionaries generated by hardware models. This method can also be used to verify the test vectors. In the future, VHDL will be the mechanism to allow software models to be transferred between platforms in the early 1990's.

Vectors translators are available today, such as from TSSI and others. However, the ability to perform fault isolation testing in addition to the more common go no/go testing depends largely on the capability of the ATE to branch or loop to the relevant sections of vector code. Current ATE systems are in their infancy to provide these capabilities. Future enhancements will simplify both the hardware and software aspects.

4.4.3.1.4 Incoming Die. The graph in Figure 4-31, shows the impact of die yield on final test yield. The graph includes information for final test yields of MCMs with 8, 20, and 36 die.

There are two ways to analyze the information shown. The first way is to pick a value of die yield to determine the final test yield. 95% die yield will give a final test yield range of 15% to 65%, depending on the number of die in the MCM. This is obviously not adequate for a volume manufacturing facility. The second way is to pick a final test yield desired, and determine the die yield required. If a final test yield of 97% is desired, the inset box will need to be used for an accurate result. The graph shows that die yield must be between 99.6% and 99.9%, or about 1000 to 4000 ppm, to achieve the final test yield of 97%.

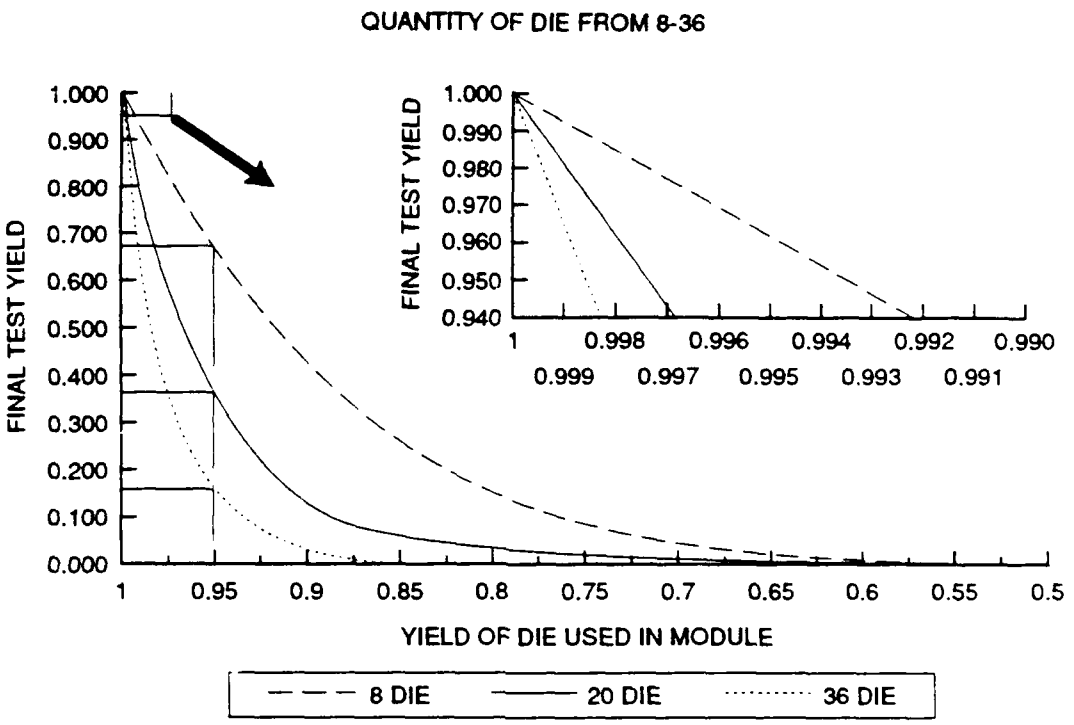


Figure 4-31. Effect of Die Yield on Final Test Yield

This is the range of die yield required for an acceptable final test yield for volume manufacturing. This will require that the incoming test strategy include tests to ensure the highest possible die quality.

Die could be received from a wide variety of manufacturers. Each manufacturer has a unique strategy for testing die at probe and at assembly. These facts show the requirement for a flexible strategy for receiving bare die from potential manufacturers and for in-house testing.

The majority of the die used in MCMs will most likely be large ASICs, microprocessors, memories, etc. Large, expensive devices are tested with more functionality than the lower cost, high volume products, and that there is a trend toward increased testing at the probe level. The major emphasis on incoming die needs to be on working with the die vendors to continue the trend toward improved testing at probe. As the IC technology used becomes more mature, the test effort can be reduced by either lower speed testing, reduced functional tests, or both.

Preliminary work at Sandia National Laboratory (SNL) and GE shows that correlation is possible between high speed package testing and lower speed testing at probe. For modules with 10-20 die, such a pre-testing correlation can equate to no need of extensive separated die testing. In fact the wafer manufacturer could perform the necessary screening at little extra cost. To convince the wafer vendors of the efficiency of such an approach, it is necessary to gather statistics on several design types (RAM, processor, random logic) and

technologies. Optimal quick test methodologies should be tried. Correlation of module yields to probe yield should also be studied.

There will always be a portion of the delivered die that is not adequately tested by the manufacturer. These devices will either be tested at incoming inspection, or be evaluated after assembly. This decision will be based on economics. There will, most likely, be a combination of test strategies performed on the die in any one MCM design. Therefore, some die may be adequately tested at the manufacturer, some tested in house, and some not tested until after MCM assembly due to their high reliability.

Currently a thorough visual inspection is being performed at GE to screen the devices for scratches and other failures that may happen during or after sawing as well as during packing and shipment. MIL-STD-883 Method 2008, is being used as a guideline for acceptance or rejection of components. Critical areas of investigation are: a) die pads for wafer level probe test damage, b) chipping due to sawing or handling, scratches on the device surface that penetrate the passivation layer, and d) other visual failures. Experience shows that, on average, some 30% of all components inspected fail the acceptance criteria with current vendor inspection.

Test interface methods for bare die needs to be addressed further. Both SNL and GE central research and development (GE) have been looking into new interface methods.

Since the MCM yield is exponentially dependent on the number of die placed, MCMs that involve 10 or more die may require more extensive pretesting of die than would normally occur at wafer probe. The first option should be a higher speed, duration, and temperature enhanced wafer probe (with the cooperation of the foundry). Thus, the ability to temporarily package the die individually, extensively test them at frequency and temperature, and return them to naked die is a needed process.

GE has developed temporary packaging methods that involve the high density interconnect (HDI) process. These methods are described in a paper titled "Bare Chip Test Techniques for Multichip Modules", authored by R.A. Fillion, R.J. Wojnarowski, and W. Daum. A brief description of these techniques follows.

a. A protective overcoat is applied to the chip to be tested. New pads are created on top of the overcoat and connected to the chip pad using laser drill and patterning techniques. The new pads can either be probed while in the holding substrate, or used to bond out the chip to an individual IC package. The original pads have minimal contact, and can be reused upon removal of the protective overcoat. This method would be applicable to ASIC devices that need burn-in or can be returned to the manufacturer in the package for full testing.

b. The standard HDI overlay process can be used to create an array of memory devices in a single "test substrate". They could be connected as a memory

bank for typical testing or burn-in. The HDI overlay can be removed, and the devices recovered.

c. A similar technique to the one above would create a test layer on the actual "product substrate". The connection would allow test points and interconnections to enhance testability. The temporary layer could be removed after testing is complete.

Another approach to temporary packaging has been carried through feasibility studies by Sandia. In this approach, the die are temporarily attached to a package with either low temperature thermo plastic or an easily solvent dissolved polymer. Then, the bond pads are connected with a standard wire bonder adjusted to provide low bond strength loops. The package lids are tacked on rather than hermetically attached simply to provide mechanical protection. After testing, the die are easily removed with little handling degradation. This process is labor intensive. Simple electroless plating solution for the pads and/or wire are being considered to allow chemical removal of the bond wire and lessen the damage to the pads. This method, however, may not be acceptable in military applications due to "rework" on the IC bond pads.

The final analysis for the incoming die test strategy indicates that a flexible program needs to be in place to accommodate different die vendors, combinations of die in each MCM, cost of die, cost of die test, and cost of rework on an individual MCM design basis. Emphasis will be placed on working with the IC manufacturers to improve testing at probe.

4.4.3.1.5 Data Collection. Data needs to be collected from the manufacturing test floor for failure analysis, effectiveness of tests, and statistical process control (SPC). Information can be utilized for troubleshooting various problems with the equipment, process, and components. This system should be tied in to the foundry communications network that will handle tracking of products and design data. This will allow the test engineer to access current information from his desk. A high level of collected data accuracy and real time data manipulation will allow reduced problem identification time and increased factory control.

4.4.3.2 Specialized Testability Components Cost Versus Benefit

4.4.3.2.1 Specialized Environmental Test Components. There is a need to objectively, quantitatively measure and compare the aging, thermal, mechanical, and electrical properties of an MCM technology. Some of the data can be collected with an inexpensive set of Assembly Test die including an electrical metrology test chip.

The electrical test chip will have high frequency sources, attenuators, amplitude to digital output, RF inputs and outputs, cross talk, and reflection detection. This chip could have a ring oscillator in four segments, so the MCM interconnections can be used to piece together the ring oscillator. This would be a good check of the RF properties of the interconnect. With on-chip amplitude-to-digital detection, attenuation studies could be performed by passing RF signals between chips. Using the same circuitry, cross talk between internal

MCM lines could be measured. Variable frequency oscillators would allow studies as a function of frequency.

Thermal management and environmental aging test chips are available in quantity from Sandia National Labs and from Texas Instruments. A mechanical stress test chip will soon be out of wafer fab at Sandia. No RF/DC metrology test chip is commercially available.

4.4.3.2.2 Reliability. The addition of specialized testability components to operational MCMs will have a minimal impact on both the initial yield of the MCMs and the longer term reliability of the MCMs. The approach used to evaluate this impact will be to analyze the predicted yield of an MCM with and without specialized testability components. The analysis included evaluating the impact with fully burned-in parts and parts that have not been burned-in (B/I). This will allow a comparison of the impact on initial yields and the impact on the longer term reliability of the MCMs. MIL-STD-217E was used to estimate the failure rates of the IC. It is conservative when applied to bare die. Failures in time (FIT), is the term used in MIL-STD-217E to describe the reliability of components.

The following is a list of components and critical data for the baseline MCM:

IC	QTY	# OF GATES	217E FAILURE RATE
0.8 Micron CMOS	1	142k	0.832 Kfits
0.8 Micron CMOS	6	32k	0.416 Kfits
0.8 Micron CMOS	1	110k	0.832 Kfits
MIPS R4000	1	120k	0.156 Kfits
SRAM 16k x 9	16		0.520 Kfits
Clock Buffer	1	80	0.013 Kfits

The following are the specialized testability components that would be added to the MCM to provide access to internal nodes:

IC	QTY	# OF GATES	217E FAILURE RATE
1.2 Micron CMOS	1	2k	0.052 Kfits
BICMOS Scan	15	1k	0.078 Kfits

Based on the given conditions it is possible to calculate the estimated delta percentage of failures with and without testability components during the first 168 hours of operation for the MCM. For the baseline MCM with specialized testability components added, it is estimated that a delta of 1.4% of the MCMs would fail in the first 168 hours over the baseline design.

The failure rate was then calculated based on using ICs that had been burned in for 168 hours at 125°C. This calculation was done to estimate the longer term reliability impact of adding specialized testability components to MCMs. For the baseline MCM with specialized testability components added, it is estimated that a delta of 0.1% of the MCMs would fail in the first 1000 hours.

The small delta in the yield between the baseline MCM and the MCM with specialized testability components is due to the fact that the majority of the failures will be as a result of the baseline components and not due to the testability components.

Calculations were done on two other versions of the above baseline design to evaluate the effects of adding testability. BIST and scan were added on the existing ICs, and the gate count and reliability number were adjusted to reflect the change. The chart below shows a summary of all the findings, in delta % from baseline design.

	MCM Yield Delta No B/I	MCM Yield Delta With IC B/I
Baseline design	0.0	0.0
Baseline + scan	0.1	0.0
Baseline + scan + BIST	0.1	0.0
Baseline + scan ICs	1.4	0.1

The largest delta is when adding additional ICs as shown in the above example. Adding silicon structures on the existing devices has little effect on reliability, and is well worth the gain in ability to diagnose problems.

4.4.3.2.3 Performance. The performance impact of testability on an MCM is dependent on the technology (CMOS, TTL, etc.) that is implemented. Typical testability functions require both controllability and observability. The performance impact for controllability is typically two gate delays, while the impact of observability is typically one additional load. Some examples of known performance impacts for testability functions are shown below.

- BOUNDARY SCAN - 2g delay (mux) per I/O pin, some control and enable signals for bi-directs
- DIGITAL WRAP - 2g delay or (1g delay and 1 load) depending on implementation
- DIGITAL READBACK - 1 additional load per signal
- CLK MUX - Assuming a synchronous design, no performance impact since all logic is affected the same; 2 gate phase delay on clock signal; may introduce greater clock skew between MCMs depending on implementation.
- BIST - Inject/capture requires 2 gate delay & 1 load per signal

Most products can be designed with sufficient margin to allow the delays and loading described. MCM packaging techniques will reduce these effects to a degree.

4.4.3.2.4 Cost. Typical percentages, often applied to the cost of testability in the past, are no longer sufficient. The cost of test for large designs will be dependent upon design complex-

ity, the level of fault detection and isolation to be achieved, number of design iterations, etc. The variation in the silicon area required by testability ranged from 1.3% to 13% on several TI designs for military systems.

Some of the detailed factors contributing to test cost are:

- Engineering design time - reduced by using modular test functions
- Gate count - generally increases for testability
- Test vector development - generally reduced, some areas increase
- Control/observation access - minimal impact on cost
- Imbedded test execution - increased impact on cost
- Reduced test time in factory needed - reduces amount of test equipment

Some areas that allow reduced cost are:

- Utilize existing logic to perform the required test function(s).
- Understand the reason for each test function and each test. Understand what the requirements/needs are and the likely failure modes.
- Basic testability can often be achieved through good design practices.
- As density of ASICs increase, % impact of testability functions will be reduced, due to boundary scan being largely based on I/O.

4.4.3.3 Possible Extensions to IEEE 1149.1 and Feasibility

4.4.3.3.1 BIST. A method of initiating and executing IC level BIST is detailed in the IEEE 1149.1 standard specification. The 1149.1 standard does not attempt to standardize IC BIST techniques, but rather it describes the process whereby an application specific BIST methodology can be started and stopped under control of the 1149.1 four-wire test bus. While most IC BIST methods are aimed at testing the interior logic of an IC, TI has developed boundary BIST capabilities targeted at testing exterior logic on a board or common substrate. TI's exterior BIST method has been proven in TI's SCOPE octal test components and provides for psuedorandom, binary count up/down, or toggling patterns to be generated and output from IC output boundary pins, while the IC input boundary pins sample or compress incoming signal data. The advantage of TI's external boundary BIST over external boundary scan is the ability to test the interconnects and or combination logic residing between ICs on the board or common substrate at-speed. At-speed boundary BIST testing enables testing for timing sensitive interconnectivity faults between ICs.

4.4.3.3.2 Other Possible Extensions and Techniques. In MCM technology, functional testing can be accomplished by allowing the multiple ICs on the substrate to operate a function while test circuitry monitors the functional operation and determines whether it passed or failed. The test circuitry can be incorporated on the MCM as either external test components or as part of the functional ICs. Compaction test circuitry can be designed into

each ICs input and output boundary to allow taking signatures of the I/O transactions between ICs during normal operation. Control and qualification test circuitry is required to enable the compaction circuitry during normal operation of the functional IC logic.

TI has developed an IC level event qualification architecture that provides qualification and control when boundary resident compaction test circuits are enabled. Using event qualification, boundary test circuitry resident in multiple ICs on an MCM can be enabled during functional operation of the MCM to collect functional signature of the transactions between multiple ICs. Access to setup the test and extract the test signatures is accomplished via the IEEE 1149.1 test bus.

The advantage of including event qualification in MCMs is that it provides an embedded at-speed test approach to verify correct at-speed interactions between ICs without having to resort to using external functional test equipment and probing mechanisms, and reduces the cost of functionally testing MCMs. Also, since the test logic is embedded into the ICs of the MCM, no abnormal loading effect is present during testing.

All of the ICs and methods in this section on IEEE 1149.1 extensions should be evaluated by the MCM designer for enhancing testability. The impact of these few basic functions that can be imbedded in a design, can have a great impact on detection and isolation of faults in an MCM.

4.4.3.4 Use of IEEE 1149.1 for In-Process Test and Burn-In. The use of IEEE 1149.1 boundary scan techniques as the basis for the burn-in monitoring strategy and the manufacturing defects strategy is becoming possible as the IEEE standard becomes accepted. This acceptance will cause component manufactures, especially large ASICs and microprocessors, to incorporate scan. The following ASIC vendors have IEEE 1149.1 boundary scan cells in their library: VTI, LSI, TI, Harris, and NCR. Xilinx will offer scanable FPGAs in 1991. The following microprocessors have been described as going to have IEEE 1149.1 compliant boundary scan: C40, C50, 68040, and R4000. Several test equipment vendors have announced ATE products that support or aid in the use of scan testing. These include Teradyne, Schlumberger, GenRad, HP, and IMS, as well as TI's ASSET™ test and emulation system. A system, for both burn-in and manufacturing defects testing, can be developed from current hardware, however, that will interface to, and exercise, the MCM at a much lower cost by reducing the number of connections to the MCM required for testing.

100% scan of a unit under test is not required. All assemblies with a combination of scan and non-scan components will benefit to the degree of additional access available.

Two areas exist that will continue to be a problem for any MCM assembly, due to limited access; 1) shorts 2) catastrophic failures. Observability of shorts is limited as the entire node is pulled down with no means of detecting the location along the node that is shorted. Shorts can also be in the IC, especially at the I/O. One solution is to develop a current monitor for ICs that will output a failure indication via the boundary scan bus. Failures in the boundary scan chain are currently detectable with a standard response when

selected. GE has developed a method of verifying opens, shorts, and vias on prototypes by probing assembly layers, and making a temporary pattern on the top layer for later interconnection. Other solutions are needed to detect shorts and catastrophic failures, such as automated thermal imaging techniques.

Performing manufacturing defects testing and burn-in monitoring can be approached three ways:

- Using IEEE Std. 1149.1 boundary scan for exercising bare die and/or assembled MCMs during burn-in and as the primary access to the UUT during manufacturing defects test of the assembled MCMs
- Using built-in self-test hardware (BIST) and/or built-in test software (BIT) to test the status of the parts during burn-in and perform the manufacturing defects test
- Using conventional, edge connected, pattern based, functional tests to monitor the status of the parts during burn-in and perform the manufacturing defects tests

The preferred approach is the use of IEEE Std. 1149.1 boundary scan.

UUT REQUIREMENTS: In order to use one of the approaches defined above, the UUT must meet the following requirements:

a. To use boundary scan as the vehicle for burn-in monitoring and manufacturing defects testing, the MCMs must have IEEE 1149.1 boundary scan on a majority of the non-memory components. The scan path configuration may be a star configuration, a ring configuration, or a hybrid with both star and ring attributes. Embedded scanable ICs, ie., TI's octals, may be used to supplement MCM designs where the level of scan accessibility is not adequate. Memory in the MCMs must either be addressed by an on module processor or have its address, data, and control lines available at the MCM I/O.

b. To use BIST as the technique for burn-in monitoring and manufacturing defects testing, the MCMs must have some form of BIST at the MCM level) that covers the interconnection structure between the ICs, as well as BIST within the ICs that tests the IC functions.

c. To use BIT as the technique for burn-in monitoring and manufacturing defects testing, the MCMs must contain some form of processor (microprocessor or digital signal processor) through which BIT code is executed to test the functionality of the MCM. The BIT technique is probably only feasible at the MCM level.

d. To use the conventional functional test approach to burn-in monitoring and manufacturing defects testing, the IC and/or MCM must have a high degree of design-for-testability built in. Without this testability the non-recurring cost of developing the tests and recurring cost of applying the tests would be too high.

The test systems for burn-in and manufacturing defects testing of MCMs will be built with common functions due to similar test interfaces and functions used to test the MCM. The following is a baseline estimate for configuring the test system.

TEST SYSTEM HARDWARE REQUIREMENTS: The system will be based on instrument on a card technology integrated into a VXI chassis.

The instrument hardware should have the following features:

- The IEEE 1149.1 controller should be a standard B size, single slot VXI test instrument.
- IEEE 1149.1 scan interface connector on the front panel
- Resyncronizing electronics mounted in an external pod, such that it can easily be installed in multiple test fixtures
- Support both ring and star configurations
- Control/monitor at least two rings in the ring configuration
- Control/monitor at least ten nodes in the star configuration
- Control/monitor multiple UUTs simultaneously
- Support burst mode including sending data to the UUT, receiving data from the UUT, and verifying the received data with a minimum of 64K bits of serial data
- Operate at a minimum of 25-MHz clock and data rates in the burst mode
- Integrated with a 192-pin, 1-MHz, digital section, for emulating buses, and for handling standard vector patterns.

TEST SYSTEM SOFTWARE REQUIREMENTS: The system should include embedded ASSET software based on Intel 80X86-MS/DOS code.

The system software should have the following features:

- ATPG of scan patterns for scan path integrity testing

- ATPG of scan patterns for structural interconnect testing
- Graphical display of schematics and module topology for aiding the operator in diagnostics
- Interactive debug modes to aid the operator in diagnostics
- Virtual guided probe system to back trace errors from the module's principle outputs to the faulty component via the scan path
- IEEE 1149.5 TM-bus control software
- IEEE 1149.1 bus analyzer/event qualification software
- Fault dictionary which operates in the following modes:
  - Module level conventional fault dictionary with decision tree based upon the module's principle outputs
  - Module level fault dictionary with decision tree based upon the module's virtual outputs (scan outputs)
  - Cluster level fault dictionary with decision tree based upon the module's virtual outputs
  - Hybrid fault dictionary with decision tree based upon the module's principle outputs and virtual outputs which is integrated with the virtual guided probe system to enhance the guidance algorithm.

4.4.3.5 Feasibility and Requirements of Potential BIST Structures. BIST will be a major contributor to successful dynamic performance testing of the multichip modules. The incorporation of BIST structures as key elements of the MCM design will support the hierarchical test methodology required for future success in MCM procurement.

Incorporation of BIST is a design issue, as opposed to an MCM foundry issue. Because of this, it must be incorporated by the customer during functional circuit design. Due to the complexity and diversity of the expected MCMs, standard BIST architectures will need to be developed to decrease up-front design time for testability. Since it is expected that the majority of die will be VLSI components (ASIC, microprocessors, etc.) and memory, the BIST architectures will apply to the use of these components.

BIST will be implemented within MCMs in two ways, depending upon the product type and associated MCM design constraints.

- Implement BIST structures into ASIC or custom components

- Surround appropriate clusters of components with test components containing the necessary BIST structures.

Implementing BIST structures within ASIC or custom components should have the least impact on the MCM design. The addition of dedicated test components to the MCM will be more costly in terms of design capacity. The addition of test components containing BIST structures must be addressed since many different combinations of ASIC and off-the-shelf die may be included in the MCM.

BIST can be classified as "Off-line" or "Continuous". The type of BIST applied to MCM components will vary depending upon the design and the functions to be tested.

Off-line BIST requires that the component(s) under test be taken off-line from their normal functional operation to perform testing. It is an exhaustive test, possibly testing multiple functions. It is intrusive to component operations and typically does not leave the component in the same state it was in prior to test execution. Off-line BIST may execute autonomously or require external control.

An autonomous BIST is completely self-contained. No external inputs are required except for test initiation. During execution, the device's outputs are disabled so that its self-test operations do not affect the operation of external devices.

Externally controlled BIST is not self-supporting. It requires external support for tests to execute. BIST initialization, execution and evaluation are all controlled by external equipment (usually via a scan path interface). The BIST structures within the device are limited to stimulus generation and response comparison/compression. Typical examples of components supporting externally controlled BIST are the TI SCOPE™ octal devices.

Off-line BIST is the most applicable to MCM final test in the foundry. While autonomous execution is the most desirable, design tradeoffs will determine the feasibility between autonomous BIST and externally controlled BIST for each MCM.

Off-line BIST may perform structural tests and/or functional tests of the circuit design. Structural tests imply pattern specific tests which detect logical operation of the circuit elements and their interconnections. Functional tests do not necessarily verify complete logical operations of the circuit; they verify the function performs as it was intended. A functional test, for example, might be an interface wrap-around test using a predefined set of test patterns to verify the operation of an interface's input and output logic blocks.

The use of BIST for interconnect testing via boundary scan has also been discussed. BIST is less likely to be beneficial for MCM interconnect testing assuming that boundary scan has been applied to the MCM components and is accessible by the MCM tester. The number of nets within the MCM is expected to be too high (1000+ nets) to allow a feasible interconnect self-test to be embedded within the MCM. The test can be greatly improved by taking advantage of both BIST and boundary scan functions.

Continuous BIST is a form of continuous self-test which executes in background within the circuit under test. This form of BIST is non-intrusive to component operation and executes continuously checking for invalid circuit operations.

Continuous BIST provides increased dynamic fault detection capabilities for the fielded product. It should be incorporated whenever possible to support the hierarchical test methodology. It will be useful for MCM testing at the foundry during burn-in.

4.4.3.5.1 Current Methods

BIST Functions

BIST consists of three required functions. These functions are stimulus generation, response comparison and test control. As a minimum, MCMs should have stimulus generation and response comparison functions embedded. Test control should be embedded wherever feasible.

The test control function controls execution of the test (such as starting, stopping, stimulus selection, response technique selection, etc.) by manipulating the stimulus generation and response comparison functions. It also provides the test/device pass/fail determination. Test control must be embedded when implementing continuous BIST. This form of BIST relies on the circuit under test to generate a predictable stimulus.

Stimulus generation may be provided in several ways. Typical methods include random or pseudo-random pattern generation using linear feedback shift registers, hardwired or fixed test patterns, and algorithmically generated stimulus. Different techniques are required for the various functions within a device. Embedded memory is easily tested with algorthimically generated stimulus and canned test patterns while simple combinatorial logic is easily testable with pseudo-random patterns.

Response comparison may be provided through direct comparison of response data with known good results at specific intervals or through compression/compaction of the data. Compression of data results in signatures for the logic under test which can be compared against known good signatures determined during logic simulation. Compaction of data allows a large amount of data to be converted into a reduced format, making fewer data comparisons during analysis.

Traditional BIST Structures

Design structures have been developed over the years which are directly applicable to the implementation of BIST of MCMs. These structures typically aid in the pattern generation or response comparison/compression capabilities. Some techniques include:

Self-Checking Logic: Self-checking logic structures are often implemented using parity trees, special decoding logic, and error correcting codes to monitor correct operation of a circuit. Parity is often added to programmable logic array (PLA)

structures to detect faults in combinational networks or state machines using these structures. Special decoding logic may include determining that a logic structure has a unique number of active outputs, or a specific state is never acquired by a state machine (illegal inputs, etc.).

Redundant Logic: Redundant logic structures are often utilized to indicate proper operation of a circuit. This is sometimes called shadow processing. The redundant logic operates in the same manner as the circuit that it shadows but its output is disabled so long as the shadowed circuit is functional. The outputs of multiple redundant circuits are compared to deduce proper circuit operation (voting).

Scan Design: Scan path building blocks provide the basis for the controllability and observability. Examples of scan architectures are IEEE 1149.1 Boundary Scan Cells and Level Sensitive Scan Design Shift Register Latchs (SRL).

Linear Feedback Shift Registers (LFSR): LFSR registers are hardware implementations of prime polynomial division. The output from such division results in a pseudo-random pattern generation.

Built-In-Logic-Block-Observer (BILBO) Registers: BILBO is a configurable LFSR structure supporting both pseudorandom pattern generation and signature analysis.

Multiple Input Signature Register (MISR): A MISR is often used for parallel data compression. It is an LFSR having multiple parallel inputs and configured to support parallel signature analysis.

Example BIST Applications

TI has developed built-in self-test for a number of ASIC components and board-level designs. A brief list is shown below.

BIST Function	Component(s) or Board(s)
RAM Tester	3D Memory Modules (Si-on-Si)
RAM/ROM Memory Tester	Signal Processor ASIC
Interface Wrap Test	1750 CMOS Chipset
Register Test	1750 CMOS Chipset
Counter Test	Signal Processor/1750 CMOS Chipset
Bus Arbiter Test	Data Processor ASIC
EDAC Test	Data Processor ASIC
Combinational PRPG/PSA	TI SCOPE™ Demonstration Boards
ALU/Multiplier Test	Vector Processor ASIC
Video Chain Signature Analyzer	Video Processor Board

MCM BIST Requirements

For BIST to be useful for MCM testing at the foundry, standard requirements must be in place regarding the external interfaces, execution control, and reporting mechanisms.

An MCM self-test may include many BIST functions which support multiple operating modes. Each BIST function on the MCM should be initiated and/or controlled via the IEEE 1149.1 interface, as well as a functional interface or discrete. It should be possible, via these interfaces, to select which BIST functions are to be activated, provide initialization data whenever necessary, initiate test execution, and gather BIST results.

Standard methods for reporting BIST results should be implemented within the MCM. Each ASIC implementing BIST should contain a BIST results register which indicates the go/no-go status of each function tested by BIST. The format and size of the BIST register should be common among devices on the MCM.

Additional results, such as signature values, data-bit-in-error, etc., should be provided if helpful in isolating failures at the MCM, board, and system levels. This information is design specific and likely cannot be standardized.

Critical errors which affect access to the BIST register should be reported via a discrete signal.

A BIST control register should be provided for autonomous BIST. This register should support initiation/activation of BIST functions. Autonomous BIST should support a mode in which BIST is forced to fail. This mode should be selected via the BIST control register. When the "forced failure" condition is enabled, any initiated/activated BIST function should return a fail status in the BIST results register. The goal of the "forced failure" mode should be to confirm the valid execution of the BIST response comparison/compression in the presence of "faulty" input data for the function being testing.

Access should be provided to autonomous BIST such that it can be aborted via the scan interface, if necessary.

MCM self-test should have access to all BIST functions via the interfaces defined above.

Feasibility

It is apparent, with the complexity and sophistication of MCMs in the future, that BIST techniques will be important in performing feasible dynamic tests of these components. MCMs will likely contain VLSI components with dynamic pattern sets in the 100,000 to 1,000,000 pattern range (per component). A TI developed MCM contains three unique ASICs with pattern sets of approximately 100k, 235k and 600k. Multiple ASICs are included on the MCM such that the total number of patterns necessary to dynamically test the MCM, testing each ASIC independently, is 2,035,000.

Dynamic testing of MCMs of the complexity envisioned, will rely heavily on the self-test capability built-in to the MCM. Generating dynamic patterns for application at the MCM I/O pins will be very difficult for MCMs containing microprocessors, memory, very large scale integrated circuits, and large application specific ICs. Scan design, though helpful in many ways, will be limited in its direct support of dynamic MCM testing.

Implementing boundary scan on components within the MCM will provide controllability and observability of internal nodes but will not allow pattern application to be performed at operational speeds. Bit application rates of approximately 25K bits/sec has been demonstrated within TI, using PC-based software driving a scan protocol generator chip. Implementing the stimulus generation and scan control in hardware may allow bit application rates to approach the speed of the IC technology. However, even if the bit application rate can be increased, there are few cases where the pattern application rate will meet the operational speeds and, thus, be useful for dynamic testing of the MCM.

BIST will allow the number of patterns required to test an MCM to be reduced. MCMs will be functionally tested using BIST from the inside out. For a TI design which incorporated BIST for embedded memory testing, it was calculated that approximately 10,240 patterns were saved and that test execution time was decreased by a factor of 5.

More and more off-the-shelf components are beginning to implement BIST. This includes microprocessors (TI 1750, Intel 80960 RISC, and Intel 80386) and interface devices (TI PI-Bus & TM-Bus, and United Technologies 1553BCRT). Several examples of BIST execution speed and gate overhead for testability are given below.

BIST OVERHEAD EXAMPLES

Component	BIST Execution	BIST Gates	% Gate Overhead
1	250 µsec	1200	10.9
2	65 µsec	1104	1.3
3	n/a	1000	5.4

4.4.3.5.2 Enhancements

BIST Design Macros

A major thrust in the future of BIST will be in the design of modular BIST macros that can be "dropped-in" for specific BIST functions. Such macros have already been created for scan path functions. TI has developed ASIC macrocells supporting externally controlled BIST, as described in paragraph 4.4.3.3.1, and has implemented these in several designs. Just as with scan path design in the past, the incorporation of BIST will impose requirements on the circuit design in order for the macros to be utilized.

While BIST methods will always have some design specific aspects, it is possible to standardize some of the functions which are used in implementing a BIST. Stimulus generation and response compression structures are fairly easy to generate by using pseudorandom pattern generators and signature analyzers. These functions are available in some testability ICs, and can be inserted as a macro into other devices. A number of test control functions can also be standardized for use in multiple applications. These include:

- Memory test controllers (RAM and ROM)
- Counter/Timer test controllers
- Combinational logic test controllers
- Interface test controllers

Standardized Control Structures

High-speed control structures based on programmable ring oscillators need to be developed. Such structures are necessary to decrease BIST execution time and to increase the feasibility for using scan-based testing for low-to-medium frequency dynamic testing. The execution speed of BIST is especially critical for scan-based testing and memory testing. TI has experimented with the use of ring oscillators in BIST; in one test case, a 35% improvement in test execution speed was measured for a standard cell CMOS design. The improvement is technology and design dependent. Further study needs to be done to evaluate other technologies and design types.

Compaction/DeCompaction Structures

New structures for compaction and decompaction of test patterns are needed for use in autonomous BIST employing scan-based tests. Executing tests via scan currently require the storage of hundreds or thousands of test vectors. Storing these vectors on the MCM is often unreasonable for today's designs. Onboard storage may become more realistic if new compaction/decompaction techniques are developed.

Pattern Generation/Compression Structures

More efficient and less expensive stimulus generation and response compression structures need to be developed to reduce the design overhead incurred by these functions and modularize the structures. One relatively new structure is Cellular Automata (CA). CA is similar to the Linear Feedback Shift Register (LFSR) and may be used for pattern generation and compression. Though the circuit overhead is slightly higher than with the LFSR implementation, its design is much more modular.

Test Control and Scheduling

Test control and scheduling of BIST is an important part of the BIST design and is often the most design specific function. TI, through the SCOPE™ event qualification architecture, has developed ASIC macros for test control which support multiple test execution protocols. The macros are modular to allow tailoring to the exact need.

BIST Design Tools

For BIST to be readily implemented in new designs of the complexity envisioned for the MCMs, extensive growth in the area of BIST design tools is necessary. These tools are necessary to remove the burden of BIST design from the designer and allow concentration on functional design. The designer simply selects the BIST test methodology to be employed and the BIST design structures to be used. Some companies are beginning to provide such tools. VLSI Technology, Inc., provides a basic BIST design compiler. This type of tool needs to be incorporated into the foundry as part of the methodology to reduce design cycle time.

4.4.3.6 Test Enhancements for High Frequency

4.4.3.6.1 Scan Based Analog Test Circuitry. New testability structures have been designed for controllability and observability of digital signals with the advent of the IEEE 1149.1 standard and other BIST techniques, but are limited to standard moderate speed digital signals. The emerging IEEE 1149.4 extension is aimed at analog testing and will be incorporated as soon as possible.

The real requirement in the analog/RF test community is the "accurate" generation and measurement of analog signals. This breaks down into two parts, the ability to transport the signal from one point to another, with the required fidelity, and the ability to accurately generate or measure that signal. Instrumentation technology is continuing to keep pace with the test requirements through the research and development of the major instrument manufacturers, for example, by the introduction of coplanar probes, etc.

A major problem associated with the stimulation and measurement of analog signals is their potential diversity. They vary anywhere from DC, with its Kelvin connection requirement, through millimeter wave signals, with their precision impedance matching requirement. Their measurements may be as simple as measuring a voltage amplitude or as difficult as measuring complex waveform purity. Figure 4-32 shows the diversity of probes required in a sample receiver, that range from RF to video frequencies, and high power to noise floor of -100 dB.

The embedded probes and instrumentation should be akin to BIST circuitry in the digital world. Given the analog/RF circuit, a test engineer can develop probes if needed, a switching network (simple or complex), and instruments tailored to meet the requirements for embedded test. This type of ad-hoc analog testability has been down within many TI programs. In order to give it a structured approach (like digital with standard probes, network components, and instruments) the frequency domain must be standardized. D to A and A to D converters with a given conversion time and resolution may be tied to the IEEE 1149.1 bus via memory for embedded applications. These embedded instruments after being networked to the nodes-under-test would be working in a standardized frequency domain at a lower frequency. These simple embedded instruments may be sufficient, but the vast majority of the analog/RF applications require capabilities beyond embedded capabilities.

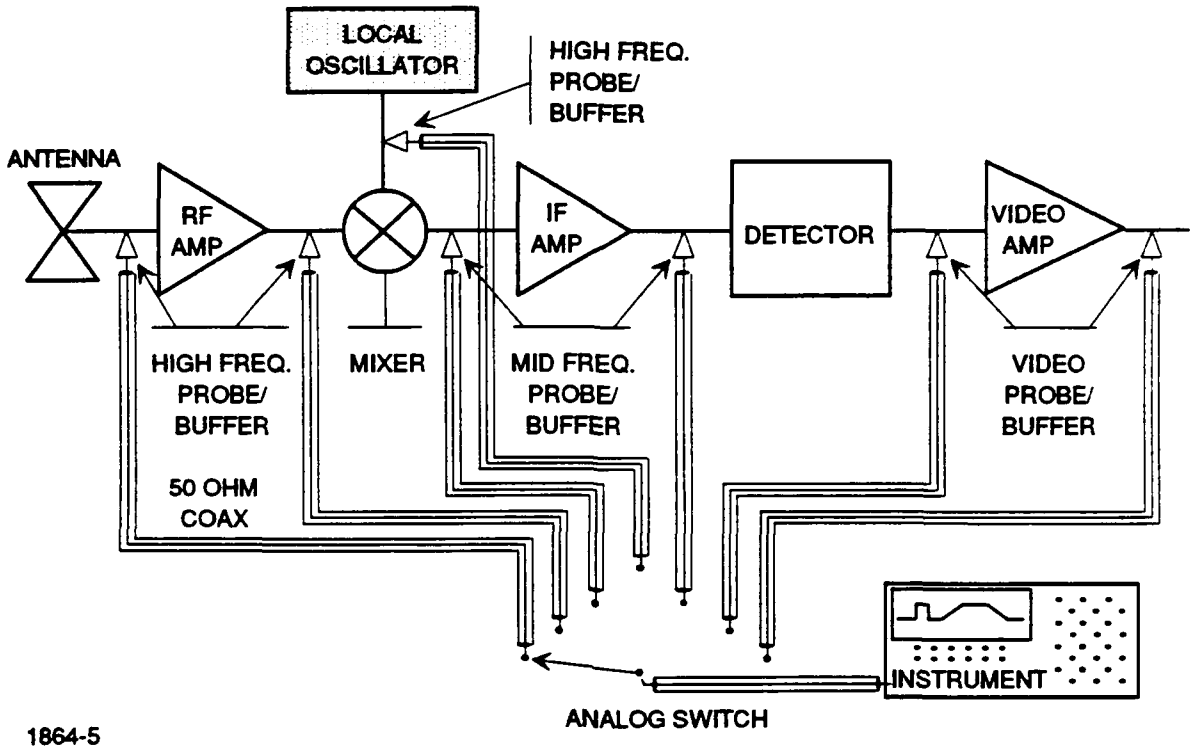


Figure 4-32. Sample Receiver and Probe Type

4.4.3.6.2 <u>High Speed Digital Enhancements</u>. The test of MCMs operating in the multi-GHz frequency range poses a tremendous challenge to the foundry due to the limited availability of adequate test equipment, the fact that devices with little or no test history will be used, and the high circuit density on the MCMs.

Due to the low device yield, the high circuit complexity, the lack of adequate test equipment, and the very high cost overhead in generating and debugging test programs, the full functional test of completed MCMs at speed may be too costly and time consuming to be a viable option. Thus, the test problem will have to be broken into several tasks, ensuring the overall functionality of the MCMs. It should also be realized that the signal speed at the inputs and outputs to the MCM will be slower than that within the MCM, since data passed between the individual MCMs cannot operate at multi-GHz speeds due to delay, latency, etc. This feature will be utilized throughout the test.

To solve the above problems, a four-tier test approach can be developed addressing the following areas:

- Device Pretest via High Speed Active Probe Interfaces
- HDI Interconnect DC Validation using Boundary Scan
- HDI Interconnect Microwave Compatibility Verification via TEG Structures
- MCM Functional Test Verification through BIST, Signature Analysis, etc., using existing automated test equipment.

The device pretest will ensure that all devices placed into the MCM will have functional inputs and outputs in addition to some functional integrity to the device. The BIST features and boundary scan cells on the individual devices will interact with fast buffer and control devices on the probe card to interface to lower-speed test equipment allowing an adequate characterization of the device to be performed.

Once the parts have been positioned in the MCM and interconnected via HDI, the structural integrity of the circuit will be tested using the IEEE 1149.1 boundary scan approach.

The high frequency integrity of the HDI interconnect can be verified using the test element groups (TEGs) on the MCM by probing with high frequency probe stations and high frequency test equipment.

The final, functional test of the MCM can be performed using lower speed automated test equipment (ATE) interfacing to the lower speed MCM inputs and outputs and exercising the MCM as required.

During the development of the test strategy and approach for multi-GHz testing, the following areas need to be addressed further:

- Probe test development, including interface pretest, HDI high frequency compatibility verification and MCM functional testing
- Boundary scan test development, including chip set additions
- BIST development
- Burn-in strategy
- Test vector generation
- Test and burn-in strategy description
- Testing of the passive design validation TEGs
- Testing of the GaAs test vehicles as active TEGs.

4.4.3.7 Hardware and Software Technology

4.4.3.7.1 Existing

4.4.3.7.1.1 Digital Pin Electronics. The two major hardware issues for MCMs are pin count and testing at speed. Current board test systems are aimed at large pin count, low speed testing and in general, are not applicable to MCM testing. The IC test systems, however, are currently at 200 to 400 MHz and 256 to 512 test pins. This is adequate for today's MCM requirements. Other manufacturers are developing digital electronics that interface to a standard card cage configuration, that will be useful for manufacturing defects testing and possible low end performance testing in the future. The high end ASIC verification type testers cost about $2500/pin, but there is a low end system from Hi-level that costs about $1000/pin. This system is limited to 110 MHz and 544 pins, but may have application for a high volume low end product. It may also prove useful for integration into the manufacturing defects tester as the digital section.

The table below shows the current features of several major test systems.

ATE Manufacturer	Frequency Range (MHz)	Max Pin Count	Vector Depth	Addresses Scan
HiLevel Topaz	50 - 110	256 - 544	66K	Y
HP 82000	50 - 400	512 - 256	1M	Y
IMS XL	100	448	64K	Y
LTX	100 - 200	512	4M	Y
Teradyne	100 - 400	512	1M	Y

4.4.3.7.1.2 Software. Some form of boundary scan interface is available on several of the IC and board testers to make use of the latest test circuitry. Other boundary scan tools are available from Alpine Image Systems and Texas Instruments. These tools can convert parallel data into the serial data and generate the protocol required for boundary scan testing. Some tools are interactive for engineering evaluation of new designs that incorporate boundary scan.

Tools are available for translation of go no/go vectors from various simulators, but the netlist and fault dictionary information are not readily translated to the desired test system. Today, Test Systems Strategies, Inc. (TSSI), the major company that supplies translation between simulators and test systems, translates diagnostic information to only two test systems. These two systems are board testers, and would not be used in a MCM foundry. Most of the tools available are for the device level, where most of the design activity is located.

4.4.3.7.1.3 Probe Technology. The interface between the die or MCM being tested and the ATE will be some form of probe. Several probe technologies will be available for use in the foundry. Each of these technologies have advantages and disadvantages. These technologies are discussed below.

Standard probe cards are available from a variety of vendors and are the most common interface between the device-under-test (DUT) and the tester. Die with pad counts up to about 200 pads can be tested in that fashion. This limitation is posed by the need to have flexible cabling between the tester and the probe card itself. As the speed of testing increases, the capacitive load imposed by the fixturing limits the test performance. In addition, burn-in and at-temperature testing is severely limited. Damage due to the sharp probe tips is also likely, such that extraordinary care needs to be taken during the IC pretest.

The die are mounted on a membrane that is stretched over a frame, thus allowing test of a large number of components with minimal additional handling. However, although the die positioning is precise, the change in both temperature and humidity results in a slight shift of the components on the membrane with time making automatic stepping during testing

impossible. Manual alignment is essential, causing additional risks. Notwithstanding the above, the fact that the probe cards are readily available and the long experience with this type of test at the wafer level still makes it an attractive alternative if the test is executed with due care.

Pico probing is a subset of probe card testing and has been developed specifically for manual fault isolation of microcircuits using a thin wire, thus minimizing probing damage. This method, however, severely limits the types of tests that can be performed since only a very small number of probes can be applied at any one time. Typically, this method is only used for detecting power and ground shorts.

Membrane probing is a technology that is being developed and is currently in its infancy. It shows great promise since it allows a controlled impedance to be maintained from the tester electronics to within a fraction of an inch of the die under test. In addition, large pin count devices can be tested and the probing damage is minimal due to the large overdrive capability of the membrane. Currently, the high cost of membrane probes, their limited availability, long lead time, and difficult alignment make them a useful alternative in only a few high volume cases.

The interface to the unpackaged MCM could be a probe card accessing the perimeter of the MCM including test points, metal-on-elastomer (MOE) interface, a large area membrane probe, or a temporary package.

The MOE interface has been developed at GE and offers an attractive alternative to the above methods. In this case, a MOE interface is used where the perimeter connections of the MCM are bridged to a PCB load card on the tester. This allows the signal impedance to be maintained from the tester to the MCM. The signal loading is also minimized since no flexible cabling is required. In addition, temperature testing is possible. However, the limitations of this test interface still need to be evaluated to rate its performance.

Commercial vendors offer probe cards that are useful in a MCM foundry as shown in these examples.

- FRESH Technology group has a 448 pin 200 MHz probe card technology that is available for about $2500. This technology will accommodate a large portion of the foundry products, both ICs and small dimension MCMs

- VTE currently offers a contractor for testing fine pitch flat packs down to 8-mil pitch with 564 pins. It is also intended for burn-in testing. They also offer a membrane probe card for IC testing

- Tektronix had been in the membrane probe business for a short period of time, but is not currently producing a product. (See paragraph 4.4.3.7.2.3 for future products.)

4.4.3.7.1.4 **Fixtures.** A wide range of MCM package types is expected in the foundry. Some may be connected by gold bumps on the surface, while others will have perimeter connections. A universal interface is unlikely for all package configurations today, due to performance considerations.

The configuration of Digital Pin Electronics (DPE) today allow a small footprint for the DUT interface card. This small footprint inherently reduces the cost of fixturing. The MDT system interface can be designed to the same DPE footprint. One DUT card should be produced for each package type that can be used on both the IC tester and the MDT interface.

Ad-hoc methods have been used to reduce repair time and increase signal integrity, such as using stacked, replaceable connectors. These techniques can be used to a degree in the MCM foundry, limited only by the bandwidth of the connector system. Personality cards can be configured with these techniques, to interface to the common "test head" board.

4.4.3.7.2 **Future**

4.4.3.7.2.1 **Digital Pin Electronics.** The current ATE will be adequate for the near term MCMs with a frequency range of up to 200 MHz and a pin count of up to 500 pins. Hewlett-Packard currently has a model that will run 400 MHz at a reduced capacity. Major ATE manufacturers will be introducing new models, and more performance over the next 10 months. This includes performance enhancements and features tied to testability.

4.4.3.7.2.2 **Software.** ATE, design tool, and third party software manufacturers, are aware of the need to address the increased interest in MCMs. Improvements are being made to the handling of boundary scan interfaces, and simulation of circuits with clusters of circuitry surrounded by boundary scan, in future product releases. This type of development needs to take place in all of the five major software tool types required in the foundry. The foundry will use these tools to develop a toolkit within the Mentor Falcon™ framework, and the University of Arizona (U of A) Package Design Simulation (PDS) analysis tools. These tools will be available for evaluating customer designs and developing test software. A summary of the five areas and future enhancements is outlined below. A corresponding software roadmap is shown in Figure 4-33.

Analysis Tools

The U of A has been working with GE on the noise analysis tool included in GE's HYPACK tool. Further developments are planned for 2D and 3D analysis to cover frequencies to 750 MHz in five years. These enhancements, plus electromechanical and thermal analysis tools, are planned for incorporation into the PDS package at the U of A.

The design for testability analysis tool, TIGER™, is available from MCC for aiding circuit design. This tool, actually a knowledge-based system, guides the designer by identifying testability problems, and "what-if" solutions. The tool will be reviewed and updated for application to MCMs.

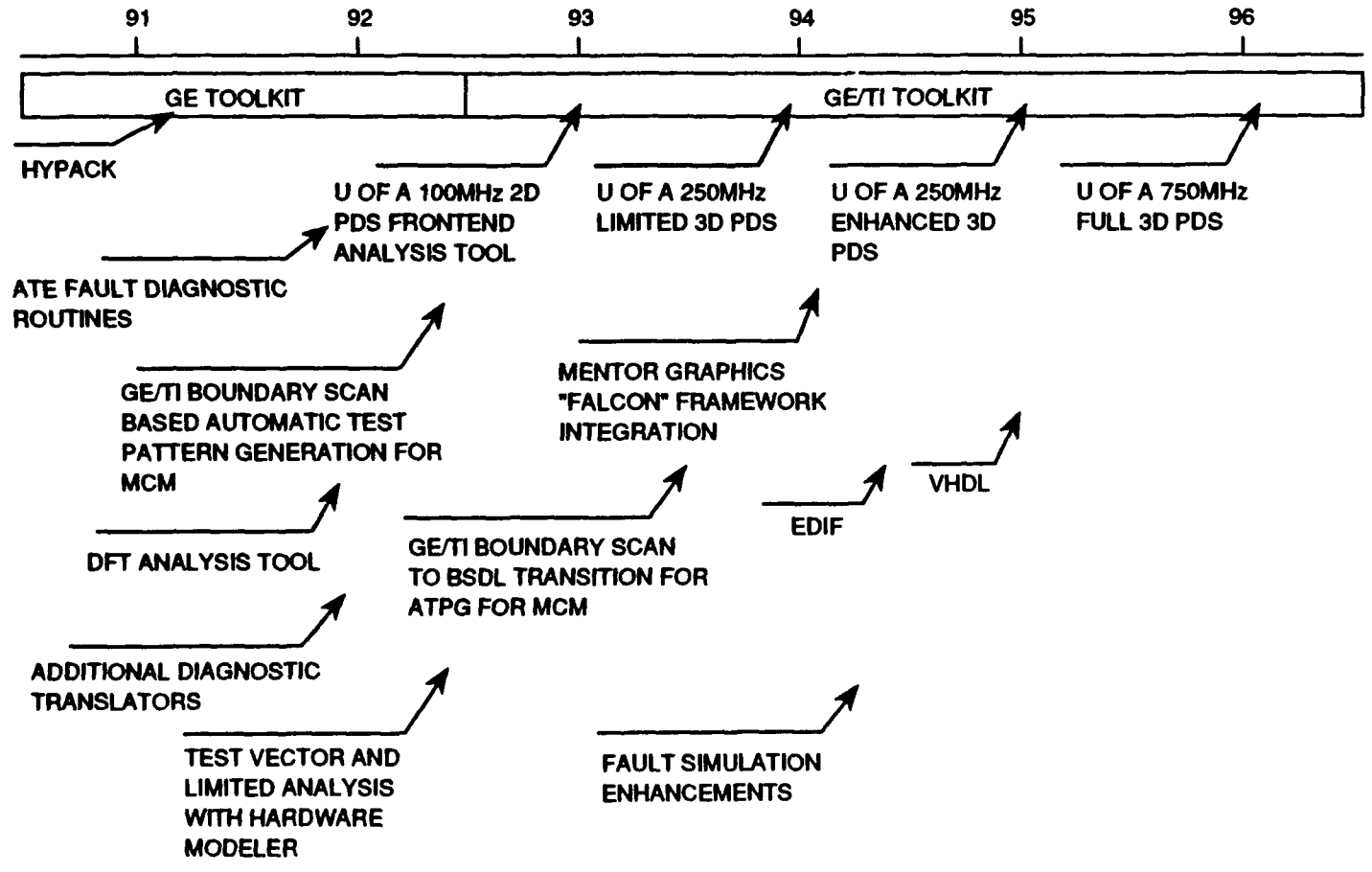


Figure 4-33. MCM Test Software Roadmap

Algorithmic Test Generation

The industry standard IEEE 1149.1 boundary scan test was developed to provide a solution to the testing of the connections of the components on boards and is fully applicable for verifying the MCM interconnect and associated IC inputs and outputs. The use of boundary scan is a requirement to put the MCM foundry on par with PCB board technology. Tools, incorporating boundary scan and other techniques, are key elements to improving test generation and reducing the cost of test. These tools include a scan path integrity test generator, a scan path based interconnection test generator, and embedded memory test generator. These tools should execute on a workstation in an off-line mode.

GE is currently developing a tool for generating boundary scan path based MCM interconnect tests. The tool will require a functional description of the boundary scan cells on the ICs and an MCM netlist. The emerging boundary scan description language (BSDL) standard will ultimately be used to describe the configuration of the boundary scan chain, and the EDIF standard will be used to describe the netlist.

Fault Simulation

Enhancements to the existing fault simulation capabilities and methodologies will also be required in the future. These include the automatic generation of the input vectors as well as the output vectors. The simulator will also have to recognize that the cells along the boundary scan path are available as inputs and outputs. Additional simulation related issues are discussed below.

Test vector verification via a hardware modeler provides an alternative approach to test vector verification. The hardware modeler will be instructed in software to provide the physical links to all the individual components on the MCM and the test and fault isolation vectors provided by the customer will be run through the modeler. Faults can be injected at the IC pin level and their results can be observed at the MCM's primary outputs.

To date, a number of independent gate level modeling platforms exist that require a large run time to provide test vectors and adequate fault coverage at the IC level. As the complexity of IC designs increases, the IC industry as a whole, will need to provide capabilities to overcome the shortcoming of current device modeling approaches. One of the primary deficiencies is the inability of the hardware model to resolve input patterns that include one or more pins in an unknown state.

With today's simulators gate level fault simulation of an entire complex MCM is not practical, if even possible. Therefore, a divide and conquer methodology will need to be developed. This methodology could operate like this. Perform the entire MCM simulation using only behavior and hardware level models; no gate level models. This is a control run to determine what the outputs should be. Then iteratively run the fault simulation after substituting one part's gate level model for its behavioral model using a subset of the input vectors that are associated with faults in the part with the gate level model. Continue rerunning the simulator, substituting models and vectors for one IC at a time. These fault

simulations can be done in parallel to save time. After all fault simulations are completed, the results of the independent simulations are combined to produce a composite gate level fault simulation.

Mentor and Valid simulator companies have both shown interest in adapting to the requirements of the MCM level of simulation. Discussions with Mentor have also included the need for simulation of BIT tests.

Translation

Since, typically, many ICs from different vendors will be integrated on a single MCM, it will be difficult to acquire models, generate test vectors, and to analyze the vectors at the foundry because of the large effort required. The customer will be best suited to perform this task. This fact will cause the foundry to accept data from many CAE/CAD systems and this data will have to be converted into the system used by the foundry. This problem will be minimized if the CAE/CAD systems evolve using industry standards including VHDL for models and EDIF for vectors and netlist data.

In addition, a translator is being written by TSSI to translate the diagnostic information to the HP82000 IC tester.

Execution

The ATE systems that have been selected for performance testing of the MCMs in the foundry will require enhanced diagnostic software to be compatible with a high volume foundry. Additionally, the diagnostic routines that execute on the MCM test systems will need to comprehend scan based inputs and outputs. This requirement is true for both fault dictionary and guided probe routines. TI is presently working on a fault dictionary routine with this capability.

4.4.3.7.2.3 Probe Technology. Companies are developing methods that are required to be comparable in pitch and speed to MCMs. They use flex circuit technology, membrane probe, and micro coax as the 50-ohm line. Some cannot stagger leads and therefore reduce the number of potential pads contacted per square inch.

Tektronix is currently redesigning their membrane probe for announcement at the International Test Conference in October 1991. It is to be a 4-mil pitch, 50-ohm probe capable of low GHz performance. The cost, however, will be about $10k, which would only be practical for volume production.

VTE has a probe assembly technology for TAB tape testing using the flex circuit technique. This technology is being extended to 600 contacts to as low as 4-mil spacing. This technique will also be too expensive for low volume applications, at approximately $9000 for a 300-pin card, plus the engineering charges.

APT is adapting their backplane technology to probe cards, and are in Beta test at this time. This method can match delays due to the individual micro coax used. They are working on methods for a 1.2-Ghz product to be introduced in the future.

ATE companies are working with probe companies to reduce the electrical problems at the interface between probe card and test equipment. The emphasis has been on the area of die test. This is an area that will be key in the future of improved probe testing, but will also be adaptable to the MCM physical size.

TI is currently developing in-house membrane probe capability for room temperature and burn-in applications.

4.4.3.7.2.4 Fixtures. The high frequency test problems are being addressed by other areas in the industry. APT is adapting their high frequency technology to produce a low cost method of adapting to ATE. The card being developed replaces the cables in the ATE interface for a more uniform and reliable impedance to the device under test. This system can be either 50 or 100-ohm in the $2000 price range.

A common, fine pitch, elastomer concept by Sandia National Labs, may be useable for either the surface array connector or the perimeter connector package. The fine pitch of the elastomer would place at least one conductive element on each pad or lead. More research is needed in this area.

4.4.3.8 Rapid Prototypes

4.4.3.8.1 Definition. A rapid prototype is a functional MCM unit that allows evaluation of the intended application in a developmental environment. The package type, size, and pin configuration may be different from the final product to reduce delivery time. The unit may not meet all timing requirements due to the possibility of limited simulation and package layout.

TYPICAL APPLICATIONS	LAB	NON-LAB
1. COMPUTER	Yes	Yes
2. MILITARY	Yes	No
3. COMMUNICATIONS	Yes	Yes
4. AUTOMOTIVE	Yes	Limited

4.4.3.8.2 Test, Analysis, Isolation. Testing of prototypes will be evaluated on an individual design basis. The customer may evaluate the first samples in the system or in an engineering evaluation set-up. Also, a percentage of prototypes built are never put into production. The design and function of some MCMs may also be unavailable to the foundry for use during test development until a production test is required.

Test structures located on each individual die, a test specific die, or on the overlay can be used to verify production quality and overall performance. GE and Sandia have both

generated techniques to aid in the evaluation process. GE has developed TEGS that evaluate the interconnect integrity. The TEGS can be measured after each layer of overlay for close process monitoring. The Sandia test die are described in paragraph 4.4.3.2.2, Reliability.

4.4.3.8.3 Burn-In Requirements. The GE HDI process incorporates materials that are different from other MCM and hybrid processes. The testing to date shows a robust packaging technique that does not have the same failure characteristics as other packages. This fact, plus the definition for rapid prototypes above, does not warrant burn-in as a requirement.

4.4.3.9 Volume Production Considerations

4.4.3.9.1 Incoming. Moving the test burden to the die manufacturer is a must for high volume production. The manufacturer can better address the die test issues from the technical and capital aspects than replicating these functions in the foundry. GE is currently working with several semiconductor companies to set up die acceptance criteria and inspection after wafer sawing.

One alternative to relying on the die manufacturer is to develop the handling techniques required to pick and place individual die to a membrane probe test fixture arrangement. This may involve using temporary adhesives or mechanical systems to hold the die. A vision system could be used as an inline check for gross defects. This ability would avert any problems with manufacturers that were not willing to develop the additional capability to do assembly level testing at wafer probe. It would also greatly reduce the additional cost of retesting the ICs by eliminating temporary packaging schemes.

The impact of incoming test affects the final test capital costs to a great degree. By adding the incoming test for a 20-die MCM, at a volume of 15000 per month, there is a net decrease in the total capital cost of test equipment of approximately 27%. This is due to the reduction of the quantity of test equipment required for MCM assembly level troubleshooting.

4.4.3.9.2 Production Test. Test time of the MCM will become a key element for high volume production. This includes both the go-no/go test and troubleshooting. The greatest impact on test time is the amount of DFT in the design. (See figures in paragraph 4.4.3.1.1.) The ability to access and observe the required points directly affects the set-up of conditions and detection of errors. BIST can also be running concurrently in multiple ICs as part of the "kernel" test. The actual test time savings varies with design, but can easily reduce the test and troubleshooting time by 50%. Test time is tied directly to foundry capital costs.

A second impact on test time is the vector download time in the ATE. The ideal situation would be to have all the vectors loaded into the ATE memory at one time. Many test systems do not have the capacity to hold 100% of the vectors, and some designs will require an excessive number of vectors to test the MCM.

Fault isolation methods will need to be put into place for each product to quickly and accurately detect the failure.

4.4.3.9.3 Rework. Rework in a volume situation will be handled in a more efficient manner by utilizing the rapid prototype portion of the foundry originally set up as the baseline facility. The expanded facility will be more automated for handling high volumes.

Trouble sheets will need to be on-line, and tied to a bar code system for identifying the MCM configuration. This level of control will allow product lots/runs to be mixed on the production floor and still maintain data for evaluation. Units will be able to be held, if necessary, until sufficient quantities are accumulated for efficient testing.

4.4.3.9.4 Common HDI and Silicon on Siiicon Foundry. TI is involved in developing MCMs using the SOS approach. The HDI and SOS foundries may be consolidated at some point in the future to service the diverse MCM market. Test methods will be very similar for both MCM construction methods. One additional piece of test equipment will be required in the foundry to test the silicon substrate. The tester, like the Integra-Test Micro-prober 90, will cost about $160,000. Because the die used in SOS MCMs are mounted in TAB tape, the fixtures used during die test will be unique to that technology. The manufacturing defects (interconnect) test will apply to both HDI and SOS after components are connected. The final performance test will also be identical.

4.4.3.9.5 Burn-In. The application of burn-in to ICs in MCMs is no different than any other assembly. The difference comes in how to handle the die, and the methodology used for screening when high reliability is required. The burn-in strategy will be design dependant due to the variation in failure rates of die used in the design.

It is important to understand why test or burn-in is accomplished and the effect this screening has on the non-conformance of the finished product.

A determination must be made on a part by part basis as to whether or not 100% test or burn-in is cost effective prior to the start of assembly. The cost of non-conformance must be compared to the cost of performing 100% test or burn-in. When the cost of test or burn-in exceeds the cost of non-conformance, then it is not cost effective to continue 100% test or burn in.

By using the average outgoing quality (AOQ) of a die and the quantity of the die that will be used in an MCM, it is possible to calculate the probable number of units that will be defective without burn-in.

To calculate the cost effectiveness of burn in, it is necessary to know the early failure rate, the intermediate failure rate, and the field failure rate expressed in failures in time (FIT). By using the failure rate and the quantity of die in a MCM, it is possible to calculate the probable number of failures at any point in time after the initial testing of the MCM.

Software programs are available for this type of analysis. However, the data is not always available. The MCM foundry will need to collect the data that is available and generate additional data where practical. Failure data from similar die technology and size might be used for correlation to unavailable die information.

Under low volume and prototype conditions, burn-in of die can be handled either by prepackaging die for burn-in, burning-in the die in the final MCM package, or lot qualification at the manufacturer. These current methods are not cost effective for high volumes (Figure 4-34).

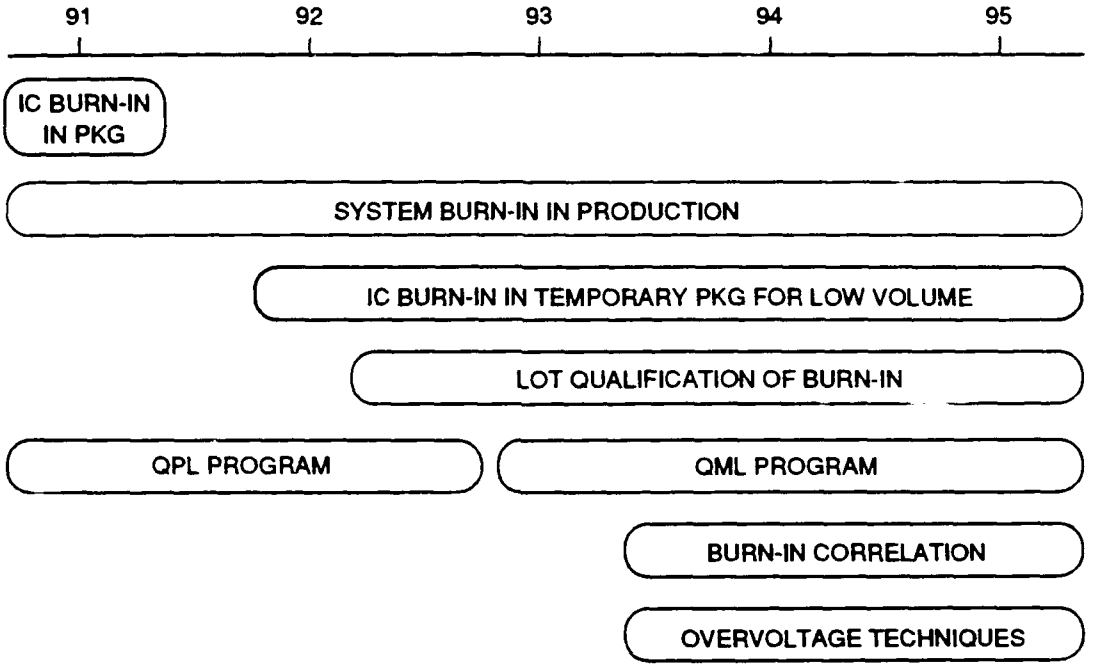


Figure 4-34. Burn-In Roadmap

In the high volume foundry, methods need to be developed to handle die for burn-in, or methods established at the IC manufacturer for correlation screening. "Overvoltage" screening methods need to be studied as a method of reducing the cost of producing more reliable die. Studies should also be conducted to investigate possible correlation to functional yield at probe. The resulting methodology needs to be under a Qualified Manufacturers List (QML) plan. Verification will need to be instituted until the QML plan is qualified. Some of the corporations in the QML program are ATT, Honeywell, Intel, and IBM. TI is currently reviewing the QML program for its semiconductor operations.

4.4.4 Foundry Implementation

The recommended foundry implementation is outlined below, based on the information collected in the above research.

4.4.4.1 Methodology

4.4.4.1.1 Roadmap. The MCM test methodology roadmap, Figure 4-35, is divided into three basic areas; incoming test, manufacturing defects test, and functional test. The roadmap addresses all products in the MCM foundry for the next few years. The specific test method,

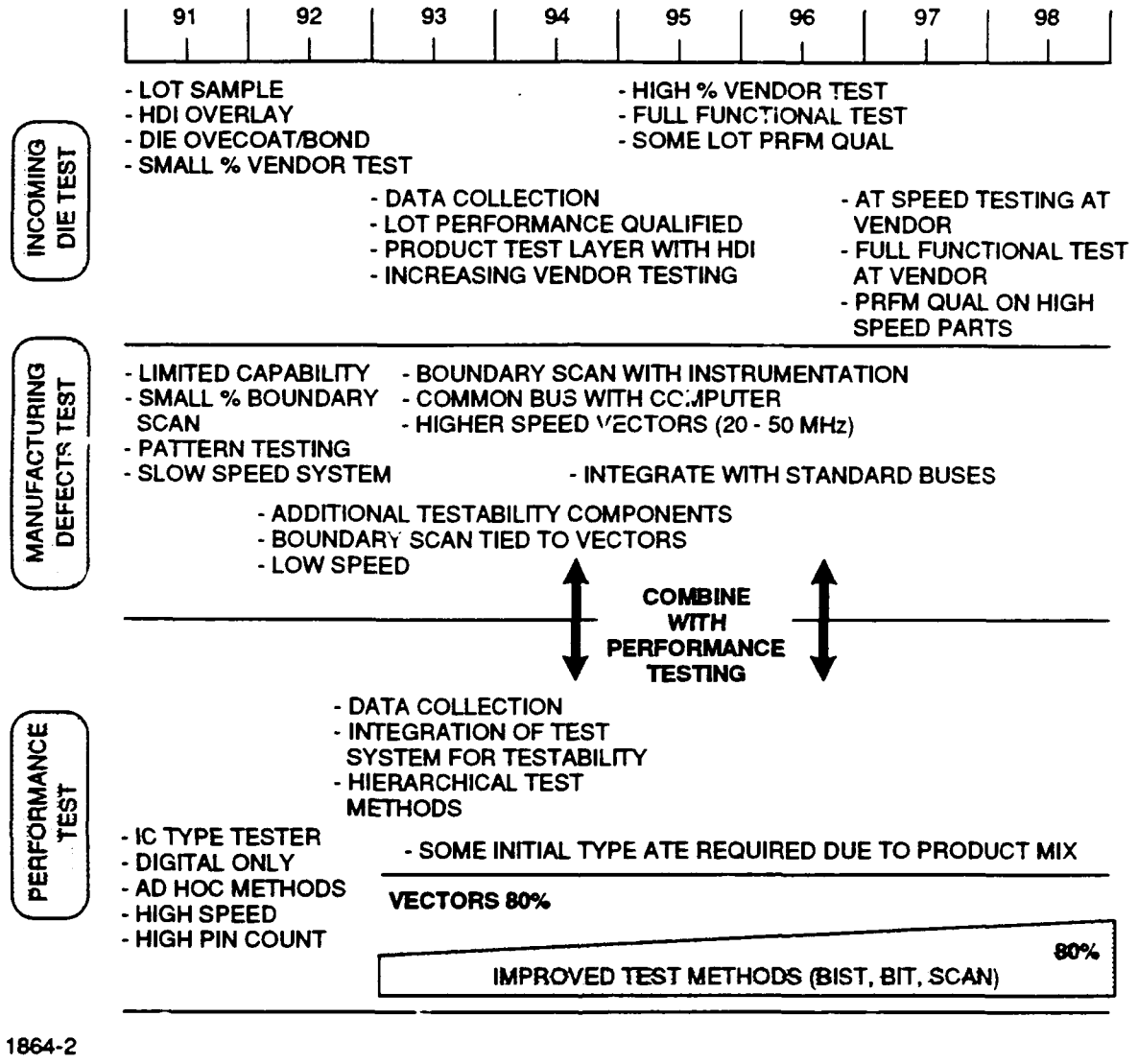


Figure 4-35. Test Technology Roadmap

or combination of methods, to use on an individual product will be determined by many factors, such as product application, cost, and performance. The methodology must be flexible to allow the foundry to take advantage of vendor and foundry test capabilities.

The row across the top of the roadmap is the incoming die strategy. The foundry will need to inspect die according to die type and vendor test strategy. This basic evaluation will determine the need for additional testing, either at the vendor, or in-house. Die tests at wafer probe need to be the equivalent of today's packaged IC test, for the long term MCM foundry strategy. The roadmap shows several combinations of lot qualification and temporary packaging methods to test and burn-in die that should be used until the die manufacturers test to the standards of today's packaged ICs. Lot qualification of die for speed can be done by packaging a sample of the die. Advances in probe technology and the trend toward better

testing at probe, indicates that adequate testing capability will be available in the future from the die manufacturers.

Individual die test and burn-in will initially be performed by pre-packaging parts for handling. GE has developed several methods using the HDI process to allow for single or multiple die to be packaged and tested. These methods can be improved, and others need to be developed to allow easy placement, test, and removal of individual die, such as on blue tape used by the IC industry. Lot qualification can be used in some cases. In the long term, "overvoltage" methods need to be investigated for quick temperature screening correlation that can be accomplished at probe. Correlation to probe would further reduce die test cost for burn-in, making high reliability die available for more standard products. For some products burn-in of the die should be performed at the module level.

Manufacturing defects testing will be based on boundary scan techniques. This technique allows testing of the interconnect between die with a minimum of additional routing. Other testability features in the MCM will be used in conjunction with scan to gain as much diagnostic information as possible. Each design will be different and will require the test strategy to be flexible. The combination of built-in self-test (BIST) and conventional pattern testing algorithms will be used with scan to allow the design engineer to optimize the test for the design. In addition, test element groups will be used to evaluate the foundry fabrication integrity.

A simplified test system will be developed for manufacturing defects testing. The system will communicate with IEEE 1149.1 boundary scan protocol and other prevalent test interfaces the future. A small digital section that is tied to the scan interface to allow handshaking will be incorporated. This will allow efficient use of testability features in the MCM. As testability becomes predominant, we believe the manufacturing defects test system will accomplish a greater amount of testing, due to test features residing on the MCM. This will continue to reduce the cost of test and capital costs.

As shown on the roadmap, the manufacturing defects tester and the performance tester functions will merge to a great degree in a few years. This high cost, high speed test system will migrate toward the moderate cost, integrated manufacturing defects test systems of the future. However, the range of designs in the foundry will include those that require extensive patterns, due to designs that are simply repackaged and not redesigned for testability. There will be a mix of complex ATE and the future manufacturing defects tester type system on the test floor for a long period of time.

The area of performance testing also needs to be flexible to make the best use of testability features and test system capabilities. The foundry today will need a performance test system that can handle the I/O, clock speed, and pattern depth of the "typical" MCM. The test system will be an IC type tester, versus a board type tester, due to the performance available.

4.4.4.1.2 Flow Diagrams. The flow diagram in Figure 4-36 shows the incoming die test options and how the incoming methodology will be driven by the cost of rework after

assembly. The three incoming paths represent the options for bringing die into the foundry with estimates of the percentage of die through each path after the foundry is established. The failures that are seen at MCM test drive the incoming strategy. The initial strategy will be determined by the items listed in Figure 4-36 under the heading VARIABLES.

The incoming test strategy will be key to a successful foundry. Personnel need to be assigned to the task of creating alliances, methods, and options for obtaining thoroughly tested die for the foundry.

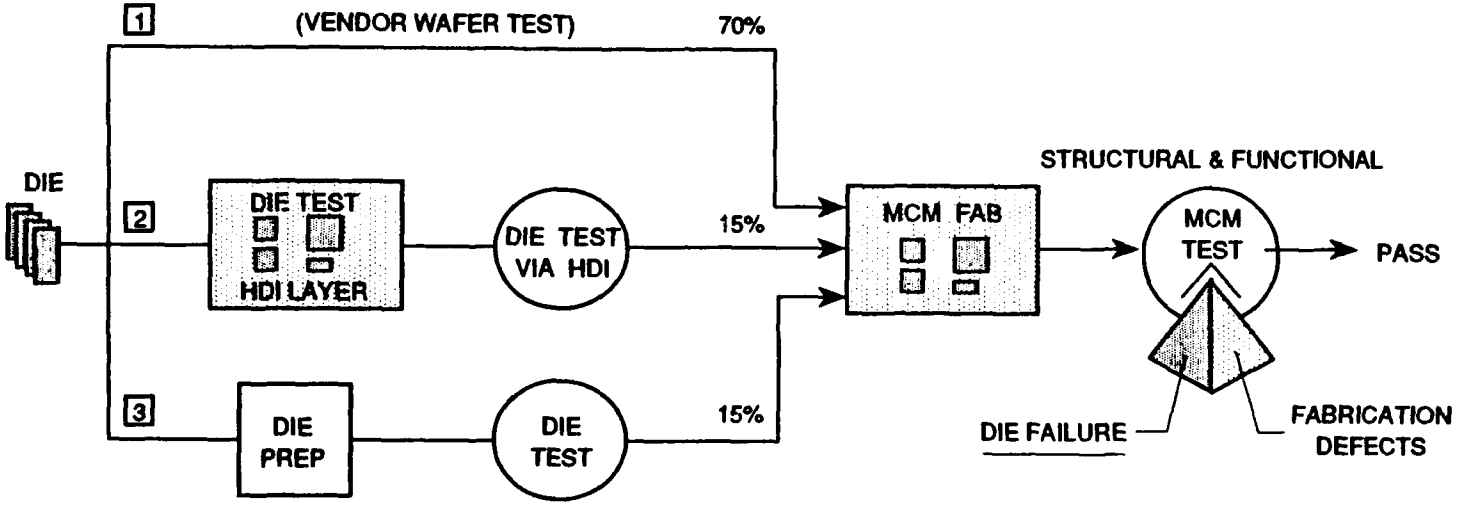
Figure 4-37 shows the options of test to the customer. Typically, the MCM will be tested with the customers vectors after verification of proper assembly at the manufacturing defects test. Test Elements Groups may be used to qualify interconnection and performance of the interconnect for some defense customers or proprietary projects. Some customers may take delivery without further testing, but rely on die test and MDT. Some customers will require screening to certain environmental conditions. In any case, the customer and foundry will need to work together and agree on the test strategy and requirements prior to production of the MCM.

4.4.4.1.3 Design for Testability. The foundry will need to work closely with the customer to verify a certain level of testability, or agree on the test methods that will be used and the level of acceptable fault detection and isolation. This review should be part of the "quote" given to the customer. The foundry should use rule based guidelines applied to the specific design. TI is in position to support the MCM foundry with the Test Technology Center and Lab involvement in development of the IEEE 1149.1 standard, test products, and infusion of DFT in the company and to customers (details in paragraph 4.4.3.1.1).

4.4.4.1.4 Customer Interface. The transfer of data from the customer will need to be flexible at the start, with future interface definition being developed with industry. Standards need to be part of the future interface, with translators being used in the near term. The transfer of test vectors will need to be discussed early to verify compatibility (details in paragraph 4.4.3.1.3).

4.4.4.1.5 Vendor Interface. Working with the die vendors can not be overstressed. The area of incoming die will be key to low cost modules. The reduced amount of handling, capital equipment utilization, and expertise of the semiconductor industry can keep the cost of tested die lower than the foundry with its additional handling, etc. The quality of die will reduce the number of MCM failures, and, therefore, the amount of time spent troubleshooting these complex modules (details in paragraph 4.4.3.1.4).

4.4.4.1.6 Standards. Certain items can be incorporated in most areas of the foundry to take advantage of standards and standardization. The use of EDIF and VHDL will be very useful if developed properly. These standards are being reviewed at this time and will require some attention from the MCM industry in the form of participation and review of the proposed standard changes. EDIF is moving in the direction of test and could provide a significant link to the foundry in the future. The chair for the EDIF subcommittee on Test Technology currently resides at TI.



VARIABLES:
- # OF DIE/MCM
- TYPES OF DIE/MCM
- VENDOR WAFER TEST STRATEGY
- HANDLING COSTS/RISKS
- VOLUME OF MCMs OVER TIME
- VARIANCE IN TEST COMPLETENESS

- % DIE DEFECTS
- COST OF REWORK/SCRAP

← **DRIVES DIE TEST STRATEGY**

DIE TEST COSTS VS REWORK/SCRAP COST

1864-3

Figure 4-36. Die Test Costs Versus Rework/Scrap Cost

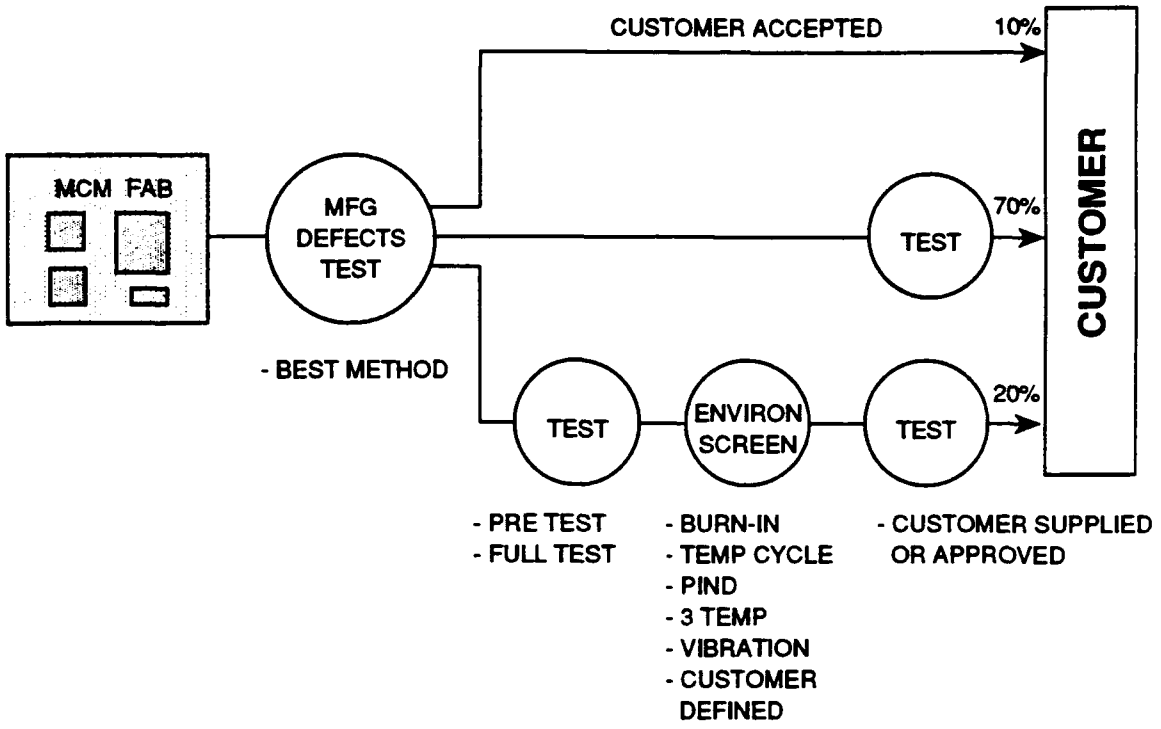


Figure 4-37. Fabrication Test Flow Options

TI played a major role in the development of the architecture that became the IEEE 1149.1 boundary scan standard. TI continues to be active in all of the IEEE 1149 test bus definitions through the Test Technology Center of DSEG.

Macros, or cells, in the design libraries of the CAE/CAD system should include testability as an integral part of the circuit. This embeds the methodology and knowledge base of the cell designer into the circuit. Large functions are more likely to include this type of "cookbook" testability.

4.4.4.2 Technology

4.4.4.2.1 Die Handling. Individual die handling for test is very limited today. Handling bare die is labor intensive, prone to damaging the die, and should be used only as an alternative to die manufacturer testing at the wafer level. For those die which are not tested adequately by the die manufacturer, some form of low cost handling needs to be developed for a high volume foundry. Low volume methods are available today.

4.4.4.2.2 Probe. Probe technology is being addressed by industry, as far as capability. The one area needed for the foundry is lower cost. The estimated $10,000 cost of most technologies is too high for all but high volume products. A cost effective solution is needed for frequencies of 200 MHz to 400 MHz.

4.4.4.2.3 Automated Test Equipment. The ATE for the foundry, in the beginning, will consist of an ASIC verification system that will be used for incoming die test and final MCM test. The system will be selected to meet the typical I/O count of the die and MCMs of about 300. The frequency will be based on die test more than MCM I/O speeds, and will be in the 200-MHz to 400-MHz range. The foundry will use this system for rapid prototypes and characterization when higher throughput machines are needed for any specific program. Specific IC production testers are available that have more capability located at each pin to reduce test time.

ATE manufacturers will need to continue to improve the way ATE accesses test structures embedded in MCMs and develop new and innovative ways to take advantage of those structures. With the boundary scan standard becoming mature, the ATE manufacturers are seeing the need for increased vector depth and automatic boundary scan protocol generation to reduce the cost of test generation and execution.

A test system needs to be developed which is directed at the testability of the MCM versus broadside vectors. The initial system will be used for manufacturing defects testing where boundary scan is to be used. The system must provide the user with friendly, efficient interfaces to download BIT code, perform interactive boundary scan diagnostics, drive IEEE 1149.5 Test Maintenance (TM) buses, perform cluster test routines via the boundary scan bus, and utilize broadside vectors. This will be a PC based system that integrates TI's ASSET boundary scan system and instrument-on-a-card digital technology. This system will also serve as a vehicle for understanding additional requirements for an integrated test system in the future.

One major problem caused by the lack of physical access is the detection and isolation of shorts. The use of HDI and real time process control feedback is expected to minimize the occurrence of shorts within the MCM interconnect, but it probably will not eliminate it. The ability to detect and isolate shorts before or shortly after powering up a MCM is critical to minimize the risk of a short causing a good part to be damaged. One possible solution for the future is to develop a current monitor for ICs that will output a failure indication via the boundary scan bus. Another possible aid to isolating shorts is automated thermal imaging techniques.

4.4.4.2.4 Software. The foundry will be involved in a wide variety of design applications from various customers. A suite of time saving tools needs to be utilized to interface to the customer, evaluate designs, generate programs, and troubleshoot products. Several types of software which are needed for the foundry are categorized below. The basic capabilities of today's software are applicable to the MCM foundry, but the software needs further development to address more complex circuits, better user interface, and more automatic generation of test routines.

1. Fault simulation
2. Analysis
   - Noise analysis
   - DFT analysis
   - Process control and trend analysis

3. Conversion
   - Vector conversion
   - ATPG
4. System runtime
   - Fault dictionary
   - Interactive debug modes to aid the operator in diagnostics.

4.4.4.3 Risk Assessment. The main risk to a successful, low cost foundry is the quality of incoming die. The foundry needs the die to come from the IC manufacturer ready for insertion into the MCM. Methods have been outlined in this study for the in-house testing of die as an alternative. The added testing in-house is adequate for some projects but will always introduce the chance of damage, due to additional handling in addition to the added cost.

A secondary risk is the level of testability incorporated in the MCM. The foundry will not always be consulted with sufficient time to properly influence testability, or the customer will not be willing to change a design due to various reasons. Increased test time will solve most testability problems but is not desirable due to the adverse affect on foundry throughput and increased troubleshooting effort. The acceptance criteria for the completed MCM will always need to be agreed upon in advance of release for production.

4.5 MATERIALS AND PROCESS DEVELOPMENT

4.5.1 Enhancements to GE Baseline

During the technology interchange between TI and GE engineers, several potential incremental enhancements to the present GE baseline processes were identified. These enhancements are both process and product design related and try to incorporate the advantages of both the GE/HDI methods as well as some of the advantages of the chips last technologies. The generic GE/HDI construction is readily conformable to many target uses. With a family of dielectric and adhesive systems developed and characterized, this MCM technology can serve the military and commercial markets with minimum change to other processes. This family of dielectric/adhesive systems will be necessary to handle the wider range of die types such as GaAs, InSb, HgTe, etc. These enhancements (as were shown in the cost analysis) are required to reduce MCM cost to meet projected design to cost goals for the high volume facility. These enhancements are listed in Table 4-2. This table is listed in the order of insertion into the MCM foundry and/or evaluated in full scale development for possible insertion. The level of risk and the major area of impact on the foundry is also listed. The cost rank column relates the enhancements to each other from an effect on MCM cost standpoint.

A description of the enhancement and the rational for why its needed, potential risks and additional areas of impact will be described in the following paragraphs. The difference between the "low", "med", and "high" risk is based on the amount of development required for each enhancement. A "low" risk requires no process, equipment or materials development and only requires process/material characterization and/or equipment installation. A "med" risk enhancement requires minor process/equipment/material development prior to process

TABLE 4-2. GE BASELINE ENHANCEMENTS

Cost Rank	Enhancement	Risk	Impact	Insertion Year Minimum	Aggressive
2	Kapton Lamination for all layers	Low	V,Q,L	92	92
8	Water Jet Trim	Low	V,C	92	92
9	Upstream Epoxy for Pick and Place	Low	V,C	92	92
11	Semi-Automated Material/Data Handling	Low	V,Q,L	92	92
3	Batch Lamination	Low	V,C,L	93	92
1	Pre-molded Substrates with Metal O Applied	Med	V,C,L	93	92
10	Combine Mfg. and Functional Test	Low	V,C	93	93
4	Layer 1 Pads to "Grid"	Med	V,C,L	94	93
5	Mask Processing on Layer 2 and Above	Med	V,C,L	94	93
7	Kapton with Adhesive Applied	Med	V,C,L	94	93
6	Electrophoretic Resist	Med	V,Q,L,S	94	92
12	Automated Plating Process	Low	V,Q,L,S	94	93
13	In Line MRC	Low	V,L	94	94
14	Kapton With Adhesive and Metal Applied	Med	V,C,L	94	94
15	Boundry Scan for MCM Test	High	V,C	95	94
16	Full Metal Deposition in MRC	Med	V,C,L	95	94
17	Photo-Imagable Dielectric	Med	L	96	95
18	Pre-Tested Die	High	Q,L	96	95
19	Die With Bond Pads Larger	High	V,C,L	97	96
20	High Rate Drill	High	V,C,L	97	96

V = Volume Q = Quality C = Capital $ L = Fabrication Labor S = Safety

characterization and/or equipment installation. A "high" risk enhancement requires significant development in all areas and/or requires significant control over supplier product characteristics.

1. Premolded substrates multiple MCMs up with metal 0 applied and imaged: This is a critical need for high volume low cost MCMs. It is envisioned that 8-inch wafers would be produced by substrate suppliers, for high volume applications that would have the cavities for the die premolded. It would then be possible to have multiple MCM modules on a given slice, thereby reducing fabrication cost. A further enhancement would be having the metal 0 deposition completed on the substrates prior to delivery to the TI foundry. This would reduce processing steps and, by allowing the supplier to do these steps in mass, reduce overall product cost. These substrates

could be made of several different materials depending on the final system needs. For the military market these substrates would be either Aluminum Oxide (Al_2O_3) or Aluminum Nitride (AlN) with or without buried cofired metal conductor to allow for integral hermetic packaging. Two suppliers, W.R. Grace/Coors and Ceramic Process Systems, have indicated capability to build premolded substrates with or without metal 0. W.R. Grace/Coors has demonstrated prototype capability in the cofired metal conductor technology. Ceramic Process Systems has built substrates with cavities for other applications for other companies that do not have the cofired conductor technology. For the commercial market, the substrate could be made of several other materials; plastics, metals, composite metal/plastic, composite metal/graphite, etc.; that would be chosen based on performance requirements of the module. These materials are all less expensive and more easily molded than the ceramic materials. The inputs that we have received from commercial companies indicates that they have needs for MCMs that could require ceramic substrates for their high power applications, but that also have MCMs requirements that could be built with plastic substrates.

Risk: **Med** - The ability to fabricate premolded substrates has been shown, but both Grace/Coors and Ceramic Process Systems have indicated that 1-3 man years of effort are required to characterize their processes depending on the type of substrate required.

2. Kapton lamination for all layers: This is productionization of development work presently underway at GE-CRD. For this enhancement instead of laminating Kapton only at the first lamination step, Kapton would be used on all dielectric layers. This would reduce the number of types of materials required to build the MCMs and thereby, allow the purchase of larger quantities of materials at a lower cost. Advantages can also be gained due to the control of the dielectric thickness inherent in a cast film and also due to the elimination of foreign material in the MCMs due to entrapment in the liquid dielectric prior to curing. At present dielectric thickness control for higher frequency circuits is maintained/controlled by very labor intensive measurement steps. Also, the topology improvement that can be obtained using cast films, due to leveling of the surface in the space between the die and the substrate reduces the imaging defects caused by changes in focus for the laser imaging system. This multilayer process has been identified as a necessary entity for stacked 3-D modules (a technology extension to be discuss in paragraph 4.8.1.2). The stacking of the HDI module to module could potentially cause interlayer dielectric shorts due to the low Tg and low solvent resistance of the SPI-SPI/Epoxy dielectric layers. This enhancement will ease all of the issues.

Risk: **Low** - process is under development at GE and reliability data indicates product characteristics similar to the normal HDI process. A challenge will be to work with the dielectric suppliers to obtain a family of materials that have varying thickness such that the electrical performance of the module can be tailored with controlled material thickness variations.

3. Batch Lamination: This is an extension of technology used in the manufacture of PWBs that integrates with the Kapton lamination of all layers discussed previously. At

present, one MCM is laminated at a time, in this enhancement. With the use of Kapton on all layers, several could be laminated at once. There are several different ways that this could be accomplished: autoclave bonding, flat bed lamination, and a pinch roller approach. The autoclave process would be very similar to the present one-at-a-time process in that the substrate would be placed in a vacuum fixture with rubber bladders on both sides of the MCM. A vacuum would then be pulled on the MCM via the vacuum fixture while pressure and temperature are applied to the outside of the fixture. What gives the autoclave process the throughput lift is that several vacuum fixtures can be placed within the pressure vessel at one time and with further process characterization, it would be possible to laminate the substrates back to back there by doubling the equipment capacity. The flat bed lamination approach again is a process used widely in the PWB industry, and in the past few years equipment manufacturer have developed machines with vacuum systems that are similar to autoclave processes. The advantage that flat bed lamination brings is higher throughput due to faster heatup rates. A disadvantage lies in the reduced pressure control and, thereby, an effect on dielectric thickness. While increased pressures can reduce the variation of dielectric thickness, it's impact on the substrate and on the die is unknown. The pinch roller approach is similar to the dry film lamination process used in many industries. In this case, a piece of equipment would have to be developed to apply pressure, temperature, and vacuum to the substrates. It is envisioned that the substrates would be placed on a conveyor system that would feed into the pinch roller machine. In this way, a continuous lamination process could be implemented. Again, the concerns identified for the flat bed process would apply here.

Risk: **Low** - Initial implementation would most likely be with the autoclave process due to it similarity to the present process, but with much higher throughput. The pinch roller process would need both equipment and substrate/die reliability development and could be implemented when qualified.

4. Designs such that Metal 1 pads are on "grid": This is a key process enhancement/ product design requirement that plays a key roll in reducing the artwork/drill data required to build MCMs. In this enhancement the product design would be such that the pads on metal layer 1 that connect to metal layer 2 are on a "grid" pattern. This would allow layers 2 and higher to be drilled and imaged with non-adaptive data. This would reduce the customization that each MCM has and therefore make the configuration management issues regarding the data much easier to handle.

   Risk: **Med** - Requires that some amount of de-optimization of the design be made, which could impact silicon density and electrical function for the MCM. The effect on electrical function should be minimal, but does need to be reviewed. The impact of this enhancement is greatest when combined with the following:

5. Mask process for L2 and higher (implies plasma etching of vias): This enhancement when coupled with the one above has significant impact on the capital equipment cost needed in the foundry. After the metal layer 1 pads are on "grid" a series of photomasks could be used to produce the via sites and conductors for the following layers. After the via sites are etched, the vias are plasma/RIE etched into the

dielectric and, then, conventionally processed. This would eliminate the need for laser drilling or imaging for these layers and, thereby, reduce number of adaptive laser drill/imaging systems that are required for the foundry. This also has a major impact on fabrication labor, due to it's similarity to S/C photolithography systems which are already highly automated. An additional benefit is that this is also the method used to image and form vias in the chip's last technologies which would give the foundry the capability to build the technology that best applies to the customers design requirements at the minimum cost.

Risk: **Med** - This has the same risks as the Metal 1 pads on "grid" enhancement with the addition of the required process development on the via formation processes. Since this is a common process in the industry and at TI on a lab scale, the development tasks are well understood and are minor.

6. Electrophoretic resist: This is a process that is under development at GE-CRD. The effort would be to productionize the process in the TI foundry. The electrophoretic photoresist is very attractive for several reasons. The process is more robust than the present method of spraying photoresist on the MCMs due to the fact that it is actually plated to the metal surface in equipment very similar to the automated plated line. The electrophoretic resist has enhanced conformance to minor imperfections in the surface topography of the MCMs thereby reducing defects caused by lifting/missing resist. Another advantage is related to safety and environmental concerns. The solvents used in the present sprayed or spun on resists require special handling and control. The electrophoretic systems are fully aqueous and require no special handling. A final advantage is one of process automation. The equipment, as mentioned earlier, is similar to the automated plating line and as such lends itself to greater throughput with less manufacturing labor.

   Risk: **Med** - Process and equipment is available from several U.S. companies that supply the PWB industry. GE-CRD is presently developing the process to apply it to MCMs, but has experienced trouble with the processing on Metal O. Process development continues to be needed at both GE and with the supplier.

7. Kapton with adhesive applied: This enhancement ties into the Kapton lamination for layers and batch lamination enhancements. In this enhancement the Kapton would be purchased with the adhesive system already applied. This would allow the lamination process to bypass the operation where the adhesive is sprayed onto the substrate. This eliminates an area of contamination to the clean room, an opportunity for airborne contaminates to land on the uncured adhesive and a significant amount of fabrication labor.

   It is also envisioned that the adhesive material can be tailored for the different layers. A thermoplastic could be used to laminate layer 1 to layer 0 and a thermoset material could be used for all other layers.

   Risk: **Med** - The dielectric films with adhesives that exist as a volume product today are too thick (37 microns and higher) and the Tg of the adhesives are too low

(less than 150 celsius). Manufacturers of these products would have to develop the processes to make these films. Several custom material suppliers have expressed interest in working with TI/GE on this development effort. This product would have application to not only the GE-HDI technology, but also the chips last technologies and the PWB industry.

8. Water jet trim: This is a process used in many industries to separate parts from the frames that they are processed in. One advantage of the MCM foundry is in the reduction of the number of eximer lasers required in the foundry and the resulting capital cost reduction.

   Risk: **Low** - The equipment already exists in the industry to do this. Minor development work to integrate into the CIM data flows.

9. Upstream epoxy for pick and place: This is a separate die attach dispenser prior to the pick and place machine. This will double the capacity of the pick and place machine and delay the need for additional pick and place machines.

   Risk: **Low** - The equipment already exists in the industry to do this.

10. Combine manufacturing defects with functional test: This applies to high volume part numbers built in the foundry. Electrical testing would be reduced on the parts and, therefore, increase the throughput, reduce the cycle time, and reduce the capital equipment required. It is assumed that due to the large part number volume, the process/product would be fully qualified and the yield would be high. The manufacturing defects screening could then be eliminated.

    Risk: **Low** - Design for testability is rapidly evolving.

11. Semi-automated material/data handling: A significant amount of the manufacturing equipment and processes are similar to, if not the same as that used in the semiconductor industry. Semiconductor processing has become very automated in the past few years with TI being a leader in equipment, material, and process automation. This capability will be leveraged when installing a facility. Elements from the MMST program can be integrated in the facility, as well as from data handling and further extending the process automation previously developed in the TI Surface Mount Assembly operation.

    Risk: **Low** - Equipment and control systems already exist for most process. The key will be to integrate into the facility with the minimum cost (recurring and non recurring) and maximum flexibility and ease of use.

12. Automated plating line: This is an automation of the existing GE process. The advantages are not only in the throughput and labor reduction areas, but also in the process control area. Plating systems can be purchased which integrate the mechanical operations of the systems with the sensors controlling the process to provide overall process control.

Risk: **Low** - The equipment already exists in the industry to do this.

13. In line MRC: This is similar in concept to the automated plating line in that it allows MCMs to be processed continuously instead of in batches. The concept would be that the MCMs would be placed onto a conveyorized machine that has several vacuum chambers in series. These chambers would be of the "load/lock" design, such that the parts go from chamber to chamber without being vented back to atmospheric pressure. This would allow the deposition to take place in the central chamber while other parts are being pulled down to the required pressure in the previous chamber. This not only increases throughput, but also reduces equipment wear in the critical deposition chamber due to not having to be cycled from atmospheric pressure to process pressures for each processing load of MCMs. Throughput of the process could be enhanced by add several deposition chambers in the series and having the MCMs move through them.

    Risk: **Low** - Equipment to do similar processing is used to produce a wide variety of products; one of which is the metallization on compact disks. It is believed that with minor equipment modification a similar process could be done on MCMs.

14. Kapton with 1000 Å of Cu applied with adhesive: This enhancement is an extension of the previous enhancement. By applying the thin layer of copper metal to the raw material the process step, applying the copper in the fabrication process is eliminated. This thin layer of copper is only required to allow definition of the vias for the plasma etching step. After the vias are formed this thin layer of copper would be etched away and the rest of the process completed. As in the previous enhancement this material would be applicable to the GE-HDI, chips last, and PWB technologies.

    Risk: **Med** - The risks are the same as in the previous enhancement. The technology to apply the metal to the dielectric film is already available in the industry and posses only a low risk.

15. Boundry scan designed into MCM design: An entire section of this report has discussed Boundry Scan at the die level. If this could be extended to the entire MCM the level of testing required would be significantly reduced. This would reduce capital equipment costs due to a reduction in the number of tester required and, therefore, the amount of test labor would also be reduced. A significant probability exists that the amount of effort required to generate the test programs would also be reduced, further reducing the support cost component of the MCMs.

    Risk: **High** - This enhancement implies that the die have boundry scan designed into them prior to being able to apply this concept to the MCM as a whole. At present there are only a small percentage of the die that have boundry scan designed into them. The time phasing of this enhancement will be driven on the availability of die with boundry scan.

16. Full metal deposition in MRC: This enhancement significantly reduces or eliminates the need for a wet plating operation. In this enhancement titanium would be deposited as is done now at GE, but the full thickness of deposited copper would then be followed by a titanium coating in the vapor deposition system. This eliminates the need to handle the parts between the vapor deposition process. From a throughput standpoint, product cycle time and fabrication labor are both reduced. The capital cost would be slightly higher (the difference between a plating line and a conveyorized MRC), but it would be offset by the reduced fabrication labor and cycle time. The uniformity of the metal thickness would be improved over the plating process due to the dynamics inherent in plating processes.

Risk: **Med** - A full study of the impact on cost would need to be completed to allow dollarization of the impact. A plating process for any metals would still be needed to selectively deposit (gold, tin/lead, etc.). Development work would need to be completed on the changes, if any, on the physical properties of the deposited metal.

17. Photo-imagable dielectric: This enhancement is a marriage of the dielectric and photoresist technologies. The goal would be to apply a dielectric that is UV light sensitive and to write images on the dielectric. The vias could be formed photographicly. The metal deposition step which is normally done could then be completed. This dielectric system could be done with either a mask or laser process, and it would be compatible with both the GE-HDI or chips last technologies. Presently, the photo-imagable dielectric systems are all liquids which require either spin or spray coating. This would change the capital equipment needs in the foundry, but the impact on fabrication labor could be substantial.

Risk: **Med** - Several companies have recently announced photo-imagable dielectric systems, but detailed data on the properties of the dielectrics are not known. Further study would be required to understand the effect on dielectric - metal and dielectric-to-dielectric adhesion. The problem of airborne contamination would again resurface and would also need to be reviewed.

18. Pre-tested die, die known dimensions: The pre-tested die issue has been discussed earlier in this report as well. An inexpensive method of die testing (either in the MCM foundry or at the supplier) will be critical in reducing the cost of the MCM. This is true for both the chips first and chips last MCM approaches, but more so for the GE-HDI approach. The need to control the die dimensions (X,Y,Z) is important to further reduce the substrate manufacturing effort. The thickness control of the die is critical from the substrate molders standpoint. If the die can be controlled to a given tolerance within a lot and from lot to lot then the molding operation can be further automated to reduce substrate costs. This would apply to all substrate materials, but the major impact would be related to the ceramic based and patterned substrates. In these cases special techniques would have to be developed to handle situations where the die change in depth.

Risk: **High** - Both of these enhancements require further control of the die manufacturing process and potentially require manufacturing changes. This will be difficult to accomplish until an infrastructure exists for the MCM market.

19. Die with bond pads larger: This enhancement is related to the enhancements discussed earlier on having the L1 pads on "grid" and on the mask process for layers 2 and above. This enhancement would eliminate the requirement for the Layer 1 pads on "grid" and would allow the mask process to be used on all layers of the MCM. This would further reduce labor and capital costs as discussed earlier.

    Risk: **High** - This will require a special design of the die to fit the GE-HDI technology. This can only be accomplished with very high volume die, for specific applications where die costs can be higher or for the cases where vertical integration within a company can be accomplished. TI is in a position to do this for the instances where it is the system integrator/designer.

20. High rate drill: The via drilling operation is the most time consuming operation within the GE-HDI process, with the exception of the substrate fabrication process (and potential enhancements to this have been discussed earlier). The mask process for layer 2 and higher, tied with the layer 1 pads on "grid" will reduce/eliminate the need for this enhancement. However, highly complex designs could force a need for a faster laser drill. These complex MCM designs might require 2 layers to get to "grid" and, therefore, double the amount of vias to be drilled. In high volume it could be necessary to have a faster drilling process both for cycle time and labor considerations.

    Risk: **High** - Technology does not exist yet to specify the machine much less build one. The initial laser writer/driller that will be purchased for the effort is at the state of the art (at a price that is affordable). Further knowledge would have to be gained prior to defining this laser drilling system.

4.5.2 Define Time Phasing of Enhancement Incorporation Into Product Flow

The time phase of the enhancements into the foundry is driven by several factors:

- Production volume and time phasing
- Process development
- Equipment availability and cost.

The driver to enhancement insertion will be production volume and product delivery schedules. Figures 4-38, 4-39, and 4-40 show three different enhancement insertion schedules depending on production volume based on the minimum, medium, and maximum business plan opportunities along with relative MCM costs based on those production volumes and enhancements.

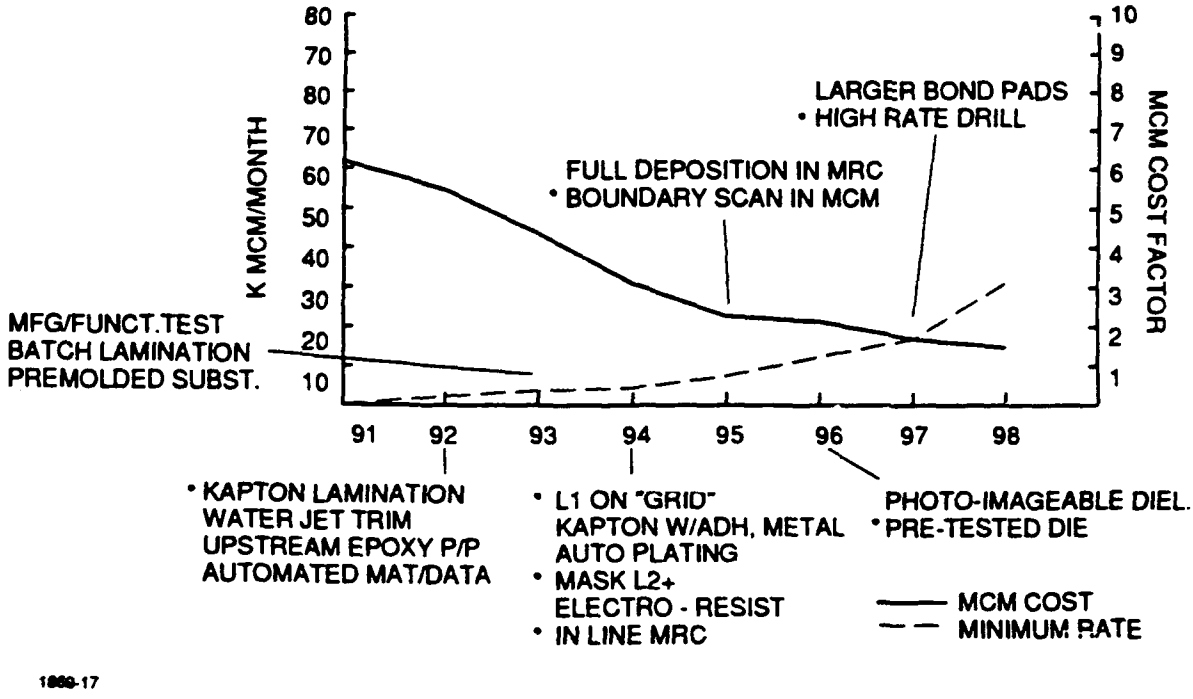


Figure 4-38. MCM Foundry Minimum Volume Business Opportunity

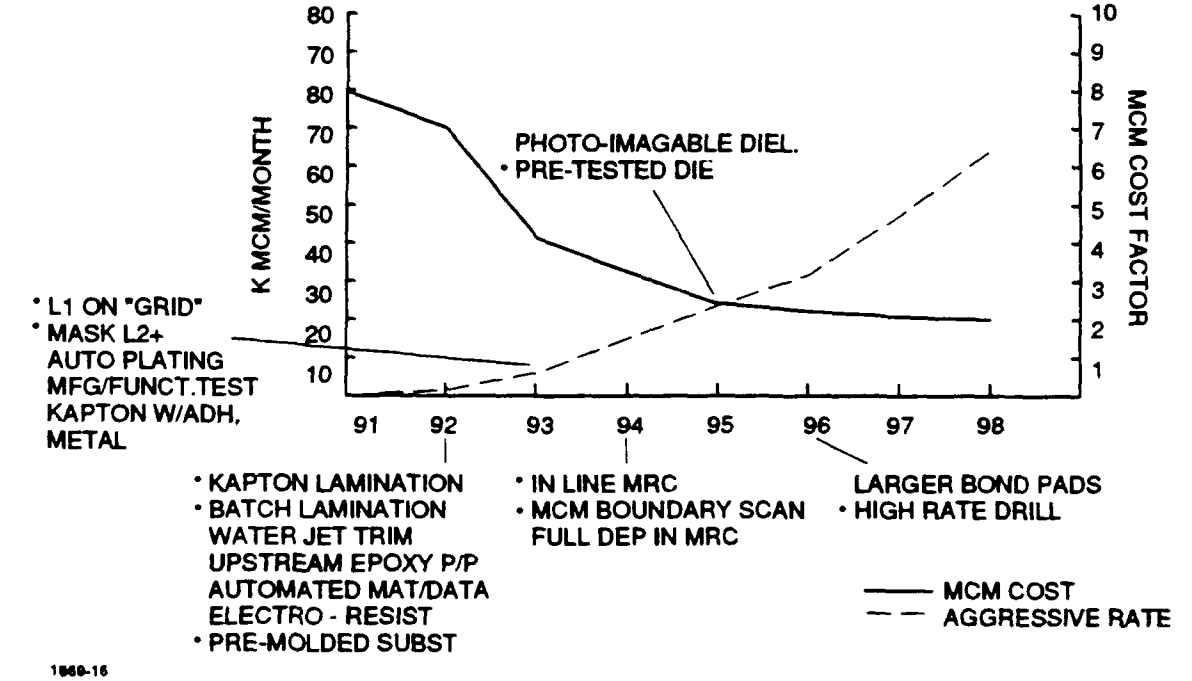


Figure 4-39. MCM Foundry Aggressive Volume Business Opportunity

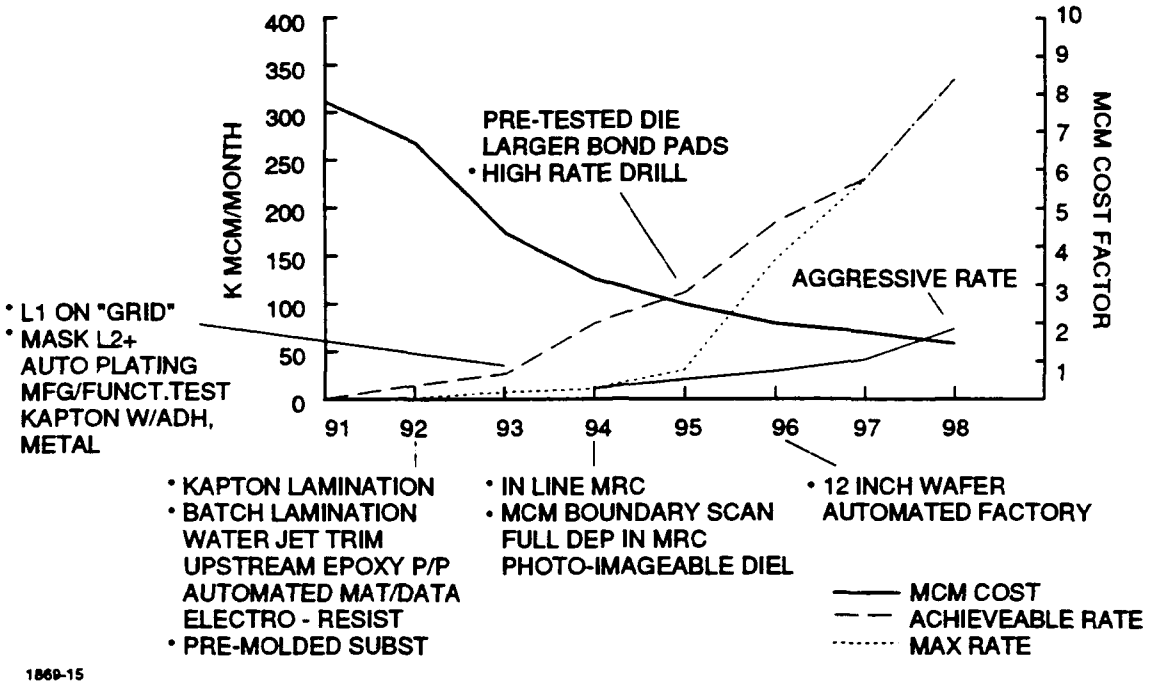


Figure 4-40. MCM Foundry Maximum Volume Business Opportunity

Figure 4-38 shows the minimum business opportunity. In this case the foundry would be grown off of the prototype factory. The following enhancements would be implemented immediately, with the other enhancements based on volume, development, or equipment availability concerns:

- Kapton lamination for all layers
- Water jet trim
- Upstream epoxy for pick and place
- Automated material/data handling.

All low risk insertions and allow the facility personnel the maximum time to learn the process.

Figure 4-39 shows the aggressive business opportunity. In this case the high rate foundry would be built at the most 6 months behind the prototype facility. This is a higher risk situation due to having little to no fabrication knowledge for this volume of MCMs, either chips first or chips last. The following enhancements would be implemented immediately, with the other enhancements based on volume, development, or equipment availability concerns:

- Kapton lamination for all layers (probably executed under 90-09)
* Batch lamination
- Water jet trim
- Upstream epoxy for pick and place

- Automated material/data handling
* Electrophoretic resist
* Premolded substrates multiple MCM's up with metal 0 applied and imaged

The items marked with an "*" are enhancements that would be installed immediately in addition to the minimum business plan enhancements. All of these are enhancements that impact fabrication labor, product cycle time or capital equipment costs and are no more than Medium risk enhancements.

Figure 4-40 shows the maximum business plan. Presently, the aggressive business opportunity enhancement insertion schedule should be followed until the business plan becomes more clear. This will reduce the risk from the capital expenditure and development cost standpoint. It is anticipated that in mid to late 1992 a review of the MCM market and TI MCM production capability will be made. With this information a plan can be made to react to the market requirements and manufacturing capabilities. A plan is shown to increase output to the maximum business opportunity by pulling forward enhancements starting in 1994 assumes market and manufacturing conditions warrant it. In addition to pulling forward the enhancements already defined, it will be necessary to define additional enhancements to increase output without just replicating the presently proposed capital equipment.

4.5.3 Capability of Package Suppliers to Provide Both Commercial and Military Packages

The TI foundry will fabricate multi-chip modules for both commercial and military customers.

In the non-military marketplace today, the bulk of MCMs are directed at the high-end segment of that industry, namely, mainframe computers and workstations and some limited applications for personal and laptop computers. MCM packaging for these applications, typically, is either high reliability hermetic military configurations or tailored designs for captive technologies. In both cases, the packages are costly and by no means offer any form of standardization. Plastic packaging methodology, or equivalent, is necessary for the commercial MCM market to meet TI's low cost objective. Existing single chip configurations, e.g., pin grid arrays, perimeter leaded carriers, area pad arrays, etc., can be re-tooled to allow for multichip mounting, and new encapsulation schemes can be developed which are compatible with individual MCM technologies.

To effectively address the utilization of modified packages and the development of new packaging for MCMs, for both commercial and military applications, a family of substrate sizes and package footprints (with complementary test sockets), a selected number of materials and a limited number of interconnect schemes will be established which are consistent with standards generated by the IEEE MCM Standards Task Force. The remaining tasks for the TI foundry will then be to (1) develop the methodology necessary to allow for "drop-in" packaging of conforming MCM substrates into the standardized set of commercially available packages, and to (2) coordinate the design, development, and manufacture of a family of new package configurations with various packaging vendors which are consistent with MCM standards.

The techniques for assembly of the TI-MCM substrates into "drop-in" packages involves traditional hybrid and semiconductor methods. The challenge of the second task is much greater. For example, for the GE-HDI technology vendor-supplied pre-molded cavity substrates (see paragraph 4.8) are a necessary technology enhancement to meet the low cost-high volume DARPA objective established for the TI foundry. Vendor activity has been initiated with two (2) companies, W.R. Grace & Company/Coors Ceramics and Ceramics Process Systems, during the SWAP study program in conjunction with the development of pre-formed substrates.

The packaging schemes planned for commercial MCMs are largely predicated by the needs of our customers. For mainframe computer and workstation applications, it is unlikely that hermetic level performance and reliability will be necessary. However, in automotive applications a very high level of reliability is required without hermeticity. Automotive electronics must withstand very harsh environmental conditions. In that industry plastic packaging is widely used, not only because of its cost advantage, but also because the reliability of today's plastic packages has improved significantly.

The GE-HDI technology appears well-suited to low cost packaging methodologies. A pre-formed cavity substrate will function as the package base. Interconnection of the die mounted on the substrate to I/O pads on its periphery will be by means of the HDI overlay process, thus, eliminating the need for wirebonding to a secondary package. Several substrate materials will be amenable to the TI foundry technology, including plastic, silicon, ceramic, and organic or metal composites. The next step is to provide a method of sealing the substrate from the environment. Possible techniques under investigation to accomplish this include: epoxy mounting of an opaque lid onto an integrated substrate (Figure 4-42), plastic encapsulation of the substrate by injection molding, and protective overcoats like the Dow Corning SPEC coating or their Q3-6646 silicone gel. The degree of environmental and mechanical protection that these methods offer might also be suitable for certain military applications.

Military MCM packaging typically requires size and weight limitations, extended performance and robustness of design, and space environment reliability. The integrated hermetic package scheme developed for the GE-HDI multichip module technology, illustrated in Figures 4-41 and 4-42, appears ideally suited to satisfy these military needs and also to address the DARPA low cost objective.

The TI foundry will meet the demands of all military customers, including packaging substrates in various multilayer ceramic and metal can "drop-in" packages. These packages, however, are either very expensive or do not take full advantage of the fabrication technology. The integrated hermetic configuration allows for both the maximum level of 26 performances, by eliminating secondary package interface, and an opportunity at significantly reducing the cost of cofired multilayer packaging.

As mentioned earlier, a family of integrated hermetic packages will be developed for the TI foundry consistent with standards established by the IEEE MCM Task Force. This will not only allow for cost reduction derived from lesser tooling and test fixturing needs, but

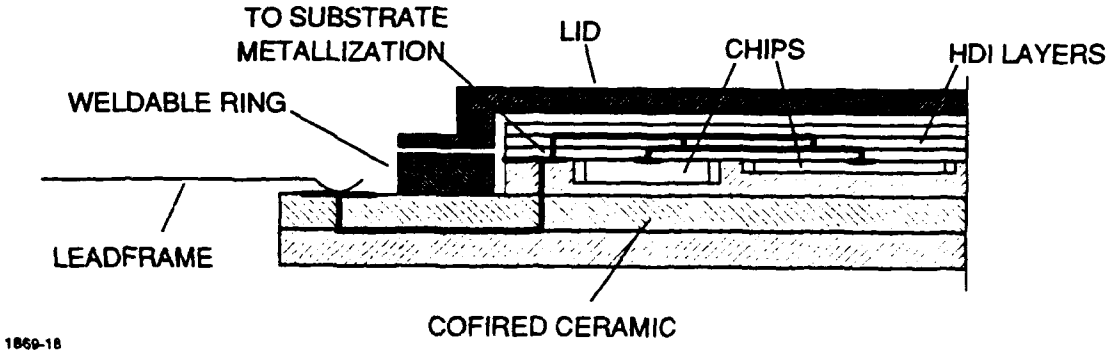


Figure 4-41. HDI Integrated Hermetic Package Planar Multilayer Weldable Ring Configuration

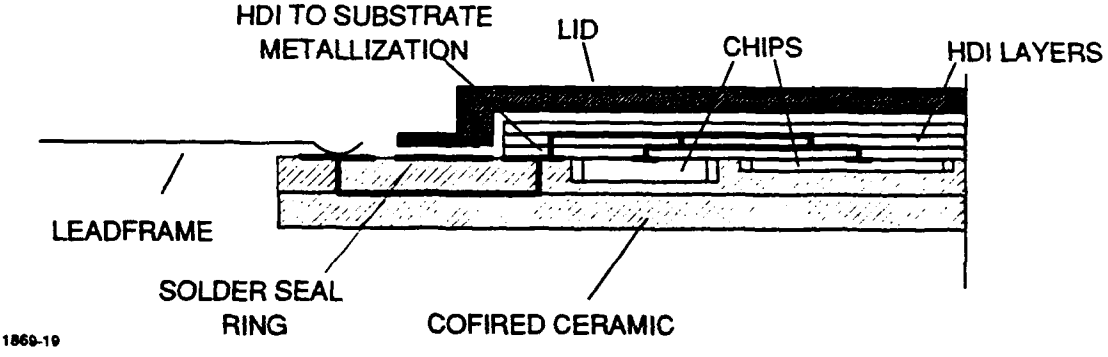


Figure 4-42. HDI Integrated Hermetic Package Planar Multilayer Solder (or epoxy) Ring Configuration

also help eliminate the use of custom packages, which is of paramount importance if the cost of MCM fabrication is to be driven downward.

4.6 FACILITY AND EQUIPMENT PLAN

A major emphasis of the Foundry Development Program is to provide the foundation upon which a viable, profitable business is built. This is accomplished by weighting business decisions against customer needs and start up risks.

The initial foundry will provide low volume manufacturing capability to serve the initial MCM market requirements. The startup facility will be matched to market demands. The growth of the MCM foundry from the startup baseline to the high volume, low cost factory will be market driven. This growth strategy will provide balance between market need and foundry risk. As the projected business plan continues to evolve, the facility growth plan may change, and near term risk will become better defined. Implementing a flexible

market driven growth plan allows facility growth to be accelerated as market segment penetration develops.

4.6.1 Facility Modularity

The foundry will evolve through a multi-phased program designed to maximize efficiency. The goal in the early stage is to move from a laboratory prototype environment, where the process was developed, to a formal manufacturing environment with improved capabilities. The emphasis in the implementation of the high volume, low cost addition to the baseline facility will be to increase the production rate, reduce manufacturing cost, and finally to reproduce the facility as required to provide total production capacity matching market opportunity.

Phase I of the plan is the basic capability phase. This serves as the startup operation to mature the processes. During this phase, the processing techniques developed by the laboratory scientists and technicians are evaluated and enhanced to improve the robustness of the processes. Part of this phase includes research and development to introduce modifications to improve manufacturability. The objective of this phase is to transfer the baseline process from its current environment to a formal manufacturing environment and verify low volume production capability.

Phase II of the plan is to ramp up production. This phase begins prior to production requirements exceeding the capacity of the initial foundry. New equipment is added in high usage areas to balance the line. This process continues as firm production requirements continue to increase due to continued growth in market share.

Utilizing the two phase approach, the MCM foundry is designed to function as two factories in one. Factory number one has the baseline capability (see Figure 4-43). This portion of the foundry supplies low volume, high part number mix and rapid reaction production modules. Factory number two is constructed adjacent to factory number one and serves the high volume market (see Figure 4-44).

The role of the baseline foundry changes as the high volume foundry begins to mature. The baseline foundry focus shifts away from providing limited capability for all products and development of new products and processes to providing a facility capable of:

- Rework of expensive designs
- Quick turnaround prototyping for new designs
- Low volume production area for military applications
- Process improvement laboratory for new technique evaluation.
- Rapid prototyping capability for military or commercial

The high volume foundry will continue to use portions of the baseline capability during the expansion to avoid another large capital investment. New equipment and trained operators are added as needed to provide a smooth transition.

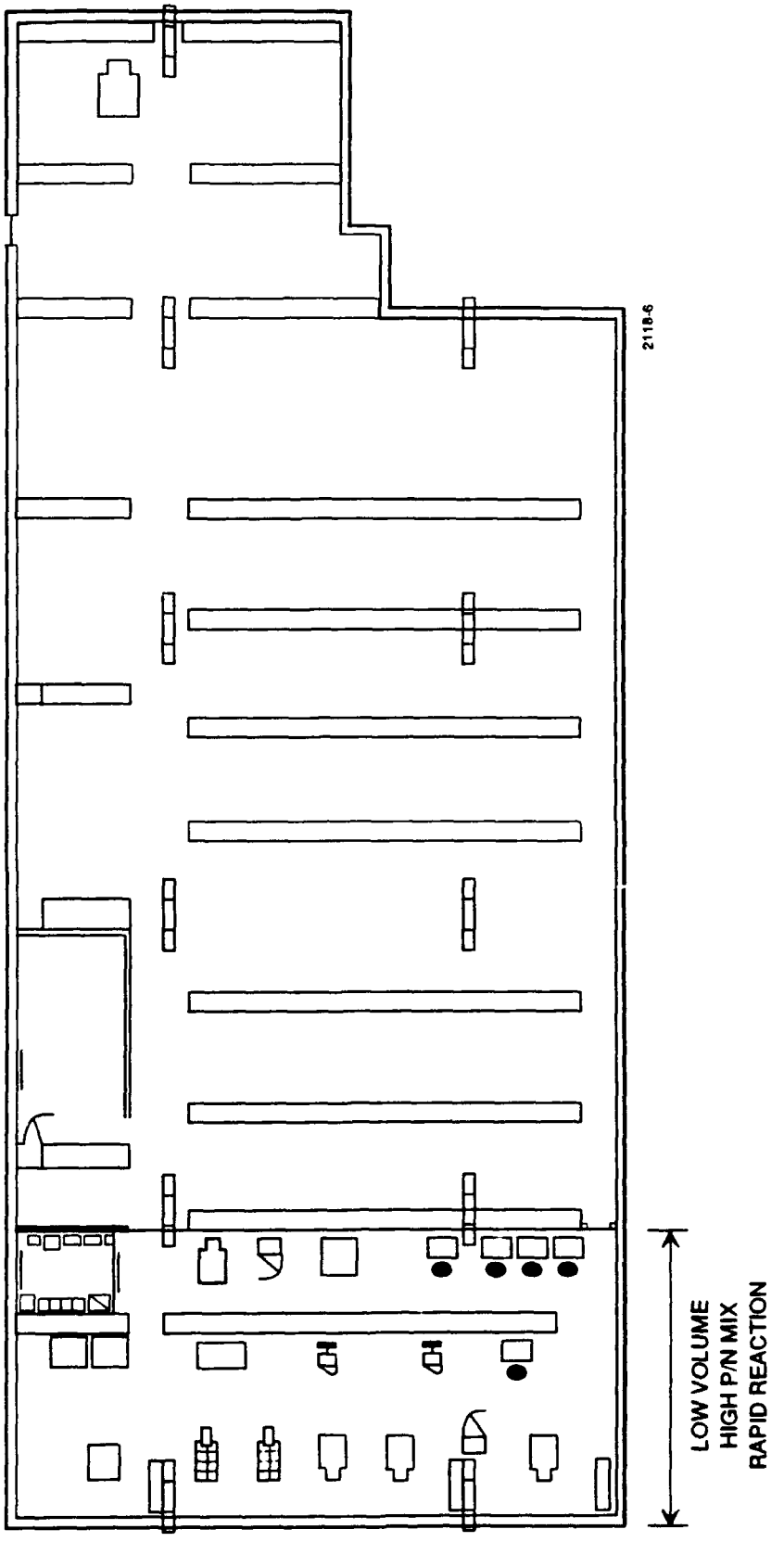
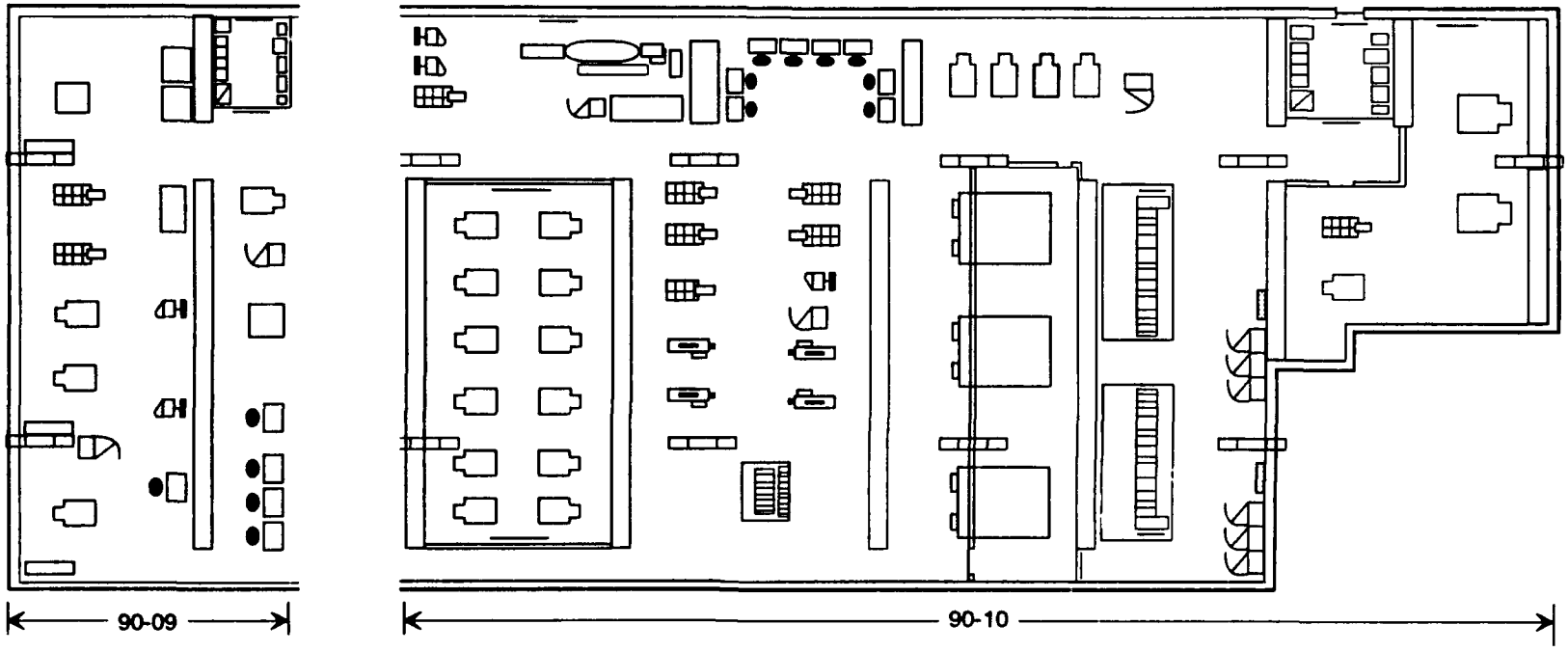


Figure 4-43. DARPA Baseline Foundry (1K/month)



INITIAL MERCHANT FOUNDRY
CUSTOMER PRODUCT MIX

- HIGH MIX PART NUMBERS
- SMALL VOLUME RUNS
- HIGH PERFORMANCE APPLICATIONS
- PERFORMANCE DRIVEN

TRANSITION TO HIGH VOLUME CUSTOMER PRODUCT MIX

- GREATER THAN 100 UNITS PER PART NUMBER
- LOW COST MANUFACTURING
- MEDUIM/HIGH PERFORMANCE APPLICATIONS
- INTEGRATED DESIGN TO MANUFACTURING
- RAPID PROTOTYPING SERVICE
- QUICK DESIGN TO MANUFACTURE TURNAROUND

2118-8

Figure 4-44. MCM Foundry Elements

The final stage of the foundry expansion program is reproduction of the entire facility. This may be done for several reasons after the technology has fully matured. The following reasons may dictate another foundry location:

- Proximity to customer
- Reduced labor rates
- Import/export regulations
- Continuing expansion of market demand.

4.6.2 Basic Capability

Basic capability is described as the minimum amount of equipment required to build a single MCM. Basic capability is always the most expensive option on a per part basis for direct labor, capital equipment, floor space, and support.

In a startup operation, the initial business plan often reflects very limited production requirements. Capital equipment purchase decisions are governed by these requirements. Initial capital investment for an entire start up facility is relatively high, while the pay back cycle for low volume production is over a long period. Therefore, the decision to purchase highly automated equipment is governed by asset recovery based on the market demand.

4.6.3 Foundry Expansion

It is anticipated that production volume requirements will eventually force the need to expand beyond the basic facility. Again, this expansion will be based on a developing business plan and through close consultation with existing customers and constant evaluation of the market demand.

If the market growth is slow, asset recovery time may continue to drive capital equipment purchases toward less expensive equipment with limited automation. While this keeps the per part production costs high it does minimize the profit and loss risk. While the short term profit and loss risk is minimized, the long term risk is to loose all competitive advantage. However, if growth is rapid, asset recovery time decreases. This provides a flexible environment for the foundry to begin looking at the timing of automated equipment and process development programs.

Insertion of automated equipment provides the foundry the improved process control capabilities needed to reduce the cost of the final product. These improvements raise capital costs in the initial stages but can ultimately reduce the per part cost significantly. In addition, process and materials improvements can be added to the foundry. These new processes and materials are aimed at producing significant yield improvements and reducing per part costs.

4.6.4 Modeling Foundry Production

Factory process modeling techniques provide the means to evaluate and plan the facility equipment, space and capital requirements. Modeling has been used extensively throughout this study.

4.6.4.1 Static Model. A production process model is the first step in determining the type of equipment required for a foundry. The model must be flexible enough to allow for "What If" possibilities to be explored. A static spreadsheet is developed from a process flow document. The model lists each step in the production process in the order of process flow.

4.6.4.1.1 Model Inputs. The spreadsheet model reflects a direct correlation between a number of inputs including production quality, expected process yield, labor and equipment required for each process step. In turn, each input has an effect on the final calculation.

The first input to the model is the actual number of MCM'S which must be produced in a day. An expected process yield is used to determine the number of extra parts which must be produced to achieve the necessary output. The number of MCM's per carrier is an important consideration in these calculations, as they are a factor of total module cost.

Each process step requires specific information about the direct labor associated with that step. The model assumes that an operator is always required for setup and load, but only a percentage of the actual processing time may require the operator's attention.

The model reflects a listing of the generic equipment for each process step. The processing time for each piece of equipment is broken into detailed subgroups. Areas taken into account are:

- Setup
- Load time
- Lost size
- Carrier specific operations
- Substrate specific operations

4.6.4.1.2 Model Outputs.

4.6.4.1.2.1 Major Element Processing Time. Model outputs combine the data for each major sub function in the process flow to determine total machine time associated with that function for the entire run. This output is divided by the number of MCMs produced to determine the amount of processing time per MCM for each major sub function of the process.

4.6.4.1.2.2 Total Non-exempt Labor. The model also totals the direct labor required for both the function and the entire run. Total for each group can again be divided by the number of MCMs processed to determine the amount of processing labor required by each major process sub grouping per MCM. Total labor for all the sub-groups can be divided by

the number of hours in a shift (7.5 Hr/shift) to determine the number of operators required to support the production requirements.

4.6.4.1.2.3 Machine Processing Time. Final information provided by the static model is the total processing time by machine type. The model totals machine utilization time for each type of equipment. This number is then used to determine the number of machines required

to achieve a given production rate over a given number of hours. The number of machines multiplied by the cost per machine yields the rough capital investment required for processing equipment.

4.6.4.2 Dynamic Modeling. Static modeling is a good technique until the factory starts to approach capacity. At this point, it is necessary to use the more sophisticated dynamic modeling concepts to fully understand the factory. The SWAP team used the commercial software package WITNESS™ to configure a model of the MCM foundry. It should be noted that factory modeling software developed under the Air Force/DARPA funded MMST program at TI was not available at the time of this study. However, this capability can be very useful for future modeling requirements.

The dynamic modeling software provides the capability for equipment operations to be modeled based on individual pieces of equipment, rather than generic equipment types. This tool permits examination of adding equipment to enhance process capabilities at specific points. Working against the baseline business plan the TI-GE team performed "What If" studies to better understand the relationship between the time phasing of automation, manufacturing cost goals, and capital asset recovery.

An example of this study technique is demonstrated in the procurement vapor metal deposition equipment. The static model indicated that the foundry would need to purchase the second deposition machine by the beginning of the third production year. Two more machines were required in the fourth, year and five machines in the fifth year. Alternately, the dynamic model suggests that purchasing a highly automated sputtering machine, with increased capital cost, would provide 2.5 times the throughput with less than half the direct labor. This would ultimately be the most cost effective approach. These are the types of facility and capital issues that will be addressed as the volume through the factory increases.

4.6.4.2.1 Example of Dynamic Models. Several factory models were run to compare the capital cost, cycle times and relative sensitivities of each. Four models were examined for the 1000 substrates per month (Table 4-3) and the 15,000 substrates per month rates (Table 4-4). These models are: Baseline (GE-HDI process), Baseline With Partial Enhancements (BWPE), Baseline With Full Enhancements (BWFE), and Chips Last.

The first model is the baseline. This is the GE-HDI process, using 4 substrates per carrier on a 6-inch carrier, and 4 carriers per lot. This is the model that the others will be compared against.

TABLE 4-3. 1K/MO MCM INTERCONNECT FABRICATION STUDY

	MODEL			
	BASELINE	PARTIAL ENHANCEMENTS ADAPTIVE DRILL	FULL ENHANCEMENTS MASK PROCESSING	CHIPS LAST
SUBST/CARRIER	4	7	7	7
CARRIERS/LOT	4	4	4	4
OUTPUT/MO	1,000	1,008	1,009	1,011
HRS/SUBST	3.05	1.00	1.10	2.20
DIR FAB PEO	22	8	8	16
DIR SUP PEO	10	5	5	8
CYCLE TIME (D)	8.8	3.2	4.6	4.7
CAPITAL $FACTOR	1X	1.6X	1.3X	1.1X

TABLE 4-4. 15K/MO MCM INTERCONNECT FABRICATION STUDY

	MODEL			
	BASELINE	PARTIAL ENHANCEMENTS ADAPTIVE DRILL	FULL ENHANCEMENTS MASK PROCESSING	CHIPS LAST
SUBST/CARRIER	4	7	7	7
CARRIERS/LOT	4	12	12	12
OUTPUT/MO	15,000	15,120	15,141	15,162
HRS/SUBST	2.90	0.40	0.415	0.80
DIR FAB PEO	311	44	45	87
DIR SUP PEO	40	25	25	35
CYCLE TIME (D)	8.8	3.2	4.6	4.7
CAPITAL $FACTOR	1X	.86X	.69X	.51X

The next model (BWPE) represents the baseline process with the enhancements of laser adaptive drill and image mask. Adaptive laser drilling is performed on all layers, as in the baseline GE process, except the pattern image step is replaced with mask imaging. Instead of using the laser to pattern the image, photoimagable resist is applied and exposed using a S/C style stepper. This process assumes that the pad layer on layer 1 is large enough to handle chip movement. Also, the number of substrates per carrier has increased due to utilizing an eight inch carrier.

The third model (BWFE) represents all enhancements mentioned above with adaptive laser on layer 1 and mask vias and image pattern for layers 2 through n. This process adaptively laser drills vias and circuit patterns on layer 1 to get layer 1 pads to grid. Metal deposition on layer 2 through n dielectric is followed by via formation using via mask and a non-isotropic plasma process and mask imaging for circuit lines on layers 2 through n.

The last model is a model of a chips last approach. This model describes a process which uses a full mask formation of vias and circuit patterns on all layers followed by assembly of die to the completed MCM's. Metal deposition on dielectric is followed by via formation using same processes mentioned above.

The first comparison is at the 1000 substrate per month level. There is no automation and few batch processes at this production rate. The work is highly labor intensive and equipment is geared for small lots. Except for the baseline, all use 7 substrates per carrier with 4 carriers per lot. The change to an eight inch carrier greatly reduces the amount of labor per substrate. Further, this alone helps reduce the number of people for the fabrication processes. The baseline capital is less expensive initially, but more labor intensive. The capital needed for the enhancements on other processes are more expensive, but the cycle time is shorter due to reduced equipment and inspection requirements. The enhanced models assume SQC and sampling techniques to reduce inspection time.

Capital equipment for the partial enhancement process (BWPE) is the same as the baseline, with the addition of steppers for imaging, electrophoretic coaters, plating lines, laminators, and a sputter-coater and laser. Capital for full enhancements (BWFE) is the same as above, less the additional laser. Capital for the chips last approach is the same as above, but without any lasers. The associated capital costs reflect these differences.

At the 15,000 substrates per month level, there are many improvements on all four models. There is more assumed automation, batch processing, less labor intensive equipment geared for larger volumes. Again, except for the baseline, all models have 7 substrates per carrier and 12 carriers per lot. The changes made to the models for large volume production include: carriers pre-molded with multiple MCM per each carrier, batch lamination introduced for the higher volume, and higher capacity plasma etching, sputtering, plating and imaging equipment.

The baseline capital at the 15,000 substrate per month level is the most expensive of the alternatives, and most labor intensive. The baseline uses 4 substrates per carrier and a small carrier. By going to 7 substrates per carrier (Table 4-5), labor hours per substrate are dramatically improved along with four fabricators needed. Further enhancing this model by adding faster laser for imaging, the labor per substrate is even less, with lower capital cost due to less lasers. This situation shows the sensitivity of the factory models to larger carrier sizes.

The third case study model at the 15,000 substrate per month level, the partial enhancement process (BWPE), uses three less lasers than the baseline causing the capital to be reduced and lower hours per substrate. The capital for full enhancements (BWFE) uses even less lasers, but one additional expose steppers. The capital is reduced but the hours per substrate are increased since there are more steps in the imaging process.

The final Case Study, chips last, requires no lasers. This approach showed the lowest capital investment, but the labor and cycle times are increased. This increase is due to the additional imaging steps.

TABLE 4-5. 15K/MO MCM FOUNDRY MODEL SUMMARY

	MODEL	
	BASELINE WITH CURRENT ADAPTIVE LASER DRILL AND LASER IMAGING	BASELINE WITH ENHANCED ADAPTIVE LASER DRILL AND LASER IMAGING
SUBST/CARRIER	7	7
CARRIERS/LOT	12	12
OUTPUT/MO	15,000	15,000
HRS/SUBST	0.47	0.395
DIR FAB PEO	52	44
DIR SUP PEO	29	25
CYCLE TIME (D)	4.22	3.95
CAPITAL $FACTOR	1.1X	.93X

The results of the models show that increasing the number of substrates per carrier decreases the labor hours per substrate. Enhancements by introduction of batch processing, automation and higher volume machines also lower cost. Furthermore, by adding high rate via drill and faster patterning lasers for the drilling and imaging steps, capital costs and labor can be reduced even more.

4.6.5 Leveraging Existing Technologies

The current GE-HDI multichip module is produced by a combination of processing techniques common to the manufacturing of integrated circuits (ICs), and advanced multilayer PWBs. The teaming arrangement between TI/GE brings a unique combination of skills to the MCM production foundry. GE's CRD center has provided the baseline MCM production technology along with an advanced material science background in polymer chemistry. TI provides experience in high volume production of both integrated circuits, and advanced multilayer PWBs.

The TI Semiconductor Division currently produces and packages more ICs than any other company in the United States. This is a direct result of special skills groups. An example is the capability within TI for advanced clean room design. This is discussed in greater detail in section 4.6.7.

Highly automated production facilities are a critical element of reducing manufacturing cost. TI has been directly involved in the design and manufacturing of advanced automation within the semiconductor industry. TI's automation group developed the first automated frontend, and owns the patents for computer controlled wire bonding and vision aligned bonding techniques.

The GE overlay process utilizes many of the same lamination, plating, and photolithography techniques as the TI advanced PWB facility. There is an opportunity for

combining the procedures for high volume PWB technology into the overlay process to further improve processing yield and productivity.

TI is also the contractor on the MMST program funded jointly by the Air Force and DARPA. MMST will provide a number of benefits to the semiconductor processing business. The individual machine processing cell concept would provide the high cleanliness and quality control required by an industry continually pushing technological limits.

In addition, the foundry can leverage off of TI's existing programs of Total Quality Management (TQM), including expertise in Statistical Process Control (SPC), and Just-In-Time (JIT) manufacturing techniques.

4.6.6 Processing Other MCM Products within the Foundry

In addition to quality and producibility improvements to the GE-HDI MCM process, it is important to support specific customer demands from a business perspective. The TI foundry must be able to provide assembly of all of the current MCM technologies with a minimal addition cost to the foundry. Most of the equipment required to process these other MCM types is common to the chips first technology, and will be available in the foundry.

As discussed earlier, the design and routing system used by the TI foundry, has proven the ability to route a design for either the chips first or chips last technology. Therefore, one design system will provide the capability for all the current technologies with no added cost.

Other technologies all require some form of photolithography, the exposure of a photo sensitive material, to image the interconnect patterns on substrates. In the TI foundry the adaptive patterning laser can directly image a part for low volume production, or image the pattern directly onto a photomask plate for direct printing in higher volumes. Under normal circumstances photomasks are long lead time items. This reduces the photomask fabrication process from several weeks to a few days. A chemical hood is required to develop the photomask plate, once exposed. The cost of this chemical hood will be approximately $50K.

Finally, chip placement for the other MCM technologies (TAB, Flip TAB, and Flip Chip) requires high accuracy. The accuracy required is +/- .001" with a theta of +/- .05 degrees. The pick and place machine selected for the TI foundry must have placement capabilities better than these requirements to meet the needs of the all mask process. There should be no additional cost associated with chip last placement.

4.6.6.1 Chips Last Substrate Technology. Other MCM technologies are designed around some form of silicon and polyimide substrate e.g. the interconnect medium. This substrate must be plated with metal and patterned in a similar fashion to the GE overlay process.

The current TI (SOS) technology, a Flip TAB approach, requires most of the same processing steps as the GE-HDI approach, with a different interconnect metal chemistry. The effect on the foundry will be different targets in the metal deposition equipment and a different etch chemistry for metal removal. The etch chemistry processing is of little cost

differential, if incorporated into the etch system during the design phase. The additional cost required is approximately $50k.

4.6.6.2 **TAB and Flip TAB Technology.** The TI-SOS process requires the incoming ICs to have gold bumps applied over the bond pads and Inner Lead Bonded (ILB) to TAB tape carriers. These operations are currently accomplished by another group within the TI Semiconductor Division (TI SC). The SWAP team sees no reason to replicate this technology or equipment at this time.

The TAB approach does require the addition of trim and form dies to excise the part from the tape carrier. These are product specific tooling issues which required for each new TAB assembly, and cost about $10k each.

The TAB type MCMs do require the addition of an OLB to attach the exposed tips of the leads to the substrate. This piece of equipment is readily available within the industry and would require additional capital of about $200k to implement.

TAB and Flip TAB MCM capabilities can be added to the initial foundry, in low volume, for less than $300,000 of additional equipment. In addition to adding assembly of TAB type MCMs, this equipment permits the foundry to image the photomask plates to manufacture the TAB tape. This capability combined with improved vendor relationships, could reduce the cycle time required to obtain TAB tape for manufacturing.

4.6.6.3 **Flip Chip MCM Technology**. Flip chip MCM technology is added to the foundry by including a solder plating system to form solder bumps on both die and substrates, and by providing a reflow furnace to form the eutectic bond. Cost of this equipment is approximately $100k.

4.6.6.4 **Wire Bonded MCM Technology**. The addition of a gold, or aluminum wire bonder to the foundry will provide the capability to produce Wire bonded MCMs for about $125K of additional equipment. This completes the matrix of equipment required to design and manufacture all current forms of MCM within one foundry.

This strategy will give the TI foundry the ability to provide any MCM customer with the type of product that best meets that customers requirements or preference for approximately $500,000 in additional capital above the investment needed for the baseline factory.

4.6.7 Foundry Layout

The preferred floor plan for any production facility would normally be an inline process flow which provides the most efficient processing environment. In the case of the GE-HDI process, this is not practical. The repetitive nature of the process requires that a piece of equipment be utilized in several different parts of the process. Therefore, similar processes will be grouped together in a work cell concept.

The goal of the initial foundry design is to provide a complete production facility for the technology insertion. Once that role has been completed and the high volume foundry starts to ramp up production, the role of the initial foundry changes to provide production support for low volume products, rapid prototyping, rework, and low volume military products. The initial foundry will also serve as the process improvement laboratory for the entire foundry.

The high rate factory will be developed while the adjoining initial foundry continues to operate. This strategy provides the advantage of producing product while processing steps are enhanced for high volume production.

The foundry technician, engineering support, and design office areas will be located adjacent to the foundry to provide rapid reaction to problems. The incoming material, substrate fabrication, test, and shipping areas will also be located close to the foundry. Therefore problems and possible solutions may be communicated quickly.

The goal of the overall foundry design is to get "ART TO PART" to the customer as quickly as possible.

4.6.8 Facility Installation Costs

The facilities installation cost are usually significant for any startup factory. Typically, costs include design and construction of office areas, fabrication cleanroom floor space, support areas, incoming material receiving, utilities, and test areas.

The major facility expense will be due to the construction of the manufacturing cleanroom. The current GE design rules call for line widths of 39 microns, and 51 micron spaces. GE's experience has been that large particles 15 to 20 microns and larger are the most damaging, while particles of 1 to 5 microns are not a concern. Planned extensions of the technology require 20 micron lines and spaces, or smaller. A cleanroom designed around current technology requirements will be inadequate for future MCM applications.

MCM technology has a different contamination problem from that of an IC processing frontend. Silicon slices used in producing ICs usually contain hundreds or in some cases thousands of circuits, while MCM carriers will contain between 2 to 20 modules. A silicon slice containing 400 memory ICs exposed to a total of 20 particles would contaminate 5% of all the circuits. In contrast, 20 particles could reduce the yield of an MCM carrier to 0%.

The particles required to damage memory circuits are approximately 1/300 of the size required to damage a MCM. This introduces the concept of defect density which is not sized related. Calculations indicate that a defect density of .006 defects per sq. cm. could result in a 15% yield loss on a 7 module MCM carrier.

It is for this reason that a Class 10 clean room, for 1 micron and larger particles is specified. A Class 10 cleanroom is defined to have less than 10 particles per cubic foot that

exceed 1 micron or larger. To create a cleanroom of this quality requires advanced cleanroom technology, a significant capital investment, and continued maintenance.

Significant costs are incurred because every aspect of the room must be considered during the design. For examples, blowers must be sized to meet flow requirements for the size of the facility, and the back pressure of the filters selected. The paint on the walls cannot create particles by flaking off, and shelves are made of mesh material so air flows through instead of providing a place for particles to collect.

In addition to considering cleanroom construction, special cleanroom clothing must be provided to reduce particles brought in from the outside. These clothes are made of materials that do not create additional particles by shedding. They must be washed in special chemicals that do not create flaking from soap residue. Clean room clothing for this type of facility includes: complete hair cover, face cover, gloves, and boots. The only exposed part of the skin is the area around the eyes, which requires safety glasses.

The facility must provide separate areas to change from street clothes to clean room clothes, as well as a high velocity blower area separating the changing room from the clean room. This "air shower" removes particles that are loosely attached to the special clean room garments.

One area of concern is that semiconductors are very sensitive to Electro Static Discharges (ESD). Static electricity is a problem for electronics when allowed to discharge. When this happens, very high voltages of short duration can destroy circuits immediately or damage them to the point they will fail at a later time. The easiest way to prevent ESD is to avoid the static charge buildup. Conductive floor tiles, wrist straps, and conductive work surfaces are utilized to dissipate charges as they form. Ion charge generators can be located near the ceiling and at some work surfaces to negate charge formation. Humidity must also be controlled to reduce static charge build up caused by movement through the dry air.

The cleanroom design must take into consideration chemical vapors due to possible explosions. Areas of the clean room will require special exhaust and explosion proof design features to eliminate this hazard.

The use of the adaptive laser introduces a series of requirements which are necessary to protect the operator. The laser must be kept in a closed area with restricted access. While the laser with the safety cover attached is within FDA Class IV standards, the covers must be removed to repair or calibrate the system. This requires the laser to be located inside a room, with safety interlocked doors, to shut down the laser power when the covers are removed.

In addition, laser accuracy requirements are such that constant temperature and humidity levels are required to keep the beam from drifting. Additional equipment and controls must be provided to maintain this temperature and humidity within the laser room. The laser room and support structure must be checked prior to facility construction to isolate the laser from any vibration caused by the facility or its surroundings.

Any foundry will require a variety of electrical power, gas, liquid supply and drain systems.

The foundry has a variety of electrical requirements, ranging from standard 115vac @ 5 amps up to 408vac 3 phase, 30 amps for the adaptive lasers and metal sputtering equipment. There are also recommendations for isolated, and/or filtered power by some of the equipment manufacturers.

The power requirements for the adaptive laser alone is 408vac 3 phase, 10 amps in normal operation, and 30 amps for the start up surge. A foundry producing 10,000 modules per month requires 10 adaptive laser plotters and drills. The design of the electrical system in the foundry is of significant importance.

The MCM foundry gas delivery system has special requirements in a Class 100 clean room. High purity gas for frontend use requires electro polished stainless steel (EPSS) tubing. Copper is not used because over time the fluxes used and the tin-lead solder can leach out and produce damaging particles. Plumbing with EPSS tubing is about 10 times the cost of standard copper plumbing.

Deionized (DI) water is supplied to the foundry for cleanup in the plating areas. The final rinse of DI water is necessary to remove any contaminates that could later corrode the metal system. The DI water system at TI is capable of supplying a sufficient amount of 12 meg-ohm water. This is an increase in cost of approximately 5 times of standard city water.

Some equipment in the foundry, particularly the adaptive laser and metal sputtering machines, require additional cooling. Recirculating chilled water (53°) is preferable to city water for several reasons. First, it is approximately the same cost as city water, secondly it is colder so less is required, and finally there is no waste or added sewer cost.

The current MCM manufacturing process requires acids, solvents, and heavy metal plating solutions which require special drains, and chemical recovery. Furthermore, the gold plating line requires the use of cyanide. Every piece of equipment within the foundry is required to meet both safety and environmental standards. Sump pans are placed around all plating processes in case of leaks, along with a safety shower, and oxygen masks are all part of the design of the manufacturing facility.

When all areas of the foundry are considered, the projected cost for designing and building a 2000 sq.ft. manufacturing facility with 2000 sq.ft. of support area capable of producing, testing, and shipping 800-1000 MCMs/month is approximately $2.5M, while the 10K MCM/month is about 6 times that cost. This assumes support functions such as gas delivery, DI water processing, and some chemical recovery are already present, and the facility building currently exists. TI has an advantage in these areas, as well as the engineering experience to build a high volume foundry.

4.6.9 Non-Recurring Startup Costs

The non-recurring startup costs for the foundry are in excess of the total capital and facilities costs of implementing the baseline technology. Some of these costs are partially offset by the DARPA MCM Merchant Foundry contract in the early stages, like the technology transfer, facility development, and equipment procurements efforts. In the long term these costs will continue as the foundry grows into high volume production.

The technology transfer is a significant portion of non-recurring costs for the new foundry. For the GE-HDI technology transfer of this magnitude, several members of the TI foundry insertion team will travel to GE in Schenectady, New York to become familiar with every step of the process. This team will be composed of CAD designers, engineering support personnel, and operators.

The CAD designers must learn the new system developed by TASK Technologies and the interactions with the various HYPACK tools. The systems engineering support personnel must become familiar with the various data formats and their interaction with the equipment. They are also responsible for the transition of the PROMIS™ system from the GE facility to the TI foundry.

The operators and production support staff will learn the HDI manufacturing process. They must become familiar with all aspects of the fabrication process. They will be required to learn the operation of equipment and how to distinguish processes that are operating correctly from those that are out of specification.

In Dallas, a portion of the team will be responsible for the development of the cleanroom facility described earlier. Specifications and planning of the layout will require a considerable effort as does the overseeing of the construction effort. Administration and support areas must be considered during this construction phase.

Equipment procurement as described earlier is a lengthy process requiring a considerable amount of effort. While some pieces of equipment are almost off the self items, some like the laser, plating systems, and pick and place machine require almost full time effort.

Once the initial foundry is up an running the majority of the effort shift to improving the process. It is this process development effort that will be the key to the extension of the foundry to the enhanced low cost, high volume facility. Existing process must be hardened, processes monitoring tools must be developed to insure consistency. New process must be investigated to improve productivity and overall yield.

The growth of the foundry is marked by repeating cycles of many of the non-recurring efforts mentioned above. The cleanroom will continue to expand, new equipment will be purchased to increase production, and improved processes will be developed to reduce costs and improve yield.

4.6.10 Duplicating Critical Capital

During the initial year of operation, the foundry will function with only 1 piece of each type of equipment. Therefore, machine downtime will be critical. While planning for routine downtime is essential to machine maintenance, no amount of planning can offset the catastrophic failure which leaves a piece of equipment offline for an extended period of time. A failure of this type effectively blocks production, since no materials can proceed past the breakdown point.

The foundry cannot afford prolonged downtime for any one piece of equipment. This prolonged downtime disrupts production. Equipment should be added when a critical load level is reached, above 75%. Production problems, caused by excessive downtime involving equipment that is below the critical usage level, may be resolved by using overtime.

4.6.11 Production Yield Versus Capital Equipment

Final product yield, the percentage of shippable parts produced vs. the total number of parts started, will have a significant effect on the capital equipment requirements. In the TI foundry, a yield loss is offset by processing additional parts, (example: 125 parts must be processed at 80% ATY to obtain 100 shippable parts). Whether the interconnect overlay is reworked or the entire part be discarded, the effect on the foundry is the same as processing additional product.

Using the static 10K/month model and starting with 100% yield, the ATY was reduced by 5% per run. The equipment costs required to fabricate parts increased by 70% when the yield decreased from 100% to 50%. In addition, direct labor increased from 2.14 hr/MCM to 3.65 hr/MCM, operators from 130 to 222, and support personnel from 39 to 67 (assuming 30% support). Similar increases are expected for chemicals, processing materials, and floor space, all with an associated cost increase to the percentage of shippable product.

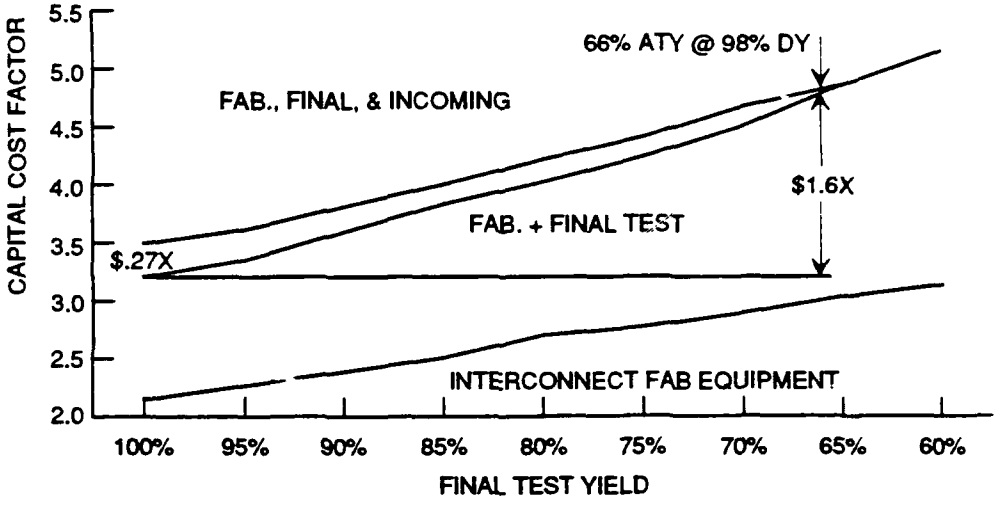
The primary contributor to yield loss could potentially be the effect of incoming IC die yield. Assuming that 98% of the pretested die received from the vendor are Good Electrical Bars, (GEB), an MCM with 6 ICs will have an ATY of only 88.5% ($98\%^6$). MCM with 20 die will only yield 66.7% and an MCM with 35 die yields 49.3% assuming there are no other items contributing to yield loss.

It is apparent that 98% GEB is not good enough. Steps must be taken to improve the quality of IC die received. The easiest is to have the vendor improve testing methods at final probe test. Dies are easily tested in the slice format, and handling is reduced. The foundry must provide incoming test for some ICs, since not all IC vendors will be able to improve testing.

For analysis a lower ATY of the final product also requires more modules to be tested to find the unacceptable ones. Assuming that the amount of final test equipment required is equal to the inverse of ATY (example: an 50% ATY requires testing of 200 modules to obtain 100 good modules). Final test for a MCM requires a board level test

capability, which is typically much more expensive than a single IC tester. Additionally, support levels are also much higher since the generation of test programs for MCMs will require much more labor than for the individual ICs.

Figure 4-45 illustrates the effects of incoming die yield on the total capital equipment required by the foundry. The effect is most obvious as the number of die/MCM increases and as production quantity increases. This figure is for 10,000 MCM/month with 20 ICs each, with incoming die quality of 98% GEB.



ASSUMPTIONS:
- 10K MCM/MONTH OUTPUT
- 20 IC's/MODULE-MIDPOINT OF SURVEY COMPLEXITY
- 2 INTERCONNECT LAYERS
- ALL DEFECTS ARE THE RESULT OF DIE YIELD
- DOES NOT INCLUDE INTERCONNECT YIELD FAILURES
- CALCULATED USING STATIC MODEL

2116-1

Figure 4-45. Capital $ Versus Final Yield

Lower Line: Total amount of interconnect fabrication equipment required as a function of module yield.

Middle Line: Module fabrication equipment plus final test equipment costs as a function of module yield.

Upper Line: Total fabrication, incoming test, and final test equipment costs as a function of module yield. The middle and upper lines converge at the 65% point ($66.7\% = 98\%^{20}$).

Discussion: The TI foundry requires a $3.2X cost factor in capital equipment to fabricate and test 10K modules/month with 100% yield. Assuming 98% incoming die yield, the final ATY becomes 66.7%, and requires $1.6X cost factor in additional capital equipment. The addition of 10% for incoming test equipment to improve die yield to 99.9% with a

resulting ATY of 95% on finished modules reduces the additional fabrication and test capital equipment cost factors from $1.6X to $0.1X.

4.7 QUALITY AND RELIABILITY PLAN

The concept of quality and reliability in industry today must be the responsibility of all functions within a company and, therefore, must be driven by upper management. The Total Quality Management (TQM) methodology is consistent with this philosophy and a goal of nurturing an attitude of continuous improvement within the TI-MCM foundry.

What is TQM? Several books have been written on this subject, but a partial summary is that it is a methodology that brings together all of the established quality practices, e.g., Just-in-Time (JIT), Statistical Process Control (SPC), Quality Circles, concurrent engineering etc., under one name and with a single direction. The common thread that is evidenced in these books is that one piece of the system cannot work without the others. The TQM approach abandons such traditional means to quality as inspections and corrective action, specification conformance, and the assignment of the quality control responsibility to a single function in favor of such proactive measures as designing for reliability, streamlining of fabrication, in-process control, and total employee involvement in quality objectives.

At TI, several examples have existed where some quality measures were implemented, but without a total methodology in place. For example, JIT without SPC resulted in a factory that was continually stopping due to process related problems that could not be resolved because data process control derived from SPC was not available. When SPC is implemented without JIT, processes were shutdown in order to bring them under control (i.e., to within control limits not just specification limits). Both of these examples resulted in reduced output and higher product cost.

The TQM roadmap proposed for the TI-MCM foundry will involve the following:

- Customer requirements definition
- Communication of TQM elements to customer
- Conversion of customer requirements into manufacturing methods
- Translation of manufacturing methods into efficient fabrication processes
- Determination of whether existing processes satisfy needs
- Controlled procedure for initiating process change
- Demonstration of control of all processes
- Evaluation of product to ensure conformance to customer requirements
- Validation and qualification of manufacturing processes
- Periodic audits of manufacturing facility to assure procedural and product integrity
- Continual communication with customers on their perception of our product and to suppliers on material requirements.

The startup phase of the MCM foundry presents a major concern in following this roadmap. At this state in MCM development, there are only a few loosely defined DoD/ industry-wide requirements; further definition of these requirements is needed. TI/GE is very interested in assisting in the development of these requirements as part of a DoD/industry-wide team. This team needs to have members from military services, commercial users, raw material suppliers, Academia, National labs and MCM fabricators. It is in the best interest of all concerned that a clear and concise set of requirements be defined that meet the end users needs. These requirements will then lead to standards and specifications, tailored for MCM's, both for military and commercial application.

In work pursued previously at GE for their prototype MCM facility under DARPA, AFWL and for both internal and external GE programs, and during the study phase activity of this program, groundwork has been laid that addresses many elements of a comprehensive quality plan. Included in this work was activity directed at the very important overall objective of establishing the TI-MCM foundry as a qualified supplier for both commercial and military customers.

In this approach, the concept of a qualified manufacturers list (QML) of MCM suppliers, similar to both the monolithic and hybrid world, will be endorsed for the new TI foundry. In preliminary work that GE has been involved through the JEDEC 13 JC 13.5/13.6 hybrid microcircuits committee and via interface with the IITRI Reliability Analysis Center and Rome Laboratories (previously RADC), initial steps have been taken to define the GE/TI-MCM technologies in appropriate military specifications. GE/TI and the industry team would hope to continue this effort and have the TI foundry serve as an "alpha" site for MCM facility qualification.

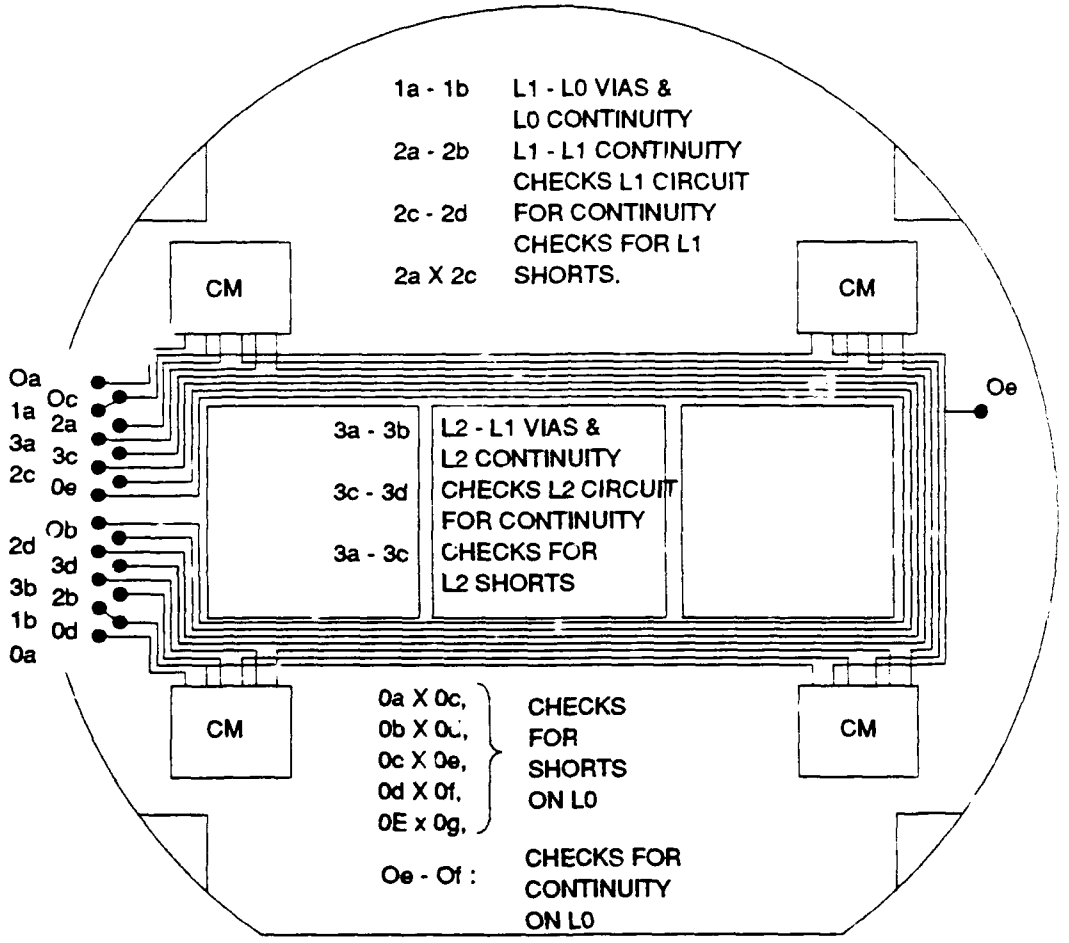
The QML procedure specifies the necessary requirements of a comprehensive quality assurance and reliability plan of which the TI-MCM foundry roadmap is directed and, more importantly, defines means of establishing the detailed database that is necessary to guarantee continuing improvements in quality as well as reduction in product cost. Some of these methods and vehicles and an outline of the QML approach to quality assurance and reliability are discussed in sections 4.7.1 and 4.7.2 of this report.

4.7.1 Process Control Monitors (PCM), Conformance Modules (CM), Test Element Group (TEG) Substrates, and Standard Evaluation Circuits (SEC)

It is envisioned that several different methods will be used to show conformance to industry, military and foundry operational standards. To meet these requirements there will be the need for various test structures to be designed, built and evaluated by the TI foundry. The following test vehicles have been identified for this purpose:

- Process Control Monitors (PCM)
- Conformance Modules (CM)
- Test Element Group (TEG) substrates
- Standard Evaluation Circuits (SEC).

The PCM is a vehicle that is designed to address both the baseline MCM process and to assist in developing advanced processes. In conjunction with these applications, it can be utilized to monitor individual processes or groups of processes, to establish process windows or tolerances for new processes, to investigate defect densities, and to setup designed experiments when process irregularities appear. Figure 4-46 illustrates a PCM scheme for in-line monitoring of the GE-HDI process.



1869-1

Figure 4-46. Process Control Monitor

4.7.1.1 PCM and CM Design. It is envisioned that a process control monitor (PCM) could be developed that will fit into the planned 8-inch wafer manufacturing process that could provide data on process repeatability, conformance to requirements and MCM design rules. A pictorial of the PCM layout is shown below.

The product characteristics that can be measured in process are:

- Intra-layer
  - Electrical
    - Continuity
    - Shorts
    - Insulation Resistance
    - Conductor Resistance
  - Visual
    - Conductor Width/Spacing
    - Conductor Height
- Inter-layer
  - Electrical
    - Continuity through Via Connections
    - Shorts
    - Insulation Resistance
    - Conductor Resistance

These response variables can be measured during the process flow by off the shelf; inexpensive automated test equipment. In fact, using existing semiconductor slice handling equipment this can be done without operator assistance. This is a simple design and can be modified to fit other substrate and module sizes. During the module design process the electrical performance variables can be modeled and necessary changes to the PCM design can be made. For example, if it is determined that the circuit length on the PCM is too short to adequately model the actual MCM design, then the PCM design can be modified to increase the circuit length.

Four Conformance Modules (CMs) can be built with each slice and integrated into the PCM Circuit. It is possible to obtain data on the robustness of the manufacturing process on an ongoing basis by evaluating the CMs. The CMs could be designed in such a way as to allow minor changes that will enable the existing MCM design rules to be stressed. For example, on a slice there could be CM's that are: 0.5X, 1X and 2X of the nominal design rules. Data could be obtained that relates process capability to design complexity and would be invaluable as an aid in working with customers to optimize design as a function of cost. The fourth CM could be used for destructive testing as part of final lot/slice acceptance.

4.7.1.2 TEG Design. Test Element Group (TEG) substrates have been developed for the GE-HDI process in order to verify baseline process flows and to demonstrate the overall yield of these sequences of operations. TEG substrates are representative not only of the total substrate fabrication process flow, but also reflect the complexity of design and the baseline design rules. These circuits, when properly designed, include active devices, and test structures for via resistance, metal continuity and bridging (on-chip, from chip-to-chip, and from chips-to-buslines), via strings, and dielectric integrity. TEG substrate designs should exist for each process flow with new TEG layouts evolving along with new and more aggressive circuit designs and advancing design rules. Figure 4-47 shows the layout of the most recent GE-HDI TEG-5 substrate.

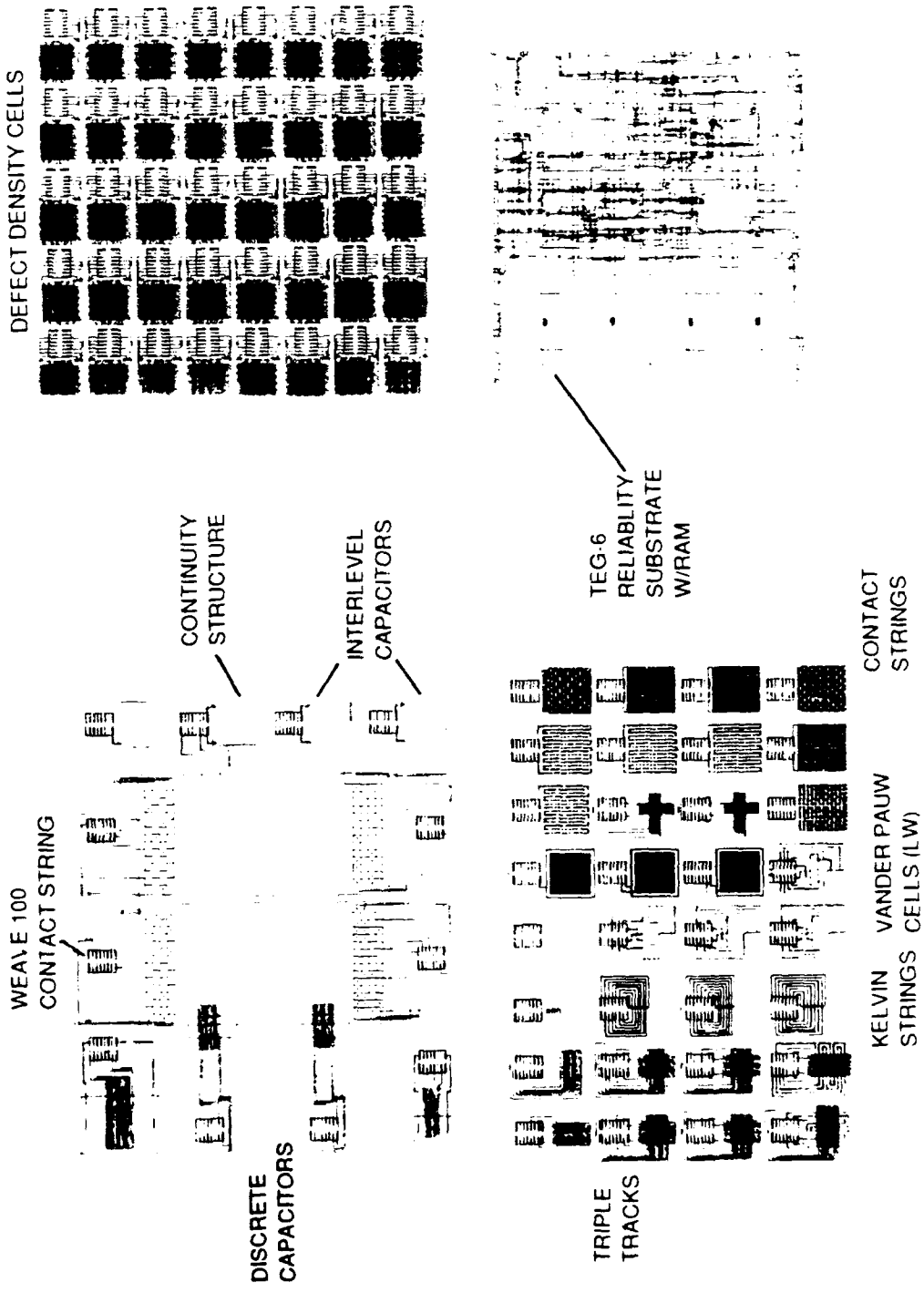


Figure 4-47. TEG-5 HDI Substrate

In comparison to the PWB quality concept, the GE-HDI test element group (TEG) substrate is a complex version of a bare printed wiring board test coupon, with the additional inherent characteristic of the GE technology of the need to bury the die under the interconnect layers.

4.7.1.3 SEC Design. The final evaluation vehicle envisioned for the TI-MCM foundry is the Standard Evaluation Circuit (SEC). The basic function of the SEC is to serve as a product conformance or qualification vehicle, hence, it must be representative of the validated methods and materials from design procedures through substrate fabrication and final assembly. The SEC may be designed solely for its role as a quality and reliability monitoring vehicle or it can be an actual product meant for design use. Any SEC, whether specifically designed or a standard product, must be designed to stress all minimum geometric and electrical design rules, it must represent the level of complexity of circuits fabricated on the QML line or the line intended for validation, it will contain fully functional circuits capable of being tested and screened in a manner similar to actual product MCMs, and it must be assembled in qualified packages with certified assembly processes. In this vein, it is likely that the previously described TEG substrates would serve as the basic ingredient of the SEC. With follow-on assembly into qualified packages, it would satisfy the requirements outlined above.

Again drawing an equivalency to the PWB world, the Standard Evaluation Circuit (SEC) for multichip modules would compare to a fully assembled printing wiring board.

4.7.2 MCM Qualification

As was discussed earlier, in order to assure a high level of quality and reliability, the TI-MCM foundry will employ a TQM philosophy. Inherent in this attitude is the need to adapt internal quality procedures that are consistent with both military and commercial facility and product requirements. To this end the qualified manufacturer approach (QML) will be pursued based on quality assurance and reliability provisions similar to those outlined in MIL-I-38535, the monolithic microcircuits general specification, and MIL-H-38534, the hybrid microcircuits general specification. Both of these military specifications would apply as guidelines for the MCM foundry, the former document addressing general quality assurance provisions as well as both integrated circuit and MCM substrate fabrication requirements, the latter specification dealing with MCM assembly and testing needs that are readily applicable to the TI-MCM foundry.

4.7.2.1 Need for Industry Wide Qualification Standards and Evaluation Vehicles. In the Printed Wiring Board (PWB), Integrated Circuits (IC) and Hybrid industries, test vehicles and standards exist that help define both military and commercial customer requirements. These include a description of an evaluation circuit that, when fabricated and tested, serves as a standard for qualification. The evolving MCM industry is in need of a similar test vehicle. This vehicle is not only for certification and qualification purposes, but also for yield enhancement and reliability modeling, including failure mode determination and reliability prediction analysis.

If, as mentioned in the overview of this section, we adopt the monolithic circuit and hybrid microcircuit fabrication and testing requirements, the elements of both a standard evaluation circuit (SEC) and the necessary reliability screening are well defined by those governing specifications. The remaining tasks for the MCM industry are to determine the specific elements that must be included in a representative circuit and then to establish the SEC as an acceptable qualification vehicle instead of having to fabricate actual product or demonstration circuits.

The MCM standard evaluation circuit must be representative of an actual product fabricated within the foundry. It can be an actual product off the line. Representative circuits must provide a means for measuring design integrity, functional performance, fabrication and assembly effectiveness including rework and repair procedures, and reliability. Product design documentation for the evaluation circuit shall include information on design methodology and the software tools in the design, the functions it is to perform, configuration, and performance simulation. It must be fabricated and assembled to the same validated procedures as for a normal product and demonstrate the capability of being tested in an identical manner to QML microcircuits. It will include test elements, or sensors, that can determine whether the assembly and packaging of the MCM elements has resulted in any damage or degradation of their function. Hence, such effects as corrosiveness, mechanical damage, electrostatic degradation, mechanical stress, bond pad damage and moisture must be able to be measured on the standard evaluation circuit.

As mentioned in paragraph 4.7.1, TEG substrates are utilized to evaluate baseline processes for the GE-HDI technology. These test vehicles already address many of the requirements of the standard evaluation circuit. For example, the illustrated TEG-5 design of Figure 4-50 was developed to address a 5-layer interconnect process. It includes parametric test elements, a defect density extraction element and active RAM devices. The parameter test elements are a group of over 50 detailed passive structures designed to allow for evaluation of the interconnect integrity. These elements are readily testable by means of a probe card that examines such key concerns as metal continuity, linewidth and resistivity, metal-to-metal and interlevel isolation, metal-to-metal contact resistance, contact string reliability, and interlevel capacitance.

The TEG-5 design also includes defect density extraction elements. In our discussion in paragraph 4.7.1, it is pointed out that these type of structures would be provided in process control monitor circuits in the TI foundry as their function is directly related to in-process monitoring rather than to evaluate the overall process capability. In any case, these cells are designed to characterize and quantify the defect density level of the TEG-5 process. Statistical data can be extracted on defects in the interconnection layers and employed to predict actual module yield loss due to random defects such as particulate.

The RAM circuit segment of the TEG-5 substrate is the active chip porion of the evaluation vehicle. In this design, four separate 64 Kbit random access memories are configured to form a 256 Kbit RAM module. Each memory die can be functionally tested with sophisticated test equipment such as a Tektronix LT1000 VLSI-VHSIC component

tester. In the specific case of the TEG-5 substrate, this active module is positioned on the substrate to allow for easy removal and packaging as a limited version of a standard evaluation vehicle that can, subsequently, be screened to customer requirements.

Modifications to the TEG-5 design and new designs will better address the total requirements of a standard evaluation circuit as these test substrates will also incorporate assembly test chip monitors. Such chips, e.g., the Sandia National Laboratory ACT series (see Figure 4-48), appear ideally suited for monitoring the assembly and packaging integrity of MCMs. These die, however, would have to be made commercially available to the MCM foundries.

In the ACT design a variety of sensors are included that can determine whether the assembly and packaging of semiconductor devices has resulted in any damage or degradation of the functionality of the devices. The Sandia ACT chips can provide immediate and quantitative monitoring of baseline assembly processes and offer the ability to gather comparative data on new packages, materials and manufacturing processes. Included in the layout of these die (as shown in Figure 4-48) are such test structures as: detectors for mobile ion contamination, moisture, electrostatic discharge, edge damage, bond pad cratering and bond pad positioning; triple-track circuits for early corrosion detection, ladder patterns of 1.25 μm lines and spaces, and separately addressable pezoresistive strain gauges.

After the addition of such an assembly test monitor chip to the TEG design, the foundry will also assure that all final assembly level considerations are made in packaging of the substrate and, of course, address optimization of the design for cost, testability, manufacturability, performance and packaging compatibility. The latter desire must address a package mounting that is compatible with standard SMT assembly techniques.

Having defined the standard evaluation circuit or qualification vehicle, the remaining elements of a comprehensive MCM quality and reliability plan center around the quality assurance and qualification testing measures that will be introduced in the TI foundry.

4.7.2.2 <u>QML Approach.</u> The path that TI/GE will follow is directed at an ultimate goal of establishing the TI foundry as not only a high volume and low cost supplier of MCMs but also a qualified manufacturer of both commercial and military MCMs. This avenue requires the implementation of and efficient and comprehensive quality assurance program that addresses the needs of the entire MCM marketplace. With a quality doctrine based on criteria established for the Malcolm Baldrige Award and a formal program in pursuit of Quality Manufactures List (QML) status, similar to that adopted by both the monolithic and hybrid world, the TI-MCM foundry organization will be in a position to meet the quality challenge.

The key concepts, designed to be quality excellence standards for the Malcolm Baldrige award, that will serve as self-assessment guidelines for the TI foundry quality program include:

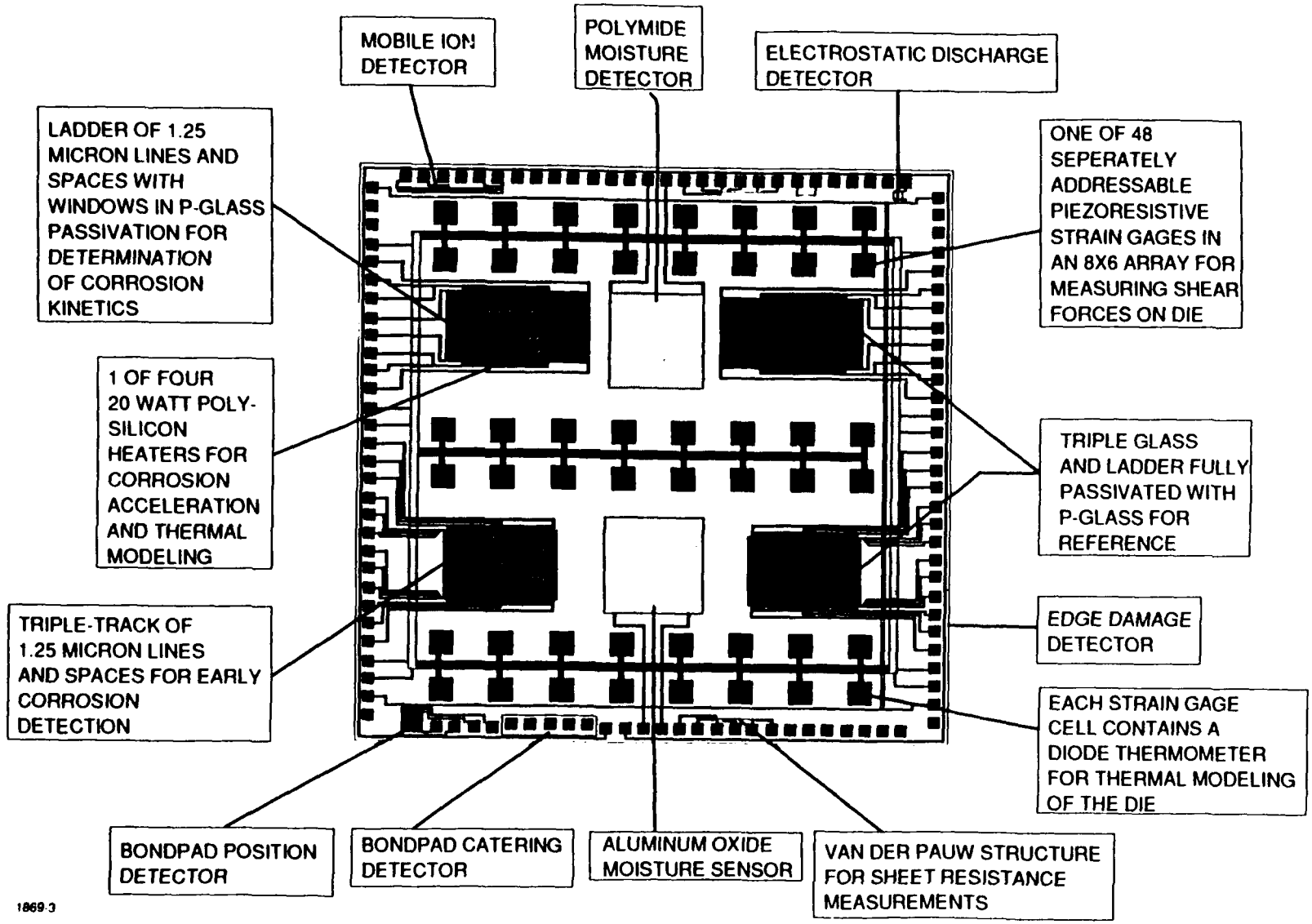


Figure 4-48. SANDIA Assembly Test Chip (ACT)

- Customer-driven quality. Quality program that addresses product and service attributes that contribute value to the customer, leads to customer satisfaction, and affects customer preference.

- Leadership. Quality values, goals and systems for achieving these are directed by the highest levels of management and involve their personal involvement.

- Continuous Improvement. A well-defined and well-executed approach to continuous improvement of all operations and of all work unit activities in order to achieve the highest levels of quality and competitiveness.

- Fast response. Rapid response to customer requirements and expectations for shorter product introduction cycles through quality systems and processes that are designed to meet both quality and response goals with response time as the major focus of quality improvement.

- Actions based on facts, data, and analysis. Actions in setting, controlling, and changing systems and processes to meet quality improvement goals are based on reliable information, data, and analysis including customer feedback, product performance, supplier evaluation and competitive benchmarking.

- Participation by all employees. A fully committed and well-trained work force that is encouraged to participate in meeting quality objectives and to support continuous improvement activities.

Highlighting general quality assurance provision the following measures will be enacted in the TI military and commercial product facility.

1. Technical Review Board (TRB) that deals with and is responsible for such issues as process change control, continued improvements in quality, reliability data and failure analysis, corrective action, product recall, and the qualification status of the MCM technology.

2. Quality management plan that is overseen by TRB that includes such items as a quality enhancement and improvement plans, programs for failure analysis and corrective action, field failure returns, SPC, a change control plan, a test vehicle (TEG and SEC) assessment plan and overall plan for certification and qualification.

3. Formal change control procedures for design, fabrication, assembly, packaging, testing and for such miscellaneous changes as key management, business plans and calibration procedures.

4. Formal status reporting describing the health of the foundry manufacturing line including critical changes in MCM quality, reliability, performance and interchangeability.

5. Periodic revalidation reviews to update the QML baseline, procedures, business plan and quality program.

The formal methodology validation and product qualification procedure that will be pursued to attain QML status, again patterned after the established monolithic (MIL-I-38535) and hybrid microcircuit (MIL-H-38534, MIL-STD-1772) standards, consists of the following elements.

A. Certification

1. Quality management program documentation including a comprehensive quality management (QM) plan (see outline), a QML certification and qualification test plan approved by the TRB that defines the testing that will be used to certify processes, the devices (TEGs, SECs) that will be tested, the accept/reject criteria, etc.

2. Quality Management (QM) Plan outline. The following provisions will be addressed in the TI-MCM quality management plan document.

   a. Index of certified baseline documents
   b. Conversion of customer requirements including device specifications, incoming inspection procedures, MCM screening and technology conformance inspection procedures, etc.
   c. Function organization chart (TRB, QA, Production, including charters)
   d. Flow charts (design through shipment)
   e. Change control program (major changes, required testing, TRB responsibility
   f. Failure analysis
   g. Self-audit program and audit results
   h. TRB reporting (to qualifying activity) procedure
   i. Yield improvement program
   j. SPC program
   k. Test method suitability including outside labs
   l. Major test methods
   m. Calibration procedures
   n. Retention of qualification
   o. Training program
   p. Cleanliness and atmospheric controls
   q. ESD program
   r. Certification and qualification test plan
   s. Third party design center procedure
   t. Supplier certification program

3. Process interface procedures that demonstrate that the interfaces between processes are under control and verification tests are performed.

4. Process capability demonstration via the design and fabrication of devices, performance of testing, running of software benchmarks to show the foundry's comprehension of the capability of the manufacturing process as related to quality, reliability and producibility. An ongoing test schedule showing 100% and sample testing will be set up that demonstrates the foundry capability to continue to build high quality, reliable and producible MCM product to design rules.

   The environmental and mechanical testing to be performed will resemble that of Table 4-6 which specifies the major tests for evaluation of both plastic and hermetic encapsulation. Actual test requirements may vary depending on customer specification, e.g., Class-S military requirements would demand hermetic level screening. Furthermore, evolving MCM technologies in all likelihood will require that new test procedures be developed to address different failure modes. It is anticipated that during the QML procedure for the TI foundry, the documented qualification test plan will establish the minimum level of testing to be performed for product qualification.

5. Management and technology validation including an on-site audit by the qualifying activity of, at a minimum, the foundry quality assurance system and the provisions implemented to control designs, fabrication, assembly and packaging, and electrical testing.

6. Letter of certification issued by the qualifying activity after technology validation with qualification signaled to begin within six months.

B. Qualification

1. A one time generic, product qualification procedure will be initiated no later than six months after foundry certification. The qualification test plan prepared during the certification of the foundry must be implemented for two demonstration vehicles, or for our high volume MCM foundry, standard evaluation circuits (SEC). As previously discussed in paragraphs 4.7.1 and 4.7.2.1 the SEC accurately represents an actual product in its complexity of design, fabricated to certified processes, assembly, packaging and screening provisions. The test plan details the test flow, limits and data to be measured, recorded and analyzed, test sampling techniques, and traceability records. The testing sequence requires comprehensive screening to MIL-STD-883C including Group A electrical tests, Group B, Group C life tests, Group D and also Group E (RHA) testing, where applicable. It will also specify materials, manufacturing construction techniques (including design tools) and test and reporting methods. It must accurately describe the standard evaluation circuits that will be qualified.

2. Upon completion of the qualification testing the Technical Review Board (TRB) shall present a comprehensive qualification test report to the qualifying activity

TABLE 4-6. TYPICAL MCM ASSEMBLY TESTS

Test	MIL-STD-883 Test Method or Alternative Test
Temperature Cycling or Thermal Shock	1010, Condition C 100 Cycles, -65 to 150°C 1011, Condition C 15 Cycles, -65 to 150°C
Stabilization Bake	1008, Condition C 48 Hours @ 150°C
Wirebond Strength	2011, Condition D
Constant Acceleration or Mechanical Shock	2001, Condition A, Y1 Direction Only 2002, Condition B, Y1 Direction Only
Pressure Chamber (non-hermetic only) or THB 85/85 (non-hermetic only)	JEDEC 22-B, TMA 102A 168 Hours, 121°C, 2 atm JEDEC 22-B, TMA 101 1000 Hours, 85°C, 85% rh
Internal Wafer Vapor (hermetic only)	1018, 1000 ppm max @ 100°C
Variable Vibration Frequency	2007, Condition A
Fine and Gross Leak (hermetic only)	1014, Condition A, Fine Leak Condition C, Gross Leak
PIND Test (Class-S hermetic only)	2020, Condition A or B
Flammability	UL94-V-0, ASTM 2863-77
Fungus Resistance	MIL-F-13927
Salt Atmosphere	1009
Vapor Phase Cracking Susceptibility	Drybake and Leave for 72 Hours and Then Solder

that presents an analysis of the qualification data and demonstrates that all processes are under control and repeatable.

3. QML listing upon successful completion of all qualification tests on two demonstration vehicles, or standard evaluation circuits, and the acceptance of the qualification documentation by the qualifying activity.

4. Maintenance and retention of QML by periodic fabrication and testing of selected SEC designs as defined by quality management program documentation.

The QML philosophy, predicated on the total quality management principals of the Malcolm Baldrige National Quality Award and documented military standards will significantly enhance the capability of the TI-foundry to meet the DARPA goals of high volume and low cost manufacturing of both commercial and military multichip modules.

4.7.3 Quality Function Deployment

Concurrent with the development of the Military/Industry specifications, actual engagements with potential customers needs to begin. Quality Function Deployment (QFD) will be the method used to capture the customer requirements and communicate the relation between these requirements and factory operations.

QFD is an iterative process and is most efficient when there is active customer involvement. The QFD process involves the development of four "houses of quality" that span the product inception to production operations. The descriptions of the four houses are:

House 1 - "House of Quality" - The customer careabouts are defined through interaction with the customer. These "whats" are then related to engineering characteristics, the "hows". This then leads into house 2:

House 2 - "Parts Deployment" - The "hows" from the first house becomes the "whats" for the second house. The product characteristics "hows" are then defined that relate to the engineering characteristics.

House 3 - "Process Planning" - These product characteristics are then related to the key process operations that are required to build the product.

House 4 - "Production Planning" - The key process operations are then related to the production requirements for producing the product.

The QFD process ties the customer requirements all the way down to the production requirements and leaves a trail as to how it was developed. This is an excellent method to use both in showing the customer how it plans to support their requirements, but also as a means of communication to the foundry personnel of how their job functions tie to the customer requirements.

Existing processes have been developed and for the most part been run by highly trained personnel in a prototype environment. For a High Volume facility to operate cost effectively the processes are going to have to be made more robust at the same time made less expensive (labor, materials, capital). This is optimized best with the use of Experimental Design Techniques in the process/equipment definition phase.

4.7.4 Design of Experiments

A critical requirement for the MCM foundry (or any other manufacturing process) is the need for process understanding followed by tight process control. Process understanding can be either learned from experience (usually at great expense in time and money) or by experimental designs. The TI plan for how experimental designs will be used will be based on data from GE relating to their existing defect pareto and on inputs from TI/GE engineers related to the proposed enhancements to the existing GE manufacturing flow.

The inputs required for experimental designs are process variables and response or quality variables. These response variables can be parametric or qualitative (pass/fail) in nature, but a greater understanding of the process/ product can be obtained with parametric response data. It is envisioned that industry, academia, national lab and customer inputs will be used in addition to GE/TI experience in identifying the response variables. TI and GE engineers will then define the process variables that are believed to effect each response variable, their relationship to each other and the relative importance of each variable.

Once the variables have been identified for each process; the actual design of the experiment will occur. The process variable settings are defined in such a way as to insure that "failures" are evident in the response variables, but not such that the settings cause a test to become invalid. TIs experience with this has shown that this is an iterative process especially for complex processes with many process variables. In these situations, it is normally best to divide the test into several sub-tests and identify the key variables within each sub-test. A final test is designed using the key variables from the sub-tests, then the final definition of the key process variables is obtained along with information relating to the process parameter setpoints. If required, further tests can be run to further refine the process setpoints.

4.7.5 SPC Methods

After key process variable and parameter setpoint definition has been completed, the implementation of Statistical Process Control (SPC) methodology can be completed. The most important concern in controlling a process with SPC is the belief of the line operator that SPC is really helping, not just a make work effort for the operator. SPC training will be required for MCM foundry personnel so that everyone speaks the same SPC "language". This training is for everyone (line operator, engineer, management) prior to the startup of the experimental design effort. SPC techniques can be used in the experimental designs and a "buy in" of all involved can occur.

SPC must be recognized as a way of life and not just a means to an end. Everyone must believe that it is the right way to operate a manufacturing business. Training will become an ongoing activity, not just something that happens at the beginning and is cast aside.

4.7.6 Process Monitoring Procedures

The data collection method will be an evolving one. At the beginning, manual (paper) control charts will be developed and maintained. As process methodology is refined, computer monitoring systems will be installed/developed to collect and present the data to the manufacturing operator. Finally this data will be processed by a control system that assists the manufacturing operator in understanding that a change has occurred in the process and aid in bringing the process back into control.

The need to control the critical process parameters is clear from the SPC methodology perspective. The entire goal of SPC is to reduce the variability of the product that is being manufactured. Control of the manufacturing process variables is one of the methods used to reduce this product variability.

4.7.7 Supplier Control

Another key method in reducing the final product variability is to reduce the variation of the purchased products (dielectric materials, chemicals, substrates, etc.) that are required to build the final MCM. This will require close coordination and team work between the MCM foundry organization and its suppliers. For this reason the suppliers will also be required to develop their own plans for implementing their own TQM systems that encompasses the designed experiments as well as SPC and critical process control philosophies. It is envisioned that the MCM foundry organization will take the lead in working with these suppliers to help them develop their own TQM plans and procedures.

For example, a design requirement for a product might be that for current carrying reasons the conductors must be 12 microns thick and have a conductor width of 50 microns. The 50 micron conductor width requirement falls within the existing design rules, but the 12 micron thick conductor is 3X the present design rules. An experimental design effort would be undertaken to determine impact of this on product manufacture and to allow definition of the key process variables and parameter setpoints. This requirement indicates potential concerns in the following process areas:

- Conductor Image and Etch Resolution
  - Due to increased amount of conductor metal to be etched
- Conductor Metal Plating Capability
  - Intrasubstrate Metal Thickness Uniformity

- Next Layer Dielectric Spacing
  - Additional Metal Thickness Impact on Dielectric Uniformity/Adhesion.

The first step in the experimental design would be to identify the response variables:

- Conductor Thickness --> relation to circuit resistance
- Conductor Width ------>
- Dielectric Thickness
- Presence of Laminate Voids
- Capacitance
- S/W
- Speed.

Process variable definition would then occur such that variables are defined that would have an impact on the response variables. Some of the variables might be:

- Resist Thickness
- Etchant Chemistry --> etch rate
- Etchant Temperature -/
- Artwork Etch Factor
- Plating Current Density
- Plating Chemistry
- Adhesive/Dielectric Rheology
- Adhesive/Dielectric Coating Rate.

The process variables would then be reviewed for possible interactions with each other from the standpoint of impact on the response variables. Once this is determined the actual definition of the test matrix can begin. This can be accomplished manually or by using purchased software. Both methods have been used by TI. The levels for each variable (test conditions) will then be set and the testing initiated. Once the testing is completed the response variables will be analyzed and the impact of the process variables ranked to determine impact on the response variables. Testing error can also be defined and a determination of whether additional testing is required can be made. The optimum process variable set points can be determined with additional analysis and testing.

In this hypothetical case, assume that etchant temperature and adhesive/dielectric rheology are the most critical process variables affecting circuit geometry and dielectric thickness, the key response variables. An SPC control plan would be put together to monitor these process variables based on the optimum, upper and lower specifications defined in the designed experiment. As data is collected on the variables a new set of limits; process control limits; will be established based on the data. These control limits and not the specification limits would be the method for determining if the process was operating properly or not. Again, as mentioned earlier the goal will be to reduce the variability of the process variables (and therefore the spread between the upper and lower control limits) and thereby reduce the variability of the product.

For the etchant temperature, an electronic controller can be installed on the process that will maintain the temperature to the desired settings as well as provide digital data to a factory data collection and management system for continuous monitoring. This will provide a method for process review and analysis on an ongoing basis that will provide further insight into the effect of process variables on product response variables.

The adhesive/dielectric rheology possess a more complex control system. Not only are controls installed within the manufacturing process to monitor the product, but the need to go back to the material supplier to work the issues related to reduced variation at the supplier level. A sample inspection plan would be implemented in the beginning, but the eventual goal would be to have confidence in the supplier to provide the product that meets the needs of the manufacturing process and only monitor the suppliers own internal process variable data. In order to do this it will be important to bring the supplier on board early in the experimental design process so that his understanding of what is important to the final product is understood.

This methodology will allow the MCM foundry to operate at the optimum process setpoints using optimized materials purchased from suppliers that understand the product requirements. The supplier will benefit from having a satisfied customer and would therefore have a head start on any further development activity and the resulting sales that it would generate. The MCM factory would benefit from reduced manufacturing costs (yield, inspection, process adjustments, etc.) due to process controls within his factory as well as his suppliers, a win-win situation for both.

4.8 TECHNOLOGY EXTENSIONS

A critical requirement of this study is to address how the GE-HDI MCM technology is extendable into non-digital electronics. The GE-HDI technology is uniquely positioned to support a wide array of non-digital electronics including analog, power, microwave and opto-electronic. This section will identify how the GE-HDI technology can be extended into these and other areas and what developments are needed and/or are already underway.

4.8.1 3-D Memory Cubes

Under DARPA funding, TI has developed a 3-D memory cube technology that stacks eight or more TAB interconnected static RAM chips to a 3-dimensional cube (see Figure 4-49). In its baseline form the TI cube is solder attached to the top of a SOS multichip substrate. DARPA has initiated a program to integrate the TI memory cube into the GE-HDI process. For high memory content modules, the incorporation of the TI memory cubes into the GE-HDI modules can provide the highest volumetric yet proposed. This extension will also improve the reliability of the cube interconnect to the MCM interconnect structure and offer the ability of using the adaptive laser to add redundancy capability to the memory cube.

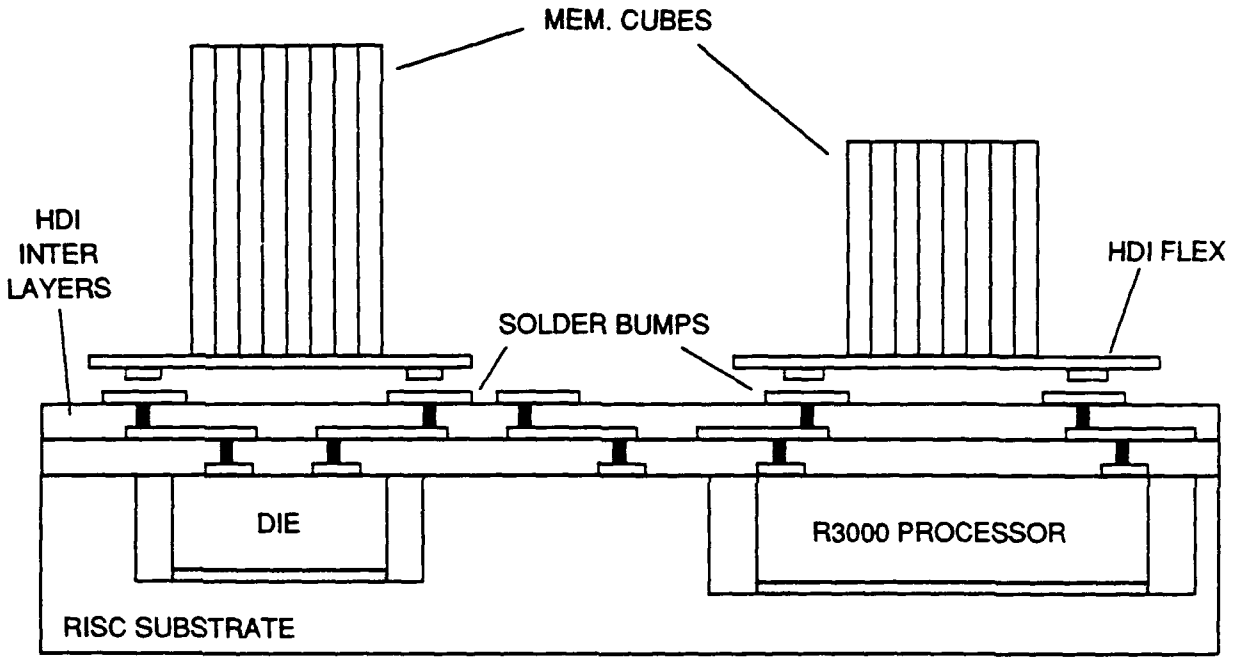


Figure 4-49. RISC Module with Memory Cubes on Top

4.8.2 Stacked HDI

Another enhancement of the GE-HDI process is the stacking of multiple MCM substrates into a 3-D structure. GE is developing a stacked HDI capability under AFPL funding for high density space application. The nearly planar surface of a completed GE-HDI module permits the direct mounting of one MCM substrate onto another forming a 3-D stack of HDI modules. The "chips last" MCM approaches all have their chips mounted on top of the MCM substrate, precluding the option of direct stacking. The interconnect between HDI planes can be with area contacts, flexible cables or with an application of the basic GE-HDI interconnect process to the edges of the HDI stack. With a GE-HDI stack of four substrates, a silicon density of more than 300% is achievable. Figure 4-50 shows a 3-D HDI stack that has layer to layer interconnections made with the GE-HDI technology.

4.8.3 Analog HDI

Although the GE-HDI process was developed to support the packaging and interconnection of high speed digital ICs, active and passive testing has indicated that the GE-HDI process is directly extended to most analog domains. The front ends of most military electronics systems is analog rather than digital. The analog comes from sensors such as radar, radio waves, sonar, remote sensors, and the like. These signals can either be processed as analog signals or they must be converted to digital for digital signal processing. The GE-HDI technology has shown good performance up to 26 GHz analog, to 2 GHz and to high power densities. A development program has been initiated to put in place a CAD capability, design rules, improved performance materials and test methodology for analog and

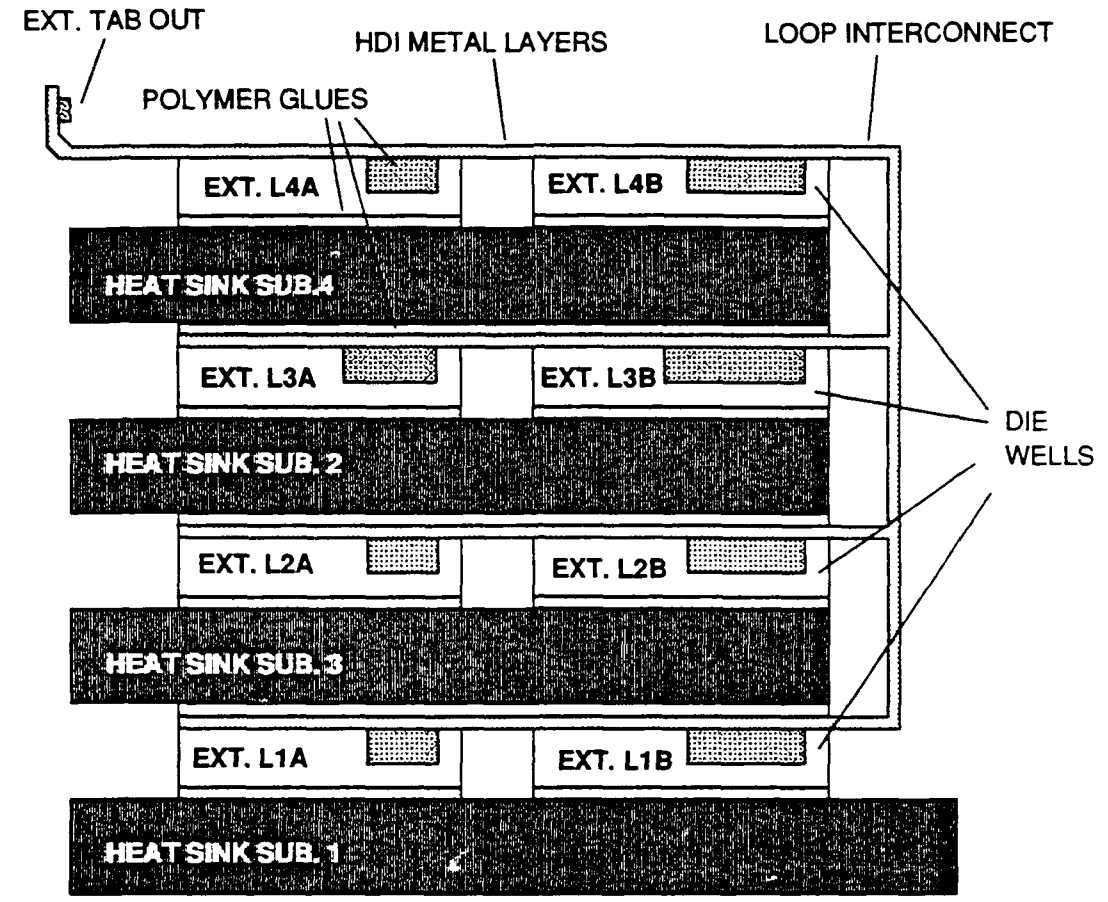


Figure 4-50. AFWL Extended Stack Concept View

mixed analog/digital HDI modules. Initial designs will feature 12-bit A/D and signal processing chips on a common HDI module. These developments include lower dielectric constant material, gold metal processes and imbedded thin film resistors.

4.8.4 Flexible HDI

The polyimide film that is used to form the first layer interconnect, can provide a flexible interconnect between chips and between GE-HDI modules. Multiple substrates are fabricated in the GE-HDI process with one common overlay film. By selectively applying the overlay adhesive that bonds the film to the substrates, multiple HDI structures can be connected together via the polyimide film. This flexible film can contain multilayer metallizations that could form a second level interconnect structure that connects together two or more MCMs (see Figure 4-51). Like most flexible tape interconnect, these structures can be folded into a stack or formed to a non-planar surface.

4.8.5 Optical Interconnect HDI

Opto-electrical implementation of HDI is a clear area of research. The HDI laser can ablate polymers forming micro-tunnels which may be made to totally internally reflect, to produce a light pipe that is integral to the HDI technology. Additionally, the extended HDI concepts allow the module to module interconnect by optical means (see Figure 4-52).

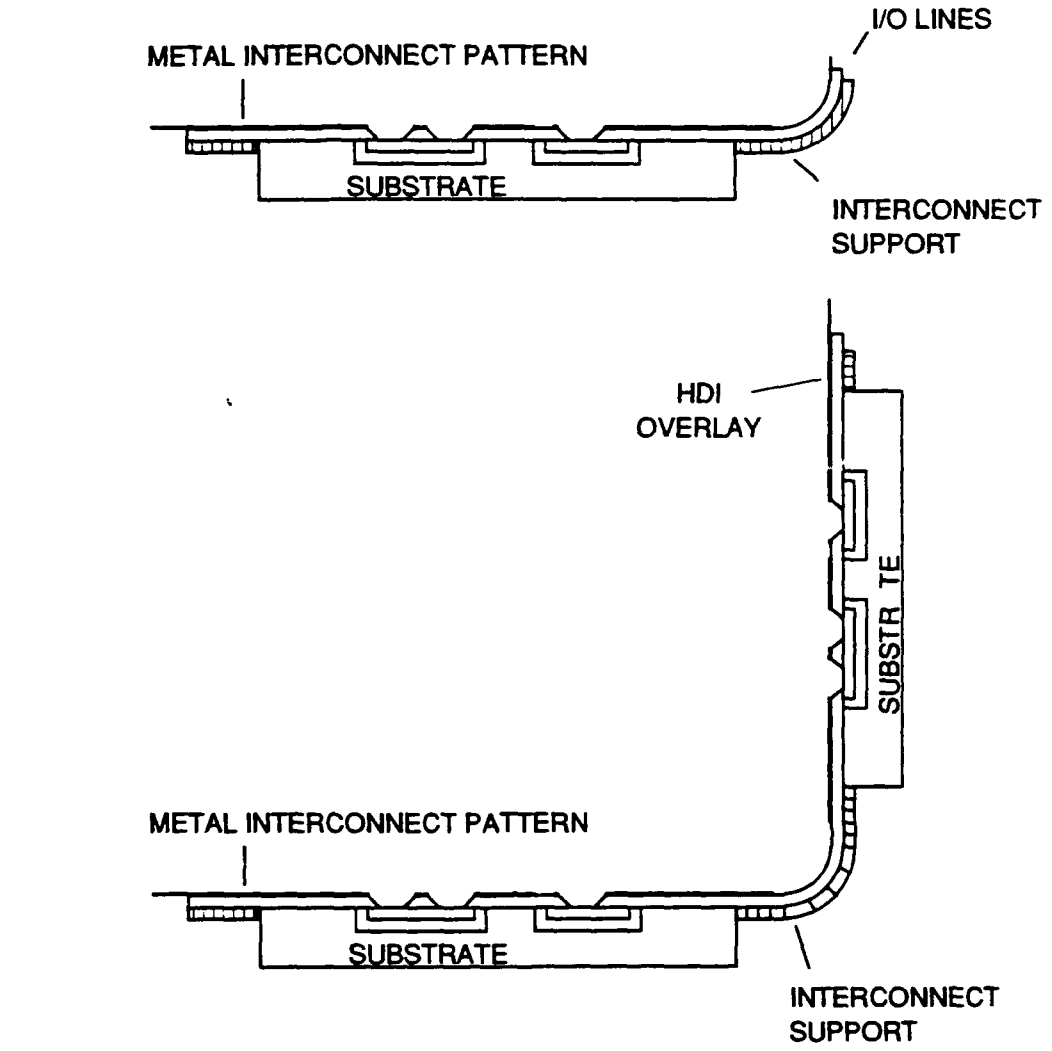


Figure 4-51. Flexible Interconnect Process

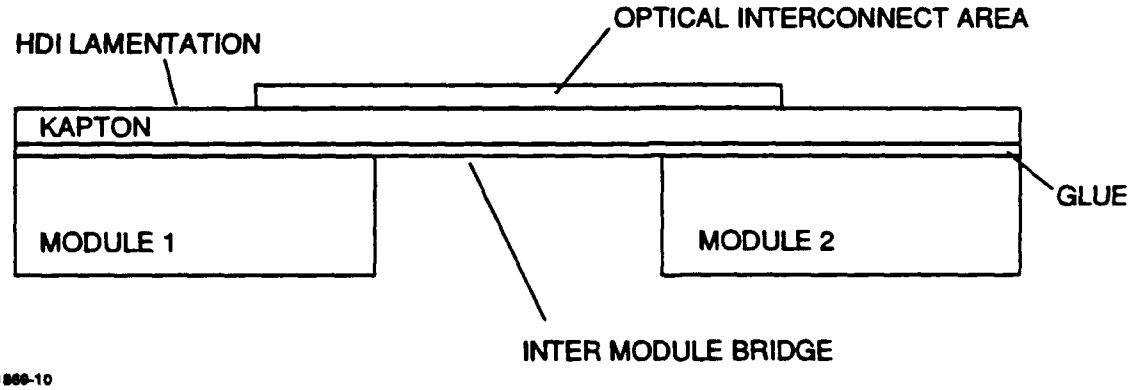


Figure 4-52. Inter Module Bridge for Optics

The opto HDI concepts have been under review within the General Electric Co. for some time. The unique ability for HDI, to laser adaptively expose and adapt polymers that are optical in characteristics, to interconnect optical die, is believed to be a novel idea. The HDI lasers using optical polymeric materials can hook up laser diodes etc., to the design rules of HDI in principle. It is believed that the short length of the adapted polymeric materials, from the die to die or die to fiber, will allow the interconnection to take place with minimum losses. This extension will enable the HDI basic ideas to be used in a much broader scope. The adaptive capability of the laser patterning can be used to minimize mechanical alignment of a fiber to a device or HDI light channel. Indeed, lenses can be created by software control of laser ablation.

4.8.6 Power HDI

As technologies like the GE-HDI process increase, the packaging density and electrical performance of electronic hardware and power density will increase dramatically. A 10:1 silicon density increase with a 2:1 power savings will still require a 5:1 increase in power delivery density. Increase current distribution by a 5:1 factor would increase supply losses and noise to an unacceptable level. A better solution is to have power distributed at a higher voltage level, 25 or 50 volts rather than 5 volts, with a corresponding 5:1 to 10:1 reduction in current and if power losses. Distributed power conversion modules would covert locally to the 5 or 3 volts needed for circuit operation. A GE-funded development program is underway to combine high efficiency power conversion components with high density interconnection. The program will take advantage of HDI's high thermal performance, high electrical performance and robustness.

4.8.7 High Frequency Digital

Under DARPA funding, GE has designed passive and active interconnection test coupons to evaluate the electrical performance and characteristics of 200 MHz and 5 GHz digital multichip modules. The baseline process shows promise up to 300 MHz or higher with development identified to optimize the GE-HDI process for digital MCM assemblies up to 5 GHz. These extensions include lower dielectric constant polymers, replacement of the HDI Ti barrier metallization, development of thin film resistor elements and test and CAD capability.

5.0 SUMMARY AND CONCLUSIONS

5.1 IMPORTANCE OF MCM TECHNOLOGY DEPLOYMENT

MCM technology is crucial to maintaining the competitive position of the U.S. electronics industry. Government users of this technology will be in the performance driven product areas of data and signal processing, space applications, and missiles and smart munitions. Commercial users of this technology will also be performance driven, primarily in the areas of supercomputers, workstations, and some personal computers.

This study confirms that the MCM market need is developing, and that the market gap will be between late 1992 and 1994. It is during this period that entry products will be defined, configured, and deployed. The driving force will initially be performance; as volume increases and manufacturing cost decreases, other market segments will be penetrated. The initial volume manufacturing demand for MCM technology will be the commercial market segments. Performance requirements will drive users to off shore suppliers if cost effective domestic capability is not in place to meet approaching needs. The resultant high domestic manufacturing cost, if initial volume requirements are allowed to migrate off shore, will limit any penetration of domestic production into both the commercial and military applications. The government cost benefit from domestic MCM production capability will not be significant if this happens.

This effect will be even more profound in the commercial segments, where the quickly decreasing cost/performance relationship will elude the foundry if the initial market gap is not intercepted and applied manufacturing developments are not executed concurrently. While technical capability will be in place for government applications, the higher cost will limit insertions to very few applications where the performance over cost relationship is dominant. This will, to a large extent, prevent the government from reaping the significant advantages of MCMs on a broad scale. In the long term, overseas component, subsystem, and systems supplies will migrate from the commercial market place with its volume driven low costs into the military market place, putting the U.S. based military electronics industry at risk.

5.2 MARKET

5.2.1 Market Overview

The market study leads to the conclusion that MCM packaging technology has broad acceptance within the industry as the next generation system level packaging solution. The increasing challenge of system performance in the areas of speed, size, weight, and thermal management is driving both the military and consumer market segments into MCM technology. The demand of the industry for this packaging technology will be either filled by the domestic industry, which at present is not well positioned for the high volume manufacturing challenge between 1992 and 1994, or by offshore suppliers. The opportunity still exists for the domestic industry to become well positioned to serve significant domestic market share. However, given the rapid growth in volume forecasts, and given the very near term timing and magnitude of the predicted domestic market growth, the domestic industry

will be challenged to develop the internal capability and target the key strategic external industry infrastructure issues quickly enough to remain competitive in a high volume manufacturing scenario. It is only through domestic competence in high volume MCM market segments that the DoD can expect to gain a price advantage from domestic suppliers.

Critical to maintaining domestic leadership in this industry will be rapid development of industry infrastructure and supporting tools to "enable" both the merchant foundries and the MCM users. Sponsorship of such industry infrastructure efforts and applied manufacturing development programs will be instrumental to the military MCM user programs to ensure both programmatic technical success and lower cost in production.

5.2.2 Market Segments

A broad range of market segments were addressed in the market survey of section 3.0. These segments included military, automotive, commercial, telecommunication, and consumer. All of these segments have different performance versus cost curves, and the rate at which the MCM foundry can meet or intercept this performance/cost relationship for a given segment will determine the rate at which the foundry market base will increase. The MCM foundry will initially serve performance driven market segments in military applications, super-computers, mainframes, and high-end workstations. Other applications the commercial market are rapidly approaching system level performance needs that will require MCM packaging to maintain competitive market positions. As volume drives cost downward, and as other market segments are driven to higher performance, additional segments will be penetrated by the foundry on a merchant basis. The key market window for initial market penetration is between late 1992 and early 1994.

5.3 TECHNOLOGY

5.3.1 Present HDI Technology Status

The GE-HDI MCM interconnect technology was developed in 1985 with combined DARPA, Air Force, and GE funding totalling more than $25 M. It is a proven technology, with over 40 designs completed and over 390 modules produced to date for 9 different customers. Applications to date have been both military and commercial. The GE-HDI technology, in its current state of development, offers the lowest non-recurring cost of any available MCM interconnect technology due to the elimination of the cost and cycle time associated with TAB and photomask procurement.

Rapid prototyping capability is a natural extension of the baseline GE-HDI MCM technology. Design and manufacturing are integrated by nature of a common database. This inherent direct "art" to "part" flow within the foundry is the key element to achieving reduced cycle times and the ability for quick turn prototyping and rapid execution of engineering design changes. Elimination of the additional processing and procedural steps required for mask processing is a major cost and cycle time benefit in a small part run, rapid prototyping, iterative design scenario.

The baseline GE-HDI technology is currently ideal for low volume manufacturing. It is expected that the initial foundry will be required to serve a market with a high part number mix and manufacturing requirements of less than 100 units per part number. There is a clear match between the baseline GE-HDI capability and the anticipated market requirements in the initial stages of the foundry startup. The technology has enormous potential for extension to the high volume, low cost requirements anticipated after 1994 with the market driven, time phased, applied manufacturing development program proposed in section 4.

5.3.2 High Performance Capability

The GE-HDI technology offers unique advantages in MCM packaging performance. These advantages are packaging density, electrical performance, robustness, reliability, and thermal performance. The baseline HDI configuration offers the highest 2-D silicon packaging density available. Mechanical integrity and high reliability performance have been demonstrated under Mil-Std-883 test methods 2001, 2002, and 2007 with Air Force funding. Electrical performance has been demonstrated, with test coupons, to the multi GHz range. The inherent characteristics of shorter interconnect lengths, controlled line width and spacing, and controlled dielectrics enhance this technology's electrical performance over that of standard technologies. Mechanical performance is enhanced by an extremely robust structure due to the overlay process. This leads to high performance in severe shock and vibration environments as well as significant high density packaging integration leverage.

5.3.3 GE HDI Technology Flexibility

The GE HDI technology is extended beyond digital performance limits into analog, power, electro-optical, and microwave domains. GE has active IR&D projects underway to develop analog CAD capability, design rules, enhanced materials, and test methods. IR&D funding has been used to develop a microwave HDI capability that encompasses CAD, process development, design, fabrication and testing C-band and Ku-band modules. IR&D funding is also being applied to high frequency, high efficiency power conversion efforts. A DARPA contract is being executed to develop new interconnect structures to extend the digital capability into the multiple GHz range.

The basic technology lends itself to multiple packaging formats. This allows a multitude of unique MCM module form factors to be considered at the point of design. For instance, the GE 2-D overlay process has potential to be integrated with the TI 3-D memory stacking technology; DARPA funding is in place to demonstrate this integration in 1991. Additional work is being funded by the Air Force to develop and demonstrate 3-D stacking of HDI MCM substrates. The HDI MCM can itself become the package in commercial applications; this has been implemented on a functional SPARC workstation module and offers tremendous cost savings in high volume production. This "substrate as the package" approach is unique to the HDI technology and not available in "chip last" approaches due to the geometry of the structure.

Finally, the HDI overlay process requires no special IC processing beyond normal wafer fabrication flow. Multiple IC technologies, such as Silicon and gallium arsenide based

chips, can be implemented easily into the same MCM interconnect with no extra or special processing.

5.4 TI/GE TEAM

5.4.1 Capability

TI and GE have formed a strategic business alliance that will result in an MCM foundry owned by TI using the GE HDI technology as the cornerstone packaging approach. TI and GE are uniquely positioned within the domestic industry for the challenge of inserting viable MCM packaging technology. The team brings complementary expertise to the challenge of advanced packaging, specifically to the challenge of insertion of a viable MCM foundry. GE brings significant strength in pure research for both materials and processes; expertise in software development; and a demonstrated ability to develop baseline processes, proven designs, prototype manufacturing, and test capability. TI brings significant strength in applications engineering for system level technology trades and definition of product specific designs, as well as manufacturing expertise to support the market driven transition to high volume, low cost production.

The value of this complementary TI and GE skillset has already been recognized by DARPA with the award of the MCM Merchant Foundry program to this team. The HDI overlay technology will be transferred from GE's prototype facility to a low volume manufacturing facility at TI as a result of this program. This low volume facility will form the cornerstone for the high volume, low cost factory extensions addressed by the SWAP effort.

TI's Custom Manufacturing Service (CMS) Division has a worldwide corporate infrastructure in place to support MCM foundry customer interfacing needs. CMS provides SMT and throughole customs manufacturing and assembly services to a balanced portfolio of customers servicing a variety of commercial markets worldwide. The CMS capability will be expanded to support the MCM foundry with customer support, technical briefings, training, and customer feedback. Commercialization of MCM assembly services will be a natural product extension of TI's custom manufacturing business.

5.4.2 Resources Available

Both TI and GE are stable companies with the commitment and the resources to support establishment of a domestic, dual use MCM foundry. Supporting corporate infrastructure is in place at both companies for customer support, marketing, design tool development, processing and materials research, manufacturing production systems and capability, and component and assembly test. When combined, resources of TI and GE result in a high degree of vertical integration. All areas of the global MCM foundry development challenge identified in this study are supported with excellent starting point positions. It is a primary component of the proposed plan to use both TI and GE existing capability in a complementary fashion to establish production MCM foundry capability and to invent only

when absolutely necessary. The necessary systems and expertise to successfully achieve this objective exist within TI and GE in the military and commercial business sectors.

5.4.3 Industry Team Members

TI and GE have recognized the value of strategic teaming with members of academia, industry suppliers, potential industry customers, and national laboratories where complimentary technology development programs and skillsets exist. Strategic teaming offers an excellent method of using mature starting points to avoid duplication of development work. Properly executed teaming will result in accelerated implementation of the internal foundry infrastructure, and will aid in the development of external MCM technology infrastructure, while reducing the risk to all. The following paragraphs outline some strategic areas where teaming on a follow on program will be instrumental.

5.4.3.1 Universities. Ongoing research activities in the university environment offer an extremely powerful resource and should be encouraged in a follow on program by the foundry. The University of Arizona has had an active program in development of electrical design and analysis tools since 1984. A program with the University of Arizona as a component of a SWAP follow on effort has been proposed to compliment and further develop the existing HYPACK design tools.

TI is a member of the University of Maryland's Computer Aided Life Cycle Engineering Center (CALCE). This effort sponsors the development of Reliability and Maintainability (R&M) tools. These tools have been integrated into an internal workstation toolset at TI, named Computer Aided Reliability and Maintainability Applications (CARMA). The MCM Foundry team plans to leverage from systems and activity in place and enhance this system support for MCM product applications.

Inputs from the Illinois Institute of Technology Research Institute (IITRI) Reliability Analysis Center (RAC) were of substantial merit in formulating the QML plan presented in section 4.7. IITRIs experience and existing relationship with Rome Air Development Center (RADC) is expected to be a key part of the MCM Foundry and product qualification plan.

5.4.3.2 National Laboratories. Sandia National Laboratories has several ongoing activities that complement needs the foundry will have during the startup phase. Service has developed test chips for stress, environmental, and temperature monitoring. Work on testability methods for both IC test and module test will supplement foundry needs. Finally, work dealing with mechanical interface to bare ICs will be used to accelerate development of solutions to this mechanical fixturing challenge in the foundry test strategy.

5.4.3.3 Systems Manufacturers. Several relationships have developed during the course of the SWAP effort. Both TI Defense Systems and Electronics Group (DSEG) and GE Aerospace have active programs either using prototype MCM products or inserting MCM products into existing programs. Relationships have been established with Boeing, Martin-Marietta, Alliant Techsystems, and SUN Microsystem. Alliant TechSystems (formerly Honeywell) has offered inputs based on a need for advanced packaging leverage in a Planned

Product Improvement update phase of their SADARM program. This program offers, for a military product, the challenge of both high volume and low cost requirements to the foundry in the 1994 and later time frame. Sun Microsystems has indicated strong interest in MCM packaging technology for multiple uses within their product line with high volume needs in the 1993 and later time frame.

5.4.3.4 Suppliers. Several strategic relationships have been established with suppliers during the study phase of the SWAP program that will be further developed in a follow on effort. These relationships are in basic areas of materials and support systems.

In the area of materials, WR Grace/Coors have provided inputs for low cost, integrated packages and low cost, high performance HDI substrates. Ceramic Process Systems has provided inputs for net shape, pre-molded substrates in six and eight-inch wafer slice formats to use in high volume, low cost applications. Dow Corning has proposed follow on effort to their development in ceramic based environmental coatings; materials which show promise in increasing MCM reliability in low cost, pseudo hermetic approaches.

Task Technologies, Mentor Graphics, and Digital Equipment have all provided inputs or valuable critique on design systems or manufacturing system architecture.

5.5 BARRIERS TO MCM TECHNOLOGY INSERTION

5.5.1 Current R&D Focus

The current focus of MCM technology efforts at both TI and GE, and in the industry in general, is on developing a technical solution at the component level. This is illustrated by the development of 3-D memory packaging by TI and the GE HDI overlay by GE; both offer tremendous advantage to a particular part of the packaging design problem. What is needed next is a thrust to develop system level packaging solutions and a systematic program to enhance and mature the manufacturing processes for MCMs before the need for high volume manufacturing arrives.

5.5.2 Near Term Barriers

Barriers to the successful introduction of domestic Merchant MCM capability are:

- The market is still developing, immature, and largely captive
- Much of the market is sensitive to current MCM prices and will elect other packaging alternatives until true low cost MCM manufacturing is available
- Required facility and capital investment is high regardless of the MCM interconnect technical approach
- The industry supporting infrastructure is not in place:
  - Bare chip procurement and specification
  - Test at IC and MCM
  - Design tools for MCM simulation

- Reliability guidelines and standards
- Package and socket standards

- The market window of opportunity is near term, rapidly approaching, with little reaction time available
- Significant CIM system and applied manufacturing capability development is needed.

5.5.3 Path to Success

There are several key elements the Merchant foundry must include for success in developing MCM products as a viable business. These are:

- Baseline technology which serves the broadest application spectrum while offering significant potential for low cost manufacturing
- Applied manufacturing development program to mature the processes and materials in a production environment, to further develop the design and analysis tools, and to develop the foundry internal infrastructure
- Strategic teaming with complementary members of Industry (both suppliers and customers), Universities, and National Laboratories
- Active participation in industry infrastructure development.

The execution of these elements in the development phase of production capability within the foundry offers the opportunity to reduce the risk during the startup phase for all involved: the TI/GE foundry team, DARPA, the foundry customers, and the suppliers. Successful execution of the MCM manufacturing insertion program within the MCM Merchant Foundry effort and the applied manufacturing development phases of section 4 will result in technical capability that can readily be translated into product applications meeting customer needs.

5.6 TECHNOLOGY DEVELOPMENT AND ENHANCEMENTS

5.6.1 Automation

It is envisioned that the foundry will support the total MCM design and manufacturing process, allowing customer interfaces as early as the initial design concept, or as late as interconnect fabrication. A Computer Integrated Manufacturing System (CIM) is required to manage the data, design, manufacturing, test, and assembly processes of this foundry which is capable of providing high-volume, low-cost modules. A listing of the elements of CIM follows:

- Concurrent Engineering
- Framework CAD Tool Encapsulation
- In-Process Data Management
- Manufacturing Planning and Control
- Process and Test Data Collection and Analysis
- Product Data Management, Control, and Customer Data Interface.

In addition to capabilities supporting the CIM concept, enhancements are necessary to support high-volume production and advanced technology requirements. In computer aided engineering (CAE), tools supporting high-speed part module libraries/electrical analysis, and thermal analysis are needed. In computer aided design (CAD layout), analysis tools supporting transmission line analysis, back annotation, and impedance and switching noise in power and ground structures are necessary.

For manufacturing, interfaces between the MCM foundry and existing TI planning and control systems are required. Data management capabilities are required to manage in process data on a part-by-part basis. An additional factory control system will be considered for insertion in the future (MMST). This system, now in development at TI, will be evaluated to determine what resources will be required to extend the system capability to include the requirements for MCM processing.

Test methodologies and tools for fault simulation are required. Methods to automatically capture test vectors at the design level and supplement them for functional test are also needed. Test software and hardware that takes advantage of boundary scan must be implemented. Improved test methods such as BIST, BIT, and SCAN are required. Finally, hierarchical test methods must be implemented.

5.6.2 Manufacturing

A plan has been defined and presented that shows the natural evolution of a prototype/ lab facility located at the GE-CRD site to a low volume manufacturing facility at located at TI followed by market driven extension into a co-located high volume/low cost facility. An aggressive business plan has been detailed in sections 3 and 4, which will bring the low cost high volume facility on line by early 1994. The work required to execute this business plan, while significant, is of acceptable risk based on existing knowledge of the market, existing and planned manufacturing enhancements, and DARPA involvement.

Many of the elements that reduce the risk are already in place at TI or GE. An existing clean room has been identified at TI containing 11,000 sq ft of space that can be utilized by the MCM foundry. This clean room will co-locate the low volume and high volume facility to promote process commonality and common manufacturing learning.

TI's leadership position in the Semiconductor and PWB manufacturing industries provides leverage in the areas of manufacturing technology and facility automation. These skills, coupled with GE's strong material science and technology development capability will give the TI/GE team a clear advantage in the developing MCM marketplace. This team has already identified more than 20 enhancements to the baseline GE-HDI MCM process as a part of a manufacturing improvements roadmap, and more improvements are expected as the real challenges of low cost/high volume manufacturing are addressed.

Factory modeling has been completed that indicates the impact of these enhancements on product cost and facility return on investment. This capability will allow the TI/GE team

to evaluate new potential enhancements and further refine the MCM production cost estimates.

The baseline GE-HDI process will be initially installed in the TI low volume factory under the DARPA Merchant MCM Foundry (90-09) Program. Existing knowledge and methods will be transferred from GE to TI, and as the production enhancements are implemented at the TI facility, upgraded capability will be transferred back to GE. The TI/GE team has developed an excellent working relationship with truly complementary skills, and this symbiotic relationship is expected to continue beyond the initial startup phase of the MCM foundry to provide a two way flow of technology and manufacturing advancements.

5.6.3 Integration of Technologies

A powerful extension of the system level packaging solution capability of the GE HDI technology will be integration with the 3-D memory packaging capability. 3-D memory packaging, developed by TI with DARPA funding, provides tremendous leverage at the system level in design, packaging density, and performance. GE-HDI provides impressive advantages in system level packaging for 2-D IC arrays with unequalled performance capability in thermal, mechanical, electrical, and reliability environments. When combined, these integrated approaches will allow system designers to achieve tremendous improvements in system packaging performance.

5.6.4 Technology Enhancements

Equally as important will be the integration of high volume manufacturing techniques including, the best processing elements of the chip first and chip last technologies, as a part of the SWAP foundry program. Taking advantage of the key manufacturing features of either MCM approach and progressively implementing high volume manufacturing enhancements will result in the highest performance, and lowest cost interconnect approach achievable.

Significant planned improvements will be:

- Pre-molded substrates with metal 0 applied
- Laminate polyimide film for all layers
- Batch lamination of carriers
- Layer 1 pads swapped to grid in design layout; adaption on layer 1
- High rate via and interconnect patterning processes (masks, improved lasers, etc.)

Insertion of these enhancements will retain all of the unique benefits of the baseline HDI process in rapid prototyping due to the adaptive lithography feature and low nonrecurring costs, while increasing the technology cost advantage over other approaches in both low and high volume production. The choice of a specific fabrication path, of either the enhanced baseline adaptive process or the enhanced high volume fabrication process, will be determined according to a customer's requirements of volume, cost, and schedule.

Unique among all MCM approaches is this ability to transfer without redesign or change in performance from single part prototypes to high volume production.

5.6.5 Additional Foundry Capabilities

Ultimately, with the completion of the applied manufacturing enhancements effort, either a chip first (HDI) or a chip last (TI SOS) interconnect can be fabricated with the same processing equipment and basic set of manufacturing processes. This will result in a foundry able to serve any customer's needs with either type of interconnect. The selection of which type of MCM interconnection to use will depend on the customer's particular requirements and demands. This will result in a capable suite of technologies within a low cost production facility, and the ability of that facility to meet the customer's needs with the lowest cost approach.

5.7 APPLIED MFG IMPROVEMENTS PROGRAM

5.7.1 Impact to the Mature MCM Foundry

The potential impact of an applied manufacturing improvements program to the MCM foundry is illustrated in Figure 5-1. The line labeled Foundry Volume represents the total MCM product volume per the accelerated business plan described in section 3. The line labeled "Market Forecast" represents the price less chip figure potential customers have established as a target (ref. Electronicast). The upper dashed line, labeled "Commercial Baseline", represents the price less chip targets the foundry would need to receive to make an acceptable return on the investment (capital and facilities) and operating costs (payroll and variable overhead) that an extension of the baseline process represents. The impact of the manufacturing improvements program is illustrated by the lower dashed line, labeled "Commercial Enhanced", which represents the price less chip targets the foundry would charge to make an acceptable return on investment and cost with lower capital and labor content in the extended, high volume factory (ref. sec 4.6). The difference between these two lines, "Commercial Baseline" and "Commercial Enhanced", is the potential reduction in production cost associated with executing the manufacturing improvements described within this study.

It is reasonable to assume that execution of an improvements program in the 1992 through 1995 time frame, just leading the developing MCM high volume market gap, would have major impact on domestic market customer requirement support. This anticipated improvement in the competitive position of the foundry is also expected to accelerate penetration into the market segments highly sensitive to cost. Creating the potential for improved market penetration will:

- Reduce product cost more quickly, both military and commercial
- Accelerate the foundry business base growth, opening new markets
- Increase the potential to serve segments highly cost pressured
- Reduce the risk of off shore MCM production and the corresponding loss of the United States leadership position in the computer industry.

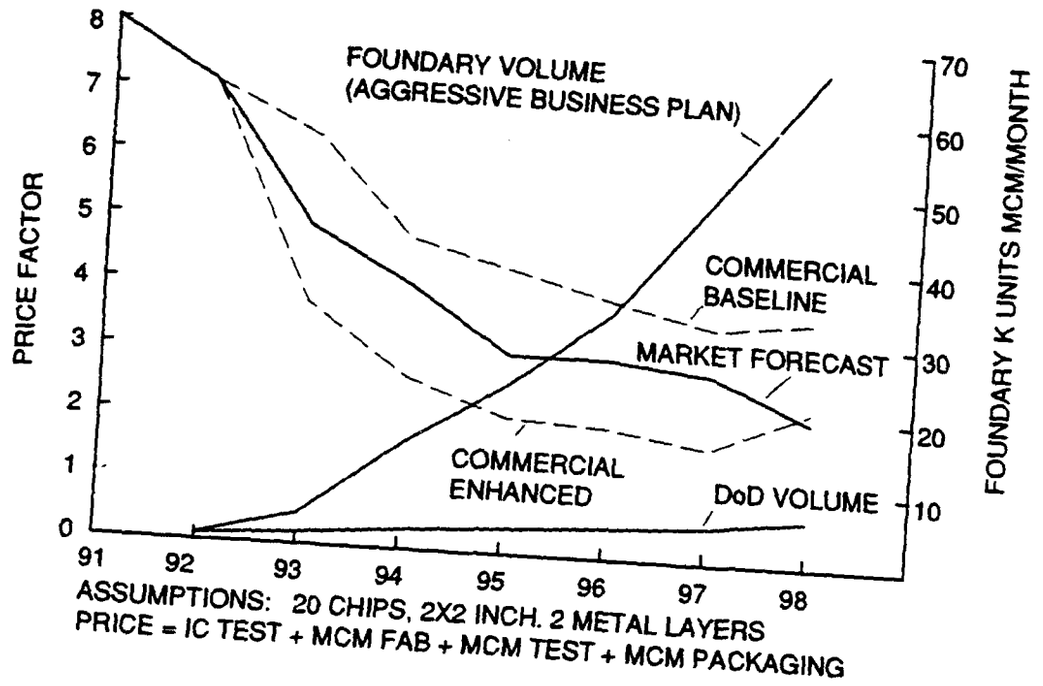


Figure 5-1. Applied Manufacturing Improvements Program Impact to MCM Foundry

5.7.2 Impact to DoD

The potential impact of an applied manufacturing improvements program to the DoD is illustrated in Figure 5-2. The lines labeled DoD Volume 1 and DoD Volume 2 represent two assumptions for projected MCM foundry DoD business base. Assumption 1 projects 10% of foundry product for government applications, and assumption 2 projects 20%.

The DoD Volume 1 assumption is nearly substantiated by programs identified at present. It is reasonable to view this forecast as conservative for the following reasons:

- Missile and smart munitions DoD segments are identified as the high volume areas of the government applications
- The strengths of MCM advanced packaging are essential to the missile and smart munitions applications, where the packaging performance benefits translate directly into improved system performance
- The 90% commercial, 10% government market mix is a forecast for the industry in general
- The SWAP foundry mix of commercial to DoD product mix will differ from that of the general market forecast; this will be a "dual use" facility, unlike most other MCM suppliers, which will tend to increase the relative proportion of DoD production.

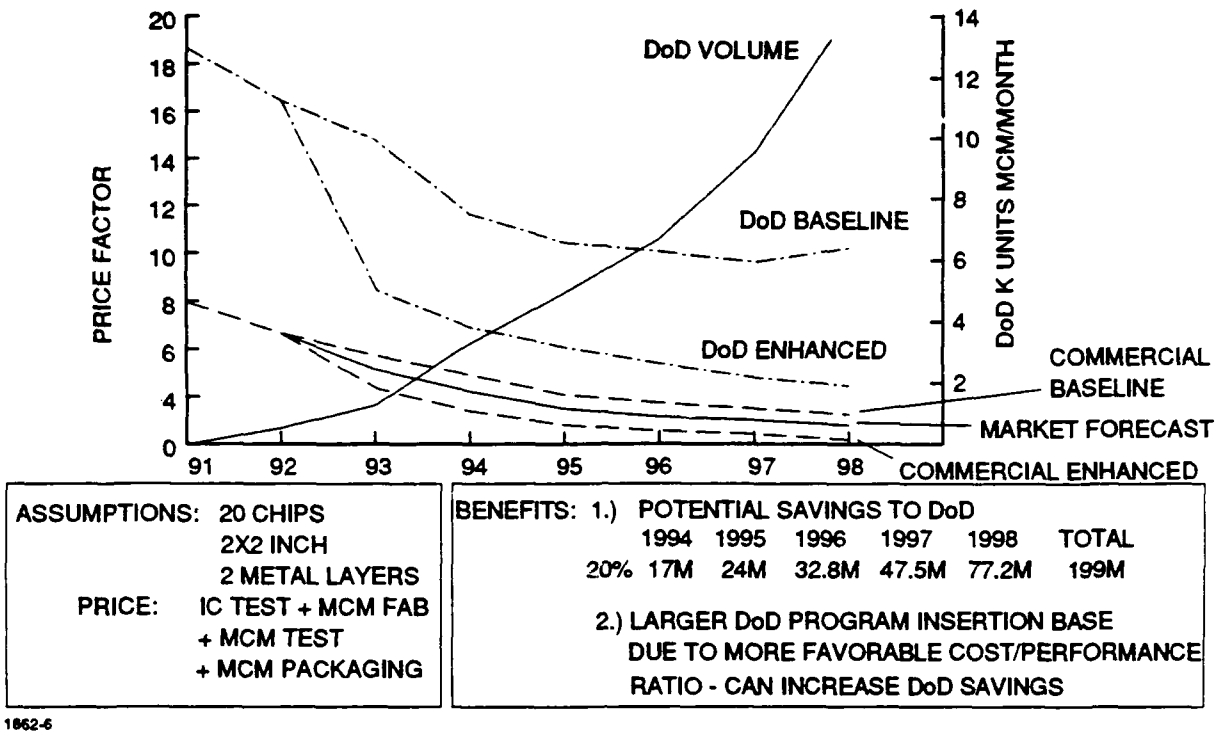


Figure 5-2. Applied Manufacturing Improvements Program Impact to DoD

For these reasons, a second case was identified, where DoD products are 20% of the Merchant foundry business base. It should be noted at this point that in doubling the DoD business base within the foundry, TI/GE have either reduced the commercial base by 10% or increased the total foundry base by approximately 10%. Neither change is significant enough to impact the business plan. This leads to the conclusion that a "dual use" MCM foundry is also advantageous to the government not only for cost reduction but for available capacity, as it will be sized for commercial volumes, and support for high volume DoD applications will certainly be in place.

As in the previous figure, the line labeled "Market Forecast" represents the price less chip figure potential customers have established as a target for commercial MCM products (ref. Electronicast). The "Commercial Baseline" and "Commercial Enhanced" lines are to a different scale, but represent the same data points as in section 5.7.1. The "DoD Baseline" trend represents the price less chip targets the foundry would charge to make an acceptable return on investment and cost when the baseline capability is extended to high volume production. The "DoD Enhanced" line represents the price less chip targets the foundry could operate to as a result of a manufacturing improvements program resulting in improved yields, lower with lower capital and labor content in the extended, high volume factory (ref. sec 4.6). The difference between these two lines, "DoD Baseline" and "DoD Enhanced", is the potential reduction in production cost associated with executing the manufacturing improvements described within this study.

Summing these potential savings between 1994 and 1998 for the accelerated business plan results in a bandwidth of potential savings, ranging from a minimum of $ 99M for DoD Volume 1 to $ 199M for DoD Volume 2. It is reasonable to conclude that potential savings for DoD applications is approximately $ 200 M or greater.

6.0 RECOMMENDATIONS

6.1 INTEGRATION OF MERCHANT MCM FOUNDRY AND SWAP PROGRAMS

TI and GE recommend that DARPA consider the integration of the Merchant MCM Foundry initiated from the Merchant MCM Foundry program and any follow on effort from this Silicon Wafer Advanced Packaging program. The conclusions reached in this study confirm these DARPA sponsored MCM insertion programs have complementary elements within the individual program scope. When combined, the Merchant MCM Foundry program and the SWAP program address the whole of the MCM technology insertion challenge.

It is the conclusion of TI and GE, based on market research conducted for this study, that the initial needs of MCM customers will be served by a facility much like that addressed in Merchant MCM Foundry. The Merchant MCM Foundry program is targeted at technology transfer from a prototype laboratory environment to a low volume, baseline manufacturing environment. The resulting facility will be capable of meeting customer needs for:

- High mix of part numbers
- Small volume part number runs
- High performance capability
- Insertions driven by customer performance requirements
- Primarily DoD applications.

Using the Merchant MCM Foundry facility as a starting point, this study concludes that building an adjacent high volume, low cost manufacturing facility will meet both the objectives of the SWAP program and market requirements after 1993. This factory will primarily address:

- Broad-based customer support
- Greater than 1000 units per part number
- Low cost manufacturing techniques
- Medium performance applications, cost driven market segments
- Fully integrated design to manufacturing systems
- Rapid prototyping capability
- Quick design to manufacturing cycle times
- Mixed DoD and commercial applications

6.2 SWAP FOLLOW ON PROGRAM

TI and GE propose that DARPA sponsor an Applied Manufacturing Improvements program as a follow on to the SWAP study phase. This program should build on the Merchant MCM Foundry baseline technology transfer program. Using the low volume manufacturing capability with the Merchant MCM Foundry effort, effort should then concentrate on a systematic foundry capability development to address all areas of the high volume, low cost need. Elements of the program should be:

- CAE/CAD/CAT/CIM development
- Applied process and material development
- Industry and government infrastructure development.

The SWAP program can be the catalyst for enabling the domestic industry to penetrate the rapidly approaching market gap that is clearly developing. Areas to be addressed with such a program span manufacturing capability and supporting industry and government infrastructure. Benefits of a successful program in these areas are enormous - for the government, for commercial users, and for the merchant foundry.

6.3 INSERTION PROGRAMS

DARPA sponsorship of several strategic insertion programs to transition production MCM technology into the program offices is recommended. Potential candidates include:

- SADARM
- ATCURE
- ALLADIN follow on applications
- LH
- ATF
- other (SDIO, Satellite).

MCMs are a part of the packaging strategy on the ATCURE program. This program offers an opportunity to develop manufacturing capability with an applied manufacturing requirements program targeted at genuine DoD needs. There is potential on the ATF FSD phase for insertion of MCM packaging technology in the Mission Display Computer and on the jet engine control system. These and other DoD applications should be evaluated. DARPA is in a prime position to sponsor government and industry teaming for MCM insertions in these and similar program areas.

APPENDIX A

SILICON WAFER ADVANCED PACKAGING PROGRAM

MULTICHIP MODULE

CUSTOMER SURVEY

SILICON WAFER ADVANCED PACKAGING PROGRAM
MULTICHIP MODULE
CUSTOMER SURVEY

For the purposes of this survey, a multichip module is defined as a multilayered, high density interconnect structure combining multiple chips on a common substrate.

1. What is your primary customer base?

   41% Commercial
   59% Military
   _____ Both (please specify: _____% Commercial, _____% Military)

2. Please identify your multichip module requirements in the following table. Assume 100 square inches of board surface area will equate to four (4) MCMs.

Product Application	1991	1992	1993	1994	1995	1996	1997	2000
Automotive								
Avionics	250	4369	11.4K	18K	29.5K	138K	131K	428K
Consumer								
Computer								
• Mainframe	35	46	300	600	1000	10K	10K	10K
• Workstations	100	98K	150K	175K	105K	130K	170K	200K
• PC/Laptop/ Notebooks								
Missiles	5	70	550	1084	2130	2228	2220	7020
Munitions			500	60	510	70	520	70
Satellites	80	139	1063	1158	1340	1455	1658	1950
Telecom								

3. Does your company plan to fulfill its MCM requirements from internal production?

   25% Yes
   75% No

4. What are your MCM cost targets? Cost shown is less die.

$ Per Sq. In.	1991	1992	1993	1994	1995	1996	1997	2000
$200 - 150	100%	75%	29%	14%	13%	14%	17%	14%
149 - 100	0%	25%	67%	67%	46%	19%	0%	4%
99 - 50	0%	0%	1%	19%	40%	53%	33%	24%
< 50	0%	0%	3%	0%	1%	14%	50%	57%

5. Please check the box which best describes the level of service you would expect a MCM foundry to provide:

Customer Input*	Service Desired**	Foundry Output
36% Artwork Database/Test Program	45%	MCM Fab, Test
64% Net List/Schematic Parts List	64%	CAD Layout, MCM Fab, Test
64% Module Specification	36%	Up-front Analysis (Analog, Digital, Thermal Simulation), Electrical Design, CAD Layout Fab, Test

* Respondents would provide.

** Respondents expect.

6. What is the cycle time requirement from your input to foundry output?

5-6 Weeks ARO Fab Only
10 Weeks ARO CAD Design and Fab

7. What percentage of your MCM designs are in the following categories?

20% Repackaging of existing functional design
66% New functional design
24% New IC designs (ASIC)

8. What CAD system(s) do you plan to use for multichip designs?

15% Cadence
27% Dasix
____ Internally developed SW
27% Integraph
91% Mentor
____ Racal-Redac
36% Valid
____ Viewlogic
9% Other

9. What system circuit analysis do you need?

64% Transmission Line
73% Parametric (inductive capacitance)
82% Timing Analysis
64% Behavorial Level Analysis
18% Other

10. What hardware do you run your CAD software on? (Please specify)

18% PCs (_____)
91% Workstations (_____)
18% Mainframes (_____)
9% Combination of above (_____)

11. Of your total MCM designs, what percentage of the following functions are required?

14% Linear
23% Logic
41% Microprocessor
38% Memory
0% Other (Please specify _____)

12. How many ICs will be incorporated in your multichip module?

1% <5
27% 5 - 10
33% 10 - 20
20% 20 - 30
20% >30

13. How many I/O will the chips in your MCM have?

18% <100
40% 100 - 250
23% 250 - 400
11% 400 - 700
22% >700

14. How many I/O will your multichip module require?

12% <100
28% 100 - 250
36% 250 - 400
24% 400 - 700
_____ >700

15. What will be the equivalent gate count of the multichip circuit?

3.3E6 Equivalent gate count RANGE: (0.1 - 4.8) E6

16.

System Performance Goals	1991 (% Total)	1995 (% Total)	1998 (% Total)
<25 MHz	24	10	5
25 - 50 MHz	41	33	23
50 - 75 MHz	12	12	22
75 - 100 MHz	11	14	12
>100 MHz	12	30	38

17. What temperature environment will your multichip module be operating in?

8% Room ambient
58% -55°C to +125°C
11% 0°C to +40°C
23% Other (Please specify_____)

18. What substrate interconnect material would you prefer for your multichip module?

25% Polymer
19% Ceramic
25% Silicon
31% Other (Please specify_____)

* Please explain your preference _____
_____

19. What kind of package do you prefer your multichip module in?

6% Hybrid Leaded (glass lead feedthru)
12% Pin Grid Array
24% Gull Wind Leaded Surface Mount
12% Commercial Grade
35% Military Grade
12% None

20. What is the forecasted power dissipation of your multichip module?

53 Watts (AVERAGE) RANGE 5-100 WATTS

21. What kind of interconnect do your plan to interface you MCM to?

	1991 (% Total)	1995 (% Total)	1998 (% Total)
Thru-hole PWB	0	0	0
Combined SMT/Thru-hole MLB PWB	29	21	13
High reliability constrained SMT PWB	46	56	51
Other (Please describe)	25	23	36

* Data represents summary of raw respondent data. All data, with the exception of Question #2 reference above, is shown as a percentage or average of the total response.