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TEST DIAGNOSTICS OF RF EFFECTS IN INTEGRATED CIRCUITS

Martin Marietta Space Systems

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This report presents the results of an effort to measure the RF upset susceptibilities of CMOS and low power Schottky integrated circuits and to demonstrate a test probe methodology for measuring RF noise coupling, generation, and propagation into and upon these integrated circuit chips. RF interference used was continuous wave (CW) from 1MHz to 200 MHz. This was combined with the digital signal using an op-amp combiner and directly coupled into the device ports. Upset threshold voltage levels were measured, complex input impedances were measured, and upset power levels were calculated and plotted. A scanning electron microscope (SEM), quantitative voltage contrast (QVC) system was used to measure internal waveforms along the intended signal path, on adjacent metals runs, and an internal power and ground connections.

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PREFACE

Martin Marietta Astronautics Group submits this Final Technical Report MCR-89-505 to Rome Air Development Center in fulfillment of requirements of contract F30602-87-C-0079, "Test Diagnostics of RF Effects in Integrated Circuits," CDRL item A004, Technical Report (Final).

The work for this contract was performed during the previous two years in the Failure Analysis Laboratory of Martin Marietta Astronautics Group in Denver, Colorado. The instrumentation that was used to perform the internal circuit voltage measurements was developed as a part of an earlier IRAD task at Martin Marietta. Daniel Koellen and Steven Anderson are to be acknowledged for their work on the IRAD and for their significant contributions to this program.

This was a very successful program that provided information on the propagation of RF interference into and upon integrated circuit chips. The information obtained increases the understanding of the RF effects and will be valuable to RADC for validating new SPICE models.

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1.0 INTRODUCTION

Integrated circuits (IC's) have revolutionized circuit design for commercial and military electronics. There are several advantages to using integrated circuits versus using discrete components in electronic systems. Their use reduces system weight and size, increases reliability, and may reduce cost. These advantages become more significant as the integrated circuit complexity and density increases.

The disadvantages also become more significant with the complexity and density increase. The trend is toward IC's which operate at higher frequency, lower power and with closer physical placement of individual circuit elements on the IC chip. These characteristics cause the IC's to be more susceptible to electrical overstress and damage due to electrical transients such as electrostatic discharge (ESD). Integrated circuit manufacturers have addressed many of the problems with innovations in processing, layout, and design. For example, protection networks have been incorporated in many integrated circuits that reduce their susceptibility to damage due to ESD.

The manufacturers have not adequately addressed the electromagnetic compatibility (EMC) of integrated circuits. EMC means that the integrated circuit will be able to function as intended in its end-use electromagnetic environment to a large extent. The manufacturers have not measured the susceptibility of integrated circuits to electromagnetic interference and have not considered electromagnetic compatibilty during the design and fabrication phases of manufacturing. It is likely that the susceptibilty of integrated circuits to electromagnetic and radio frequency (RF) interference increases as their complexity increases [1-5]. In order for manufacturers to include EMC in the IC design they need to understand the response of internal nodes to injected interference. The purpose of this study was to develop a method to measure the response of the internal nodes to conducted interference injected into various device inputs and to track subsequent internal propagation.

2.0 PROBLEM DEFINITION

The susceptibility of integrated circuits to upset by injection of RF signals is a quantity that is not specified or measured by the manufacturer. This parameter is important to the circuit designer if a device is to be used in a circuit that will operate in a strong RFI (Radio Frequency Interference) environment. The designer may use extensive shielding and/or filtering to attenuate RFI coupling to the integrated circuit. If the susceptibility of the device to RFI were known, the filtering and shielding required might be reduced or eliminated, perhaps reducing design time, cost, weight and packaging difficulties. The susceptibility of a system to RF signals could be better predicted if the susceptibility of its integrated circuits were known.

An effective way of obtaining EMC would be to use devices that have reduced or no susceptibility to RFI rather than designing external circuitry to obtain the same. Simply measuring or attempting to model the susceptibility of the device to RFI is not the complete answer. The best approach is to design-in EMC at the chip level.

Factors internal to the chip effect the susceptibility to RFI. These factors include processing technology, structure size and placement. Earlier studies performed at Martin Marietta and at RADC [6,7] found that the RF susceptibility of the two functionally identical devices analyzed were different. The two devices studied were the Intel 8086 16-bit microprocessor and the CD4013B dual D-type flip-flop. The structures of the two devices differed in processing technology (NMOS vs CMOS) and in configuration. The evaluation showed that only 2.5 milliwatts of RFI conductively coupled to an input of the 8086 was required for upset while the CD4013B required 300 milliwatts. Thus, while two devices with different configuration and processing can respond properly in their intended operating scheme, they differ substantially in their EMC. Additionally, when the clock input of the CD4013B was modified such that the ESD protection network was removed from the circuit, the device was found to be 8 dB less susceptible. The circuit that was included to protect the device from ESD seems to have increased the device's susceptibility to EMI. The factors contributing to these changes in susceptibility must be understood so that EMC parameters can be included in the design of the device.

New designs for integrated circuits are implemented using computer aided design (CAD) techniques that produce the physical layout of the various processing layers according to design rules. Alignment tolerance, etch tolerance, metal step coverage, current density, via formation and other factors presently influence the generation of the design rules. Design rules that address the device's EMC have not been generated. In order to implement EMC at the initial chip design stage, design rules and CAD parameters must be generated that address the EMC of the device. To do this, one must be able to study the effects of various processing, layout and design factors on EMC. The response of the internal nodes of integrated circuit to RFI needs to be measured without effecting the operation and response of the measured node. Implementing these data into changes in design rules and perhaps into device processing would improve the manufacturer's ability to design-in EMC.

3.0 APPROACH

The approach used to accomplish this study consisted of the following tasks. The appropriate section is listed and a brief summary of the contents is provided.

Section 4 (Task 1) - Literature Review and Vendor Contact
A computer database search of published materials by the Martin Marietta Research Library was performed and the Government Information and Data Exchange Program (GIDEP) Engineering Data Bank was reviewed. Vendors were contacted about including electromagnetic compatibility into their IC design.

Section 5 (Task 2) - Program Plan Development
A program plan was developed which utilized the information gained during the literature review and vendor contacts in conjunction with the initial technical proposal.

Section 6 (Task 3) - Device Selection and Circuit Schematic Development
Four devices were selected for RF upset characterization based upon technology, function, nodal accessibility, chip physical layout, input protection circuit structures, and previous test history. Circuit schematics, logic diagrams, and component physical layouts were developed.

Section 7 (Task 4) - Instrumentation and Test Fixture
Instrumentation was assembled and combiner circuitry was designed and built. Fixturing was designed and built to allow testing of the IC's within the Scanning Electron Microscope (SEM) chamber.

Section 8 (Task 5) - Device RF Upset Characterization
RF upset characterization was performed on two inputs and a power pin for each device. RF interference signals from 1.2 MHz to 200 MHz were combined with the intended signal, and upset levels at which improper device output occurred were measured and recorded.

Section 9 (Task 6) - SEM Quantitative Voltage Contrast Measurements
Circuit internal nodes were measured using SEM quantitative voltage contrast (QVC) with and without RF interference signals. The propagation, attenuation, and intercoupling of the RF signals were measured.

Section 10 - Conclusions

Conclusions from the device upset characterization and the measurements using the SEM QVC system are presented. Comparisons between technologies, device function, and input function are provided.

4.0 LITERATURE REVIEW AND VENDOR CONTACT

This section discusses the literature search and the vendor contacts that were made prior to the preparation of the test plan.

4.1 Literature Review

The Martin Marietta Research Library and the GIDEP Engineering Data Bank were used for the literature search. The following key words were used: eletromagnetic interference (EMI), EMI upset, EMI susceptibility, RF interference (RFI), RF upset, RF susceptibility, EMC, combiner, and integrated circuit. Abstracts for documents were obtained from the following databanks: Defense Research, Development, Test and Evaluation Online Systems (DROLS), the Institute of Electrical Engineers database of Physics Abstracts, Electrical and Electronic Abstracts, and Computer and Control Abstracts (INSPEC), the National Technical Information Service (NTIS), Scientific and Technical Aerospace Reports (STAR), International Aerospace Abstracts (IAA), Applied Science and Technology Index (ASTI), and the Government Publications Index. The abstracts were obtained and selected articles were obtained and reviewed. In addition, recent magazine articles and various symposium proceedings were reviewed. The pertinent articles are listed in the bibliography.

These articles provided useful information in a number of areas and were used during the program plan development.

4.2 Vendor Contacts

The following vendors were contacted: Signetics, National Semiconductor (Fairchild), SGS-Thompson (MOSTEK), INMOS and Unisys (Burroughs). The area of questioning was related to the inclusion of electromagnetic compatibility into their IC design. None of the manufacturers indicated that this was a concern during design. One manufacturer indicated that silicon designs with several parallel metal traces carrying high frequency (greater than 20 MHz) signals are sensitive to capacitive coupling. He stated that a method to compensate for this effect is to use a metallization ground plane separate from the signal line metallization plane.

An EMI problem on a device designed in the late 1970's was identified by one of the manufacturers. A particular input was sensitive to EMI due to coupling of the EMI from the bond pad to an adjacent metallization line. This adjacent line was susceptible due to the small geometry of the transistors to which it was connected. The manufacturer modified his design to include a larger transistor that would not respond to the fast EMI signal, this transistor acted as a low pass filter. This problem did not cause the manufacturer to have a concern about including EMC into design considerations.

The response was surprising since it is imperative that the devices operate as intended in a variety of environments. Relatively common scenarios can produce narrow-band and broad-band interference with enough amplitude to cause a concern [2,3].

It is possible that EMC has been considered to some extent but it has not been fully addressed due to the difficulties of incorporating changes that produce an EMI immune circuit and at the same time do not degrade other parameters of interest, such as operating frequency.

4.3 Conclusions

The literature review provided information on: EMI measurement techniques, upset susceptibility levels and concerns, protect circuitry effects, computer simulations, electromagnetic environments, and internal node voltage measurement techniques. This information helped in the development of the program plan. The vendor contacts provided insight into the lack of data in the area of EMC, reinforcing the necessity of obtaining this type of information.

5.0 PROGRAM PLAN DEVELOPMENT

A Program Plan was written to explicitely identify the tasks to be performed during this study, establish the schedule, and discuss related work. The sections in the Program Plan were: Introduction, Definition of Problem, Approach, Test Method, Data, Test Configuration, Device Selection and Preparation, Work Breakdown Structure, Program Schedule, IRAD Activity, References, and Bibliography.

The contents of the Program Plan are included in the appropriate sections of this report.

6.0 DEVICE SELECTION AND CIRCUIT SCHEMATIC DEVELOPMENT

6.1 Device Selection

There were a number of considerations involved in selecting devices for this study. It was desired to obtain information about the sensitivity of and the sensitivity differences between combinational logic and sequential logic circuits, test different technologies, test different ESD input protect structures, and test circuits which have widespread usage. For the SEM measurements it was important that the passivation could be removed without changing the characteristics of the part and that internal nodes were accessible for probing. Long parallel metallization runs on the die surface were desired to analyze coupling effects.

The criteria used to identify candidate devices for selection are shown below.

Circuit Density
- -Medium and large scale

Manufacturing Technology
- -Bipolar
- -MOS
- -Gallium arsenide

Functional Type
- -Digital
- -Analog

Previous Evaluation Work

Package Type

Thirty-five part types of different densities, technologies and functional types were initially identified. The testability, availability, and cost were then considered and the list was reduced to twelve part types. Additional analyses and evaluations were performed, including destructive physical analysis, and the final selection was made. The four part types selected are listed in Table 6.1.1.

Part Number	Part Name	Technology	Logic Type
CD4013B	D-type flip-flop	CMOS	Sequential
SN54ALS74A	D-type flip-flop	Advanced Low Power Schottky	Sequential
CD4585B	4-bit magnitude comparator	CMOS	Combinational
SN54LS85	4-bit magnitude comparator	Low Power Schottky	Combinational

Table 6.1.1 - Device Description

Data sheets for each of these device types are provided in Appendix A.1.

These device types provide a direct comparison between functionally similar circuits processed from complementary metal-oxide-semiconductor (CMOS) and Schottky technologies.

6.2 Pin Selection

Three pins on each device were selected for injection of RFI. These were selected as a result of an evaluation of their function, the results of previous studies [6,7], and by their electrical and physical internal paths. A variety of input protect structures, physical layouts, and electrical functions were desired to obtain as much comparison data as possible. The CD4013B had been tested previously [6,7] with RF being injected into power (Vdd) and the clock and data inputs. These pins were also used during this test on both of the D-type flip-flops. Power is labelled Vdd for the CMOS device and is labelled Vcc for the Schottky device.

For the 4-bit magnitude comparators, the pins selected were power (Vdd or Vcc) and the B0 and B3 inputs. There were many more possibilities on this part type than on the flip-flop. Many factors were considered, with the final selection being primarily determined by the combination of the electrical function and the physical internal path. The B0 input has one of the longest metal runs to the first gate on the CMOS circuit. The B3 input has one of the shortest metal runs to the first gate. For the Schottky device there was little physical difference between pin layouts. Functionally these two pins are the least significant (B0) and most significant (B3) bits for word B. This should provide an interesting comparison by function.

6.3 Device Description

The CD4013B and the SN54ALS74A are dual D-type positive-edge-triggered flip-flops. Each IC has two identical independent flip-flops and each flip-flop has a single data input. The logic level present at the data input is transferred to the Q output during the positive-going transition of the clock pulse. The functional diagrams for both device types are shown in Figure 6.3.1.

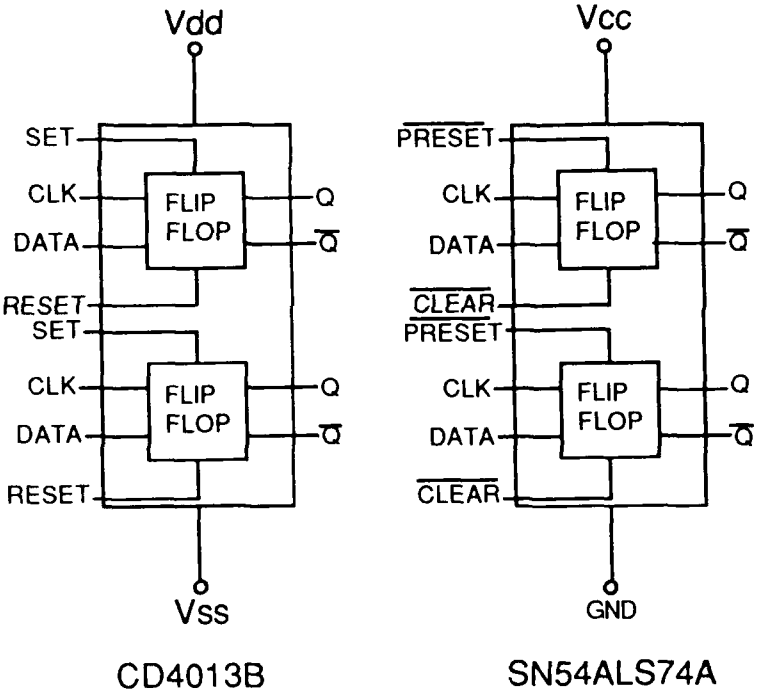


Figure 6.3.1 - Flip-Flop Functional Diagrams

The set input on the CD4013B is equivalent to the preset-not input on the SN54ALS74A. The reset input on the CD4013B is equivalent to the clear-not input on the SN54ALS74A. These inputs are equivalent, however they require the opposite logic levels as shown in Table 6.3.1.

CD4013B

INPUTS				OUTPUTS	
Set	Reset	Clock	D	Q	Q-not
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H
L	L	L to H	H	H	L
L	L	L to H	L	L	H

SN54LS74A

INPUTS				OUTPUTS	
preset-not	Clear-not	Clock	D	Q	Q-not
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	L to H	H	H	L
H	H	L to H	L	L	H

H = Logic high level
L = Logic low level
X = Don't care

Table 6.3.1 - Function Tables for Flip-Flops

For the CD4013B, a high level on the reset input produces a low level on the Q output and a high level on the Q-not output. A high level on the set input produces a high level on the Q output and a low level on the Q-not output. When reset and set are low, the logic level on the D input is transferred to the Q output at the rising edge of the clock pulse.

For the SN54ALS74A, a low level on the clear-not input produces a low level on the Q output and a high level on the Q-not output. A low level on the preset-not input produces a high level on the Q output and a low level on the Q-not output. When clear-not and preset-not are high, the level on the D input is transferred to the Q output at the rising edge of the clock pulse.

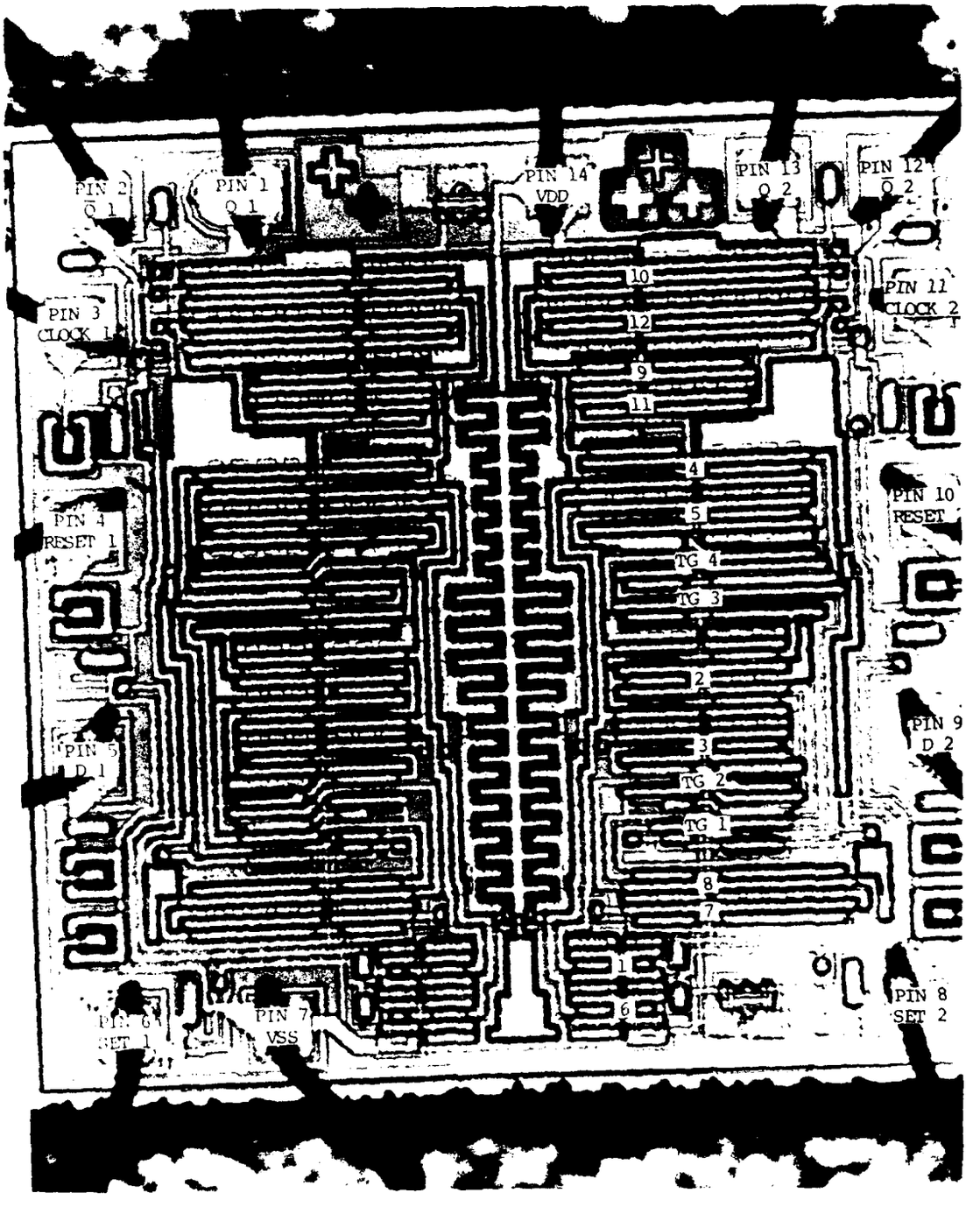


Figure 6.3.2 - CD4013B Die Photograph With Labels

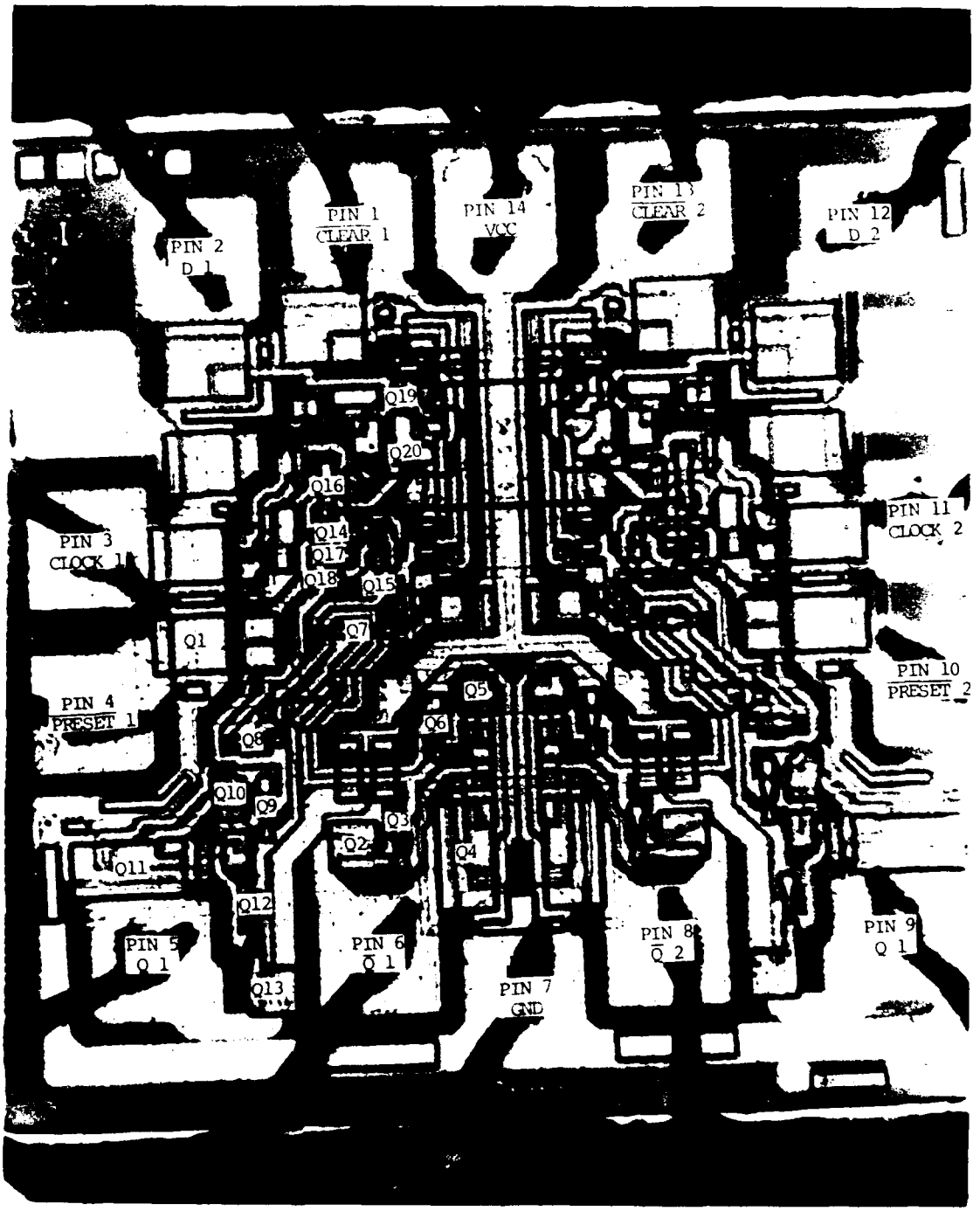


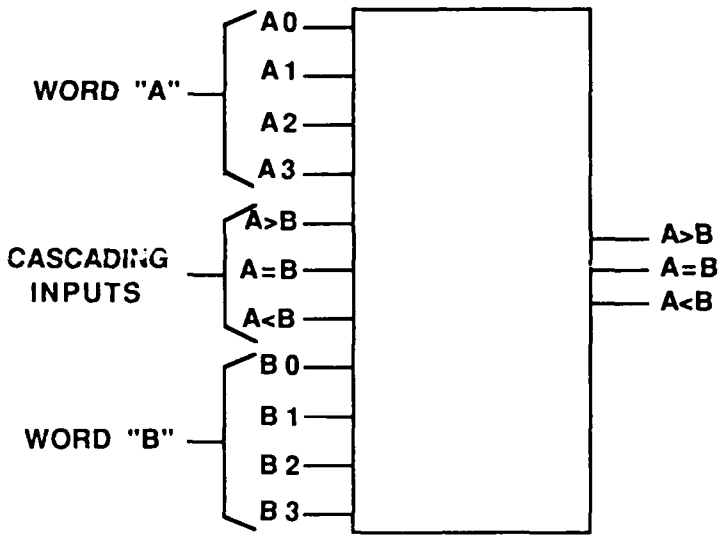
Figure 6.3.3 - SN54ALS74A Die Photograph With Labels

The CD4013B IC's are in 14-lead dual-in-line ceramic packages (CERDIP's). They are manufactured using complementary n-channel and p-channel metal-oxide-semiconductor field effect transistors (MOSFET's). The substrate is n-type silicon. A die photograph is shown in Figure 6.3.2. The die measures 67 mils by 67 mils. The interconnect bond wires are 1.2 mil aluminum. The minimum linewidth of the aluminum metallization is 9 microns and the minimum spacing between lines is 8.5 microns. The recommended maximum operating clock frequency with 5 volts on Vdd is 3.5 megahertz (MHz).

The SN54ALS74A IC's are in 14-lead CERDIP's. They are manufactured using advanced low power Schottky (ALS) bipolar transistor technology. The substrate is p-type silicon and individual collector tubs are isolated along the surface of the die with a silicon dioxide (SiO_2) insulator. A die photograph is shown in Figure 6.3.3. The die measures 45 mils by 45 mils. The interconnect bond wires are 1 mil aluminum. The minimum linewidth of the aluminum metallization is 4.2 microns and the minimum spacing between lines is 6.5 microns. The recommended maximum clock frequency with 5 volts on Vcc is 25 MHz.

The CD4585B and the SN54LS85 are 4-bit magnitude comparators. These circuits compare two 4-bit words, A and B, and provide the response to this comparison at the output pins. The output pins are A<B, A=B, and A>B. In addition, there are three cascade inputs which can be connected to the outputs of another 4-bit magnitude comparator to allow comparison of two 8-bit words. The cascade inputs form the least-significant bits and are therefore active in affecting the output of the comparator in the case where the two 4-bit A and B words are equal. The functional diagram for these device types is shown in Figure 6.3.4.

The function table is shown in Table 6.3.2. The values in parentheses are for the CD4585B. Where there are no parentheses, the input states for both device types are identical. The primary result of the differences noted in the function of the two circuits is that for the top four rows in the function table, a high logic level is required on the A>B cascade input on the CD4585B for the circuit to function correctly. A low logic level on the A>B cascade input causes the A>B output to be low, regardless of the values for word A or B.



CD4585B Vdd=16 Vss=8

SN54LS85 Vcc=16 Gnd=8

Figure 6.3.4 - Comparator Functional Diagram

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3,B3	A2,B2	A1,B1	A0,B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3	X	X	X	X	X	X(H)	L	L	H
A3=B3	A2>B2	X	X	X	X	X(H)	L	L	H
A3=B3	A2=B2	A1>B1	X	X	X	X(H)	L	L	H
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X(H)	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L(X)	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L(X)	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	H	L	L

H = Logic high level
L = Logic low level
X = Don't care

Table 6.3.2 - Comparator Function Table Note: ( ) are for the CD4585B, rest of data valid for both device types.

The CD4585B IC's are in 16-lead CERDIP's. They are manufactured using complementary MOSFET's using an n-type silicon substrate. A die photograph is shown in Figure 6.3.5. The die measures 100 mils by 75 mils. The interconnect bond wires are 1.2 mil diameter aluminum. The minimum linewidth of the aluminum metallization is 9 microns and the minimum spacing between metallization lines is 8.5 microns. This device does not have a recommended maximum clock frequency like the CD4013B or SN54ALS74A since it has no clock input. The specification related to frequency is the propagation delay time between a change in the input logic level and the time at which the output is guaranteed to be correct. The maximum propagation delay is 600 ns at Vdd = 5 volts.

The SN54LS85 IC's are in 16-lead CERDIP's. They are manufactured using low power Schottky (LS) bipolar transistor technology. The n-type collector tubs are junction isolated in contrast to the SN54ALS74A ALS process which has dielectric isolation. A die photograph is shown in Figure 6.3.6. The die measures 65 mils by 58 mils. The interconnect bond wires are 1 mil diameter aluminum. The minimum linewidth of the aluminum metallization is 4 microns and the minimum spacing between aluminum metallization lines is 10 microns. The maximum specified propagation delay time is 45 ns at Vcc = 5 volts.

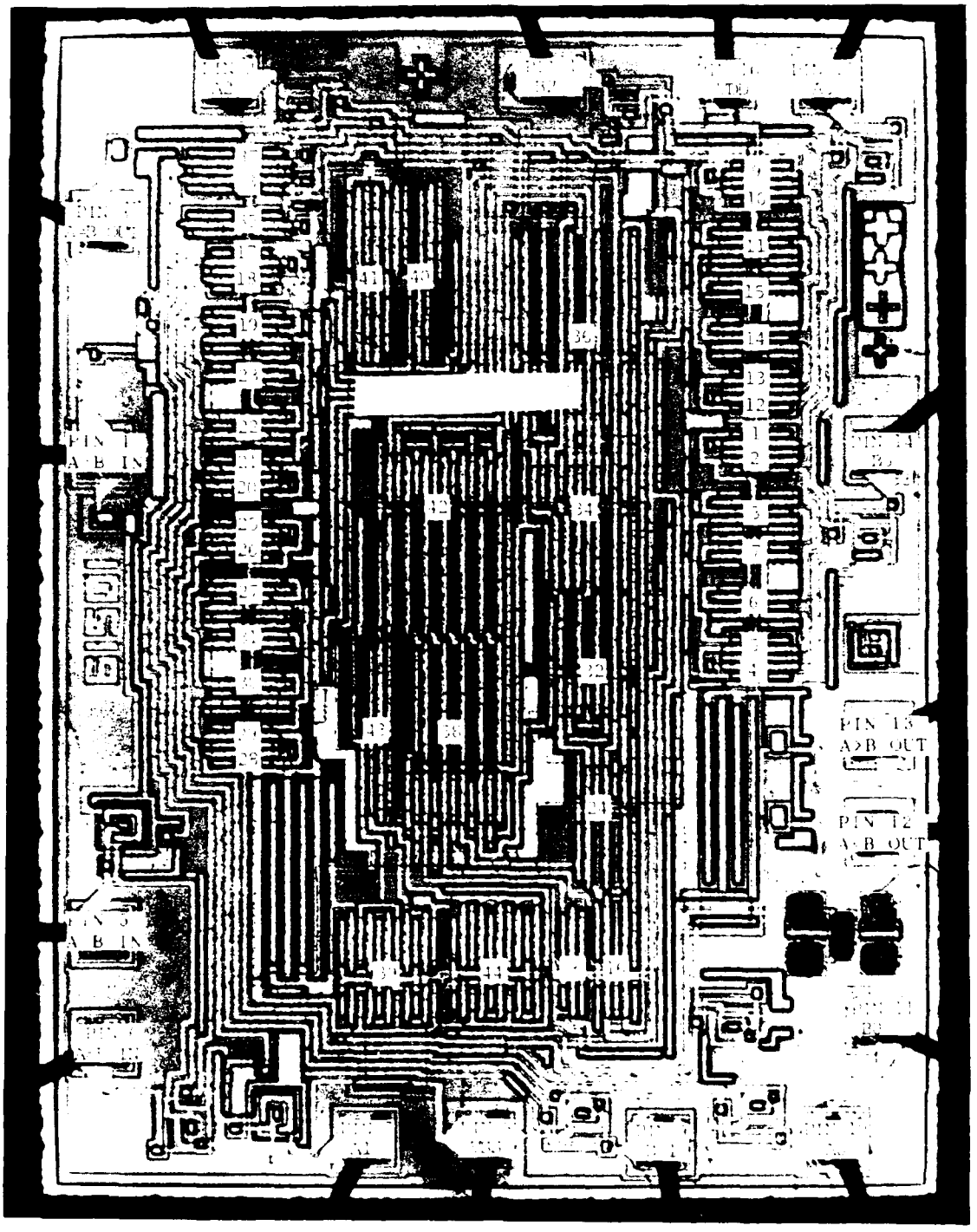


Figure 6.3.5 - CD4585B Die Photograph With Labels

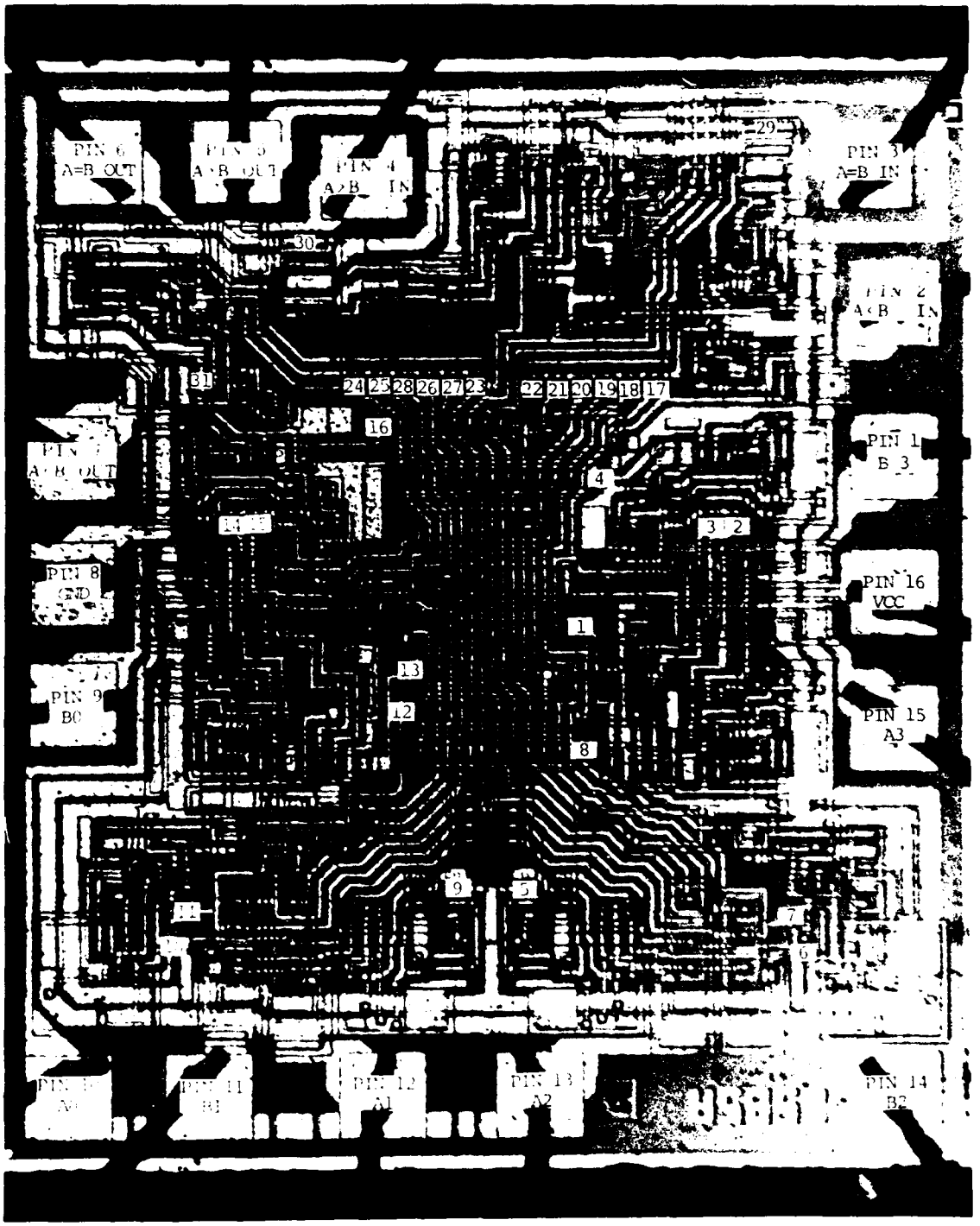


Figure 6.3.6 - SN54LS85 Die Photograph With Labels

6.4 Circuit Schematic and Physical Layout

The circuit schematics and the physical layouts of each of the four devices were developed to allow internal node identification for measurement using the SEM. A ten inch by sixteen inch photograph was used initially to identify each of the transistors on the devices. From this, a logic diagram was developed and the gates were numbered. The logic diagrams and the gate locations are shown in the following sections.

6.4.1 CD4013B

The overall photograph of the CD4013B with the pins and gates labelled was shown in Figure 6.3.2. The numbering for the gates is provided in the logic diagram in Figure 6.4.1.1. Individual gates are standard CMOS structures such as the inverter, NAND, and transmission gate shown in Figure 6.4.1.2. The structure for the clock input is shown in Figure 6.4.1.3 and for the data input in Figure 6.4.1.4.

6.4.2 SN54ALS74A

The overall photograph of the SN54ALS74A with the pins and a portion of the transistors labelled was shown in Figure 6.3.3. The numbering of the transistors is provided in Appendix A.1 on the schematic supplied by the manufacturer. The complete schematic was not developed. The logic diagram from the data sheet is provided in Figure 6.4.2.1. An adequate number of components were identified to allow identification of the nodes of interest. The structure for the clock input is shown in Figure 6.4.2.2 and the structure for the data input is shown in Figure 6.4.2.3.

6.4.3 CD4585B

The overall photograph of the CD4585B with the pins and gates labelled was shown in Figure 6.3.5. The numbering for the gates is provided in the logic diagram in Figure 6.4.3.1. Individual gates are standard CMOS structures such as the inverter, NAND, and NOR gate illustrated in Figure 6.4.3.2. NOR gates with additional inputs, such as gate 36, are produced by placing additional p-channel FET's in series and n-channel FET's in parallel. The input structure used for both B0 and B3 is shown in Figure 6.4.3.3.

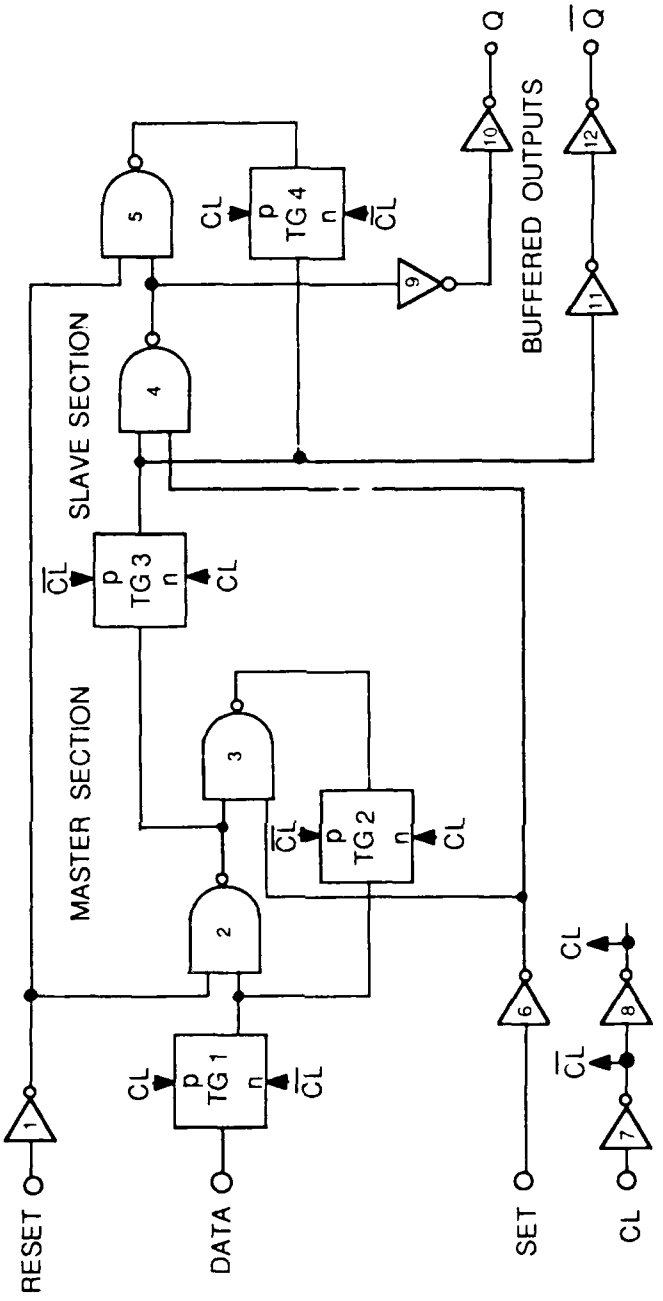


Figure 6.4.1.1 - CD4013B Logic Diagram
Note: Transmission gates are numbered TG 1 through TG 4, logic gates are numbered 1 through 12, inputs are on the left hand side, and outputs are on the right hand side.

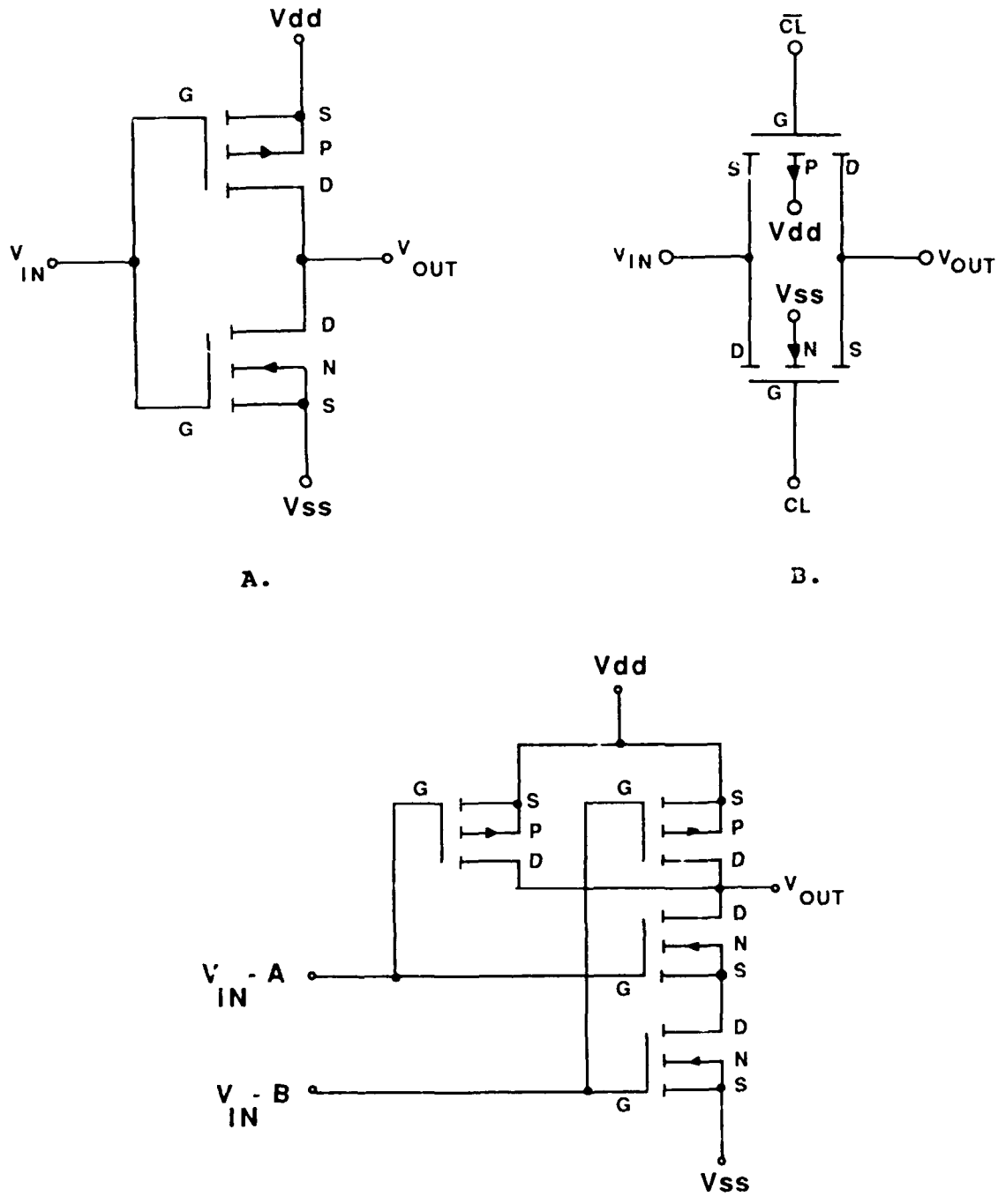


Figure 6.4.1.2 - CD4013B CMOS Logic Configuration,
A. Inverter
B. Transmission Gate
C. NAND Gate, Two Input

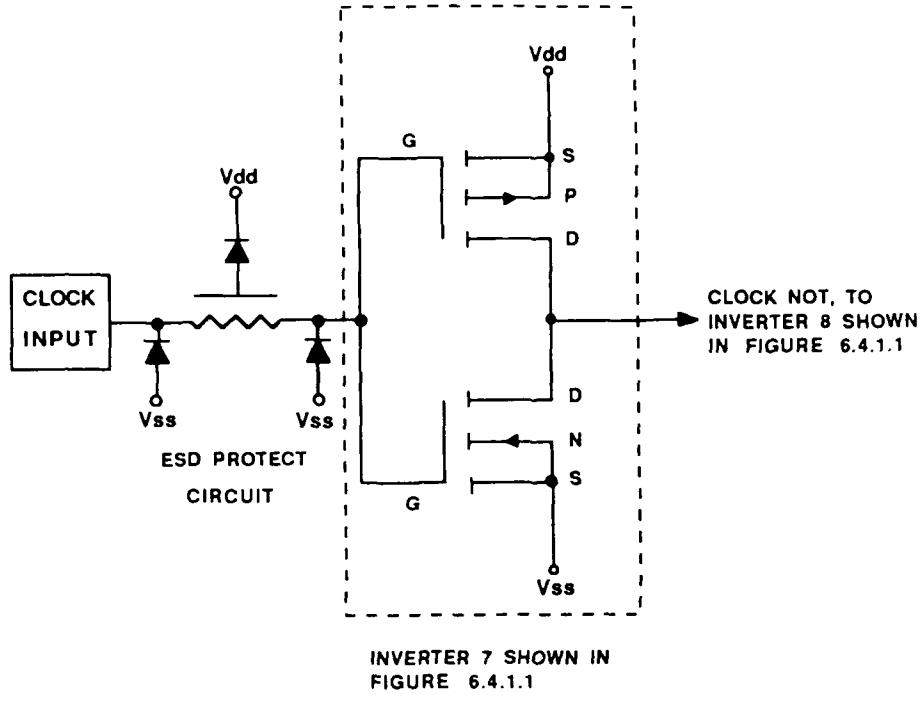


Figure 6.4.1.3 - CD4013B Clock Input Circuit

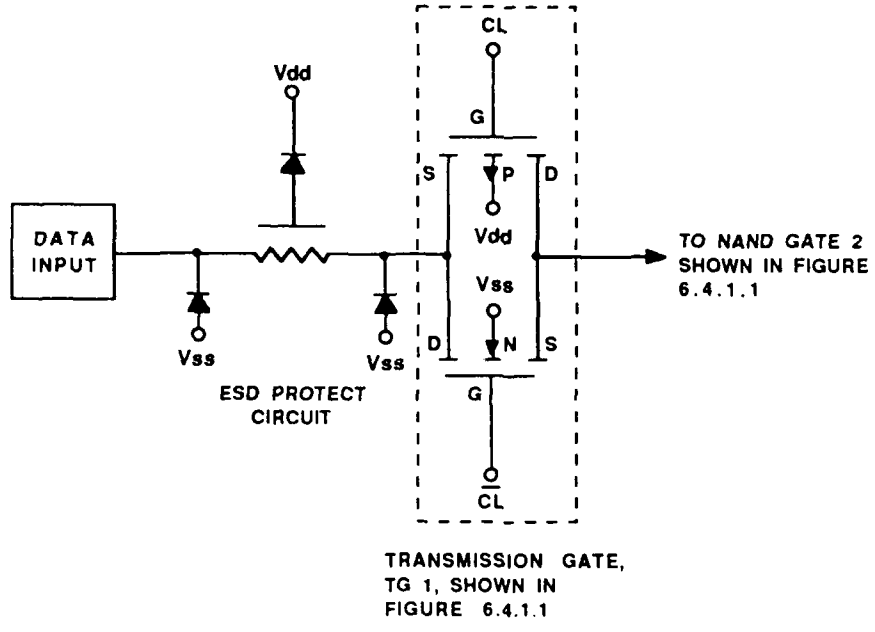


Figure 6.4.1.4 - CD4013B Data Input Circuit

54ALS74 LOGIC DIAGRAM

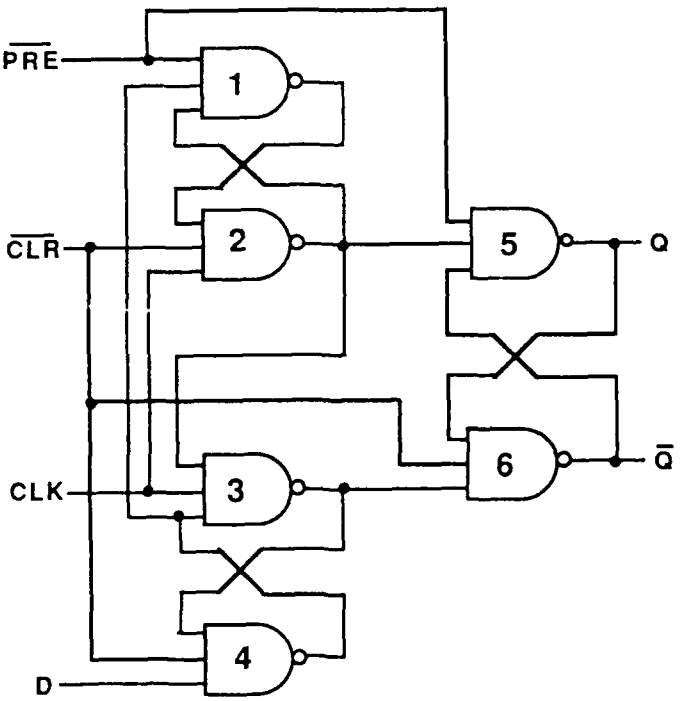


Figure 6.4.2.1 - SN54ALS74A Logic Diagram
Note: Logic gates are numbered 1 through 6, inputs are on the left hand side, and outputs are on the right hand side.

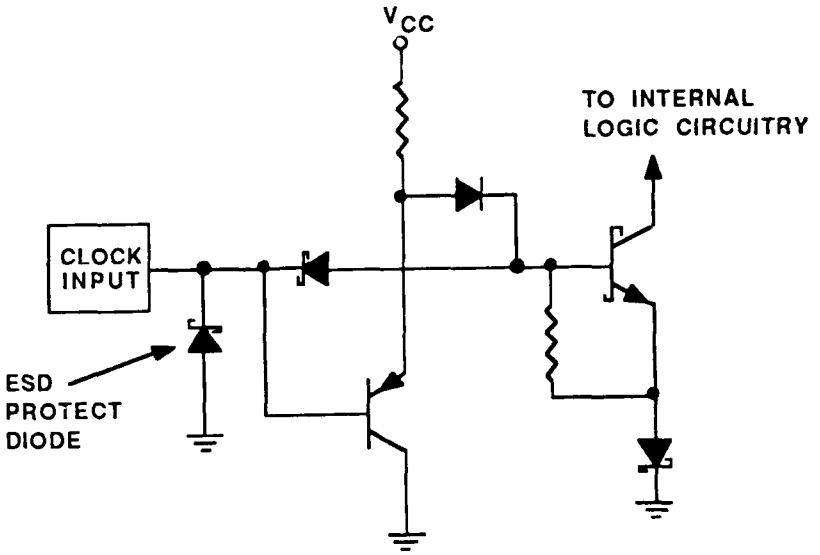


Figure 6.4.2.2 - SN54ALS74A Clock Input Schematic

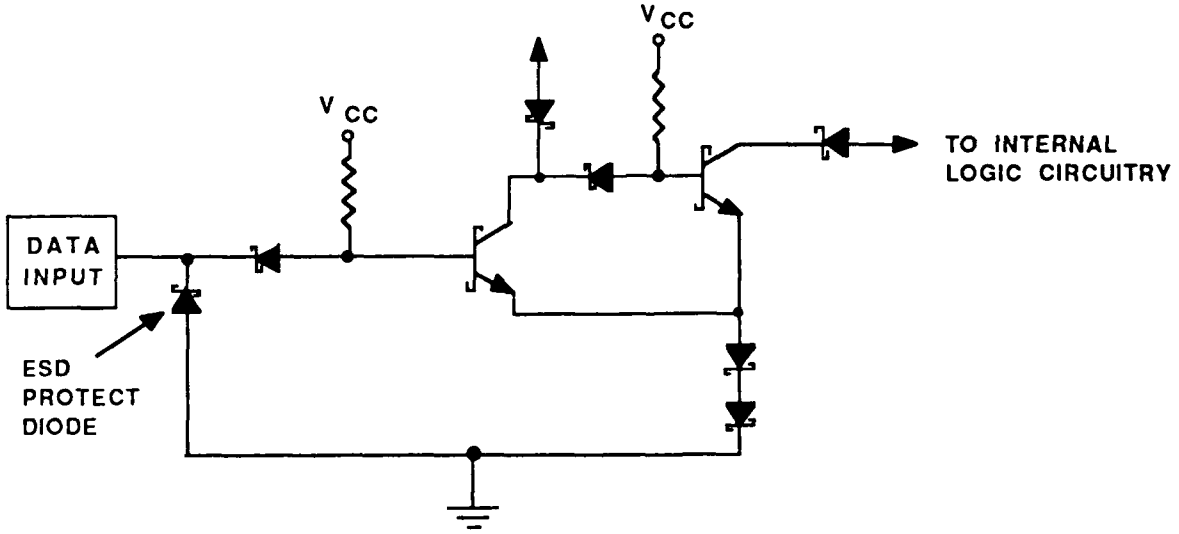


Figure 6.4.2.3 - SN54ALS74A Data Input Schematic

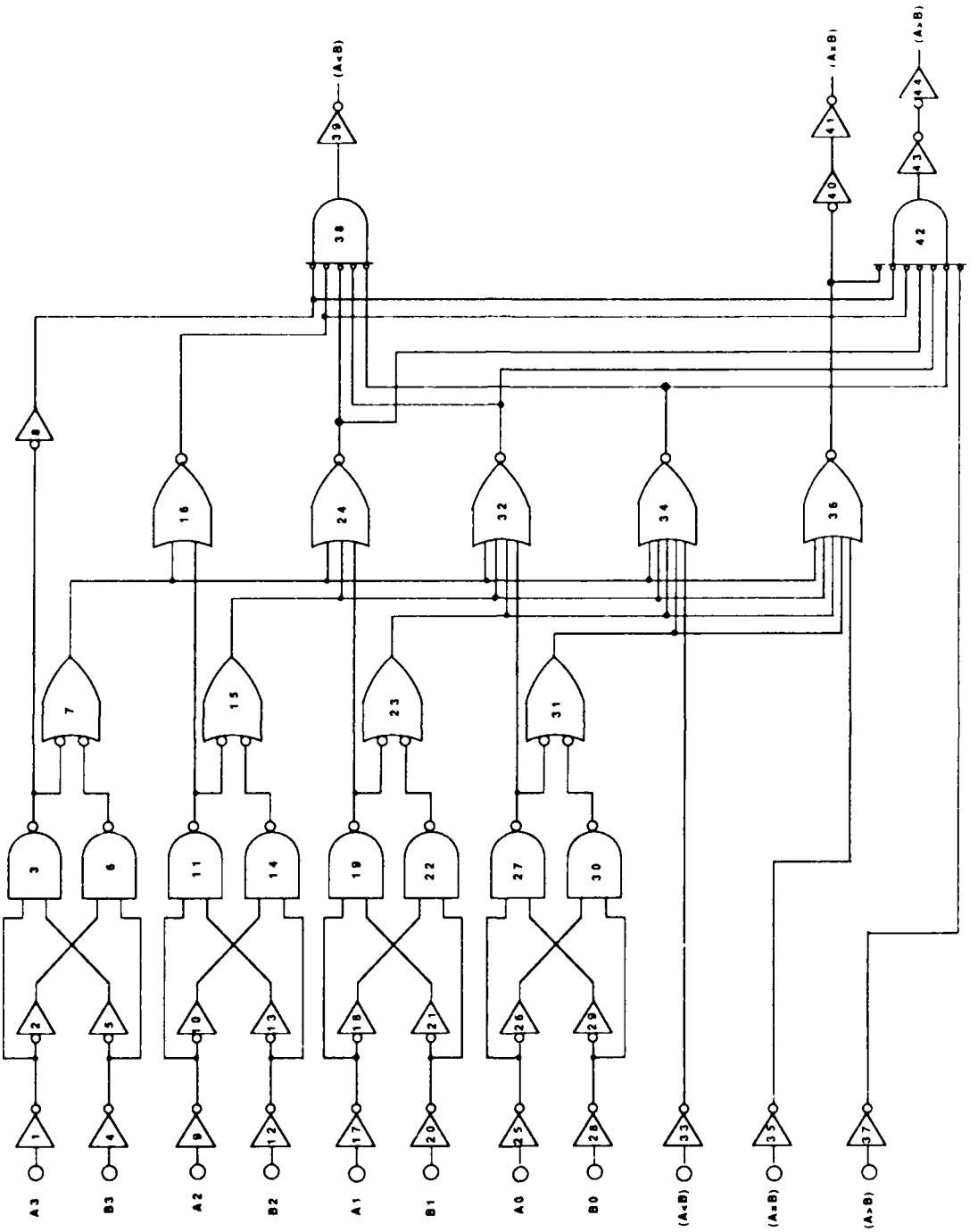


Figure 6.4.3.1 - CD4585B Logic Diagram
Note: Logic gates are numbered 1 through 44, inputs are on the left hand side, and outputs are on the right hand side.

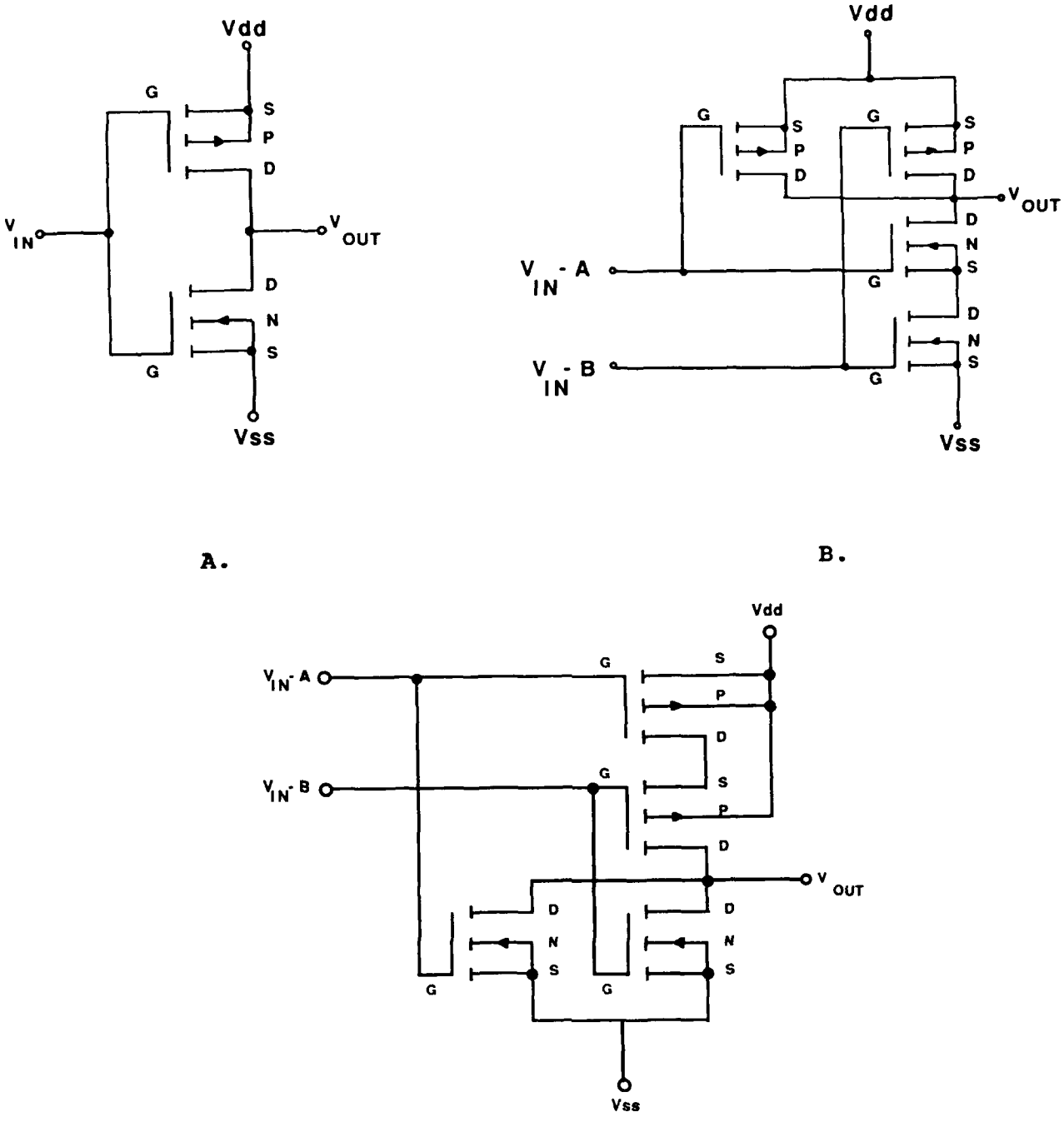


Figure 6.4.3.2 - CD4585B CMOS Logic Configuration,
A. Inverter
B. NAND Gate, Two Input
C. NOR Gate, Two Input

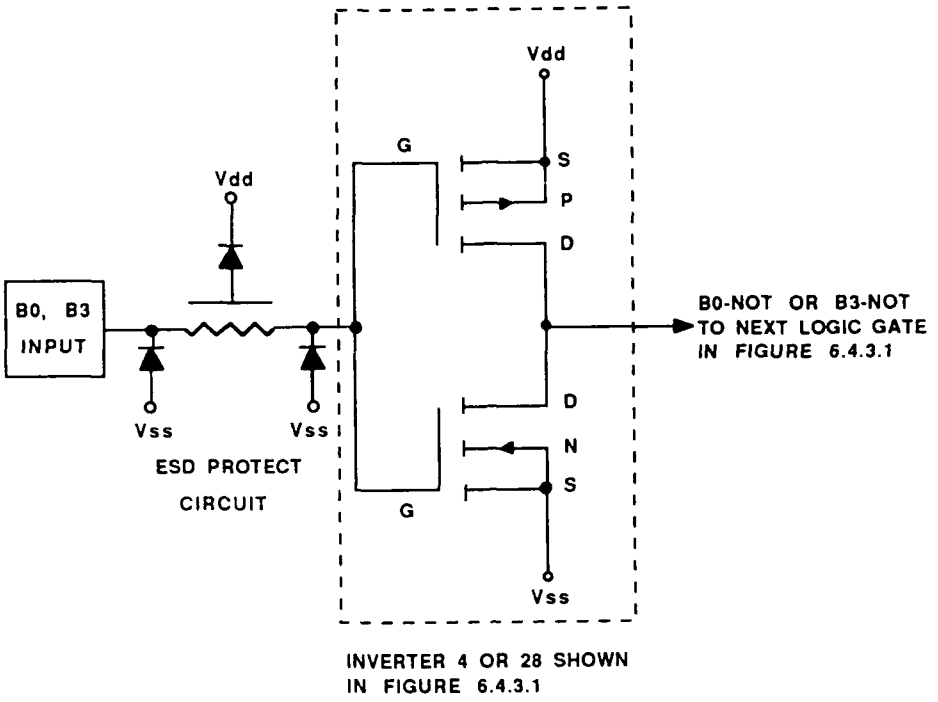


Figure 6.4.3.3 CD4585B Input Circuit Schematic
For B0 and B3 Inputs

6.4.4 SN54LS85

The overall photograph of the SN54LS85 with the pins and nodes labelled was shown in Figure 6.3.6. The logic diagram is shown in Figure 6.4.4.1. The schematics corresponding to the sections in the logic diagram are shown in Figures 6.4.4.2 through 6.4.4.4. Figure 6.4.4.2 is the schematic for the input NAND gate (A3, B3 inputs). Figure 6.4.4.3 is the schematic for the two AND gates and the NOR gate that follow the input NAND gate. Figure 6.4.4.4 is the schematic for the output section AND gates (A>B output).

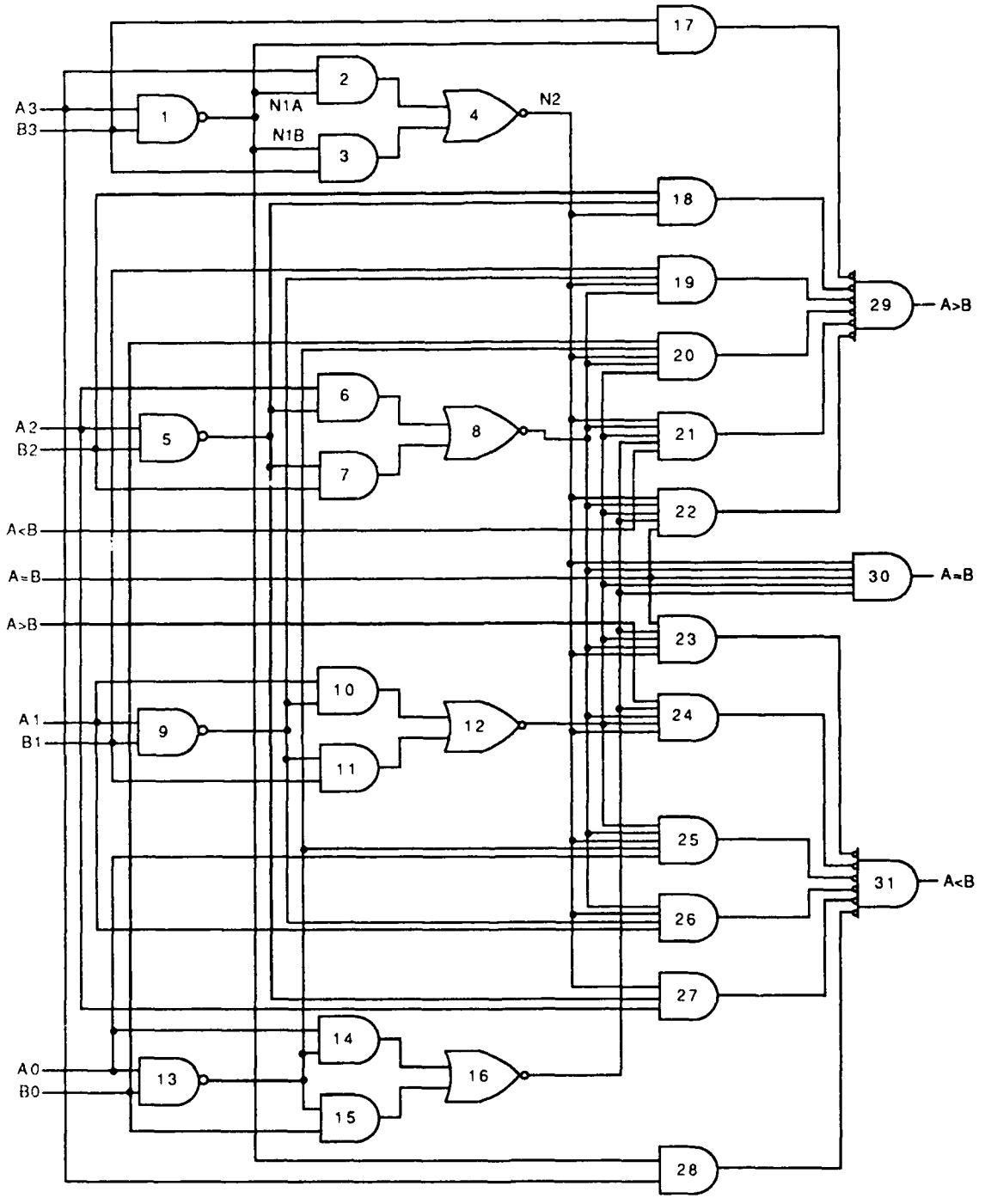


Figure 6.4.4.1 - SN54LS85 Logic Diagram
Note: Logic gates are numbered 1 through 31, inputs are on the left hand side, and outputs are on the right hand side. The labels N1A, N1B, and N2 identify locations in Figures 6.4.4.2 - 6.4.4.4.

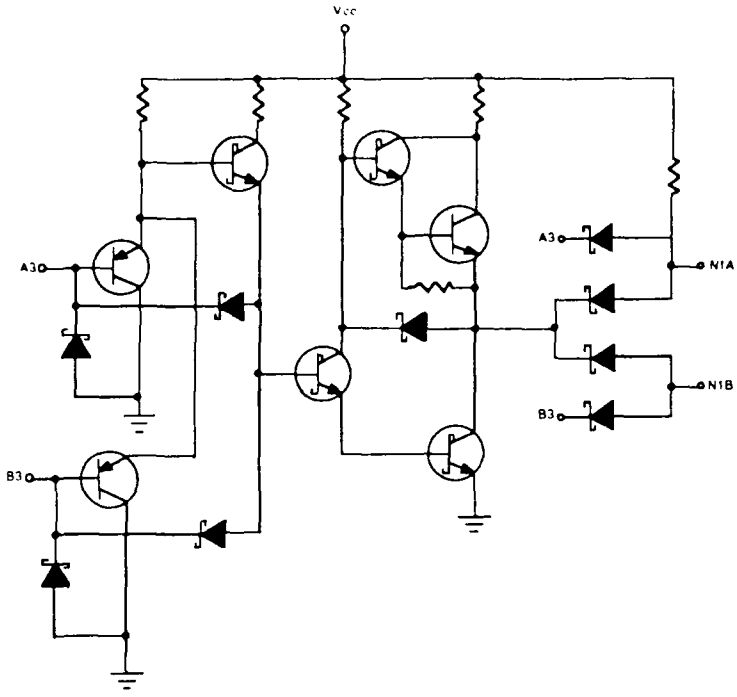


Figure 6.4.4.2 - SN54LS85 Input Section Schematic
Note: Reference Figure 6.4.4.1
for labelling scheme.

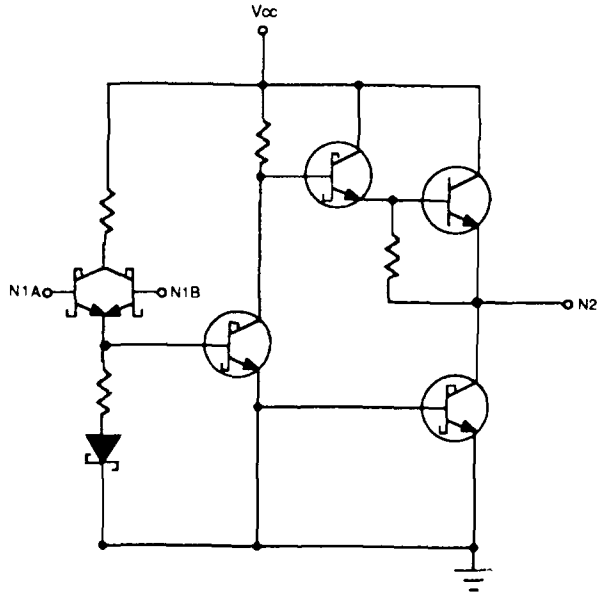


Figure 6.4.4.3 - SN54LS85 Center Section Schematic
Note: Reference Figure 6.4.4.1
for labelling scheme.

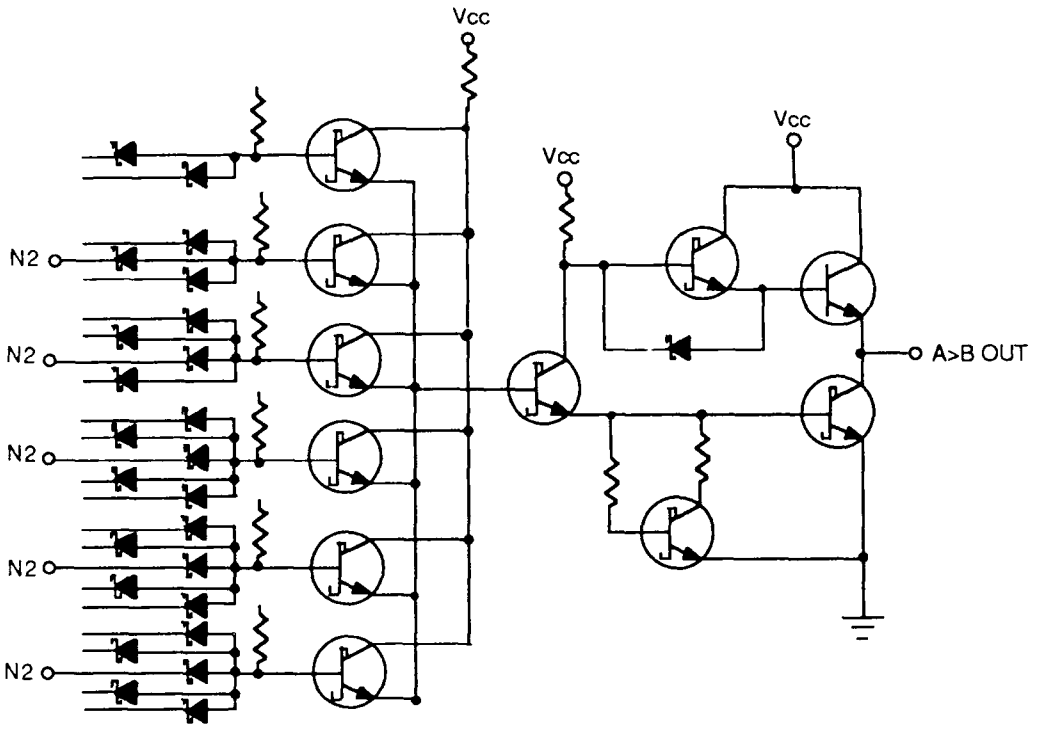


Figure 6.4.4.4 - SN54LS85 Output Section Schematic
Note: Reference Figure 6.4.4.1
for labelling scheme.

6.5 Device Preparation

The following procedure was performed to prepare parts for the SEM measurements.

An initial detailed electrical parametric test was performed on five each of the CD4013B and the SN54ALS74A IC's using a GenRad 1732 automated test system and on five each of the CD4585B and the SN54LS85 IC's using the Tektronix 3260 automated test system. RF upset susceptibility threshold testing was performed at RF frequencies of 1.2, 10, and 50 MHz.

The lids on two of each of the part types were then removed by polishing the tops on a diamond wheel until they were very thin and then removing the remaining ceramic with an Xacto knife or pin. The die surface passivation was removed with hydrofluoric acid (HF) fumes or with a plasma stripper using CF_4 gas.

The CD4013B and CD4585B are passivated with silicon dioxide (SiO_2) and were stripped using HF fumes. Approximately forty-five seconds were required to remove the passivation. The parts were then rinsed for one minute in deionized water, one minute in isopropyl alcohol, and blown dry using nitrogen gas.

The SN54ALS74A and the SN54LS85 are passivated with silicon nitride (Si_3N_4) and were stripped using the plasma stripper. The gold headers had to be coated with photoresist prior to the etching process to prevent gold redeposition on the die surfaces. Approximately twenty minutes were required to remove the passivation. The photoresist was removed using a one minute acetone rinse followed by a one minute rinse in deionized water and then blown dry using nitrogen gas. A five minute, 300°C bake was then performed to eliminate current leakage due to surface charge induced by the plasma stripping process.

The entire die surface area on all part types was exposed to an electron beam for thirty minutes at 5 kiloelectron-volts (keV). The beam current was 2×10^{-9} amps and the working distance was 39 millimeters. The purpose of this test was to simulate exposure that will occur during the SEM QVC measurements.

The RF upset threshold susceptibility testing and the detailed electrical parametric testing were repeated after deprocessing. No significant deviation from the initial measurements was noted and the devices were ready for SEM QVC testing.

7.0 INSTRUMENTATION AND TEST FIXTURE

This section describes the instrumentation and test fixturing that were used to test the selected integrated circuits for upset level.

7.1 Test Fixture

The test fixture was designed and built to allow the device under test (DUT) to be tested in the SEM chamber. Figure 7.1.1 shows a sketch of the DUT fixture and Figure 7.1.2 is a photograph of the test fixture. Shop drawings are provided in Figures 7.1.3 - 7.1.7. The DUT fixture consists of two printed circuit boards, one oriented horizontaly the other vertically. Each board has eight SMB connectors through which the input signals are applied to the 16-pin zero insertion force socket. The circuit boards are made of PTFE material with copper clad on both sides. Isolation between signal lines is provided by a ground plane between the traces. Each of the signal lines was designed to be of equal length to eliminate timing problems due to variation in the propagation delay of signals applied to different pins. The two boards are attached to the mounting frame, which in turn is attached to the SEM stage.

Figure 7.1.8 shows a sketch of one of the two digital signal interface connector and cable assemblies, which connects one of the two 40-pin dual inline vacuum feedthrough connectors to the SMB connectors on the DUT fixture. Shop drawings are provided in Figures 7.1.9 - 7.1.11. A 35 ohm series resistor is built into the interface connector for each line to reduce ringing. The signals are applied to every other pin of the dual inline connector while the remaining pins are grounded to reduce signal coupling. Another coaxial cable connects the DUT card to an SMA vacuum feedthrough connector to which the RF signal is applied.

The capacitance of the dual inline feedthrough connector and cable assembly was measured to be approximately 20 picofarads (pF). The capacitance of the DUT fixture input was measured to be approximately 30 pF.

To measure the isolation between adjacent inputs, a digital 1 megahertz (MHz) signal was applied to an input and the coupled signal was measured on an adjacent input. Next, a 1 MHz and a 500 kilohertz (kHz) signal were applied to two inputs and the coupled signal was measured on the input pin between them. In both cases the isolation was 26 decibels (dB) or better.

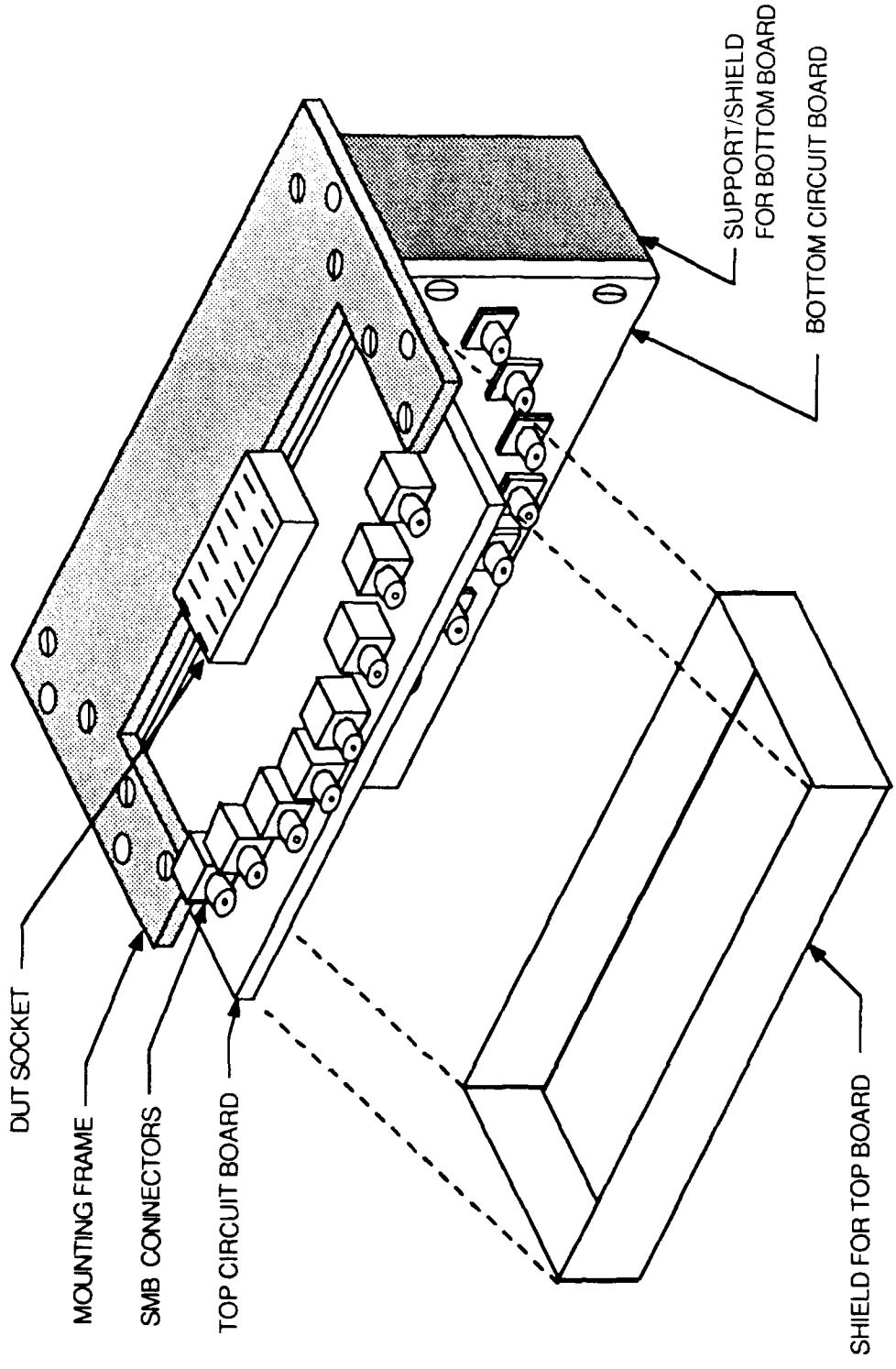


Figure 7.1.1 - Sketch of DUT Fixture

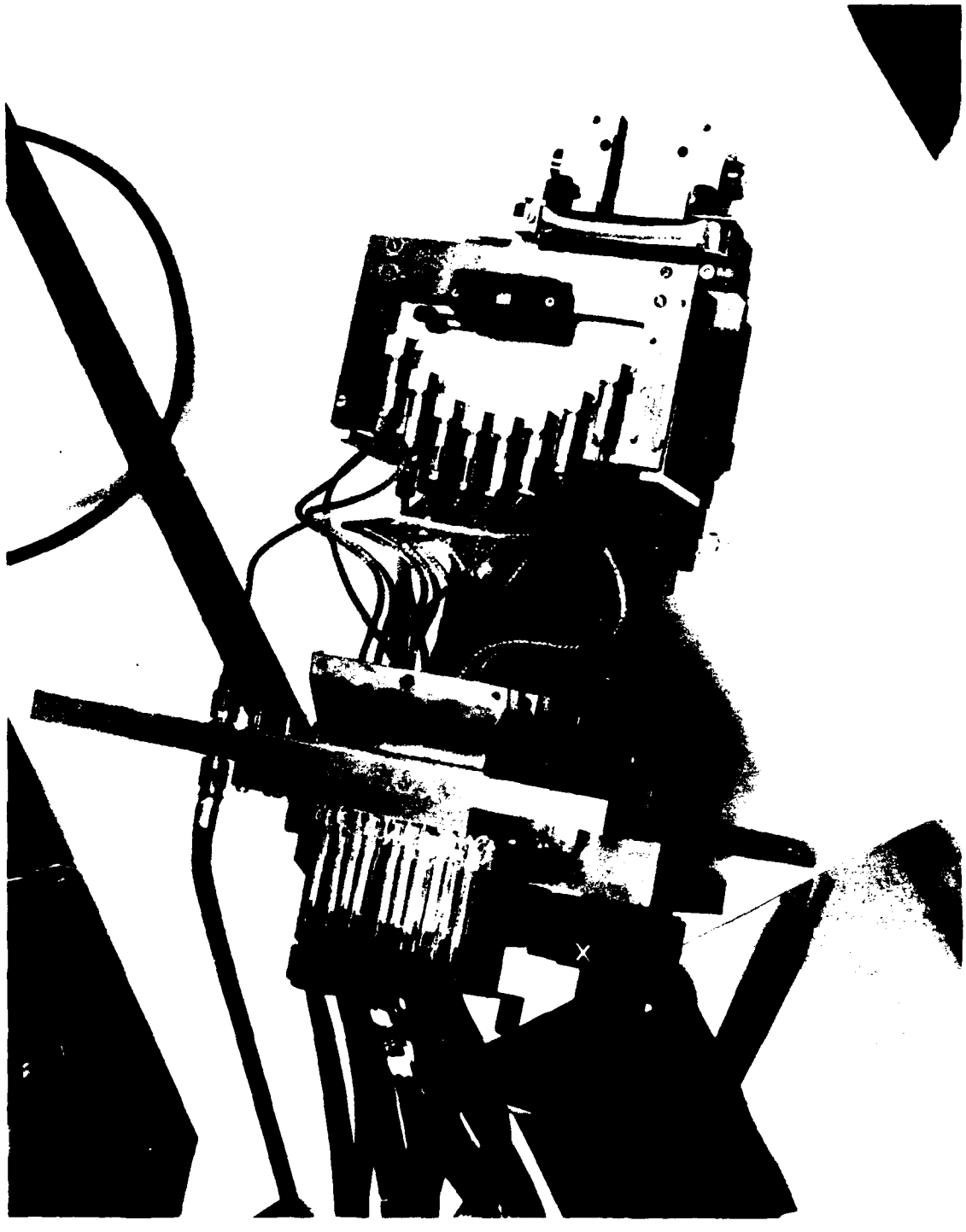


Figure 7.1.2 - Photograph of DUT Fixture

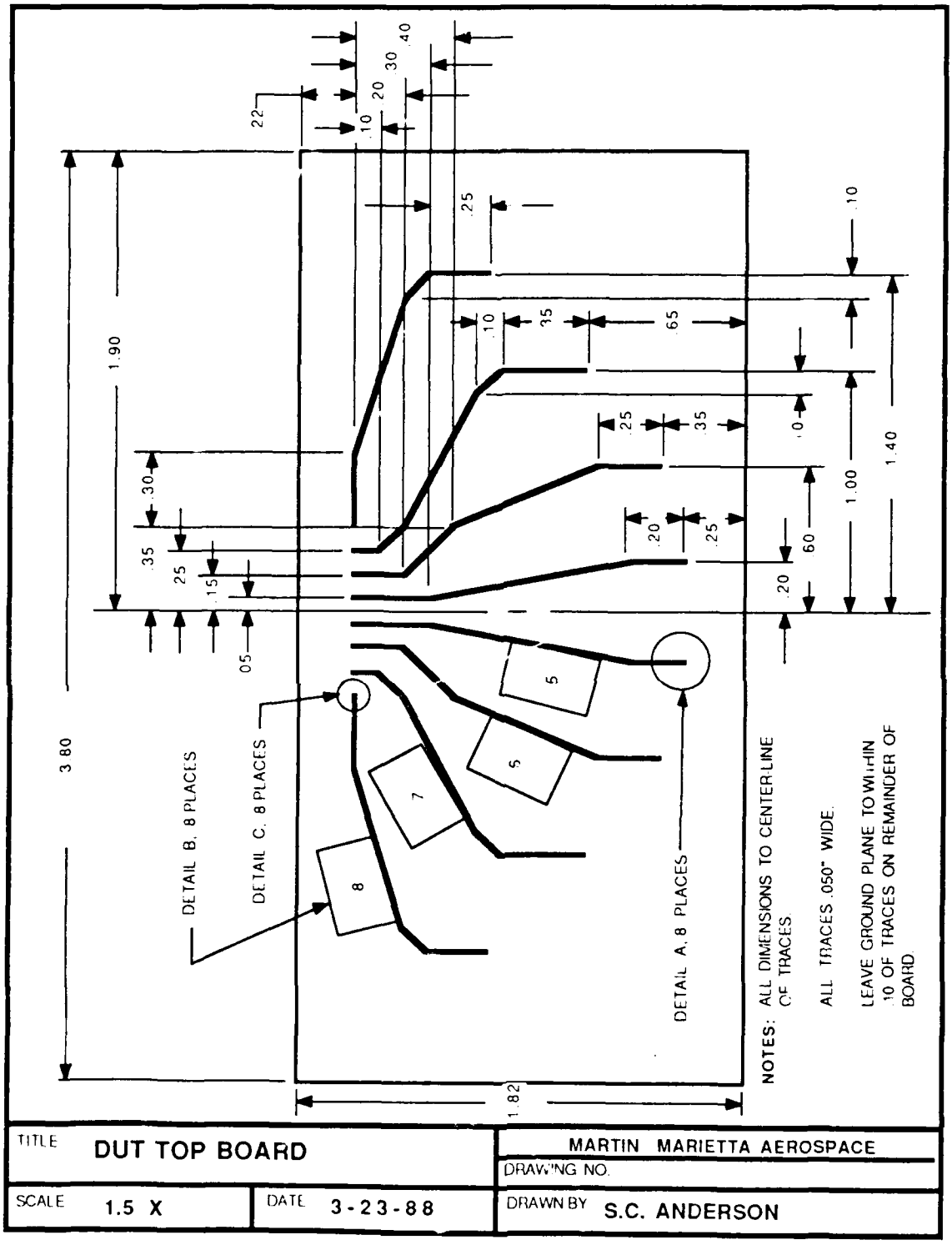


Figure 7.1.3 - Test Fixture Top Board Shop Drawing

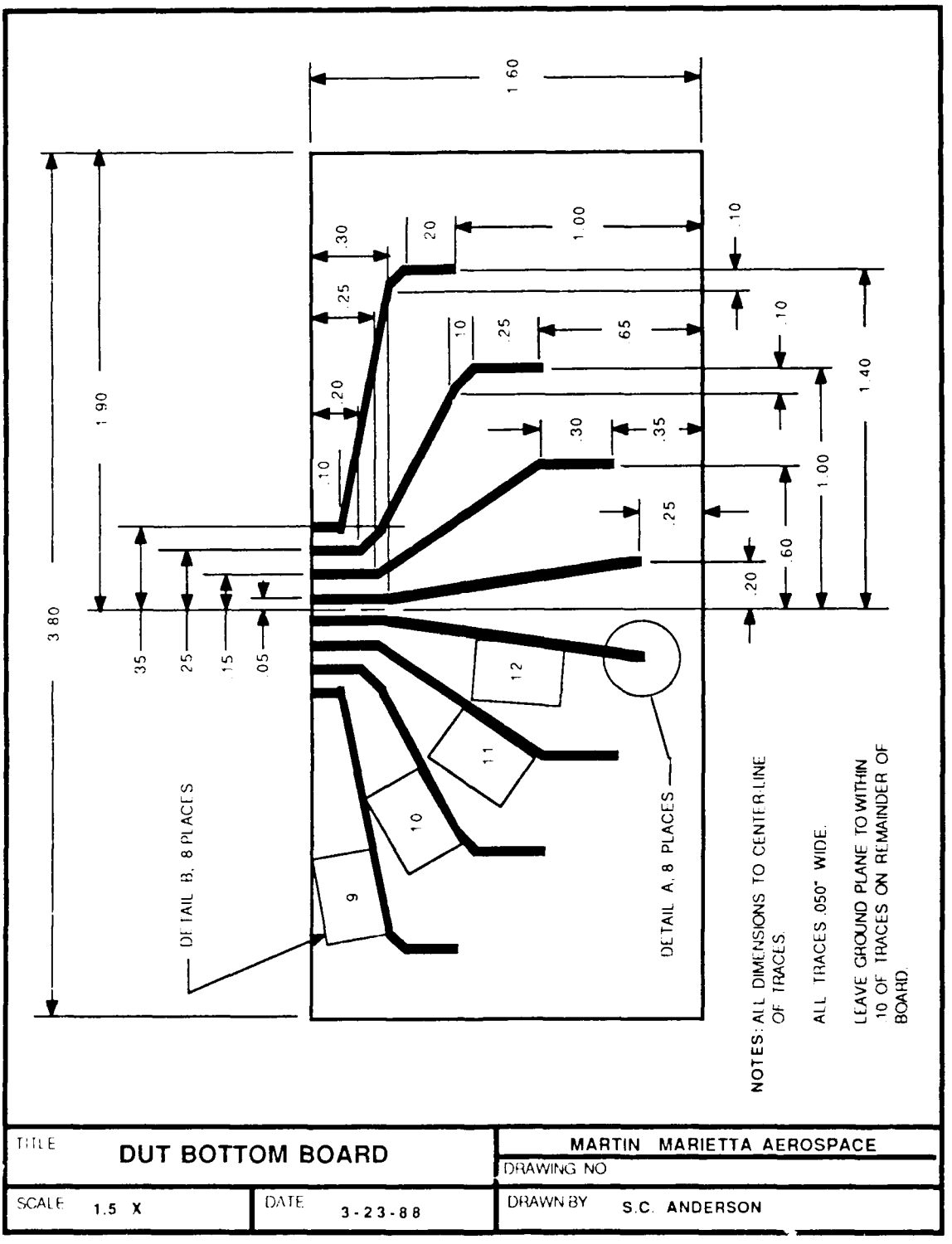


Figure 7.1.4 - Test Fixture Bottom Board Shop Drawing

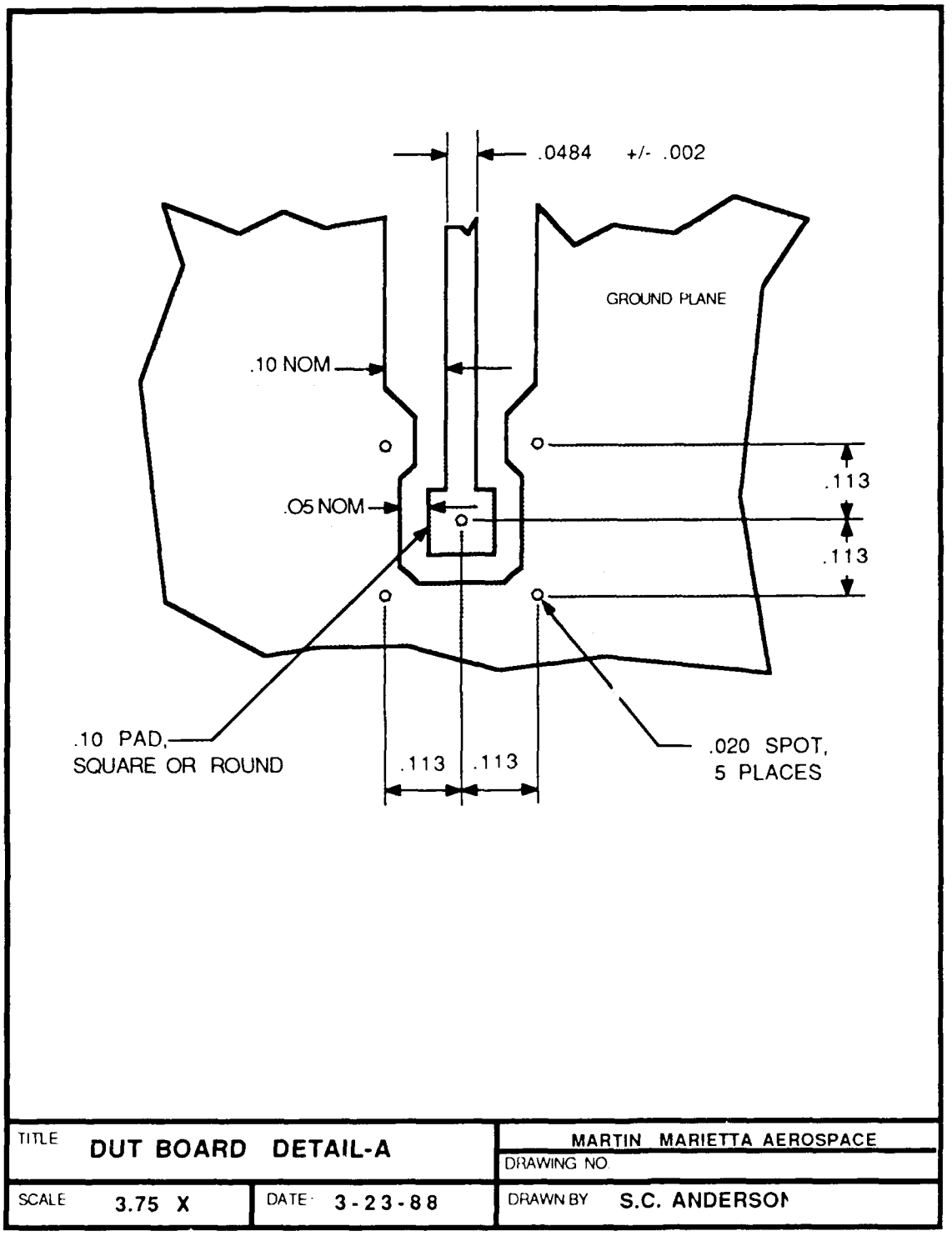


Figure 7.1.5 - Test Fixture Shop Drawing Showing Detail A (Ref. Figure 7.1.3 and 7.1.4)

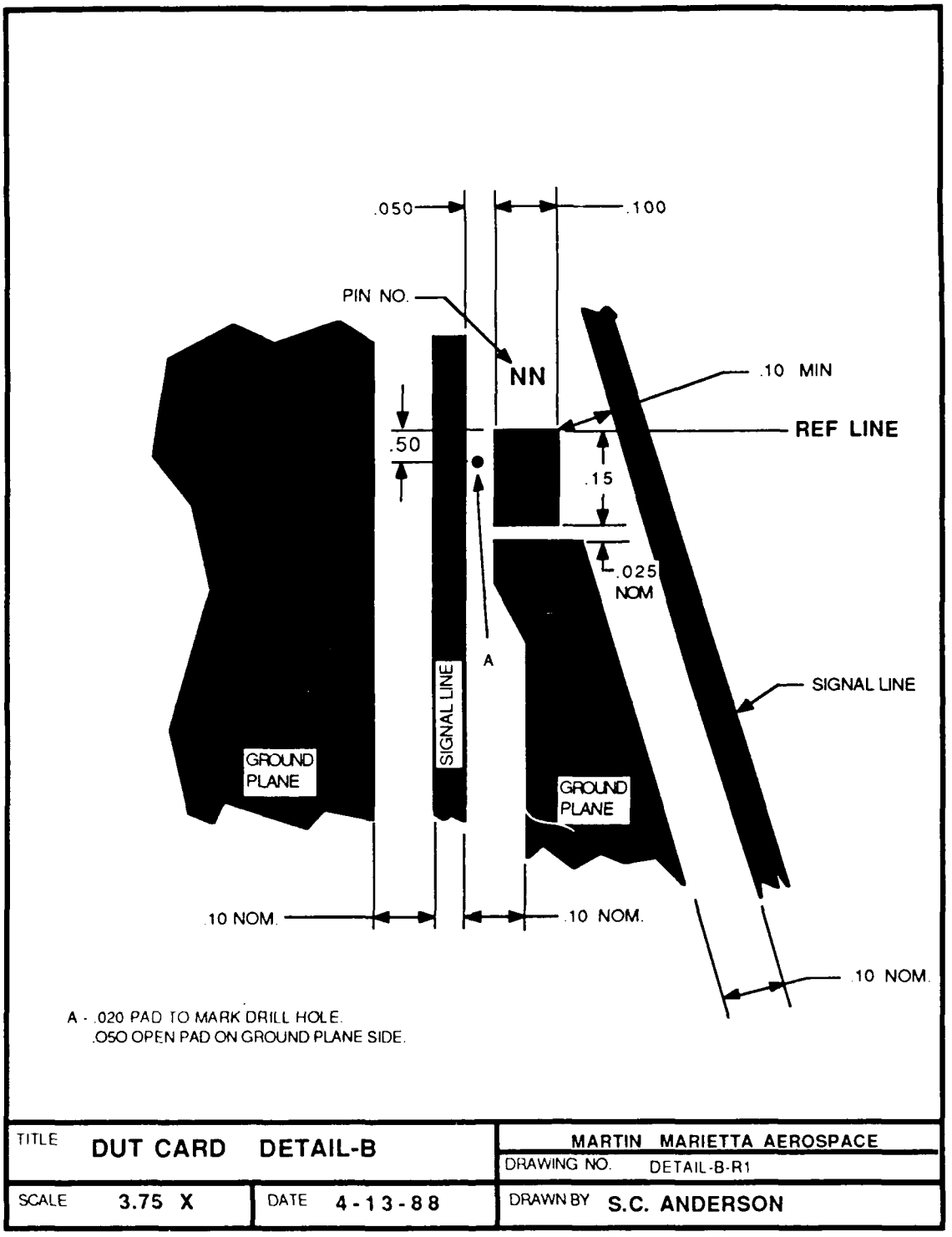


Figure 7.1.6 - Test Fixture Shop Drawing Showing Detail B (Ref. Figure 7.1.3 and 7.1.4)

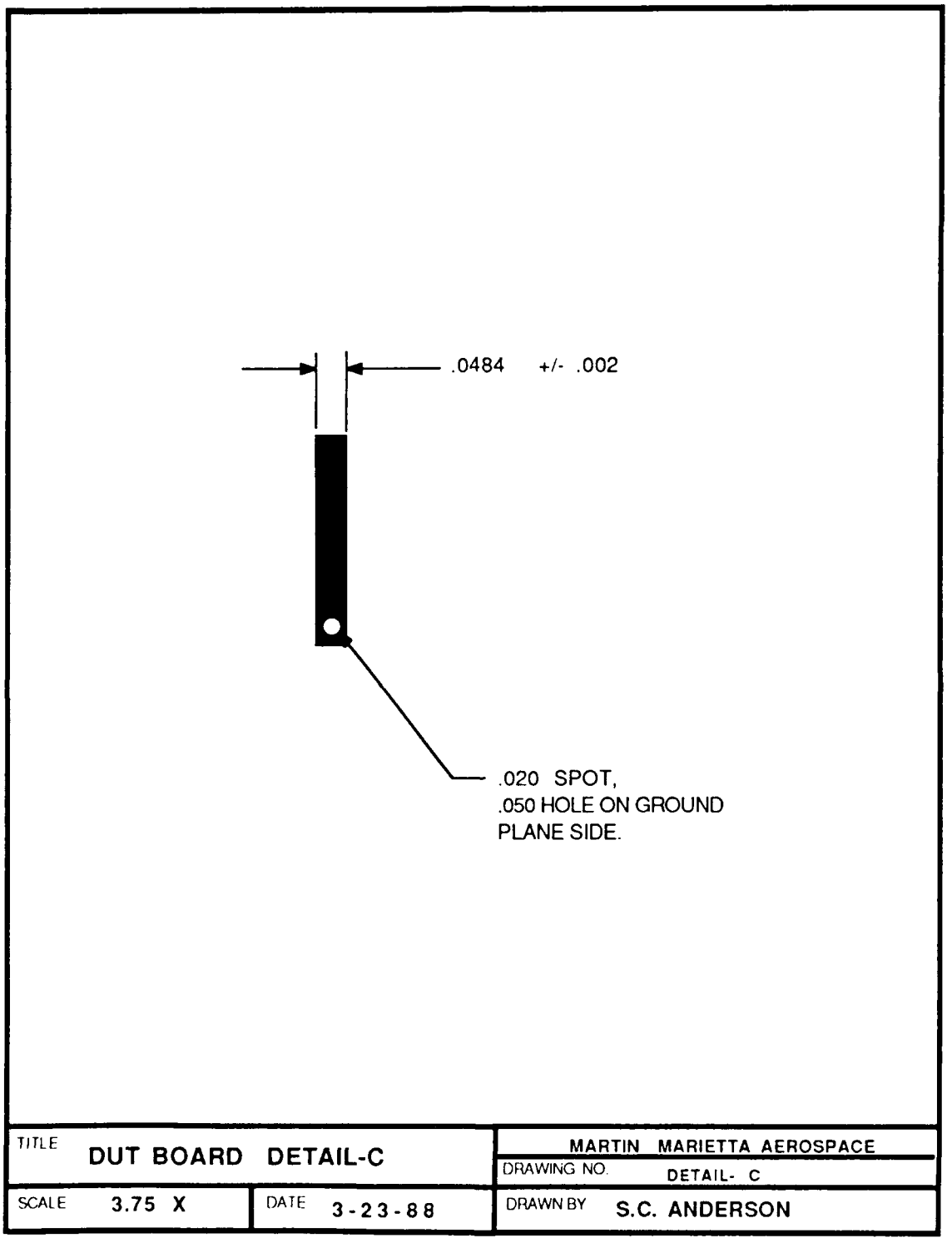


Figure 7.1.7 - Test Fixture Shop Drawing Showing Detail C (Ref. Figure 7.1.3)

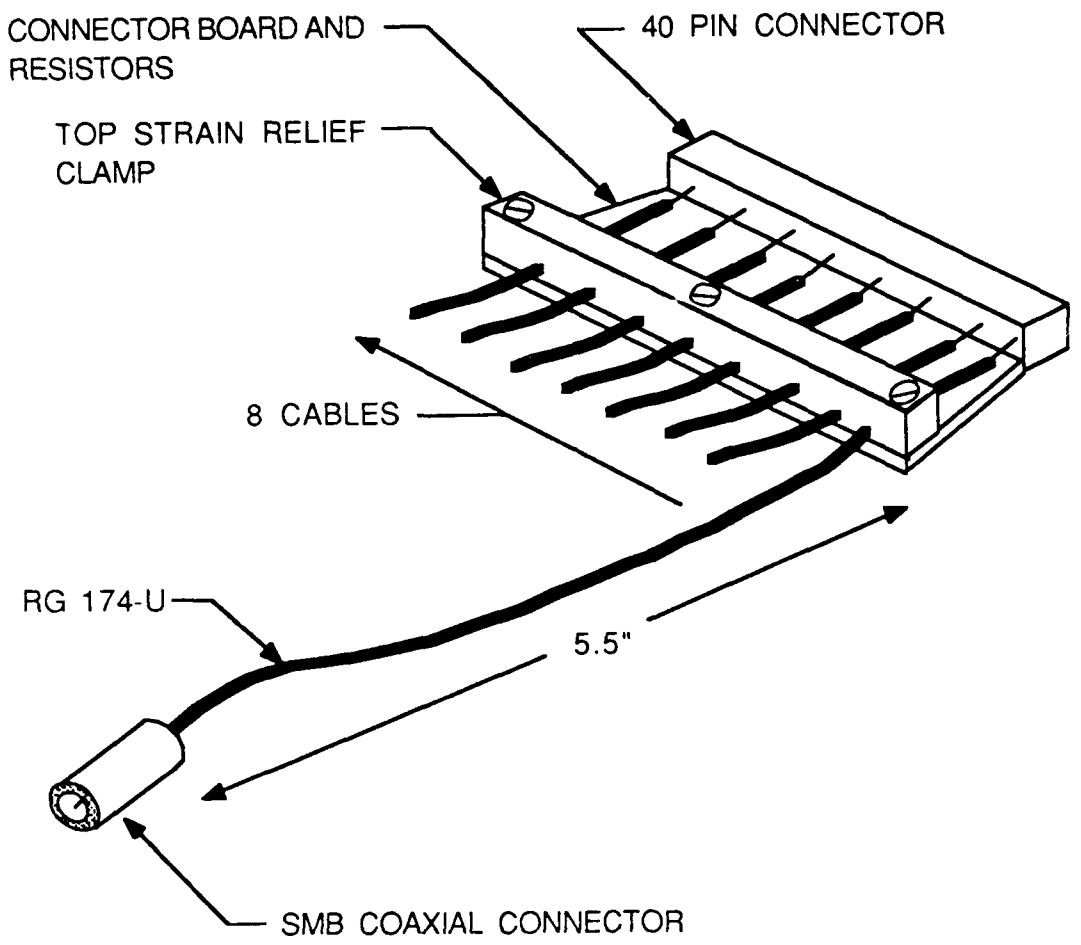
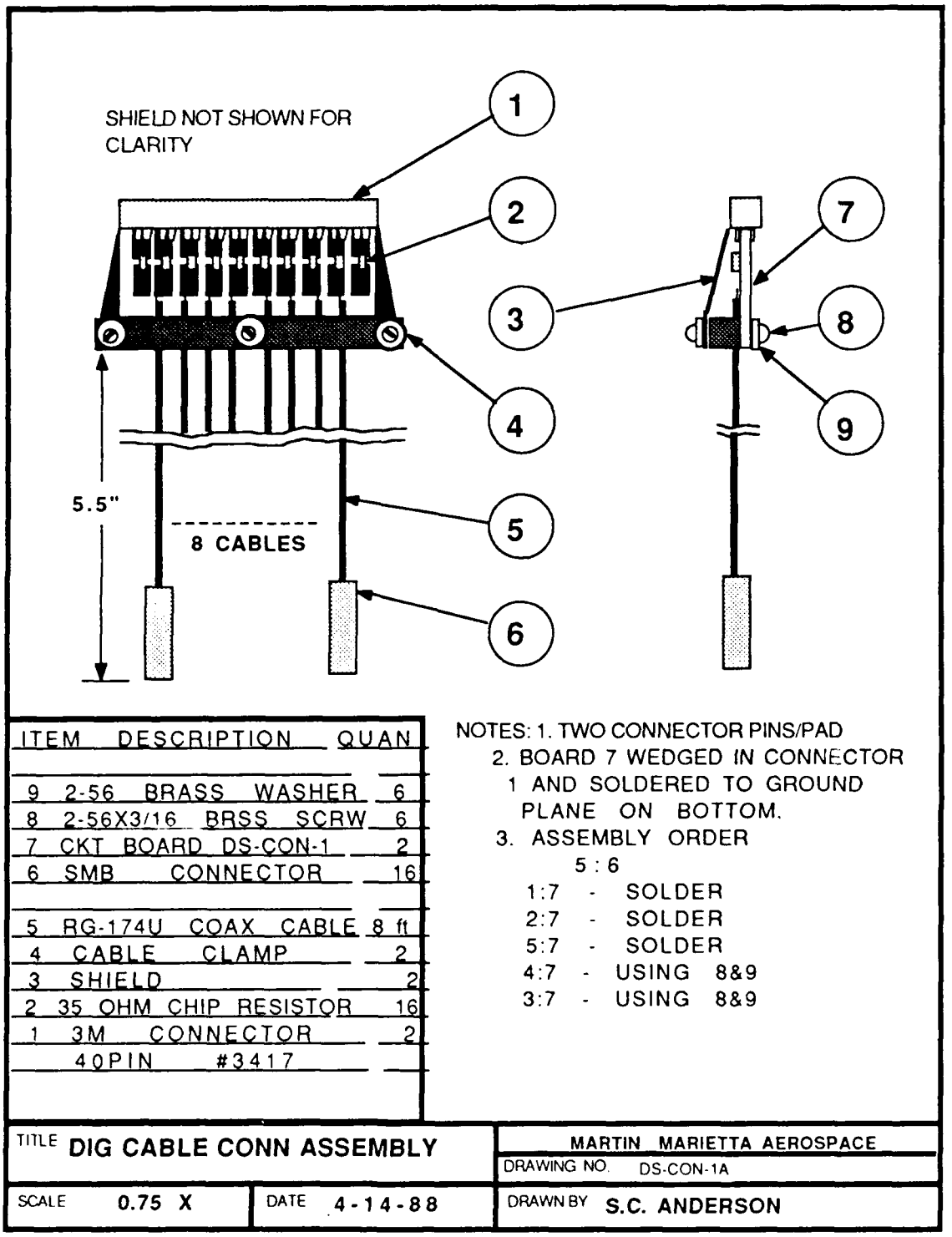


Figure 7.1.8 - Sketch of Digital Signal Interface Connector and Cable Assembly



ITEM	DESCRIPTION	QUAN
9	2-56 BRASS WASHER	6
8	2-56X3/16 BRSS SCRW	6
7	CKT BOARD DS-CON-1	2
6	SMB CONNECTOR	16
5	RG-174U COAX CABLE	8 ft
4	CABLE CLAMP	2
3	SHIELD	2
2	35 OHM CHIP RESISTOR	16
1	3M CONNECTOR 40PIN #3417	2

NOTES: 1. TWO CONNECTOR PINS/PAD
2. BOARD 7 WEDGED IN CONNECTOR 1 AND SOLDERED TO GROUND PLANE ON BOTTOM.
3. ASSEMBLY ORDER
5 : 6
1:7 - SOLDER
2:7 - SOLDER
5:7 - SOLDER
4:7 - USING 8&9
3:7 - USING 8&9

TITLE DIG CABLE CONN ASSEMBLY		MARTIN MARIETTA AEROSPACE DRAWING NO. DS-CON-1A
SCALE 0.75 X	DATE 4-14-88	DRAWN BY S.C. ANDERSON

Figure 7.1.9 - Connector and Cable Assembly Shop Drawing

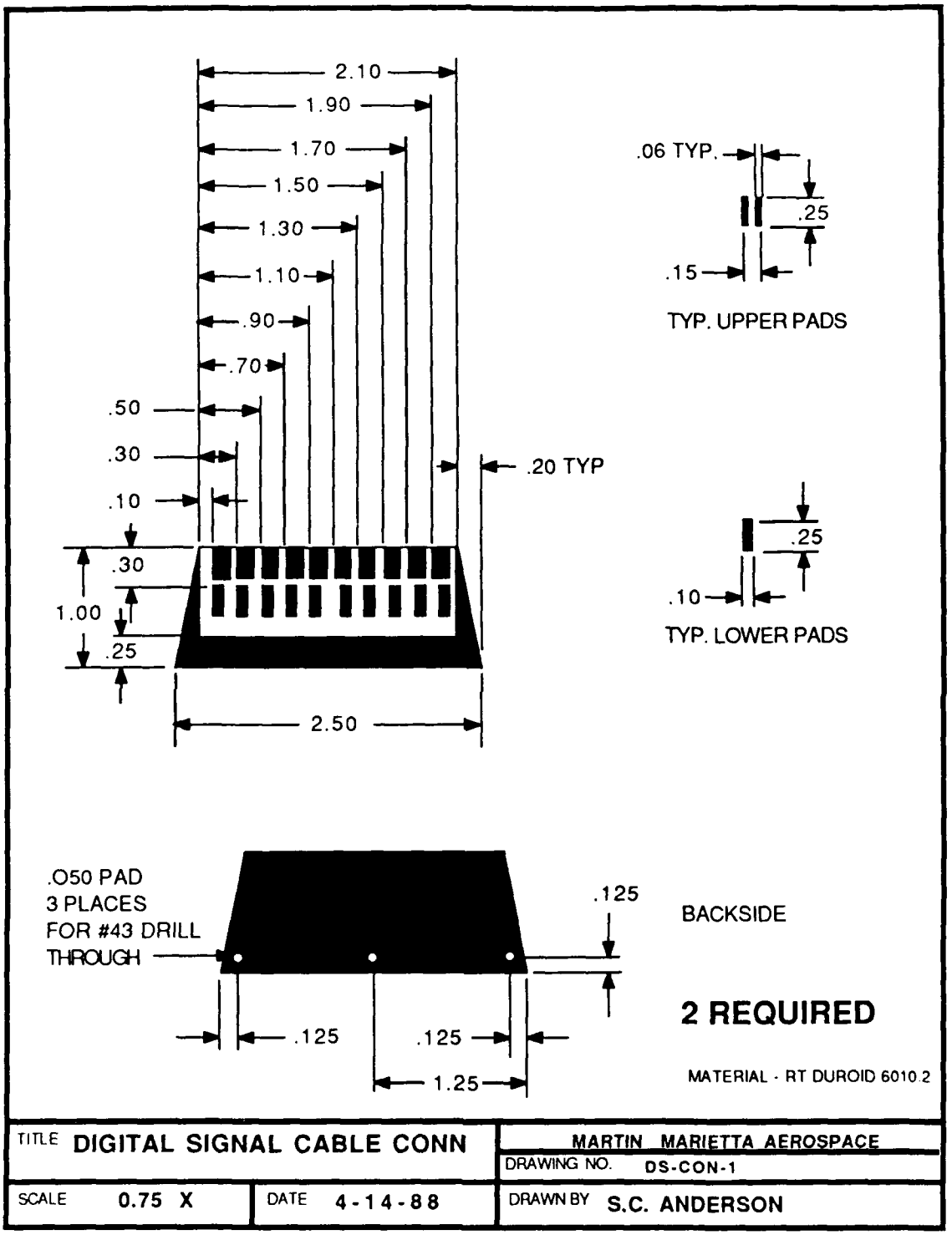


Figure 7.1.10 - Cable Connector Shop Drawing

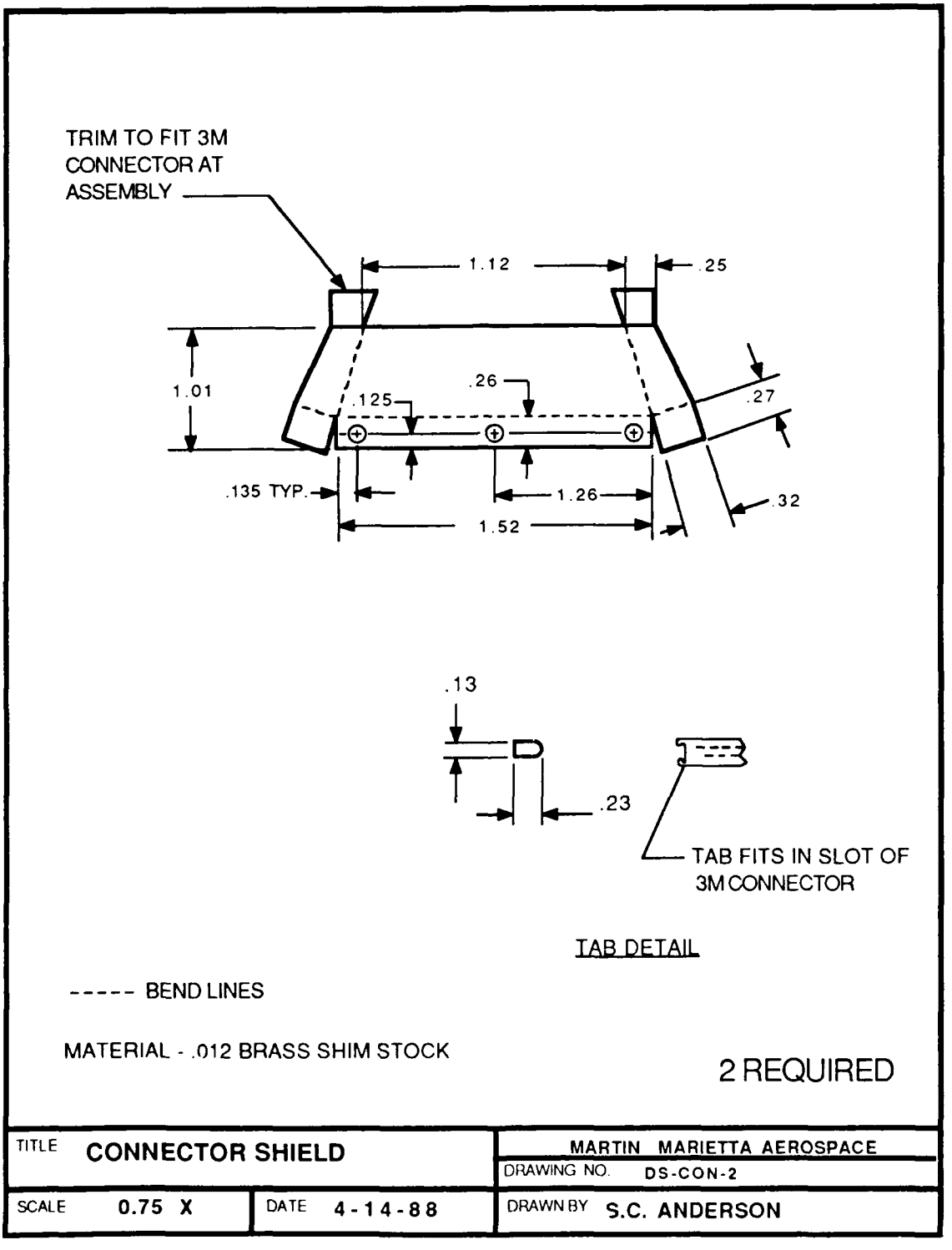


Figure 7.1.11 - Connector Shield Shop Drawing

The SEM interface was also characterized with an RF input. A sinusoidal signal ranging in frequency from 1 to 200 MHz was applied to pin 8 of the DUT board through an SMA connector on the front of the vacuum panel and coupling was measured on pins 7 and 9 of the DUT socket. For most of the frequency range, isolation was in excess of 40 dB. At 60 MHz there seems to be a resonance, and isolation between pins 8 and 7 drops to 14.2 dB. Figure 7.1.12 shows the SEM interface isolation characteristics.

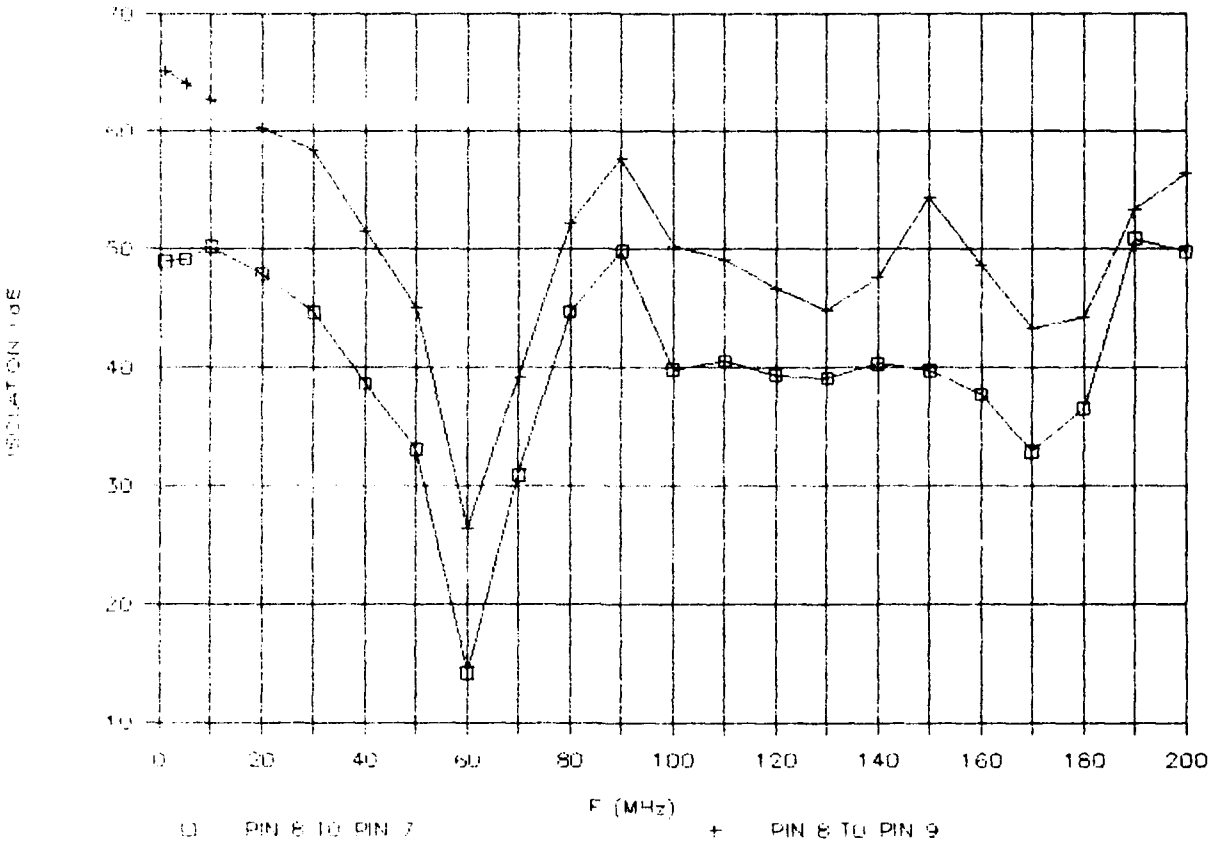


Figure 7.1.12 - Characterization of SEM Interface With Sinusoidal Signal Applied to Pin 8 and Coupling Measured on Pins 7 and 9

7.2 Data Acquisition System

A Tektronix DAS9200 system was used to supply the test vectors to the DUT and to acquire the outputs of the DUT. The DAS9200 is based on a Motorola 68010 microprocessor and it is equipped with 2 megabytes of random access memory , a 20 megabyte hard-disk drive, 400 kilobyte floppy-disk drive, high resolution color monitor, color printer, three RS-232C ports and 8 module slots. To generate and acquire signals, there are three modules.

The 92A16 module can acquire 16 channels of data at rates of up to 200 MHz and memory depth of 4000 per channel. It uses two P6461 8-channel probes to acquire data with either an internal or external clock. For each channel, P6461 probes provide individual flex cables with a hybrid circuit at the end which acquires the reference and signal inputs from the DUT.

The 92S16 module is capable of 16-channel algorithmic pattern generation with 1000 memory depth plus 2 strobe/data channels. Two P6464 pattern generation probes deliver the output pattern to the DUT. Each P6464 probe provides 8 channels of data output plus strobe and clock channels. For each channel there is an individual flex cable with a hybrid circuit channel driver at the end.

The 92S32 module is capable of 32-channel stored pattern generation with 8000 memory depth plus 4 strobe/data channels. This module is controlled by the 92S16 module, together they provide a capability for 48-channels of pattern generation. The DAS9200 is set for a TTL threshold level of 1.4 volts, signals below this level are interpreted as low and signals above this level are interpreted as high. Signals are sampled and stored on the rising edge of the DAS clock.

7.3 RF Signals

The RF interference signal was generated using a Hewlett-Packard 8656A signal generator which is capable of generating signals from 0.1 to 990 MHz. The signal used, was a continuous wave (CW) sinusoid ranging in frequency from 1.2 to 200 MHz. The signal was conditioned using a 40 dB RF amplifier and a 0 to 12 dB variable attenuator. The Electronic Navigation model 603L 40 dB RF amplifier is rated at 3 watts (W) for a bandwidth of 0.8 to 1000 MHz. The Hewlett-Packard 355C VHF variable attenuator is rated at 0.5 W for a bandwidth of DC to 1000 MHz with a 50 ohm load.

7.4 Combiner

A method was required to add the RF interference signal to the digital signal. Several schemes were analyzed: 1) a Picosecond Pulse Labs model 5590 bias-tee, a Mini Circuits model ZFSC-2-4 splitter/combiner and a circuit using a Comlinear CLC103 op-amp. The following criteria were used to evaluate the three given combiners: power handling capability, distortion, insertion loss, coupling between inputs, and ability to drive various loads.

7.4.1 Picosecond Pulse Labs Bias-tee

A bias-tee has three ports, one high frequency input port (RF port), one low frequency input port (LF port), and one output port. The Picosecond Pulse Labs model 5590 bias-tee tested was rated at 25 W at DC. With additional inductors, the low frequency cutoff of the RF port is specified at 10 kHz and the insertion loss is specified at 0.5 dB.

A 1 to 300 MHz sine wave was applied to the RF port with a 50 ohm load on the output and a 1 megohm load on the LF port. Isolation was very poor for 5 MHz and below, however, isolation increased to 46 dB at higher frequency. The insertion loss was less then 3.3 dB, which is very good. (Figure 7.4.1.1.)

A 1 to 300 MHz sine wave was applied to the RF port with a 1 megohm load on the output and on the LF port. Isolation was very poor for 5 MHz and below, however, isolation increased to 51 dB at higher frequency. The insertion loss was between 35 and 57 dB for all frequencies tested, this is very poor. (Figure 7.4.1.2.)

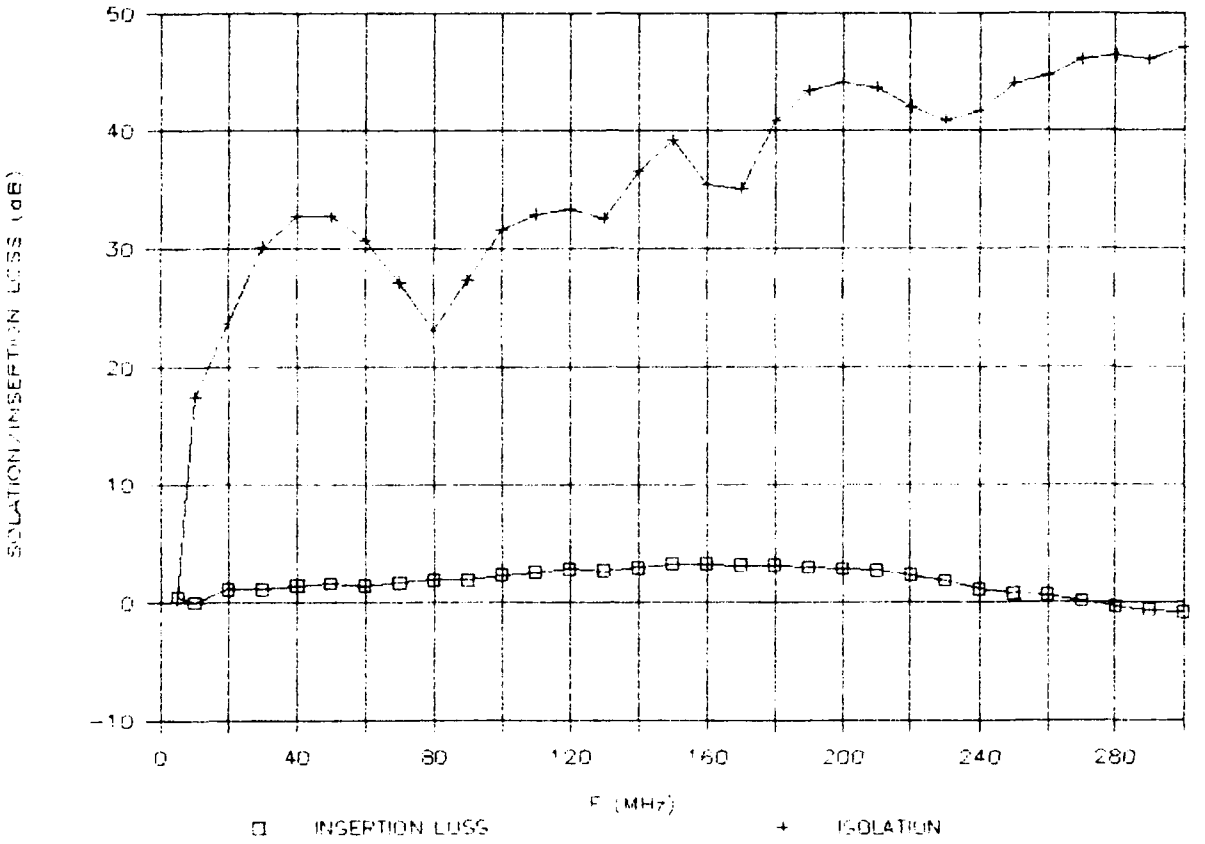


Figure 7.4.1.1 - Characterization of Bias-tee Isolation and Insertion Loss (50 ohm load)

A square wave between 1 and 200 kHz was applied to the LF port with the high frequency port and the output terminated with 50 ohm loads. The insertion loss and the isolation were measured to be between 2.9 and 5 dB for all frequencies tested, these values are good for the insertion loss but are very bad for the isolation.

The bias-tee is only usable for DC inputs on the LF port such as Vcc pin upset testing, and 5 MHz and above inputs on the RF port.

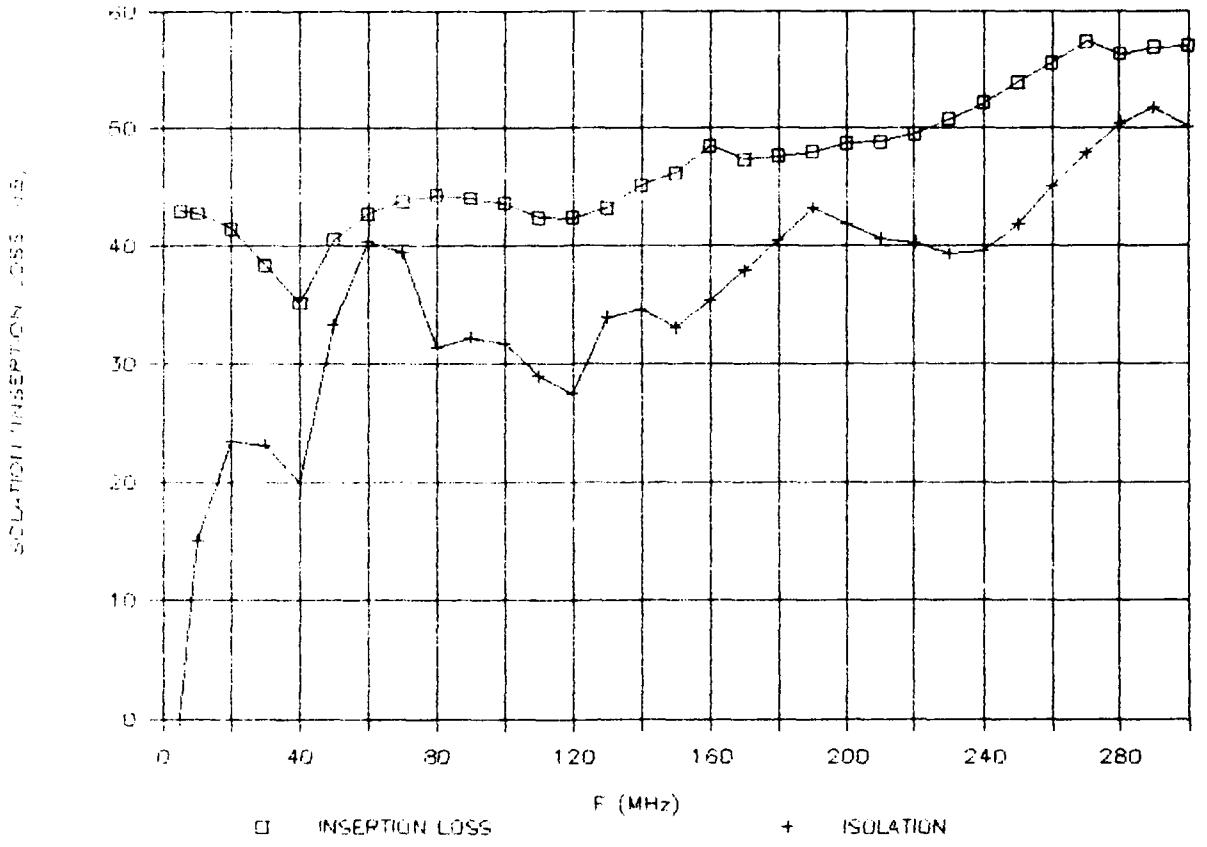


Figure 7.4.1.2 - Characterization of Bias-tee Isolation and Insertion Loss (1 megohm load)

7.4.2 Mini-Circuits Splitter/Combiner

The ZFSC-2-4 Mini-Circuits splitter/combiner is a three port network and can be used in two ways: 1) to split an incoming signal into two outputs and, 2) to combine two incoming signals into one output. This device is rated at 1 W, with 23 dB isolation and 0.5 dB insertion loss for a frequency range of 200 kHz to 1 GHz. For this project, only the combiner configuration was evaluated.

A 1 to 300 MHz signal was applied to input 1 with 50 ohm loads on input 2 and the output. Next, a signal was applied to input 2 with 50 ohm loads on input 1 and the output. In both cases, the insertion loss was measured to be between 2.8 and 6.5 dB and the input isolation was measured to be between 25.1 and 41.6 dB. Both inputs behaved the same (Figure 7.4.2.1).

A 1 to 300 MHz signal was applied to input 1 with 1 megohm loads on input 2 and the output. The input isolation was measured to be between 42.6 and 91 dB (power) which is very good, while the insertion loss was measured to be between 39.5 and 47.8 dB (power) which is very poor, see Figure 7.4.2.2. Due to impedance mismatch it is necessary to calculate the isolation and the insertion loss in terms of power.

A 1 to 300 MHz signal was applied to input 2 with a 50 ohm load on input 1 and a 1 megohm load on the output. The input isolation was measured to be between 3.3 and 28.7 dB and the insertion loss was measured to be between 36.6 and 47.4 dB (power), very poor for both of these parameters.

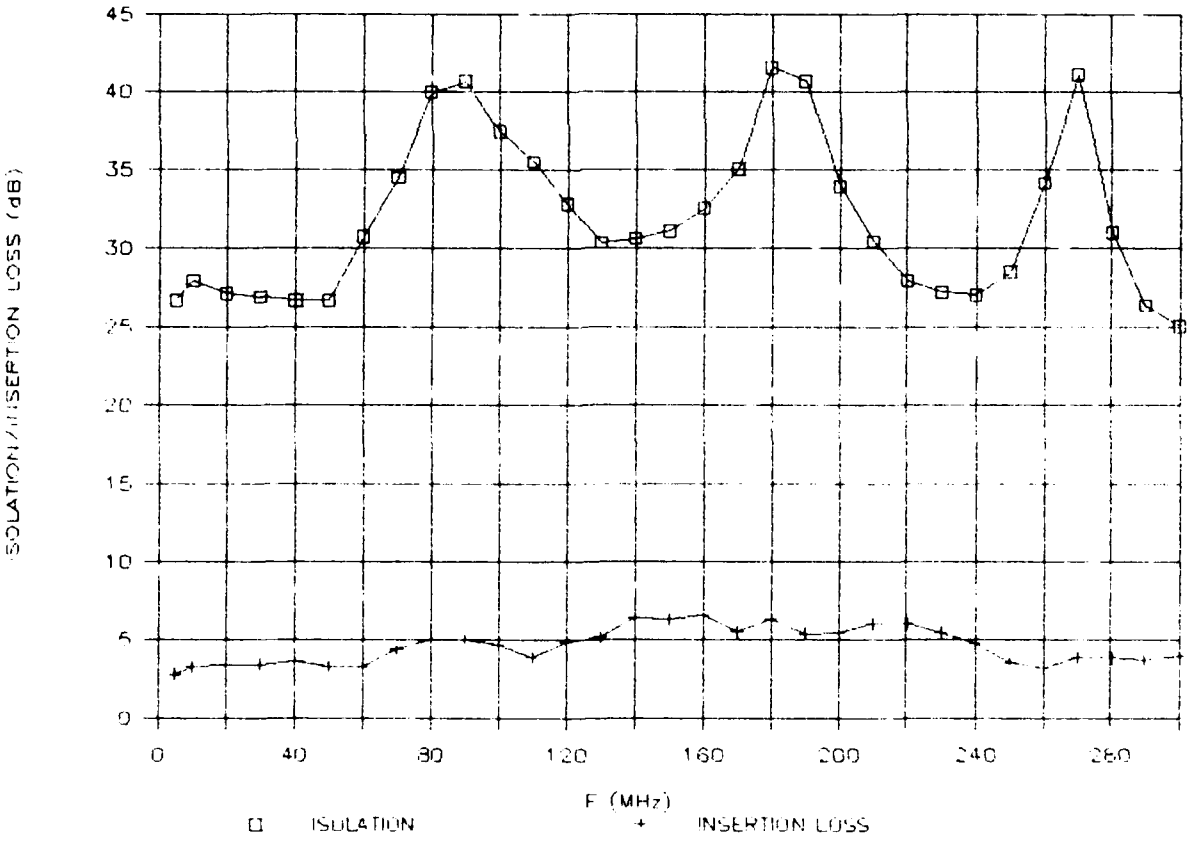


Figure 7.4.2.1 - Characterization of Splitter/Combiner for Isolation and Insertion Loss (50 ohm loads)

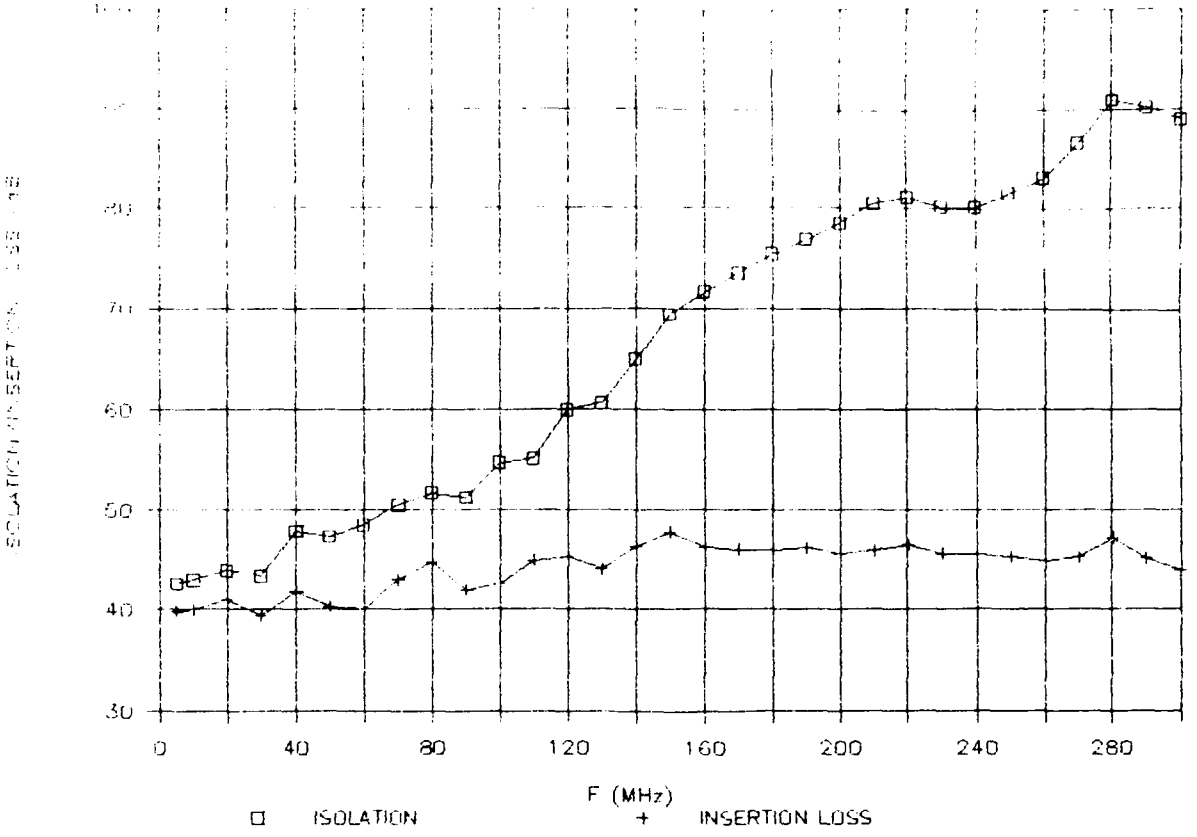


Figure 7.4.2.2 - Characterization of Splitter/Combiner for Isolation and Insertion Loss (1 megohm loads)

A square wave with period ranging between 20 nanoseconds (ns) and 1 microsecond (us) was applied to input 1 with 50 ohm loads on input 2 and the output. The same square wave was then applied to input 2 with 50 ohm loads on input 1 and the output. In both instances, the insertion loss was between 2.8 and 6 dB and the input isolation was between 14 and 27.6 dB. Both of these parameters are within the usable range. However, a square wave with a period of less than 1 us could not be passed through the combiner.

This combiner is not usable with loads other than 50 ohm, it does not pass through waveforms with a period of less than 1 us, and it AC couples the signals. External level shifting would be required to obtain digital logic levels.

7.4.3 Op-amp Combiner

The third combiner evaluated is based on the Comlinear CLC103 op-amp, using a circuit similar to that published in an earlier RADC report [8]. The CLC103 is rated at Iout of 200 mA for a full power bandwidth of 80 MHz with a 20 V peak-to-peak input. A copy of the data sheet for the Comlinear Corporation CLC103 op-amp and the parts list for the combiner circuit are in Appendix A.2. This data sheet was reprinted with the written permission of Comlinear Corporation. A schematic of the combiner circuit is shown in Figure 7.4.3.1.

The RF input of the combiner was characterized for a frequency range of 0.1 to 200 MHz with a 1 megohm load. The gain of the circuit decreases from 6.8 dB at 1 MHz to -7.4 dB at 200 MHz. The isolation between the RF and the digital input is between 33.4 and 45.3 dB. Figure 7.4.3.2 shows the characteristics of the op-amp combiner with respect to frequency.

The op-amp combiner was also characterized for digital inputs using the DAS9200. With the digital input switching 0 to 4.5 volts (V) at frequencies ranging from 1 kHz to 25 MHz, the combiner output remained at 4.8 V and the coupled signal at the RF port was 10 millivolts (mV).

As can be seen in Figure 7.4.3.2, the transfer function of the op-amp combiner for RF is flat until the -3 dB point is reached at approximately 70 MHz. However, the response of the combiner flattens out again until the -6 dB (50% power) point occurs at approximately 150 MHz. Thus, the 50% power bandwidth of the op-amp combiner circuit is approximately 150 MHz.

The op-amp combiner circuit exhibited characteristics superior to those of the Picosecond Pulse Labs bias-tee and the Mini-Circuits splitter/combiner. Thus, the op-amp combiner circuit was chosen for the RF upset testing.

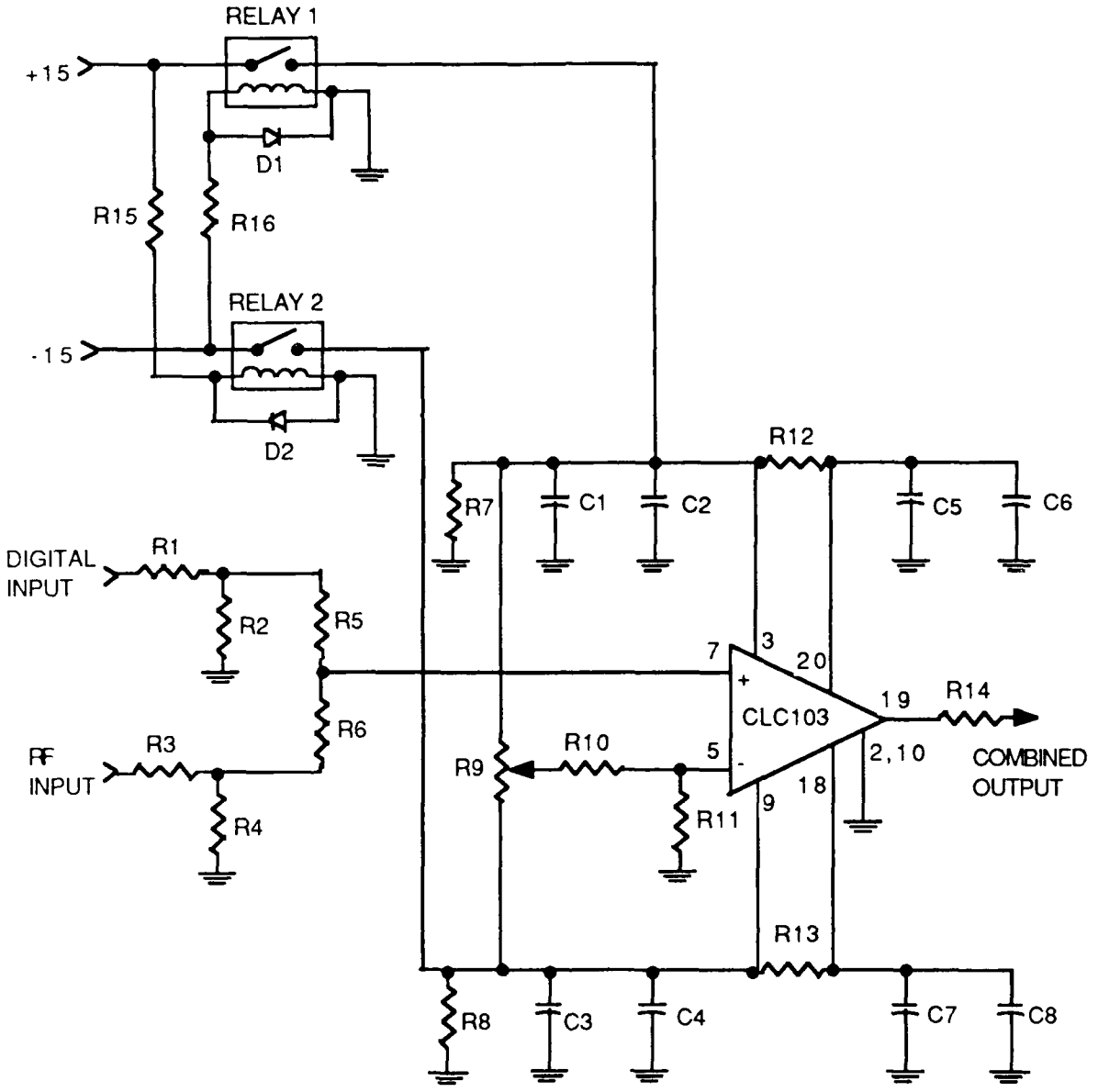


Figure 7.4.3.1 - Op-amp Combiner Schematic

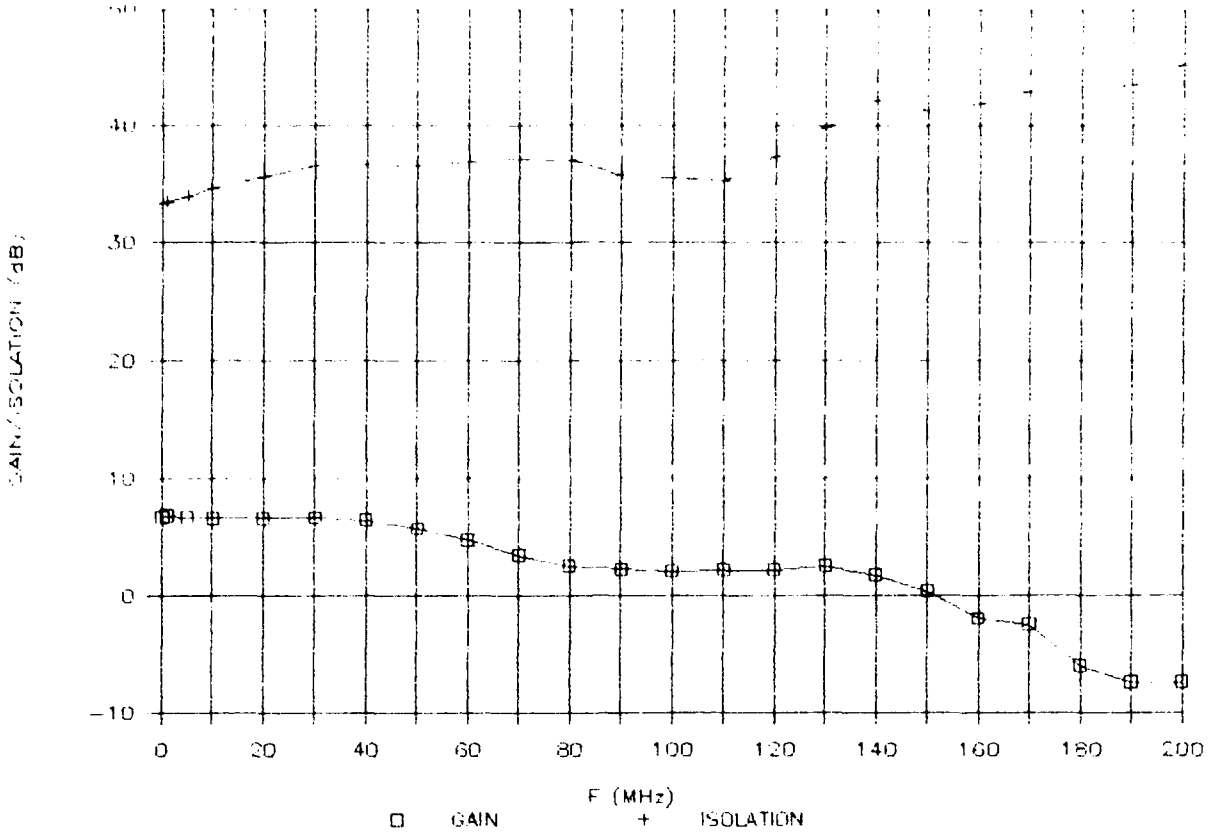


Figure 7.4.3.2 - Characterization of Op-amp Combiner for Isolation and Gain (1 megohm Loads)

7.5 Test Configuration

The test configuration is shown in Figure 7.5.1. The equipment required to synchronize the RF and digital signals consists of a Hewlett-Packard model 8082A pulse generator and Tektronix P6460 external control probe for the DAS9200 system. The pulse generator is capable of producing fast pulses with repetition rates between 1 kHz and 250 MHz, transition times down to 1 ns and amplitudes up to 5 V. The P6460 probe is used to acquire the external clock signal for the DAS9200 system.

The modulation and synchronization control clock works as follows: The RF signal from the Hewlett-Packard 8656A signal generator is applied to the external trigger input of the Hewlett-Packard 8082A pulse generator, the output of which is fed to the clock input of the Tektronix P6460 external control probe which supplies the clock signal for the DAS9200 system. Thus, the DAS9200 is synchronized with the RF signal.

The RF signal produced by the Hewlett-Packard 8656A signal generator goes to the Modulation and Synchronization Control block and to the variable attenuator. The output of the variable attenuator goes to the 40 dB RF amplifier, the output of which is applied to the RF port of the combiner. The test pattern for the DUT pin being tested is applied to the digital port of the combiner. A Tektronix storage oscilloscope is used to measure the RF input into the combiner and the combined output of the combiner. The output of the combiner is connected to an SMA vacuum feedthrough connector, which in turn is connected to the DUT fixture by a coaxial cable.

The pattern generator and acquisition pods from the data acquisition system described in Section 7.2, are connected to the dual inline vacuum feedthrough connectors, which are connected to the DUT fixture by the coaxial cable assembly described in Section 7.1. The data acquisition system also provides the trigger signal for the E-beam tester interface. Thus, the QVC sampling rate is synchronized with the digital test signals for the DUT, which in turn are synchronized with the RF interference signal.

The E-beam tester interface is controlled by the IBM AT personal computer, which facilitates displaying and storing the acquired QVC waveforms. The E-beam tester interface also provides the trigger signal for the Hewlett-Packard 1900A pulse generator which generates the fast pulses for the beam blanker. The E-beam tester interface also permits the computer to take over the control of the SEM during a QVC waveform acquisition.

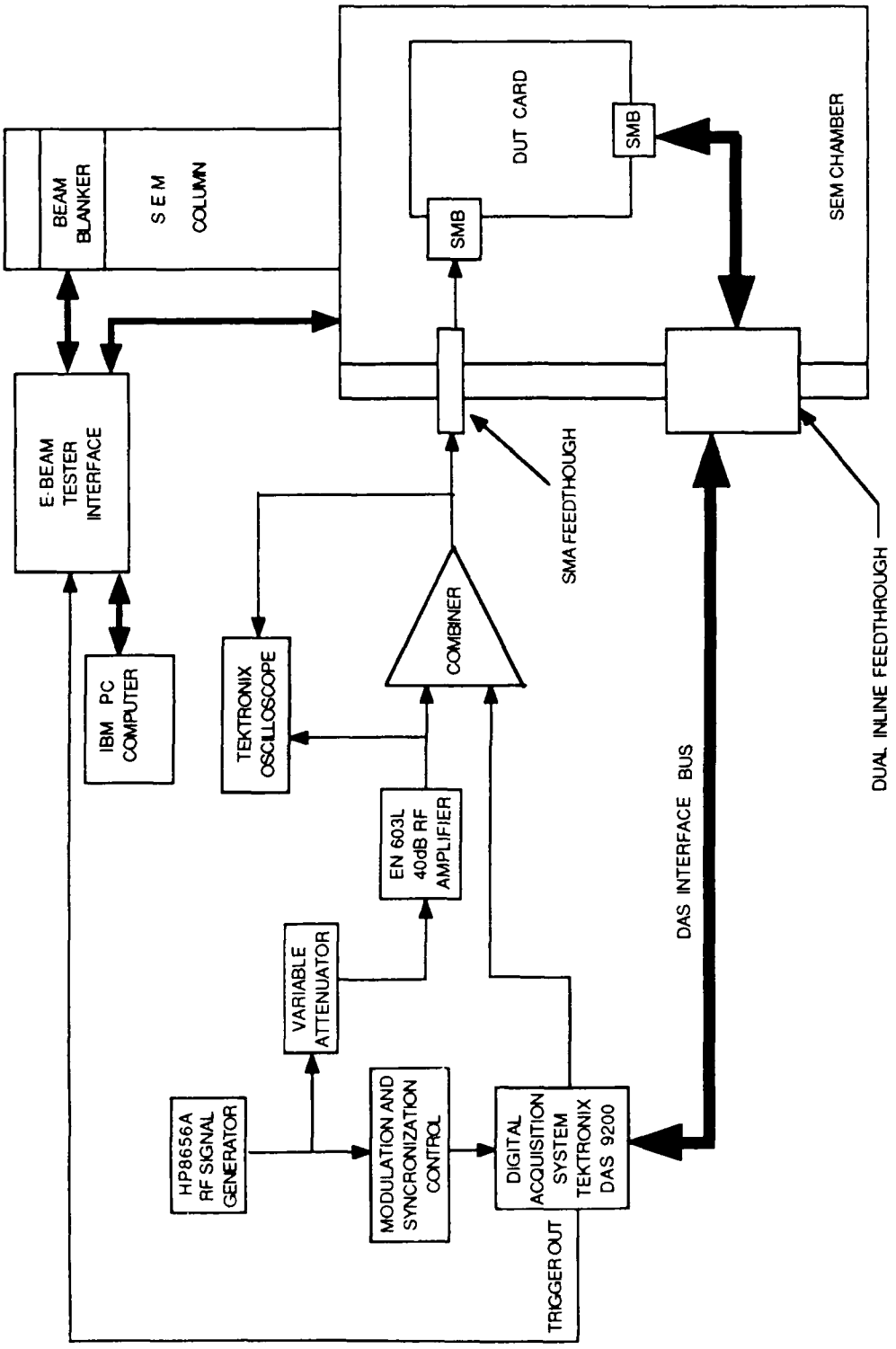


Figure 7.5.1 - Test Configuration

8.0 DEVICE RF UPSET CHARACTERIZATION

This section describes the RF upset characterization testing and the results obtained.

8.1 Definition of Upset

In this report, circuit upset due to injected RFI will be defined in three levels: functional failure, parametric changes, and feedthrough.

Functional failure is defined as any anomalous output logic level (e.g. a logic 1 when a logic 0 is expected or a logic 0 when a logic 1 is expected) at one or more output pins. To prevent permanent device damage the power level was not increased above the level that caused a functional failure.

Parametric changes can be divided into DC (supply current, threshold levels and output levels) and AC (propagation delay, rise/fall times, and set and hold times) characteristics. Although a minor change in these parameters may not cause a nominal device to go out of specification, it could cause a system failure if the device is used in a marginal design or if the device itself is marginal. Any change in the measured parameters as a resulted of the injected RFI will be considered upset.

Feedthrough is coupling of the RFI to other internal nodes or to the outputs. This was measured at the outputs using an oscilloscope and at a variety of internal nodes using the SEM QVC system.

8.2 Test Methodology

Figure 8.2 illustrates the test methodology. The device under test (DUT) was operated in its intended mode and the output waveform stored in the data acquisition system (DAS9200). The RF interference test waveform at the lowest frequency and at an initial amplitude was applied and the circuit operated. The RF level was increased or decreased until the upset threshold level was reached. The peak-to-peak RF voltage upset level was recorded, the device was verified to be functioning properly without RF interference, the RF frequency was increased, and the test repeated.

The peak-to-peak upset voltage level and the complex impedance (Z = R + jX) were used in Equation 1 to calculate upset power.

$$P_{ave} = (1/8)Vpp^2\{R/(R^2+X^2)\} \qquad 1)$$

Where P_{ave} is average power, Vpp is peak-to-peak RF voltage, R is the real part of the complex input impedance, and X is the imaginary part of the complex input impedance.

An upset condition is detected by the DAS9200 by comparing the output waveform on both Q and Q-not with RF applied, to the normal operating baseline waveform. The normal operating baseline waveform, for a given output, is the sequence of high and low logic levels that occurs without RF applied.

To better describe the data, a number of graphs are provided. In analyzing the results it is apparent that a comparison of upset susceptibility can be done most easily by comparing voltage levels for the different conditions for a given device type. To compare one device type to another it is more meaningful to relate upset power levels, since this takes into account the differences in impedance of the inputs.

Specifics of the test vectors and the upset criteria are discussed for each of the devices in the following sections.

8.3 CD4013B Upset Testing

The upset tests were performed with RF applied to the Vdd, clock input, and data input pins through the combiner described in Section 7.4. The RF interference was discrete CW at frequencies of 1.2, 5, 10, 50, 100, and 200 MHz. All testing was performed without synchronization between the RF signal and the clock and data input signals. Two devices, serial number (SN) 1 and 2, were tested with set and reset active and with set and reset low.

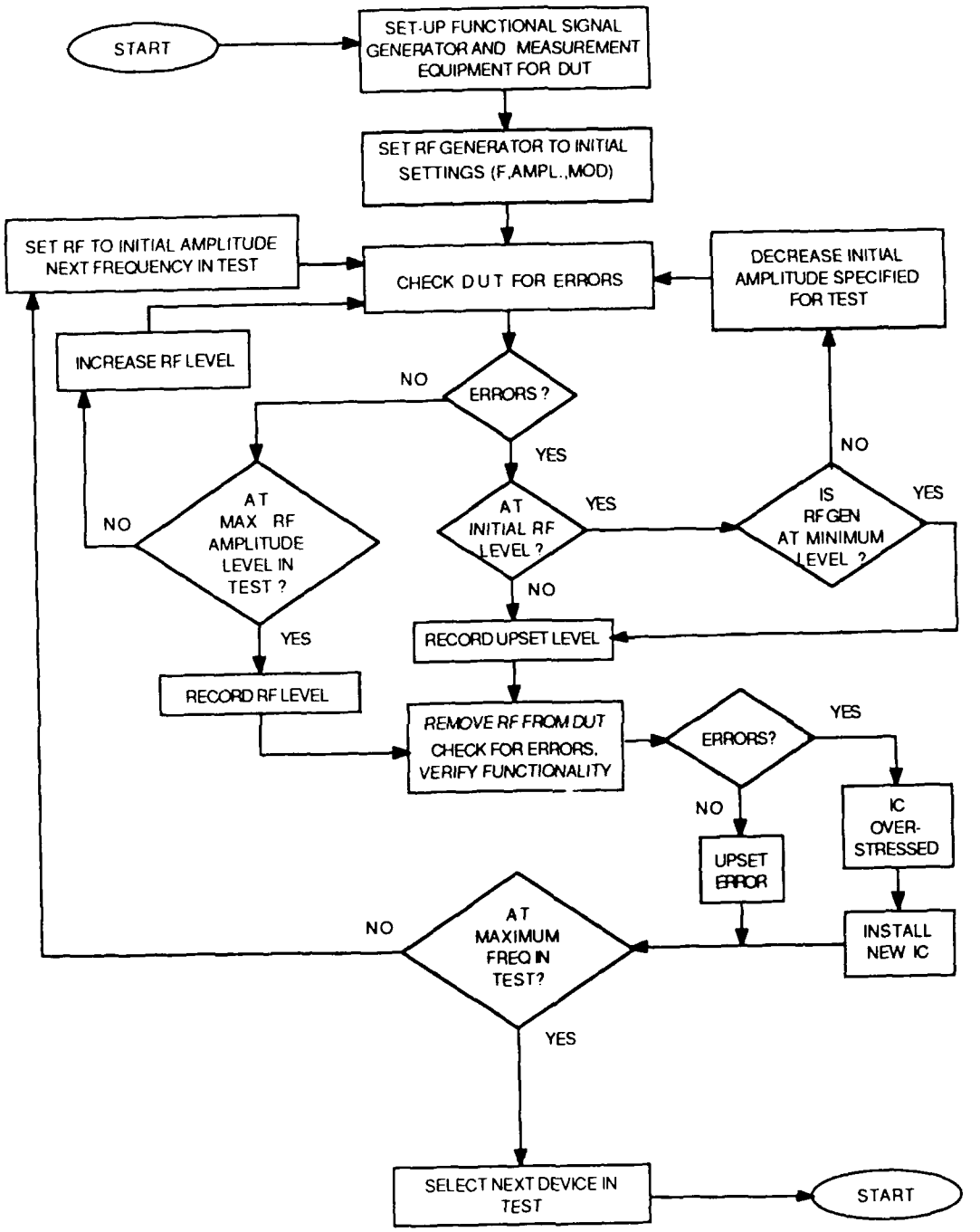


Figure 8.2 - Test Methodology Flow Chart

The complex input impedances of the Vdd, clock input, and data input pins were measured with respect to Vss at each of the RF test frequencies using an HP4191A Impedance Analyzer. Measurements were taken at 1.2, 5, and 10 MHz with the system calibrated up to 15 MHz and measurements were taken at 50, 100, and 200 MHz with the system calibrated up to 1000 MHz. The measured values along with the computed values for the real (R) and imaginary (X) parts for the complex input impedance are given in Table 8.3.1.

		Pin 14, Vdd		
Freq(MHz)	|Z|(ohms)	Theta(deg)	R(ohms)	X(ohms)
1.2	1200	-61	582	1049
5.0	360	-85	31	359
10.0	186	-81	29	184
50.0	38	-71	12	36
100.0	10	-30	9	5
200.0	29	74	8	28

		Pin 5, Data		
Freq(MHz)	|Z|(ohms)	Theta(deg)	R(ohms)	X(ohms)
1.2	23000	-88	803	22986
5.0	5700	-89	99	5699
10.0	2800	-87	146	2796
50.0	596	-84	62	593
100.0	311	-80	54	306
200.0	167	-75	43	161

		Pin 3, Clock		
Freq(MHz)	|Z|(ohms)	Theta(deg)	R(ohms)	X(ohms)
1.2	21000	-88	733	20987
5.0	5100	-88	178	5097
10.0	2500	-85	218	2490
50.0	555	-80	96	547
100.0	305	-74	84	293
200.0	172	-71	56	163

Table 8.3.1 - CD4013B Complex Input Impedance Measurements

The values for the real and imaginary portions of the complex impedance are used in Equation 1 in the form of conductance (G). Where $G = R/(R^2+X^2)$. The units used for conductance are siemens (S). Figure 8.3.1 displays input conductance versus frequency for the Vdd, clock input, and data input pins.

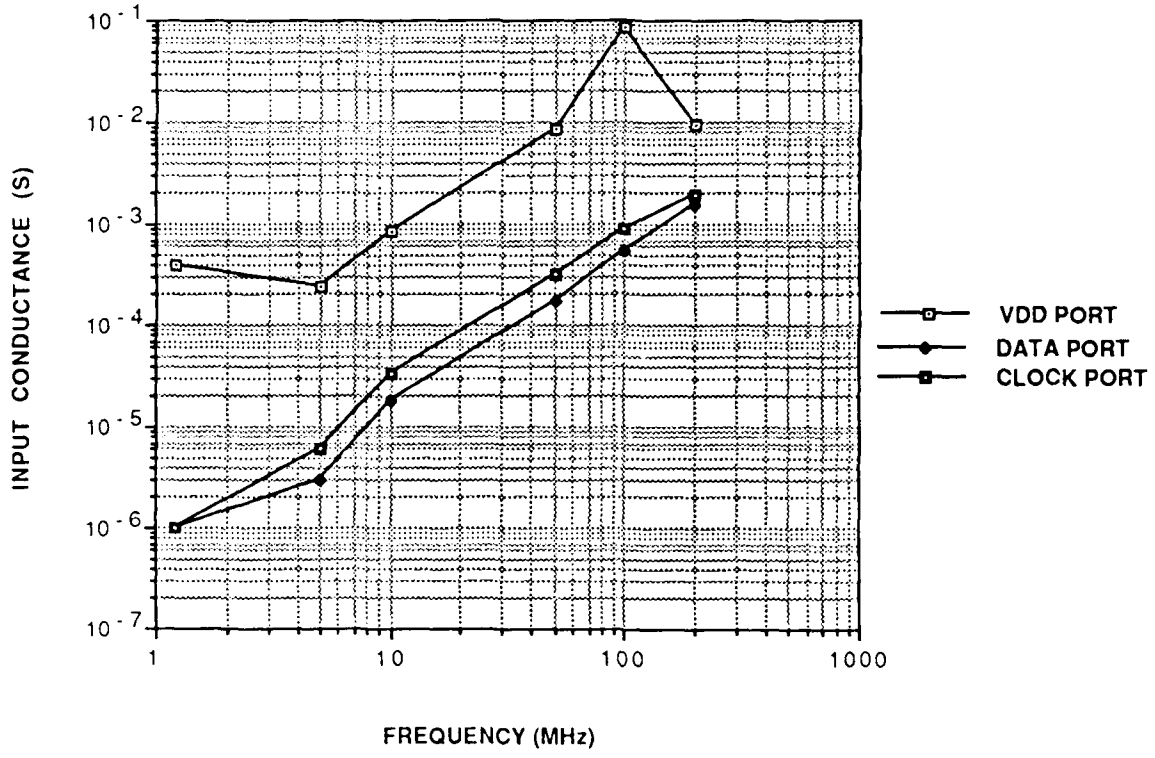


Figure 8.3.1 - CD4013B Input Conductance Versus Frequency

The peak-to-peak voltage levels required to cause upset are provided in Table 8.3.2.

		Pin 14, Vdd		
Freq(MHz)	A(V)	B(V)	C(V)	D(V)
1.2	2.1	2.1	0.8	0.8
5.0	4.8	6.0	8.4	5.2
10.0	7.6	7.3	6.3	5.2
50.0	4.5	4.8	4.8	4.8
100.0	*	*	3.6	4.4
200.0	*	*	*	*

		Pin 5, Data		
Freq(MHz)	A(V)	B(V)	C(V)	D(V)
1.2	3.2	4.0	2.2	2.8
5.0	9.0	7.0	2.7	3.6
10.0	7.2	10.4	3.1	3.6
50.0	9.4	10.8	4.4	4.8
100.0	*	*	3.9	6.4
200.0	*	*	*	*

Table 8.3.2 - CD4013B Upset Voltage Levels
(continued on next page)

		Pin 3, Clock		
Freq(MHz)	A(V)	B(V)	C(V)	D(V)
1.2	2.8	3.2	1.6	1.9
5.0	7.4	4.9	2.9	2.4
10.0	6.4	7.4	2.8	3.6
50.0	10.4	10.8	3.8	5.0
100.0	*	*	2.6	6.0
200.0	*	*	*	*

A = SN1 S,R = low
B = SN2 S,R = low
C = SN1 S,R = active
D = SN2 S,R = active
* = No upset achieved

Table 8.3.2 - CD4013B Upset Voltage Levels (cont.)

The voltages in Table 8.3.2 and the input conductance values are inserted into Equation 1 to calculate average upset power. The resulting graphs, plotted as dBm versus frequency are given in Figures 8.3.2 - 8.3.5. Similar results were obtained on each serial number for the given conditions. The data and clock pins were more susceptible to upset, by 6 to 8 dB, with set and reset active than with set and reset low. The difference is easily identified in Table 8.3.2, with up to seven volts difference between upset voltage levels for the set and reset low conditions versus the active conditions. The condition of the set and reset pins, low or active, did not have as significant of an effect upon the upset levels for the Vdd pin.

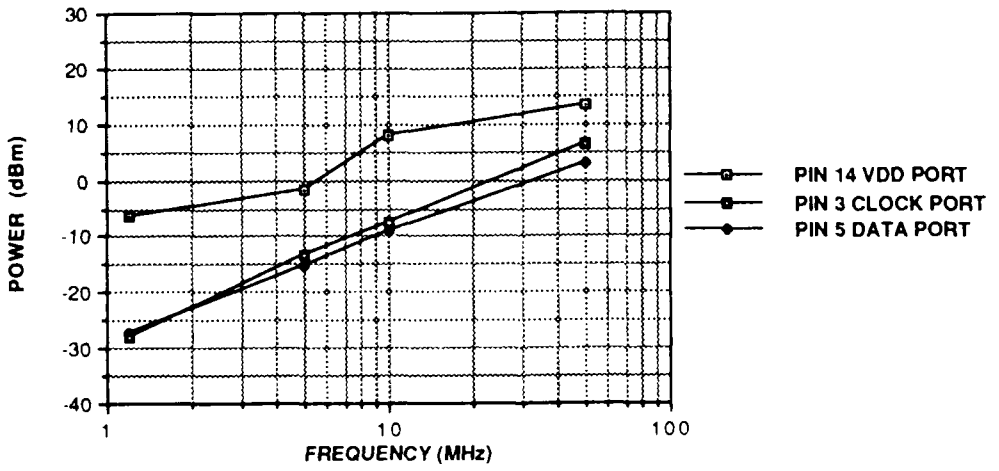


Figure 8.3.2 - CD4013B Upset Power Versus Frequency
SN 1, Set and Reset Low

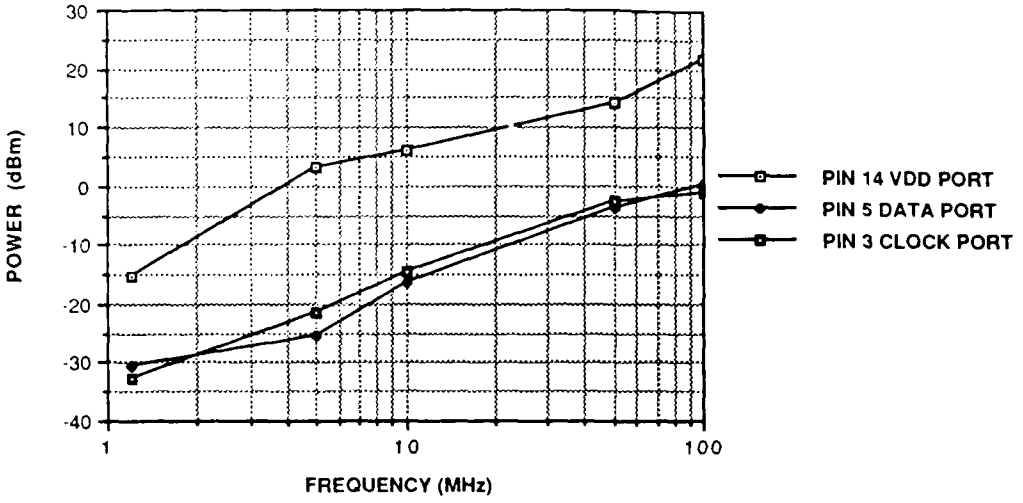


Figure 8.3.3 - CD4013B Upset Power Versus Frequency SN 1, Set and Reset Active

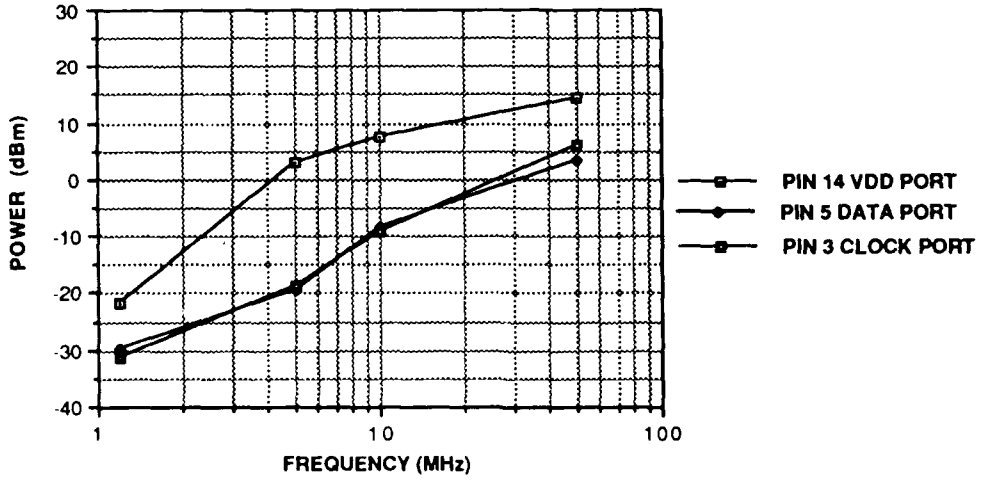


Figure 8.3.4 - CD4013B Upset Power Versus Frequency SN 2, Set and Reset Low

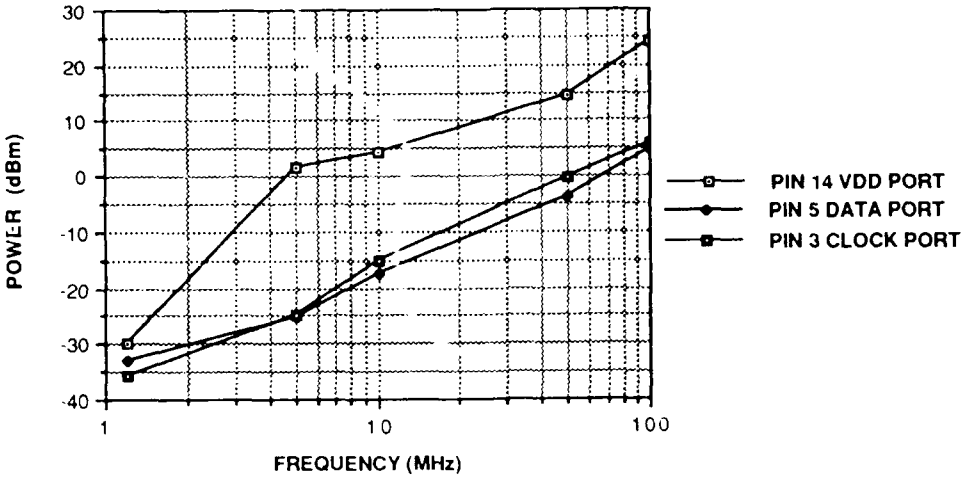


Figure 8.3.5 - CD4013B Upset Power Versus Frequency
SN 2, Set and Reset Active

The waveforms related to operating the CD4013B using the DAS9200 are shown in Figure 8.3.6. The clock frequency is 1.25 MHz which produces an 800 ns clock period. These waveforms are for the case when set and reset were active. When set and reset were low, the output waveforms had the same shape as the data waveform offset by half a clock cycle. The system clock provided the timing for the sampling of the voltage levels of the Q and Q-not outputs. Both outputs of the two flip-flops were sampled every 200 ns. Both flip-flops failed when RF was injected into the Vdd input, while only the flip-flop that had RF on the data or clock input failed under those conditions.

The waveforms, as they appear on the oscilloscope, were photographed at the point where the DAS9200 system detected a failure. Photographs for serial number 1 with set and reset low are provided in Figures 8.3.7 - 8.3.18. Each photograph shows the RF waveform appearance prior to the combiner and the Q output waveform. Figures 8.3.7 - 8.3.10 show the waveforms for the condition of RF injected into pin 14, Vdd, at 1.2, 5, 10, and 50 MHz. Figures 8.3.11 - 8.3.14 show the waveforms for the condition of RF injected into pin 5, the data input at the same frequencies. Figures 8.3.15 - 8.3.18 show the waveforms for the condition of RF injected into pin 3, the clock input at the same frequencies.

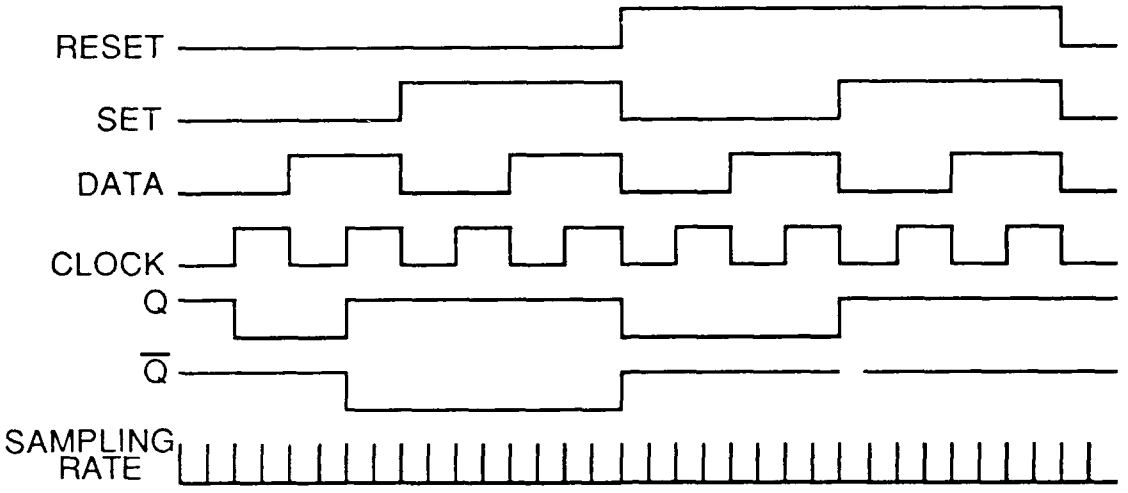


Figure 8.3.6 - CD4013B Timing Diagram

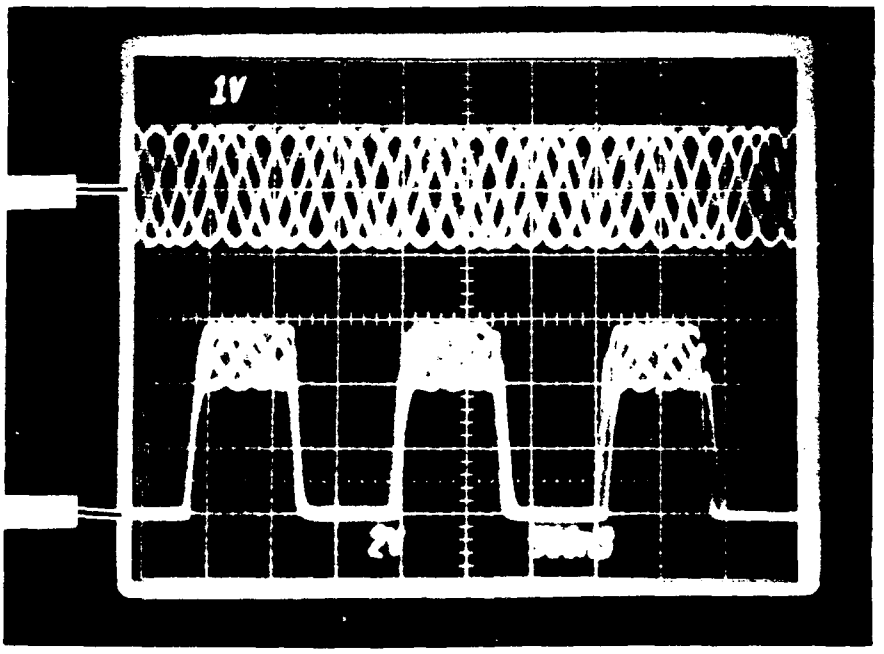


Figure 8.3.7 - CD4013B RF Upset Oscilloscope Photograph
RF Interference on Vdd
Top trace = 1.2 MHz RF
Bottom trace = Q output

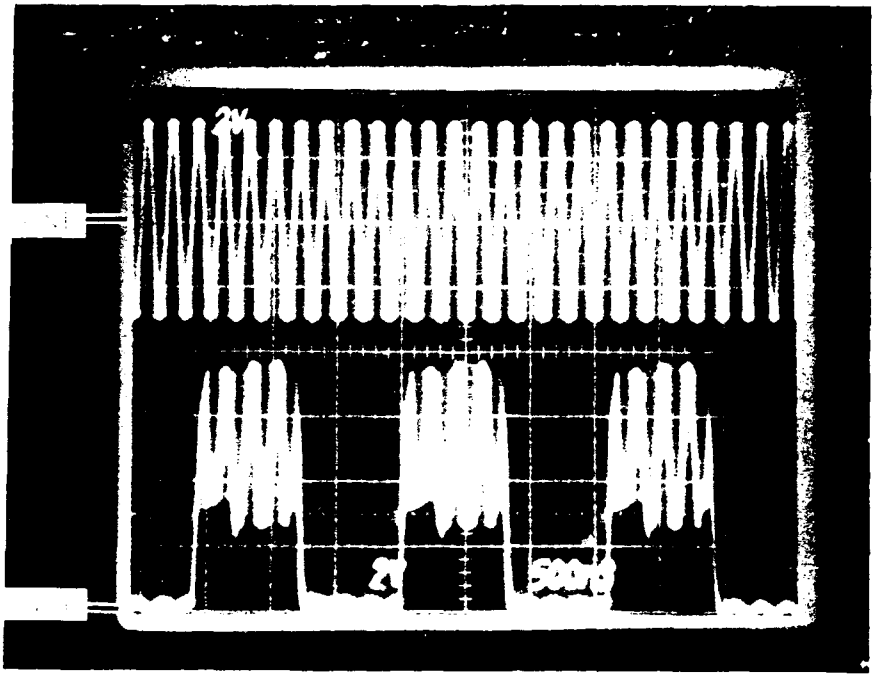


Figure 8.3.8 - CD4013B RF Upset Oscilloscope Photograph
RF Interference on Vdd
Top trace = 5 MHz RF
Bottom trace = Q output

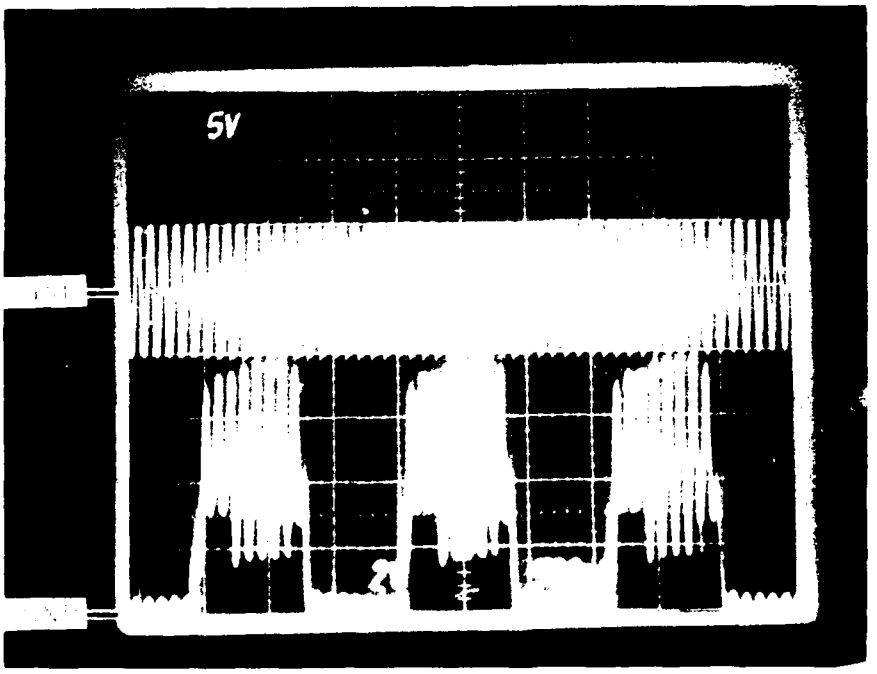


Figure 8.3.9 - CD4013B RF Upset Oscilloscope Photograph
RF Interference on Vdd
Top trace = 10 MHz RF
Bottom trace = Q output

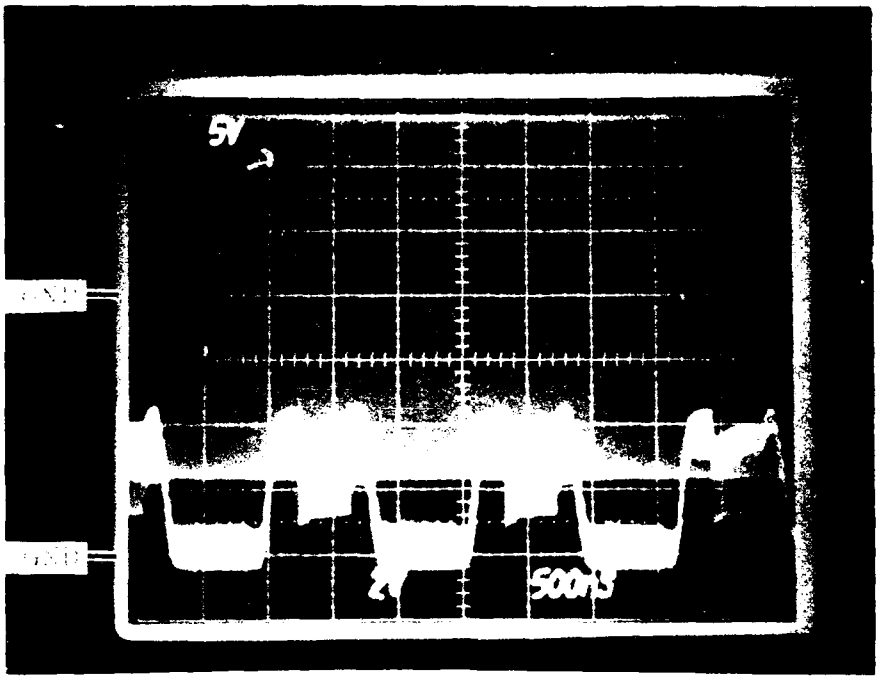


Figure 8.3.10 - CD4013B RF Upset Oscilloscope Photograph
RF Interference on Vdd
Top trace = 50 MHz RF
Bottom trace = Q output

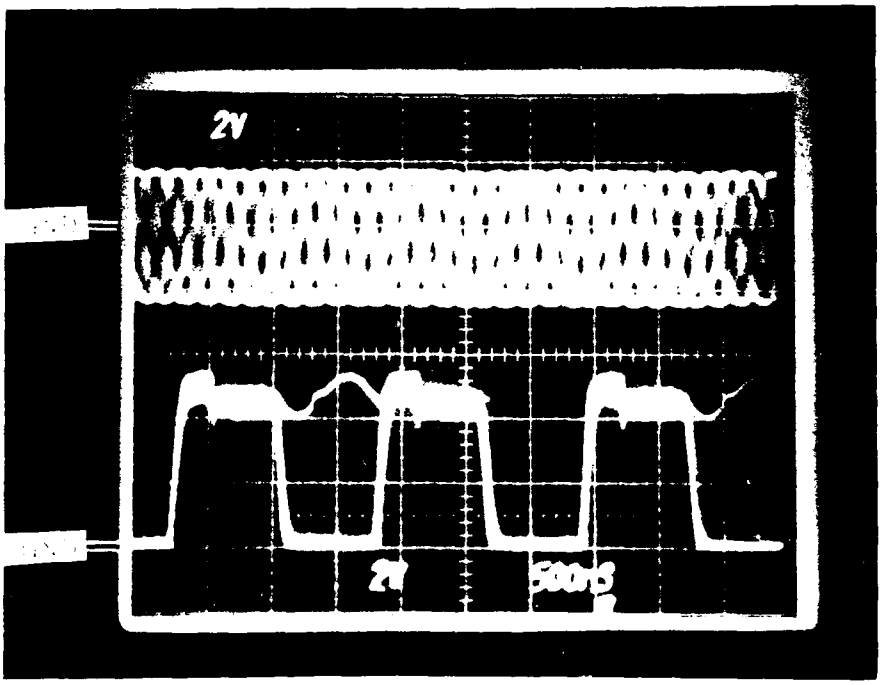


Figure 8.3.11 - CD4013B RF Upset Oscilloscope Photograph
RF Interference on Data Input
Top trace = 1.2 MHz RF
Bottom trace = Q output

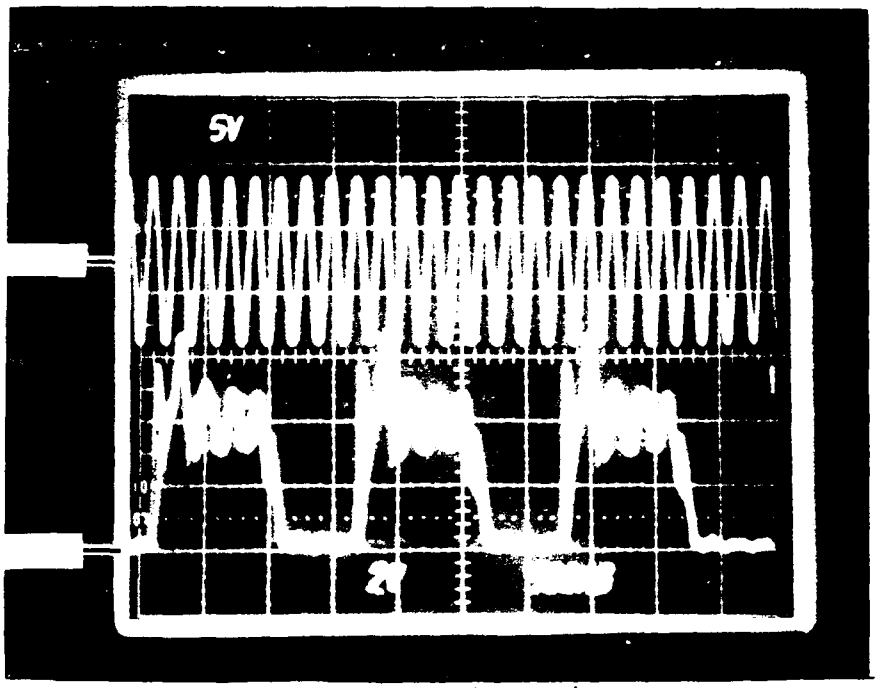


Figure 8.3.12 - CD4013B RF Upset Oscilloscope Photograph
RF Interference on Data Input
Top trace = 5 MHz RF
Bottom trace = Q output

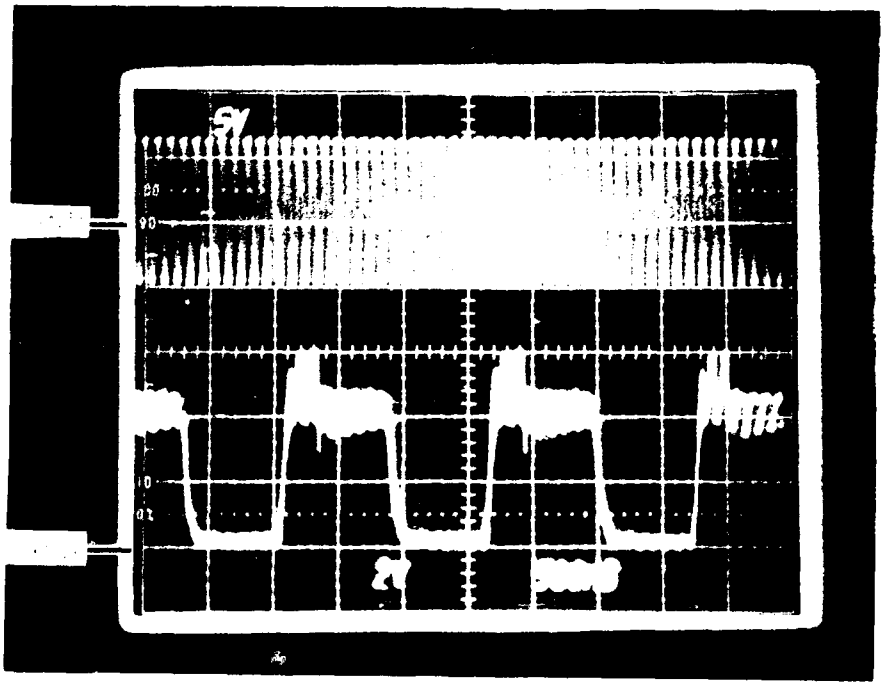


Figure 8.3.13 - CD4013B RF Upset Oscilloscope Photograph
RF Interference on Data Input
Top trace = 10 MHz RF
Bottom trace = Q output

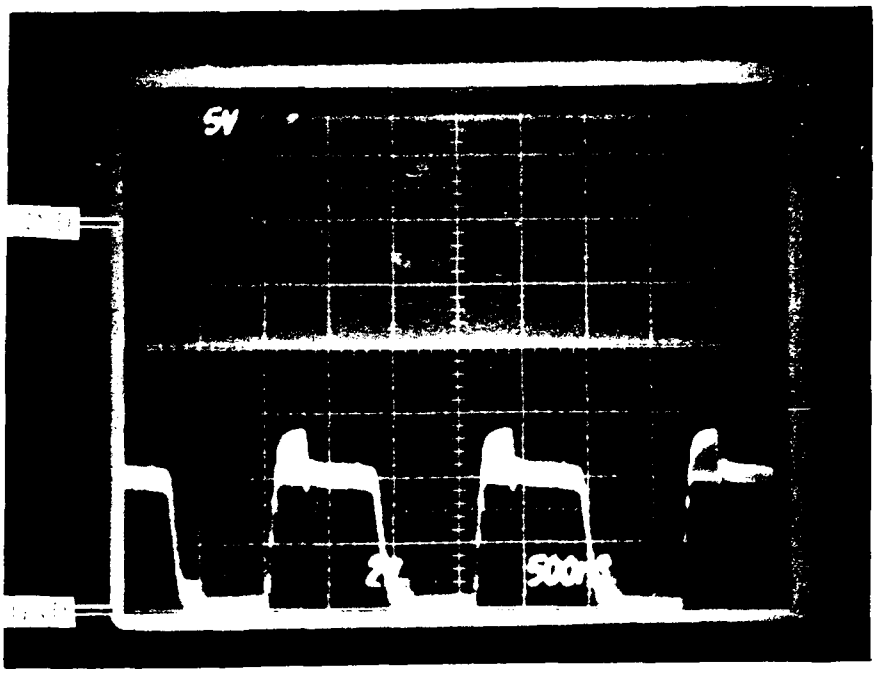


Figure 8.3.14 - CD4013B RF Upset Oscilloscope Photograph
RF Interference on Data Input
Top trace = 50 MHz RF
Bottom trace = Q output

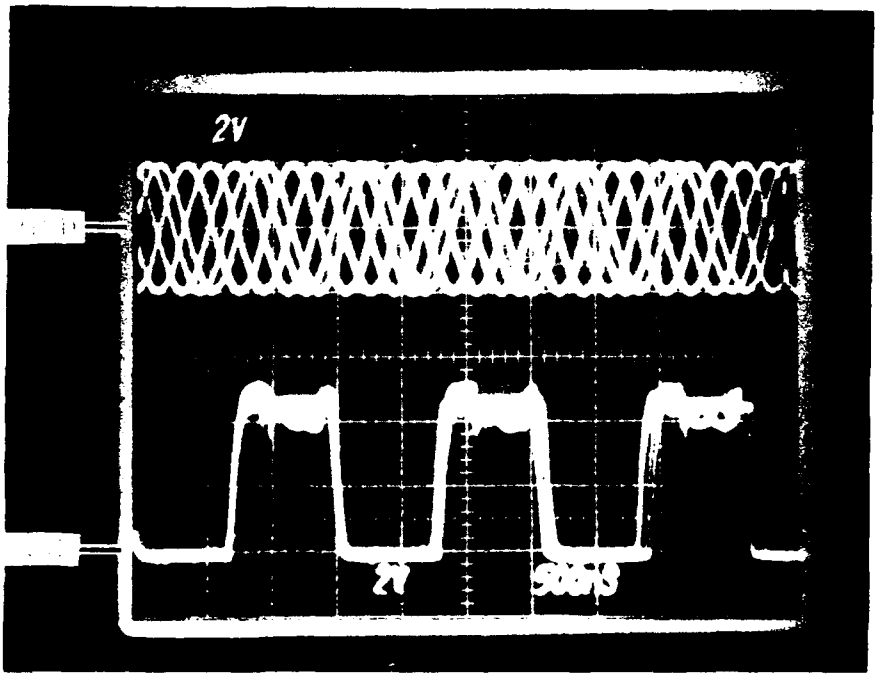


Figure 8.3.15 - CD4013B RF Upset Oscilloscope Photograph
RF Interference on Clock Input
Top trace = 1.2 MHz RF
Bottom trace = Q output

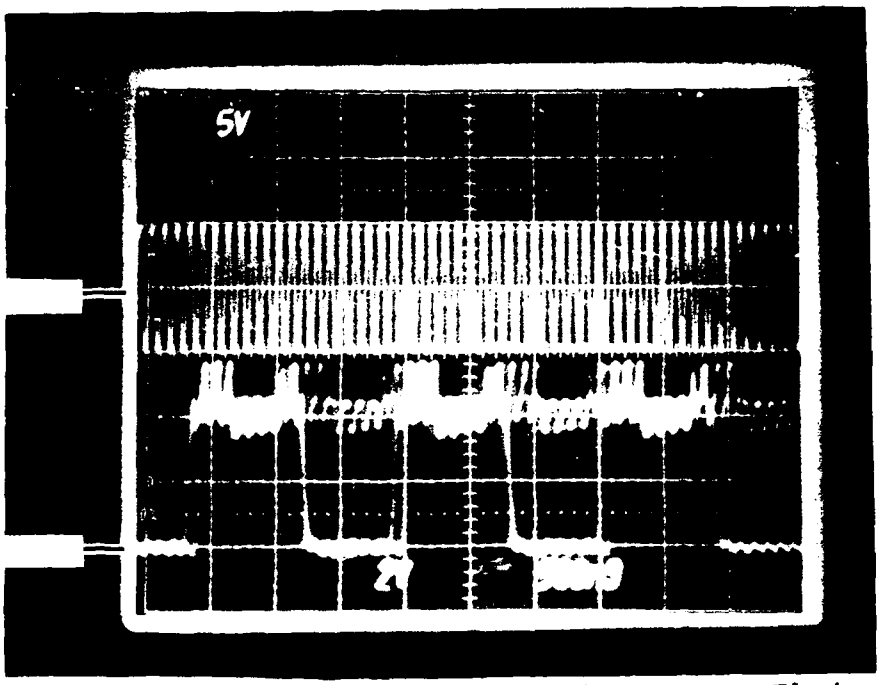


Figure 8.3.16 - CD4013B RF Upset Oscilloscope Photograph
RF Interference on Clock Input
Top trace = 5 MHz RF
Bottom trace = Q output

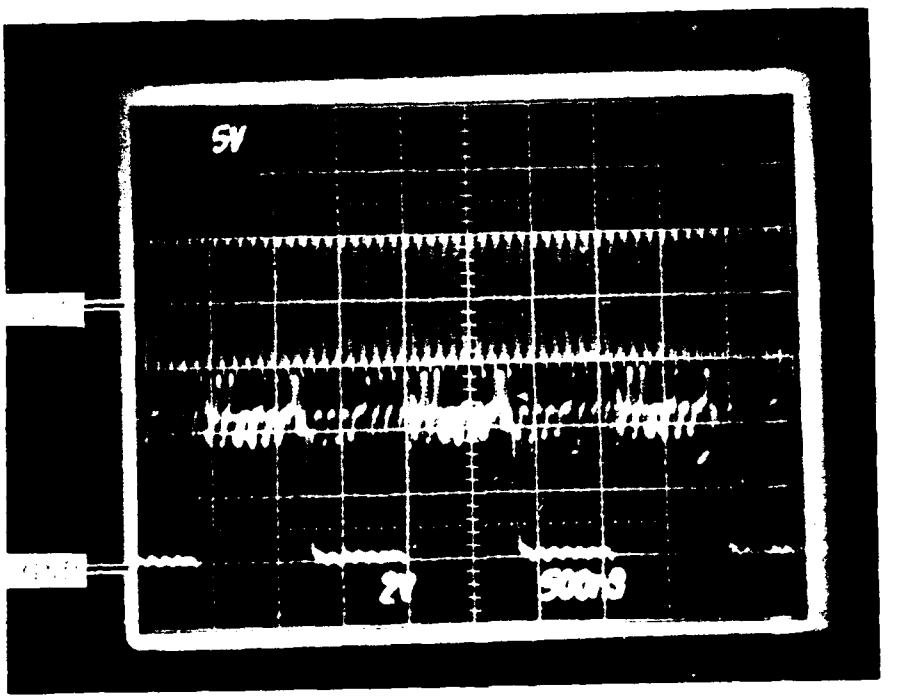


Figure 8.3.17 - CD4013B RF Upset Oscilloscope Photograph
RF Interference on Clock Input
Top trace = 10 MHz RF
Bottom trace = Q output

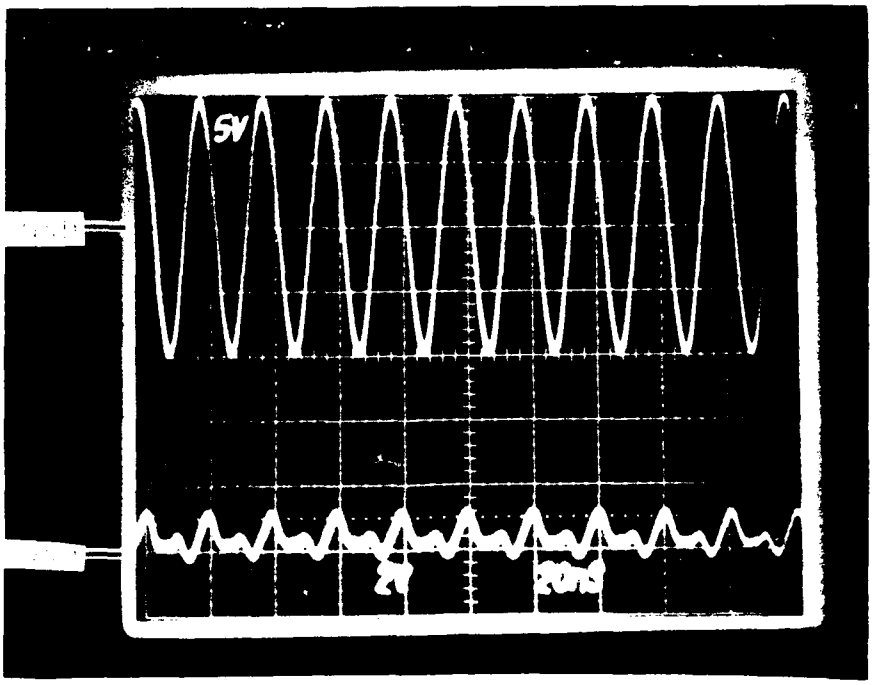


Figure 8.3.18 - CD4013B RF Upset Oscilloscope Photograph
RF Interference on Clock Input
Top trace = 50 MHz RF
Bottom trace = Q output

8.4 SN54ALS74A Upset Testing

The upset tests were performed with RF applied to the Vcc, clock input, and data input pins. The RF interference was discrete CW at 1.2, 5, 10, 50, 100, and 200 MHz. Testing was performed with and without synchronization between the RF signal and the clock and data signals.

The complex input impedance of the Vcc, clock input, and data input pins were measured with respect to the ground pin at each of the RF test frequencies. The measured values along with the computed values for the real (R) and imaginary (X) parts of the complex input impedance are given in Table 8.4.1.

		Pin 14, Vcc		
Freq(MHz)	|Z|(ohms)	Theta(deg)	R(ohms)	X(ohms)
1.2	1400	-10	1379	243
5.0	1100	-37	878	662
10.0	771	-54	453	624
50.0	190	-74	52	183
100.0	90	-72	28	86
200.0	32	-45	23	23

		Pin 2, Data		
Freq(MHz)	|Z|(ohms)	Theta(deg)	R(ohms)	X(ohms)
1.2	28000	-88	977	27983
5.0	6800	-89	119	6799
10.0	3400	-89	59	3399
50.0	691	-88	24	691
100.0	343	-87	18	342
200.0	162	-85	14	161

		Pin 3, Clock		
Freq(MHz)	|Z|(ohms)	Theta(deg)	R(ohms)	X(ohms)
1.2	31000	-88	1082	30981
5.0	7600	-89	133	7599
10.0	3800	-89	66	3799
50.0	772	-89	13	772
100.0	385	-88	13	385
200.0	185	-86	13	184

Table 8.4.1 - SN54ALS74A Complex Input Impedance Measurements

The values for the real and imaginary portions of the complex impedance are used in Equation 1 in the form of conductance. Figure 8.4.1 displays input conductance versus frequency for the Vcc, clock input, and data input pins.

The peak-to-peak upset voltage levels are provided in Table 8.4.2.

			Pin 14, Vcc			
Freq(MHz)	A(V)	B(V)	C(V)	D(V)	E(V)	F(V)
1.2	6.0	6.4	6.4	9.6	5.6	10.0
5.0	5.5	6.2	6.0	6.4	6.0	7.2
10.0	5.4	6.0	6.8	6.1	5.9	23.0
50.0	5.0	4.8	4.8	6.7	4.4	8.4
100.0	2.4	2.8	4.0	*	4.2	*
200.0	*	1.0	1.2	*	*	*

			Pin 2, Data			
Freq(MHz)	A(V)	B(V)	C(V)	D(V)	E(V)	F(V)
1.2	2.4	2.5	2.3	5.6	2.8	4.0
5.0	2.6	3.6	8.0	8.0	5.6	8.8
10.0	2.6	5.2	3.6	3.4	6.3	10.0
50.0	3.0	3.4	3.6	7.3	3.0	2.8
100.0	3.1	2.3	2.2	3.3	3.1	2.2
200.0	1.8	1.2	1.4	0.9	*	*

			Pin 3, Clock			
Freq(MHz)	A(V)	B(V)	C(V)	D(V)	E(V)	F(V)
1.2	1.9	1.6	2.0	2.2	2.0	3.4
5.0	1.4	1.8	2.1	2.0	2.2	3.2
10.0	1.4	1.6	1.8	2.0	1.8	3.3
50.0	1.5	1.5	1.8	2.1	1.7	2.6
100.0	1.6	1.4	1.8	2.4	1.6	3.2
200.0	1.0	1.0	1.5	1.3	1.2	2.4

A = SN 1, No sync, Clk = 1.25 kHz
B = SN 1, No sync, Clk = 500 kHz
C = SN 1, No sync, Clk = 1.25 MHz
D = SN 1, Sync, Clk = 1.25 MHz
E = SN 4, No sync, Clk = 1.25 MHz
F = SN 4, Sync, Clk = 1.25 MHz
* = No upset achieved

Table 8.4.2 - SN54ALS74A Upset Voltage Levels

The voltages in Table 8.4.2 and the input conductance values are inserted into Equation 1 to calculate average upset power. The resulting graphs, plotted as dBm versus frequency, are given in Figures 8.4.2 - 8.4.7.

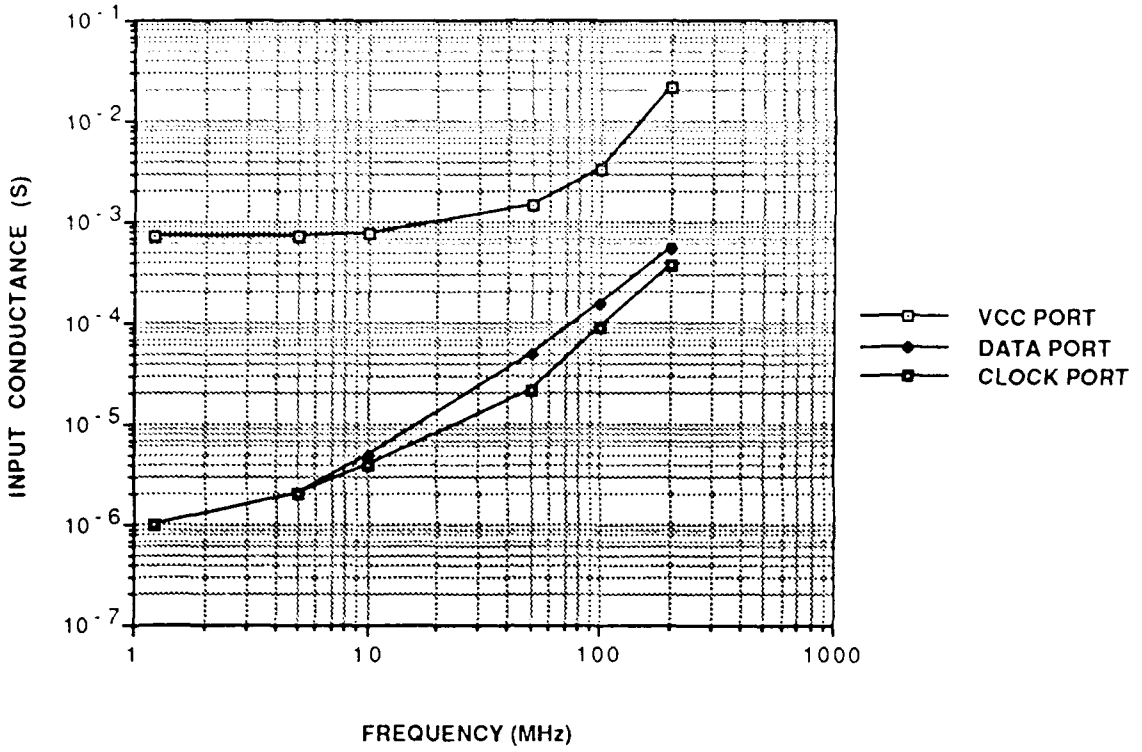


Figure 8.4.1 - SN54ALS74A Input Conductance Versus Frequency

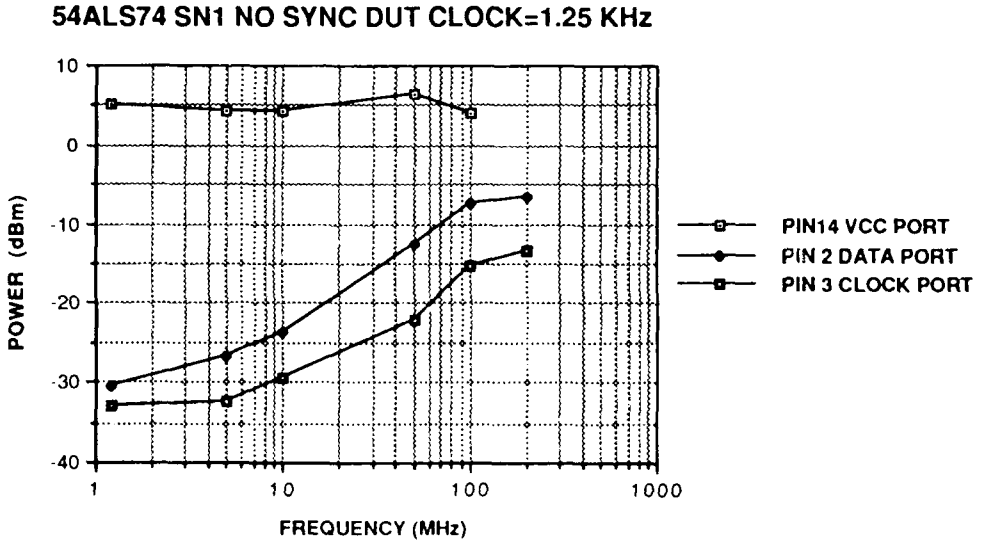


Figure 8.4.2 - SN54ALS74A Upset Power Versus Frequency
SN 1, No Sync, Clk = 1.25 kHz

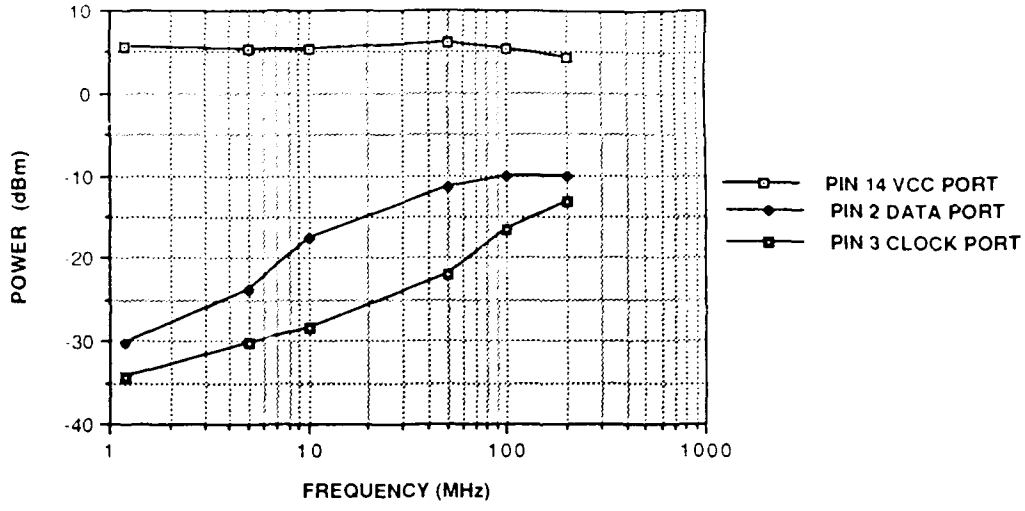


Figure 8.4.3 - SN54ALS74A Upset Power Versus Frequency SN 1, No Sync, Clk = 500 kHz

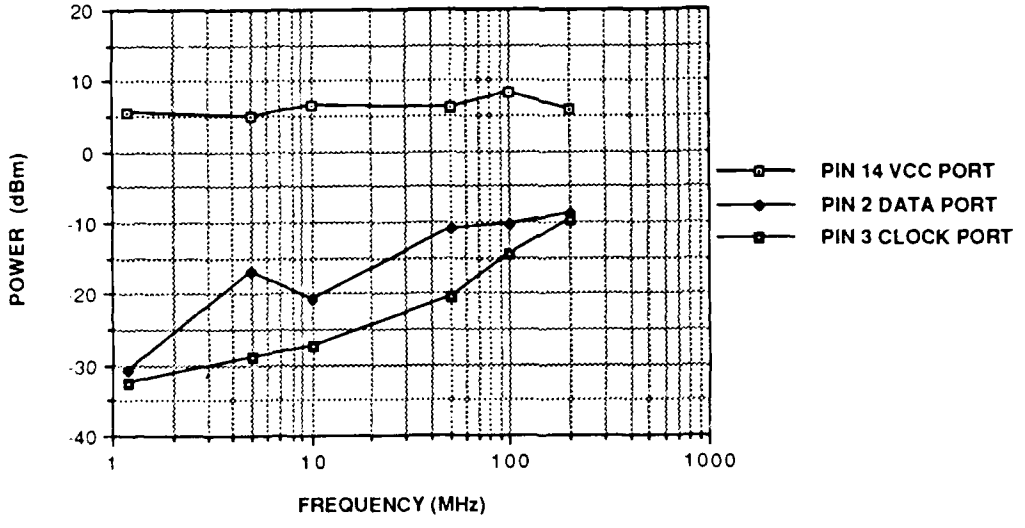


Figure 8.4.4 - SN54ALS74A Upset Power Versus Frequency SN 1, No Sync, Clk = 1.25 MHz

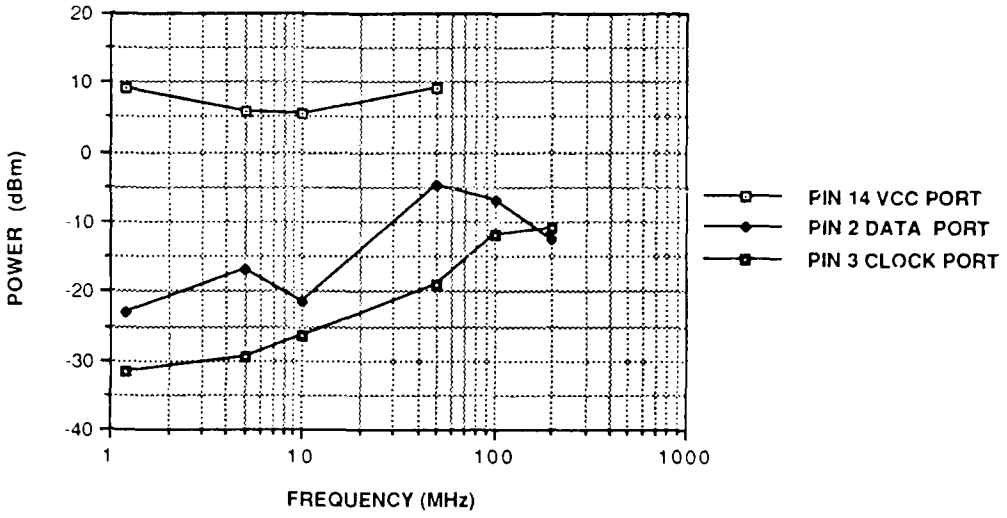


Figure 8.4.5 - SN54ALS74A Upset Power Versus Frequency SN 1, Sync, Clk = 1.25 MHz

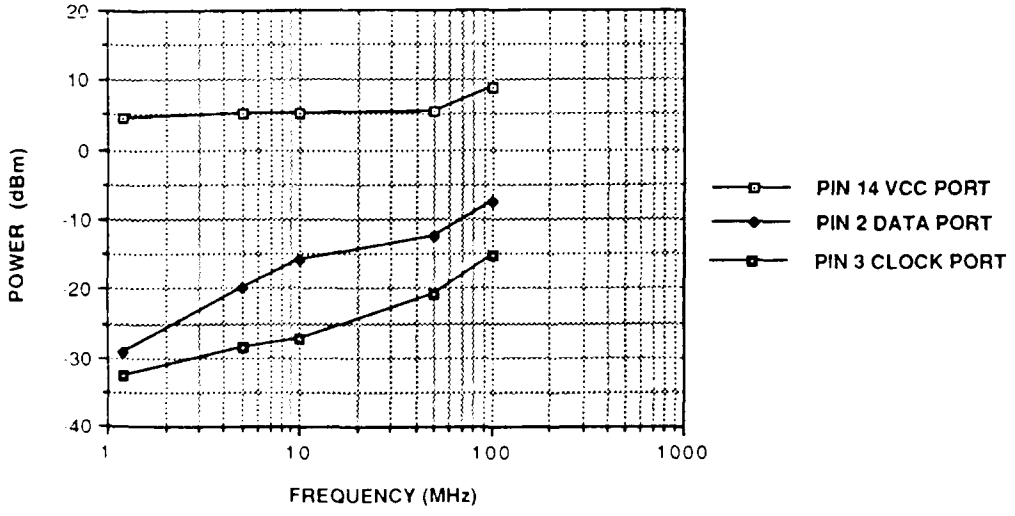


Figure 8.4.6 - SN54ALS74A Upset Power Versus Frequency SN 4, No Sync, Clk = 1.25 MHz

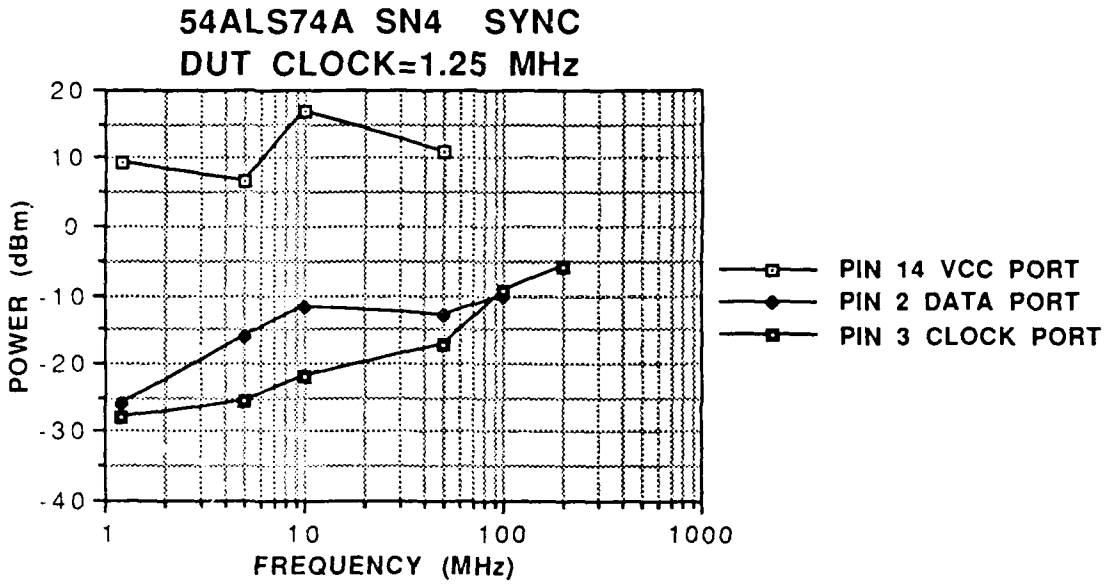


Figure 8.4.7 - SN54ALS74A Upset Power Versus Frequency, SN 4, Sync, Clk = 1.25 MHz

The results indicate that the clock operating frequency has little effect on the upset level. The parts exhibited lower upset voltage levels without synchronization of the RF with the clock. This effect is expected since the most sensitive coincidence of the timing of these two signals is allowed to occur without the synchronization.

The waveforms related to operating the SN54ALS74A using the DAS9200 are shown in Figure 8.4.8. The clock frequency was varied from 1.25 kHz to 1.25 MHz. The sampling rate for the output level varied from 200 us at 1.25 kHz to 200 ns at 1.25 MHz. Both flip-flops failed when RF was injected into the Vcc input while only the flip-flop that had RF on the data or clock input failed under those conditions.

The waveforms, as they appear on the oscilloscope, were photographed at the point where the DAS9200 system detected a failure. Photographs for serial number 1 with set and reset active and no synchronization between the timing of the RF interference and the digital signals are provided in Figures 8.4.9 - 8.4.26. The photographs show the Q output waveform, the RF waveform appearance prior to the combiner and the sampling signal waveform. Figures 8.4.9 - 8.4.14 show the waveforms for the condition where RF is injected into pin 14, Vcc at 1.2, 5, 10, 50, 100, and 200 MHz. Figures 8.4.15 - 8.4.20 show the waveforms for the condition where RF is injected into pin 5, the data input at 1.2, 5, 10, 50, 100, and 200 MHz. Figures 8.4.21 - 8.4.26 show the waveforms where RF is injected into pin 3, the clock input at 1.2, 5, 10, 50, 100, and 200 MHz.

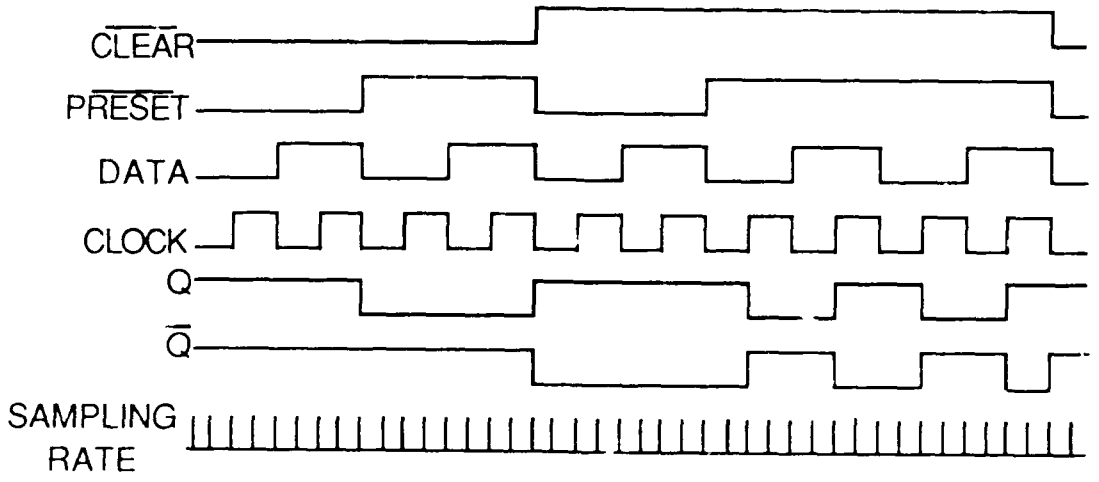


Figure 8.4.8 - SN54ALS74A Timing Diagram

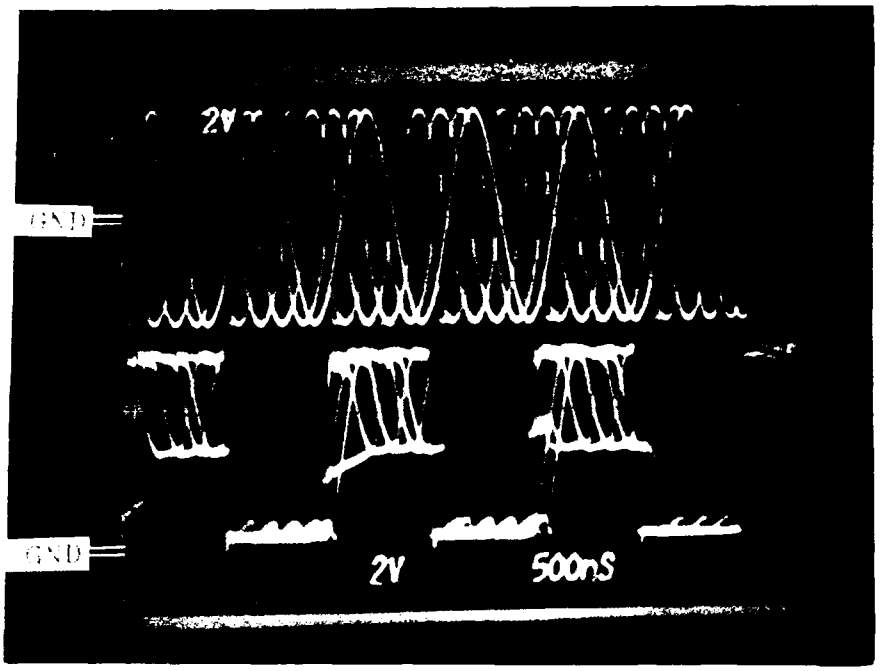


Figure 8.4.9 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Vcc
Top trace = 1.2 MHz RF
Bottom trace = Q output

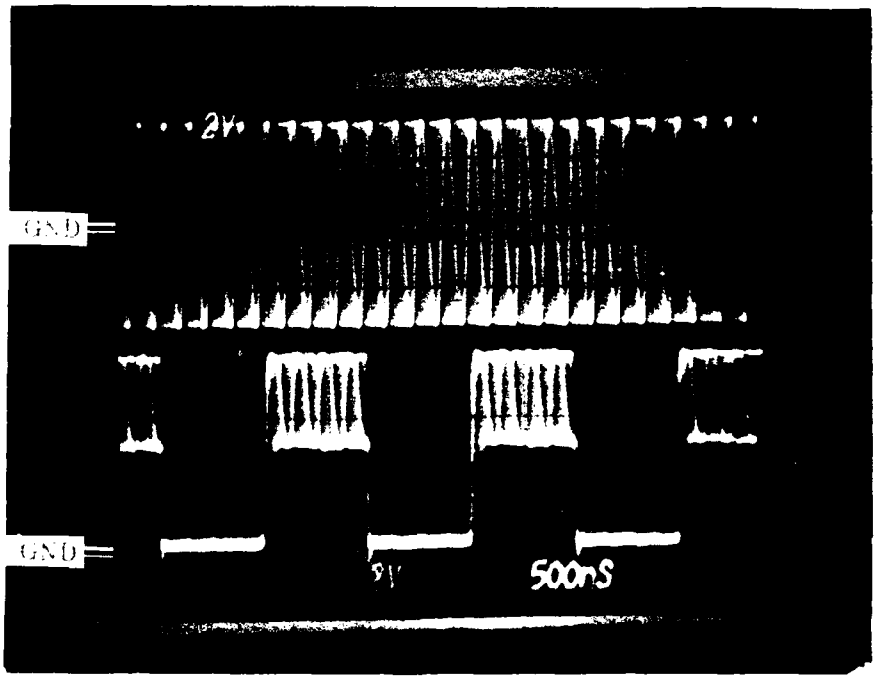


Figure 8.4.10 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Vcc
Top trace = 5 MHz RF
Bottom trace = Q output

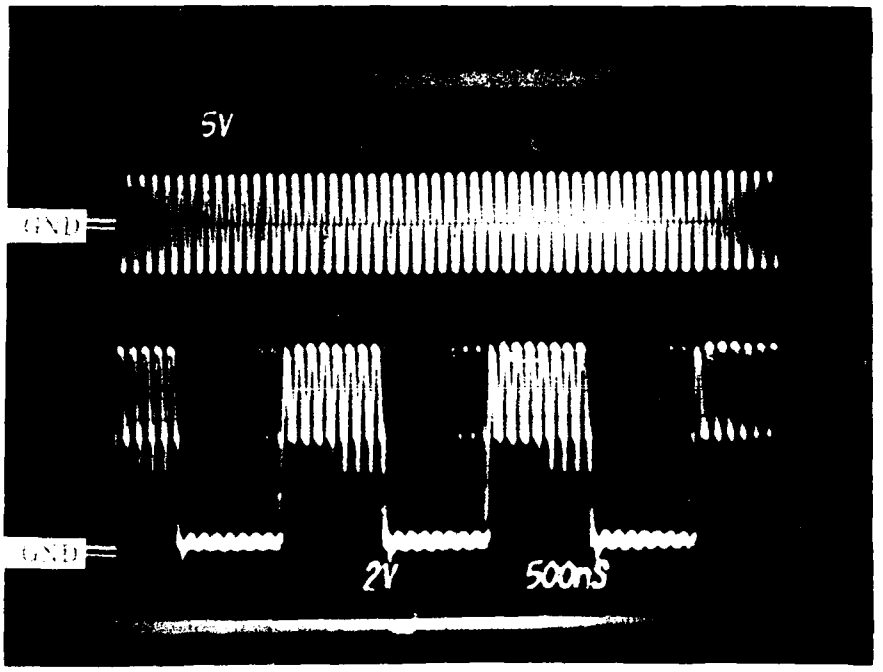


Figure 8.4.11 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Vcc
Top trace = 10 MHz RF
Bottom trace = Q output

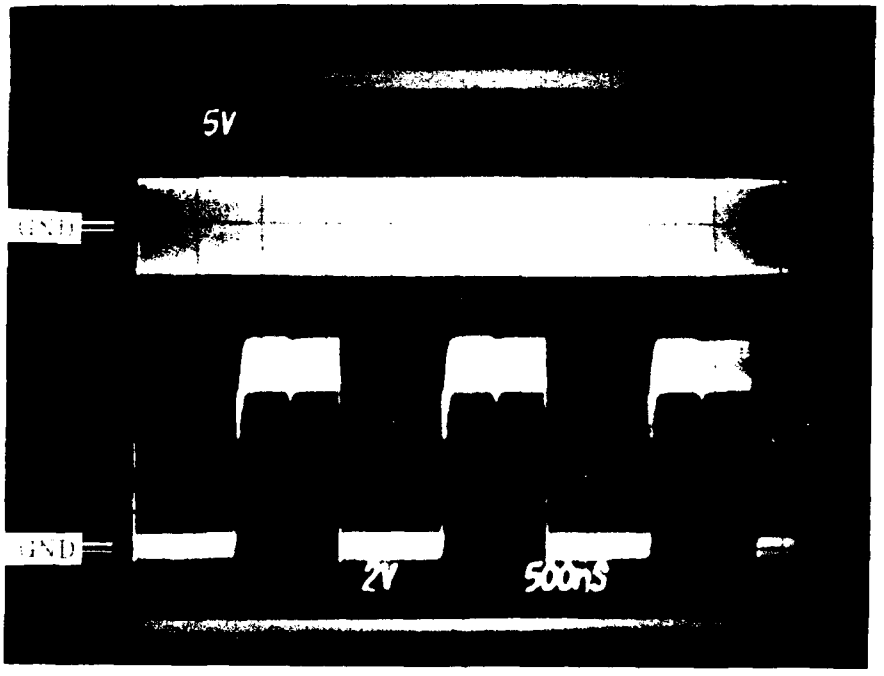


Figure 8.4.12 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Vcc
Top trace = 50 MHz RF
Bottom trace = Q output

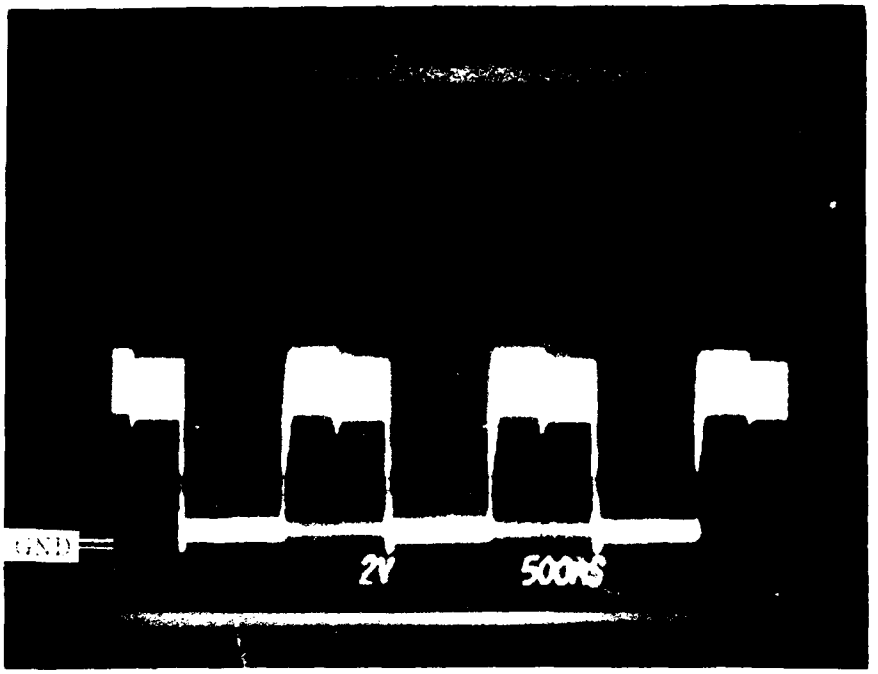


Figure 8.4.13 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Vcc
100 MHz RF (not shown)
Bottom trace = Q output

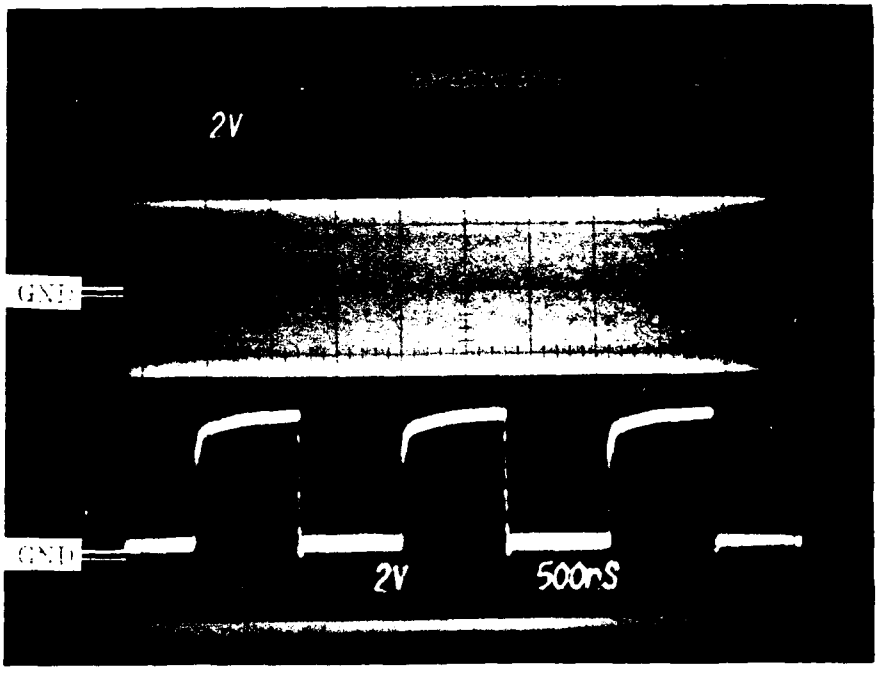


Figure 8.4.14 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Vcc
Top trace = 200 MHz RF
Bottom trace = Q output

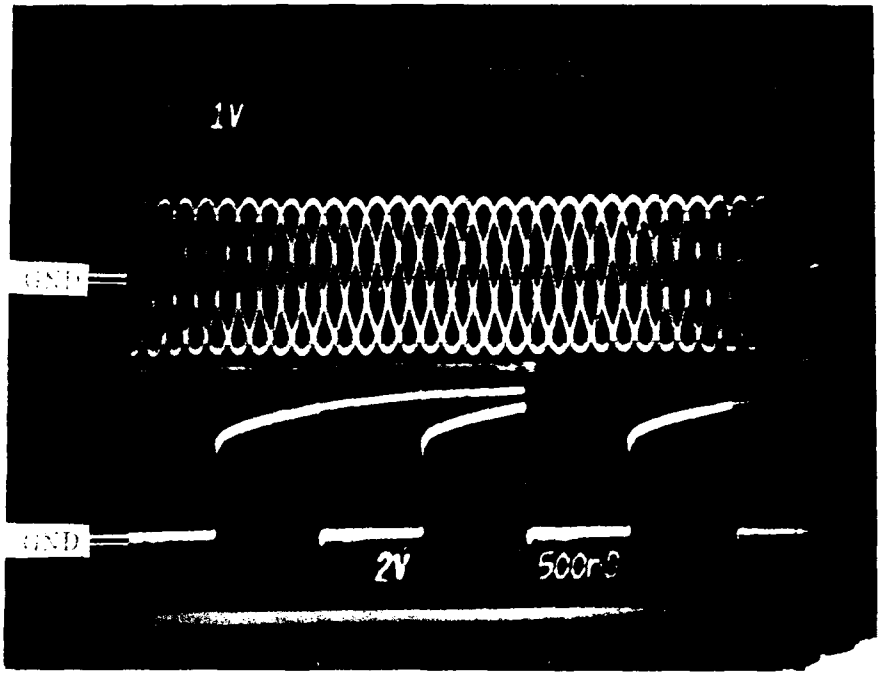


Figure 8.4.15 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Data Input
Top trace = 1.2 MHz RF
Bottom trace = Q output

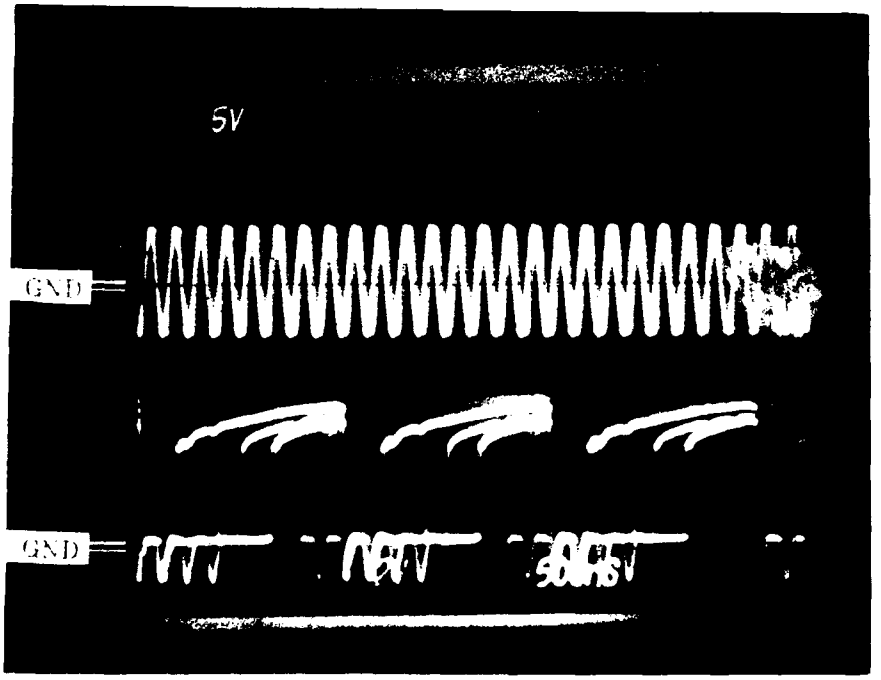


Figure 8.4.16 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Data Input
Top trace = 5 MHz RF
Bottom trace = Q output

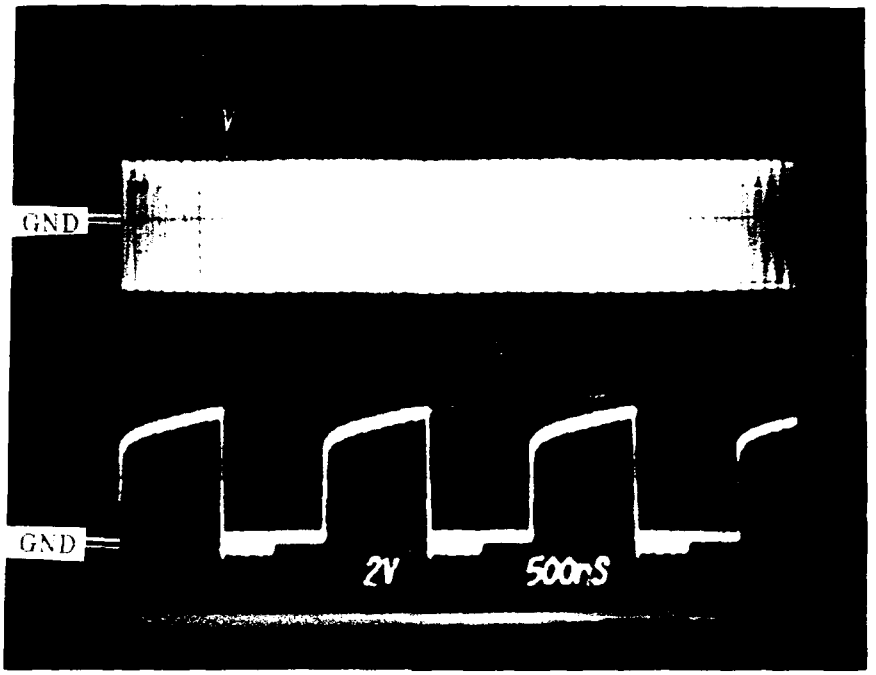


Figure 8.4.17 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Data Input
Top trace = 10 MHz RF
Bottom trace = Q output

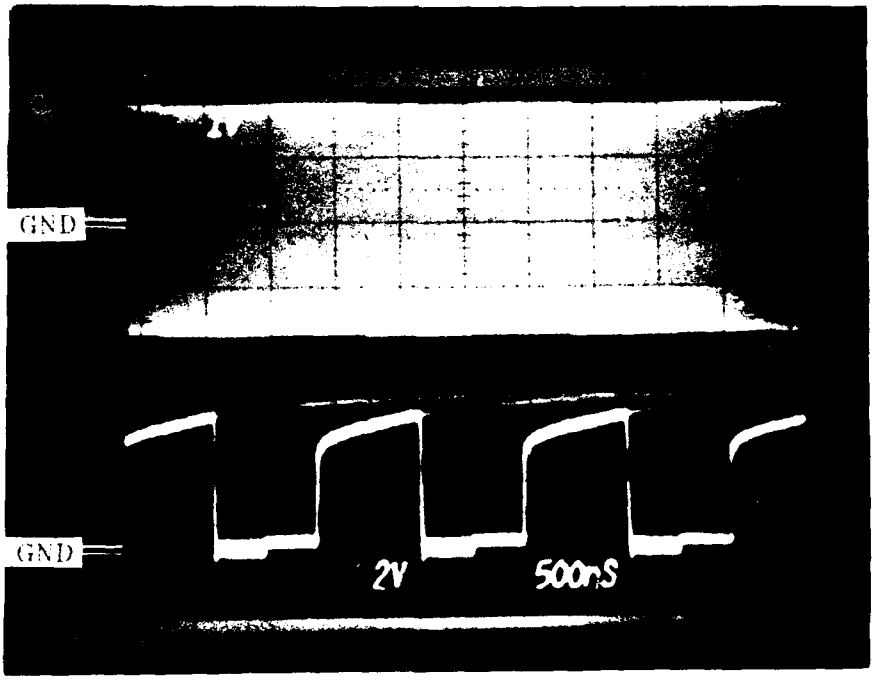


Figure 8.4.18 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Data Input
Top trace = 50 MHz RF
Bottom trace = Q output

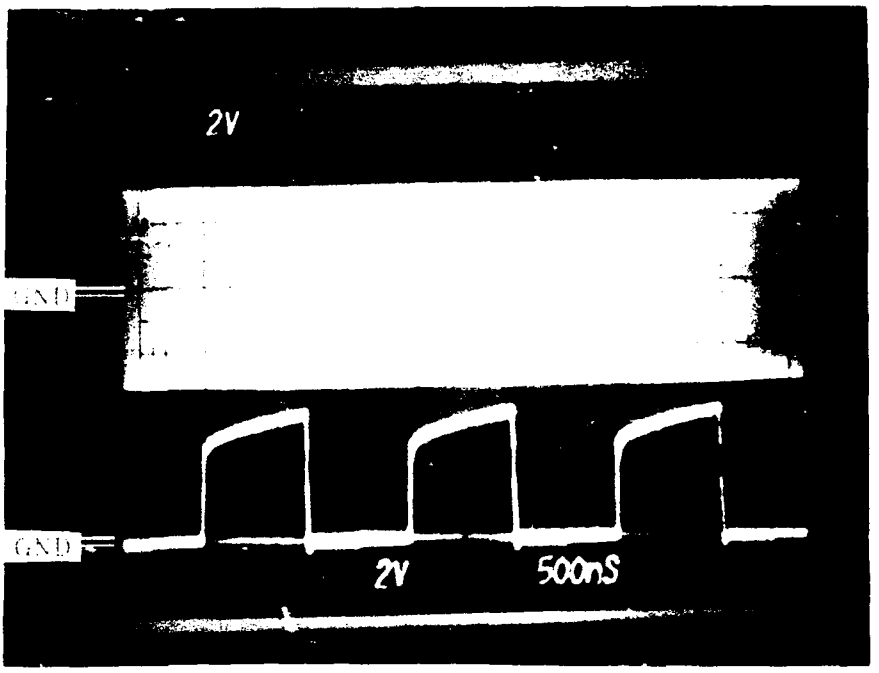


Figure 8.4.19 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Data Input
Top trace = 100 MHz RF
Bottom trace = Q output

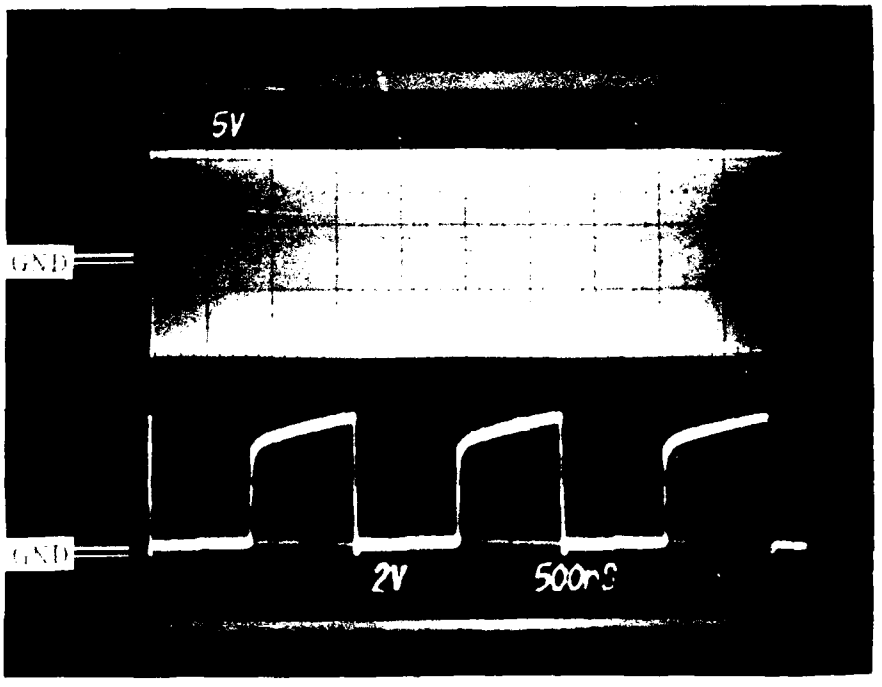


Figure 8.4.20 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Data Input
Top trace = 200 MHz RF
Bottom trace = Q output

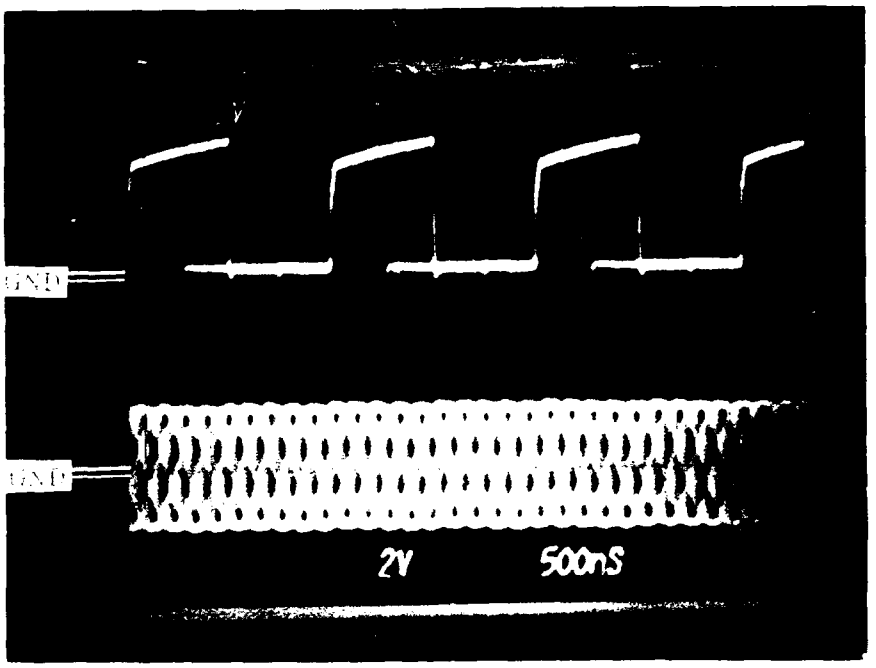


Figure 8.4.21 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Clock Input
Top trace = 1.2 MHz RF
Bottom trace = Q output

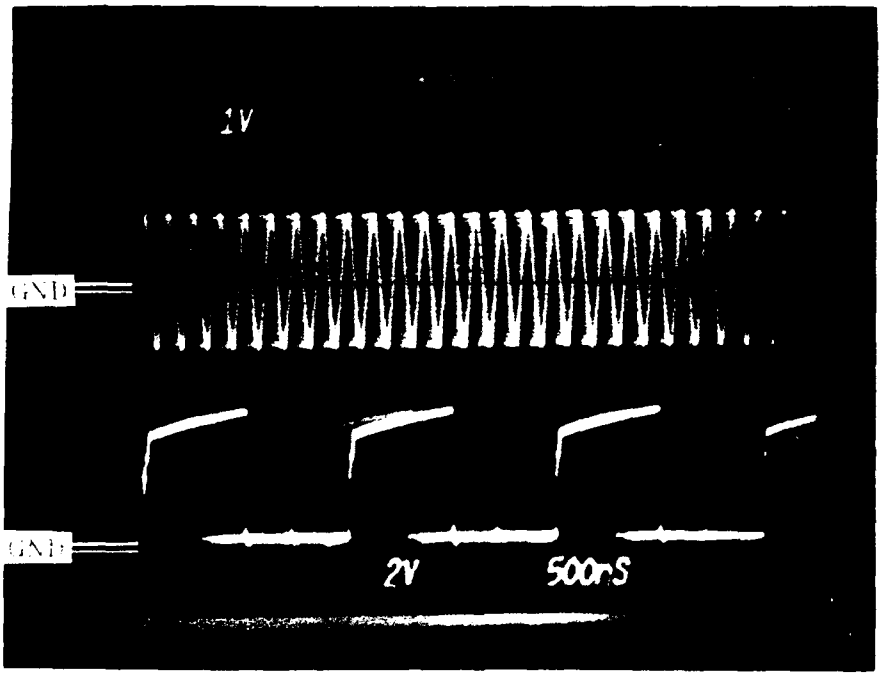


Figure 8.4.22 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Clock Input
Top trace = 5 MHz RF
Bottom trace = Q output

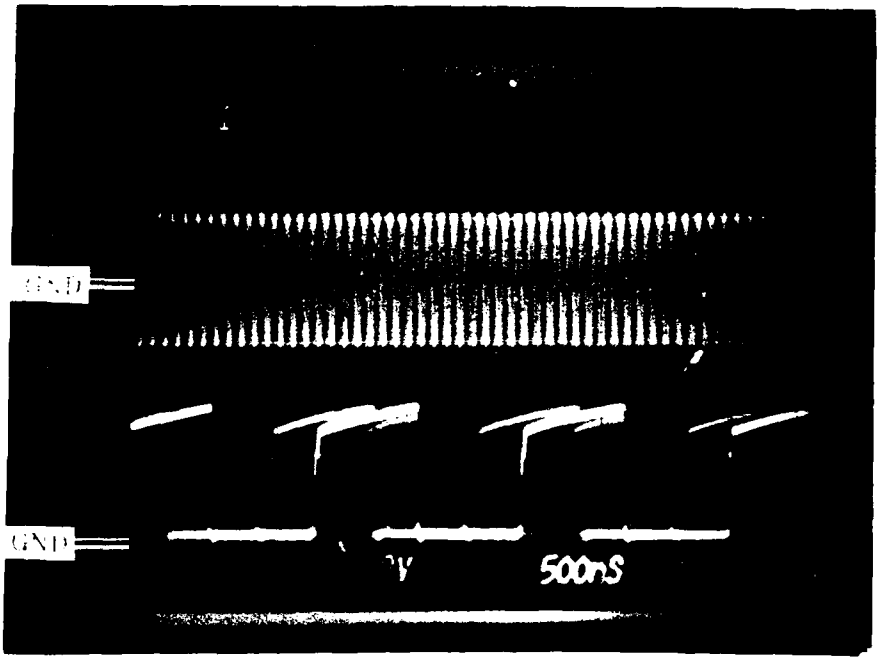


Figure 8.4.23 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Clock Input
Top trace = 10 MHz RF
Bottom trace = Q output

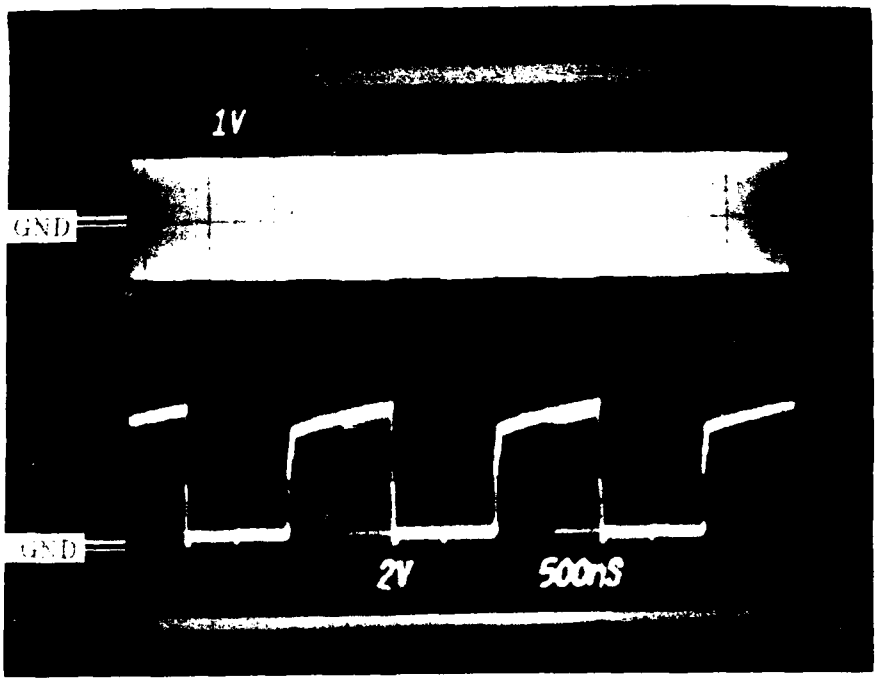


Figure 8.4.24 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Clock Input
Top trace = 50 MHz RF
Bottom trace = Q output

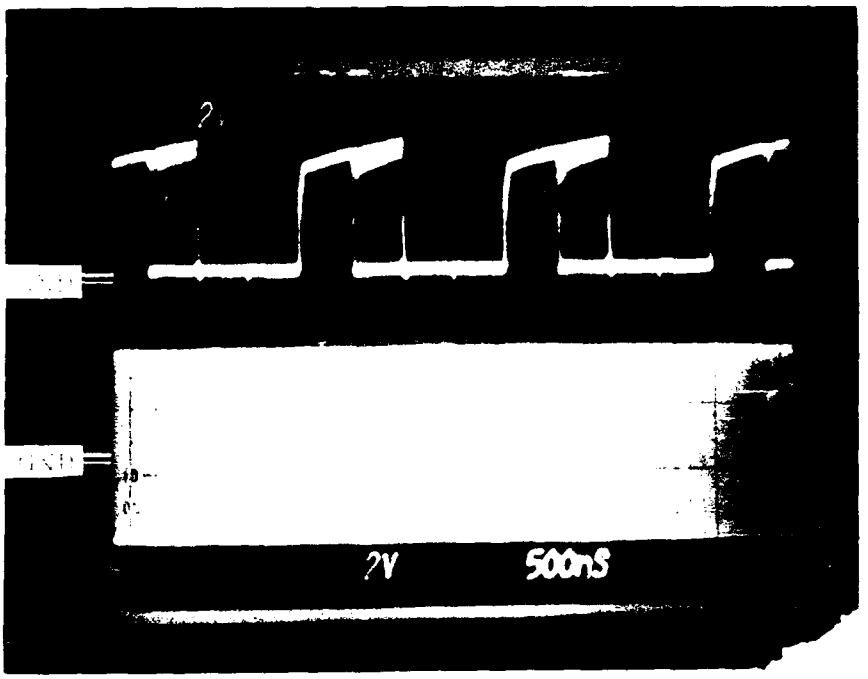


Figure 8.4.25 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Clock Input
Top trace = Q output
Bottom trace = 100 MHz RF

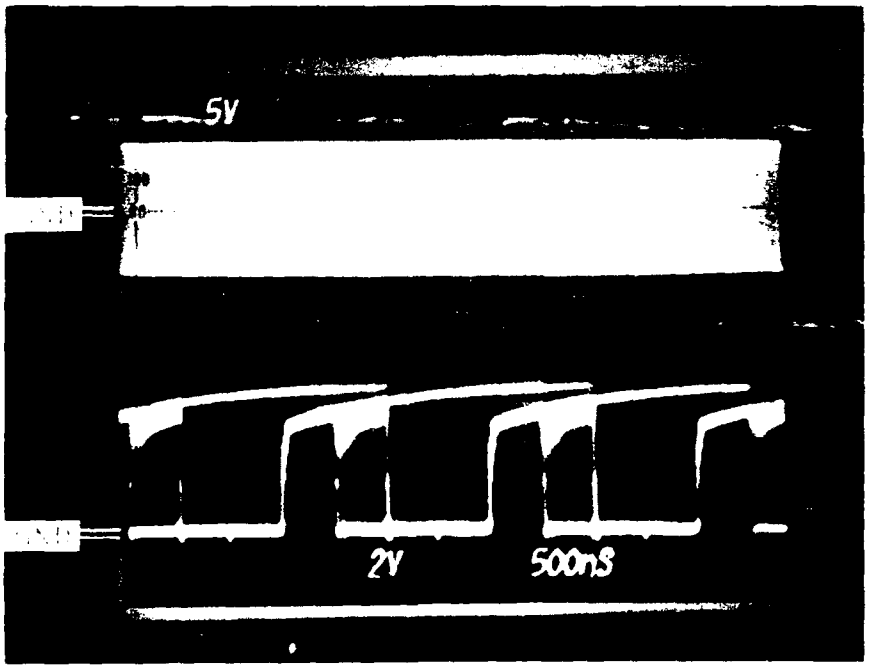


Figure 8.4.26 - SN54ALS74A RF Upset Oscilloscope Photograph
RF Interference on Clock Input
Top trace = 200 MHz RF
Bottom trace = Q output

8.5 CD4585B Upset Testing

The upset tests were performed with RF applied to the Vdd, B0 input, and B3 input pins. The RF interference was discrete CW at 1.2, 5, 10, 50, 100, and 200 MHz. All testing was performed without synchronization between the RF signal and the digital input signals. One device was tested and three different sets of test vectors (instruction sets) were used. The first and second instruction set were subsets of the third set. The first instruction set included 16 input/output combinations. Each of these 16 combinations were supplied to the DUT for two DAS9200 clock cycles as shown in Table 8.5.1.

INPUTS											OUTPUTS		
A<B	A=B	A>B	A3	A2	A1	A0	B3	B2	B1	B0	A<B	A=B	A>B
0	0	1	1	0	0	0	0	1	1	0	0	0	1
0	0	1	1	0	0	0	0	1	1	0	0	0	1
0	1	0	0	1	0	0	0	1	0	1	1	0	0
0	1	0	0	1	0	0	0	1	0	1	1	0	0
0	0	1	0	0	1	0	0	0	1	0	0	0	1
0	0	1	0	0	1	0	0	0	1	0	0	0	1
0	1	0	0	1	0	1	0	1	0	1	0	1	0
0	1	0	0	1	0	1	0	1	0	1	0	1	0
0	0	1	1	0	1	0	1	0	1	0	0	0	1
0	0	1	1	0	1	0	1	0	1	0	0	0	1
0	1	0	1	0	0	0	1	0	0	1	1	0	0
0	1	0	1	0	0	0	1	0	0	1	1	0	0
0	0	1	1	1	0	1	1	1	0	0	0	0	1
0	0	1	1	1	0	1	1	1	0	0	0	0	1
0	1	0	1	0	1	1	1	0	1	1	0	1	0
0	1	0	1	0	1	1	1	0	1	1	0	1	0
0	0	1	0	1	0	1	0	1	0	0	0	0	1
0	0	1	0	1	0	1	0	1	0	0	0	0	1
1	0	0	0	0	1	0	0	0	1	1	1	0	0
1	0	0	0	0	1	0	0	0	1	1	1	0	0
0	0	1	1	0	0	1	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0	1	0	0	0	0	1
0	1	0	0	0	1	1	0	0	1	1	0	1	0
0	1	0	0	0	1	1	0	0	1	1	0	1	0
0	0	1	1	0	1	1	1	0	1	0	0	0	1
0	0	1	1	0	1	1	1	0	1	0	0	0	1
1	0	0	0	1	0	1	1	0	0	1	1	0	0
1	0	0	0	1	0	1	1	0	0	1	1	0	0
0	0	1	1	0	1	1	1	0	1	0	0	0	1
0	0	1	1	0	1	1	1	0	1	0	0	0	1
0	1	0	1	0	1	1	1	0	1	1	0	1	0
0	1	0	1	0	1	1	1	0	1	1	0	1	0

Table 8.5.1 - Comparator Instruction Set 1

Logic low levels are indicated with a "0" and logic high levels are indicated with a "1".

It should be noted that the same instruction set is used for both the CD4585B and the SN54LS85 comparators. The logic level in Table 8.5.1 for the A>B cascade input is valid only for the SN54LS85. For the CD4585B, the A>B cascade input was always at a logic high level as required for correct operation.

The test vectors (input pin values for a given line) for instruction set one were chosen to provide a number of different combinations and to provide output logic level change sequences that could be easily monitored with an oscilloscope. Each of the three output pins changed in a repetitive manner. Evaluation of these test vectors indicated that they did not test for all possible output conditions which could be upset.

The second set of test vectors included 24 input combinations (each repeated twice as in instruction set 1). All expected upsettable output conditions were included and the repetitive sequence of output level changes were maintained. These are shown in Table 8.5.2. Again it should be noted that the A>B cascade input was always at a logic high level for the CD4585B.

There were many possible input combinations that were not tested in instruction set 1 or 2. The third instruction set included all possible input combinations. For the third set, the cascade inputs were in their three possible states, 001, 010, or 100 for A<B, A=B, or A>B respectively, while the A and B words were incremented from 0000 and 0000 to 1111 and 1111. This produced a total of 768 test vectors, i.e., 3 cascade input combinations times 2^8 possible values for words A and B. The values of the output pins for each test vector were as provided in Table 6.3.2. This test was performed to assure that the most sensitive test vector was included.

INPUTS											OUTPUTS		
A<B	A=B	A>B	A3	A2	A1	A0	B3	B2	B1	B0	A<B	A=B	A>B
0	0	1	0	0	1	0	0	0	1	0	0	0	1
0	0	1	0	0	1	0	0	0	1	0	0	0	1
0	0	1	0	1	0	0	0	1	0	0	0	0	1
0	0	1	0	1	0	0	0	1	0	0	0	0	1
0	1	0	0	0	1	0	0	0	1	0	0	1	0
0	1	0	0	0	1	0	0	0	1	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0	0	1	0
0	1	0	1	0	1	1	1	0	1	1	0	1	0
0	1	0	1	0	1	1	1	0	1	1	0	1	0
0	1	0	1	1	0	1	1	1	0	1	0	1	0
0	1	0	1	1	0	1	1	1	0	1	0	1	0
0	0	1	1	0	1	0	1	0	1	1	1	0	0
0	0	1	1	0	1	0	1	0	1	1	1	0	0
0	0	1	1	1	0	0	1	1	0	1	1	0	0
0	0	1	1	1	0	0	1	1	0	1	1	0	0
0	1	0	0	0	1	1	0	0	1	0	0	0	1
0	1	0	0	0	1	1	0	0	1	0	0	0	1
0	1	0	0	1	0	1	0	1	0	0	0	0	1
0	1	0	0	1	0	1	0	1	0	0	0	0	1
0	1	0	0	0	1	0	0	0	1	0	0	1	0
0	1	0	0	0	1	0	0	0	1	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0	0	1	0
0	1	0	1	0	1	1	1	0	1	1	0	1	0
0	1	0	1	0	1	1	1	0	1	1	0	1	0
0	1	0	1	1	0	1	1	1	0	1	0	1	0
0	1	0	1	1	0	1	1	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0	1	1	1	0	0
0	1	0	1	0	1	0	1	0	1	1	1	0	0
0	1	0	1	1	0	0	1	1	0	1	1	0	0
0	1	0	1	1	0	0	1	1	0	1	1	0	0
1	0	0	0	0	1	1	0	0	1	0	0	0	1
1	0	0	0	0	1	1	0	0	1	0	0	0	1
1	0	0	0	1	0	1	0	1	0	0	0	0	1
1	0	0	0	1	0	1	0	1	0	0	0	0	1
0	1	0	0	0	1	0	0	0	1	0	0	1	0
0	1	0	0	0	1	0	0	0	1	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0	0	1	0
0	1	0	1	0	1	1	1	0	1	1	0	1	0
0	1	0	1	0	1	1	1	0	1	1	0	1	0
0	1	0	1	1	0	1	1	1	0	1	0	1	0
0	1	0	1	1	0	1	1	1	0	1	0	1	0
1	0	0	1	0	1	0	1	0	1	1	1	0	0
1	0	0	1	0	1	0	1	0	1	1	1	0	0
1	0	0	1	1	0	0	1	1	0	1	1	0	0
1	0	0	1	1	0	0	1	1	0	1	1	0	0

Table 8.5.2 - Comparator Instruction Set 2

The complex input impedance of the Vdd, B0 input, and B3 input pins were measured with respect to the Vss pin at each of the RF test frequencies. The measured values along with the computed values for the real (R) and imaginary (X) parts of the complex input impedance are given in Table 8.5.3.

		Pin 16, Vdd		
Freq(MHz)	|Z|(ohms)	Theta(deg)	R(ohms)	X(ohms)
1.2	1100	-80	191	1083
5.0	28[illegible]	-81	45	283
10.0	150	-79	29	147
50.0	27	-62	13	24
100.0	11	20	10	4
200.0	39	72	12	37

		Pin 11, B0		
Freq(MHz)	|Z|(ohms)	Theta(deg)	R(ohms)	X(ohms)
1.2	22000	-89	384	21997
5.0	5400	-89	94	5399
10.0	2700	-87	141	2696
50.0	572	-83	70	568
100.0	298	-79	57	292
200.0	158	-74	44	152

		Pin 14, B3		
Freq(MHz)	|Z|(ohms)	Theta(deg)	R(ohms)	X(ohms)
1.2	24000	-89	419	23996
5.0	6000	-89	105	5999
10.0	2900	-89	51	2900
50.0	613	-85	53	611
100.0	311	-82	43	308
200.0	159	-77	36	155

Table 8.5.3 - CD4585B Complex Input Impedance Measurements

The values for the real and imaginary portions of the complex impedance are used in Equation 1 in the form of conductance. Figure 8.5.1 displays input conductance versus frequency for Vdd, B0 input, and B3 input pins.

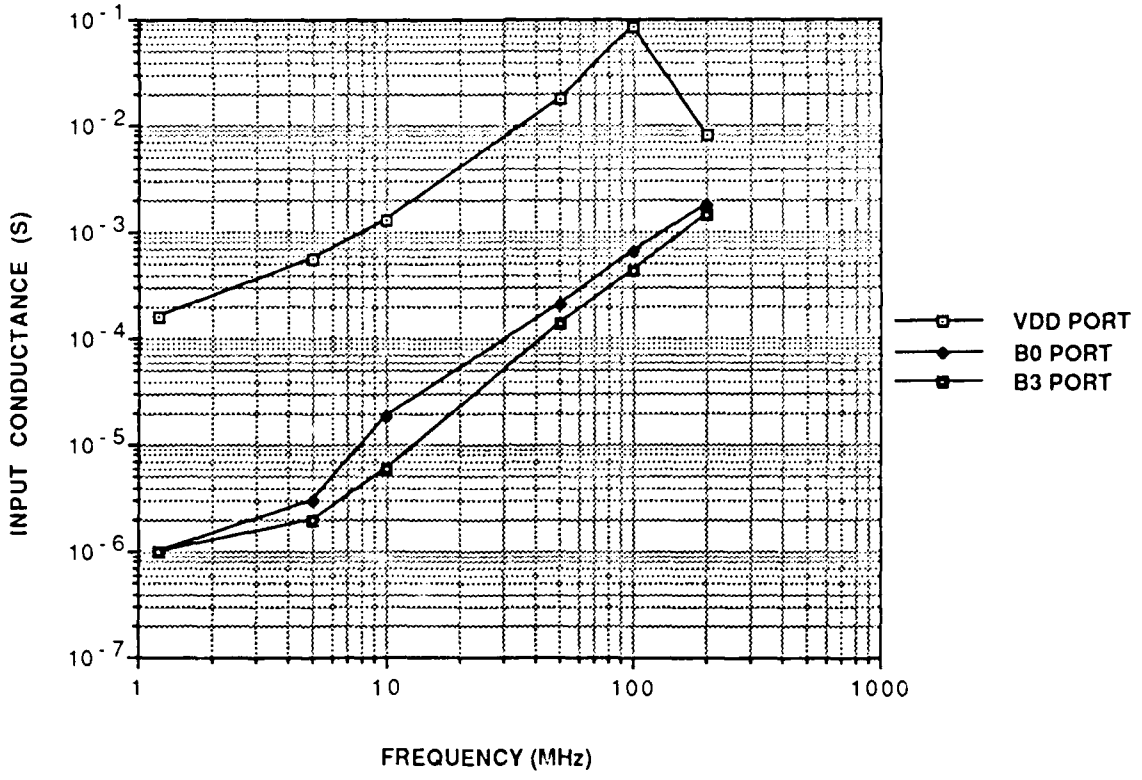


Figure 8.5.1 - CD4585B Input Conductance Versus Frequency

The peak-to-peak upset voltage levels are provided in Table 8.5.4. The voltage readings in the three columns are for instruction set 1 (I.S.1), instruction set 2 (I.S.2), and instruction set 3 (I.S.3).

	Pin 16, Vdd		
Freq(MHz)	I.S.1(V)	I.S.2(V)	I.S.3(V)
1.2	3.0	2.5	4.4
5.0	9.4	9.2	10.0
10.0	10.0	10.0	9.2
50.0	4.0	4.4	4.4
100.0	*	*	*
200.0	*	*	*

	Pin 11, B0		
Freq(MHz)	I.S.1(V)	I.S.2(V)	I.S.3(V)
1.2	2.8	3.0	3.4
5.0	5.6	5.6	8.0
10.0	6.4	8.4	9.2
50.0	*	*	*
100.0	*	*	*
200.0	*	*	*

	Pin 14, B3		
Freq(MHz)	I.S.1(V)	I.S.2(V)	I.S.3(V)
1.2	2.9	2.9	3.6
5.0	5.6	5.6	6.2
10.0	6.4	8.4	9.2
50.0	*	*	*
100.0	*	*	*
200.0	*	*	*

* = Upset not acheived

Table 8.5.4 - CD4585B Upset Voltage Levels For Instruction Sets (I.S.) 1, 2, and 3

The voltages in Table 8.5.4 and the input conductance values are inserted into Equation 1 to calculate average upset power. The resulting graphs, plotted as dBm versus frequency, are given in Figures 8.5.2 - 8.5.4.

When the first and second instruction sets were used, the least-significant bit was switching at a rate of 500 kHz. During these two sets, output levels detected at the time of failure with the DAS9200 were different than expected. For example, all outputs would be low at a given time rather than simply the wrong output being high. For the third run the operating frequency was decreased to 250 kHz to assure that the part was not being operated at too high of a data rate. The result of the decrease in operating frequency was a slight increase in the voltage levels required for upset.

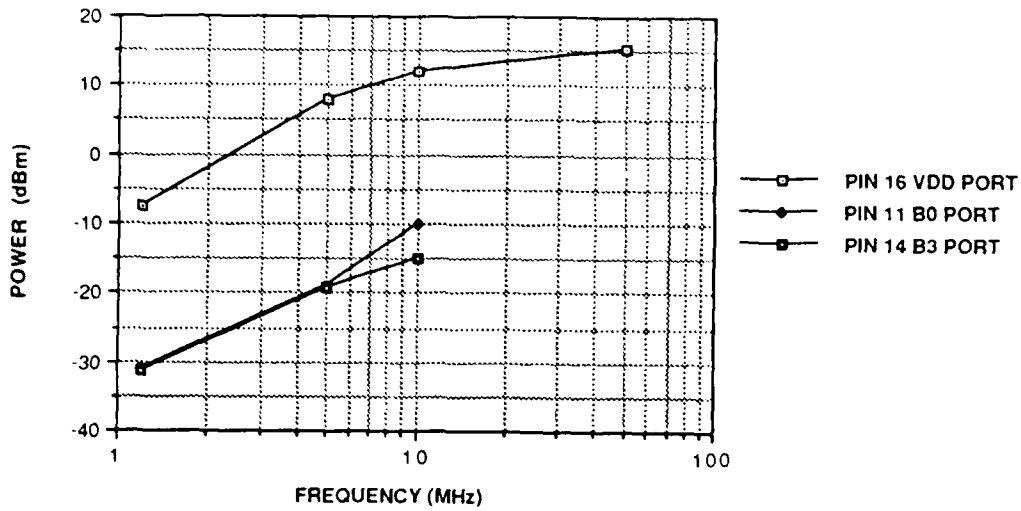


Figure 8.5.2 - CD4585B Upset Power Versus Frequency Instruction Set 1

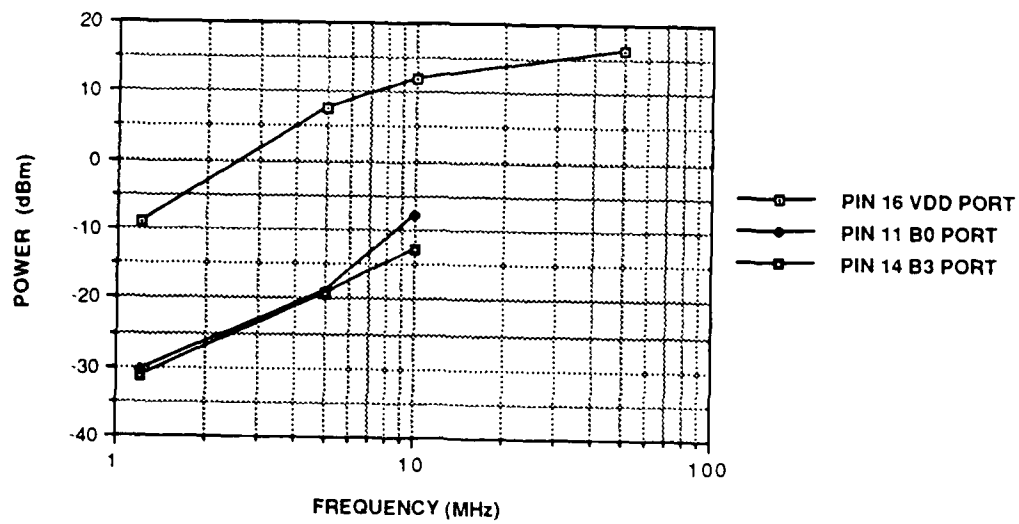


Figure 8.5.3 - CD4585B Upset Power Versus Frequency Instruction Set 2

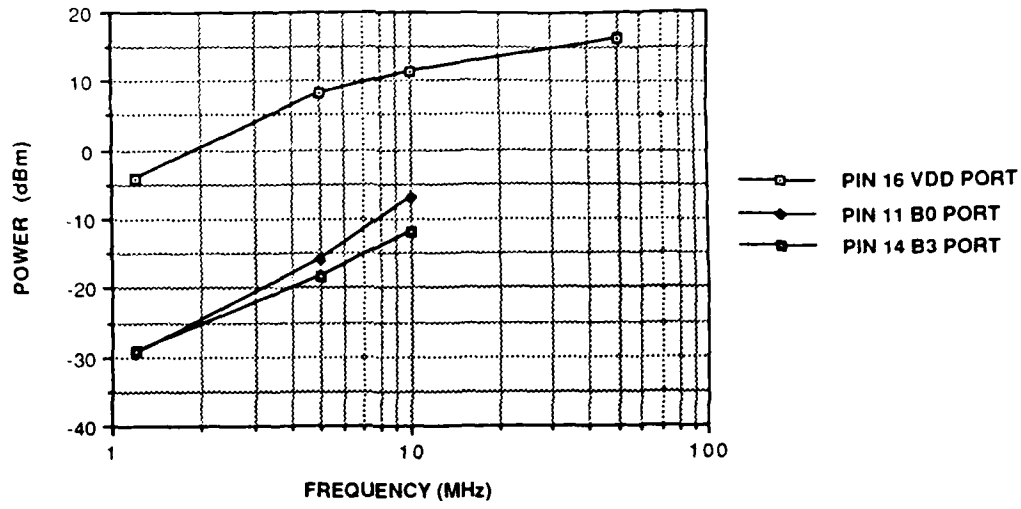


Figure 8.5.4 - CD4585B Upset Power Versus Frequency Instruction Set 3

The waveforms, as they appear on the osciloscope, were photographed at the point where the DAS9200 system detected a failure. The A>B output was monitored. Due to the similarity of the appearance of the output waveforms for a number of input conditions, only a limited number of photographs were taken. Waveforms of the failures that occurred with RF interference on Vdd, are shown in Figures 8.5.5 - 8.5.7 at 1.2, 5, and 50 MHz. The appearance at 10 MHz was similar to the 5 MHz waveform. Waveforms of the failures that occurred with RF interference on the B0 input are shown in Figures 8.5.8 and 8.5.9 at 1.2 and 5 MHz. The appearance at 10 MHz was similar to the 5 MHz waveform. The appearance of the output waveforms with RFI on the B3 input were similar to the output waveforms with RFI on the B0 input.

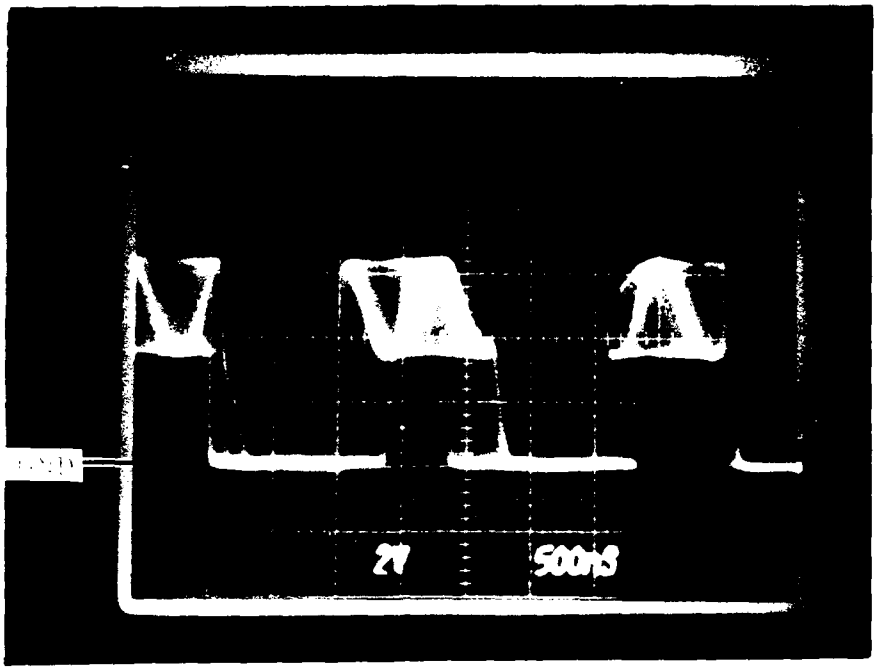


Figure 8.5.5 - CD4585B RF Upset Oscilloscope Photograpn
RF Interference at 1.2 MHz on Vdd
Trace = A>B output

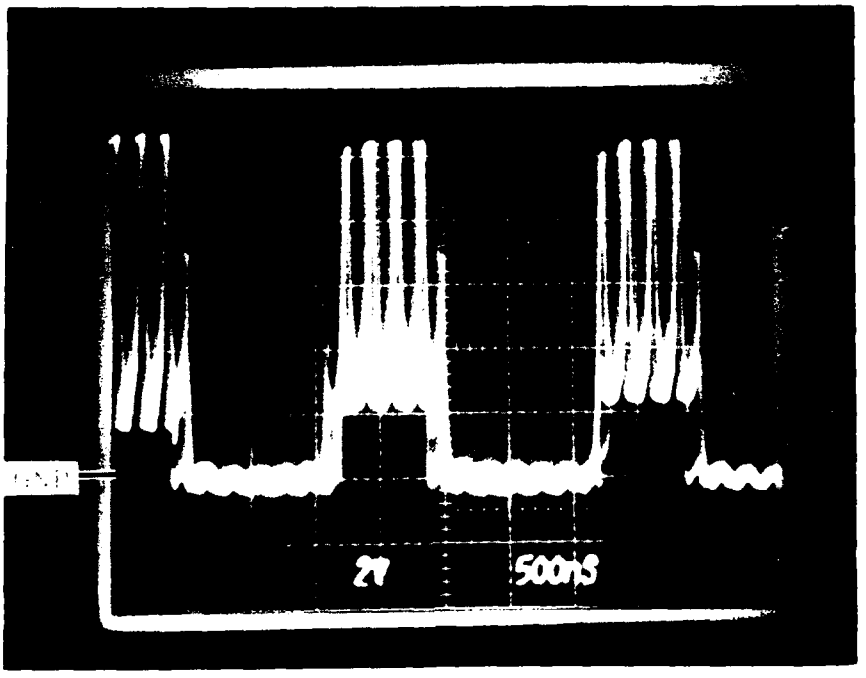


Figure 8.5.6 - CD4585B RF Upset Oscilloscope Photograph
RF Interference at 5 MHz on Vdd
Trace = A>B output

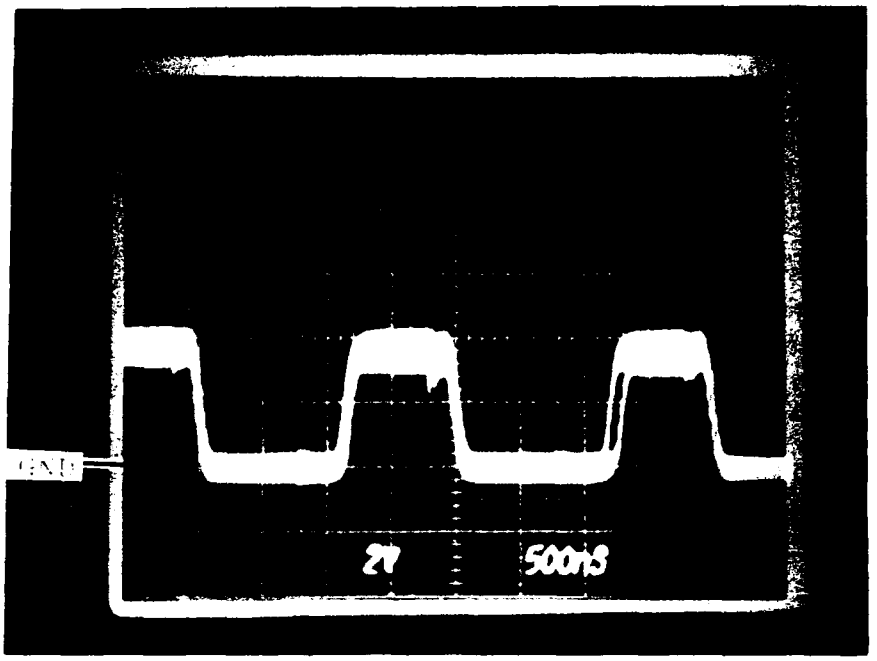


Figure 8.5.7 - CD4585B RF Upset Oscilloscope Photograph
RF Interference at 50 MHz on Vdd
Trace = A>B output

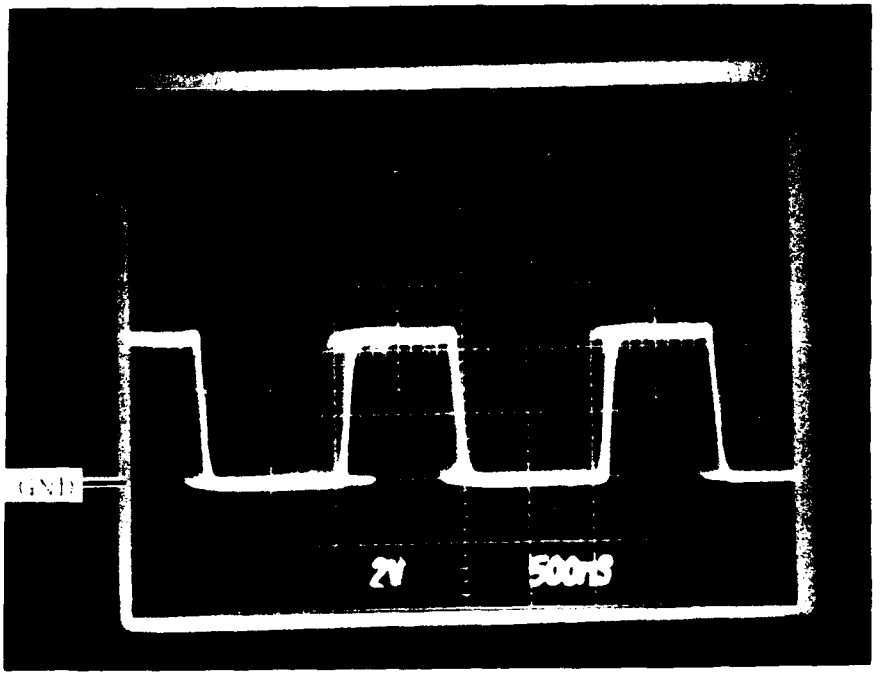


Figure 8.5.8 - CD4585B RF Upset Oscilloscope Photograph
RF Interference at 1.2 MHz on B0 Input
Trace = A>B output

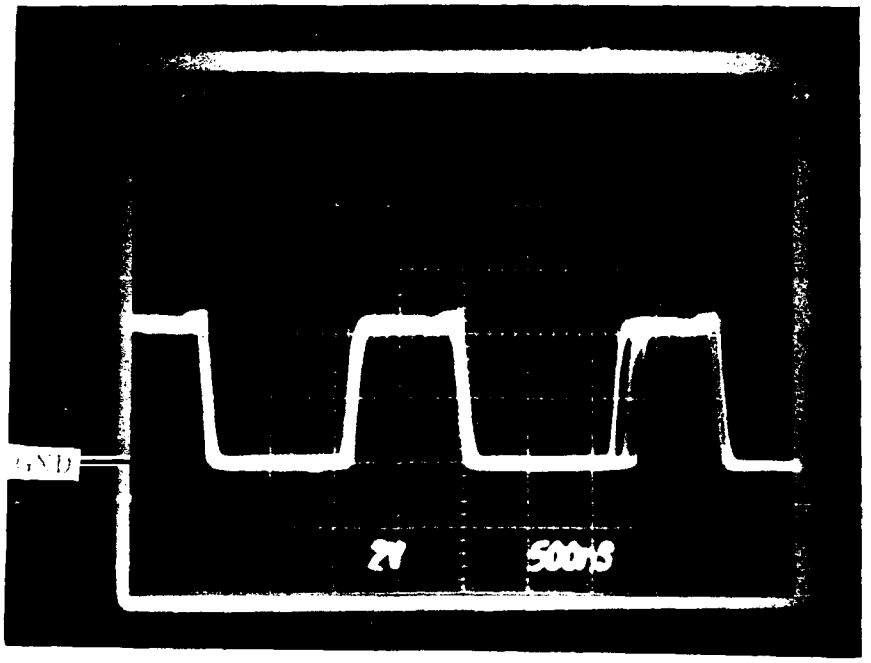


Figure 8.5.9 - CD4585B RF Upset Oscilloscope Photograph
RF Interference at 5 MHz on B0 Input
Trace = A>B output

8.6 SN54LS85 Upset Testing

The upset tests were performed with RF applied to the Vcc, B0 input, and B3 input pins. The RF interference was discrete CW at 1.2, 5, 10, 50, 100, and 200 MHz. All testing was performed without synchronization between the RF signal and the input signals. One device was tested and three different sets of test vectors were used. These were the same sets of test vectors described in the previous section.

The complex input impedance of Vcc, the clock input, and the data input were measured with respect to the ground pin at each of the RF test frequencies. The measured values along with the computed values for the real (R) and imaginary (X) parts of the complex input impedance are given in Table 8.6.1.

		Pin 16, Vcc		
Freq(MHz)	|Z|(ohms)	Theta(deg)	R(ohms)	X(ohms)
1.2	40	78	8	39
5.0	135	32	114	71
10.0	141	1	141	2
50.0	44	-60	22	38
100.0	10	-36	8	6
200.0	30	80	5	29

		Pin 9, B0		
Freq(MHz)	|Z|(ohms)	Theta(deg)	R(ohms)	X(ohms)
1.2	1400	-13	1364	315
5.0	1300	-20	1222	445
10.0	1100	-36	890	647
50.0	355	-74	98	341
100.0	176	-78	37	172
200.0	77	-76	19	75

		Pin 1, B3		
Freq(MHz)	|Z|(ohms)	Theta(deg)	R(ohms)	X(ohms)
1.2	573	21	535	205
5.0	764	4	762	48
10.0	782	-18	744	242
50.0	420	-74	116	404
100.0	207	-79	39	203
200.0	89	-78	18	87

Table 8.6.1 - SN54LS85 Complex Input Impedance Measurements

The values for the real and imaginary portions of the complex impedance are used in Equation 1 in the form of conductance. Figure 8.6.1 displays input conductance versus frequency for Vcc, B0 input, and B3 input pins.

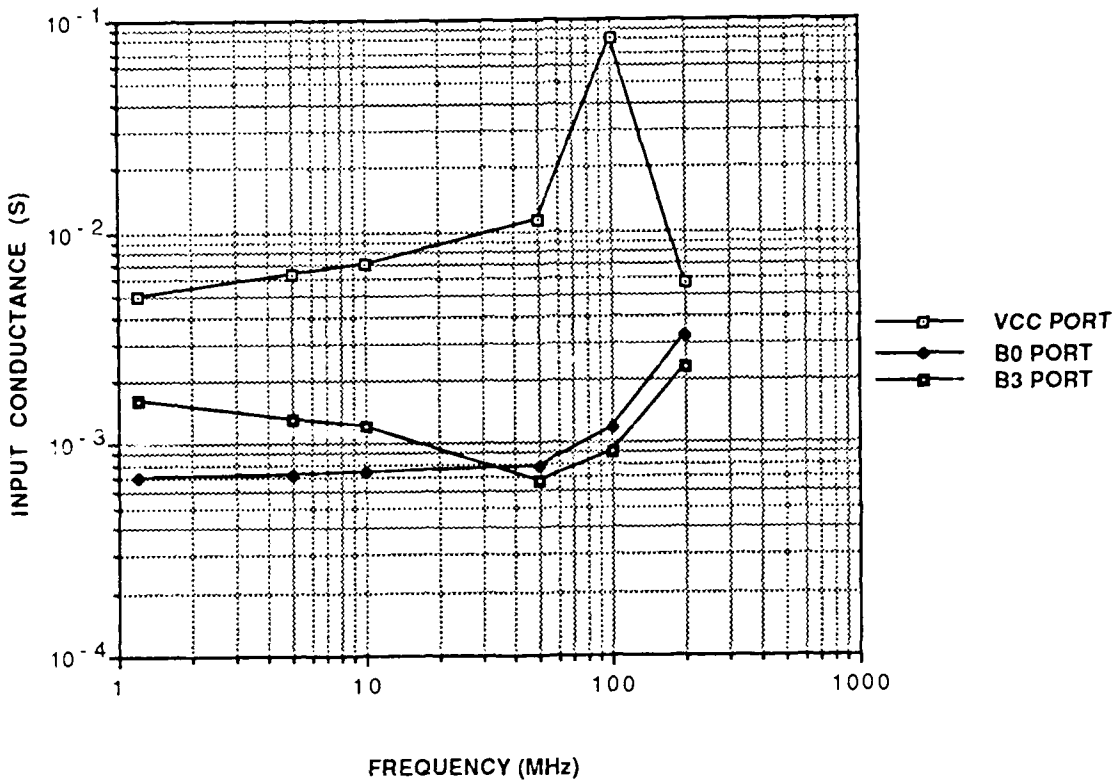


Figure 8.6.1 - SN54LS85 Input Conductance Versus Frequency

The peak-to-peak upset voltage levels are provided in Table 8.6.2.

	Pin 16, Vcc		
Freq(MHz)	I.S.1(V)	I.S.2(V)	I.S.3(V)
1.2	3.0	2.9	2.8
5.0	15.0	8.4	12.0
10.0	11.6	7.6	10.0
50.0	7.0	9.6	9.2
100.0	3.6	3.8	3.6
200.0	*	*	*

	Pin 9, B0		
Freq(MHz)	I.S.1(V)	I.S.2(V)	I.S.3(V)
1.2	1.5	1.3	1.4
5.0	7.0	4.7	5.6
10.0	7.2	4.8	5.0
50.0	2.3	2.6	2.6
100.0	5.4	4.2	3.4
200.0	1.0	1.8	1.7

	Pin 1, B3		
Freq(MHz)	I.S.1(V)	I.S.2(V)	I.S.3(V)
1.2	1.4	2.2	1.4
5.0	2.4	3.2	6.4
10.0	4.4	4.2	6.4
50.0	3.0	2.6	2.6
100.0	6.0	3.2	3.6
200.0	2.0	1.6	1.6

Table 8.6.2 - SN54LS85 Upset Voltage Levels For Instruction Sets (I.S.) 1, 2, and 3

The voltages in Table 8.6.2 and the input conductance values are inserted into Equation 1 to calculate average upset power. The resulting graphs, plotted as dBm versus frequency, are given in Figures 8.6.2 - 8.6.4. The least significant bit was changing at the rate of 1.25 MHz for each of the three runs. The only difference between the runs was the instruction set. The curves for the B0 and B3 inputs show little increase with frequency primarily due to the shape of the admittance curves. The basic shape and the approximate upset levels are similar for each of the graphs. Upset voltage levels are both higher and lower comparing between the three runs at the different RF interference frequencies, i.e., there is no indication that the instruction set used is critical for determining the upset voltage level.

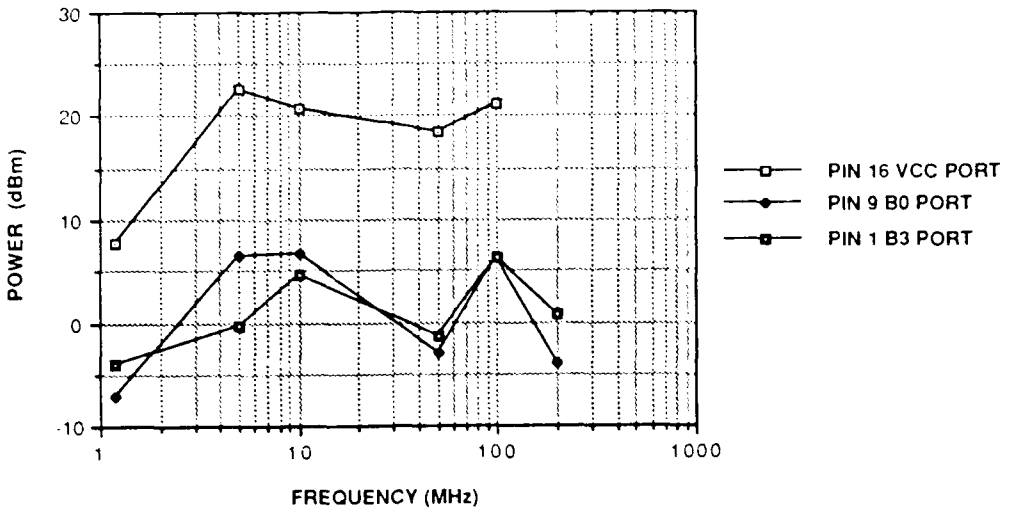


Figure 8.6.2 - SN54LS85 Upset Power Versus Frequency Instruction Set 1

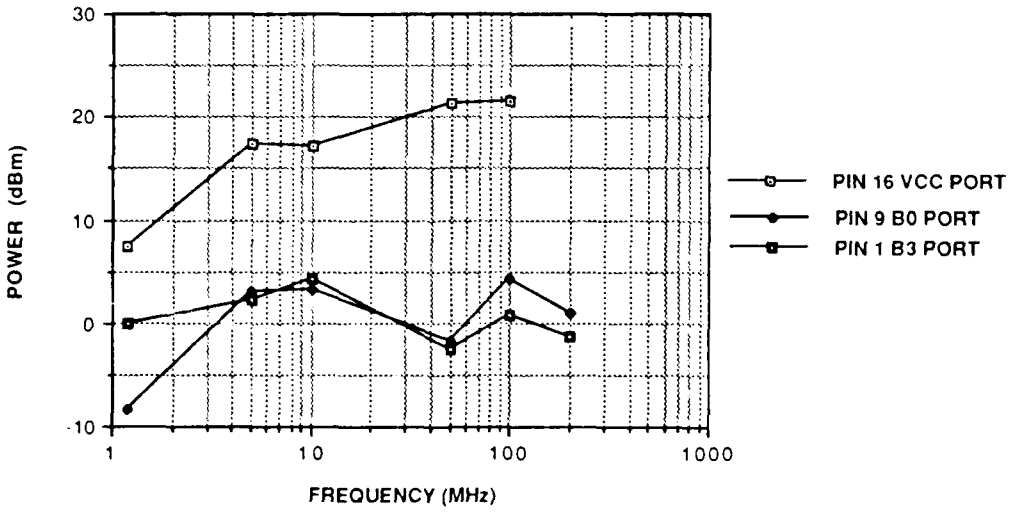


Figure 8.6.3 - SN54LS85 Upset Power Versus Frequency Instruction Set 2

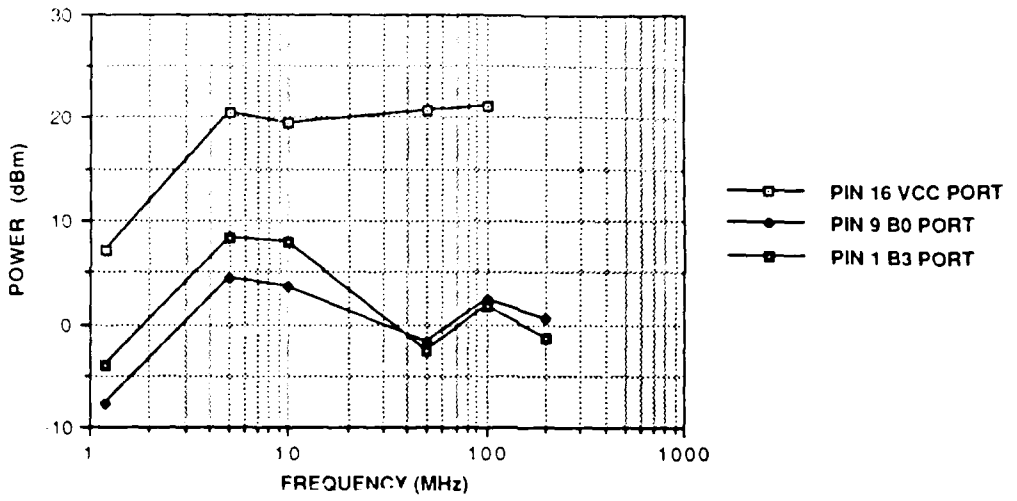


Figure 8.6.4 - SN54LS85 Upset Power Versus Frequency Instruction Set 3

The A>B output waveforms, as they appear on the oscilloscope, were photographed at the point where the DAS9200 system detected a failure. Due to the similar appearance of the output waveforms for a number of input conditions only a limited number of photographs were taken. Waveforms of the failures that occurred with RF interference on Vcc are shown in Figures 8.6.5 - 8.6.7 at 1.2, 5, and 50 MHz. The appearance at 10 MHz was similar to the 5 MHz waveform and the appearance at 100 MHz was similar to the 50 MHz appearance. Waveforms of the failures that occurred with RF interference on the B0 input are shown in Figures 8.6.8 - 8.6.12 at 1.2, 5, 10, 50, and 200 MHz. The appearance at 100 MHz was similar to the 50 MHz waveform. The appearance of the output waveforms with RFI on the B3 input were similar to the output waveforms with RFI on the B0 input.

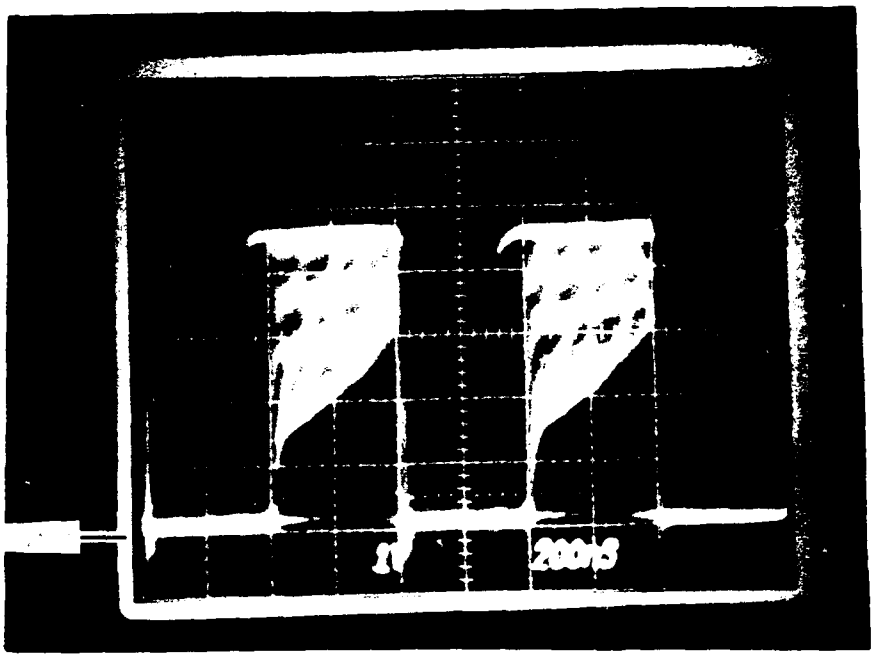


Figure 8.6.5 - SN54LS85 RF Upset Oscilloscope Photograph
RF Interference at 1.2 MHz on Vcc
Trace = A>B output

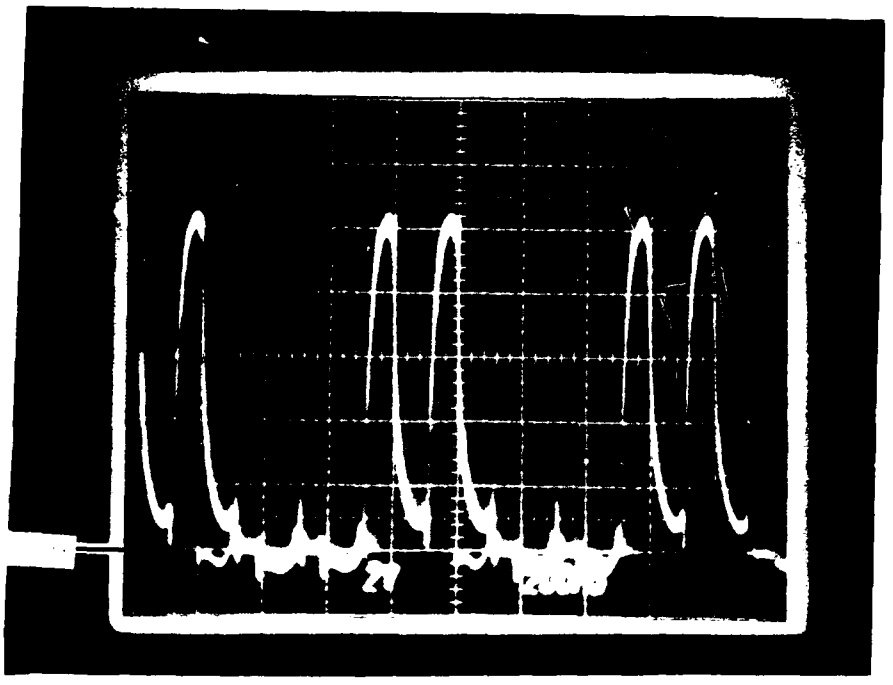


Figure 8.6.6 - SN54LS85 RF Upset Oscilloscope Photograph
RF Interference at 5 MHz on Vcc
Trace = A>B output

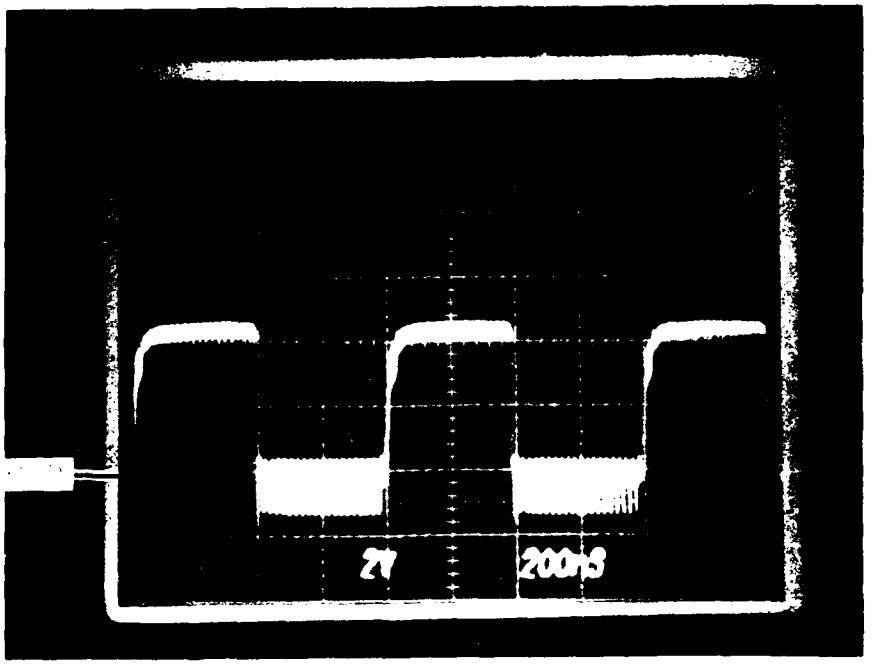


Figure 8.6.7 - SN54LS85 RF Upset Oscilloscope Photograph
RF Interference at 50 MHz on Vcc
Trace = A>B output

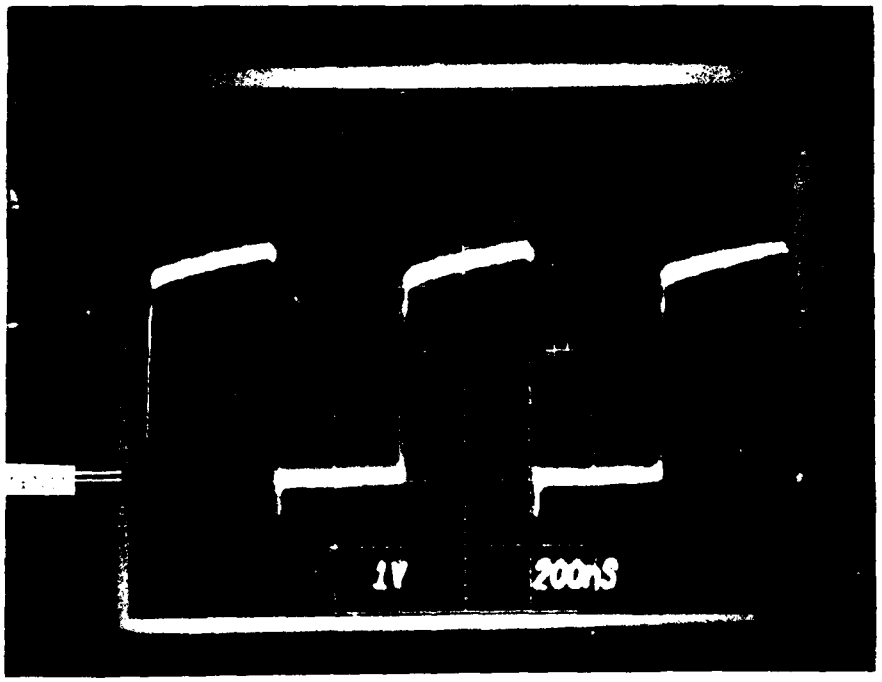


Figure 8.6.8 - SN54LS85 RF Upset Oscilloscope Photograph
RF Interference at 1.2 MHz on B0 Input
Trace = A>B output

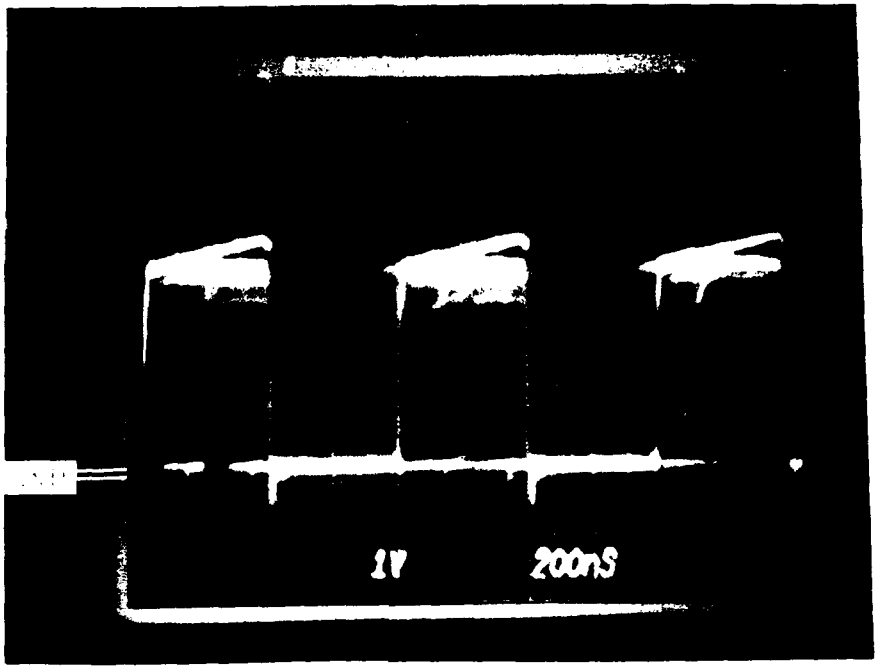


Figure 8.6.9 - SN54LS85 RF Upset Oscilloscope Photograph
RF Interference at 5 MHz on B0 Input
Trace = A>B output

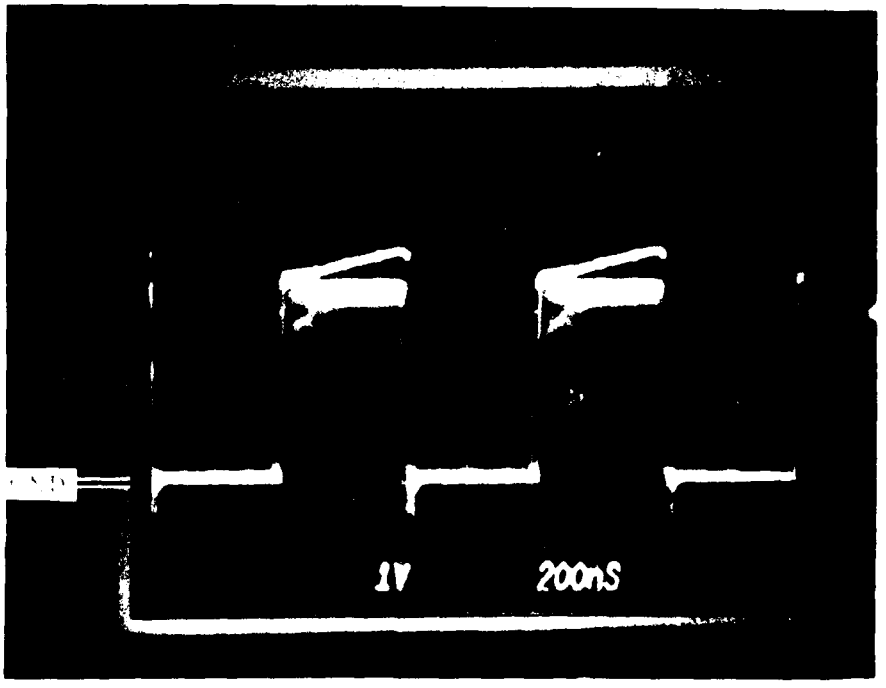


Figure 8.6.10 - SN54LS85 RF Upset Oscilloscope Photograph
RF Interference at 10 MHz on B0 Input
Trace = A>B output

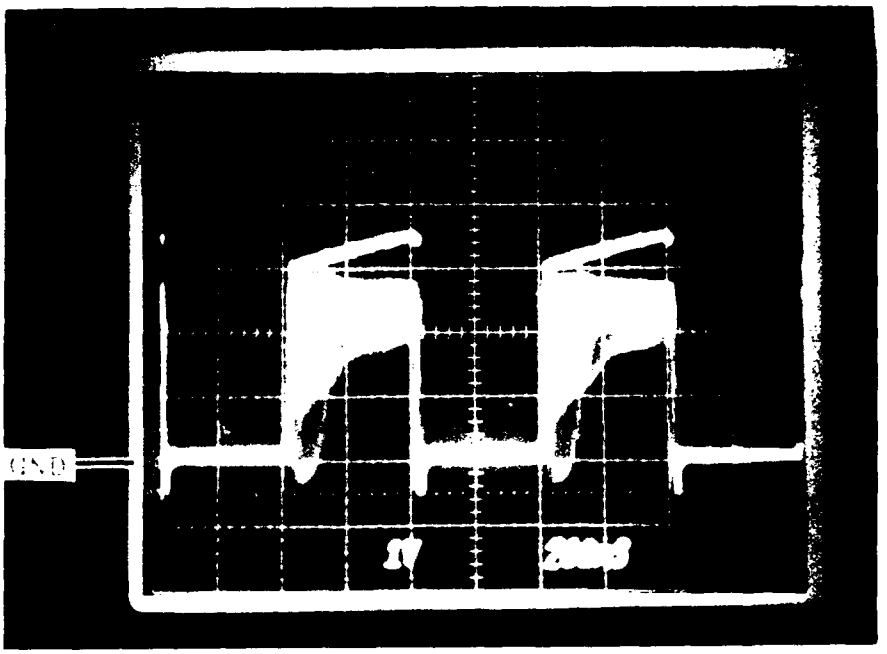


Figure 8.6.11 - SN54LS85 RF Upset Oscilloscope Photograph
RF Interference at 50 MHz on B0 Input
Trace = A>B output

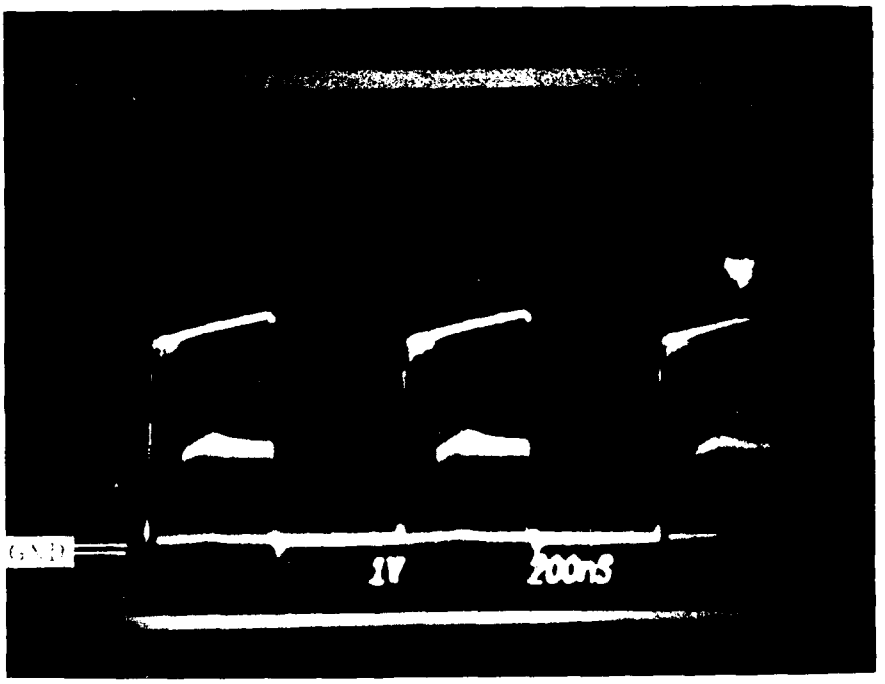


Figure 8.6.12 - SN54LS85 RF Upset Oscilloscope Photograph
RF Interference at 200 MHz on B0 Input
Trace = A>B output

8.7 Upset Susceptibilty Comparison

A comparison of the upset susceptibilities can be performed in a variety of ways between the four device types tested. Two basic technologies, Schottky and CMOS, are represented and two device functions, flip-flops (sequential logic) and comparators (combinational logic), as well as measurements on the power, clock, data, B0, and B3 inputs. These will be compared in different combinations to allow better understanding of the data.

8.7.1 Power Input Comparison

The upset levels for the Vdd and Vcc pins have been combined and plotted together to allow comparison between the four device types. Figure 8.7.1.1 shows the comparison between the peak-to-peak voltage levels. In general the parts exhibit a low voltage upset level at low frequencies which peaks at mid-frequency and then decreases at higher frequencies. The comparison between upset power levels is shown in Figure 8.7.1.2. This comparison shows that the power required for upset is relatively constant for the Schottky devices except for the lowest frequency on the SN54LS85. For the CMOS devices the power required for upset increases at a fairly constant rate up to 50 MHz.

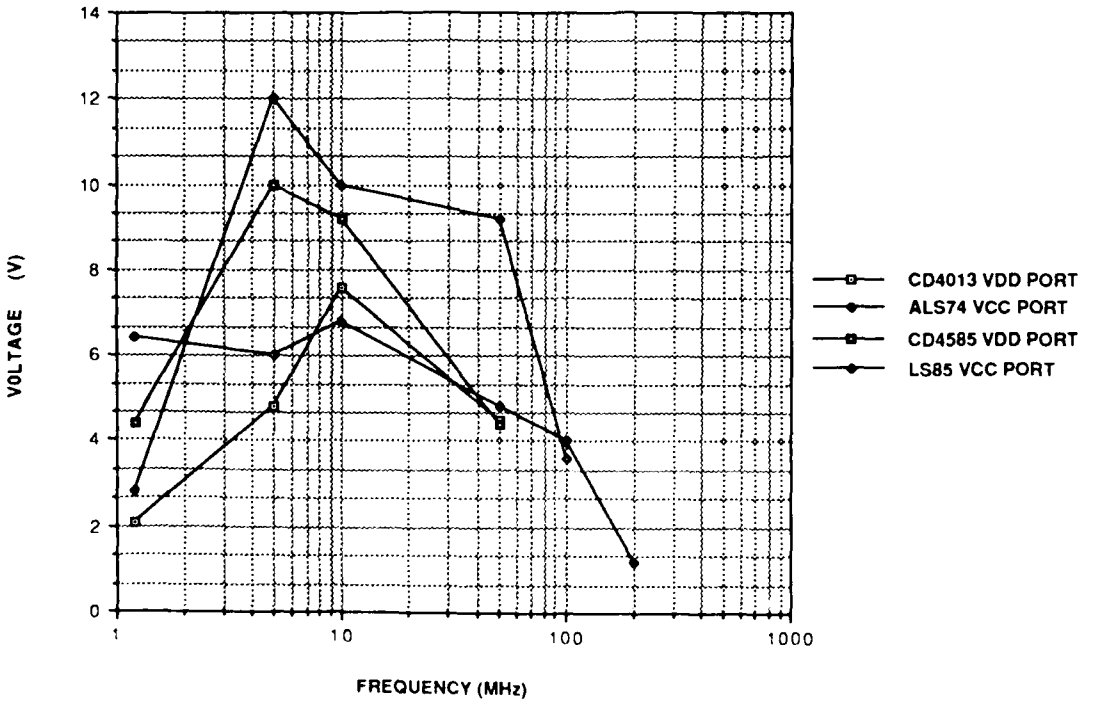


Figure 8.7.1.1 - Upset Voltage Level Comparison for Power Inputs

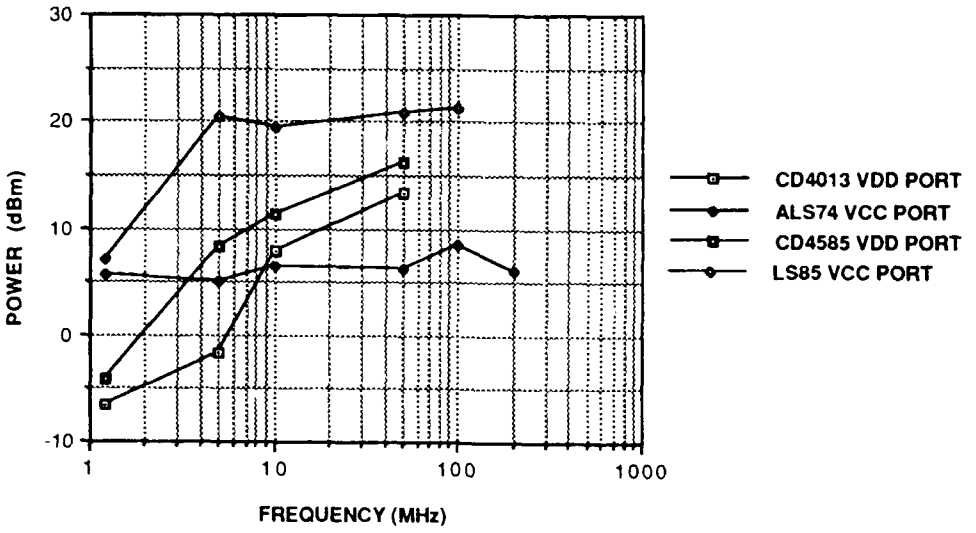


Figure 8.7.1.2 - Upset Power Level Comparison for Power Inputs

8.7.2 Data, Clock, B0, and B3 Input Comparison

Examination of the graphs from Sections 8.3 - 8.6 showing upset power levels, indicates that a limited number of inputs can be used for the comparison and the data will be representative of the complete data base.

There are a total of 8 inputs to be compared; CD4013B - data and clock inputs, SN54ALS74A - data and clock inputs, CD4585B - B0 and B3 inputs, and SN54LS85 - B0 and B3 inputs. A chart with curves of each of these eight inputs would be too crowded and difficult to interpret. Therefore, relevant comparisons will be considered and specific graphs of these will be shown. A review of the data indicates that for both of the comparator types the upset voltage and upset power for B0 and B3 are very close (reference Tables 8.5.2 and 8.6.2, and Figures 8.5.4 and 8.6.4). For the comparisons, either B0 or B3 can be used and it will properly represent the data for the other one. For the following figures, B0 is displayed. The data and clock inputs exhibit enough of a difference that both will be displayed for each technology.

A comparison of the upset voltage levels is given in Figures 8.7.2.1 and 8.7.2.2. Figure 8.7.2.1 shows the CMOS devices and Figure 8.7.2.2 shows the Schottky devices. The CMOS devices exhibit similar behavior, with increasing voltage required for upset as frequency increases. From later testing, it appears that this is primarily due to the attenuation of the voltage level in the input protection circuit (Reference Section 9.) The response of the Schottky devices is different than that of the CMOS devices. The data and B0 inputs resemble the power pin voltage response. The clock input on the SN54ALS74A has a relatively constant voltage upset level of 1 to 2 volts peak-to-peak over the entire frequency range. The clock circuitry sets the internal states of the transistor on the rising edge. This edge triggering combined with the fact that there is no series protection circuit resistor, such as on the clock input for the CMOS device, produces this high RF upset susceptibility.

The same combinations as displayed in Figures 8.7.2.1 and 8.7.2.2 are shown in Figures 8.7.2.3 and 8.7.2.4 as dBm versus frequency. The CMOS dBm curves in Figure 8.7.2.3 are even more tightly grouped than the voltage curves. This indicates that the circuit function is secondary to the technology effect. The CMOS devices with their input protect circuitry have a fairly constant decrease in susceptibility with increasing frequency. The Schottky data in Figure 8.7.2.4 show a significant difference between the power levels required for upset between the two device types. This is due to the conductance difference of the inputs (reference Figures 8.4.1 and 8.6.1). The conductance of the inputs on the SN54LS85 are higher than the SN54ALS74A. In fact, from Figures 8.3.1, 8.4.1, and 8.5.1 the ALS device conductance is more comparable to the CMOS conductance.

As given in Appendix A.1, the specified current for a low condition on the inputs of the ALS device is -200 uA while it is -1200 uA for the LS device. The specified current for a high condition on the inputs of the ALS device is 20 uA while it is 60 uA for the LS device. These numbers directly relate to the power required for upset. More current is required to operate the LS device than the ALS device and consequently, more power is required for upset on the LS device.

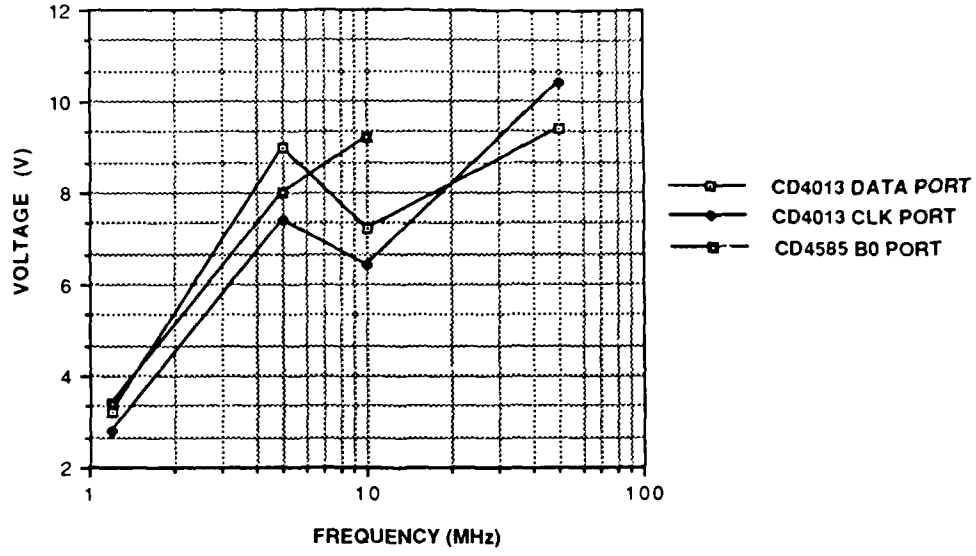


Figure 8.7.2.1 - CMOS Technology Upset Voltage Levels

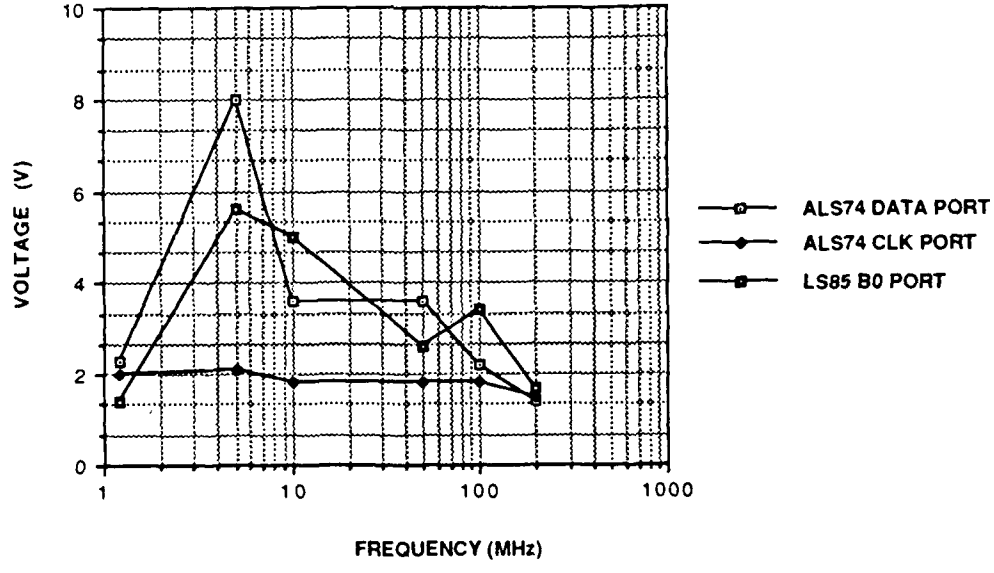


Figure 8.7.2.2 - Schottky Technology Upset Voltage Levels

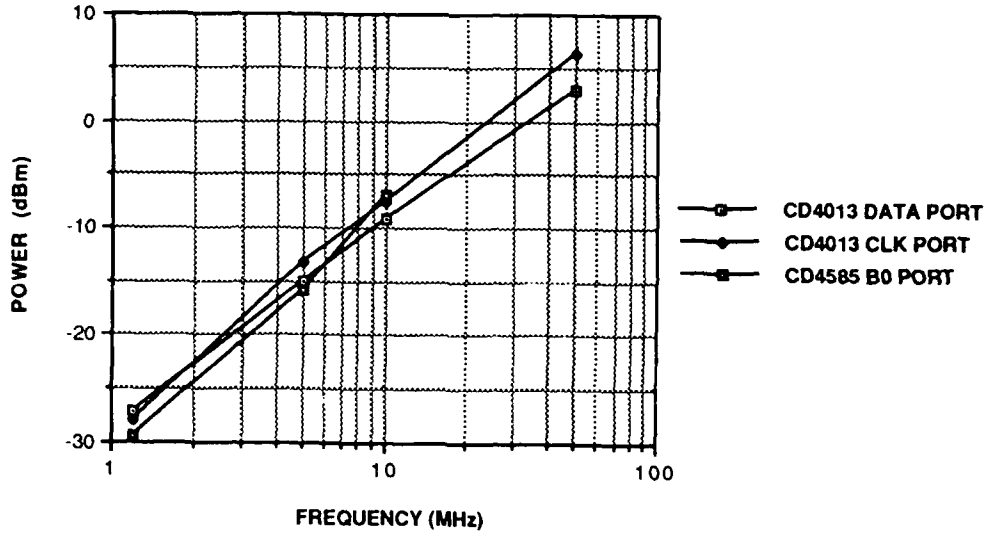


Figure 8.7.2.3 - CMOS Technology Upset Power Levels

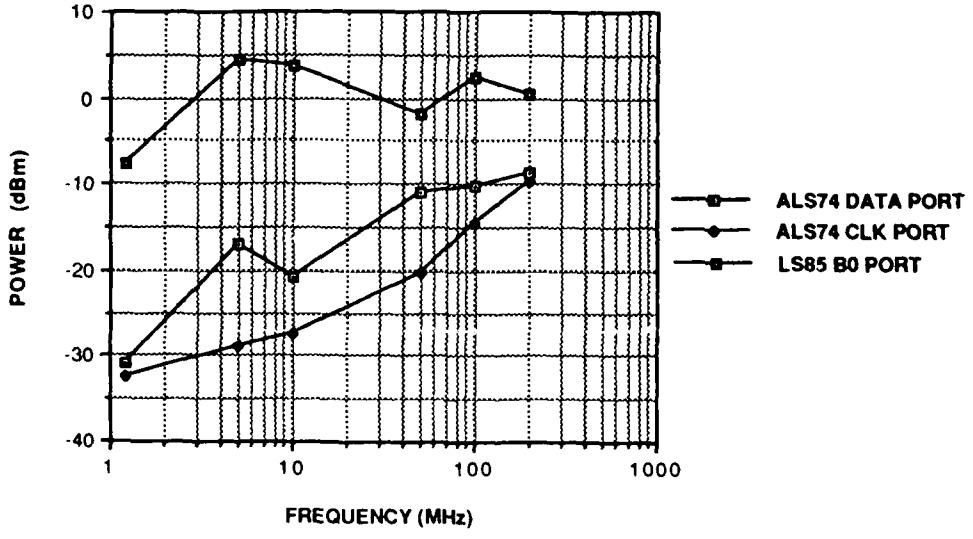


Figure 8.7.2.4 - Schottky Technology Upset Power Levels

8.7.3 Technology Comparison

A comparison between the upset voltage levels for the CMOS and Schottky devices' inputs is provided in Figure 8.7.3.1. This is a combination of Figures 8.7.2.1 and 8.7.2.2. A comparison between the same inputs showing upset power versus frequency is provided in Figure 8.7.3.2. Since all three of the CMOS curves are tightly grouped, two of the curves have been eliminated in Figure 8.7.3.3 for ease of viewing.

Below 10 MHz, the ALS device is the most susceptible to upset followed by the CMOS device and then the LS device. At 50 MHz and above the CMOS device becomes the least susceptible due to the attenuation of the RFI by the input protect circuitry. The relatively flat appearance of the curve for the LS input is due to the same appearance of the conductance (Figure 8.4.1). Above 100 MHz the conductance in Figure 8.4.1 is increasing, indicating that the slope of the susceptibility curve will increase and likely be similar to the CMOS or ALS curve slopes.

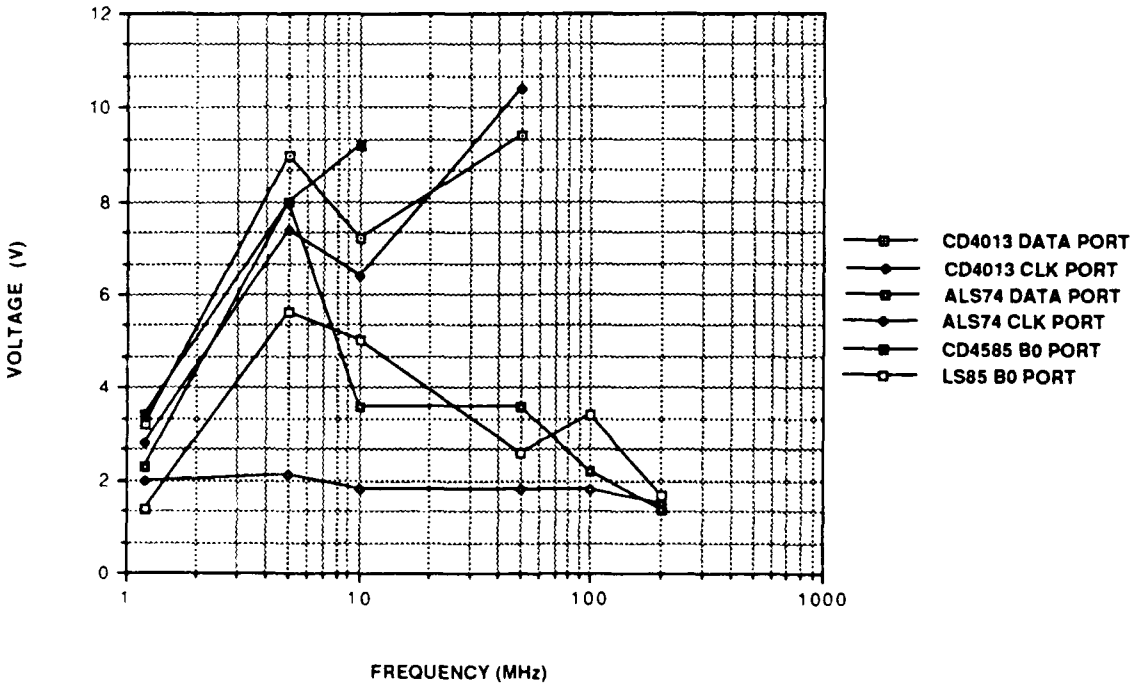


Figure 8.7.3.1 - CMOS and Schottky Upset Voltage Comparison for Inputs

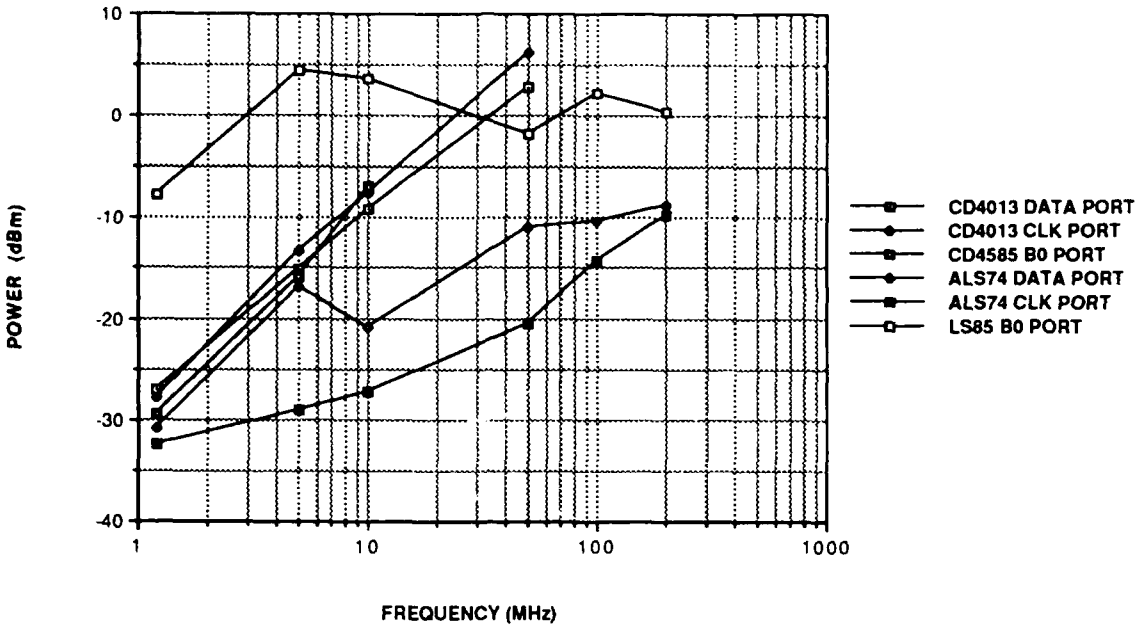


Figure 8.7.3.2 - CMOS and Schottky Upset Power Comparison for Inputs

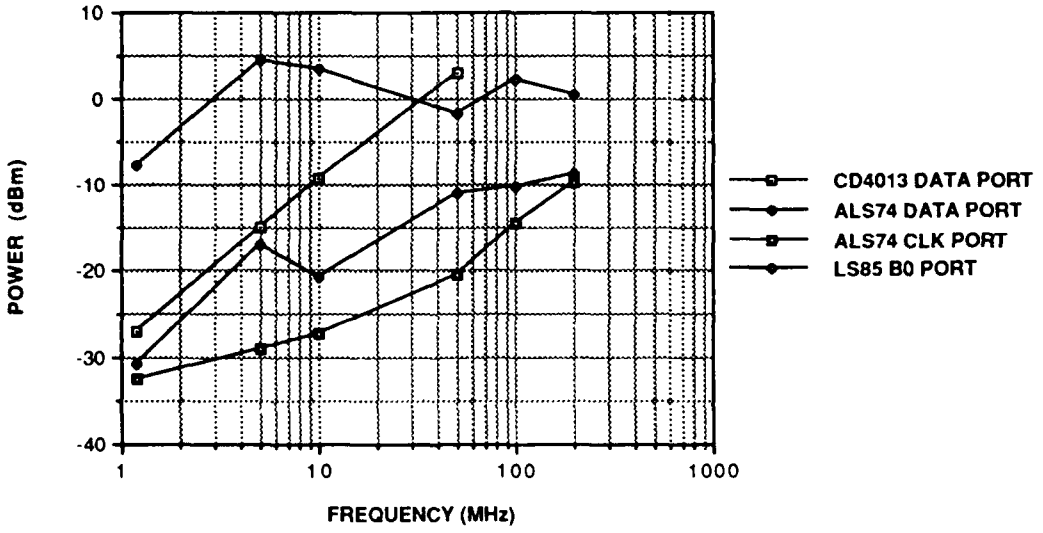


Figure 8.7.3.3 - Upset Power Comparson for One CMOS and Three Schottky Inputs

9.0 SEM QUANTITATIVE VOLTAGE CONTRAST MEASUREMENTS

Measurements were performed on the scanning electron microscope utilizing an energy spectrometer to perform quantitative measurement of the voltages present on the integrated circuit surface. Three of the four previously tested parts were measured in this system. Due to time limitations the fourth part was not measured. A discussion of quantitative voltage contrast, the QVC system used for this study, and the results of the measurements will be given in this section. Daniel Koellen published an article [9] discussing the details of the QVC system utilized for this study. Sections 9.1 and 9.2 contain information that has been extracted from that article. Most of the information has been copied directly with the remainder being modified to correspond to the configuration used in this test.

9.1 Quantitative Voltage Contrast

When a metallization trace within an IC is bombarded by the electron beam of a SEM, low energy secondary electrons are produced. For aluminum, the range of secondary electron kinetic energy is between 1 and 15 eV [10], they are easily influenced by nearby electric fields. Thus, a potential on the bombarded conductor will influence the secondary electron intensity and energy distribution.

The potential of the conductor modifies the potential barrier the secondary electrons must overcome at the surface of the conductor before they are emitted. A positive potential increases the barrier permitting fewer electrons to be emitted while a negative potential lowers the barrier and permits a greater number of electrons to be emitted. This intensity modulation is utilized for qualitative voltage contrast imaging of voltage levels, often used for determining logic states or trace continuity. Since this effect is non-linear it is not used for quantitative voltage measurements [10-12].

The energy distribution of the secondary electrons is also modified by a potential present on a bombarded metallization trace. The energy distribution is shifted by an amount proportional to the potential on the trace. For example, a potential of five volts will shift the energy distribution by five electron-volts [10,12,13]. The potential on a trace is measured by detecting the shift in the energy distribution using an electron energy spectrometer. A voltage-time waveform is constructed through a sampling technique in which the electron beam of the SEM is pulsed on synchronous with the device's clock or operating signals. Voltage measurements are made in specific time increments and the waveform is reconstructed from this collection of voltage measurements. The measured waveform must be repetitive as in any sampling scheme.

9.2 Scanning Electron Microscope QVC System

A Cambridge Stereoscan 180 SEM was modified for QVC measurements. The electron source and column, specimen chamber, vacuum system and the SEM control electronics were retained and utilized for the QVC SEM system. Instrumentation designed and built specifically for QVC applications includes the electron spectrometer for electron energy analysis, the beam blanker to pulse the electron beam on, the interface for functional signals from the exerciser to the DUT socket in the SEM chamber and the linearization (feedback) unit which quantifies the voltage measurements.

The "E-beam Tester Interface" shown in Figure 7.5.1 consists of a boxcar averager, a linearization circuit, and a beam blanker pulse generator. The boxcar averager is a commercial unit that provides sample and hold for the linearization unit, variable delay for the beam blanker, signal averaging and waveform reconstruction.

The electron spectrometer measures the energy of the secondary electrons emitted from the sample. From this, the shift in the secondary electron energy distribution is derived. An electron spectrometer must meet the following criteria [14]: 1) reduce the effect of local retarding fields at the IC surface, 2) determine the secondary electron energy distribution, and 3) suppress backscattered and tertiary electrons produced within the spectrometer.

In addition, the electron spectrometer designed for this system needed to satisfy the following conditions: 1) good linearity, 2) high transmission, 3) low profile for short working distance, 4) voltage range of +/-15 volts, 5) easy alignment, 6) serviceability and 7) reliable operation.

A diagram of the electron spectrometer built for this system is shown in Figure 9.2.1. The secondary electrons enter the spectrometer at the the bottom through the extraction grid and, if they have sufficient energy, travel through the retarding grid and are deflected to the right towards the scintillator. The scintillator and the signal processing electronics of the SEM were maintained.

The extraction grid produces a large field normal to the surface of the IC that accelerates the secondary electrons to the spectrometer and reduces the effect of local retarding fields from nearby traces. The potential on the extraction grid can vary from 0 to 2000 volts with 1000 volts normally applied, giving a field of 500 V/mm at the IC surface.

The retarding (or filter) grid produces a barrier in which only electrons of sufficient kinetic energy can traverse. The electron spectrometer may be thought of as an electron filter that permits transmission of electrons with a kinetic energy greater than the value determined by the retarding grid potential. The detector current is then proportional to the integral of the portion of the electron energy distribution greater than the retarded energy.

The deflection electrode and grid guide the filtered electrons toward the detector. The shield electrode reduces the influence of the extraction field on the filtered electrons.

The suppression grid prevents backscattered electrons and tertiary electrons generated at the top plate from reentering the spectrometer. The suppression grid is biased at -40 volts and the top plate at +5 volts.

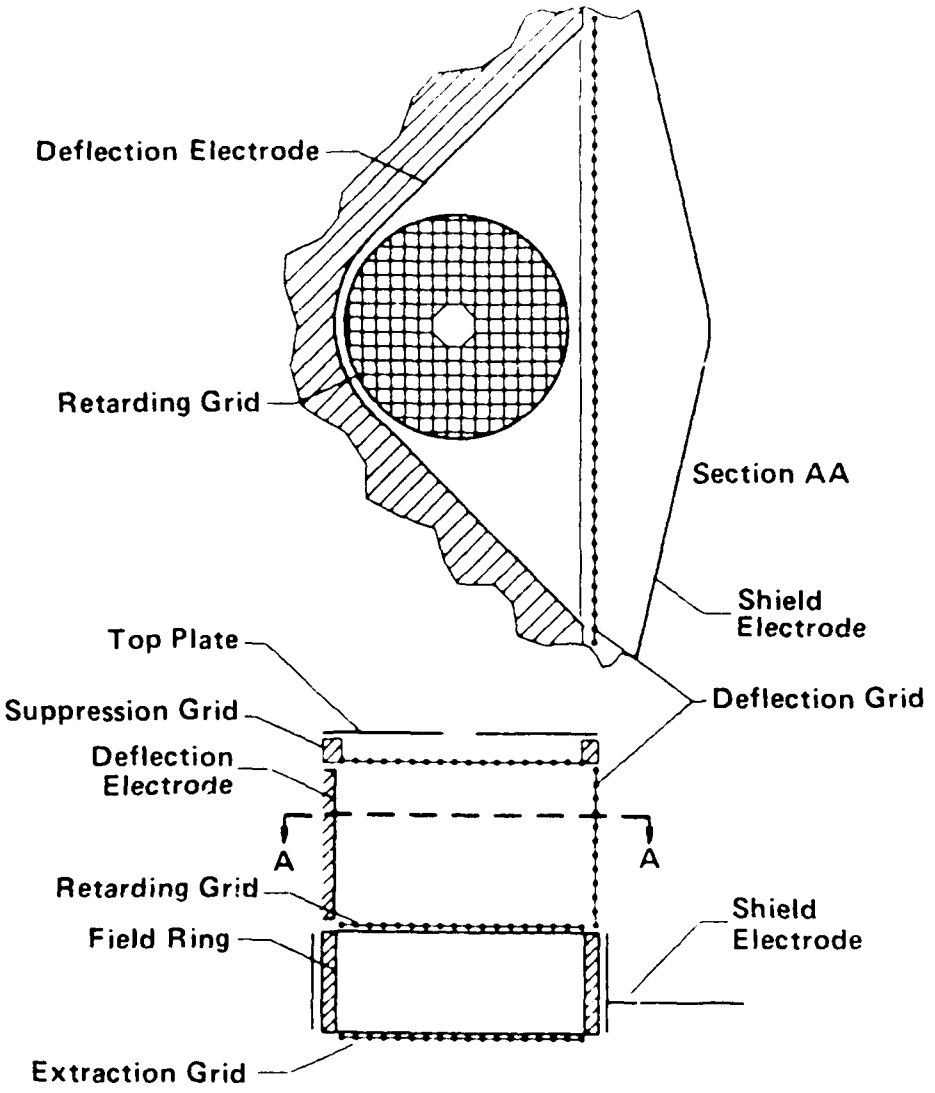


Figure 9.2.1 - Electron Spectrometer

The beam blanker was designed to the following conditions: 1) produce a pulse of sufficiently short duration, 2) be able to blank electron beams within the range of beam energies to be used, 3) be easily aligned, 4) be easily serviced and 5) maintain a constant load to the pulse generator.

A diagram of the beam blanker built for this system is shown in Figure 9.2.2. The blanking plate assembly is a ceramic substrate with gold metal traces. The electron beam is deflected using complementary pulses referenced to ground. These pulses are fed to the blanking plate via the center conductor; the conductors on the lower and upper side of the assembly are at ground. At the blanking plate, a thin film 50 ohm resistor terminates the signal trace to ground. The substrates are mounted parallel to each other but oriented 180 degrees from each other.

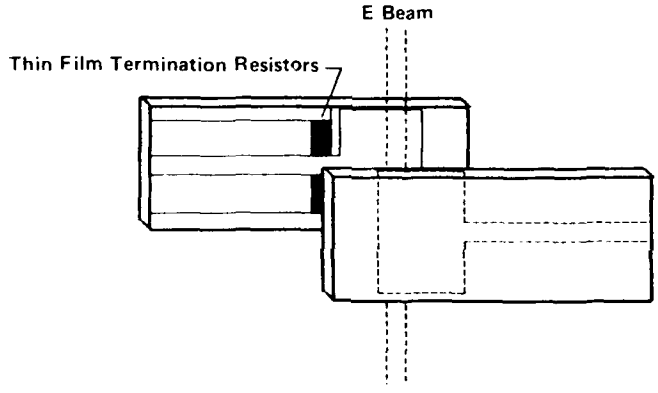


Figure 9.2.2 - Beam Blanker

The beam blanker is situated between the two condenser lenses in the electron column. Below the plates is an aperture that blanks the electron beam.

During operation complementary pulses are applied to the blanking plates, deflecting the electron beam toward the positively biased plate. When an electron pulse is required, ground potential is applied to the plates and the electron beam aligns with the aperture. This generates an electron pulse. The time duration of the electron pulse is determined by the length of time that the plates are at ground potential.

The linearization unit is used to acquire and process the detected secondary electron signal from the electron spectrometer and detector. The linearization unit provides feedback to the electron spectrometer to maintain the detector current at a predetermined value. This is done by changing the potential on the retarding grid until the detector current returns to its nominal value. The change in retarding grid potential is proportional to the change in sample voltage and is used as the measured voltage. The linearization unit is necessary for calibration for accurate voltage measurements.

A sample and hold unit samples the detector current coincident with the electron beam pulse. The sampled voltage is subtracted from a reference voltage which is set at the level required for nominal detector current. The error signal is added to the signal from the feedback amplifier and the summed signal controls the retarding grid voltage. The summed signal is also the measured voltage output. Using a sample and hold on the feedback amp permits operation over a wide range of duty cycles without changing the system bandwidth.

9.3 QVC Measurements

Measurements were taken at internal nodes on the CD4013B, CD4585B, and the SN54LS85. The waveforms acquired will be presented and discussed in this section.

9.3.1 CD4013B QVC Measurements

The most extensive QVC measurements performed for this study were taken on the CMOS devices. Measurements on the CD4013B were taken at internal nodes with no RF interference, with 5 MHz, 10 MHz, and 20 MHz RF interference on the data input, and with no RF interference and 5 MHz RF interference on the clock input. Waveforms were taken along the signal path, at internal Vdd and Vss contacts, and at adjacent associated circuitry. The waveforms are printed on standard computer forms. The originals are relatively large and only one would fit per page of this report. Since there are over 60 of these plots for this section alone, a reduction of the size was required. This was accomplished on a copy machine, thus the plots presented here are reduced copies of the originals.

Each of the QVC waveform plots displays voltage versus time. The horizontal axis (time scale) is labelled, e.g., microseconds. The vertical axis (voltage scale) is not labelled. The units for the numbers on this axis are volts. The time per horizontal division and voltage per vertical division is provided on each of the oscilloscope photographs.

Figure 9.3.1.1 provides the logic diagram for the CD4013B for easy reference to the waveforms. Figures 9.3.1.2 - 9.3.1.5 show the osciloscope waveforms of the data input and Q output under the four test conditions, no RF, and 5 MHz, 10 MHz, and 20 MHz RF. The QVC waveforms will be presented by node with each of the four test conditions presented together for comparison.

Figure 9.3.1.6 shows the QVC waveforms after the data input pin ESD protect network, prior to transmission gate 1 (TG1). This is the input node for TG1. The variation of the voltage amplitude and offset is partly due to the measurement system. Amplitude and offset could be altered by adjustment of the operating parameters of the system irrespective of the actual signal. This and the limited operating frequency of about 20 MHz are the primary deficiencies of the SEM QVC system used for this study.

Figure 9.3.1.7 shows the data input signal QVC waveforms present at the output node of TG1. This transmission gate is active during the first half of each of the logic levels on the data input, i.e., it transmits the logic level present during the first half of the high data level and then locks in the logic level at that time (falling edge of the clock pulse) followed by transmitting through the low logic level during the first half of the low data level and then locks in the logic level present at that time. For the 5 Mhz signal, the effect of this timing is to transmit through the high logic level and lock in on a high level followed by transmitting through the low level but locking in on a high level. The 5 MHz RF interference signal is within the operating capability of this device. At 10 MHz the circuit cannot respond properly and a distorted waveform occurs. A similar effect appears to be occurring at 20 MHz.

Figure 9.3.1.8 show the data input signal QVC waveforms following inversion of the signals by NAND gate 2. The signals from NAND gate 3 are shown in Figure 9.3.1.9 (this was not measured at 20 MHz).

The slave section transmission gate (TG3) and the NAND gates and inverters going to the Q output were measured and are shown in Figures 9.3.1.10 - 9.3.1.13.

Figures 9.3.1.14 - 9.3.1.25 show the waveforms at various nodes along the clock and data signal paths with 5 MHz RFI on the clock input pin.

The effect on the clock signal, of RF interference on the data input pin, was measured at 5 MHz, 10 MHz, and 20 MHz (Figures 9.3.1.26 - 9.3.1.28). The coupling effect was also measured at internal contact points for Vdd and Vss (Figures 9.3.1.29 and 9.3.1.30). Coupling is apparent.

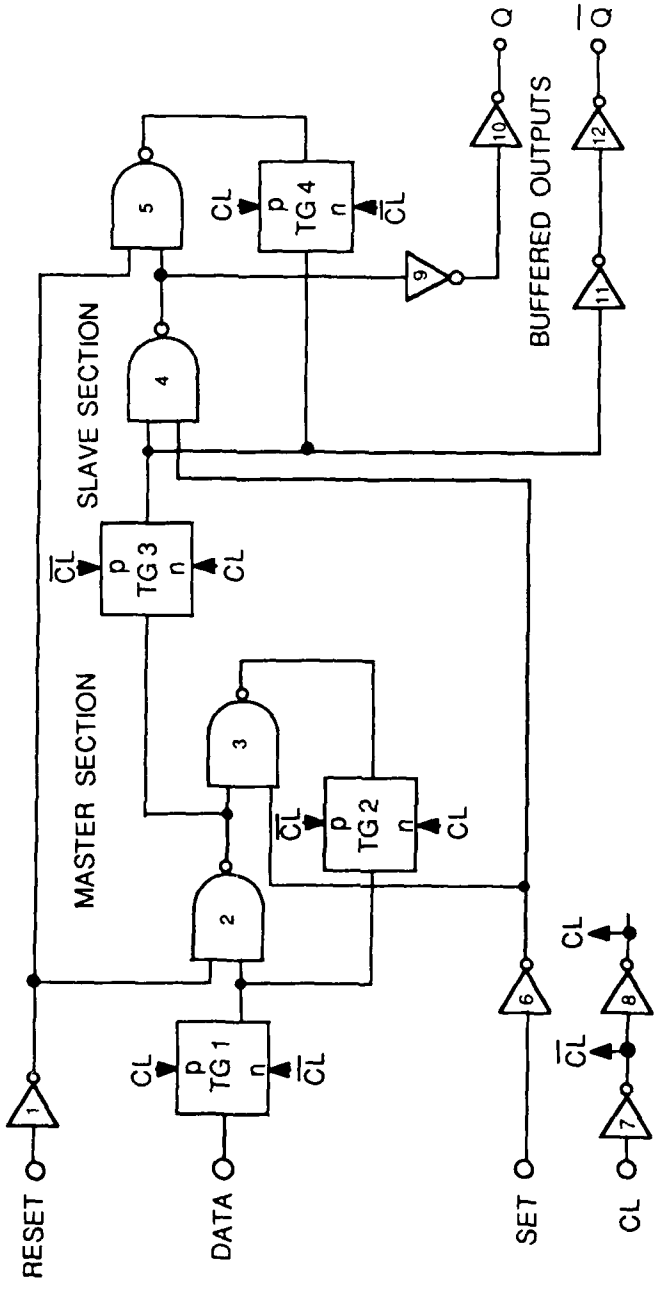


Figure 9.3.1.1 - CD4013B Logic Diagram
Note: Transmission gates are numbered TG 1 through TG 4, logic gates are numbered 1 through 12, inputs are on the left hand side, and outputs are on the right hand side.

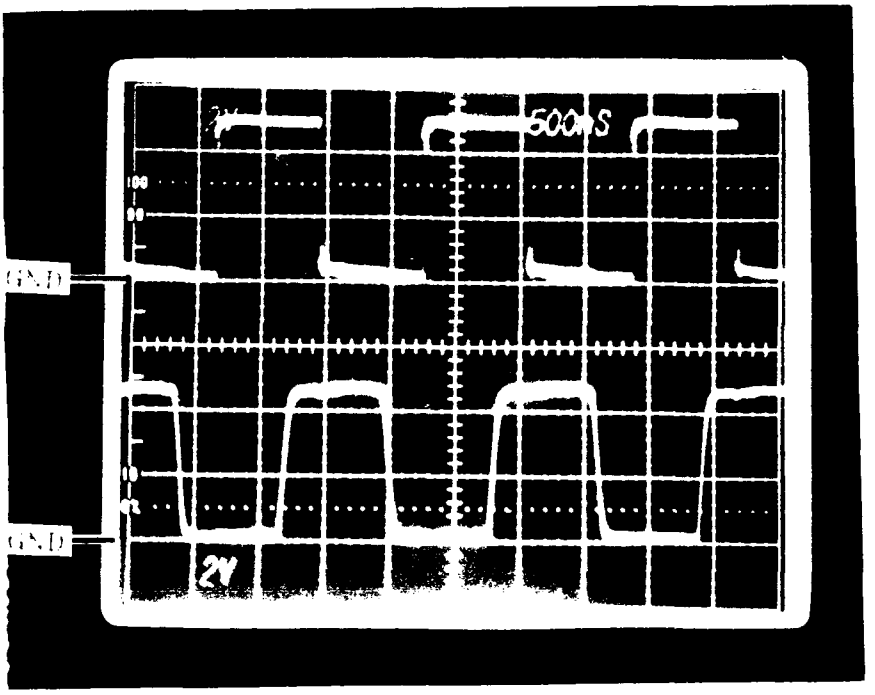


Figure 9.3.1.2 - CD4013B Oscilloscope Photograph, No RF
Top trace = Data input
Bottom trace = Q output

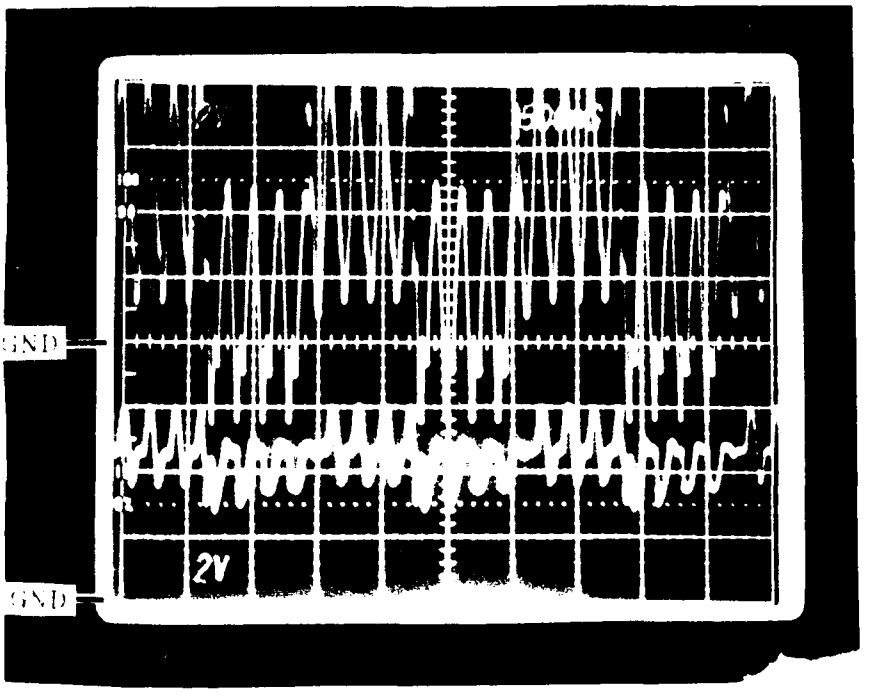


Figure 9.3.1.3 - CD4013B Oscilloscope Photograph
Top trace = Data input with 5 MHz RF
Bottom trace = Q output

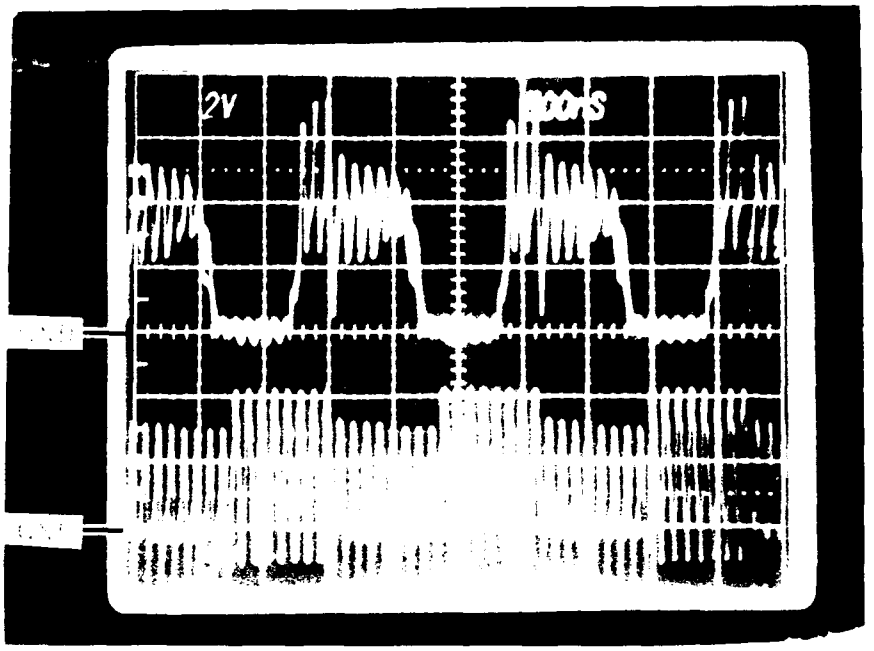


Figure 9.3.1.4 - CD4013B Oscilloscope Photograph
Top trace = Q output
Bottom trace = Data input with 10 MHz RF

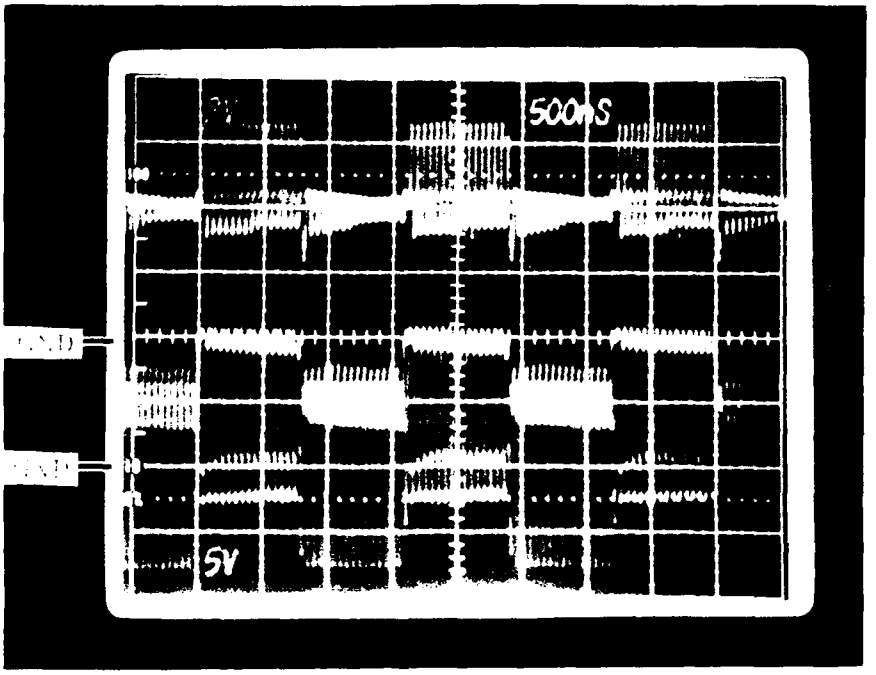
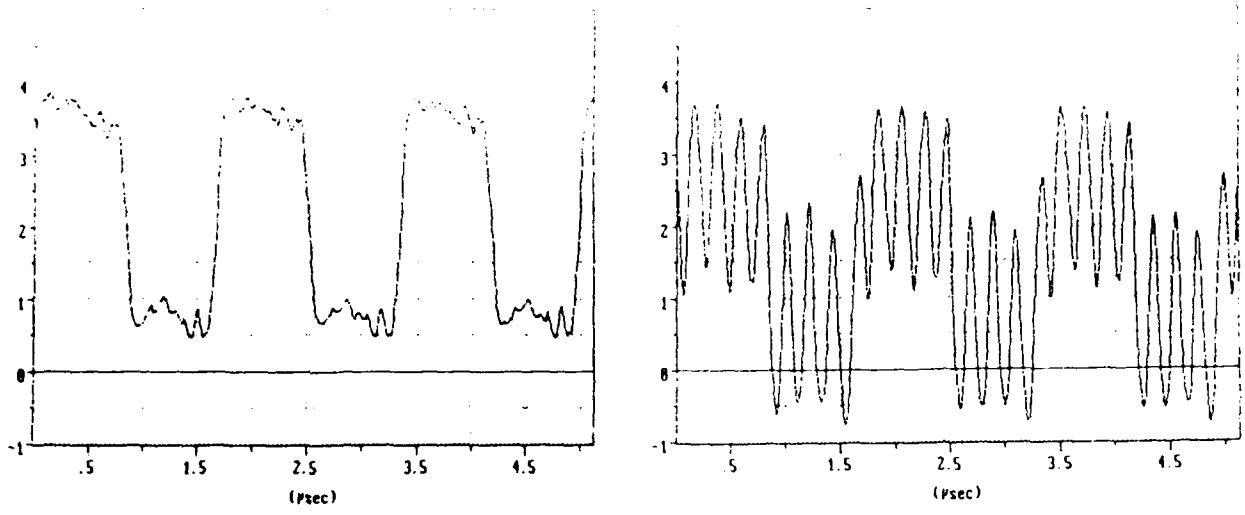
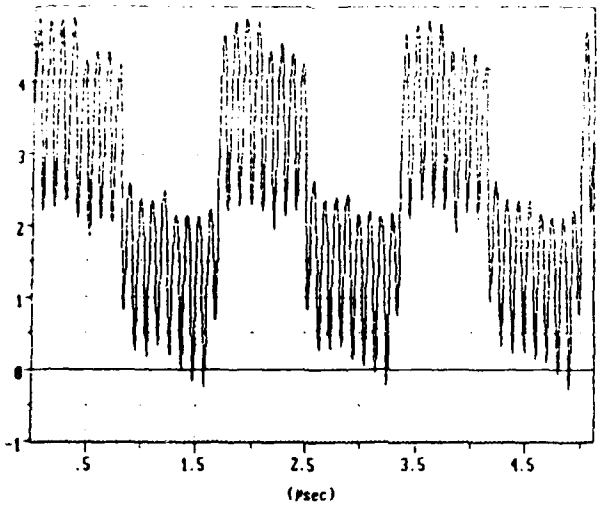


Figure 9.3.1.5 - CD4013B Oscilloscope Photograph
Top trace = Q output
Bottom trace = Data input with 20 MHz RF

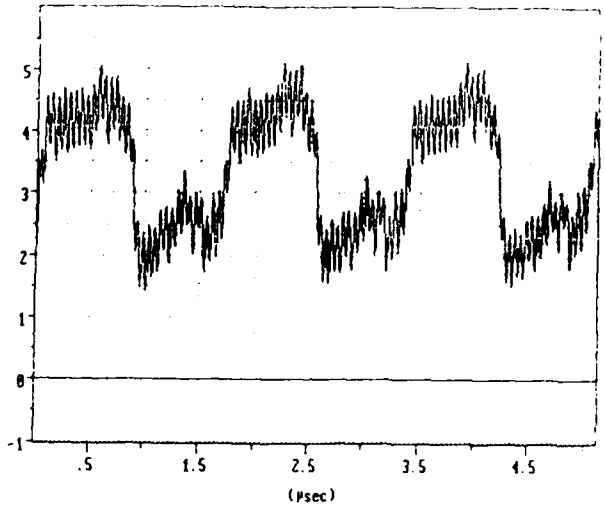


A.

B.



C.



D.

Figure 9.3.1.6 - CD4013B QVC Waveforms at Input Node of TG1, Data Input Signal Path
A. No RF
B. 5 MHz RF on Data Input Pin
C. 10 MHz RF on Data Input Pin
D. 20 MHz RF on Data Input Pin

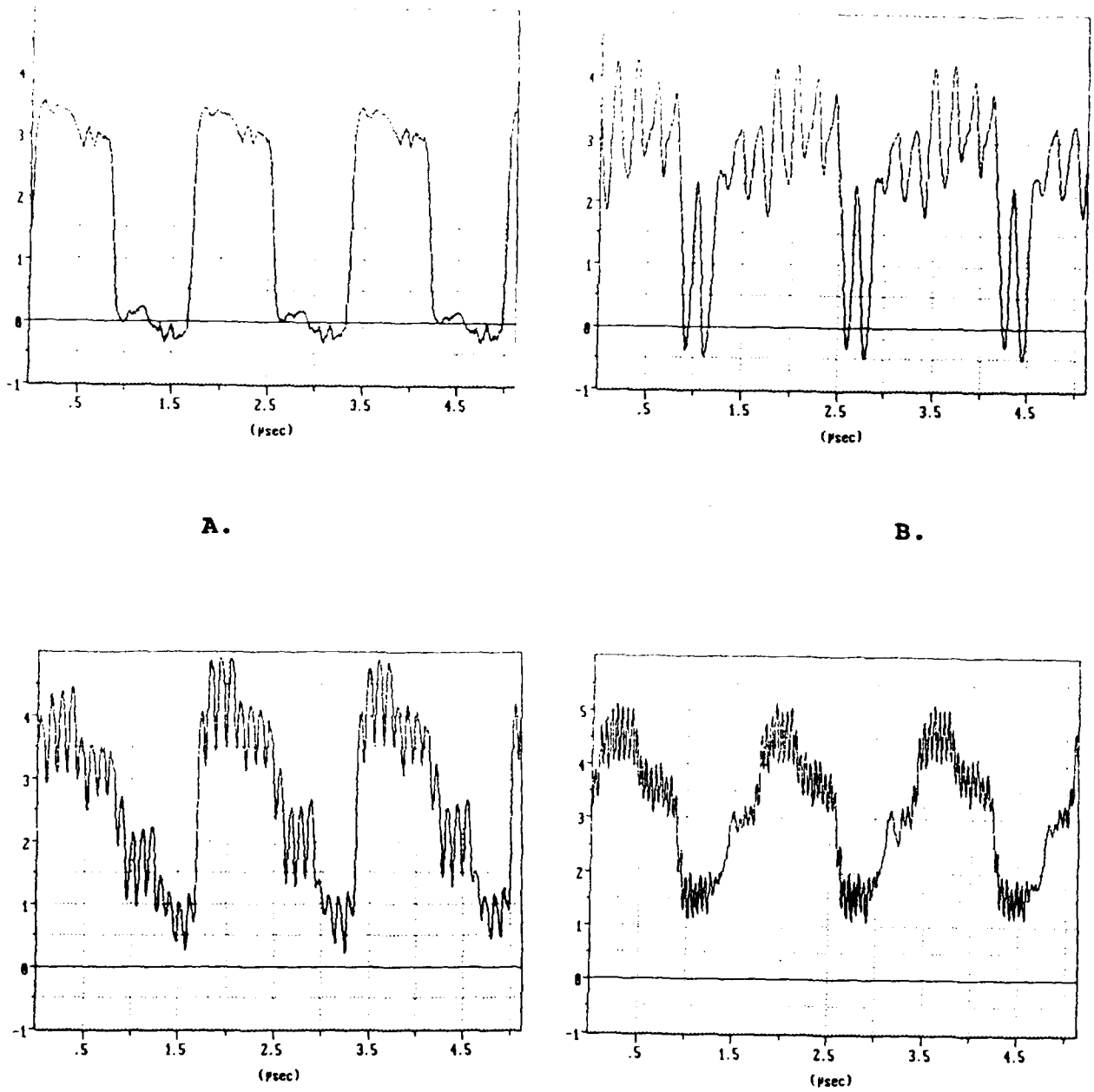
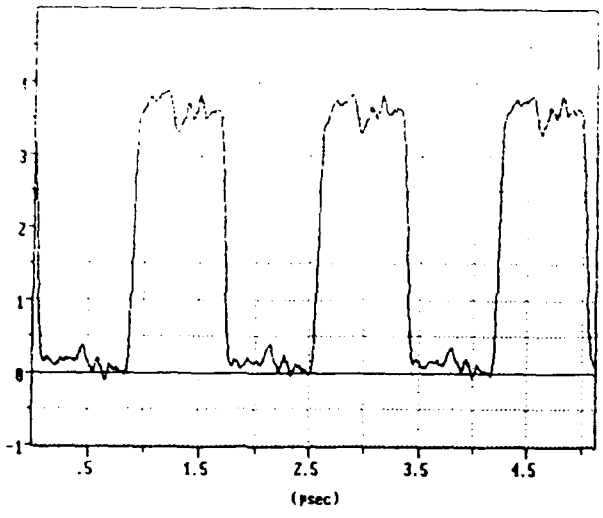
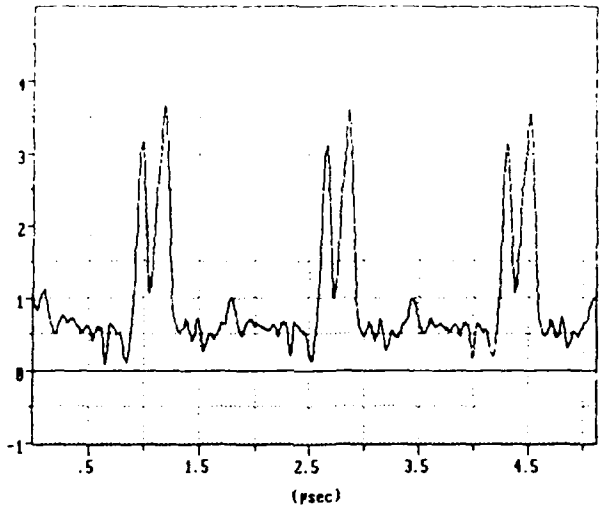


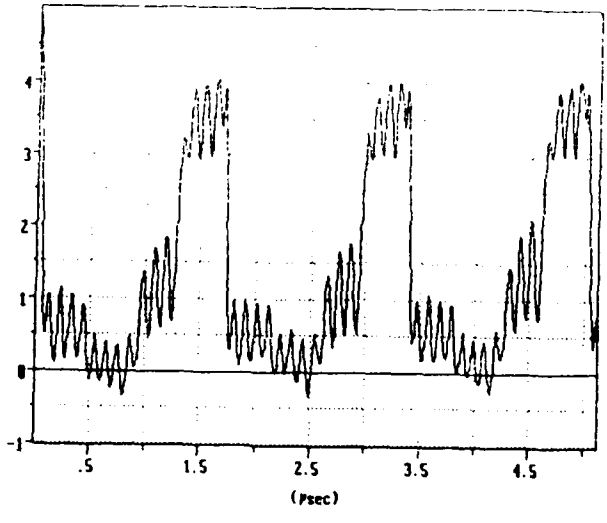
Figure 9.3.1.7 - CD4013B QVC Waveforms at Output Node of TG1, Data Input Signal Path
A. No RF
B. 5 MHz RF on Data Input Pin
C. 10 MHz RF on Data Input Pin
D. 20 MHz RF on Data Input Pin



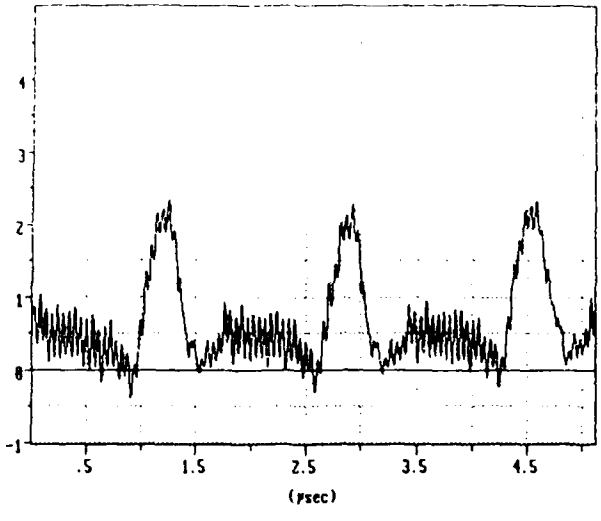
A.



B.

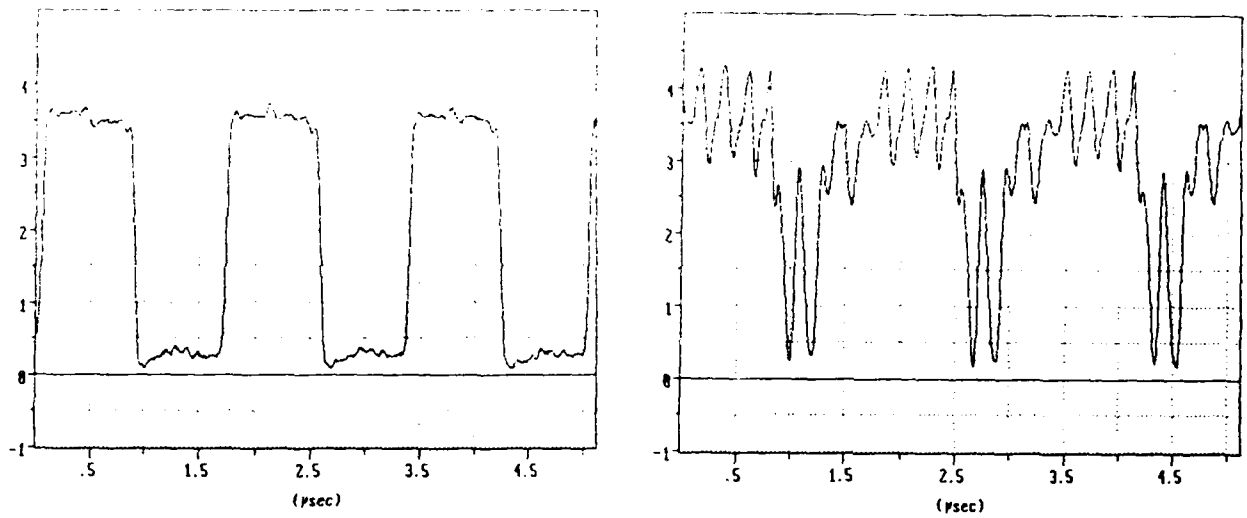


C.



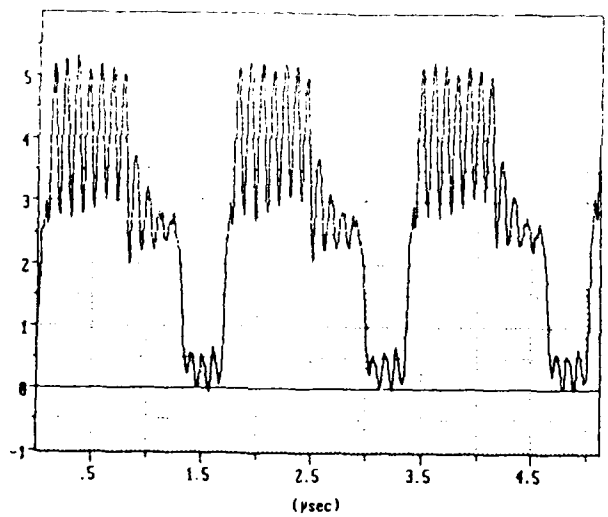
D.

Figure 9.3.1.8 - CD4013B QVC Waveforms at Output Node of NAND Gate 2, Data Input Signal Path
A. No RF
B. 5 MHz RF on Data Input Pin
C. 10 MHz RF on Data Input Pin
D. 20 MHz RF on Data Input Pin



A.

B.



C.

Figure 9.3.1.9 - CD4013B QVC Waveforms at Output Node of NAND Gate 3, Data Input Signal Path
A. No RF
B. 5 MHz RF on Data Input Pin
C. 10 MHz RF on Data Input Pin

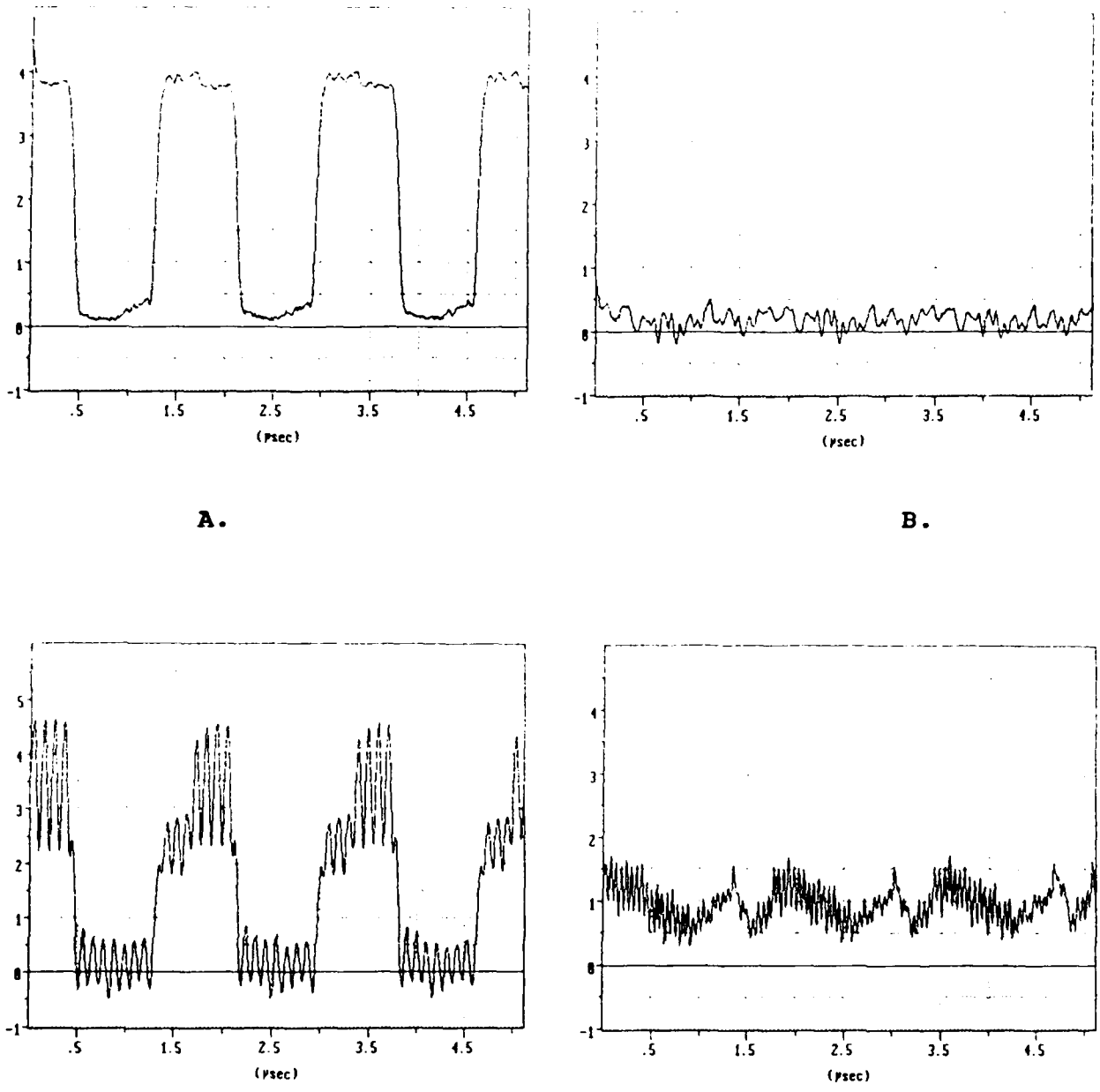
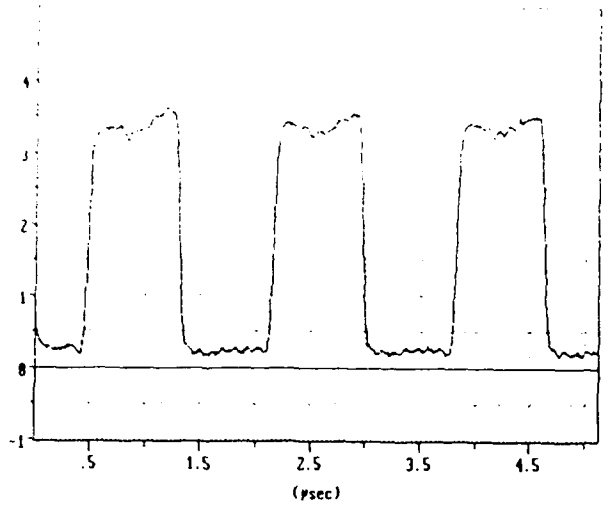
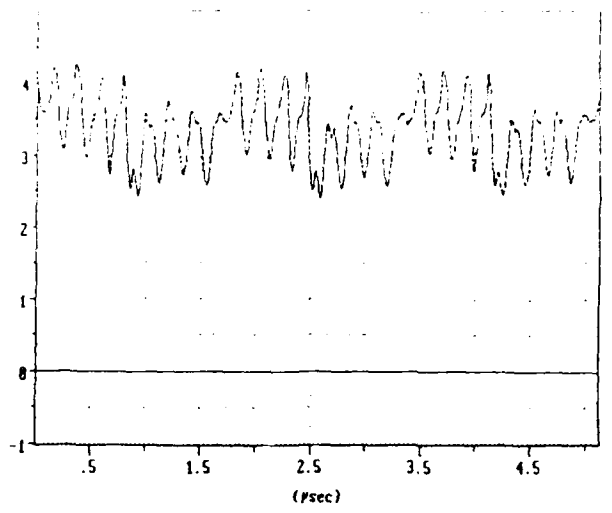


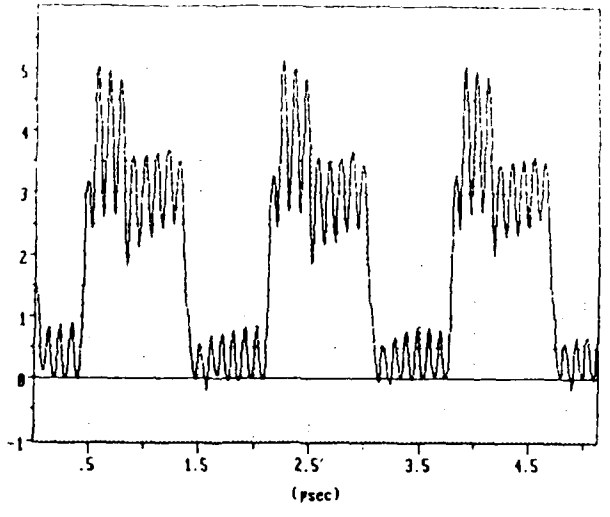
Figure 9.3.1.10 - CD4013B QVC Waveforms at Output Node of TG3, Data Input Signal Path
A. No RF
B. 5 MHz RF on Data Input Pin
C. 10 MHz RF on Data Input Pin
D. 20 MHz RF on Data Input Pin



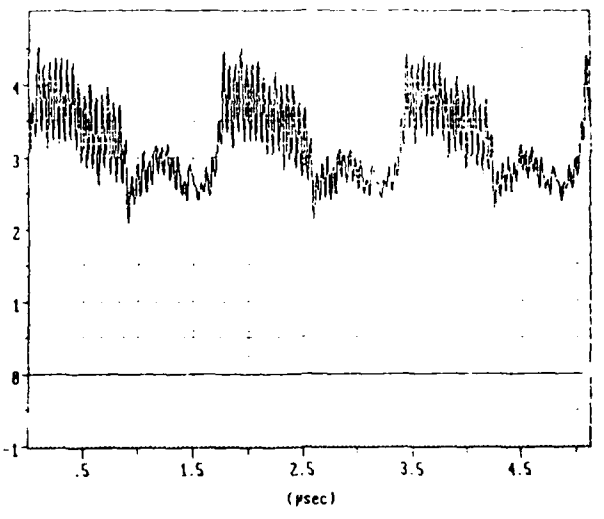
A.



B.

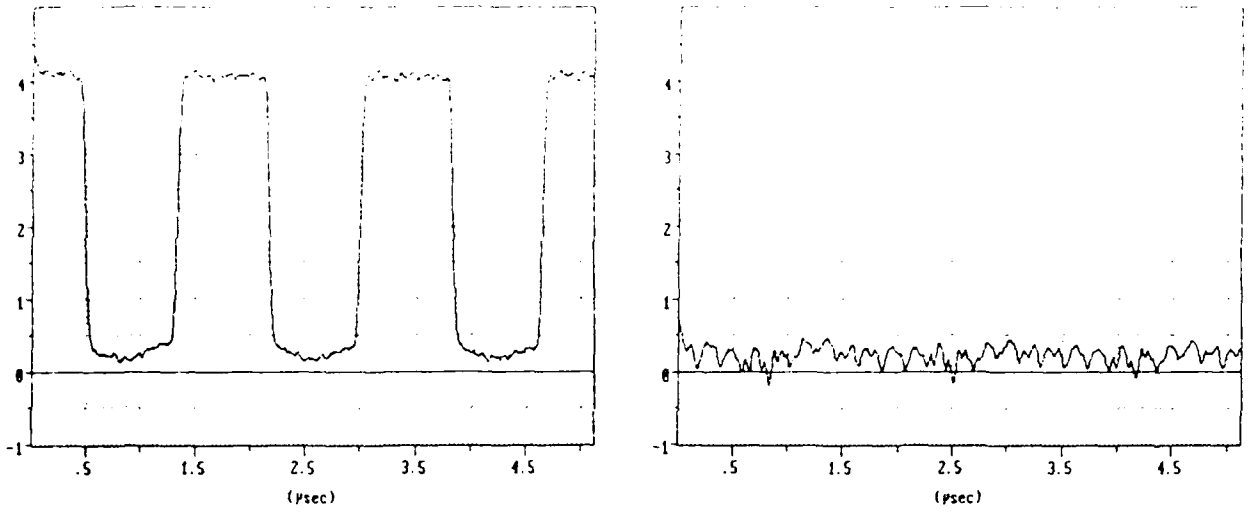


C.



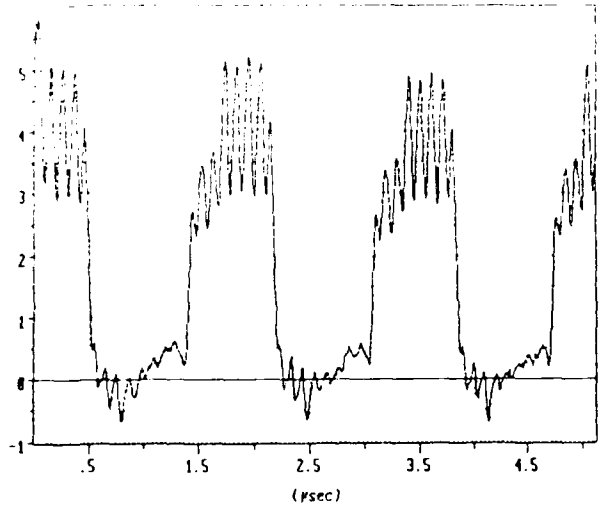
D.

Figure 9.3.1.11 - CD4013B QVC Waveforms at Output Node of NAND Gate 4, Data Input Signal Path
A. No RF
B. 5 MHz RF on Data Input Pin
C. 10 MHz RF on Data Input Pin
D. 20 MHz RF on Data Input Pin



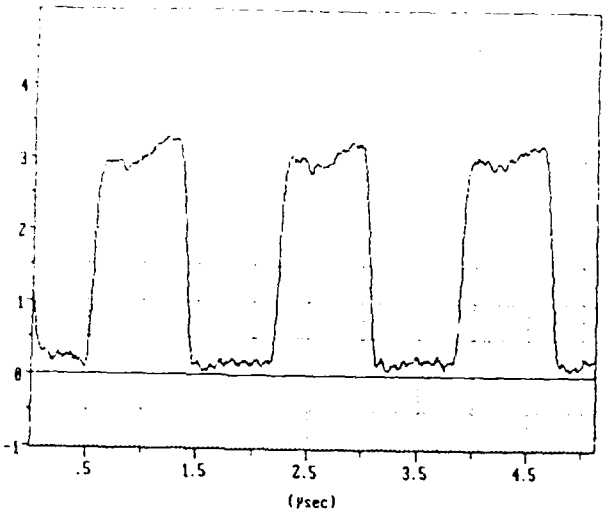
A.

B.

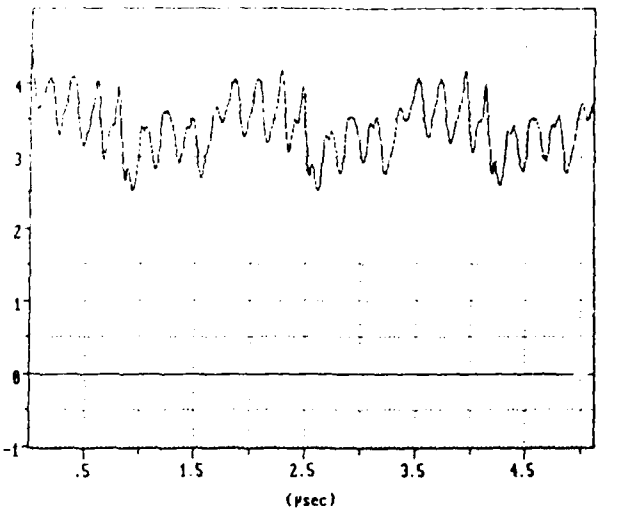


C.

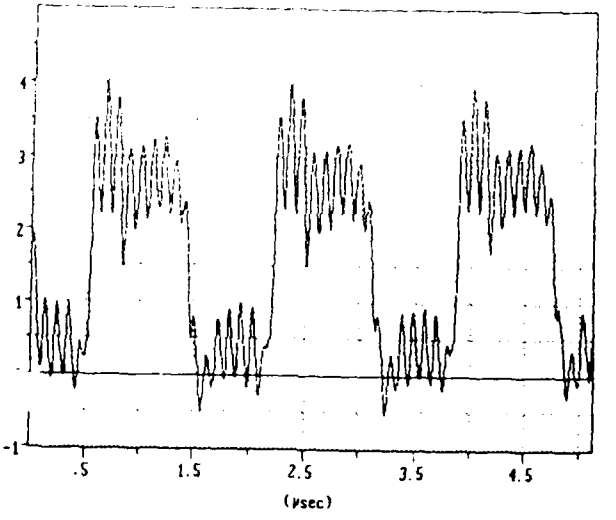
Figure 9.3.1.12 - CD4013B QVC Waveforms at Output Node of Inverter 9, Data Input Signal Path
A. No RF
B. 5 MHz RF on Data Input Pin
C. 10 MHz RF on Data Input Pin



A.



B.



C.

Figure 9.3.1.13 - CD4013B QVC Waveforms on Metallization at Q Output Pin Bond Pad
A. N RF
B. 5 MHz RF on Data Input Pin
C. 10 MHz RF on Data Input Pin

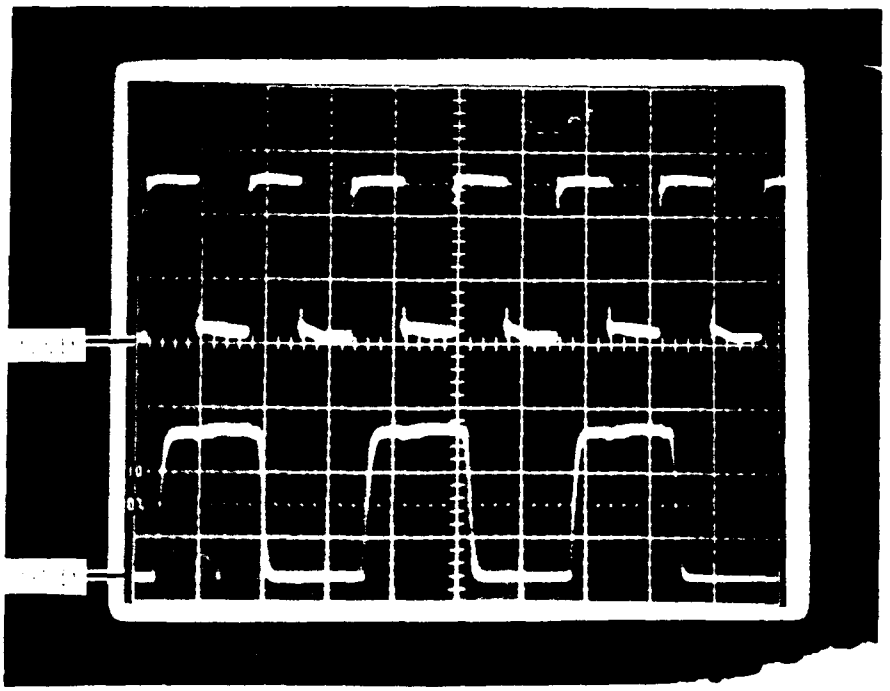


Figure 9.3.1.14 - CD4013B Oscilloscope Photograph, No RF
Top trace = Clock input
Bottom trace = Q output

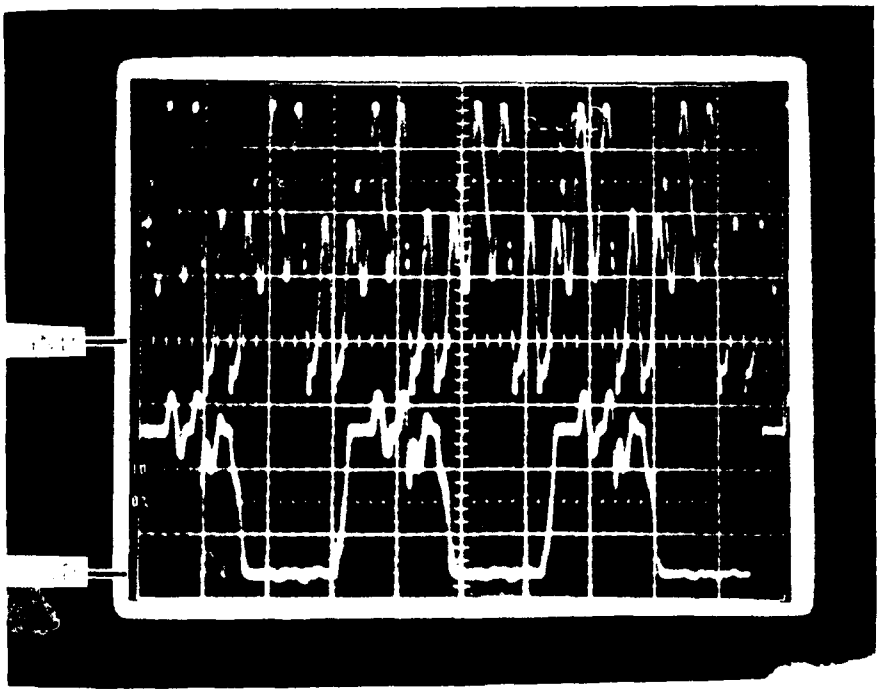
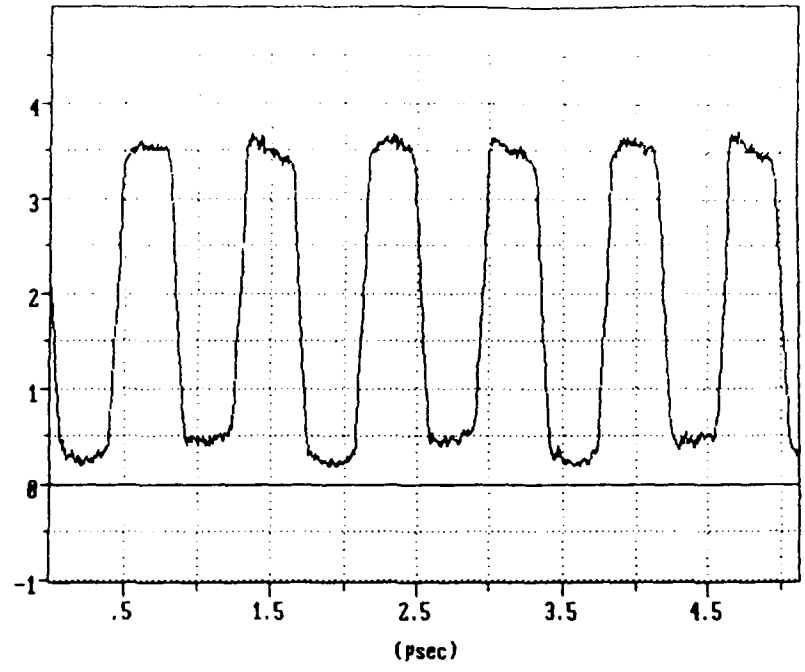
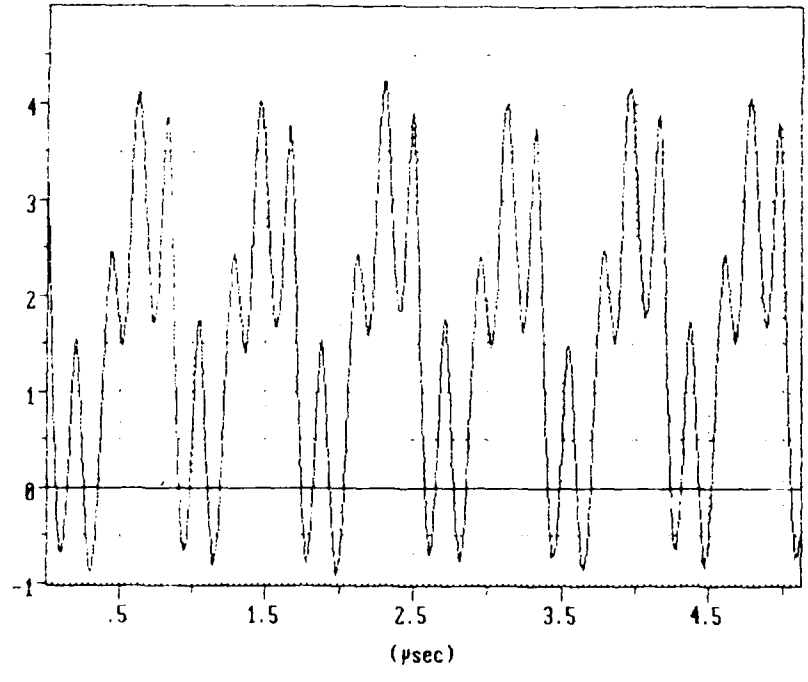


Figure 9.3.1.15 - CD4013B Oscilloscope Photograph
Top trace = Clock input with 5 MHz RF
Bottom trace = Q output

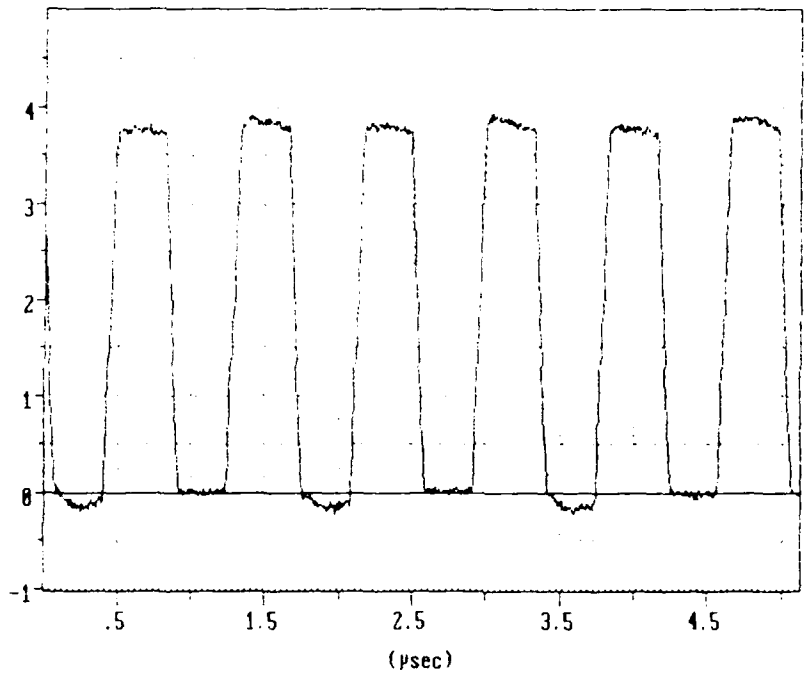


A.

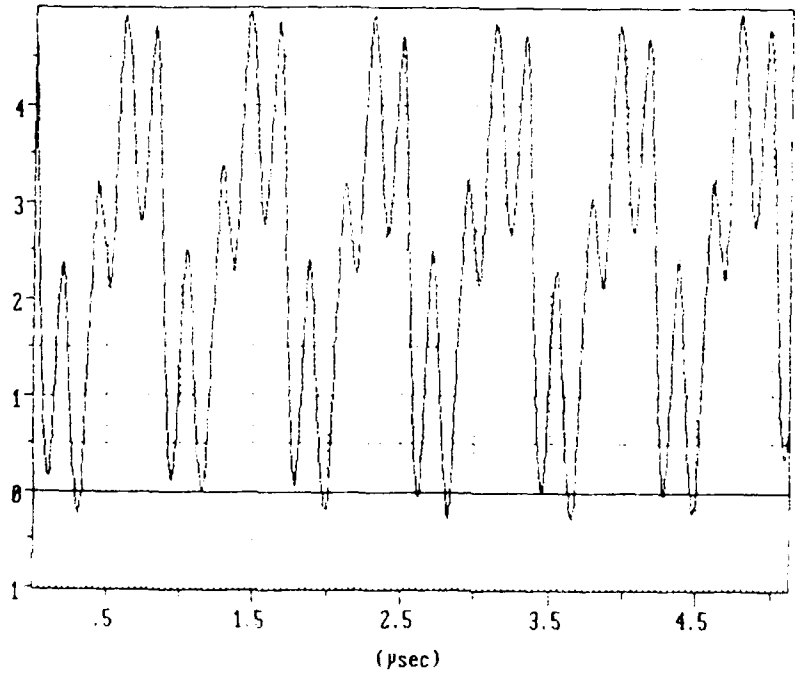


B.

Figure 9.3.1.16 - CD4013B QVC Waveforms at Clock Input Pin Bond Pad Prior to ESD Network
A. No RF
B. 5 MHz RF on Clock Input Pin

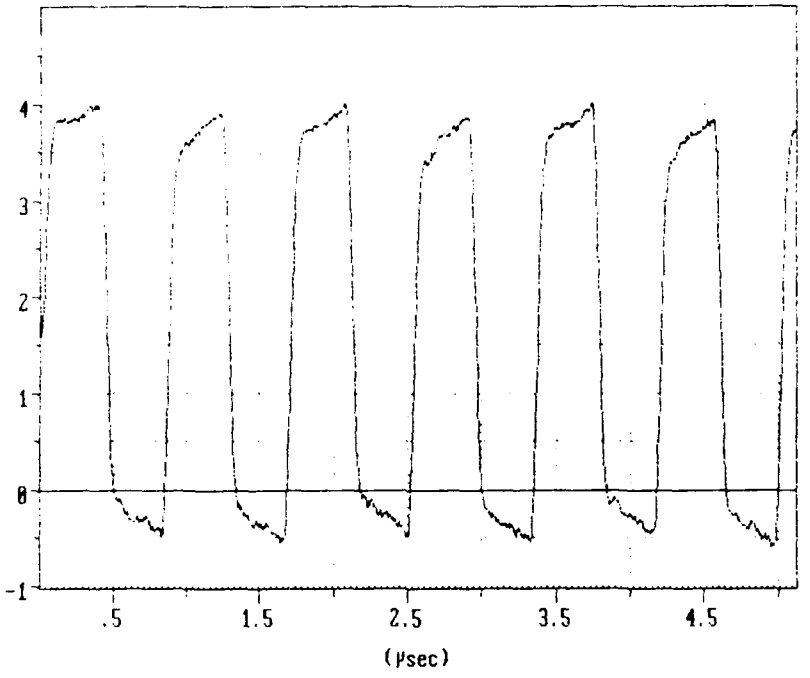


A.

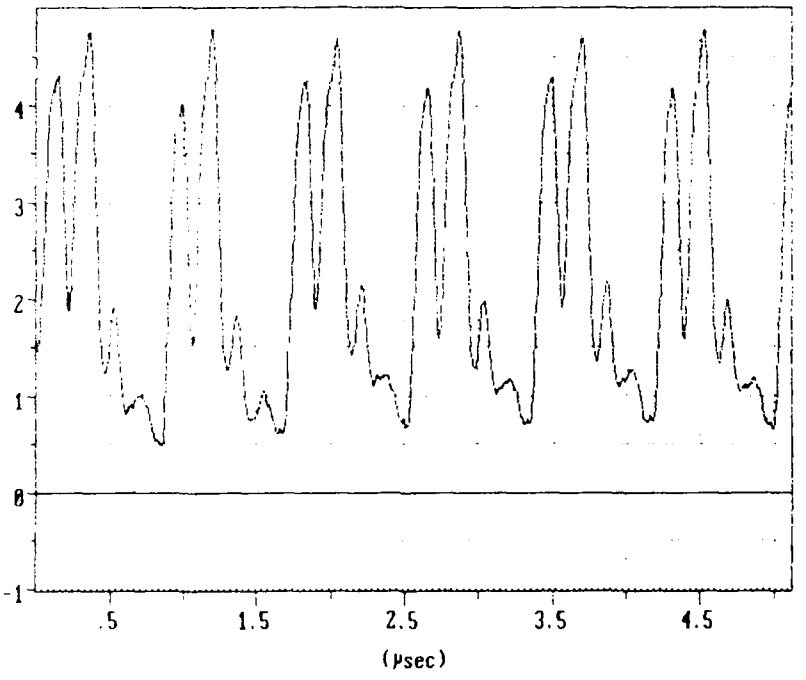


B.

Figure 9.3.1.17 - CD4013B QVC Waveforms at Input Node of Inverter 7, Clock Input Signal Path
A. No RF
B. 5 MHz RF on Clock Input Pin

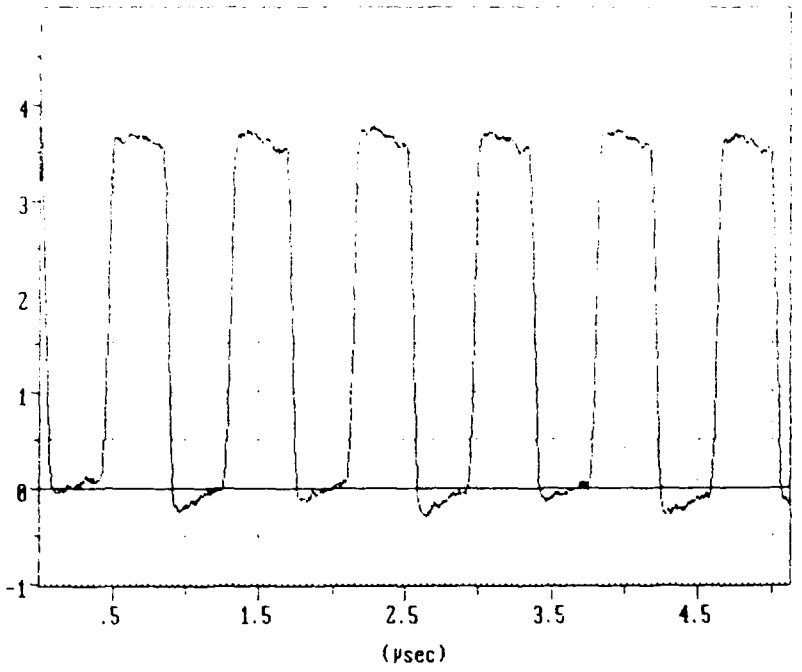


A.

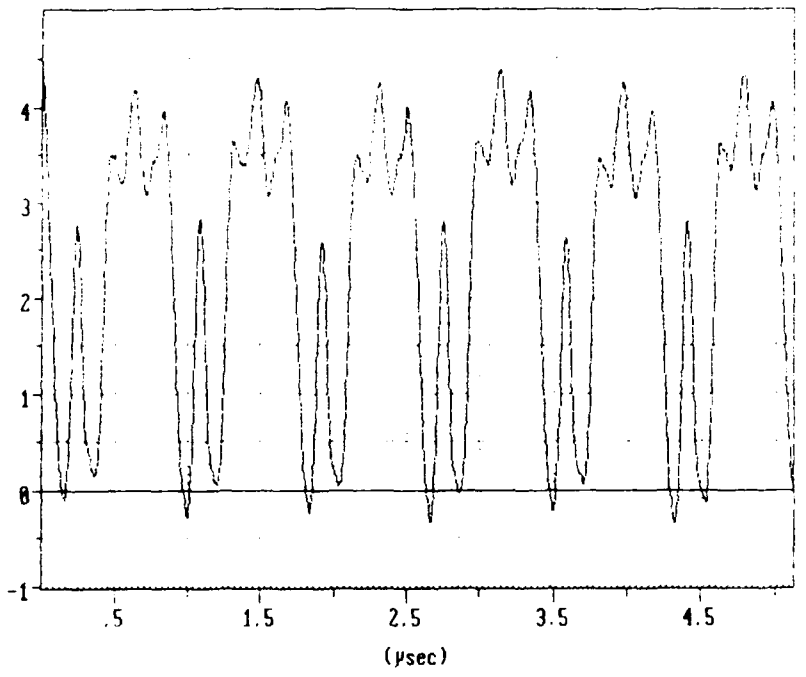


B.

Figure 9.3.1.18 - CD4013B QVC Waveforms on Output Node of Inverter 7, Clock Input Signal Path
A. No RF
B. 5 MHz RF on Clock Input Pin

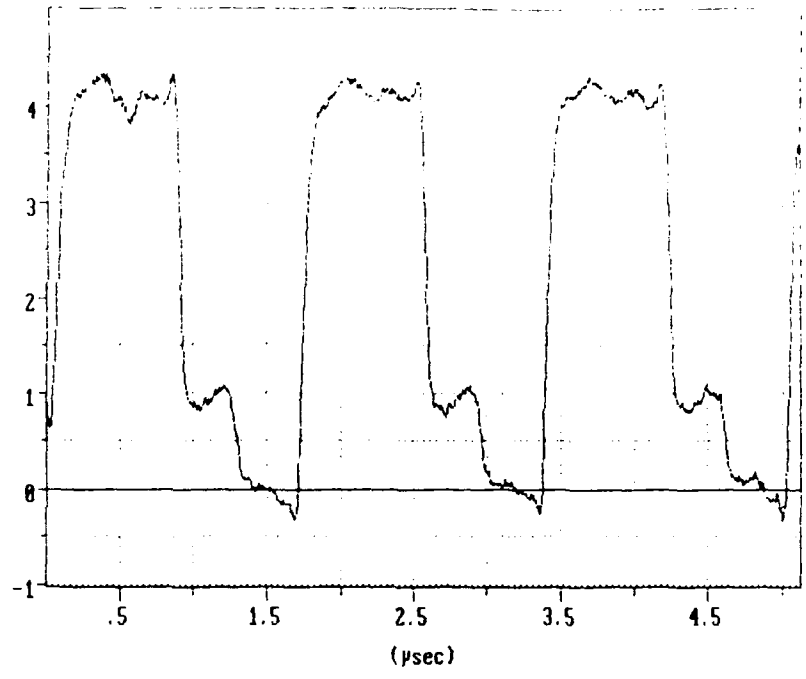


A.

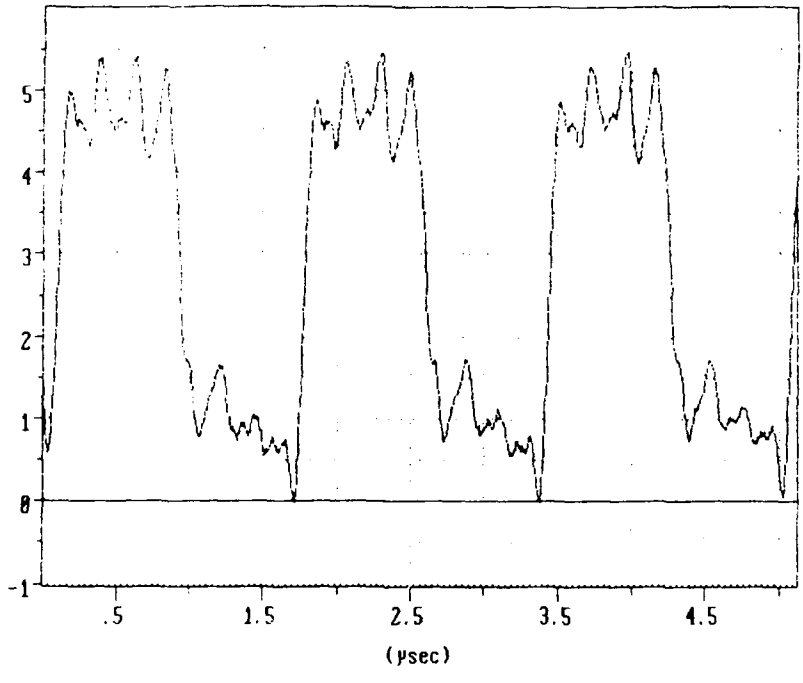


B.

Figure 9.3.1.19 - CD4013B QVC Waveforms on Output Node of Inverter 8, Clock Input Signal Path
A. No RF
B. 5 MHz RF on Clock Input Pin

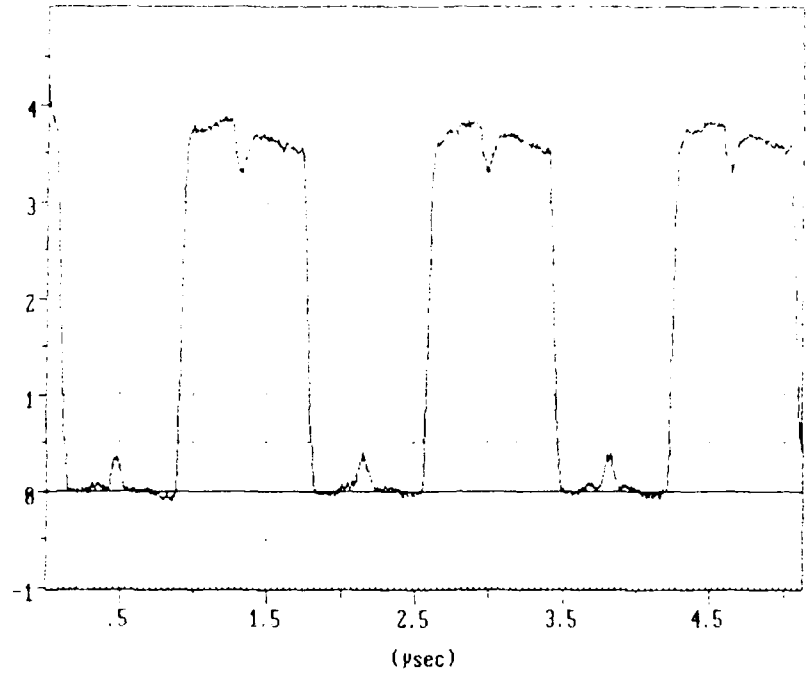


A.

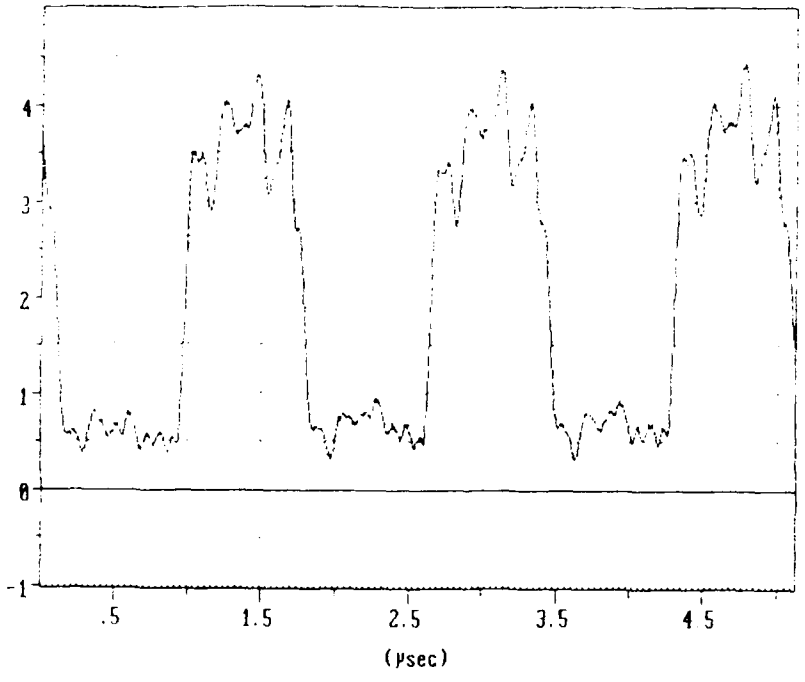


B.

Figure 9.3.1.20 - CD4013B QVC Waveforms on Output Node of TG1
A. No RF
B. 5 MHz RF on Clock Input Pin

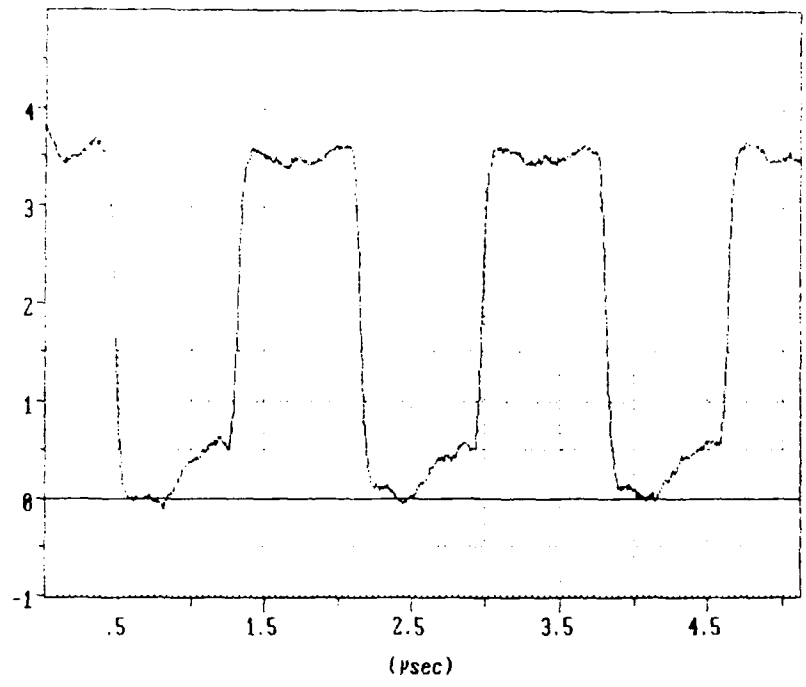


A.

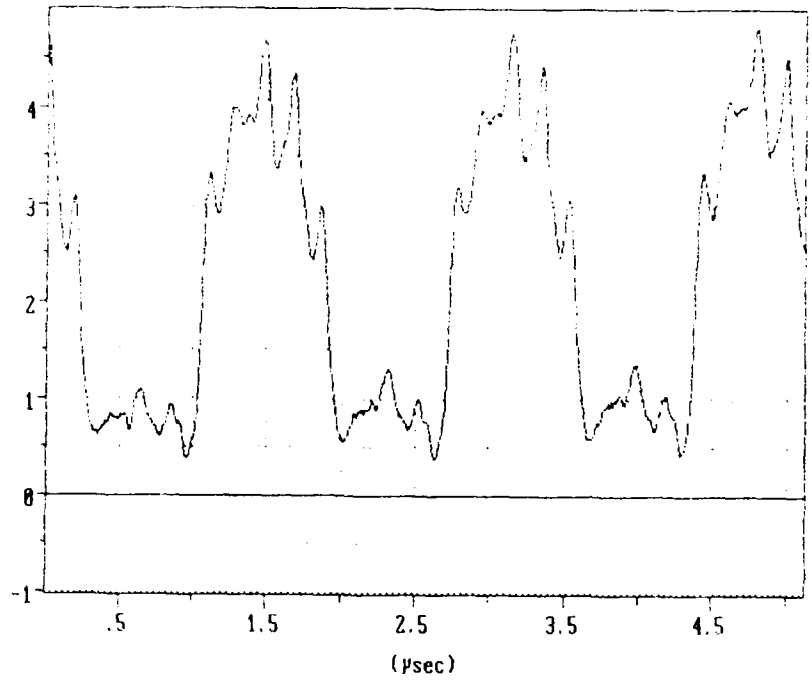


B.

Figure 9.3.1.21 - CD4013B QVC Waveforms on Output Node of NAND Gate 2
A. No RF
B. 5 MHz RF on Clock Input Pin

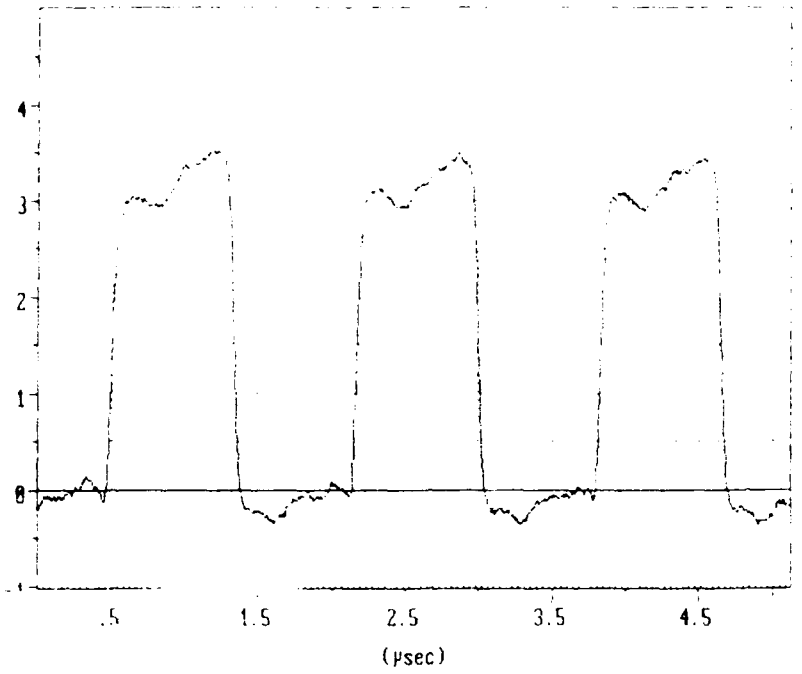


A.

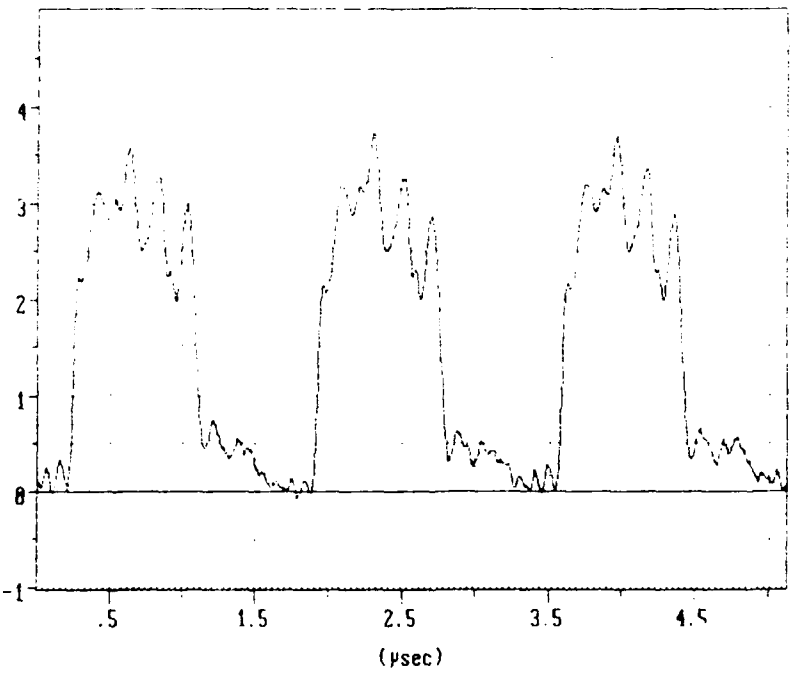


B.

Figure 9.3.1.22 - CD4013B QVC Waveforms on Output Node of TG3
A. No RF
B. 5 MHz RF on Clock Input Pin

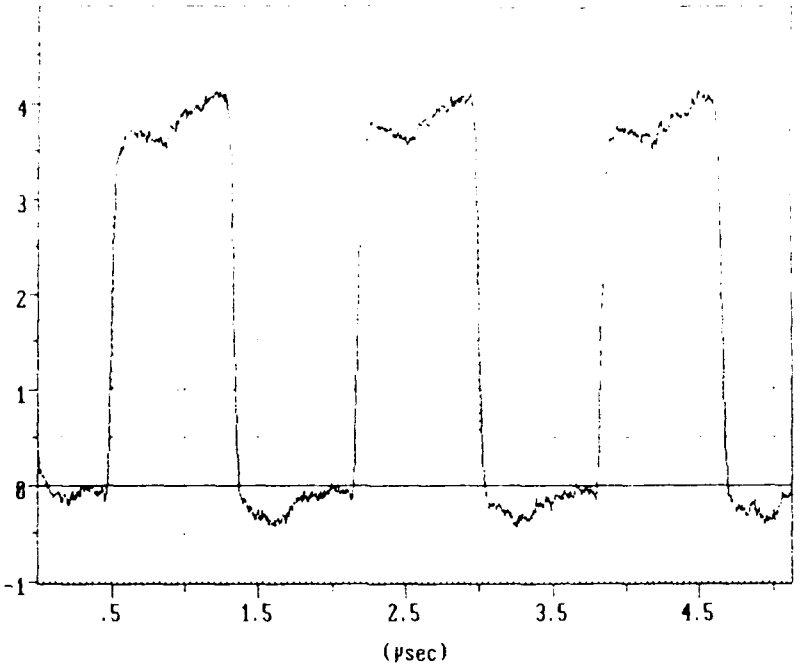


A.

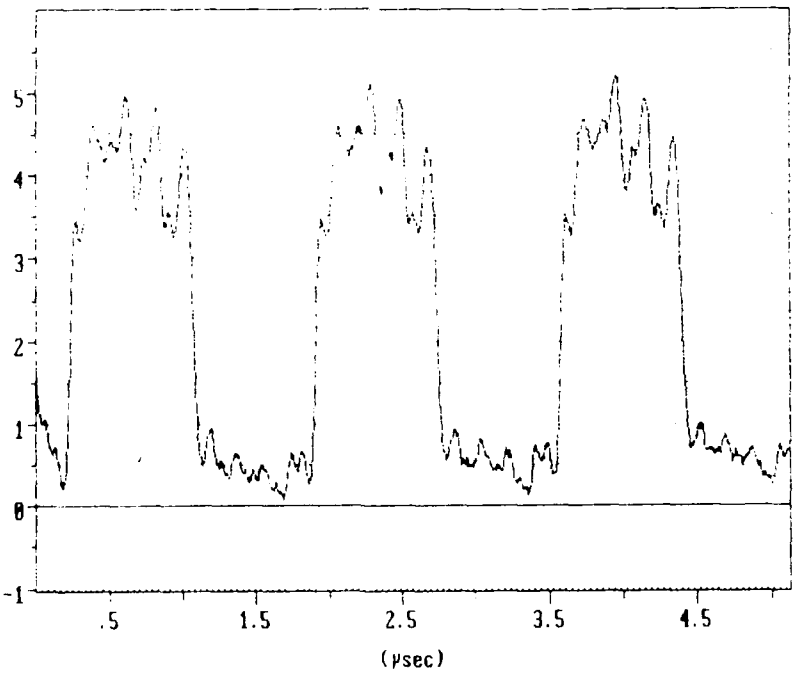


B.

Figure 9.3.1.23 - CD4013B QVC Waveforms on Output Node of NAND Gate 4
A. No RF
B. 5 MHz RF on Clock Input Pin

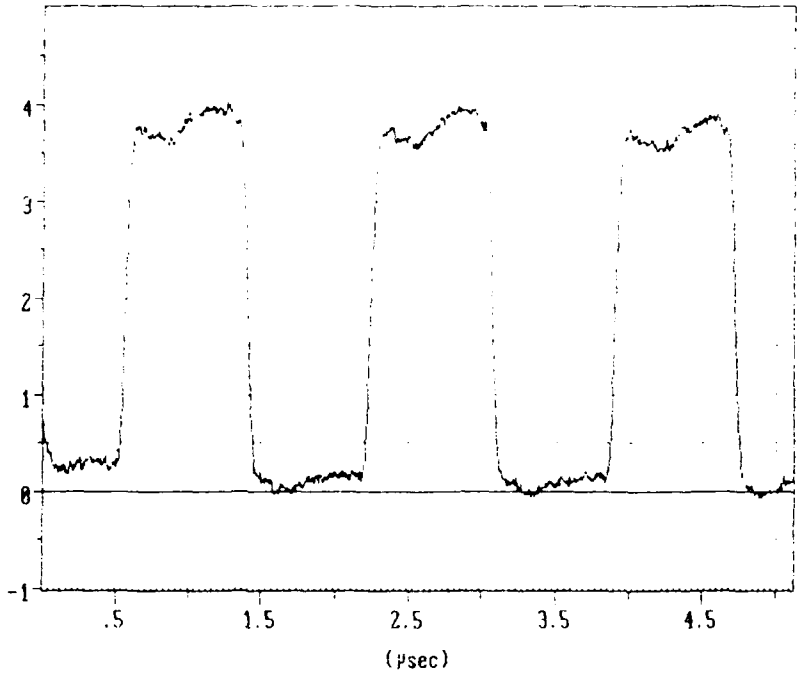


A.

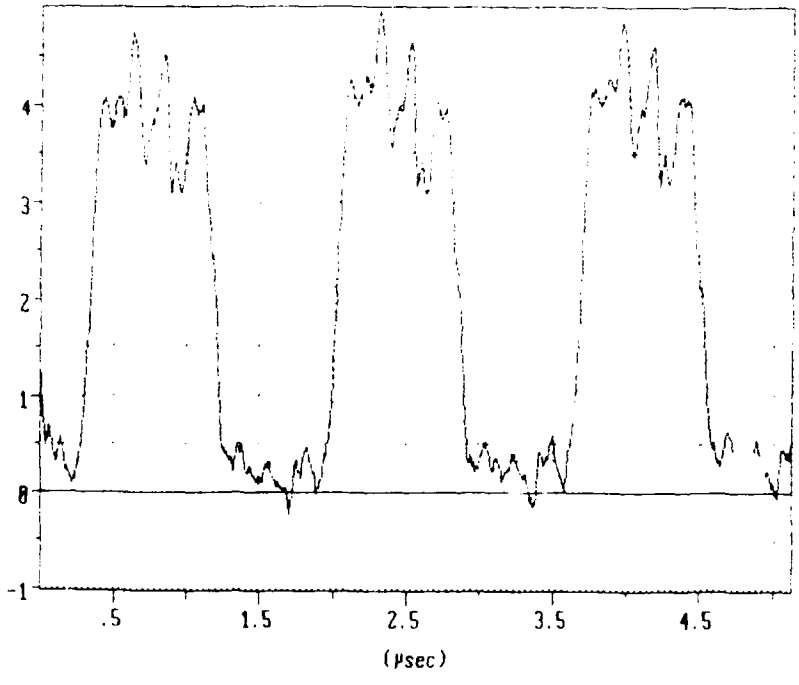


B.

Figure 9.3.1.24 - CD4013B QVC Waveforms on Output Node of NAND Gate 9
A. No RF
B. 5 MHz RF on Clock Input Pin

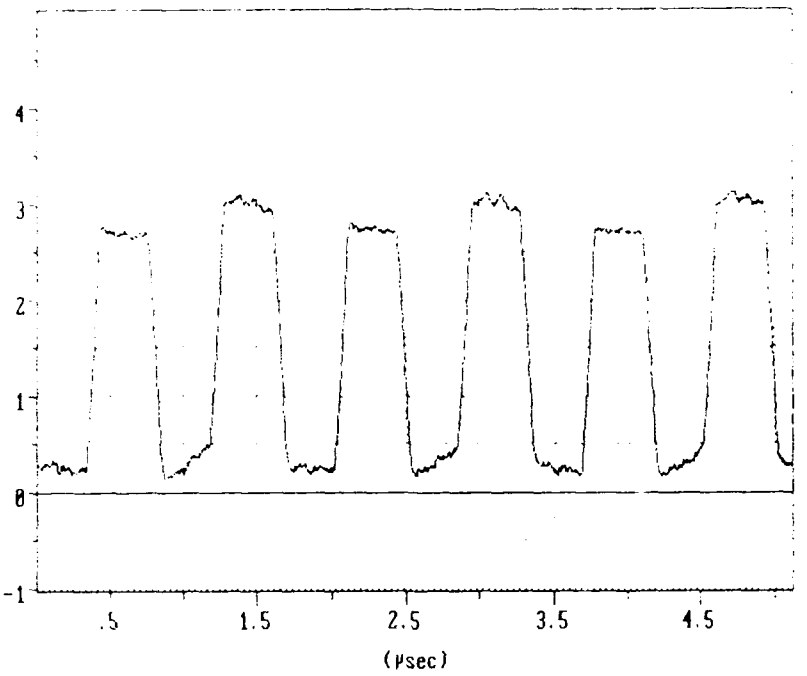


A.

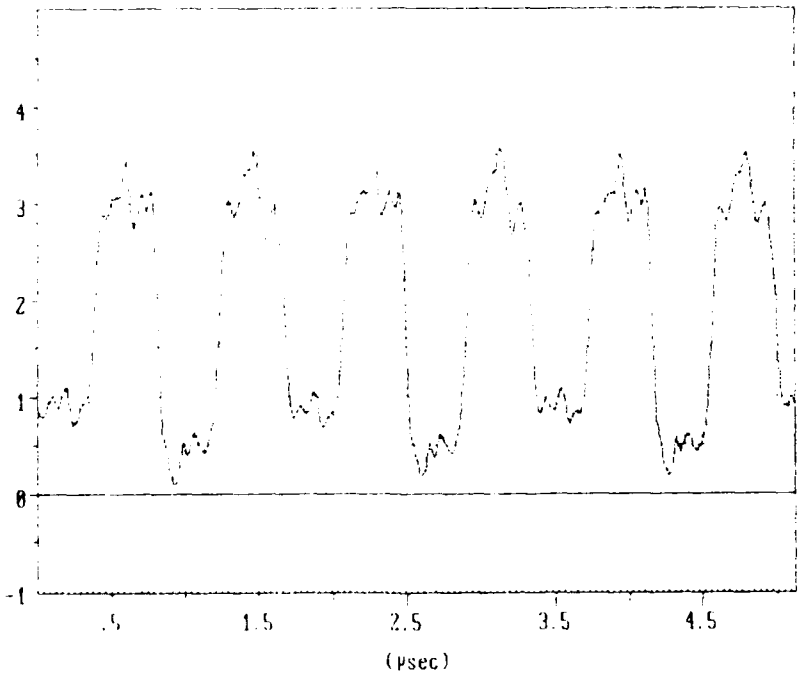


B.

Figure 9.3.1.25 - CD4013B QVC Waveforms on Metallization of Q Output Pin Bond Pad
A. No RF
B. 5 MHz RF on Clock Input Pin

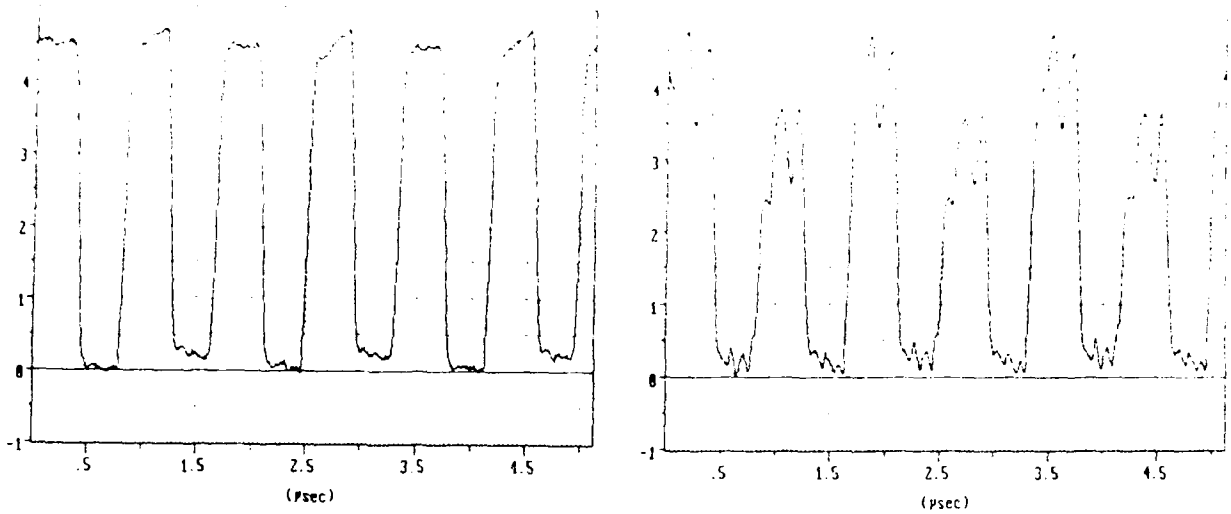


A.



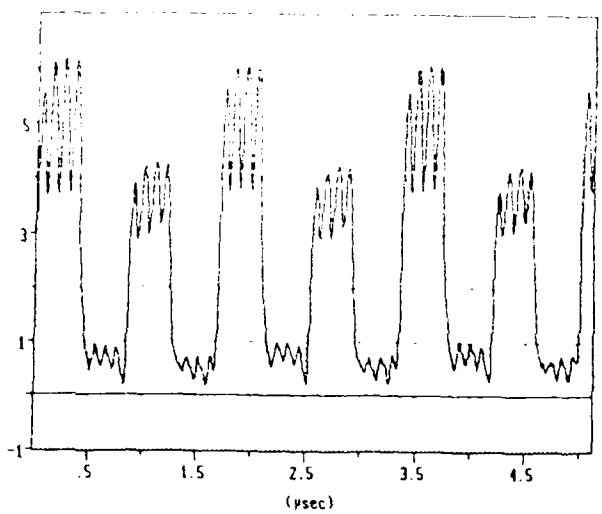
B.

Figure 9.3.1.26 - CD4013B QVC Waveforms on Input Node of Inverter 7
A. No RF
B. 5 MHz RF on Data Input Pin



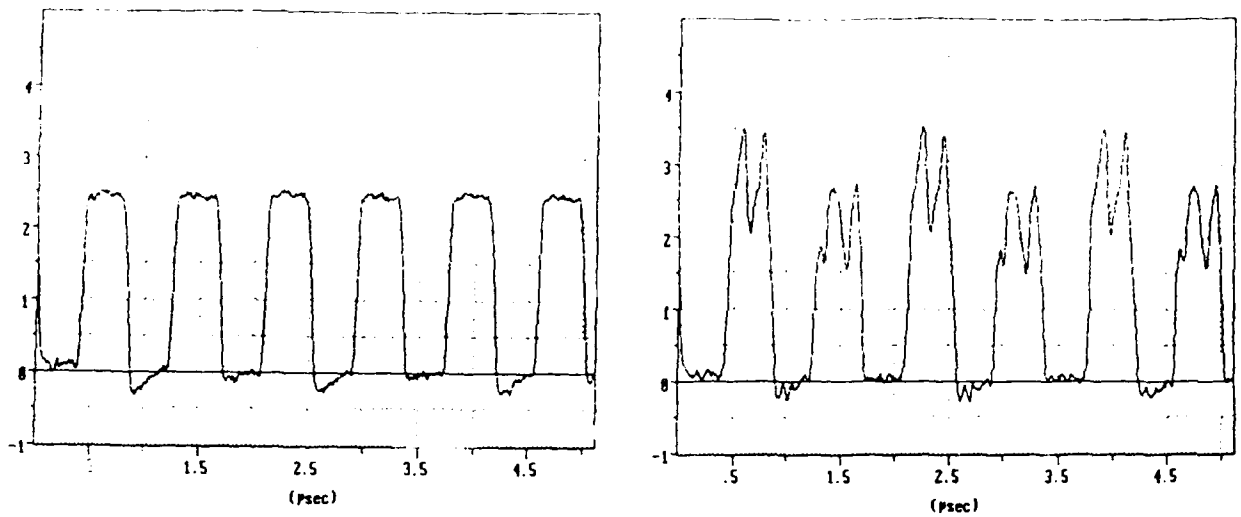
A.

B.



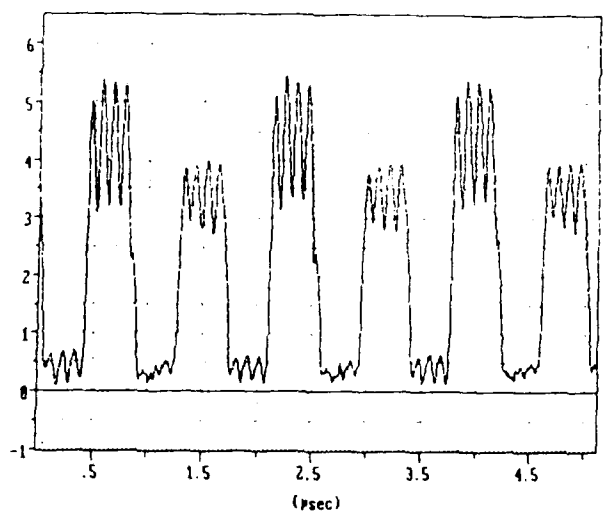
C.

Figure 9.3.1.27 - CD4013B QVC Waveforms on Output Node of Inverter 7
A. No RF
B. 5 MHz RF on Data Input Pin
C. 10 MHz RF on Data Input Pin



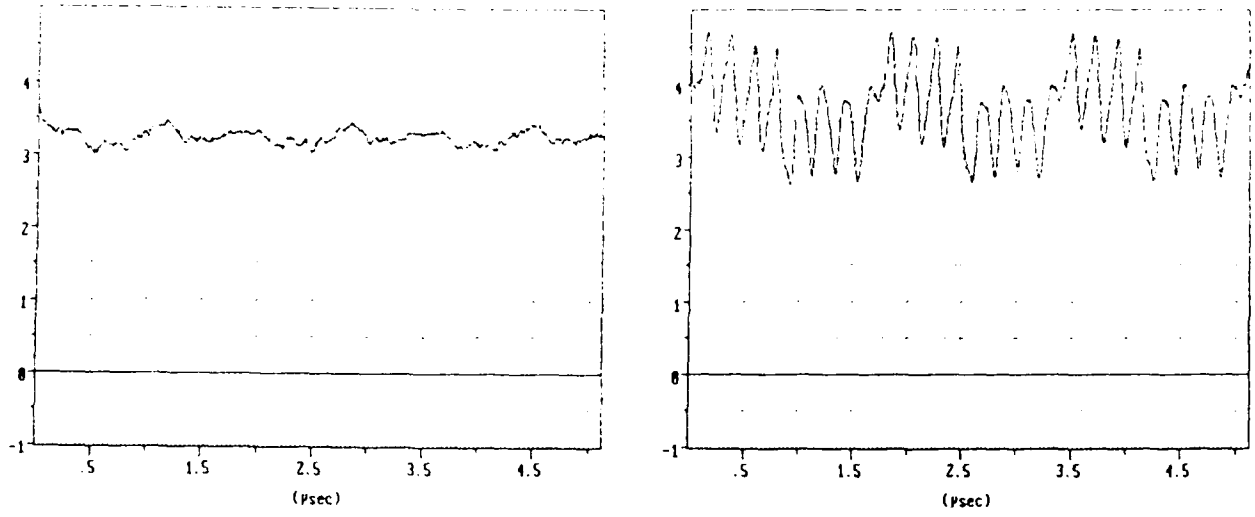
A.

B.



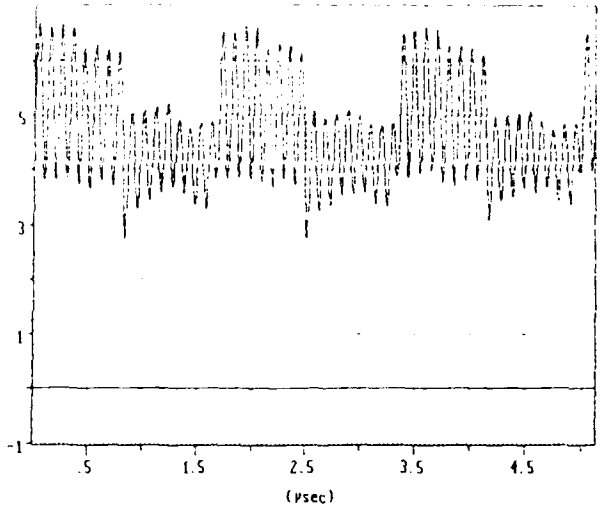
C.

Figure 9.3.1.28 - CD4013B QVC Waveforms on Output Node of Inverter 8
A. No RF
B. 5 MHz RF on Data Input Pin
C. 10 MHz RF on Data Input Pin



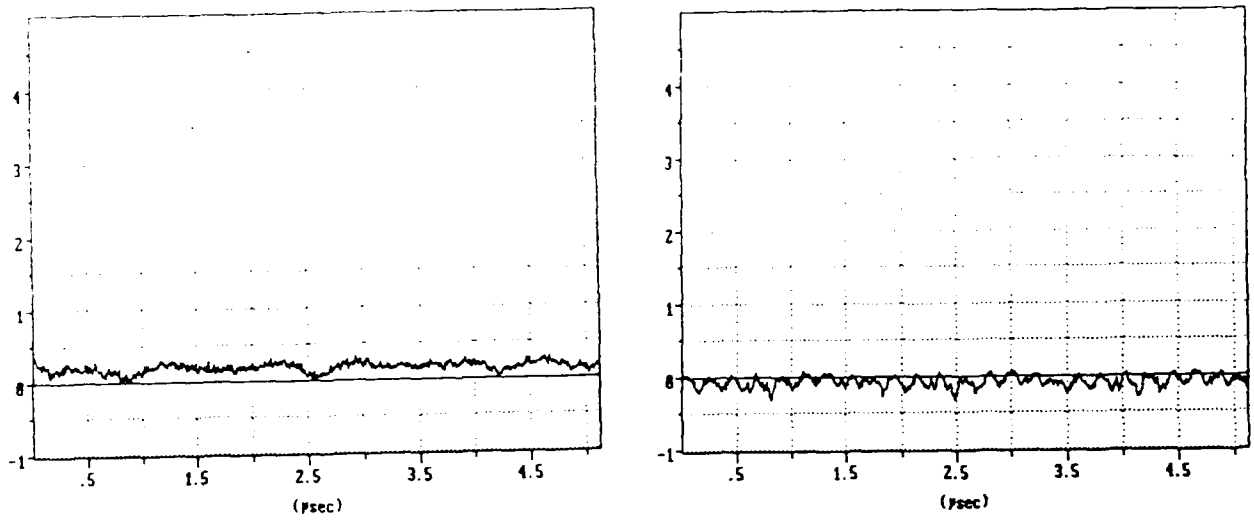
A.

B.



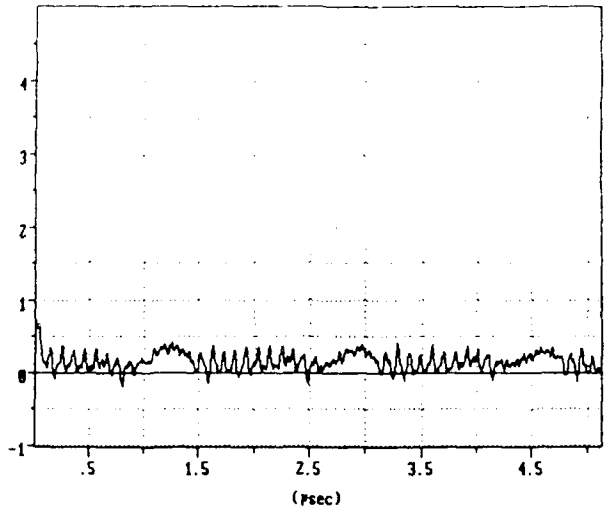
C.

Figure 9.3.1.29 - CD4013B QVC Waveforms on Vdd Node on Source of P-channel MOSFET of Inverter 11
A. No RF
B. 5 MHz RF on Data Input Pin
C. 10 MHz RF on Data Input Pin



A.

B.



C.

Figure 9.3.1.30 - CD4013B QVC Waveforms on Vss Node on Source of N-channel MOSFET of Inverter 11
A. No RF
B. 5 MHz RF on Data Input Pin
C. 10 MHz RF on Data Input Pin

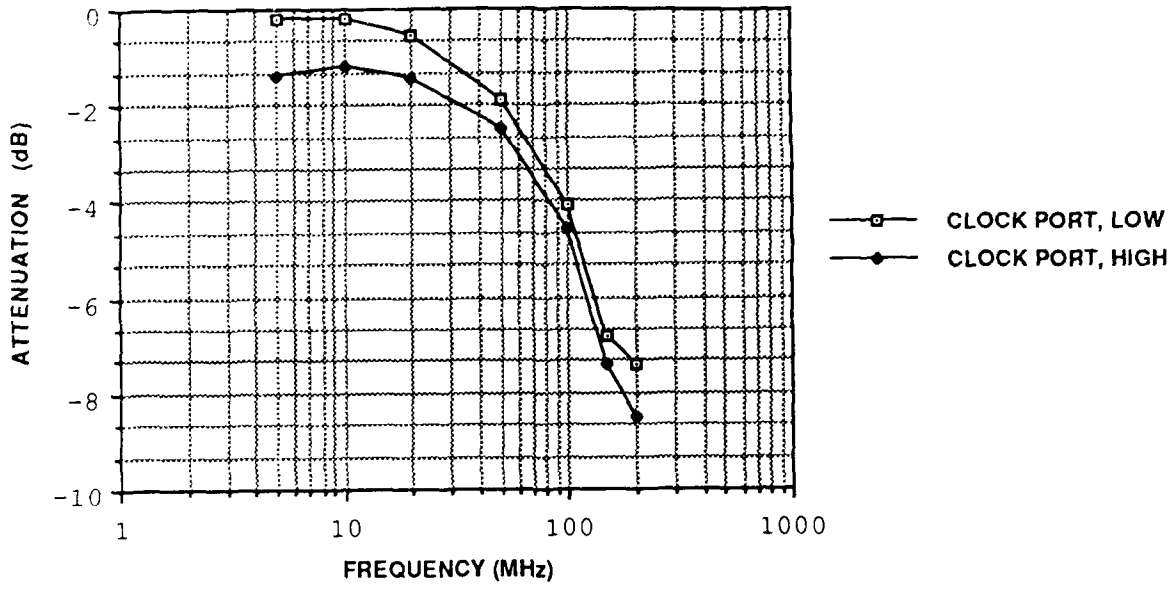
Voltage amplitude variations occurred with the QVC system between different physical locations. For instance, near the perimeter of the package or on metallization where residual glassivation was present, the amplitude was lower. Due to this condition and the limited bandwidth of the SEM QVC system, additional testing was required. Mechanical probing of the input structure was performed to measure the attenuation of the input signal, due to the input protection network, over frequency. Two Tektronix P6501 high frequency probes were used to obtain the signal levels at the bond pad and after the protect resistor on the data and clock inputs. Measurements were taken at 1 MHz, 5 MHz, 10 MHz, 50 MHz, 100 MHz, 150 MHz, and 200 MHz. The attenuation was measured on pin 3, clock, and pin 5, data, with both a high and low logic level. These are shown in Figure 9.3.1.31.

9.3.2 CD4585B QVC Measurements

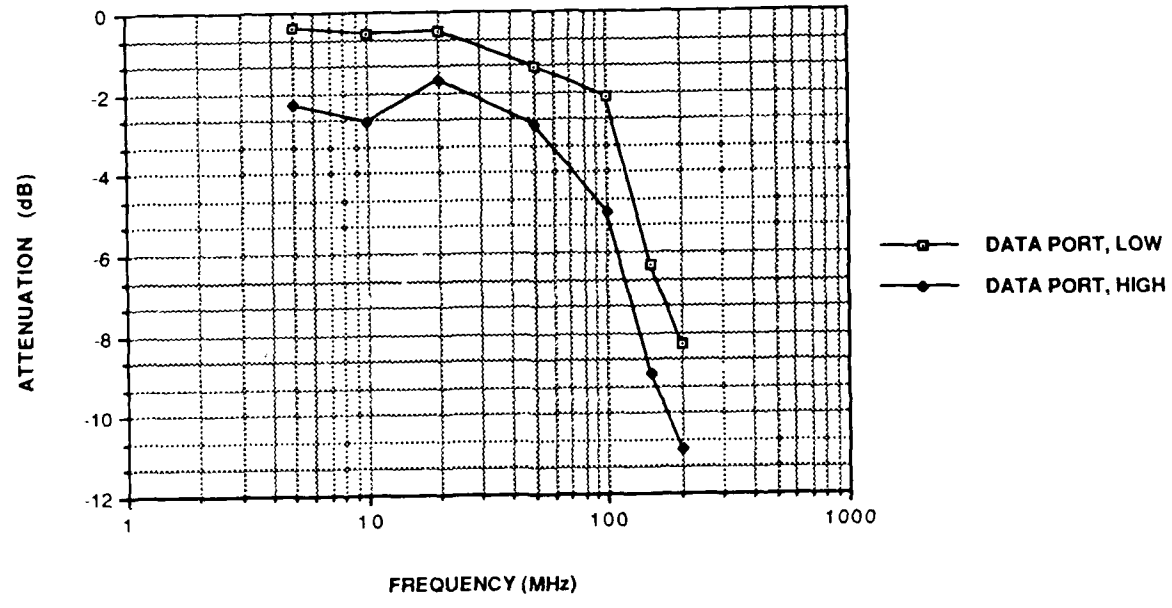
Measurements on the CD4585B were taken at internal nodes with no RF interference, with 1 MHz, 5 MHz, and 10 MHz RF interference on the B0 input. Waveforms were taken along the signal path, at internal Vdd and Vss contacts, and at traces adjacent to the input trace with the RFI.

Figure 9.3.2.1 provides the logic diagram for the CD4585B for easy reference when viewing the waveforms. Figures 9.3.2.2 - 9.3.2.5 show the waveforms taken on the oscilloscope of the B0 input and the A>B output under the four test conditions, i.e., no RF, and RF at 1 MHz, 5 MHz, and 10 MHz.

Figure 9.3.2.6 shows the QVC waveforms before the ESD protection network on the B0 input. Figure 9.3.2.7 shows the same waveforms after the ESD protection network at inverter 28 input node. The apparent difference in amplitude is due to the measuremnet system and not to an increase in the signal level.



A. Clock input



B. Data input

Figure 9.3.1.31 - CD4013B Input Protection Circuit Signal Attenuation Versus Frequency

Figure 9.3.2.8 shows the appearance of the waveforms on the output node of the first inverter, G28. Figure 9.3.2.9 shows the same waveforms on the output node of the second inverter, G29. The waveforms in Figures 9.3.2.7 and 9.3.2.9 should look the same since they have been inverted two times. It should be noted that the waveforms for "no RF" in Figures 9.3.2.8 and 9.3.2.9 were taken at a later time and are on a different scale than the other waveforms. They cannot be used for direct comparison. The waveforms with 1 MHz RF interference in Figures 9.3.2.7 and 9.3.2.9 look similar with some change of wave shape. The waveforms with 5 MHz and 10 MHz RF interference are being affected by the RF interference. The waveform with 10 MHz interference already has the appearance of the resulting output waveform.

Figures 9.3.2.10 - 9.3.2.14 show the waveforms at additional nodes through the circuit. The primary effect of these later gates is wave shaping.

The appearance of the waveforms at internal nodes continued changing further into the circuit at the lower frequencies than at the higher frequencies. With 10 MHz RF interference the waveforms changed little after going through two gates. With 5 MHz RF interference the waveforms changed little after going through three gates. With 1 MHz RF interference the waveforms were changing slightly through the entire circuit.

The appearance of Vdd and Vss at internal nodes was recorded with no RF and with 1 MHz RF interference (Figures 9.3.2.15 and 9.3.2.16). The appearance of an adjacent parallel metallization line was measured under these same two conditions (Figure 9.3.2.17). Some coupling of the RF signal is observed.

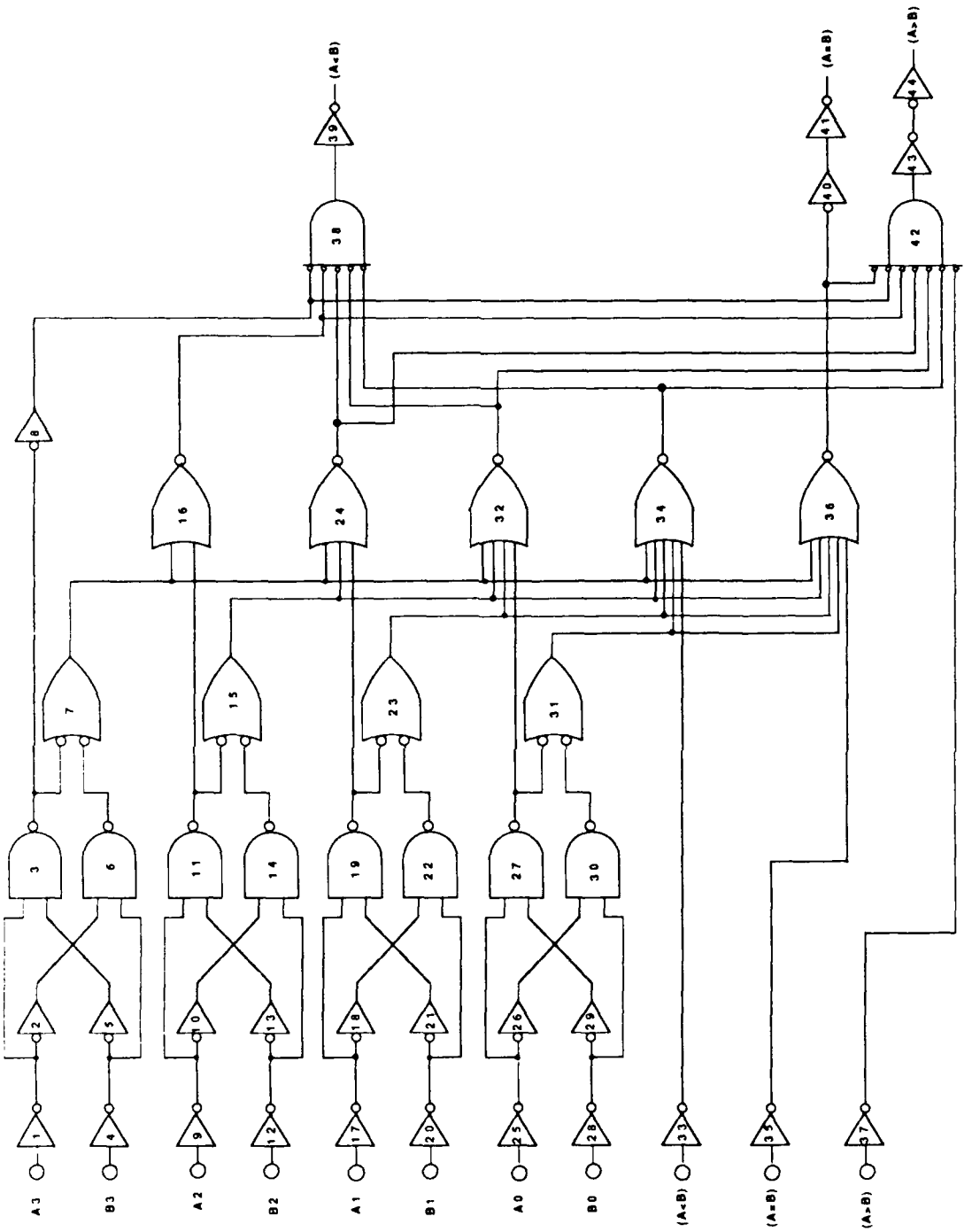


Figure 9.3.2.1 - CD4585B Logic Diagram
Note: Logic gates are numbered 1 through 44, inputs are on the left hand side, and outputs are on the right hand side.

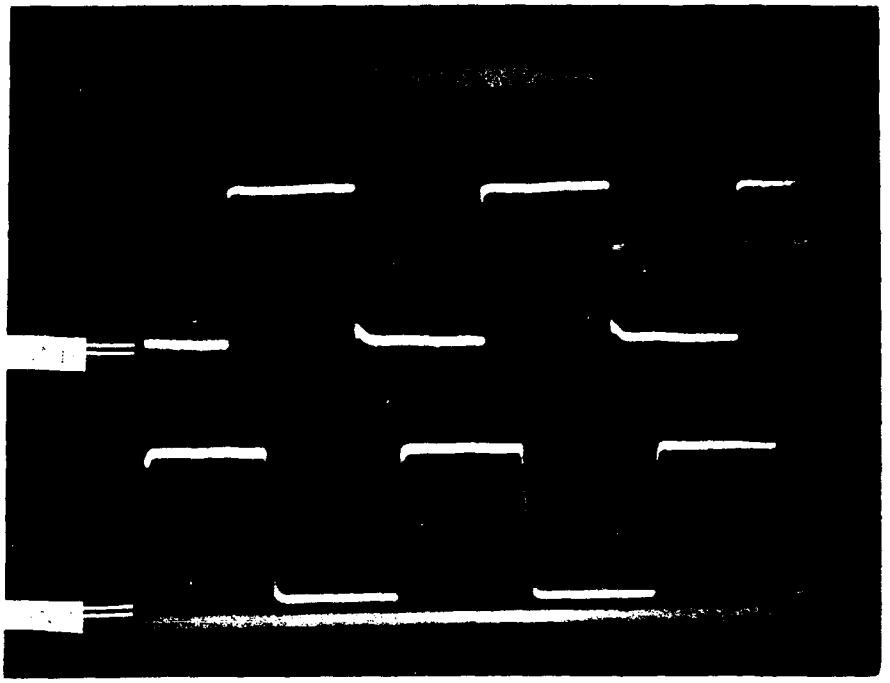


Figure 9.3.2.2 - CD4585B Oscilloscope Photograph, No RF
Top trace = B0 input
Bottom trace = Q output

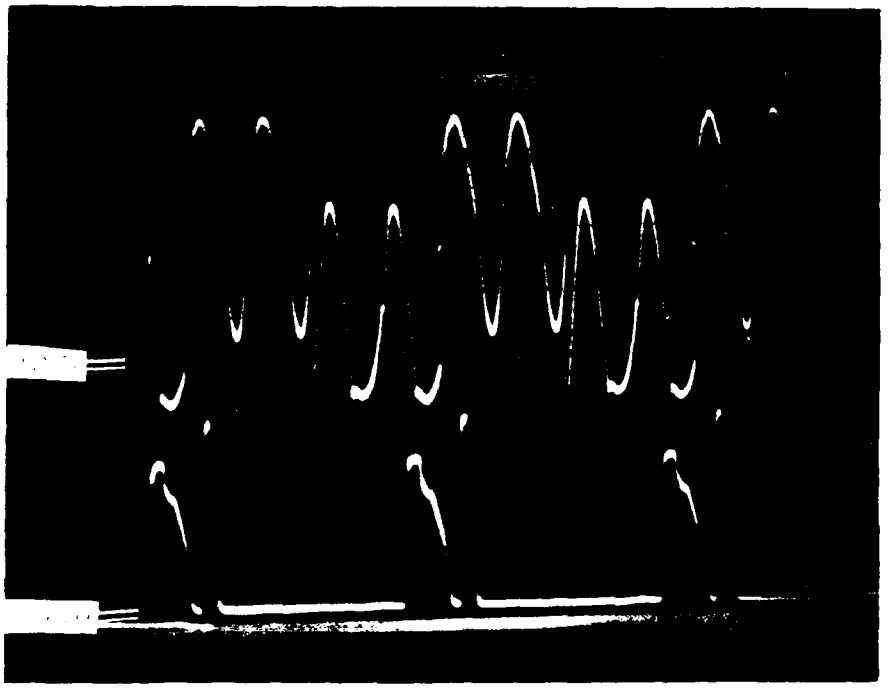


Figure 9.3.2.3 - CD4585B Oscilloscope Photograph
Top trace = B0 input with 1 MHz RF
Bottom trace = Q output

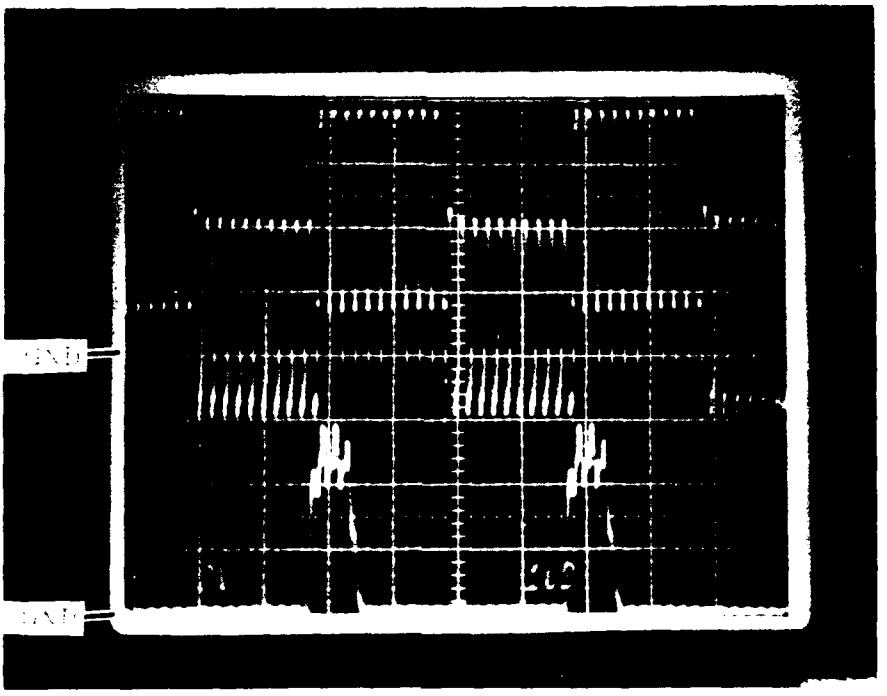


Figure 9.3.2.4 - CD4585B Oscilloscope Photograph
Top trace = B0 input with 5 MHz RF
Bottom trace = Q output

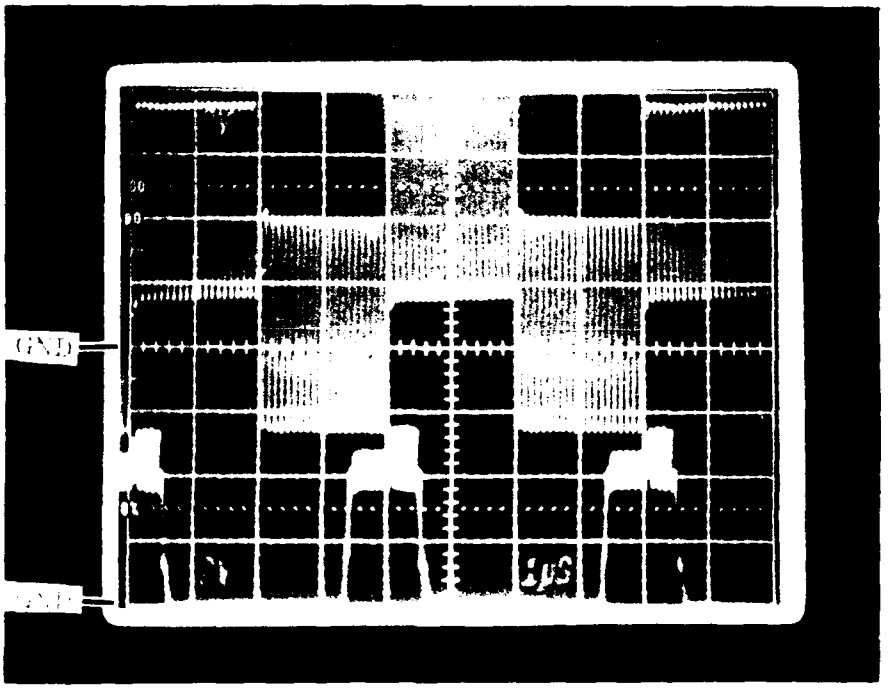


Figure 9.3.2.5 - CD4585B Oscilloscope Photograph
Top trace = B0 input with 10 MHz RF
Bottom trace = Q output

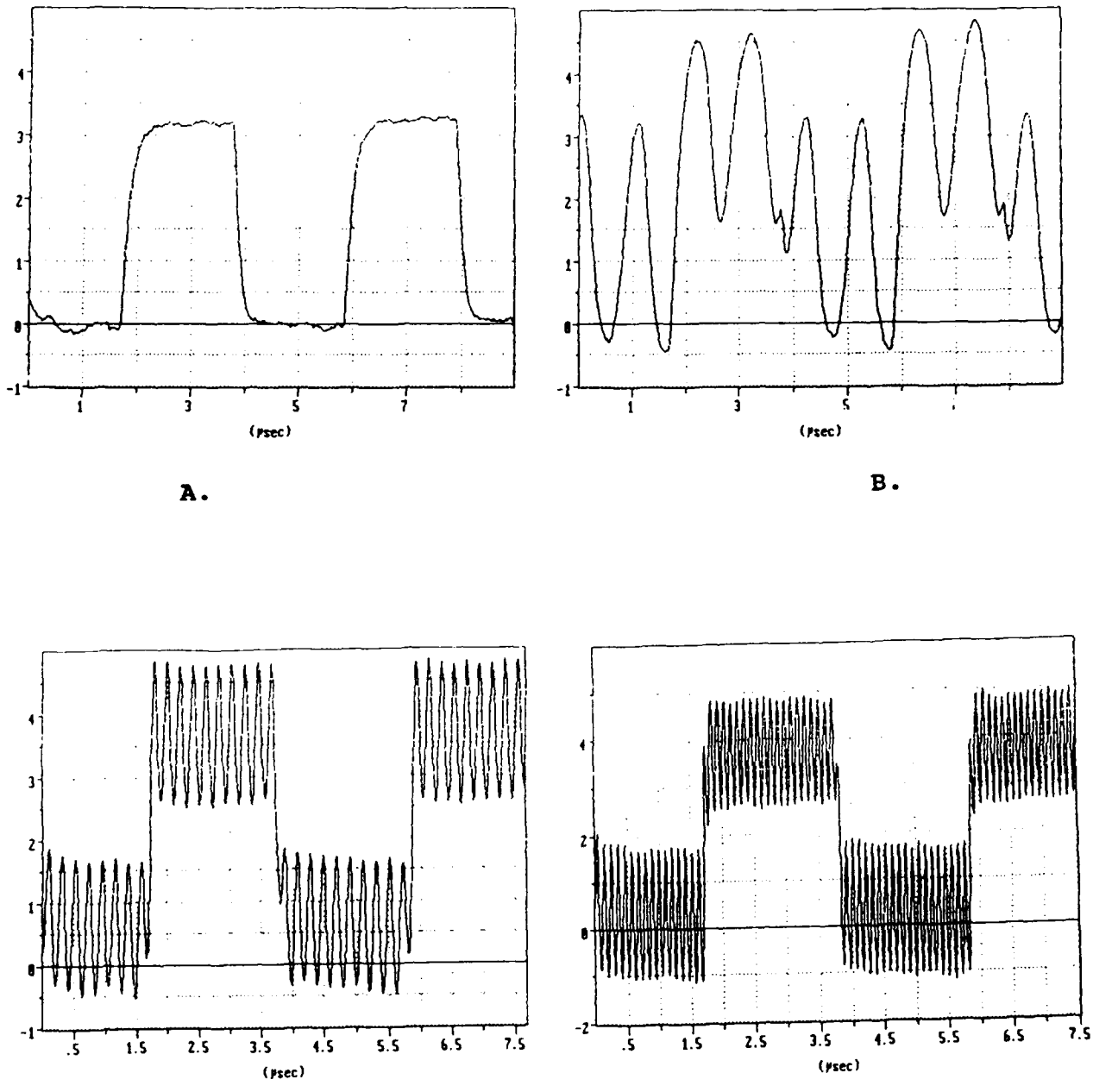
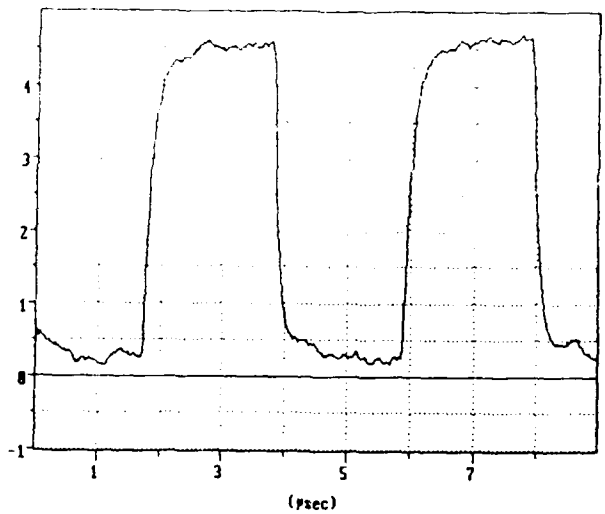
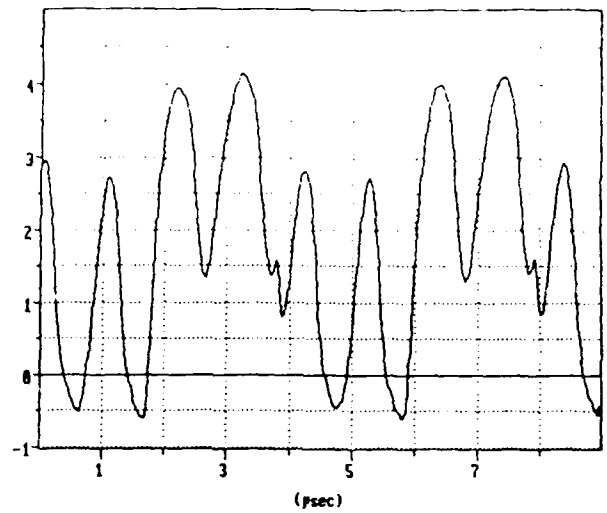


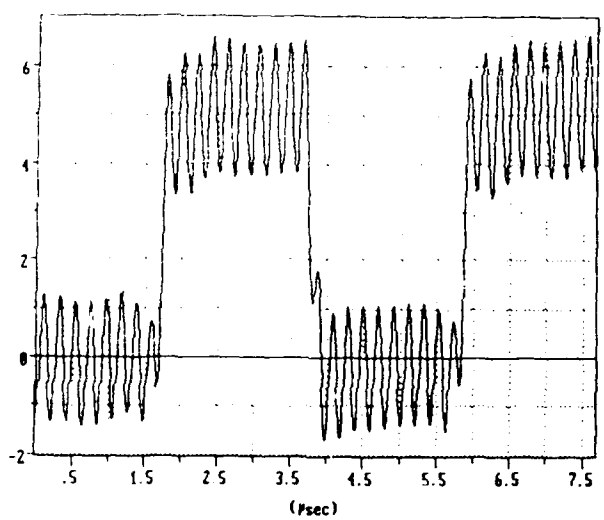
Figure 9.3.2.6 - CD4585B QVC Waveforms at B0 Input Pin Bond Pad Prior to ESD Network
A. No RF
B. 1 MHz RF on B0 Input Pin
C. 5 MHz RF on B0 Input Pin
D. 10 MHz RF on B0 Input Pin



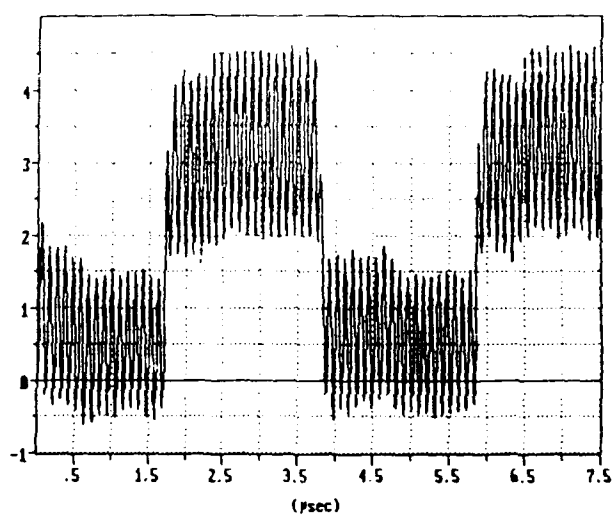
A.



B.

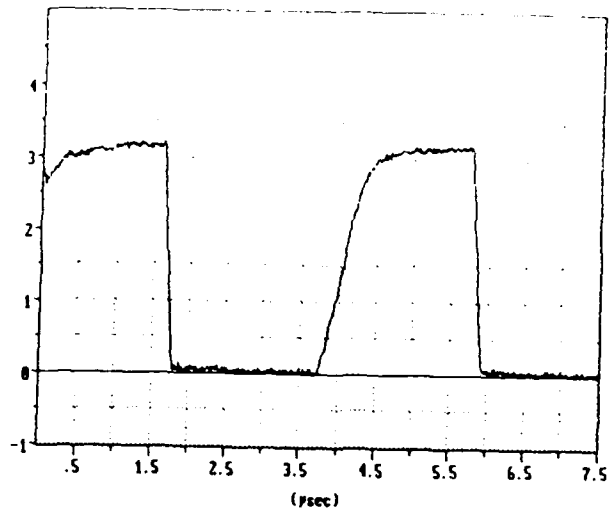


C.

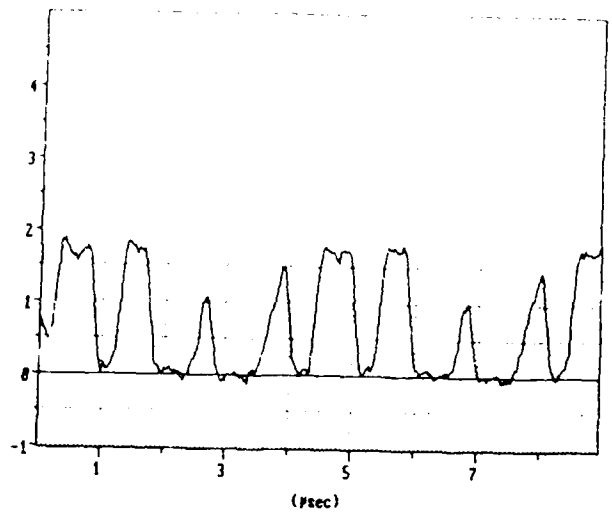


D.

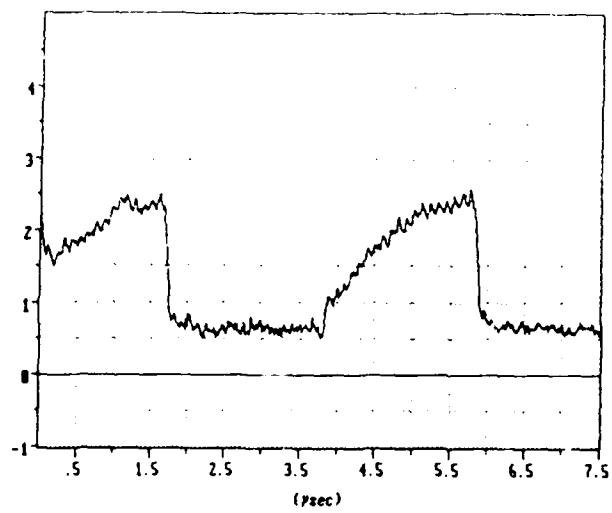
Figure 9.3.2.7 - CD4585B QVC Waveforms at Input Node of Inverter 28, B0 Input Signal Path
A. No RF
B. 1 MHz RF on B0 Input Pin
C. 5 MHz RF on B0 Input Pin
D. 10 MHz RF on B0 Input Pin



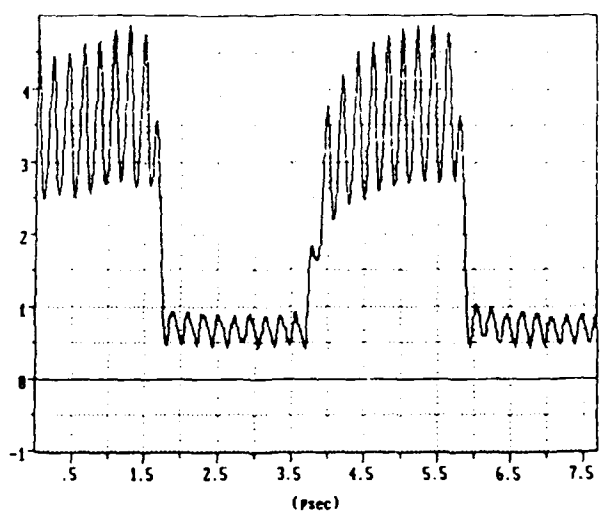
A.



B.



C.



D.

Figure 9.3.2.8 - CD4585B QVC Waveforms at Output Node of Inverter 28, B0 Input Signal Path
A. No RF
B. 1 MHz RF on B0 Input Pin
C. 5 MHz RF on B0 Input Pin
D. 10 MHz RF on B0 Input Pin

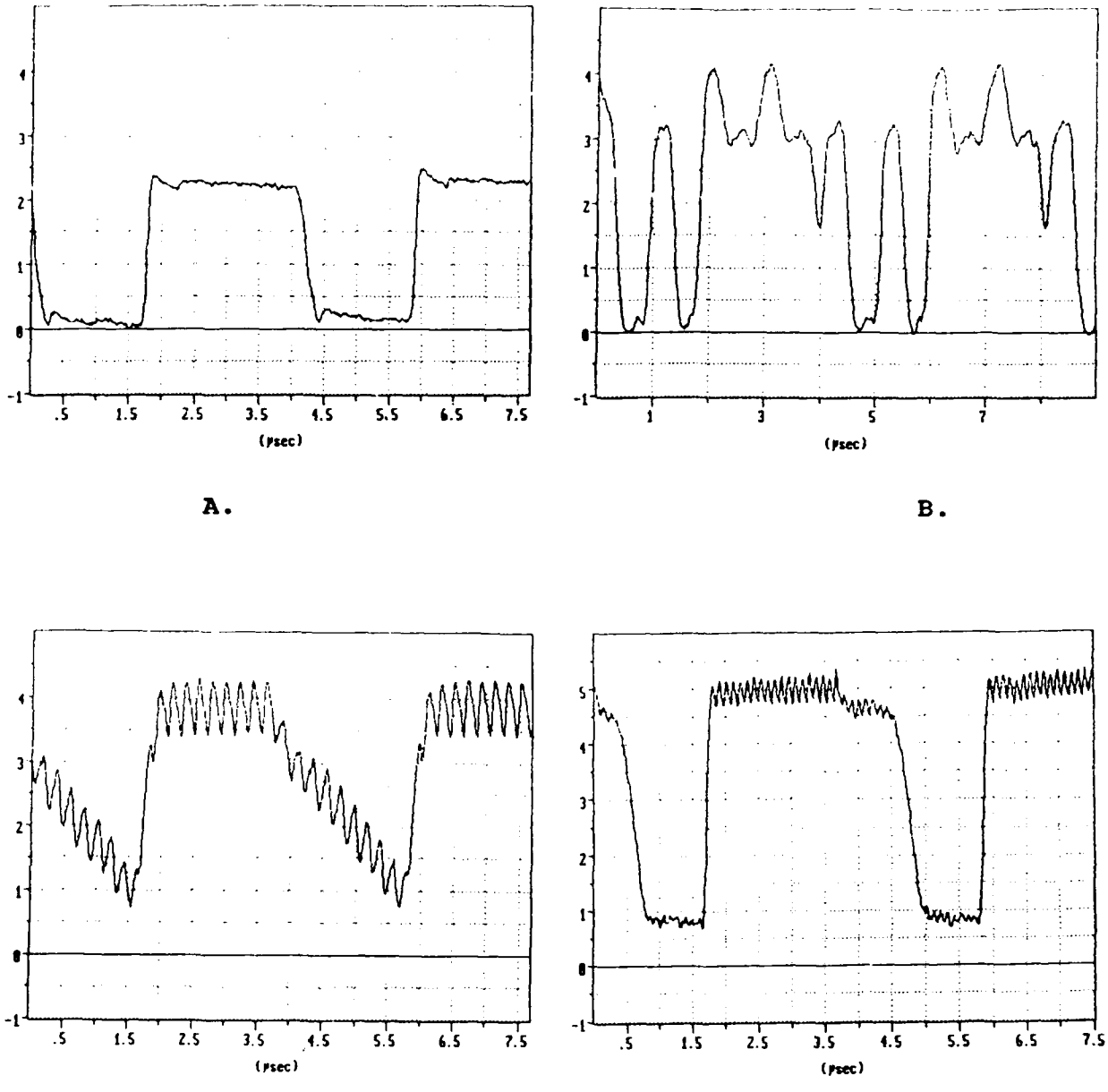
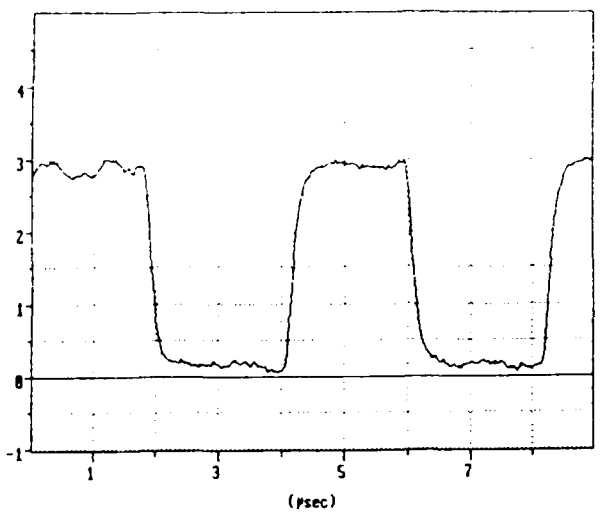
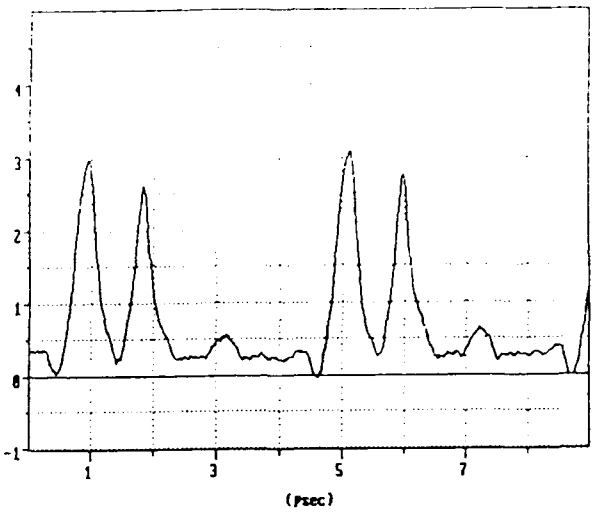


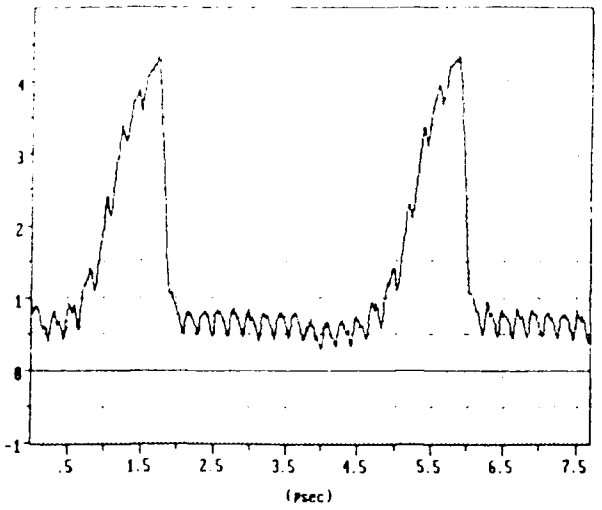
Figure 9.3.2.9 - CD4585B QVC Waveforms on Output Node of Inverter 29, B0 Input Signal Path
A. No RF
B. 1 MHz RF on B0 Input Pin
C. 5 MHz RF on B0 Input Pin
D. 10 MHz RF on B0 Input Pin



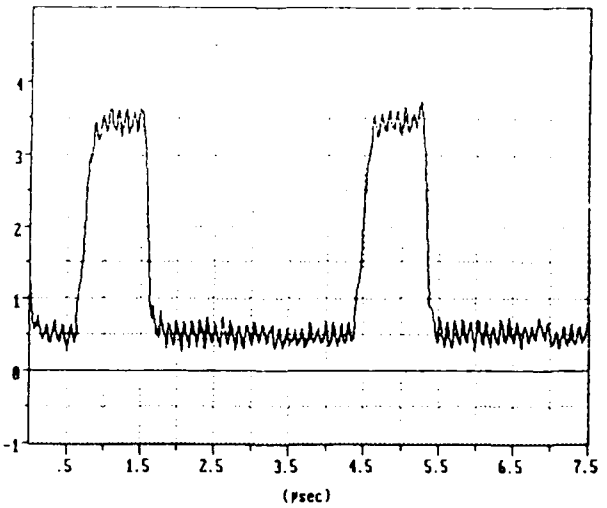
A.



B.

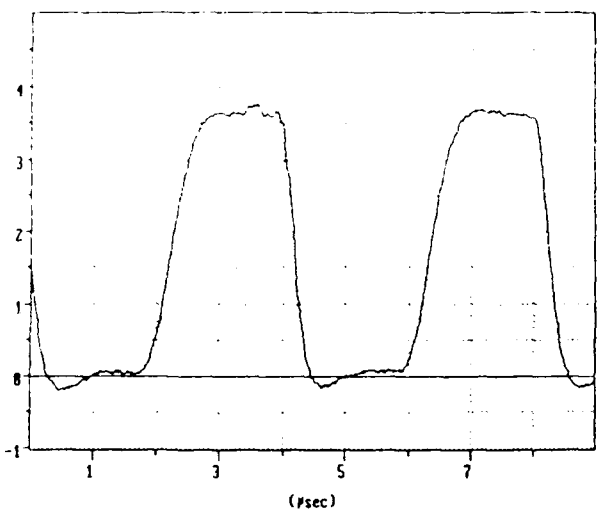


C.

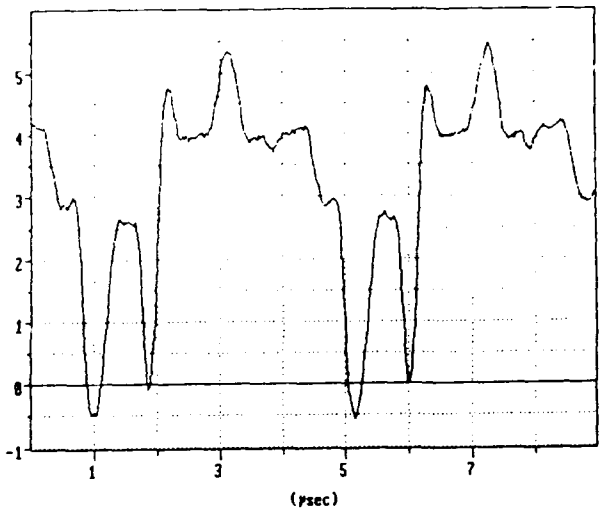


D.

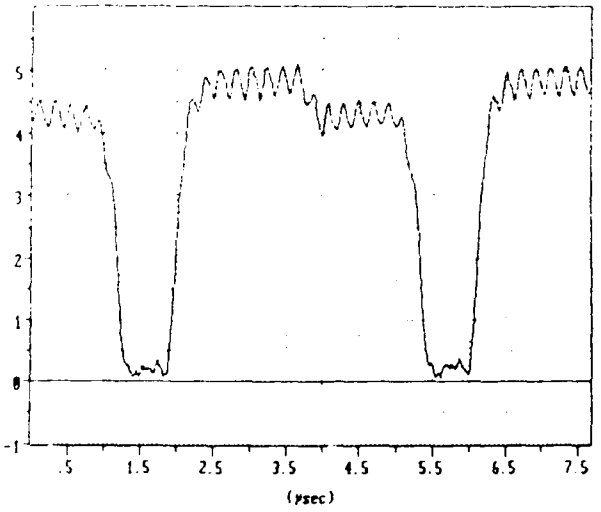
Figure 9.3.2.10 - CD4585B QVC Waveforms on Output Node of NAND Gate 27, B0 Input Signal Path
A. No RF
B. 1 MHz RF on B0 Input Pin
C. 5 MHz RF on B0 Input Pin
D. 10 MHz RF on B0 Input Pin



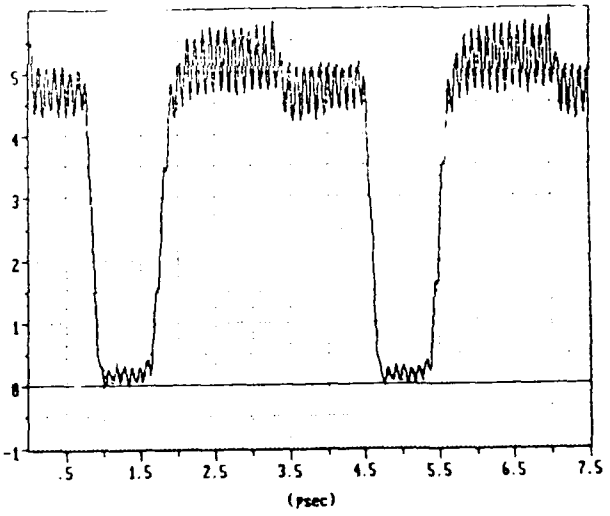
A.



B.



C.



D.

Figure 9.3.2.11 - CD4585B QVC Waveforms on Output Node of NOR Gate 32, B0 Input Signal Path
A. No RF
B. 1 MHz RF on B0 Input Pin
C. 5 MHz RF on B0 Input Pin
D. 10 MHz RF on B0 Input Pin

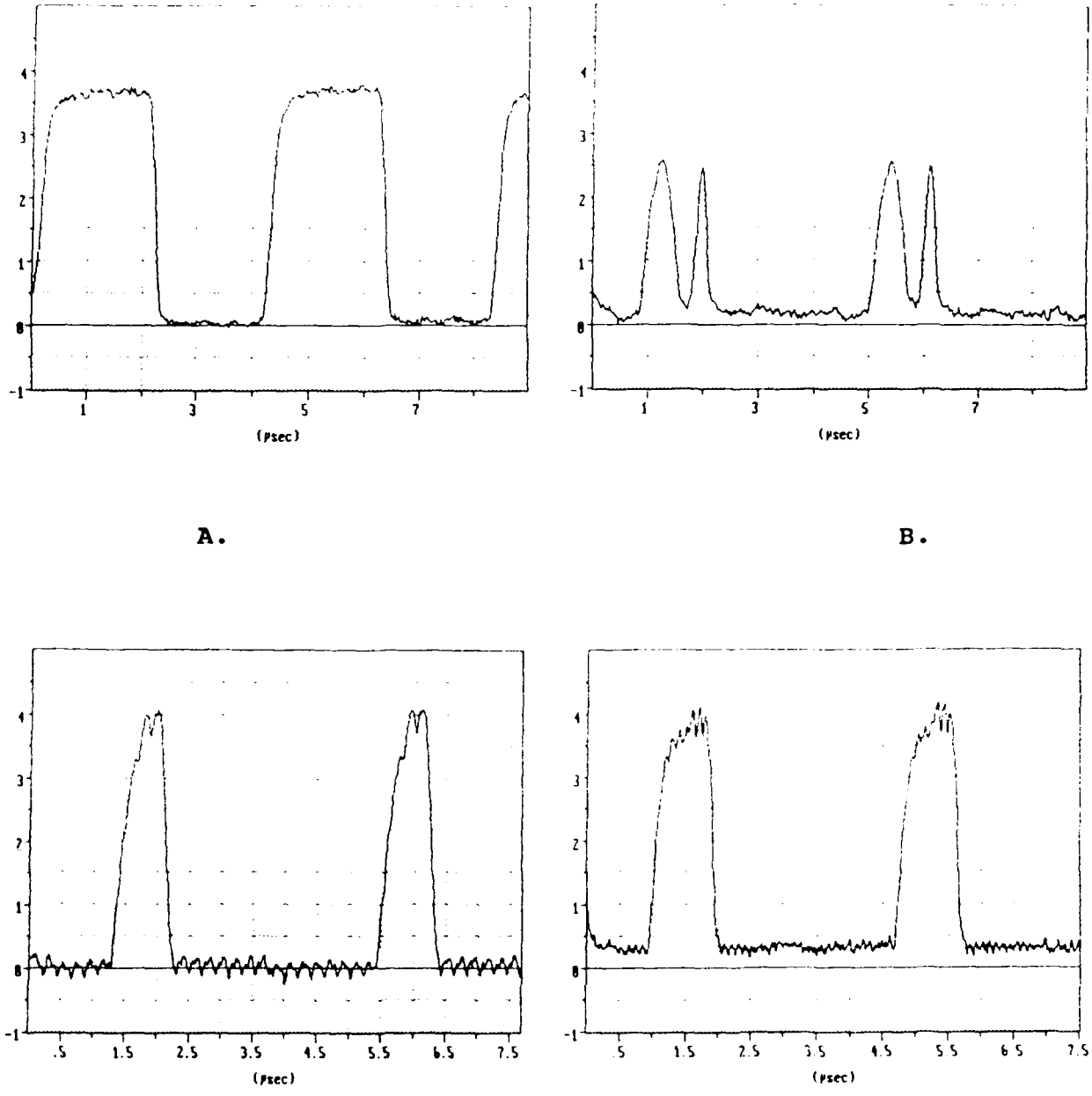


Figure 9.3.2.12 - CD4585B QVC Waveforms on Output Node of AND Gate 42
A. No RF
B. 1 MHz RF on B0 Input Pin
C. 5 MHz RF on B0 Input Pin
D. 10 MHz RF on B0 Input Pin

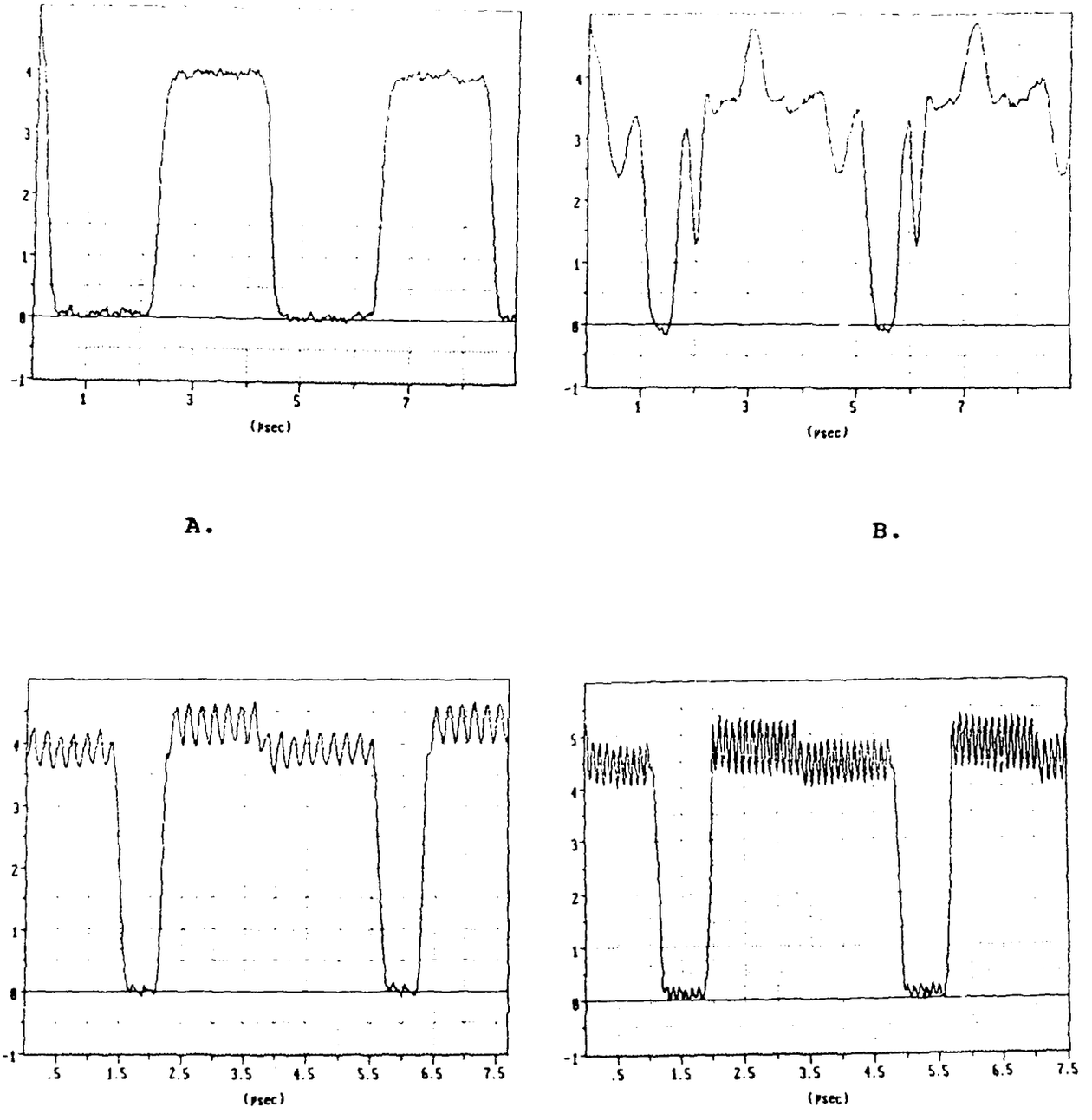
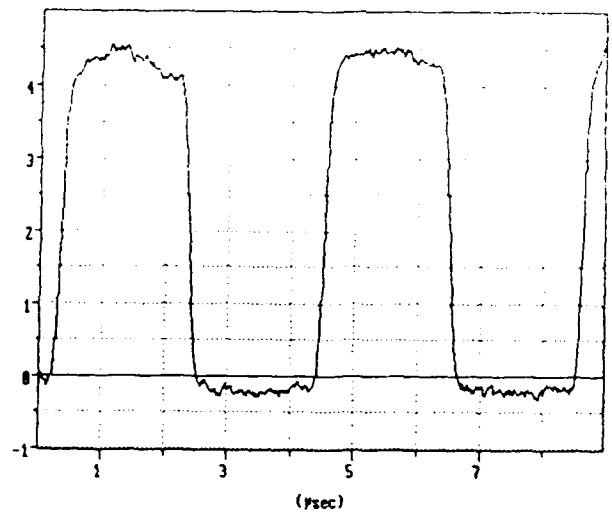
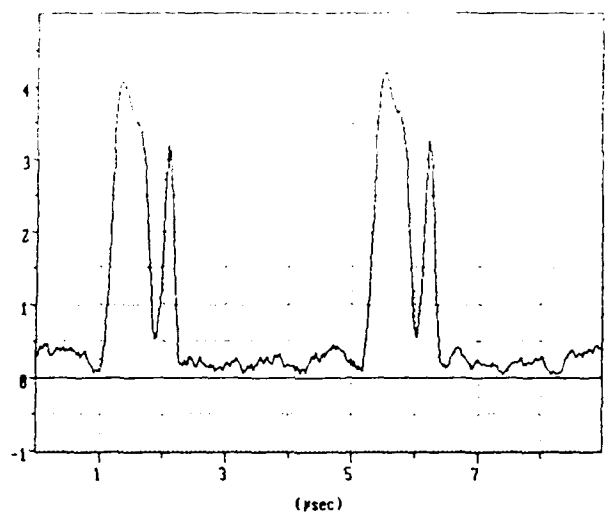


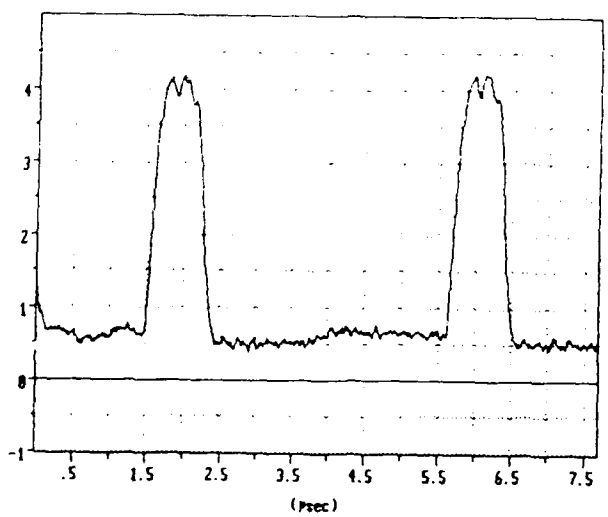
Figure 9.3.2.13 - CD4585B QVC Waveforms on Output Node of Inverter 43
A. No RF
B. 1 MHz RF on B0 Input Pin
C. 5 MHz RF on B0 Input Pin
D. 10 MHz RF on B0 Input Pin



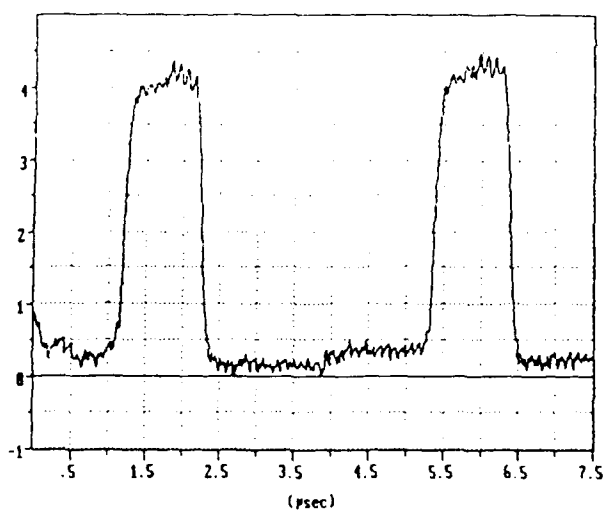
A.



B.

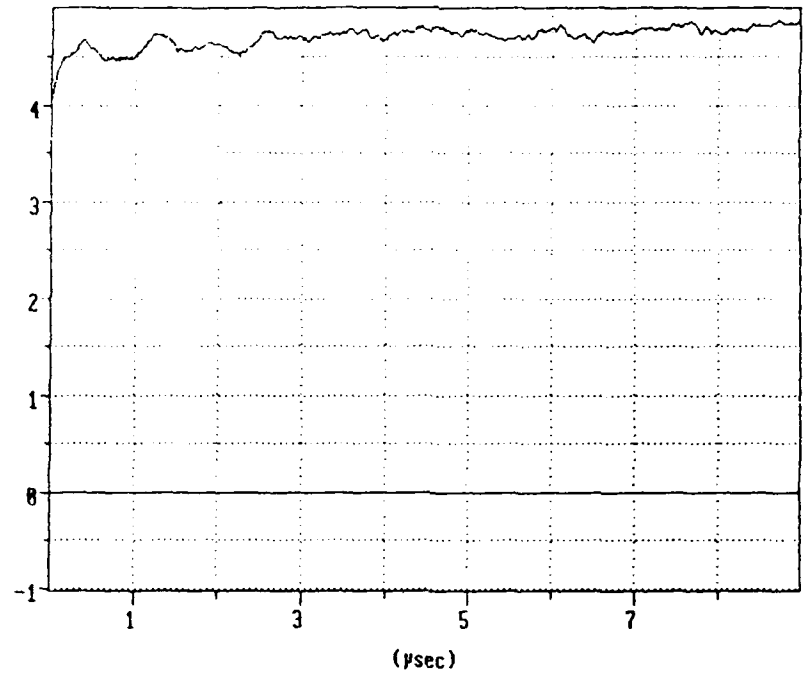


C.

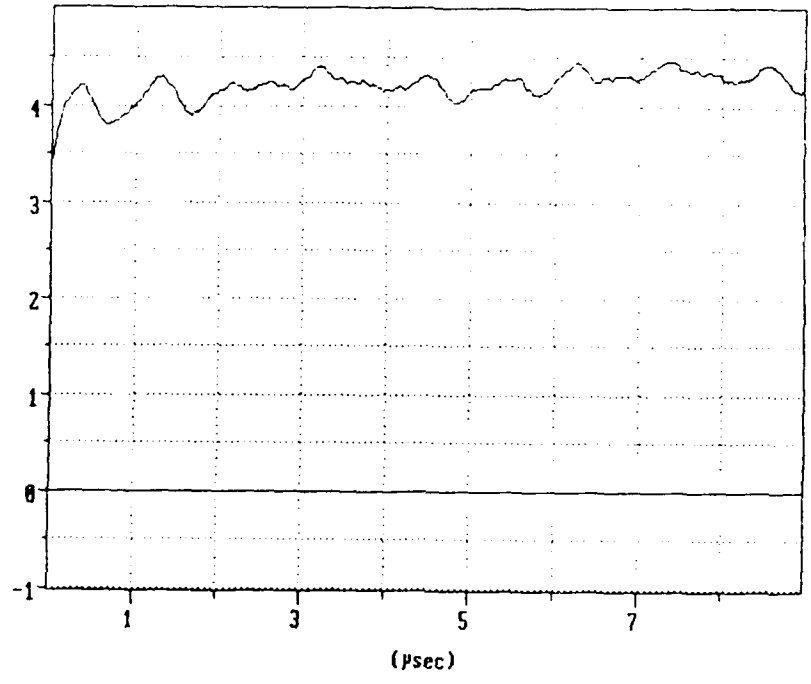


D.

Figure 9.3.2.14 - CD4585B QVC Waveforms on Bond Pad of A>B Output Pin
A. No RF
B. 1 MHz RF on B0 Input Pin
C. 5 MHz RF on B0 Input Pin
D. 10 MHz RF on B0 Input Pin

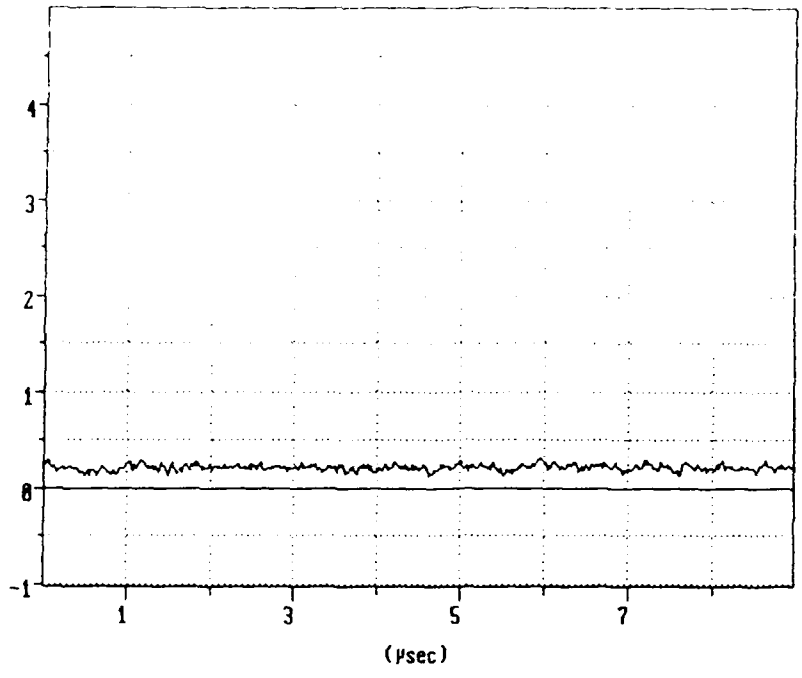


A.

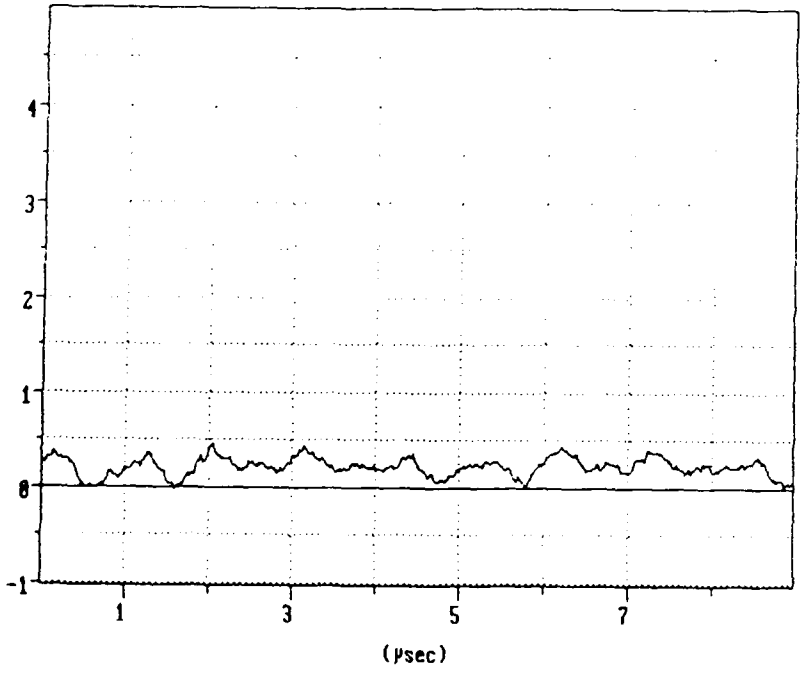


B.

Figure 9.3.2.15 - CD4585B QVC Waveforms on Vdd Node on Source of P-channel MOSFET of Inverter 29
A. No RF
B. 1 MHz RF on B0 Input Pin

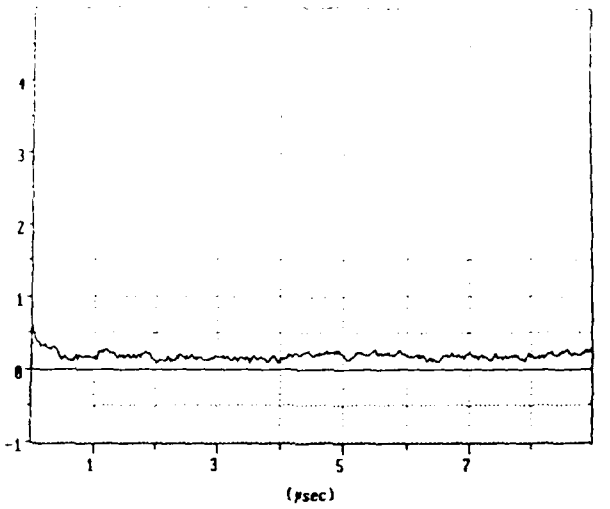


A.

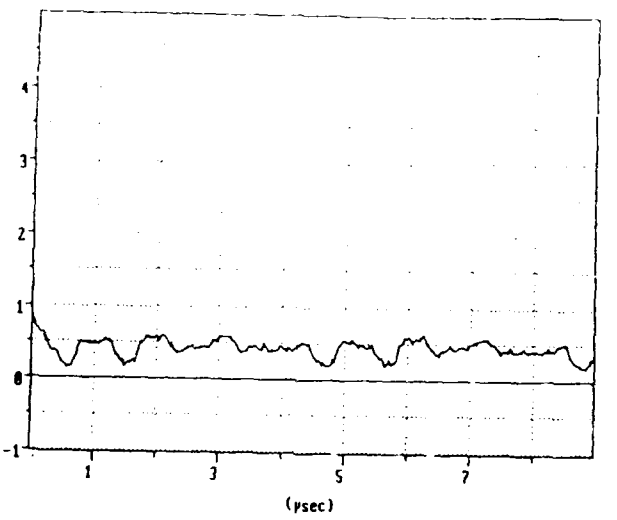


B.

Figure 9.3.2.16 - CD4585B QVC Waveforms on Vss Node on Source of N-channel MOSFET of Inverter 29
A. No RF
B. 1 MHz RF on B0 Input Pin



A.



B.

Figure 9.3.2.17 - CD4585B QVC Waveforms on Metallization Trace Between Gate 23 and Gate 36, For Exact Location Reference the Arrow in Figure 6.3.5
A. No RF
B. 1 MHz RF on B0 Input Pin, Producing RF Signal on Parallel Metallization Trace Between Gate 27 and Gate 32

9.3.3 SN54LS85 QVC Measurements

Limited QVC measurements were taken on the SN54LS85. The logic diagram is shown in Figure 9.3.3.1 for easy reference to the waveforms. Oscilloscope waveforms are shown in Figures 9.3.3.2 and 9.3.3.3 of the B0 input and the A>B output with no RF and with 5 MHz RF interference. Three sets of internal node waveforms were acquired and are shown in Figures 9.3.3.4 - 9.3.3.6. Wave shaping of the signal occurs through the stages as shown. The output node of logic section 16 has the appearance of the oscilloscope output waveform.

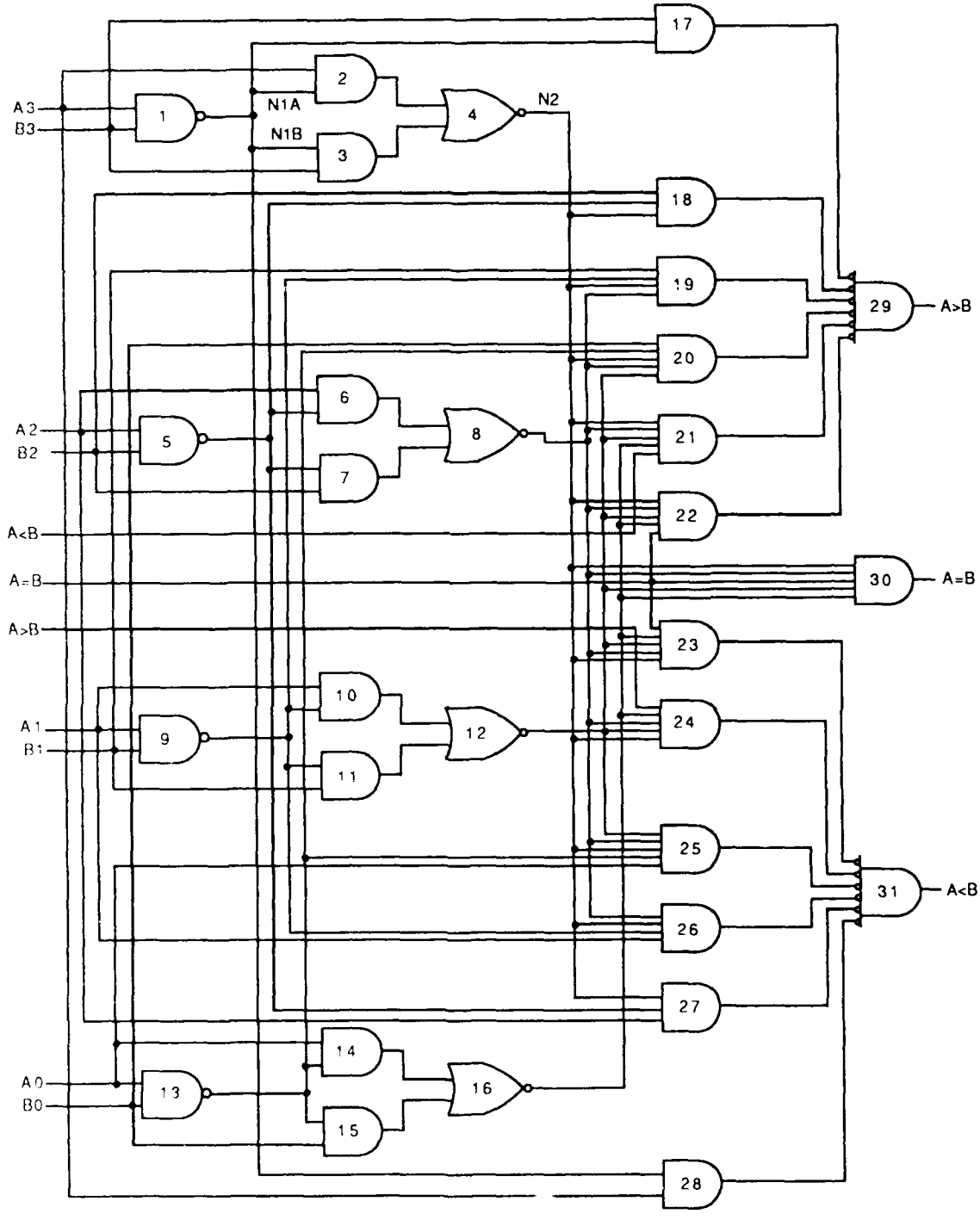


Figure 9.3.3.1 - SN54LS85 Logic Diagram
Note: Logic Gates are Numbered 1 Through 31, Inputs are on the Left Hand Side, and Outputs are on the Right Hand Side

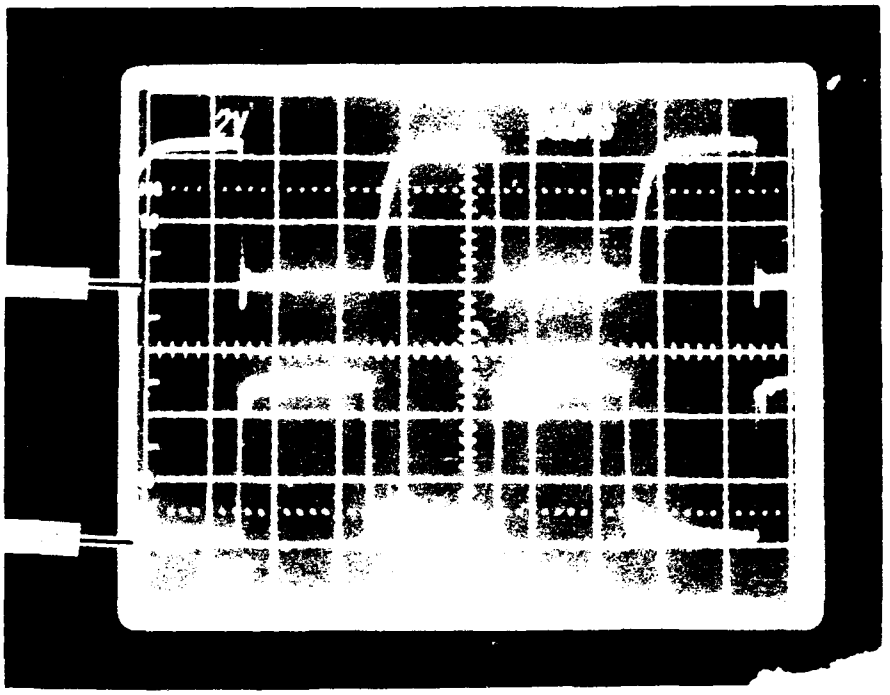


Figure 9.3.3.2 - SN54LS85 Oscilloscope Photograph, No RF
Top trace = A>B output
Bottom trace = B0 input

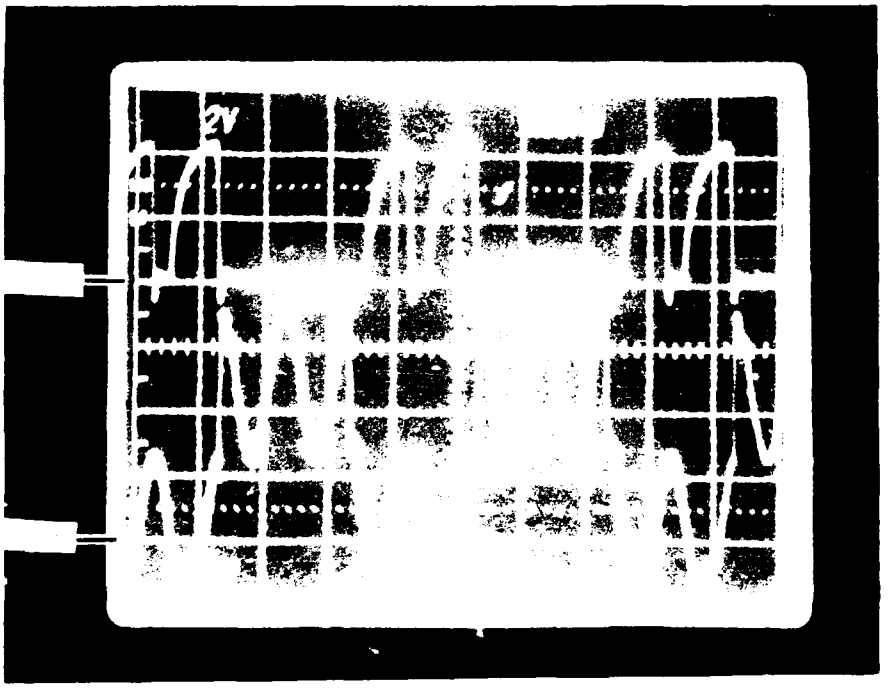
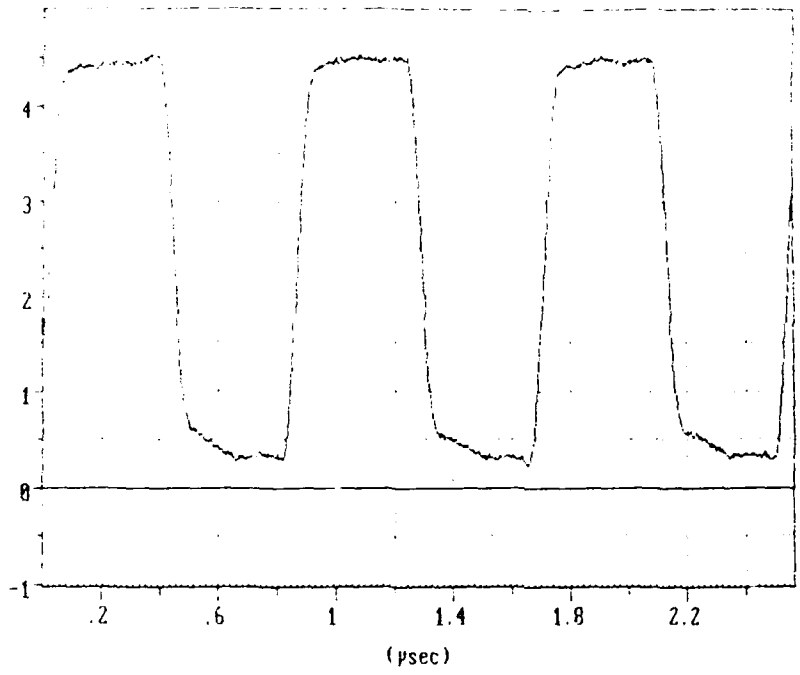
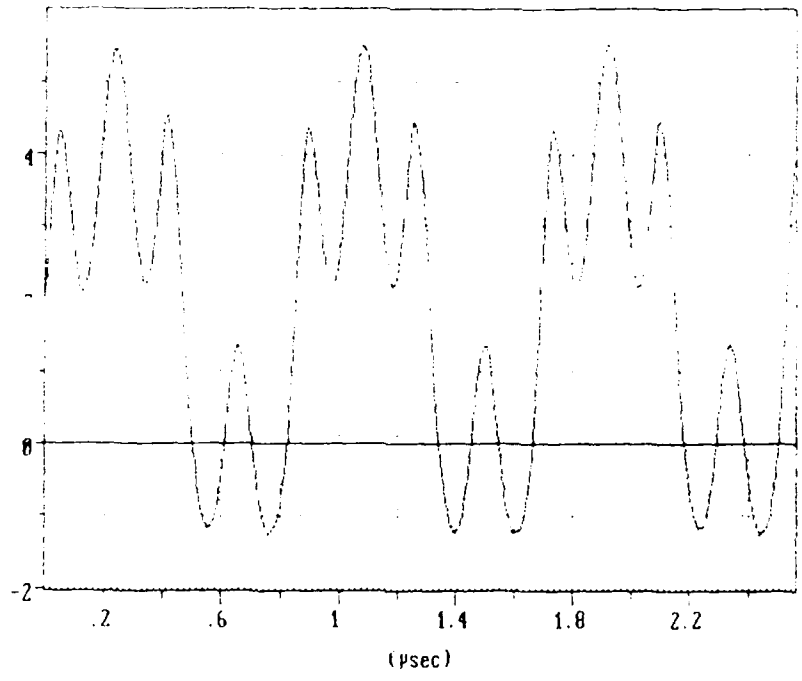


Figure 9.3.3.3 - SN54LS85 Oscilloscope Photograph
Top trace = A>B output
Bottom trace = B0 input with 5 MHz RF

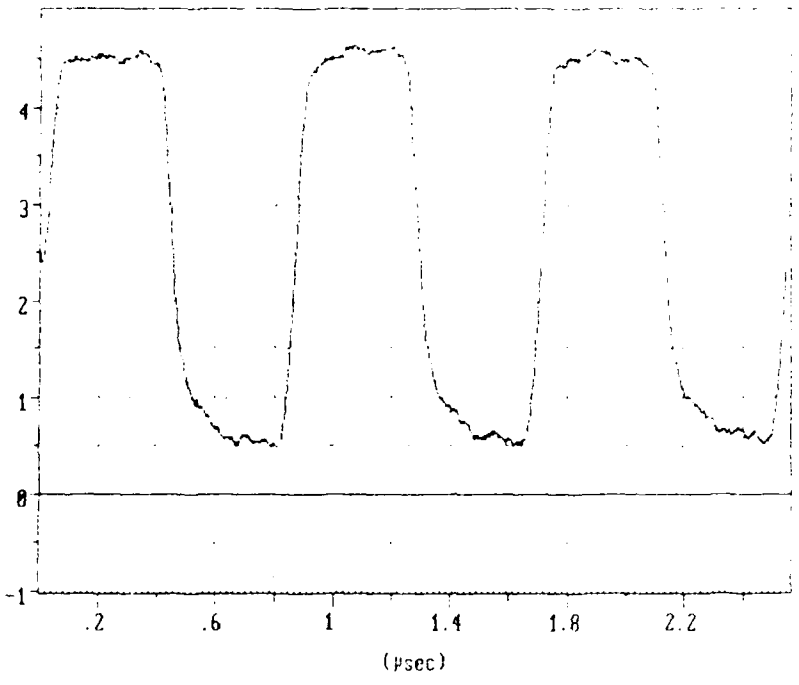


A.

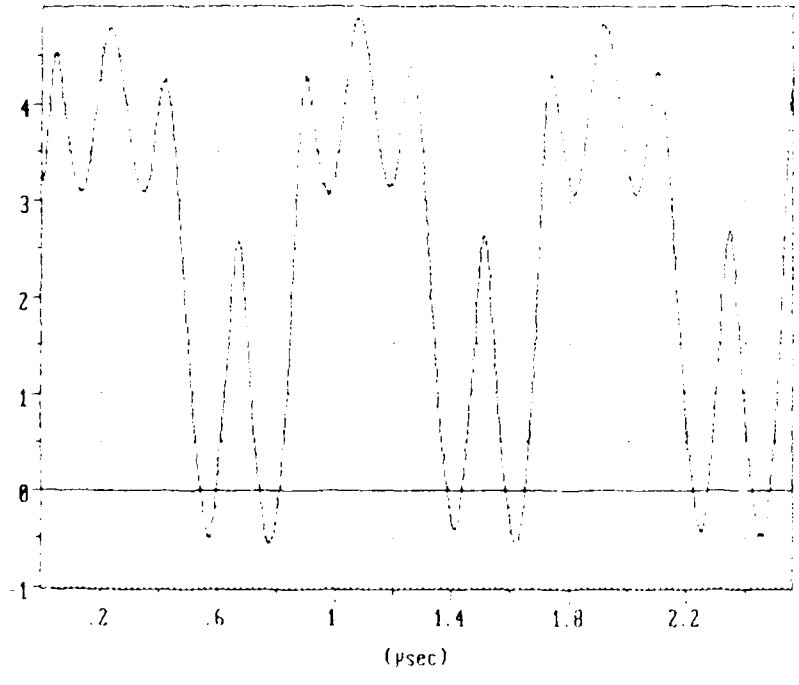


B.

Figure 9.3.3.4 - SN54LS85 QVC Waveforms at B0 Input Pin Bond Pad
A. No RF
B. 5 MHz RF on B0 Input Pin

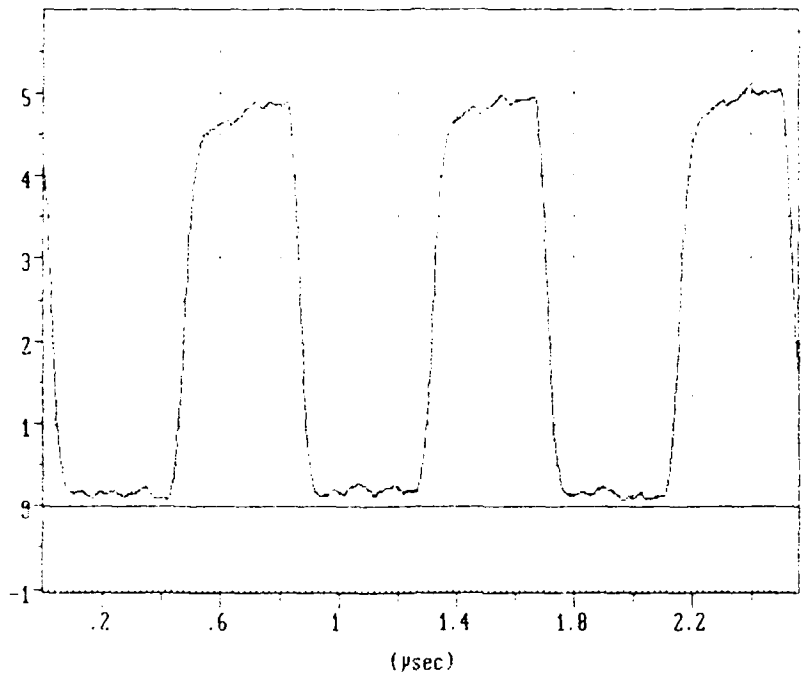


A.

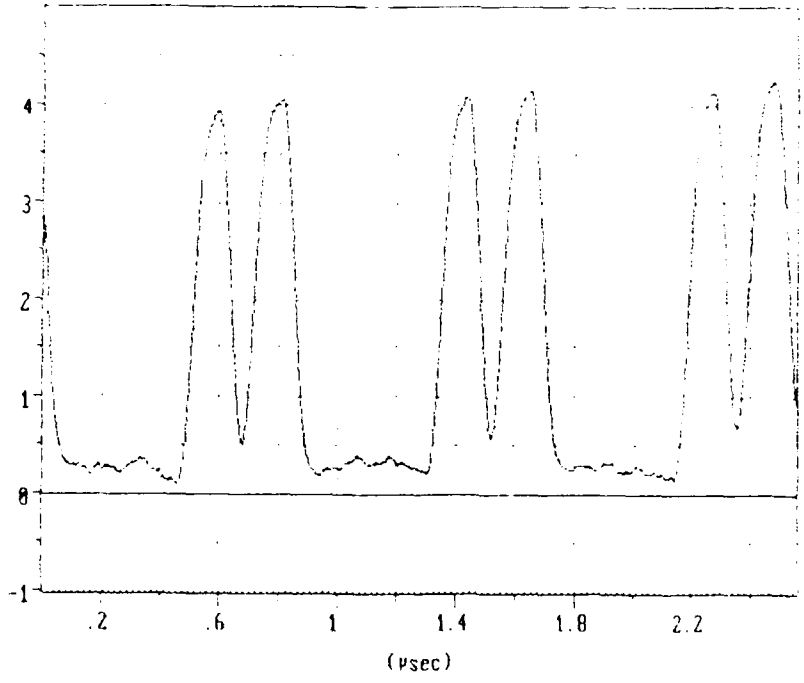


B.

Figure 9.3.3.5 - SN54LS85 QVC Waveforms on Output Node of AND Gate 15, B0 Input Signal Path
A. No RF
B. 5 MHz RF on B0 Input Pin



A.



B.

Figure 9.3.3.6 - SN54LS85 QVC Waveforms on Output Node of NOR Gate 16, B0 Input Signal Path
A. No RF
B. 5 MHz RF on B0 Input Pin

10.0 CONCLUSIONS

This study provided excellent RF upset susceptibility data on the CD4013B, CD4585B, SN54ALS74A, and SN54LS85 integrated circuits. The SEM QVC system enabled measurement of waveforms at internal nodes of the integrated circuits. Thus, providing information on the effects of RFI on the circuit behavior. A discussion of the conclusions of this study along with recommendations for additional analyses are included in this section.

10.1 RF Upset Susceptibility

Excellent results were obtained for the RF upset susceptibility of the four device types. All of these devices exhibit relatively low upset power levels indicating that RF upset is a valid concern. Conclusions from the RF upset data include:

1) The peak-to-peak voltage level required for upset on the power pins (Vdd and Vcc) was low at low frequencies, increased at mid-frequencies and then decreased at the higher frequencies (ref. Figure 8.7.1.1).

2) The power level required for upset on the power pins was relatively constant versus frequency for the Schottky devices and steadily increased with frequency for the CMOS devices, due to the low pass filtering by the input protect network (ref. Figure 8.7.1.2)

3) The peak-to-peak voltage level required for upset on the signal input pins (data, clock, B0, and B3) increased with frequency on the CMOS devices, was relatively constant on the SN54ALS74A clock input, and peaked at 5 MHz for the remainder of the Schottky inputs (ref. Figure 8.7.3.1).

4) The power level required for upset on the signal input pins increased with frequency on the CMOS and SN54ALS74A devices but was relatively constant versus frequency for the SN54LS85 devices (ref. Figure 8.7.3.2).

5) The input most sensitive to RF upset was the clock input on the SN54ALS74A devices. The input circuit for this pin does not contain a series resistor and the clock circuitry responds to the rising edge of the input signal. These factors produced an input that caused circuit upset in the 1 to 3 volt peak-to-peak range.

6) The integrated circuit that was the least susceptible to RF upset was the SN54LS85. This is due to the facts that there was no edge-triggered input, such as on the SN54ALS74A, and that the input conductance was higher on this device type than on the other three device types.

10.2 Input Conductance Data

The differences between the appearance of the curves for the peak-to-peak voltage data and the appearance of the curves for the power level data are primarily due to the input conductance versus frequency. The input conductance is the latter portion of the equation used to calculate upset power. This equation is:

$$P_{ave} = (1/8)Vpp^2\{R/(R^2+X^2)\}.$$

Where P_{ave} is average power, Vpp is peak-to-peak voltage, R is the real part of the complex input impedance, and X is the imaginary part of the complex input impedance. The input conductance (G) is $R/(R^2+X^2)$.

The input conductance curves had the following attributes:

1) Relatively simple and quick to obtain.

2) Provides information on order of magnitude of power required for upset versus frequency for a given device type.

3) Provides comparison between technologies versus frequency.

4) Provides a technique for selecting inputs to be used for additional RF upset voltage measurements.

5) Can be measured up to a frequency of 1 GHz with the an HP4191A Impedance Analyzer.

10.3 SEM QVC Measurements

The quantitative voltage contrast technique on the scanning electron microscope is an excellent method for obtaining voltage waveforms at internal nodes on integrated circuits, within certain constraints. These internal waveform measurements are essential for understanding RFI effects. The following summarizes these attributes and limitations:

1) The SEM QVC measurement technique provides a non-loading non-interfering voltage waveform acquisition capability.

2) The glass passivation layer could be successfully removed from the surface of the IC's to allow the SEM QVC measurements without effecting their RF upset characteristics.

3) Interface connectors and fixturing were able to provide access to the IC's in the SEM chamber for the RF testing.

4) The maximum frequency of the RFI that could be acquired with the system was approximately 20 MHz. Therefore, the Schottky devices could not be measured above their normal operating frequency.

5) Examination of the waveforms at an output pin, for a circuit that was subjected to RFI, is not adequate for understanding the internal effects. For instance, two frequencies of RFI may produce similar output pin responses and the voltage waveforms at internal points may be significantly different.

10.4 Additional Testing

Additional RF upset testing is necessary to provide data for integrated circuit manufacturers to decrease the susceptibility of their circuits to RF upset. The information is also important for system design considerations. Recommendations and difficulties related to this additional testing follows:

1) A combiner circuit that can be used in the GHz range needs to be designed. The combiner used for this study was limited to about 200 MHz and a significantly different design will be required to test at the frequencies necessary for the faster technologies.

2) A voltage measurement technique with higher bandwidth is required. Two possibilities are the electro-optic laser prober and a probe utilizing the multiphoton photoelectric effect. These optical techniques are being developed and may provide the picosecond or sub-picosecond measurement capability necessary for GHz testing. The first technique requires an electro-optic material such as GaAS. Circuits manufactured with this technology are of great interest, making this a viable alternative.

3) Low power, high speed complex circuits such as VHSIC, VLSIC, ULSIC, and MIMIC require RF characterization. The systems in which these circuits are used become so complex that it is very difficult to assure EMC. Testing of the circuits is also a formidable task but is easier than testing at the system level and also provides quantitative component susceptibility data.

4) High impedance, high frequency mechanical probes can be used for additional input circuit characterization. These have a bandwidth of 750 MHz and can be used to gain information on input circuit effects and how these relate to device upset susceptibility.

This study has provided a significant amount of information on integrated circuit RF upset susceptibility. It has also shown that additional studies are warranted with new combiner designs and new measurement techniques for more complex circuits.

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APPENDIX A.1 DEVICE DATA SHEETS

CD4013B Types

CMOS Dual 'D'-Type Flip-Flop

High Voltage Types (20 Volt Rating)

The RCA CD4013B consists of two identical, *independent data type flip flops*. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

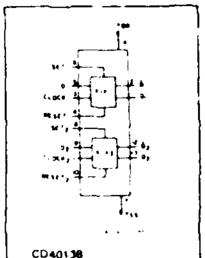
The CD4013B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features

- Set Reset capability
- Static flip-flop operation – retains state indefinitely with clock level either "high" or "low"
- Medium-speed operation – 16 MHz (typ.) clock toggle rate at 10V
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range, 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range) 1 V at V_{DD}=5 V; 2 V at V_{DD}=10 V; 2.5 V at V_{DD}=15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Registers, counters, control circuits



CD4013B
FUNCTIONAL DIAGRAM

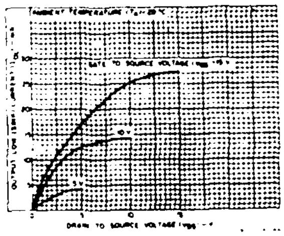


Fig. 1 – Typical output low (sink) current characteristics

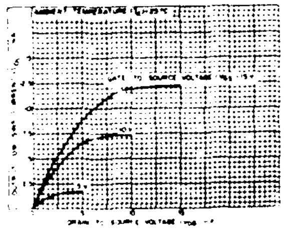


Fig. 2 – Minimum output low (sink) current characteristics

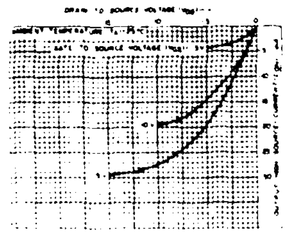


Fig. 3 – Typical output high (source) current characteristics

RECOMMENDED OPERATING CONDITIONS

At T_A = 25°C Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN	MAX	
Supply Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V
Data Setup Time t_S	5	40	–	ns
	10	20		
	15	15		
Clock Pulse Width t_W	5	140	–	ns
	10	60		
	15	40		
Clock Input Frequency f_{CL}	5	dc	3.5	MHz
	10		8	
	15		12	
Clock Rise or Fall Time t_{rCL}, t_{fCL}*	5		[illegible]	μs
	10		6	
	15		2	
Set or Reset Pulse Width t_W	5	180		ns
	10	80		
	15	50		

*If more than one unit is cascaded in a parallel clocked operation, t_{rCL} should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, K, H Pkgs Values at −40, +25, +85 Apply to E Pkgs							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	40	+85	+125	Min	+25 Typ	Max	
Quiescent Device Current I_{DD} Max	-	0,5	5	1	1	30	30		0.02	1	μA
	-	0,10	10	2	2	60	60		0.02	2	
	-	0,15	15	4	4	120	120		0.02	4	
		0,20	20	20	20	600	600		0.04	20	
Output Low (Sink) Current I_{OL} Min	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1		mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6		
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8		
Output High (Source) Current I_{OH} Min	4.6	0.5	5	0.64	0.61	0.42	0.36	0.51	1		
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2		
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6		
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8		
Output Voltage Low-Level V_{OL} Max		0.5	5	0.05				-	0	0.05	V
	-	0,10	10	0.05				-	0	0.05	
	-	0,15	15	0.05				-	0	0.05	
Output Voltage High-Level V_{OH} Min	-	0.5	5	4.95				4.95	5	-	
	-	0,10	10	9.95				9.95	10	-	
		0,15	15	14.95				14.95	15		
Input Low Voltage V_{IL} Max	0.5,4.5	-	5	1.5				-	-	1.5	V
	1.9	-	10	3				-	-	3	
	1.5,13.5	-	15	4				-	-	4	
Input High Voltage V_{IH} Min	0.5,4.5	-	5	3.5				3.5	-	-	
	1.9	-	10	7				7	-	-	
	1.5,13.5	-	15	11				11	-	-	
Input Current I_{IN} Max		0.18	18	±0.1	±0.1	±1	±1		$\pm 10^{-5}$	±0.1	μA

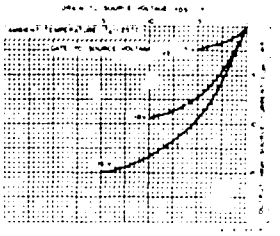


Fig. 4 – Minimum output high (source) current characteristics.

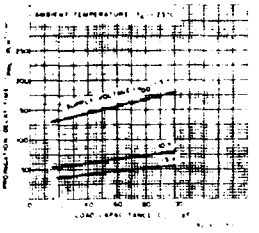


Fig. 5 – Typical propagation delay time vs. load capacitance (CLOCK or SET to Q, CLOCK or RESET to $\overline{Q}$).

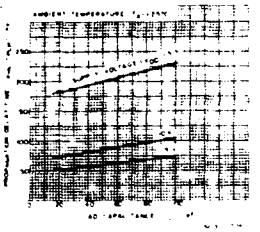


Fig. 6 – Typical propagation delay time vs. load capacitance (SET to $\overline{Q}$, RESET to Q).

Fig. 7 – Logic diagram and truth table for CD4013 (one of two identical flip-flops).

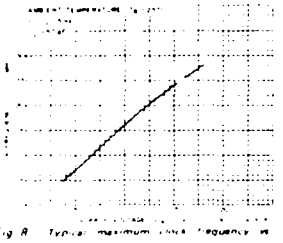


Fig. 8 – Typical maximum clock frequency vs. supply voltage.

MAXIMUM RATINGS, *Absolute Maximum Values*

DC SUPPLY VOLTAGE RANGE (V_{DD})
(Voltages referenced to V_{SS} Terminal) -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ±10 mA
POWER DISSIPATION PER PACKAGE (P_D)
For T_A = −40 to +60°C (PACKAGE TYPE E) 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K) 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE TEMPERATURE RANGE (All Package Types) 100 mW
OPERATING TEMPERATURE RANGE (T_A)
PACKAGE TYPES D, F, K, H −55 to +125°C
PACKAGE TYPE E −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max +265°C

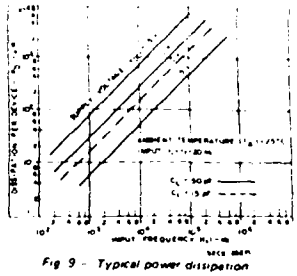


Fig. 9 – Typical power dissipation vs. frequency.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS MIN.	TYP.	MAX.	UNITS
Propagation Delay Time, Clock to Q or $\overline{Q}$ Outputs, t_{PHL}, t_{PLH}	5	–	150	300	ns
	10	–	65	130	
	15	–	45	90	
Set to Q or Reset to $\overline{Q}$ t_{PLH}	5	–	150	300	ns
	10	–	65	130	
	15	–	45	90	
Set to $\overline{Q}$ or Reset to Q t_{PHL}	5	–	200	400	ns
	10	–	85	170	
	15	–	60	120	
Transition Time t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Maximum Clock Input Frequency, Frequency[a] f_{CL}	5	3.5	7	–	MHz
	10	8	16	–	
	15	12	24	–	
Minimum Clock Pulse Width t_W	5	–	70	140	ns
	10	–	30	60	
	15	–	20	40	
Minimum Set or Reset Pulse Width t_W	5	–	90	180	ns
	10	–	40	80	
	15	–	25	50	
Minimum Data Setup Time t_S	5	–	20	40	ns
	10	–	10	20	
	15	–	7	15	
Clock Input Rise or Fall Time t_{rCL}, t_{fCL}	5	–	–	70	μs
	10	–	–	6	
	15	–	–	2	
Input Capacitance C_{IN}	Any Input	–	5	7.5	pF

[a] Input t_r, t_f = 5 ns

TEST CIRCUITS

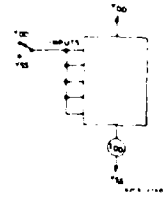


Fig. 10 – Quiescent device current.

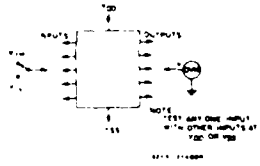


Fig. 11 – Input voltage.

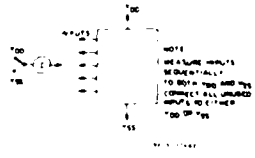
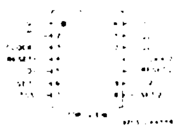


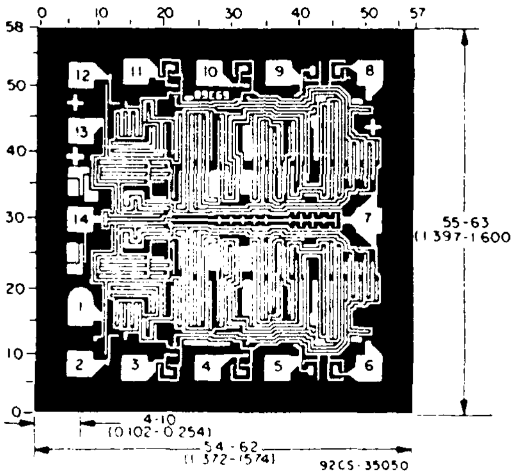
Fig. 12 – Input current.



TERMINAL ASSIGNMENT

Fig. 13 - Dynamic power dissipation test circuit

DIMENSIONS AND PAD LAYOUT FOR CD4013BH



Dimensions in parentheses are in millimeters [illegible] Grid graduations are in mils [illegible]

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of [illegible] mils [illegible] applicable to the nominal dimensions shown.

CMOS 4-Bit Magnitude Comparator

High Voltage Types (20 Volt Rating)

The RCA CD4585B is a 4 bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4 bit words. This logic circuit determines whether one 4 bit word (Binary or BCD) is "less than", "equal to", or "greater than" a second 4 bit word.

The CD4585B has eight comparing inputs (A3, B3 through A0, B0), three outputs (A < B, A = B, A > B) and three cascading inputs (A < B, A = B, A > B) that permit systems designers to expand the comparator function to 8, 12, 16 ... 4N bits. When a single CD4585B is used, the cascading inputs are connected as follows: (A < B) low, (A = B) high, (A > B) high.

Cascading these units for comparison of more than 4 bits is accomplished as shown in Fig. 13.

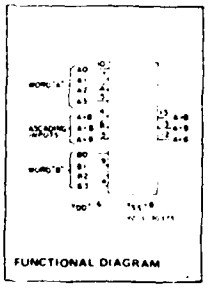
The CD4585B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix). This device is pin-compatible with low-power TTL type 7485 and the CMOS types MC14585 and 40085.

Features

- Expansion to 8,12,16 ... 4N bits by cascading units
- Medium speed operation
  compares two 4 bit words
  in 180 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Standardized symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package temperature range) = 1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Servo motor controls
- Process controllers



FUNCTIONAL DIAGRAM

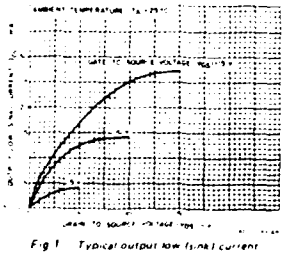


Fig. 1 — Typical output low (sink) current characteristics.

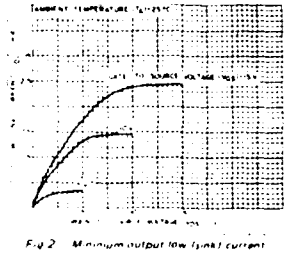


Fig. 2 — Minimum output low (sink) current characteristics.

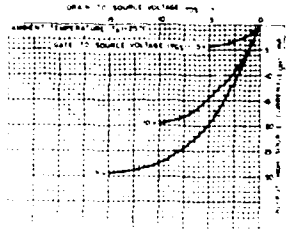


Fig. 3 — Typical output high (source) current characteristics.

MAXIMUM RATINGS, *Absolute Maximum Values*

DC SUPPLY VOLTAGE RANGE (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... 0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... 0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D)
For T_A = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate E linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING TEMPERATURE RANGE (T_A)
PACKAGE TYPES D, F, K, H ..... −55 to +125°C
PACKAGE TYPE E ..... −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A < B	A = B	A > B	A < B	A = B	A > B
A3 > B3	X	X	X	X	X	1	0	0	1
A3 = B3	A2 > B2	X	X	X	X	1	0	0	1
A3 = B3	A2 = B2	A1 > B1	X	X	X	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	X	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	X	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	1	0	0
A3 = B3	A2 < B2	X	X	X	X	X	1	0	0
A3 < B3	X	X	X	X	X	X	1	0	0

X = Don't Care Logic 1 = High Level Logic 0 = Low Level

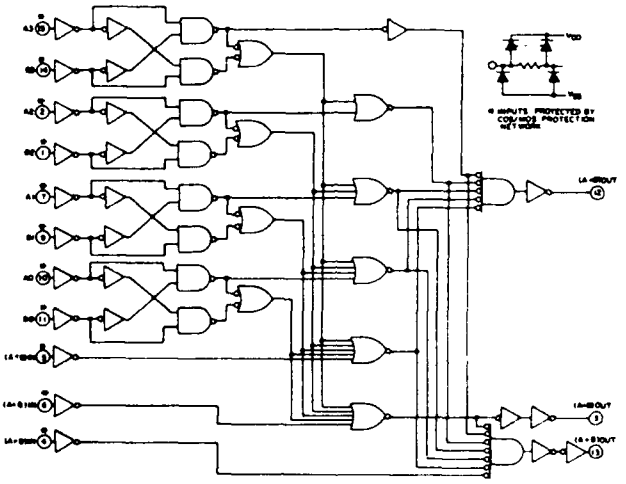


Fig. 4 – Logic diagram.

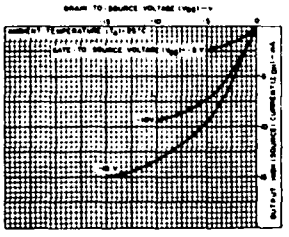


Fig. 5 – Minimum output high (source) current characteristics.

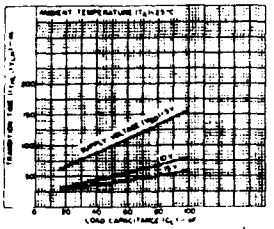


Fig. 6 – Typical transition time as a function of load capacitance.

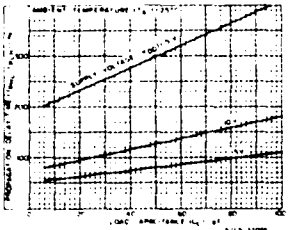


Fig. 7 – Typical propagation delay time (comparing inputs to outputs) as a function of load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H Packages Values at -40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current I_{DD} Max		0,5	5	5	5	150	150	-	0.04	5	μA
	-	0,10	10	10	10	300	300	-	0.04	10	
	-	0,15	15	20	20	600	600	-	0.04	20	
	-	0,20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current I_{OL} Min	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current I_{OH} Min	4.6	0,5	5	0.64	0.61	0.42	0.36	0.51	-1	-	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage Low Level V_{OL} Max	-	0,5	5	0.05				-	0	0.05	V
	-	0,10	10	0.05				-	0	0.05	
	-	0,15	15	0.05				-	0	0.05	
Output Voltage High Level V_{OH} Min	-	0,5	5	4.95				4.95	5	-	
	-	0,10	10	9.95				9.95	10	-	
	-	0,15	15	14.95				14.95	15	-	
Input Low Voltage V_{IL} Max	0.5,4.5	-	5	1.5				-	-	1.5	V
	1,9	-	10	3				-	-	3	
	1.5,13.5	-	15	4				-	-	4	
Input High Voltage, V_{IH} Min	0.5,4.5	-	5	3.5				3.5	-	-	
	1,9	-	10	7				7	-	-	
	1.5,13.5	-	15	11				11	-	-	
Input Current I_{IN} Max		0,18	18	±0.1	±0.1	±1	±1	-	$\pm 10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} Volts	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time Comparing Inputs to Outputs t_{PHL}, t_{PLH}		5	300	600	ns
		10	125	250	
		15	80	160	
Cascading Inputs to Outputs, t_{PHL}, t_{PLH}		5	200	400	
		10	80	160	
		15	60	120	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

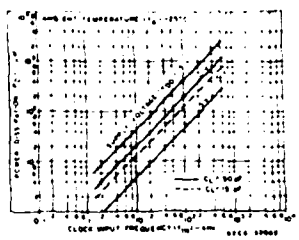


Fig. 8 – Typical dynamic power dissipation as a function of clock input frequency (see Fig. 9–dynamic power dissipation test circuit)

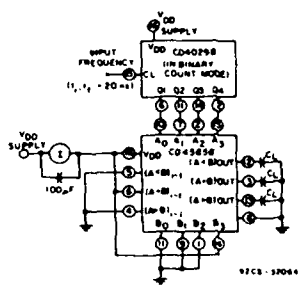


Fig. 9 – Dynamic power dissipation test circuit

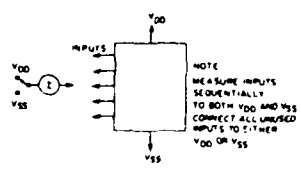


Fig. 10 – Input current test circuit

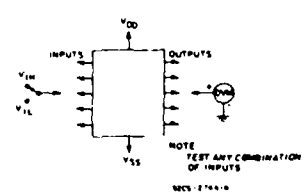


Fig. 11 – Input voltage test circuit

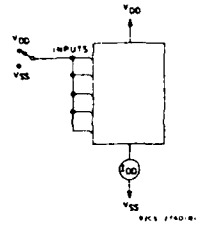


Fig. 12 – Quiescent-device-current test circuit.

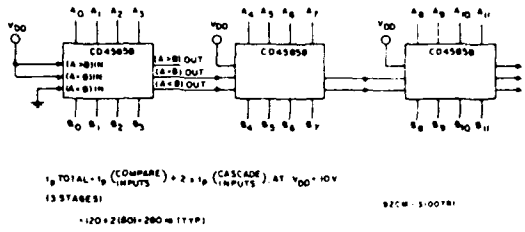
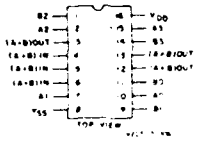
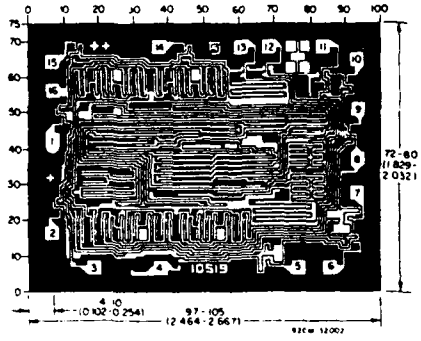


Fig. 13 – Typical speed characteristics of a 12-bit comparator.

TERMINAL ASSIGNMENT





Dimensions and Pad Layout for CD4585BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

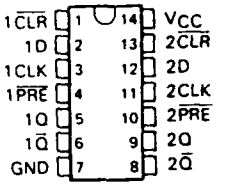
The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip therefore may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

D2661, APRIL 1982 – REVISED MAY 1986

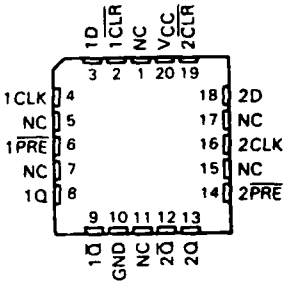
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (C_L = 50 pF)	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS74A	50 MHz	6 mW
'AS74	134 MHz	26 mW

SN54ALS74A, SN54AS74 . . . J PACKAGE
SN74ALS74A, SN74AS74 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS74A, SN54AS74 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

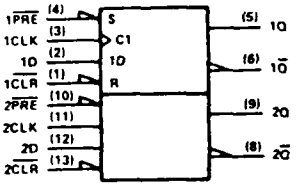
The SN54ALS74A and SN54AS74 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS74A and SN74AS74 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

* The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS74A, SN54AS74 . . . . . −55°C to 125°C
SN74ALS74A, SN74AS74 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS74A			SN74ALS74A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				-0.4			-0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		34	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			15			ns
		CLK high	17.5			14.5			
		CLK low	17.5			14.5			
t_{su}	Setup time before CLK↑	Data	16			15			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	10			10			
t_h	Hold time, data after CLK↑		2			0			ns
T_A	Operating free-air temperature		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS74A			SN74ALS74A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = -18 mA			-1.5			-1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = -0.4 mA	V_{CC}-2			V_{CC}-2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	CLK or D	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	CLK or D	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK or D	V_{CC} = 5.5 V,	V_I = 0.4 V			-0.2			-0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					-0.4			-0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	-30		-112	-30		-112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.4	4		2.4	4	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS74A		SN74ALS74A		
			MIN	MAX	MIN	MAX	
f_{max}			30		34		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	18	3	13	ns
t_{PHL}			5	17	5	15	
t_{PLH}	CLK	Q or $\overline{Q}$	5	23	5	16	ns
t_{PHL}			5	20	5	18	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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recommended operating conditions

			SN54AS74			SN74AS74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		90	0		105	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4			4			ns
		CLK high	4			4			
		CLK low	5.5			5.5			
t_{su}	Setup time before CLK↑	Data	4.5			4.5			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2			2			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS74			SN74AS74			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	CLK or D	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK or D	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	$\overline{PRE}$ or $\overline{CLR}$					−1.8			−1.8	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	See Note 1		10.5	16		10.5	16	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-current output current, I_{OS}.
NOTE 1: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS74		SN74AS74		
			MIN	MAX	MIN	MAX	
f_{max}			90		105		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	8.5	3	7.5	ns
t_{PHL}			3.5	11.5	3.5	10.5	
t_{PLH}	CLK	Q or $\overline{Q}$	3.5	9	3.5	8	ns
t_{PHL}			4.5	10.5	4.5	9	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

54ALS74A	ALS/AS LOGIC DATA BOOK 1986, PAGE 2-77	ERRATA DATE: 10-10-86

RECOMMENDED OPERATING CONDITIONS/SWITCHING CHARACTERISTICS PAGE: 2-78

CORRECTION:	FROM:	TO:
fmax	30 MHz MIN	25 MHz MIN
tclock	30 MHz MAX	25 MHz MAX

54ALS86	ALS/AS LOGIC DATA BOOK 1986, PAGE: 2-81	NO ERRATA
54ALS109A	ALS/AS LOGIC DATA BOOK 1986, PAGE 2-89	NO ERRATA
54ALS112A	ALS/AS LOGIC DATA BOOK 1986, PAGE 2-93	NO ERRATA
54ALS113A	ALS/AS LOGIC DATA BOOK 1986, PAGE 2-97	ERRATA DATE: 10-10-86 6-24-88

SWITCHING CHARACTERISTICS PAGE: 2-99

CORRECTION:	FROM:	TO:
tPLH, PRE/ TO Q OR Q/	23 ns MAX	21 ns MAX

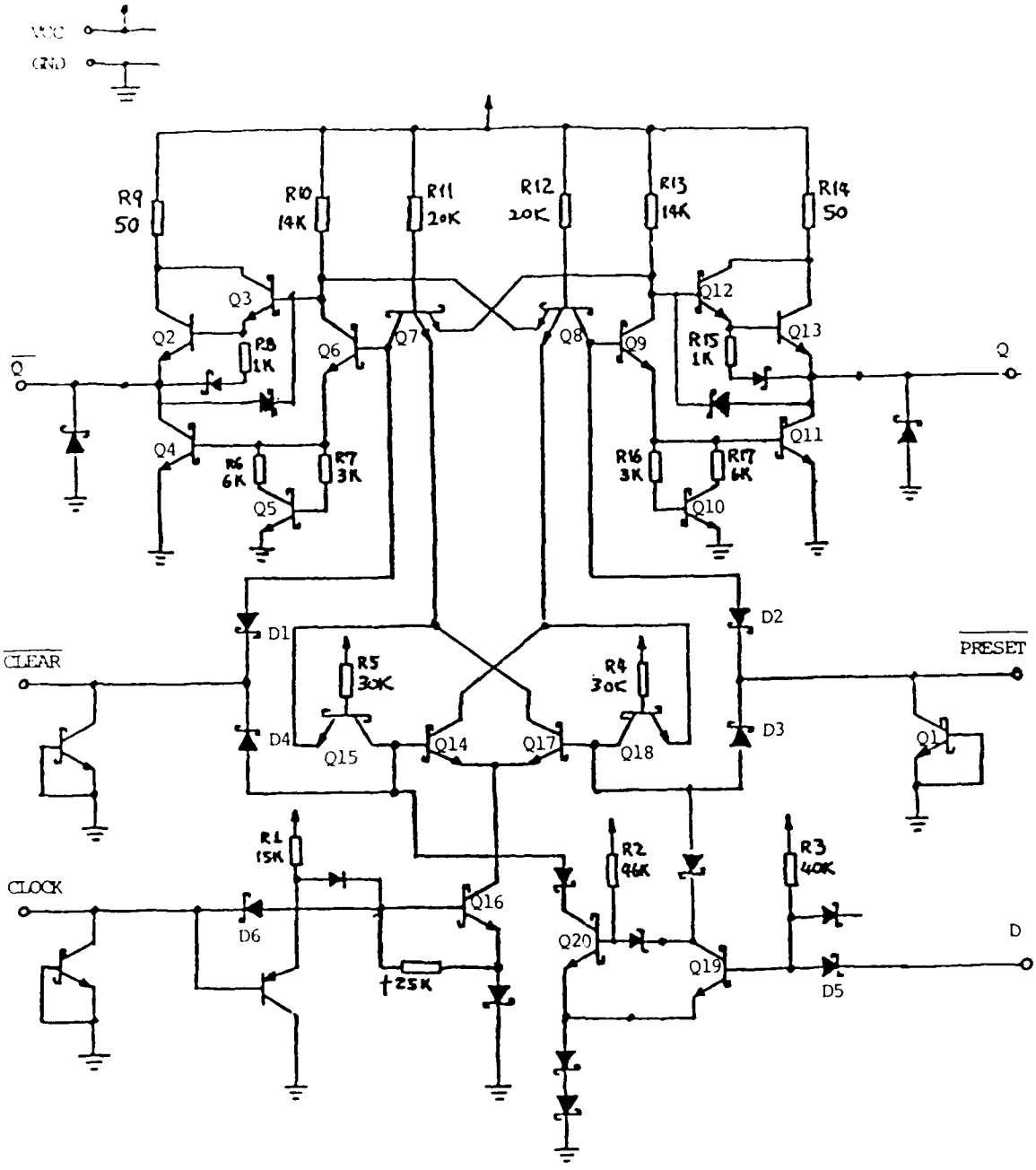
NOTE 1 - CHANGE TO: ICC IS MEASURED WITH J, K, CLK, AND PRE/ GROUNDED.

54ALS114A	ALS/AS LOGIC DATA BOOK 1986, PAGE 2-101	NO ERRATA
54ALS133	ALS/AS LOGIC DATA BOOK 1986, PAGE 2-109	ERRATA DATE: 10-10-86

SWITCHING CHARACTERISTICS PAGE: 2-110

CORRECTION:	FROM:	TO:
tPHL, ANY INPUT TO Y	5 ns MIN	1 ns MIN

54ALS137	ALS/AS LOGIC DATA BOOK 1986, PAGE 2-115	NO ERRATA
54ALS138	ALS/AS LOGIC DATA BOOK 1986, PAGE 2-119	NO ERRATA
54SALS139	ALS/AS LOGIC DATA BOOK, 1986, PAGE 2-125	NO ERRATA
54ALS151	ALS/AS LOGIC DATA BOOK 1986, PAGE 2-129	NO ERRATA
54ALS153	ALS/AS LOGIC DATA BOOK 1986, PAGE 2-133	NO ERRATA



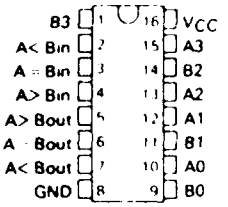
SN54ALS74A Schematic with Transistors Labelled

4-BIT MAGNITUDE COMPARATORS

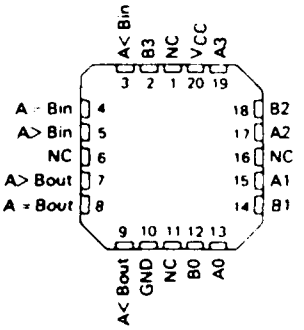
MARCH 1974 – REVISED MARCH 1988

TYPE	TYPICAL POWER DISSIPATION	TYPICAL DELAY (4 BIT WORDS)
85	275 mW	23 ns
LS85	52 mW	24 ns
S85	365 mW	11 ns

SN5485, SN54LS85, SN54S85 . . . J OR W PACKAGE
SN7485 . . . N PACKAGE
SN74LS85, SN74S85 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS85, SN54S85 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

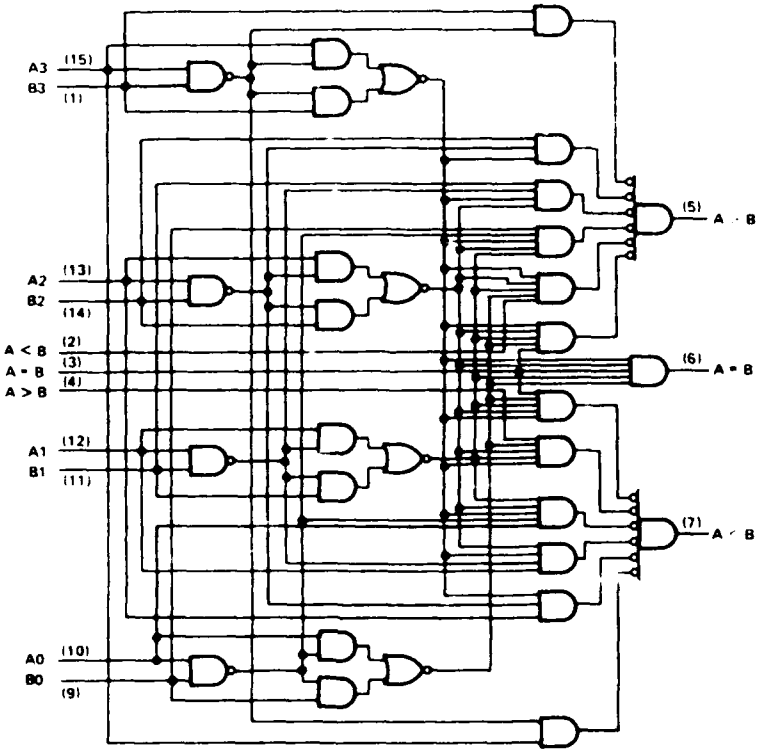
description

These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading paths of the '85, 'LS85, and 'S85 are implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

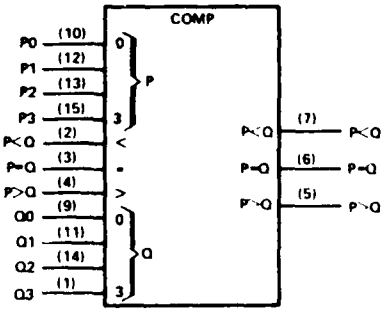
FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B2	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A2 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

logic diagrams (positive logic)



logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

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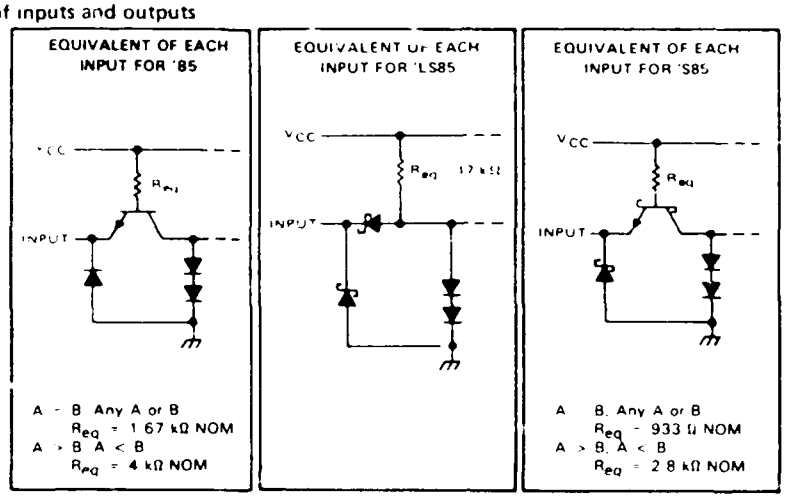
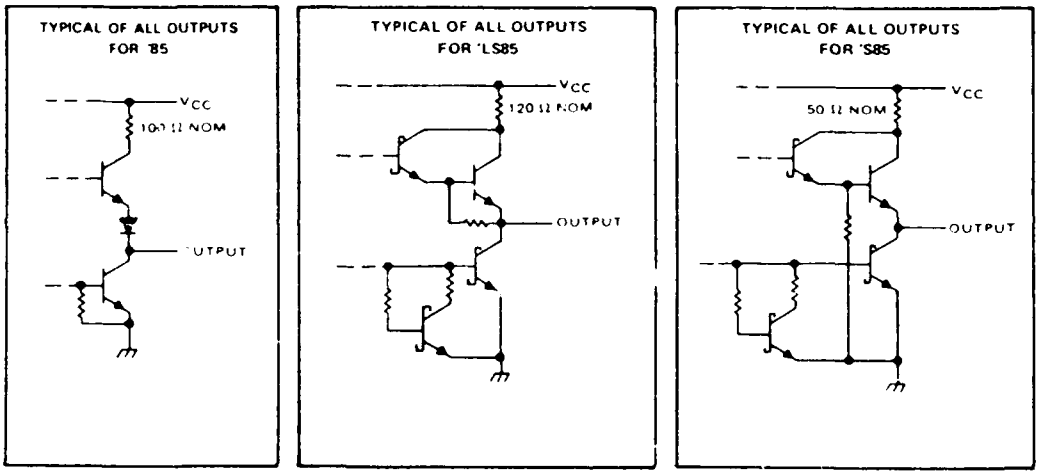
schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54' SN54S'	SN54LS	SN74 SN74S	SN74LS	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	7	7	V
Input voltage	5.5	7	5.5	7	V
Interemitter voltage (see Note 2)	5.5		5.5		V
Operating free-air temperature range	−55 to 125		0 to 70		°C
Storage temperature range	−65 to 150		−65 to 150		°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor. This rating applies to each A input and each B input with respect to the B input of the '85 and 'LS85.

recommended operating conditions

	SN5485			SN7485			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage					2			V
V_{IL} Low-level input voltage							0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN,	I_I = -12 mA				-1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = -400 μA		2.4	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA			0.2	0.4	V
I_I Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH} High-level input current	A < B, A > B inputs	V_{CC} = MAX,	V_I = 2.4 V				40	μA
	all other inputs						120	
I_{IL} Low-level input current	A < B, A > B inputs	V_{CC} = MAX,	V_I = 0.4 V				-1.6	mA
	all other inputs						-4.8	
I_{OS} Short-circuit output current§		V_{CC} = MAX, V_O = 0		SN5485	-20		-55	mA
				SN7485	-18		-55	
I_{CC} Supply current		V_{CC} = MAX, See Note 4				55	88	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 4: I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A < B, A > B	1	C_L = 15 pF, R_L = 400 Ω, See Note 5		7		ns
			2			12		
			3			17	26	
		A = B	4			23	35	
t_{PHL}	Any A or B data input	A < B, A > B	1			11		ns
			2			15		
			3			20	30	
		A = B	4			20	30	
t_{PLH}	A < B or A = B	A > B	1			7	11	ns
t_{PHL}	A < B or A = B	A > B	1			11	17	ns
t_{PLH}	A > B	A = B	2			13	20	ns
t_{PHL}	A > B	A = B	2			11	17	ns
t_{PLH}	A > B or A = B	A > B	1			7	11	ns
t_{PHL}	A > B or A = B	A > B	1			11	17	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 5: Load circuits and voltage waveforms are shown in Section 1.

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recommended operating conditions

	SN54LS85			SN74LS85			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS85			SN74LS85			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.7	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	A < B, A > B inputs	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
		all other inputs					0.3			0.3	
I_{IH}	High-level input current	A < B, A > B inputs	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		all other inputs					60			60	
I_{IL}	Low-level input current	A < B, A > B inputs	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		all other inputs					−1.2			−1.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 4		10.4	20		10.4	20	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 4: I_{CC} is measured with outputs open, A > B grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A < B, A > B	1	C_L = 15 pF, R_L = 2 kΩ, See Note 5		14		ns
			2			19		
			3			24	36	
		A = B	4			27	45	
t_{PHL}	Any A or B data input	A < B, A > B	1			11		ns
			2			15		
			3			20	30	
		A = B	4			23	45	
t_{PLH}	A < B or A > B	A > B	1			14	22	ns
t_{PHL}	A < B or A > B	A > B	1			11	17	ns
t_{PLH}	A = B	A = B	2			13	20	ns
t_{PHL}	A = B	A = B	2			13	20	ns
t_{PLH}	A < B or A > B	A < B	1			14	22	ns
t_{PHL}	A < B or A > B	A < B	1			11	17	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 5: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

	SN54S85			SN74S85			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	SN54S85	2.5	3.4		V
				SN74S85	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	A < B, A > B inputs	V_{CC} = MAX, V_I = 2.7 V				50	μA
		all other inputs					150	
I_{IL}	Low-level input current	A < B, A > B inputs	V_{CC} = MAX, V_I = 0.5 V				−2	mA
		all other inputs					−6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 4			73	115	mA
			V_{CC} = MAX, T_A = 125°C, See Note 4	SN54S85W			110	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 4: I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A < B, A > B	1	C_L = 15 pF, R_L = 280 Ω, See Note 5		5		ns
			2			7.5		
			3			10.5	16	
		A = B	4			12	18	
t_{PHL}	Any A or B data input	A < B, A > B	1			5.5		ns
			2			7		
			3			11	16.5	
		A = B	4			11	16.5	
t_{PLH}	A < B or A = B	A > B	1			5	7.5	ns
t_{PHL}	A < B or A = B	A > B	1			5.5	8.5	ns
t_{PLH}	A = B	A = B	2			7	10.5	ns
t_{PHL}	A = B	A = B	2			5	7.5	ns
t_{PLH}	A > B or A < B	A > B	1			5	7.5	ns
t_{PHL}	A > B or A < B	A > B	1			5.5	8.5	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 5: Load circuits and voltage waveforms are shown in Section 1.

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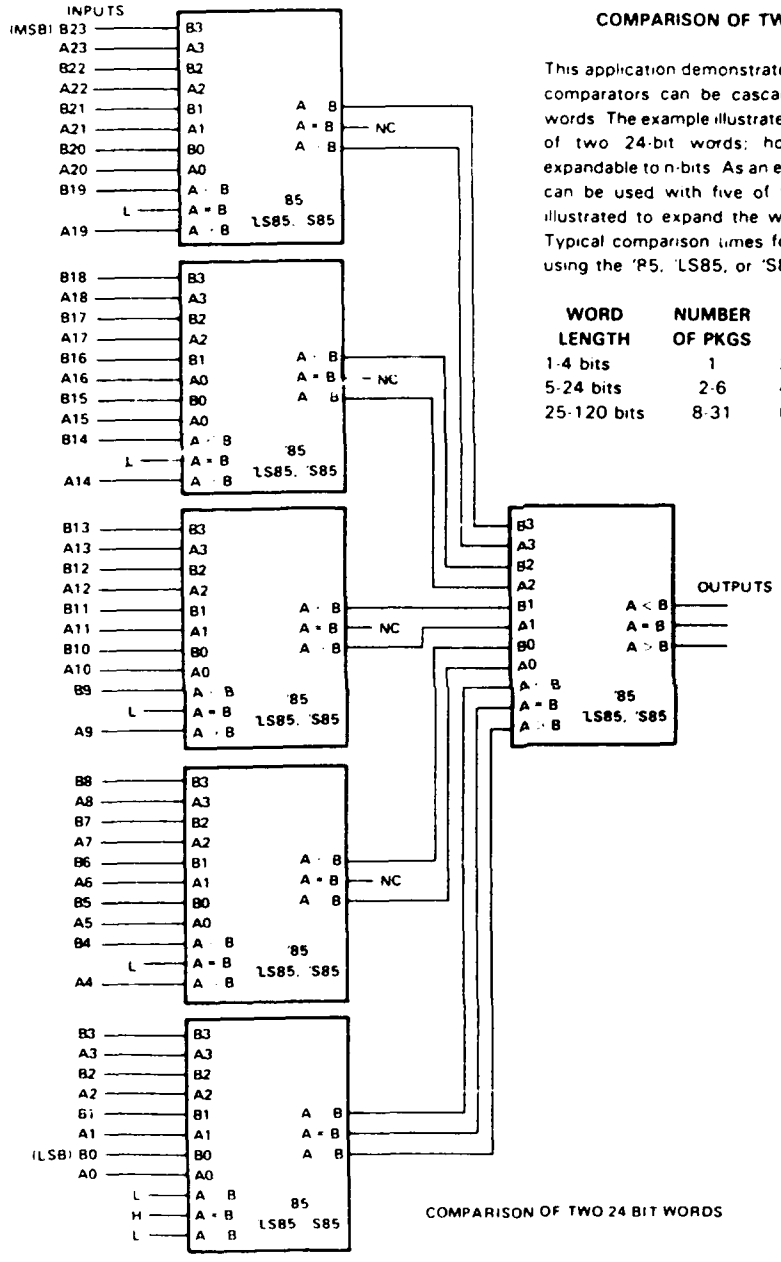
TYPICAL APPLICATION DATA



COMPARISON OF TWO N-BIT WORDS

This application demonstrates how these magnitude comparators can be cascaded to compare longer words. The example illustrated shows the comparison of two 24-bit words; however, the design is expandable to n-bits. As an example, one comparator can be used with five of the 24-bit comparators illustrated to expand the word length to 120-bits. Typical comparison times for various word lengths using the '85, 'LS85, or 'S85 are:

WORD LENGTH	NUMBER OF PKGS	'85	'LS85	'S85
1-4 bits	1	23 ns	24 ns	11 ns
5-24 bits	2-6	46 ns	48 ns	22 ns
25-120 bits	8-31	69 ns	72 ns	33 ns

APPENDIX A.2 OP-AMP COMBINER DATA

Comlinear Corporation

Fast Settling, High Current Wideband Op Amps

CLC103AI, CLC103AM (MIL-Rel)

2

APPLICATIONS:

- coaxial line driving
- DAC current to voltage amplifier
- flash A to D driving
- baseband and video communications
- radar and IF processors

FEATURES:

- 80MHz full-power bandwidth ($20V_{pp}$, 100Ω)
- 200mA output current
- 0.4% settling in 10ns
- 6000V/μs slew rate
- 4ns rise and fall times (20V)

DESCRIPTION:

The CLC103 is a high-power, wideband op amp designed for the most demanding high-speed applications. The wide bandwidth, fast settling, linear phase, and very low harmonic distortion provide the designer with the signal fidelity needed in applications such as driving flash A to Ds. **The 80MHz full-power bandwidth and 200mA output current of the CLC103 eliminate the need for power buffers in most applications;** the CLC103 is an excellent choice for driving large high-speed signals into coaxial lines.

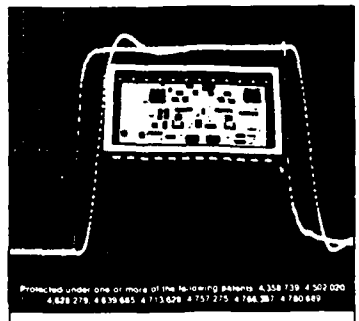
In the design of the CLC103 special care was taken in order to guarantee that the output settle quickly to within 0.4% of the final value for use with ultra fast flash A to D converters. This is one of the most demanding of all op amp requirements since settling time is affected by the op amp's bandwidth, passband gain flatness, and harmonic distortion. This high degree of performance ensures excellent performance in many other demanding applications as well.

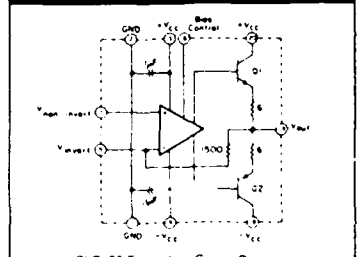
The dynamic performance of the CLC103 is based on Comlinear's proprietary op amp topology. This new design provides performance far beyond that available from conventional op amp designs, unlike conventional op amps where optimum gain-bandwidth product occurs at a high gain, minimum settling time at a gain of −1, and maximum slew rate at a gain of +1, the Comlinear design provides consistent, predictable performance across its entire gain range. For example, the table below shows how **the −3dB bandwidth remains nearly constant over a wide range of gains.** And since the amplifier is inherently stable, no external compensation is required. The result is shorter design time and the ability to accommodate design changes (in gain, for example) without loss of performance or redesign of compensation circuits.

The CLC103 is constructed using thick film resistor/bipolar transistor technology. The CLC103AI is specified over a temperature range of −25°C to +85°C, while the CLC103AM is specified over a range of −55°C to +125°C and is screened to Comlinear's M-Standard for high reliability applications. Both devices are packaged in 24-pin ceramic DIPs.

Typical Performance

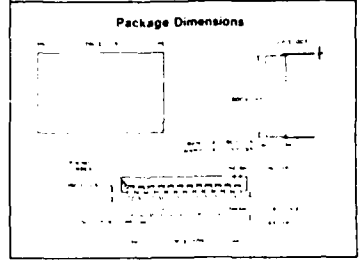
parameter	gain setting						units
	+4	+20	+40	−4	−20	−40	
3dB bandwidth	230	150	130	155	145	125	MHz
rise time (20V)	4	4	4	4	4	4	ns
slew rate	6	6	6	6	6	6	V/ns
settling time (0.4%)	10	10	12	10	10	12	ns





CLC103 Equivalent Circuit Diagram
(all undesignated pins are internally unconnected)

Package Dimensions



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DS103-03 October 1988

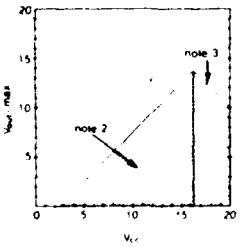
Electrical Characteristics (A_V = +2, V_{cc} = ±15V, R_L = 100Ω)

Parameters	Conditions	typ	min and max ratings[1]			units	symbol
	Ambient Temperature (AM)[1]	+25°C	-55°C	+25°C	+125°C		
	Ambient Temperature (AI)[1]	+25°C	-25°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
* 3dB bandwidth	V_{out} = 4V_{pp}	150	>125	>135	>120	MHz	SSBW
gain flatness	V_{out} = 4V_{pp}						
* peaking	DC to 50MHz	0.1	<0.6	<0.3	<0.3	dB	GFPL
* peaking	>50MHz	0.2	<1.5	<0.6	<0.6	dB	GFPH
* rolloff	at 100MHz	–	<0.4	<0.6	<0.8	dB	GFR
group delay	to 75MHz	30±0.5	–	–	–	ns	GD
linear phase deviation	to 75MHz	1	<3	<2	<4	°	LPD
reverse isolation - non-inverting	to 150MHz	55	>45	>45	>45	dB	RINI
TIME DOMAIN RESPONSE							
rise and fall time	5V step	2.3	<2.8	<2.6	<2.9	ns	TRS
	20V step	4	<5	<5	<5	ns	TRL
settling time to 0.4%	10V step	10	<25	<20	<25	ns	TSP
overshoot	5V step	5	<15	<10	<10	%	OS
slew rate (overdriven input)		6	>5	>5	>5	V/ns	SR
overload recovery							
<50ns pulse, 200% overdrive		30	–	–	–	ns	OR
DISTORTION AND NOISE RESPONSE							
* 2nd harmonic distortion	2V_{pp}, 20MHz	-48	<-40	<-40	<-40	dBc	HD2
* 3rd harmonic distortion	2V_{pp}, 20MHz	-48	<-40	<-40	<-40	dBc	HD3
equivalent input noise							
noise floor	>100kHz	-158	<-152	<-152	<-152	dBm(1Hz)	SNF
integrated noise	1kHz to 100MHz	28	<56	<56	<56	μV	INV
* noise floor	>5MHz	-158	<-152	<-152	<-152	dBm(1Hz)	SNF
* integrated noise	5MHz to 100MHz	28	<56	<56	<56	μV	INV
STATIC, DC PERFORMANCE							
* input offset voltage		10	<30	<25	<30	mV	VIO
* average temperature coefficient		35	<80	<80	<80	μV/°C	DVIO
* input bias current	non-inverting	10	<40	<30	<40	μA	IBN
* average temperature coefficient		20	<125	<125	<125	nA/°C	DIBN
* input bias current	inverting	20	<110	<60	<110	μA	IBI
* average temperature coefficient		250	<500	<500	<500	nA/°C	DIBI
* power supply rejection ratio		54	>45	>45	>45	dB	PSRR
common mode rejection ratio		38	>30	>30	>30	dB	CMRR
* supply current	no load	30	<36	<34	<36	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	250	>100	>100	>100	kΩ	RIN
	capacitance	2.4	<3	<3	<3	pF	CIN
output impedance	at DC	–	<0.1	<0.1	<0.1	Ω	RO
	at 100MHz	2, 45	–	–	–	Ω, nH	ZO
output voltage range	no load	–	>±11	>±11	>±11	V	VO

MTBF is 1.76 million hours (AM version, GF @ 70°C case, per MIL-HDBK-217E)

Absolute Maximum Ratings

Output Voltage Limit



supply voltage (V_{cc})	±20V
output current	±200mA
thermal resistance (θ_{ca})	see thermal model
junction temperature	+175°C
operating temperature	AI -25°C to +85°C
	AM -55°C to +125°C
storage temperature	-65°C to +150°C
lead temperature (soldering 10s)	+300°C

* note 1: Parameters preceded by an * are the final electrical test parameters and are 100% tested. AM units are tested at -55°C (power stable), +25°C (low-duty cycle pulsed testing), and +125°C (low duty cycle pulsed testing). AI units are tested only at +25°C although their performance is guaranteed at -25°C and +85°C as indicated above.

note 2: This rating protects against damage to the input stage caused by saturation of either the input or output stages. Under transient conditions not exceeding 1μs (duty cycle not exceeding 10%), maximum input voltage may be as large as twice the maximum V_{cm} should never exceed ±5V (V_{cm} is the voltage at the non-inverting input, pin 7.)

note 3: This rating protects against exceeding transistor collector-emitter breakdown ratings. Recommended V_{cc} is ±15V.

Typical Performance Characteristics (A_v = +20, V_{cc} = ±15V, R_L = 100Ω)

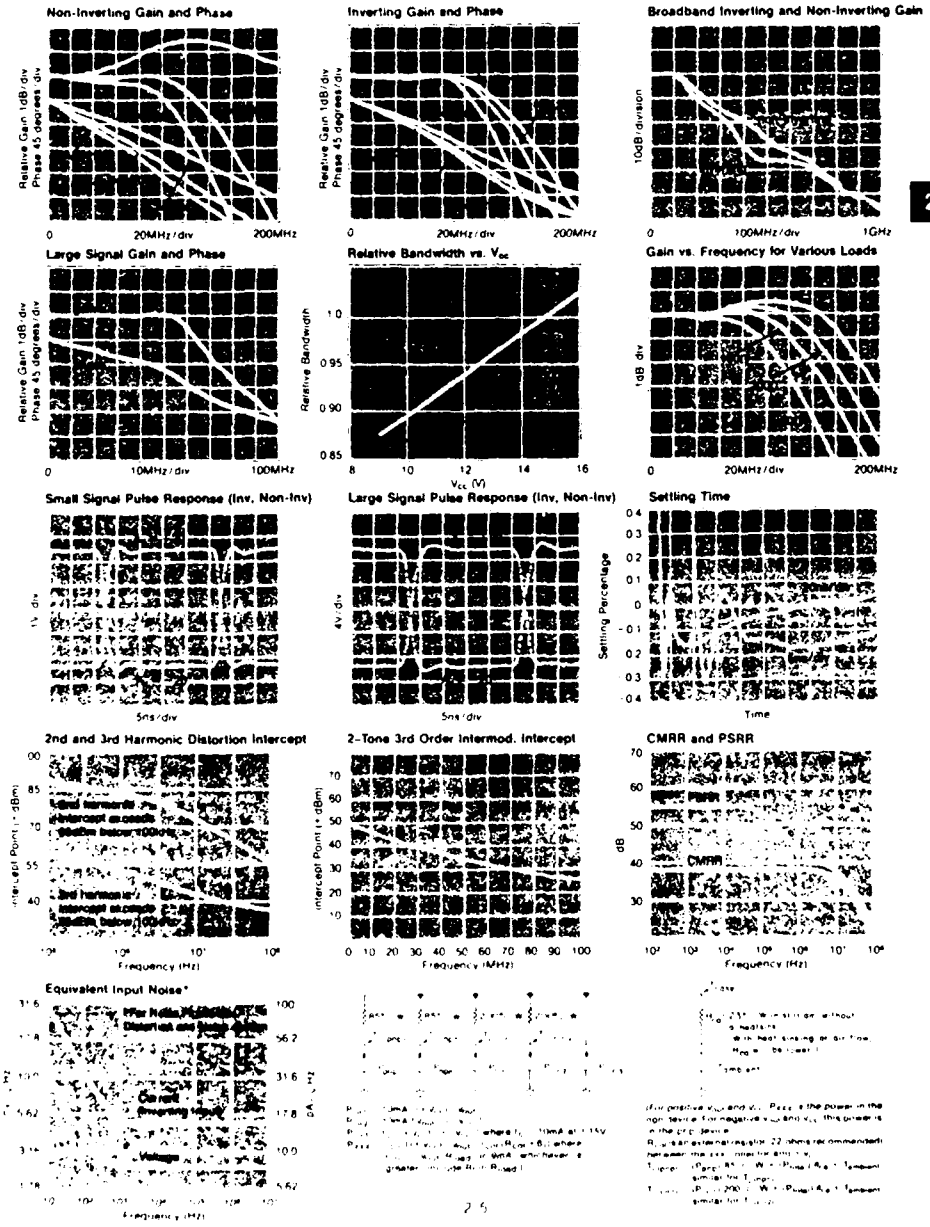


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figure 1: recommended non-inverting gain circuit

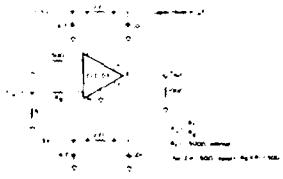

figure 2: recommended inverting gain circuit

Test / future layout artwork is available upon request

CLC103 Operation

The CLC103 is based on Comlinear's proprietary op amp topology, a unique design which uses *current feedback instead of the usual* voltage feedback. This design provides dynamic performance far beyond that previously available, yet it is used basically the same as the familiar voltage-feedback op amp (*see the gain equations above*). A complete discussion of current feedback is given in application note AN300-1.

Layout Considerations

To obtain optimum performance from any circuit operating at high frequencies, good PC layout is essential. Fortunately, the stable, well-behaved response of the CLC103 makes operation at high frequencies less sensitive to layout than is the case with other wideband op amps, even though the CLC103 has a much wider bandwidth.

In general, a good layout is one which minimizes the unwanted coupling of a signal between nodes in a circuit. A continuous ground plane from the signal input to output on the circuit side of the board is helpful. Traces should be kept short to minimize inductance. If long traces are needed, use microstrip transmission lines which are terminated in their characteristic impedance. At some high-impedance nodes, or in sensitive areas such as near pin 5 of the CLC103, stray capacitance should be kept small by keeping nodes small and removing ground plane directly around the node.

The $\pm V_{cc}$ connections to the CLC103 are internally bypassed to ground *with 0.1μF capacitors to provide* good high-frequency decoupling. It is recommended that 1μF or larger tantalum capacitors be provided for low-frequency decoupling. *The* 0.01μF capacitors shown at pins 18 *and 20 in figures 1 and 2* should be kept within 0.1" of those pins. A wide strip of ground plane should be provided for a signal return path between the load-resistor ground and these capacitors.

Since the layout of the PC board forms such an important part of the circuit, much time can be saved if prototype amplifier boards are tested early in the design stage. Encased/connectorized amplifiers are available from Comlinear.

Settling Time, Offset, and Drift

After an output transition has occurred, the output settles very rapidly to the final value and no change occurs for several microseconds. Thereafter, thermal gradients inside the CLC103 will cause the output to begin to drift. When this cannot be tolerated, or when the initial offset voltage and drift is unacceptable, the use of a composite amplifier is advised.

A composite amplifier can also be referred to as a feed-forward amplifier. Most feed-forward techniques such as those used in the vast majority *of wideband op amps*, involve the use of a wideband AC-coupled channel in parallel with a low-bandwidth, high-gain DC-coupled amplifier. For the composite amplifier suggested for use with *the CLC103*, the CLC103 replaces the wideband AC-coupled amplifier and a low-cost monolithic op amp is used to supply high open-loop gain at low frequencies. Since the CLC103 is strictly DC coupled *throughout*, crossover distortion of less than 0.01dB and 1° results.

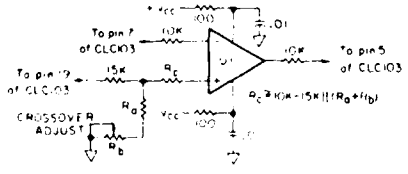

figure 3: non-inverting gain composite amp to be used with figure 1 circuit

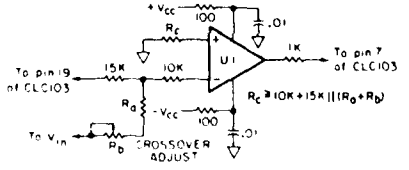

figure 4: inverting gain composite amplifier to be used with figure 2 circuit

For composite operation in the non-inverting mode, the circuit in figure 1 should be modified by the addition of the circuit shown in figure 3. For inverting operation, modify the circuit in figure 2 by the addition of the circuit in figure 4. Keep all resistors which connect to the CLC103 within 0.2" of the CLC103 pins. The other side of these resistors should likewise be as close to U1 as possible. For good overall results, U1 should be similar to the LF356; this gives 5μV/°C input offset drift and the crossover frequency occurs at about 2MHz. Since U1 has a feedback network composed of $R_a + R_b$ and a 15kΩ resistor, which is in parallel with R_g and the internal 1.5kΩ feedback resistor of the CLC103, R_b must be adjusted to match the feedback ratios of the two networks. This is done by driving the composite amplifier with a 70kHz square wave large enough to produce a transition from +5V to −5V at the CLC103 output and adjusting R_b until the output of U1 is at a minimum. R_a should be about $9.5R_g$ for best results; thus, R_b should be adjusted around the value of $0.5R_g$.

Bias Control

In normal operation, the bias control pin (pin 16) is left unconnected. However, if control over the bias of the amplifier is desired, the bias control pin may be driven with a TTL signal; a TTL high level will turn the amplifier off.

Distortion and Noise

The graphs of intercept point versus frequency on the preceding page make it easy to predict the distortion at any frequency, given the *output voltage of the* CLC103. First, convert the output voltage V_O to $V_{rms} = (V_{pp}/2\sqrt{2})$ and then to $P = (10\log_{10}(20V_{rms}^2))$ to get the output power in dBm. At the frequency of interest, its 2nd harmonic will *be* $S_2 = (I_2 - P)$dB below the level of P. Its third harmonic will be $S_3 = 2(I_3 - P)$dB below the level *of P*, as will the two-tone third order intermodulation products. These approximations are useful for P<− 1dB *compression levels*.

Approximate noise figure can be determined for the CLC103 using the Equivalent Input Noise graph on the preceding page. The following equation can be used to determine *noise figure (F) in dB*:

$$F = 10\log\left[1 + \frac{v_n^2 + \frac{i_n^2 R_s^2}{A_v^2}}{4kTR_s\Delta f}\right]$$

where v_n is the rms noise voltage and i_n is the rms noise current. Beyond the breakpoint of the curves (i.e., where they are flat), broadband noise figure equals spot noise, so Δf should equal one (1) and v_n and i_n should be read directly off the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.

Application Notes and Assistance

Application notes that address topics such as data conversion, fiber optics, and general high-frequency circuit design are available from *Comlinear or your Comlinear* sales engineer.

Comlinear maintains a staff of highly-qualified applications engineers to provide technical and design assistance.

R1 - 39 ohm
R2 - 25 ohm
R3, R4 - 27 ohm
R5, R6 - 270 ohm
R7, R8 - 150 kilohm
R9 - 5 kilohm pot
R10 - 50 kilohm
R11 - 180 ohm
R12, R13 - 22 ohm
R14 - 50 ohm
R15 - 316 ohm
R16 - 230 ohm

C1, C3, C5, C7 - 1 uF
C2, C4, C6, C8 - 0.01 uF

D1, D2 - 1N4148

RELAY 1, RELAY 2 - Teledyne 412

U1 - CLC103AI

Parts List for Op-amp Combiner

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