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COMPUTER CONTROLLED CRYOGENIC TEMPERATURE CONTROLLER

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MATERIALS LABORATORY
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In laboratories which do materials characterization it is necessary to a have a temperature controller which can be computer controlled, is accurate to within .1-.2K, can control temperature from 15-350K with a drift of no more than .1, and is relatively unaffected by the presense of a magnetic field on the sample container. The subject controller uses two thermometers to meet these requirements. One is a commercially available calibrated silicon diode manufactured expressly for this type of application. The second thermometer is used for control. Once the sample has reached the setpoint according to the calibrated thermometer the control thermometer's value is sampled and used as the new setpoint. Since the control thermometer should be insensitive to a mag field the sample will remain at the desired temperature when the magnetic field is applied. In our application the control thermometer is constructed of a carbon-glass resister and a platinum resister. Their resistances are added and used as a single thermometer.

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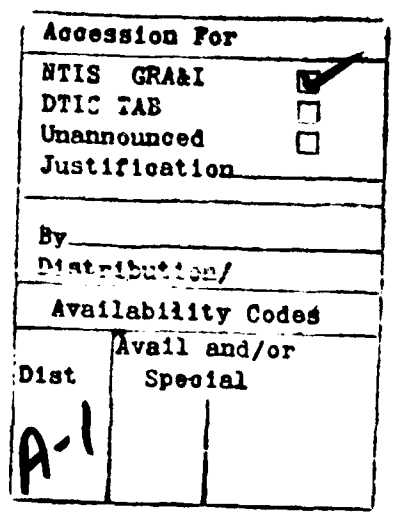

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I INTRODUCTION

The Electronic and Optical Materials Branch of the Materials Lab is involved in the characterization of new semiconductor materials of interest to the Air Force. In the Transport Properties Lab two fully automated Hall-Effect systems contribute to this effort. The Hall-Effect technique is used to accurately measure and identify electronically active impurities present in semiconductor materials. Electrical parameters are measured at temperatures from 12° K up to 350°K. At each temperature increment sixteen different sample configurations are made by switching electrical connections and applying a magnetic field perpendicular to the sample . A continuing problem in the automation of these systems was the lack of a commercially available cryogenic temperature controller that would meet all of our requirements. These requirements are:

1) Temperature accuracy of ± .2°K

2) Temperature controllability of ±.01°K from 10 - 40 °K, ±.1 °K from 41 - 380° K

3) Insensitivity to magnetic field in the sensor area,
i.e. requirement 2. must be satisfied in an applied mag. field of 1 to 10 kgauss.

4) The temperature controller must be able to receive a desired set point from the computer controlling the experiment and be able to signal the computer that the desired set point has been reached and is stable.

5) Operating temperature range, 10 - 380 °K

Samples are mounted on a 65 gram cylindrical block of copper machined to the dimensions shown in figure 11. At each end of the block are about 15 turns of heater windings wired in series such that the total heater resistance is approx. 50 Ω. Mounted

directly beneath the sample in the holder is a calibrated Si. diode cryogenic thermometer [1]. This thermometer-diode is driven by a 10μA current source, the voltage drop across the diode is directly proportional to its temperature. At one end of the block near a set of heater windings are two control thermometers; one platinum [2] and one carbon-glass [3]. A Janis [4] cryogenic dewar serves as a container for the system. Liquid helium from a reservoir in the dewar is fed through a capillary tube to an area directly below the sample chamber. As the helium exits from the tube it comes into contact with a separate small heater which forces it into a gas. As the gaseous helium flows by the sample block it provides the cooling necessary to lower the sample to the 5-20°K temperature range. By applying electrical current to the heater windings on the sample block the temperature controller is able to maintain a setpoint. At each setpoint sample measurements are taken with and without a magnetic field present.

A satisfactory cryogenic temperature controller was designed and built during the time period June 1982 - June 1983. The approach taken in the design of the system is to use two thermometers: one a calibrated silicon diode , the other a control thermometer designed from carbon-glass and platinum resistor-thermometers. The latter are combined into a single thermometer circuit that has a sensitivity comparable to the silicon diode but has very little magneto-resistance at the magnetic fields we typically work with; 1-10kGauss. The unique feature of this controller is its use of a calibration thermometer to reach setpoints and a control thermometer to maintain setpoints. The control thermometer is, in effect, calibrated at each setpoint when it is sampled by a sample-and-hold circuit. A full description is given in subsequent sections. After several months of testing a second controller was built from the same design with only minor modifications and installed on a second automated Hall system. These two controllers were assembled with point-to-point wiring. In 1986 the controller layout was transferred to printed circuit board(PCB) and all subsequent controllers are constructed from these PCB modules.

II BASIC DESIGN

The simplified block diagram shown illustrates the basic flow of control of the temperature controller.

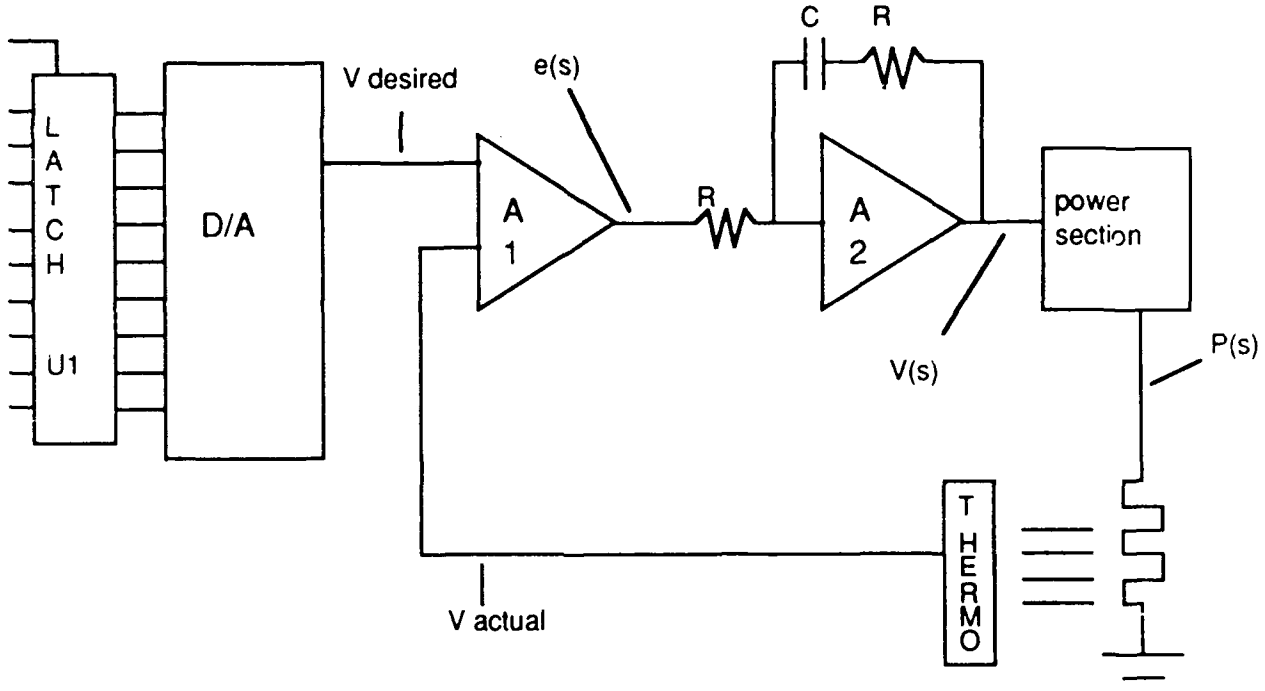


FIGURE 1. Basic Control Loop

From left to right:

1) A new temperature setpoint from a control computer is converted to binary and output in 16-bit parallel format to the input latch (U1)and is 'latched in'.

2) Initially, the output of the latch is enabled and the binary value is converted to an analog voltage signal by the D/A (U2). This is the desired thermometer setpoint voltage (Vdes).

3) The differential amplifier (A1) subtracts the desired setpoint voltage (Vset)from the actual thermometer voltage (Vact),and generates an amplified (X10)error signal (e(s)).

4) The error signal e(s) drives a PI (position-integral)circuit (A2). This circuit conditions the error signal and feeds it to the power amplifier.

5) The power amplifier converts the conditioned error V(s) to a power signal which drives the heater windings and raises the sample holder temperature.

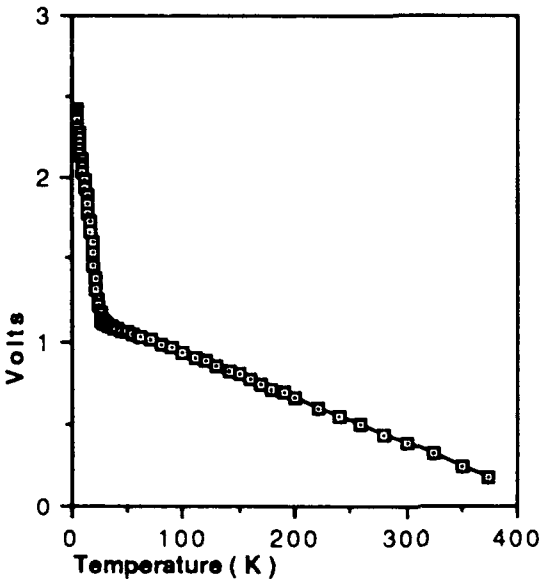
6) The thermometers convert the current sample temperature to a voltage. This voltage is fed back to A1, thus closing the control loop.

The block diagram shown above could be generic to almost any computer-driven control loop. For instance, by substituting a motor/gear-drive for the heater, position could be controlled instead of temperature.

The basic design shown in Fig. 1 has several shortcomings when applied to our temperature control requirements:

1) The Si diode used as a thermometer has a significant magneto-resistance; i.e. its temperature-voltage response is affected by the presence of a mag. field. Unfortunately it is probably the best cryogenic calibration thermometer available. Its values are accurate even after day-to-day thermal cycling and it has good sensitivity throughout the temperature range of interest (10 - 350°K).

2) While the sensitivity of the Si. diode thermometer is good, it is also non-linear. It varies from a maximum of approx. 70mv/°K at 10°K to approx. 2mv/°K at 350°K, as illustrated in fig. 2. The control loop parameters must be modified as the temperature range changes in order to maintain controller stability and accuracy.



Calibration Thermometer Value vs Temperature

Figure 2

3) The thermal response of the sample holder varies with temperature. If the response was constant it could be easily modeled and simply treated as a constant gain block in the control loop. Since it varies with temperature the control loop parameters must be adjusted as the temperature range changes in order to maintain good controller response characteristics. This is illustrated in fig. 3, the change in the specific heat of copper parallels the change in thermal response of the copper sample holder.

As can be seen from fig. 3, the heat capacity of copper increases with temperature. This causes a short thermal response at low temperatures and a more sluggish response at higher temperatures. The P-I filter (A2) parameters are adjusted in order to compensate for these changes in sample holder characteristics as well as the increased power gain required to drive and maintain the sample holder at higher temperatures.

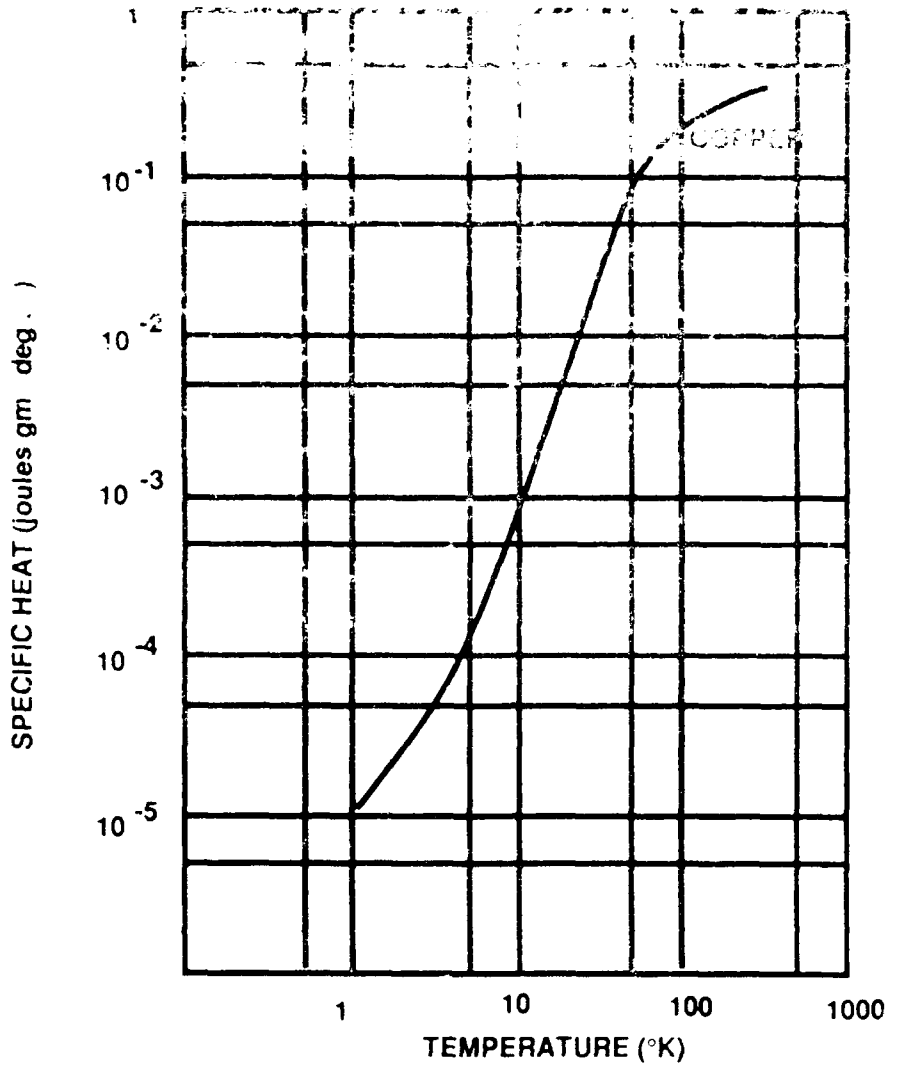


Figure 3. Specific Heat of Copper vs. Temperature

4) The temperature controller should signal the interface that the desired temperature has been reached and is stable. Some sort of visual feedback to the operator would also be desirable.

III CURRENT DESIGN

As shown in the fig. 4 block diagram, a sample-and-hold circuit is added to the system as well as switches to allow different thermometers to be switched intc the control loop. A timing and logic section monitors the error signal (E(s)), when E(s) has been sufficiently small for a prese' period of time it triggers the sample-and hold, waits for the temperature to stabilize, and switches control thermometers at the appropriate time. The gain of the power section is varied to match the thermal response of the sample holder and thermometer. The filter R-C values are variable to match the time-response of the system as the temperature varies.

The sample-and-hold circuit is the most significant addition to the basic control loop. It functions in this way: when the setpoint temperature is reached according to the calibrated silicon-diode thermometer, the real-time value of the control thermometer is measured and stored. This value becomes the new setpoint as the control thermometer is switched into the control loop and the calibration thermometer is switched out of the control loop. This sample-and-hold action is accomplished by the analog-to-digital converter and digital-to-analog converter integrated circuits under the control of the logic section. The logic section also controls the front panel LEDs. These indicate the current state of the controller, for example, which thermometer is in the control loop or is the error signal within the acceptable error-limit window.

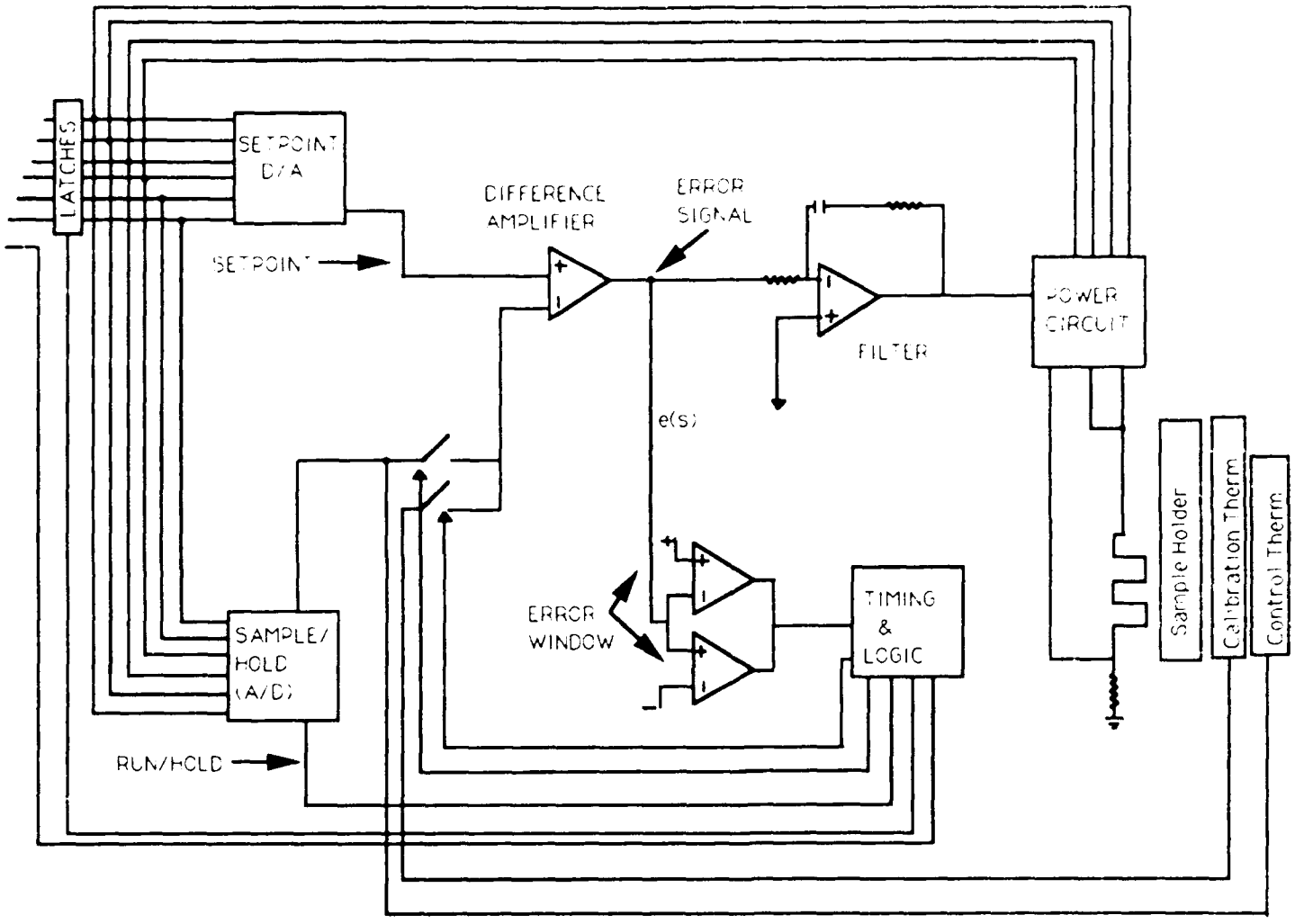


Figure 4 Final Design Block Diagram

IV CIRCUIT DESCRIPTION

Before a detailed circuit description can be given the reader should examine fig. 5, the overall system schematic, and fig. 6, the controller state diagram. The front panel LED's mentioned in the state diagram are 5 different colored LED's mounted on the front panel of the controller and are used to display which state the controller is in at any time. These are simply visual aids that are optional but recommended .

It should also be mentioned that the schematics in this report have some minor components or circuit connections omitted for clarity. None of these are critical to understanding the operation and design of the system, they are typically trim potentiometers or power supply connections. Their inclusion would have made the schematic more cluttered and added nothing to the analysis of the operation of the controller.

1. SETPOINT D/A AND SAMPLE-AND-HOLD A/D (figure 7)

The voltage drop across a calibrated silicon diode located in the sample holder (fig.11) is used for all temperature measurements in this system. The desired temperature setpoint is converted to its corresponding voltage from a calibration table stored in the controlling computer, this voltage is then converted to 16-bit binary and output to the temperature controller along with a positive-going strobe pulse from a TTL-parallel computer I/O port. Since the setpoint digital-to-analog convertor (D/A) in the current design has a maximum output voltage of 5 volts, the conversion algorithm is INT(Vdes/5.0)*65535. The strobe signal clocks the 16-bit setpoint into U1, U2, and U3. The strobe is also routed to the controller's logic section where it resets all circuitry to a known initial state. This initial state will be referred to as state (0) . In this state the outputs of U1 and U2 are enabled and D0-D15 of U6 (the sample-and-hold A/D) are disabled so the latched binary values in U1 and U2 are input to U7, the setpoint D/A. U4 and U5's only function is to invert the binary signals to the setpoint D/A. This is because the D/A (U7) in the current design requires a complemented straight binary input(CSB), future designs will not require this and U4 and U5 can be omitted.

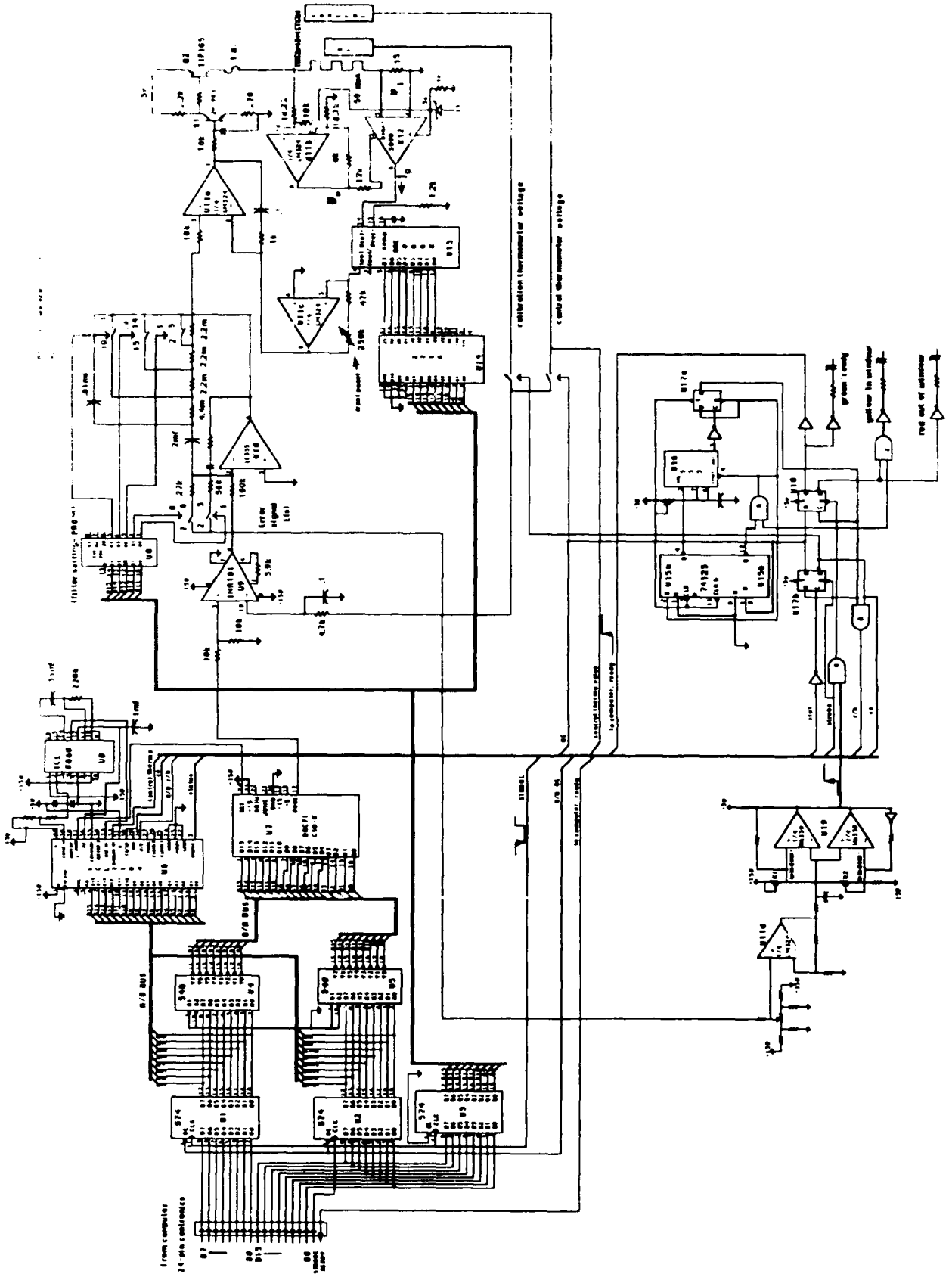


Figure 5 [illegible] schemati[illegible]

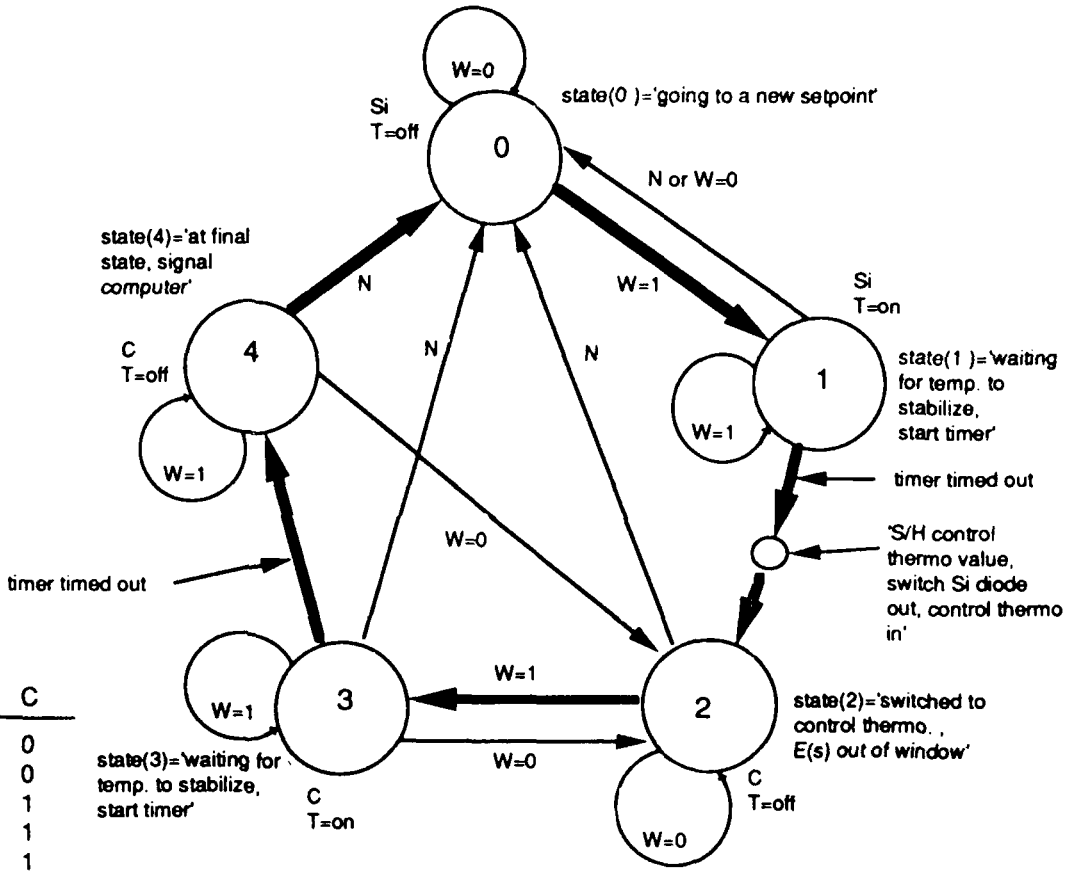
"N"=new setpoint
reset system

"W"=1, E(s) in window
"W"=0, E(s) out of
window

"T"=1, timer running
"T"=0, timer off

"Si"=silicon diode
thermometer
in control loop

"C"= control thermo
in control loop



FRONT PANEL LED TRUTH TABLE

state	red	yellow	green	Si	C
0	1	0	0	1	0
1	1	1	0	1	0
2	1	0	0	0	1
3	1	1	0	0	1
4	0	0	1	0	1

Figure 6. Controller State Diagram

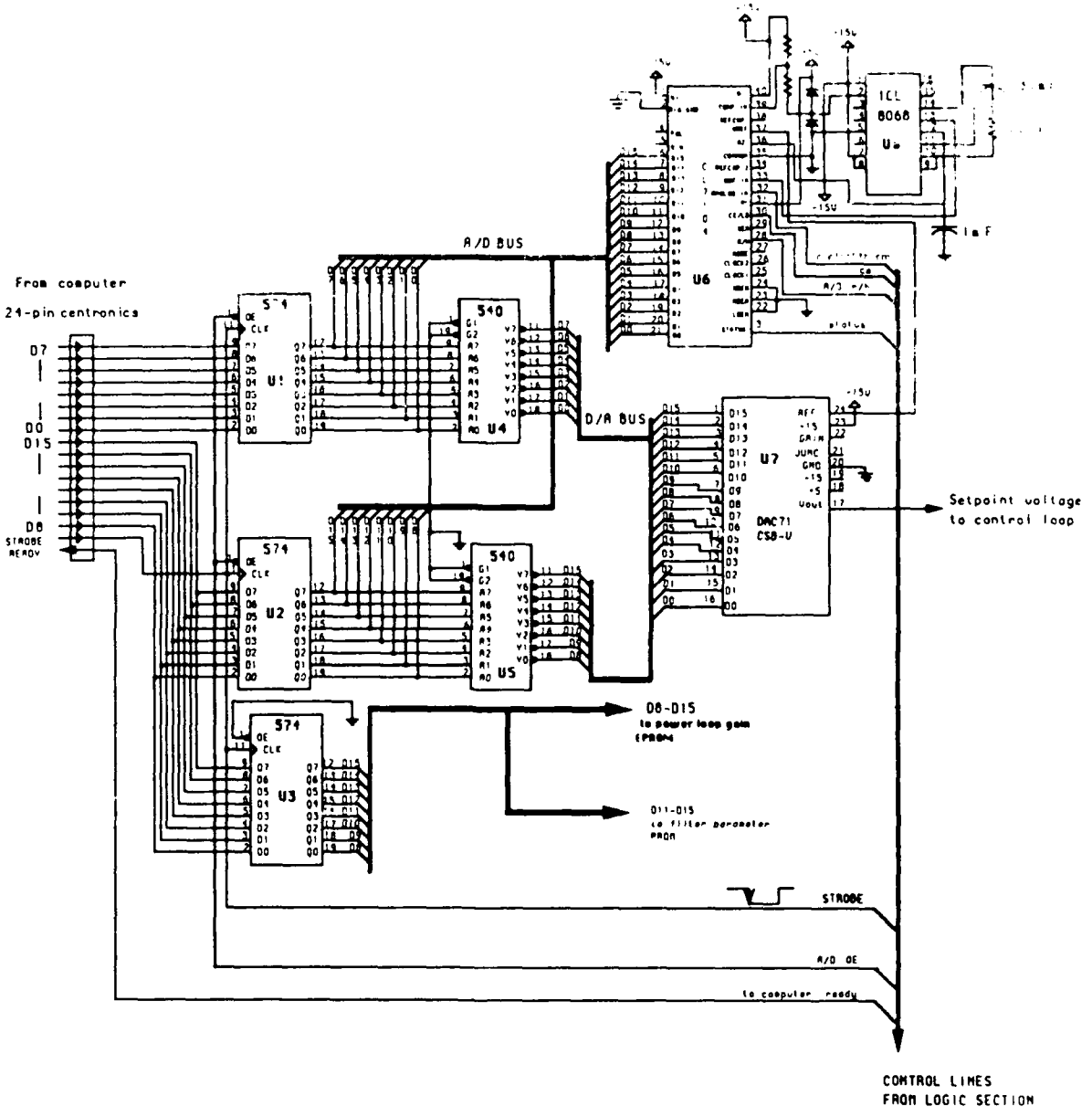


Figure 7. Setpoint Latching and Sample/Hold Circuit

The sample-and-hold A/D (U6) analog input is wired directly to the output of the control thermometer so that when the run/hold line to the A/D is asserted the control thermometer value is sampled and stored. The logic section disables the output of U1 and U2 and enables the output of the A/D (U6), thus when this switch takes place the sampled value of the control thermometer becomes the new setpoint value and remains so until a new setpoint from the computer is latched in and the controller is reset.

U3 also contains the uppermost 8 bits of the setpoint from the computer as does U2. U3 is necessary in this system because the values of these bits are monitored by other sections of the circuit and need to be active at all times. Since the output of U2 is disabled between state (1) and state (2) in the state diagram (fig. 6), these bits must be be stored in another latch that is always active. U8 is a companion chip to U6 and this 2-chip set can be treated as a single A/D block. Future designs will use a 1 chip A/D, reducing chip count and printed-circuit board space.

2. CONTROL LOOP (figure 8)

U9, a difference amplifier, receives as input the setpoint voltage. It compares this value with the feedback from the thermometer and generates an error signal E(s). E(s) branches to two circuit sections: the first to an error window comparator circuit in section C, the logic and timing circuit, the second to a position-integral(PI) filter to condition the signal before driving the heater power section. The damping and time-constant values of the filter must be changed to track the changes in thermal response of the sample holder. This is accomplished by changing the values of the input resistors and the feedback resistors to U10. The correct filter settings corresponding to the current temperature are stored in a programmable read-only memory (PROM) IC, U8. The outputs of U8 drive analog FET switches (LF13201) which perform the resistor switching functions. The conditioned error signal is routed to U11a, the input to a minor loop. This minor loop, consisting of U11, U12, U13, and U14, acts as a variable gain, error-voltage-to-power conversion block. U11a drives the Q1-Q2 transistor pair into conduction which forces current into the sample holder heater windings. U11b senses the voltage drop across the heater while the

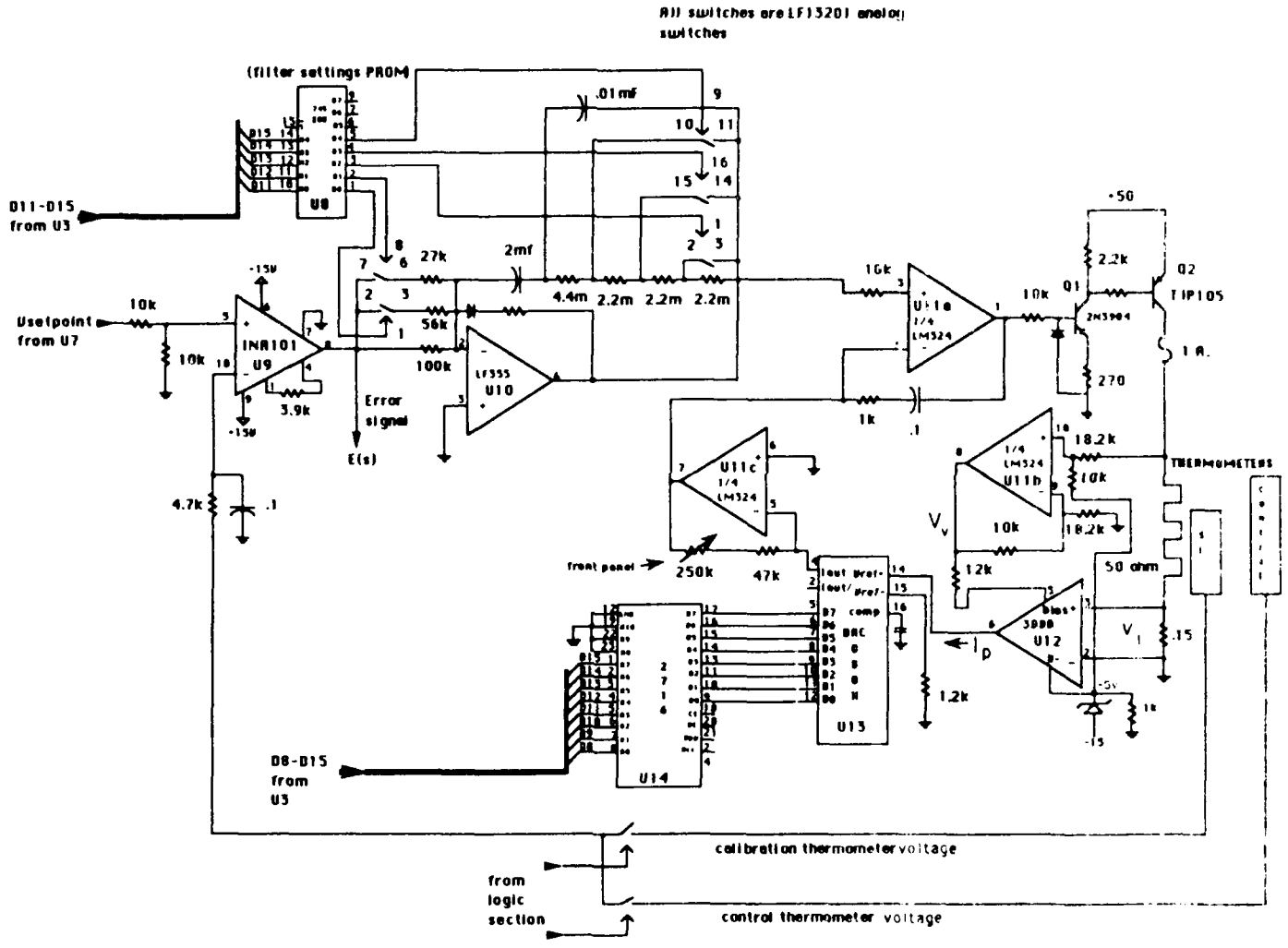


Figure 8 Control section

voltage drop across the .15Ω sense resistor at the input to U12 is a heater current signal (V_i). U12, an LM3080 transconductance amplifier, generates a current whose magnitude is proportional to the product of the voltage difference at its inputs and the current into the pin labeled bias current. The output of U11b (V_v) and the heater current signal (V_i) are multiplied by U12. The magnitude of the current out of pin 6 of U12(I_p) is directly proportional to the power dissipation in the heater windings. The U14-U13 IC pair function as a means of varying this loop's gain. If the binary inputs to U13 are all 1's then I_{out} of U13 equals I_p, otherwise I_{out} is reduced linearly as the binary input value to U13 is reduced. Reducing I_{out} has the effect of increasing the loop gain, i.e. a binary input to U13 of 255 gives the minimum minor loop gain, an input of 1 gives the maximum loop gain. U14 contains the table of gain values necessary to compensate for the changes in thermal response of the system and maintain major loop stability. U11c acts as a current-to-voltage converter and closes the minor power loop by feeding its output to U11a, pin 2. Adjustments in gain can be made manually by varying the value of the 250kΩ potentiometer in the feedback path of U11c, this pot is mounted on the front panel of the controller. It should be noted that since the feedback signal in this minor power loop is proportional to the power dissipation in the heater windings, the resistance value of these heater windings is not critical. This has been tested by increasing the heater resistance to 100Ω from its normal 50Ω value. There was no visible effect on controller accuracy or controllability.

Two thermometers monitor the temperature of the sample holder. Depending on which state the controller is in, either the calibration silicon diode voltage or the control thermometer voltage is fed back to U9, thus closing the major control loop.

3. TIMING AND LOGIC (figure 9)

When a new setpoint is received from the computer a negative-going pulse on the strobe line resets U15, U16, U17, and U18. This resets the system to state (0); see fig 6. The temperature error signal, E(s), is input to the comparator window circuit. This circuit is made up of ICs U11d, and U19. After being amplified by U10 (fig. 8) and U11d, the error signal is about 500X the actual temperature error. The error window limits, window+ and window-, are set at +.1 volt and -.1volt so the actual temperature error swing allowable is (.2v/500) , about .4mV. This allows a very limited temperature drift at 20°(70mV/°) and a considerably greater drift at 300°(2.5mV/°). When E(s) is sufficiently small the output of the window comparator snaps to logic '1' state. This signal is gated through AND gates A and B and triggers U15a. U15a simply converts the positive change of state of the window comparator to a short negative pulse and starts the timer running, U16. This puts the controller in state(1) of the state transition diagram. If the timer runs to completion without being reset it generates a pulse at pin 3 and sets U17a, a D flip-flop. This translates to the the actual temperature being at the setpoint (E(s)≈0) for a sufficiently long period of time to assume that the temperature is stable. The logic '1' state of the Q output of U17a ANDED with the logic '1' of the Q' output of U17b sets the R/H line to the S/H circuit (section A) to 'run'. The S/H returns a pulse on the A/D status line when a control thermometer voltage value has been sampled. This pulse sets U17b and resets the S/H circuit to 'hold'. When U17b (a D flip-flop) is set, the Q and Q' outputs of that IC force several things to occur:

1. The silicon diode calibration thermometer is switched out of the main control loop.
2. The control thermometer is switched into the main control loop.
3. The outputs of latches U1 and U2 (section)are disabled , (OE = '1')
4. The output lines, D0-D15, of the sample-and-hold A/D are enabled, (ce = '0')
5. The '0' to '1' transition at the Q output of U17b triggers U15b into generating a short pulse. This pulse resets U15a, U16, and U17a. This puts the controller logic in state (2) of the state transition diagram.

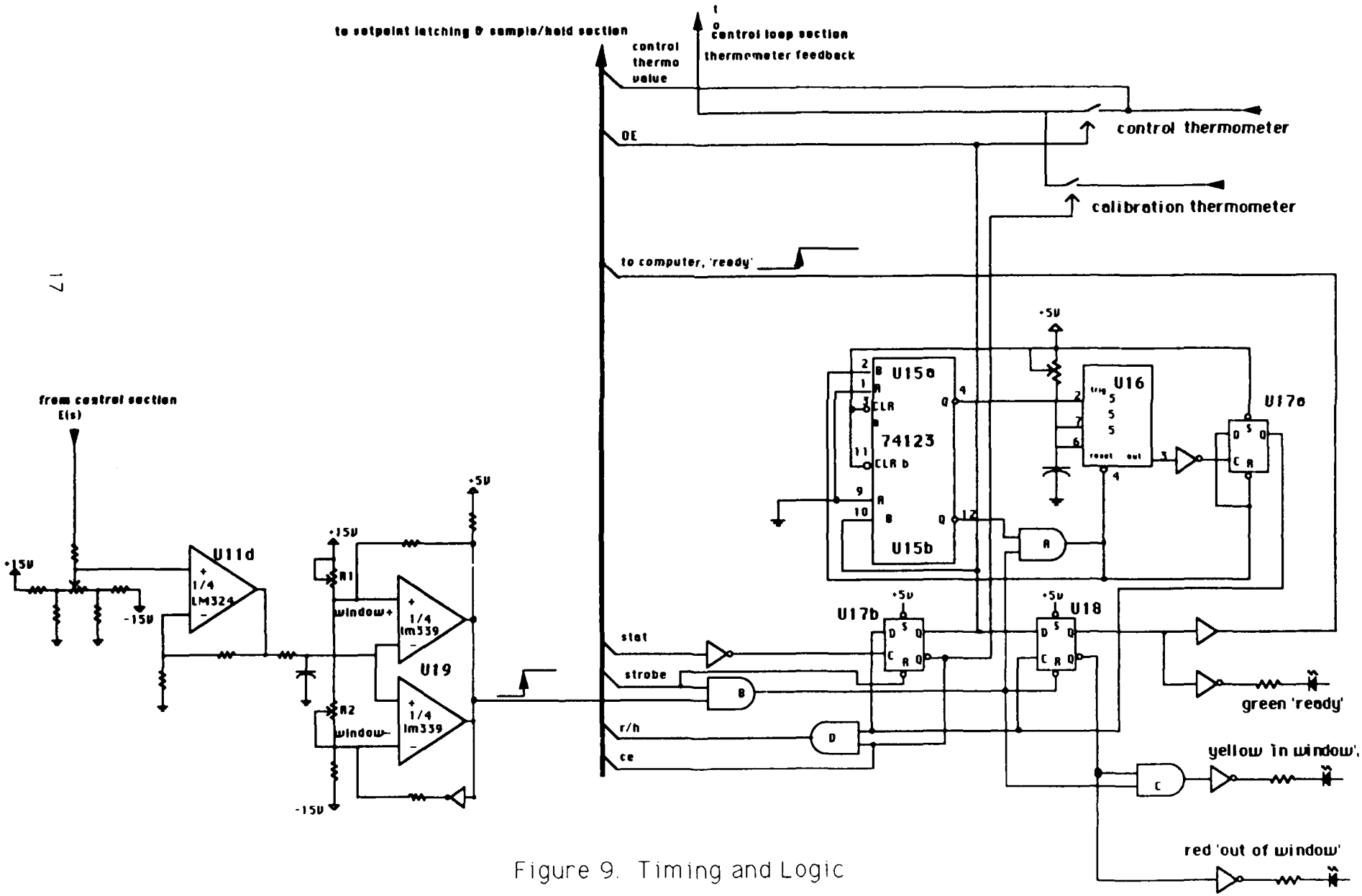


Figure 9. Timing and Logic

... E(s) is within the error window limits again, using the control thermometer for control loop setpoint and feedback values, the controller moves to state (3). Again the timer, U16, is triggered. If it runs to completion its output pulse negative edge sets U17a which in turn sets U18. The controller is now in state(4) and remains there unless E(s) drifts out of the error window or a new temperature setpoint is received. This cycle is repeated for every temperature setpoint in a data collection run.

4. The Control Thermometer (figure 10)

In the other circuit sections the control thermometer is simply shown as a box which generates a voltage that varies in some predictable way with sample temperature. This is because different end users may wish to use different control thermometer circuits depending on their system requirements. This section describes the circuit we use and what system constraints are met in this design. This controller's design requires that the sampled control thermometer have a negative Δvoltage/Δtemperature with roughly the same magnitude as the calibration silicon diode, see fig. 2. The makes the control loop design simpler since the thermometer voltage response is an important control loop parameter. If the control thermometer has roughly the same response as the Si. diode then the loop gain won't need to be adjusted to compensate when the control thermometer is switched into the control loop.

The design shown in fig. 10 is the control thermometer circuit that we currently use. The platinum and carbon-glass resistor/thermometers are mounted on the sample holder near the heater windings on one end of the copper block. Since both thermometer cases are cylindrical we simply insert them into cylindrical holes drilled into the sample holder. Thus they have a 360° contact surface with the copper block. The platinum resistor, marked PT in the schematic, has good thermal sensitivity from about 30°k to 380°k. The carbon-glass resistor, marked CGR in the schematic, has good thermal sensitivity from 5°k to 40°k and also has a low magneto-resistance in this range. Our circuit design adds and conditions the response of the two thermometers to form a control thermometer with desireable characteristics from 5°k to 380°k with a minimal magneto-resistance.

Each thermometer has an excitation current driving it. Their voltage drops are amplified and then added. Q4 acts as a low-noise front end for U21, they can be considered a single op-amp which amplifies and filters noise from the platinum resistor. Q5 and U22 act in the same respect for the carbon-glass resistor. Future designs will probably omit Q4 and Q5 since some very low-noise operational amplifiers are now available that could be used in place of U21 and U22. Since the output of U21 increases with temperature and the output of U22 decreases, U23 can be considered as adding the two thermometers' responses and generating a single control

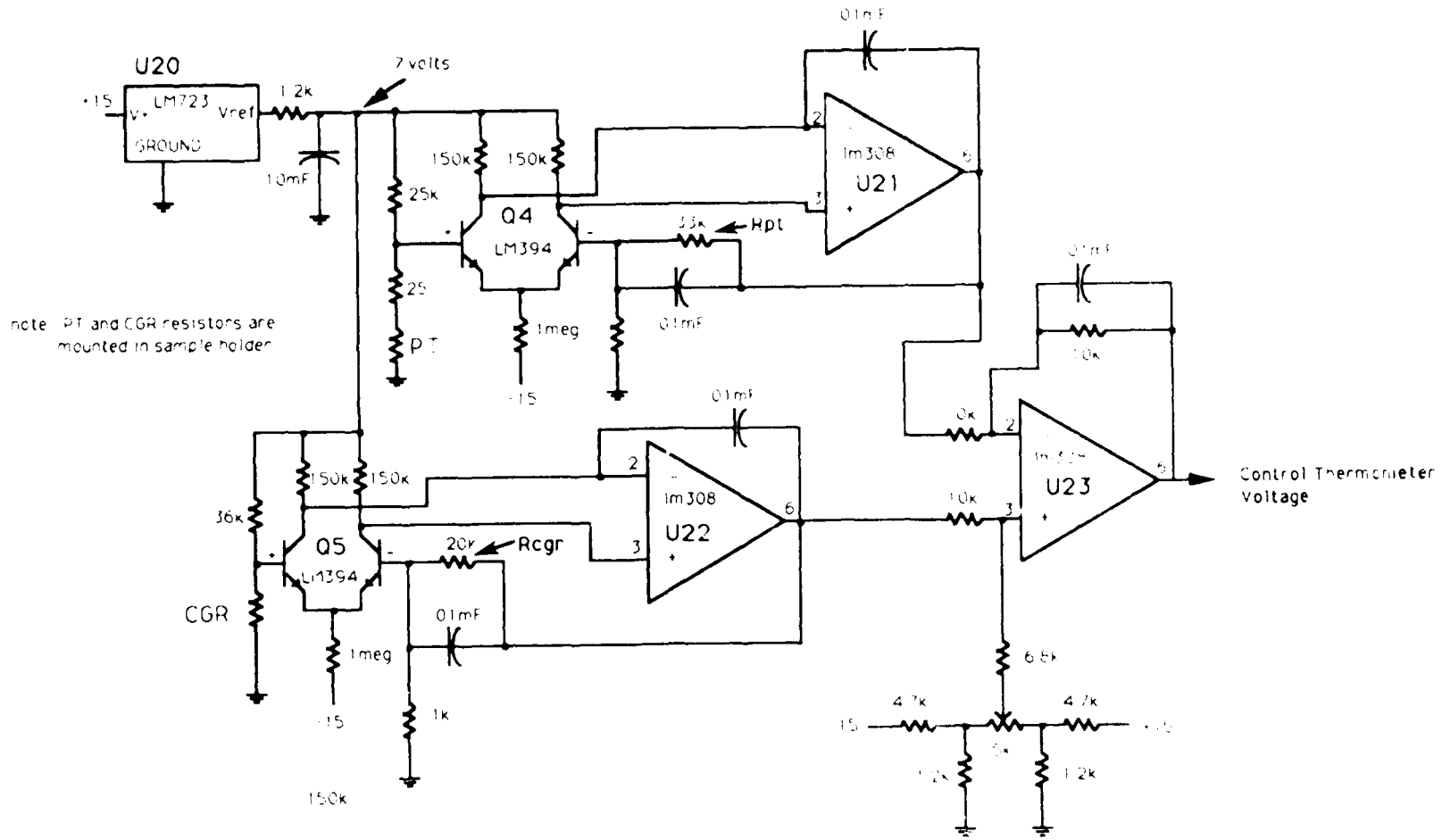


Figure 10. Control Thermometer Section

thermometer signal from their sum/difference. This circuit-thermometer configuration allows a designer to customize his thermometer response to fit the control requirements. By varying R_{PT} and R_{CGR} the thermometer sensitivity can be varied at different temperature ranges. This general concept can be expanded to three or more thermometers if more op-amps are added and summed with the above. U23 provides a low source impedance control thermometer signal for the control loop.

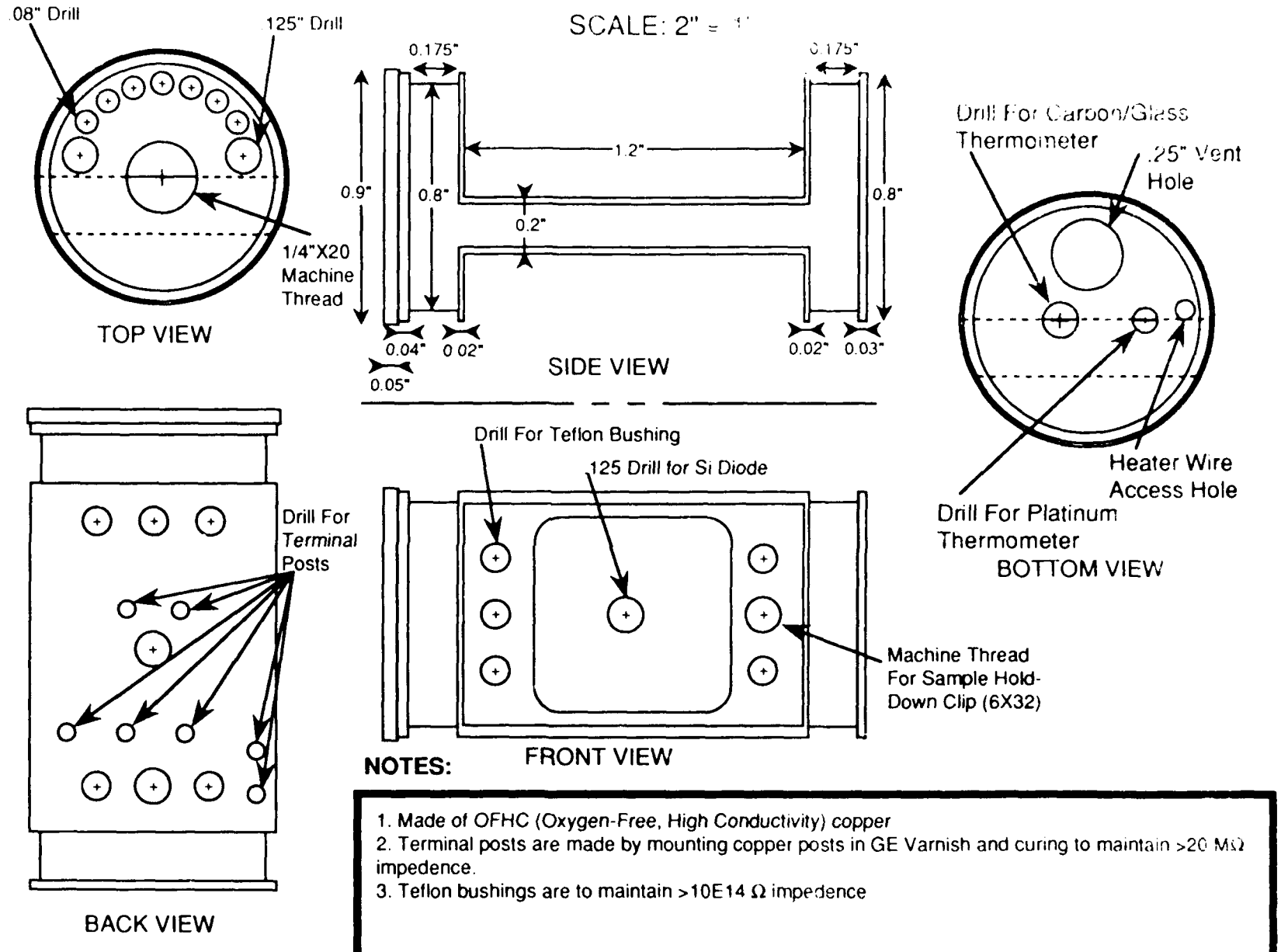


Figure 11. Sample Holder Block

V. CONCLUSION AND RESULTS

The basic controller design described above is used daily in the Electrical Transport Properties Lab in the Electronic and Optical Materials Branch of the Materials Laboratory. There are currently three controllers constructed, two in use and one back-up. They have proven extremely reliable. The original controller, built in 1983, is still in operation. The last controller built used printed circuit boards for easier maintenance and reduced size as opposed to the first two which were built with point-to-point wiring.

There are many improvements and simplifications which will be incorporated into future designs if more controllers are needed. It is estimated that the chip count could be reduced by 33% if we spent the time to do so. As an example, future controllers, if built, will use a 12-bit D/A and A/D chip set as opposed to the current 16-bit IC's used. Since we are primarily an electronic materials characterization lab and not an electronics design lab it is questionable as to how cost effective it would be for us to continue improving this controller should a commercial controller be introduced which meets our requirements. This controller design also has some shortcomings; it requires that the magnetic field be switched on and off at each setpoint, i.e. it will not work at different temperature setpoints if the magnetic is constantly present. Also, it has no provision for stand-alone operation; it requires computer control.

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   Wilmington, MA 01887

*U.S.Government Printing Office: 1989 — 748-056/24184