Effects of Heavy Ions on Microcircuits in Space: Recently Investigated Upset Mechanisms

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Upsets of microcircuits in space have been attributed to heavy ions. In recent studies of the failure mechanisms, we have employed a wide range of test methods. These studies and the application of the test results to space-borne microcircuits are presented.

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PREFACE

We would like to thank our colleagues at The Aerospace Corporation for their generous assistance in the development of the instrumentation and software and in the collection of data. Our thanks are also due to the staff of the LBL 88-in. cyclotron, without whose support and efficient operation of the accelerator, this work would not have been possible.

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FIGURES

I. INTRODUCTION

The effects of cosmic rays on microcircuits in space have been studied for over a decade. A cosmic ray can deposit sufficient charge in the sensitive volume of a semiconductor device to cause temporary upset--single event upset (SEU)--of the logic state. In order to predict such an upset, we must know the space heavy ion environment, as well as the susceptibility of a microcircuit to these ions. Since a detailed description of the environment has been provided by Adams et al. (Ref. 1), it is possible, in principle, to obtain an upset prediction by use of a computer program, provided the susceptibility of a device and the orbit are known. However, the susceptibility of a device to heavy ions appears to elude a simple description, mainly because the geometry of basic circuits and the technology with which they are fabricated vary widely.

It was only a few years ago that we started observing the susceptibility of bistable elements, such as random access memories (RAMS) and latches, at an accelerator site, where we had a copious supply of simulated cosmic rays--especially heavy ions. We used a test chamber in which a microcircuit can be mounted, as shown in Fig. 1. The beam properties and fluence are monitored using the solid state detector, the scintillation foil, and the position sensitive detector. A more detailed description of the test procedures can be found elsewhere (Ref. 2). Briefly, the procedure used to measure the SEU susceptibility of a microcircuit is as follows. An individual chip is irradiated with a known total fluence of particles, and the total number of errors is recorded. The bit error probability (or cross section) is calculated from the expression $\sigma = (N/F) \sec \theta$, where N and F are the number of bit errors and beam fluence, respectively, and θ is the incident angle of the beam measured with respect to the chip-surface normal. By appropriate choice of ion species and orientation of the microcircuits under test, it is possible

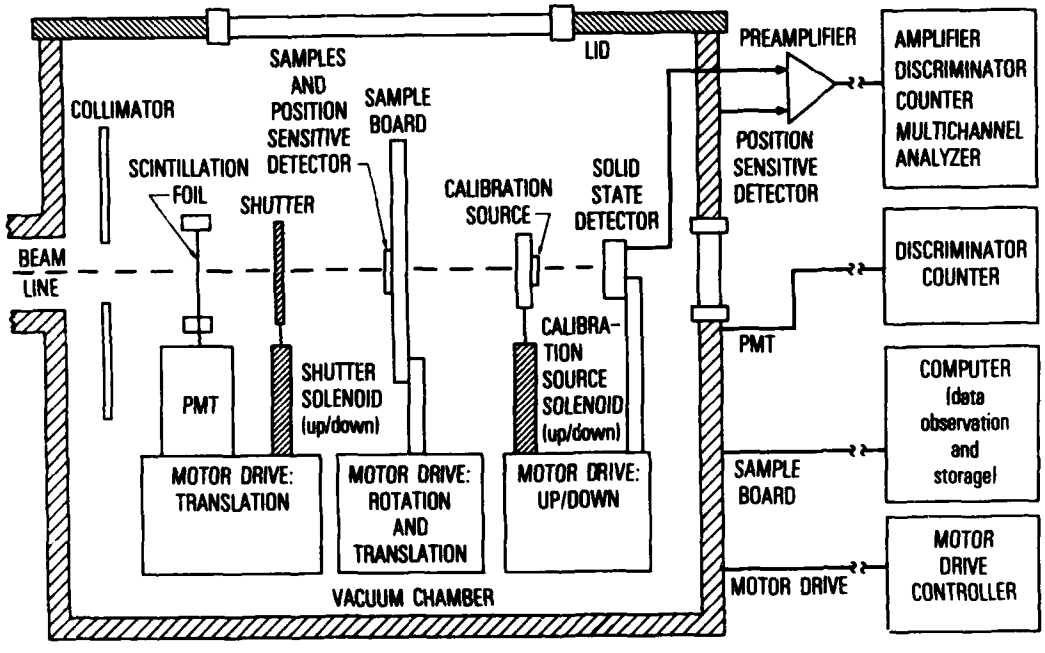

Fig. 1. Schematic Presentation of the Experimental Setup

to obtain the saturation cross section and the threshold linear energy transfer (LET) for upset. An example is shown in Fig. 2.

Recently, we have expanded the studies to include the measurement of types of upsets which may not have been observed earlier. First, there are upsets that have a finite lifetime (Ref. 3); these upsets are expected to appear predominantly in the fast RAMs and must be measured quickly within the range of the time decay of the stored charge.

A second type of error is that associated with combinatorial logic circuits (Ref. 4), such as the arithmetic and logic unit (ALU) of a microprocessor. Once such an error is transferred to a bistable element, it becomes permanent. We have chosen the M6800 microprocessor for this study.

Third, testing for vulnerability to SEU and latch-up has been performed at temperatures other than room temperature in order to assess the characteristics of microcircuits operated at the extremes of the temperature range encountered in operational spacecraft.

In what follows, we summarize the current experimental efforts to understand the susceptibility of microcircuits to heavy ions in space.

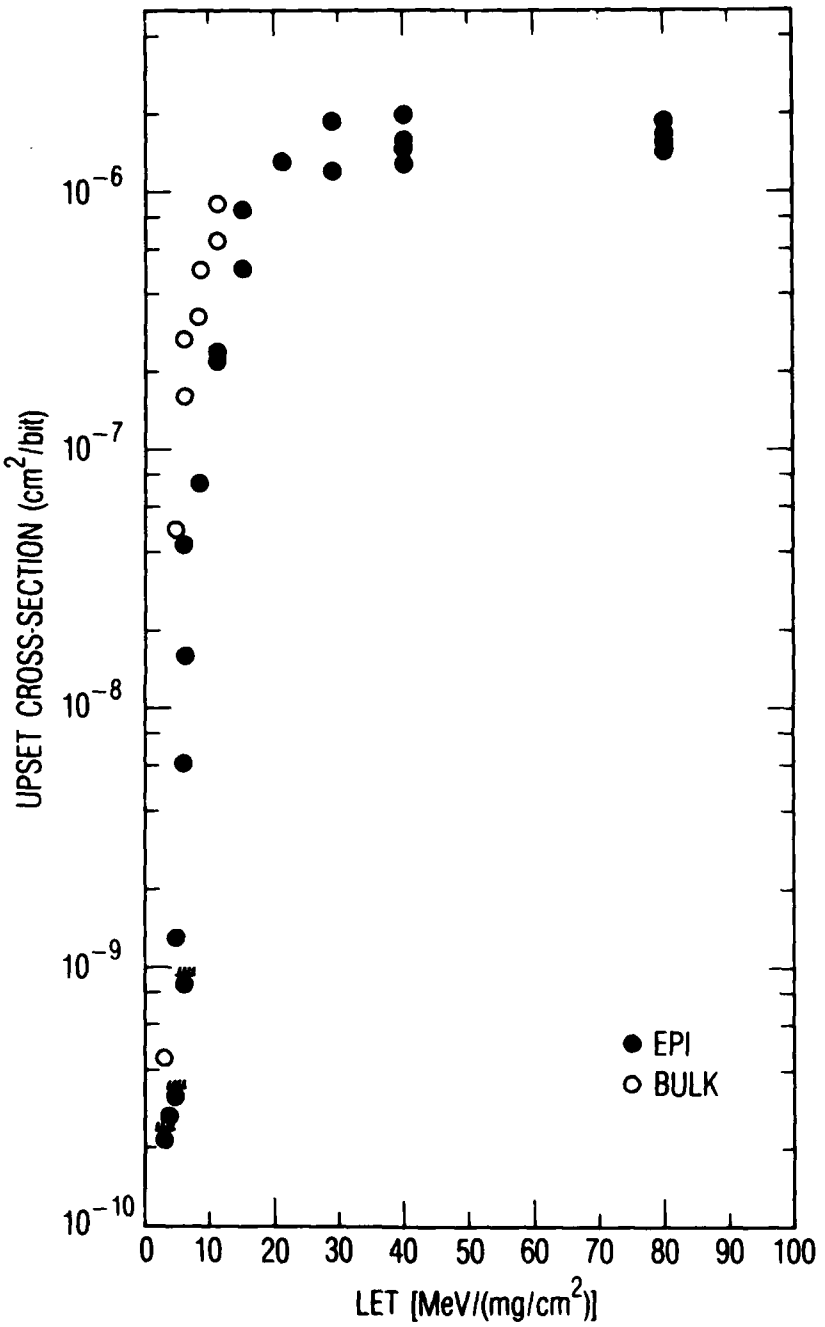

Fig. 2. SEU Cross Sections Obtained from IDT71681 (4k x 4 NMOS RAM)

II. UPSET MECHANISMS AND OBSERVATION TECHNIQUES

A. SINGLE EVENT DISTURBED PHENOMENON

It has been reported that a new class of single event soft errors was "observed" during a computer simulation study (Ref. 3). It was predicted that these soft errors would occur in static random access memory (SRAM) cells containing transistors with very high resistive loads, and that the critical charge for these errors would be less than or equal to that for the normally encountered type of SEU. It is stated in Ref. 3 that these new upsets, termed single event disturbed (SED) upsets, manifest themselves in the following way: "Attempts to read disturbed RAM cell states can introduce errors, even if the cell held correct information before the transient and will recover without upset. Some of the latest high density static RAM designs can be misread for milliseconds after a single event interaction that does not cause upset." Accordingly, we decided to look for erroneous read outputs, followed by a spontaneous recovery. Since it is difficult to predict the relaxation time of the disturbance from the theory (Ref. 3), we decided to cover a time range between 10 nsec and 2 sec.

We chose IDT6116 (2k x 8) and IDT71681 (4k x 4) RAMs for the study. The cells of these RAMs have high resistive loads, as shown in Fig. 3a. These should be compared with the standard 6-cell complementary metal oxide semiconductor (CMOS) cell, shown in Fig. 3b, where the loads are active transistors. Because of the active load, the relaxation time is short, and no SED upsets are expected in a CMOS cell.

It was not easy to adapt a single test method to cover the approximately eight orders of magnitude in the relaxation time. We therefore performed the study in two parts, using two different test methods. In the first part, we searched for events with relaxation times of several microseconds to a few seconds. In the second part, we looked for SED errors in the time range of several nanoseconds to several

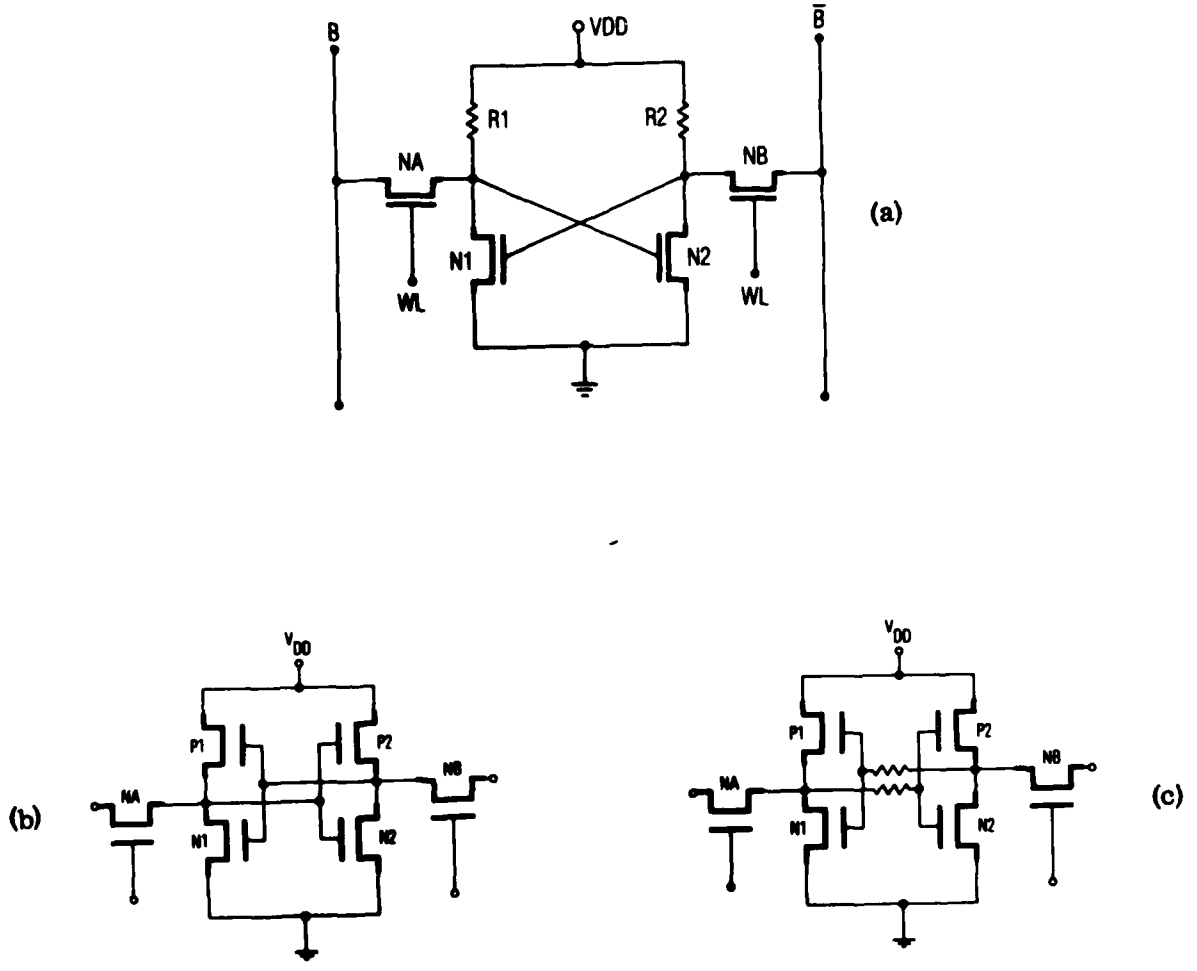

Fig. 3. (a) A Four-Transistor NMOS RAM Cell with High Resistive Loads; (b) A Six-Transistor CMOS RAM Cell; (c) A Six-Transistor CMOS RAM Cell with Cross-Coupled Resistors.

microseconds. For the first phase of the study, we developed a program to repetitively read the contents of a single-byte address location as fast as our computer would allow--every 7 μsec. The flow chart of the program is shown in Fig. 4. Upsets that recover spontaneously (SED upsets, by definition) are detected in Loop A of the program in Fig. 4. Upsets that do not recover spontaneously are recorded as SEUs in Loop B. Before exposing a device to an ion beam, the program set the read counter (RC) to some predetermined number and filled the address location of the byte under interrogation with a checkerboard pattern (8 bits). During beam exposure, the contents of the byte address were read out every 7 μsec. If an error was found, it was recorded, and the RC was decremented by one. This read cycle was repeated until the error was no longer seen, or until the contents of RC became zero. If recovery was observed (Loop A), the error was tagged as SED; otherwise, it was classed as SEU. The basic time period of the event detection could be varied from 17 μsec to 20 msec (see Fig. 4). We called the preceding program Test Program A (dynamic measurement). For the dynamic measurements, the RC was normally set at 100, and the delay was set at 17 μsec, meaning that once an error was found, the tester would keep interrogating for an additional 99 times (100 x 17 μsec = 1.7 msec). With a delay of 20 msec per detection, the additional 99 times in reading would mean testing the RAM cell for 2 sec.

In addition to the preceding Test Program A, we also used our two standard SEU programs: Test Program B and Test Program C.

In Test Program B, a pattern was written at all address locations on the RAM and then sequentially interrogated without delay in order to check for errors. This process continued while the device under test (DUT) was being exposed to the beam (semi-dynamic or semi-static measurements).

In Test Program C, a pattern was written at all address locations before exposure to the beam. After an appropriate exposure time, the beam was turned off and the device checked for errors (static measurement).

The nominal test cycle of "(write)/read/check" required 7 μsec, 5 msec, and 20 sec for Test Programs A, B, and C, respectively. It should be

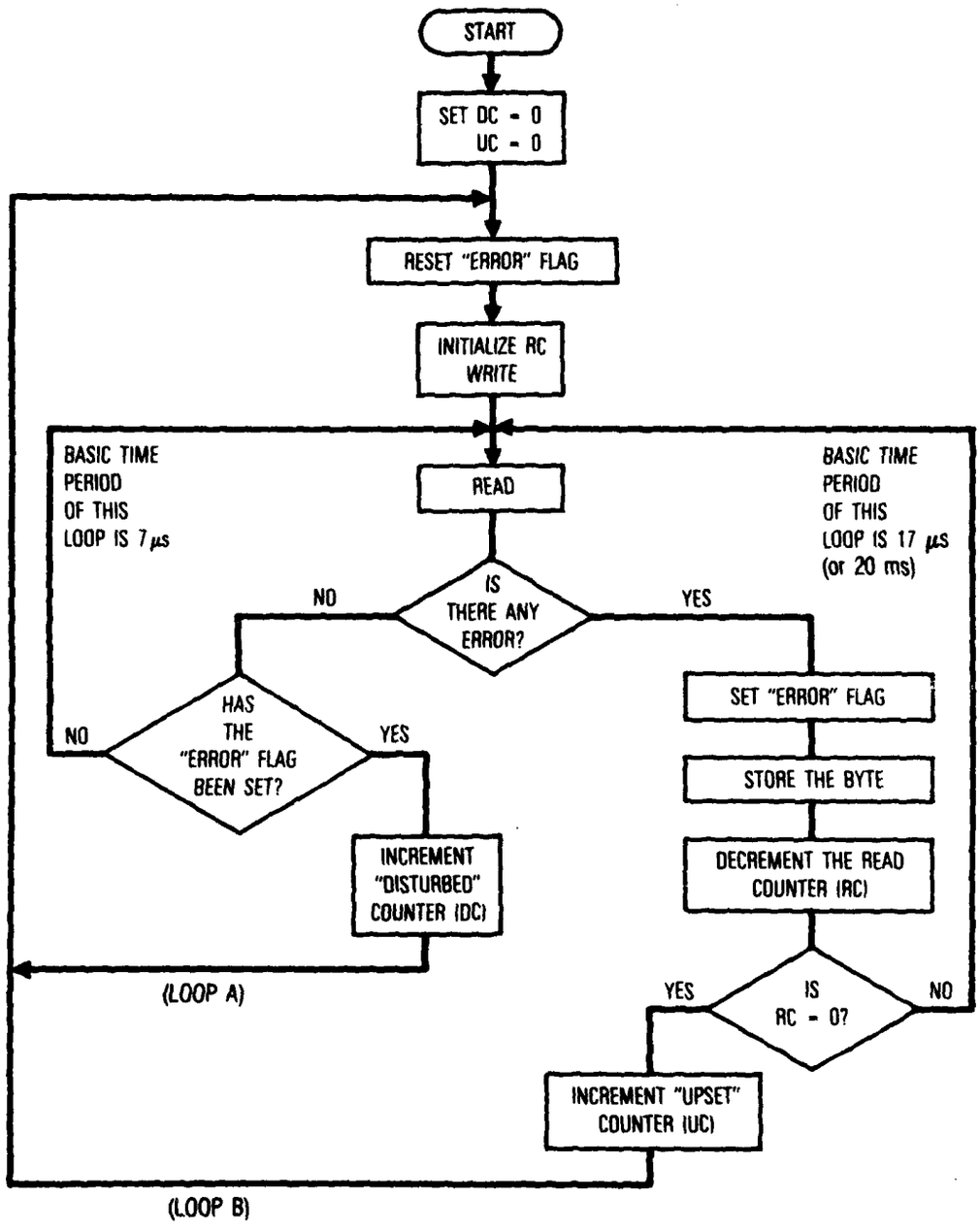

Fig. 4. Program Flow Chart of the IDT6116 2k x 8 RAM Tester

noted that all address locations were interrogated during each read cycle of Test Programs B and C, while only one address location was interrogated in Test Program A.

We used Kr(270 MeV), Ar(163 MeV), Ne(84 MeV), O(35 MeV), O(160 MeV), and N(63 MeV) ions for the preceding observations.

The flux of ions was adjusted so that during the execution of the dynamic program, any given memory cell location was struck by particles approximately once per second. For semi-dynamic and static programs, the rate was about 10 to 100 times slower.

We observed no error that recovered spontaneously within the limits imposed on the time of recovery (TR) by the experimental technique. The limits on TR were from 7 to 2,000,000 μsec. During the study, we saw thousands of normal SEU errors. The error rates (cross section) vs LET for these errors are plotted in Fig. 5. Three groups of upset data are shown. Closed circles show the results of the static measurements C. Open triangles indicate the results of the semi-dynamic measurements B. Open squares indicate the results of the dynamic measurements A. At the larger LET, the discrepancies among the data points derived from the three measurements are rather small--a factor of 2. For LET between 6 and 10 MeV/(mg/cm^2), the faster the read cycle, the larger the cross section. For LET of less than 6 MeV/(mg/cm^2), the cross sections tend to converge.

In the second portion of the study, we addressed relaxation times between several nanoseconds and several microseconds. The RAM data lines were continuously monitored by the logic analyzer during the read-out cycle of the RAM. The logic analyzer was programmed to trigger, once the contents of the data deviated from the specified value. This set of studies did not reveal any candidates of SED upsets for IDT6116 RAM, as shown in Fig. 6. When a cell was enabled, upset bits triggered the logic analyzer (see T in the figure). The flip from "0" to "1" appears to be delayed because of an external capacitance in our detector circuit.

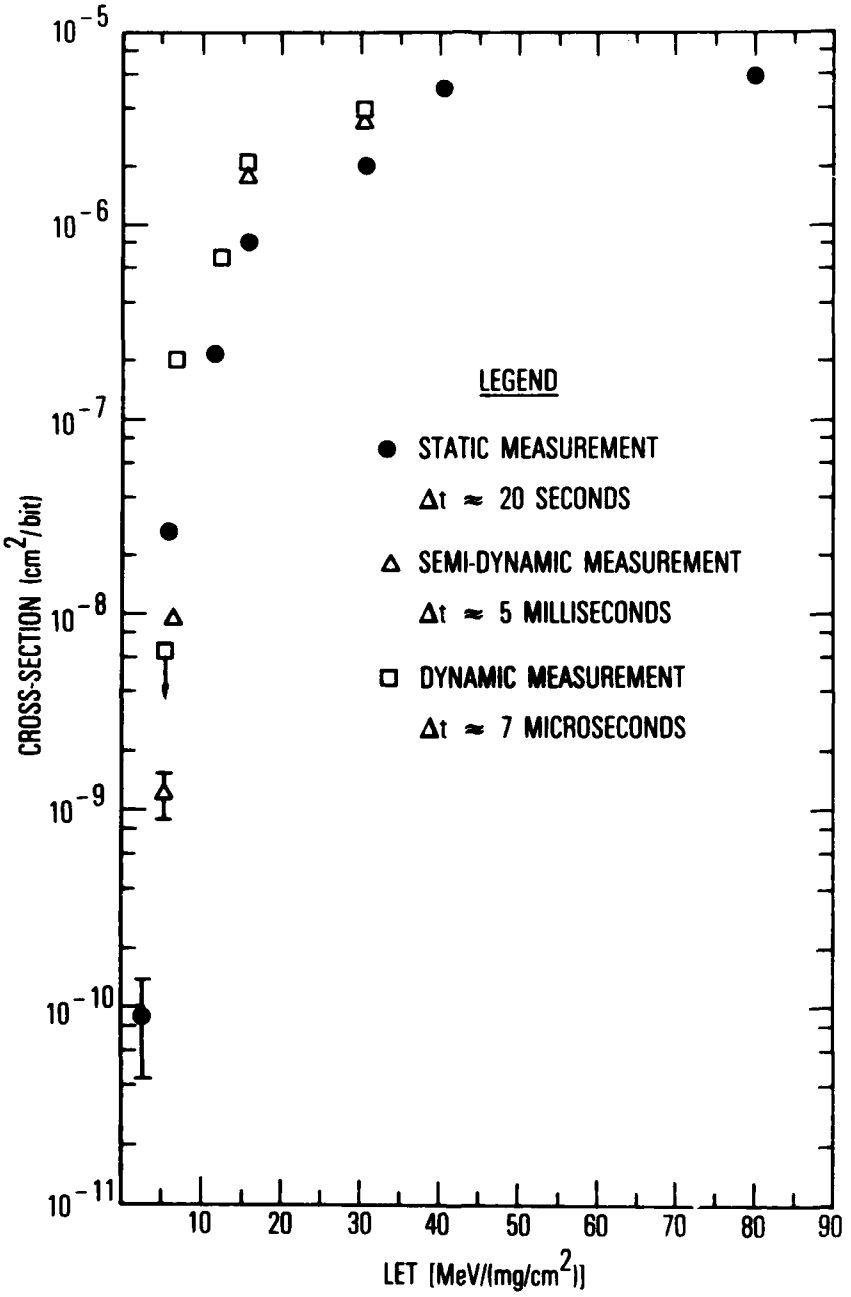

Fig. 5. A Comparison of Cross Sections for IDT6116 2k x 8 RAM Obtained Using the Three Test Programs

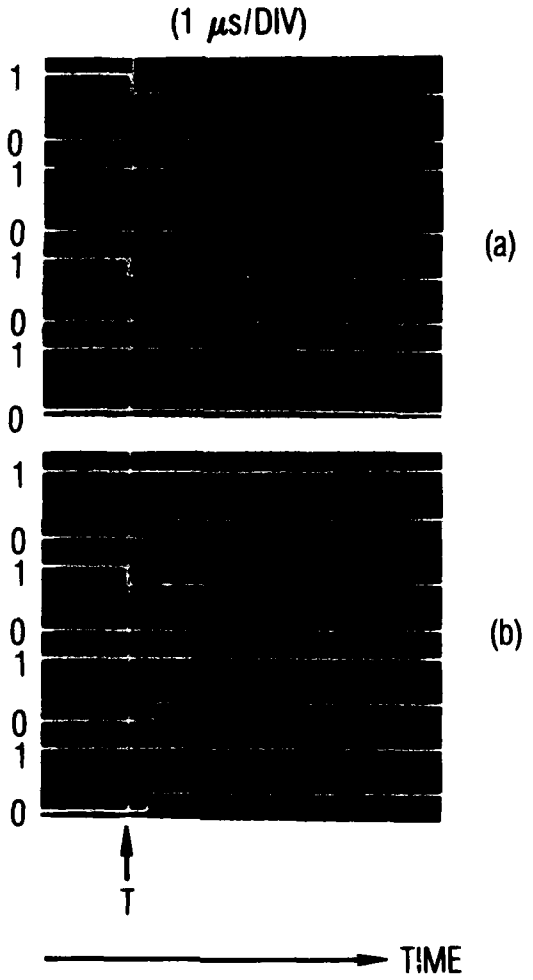

Fig. 6. Snapshots of 8 Bits (IDT6116 2k x 8 RAM) Captured by the Logic Analyzer. (a) Two upsets from "1" to "0"; (b) One upset from "1" to "0", and 3 upsets from "0" to "1". Because of an external capacitance, the transitions from "0" to "1" have some delay time.

We decided to look for SED upsets in another device, IDT71681. This device (4k x 4 NMOS RAM) has a cell structure very similar to that shown in Fig. 3a, but the device is of a much more recent design (1981 for IDT6116 vs 1983 for IDT71681). The static and semi-dynamic test results for IDT71681 are shown in Fig. 2. The results resemble the data in Fig. 5 for similar tests on the IDT6116.

In the logic analyzer tests of the 4k x 4 device, some striking differences from the IDT6116 results were observed. As before, four data lines were continuously monitored. The logic analyzer was triggered only when a data line deviated from the specified value. The results are shown in Fig. 7. We saw a bit that showed a telltale sign of an SED error, as shown in Fig. 7d. The maximum duration of an SED error was about 1 μsec, and SED errors occurred about 10% as often as SEUs. By increasing the sampling period of the logic analyzer, we attempted to observe SED errors which might last longer than 1 μsec. We did not see any such errors.

B. COMBINATORIAL LOGIC CIRCUIT TESTS

Circuit elements which do not include memory elements have been predicted to introduce upsets (Ref. 4). However, the upsets will normally pass through the circuit elements without causing noticeable consequences (problems). For example, a transistor in an adder circuit can be affected momentarily by a heavy ion. The addition, however, will soon return to the correct value once the charge deposited by the ion dissipates. The matter can be more complicated if the combinatorial circuit elements become complex and also if the outputs of the combinatorial circuit elements are clocked out into memory elements very often. We would like to show one example in order to illustrate this effect. We chose an M6800 microprocessor for this test. The block diagram is shown in Fig. 8. We focused on the ALU, which is described by the manufacturer as not containing a memory element. We measured the susceptibility of two 8-bit general registers (or accumulators), A and B, of the microprocessor. The microprocessor was programmed to transfer the contents of the registers back and forth between A and B (only during exposure to the ion beam). The

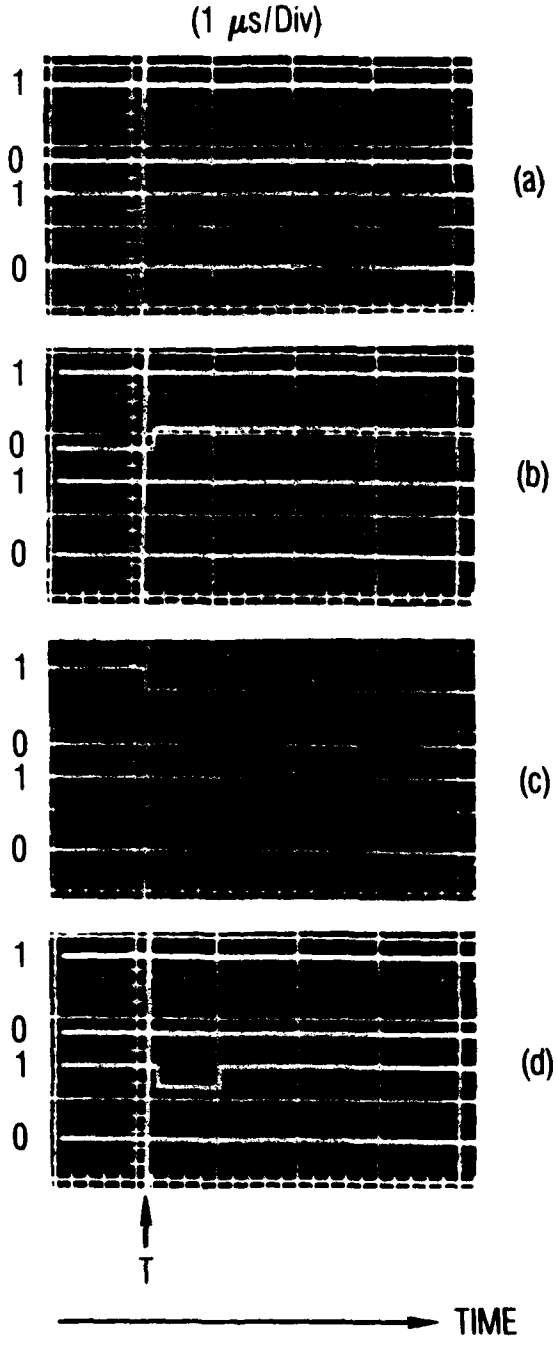

Fig. 7. Snapshots of 4 Bits (IDT71681 4k x 4 RAM) Captured by the Logic Analyzer. (a) No upset; (b) One upset from "0" to "1"; (c) One upset from "1" to "0"; (d) The upset recovers after 1 μsec (a telltale sign of SED)

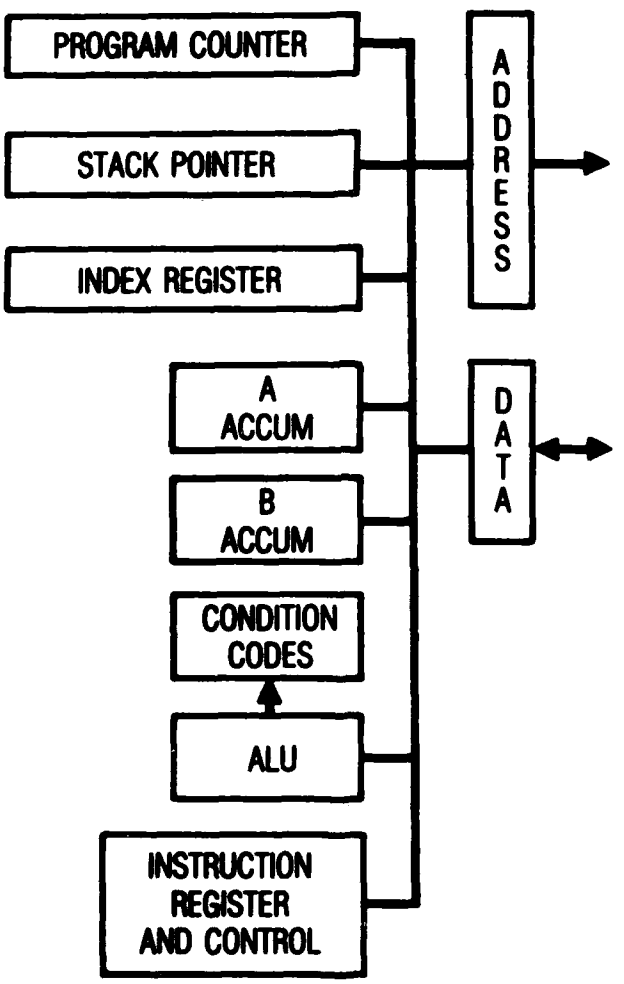

Fig. 8. Block Diagram of the M6800 Microprocessor

8-bit word was periodically tested against the original word. In this fashion, we tested the combined susceptibility of registers A and B. Later the ALU was placed in the program loop to test the vulnerability of the ALU section. It is very interesting to note that a statistically significant upset rate is attributable to the ALU, as shown in Fig. 9. The cross sections for A and B registers as well as P and X registers are also measured.

We have tested many types of microprocessors. The test results of M6800 are by no means typical. The ALU in M6800 is more susceptible to SEU than expected. At the other end of the scale is the ALU of a 4-bit slice processor (AM2901), whose ALU did not show any sign of susceptibility to SEU.

C. ELEVATED TEMPERATURE ENVIRONMENT TESTS

We developed a system where an individual temperature controller (in the form of a heater and temperature monitor) is mounted in good thermal contact with each test device. A single individual controller is put together using a homemade dual-in-line pin socket, a thermistor, and a small wire-wound power resistor (50 Ω). The test device is plugged into the socket and thermally coupled to the power resistor underneath with high temperature epoxy or thermal grease. Thermal epoxy is used to attach the thermistor to the top of the delidded chip carrier, next to the recess where the die is located. With this arrangement, we were able to reach temperatures in excess of 120°C in less than 5 min, starting from room temperature. After a little practice, we could maintain the temperature within 1°C of the desired value, using a control circuit sensing the thermistor output.

The effect of raising the temperature was an increased susceptibility in some RAMs. For example, in the radiation hardened RAM cells, cross-coupled inverters are tied through resistors (several hundred of kΩ in CMOS circuits, as shown in Fig. 3c). The resistance normally prevents upsets by limiting the transfer of charge from the affected transistors

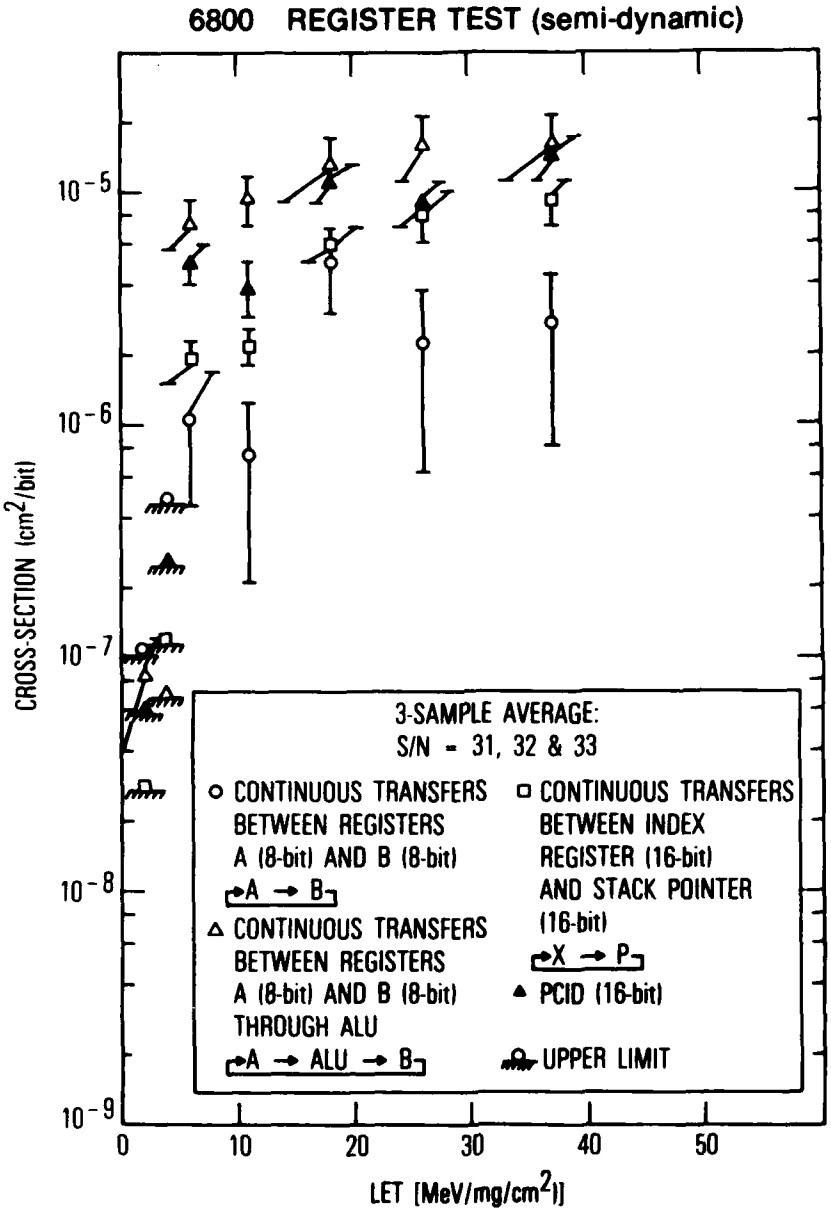

Fig. 9. Upset Cross Section for the M6800 Microprocessor. Registers A, B, P, and X are observed. The combinatorial circuit element, ALU, is also measured against SEU.

(Ref. 5). However, a raised temperature reduces the resistance, increasing the susceptibility to upset.

In testing the SNL RAMs, we obtained data on two devices with 400 kΩ resistors (SN 5551 and 5567) and on two devices with 130 kΩ resistors (SN 5 and 2267). Figure 10 shows the upset cross section, plotted as a function of temperature, for the 5551, 400 kΩ device. The onset of errors is observed above 100°C, with a sharp rise in cross section taking place at 120°C. The data were obtained with krypton incident at 60°C [effective LET of 82 MeV/(mg/cm^2)]. No upsets in either of the two 400 kΩ devices were observed with krypton incident normally [LET of 41 MeV(mg/cm^2)], at temperatures up to and including 120°C.

The experimental devices with the 130 kΩ cross-coupled resistors are more susceptible to SEU, as shown in Fig. 11. Here we can observe the following features: the apparent saturation of the cross section at values close to 2 x 10(-3) cm^2 for high temperature and LET values, as well as the exponential dependence of the cross section on temperature below the saturation regions.

N-channel metal oxide semiconductor (NMOS) RAM cells (see Fig. 3a) will also be susceptible to high temperatures, since the load resistance decreases with increasing temperature (and hence a lower noise immunity results). We chose IDT6116 (2k x 8) NMOS RAM for this test. Figure 12 shows the results obtained with argon and nitrogen. These results are shown here as an example of the dependence of the SEU susceptibility on the temperature. The threshold of the cross section at the lower end of LET increases with the temperature.

An example of the effect of elevated temperatures on latch-up is shown in Fig. 13 for the HM6504 (4k x 1) RAM (SN 11). Latch-up in this device occurred at room temperature, and the saturation cross section increased with increasing temperature. The threshold, on the other hand, decreased as the temperature increased.

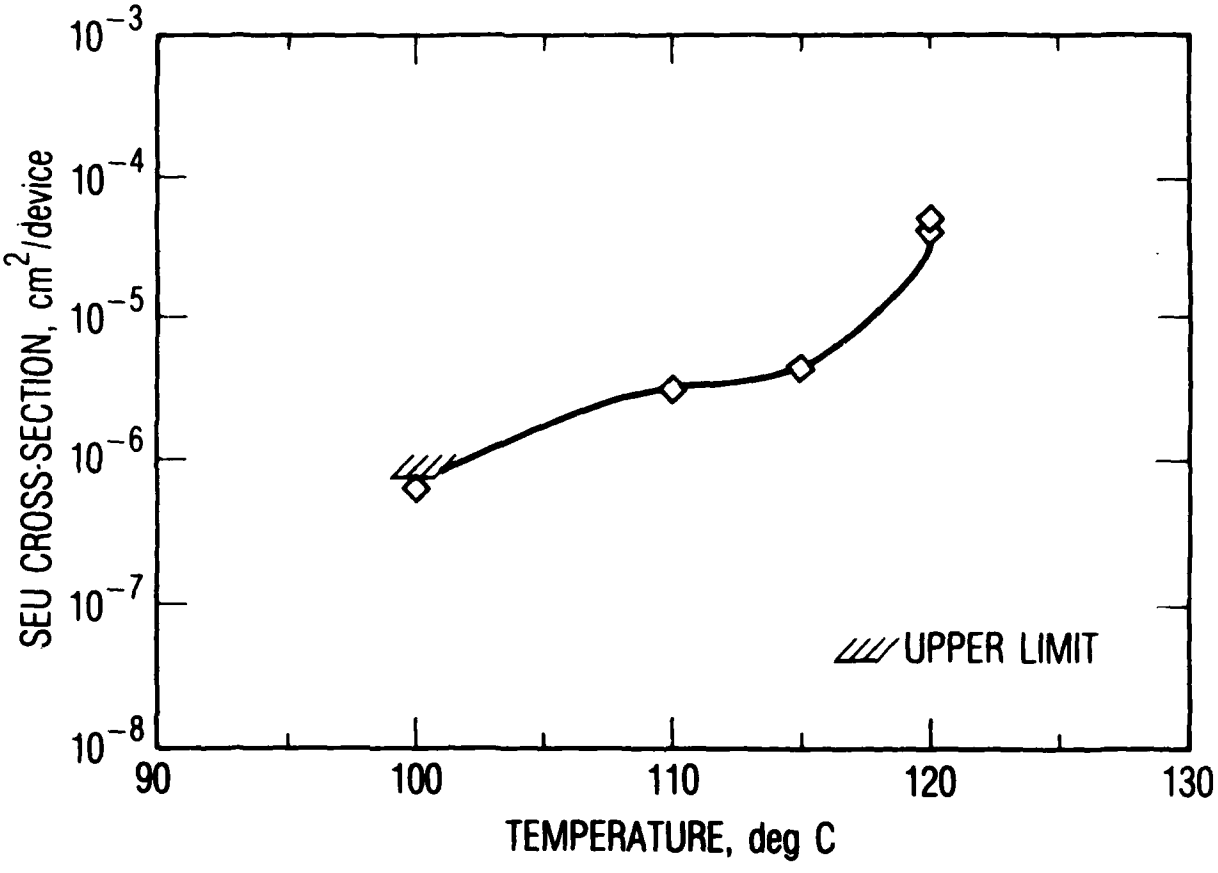

Fig. 10. SEU Results for the SNL SA3240 RAM (400 kΩ Resistors) at LET = 82 MeV/(mg/cm^2): Cross Section vs Temperature

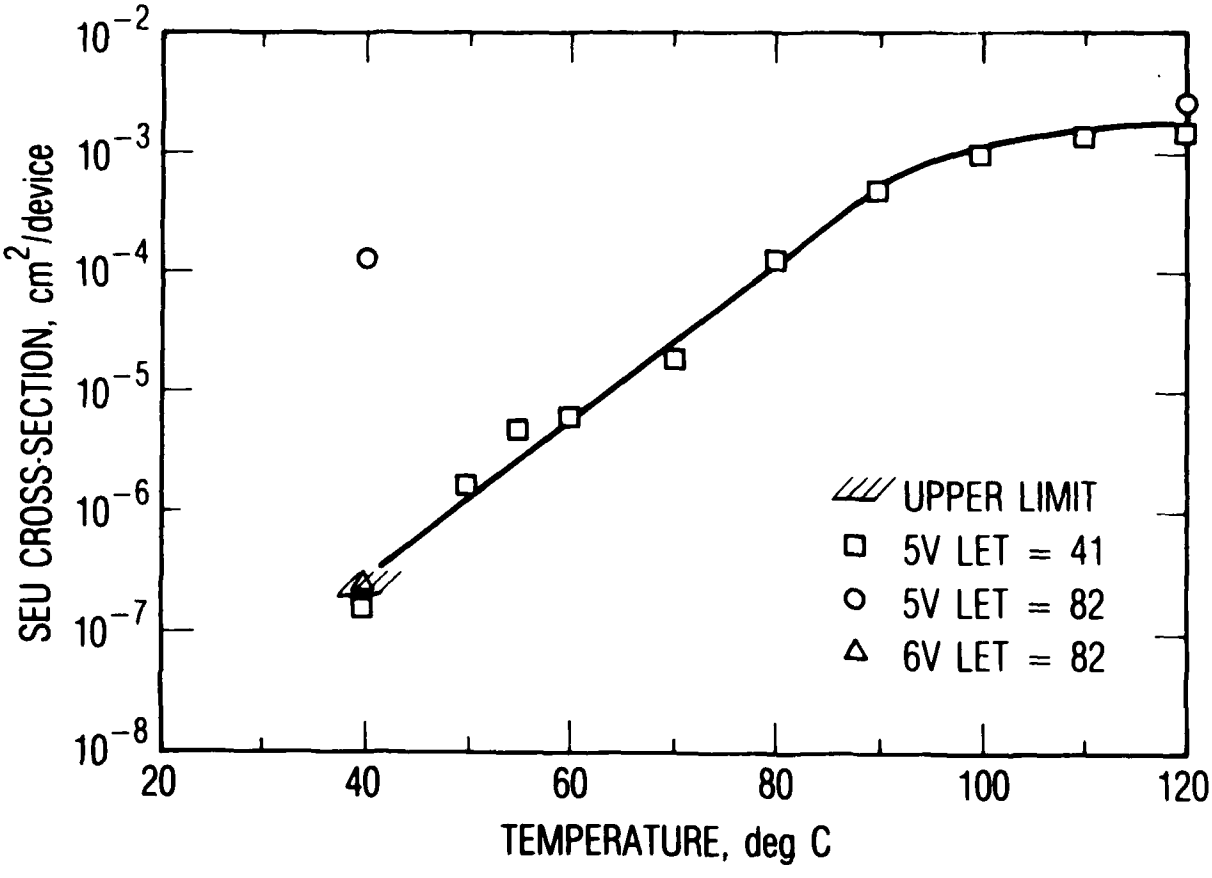

Fig. 11. SEU Results for the Experimental SNL SA3240 RAM (130 kΩ Resistors): Cross Section as a Function of Temperature, LET, and Bias

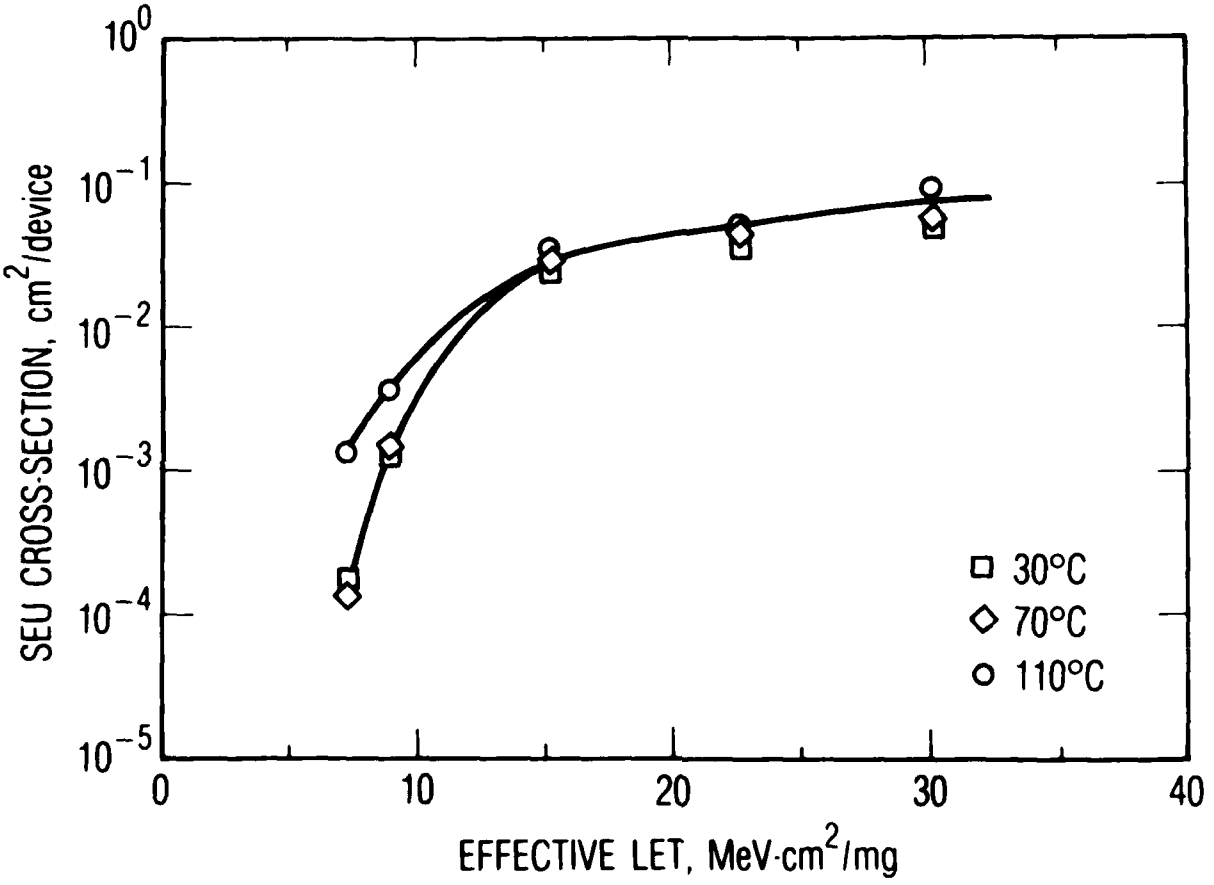

Fig. 12. SEU Results for the IDT6116 NMOS RAM: Argon and Nitrogen Data

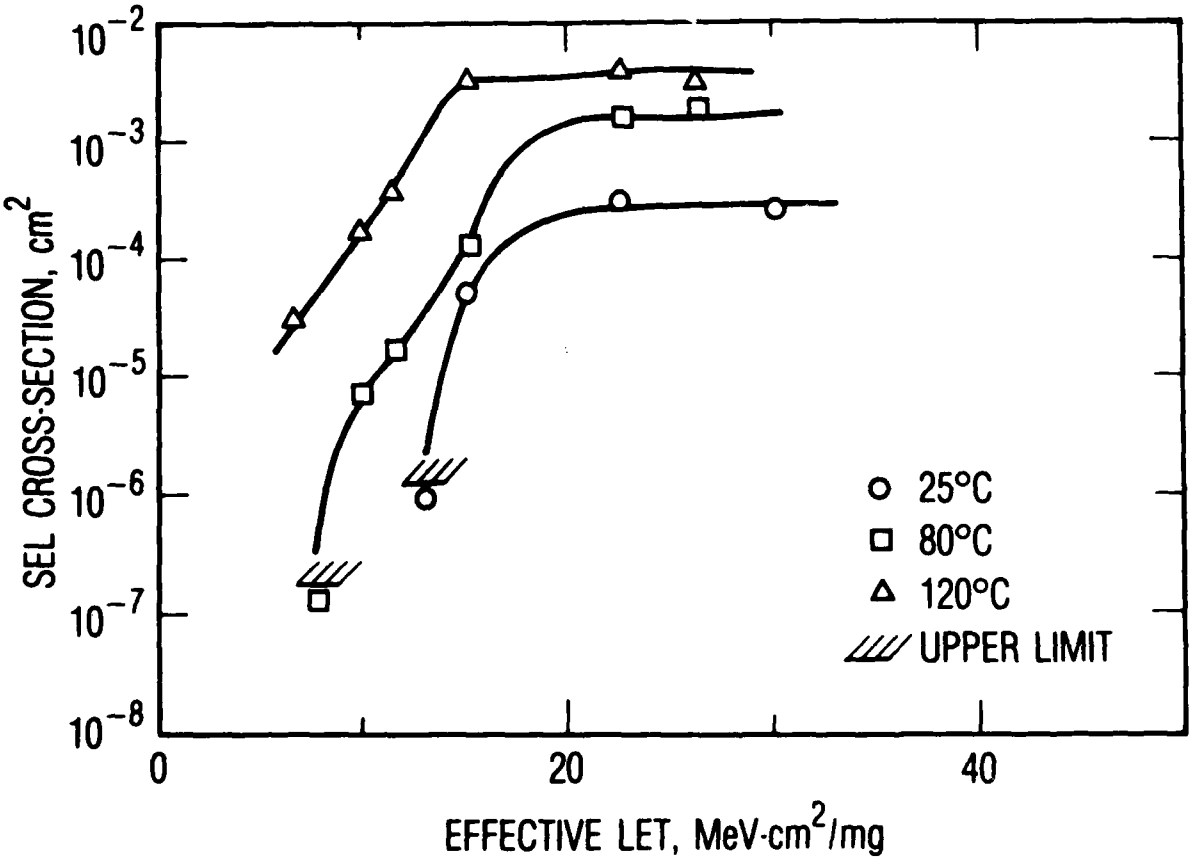

Fig. 13. Latch-Up Results for the HM6504 4k x 1 CMOS RAM

III. DISCUSSION AND CONCLUSIONS

In our study of the complex problem of upset mechanisms and their effect on the frequency of upset in space, we have focused our attention on two quantities: the LET of the particles causing SEU (and latch-up) and the upset cross section, which is a function of LET (see Figs. 2, 5, 9, 12, and 13). The dependence of the cross section on LET in large measure determines the device response to the particle environment in space.

The existence of the SED phenomenon, predicted in Ref. 3, might be deduced from the IDT6116 RAM data in Fig. 5, where, between a LET of 6 and 15 MeV-cm^2/mg, the cross section obtained with the dynamic measurement is considerably higher than the static and "semi-dynamic" measurements indicate. Our inability to detect cell recovery from a "disturbed" condition during the dynamic tests could be due to the fact that the act of interrogation forces the cell into a stable, altered state, i.e., an SEU. Strictly speaking, this is not an SED, since the theory predicts that a disturbed RAM cell ultimately returns to its original state. In what follows, we will designate this modified form of SED (if it really exists) as a modified single event disturbance (MSED). The existence of MSED at LET values significantly higher than threshold can be attributed to particles cutting corners in the sensitive region and to statistical fluctuations in the charge deposited there. At the lower values of LET, even the maximum possible charge deposited on a cell will neither upset (SEU) the cell nor make it unstable (MSED). Thus the dynamic and static results converge. The MSED could be one of the factors that tend to smooth the "knee" section of a cross section vs LET curve.

Another interpretation of the results, just as plausible as MSED, is that fast, repetitive reading of the cell tends to disturb it and thus lowers its immunity to transient signal response. Effectively, this would result in a reduced threshold LET for SEU and in an increase of observed upset cross section near threshold. However, for LET values well above the

"knee" in the cross section vs LET curve, no differences in measured cross-section values obtained with the various programs would be expected if the noise immunity interpretation is correct.

From the practical viewpoint of predicting upset rate in space, all of the preceding fine distinctions in upset mechanisms are strictly academic, and the data of Fig. 5 can safely be used to derive the device upset rate at room temperature. However, circuit simulations to validate or disprove the preceding hypotheses ought to increase our understanding of the device behavior in the radiation environment.

In the case of the IDT71681 (4k x 4) RAM, the observed SED-like pulses (see Fig. 7d) are far too short to affect the upset rate at normal frequencies of RAM interrogation. Hence the data in Fig. 2 adequately characterize the device. However, the presence of the pulses should be taken as a silent warning that such a thing as SED may be occurring and may, in some other devices, bring disturbing consequences.

We now turn our attention to the effect of upset in combinatorial logic devices. To the best of our knowledge, the ALU of the M6800 microprocessor does not hold memory elements. Hence, the order-of-magnitude increase in upset rate when the ALU is included in the loop testing the A and B accumulators can be interpreted as being due to upsets in the ALU combinatorial logic. The mechanism is certainly a plausible one.

At this point, we cannot proceed beyond the hypothesis stage, since we do not have a really good theory to predict such an error rate without detailed circuit information from the manufacturer--information which at best is hard to come by. Fortunately, one only has to be aware of the possibility of combinatorial logic upset and test for its possible effect at an accelerator site, without having complete knowledge of the device circuit. In other cases we have investigated, the combinatorial logic

upset was not a problem at all (e.g., the ALU of the AM2901 bit slice processor). Since the theory is in its infancy, we need to resort to experiment.

The tests at elevated temperature revealed some obvious and other not-so-obvious results. No great surprises are seen in the SNL RAM data. Because of the negative temperature coefficient of the cross-coupling resistors, the critical charge for upset decreases with increasing temperature, resulting in a drastic increase in SEU cross section. We hope that the results will prove valuable in validating models used for hardening the devices and in the improvement of future designs.

The nature of the dependence of the SEU threshold on temperature needs further study using several device types. NMOS memory cells with resistive loads (e.g., IDT6116) are susceptible to temperature change. The data shown in Fig. 12 are partial results of our work currently in progress.

The HM6504 data suggest that once latch-up begins to occur along a particular path, the cross section rises drastically with temperature, while there is relatively little further change in threshold LET.

While the SEU (and latch-up) susceptibility data, like the data of Figs. 2, 5, 9, 12, and 13, are necessary to predict the upset rate in space, two additional pieces of information are needed: the particle environment in orbit and the mechanical shielding on the spacecraft. Schemes such as the one put forward by Adams and his colleagues (Ref. 1) describe the latter two ingredients for a wide range of conditions. Our concern is that the first ingredient be just as accurate and up-to-date as the others. In that context, we believe, on the basis of our present studies, that SED phenomena are not a major portion of the upset mechanism. Even though we tested only two device types, they are quite typical of devices with RAM cells containing high resistive loads. The duration of SED upsets appears to be much shorter than predicted and the occurrence less frequent. On the other hand, upsets arising from combinatorial errors are surprisingly significant in the ALU of M6800

microprocessor. Data from other microprocessors that we have tested did not show such a high susceptibility of the ALU. We certainly need to pay attention to this problem while testing other device types.

The high temperature environment must be taken into consideration for assessing the sensitivity of microcircuits to cosmic rays in general. In particular, devices with resistors in circuit elements known to be critical need to be tested over the full operating temperature range.

REFERENCES

1. J. H. Adams, Jr., R. Silberberg, and C. H. Tsao, "Cosmic Ray Effects on Microelectronics," IEEE Trans. Nucl. Sci. NS-29, 169 (1982).

2. R. Koga, W. A. Kolasinski, and S. Imamoto, "Heavy Ion Induced Upsets in Semiconductor Devices," IEEE Trans. Nucl. Sci. NS-32, 159 (1985).

3. S. E. Diehl-Nagle, "A New Class of Single-Event Soft Errors," IEEE Trans. Nucl. Sci. NS-31, 1145 (1984).

4. S.E. Diehl-Nagle, J. E. Vinson, and E. L. Peterson, "Single Event Upset Rate Prediction for Complex Logic Systems," IEEE Trans. Nucl. Sci. NS-31, 1132 (1984).

5. J. L. Andrews, J. E. Schroeder, B. L. Gingerich, W. A. Kolasinski, R. Koga, and S. E. Diehl, "Single Event Error Immune CMOS RAM," IEEE Trans. Nucl. Sci. NS-29, 2040 (1982).