APPENDIX B
DOD No. 88.1

U.S. DEPARTMENT OF DEFENSE

SMALL BUSINESS INNOVATION RESEARCH (SBIR) PROGRAM
PHASE 1—FY 1988
PROJECT SUMMARY

Topic No. 87-14 Military Department/Agency SDIO

Name and Address of Proposing Small Business Firm

AstroPower Division/Astrosystems, Inc.
30 Lovett Avenue
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Name and Title of Principal Investigator

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Proposal Title Electronic GaAs-on-Silicon Material for Advanced High-Speed Optoelectronic Devices

Technical Abstract (Limit your abstract to 200 words with no classified or proprietary information/data.)

AstroPower has successfully demonstrated the growth of device quality GaAs on silicon, using its novel selective liquid phase epitaxial growth technology, during this Phase I research program. Selective growth and graded interlayers were used to reduce lattice strain and minimize lateral dislocation propagation, resulting in a stoichiometric GaAs composition. Device quality layers of lightly n-doped GaAs were grown and junctions were fabricated. Layer quality and uniformity were demonstrated by fabrication of working LEDs. The feasibility study and preliminary equipment design for three inch diameter GaAs on silicon selective liquid phase epitaxy, SLPE, was prepared.

Anticipated Benefits/Potential Commercial Applications of the Research or Development

Fabrication of MMICs onto heteroepitaxial GaAs on silicon will offer increased potential for weight reduction and lower costs, in addition to the benefits of greater speed and relative radiation immunity of MMIC fabrication on homoepitaxial GaAs. Device quality GaAs on silicon substrates will provide the benefits of GaAs on a robust substrate. Growth of device quality, large area, GaAs epitaxial layers on silicon substrates will lead to the development of a new generation of microelectronic and optoelectronic integrated circuits.

List a maximum of 8 Key Words that describe the Project.

GaAs-on-Silicon, Heteroepilayers, MMIC, SLPE, semi-insulating

Nothing on this page is classified or proprietary information/data.

4. Introduction

The development of device quality GaAs on silicon is recognized as one of the most desirable new technologies [1]. In this Phase I research program, AstroPower has shown that large areas of device quality GaAs on silicon can be grown using its novel technique, SLPE, selective liquid phase epitaxy. Important program demonstrations are listed below.

- Growth of gallium arsenide on silicon substrates with areas greater than one cm^2 using the novel AstroPower selective liquid phase epitaxy technique.
- Growth of device quality GaAs on silicon using the selective liquid phase epitaxial growth technology.
- Fabrication of an LED on a selective GaAs/Si heterostructure grown by liquid phase epitaxy.

Device quality, heteroepitaxial GaAs on silicon has numerous applications in advanced optoelectronic and high speed devices as well as being a source of low-cost, large-diameter GaAs layers. The technology is key to monolithic high speed integrated circuits and also to optical communication techniques with the next generation of VLSI, since optical interconnects have significant advantages over metallic interconnects in both speed and chip dimensions [2,3].

MESFET's, heterojunction bipolar transistors, double heterostructure injection lasers, avalanche photodiodes, and similar structures using MOCVD or MBE GaAs on Si substrates have been fabricated at several large research centers [4]. In addition, a GaAs enhancement/depletion MESFET 1-kbit SRAM has been fabricated on a 2 inch Si substrate [5]. However, materials development of device quality GaAs on Si with low dislocation densities remains a priority. GaAs with high dislocation densities will not support efficient, stable, minority carrier devices. Dislocation densities remain at 10^8 to $10^9/cm^2$ [6], with the best reported at 10^6 to $10^8/cm^2$ [7].

The use of heteroepitaxial GaAs on silicon is a desirable approach for advanced microwave and millimeter wave devices. The use of GaAs permits operation in the microwave and millimeter (30-300 GHz) bands. Device quality GaAs on silicon substrates will provide the benefits of GaAs on a substrate that has a higher level of power dissipation, is less expensive, and is available in sizes up to eight-inch diameter. Progress on the development of this technology has been affected by strains and dislocations introduced into the GaAs layer by the lattice mismatch and thermal expansion coefficient mismatch between the two materials. Working LED's, minority carrier devices requiring low dislocation densities, were demonstrated during Phase I. The

use of AstroPower's selective liquid phase epitaxy technique virtually eliminates the deleterious effect of the lattice mismatch and thermal expansion mismatch by minimizing the contact area between the GaAs and the silicon.

Growth of device quality, large area, GaAs epitaxial layers on silicon substrates will lead to the development of a new generation of microelectronic and optoelectronic integrated circuits. AstroPower proposes the continued development of its GaAs heteroepitaxial layers on 3 inch diameter silicon substrates, to be grown utilizing SLPE, during Phase II. High quality heterolayers can be used for fabrication of monolithic microwave integrated circuits, MMIC, and of monolithic microelectronic and optoelectronic circuits. The selective liquid phase epitaxial GaAs grown by AstroPower has the advantages of:

- Growth of thick, electrically isolated layers, with the benefit of reduced dislocations as a result of SLPE.
- Single crystal growth over the entire masked region, since nucleation occurs only in the vias and lateral overgrowth occurs from the via front.
- Use of an easily scalable process, which can handle wafers up to 8 inch diameter by simple scale-up of present equipment.

These desirable advantages have not been demonstrated by vapor phase epitaxial growth. Continuation of this research will create a new material system for microelectronic and optoelectronic applications. Production of GaAs/Si 3 inch substrates is planned for Phase III.

This Phase I Final Report details the six-month research program "Electronic GaAs-on-silicon Material for Advanced High-Speed Optoelectronic Devices" and the significant results of this research as listed below.

4.1 Smooth, device quality GaAs layers, greater than 1 cm^2 in area, have been grown using selective liquid phase epitaxy.

4.2 Device quality, n-doped GaAs layers with a carrier concentration of 1-2 x 10^{17} were grown by impurity reduction and selective doping of the top GaAs layer.

4.3 GaAs layer quality and uniformity were demonstrated by LED fabrication.

4.4 The feasibility study and preliminary equipment design for SLPE growth of three inch diameter GaAs on silicon was prepared.

5. Research Objectives

The goal of this work was to develop the technology used to grow large area, device quality heteroepitaxial GaAs on silicon.

The procedure used, selective epitaxy, differs from conventional liquid phase epitaxial growth. In the selective epitaxy procedure, a masking layer is placed on the substrate material. The passivating masking oxide layer is a thermally grown, e-beam, or sputtered oxide layer. Small windows ("vias") are then opened in the masking layer using appropriate geometries and spacing to serve as nucleation sites. Several via geometries were successfully implemented. Figure 1 shows two of the via geometries that were used.

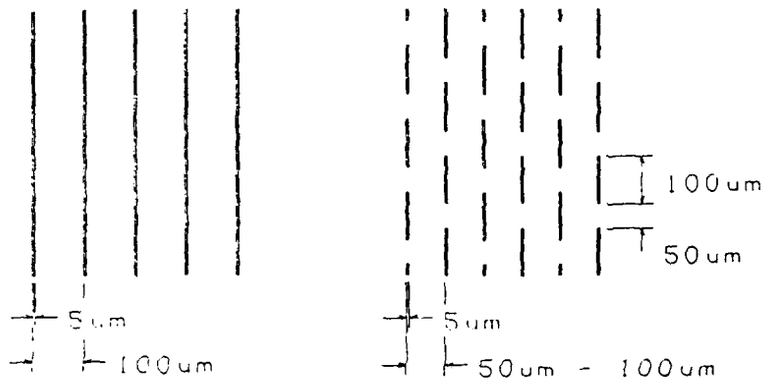


Figure 1. Nucleation Via Geometries.

Epitaxial growth of the appropriate layer or interlayer occurs through the vias in the masking layer. Advantages of the via approach are that stresses caused by lattice mismatch and differential thermal expansion are effectively limited to the via area, which is less than 5% of the total wafer area.

The specific objectives for the Phase I research were:

5.1 Prepare smooth, low-defect GaAs layers 1 cm^2 in area by the double selective liquid phase epitaxial growth technique.

5.2 Develop semi-insulating GaAs layers by impurity reduction and selective doping of the top GaAs layer.

5.3 Demonstrate GaAs layer quality and uniformity by fabrication of simple devices: majority carrier devices (FET's) and minority carrier devices (LED's).

5.4 Prepare feasibility study and preliminary equipment design for square geometry (four-inch by four-inch) GaAs-on-silicon double selective epitaxial wafer growth.

6. Research work

The Phase I research effort has been an experimental program to develop procedures using selective liquid phase epitaxy which implemented the research objectives. In the process of developing crystalline thin-film solar cells, AstroPower has gained considerable skill and experience into the growth phenomena with thin GaAs films from small aperture nucleation sites [8,9]. SLPE growth is divided into sequential elements that have been described in earlier AstroPower research, 1) wetting, 2) nucleation, and 3) non-impinging crystal growth [10].

The structure which resulted in large area, GaAs on silicon is shown in Figure 2. First, GaP was selectively nucleated in

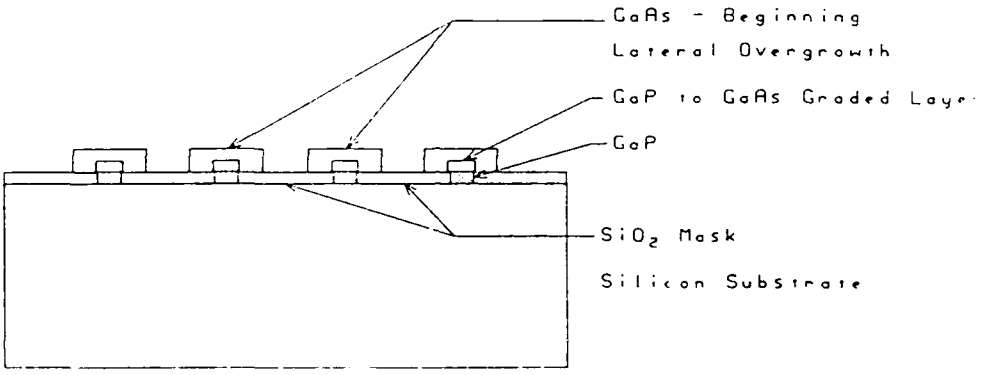


Figure 2. Diagram of SLPE Growth of GaAs on GaP/Si.

the vias. The GaP growth was followed by a transition layer which graded the composition from GaP to GaAsP to GaAs. The average transition depths were 2.5 microns. GaAs overgrowth yielded complete device quality GaAs films on silicon. The technical approach used in this program achieved the objectives by implementing these tasks:

6.1 Selective Wetting and Nucleation of GaAs on masked Si substrates with a GaP interlayer.

6.2 Overgrowth of GaAs on GaAs/GaP/Si.

6.3 Characterization of GaAs grown during tasks 6.1 and 6.2.

6.4 Fabrication and testing of an LED on the GaAs/GaP/Si.

6.5 Preparation of a feasibility study and preliminary equipment design for 3 inch diameter GaAs/Si wafers using selective liquid phase epitaxy.

Epitaxial layers were grown in this research using a multiple-bin liquid phase epitaxial slider boat growth apparatus similar to that used by Nelson [11]. Advantages of the slider apparatus over other techniques, such as dipping, are: 1) the substrate wafer can easily be brought in and out of contact with the melts, 2) several melts can be used in sequence, 3) growth is restricted to one side of the wafer, 4) substrate-solution contact is from the bottom of the melt where there are no floating oxides or other contaminants, 5) excess solution can be wiped off the wafer by the slider action of the boat, and 6) thermal equilibration and temperature profiling are greatly facilitated. The graphite slider apparatus fits into a quartz tube heated by a three or four zone furnace. The furnace zones are controlled to within +/- 1°C. The furnace atmosphere is a flowing high purity palladium diffused hydrogen.

The fabrication of the GaAs/Si heterostructure by solution growth presented two main problems. First, the 4% lattice mismatch between GaAs and Si can hinder or prohibit growth. The second problem, which is unique to solution growth, concerns the relative solubilities of the compound being grown and the substrate material. Ideally the growth material will have a high solubility in the solvent selected while the substrate material's solubility will be negligible.

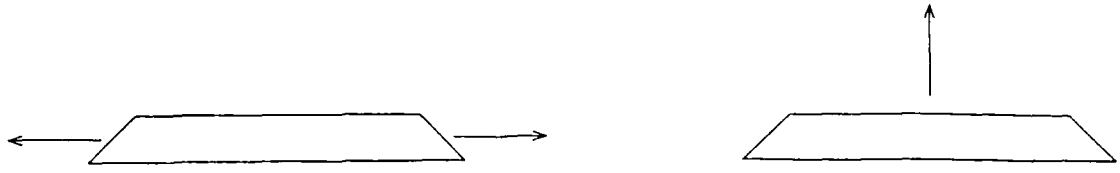
Evaluation of the grown layers and overgrowth structures was by optical and scanning electron microscopy. Chemical etching and optical microscopy were useful for both the edges of cleaved wafers and top surface analysis. Etchants for silicon, gallium phosphide, and gallium arsenide are readily available for this procedure.

6.1 Selective Wetting and Nucleation of GaAs on masked Si substrates with a GaP interlayer.

Large area overgrowth of GaAs on any substrate depends on consistent nucleation of GaAs on the substrate. GaAs was selectively nucleated and overgrown on selectively masked silicon using the stripe mask and a GaP interlayer. The nucleation melt was the Sn-Bi melt used in conjunction with growth parameters which minimized meltback of the substrate and maximized the amount of GaAs held in the melt available for nucleation. Step cooling or supersaturation were used as the nucleation driving force. Uniform wetting of the vias yielded uniform, high percentage nucleation. Nucleation in vias of different geometries is a consistent reproducible process at AstroPower.

Selective stripe epitaxy, SSE, is a growth technique developed at AstroPower which uses heteroepitaxial growth through stripes in a masked silica layer, examples were shown in Figure 1. Photolithography was used to define the vias through an oxide. This oxide can be a thermal or an e-beam oxide. The

dominant growth mechanism on substrates with (111) orientation is in the lateral direction, as shown in Figure 3a and in the vertical direction on substrates with (100) orientation, shown in Figure 3b. Therefore (111) silicon substrates were used.



3a (111) 3b (100)

Figure 3. Dominant crystal growth directions.

Figure 4 shows a cleaved edge selective liquid phase epitaxy crystal on (111) Si. This shows the dominant growth direction and also shows that by using appropriate growth techniques, melt entrapment will not occur as adjacent crystals grow together, and AstroPower's experience is that trapped melt does not exist.

Figure 4. SSE Crystal.

6.2 Overgrowth of GaAs on GaAs/GaP/Si.

The growth structure illustrated in Figure 2 demonstrates an important attribute of selective epitaxial growth. Device quality GaAs is obtained by lateral overgrowth over the SiO_2 mask. Defects occurring at the initial growth interface in the vias will not propagate laterally into the overgrowth region. This occurs because defects do not bend over, but propagate only in one direction, in this case vertically.

Fan [12] has shown in numerous publications that the boundary of adjacent coherent overgrowth results in a continuous layer with no barrier properties. Our previous experience [13,14]

indicates that high aspect ratios are achievable, offering consistent, reproducible results. Higher aspect ratios allow for greater via spacing. Selective LPE growth has achieved good results on (100) and best results on (111) substrates with lamellar overgrowth up to 70 microns over silica masked substrates [15].

This task used (111) Si substrates and developed the lateral overgrowth technique during Phase I. Growth aspects were controlled by the nucleation site density and the solute mass flux across the convection free boundary layer at the interface. Various ramp cooling rates were used, which optimized local growth vectors and surface morphology. Ramp cooling rates at the melt well in the graphite boat were controlled from 0.1 to 1.5 ^{o}C/min. Multistage rates were used to optimize the transition from vertical to lateral growth.

GaAs layers grown by SSE have reduced thermal mismatch, fewer lattice mismatch dislocations, and limited Si interface sheet charge since the reduced nucleation area limits interface area. Furthermore, offset SSE eliminates lateral tension accumulation and between-stripe cracking. Homoepitaxial overgrowth of GaAs improves the GaAs/Si heteroepitaxial layer. The overgrowth layer is of very high structural quality. This is consistent with Fan's experience where efficient GaAs homoepitaxial solar cells have been fabricated from predominately overgrowth structures [16].

6.3 Characterization of heteroepitaxial GaAs

Implementation of this task was concurrent with the previous tasks. GaAs nucleated crystals and overgrowths obtained during tasks 6.1 and 6.2 were analyzed to determine morphology, gross impurities, and dislocations and to assure stoichiometric GaAs composition. AstroPower has SEM, EDAX, and photoluminescence equipment which was used for analysis of both top and cleaved edge surfaces of the GaAs crystals. This analysis of material grown permitted modification of growth parameters during development processes for the first two tasks.

6.4 Fabrication and testing of an LED on the GaAs/GaP/Si.

The procedure for fabricating light-emitting diodes used conventional planar GaAs LED processing technology. The moderately doped GaAs overgrowth layer was n-type and served as the base of the LED. Junctions were formed by zinc diffusion or by LPE growth of a heavily doped p-type emitter. The substrate was electrically connected to the heteroepitaxial layer using a degenerately doped nucleation layer. Standard metal contacts were used for back contacts. The top contact was a very thin layer of a gold-zinc alloy. This thin layer allowed the generated light to pass through it.

6.5 Preparation of a feasibility study and preliminary equipment design for 3 inch diameter GaAs/Si wafers using SLPE

Phase I of this program was concluded with a detailed examination of the process and equipment required for production of 3 inch diameter GaAs on silicon wafers. This study integrated the technology developed during the first four tasks of this Phase I research conducted using seed wafers. This production and equipment design drew from AstroPower's experience operating a pilot line production facility and also a semi-continuous liquid phase silicon-film growth apparatus capable of 500 cm^2 per growth run which is comparable to ten 3 inch wafers per three hour growth run.

7. Research Results

The Phase I research results discussed in this section are both experimental and theoretical activities. These research results demonstrate the local growth of GaAs by means of selective liquid phase epitaxy on silicon substrates. These results and findings provide a strong basis for the Phase II program and further development of this concept.

7.1 Selective Wetting and Nucleation of GaAs on masked Si substrates with a GaP interlayer.

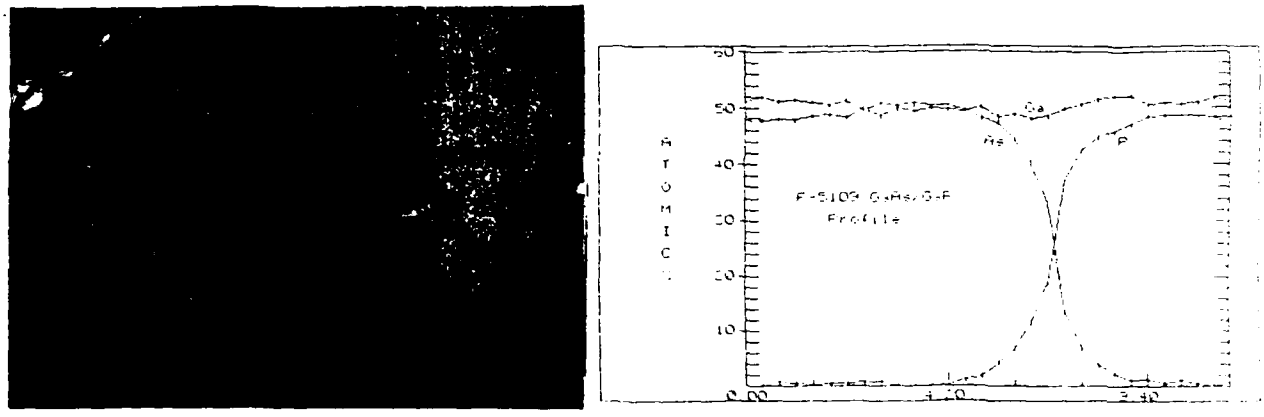
7.1.1 GaP Interlayer on Silicon

The experimental work with the GaAs/GaP/Si approach began with planar GaP on Si growth, followed by selective GaP on Si growth. Figure 5 shows heteroepitaxial GaP in vias grown on <111> silicon substrates using tin as the solvent. This approach has shown itself to be effective with proper growth parameter modifications. EDAX analysis shows the GaP to be stoichiometric without silicon contamination.

Figure 5. GaP Nuclei in Vias Directly on Silicon <111> Substrates.

7.1.2 GaAs on GaP

The GaAs/GaP/Si approach continued by refining AstroPower GaAs on GaP growth techniques. The process utilized planar growth to refine the morphology and the transition layer thickness. Figure 6a shows the featureless surface of planar GaAs grown on <111> GaP substrates using a tin-bismuth composition as the solvent. The EDAX edge scan analysis of Figure 6b shows the GaP to GaAs transition to be stoichiometric and to occur over approximately 2.5 microns.

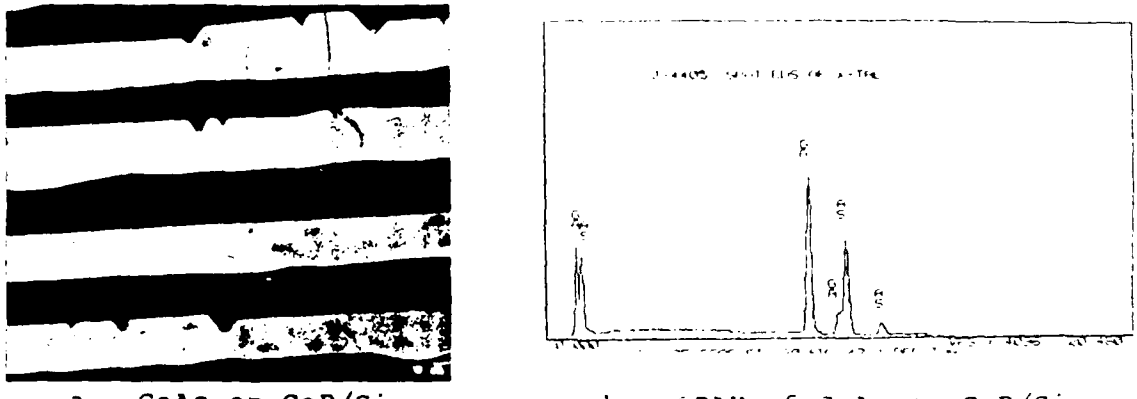


a. GaAs on GaP b. EDAX of GaAs/GaP

Figure 6. Planar GaAs on <111> GaP.

7.1.3 GaAs on GaP/Silicon

This set of experiments integrated the results of the preceding two sets of work. A procedure was designed to incorporate the transition growth of GaAs on GaP with the growth of GaP on Si. Stoichiometric selective growth of GaAs on GaP/Si was achieved. Figure 7a shows the surface morphology and the beginning of lateral overgrowth. Figure 7b is an EDAX evaluation of the grown GaAs layer and shows stoichiometric GaAs.



a. GaAs on GaP/Si b. EDAX of GaAs on GaP/Si

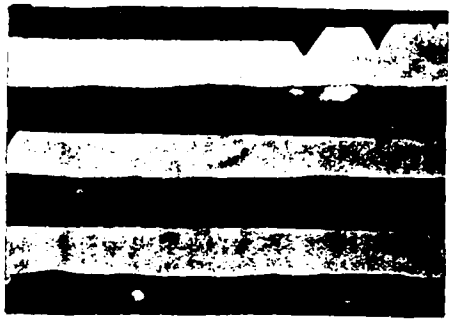
Figure 7. Selective GaAs on GaP/Si.

7.2 Overgrowth of GaAs on GaAs/GaP/Si.

This work extended the three sets of experiments performed in attaining GaAs on GaP/Si. One cm^2 areas of selective GaAs on GaP/Si heteroepitaxial layers were grown. Figure 8 shows the steps followed in achieving selective growth of GaAs on GaP/Si. Selectively nucleated GaP on silicon is shown in 8a. The

selective quick-grade layer shown in 8b grades from GaP to GaAs on GaP/Si. The featureless growth of 8c is lateral overgrowth of selective GaAs/GaP/Si.

8a. Selective GaP/Si



8b. Selective GaAs/GaP/Si

8c. Lateral Overgrowth: GaAs on GaAs/GaP/Si

Figure 8. SLPE Growth of GaAs on GaP/Si.

This surface quality is good, but can be improved by: a) a more gentle grade from GaP to GaAs and b) careful manipulation of the growth parameters. The growth rates were high (1°C/min.) and the transition layer driving force was high. Careful refining of these procedures will improve the process during Phase II.

7.3 Characterization of GaAs grown during tasks 7.1 and 7.2.

Implementation of this task was concurrent with the previous tasks. GaAs nucleated crystals and overgrowths obtained during tasks 7.1 and 7.2 were analyzed to determine morphology, gross impurities, and dislocations and to assure stoichiometric GaAs composition. AstroPower has SEM, EDAX, and photoluminescence equipment which was used for analysis of both top and cleaved edge surfaces of the GaAs crystals. This analysis of material

grown permitted modification of growth parameters during development processes for the first two tasks.

7.4 Fabrication and demonstration of an LED on the GaAs/GaP/Si.

During Phase I, one cm^2 area selective GaAs on silicon heteroepitaxial layers were grown and monolithic gallium arsenide-on-silicon light emitting diodes were demonstrated. LEDs fabricated from these growths are shown in Figure 9.

a. Off b. On

Figure 9. GaAs/Si LED.

The procedure for fabricating light-emitting diodes used conventional planar GaAs LED processing technology. The moderately doped GaAs overgrowth layer was n-type and served as the base of the LED. Junctions were formed by zinc diffusion or by LPE growth of a heavily doped p-type emitter. The substrate was electrically connected to the heteroepitaxial layer using a degenerately doped nucleation layer. Standard metal contacts were used for back contacts. The top contact was a very thin layer of a gold-zinc alloy. This thin layer allowed the generated light to pass through it.

7.5 Feasibility study and preliminary equipment design for 3 inch diameter GaAs/Si wafers using SLPE.

7.5.1 Single wafer, multi-melt horizonal slider.

A single wafer, multi-melt horizonal SLPE slider unit for three-inch diameter wafers is the first step in the scaling of the SLPE technology. The technical issues in the design of this unit are minimal. Scaling to three-inch wafers entails increasing boat and slider lengths and boat width:

Boat length (inches): $3.3(n + 1)$
where n = number of wells required

Slider length (inches): (2 x Boat length) + 1

For a 5-well boat, for example, the boat length is 19.8 inches and the slider is 40.6 inches. The minimum quartz tube diameter is 3.88 inches, based on scaling of horizonal dimensions only. The determination of the minimum number of required boat wells is clearly a key decision in the single-wafer scaling process.

The single wafer multi-melt SLPE system appears to have minimal technical problems in design and implementation and is highly feasible for the preparation of three-inch GaAs on silicon material at the prototype level.

7.5.2 Multiwafer, multi-melt batch mode SLPE unit.

Multiwafer LPE processes for high volume production of light-emitting diodes have been used at various companies for the past fifteen years. The equipment used at Bell Laboratory and AT&T are described by Saul and Lorimor [17]. The silicon amphoteric-doping of GaAs and AlGaAs, in particular, lends itself to single melt, multiwafer production LPE growth of both IR and visible LED's [18]. LPE systems which handle 50 wafers per run are being used in production [19]. In addition to the slider LPE technology, multiwafer dipping using the "infinite melt" procedure has been developed by Kamath and coworkers [20] at Hughes. However, these techniques are not suited to multiple melt processes.

In searching for past history of multiwafer, multimelt LPE processes, few references are available, and refer to laboratory scale processes. In particular, Heinen [21] reports on the design and successful operation of a 16 wafer, 4-melt LPE slider growth system for use with AlGaAs Burrus LED's and InGaAsP on InP. With this system, the InGaAsP quaternary is limited to single phase equilibrium growth. Dutt [22,23,24] has revised Heinen's design to incorporate two-phase melts, necessary for successful InGaAsP quaternary work, but not necessary for GaAs on silicon material growth.

Centrifugal LPE described by Bauser [25,26] can be used for multi-wafer, multimelt growth. However, its application has been restricted to small geometry wafers and to specialized growth of superlattice structures involving the multiple use of two or more melts. In addition, the multi-layer process is restricted due to the cyclic nature of the design. In principal there is no reason, except cost, preventing larger geometries from being used in the centrifugal LPE apparatus.

Having considered these possibilities, the present recommendation is to avoid the multiwafer, multimelt LPE design for production. The complexity and the jamming tendency of the multiwafer, multimelt boat design outweigh the potential benefits this system might offer. The continuous (or semi-continuous) process should be next in the production level developmental sequence.

7.5.3 Continuous-mode SLPE unit.

Continuous LPE growth apparatus have been constructed in at least three major programs:

- Under contract with DOE Sandia National Laboratories, Varian developed a "transient-mode" LPE apparatus [27]. This unit has a single load-lock entry/exit for the single-wafer carrier. Each melt is pulse-heated from above with an individual source wafer (on top of the melt) to supersaturate each melt before the seed wafer is inserted prior to growth.

- Takahashi [28] has reported the concept for a large-scale continuous LPE furnace. This furnace used individual wafer carriers and had both entry and exit load-lock features. This unit also required a vertical temperature gradient. Only two melts were described, but additional melts could easily be incorporated.

- AstroPower has designed, constructed, and operated a continuous LPE process for growth of crystalline silicon on metallic ribbon material [29]. This apparatus is shown in Figure 10 (see pg. 15). The speed of the substrate through the growth apparatus has varied from 0.1 to 10 cm/min. The continuous process has led to an uniformity not seen on smaller laboratory scale growths. Uniform growths with areas over 500 cm^2 have been accomplished routinely.

Figure 10. AstroPower's Continuous LPE Apparatus.

The recommendation for the development of continuous mode LPE for GaAs on silicon is to take advantage of the AstroPower experience with the silicon-on-ribbon apparatus, described above, adjusting the design to a semi-continuous process. Provisions for individual wafer carriers and entrance/exit load-locking in a semi-continuous mode will need to be designed. This work should start early in the Phase II program. This approach has the long term advantage of eventually combining the GaAs on silicon and the silicon-on-ribbon technologies.

8. Conclusion

8.1 Selective liquid phase epitaxial techniques were successfully applied to the preparation of selective GaAs heteroepitaxial layers on silicon substrates.

8.2 Selective epitaxial growth of GaAs on Si was successfully accomplished by the use of a gallium phosphide interlayer resulting in GaAs on silicon. Appropriate solvent systems were used to minimize meltback and to enhance lateral growth free of dislocations.

8.3 LED's fabricated from the present planar structures demonstrate the potential for LPE growth of GaAs on silicon.

8.4 High quality GaAs/Si heterolayers can be used for fabrication of monolithic microwave integrated circuits, MMIC, and of monolithic microelectronic and optoelectronic circuits.

8.5 These GaAs on Si layers, grown by a commercially viable technique, will create a new material system for microelectronic and optoelectronic applications.

9. Recommendations

9.1 Continue the development of the technology to achieve large area, device quality GaAs on silicon during Phase II. Issues remaining are those of integrating the processes to further scale up growth area and determining the best pilot-scale production plan.

9.2 Optimization of nucleation and overgrowth techniques using selective liquid phase epitaxy to improve morphology and maintain device quality heteroepitaxial structures.

9.3 Demonstration of a simple, high performance, monolithically integrated optical source circuit demonstrating material quality.

9.4 Liquid-phase epitaxy continues to be the process by which the highest quality commercial heterostructure semiconductor devices are produced. For example, recent improvements in AlGaAs light-emitting diodes by heterostructure LPE growth methods in Japan have resulted in an order of magnitude improvement in brightness. Therefore, it is very important that the study of LPE heterogrowth be continued.

9.5 Non-equilibrium liquid-phase heteroepitaxial research is an area that is virtually untapped. Funding for this technology will give balance to programs that are supporting other non-equilibrium epitaxial growth techniques, MBE and MOCVD. This technology can be expected to lead to large, uniform, minimal-defect semiconductor wafers with a broad continuum of bandgaps.

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11. Key Personnel

Nancy E. Terranova was a major contributor to the GaAs on silicon development and in LED fabrication and testing. Ms. Terranova received her BEE from the University of Delaware. Her experience includes design and fabrication skills for heterojunction and homojunction III-V solar cells. Present work involves the design and implementation of experiments which will lead to large area, device quality GaAs on silicon, InP on silicon, and in the development of GaAs on silicon LED's for optoelectronic ICs. This work utilizes liquid phase epitaxial growth of the appropriate structure, followed by material analysis, and testing.

Gerald H. Negley was a major contributor to the GaAs on silicon theoretical development and in LED testing. Mr. Negley received his M.S in Physics from the University of Delaware. He is presently growing different III-V semiconductor materials by liquid phase epitaxial growth. He has successfully grown GaAsP layers on GaP, GaAsP solar cell structures, GaP on GaAs, germanium on silicon, silicon layers on GaP as well as the GaAs on silicon layers. Reliable ohmic contacts for a wide variety of III-V compounds have been developed under Mr. Negley's supervision.

Louis C. DiNetta was responsible for material characterization of the grown GaAs film by employing our SEM and EDS facility. Prior to joining AstroPower in December, 1985, Mr. DiNetta spent nine years at the Institute of Energy Conversion, University of Delaware, in the Device Development group. In that group he was responsible for the planning and organization of all device fabrication, as well as for any process and equipment developments and/or modifications necessary to support the many ongoing research projects.

James P. Curran, Technician, was responsible for the experimental selective liquid phase epitaxial growths, substrate and melt preparation. Mr. Curran has worked for 18 years previous to his employment at AstroPower as a technician at the Franklin Mint, Franklin Center, PA.

The principal investigator was James B. McNeely. He has run major GaAs manufacturing and GaAsP epitaxial layer manufacturing facilities for different companies. Mr. McNeely has a M.S. in Chemical Engineering. Mr. McNeely brings to the project his considerable knowledge and experience in materials development. He has been responsible for major III-V compound semiconductor bulk and epitaxial layer research and development facilities for Monsanto, Litronix, and M/A-COM Laser Diode Laboratories. His experience includes the organization, startup, and management of semiconductor materials operations. He was partially responsible

for Monsanto's position as the world's leading supplier of III-V compounds in the 1960's. Since joining AstroPower, Mr. McNeely has been involved with growing and characterizing epitaxial layers of GaAs, GaAsP, and GaP on a variety of substrates.

The General Manager of AstroPower Division is Dr. Allen M. Barnett. Dr. Barnett has a Ph.D. in Electrical Engineering from Carnegie Mellon Institute of Technology. He has successfully led three different organizations into positions of technical leadership in the development of high-technology products. These groups included a major industrial research and development laboratory, a start-up company and a university applied research institute. Dr. Barnett has planned and implemented all the steps necessary to take a new concept from the laboratory through product development and into the marketplace. Dr. Barnett is an experienced inventor and has been the recipient of four IR-100 awards for the development of industrial products and seven patents. A Professor of Electrical Engineering at the University of Delaware, he has established undergraduate and graduate level semiconductor device fabrication programs using both silicon and the III-V compounds. He is developing advanced semiconductor devices based on the heteroepitaxial growth of semiconductors on silicon, III-V, and non-crystalline substrates. These devices include thin-film polycrystalline silicon, thin-film gallium arsenide, and other III-V compound solar cells. He is also developing hybrid silicon/GaAs and silicon/germanium optically interconnected circuits.