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MICROPROCESSOR CONTROL OF A FAST ANALOG-TO-DIGITAL CONVERTER FOR AN UNDERWATER FIBER OPTIC DATA LINK

by

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Microprocessor Control of a Fast Analog-to-Digital Converter for an Underwater Fiber Optic Data Link

by

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ABSTRACT

This thesis reports on the design and evaluation of a microprocessor-controlled, high-speed analog-to-digital converter. The processor supervises and manages the digital conversion, split-phase encoding (Manchester) and framing of the input signal. This converter is designed to be applied in an underwater package which will serially transmit sensor data over a fiber optic link to a shore station. This intelligent sensor will provide for ease of future system enhancements. An example would be the implementation of one package to multiplex several analog channels from a local sensor network over the single fiber optic link to the shore station.

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I. INTRODUCTION AND BACKGROUND

A. THE DESIRED SYSTEM

The collection and understanding of underwater acoustics have played a primary role in man's exploration and study of the seas. Today, this collection and processing of underwater sound is the main detection and identification method of living and mechanical objects concealed beneath the water's surface. By using an array of transducers, position information is obtainable for a sound source of interest. Figure 1 depicts, in terms of a simple block diagram, one architecture for such a transducer array or network. This network would be deployed on the ocean floor and transmit data back to a shore station via a physical channel. Figure 1 shows this network consisting of multiple transducers all providing input signals to a single node. This node combines and encodes the multiple input signals into a single data signal. The data signal is then transmitted over a channel to shore where circuits receive, decode and sort out each of the original input signals. An initial hardware design for the block labeled, "Signal Multiplexing and Encoding Unit" in the network architecture depicted is the subject of this thesis. For simplification this unit shall be referred to as the "Prototype" throughout the remainder of

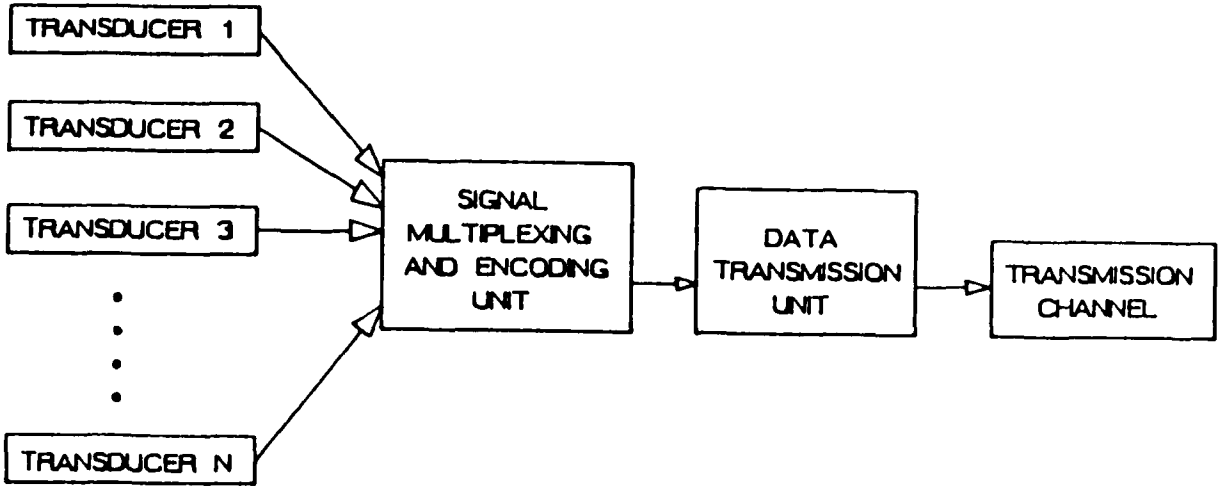

Figure 1. Block Diagram of the Desired System

this paper. This one word title was chosen as this is only intended to be an initial design attempt to study the feasibility of one selected architecture for this unit. The challenge in the Prototype design was to provide for switching between each transducer signal in the N-transducer network and encoding these signals at rates fast enough to provide for accurate signal reconstruction at the shore receiving station.

The Naval Postgraduate School has a project currently in progress to implement a transducer network as described above. This project has provided funding for this thesis and construction of the initial Prototype. Initial design specifications were also provided along with the desired functional capabilities of the network.

The approach taken in this design was to do the digital conversion of the analog signal from the transducer and then to encode the digital words for transmission. Providing for the expected high data rates of several megabits per second was the major problem in the design. This manifested itself in the selection of components with suitable throughput to avoid data flow bottlenecks and in the timing and control of individual components to insure synchronous flow of data with minimal delays.

B. CHARACTERISTICS OF OPERATIONAL ENVIRONMENT

The designed Prototype circuit must be able to operate independently at a remote site on the ocean floor for long periods of time with a high degree of reliability. This would indicate that the circuit should be low in power consumption and kept as simple in architecture as possible. Component expense was also a design consideration, given the low probability of recovery of a small system deployed on the ocean floor. The design was to be inexpensive enough to be considered expendable.

C. PROPOSED PROTOTYPE ARCHITECTURE

Figure 2 is the functional block diagram for the Prototype design. A total of N analog-to-digital converters, one for each transducer signal, are shown being multiplexed into one signal encoding and framing circuit. The signal is then passed from the Prototype to the transmitting circuit. A microprocessor provides the timing and control to insure coordinated asynchronous operation of the design. The discussion of timing in the next chapter presents the reasoning for multiplexing the N input channels between the analog-to-digital (A/D) conversion and encoding functions. Framing of the encoded signal, the last functional block in Figure 2, was a major concern. Framing was considered necessary to allow for possible idle time on the transmission channel between sample words.

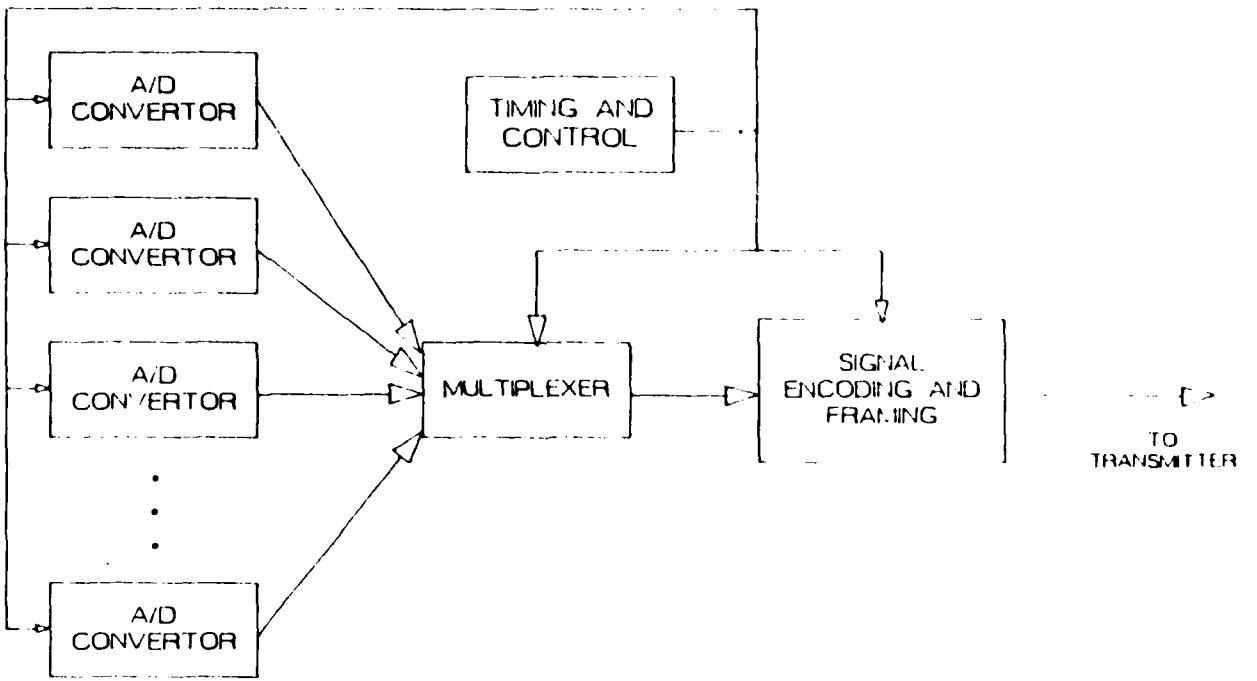

Figure 2. Block Diagram of the Protoype Design

II. DESIGN APPROACH AND DECISIONS

A. GIVEN DESIGN SPECIFICATIONS

The following are the design specifications provided at the beginning of the Prototype design effort.

1. The input signal from a transducer would be analog and have a bandwidth from zero to twenty kilohertz.
2. The circuit would be powered from a battery supply.
3. The analog signal would be sampled at an appropriate rate with each sample being converted into a twelve bit digital word.
4. The transmission channel to shore would be a single fiber optic element.
5. The digital data will be recorded ashore and processed in non-real-time.
6. The circuit would have a low purchase cost to allow it to be expendable.
7. The circuit should have high reliability.

These design specifications were used to further refine the design. The following decisions were made based on the provided specifications.

1. All of the integrated circuit components would be of the complementary metal oxide semiconductor (CMOS) digital family. CMOS devices interface well with a battery supply due to their low power consumption relative to other digital integrated circuit families. An added advantage is the higher noise immunity that CMOS devices exhibit. A disadvantage was that of higher individual component cost.
2. A commercially available analog-to-digital (A/D) converter with twelve bit output word for each sample would be used.

3. The digital signal would be split-phase encoded before being output to the transmission device. This type of encoding, commonly referred to as Manchester encoding, is a standard format in fiber optic transmission. This allows recovery of the clock signal used to send the data signal, and allows for the synchronization of the receiving station without passing the sending clock on a separate control line.

4. The Prototype would be designed for real-time operation in order to strive to maximize both the circuit's sampling frequency and the number of possible analog inputs.

5. All circuit components used should be readily available to keep overall costs low.

B. TIMING REQUIREMENTS AND DATA RATES

Before selecting integrated circuit components in the CMOS family, performance guidelines had to be established. Performance was measured in terms of a component's ability for data throughput, where throughput is defined as the maximum number of bits that a component can process from its input to output in one second. Since a design goal was real-time performance, throughput would be the main consideration. The Prototype was to be capable of, at the least, converting all N transducer signal samples within one sample period.

Shannon's sampling theorem states that a band-limited signal can be uniquely represented by sampled values at equal intervals if sampled faster than twice the signal's maximum frequency. This sampling frequency that is two times the signal's maximum frequency is called the Nyquist

frequency. The given maximum output frequency of a transducer is 20 kHz; therefore the Prototype should sample at a rate greater than 40 kHz. This equates to a required sample period of less than 25 microseconds. The A/D converter chosen should then be capable of performing a conversion in 25 microseconds divided by N, where N is the number of transducers, in order to satisfy Shannon's sampling theorem. The Manchester encoder is also required to encode a 12 bit word from the converter at the same rate of 25/N microseconds. This holds true for the two basic possible modes of interfacing the encoder and converter. The first possibility is that the converter will pass each bit to the encoder as it becomes available. This will be called the serial mode as the converter is transmitting the 12 bit sample word to the encoder serially. The second possibility is that the converter will pass all 12 bits at once after the conversion of a sample is completed. This will be called the parallel mode as now the 12 bit sample word passes in parallel from the converter to encoder. Throughput will be the same for the Prototype regardless of which mode is used. Figure 3 is a timing diagram representing the progression of sample words through a converter and encoder by both the serial and parallel modes. Starting at the top of Figure 3, the first trace is of a command signal. When this signal is high, the analog input is sampled, and when the command signal is low the

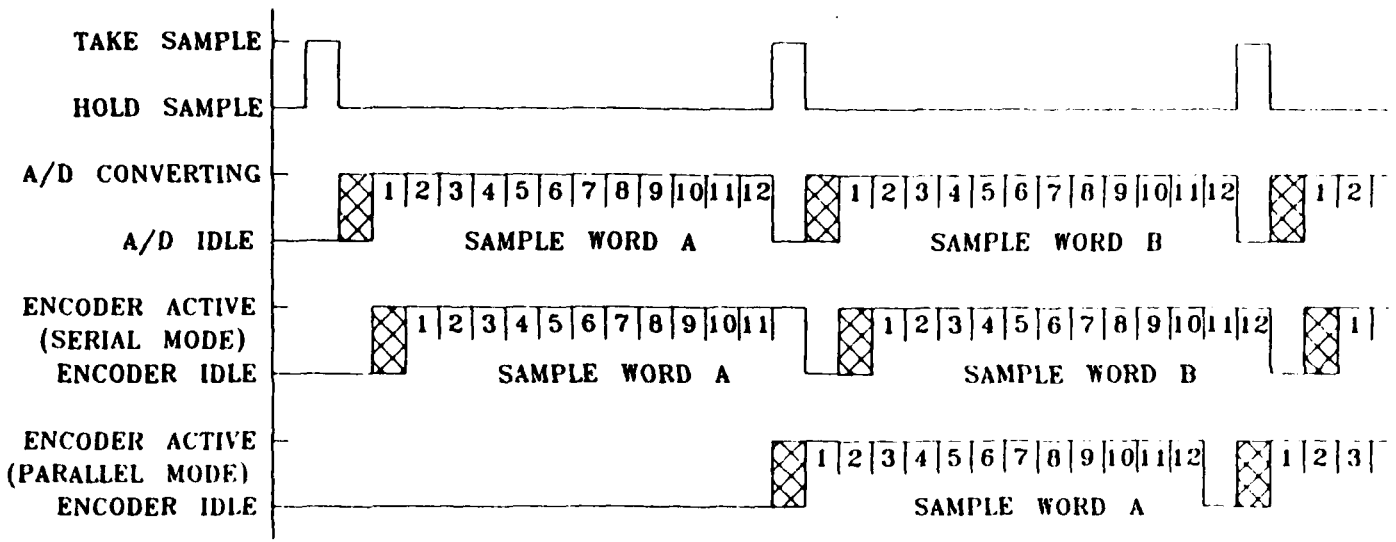

Figure 3. A/D Converter and Encoder Timing Diagram

sample is held constant at the converter's input. The interval between the leading edge of two high pulses represents the sample period. The second trace represents the sequential bit generation of a sample word. Note that the converter senses the high to low transition of the command signal and begins the conversion cycle at that point when a new sample is held constant at it's input. The crosshatch areas represent the inherent time dela, due to the converter's approximation circuitry. The third trace represents the sequential bit encoding of each sample word by the encoder, with the word being passed from the converter by the serial mode. The bottom trace is the same representation as the third trace except each word is passed from the converter to the encoder by the parallel mode. The crosshatch areas in the lower two traces also represent delays due to circuit transition times. By comparing the third and fourth traces it is seen that the difference between the modes is the time it takes a word to propagate through the system. This time is defined as the system's delay time. The parallel mode obviously has the larger delay time; however, it will not dramatically impair the Prototype's real-time performance since the word length is to be less than 25 microseconds.

The system's bottleneck in data throughput will obviously occur at the component which takes the longest time to perform its operation. However, if the restriction

in data flow is due to a slower A/D converter, it is possible to relieve this restriction by multiplexing the N channels after the A/D converter. This would increase the number of A/D converters required to N and therefore increase total system costs. Conversely, it would simplify the multiplexing task since it would now be done to a parallel digital signal. A data flow restriction at the encoder would not be as likely to be relieved in the same manner as this method would require multiplexing serial data and greater cost, due to the N A/D converters required as well as the N encoders. Therefore, it is critical that the Manchester encoder operate significantly faster than the 25 microseconds maximum sample interval. The A/D converter, however, only needs to have a conversion rate less than 25 microseconds. If multiplexing of the N channels occurs between the converter and encoder, then the number of transducers (N) that can be supported by the system will be the throughput of the encoder divided by the throughput of the converter.

The above discussion is based on sampling at just above the Nyquist frequency. Astrom and Wittenmark [Ref. 1, pp. 20-31] discuss choosing a sampling frequency and indicate that the Nyquist frequency does not guarantee a reconstructed signal within acceptable error tolerances if a delay in reconstruction is not permitted. They present formulas for computing the maximum possible error in the

reconstructed signal based on the sampling rate and using either a zero-order or first-order reconstruction method. A standard digital-to-analog converter is an example of a zero-order reconstruction. The reconstructed signal is held constant until a new sample word is provided for conversion. The original signal is then approximated as a series of step functions. To reduce the error in a reconstructed signal a first-order polynomial can be used to extrapolate between the sample points. This is a first-order reconstruction method. Table I gives the results of calculations using these error formulas for a sampled and reconstructed sinusoidal at selected sampling rates. The first column in this Table lists the number of samples per period. Therefore the first row gives values for sampling at the Nyquist frequency. Reading across this first row, we see from the second and third columns, that sampling at the Nyquist frequency yields a maximum relative error of approximately 157 percent for zero-order reconstruction, and 493 percent for first-order reconstruction. The fourth column in Table I lists the sample period in microseconds for the 20 kHz sampled frequency of the Prototype design. Studying Table I, we see that, if a first-order method is used, then 1 percent maximum relative error can be achieved by sampling at 45 times the maximum signal frequency. This equates to a sample period of 1.11 microseconds in the case of this system.

TABLE I
CALCULATED RELATIVE ERRORS EXPECTED WHEN SAMPLING AND RECONSTRUCTING A PURE SINE WAVE

Number of Samples per Period	Maximum Relative Percent Error for Reconstruction Method: Zero-order	First-order	Sample Period in microseconds for a 20 kHz Input Frequency
2	157.080	493.480	25.00
4	78.540	123.370	12.50
10	31.416	19.739	5.00
15	20.944	8.773	3.33
20	15.708	4.935	2.50
25	12.566	3.158	2.00
30	10.472	2.193	1.67
45	6.981	0.975	1.11
50	6.283	0.790	1.00
75	4.189	0.351	0.67
100	3.142	0.197	0.50
200	1.571	0.049	0.25
300	1.047	0.022	0.17
400	0.785	0.012	0.13
500	0.628	0.008	0.10

From Table I, to ensure a maximum relative error of approximately one percent with a zero-order reconstruction, a sampling rate of 300 times the maximum frequency is required. With a maximum frequency of 20 kilohertz this corresponds to a sample period of 0.167 microseconds. This is several orders of magnitude faster than simply sampling at the Nyquist frequency. However, although a real-time design goal was used to maximize the Prototype's throughput performance, higher order reconstruction will actually be possible since the data will be recorded ashore.

The examination of data rate requirements indicates a trade-off between speed and cost of components. If a high quality (low relative error) reconstructed signal is desired, then fewer transducers will be allowed in the network, unless more sophisticated, higher order reconstruction techniques are used on the stored data ashore. At this point, some assumptions were made to permit initial calculations for use in component comparisons. It was assumed that five transducers will be in the network and that twenty percent maximum relative error between the original transducer analog signal and the reconstructed signal is tolerable using a first-order reconstruction method. Using these assumptions and Table I, the system sample period will be five microseconds. If multiplexing of five signals is done after the A/D conversion, then the A/D converter must be capable of a

conversion in five microseconds. If the multiplexing is done prior to the A/D conversion, the converter must have under a one microsecond conversion time. In either multiplexing scheme, the Manchester encoder will have to encode a sample word in under a microsecond. This equates to a throughput of 12 bits per microsecond or 12 megabits per second.

C. THREE POSSIBLE PROTOTYPE IMPLEMENTATIONS

This system required control logic to coordinate the flow of sample words through the components. This was true regardless of whether the A/D converter and encoder operate in a synchronous or asynchronous manner. There were three possibilities considered for implementing the control portion of the system. They were a hardware implemented control logic circuit, an Erasable Programmable Read-Only Memory (EPROM) controller and a microprocessor controller. Early in the project all three seemed feasible.

The hardware controller could consist of a logic circuit with status inputs from the A/D converter, the signal multiplexer and the Manchester encoder. These inputs would generate appropriate control outputs back to the three main components to ensure synchronous operation of the entire system. This hardware controller would be simplified if all circuit components were supplied timing by one common clock.

An EPROM controller would simply consist of an EPROM with its address bus connected to a clocked counter circuit and possibly the status lines from the three system components. The data bus from the EPROM would provide the necessary control inputs back to the components. By appropriate programming of the EPROM, system control could be achieved as the counter sequentially accessed the EPROM's addresses. This controller implementation could possibly reduce the required hardware components and also allow for easier correction of design mistakes or future system expansion.

The microprocessor controller is the most flexible of the three considered possibilities and probably the most expensive. A microprocessor could be used to control the system's components directly via the components' control inputs or to control the data bus and the components' access to it. The growth of the level of complexity of the system would seem almost endless with a microprocessor controller and this might very well be a hindrance in the Prototype's initial design. However, a microprocessor controller would provide the highest number of possible solutions for problems encountered during the initial design as well as flexibility in future system growth.

D. RATIONALE FOR MICROPROCESSOR IMPLEMENTATION

The microprocessor implementation of the system's controller was chosen for the Prototype's design and development for a number of reasons. The added flexibility discussed in the previous section was the most compelling advantage. Being a first design effort this flexibility should prove invaluable to working out problem areas with the most viable solutions. The microprocessor controller has the added feature of being capable of accessing the data bus and providing secondary functions such as pre-processing on the data or providing storage of data for back-up purposes. This flexibility in problem solving and in the design of future system enhancements would add up to lower overall development costs when compared to a hardware or EPROM implemented controller. The microprocessor controller can also perform the multiplexing task between the conversion and encoding stages. However, areas of concern are in the increased number of components and subsequent effects on system cost and power consumption. These two measures of system efficiency will be evaluated on the Prototype.

E. MAIN HARDWARE COMPONENT SELECTION

1. The 80C86 Microprocessor

The 80C86 manufactured by Harris Semiconductor was chosen for a multitude of reasons, but foremost was that it was a CMOS device and readily available. All of the main support circuits that might be needed, such as the clock generator driver(82C84A), serial communications interface (82C52), and priority interrupt controller (82C59A), were commercially available.

Just as important, the 80C86 supports a parallel 16 bit data bus and fully implements the instruction set of the 8086 microprocessor by the Intel Corporation. A 16 bit parallel data bus would provide enough bus width for passing the 12 bit sample word with a single bus access. Two bus cycles would be required on a more common 8 bit data bus microprocessor and present more delay in the processing of each sample word. The fact that there exists a seemingly endless library of reference material on the 8086 assembly code was an additional attribute for using the 80C86. Finally, the 80C86 would be readily interfaced to communicate with any personal computers which are based on the 8086 family of microprocessors.

The last deciding factor was that of the microprocessor's speed or maximum operating clock frequency. The 80C86 was advertised to be a circuit of

static design and therefore required no refresh for its internal registers, counters or latches. The Harris Semiconductor 80C86 specifications sheet [Ref. 2, pp. 3-7] reports that this eliminates the restriction of a minimum operating clock frequency found on other microprocessors. The 80C86 is capable of operating at all clock frequencies down to DC. No upper clock frequency limit was given, but the 82C84A (clock generator driver) imposes a limit of 8.33 MHz on the clock frequency [Ref. 2, pp. 3-82]. This certainly would seem to provide adequate speed for the desired application. The 80C86 reportedly would operate at lower clock frequencies down to and including DC. This would allow single stepping of the microprocessor using the clock and could prove valuable for debugging of Prototype's software.

2. The AD7572JN05 Analog-to-Digital Converter

A cursory search of catalogs of major manufactures of integrated circuits revealed that the maximum advertised conversion times ranged from 12 to 5 microseconds for high speed 12 bit A/D converters. This was assumed to be a fair indicator of the performance that could be expected from readily available converters. The AD7572JN05 is a 12 bit converter at the fast end of this range with the advertised

maximum convert time of 5 microseconds. The circuit is manufactured by Analog Devices Semiconductor as a CMOS device and is commercially available.

The AD7572JN05 was also designed to be easily interfaced to an 8 or 16 bit microprocessor. The circuit incorporates a tri-state data bus along with control inputs to select the converter and to read its data. Advertised bus access and relinquish times are 90 and 75 nanoseconds respectively [Ref. 3, p. 1] which are adequate for interfacing with the 80C86 high speed bus times. An additional reported feature of the AD7572JN05 was its stable operation provided by a buried-zener reference which keeps the full-scale drift low over the range of operating temperatures.

A disadvantage of the AD7572JN05 was that it was a relatively new circuit introduced by Analog Devices Semiconductor in 1986. Therefore, no reference material could be found on application of the circuit other than that provided by Analog Devices Semiconductor specifications information [Ref. 3, pp. 1-12]. However, since this circuit provided the fastest maximum convert time for 12 bits in the available converters, it was chosen for use in the system. Additionally, several sample-and-hold circuits were available from Analog Devices Semiconductor that were designed to interface with the AD7572JN05 and to operate at a comparable speed.

3. The HD-15531B Manchester Encoder/Decoder

Again speed and availability were the prime considerations in choosing the Manchester encoder circuit. The HD-15531B is a CMOS device with an advertised data rate of 2.5 megabits per second and is manufactured by Harris Semiconductor. This circuit is compatible with the 80C86 and Harris Semiconductor provides a circuit schematic and timing diagrams for implementing the HD-15531B as an encoded Universal Asynchronous Receiver Transmitter (UART). Using the HD-15531B as an encoded UART would provide for a simple interface between it and the 80C86 microprocessor.

The disadvantage of the HD-15531B is that its maximum advertised data rate is less than the system's projected need. Recalling the timing discussion earlier in this chapter, a rate of 12 megabits per second was the goal set for the encoding circuit's throughput. The 2.5 megabits per second of the HD-15531B is well short of this. It was the fastest CMOS Manchester encoding circuit however that was readily available within the time frame of this research. The decision to use the HD-15531B necessitated lowering the performance goal for the Prototype. If only one input signal were considered then the required encoder rate would be 2.4 megabits per second to allow it to keep up with the converter rate of a 12 bit sample word every 5 microseconds. Once a single input channel Prototype was built, experiments with the expected signal could be

performed to find the minimum acceptable sample rate. The minimum sample rate determined, along with the reconstruction method, the number of transducer inputs the Prototype would support.

Additional features of the HD-15531B are that it contains an independent decoder circuit and that it is programmable to frame transmitted data into variable lengths. The decoder side of the HD-15531B would be used in the Prototype to provide a decoded word to feed to a digital-to-analog (D/A) converter to reconstruct the signal for comparison to the original signal. This provides a basis for future selection of a minimum sampling rate. The programmable framing feature of the HD-15531B allows for variable word lengths of 2 to 28 bits with a parity bit and a choice of synchronization characters [Ref. 2, pp. 5-24].

III. THE PROTOTYPE CIRCUIT

A. THE ARCHITECTURE

The Prototype was built to test the design concept and obtain actual timing measurements of each selected component. Only one A/D converter was used in constructing the Prototype due to the selected encoder's transmission rate. This was not considered a detriment since only a single channel was necessary to obtain performance measurements of the selected converter and the architecture of the design.

Figure 4 depicts the Prototype's basic architecture. The sampling operation is carried out by having the microprocessor execute an endless instruction loop. On each cycle through the loop a sample is processed in several steps. First, the microprocessor reads a sample word from the A/D converter that is output to the encoder. The microprocessor then idles until the encoder has completed the transmission of the previous sample word before writing the new word to the encoder. Then the microprocessor jumps back to the beginning instruction and reads the next sample word from the A/D converter. The microprocessor waits on the encoder as encoding was perceived to be the slowest process in the cycle. This instruction loop supports as many A/D converters in the system as the microprocessor is capable of addressing.

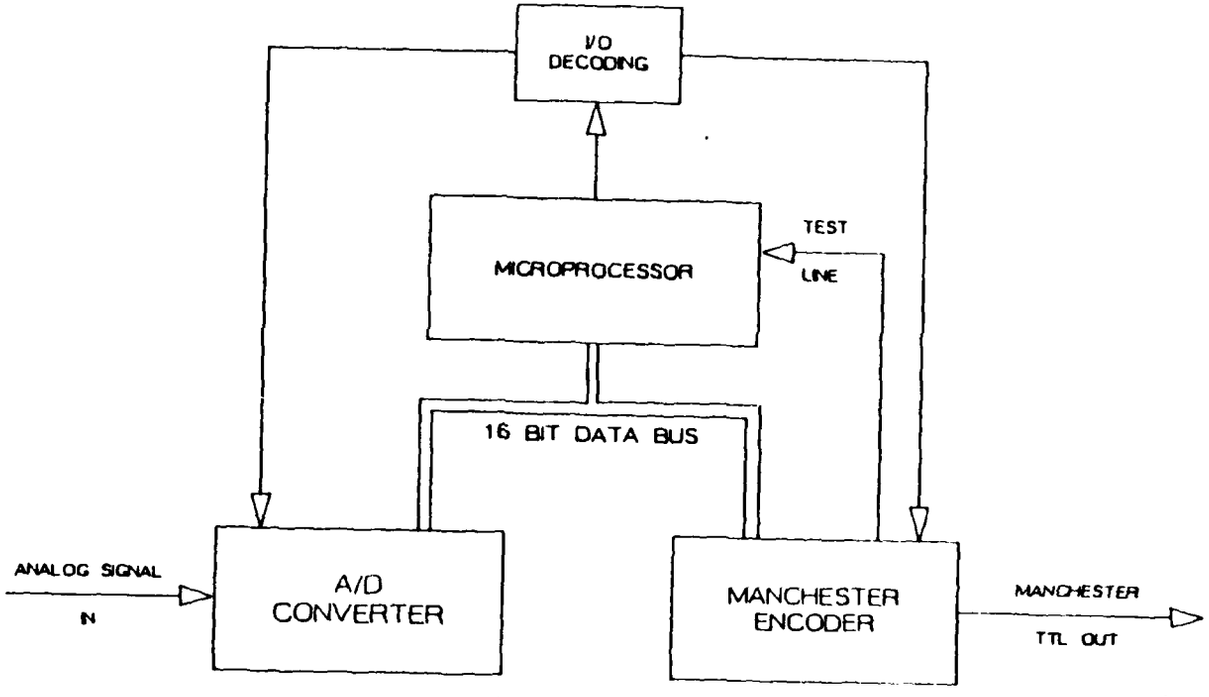

Figure 4. The Basic Prototype's Architecture

In the case of the 80C86, 65,536 different addresses are provided for input and output (I/O) devices. However, the Prototype's present I/O decoding logic provides only for the addition of four more A/D converters to the system's data bus for future expansion.

Each sample word is intentionally directed through the microprocessor as opposed to directly from the A/D converter to the encoder. This was done to determine how much the cycle is slowed by the microprocessor's execution of instruction and whether it would be feasible to do any manipulations of the samples during the instruction loop without detrimental slowing of the sample rate. This also allows a four bit identification header to be attached to the sample word. This header would identify which A/D converter the sample originated from if additional A/D converters were added to the system.

B. THE MICROPROCESSOR CIRCUIT

The 80C86 microprocessor can be configured to operate independently or in a multiprocessor environment. The Prototype's 80C86 was wired to operate in the independent mode which greatly reduced the number of support devices required. Figure 5 shows the 80C86 and the devices supporting its operation in the Prototype. The clock driver is implemented with the 82C84A by Harris Semiconductor. This device takes the input from the

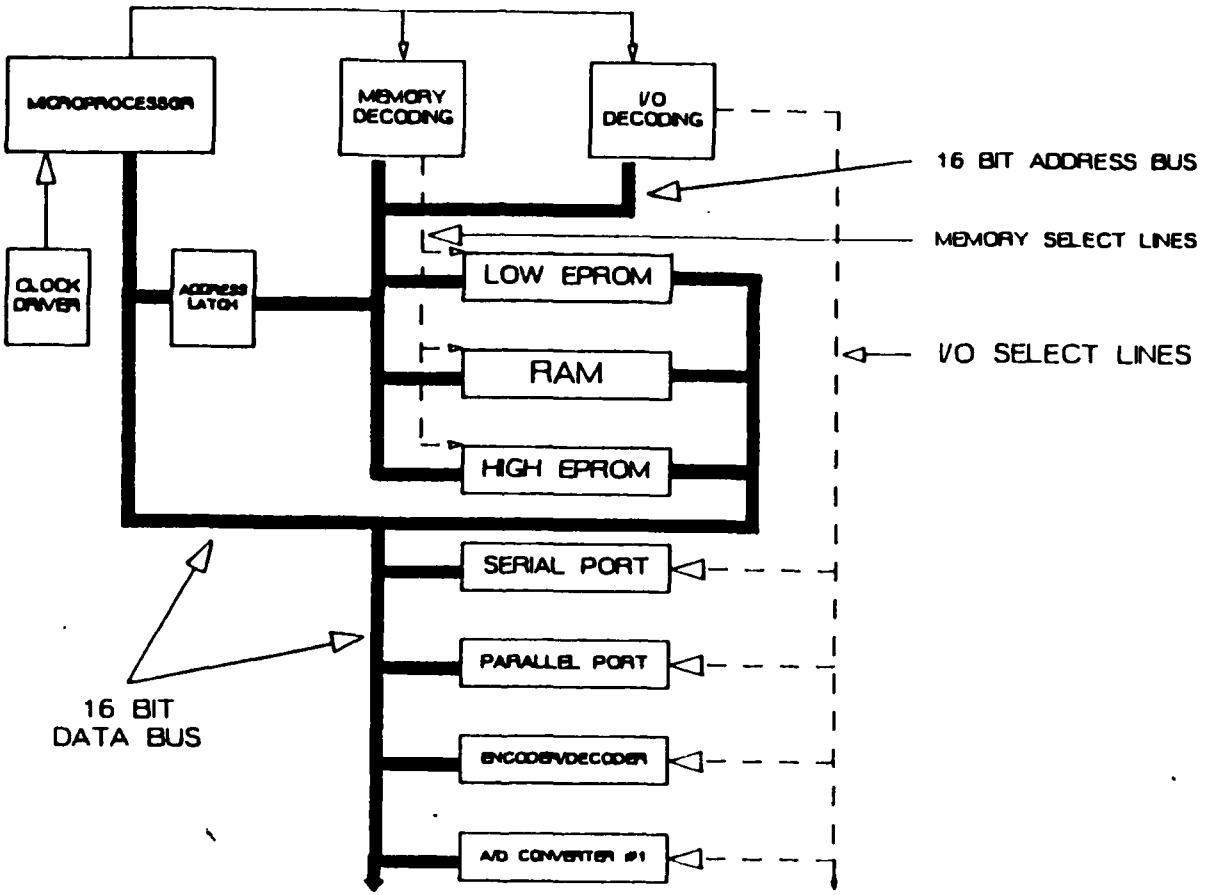

Figure 5. 80C86 Microprocessor and Support Devices

system's oscillator and divides the oscillator's frequency by three. It also provides the 33 percent duty cycle required by the 80C86. Additionally it provides synchronization of the system reset command.

Address latching is required since the 80C86 has a common, time multiplexed bus for both address and data. This common bus allows the 80C86 to be packaged as a 40 pin device and thus take up less space on a circuit board. The 80C86 has 20 address lines but only the lower 16 are utilized in this design since a large memory was not necessary. All 16 data lines are used since this provides for half as many bus cycles since the 80C86 can fetch instructions in words (16 bits at a time). It also allows for all 12 bits of a sample word to be passed in one bus cycle as discussed in the preceding chapter.

The serial and parallel ports shown in Figure 5 are not utilized in the present system, but were included in the Prototype to provide for future system expansion. Table II gives the Prototype's memory and I/O Maps implemented by the decoding logic. It is worth noting that the Prototype provides separate memory and I/O device address decoding. This allows for overlap of memory and I/O addresses. Overlapping of addresses has not been done in the present Prototype software to avoid any confusion by unnecessarily complicating the address mapping.

TABLE II
PROTOTYPE'S MEMORY AND INPUT/OUTPUT MAP

Memory Addresses	
0000 to 0FFF	Low EPROM
4000 to 7FFF	RAM
F000 to FFFF	High EPROM

Input/Output Addresses	
1000 to 1003	Serial Port
1004 to 1007	Parallel Port
1008 to 100B	Encoder
100C to 100F	A/D Converter
1010 to 1013	Reserved
1014 to 1017	Reserved
1018 to 101B	Reserved
101C to 101F	Reserved

C. THE ENCODER CIRCUIT

The Manchester encoder was wired to appear to the system bus as a serial I/O port. Two eight bit CMOS parallel-load shift registers (74C165) are used to latch the data bus when the HD-15531B Manchester encoder receives an enable and write signal from the microprocessor. The encoder side of the HD-15531B provides the necessary logic internally to shift in these registers to provide the 16 data bits serially for encoding. The Prototype's HD-15531B is programmed to provide framing and error checking on 16 bit packets. Figure 6 shows the HD-15531B and its supporting registers. The decoder is similarly provided with two eight bit parallel-out shift registers (74C164) to place the decoder's serial output back on a parallel bus. The decoder's registers are wired however to an isolated 12

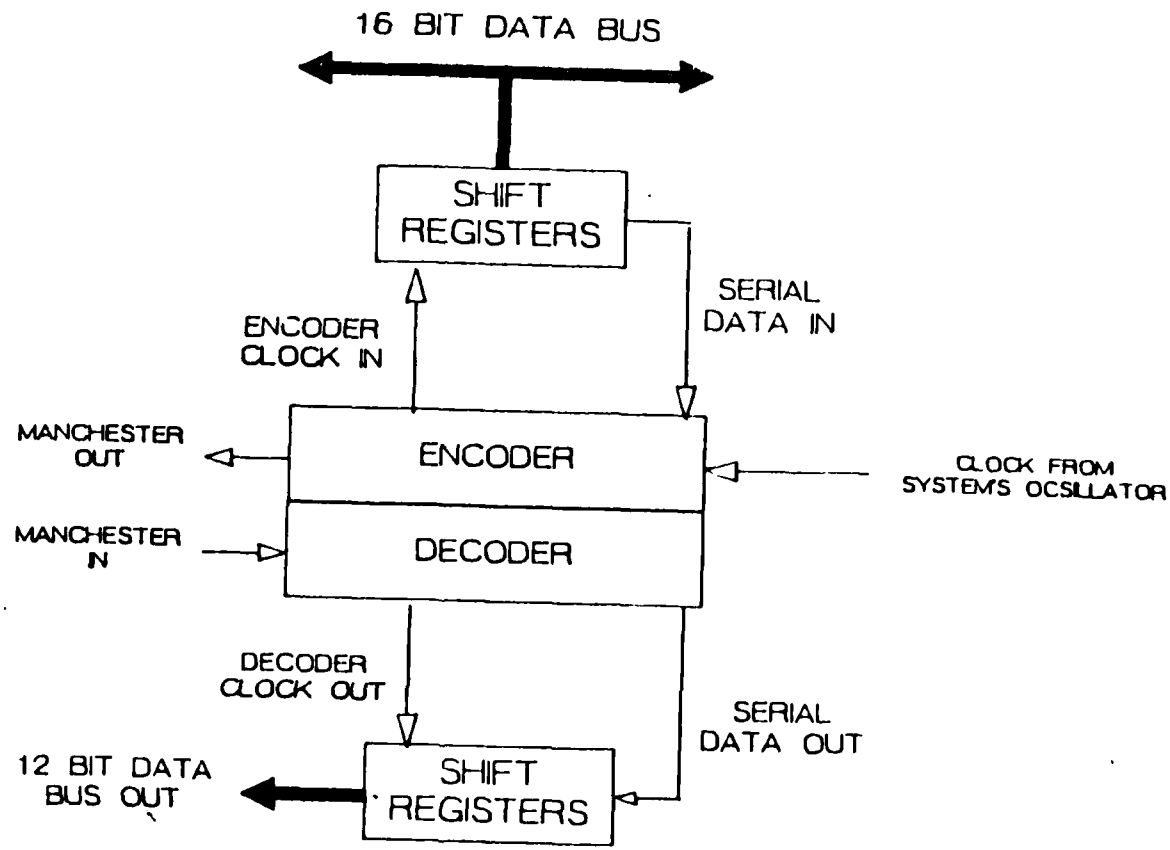

Figure 6. The HD-15531B Encoder/Decoder and Shift Registers

bit bus. This provides the decoded 12 bit word for reconstruction and was used in evaluating the Prototype's performance. The HD-15531B decoder was utilized to emulate the shore station's receiving decoder for the purposes of this project.

D. THE A/D CONVERTER CIRCUIT

The A/D Converter circuit was designed to appear to the system bus as a parallel input port. This was simple to implement due to the buffered parallel data output available from the AD757205 (the 12 bit A/D converter used). When the AD757205 receives an enable and read command from the microprocessor, it places the last converted sample on the 12 bit output, which is connected directly to the lower 12 bits of the system's data bus. The AD757205 simultaneously begins the digital conversion of a new sample of the input analog signal as it outputs the previous sample to the data bus. The circuit consists only of the AD757205 and a sample-and-hold amplifier. An AD583, also manufactured by Analog Devices, was used for the sample-and-hold in the Prototype. The A/D converter circuit is the simplest in the system. This is important, since it is the intent of the architecture that one of these circuits be provided for each analog input.

E. THE PROTOTYPE'S TIMING

The Prototype's timing is provided from a single oscillator to all devices through appropriate divide down circuits. This was done to provide for easy changes in the system's operating speed and also to prevent any delays due to asynchronous operation between devices. Figure 7 indicates the relationships between the system's oscillator and each clocked device. The clock frequencies given in Figure 7 are those of the design's expected limit. A 30 MHz oscillator would provide operation of the HD-15531B encoder/decoder at its advertised upper throughput limit of 2.5 megabits per second. Also, this would drive the AD757205 A/D converter at its optimum operating frequency of 2.5 MHz for a maximum conversion time of 5 microseconds. The 30 MHz oscillator would exceed the advertised upper limit of the 82C84A clock driver of 25 MHz. However, a documented design [Ref. 4] has the 82C84A operating on a 30 MHz crystal. This design lead to experimentally operating the 82C84A on a breadboard with various crystals up to 32 MHz. The 82C84A still produced a satisfactory clock pulse train at this upper frequency and the 30 MHz design oscillator frequency appeared to be within the 82C84A operational range. There was no difficulty expected in operating the 80C86 microprocessor at 10 MHz.

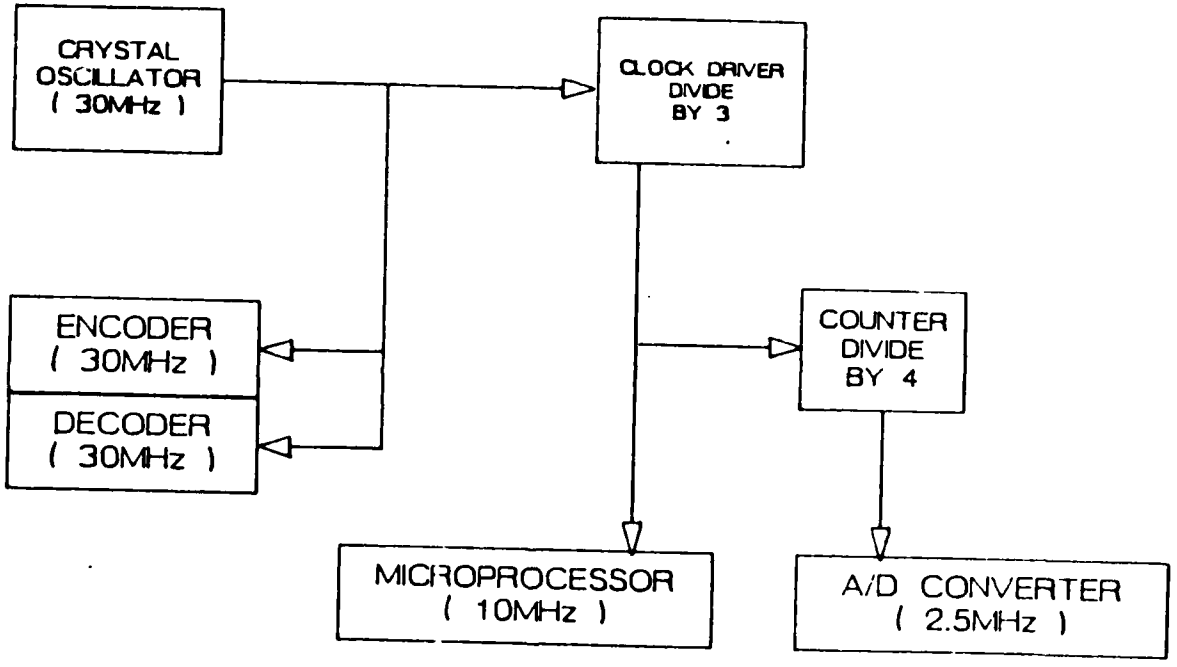

Figure 7. The Clock Relationships of System Devices

F. SOFTWARE

As discussed in the beginning of this chapter, the microprocessor's operating instruction routine was to be extremely simple for the purposes of bench-testing and evaluating the Prototype. The initial loop is as follows in 80C86 assemble language syntax:

```
        MOV     DX, 1F0C;       Load A/D converter address
START   IN      AX, DX;         Read A/D sample word
        MOV     DL, 08;         Load encoder address
        WAIT;                   Test to see if encoder is done
        OUT     DX, AX;         Write sample word to encoder
        MOV     DL, 0C;         Load A/D converter address
        JMP     START;          Loop forever
```

This routine provides for the maximum overlap of the A/D converter and encoder operation before the microprocessor idles waiting for the encoder to finish its transmission. The routine is so short that it was loaded in the high EPROM memory starting at the hex address FFF0. This is the address that the 80C86 goes to on a reset for a vector routine to re-initialize the microprocessor. The above routine occupied twelve of the sixteen bytes reserved in high memory for the reset vector. During the evaluation of the Prototype the software never outgrew this reset vector space and therefore the low EPROM and RAM were never utilized.

G. PREDICTED DATA THROUGHPUT

With the Prototype operating at the design oscillator frequency of 30 MHz the A/D converter should be able to produce a sample every five microseconds in the worst case (full scale deflection of the analog signal). The encoder would be transmitting at 2.5 megabits per second or a 16 bit word every 6.4 microseconds, so the encoder is the bottleneck in data flow. The other expected delay in a sample cycle would be the time required for the microprocessor to execute the instructions that test to see if the encoder is idle and then write a sample to the encoder. At this point the 80C86 WAIT instruction should be described. This instruction causes the microprocessor to check the logic level of its input pin labelled "test". If this input is a logic low then execution continues. If the input is a logical high, then the microprocessor idles until the input goes low. The WAIT instruction takes three clock cycles even if the "test" input is low when the instruction executes. The instruction writing to the encoder will take four processor clock cycles. Therefore the total time involved in the execution of these two instructions should be 0.7 microseconds. Operating with a 30 MHz oscillator we should achieve a sample rate of 7.1 microseconds or 140.8 kilohertz. This would give us seven times the maximum expected analog frequency.

H. PROTOTYPE CONSTRUCTION

The Prototype's main board was constructed using wire wrap methods on a board with an edge connector and chassis enclosure that made it compatible with the TM503 Instrument rack manufactured by Tektronix [Ref. 5]. This board and chassis were used to provide size constraints on the Prototype's circuit since it would eventually be enclosed in a container for underwater deployment. It was felt that the smaller the final package the better. The board and chassis also made it convenient to draw power from the TM503 Instrument rack. This reduced bench top clutter during evaluation tests since numerous power supplies were not required. Voltage regulators were installed on the main board to step down the TM503 voltages to the required 5, +15 and -15 values. These regulators also provided protection for the CMOS devices.

All of the Prototype's components were provided sockets on the main wire wrap board with the exception of the A/D converter circuit components. Due to the recommendation of Analog Devices against using a wire wrap board for the AD757205 [Ref. 3, p. 9], a circuit board was required to insure achieving the maximum performance from the AD757205. A two-sided circuit board was laid out using an interactive software package on a personal computer. The two-sided board was necessary to provide the A/D converter

and sample-and-hold amplifier with a large ground plane to improve noise immunity and reduce leakage currents from the sample-and-hold circuit. The circuit board was provided with a socket to mate it to a plug installed on the main board. The AD757205 was connected to allow bipolar input signals between a negative and positive 2.5 volts.

A coaxial female plug was installed on the front panel of the chassis for input of the analog signal. Additional female plugs are provided for Manchester output from the encoder, Manchester input to the decoder, and the 12 bit sample word in parallel along with a valid word output from the decoder. The only other fixtures on the front panel are a system reset button and a light indicating the system has power. The front panel layout is shown in Figure 8.

All construction was done by the author with the exception of the circuit board. The Naval Postgraduate School Production Lab produced the board and installed the component sockets using board layouts done by the author. Detailed wiring schematics and the circuit board layout for the Prototype are on file with the thesis advisor.

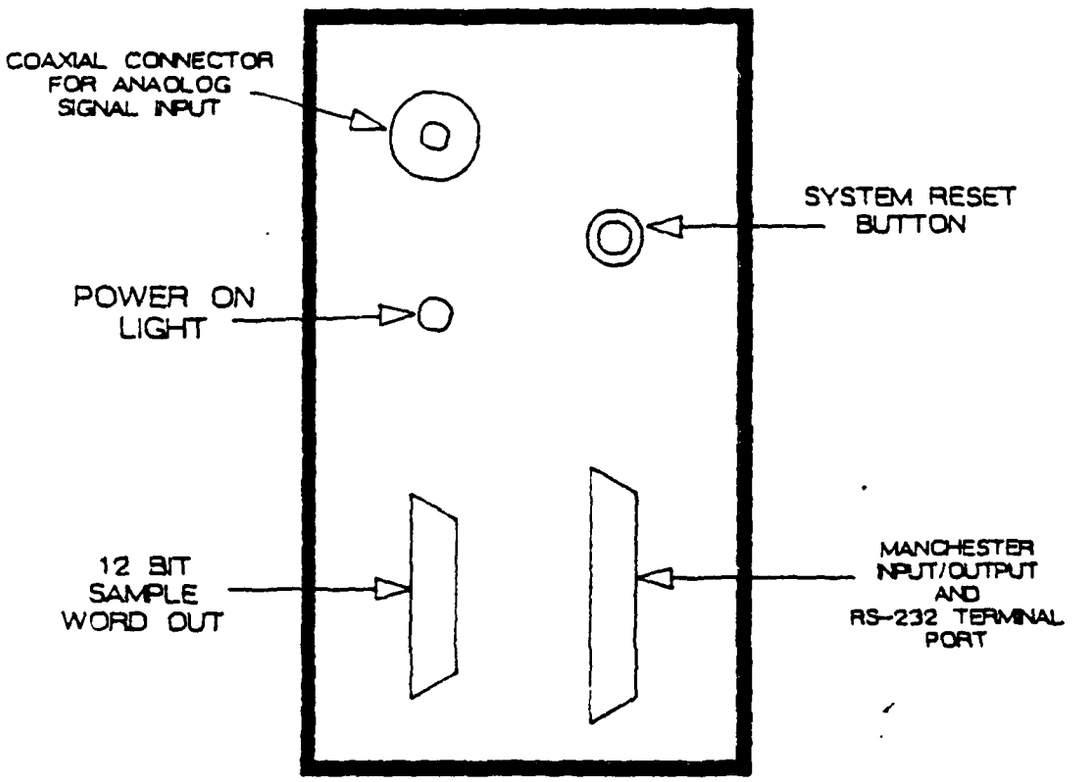

Figure 8. Prototype's Front Panel Layout

IV. PROTOTYPE TEST AND EVALUATION

A. BENCHTESTING SET-UP

The analog signal input was provided by a signal generator for the Prototype's evaluation. The output of the encoder was connected directly to the input of the decoder to simulate the transmission of the Manchester code over a fiber optic channel. The twelve bit parallel output from the decoder was connected by a ribbon cable to a reconstruction circuit assembled on a breadboard. This circuit consisted of two eight bit shift registers (used to provide sample words in parallel from the decoder's serial output), a twelve bit digital-to-analog converter (D/A) and two operational amplifiers. The twelve bit sample word latch was triggered when the decoder indicated that it had received and decoded a valid word. A DAC7541 by Analog Devices was used for the D/A converter. Operational amplifiers completed the reconstruction circuit and provided conversion of the D/A converter's current output to voltage. This circuit is a zero-order type reconstruction of the original analog signal. A simple resistor and capacitor filter was placed on the operational amplifier's output to provide a simple first-order reconstruction of the analog signal. A 60 MHz oscilloscope was used to display the input and reconstructed output for evaluation.

B. TIMING DIAGRAMS

Timing diagrams of the Prototype's operation were recorded using a Hewlett-Packard Model 1615A logic analyzer driving a Hewlett-Packard Model 7470A plotter. Figure 9 is a timing diagram of the data flow through the system. Trace 0 is the chip select line for the A/D converter which is active low. Trace 1 is the A/D converter's output which indicates conversion is in progress when the output is high. Trace 2 is the read line from the microprocessor and is active low. The remaining traces pertain to the Manchester encoder/decoder. Trace 3 is the encoder's enable input which is active high. Trace 4 is the microprocessor's write line used to latch the encoder's shift registers on an active low. Trace 5 is the clock to the encoder's shift register and trace 6 is the decoder's shift register clock. Traces 5 and 6 indicate when a latched word from the system's data bus is being shifted into the encoder and out of the decoder. Note that sixteen clock pulses are present each time either shift register clock is active. The last trace shown (number 7) is of a decoder output which indicates that a valid word has been received and decoded with an active high.

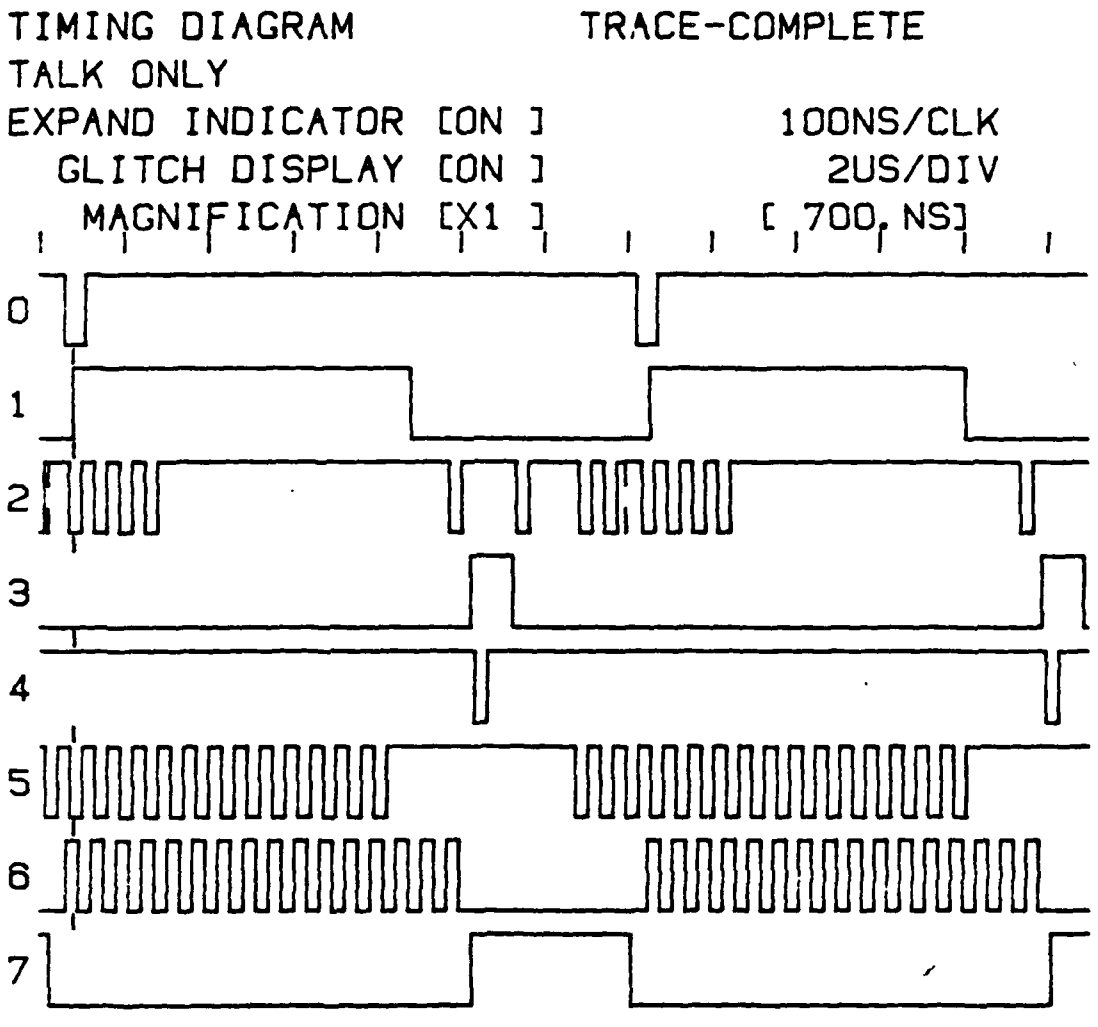

Figure 9
Timing Diagram of Data Flow Through Prototype

It can be seen that as soon as a new word begins to shift out of the decoder, this output goes low until the sixteen bit frame received has been completely shifted out. This output is used to latch the last twelve bits for the D/A converter for signal reconstruction.

The traces in Figure 9 were recorded with a 20 MHz oscillator driving the system's clocks. It is predicted that the system's performance is approximately two-thirds of that calculated for the 30 MHz design oscillator frequency. Examining Trace 1, the A/D converter is taking approximately 8 microseconds to do a conversion, about two-thirds the five microsecond conversion rate expected at 30 MHz. From Trace 5, the encoder is transmitting sixteen bits in approximately 10 microseconds, or at a data rate of 1.6 megabits per second. Again the encoder is performing as expected at this clock frequency. However, the entire system cycle is taking longer than would be expected. Trace 1 shows that the sample rate being achieved is approximately 13.5 microseconds or a sample frequency of 74 kHz. This is fourteen percent slower than expected.

The slower operation is due to unexpected delays in two areas of the cycle. Both delays can be seen by comparing traces 4 and 5. A delay of seven processor clock cycles was predicted between the completion of one encoder transmission and the beginning of the following one.

There is approximately a two microsecond delay between the end of an encoder transmission and the write from the microprocessor to the encoder with the next sample word for transmission. A one microsecond delay would be expected for 7 processor clocks at 6.67 MHz (20 MHz divided by 3). The answer is found on Trace 2 where we see that the microprocessor is executing a read prior to writing to the encoder. This indicates a memory fetch and four additional processor cycles than expected for a 1.65 microsecond delay.

The other delay occurs after the write to the encoder. There is approximately two microseconds delay between the write to the encoder and the actual beginning of transmission. This should have been expected as the encoder sends out a synchronization character and parity bit prior to the frame transmission. This delay represents the price paid in time for the framing and error detection features of the encoder. Considering these new cycle delays and using a 14 percent slower sampling rate, the predicted operation of the Prototype would be a maximum sampling frequency of 121 kHz or approximately six times the maximum input frequency.

C. RECONSTRUCTED SIGNAL WAVEFORMS

Evaluation of sample accuracy of the system was done by comparing an analog input signal to the reconstructed signal from the Prototype's sample word after Manchester decoding. The input and reconstructed signals were displayed simultaneously on a 60 MHz oscilloscope using the decoder's valid word output as an external trigger source for the scope.

Figure 10 shows a 2.6 kHz sine wave with a four volt peak-to-peak amplitude. This was the first test input and the zero-order reconstructed waveform is also shown. The reconstructed wave was displayed on a 0.5 volt per division scale and therefore is less than half the amplitude of the input signal. This signal attenuation can be easily corrected using an operational amplifier with the properly scaled gain to reconstruct the signal's amplitude to that of the input. Figure 11 is the same input signal only now the reconstructed wave form is passed through a single stage resistor capacitor (RC) filter to display a crude first-order reconstructed signal. The system does a good job in accurate digital conversion of a 2.6 kHz input signal. This is as expected since the signal is being sampled at approximately 30 times its frequency. Referring back to Table I, we should be observing about 10 percent error in the reconstructed signal in Figure 10 and 2 percent in Figure 11.

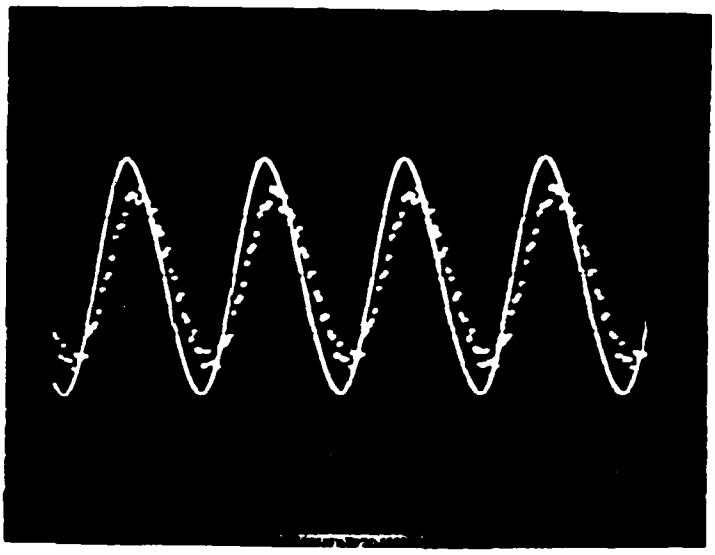

Figure 10
2.5 kHz Sine Wave Input and Zero-order Reconstructed Output (Scale: 150 microseconds/division)

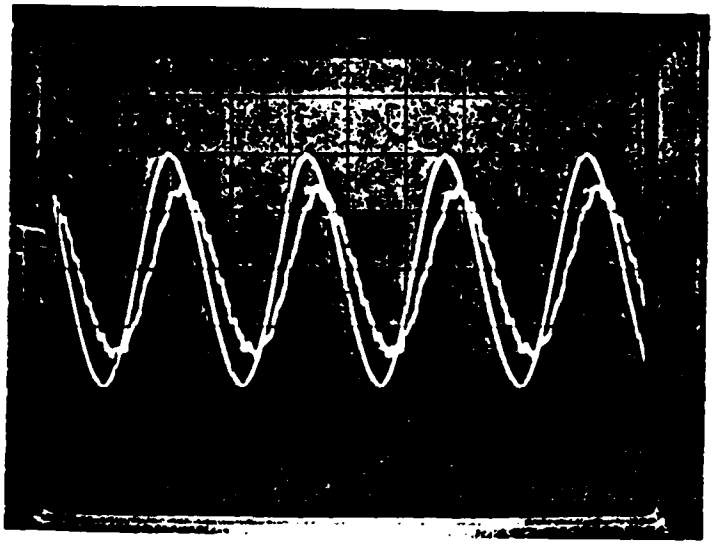

Figure 11
2.5kHz Sine Wave Input and First-order Reconstructed Output (Scale: 150 microseconds/division)

There is a noticeable phase shift between the two waveforms in the preceding figures. This is due to the delay in sample processing by the system. Recall that the A/D converter always outputs the previous conversion and begins a new one when it receives an enable and read from the microprocessor. We therefore fall one sample period behind at the A/D converter. Referring back to Figure 9, it takes approximately 22 microseconds from the time a sample is read at the A/D converter until it is latched at the D/A converter's bus by the decoder's valid word output. So the total delay or phase shift we should see in these test waveforms is around 35 microseconds. Figures 12 and 13 are again the same test waveforms as in the previous figures only the oscilloscope's time scale is now 50 microseconds per division. The delay is measured to be approximately as expected. It should be noted that this delay is expected to remain constant regardless of the frequency of the input signal as the delay is dependent on the system clock frequency. However, the phase difference will naturally grow as the input signal frequency is increased. A delay of 35 microseconds is not seen as detrimental to the design goal of real-time operation in this application.

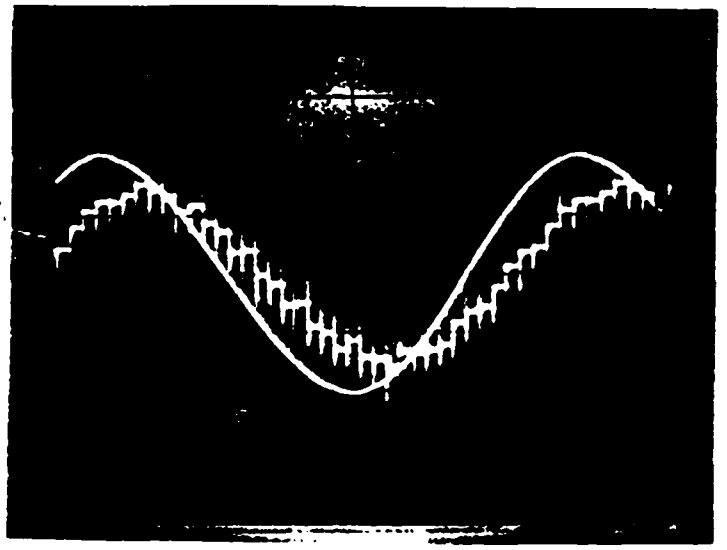

Figure 12
2.6 kHz Sine Wave Input and Zero-order Reconstructed Output (Scale: 50 microseconds/division)

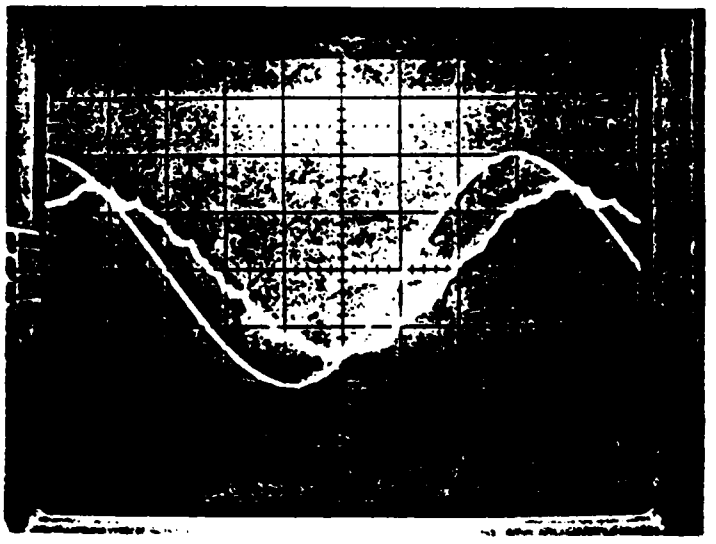

Figure 13
2.6 kHz Sine Wave Input and First-order Reconstructed Output (Scale: 50 microseconds/division)

In Figures 14 and 15 we see a 10 kHz input signal with its zero-order and first-order reconstructed signals respectively. The sampling rate has now dropped to approximately 7.4 times the input signal frequency. Table I, indicates we should expect about equal error in both reconstructed waves of approximately 40 percent. The photographs appear to support this. In fact, the time difference between the input signal and reconstructed signals appears to have grown larger than 35 microseconds. This however is due to the large error in signal reconstruction.

A 19.2 kHz input signal with the respective reconstructed signals is shown in Figures 16 and 17. The sample frequency is now only four times that of the input frequency. Table I now predicts that the error in the first order reconstruction will be over 100 percent and the zero-order about 78 percent. Again, the reconstructed waveforms support the values in Table I.

The last test input signal was a 2.4 kHz square wave with a 4.5 volt peak-to-peak amplitude. Figures 18 and 19 show the zero-order and first-order reconstructed signals. The square wave input was used to measure the variation between sample outputs when a constant voltage signal is processed by the system. This would provide some

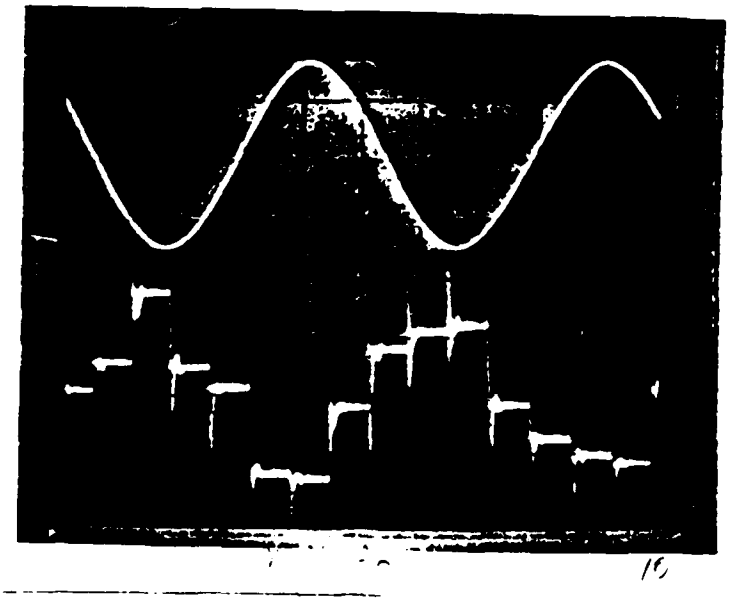

Figure 14
10 kHz Sine Wave Input and Zero-order Reconstructed Output (Scale: 20 microseconds/division)

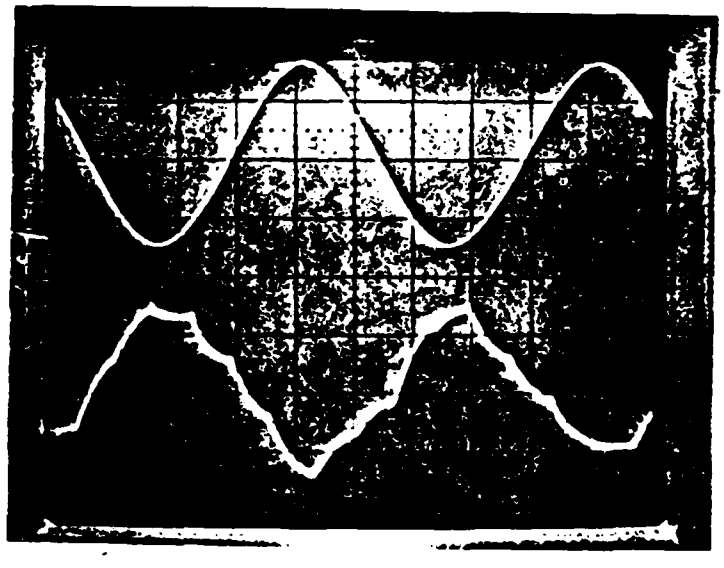

Figure 15
10 kHz Sine Wave Input and First-order Reconstructed Output (Scale: 20 microseconds/division)

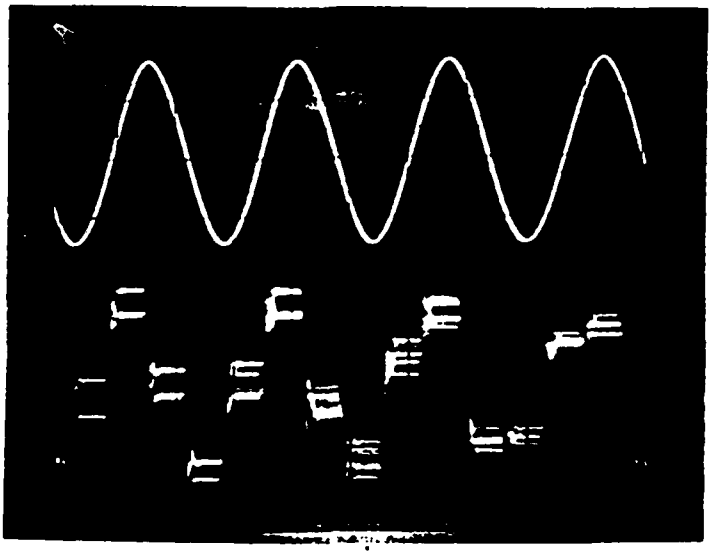

Figure 16
19.2 kHz Sine Wave Input and Zero-order Reconstructed Output (Scale: 20 microseconds/division)

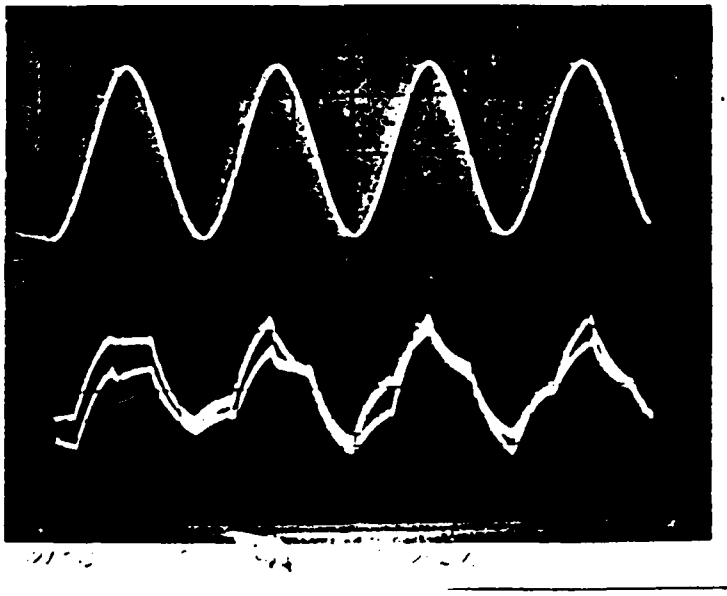

Figure 17
19.2 kHz Sine Wave Input and First-order Reconstructed Output (Scale: 20 microseconds/division)

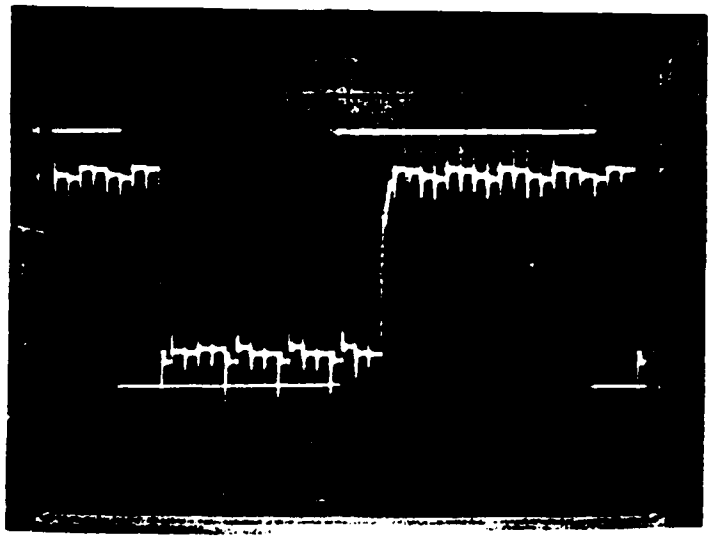

Figure 18
2.4 kHz Square Wave Input and Zero-order Reconstructed Output (Scale: 50 microseconds/division)

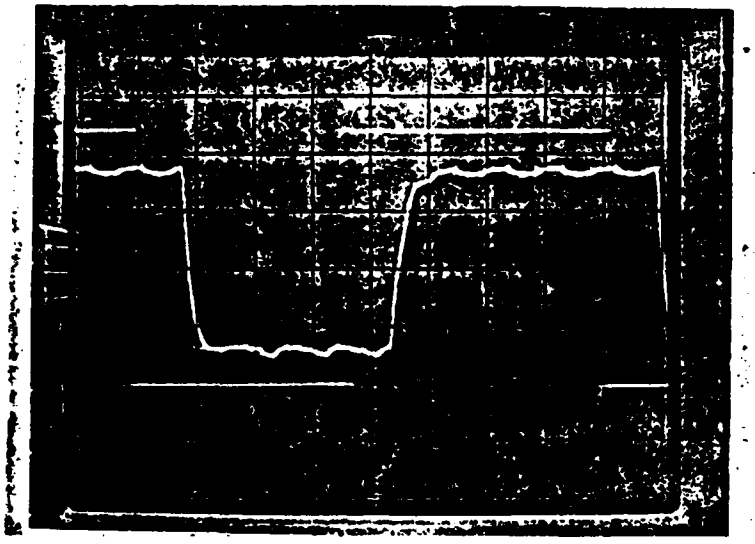

Figure 19
2.4 kHz Square Wave Input and Zero-order Reconstructed Output (Scale: 50 microseconds/division)

indication of the inherent error present in the system design itself. The reconstructed signals displayed in the two photographs are on the 0.5 volts per division scale. Both reconstructed signals vary approximately 0.1 volts when they should be holding a constant value. This would be approximately 6 percent of the peak-to-peak amplitude of the reconstructed signals. Table I gives a maximum error of 10 percent for the zero-order reconstruction and 2 percent for the first-order. The only direct conclusion that can be drawn from Figures 18 and 19 without further investigation is that the sample error occurs in a definite repetitive pattern. This could be caused by a high frequency symmetric noise signal riding on the waveform generator's output.

V. CONCLUSIONS AND RECOMMENDATIONS

A. PROTOTYPE SYSTEM PERFORMANCE

With the 20 MHz oscillator installed, the Prototype was able to sample at approximately 74 kHz. When a 32 MHz oscillator is available (several have been placed on order), it should be installed and the system performance verified. A 33 percent improvement in the throughput would be expected and the Prototype should achieve a sampling frequency of approximately 111 kHz.

The present sampling frequency allows a 20 kHz signal to be sampled approximately four times a period. This is inadequate for even a single analog input unless higher-order reconstruction algorithms are used. If the Prototype performs as expected with a 30 MHz oscillator, then the 20 kHz input will be sampled roughly 5.5 times a period. This still may not provide for an accurate enough zero-order reconstructed signal for even a single input.

B. IMPROVING THE DESIGN'S PERFORMANCE

The bottleneck in the present design is the serial encoding of the parallel sample words. If five A/D converters were installed and each one read every five microseconds, the microprocessor would be writing a sample

word to the encoder at the rate of one per microsecond. This rate of operation is theoretically possible with the present Prototype operating on a 30 MHz oscillator with software modified to read five A/D converter addresses in each loop through the routine. This would provide for each analog input to be sampled at 10 times the maximum input frequency, an acceptable rate to insure moderately accurate zero-order reconstruction. However, the encoder would have to be capable of transmitting at rates around 20 megabits per second to provide for sending a 16 bit frame with parity bit and a synchronization pattern. There are Manchester encoder/decoder devices on today's market with rated transmission rates of up to 25 megabits per second. These devices do not have the framing and error detecting features of the Prototype's encoder.

C. PROTOTYPE SYSTEM EXPANSION

The present Prototype has the hardware wiring in place to support communications with an external terminal. There also exists enough memory expansion available to allow the addition of software for terminal communication such as an interactive monitor program. This would provide an excellent environment for future software development if the Prototype is used for future research.

There is very little room left on the main system board for any additional hardware. The removal of the parallel ports, which are not used at this time, would provide room equivalent to two 40 pin devices.

D. POWER CONSUMPTION

The Prototype was provided power by three metered power supplies during evaluations using the logic analyzer. Rough measurements of the Prototype's power consumption were made using the current and voltage outputs of the power supplies. This gave an instantaneous power consumption of 14.3 Watts for the Prototype. The majority of this power is being radiated as heat from the voltage regulators. This figure should be used only as a basis for determining relative power requirement changes after future circuit alterations to the Prototype. The actual power consumption of the circuit should be in the milliwatt range. The replacement of the few non-CMOS devices with their CMOS counterparts will relatively lower the power needs.

The design of a power-down circuit is recommended as the microprocessor and clock driver are both well suited for such implemention. The devices have standby modes with considerably less power required. When the system has no

analog signals input that are of interest to the user, the system could be placed in a stand-by mode to conserve the battery supply. Morz and Niewierski discuss additional application techniques for reducing the power requirements of CMOS circuits and power-down designs in a recent paper [Ref. 6, pp.185-191].

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