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**RADC-TR-87-198**  
Final Technical Report  
November 1987



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# **AUTOMATED TEST REQUIREMENT DOCUMENT GENERATION**

**Rockwell International Corporation**

**Robert Haas and Fred Suzuki**

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**Air Force Systems Command**  
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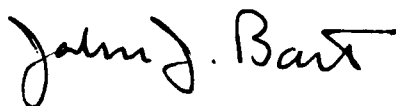
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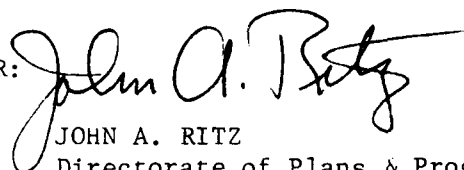
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REPLY TO  
ATTN OF: XP (Capt Evans/Av587-3705)

14 Jul 88

SUBJECT: Technology Screening of Unclassified/Unlimited Reports

TO: DTIC/HAS

1. Reference your letter, 9 Jun 88 same subject, we have reviewed the following report for security and critical technology:

Source: Rockwell International Corporation  
Title: Automated Test Requirement Document Generation  
Contract No. F30602-85-C-0019  
Report No. RADC-TR-87-198  
Date of Report: November 1987

2. We do not feel the report contains any critical technology. It is a study of who is doing TRD generation manually and via CAD/CAE. They make recommendations on how to streamline this process by incorporating better methods as well as computer tools. No software or hardware configurations are presented in depth or prescribed by the report. The report lists software available to do CAD/CAM but these are typical listings one would find in a vendor's catalog. No specific techniques for modeling Units Under Test (UUT's) are given, just different possible generic methods. This is because a UUT is not a specific device in this report. It could be any type of Circuit, Board or System.

3. Based on our review we feel that this report can have unlimited release.

  
BILLY G. OAKS  
Directorate of Plans & Programs



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SECURITY CLASSIFICATION OF THIS PAGE

| REPORT DOCUMENTATION PAGE  |       |   |   | Form Approved<br>OMB No. 0704-0188 |                                  |
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| 09   | 01    |   |   |                                    |                                  |
| 14   | 02    |   |   |                                    |                                  |
| 19 ABSTRACT (Continue on reverse if necessary and identify by block number)<br>This study summarizes the potential and requirements for automating the Test Requirement Document (TRD) generation process. TRDs are complex, time consuming and very expensive to prepare. Cost reduction of the TRD generation process is requisite for improving the life-cycle cost of weapon systems.<br><br>Current state of the art was surveyed to form a basis for identifying generation techniques employed, planned improvements and future improvement objectives. A prominent limitation is that many current CAD/CAE workstations are incapable of maintaining large data bases efficiently, thus limiting possibilities of combining programs on a common host. This roadblock and other technological and logistic hurdles are identified and investigated. The extent of current automation is discussed.<br><i>Requirements, data acquisition, state of the art.</i> |       |   |   |                                    |                                  |
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## GLOSSARY OF ACRONYMS

### ABBREVIATION

### DEFINITION

|          |  |
|----------|--|
| AFSATCOM | Air Force Satellite Communication              |
| AI       | Artificial Intelligence                        |
| ASIC     | Application Specific Integrated Circuits       |
| ASSD     | Autonetics Strategic Systems Division          |
| ATE      | Automatic Test Equipment                       |
| ATLAS    | Abbreviated Test Language for All Systems      |
| ATPG     | Automatic Test Program Generation              |
| ATRED    | Automatic Test Requirement Document            |
| ATRD     | Automatic Test Requirement Document            |
| ATRD     | Automatic Test Requirement Document Generation |
| BILBO    | Built-In Logic Block Observer                  |
| BIT      | Built-In-Test                                  |
| BIST     | Built-In-Self-Test                             |
| BITE     | Built-In-Test Equipment                        |
| CAD      | Computer Aided Design                          |
| CADAT    | Computer Aided Design And Test                 |
| CAE      | Computer Aided engineering                     |
| CAMELOT  | Computer Aided Measure of Logic Testability    |
| CEPS     | CITS Expert Parameter System                   |
| CITS     | Central Integrated Test System                 |
| DB       | Data Base                                      |
| DoD      | Depart of Defense                              |
| EM       | Electro-mechanical                             |
| EMMA     | Expert Missile Maintenance Aid                 |
| ENG      | Engineering                                    |
| FORTTRAN | Formula Translation                            |
| HILDO    | Highly Integrated Logic-Device Observer        |
| HITS     | Hierarchical Integrated Test Simulator         |
| ID       | Identification                                 |
| IR&D     | Independent Research and development           |
| ITA      | Interface Test Adaptor                         |
| LASAR    | Logic Automated Stimulus and Response          |
| LRU      | Line Replaceable Unit                          |
| LSSD     | Level-Sensitive Scan Design                    |
| MATE     | Modular Automatic Test Equipment               |
| MSI      | Medium Scale Integration                       |
| NSIA     | National Security Industrial Association       |
| PAWS     | Personal ATLAS Workstation                     |
| PROC     | Procedure                                      |
| QA       | Quality Assurance                              |
| RADC     | Rome Air Development Center                    |
| REF      | Reference                                      |
| REQ      | Requirement                                    |
| REQMTS   | Requirements                                   |



GLOSSARY OF ACRONYMS continued

ABBREVIATION

DEFINITION

|        |  |
|--------|--|
| SCOAP  | Sandia Controlability/Observability Analysis Program |
| SIM    | Simulator  |
| SPICE  | Simulation Program with Integrated Circuit Emphasis  |
| SSI    | Small Scale Integration                              |
| SRU    | Shop Replaceable Unit                                |
| STRAT  | Strategy   |
| SYSCAP | System Circuit Analysis Program                      |
| TAD    | TRD ATLAS Development                                |
| TDA    | Testability Design Aid                               |
| TEST   | Tester   |
| TISSS  | Tester Independent Software Support System           |
| TPS    | Test Program Set                                     |
| TRD    | Test Requirement Document                            |
| TTL    | Transistor-Transistor Logic                          |
| UUT    | Unit Under Test                                      |
| VHSIC  | Very High Scale Integrated Circuits                  |
| VLSI   | Very Large Scale Integration                         |
| VMS    | Virtual Memory System                                |
| WP     | Wordprocessor  |

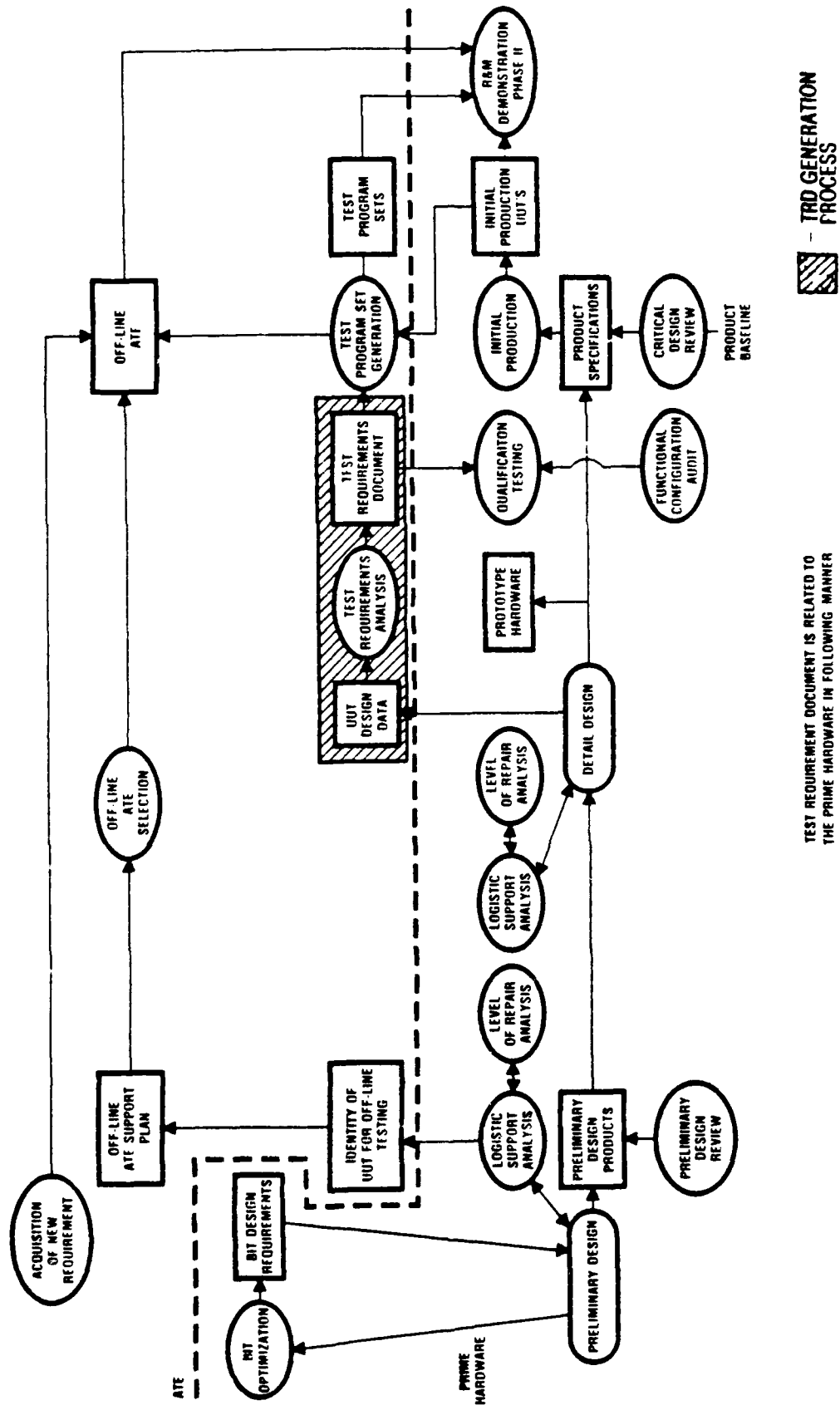
## EXECUTIVE SUMMARY

### INTRODUCTION

The testing process for a Unit Under Test (UUT) relies on a series of interrelated Automatic Test Equipment (ATE) and prime hardware elements to produce the desired testing results. The Test Requirement Document (TRD) is the key to the transition of the UUT design into a product with known, verifiable performance. Figure EX-1 illustrates the relationship of the TRD to the test environment.

The TPS provides the Test Program and Interface Test Adapter (ITA) needed to interface a UUT to the automatic test equipment. The process for developing these items starts with the TRD, which provides all of the UUT test requirements.

The TRD development currently starts after the design has been finalized due to the high cost of TRD development. If a rapid automated process is available, the TRD can be developed based on preliminary design data. The TRD can then be used iteratively to determine if testability requirements for isolation and detection have been met and if test points, control circuits, BIT, BITE or redesign is needed before any commitments for hardware development are made. As the design reaches finalization, a simple update to the TRD data base will allow for generation of the final TRD.



TEST REQUIREMENT DOCUMENT IS RELATED TO THE PRIME HARDWARE IN FOLLOWING MANNER

TRD GENERATION PROCESS

Figure EX-1 TRDs Relationship to the Test Environment

## PURPOSE OF THE STUDY

The purpose of this effort was to investigate the processes involved and develop an approach aimed at the automation of Test Requirement Documents (TRD), and the incorporation of that capability into computer aided design (CAD) processes. This effort was divided into the following tasks:

Automated  
TRD  
Generation

- Survey current methods of TRD generation and application.
- Investigate various means used by skilled engineers to manually perform TRD development tasks.
- Identify and assess the current state-of-the-art automation of TRDs.
- Evaluate and assess those methods investigated.
- Investigate near future and future prospects for automating TRD generation.
- Recommend a course of action which can be used as a guide for implementing a program of transition to a fully automated TRD.

The program was divided into two phases.

1. Perform an industry and government wide survey analysis to determine current generation methods, application of TRDs, and to establish the role of the TRD in the Unit Under Test's (UUT) development cycle. The first phase also included defining the manual methods used for generating most TRDs and defining the state-of-the-art.
2. Tabulate, reduce and summarize the results, to evaluate and assess the various methods and processes for application to an automated TRD process, and to create a recommended plan for developing a TRD generation process and a guide for implementing the plan.

The study encompassed the end-to-end generation of TRDs required for five different areas of application: simple digital, complex digital, analog, hybrid, and electro-mechanical. The study also included Unit Under Test (UUT) complexities ranging from System Level to Snop Replaceable Units (SRU).

PROGRAM ACTIVITIES

| <p>The program activities performed to investigate all aspects of TRD generation, automation, current practices and future prospects, and their results were as follows:</p>   |  | <p>Automated TRD Generation</p> |
|--|--|---------------------------------|
| Study Task   | Results/Conclusions  |                                 |
| <p>◦ Survey</p> <p>The survey was conducted using mail, telephone, personal contact and literature search.</p> <p>Investigate Manual Method</p> <p>In this investigation, the manual generation of an analog LRU TRD, requiring 1500 hours to generate, was used as a baseline for comparison with automation methods.</p> | <ul style="list-style-type: none"> <li>- The majority of TRD developers used a digital simulator</li> <li>- Half of the TRD developers use Computer Aided Engineering (CAE) and/or document generators for some portion of the development</li> <li>- 60% were not satisfied with the present development method</li> <li>- 70% did not think TRDs were cost effective</li> <li>- TRDs are needed to enable the AF to obtain bids from TPS developers</li> <li>- TRD automation has progressed rapidly for digital UUTs but little has been accomplished for other types</li> </ul> <p>Summary of Total Testing Requirements</p> <ul style="list-style-type: none"> <li>- 300 hours</li> </ul> <p>Performance Tests</p> <ul style="list-style-type: none"> <li>- 400 hours</li> </ul> <p>Diagnostic Tests</p> <ul style="list-style-type: none"> <li>- 400 hours</li> </ul> <p>Abbreviated Test Language for All Systems (ATLAS) Procedures</p> <ul style="list-style-type: none"> <li>- 200 hours</li> </ul> <p>Quality Assurance Verification</p> <ul style="list-style-type: none"> <li>- 200 hours</li> </ul> <p>Total <u>1500</u> hours</p> |                                 |

| Study Task   | Results   |                                     |  |   |   |                                     |
|--|---|-------------------------------------|--|---|---|-------------------------------------|
| <ul style="list-style-type: none"> <li>◦ Assess the state of the art of TRD automation</li> </ul> <p style="margin-left: 20px;">Areas of automation assessed were in document generation and fault simulation.</p> | <p>Most digital TRDs were developed using Engineering Computer Aids</p> <p>Some analog TRDs for simple circuits use device level simulators</p> <p>Remainder done manually</p>  |                                     |  |   |   |                                     |
| <ul style="list-style-type: none"> <li>◦ Compare TRD aspects in the present, near future, and future</li> </ul>  | <table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 33%; text-align: center;"><u>Present</u></th> <th style="width: 33%; text-align: center;"><u>Near Future</u></th> <th style="width: 33%; text-align: center;"><u>Future</u></th> </tr> </thead> </table>       |                                     |  | <u>Present</u>  | <u>Near Future</u>                              | <u>Future</u>                       |
| <u>Present</u>   | <u>Near Future</u>  | <u>Future</u>                       |  |   |   |                                     |
| <p style="margin-left: 20px;">TRD form</p>   | <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%; text-align: center;">Paper</td> <td style="width: 33%; text-align: center;">Paper</td> <td style="width: 33%; text-align: center;">Electronic</td> </tr> </table>   |                                     |  | Paper   | Paper   | Electronic                          |
| Paper  | Paper   | Electronic                          |  |   |   |                                     |
| <p style="margin-left: 20px;">format (based on MIL-STD-1519)</p>   | <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">Interpretive Standards, No Electronic Compatibility</td> <td style="width: 33%;">Streamlined Standards, Electronic Compatibility</td> <td style="width: 33%;">Standardized Electronic Format</td> </tr> </table> |                                     |  | Interpretive Standards, No Electronic Compatibility           | Streamlined Standards, Electronic Compatibility | Standardized Electronic Format      |
| Interpretive Standards, No Electronic Compatibility  | Streamlined Standards, Electronic Compatibility   | Standardized Electronic Format      |  |   |   |                                     |
| <p style="margin-left: 20px;">Timeline</p>   | <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">After Prototype Development</td> <td style="width: 33%;">Parallel with Prototype Development</td> <td style="width: 33%;">Parallel with Prototype Development</td> </tr> </table>                                |                                     |  | After Prototype Development                                   | Parallel with Prototype Development             | Parallel with Prototype Development |
| After Prototype Development  | Parallel with Prototype Development   | Parallel with Prototype Development |  |   |   |                                     |
| <p style="margin-left: 20px;">Developer</p>  | <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">1) Independent Contractor<br/>2) Logistics<br/>3) Test Engineer</td> <td style="width: 33%;">Designer</td> <td style="width: 33%;">Computer Generated</td> </tr> </table>  |                                     |  | 1) Independent Contractor<br>2) Logistics<br>3) Test Engineer | Designer  | Computer Generated                  |
| 1) Independent Contractor<br>2) Logistics<br>3) Test Engineer  | Designer  | Computer Generated                  |  |   |   |                                     |
| <p style="margin-left: 20px;">CAE/CAD</p>  | <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">Schematic Capture</td> <td style="width: 33%;">UUT &amp; TRD Development</td> <td style="width: 33%;">UUT &amp; TRD Development</td> </tr> </table>  |                                     |  | Schematic Capture   | UUT & TRD Development                           | UUT & TRD Development               |
| Schematic Capture  | UUT & TRD Development   | UUT & TRD Development               |  |   |   |                                     |
| <p style="margin-left: 20px;">Data Transfer Interfaces</p>   | <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">Wire List Transfer</td> <td style="width: 33%;">Schematic/ Drawing/ Document/</td> <td style="width: 33%;">All Data</td> </tr> </table>  |                                     |  | Wire List Transfer  | Schematic/ Drawing/ Document/                   | All Data                            |
| Wire List Transfer   | Schematic/ Drawing/ Document/   | All Data                            |  |   |   |                                     |
| <p style="margin-left: 20px;">Computer Processing Technique</p>  | <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">Simulation/ Designation Generation</td> <td style="width: 33%;">Distributed</td> <td style="width: 33%;">Concurrent</td> </tr> </table>  |                                     |  | Simulation/ Designation Generation                            | Distributed                                     | Concurrent                          |
| Simulation/ Designation Generation   | Distributed   | Concurrent                          |  |   |   |                                     |
| <p style="margin-left: 20px;">Data Bases</p>   | <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">Local</td> <td style="width: 33%;">Company</td> <td style="width: 33%;">National</td> </tr> </table>   |                                     |  | Local   | Company   | National                            |
| Local  | Company   | National                            |  |   |   |                                     |

## SURVEY RESULTS

A literature search was performed as part of this effort and confirmed the findings of the mail, telephone and personal contacts summarized in the previous table.

## MANUAL METHODS INVESTIGATION

Investigation of the Manual Method required analyzing and dividing the method into processes and task had to be defined. The process was defined as a group of tasks which when combined and further divided provide an unique identifiable activity.

A task was defined as an activity by three or less personnel using a specific skill to perform part of one process, reporting to a single functional group (such as Prepare Artwork for Formal TRD Document).

In order to provide a baseline for comparison with an automated process, average time required where determined. The Analog LRU TRD was selected because it was representative of a manually developed average complexity UUT.

## ASSESSMENT OF THE STATE-OF-THE-ART

This task addressed a large number of computer aids (programs and tools), used for the generation of TRD documents. Automation was concentrated in the simulation, and document generation areas. Simulation is the area where duplication is most significant because of the time and resources required. Digital simulation is widely used in the digital area and has made the most advances in the last 10 to 15 years.

Digital fault simulation is performed using the parallel, concurrent and parallel value algorithms. Fault simulators for other UUT types do not exist and are performed manually. The form and content of a TRD using a simulator, and one developed by manual method differs in that TRD developed using a digital simulators requires only a performance flow diagram whereas non-digital TRD developed manually requires a detail flow diagram. The simulator performance and diagnostic outputs are included as a table simplifying the flow diagram.

## COMPARING THE PRESENT, NEAR FUTURE AND FUTURE

The investigation determined methods and the practicality of combining the capabilities into an automated procedure. The survey analysis showed that the TRD, as now defined, does not provide an adequate set of verified data to accurately estimate Test Program Set (TPS) costs. The TRD development cycle is too long, frequently providing data that does not agree with the latest UUT configuration. In addition, the tests specified may not be possible with the selected or available equipment.

To correct these conditions, an investigation of possible automation in the near future was performed, which centered on applying technology now available, such as, simulation programs (HITS, LASAR, etc.), usage of common data bases, document generators (TAD, PAWS, etc), or under development, such as, standardizing ATE, MATE, and analog and hybrid simulators.

The development needed for the future requires considering related activities (TPS development, Failure Mode and Effects Analysis generation, etc.) to ensure that the automated TRD would provide a useful purpose in the future environment, and that the automated techniques investigated would function effectively as part of a larger automated process.

## CONCLUSIONS

|   |                                 |
|---|---------------------------------|
| <p>The conclusions resulting from the program indicate automation is feasible and practical.</p>  | <p>Automated TRD Generation</p> |
| <ul style="list-style-type: none"> <li>◦ Automation is feasible and practical. "Island of automation" exist which can be integrated to provide an automated TRD document generator.</li> <li>◦ Automation is being applied to simple digital fault simulators and specialized document generators.</li> <li>◦ Further development of simulators is required for analog, hybrid and electro-mechanical systems.</li> <li>◦ Incorporating techniques such as Expert Systems (ES), Built-in-Test (BIT), Built-In-Test-Equipment (BITE), and Design for Testability will enhance the automation of TRDs.</li> <li>◦ Improvement in the TRD process hardware/software and new networking techniques, provide diversified capabilities for data gathering, simulation and document generation.</li> <li>◦ Development of TRDs is simplified by good testability design, i.e. MIL-STD-2165.</li> </ul> |                                 |

"Islands of automation" (such as simulators, specialized wordprocessor) do exist which can be interfaced to provide an automated TRD document generator. However, this process can not become completely automated until the fault simulator becomes capable of automatically providing the necessary input stimulus to attain the high percent detection required for a TRD. Techniques such as Design for Testability, Built-In-Test (BIT), Built-In-Test Equipment (BITE) and AI (Artificial Intelligence) - Expert Systems - need to be fully applied before a completely automated process can be attained.



## RECOMMENDATIONS

| The program identified a number of recommendations which will allow progressive development of an automated process.  | Automated TRD Generation |
|---|--------------------------|
| <ul style="list-style-type: none"><li>◦ Modify existing Mil-Specification<ul style="list-style-type: none"><li>- Provide standardized format for types of UUT as appendices to MIL-STD-1519</li><li>- Enhance requirement to include more comprehensive Theory of Operation</li><li>- Requirement for use of MATE test equipment where applicable</li><li>- Provide requirement for executable ATLAS code and ATLAS test flow diagram</li><li>- Define standard interface requirement for ATRDG shell</li><li>- Specify required TRD output format to allow for a standardized non-hard copy output (such as tape, disk, modem, etc.)</li></ul></li><li>◦ Develop and modify TRD hardware/software process<ul style="list-style-type: none"><li>- Interface CAE networks with other resources</li><li>- Provide link to a large variety of commercial and government simulators via global data base networks</li><li>- Develop high-speed main-frame computer and hardware simulators for simulation of large complex circuits</li><li>- Data base routine to access logistics, engineering and contract administration's data bases (CALIS, etc.)</li><li>- Develop software required to achieve the specified interfaces to data base and TRD output</li><li>- Further development of simulators for complex digital, analog, hybrid and electro-mechanical UUTs</li><li>- Define and develop the executive programs to create the ATRDG</li></ul></li><li>◦ Incorporate emerging technology<ul style="list-style-type: none"><li>- Incorporate Expert System techniques into the ATRDG shell and simulation for data management, test strategy, resource selection, automatic pattern generation of analog and digital (sequential) circuits</li></ul></li><li>◦ Further development of simulators<ul style="list-style-type: none"><li>- Improve automatic pattern generator to handle sequential circuits</li><li>- Enhance simulation capability to include complex digital, analog, hybrid and electro-mechanical</li></ul></li></ul> |                          |

The implementation and orderly transition from the present methods to those proposed in this report can be accomplished by modifying the specification as the first step. The specification can be imposed in new contracts, when feasible, by specifying the applicable revision. The recommended changes to the TRD specification are as follows:

1. Require a complete and detailed Theory of Operation.

2. Require use of a Modular Automatic Test Equipment (MATE) library to identify possible ATE configurations.
3. Generate executable MATE ATLAS code.
4. Define a standard electronic TRD file format for incorporation and modification as a part of the TPS.
5. Define TRD development phases.
6. Define interface and output formats.

New computers and CAE stations are evolving rapidly. To ensure automated process development will keep pace with equipment development, new processes should be developed for application on a higher level system. The intent is to transfer the programs to a local system when the capabilities exist at that level. The expanded CAD workstation capabilities are to include the following:

1. Interface with remote data bases.
2. Automatic parallel and distributed processing.
3. Integrated design and TRD activities.
4. Expanded local computer capabilities and memory.
5. Develop standard interfaces to simulators for all types and level of UUTs.
6. Incorporate TRD document generators in the workstation.
7. Integrate an Expert System for data base and TRD activities.

Automated data gathering requires access to source data bases. Access to other system data bases requires development of interfaces, communication standards, data base resident software, and a data access control program.

Among other areas, the use of AI will reduce the number of operator interventions by examining the requirements and selecting the applicable resource for accomplishing the various tasks.

Simulation exists for digital, some level of analog and hybrid. Except for digital simulators, fault analysis required for TRDs does not exist. New developments are needed to expand the simulation capabilities. Work currently under way indicates that possible solutions will come from improvements in the near future. These improvements will occur in the area of functional modeling of complex devices and SRUs, test and hardware simulations, mathematical representations, usage of a testability analysis approach, built-in-test, and higher speed simulators. It is recommended that expansion of Test/Design Simulation software be made as follows:

1. Develop a resident program to choose best available simulator.
2. Develop a standard device library.

3. Provide hierarchical and intertechnology data interfaces.

Due to the evolution of engineering methods, available tools, processing power, and military standards, a program should be established that would standardize and drive requirements, as well as, monitor industry/DoD efforts toward automating the TRD.

## 1. INTRODUCTION AND SUMMARY

The object of this program was to define a program for the Automation of Test Requirement Document (TRD) generation and the incorporation of that capability into the Computer Aided Design (CAD) processes.

Specifically the goals were to:

- Determine how the current high-cost and long development period required for TRD generation could be reduced by automating the process.
- Define methods to expand the CAD process to include TRD generation.
- Define how to apply Expert Systems, a branch of Artificial Intelligence (AI), to the TRD generation process.

### 1.1 BACKGROUND

The TRD is a document containing all technical data required to describe each test to be performed on a Unit Under Test (UUT). Each test requires a minimum of one page, consequently, TRDs with hundreds of pages are common.

The military establishment has not been able to obtain consistent and effective TRDs. The cost is high and continues to increase with the increase in UUT complexities. The cause of this high cost can be attributed to the TRD preparation being manpower intensive.

Though digital simulators have been used for years and the recent introduction of a TRD document generator, such as TRD ATLAS Developer (TAD), Personal ATLAS Workstation (PAWS), etc., has provided a tool to assist in the TRD generation, the process is still very labor intensive. In other UUT types such as analog, hybrid and electro-mechanical, the process is performed manually.

To improve this condition it is necessary to identify the tools available, those in development, and to formulate an implementation plan. That plan will integrate these tools to automate the TRD generation process thus reducing the cost and providing a consistent and effective TRD.

Circuits are now being developed using Computer Aided Engineering (CAE) workstations, personal computers and simulators that are reducing engineering costs and providing convenient tools with applications to some TRD activities.

### 1.2 OVERVIEW

The automatic testing process relies on an interrelated series of elements to produce the desired results. The TRD is the key to transitioning the design into an item with known, verifiable performance.

Figure 1-1 illustrates the relationship of the TRD to other test elements.

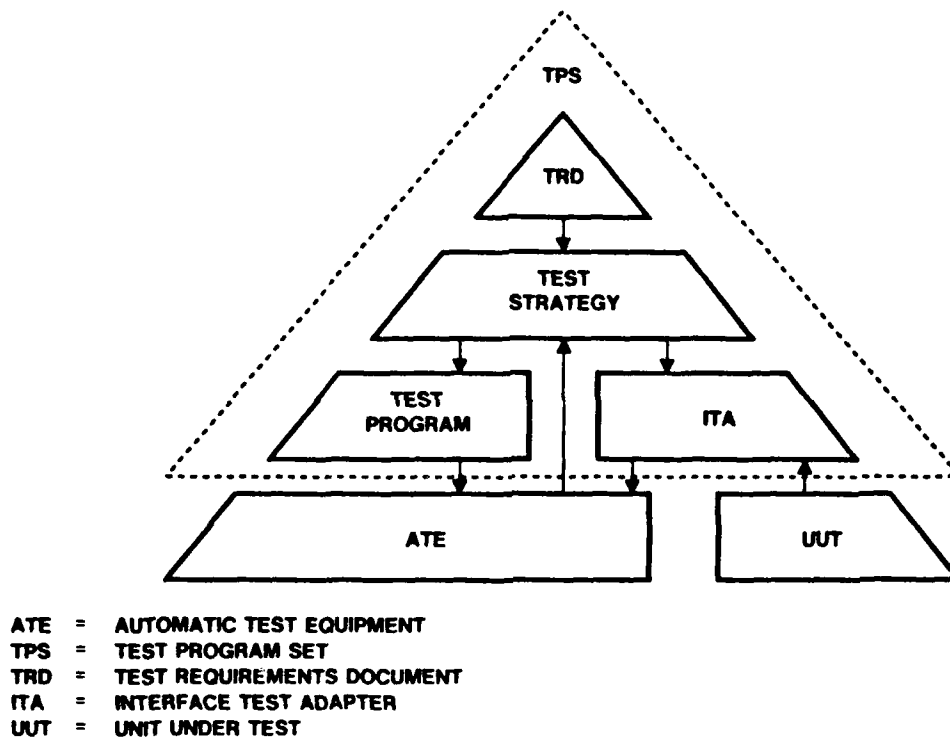


Figure 1-1. ATE/TPS Overview

The Test Program Set (TPS) provides the Test Program and Interface Test Adapter needed to interface a UUT to the Automatic Test Equipment. The requirement for developing these items starts with the TRD, which provides all of the UUT test requirements. The Test Strategy introduces Automatic Test Equipment (ATE) capabilities and optimizes the testing. The Test Program is a software program written in Abbreviated Test Language for All Systems (ATLAS) or Tester Language code, which can be executed by the ATE. The Interface Test Adapter (ITA) provides the electrical and physical interface between the ATE and the UUT.

To study the automation of the TRD development, the process was divided into the activities illustrated in Figure 1-2.

A TRD provides all data needed to perform tests on a UUT using ATE. Data (documents, drawings, schematics, wire lists, parts lists, etc.) must be obtained from a variety of sources which includes: Contracts, Design, Equipment Manufacturers, Test and the customer. Once accumulated, information relating to operation, functional, and fault tests must be identified and formatted into the TRD description pages. Functional test sequences, stimuli, and connection requirements are developed and checked, using some form of simulation. Once a functional test is defined, it will verify the operation of the UUT; faults are inserted into the simulation, and fault detection and

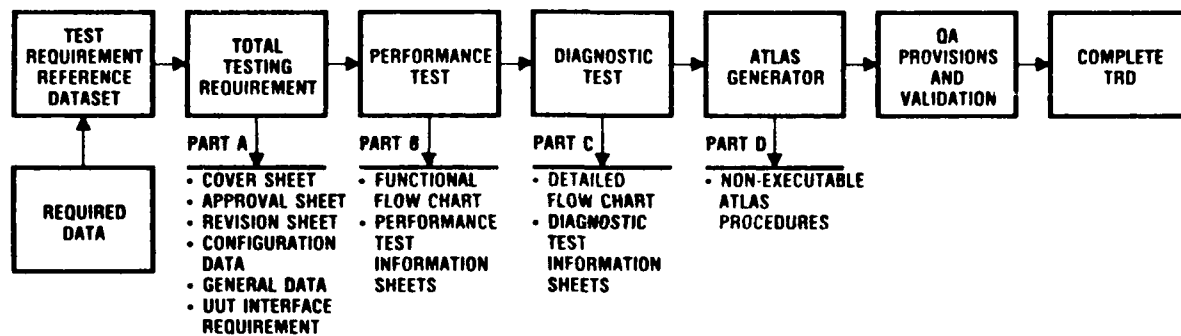


Figure 1-2. Simplified Flow Chart

Isolation tests are developed. Functional and fault test development are iterative processes. Its function is to develop an efficient test procedure to minimize test time, simplify test procedures and to minimize the test equipment needed. The defined tests must be converted into ATLAS code for eventual use on a selected ATE.

The program was organized as shown in Figure 1-3.

#### SURVEY ACTIVITIES

A number of survey analysis were conducted:

Pre-contract - Conducted to establish Rockwell in-house capabilities and tools.

Mail Survey - After contract award, 200 questionnaires were mailed to obtain data from all segments of the industry. Responses provided data that when correlated with the literature search established the industries' state-of-the-art.

Telephone Survey - Conducted to supplement mail responses and to obtain individual opinions.

Personal Contact - Discussions were held with Daisy, Teradyne, Grumman, Bob Cote Consultant, Navy, Harris, Systec and Army which provided a mix of TRD users, tool developers, TRD managers, and TRD developers. The purpose was to obtain specific information concerning techniques, plans and concerns.

Literature Search - Researched 575 articles related to TRDs, computers, workstations, software, techniques and evaluations. The literature

confirmed survey findings and provided a basis for evaluations, assessments, investigation and recommendations.

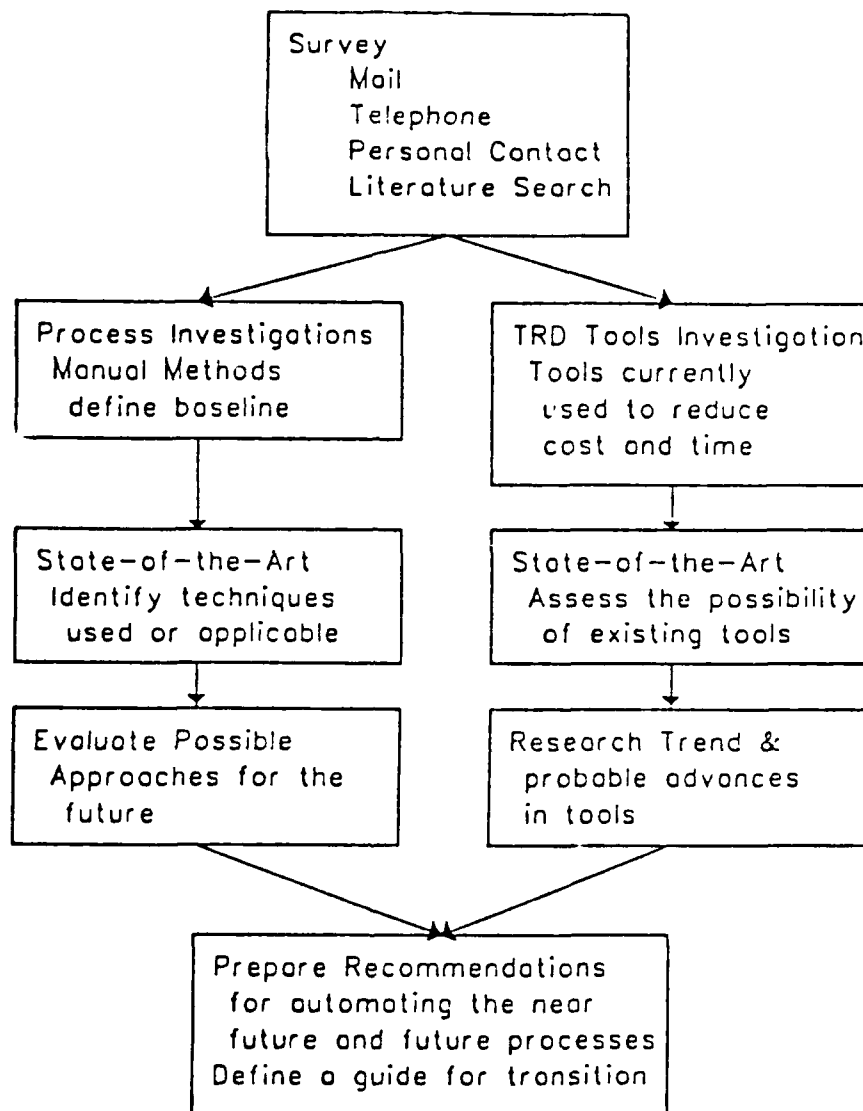


Figure 1-3. TRD Automation Study Plan

Process Investigation - A baseline of the manual method process was established and was used to evaluate possible areas of automation. The Analog LRU TRD was selected because it was representative of a manually developed average complexity UUT. Methodology and time required for the manual method is described in detail under paragraph 2.2.2. The major elements within the manual method process and time required for each are listed in Table 1-1.

Table 1-1. TRD Generation Steps Defined For Manual Method

Part A - Summary of Total Testing Requirements

|                       |    |
|-----------------------|----|
| Develop Contract Plan | 24 |
| Gather Related Data   | 28 |
| Theory of Operation   | 40 |
| Physical Description  | 8  |
| Electrical Interface  | 60 |
| Mechanical Interface  | 8  |
| Special Equipment     | 8  |
| Special Tool          | 8  |
| Test Data             | 50 |
| Boiler Plate          | 4  |

Part B - Performance Tests and Part C - Diagnostic Tests

|                             |     |
|-----------------------------|-----|
| Test Design                 | 200 |
| Test and Isolation Strategy | 400 |
| Detailed Test Requirement   | 202 |

Part D - ATLAS Procedures

|              |     |
|--------------|-----|
| Create ATLAS | 200 |
|--------------|-----|

Quality Assurance Verification

|               |            |
|---------------|------------|
| QA Provisions | 40         |
| QA Validation | <u>160</u> |

|            |      |
|------------|------|
| Total Time | 1500 |
|------------|------|

Tool Evaluation - All tools identified in the analysis were categorized and evaluated for application to TRD generation. Data base listings and matrices were prepared to expedite the evaluation. Tools are divided into categories according to type UUT.

State-of-the-Art Efforts Identified and Assess the Processes and Tools Available - Areas requiring development, possible combinations of capabilities and application of similar techniques were assessed to arrive at the current, near future and future techniques for TRD development. By evaluating the information provided by TRD and tool development the current state plus the near future advances were defined for each level and type UUT.



### 1.3 SUMMARY

There are islands of automation for the simple digital UUT that if integrated can provide an automated TRD generator.

The use of a networked system containing a large variety of hardware will enable a CAE workstation to utilize network capabilities. Automation of TRD generation for all types and levels of UUT is limited by the on net capabilities and the ability to interface the various software programs needed for TRD generation.

Some specific results are listed as follows:

- TRDs are generated manually except for simple digital UUTs.
- TRD document generators are now available such as TRD Atlas Development (TAD) and Personal Atlas Workstation (PAWS). Tools of this type can be integrated into an automated TRD generator.
- Numerous digital fault simulators have been identified. Great progress and improvements have been made in the digital simulator with the introduction of parallel, concurrent and parallel value list algorithms.
- To handle Very Large Scale Integration (VLSI) chips, functional modelling and hardware modelling has been introduced. Modelling language such as Register Transfer Language and Hardware Description Language has made modelling of complex chips feasible.
- Analog fault simulators do not exist although simulators such as Simulation Program with Integrated Circuit Emphasis (SPICE) and System Circuit Analysis Program (SYSCAP) can be used. These programs do not have an automated fault simulation capability making it very expensive and time consuming to run. Further investigation in this area is warranted to develop an efficient fault simulator that can be implemented in an automated TRD process.
- Hybrid simulators do not exist. Until an efficient analog simulator is developed the UUT of this type needs to be partitioned and simulated independently.
- E-M simulators do not exist. Very few companies are involved in the generation of this type TRDs. This area requires further study to determine if developing a simulator will be cost effective since no information were available in the survey analysis.
- The incorporation of Expert Systems, a branch of Artificial Intelligence, can be made in the following areas:
  - Automatic pattern generator of the fault simulator
  - Test and fault isolation strategy
  - Minimize operator intervention

The recommendation for developing an automated TRD generator on a CAE station was divided into three areas of activity:

- MIL Specification change
  - Needed to eliminate duplication
  - Better define TRD roles and uses
  - Define an electronic standard format for the TRD

Application of new hardware

- To expand simulation capabilities
- Allow access to information resident in Engineering, Reliability, Logistics and Contract data bases
- Optimize the selection and utilization of networked hardware

Develop techniques and software

- Which will utilize the capabilities of available commercial and government software
- Operate with minimum operator intervention
- Provide the designer with a TRD early in the design cycle.

## 2. DATA GATHERING

The contract period and tasks tend to naturally fall into two phases. Phase I is that effort associated with collecting all the necessary data, while Phase II is the analysis and evaluation of this data to develop the recommendation. Some data gathering and survey update activities were performed in Phase II to ensure that the study data is as current as possible at the conclusion of the contract.

### 2.1 SURVEY

The survey analysis phase provided an industry wide base from which to evaluate and assess all aspects of TRD generation and automation. CAD/CAE systems were also reviewed to provide data needed to determine the feasibility of automating TRD activities on a CAD workstation. The survey effort was conducted by: 1) Identifying personnel willing to participate in a mail survey, develop and distribute the survey forms, categorize the responses and enter the data in the data base survey analysis files. 2) Conducting a telephone survey of people willing to respond to the mail survey, who failed to complete the survey forms in two months, and 3) Conducting an interview of people identified as providing significant contributions to the mail and telephone surveys.

#### 2.1.1 Pre-Contract

Prior to award of this contract, Rockwell had identified a need to improve in-house TRD and TPS capabilities and had initiated a study. The results of the Rockwell study indicated the need for a data management program to accumulate and aid in the evaluation of the large quantities of data which would be gathered. To provide this capability, a number of commercial data base programs were evaluated, and a program selected. This program, hosted on an IBM-XT, provided data manager, wordprocessor, communications, and a spreadsheet with graphics. This program was well suited to this effort because of its ability to handle large data files and project processing features. A project processing routine was written to store and tabulate the results.

The selection of this program provided an experience base which was directly applicable to the Automated Test Requirement Document Generation (ATRDG) contract. Rockwell purchased software was used to support this contract. This integrated software package was used to: store in-house analysis data, prepare reports and status IR&D efforts.

As a part of this task, a Rockwell wide survey analysis was conducted to gather information needed to determine what improvements in TRD computer tools would be economical and beneficial to the Air Force.

The TRD portion of the study initially surveyed several divisions of Rockwell to get an accurate status of the corporation technology, tools, processes, and methods currently in use.

A questionnaire was prepared by Autonetics Strategic Systems Division (ASSD) engineering and logistics personnel, which was based on the experience and knowledge developed on the Air Force Satellite Communication (AFSATCOM), Space Shuttle, Peacekeeper and other programs. The original purpose of the questionnaire was to provide the engineering simulator development group with information needed to determine what improvements in TRD computer tools would be economical and beneficial to the Rockwell.

The analysis was conducted by internal mail with telephone contact being used to clarify questions and for follow-up.

The conclusion and recommendations which resulted, were never published due to the termination of the task upon receipt of the ATRDG contract. The data is summarized in Table 2-1 and was combined with contract analysis data for analysis.

The study provided experience in data gathering techniques, how to format questions, how to use the data base, and how Rockwell was currently generating TRDs. The application of tools and types of problems provided an excellent base for this study. The high percentage of forms returned tended to indicate that surveys were an excellent means of obtaining data.

Full advantage was taken of the diversity of activities and approaches used by various divisions of Rockwell. The in-house analysis influenced the selection of questions to be addressed in the contract survey.

Responses to most questions did not indicate specific areas needing immediate improvement. The most frequently mentioned items are listed in Table 2-1, and indicate a sequence for developing improved capabilities.

The survey results indicate that Rockwell uses manual methods for most activities associated with TRD generation. The areas requiring improvements are: expanded digital capabilities with well documented users manuals, better pattern generation, a wider range of models with more user defined parameters. The fault analysis features developed for engineering purposes are in excess of those needed, and should be de-emphasized in favor of improved run time and fault isolation. CAD and document generation and data base features are needed to reduce manual efforts involved. TRDs were developed on a multitude of major weapon systems, thus providing a well-rounded understanding of the TRD development process.

Table 2-1. In-House Survey Results

| Activity   | Summary of Results   |
|--|--|
| I Data Base  | 98% of the activity done manually  |
| II Test Requirement Document Interface Description | 52% manually documented - remainder done with Data Base or Wordprocessor Programs  |
| III Flow Charts                                    | 60% hand drawn - remainder use some type drawing tool such as CAD  |
| IV Test Data Sheet                                 | 50% generated by hand  |
| V Automated Test Program Generation (ATPG)         | 80% use some type of simulator or pattern generator, all agree that ATPG saved time. 44% have used more than one ATPG/Simulator  |
| VI ATPG Features                                   | <ul style="list-style-type: none"> <li>A - General <ul style="list-style-type: none"> <li>Digital Capabilities</li> <li>Well Documented Users Manual</li> <li>Shared Data Base</li> </ul> </li> <li>B - Model Data <ul style="list-style-type: none"> <li>Large Transistor-Transistor-Logic (TTL) Library</li> <li>Functional and Data Bus Variable Model Parameters</li> </ul> </li> <li>C - Pattern Generator <ul style="list-style-type: none"> <li>Digital Patterns</li> </ul> </li> <li>D - Fault Analysis <ul style="list-style-type: none"> <li>Fault Detection</li> <li>Concurrent</li> <li>Three-State Fault Detector</li> <li>Analog High-Rail and Low-Rail Faults</li> </ul> </li> <li>E - Run Features <ul style="list-style-type: none"> <li>Circuit Connection Analysis</li> <li>Fault Collapse and Back Trace</li> <li>Restart</li> </ul> </li> <li>F - Output <ul style="list-style-type: none"> <li>Data Transfer</li> <li>CAD Interface</li> <li>Automatic TRD Page Generation</li> <li>Replacement Sequence</li> <li>Determination</li> </ul> </li> </ul> <p>Items of little interest included:</p> <ul style="list-style-type: none"> <li>Analog Node Short Capabilities</li> <li>Monte Carlo fault pattern and fault capabilities</li> <li>Power Supply ON/OFF</li> <li>Automatic node naming</li> <li>Transportability</li> <li>Tester and ATLAS Interfaces</li> </ul> |

### 2.1.2 Mail Survey

The mail survey included identifying people to contact, determining what questions to include in the questionnaire, organizing the resulting data and determining what follow-up was appropriate.

The initial contact lists were developed by obtaining lists of people who had attended conferences and meetings on topics which relate to TRD generation. These meetings included lists of Modular Automatic Test Equipment (MATE) TPS Standing Committee, NSIA (National Security Industrial Association) Integrated Diagnostics Working Group, JLC-NSIA, Automatic Testing Committee, and TISSS (Tester Independent Software Support System) Committee listings.

Telephone contacts, preceding the mail survey analysis, provided:

1. A method of accurately determining who was involved in TRD activity
2. Who was able and wanted to contribute data
3. Who should be considered for personal contact (trip).

The main points established during the phone conversation, were which of the questionnaires the person contacted was interested in responding.

The initial list of 500 was reduced to a mailing list of approximately 200 by the preliminary telephone screening.

The mail questionnaire was developed using the in-house questionnaire, the contract statement of work and comments received from experienced people in the field. The number of questions was felt to be excessive, due to the variety of disciplines and the range of UUTs; therefore, the questions were divided into groups relating to specific TRD activities. This resulted in a number of short forms which were sent to people expressing an interest in that particular TRD activity.

Mail Survey Form Development - Under the heading of Considerations, the various elements in Figure 2-1 reflect factors used to finalize the survey analysis forms. These considerations were divided into two major pieces of the survey. One was intended to collect data regarding present techniques, while the other was directed towards the use of tools in generating the TRDs.

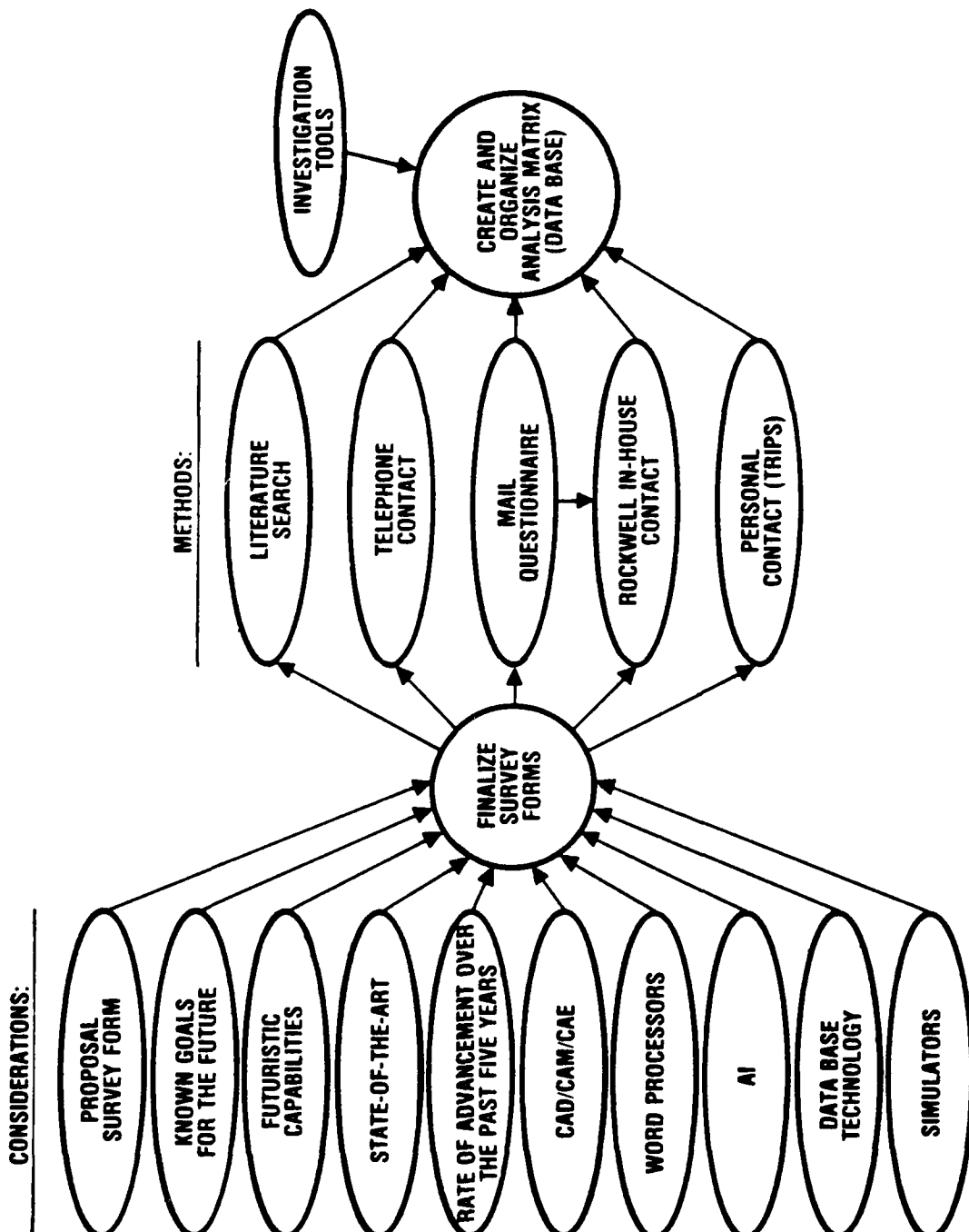


Figure 2-1. Survey Flow Chart

Information requested or that which could be derived from the analysis included:

- Role played by the TRD in the development cycle. Determine if all sections of the TRD were being developed, and how they interface with CAD, TPS and ATE.
- Historic (why that method was selected). Determine if the method used was related to existing computer capability, previous use, commercially available tools or other reasons not related to effectiveness.
- Current methods and resources used.
- Planned or in-work changes to the existing methods. Improvements considered.
- Step variations due to type of UUT. Variations in TRD caused by different types of UUT (System, Line Replaceable Unit (LRU), Shop Replaceable Unit (SRU), etc.).
- ATPG and simulators currently used. Such as LOGOS, Logic Automated Stimulus and Response (LASAR), Hierarchical Integrated Test Simulator (HITS), In-house, etc.
- Experiences with other simulators. Determine if preference was based on a wide base of experience.
- Are present techniques suitable for automation. Determine if any attempt has been made to modify the TRD generator.
- Projected methods of accomplishing the task in five years.
- Long-term projection for accomplishing the task.
- If manual generation was used - what skill-level and algorithms were required and how long did it take to complete?
- Effects of MATE, ATLAS, ADA or ATE configurations on TRDs.

A set of forms were developed which divided the activity into the following categories:

- TRD Developer
- TOOL Developer
- User
- Management
- Engineering



A further division was made to reduce the size of each questionnaire by dividing each of the above categories into:

- Digital Small
- Digital Large
- Hybrid
- Analog
- Electro-mechanical

This was done since most of the survey recipients contacted in the original telephone contact indicated they specialized in some aspect of the TRD activity. It was now possible to develop a questionnaire which was more concise, and addressed the specific portion of TRD development the recipient was involved in.

The ten percent (20 of 200) response was surprisingly low, considering the screening which had been accomplished with the initial phone contact.

The second round of follow-up telephone calls gave the following results:

- |                  |  |
|------------------|--|
| 30 out<br>of 100 | Still intended to respond but had not found the time. Most noted that completing this type effort had a low priority, and their workload was high.           |
| 70 out<br>of 100 | Never received the forms (lost in the mail).   |
| 6 out<br>of 100  | Did not feel they were involved or qualified in the activity addressed in the survey analysis.   |
| 9 out<br>of 100  | Declined because of the request to release data, and either considered the information requested proprietary, or would not state why they would not respond. |

An additional two mail responses were received as a result of the phone calls. The data received was not sufficient to allow statistical evaluation, but it did provide an indication of the state-of-the-art and concerns of companies involved. The data was tabulated and entered into the data base.

The mail survey analysis was intended to produce information related to key questions which could be categorized and sorted.

Table 2-2. Mail Survey Responses

| Evaluation Category                                      | No. Responding |
|--|----------------|
| A USER   |                |
| 1 TRD User   | 7              |
| 2 TRD Developer  | 7              |
| 3 Tool Developer   | 4              |
| 4 Manager  | 2              |
| 5 UUT Engineer (Test Points, etc)                        | 0              |
| B UUT TYPE   |                |
| 1 Electro-mechanical                                     | 6              |
| 2 Hybrid   | 9              |
| 3 Analog   | 10             |
| 4 Digital - Small  | 7              |
| 5 Digital - Complex                                      | 8              |
| C TIME   |                |
| 1 Current  | 20             |
| 2 Next Five Years  | 1              |
| 3 Distant Future   | 0              |
| 4 Past   | 0              |
| D TYPE EFFORT  |                |
| 1 TRD Task (Manual Methods) Contains Series of Processes | 15             |
| 2 TRD Process (State-of-The-Art)                         | 3              |
| 3 TRD Automation   | 5              |
| E AUTOMATION APPLICABILITY                               |                |
| 1 CAD/CAM  | 1              |
| 2 AI   | 0              |
| 3 Data Base  | 0              |
| 4 LAN  | 1              |
| 5 Simulation   | 6              |
| 6 Hand   | 5              |
| 7 PC System  | 3              |
| 8 Wordprocessor  | 1              |
| F RESPONSE   |                |
| 1 Declined   | 4              |
| 2 Product For Sale (Tools, Computers, Software, Testers) | 2              |
| 3 Service For Sale (TRDs, TPSS, UUT Support)             | 5              |
| 4 Military   | 5              |
| 5 Commercial   | 0              |
| 6 Aerospace  | 6              |
| G APPLICABILITY TO CONTRACT                              |                |
| 1 High   | 10             |
| 2 Partial  | 6              |
| 3 None   | 6              |

### 2.1.3 Telephone

A telephone survey was conducted of people still interested in responding. A short questionnaire was developed, and 30 people were contacted. Ten of those contacted responded to the questions. In general, the results indicated that most people used some computer tools but still classified their activity as manual. They all felt additional automation was possible and needed. The results are summarized below:

1. Most people were involved with all types of TRDs except Electro-mechanical.
2. The majority used circuit simulators with about half using CAE and Document Writers.
3. Sixty percent were not satisfied with their present techniques.
4. Seventy percent did not think TRDs were cost effective.
5. An average of eighty percent categorized their methods as manual.
6. Half thought TRDs would be eliminated in the future.
7. Sixty percent thought software tools were available commercially.
8. About sixty percent used manual methods and simulators for testability analysis.

### 2.1.4 Survey Visit (Trip)

The survey trip provided an informal contact with key people active in TRD related activities. The selection of people contacted was influenced by the following factors:

1. Ability to provide significant information relating to the technology, future plans and TRD automation
2. Geographically located in close proximity to other companies participating in TRD activities.
3. Availability and willingness to spend a half day discussing their activities.

The following organizations and individuals were contacted during the trip:

Daisy Systems Corp., Los Angeles, CA  
Teradyne Inc., Boston MA  
Grumman Aerospace Corp., Bethpage NY;  
Robert Cote Consultant, Franklin Lakes, NY;  
NAVAIRENGCEN, Lakehurst, NJ;  
System Corp., Stony Brook, NY;  
Harris Corp., Winter Park, FL;  
HHB Systems Inc., Mahwah, NJ;  
PM-IPS Fort Monmouth, NJ

Those contacted performed TRD activities in the following categories:

- TRD developers
- TRD users
- Tool developers
- TRD managers

The general format of meetings was:

- 1) A brief description of the purpose for the meeting.
- 2) A discussion on the visatee's involvement in the TRD activity.

In summary, the information gathered during the trip reflects the following concerns and suggestions:

1. TRD is needed to allow TPSs to be bid competitively.
2. TRDs accuracy and means of verification must be improved.
3. TRDs are expensive and frequently impose requirement need for design tests on the TPS developer and user.
4. TRDs should be developed as a guide, finalized and formally released after the TPS is completed.
5. UUT developers should be responsible to contract or develop the TPS; thus, eliminating the dispute over who is responsible for errors.
6. The division of TRD/TPS content should be on a sliding scale depending upon the type of UUT and ATE.
7. TRDs in their present form can be eliminated in an automated system.
8. HITS may not be able to keep up with the growth of commercial simulators such as LASAR 6 and Computer-Aided Design And Test (CADAT), due to amount of funding available to support much development.
9. TRD and TPS development contents overlap, and TPS developers prefer to get data directly from UUT specifications or design data to ensure information is current.
10. Automation of TRD has progressed to the point of developing a digital TRD from a single workstation, however, little work has been done in the analog or electro-mechanical (EM) areas.

The results of these contacts illustrated the wide variety of needs and thoughts as to what functions the TRD should play, and how it could be used effectively.

### 2.1.5 Literature Search

Published information was easy to obtain and provided more detail, current data, and future capabilities, for the time spent than any other survey method. The literature search included TRD activities, computer tools which could apply to TRDs and CAD systems. All information is categorized by applicable TRD task, application, time availability, for that activity. Summaries and matrices were developed and provide rapid access to specific data used for conclusions and recommendations.

Approximately 575 articles (Conference papers, sales literature, technical reviews, and journals), were reviewed, categorized, and evaluated. The articles selected discussed one of the following topics:

- TRDs
- CAE/CAD
- Digital Simulation
- Analog Simulation
- Hybrid Simulation
- Electro-mechanical Analysis
- TPS Generation
- Data Base
- Communication-Data
- Computers with potential application for TRD development
- Testability
- ATE

No maximum quantity of articles was established.

Information concerning historic advancement over the past five years has been obtained primarily from the literature search. The TRD activity is quite dynamic, and since many engineers involved today were not involved five years ago, comparing articles, written during the period, has provided a base for this determination.

The maturity of digital circuit development has resulted in an abundance of papers discussing the various methods for automating the simulation, testability analysis, test generation and TRD development. Some automation exists for the activities listed in the manual method. The major concerns are how to tie the different tools together, how to provide a single economical host, define a point for human intervention and input, how to reduce computer run times, how to expand the capabilities to complex digital circuits, and how to interface with analog, E-M and other disciplines.

Few articles were obtained on analog circuitry. The analog area is still generally restricted to the use of a simulator program, such as SPICE, which is not readily adaptable to fault simulation. No articles, of any significance relating to E-M were found.

The articles were summarized and categorized as follows:

Categories A thru G (Table 2-2) from the Mail Survey analysis were used to ensure commonality of data gathered. Table 2-3, Categories H thru K were added to provide additional information concerning the literature.

The conclusions derived from the Literature Search were:

1. Testability analysis and some digital simulation are already being accomplished on CAD/CAE workstations.
2. TRDs are being generated with computer programs specifically designed for that purpose but generally have not been integrated with the simulation efforts.

Table 2-3. Additional Literature Sort Categories  
[Extension of Table 2-2]

| Evaluation Category                                       | No. Responding |
|---|----------------|
| H DATA INPUT  |                |
| 1 CAD/CAE   |                |
| 2 Manual  |                |
| 3 Communication   |                |
| 4 Built-In-Test (BIT)/Built-In-Test-Equipment (BITE) Data |                |
| 5 Feedback  |                |
| 6 Foreign Data Source                                     |                |
| I TRD OUTPUT  |                |
| 1 Wordprocessor   |                |
| 2 Graphic   |                |
| 3 Data Base   |                |
| J SIMULATOR   |                |
| 1 Digital   |                |
| 2 Analog  |                |
| 3 Hybrid  |                |
| 4 Electro-mechanical                                      |                |
| 5 AI Tool for Test Program Generation (TPG)               |                |
| 6 AI Tool for Fault Analysis                              |                |
| K LEVEL   |                |
| 1 System  |                |
| 2 LRU   |                |
| 3 SRU   |                |

3. Digital simulation is widely used and mature, Analog simulation is less mature and primarily supports low complexity devices. Hybrid is a combination of digital and analog with several possible integration approaches. Electro-mechanical simulation data is practically nonexistent. The CAD capabilities for development, rotation, and interference evaluation coupled with an analog simulator appears to be feasible.

4. Rapidly expanding computer, data base systems, communication links and special purpose hardware will provide a rapid access to data, allow for optimized parallel process and sharing of resources which is essential in the development of an efficient automated TRD generator.
5. Expert Systems, a branch of Artificial Intelligence, will be applicable to minimize operator decisions, optimize equipment specifications, select test sequences and for similar tasks when rule and procedures have been established.

All collected data were placed in a data bank using the following format:

#### LITERATURE

|           |  |
|-----------|--|
| L Ref No. | Literature sequence number used as a reference |
| Title     | Title of article                               |
| Author    | Name of author                                 |
| Date      | Date of publication                            |
| Ref Doc   | Reference documentation                        |
| Eva Cat.  | Code classifying article for sorting           |

Appendix B contains a complete listing of the literature gathered and reviewed

#### 2.1.6 Summary of Surveyed Data

##### CAD/CAE Workstation

CAD/CAE Workstation such as MENTOR, VALID and DAISY expanded to interface and include: TRD development, graphics, data bases, network access and the required software are necessary to implement an effective design/ATRDG station. By providing access to data resident on other systems the local workstation acquires the capability of the entire system. Interface standards will minimize the number and types of software programs required. Networked resources allow for parallel solutions on the best suited resource available for test and design simulation. The following workstations were included in the investigation:

Daisy  
Valid  
Auto-trol  
Mentor  
Calma  
Tektronix  
HP

## Testability

Testability analysis programs are available on many CAE stations and provide estimates of testability and tools for improving the testability of the UUT design. Testability programs provide a method for analyzing all types and level circuits rapidly. The techniques currently used in the fault analysis portions of simulators lack the ability to model all types and levels of UUTs and they are comparatively slow. New developments in the Testability analysis approach may provide an acceptable means of fault simulation. The main issues are; accuracy, test pattern or signal generation, timing and fault analysis.

Testability Analyzers generally provides test point selection capability to improvements the testability of the circuit being designed.

There are numerous programs on the market based on the Sandia Controllability/Observability Analysis Program (SCOAP), such as COPTR, DTA, STAMP, etc(Calma), which measures controllability and observability by examining each node on a circuit. Others such as LOGMOD is based on Logic Model which uses cause and effect of the device or devices to measure the testability of a circuit.

The Marlett's algorithm (HHB Systems) is a modified D-Algorithm for the generation of test vectors for logic circuits, uses Controllability and Observability data for the selection of path and output pin for a given fault.

The following articles in Appendix A relates to Testability:

55, 151, 152, 153, 154, 304, 410, 423, 429, 433, 437, 460,  
523, 527, 545, 560, 575

## Simulator

Simulators are needed to support each type and level of UUT included in the contract. System level and large circuit simulators do not provide detail node information, and are most useful for design. Additional development in the area of developing test signals, and fault analysis techniques for this type simulation is required, if TRDs at this level are to be produced automatically. Mathematical analysis approaches usually deal with the functional performance of the UUT, and do not always relate to a specific circuit node operation.

The application of simulator will vary depending upon UUT types and levels. Currently hot mock-up, and hand analysis techniques are used for most simulations except for digital and simple analog.



The simulator, used in Part B and C of the TRD, effort involves the development of model of the UUT. The following steps are performed to create the circuit model if computer simulation is employed.

- o Verify that models exist for all the components in the UUT. Models will have to be generated for those UUT components that have not been modeled before.
- o Use CAE schematic capture capabilities, or create the UUT model by: a) Assign numbers to all nodes (component junctions) or use wire list inputs. b) Assign reference designators (i.e. Q1, Q2, R1, ...) to component models. c) Code the UUT model by typing reference designators together using the node number.
- o The UUT model is then entered into the computer via keyboard, punch card, or magnetic tape or CAE.

### Digital

Numerous digital simulators are available and utilized in the industry and by the military: they are effective on small to medium scale IC and have problems with complex circuits, microprocessors, memories, and other complex devices. Many of these devices require a large and varying number of clock cycles to produce recognizable outputs; thus, complicating program generation. The ATPGs used today are being applied successfully to simple digital circuitry of less than 100,000 nodes.

Many of these simulators are commercially available and are used to generate the required data for TRDs. They include; LASAR, LOGOS, CAPS, TESTAIDS, etc.

The design use of simulator varies but include logic simulation, functional evaluation, timing verification, worst case timing, stress analysis, fault and testability analysis, test point selection, design verification, and simulation/brass board tradeoff

Accurate simulation must consider the UUT types, since the same function developed say in TTL will have different characteristics then the same function in a CMOS device (example: a floating input to a one-input AND gate will produce a high output in TTL but in CMOS the output state is unknown).

### IC Modeling

Most simulator provide model such as primitive, macro and functional. These are software models that performs the same operation that the device being modeled exhibits. Some simulators (Daisy, LASAR6, etc) provide the capability of using a hardware model which uses the actual device being used in the circuit to simulate their operation; due to the differences in operating speed (device being real time and the simulation being much slower) a shell is developed (containing hardware and software), which satisfies the input/output requirements of the device.

Hardware modeling, which uses the actual device as models, must operate at real time rates much faster than the software simulation rate. To provide data to the hardware model and to use the model outputs an interface shell is built around the hardware device to allow the device to start when all input data is available. When the data is available the interface (shell) conditions, clocks and controls the device and runs the device at real time rate. The resulting outputs are stored to be provide to the software when needed. This procedure may require a high initial model development cost but offers the advantage of simulating all possible input conditions including those not normally encountered or included in a software model. This technique avoids the dilemma of having to model complex IC such as microprocessor which is not fully documented and some features considered proprietary preventing a complete software model development.

### Good Circuit Simulation

As circuits become large, simulation run times and computer memory requirements become prohibitive. To allow for a large and complex circuit analysis, gates are grouped together to form functional blocks. The functional blocks can be modeled considering input and output, simplifying the model, decreasing simulation run time and amount of data generated; thus, extending the application of the simulator.

To allow users to model devices most simulators use a hardware description language or register transfer language to simplify development of models. Since much of the information required is repetitive, the device model can be developed using computer generated software. Standardization of Hardware Description Languages (HDL) has been underway for Very High Scale Integrated Circuits (VHSIC) design and CAE model development.

Program such as HITS provides a hierarchical multi-level simulation which allow the mixed models, and model swapping. This technique will allow to simulate large and complex circuit in stages by swapping all or part of the models in the circuit extending the capability of the simulator.

Propagation delay of device use unit-delay or multiple of the unit-delay or zero-delay. In the unit-delay simulation all gates have the same unit-delay or multiple of that delay, whereas, in zero-delay the gates are handled as an ideal switching element.

Most common states in a digital simulation are 1, 0, HIZ and unknown. Additional states include drive levels, rise and fall states. The drive levels are significant for situations of drive/bus contention, attenuation considerations and high impedance determination. Numerous simulators have larger number of states but are transparent to the user.

Majority of the simulators use static simulation which applies one pattern to a digital circuit, then exercizes the circuit until all node have reached a stable state, then the data is outputted. There are circuits where it is not feasible to disable a clock line requiring a dynamic simulator which applies clock pulses and patterns to the circuit at a simulation rate equal to the operational rate. The fault signature is readily available and stored in a matrix for a static simulation but is not easily done for a dynamic simulation. Until a more efficient method of storing dynamic simulation fault signature is developed static simulation will be the prevalent method.

## Fault Simulation

Fault simulation is a very computer intensive task, consequently time consuming and expensive. The computational efficiency of the simulator is dictated by fault analysis technique, fault collapsing, and fault selection capabilities.

Fault analyzers contained in simulation programs are based on faulting nodes to specified states (most commonly 1 and 0), and exercising the UUT until an identifiable fault signature has been obtained. Fault isolation and detection calculation are made from the results obtained during the circuit simulation. Time required to run large boards is high, and require, skilled engineers intervention to attain adequate results.

The most common fault analysis technique used is the concurrent simulation which determines fault detection by propagation of a super fault lists during a single pass simulation. Other techniques such as parallel, concurrent/parallel (Parallel Value List), deductive and serial are used. The Serial technique is not used for any of the sophisticated simulator since it is a very slow.

All commercially available simulator provides fault collapsing to reduce the number of faults which must be simulated by a factor of two or greater. This feature is very valuable in reducing the simulation cost.

Another cost saving feature is fault selection to allow the user to selectively run fault and to determine how far the faulty behavior propagates to the output. Without this feature the user will need to analyze it's fault propagation manually. Most all simulators provide this capability.

## Vector Generation

Patterns used for digital circuits are derived in a variety of ways: mockup tests, pattern generators, which work well for combinational circuits, engineering acceptance test patterns, by hand or mathematically driven. Patterns are required for digital and hybrid UUTs to determine if the UUT is functional and to identify and isolate faults.

Various algorithms are currently in use. Most start with a random pattern on data lines and specified states on address and control lines. Subsequent states are derived using an algorithm or by monitoring output state changes. Ineffective patterns are discarded and unchanged and uncontrollable nodes are reported.

Test vector generation strategies used to develop test patterns varies from simulator to simulator. The following strategies are being used:

- Path Sensitization (D Algorithm)
- Heuristics
- Random
- Equation Generation
- Mix-Manual Automatic
- Marlett's Algorithm (Modified D Algorithm)

The most common strategy is the path sensitization technique but this algorithm is very efficient with combinational circuit and has difficulty with sequential circuit. Recently, technique to handle sequential circuits have been introduced such as the Marlett's Algorithm which is a modified D Algorithm and the HITEST program by General Radio which uses expert system in the derivation of the vectors. This area needs further investigation and is a potential area for research and development.

The following articles in Appendix A relate to Logic Simulators:

8, 53, 54, 70, 71, 74, 162, 164, 171, 173, 213, 285, 289, 296, 313, 315, 318, 323, 325, 388, 390, 412, 426, 545, 557, 559, 561, 570

The following articles in Appendix A relate to Fault Simulation:

6, 10, 53, 54, 70, 74, 93, 136, 162, 170, 171, 176, 273, 296, 318, 342, 351, 352, 366, 412, 417, 418, 426

#### Analog

An analog type format is required because digital models consider states, and are not sufficiently detailed to allow application to other types of UUTs. SPICE and SYSCAP have been used for years to simulate circuits at the transistor level, these programs are being applied to higher level circuits by developing functional models to replace the transistor models. This type model has limitations because of the difficulties involved in developing accurate models. If a standardized Analog format was established, models could be transferred from simulator to simulator, reducing the model development efforts. Other analog simulators, such as the Analog Work Bench and Saber offer faster simulators designed for use with higher level UUTs. No analog simulators have an automatic fault simulation capability.

The SYSCAP program uses the Ebbers and Moll mathematical model, whereas, Spice uses the Gummel and Poone mathematical model for the transistor. Some Spice version provides the capability to use either one in a simulation.

#### Hybrid

Hybrid simulation is required for circuits containing analog and digital functions. Two approaches are being used to simulate these circuits: 1) Serial analysis where the simulators are integrated and the simulators determines which type solution is needed based on the device type and output, and 2) separate simulators where the simulation data is developed in steps alternately solving analog and digital portions of the circuit.

#### E-M

Mechanical and electronic simulators co-exist on CAE workstations and computers and simulations are run separately with the operator providing data to each simulation tool as needed. No automated fault simulation tool was identified in the survey analysis.

## TRD Generators

TRD generators, such as PAWS and TAD, provide a means of producing the TRD document and ATLAS code from data inputted by the operator.

### 2.1.7 Survey Observations

The survey results indicated rapid advances are being made in some areas, and a continuing effort was required to insure that the recommendations consider data which was published during the early part of the Prepare Recommendation Phase of the contract. The mail survey results illustrated the difficulty in obtaining information directly from people busily engaged in their assigned tasks. Literature and personal contact proved to be the best sources for information.

The TRD generation is dictated by MIL-STD-1519 but the results revealed that each activity involved with the TRD had some differing opinions concerning the role of the TRD. The following is a list of aspects not recognized by all segments of the TRD community:

1. TRD users indicate that the TRD should provide an accurate source for all information needed to test a UUT. The TRDs today frequently lag UUT design changes, do not provide accurate data and contain unobtainable tests using the available ATE.
2. TPS developers indicate that the TRDs frequently contain test which check design parameters and should not be required for maintenance or trouble shooting type tests. These tests become a requirement on the TPS developer and increase costs, test program complexities and test times. The TRD also contain errors which must be identified and changed to insure that the TRD and TPS agrees.
3. The government agencies see the TRD as a vehicle which enables competitive bids for TPS development thus reducing TPS costs. They also see the TRD as serving as an interface between the UUT manufacturer and the TPS developer.
4. The developers of computer aids see the TRD as a document which in some present concepts represents an unnecessary break point in the automation process. This is because computer aids now allow Test Program generation directly from the simulation output.

The technical mechanics of TRD generation vary depending upon, TRD developer sophistication, type and level of TRD and the aid utilized. The TRD developers in general develop TRDs using the lower level engineers to gather data, input computer programs, compile results and perform simple analysis. The analysis and interpretation of data is left to senior engineers and UUT designers, who are experienced in the UUT function and operation. The TRD computer tools are developed by senior engineers or specialists who are experienced in test and computer programs. The results indicated that higher level of automation used, the lower the level of engineer required, and the lower the total cost.

## 2.2 INVESTIGATE MANUAL METHODS

### 2.2.1 TRD Generation Tasks

#### Test Requirement Document Generation

TRDs are generated for different levels of the UUT. Levels of structure above the component part level have been divided into three categories: SRU, LRU and System. The basic structure of the TRD remains unchanged for each level; however, TRD development techniques vary depending upon the UUT complexity. Figure 2-2, a generic flow chart, illustrates the development of a TRD. The flow illustrated depicts an existing small scale digital TRD process which should closely parallel a typical future flow for any type UUT. The five types of TRDs being evaluated are as follows.

- Systems comprised of digital components in the lower integration scales.
- Systems comprised of digital components in the higher integration scales.

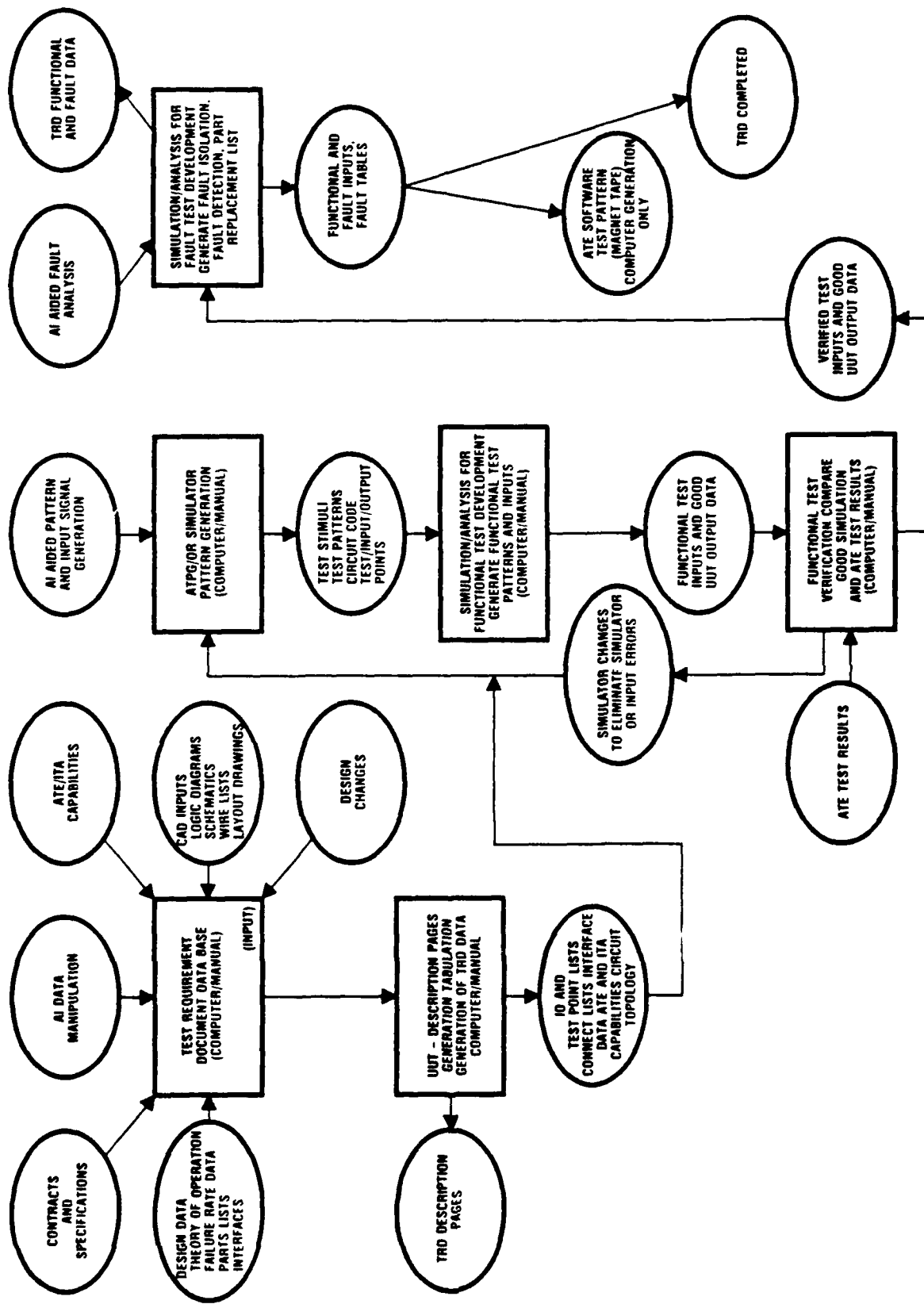


Figure 2-2. TRD Development Flow

- Systems comprised of analog components
- Systems comprised of digital, analog, and hybrid components.
- Electro-mechanical systems

The complete list of data required for TRD generation is shown in Figure 2-3.

#### UUT Description Pages

The UUT description pages effort involves the generation of part A of the TRD in the format specified by MIL-STD-1519 and DI-T-3734A. The following are required to complete part A of the TRD.

- Complete the Configuration Data Sheet for listing all reference drawings and specifications used to develop the TRD.
- Complete the General Design Data Sheet in the following manner:
  - 1) Obtain information concerning the UUT weight, special tools to be used, and handling requirements.
  - 2) Use the specifications to list input power requirements and tolerances.
  - 3) Obtain from specifications and drawings any pretest procedures and safety precautions.
- Complete the Interface Definition Sheets as follows:
  - 1) From parts lists and connector data provide any mating connector and test point connector information.
  - 2) Obtain information from specifications on special holding fixtures required to test the UUT.
  - 3) Using schematics and specifications list all pins with a detailed description of each pin function.
- Prepare a Cover Sheet, Approval Sheet, and Revision Sheet in the format specified by MIL-STD-1519.
- Part A sheets are then prepared by hand or by using a word processor.

Delivery of part A of the TRD is usually required at the beginning of the TRD Simulation (Part B and C) to facilitate test circuit coding.



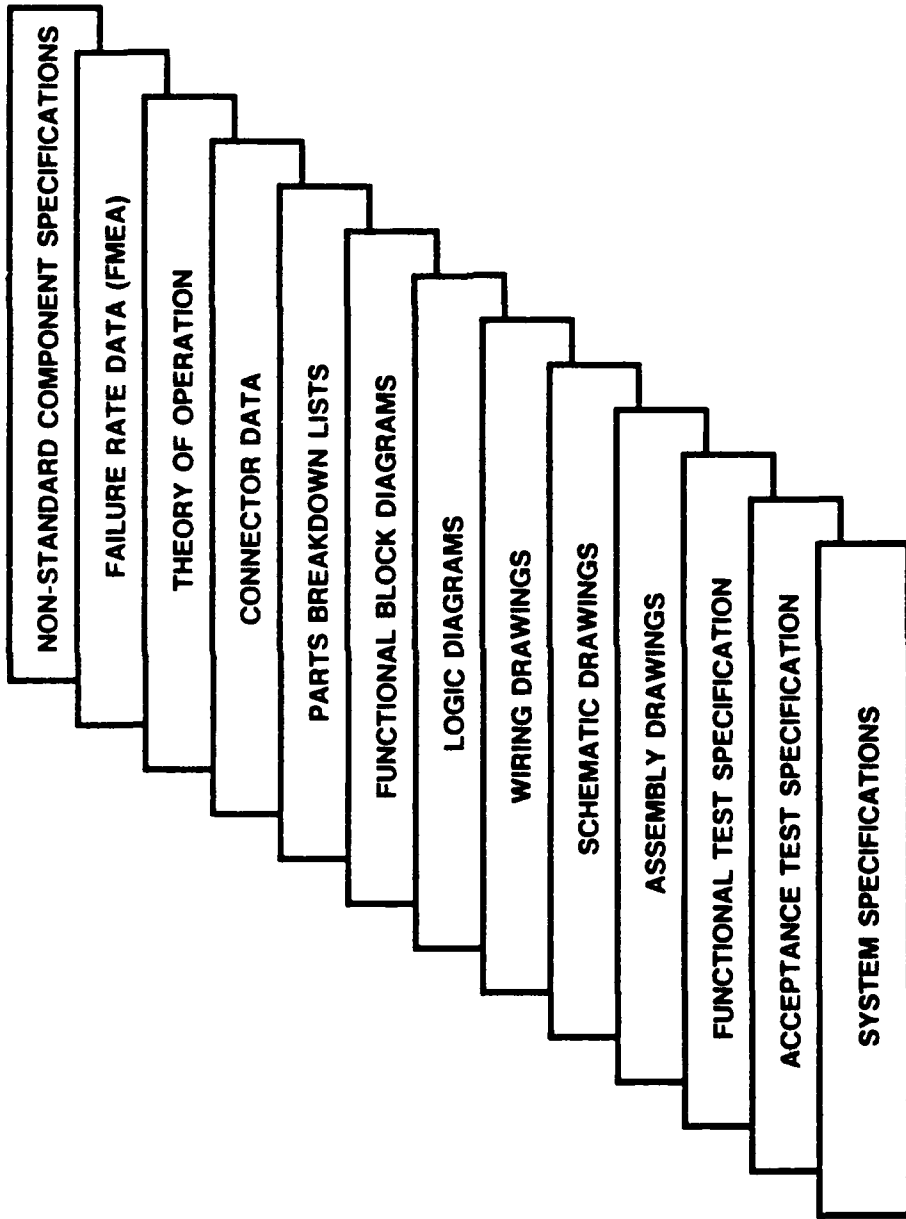


Figure 2-3. Required Data

## Functional Test Verification

The functional test verification consists of comparing the simulation program outputs with the functional test specification outputs. If the outputs do not agree, errors must exist in the UUT model, input signals or a UUT design error. After the errors are corrected, the simulation is rerun and the process repeated, until the program and specification outputs agree.

## Automatic Test Pattern Generation

An ATPG program is used for pattern generation for digital UUTs only. The ATPG uses algorithms to produce the minimum number of patterns for each input and output.

The ATPG is currently applicable to simple digital analysis. Other methods (hand and hot mock-up) utilize engineering-developed patterns, such as the functional test procedure patterns for parts such as Programmable Logic Arrays or other Application Specific Integrated Circuits (ASICs).

## Fault Simulation

Simulation of faults is accomplished, when a computer program is used by faulting all active UUT nodes (high, low and open). The UUT output of this fault-run is then compared with the functional test data to determine fault signatures. This activity generates fault data including fault detection, isolation and part replacement lists.

## Software Programming

Fault signatures are obtained by monitoring the outputs and test points with faults inserted. Hand analysis is accomplished by signal tracing from a fault to the outputs or test points.

ATLAS is a readable test language which can be converted or executed by an ATE. The ATLAS contained in the TRD is not complete. It is developed without knowing what the test instruments will be or what connections will be provided in the ATE. Therefore, TRD ATLAS code is considered non-executable and is essentially a word description of the test flow diagram. If the test flow is presented in the TRD the ATLAS code is largely a duplicated effort.

## Complete TRD

Completing the TRD involves the following:

- Layout the Test Flow per the applicable functional test specification [Go path only].
- Complete TRD Cross Reference Sheet. This cross reference correlates the TRD tests with the functional test specification tests.
- Layout the Detailed Test Flow [GO and NO-GO paths]. This flow details the testing philosophy for fault isolation, and is reviewed with the design engineer to ensure that it adequately covers the UUT.

- Complete the Detail Test Information Sheets by following the Detailed Test Flow.
- A TRD is then processed through word processing and the flows are entered into CAD.
- The final TRD is reviewed by the design engineer, and corrections made before delivery of the document.

The results of the survey indicated that there were few differences in the Manual Method use for different types or levels of UUT. A description of the Manual Method was developed and used as a baseline for evaluating automatic methods.

### 2.2.2 Efforts and Times Required

The manual method for TRD generation was divided into 16 major steps which were further divided to: identify tasks to specific skills, tasks performed by three or less people, or tasks with a single organizational responsibility.

The original proposal addressed the Manual Method as being different for each type and level of TRD, the results indicated that there were few differences and the Manual Method could be established as a single baseline for evaluating all methods.

Manually generated TRDs (no computer aids) use the method described in Table 2-4. If computer aids were considered as a part of the Manual method, all combinations of computer aids used by any company would have to be detailed, which is redundant. For this reason, the analog LRU TRD was used as a guide for generating the generic manual method. This method does not use aids or unique processes, and for this reason is applicable to all TRDs.

The 1500 hours (in-house average) required to produce a high quality Analog LRU TRD were used to establish a base line for comparing manual methods to computer based or automated generation procedures. This in-house average was obtained from Rockwell's Logistics organization which has the responsibility of developing TRDs. The time required and description of the 16 major steps is listed in Table 2-4. To show the improvement that will be made by implementation of automated process in the near future and future Table 2-4 was reduced to 13 major steps and is give in Table 2-5.

A simplified diagram of the TRD generation process is shown in Figure 1-2. It consists of 6 major categories which are:

|                                       |        |
|---------------------------------------|--------|
| Data Gathering                        |        |
| Summary of Total Testing Requirements | Part A |
| Performance Tests                     | Part B |
| Diagnostic Tests                      | Part C |
| ATLAS Procedures                      | Part D |
| Quality Assurance Verification        |        |

This flow diagram and Table 2-5 will be used to show the area of automation to be implemented in the near future and future and the hours saved by the implementation.

Table 2-4. TRD Generation Steps Defined For Manual Method

| Value     | Process               | Task                            | Description   |
|-----------|-----------------------|---------------------------------|---|
| 1500      |                       |                                 |   |
| <u>24</u> | Develop Contract Plan |                                 | Review all contractual instructions. Identify and obtain copies of all customer imposed specifications and procedures required for developing TRDs.   |
| 8         |                       | Review Contractual Requirements | Review the contractual requirements and establish a plan of action, development schedule and milestone chart. These items shall be dependent on the UUT development schedule.   |
| 16        |                       | Customer Specifications         | Obtain all customer specifications applicable to the contract.  |
| <u>28</u> | Gather Related Data   |                                 | Prepare a list of all UUT design and requirements data needed to prepare the TRD.   |
| 2         |                       | Available Data                  | Compile a list of applicable drawings and specifications.   |
| 6         |                       | Related Design Documentation    | Obtain the following design documents.<br><br>UUT Acceptance test specification<br>UUT Functional test specification<br>UUT Parts list<br>Assembly diagram<br>Subassembly diagram<br>Schematic diagram<br>Wiring diagram*<br>System and UUT Drawings<br>System specification* |
|           |                       |                                 | *Not critical to SRU TRD development  |
| 20        |                       | Generate Missing Design Data    | Data not readily available must be generated. Contact the UUT developer and request additional information, or assist in creating the data.   |

Table 2-4. TRD Generation Steps Defined For Manual Method (Continued)

| Value     | Process               | Task                | Description   |
|-----------|-----------------------|---------------------|---|
| <u>40</u> | Theory of Operation   |                     | Interpret the Theory of Operation from a test standpoint  |
| 16        |                       | Theory of Operation | The Theory of Operation is defined by the engineer developing the UUT. A logic diagram can provide a description for more complex UUTs, but is usually not critical to the TRD development. |
| 24        | Generate Missing Data |                     | Data not readily available must be generated. Contact the responsible engineer and request all required information not already in hand.  |
| <u>8</u>  | Physical Description  |                     | Description of UUTs   |
| 6         |                       | Necessary Data      | Obtain the following physical characteristics of the UUT incorporate them into the TRD.<br><br>Weight<br>Handling requirements<br>Safety requirements<br>Power requirements                 |
| 2         |                       | Format Data         | Format all the design data requirements into the MIL-STD format.  |
| <u>60</u> | Electrical Interface  |                     | Present all electrical interface data required to support the UUT.  |
| 16        |                       | Get Data            | Obtain from the functional test specification, schematic drawing, parts list, engineering, and connector information all required electrical interface TRD information.                     |

Table 2-4. TRD Generation Steps Defined For Manual Method (Continued)

| Value    | Process              | Task                | Description  |
|----------|----------------------|---------------------|--|
| 4        |                      | UUT Connector ID    | Provide the following UUT connector information. Cross reference the mating connector data for all connectors. Identify all test point connectors from the parts list and functional test specification.   |
| 40       |                      | Pin-Out Information | <p>Generate the pin-out requirements for the TRD. Each pin must be identified by signal name, mnemonic, and descriptive data sufficient to define each signal. This information can be obtained from engineering, functional test specifications and the schematic diagram. Descriptive data shall contain the following as applicable:</p> <ul style="list-style-type: none"> <li>Maximum wire length</li> <li>Grounding requirements</li> <li>Shielding requirements</li> <li>Wire or coax type</li> <li>Minimum wire size</li> <li>Separation of circuits</li> <li>Twisted pair requirements</li> <li>Impedance matching load requirements</li> <li>Signal characteristics</li> </ul> |
| <u>8</u> | Mechanical Interface |                     | Define all mechanical interface data required for the UUT.   |
| 2        |                      | Get Data            | Obtain from engineering the following mechanical interface TRD information. The descriptive data for all special mounting, holding, and support fixtures.  |
| 6        |                      | Generate Drawings   | Obtain drawings of all interface test equipment.   |

Table 2-4. TRD Generation Steps Defined For Manual Method (Continued)

| Value     | Process           | Task                  | Description   |
|-----------|-------------------|-----------------------|---|
| <u>8</u>  | Special Equipment |                       | Identify all special test equipment. Research all items and justify their use. Write a brief item description and include all UUT applications.                                 |
|           |                   | Equipment Drawings    | Obtain drawings of all special test equipment from engineering. The drawings should display all dimensions.   |
| <u>8</u>  | Special Tool      |                       | Identify all engineering specified special tools. Research the application of all tools and justify their use. Write a brief item description and include all UUT applications. |
| 8         |                   | Special Tool Drawings | Obtain drawings of all special tools. The drawings should display tooling dimensions.   |
| <u>50</u> | Test Data         |                       | Generate any test procedures which would assure proper test conditions.   |
| 40        |                   | Get Data              | Define the general test procedures and precautions to assure proper test conditions as stated in the functional test specification.   |
| 10        |                   | Format Data           | Format all test data from the functional test specification to provide a description of the UUT test.   |
| <u>4</u>  | Boiler Plate      |                       | Generate TRD boiler plate sheets for the UUT.   |
| 4         |                   | TRD Sheets            | Generate required boiler plate sheets   |

Table 2-4. TRD Generation Steps Defined For Manual Method (Continued)

| Value      | Process                     | Task                  | Description   |
|------------|-----------------------------|-----------------------|---|
| <u>200</u> | Test Design                 |                       | Define the UUT end-to-end test in flow chart form.  |
| 200        |                             | Functional Flow Chart | Generate the functional flow chart to graphically illustrate the end-to-end test sequence. Arrange so as to define the progressive strategy of testing from program entry to successful completion. Test in each block shall identify the function and nature of the test. The testing sequence should be similar to that in the functional test specification.                             |
| <u>400</u> | Test and Isolation Strategy |                       | Develop a test and isolation strategy for the UUT.  |
| 360        |                             | Fault Simulation      | Determine fault signature using hand analysis by signal tracing from fault to the outputs or test points.   |
| 40         |                             | Evaluate Results      | The UUT output of the fault simulation is then compared with the functional test output signals to determine the fault signature. This activity generates all fault data including fault detection, isolation, and part replacement lists. Fault signatures are obtained by monitoring the outputs and test points with faults inserted and noting difference from a good circuit response. |



Table 2-4. TRD Generation Steps Defined For Manual Method (Continued)

| Value      | Process                   | Task                 | Description   |
|------------|---------------------------|----------------------|---|
| <u>202</u> | Detailed Test Requirement |                      | Generate the detailed test requirements using the UUT test and isolation data and the functional flow chart.  |
| 100        |                           | Detailed Flow Charts | Detailed flow charts are required for all tests to be performed on the UUT. The detailed flow chart shall depict the test flow and UUT stimuli/response measurements. The patterns of each detailed flow chart shall be complete in that all the processes, decisions, branches, parallel operations and exits shall be identified. Process statements and symbol notation shall be provided in the detailed flow chart in sufficient detail to define the function tested, test methodology and the expected/required response. Stimuli/response tolerance shall be indicated and in accordance with the specified requirements of the UUT. Expressions of tolerances shall be consistent. In cases where absolute limits are established, the detailed flow chart shall indicate the delimiter required to ensure specified UUT performances. Additionally, a detailed flow chart shall be prepared for power up and power down routines plus other analog tests. |

Table 2-4. TRD Generation Steps Defined For Manual Method (Continued)

| Value      | Process      | Task                        | Description  |
|------------|--------------|-----------------------------|--|
| 24         |              | Detailed Cross Ref.         | A direct correlation shall be maintained between the detailed flow chart and the parameters described in the UUT acceptance test procedure. Each acceptance test procedure paragraph number, functional test description, detailed functional test number, and related circuit elements shall be listed in a cross-reference list. |
| 70         |              | Test Sheets                 | The detailed test information sheet shall be completed to furnish additional detailed flow chart data. Each sheet(s) must correspond to a specific block on the detailed flow chart.   |
| 8          |              | Format Data                 | Input and output signals obtained from the functional test specification should be referred to on the detailed test information sheet and included as part of the TRD.   |
| <u>200</u> | Create ATLAS |                             | Generate ATLAS code from detailed flow chart.  |
| 100        |              | Formal Document Preparation |  |
| 60         |              | Art Work Preparation        |  |
| 40         |              | Word Processing             |  |

Table 2-4. TRD Generation Steps Defined For Manual Method (Continued)

| Value      | Process       | Task               | Description  |
|------------|---------------|--------------------|--|
| <u>40</u>  | QA Provisions |                    | Quality assurance will verify that all required TRD data is created and meets all customer specifications.   |
| 40         |               | Inspection of TRD  | Review the TRD and assure that all information, instructions, and format requirements are met as stated in the contract. Check all drawings, specifications, and part numbers in the TRD for accuracy.   |
| <u>160</u> | QA Validation |                    | Quality assurance will evaluate all tests for function and accuracy.   |
| 40         |               | Validate Test Plan | Prepare a validation test for each test in the detailed flow chart. Verify each test by applying stated inputs into a good UUT and comparing the results with those of the TRD.  |
| 20         |               | Test Equipment     | It is the contractors responsibility that acceptable inspection and validation facilities are used to check the TRD. All special equipment and tools listed in the TRD should be utilized for quality assurance validation tests.                    |
| 60         |               | Perform Test       | Perform validation of each test. Record all results and note deviation to the expected output values stated in the TRD.  |
| 40         |               | Evaluation         | Evaluate the validation test results. If any test fails to meet test standards or requirements then the TRD must be returned to the developer for correction. Once the TRD is acceptable, it can be sent to the procuring activity for final review. |

Table 2-5. Present TRD Development Hour Breakdown

| <u>Present</u>             | <u>Manual</u>     |
|----------------------------|-------------------|
| Develop Contract Plan      | 24                |
| Gather Related Data        | 28                |
| Theory of Operation        | 40                |
| Physical Description       | 8                 |
| Elect & Mech Interface     | 68                |
| Special Equipment & Tools  | 16                |
| Test Data                  | 50                |
| Boiler Plate               | 4                 |
| Test Design                | 230               |
| Test Isolation Strategy    | 430               |
| Detailed Test Requirements | 202               |
| Create Executable ATLAS    | 200               |
| QA Provisions & Validation | 200               |
|                            | <u>1500 hours</u> |

### 2.3 TOOLS INVESTIGATION

The Application of Methods and Tools (Table 2-5), list the steps identified in the vertical axis and the type tool which can be applied to the step on the horizontal axis. The overlaps and voids are illustrated in the table.

Table 2-6. Application of Methods and Tools

| Function                     | Tool or Method |     |     |    |       |      |    |     |
|------------------------------|----------------|-----|-----|----|-------|------|----|-----|
|                              | CAD            | CAE | SIM | WP | ATLAS | TEST | DB | MAN |
| Develop Contract Plan        |                |     |     |    |       |      |    |     |
| Review Contractual Reqt.     |                |     |     |    |       |      |    | X   |
| Obtain Customer Spec.        |                |     |     |    |       |      |    | X   |
| Gather Related Data          |                |     |     |    |       |      |    |     |
| Available Contract Data      |                |     |     |    |       |      | X  | X   |
| Related Design Documentation |                |     |     |    |       |      | X  | X   |
| Generate Missing Design Data |                |     |     |    |       |      | X  | X   |
| Theory of Operation          |                |     |     |    |       |      |    |     |
| Theory of Operation          |                |     |     |    |       |      | X  | X   |
| Generate Missing Data        |                |     |     |    |       |      | X  | X   |
| Physical Description         |                |     |     |    |       |      |    |     |
| Necessary Data               |                |     |     |    |       |      | X  | X   |
| Format Data                  |                |     |     |    |       |      | X  | X   |
| Electrical Interface         |                |     |     |    |       |      |    |     |
| Get Data                     |                |     |     |    |       |      | X  | X   |
| UUT Connector ID             |                |     |     |    |       |      | X  | X   |
| Pin-Out Information          |                | X   |     |    |       |      | X  |     |
| Mechanical Interface         |                |     |     |    |       |      |    |     |
| Get Data                     |                |     |     |    |       |      | X  | X   |
| Generate Drawings            | X              | X   |     |    |       |      |    |     |

- CAD = Computer Aided Design System
- CAE = Computer Aided Engineering System
- SIM = Simulator
- WP = Wordprocessor
- ATLAS = Abbreviated Test Language for All Systems
- TEST = Tester
- DB = Data Base
- MAN = Manual

Table 2-6. Application of Methods and Tools (Continued)

| Function  | Tool or Method |     |     |     |    |       |      |    |     |
|---|----------------|-----|-----|-----|----|-------|------|----|-----|
|   | Process/Task   | CAD | CAE | SIM | WP | ATLAS | TEST | DB | MAN |
| Special Equipment<br>Equipment Drawings         |                |     |     |     |    |       |      |    | X   |
| Special Tool<br>Special Tool Drawings           | X              |     |     |     |    |       |      |    | X   |
| Test Data<br>Get Data                           |                | X   |     |     |    |       |      | X  | X   |
| Format Data                                     |                |     |     |     |    |       |      | X  | X   |
| Boiler Plate<br>TRD Sheets                      |                |     |     | X   |    |       |      |    | X   |
| Test Design<br>Functional Flow Chart            | X              | X   |     | X   |    |       |      |    | X   |
| Test and Isolation Strategy<br>Fault Simulation |                | X   | X   |     |    |       |      | X  | X   |
| Evaluate Results                                |                | X   | X   |     |    |       |      |    | X   |
| Detailed Test Req.<br>Detail Flow               |                |     |     | X   |    |       |      |    | X   |
| Detailed Cross Ref.                             |                | X   |     | X   |    |       |      |    | X   |
| Test Sheets                                     |                |     |     | X   |    |       |      |    | X   |
| Format Data                                     |                |     |     |     |    |       |      | X  | X   |
| Create ATLAS                                    |                |     |     |     |    |       | X    |    |     |
| QA Provisions<br>Inspection of TRD              |                |     |     |     |    |       |      |    | X   |
| QA Validation<br>Validate Test Plan             |                |     |     |     |    |       | X    |    | X   |
| Test Equipment                                  |                |     |     |     |    |       | X    |    |     |
| Perform Test                                    |                |     |     |     |    |       | X    |    |     |
| Evaluation                                      |                |     |     |     |    |       |      |    | X   |

No known system combines those tools mentioned above into a usable integrated program.

The TRD is currently used to develop test procedures for UUT testing. For most programs the TRD is developed after the hardware has been designed, and the engineering acceptance test procedure completed. By introducing TRD development as a part of the design, simulating the UUT at two different times can be eliminated. Eliminating the separate test simulation will shorten the total development cycle, and reduce the rework needed to obtain required testability levels.

The tasks defined as the Manual Method were compared to the available automated functions to determine which portions of the effort could now be done with computer tools. Analysis of the data indicated that automation was concentrated in the simulation, engineering and document generation areas. Each of the above areas of automation is applied independently, which results in duplicated simulation activities by the designer and the TRD developer. Simulation is widely used for digital circuits and occasionally for analog; other areas seldom use simulators. The form and content of a TRD using a simulator and one developed by manual methods is different in the fault detection and isolation procedures. Mil-Specifications and contracts requirements frequently vary with type and level UUT.

## 2.4 ASSESSMENT OF THE STATE-OF-THE-ART

Recognizing the fact that analysis techniques for design and maintenance are different but related; the Identification of the state-of-the-art included tools currently being used for TRD development. Electro-mechanical TRD automation has received very little attention, and application of a modified analog simulator in conjunction with the mechanical CAD is expected to provide the needed capabilities. No company contacted indicated development of an Electro-mechanical TRD generator

The following TRD generation topics were reviewed:

- Hardware requirements
- Software features
- Interactive/Batch
- Digital, Analog, Hybrid, Testability and EM simulators
- Model Library
- Fault detection, isolation
- Document generation
- Data base
- TRD generation
- Artificial Intelligence

The state-of-the-art computer tools identified in the survey analysis are listed in Appendix C.

Significant changes in the state-of-the-art occurred during 1986, resulting in a re-evaluation and modification of the tools listed in Appendix C.

Some of these tools are primarily used as design tools; they are listed to provide a capability which is needed for an automated TRD generator and is not otherwise available. Tools used for analysis by both test and design engineers are applied at different times during the development cycle resulting in duplicate efforts.

Data Base listings and four matrices (Digital, Analog, CAE Workstations, and AI), consisting of key items were prepared. The following conditions were noted:

The composite state-of-the-art represents an overall capability which contains overlaps and voids.

Tools, methods and techniques in existence resulted from individual companies developing the most cost effective approach with available resources.

Differences in computers, programming resources and contract requirements influenced the area automated and the extent of the automation.



### 3. EVALUATION

#### 3.1 EVALUATION OF METHODS

Automation of TRDs has resulted from the need to reduce costs and improve quality. For these reasons the high cost, labor intensive activities were addressed first. The development in the areas of digital simulation, document generation and ATLAS were automated. Until 1986, little had been done to standardize or interface computer tools in a workstation environment. Table 3-1 illustrates the major activities and lists the present merits and drawbacks of the methods in common use.

#### 3.2 ASSESSMENT OF METHODS

The data base contains items gathered during the Survey phase of the contract. This data was assigned sequential numbers and filed in the order received. The data base lists key elements and a summary for each data item. Data was sorted and evaluated, and the need for additional detail identified. To provide the needed detail in an easy to use format, four matrices were developed. The matrices contained data base items that were judged to satisfy the basic requirements of an automated process (ie. compatible hardware and software, user able to modify input, output and control of the software, language common with other needed capabilities).

The areas of primary interest were cost, value, compatibility, resource, effectiveness, technology limits, and CAD applicability. Data base items sometimes discussed specific issues which had to be related to a complete description of a method before an evaluation was possible.

When seven or more data base items discussed the same topic, they were listed in a matrix for comparison with items listed in other matrices. By using a matrix, it was possible to categorize, compare and analyze information contained in the articles. The articles usually discussed a key feature of a system. Frequently it was necessary to group information from several articles in order to obtain a composite of the systems capabilities.

The matrix (Appendix B) was divided into major categories (Digital, Analog, CAE/CAD Workstations and AI) within each category. From the matrix it was possible to compile a more complete description of the key methods.

Table 3-1. Merits and Drawbacks of Methods

| Activity                        | METHOD              | MERIT  | DRAWBACK  |
|---------------------------------|---------------------|--|---|
| DATA GATHERING                  | MANUAL              | Able to gather all types and form of data from all sources   | Labor intensive<br>Data management and interpretation difficult                                     |
|                                 | CAE/CAD             | Provides current design data   | All required data not available<br>Interface program needed   |
|                                 | DATA BASES          | Cost effective<br>Current  | Limited amount of data available<br>Needs interface program   |
| TRD PAGE DEVELOPMENT            | MANUAL              | Format adaptable to all types UUT<br>Optimized layout  | Time consuming<br>Variable formats  |
|                                 | CAE/CAD             | Rapid Flow diagram and schematic development<br>Mechanical design<br>Deliverable prints<br>Mixed text-graphics           | Same type and page for data input done manually<br><br>Usually stand alone<br>Special hardware      |
|                                 | DOCUMENT GENERATOR  | Data entered once<br>Flow diagrams and ATLAS generated<br>Consistent format  | Limited interface<br>Operator input   |
| FUNCTIONAL AND FAULT SIMULATION | MANUAL              | Mixed mode analysis<br>Optimized pattern<br>No model development   | Time consuming<br>Incomplete analysis<br>Inaccurate   |
|                                 | CAE/CAD             | Schematic capture<br>Analog, Digital and Mechanical done separately<br>Good model variety                                | Limited analysis<br>Not primarily intended for test<br>Limited model detail<br>Proprietary software |
|                                 | COMPUTER SIMULATION | High speed, accurate<br>Separate Analog/Digital hardware and software<br>Good model library<br>Rapid circuit development | Time consuming programs<br><br>Proprietary and incompatible   |
| QA VERIFICATION                 | MANUAL              | Independent verification   | Time consuming  |
|                                 | COMPUTER SIMULATION | Aid in verification  | Requires models and circuit code  |

Items in the matrices were assigned a Characterization Number. The Characterization Number aided in the determination of the most suitable combination of processes required for each of the five types and the three levels of UUTs being considered. The Characterization Number was used by sorting digit groups to obtain a list of relate item.

The data contained in the matrices was used to assess data and to prepare recommendations.

The survey data indicates that existing TRD generation programs accomplished multiple tasks, and possessed overlapping capabilities. Furthermore; these programs were written in different languages, operated on different computers, and were not easily modified or segmented by the user.

NOTE: Items are not listed in the same order as shown in the (Automatic) Application Code description. All digits within ( ) refer to the Application Code. When sorting for Application Code, LASAR 6 would appear on four different Application Code sorts (Manual Data Entry, Circuit Simulation, Workstation and CAE/CAD Interface). Manual Application Code Numbers are shown for Automatic/Manual comparison purposes only.

Features and capabilities of the surveyed methods were compared to the requirements of TRD generation for each UUT. Model algorithms, cost considerations, necessary resources, effectiveness of the approach and technological limits were evaluated empirically. Comparison of costs, delay time and skill levels, required for utilization provided a method for determining the optimum features for each type UUT. The assessment considered the impact of incorporating the metnods or parts of methods identified into CAD. The configuration of the CAD system and compatibility of operating systems were included in the assessment.

Prior to 1986 digital simulation activities could be divided into five general areas of activity:

1. CAD/CAE system - Primarily concerned with the design and development of electronic units
2. Simulation and pattern generation - Design tools used to verify the design and adapted for the testability analysis required for TRDs
3. TRD document generators - Provided documentation of test flow diagrams, generic ATLAS programs, part replacement data, functional and fault test sequences, from manual keyboard inputs
4. Artificial Intelligence - applied to system analysis to provide the additional knowledge and reasoning to improve testability and designs
5. Improved computers and hardware - the development of faster, larger capacity computers and hardware/software simulators.

In 1986, the five general areas were combined into automated processes, either by expansion of existing capabilities (such as Teradyne) or by combining the capabilities available from several companies (such as HHB & Factron). The main thrust has been to develop the test program on a workstation which had CAD capabilities. Test program development on a CAD workstation has resulted in by-passing the TRD. Since the TRD was not included in the CAD developed Test Program; it is necessary to transfer data to a TRD generator (such as TRD ATLAS Development (TAD) or Personal ATLAS Workstation (PAWS)), to complete the process. The drawback to this type automated process is that it usually produced test programs for a specific commercial tester. Considering the impact of the 1986 improvements, determining the future need, the use of the TRD becomes a critical element in evaluation and recommendation of the development of an automated TRD process. It is apparent that the TRD must be changed to eliminate duplicated and unnecessary data; it must perform an essential function as a part of the TPS. Definition of the future TRD will relate the development cycle of the TRD/TPS to the development of the UUT and the ATE.

Schematic capture of engineering data on a CAD/CAE system for TRD development has been accomplished where the data was originally generated on the CAE workstation.

Most CAE workstations provide a simple functional analysis, limited testability analysis, and wire list outputs. In most cases data can be transferred to other computer programs through a manufacturer-developed interface program.

The digital simulation programs, such as HITS, run on larger computers and provide accurate simulations of SRUs and LRUs. Simulation outputs include fault detection, fault isolation, faulty component tables, testability calculations, and test patterns and sequences; all of which can be included in the TRD and the ATLAS program. The small and medium digital area is the most automated of the areas included in the study. However, the following capabilities are not universally available: CAE to simulator data transfer, simulator feedback to the CAE, improved automatic pattern generation, and a simulator-to-TRD wordprocessor interface.

Large-scale digital automation is being considered at the part level in the TISSS program. This program is using existing simulators, and large functional models for simulation. The technique may be applicable to large-scale digital UUT simulation, and should be analyzed after completion of the TISSS contract. The need for this level of simulation is recognized, and is being worked by a number of companies.

The feasibility of automating complex digital UUTs will require additional development in the areas of functional and logic simulation, reducing computer run times, pattern generation, model generation, hardware in active simulation and system interfaces.

Automated analog TRD generation has not been used for the following reasons:

1. Acceptance of current manual methods
2. Complexity of analog functional models
3. Requirements for serial analysis
4. Excessive computer run time
5. Skill level of personnel required

Previous approaches required expanding the capabilities of analog design simulators, adding functional modeling capabilities, and converting output formats. The results were excessive computer run times, outputs that required skilled engineering evaluation, complex model development, and transcription of data into a form acceptable for the TRD.

Two companies, Analog Design Tools and Analogy, have developed analog workstations; however, they have not included automatic fault detection and isolation.

Hybrid TRD development is accomplished by hand or by combining the results obtained from separate analog and digital simulations. The only exception is the use of a Hybrid simulator on several programs by Rockwell. This simulator is considered to be proprietary and still in the development phase.

Combined simulation required for hybrid UUTs is possible. However, the analog simulations tend to slow the digital analysis. Due to need for serial analysis, this application is slower than parallel or concurrent simulation.

The state-of-the-art in Electro-mechanical TRD development is related to hybrid simulation in that both analog and digital electrical signals may be involved. Mechanical simulation involves physical units of measure, which generally can be simulated using analog simulators. TRDs of this type are generated by hand, but may use the tools listed in the hybrid description. Development of an automated process probably will not be practical until a good hybrid simulator exists.

The state-of-the-art as viewed from a variety of complexity standpoints (System-LRU-SRU), tends to divide into two categories: tool which can be used for all types and levels of TRDs, and tools which must be developed specifically to support the unique requirements of the UUT. The current trend is to expand the SRU tools and techniques to include all but the complex LRUs. System level and complex LRUs use computer programs which analyze control, stability, safety and functionality. These commercially available tools were developed for the system design engineer to theoretically analyze the system operation, and perform a top down system development. Few people were found who have performed system design, and have also developed TRDs.

TRDs are not normally written at the system level, and probably will not be until VHSIC devices are incorporated into SRUs. By using the analysis matrix, and summarizing the results, certain tools are listed in all categories while others appear only once. It becomes obvious that the high development cost, and complexity associated with tools supporting only one or two areas will be developed only if a need arises which will justify the expenditure. Today's major thrust is in the high-complexity digital area, and aid development in that area has the highest priority.

## 4. ASSESSMENT OF THE TRD PROCESS

### 4.1 NEAR FUTURE PROSPECTS FOR AUTOMATION

Automation of the various process was investigated to determine feasible approaches for combining the known and expected new TRD generation tools. Compatibility with CAE workstations, and the amount of operator participation were two of the key characteristics considered for each tool.

The recent trend appears to be toward a workstation combining the design and verification activities on a dedicated hardware/software system. Examples of systems which have accomplished this are systems offered by Daisy, Mentor and Valid. These systems offer capabilities for simple circuit design, design test and verification, testability analysis and physical circuit development involving multilayer boards or substrates. Expanding these capabilities for simple digital TRD development requires developing software which will provide all the capabilities, currently available on a number of computers, on a single workstation. The main concern from a utilization standpoint is the execution time required for TRD development which will reduce time available for the design related tasks listed above. Complex Digital, Analog, Hybrid and Electro-mechanical present additional problems requiring development of both hardware and software to automate the TRD process on a workstation.

Impact of Test on Design - BIT, BITE and BIST all add additional circuitry to the UUT to provide a method for establishing and monitoring the functionality of the UUT. This circuitry aids in the test required by the TRD. The use of this circuitry aids in providing continuity of failure data from the system test to the individual UUT test by providing a common monitor at all levels. Utilization of BIT, BITE or BIST requires that the circuits be powered, interfaced, and tested by the ATE. Use of these built-in circuits may reduce or eliminate some of the ATE equipment normally required. Use of these features in TRDs is relatively new, and very few articles were found which describe applications of this kind. The incorporation of these capabilities should become commonplace in the next five years. This incorporation of UUT based tests on the TRD process will require a method to extract test data from the UUT and utilizing this data for analysis on the ATE. The TRD must incorporate test procedures for these circuits and make test decisions based on all possible data obtained from the circuit, simulation of test circuits must be included to establish the credibility of the UUT test data. The decision to use or reject UUT data should be defined by the TRD and if possible implemented automatically. This process will add complexity to the TRD and increase the amount of testing required for a particular type UUT.

Developments by CAE/CAD manufacturers to provide complete design capabilities on a workstation has resulted in transporting software to common computer systems, such as, the VAX and APOLLO computers. Companies such as Fairchild and HHB, have developed workstations which provide capabilities interfaced to testers. The "islands of automation" are becoming complete processes linked together on computers, which have data bases, tester interfaces, communication programs, network capabilities and high speeds.

Outputs available from the CAE design data base should include connect list, parts list, theory of operation, interface descriptions, environmental requirements, input signal and power specifications. Some of this data is not currently incorporated. Since simulation is a key area in the development of an automatic TRD generator, a gap is created in the automated process for all but digital simulation. Analog, Hybrid and Electro-mechanical simulators are few, and those that do exist do not provide for automatic fault simulation required for the TRD. Design simulators such as SABER, and Analog workbench require expansion to include fault capabilities before an automated process will be available. Analog simulators such as SPICE, and System Circuit Analysis Program (SYSCAP) are intended for design at a low complexity level. Application of these analog programs would require developing models of complex devices, and intensive computer analysis (days to weeks depending upon circuit complexity).

Significant progress is being made in fields related to TRD automation. The study of the process indicated that the data included in the TRD should be changed. Two possibilities exist: 1) the TRD be changed to include only UUT description, and all other activities be performed as a part of the TPS, or 2) the TRD be changed to include: a complete detailed Theory of Operation, executable MATE ATLAS code, a list of MATE test equipment capable of performing the test, and an Interface Test Adapter (ITA) connection list. With the advances in tools and the automation of the TRD, the second possibility appears to be the most cost effective. Most capabilities needed to accomplish the automation exist or are in the planning stages. Interfaces to a variety of sources, and sharing of resources will require development of new controls and techniques to insure successful operation without interfering with other activities such as design.

The recommendations, resulting from this study, allow for the development of an automated TRD generator by modifying the TRD and TPS Mil-Specifications, to redefine the role of both activities, and by using a software control program. The control program will provide and control application of AI, Data Bases, all types of Simulators, Wordprocessors and Communication programs to the best suited resources for the particular workstation activity being performed. Additional developments are needed in the areas of computer hardware, and simulation programs before a completely automated system is realized.

Simple Digital circuits are already being developed on workstations, the areas requiring improvement are data base interfaces and automated TRD generator inputs. The evolutionary process for progressing from the Present to the Near Future and the Future will be to develop new specifications, apply higher capacity equipment, develop data base interfaces and TRD generator input routines.

Complex Digital Systems will evolve from the existing technology with the adaptations of system level simulators, hardware models and hardware simulators. Recently announced hardware advances will tend to enable development and simulation at a local level. Development of the TRD on a workstation will be accomplished by adding the TRD generator to the workstation and interfacing with data bases, testers, hardware and model simulators. These tasks can be accomplished in the near future with existing or anticipated tools.



The Analog system requires extensive development in the areas of complex simulation and fault analysis. Systems on the market and proposed for the near future do not satisfy these shortcomings. Signal generation for analog circuits are usually generated by hand, automatic generation will require analysis of the functional requirements and the tolerances associated with each input.

The Hybrid system remains a combination of analog and digital systems. Development of an automated system requires all of the items listed in the analog and digital systems plus a means of interfacing the two capabilities. The near future capabilities will be limited to mathematical simulations and simple circuits.

The Electro-mechanical system is similar to the hybrid problem except mechanical and electronic characteristics must be translated to interact.

The conclusion derived from the analysis are illustrated in Figure 4-1, Table 4-1 and Table 4-2. Figure 4-1 shows the automation that will occur in the near future and Table 4-1 shows the reduction in TRD development hours compared to the manual method of generating TRDs. Table 4-2 illustrate the hardware/software which will be required for the near future.

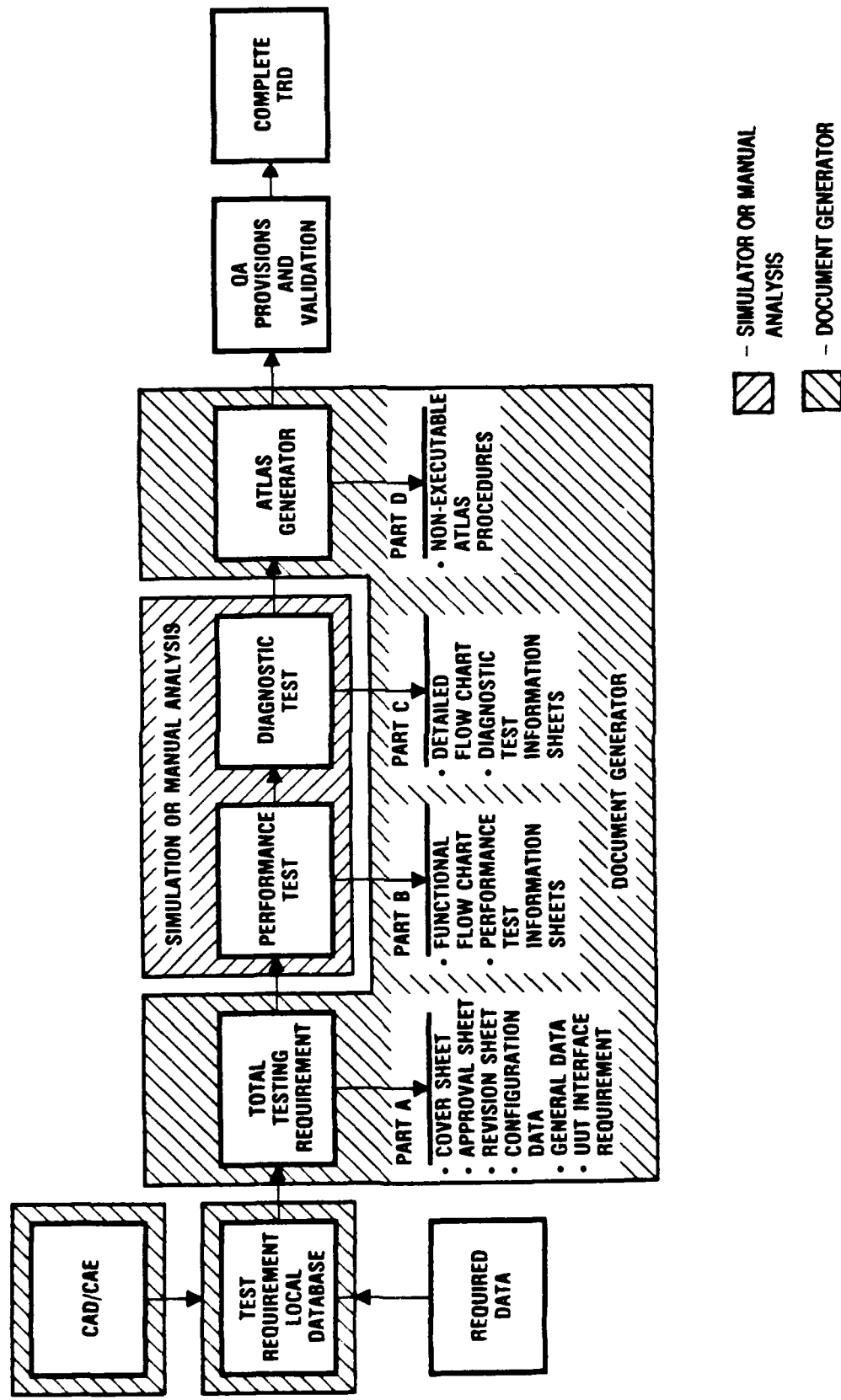


Figure 4-1 Near Future TRD Generation

Table 4-1 Near Future TRD Development Hour Breakdown

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| <u>Present</u>             | <u>Manual</u> | <u>Near<br/>Future</u> |
|----------------------------|---------------|------------------------|
| Develop Contract Plan      | 24            | 20                     |
| Gather Related Data        | 28            | 16                     |
| Theory of Operation        | 40            | 16                     |
| Physical Description       | 8             | 4                      |
| Elect & Mech Interface     | 68            | 8                      |
| Special Equipment & Tools  | 16            | 8                      |
| Test Data                  | 50            | 50                     |
| Boiler Plate               | 4             | 4                      |
| Test Design                | 230           | 200                    |
| Test Isolation Strategy    | 430           | 300                    |
| Detailed Test Requirements | 202           | 28                     |
| Create Executable ATLAS    | 200           | 200                    |
| QA Provisions & Validation | <u>200</u>    | <u>150</u>             |
|                            | 1500 hours    | 1004 hours             |

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Table 4-2 Near Future Hardware/Software Requirement

| <u>Hardware Configuration</u>          | <u>Software Configuration</u> |
|--|-------------------------------|
| 1. VAXstation II                       | 1. VMS-ws                     |
| a. Hi-resolution color graphic monitor | 2. Mentor program             |
| b. 16 MB RAM                           | 3. ATRED program              |
| c. 210 MB hard disk                    | 4. DECnet                     |
| d. Ethernet controller                 | 5. RJE emulator               |
| e. Mouse/Tablet                        | 6. SPICE simulator            |
| 2. Color plotter                       | 7. HITS simulator             |
| 3. SNA gateway                         | 8. CAE/CAE program            |
| 4. Modem                               |                               |

## 4.2 FUTURE PROSPECTS

Selection of possible techniques and programs for future applications required considering new approaches to unresolved problems. Developing techniques for simulating complex UUTs is one of the key unresolved issues. The application of programs similar to testability analysis programs, such as SCOAP could provide rapid analysis by eliminating the need to check each nodes performance for functional and fault conditions; however, development of test patterns or input signals for use on the ATE do not currently result from this type analysis. Further investigation into the behavior of functional models and circuits is needed to resolve these conditions. The limitation of developing an Analog/Digital/Electro-mechanical hybrid simulator appears to be restricted to serial-circuit solution approaches. The time required to solve complex circuits serially is prohibitive. The alternate solution is to develop and interface specialized simulators which will interactively and concurrently solve portions of the circuit. To effectively perform this function a control program must be developed which will select the proper resources and and combine the results.

New computer hardware needed to provide a variety of capabilities and high speed can be provided by a network of capabilities used as needed rather than developing a system specifically designed to provide TRD generation capabilities. This approach will allow TRD developments for all types and levels UUT to be developed on any CAE workstation available on the network.

Figure 4-2 shows the area of automation that will be required for a fully automated process for the future. Table 4-3 illustrates the reduction in development hours in relation to the manual method and the near future processes. Typical hardware needed to develop such a system is illustrated in Table 4-4. Approximate costs are estimates and do not indicate current costs of equipment listed in the figure.

Requirements to reach the future configuration of each type UUT are:

- 1) The future of the simple digital will require integrating the capabilities into the complex digital system by standardizing model interfaces and languages to enable model swapping to insure that detailed analysis is available when needed.

- 2) The future complex digital system will require the standardization of interfaces and controls to enable allocation of tasks to a variety of linked capabilities. The workstation will select the optimum resource for the task at hand, divide the tasks and control parallel processing of the tasks. Data will be returned to the local station, organized, stored and and outputted with minimum operator participation. This can be accomplished by developing a shell program which incorporate AI techniques and provides a framework for the incorporation of new capabilities as they become available.

3) Automatic generation of analog TRDs will require developing an input stimulus generator which will be capable of providing signals variable through the specified tolerances. The identification of output changes caused by the input must be evaluated. Future application of AI techniques to signal generation is necessary to resolve this problem.

4) Fault analysis and complex circuits will require developing a new approach to simulation, possibly the adaptation of engineering system design techniques or testability analysis approaches.

5) A generic solution to integrate all types and levels of electro-mechanical UUTs is possible in the future, by using a shell program all needed resources will be available at any workstation in the network.

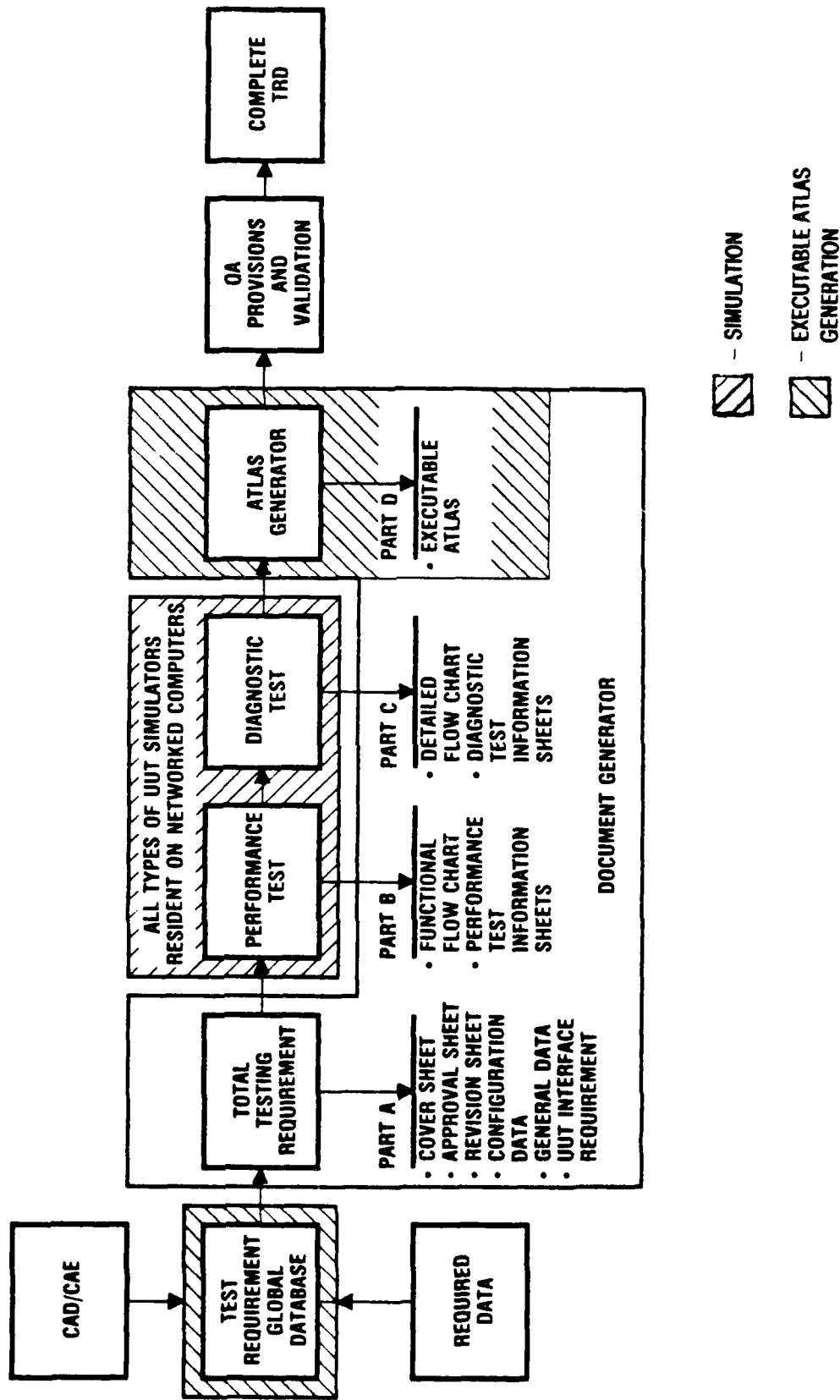


Figure 4-2 Future TRD Generation

Table 4-3 Future TRD Development Hour Breakdown

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| <u>Present</u>             | <u>Manual</u> | <u>Near<br/>Future</u> | <u>Future</u> |
|----------------------------|---------------|------------------------|---------------|
| Develop Contract Plan      | 24            | 20                     | 8             |
| Gather Related Data        | 28            | 16                     | 8             |
| Theory of Operation        | 40            | 16                     | 16            |
| Physical Description       | 8             | 4                      | 4             |
| Elect & Mech Interface     | 68            | 8                      | 8             |
| Special Equipment & Tools  | 16            | 8                      | 8             |
| Test Data                  | 50            | 50                     | 24            |
| Boiler Plate               | 4             | 4                      | 4             |
| Test Design                | 230           | 200                    | 100           |
| Test Isolation Strategy    | 430           | 300                    | 200           |
| Detailed Test Requirements | 202           | 28                     | 28            |
| Create Executable ATLAS    | 200           | 200                    | 60            |
| QA Provisions & Validation | <u>200</u>    | <u>150</u>             | <u>130</u>    |
|                            | 1500 hours    | 1004 hours             | 598 hours     |

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Table 4-4 Future Hardware/Software Requirement

Hardware Configuration

1. Advanced general purpose supermicro computers
  - a. Full CAE/CAD function
  - b. Full networking down to record locking
  - c. 300 dpi color graphics monitor
  - d. Video input
  - e. Voice input
  - f. Tablet input
2. Printer
  - a. Color laser page printer
  - b. Plotter
  - c. High speed laser
3. Satellite/microwave comm link to world wide parts/module data bases
4. Super FAST crunchers for real-time analysis and fault simulation

Software Configuration

1. Operating system
  - a. Full networking for mixed vendors
  - b. Multi-tasking
  - c. GOOD user interface
2. CAE/CAD system
3. DoD Security
4. ATRD program

Table 4-4. Future Hardware/Software Requirement (Cont)

Printers and plotters:

More than one type of printer/plotter will be required. LASAR printers are OK for small page text and graphics. But plotters will be needed to output large schematic and detailed flow diagrams from the design or logistics.

|                 |             |  |
|-----------------|-------------|--|
| Laser printers: | \$4,500.00  | (Fast, heavy duty, graphics+text)          |
| Color Plotters: | \$15,000.00 | (4'wide, unlimited length, floor standing) |

Micro Computers (8-16 bit):

The small computer allows a limited use distributed processing. The local CPU is not powerful enough to run large simulation in a timely manner. The small computer can be hooked up (via a network or some type of communication line) to a larger system and have the completed simulation set back.

Cost: \$5,000 (min 640K memory, 30MB hard disk, PGA with multi-scan monitor)

Supermicro/mini computers (32 bit):

The supermicro has the power to run large simulations locally, and the graphics to be a complete CAE/CAD work system. The communications and CPU power combined with integrated networking operating system allow the supermicro/mini to be a fully cooperating member of a larger network.

Cost: \$12,000-up (3MB memory, 140MB hard disk, Ethernet, 19" color monitor,, Graphics @ 1024x1024 resolution, floating point hardware)

Supermini computers (32 bit):

The supermini can be the base CPU type in a network of supermicros. The main data bases can be accessed here and large simulation (batch) may be send here. The more powerful this system the better the entire network will do overall. These systems can be stacked as needed when the demand requires.

Cost: \$350,000 (68MB memory, 8 Gigabyte disk, Ethernet, Array processor)

## 5. GUIDE FOR IMPLEMENTATION

### 5.1 BASIS FOR IMPLEMENTING CHANGES

The investigation of the near future and far future was conducted by defining the specification and application changes that were necessary to overcome the criticisms expressed during the survey. The major criticisms expressed below, represent the concerns of different groups, TRD Users, Developers, Military, and Tool Developers.

1. TRD users indicate that the TRD should provide an accurate source for all information needed to test a UUT. The TRDs today frequently lag UUT design changes, do not provide accurate data, and contain unobtainable tests using the available ATE.
2. TPS developers indicate that the TRDs frequently contain tests which check design parameters, and as such are too stringent for maintenance or trouble shooting tests. These tests become a requirement on the TPS developer, increase costs, test program complexities and test times. The TRD also contains errors which must be identified and changed to ensure that the TRD and TPS agrees.
3. The government agencies see the TRD as a vehicle which enables competitive bids for TPS development thus reducing TPS costs. They also see the TRD as serving as an interface between the UUT manufacturer and the TPS developer.
4. The developers of computer tools, see the TRD as a document which in some present concepts represent an unnecessary break point in the automation process. This is because computer tools now allow Test Program generation directly from the simulation output.

### 5.2 RECOMMENDED CHANGES

From these comments the following changes to MIL-STD-1519 specification and the methods used were defined which would possibly eliminate the condition.

1. Automate TRD development on a CAE station thus allowing the design engineer to produce the TRD with minimum additional effort.
2. Expand existing CAE data bases to include all items needed to develop the TRD.
3. Modify the TRD function and output to consider ATE capabilities to ensure that realizable tests were defined.
4. Identify and omit design verification parameters and tests which need not be performed in the test intended to verify function operation or fault tests.
5. Provide the TRD on a specified type of electronic media, such as magnetic tape, to the TPS and Tool developer for necessary updates and modification.

6. Define a phased development cycle for the TRD that parallels the UUT life cycle allowing additions to the TRD to occur once the data is available from the UUT development cycle.
7. Provide a minimum TRD content (including a well defined Theory of Operation) when released to obtain quotes for TPS development.
8. Verify the accuracy and completeness of the TRD when released for TPS quote and when completed.
9. Establish the TRD as an integral portion of the TPS to provide all needed UUT test information and characteristics.

The present mechanics of TRD generation vary depending upon TRD developer sophistication, type and level of TRD, and the tool utilized. However, most TRD are developed using lower level engineers to gather data, input computer programs, compile results and perform simple analysis. The analysis and interpretation of data is left to senior engineers and UUT designers, who are experienced in the UUT function and operation. The changes proposed below propose that through automation it will be possible for the design engineer to perform the TRD task with minimum impact on design productivity.

The TRD generation steps identified in Table 2-5 were analyzed to determine the type of effort required and automation category which might be applicable to each task. The analysis shown in Table 5-1 was based on the data gathered during the survey and the literature search. Table 5-1 is a simplification of Table 2-5 showing the steps required for TRD generation under the title "Function"; how the step is performed under "Type of Task"; and under "Category" the automation process that is applicable to that step.

Table 5-1. Automation of TRD Tasks

| FUNCTION                        | TYPE OF TASK        | CATEGORY |
|---------------------------------|---------------------|----------|
| DEVELOP CONTRACT PLAN           | CREATE              | M*       |
| REVIEW CONTRACTUAL REQUIREMENTS | GATHER & REVIEW     | D        |
| CUSTOMER SPECIFICATIONS         | GATHER & REVIEW     | D        |
| GATHER RELATED DATA             | GATHER              | D        |
| AVAILABLE DATA                  | COMPILE             | D        |
| RELATED DESIGN DOCUMENTS        | COMPILE FROM DESIGN | D        |
| GENERATE MISSING DESIGN DATA    | RESEARCH & DOCUMENT | M*       |
| THEORY OF OPERATION             | REVIEW              | M*       |
| DEFINE THEORY OF OPERATION      | DOCUMENT            | D        |
| GENERATE MISSING DATA           | COMPILE             | M*       |
| PHYSICAL DESCRIPTION            | COMPILE FROM ENG.   | D        |
| NECESSARY DATA                  | EXTRACT DATA        | D        |
| FORMAT DATA                     | DOCUMENT            | G        |

M -MANUAL D -DATA BASE S -SIMULATOR G -TRD DOCUMENT GENERATOR  
T -TEST STRATEGY \* -DESIGN RESPONSIBILITY

Table 5-1. Automation of TRD Tasks (Continued)

|                            |                         |    |
|----------------------------|-------------------------|----|
| ELECTRICAL INTERFACE       | DEFINE REQUIREMENTS     | M* |
| GET DATA                   | COMPILE FROM ENG.       | D  |
| UUT CONNECTOR ID           | TRANSLATE/CROSS REF     | G  |
| PIN OUT INFORMATION        | TRANSLATE/CROSS REF.    | G  |
| MECHANICAL INTERFACE       | DEFINE REQUIREMENTS     | M* |
| GET DATA                   | COMPILE FROM ENG.       | D  |
| GENERATE DRAWINGS          | COMP. FROM ENG.         | D  |
| SPECIAL EQUIPMENT          | REVIEW ENG. REQ.        | M* |
| EQUIPMENT DRAWINGS         | COMP/TRANS              | D  |
| SPECIAL TOOLS              | REVIEW/JUSTIFY          | M* |
| SPECIAL TOOL DRAWINGS      | COMPILE DRAWINGS        | D  |
| TEST DATA                  | GENERATE TEST PROC.     | T  |
| GET DATA                   | DEFINE TESTS            | T  |
| FORMAT DATA                | TRANSLATE TO TRD        | G  |
| BOILER PLATE               | GENERATE PAGES          | G  |
| TRD SHEETS                 | TRD PAGES               | G  |
| TEST DESIGN                | DEFINE END TO END TESTS | T  |
| FUNCTIONAL FLOW CHART      | DEVELOP FLOW CHARTS     | G  |
| TEST ISOLATION STRATEGY    | DEV TEST & ISO. STRAT   | T  |
| FAULT SIMULATION           | DETERMINE FAULT SIGNAT. | S  |
| EVALUATE RESULTS           | EVALUATE SIMULATION     | T  |
| DETAILED TEST REQUIREMENTS | DEFINE TEST REQMTS.     | T  |
| DETAIL FLOW                | DEV TEST FLOW CHARTS    | G  |
| DETAILED CROSS REFERENCE   | CHART/PROC CROSS REF    | G  |
| TEST SHEETS                | PREPARE TEST SHEETS     | G  |
| FORMAT DATA                | FORMAT & COMMENT        | G  |
| CREATE ATLAS               | GENERATE ATLAS          | G  |
| QA PROVISIONS              | CHECK CUST. COMPLIANCE  | M  |
| INSPECTION OF TRD          | CHECK TRD CONTENTS      | M  |
| QA VALIDATION              | EVALUATE TESTS          | M  |
| VALIDATE TEST PLAN         | CHECK INPUT TO OUTPUT   | M  |
| TEST EQUIPMENT             | CHECK SPECIAL TOOLS     | M  |
| PERFORM TEST               | RUN TESTS               | M  |
| EVALUATION                 | EVALUATE TEST RESULTS   | M  |

The investigation of specific tools application to the tasks identified, required analyzing the Tools and their attributes described in the survey data, literature, and matrices. The investigation was divided into major categories: Testability, CAE workstations, Computers and Peripherals, Simulators and TRD generators. The investigation provided a means for estimating when the automated process would be available as well as defining it's probable capabilities. Appendix D contains the list identifying the data included in the analysis, brief description, and how the data would be applied.

### 5.3 ACTIONS REQUIRED TO IMPLEMENT CHANGES

Recommended changes can be divided into the various aspects of TRD automation as follows:

1. Modify existing Mil-Specification.
2. Develop and modify TRD process
  - Hardware
  - Software
3. Incorporate emerging technologies.
4. Further develop simulators.

#### 5.3.1 Modify Existing Mil-Specification

In order to develop the TRD automatically early in the development cycle, to minimize the impact on design, and to control the number of versions produced, several revisions are needed to MIL-STD-1519.

Provide standardized format for types of UUT as appendices to MIL-STD-1519.

- TRDs produced automatically will provide a standardized format based on the type and level of UUT. To control the contents of the TRDs, additional page formats should be defined which will include complex signals, mechanical diagrams, etc. Standardized formats should define the method for accessing and transferring data; formatting of the data; methods for modifying the approval channels; identify central reporting; how to interpret the data.

Enhance requirements to include more comprehensive Theory of Operation.

A detailed description, with tables, figures, illustrations and references should supplement a written Theory of Operation technical description. Theory of Operation can become essential in case of redesign, questionable test results, substitution of stimuli or effects of stimuli sequences. Page formats for test patterns should provide areas which insure incorporation of adequate signal patterns, drawings, diagrams needed to fully define the test pattern and its application. The Theory of Operation page should require a general overview, application of the UUT, input, output signals, their criticality and function, symptoms of faulty operation and unusual or special conditions which could possibly occur.

Requirements for use of MATE test equipment where applicable.

The TRD should provide complete UUT description of testing, and verify the testability of the UUT and define a test strategy for a selected set of test equipment from the MATE test equipment library. By requiring the use of the MATE Automatic Test Equipment library it will identify a possible ATE configuration. Equipment included in the MATE library has ATLAS commands which will enable the application of the test equipment for all of its measurement functions, by knowing the measurement needed for a test, the capabilities of the equipment, and the ATLAS commands needed to exercise the equipment, a library of ATLAS subroutines can be developed and used to translate TRD specified test into executable test routines. MATE is specified to control known set of equipment, interfaces and ATLAS.

Provide requirement for executable ATLAS code and ATLAS Test Flow Diagram.

- The generation of now executable ATLAS code and Test Flow Diagrams represents a duplication of information in that the same data is presented in two forms. This problem can be overcome in two ways: 1.) Eliminate ATLAS code from the TRD or 2.) develop an executable ATLAS code. In order to produce executable ATLAS code, activities currently performed as a part of the TPS must be done as a part of the TRD. Areas involved relate to preliminary selection of ATE equipment, applying an Automated Test Strategy program and providing additional data to the test program developed. These efforts must be defined in the TRD and TPS specification.

Define standard interface requirement for ATRDG shell.

THE ATRDG shell must perform the following functions:

1. Reside on the CAE and be callable at any time.
2. Automatically access and search data base.
3. Transfer data to a local data base.
4. Select optimum simulator.
5. Transfer data to and from one or more simulators.
6. Integrate data from simulators.
7. Determine if distributed processing should be used.
8. Distribute tasks.
9. Operate in background with minimum operator participation.
10. Provide operator instruction, menu shortfall lists and other output data related to TRD.
11. Provide for easy addition or change of utilized hardware or software.
12. Operate a networked system.
13. Perform tasks in the background (transparent to the operator).
14. Create a TRD.
15. Provide for control and protection of data.
16. Provide for modification.
17. Be written in standard source language.

Specify required TRD output format to allow for a standardize non-hard copy output (such as tape, disk, modem, etc.).

- Provide a standardized electronic media output of the TRD, simulation data, and possible ATE equipment, will allow the TRD to be expanded and become the documentation of TPS activities. This will eliminate duplicated efforts currently required as a part of the TRD and TPS. This approach will result in multiple release of the TRD. The early releases will be usable for TPS bidding, UUT descriptions and interfaces, and later releases representing a complete documentation of the UUT tests. By preserving the electronic media files they can be modified and used for development of the Technical Order without duplicating the data gathering, simulation, description of test procedures already defined. The controlling specifications for all three activities will be impacted by the use of an automated approach.

The revised Mil-Specification must define and control:

- The content, control, approval and distribution of each release of the TRD
- The standardization of hardware and software interfaces
- The revision, addition and summaries for each release
- The controlling agency responsible for the integrity of the TRD
- The area where specification deviations are permissible

IMPLEMENTATION OF CHANGE - The TRD specification changes listed above are needed for an automated process. These techniques could be applied to areas which are still under development. By redefining a specification for automated TRD development in the near future the specification would also act as a guide for the development of the automated process.

### 5.3.2 Develop And Modify TRD Process Hardware

Interface CAE networks with other resources.

Progressing from the existing configuration which consists of specialized simulators, general purpose computers, TRD document generators, and the near future system which is centered around a CAE workstation with expanded computer capabilities; requires utilizing links to simulators and TRD document generators. All of the technology required to accomplish this configuration is currently in use, or has been introduced in the marketplace. Implementation involved purchasing and linking the resources. Figure 5-1 depicts one of a variety of combinations which could provide the needed capability.



Provide link to a large variety of commercial and government simulators via global data base networks.

The hardware configuration recommended for the future configuration illustrated in Table 5-2, is a networked system with capabilities far beyond the anticipated needs of a TRD development. However, the configuration is required to provide computational, and special purpose hardware when needed.

Develop high-speed main-frame computer and hardware simulators for simulation of large complex circuits.

Large complex circuits require high-speed main-frame computers for simulation and the possibilities of special hardware techniques was not established in this program. The approach considered feasible was to anticipate development of interfaces and standard hardware which will enable resource selection and application on a shared basis. As networks capabilities are expanded computer services will be available on a rental and contract basis allowing utilization of hardware which could not be justified for TRD development effort.

### 5.3.3 Develop and Modify TRD Process Software

Software needed to develop TRDs on CAE system requires application of a variety of specialized programs, such as listed in matrices are readily available and currently in use. The near future system will use existing software with the only improvements needed in the interface area. Software exists for the digital, analog and electro-mechanical analysis; networking, data base application, AI, testability, document generation and CAE. With the advent of the 32-bit computer for the CAE workstation level it is feasible to use large varieties of software and provide a user friendly interface to all capabilities needed for TRD development. Software needed to accomplish near future goals is a simple modification to the CAE operating software that allows additional routines to be used and some special purpose interface routines to be developed. This new software can be divided into the following parts:

Data base routine to access logistics, engineering and contract administration's data bases (CALS, etc.).

Data gathering being one of the most labor-intensive area automating this activity presents several problems. The data gathering activities can only be automated if the data is resident in a data base and the operator can access it. Engineering and Logistics data is available and can be accessed if a routine resides in the data base program to allow access. Contract data and preliminary design data may be available but should be already known by the designer, if the designer is responsible for TRD development he can insert the needed information eliminating the need to gather the data a second time.

Resident data base routines, embedded in Logistics, Engineering and contract data bases to allow the CAE station access to specific items for the Automated Test Requirement Document Generation.

Develop software required to achieve the specified interfaces for Data Base and TRD output.

Simulator/CAE interface program to allow simulator data to be transferred to the CAE workstation. The TRD document generator/CAE workstation interface to allow data to be transferred to the document generator for output.

Forms of the above programs have been developed and are used to accomplish some of these tasks; however, the variety of computers operating systems and source code has created a need for different routines to be written for each application, as illustrated in the data base matrix.

Further development of simulators for complex digital, analog, hybrid and electro-mechanical UUTs.

Another labor intensive area is simulation which is partially automated. The simulation of Analog, Hybrid and EM require development of new techniques. Some capabilities have been around for years but they are not widely used and do not provide the fault analysis capabilities required for TRD development. This area requires a great deal of future study such as:

Analog Signal Generator  
Analog Fault Analysis Program  
Complex Circuit Analysis Technique  
Data transfer between the existing programs.

Define and develop the executive programs to create the ATRDG.

TRD development on a CAE station is closely related to UUT design and can best be accomplished by the designer with an automated process.

The approach best suited for this set of conditions is to develop a framework program which will provide capabilities listed above under "Interface CAE networks with other resources".

To accomplish these items standard interfaces should be created which will allow large quantities of existing software to be modified to interface with the standard. New software should be written with the standard in mind. Software exists which allows computers with different operating systems to be interfaced. This will allow special purpose hardware and software to be used with a minimal amount of additional programming.

Resource selection includes analyzing the task being performed to identify the optimum solution. This will use a knowledge-base approach to evaluate the type and size of circuit simulators from the software available; resource workload; effort required to complete, if the task can be divided among available resources; and if other related tasks can be run in parallel.

1. Select the optimum resource available for the specific task.
2. Select the most appropriate simulator.
3. Allow the inclusion of commercial hardware and software as it is developed.

4. Perform all required tasks with little or no operator intervention.
5. Develop a TRD in a background mode.

#### 5.3.4 Incorporate Emerging Technology

##### Incorporate expert system techniques into the ATRDG shell and simulation

Artificial Intelligence is currently being applied by Rockwell to the maintenance cycle on the (Central Integrated Test System (CITS)) Expert Parameter System (CEPS) and Expert Missile Maintenance Aid (EMMA) programs. AI is also being successfully applied to TRD development by several companies. By including these techniques to the automated TRD process, TRD development by the designer is feasible.

Application of AI (Expert Systems) techniques can reduce operator involvement in the resource selection, data handling and test sequencing required for the TRD, AI is being used to perform tasks similar to B-1B, EMMA and other current military contracts.

To develop a fully Automated TRD Document Generator the Application of Expert System to the following area warrants investigation.

Data Management

Test Strategy

Resource Selection

.Automatic Pattern Generation of Analog and Digital (Sequential) Circuits

#### 5.3.5 Further Development of Simulators

##### Improve automatic pattern generator to handle sequential circuits

Interactive pattern generation resulting from the analysis of results from previous steps is necessary and must be performed rapidly to minimize simulator time. AI techniques may provide a solution to this problem.

##### Enhance simulation capability of complex digital, analog, hybrid and electro-mechanical UUTs

Analysis techniques used for simple digital circuits do not work well in other environments due to the signal complexity and faults which cannot be identified as simple pass/fail designators. Long run times required for most simulations has precluded application of design simulators for TRD development. Approaches such as those used for testability analysis has not developed to the point of providing test patterns but is an area which can be further explored as a feasible application.

## APPENDIX A

### LITERATURE SEARCH LISTING

The following are literature acquired during the survey phase of the study to identify the automated tools and aids necessary for an automated TRD process. The data were entered sequentially as they were acquired and sorted for applicability to this study. Articles not pertinent to this effort were excluded from the list. Consequently, there are numbers missing in the listings.

The listing provides the name of the author, subject, publication, date and an evaluation numbers. The alphanumeric evaluation code can be found in Figure 2-2 and Figure 2-3

2. Donald E. Block, "MICROPROCESSOR-BASED TURNKEY SYSTEM SOLVES DOCUMENTATION PROBLEMS", Design News, 08Apr85, (A2, B, C1, D3, E1, E8, G2, H2, I1, J, K)
4. Edward J. McCluskey, "BUILT-IN SELF-TEST TECHNIQUES", IEEE Design & Test, 01Apr85, (A5, B, C1, D3, E5, G2, H2, I3, J, K)
5. Edward J. McCluskey, "BUILT-IN SELF-TEST STRUCTURES", IEEE Design & Test, 01Apr85, (A5, B, C1, D3, E5, G2, H2, I3, J, K)
6. John P. Hayes, "FAULT MODELING", IEEE Design & Test, 01Apr85, (A5, B4, B5, C1, D3, E5, G2, H4, I3, J1, K)
8. David I. Smith, "CATS: PRECURSOR TO AEROSPACE EXPERT SYSTEMS?", Aerospace America, 01Apr85, (A3, B, C2, D3, E2, G1, H2, I3, J6, K)
9. Michael Franz, "INPUT VECTORS DRIVE SIMULATION OF LOGIC-ARRAY DESIGN", EDN, 13Jun85, (A5, B4, B5, C1, D2, E5, G2, H2, I3, J1, K)
10. Michael Franz, "USE SIMULATION VECTORS TO GENERATE TEST VECTORS", EDN, 27Jun85, (A5, B4, B5, C1, E5, G2)
14. Vincent G. Calfapietra, "THE ARMY'S ATE FOR ELECTRONIC SYSTEMS", Test & Measurement World, 01May85, (A5, B, C1, D3, E5, G2, H2, I3, J, K)
21. Dwight B. Davis, "STRATEGIC COMPUTING INITIATIVE", High Technology, 01Apr85, (A1, B, C1, D3, E3, G2, H2, I3, J, K)
25. Julie Pingry, Senior Editor, "EFFICIENT COMMUNICATION ELUDES DESIGN NETWORKS", Digital Design, 01Apr85, (A2, B3, B4, B5, C1, D3, E1, E4, G2, H3, I3, J, K)
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28. A.F. Murray & P.B. Denyer, "TESTABILITY AND SELF-TEST IN NMOS AND CMOS VLSI SIGNAL PROCESSOR", IEEE Proceedings, Vol. 132, 01Jun85, (A5, B4, B5, C2, D3, E5, G2, H2, I3, J1, K)

30. C.R. Shashidhar & F.P. Coskley, "FAULT DIAGNOSIS OF SPC SWITCH SYSTEMS BASED ON STRUCTURE AND SIGNALLING", Software & Microsystems, 01Apr85, (A5, B, C1, D3, E5, G2, H2, I3, J, K)
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477. Richard Goering, "SIMULATION CHALLENGES BREADBOARDING FOR DESIGN VERIFICATION", Computer Design, 15Jun86, (A5, B4, B5, C1, D2, E5, G2, H2, I3, J1, K)

478. Michael Bloom, "ACCELERATORS BREAK BOTTLENECKS IN LOGIC AND FAULT SIMULATION", Computer Design, 15May86, (A5, B4, B5, C1, D2, E5, G2, H2, I3, J1, K)
479. Unknown, "ACCELERATOR BUASTS 200 BILLION GATE EVALUATIONS/S", Computer Design, 01Aug86, (A5, B4, B5, C1, D2, E5, G2, H2, I3, J1, K)
480. Bob Milne, "ADVANCED SOFTWARE IMPROVES SILICON LAYOUT AND SHARPLY RAISES SIMULATION EFFICIENCY", Electronic Design, 12Jun86, (A5, B, C1, D2, E5, G2, H2, I3, J, K)
481. Unknown, "SOFTWARE INTEGRATES CAE AND ATE", Electronics Test, 01Jul86, (A5, B, C1, D2, E5, G2, H2, I3, J, K)
482. Jean - Noel Lebrun and Raffy Goshen, "SPICE IMPROVEMENTS EASE ANALOG SIMULATION", Computer Design, 01Aug86, (A5, B3, C1, D2, E5, G2, H2, I3, J2, K)
483. Jeffery T. Deutsch, Thomas D. Lovett, and Michael L. Squires, "PARALLEL COMPUTING FOR VLSI CIRCUIT SIMULATION", VLSI Systems Design, 01Jul86, (A5, B3, C1, D2, E5, G2, H2, I3, J2, K)
484. Greg Barros, "A SURVEY OF CIRCUIT SIMULATION PROGRAMS", VLSI Systems Design, 01Jul86, (A5, B3, C1, D2, E5, G2, H2, I3, J2, K2, K3)
485. David Brock, "BOARD TEST MIRRORS SYSTEMS TEST", Electronics Test, 01Apr86, (A5, B, C1, D3, E5, G2, H4, I3, J, K1)
486. Stephen F. Scheiber, "COMPUTER-AIDED CIRCUIT DESIGN AND TEST - BRIDGING THE GAP", Test & Measurement World, 01Mar86, (A5, B, C1, D3, E5, G2, H2, I3, J, K)
487. Nicolas Mokhoff, Senior Editor, "FIBER OPTICS POINTS WAY TO SPEED DIVERGENT NETWORKS", Computer Design, 01Aug86, (A2, B, C1, D3, E4, G2, H4, I3, J, K)
488. Nicolas Mokhoff, Senior Editor, "PC'S AND LAN S REVOLUTIONIZE THE OFFICE", Computer Design, 01Jul86, (A2, B, C3, D3, E2, E4, G2, H4, I3, J, K)
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490. Roger Allan, "INEXPENSIVE LAN CONNECTIONS CUT NETWORKING COSTS", Electronic Design, 17Apr86, (A2, B, C1, D3, E4, G2, H4, I3, J, K)
491. Unknown, "GATEWAY TO ETHERNET ON ONE CONTROLLER BOARD", Electronic Design, 17Library - (C)Copyright Microsoft Corp 1986?86, (A2, B, C1, D3, E4, G2, H4, I3, J, K)
492. Robert B. Mills, "PUTTING FACTORY NETWORKS TO WORK", CAE, 01Jan86, (A2, B, C1, D3, E4, G2, H4, I3, J, K)

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494. Ray Weiss, "POWERFUL UNIX - BASED WORKSTATIONS TAKE ON MINICOMPUTERS, MAINFRAMES", Electronic Design, 15May86, (A2, B, C1, D3, E7, G2, H2, I3, J, K)
495. Unknown, "HIERARCHICAL AND CONCURRENT FAULT SIMULATION", Electronics Test, 15Library - (C)Copyright Microsoft Corp 1986?86, (A5, B4, B5, C1, D2, E5, G2, H2, I3, J1, K)
496. Unknown, "WORKSTATION", EDN, 25Dec86, (A2, B, C1, D3, E7, G2, H2, I3, J, K)
497. Unknown, "CAE WORKSTATIONS", EDN, 25Dec86, (A5, B, C1, D3, E1, E7, G2, H2, I3, J, K)
498. Unknown, "DOCUMENT EDITOR", EDN, 25Dec86, (A2, B, C1, D1, E1, E3, G2, H2, I1, J, K)
499. Unknown, "ANALOG CAE BROCHURE AND VIDEOTAPE", EDN, 25Dec86, (A5, B3, C2, D3, E5, G2, H2, I3, J2, K)
500. Nicolas Mokhoff, Senior Editor, "RISK'S AND PARALLEL PROCESSORS DRIVE MULTIPROCESSING INNOVATIONS", Computer Design, 01Dec86, (A2, B, C1, D1, E7, G2, H2, I1, J, K)
501. Richard Goering, Senior Editor, "PRICE AND PERFORMANCE IMPROVEMENTS DRIVE DESIGN TOOL MARKET", Computer Design, 01Dec86, (A2, B, C2, D3, E1, G2, H2, I2, J, K)
502. Unknown, "DESKTOP WORKSTATIONS CHALLENGE MINICOMPUTERS", Computer Design, 01Dec86, (A2, B, C2, D3, E7, G2, H2, I3, J, K)
503. Unknown, "SYSTEM ACCELERATES LOGIC AND FAULT SIMULATION IN SOFTWARE", Computer Design, 01Dec86, (A5, B4, B5, C1, D2, E5, G2, H2, I3, J1, K)
504. Unknown, "SCHEMATIC PACKAGE SETS PRICE/PERFORMANCE STANDARD FOR PC-BASED CAD", Computer Design, 01Dec86, (A5, B, C1, D3, E1, G2, H2, I2, J, K)
505. Unknown, "SIMULATION ENGINE TAILORED TO SMALL- AND MEDIUM- SIZE DESIGNS", Computer Design, 01Dec86, (A5, B4, B5, C1, D2, E5, G2, H2, I3, J1, K2, K3)
506. Unknown, "LOW - COST 32-BIT GRAPHICS WORKSTATIONS DELIVER 5-MIPS INSTRUCTION EXECUTION", Computer Design, 01Dec86, (A2, B, C1, D2, E7, G2, H2, I3, J, K)
507. Unknown, "SIMULATION ENVIRONMENT HANDLES ANALOG/DIGITAL DESIGNS", Computer Design, 01Jan87, (A5, B3, B4, B5, C2, D2, E5, G2, H2, I3, J1, J2, K)
508. Richard Goering, Senior Editor, "UNIX COPROCESSOR SYSTEM MAY REVOLUTIONIZE PC - BASED CAE/CAD", Computer Design, 01Jan87, (A2, B, C2, D3, E3, G2, H2, I2, J, K)

509. Richard Goering, Senior Editor, "FAULT SIMULATION STRIVES FOR DESIGNER ACCEPTANCE", Computer Design, 01Jan87, (A5, B, C2, D2, E5, G2, H2, I3, J, K)
510. Unknown, "IBM 580 EMULATION UNITES WORKSTATIONS AND MAINFRAMES", Computer Design, 15Nov86, (A2, B, C1, D3, E5, G2, H2, I3, J, K)
511. Mike Waters, "EDIF VERSION 200 TAKES ON PRODUCTION ENVIRONMENT", Computer Design, 15Nov86, (A2, B, C1, D1, E8, G2, H2, I1, J, K)
512. J.F. Petersen and S.L. Picus, "UNIX ENVIRONMENT OFFERS FLEXIBLE I/O DESIGN", Computer Design, 15Nov86, (A5, B, C1, D2, E5, G2, H2, I3, J, K)
513. Doug Johnson, "ANALOG SIMULATOR MODELS MULTITECHNOLOGY SYSTEMS", Computer Design, 15Nov86, (A5, B3, C2, D2, E5, G2, H2, I3, J2, K)
514. David W. Daugherty, "DIVIDE AND RULE: CAE TOOLS CONQUER DESIGN TASKS", Electronics Test, 01Dec86, (A5, B3, C2, D3, E1, G2, H2, I3, J2, K)
515. Michael Bloom, "MIXED - MODE SIMULATORS BRIDGE THE GAP BETWEEN ANALOG AND DIGITAL DESIGN", Computer Design, 15Jan87, (A5, B3, B4, B5, C2, D2, E5, G2, H2, I3, J1, J2, K)
516. Unknown, "ANALOG SIMULATION", EDN, 27Nov86, (A5, B3, C2, D2, E5, G2, H2, I3, J2, K)
517. Unknown, "LISP DEVELOPMENT", EDN, 27Nov86, (A3, B, C2, D3, E2, G2, H2, I3, J6, K)
518. Ernest Meyer, "DESIGN VERSUS AUTOMATION", VLSI Systems Design, 01Jan87, (A5, B4, B5, C2, D3, E1, E2, G2, H1, I3, J1, K)
519. Sanjeev Aggarwal, Thomas Deakins, Fumio Taku, Carol Tegnell, "ELECTRONIC DESIGN AUTOMATION: ISSUES AND TRENDS", VLSI Systems Design, 01Jan87, (A5, B, C1, D3, E1, G2, H1, I3, J, K)
520. Cindy Thames, Andrew S. Rappaport, "GET READY FOR CAE PERSONALIZATION", VLSI Systems Design, 01Jan87, (A2, B, C1, D3, E1, G2, H2, I3, J, K)
521. Ralph Marlett, "AUTOMATED TEST GENERATION FOR INTEGRATED CIRCUITS", VLSI Systems Design, 01Jan87, (A2, B5, C1, D3, E5, G2, H2, I3, J1, K3)
522. Peter Odryna, Sani Nassif, "THE ADEPT TIMING SIMULATION ALGORITHM", VLSI Systems Design, 01Jan87, (A5, B, C2, D3, E5, G2, H2, I3, J, K)
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524. William E. Den Beste, "TOOLS FOR TEST DEVELOPMENT", VLSI Systems Design, 01Jan87, (A2, B, C1, D3, E1, E5, G2, H2, I3, J, K)
525. Lori Valigra, "WORKSTATIONS EDGE OUT TERMINALS", Digital Review, 09Feb87, (A2, B, C1, D3, E1, G2, H2, I3, J, K)

526. Dr. George Schussel, Dr. Carma McClure, Pieter Mimno, "COMPUTER AIDED SOFTWARE ENGINEERING SYMPOSIUM", Digital Consulting, Inc. Seminar, 24Feb87, (A3, B, C2, D3, E2, G2, H2, I3, J6, K)
527. Lawrence H. Goldstein, "CONTROLLABILITY/OBSERVABILITY ANALYSIS OF DIGITAL CIRCUITS", copy from Sandia Labs, 24Library - (C)Copyright Microsoft Corp 1986?87, (A5, B4, B5, C1, D3, E5, G2, H2, I3, J1, K)
528. Kristen Wells, "VALIDTOOLS PORTED TO DEC VAX-STATIONS", Validator Issue No 8, 01Aug86, (A2, B4, B5, C1, D3, E5, G2, H2, I3, J1, K)
529. Chris Everett, "SCAN-PATH TOOLS SPEED THE CONVERSION OF YOUR DESIGN INTO A TESTABLE CHIP", EDN, 04Mar87, (A5, B4, B5, C1, D3, E5, G2, H2, I3, J1, K)
530. Margery Conner, "GRAPHICS ENGINES", EDN, 04Mar87, (A2, B, C1, D3, E1, G2, H2, I2, J, K)
531. Karl J. Huenne, "PARTITION CUSTOM IC'S ALONG TECHNOLOGY LINES", EDN, 04Mar87, (A5, B3, C2, D3, E5, G2, H2, I3, J2, K)
532. Wayne Howe, "ENHANCED DATA ANALYSIS TOOL OFFERS WINDOWING, ANALOG-DIGITAL CONVERSION", News/Software, 10Nov86, (A2, B, C1, D3, E1, E5, E7, G2, H2, I, J1, J2, K)
533. Gary R. Martins, "AI: THE TECHNOLOGY THAT WASN'T", Defense Electronics, 01Dec86, (A3, B, C2, D3, E2, G1, H2, I3, J6, K)
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537. Collett, "BEHAVIORAL MODELS SIMPLIFY SYSTEM SIMULATION", Digital Design, 01Nov86, (A5, B5, C1, D2, E5, G2, H2, I3, J1, K)
538. Stan Stringfellow & Bruce Sherman, "ADA FINDS A REAL-TIME HOME", Digital Design, 01Nov86, (A2, B, C2, D3, E3, G2, H2, I3, J, K)
539. Athanasios Kalekos, "CAE/CAD DATABASES: WHAT TO LEAVE IN, WHAT TO LEAVE OUT", Digital Design, 01Nov86, (A2, B, C1, D3, E1, G2, H2, I2, J, K)
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541. Unknown, "GRAPHICS TOOL KIT", EDN, 04Mar87, (A2, B, C1, D3, E1, G2, H2, I2, J, K)

542. Unknown, "TWO APPROACHES TO MIXED-MODE SIMULATION", VLSI Systems Design, 01Nov86, (A5, B3, C2, D2, E5, G2, H2, I3, J2, K)
543. K.C. Kmack and T.L. Weaver, "CONNECTING DISSIMILAR CONTROLLERS AND LAN'S", Control Engineering, 01Oct85, (A2, B, C1, D3, E4, G2, H4, I3, J, K)
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545. Unknown, "GATEWAY SALES LITERATURE", N/A, 26Dec86, (A5, B4, B5, C1, D3, E5, G2, H2, I3, J1, K)
546. Unknown, "TEKTRONIX SALES LITERATURE", N/A, 01Jan87, (A5, B4, B5, C1, D3, E5, G2, H2, I3, J1, K)
547. Unknown, "SILICON DESIGN LABS SALES LITERATURE", N/A, 01Jan87, (A5, B4, B5, C1, D3, E5, G2, H2, I3, J1, K)
548. Unknown, "SILVAR LISCO SALES LITERATURE", N/A, 01Jan87, (A5, B4, B5, C1, D3, E5, G2, H2, I3, J1, K)
549. Unknown, "SIMUCAD SALES LITERATURE", N/A, 01Jan87, (A5, B4, B5, C1, D3, E5, G2, H2, I3, J1, K)
550. Unknown, "SRITEK SALES LITERATURE", N/A, 01Jan87, (A2, B, C1, D3, E7, G2, H2, I3, J, K)
551. Unknown, "ELECTRICAL ENGINEERING SOFTWARE SALES LITERATURE", N/A, 01Jan87, (A2, B4, B5, C1, D3, E5, G2, H2, I3, J1, K)
552. Unknown, "HEWLETT PACKARD SALES LITERATURE", N/A, 01Jan87, (A2, B, C1, D3, E5, G2, H2, I3, J, K)
553. Unknown, "ANALOGY SALES LITERATURE", N/A, 01Jan87, (A2, B3, C1, D3, E5, G2, H2, I3, J2, K)
554. Unknown, "ANALOG DESIGN TOOLS SALES LITERATURE", N/A, 01Jan87, (A2, B3, C1, D3, E5, G2, H2, I3, J2, K)
555. Unknown, "DEC SALES LITERATURE", N/A, 01Jan87, (A2, B, C1, D3, E5, G2, H2, I3, J, K)
556. Unknown, "PHOENIX SALES LITERATURE", N/A, 01Jan87, (A2, B, C1, D3, E5, G2, H2, I3, J, K)
557. Unknown, "TERADYNE SALES LITERATURE", N/A, 01Jan87, (A2, B, C1, D3, E5, G2, H2, I3, J, K)
558. Unknown, "SUN SALES LITERATURE", N/A, 01Jan87, (A2, B, C1, D3, E5, G2, H2, I3, J, K)
559. Unknown, "MENTOR GRAPHICS SALES LITERATURE", N/A, 01Jan87, (A2, B4, B5, C1, D3, E5, G2, H2, I3, J1, K)



560. Unknown, "DAISY SALES LITERATURE", N/A, 01Jan87, (A2, B4, B5, C1, D3, E5, G2, H2, I3, J1, K)
561. Unknown, "HHB SALES LITERATURE", N/A, 01Jan87, (A2, B4, B5, C1, D3, E5, G2, H2, I3, J1, K)
562. Unknown, "GAI SALES LITERATURE", N/A, 01Library - (C)Copyright Microsoft Corp 1986?87, (A2, B, C1, D3, E5, G2, H2, I3, J, K)
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564. A. Jesse Wilkinson, "BENCHMARKING AN EXPERT SYSTEM FOR ELECTRONIC DIAGNOSIS", IEEE 1986 Int. Test Conference, 01Library - (C)Copyright Microsoft Corp 1986?87, (A3, B, C1, D3, E2, G2, H2, I3, J6, K)
565. Ken Olsen, "THE DIFFERENTIAL COPY", Technology Assessment Group Inc., 01Nov86, (A2, B, C1, D3, E3, G2, H2, I3, J, K)
566. Martin Gold, "ANALOG DESIGN TOOLS BYPASS SPICE PROBLEMS", Electronic Design, 05Mar87, (A5, B3, C1, D2, E5, G2, H2, I3, J2, K)
567. Unknown, "AUTO-TRON SALES LITERATURE", N/A, 01Jan87, (A5, B, C1, D2, E5, G2, H2, I3, J, K)
568. Unknown, "PAWS SALES LITERATURE", N/A, 01Jan87, (A5, B, C1, D2, E5, G2, H2, I3, J, K)
569. Douglas A Vander Heide, "TAD SALES LITERATURE", N/A, 01Jan87, (A2, B, C1, D2, E7, G2, H2, I3, J, K)
570. N/A, "TDA SALES LITERATURE", N/A, 01Jan87, (A5, B2, B3, B4, B5, C1, D2, E5, G2, H2, I3, J1, J2, J3, K)
571. N/A, "SYSCAP SALES LITERATURE", N/A, 01Jan87, (A5, B3, C1, D2, E5, G2, H2, I3, J2, K)
572. N/A, "SMART SALES LITERATURE", N/A, 01Jan87, (A2, B, C1, D3, E3, G2, H2, I3, J, K)
573. N/A, "DORIS SALES LITERATURE", N/A, 01Jan87, (A3, B, C1, D3, E2, G2, H2, I3, J6, K)
574. N/A, "CADSAL SALES LITERATURE", N/A, 01Jan87, (A5, B, C1, D2, E5, G2, H2, I3, J, K)
575. N/A, "CAFIT SALES LITERATURE", N/A, 01Jan87, (A5, B, C1, D2, E5, G2, H2, I3, J, K)

## APPENDIX B MATRIX DATA

The data base contains items gathered during the Survey phase of the contract. This data was assigned sequential numbers and filed in the order received. The data base lists key elements and a summary for each data item. Any of these elements can be selected as a basis for sorting. Evaluation of the data by sorting this limited amount of information was unsatisfactory; therefore, matrices were developed which contained data base items that were judged to satisfy the basic requirements of an automated process (ie. compatible hardware & software, user able to modify input, output and control of the software, language common with other needed capabilities).

The areas of primary interest were cost, value, compatibility, resource, effectiveness, technology limits, and CAD applicability. Data base items sometimes discuss specific issues which had to be related to a complete description of a method before an evaluation was possible.

When seven or more data base items discussed the same topic, they were listed in a matrix for comparison with items listed in other matrices. By using a matrix it was possible to categorize, compare and analyze information contained in the articles. The articles usually discussed a key feature of a system. Frequently it was necessary to group information from several articles in order to obtain a composite of the systems capabilities.

Based on the aforementioned criteria a matrix for AI Simulator, Analog Simulator, CAE Workstation and Digital Simulator was developed. The matrices are presented below:

### AI SIMULATOR

---

|                     |   |
|---------------------|---|
| REF NO:             | 1   |
| AI SIMULATOR:       | ART   |
| COMPANY:            | INFERENCE CORP.   |
| WORKSTATIONS:       | SUN-3(UNIX), (LMI, SYMBOLICS, TI) LISP MACHINES,<br>VAX(UNIX) |
| LANGUAGE:           | LISP, C   |
| RULE TYPES:         | INFERENCE, HYPOTHESIS, CONSTRAINT, BELIEF,                    |
| PRODUCTION          |   |
| RULE FIRING:        | FORWARD & BACKWARD CHAINING, HYPOTHETICAL                     |
| REASONING,          |   |
| DESCRIPTION,        | FEATURE & LANGUAGE INTEGRATION, OBJECT                        |
|                     | EMBEDDED  |
| FEATURES:           | NON-MONOTONIC, EXPLANATION, FACTS LISTS                       |
| FRAME TYPES:        | DECLARATIVE, PROCEDURAL, ASPECTS, TYPES, GRAPHICS             |
| COST:               | 60-80 K STATE OF ART: NEAR FUTURE                             |
| CAD CAE COMPATIBLE: | YES PROPRIETARY: YES  |

MATRIX DATA CONTINUED

|                     |  |                           |
|---------------------|--|---------------------------|
| REF NO:             | 2  |                           |
| AI SIMULATOR:       | KEE  |                           |
| COMPANY:            | INTELLICORP  |                           |
| WORKSTATIONS:       | (SYMBOLICS, LMI, TI, PC, XEROX) LISP MACHINES,<br>VAX(UNIX)                                  |                           |
| LANGUAGE:           | LISP   |                           |
| RULE TYPES:         | INFERENCE, HYPOTHESIS, CONSTRAINT, BELIEF,   |                           |
| PRODUCTION          |  |                           |
| RULE FIRING:        | FORWARD & BACKWARD CHAINING, OBJECT DESCRIPTION,<br>FEATURE & LANGUAGE INTEGRATION, EMBEDDED |                           |
| FEATURES:           | FACTS LISTS, ASSERTIONS, NON-MONOTONIC, EXPLANATION  |                           |
| FRAME TYPES:        | DECLARATIVE, PROCEDURAL, ASPECTS, TYPES, GRAPHICS  |                           |
| COST:               | 60 K   | STATE OF ART: NEAR FUTURE |
| CAD CAE COMPATIBLE: | YES  | PROPRIETARY: YES          |
| REF NO:             | 3  |                           |
| AI SIMULATOR:       | RULEMASTER   |                           |
| COMPANY:            | RADIAN CORP.   |                           |
| WORKSTATIONS:       | SUN(UNIX), APOLLO(UNIX), VAX(UNIX), IBM PC AT  |                           |
| LANGUAGE:           | C  |                           |
| RULE TYPES:         | INFERENCE, PRODUCTION  |                           |
| RULE FIRING:        | FORWARD & BACKWARD CHAINING  |                           |
| FEATURES:           | ASSERTIONS, FUZZY LOGIC, RULE LEARNING, EXPLANATION  |                           |
| FRAME TYPES:        | N A  |                           |
| COST:               | 1-17 K   | STATE OF ART: NEAR FUTURE |
| CAD CAE COMPATIBLE: | YES  | PROPRIETARY: YES          |
| REF NO:             | 4  |                           |
| AI SIMULATOR:       | DUCK   |                           |
| COMPANY:            | SMART SYSTEMS TECH.  |                           |
| WORKSTATIONS:       | IBM & VAX MAINFRAMES, IBM PC AT, SYMBOLICS MACHINES  |                           |
| LANGUAGE:           | NLISP  |                           |
| RULE TYPES:         | INFERENCE, PRODUCTION  |                           |
| RULE FIRING:        | FORWARD & BACKWARD CHAINING  |                           |
| FEATURES:           | ASSERTIONS, NON-MONOTONIC, EXPLANATION   |                           |
| FRAME TYPES:        | N/A  |                           |
| COST:               | 6 K  | STATE OF ART: NEAR FUTURE |
| CAD CAE COMPATIBLE: | YES  | PROPRIETARY: YES          |
| REF NO:             | 5  |                           |
| AI SIMULATOR:       | KNOWLEDGE ENGINEERING SYSTEM II  |                           |
| COMPANY:            | SOFTWARE ARCHITECTURE & ENGINEERING  |                           |
| WORKSTATIONS:       | IBM PC/XT-AT, VAX(UNIX), APOLLO(UNIX)  |                           |
| LANGUAGE:           | LISP, C  |                           |
| RULE TYPES:         | HYPOTHESIS, PRODUCTION, BAYESIAN   |                           |
| RULE FIRING:        | FORWARD & BACKWARD CHAINING  |                           |
| FEATURES:           | FACTS LISTS, EXPLANATION   |                           |
| FRAME TYPES:        | DECLARATIVE, ASPECTS   |                           |
| COST:               | 4 K  | STATE OF ART: NEAR FUTURE |
| CAD CAE COMPATIBLE: | YES  | PROPRIETARY: YES          |

MATRIX DATA CONTINUED

REF NO: 6  
 AI SIMULATOR: M.1  
 COMPANY: TEKNOLEDGE CORP.  
 WORKSTATIONS: IBM PC/XT-AT  
 LANGUAGE: C  
 RULE TYPES: INFERENCE, BELIEF  
 RULE FIRING: BACKWARD CHAINING, LANGUAGE INTEGRATION  
 FEATURES: FACTS LISTS, EXPLANATION  
 FRAME TYPES: N A  
 COST: 5 K STATE OF ART: NEAR FUTURE  
 CAD CAE COMPATIBLE: YES PROPRIETARY: YES

REF NO: 7  
 AI SIMULATOR: S.1  
 COMPANY: TEKNOLEDGE CORP.  
 WORKSTATIONS: IBM PC AT, SUN(UNIX), VAX(UNIX), IBM/VM MAINFRAME,  
 LISP MACHINES  
 LANGUAGE: LISP, C  
 RULE TYPES: INFERENCE, PRODUCTION  
 RULE FIRING: BACKWARD CHAINING, FEATURE & LANGUAGE INTEGRATION,  
 OBJECT DESCRIPTION  
 FEATURES: EXPLANATION  
 FRAME TYPES: DECLARATIVE, PROCEDURAL, TYPES  
 COST: 25-45 K STATE OF ART: NEAR FUTURE  
 CAD CAE COMPATIBLE: YES PROPRIETARY: YES

REF NO: 8  
 AI SIMULATOR: PERSONAL CONSULTANT PLUS  
 COMPANY: TEXAS INSTRUMENTS  
 WORKSTATIONS: TI & IBM PC  
 LANGUAGE: LISP  
 RULE TYPES: PRODUCTION  
 RULE FIRING: BACKWARD CHAINING, FEATURE & LANGUAGE INTEGRATION,  
 OBJECT DESCRIPTION  
 FEATURES: N A  
 FRAME TYPES: GRAPHICS, EDITORS, MULTIPLE WINDOWS, RULE SYNTAX  
 COST: 3 K STATE OF ART: NEAR FUTURE  
 CAD CAE COMPATIBLE: YES PROPRIETARY: YES

REF NO: 9  
 AI SIMULATOR: KNOWLEDGE CRAFT  
 COMPANY: CARNEGIE GROUP INC.  
 WORKSTATIONS: (SYMBOLICS, LMI, TI, & OTHERS) LISP MACHINES,  
 VAX(UNIX)  
 LANGUAGE: LISP  
 RULE TYPES: INFERENCE, HYPOTHESIS, PRODUCTION  
 RULE FIRING: FORWARD & BACKWARD CHAINING  
 FEATURES: FACTS LISTS, NON-MONOTONIC, EXPLANATION  
 FRAME TYPES: DECLARATIVE, PROCEDURAL, ASPECTS, TYPES, GRAPHICS  
 COST: 50 K STATE OF ART: NEAR FUTURE  
 CAD CAE COMPATIBLE: YES PROPRIETARY: YES

MATRIX DATA CONTINUED

REF NO: 10  
 AI SIMULATOR: IN-ATE  
 COMPANY: AUTOMATED REASONING  
 WORKSTATIONS: MACINTOSH PC, (LMI, SYMBOLICS) MACHINES, VAX(UNIX)  
 LANGUAGE: ZETALISP, C  
 RULE TYPES: LAPLACIAN LEARNING, DEMPSTER-SHAFER, PRODUCTION  
 RULE FIRING: LOGIC MODELING  
 FEATURES: NON-MONOTONIC  
 FRAME TYPES: N A  
 COST: 2.5-15 K STATE OF ART: NEAR FUTURE  
 CAD CAE COMPATIBLE: YES PROPRIETARY: YES

REF NO: 11  
 AI SIMULATOR: NEXPERT-OBJECT  
 COMPANY: NEURON DATA  
 WORKSTATIONS: IBM PC AT  
 LANGUAGE: C  
 RULE TYPES: PRODUCTION, RULECLASSES  
 RULE FIRING: FORWARD AND BACKWARD CHAINING  
 FEATURES: NON-MONOTONIC  
 FRAME TYPES: OBJECTS  
 COST: 5 K STATE OF ART: NEAR FUTURE  
 CAD CAE COMPATIBLE: NO PROPRIETARY: YES

REF NO: 12  
 AI SIMULATOR: DORIS 2.0  
 COMPANY: ROCKWELL  
 WORKSTATIONS: SYMBOLICS, VAX WORKSTATIONS  
 LANGUAGE: COMMON LISP  
 RULE TYPES: INFERENCE, PRODUCTION  
 RULE FIRING: FORWARD AND BACKWARD CHAINING  
 FEATURES: DEPTH FIRST SEARCH  
 FRAME TYPES: OBJECTS  
 COST: PROPRIETARY STATE OF ART: NEAR FUTURE  
 CAD CAE COMPATIBLE: NO PROPRIETARY: YES

ANALOG SIMULATOR

---

REF NO: 13  
 ANALOG SIMULATOR: DSPICE (SPICE2)  
 COMPANY: DAISY SYSTEMS CORP.  
 ALGORITHMS USED: NEWTON-RALPHSON, LOWER/UPPER DECOMPOSITION,  
 TRAPEZOIDAL, BACKWARD EULER, GAUSSIAN ELIMINATION  
 INTERFACE: INTERACTIVE & BATCH  
 HARDWARE: VAX(UNIX), LOGICIAN  
 COST: 85 K STATE OF ART: PRESENT  
 CAD/CAE COMPATIBLE: YES PROPRIETARY: YES  
 SPICE COMPARISON: SPICE 2G.5

MATRIX DATA CONTINUED

REF NO: 14  
 ANALOG SIMULATOR: MSPICE (SPICE2)  
 COMPANY: MENTOR GRAPHICS CORP.  
 ALGORITHMS USED: LOWER/UPPER DECOMPOSITION, TRAPEZIODAL,  
 NEWTON-RALPHSON, BACKWARD EULER,  
 GAUSSIAN ELIMINATION  
 INTERFACE: INTERACTIVE  
 HARDWARE: APOLLO(AEGES)  
 COST: 7.1 K STATE OF ART: PRESENT  
 CAD/CAE COMPATIBLE: YES PROPRIETARY: YES  
 SPICE COMPARISON: SPICE 2G.6

REF NO: 15  
 ANALOG SIMULATOR: MSIMON (POWER SPICE)  
 COMPANY: MENTOR GRAPHICS CORP.  
 ALGORITHMS USED: TRAPEZOIDAL, ITERATIVE TIMING ANALYSIS,  
 LOWER/UPPER DECOMPOSITION, RELAXATION  
 INTERFACE: INTERACTIVE  
 HARDWARE: APOLLO(AEGES)  
 COST: 17.1 K STATE OF ART: PRESENT  
 CAD/CAE COMPATIBLE: YES PROPRIETARY: YES  
 SPICE COMPARISON: FASTER

REF NO: 16  
 ANALOG SIMULATOR: HSPICE  
 COMPANY: CALMA CO.  
 ALGORITHMS USED: LOWER/UPPER DECOMPOSITION, TRAPEZOIDAL,  
 NEWTON-RALPHSON, BACKWARD EULER,  
 GAUSSIAN ELIMINATION  
 INTERFACE: INTERACTIVE & BATCH  
 HARDWARE: APOLLO(AEGES)  
 COST: 15 K STATE OF ART: PRESENT  
 CAD/CAE COMPATIBLE: YES PROPRIETARY: YES  
 SPICE COMPARISON: SPICE2

REF NO: 17  
 ANALOG SIMULATOR: SABER  
 COMPANY: ANALOGY  
 ALGORITHMS USED: NEWTON-RALPHSON, GEAR 2 INTEGRATION, SPARSE MATRIX  
 INTERFACE: INTERACTIVE & BATCH  
 HARDWARE: SUN(UNIX), IBM(CMS), VAX(UNIX, VMS), APOLLO(AEGES)  
 COST: 9-65 K STATE OF ART: NEAR FUTURE  
 CAD/CAE COMPATIBLE: YES PROPRIETARY: YES  
 SPICE COMPARISON: TEN TIMES FASTER

MATRIX DATA CONTINUED

|                     |   |                           |
|---------------------|---|---------------------------|
| REF NO:             | 18  |                           |
| ANALOG SIMULATOR:   | PRECISE (SPICE2, SPICE3)  |                           |
| COMPANY:            | ELEC. ENG. SOFTWARE   |                           |
| ALGORITHMS USED:    | LOWER/UPPER DECOMPOSITION, TRAPEZOIDAL,<br>NEWTON-RALPHSON, BACKWARD EULER,<br>GAUSSIAN ELIMINATION |                           |
| INTERFACE:          | INTERACTIVE & BATCH   |                           |
| HARDWARE:           | SUN(UNIX), IBM(CMS), VAX(UNIX, VMS),  |                           |
| APOLLO(AEGES),      | ELXSI   |                           |
| COST:               | 10-70 K   | STATE OF ART: NEAR FUTURE |
| CAD/CAE COMPATIBLE: | YES   | PROPRIETARY: YES          |
| SPICE COMPARISON:   | FASTER  |                           |
| REF NO:             | 19  |                           |
| ANALOG SIMULATOR:   | SIMON (POWER SPICE)   |                           |
| COMPANY:            | ECAD  |                           |
| ALGORITHMS USED:    | LOWER/UPPER DECOMPOSITION, TRAPEZOIDAL,<br>ITERATIVE TIMING ANALYSIS                                |                           |
| INTERFACE:          | INTERACTIVE & BATCH   |                           |
| HARDWARE:           | VAX(VMS), APOLLO(AEGES), SUN(UNIX), ELXSI   |                           |
| COST:               | 15-45 K   | STATE OF ART: NEAR FUTURE |
| CAD/CAE COMPATIBLE: | YES   | PROPRIETARY: YES          |
| SPICE COMPARISON:   | FASTER  |                           |
| REF NO:             | 20  |                           |
| ANALOG SIMULATOR:   | LSIM (SMILE)  |                           |
| COMPANY:            | SILICON DESIGN LABS   |                           |
| ALGORITHMS USED:    | ADEPT TIMING, E-LOGIC, INTERACTIVE INTEGRATION  |                           |
| INTERFACE:          | INTERACTIVE   |                           |
| HARDWARE:           | SUN(UNIX), APOLLO(UNIX), VAX(UNIX,VMS)  |                           |
| COST:               | 40K PER STATION   | STATE OF ART: NEAR FUTURE |
| CAD/CAE COMPATIBLE: | YES   | PROPRIETARY: YES          |
| SPICE COMPARISON:   | FASTER  |                           |
| REF NO:             | 21  |                           |
| ANALOG SIMULATOR:   | SYSCAP  |                           |
| COMPANY:            | ROCKWELL  |                           |
| ALGORITHMS USED:    | DC-FAULT ANALYSIS, WORST CASE, PARAMETER  |                           |
| SENSITIVITY,        | MONTE CARLO   |                           |
| INTERFACE:          | INTERACTIVE & BATCH   |                           |
| HARDWARE:           | VAX(VMS), IBM(CMS), CDC   |                           |
| COST:               | 100K  | STATE OF ART: PRESENT     |
| CAD/CAE COMPATIBLE: | YES   | PROPRIETARY: YES          |
| SPICE COMPARISON:   | FASTER  |                           |

MATRIX DATA CONTINUED)

REF NO: 22  
 ANALOG SIMULATOR: ANALOG WORKBENCH(SPICE3)  
 COMPANY: ANALOG DESIGN TOOLS  
 ALGORITHMS USED: DC OPERATING POINT, NONLINEAR TRANSIENT,  
 FAST FOURIER TRANSFORM, NOISE FACTOR, LINEAR AC,  
 DC SWEEP  
 INTERFACE: INTERACTIVE  
 HARDWARE: SUN(UNIX), HP9000-320(UNIX), APOLLO(AEGES), IBM  
 PC AT  
 COST: 64K STATE OF ART: PRESENT  
 CAD/CAE COMPATIBLE: YES PROPRIETARY: YES  
 SPICE COMPARISON: SPICE3 COMPATIBLE

CAE WORKSTATION

REF NO: 23  
 CAE WORKSTATION: DOMAIN 3000  
 COMPANY: APOLLO COMPUTER INC.  
 CENTRAL PROCESSOR: 68020  
 LOCAL MEMORY: 2-4 M HARD DISK: 72 M  
 CLOCK RATE: 16.6 MHZ GRAPHIC SUPPORT: YES  
 PROPRIETARY: YES COST: 30 K  
 AUTO FAULT SIMULATION: NO MULTI USERS:

REF NO: 24  
 CAE WORKSTATION: VAXSTATION II  
 COMPANY: DIGITAL EQUIP CORP.  
 CENTRAL PROCESSOR: MICROVAX II  
 LOCAL MEMORY: 2-8 M HARD DISK: 31-71 M  
 CLOCK RATE: 16.6 MHZ GRAPHIC SUPPORT: NO  
 PROPRIETARY: YES COST: 21.6 K  
 AUTO FAULT SIMULATION: NO NO. USERS: 1-40

REF NO: 25  
 CAE WORKSTATION: RT-6150/1  
 COMPANY: IBM CORP.  
 CENTRAL PROCESSOR: RISK  
 LOCAL MEMORY: 1-4 M HARD DISK: 40-210 M  
 CLOCK RATE: 5.8 MHZ GRAPHIC SUPPORT: NO  
 PROPRIETARY: YES COST: 20-50 K  
 AUTO FAULT SIMULATION: NO NO. USERS:

REF NO: 26  
 CAE WORKSTATION: 3/260M  
 COMPANY: SUN MICROSYSTEMS INC.  
 CENTRAL PROCESSOR: 68020  
 LOCAL MEMORY: 8-32 M HARD DISK: 60-560 M  
 CLOCK RATE: 20 MHZ GRAPHIC SUPPORT: YES  
 PROPRIETARY: YES COST: 51-84 K  
 AUTO FAULT SIMULATION: NO NO. USERS:



MATRIX DATA CONTINUED

REF NO: 27  
 CAE WORKSTATION: LOGICIAN  
 COMPANY: DAISY  
 CENTRAL PROCESSOR: 80286, 80287  
 LOCAL MEMORY: 2-16 M  
 CLOCK RATE: 20 MHZ  
 PROPRIETARY: YES  
 AUTO FAULT SIMULATION: YES

HARD DISK: 40-140 M  
 GRAPHIC SUPPORT: YES  
 COST: 20 K  
 NO. USERS: 1-2

REF NO: 28  
 CAE WORKSTATION: HP9000 MODEL 320  
 COMPANY: HEWLETT PACKARD CO.  
 CENTRAL PROCESSOR: 68020  
 LOCAL MEMORY: 1-7.5 M  
 CLOCK RATE: 16.6 MHZ  
 PROPRIETARY: YES  
 AUTO FAULT SIMULATION: NO

HARD DISK: 16-4000 M  
 GRAPHIC SUPPORT: YES  
 COST: 20-40 K  
 NO. USERS: 25

REF NO: 29  
 CAE WORKSTATION: IDEA 1000  
 COMPANY: MENTOR GRAPHICS CORP.  
 CENTRAL PROCESSOR: 32 BIT VLSI  
 LOCAL MEMORY: 2-4 M  
 CLOCK RATE: 16.67 MHZ  
 PROPRIETARY: YES  
 AUTO FAULT SIMULATION: NO

HARD DISK: 50-167 M  
 GRAPHIC SUPPORT: YES  
 COST: 28-77 K  
 NO. USERS:

REF NO: 30  
 CAE WORKSTATION: SCALDSYSTEM  
 COMPANY: VALID  
 CENTRAL PROCESSOR: 68020  
 LOCAL MEMORY: 12 M  
 CLOCK RATE:  
 PROPRIETARY: YES  
 AUTO FAULT SIMULATION: NO

HARD DISK: 2000 M  
 GRAPHIC SUPPORT: YES  
 COST: 35-170K  
 NO. USERS: 16

REF NO: 31  
 CAE WORKSTATION: CAE 2000  
 COMPANY: TEKTRONIX  
 CENTRAL PROCESSOR: 78032  
 LOCAL MEMORY: 1-4 M  
 CLOCK RATE: 16.7 M  
 PROPRIETARY: YES  
 AUTO FAULT SIMULATION: NO

HARD DISK: 31-71 M  
 GRAPHIC SUPPORT: YES  
 COST: 34.5-90 K  
 NO. USERS: 1-200

## DIGITAL SIMULATOR

|                       |  |                    |         |
|-----------------------|--|--------------------|---------|
| REF NO:               | 32   |                    |         |
| DIG SIMULATOR:        | TCAT (TEGAS 5)   |                    |         |
| COMPANY:              | CALMA CO.  |                    |         |
| ALGORITHMS USED:      | FAULT COLLAPSING, STUCK AT FAULT   |                    |         |
| SIMULATION TECHNIQUE: | PARALLEL   |                    |         |
| USER INTERFACE:       | INTERACTIVE & BATCH  |                    |         |
| HARDWARE:             | APOLLO(AEGES), VAX(VMS), IBM PC/XT-AT  |                    |         |
| COST:                 | 20-40 K  | STATE OF ART:      | PRESENT |
| ATE INTERFACE:        | YES  | PROPRIETARY:       | YES     |
| CAD/CAE COMPATIBLE:   |  | EVENTS PER SECOND: | 2000    |
| REF NO:               | 33   |                    |         |
| DIG SIMULATOR:        | DAISY LOGIC SIM  |                    |         |
| COMPANY:              | DAISY SYSTEMS INC.   |                    |         |
| ALGORITHMS USED:      | FAULT COLLAPSING, STUCK AT FAULT   |                    |         |
| SIMULATION TECHNIQUE: | CONCURRENT   |                    |         |
| USER INTERFACE:       | INTERACTIVE & BATCH  |                    |         |
| HARDWARE:             | IBM PC/AT, VAX(UNIX), LOGICIAN, IBM(CMS)   |                    |         |
| COST:                 | 55 K   | STATE OF ART:      | PRESENT |
| ATE INTERFACE:        | YES  | PROPRIETARY:       | YES     |
| CAD/CAE COMPATIBLE:   | YES  | EVENTS PER SECOND: | 3-100 K |
| REF NO:               | 34   |                    |         |
| DIG SIMULATOR:        | TEST GRADE   |                    |         |
| COMPANY:              | GATEWAY DESIGN AUTO  |                    |         |
| ALGORITHMS USED:      | EQUIVALENT FAULT SUBSETS, STUCK AT FAULTS,<br>BACKTRACING & FORWARD PATH SENSITIZATION   |                    |         |
| SIMULATION TECHNIQUE: | CONCURRENT   |                    |         |
| USER INTERFACE:       | INTERACTIVE & BATCH  |                    |         |
| HARDWARE:             | APOLLO(AEGES), IBM(MVS, CMS), SUN(UNI), VAX(VMS),<br>ELXSI   |                    |         |
| COST:                 | 35-150 K   | STATE OF ART:      | PRESENT |
| ATE INTERFACE:        | YES  | PROPRIETARY:       | YES     |
| CAD/CAE COMPATIBLE:   | YES  | EVENTS PER SECOND: |         |
| REF NO:               | 35   |                    |         |
| DIG SIMULATOR:        | HILO-3   |                    |         |
| COMPANY:              | GENRAD   |                    |         |
| ALGORITHMS USED:      | 5-STATE, 15-VALUE LOGIC STRENGTH, CAMELOT,<br>PARALLEL VALUE LIST, AUTOMATIC TEST PATTERN<br>GENERATION USING CRITICAL PATH TECHNIQUES |                    |         |
| SIMULATION TECHNIQUE: | PARALLEL & CONCURRENT  |                    |         |
| USER INTERFACE:       | INTERACTIVE & BATCH  |                    |         |
| HARDWARE:             | VAX, APOLLO, IBM, SUN, RIDGE, HP9000, ELXSI,<br>OPUS,  |                    |         |
|                       | VALID  |                    |         |
| COST:                 | 12-160   | STATE OF ART:      | PRESENT |
| ATE INTERFACE:        | YES  | PROPRIETARY:       | YES     |
| CAD/CAE COMPATIBLE:   | YES  | EVENTS PER SECOND: | 3000    |

MATRIX DATA CONTINUED

REF NO: 36  
 DIG SIMULATOR: CADAT 5  
 COMPANY: HHB SOFTRON  
 ALGORITHMS USED: BACKTRACING, FAULT COLLAPSING, STUCK AT FAULTS,  
 MODEL SOURCE CODES, DETECTS & SUPPRESSES FAULTS  
 SIMULATION TECHNIQUE: CONCURRENT  
 USER INTERFACE: INTERACTIVE & BATCH  
 HARDWARE: APOLLO, SUN, IBM PC/XT-AT, VAX, DATA GENERAL  
 COST: 3-80 K STATE OF ART: PRESENT  
 ATE INTERFACE: YES PROPRIETARY: YES  
 CAD/CAE COMPATIBLE: EVENTS PER SECOND: 1000

REF NO: 37  
 DIG SIMULATOR: SILOS, PC=(PSILOS)  
 COMPANY: SIMUCAD  
 ALGORITHMS USED: FAULT COLLAPSING, INPUT & OUTPUT STUCK AT FAULTS,  
 FAULT BLOCKING, STATISTICAL FAULTING  
 SIMULATION TECHNIQUE: CONCURRENT  
 USER INTERFACE: INTERACTIVE & BATCH  
 HARDWARE: APOLLO(AEGES, UNIX), SUN(UNIX), IBM(CMS) & PC/AT,  
 VAX(VMS, UNIX)  
 COST: 3-125 K STATE OF ART: PRESENT  
 ATE INTERFACE: YES PROPRIETARY: YES  
 CAD/CAE COMPATIBLE: YES EVENTS PER SECOND: 1500

REF NO: 38  
 DIG SIMULATOR: MACH 1000  
 COMPANY: SILICON SOLUTION  
 ALGORITHMS USED:  
 SIMULATION TECHNIQUE: CONCURRENT  
 USER INTERFACE: INTERACTIVE & BATCH  
 HARDWARE: ETHERNET SERVER INTERFACE  
 COST: 120K-1M STATE OF ART: NEAR FUTURE  
 ATE INTERFACE: YES PROPRIETARY: YES  
 CAD/CAE COMPATIBLE: YES EVENTS PER SECOND: 1M

REF NO: 39  
 DIG SIMULATOR: HELIX  
 COMPANY: SILVER LISCO  
 ALGORITHMS USED:  
 SIMULATION TECHNIQUE: CONCURRENT  
 USER INTERFACE: INTERACTIVE & BATCH  
 HARDWARE: APPOLO (AEGES,UNIX), IBM PC/RT & RISC, VAX (VMS),  
 PRIME  
 COST: 20K-40K STATE OF ART: PRESENT  
 ATE INTERFACE: YES PROPRIETARY: YES  
 CAD/CAE COMPATIBLE: YES EVENTS PER SECOND: 450

MATRIX DATA CONTINUED

REF NO: 40  
 DIG SIMULATOR: LASAR6  
 COMPANY: TERADYNE  
 ALGORITHMS USED: EQUIVALENT FAULT REMOVAL, STUCK AT FAULTS, MODEL SOURCE CODING, DETECTS & SUPPRESSES FAULTS, BACKTRACING  
 SIMULATION TECHNIQUE: CONCURRENT  
 USER INTERFACE: INTERACTIVE & BATCH  
 HARDWARE: VAC (VMS), APPOLLO (AEGES)  
 COST: 50-280K STATE OF ART: PRESENT  
 ATE INTERFACE: YES PROPRIETARY: YES  
 CAD/CAE COMPATIBLE: YES EVENTS PER SECOND: 500-600

REF NO: 41  
 DIG SIMULATOR: FSIM (QUICKSIM)  
 COMPANY: MENTOR GRAPHICS INC.  
 ALGORITHMS USED: EQUIVALENT FAULT COLLAPSING REMOVAL, STUCK AT FAULTS, DETECTS & SUPPRESSES FAULTS, IDEA  
 SIMULATION TECHNIQUE: CONCURRENT  
 USER INTERFACE: INTERACTIVE & BATCH  
 HARDWARE: APPOLLO (AEGES), VAX(VMS)  
 COST: 17.9-40K STATE OF ART: PRESENT  
 ATE INTERFACE: YES PROPRIETARY: YES  
 CAD/CAE COMPATIBLE: YES EVENTS PER SECOND:

REF NO: 42  
 DIG SIMULATOR: VALIDSIM  
 COMPANY: VALID LOGIC SYSTEMS  
 ALGORITHMS USED: USES A FAULT GRADING TECHNIQUE  
 SIMULATION TECHNIQUE: CONCURRENT  
 USER INTERFACE: INTERACTIVE & BATCH  
 HARDWARE: VAX(VMS,UNIX), IBM PC/AT & (CMS), SCALDSYSTEM  
 COST: 70K STATE OF ART: PRESENT  
 ATE INTERFACE: YES PROPRIETARY: YES  
 CAD/CAE COMPATIBLE: YES EVENTS PER SECOND:1200

REF NO: 43  
 DIG SIMULATOR: HITS  
 COMPANY: NAVAIRENGCEN  
 ALGORITHMS USED: SET-INTERSECTION, STUCK AT FAULTS  
 SIMULATION TECHNIQUE: CONCURRENT  
 USER INTERFACE: INTERACTIVE & BATCH  
 HARDWARE: VAX(VMS,UNIX)  
 COST: 230 STATE OF ART: PRESENT  
 ATE INTERFACE: NO PROPRIETARY: NO  
 CAD/CAE COMPATIBLE: NO EVENTS PER SECOND:

MATRIX DATA CONTINUED

|                       |   |                    |         |
|-----------------------|---|--------------------|---------|
| REF NO:               | 44  |                    |         |
| DIG SIMULATOR:        | TDA   |                    |         |
| COMPANY:              | ROCKWELL  |                    |         |
| ALGORITHMS USED:      | PIN TO PIN SHORTS, HIGH-RAIL (SELECTABLE VOLTAGE) |                    |         |
| SIMULATION TECHNIQUE: | SERIAL  |                    |         |
| USER INTERFACE:       | INTERACTIVE & BATCH                               |                    |         |
| HARDWARE:             | VAX(VMS)  |                    |         |
| COST:                 | 80K   | STATE OF ART:      | PRESENT |
| ATE INTERFACE:        | NO  | PROPRIETARY:       | YES     |
| CAD/CAE COMPATIBLE:   | NO  | EVENTS PER SECOND: |         |

APPENDIX C  
STATE OF THE ART COMPUTER TOOLS

Following are tools identified in the survey analysis. The number following the "Name" in parenthesis refers to the literature reference number in Appendix A.

| <u>NAME</u>                                     | <u>DESCRIPTION</u>   | <u>COMPANY</u>       |
|---|--|----------------------|
| ADEPT (522)                                     | Analog Design Tool for automatic dynamic electrical partitioning of transistors  |                      |
| AFCAD (567)                                     | Wordprocessor office automation  | Auto-Trol            |
| ANGEL (310)                                     | An automatic logic synthesizer for integrated VLSI design systems  |                      |
| ANSYS (567)                                     | Provides finite element analysis   | Auto-Trol            |
| ARCIS (71)                                      | A simulator for those developing gate arrays   | Matra Design Systems |
| BILBO (136)                                     | Integrates Scan Path Design with signature analysis. Registers output pseudorandom patterns to test combinational logic circuits |                      |
| BIST (4, 5)                                     | Hardware Generated Tests   |                      |
| BITGRADE (545)                                  | Fault Simulator-determines fault grades of many digital test patterns  | Gateway Design       |
| BOXER (567)                                     | 3D Solids Modeler  | Auto-Trol            |
| CADAT (53, 70, 71, 74, 164, 313, 315, 323, 561) | A 12-state Digital Simulator which carries 9 additional internal states  | HHB                  |
| CAFIT (575)                                     | Testability Analyzer which provides a figure of merit  | Navy                 |
| CADSAL (574)                                    | System Analysis Tool   | Rockwell             |
| CAL-MP (567)                                    | LSI Layout   | Auto-Trol            |
| CATS (8, 313)                                   | All purpose logic & fault simulator  | HHB                  |
| CAMELOT (55, 304, 317, 523)                     | A Computer Aided Measure of Logic Testability, this algorithm provides normalized values for controllability & observability     | Sears Com Computers  |

|   |  |                 |
|---|--|-----------------|
| COMET (523)                                       | Modified version of SCOAP for semicustom designs   |                 |
| COP (53, 55, 423)                                 | Algorithm for Testability with random patterns   | Bell Northern   |
| COPTR (55, 304)                                   | Testability based on SCOAP which serves as a pathfinder for automatic test generation programs                         | Calma           |
| CVT-FERT (418)                                    | A transistor level fault simulator which handles dynamic & static memory conditions as well as oscillations and races  |                 |
| DAISY LOGIC SIMULATOR (71, 313, 323)              | A logic simulator which carries internal & external states   | Daisy           |
| DIANA (567)                                       | IC Simulation  | Auto-Trol       |
| DORIS (573)                                       | AI shell written in LISP on a Symbolics computer   | Rockwell        |
| DTA (154, 185, 337, 357, 560)                     | CAE Testability based on SCOAP using test point selection  | Daisy           |
| EMTP (567)  | Electromagnetic Transient Simulator  | Auto-Trol       |
| FAN (350, 423)                                    | A automatic Test Pattern Generator which uses concurrent simulation of large digital circuits ( 10K gates )            |                 |
| FANSIM3 (426)                                     | Simulates complex digital circuits at gate & functional levels   |                 |
| FSIM (53, 559)                                    | Concurrent Functional Fault Simulator- enhanced version of CADAT fault simulator                                       | Mentor Graphics |
| GARDS (567)                                       | GARDS Gate Array Design  | Auto-Trol       |
| HAL (321)   | A high speed logic simulation machine which applies hardware implementation, parallel processing & pipeline processing | NEC Corp        |
| HDL (SYNTHESIS) (421)                             | A hardware description language in digital systems testing/verification  | GenRad          |
| HILO (53, 164, 296, 313, 318, 323, 325, 390, 412) | A 15 state concurrent logic fault simulator which uses a hybrid parallel-concurrent algorithm                          | GenRad          |

|                                 |  |                      |
|---------------------------------|--|----------------------|
| HITAP (55, 523)                 | Testability Analysis Program which provides ratings for observability & controlability to determine specific test points in a design | GenRad               |
| HITEST (39, 335)                | A test generation program which uses knowledge engineering through a parallel value list technique                                   | GenRad               |
| HITS (162, 285, 289)            | Digital Simulator, a hierarchical integrated test simulator modeling language  | Navy/Air Force       |
| IN-ATE (406, 460)               | Provides expert rules specifying fault diagnosis for mechanical troubleshooting  | IN-ATE               |
| LASAR (53, 70, 164, 323, 557)   | 15-state Gate, RAM, ROM, Concurrent digital fault simulator with Time Windows  | Teradyne             |
| LISP (63, 241, 234, 340, 438)   | A symbolic AI Language which comes with powerful document management tools   |                      |
| LOGICPRO (71)                   | A logic simulator which works at the switch and gate level, includes CMOS & TTL logic primitives                                     | E/Z CAD<br>E/Z CAD   |
| LOGOS (428)                     | Improves Automatic Test Generation of Digital Circuits   | Grumman              |
| LOGMOD (151, 406)               | Testability Analyzer, automatically generates the optimal fault paths  | Detex                |
| MATE/ATLAS (187, 262, 270, 281) | Test Program Language, ease of movement of a TPS from one tester to another through ATLAS  | Air Force            |
| MENTOR (201, 205, 207, 559)     | CAE Programs, compute engine accelerator   | Mentor               |
| MSC/NASTRAN (567)               | Finite Element Analysis  | AUTO-TROL            |
| PAFEC (567)                     | Finite Element Analysis  | AUTO-TROL            |
| PASA (567)                      | Power Flow   | AUTO-TROL            |
| PATRAN-G (567)                  | Mechanical Design & Analysis   | AUTO-TROL            |
| PAWS (294, 568)                 | TRD Developer Program, provides the capability to automate the generation of TPS documentation                                       | TYX                  |
| PC-LOGS (71)                    | A logic simulator which is part of a schematic-capture system targeted at gate array design  | Personal CAD Systems |



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| PODEM (335, 350)   | Patn Oriented Decision Making Algorithm - accelerates the test pattern generation for error correction and translator circuits |                     |
| RIM (471)  | Relational Information Management System data base   | Boeing              |
| ROMULUS (567)  | 3D Design & Analysis   | AUTO-TROL           |
| RTL (162, 285, 304, 317, 366, 419)                                     | Register Transfer Language   |                     |
| SCOAP (55, 429, 523, 527)  | Controlability/Observability Analysis Provides 6 measurement values  | Sandia              |
| SDS (567)  | VLSI Design  | AUTO-TROL           |
| SILOS (71)   | Microcomputer simulator which isn't currently tied directly to any PC-based schematic capture package                          | Simutec             |
| SIMULOG (71)   | Logic simulator which accepts almost every ILOGS or SILOS type format  | Chancellor Computer |
| SPICE (68, 132, 198, 321, 322, 326, 370, 415, 476, 482, 483, 484, 522) | Analog Simulator, Provides circuit analysis and simulation at the electronic component level                                   | UC Berkeley         |
| SPLICE (68, 409, 522)  | Uses iterated timing   | UC Berkeley         |
| STAFAN (55, 304)   | Uses test vectors to calculate Controlability/Observability  | AT&T BELL           |
| STAMP (152, 407)   | Conducts testability analysis & develops fault isolation strategies for Digital Analog, Electro-Mechanical & Hybrid Systems    | ARINC               |
| STATGRADE (545)  | Digital Fault Analysis using statistics  | Gateway Design      |
| SUPERCOMPACT (567)   | Microwave Design   | AUTO-TROL           |
| SYSCAP (571)   | Analog Simulator with DC-fault analysis for SRU & component level testing  | Rockwell/CDC        |
| T (567)  | Derivative of LISP - AI Language   | AUTO-TROL           |
| TAD (569)  | TRD Development Program  | D. Vanderhide       |
| TAGS (557)   | Technology for the Automatic Generation of Systems   | Teradyne            |

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| TAS (567)                           | Thermal Analysis   | AUTO-TROL      |
| TEGAS (164, 171, 323)               | 4-state gate & functional Digital Simulator  | GE             |
| TESTGRADE (545)                     | Interactive logic & concurrent Fault Simulator   | Gateway Design |
| TESTSCAN (545)                      | Automatic SCAN Test Generator for digital circuits   | Gateway Design |
| TRIFLEX (567)                       | Piping Design & Analysis   | AUTO-TROL      |
| TDA (570)                           | Hybrid, Digital, & Analog fault simulator  | Rockwell       |
| TEST (433)                          | Computer Aided Test Analysis system to detect and isolate faults   |                |
| THEMIS (54, 164)                    | Concurrent Fault Simulator Hierarchical, event driven, multi-level, interactive, logic simulator, for switch, logic, register transfer, functional & behavioral levels, for LSI VLSI & PC IO state, 10X parallel speed | Prime          |
| VALIDATION DESIGNER (323, 343, 545) | CAE System simulator & hardware modeler  | Valid          |
| VERILOG (323, 343, 545)             | Mixed Level Hardware Description Language  | Gateway Design |
| LOGIC EVALUATOR (53, 164, 213)      | Digital Hardware Simulator with a concurrent algorithm   | Zycad          |

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