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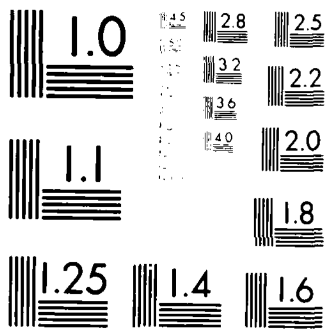

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TECHNICAL REPORT RE-85-10

AN AUTONOMOUS REAL-TIME DATA LOGGING RAIN GAUGE System

Dr. Richard A. Lane
Advanced Sensors Directorate
Research, Development, and Engineering Center

JULY 1985

U.S. ARMY MISSILE COMMAND
Redstone Arsenal, Alabama 35898-5000

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It is known that rain has a detrimental effect on radar signals; however, radar signal degradation as a function of rain intensity is difficult to quantify. This report describes a means of electronically instrumenting off-the-shelf tipping bucket rain gauges such that each rain gauge is an autonomous real-time data recording entity. From information obtained from these devices, rain intensity can be derivated.

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The heart of this system is a real-time clock integrated circuit chip. This device coupled with supporting logic and 4K Random Access Memory (RAM) provide recording and retention capabilities. Each time a rain gauge bucket tips, the time occurrence of this event is recorded and retained in RAM. This sequence continues until testing is terminated at which time data contained in RAM is read out. This mode is designated as Data Retrieval. Data retrieval consists of attaching a Motorola 6800 microprocessor system to the memory board and sequentially reading each memory location. The software is written such that as the data is extracted from memory, it is formatted and sent through an RS-232 port. This port is capable of driving a terminal or printer or any RS-232 compatible device.

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A

LIST OF ILLUSTRATIONS

I. INTRODUCTION

The PERSHING Project Manager's Office requested that the Advanced Sensors Directorate of the Research, Development, and Engineering (RD&E) Center conduct a series of rain tests on the PERSHING II Missile System. The purpose of these tests was to determine the effects of rain on the PERSHING II terminal guidance system. Specifically, the radar altimeter and the correlator.

To accomplish the goals of the test plan and provide a correct evaluation of the terminal guidance parameters, it was necessary to accurately evaluate the rainfall with respect to time so that definitive rain rates could be established. Then, with this information available, correlation, evaluation, and correct conclusions could be made relative to the PERSHING system performance.

It was necessary to design and implement a measuring system to accurately measure rainfall with respect to time so that the requirements of the test plan could be met. The test plan objective was to develop a system that was reliable, simple and easy to use, low cost, and operational within 3 months.

II. SYSTEM OPERATION OVERVIEW

The design and operation of the rain gauge system characterizes itself into three distinct areas. These areas are initialization, operation, and data retrieval. To take advantage of this segmentation and to convey the maximum information, these three areas are addressed individually.

The heart of this rain gauge system is the real-time clock integrated circuit. After a period of evaluation the National MM58174A microprocessor-compatible, real-time clock was selected. Selection was not based primarily on technological superiority but a combination of technological features and delivery, with delivery being the forcing function. The MM58174A is a low threshold metal-gate Composite Metal Oxide Semiconductor (CMOS) device that functions as a real-time clock and calendar in bus-oriented microprocessor systems. Timekeeping is maintained down to 2.2 V to allow power standby battery operations. The time base is generated from an external 32.768 kHz crystal controlled oscillator. Some of the features of this device are independent registers for: tenths of seconds, seconds, day of week, days, tens of days, months, tens of months; relatively fast access of 900 ns; and 2.2 V, 10 μA, battery standby operation in a 16-pin dual in-line package. Specifications are given in Appendix A.

Due to the supply system restraints and since some integrated circuits were on hand, the rain gauge system used various technologies; i.e., CMOS, Transistor-Transistor Logic (TTL), Fairchild Advanced Schottky Technology (FAST), etc. If time had permitted the system would have been implemented using 74HCXXX low-power, high-speed, CMOS devices.

To achieve a basic understanding of the system, a block diagram explanation of the system's three phases of operation will be given, followed by a detailed explanation of the theory of operation for each phase.

A. Initialization

The addresses required to activate the various internal registers contained in the MM58174 real-time clock chip are given in Table 1. An initialization block diagram is shown in Figure 1.

Required time information for initialization is entered into the system via two thumb-wheel switches, the REGISTER SELECTOR SWITCH and the DATA INPUT SWITCH. The desired data information is entered via the DATA INPUT SWITCH which is connected to the clock chip data bus. The internal clock register number, or address, into which the data is to be placed is entered into the REGISTER SELECTOR SWITCH in hexidecimal format. The LOAD SWITCH is then depressed which energizes the GATED OSCILLATOR. The output of the GATED OSCILLATOR drives the ADDRESS SELECTOR which constitutes the clock chip's address bus. In the sequence of events, the ADDRESS SELECTOR output is EXCLUSIVELY OR-ED with the contents of the information previously placed into the REGISTER SELECTOR SWITCH. When a coincidence occurs, a pulse is generated, applied to the clock chip, and designated WRITE ENABLE, E. The occurrence of this pulse loads the data that has been placed in the DATA SWITCH into the register addressed by the REGISTER SELECTOR SWITCH which was programmed (see Table 1). This procedure of loading data into selected registers proceeds until all time data is loaded into the appropriate registers of the MM58174A real-time clock chip.

B. Operation

When the initialization mode is completed the device is placed in the OPERATE mode. The block diagram of the OPERATE mode is given in Figure 2. In this mode, data logging commences. As the bucket fills with water, it pivots and discharges the bucket's contents. Each bucket fills to a volume that represents 0.01 inch of rainfall. As the bucket discharges, a momentary switch closure is activated. This switch closure activates the GATED OSCILLATOR which in turn drives the ADDRESS SELECTOR. The address selector identifies and activates those registers in the real-time clock from which real time data is to be removed and stored in Random Access Memory (RAM). In this application, registers that contained data relative to hours, minutes, and seconds were selected and stored in memory. The completion of the data storge cycle is signaled by an ADDRESS SELECTOR value of one. When this occurs, a predetermined value is stored into the ADDRESS SELECTOR and the cycle is terminated. The system now awaits the next bucket tip. The value that is stored into the ADDRESS SELECTOR represents the starting point or the first register in the MM58174 whose contents will be addressed and stored into RAM at the next occurrence of a bucket tip. A drawing and parts nomenclature of a rain gauge of the type used in the PERSHING II rain tests is shown in Figure 3.

C. Data Retrieval Mode

As the real time test data occurs, it is stored in RAM and can be retrieved when desired to accomplish data evaluation. A block diagram of the data retrieval mode is shown in Figure 4.

To accomplish data retrieval, the flat cable that connects the electronics control board to the memory board is removed and replaced with the flat cable that is connected to the Motorola 6800 microprocessor system. The

TABLE 1. Address Decoding for Internal Registers

Selected Counter	Address Bits				
	AD_3	AD_2	AD_1	AD_0	MODE
0 TEST ONLY	0	0	0	0	WRITE ONLY
1 TENTHS OF SECS	0	0	0	1	READ ONLY
2 UNITS OF SECS	0	0	1	0	READ ONLY
3 TENS OF SEC	0	0	1	1	READ ONLY
4 UNITS OF MINS	0	1	0	0	READ OR WRITE
5 TENS OF MINS	0	1	0	1	READ OR WRITE
6 UNITS OF HOURS	0	1	1	0	READ OR WRITE
7 TENS OF HOURS	0	1	1	1	READ OR WRITE
8 UNITS OF DAYS	1	0	0	0	READ OR WRITE
9 TENS OF DAYS	1	0	0	1	READ OR WRITE
10 DAY OF WEEK	1	0	1	0	READ OR WRITE
11 *UNITS OF MONTHS*	1	0	1	1	READ OR WRITE
12 TENS OF MONTHS	1	1	0	0	READ OR WRITE
13 YEARS	1	1	0	1	WRITE ONLY
14 STOP/START	1	1	1	0	WRITE ONLY
15 INTERRUPT	1	1	1	1	READ OR WRITE

program given in Appendix B is loaded into the microprocessor memory and the starting address of 0010 initiates the program. A listing of an abbreviated program, which was also used in this effort, is given in Appendix C. A flow diagram of the software program is given in Figure 5.

The microprocessor software initializes the required peripheral interface adaptors, resets the memory address counter and then sequentially reads the information stored in RAM. This information represents the time data previously received from the internal registers of the real-time clock device for each occurrence of a bucket tip. The microprocessor takes this information, formats it, and sends the data out to a terminal, line printer, or any compatible RS-232 device.

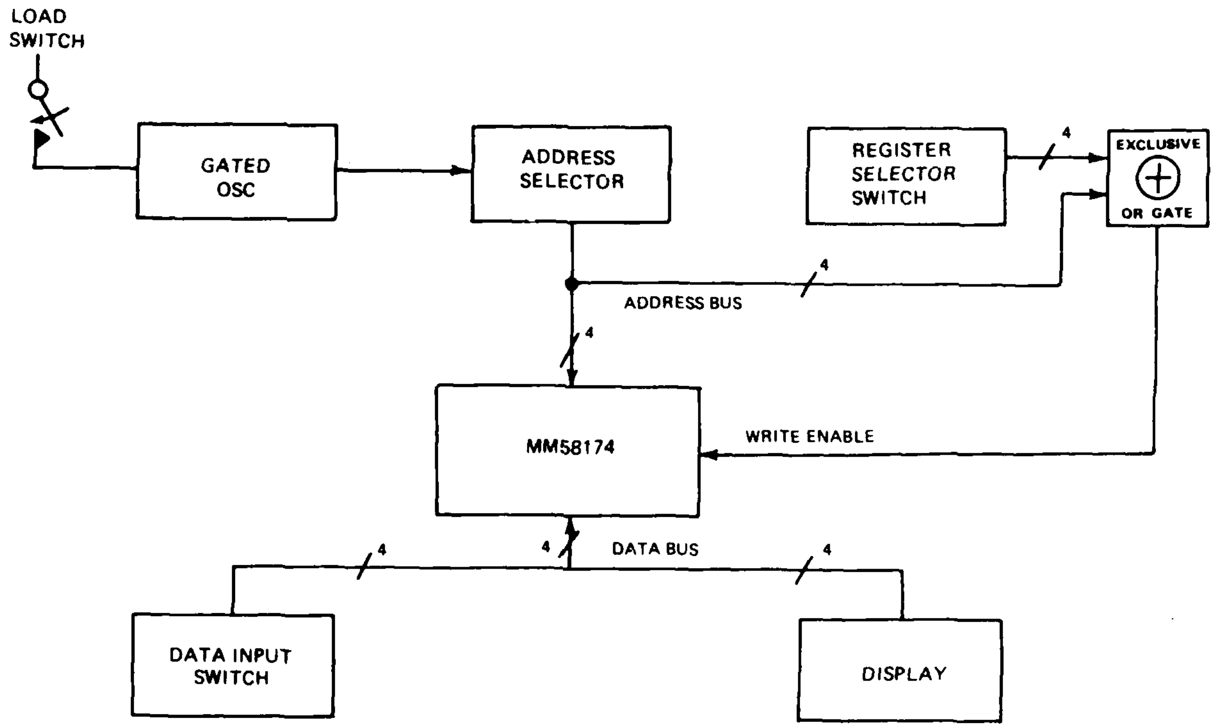


Figure 1. Initialization block diagram.

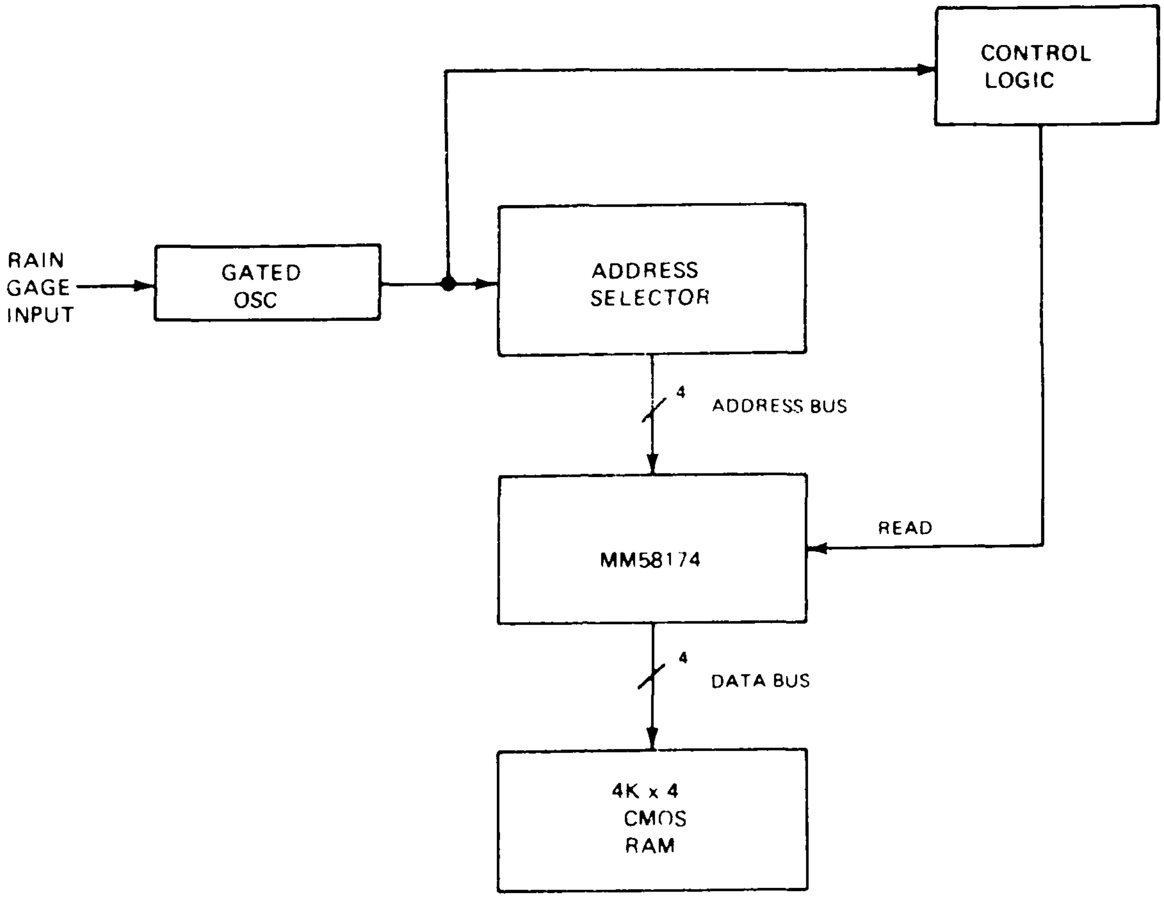
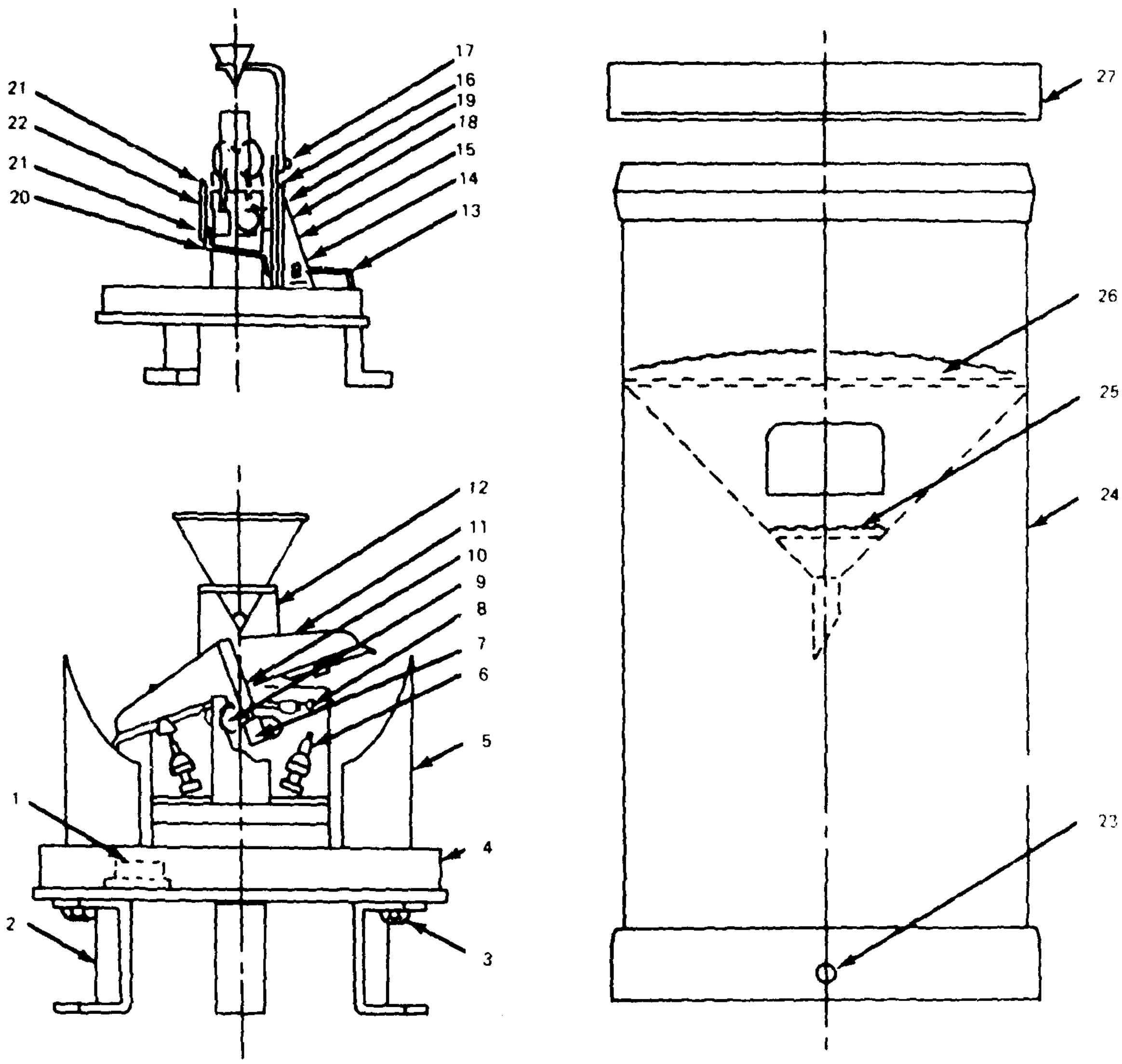


Figure 2. Operation block diagram.



1. Bubble level
2. Leg
3. Support nut
4. Base casting
5. Water drain
6. Calibration assembly
7. Bucket counter weight
8. Mercury switch stop
9. Mercury switch
10. Tipping bucket shaft
11. Tipping bucket assembly
12. Lower funnel with bracket
13. Two-wire conductor
14. Terminals
15. Support brace
16. Major bucket support
17. Funnel support bolt and nut
18. Switch support assembly with shaft
19. Tipping assembly (switch shaft)
20. Bottom bracket for shaft support
21. Connectors for side support
22. Side support for tipping bucket shaft
23. Case screws
24. Outer case
25. Insect screen, small
26. Insect screen, large
27. Cover

Figure 3. Typical tipping bucket rain gauge.

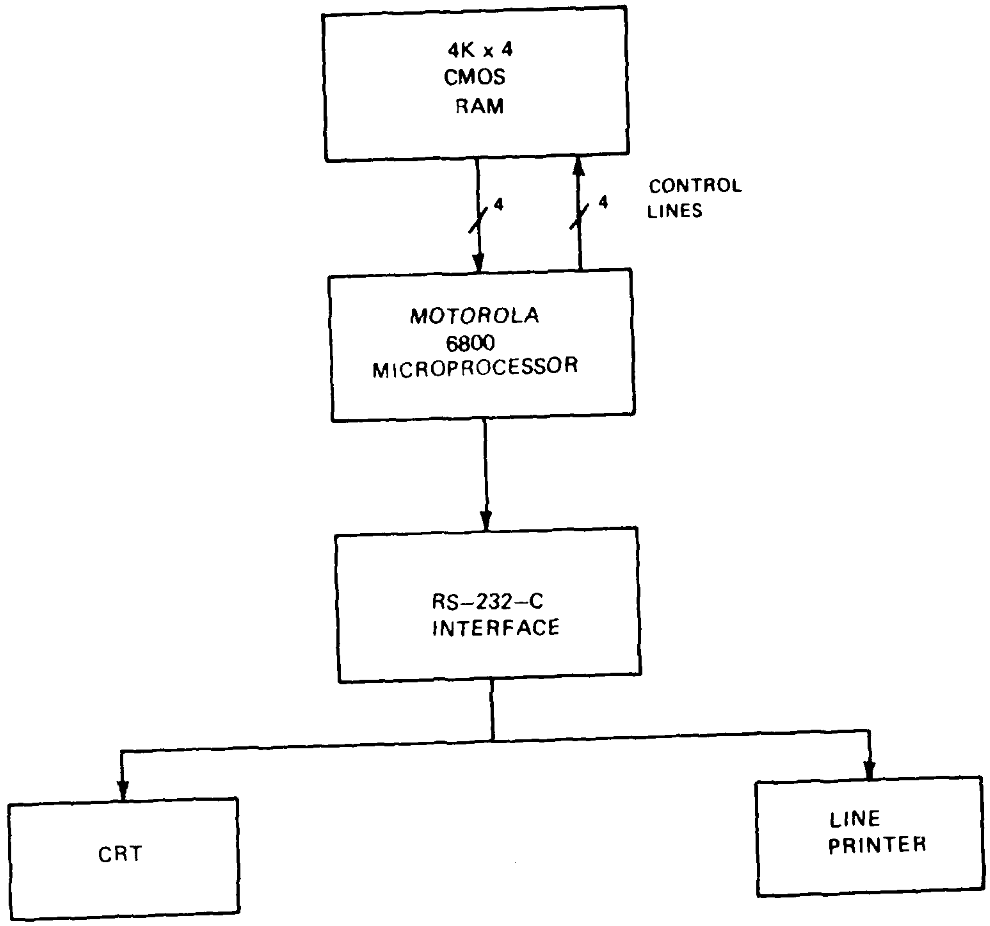


Figure 4. Data retrieval block diagram.

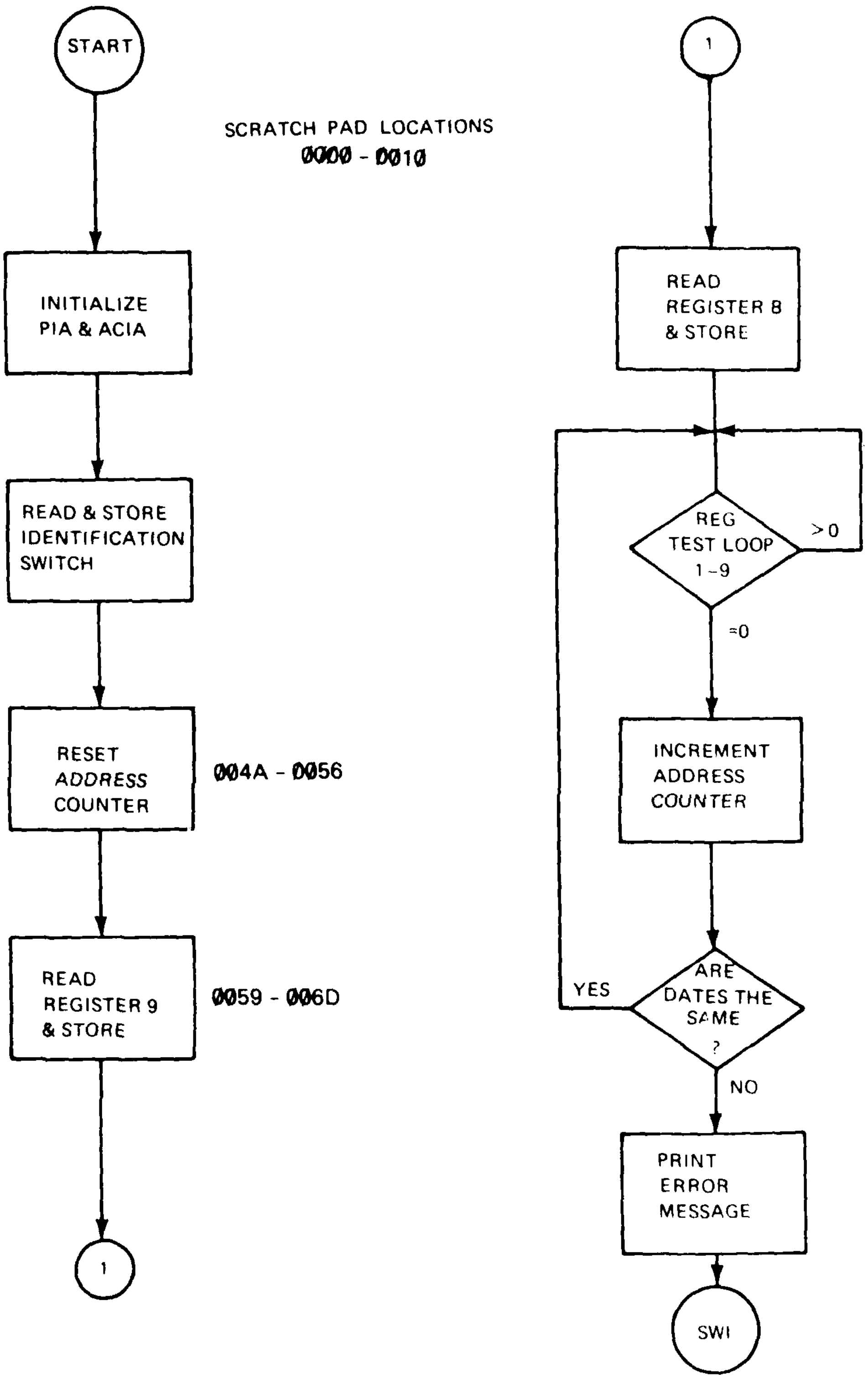


Figure 5. Program flowchart.

III. THEORY OF OPERATION

A. Initialization

Initialization of the system consists of placing current real-time information into the various registers of the MM58174A chip. Table 1 gives the various registers, the register function, and the register address selection bit patterns. For the system implemented for the PERSHING rain tests, all registers were addressed and data placed in them; however, only registers 7 through 1 were of interest for data purposes.

As shown in Figure 6, initialization begins with the TEST/OPERATE switch S-4 being placed in the TEST position and the READ/WRITE switch S-5 placed in the WRITE position. The value "0" (test only reg, Table 1) is placed in thumb wheel switch S-2 which is a BCD switch used for data entry. Outputs from S-2 have pull-up resistors to Vcc and are common with the inputs to U19. U19 is a 74F240 which is an octal inventing bus/line driver chip.

After the desired value is placed in S-2, the WRITE DATA SWITCH S-3 is depressed. The closure of S-3 pulls U2 pin 5 to ground. U2 is a hex debounce chip which gives a clean transition from Vcc to ground on pin 11 of U2. This action causes a logic high to appear on pin 5 of the 74123 chip U7, which is a pair of multivibrators. The 74123 chip is configured as a gated oscillator. A logic low on U7 pin 3 of the 74123 chip turns the oscillator off, while a logic high turns the oscillator on. Oscillator frequency is approximately 200 kHz. The output of the gated oscillator is then routed along two paths. One path goes to U25 pin 1, which is a 74C13. U25 is a CMOS Schmitt trigger which is used primarily for waveshaping, but is also used for the inherent propogation delays associated with CMOS. From U25 pin 4, the signal is routed through the TEST/OPERATE switch and through time delays U22 and U23. From here timing signals are generated, i.e., READ and WRITE signals and the WRITE ENABLE are generated and applied to U16 pin 3 and U17 pin 13, respectively. The complement of the signal which is generated at U24 is also applied to the DISPLAY ENABLE U18 pin 5. U18 is a dot matrix display that gives a visual indication of the data that is being placed into the real-time clock-chip internal registers.

Go back to the U7 output pin 13 and pick up where the signal is applied to U8 pin 4 to complete the initialization portion. The output from the gated oscillator drives the address selector, which is a 74193 up-down binary counter with preloads. The address selector is preloaded with the value of hex twelve and is configured to count-down upon receiving input pulses from the gated oscillator U7. The outputs from the address selector go to the real-time clock chip U16 and a quad two-input exclusive OR gate, U9. The application of the address selector outputs to the inputs of U16 addresses the various internal registers where the desired time information represented by hex data switch S-2 is to be placed. The outputs from the address selector Q_0 through Q_3 are applied to one input of the quad exclusive OR gates of U9. The other input to the exclusive OR gates is provided by register selector hex switch S-1. The exclusive OR-ing of these two inputs provides a timing pulse that is routed through U10, U12, S-4, U21, U22, and monostable U24. U24 generates a pulse on outputs Q and $\overline{Q}$. These outputs are applied to U11, pins 2 and 4. With the READ/WRITE switch S-5 placed in the WRITE position U19 is enabled. This allows data placed in S-2 to be passed through U19 and placed on the inputs of U17, which constitutes the system's bidirectional data bus.

U11 pin 5 is held low and thus the gate is disabled and READ to U16 is held high. Similarly, with S-5 in the WRITE posision, U11 pin 1 is pulled high and the Q output from U24 enables output pin 3. Pin 3 output is applied to U16 pin 3 and to U17 pin 13 via U26. U17 is a bus transceiver. When U17 pin 13 is asserted high, the data that exists on U17 pins 8, 9, 10, and 11 will appear on U17 pins 3, 4, 5, and 6. The coincidence of CHIP SELECT and WRITE pulse loads the data present on pins 4, 5, 6, and 7 of U16 into the register designated by the bit pattern that exists on address pins 9, 10, 11, and 12 of U16.

This sequence of events occurs each time data is placed into the real-time clock chip. Addressing of the clock chip's internal register starts with zero and follows the address programming given in Table 1. The only variables in this sequence is the data that is to be placed into the two switches S_1 and S_2. This sequence of events comprises the initialization of the real-time clock and results in current time information being placed into the various registers of the MM58174 chip.

B. Operation

The initialization phase of system operation is completed with the loading of current time information into all of the real-time clock internal registers. The operate mode is initiated by placing the TEST/OPERATE switch S-4 to the OPERATE position, followed by placing the READ/WRITE switch S-5 to the READ position and pushing the RESET switch S-6. RESET zeros the MEMORY ADDRESS COUNTER and prepares the memory to receive data. It is desirable to manually tip the rain bucket approximately four to six times. This ensures the bucket mechanism is operating properly and preloads the ADDRESS SELECTOR, resets flip-flop (F/F) U-13 and establishes a beginning time reference.

A typical operating cycle works in the following manner. As shown previously in Figure 3, water collects in the calibrated bucket, reference number 11, until it becomes overbalanced at which time it tips. Two variations of tipping buckets were used. One used a mercury switch, reference number 8, for creating the pulse and the other used a magnet in close proximity to a magnetic reed switch. In both implementations, a pulse is generated as a result of a bucket tip which represents a volume of rainfall per unit of area. The rising edge of the output from the rain gauge is applied to monostable U24 (see Figure 6). This triggers the monostable which RESETS R/S F/F U13. When F/F U13 is RESET, a logic low appears at U13 pin 8. This low is applied to U11 pin 8 which causes it to go to a logic high. This high appears at U7 pin 3, the gated oscillator input, which is then turned on. The output from the gated oscillator drives the ADDRESS SELECTOR U8, which generates the addresses for designating the internal time-storage registers of the real-time clock chip. In addition, the output from the ADDRESS SELECTOR U8 is also applied to U10 via inverters in U12. The ADDRESS SELECTOR begins at the count of twelve and counts down. When the count of one is reached by the address selector, it is decoded and an output is generated from U10 which is routed through S-4 contacts to monostable U27 pin 1. Once triggered, U27 output is applied to R/S F/F U13 and the preload input of the address selector. The output of U24 pin 4 when applied to U13 pin 10, sets the F/F which turns off the gated oscillator. Also, the application of U24 pin 4 signal to the ADDRESS SELECTOR U8 pin 11, preloads the ADDRESS SELECTOR with the count of twelve in preparation for the next bucket tip. The output from the gated oscillator follows

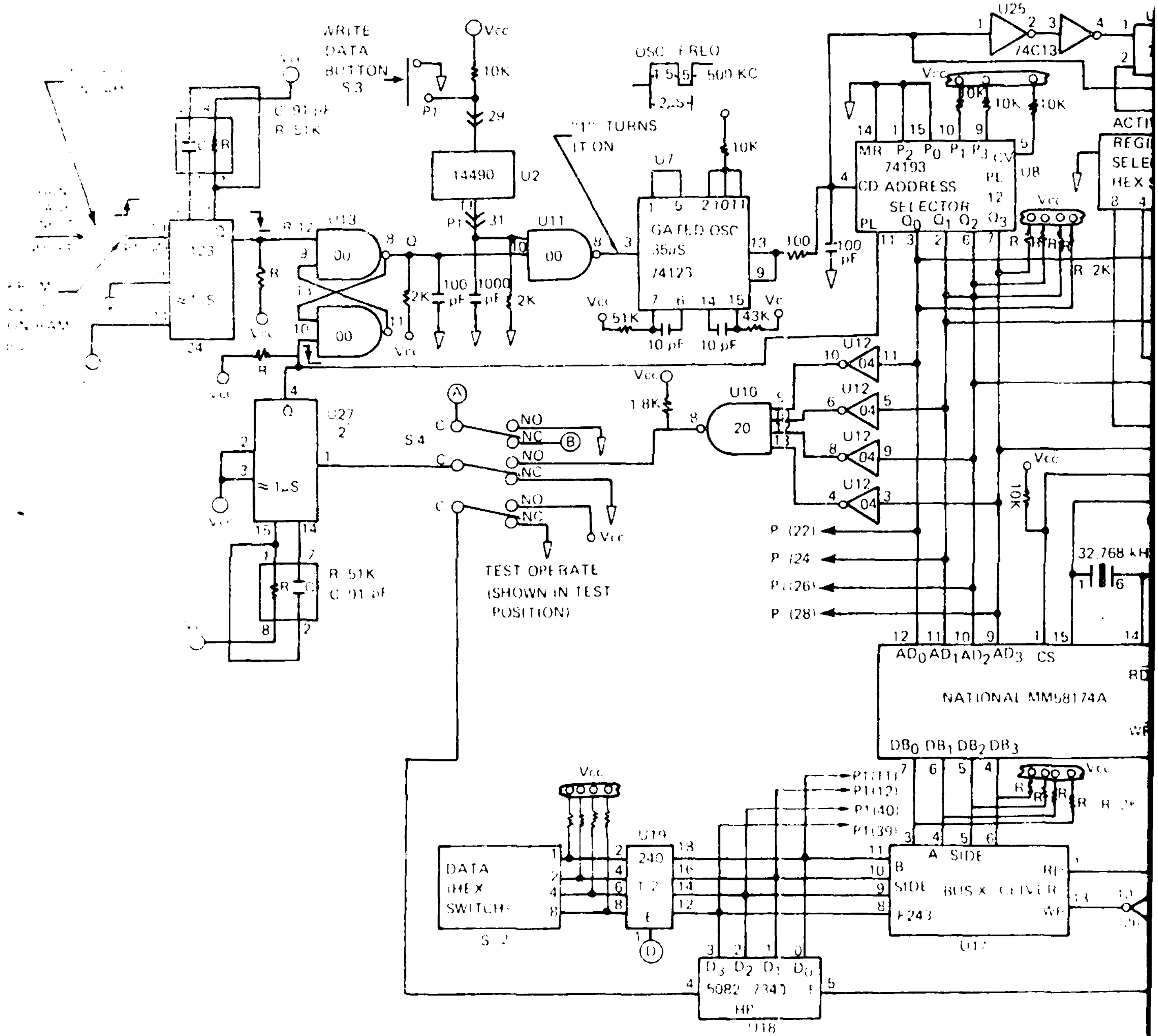
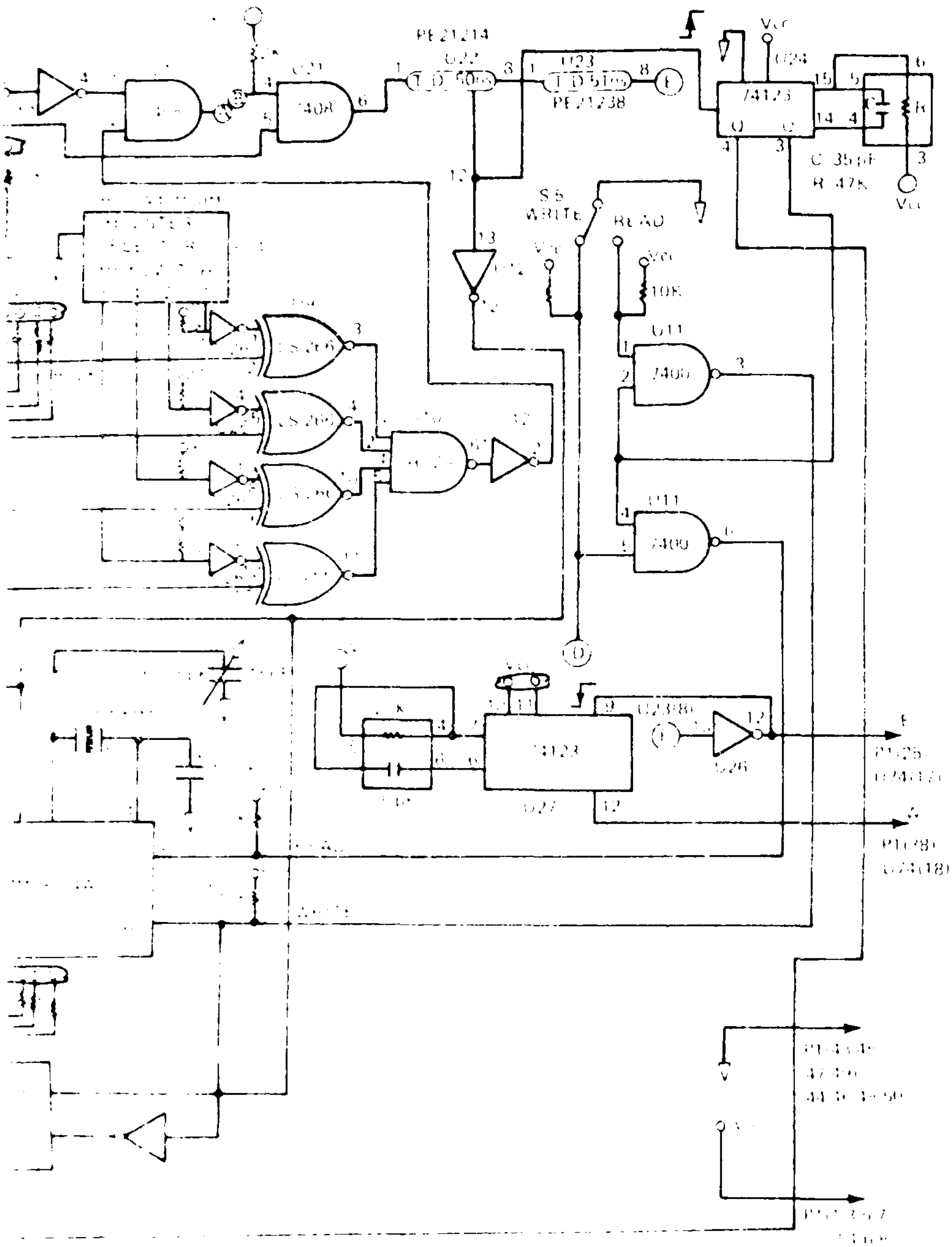


Figure 6. Control b


PE21214
U22
T D 50ns
U23
T D 5ns
PE21238
U21
7408
Vcc
U24
74123
C 35pF
R 47K
S5
WRITE
READ
10K
U11
7400
74123
U27
U26
P1(25)
P1(8)

the same chain of gates as when initialization takes place, except instead of a WRITE pulse being generated, a READ pulse is generated. The READ pulse in coincidence with the application of the CHIP SELECT signal places the real-time data that is current in the real-time clock chip internal registers on the data bus which is U16, pins 4, 5, 6, and 7. The bus transceiver chip, U17 is energized and the data passes through it. Integrated circuit U18 is disabled by pin 4 being grounded by the TEST/OPERATE switch as is U19 by the READ/WRITE switch being placed in the READ mode. The data that is now on the bus is sent via flat cable P1, pins 11, 12, 39, and 40 to the RAM board.

Figure 7 gives the schematic for the RAM board. The memory portions consists of Harris 6504 CMOS chips U35 - U64, in a variable width by 4K deep RAM configuration. Also, on the memory board, 74193 U3 - U5 binary counters are configured to implement the memory address counter. Other associated electronics are buffers, drivers, a 74154 demultiplexer used for memory segment selection, debounce chips, etc.

Outputs from the ADDRESS SELECTOR are applied to the flat cable P1 pins 22, 24, 26, and 28. These signals are applied to the 1-of-16 decoder/demultiplexer U28, which decodes these signals and selects the memory string for data storage that will correspond with the real-time clock registers; i.e., month, day, hour, minute, etc.

Several events must occur before data can be stored in the memory device. First, the memory ADDRESS COUNTER selects the memory location based on the bucket tipping, and turns on the gated oscillator.

The internal registers of the clock vary in bit width depending on their function. For example, the registers used for day, hour, and minutes are all four bits wide as is the tens position and tenths positions of seconds. Similarly, tens position of minutes and units position of seconds are three bits wide while the tens position of hours and days are both two bits wide. Each time the bucket tips the memory ADDRESS COUNTER is incremented by one count. After the ADDRESS COUNTER is asserted, valid data must be present on the data bus after which time the "WRITE" line W must be brought low followed by the ENABLE line E being brought low. When E is brought low, data that is present on the data bus is latched into memory. Now as each internal register of the clock chip is addressed, that address is decoded by the 74154 U28 demultiplexer chip which with other logic generates the E pulse.

The detail signal flow is as follows. As the various internal registers of the real-time clock chip U16 are selected by the ADDRESS SELECTOR U8, these outputs Q_0-Q_3 are also applied to the demultiplexer chip U28, located on the memory board via P1 pins 22, 24, 26, and 28. The action of the bucket tipping has incremented the memory ADDRESS COUNTER by going through Schmitt trigger U1 pin 1 for shaping and then to U2-1 pin 1 which is a hex debounce device. From here the pulse is applied to the address counter U3 pin 5 which selects the next memory location.

Now, data from the real-time clock chip is placed on the data bus which originates at the real-time clock chip U6, pins 4, 5, 6, and 7. This data goes through U17 to the memory board where it is applied to the memory bus connector P1, pins 39, 40, 12, and 11 which are D_3 through D_0, respectively.

Up to this point the following events have transpired; the bucket has tipped, resulting in a register in the real-time clock chip being selected and the application of the ADDRESS SELECTOR outputs being applied to the demultiplexer chip which results in the selection of 1 of 16 unique outputs from U28. These outputs are applied to one side of OR gates U76 and U77. The other side of the OR gates are tied to the output of U74 pin 16. This device is a driver whose input, pin 17, comes from U26 pin 12 on the electronic control board (ECB). This is the ENABLE signal E which was generated from the signals discussed previously, going through U25, U21, and time delays U22 and U23. From U23 pin 8, this signal is applied to inverter U26 pin 13. The output of U26 pin 12 becomes the ENABLE signal and is applied to the memory board through cable connector P1 pin 25 to a buffer-driver U74 pin 17. The output from this driver, pin 16, is applied to the other inputs of OR gates as previously discussed. The coincidence of two inputs on any of the OR gates will initialize that memory string.

The output from U26 pin 12, the ENABLE signal, is also applied to U27 which is a monostable. The output from U27, pin 12, is applied to the memory board via the flat cable pin 38 to buffer driver U74 pin 18. This signal, from U27 pin 12, becomes the W or WRITE signal and its assertion to the memory devices completes signal requirements to write data into the storage elements. This sequence of events transpires each time a bucket tip occurs.

C. Data Retrieval

Data retrieval from the RAM board is accomplished by simply removing the connector from the RAM board and replacing it with a connector from a 6800 microprocessor system.

Appendixes B and C give two versions of software that were used to remove data from RAM. The listing in Appendix C is a reduced version of Appendix B, in that not as many clock registers were queried and no error messages were printed out after automatic detection of nonvalid data.

The microprocessor is interfaced to the RAM board via a Motorola 6821 Peripheral Interface Adapter (PIA). This device provides for parallel data paths and yields the flexibility of designating input and outputs under software control.

The software was written so that when executed, a pulse would be applied to the memory ADDRESS COUNTER followed by the ENABLE pulse E being brought low. The assertation of the E pulse placed data from the designated address on the data bus connector P1 pins 14, 16, 18, and 20, which are Q_0 through Q_3, respectively. This data is latched into the PIA and read by the microprocessor where it is formatted and sent to a RS-232 port via an asynchronous control interface adapter (ACIA). The ACIA provides the means of taking parallel digital data and formatting it into serial digital data with the RS-232-C standard. The RS-232 port allows for driving printers, terminals or other peripheral equipment that meet the RS-232-C requirements.

In the system under discussion, the data was transferred from the Motorola 6800 microprocessor system to a computer. There the data was reduced, analyzed, and plotted to yield rain rate as a function of time.

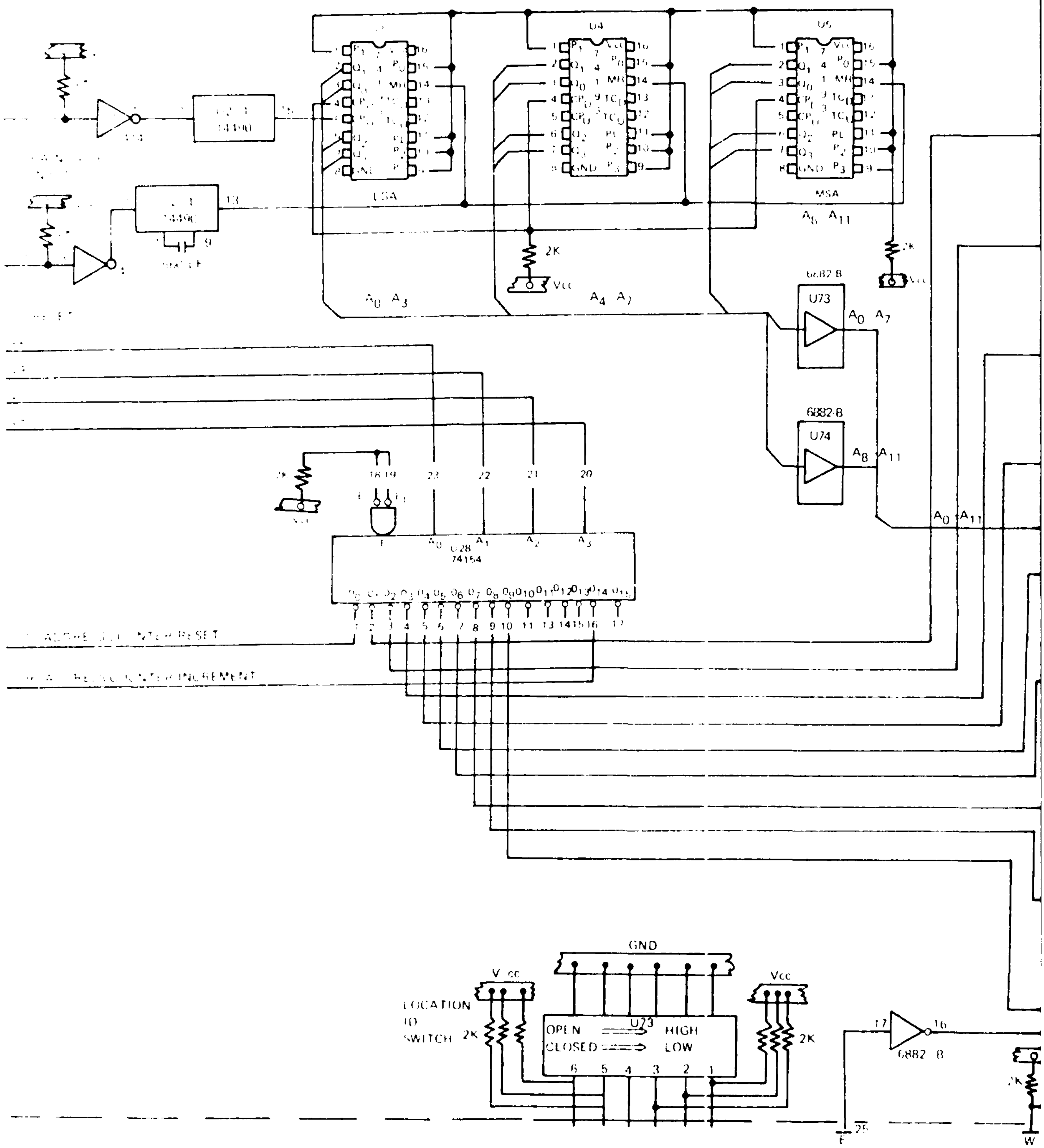
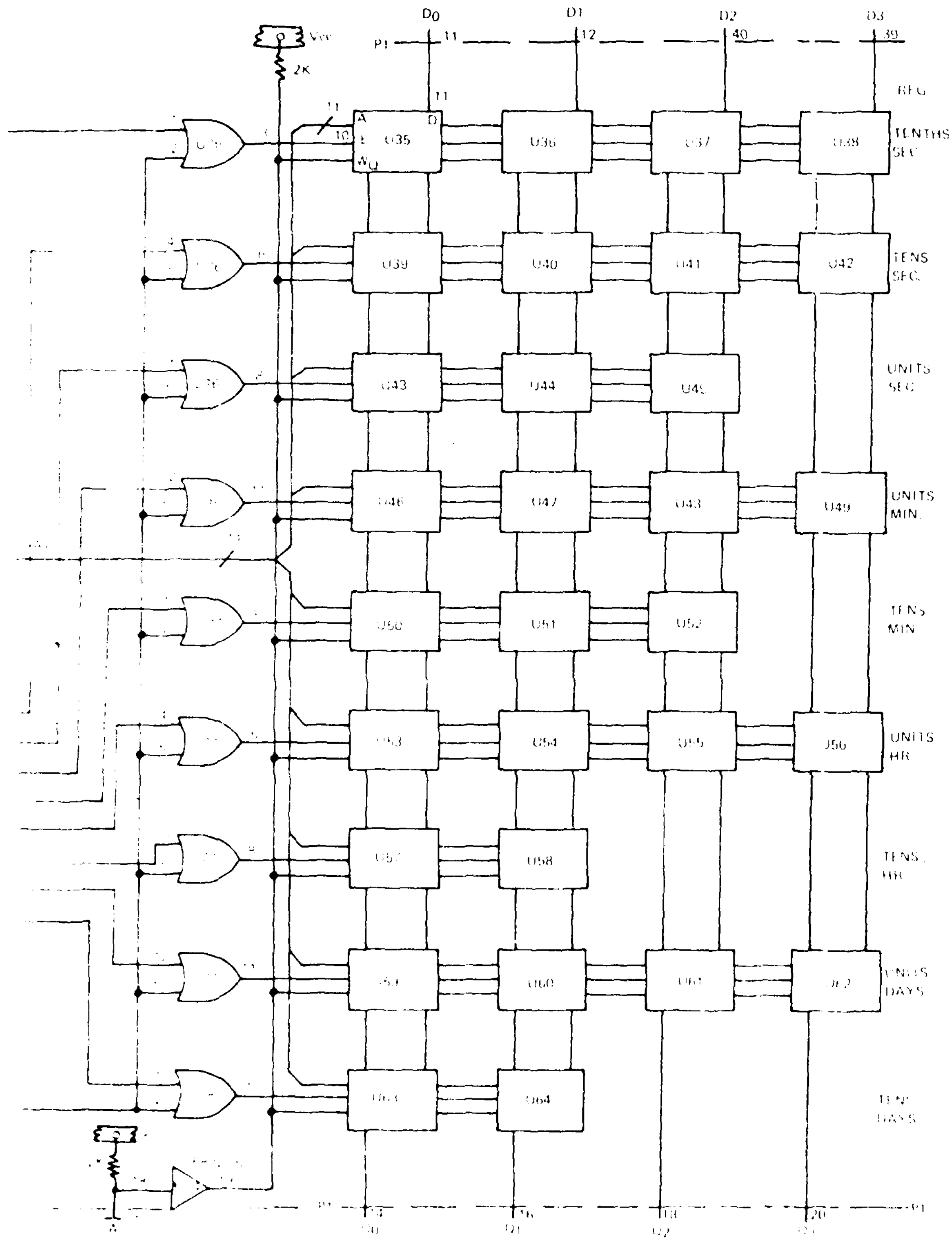


Figure 7. RAM board schem



D0
D1
D2
D3
P1
11
12
40
39
Vcc
2K
REG
11
A
D
10
U35
U36
U37
U38
TENTHS
SEC
U39
U40
U41
U42
TENS
SEC.
U43
U44
UNITS
SEC
U46
U47
U49
UNITS
MIN.
U51
TENS
MIN
U54
U56
UNITS
HR
U58
TENS
HR
U60
DAYS
U64
14
16
18
20
P1

IV. CONCLUSION

The creation of this system is considered to be an outstanding accomplishment, considering the time frame alloted for completion. It is evidence of what can be accomplished in-house where a spirit of cooperation and urgency prevail. The time restraint placed on this project was 3 months from conception to operational hardware.

Much time was spent modifying and altering the design to compensate for the shortcomings in acquiring needed components. Considering all the problems that were surmounted, the system performed in an outstanding manner and advanced the art of rain testing and rain measurement significantly.

V. RECOMMENDATION

Although the rain gauges performed admirably, a redesign of the system would be beneficial. Some of the benefits that could be derived are reduction in physical size and power consumption. This realization could be made by using a low power 74HC family of integrated circuit devices and by implementing memory components that have a higher level of integration.

Better microprocessor utilization could be realized by development of software that would perform real-time rain intensity calculations based on test requirements. This would allow various formats for the data to be accomplished in real-time and provide greater flexibility of the system by merely modifying the software.

APPENDIX A

NATIONAL MM58174 MICROPROCESSOR-COMPATIBLE
REAL-TIME CLOCK SPECIFICATIONS

National Semiconductor

MM58174 Microprocessor-Compatible Real-Time Clock

General Description

The MM58174 is a low threshold metal gate CMOS circuit that functions as a real-time clock and calendar in bus-oriented microprocessor systems. The device includes an interrupt timer which may be programmed to one of three times. Time-keeping is maintained down to 2.2V to allow low power standby battery operation. The timebase is generated from a 32768 Hz crystal controlled oscillator.

- Independent interrupt system with free drain output
- TTL compatible
- Low power standby operation (2.2V, 10μA)
- Low cost internally biased oscillator
- Low cost 16-pin dual-in-line package

Features

- Microprocessor-compatible
- Tenths of seconds, seconds, tens of seconds, minutes, tens of minutes, day of week, days, tens of days, months, tens of months, independent registers
- Automatic leap year calculation
- Internal pull-ups to safeguard data
- Protection for read during data changing
- Fast access time (500 ns)

Applications

- Point of sale terminals
- Word processors
- Teller terminals
- Event recorders
- Microprocessor controlled instrumentation
- Microprocessor time clock
- TV/VCR reprogramming
- Intelligent telephone

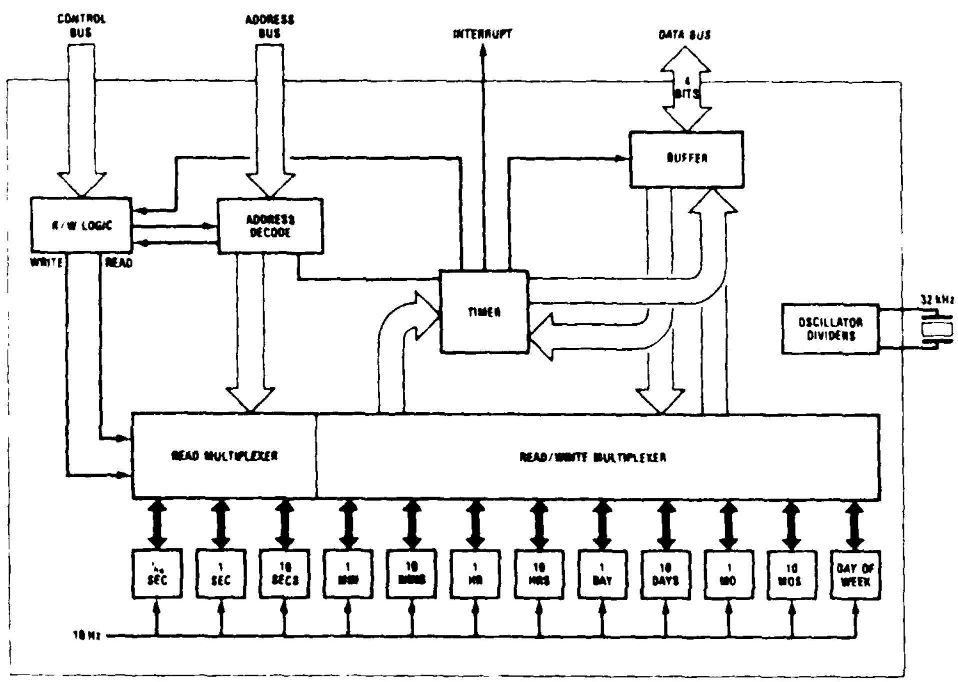


Figure 1. Block Diagram

Absolute Maximum Ratings

Voltage at All Inputs and Outputs	V_{DD} + 0.3 to V_{SS} − 0.3
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
$V_{DD} - V_{SS}$	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics T_A = 0°C to +70°C, V_{SS} = 0V

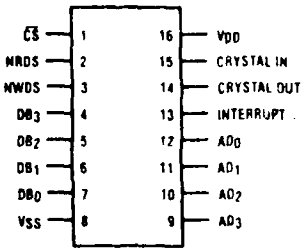
Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage, V_{DD}	Stand-by mode (no READ or WRITE instructions)	2.2			V
Supply Current, I_{DD}	Operational mode	4.0		6.0	V
	V_{DD} = 2.5V		4.0	10	μA
	V_{DD} = 5.0V		1.0		mA
Input Logic Levels	V_{DD} = 5.0V				
for signals:					
AD_0-AD_3, DB_0-DB_3, NWDS, NRDS, $\overline{CS}$					
Logic "1"		2.0			V
Logic "0"				0.8	V
Input Capacitance				10	pF
Input Current Levels	V_{DD} = 5.0V				
Current to V_{SS} for signals: AD_0-AD_3, DB_0-DB_3, NRDS	$V_{IN} = V_{DD}$			20	μA
Internal Resistor to V_{DD}					
for signals:					
NWDS		50	100		kΩ
$\overline{CS}$		10	100		kΩ
Output Logic Levels	V_{DD} = 5V				
for signals:					
DB_0-DB_3					
Logic "1"	I_{OH} = 0.1 mA	2.4			V
Logic "0"	I_{OL} = 1.6 mA			0.4	V
INTERRUPT					
Logic "0"	For I_{DS} = 5 mA			1.0	V
Off Leakage	V_{OUT} = 5V			5	μA

Functional Description

The MM58174 is a microprocessor bus-oriented real-time clock. The circuit includes addressable real-time counters for tenths of seconds through months and a write only register for leap year calculation. The counters are arranged as bytes of four bits each. When addressed a byte will appear on the data I/O bus so that each word can be accessed independently. If any byte does not contain four bits (e.g. days of the week uses only 3 bits), the unused bits will be unrecognized during a write operation and tied to V_{SS} during a read operation.

The addressable reset latch causes the pre-scaler, tenths of seconds, seconds, and tens of seconds to be held in a reset condition. If a register is updated during a read operation the I/O data is prevented from updating and a subsequent read will return the illegal b.c.d. code '1111'. The interrupt timer may be programmed for intervals of 0.5 second, 5 seconds, or 60 seconds and may be coded as a single or repeated operation. The open drain interrupt output is pulled to V_{SS} when the timer times out and reading the interrupt register provides the status and internal selected information.

Connection Diagram



Order Number MM58174N
See Package 19

Circuit Description

The block diagram shown in Figure 1 shows the structure of the CMOS clock chip. A 16-pin DIL package is used.

Crystal Oscillator

This consists of a CMOS inverter/amplifier with on-chip bias resistor and capacitors. A single 6-36pF trimmer is all that is required to fine tune the crystal (see Figure 2). The output of the oscillator is blocked by the start/stop F/F.

Non-Integer Divider

This counter divides the incoming 32,768 Hz frequency by 15/16 down to 30,720 Hz.

Fixed Divider (512)

This is a standard 9 stage binary ripple counter. Output frequency is 60 Hz. This counter is reset to zero by start/stop F/F.

Fixed Divider (6)

This is a three stage Johnson counter with a 10 Hz output signal. This counter is reset to zero state by the start/stop F/F.

Synchronization Stage

Both 10 Hz and 32,768 Hz clocks are fed into this section. It is used to generate a pulse of 15.25 s width on the rising edge of each 10 Hz pulse.

This pulse is used to increment all the seconds, minutes, hours, days, months, and year counter and also to set the data changed F/F.

Data Changed F/F

This is set by the rising edge of each 10 Hz pulse to indicate that the clock value has changed since the last read operation. It is reset by any clock read command. The flip flop sets all data bus bits to a "1" during NRDS time indicating that a register has been updated.

Seconds Counters

There are three counters for the seconds:

a) tenths of seconds
b) units of seconds
c) tens of seconds

The outputs of all three counters can be separately multiplexed on to the command 4-bit output bus. Table 1 shows the address decoding for each counter. All three counters are reset to zero by the start/stop F/F.

Minutes Counters

There are two Minutes counters:

a) units of minutes
b) tens of minutes

Both counters are parallel loaded with data from the 4-bit input bus when addressed by the microprocessor and a Write Data Strobe pulse given. Similarly, the output of both counters can be read separately onto the common 4-bit output bus (Table 1).

Hours Counters

There are two Hours counters which will count in a 24 hour mode:

a) units of hours
b) tens of hours

Both counters have identical parallel load and read multiplex features to the Minutes counters

Seven Day Counter

There is a seven state counter which increments every 24 hours. It will have identical parallel load and read multiplex capabilities to the Minutes and Hours counters. The counter counts cyclically from 1-7.

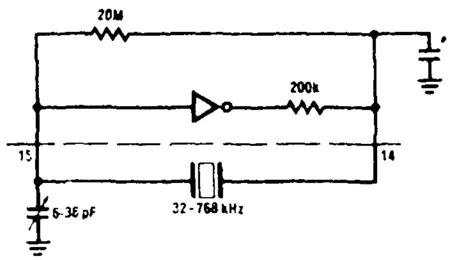


Figure 2. Crystal Oscillator

Days Counter

There are two Days Counters

a) units of days

b) tens of days

The Days counters will count up to 28, 29, 30, or 31 days depending on the state of the Months counters and the Years Status Register. Days counters have parallel load and read multiplex capabilities.

Months Counters

There are two Months counters:

a) units of months

b) tens of months

The Months counters have parallel load and read multiplex capabilities

Years Status Register

The Years Status register is a *shift register of 4 bits. It* will be shifted every year on December 31st. The status register must be set in accordance with Table 3. No readout capability is provided.

Chip Select (CS)

An external chip select is provided. The chip enable is active low

Counter and Register Selection

Table 1 shows the coding on the address lines AD_0-AD_3 which select the registers in the circuit to be either parallel loaded or read on to the output bus

Interrupt Output

An exclusive address selects the interrupt latches (address 15). These latches enable the interrupt output and dictate the frequency of the interrupt as shown in Table 2. The interrupt output flip flop is reset by reading the interrupt register. Writing DB_3 at chip address 15 (F) selects single or repeated interrupt

The contents of the interrupt register are read onto the data bus by reading the interrupt status of the circuit. Table 2 gives the interrupt bits corresponding to data bus bits. DB_3 indicates that an interrupt has occurred. The trailing edge of the NRDS pulse that reads the interrupt status automatically reset DB_3 to zero. The next

Table 1. Address Decoding for Internal Registers

Selected Counter	Address Bits AD_3	AD_2	AD_1	AD_0	Mode
0 Test Only	0	0	0	0	Write only
1 Tenths of secs.	0	0	0	1	Read only
2 Units of secs.	0	0	1	0	Read only
3 Tens of secs.	0	0	1	1	Read only
4 Units of mins.	0	1	0	0	Read or Write
5 Tens of mins.	0	1	0	1	Read or Write
6 Units of hours	0	1	1	0	Read or Write
7 Tens of hours	0	1	1	1	Read or Write
8 Units of days	1	0	0	0	Read or Write
9 Tens of days	1	0	0	1	Read or Write
10 Day of week	1	0	1	0	Read or Write
11 Units of months	1	0	1	1	Read or Write
12 Tens of months	1	1	0	0	Read or Write
13 Years	1	1	0	1	Write Only
14 Stop/Start	1	1	1	0	Write Only
15 Interrupt & Status	1	1	1	1	Read or Write

Table 2a. Interrupt Selection Data

Mode: Address 15, Write Mode

Function	DB_3	DB_2	DB_1	DB_0
No Interrrupt	X	0	0	0
Int. at 6.0 sec. Intervals*	0/1	1	0	0
Int. at 5.0 sec. Intervals*	0/1	0	1	0
Int. at 0.5 sec. Intervals*	0/1	0	0	1

* ±16.6ms

$DB_3 = 0$, single interrupt $DB_3 = 1$, repeated interrupt

Table 2b. Interrupt Read Back (Status)

Mode: Address 15, Read Mode

Interrupt Status	DB_3	DB_2	DB_1	DB_0
Reset	0	0	0	0
60 sec. signal	0/1	1	0	0
5.0 sec. signal	0/1	0	1	0
0.5 sec. signal	0/1	0	0	1

$DB_3 = 0$, no interrupt $DB_3 = 1$, interrupt from timer

Table 3 Years Status Register

Mode: Address 13, Write Mode

	DB_3	DB_2	DB_1	DB_0
Leap year	1	0	0	0
Leap year + 1	0	1	0	0
Leap year + 1	0	0	1	0
Leap year + 1	0	0	0	1

system NRDS pulse after that which has read the interrupt status automatically restarts the interrupt timer if in continuous mode.

When DB_3 is set to zero at chip address 15 (F) the timer is reset at the completion of the selected timing period and must be set by software if a subsequent interrupt is required. Setting DB_3 to 1 allows automatic repeated timer interrupts, starting after the next system NRDS pulse after that which has read the interrupt register.

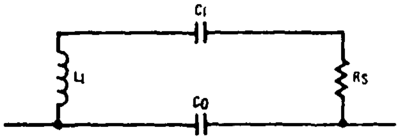
Interrupt should be initialized by applying the reset condition and reading three times at address 15 (F).

Start/Stop

A logic "1" on DB_0 at chip address 14 (E) will start the clock running, a logic "0" will stop the clock. This function allows the loading of time data into the clock and its precise starting.

Test Mode

This mode is incorporated to facilitate production testing of the circuit. For normal operation, the circuit must be set to the non-test mode as part of the system initialization. This is accomplished by writing a logic "0" to DB_3 at AD_0.



$C_I = 0.003\,pF$ $R_S \leq 35\,k\Omega$
$C_0 = 3.0\,pF$ $Q \leq 40\,k\Omega$

Figure 3. Typical Crystal Parameters

Table 4. Timing: Data from Peripheral to Microprocessor

Symbol	Parameter	Min.	Typ.	Max.	Units	Comm.
t_{ACS0}	Address. Bus Valid to Chip Select ON (CS = 0)		40		ns	$V_{DD} = 5V$
t_{CSR}	Chip Select ON to Read Strobe	70			ns	
t_{RD}	Read Cycle Access Time from Read Strobe to Data Bus Valid		450	500	ns	CL = 100 pF
t_{RH}	Data hold time from trailing edge of Read Stobe	0		250	ns	
t_{RA}	Address Bus hold time from trailing edge of Read Strobe	50	500		ns	
t_{ACS1}	Address change to Chip Select OFF		40		ns	
t_{AD}	Address Bus Valid to Data Valid		850	1200	ns	CL = 100 pF
t_{HZ}	Time from trailing edge of Read Stobe until interface device bus drivers are in Tri-State mode	0		250	ns	

Table 5. Timing: Data from Microprocessor to Peripheral

Symbol	Parameter	Min.	Typ.	Max.	Units	Comm.
t_{ACS0}	Address Bus Valid to Chip Select ON (CS = 0)		40		ns	$V_{DD} = 5V$
t_{CSW}	Chip Select ON to Write Probe	310	450		ns	
t_{AW}	Address Bus Valid to Write Strobe	350			ns	
t_{WW}	Write Strobe Width	430			ns	
t_{DW}	Data Bus Valid before Write Stobe	50			ns	
t_{WD}	Address Bus hold time following Write Strobe	100			ns	
t_{WA}	Data Bus hold time following Write Strobe	50			ns	
t_{ACS1}	Address change to Chip Select OFF (CS = 1)		40		ns	

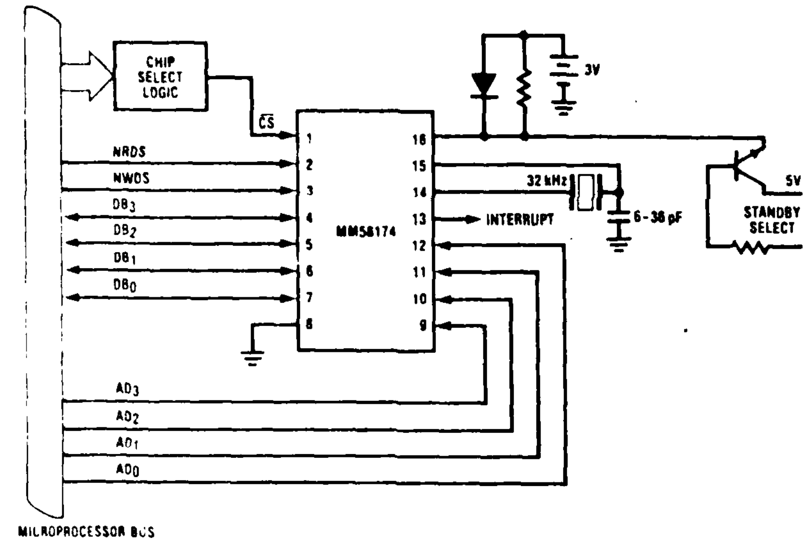


Figure 4. Typical Microprocessor Interface

Timing Waveforms

Read Mode

Figure 5 gives detailed timing in accordance with the Microbus Specification for Microprocessors for the transfer of data from peripheral to microprocessor. See Table 4.

All times are measured from (or to) valid logic "0" level = 0.8V or valid logic "1" level = 2.0V.

Write Mode

Figure 6 gives detailed timing in accordance with the Microbus Specification for Microprocessors for the transfer of data from Microprocessor to peripheral. See Table 5.

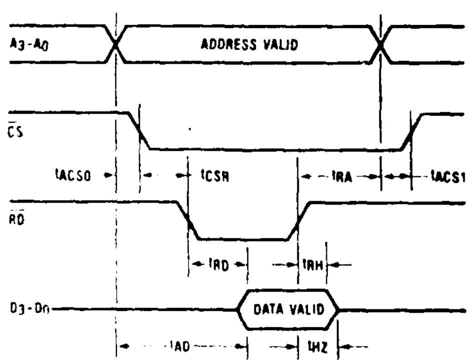


Figure 5. Read Cycle Waveforms

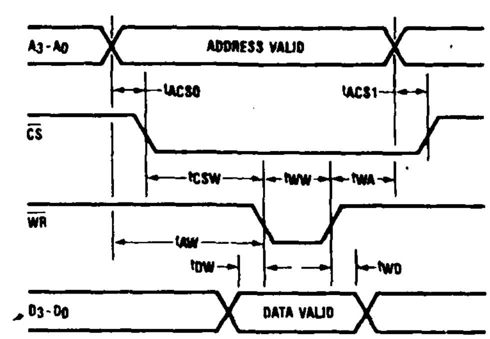


Figure 6. Write Cycle Waveforms

APPENDIX B

MOTOROLA 6800 MICROPROCESSOR PROGRAM LISTING

MOTOROLA 6800 MICROPROCESSOR PROGRAM LISTING

INITIALIZE PIA & ACIA

0000 - 000F Scratch Pad

0010	86	LDA A	#$00	
0012	B7	STA A	$8005	
0015	B7	STA A	$8007	
0018	86	LDA A	#$F0	CONFIGURE PA_4 -PA_7 AS OUTPUTS PA_0 -PA_3 AS INPUTS
001A	B7	STA A	$8004	
001D	86	LDA A	#$C0	CONFIGURE PB_0 -PB_5 AS INPUTS PB_6 -PI_7 AS OUTPUTS
001F	B7	STA A	$8006	
0022	86	LDA A	#$04	
0024	B7	STA A	$8005	
0027	B7	STA A	$8007	
002A	86	LDA A	#$40	
002C	B7	STA A	$8006	SETS PB_6 HIGH (E)
002F	01	NOP		
0030	01	NOP		
0031	01	NOP		
0032	01	NOP		
0033	86	LDAA	#$03	
0035	B7	STAA	$6808	RESETS ACIA
0038	86	LDAA	#$19	CONFIGURE ACIA - 8 DATA BITS, EVEN PARITY, 1 STOP BIT (ACIA
003A	37	STA A	$6808	CONTROL REG)
003D	01	NOP		
003E	01	NOP		
003F=63	01	NOP		
0040=64	B6	LDA A	$8006	READ ID SWITCH
0043	BD	JSR	$01F4	ACIA CHAR X-MISSION
0046	86	LDAA	#$0A	LF
0048	BD	JSE	$01F4	
004B	86	LDA A	#$0D	CR
004D	BD	JSR	$01F4	
0050	01	NOP		
0051	86	LDA A	#$F0	
0053	B7	STA A	$8004	ADDRESS COUNTER, TAKES MR LOW
0056	86	LDA A	#$00	
0058	B7	STA A	$8004	LATCHES MR HIGH
005B	86	LDA A	#$F0	
005D	B7	STA A		LATCHES MR LOW

0060	01			
0061	01			
0062	01			
0063	01			
0064	86	LDA A	#$90	0064-0078 STORES DATE, TENS
0066	B7	STA A	$8004	SELECT REG 9 (DATE)
0069	5F	CLR B		00 ACTIVES PB$_6$
006A	F7	STA B	$8006	SENDS E LOW TO RAM
006D	C6	LDA B	#$40	
006F	B6	LDA A	$8004	CLOCK DATA
0072	F7	STA B	$8006	SENDS E HIGH
0075	B7	STA A	$0000	
0078	01	NOP		
0079	01	NOP		
007A	86	LDA A	#$80	007A-008E STORE UNITS DATE
007C	B7	STA A	$8004	
007F	5F	CLR B		
0080	F7	STA B	$8006	
0083	C6	LDA B	#$40	
0085	B6	LDA A	$8004	
0088	F7	STA B	$8006	
008B	B7	STA A	$0001	
008E	01	NOP		
008F=143$_d$	01	NOP		
0090=144$_d$	86	LDA A	#$39	
0092	BD	JSR	$01F4	
0095	86	LDA A	#$20	SPACE
0097	BD	JSR	$01F4	
009A	86	LDA A	#$90	
009C	B7	STA A	$8004	SELECT REG 9
009F	5F	CLR B		00 ACTIVATES PR$_6$
00A0	F7	STA B	$8006	SENDS E LOW
00A3	C6	LDA B	#$40	
00A5	B6	LDA A	$8004	CLOCK DATA
00A8	B1	CMP A	0000	(ACCA-M0000)=0 then Z=1
				DATE DOESN'T COMPARE THEN
				JUMP TO 0125$_h$
00AB	26	BNE	78-(125$_h$)	BRANCHES IF Z=0, GT, LT
				0.IF Z = 1GOES TO AD
00AD	F7	STA B	$8006	SENDS E HIGH
00B0	46	ROR A		D$_0$ INTO C BIT
00B1	46	ROR A		
00B2	46	ROR A		
00B3	44	LSR A		
00B4	44	LSR A		
00B5	44	LSR A		
00B6	44	LSR A		
00B7	44	LSR A		
00B8	44	LSR A		
00B9	C6	LDA B	#$30	
00BB	1B	ABA		A+B INTO A
00BC	BD	JSR	$01F4	

00BF	86	LDA A	#$0A	LF
00C1	BD	JSR	$01F4	
00C4	86	LDA A	#$0D	CR
00C6	BD	JSR	$01F4	
0009=201$_d$	01	NOP		
00CA=202$_d$	86	LDA A	#$38	
00	BD	JSR	$01F4	
00CF	86	LDA A	#$20	SPACE
00D1	BD	JSR	$01F4	
00D4	86	LDA A	#$80	
00D6	B7	STA A	$8004	SELECT REG 8
00D9	5F	CLR B		00 ACTIVTES PB_6
00DA	F7	STA B	$8006	SENDS E LOW
00DD	C6	LDA B	#$40	
00DF	B6	LDA A	$8004	
00E2	B1	CMP A	0001	(ACCA-M0001)=0, THEN Z=1
00E5	26	BNE	3E (125$_h$)	BRANCHES IF Z=0, IF Z-1 GOES TO E7
00E7	48	ASL A		
00E8	48			
00E9	48			
00EA	48			
00EB	F7	STA B	$8006	SENDS E HIGH
00EE	C6	LDA B	#$30	
00F0	44	LSR A		
00F1	44	LSR A		
00F2	44	LSR A		
00F3	44	LSR A		
00F4	1B	ABA		A+B INTO A
00F5	BD	JSR	$01F4	AC1A
00F8	86	LDA A	#$0A	LF
00FA	BD	JSR	$01F4	
00FD	86	LDA A	#$0D	CR
00FF	BD	JSR	$01F4	
0102=258$_d$	3F	SWI		
0103	01	NOP		
0104=260$_d$	86	LDA A	#$37	
0106	B7	STA A	$0003	
0109	BD	JSR	$01F4	AC1A
010C	86	LDA A	#$20	ASC11 SPACE
010E	BD	JSR	$01F4	
0111	B6	LDA A	$0003	
0114	48	ASL A		
0115	48	ASL A		
0116	48	ASL A		
0017	48	ASL A		ACCA=XO (D_7-D_4 =X, D_3-D_0 =0)
0118	B7	STA A	$8004	SELECT REG X
019B	5F	CLR B		
011C	F7	STA B	$8006	E GOES LOW
011F	C6	LDA B	#$40	

0121=289$_d$	7E	JMP	$4085	
0185=389$_d$	B6	LDA A	$8004	D_3-D_0 =DATA
0188	F7	STA B	$8006	E GOES HIGH
018B	48	ASL A		
018C	48	ASL A		
018D	48	ASL A		
018E	48	ASL A		
018F	7E	JMP	01D5	BITS 7 THRU 4 CONTAIN DATA AFTER ASLA
0192	44	LSR A		
0193	44	LSR A		
0194	44	LSR A		
0195	44	LSR A		
0196	C6	CDA B	#$30	BIT 7 THRU 4 CONTAIN 0, BITS 3 THRU 0 CONTAIN DATA
0198	1B	ABA		A+B INTO A (3x)
0199	BD	JSR	$01F4	
019C	86	LDA A	#$0A	LF
019E	BD	JSR	01F4	
01A1	86	LDA A	#$0D	CR
01A3	BD	JSR	$01F4	AC1A
01A6	B6	LDA A	$0003	
01A9	4A	DEC A		
01AA	81	CMP A	#$30	(ACCA-30)=0, THEN Z=1
01AC	27	BEQ	05 (01B3)	BRANCHES IF Z=1
01AE	7E	JMP	0106	
01B1	3F			
0125=293$_d$	B6	LDA A	$8006	READ ID SWITCH
0128	BD	JSR	$01F4	ACIA
012B	86	LDA A	#$0A	LF
012D	BD	JSR	$01F4	
0130	86	LDA A	#$0D	CR
0132	BD	JSR	$01F4	
ERROR MESSAGE				
01F4=500$_d$	F6	LDA B	$6808	
01F7	57	ASR B		
01F8	57	ASR B		
01F9	24	BCC	F9	
01FB	B7	STA A	6809	
01FE	5F	CLR B	B	
01FF=512$_d$	39	RTS		
0135	86	LDA A	#$44	D
0137	BD	JSR	01F4	
013A	86	LDA A	#$41	A
013C	BD	JSR	01F4	
013F	86	LDA A	#$54	T
0141	BD	JSR	$01F4	
0144	86	LDA A	#$45	E
0146	BD	JSR	01F4	
0149	86	LDA A	#$53	S
014B	BD	JSR	01F4	

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014E        86      LDA A     #$20
0150        BD      JSR       01F4
0153        86      LDA A     #$49      I
0155        BD      JSR       01F4
0158        86      LDA A     #$4E      N
015A        BD      JSR       01F4
015D        86      LDA A     #$56      V
015F        BD      JSR       01F4
0162        86      LDA A     #$41      A
0164        BD      JSR       01F4
0167        86      LDA A     #$4C      L
0169        BD      JSR       01F4
016C        86      LDA A     #$49      I
016E        BD      JSR       01F4
0171        86      LDA A     #$44      D
0173        BD      JSR       01F4
0176        86      LDA A     #$0A      LF
0178        BD      JSR       01F4
017B        86      LDA A     #$0D      CR
017D        BD      JSR       01F4
0180=384    3F      SWI
0181        01
0182        01
0183        01
0184        01

01B3=435d   C6      LDA B     #$E0      INCREMENT ADDRESS
01B5        F7      STA B     $8004     COUNTER 01B3-01CA
01B8        BD      JSR       01C8
01BB        C6      LDA B     F0
01BD        F7      STA B     8004
01C0        01      NOP
01C1        01      NOP
01C2        01      NOP
01C3        01      NOP
01C4=452d   7E      JMP       0090

01C8        C6      LDA B     #$F0
01CA        F7      STA B     $0008
01CD        5F      CLR B
01CE        5C      INC B
01CF        F1      CMP B     $0008
01D2        26      BNE       FA (01C8)  GOES TO 01C8d BRANCHES IF Z=0
01D4        39      RTS
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```
01D5     F6     LDA B     $0003
01D8     C1     CMP B     #$37         (ACCB-M000 )=0 THEN Z=1
01DA     27     BEQ       0B (01E7)    BRANCHES IF Z=1
01DC     C1     CMP B     #$35
01DE     27     BEQ       0E (01EE)    BRANCHES IF Z=1
01E0     C1     CMP B     #$33
01E2     27     BEQ       0A (01EE)    BRANCHES IF Z=1
01E4     7E     JMP       0192

01E7     48     ASL A
01E8     48     ASL A
01E9     44     LSR A
01EA     44     LSR A
01EB     7E     JMP       0192

01EE     48     ASL A
01EF     44     LSR A
01F0     7E     JMP       0192
```

APPENDIX C

ABBREVIATED MOTOROLA 6800 MICROPROCESSOR PROGRAM LISTING

ABBREVIATED MOTOROLA 6800 MICROPROCESSOR PROGRAM LISTING

INITIALIZE PIA & ACIA

0000 - 000F Scratch Pad.

0010	86	LDAA	#$00	
12	B7	STAA	$8005	
15	B7	STAA	$8007	
18	86	LDAA	#$F0	
1A	B7	STAA	$8004	Configures PA_4-PA_7 as outputs PA_0-PA_3 as inputs
1D	86	LDAA	#$C0	
1F	B7	STAA	$8006	Configures PB_0-PB_5 as inputs PB_6-PB_7 as outputs
22	86	LDAA	#$04	
24	B7	STAA	$8005	
27	B7	STAA	$8007	
2A	86	LDAA	#$40	
2C	B7	STAA	$8006	Sets PB_6 High (E)
2F	01	NOP		
30	01	NOP		
31	01	NOP		
32	01	NOP		
33	86	LDAA	#$03	
35	B7	STAA	$6808	Resets ACIA
38	86	LDAA	#$19	
3A	B7	STAA	$6808	Configures ACIA - 8 Data bits, even parity 1 stop bit (ACIA Control Reg.)
3D	01	NOP		
3E	01	NOP		
$003F_h=63_d$	01	NOP		
0040	B6	LDAA	$8006	Read ID Switch
43	BD	JSR	$01FA	ACIA Char. X-Mission
46	86	LDAA	#$0A	LF
48	BD	JSR	$01F4	
4B	86	LDAA	#$0D	CR
4D	BD	JSR	$01F4	
50	01	NOP		
51	86	LDAA	#$F0	
53	B7	STAA	$8004	
56	86	LDAA	#$00	
58	B7	STAA	$8004	MR goes high
5B	86	LDAA	#$F0	
5D	B7	STAA	$8004	MR goes low and stays
60	7E	JMP	0104	

```
  61        01
  62        01
  63        01
0104h=260d  86     LDAA     #$37
  106       B7     STAA     $0003
  109       BD      JSR     $01F4   ACIA
  10C       86     LDAA     #$20    ASCII Space
  10E       BD      JSR     $01F4
  111       B6     LDAA     $0003
  114       48     ASLA
  115       48     ASLA
  116       48     ASLA
  117       48     ASLA             ACIA=X0
  118       B7     STAA     $8004   Selects Reg.X
  11B       5F     CLRB
  11C       F7     STAB     $8006
  11F       C6     LDAB     #$40
  121 = 289d 7E     JMP     $0185
0185 = 389d B6     LDAA     $8004
   88       F7     STAB     $8006   sends E high
   8B       48     ASLA
   8C       48     ASLA
   8D       48     ASLA
   8E       48     ASLA
   8F       7E      JMP     01D5

   92       44     LSRA
   93       44     LSRA
   94       44     LSRA
   95       44     LSRA
   96       C6     LDA B    #$30             |  0  | DATA |
   98       1B     ABA              A+B into A (3X)
   99       BD     JSR      $01F4


   9C       86     LDAA     #$0A    LF
   9E       BD      JSR     01F4
   A1       86     LDAA     #$0D    CR
 01A3       BD      JSR     $01F4   ACIA
 01A6       B6     LDAA     $0003
 01A9       4A     DECA
  1AA       81     CMPA     #$30    (ACCA-30)=0, then Z=1
  1AC       27      BEQ       05    (01B3 Branches if Z=1
  1AE       7E      JMP     0106
  1B1       3F
 ACIA     X-Mission
01F4h=500d  F6     LDAB     $6808
 01F7       57     ASRB
 01F8       57     ASRB
```

01F9	24	BCC F9		
01FB	B7	STAA	6809	
01FE	5F	CLR B		
$01FF_h=512_d$	39	RTS		
$01B3_h=435_d$	C6	LDAB	#$E0	Increment Address Counter 01B3-01CA
1B5	F7	STAB	$8004	
1B8	BD	JSR	01C8	
1BB	C6	LDAB	F0	
1BD	F7	STAB	8004	
1C0	01			
1C1	01			
1C2	01			
1C3	01			
$01C4_h=452_d$	7E	JMP	0104	
01C8	C6	LDAB	#$F0	
1CA	F7	STAB	$0008	
1CD	5F	CLRB		
1CE	5C	INCB		
1CF	F1	CMPB	$0008	
1D2	26	BNE	FA (01C8)	
1D4	39	RTS		
01D5	F6	LDAB	$0003	
D8	C1	CMPB	#$37	$(ACCB-M_{0003})=0$ then Z=1
DA	27	BEQ	0B (01E7)	
DC	C1	CMPB	#$35	
DE	27	BEQ	0E ([illegible])	
E0	C1	CMPB	#$33	
E2	27	BEQ	0A (01EE)	
01E4	7E	JMP	0192	
01E7	48	ASLA		
E8	48	ASLA		
E9	44	ASLA		
EA	44	LSRA		
01EB	7E	JMP	0192	
01EE	48	ASLA		
EF	44	LSRA		
F0	7E	JMP	0192	

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