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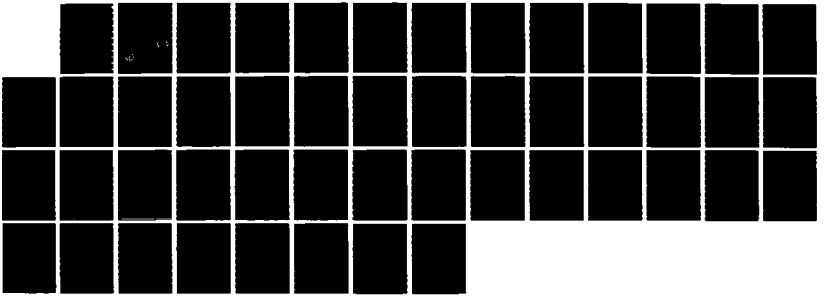

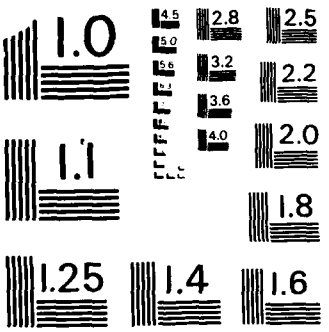

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AUTOMATIC GAIN CONTROL AMPLIFIER

BY JOHN T. GALLAGHER

UNDERWATER SYSTEMS DEPARTMENT

24 MAY 1985

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The Automatic Gain Control compresses a short duration signal so that the signal may be saved by a magnetic tape recorder. To respond to a short duration signal, the signal is digitized and stored in RAM while a gain for the signal is determined. After the gain is applied, the compressed signal is converted back to analog form.

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The gain processes are applied to multichannels without significant loss of phase difference between the channels. Thus, the time relationship between the various received signals is preserved. The gain applied to each channel is unique.

The gain code is also available for storage on magnetic tape. Each code is summed to yield an analog voltage, then multiplexed with the other channels' gain signal. The multiplexed output is also available for recording.

FOREWORD

This report describes a multichannel Automatic Gain Control circuit that is implemented using Analog-to-Digital conversion, digital processing of the signal, and Digital-to-Analog conversion to the compressed signal. The purpose of the circuit was to obtain signal compression reducing the dynamic range of the signal so that the signal could be recorded on magnetic tape. This work was funded by the Naval Sea Systems Command, PMS-409, under task number S0222AS.

The author wishes to thank Mr. Manfred K. Pruessner for developing the initial concept for the circuit.

Approved by:

A. M. JOX, Head
Surface ASW Division

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CHAPTER 1

INTRODUCTION

By combining analog and digital circuitry, a fast Automatic Gain Control (AGC) capable of amplifying the first instant of a received signal burst has been built. The AGC provides a constant gain for the duration of an input signal's pulse length. To determine and apply the gain to the first instant of the signal, the analog signal pulse is digitized by an analog-to-digital (A/D) converter and then delayed in RAM while the signal level is detected and the necessary gain determined. After the gain is applied to the digital signal, the signal is returned to analog form by a digital-to-analog (D/A) circuit. The dynamic range of the signal is compressed by the AGC circuitry so that the signal can be recorded for future processing.

The system, for which the AGC is intended, compares the phase of several received signals. Therefore, any distortion between channels must be minimized. Signals as low as 40 mvolts peak can be digitized and reconstructed without significant loss of phase information between channels. (Less than 1 microsecond difference between any two channels.)

Because each channel is processing a unique signal, which will later be compared with the signal of the other channels, the tolerance of the transfer function among the channels is constrained to result in phase shifts less than 1 microsecond between any two channels for frequencies above 1 kHz. Therefore, the digital processing must be sequenced by a common clock and the analog portion of the circuit must have closely matched components between channels.

The initial stage of the AGC circuit consists of a manually adjusted differential gain stage and manually set high- and low-pass filter sections. The signal is then passed to a sample and hold circuit which is an integral part of the A/D hybrid circuit. Concurrently, the same signal is passed through a precision ac-dc converter and the peak dc level is sampled and converted to a digital code by a second A/D converter. The converter's digital output is used to establish a gain code for the signal. Although the signal determines the gain, the gain code's time duration before resetting is manually set using a panel switch.

A detection causes a sample of the signal pulse envelope to be taken and a gain code generated. Without a signal present, the background noise level is periodically sampled and a gain code based on the noise level is generated. By applying a gain for the noise level, signals too low to trigger the pulse detector will be amplified and made available for processing.

Meanwhile, the digitized signal is stored in RAM for a predetermined time (manually adjusted to 10 discrete time periods of 10 to 20 milliseconds) before being passed to the shift registers. The gain is applied by shifting (up) the digitized signal code with each shift pulse doubling the gain. There are seven discrete gains possible from 2 to 128.

After the gain process, the digitized signal is delivered to a D/A converter and low-pass filter through which the now compressed analog signal is reconstructed. The signal is then available for recording on tape and further processing.

Each of the channels of the AGC are made as close to identical as possible by matching, between channels, the passive component values in the analog circuits. The analog circuits are located at the initial and final stage of each channel. A block diagram of one of the channels is shown in Figure 1.

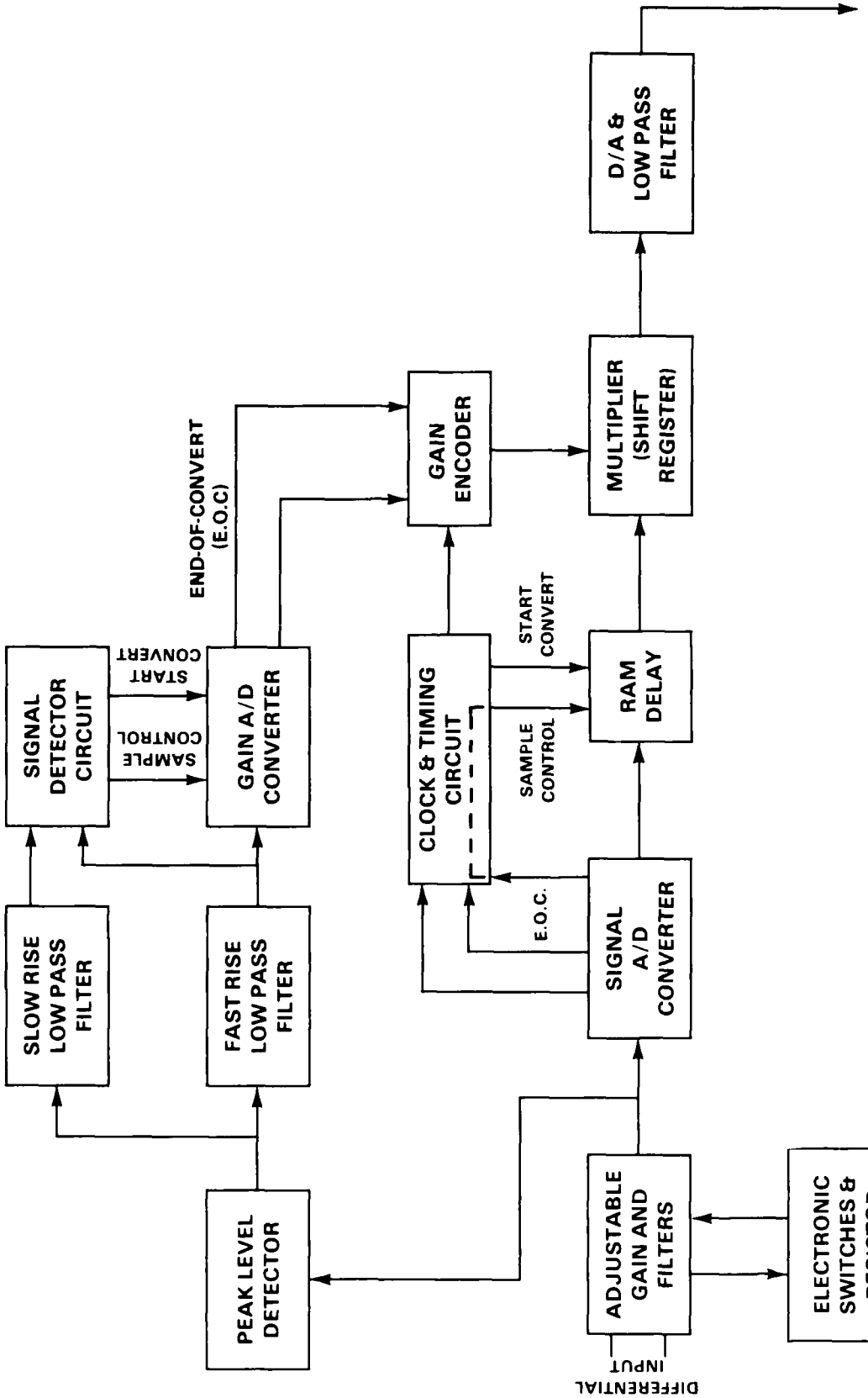


FIGURE 1. BLOCK DIAGRAM OF AN AGC CHANNEL

CHAPTER 2

ANALOG INPUT

A differential input amplifier, capable of four discrete gains, receives the input to the AGC amplifier. The amplifier has a single ended output and provides manually selected gains of 0, 10, 20, and 30 dB. To obtain the desired gain, a CMOS electronic switch (DG-308) is used to add parallel resistors to the differential amplifier's resistor networks. The resistor values are given in Table 1. Though the common mode rejection (CMR) is not as critical as in very low signal applications, ratios of better than 48 dB at zero gain are obtained. The 48 dB CMR is entirely due to the match between the inverting and non-inverting resistor networks.

The output of the differential amplifier is input to a two-pole, high-pass active Butterworth filter. The filter's operational amplifier is set for a non-inverting gain of 1.58. The damping coefficient is determined solely by the gain of the amplifier. The relationship is $\alpha = 3-K(\text{gain})$ where $\alpha = 2/\text{damping coefficient}$. The cut-off frequency is determined exclusively by the RC network. By making the resistor R_1 equal to R_2 and capacitor C_1 equal to C_2, the overall sensitivity of the circuit to α is minimized. With the capacitor values constant one may change the cut-off frequency by changing the value of the resistive components of the RC network. The initial value for resistors is 100k ohm which corresponds to a frequency of 1.6 kHz. By placing a resistor in parallel with each 100k ohm resistor, one changes the cut-off frequency of the filter. A CMOS electronic switch (DG-507) is used to change the resistor value of the RC network. The resistors that are added in parallel to the fixed 100k ohm resistors of the RC network are identical in value. In this way the damping coefficient maintains its total dependence on the amplifier gain. Table 2 lists the value of the resistor added to each 100k ohm resistor and the corresponding frequency. The cut-off frequencies were chosen to be one-third octave up from the previously lower frequency starting at 1.6 kHz. Figure 2 shows the schematic representation of the circuit.

The output of the high-pass filter is passed to a similarly constructed low-pass Butterworth filter. Switching is accomplished with the same type of CMOS electronic switch (DG-509) adding a unique set of parallel resistors for each of the eight possible additional cut-off frequencies. The original non-paralleled resistor frequency is 2 kHz. The eight switchable frequencies are one-third octave apart from 3.1 kHz to 16 kHz.

TABLE 1. FEEDBACK AND INPUT RESISTOR VALUES FOR THE ANALOG GAIN CIRCUIT

Gain	R_1	R_f
0 dB	10 KΩ	11.1 K||100 KΩ
10 dB	4.64 K||10 KΩ	11.1 K||100 KΩ
20 dB	10 KΩ	10 KΩ
30 dB	4.64 K||10 KΩ	10 KΩ

TABLE 2. RESISTOR VALUES ASSOCIATED WITH FILTER CUT-OFF FREQUENCIES

	High-Pass Filter	Low-Pass Filter
Common	100.0 KΩ - 1.6 kHz	80.6 KΩ - 2.0 kHz
1	398.0 KΩ - 2.0 kHz	130.0 KΩ - 3.1 kHz
2	174.0 KΩ - 2.5 kHz	80.6 KΩ - 4.0 kHz
3	100.0 KΩ - 3.1 kHz	55.6 KΩ - 5.0 kHz
4	68.0 KΩ - 4.0 kHz	44.2 KΩ - 6.0 kHz
5	47.0 KΩ - 5.0 kHz	26.7 KΩ - 8.0 kHz
6	33.0 KΩ - 6.0 kHz	19.6 KΩ - 10.0 kHz
7	24.9 KΩ - 8.0 kHz	15.8 KΩ - 12.5 kHz
8	19.6 KΩ - 10.0 kHz	11.5 KΩ - 16.0 kH

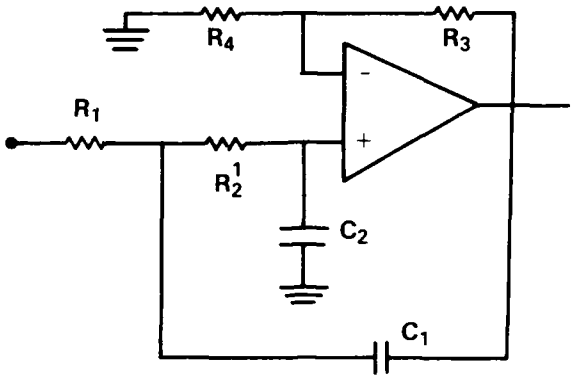


FIGURE 2A. TWO-POLE LOW-PASS FILTER WITH GAIN

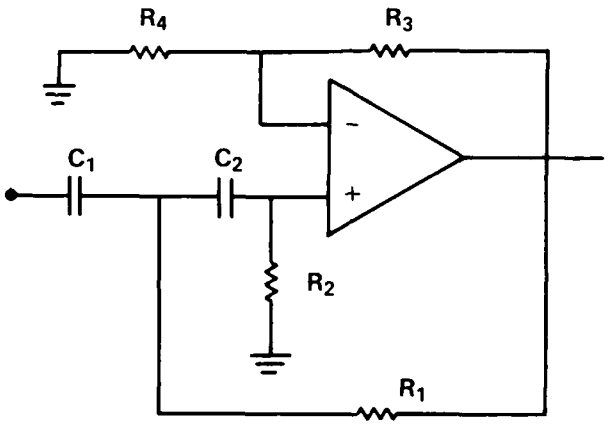


FIGURE 2B. TWO-POLE HIGH-PASS FILTER WITH GAIN

The filters allow the operator to establish a narrow band around the transmitted frequency that improves the signal-to-noise ratio. The component values are closely matched between the different channels. Matching of components is extremely important for both high-pass and low-pass filters since the rate of change of the phase response is highest at the cut-off of the 3 dB frequency. The cut-off is very close to the signal frequency. Therefore, small variations in the component values can cause significant phase changes in the signal from channel to channel. The equations for the high- and low-pass filters are:

LPF: $\therefore w_o = \frac{1}{RC}$

$$H(S) = \frac{k}{S^2(C_1C_2R_1R_2) + S(C_2R_2+C_2R_1) + S(1-k)\,C_1R_1 + 1} \tag{1}$$

$$R_1 = R_2 \;;\; C_1 = C_2 \;;\; K = 1 + \frac{R_3}{R_4} \tag{2}$$

HPF: $\therefore w_o = \frac{1}{RC}$

$$H(S) = \frac{K(R_1C_1R_2C_2)S^2}{S^2(C_1C_2R_1R_2) + S(C_1R_1+C_2R_1) + S(1-k)\,R_2C_2 + 1} \tag{3}$$

The phase and ultimately the time relations are

$$\phi_{HP} = 180° - \tan^{-1}\left(\frac{\alpha\, w\, w_o}{w_o{}^2-w^2}\right) \;;\; \phi_{LP} = 0° - \tan^{-1}\left(\frac{\alpha\, w_o\, w}{w_o{}^2-w_o}\right) \tag{4}$$

$$T_{delay} = -\frac{d\phi}{dw} \qquad \Delta T_d = (S^{T_d}_{w_o})\,(T_d) \sum_i S^{w_o}_X \left(\frac{\Delta X_i}{X_i}\right) \;;$$

X_i = passive ckt components (5)

$$\Delta T_{X_i} = \frac{\Delta\phi}{w} = \frac{1}{w}\left\{\sum_i \left[S^{\phi}_{w_o}\,\phi\left(S^{w_o}_{X_i}\,\frac{\Delta X_i}{X_i}\right) + S^{\phi}_{\alpha}\,\phi\left(S^{\alpha}_{X_i}\,\frac{\Delta X_i}{X_i}\right)\right]^2\right\}^{1/2} \tag{6}$$

is the difference in time delay between channels resulting from the passive element's tolerance.

$$\Delta T_k = \frac{1}{w} S_\alpha^\phi \phi \sum_{i=3}^{4} S_{R_i}^\alpha \frac{\Delta R_i}{R_i} \text{ for the gain resistors' tolerances.} \tag{7}$$

$$S_{w_o}^\phi = \frac{w_o}{\phi} \frac{\partial \phi}{\partial w_o} = \frac{\alpha\, w\, (w_o^2+w^2)}{(w_o^2-w^2) + (\alpha\, w_o\, w)^2} \cdot \frac{w_o}{\phi} \tag{8}$$

where Φ is the phase relationship defined in Equation (1).

$$S_\alpha^\phi = \frac{\alpha}{\phi} \frac{\partial \phi}{\partial \alpha} = \frac{\alpha\, w_o(w^2-w_o^2)}{(w_o^2-w^2) + (\alpha\, w_o\, w)^2} \cdot \frac{\alpha}{\phi} \tag{9}$$

$$w_o = \frac{1}{R_1 R_2 C_1 C_2}^{1/2} \tag{10}$$

$$S_{X_i}^{w_o} = -1/2 \tag{11}$$

$S_{X_i}^\alpha = \frac{X_i}{\alpha} \frac{\partial \alpha}{\partial X_i}$ which is different for high-pass and low-pass filters. However, for $w = w_o$ (worst case) $S_\alpha^\phi = 0$, Therefore, the shift delay difference between channels reduces to:

$$\Delta T = \frac{1}{w} \left\{ \sum_i \left[S_{w_o}^\phi \phi \left(S_{X_i}^{w_o} \frac{\Delta X_i}{X_i} \right) \right]^2 \right\}^{1/2} = \frac{1}{w} (8) \left\{ \left[\left(\frac{2\alpha\, w^4}{\alpha^2\, w^4} (-1/2) \ (2 \text{ Tol.}) \right]^2 \right\}^{1/2} \tag{12}$$

$$\Delta T = \frac{8}{w\alpha} (2 \text{ Tol.}) \text{ ; if } w = 2\pi \ (3{,}000) \text{ rad/sec ; } \alpha = (3\text{-}K) = \sqrt{2} ,$$

$$\Delta T < 1 \ \mu\text{sec} , \text{ Tolerance} < \frac{10^{-6}(2\pi)(3\text{x}10^3)(\sqrt{2})}{2(8)} = .00166$$

where K is the gain of the amplifier.

A 0.166 percent match between components insures less than a 1 microsecond shift between channels for the worst case condition ($w = w_o$). However, w should never equal w_o.

In order to eliminate any dc offset from entering the Sample and Hold, the output of the low-pass filter is coupled through a 1 fd capacitor. A 1K ohm resistor was added from the Sample and Hold input to ground to eliminate a very slow moving bias that was witnessed when the capacitor was added to the circuit. Together the capacitor and resistor form a one-pole, high-pass filter with a 160 Hz cut-off frequency. The capacitor and resistor are matched to 0.2 percent among all channels. (The analog input circuit is shown in Figure 3.)

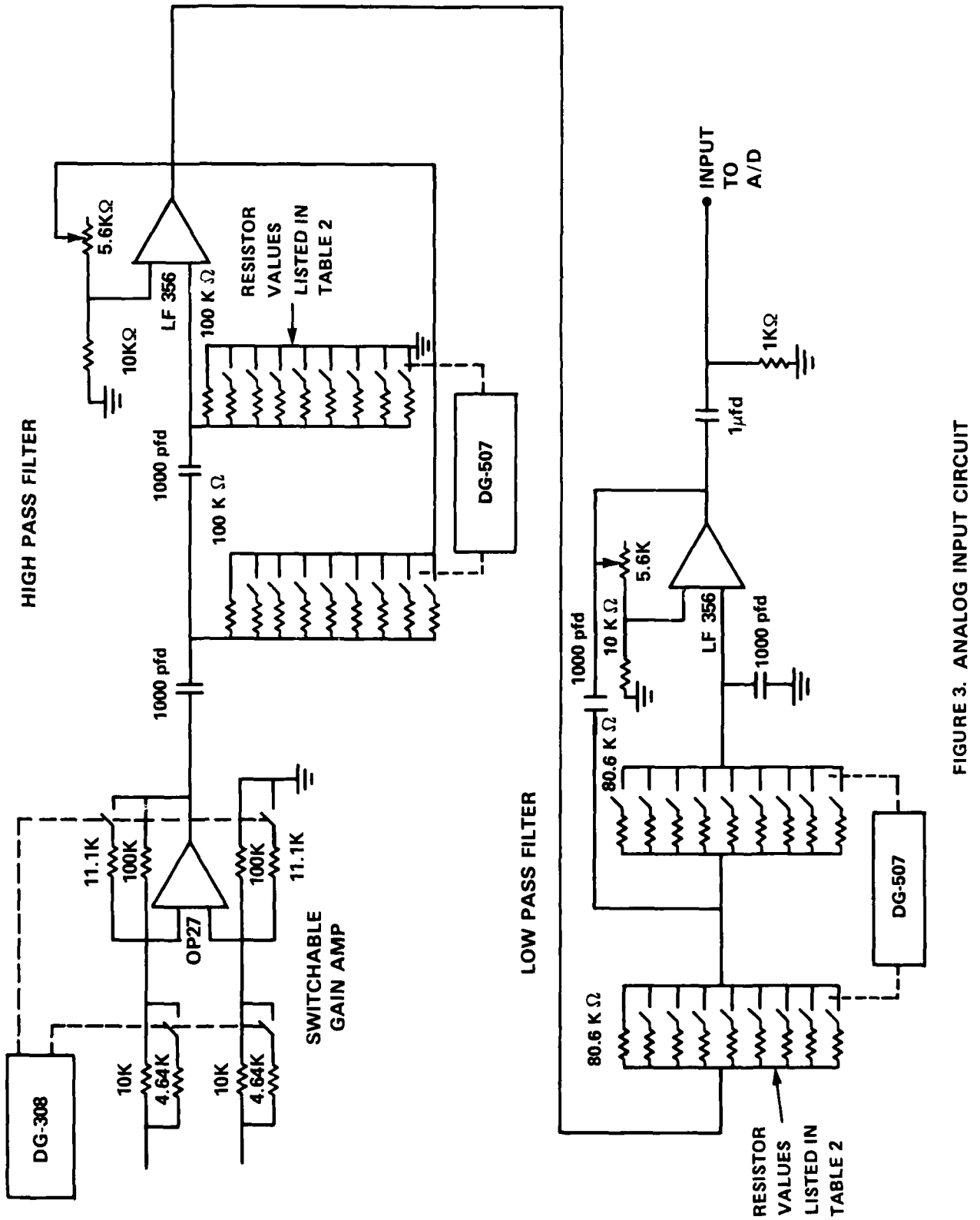


FIGURE 3. ANALOG INPUT CIRCUIT

CHAPTER 3

DIGITAL CIRCUITS

CLOCK CIRCUIT

The digital circuit of the AGC requires a synchronous clock to form the basis of the timing logic. Since the signal sample rate is set at 50 kHz, it is necessary to subdivide all of the required functions within a 20 μsec period. By providing 16 pulses within the 20 μsecs (800 kHz), all of the system's requirements are satisfied. (Schematic is shown in Figure 4.)

The 4520 synchronous counter chips that are used in the AGC circuit clock specify 1.5 MHz as the highest frequency that may be used when +5 volts are used as the power source. Therefore, to use the available +5 volts and to interface the TTL logic of the A/D converter with the CMOS logic, 800 kHz was chosen as the oscillator frequency. Using an 800 kHz oscillator requires that the oscillator pulses be used as part of the timing controls. It is not possible to have the oscillator output synchronous with the remainder of the clock pulses. However, the difference is constant within 250 nanoseconds, and does not create any timing problems.

A CMOS oscillator (Motorola K1152A) provides the necessary 800 kHz output used as trigger pulses on the "enable" inputs of the 4520 counter chips. The clock input on the chips acts as the "enable" for the chip. By reversing the enable and clock function on the 4520 counter chip, the trailing edge of the oscillator pulse causes the counter to increment. This technique allows the oscillator pulses to be used as part of the clock.

On the first stage (first 4520 chip), the clock input is permanently held low. Holding the enable low on the first stage allows the counter to maintain a constant time difference between the oscillator and clock chips without the time differences accumulating. On the remaining three stages, the previous clock pulses are supplied to a NAND gate which pulls down the clock input and "enables" the counter to increment the next oscillation trailing edge.

The first four counter outputs plus the oscillator output are used exclusively to manipulate an individual sample taken from the A to D converter. The remaining ten counter outputs (1024) are used for addressing the RAM storage which delays the signal for a discrete time period. The time period is variable in ten discrete steps from 10 to 20 milliseconds. The delay is varied by using the reset function of the three counter stages used for the RAM address. The ten address outputs are switched into a set of two NAND gates which, after the desired delay, generate a reset pulse and initialize the address.

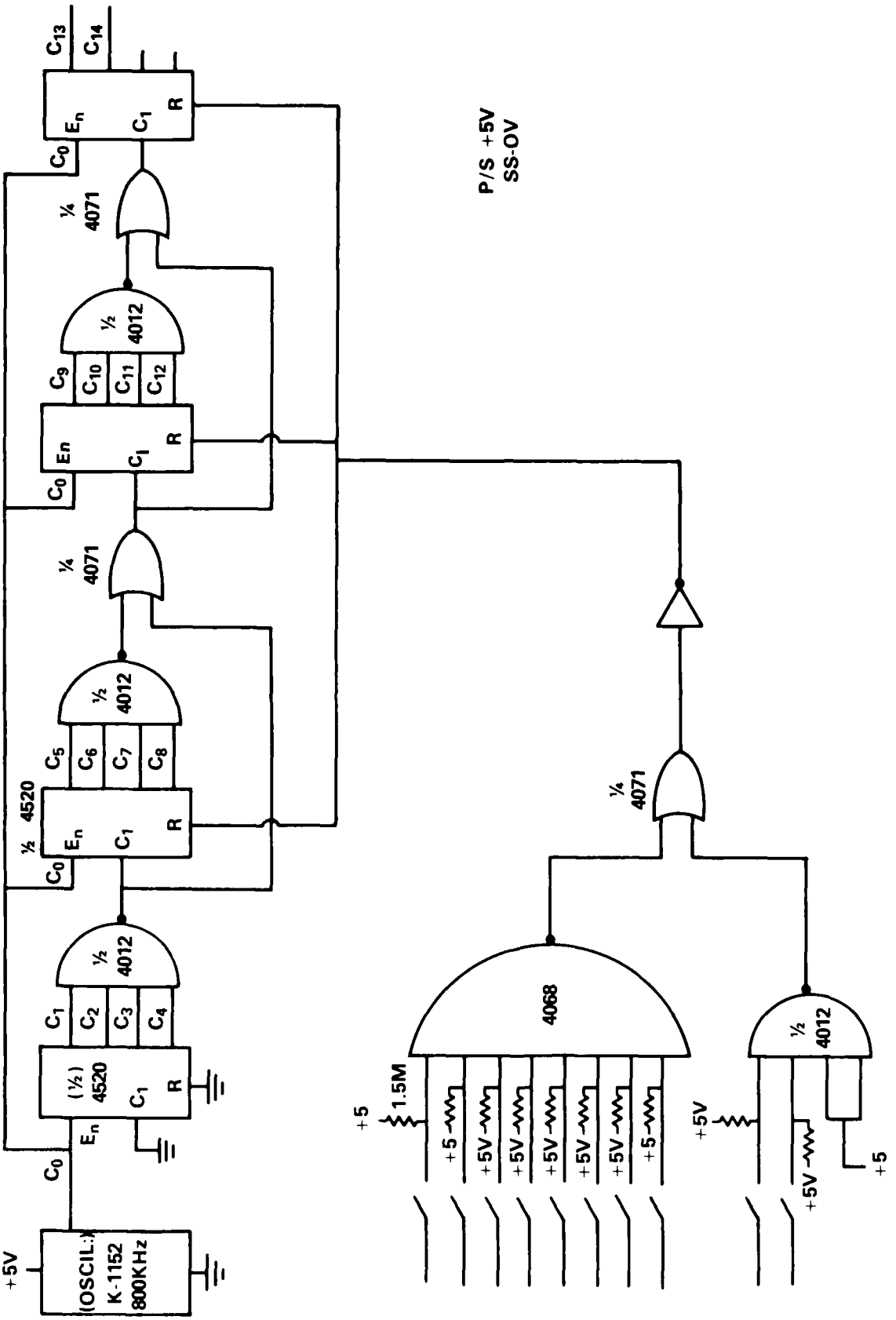


FIGURE 4. SYSTEM CLOCK CIRCUIT

Each input to the NAND gate is connected to +5 volts through a 1.5M ohm resistor. The +5 volt switch scheme works since the counter output is a low impedance and the NAND gate input is a high impedance. Consequently, with the switch closed, the +5 volts are dissipated across the 1.5M ohm resistor, and the counter output line determines the NAND gate input. With the switch open, the drop across the resistor is negligible, and the input to the NAND gate is held "high." To obtain a desired time delay, the appropriate switches are opened holding these inputs constantly high, and the reset pulse is generated.

Any delay up to 20.48 milliseconds in increments of 20 microseconds is possible by changing the proper mix of open and closed address line switches. The ten individual switches that open the address line inputs to the NAND gates are mounted on the timing circuit board. External on the AGC front panel is a rotary switch which can close a sequence of a distinct set of six switches that are set in the open position on the internal switches. There is a default rotary switch position where the six address lines connected to the rotary switch remain open. In the default position, all delay is controlled by the internal switches. Each of the remaining 11 switch positions close a unique subset of the six address lines connected to the reset pulse NAND gate. The 11 possible delays occur in approximately 1 millisecond intervals from 10 to 20 milliseconds. The incremented switch time of the address lines connected to the rotary switch is given in Table 3.

TIMING CIRCUIT

The first four counter outputs and the oscillator output "free run" within the 20 microsecond interval and are combined in various sets to create the timing pulses necessary to manipulate the digitized input signal. (See the timing circuit schematic in Figure 5.) The current sample is received, digitized, and stored while the delayed digitized sample is shifted (a gain is applied) and output to a D/A converter. The process is repeated simultaneously on all channels.

At the start of the 20 microsecond period, a 1.25 microsecond pulse is generated to place the address registers of CMOS RAMs in a high impedance state. The 6514 CMOS RAMs require that address information be latched into the RAMs's registers by the falling edge of the enable input for every address change. The CMOS RAM enable inputs correspond to the Chip Select Input of the NMOS 2114 RAM. While it is not necessary to reset the chip select on the 2114 with each address change, it is necessary on the pin compatible 6514 CMOS RAM.

The enable pulse for the RAM address is generated by NOR gating the first four counter outputs. Since the address change is only dependent on the falling edge of the pulse, the leading edge is not required to occur simultaneously with the oscillator pulse. In addition, the same enable pulse is used to allow an AND gate to pass the clock oscillator pulse occurring 625 nanoseconds into the period.

TABLE 3. TIME DELAY ASSOCIATED WITH PANEL SWITCH POSITION

Switch Position	Panel Delay Reading (msec)	Actual Delay (msec) (Calculated)
1	Default	Internal SW. control
2	10	10.24
3	11	10.96
4	12	11.92
5	13	13.12
6	14	14.08
7	15	15.04
8	16	16.00
9	17	16.96
10	18	18.00
11	19	18.96
12	20	20.16

The leading edge of the aforementioned pulse is used to trigger a dual monostable (one-shot) pulse generator (74123) that controls the signal's A/D conversion. The TTL pulse generator requires a minimum trigger pulse duration of 100 nanoseconds. A 6 microsecond pulse is generated by the leading edge of the trigger. The inverse output (Q1) is used as a sample control pulse that allows the sample and hold to track the input signal. The rising edge of the sample control pulse is used to trigger a 1 microsecond start convert pulse. The trailing edge of the start convert pulse initiates the A/D conversion process. The 1 microsecond delay is necessary to settle the sample and hold output after the tracking is stopped.

For both the 6 and 1 microsecond pulses, it was necessary to deviate from the theoretical R-C values. The 6 microsecond pulse required a 22K ohm resistor in place of the 20K ohm resistor theoretically calculated for use with the 1,000 pfd capacitor. The 1 microsecond pulse required 12.1K ohm resistor in place of the 10K ohm resistor calculated for use with the 271 pfd capacitor. Both the 6 and 1 microsecond pulse durations are minimum requirements for the A/D converter to meet the manufacturer's specifications.

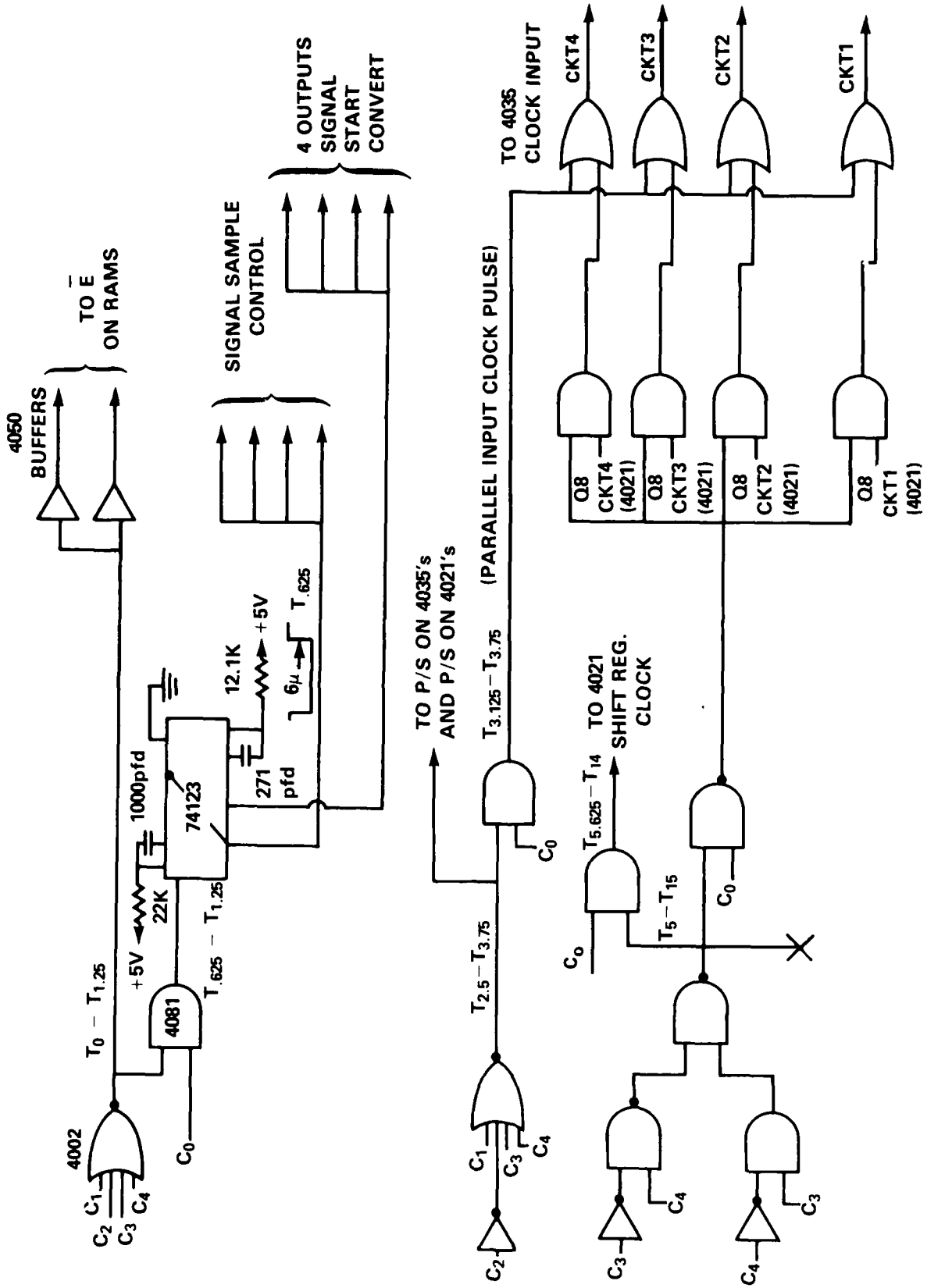


FIGURE 5. TIMING LOGIC CIRCUIT

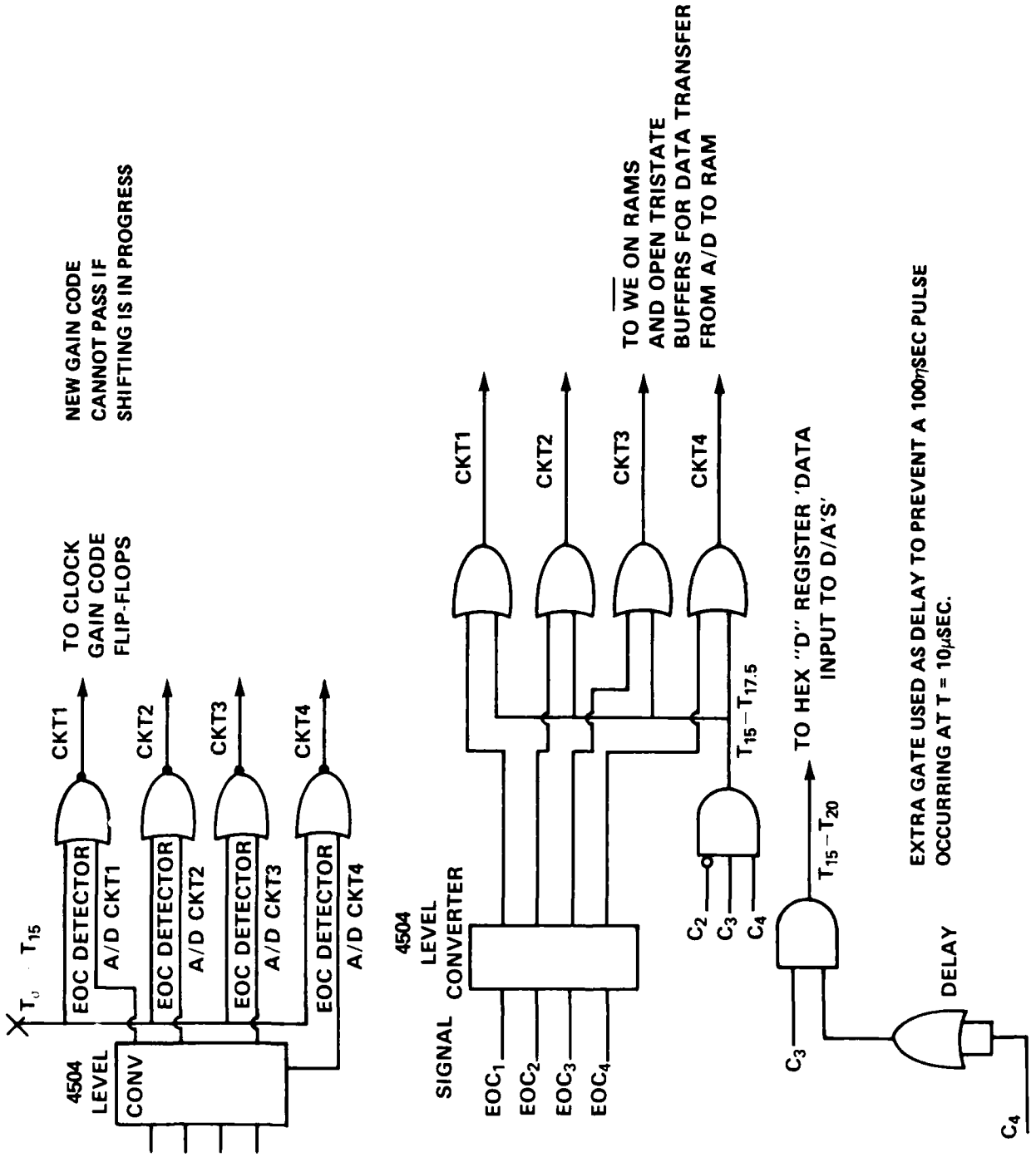


FIGURE 5. TIMING LOGIC CIRCUIT (CONT.)

The other timing pulse involved with the signal conversion process occurs 15 microseconds into the period when four OR gates (one for each channel) are enabled for 2.5 μseconds. The end of convert pulse goes low resulting in a low output on the RAM write input and on the tristate buffer (4503) registers on the input-output lines of the RAMs. The signal data is then written into the RAM. Each channel is activated by its own end-of-convert (EOC) pulse.

Since the EOC pulse is a TTL level pulse, it is processed through a TTL-CMOS Level Converter (4504) prior to generating the write pulse (actually a write bar; negative logic pulse). Also, each output is passed through a pair of buffers (4050's) prior to the $\overline{WE}$ RAM input. (CMOS devices cannot drive more than two TTL devices.) The RAM address lines are also passed through buffers (4050's) for this same reason.

Prior to the write pulse and after the enable pulse (negative logic), the delayed digitized signal sample is on the RAM's input-output lines. Therefore, 2.5 μsecs after the address changes, a 1.25-μsec pulse is generated (using a four input NOR gate) that places the shift registers into the parallel input mode. The seven-bit gain code is passed to its shift register (4021) by the leading edge of the pulse. The signal shift registers (3-4035's per channel) are only put into a parallel input mode by the pulse and require a clock pulse to actually cause the data to enter the shift register. Thus, the same parallel input pulse is used to enable an AND gate for one clock pulse. The leading edge of the oscillator clock pulse brings the data into the register.

From the 5 to 15 microsecond interval, a gate enable pulse for passing eight clock oscillator pulses is created. The 10 microsecond gate enables an AND gate for passing eight clock pulses to the gain shift register clock input. The gate also enables a NAND gate which inverts the pulse train during the gate period. The eight clock pulses delivered to each channel's gain shift register cause each bit of the seven-bit gain code to be passed in turn to the MSB output of the 4021 Shift Registers (Q8). Each channel's output from its gain code shift register enables an AND gate which will pass the inverted pulse train if the shift register output is high. The shift pulse output train to the signal shift registers from each channel's AND gate is multiplexed through a two input OR gate with the parallel input clock pulse previously described.

The trailing edge of the same 10 microsecond pulse passes the current output of the Gain A/D converter for each of the four channels, to a set of registers. If a conversion is in progress, the EOC pulse prevents the data from being transferred until the conversion is complete. The "enabling" by the EOC pulse from the gain A/D is accomplished with a quad two input NOR gate, each channel having its own gate.

The final pulse required from the timing circuit transfers the "multiplied" (shifted) signal data to the D/A converters. The data is transferred from the shift registers to a set of data registers by the leading edge of a pulse occurring 15 μsecs into the sampling period. The AND gate combination of the 5 and 10 μsec pulse requires that the 10 μsec pulse be delayed long enough to ensure that the 5 μsec pulse is low. If the delay is not implemented, a 100 nanosecond glitch occurs at the 10 μsec crossing point. Although the clock is synchronous, the rising edge of the 10 μsec pulse turns on the AND

gate before the falling edge of the 5 μsec pulse can turn the same AND gate off. This is due to the difference in the slopes of the clock's leading and trailing edge such that the leading edge reaches a turn-on voltage level sooner than the trailing edge of the other pulse reaches a turn-off voltage level. The time difference is approximately 100 nanoseconds throughout the clock.

The logic chosen for most of the timing applications is based on optimum use of circuit board real estate rather than the most convenient gate. Thus, the exclusive OR for the 5 to 15 microsecond pulse is a combination of extra gates rather than a 4070 with three unused gates. Likewise, the parallel input gate uses a four input NOR gate because one gate remains from the RAM enable gating scheme. The delay necessary for the 1 microsecond pulse is accomplished with an OR gate left over from the implementation of the synchronous clock circuit. (Timing circuitry and the timing diagram are shown in Figures 5 and 6, respectively.)

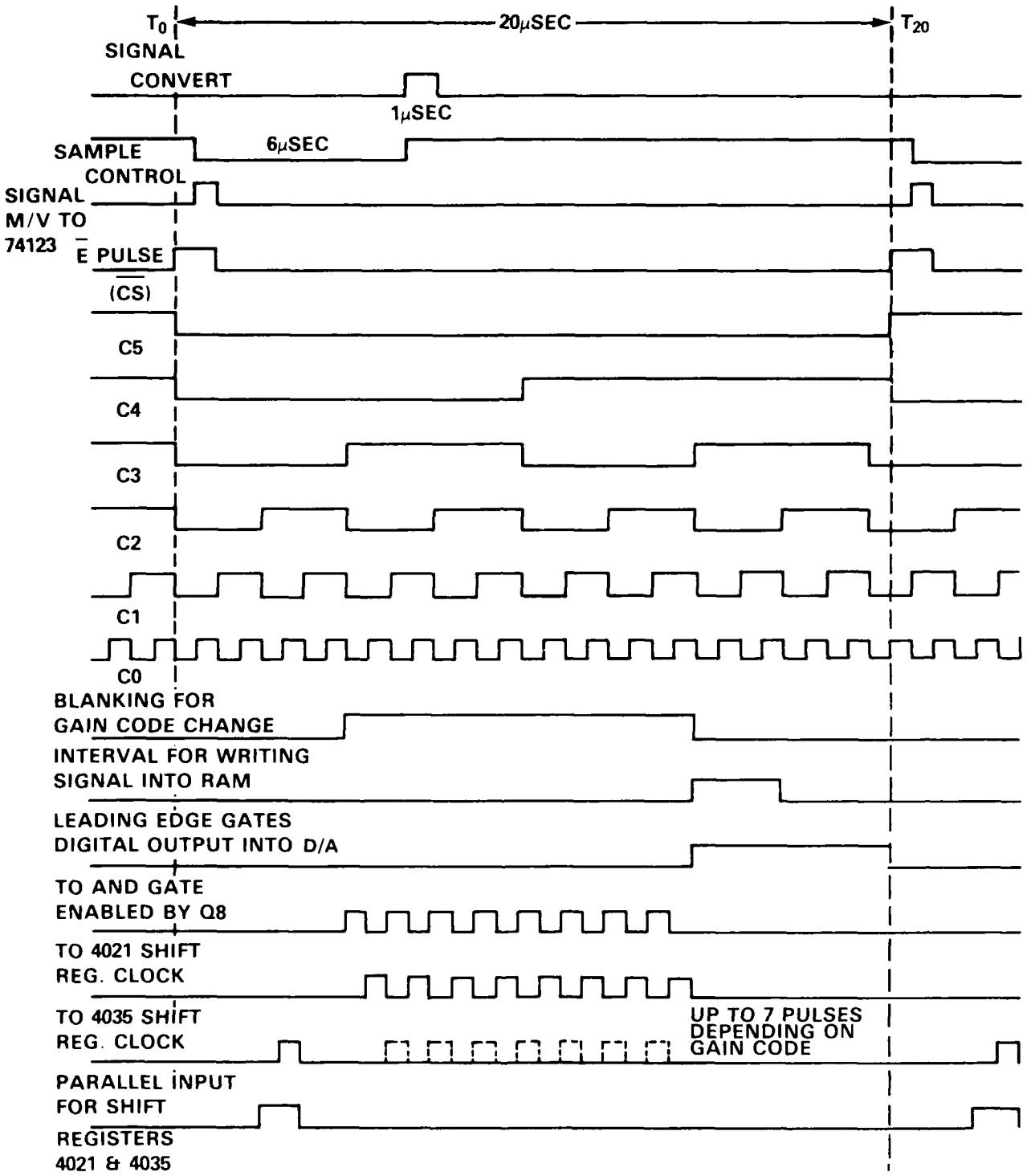


FIGURE 6. TIMING DIAGRAM

CHAPTER 4

SIGNAL PROCESSING

As previously described, the analog signal is tracked for 6 microseconds prior to being sampled. After allowing for a 1-microsecond settling time, the A/D conversion process begins. This process is initiated by the falling edge of the 1-microsecond settling pulse and takes a maximum of 9 microseconds. Therefore, approximately 16.6 &sec into the start of the sampling period, the data is transferred through a set of two tristate buffers (4503) into the RAM storage. Between the tristate buffers and the A/D converter are a set of TTL to CMOS level converters (4504's). Although the test circuits have never shown a missed bit, it is theoretically possible for a missed bit to occur. The minimum signal level from the A/D converter is 2.5 volts, while the minimum CMOS level for a guaranteed "1" is 3.5 volts. The level converters compensate for this inequity.

The new digitized signal data is entered into RAM (3-6514's per channel) deleting the delayed signal data that has been transferred to a set of shift registers (3-4035's/channel). Three 6514 RAM's in parallel are capable of storing 1,024 12-bit signals. Each consecutive address represents 20 microseconds between samples. The delay is determined by resetting the clock once a maximum address has been attained. The delay allows the signal strength to be processed so that a gain code (a train of shift pulses) can be determined and generated.

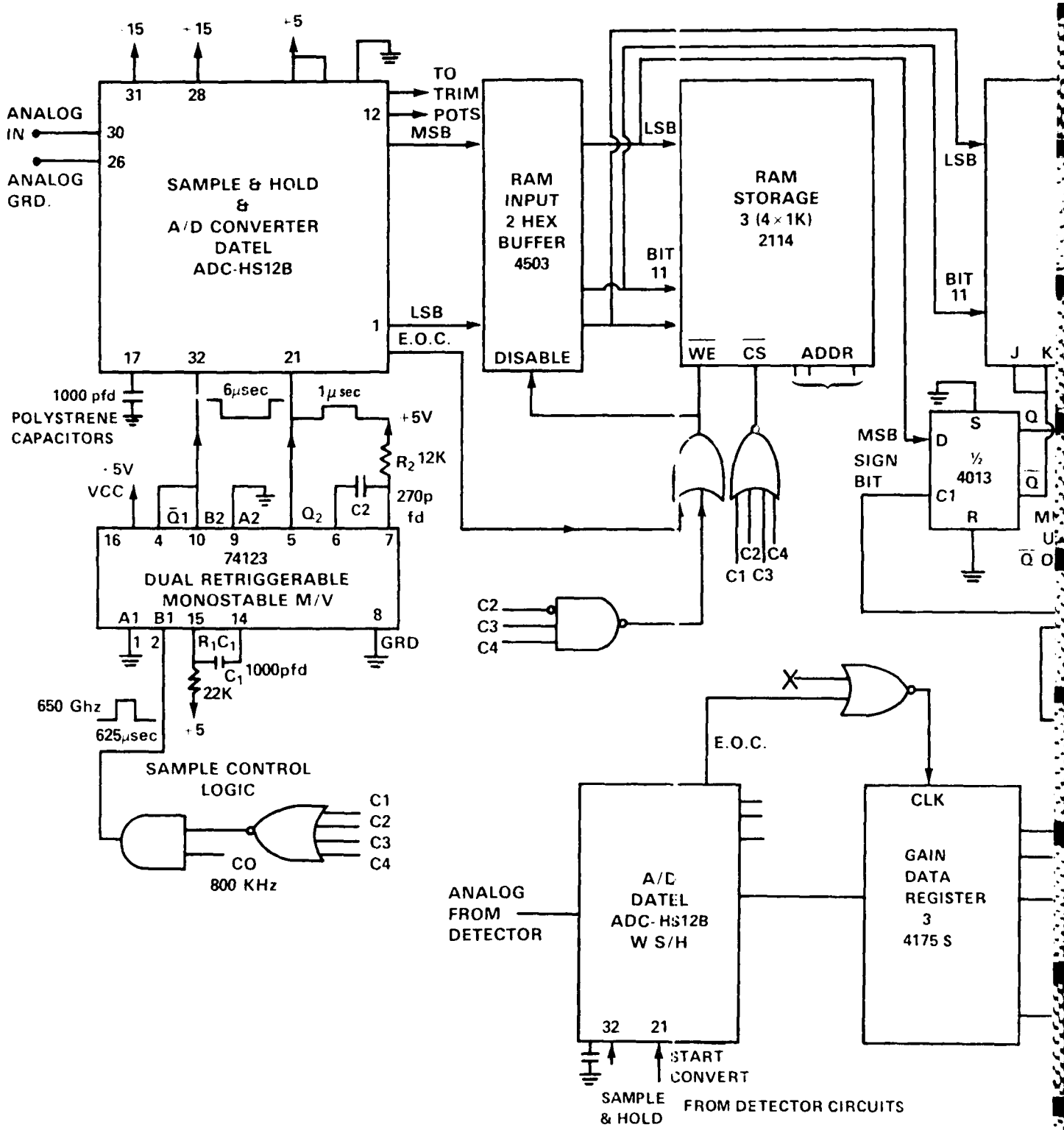
The signal's MSB is not transferred from the RAM to the shift register, but rather to a J-K flip-flop (4013). The parallel input pulse that causes the data to enter the shift register also clocks the MSB into the flip-flop. Since the signal is sinusoidal and the data is digitized in complementary offset binary format, the Most Significant Bit (MSB) is actually a sign bit and should not be shifted. The inverse of the sign bit is entered into the lowest shift register's serial J-K input. Because the magnitude of the signal is coded as 1's for negative voltage and 0's for positive voltages, making the serial input bit dependent on the sign bit is necessary to maintain symmetry. The binary digit added to the signal code when it is shifted up must be the opposite for a positive signal than that digit used for the negative signal.

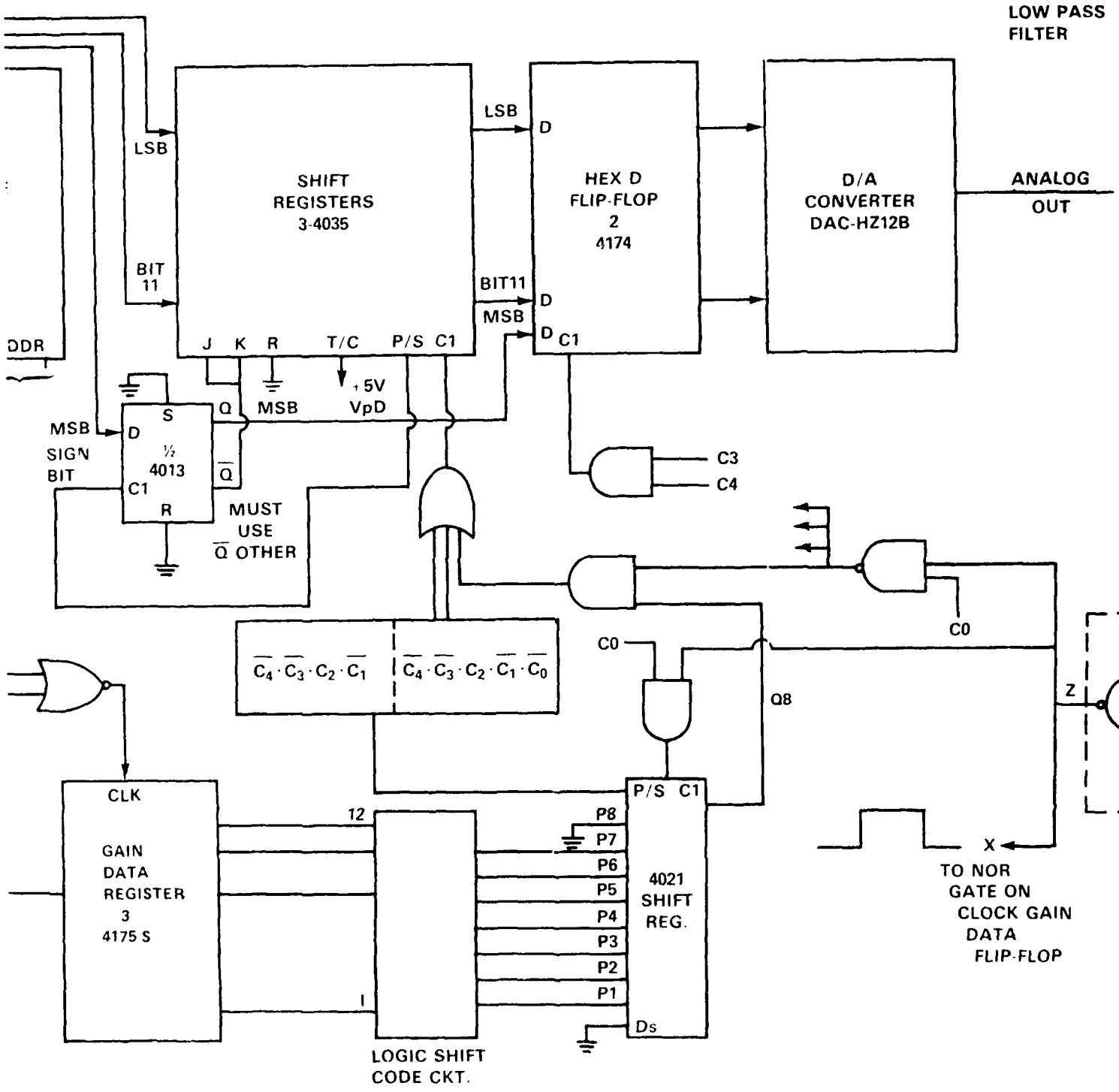
The shift register is clocked once for each bit in the gain code. The gain pulses are sequenced so that the shift pulses fed into the shift registers clock input occur as a group, i.e., the unit does not stop transmitting shift pulses and then restart on the same signal sample. In addition, the true/complement input of the shift register is permanently wired high and the reset input permanently wired low. The 2's complement logic that is input to the shift register is not changed within the shift register.

After the multiplication has taken place, the data is transferred to a data register. The transfer takes place 15 microseconds into the sample period. As soon as the data register is latched with the new data, the D/A conversion is initiated. Three microseconds settling time is required for the new data, but any transient spikes are easily eliminated by the smoothing filters. The D/A converter (DAC HZ12BMC) outputs a dc level for each code it receives. Therefore, the output of the converter is renewed every 20 seconds. A change in the level depends on the amplitude and frequency of the input signal. (The implementation is shown in Figure 7.)

The stairstep sinusoidal output of the D/A converter is passed through a four-pole, low-pass Butterworth filter. The filter smoothes the stairstep shape of the outputs into a sinewave. The low-pass, cut-off frequency of the filter can be switched to either 20 kHz or 5 kHz. A CMOS electronic switch (DG 384) is used to add the parallel resistors that make the cut-off frequency changes. When the output signal from the D/A has few level changes and the frequency is below 5 kHz, the 20 kHz filter output is still stairstepped. Switching to the 5 kHz cut-off frequency provides output smoothing for low amplitude, low frequency conditions.

In addition to the reasons previously stated for the input filters, the output filter requires gain to prevent a switching glitch from occurring during the transition at the zero crossing point. When the filter op amp is in a follower configuration, a switching glitch is present since the op amp's input protection diode effectively shorts the output to the input during the fast changes occurring during zero crossings. (The "gain" lifts the positive and negative levels away from zero, creating a rapid switch through the zero reference level.) Using the follower configuration requires a sample and hold on the output of the D/A converter. Rather than use an additional sample and hold, the filters with gain are used to eliminate the glitch. (The output circuitry is shown in Figure 8.)


-15
+15
+5
31
28
12
TO TRIM POTS
MSB
ANALOG IN
30
26
ANALOG GRD.
SAMPLE & HOLD & A/D CONVERTER DATEL ADC-HS12B
1
LSB
E.O.C.
17
32
21
RAM INPUT 2 HEX BUFFER 4503
DISABLE
LSB
BIT 11
RAM STORAGE 3 (4×1K) 2114
WE
CS
ADDR
LSB
BIT 11
J
K
1000 pfd POLYSTRENE CAPACITORS
6μsec
1μsec
+5V
R2 12K
-5V
VCC
Q1
B2
A2
Q2
C2
270p fd
16
4
10
9
5
6
7
74123
DUAL RETRIGGERABLE MONOSTABLE M/V
A1
B1
15
14
8
1
2
R1C1
C1 1000pfd
22K
GRD
650 Ghz
625μsec
+5
SAMPLE CONTROL LOGIC
C1
C2
C3
C4
CO
800 KHz
C2
C3
C4
C2 C4
C1 C3
MSB SIGN BIT
S
D
½ 4013
C1
R
Q
Q
X
E.O.C.
ANALOG FROM DETECTOR
A/D DATEL ADC-HS12B W S/H
CLK
GAIN DATA REGISTER 3 4175 S
32
21
START CONVERT
SAMPLE & HOLD
FROM DETECTOR CIRCUITS



)R CIPCUITS

FIGURE 7. SIGNAL PROCESSING LAYOU

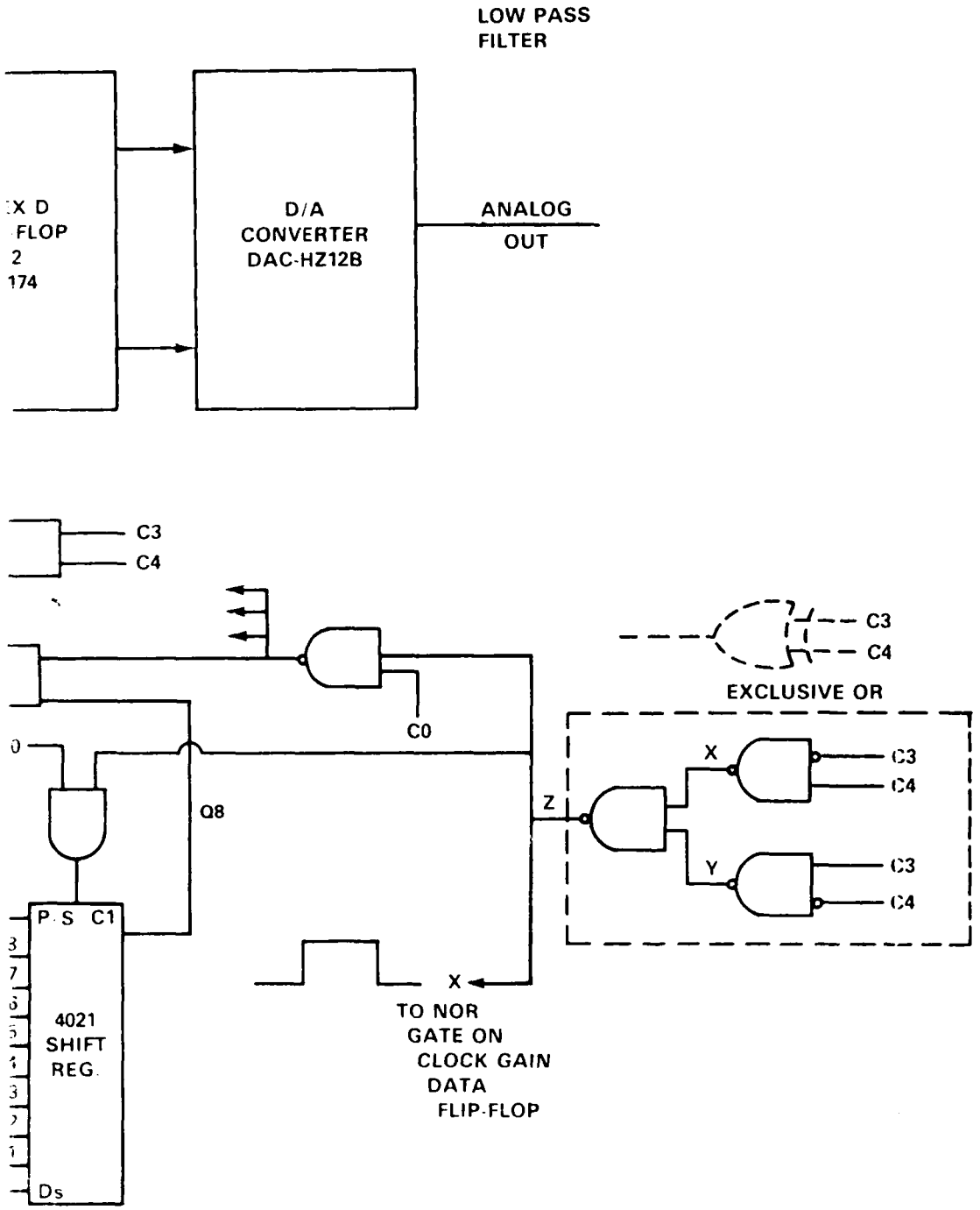


FIGURE 7. SIGNAL PROCESSING LAYOUT

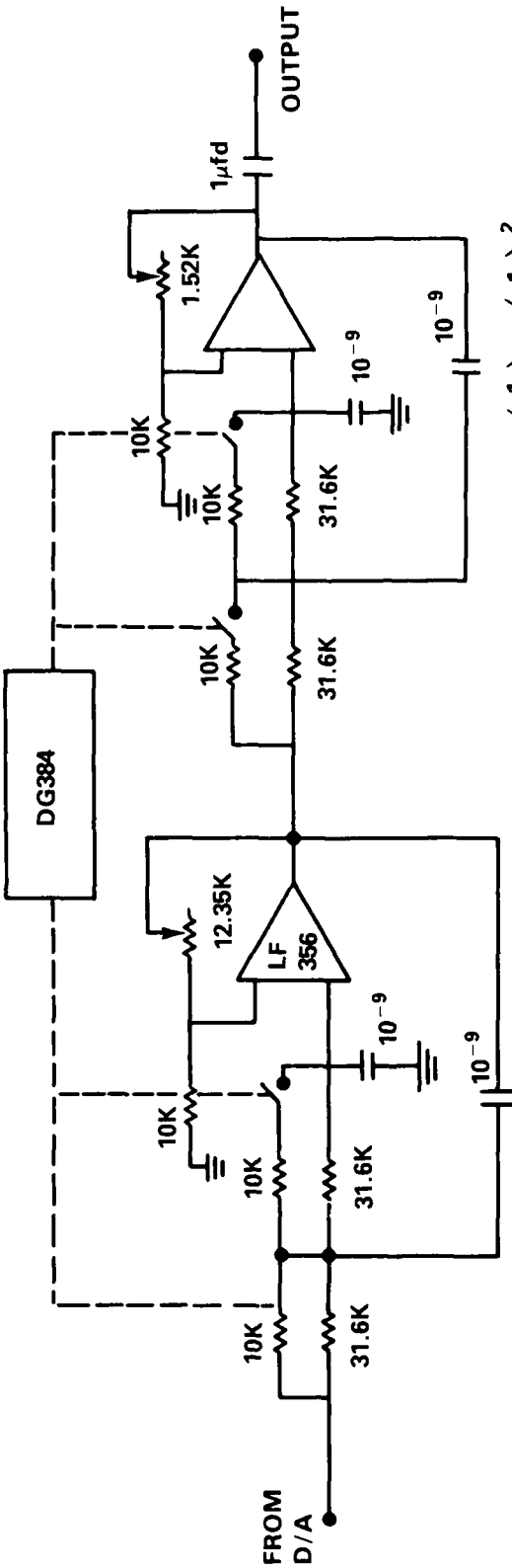


FIGURE 8. ANALOG OUTPUT CIRCUIT

CHAPTER 5

GAIN CIRCUIT

The purpose of the delay circuits is to allow time to determine a suitable gain to apply to the input signal. Consequently, the input to the signal A/D converter is also connected to a precision ac to dc converter (full-wave rectifier) (Figure 9). Two offset potentiometers, one on each op amp, are used to adjust the value of the inverted and non-inverted half-wave to equal values. All the resistors of the circuit are as closely matched to each other as possible. The first two op amps form an absolute value circuit whose output is connected to two parallel low-pass filters.

Both filters use gain and offset potentiometers to set a dc output level. The difference between the two filters is the speed of the rise time. The rise time is dependent on the cut-off frequency of the filter and both filters' (16Hz and 160Hz) cut-off frequencies are well below the expected received frequency. The level of the faster filter is adjusted to the peak of the full wave rectified sine wave outputting a dc voltage equal to the peak level. The gain potentiometer is used to set the level for large signals and the offset potentiometer sets the level for small signal inputs (50m Volts). It is necessary to repeat these adjustments because of interaction between the two settings.

The slow filter (16 Hz) is set so that its dc output level is slightly above the fast filter's output. Thus, when a signal (pulsed sine wave) is detected, the fast filter's leading edge rises above the slow filter's leading edge. Each filter's output is amplified and then compared against each other. When the start of a pulsed sine wave is detected, the change in balance between the two inputs to the comparator (LM-311) cause a +5 volt output pulse. The comparator output pulse sets into motion the circuit for setting a signal gain (shown in Figure 9).

The background noise, when no signal is present, can cause the slow and fast detector filter's output to trigger the comparator. Any crossing of the rising edges of the two filters' outputs causes the comparator to generate a trigger pulse. To distinguish whether the noise or a legitimate signal caused the comparator pulse, the pulse is passed to a decision circuit. The pulse duration of the comparator's output is the criterion used by the decision circuit to determine a legitimate signal pulse. Using the pulse duration as well as the difference between the steady-state outputs of the slow and fast filters for the determining detection allows the sensitivity of the comparator to be increased. (The difference between the level of the steady-state outputs of the slow and fast detector filters can be set closer, which then generates a detection pulse for lower-level signals.)

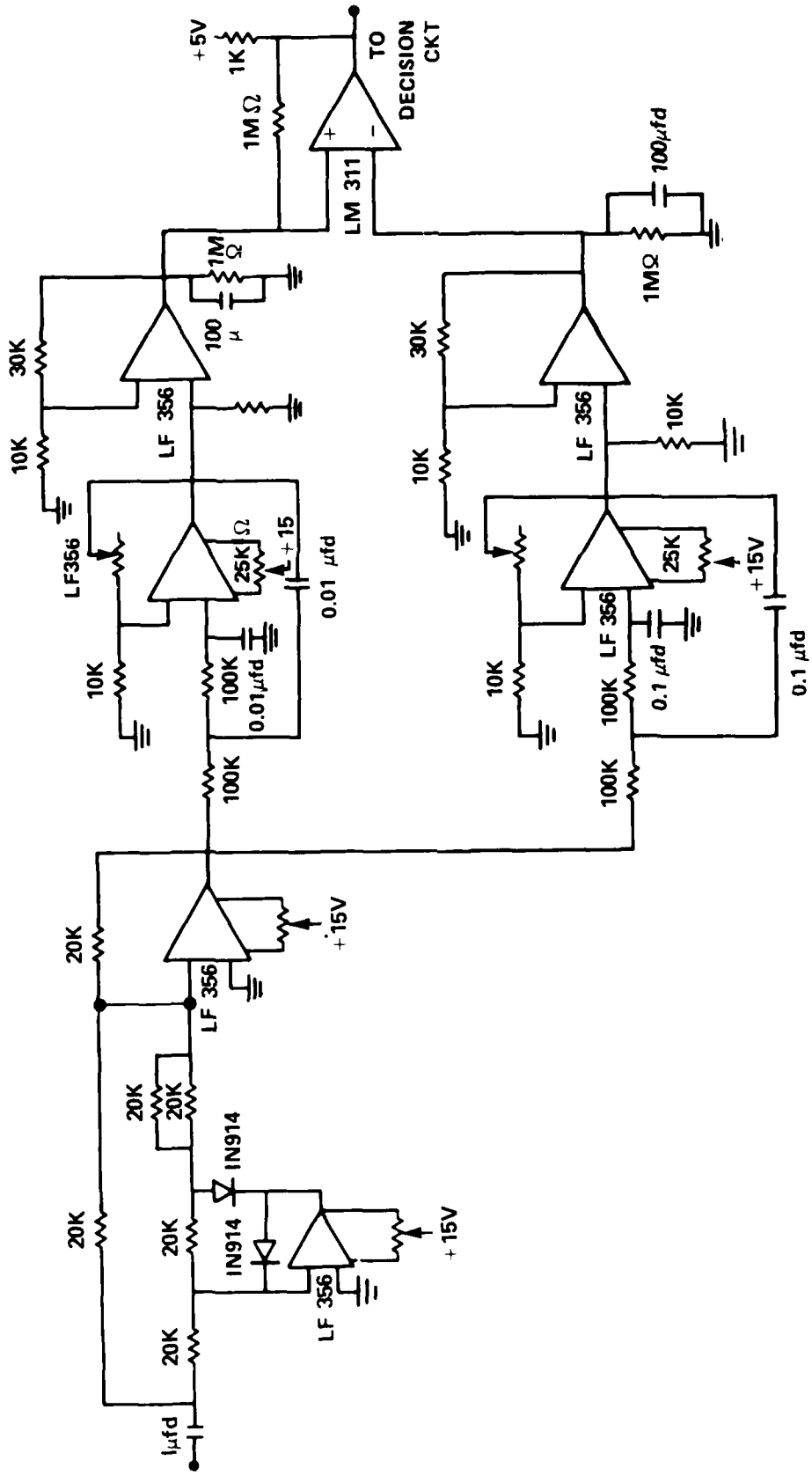


FIGURE 9. PRECISION A.C. - D.C. CONVERTER CIRCUIT

Initially, the leading edge of the received signal's envelope rising over the consistent background level provided by the slow filter was thought to be all that was necessary. Using the inputs from a signal generator, the circuits performed as expected without any false alarms. The slow filter's output level was set at 10 mV above the fast filter's constant signal level with a steady-state input signal level of 100 mV peak. With this sensitivity setting, the AGC performed as expected for all voltage ranges of the pulsed input signal.

However, when tapes of received signals recorded during previous tests were played into the AGC, the large number of false alarm triggers destroyed any distinction between the real pulse and the extraneous rise and fall of the background noise. Desensitizing the comparator by increasing the difference between the slow and fast filter's steady-state output level eliminated some of the false detections but not enough to avoid rendering the AGC circuit useless for lower level signals.

The background noise on the tape recorded signals caused both filters' outputs to vary erratically. Lowering the cut-off frequency smoothes the output but it also dramatically slows the envelope's rise time. Consequently, both desensitizing the comparator and slowing the filter response were eliminated as possible solutions.

Although the tape recorded signals and noise were amplified, the tape signals were used to validate the decision circuit design. This same tape includes a very strong direct path signal and a much weaker reflected signal that is received approximately 1 second after the reception of the direct path signal. By having a strong signal followed by a weak signal, the gain code change and the reaction of the AGC to diverse signal levels could be evaluated.

The sensitivity of the comparator can remain, as originally intended, with a narrow difference between the steady-state level outputs of the slow and fast filter. The rise time of the filters can also remain the same by using the digital pulse length decision circuit shown in Figure 10. The circuit ensures that the comparator's output remains high for a reasonable period of time before allowing a gain sample to be taken.

When the comparator's output goes high (positive), the rising edge of the pulse clocks a 4013 CMOS J-K flip-flop high. The D input of the flip-flop is permanently wired high, while the comparator's output is applied to the flip-flop clock input through an AND gate that is enabled by the inverse output (Q) of the same flip-flop. Once the flip-flop is clocked, the disabled AND gate will prevent additional clock triggers (comparator output pulses) from passing until the flip-flop is reset. The output of the comparator is also applied to an R-S NAND Latch (4044). The output of the NAND R-S Latch will follow the Reset (R) input as long as the Set (S) input is low. Once the S input goes high, the R input must remain high in order for the output to remain high. If the R input goes low, once the S input is high, the output will remain low regardless of any change in the R input.

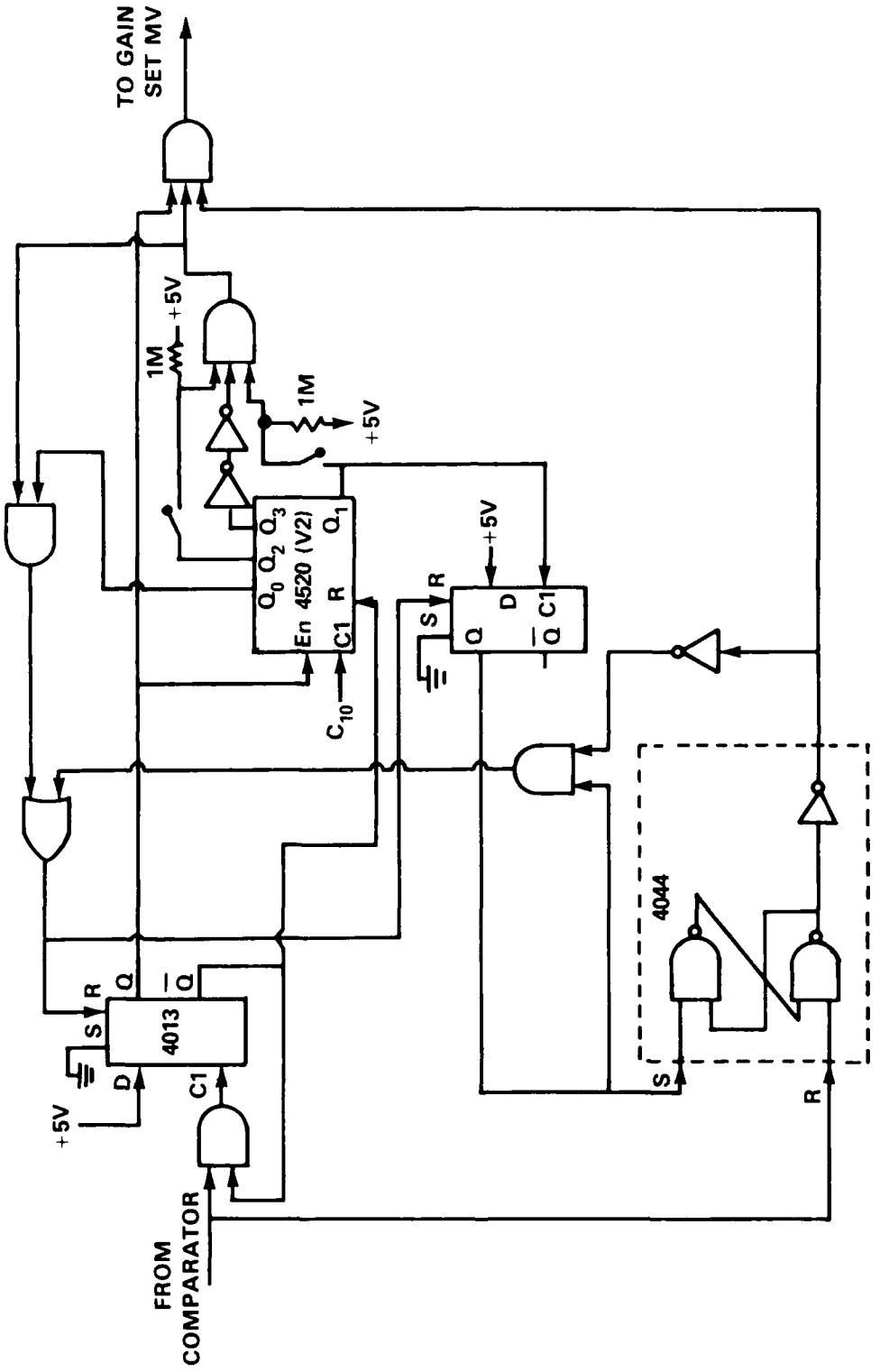


FIGURE 10. DECISION LOGIC CIRCUIT

The Q of the aforementioned flip-flop also is connected to the reset input of a 4520 CMOS counter chip. Prior to a signal being clocked into the flip-flop, the high output of Q holds the counter in the reset mode. Once the flip-flop is clocked, the Q goes low and the counter starts to time the comparator's output pulse. The rising edge of the master synchronous clock's 320 microsecond pulse (C10) is used as the auxiliary counter's clock input while the positive output of the flip-flop acts as the enable pulse for the counter. Initiation of the counting can take place anywhere within a 640 microsecond window between the rising edges of the main counter's output. As well as this random delay, an additional 640 microsecond intentional delay occurs prior to the R-S latch being locked (S input goes high). Although these time delays may seem long, the additional counter chip required to shorten the delay did not aid the circuit's decision process.

After the R-S latch is locked, the counter continues to increment unless a reset pulse to the flip-flop causes the Q1 of the flip-flop to reset the counter. A reset pulse to the flip-flop is initiated by either the R-S latch output going low, once S is high, or completion of the preset time period required to validate a pulse. The Q1 (second output) pulse, occurring 640 microseconds after the start of the counter, is used to clock a second flip-flop (the other half of the 4013) which locks the R-S latch (holds the S input high), the Q1 pulse also enables an AND gate that will pass a reset pulse to the flip-flops should the R-S latch output go low. The same reset pulse also resets the flip-flop providing the S input to the R-S latch.

Unless a reset pulse is generated, the counter continues incrementing until a preset time period of either 4.48, 5.76, 7.04, or 8.32 milliseconds has elapsed. After the preset time period has elapsed, a positive (high) trigger pulse is passed to the one-shot multivibrator circuit which initiates the gain code process for the received signal. If the R-S latch remains high, the pulse duration will be 640 microseconds, more than adequate to trigger the multivibrators. The pulse is generated by AND gating the appropriate counter outputs with the latch circuits. The fourth counter output (Q3) is delayed prior to the AND gate in order to prevent a false trigger from occurring during the transition of either the third or second counter output going low while the fourth counter output goes high. The third (Q2) and second (Q1) counter inputs to the AND gate can be switched using a system identical to the one used for the main clock reset. The output of the AND gate enables another AND gate which passes the first counter output (Q0) to reset both the flip-flop and re-initializing the decision circuit (shown in Figure 10.)

Without a signal applied, the input noise is sampled and a gain based on the received noise level is used. The sample time period results from the clock's reset pulse being input to a counter (4520) and a preselected counter output causing the generation of a sample pulse to the gain A/D. Any one of the eight outputs of the counter may be manually selected. Up to 5.12 seconds between noise samples is possible. (The reset time is between 10 to 20 milliseconds, and the selectable outputs of the counter are 2 to 256 times the reset period.)

The counter output is gated to a one-shot multivibrator (74123), one for each channel. The gate is used to prevent the counter pulse from generating its sample pulse while a signal is being processed. A 25 microsecond sample pulse is generated and sent to the gain A/D sample control input. The trailing edge of the noise sample pulse triggers another one-shot multivibrator (74123, one for each channel) generating the 1 microsecond start convert pulse for the gain to A/D converters.

When a decision circuit pulse occurs, resulting from the start of a received signal, a separate one-shot multivibrator is triggered. The multivibrator (the other half of the noise sample control pulse multivibrator) generates a pulse that disables the AND gate for the noise sample control trigger and the AND gate used to pass the initiating decision circuit pulse. The pulse duration is manually set to either 0.16, 0.5, 0.75, 1.0, or 1.5 seconds. The pulse prevents additional comparator pulses from regenerating (lengthening the pulse) and ensures that only one gain will be realized by the signal throughout the duration of the pulse.

The decision circuit pulse also triggers another one-shot multivibrator which creates a signal sample control pulse for the gain A/D converter. (Once again each channel has its own signal control pulse multivibrator.) Unlike the noise sample control pulse, the trigger sample control pulse tracks the signal envelope for 125 microseconds before generating the 1-μsec start convert pulse. The same multivibrator is used for both noise and signal start convert pulses.

Both the noise and signal sample control pulses are AND gated together before being input to the start convert multivibrator. Consequently, one continuous sample control pulse will result should the signal sample control pulse occur after the start of the noise sample control pulse. In addition, the start convert pulse is fed back to its own input, through an OR gate, to ensure the completion of the 1-μsecond start convert pulse should the signal sample pulse occur within the start convert's 1-μsecond pulse duration. The noise sample control is held high for at least 0.5 seconds after the signal sample control pulse starts. Therefore, it is not possible for the noise sample control to immediately follow the signal sample control. (The schematic for one channel is shown in Figure 11.)

Since each channel has its own gain A/D control pulse circuitry, one channel may be in the noise sampling mode while another channel is in the signal receiving mode. Thus, the gain A/D control pulse is independent for each channel and is initiated by its own channel's input. However, the signal A/D converter's control pulse generating circuitry, which digitizes the actual signal for processing, samples concurrently (the same pulse is used) on all channels.

Once the gain A/D converter has digitized the dc level output of the "fast" low-pass filter, either noise or signal, the data is transferred through a pair of CMOS level converters (4504) to a set of D flip-flops (3-4175's). The end of convert pulse from the gain A/D converter provides the rising edge for the data to be latched by the flip-flops. Both the 12-bit digitized dc input level and each bit's inverse is available on the output of the flip-flops.

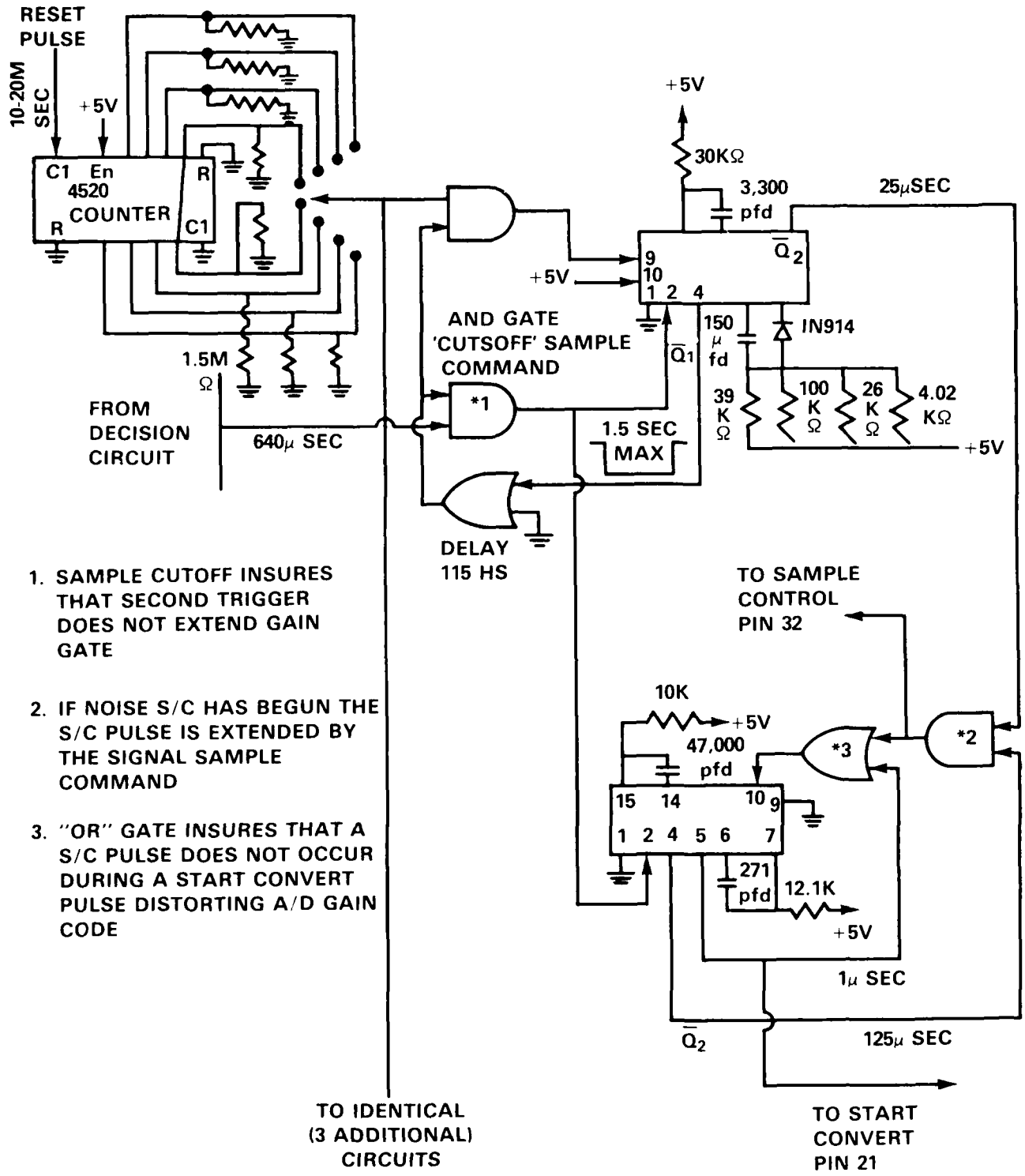


FIGURE 11. GAIN CODE TRIGGER CIRCUIT

Based on the dc input voltage, the digital logic generates a seven-bit gain code representing the seven possible gains. A pulse is generated for each 10 dB below a 5 volt reference level that the input is. However, care must be taken not to generate a shift pulse on the 5 volt transition. Shifting the same number of pulses as the transition point above (every 6 dB) causes the signal's MSB to be arithmetically shifted out of the code. For the shift points used for the aforementioned code only the +5 volt shift point presents this problem. Therefore, the first shift pulse is generated below the +5 volt level. The gains for the input signal levels are listed in Table 4. (The schematic of the gain coding circuit is shown in Figure 12).

The gain pulses are passed in parallel to the gain shift register (4021) every 20 microseconds. The timing for loading the shift register is synchronized with the signal processing of the received input (noise or signal). The seven-bit gain code is non-alternating in that the number of gain pulses occur without skipping a pulse. The output of the shift register during its clocked period is a single positive pulse with a duration that corresponds to the number of gain pulses. Since a zero is initially put into register Q8 and zeros are transferred up as shifting occurs, the output of Q8 is zero unless the clock shifts up a gain pulse yielding a 1.25 microsecond positive (high) output. Each 1.25 microseconds of duration represents one gain code bit. The single pulse out of Q8 "enables" an AND gate to pass oscillator clock pulses that serially clock the signal shift registers. Each passed clock pulse corresponds to a high (positive) gain code bit. The clock pulses to the gain code shift register (4021) are the inverse of the signal shift register's (4035's) clock pulses.

TABLE 4. GAIN APPLIED VERSUS PEAK INPUT VOLTAGE

Voltage (peak)	Gain	Gain (dB)
5 V	1	0
1.58 - 5	2	6
.5 - 1.58	4	12
.158 - .5	8	18
50 mV - 158 mV	16	24
15.8 mV - 50 mV	32	30
5 mV - 15.8 mV	64	36
5 mV	128	42

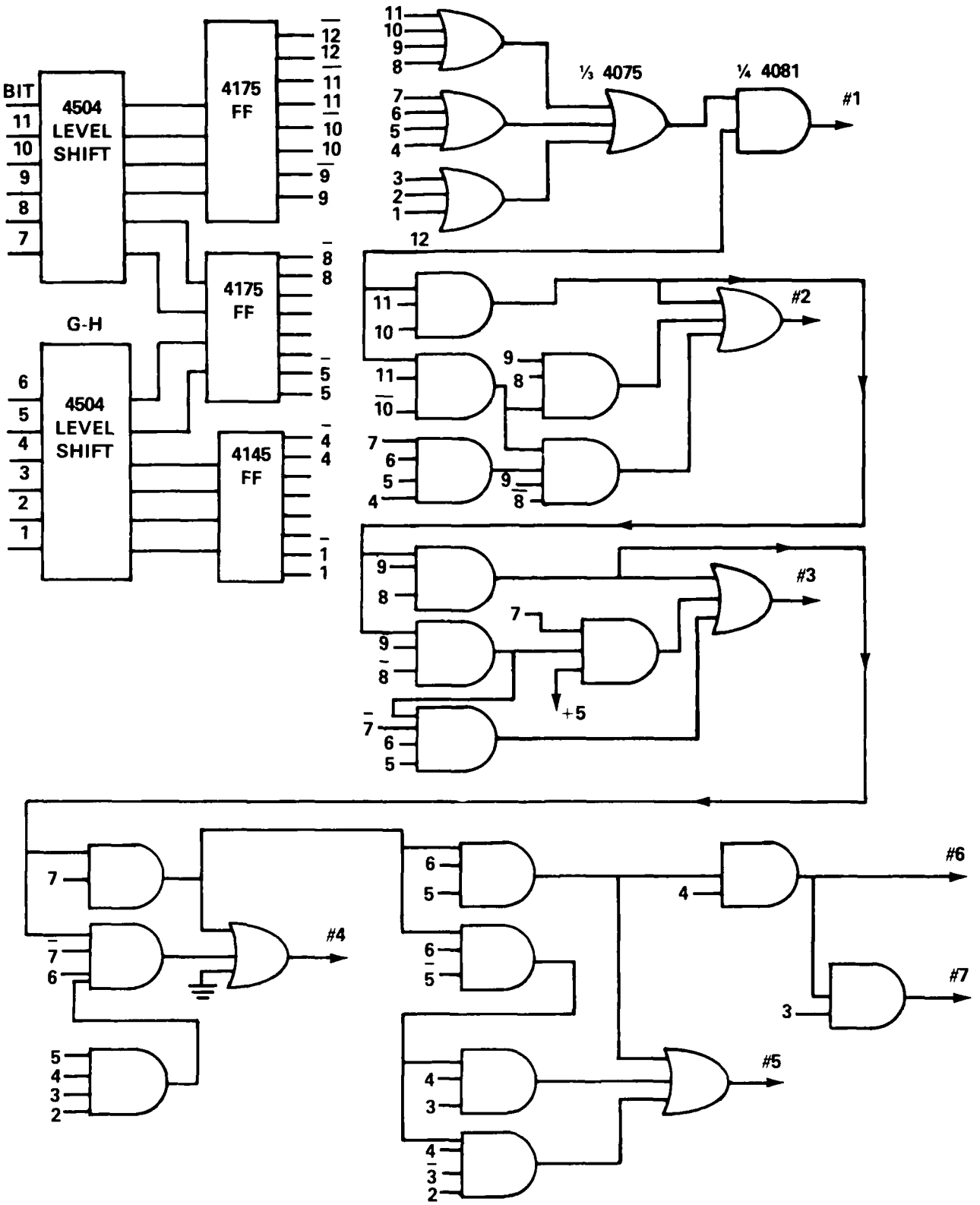


FIGURE 12. GAIN CODE LOGIC CIRCUIT

CHAPTER 6

GAIN CODE RECORD

The input of the signal shift register (4035) also clocks a counter (4520) every 20 microseconds. The three-digit representation of the gain code from the counter is stored in a hex D type flip-flop. (Actually, the code from two channels is stored in the same register.) The rising edge of the pulse that causes the digitized signal to be passed to the D/A converter also causes the gain code to be passed to the register.

The gain code that is passed to the register is not sampled every 20 microseconds. Because of the bandwidth constraints of the tape recorder (Honeywell 101), each channel is sampled for 0.64 millisecond every 5.12 milliseconds. In order to characterize the start and stop of the gain code, its information is blanked for alternate time periods of 2.56 milliseconds. As each channel's three-digit gain code is multiplexed to the output, it is weighted and summed by an op amp follower circuit. (CA3130 operated with a +5 volt supply.) The output of the op amp is a series of non-return to zero analog pulses, each representing the number of bits in gain code. Channel 1's output is defined by adding a 2.5 volt pulse to the value of the gain pulse. Consequently, Channel 1's gain code record output is at a level higher than any of the other channels. (The schematic of the gain code record circuit is shown in Figure 13.)

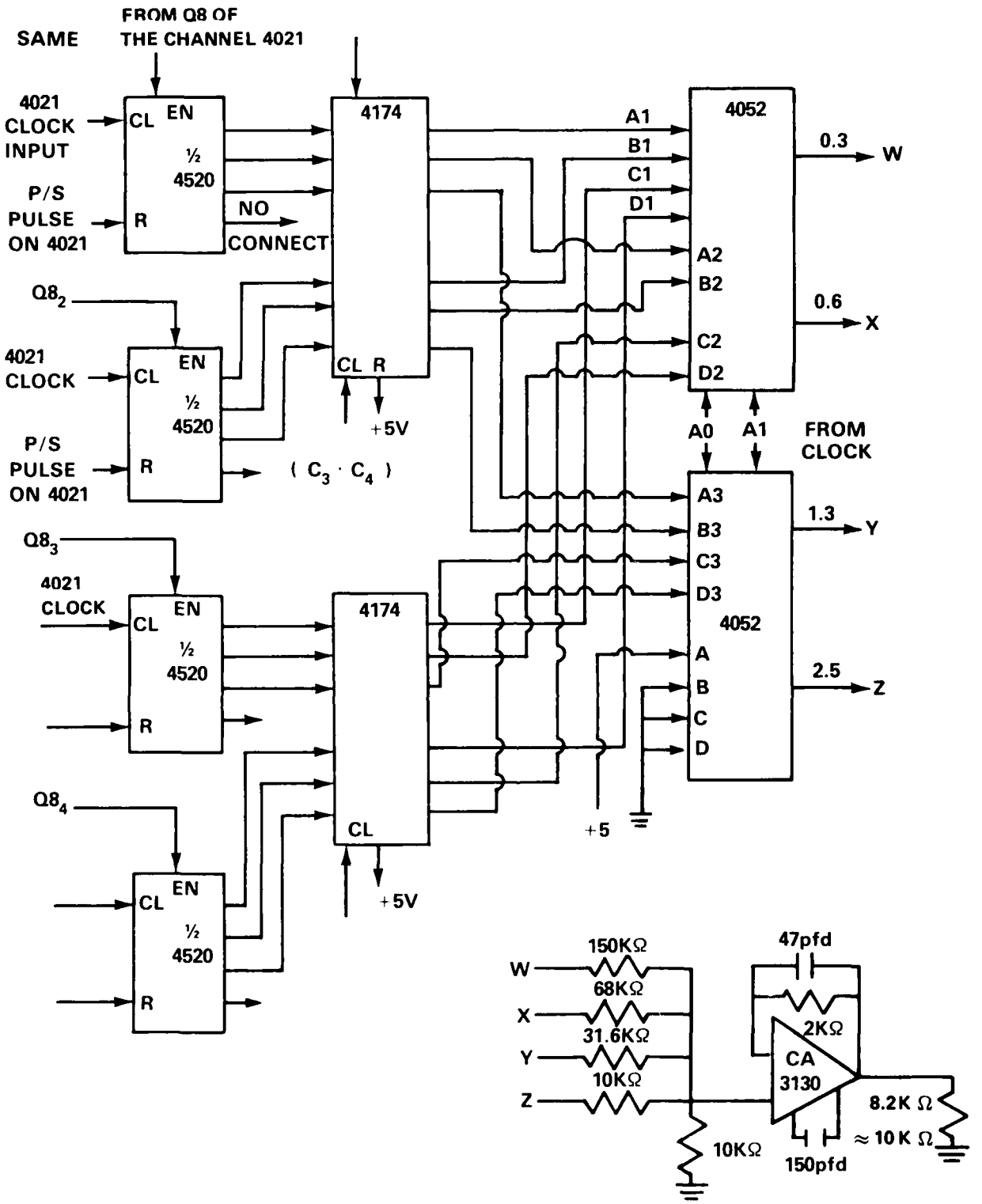


FIGURE 13. GAIN CODE RECORD CIRCUIT

CHAPTER 7

POWER SUPPLY

Three power supply voltages are required by the circuit, ±15 volts, and +5 volts. The only connection between the ±15 volts and +5 volts is through the ground plane on the four analog input boards. The analog input boards contain the A/D converters for the system.

Decoupling capacitors are liberally used for both the analog and digital circuits. In addition to using a 1-microfarad capacitor in parallel with a 0.01-microfarad capacitor at power supply (+15, -15, and +5 volts) inputs to the A/D and D/A converters, the same values are used at a rate of one set for every three op amps. Each power line (+15 and -15 volts) on the circuit board has a set of decoupling capacitors for every three op amps.

The digital circuit's +5 volt supply also requires decoupling capacitors. Pulses on the +5 volt supply line are caused by the A/D converter's internal clocks. The frequency of the internal clock is 1.5 MHz. (0.1-microfarad and 1-microfarad capacitors are used for the digital circuit.) Each RAM (6514) has a 0.1-microfarad capacitor placed as close as possible to it. The one-shot multivibrators with long pulse lengths also have 1 microfarad and 0.1-microfarad capacitors close to their inputs. These one-shot multivibrators with pulse lengths of 1.5 seconds to 160 milliseconds show noticeable changes in pulse length without the decoupling capacitor. For the 1.5 second pulse, the duration varied as much as 25 percent from pulse to pulse. As each decoupling capacitor was added, the noise pulses on the +5 volt power line decreased.

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